MULTI-LAYER ULTRA-WIDEBAND WILKINSON COMBINER FOR ARRAYS

A Dissertation

by

SEAN ARTHUR GOLDBERGER

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DOCTOR OF PHILOSOPHY

Chair of Committee,	Kai Chang
Committee Members,	Robert Nevels
	Steve Wright
	Mary McDougall
Head of Department,	Miroslav M. Begovic

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ABSTRACT

This work investigates an ultra-wideband (UWB), compact, and multilayer Wilkinson power combiners for tightly coupled array (TCA) designs. The Wilkinson topology designs encompass UHF, L-, and S-bands. These combiners integrate into an experimental UWB TCA. The experimental UWB TCA divides into twenty-four columns, with each column containing eight unit cells, and each cell one-inch square. The Wilkinson power combiner contains eight input ports and one output port. Twenty-four combiners mount to the TCA's back. The combiner condenses the two-dimensional array (8x24) to a one-dimensional or linear array (1x24).

The proposed Wilkinson power combiner possesses a multilayer design reducing common mode current problems caused by vias. The Wilkinson combiner covers 500 MHz to 3.28 GHz and provides a 6.56:1 bandwidth. It achieves tight impedance matching through stripline coupling. The proposed design provides minimal phase error, equal power reception, and low power handling. The power combiner interfaces with an experimental UWB TCA antenna through SMP snap connectors.

This paper examines signal combining efficiency to provide minimum path loss. This paper also examines interconnecting transmission lines traversing multiple laminate layers. This necessitates proper current handling because interconnects influence impedance, transmission, and isolation. Integrating a via picket fence improves port isolation and reduces propagating parallel plate modes.

The proposed combiner design achieved the following important attributes at or better than the minimum required specifications. The measured combiner design successfully demonstrated -7.8dB minimum return loss for input and -18.1dB return loss for the outputs; 10.92dB ± 1.28dB insertion loss; -12.2db minimum isolation; ± 1.38^{o} minimal phase error; ± 0.57dB power reception imbalance. The proposed UWB combiner design condensed the four-stage Wilkinson footprint to consume no more than 0.4in^2 (258mm^2) surface area, weighed only 1.5oz (42.5g), and less than a half-inch thick.

DEDICATION

This thesis is dedicated to my parents, grandparents, and sister.

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Contributors

This work was supervised by a dissertation committee consisting of Professors Kai Chang [advisor] and Professors Robert Nevels and Steven Wright of the Department of Electrical and Computer Engineering and Professor Mary McDougall of the Department of Biomedical Engineering.

Bit Systems provided the testing equipment, software, and computer equipment to complete this project. Jenn and David C. helped provide testing assistance and optimization. David C. designed the Wilkinson combiner test coupons. Roger at Bit Systems designed the Rev1 combiner.

The student completed all other work conducted for the dissertation independently.

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NOMENCLATURE

RF	Radio Frequency
SDR	Software Defined Radio
UWB	Ultra-Wideband
TCA	Tightly Coupled Array
AT&T	American Telephone and Telegraph
RCA	Radio Corporation of America
FM	Frequency Modulation
RFID	Radio Frequency Identification
TxDOT	Texas Department of Transportation
TV	Television
GPS	Global Positioning System
PCS	Personal Communication Systems
PB	Percent Bandwidth
RB	Ratio Bandwidth
ITU	Internal Telecommunications Union
IEEE	Institute of Electrical and Electronic Engineers
FCC	Federal Communications Commission
R&O	Report and Order
RADAR	Radio Detection and Ranging
SAR	Synthetic Aperture Radar
MIMO	Multiple Input Multiple Output

NASA	National Aeronautics and Space Administration
FOV	Field of View
CSA	Current Sheet Array
MIT	Michigan Institute of Technology
DoD	Department of Defense
USSR	Union of Soviet Socialist Republics
TEM	Transvers Electromagnetic
WLAN	Wireless Local Area Network
USARDL	United States Army Research & Development Laboratories
WPC	Wilkinson Power Combiner
QUCS	Quite Universal Circuit Simulator
MMIC	Millimeter Integrated Chip
LTCC	Low Temperature Co-fired Ceramics
DGS	Defected Ground Structure
EBG	Electromagnetic Bandgap
MCMLS	Multiple Coupled Microstrip Line Structure
LCP	Liquid Crystal Polymer
VSWR	Voltage Standing Wave Ratio
Rev1	First Combiner Design
CAD	Computer-Aided Design
PTFE	Polytetrafluoroethylene
EMI	Electromagnetic Interference

EMC	Electromagnetic Compatibility
FR4	Flame Retardant 4
VNA	Vector Network Analyzer
PPW	Parallel-Plate Waveguide
Rev2	Second Combiner Design
CTE	Coefficient of Thermal Expansion
NiP	Nickel Phosphorous

TABLE OF CONTENTS

Page

LIST OF FIGURES

Page

LIST OF TABLES

CHAPTER I

INTRODUCTION AND LAYOUT

I.A. Introduction

Commerce expansion increases demand to defy communication equipment limitations. Communicating with numerous mobile devices and connecting nomads together increases dependence upon wireless systems and strains them to their limits…Managing multiple radio frequency (RF) connections requires numerous receivers and transmitters with equal numbers of antennas localized in one area. New RF hardware meshes with RF spectrum allocations recruited for various commerce communication systems. These hardware improvements necessitate increasing capability, modularity, electromagnetic and environmental resilience, and decreasing size. Software defined radio (SDR) combines receivers and transmitters into one unit providing more capability and reducing cost. Interfacing with a SDR calls for new broadband antennas. An ultra-wideband (UWB) antenna consolidates numerous wireless standard frequency reception and transmission under one antenna rather than several antennas. A tightly coupled array (TCA) exploits inter-element coupling and provides a smaller profile and ultra-wide bandwidth costing less than a traditional array.

I.B. Thesis Statement

This work investigates Wilkinson power combiners for tightly coupled array (TCA) designs. The proposed Wilkinson power combiner has a multilayer design reducing common mode current problems, 3.75:1 minimum bandwidth, tight impedance matching, minimal phase error, equal power reception, low power handling, weighs less than one pound, and is less than or equal to 0.5 inches thick.

I.C. Dissertation Layout

Chapter II presents: communication history, defines bandwidth, array background information, some fundamental mathematics on the Wilkinson combiner including even and odd mode analysis, and covers Wilkinson power combiner advancement chronologically through published literature.

Chapter III presents operation problems from a problematic prior UWB Wilkinson combiner design attempt for a TCA.

Chapter IV discusses a successful solution to the UWB TCA combiner. Chapter IV includes TCA combiner design requirements, measurements from an industry-fabricated combiner, provides operation standards, combiner design strategy, signal combining efficiency, interconnecting transmission lines traversing multiple laminate layers, and in-depth UWB combiner design discussion, simulations, and measurements.

Chapters V and VI provide concluding thoughts and future enhancements.

CHAPTER II

BACKGROUND AND LITERATURE REVIEW

II.A. History Demonstrates Commerce Motivates Communication

The Creator gave Man freewill. Freewill grants Man unhindered thinking. Man freely expresses unhindered thought through unrestricted speech. Thus, Man's unrestricted speech became an inalienable right endowed by their Creator. Man's open communication with one another and their Creator distinctly separates us from other species found in nature. Thus making open communication a fundamental liberty desired and sought by all men. Fig. 1 graphically depicts Man's development of communication through history beginning with the Greek Empire through present day.

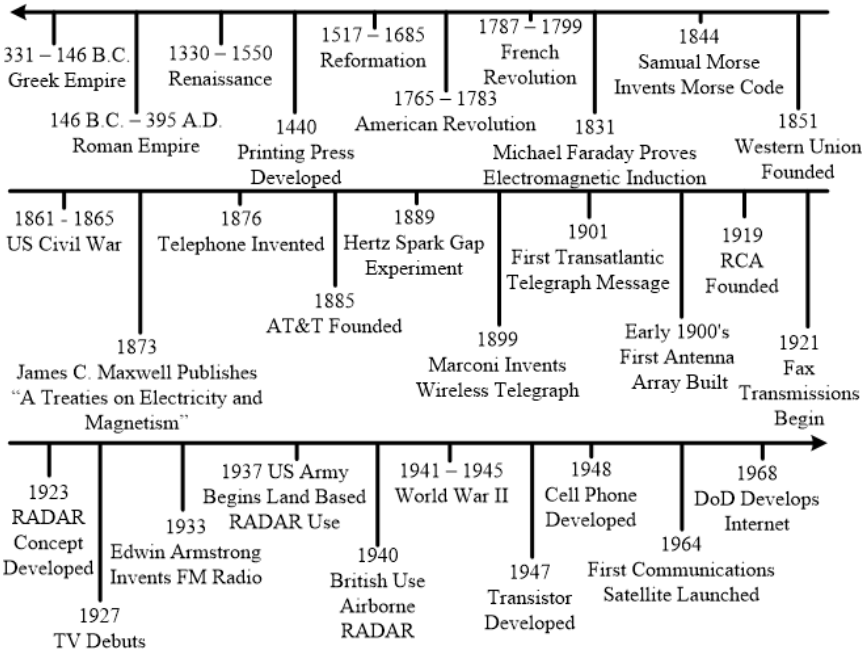

Fig. 1. Communications development timeline.

Ancient laborious communication techniques sent communications across great distances. Communication techniques through the Greek (323–30B.C.) and Roman (30B.C.–410A.D.) Empires involved runners, horses, chariots, smoke signals, handwritten scrolls, and ships. Greece consolidated commerce language. Rome established a transportation network increasing commerce and reasonably safe travels. These communication improvements opened conduits for communicating scientific and societal ideas and commerce expansion into Europe, North Africa, Asia, and ultimately the globe.

Greek and Roman communication enhancements spread scientific and societal ideas faster. The Renaissance (1330–1550A.D.) and Reformation (1517–1685A.D.) ideas produced the Guttenberg printing press (1440A.D.), American and French Revolutions (1776–1799A.D.), and Industrial Revolution (1760–1840A.D.). The American Revolution produced liberty and capitalism. Liberty and capitalism stimulated international commerce growth. Liberty and commerce growth invigorated innovation and science exploration. Innovation and science exploration encouraged respected scientists, for example Michael Faraday. Michael Faraday, father of electromagnetic induction, traveled throughout Europe and America giving lectures and demonstrating the latest electricity and electromagnetism developments. Continued commerce growth spread scientific advancement and societal improvement generating further innovation and commerce.

Increasing commerce triggered further communication innovation to conduct commerce faster. Communication techniques advanced in 1844 following Samuel

Morse's telegraphed message, "What hath God wrought," over a 40 mile electrical cable connecting Washington D.C. and Baltimore, MD [1]. Building upon Morse's success, Western Union developed the first electronic communications business sending telegraph messages for a price in 1851 [2]. Telegraph communications established a new communication transportation network as 23,000 miles of electrical cable crisscrossed the United States prior to 1861 [3]. Communication techniques took another leap in 1876 following Alexander Graham Bell inventing the telephone. American Telephone and Telegraph (AT&T) combined Morse's and Bell's inventions and initiated paid written and voice communications in 1885 [4]. Innovative written and voice communication techniques significantly shifted communications from ancient laborious communication techniques.

The telegraph and telephone streamlined communications but limited to immobile locations. Communications leaped forward after Guglielmo Marconi transmitted the first wireless telegraph message across the Atlantic Ocean in 1901. Marconi aided building the Radio Corporation of America (RCA) in 1919 [5] to sell wireless communications parts and equipment. Wireless telegraph communication made commerce communication possible through mobile stations.

Electrical wired and wireless communication techniques continue to advance commerce growth and spread scientific advancement and societal improvement triggering further innovation and commerce. In 1933, Edwin Armstrong invented, patented, and developed frequency modulation (FM). FM made voice transmission clear, stronger, and richer effortlessly attracting listeners. Armstrong also developed dual-

channel multiplexing, i.e., carrying voice and data simultaneously, stereo sound, and used the moon as a satellite [6]. World War II (1941-1945) introduced shipboard radar and airborne radar along with mobile FM transceivers. Wartime research developed passive radio communication named radio frequency identification (RFID) [7] and commercialized cellular communications and television (TV). Westinghouse Electric Corporation and the Glenn L. Martin Company, known today as Lockheed Martin, formed a joint venture called Stratovision [8] in 1945. The concept sought to provide TV and FM radio to 78% of the American population. Continuously flying B-29 style aircraft at 30,000 feet provided signal coverage for a 422 mile diameter circle. Fig. 2 shows one of the research aircraft. Stratovison succeeded but operationally expensive. The Stratovison model later became satellite TV and satellite radio.

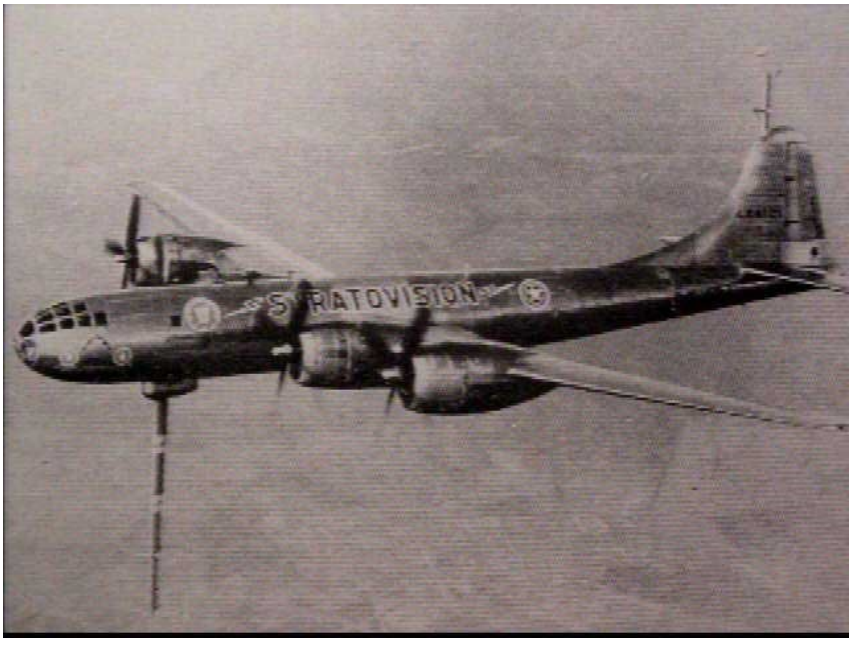

Fig. 2. Stratovision B-29 research aircraft with TV transmit antenna extended below aircraft (photo courtesy of the Early Television Museum). Photo reprinted from [8].

Between 1945 and 1991, weather and broadcasting satellites were developed, microwave communication, manned space flight, radio telescopes, aviation and maritime communication and navigation enhancements, global positioning system (GPS), and computer networking. The 1990's tech boom introduced digital communications and media, personal communication systems (PCS), and wireless personal computer networking. Fig. 3 shows various manned, communication, and scientific spacecraft designed and deployed to advance open communication fueled by commerce. Free market commerce expansion inspired communications to rapidly transition from ancient laborious communication techniques to manmade satellites creating a 5000 year leap in less than 250 years and the evolution continues.

Fig. 3. Various manned, communication, and scientific spacecraft on public display in the James S. McDonnell Space Hangar at the Steven F. Udvar-Hazy Center located in Chantilly, VA. Photo taken by the author.

II.B. Defining Bandwidth and Ultra-Wideband

A broadband antenna has wide bandwidth. The difference between f_U and f_L defines bandwidth (B). f_U And f_L define the upper and lower frequency limits respectively for the specified antenna. The f_U and f_L designations originate from the antenna functioning according to a chosen performance metric containing gain, impedance, nulls, etc. Eq. 1

and 2 represent two methods for describing bandwidth mathematically. Eq. 1 calculates percent bandwidth (*PB*) and Eq. 2 represents ratio bandwidth (*RB*). f_C Represents the center frequency between f_U and f_L. For example, consider an antenna operating between 300MHz and 3000MHz (3GHz). This antenna has $B = 3000 - 300 = 2700MHz$, $PB = \frac{(B)}{1350} x100\% = 200\%$, and $RB = \frac{3000}{300} = 10 \text{ or } 10:1$.

$$f_C = (f_U - f_L)/2$$
$$PB = \frac{f_U - f_L}{f_C} x100\% \quad (1)$$

$$RB = \frac{f_U}{f_L} \quad (2)$$

Narrow band antennas such as dipoles and microstrip patch antennas describe *B* as *PB*. Wideband antennas such as spirals and horns describe *B* as *RB*. *RB* also defines bandwidth for the TCA and Wilkinson power combiners. Tables I and II list frequency band allocations from the ITU and IEEE respectively, which assist in defining frequency band coverage for antenna designs.

TABLE I
INTERNATIONAL TELECOMMUNICATIONS UNION (ITU)
FREQUENCY ALLOCATIONS

Band Name	Frequency Span
Very-High-Frequency (VHF)	30MHz – 300MHz
Ultra-High-Frequency (UHF)	300MHz – 3GHz
Super-High-Frequency (SHF)	3 – 30GHz
Extremely-High-Frequency (EHF)	30 – 300GHz

ITU oversees information and communications technology matters for the United Nations.

TABLE II
INSTITUTE OF ELECTRICAL AND ELECTRONIC ENGINEERS (IEEE)
FREQUENCY ALLOCATIONS

Band Name	Frequency Span
VHF	30MHz – 300MHz
UHF	300MHz – 1GHz
L-Band	1 – 2GHz
S-Band	2 – 4GHz
C-Band	4 – 8GHz
X-Band	8 – 12GHz
Ku-Band	12 – 18GHz
K-Band	18 – 26.5GHz
Ka-Band	26.5 – 40GHz
General RF	3kHz – 300GHz
General Microwave	300MHz – 30GHz
General millimeter wave (mmW)	30GHz – 300GHz

A standard definition describing the UWB designation does not exist. Stutzman and Thiele define a UWB antenna as, “If the impedance and the pattern of an antenna do not change significantly over about an octave $\left(f_U / f_L = 2\right)$ or more, we will classify it as a [UWB] antenna.” [9]. The Federal Communications Commission (FCC) Report and Order (R&O) [10] published in February 2002 defines UWB as any device possessing a minimum 500MHz bandwidth. The 2007 IEEE Standard for UWB radar [11] defines an UWB antenna possessing $PB \geq 25\%$ or $RB \geq 1.25$. I selected the IEEE definition for this dissertation.

II.C. Communicating with Phased Arrays

An antenna array provides the gain desired to amplify the incoming or outgoing electromagnetic signal for a communications system. Array development has significantly progressed since the wireless age began. Haupt and Rahmat-Samii provide a good historical overview of array and phased array development in an IEEE Antennas and Propagation magazine article [12]. S. G. Brown of Great Britain [13] developed the first antenna array made from dipoles at the turn of the 20^{th} century. The wireless telegraph Marconi developed [14] could not have been possible without assistance from Ferdinand Braun, a German physicist. Braun developed the antennas used by Marconi's wireless experiments. Braun also built and experimented with the first phased array [15]. Braun's array, featured in Fig. 4, composed from three monopole antennas forming an equilateral triangle. He introduced a 90^{o} phase delay forming a cardioid antenna pattern. Changing the transmitting antenna from C to B or A the antenna pattern steers $\pm 60^{o}$. Marconi and Braun share the 1909 Nobel Prize for Physics.

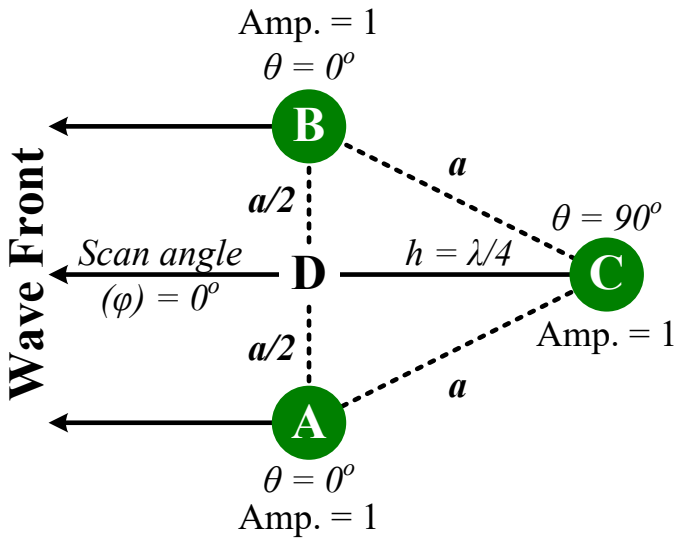

Fig. 4. Graphical explanation of first phased array designed and tested by Braun as depicted for his 1909 Nobel Prize in Physics lecture.

RADAR, synthetic aperture radar (SAR), missile detection, and weather radar applications frequently employ phased arrays. Over the past 30 years, phased arrays have begun moving beyond radar and into science and communication applications. New radio telescopes are implementing phased arrays to scan the heavens faster and improve object tracking. [16, 17]

Ioannis Tzanidis, a doctoral student of Dr. Volakis at The Ohio State University, in his dissertation stated, “Besides radars, new generation of communication networks will be based on multifunctional multiple input multiple output (MIMO) antennas that setup a wireless grid through which nodes exchange information at high data rates. To accommodate that, the wireless channels need to be UWB, utilizing the whole currently available bandwidth between 698MHz − 2.7GHz.” [18].

Mobile communications continues to grow and stress existing systems encouraging new developments to handle growing capacity. Based on Cisco's visual networking index, global mobile data will increase to 2.8 gigabytes by 2019 from 360 megabytes consumed per customer in 2014. Globally, mobile data traffic will increase 10-fold by 2019 producing an annual 57% growth rate [19]. Cisco also identified by 2019 5.2 billion mobile customers will use 11.5 billion mobile devices an increase from 4.3 billion mobile customers and approximately 7 billion mobile devices in 2014 [19]. Future mobile data and devices will strain 4G cellular service as anticipated by classical information theory [20, 21]. Moving mobile data to higher frequencies will substantially improve channel bandwidth and relieve forecasted congestion. Moving to higher frequencies also introduces higher path loss due to the shorter wavelengths. To help compensate for the loss, cellphone and base station antenna gain needs improvement. Research continues, as described in references [22 – 27], to develop phased arrays for 5^{th} generation (5G) mmWave (30 – 300GHz) cellphones and base stations to take advantage of beamforming, higher gain, more bandwidth, antenna diversity, and MIMO technology. David Gesbert and Jabran Akhtar provide a good overview of MIMO and spacial multiplexing in reference [28].

Space communication networks also continue to increase capacity as utilization develops inspiring enhanced RF systems. Rahmat-Samii and Densmore wrote an extensive IEEE transactions article [29] reviewing antenna technology and trends for satellite communications. Multi-beam and steerable applications including aeronautical, ship, submarine, and automobile communications increasing rely upon phased arrays.

Rahmat-Samii and Densmore state [29] satellite antenna development desires to provide "…uninterrupted, seamless, and high throughput connectivity no matter where." Implementing MIMO communications challenges future satellite antennas.

Research and development continues on improving space – space, space – earth, and inter-planetary communications. National Aeronautics and Space Administration (NASA) summarizes their communication objectives as follows [30], "The communication infrastructure will provide continuous maximum coverage for areas of concentrated space presence and activity." Interacting with active legacy communication systems requires flexibility to support numerous communication standards. Selecting, integrating, and supporting traditional RF systems consumes money, personnel, and space. Space mission funding originates from tax money allocation by congress, therefore NASA sees, "Affordability is a fundamental aspect of all future space endeavors for NASA, commercial, and military assets." [30]. To reduce cost, labor, and equipment quantity, NASA seeks to implement, "…modular SDR technology [to] reduce the upfront specifications to high-level parameters like RF bandwidth, RF output power, data traffic volume, etc…" [30]. Computational limitations and RF "front end" hardware restrict SDR's flexibility to manipulate digital signals through modulation, error correcting codes, framing protocols, cryptography algorithms, etc. [30]. NASA's quest to implement SDR for future space missions requires upgrading the RF "front end." RF "front end" components represent filters, amplifiers, power combiners/divider, antennas, mixers, transmission lines, etc. New RF "front end" components need to be wideband, low power, low profile, and lightweight [31].

As mobile and space communications expand and decreasing cost and space, antennas must keep up with demand. A TCA phased array provides a smaller planar profile and increased bandwidth, providing up to 45:1 bandwidth [18], and less cost as contrasted with traditional arrays. As discussed in the prior section, communications has come a long way. Communicating with numerous mobile devices and connecting people together increases dependence upon wireless systems.

II.D. Phased Array Overview

A phased array involves at least two identical antennas tuned so the radiation pattern holds minimum specified radiation characteristics over a target frequency range for maximum field of view (FOV). Phased array features include wide-angle beam scanning without mechanical help, adaptive beamforming, distributed aperture, multiple beams, and designs for low radar cross section. Table III lists common phased array research areas. Table IV shows phased array design considerations. Phased arrays contain grouped like antenna elements selected from one antenna classification type: wires, loops, broadband dipoles, traveling wave, frequency independent, apertures, horns, microstrips, and reflectors [32].

TABLE III
GENERAL RESEARCH TOPICS FOR PHASED ARRAYS

Antenna Elements	Blindness
Finite and Infinite Arrays	Electronic Scanning
Linear, Planar, Conformal Designs	Phase Shifters
Polarization	Low Noise Amplifiers (LNA)
Mutual Coupling	Design and Fabrication Methods
Analog and Digital Beam Forming	Measurements
Bandwidth	Characterization
Computer and Mathematical Modeling	RADAR Cross-Section (RCS)
Impedance	Materials
Gain Optimization	Passive vs. Active Electronic Scanning
Side Lobes	Noise Analysis
Grating Lobes	Reconfiguration

TABLE IV
PHASED ARRAY DESIGN CONSIDERATIONS

Field of View	Scan Sector
Bandwidth	Polarization
Gain	Half-Power Beamwidth
Side Lobe Level	Front–to–Back Ratio
Null Depth	Impedance
Noise Figure	Antenna Elements
Cables	Filters
Power Combiners	Connectors
Phase Shifters	Physical Limitations
Budget	Application Durability
Fabrication	Support Structure
Ground Plane	Testing

MIT Lincoln Laboratory published *Ultrawideband Phased Array Antenna Technology for Sensing and Communications Systems* [33] covering necessary electromagnetic background material the reader may need to review for understanding ultra-wideband arrays. I recommend reviewing chapters 1–3. Those readers not familiar with phased array theory, please refer to *Phased Arrays* by R. C. Hanson [34], *Phased Array Antennas* by A. K. Bhattacharyya [35], and *Phased Array Theory and Technology* by R. J. Mailloux [36].

Fig. 5 presents a linear phased array section designed for reception. A power combiner sums the incoming far field electromagnetic wave impressed on array elements. A phase shifter connects to each array power combiner. The incoming electromagnetic wave hits the array from all θ_S angles possible. As the phase shifter varies phase angles, the array's main beam scans the FOV. Fig. 6 shows a generic array aperture and radiation pattern steering via changing elevation angle θ and azimuth angle φ. Classic ½ wavelength $(\lambda_o / 2)$ spacing between array elements introduces cross talk. Eq. (3) defines free-space wavelength (λ_o) with c representing the speed of light $\left(3x10^8 \, Meters / \mathrm{Sec} \, or \, 1.118x10^7 \, Miles / Minute\right)$ and f frequency in Hertz. Cross talk occurs when a received RF wave segment at each array element also bleeds or couples into neighboring array elements. The coupled RF wave either strengthens or weakens as the element spacing decreases or increases potentially causing adverse characteristic changes. Element cross talk describes array mutual coupling shown in Fig. 5. G.H. Brown from RCA discovered mutual coupling between array elements becomes an important factor for array designs as discussed in [37] back in 1937.

$$\lambda_o = \frac{c}{f} \tag{3}$$

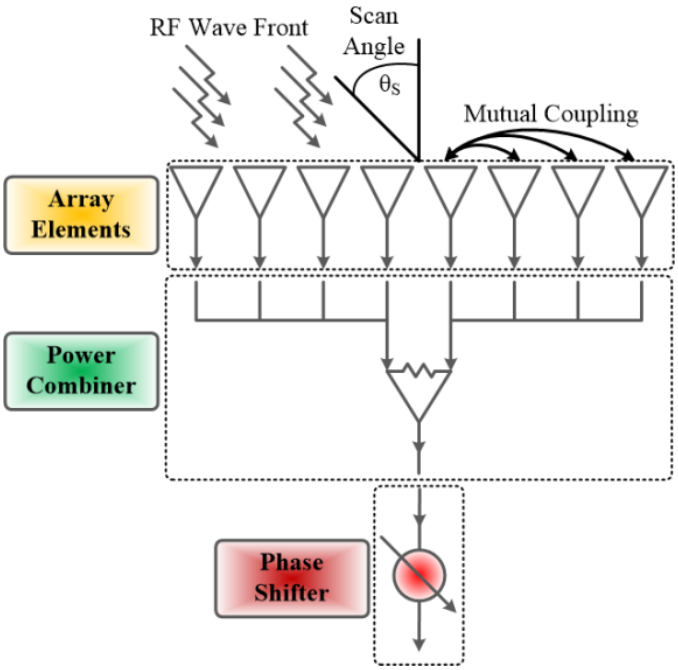

Fig. 5. Block diagram of a sectioned receiving linear phased array.

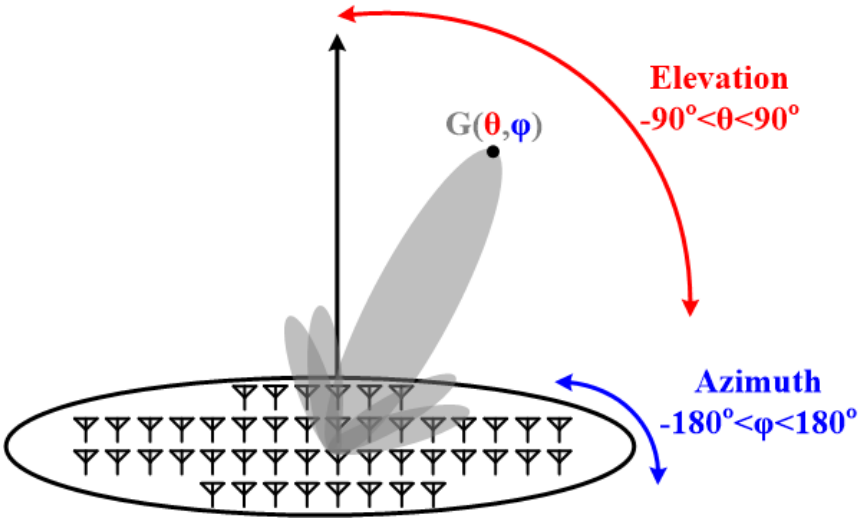

Fig. 6. Generalized phased array aperture with far field radiation pattern steered along θ and φ.

II.E. Tightly Coupled Array Overview

The conventional method to designing a broadband phased array requires focusing on designing one array element for desired bandwidth and radiation characteristics then manipulating dimensions, materials, impedance handling, etc., to compensate for the mutual coupling between elements to improve array gain, bandwidth, beam width, grating lobes, etc. Rather than struggle with array mutual coupling, the engineer will utilize the mutual coupling and integrate it into the design, taking the focus off just one element and looking at the entire array. The tightly coupled array (TCA) design approach originates from the current sheet array (CSA) proposed by Wheeler [38] and developed by Munk [39].

II.F. Achieving UWB Phased Array Power Combining

Phased array applications include RADAR, satellite communications, radio telescopes, broadcasting, and amateur radio. Many traditional UWB phased array designs are large, requiring ample space for feed networks and phase shifters. Designing and implementing the application correct power divider/combiner requires studying and understanding the fundamental power division concepts and characteristics.

Signal division, or summing a specified fraction (β) across an identified spectrum and simultaneously controlling amplitude and phase over each path, presents an engineering design challenge. Fig. 7 portrays a signal division, or summing block diagram. Important design stipulations involve appropriate impedance matching, transmission loss, signal isolation, phase stability, and bandwidth. RF engineers

endeavor to overcome these challenges encountered for numerous applications, particularly phased arrays, while balancing loss, cost, weight, and size. Phased arrays contain numerous antenna elements where incoming signals divide from and/or sum down to a single transmitter and/or receiver.

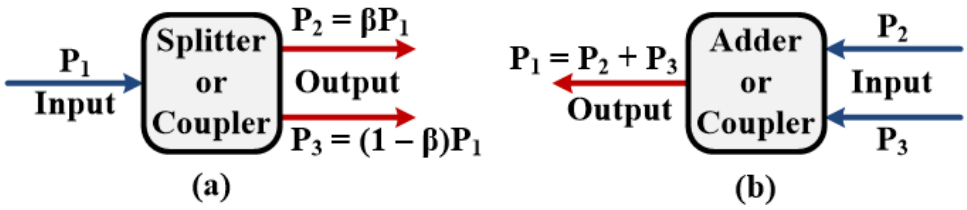

Fig. 7. Signal divider (a) and summer (b) block diagrams.

The MIT Radiation Laboratory developed and documented several different signal dividers and combiners during the 1940's [40]. The path to developing a compact and low-cost power divider began with T-junctions, hybrid circuits, and couplers [41-43]. Fig. 8 portrays a simple three-port T-junction power divider implemented as a waveguide and microstrip. The ideal power divider possesses matched ports, lossless circuit, and infinite port isolation. A T-junction offers lossless conditions and lacks matched ports and good signal isolation. Phased arrays function better with matched and isolated ports.

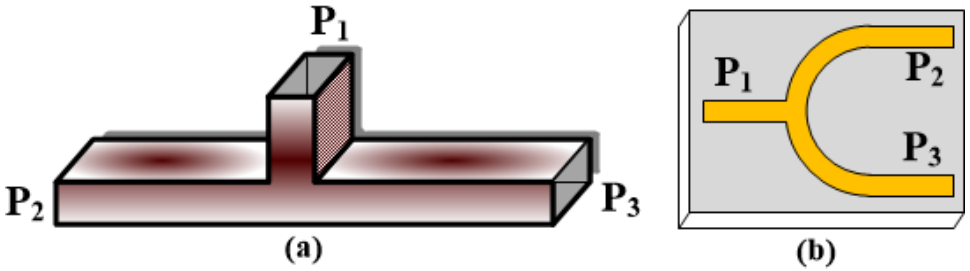

Fig. 8. A simple T-junction power divider realized as a waveguide (a) and microstrip (b).

Understanding the power division problem and seeking a resolution, Sylvania Electronic Systems (SES) assigned one of their engineers to the project, a World War II Navy veteran named Ernest J. Wilkinson (1927 – 2012). During his career at SES and GTE[1], he worked on weapon systems, RADAR, communication equipment, and satellite communications [44-45]. His understanding of RF led to the introduction of the "N-Way Hybrid Power Divider", which now bears his name [46-47]. The Wilkinson power divider takes an incoming signal and equally splits it between *n* outputs. London and Maloratsky provide some additional historical notes regarding Russia's contribution toward the n-way power divider in reference [48-49].

The rudimentary Wilkinson signal transition design includes an n-way junction made from a shorting plate, quarter-wavelength transmission lines, and isolation resistors positioned between output ports and a non-ground common point. The Wilkinson power divider/combiner possesses matched ports and good isolation at the expense of introducing some loss. This passive and bi-directional device integrates into almost any

[1] Sylvania Electronic Systems (SES) began in 1924 manufacturing radio tubes and grew substantially from war research and production during the 1940's. In 1959, SES merged with General Telephone forming General Telephone and Electronics Corp (GTE). GTE became Verizon in 2000 [49].

RF receiver or transmission system. Fig. 9 shows a cable TV splitter. A cable TV splitter represents a common application of a power divider the reader may easily recognize.

Fig. 9. An industry fabricated 3dB cable TV signal splitter. Photo taken by the author.

Planar transmission line development utilizing photo etching technology known as microstrip, or stripline, arrived in the 1950's [50]. Photo etching modernized phased arrays by integrating new economical planar transmission lines. Eight months following Wilkinson's paper, J. R. Dent published a paper [51] implementing Wilkinson's design using stripline, rather than coax. Dent's effort made advancing power divider development less expensive and further appealing to commercialization. Broadband power divider continued through the 1960's. Research funds remained plentiful from both NASA and the Department of Defense (DOD) as space race with the Union of Soviet Socialist Republics (USSR) reached its zenith, as Neal Armstrong walked on the moon in July, 1969.

Parad[2] and Moynihan[3] developed an unbalanced amplitude version of the Wilkinson power divider [52] in 1965. Seymour B. Cohn[4] introduced a planar multistage Wilkinson power divider considerably enhancing bandwidth and port isolation [53] in 1968. Cohn also provided mathematical insight using even and odd mode analysis for the Wilkinson combiner. Cohn's work made the Wilkinson power divider into the circuit representation and design recognized today "… [a] T junction followed by a multiplicity of cascaded pairs of TEM line lengths and interconnecting resistors" [53].

For the Wilkinson power divider/combiner, the nouns divider or combiner define the signal path placement. Interchanging the nouns, divider or combiner, may occur without consequence.

Currently, research focuses on making the Wilkinson combiner smaller, providing band selectivity, and wideband coverage. "In recent years, wireless communication systems such as a mobile phone, WLAN, ETC, and etc., are remarkably developed. Accordingly, various microwave devices are demanded with high performance that are small size, low-cost, wide-band, and multi-band. Therefore, many researchers have made an effort to miniaturize Wilkinson power dividers." [55] TCA antennas need a signal combiner covering their entire operating spectrum. The combiner's structure must fit comfortably and concealable behind the array as not to interfere with the radiation pattern. The combiner condenses the array from two-dimensional to one-dimensional.

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[2] Employed by SES
[3] Employed by United States Army Research & Development Laboratories (USARDL)
[4] Employed by Rantec, a division of Emerson Electric Co. today known as Rantec Microwave Systems Inc. [54]

II.G. Examining a Basic Wilkinson Power Combiner

The rudimentary three-port Wilkinson power combiner (WPC) illustration in Fig. 10 exhibits ports matched to Z_0. Fig. 10 illuminates two quarter-wave transmission lines $(l = \lambda_0 / 4)$ each valued at $Z = \sqrt{2}Z_0[\Omega]$ and an isolation resistor $\left(R = 2Z_0[\Omega]\right)$ bridges ports two and three. Microstrip or stripline simplifies replicating a planar WPC.

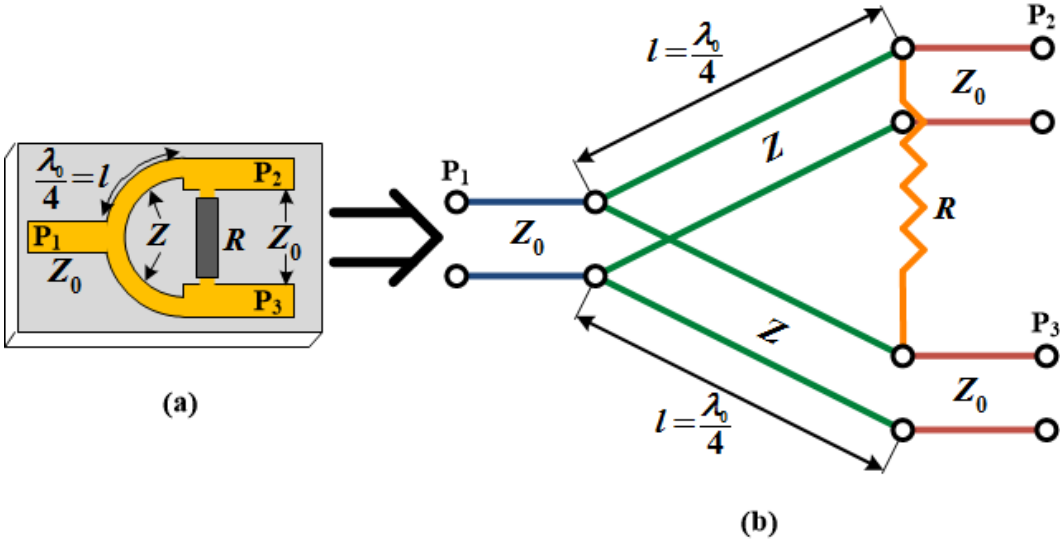


Fig. 10. Rudimentary single stage WPC constructed from microstrip (a) and transmission line model (b).

Fig. 10 represents an ideal WPC design example. Implement characteristic impedance $Z_0 = 50\Omega$ using resonate frequency f_c = 2.0 GHz ($\lambda_0 = 5.91$ inches). Create two quarter-wave transmission lines possessing impedance $Z = \sqrt{2}Z_0 = 70.71\Omega$ with $l = \lambda_0 / 4 = 1.48$ inches long. The isolation resistor assigned $R = 2Z_0 = 100\Omega$. Next, simulate

the WPC circuit using microwave circuit simulator Quite Universal Circuit Simulator (Qucs) [56]. Fig. 11 displays the simulation results.

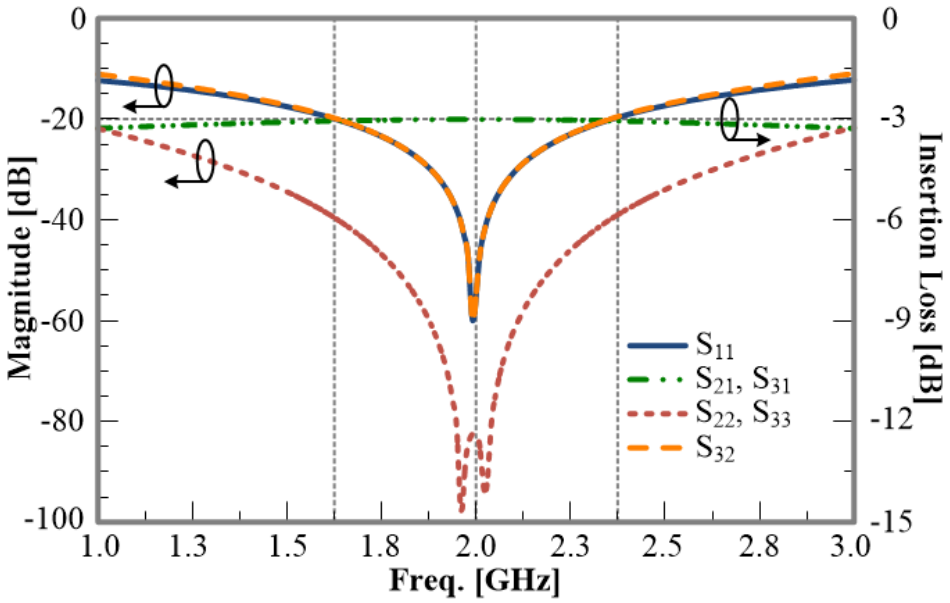


Fig. 11. Rudimentary and ideal WPC simulation results from Qucs.

The WPC simulation analysis indicates:

1. The combiner device produces a 2.0 GHz resonance.
2. The circuit spans 1.6 – 2.4 GHz and providing an 800 MHz bandwidth.
3. Ports P_1, P_2, and P_3 possess a minimum -20dB return loss (S_{11}, S_{22}, and S_{33}) indicating matched ports.
4. The -3dB transmission signal or insertion loss (S_{21}, S_{31}) shows ports two and three equally receiving 50% of the power originating from port one.
5. Ports P_2 and P_3 20dB minimum isolation (S_{32}) expresses signal path crosstalk or mutual coupling attenuation spanning the 800 MHz bandwidth.

WPC results repeat every odd harmonic, $\ldots, 3f_c, 5f_c, \ldots$. Naturally, even harmonics occur $\ldots, 2f_c, 4f_c, \ldots$

II.H. Even-Odd Mode Analysis

Performing three-port WPC circuit analysis involves superposition or even-odd mode network analysis. Reed and Wheeler published *A Method of Analysis of Symmetrical Four-Port Networks* [57] in 1956. Their effort made mathematically understanding multi-port microwave components easier. Pozar [40] and Collin [58] provide comprehensive explanations covering even-odd mode analysis. Even-odd mode analysis [57] breaks the symmetrical Wilkinson circuit into two parts and superposition simplifies circuit analysis. Fig. 12 illustrates a normalized and symmetric WPC. The WPC splits along the symmetry line to perform even-odd mode analysis.

Fig. 12 displays Z_0 and Z transmission lines become resistors. Next, normalize all components by Z_0. Then split the isolation resistor R at the symmetry line and add a voltage node where R encounters the two quarter-wave transmission lines. Fig. 12 contains the impedance normalization details. Each branch entails even-odd mode analysis, however symmetric circuits allow performing even-odd mode analysis on one branch then duplicating the result for the remaining branch. V_1 symbolizes the Port one node voltage. V_{s2} and V_{s3} define Ports two and three voltage sources respectively. Grounds terminate Port one resistors.

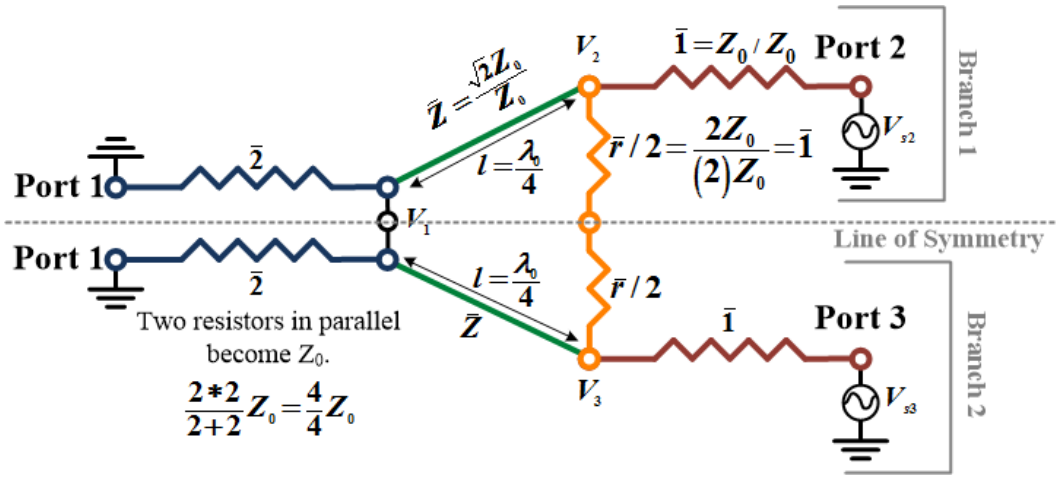


Fig. 12. Normalized basic Wilkinson combiner circuit for even-odd mode analysis.

Two separate excitations define modes. Eq. (4) expresses the even mode *(E)* voltage source value for both input ports. Eq. (5) expresses the odd mode *(O)* voltage source value for both input ports. Taking the sum of both even and odd mode voltage components gives $V_{s2}^{E}+V_{s2}^{O}=V_{s2}=4V_0$ and $V_{s3}^{E}+V_{s3}^{O}=V_{s3}=0$ respectively. Applying superposition for even and odd modes provides the excitations $V_{s2}=4V_0$ and $V_{s3}=0$ aid describing the network S parameters.

$$V_{s2}=V_{s3}\therefore V_{s2}^{E}=V_{s3}^{E}=2V_0 \tag{4}$$

$$V_{s2}=-V_{s3}\therefore V_{s2}^{O}=-V_{s3}^{O}=2V_0 \tag{5}$$

II.H.1. Even Mode

The Fig. 12 symmetry line represents a virtual open circuit demonstrated by Fig. 13. The isolation resistor shows no current flowing, thus the normalized input impedance looking into port two toward port one simplifies to $\bar{Z}_{in,2}^{E} = \bar{Z}^{2} / 2$. When frequency (*f*) equals center frequency (f_c) then $\bar{Z}_{in,2}^{E} = \left(\sqrt{2}\right)^{2} / 2 = \bar{1}$ matches port two. Every frequency, except f_c, influences port impedance for either better or worse thus demonstrating the quarter-wave transformer's limited matching bandwidth to f_c.

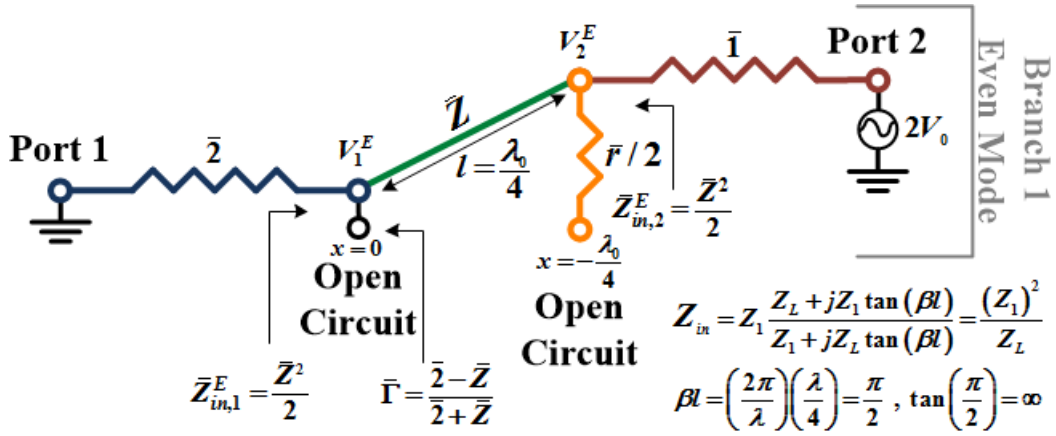


Fig. 13. Even mode bisection of Wilkinson combiner

Using a voltage divider, the voltage V_2^E becomes $V_2^E = \frac{2V_0}{1 + Z_{in}^E} = V_0$ when $f = f_c$. Eq. (6) aids in determining the voltage V_1^E.

$$V(x) = V^{+}\left(e^{-j\beta x} + \Gamma e^{j\beta x}\right),\ \beta = \frac{2\pi}{\lambda} \tag{6}$$

Set $V_2^E\left(x=-\frac{\lambda}{4}\right)=V(x)$ in Eq. (6) gives Eq. (7) and then setting $V_1^E(x=0)=V(x)$ in Eq. (6) gives Eq. (8) to define V_1^E.

$$V_2^E\left(x=-\frac{\lambda}{4}\right)=V^+\left(e^{j\frac{\pi}{2}}+\Gamma e^{-j\frac{\pi}{2}}\right)=jV^+(1-\Gamma)=V_0 \tag{7}$$

Algebraically manipulating Eq. (7) defines V^+ as $V^+=\frac{V_0}{j(1-\Gamma)}=\frac{-jV_0}{(1-\Gamma)}$. Setting $x=0$ in Eq. (6) and V^+ defined produces V_1^E in Eq. (8).

$$V_1^E(x=0)=V^+\left(e^{-j0}+\Gamma e^{j0}\right)=V^+(1+\Gamma)=-jV^0\frac{(1+\Gamma)}{(1-\Gamma)} \tag{8}$$

Fig. 13 shows the defined reflection coefficient (Γ) looking into port one simplifies Eq. (8) thus yielding Eq. (9).

$$V_1^E=-jV^0\sqrt{2} \tag{9}$$

II.H.2. Odd Mode Analysis

The Fig. 12 symmetry line represents a virtual short circuit demonstrated by Fig. 14. The second superposition portion implements Eq. (5) in Fig. 14. The Port two input impedance $\left(\bar{Z}_{in,2}^{O}\right)$ equals $\bar{r}/2$ assuming $f = f_c$. Shorting Port one forces the quarter-wave transformer $\left(\bar{Z}\right)$ to render a Port two open circuit. Impedance matching port two requires $\bar{r} = \bar{2}$ in Fig. 14 forces $V_1^O = 0$ and $V_2^O = V_0$ thus directing Port two reflected current through the isolation resistor avoiding crosstalk.

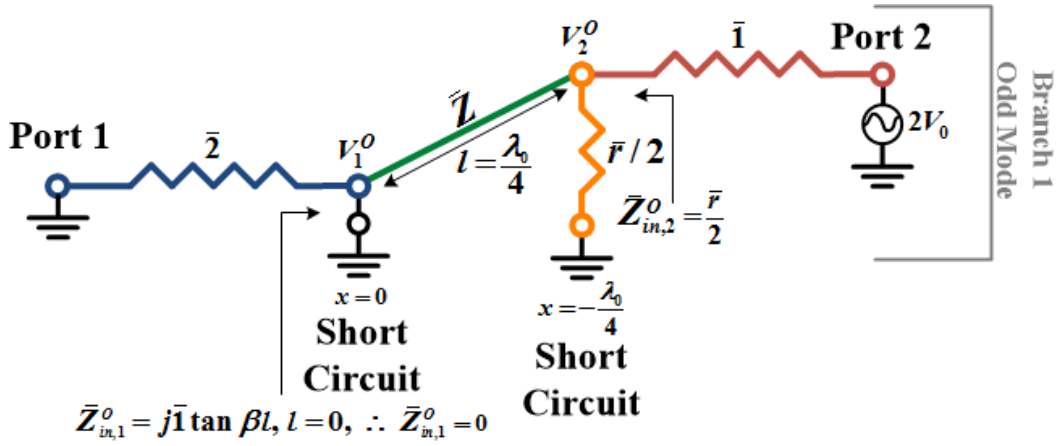


Fig. 14. Odd mode bisection of Wilkinson combiner

Moving the source to port one then the impedance $\left(\bar{Z}_{in,1}^{O}\right)$ looking from port one toward port two equals $\left(\sqrt{2}\right)^2/2 = \bar{1}$ with ports two and three matched. Fig. 15 illustrates applying V_1^O at port one forces $V_2^O = V_3^O$ matching ports two and three. Therefore, the open circuited isolation resistor $\left(\bar{r}\right)$ mimics the even mode outcome.

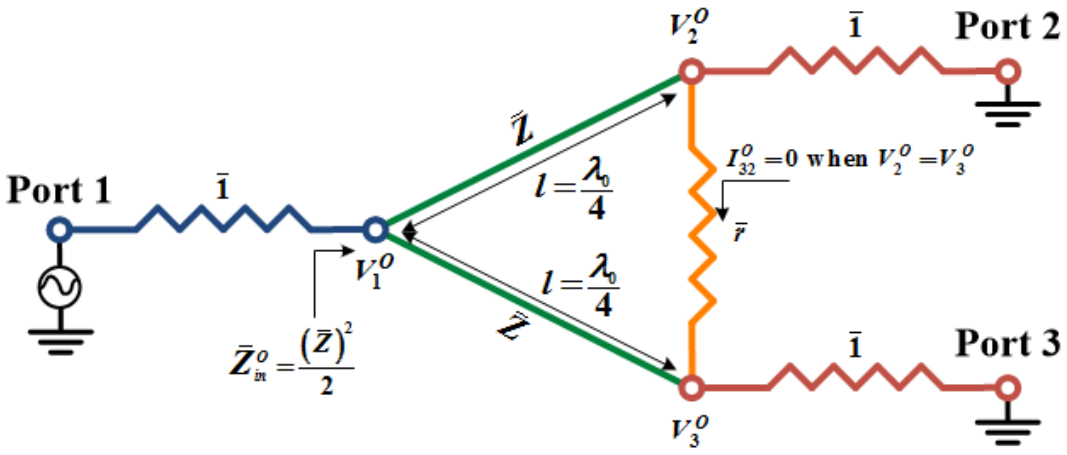


Fig. 15. Odd mode Wilkinson combiner for impedance from port one.

II.H.3. Even and Odd Mode Analysis Summary

Uniting the superposition analysis with the network analysis describes the S-parameters for the Wilkinson combiner in Fig. 13 as:

1. $S_{11} = \dfrac{V_1^{E-} + V_1^{O-}}{V_1^{E+} + V_1^{O+}} = \dfrac{0}{V_1^+} = 0$ ($\bar{Z}_{in} = \bar{1}$ when $\bar{r} = \bar{2}$ at port one).

2. $S_{22} = S_{33} = \dfrac{V_2^{E-} + V_2^{O-}}{V_2^{E+} + V_2^{O+}} = \dfrac{0}{V_2^+} = 0$ (When

$\bar{Z}_{in,2,3} = \bar{Z}^2 / 2 = \left(\sqrt{2}\right)^2 / 2 = \bar{1}$ for both even and odd modes).

3. $S_{21} = S_{31} = S_{12} = S_{13} = \dfrac{V_1^{E-} + V_1^{O-}}{V_2^{E+} + V_2^{O+}} = \dfrac{-jV_0\sqrt{2}}{2V_0} = -\dfrac{j}{\sqrt{2}}$ (Due to the symmetry and reciprocal network).

4. $S_{32} = S_{23} = \frac{V_3^{E-} + V_3^{O-}}{V_2^{E+} + V_2^{O+}} = \frac{0}{V_2^{+}}$ (Isolation resistor either open or short-circuited causing $V_2 = V_3$).

Thus demonstrating the even mode controls impedance matching ports one, two, and three while both even and odd modes control transmission and isolation. Modifying the transmission line characteristic impedance influences all combiner components and analysis.

II.I. Wilkinson Power Combiner Advancement

The Wilkinson power combiner/divider literature review covers seventeen peer-reviewed designs spanning 1968 to 2015 covering UWB and narrow band techniques. Implementation methods consist of multilayer, MMIC, LTCC, lumped components, artificial transmission lines, DGS, and EBG. Table V summarizes the authors' measured results.

TABLE V
PEER-REVIEWED PAPERS COMPARING WILKINSON POWER COMBINERS

Reference	Frequency [GHz]	Bandwidth	Area [mm^2]	RL [dB]	IL [dB]	Amp. Imbal. [dB]	Phase Unbal.	Min. Isolation [dB]
Goodman (1968) [59]	1-12.4	12:1	130mm	-19	-3 ± 0.75	± 0.1	-	-20
Sun (2004) [60]	15-45	3:1	0.45	-15	-5	-	-	-15
Woo (2005) [61]	1.5	-	-	-40	-3.3	-	-	-
Wentzel (2006) [62]	0.3-2.8	9.3:1	-	-10	-3 ± 0.25	-	-	-8
Lee (2006) [63]	3-5.5	1.83:1	17	-	-5.5	-	-	-9
Seman (2007) [64]	3.1-10.6	3.4:1	560	-12.5	-3.5 ± 0.2	-	± 3°	-
Li (2007) [65]	1.5	-	295.6	-36	-3.16	-	-	-30
Abbosh (2008) [66]	4-8	2:1	750	-10	-3.4 ± 0.2	± 0.2	± 2°	-10
Kawai (2009) [67]	0.85-1.2	1.4:1	345	-15	-3.5	-	± 3°	-20
Chieh (2009) [68]	2-18	9:1	-	-10	-3.5 ± 1.5	± 0.46	-	-11
Tang (2010) [69]	0.71-0.99	1.4:1	32	-10	-3.5 +/-0.2	-	-	-20
Xu (2012) [70]	2-8	4:1	930	-18	-3.85 ± 0.82	-	-	-20
He (2012) [73]	0.81-1.14	1.4:1	399	-10	-3.3	-	-	-20
Pribawa (2012) [74]	1-2	2:1	9000	-12.3	-7.8	-	-	-12.8
Liu (2013) [75]	0.5-1.5	3:1	625	-8.5	-11.8 ± 0.4	± 0.4	± 3°	-15
Trenz (2014) [76]	2-28	14:1	30	-10	-3.3 ± 0.6	-	-	-10
Ahmed (2015) [78]	1-7	7:1	2200	-10	-3 ± 0.5	± 0.2	± 2°	-15

Goodman [59] designed and tested a UWB stripline Wilkinson power combiner (WPC) in 1968 spans 1.0 – 12.4 GHz and providing a 12:1 bandwidth. The WPC design features an impedance matching Klopfenstein taper to achieve semi-infinite bandwidth. Goodman fabricated the circuit on a single layer substrate 130mm long. The WPC measurements demonstrate -19dB or better return loss, -3.425dB ±0.325dB insertion loss, 0.1dB amplitude imbalance, and -20dB or better isolation.

Sun et al. [60] designed and tested a folded two-stage multilayer WPC in 2004 for mmwave applications. The circuit spans 15 – 45 GHz with a 3:1 bandwidth. Sun fabricated the WPC on GaAs accomplished via millimeter integrated chip (MMIC) fabrication techniques. Circuit fabrication requires two metallization layers separated by a dielectric. The WPC footprint enjoys a $0.45mm^2$ surface area that consumes half the territory for a standard two-stage WPC. Sun's WPC proposal envisioned for fifth generation (5G) application adoption. The WPC measurements reveal -15dB return loss, -5dB insertion loss, and -15dB isolation.

Woo et al. [61] offered a defected ground structure (DGS) to suppress WPC second and third harmonics in 2005. The WPC design selects a 1.5 GHz resonant frequency with second and third harmonics befalling 3 GHz and 4.5 GHz respectively. Woo fabricated the asymmetric spiral DGS design on a GML1000 substrate 1.63mm thick. Woo sought to implement a DGS to accomplish WPC second and third harmonic suppression. Woo also examined circumstances involving metal backplane separation distance (0 – 5mm) from the WPC. Measurements indicated the DGS increases resonant frequencies when decreasing the WPC and the metal bottom separation distance. Implementing a DGS attenuated second and third harmonics 18dB. WPC measurements illustrate -40dB maximum return loss and -3.3dB maximum insertion loss.

Wentzel et al. [62] presented a new hybrid two-stage WPC using extra capacitive and inductive components in 2006. The WPC spans 300 MHz – 2.8 GHz and provides a 9.3:1 bandwidth. Wentzel examined the added insertion loss the WPC second stage length introduced. Implementing inductors and capacitors improved higher frequency

impedance and reduced transmission ripple. Frequency dependent internal losses from the chip inductors and capacitors introduce bonus resonances. Improving transmission loss depends on the second stage inductor values. Lower inductance improves insertion loss versus increasing inductance deteriorates insertion loss. The WPC offers -10dB or better return loss, -3dB ± 0.25dB insertion loss, and -11dB ± 3dB isolation.

Lee et al. [63] produced a miniaturized WPC implemented through pi-type multiple coupled microstrip line structure (MCMLS) in 2006. Lee's design reduced the circuit surface area by 37% and thus reducing manufacturing cost. The MCMLS introduces capacitance reducing shunt capacitance and thereby reduces transmission line characteristic impedance. The fabricated WPC assimilated chip capacitors and resistors yield identical complications mentioned by Wentzel [62]. The WPC fabricated on a Teflon substrate relishes a 17mm^2 surface area. Lee's circuit spans 3.0 – 5.5GHz and provides 1.83:1 bandwidth. Lee's WPC provides nearly equal transmission phase, -5.5dB average insertion loss, and -9dB or better isolation.

Seman et al. [64] presented a UWB multilayer WPC in 2007 spans 3.1 – 10.6 GHz providing a 3.4:1 bandwidth. Seman sought to create a multilayer UWB power divider on low temperature co-fired ceramics (LTCC) dielectrics to improve multilayer signal transfer without a via. Seman fabricated multiple WPC design iterations on Rogers RO4003™ hydrocarbon ceramic laminates possessing a 0.508mm thick. Increasing the circular stub radius narrowed the frequency range. Decreasing the circular stub radius widened and shifted higher the frequency range. Measurements demonstrate the WPC

possesses -12.5dB or better return loss, -3.5dB ± 0.2dB insertion loss, and transmission phase varies ± 3^{o}.

Li et al. [65] proposed in 2007 a condensed WPC capacitively loaded with 3^{rd} and 4^{th} harmonic suppression. The WPC design provides a 1.5 GHz resonant frequency. Li designed a condensed WPC able to handle spurious passband responses or harmonics introduced from transmission line periodic characteristics. A chip capacitor positioned perpendicular and halfway along each quarter-wavelength branch provides the harmonic suppression. Li's design achieved a 48% size reduction compared to a conventional WPC and sports a 295.6mm^2 surface area. Li fabricated the WPC on a Rogers RT/duroid® 5870 laminate 31mil thick. Third and fourth harmonic suppression achieved -18dB and -38dB respectively. The WPC offers -36dB or better return loss for S_{11} and -25dB or better for S_{22}/S_{33}, -3.16dB for S_{21} and -3.11dB for S_{31} insertion loss, and -30dB or better isolation.

Abbosh [66] proposed in 2008 a compressed multilayer WPC utilizing broadside microstrip/slot coupling. Abbosh's design positions the output ports on different layers. The WPC functions in the C-band (4 – 8 GHz) providing a 2:1 bandwidth. Fabricating the WPC required three conductive material layers separated by two dielectric layers. The WPC design implemented a T-junction fashioned from a slot and two microstrip lines. A slotted ground plane resides in the middle layer. A capacitive disk terminates one microstrip line and the other microstrip line terminated by an inductive circular slot. Simulated and measured results agreed and showed -10dB or better return loss, -3.4dB ±

0.2dB insertion loss, and -10dB isolation. Transmission phase varied by ± 2^{o} and provided ± 0.2dB amplitude imbalance.

Kawai et al. [67] presented a lumped-element quadrature WPC in 2009. Kawai desired to fashion a small, low cost, and wide band WPC. Kawai's design features a parallel LC-ladder circuit connected in series to an RL circuit. Each RL circuit node forms a T or π network branch. Each T and π network introduces a 90^{o} phase shift. Kawai's WPC spans 0.85 – 1.2 GHz providing a 1.4:1 bandwidth or 350 MHz and 1.0 GHz center frequency. Kawai fabricated his design on a Rogers TMM4® hydrocarbon ceramic thermoset polymer composite 0.508mm thick. The WPC consumed only 342mm^2 surface area of composite territory. The fabricated WPC integrated chip inductors, capacitors, and resistors yield duplicate complications mentioned by Wentzel [62]. Measurements demonstrate the WPC possesses -15dB or better S_{11}, -20dB or better S_{22}, and -15dB or better S_{33} return losses, transmission phase varied ± 3^{o}, -3.5dB insertion loss, and -20dB or better isolation.

Chieh et al. [68] presented a Butterworth (maximally flat) seven stage WPC in 2009. Chieh's WPC operates from 2.0 – 18 GHz providing a 9:1 bandwidth. Chieh fabricated the WPC on a liquid crystal polymer (LCP) foundation 12mil thick. He observed multi-layer boards require a thin adhesive layer that changes the dielectric to inhomogeneous. Self-adhesive LCP layers maintain the dielectric homogeneity. Chieh selected NiCr thin film resistors to preserve a minimal profile. The thin film resistors diminish losses and self-resonances native to chip resistors. The Butterworth cascade design eliminates the passband ripple present in Tschebyscheff (pronounced Chebyshev) polynomial designs

[53]. Chieh sought to construct a WPC on LCP for future mmwave applications. Measurements reveal the WPC possess a -10dB or better return loss with a 1.6:1 VSWR, -3.5dB ± 1.5dB insertion loss, ± 0.46dB or better amplitude imbalance, and -11dB or better isolation.

Tang et al. [69] created a tunable WPC in 2010. Tang replaced the λ/4 transmission sections with a lumped inductor and tunable varactor forming a nonlinear transmission line (NLTL). The WPC spans 710 MHz – 990 MHz providing a 1.4:1 bandwidth. Tang fabricated the WPC on FR4. He sought to design a compact and tunable UHF WPC using a NLTL design. The NLTL WPC design consumes 32mm^2 surface area, only 3% of a conventional WPC. Tang's WPC provides -10dB or better return loss, -3.5 ± 0.2dB insertion loss, and -20dB or better isolation over the operating bandwidth.

Xu et al. [70] created in 2012 a UWB four stage WPC covering 2 GHz – 8 GHz, a 4:1 bandwidth. Xu sought to design a compact WPC for UWB applications using the analytical approach found in [71] and HFSS [72]. Xu fabricated his WPC on a Rogers RT/duroid® 5880 laminate 0.508mm thick. The WPC consumed only 930mm^2 surface area of laminate terrain. Measurements show the WPC possess a -18dB or better return loss, -3.85dB ± 0.82dB insertion loss, and -20dB or better isolation.

He et al. [73] presented in 2012 a WPC with harmonic suppression using electromagnetic bandgap (EBG) circuitry. He pursued a condensed WPC design that rejects higher harmonics. The WPC covers 0.81 GHz – 1.14 GHz providing a 1.4:1 bandwidth. The EBG rejects harmonics spanning 3.2 GHz – 4.2 GHz and 4.4 GHz – 5GHz. He fabricated the WPC and EBG on an F4B woven-glass PTFE substrate 1.5mm

thick. The WPC footprint consumes 399mm^2 decreasing surface area 50%, -verses a conventional design consuming 793mm^2. WPC measurements highlight -10dB or better return loss, -3.3dB insertion loss, and -20dB or better isolation over the operating bandwidth.

Pribawa et al. [74] presented a six input to one output WPC in 2012. The WPC operates in L-band (1-2GHz) providing a 2:1 bandwidth. Pribawa desired to advance knowledge concerning specialized planar combiners requiring unusual input port numbers. Pribawa fabricated the WPC on an Arlon DiClad® 527 woven PTFE and fiberglass laminate 1.6mm thick. A fabrication challenge Pribawa overcame originated from fabrication limits regarding the isolation resistor and bonding wire placement. The WPC footprint covers 9,000mm^2 of laminate surface area. WPC measurements illustrate a -12.3dB or better return loss, -7.8dB or better insertion loss, and -12.8dB or better isolation.

Liu et al. [75] presented in 2013 a condensed multilayer eight input to one output UWB WPC. The WPC covers 0.5 – 1.5 GHz providing a 3:1 bandwidth with a 1.0 GHz center frequency. Liu toiled to integrate a WPC for MMICs using LTCC technology to improve performance, miniaturization, and cost. Liu fabricated the WPC on DuPont™ GreenTape™ 951 LTCC using six layers and each layer 96µm thick. He chose vias to interconnect the different LTCC layers together. The WPC occupies 625mm^2 LTCC surface area and 2.1mm thick. WPC measurements reveal -8.5dB or better return loss for input and output ports and 2.2:1 VSWR for port one, -11.8dB ± 0.4dB insertion loss, and

-15dB isolation. Transmission phase varied ± 3° and 0.4dB or better amplitude imbalance.

Trenz et al. (2014) [76] presented two multi-octave Wilkinson power dividers (WPD) in 2014. They cover 2.0 – 28 GHz providing a 14:1 bandwidth. Trenz sought to produce a small WPD for biomedical applications spanning three octaves over 2.0 – 25 GHz. Trenz fabricated the designs on Rogers RT/duroid® 5880 laminate 0.127mm thick. The first design possessed seven stages and the second design four stages. The first WPD surface area covered 30mm^2 and the second WPD covered 16mm^2. Electroplated NiAu, 45μm thick, coats the circuit to thwart corrosion. Trenz selected thin-film surface mounted isolation resistors. He modified resistor solder pads to minimize extra-length effects discussed by Horst in [77]. Trenz's first seven stage design provided slightly higher coverage 1.0 – 28 GHz. His second four stage design covered 2.0 – 28 GHz. The WPDs possessed -10dB or better S_{11} return loss and -13dB or better S_{22} and S_{33} return loss, -3.3dB ± 0.6dB insertion loss, and -10dB or better isolation.

Ahmed et al. [78] proposed an UWB and multilayer Butterworth WPC in 2015. The design covers 1.0 – 7.0 GHz providing a 7:1 bandwidth. He strove to design a condensed UWB for phased arrays, power amplifiers, balanced mixers, multiport networks, medical imaging, and frequency multipliers. Ahmed fabricated the WPC on a Rogers RO4003™ hydrocarbon ceramic laminate 0.406mm thick. Two conductive material layers separated by a dielectric form the WPC. A T-junction connects the slotline and microstrip lines. Shorted circular stubs terminate the microstrip lines. Open circuit circular stubs terminate the stripline. The ground plane contains a round dumbbell slot completing the

slotline open circuit. The WPC footprint occupies 2,200mm^2 surface area laminate. WPC measurements indicate -10dB or better return loss, -3dB ± 0.5dB insertion loss, ± 0.2dB amplitude imbalance, -15dB or better isolation, and transmission phase varied ± 2^o.

CHAPTER III

WHAT'S THE PROBLEM?

III.A. Original Combiner Impact on TCA

The first TCA test checked to perceive if impedance mismatch and other design flaws impact the TCA. Fig. 16 displays the TCA VSWR. Next to verify the 1.0 – 1.5 GHz hump orginiated from the combiners, I assembled the combiners without the antenna. All 128 combiner input ports terminated with a 50Ω loads. Fig. 17 displays the measurement setup. The VSWR measurement in Fig. 16 shows overlap for the 1.0 – 1.5 GHz hump demonstrating combiner impedance mismatch impacts antenna impedance.

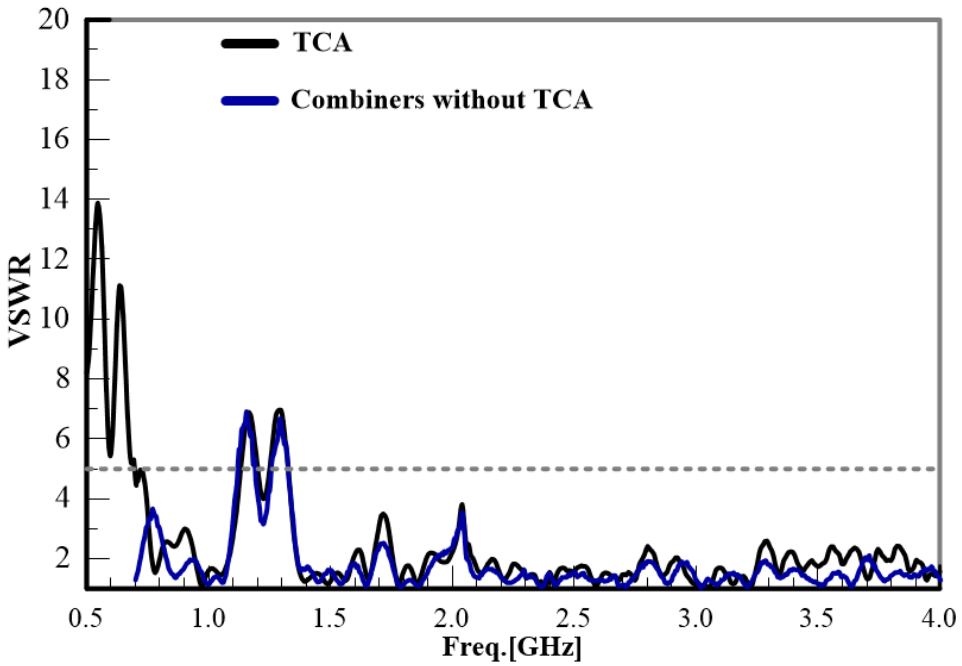


Fig. 16. Measured TCA and grouped combiners VSWR.

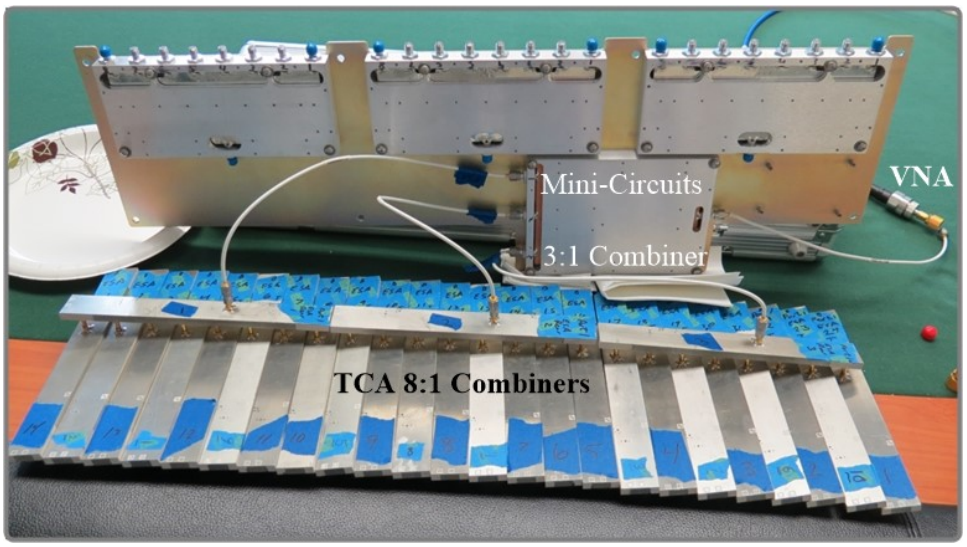


Fig. 17. TCA combiner measurement without TCA.

The Rev1 combiners demonstrate their impedance mismatch and design flaws impact TCA impedance. These problems appear in the TCA pattern measurements. Fig. 18 shows the TCA broadside gain. The Fig. 18 “dip and sag” describe gain losses covering 1.0 – 1.5 GHz and 1.75 – 2.5 GHz.

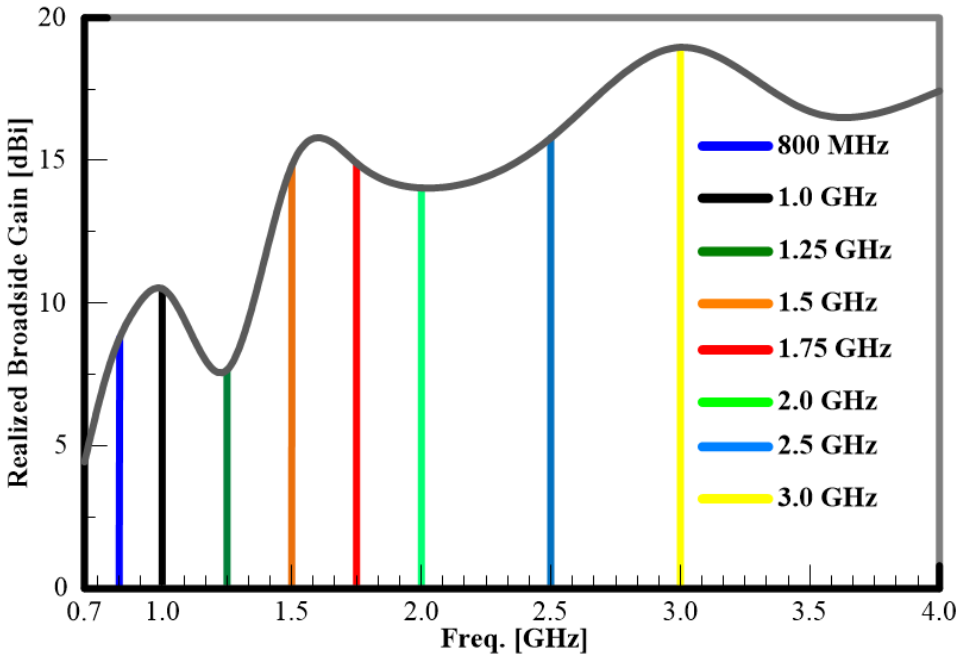


Fig. 18. Measured realized gain for 8 x 24 TCA.

All twenty-four columns sum to form the main pattern. I took broadside measurements for each column to check for combiner drop out. A 50Ω load terminated columns not measured. Fig. 19 displays the results. Assuming no combiner problems then measured gain will look uniform. The results show different combiners will cause gain loss or drop complete depending on frequency. The 2.5 GHz measurement displays the most dramatic impact. The gain dips in Fig. 19 varies by combiner and port showing combiner design problems influence entire antenna columns and individual elements.

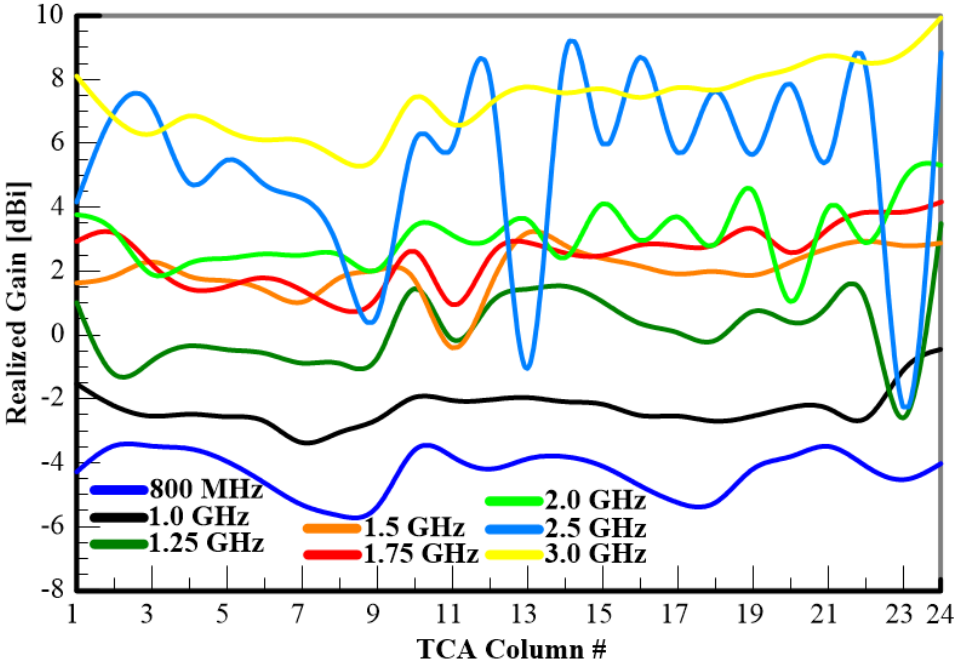


Fig. 19. Measured broadside realized gain across all 24 TCA columns.

I took insertion loss measurements for all combiners shown in Fig. 17. Fig. 20 shows fourteen insertion loss measurements compared with the Mini-Circuit 8:1 combiner. The Fig. 20 insertion loss dip covering 1.0 – 1.5 GHz also occurred in Fig. 18. The RF trap frequency varies and some combiners possess more than one notch. The Rev1 multilayer interconnect handling contribute to the RF trap. The notch frequency variance also demonstrates manufacturing difficulties.

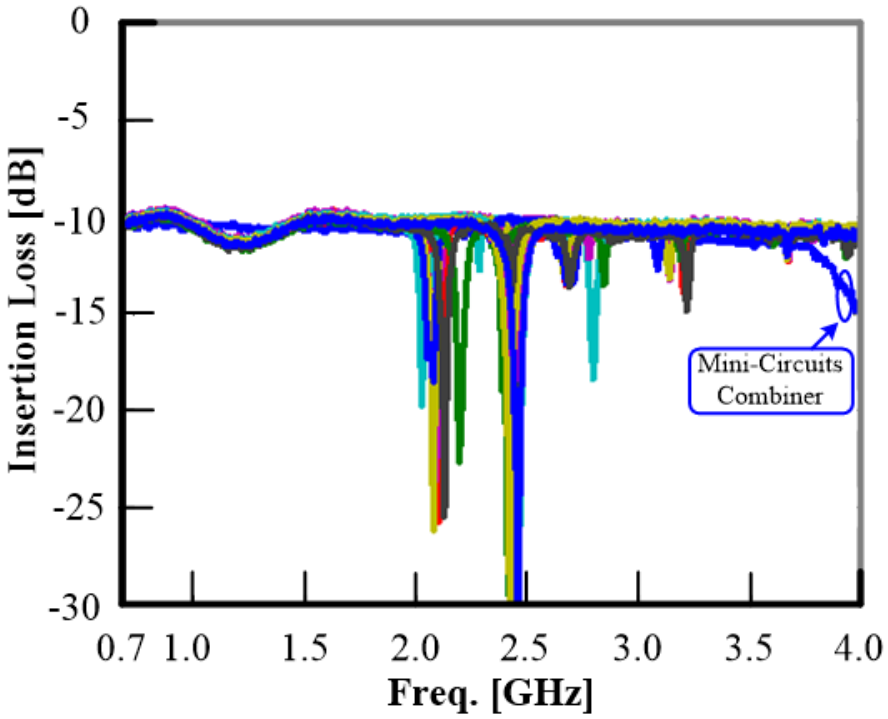


Fig. 20. Fourteen Rev1 combiner measurements plotted together.

The next section covers design and in-depth measurements for the original Wilkinson TCA combiner. These measurements reveal the problems that require redesign and deeper analysis.

III.B. Original Wilkinson TCA Combiner Design (Rev1)

My colleague, Roger, developed an initial design featuring a two stage and three level stripline Wilkinson combiner using the Tschebyscheff design process developed by Cohn [53]. Fig. 21 shows the two stage design. The space and weight requirements pushed for a multilayer design featuring embedded resistors made from OhmegaPly® [79]. Fig. 22 shows the three level stripline design.

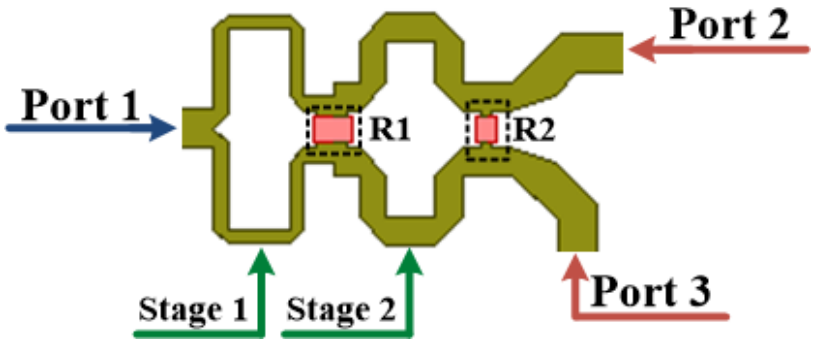


Fig. 21. Roger's two stage Wilkinson combiner.

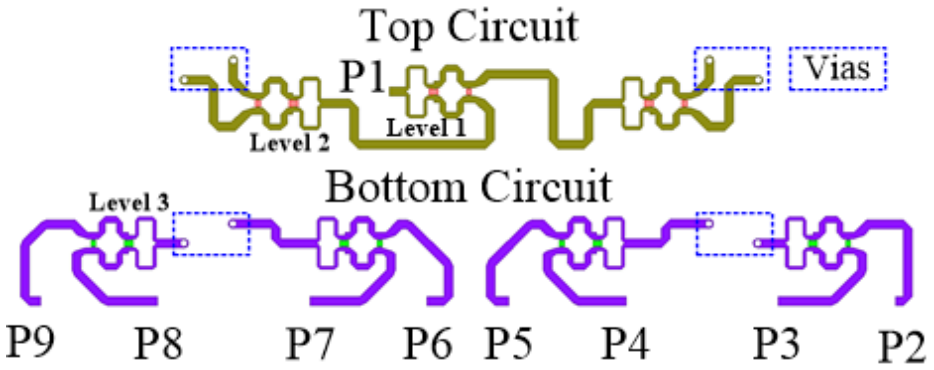


Fig. 22. Roger's two stage and three level stripline Wilkinson combiner.

Fig. 23 shows the CAD representation displaying internal circuitry and dimensions. The design possesses a 0.25 inch (6.35mm) fabrication thickness (**h**), an 8 inch (203.2mm) length (**L**), and 0.98 inch (24.89mm) width (**W**). The eight-inch length accounts for the TCA column length. The 0.98 inch width factors a small gap separating adjacent combiners to allow installation and comfortable seating. A discussion on interconnects occurs in chapter IV section IV.E.

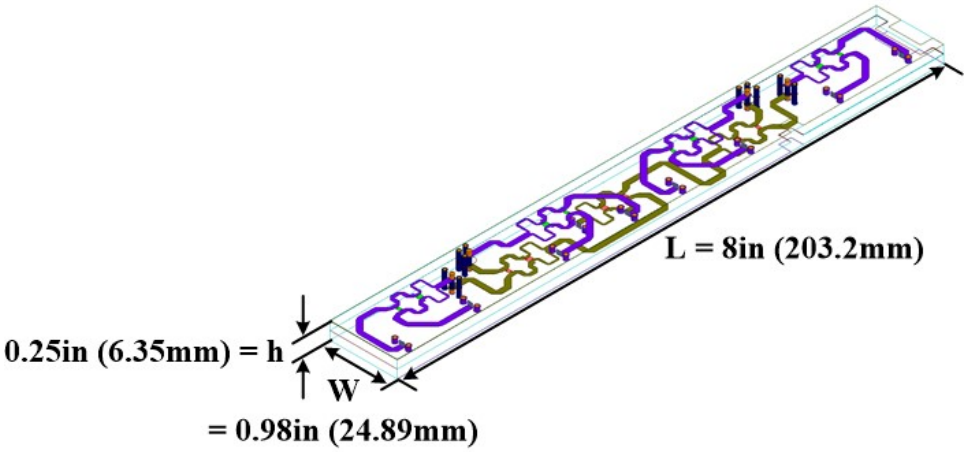


Fig. 23. Roger's combiner CAD representation.

Roger selected the Rogers RO3003™ [80], a ceramic-filled PTFE composite, became the circuit's foundation. The RO3003™ features possessed a 3.0 permittivity (ε_r), tanδ = 0.001, and 60mil (1.524mm) thickness. Four sheets glued together form the combiner. Fig. 24 displays the fabricated design. Resistor test pads, marked by the dashed red lines, allow verifying the correct embedded resistor values. The chemical etching feature test takes the smallest feature size and uses offsetting squares. The sharper the corners checks for over or under etching. Each port contains a soldered female SMP connector. Dashed blue boxes highlight the drill holes connecting the different layers. Aluminum coats the external copper layers to prevent corrosion. The electroplated aluminum connects the top and bottom ground layers on all four sides. The combiner weighs 2.5oz (70.87g). The painter's tape indicates TCA placement, orientation, port number, and testing order.

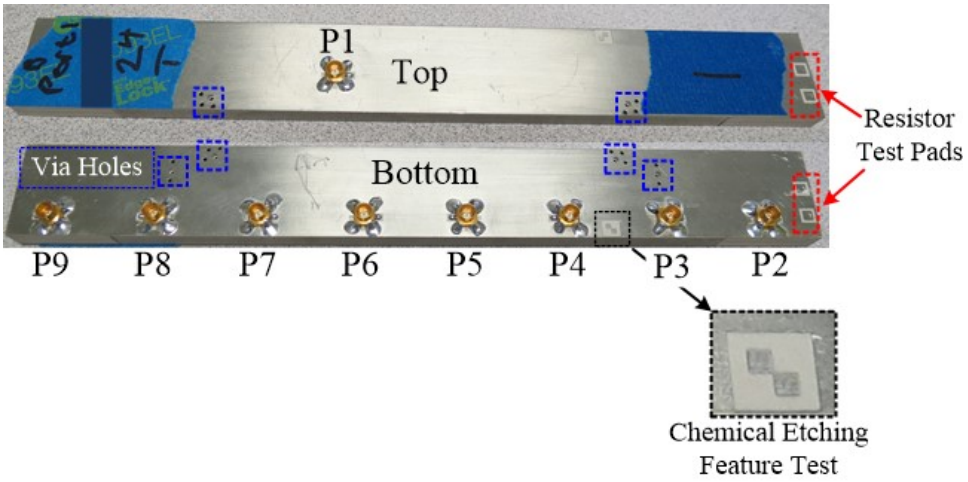


Fig. 24. Roger's fabricated combiner.

III.C. Rev1 Measurements

The author and assistance provided by colleague Jenn completed the Rev1 measurements, analysis, and antenna interaction testing. A Keysight FieldFox 9923A [81] tested and recorded the combiner measurements using custom designed phased matched cables from Times Microwave [82]. Fig. [27 - 39] show the measured results. Table VI provides a major result summary and comparison with the Mini-Circuit combiner.

TABLE VI
WILKINSON COMBINER REV1 MEASUREMENT COMPARISON

Source	Design Std.	Mini-Circuit [83]	Rev1
Freq. [GHz]	0.8 – 3	0.6 - 3.6	0.8 – 1, 1.5 – 2.4, 2.7 – 4
Bandwidth	3.75:1	6:1	1.25:1
Min. RL P1 [dB]	-15	-14	-2
Min. RL P2 – 9 [dB]	-20	-19	-12
VSWR P1	1.5:1	1.5:1	3.5:1
VSWR P2 - 9	1.4:1	1.4:1	1.7:1
IL [dB]	1 ± 0.5	1.5 ± 0.6	1.8 ± 0.64
Amp. Imbalance [dB]	± 0.5	± 0.5	± 0.85
Phase Unbalance	± 4.0°	± 4.0°	± 12.5°
Max Phase Std. Dev.	≤ ± 1°	± 1.54°	± 79.17°
Min. Iso. [dB]	-20	16.0	17

Fig. 25 displays averaged return loss, insertion loss, and isolation results. Each port and transmission path experienced analogous results. Port one offers a minimum -2dB return loss (P_1 RL) and Ports 2 – 9 possess a minimum -12dB return loss (Avg. P_{2-9} RL). The -11dB insertion loss remains constant except 1 – 1.5 GHz and 2.5 – 2.7 GHz. The 2.6 GHz mark indicates a notch filter or RF trap exists. Ports 2 – 9 possess a -17dB minimum isolation. Measured bandwidth stretches from 700 MHz to 4.0 GHz providing a 5.7:1 bandwidth. The Rev1 combiner possesses a limited operational frequency range: 800 MHz – 1 GHz, 1.5 GHz – 2.4 GHz, and 2.7 GHz – 4.0 GHz.

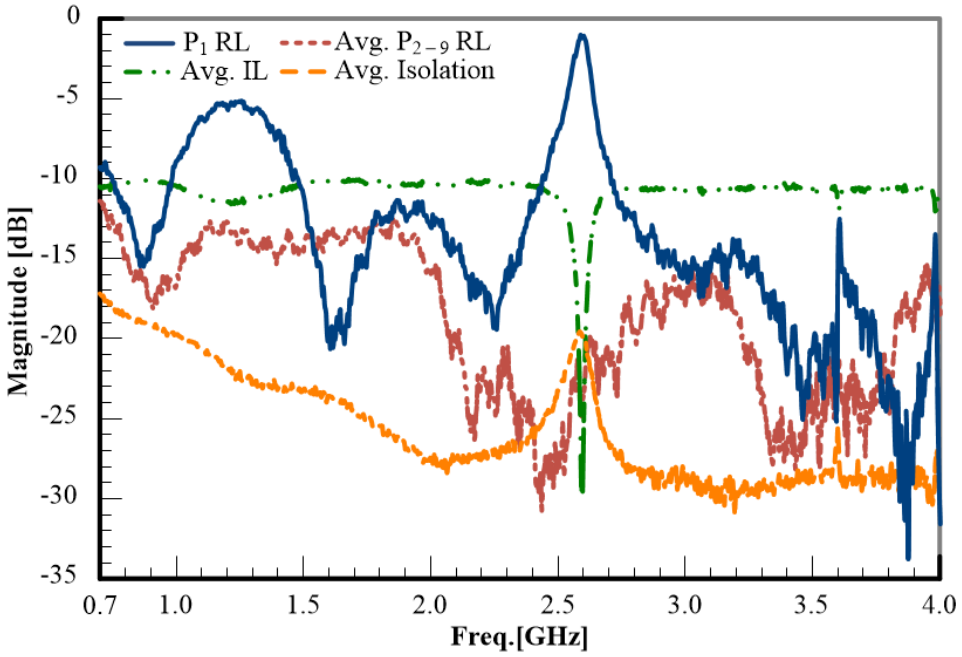


Fig. 25. Rev1 combiner measured results.

Fig. 26 and Fig. 27 presents the impedance information, first the VSWR then the Smith chart. Port one shows 1.9:1 average VSWR covering 700 MHz – 4.0 GHz. VSWR

describes a 1.59dB mismatch loss approximately reflecting 31.6% power at 1.2 GHz. The Port one mismatch loss excludes the 2.5 GHz notch. Ports 2 – 9 possess an average 1.3:1 VSWR, 3% reflected power, and 0.33dB mismatch loss. The Smith charts show a good 50Ω impedance match for Ports 2 – 9 and mediocre impedance match for Port one.

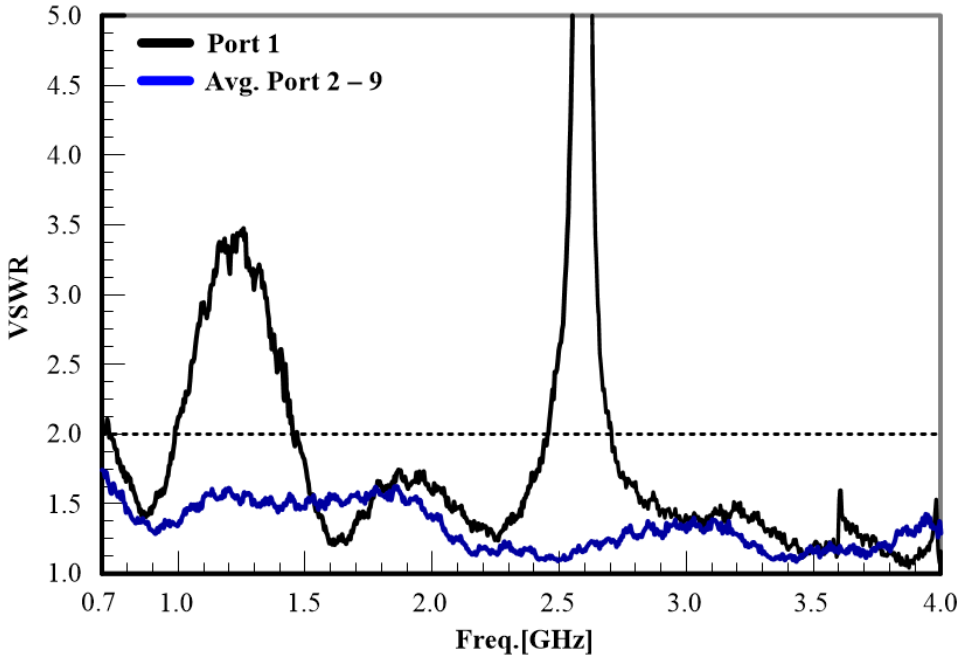
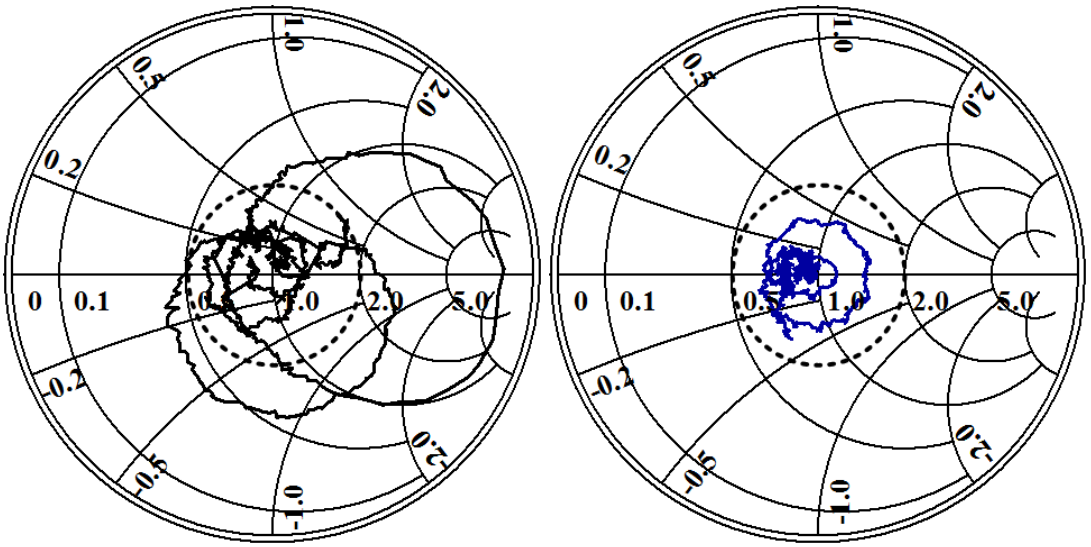


Fig. 26. Rev1 combiner VSWR measured results.



(a) (b)

Fig. 27. Rev1 combiner measured impedance from 700 MHz to 4.0 GHz with the dashed circle marking VSWR = 2: (a) Port one and (b) Ports 2 – 9.

Fig. 28 - 32 discuss the transmission phase. Fig. 28 shows good agreement from Ports 2 – 9 from 700 MHz to 1.5 GHz and deteriorating agreement 1.5 – 4.0 GHz. The 2.6 GHz notch forces a phase inflection. The transmission paths from Port one to Ports 2 – 9 possess a poorer insertion loss. Manufacturing errors and impedance matching errors cause the varying insertion loss for the eight transmission paths. Additional transmission path losses cause phase to lag. Fig. 29 gives a magnified phase view covering 1.795 to 1.805 GHz and displaying a ± 12.5^{o} transmission phase variation. Fig. 30 shows the average phase difference.

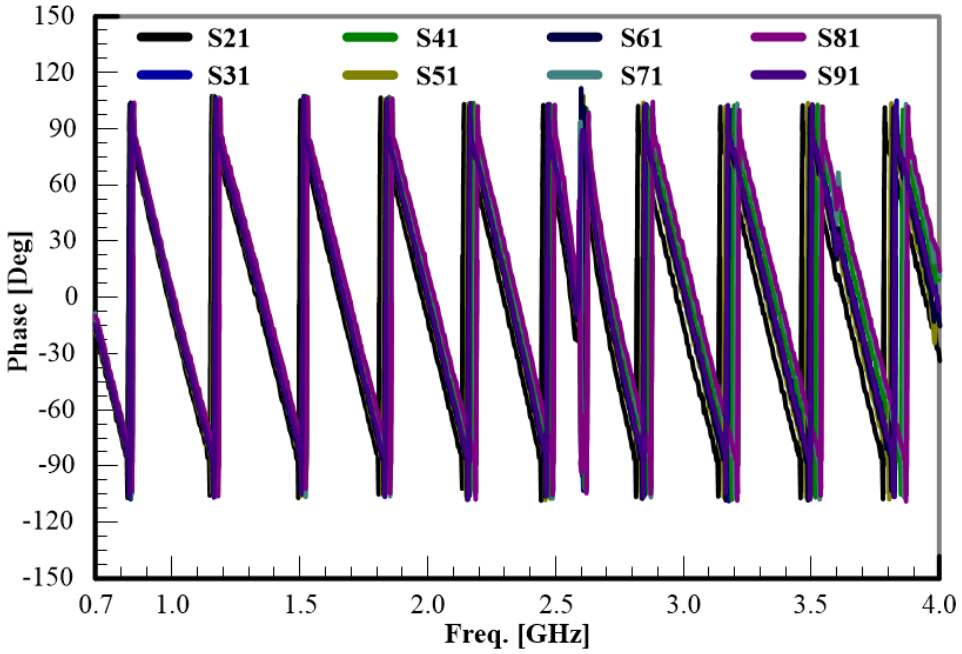


Fig. 28. Rev1 combiner measured transmission phase from Ports 2 – 9 to Port one.

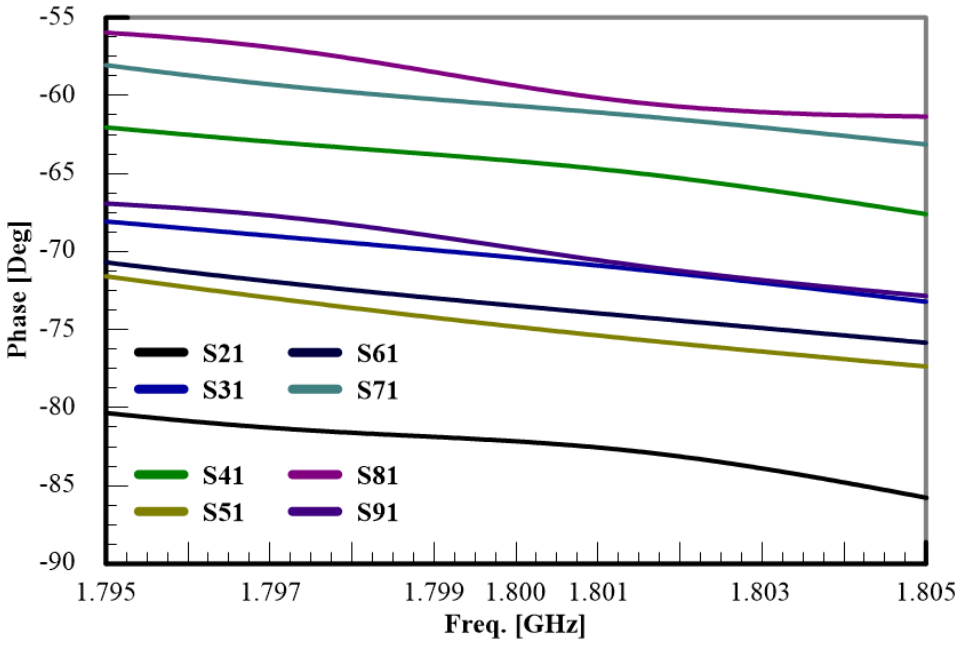


Fig. 29. Rev1 measured transmission phase from Ports 2 – 9 to Port one showing phase stability.

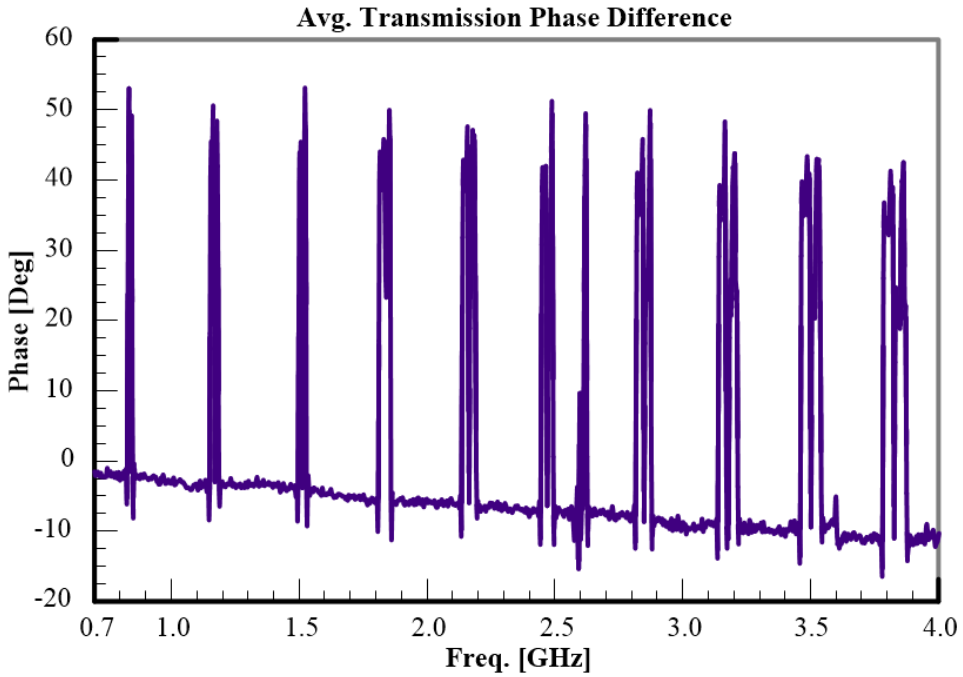


Fig. 30. Rev1 combiner measured average transmission phase difference from Ports 2 – 9 to Port one.

Fig. 31 and Fig. 32 display phase information for specific frequencies. Fig. 31 shows a 30^{o} maximum and minimum phase swing. Fig. 32 shows phase variance across the operating spectrum. Table VII lists the inter-port mean phase standard deviation in 200 MHz steps. The standard deviation (σ) increases from 3^{o} to 12^{o}.

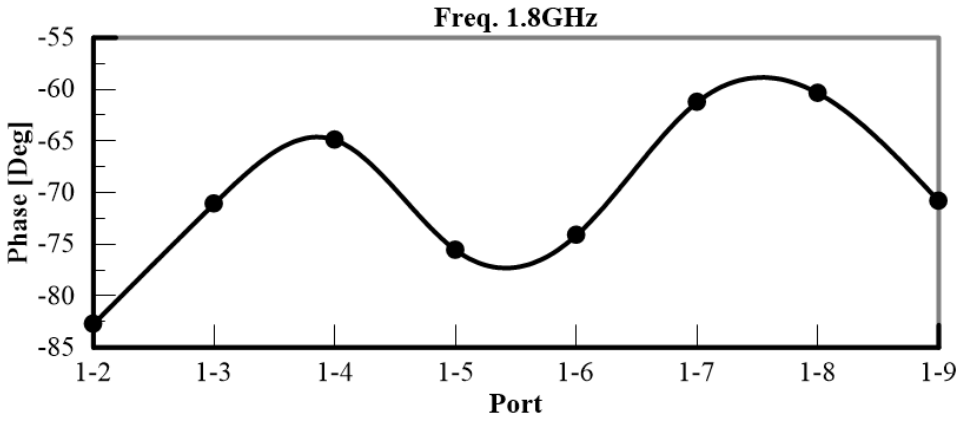


Fig. 31. Rev1 measured 1.8 GHz transmission phase from Ports 2 – 9 to Port one.

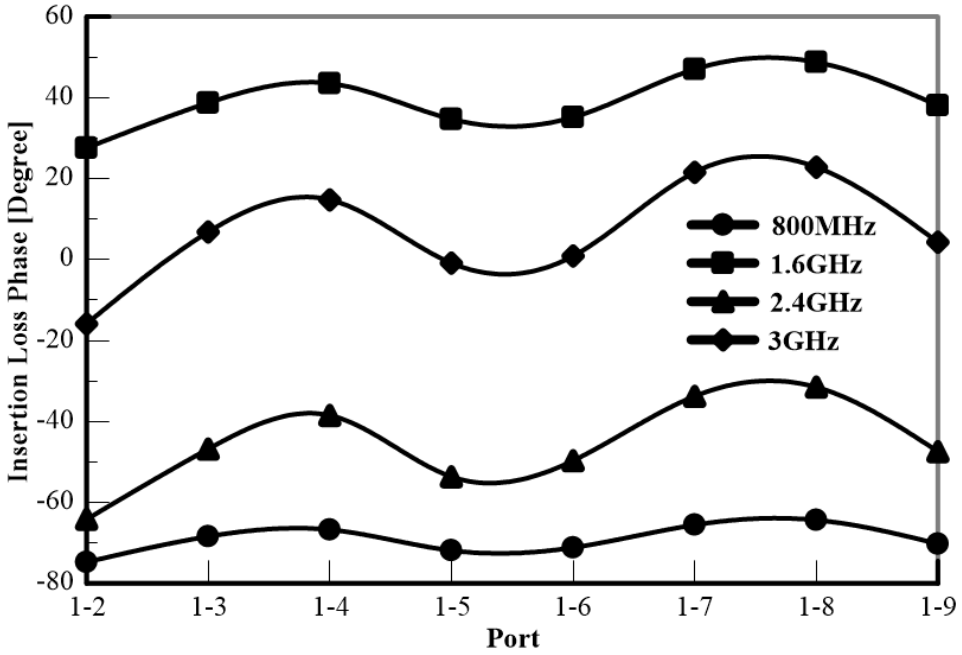


Fig. 32. Rev1 measured transmission phase from Ports 2 – 9 to Port one.

TABLE VII
REV1 PHASE ERROR

Freq. [GHz]	Mean	σ [+/- Deg.]
0.8	-69.12	3.28
1.0	-1.92	4.27
1.2	73.52	5.15
1.4	27.71	5.40
1.6	39.19	6.56
1.8	-70.12	7.13
2.0	0.34	8.18
2.2	71.54	9.21
2.4	-45.68	10.12
2.6	-18.59	79.17
2.8	-61.52	11.15
3.0	6.80	11.99

Fig. 33 shows the tri-level combiner insertion loss higher than 9dB. The combiner provides a -1.8dB mean isertion loss. The insertion loss remains stable except spans 1.0 – 1.5 GHz and 2.5 – 2.7 GHz. Measurements indicate 0.64dB mean loss for one transmission path.

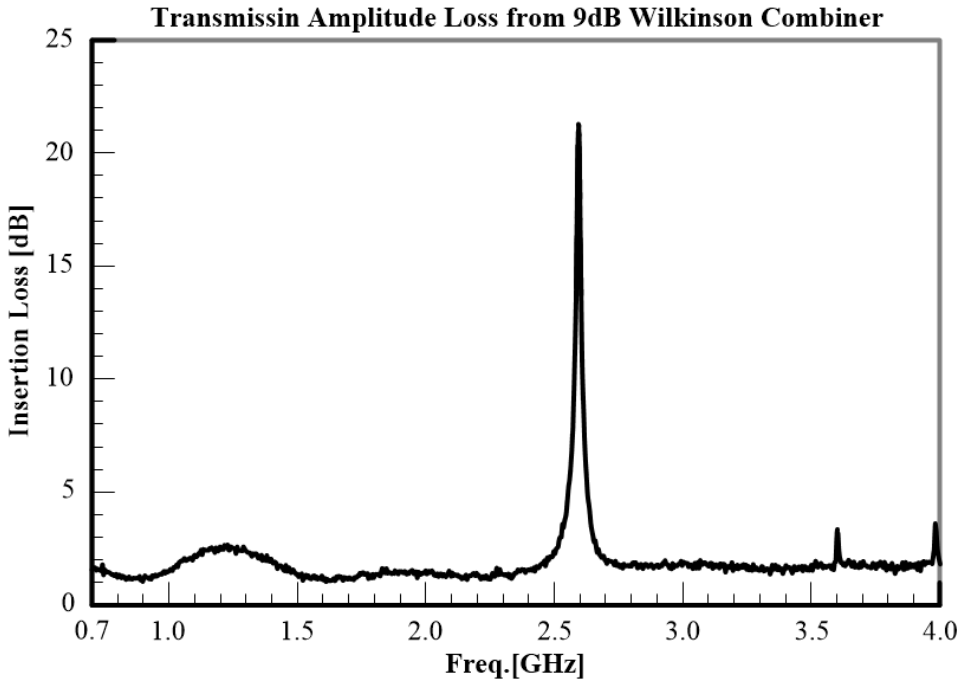


Fig. 33. Rev1 combiner average insertion loss measured from Ports 2 – 9 to Port one.

Fig. 34 displays static frequency insertion loss per port. The insertion loss variance and the mean 0.64dB loss per transmission path spanning 800 MHz and 3.0 GHz don't agree. The insertion loss fluctuates ± 1.125dB from maximum (-11.75dB) to minimum (-9.5dB). Fig. 34 shows inconsistent transmission path losses based on port path.

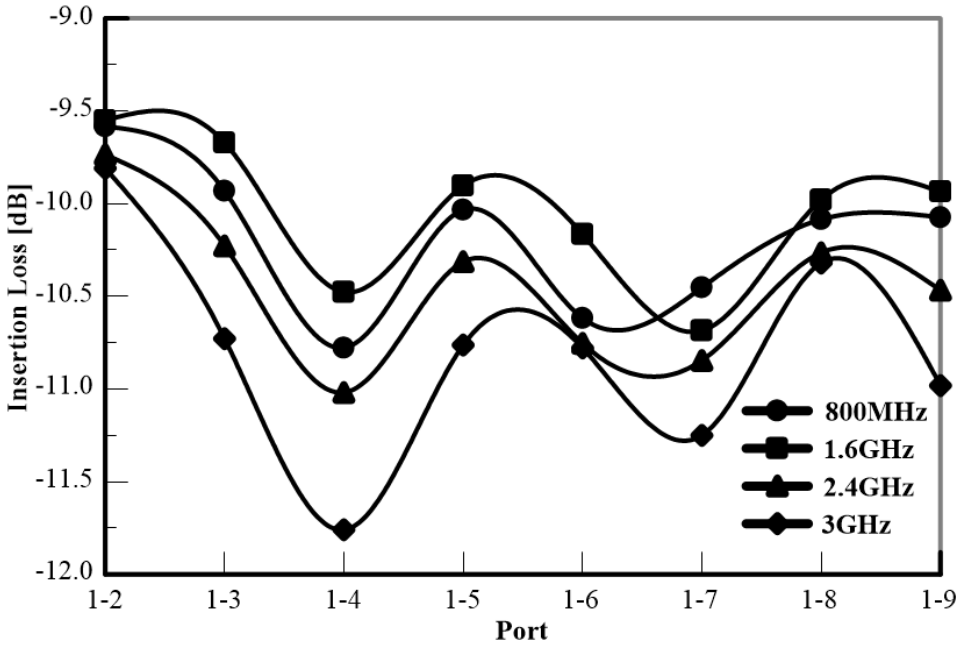


Fig. 34. Rev1 measured static frequency insertion loss from Ports 2 – 9 to Port one.

Fig. 35 shows isolation by port for four frequencies. Diverse parallel path combinations establish isolation consistency. The frequencies spanning 800 MHz and 1.6 GHz possess less isolation than frequencies higher than 1.6 GHz. When ports branch off the same combiner, see 23, 45, and 67 in Fig. 35, the isolation diminishes. Increasing frequency increases the electrical length separating adjacent output ports producing

increased isolation. Fig. 35 confirms stripline via picket fence missing. The via picket fence isolates transmission lines and suppress parallel plate modes.

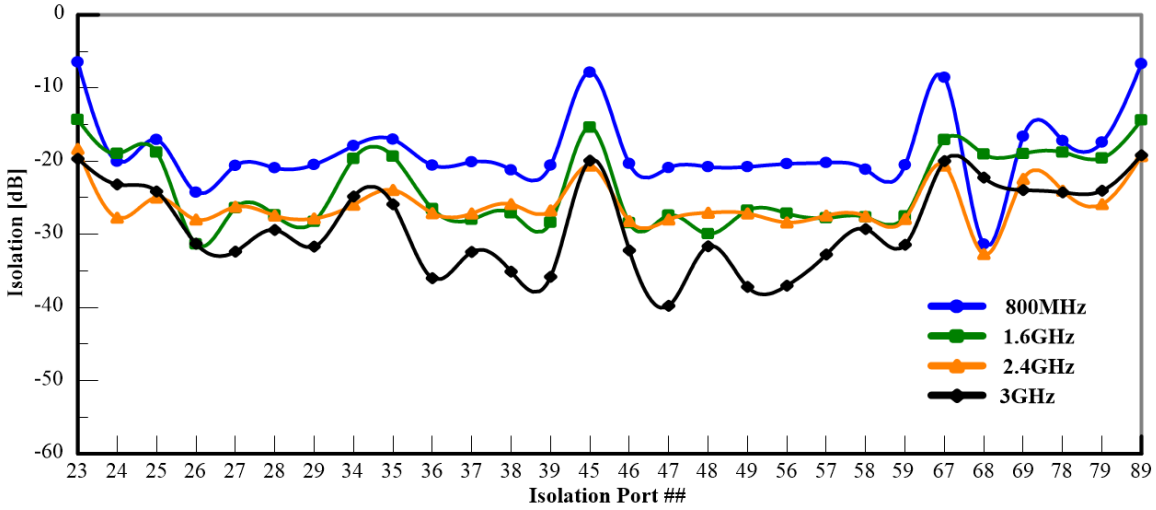


Fig. 35. Rev1 Ports 2 – 9 isolation static frequency measurements.

Fig. 36 displays the average amplitude difference traversing all signal transmission paths. Subtracting transmission magnitudes ($|S_{21}| - |S_{31}|$) provides amplitude imbalance. I completed these calculations for 28 combinations and found the mean. The 2.1dB max and 0.4dB minimum amplitude differences provide a ± 0.85dB amplitude fluctuation producing a < 0.5dB average difference spanning 700 MHz and 4.0 GHz.

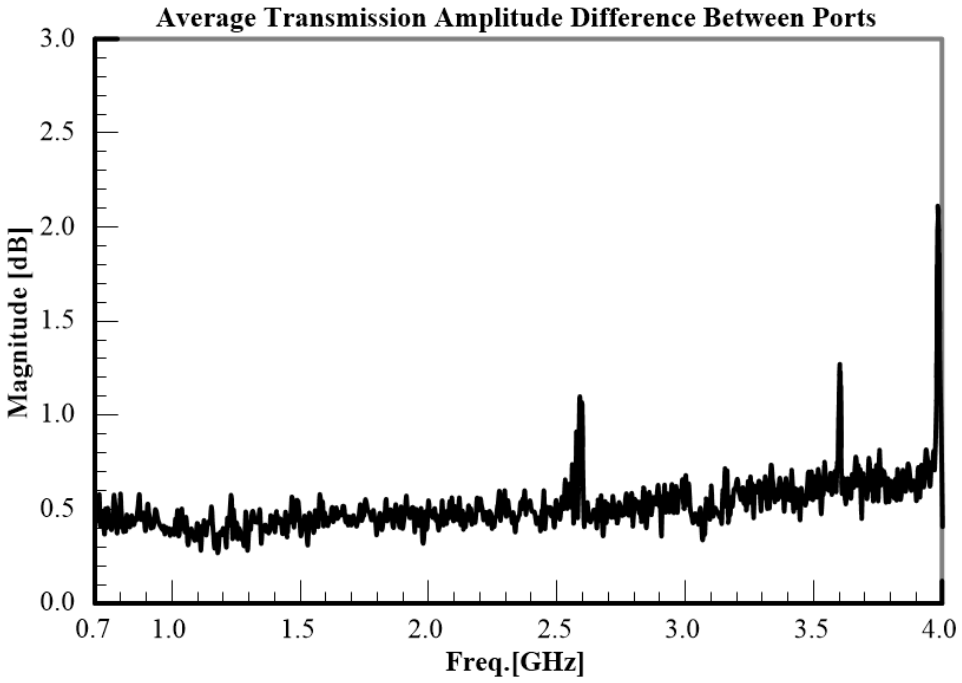


Fig. 36. Rev1 combiner amplitude imbalance measured from Ports 2 – 9 to Port one.

Fig. 37 displays Rev1 signal combining efficiency. The combiner offers an average single path loss from Port one to Port 2 – 9 of 0.64dB. Fig. 37 illustrates eight combined signals offer a 70% starting efficiency assuming 0.6dB loss. Fig. 37 illustrates an approximate 70% efficiency swinging ± 10% and a momentary plummet.

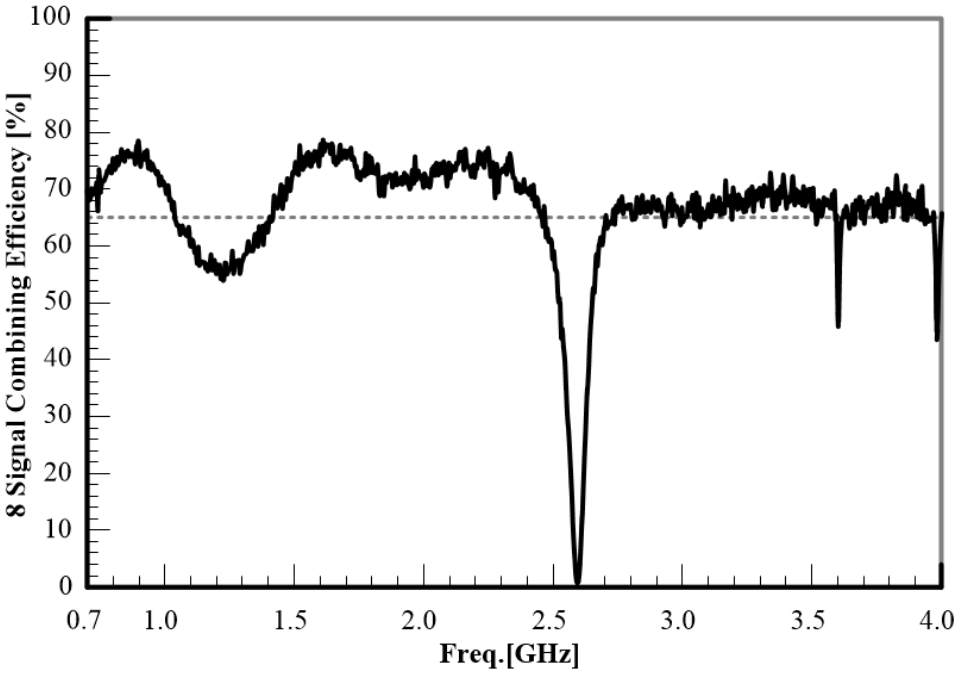


Fig. 37. Rev1 combiner efficiency extracted from averaged power transmitted from Ports 2 – 9 to Port one.

CHAPTER IV

SOLVING THE UWB COMBINER PROBLEM

IV.A. Design Requirements

A. M. Abbosh, a University of Queensland professor in St. Lucia, Australia, made the following observation perusing his multi-layer WPC, "*The exploding growth of wireless communication systems has led to increasing demand for the multilayer integration technology…*" [66].

The weighty and bulky designs Table VIII presents necessitate examining alternatives. Their encumbrance and dimensions inhibit adoption. The UWB Wilkinson topology design encompasses UHF, L-, and S-bands. The new combiner interfaces with an UWB TCA provided by Bit Systems. The experimental TCA divides into twenty-four columns with each column containing eight unit cells. One inch by one inch square defines the unit cell. The Wilkinson power combiner (WPC) contains eight input ports and one output port. Twenty-four combiners will mount to the TCA backplane. The new combiner condenses the 2-D array (8x24) down to a 1-D or linear array (1x24). Each TCA unit cell contains a female SMP connector. Adjacently seating the combiners forces compactness and low profile necessitates a multilayer design.

The combiner design requires minimal phase error, equal power reception, low power handling, weighs less than one pound, and less than or equal to half an inch thick and adds electromagnetic interference (EMI) and electromagnetic compatibility (EMC) signal protection.

IV.B. Mass Manufactured Combiners Not the Answer

Purchasing an evaluation combine mandated scrutinizing several combiner data sheets [83 – 86] and comparing information. Table VIII summarizes the comparison data. Their size and weight dissuaded me from purchasing them for TCA integration. The ZB8PD-362+ smaller size and accessible information provided an edge compared alongside three other competing models.

TABLE VIII
MANUFACTURED WILKINSON POWER COMBINER COMPARISON

Manufacturer	Mini-Circuits [83]	RF-Lambda [84]	Pasternac [85]	Fairview Microwave [86]
Model Number	ZB8PD-362+	RFLT8W0504G	PE2091	MP8213-8
Frequency	0.6 - 3.6 GHz	0.5 – 4 GHz	0.69 - 2.7 GHz	0.7 - 2.7 GHz
Length	7.1in	7.5in	8.3in	8.0in
Width	3.13in	5.12in	4.70in	4.64in
Weight	2lbs	-	-	-
Insertion Loss	1.5dB ± 0.6dB	1.9dB ± 1dB	1.2dB	1.0dB
Amplitude Imbalance	± 0.5dB	± 0.5dB	± 0.5dB	± 0.8dB
Phase Unbalance	± 4.0°	± 4.0°	± 8.0°	-
Minimum Isolation	16.0dB	16.0dB	20.0dB	20.0dB
VSWR Port 1	1.5:1	1.8:1	1.4:1	1.4:1
VSWR Ports 2 - 9	1.4:1	1.2:1	-	1.2:1

Designing an eight input to one output combiner for compact and lightweight UWB hardware necessitated obtaining minimum design standards and comparative measurements. The Mini-Circuits ZB8PD-362+ combiner pictured in Fig. 38 met the frequency requirements and based on the data sheet information in Table VII would work except for three points. The ZB8PD-362+ 2.63 inch width, 2lb weight, and non-SMP interface prevented adopting the combiner.

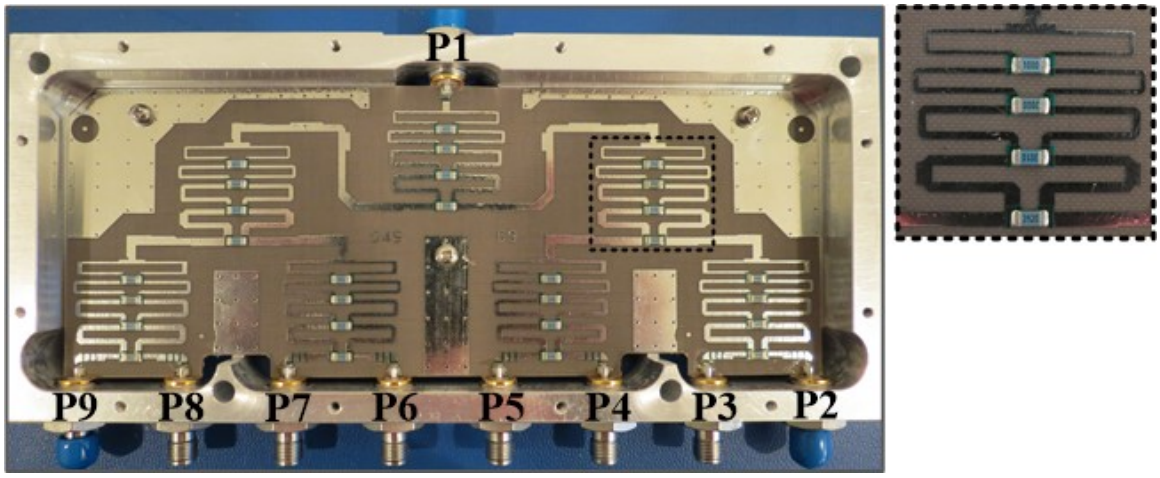


Fig. 38. Mini-Circuits ZB8PD-362+ eight to one Wilkinson power combiner.

The ZB8PD-362+ design features three levels and four stages constructed on FR4. The top copper layer coated by tin to prevent oxidation. A sturdy aluminum housing contains the design. The ZB8PD-362+ design included capacitive loading to improve impedance matching, stepped impedance transformers, and low pass filters for harmonic suppression. The ZB8PD-362+ measured 3.13 inches (79.5mm) wide, 7.06 inches (179.3mm) long, and weighed 1.76lbs (800g) without the top and bottom aluminum plates.

A Keysight FieldFox RF Vector Network Analyzer (VNA) 9923A [81] tested and recorded the combiner measurements using custom designed phased matched cables from Times Microwave [82]. Fig. [38 – 50] show the measured results. Table IX provides a major result summary and data sheet comparison.

TABLE IX
MINI-CIRCUIT ZB8PD-362+ DATA COMPARISON

Source	Data Sheet [83]	Measurements
Frequency	0.6 - 3.6 GHz	0.7 – 3.6 GHz
Insertion Loss	1.5dB ± 0.6dB	1.22dB ± 0.4dB
Amplitude Imbalance	± 0.5dB	± 0.675dB
Phase Unbalance	± 4.0°	± 3.0°
Minimum Isolation	16.0dB	10dB
VSWR Port 1	1.5:1	1.5:1
VSWR Ports 2 - 9	1.4:1	1.4:1

Fig. 39 displays averaged return loss, insertion loss, and isolation results. Each port and transmission path experienced analogous results. Port one possesses a minimum -14dB return loss (P_1 RL) and Ports 2 – 9 possess a minimum -19dB return loss (Avg. P_{2-9} RL). A -10dB insertion loss remains stable. Measured bandwidth stretches from 700 MHz to 3.7 GHz providing 5.3:1 bandwidth. Ports 2 – 9 possess a -30dB minimum average isolation. The low pass filter holds a 3.7 GHz or -3dB cutoff.

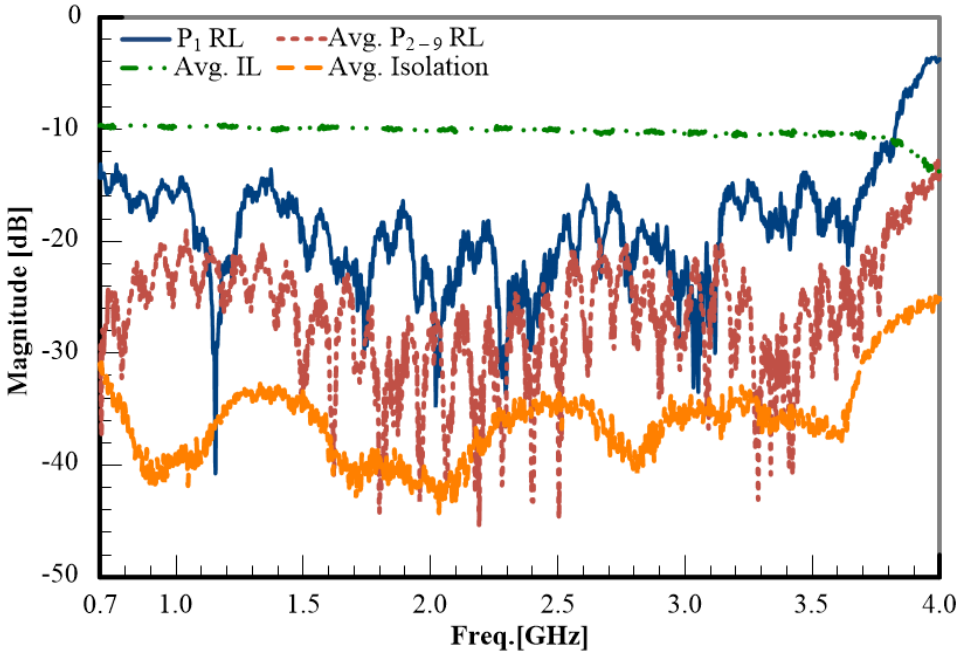


Fig. 39. Mini-Circuits combiner measured results.

Fig. 40 and Fig. 41 presents the impedance information, first the VSWR then the Smith chart. Port one expresses a 1.6:1 VSWR, 5% reflected power, and 0.36dB mismatch loss covering 700 MHz to 3.7 GHz. Ports 2 – 9 show an averaged VSWR of 1.3:1, 2% reflected power, and 0.08dB mismatch loss. The Smith charts show a good 50Ω impedance match for Ports 1 – 9.

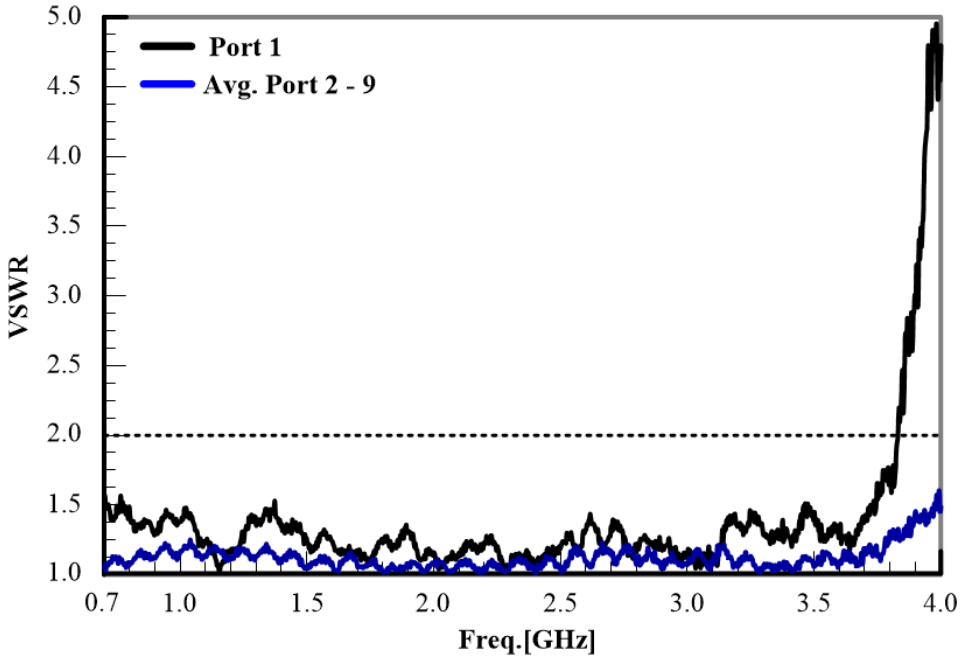
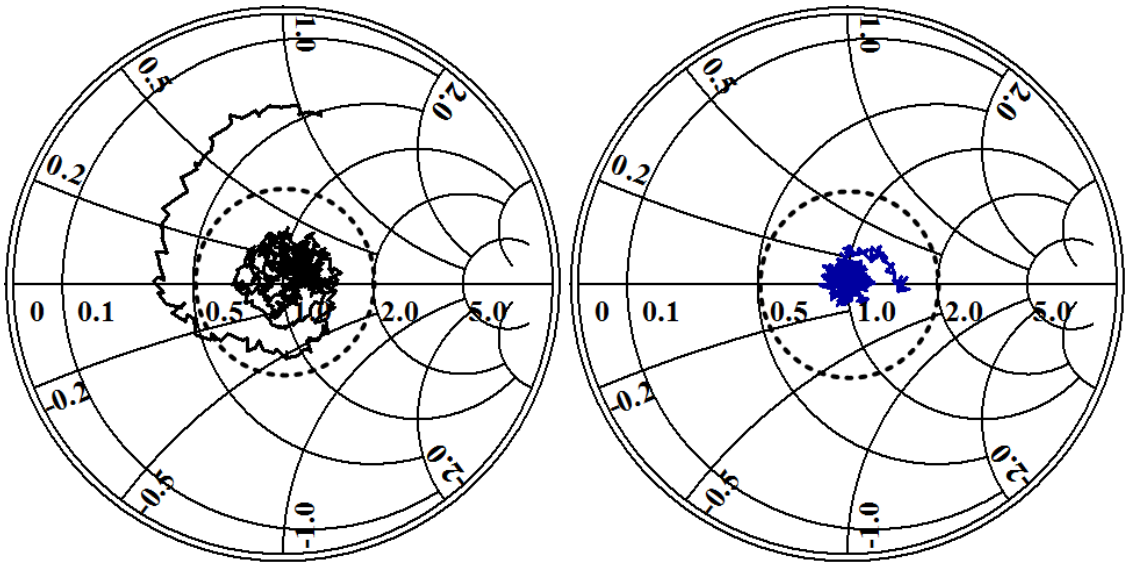


Fig. 40. Mini-Circuit combiner VSWR measured results.



(a) (b)

Fig. 41. Mini-Circuit combiner measured impedance from 700 MHz to 4.0 GHz with the dashed circle marking VSWR = 2: (a) Port one and (b) Ports 2 – 9.

Fig. 42 - 46 discuss the transmission phase. Fig. 42 shows good agreement from Ports 2 – 9. Fig. 43 provides a magnified phase view covering 1.795 to 1.805 GHz and displaying a ± 3^{o} transmission phase variation. Fig. 44 displays a ± 0.5^{o} average phase difference across frequency and ports.

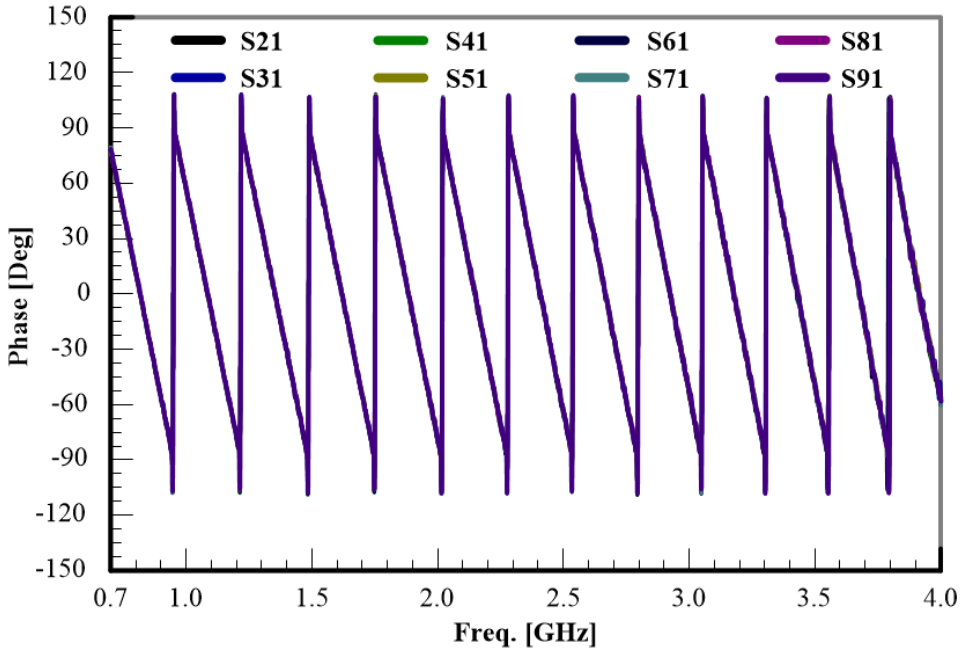


Fig. 42. Mini-Circuit combiner measured transmission phase from Ports 2 – 9 to Port one.

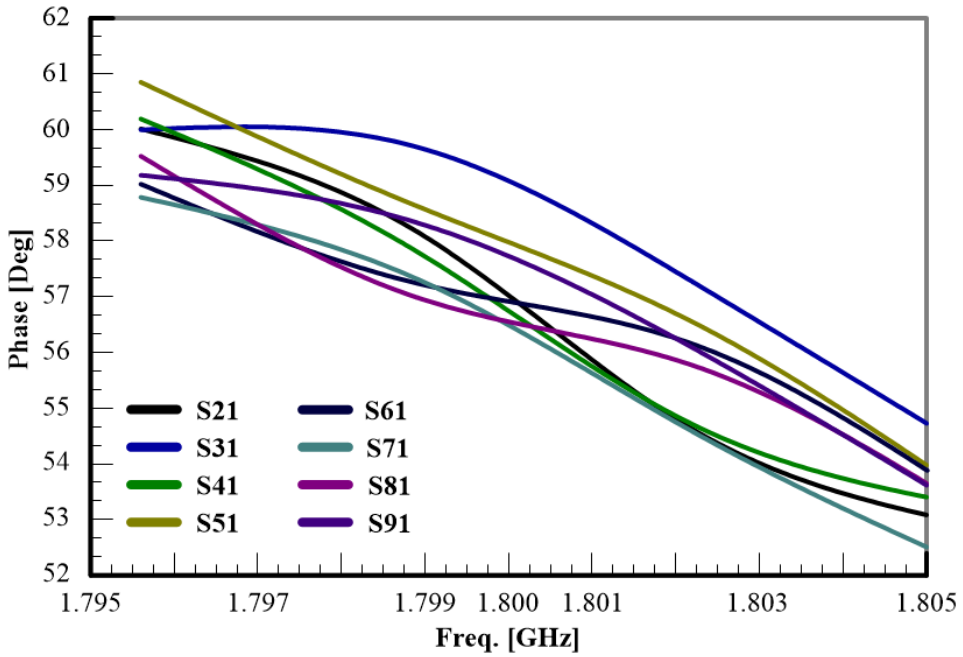


Fig. 43. Mini-Circuit measured transmission phase from Ports 2 – 9 to Port one showing phase stability.

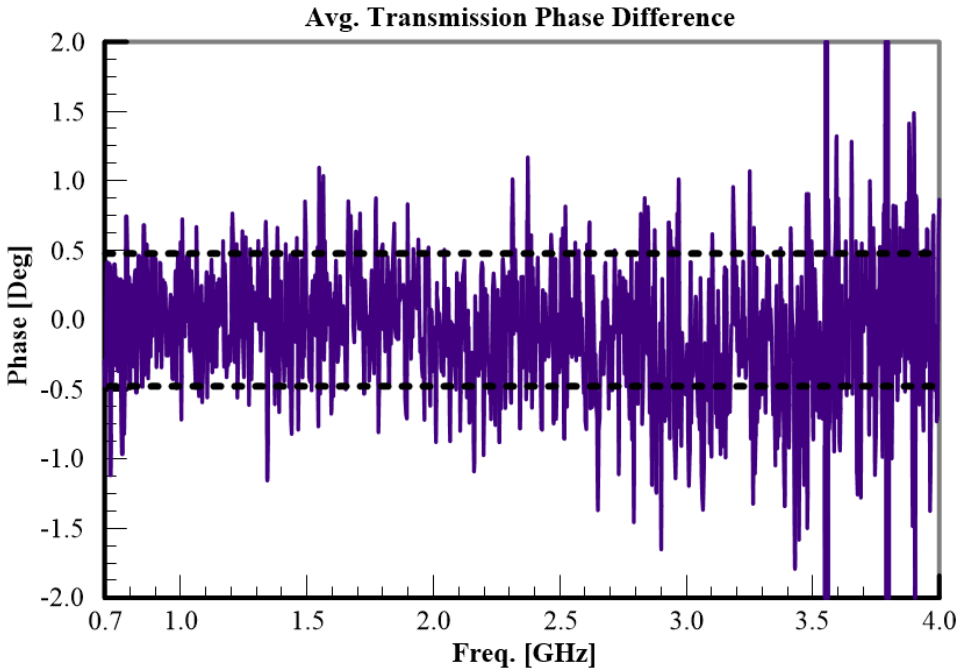


Fig. 44. Mini-Circuit combiner measured average transmission phase difference from Ports 2 – 9 to Port one.

Fig. 45 and Fig. 46 display phase information for specific frequencies. Fig. 45 shows a 3^{o} maximum and minimum phase swing. Fig. 46 shows phase variance remains constant. Table X lists the transmission path mean phase standard deviation in 200 MHz steps. The standard deviation shows a 3^{o} swing consistent with Fig. 45 and Fig. 46 and agrees with Table X.

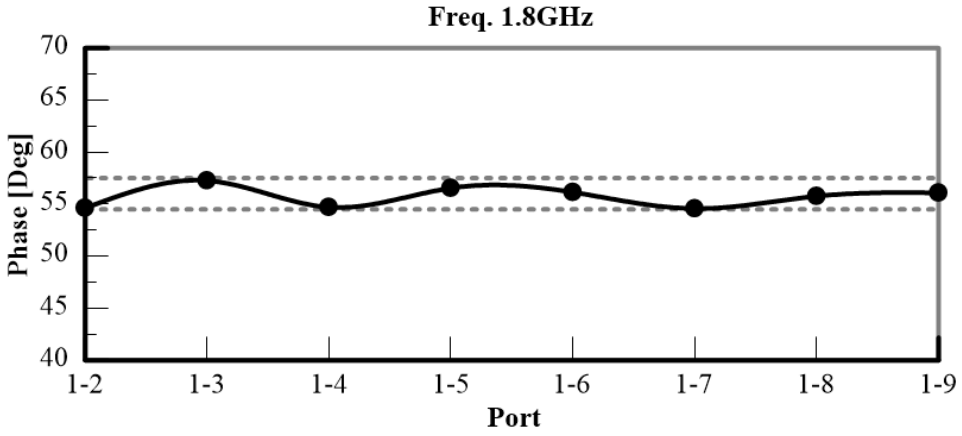


Fig. 45. Mini-Circuit measured 1.8 GHz transmission phase from Ports 2 – 9 to Port one.

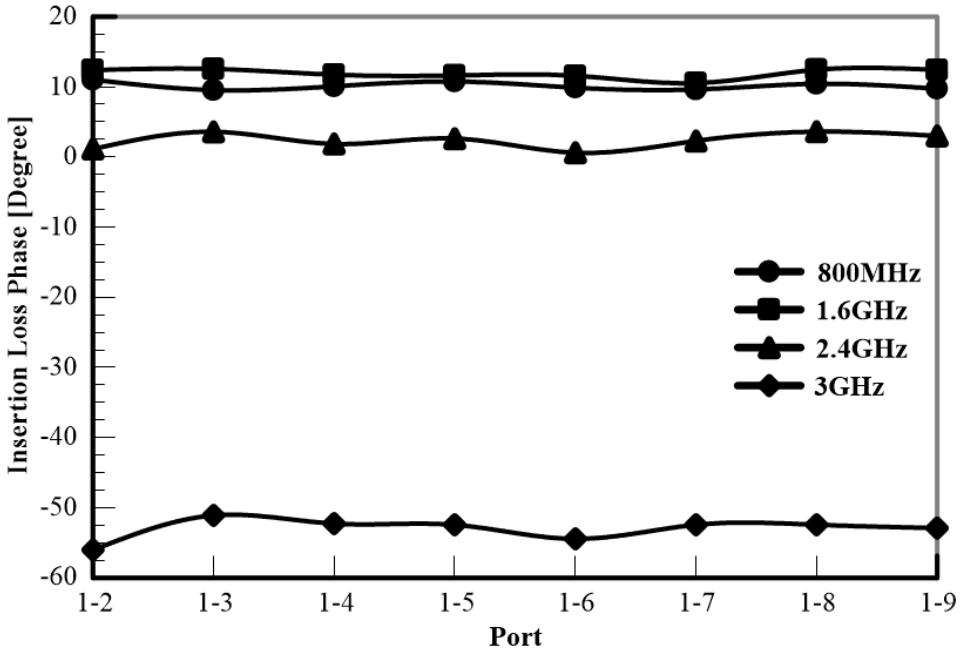


Fig. 46. Mini-Circuit measured transmission phase from Ports 2 – 9 to Port one.

TABLE X
ZB8PD-362+ PHASE ERROR

Freq. [GHz]	Mean	σ [+/- Deg.]
0.8	10.13	0.51
1.0	56.88	0.68
1.2	-78.22	1.07
1.4	-32.03	1.54
1.6	11.89	0.64
1.8	55.72	0.93
2.0	-79.23	0.66
2.2	-37.10	0.55
2.4	2.34	1.02
2.6	46.72	1.17
2.8	85.64	1.02
3.0	-52.99	1.43

Fig. 47 shows the three level combiner insertion loss higher than 9dB. Possesses a -1.22dB mean isertion loss. Loss increases linearly until 3.8GHz cutoff or -3dB point. Measurements show a 0.4dB average loss for each transmission path. The losses orginiate from eletrical lengths increasing, immpedance mismatch, parastics from solder, solder pads, and chip resistors, dielectric varience from frequency response, and connector losses.

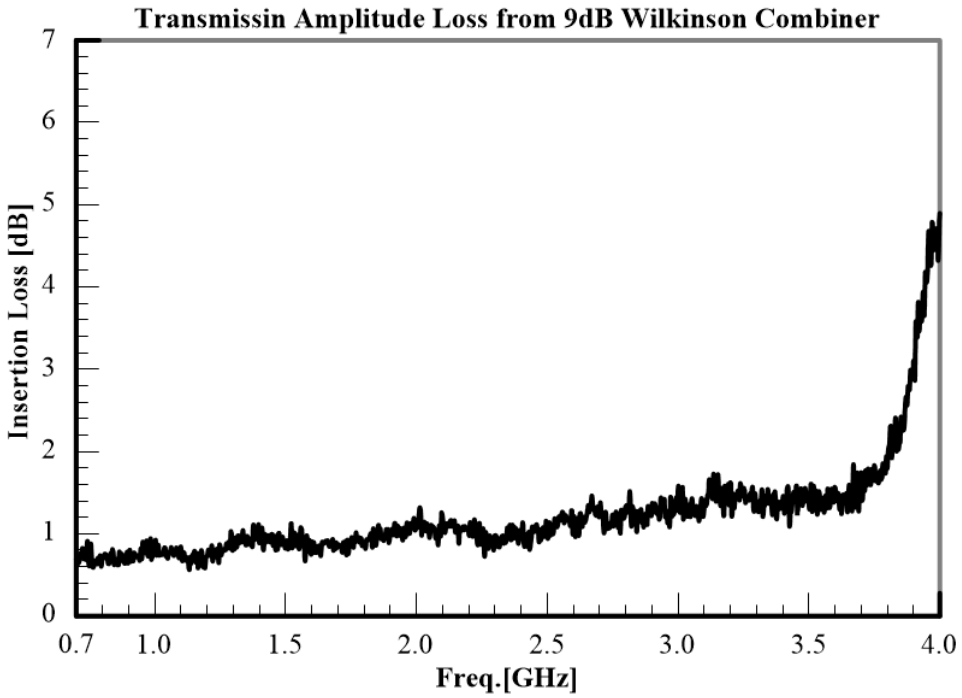


Fig. 47. Mini-Circuit combiner average insertion loss measured from Ports 2 – 9 to Port one.

Fig. 48 displays insertion loss results covering static frequencies. The insertion loss variance and 0.4dB loss swing per transmission path agree covering 800 MHz – 2.4 GHz. When the filter's 1dB frequency nears, ringing appears. The electrical transmission line lengths contracted. Smaller wavelengths introduce additional loss when propagating distance increases. The opposite occurs for lower frequencies.

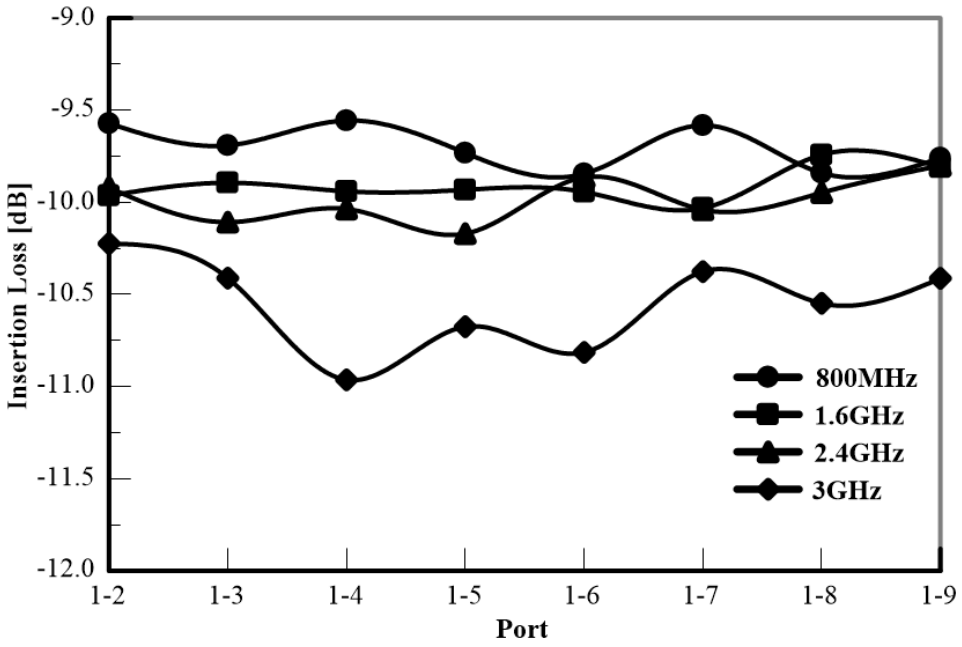


Fig. 48. Mini-Circuit measured insertion loss from Ports 2 – 9 to Port one.

Fig. 49 shows static frequency isolation by different port combinations establishes consistency. When ports branch off the same combiner, see 23, 45, and 67 the isolation decreases.

When the frequency increases, the electrical distance increases between adjacent output transmission paths increasing path isolation.

Fig. 38 displays a shorting wall or fence between combiners. The Mini-Circuit shorting wall supports good signal isolation.

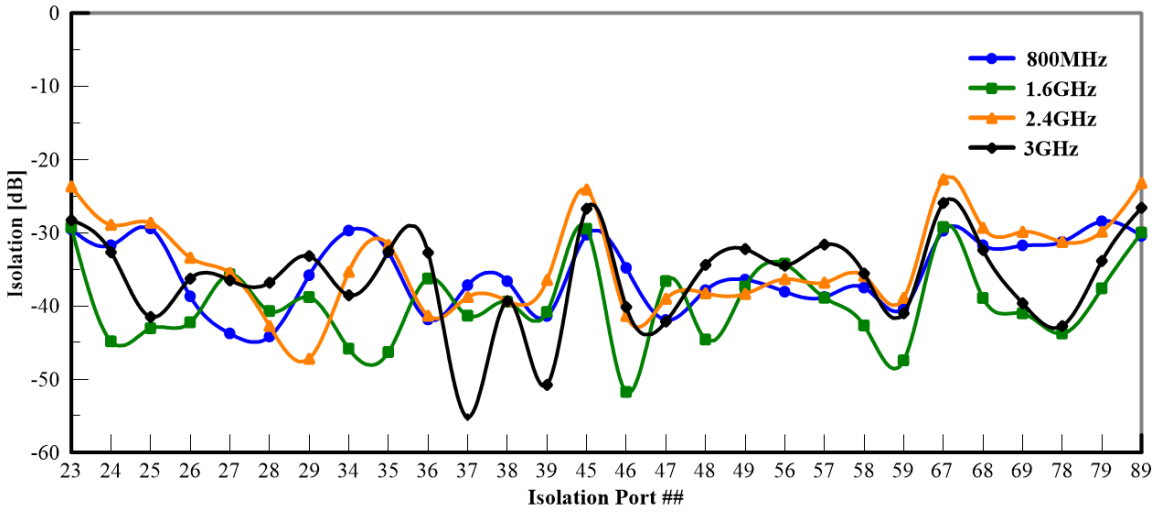


Fig. 49. Mini-Circuit isolation static frequencies measured between Ports 2 – 9.

Fig. 50 displays the average amplitude difference traversing all signal transmission paths. Amplitude imbalance determined by taking the transmission magnitude (S_{21}) and subtracting S_{31}. I performed isolation measurements for twenty-eight combinations. A 1.35dB max difference and 0dB minimum provides a ± 0.675dB amplitude swing with an average difference less than 0.4dB between 700 MHz and 4.0 GHz.

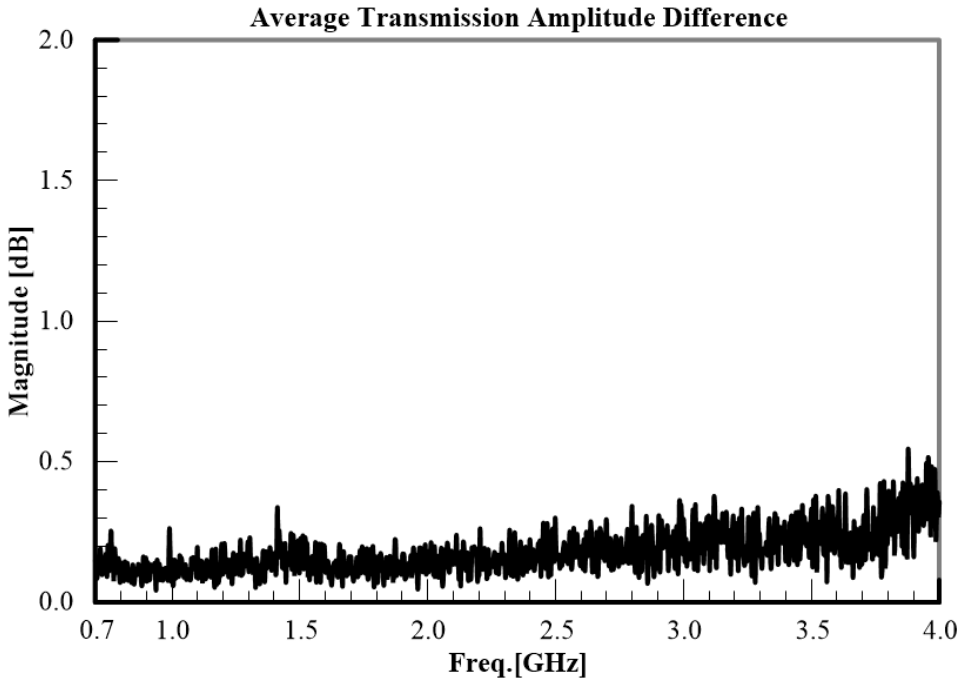


Fig. 50. Mini-Circuit combiner amplitude imbalance measured from Ports 2 – 9 to Port one.

Fig. 51 displays the signal combining efficiency. The combiner offers an average single path loss from Port one to Ports 2 – 9 of 0.4dB. Based on Fig. 51, eight combined signals possess an 80% starting efficiency. Fig. 51 shows an ~ 88% starting efficiency and declines till ~ 72% then plummets.

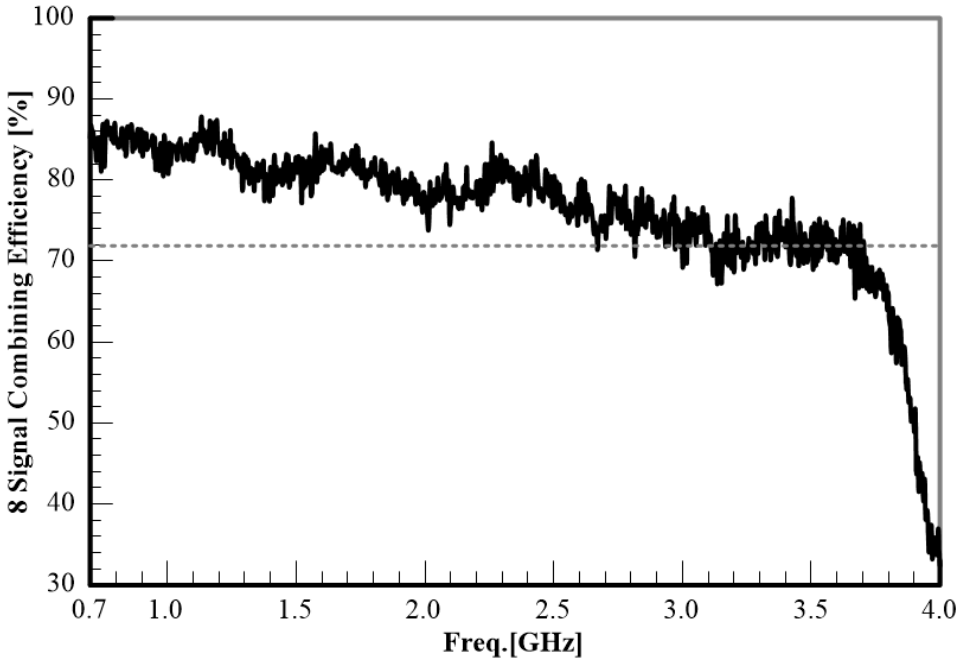


Fig. 51. Mini-Circuit combiner efficiency extracted from averaged power transmitted from Ports 2 – 9 to Port one.

Examining the results in Table VIII and Table IX I extracted measurements standards to gauge success.

A. 3.75:1 Minimum Bandwidth
B. -15dB Minimum Port one Return Loss
C. -20dB Minimum Ports 2 – 9 Return Loss
D. 1.5:1 VSWR Port one
E. 1.4:1 VSWR Ports 2 – 9
F. 1.5dB ± 0.8dB Insertion Loss
G. ± 0.5dB Amplitude Imbalance
H. ± 4^{o} Phase Unbalance
I. Transmission Phase Standard Deviation ≤ ± 1.5^{o}
J. -16dB Minimum Isolation

IV.C. UWB Combiner Design Strategy

Redesigning the Rev1 Wilkinson combiner and eradicate the flaws discovered in chapter III required examining many aspects of combiner development analytically, simulations, and measurements. First, set design and operation standards based upon measurements from an industry-fabricated combiner and antenna integration requirements. Next, I observed signal combining efficiency for multiport WPC designs. Third, examined interconnecting transmission lines traversing multiple laminate layers and how interconnects influence the WPC. Fourth, I studied how parallel stripline coupling influences isolation and impedance. Fifth, chose thin film resistors for multilayer designs. Finally, I provide in-depth UWB combiner design discussion and conduct experiments on a fabricated eight port WPC.

Currently, research focuses on making the Wilkinson combiner smaller, providing band selectivity, and wideband coverage. Kawai, an Electrical Engineering Ph. D. student from the University of Hyogo in Japan, observed "*In recent years, wireless communication systems such as a mobile phone, WLAN, ETC, and etc. are remarkably developed. Accordingly, various microwave devices are demanded with high performance requiring small size, low cost, wide band, and multi-band. Therefore, many researchers made an effort to miniaturize Wilkinson power dividers*" [67].

TCA antennas need a signal combiner covering its entire receiving spectrum. The combiner's structure fits comfortably and concealable behind the TCA preventing radiation pattern interference. The combiner condenses the antenna from a two-dimensional array to one-dimensional array. A small profile combiner simplifies

mounting thus enhancing attraction for applications involving weight and size restrictions.

Signal combining and splitting designs pursue uniform phase, uniform amplitude, and circuit losses across all ports and paths for the desired frequency range. Two approaches for RF signal combining involve tree (parallel) and chain (series) structures. Transmission hardware selection determines size, weight, and loss with microstrip possessing the smallest size and lightest weight and waveguides possessing the least loss. For further reading on other power combining approaches, I recommend reading *Millimeter-Wave Power-Combining Techniques* by Kai Chang [87].

Fig. 52 exhibits how parallel structures or corporate networks sum signals. Wilkinson combiners, rat race couplers, and coupled line directional couplers demonstrate bi-directional corporate network hardware. These circuits offer matched ports and good isolation. The total signals (S_k) combined through a corporate network calculated by a binary [88] equation, 2^N, with N representing a positive integer. Each stage contains 2^{N-M} adders with M representing a level's identifying positive integer ascending left to right from one to N. For example 32 input signals equates to 2^5 signals, $N = 5$. Summing 32 signals requires five combining levels, $M = N$, to output one signal (S_{OUT}). To split a signal, reverse the process described.

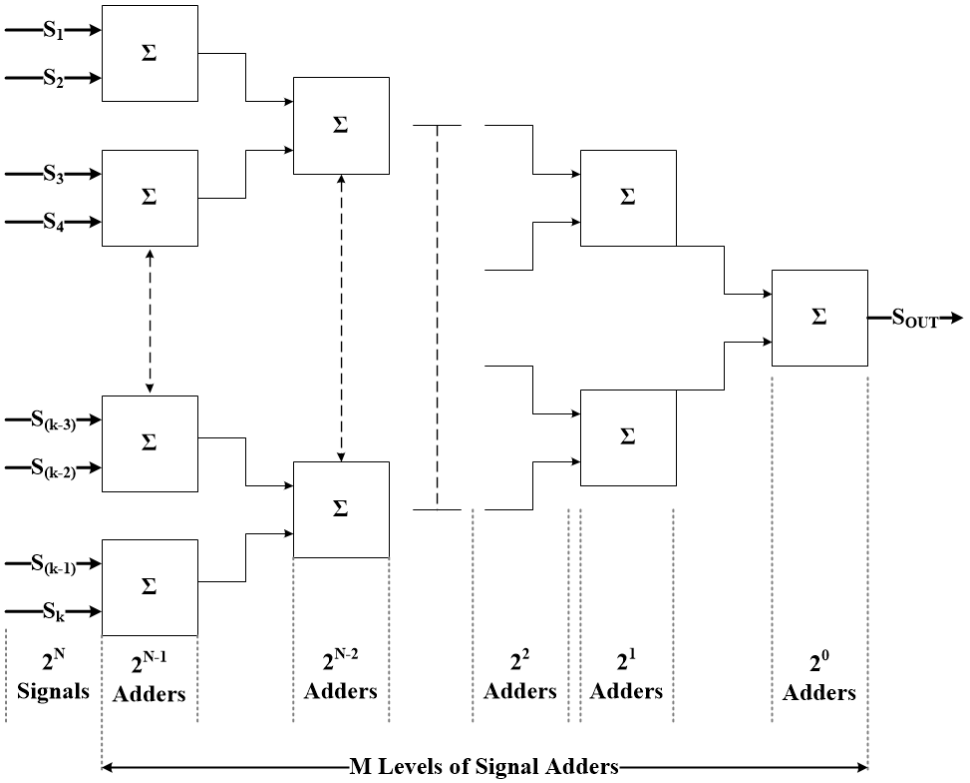


Fig. 52. A corporate network block diagram representing received signal summation.

IV.D. Signal Combining Efficiency

Bi-directional adder losses constrain combining efficiency. Losses depend upon frequency. Fig. 53 demonstrates loss impact on combining efficiency. The total loss for an ideal binary combiner determined from $L = \alpha^M$, where α represents loss per combining level and $M = log_2 N$, [89]. Eq. (10) defines signal efficiency with P_T (power transmitted), P_I (power in), L (circuit losses) or reflected power (P_R), and η_c (efficiency).

$$P_T = P_I - L$$
$$\eta_c = \frac{P_T}{P_I} \bullet 100\% \tag{10}$$
$$L = P_R$$

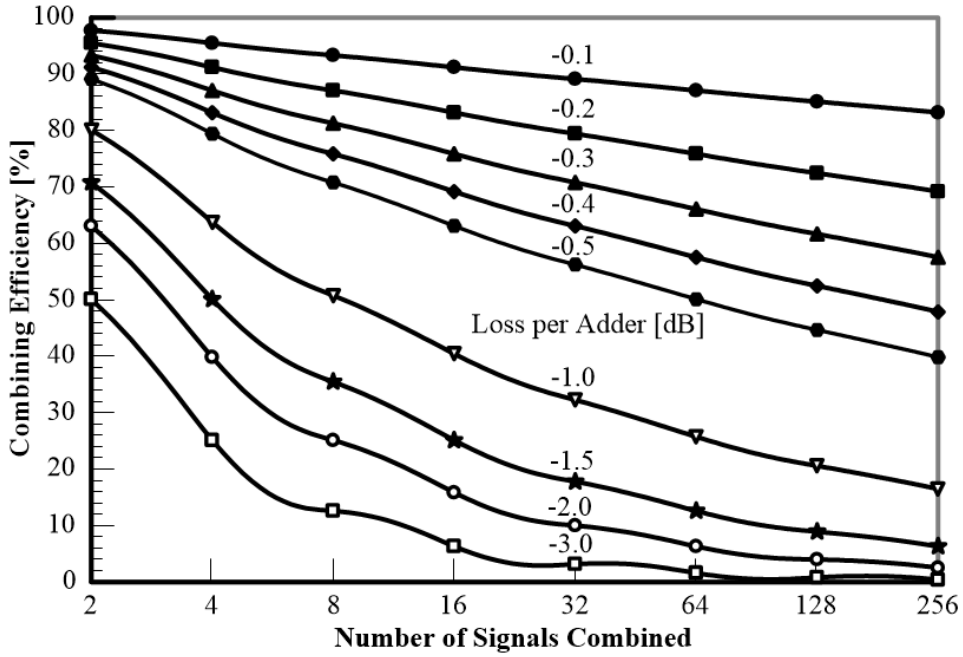


Fig. 53. Combining efficiency for corporate networks based on ideal adder losses.

IV.E. Interconnecting Multiple Layers

The selected method to achieve compactness, EMI, and EMC for phase array integration involved a stripline design. The new compact WPC design necessitates a multilayer assembly suitable for the allotted space. The stripline enclosure prevents external and internal electromagnetic interference. Fig. 54 shows the stripline components and TEM mode artistic rendering. The stripline TEM mode and a rectangular waveguide TM_{01} mode look similar [90]. Eq. (11) from [91] determines stripline impedance. The effective width (w_{eff}) becomes essential when considering parallel line coupling and separation distance.

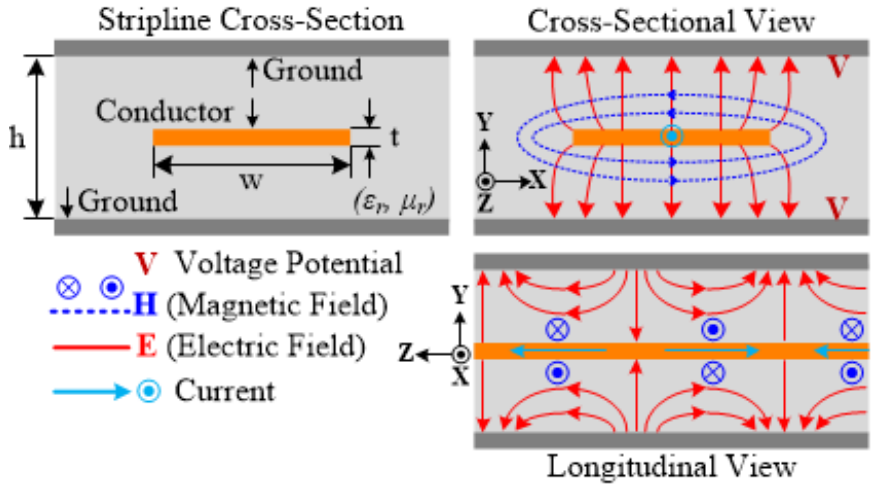


Fig. 54. Stripline cross-sectional view detailing electromagnetic fields and current.

$$Z_0 = \frac{30}{\sqrt{\varepsilon_r}} \ln\left\{1 + \frac{4}{\pi}\frac{h-t}{w_{eff}}\left[\frac{8}{\pi}\frac{h-t}{w_{eff}} + \sqrt{\left(\frac{8}{\pi}\frac{h-t}{w_{eff}}\right)^2 + 6.27}\right]\right\} \ [\Omega]$$

$$\frac{w_{eff}}{h-t} = \frac{w}{h-t} + \frac{\Delta w}{h-t}$$

$$\frac{\Delta w}{h-t} = \frac{x}{\pi(1-x)}\left\{1 - \frac{1}{2}\ln\left[\left(\frac{x}{2-x}\right)^2 + \left(\frac{0.0796x}{\frac{w}{h} + 1.1x}\right)^m\right]\right\} \tag{11}$$

$$m = \frac{2}{1 + \frac{2x}{3}(1-x)}$$

$$x = \frac{t}{h}$$

The measured frequency range designated to 700 MHz – 4.0 GHz. Therefore, copper retains a minimum 0.0984 mils (0.0025mm) skin depth. The selected laminate provides a

1.3mil (0.033mm) ½oz copper thickness. Therefore, the signal will not penetrate layers without assistance.

A multilayer assembly includes a transmission line interconnect methodology involving either coupling [66] or vias [74]. Coupling uses the electric field and vias the magnetic field. Coupling transmission lines from one layer to another dictates dielectric thickness. A thick dielectric alters the impedance between layers introducing higher attenuation. Decreasing dielectric thickness decreases stripline width maintaining impedance. A thin dielectric (≤ 20mil or 0.508mm) decreases the minimum feature size for my proposed design lower than the manufactured recommended 4mil (0.102mm). Stripline interlayer coupling transitions introduce additional design challenges. Introducing a via transition keeps the WPC dimensions higher than the minimum feature size and simplifies circuit design. One transmission via and one grounding via possess three design parameters:

- r_{via} – Via hole radius.
- r_{pad} – Via launching and landing pad radius.
- r_{port} – Via coupling port radius.
- s – Via separation measured center to center.
- $h_{\#}$ – Distance between transmission lines or ground planes.

The ground via's longer length compared to the transmission via maintains equal ground potential. Fig. 55 gives an exploded three-dimensional drawing distinguishing the different parts. Fig. 56 provides a top down perspective of the three main layers. Contingent on via location and length, layer two begins transmission interconnect and layer four terminates it.

The Fig. 55 grey column represents the void between via launching pad and the layer one initial hole requires filling. The filler contains dielectric slurry comprising of adhesive and powered dielectric material from the drilled hole. The dielectric slurry influences impedance slightly by introducing an inhomogeneous material. Assuming spherical particles housed in a cylinder, the Maxwell-Garnett mixing rule [119] assists in determining the slurry's effective dielectric constant.

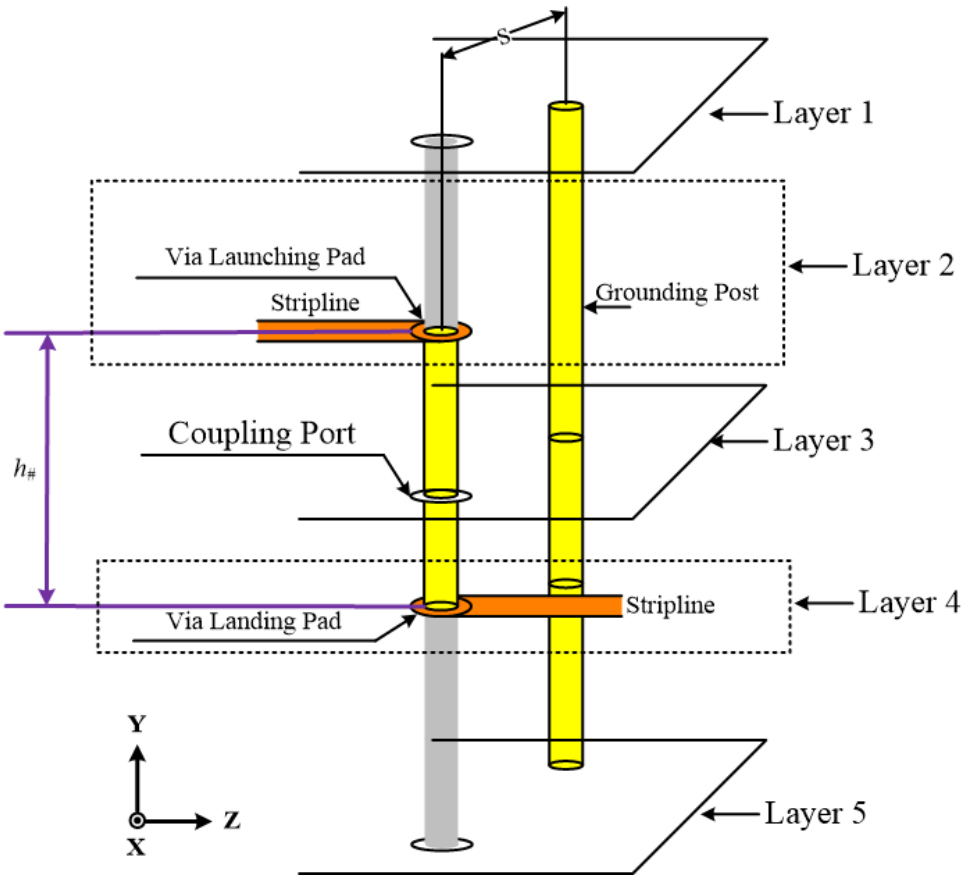


Fig. 55. Stripline via transition.

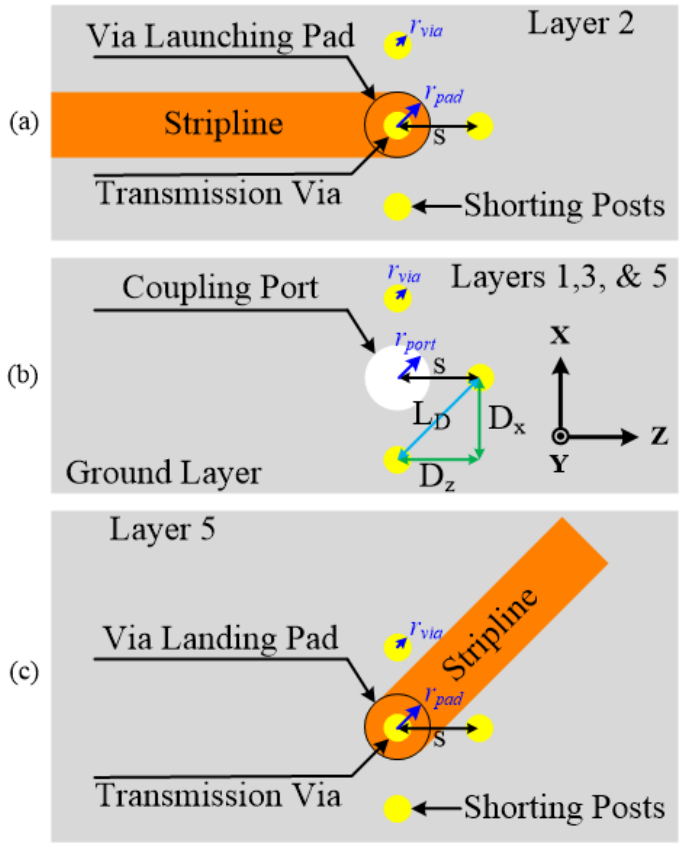


Fig. 56. Stripline-to-stripline via transition two-dimensional perspective with (a) layer 2 launching pad, (b) ground layer and coupling port, and (c) layer 5 landing pad.

Two types of currents flow on a stripline: differential and common-mode. Differential-mode currents possess the same magnitude but possess opposite phases. Common-mode currents or antenna currents [92 and 93] possess equal magnitude and phase. Common-mode currents radiate. Paul [94] introduces displacement current to Kirchhoff's current law to model common-mode current and account for RF emissions from stripline and microstrip circuits.

Fig. 57 demonstrates stripline differential current flowing equal and opposite directions along the ground plane provides a balanced signal. The stripline needs equal

potential maintained on the ground planes or else a parallel plate waveguide propagating mode develops. Implementing a via "picket fence" helps maintain equal potential between ground planes.

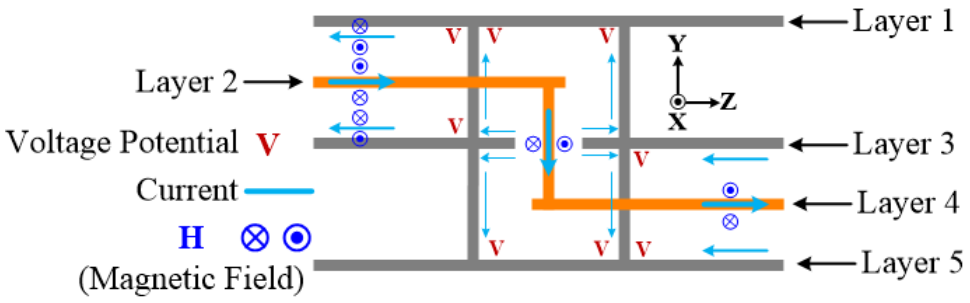


Fig. 57. Stripline transition displaying current flow.

The stripline forward and return currents both maintain magnetic fields. Magnetic fields cancel with equal and opposite currents. The transmission via creates an unbalanced current transitioning between layers while return current travels elsewhere. When no ground vias exist alongside the transmission via, the return current will take the closest layer interconnect including the transmission via and RF connector. The return current reflections on the transmission line deteriorate the impedance.

To assist understanding how the stripline and via fields impact impedance, Fig. 58 endeavors to artistically render field interaction within the physical structure. Fig. 58 (a) shows the stripline doesn't end abruptly, but terminates with a rounded end. Fig. 58 (a) demonstrates the rounded end forces the magnetic field to change directions by 90°, but not without introducing fringing fields. The fringing fields make the stripline appear electrically longer and wider changing the stripline inductance and impedance thus

manipulating phase. Fringing fields influence electromagnetic interference (EMI) by radiating. The extra dielectric layer covering the stripline discontinuity assists by reducing radiation loss and insertion loss [95]. A ground via near the stripline termination captures the radiated field and grounds it. The grounding vias assist by maintaining equal potential between ground planes.

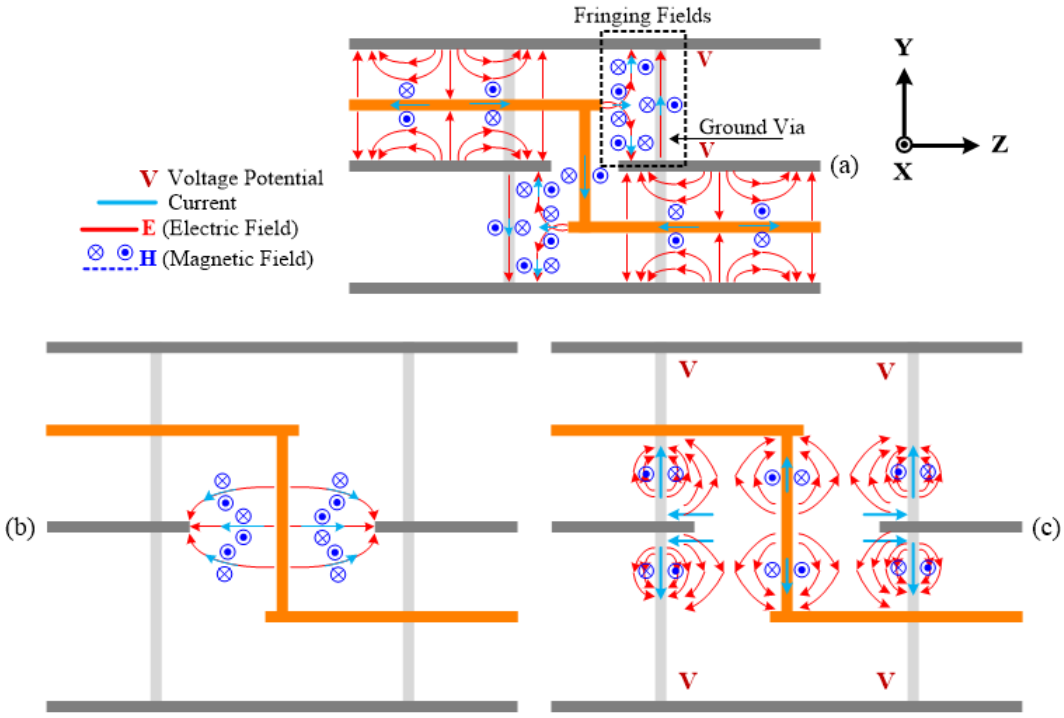


Fig. 58. Stripline via transition (a) stripline TEM, (b) fringing fields from transmission via, to (c) coaxial TEM mode.

The TEM wave perceives the transmission via likens to a coaxial line. Fig. 58 (c) shows the fields. Grounding vias assist by forming a virtual coax line interconnecting the striplines. The **H**-field divergence results produce a scalar field describing a sink belonging to the transmission via. The **H**-field curl produces a –y directed current along

the transmission via. The current supports a magnetic field and agrees when taking the **E**-field curl produces a negative **H**-field. The **E-**field components now propagate along y and x directions. Together, these fields form a TEM coaxial field structure.

The transmission via and grounding via characterize an unbalanced feed line. The unbalanced feed will produce unequal currents on the transmission via and grounding via. Therefore the currents do not cancel allowing more current on the through via. The unequal current on neighboring ground vias create an electric field similar to the electric field traveling on the transmission via per Faraday's Law. Faraday's Law states a conductor forms a voltage potential resulting from an external magnetic flux.

When the distance between two vertical grounding vias equals $\lambda_{eff}/2$ excites a resonate mode. The excited mode possesses electric and magnetic field phases opposite the stripline's fields. A specific frequency nulls the fields. The canceled fields produce a rapidly attenuated transmission signal creating a high Q and high order notch filter. By taking the proper design steps, the mode cancelation occurs outside the essential frequency spectrum. Eq. (12), modified from Eq. (1) in [120], provides a theoretical calculation to determine the resonating mode frequency (f_m).

$$\begin{aligned} \mathrm{L}_D &= \sqrt{D_y^2 + D_z^2} \\ f_m &\approx \frac{c_0}{2\sqrt{\varepsilon_r} L_D} \end{aligned} \tag{12}$$

IV.E.1. Via Impedance Implications

The transmission via length, pad size, coupling port, spacing s, and the number of grounding vias influence impedance. Fig. 59 shows a circuit level break down on how the via impacts impedance, modified from [96]. The launching pad, transmission via, and landing pad equate to a transmission line containing RLCG components. The R and G components represent losses. Parallel mutual coupling (C_{pv} and C_{pp}) and mutual inductance (L_{cp} and L_{pp}) form a potential tank circuit. These tank circuits appear between the launching pad and via, landing pad and via, and lastly between launching pad and landing pad. The LC tank circuit resonance (f_r) creates a notch filter and Eq. (13) calculates f_r. C_{pad} symbolizes pad coupling to ground. C_{via} symbolizes via coupling to ground. C_{pv} and C_{pp} exist due to C_{pad} and C_{via} coupling.

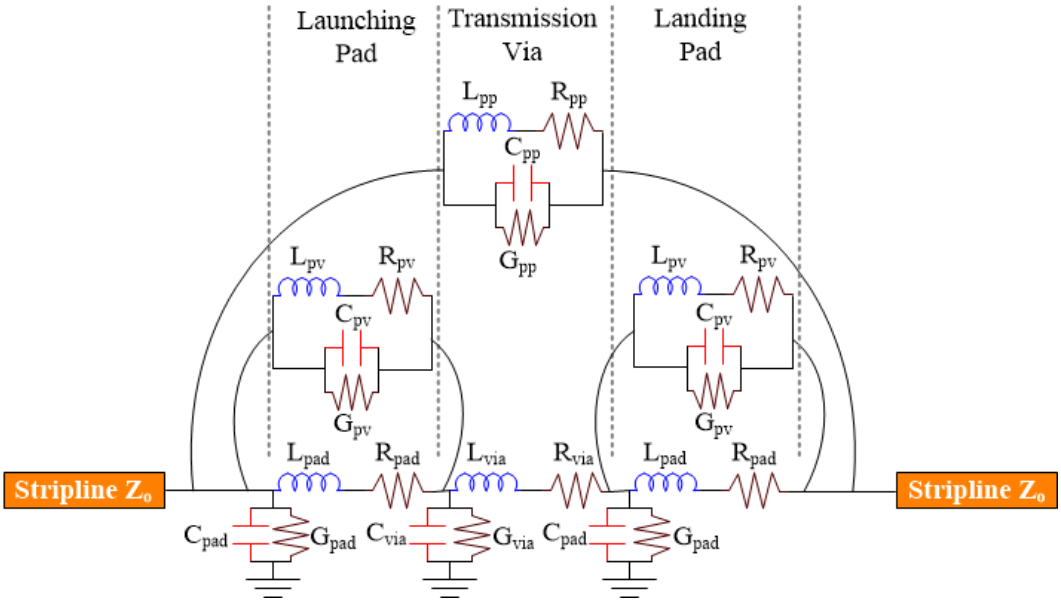


Fig. 59. Transmission via equivalent circuit model.

$$f_r = \frac{1}{2\pi\sqrt{L_{pv,pp}C_{pv,pp}}} \tag{13}$$

My electromagnetic simulation experiments concluded the following observations and conclusions agree with [96]. Increasing r_{pad} enlarges the pad surface area increasing charge between conductors thus increasing capacitance. Increasing r_{via} increases the cross-sectional area current travels. Increasing r_{via} reduces launching pad magnetic field storage (inductance) and dissipation (loss).

Reducing the dielectric thickness increases capacitance. Capacitance increases when ground plane separation decreases. Fig. 58 (b) displays the coupling port's capacitive and inductive values change when fields couple the opening. Decreasing r_{port} increases capacitance and decreases inductance. Fig. 60 show the coupling port resembles a small coax cable segment. Eq. (14) from [40] describes the inductance and capacitance for a coax transmission line. In Eq. (14), replace s with r_{port}.

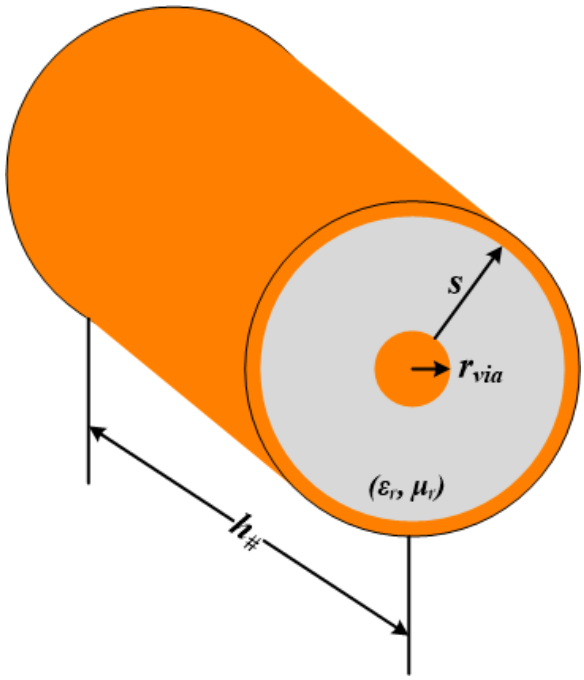


Fig. 60. Pictorial representation of a coaxial cable.

$$L_{coax} = \frac{\mu_o \mu_r}{2\pi} h \ln \frac{s}{r_{via}}$$
$$C_{coax} = \frac{2\pi\varepsilon_o \varepsilon_r}{\ln\left(\frac{s}{r_{via}}\right)} \tag{14}$$
$$Z_o = \sqrt{\frac{L}{C}} \ [\Omega]$$

The transmission and ground vias together resemble an inductor owing to the magnetic field. Decreasing s and keeping r_{via} constant decreases inductance and increases capacitance. If s becomes too small, then the magnetic field surrounding the via becomes perturbed thus shorting the transmission path. Decreasing r_{via} and keeping s constant increases inductance and decreases capacitance. If s becomes too large, then a

propagating mode develops affecting the transmission signal. Decreasing via $h_{\#}$ also reduces inductance and increases capacitance.

If not enough grounding vias or shorts surround the transmission via, then return current unbalance negatively influences impedance. Reference [97] provided some guidance on visualizing the inductance from the transmission via and associated grounding vias. Fig. 61 shows four different via configurations. Eq. (15 - 18) from [97] describe the stripline interconnect inductance for one, two, four, and six ground vias surrounding the transmission via. Eq. (19) expresses when the ground via number approaches infinity, the interconnect inductance equals coax inductance. Each ground via spaced s from the transmission via.

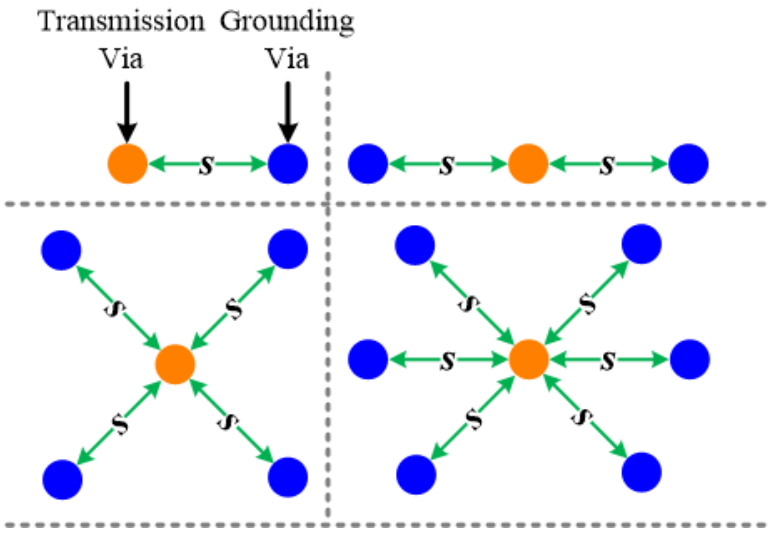


Fig. 61. Different stripline via configurations showing one, two, four, and six grounding vias.

$$L_1 = \frac{\mu}{2\pi} 2h \left(\ln \frac{s}{r_{via}} \right) \tag{15}$$

$$L_2 = \frac{\mu}{2\pi} h \left(\frac{3}{2} \ln \frac{s}{r_{via}} + \frac{1}{2} \ln(2) \right) \tag{16}$$

$$L_4 = \frac{\mu}{2\pi} h \left(\frac{5}{4} \ln \frac{s}{r_{via}} + \frac{1}{4} \ln(2) \right) \tag{17}$$

$$L_6 = \frac{\mu}{2\pi} h \left(\frac{7}{6} \ln \frac{s}{r_{via}} + \frac{1}{6} \ln(2) \right) \tag{18}$$

$$L_\infty = \lim_{x \to \infty} = \frac{\mu}{2\pi} h \left(\frac{x+1}{x} \ln \frac{s}{r_{via}} + \frac{1}{x} \ln(2) \right) = \frac{\mu}{2\pi} h \left(\ln \frac{s}{r_{via}} \right) \tag{19}$$

Table XI lists the via properties provided by a fabrication house. These properties applied to Eq. (14) and Eq. (15 - 18) show numerically how the interconnect configurations influence inductance. I normalized the inductance in Table XI by $\frac{\mu}{2\pi} h$ for simplicity and removing frequency dependence. Increasing ground via numbers increases return current flow cross-sectional area and decreases interconnect inductance. Six ground vias comes close to forming a virtual coaxial connection between striplines.

TABLE XI
MANUFACTURING VIA PROPERTIES

Via Parameters		Interconnect Normalized Inductance	
TL	[mil]	Via Configuration	L
r_{via}	15	1 Gnd.	3.08
r_{pad}	23	2 Gnd.	2.66
r_{port}	27	4 Gnd.	2.10
s	70	6 Gnd.	1.91
		Coax ($x \to \infty$)	1.54

IV.E.2. Interconnect Testing

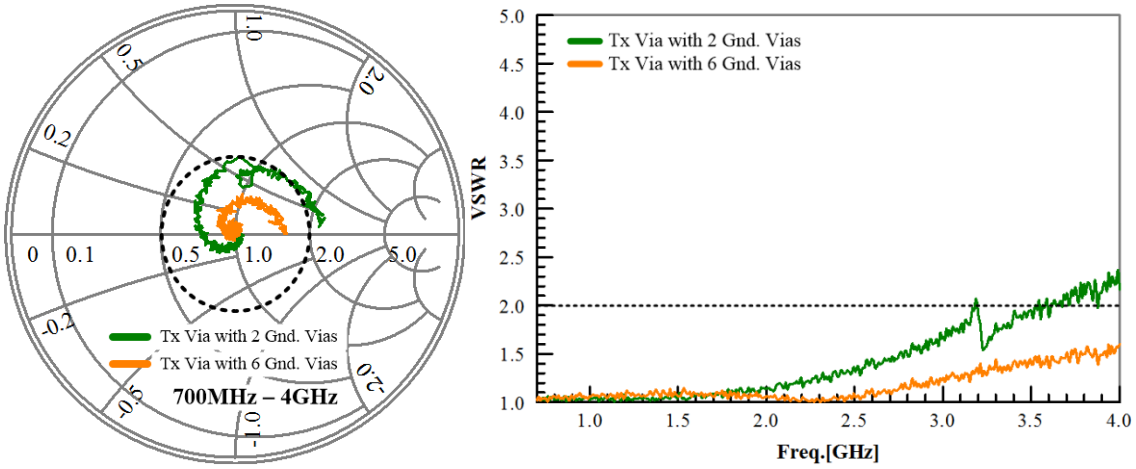
A fabricated testing kit[5] obtained a visual perspective on interconnect configuration and the via integration. The test circuit contains two different 50Ω stripline interconnect configurations, a standard 50Ω stripline, 50Ω stripline with via fence, 2:1 stripline combiner without a via fence, 2:1 stripline combiner with a via fence, and a 4:1 multilayer stripline combiner. Fig. 62 shows the fabricated test board.

Fig. 62. Fabricated via and stripline testing kit.

A Keysight FieldFox 9923A [81] tested and recorded the combiner measurements using custom designed phased matched cables from Times Microwave [82]. Fig. 63 (a) shows via impedance and agrees with Table XI. The six ground vias provides a better impedance match and lower inductance. Fig. 63 (b) shows a 1.1:1 VSWR between 0.7 and 2.5 GHz. The impedance match breaks down above 2.5 GHz. Improving the impedance match requires adjusting via spacing, coupling port radius, and via radius.

[5] The author would like to acknowledge the assistance provided by colleagues David C. and Jenn for designing the via test kit.

Fig. 63 (a and b) exhibit the two ground configuration introduces a small resonance at 3.2 GHz. The resonance represents an LC resonance occurring between via launching pad and landing pad. Fig. 59 shows where the resonance may develop. An LC resonance could occur between ground vias when return current seeks balance.



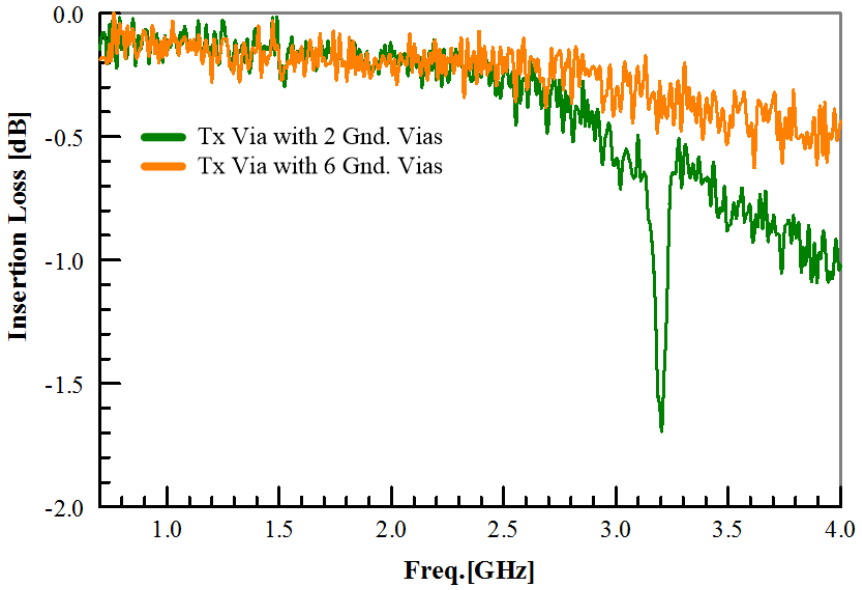
(a) (b)

Fig. 63. Stripline interconnect impedance for two and six ground vias.

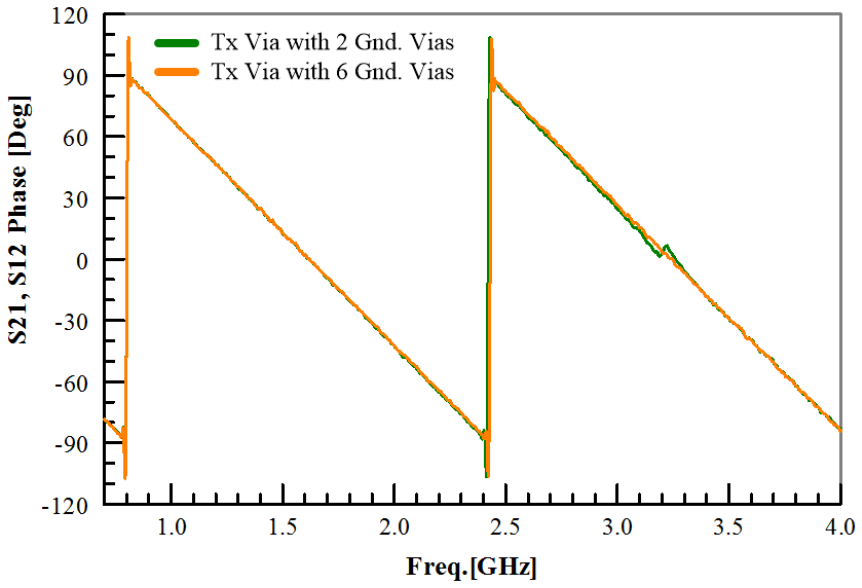
Fig. 64 (a) shows a 3.2 GHz transmission nadir. The two via configuration offers an average 0.055dB trace loss between 700 MHz and 2.5 GHz and 0.228dB between 2.5 GHz and 4.0 GHz. The six via configuration offers an average 0.057dB trace loss between 700 MHz and 2.5 GHz and 0.117dB between 2.5 GHz and 4.0 GHz. Fig. 64 (b) shows the phase for two vias lags the six vias by 1°. The increased inductance increased the stripline effective length just enough to offset the phase. The 3.2 GHz interconnect resonance produces a 5° phase shift. The raw phase data indicates a small transmission length difference between tests strips indicating a slight manufacturing error. The 2.0

GHz mark indicates the two via design impedance degrading begins and the degrading impedance contributes to the phase lag.

Reducing the dielectric height would contribute additional capacitance tightening the impedance match and reducing the path loss between striplines. However, decreasing the height would decrease the minimum feature size causing manufacturing difficulties. Increasing r_{pad} and increasing r_{via} a small amount would increase capacitance and decrease inductance improving the interconnect impedance and reducing insertion loss.



(a)



(b)

Fig. 64. Interconnect configuration impact on transmission (a) and phase (b).

IV.E.3. Stripline Picket Fence

A noise problem originates from the stripline supporting a propagating wave unless sufficient ground vias suppress the wave. A stripline and a multilayer stripline excite an artifact called the parallel-plate waveguide (PPW) mode [98 – 100]. A PPW mode becomes excited when the voltage potential between the ground planes becomes unbalanced. The PPW creates excess noise. The PPW mode adds multiple reflections negatively influencing impedance and increasing insertion loss. Minimizing the PPW mode's negative influence requires a via "picket fence" bounding the stripline to balance the voltage potential between ground planes. Vias paralleling the stripline suppress the PPW mode. Ideally, the grounding vias stop the PPW mode, however, the fields propagate between grounding vias. Other grounding vias located throughout the circuit assist negating any propagating mode and assist maintaining voltage balance.

A resonant mode's existence depends upon the distance between grounding vias [101]. Fig. 65 visualizes the construction. Three stripline widths (w) separate the grounding vias. The distance between the inner radius and outer radius for a coax cable equals three times the inner radius. Thus, setting the cross-sectional via spacing to $3w$ permits the stripline to function similarly to a coax cable. The stripline supports a propagating waveguide mode when $f_o = \frac{c_o}{2(3w)}\sqrt{\varepsilon_r}$. Vias placed too close to the stripline perturb the TEM mode shorting the transmission line. A distance s separates adjacent vias approximately $\frac{\lambda_{eff}}{8}$ with λ_{eff} determined by the highest operating frequency.

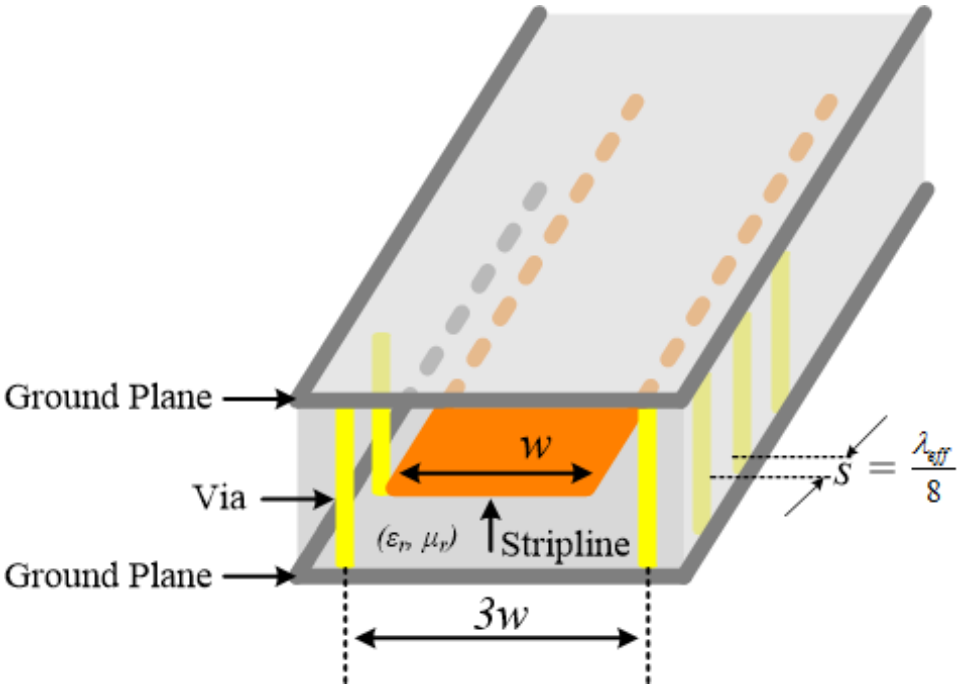
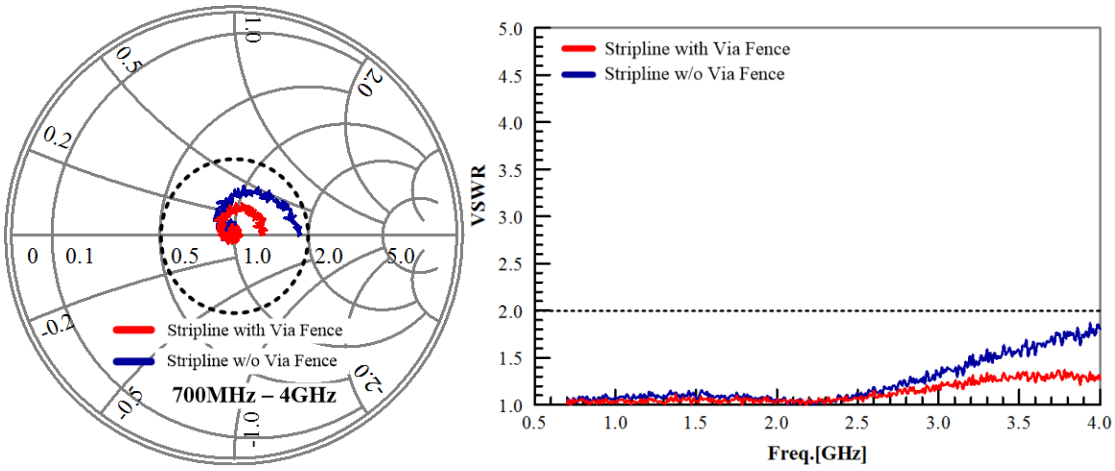


Fig. 65. Stripline "picket fence" construction.

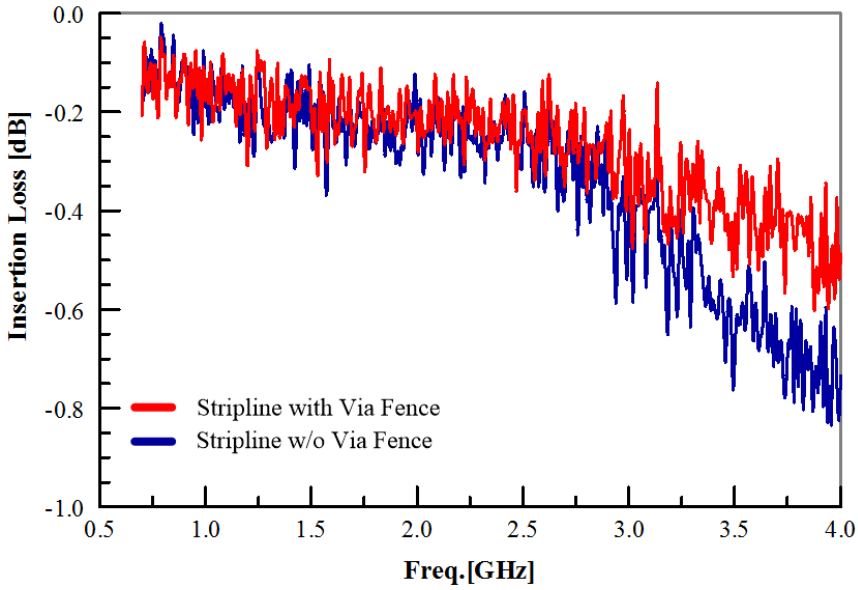
Fig. 62 shows the sample stripline circuits fabricated to show performance impact when not implementing a via "picket fence." The ground vias separate lengthwise $3w$ = 160mils (4.06mm) and widthwise by s = 240mils (6.1mm). Providing a λ_{eff} = 320mils (8.13mm) for 21.3 GHz and λ_{eff} = 1920mils (48.77mm) for 3.55 GHz respectively. Fig. 66 (a and b) shows adding the via fence increases the cross-sectional area available for return current to flow thus reducing the inductance. The impedance match begins to change above 2.5 GHz. Additional losses come from the stripline to microstrip transition and SMP connector.



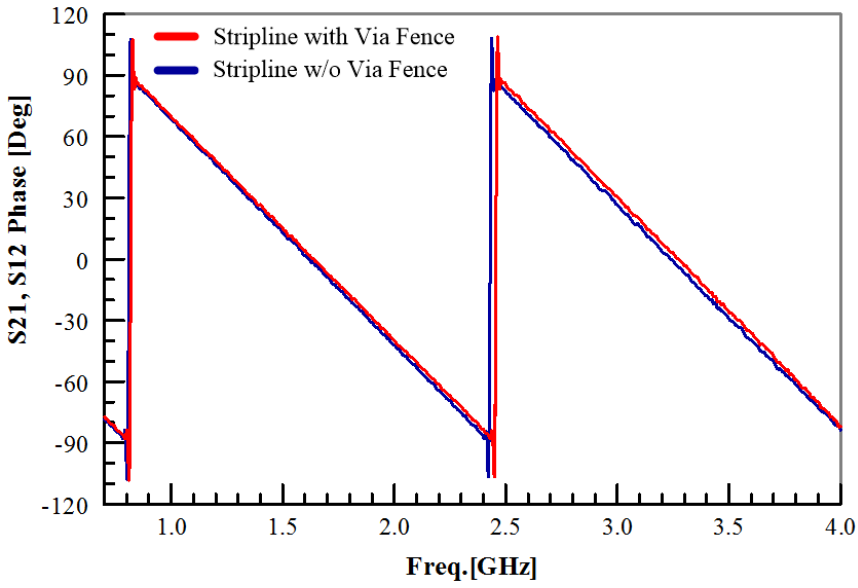
(a) (b)

Fig. 66. Stripline impedance (a) and VSWR (b) for with and without a via fence.

Fig. 67 (a) shows the via less stripline averages -0.2dB trace loss between 700 MHz and 2.5 GHz and -0.5dB between 2.5 GHz and 4.0 GHz. The shorting fence configuration averages -0.19dB trace loss between 700 MHz and 2.5 GHz and -0.36dB between 2.5 GHz and 4.0 GHz. Fig. 67 (b) shows the no picket fence phase lags the picket fence by 1^{o} and a 5^{o} maximum. The increased inductance increased the stripline effective length just enough to offset the phase. The raw phase data indicates a small transmission length difference between tests strips indicating a slight manufacturing error.



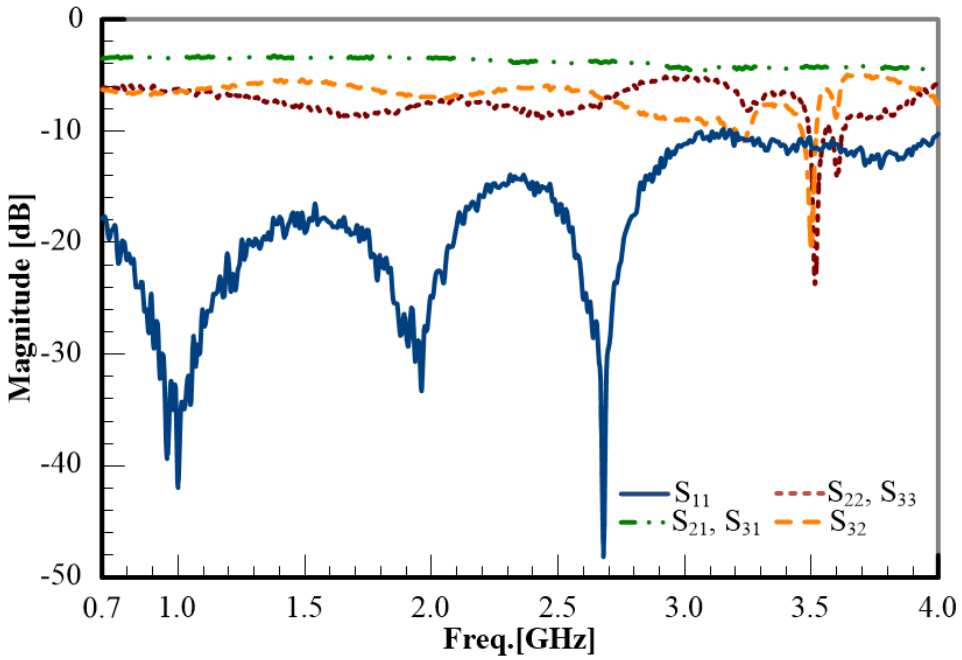
(a)



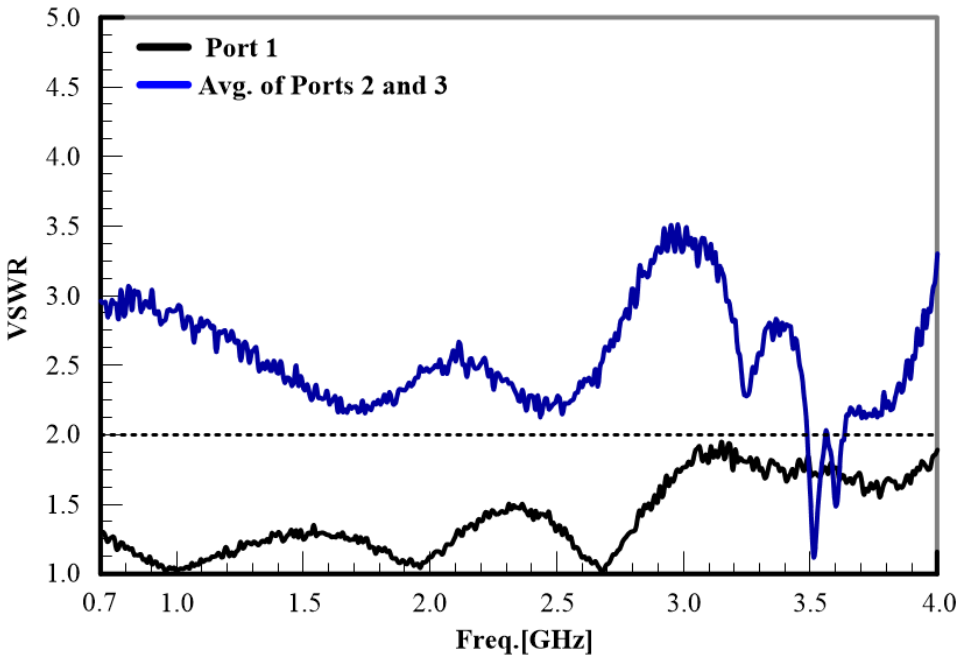
(b)

Fig. 67. Stripline insertion loss (a) and phase (b) for with and without a via fence.

Fig. 62 shows sample 2:1 multilayer Wilkinson combiner built without a supporting via fence. Fig. 68 (a) presents the return loss, insertion loss, and isolation results. Port one provides a minimum -14dB return loss (S_{11}) over 0.7 – 2.5 GHz and Ports two and three possess a minimum -6dB return loss (S_{22}, S_{33}) over 0.7 – 2.5 GHz. The insertion loss remained stable and averaged -4dB over 0.7 – 2.5 GHz. Ports two and three possess poor port isolation over 0.7 – 2.5 GHz with a -5dB minimum isolation. Port one provides a good impedance match, however, Ports two and three possess a 3:1 or worse match. Fig. 68 (b) and Fig. 69 present impedance information, first the VSWR then the Smith charts. Port one shows a 1.5:1 VSWR between 700 MHz and 2.5 GHz. Ports two and three show a mean VSWR of 2.7:1 between 700 MHz and 2.5 GHz. The Smith charts show a decent 50Ω impedance match for Port one and mediocre impedance match for Ports two and three over 0.7 – 4.0 GHz.

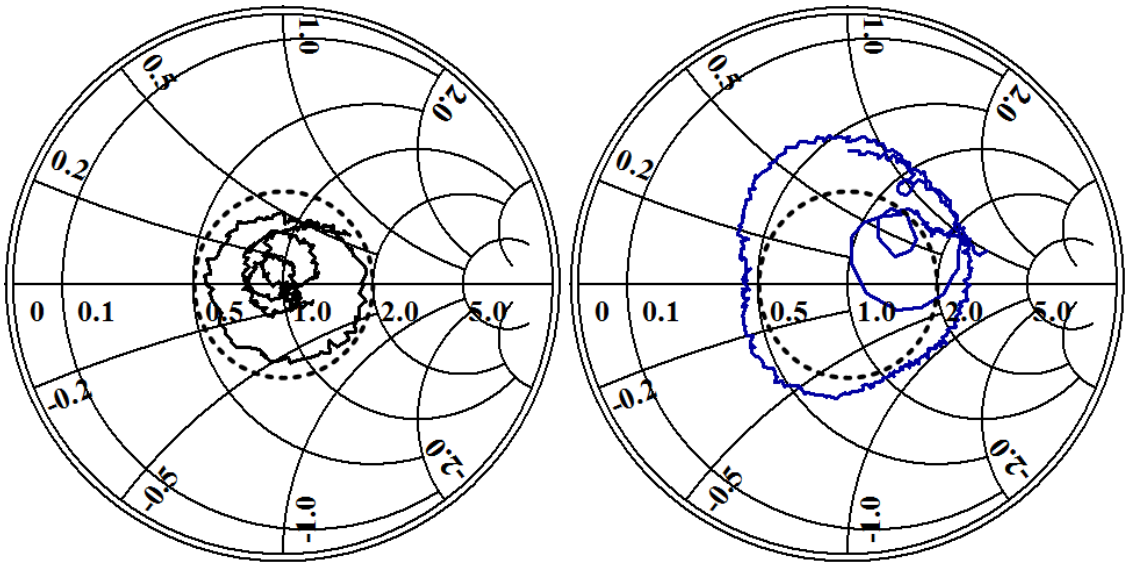


(a)



(b)

Fig. 68. 2:1 Wilkinson combiner design without a via fence measured results for (a) insertion loss, return loss, and isolation and (b) VSWR.

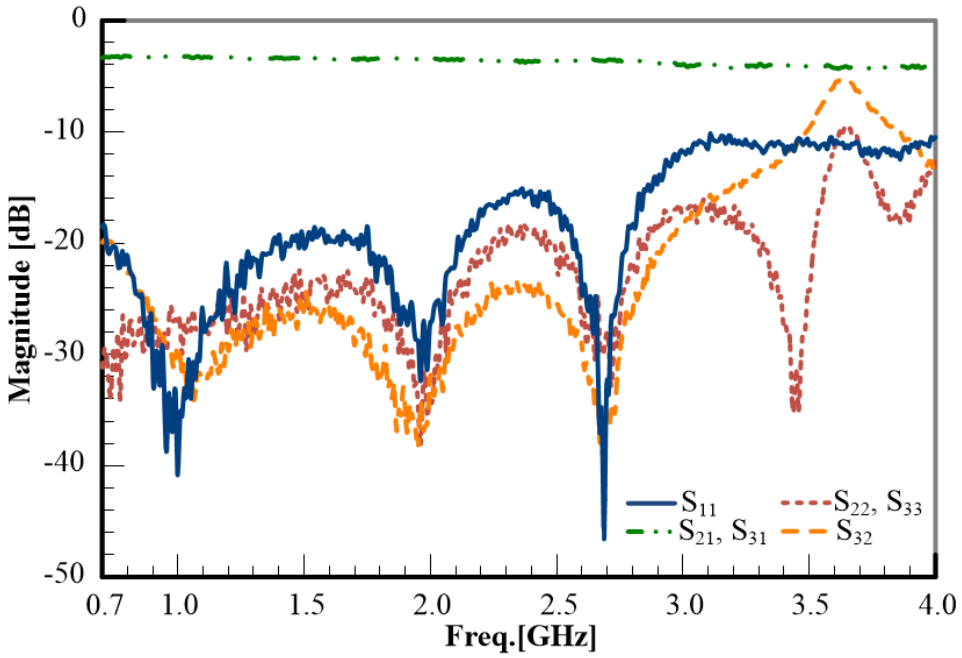


(a) (b)

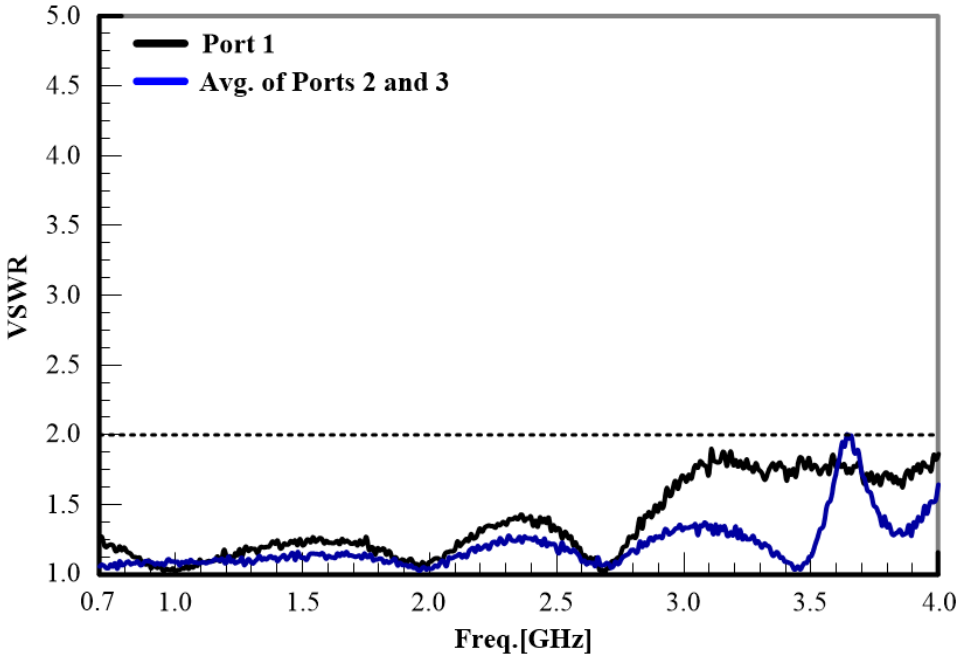
Fig. 69. 2:1 WPC without via fence measured impedance from 700 MHz to 4.0 GHz with the dashed circle marking VSWR = 2: (a) Port one and (b) Ports two and three.

Fig. 62 shows sample 2:1 multilayer Wilkinson combiner built with a supporting via fence. Fig. 70 (a) shows the return loss, insertion loss, and isolation results. Port one possess a minimum -16dB return loss (S_{11}) over 0.7 – 2.5 GHz and Ports two and three possess a minimum -20dB return loss (S_{22}, S_{33}) over 0.7 – 2.5 GHz. The -3.5dB insertion loss remained constant over 0.7 – 2.5 GHz. Ports two and three possess good port isolation over 0.7 – 2.5 GHz with a -24dB minimum isolation.

Fig. 70 (b) and Fig. 71 presents the impedance information, first the VSWR then the Smith charts. Port one shows a 1.3:1 VSWR between 700 MHz and 2.5 GHz. Ports two and three show a mean VSWR of 1.4:1 between 700 MHz and 2.5 GHz. The Smith charts show a good 50Ω impedance match for Port one and better impedance match for Ports two and three over 0.7 – 4.0 GHz.

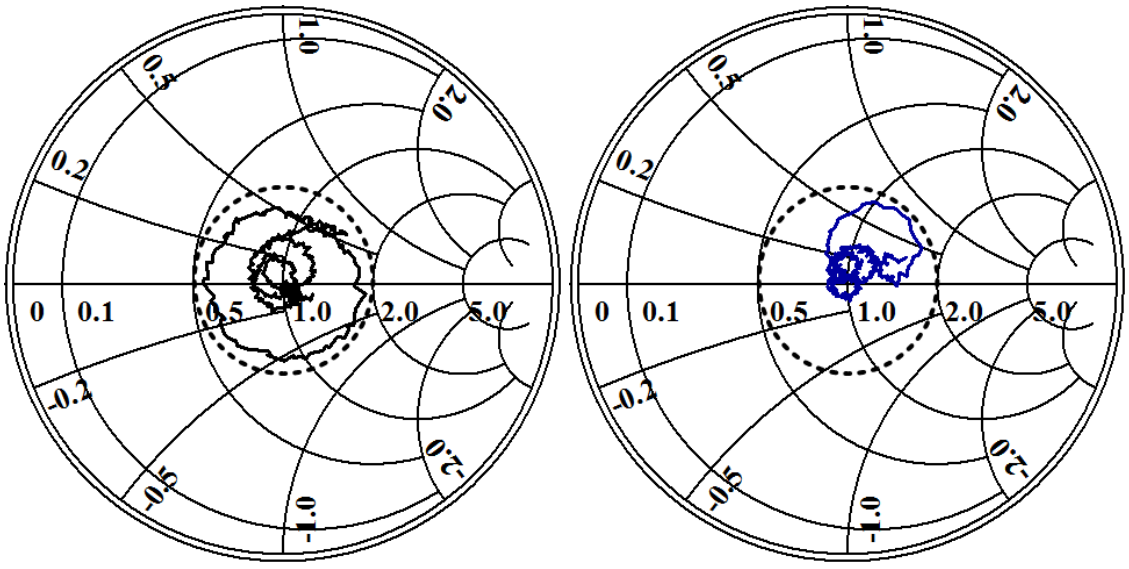


(a)



(b)

Fig. 70. 2:1 Wilkinson combiner design with a via fence measured results for (a) insertion loss, return loss, and isolation and (b) VSWR.

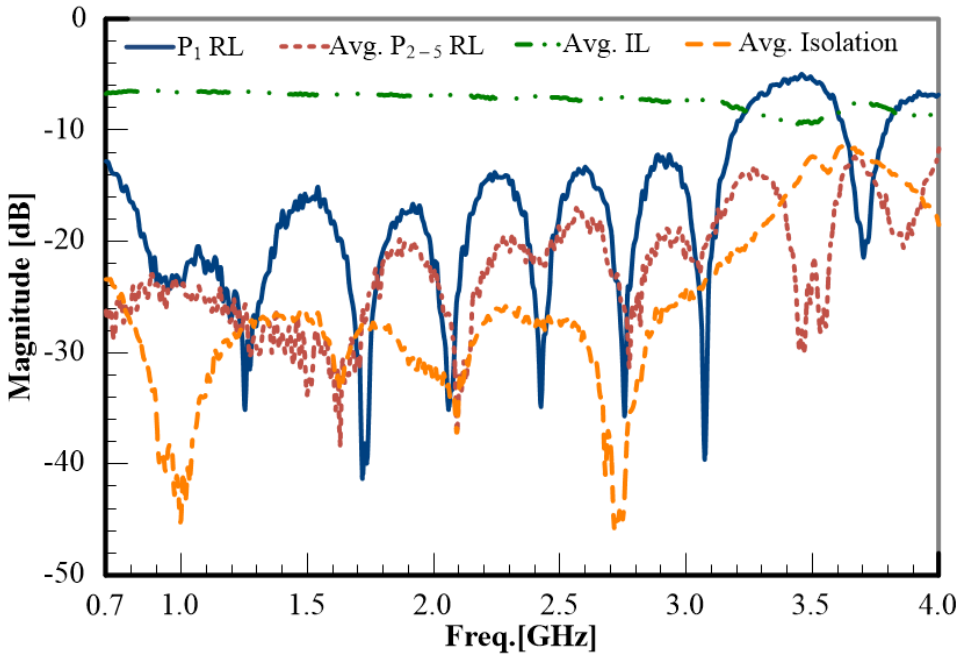


(a) (b)

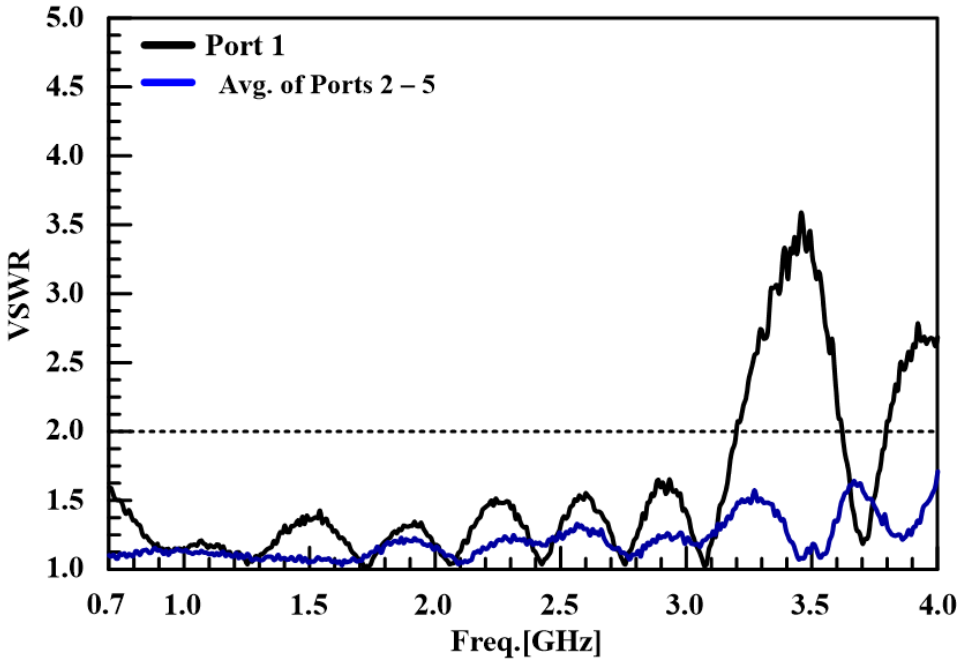
Fig. 71. 2:1 WPC with via fence measured impedance from 700 MHz to 4.0 GHz with the dashed circle marking VSWR = 2: (a) Port one and (b) Ports two and three.

A 4:1 multilayer WPC shown in Fig. 62 combines the via picket fence and via interconnects properly handling current. Fig. 72 (a) shows the return loss, insertion loss, and isolation results. Port one possess a minimum -16dB return loss (S_{11}) over 0.7 – 2.5 GHz and Ports 2 – 5 possess a minimum -20dB return loss (S_{22}, S_{33}) over 0.7 – 2.5 GHz. The -3.5dB insertion loss remained constant over 0.7 – 2.5 GHz. Ports 2 – 5 possess good port isolation over 0.7 – 2.5 GHz with a -24dB minimum isolation.

Fig. 72 (b) and Fig. 73 presents the impedance information, first the VSWR then the Smith charts. Port one shows a 1.5:1 VSWR between 700 MHz and 2.5 GHz. Ports 2 – 5 show a mean VSWR of 1.3:1 between 700 MHz and 2.5 GHz. The Smith charts show a respectable 50Ω impedance match for Port one and better impedance match for Ports 2 – 5 over 0.7 – 4.0 GHz.

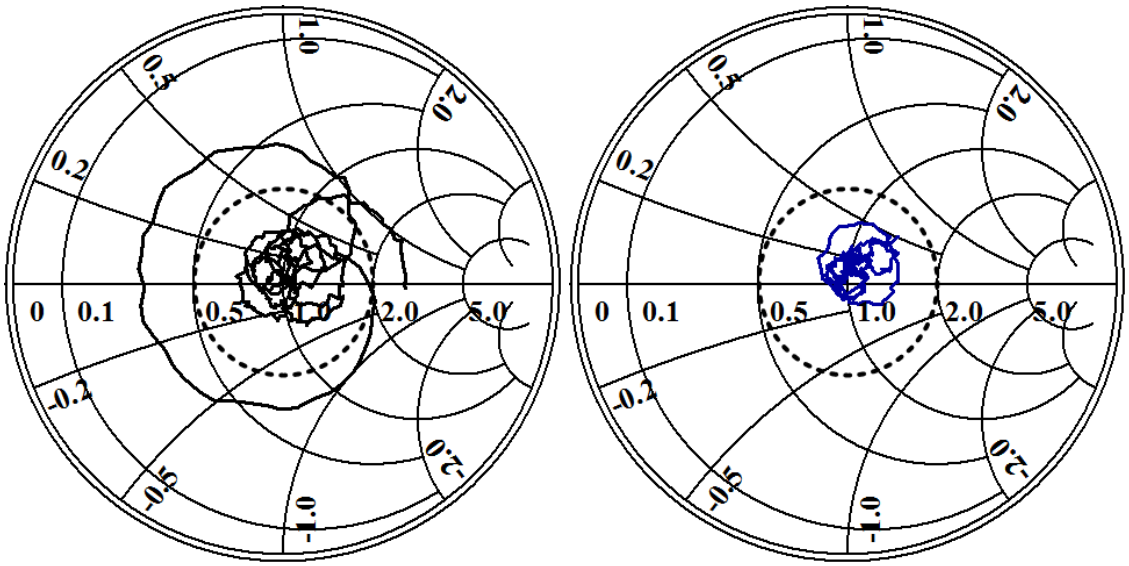


(a)



(b)

Fig. 72. 4:1 WPC with via fence and interconnects measured results for (a) insertion loss, return loss, and isolation and (b) VSWR.



(a) (b)

Fig. 73. 4:1 WPC with via fence and interconnects measured impedance from 700 MHz to 4.0 GHz with the dashed circle marking VSWR = 2: (a) Port one and (b) Ports 2 – 5.

These experiment results show substantial operating improvement when a stripline via fence and proper multilayer interconnects complement each other in a WPC.

IV.F. Revision 2 (Rev2) Design

I designed the four stage and three level combiner using the Tschebyscheff design process developed by Cohn [53]. The design used a 1.5 GHz center frequency. My colleagues, Jenn and David C., assisted with the simulations, layout, and optimization to develop the second design. David C. provided the final positions for all vias. Fig. 74 shows the four stage design. Table XII lists the design parameters. Fig. 75 shows the three level stripline CAD design.

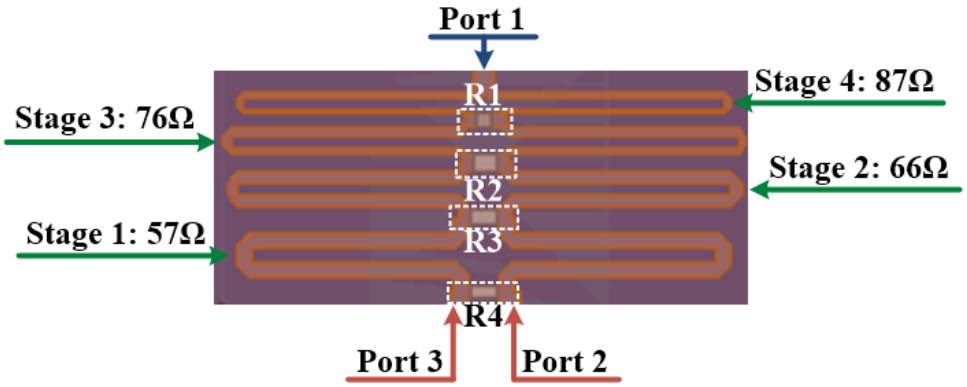


Fig. 74. Rev2 four stage Wilkinson combiner.

TABLE XII
REV2 COMBINER STRIPLINE PARAMETERS

TL	Z [Ω]	W [mil]	R [Ω]
Stage 4	87	10.3	R1 = 250
Stage 3	76	14.9	R2 = 200
Stage 2	66	19.6	R3 = 125
Stage 1	57	28.4	R4 = 100
TL Connector	50	36.4	

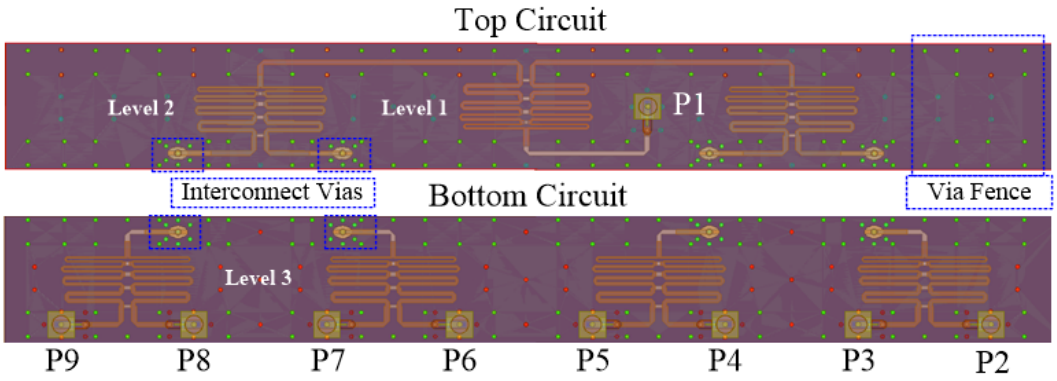


Fig. 75. Rev2 four stage and three level stripline Wilkinson combiner.

Fig. 76 shows the CAD representation displaying internal circuitry and dimensions. The design possesses a 0.125 inch (3.175mm) fabrication thickness (***h***), an 8 inch (203.2mm) length (***L***), and 0.98 inch (24.89mm) width (***W***). The eight-inch length

accounts for the TCA column length. The 0.98 inch width factors a small spacing between attached combiners to allow installation and comfortable seating.

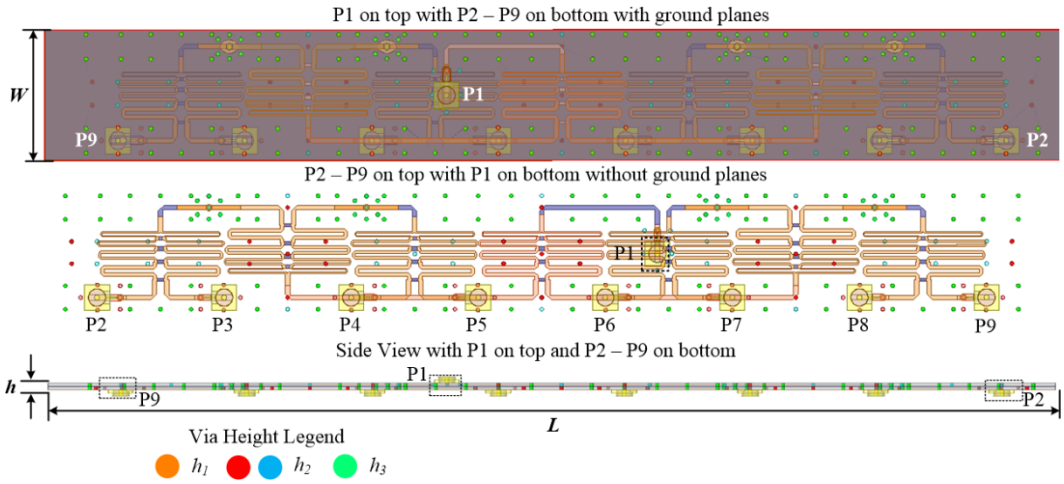


Fig. 76. Rev2 CAD design.

Table XIII lists the via design parameters recommended by the manufacturer. The Rev2 design went through extensive scrutiny. Simulations checked every transmission line, discontinuity, transition, via, and bend separately to check impedance and transmission. Modifying transmission line chamfering, width, and length also assisted to improve impedance and transmission. Simulations omitted for brevity.

TABLE XIII
VIA PARAMETERS

TL	[mil]
r_{via}	15
r_{pad}	23
r_{port}	27
s	70
h_1	30
h_2	60
h_3	120

Resolving Rev1 complications and fulfilling application needs dictated examining numerous laminates, i.e., Rogers duroid® 5880, 5870, 5980LZ, 3000, and 6000 series. The Rogers RO3003^{TM} [80], a ceramic-filled PTFE composite laminate, offers dielectric and mechanical consistency and stability. The RO3003™ datasheet describes dielectric temperature stability when temperature fluctuates between -58^{o}F – 302^{o}F (-50^{o}C – 150^{o}C). The dielectric constant varies ± 0.025 across frequency (1.0 – 10 GHz). The RO3003^{TM} possesses a 3.0 permittivity ($\boldsymbol{\varepsilon_r}$), tan$\delta$ = 0.001, 30mil (0.75mm) thickness, and 0.67mils (0.017mm) metal thickness. A multilayer adhesive bond the four sheets together forming the combiner. The Rev2 manufacturer did not disclose which adhesive however, Rogers does suggest several in [102]. Fig. 77 displays the fabricated design.

Nghiem et al. [99, 100, and 103] investigated multilayer bonding adhesive minimizes leaky propagating parallel plate modes introduced by air gaps between layers. An adhesive dielectric constant equaling or surpassing the laminate's dielectric constant assists to suppress the propagating parallel plate mode hence reducing crosstalk.

Resistor test pads, marked by the dashed red lines, allow verifying the embedded resistors' correct the values. The resistor value text etched into the Rogers RO3003™ performs the chemical etching smallest feature test. The test corners checks for over or under etching. Each port contains a soldered female SMP connector. Some dashed blue boxes highlight via drill holes to connect different layers together. Electroplated aluminum coats the external copper layers to prevent corrosion. Electroplated aluminum connects the top and bottom ground layers on all four sides. The combiner weighs 1.5oz (42.5g).

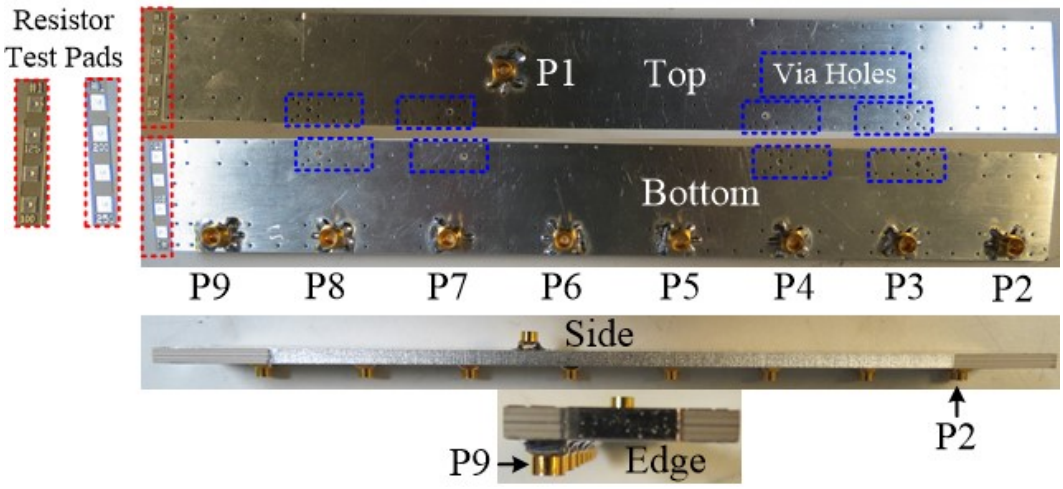


Fig. 77. Rev2 fabricated model.

Selecting the RO3003™ proved a wise decision for handling environmental extremes. While attending a conference in 2015, I spoke with an attendee regarding the design pictured in Fig. 77. Her research group attempted a multilayer circuit design using duriod® 5880, however the MIL-STD-810 environmental tests broke down the layer bonds leading to circuit disintegration. Rogers specifically designed the RO3000® series to handle multilayer circuits unlike the duroid® 5880. Her group's effort to test multilayer designs provides a limitation to the RF engineer's multipurpose duroid® 5880.

Striplines designs possess several important factors contributing to signal loss: characteristic impedance variation, inhomogeneous dielectric constant, dielectric losses, conductor resistance, stripline metallic coatings and glue, solder and flux parasitics or LC resonances, metal thickness, circuit layout, over/under photoetching, and drill errors.

Using the equations and tables provided by Cohn [53] originate from Tschebyscheff filter design and introduces ripple. Fig. 78 republishes FIG. 3-26 [104] restoring visual clarity and introducing additional annotations and alterations associating the argued UWB Wilkinson design. Fig. 78 displays VSWR ripple vs. bandwidth covering two, three, and four stage Wilkinson combiners.

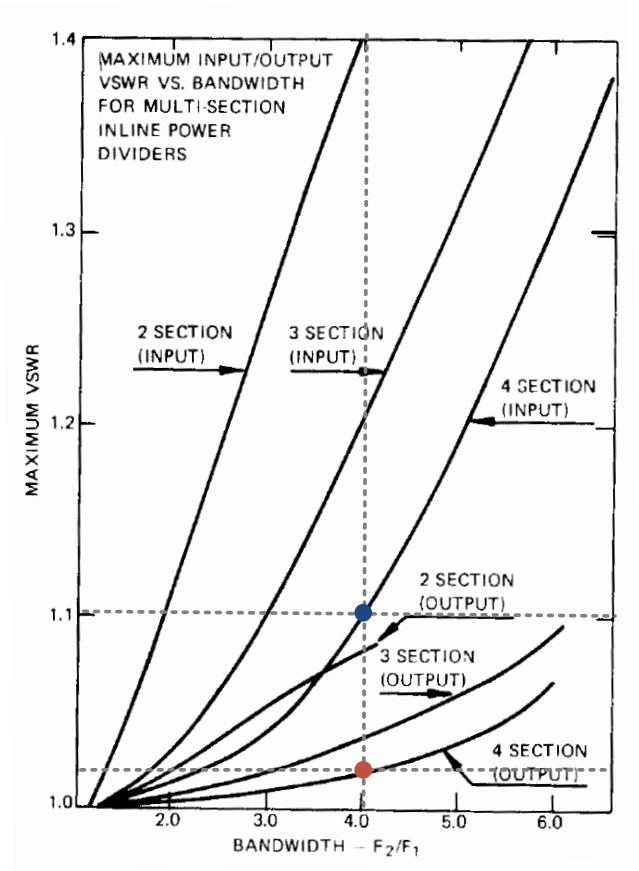


Fig. 78. “Maximum Input-Output VSWR vs. Bandwidth for a Multisection In-Line Power Divider.” Reprinted and lightly edited with permission from [104]. Order Detail ID: 71045382 Stripline circuit design by HOWE, HARLAN Reproduced with permission of ARTECH HOUSE INC in the format Thesis/Dissertation via Copyright Clearance Center.

The operating frequencies cover 800 MHz to 3.0 GHz providing a 3.75:1 bandwidth. Cohn's broadband design [53] recommends four stages to achieve a 4:1 bandwidth. A four stage design, pictured in Fig. 78, offers a 1.1:1 maximum VSWR input ripple and 1.03:1 maximum output ripple. Based on the design parameters discussed in Table I in [53], initial four stage design transmission line and resistor values came from [53, 105, and 106]. Eq. (20) determined a 1.2 fractional bandwidth with $f_1 = 3.2\ GHz$ and $f_2 = 0.8\ GHz$. Young's transformer tables [105] include the desired 4:1 impedance ratio ($R = 4$). Table XIII in [105] state $Z_1 = 1.18876$ and $Z_2 = 1.67300$ for $R = 4$ and $W = 1.2$ with $Z_3 = R / Z_2$ and $Z_4 = R / Z_1$. Table III in [105] provides a maximum 1.2:1 VSWR ripple.

$$\text{Fractional Bandwidth } (W) = \frac{2\left(\frac{f_2}{f_1} - 1\right)}{\left(\frac{f_2}{f_1} + 1\right)} \tag{20}$$

Young's tables don't provide the resistor values R_1, R_2, R_3, and R_4. Cohn provides an iterative computational method to optimize impedance and resistor values for multi-stage Wilkinson combiners detail in [53]. Cohn provides 50Ω normalized iteration results for a four stage combiner: $Z_1 = 1.1157$, $Z_2 = 1.2957$, $Z_3 = 1.5435$, $Z_4 = 1.7926$, $R_1 = 9.6432$, $R_2 = 5.8326$, $R_3 = 3.4524$, and $R_4 = 2.0633$. Howe [107] took Cohn's computational method and extracted a design guidance figure. Fig. 79 republishes FIG. 3-28 [107] restoring visual clarity and introducing additional annotations and alterations associating the argued UWB Wilkinson design. Fig. 79 pictorially describes the four

stage design values for bandwidths between two and nine. Fig. 79 includes markings for the transmission line impedances and resistors.

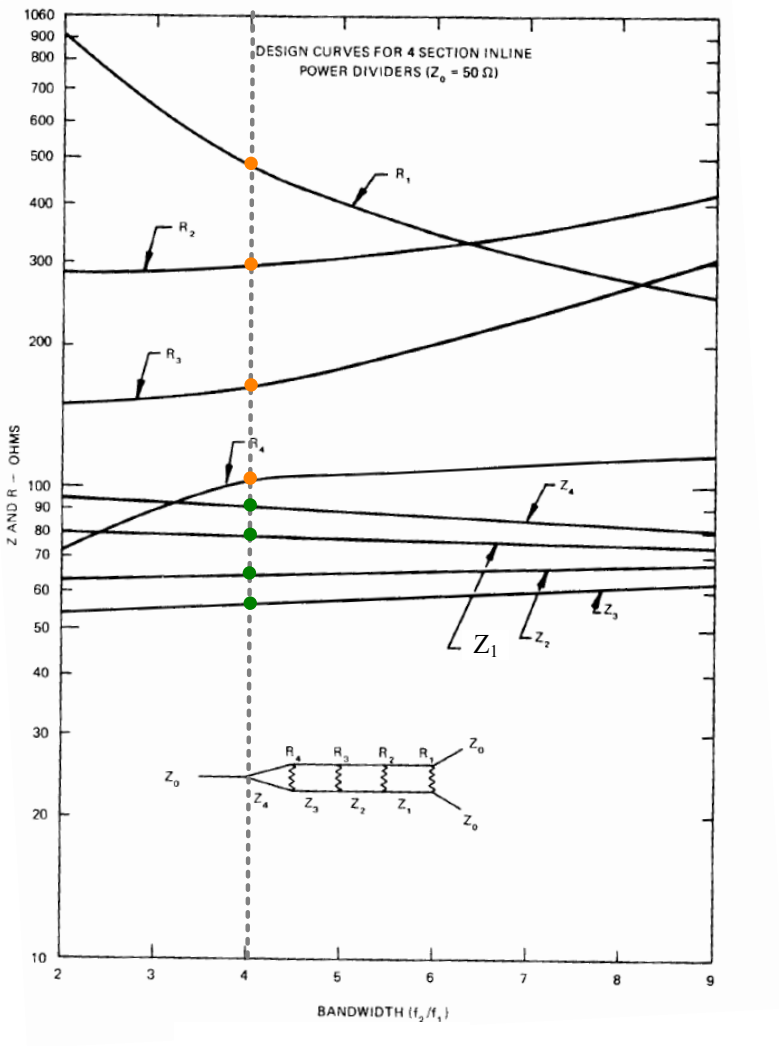


Fig. 79. “Design curves for four-section in-line equal-split power dividers.” Reprinted and lightly edited with permission from [107]. Order Detail ID: 71045382 Stripline circuit design by HOWE, HARLAN Reproduced with permission of ARTECH HOUSE INC in the format Thesis/Dissertation via Copyright Clearance Center.

IV.F.1. Stripline Coupling and Isolation

The compact Wilkinson combiner means less room for transmission line separation. The four-stage design introduces a higher inductance than a single stage design introduced by the additional transmission line length. Improving the impedance match meant adding capacitance. Placing the stage transmission line sections close to each other, the stripline coupling adds capacitance, but also increases crosstalk. Fig. 80 describes the coupled transmission line structure with odd and even mode fields. Odd mode currents and magnetic fields possess equal and opposite magnitudes and phase while even mode currents and magnetic fields possess the same magnitudes and phase. Because the even mode current travel the same direction causing a magnitude reduction thus the arrow becomes smaller than odd mode current arrow. The even mode introduces the coupling and crosstalk.

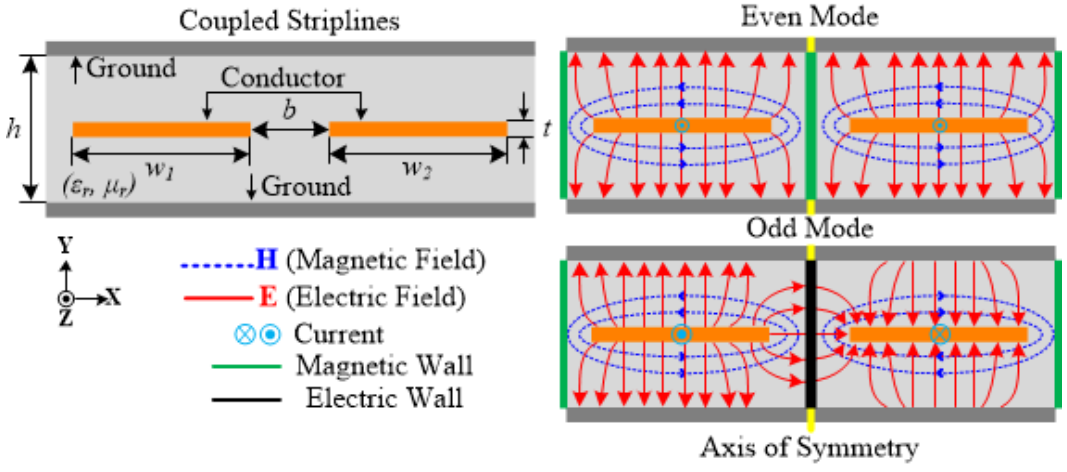


Fig. 80. Coupled stripline structure and modal fields. .

Fig. 81 shows the fringing capacitance and gap capacitance for coupled striplines. Assuming the strip conductors possess the same width and positioned the same between ground planes, then $C_{11} = C_{22}$. Fig. 80 displays the even mode electric field maintains symmetry around the yellow centerline and no current traverses striplines. A magnetic wall produces an open circuit and an electric wall forms a short circuit. Eq. (21) shows even mode capacitance, Eq. (22) odd mode, and Eq. (23) gap capacitance.

$$C_e = C_{11,e} \tag{21}$$

$$C_o = C_{11,o} + 2C_{12} \tag{22}$$

$$C_{12} = \frac{2C_{12}2C_{12}}{2C_{12}+2C_{12}} = \frac{4}{4}C_{12} \tag{23}$$

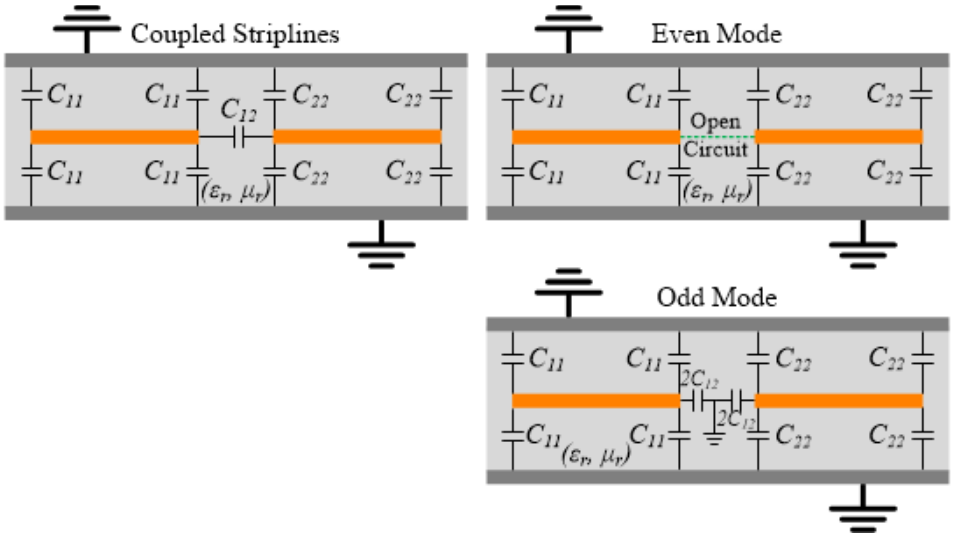


Fig. 81. Coupled stripline capacitance representation by mode.

Cohn [108 and 109] used conformal mapping to determine the capacitance and impedance for coupled striplines. Completing the conformal mapping requires making some assumptions. The assumption both parallel striplines possess the same width simplifies mathematics to maintain structural symmetry. A second assumption states the dielectric bonding layer does not change the dielectric constant therefore expect solution error. Due to the mathematical complexity for a four-stage Wilkinson combiner, discussion covers the solution for a single stage design only. Cohn [108] introduces Eq. (24) and fringing capacitance Eq. (25) for a stripline.

$$\varepsilon = 0.0885\varepsilon_r \tag{24}$$

$$C_f'\left(\frac{t}{h}\right) = \frac{\varepsilon}{\pi}\left\{\frac{2}{1-t/h}\ln\left(\frac{1}{1-t/h}+1\right)-\left(\frac{1}{1-t/h}-1\right)\ln\left(\frac{1}{(1-t/h)^2}-1\right)\right\} \tag{25}$$

Eq. (26) and Eq. (27) denote the even and odd mode impedance solutions from conformal mapping two coupled striplines assuming zero line thickness. Eq. (28) and (29) state the complete elliptical integrals of the first kind. Eq. (30) and Eq. (31) denote the elliptical integral moduli. Eq. (32) shows mutual dependence between moduli. Figure 7.29 in [110] shows the design curves for parallel striplines when changing width, height, and separation. Figure 7.29 in [110] visualizes the frequency independent even and odd mode impedance showing a wishbone formation varies coupled stripline separation (*b*) for a basic Wilkinson combiner containing coupled striplines. Z_{oo} and Z_{oe} converge to 73.23Ω, the stripline's intrinsic impedance.

$$Z_{oe} = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{K\left(k_e^{'}\right)}{K\left(k_e\right)} \tag{26}$$

$$Z_{oo} = \frac{30\pi}{\sqrt{\varepsilon_r}} \frac{K\left(k_o^{'}\right)}{K\left(k_o\right)} \tag{27}$$

$$K\left(k_{e,o}\right) \int_0^{\pi/2} \frac{d\vartheta}{\sqrt{1 - k_{e,o}^2 \sin^2 \vartheta}} \tag{28}$$

$$K\left(k_{e,o}^{'}\right) \int_0^{\pi/2} \frac{d\vartheta}{\sqrt{1 - \left(k_{e,o}^{'}\right)^2 \sin^2 \vartheta}} \tag{29}$$

$$k_e = \tanh\left(\frac{\pi}{2}\frac{w}{h}\right) \tanh\left(\frac{\pi}{2}\frac{w+b}{h}\right) \tag{30}$$

$$k_o = \tanh\left(\frac{\pi}{2}\frac{w}{h}\right) \coth\left(\frac{\pi}{2}\frac{w+b}{h}\right) \tag{31}$$

$$k_{e,o}^{'} = \sqrt{1 - k_{e,o}^2} \tag{32}$$

Cohn manipulated Eq. (25) to produce Eq. (33), (34), and (35) for coupled lines with zero line thickness. Fig. 82 republishes Cohn's plot with permission [109] and displays the normalized fringing capacitance determined by Eq. (33) and Eq. (34). Both even and odd mode capacitances converge to Eq. (35) with zero conductor thickness.

$$C_{fe}^{'}\left(0, \frac{b}{h}\right) = \varepsilon \left[\frac{b}{h} - \frac{2}{\pi} \ln\left(\cosh\frac{\pi b}{2h}\right)\right] \tag{33}$$

$$C'_{fo}\left(0,\frac{b}{h}\right)=\varepsilon\left[\frac{b}{h}-\frac{2}{\pi}\ln\left(\sinh\frac{\pi b}{2h}\right)\right] \tag{34}$$

$$\frac{C'_f(0)}{\varepsilon}=\frac{2}{\pi}\ln 2=0.4407 \tag{35}$$

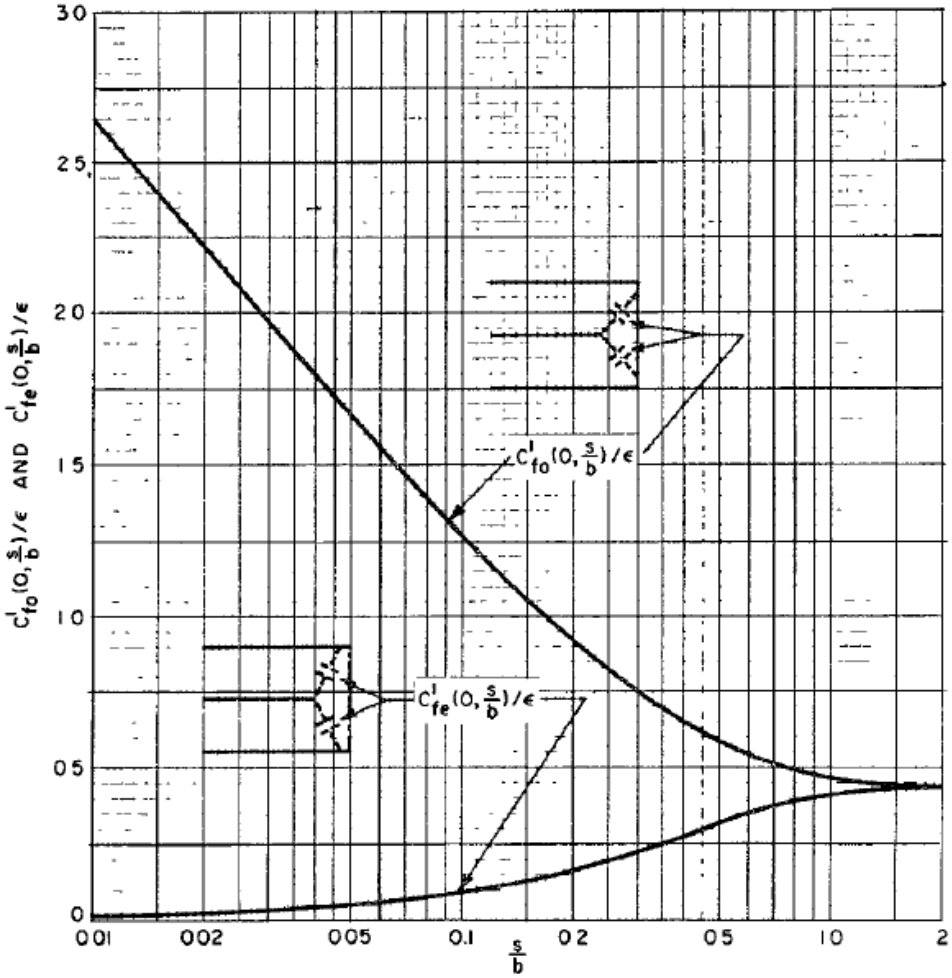


Fig. 82. Fringing capacitances for coupled striplines with zero thickness. Reprinted with permission from [109]. Order Detail ID: 71045384 IRE transactions on microwave theory and techniques by IRE PROFESSIONAL GROUP ON MICROWAVE THEORY AND TEC Reproduced with permission of PROFESSIONAL GROUP ON MICROWAVE THEORY AND TECHNIQ in the format Republish in a thesis/dissertation via Copyright Clearance Center.

Cohn then introduced conductor thickness using Eq. (25), Eq. (33), and Eq. (34). Eq. (36) and Eq. (37) tie Eq. (38) and Eq. (39) back to Fig. 81. Fig. 83 shows conductor thickness influences fringing capacitance minimally. Four different metal thickness chosen come from the Rogers RO3000™ datasheet [80] and common metal thickness found on Rogers' material. Eq. (37) shows the odd mode capacitance retains independence of conductor thickness and the even mode capacitance fluctuates fractionally with Eq. (35). Comparing Fig. 82 and Fig. 83 shows conductor thickness minimally influences capacitance and a zero thickness conductor assumed for calculating fringing capacitance provides adequate results.

$$C'_{fe}\left(\frac{t}{h},\frac{b}{h}\right)=C'_{f}\left(\frac{t}{h}\right)\frac{C'_{fe}\left(0,\frac{b}{h}\right)}{C'_{f}\left(0\right)} \tag{36}$$

$$C'_{fo}\left(\frac{t}{h},\frac{b}{h}\right)=C'_{fo}\left(0,\frac{b}{h}\right) \tag{37}$$

$$C_{11,e}=C_{22,e}=C'_{fe}\left(\frac{t}{h},\frac{b}{h}\right) \tag{38}$$

$$C_{11,o}=C_{22,o}=C'_{fo}\left(\frac{t}{h},\frac{b}{h}\right) \tag{39}$$

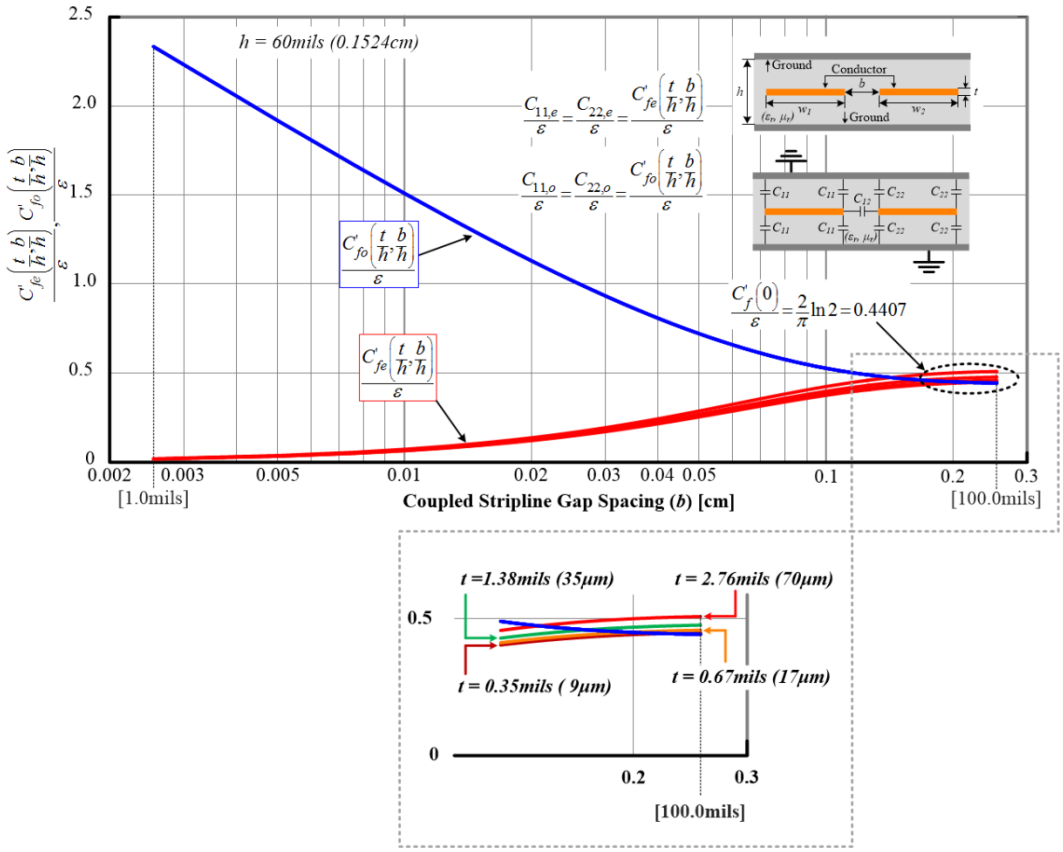


Fig. 83. Coupled striplines normalized fringing capacitance for specific thickness.

A parallel plate capacitor, Eq. (40), approximates the gap capacitance. Fig. 84 normalizes Eq. (40) and varies conductor thickness. Decreasing stripline separation increases gap capacitance between striplines therefore increasing crosstalk.

$$\frac{C_{12}}{l} = \varepsilon \frac{t}{b} \left[\text{F/Unit Length}\right] \tag{40}$$

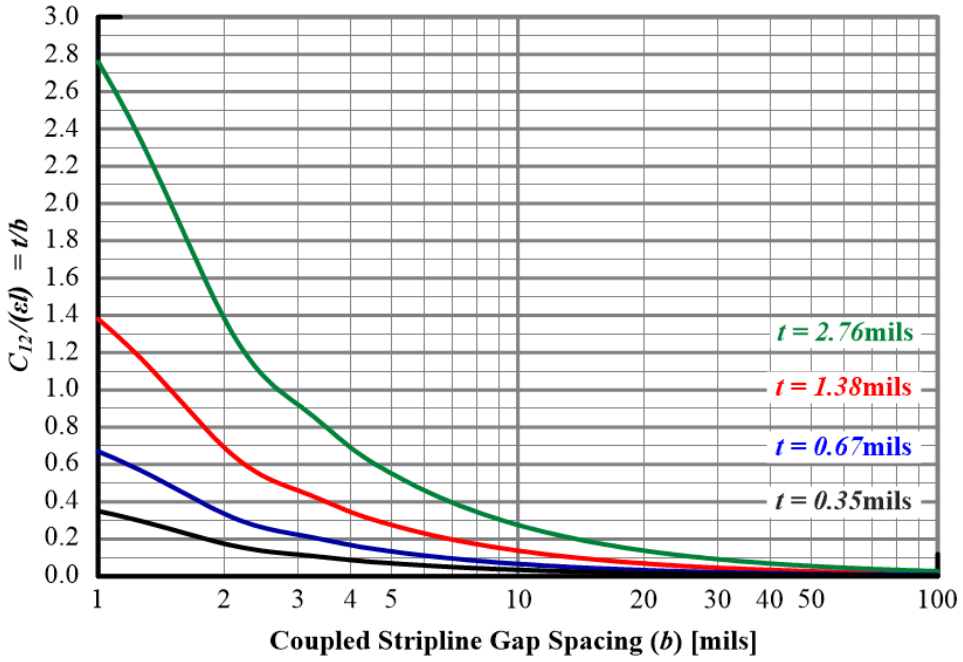


Fig. 84. Normalized coupled stripline gap capacitance per unit length.

The following investigation examines WPC mode analysis regarding how odd and even mode impedance influences S-parameters. Eq. (42) – Eq. (49), modified from in [111], provide a theoretical understanding to observe stripline separation influencing S-parameters. Fig. 85 demonstrates WPC network scrutiny now includes odd and even mode impedances from Eq. (26) and Eq. (27) and stripline separation. Matching ports two and three forces equal port voltage influencing input impedance $Z^{o}_{in,1} = Z^{e}_{in,1}$ because the isolation resistor behaves like an open circuit. Eq. (41) calculates $Z^{e}_{in,1}$ and includes 0.5 multiplier accounting symmetry splitting. When $l = \lambda / 4$ then $Z^{e}_{in,1} = \dfrac{(Z_{oe})^2}{2}$. Eq. (42) determines the reflection coefficient and set equal to S_{11} in Eq. (43).

$$Z_{in,1}^{e} = 0.5Z_{oe}\frac{Z_o + jZ_{oe}\tan\beta l}{Z_{oe} + jZ_o\tan\beta l} \tag{41}$$

$$\Gamma_1^o = \Gamma_1^e = \frac{Z_{in,1}^e - Z_o}{Z_{in,1}^e + Z_o} \tag{42}$$

$$S_{11} = \Gamma_1 \tag{43}$$

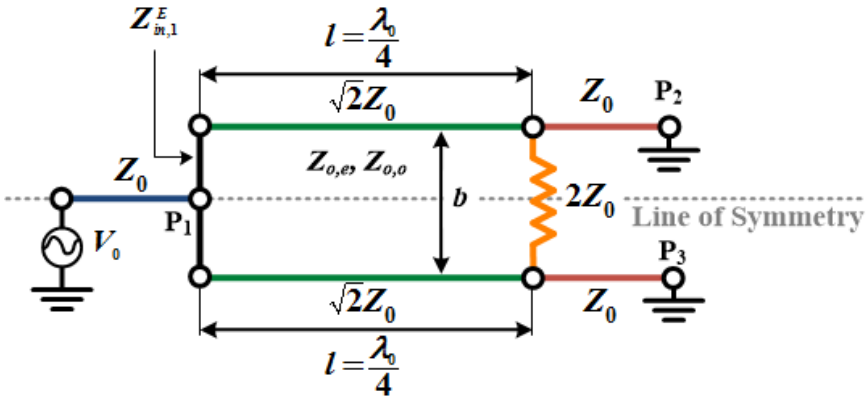


Fig. 85. Odd mode WPC analysis for impedance from port one.

Fig. 86 presents return loss, Eq. (43), when $l = \lambda/4$ and separation distance fluctuates. Figure 7.29 in [110] even mode impedance dominates S_{11} and crosses the -20dB mark when b = 40mils. Fig. 87 displays VSWR when separation distance changes for S_{11}.

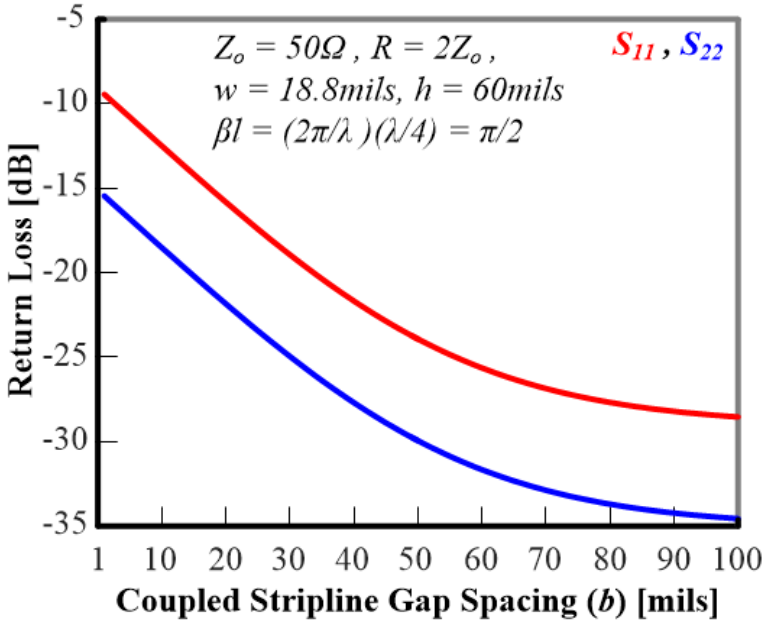


Fig. 86. 3dB WPC return loss when varying separation distance.

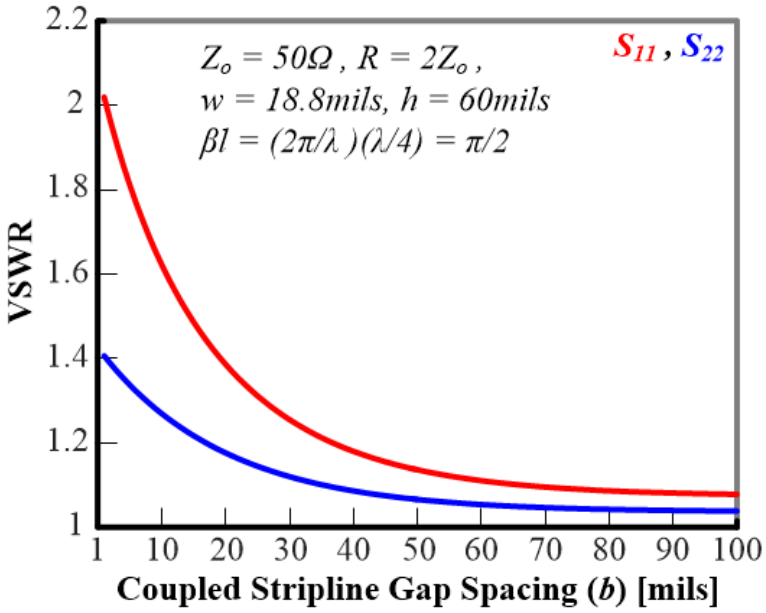


Fig. 87. 3dB WPC VSWR when varying separation distance.

Odd and even mode analysis divides the WPC along the symmetry line. Fig. 88 shows the odd mode divides the isolation resistor and shorts port one. The even mode open circuits the isolation resistor and port one. Analysis proceeds only with port two due to symmetry. Looking from port two toward port one Eq. (44) and Eq. (45) define input impedance.

$$Z_{in,2}^{e} = Z_{o,e}\frac{2Z_o + jZ_{o,e}\tan\beta l}{Z_{o,e} + j2Z_o\tan\beta l} \tag{44}$$

$$Z_{in2}^{o} = Z_{o,o} \,\|\, \left(R/2\right)\frac{jZ_{o,o}\tan\beta l}{\left(R/2\right) + jZ_{o,o}\tan\beta l} \tag{45}$$

Eq. (46) determines the even and odd mode reflection coefficients.

$$\Gamma_2^e = \frac{Z_{in2}^e - Z_o}{Z_{in2}^e + Z_o} \text{ and } \Gamma_2^o = \frac{Z_{in2}^o - Z_o}{Z_{in2}^o + Z_o} \tag{46}$$

Eq. (47) expresses the influence odd and even mode impedance on the port two return loss. Fig. 86 presents return loss, Eq. (47), when $l = \lambda/4$ and separation distance fluctuates. Figure 7.29 in [110] even mode impedance dominates S_{22} and crosses the -20dB mark when *b* = 15mils. Fig. 87 displays VSWR when separation distance changes for S_{22}.

$$S_{22} = 0.5\left(\Gamma_2^e + \Gamma_2^o\right) \tag{47}$$

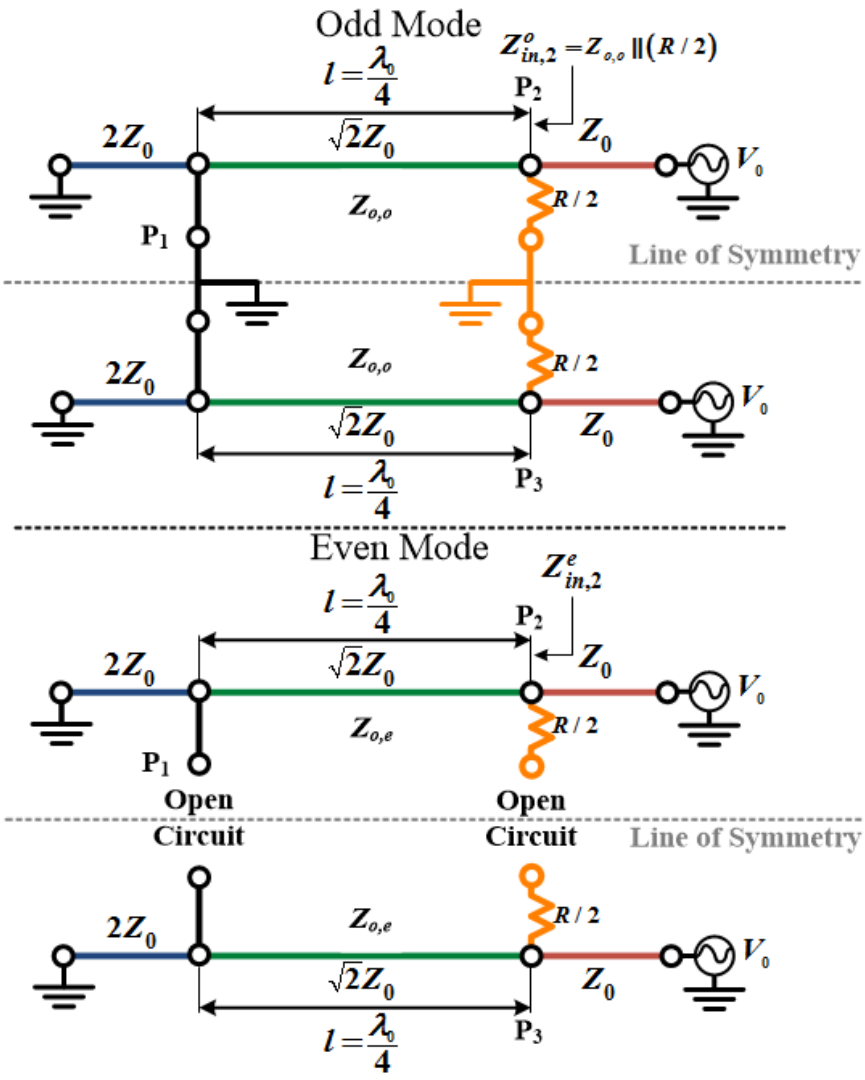


Fig. 88. 3dB WPC even and odd mode analysis includes stripline separation.

Eq. (48) demonstrates the even mode impedance controls insertion loss. Fig. 89 plots Eq. (48) and varies stripline separation demonstrates reducing transmission line

separation increases insertion loss and increases capacitance thus shunting parallel transmission lines.

$$|S_{21}|^2 = |S_{31}|^2 = 0.5\left(1 - |S_{11}|^2\right) \tag{48}$$

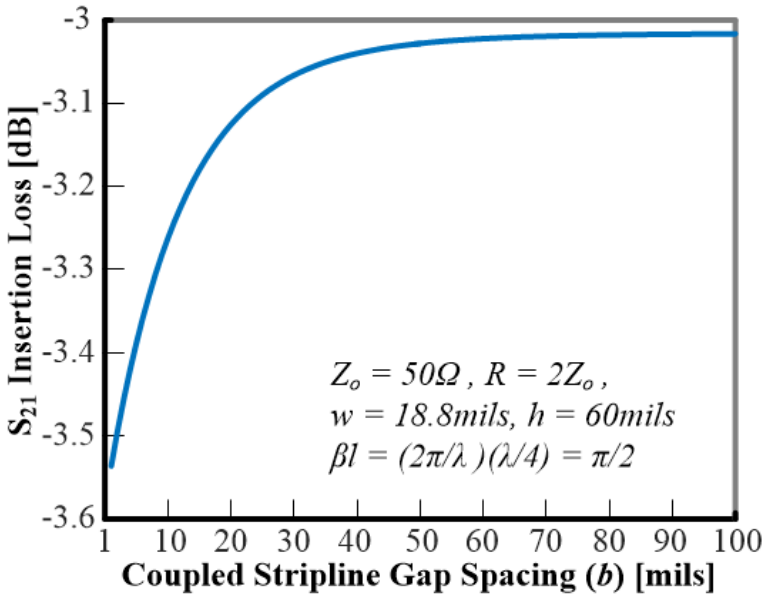


Fig. 89. 3dB WPC insertion loss versus gap spacing.

Eq. (49) shows the odd mode impedance dominates isolation due to the isolation resistor. The second term in Eq. (49) originates after performing voltage division across the isolation resistor. Eq. (49) originates from a lossless and reciprocal three port network assume matched ports one and three [40]. Fig. 90 demonstrates increasing striplines separation decreases isolation and increases crosstalk.

$$|S_{32}|^2 = 1 - 2\left|\frac{Z_{in2}^o}{Z_{in2}^o + (R/2)}\right|^2 - |S_{22}|^2 - |S_{21}|^2 \tag{49}$$

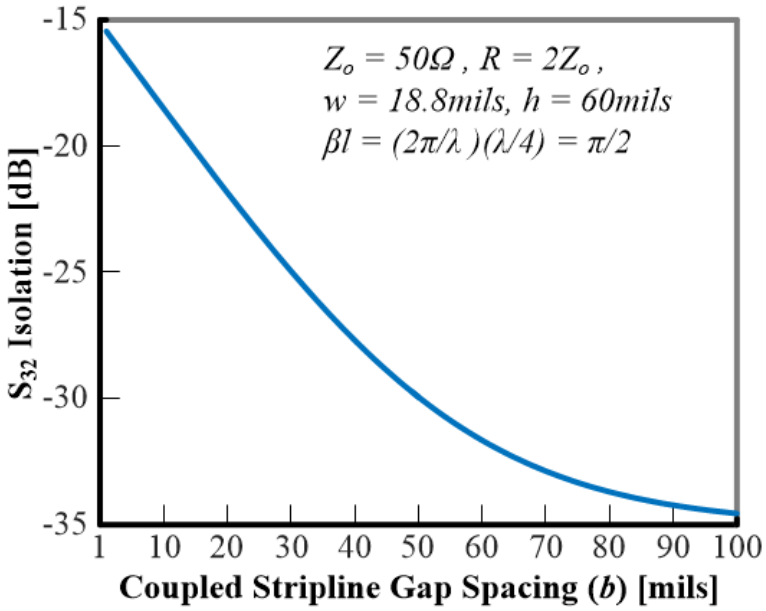


Fig. 90. 3dB WPC isolation versus gap spacing.

Fig. 91 plots Eq. (11) showing effective line width increases by metallization thickness and impedance. Fig. 91 shows a fundamental limit exists regarding minimal stripline separation. Fig. 91 illustrates different effective widths with a 36.4mil stripline width. The minimal stripline separation also increases and decreases with frequency. Stripline width varies by impedance and dielectric constant and both vary by frequency.

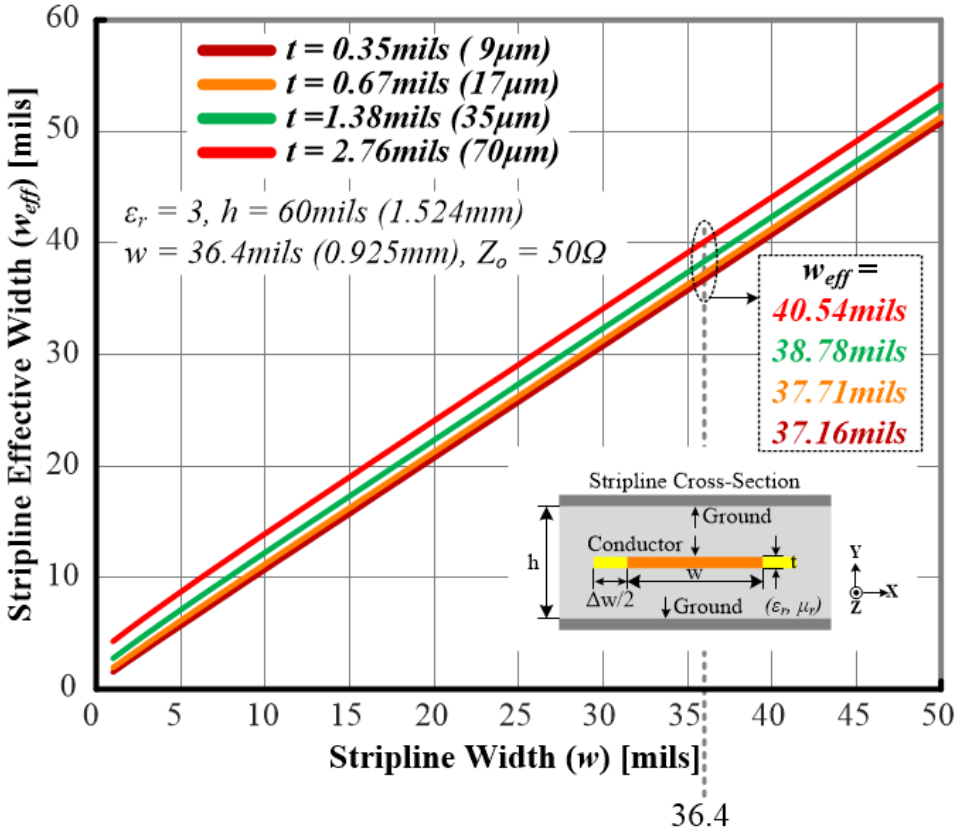


Fig. 91. Stripline Δw varies by metal thickness (t) and line width (w).

HFSS assisted optimizing the stripline separation for the Rev2 four stage design featured in Fig. 74. Table XIV lists the gap spacing selected based on multiple simulation iterations observing impedance, isolation, insertion loss, wave propagation, and current flow.

TABLE XIV
REV2 FOUR STAGE GAP PARAMETERS

TL	W [mil]	Gap (*b*) [mils]
Stage 4	10.3	20.6
Stage 3	14.9	14.9
Stage 2	19.6	19.6
Stage 1	28.4	28.4

IV.F.2. Laminate Thermal and Power Handling

Striplines do not enjoy the power capability waveguides or coax lines hold. Increasing power introduces laminate heating consequently manipulating dielectric thermal properties. Stripline power capability depends on dielectric and circuit features introducing resistance and extra heating, i.e., vias and discontinuities. The Rogers RO3003™ [80] possess a mechanical breakdown temperature (T_g) of 662^{o}F (350^{o}C) and a delaminating temperature (T_d), temperature when the coper lifts off the surface, of 932^{o}F (500^{o}C). Rogers does not publish dielectric breakdown power levels for the RO3003™.

The substrate property, Coefficient of thermal expansion (CTE), indicates the amount material expands when heated. CTE varies depending upon the measurement plane, X, Y, and Z. Reaching T_g rapidly raises CTE triggering visible laminate swelling. Rogers RO3003™ [80] provides a CTE of 17ppm/^{o}C X-plane, 16 ppm/^{o}C Y-plane, and 25ppm/^{o}C Z-plane. When vias exist in the circuit, a high Z-plane CTE indicates a high temperature swell point. Reaching CTE thermal range extremes yields interconnect breakage via thermal expansion or contraction forming open circuits. The Rogers RO3003™ [80] provides 25ppm/ ^{o}C Z-plane CTE and -67^{o}F – 550.4^{o}F (-55^{o}C - 288^{o}C) thermal range.

IV.F.3. Embedding Isolation Resistors

A multilayer Wilkinson combiner requires suitable isolation resistors. All Wilkinson combiners presented in Table V use packaged surface mount resistors. These resistors introduce additional inductance and capacitance from the resistor and solder. Assembling a multilayer circuit requires minimal height resistors or resistors positioned in a "dielectric pocket." The later introduces air gaps and changes the dielectric constant and board integrity. The former implies the resistor height less than the copper thickness.

Thin film resistors still require packaging and the part height exceeds 1.3mil (0.017mm). Standard surface mount packaging averages an 18mil height. An alternative method meant imbedding the resistor into the dielectric. Rather than spend precious time evaluating different methods, I selected to implement the resistors chosen previously by Roger for his Rev1 design. Ohmega Technologies cherishes a thirty-year record providing reliable thin film resistors for various applications. Thus OhmegaPly® [79] embedded resistor technology met the criteria. A thin film constructed from electrodeposited nickel phosphorous (NiP) on copper film forming a resistive-conductive metal alloy called OhmegaPly®. Fig. 92 shows the embedding process. Photoetching removes the copper material down to the dielectric. Then laminate the OhmegaPly® material to the dielectric. The OhmegaPly® thickness (t_R) < 0.039mil (0.001mm) offers more than a magnitude difference less than the Rogers RO3003™ ½oz copper thickness. OhmegaPly® provides reliability by removing extra packaging and solder found with surface mount resistors, stable resistance over frequency beyond 20 GHz, and design predictability.

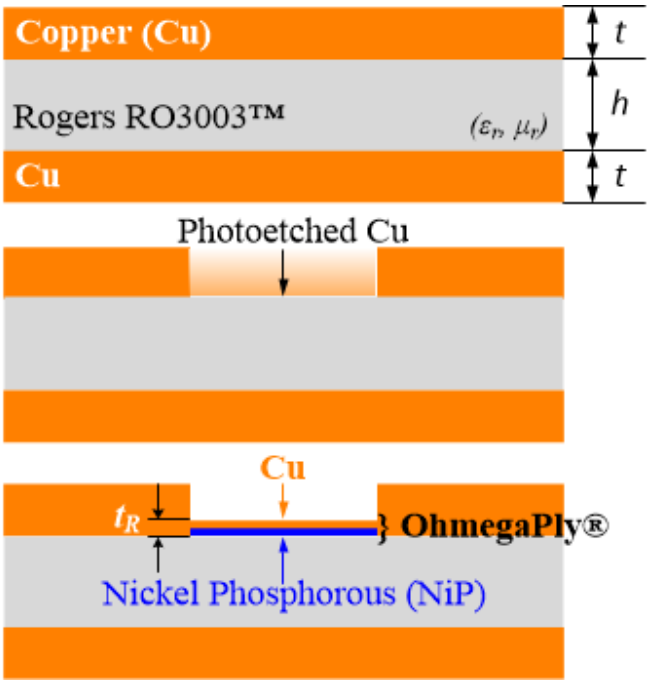


Fig. 92. Manufacturing steps for applying OhmegaPly® thin films to a substrate.

To design a resistor involves its value, a set length or width, and sheet resistivity (R_s). Resister design uses Eq. (50) for the OhmegaPly® thin film. The sheet resistivity assigned units of ohms-per-square and determined by the film thickness (t_R) and bulk resistivity (ρ) using Eq. (51). Taking the inverse of ρ provides conductivity (σ) seen in Eq. (52). The multilayer WPC used 100Ω/□ sheet resistance providing a 5% tolerance. Because manufacturing undercut errors a sheet resistance of 135Ω/□ substituted for circuit design. HFSS's mathematical limitations limit capability to solve extremely thin materials. To optimize the WPC design in HFSS [72], an OhmegaPly® 1mil film thickness with σ = 635S/m permitted simulation. Wang [112] presented a lumped component method to model surface mount and thin film resistors for multilevel WPCs.

$$R = R_s \frac{\text{Resistor Length}}{\text{Resistor Width}} [\Omega] \tag{50}$$

$$R_s = \rho / t_R [\Omega / \square \tag{51}$$

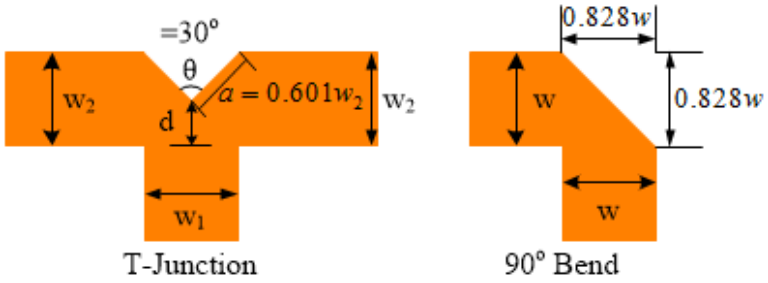
$$\sigma = \frac{1}{\rho} [S / m \text{ or } \mho \tag{52}$$

IV.F.4. Stripline Transitions

A step transition occurs when transmission line impedance changes from value to another. A turn discontinuity occurs when a transmission line bends due to circuit design and physical configuration. Chadha and Gupta [113 and 114] describe compensation techniques and Fig. 93 (a and b) shows the different transitions implemented for the WPC.

The first stage requires splitting the 50Ω line into two transmission lines with different impedance. The transmission line split forms a T-junction. The T-junction introduces a stepped transition and two right angle turns. Chadha and Gupta [113 and 114] describe a T-junction compensation technique summarized in Fig. 93 (a). An isosceles triangle forms the notch. The design method in [113 and 114] calls for a 1:1:1 and $1/\sqrt{2}:1:1$, however, the Rev2 stepped impedances did not match the ratios described in [113 and 114]. Addressing the difference required varying hypotenuse (*a*) and inset (*d*) using HFSS to optimize the notch and reduce the reflection coefficient magnitude to a minimum.

The right angle turn causes a discontinuity and introduces impedance reactance increasing the reflection coefficient magnitude. Chamfering or mitering the bend a sufficient amount reduces the reflection coefficient magnitude to a minimum. HFSS assisted optimizing the Rev2 four stage WPC right angle turns featured in Fig. 74 by varying the 90° corner chamfering shown in Fig. 93 (b).



(a) (b)

Fig. 93. Stripline transition designs for a T-junction (a) and right angle chamfering (b).

IV.G. Rev2 Simulation

The author and assistance by colleagues David C. and Jenn completed the Rev2 HFSS simulations and layout. Fig. [95 - 107] show the measured results. Table XV provides a major result summary and comparison with the Mini-Circuit combiner and design standards.

TABLE XV
WILKINSON COMBINER REV2 SIMULATION COMPARISON

Source	Design Std.	Mini-Circuit [83]	Rev2
Freq. [GHz]	0.8 – 3	0.6 - 3.6	0.5-3.3
Bandwidth	3.75:1	6:1	6.6:1
Min. RL P1 [dB]	-15	-14	-17
Min. RL P2 – 9 [dB]	-20	-19	-20
VSWR P1	1.5:1	1.5:1	2.1:1
VSWR P2 - 9	1.4:1	1.4:1	1.2:1
IL [dB]	1.5 ± 0.8	1.5 ± 0.6	1 ± 0.47
Amp. Imbalance [dB]	± 0.5	± 0.5	± 0.1
Phase Unbalance	± 4.0°	± 4.0°	± 0.35°
Max Phase Std. Dev.	≤ ± 1.5°	± 1.54°	± 0.23°
Min. Iso. [dB]	-16	-16.0	-31

Fig. 94 displays averaged return loss, insertion loss, and isolation results. Each port and transmission path experienced analogous results. Port one possess a minimum -17dB return loss (P_1 RL) over 0.8 – 3.0 GHz and Ports 2 – 9 possess a minimum -20dB return loss (Avg. P_{2-9} RL) over 0.8 – 3 GHz. Insertion loss remains steady over 0.8 – 3.0 GHz and averaging -9.8dB. A -31dB minimum isolation spans 0.8 – 3.0 GHz. Measured bandwidth stretches from 500 MHz to 4.0 GHz. Max operating ability between 500 MHz and 3.3 GHz providing a 6.6:1 bandwidth.

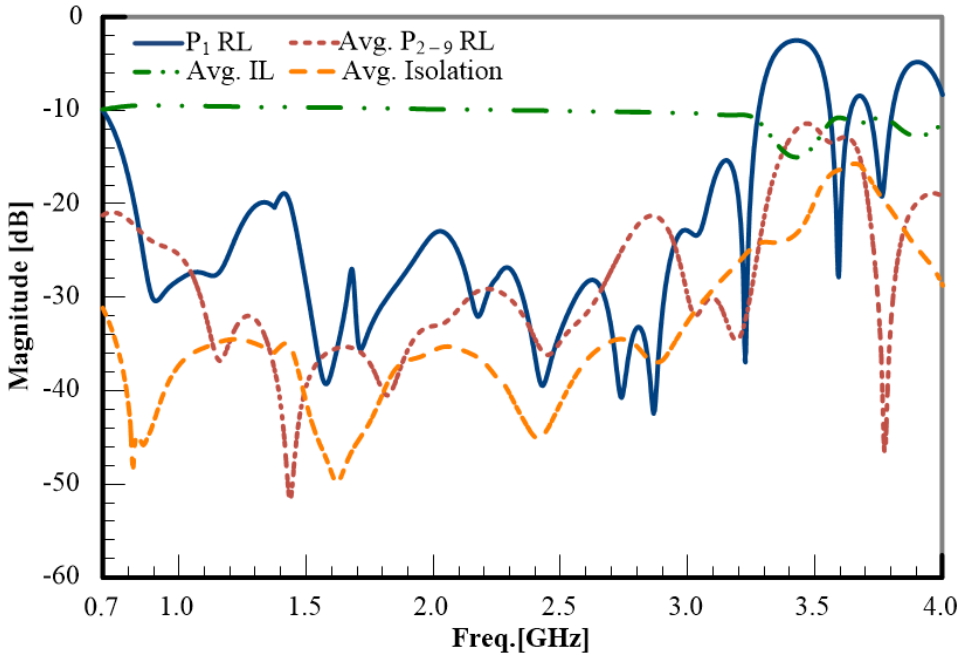


Fig. 94. Rev2 combiner simulated results.

Fig. 95 and Fig. 96 presents the impedance information, first the VSWR then the Smith chart. Port one shows a 1.3:1 VSWR between 800 MHz to 3.0 GHz and approximately 2% reflected power. Port one shows a 2.1:1 VSWR between 500 MHz to 3.3 GHz and approximately 12.6% reflected power. Ports 2 – 9 show a mean VSWR of 1.2:1 and 1% reflected power between 800 MHz and 3.0 GHz. Ports 2 – 9 possess a mean VSWR of 1.2:1 and 1% reflected power over 0.5 – 3.3 GHz. The Smith charts show a good 50Ω impedance match for Ports 2 – 9 and good impedance matching for Port one over 0.5 – 3.3 GHz.

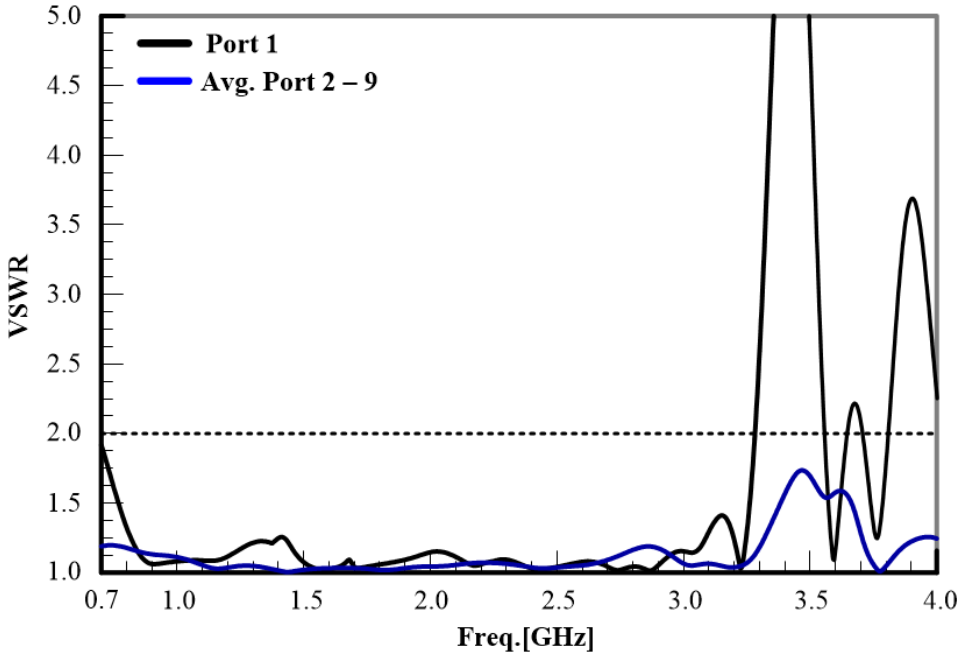
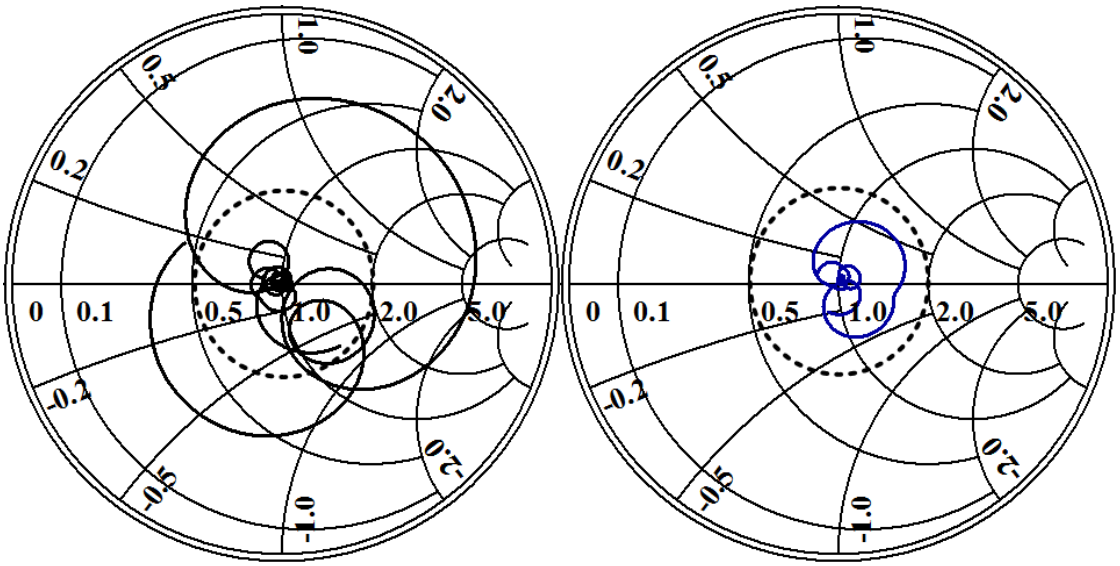


Fig. 95. Rev2 combiner VSWR simulation results.



(a) (b)

Fig. 96. Rev2 combiner simulation impedance from 700 MHz to 4.0 GHz with the dashed circle marking VSWR = 2: (a) Port one and (b) Ports 2 – 9.

Fig. 97 - 101 discuss the transmission phase. Fig. 97 shows good agreement from Ports 2 – 9 from 700 MHz to 4.0 GHz. Fig. 98 gives a magnified phase view between 1.795 and 1.805 GHz showing negligible phase variation of $\leq \pm 1^{o}$ between ports. Fig. 99 concludes an average $\pm 0.35^{o}$ transmission phase fluctuation.

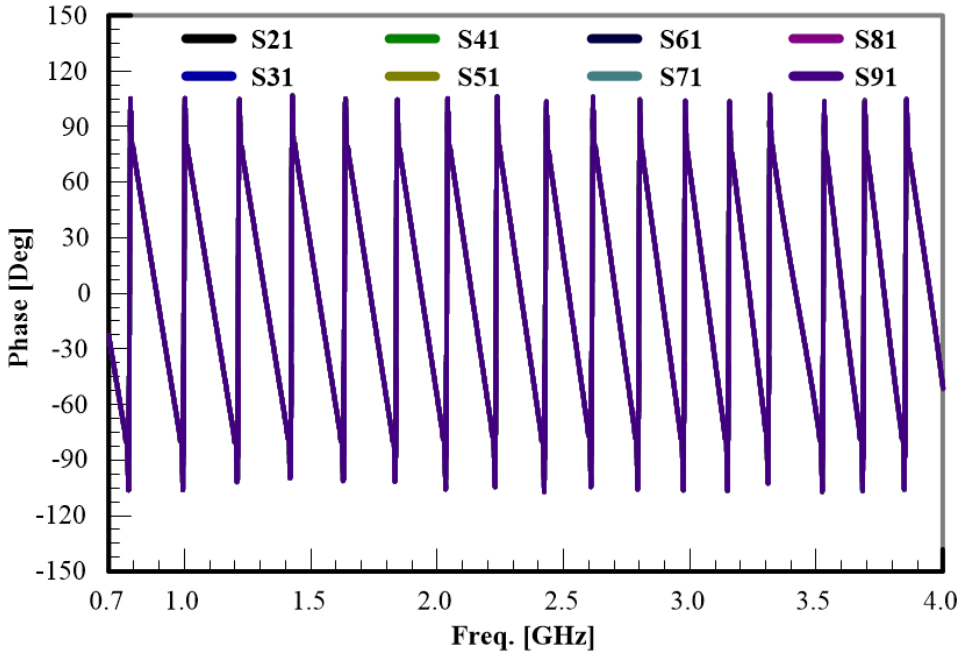


Fig. 97. Rev2 combiner simulated transmission phase from Ports 2 – 9 to Port one.

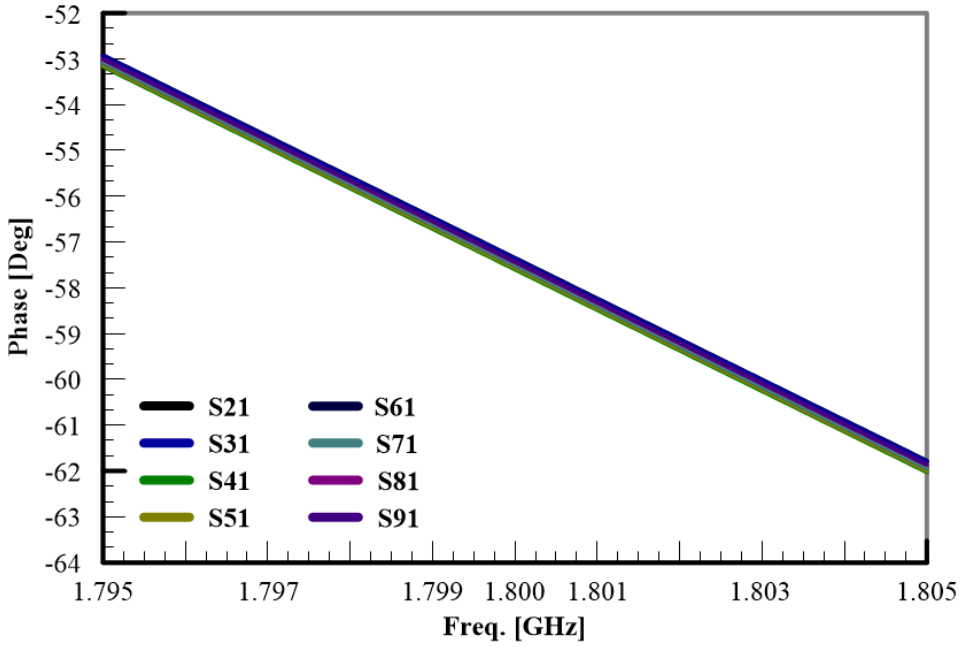


Fig. 98. Rev2 simulated transmission phase from Ports 2 – 9 to Port one showing phase stability.

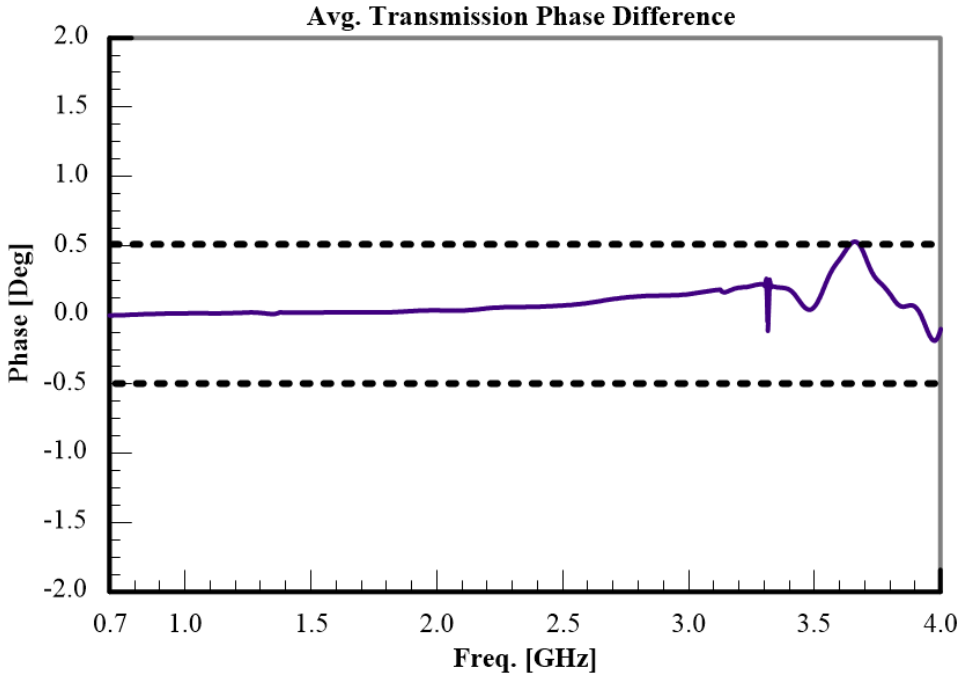


Fig. 99. Rev2 combiner simulated average transmission phase difference from Ports 2 – 9 to Port one.

Fig. 100 and Fig. 101 display phase information for specific frequencies. Fig. 100 shows almost no variation between the maximum and minimum phase. Fig. 101 shows phase variance remains constant. Table XVI lists the transmission path mean phase standard deviation in 200 MHz steps. The standard deviation shows an increasing deviation from ± 0.04° to ± 0.23°.

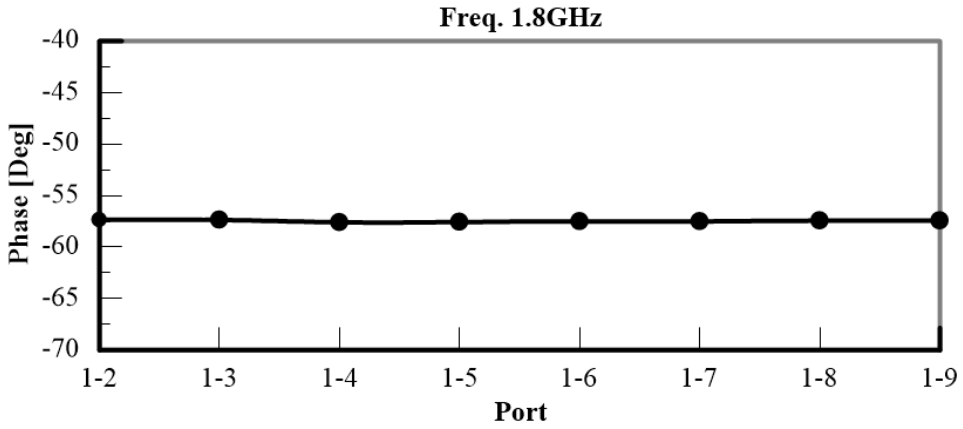


Fig. 100. Rev2 simulated 1.8 GHz transmission phase from Ports 2 – 9 to Port one.

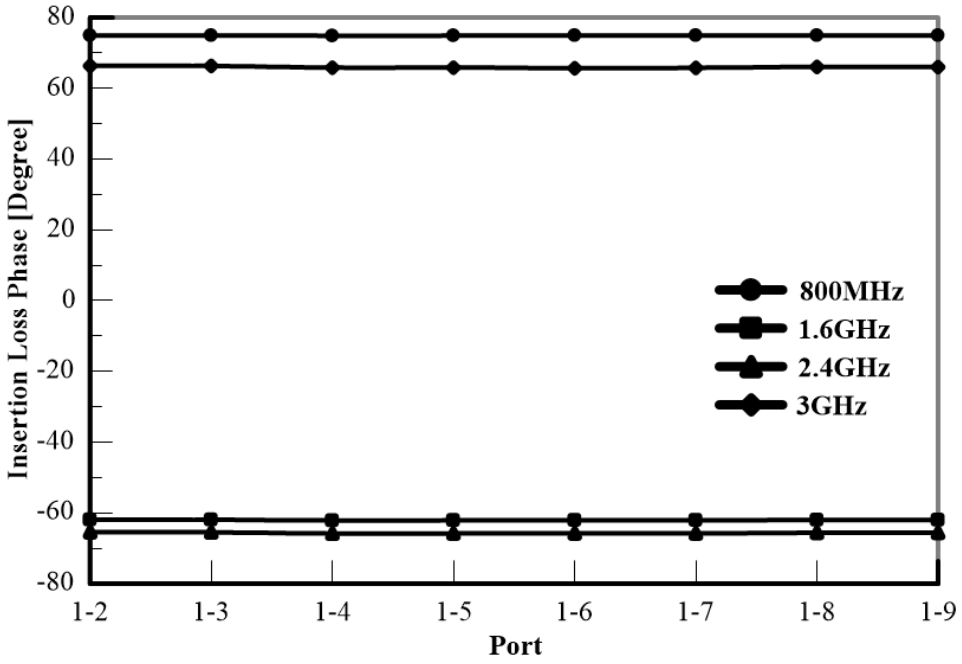


Fig. 101. Rev2 simulated transmission phase from Ports 2 – 9 to Port one.

TABLE XVI
REV2 SIMULATED PHASE ERROR

Freq. [GHz]	Mean	σ [+/- Deg.]
0.8	74.92	0.04
1.0	87.66	0.05
1.2	-80.20	0.06
1.4	-69.51	0.07
1.6	-62.03	0.08
1.8	-57.47	0.08
2.0	-56.29	0.09
2.2	-58.93	0.11
2.4	-65.67	0.13
2.6	-76.99	0.15
2.8	87.03	0.19
3.0	65.98	0.23

Fig. 102 shows the three level combiner insertion loss higher than 9dB. A -1.0dB mean isertion loss over 0.5 – 3.3 GHz. A 0.47dB average loss for per transmission path.

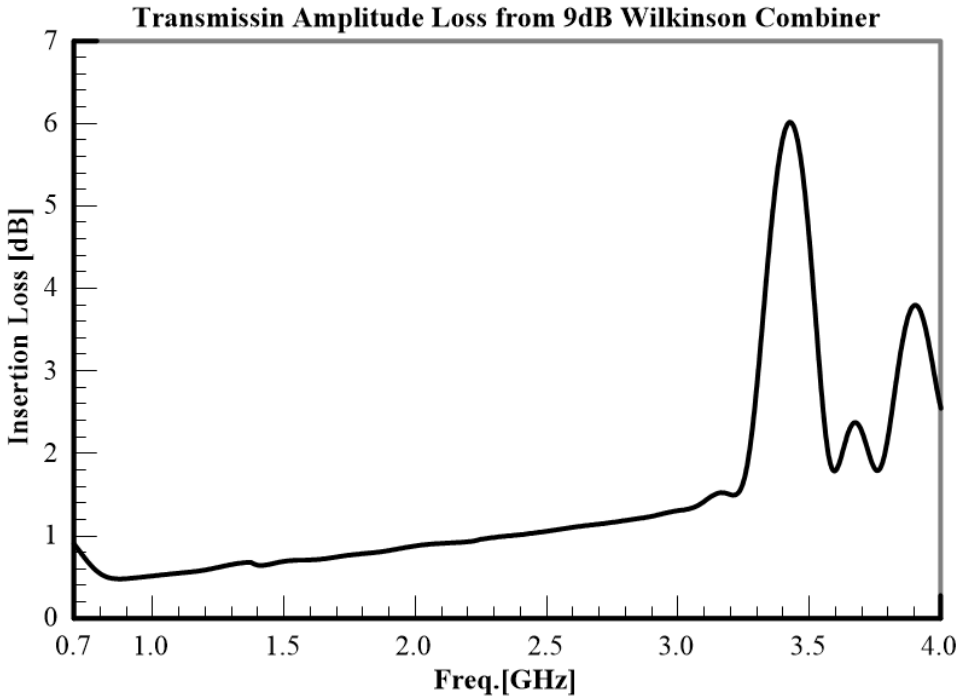


Fig. 102. Rev2 combiner average insertion loss simulated from Ports 2 – 9 to Port one.

Fig. 103 shows static frequency insertion loss per port. The insertion loss variance between 800 MHz and 3.0 GHz agrees with the 0.47dB loss variation per transmission path. The ± 0.4dB insertion loss swing between maximum (-10.3dB) to minimum (-9.5dB). Fig. 103 shows consistent transmission path losses.

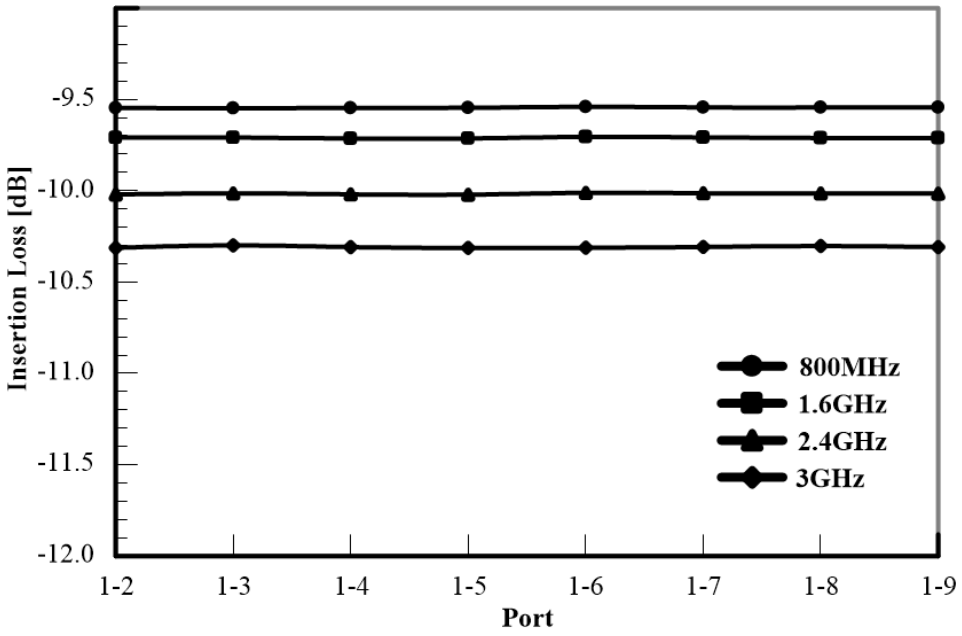


Fig. 103. Rev2 simulated insertion loss from Ports 2 – 9 to Port one.

Fig. 104 shows static frequency isolation by port and different parallel path combinations validate consistency. When ports branch off the same combiner, see 23, 45, and 67 the isolation reduces. The 3.0 GHz frequency begins isolation reduction to its 3.3GHz minimum.

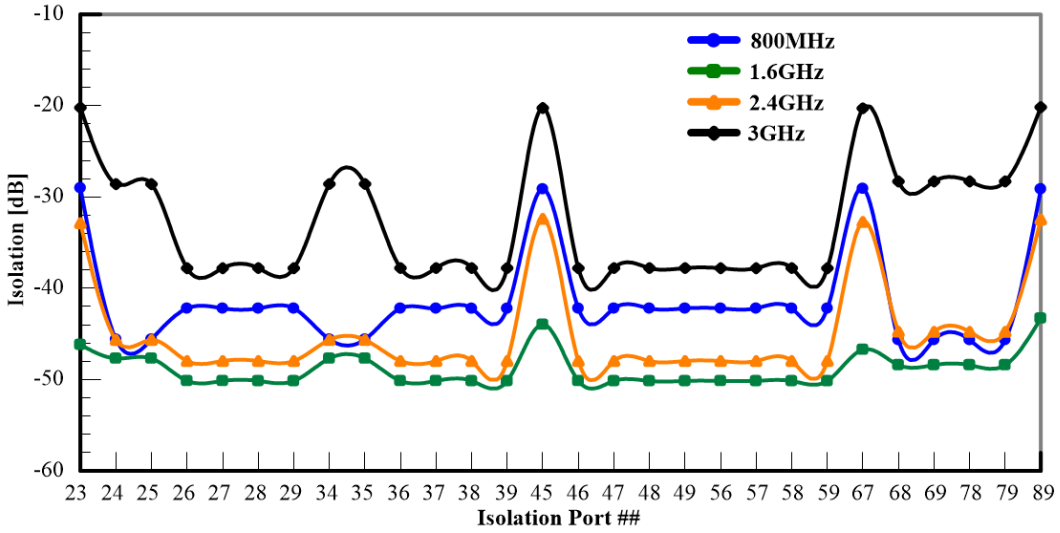


Fig. 104. Rev2 isolation static frequencies simulated between Ports 2 – 9.

Fig. 105 displays the average amplitude difference traversing all signal transmission paths. Amplitude imbalance takes the transmission magnitude (S_{21}) and subtracts S_{31}. I calculated amplitude imbalance for 28 combinations then averaged together. The amplitude 0.17dB max difference and an approximate 0dB minimum provide a ± 0.085dB amplitude variation. Rev2 provides an average amplitude difference less than 0.1dB between 500 MHz and 4.0 GHz.

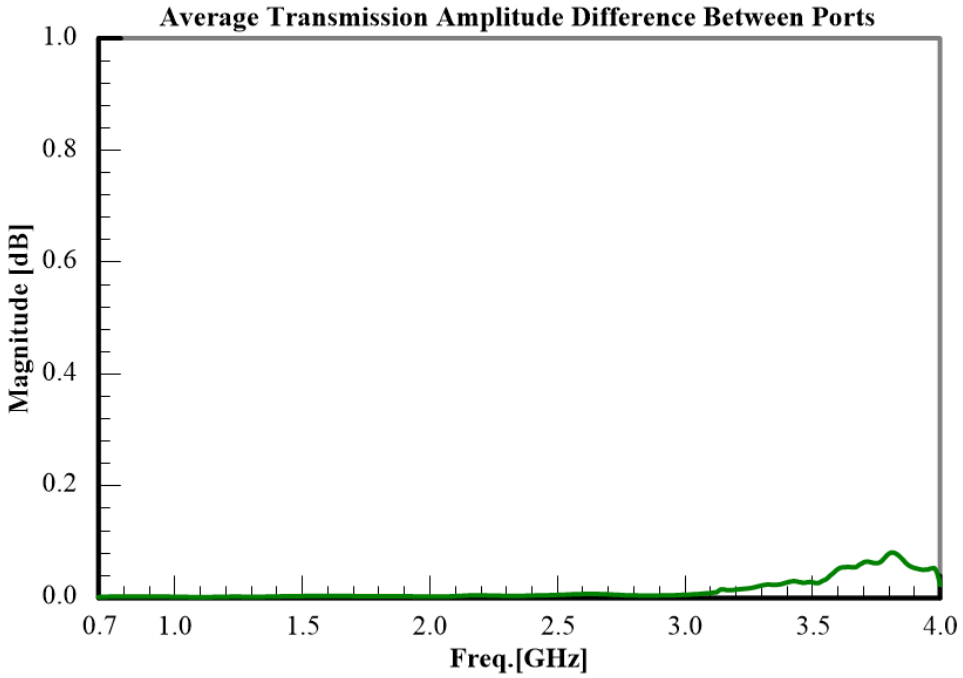


Fig. 105. Rev2 combiner amplitude imbalance simulation from Ports 2 – 9 to Port one.

Fig. 106 displays the signal combining efficiency. Eq. (10) shows signal combining efficiency and device efficiency equivalence. The combiner provides an average single path loss of 0.47dB from Port one to Ports 2 – 9. Fig. 106 shows a 72% initial efficiency for eight combined signals. Fig. 52 does not consider loss frequency response. Fig. 106 shows an 80% efficiency fluctuating ± 10% and plummets. Electrically longer transmission paths steadily decline efficiency.

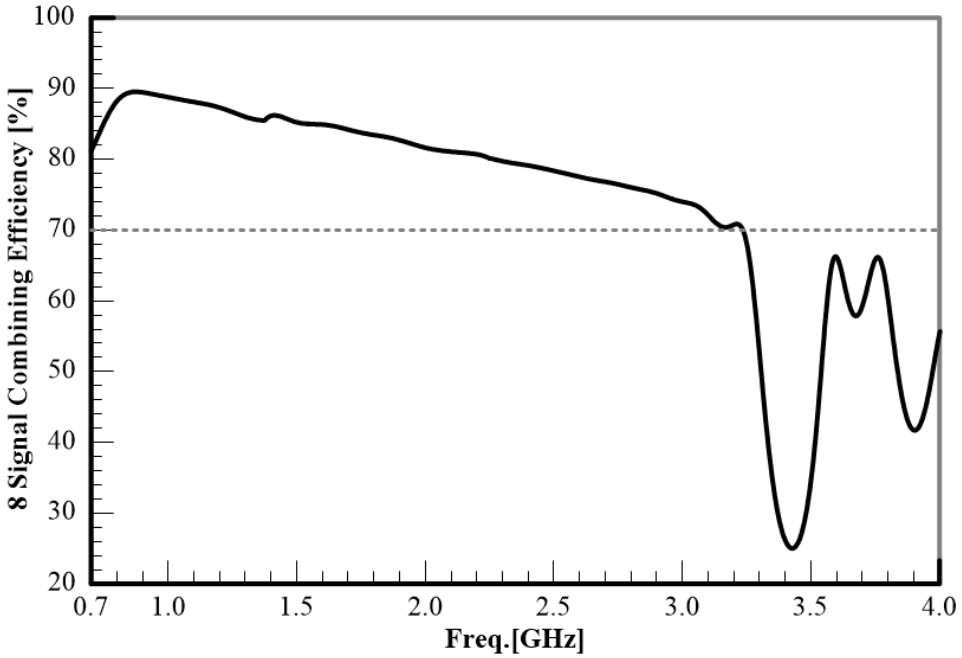


Fig. 106. Rev2 combiner efficiency extracted from averaged power transmitted from Ports 2 – 9 to Port one.

Examining the simulation results for the Rev2 combiner compared to the set design standards for the design shows agreement.

A. 3.75:1 Minimum Bandwidth (Yes)
B. -15dB Minimum Port one Return Loss (Yes)
C. -20dB Minimum Ports 2 – 9 Return Loss (Yes)
D. 1.5:1 VSWR Port one (Yes)
E. 1.4:1 VSWR Ports 2 – 9 (Yes)
F. 1.5dB ± 0.8dB Insertion Loss (Yes)
G. ± 0.5dB Amplitude Imbalance (Yes)
H. ± 4^{o} Phase Unbalance (Yes)
I. Transmission Phase Standard Deviation ≤ ± 1.5^{o} (Yes)
J. -16dB Minimum Isolation (Yes)

IV.H. Rev2 Measurements

The author and assisted by colleagues David C. and Jenn completed the Rev2 measurements, analysis, and antenna testing. A Keysight FieldFox RF Vector Network Analyzer (VNA) 9923A [81] tested and recorded the combiner measurements using custom designed phased matched cables from Times Microwave [82]. Fig. [109 – 121] show the measured results. Table XVII provides a major result summary and comparison with the Mini-Circuit combiner.

TABLE XVII
WILKINSON COMBINER REV2 MEASUREMENT COMPARISON

Source	Design Std.	Mini-Circuit [83]	Rev2 Std.	Rev2 Max
Freq. [GHz]	0.8 – 3	0.6 - 3.6	0.8 – 3	0.5 – 3.28
Bandwidth	3.75:1	6:1	3.75:1	6.56:1
Min. RL P1 [dB]	-15	-14	-11.74	-7.8
Min. RL P2 – 9 [dB]	-20	-19	-21.4	-18.1
VSWR P1	1.5:1	1.5:1	1.7:1	2.4:1
VSWR P2 - 9	1.4:1	1.4:1	1.2:1	1.3:1
IL [dB]	1.5 ± 0.8	1.5 ± 0.6	1.43 ± 0.78	1.93 ± 1.28
Amp. Imbalance [dB]	± 0.5	± 0.5	± 0.41	± 0.52
Phase Unbalance	± 4.0°	± 4.0°	± 2.0°	± 4.0°
Max Phase Std. Dev.	≤ ± 1.5°	± 1.54°	± 1.38°	± 1.89°
Min. Iso. [dB]	-16	-16.0	-17.9	-12.2

Fig. 107 displays averaged return loss, insertion loss, and isolation results. Each port and transmission path experienced analogous results. Port one provides a minimum -11.74dB return loss (P_1 RL) over 0.8 – 3.0 GHz and Ports 2 – 9 possess a minimum -21.4dB return loss (Avg. P_{2-9} RL) over 0.8 – 3.0 GHz. The insertion loss over 700 MHz – 4.0 GHz averages -10.8dB and averages -10.4dB over 0.8 – 3.0 GHz. A -37dB isolation minimum spans 0.8 – 3.0 GHz. Measured bandwidth stretches from 500 MHz to 4.0 GHz. Max operating ability between 500MHz and 3.28 GHz providing a 6.56:1 bandwidth. All data plots for Rev2 cover 0.7 – 4.0 GHz to provide comparison between

other plots provided. The Rev2 plots also display required operating range 0.8 – 3.0 GHz.

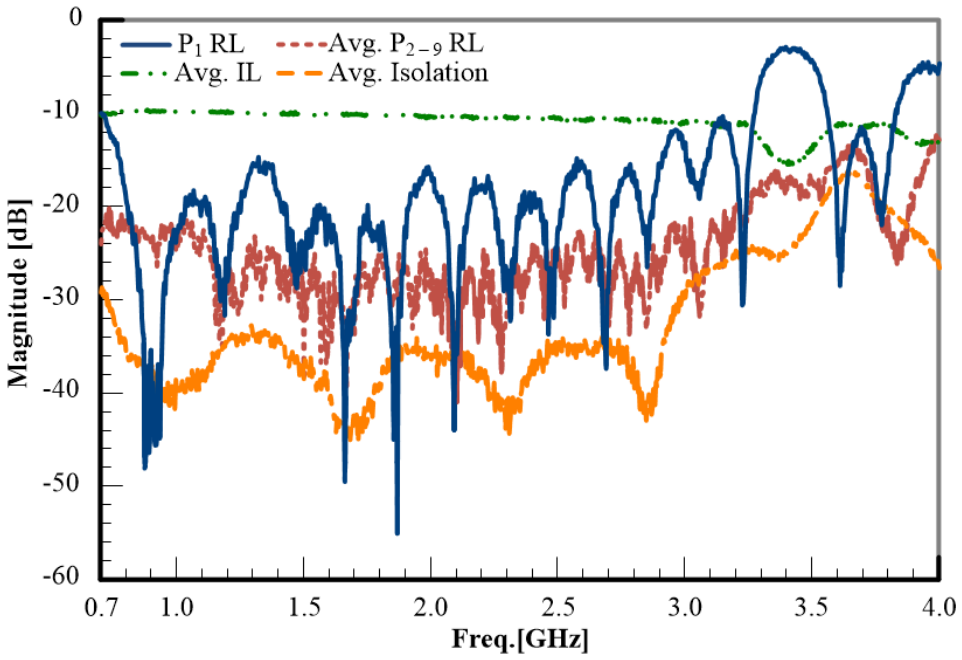


Fig. 107. Rev2 combiner measured results.

Fig. 108 and Fig. 109 presents the impedance information, first the VSWR then the Smith chart. Port one shows a 1.7:1 VSWR between 800 MHz to 3.0 GHz and 7.5% reflected power. Port one shows a 2.4:1 VSWR between 500 MHz to 3.28 GHz and 16% reflected power. Ports 2 – 9 show a mean VSWR of 1.2:1 and 1% reflected power between 800 MHz and 3.0 GHz. Ports 2 – 9 possess a mean VSWR of 1.3:1 and 1.75% reflected power over 0.5 – 3.28 GHz. The Smith charts show a good 50Ω impedance match for Ports 2 – 9 and good impedance matching for Port one over 0.7 – 3.28 GHz.

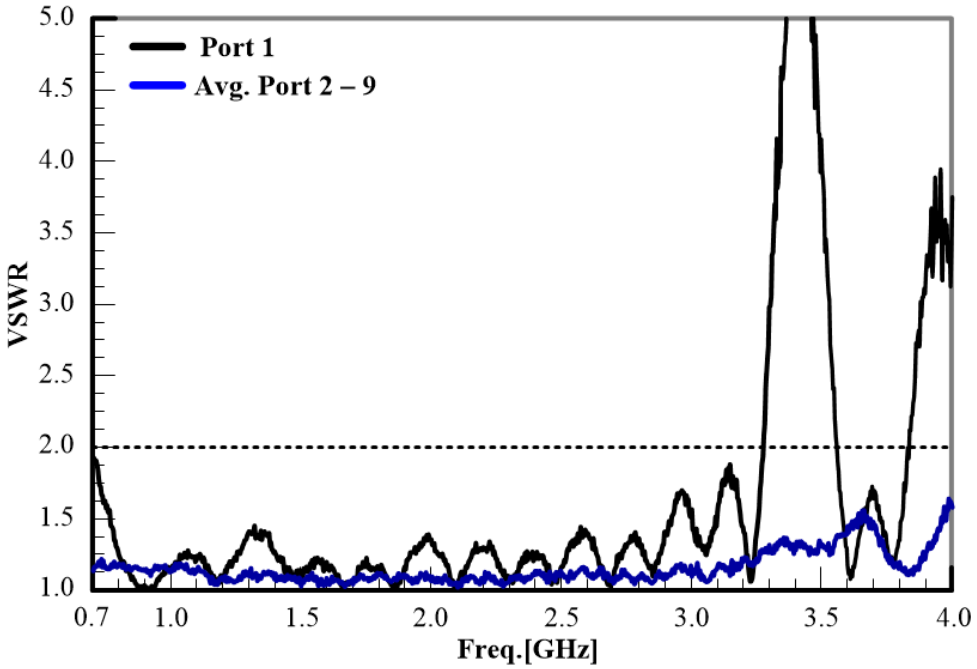
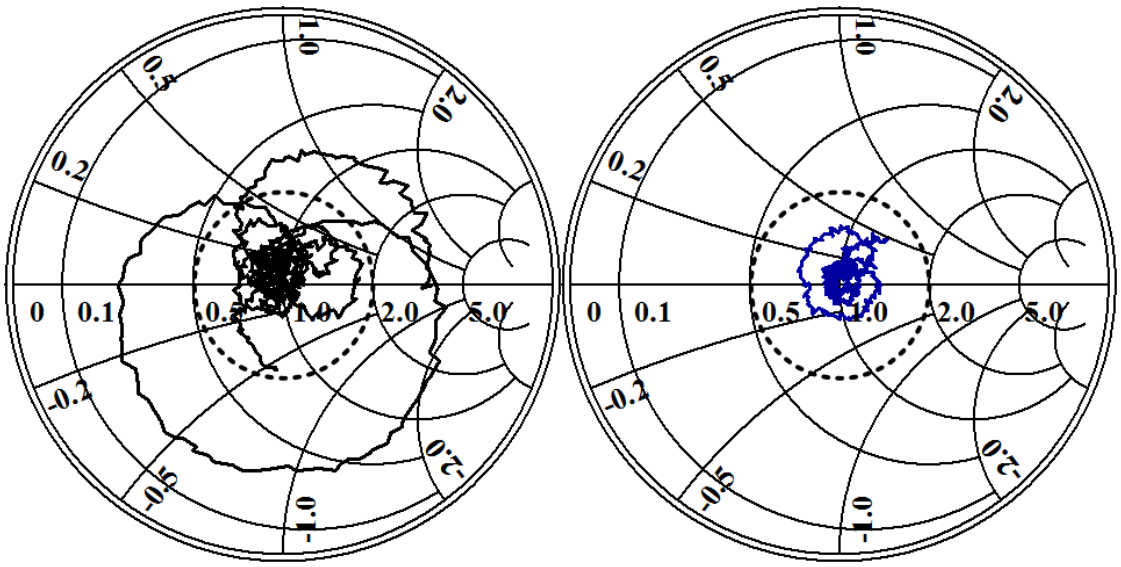


Fig. 108. Rev2 combiner VSWR measured results.



(a) (b)

Fig. 109. Rev2 combiner measured impedance from 700 MHz to 4.0 GHz with the dashed circle marking VSWR = 2: (a) Port one and (b) Ports 2 – 9.

Fig. 110 – 114 discuss the transmission phase. Fig. 110 shows good agreement from Ports 2 – 9 between 700 MHz to 4.0 GHz. Transmission phase inflections occur ± 90° introduced by the WPC quarter wave transmission line sections. Any visual phase variation beyond ± 90° originates from the graphing software. Fig. 111 gives a magnified phase view between 1.795 and 1.805 GHz. Fig. 111 presents transmission phase variation by port and frequency and displaying a ± 2° separation. Fig. 112 displays Rev2 accomplishes a mean ± 0.5° transmission phase variance.

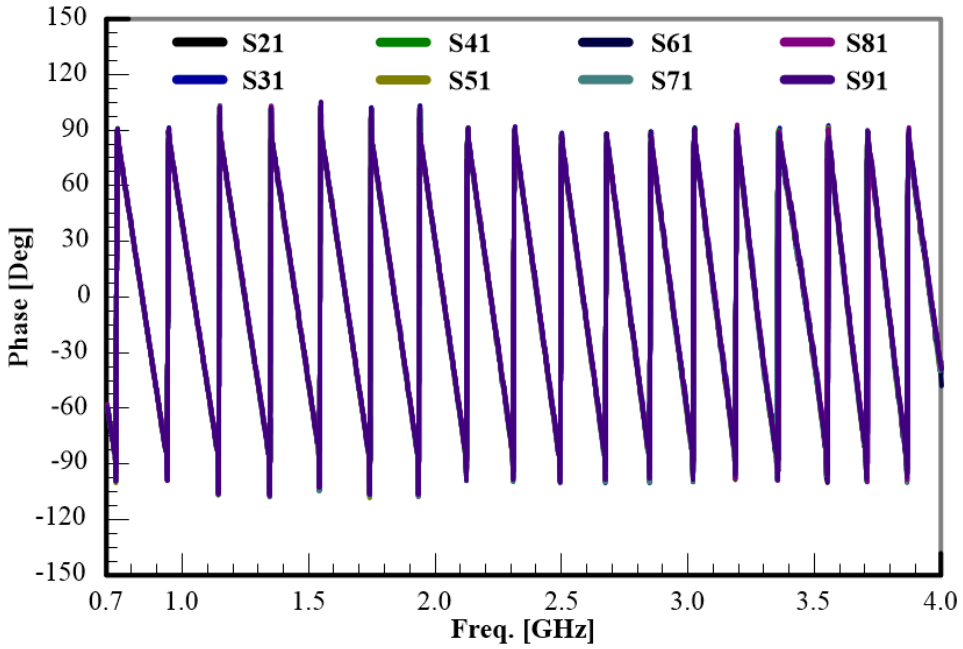


Fig. 110. Rev2 combiner measured transmission phase from Ports 2 – 9 to Port one.

Examining the data for Fig. 110, I observed the phase inflection from 90° to -90° progressed uniformly. Placing the measured phase data under scrutiny, small variations occur at the inflection points. Some ports would take one or two frequency steps longer

to reach the inflection point than the other ports. I offer two explanations. First, a small mathematical error originates from the VNA calibration or signal sampling. The VNA measurement error appears when the phase reading would flip negative, positive, then negative, and back positive again within a few frequency steps. These errors rarely occur. Second, slight differences in trace lengths, widths, and minor losses due to manufacturing contributed to the inflection point delay.

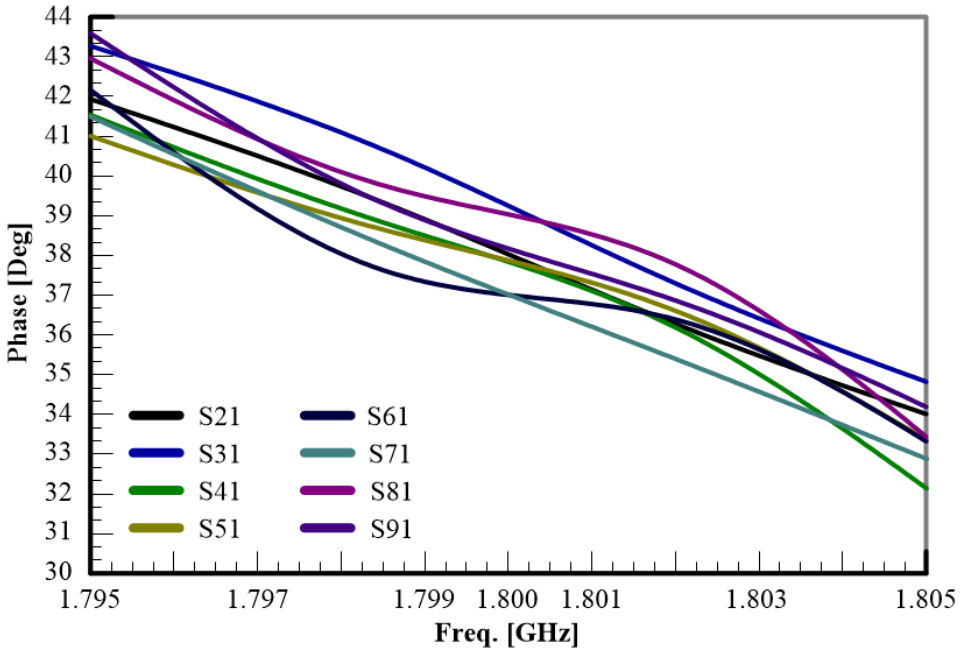


Fig. 111. Rev2 measured transmission phase from Ports 2 – 9 to Port one showing good phase stability.

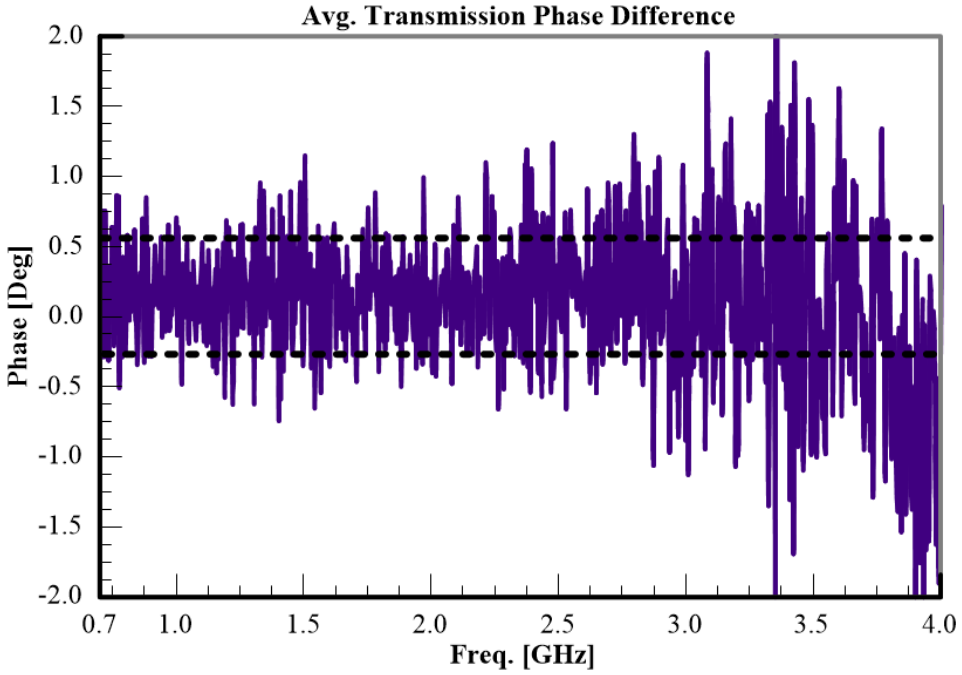


Fig. 112. Rev2 combiner measured average transmission phase difference from Ports 2 – 9 to Port one.

Fig. 113 and Fig. 114 display phase information for specific frequencies. Fig. 113 shows a 2^{o} variation between the maximum and minimum phase. Fig. 114 shows phase variance remains constant. Table XVIII lists the transmission path mean phase standard deviation in 200 MHz steps. The standard deviation varies from 0.39^{o} to 1.38^{o}.

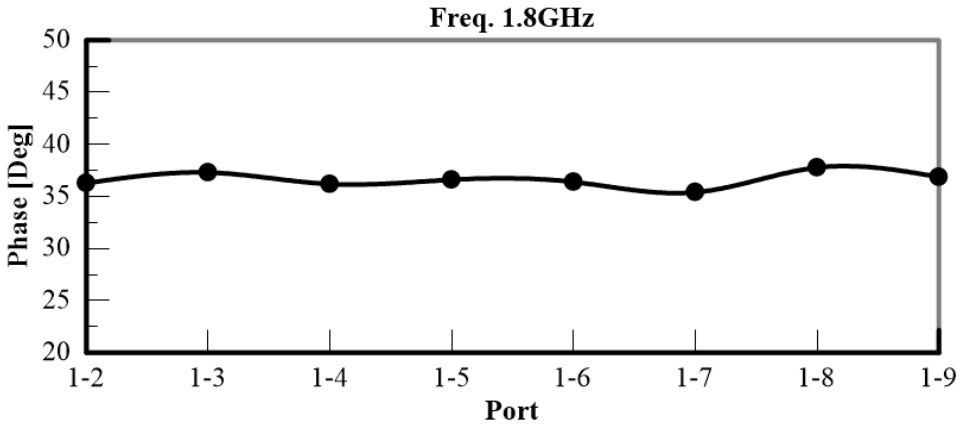


Fig. 113. Rev2 measured 1.8 GHz transmission phase from Ports 2 – 9 to Port one.

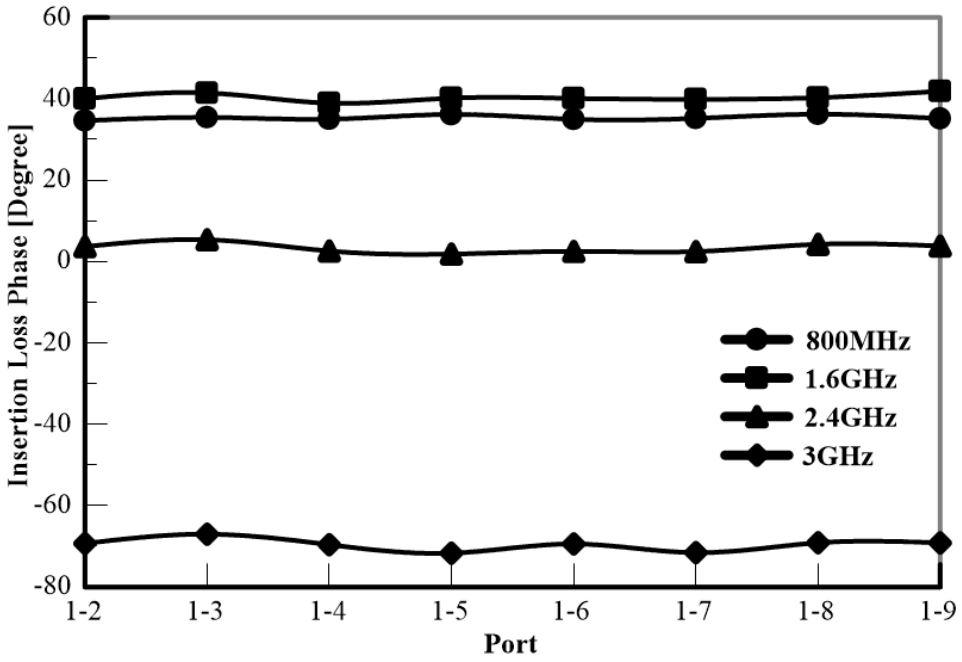


Fig. 114. Rev2 measured transmission phase from Ports 2 – 9 to Port one.

TABLE XVIII
REV2 PHASE ERROR

Freq. [GHz]	Mean	σ [+/- Deg.]
0.8	35.34	0.53
1.0	39.05	0.99
1.2	42.43	0.39
1.4	40.50	1.00
1.6	40.50	0.87
1.8	36.60	0.68
2.0	28.85	0.76
2.2	18.12	1.09
2.4	3.32	1.09
2.6	-15.54	0.78
2.8	-42.32	0.77
3.0	-69.60	1.38

Fig. 115 shows the three level combiner insertion loss higher than 9dB. A -1.43dB mean isertion loss covers 0.8 – 3 GHz and a -1.93dB mean isertion loss covers 0.5 – 3.28 GHz. An average 0.62dB loss for one transmission path over 0.7 – 4.0 GHz.

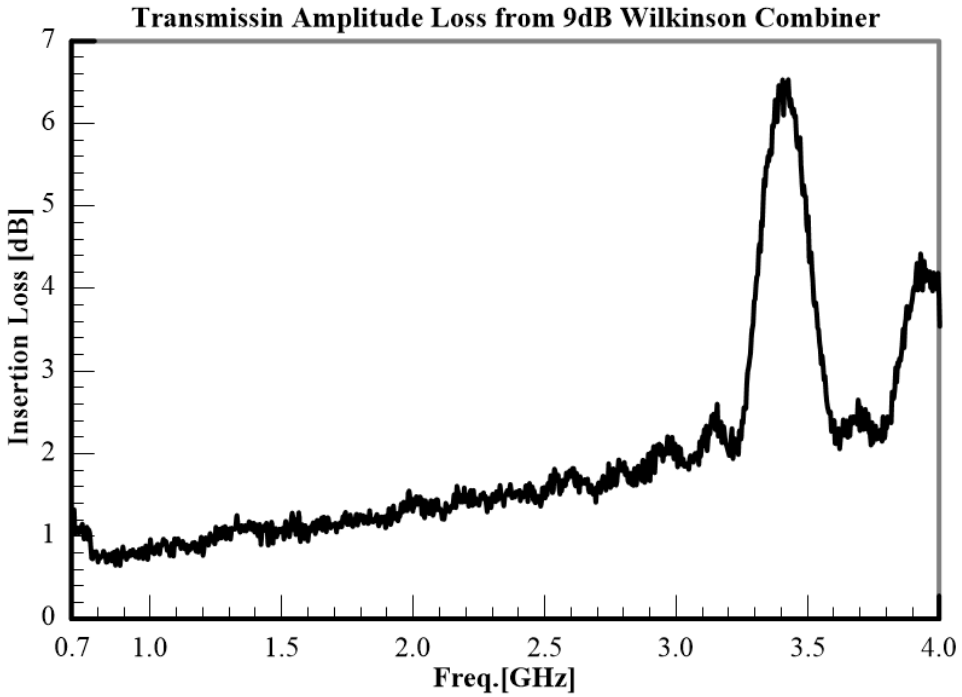


Fig. 115. Rev2 combiner average insertion loss measured from Ports 2 – 9 to Port one.

Fig. 116 shows static frequency insertion loss per port. The insertion loss variance between 800 MHz and 3.0 GHz mostly agrees with the 0.62dB loss variation per transmission path. The valley for 2.4 GHz comes from etching variations influencing stripline impedance, losses from resistor size error, and layer adhesive. Fabrication inconsistency influence stripline length and impedance. The insertion loss swing measures ± 0.78dB from maximum (-11.21dB) to minimum (-9.65dB).

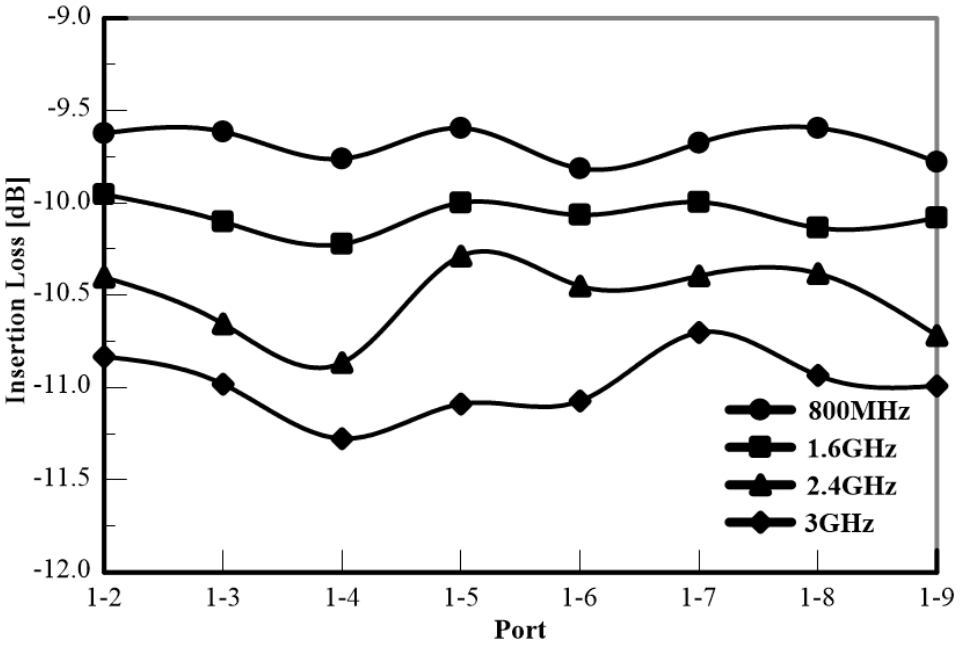


Fig. 116. Rev2 measured insertion loss from Ports 2 – 9 to Port one.

Fig. 117 shows static frequency isolation by port and different port combinations validate consistency. When ports branch off the same combiner, see 23, 45, and 67 the isolation reduces. The 3.0 GHz frequency begins isolation reduction to its 3.28GHz minimum.

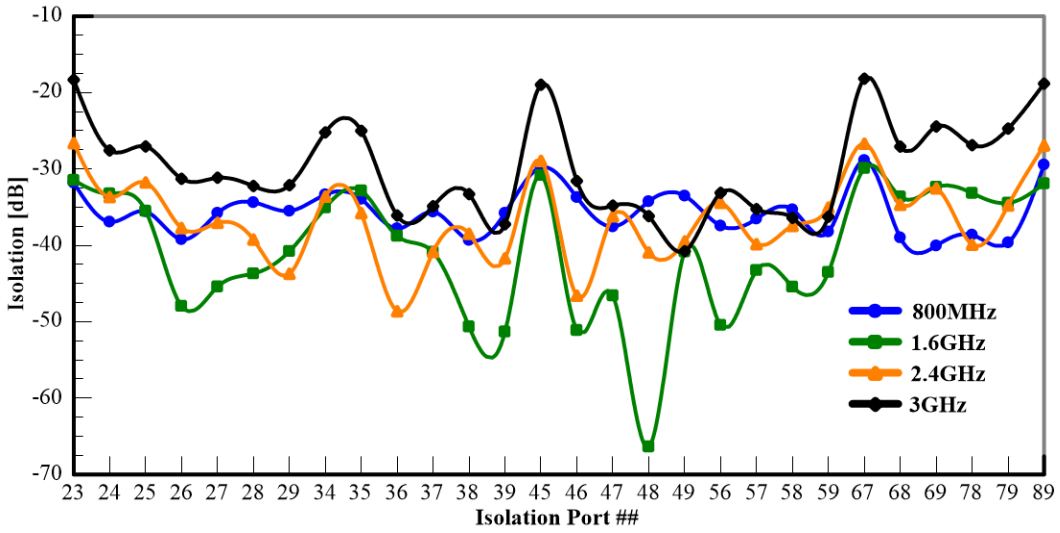


Fig. 117. Rev2 isolation static frequencies measured between Ports 2 – 9.

Fig. 118 displays the average amplitude difference traversing all signal transmission paths. Amplitude imbalance takes the transmission magnitude (S_{21}) and subtracts S_{31}. I calculated amplitude imbalance for 28 combinations then averaged the results together. Non-averaged data presents a 1.13dB max amplitude difference and an approximate 0dB minimum providing a ± 0.57dB amplitude variation. Rev2 provides a ± 0.41dB amplitude imbalance over 0.8 – 3 GHz and ± 0.41dB imbalance over 0.5 – 3.28 GHz. Rev2 provides an average amplitude difference less than 0.18dB between 500 MHz and 4.0 GHz.

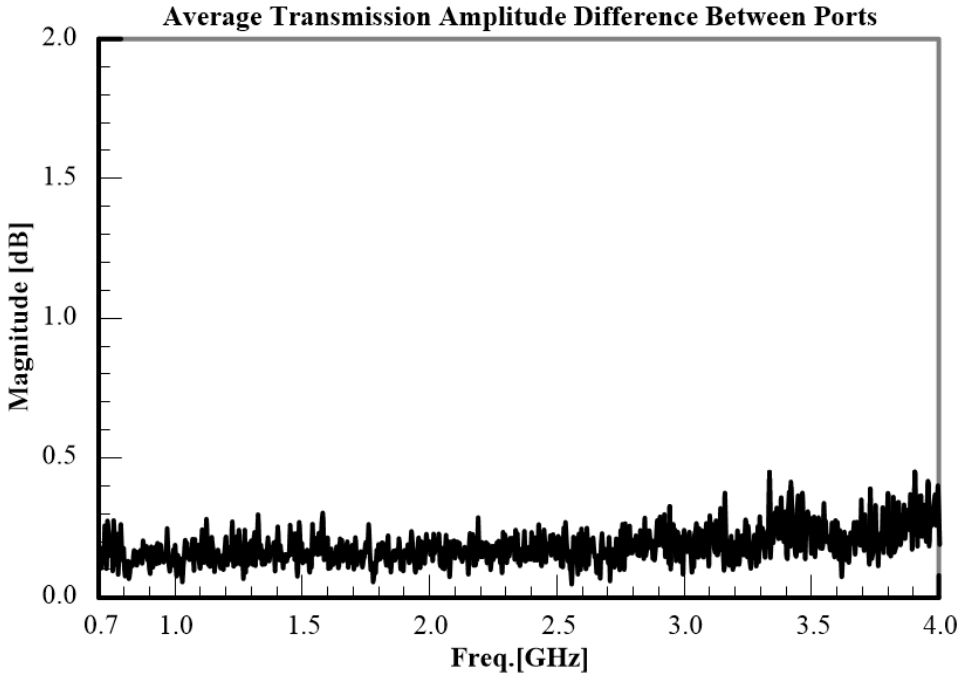


Fig. 118. Rev2 combiner amplitude imbalance measured from Ports 2 – 9 to Port one.

Fig. 119 displays the signal combining efficiency. The combiner possess an average single path loss of 0.62dB from Port one to Ports 2 – 9. Fig. 119 shows a 70% initial efficiency for eight combined signals assuming 0.6dB loss. Fig. 53 does not consider loss frequency response. Fig. 119 shows a 78% efficiency fluctuating between 86% and 64% and plummets. Electrically longer transmission paths steadily decline efficiency. Additional efficiency loss from compared with Fig. 106 originates from the HFSS model not including resistor losses, layer adhesive loss, and etching error.

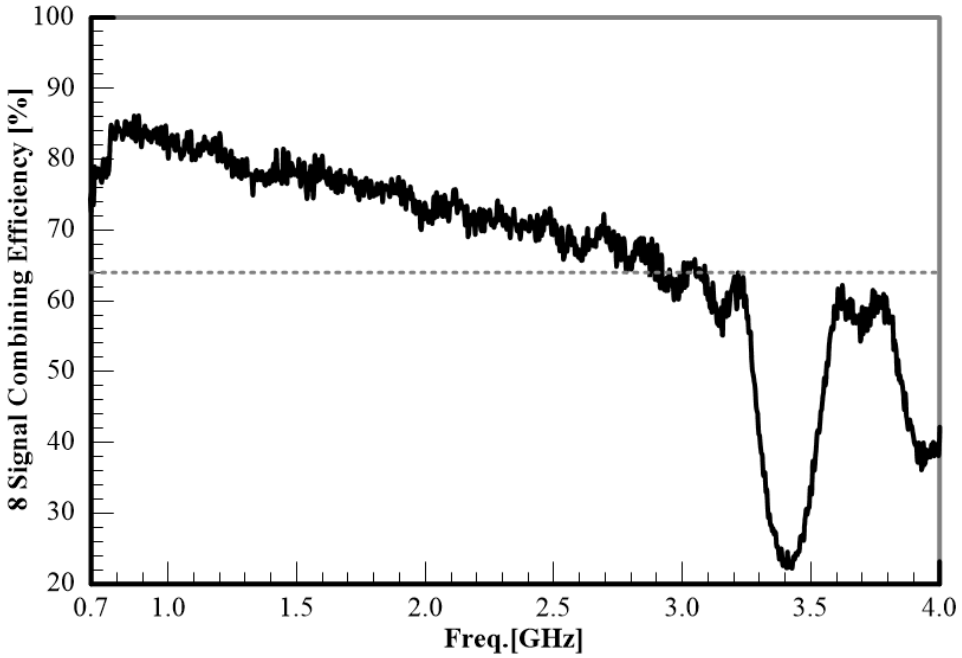


Fig. 119. Rev2 combiner efficiency extracted from averaged power transmitted from Ports 2 – 9 to Port one.

Examining the measured results for the Rev2 combiner compared to the set design standards for the design shows reasonable agreement.

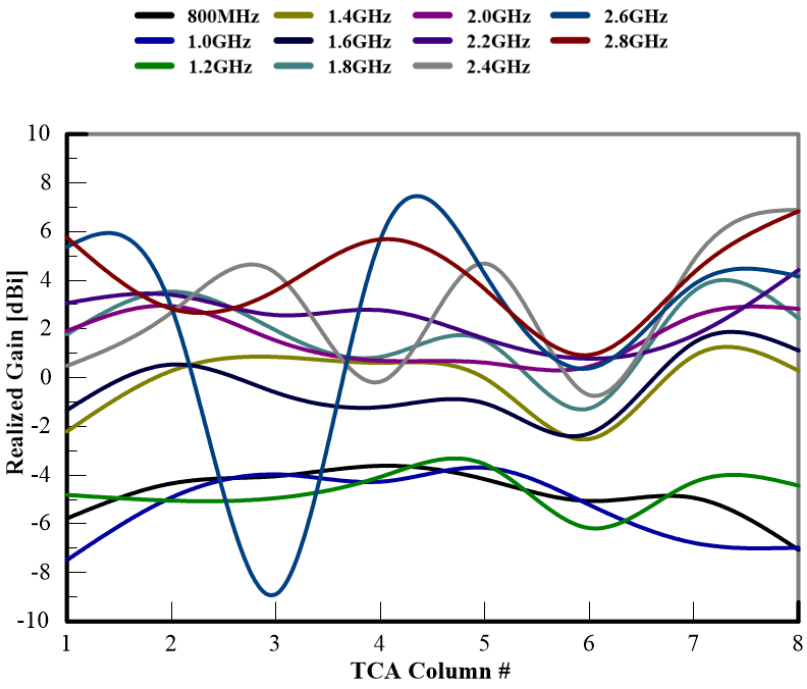
A. 3.75:1 Minimum Bandwidth (Yes)
B. -15dB Minimum Port one Return Loss (No)
C. -20dB Minimum Ports 2 – 9 Return Loss (Yes)
D. 1.5:1 VSWR Port one (No)
E. 1.4:1 VSWR Ports 2 – 9 (Yes)
F. 1.5dB ± 0.8dB Insertion Loss (Yes)
G. ± 0.5dB Amplitude Imbalance (Yes)
H. ± 4^{o} Phase Unbalance (Yes)
I. Transmission Phase Standard Deviation ≤ ± 1.5^{o} (Yes)
J. -16dB Minimum Isolation (Yes)

The Rev2 input impedance varied from design standards due to fluctuations not easily accounted in analytical design and electromagnetic simulation. These fluctuations include dielectric homogeneity changes due to layer adhesive and slurry, LC resonances

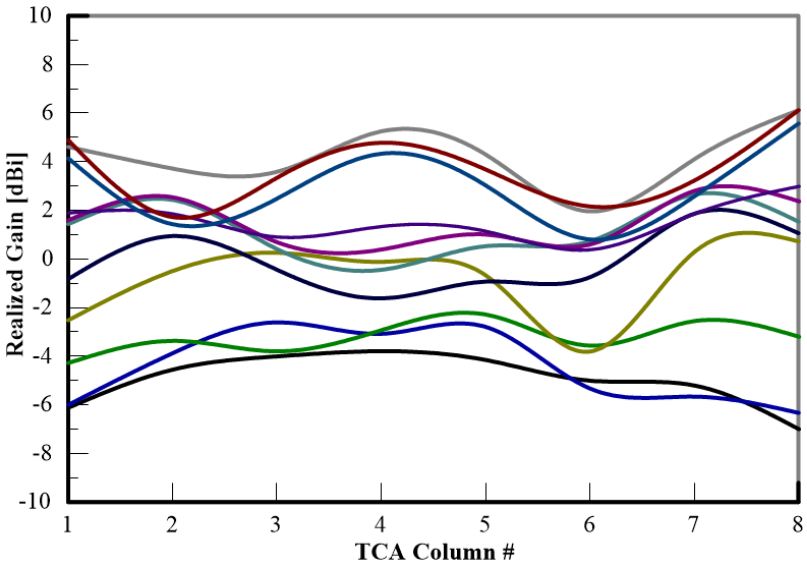
from isolation resistor pads, stripline width and length manufacturing tolerance variance, and isolation resistor error from OhmegaPly® processing.

IV.I. Rev2 Impact on TCA

All eight columns sum to form the main pattern. I took broadside measurements for each column to check for combiner drop out. A 50Ω load terminated columns not measured. Fig. 120 (a) and (b) demonstrate improving the combiner design increases TCA column gain. The Rev2 combiner removed the deep gain sags and fluctuations observed in Fig. 120 (a). An experimental 8x8 TCA provided by Bit Systems assisted combiner integration measurements. The antenna possess a problem with column six, however examining the problem rests outside the combiner investigation.



(a)



(b)

Fig. 120. TCA column broadside gain measurements showing differences between integrating the Rev1 (a) and Rev2 (b) combiners.

CHAPTER V

FUTURE RESEARCH

The Wilkinson combiner presented in Fig. 11 possesses narrow input impedance compared to its output impedance. A method to balance the impedance bandwidth to offer nearly an octave (8.0 GHz) bandwidth requires adding a quarter-wave transformer between the 50Ω line and the transmission line split [52] to compensate for the impedance unbalance. A 42Ω quarter-wave transformer bridges the 50Ω line connecting two $\sqrt{2}Z_0\Omega$ quarter-wave transmission lines and isolation resistor $\left(2Z_0\Omega\right)$ positioned between ports two and three.

Rather than chamfering the 90^o bends, curve and blend the bends to reduce corner inductance and capacitance. The blended curves and bends will improve insertion loss, return loss, and reduce transmission phase error. Smoothing all step discontinuities from each combiner stage reduces excess capacitance and inductance from fringing fields by adding transitions, thus improving impedance, transmission, and phase. Improve stripline T-junction optimization to improve impedance match and reflection coefficient phase.

Horst [77] presented several methods to reduce LC resonances from the resistor pads. Implementing these methods will help strengthen the WPC impedance match. New OhmegePly® thin film modeling needed to increase advantage and disadvantage understanding.

A method to reduce size and improve performance involves integrating a low pass filter [65 and 115 – 118]. The filter suppresses WPC harmonics. The harmonic suppression reduces power used by the harmonics and improves bandwidth, isolation loss, and return loss.

CHAPTER VI

CONCLUSION

Chapter II discussed communication history, bandwidth, and array background information. Chapter II Sections II.G and II.H discussed some fundamental network mathematics on designing a two port Wilkinson combiner and reviewed even and odd mode analysis. Chapter II Section II.I provided an overview of Wilkinson power combiner advancement chronologically through seventeen published journal articles and conference proceedings. Topics covered EBG, varactors, LTCC, coupled transmission lines, harmonic filtering, and artificial transmission lines. Table XIX provides a design behavior summary over the reviewed seventeen published articles.

TABLE XIX
PEER-REVIEWED PAPERS COMPARING WILKINSON POWER COMBINERS TO REV2 COMBINER

Reference	Frequency [GHz]	Bandwidth	Area [mm^2]	RL [dB]	IL [dB]	Amp. Imbal. [dB]	Phase Unbal.	Min. Iso. [dB]
Goodman (1968) [59]	1-12.4	12:1	130mm	-19	-3 ± 0.75	± 0.1	-	-20
Sun (2004) [60]	15-45	3:1	0.45	-15	-5	-	-	-15
Woo (2005) [61]	1.5	-	-	-40	-3.3	-	-	-
Wentzel (2006) [62]	0.3-2.8	9.3:1	-	-10	-3 ± 0.25	-	-	-8
Lee (2006) [63]	3-5.5	1.83:1	17	-	-5.5	-	-	-9
Seman (2007) [64]	3.1-10.6	3.4:1	560	-12.5	-3.5 ± 0.2	-	± 3°	-
Li (2007) [65]	1.5	-	295.6	-36	-3.16	-	-	-30
Abbosh (2008) [66]	4-8	2:1	750	-10	-3.4 ± 0.2	± 0.2	± 2°	-10
Kawai (2009) [67]	0.85-1.2	1.4:1	345	-15	-3.5	-	± 3°	-20
Chieh (2009) [68]	2-18	9:1	-	-10	-3.5 ± 1.5	± 0.46	-	-11
Tang (2010) [69]	0.71-0.99	1.4:1	32	-10	-3.5 +/-0.2	-	-	-20
Xu (2012) [70]	2-8	4:1	930	-18	-3.85 ± 0.82	-	-	-20
He (2012) [73]	0.81-1.14	1.4:1	399	-10	-3.3	-	-	-20
Pribawa (2012) [74]	1-2	2:1	9000	-12.3	-7.8	-	-	-12.8
*Liu (2013) [75]	0.5-1.5	3:1	625	-8.5	-11.8 ± 0.4	± 0.4	± 3°	-15
Trenz (2014) [76]	2-28	14:1	30	-10	-3.3 ± 0.6	-	-	-10
Ahmed (2015) [78]	1-7	7:1	2200	-10	-3 ± 0.5	± 0.2	± 2°	-15
***Rev2**	**0.8–3**	**3.75:1**	**258**	**-12**	**-10.43 ± 0.78**	**± 0.41**	**± 2.0°**	**-18**

*8:1 Combiner Design

Chapter III presented TCA operation problems originating from a problematic prior Wilkinson combiner design attempt. Results showed gain loss due to impedance matching problems and improper current handling between laminate layers causing transmission loss and RF blocks. Rev1 brief design discussion and measured results provided an in-depth analysis on why it failed.

Chapter IV introduced designing an UWB Wilkinson power combiner for integrating with UWB hardware and TCA. Sections IV.A – IV.E discussed UWB WPC design requirements. Measurements provided from a Mini-Circuit eight port to one port combiner demonstrated WPC operation standards for a successful WPC design. Examining signal combining efficiency provided minimum path loss. Interconnecting transmission lines traversing multiple laminate layers required proper current handling because interconnects influence impedance, transmission, and isolation. Integrating a via picket fence improves port isolation and reduces propagating parallel plate modes. A fabricated test circuits verified interconnect and picket fence design methods and concerns. Section IV.F provided an UWB combiner design discussion for CAD modeling, material selection, and optimized dimensions. The compact Rev2 WPC required designing coupling between parallel strip lines. Coupling discussion included design graphs, plots, and equations for factoring fringing capacitance, odd and even mode impedance, and improving signal isolation, transmission, and impedance through coupling. Laminate thermal and power properties revealed breakdown conditions. OhmegePly® thin film material formed the isolation resistors. Stripline transition

methods improved impedance. Lastly, Sections IV.G and IV.H discussed Rev2 simulations and measured results.

The condensed Rev2 four stage design consumes 0.4in^2 (258mm^2) surface area and weights 1.5oz (42.5g). The Rev2 interfaces with the experimental antenna through SMP snap connectors. The Rev2 covers 500 MHz to 3.28 GHz and provides a 6.56:1 bandwidth. Table XX compares the Mini-Circuit, Rev1, and Rev2 measurements alongside my operation standards. Table XIX compares the Rev2 design with seventeen peer-reviewed literature measurements. A literature review reveals no prior publication implementing an UWB multi-layer stripline WPC using OhmegaPly® thin film isolation resistors. Peer-reviewed publications through December 2015 express no multi-port WPC designs for TCA integration.

TABLE XX
WILKINSON COMBINER MEASUREMENT COMPARISON

Source	Design Std.	Mini-Circuit [83]	Rev1	**Rev2 Std.**	**Rev2 Max**
Freq. [GHz]	0.8 – 3	0.6 - 3.6	0.8 – 1, 1.5 – 2.4, 2.7 – 4	**0.8 – 3**	**0.5 – 3.28**
Bandwidth	3.75:1	6:1	1.25:1	**3.75:1**	**6.56:1**
Min. RL P1 [dB]	-15	-14	-2	**-11.74**	**-7.8**
Min. RL P2 – 9 [dB]	-20	-19	-12	**-21.4**	**-18.1**
VSWR P1	1.5:1	1.5:1	3.5:1	**1.7:1**	**2.4:1**
VSWR P2 - 9	1.4:1	1.4:1	1.7:1	**1.2:1**	**1.3:1**
IL [dB]	1.5 ± 0.8	1.5 ± 0.6	1.8 ± 0.64	**1.43 ± 0.78**	**1.93 ± 1.28**
Amp. Imbalance [dB]	± 0.5	± 0.5	± 0.85	**± 0.41**	**± 0.52**
Phase Unbalance	± 4.0°	± 4.0°	± 12.5°	**± 2.0°**	**± 4.0°**
Max Phase Std. Dev.	≤ ± 1.5°	± 1.54°	± 79.17°	**± 1.38°**	**± 1.89°**
Min. Iso. [dB]	-16	-16.0	-17	**-17.9**	**-12.2**

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