TWO-PHASE INVERTER WITH ACTIVE DECOUPLING

An Undergraduate Research Scholars Thesis

by

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Submitted to the Undergraduate Research Scholars program at
Texas A&M University
in partial fulfillment of the requirements for the designation as an

UNDERGRADUATE RESEARCH SCHOLAR

Approved by Research Advisor: Dr. Prasad N. Enjeti

May 2018

Major: Electrical Engineering

TABLE OF CONTENTS

ABSTRACT

Two-Phase Inverter with Active Decoupling

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This thesis proposes a novel topology for active decoupling in a two-phase inverter circuit to reduce converter size, improve converter lifetime, and increase efficiency. The two-phase output is particularly significant for renewable energy sources because offering a two-phase output will allow an inverter to connect to the grid and maintain the high efficiency provided by active decoupling. The mathematical model of the circuit was constructed and used to implement a proportional controller. The circuit schematic and controller block diagram were built, simulated, and tested using PLECS simulation software. The presented topology significantly reduces the size of the DC-Link capacitor required to stabilize the DC input voltage. The reduction in the size of the capacitor also allows a higher quality thin-film capacitor to implemented, which will increase the lifetime of the system. A single additional leg handles unbalanced loads, high power factor output, and non-linear output current. This inverter can supply power to houses and buildings without needing to connect to the grid, so off-grid solar systems can easily be setup without the need for complicated and expensive micro-inverter systems.

DEDICATION

This thesis is dedicated to my family and the supportive network that I have found in the power electronics division at Texas A&M University. I would also like to thank Dr. Enjeti for his generous support and for the guidance he has shown me throughout this process. Finally, I would like to thank my partner in this project, Sinan Al-Obaidi, for his hard work and guidance on this project.

NOMENCLATURE

GaN	Gallium Nitride
PWM	Pulse Width Modulation
V_{AN}	Voltage from Node A to Node N
V_{BN}	Voltage from Node B to Node N
V_{CN}	Voltage from Node C to Node N
Φ_A	Phase Angle of I_A
Φ_B	Phase Angle of I_B
θ_α	Phase Angle of V_α
θ_β	Phase Angle of V_β
PI	Porportional-Integral

CHAPTER I

INTRODUCTION

Solar Applications

Solar power installations have been expanding faster than any other source of power production and in the last quarter of 2016 had the highest amount of new energy addition, in gigawatts, of any energy source [1]. The solar market has grown rapidly and consistently in the last decade averaging 59% growth over the last ten years [2]. The growth in the popularity of solar power can be largely attributed to the rapidly declining price per kilowatt cost of solar panels as well as incentives from governments encouraging the use of "green energy". The cost of solar installations has fallen by 70% in the past decade, which has spurred higher consumer adoption of solar power [3]. Due to the increased popularity of solar power, projects on maximizing system efficiency and efficient power conversion for interface with the grid have greatly increased in the last few years [4, 5].

Active Decoupling

To connect solar panels, which produce DC power, with the main power grid, which operates on AC power, a conversion must be made. The converter that does DC-AC conversion is called an inverter. An inverter uses a system of transistors, inductors, and capacitors to generate an AC output that oscillates in the form of sine wave with a specified frequency. An important requirement of the inverter is separating the DC power fed into the converter from the AC power output by the converter. This separation is accomplished through a process called decoupling. Passive decoupling traditionally uses a large capacitor, called a DC-Link capacitor, to block the

AC circulating currents from causing ripples to appear on the DC side of the inverter. This resulted in several drawbacks, such as increased size and cost, which forced circuit designers to use cheaper electrolytic capacitors, which are far less reliable than modern thin-film capacitors and have a shorter lifetime. These drawbacks forced designers to search for an alternative. The answer they found to this problem was active decoupling, which uses pulse width modulation (PWM) schemes and additional circuitry to decrease the necessary size of the DC-Link capacitor. Active decoupling requires a more complex closed-loop control scheme to implement, but can reduce the overall size of the system by using a dedicated capacitor for decoupling, which is much smaller than the DC-Link capacitor required for passive decoupling. A DC-Link capacitor is still necessary to filter out high frequency harmonics, but it will be much smaller than the decoupling capacitor required for the topology.

Gallium Nitride Devices

In power electronics, switching frequency plays an important role in determining the size and efficiency of a topology. The necessary size of filtering components (inductors and capacitors) for an inverter will typically go down in size as the switching frequency increases. Due to this fact, increasing switching frequency is a good thing to make circuits that have a higher "power density" or power processed per unit volume. On a practical level, a trade-off is made between size and efficiency because the non-ideal properties of circuit elements that cause efficiency to decrease typically scale with switching frequency. There are also physical limits to how quickly a transistor can be "switched" on and off, which becomes slower as the current and voltage on the device become higher. Silicon (Si) has historically been the semiconductor material of choice for transistor device designers, but Gallium Nitride (GaN) devices have recently emerged in power

electronics as high power, high switching frequency switches [6]. This is because they can operate at very high voltage and current ratings while still being able to rapidly turn on and off. In addition, the losses across the device itself are much lower than Si devices due to their high turn on and off rate.

Two-Phase Inverters

As solar power increases in popularity, more people are seeking to move "off-grid" or relying entirely on solar power instead of utility electricity. One requirement of this type of system is that the electrical output of the solar system must mimic grid output to connect with home electrical systems. Two-phase inverters exactly provide this function and are in fact the only type of inverter that can do so. One drawback of a central inverter system is that high voltage and current ratings are necessary on the converter. In addition to this, no active decoupling method currently exists, so the system is bulky and unreliable. The system also has a short lifetime because the electrolytic capacitor needed for the converter is only expected to last 10,000 hours, which is about 3 years of daily use [7]. In comparison, the other components in the system can last for longer than 20 years. Thin film capacitors typically have lifetimes greater than 30 years, but have a much higher cost per unit volume, which means the capacitance value must be very small to viably use thin film capacitors.

CHAPTER II

MATHEMATICAL MODELING

The feature of interest for the mathematical modeling of the circuit, shown in figure 1, is the reactive power generated by the load of the inverter. This load can be connected across the three terminals of the device in any fashion and the mathematical modeling of the circuit should hold. The goals of modeling the circuit are to size parameters, to determine their operating limits, and to design the logic behind the proportional controller. The mathematical derivation of the circuit is merely a preliminary design a will be changed after simulation results are observed to more reasonably model the function of the circuit.

Phase Leg Derivations

The primary phase legs of the circuit are phase A and phase B, so the voltage across phase A will be given a phase angle of zero. This will serve as a reference to the other sinusoidal wave functions to be measured from. Additionally, the voltage magnitudes are measured with from the neutral leg (N) as reference, meaning the AC voltage of the neutral leg should always be zero. The voltages and currents for the primary phases (A and B) are derived below.

$$V_{AN} = V_{AN,max}\sin(\omega t) \tag{1}$$

$$V_{BN} = -V_{AN,max}\sin(\omega t) \tag{2}$$

$$V_{AB} = 2V_{AN,max}\sin(\omega t) = V_{AN} - V_{BN} \tag{3}$$

$$i_A = I_{A,max}\sin(\omega t + \phi_A) \tag{4}$$

$$i_B = I_{B,max}\sin(\omega t + \pi + \phi_B) \tag{5}$$

The final phase of the circuit is the balancing or compensation leg (C), which is also measured with reference to N. This leg must compensate for both primary phases and therefore is represented as the addition of two voltage signals, V_α and V_β, which will compensate for the reactive power of phase A and B respectively. The impedance of the load is largely capacitive, but also has an inductive component. The inductive component should account for less than 1% of the total impedance of leg C and therefore the load can be approximated as entirely capacitive. The current through this leg can then be found as the product of the inverse of the load impedance and the voltage across the load.

$$V_{CN} = V_\alpha \sin(\omega t + \theta_\alpha) - V_\beta \sin(\omega t + \theta_\beta) \tag{6}$$

$$i_{CD} = I_\alpha \sin\left(\omega t + \theta_\alpha - \frac{\pi}{2}\right) - I_\beta \sin\left(\omega t + \theta_\beta - \frac{\pi}{2}\right) \tag{7}$$

$$I_\alpha \approx \omega C V_\alpha \quad I_\beta \approx \omega C V_\beta \tag{8}$$

Because the feature of interest for this circuit is the reactive power generated by the load of the circuit, only the reactive power will be considered for the mathematical model. Additionally, leg C drives an entirely reactive load, so there will not be any real power generated by the compensating load.

$$P_{AN} = -\frac{V_{AN} I_A}{2} \cos(2\omega t + \phi_A) \text{ (reactive)} \tag{9}$$

$$P_{BN} = -\frac{V_{BN} I_B}{2} \cos(2\omega t + \phi_B) \text{ (reactive)} \tag{10}$$

$$P_{AB} = -P_{AN} - P_{BN} \tag{11}$$

$$P_{CN} = \frac{\omega C V_\alpha^2}{2}\cos\left(2\omega t + 2\theta_\alpha - \frac{\pi}{2}\right) + \frac{\omega C V_\beta^2}{2}\cos\left(2\omega t + 2\theta_\beta - \frac{\pi}{2}\right)$$
$$+ \frac{2\omega C V_\alpha V_\beta}{2}\cos\left(2\omega t + \theta_\alpha + \theta_\beta - \frac{\pi}{2}\right) \quad (12)$$

To cancel each other, the reactive power of P_{AB} and P_{CN} must be equal and opposite. To accomplish this, the power equations are solved algebraically and the following results are found.

$$\theta_\alpha = \frac{\phi_A}{2} + \frac{\pi}{4} \quad (13)$$

$$\theta_\beta = \frac{\phi_B}{2} + \frac{\pi}{4} \quad (14)$$

$$V_\alpha = \sqrt{\frac{V_{AN} I_{A,max}\sqrt{\cos(\theta_\alpha - \theta_\beta)}}{(1+\frac{I_{B,max}}{I_{A,max}})\omega C}} \quad (15)$$

$$V_\beta = \sqrt{\frac{V_{AN} I_{B,max}\sqrt{\cos(\theta_\beta - \theta_\alpha)}}{(1+\frac{I_{A,max}}{I_{B,max}})\omega C}} \quad (16)$$

The magnitudes of each of the components of V_{CN} are dependent on the magnitude and phase of both output currents. This indicates that if the values of one component change, the other will likely change as well.

Design Example

A design example for the proposed system shown in Figure 1 at 2 kW is introduced with specifications in Table 1. An important observation about the topology is that the compensation leg is attached to the neutral leg. This means that the maximum voltage of leg C cannot be any

higher than half of the maximum DC voltage. To compensate for this difference in voltage, the current of the compensating leg must be twice as large as the current in the output legs to match the reactive power of both of the output phases. The components of the converter must be able to function under all conditions, so the worst-case scenario must be found and the minimum size of the components will be based on that figure. In the case of the compensating leg, the worst-case scenario will be at maximum current and voltage across the capacitor. The worst-case voltage will be half of the worst-case voltage for the components at the output because of the DC voltage limitation discussed above. The capacitor must be sized so that at the maximum possible value of V_{CN} is not greater than $V_{AN,max}$.

$$C_{ad} = \frac{V_{an,max}(I_{a,max}+I_{b,max})}{\omega V_{cn,max}^2} \tag{17}$$

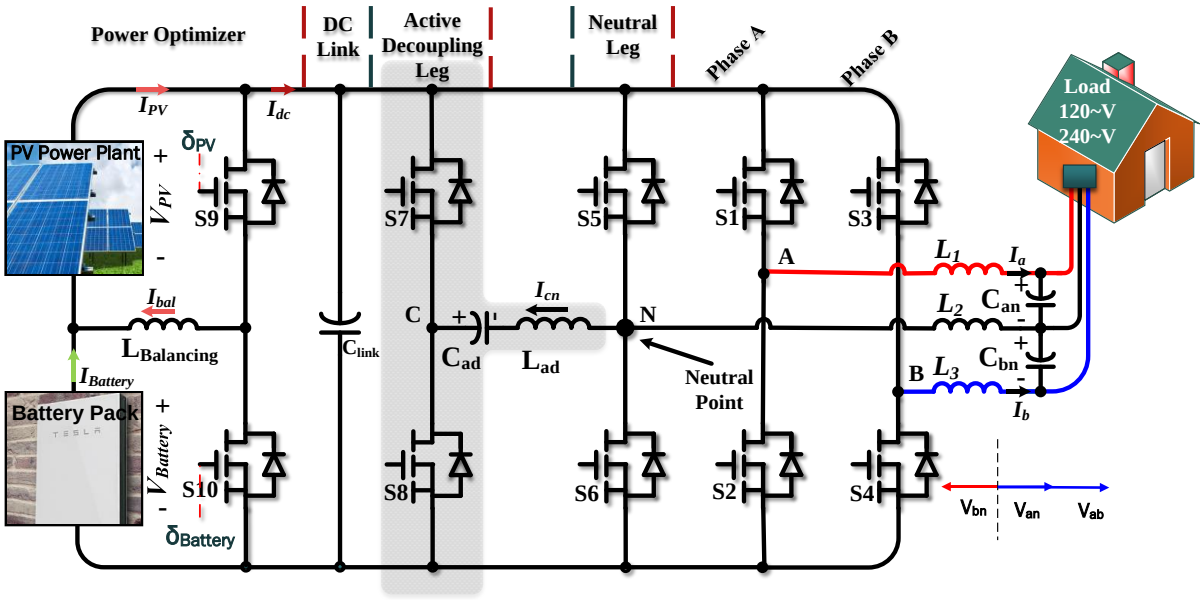

Figure 1. Proposed Converter Circuit Topology.

Table 1. Specification for design example for dual phase four leg inverter with active decoupling and integrated power optimizer.

Design Parameters	
Power Rating	2 kW
Switching(f_{sw})/Output Frequency(f_{out})	100 kHz / 60 Hz
DC Bus Voltage	400 V_{DC}
$V_{an,max}$ / $V_{bn,max}$ / $V_{ab,max}$	120 V_{rms} / 120 V_{rms} / 240 V_{rms}
Inductor Current Ripple (ΔI_L)	20% of Avg.
LC Filter Cutoff Frequency	$f_{sw}/20$
C_{link}	50 μF (for <1% input voltage ripple)

Equation 17 shows the dependence of the size of the decoupling capacitor on the magnitudes of the output current and voltages. $V_{CN,max}$ can now be re-written as a function of $V_{AN,max}$, so the equation simplifies to equation 18.

$$C_{ad} = \frac{(I_{a,max}+I_{b,max})}{\omega V_{an,max}} \tag{18}$$

The decoupling capacitor is designed for the maximum instantaneous power that is needed to match the maximum instantaneous output power using equation 18. The maximum load condition is at full rated load without any phase shift between the phase leg currents. The chosen value is 300 μF.

The remaining circuit elements are the inductors and capacitors that form filters for the currents and voltages in the circuit. The maximum voltage across the capacitors at the output will be twice the voltage across the compensation capacitor due to the DC voltage difference discussed above. The output filters for phase A and B should also be symmetric to make the circuit behave more predictably and to treat loads identically when connected across either load. The inductor and capacitor at the output of phase A and B are arranged to form a LC band-pass filter. This filter should isolate the desired output frequency, which in this case is 60 Hz. The purpose of the LC band-pass filter is to filter out switch harmonics caused by the switching devices of the converter, which produce a relatively high (>> 60 Hz) disturbance. Therefore, it is not necessary for the band-pass filter to have a very tight allowable band, because the filter must only reject the high frequency harmonics of the switching devices.

All output inductors are designed for a 20% current ripple and their selected value is 250 μH using equation 19. The capacitors (C_{an}, C_{bn}) are designed to form an output filter such that all high frequency ripples above 5 kHz ($f_{sw}/20$) are eliminated using equation 20. The chosen value was 5 μF.

$$L_{min} \geq \frac{V_{DC}}{8\Delta I_L f_{sw}} \tag{19}$$

$$C_{min} \geq \frac{1}{\omega^2 L} \tag{20}$$

CHAPTER III

SIMULATION

The circuit design and simulation used PLECS and MATLAB to develop the mathematical models of the circuit and controller and test the functionality of the circuit. MATLAB was used to confirm the mathematical model of the controller and the LC filters developed for the topology. MATLAB was helpful for visualizing the waveforms of the theoretical design equations. PLECS is a full circuit schematic simulation software for power electronics. The controller block diagram was also built in PLECS and simulated with the circuit.

MATLAB

MATLAB was used to model the reactive power generated at the output of the inverter and the control signal needed to cancel this disturbance. Once the mathematical model for the circuit was derived, the equations were input into MATLAB to make use of the simple graphical output. Manipulating values and observing their effect on the performance of the controller was also made much easier. This method was used to determine what assumptions could be made in the calculation of the controller for the circuit. Figure 2 is a MATLAB generated graph of the important power waveforms in the circuit. P_{AB} reflects the total power across both output phases, while P_{CN} shows the "balancing power" that the controller generates in order to achieve the DC resultant input power shown by P_{in}. These graphs were generated by the ideal mathematical models of their voltage and current waveforms which neglect all but the most important influences on their magnitudes. This was helpful for discerning the general behavior of the waveforms, while neglecting smaller harmonic distortions that more complex modeling would include.

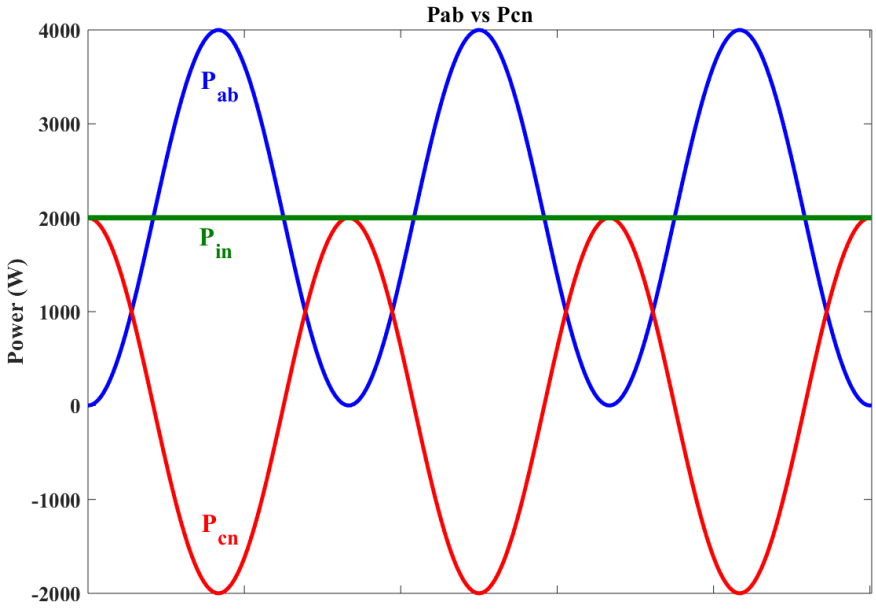

Figure 2. Reactive Output Power vs. Balancing Power and Resultant Input Power.

When designing an LC filter for an inverter circuit, a corner frequency must be chosen that adequately filters the harmonics generated by the switches of the converter. However, the exact corner frequency is somewhat flexible and can change depending on the application. In these instances, it is helpful to graph multiple LC filter frequency responses and observe which best fits the function of the converter. Figure 3 shows a parametric sweep of inductor sizes with frequency responses of each LC filter. This sweep is over a decent size range of inductors that would be reasonable choices for the high power density converter that is being designed. This graph gives a good visualization of the effect of changing inductor size on the performance of the filter. The most desirable filter should have a steep decline between 60 Hz and around 3 kHz and have the physical size of the inductor match the size of the capacitor to yield the highest power density. The inductor size can later be implemented in PLECS and the behavior can be observed in the presence of other components of the circuit for the final decision.

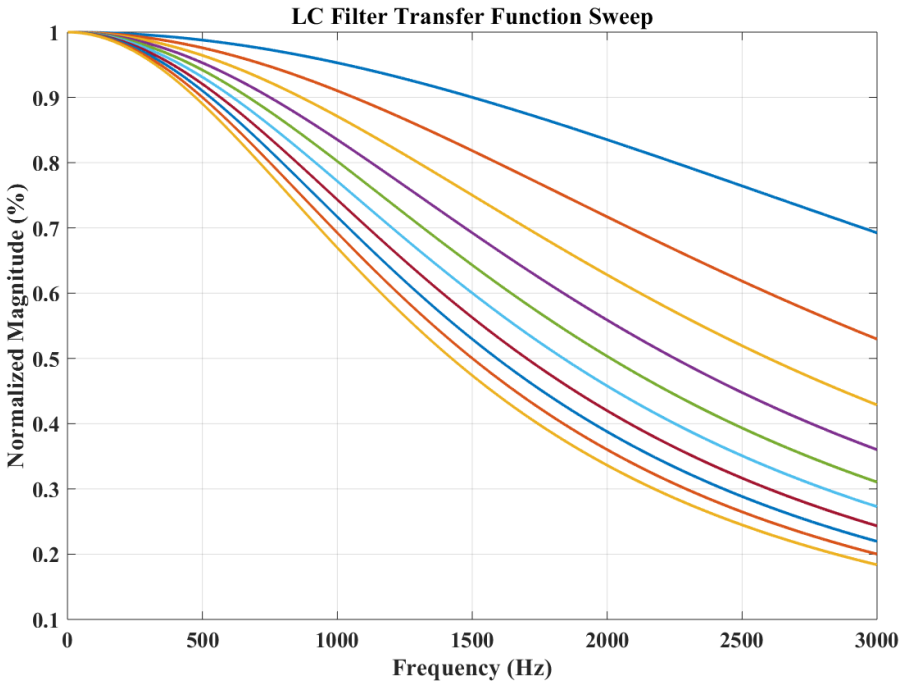

Figure 3. LC Filter Transfer Function LC Value Sweep

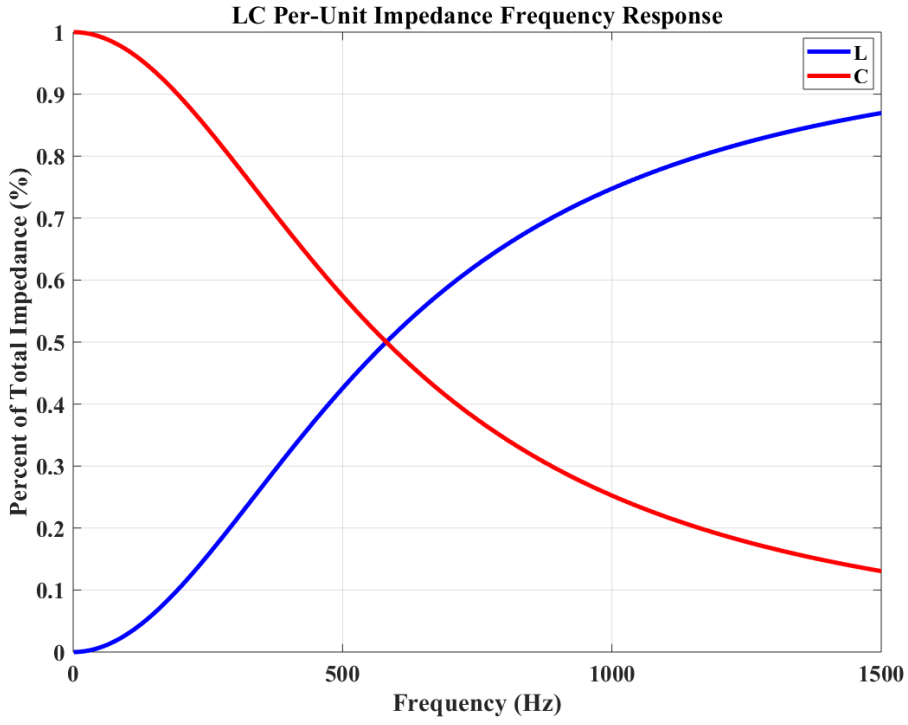

Figure 4. LC Filter Per-Unit Impedance Frequency Response

An important characteristic for the balancing load across V_{CN} is the per-unit impedance of the inductor and capacitor. The per-unit impedance reports the value of the impedance of a component as a percentage of the total impedance. Figure 4 shows the frequency response of the per-unit impedance of the inductor and capacitor across the V_{CN} load. The most important per-unit impedance value for the balancing load is at 60 Hz, which is the reference frequency for the circuit. At this frequency, the per-unit impedance of the inductor is less than 0.3% of the total impedance of the load. This confirms the earlier simplifying assumption that the impedance of the capacitor is much greater than the impedance of the inductor and therefore the inductor's impedance can be ignored when calculating current through the load.

PLECS

PLECS is the circuit schematic simulation software that was used to collect a majority of the results presented in this thesis. The PLECS schematic of the circuit presented can be found in the appendix. PLECS (and similar software like SIMULINK) is suited specifically for power electronics and can simulate the entire circuit schematic including more complex portions omitted from design equations for simplicity. In addition to simulating the circuit, PLECS can also handle control signals for the circuit to implement closed-loop control in simulation.

The calculated component sizes were implemented in the design and the design was run using open-loop control to confirm the soundness of the theory. As in the design example, the load condition was set at 2kVA with no power factor and less than 1% total harmonic distortion. The initial conditions on the components were set to typical resting values for transient analysis and the preliminary test was run.

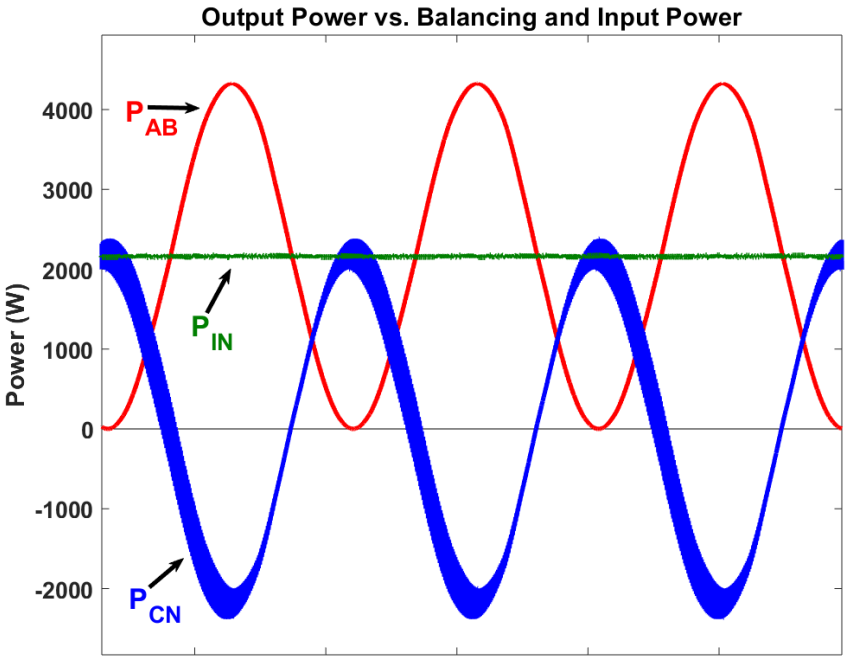

Figure 5. Transient Open-Loop Response of Output Power (P_{AB}), Input Power (P_{AB}), and Balancing Power (P_{CN}) at Full Load and Zero Power Factor

Figure 5 shows the results of the open-loop test confirming the accuracy of the mathematical models developed for the topology. This graph correlates very nicely with the ideal MATLAB graph (Figure 2) shown in the MATLAB subsection and reflects other disturbances from the circuit. The most noticeable is the distortion of the balancing power (P_{CN}) waveform on the falling edge of the sine wave. This distortion is caused by the current ripple on the inductor of the balancing load, but can be ignored because the overall effect is less than 1% ripple on the input current and power. This confirms the assumption made in the mathematical modeling section that the impedance of the inductor can be ignored for calculating the impedance of the balancing leg because it is much smaller than the impedance of the capacitor on the balancing leg.

PLECS includes control circuitry to implement a closed-loop control of the system. However, the timing is ideal, so timing delays needed to be implemented in to reflect the delay of the control system. The component parameters were also ideal, so the function of the circuit is somewhat unrealistic, but several small steps were taken to make the function of the circuit more realistic, such as including timing delays in the control topology and voltage supply input resistance.

PLECS offers other helpful features such as thermal modeling if the thermal characteristics of components are input into the software. Additionally, PLECS is capable of hardware in the loop (HIL) modeling, in which the PLECS box can either test controllers acting as the hardware output or serve as the controller for a scaled-down hardware model. These points were not focus of this project, which was to prove the concept of active decoupling as a method of increasing power density for two-phase inverters. However, these points can be topics of future research on the topology or on the subject of active decoupling for two-phase inverter circuits with active decoupling.

CHAPTER IV

RESULTS

The results for the project thus far have been in simulation on PLECS. Implementation in hardware and further testing will be the topic of future research. The results presented in this thesis are tests of the correctness of the theory behind the topology and the logic of the controller. These are tested by observing the results under various load conditions, an analysis of the transient response of the controller under load stepping, and comparing performance to other topologies.

Load Conditions

The behavior of a converter is often dependent on the load that is driven by the topology. In the case of an inverter, apparent power is the typical method of determining the size of the load of a topology. The RMS output voltage should be fixed for all load conditions, which means for linear loads, the factors that can vary based on load conditions are RMS current and power factor. Linear loads are the common test case for new topologies and the worst case scenarios are the scenarios of interest because they define the operating limits of a topology. The worst case scenario operating conditions are covered and the results are reported in this section as well as graphs displaying the transient operation of the dual-phase output inverter. Nonlinear loads are also discussed and a test case of a rectifier serving a nonlinear load is the subject of the discussion. In all cases, the results of test case are compared to the industry standard of 5% ripple current at the input of the converter. The power at the input is observed and is directly correlated with the input current.

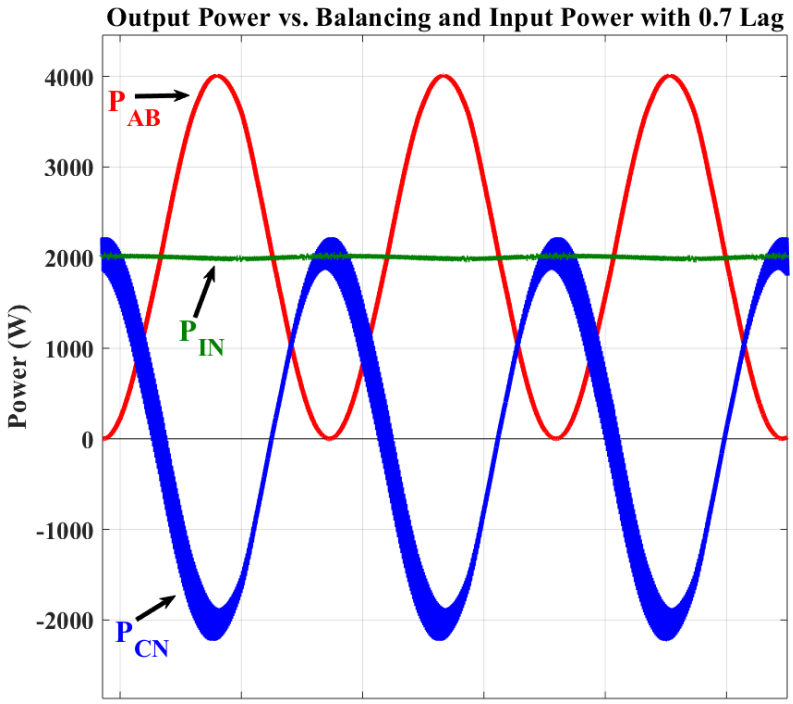

Figure 6. Transient Plot of Output, Input, and Balancing Power with one load at 0.7 lagging power factor.

The industry standard operating limits for power factor are 0.7 lagging and 0.7 leading and the maximum RMS current is defined by the power rating of the converter. The maximum power rating of the inverter that is presented is 2 kVA. Figure 6 shows a transient plot of the input, output, and balancing power in the circuit with one of the loads at a 0.7 lagging power factor. The ripple in the input power is less than 3%, which is well within acceptable limits for the industry standard of less than 5% ripple. The balancing power is well matched with the output reactive power for this condition and does just as well for 0.7 leading power factor, which produces an identical graph to Figure 6. This is because the phase shift between the two output voltages will be identical with 0.7 leading power factor. The difference between the two is that a lagging power factor reflects inductance in the load and a leading power factor reflects capacitance in the load.

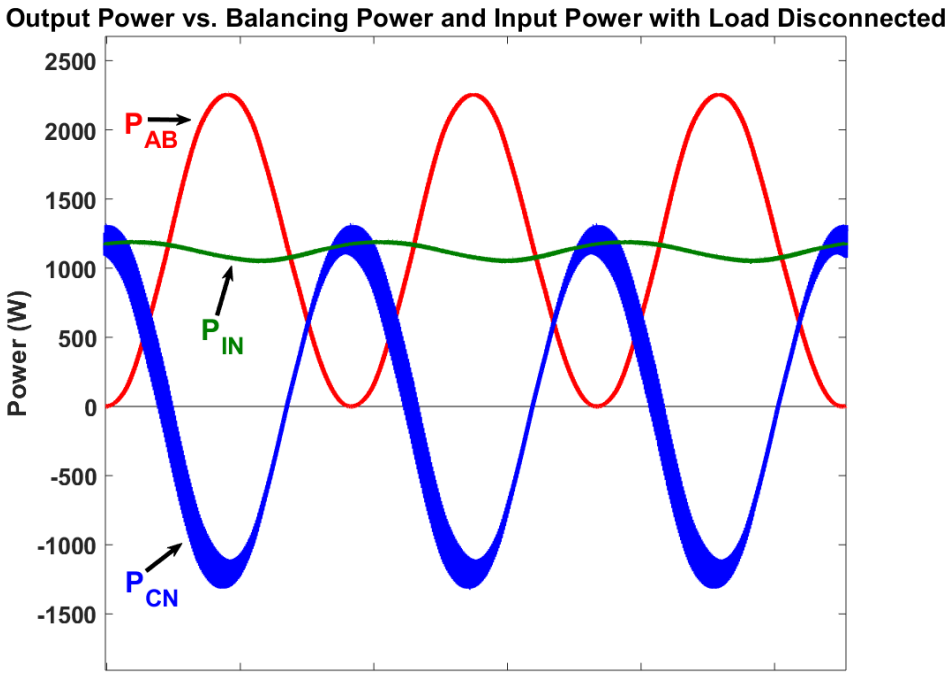

Figure 7. Transient Plot of Output, Input, and Balancing Power with One Load Disconnected and the Other Load at Full Load

One of the most difficult stress tests for a dual-phase output topology is magnitude variation of the outputs of the converter. This is a strenuous test even for a single-phase output converter, which has acceptable limits for how low output power can be. In two-phase output topologies that produce mirrored outputs across both phases struggle with differences between the magnitudes of each phase leg. Figure 7 shows the input, output, and balancing power for a single load disconnected, or at zero load, and the other phase a full load. This is the toughest stress test for a system. The observed input power ripple was 11%, which is above the IEEE standard of 5%. This means the converter should only operate with two loads attached. However, the load variation in magnitude for the converter can go as low as 10% of the rated output power of the inverter while maintaining an input power ripple of less than 5%.

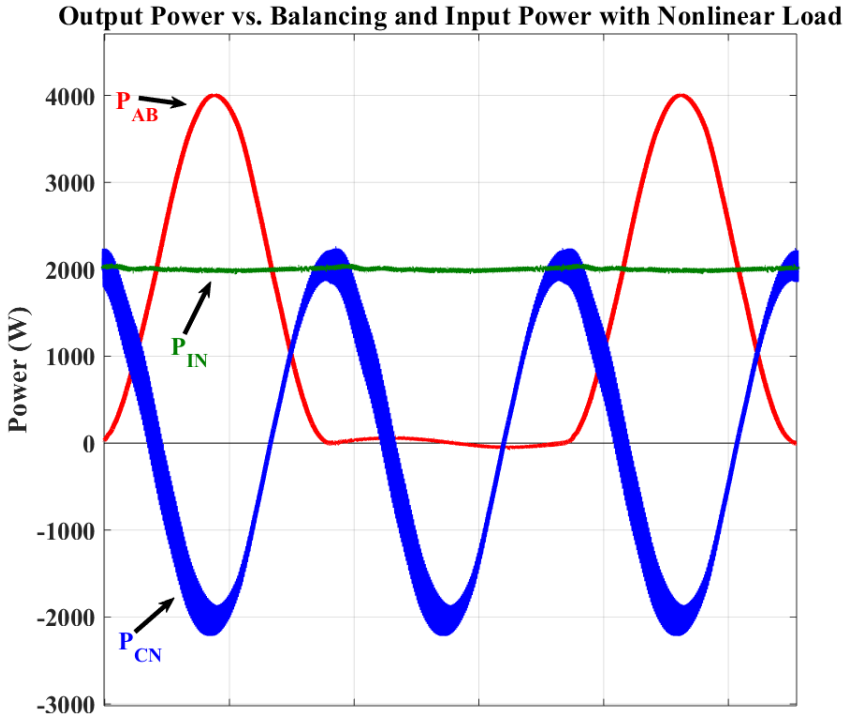

Figure 8. Transient Plot of the Output, Input, and Balancing Power with One Load Connected to a Rectifier with a Small Power Factor Load

Another common load condition is the attachment of a nonlinear load, such as a rectifier to the output of the converter. This causes a discontinuous current to the output of the converter, which can be troublesome for the controller, which reads the two output currents as the main input of the controller. High power factor loads for nonlinear loads are the worst case scenario for the inverter, because they cause large spikes in current for each of the phase legs. This results in a distorted current waveform being fed into the controller of the system, which causes the balancing waveform to be much less accurate. Figure 8 shows the transient waveforms of the output, input, and balancing power with one of the loads connected to a rectifier. There is a small nonlinear disturbance on the input power waveform, but this disturbance is less than 5% of the total input power. The output power reflects the nonlinearity of the output load.

Transient Response

A significant test of a closed-loop controller is the transient response of the controller to load stepping. Load stepping is the sudden change of the output impedance of one or more of the loads within some reasonable level. Both levels, starting and ending, should be within acceptable operating limits to observe the behavior between the two points. There are several ways to describe the behavior of the transient response between the two steady-state points, such as the speed at which the sign approaches the new value, which is typically given by rise time. Another is overshoot, which is how much the signal goes above the value that it is attempting to reach. These values show the quality of the controller and are typically not desirable values within a proportional controller, which was implemented for this project. Nevertheless, these values were approximated for the dual-phase output controller presented and several graphs are shown to analyze the response and lay the groundwork for developing a more sophisticated second order, closed-loop feedback controller.

The discussion of the controller starts with the same three values that have defined the discussion of the topology thus far, the input, output, and balancing power of the inverter. Figure 9 shows the transient response of particularly the input power to the load stepping of the one of the output phase impedances from half load to full load. This doubles the RMS current to the output phase and raises the power to the whole system to 133% of its previous value. This is a drastic step and gives a good step response from the circuit by which the function of the proportional controller can be tested. The rise time of the controller is decent and adjusts to the new power value within a single reference frequency cycle. The larger concern is the harmonic ringing of the controller. One thing to note, is that the oscillation of the input power after the transient response is caused by two sources. The first is the oscillation from the controller due to

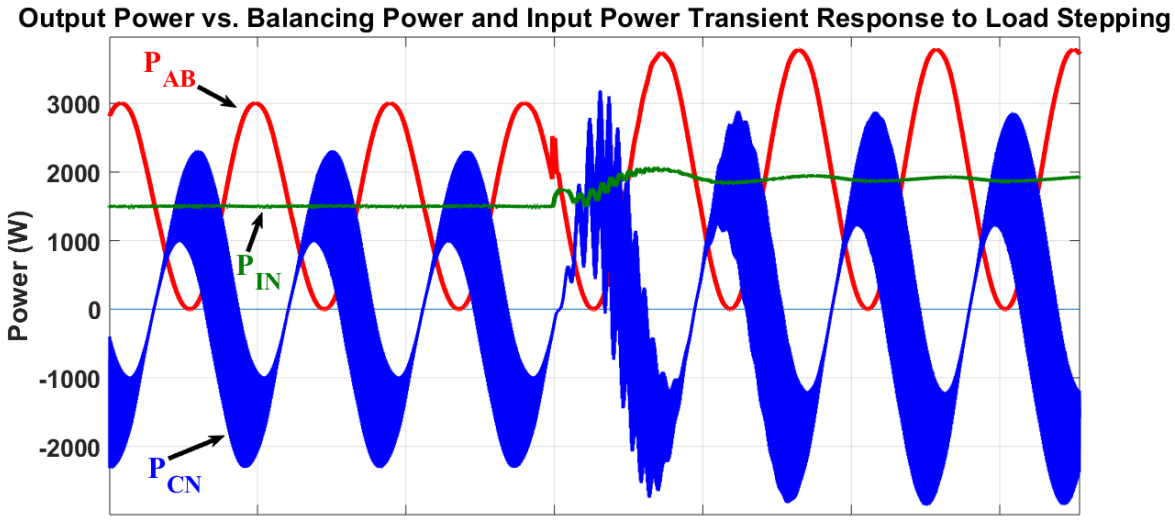

Figure 9. Output, Input, and Balancing Power Transient Response to Load Stepping of Output Impedance of One Load from 50% load to 100% load.

load stepping at the output. This response dies down quickly and the oscillations are largely dominated afterward by the second source of oscillations. This second source comes from the construction of the simulation topology, which can be seen in the appendix of this paper. The voltage source has an input resistor, which determines the input power that the system sees based on the current flowing through the resistor. This value changes when the power being consumed at the output changes. Thus, the voltage at the input must be tracked to determine the modulation signal gain for the inverter PWM switching patterns. There is a simple controller that tracks and feeds back this voltage signal to the PWM gain controller, so that the inverter will produce voltage waveforms of the correct size even when the current flowing into the input resistor changes. This controller is quite slow and is very simplistic and the mismatch of the balancing waveform to that of the output waveforms due to the speed of this controller is what causes the ringing seen long after the transient response of the balancing controller has ended. This controller will be included in the larger controller when the topology is implemented in hardware.

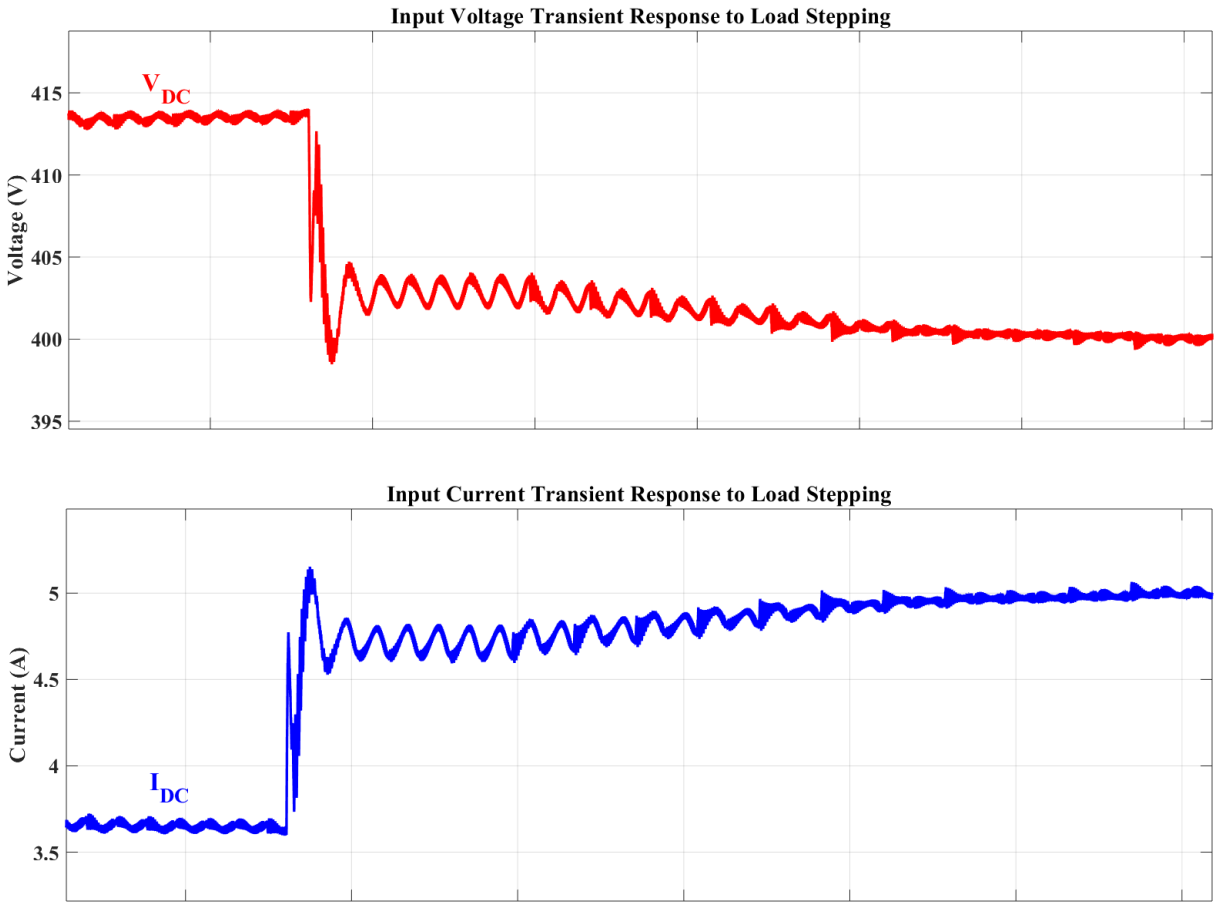

Figure 10. Transient Responses of Input Current and Voltage to Load Stepping of Output Impedance of One Load from 50% load to 100% load.

The input current and voltage step responses shown in Figure 10 clearly show the three regions of the step response of the circuit. The transient response of the balancing controller is the first region, which consists of the spike from 3.6 V to 5.1 V and one or two oscillations afterward. The second region is the response of the PWM gain controller which has a very slow rise time and no overshoot. This region starts with the small oscillations after the large step response and continue until the current settles at 5 A. The settling regions are after the current settles at 5 A and before the current spikes, when the input current is steady at 3.6 A.

The main task when designing the closed-loop controller should be limiting the overshoot of the closed-loop balancing controller, with the additional task of combining the PWM gain controller with the larger balancing controller. This can be achieved through another feedback path within the controller, which implements integral control for an overall PI controller. This will increase the stability of the system and should reduce the small current and power ripples seen in the converter to an even lower level.

The transient response of the dual-phase output inverter is good for a proportional controller and can be improved with more work on the closed loop controller and additional tests that will be needed to implement the system in hardware. The controller will need to run at more than ten times the switching frequency of the converter, which is 100 kHz for the simulation. This means the controller should have a minimum clock frequency of 1 MHz, which is true of almost every modern controller. The controller will also need to perform trigonometric functions as part of its job and will need to have that functionality.

CHAPTER V

CONCLUSION

In this thesis, the design, operation, and control of a two-phase output inverter were discussed. The mathematical model of the converter was derived and used to design the proportional controller for the topology that was developed. The mathematical model was tested and further developed using MATLAB and a design example showed the component values for an example system sized at 2 kVA. MATLAB was used as a tool to design the sizes of the inductors and capacitors for the LC filters of the system. PLECS was used to implement and test the topology and the closed-loop proportional controller of the system. Several load conditions were tested and transient analysis on the step response of the controller was performed. The results of the simulations confirmed the theoretical assertions made in the mathematical modeling section and the topology is now prepared to be implemented in hardware. The next task is to choose an appropriate apparent power level (possibly 2 kVA) to design the test system and design the component parameters. Then, the controller, will need to be re-designed as a PI controller and the rise time, overshoot, and settling time of the controller will need to be more closely examined. Finally, the controller will be selected that best fits the criteria of the design and the circuit will be constructed. Further testing will be done to reflect the increased complexity of a physical system and assess what parameters influence the performance of the design that were not considered in the simulation model.

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APPENDIX

PLECS Circuit Schematic of Two-Phase Output Inverter

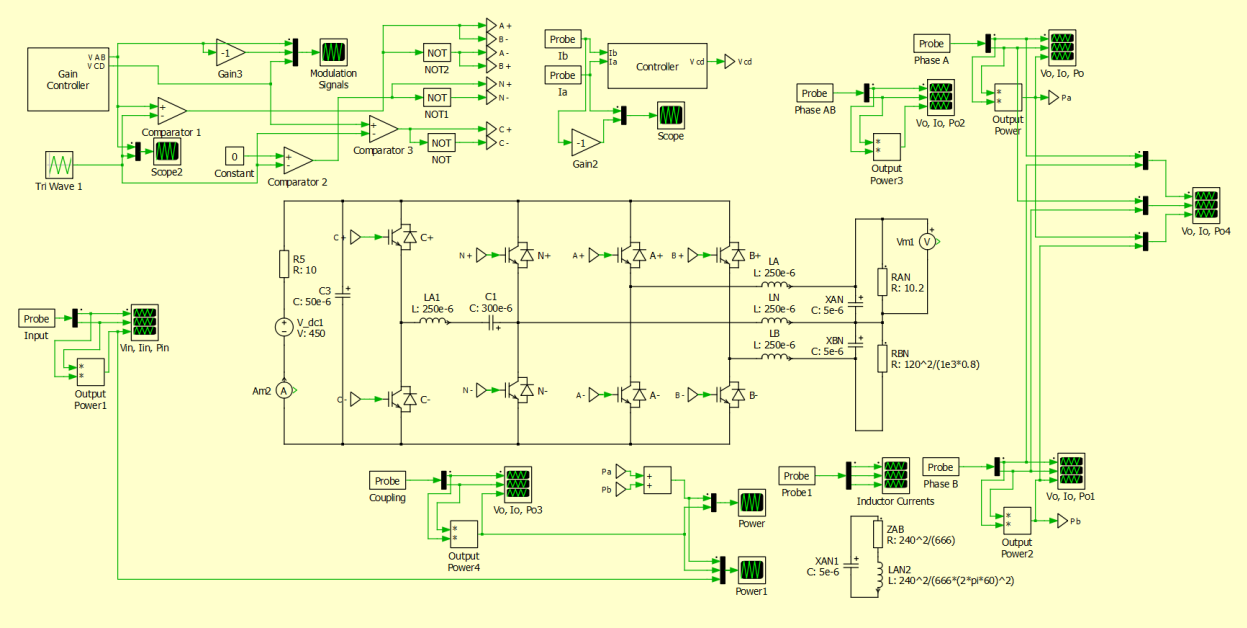

Figure 11. PLECS Circuit Schematic of Two-Phase Output Inverter