

# **HIGH SWITCHING FREQUENCY SEPIC REGULATOR WITH FPGA CONTROLLER**

An Undergraduate Research Scholars Thesis

by

FRANCISCO LAUZURIQUE

Submitted to the Undergraduate Research Scholars Program at  
Texas A&M University  
in partial fulfillment of the requirements for the designation as an

UNDERGRADUATE RESEARCH SCHOLAR

Approved by Research Advisor:

Dr. Sam Palermo

May 2020

Major: Electrical Engineering

# TABLE OF CONTENTS

|   | Page |
|---|------|
| ABSTRACT .....  | 1    |
| DEDICATION .....  | 1    |
| ACKNOWLEDGMENTS .....                                       | 2    |
| CHAPTER   |      |
| I. INTRODUCTION .....                                       | 3    |
| II. DESIGNING THE SEPIC CONVERTER .....                     | 6    |
| Selecting The GaN Transistor .....                          | 6    |
| Selecting The Duty Cycle .....                              | 7    |
| Selecting The Inductors .....                               | 8    |
| Selecting The Diode .....                                   | 8    |
| Selecting The Input Capacitor .....                         | 9    |
| Selecting The Coupling Capacitor .....                      | 9    |
| Selecting The Output Capacitor .....                        | 10   |
| Simulating The SEPIC Design .....                           | 10   |
| III. DESIGNING THE CONTROLLER FOR THE SEPIC CONVERTER ..... | 16   |
| Simulating The Control Algorithm .....                      | 18   |
| Design and Implementation on FPGA .....                     | 22   |
| IV. CONCLUSION .....  | 27   |
| Results .....   | 27   |
| Conclusion .....  | 30   |
| REFERENCES .....  | 31   |

# **ABSTRACT**

High Switching Frequency SEPIC Regulator With FPGA Controller

Francisco Lauzurique  
Department of Electrical & Computer Engineering  
Texas A&M University

Research Advisor: Dr. Sam Palermo  
Department of Electrical & Computer Engineering  
Texas A&M University

The increasing need for smaller and more efficient DC to DC regulators has motivated researches to look for alternate methods for designs. As electronic designs become smaller on size, the challenge of reducing design's size increases. DC to DC regulators occupy a large space of any electronic due to necessary components to obtain the expected functionality and efficiency. In addition, the voltage ripple on the output voltage is a very important factor as devices required a more precise input voltage to define different threshold voltages. Signal interference with noise-sensitive frequency bands such as AM radio is another important factor designer must observe when designing DC to DC regulators. In addition, with newer technologies such as USB Type-C which allows for up to 100W using USB PD specification requires that DC to DC regulators have a higher efficiency due to the heat that must be dissipated. Transient responses during switching process is another important factor for DC to DC regulators (Benefits). This research will target the main design considerations when implementing DC to DC regulators. Another important factor not mentioned yet is the BOM (bill of materials) cost, which will be reduced by the end product of the research.

## **DEDICATION**

This work is dedicated to my parents, they have always been a source of inspiration, encouragement and stamina to undertake my higher studies and to face life with grit, grace, and enthusiasm. And to my significant other for always support me and encourage me. Thank you all.

## **ACKNOWLEDGMENTS**

I would like to thank my entire family for supporting me throughout my entire college career and to my significant other for always been by my side.

I want to thank Dr. Palermo for helping throughout this entire research and motivate me. Thank you for being patient and share your knowledge with me. Thank you for all the countless hours working by my side on this project. Your experience was fundamental for the success of this research.

I also would like to thank all my fellow Aggie's working by my side on the senior design. My professors from the senior design class and my supervisor for helping and meeting with me in every lab session.

# CHAPTER I

## INTRODUCTION

As the technology of electrical devices advances, the devices require smaller and more efficient DC-DC regulators. This has motivated designers and researchers to look for alternatives components and topologies. Switching DC-DC regulators can step-down(buck) or step-up(boost) voltages with high efficiency. There are many choices when deciding upon which topology to use. Usually cost and complexity and very important factors when selecting the type of regulator. Most of the designs using switching regulators use inductors to average the power input to the system to a lower or higher average and use a series of filters in the output in order the reduce the ripples cause by the switching components. By increasing the switching frequency of the converter, we can effectively decrease the size of the passive components used for the averaging and filtering of the power. Increasing the switching frequency enables the design of integrated systems and reduces the output ripples. In addition to the mentioned advantages, increasing the switching frequencies can help reduce signal interference with noise-sensitive frequency bands such as AM radio [1]. GaN power switches have been the target of many designers due to the advantages of using these components for the conversions. GaN transistor have a very low  $R_{on}$  resistance and very high electron mobility that allows for very fast switching between ON/Off of the devices.

**Figure 1** shows a high level block diagram for the proposed design for the SEPIC regulator. The converter system will have a non regulated DC power supply as input that can vary its voltage for some allowed ranged. The Feedback (FB) or control loop would be design on an FPGA and will drive a GaN transistor with the required Duty Cycle to obtain the expected output voltage.

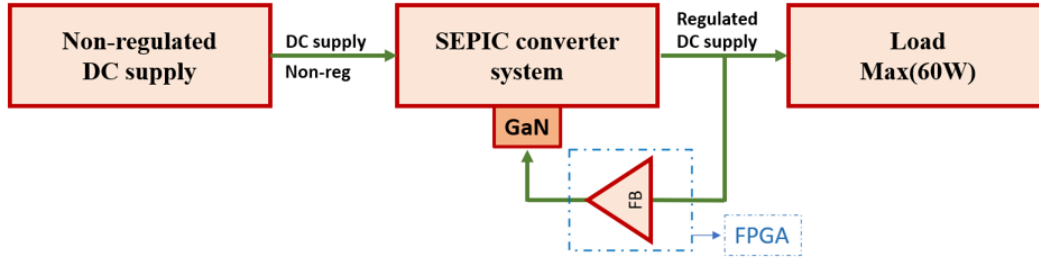


Figure 1: High Level Block Diagram

This research proposes the design of a SEPIC converter using GaN transistors. SEPIC converters can either buck or boost the voltage. The advantage of the design of a SEPIC converter vs a Buck-Boost converter is that we obtain positive output voltage and the transistor does not required an isolated gate driver since the source of the transistor is connected to the common ground of the system as illustrated in the **Figure 2**. The disadvantage of using the SEPIC topology is the complexity of the system including an extra inductor, and decoupling capacitor. Another disadvantage is that the small signal analysis for a SEPIC converter is challenging to model for simulations. In addition, the nature of the fourth order system of the SEPIC converter makes the system very unstable.

This research proposers to use GaN transistors because GaN has higher electron mobility than SiC, which allows for higher switching frequencies with lower power losses [2]. The higher the switching frequency for the DC-DC conversion the faster is the recover for the transient solution of the output voltage, but the more complex to design the feedback control loop for the system. This research proposes to target the control loop for the DC-DC regulator using an FPGA.

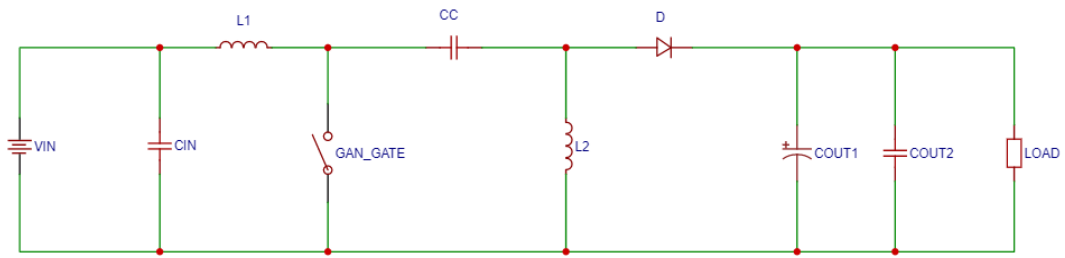


Figure 2: SEPIC DC-DC topology



## CHAPTER II

### DESIGNING THE SEPIC CONVERTER

For the design of the SEPIC converter it is important to begin by analyzing the mode in which the converter will be operating. In addition, the application targeted during the design is very important since it will provide the load conditions and ripple requirements. The load conditions for the design will play an important role since all the components will be required to operate for the targeted load conditions. Multiple components would be selected for the design of the SEPIC converter, this research begins by selecting the GaN transistor for the switching gate, the diode, the inductors, the coupling capacitor, input capacitor, output capacitor.

#### Selecting The GaN Transistor

The GaN transistor is one of the fundamental parts for the development of this design. The design of the SEPIC converter is based on the fact that by increasing the switching frequency of the transistor the size of the passive components required for the design of the converter can be decreased. Therefore, the GaN transistor must be able to achieve high switching frequencies. In addition, it is important to minimize the switching losses caused by the transistor by minimizing the  $R_{ds(on)}$  (drain-source resistance) related to the transistor and the  $Q_{gd}$  (gate-drain charge). Another important factor to keep in mind when selecting the transistor is the availability for drivers since the drivers required for this design must be able to effectively switch on and off the GaN transistor at very high switching frequencies. In the case of the SEPIC converter as opposed to the buck-boost converter, when selecting the drivers it would not be an issue having to worry about high side drivers for the implementation. The switch gate for the SEPIC is a low side and can be implemented with a non-isolated driver. Finally, it is necessary to calculate what values would the GaN transistor have to support. Important ratings to calculate for the selection of the transistor are the  $I_{pk}$  (peak current through the gate) and the  $V_{pk}$  (peak voltage) that the transistor must be able to block.

$$V_{pk} = V_{in(max)} + V_{out(max)} \quad (\text{Eq. 1})$$

$$I_{pk} = I_{L1(peak)} + I_{L2(peak)} \quad (\text{Eq. 2})$$

The peak current for the inductors on the design has not been defined, but the following components to be selected would be the inductors. The first component to be selected was the GaN transistor since this is a relatively new technology and there are a very limited amount of suppliers for these kind of transistors. This limited supply becomes a further issue when selecting the transistor based on the required ratings. Before selecting any other components, it is essential to define the Duty Cycle of the System. The GaN transistor use for the final design of the SEPIC converter is the [LMG341xR070](#) from Texas Instruments (TI), for high power applications including integrated gate drivers. This GaN transistor from TI is a very small solution with dimension of (8mm)x(8mm) and has excellent current and voltage protection circuitry.

### Selecting The Duty Cycle

Ideally the Duty Cycle for a converter would not be any issue since a SEPIC converter will ideally boost the voltage infinitely. However, due to the parasitic of the components, mainly the parasitic resistance of the inductors, the converter will reach a max voltage it can boost. Therefore, we must define a max voltage which the converter will boost by defining the lowest allowed voltage into the system. To begin with the selection of the Duty Cycle the ideal characteristic equation of a SEPIC can be use:

$$D = \frac{V_{out}}{V_{in} + V_{out}} \quad (\text{Eq. 3})$$

Then, in order to define the max Duty Cycle it is important define the lowest ( $V_{in}$ ), the max ( $V_{out}$ ). In addition to these two values, it is necessary to include the voltage drop across the diode ( $V_{drop}$ ) to the output voltage. The following equation will result in the max Duty Cycle allowed in order to remain within CCM (Continuous Conduction Mode):

$$D_{max} = \frac{V_{out(max)} + V_{D_{drop}}}{V_{in(min)} + V_{out(max)} + V_{D_{drop}}} \quad (\text{Eq. 4})$$

### Selecting The Inductors

The SEPIC converter is composed of two inductors ( $L_1, L_2$ ) for the buck and boost properties of the design. The inductor values selected for the design must ensure that the converter remains within CCM (Continuous Conduction Mode) at all times. This design uses CCM mode since it allows for smaller capacitors for the same ripple voltage than DCM (Discontinuous Conduction Mode).

$$I_{L1(peak)} = \frac{I_{out} * V_{out}}{V_{in(min)}} * \left[1 + \frac{k}{2}\right] \quad (\text{Eq. 5})$$

$$I_{L1(peak)} = I_{out} + \frac{k * I_{out} * V_{out}}{2 * V_{in(min)}} \quad (\text{Eq. 6})$$

$$L_1 = L_2 = \frac{V_{in(min)}^2 * D_{max}}{V_{out} * I_{out(max)} * k * f} \quad (\text{Eq. 7})$$

Where  $k$  stands for the max allowed ripple current in the inductors. Typically, designers use a current ripple through the inductors of 10-30% for better stability and low interference purposes [3]. Moreover, after selecting the GaN transistor, it is easier to adequately select the input switching frequency ( $f$ ) for the system. It is clear from this equation that having a high switching frequency will effectively decrease the size of the inductors.

### Selecting The Diode

Now that the switching frequency for the application has been selected, and that it is clear where would the  $V_{D_{drop}}$  affect out system, it is possible to select the diode to be use for the system. Important to notice that will low  $V_{D_{drop}}$  the system will achieve higher efficiency. For the consideration of the ratings of the diode it is important to consider the voltage that the diode must block and the current that the diode must support. The following equations describe the ratings for the

diode.

$$V_{D_{block}} = V_{in(max)} + V_{out(max)} \quad (\text{Eq. 8})$$

$$I_{D1(peak)} = \frac{I_{out} * V_{out}}{V_{in(min)}} * [1 + \frac{R}{2}] \quad (\text{Eq. 9})$$

The current rating for the diode for this design was selected based of the highest peak current through the inductors in order to ensure that the diode would not be damaged. For the design of the high switching frequency SEPIC converter a Schottky diode was selected due to its low forward drop voltage and high operating frequency.

### **Selecting The Input Capacitor**

In order to avoid ripple current into the ( $L_1$ ) inductor the SEPIC converter designed during this research will include an input capacitor ( $C_{in}$ ). In addition, the input capacitor will filter out any high frequency noise input form the unregulated supply stage. The input capacitor should have a low ESR (Equivalent Series Resistance) in order to create negligible ripples. A ceramic capacitor was selected for this stages since ceramic capacitors provide very low ESR and ESL (Equivalent Series Inductance).

$$I_{C_{in}(RMS)} = \frac{R * I_{out} * V_{out}}{\sqrt{12} * V_{in(min)}} \quad (\text{Eq. 10})$$

$$V_{rateC_{in}} = V_{in(max)} \quad (\text{Eq. 11})$$

Typical value use for a decoupling capacitor is 10uf minimum [4]. Recommended to use ceramic capacitors due to advantages mentioned before.

### **Selecting The Coupling Capacitor**

The coupling capacitor ( $C_c$ ) must be able to handle higher currents relative to the output. For this stage is recommended to use a ceramic capacitor due to all the advantages mentioned

before and that the ceramic capacitor does not have polarity. The following equations are used for the rating of the coupling capacitor.

$$I_{C_c(RMS)} = I_{out} * \sqrt{\frac{V_{out(max)} + V_{D_{drop}}}{V_{in(min)}}} \quad (\text{Eq. 12})$$

$$V_{rate_{C_c}} = V_{in(max)} \quad (\text{Eq. 13})$$

### Selecting The Output Capacitor

For the selection of the output capacitor it is important to analyze how much voltage ripple it is allowed for the targeted application. In addition, the ratings for the current in the output capacitor must be calculated. The following equations were used to calculate the required rating for the output capacitor.

$$C_{out} \geq \frac{2 * I_{out} * D_{max}}{V_{ripple} * f} \quad (\text{Eq. 14})$$

$$I_{C_{out}(RMS)} = I_{out} * \sqrt{\frac{D_{max}}{1 - D_{max}}} \quad (\text{Eq. 15})$$

A combination of electrolytic and ceramic capacitors was used on the output filter in order to reduce the high frequency output noise. By selecting ceramic capacitors to complete the required output capacitance, the output was improved [5]. The reason electrolytic capacitors were selected is that electrolytic capacitors are available with higher capacitance values while ceramic are available with lower capacitance values.

### Simulating The SEPIC Design

The simulator used for this design was Simulink from MATLAB. This simulator allows for easy implementations of DC-DC regulators. In addition, Simulink allows for the interaction of code base control loop with the topology of the system. This research proposes the control loop for the SEPIC converter through an FPGA and Simulink offers the possibility to prove the concept

for the control of the SEPIC converter. The following image is the final design of the SEPIC converter on Simulink.

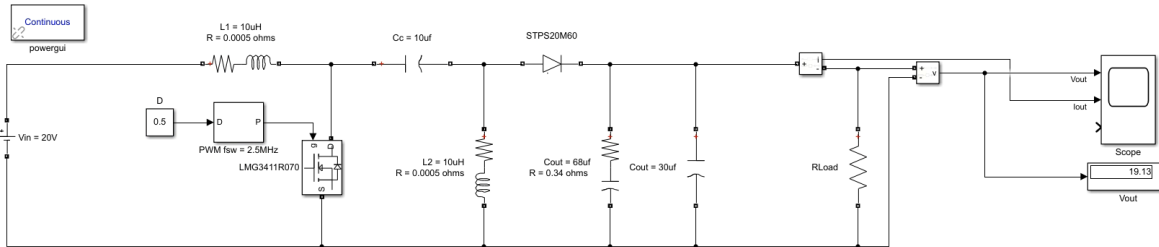


Figure 3: SEPIC DC-DC topology

The parasitic values for the components were included in this final design for a more similar behavior to the actual design. Measurements were taken from the output voltage and output current to observe how the Quasi-transient conditions would change with the variation of the non-idealities. The input voltage use for the simulation was 20V with a load of 3A and a switching frequency (fsw) of 2.5 MHz.

The simulation measurements taken from the SEPIC converter **Figure 4-7** helped defining the worse case scenarios for voltage overshoots. This measurements were used for the make the selection of the components. In addition, it defines which are the worse cases for the transition from Quasi-Transient conditions to the Quasi-Steady-State conditions. The worst case of voltage overshoot happens when the Duty Cycle is 20% which refers to passing the voltage through the system without bucking or boosting. The voltage overshoot is 25% of the expected output voltage above the expected value. Moreover, the simulations defined as the longest time for the transition of Quasi-Transient to Quasi-Steady-State as the case where the Duty Cycle has a value of 33% which relates to bucking the voltage to 10V. Finally, the plot in **Figure 8** shows the relationship between the output voltage and the Duty Cycle. With the blue color is represented the ideal relation between output voltage and Duty Cycle and the orange represents the relation between the simulated output

voltage and Duty Cycle. This relation is fundamental to understand how the output voltage of the converter gets affected due to parasitic values of the components. The ideal equation for the output voltage of the SEPIC converter predicts an infinite boost of the output voltage as the Duty Cycle reaches values close to the 100%. However, as we increase the Duty Cycle, the parasitic resistance of the inductors decrease the boosted voltage.

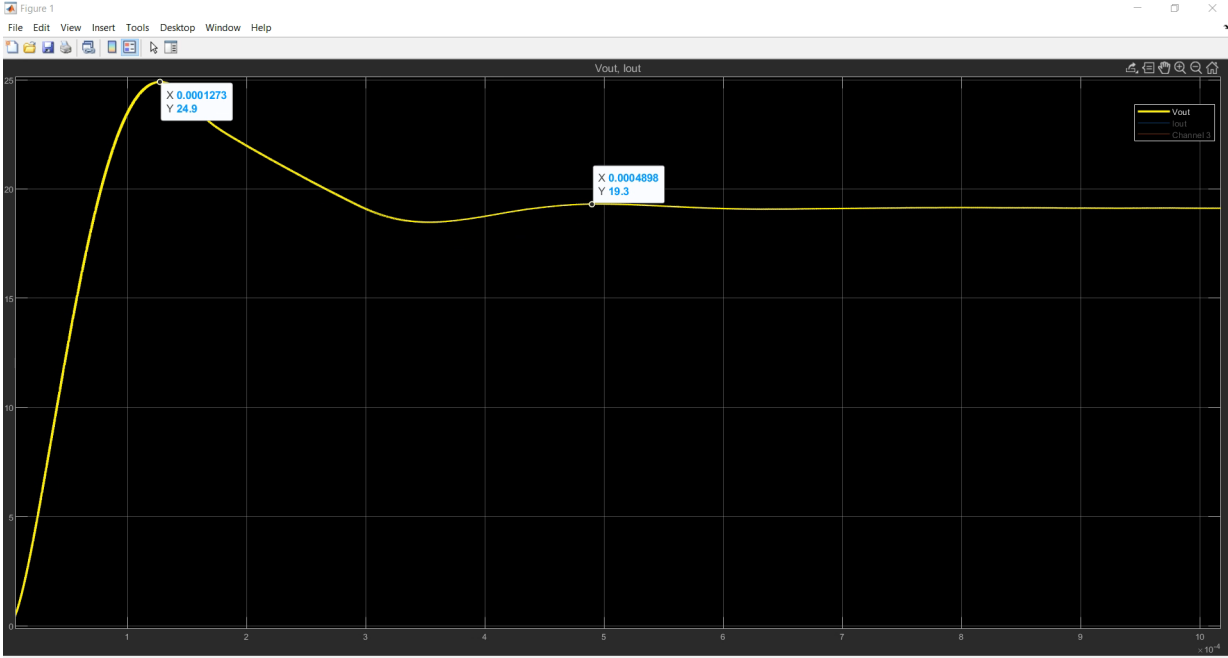


Figure 4: Quasi-Transient for Duty Cycle of 50%

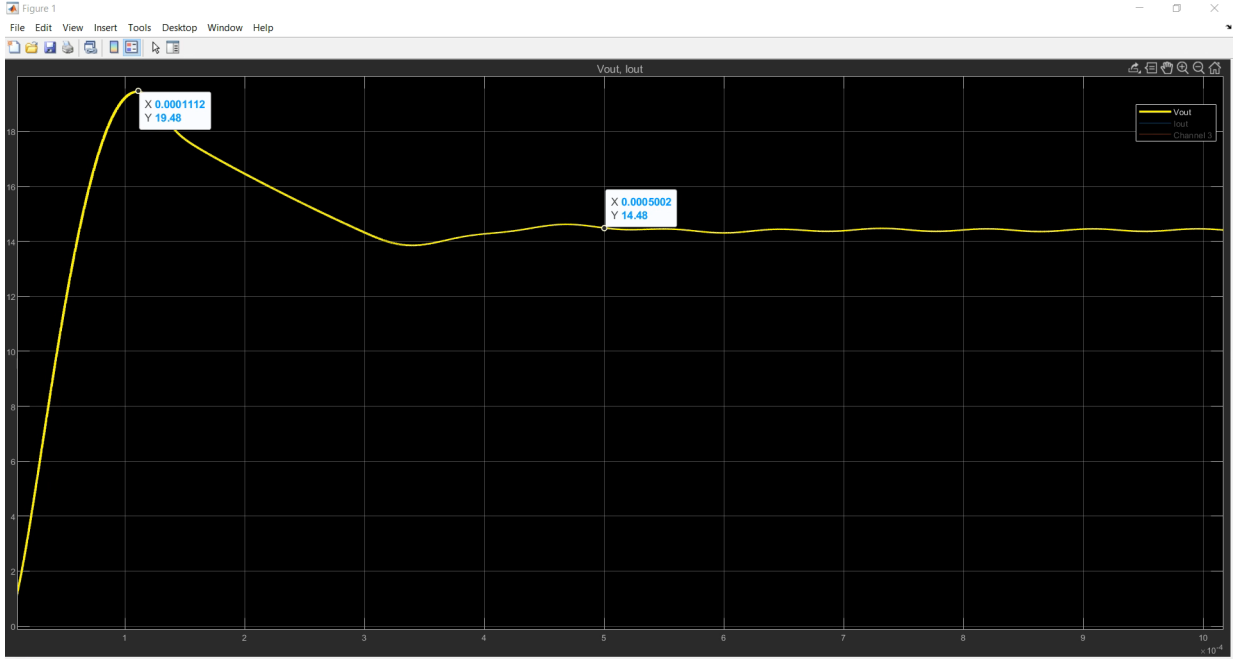


Figure 5: Quisi-Transient for Duty Cycle of 43%

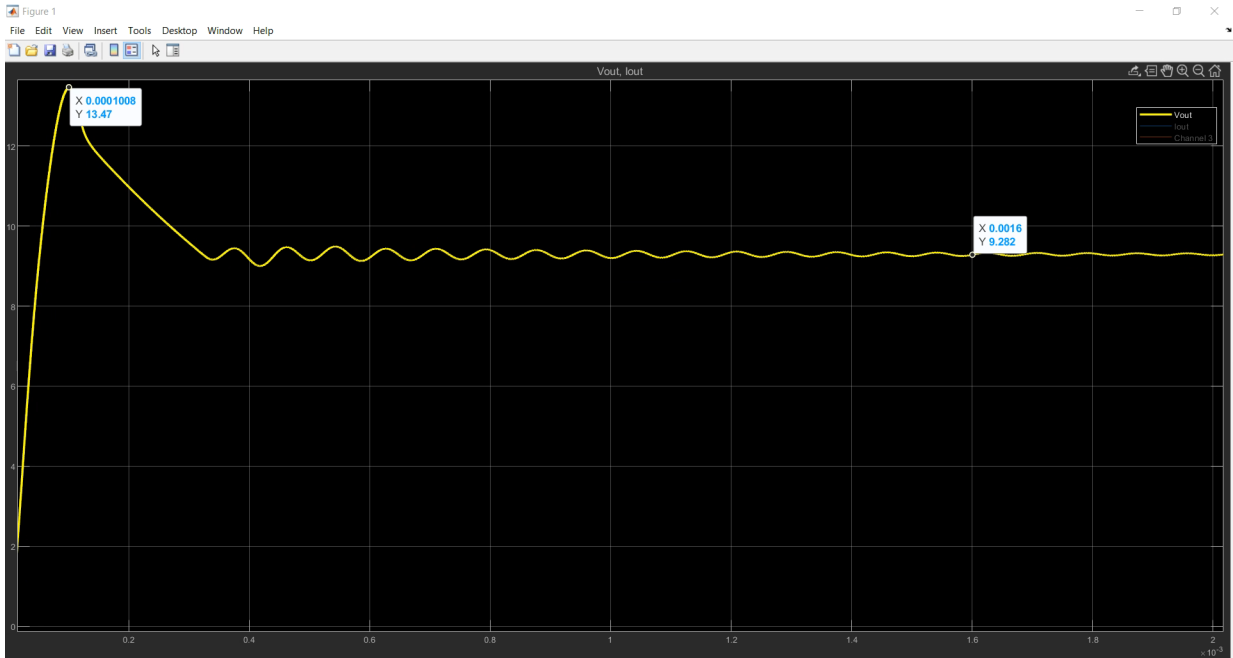


Figure 6: Quisi-Transient for Duty Cycle of 33%



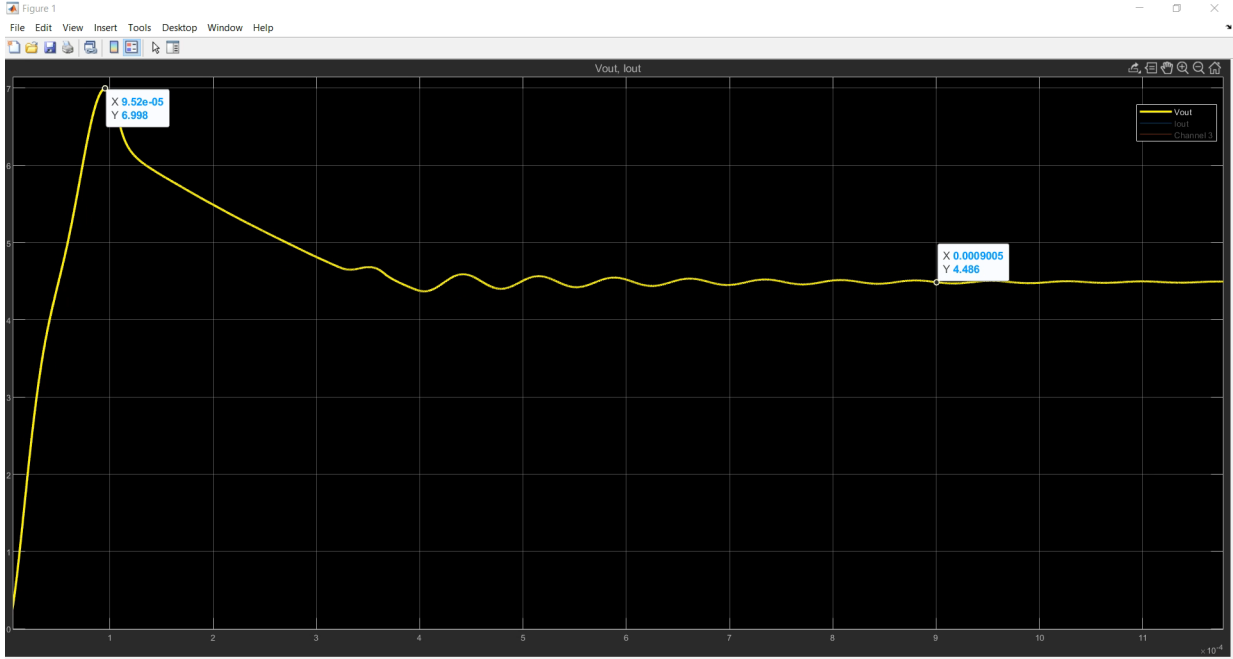


Figure 7: Quasi-Transient for Duty Cycle of 20%

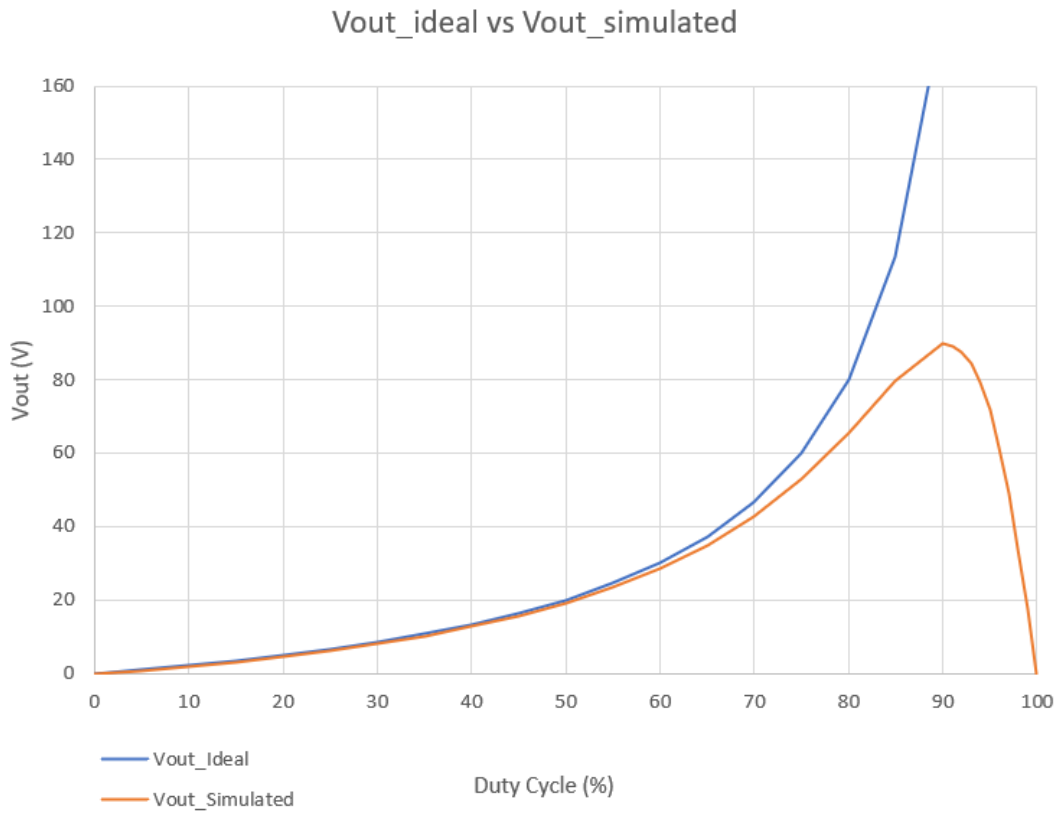


Figure 8: Vout vs Duty Cycle

## CHAPTER III

### DESIGNING THE CONTROLLER FOR THE SEPIC CONVERTER

SEPIC converters are usually avoided by designers due to the complexity of the design and more importantly the complexity of the control loop. SEPIC converters are very complex to control due to the nature of the fourth order system. The design of the compensated feedback can be very challenging. In addition, modeling the system for the small signal analysis can be cumbersome. The first step towards the design of the control loop for the system is analyzing the small signal transfer function of the converter.

Deriving the small signal transfer function for the SEPIC converter was made possible during this design by carefully following the work derived by Dr. David Middlebrook and Vorpérian [6]. The following equation describes the transfer function of the SEPIC converter from the controller to the output voltage.

$$DC\ gain = \frac{V_{in}}{(1 - D)^2} \quad (\text{Eq. 16})$$

Numerator components

$$3^{th}\ order = (-L_1 L_2 C_c D) s^3 \quad (\text{Eq. 17})$$

$$2^{nd}\ order = \left(\frac{V_{out}}{I_{out}} C_s (1 - D)^2\right) s^2 \quad (\text{Eq. 18})$$

$$1^{st}\ order = (L_1 (-D^2)) s \quad (\text{Eq. 19})$$

$$Constant = \left(\frac{V_{out}}{I_{out}} (1 - D)^2\right) \quad (\text{Eq. 20})$$

Denominator components

$$4^{th}\ order = \left(\frac{V_{out}}{I_{out}} L_1 L_2 C_c (C_{out1} + C_{out2})\right) s^4 \quad (\text{Eq. 21})$$

$$3^{th\ order} = (L_1 L_2 C_c) s^3 \quad (\text{Eq. 22})$$

$$2^{nd\ order} = \frac{V_{out}}{I_{out}} ((L_1 (C_{out1} + C_{out2}) D^2) + (L_1 C_c + (L_2 ((C_{out1} + C_{out2}) + C_c))) (1 - D)^2) \quad (\text{Eq. 23})$$

$$1^{st\ order} = ((L_1 D^2) + (L_2 (1 - D)^2)) s \quad (\text{Eq. 24})$$

$$Constant = \frac{V_{out}}{I_{out}} (1 - D)^2 \quad (\text{Eq. 25})$$

The complexity of the transfer function of the SEPIC converter makes the design for the compensator a challenging design work. This research proposes to control the SEPIC converter using an Field-Programmable Gate Array (FPGA). The design is proposed to function as a voltage to time converter. The FPGA will read the output voltage of the SEPIC converter and based on the results will control the Duty Cycle for the Pulse-Width Modulation (PWM) of the transistor. One disadvantage of using Voltage Mode Control for the converter is the slow response to changes on the output voltage. However, for this design, the largest time delay response on the controller will be created by the sampling frequency at which the Analog-to-Digital Converter can accurately convert the output voltage to a digital signal to be analyzed by the FPGA. Another important factor to take into account when choosing the correct design for the feedback topology is the non-idealities of the components to be use during the design of the control loop. The design of an analog control loop can be more challenging to design than the algorithm to run on the FPGA. The analog control loop would make more complex the already complex transfer function for the SEPIC converter. In addition, due to the number of poles and zeros the system would required a very complex stabilization scheme. For good stability on a system the Phase Margin should be greater than 45 degrees, which would be hard to achieve with a fourth order system. The design of the control loop using an FPGA would required less time and could be debugged and fixed easier than using an analog control loop. After analyzing the advantages and disadvantages of using the FPGA for the control loop, it is clear that for the design of this converter the best choice is the use of the FPGA.

## Simulating The Control Algorithm

Simulink was used for simulating the algorithm of the control loop. Simulink offers the opportunity to developed a code based control loop that would interact with a circuit. This interaction was essential to analyze since the interaction between the SEPIC converter and the FPGA would be similar to this interaction. As illustrated in **Figure 9**, the input to the control loop is the output voltage of the SEPIC converter and the output of the control loop is the Duty Cycle for the PWM block. In addition, memory blocks were used to store the value of the Duty Cycle, time at which the Duty Cycle was changed, and the voltage reference. These were necessary memory blocks since the algorithm of the block required the analysis of the past values of these values.

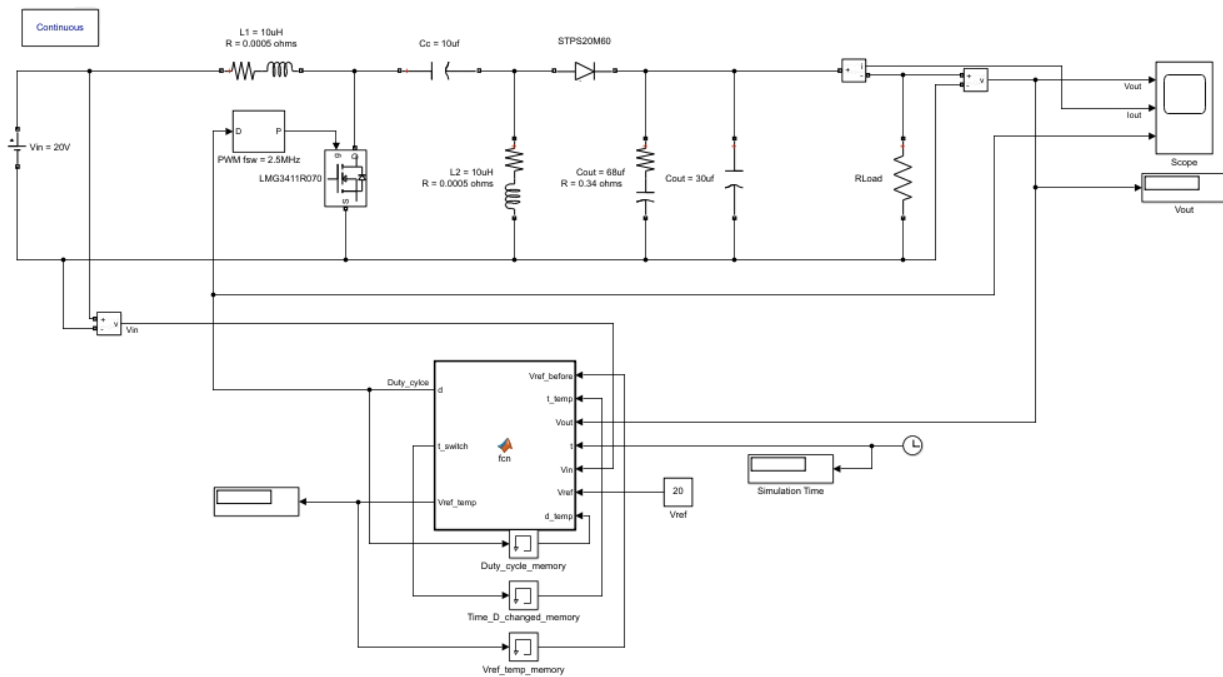


Figure 9: SEPIC converter with the control loop

**Figures 10-14** show how the control loop reacts to the output voltage outside the acceptable range. The yellow plot is for the output voltage and the red plot is for the Duty Cycle. The Duty

Cycle was expressed from values between 1 to 10, therefore, by simply multiplying the Duty Cycle by 10 we can obtain the Duty Cycle in percentage. The Duty Cycle was adjust to be between 1 and 10 for the waveform to show more detailed measurements of the output voltage. The control loop was design to initiate with a calculated Duty Cycle from the ideal Duty Cycle equation. Then, if the output voltage was found to be outside a established range, the control loop would correct the Duty Cycle to fall within the acceptable range. For most of the cases the system was able to be within the acceptable range on the first iteration, however, for low output voltage the system had to run more iterations since the acceptable range was based on a percentage of the output voltage. When the reference voltage is set for a low voltage such as 5V and the output acceptable range is based on a percentage of the reference voltage, as a result we observe a smaller range of acceptable output voltage compared to when the reference voltage is set to higher voltages such as 20V.

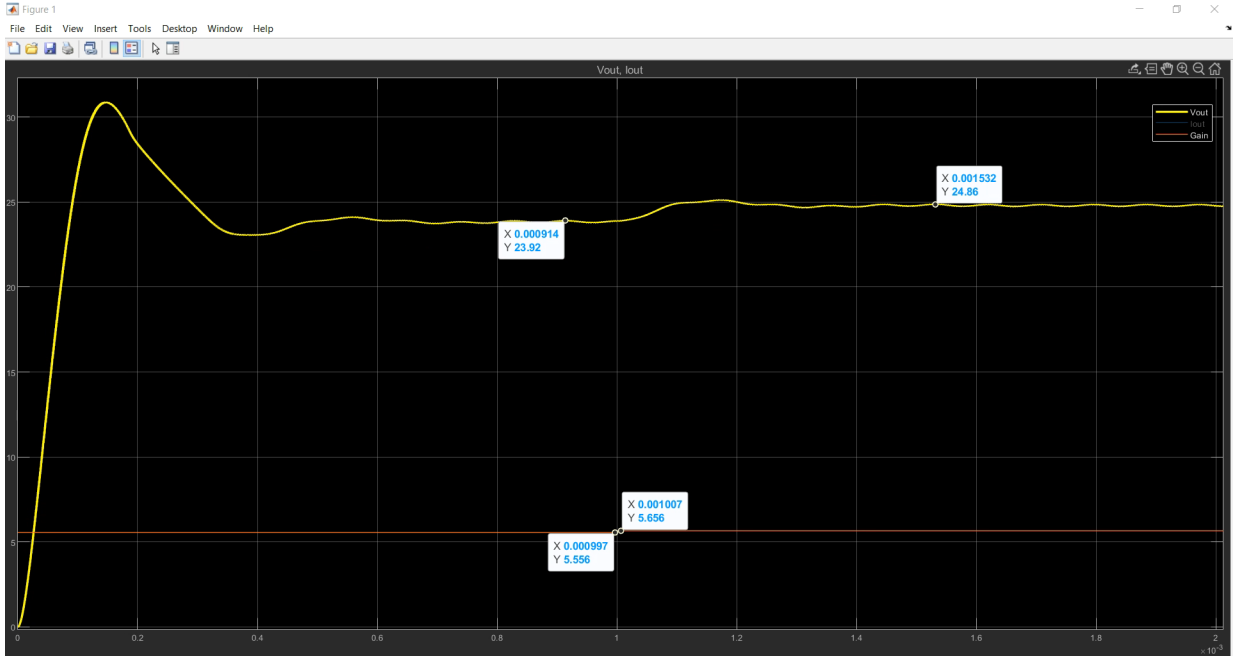


Figure 10: Boosting Vin=20V to Vout=25V

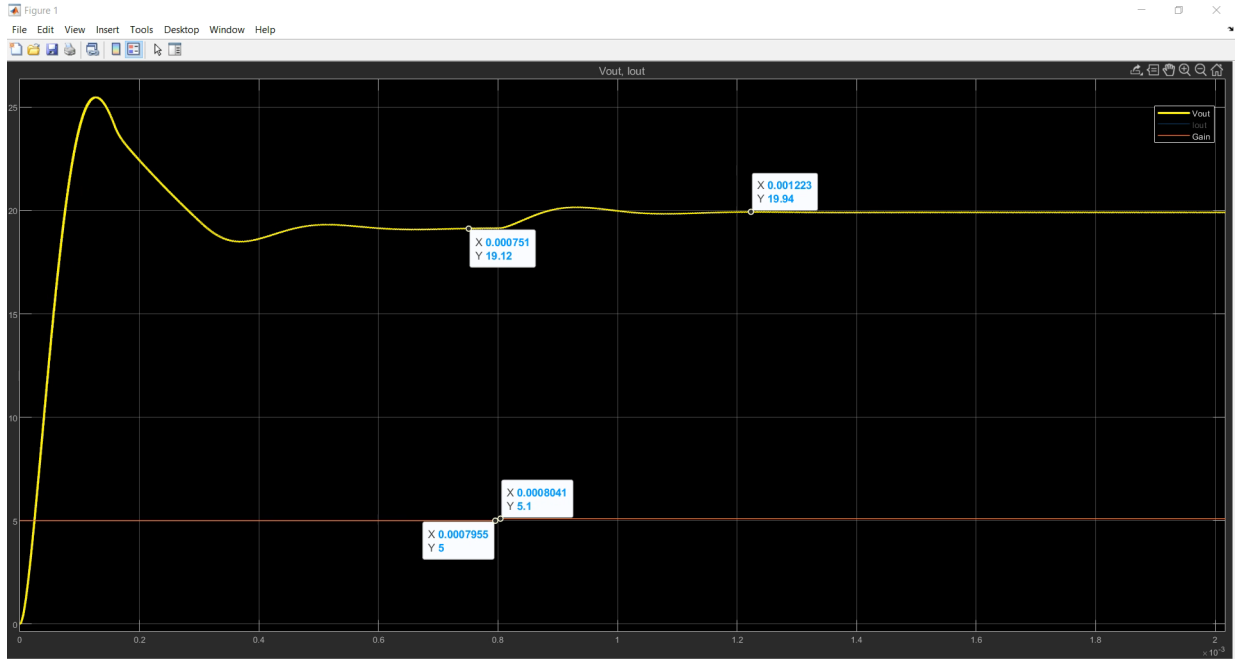


Figure 11: Passing  $V_{in}=20V$  to  $V_{out}=20V$

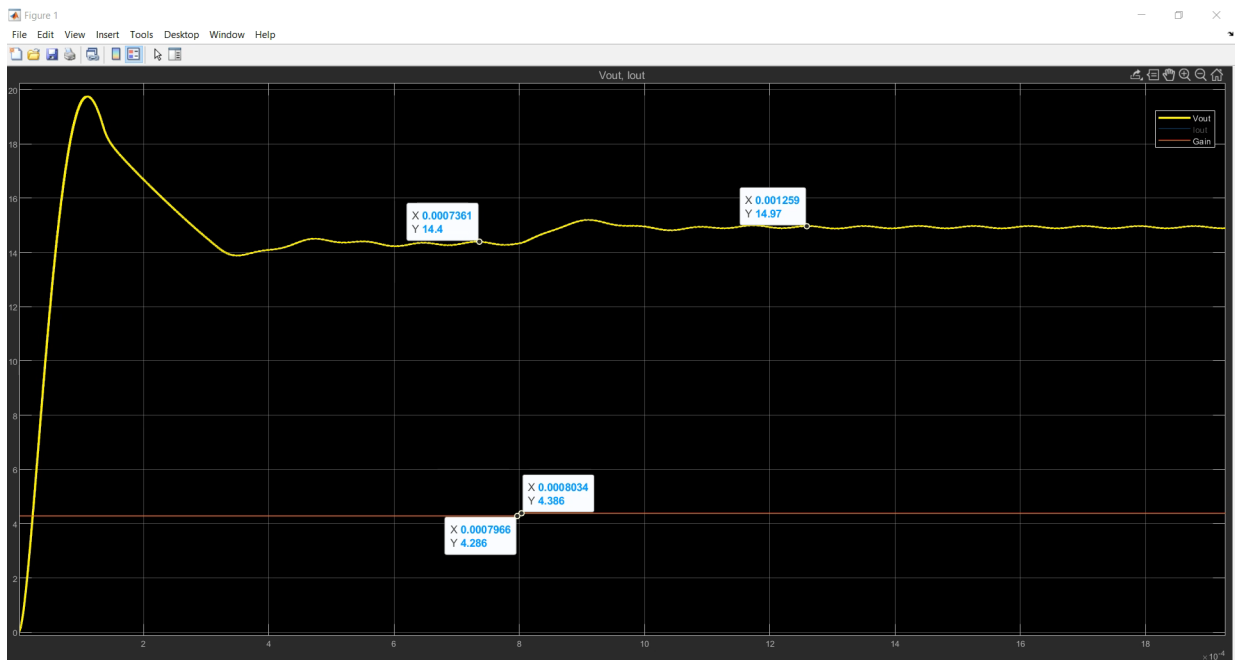


Figure 12: Bucking  $V_{in}=20V$  to  $V_{out}=15V$

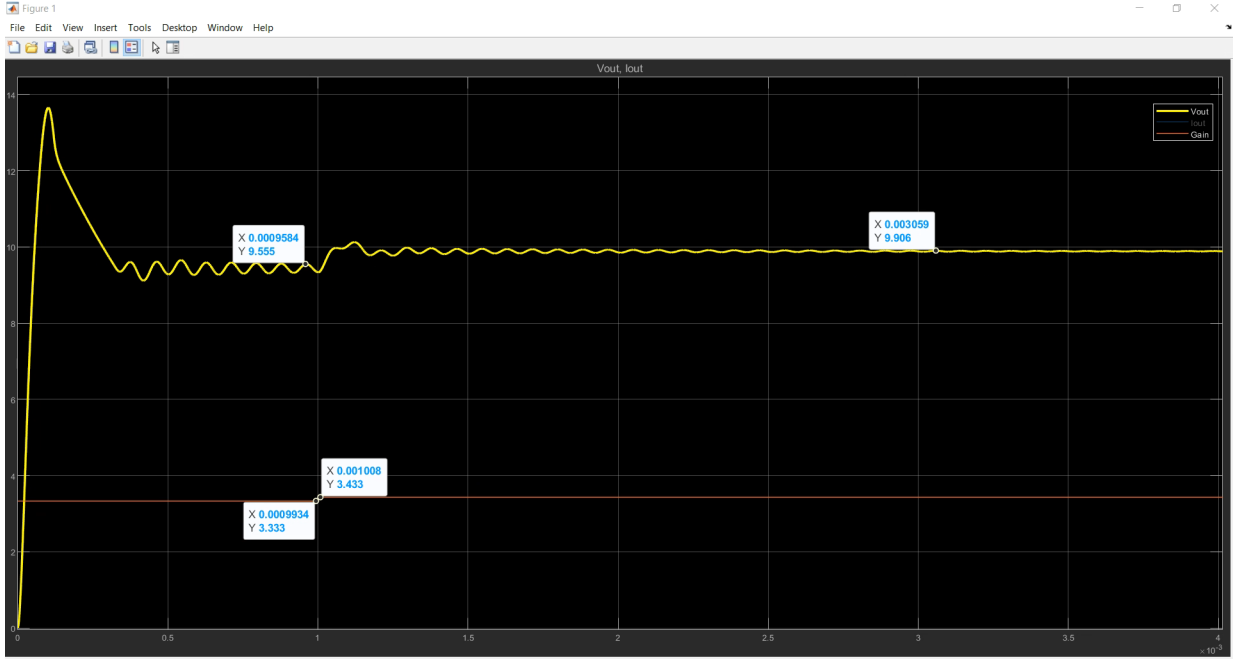


Figure 13: Bucking  $V_{in}=20V$  to  $V_{out}=10V$

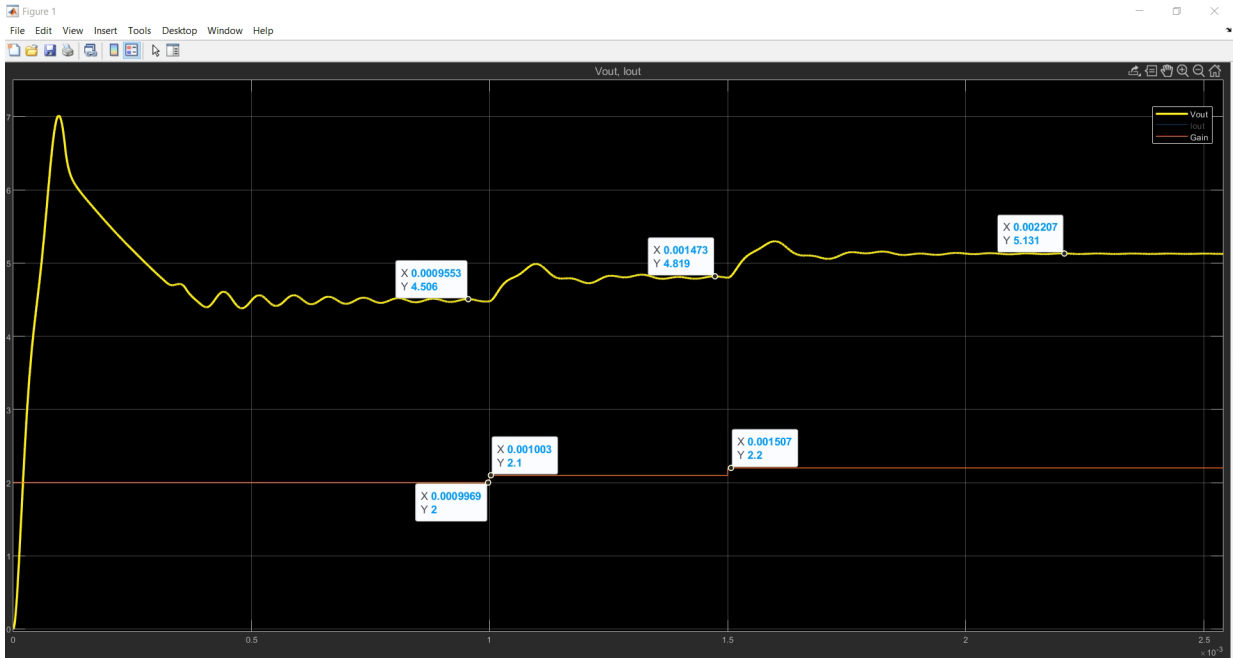


Figure 14: Bucking  $V_{in}=20V$  to  $V_{out}=5V$



## Design and Implementation on FPGA

For the design of the FPGA design it was required to break the design into three main design blocks. First, to design the 2.5 MHz PWM with a variable Duty Cycle. Second, successfully implement the ADC algorithm that would effectively read the output voltage and convert it into a digital signal to be analyzed by the FPGA. Finally, to design the algorithm to adjust the Duty Cycle accordingly with the required output voltage. The algorithm of the FPGA was design using Intel Quartus Prime, **Figure 15** show the Block Design File for the control loop of the SEPIC converter.

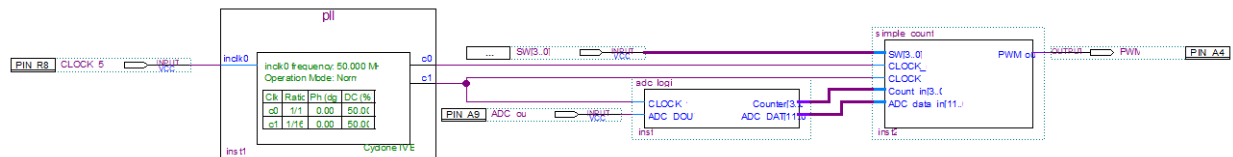


Figure 15: Block Design Files for control loop

The Phase-Locked Loop block (PLL) was design to create two oscillators with frequencies of 50 MHz for the design of the PWM and 3.125 MHz for the design of the ADC algorithm. The ADC block has two inputs, one is the 3.125 MHz oscillator to read the values from the output voltage at the required speed and the other to assign the address of which port to use from the board's header to read the analog signal. In addition, it has two output signals, one signal would be the read data and the other signal is a counter that would let the counter block know when the signal from the ADC is ready to be analyzed. The final block for the design is the counter block. The counter block has five inputs. The first input is the dip switch input (SW) which was use for the reference voltage of the system. **Figure 16** shows the relation between the values of the dip switch and the reference voltage to be maintained on the output of the system.

| SW     | Vref |
|--------|------|
| b'0001 | 5V   |
| b'0011 | 10V  |
| b'0111 | 15V  |
| b'1111 | 20V  |

Figure 16: Dip Switch reference

The second and third input on the counter block is the oscillator signals to create the 2.5 MHz PWM and to analyze the data from the ADC block. The fourth signal to the system is the counter signal output from the ADC and the fifth signal is the ADC data signal output from the ADC block. The counter block compares the signal from the ADC and ensures that the signal is between certain range. If the signal is outside the allowed range then the algorithm increases or decreases the Duty Cycle depending on the relation between the ADC signal and the reference voltage on the dip switches. Finally the FPGA outputs the PWM signal with the required Duty Cycle. **Figures 17-21** show waveform measurements from the output PWM of the FPGA. Some ripples due to high frequency can be observed on the PWM, but a buffer stage before the GaN transistor reduces the effects of the ripples during the process of turning ON/OFF the GaN transistor.

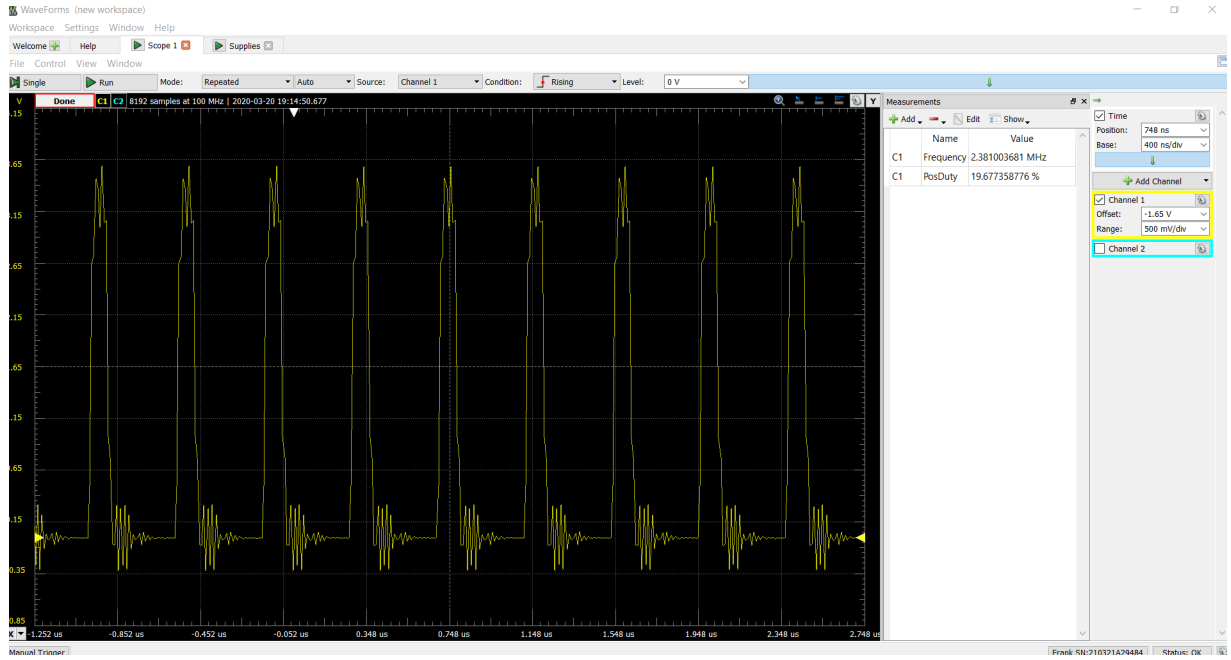


Figure 17: PWM with a Duty Cycle of 20%

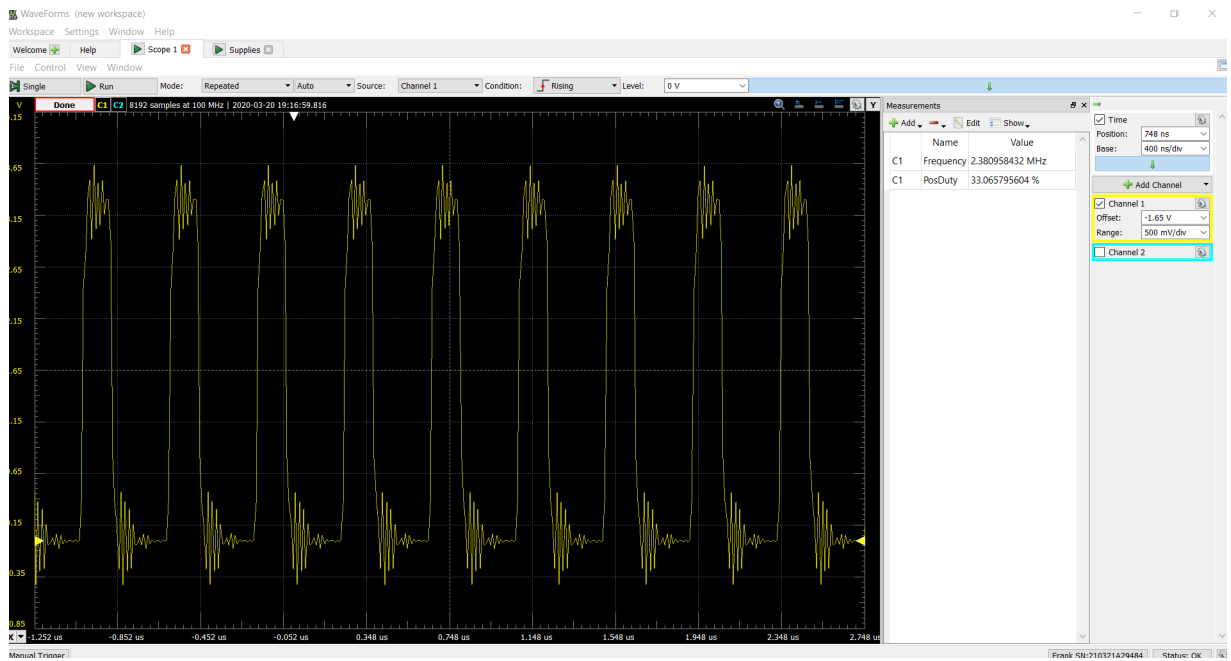


Figure 18: PWM with a Duty Cycle of 33%

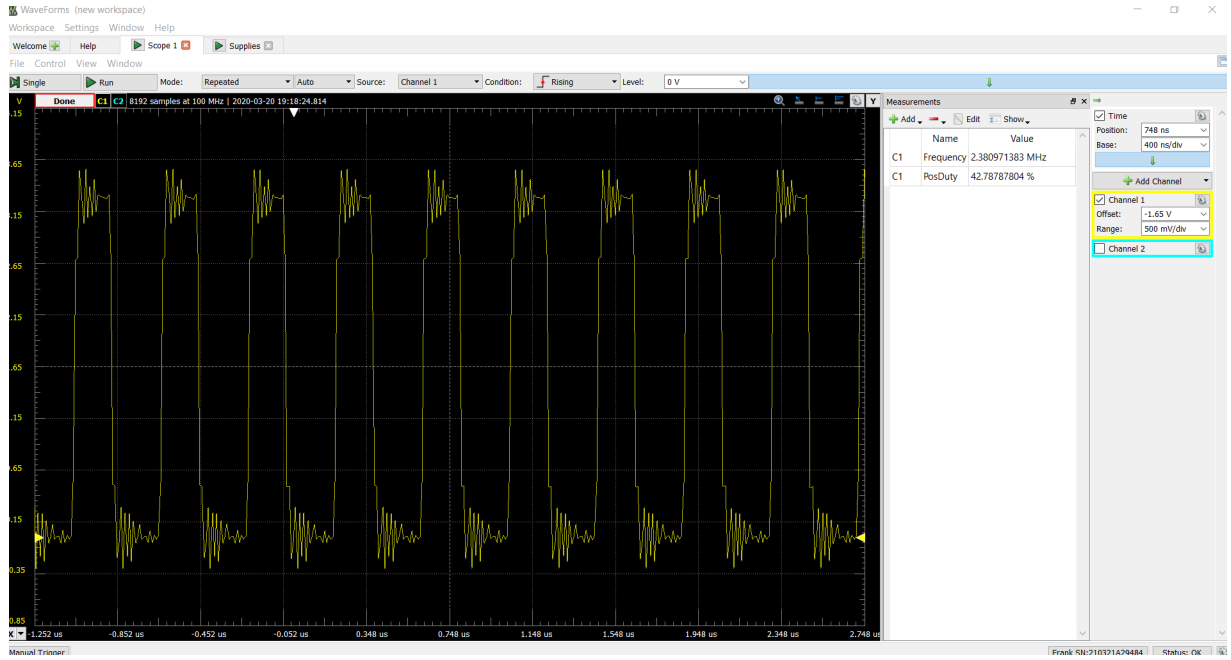


Figure 19: PWM with a Duty Cycle of 43%

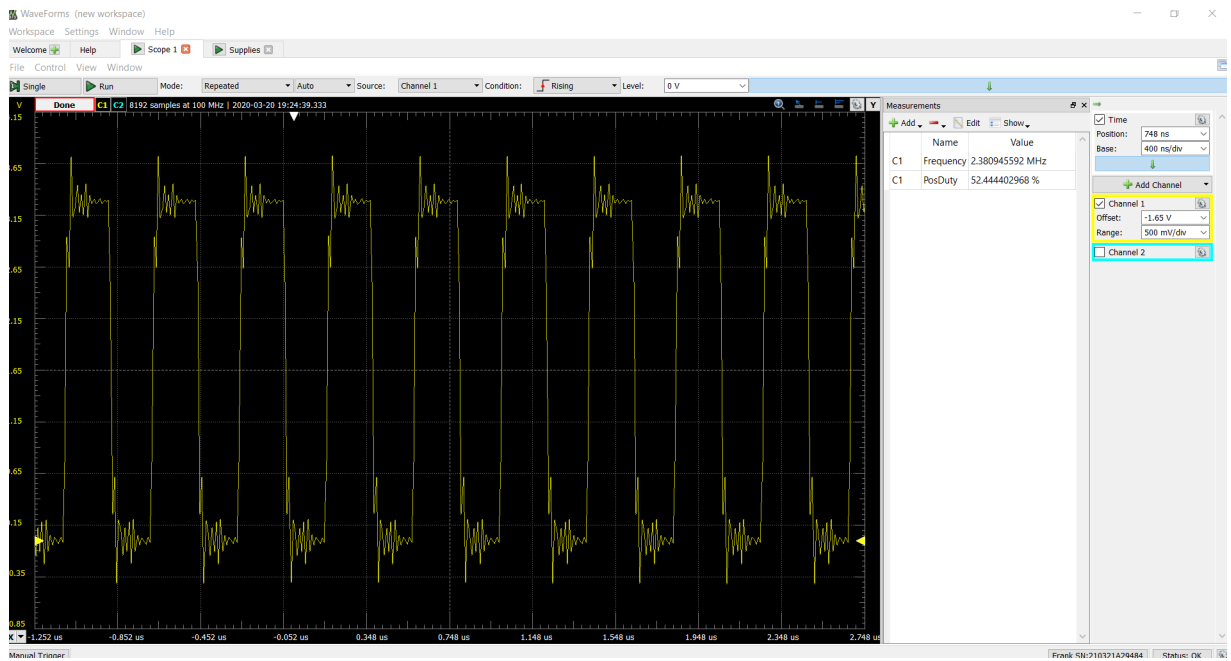


Figure 20: PWM with a Duty Cycle of 52%

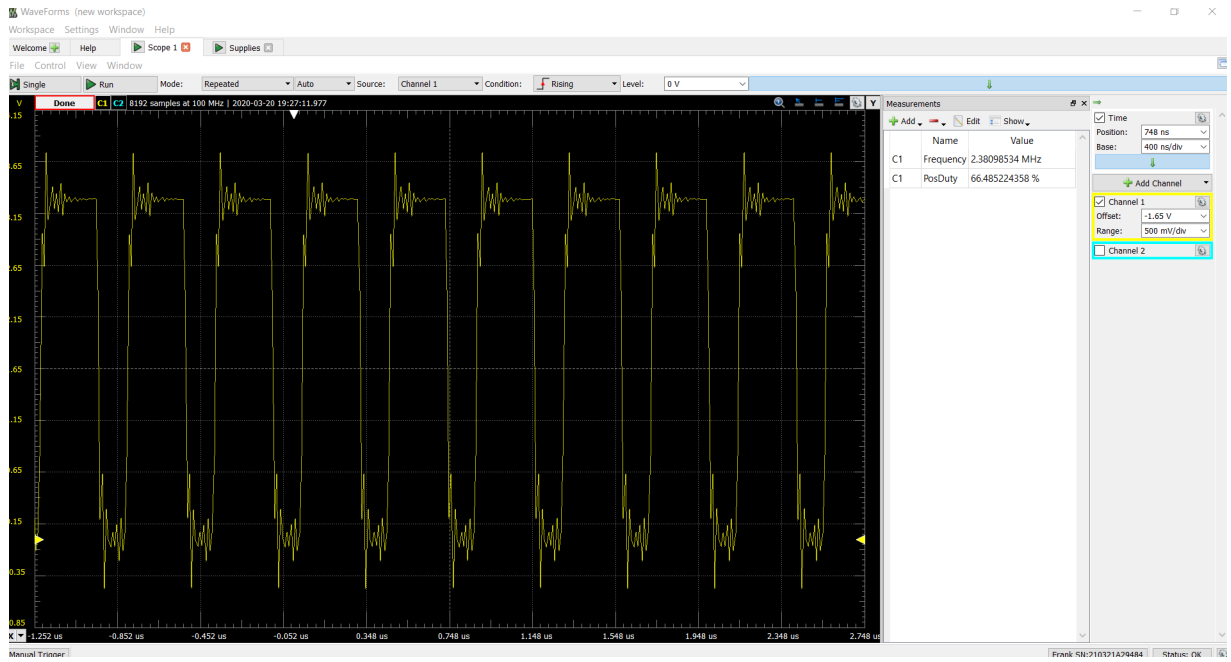


Figure 21: PWM with a Duty Cycle of 66%

## CHAPTER IV

## CONCLUSION

### Results

The final PCB design for the SEPIC converter is shown in **Figure 22**. The fundamental components for the SEPIC converter such as the GaN transistor, the inductors, and the diode are marked on the figure. The input voltage to the system must fall within 14V to 20V for the optimal behavior of the converter. The input supply to the SEPIC converter must be able to handle 3A of continuous current. The GaN transistor requires a 12V input voltage to bias the internal architecture of the chip, in addition, the PWM is required to switch the transistor ON/OFF. The SEPIC converter is design to have a variable output voltage with a maximum output voltage of 20V and a max current load of 3A, for a total of 60W maximum load.

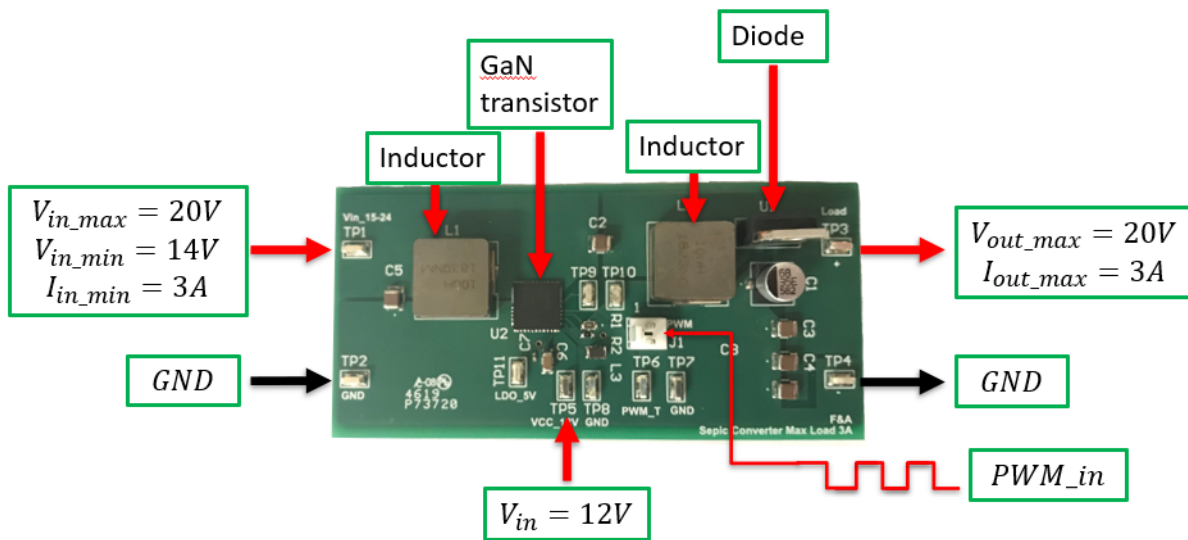


Figure 22: Final PCB design

The measurements shown in **Figures 23-25** were taken from the output voltage of the

SEPIC converter at the measured conditions. For **Figure 23** we have a PWM of 2.5 MHz, an input voltage of 20V, and a Duty Cycle of 50%, as a result, the output voltage of the system would be the same as the input voltage. For **Figure 24** the Duty Cycle was changed to 25% to prove the concept of bucking the input voltage, as a result the output voltage is 10.7V for this case. This value is a bit off the expected value due to the high switching frequency used. The higher the switching frequency the harder it is to achieve lower voltages by bucking. Finally, for **Figure 25** the Duty Cycle was changed to 70% to prove the concept of boosting the input voltage, as a result, the output voltage for this case was 25V. This value for the boosting property of the SEPIC converter was also found to be off from the expected value. The issue in this case arises from the parasitic resistance of the inductors as proven before in **Figure 8** when comparing the output voltage to the Duty Cycle. The output voltage would not follow the ideal relation with Duty Cycle due to the parasitic resistance.

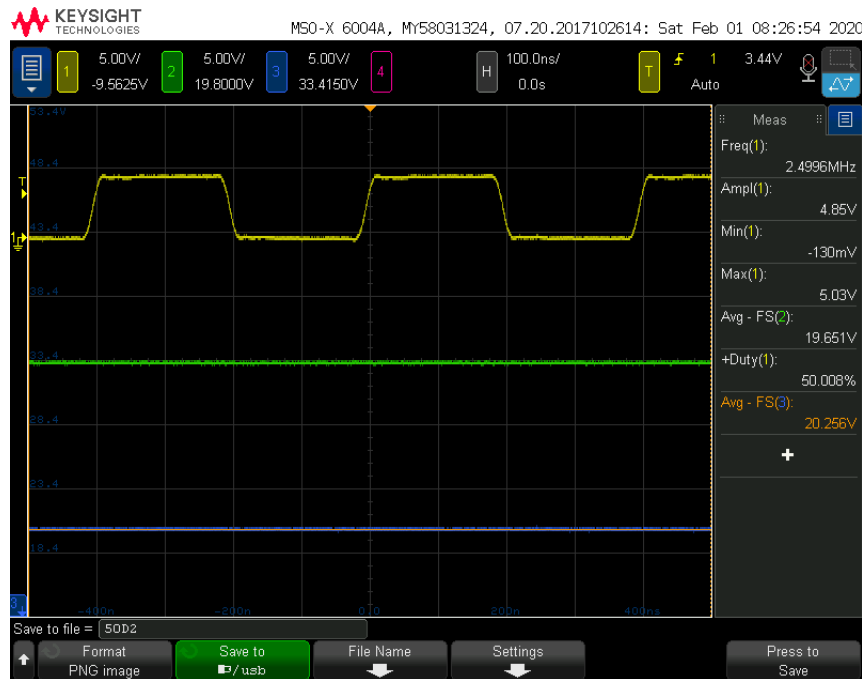


Figure 23: Measured waveform for 50% Duty Cycle

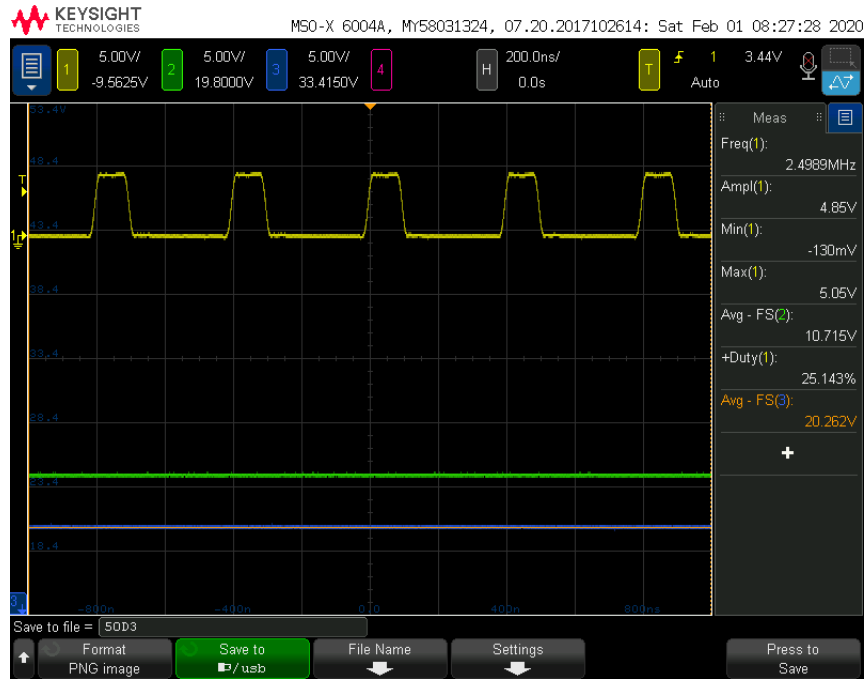


Figure 24: Measured waveform for 25% Duty Cycle

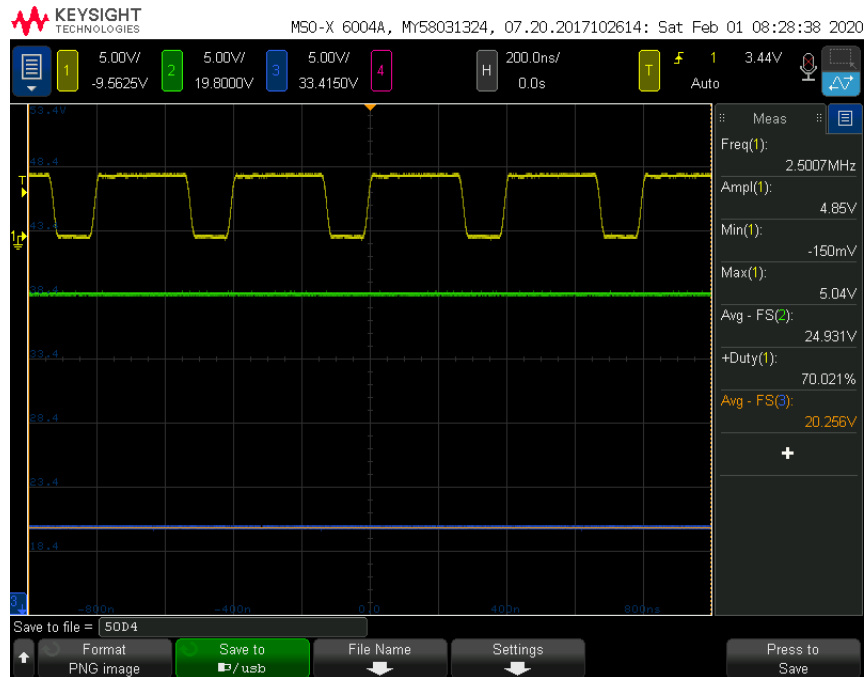


Figure 25: Measured waveform for 70% Duty Cycle



## Conclusion

The final design of the SEPIC converter was successful in decreasing the size of the components used for the topology. By increasing the switching frequency of the SEPIC converter up to 2.5 MHz the inductors used did not require large values. For this design the inductors selected were of 10 $\mu$ H. In addition, the size of the output capacitors was decreased to 98 $\mu$ F. The output voltage of the design proved to have very small ripple voltage, which is a very desirable quality for electronics that require a very precise voltage to define threshold voltages. The SEPIC converter effectively reduces interference with noise sensitive frequencies such as AM radio signal due to the high switching frequency used for the design. The final design allows up to 60W of power transfer. The transition from Quasi-Transient condition to Quasi-Steady-State condition happens faster which allows for better power efficiency. The SEPIC converter controlled by the FPGA proves to be very stable with fast transitions.

A suggested future work for this design would be the full integration of the system. The design effectively reduced the size of the components by using high switching frequencies which allows for a future integration of the design. A fully integrated or partially integrated SEPIC converter would require more extensive work. Since the inductors would have to handle high values of current maybe the partially integrated design would be a more feasible future work.

## REFERENCES

- [1] H. Xie and E. Guo, “How the switching frequency affects the performance of a buck converter,” 2019.
- [2] S. Chellappan, “Design considerations of gan devices for improving powerconverter efficiency and density.,” 2017.
- [3] EATON, “Switching regulator inductor selection,” 2016.
- [4] J. Falin, “Designing dc/dc converters based on sepic topology,” *Texas Instruments Incorporated*, 2008.
- [5] G. P. Alan Martin, Marc Davis-Marsh and I. Jorio, “Capacitor selection for dc/dc converters: What you need to know to prevent early failures, and reduce switching noise,” 2012.
- [6] R. Ridley, “Analyzing the sepic converter,” 2006.