POWER-EFFICIENT AND HIGH-PERFORMANCE CIRCUIT TECHNIQUES FOR ON-CHIP VOLTAGE REGULATION AND LOW-VOLTAGE FILTERING

A Dissertation

by

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ABSTRACT

This dissertation focuses on two projects. The first one is a power supply rejection (PSR) enhanced with fast settling time (T_S) bulk-driven feedforward (BDFF) capacitor-less (CL) low-dropout (LDO) regulator. The second project is a high bandwidth (BW) power adjustable low-voltage (LV) active-RC 4^{th}-order Butterworth low pass filter (LPF).

As technology improves, faster and more accurate LDOs with high PSR are going to be required for future on-chip applications and systems. The proposed BDFF CL-LDO will accomplish an improved PSR without degrading T_S. This would be achieved by injecting supply noise through the pass device's bulk terminal in order to cancel the supply noise at the output. The supply injection will be achieved by creating a feedforward path, which compared to feedback paths, that doesn't degrade stability and therefore allows for faster dynamic performance. A high gain control loop would be used to maintain a high accuracy and dc performance, such as line/load regulation.

The proposed CL-LDO will target a PSR better than – 90 dB at low frequencies and – 60 dB at 1 MHz for 50 mA of load current (I_L). The CL-LDO will target a loop gain higher than 90 dB, leading to an improved line and load regulation, and unity-gain frequency (UGF) higher than 20 MHz, which will allow a T_S faster than 500 ns. The CL-LDO is going to be fabricated in a CMOS 130 nm technology; consume a quiescent current (I_Q) of less than 50 μA; for a dropout voltage of 200 mV and an I_L of 50 mA.

As technology scales down, speed and performance requirements increase for on-chip communication systems that reflect the current demand for high speed data oriented applications. However, in small technologies, it becomes harder to achieve high gain and high speed at the same

time because the supply voltage (V_{DD}) decreases leaving no room for conventional high gain CMOS structures. The proposed active-RC LPF will accomplish a LV high BW operation that would allow such disadvantages to be overcome. The LPF will be implemented using an active-RC structure that allows for the high linearity such communication systems demand. In addition, built-in BW and power configurability would address the demands for increased flexibility usually required in such systems.

The proposed LV LPF will target a configurable cut-off frequency (f_o) of 20/40/80/160 MHz with tuning capabilities and power adjustability for each f_o. The filter will be fabricated in a CMOS 130 nm technology. The filter characteristics are as following: 4^{th}-order, active-RC, LPF, Butterworth response, V_{DD} = 0.6 V, THD higher than 40 dB and a third-order input intercept point (IIP3) higher than 10 dBm.

DEDICATION

To my family and to my fiancée

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CHAPTER I

INTRODUCTION

System-on-chip (SoC) solutions have become the norm in analog circuit design. The trend towards miniaturization, increased integration, and reduced cost have driven circuit designers to integrate as many functions as possible on a single chip. This has come with stringent requirements in power consumption and efficiency, while performance requirements keep increasing.

Two analog circuits, that meet all the previously mentioned requirements, are explored in this dissertation. These are: 1) Capacitor-less (CL) low-dropout (LDO) voltage regulators, due to their ubiquitous role in integrated circuits (ICs), and 2) low-voltage (LV) active-RC filters, due to their high performance, configurability requirements, and use of operational amplifiers (OpAmps) or operational transconductance amplifiers (OTAs).

Both of them are usually found in receivers for communication systems and any other circuit used for applications that require signal processing and filtering.

1.1 Capacitor-less Low dropout (CL-LDO) Voltage Regulators

LDO voltage regulators are often required to provide clean and reliable voltage supplies to on-chip circuits. More often than not this LDOs are integrated on-chip, along with all the other analog circuits, to save area. They are commonly referred to as CL-LDOs because they do not use an external capacitor, compared to those LDOs that require an external output capacitor either for stability or performance.

CL-LDOs are often required to occupy small silicon area, to use low-power, to have small noise, and to have good transient performance. These characteristics often trade-off each other,

therefore, recent advances in CL-LDOs always try achieving those goals. An introductory work to the terms and performance metrics on CL-LDOs can be found elsewhere [1].

Although, it is very hard to compare between designs, several CL-LDOs that achieve good performance have been published recently [2-15].

The proposed CL-LDO achieves high power supply rejection (PSR), small area, and good transient performance through a combination of several techniques, all of them which allow the proposed CL-LDO to be a competitive solution [16].

1.2 Active-RC Filter

Active-RC filters are an essential part of communication systems, where high-performance, power-efficiency, linearity, and LV environments put stringent requirements in the design of these circuits.

There has been a recent trend towards analog filter's operation using their supply voltage (V_{DD}) of 0.6 V, or below, which is starting to become a very active area of research [17-21]. Embedded into the development of LV high-performance active-RC filters is the design of OpAmps or OTAs that can operate and perform at the same voltage requirements such filters work. Introductory literature to the mathematics and concepts of filtering can be found elsewhere [22].

The proposed work presents a highly-configurable high-performance power-efficient LV fully-differential (FD) active-RC low-pass filter (LPF) and the improved OTA required to achieve such performance.

The dissertation is organized as follows. Chapter II presents background information on LDOs and previous works in the area. Chapter III discusses the proposed high-PSR fast settling time CL-LDO. Chapter IV discusses the recent techniques for LV design in analog filters. Chapter

V presents the proposed LV power-efficient active-RC LPF and its LV OTA. Finally, conclusions are given in Chapter VI.

CHAPTER II

LOW-DROPOUT VOLTAGE REGULATORS

2.1 Introduction

Dc-dc converters can be divided into switching voltage regulators and linear voltage regulators. A voltage regulator is a circuit that generates a fixed output voltage (V_{OUT}) that remains constant regardless of changes to its input voltage or load conditions [23]. In voltage regulators, the input voltage comes from an unregulated supply voltage (V_{DD}), which is why these two terms are often used interchangeably to describe the same voltage. Voltage regulators are used in portable systems and devices such as laptops and mobile phones; computer processing, automobile, medical equipment, etc.

Linear voltage regulators can be divided into two groups: conventional regulators and low-dropout (LDO) voltage regulators. The difference between them is the minimum amount of headroom, or dropout voltage (V_{DO}), required to maintain a regulated V_{OUT} [24]. V_{DO} is the minimum voltage required across the regulator to maintain regulation [24]. LDO voltage regulators is the classification given to those linear regulators that have a low input-to-output differential voltage ($V_{IN\text{-}OUT}$), LDOs usually have a $V_{IN\text{-}OUT} \leq 0.3$ V [25]. Throughout this thesis, the acronym LDOs is going to be extensively used to refer to LDO voltage regulators.

Compared to switching supplies, LDOs occupy less printed-circuit board (PCB) and silicon area, react faster, contribute to less noise, and are cheaper. However, their efficiency is low and also heat dissipation becomes important when high load currents (I_Ls) are required. Usually when high efficiency or large $V_{IN\text{-}OUT}$ is required, switching converters are chosen. LDOs are preferred

when powering noise sensitive applications or systems that require a small footprint and silicon area.

LDOs are generally divided into two subgroups. These are capacitor-less (CL) LDOs and externally-compensated LDOs. CL-LDOs are those LDOs that do not require an external capacitor to properly function. CL-LDOs can also be internally or output compensated. Both externally-compensated LDOs and output compensated CL-LDOs have their dominant pole at the output node. The difference is that externally-compensated LDOs have an external capacitor in the μF range, whereas output compensated CL-LDOs are designed to be stable with capacitors in the hundreds of picofarads. More often than not, adding a big output capacitor into an internally compensated CL-LDO causes the LDO to become unstable since it may have not been designed to tolerate high capacitances at the output node. On the other side, externally-compensated LDOs require a big output capacitor in order to function properly and may not work properly if no output capacitor, or a very small one, is connected to its output node.

This chapter will describe the basic terms used to describe LDOs in general. The terminology is shared regardless of the compensation method used in a particular LDO. This chapter is divided as follows. Subsection 2 discusses the building blocks that form an LDO. The performance metrics are described in subsection 3. And finally, recent publications and state-of-the-art LDOs are briefly discussed in subsection 4.

2.2 Building blocks

CL-LDOs are commonly built using a set of five blocks, as shown in Fig. 1. These blocks are: a voltage reference (V_{REF}), an error amplifier (EA), a pass device or pass transistor (M_P),

frequency compensation, and a feedback network. The CL-LDO in Fig. 1 includes load resistance (R_L), load capacitance (C_L), feedback resistors (R_{F1} and R_{F2}), compensation capacitor (C_M), and compensation resistor (R_M). Miller compensation is shown as the compensation method in Fig. 1; however, this was for illustration purposes only and any other well-known compensation method can be used.

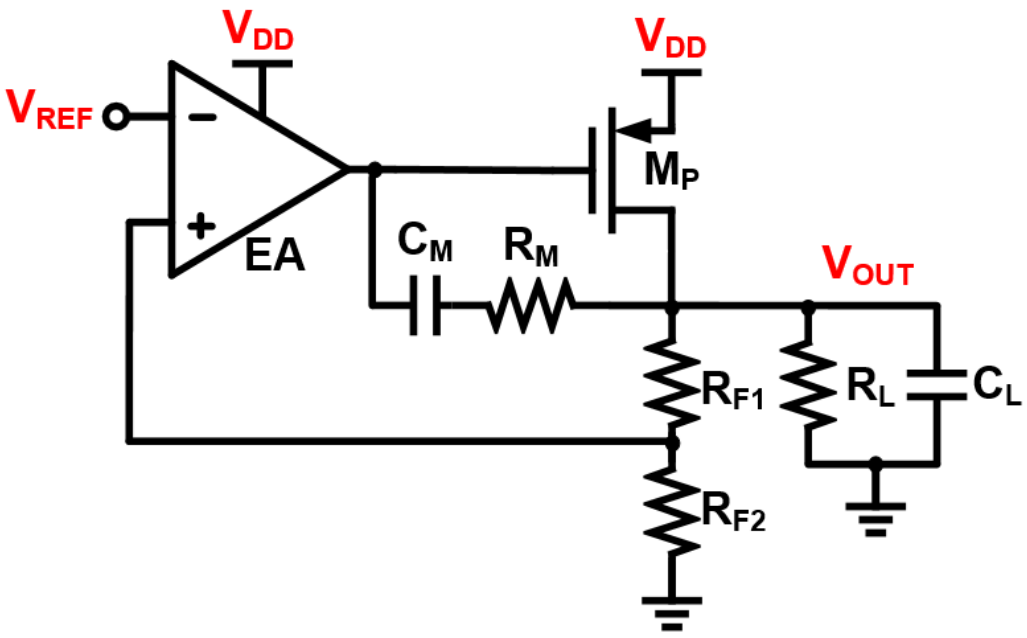


Fig. 1: Conventional CL-LDO building blocks

The EA compares V_{REF} with the voltage from the feedback network and provides the adequate gate voltage for M_P such that V_{OUT} stays constant, regardless of R_L or V_{DD}. Since C_L is usually small, and sometimes a parasitic capacitor of the load circuit, CL-LDOs usually require to be internally compensated to be stable. V_{OUT} is given by:

$$V_{OUT} = \left(1 + \frac{R_{F1}}{R_{F2}}\right) V_{REF} = \frac{1}{\beta} V_{REF} \quad (1)$$

where β is the feedback factor. As long as the CL-LDO's loop gain (LG) is high enough, V_{OUT} is independent of V_{DD} and only depends on V_{REF}.

2.3 LDO terminology

This section describes the most common terminology used in LDOs. All of these terms are also quantities that can be measured and reported. Performance metrics usually used in the literature to compare LDOs among each other are described in subsection 4.

2.3.1 Input-to-output differential voltage

The input-to-output differential voltage (V_{IN-OUT}) is the voltage difference between V_{IN}, or V_{DD}, and V_{OUT} at which the LDO is operating in steady-state at that particular time. LDOs have a range of allowed V_{IN-OUT} at which they can operate. At the lower end, V_{IN-OUT} is limited by the V_{DO}, and at the higher end it is limited by power dissipation. Even for the same LDO, these limits are not constant since both limits vary with I_L and temperature. A higher I_L increases V_{DO} and decreases the maximum V_{IN-OUT}.

V_{IN-OUT} is also important for performance, a higher (lower) V_{IN-OUT} increases (decreases) PSR.

2.3.2 Dropout voltage

V_{DO} is the minimum required V_{IN-OUT} for an LDO to maintain a regulated V_{OUT} [24]. Although the definition of V_{DO} is commonly used and accepted, in practice different companies and researchers may measure V_{DO} differently. This comes from the fact of the loosely defined term "regulated" in the definition, and from the different test benches that could be used for measuring. Some companies may interpret a 1% error or deviation in V_{OUT} as regulation being lost, whereas some other companies may use a 3 or 5 % error. Other companies determine V_{DO} to be the voltage at which a further decrease in V_{DD} also causes a decrease in V_{OUT} [26]. Therefore, caution must be used when comparing two LDOs from different vendors or even different models within the same company.

2.3.3 Quiescent Current

The quiescent current (I_Q) is the total current consumed by the LDO, excluding I_L. A low I_Q is especially important in low-power or battery operated applications were it is more likely that large periods of stand-by or inactive periods take place.

2.4 Performance Metrics

The most important performance metrics for CL-LDOs are: line and load regulation, line and load transient, noise, power supply rejection (PSR), and efficiency (η). In general, most LDOs, including both externally-compensated LDOs and CL-LDOs, share the same performance metrics discussed in this subsection.

2.4.1 Power supply rejection

PSR is the ability of a voltage regulator to block or reject changes in V_{OUT} due to fluctuations in V_{DD}. This is measured over the entire frequency range of interest. This is an important parameter for CL-LDOs whose V_{DD} is provided through a switching regulator, for systems that require high efficiency and low noise, because the switching regulator has a constant ripple at the switching frequency. The frequency of interest can vary and depends on the switching frequency of the switching regulator that precedes the CL-LDO. The PSR transfer function is inversely proportional to the LG, at low and mid-frequencies, and to C_L and the output impedance after the LG has stopped providing gain. This can be expressed approximately as in (2), where ω_{out} is the output pole frequency.

$$\frac{V_{OUT}(s)}{V_{DD}(s)} \propto \frac{1}{LG(s)} \bullet \frac{1}{\frac{s}{\omega_{out}}+1} \tag{2}$$

A more detailed analysis of PSR in a CL-LDO is discussed in chapter III, subsection 2 of this thesis and has also been discussed by other authors [1, 27, 28].

2.4.2 Line Regulation

Line regulation is a measure of the change in V_{OUT} (ΔV_{OUT}) due to a change in V_{DD} (ΔV_{DD}), and can be expressed as in (3), where LG_0 is the loop gain at dc. This metric looks at the same transfer function as PSR; however, it is measured once V_{OUT} has reached steady-state.

$$\left.\frac{\Delta V_{OUT}}{\Delta V_{DD}}\right|_{t\to\infty} = PSR(0) \propto \frac{1}{LG_0} \tag{3}$$

Similar to PSR, which is inversely proportional to LG, a higher LG_0 decreases ΔV_{OUT} due to ΔV_{DD}. Even though a low-frequency measure of PSR would give a good estimation of line regulation, it is still an important parameter to measure since it takes into account the EA's sensitivity, and therefore the CL-LDO, to changes in its dc operating point.

This performance metric is relevant in battery powered devices because the battery voltage decreases over time as it discharges. An example of a battery voltage and regulated voltage (V_{REG}) over time is shown in Fig. 2. Depending on battery chemistry, age, charge and other parameters, battery voltages can range from 1.5 V - 0.9 V for NiCd and NiMH based batteries and from 4.2 V - 2.7 V for lithium-ion [25].

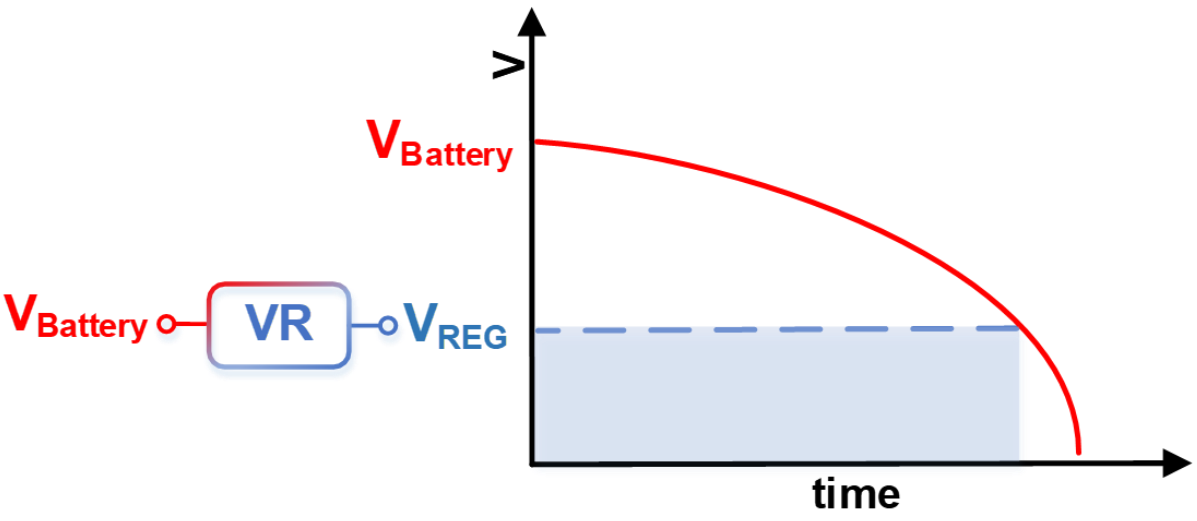


Fig. 2: Battery and regulated voltages over time

2.4.3 Load Regulation

Load regulation is the measure of ΔV_{OUT} due to a change in load current (ΔI_L) and can be expressed as in (4), where R_{OUT} is the open-loop output impedance of the CL-LDO [1]. This metric is measured once V_{OUT} has reached steady-state.

$$\left.\frac{\Delta V_{OUT}}{\Delta I_L}\right|_{t\to\infty} \approx \frac{R_{OUT}}{1+LG_0} \tag{4}$$

This metric considers the accuracy of V_{OUT} in CL-LDOs given that I_L changes depending on the amount of activity the load circuit has, for circuits processing large signals, or if the circuit, or part of it, is in stand-by or low-power mode.

2.4.4 Line Transient

Line transient measures V_{OUT} given a step change in V_{DD} with finite rise and fall times. It is also related to other metrics such as line regulation and PSR, where there is a strong correlation between line transient and PSR [1, 28]. Line transient, however, mainly focus on the region during the transient event and slightly after V_{DD} has reached its final step value. The main importance of this test is that it shows how the LDO reacts to sudden changes in V_{DD} that cannot be accounted for with a line regulation or PSR test. Strictly speaking, line regulation, PSR, and line transient test the dc, small-signal, and large-signal transfer functions from V_{DD} to V_{OUT}, respectively.

2.4.5 Load Transient

Load transient measures V_{OUT} given a step change in I_L with finite rise and fall times, as shown in Fig. 3. It is also related to load regulation. Load transient, however, mainly focus on the region during the transient event and slightly after I_L has reached its final step value. The main importance of this test is that it shows how the LDO reacts to sudden changes in I_L that cannot be accounted for with a load regulation test. Strictly speaking, load regulation and load transient test the dc and large-signal transfer functions from I_L to V_{OUT}, respectively. Load transient is strongly correlated to the LDO's output impedance and UGF [1].

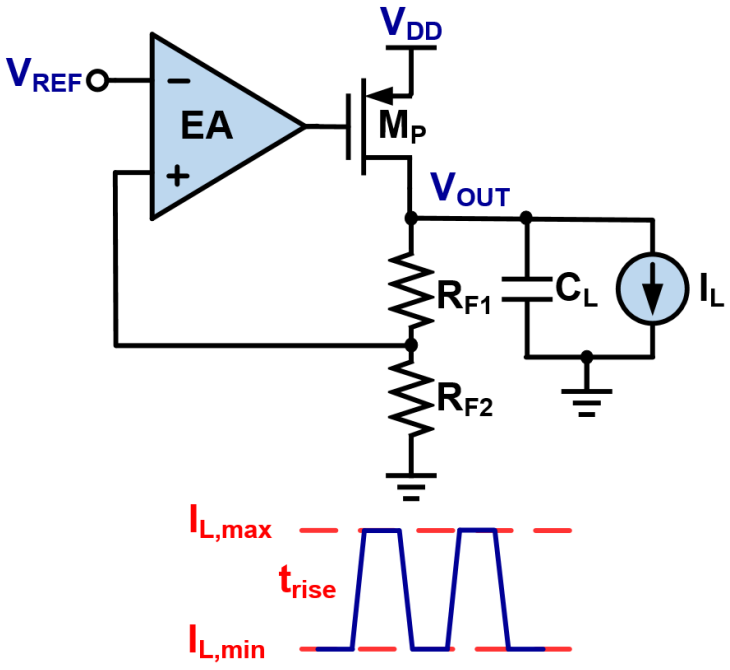


Fig. 3: LDO's load transient test

During a load transient event, V_{OUT} overshoots or undershoots depending on the polarity of ΔI_L. The maximum and minimum voltages along with the settling time (T_S) are the important points reported in comparison tables in the literature.

A load transient test is important because it tests the LDO's response to sudden changes in I_L. LDOs used in very dynamic systems, where the load is switched ON and OFF or where there are a lot of sudden I_L changes, find the information provided by this test useful.

2.4.6 Settling Time

The time it takes for V_{OUT} to settle within a certain percentage error after a transient event has occurred is called settling time (T_S). This is usually measured after a full load transient event since it is the one most likely to create the highest ΔV_{OUT}. This metric is important in systems that have circuits that have low-power modes. Circuits that are powered by LDOs have their own time constants and reaction times. The LDO has to be able to settle within a certain error before the circuit it uses starts processing a signal to prevent errors from the LDO to corrupting the signal.

As an example, let's assume an LDO is powering an analog-to-digital converter (ADC) and that at the initial state the ADC is OFF or in low-power mode. Then the ADC is going to be required for a conversion so the system turns it ON creating a load step event in the LDO. The ADC was designed, assuming an ideal V_{DD}, to have a turn-on time of 2 μs and a safety margin to start conversion of 1 μs, so 3 μs total. If an LDO with a long T_S were to be used, the ADC would have different V_{DD} values through the conversion process, creating errors in the data. To solve this either a faster LDO is required or more delay to start conversion is added to the ADC. From the LDO stand point, every active load is different and requires different specifications. Knowledge of the load and its requirements is often the starting point to designing an LDO.

2.4.7 Noise

Noise in LDOs include thermal, flicker, and shot noise. These are intrinsic properties of transistors and resistors that cannot be avoided and exist even if no other disturbances are present in the circuit. Noise is usually reported as spectral noise density, either at one specific frequency or a plot across all frequencies, or as integrated output noise, usually integrated over a specific frequency range [29]. Assuming the frequency range is the same, integrated output noise may be more useful when comparing two LDOs whenever noise is an important parameter.

The noise in a CL-LDO comes from V_{REF}, EA, and the feedback resistors. Therefore, the noise in a CL-LDO can be decreased by 1) filtering V_{REF} by using a large low-pass filter (LPF) between V_{REF} and the EA [29], 2) having a large transconductance (g_m) in EA's input pair, 3) and by decreasing the feedback resistor's value. The last two increase the CL-LDO's I_Q, which is limited by the specific application. The noise from resistors can be eliminated if the CL-LDO is used in unity-gain feedback configuration as proposed in [30]. The advantages and disadvantages of this configuration are explained in further detail in chapter III.

2.4.8 Efficiency

The efficiency (η) of a CL-LDO is calculated similarly to other voltage regulators and is given by:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{I_{OUT} V_{OUT}}{\left(I_{OUT} + I_Q\right) V_{DD}} \tag{5}$$

where P_{OUT}, P_{IN}, and I_{OUT} are the output power, input power, and output current, respectively. In practice, for CL-LDOs, efficiency is mostly determined by V_{IN-OUT} and I_Q. Both of those terms have to be minimized if a high efficiency is required. V_{IN-OUT} determines the efficiency when $I_{OUT} >> I_Q$, and ultimately, gives the best-case scenario for efficiency. When I_{OUT} is close or equal to zero, then efficiency drops and becomes very small. In those cases, keeping a very low I_Q becomes very important to extend battery lifetime.

From the system level perspective, V_{OUT} would come with a specific tolerance, usually in percentage change of nominal V_{OUT}, which needs to be met. This tolerance includes all previous performance metrics described so far, along with any other temperature, offset, and errors present in the system [26]. A more detailed discussion on LDO's performance metrics can be found in [1, 26]

2.5 State-of-the-art LDOs

Current state-of-the-art CL-LDOs only achieve high-PSR [2-8], fast T_S [9-12], or both but with high I_Q [13, 14], and therefore cannot properly address the issues present in power efficient noise sensitive applications [16].

2.5.1 High-PSR CL-LDOs

LDOs that target high PSR performance without adding devices in the high-power path can be roughly divided into four categories as shown in Fig. 4. Where V_{DD}, V_{OUT}, and V_{REF} are the LDO's supply, output and reference voltages; respectively, and LDO's EA, pass device (M_P), feedback resistors (R_{F1} and R_{F2}), load resistance (R_L), load capacitor (C_L), and K represents a feedback or feed-forward gain. These approaches are: Gate-driven feedback (GDFB) LDOs (Fig.

4a) [4-7], gate-driven feed-forward (GDFF) LDOs (Fig. 4b) [3, 31], bulk-driven feedback (BDFB) LDOs (Fig. 4c) [13], and bulk-driven feed-forward (BDFF) LDOs (Fig. 4d) [2].

GDFB LDOs (Fig. 4a) have multiple feedback loops that decrease V_{DD} ripple at V_{OUT} by increasing the regulation LG, unity-gain frequency (UGF), or both. The CL-LDO presented in [4] achieved a LG and UGF of 100 dB and 10 MHz, respectively, at an I_L of 100 mA. However, the PSR performance at high frequency deteriorates fast with a measured PSR of −16 dB at 1 MHz.

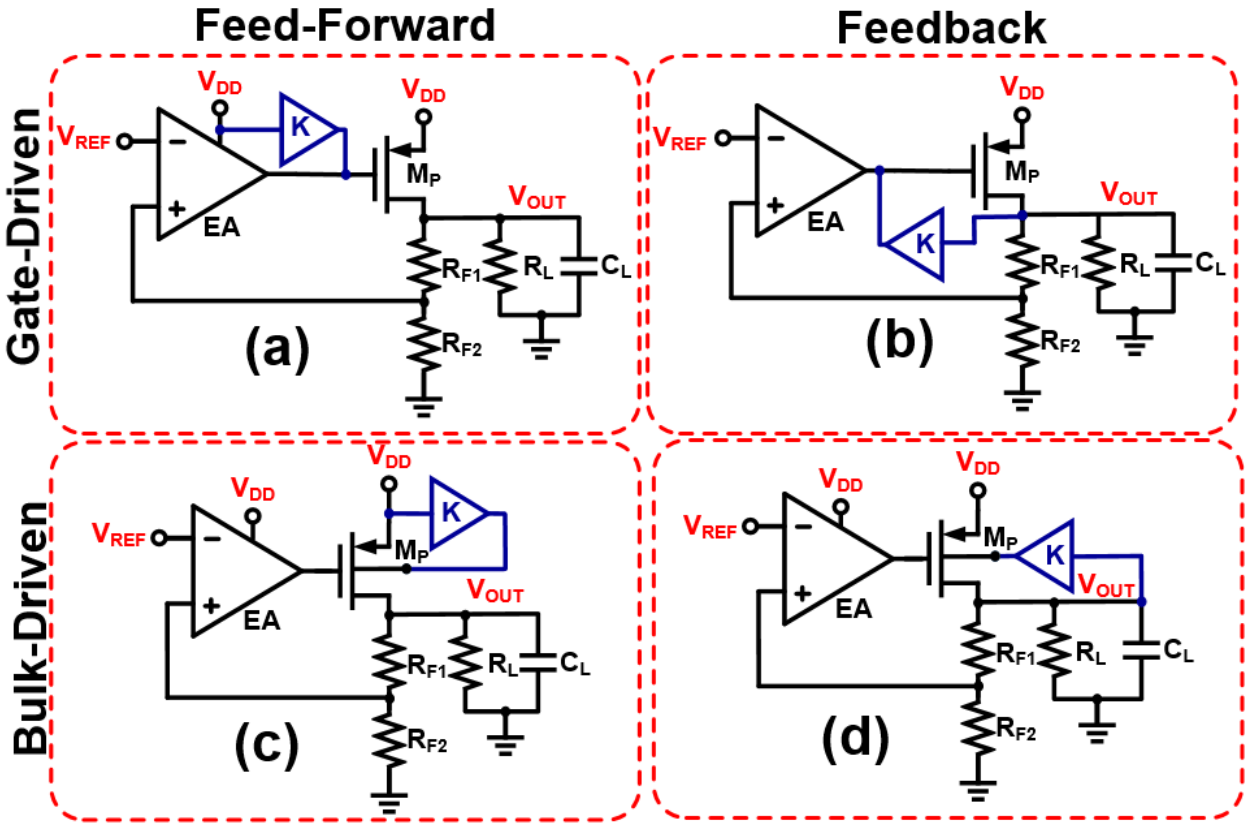


Fig. 4: LDO's PSR enhancement approaches: (a) gate-driven feedback (GDFB), (b) gate-driven feed-forward (GDFF), (c) bulk-driven feedback (BDFB), and (d) bulk-driven feed-forward (BDFF)

In GDFF LDOs (Fig. 4b) a weighted version of V_{DD}'s ripple is injected at M_P's gate. If the gate's ripple tracks the source's ripple properly (which is connected to the V_{DD} in a PMOS M_P implementation), then, no ripple is introduced at V_{OUT} by the M_P's transconductance (g_m) due to a zero V_{GS}. Then, the only source of V_{DD} noise in GDFF LDOs comes from the M_P's output conductance (g_{ds}). The CL-LDO presented in [3] used a PSR enhancer that achieved a minimum of − 50 dB PSR up to 4 MHz for different I_L and PVT variations with an internal capacitor of 28 pF, which occupies significant on-chip area. The PSR enhancer itself required 24 pF.

Bulk-driven (BD) LDOs are usually implemented using a PMOS M_P. This is due to the easy access to the PMOS' bulk terminal compared to NMOS, which would require a triple-well process for independent bulk access. In BDFB LDOs (Fig. 4c), an additional feedback path is introduced through the M_P's bulk terminal. A PSR of − 93 dB at 1 kHz was achieved by [13]; however, the CL-LDO had a low phase margin (PM) at no I_L and presented oscillations during I_L transients. Also, the maximum I_L was limited to 5 mA.

In BDFF LDOs (Fig. 4d), a weighted version of V_{DD}'s ripple is introduced through the M_P's bulk terminal via a feed-forward EA. This uses the M_P's bulk transconductance (g_{mb}) as an additional gain stage to cancel V_{DD}'s ripple at V_{OUT}. It was previously suggested in [2]; however, that no theoretical or experimental results were presented. BD has been used in other applications [18, 19, 32] successfully; therefore, we further explore this approach together with additional techniques for low-power applications.

2.5.2 Fast Settling Time CL-LDOs

Fast-T_S CL-LDOs are obtained by using improved frequency compensation such as that found in [9], where a damping-factor-control frequency compensation was used, or by increasing the available slew rate current [10-12].

The CL-LDO presented in [9] had the advantage of stable operation with a C_L or without one. However, for it to be stable without a C_L, it needed a minimum I_L of 1 mA. The LDO achieved a T_S = 2 μs for a 10−100 mA I_L step in a 1 μs rise time. This prohibits its use in low-power circuits where a shutdown is used to save power during idle times.

A CL-LDO with adaptive biasing and dynamic charging is presented in [10]. Adaptive biasing is used to improve the frequency response and increase the charging current with high I_L. The dynamic charging technique used an RC network as a high-pass filter to instantly sense the sudden I_L changes and injected additional current in the EA to quickly respond. The CL-LDO achieved a T_S = 150 ns for a 0−100 mA I_L step in a 500 ns rise time. However, the paper overlooked PSR, and its importance in rejecting V_{DD} noise. Furthermore, no PSR results were shown, which makes it hard to compare with other implementations.

A novel push-pull buffer stage to drive M_P is introduced in [11]. The buffer stage increased the available slew rate current at M_P's gate, which improved the response time to sudden I_L changes without increasing I_Q. The LDO achieved a T_S = 1.2 μs for a 0−50 mA I_L step in 100 ns rise time. However, the low-frequency and high-frequency PSR were – 46 dB and around – 2 dB at 1 MHz, respectively. This limits the implementation when used after efficient switching dc-dc converters used in modern PMICs.

In [12], a fast self-reacting CL-LDO is presented. The implementation used three fast loops to achieve a fast response time with a main loop for high gain and voltage regulation. The

LDO achieved a T_S = 1 μs for a 0−100 mA I_L step in 1 μs rise time. However, its PSR was − 60.6 dB and − 39.5 dB at 1 kHz and 10 kHz, respectively.

2.6 Conclusion

LDOs are ubiquitous in current analog circuits inside system-on-chip (SoC) circuits. Their diverse set of performance metrics and wide-range of applications make them a must-know for analog circuit designers. This is because each application and load circuit would require such a particular set of requirements that will eventually lead to designing an LDO for every critical analog path in a system.

The ever increase in complexity, density and use of integrated circuits (ICs) in every day applications only leads to a larger use of LDOs. Therefore, knowledge of the terminology discussed in this chapter proves useful, even for those not directly involved in the design of LDOs.

CL-LDOs are often preferred in such complex and compact systems due to their lack of external capacitors. Current state-of-the-art CL-LDOs tend to focus on one particular metric often neglecting, or even worsening, others in the process. High-performance CL-LDOs used in SoC systems usually require several of their performance metrics to be good. The next chapter discusses a CL-LDO with good PSR and T_S.

CHAPTER III

PSR ENHANCED WITH FAST SETTLING TIME BULK-DRIVEN FEEDFORWARD LDO REGULATOR*

3.1 Introduction

Power efficient system-on-chip (SoC) solutions are a vital part of state-of-the-art electronic devices as technology improves and more functions can be integrated on a single chip. To increase battery life and save energy, circuit functions inside the chip are only used when needed and remain off the rest of the time. An example of such functions include built-in testing capabilities for both analog and digital systems inside SoC solutions [33-36]. In addition, SoC solutions require the full integration of low-power power management integrated circuits (PMICs) [37].

Today's PMICs are often a combination of efficient switching dc-dc converters and low noise low dropout regulators (LDOs) to generate multiple clean supplies across the chip. Due to stringent latency requirements and their critical performance, modern systems that contain blocks such as precision analog-to-digital converters (ADCs), dynamically-switched RF power amplifiers [38], and voltage-controlled oscillators (VCOs) require very clean and high performance voltage supplies [39-41]. For that reason, LDOs used in this embedded systems need to have fast settling time (T_S) while still maintaining high power supply rejection (PSR) and low noise.

Capacitor-less LDOs (CL-LDOs) are preferred for SoC solutions since they can be fully integrated with no external components, and as a result bill of material (BoM) and printed circuit board (PCB) area are reduced. For CL-LDOs, the load capacitance (C_L) represents the load circuit's parasitic capacitance and is not required for stability purposes because an internal Miller compensation approach is used to stabilize the CL-LDO's loop. Moreover, the high PSR range needs to include from low frequencies up to the dc-dc converters' switching frequencies, which can be in the low megahertz range. SoCs also have critical blocks with a shutdown mode to save power and increase battery life when they are not required, which introduce load current (I_L) changes to LDOs. CL-LDOs require fast T_S to respond to quick I_L changes without impacting the load circuit's performance.

3.1.1 Proposed CL-LDO

The low quiescent current (I_Q) gain-boosted CL-LDO with the bulk-driven feedforward (BDFF) supply voltage (V_{DD}) noise cancellation technique presented herein improves PSR at mid-range frequencies, from 10 kHz and up to 5 MHz, and achieves a fast T_S by using a novel adaptive compensation based on I_L tracking.

The high loop gain (LG) from the main error amplifier (EA) attenuates V_{DD} noise at lower frequencies. The CL-LDO presented in this chapter achieves a $-$ 90 dB low frequency and $-$ 64 dB at 1 MHz PSR CL-LDO. Test results proved that the BDFF path can achieve a high frequency PSR improvement by 35 dB at 1 MHz and 20 dB up to 5 MHz. In addition, the CL-LDO uses a gain-boosted EA with an adaptive biasing buffer stage, an I_L-dependent Miller compensation scheme, and a bulk-biased linear pass transistor (M_P). Its unity-gain feedback loop configuration

is shown in Fig. 5. These techniques, which are used to enhance the control loop characteristics at high I_Ls, help to improve LG, line/load regulation, transient performance, T_S, and noise.

Overall the M_P's size is decreased by almost 50% achieving a 62.5% gate capacitance reduction, as explained in subsection 4.1, and the T_S is decreased by more than 60%. A fast T_S of 300 ns is achieved due to the improvements made in area and unity-gain frequency (UGF) increase. Furthermore, an extended C_L range (0−400 pF) increases the amount of circuits that can be powered using the proposed CL-LDO, where C_L represents the load circuit's parasitic capacitance and is not required for stability purposes because an internal Miller compensation approach is used to stabilize the internal CL-LDO's loop.

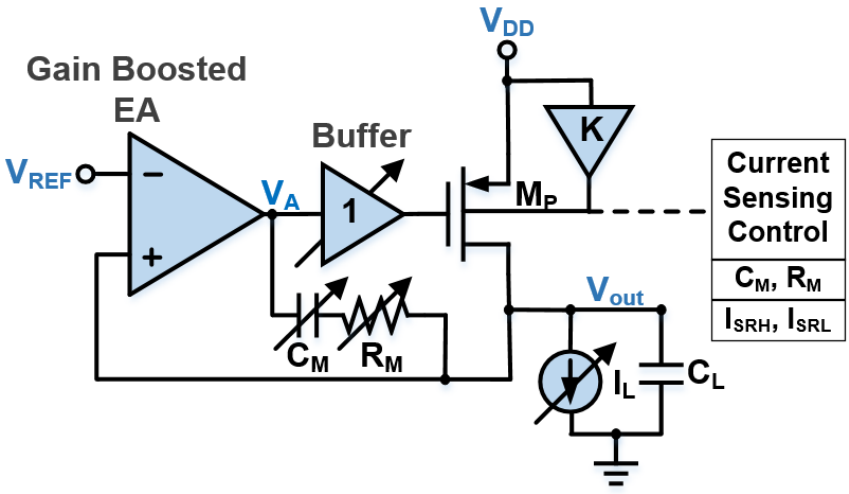


Fig. 5: Proposed LDO topology with M_P in linear (ohmic) region and adaptive scheme.

Reprinted from [16]

The chapter is organized as follows. Section 2 presents a PSR analysis for CL-LDOs. Section 3 discusses T_S improvement approaches. Section 4 discusses circuit implementation and proposed techniques. Measurement results are shown in Section 5, and finally, conclusions are given in Section 6.

3.2 PSR Analysis in Capacitor-less LDOs

CL-LDOs are commonly built using a set of five blocks. These blocks are: a reference voltage (V_{REF}), EA, M_P, frequency compensation, and a feedback network. Fig. 6 shows the block diagram of the CL-LDO shown in Fig. 1, where the transfer function from V_{REF} to the output voltage (V_{OUT}) and from V_{DD} to V_{OUT} are given by:

$$\frac{V_{OUT}}{V_{REF}} = \left.\frac{A_{EA}A_{PT}}{1+A_{EA}A_{PT}\beta}\right|_{\text{If } A_{EA}A_{PT}\gg 1} \approx \frac{1}{\beta} \tag{6}$$

$$\frac{V_{OUT}}{V_{DD}} = \left.\frac{1}{1+A_{EA}A_{PT}\beta}\right|_{\text{If } A_{EA}A_{PT}\gg 1} \approx 0 \tag{7}$$

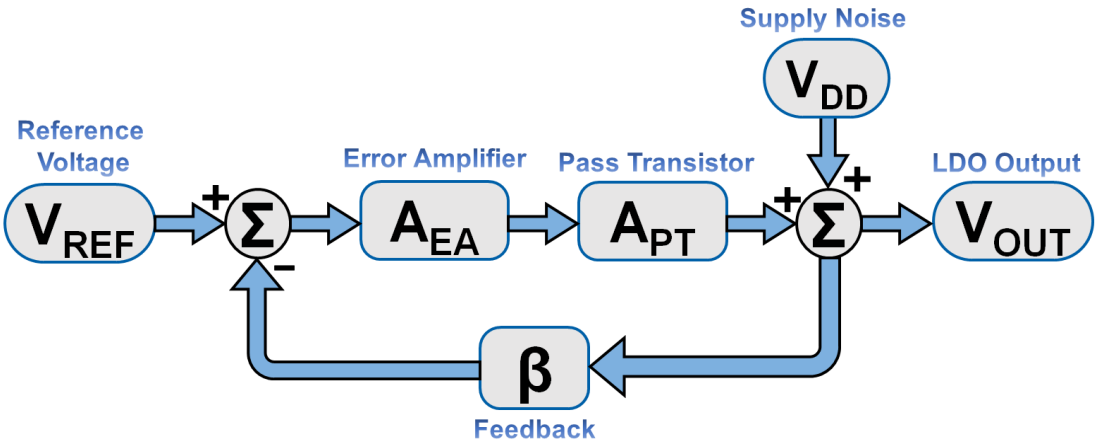


Fig. 6: Basic LDO block diagram

where A_{EA} is the EA's low frequency gain, A_{PT} is the M_P's dc gain, β is the feedback factor given by $R_{F2}/(R_{F1}+R_{F2})$ and $A_{EA}A_{PT}\beta$ is the loop's low-frequency LG. In (6) and (7) the EA's gain was assumed sufficiently high so that $A_{EA}A_{PT}\beta >> 1$. In this case, even with variations present in V_{DD}, the closed-loop regulator maintains a fixed output. Eq. (6) and (7) show that as LG increases the PSR improves, but noise from V_{REF} remains constant; hence the need for a V_{REF} with high power supply rejection ratio (PSRR). However, assuming a passive low pass filter (LPF) is used at V_{REF}'s output [28], this V_{DD} noise path can be neglected since it is significantly attenuated.

The feedback network is usually a linear and frequency independent resistive divider; although frequency dependent feedback networks have also been used. For instance, in [5] the feedback network was implemented with active devices, while in [6] an additional capacitor in parallel with R_{F2} was added to increase the regulation loop's phase margin (PM). These types of feedback networks attenuate the signal and thus, the CL-LDO's LG and UGF are reduced.

In [30], a unity-gain buffer configuration is proposed to improve closed-loop characteristics if a good PM can be maintained. An adjustable V_{REF} is used to select the desired

V_{OUT}. An additional advantage to this approach is the savings in area and noise that are obtained by avoiding feedback resistors. The unity-gain buffer CL-LDO configuration makes $\beta = 1$, and increases the EA's design stability constraints.

M_P can be implemented with an NMOS or PMOS device. An NMOS implementation offers better frequency performance when compared to PMOS [27]. However, they suffer from high dropout voltage (V_{DO}) since they require a gate voltage that is higher than V_{OUT} at the NMOS source. This is usually accomplished by using a charge pump (CP) to increase the supply and properly bias the NMOS gate. For this reason, a PMOS M_P is the preferred choice in most low voltage applications [27].

For a CL-LDO with PMOS M_P, the noise that couples to V_{OUT} and limits the low-frequency PSR comes from four different sources [31]. Shown in Fig. 7, these four sources are 1) V_{REF}, 2) finite EA PSRR, 3) M_P's transconductance (g_m) and 4) M_P's drain-to-source resistance (r_{ds}). The EA's contribution to PSR degradation in CL-LDOs was studied in [27], where the concept of Type-A and Type-B EAs was first introduced. Type-A EAs couple V_{DD} noise to their output whereas Type-B EAs isolate V_{DD} noise from their output, where examples of both are shown in Fig. 8. For that reason, a CL-LDO using a Type-A EA provides a high PSR at dc; however, they suffer from limited PSR bandwidth (BW) [1].

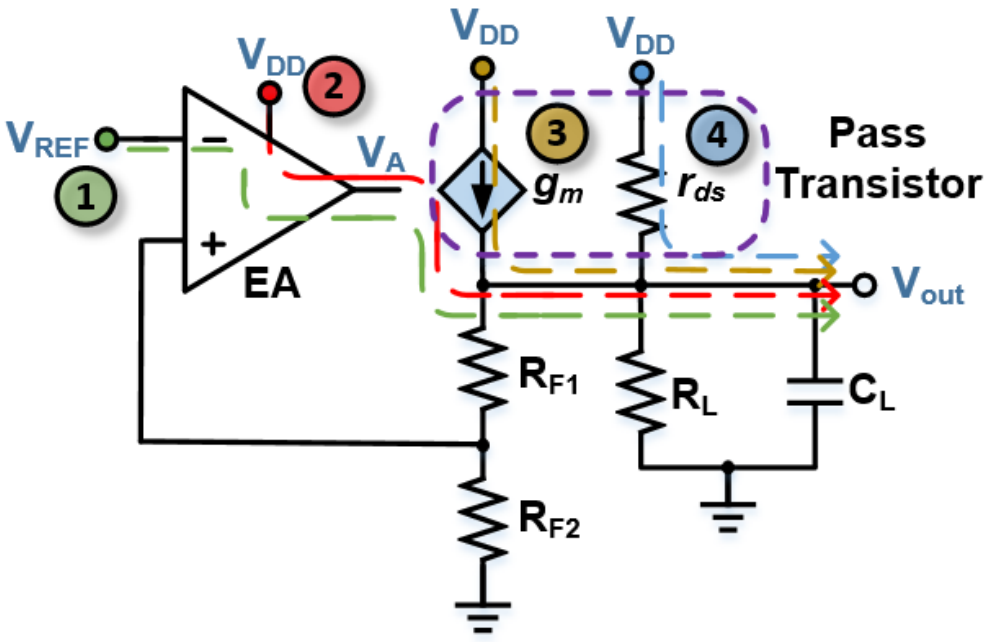


Fig. 7: PMOS CL-LDO PSR low frequency paths

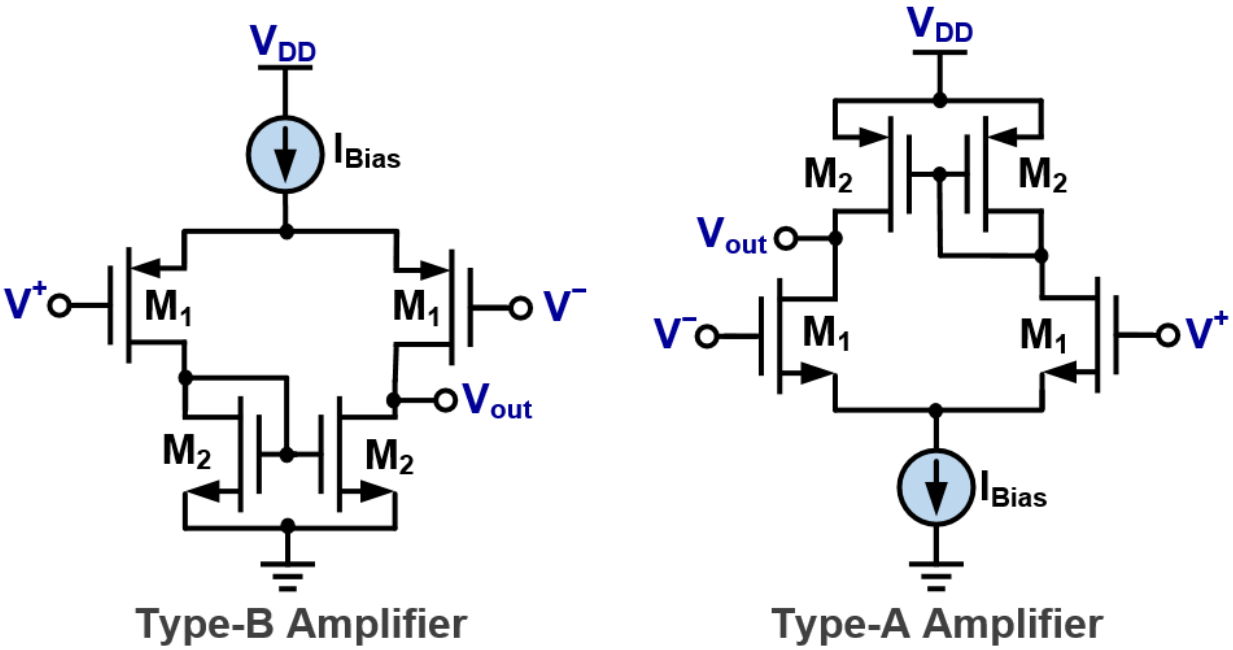


Fig. 8: Examples of type-A and type-B EAs

Table 1 shows PSR at dc, PSR BW, and the main advantage points for M_P and EA's combinations as defined in [27]. EA is the open loop PSR ($A_{EA,PSR}$) as defined in [1], and BW_{EA} is the EA's 3 dB BW.

Table 1: CL-LDO PSR properties for a given M_P and EA

Pass Device	**Error Amplifier**	**DC PSR [27]**	**PSR BW [27]**	**Main Advantage [27]**	**$A_{EA,PSR}$ [1]**
PMOS	Type-A	$\frac{1}{\beta A_{EA} A_{PT}}$	BW_{EA}	High DC PSR	1
PMOS	Type-B	$\frac{1}{\beta A_{EA}}$	$A_{PT}BW_{EA}$	High PSR BW	0
NMOS	Type-A	$\frac{1}{\beta A_{EA}}$	$A_{PT}BW_{EA}$	High PSR BW	1
NMOS	Type-B	$\frac{1}{\beta A_{EA} A_{PT}}$	BW_{EA}	High DC PSR	0

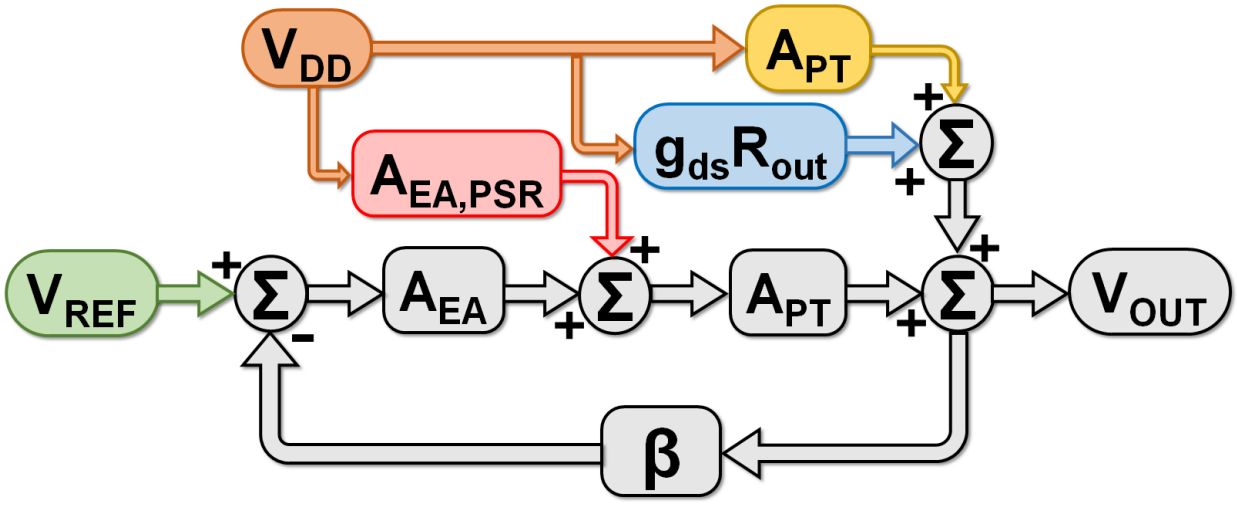


Fig. 9: PSR block diagram for a CL-LDO analysis with a PMOS M_P

Fig. 9 shows a block diagram of a basic PMOS CL-LDO as shown in Fig. 7, which includes the four paths that contribute to PSR degradation. Using Fig. 9, the PSR transfer function at dc including the four paths is given as:

$$PSR_{DC} = \frac{\left(g_m + g_{ds} + A_{EA}g_m - A_{EA,PSR}g_m\right)R_{OUT}}{1+LG} \tag{8}$$

where $R_{OUT} = r_{ds}//R_L$ is the total impedance seen at V_{OUT} and $A_{EA,PSR} \approx 1$ or 0 [1]. To achieve a high PSR, (8) needs to approach zero. This can be achieved by increasing LG or by decreasing the terms in the numerator. Increasing LG is the favored option since it comes with additional improvements to line/load regulation and transient [1] at the expense of extra I_Q. However, as technology scales, the intrinsic gain of transistors decreases, and high gain stages are harder to obtain. For CL-LDOs, high gain and UGF are necessary to improve the PSR at high frequencies. The CL-LDO's required UGF to maintain good PM ultimately limits the high frequency PSR. In the end, if PSR improvement is desired, then V_{DD}'s noise paths have to be cancelled or greatly attenuated. In this work a feed-forward path is used to achieve high PSR without altering the CL-LDO's loop stability while adaptively keeping a low I_Q relative to I_L.

3.2.1 PSR Analysis of Bulk-Driven Feed-Forward (BDFF) LDO

The two techniques used to improve PSR are gain-boosting around the main EA and a BDFF supply noise path, which improve the PSR as shown in Fig. 10. The BDFF coefficient can be selected in such a way to optimize either low-frequency PSR, PSR_{DC}, as illustrated in Fig. 10

sketch No. 4, or PSR BW, PSR_{BW}, as illustrated in Fig. 10 sketch No. 3. A detailed PSR analysis of these two options is presented hereafter.

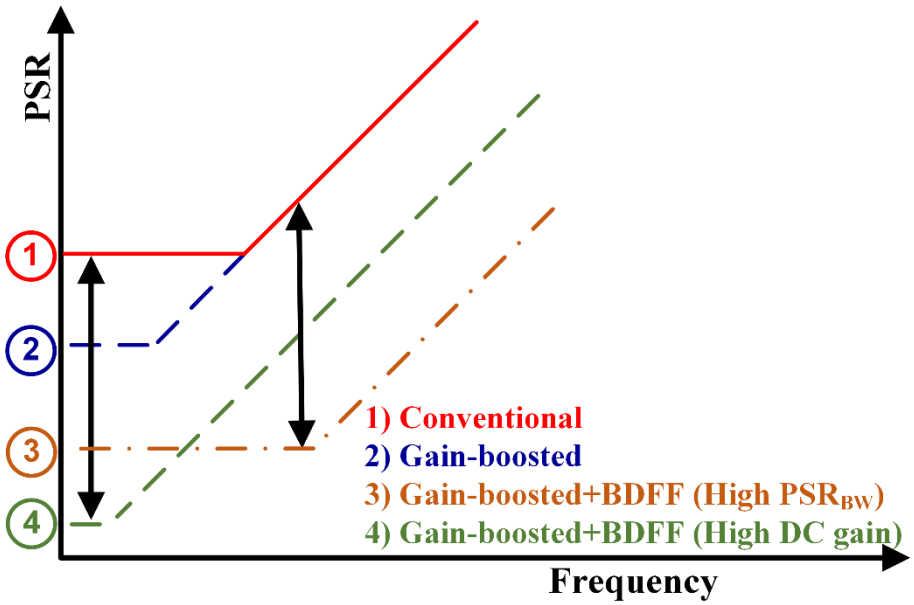


Fig. 10: CL-LDO's conventional PSR (sketch No. 1), CL-LDO's improved PSR with gain-boosting (sketch No. 2), CL-LDO's improved PSR with gain-boosting and BDFF optimized for PSR BW by using (19) (sketch No. 3), CL-LDO's improved PSR with gain-boosting and BDFF optimized for low-frequency PSR by using (14) or (15) (sketch No. 4). Reprinted from [16]

One of the proposed technique's goals is to enhance the CL-LDO's PSR. Thus, decreasing the terms in the numerator of (8) is very important. After assuming V_{REF} has been properly low-pass filtered the PSR can be approximated as:

$$PSR_{DC} \approx \frac{\left(g_m + g_{ds} - A_{EA,PSR} g_m\right) R_{OUT}}{1+LG} \tag{9}$$

$$PSR_{DC} \approx \frac{g_{ds} R_{OUT}}{1+LG} \qquad \text{Type-A EA [1]} \tag{10}$$

$$PSR_{DC} \approx \frac{\left(g_m + g_{ds}\right) R_{OUT}}{1+LG} \qquad \text{Type-B EA [1]} \tag{11}$$

where if designing a Type-A/Type-B EA, the designer can use $A_{EA,PSR} \approx 1$ or 0 [1], arriving to the results shown in (10)-(11). Note that $A_{EA,PSR}$ exact value depends on EA's transistor-level implementation.

To improve PSR, the proposed feed-forward approach tries to cancel the terms in the numerator of (9). Fig. 4d shows the CL-LDO's system-level architecture with the BDFF technique. The feed-forward signal at M_P's bulk is a weighted version of V_{DD} multiplied by a feed-forward coefficient, K. The BDFF CL-LDO's small signal model is shown in Fig. 11, and (12) shows the PSR transfer function, derived in the appendix A, where g_{mb}, C_{gs}, and C_{gd} are the M_P's bulk transconductance, gate-source capacitance, and gate-drain capacitance, respectively, and r_{oA} is the main EA's output impedance.

It has been assumed that the main EA acts as a type-B EA, which is explained in detail in subsection 4.2, and that the feed-forward coefficient circuit has a low enough output impedance to push M_P's parasitic capacitances located at the bulk node to frequencies beyond the CL-LDO's UGF, as explained in more detail in subsection 4.6. The low-frequency PSR, poles and zeros are given in (13).

$$PSR(s) \approx \frac{C_{gd}C_{gs}s^3 + \left[(C_{gs}+C_{gd})(\Delta K - g_m) + g_m C_{gd}\right]s^2 + g_{oA}\Delta K s + g_{oA}\omega_o \Delta K}{C_L(C_{gs}+C_{gd})s^3 + \left[(g_{ds}+g_L)(C_{gs}+C_{gd}) + C_{gd}g_m + g_{oA}C_L\right]s^2 + g_{oA}(g_{ds}+g_L)s + A_0 g_m g_{oA}\omega_o} \quad (12)$$

$$PSR_{DC} = \frac{\Delta K R_{out}}{1+LG} \qquad \Delta K = g_m + g_{ds} + g_{mb} - Kg_{mb}$$

$$\omega_{z1} \approx \omega_0 \quad \omega_{z2} \approx \frac{\Delta K}{(C_{gs}+C_{gd})(\Delta K - g_m)} \quad \omega_{z3} \approx \frac{(C_{gs}+C_{gd})(\Delta K - g_m)}{C_{gs}C_{gd}} \quad (13)$$

$$\omega_{p1} \approx \frac{A_o \omega_o g_m}{g_{ds}+g_L} \quad \omega_{p2} \approx \frac{C_{gd}g_m + (C_{gs}+C_{gd})(g_{ds}+g_L)}{C_L(C_{gs}+C_{gd})} \quad \omega_{p3} \approx \frac{g_{oA}}{C_{gs}+C_{gd}+\frac{C_{gd}g_m}{C_{gs}+C_{gd}}}$$

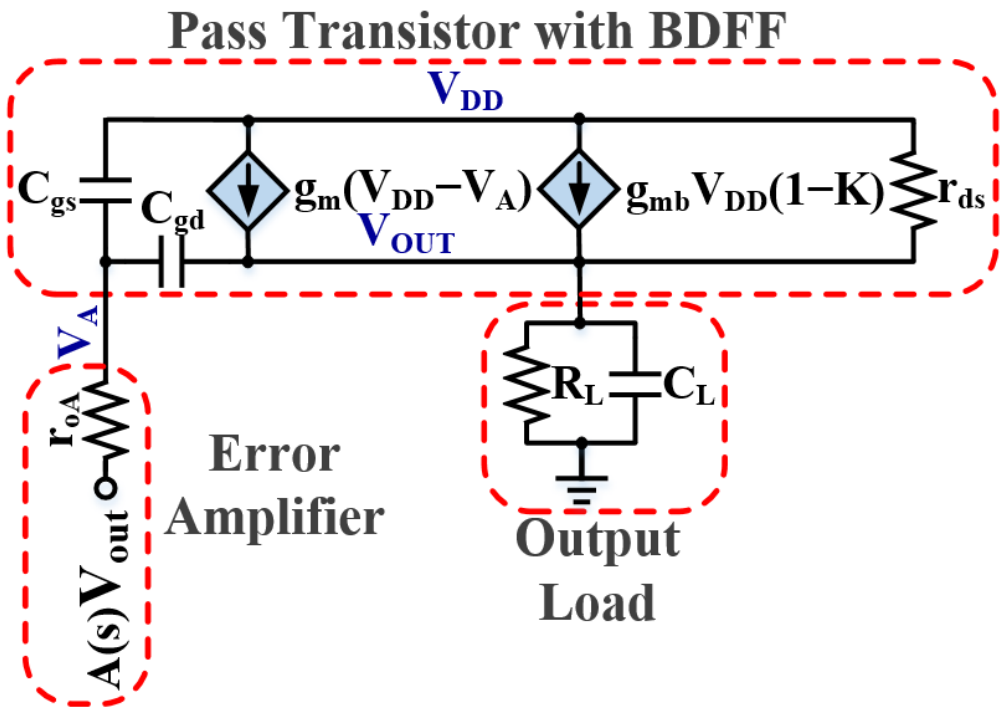


Fig. 11: Bulk-driven feed-forward (BDFF) CL-LDO's output stage PSR small signal model.

Reprinted from [16]

The system's poles can be found in the PSR formula and can be used to determine system's stability. It can be seen from the denominator of (12) that the BDFF technique does not affect the closed-loop poles' location or the system's stability, which is a general advantage of feed-forward techniques compared to feedback techniques.

The bulk modulation technique presented in [13] uses a feedback path through M_P's bulk terminal, which presents additional stability concerns due to its feedback nature. The idea proposed herein also uses the bulk terminal but with a feed-forward implementation, which as shown in (12) does not affect stability. Another difference is that the proposed BDFF only applies the required feed-forward coefficient to improve PSR, whereas in [13], the feedback includes the EA's full dc gain.

It can be seen from (13) that a tradeoff exists between PSR BW and low-frequency PSR attenuation, as ΔK decreases PSR_{DC} improves but the second zero, ω_{z2}, moves towards lower frequencies. If the ideal K_{DC} were to be used the PSR_{DC} magnitude would be zero with ω_{z2} moving to the origin. This is conceptually shown with sketches No. 3 and 4 in Fig. 10, where a higher low-frequency PSR would sacrifice PSR BW. The ideal and implemented K for this design and design tradeoffs are further addressed below.

To maximize PSR improvement, (14) shows the required ideal feed-forward coefficient, K_{DC}, to make PSR_{DC} equal to zero in (12).

$$K_{DC} = 1 + \frac{g_{ds}}{g_{mb}} = 1 + \frac{g_{ds}}{\chi\, g_m} = 1 + \frac{1}{\chi A_{PT}} \quad \text{Type-A EA [1]} \tag{14}$$

$$K_{DC} = 1 + \frac{g_m + g_{ds}}{g_{mb}} = 1 + \frac{g_m + g_{ds}}{\chi\, g_m} = 1 + \frac{1}{\chi} + \frac{1}{\chi A_{PT}} \quad \text{Type-B EA [1]} \tag{15}$$

where A_{PT} and χ are the M_P's intrinsic gain and threshold voltage (V_T) rate of change with bulk-to-source voltage (V_{BS}) as defined in [42], respectively. As shown in (14)-(15), the ideal K_{DC} needed for perfect cancellation at low-frequencies could range between 3 ~ 5 depending on M_P's size, technology, and CL-LDO's maximum I_L. This feed-forward coefficient is higher compared to gate driven feed-forward techniques because g_{mb} is smaller than g_m.

Traditional feedforward gate driven techniques, where the feedforward is introduced in M_P's gate, require a smaller feedforward gain because the feedforward coefficient is divided by M_P's transconductance. The formula for those cases is provided by

$$K_{DC,GateDriven} = 1 + \frac{g_{ds}}{g_m} = 1 + \frac{1}{A_{PT}} \tag{16}$$

However, in the proposed technique the feedforward is introduced through M_P's body/bulk which modifies the feedforward gain to those given in (14) and (15). These are higher because the body transconductance ($g_{mb} = \chi g_m$) is lower than g_m. A more realistic scenario can be expressed as (17), where a real gain coefficient (K_R) with an additional gain error (ε), given by $K_R = K_{DC} \pm \varepsilon$, is used instead of K_{DC} in (12).

$$PSR_{DC} \approx \frac{\varepsilon g_{mb} R_{out}}{1 + LG} \tag{17}$$

PSR_{DC} from (9) has now been reduced to (17) which depends on the product of ε and g_{mb} and is significantly smaller than the numerator in (9). More importantly, an additional degree of freedom was introduced to a CL-LDO's PSR. Before the BDFF path, the LG was the only

parameter to improve PSR, with the BDFF technique, ε can be used to improve PSR without affecting the CL-LDO's loop, PM, or UGF. To get more insight, (17) can be further simplified by assuming LG is higher than one, using (14) and the fact that g_{mb}/g_m is typically between 0.1 and 0.3 [42]. The proposed BDFF LDO's PSR_{DC} magnitude, as expressed in (18), only depends on the gain error between ideal and actual feed-forward coefficient.

$$PSR_{DC} \approx \frac{\varepsilon}{A_{EA}\beta}\left(\frac{g_{mb}}{g_m}\right) \approx \frac{0.3\varepsilon}{A_{EA}\beta} \tag{18}$$

Assuming LG has been fixed for a given PM and UGF, (18) can be used to determine the required error that meets the target PSR_{DC} specifications. It can also be observed, in (18), that a β =1 maximizes the CL-LDO's PSR.

An important tradeoff between low-frequency and high-frequency PSR can be seen by analyzing the feed-forward's effect from the PSR formula in (12). From the numerator, or zeros, it can be seen that as K approaches K_{DC}, the second zero is moved to lower frequencies. At the ideal K_{DC}, the zero is pushed all the way to the origin. This combined together with the low-frequency EA pole, which appears as a zero in the PSR, starts degrading the PSR gain at – 40 dB/decade if the optimal value of K_{DC} is used. The ideal and implemented K for this design and design tradeoffs are further addressed in subsection 4.4.

Shown in Table 2 are the PSR_{DC} for all Type-A, Type-B and proposed BDFF LDOs. Type-B EA's PSR_{DC} is inversely proportional to the LDO's $A_{EA}\beta$ product, while Type-A EAs further decrease PSR_{DC} by the M_P's intrinsic gain (A_{PT}), which is I_L dependent.

Table 2: CL-LDO PSR for type-A, type-B and BDFF LDOs

	Type-B	Type-A	Proposed
PSR_{DC}	$\frac{1}{\beta A_{EA}}$	$\frac{1}{\beta A_{EA} A_{PT}}$	$\frac{0.3\varepsilon}{\beta A_{EA}}$

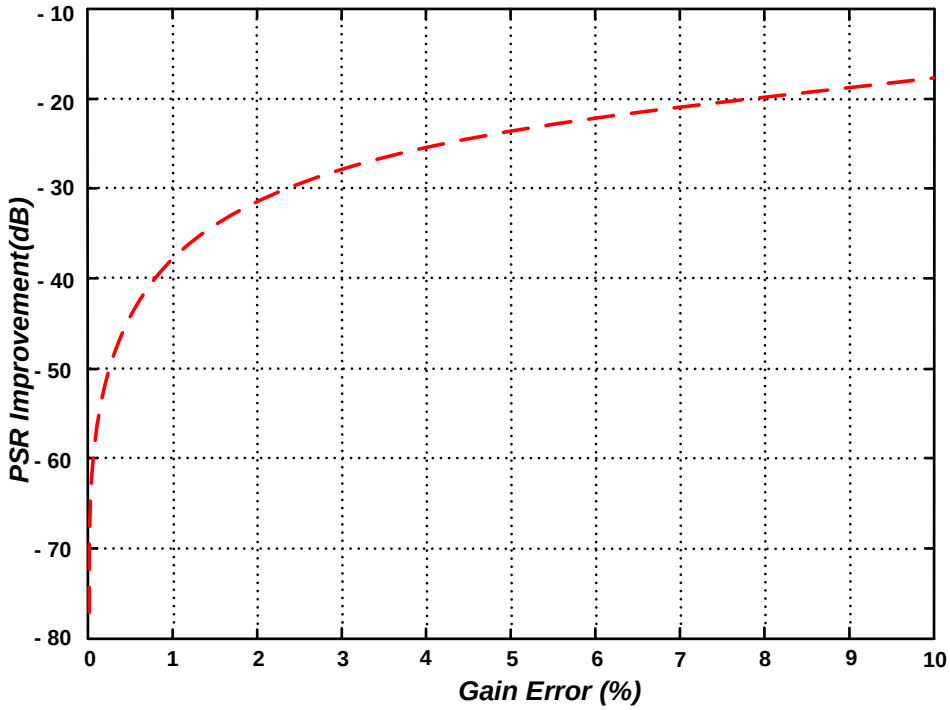


Fig. 12: PSR improvement versus gain error (ε) in percentage

PSR_{DC} with the proposed CL-LDO depends on the error between ideal and real feed-forward coefficients, i.e. ε, and the CL-LDO's $A_{EA}\beta$ product. As long as the proposed CL-LDO tracks the ideal feed-forward coefficient across I_L, the PSR_{DC} is closer to zero compared with either Type-A or Type-B. Fig. 12 shows the PSR improvement versus ε in percentage for the proposed BDFF LDO. From Fig. 12, the required error tolerance can be determined for the feed-forward

path. Fig. 13 compares the simulated PSR_{DC} for the conventional and proposed CL-LDO with all the PSR improvement techniques being used.

In order to maximize PSR_{BW} instead of PSR_{DC}, the zero introduced by the BDFF technique needs to create a complex conjugate pair in the PSR transfer function. This condition occurs when K is given by (19), which is derived in the appendix A, and is smaller in magnitude to K_{DC} required to maximize PSR_{DC}. Therefore, as shown in (14) or (15) and (19), two choices are possible with the proposed feed-forward technique. These are either to maximize the low-frequency PSR, PSR_{DC}, by using K_{DC}, or to maximize the PSR BW, PSR_{BW}, by using K_{BW}.

Fig. 14 shows a simulation plot of PSR_{DC} and PSR_{BW} versus K. The two different points can be observed, as K is increased, the PSR_{BW} achieves its maximum at K = 2.5, whereas the maximum PSR_{DC} is achieved at K = 4. A tradeoff exists since only one of these PSR characteristics, PSR_{BW} or PSR_{DC}, can be maximized. In this paper, PSR_{BW} was maximized, by implementing K_{BW}, instead of PSR_{DC}.

$$K_{BW} = 1 + \frac{1}{\chi} + \frac{1}{\chi A_{PT}} - \frac{2C_{gs}C_{gd}g_{oA}}{g_{mb}\left(C_{gs}+C_{gd}\right)^2} - \frac{C_{gs}}{\chi\left(C_{gs}+C_{gd}\right)} \tag{19}$$

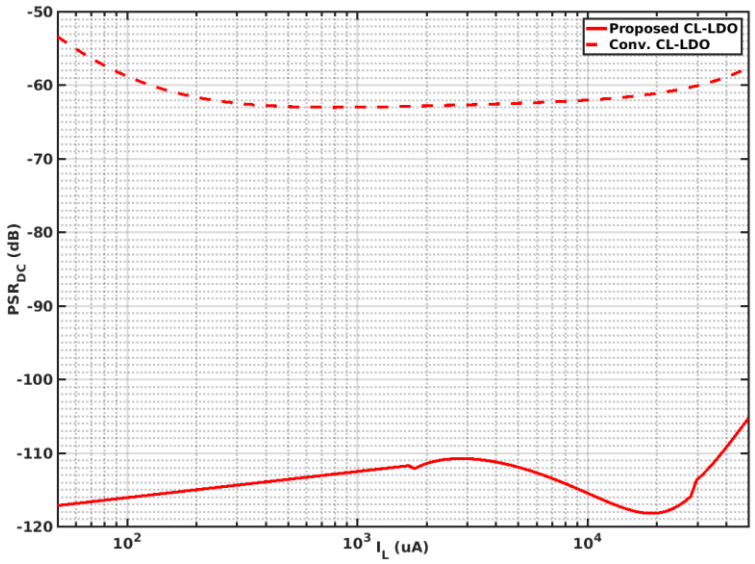


Fig. 13: Conventional versus BDFF CL-LDO's simulated PSR_{DC} versus I_L. V_{DD} = 1.2 V, V_{OUT} = 1 V. Reprinted from [16]

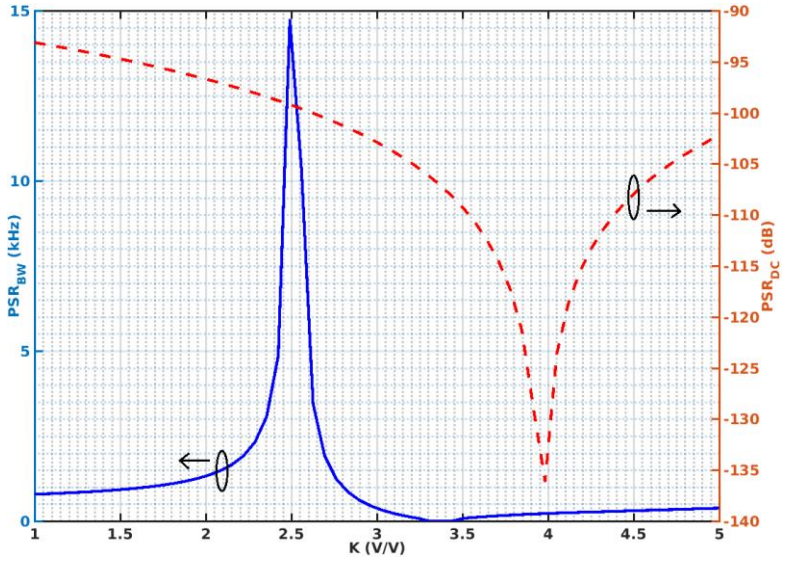


Fig. 14: CL-LDO's PSR_{DC} magnitude (dashed line) and PSR_{BW} (solid line) versus K. V_{DD} = 1.2 V, V_{OUT} = 1 V, I_L = 50 mA. Reprinted from [16]

From the previous discussion, all system level parameters for a given PSR can be determined for the proposed BDFF technique. An additional advantage of BDFF is that it requires a smaller M_P size for the same I_L specification as mentioned in [43]. This decrease in size is obtained since forward body bias reduces the effective V_T of a PMOS device.

3.3 Settling Time Improvement

The response time of an LDO is inversely proportional to its UGF and slew rate performance, as shown in (20) [43].

$$\Delta t_1 \approx \frac{1}{2\pi UGF} + C_{Gate}\frac{\Delta V_{Gate}}{I_{SR}} \tag{20}$$

where Δt_1, C_{gate}, ΔV_{gate}, and I_{SR} are the response time, M_P's gate capacitance, voltage variation at C_{gate}, and available slew rate current at M_P's gate, respectively. To decrease T_S, Δt_1 needs to be reduced which requires an increase in both the LDO's UGF and I_{SR}. Similar behavior can be expected in a CL-LDO.

To achieve a high PSR, CL-LDOs need to have a high LG at frequencies where good PSR is desired. Conventional CL-LDOs use multiple gain stages in order to achieve the required LG. However, additional gain stages introduce additional poles that limit the maximum UGF and complicate compensation. A low UGF increases the CL-LDO's T_S, therefore limiting the speed at which the CL-LDO would react to sudden I_L changes that are common in efficient SoCs.

For CL-LDOs, where the internal pole is always dominant, the maximum UGF is limited by the output pole (ω_{out}), which is I_L dependent. For low I_Q CL-LDOs, the maximum UGF for a

45° and 60° PM are given by (21) and (22), respectively, where R_{OUT} is the CL-LDO's output impedance and λ is the channel length modulation coefficient. The maximum UGF is limited by the minimum I_L and the maximum C_L. Assuming a conventional two-stage CL-LDO, the CL-LDO's T_S for 1% error and PSR versus current is shown in Fig. 15. This shows a tradeoff between maximum PSR and UGF for the design of low I_Q CL-LDOs. For those reasons, a low I_Q and high performance CL-LDO may require the ability to track changes in I_L and adjust its compensation accordingly, a novel technique to address this tradeoff is presented in subsection 4.3.

$$\text{UGF(rad/s)} \approx \frac{G_M}{C_M} \leq \frac{1}{C_L R_{OUT}} \approx \frac{I_L(\lambda V_{OUT}+1)}{C_L V_{OUT}} \tag{21}$$

$$\text{UGF(rad/s)} \approx \frac{G_M}{C_M} \leq \frac{0.577}{C_L R_{OUT}} \approx 0.577\frac{I_L(\lambda V_{OUT}+1)}{C_L V_{OUT}} \tag{22}$$

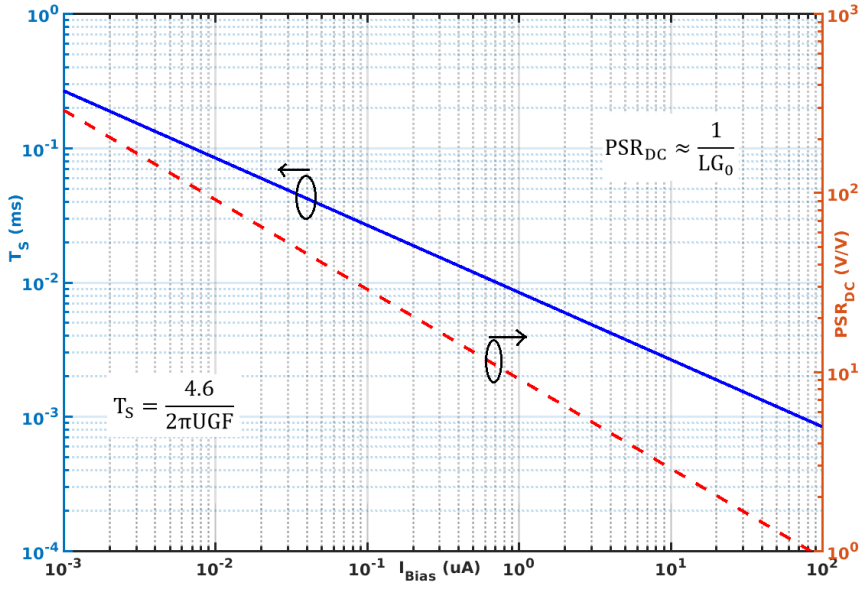


Fig. 15: Conventional CL-LDO's simulated T_S and PSR_{DC} versus bias current

To compensate CL-LDOs, a dominant pole (ω_D) is placed inside the EA, i.e., using Miller compensation, such that at the lowest I_L, the CL-LDO remains stable. However, as I_L increases, ω_{out} is pushed to higher frequencies, but the CL-LDO's UGF remains constant. This approach sacrifices faster T_S to preserve stability. To reduce T_S, a technique that increases UGF while increasing I_L without sacrificing PM and consuming minimum additional I_Q is desired. Conventional approaches to improve a CL-LDO's T_S include fast path amplifiers [12] or adaptive bias techniques [10, 11] that only work during an I_L transient step.

The second term in (20) can be reduced by increasing the available current to charge and discharge M_P's gate. However, this comes at the price of increasing I_Q which reduces efficiency. An EA with an adaptively bias output stage that increases (decreases) I_{SR} as I_L increases (decreases) is a good approach to minimize the second term in (20) since its impact on efficiency is negligible. Both implementation techniques to decrease T_S are described in subsection 4.3.

Another improvement to T_S is obtained by increasing the discharge current during a negative I_L transient, i.e., from 50−0 mA step. In conventional CL-LDOs, with feedback resistors, the resistors help to discharge I_L during a negative I_L step. Because the proposed CL-LDO avoids the use of resistors it needs an additional discharge path to ground. In this CL-LDO an NMOS connected to the output is used for that purpose. A fast comparator determines the turn-on point of the NMOS such that it discharges I_L to ground only during a negative load step, 50-0mA, when this discharge current is needed to achieve fast T_S. During a positive load transient, from 0 to 50mA, and during steady-state operation, the comparator does not trigger and does not affect performance. The transistor-level implementation of the comparator is shown in Fig. 16.

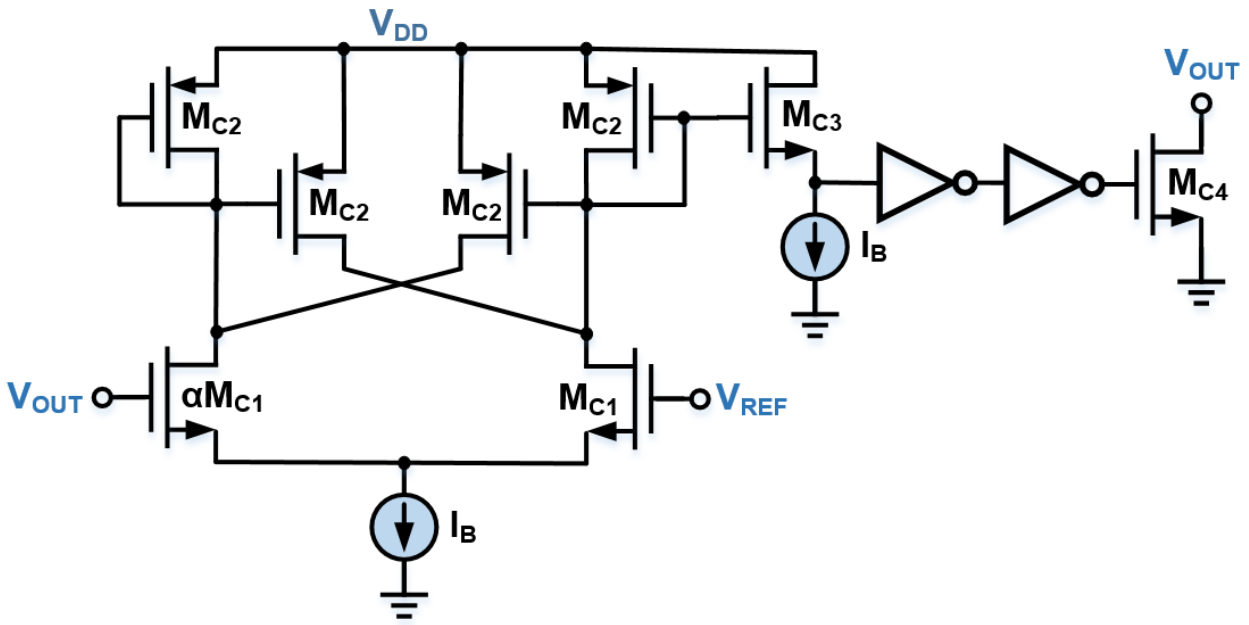


Fig. 16: Comparator's discharge path transistor-level implementation

Where $\alpha < 1$ is used to introduce an intentional offset that prevents the comparator from triggering during unwanted conditions or due to systematic offsets or mismatch after fabrication. The comparator measures the voltage difference between V_{OUT} and V_{REF}, and triggers transistor M_{C4} to discharge C_L until the difference between V_{OUT} and V_{REF} is made small.

To improve T_S in the proposed CL-LDO, with minimum power penalty, three techniques were used. The first one is to design M_P in the linear region instead of saturation at high I_Ls. This decreases M_P's area therefore decreasing C_{gs} and C_{gd}. It also decreases M_P's r_{ds}, which pushes ω_{out} to higher frequencies, both of these effects improve T_S. This comes at the price of a reduced LG because an M_P working in linear region has less gain compared to an M_P in saturation.

The second technique is to use bulk-bias (BB), BB decreases the effective M_P's V_T, which allows a smaller area to achieve the same I_L [43]. One drawback of designing M_P to work in the

linear region is a decrease in PSR. The two techniques that are used to improve PSR are gain-boosting and a BDFF supply noise path, which conceptually improve PSR as previously shown in Fig. 13. Another drawback is that the main EA's output swing now needs to accommodate for the increased voltage swing required at M_P's gate due to the gain reduction by operating M_P in linear mode. Even though the EA used in this work is not a high-swing EA, due to the source follower buffer stage, a smaller M_P is still obtained, compared to a saturation mode M_P, as results shown in Table 3. In this work, the reduction of M_P's size was ultimately limited by the EA's output swing.

Table 3: M_P's gate capacitance and area improvement. Reprinted from [16]

M_P's operation region	**Bulk-Bias**	**r_{ds}**	**Gate Capacitance**	**Reduction**	**Width**	**Reduction**
Saturation	No	15.95 Ω	12 pF	0 %	4.8 mm	0 %
Saturation	Yes	16.07 Ω	10.2 pF	15 %	4.16 mm	13.33 %
Linear	Yes	10.04 Ω	4.5 pF	62.5 %	2.34 mm	51.25 %

The third technique is a novel adaptive Miller compensation approach based on I_L sensing. For CL-LDOs, where the internal pole is always dominant, the maximum UGF is limited by the non-dominant pole, ω_{out}, which is I_L dependent. For low I_Q CL-LDOs, the maximum UGF is limited by the minimum I_L and the maximum C_L as previously shown in (21). Eq. (22) shows that as I_L increases, the maximum UGF can also be increased without sacrificing PM, and hence, the CL-LDO's T_S is also reduced.

The approach used in this paper is to adaptively increase the UGF, as I_L increases, by adjusting C_M. This approach partitions the typical C_M in different small capacitances and only

requires additional switches and a current sensing circuit to control C_M and therefore adjust the UGF. The I_{LS} at which C_M was increased or decreased were selected to maintain a PM>60° at maximum C_L. Therefore, by decreasing C_M the UGF is increased, improving the CL-LDO's T_S with minimum power overhead. As shown in Fig. 17, these three approaches decrease T_S compared to a conventional CL-LDO. As discussed further in subsection 4.3, the additional power and area overhead due to the switches and current sensing are negligible.

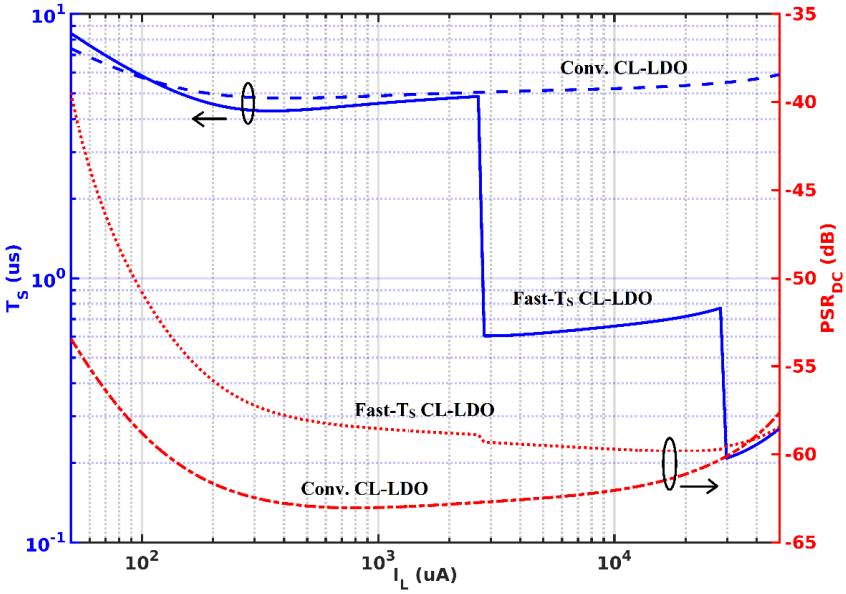


Fig. 17: Conventional versus proposed fast-T_S CL-LDO's simulated T_S and PSR_{DC}. Reprinted from [16]

3.4 CL-LDO's Circuit Implementation

The CL-LDO's main loop and main EA's transistor-level implementation is shown in Fig. 18. The main EA includes a high-gain folded cascode EA, an adaptive buffer stage, a dynamic

Miller compensation network, and an M_P. A detailed description of the different blocks is given throughout these sections.

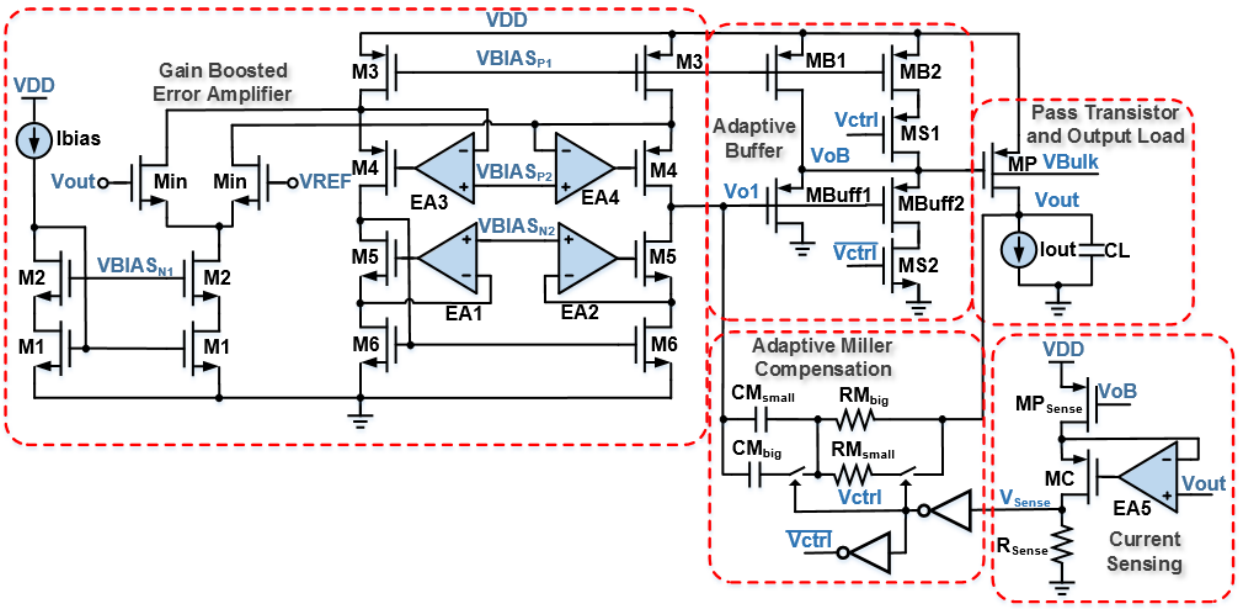


Fig. 18: CL-LDO's main loop, including main EA's transistor-level implementation. Reprinted from [16]

3.4.1 Pass Transistor with Bulk-Bias

M_P's size represents a significant portion of the CL-LDO's area. It is designed to handle the maximum I_L at low V_{DO} to maximize efficiency. M_P's larger size must accommodate an increasing area and C_{gate}, thereby decreasing transient performance. To improve all the previously mentioned drawbacks, two techniques for area reduction are used to design M_P in this work. One is to design it to work in the linear (ohmic) region, such as in [9, 11], which decreases the area requirement for a given I_L. However, it comes at the cost of a lower LG and a more stringent output

swing requirement in the main EA. To tackle these issues, a gain-boosting technique, described in subsection 4.2, was used along with bulk-biasing. BB decreases the effective M_P's V_T, which allows a lower gate voltage to achieve the same I_L. This translates to a smaller M_P size for the same I_L or more I_L for the same size [43].

Table 3 shows the improvement in area and capacitance by using a bulk-biased M_P in linear mode compared to one in saturation. Compared to an M_P designed in saturation, the linear mode M_P's size is decreased by almost 50% achieving a 62.5% gate capacitance reduction. M_P was designed for a V_{DO} = 73.2 mV, for a 1% error in V_{OUT}, and a maximum I_L = 50 mA. However, testing was performed with an input-to-output voltage differential (V_{IN-OUT}) of 200 mV. The final M_P's W/L size was 2.34 mm/120 nm. From postlayout simulations, the extracted gate capacitance is ~4.5 pF at 50 mA I_L.

3.4.2 Main Error Amplifier

The EA used inside CL-LDO regulators needs a high gain to keep a precise track of V_{REF}, despite variations in V_{DD} and I_L. In addition, due to the small C_L, CL-LDOs need a high UGF to be able to respond to fast I_L changes without significant variation in V_{OUT} and with fast T_S. For these reasons, high gain and UGF are required; however, these two characteristics conflict with each other.

Modern technologies with lower intrinsic gain demand the use of multiple stages to achieve the required CL-LDO's gain. The drawback of additional stages is the limit in the achievable UGF with a sufficient enough PM. Gain boosting [44] is a technique that combines the high-frequency behavior of a single-stage OpAmp with the high dc gain of a multi-stage design. This technique avoids the use of additional gain stages in cascade that would complicate the CL-LDO's

compensation and limit the CL-LDO's UGF. By improving the main EA's gain, the PSR is also improved, as previously shown in sketch No. 2 in Fig. 10.

The EA consists of a gain boosted NMOS folded cascode with a buffer stage to push the pole at M_P's gate to higher frequencies. A cascode bias tail current source, formed by M_1 and M_2, is used for the input diff. pair, M_{in}, while M_3, M_4, M_5, and M_6 form the folded structure. The gain-boosted EA is shown in the left side of Fig. 18, where EA1-EA4, which are implemented with single stage diff. pairs with active current loads, work as auxiliary EAs performing the gain-boosting around M_4 and M_5. The contribution of V_{DD} noise from EA1-EA4 into the NMOS folded cascode stage is negligible and they can be ignored for PSR analysis purposes. EA1 and EA2 are PMOS diff. pairs with NMOS active current loads which, in terms of PSR, behave as type-B EAs. EA3 and EA4 are NMOS diff. pairs with PMOS active current loads which, in terms of PSR, behave as type-A EAs [27]; however, because they are in closed-loop, their V_{DD} noise is decreased by their LG. The NMOS folded cascode, shown in Fig. 18, behaves as a type-B EA, at low-frequencies, as explained in [27]. As frequency increases, node V_{o1}, in Fig. 18, which is a high impedance node by design, creates a low-frequency pole with the multiplied C_M given by

$$\omega_{P1,PSR} \approx \frac{1}{R_{OUT1}A_{Buff}A_{PT}C_M} \approx \frac{1}{\left\{\left(A_{0,EA2}g_{m5}r_{o5}r_{o6}\right)//\left[A_{0,EA4}g_{m4}r_{o4}\left(r_{o3}//r_{in}\right)\right]\right\}A_{Buff}A_{PT}C_M} \qquad (23)$$

where R_{OUT1}, $A_{0,EA2}$, $A_{0,EA4}$, A_{Buff}, g_{m5}, g_{m4}, r_{o3}, r_{o4}, r_{o5}, r_{o6}, and r_{in} are the impedance at node V_{o1}; EA2's, EA4's, and Buffer's dc gain; M_5's and M_4's transconductance; and M_3's, M_4's, M_5's, M_6's, and M_{in}'s output impedance, respectively. This low-frequency pole shunts V_{DD} noise to ac ground at V_{o1}, therefore extending its PSR beyond the first pole.

The PMOS buffer stage also behaves as a type-B because the noise injected through M_{B1}'s impedance is injected into a low impedance node formed by M_{Buff}'s source, whose PSR BW is equivalent to M_{Buff}'s BW, which lies beyond the CL-LDO's UGF. For these reasons, when it comes to PSR the main EA as a whole, including the effect of EA1-EA4, behaves as a type-B EA.

The simulated transistor-level gain-boosted EA, including the auxiliary EAs and buffer stage, PSR behavior is shown in Fig. 19, where the PSR with and without the auxiliary EAs' noise contribution is shown. Fig. 19 validates the previous assumptions made that the auxiliary EAs' noise contribution to PSR is minimal and can be neglected. A close to −40 dB of attenuation up to 10 MHz is observed for the main EA, which validates the previous assumption of a type-B behavior in the frequencies of interest.

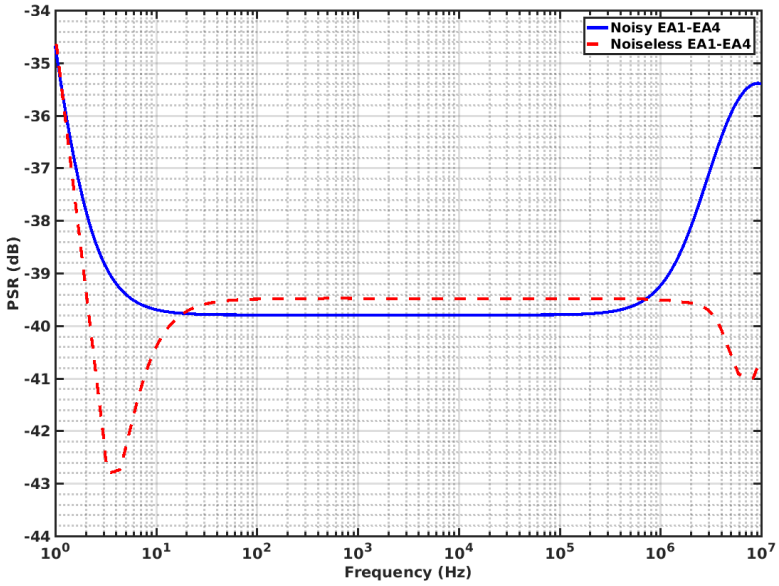


Fig. 19: Main EA's simulated PSR with and without noise in auxiliary EAs. V_{DD} = 1.2 V. Reprinted from [16]

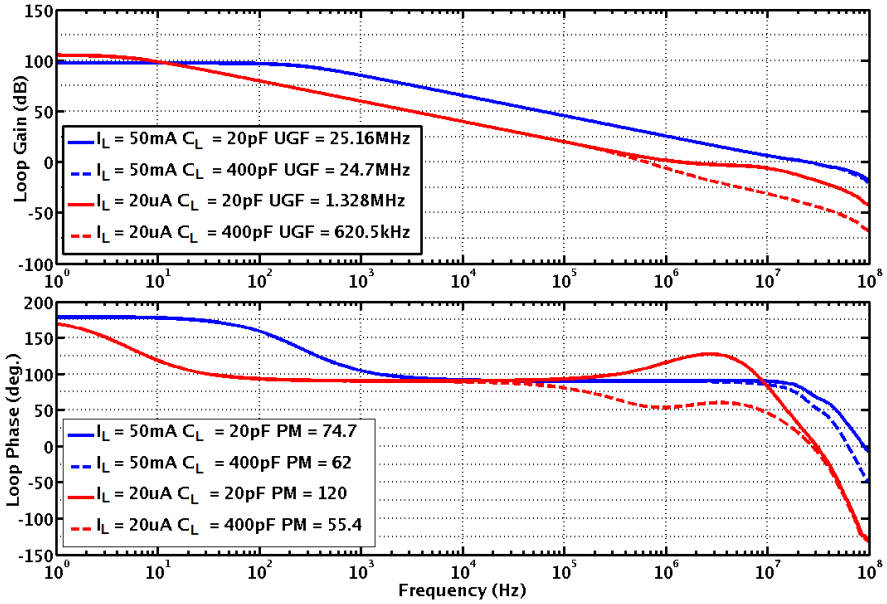


Fig. 20: Simulated CL-LDO's LG and phase, with adaptive Miller circuit, at different I_Ls. V_{DD} = 1.2 V, V_{OUT} = 1 V. Reprinted from [16]

The simulated CL-LDO's LG and phase for minimum and maximum I_L and C_L are shown in Fig. 20. The effect of the adaptive Miller compensation, explained in subsection 4.3, is shown as the UGF is pushed at high frequencies for high I_Ls without compromising the CL-LDO's stability. At high I_L, ω_{out} is pushed to very high frequencies and C_L has less impact on UGF and PM, as seen in Fig. 20, where the worst stability condition occurs at the maximum C_L. At I_L = 50 mA, the LG and UGF are 97 dB and 24.7(25.16) MHz, respectively, for a C_L of 400(20) pF. At I_L = 20 µA, the LG and UGF are 109 dB and 0.62(1.32) MHz, respectively, for a C_L of 400(20) pF. It can be observed that at a small I_L the UGF and PM change more significantly than at higher I_L. At high I_L, the worst stability condition occurs at the maximum C_L; however, for small I_L both high and low C_L need to be checked for a robust system that uses Miller compensation.

The NMOS folded cascode consumes a total of 8 μA, and the additional gain-boosting EAs, E1-E4, consume 2 μA each. The LDO's regulation voltage was set to 1 V for a nominal V_{DD} of 1.2 V.

3.4.3 Compensation and Buffer Stage

The I_L-dependent ω_{out} may interact with the CL-LDO's internally created dominant pole (ω_D) causing complex poles to degrade PM [45]. The proposed adaptive Miller compensation prevents the I_L-dependent ω_{out} to interact with the CL-LDO's ω_D, hereby avoiding instability problems while still maintaining a high UGF. To maximize the CL-LDO's loop performance, an adaptive Miller compensation scheme was used, as shown in Fig. 18.

At low I_L, when ω_{out} is located at low frequencies, an 8.4 pF C_M creates a ω_D at the first stage's output. However, as I_L increases and ω_{out} moves to higher frequencies, the proposed CL-LDO's UGF can also be increased which would improve the CL-LDO's PSR and T_S, while keeping the CL-LDO's ω_D internal. This effect is achieved by decreasing C_M, which sets ω_D due to the Miller effect, thereby increasing the CL-LDO's BW and UGF. The adaptive Miller is achieved by sensing I_L using a sense transistor, and using an ON/OFF switch to control C_M and R_M.

The current sensing circuit, as shown in the lower right red-dashed box of Fig. 18, is used to copy a scaled version of the M_P's current, where M_{PSense} is an M_P's scaled version. A cascode transistor, M_C, with a dedicated loop provided by EA5 tracks V_{OUT} to decrease the channel-length modulation error in the replica current. This tracking is required because M_P operates in the linear region and is subject to a strong channel-length modulation effect, compared to an M_P in saturation mode, which would make variations in the trigger point strongly dependent on its drain voltage.

However, the sense current circuit's speed is not important since it only needs a low-frequency tracking of V_{OUT} to determine the threshold to trigger the circuits that follow. For that reason, the EA5's BW does not need to be high and can be designed with low I_Q. The current sensing EA, EA5 in Fig. 18, consumes 2 µA.

The switching points were selected at around 1 and 27 mA of I_L, via V_{Sense}, which is the voltage across R_{Sense} in Fig. 18. The first switching point, at I_L = 1 mA, was selected to coincide with the BDFF circuit's turn ON trigger level, which allowed to recycle the same detection circuitry for both switching compensation and turning ON the BDFF circuit, more on the BDFF circuitry in subsection 4.6. The second point, at I_L = 27 mA, was determined based on worst-case process and corner simulations as a safe point where ω_{out}, non-dominant in the proposed CL-LDO and assuming a worst-case load of C_L = 400 pF, is no longer having an impact in the CL-LDO's PM. It is at this point where C_M can be safely decreased to increase the CL-LDO's UGF to improve T_S and PSR performance.

Capacitor and resistor banks are controlled to select the proper compensation values for that particular I_L region. The inverter gates that control the adaptive Miller compensation, in Fig. 18, have their turn-on slew rate controlled via a fixed current. This prevents glitches in the CL-LDO's transient response due to fast changes in C_M's value. The three compensation steps for low (I_L < 1 mA), medium (1 mA < I_L < 27 mA), and high (27 mA < I_L) currents are C_M = 7.4 pF and R_M = 21 kΩ, C_M = 0.8 pF and R_M = 5.25 kΩ, and C_M = 0.2 pF and R_M = 5.25 kΩ, respectively. The approximated poles and zeros are given in (24)−(28), where R_{o1}, R_{oB}, C_B, and g_{mB} are the first and buffer stage's output impedance, buffer's parasitic capacitance and transconductance, respectively. It was assumed that g_m is large due to M_P's size and current.

The complex pole movement can be explained as follows: At small currents the right hand-side root is smaller than the time constant associated with the Miller compensation; however, as I_L increases, it becomes more dominant and creates a complex pole pair. The root locus as a function of I_L is shown in Fig. 21, where the Miller compensation switching point's effect is included. Due to the adaptive buffer stage, the pole at M_P's gate always remains at higher frequencies than the LDO's UGF.

$$\omega_{PD} \approx -\frac{1}{A_{PT}C_M R_{O1}} \tag{24}$$

$$\omega_{P1,P2} \approx -\frac{1}{2C_M R_M} \pm \frac{1}{2}\sqrt{\left(\frac{1}{C_M R_M}\right)^2 - \frac{4g_m}{C_L C_M R_M}} \tag{25}$$

$$\omega_{P3} \approx -\frac{1}{C_B R_{OB}} \tag{26}$$

$$\omega_{Z1} \approx -\frac{1}{C_M R_M} \tag{27}$$

$$\omega_{Z2} \approx -\frac{g_m g_{mB} R_M}{C_M} \tag{28}$$

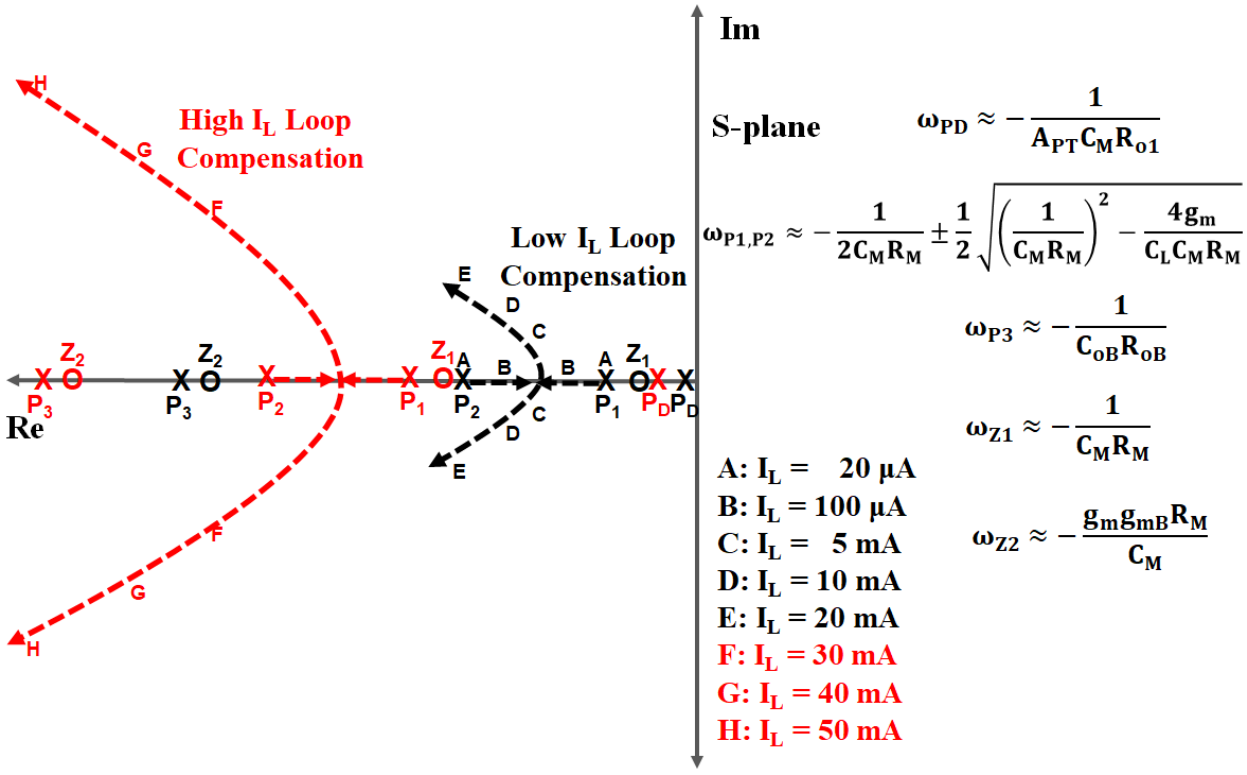


Fig. 21: Bulk-driven feed-forward LDO pole/zero movement versus I_L including the effect of adaptive compensation switching (C_L = 400 pF). Reprinted from [16]

The CL-LDO maintains stability across the entire I_L (20 µA − 50 mA) and C_L (0−400 pF) ranges. Due to the unity-gain configuration, the minimum I_L, which cannot be zero, is set by the external load and its leakage current.

The requirement for the buffer stage formed by M_{Buff1}, M_{Buff2}, M_{B1}, and M_{B2} in Fig. 18, is to push the pole at M_P's gate, when needed, beyond the CL-LDO's UGF in order to have minimum phase degradation without spending too much I_Q. Because the adaptive Miller compensation decreases and increases the loop's UGF at low and high I_L, an efficient buffer should also be able to decrease and increase its I_Q at both low and high I_L. The current sensing voltage, V_{Sense}, in Fig.

18, is also used to control the buffer stage's I_Q. The buffer consumes 8 (16) μA in the low (high) power mode. Due to these adaptive schemes, both in the Miller compensation and buffer stage, the CL-LDO's UGF increased from 620.5 kHz to 24.7 MHz, a 40x increase, while keeping a minimum PM of 57° for a C_L of 400pF.

3.4.4 PSR Feed-Forward Circuit

The feed-forward coefficient, K, is implemented with a non-inverting amplifier configuration. For the proposed BDFF, there are two K values that optimize either PSR_{DC}, using (14) found to be $K_{DC} = 4$ through simulation, as shown in Fig. 14, or PSR_{BW}, using (19) found to be $K_{BW} = 2.5$ from simulation, as shown in Fig. 14. In the proposed design, priority was given to optimization of PSR BW by implementing a feed-forward coefficient of 2.5. This is due to the tradeoff that exists between gain and BW for the feed-forward technique and its effect on PSR improvement as explained previously in subsection 2.1. This suboptimal gain coefficient has minimal impact on the proposed CL-LDO's performance due to the fact that the low-frequency PSR is sufficiently high due to the main EA's LG.

Fig. 22 shows the proposed feed-forward circuit, where a resistor (R_{DC}) and constant current source (I_{DC}) are used to generate a fixed dc level shift from V_{DD}, where the ac gain is determined by the voltage divider between the output resistance of I_{DC} and R_{DC}. This sets the bulk's terminal dc level to a fixed potential that is lower than V_{DD} so that g_{mb} can be used. Based on the results presented in [13], and to limit leakage current through the body diode, the dc forward bias was set to 0.4 V so that the PMOS body diode is not turned-on while using M_P's body effect.

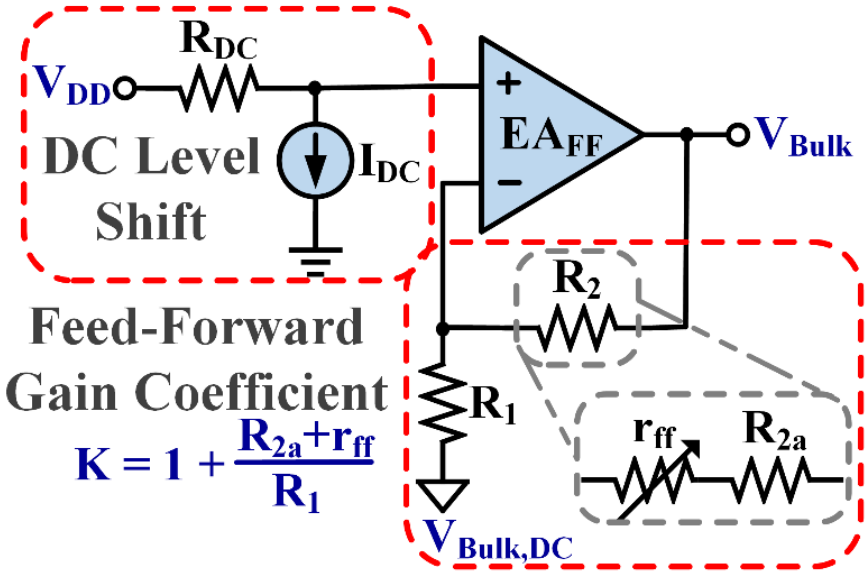


Fig. 22: Non-inverting amplifier proposed to create the bulk feed-forward coefficient. Reprinted from [16]

Process variations around the dc level shift block create a voltage dependence on the absolute value of both R_{DC} and I_{DC}. These variations affect the feed-forward path's performance both in terms of PSR and reliability to guarantee that the bulk-to-source diode never turns on. An additional low-frequency control loop, shown in Fig. 23's left side, was used to set the current and fix a constant dc drop regardless of R_{DC}'s process variations.

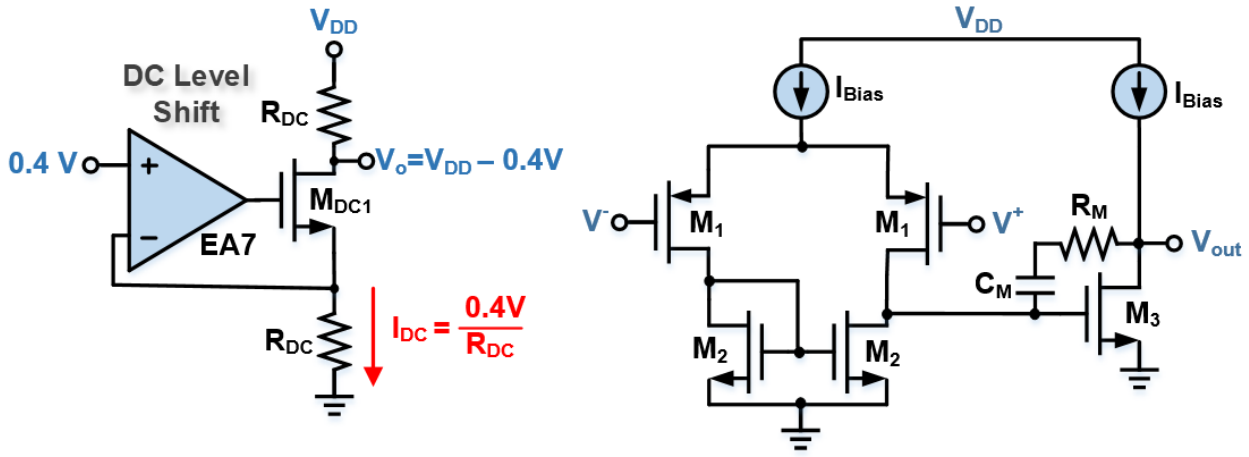


Fig. 23: Bulk-driven feed-forward dc level shift control loop

I_{DC} is created with a negative feedback loop created around transistor M_{DC1}. The feedback loop replicates the 0.4 V reference connected to the EA's positive terminal to M_{DC1}'s source, where R_{DC} converts this voltage to a constant current. The two resistors, named R_{DC} in Fig. 23, have the same value, are matched in layout, and the current through them is the same independently of R_{DC}'s absolute value or V_{DD}. This creates a constant voltage drop across the upper resistor, which is then used to feed the positive terminal of the feed-forward error amplifier (EA_{FF}), shown in Fig. 22.

I_{DC}'s output impedance, as shown in Fig. 24, is higher compared to the upper R_{DC} resistor, which makes V_{DD}'s ac gain, given by the voltage divider, approximately one. The right-side of Fig. 23 shows the EA used in I_{DC}'s implementation. EA7 is implemented by a two-stage Miller with PMOS input pair, where due to the topology and closed-loop operation, no additional V_{DD} noise is introduced [27].

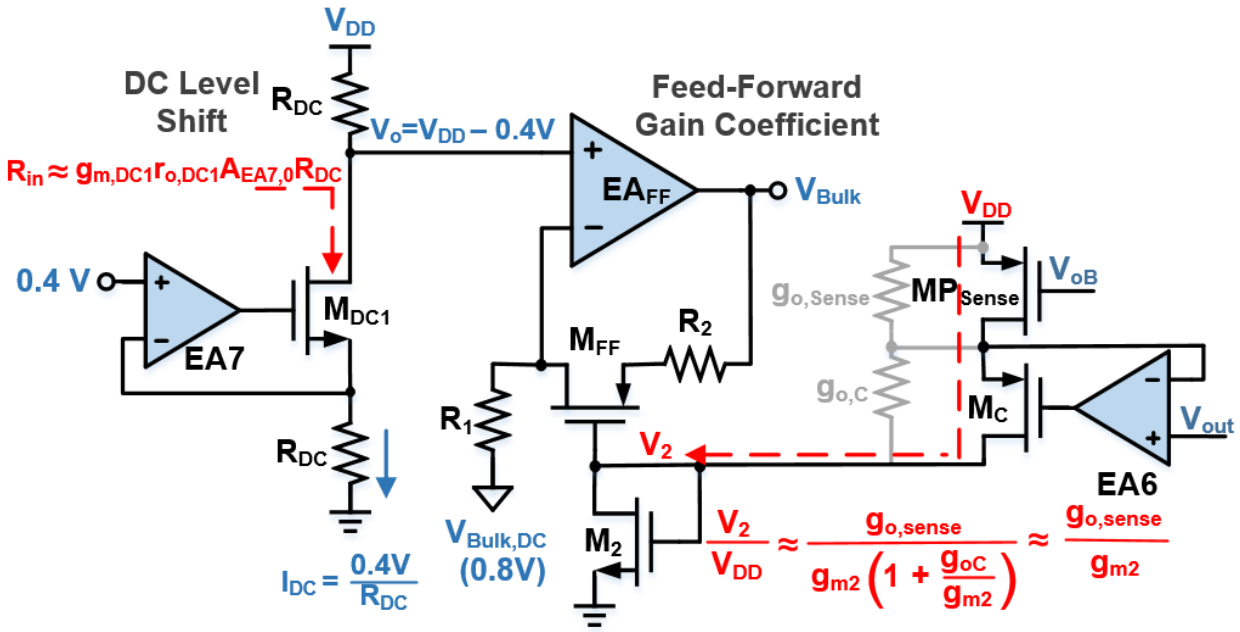


Fig. 24: Complete BDFF circuit implementation with dc level shift and feed-forward gain coefficient. Reprinted from [16]

The I_{DC} circuit consumes a total of 6 µA where the EA consumes 2 µA, the R_{DC} resistors have a value of 100kΩ and the current through them is 4 µA. In addition, this BB dc level also allows for a decrease in M_P size, for a given maximum I_L and gate voltage, due to the lower effective V_T. Resistors R_2 and R_1 set the non-inverting amplifier's ac gain. Eq. (29) can be obtained by equating the amplifier's closed-loop non-inverting gain and the desired gain given by (19).

$$1+\frac{R_2}{R_1}=1+\frac{g_m+g_{ds}}{g_{mb}}-\frac{2C_{gs}C_{gd}g_{oA}}{g_{mb}\left(C_{gs}+C_{gd}\right)^2}-\frac{g_mC_{gs}}{g_{mb}\left(C_{gs}+C_{gd}\right)} \tag{29}$$

To provide more insight into the design parameters, (30) was obtained using small signal values for g_{ds}, g_m, and g_{mb} into (29).

$$\frac{R_2}{R_1}=\frac{1}{\chi}\left(1+\lambda_p\sqrt{\frac{I_{DS,p}L_p}{2\mu_p C_{ox}W_p}}-\frac{C_{gs}}{C_{gs}+C_{gd}}-\frac{\sqrt{2}C_{gs}C_{gd}g_{oA}}{\sqrt{\mu_p C_{ox}\frac{W_p}{L_p}I_{DS,p}}\left(C_{gs}+C_{gd}\right)^2}\right) \tag{30}$$

where λ_P, $I_{DS,P}$, μ_p, C_{ox}, and χ are channel length modulation effect, M_P's current, hole mobility, oxide capacitance and V_T's rate of change with bulk-to-source (V_{BS}) voltage as defined in [42], respectively. From (30), it can be seen that the first term depends only on V_{BS} while the other terms also depends on M_P's current, parasitic capacitances, and V_{BS} combined.

A unique K_{DC} or K_{BW} maximizes the CL-LDO's PSR dc gain or BW for a given I_L. However, even if K_{DC} or K_{BW} deviates from the ideal one, the PSR is improved as previously shown. This is shown mathematically in (12), where it can be seen that a smaller than the ideal K decreases V_{DD} noise. Fig. 12 shows the PSR improvement as a function of error between the ideal K_{DC} and the implemented K, similar assumptions could be made about the optimal BW by using K_{BW} as shown in Fig. 14.

For some applications, the PSR obtained across the I_L range with a fixed feed-forward coefficient might suffice. This can speed and relax circuit design at the cost of sub-optimum PSR. To maximize PSR for all I_Ls, EA_{FF} needs to track I_L and adjust its coefficient accordingly.

3.4.5 Current Tracking Circuit

The optimal K_{DC} and K_{BW} coefficients needed to maximize PSR dc and PSR BW are given by (14) and (19), respectively. However, it was proved in previous analysis that this gain needs to be dynamically modified since it depends on M_P's current. The modified version of R_2 in Fig. 22 adds a degree of freedom over the gain as required. The gain of Fig. 22 can be derived to get

$$K = 1 + \frac{R_{2a} + r_{ff}}{R_1} \tag{31}$$

where the ratio of $(R_2+r_{ff})/R_1$ tracks the V_{BS} and current dependent relation given in (30), respectively.

The variable resistor (r_{ff}), implemented by a PMOS operating in the ohmic region, needs to be biased by a current sense circuit that tracks first-order changes in I_L to adjust K accordingly. The CL-LDO's output current needs to be sensed and transformed to voltage. This voltage is then used to control M_{FF}'s gate potential making it behave as an output current dependent variable resistor.

The current-to-voltage conversion could be achieved by a resistor, which provides a linear and simple solution. The resistor needs to be substantially large to be able to convert low currents into a discernible voltage. However, a big resistor creates headroom problems when high output currents are being demanded from the CL-LDO. The CL-LDO's I_L range, from 0-50mA, makes it harder for a resistor based sensing technique to work reliably.

Another approach is to use a diode-connected transistor. This removes the headroom problem and allows for a smaller area implementation; however, it introduces a nonlinear

component to the current-to-voltage conversion. To save area, the diode-connected transistor approach was used for this implementation. The first-order relation between voltage and current for an NMOS diode-connected transistor is given by:

$$V_{DS} = V_{TN} + \sqrt{\frac{2I_L}{N\mu_n C_{ox}} \frac{L_N}{W_N}} \tag{32}$$

where V_{DS}, I_L, N, W_N, L_N, V_{TN}, and μ_n are drain-to-source voltage, output current, current replica's size ratio; NMOS transistor's width, length, V_T, and electron mobility, respectively. Then, V_{DS} can be used as a voltage that contains information of M_P's current.

It can be observed from (30) and (32) that the nonlinear dependence on the current can be used as an advantage since the ideal feed-forward coefficient also has a nonlinear dependence on the output current. However, care must be exercised since both nonlinear dependences relate to PMOS and NMOS parameters that do not track each other. These nonlinear dependences between NMOS and PMOS are inevitable due to the current tracking implementation; however, their impact can be reduced. To decrease these process and second-order effects, long channel lengths, eight times L_{Min}, were used for both PMOS and NMOS transistors in question, M_{FF} and M_2 in Fig. 24, respectively.

The PMOS' r_{ff} transistor in linear region is given by:

$$r_{ff} = \frac{L_P}{W_P \mu_p C_{ox} \left(V_{REF} - V_{DS,N} - \left| V_{TP} \right| \right)} \tag{33}$$

where V_{REF} is the dc reference voltage chosen for the PMOS M_P's V_{BS}. Using (32), (33), and assuming $V_{TN} \approx |V_{TP}|$, we can solve for r_{ff} given by:

$$r_{ff} = \frac{L_P}{W_P \mu_p C_{ox}\left(V_{REF} - V_{DS,satNMOS} - 2V_{TN}\right)} \tag{34}$$

where $V_{DS,satNMOS}$ is the diode-connected transistor's saturation voltage given in the second term of (32).

The dynamic range of resistor R_2, $R_{2a}+r_{ff}$ as shown in Fig. 22, is from 8.8 kΩ to 7.4 kΩ, where the fixed resistor's value is 6 kΩ and r_{ff} varies from 1.4 kΩ to 2.8 kΩ across I_L. The complete feed-forward implementation is shown in Fig. 24, it includes the dc level shift circuit explained in subsection 4.5, EA_{FF} explained in subsection 4.6, and a current sense circuit similar to the one explained in subsection 4.3.

The current tracking circuit introduces additional noise through M_{PSense} that is transformed to voltage by M_2 and injected into M_{FF}'s gate. This noise is attenuated by M_2's diode configuration and by EA_{FF}'s LG. This is shown in Fig. 24, where M_C's body effect was ignored and EA6's gain was assumed higher than one and its V_{DD} noise was neglected because its closed-loop configuration attenuates it. Although this noise is attenuated by the diode configuration of M_2 and by EA_{FF}'s LG, it may pose a limit in the maximum improvement that could be achieved at low-frequencies if values close to the ideal K_{DC} coefficient were to be used. Implementations, like the one proposed here, where K_{BW} is used to maximize PSR_{BW} are not as sensitive to this effect compared to the ones maximizing PSR_{DC}.

3.4.6 Feed-Forward Error Amplifier

EA_{FF}'s transistor-level implementation is shown in Fig. 25 and was implemented using an NMOS folded cascode and a buffer stage. The buffer stage was used to drive the M_P's bulk-to-substrate capacitance. A cascode bias current source, formed by M_1 and M_2, is used for the input diff. pair, Min_{FF}, while M_3, M_4, M_5, and M_6 form the folded structure.

The dominant pole is located at the folded cascode's output, where C_C and R_C form a pole zero pair to improve stability. The buffer stage is formed by M_{B1} and M_{B2}. EA_{FF}'s buffer stage was designed to have a low output impedance to push M_P's bulk capacitances to high frequency. Fig. 26 shows the feed-forward path's small-signal model including M_P's bulk capacitances. The small signal transfer function is given by:

$$V_B = \frac{V_{DD}\left(sC_{sb}R_{o,K}+K\right)+V_{OUT}\left(sC_{db}+g_{db}\right)R_{o,K}+V_{oB}sC_{gb}}{s\left(C_{sb}+C_{db}+C_{b\text{-}sub}+C_{gb}\right)R_{o,K}+1} \tag{35}$$

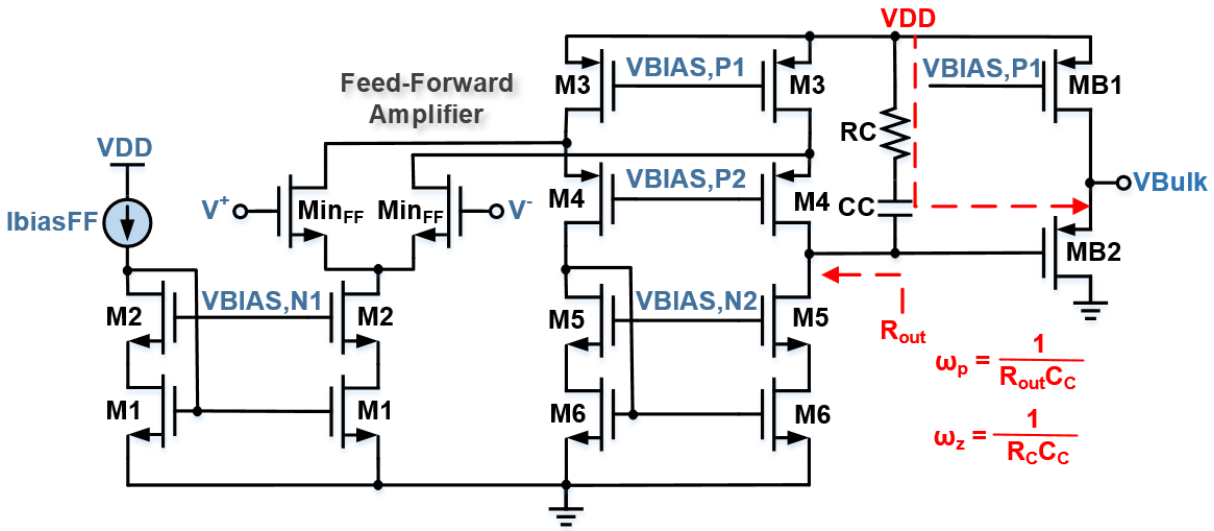


Fig. 25: EA_{FF}'s transistor-level implementation. Reprinted from [16]

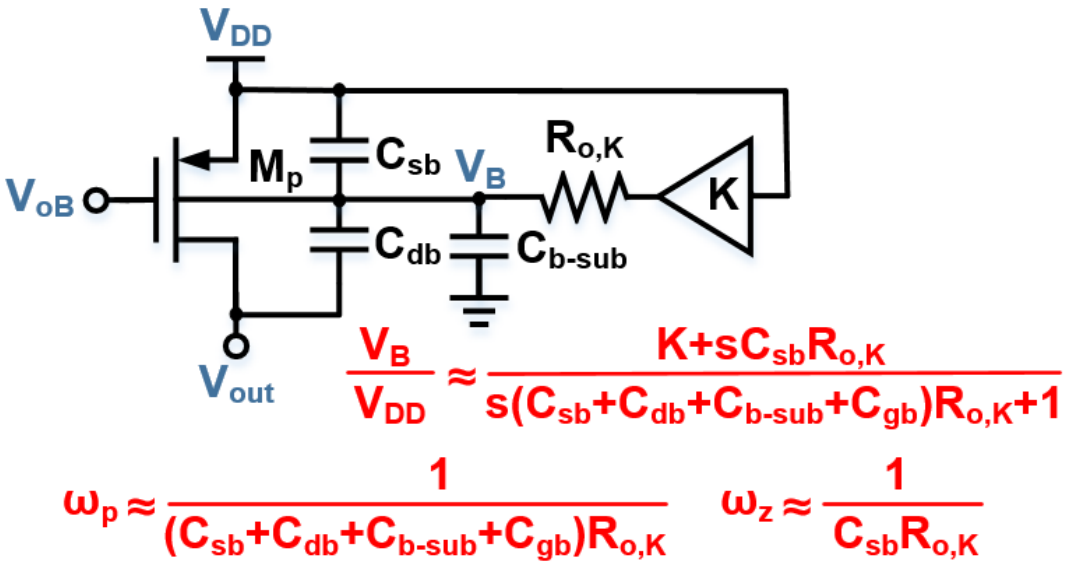


Fig. 26: Feed-forward small-signal model including M_P's bulk parasitic capacitances. Reprinted from [16]

Eq. (35) is used to determine the simplified feed-forward path's transfer function shown in Fig. 26, where it has been assumed that V_{OUT} and V_{oB} are ac ground to determine the transfer function from V_{DD} to V_B. EA_{FF} requires a low output impedance to push its closed-loop BW beyond the CL-LDO's UGF to achieve the desired PSR improvement. Beyond EA_{FF}'s closed-loop BW, the feed-forward becomes a function of the capacitor divider formed between C_{SB} and the sum of all bulk capacitances. The EA_{FF}'s closed-loop BW, including the loading effects of M_P's bulk related parasitic capacitances, was designed to be around 32 MHz, which puts it beyond the CL-LDO's UGF plus some margin, which is located at 25 MHz.

With the exception of the gain boosting technique, EA_{FF} uses the same architecture as the main EA so when it comes to PSR, it acts as a type-B EA. At frequencies higher than EA_{FF}'s UGF, V_{DD} noise should be coupled to its output in order to allow M_P's bulk to have similar noise

compared to its source. Additional noise was injected to EA_{FF} through the RC compensation, which was referenced to V_{DD} instead of ground. This has no effect on EA_{FF}'s stability and the RC network is determined solely on EA_{FF}'s required closed-loop stability.

In scenarios where PSR is not critical or when I_L is smaller than 1 mA, EA_{FF} is turned off creating a low I_Q mode that decreases I_Q and extends battery life. A MOSFET switch, not shown in Fig. 25, connects M_P's bulk terminal to V_{DD} during low-power mode. EA_{FF}'s ON/OFF state is determined by the same current sensing circuit that controls the adaptive Miller compensation below 1 mA. During normal operation EA_{FF} consumes 58 μA when V_{DD} = 1.2 V.

The feed-forward technique, shown in Fig. 24, relies on a fixed dc voltage that tracks V_{DD}. However, in reality, this voltage would vary since it depends on errors introduced by resistor mismatch and EA7's offset. Fig. 27(a) shows PSR improvement's corner simulations at different temperatures and I_Ls, and Fig. 27(b) shows Monte Carlo simulations (N=4000) for the bulk's level shifter voltage difference. These figures provide simulation data regarding PVT, mismatch, and I_L variation and their impact in PSR improvement due to the BDFF circuit.

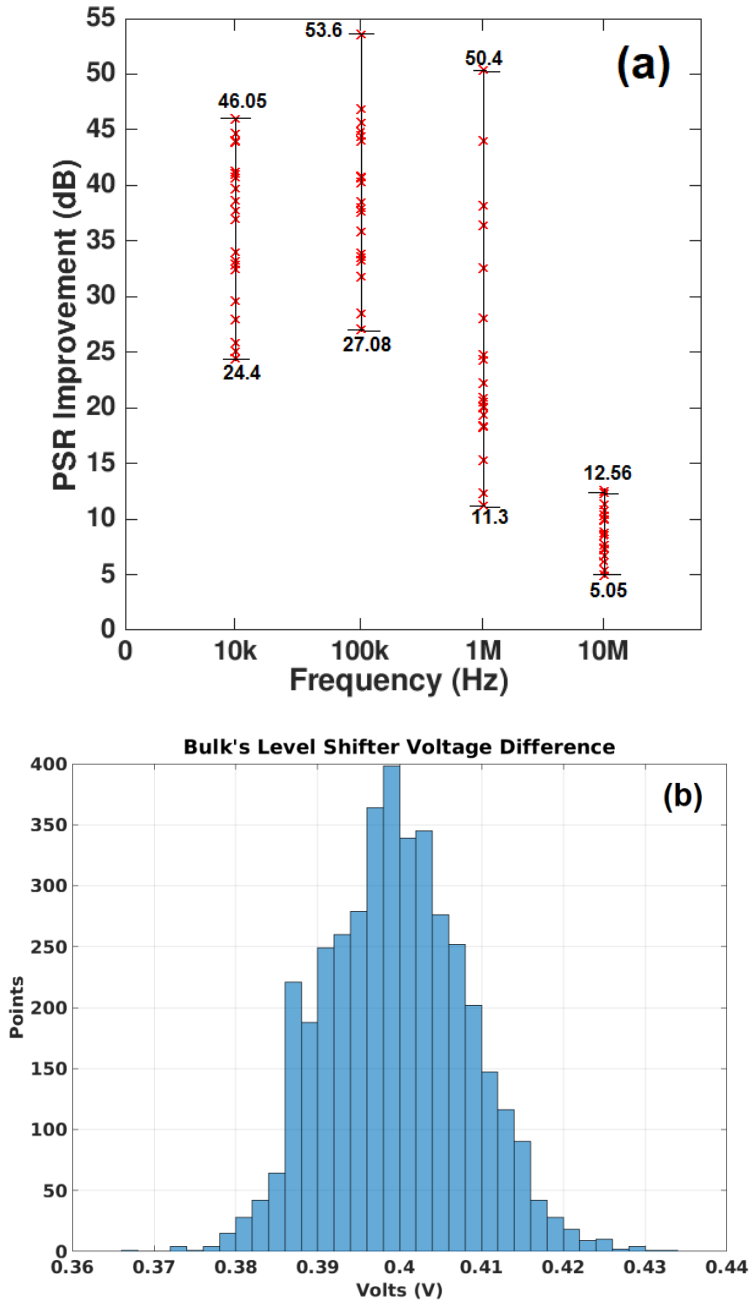


Fig. 27: (a) PSR improvement for different corners (tt, ss, sf, fs, ff), temperatures (30°C, 85°C) and I_{LS}s (5 mA, 50 mA). (b) Bulk's level shifter voltage difference, Monte Carlo simulations (N=4000) for technology's process parameters (sheet resistance, V_T, $\mu_{n/p}$, W, L, t_{ox}). V_{DD} = 1.2 V and V_{OUT} = 1 V for both simulations. Reprinted from [16]

The proposed BDFF CL-LDO's PSR BW is ultimately limited by the main loop's frequency behavior and the feed-forward technique. Two main zeros exist in the proposed CL-LDO's PSR, ω_{z1} and ω_{z2} in (4b). Similar to conventional CL-LDOs, the first PSR zero is determined by the main loop's BW [27] and the second PSR zero is introduced due to the BDFF path and varies depending on K, as explained previously. Depending on the system specifications, each designer requires to balance the tradeoff between high frequency PSR and power consumption. The frequency contributions to PSR can be included in (12) to obtain a first-order frequency dependent PSR expression given by:

$$PSR(s) \approx \frac{\left(g_m + g_{ds} + g_{mb} - \frac{Kg_{mb}}{1+\frac{s}{UGF_{FF}}} \right) R_{OUT}}{1+\frac{LG}{1+\frac{s}{\omega_{p,LG}}}} \tag{36}$$

which can be simplified as shown in (37).

$$PSR(s) \approx PSR_{DC} \frac{\left(1+\frac{s}{\omega_Z}\right)\left(1+\frac{s}{\omega_{p.LDO}}\right)}{\left(1+\frac{s}{UGF_{LDO}}\right)\left(1+\frac{s}{UGF_{FF}}\right)} \tag{37}$$

$$\omega_Z \approx UGF_{FF}\left(1-\frac{Kg_{mb}}{g_m+g_{ds}+g_{mb}}\right) \tag{38}$$

where PSR_{DC} is given in (17), UGF_{LDO} and $\omega_{p,LDO}$ are the main EA's UGF and BW, and UGF_{FF} is the EA_{FF}'s UGF. UGF_{FF}, UGF_{LDO}, and $\omega_{p,LDO}$ depend on the current used by EA_{FF} and main CL-LDO's EA.

Usually $\omega_{p,LDO}$ and UGF_{LDO} are fixed by the required CL-LDO's PM and LG. To determine the feed-forward bias current ($Ibias_{FF}$) for a given PSR, Fig. 28 shows a set of calculated PSR versus $Ibias_{FF}$ curves at two different frequencies assuming a C_L of 400 pF.

Table 4 shows a summary of I_Q for the circuits used in the proposed BDFF CL-LDO.

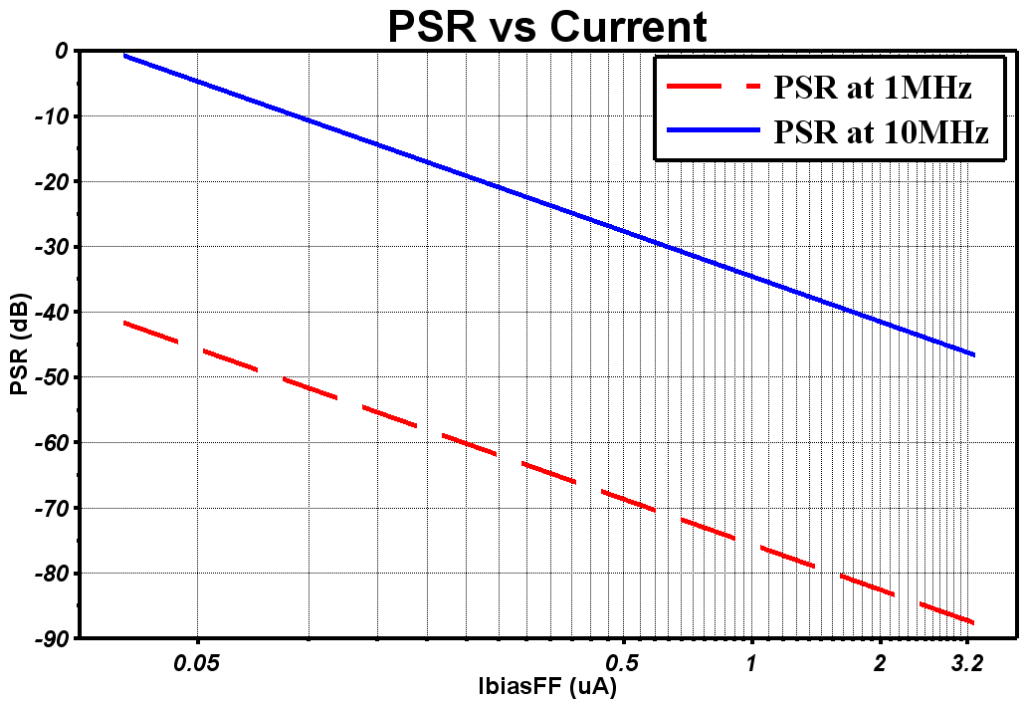


Fig. 28: Calculated PSR versus $Ibias_{FF}$ (C_L = 400 pF)

Table 4: BDFF LDO's Current Consumption Summary. Reprinted from [16]

Circuit Block	I_Q (I_L < 1 mA)	I_Q (I_L > 1 mA)
Main EA	8 µA	8 µA
Buffer Stage	8 µA	16 µA
Gain Boosting EAs (E1-E4)	8 µA	8 µA
Feed-Forward EA	0.1 µA	58 µA
Current Sense EAs (E5-E6)	4 µA	4 µA
M_P's Bulk DC Level Shifter	6 µA	6 µA
Additional bias circuits	8 µA	8 µA

3.5 Experimental Results

The proposed BDFF CL-LDO was fabricated in CMOS 130 nm process through MOSIS. The die microphotograph, with all blocks highlighted, is shown in Fig. 29. The BDFF CL-LDO occupies an area of 0.0046 mm^2. The BDFF CL-LDO has a V_{DO} = 73.2 mV at an I_L = 50 mA and a nominal V_{DD} = 1.2 V. The CL-LDO can support a V_{DD} range from 1.2 to 1.5 V and a C_L range from 0 to 400 pF. The proposed CL-LDO requires a total of 8.4 pF for compensation purposes. No internal C_L was implemented on-chip, an external C_L = 400 pF was used for testing purposes. This external C_L increases the total ESR resistance, measured at 0.1 Ω, seen by the CL-LDO compared to an internal C_L. This ESR effect is located at a higher frequency compared to the CL-LDO's UGF such that it has no effect in the loop's response or measured PSR performance in the frequencies of interest.

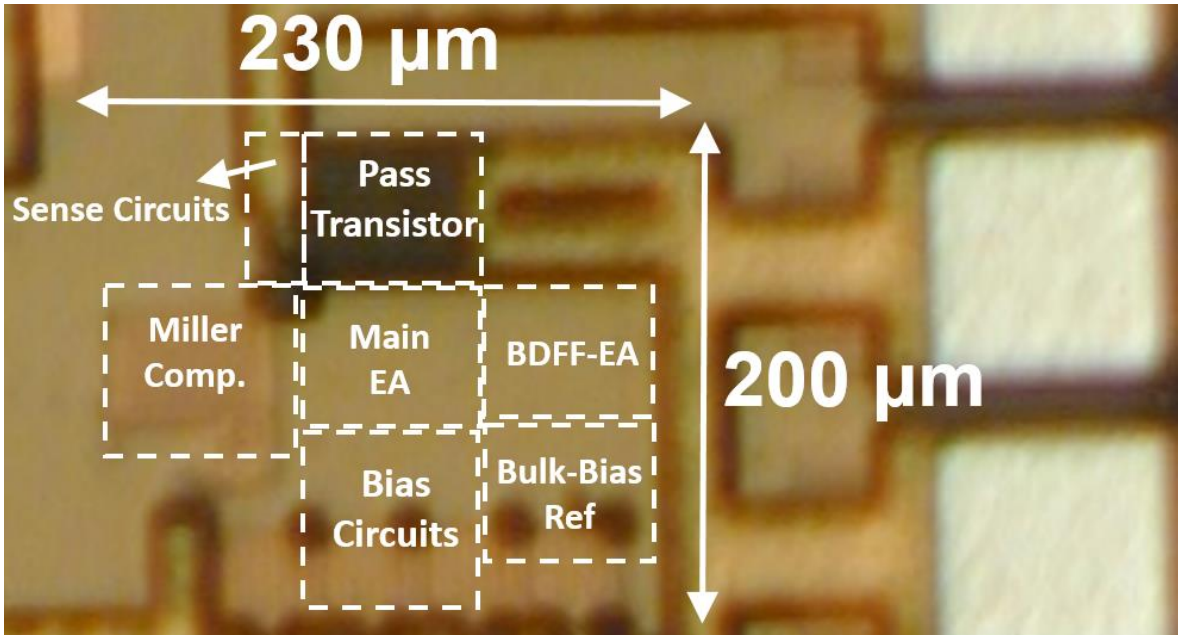
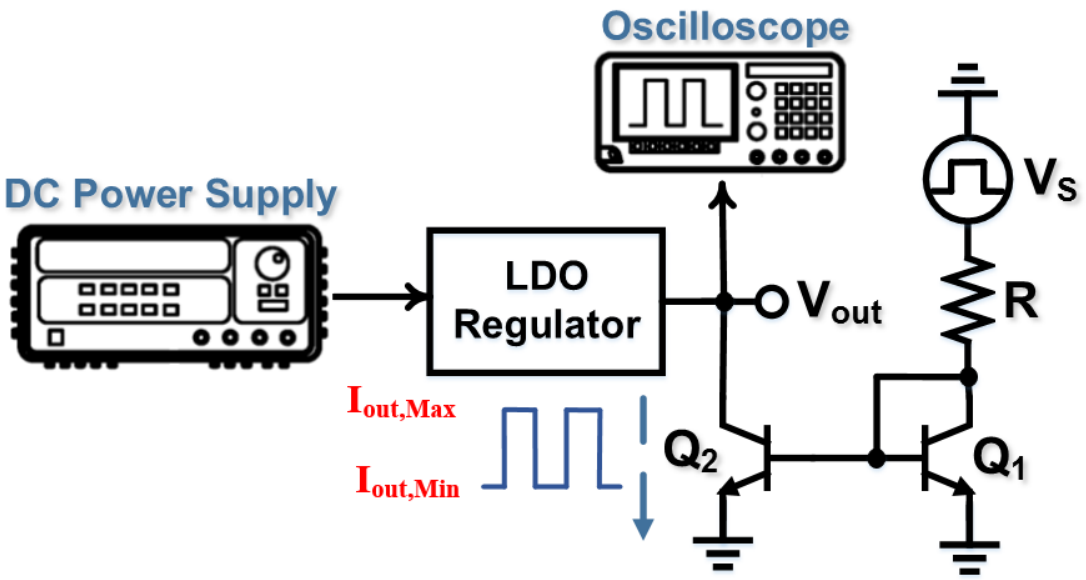
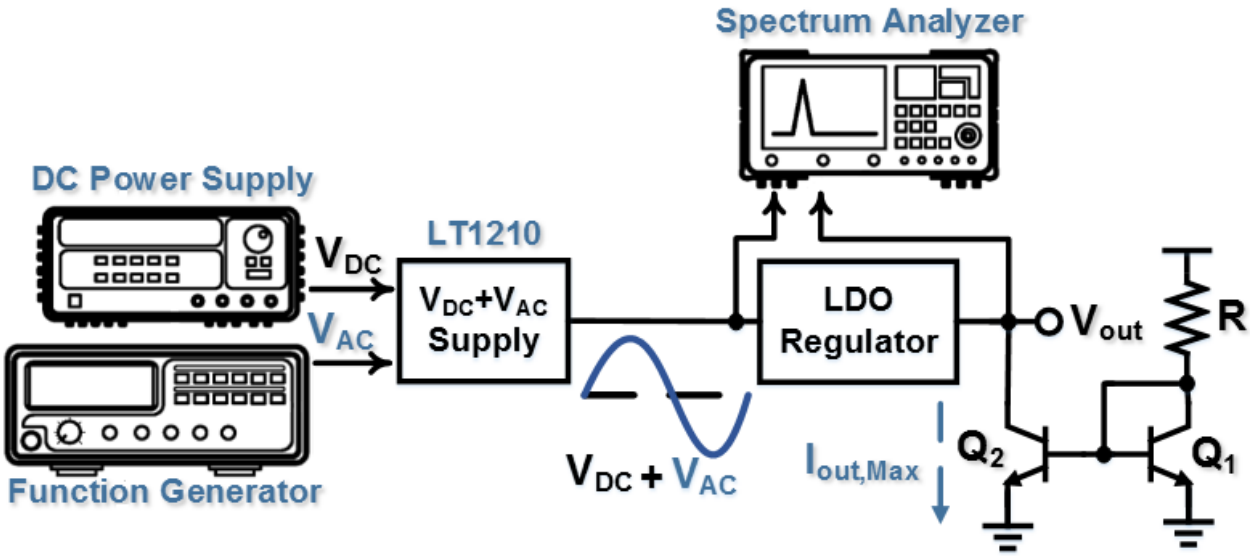


Fig. 29: Proposed BDFF LDO die microphotograph. Reprinted from [16]

The measurement setup for load transient and PSR are shown in Fig. 30(a) and Fig. 30(b), respectively. The LT1210 current amplifier, with high output current and excellent large-signal characteristics, was used as V_{DD} for the proposed CL-LDO. This current amplifier has the capability of delivering the required I_L step to the CL-LDO without a drop in its output voltage. It can also combine the ac signal from the function generator with the dc signal from V_{DD} at its output to emulate a noisy V_{DD} for the PSR measurements.



(a)



(b)

Fig. 30: Measurement setup for (a) load transient and (b) PSR

The load transient was tested with a signal generator and external NPN BJT current mirror, Q_1 and Q_2. This configuration emulates a high-input impedance load, similar to an active load,

while pulling 50 mA of current. Fig. 31 shows the V_{OUT} undershoot and overshoot for an I_L step from 0 to 50 mA in 100 ns and vice versa. The voltage undershoot and overshoot are 140 mV and 80 mV, respectively, and the CL-LDO settles in at 300 ns for a 1 % error in V_{OUT}.

The fast T_S can be attributed to the adaptive Miller compensation approach. When I_L is increased, the CL-LDO's UGF increases to 24.7 MHz, thereby improving the CL-LDO's high-frequency performance. Line transient, shown in Fig. 32, was tested by a 300 mV step with a 1 µs rise time from 1.2 to 1.5 V and back, into the CL-LDO's V_{DD}. V_{OUT} had a 2 mV deviation. Fig. 33 shows the measured T_S for different I_Qs.

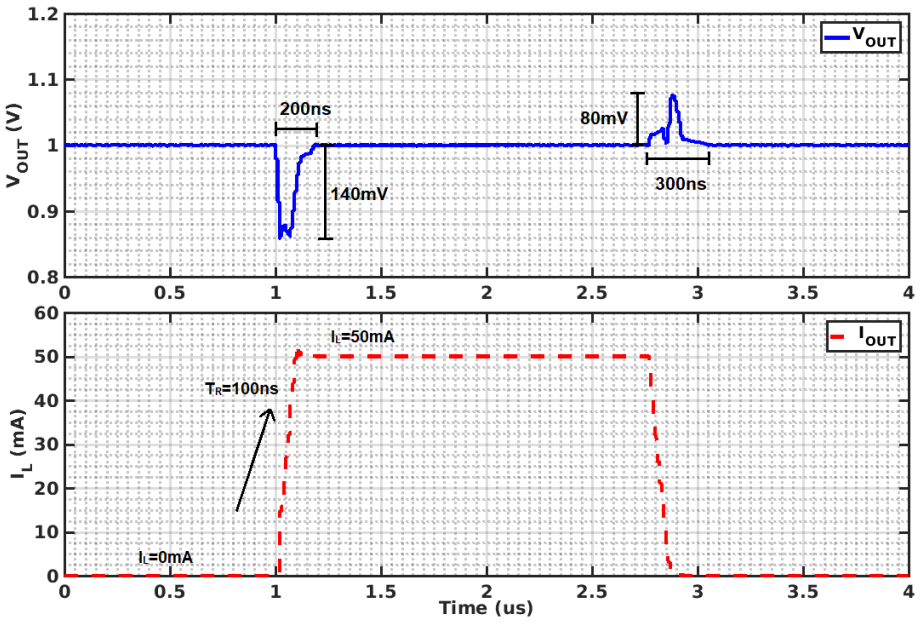


Fig. 31: Load transient response for both 0−50 mA and 50−0 mA steps with 100 ns rise time (C_L = 400 pF). Reprinted from [16]

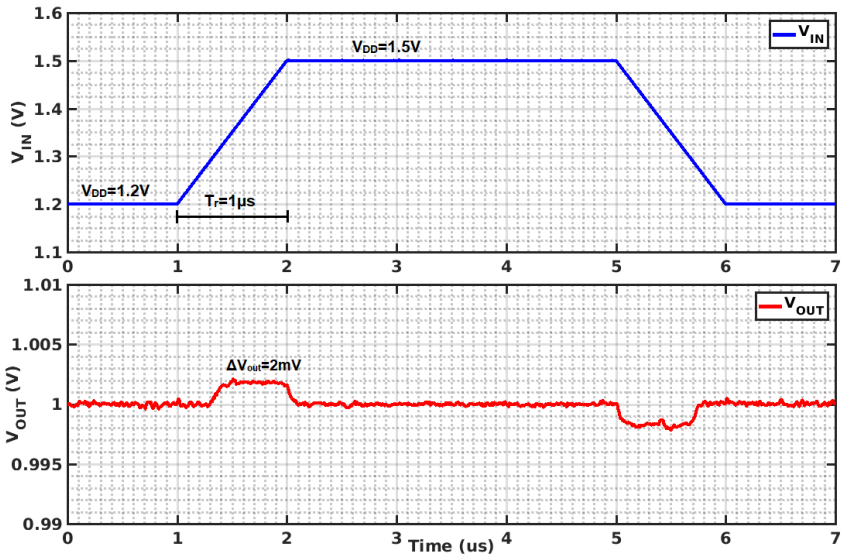


Fig. 32: Line transient response, V_{DD} from 1.2 to 1.5 V and 1.5 to 1.2 V in 1 µs rise time. (C_L= 400 pF, I_L= 50 mA). Reprinted from [16]

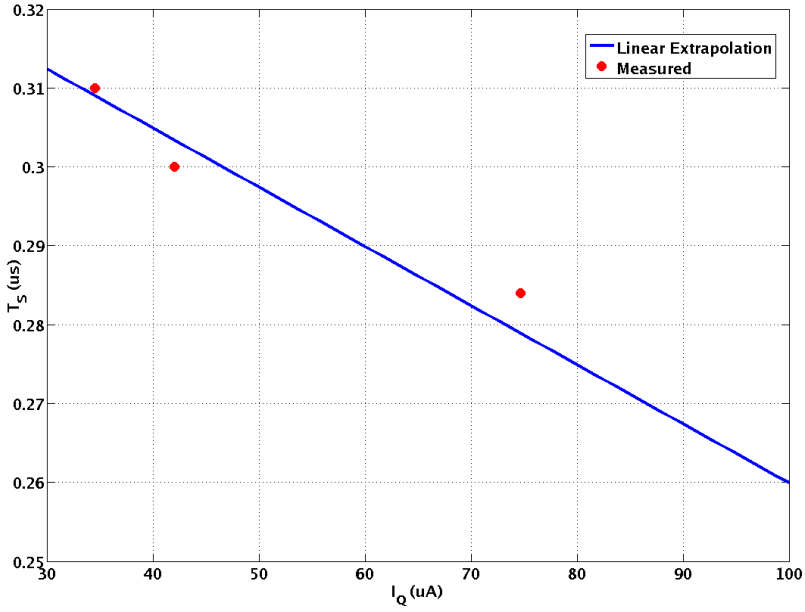


Fig. 33: Measured settling time (red dots) versus I_Q (C_L = 400 pF)

Fig. 34 shows the CL-LDO's measured PSR with and without BDFF for two different currents, which also confirms that the current tracking circuit and feed-forward coefficient are working as expected.

PSR performance at I_L = 50 mA is better than at I_L = 5 mA due to the EA's adaptive Miller compensation, explained in subsection 4.3, which decreases the internal ω_D in discrete steps as I_L decreases. This allows the CL-LDO to improve its PSR performance as I_L increases, when is likely to be more critical. Compared to the simulated performance, the low frequency PSR improvement is most likely limited by the measurement set-up and equipment's noise floor, HP3588A, which prevents measuring the technique's improvement around low frequencies. However, the main focus was to improve PSR at mid-range frequencies where most of the switching supplies would have their noise.

The proposed BDFF CL-LDO has a measured low-frequency PSR of − 90 and − 64 dB at 100 kHz and 1 MHz, respectively, for V_{OUT} = 1 V and I_L = 50 mA. The low frequency PSR improvement is limited by the measurement set-up, however, the main focus was to improve PSR at mid-range frequencies where most of the switching supplies would have their noise. An improvement of 35 dB is obtained at 1 MHz and can be up to 40 dB at lower frequencies.

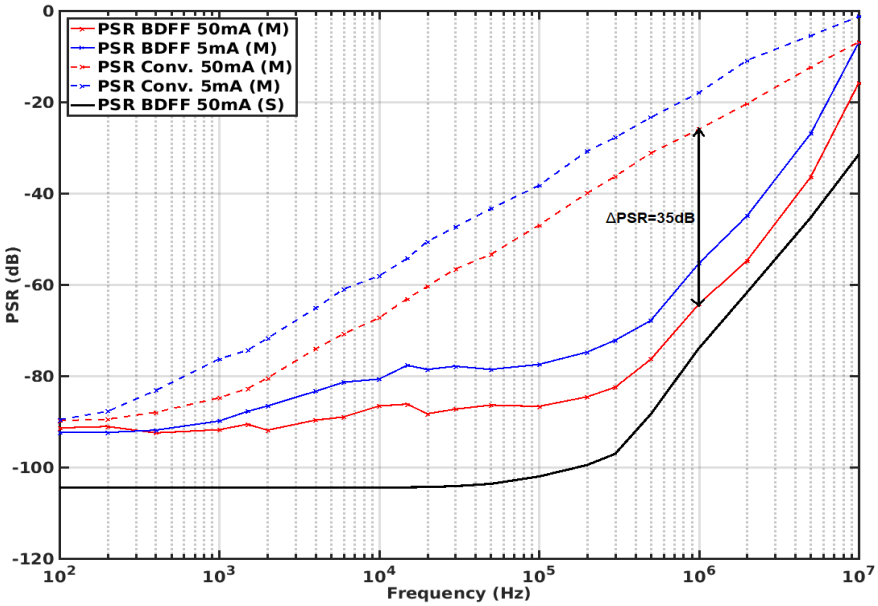


Fig. 34: CL-LDO's Simulated (S) and Measured (M) PSR with and without BDFF. V_{DD} = 1.2 V, V_{OUT} = 1 V, C_L = 400 pF

The proposed CL-LDO achieves a load regulation of 0.3 mV/mA. The three main techniques that contribute to a good load regulation in this CL-LDO are 1) using a Kelvin connection between the load and a sense pin similar to [31], 2) gain-boosting, and 3) utilizing the CL-LDO's unity-gain configuration. The Kelvin connection allows the CL-LDO to include errors, which are introduced due to the bondwire and PCB traces, inside the control loop [31]. The gain-boosting technique, shown in Fig. 18, provides high regulation LG which decreases the voltage error due to I_L variations. The use of the unity-gain configuration improves the CL-LDO's LG avoiding the attenuation introduced by the conventional feedback resistors.

Table 5 shows the performance for recent state-of-the-art LDOs. The proposed CL-LDO achieves the best PSR and T_S tradeoff for a given power reported in the literature. A figure-of-merit (FoM), shown in (39), similar to the one proposed in [15] was used as a starting point, where

T_S along with PSR performance at 1 MHz was included to compare the previously reported works. A smaller FoM means better performance. The proposed CL-LDO has a FoM of 0.16 ps which is 7.5x better than state-of-the-art CL-LDOs. The decrease in area also allowed for the best $I_{L,max}$ per area efficiency. In addition, the proposed CL-LDO also achieves the best line/load regulation and noise figures.

$$\text{FoM} = \frac{T_S}{\text{PSR}_{V/V}} \frac{I_Q}{I_{MAX}} \tag{39}$$

Table 5: Performance summary and comparison with state-of-the-art CL-LDOs

Parameters	**[3]**	**[8]**	**[13]**	**[14]**	**This work**	
Technology (nm)	180	65	130	130	130	
Chip Area (mm^2) x10^{-3}	140	87	2.45	8	**4.6**	
$I_{L,max}$ (mA)	50	25	5	25	50	
V_{IN-OUT} (V)	0.2	0.2	0.2	0.2	0.2	
V_{OUT} (V)	1.6	1	1	0.8	1	
$C_{internal}$ (pF)	28	10	-	0.73	8.4	
$C_{OUT,max}$ (pF)	100	240	-	25	100^+	400^+
C_{OUT} Range (pF)	0-100	0-240	-	0-25	**0-400**	
I_Q (µA)	55	300	99.04	112	42	
Line Regulation (mV/V)	-	3.8	-	2.25	**0.3**	
Load Regulation (µV/mA)	140	42	-	173	**10**	
ΔV_{OUT} (mV) /T_R (ns)	120/100	46/500	50/200	284/0.3	132/100	140/100
PSR (dB@1MHz)	-70	-52	-57.1*	-57	-64	
Noise@100kHz (nV/√Hz)	270	-	-	-	41	
T_S (µs)	< 6	1.7	0.16**	0.19	**0.24**	**0.3**
FoM (ps)	2.09	51.24	4.42	1.2	**0.128**	**0.16**

+ Off-chip
* Measured for a 3−100 mA load step
** For a 3 mA load step

3.6 Conclusion

A CL-LDO with a feedforward V_{DD} noise cancellation technique, adaptive bias and compensation were introduced in this chapter. These techniques allowed for a fast T_S and high PSR. The fabricated BDFF-LDO achieved up to − 90 dB of low-frequency PSR and − 64 dB at 1 MHz for I_L = 50 mA. The CL-LDO has a UGF of 24.7 MHz and an LG of 97.4 dB at I_L = 50 mA. The high LG is achieved by using only one gain stage with gain-boosting, which relaxes the feedback loop's stability requirement. The lack of feedback resistors decreased area and improved noise performance. An adaptive buffer and Miller compensation scheme, controlled by an I_L sense circuit, increased CL-LDO's UGF and slew rate current at large I_L. These also allowed T_S to reach 300 ns during an I_L step. It consumes a minimum I_Q of 42 μA from a 1.2 V V_{DD} and maintains a current efficiency higher than 99.8% across the entire I_L range.

CHAPTER IV

LOW-VOLTAGE ANALOG FILTERING TECHNIQUES

4.1 Introduction

Analog filtering is required in most signal processing applications. The trend towards smaller technologies and lower supply voltage (V_{DD}) makes analog circuit design harder as analog performance decreases with V_{DD}. Low voltage (LV) supplies in modern applications are usually less than 1 V. Therefore, techniques that allow for filters to operate at LV are of crucial importance to fully take advantage of the trend towards smaller CMOS technologies. This chapter describes the state-of-the-art techniques used in LV analog circuit design with emphasis on LV filtering. Subsection 2 discusses the conventional LV techniques such as bulk-bias (BB), bulk-driven (BD), and floating gate (FG). Time-domain amplifiers such as oscillator-based amplifiers and switched-mode operational amplifiers (SMOAs) used for filtering are described in subsection 3 and 4, respectively. Several examples of filters employing the LV techniques are discussed in subsection 5. Finally, conclusions are given in subsection 6.

4.2 Conventional Low-Voltage Amplifiers

Designing operational amplifiers (OpAmps) or operational transconductance amplifiers (OTAs) in LV can be achieved by using techniques such as BD [17-21, 32, 46], BB [17, 21], or FG [47-49]. This subsection describes and compares the most mature LV techniques used in analog circuit design. All the techniques are compared assuming a single-ended (SE) gate-driven (GD) OTA with NMOS or PMOS differential input pair and active loads, as shown in Fig. 35. Where M_N is an NMOS transistor, M_P is a PMOS transistor, V_{CM} is the common-mode voltage, V_{in}^+ is

the small-signal positive input swing, V_{in}^{-} is the small-signal negative input swing, V_{out} is the output node, and I_{Bias} is the bias current.

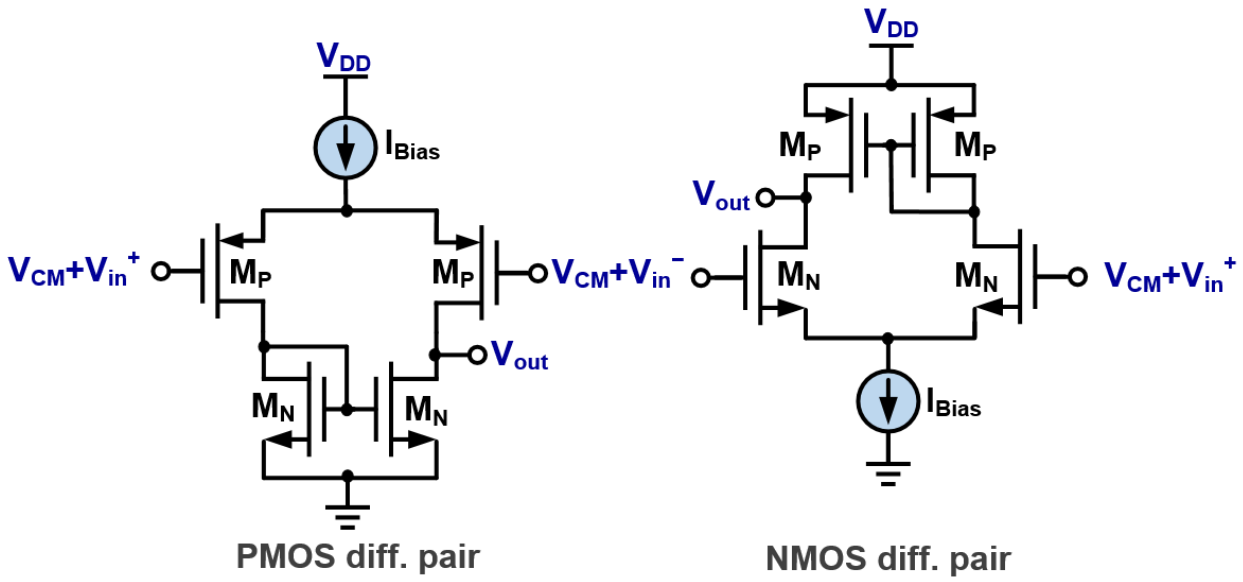


Fig. 35: Gate-driven PMOS and NMOS OTAs

The BD and BB sections are going to assume PMOS input pairs. This is to be consistent with the most common available technologies where only PMOS transistors can fully use their four terminals. However, the formulas can be slightly modified for cases where NMOS transistors use these techniques, i.e., triple-well devices.

4.2.1 Bulk-Driven

BD makes use of the transistor's body, instead of the gate, as an input terminal. When using BD, the gate is used as a voltage bias terminal to turn ON the transistor and the bulk or body is

used as signal input. Since the threshold voltage (V_T) limitation in gate-to-source voltage (V_{GS}) is what usually limits the input signal swing, rail-to-rail input common-mode range (ICMR) can be achieved when using the body as the input terminal. Assuming the gate terminal is high enough to keep the transistor ON, the bulk-to-source voltage (V_{BS}) wouldn't turn OFF the transistor even if its voltage swing is high. Fig. 36 shows the transistor representation, with the bulk terminal explicitly drawn, and small-signal model of PMOS and NMOS transistors, respectively. Where C_{gs} is the gate-to-source capacitance, C_{gd} is the gate-to-drain capacitance, g_m is the gate transconductance, g_{mb} is the bulk transconductance, r_{ds} is the transistor's output resistance, and C_{bs} is the bulk-to-source capacitance.

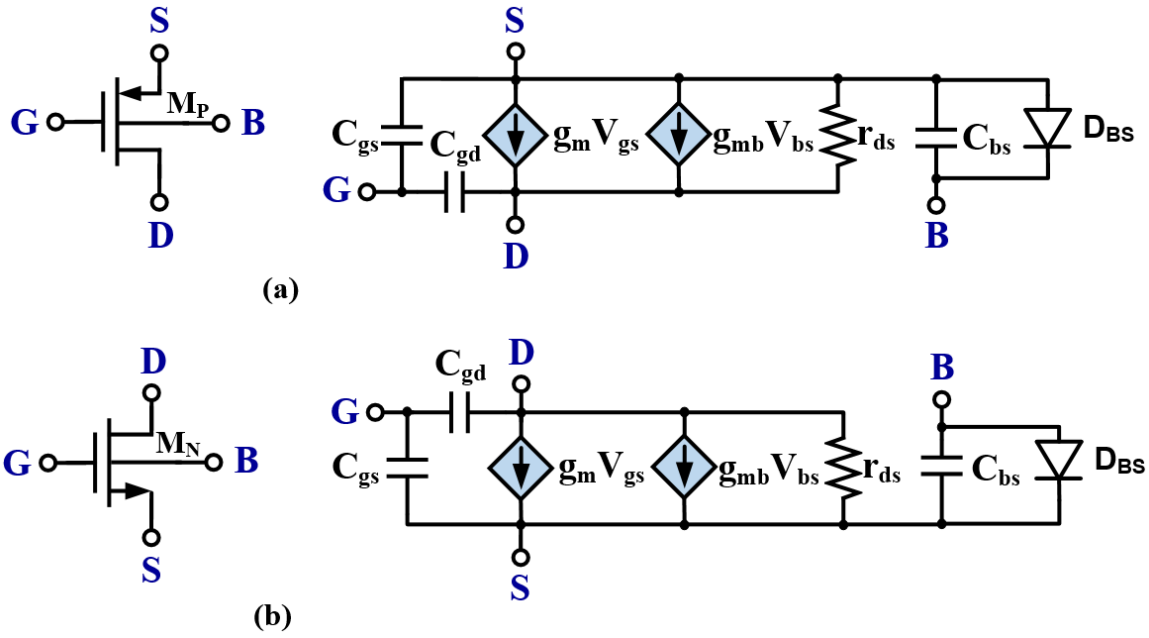


Fig. 36: Bulk-driven (a) PMOS and (b) NMOS transistors and their small signal equivalent

The transconductance of a BD amplifier is determined by g_{mb} instead of g_m. The g_{mb} for a PMOS transistor is given by [42]:

$$g_{mb,P} = \frac{\gamma_b g_{m,P}}{2\sqrt{2\phi_F - V_{SB}}} \tag{40}$$

where V_{SB} is the source-to-body voltage, ϕ_F is the Fermi level in volts, and γ_b is the body effect parameter in $\sqrt{V}$. The Fermi level is usually about 0.3 V [42]. The body effect (γ_b) is less than one, which means the transconductance of a bulk-driven OTA (BD-OTA) is smaller compared to a gate-driven OTA (GD-OTA). The typical g_{mb} is 3 to 10 times smaller than g_m [42].

A smaller g_{mb} for the same current and transistor's size is the trade-off from using the bulk as the input terminal. Having a smaller g_{mb} means that a BD-OTA has a higher input-referred noise, higher input-referred offset, smaller gain-bandwidth product (GBW), and smaller dc gain compared to a conventional GD-OTA for the same amount of power consumption.

Another disadvantage is increased area and slightly worst mismatch. A gate-driven PMOS input pair shares the same bulk among the input transistors. In a BD PMOS input pair, however, the two PMOS have to be in separate bulks or substrates. This increases the area between the two since there is a minimum distance that has to be put in place between their bulks or n-doped regions to minimize the risk for latch-up. The additional separation between the PMOS input pair adds mismatch due to the increased distance between the BD input transistors, their different bulk area, and their different bulk's doping.

The input impedance of a BD transistor ($R_{in,BD}$) is mainly determined by the bulk-to-source diode (D_{BS}) impedance. The real part of this impedance can me modeled as [50]:

$$R_{in,BD} \approx \frac{V_t}{J_0 A_D} e^{-\frac{V_{SB}}{V_t}} \approx \frac{V_t}{I_S} e^{-\frac{V_{SB}}{V_t}} \tag{41}$$

where V_t is the thermal voltage in volts, J_0 is the saturation current density in A/cm^2, A_D is D_{BS}' area in cm^2, and I_S is D_{BS}' saturation current in amperes.

As V_{SB} increases, the input impedance decreases and the input current can increase significantly. Because this impedance depends on D_{BS}, its temperature dependence follows the same profile as a pn junction, which decreases exponentially with increased temperature. This causes the current through the bulk to increase exponentially with temperature. Another consideration to keep the input impedance high is to prevent the parasitic lateral and vertical BJTs to fully turn ON [18]. Compared to the GD-OTA, the BD-OTA has a smaller input impedance. This is because the ideal GD transistor has an infinite real impedance at low-frequencies compared to its BD counterpart. The input capacitance of a BD-OTA is higher compared to a GD-OTA [20].

Since in a differential pair the bias current remains fixed, the output conductance of a BD transistor remains the same as a GD-OTA, both of them given by:

$$g_{out} = g_{ds,N} + g_{ds,P} \tag{42}$$

where g_{out}, $g_{ds,N}$, and $g_{ds,P}$ are the OTA's output conductance, NMOS transistor output conductance, and PMOS transistor output conductance, respectively.

Using (40) and (42), the BD-OTA's DC gain, 3 dB bandwidth (BW_{3dB}), and GBW can be obtained. The DC gain in V/V, BW_{3dB} in Hz, and GBW in Hz are given by (43), (44), and (45), respectively.

$$\text{DC Gain}_{BD} = \frac{\gamma_b}{2\sqrt{2\phi_F - V_{SB}}}\left(\frac{g_{m,P}}{g_{ds,N}+g_{ds,P}}\right) \tag{43}$$

$$BW_{3dB,BD} = \frac{g_{ds,N}+g_{ds,P}}{2\pi C_{out}} \tag{44}$$

where C_{out} is the total capacitance seen at V_{out}.

$$GBW_{BD} = \frac{\gamma_b}{2\sqrt{2\phi_F - V_{SB}}}\left(\frac{g_{m,P}}{2\pi C_{out}}\right) \tag{45}$$

In terms of noise, the BD-OTA has an increased input-referred noise spectral density ($\upsilon_{n,in}^2$) compared to its GD counterpart. This happens because g_{mb}, as given in (40), is smaller than g_m while the output noise remains the same for both architectures. Assuming a differential pair with active loads, the output noise spectral density ($\upsilon_{n,out}^2$) is given by:

$$\upsilon_{n,out,BD}^{\ 2} = 8kT\gamma_n\left(g_{m,N}+g_{m,P}+g_{mb,P}\right) \tag{46}$$

where k is the Boltzmann constant given by $1.38\text{x}10^{-23}$ J/°K, T is the temperature in degrees Kelvin, and γ_n is the noise coefficient, which is a technology dependent parameter.

To get $\upsilon_{n,in}^2$, $\upsilon_{n,out}^2$ is divided by the square of the BD-OTA's transconductance, given by (40), to obtain:

$$\upsilon_{n,in,BD}{}^2 = \frac{32kT\gamma_n\left(2\phi_F - V_{SB}\right)\left(g_{m,N}+g_{m,P}+g_{mb,P}\right)}{\left(\gamma_b g_{m,P}\right)^2} \tag{47}$$

Eq. (47) shows that the input-referred noise is higher than the GD-OTA's input-referred noise. If the BD-OTA's noise is normalized with respect to the GD-OTA, (48) can be obtained which can be used to determine the noise penalty paid compared to using a GD-OTA with similar characteristics to a BD-OTA.

$$\frac{\upsilon_{n,in,BD}{}^2}{\upsilon_{n,in,GD}{}^2} = \frac{4\left(2\phi_F - V_{SB}\right)}{\gamma_b{}^2}\left(1+\frac{g_{mb,P}}{g_{m,N}+g_{m,P}}\right) \tag{48}$$

The output swing of a BD-OTA, assuming all transistors need to remain in saturation, is determined by the swing at V_{out}. This swing is given by:

$$V_{CM}+V_{T,P}-\Delta V_{T,P} > V_{out} > V_{dsat,N} \tag{49}$$

where $\Delta V_{T,P}$ and $V_{dsat,N}$ are the V_T change due to having a dc voltage applied at V_{SB} different than zero, and NMOS' drain-to-source saturation voltage. Assuming a PMOS transistor, $\Delta V_{T,P}$ is given by:

$$\Delta V_{T,P} = \gamma_b\left(\sqrt{2\phi_F} - \sqrt{2\phi_F - V_{SB}}\right) \tag{50}$$

The absolute voltage swing at the output of a BD-OTA to be determined by:

$$V_{out,pk\text{-}pk,BD} = V_{CM} + V_{T,P} - \Delta V_{T,P} - V_{dsat,N} \tag{51}$$

In comparison with a GD-OTA's output swing, which is given by:

$$V_{out,pk\text{-}pk,GD} = V_{CM} + V_{T,P} - V_{dsat,N} \tag{52}$$

The output swing when using a BD-OTA is decreased due to the smaller V_T in the PMOS input transistors. The SNR is given by:

$$SNR = \frac{V_{out,RMS}}{\sqrt{\left(\upsilon_{n,out}{}^2\right)(BW)}} \tag{53}$$

Using (44), (46) and (51) into (53), the SNR of a BD-OTA is given by:

$$SNR_{BD} = \frac{V_{CM} + V_{T,P} - \Delta V_{T,P} - V_{dsat,N}}{8\sqrt{kT\gamma_n \left(g_{m,N} + g_{m,P} + g_{mb,P}\right)\left(\frac{g_{ds,N} + g_{ds,P}}{2\pi C_{out}}\right)}} \tag{54}$$

The ICMR for a BD-OTA can be analyzed by using Fig. 37, which represents a PMOS differential input pair half-side circuit, where V_G is used as bias voltage for the input transistors and the parasitic D_{BS} between source and bulk is explicitly shown. The worst side of a differential pair in terms of ICMR is the one with the diode connected transistor.

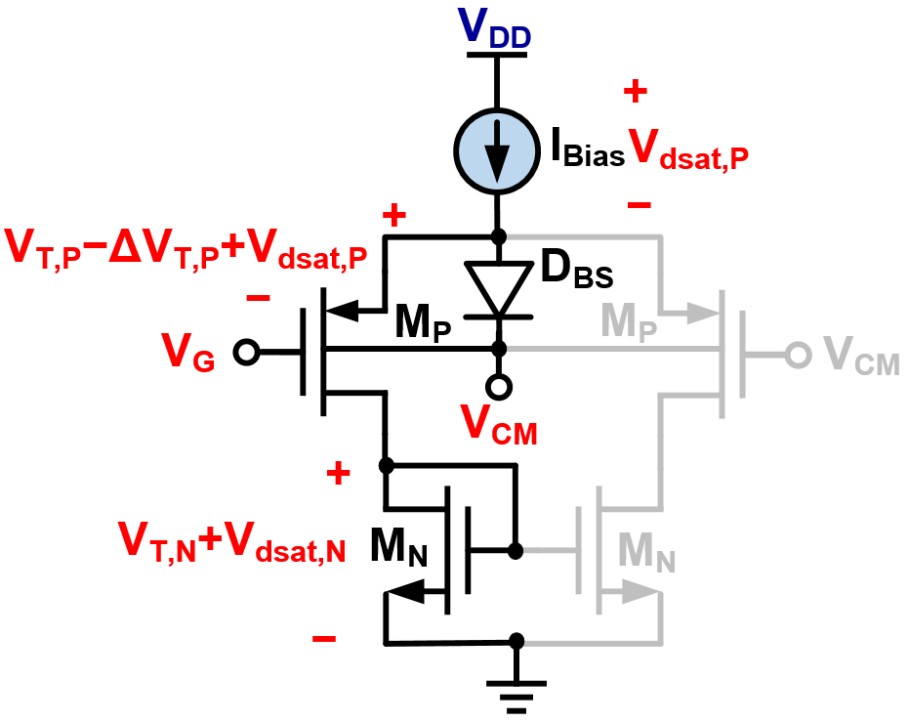


Fig. 37: Half-side single-ended BD-OTA circuit for ICMR analysis

The BD-OTA has two conditions to meet in order to keep all transistors in saturation, one is with respect to V_G and one with respect to V_{CM}. Starting with V_G, the minimum voltage allowed can be solved by using KVL in Fig. 37 to obtain:

$$V_G + V_{T,P} + V_{dsat,P} - \Delta V_{T,P} > V_{dsat,P} + V_{dsat,N} + V_{T,N} \tag{55}$$

where using (50) into (55) we get:

$$V_G + V_{T,P} + V_{dsat,P} - \gamma_b \left(\sqrt{2\phi_F} - \sqrt{2\phi_F - V_{SB}} \right) > V_{dsat,P} + V_{dsat,N} + V_{T,N} \tag{56}$$

The worst-case scenario happens around $V_{SB} \approx 2\phi_F$, which causes $\Delta V_{T,P}$ to increase to its maximum, or in other words to decrease the effective V_T to its lowest potential. This is the point where an increase in V_{SB} wouldn't decrease V_T further. With the previous assumption and solving for V_G, (57) can be obtained.

$$V_G > V_{dsat,N} + V_{T,N} + \gamma_b \sqrt{2\phi_F} - V_{T,P} \tag{57}$$

Using KVL in Fig. 37 for the maximum V_G at the limits of saturation, (58) can be obtained.

$$V_{DD} - V_{dsat,P} > V_G + V_{dsat,P} + V_{T,P} - \Delta V_{T,P} \tag{58}$$

The worst-case scenario happens when V_{SB} becomes negative, or when $V_B > V_S$. This causes $\Delta V_{T,P}$ to change polarity and increase the effective V_T for the PMOS input pair. Using (50) and assuming the polarity of V_{SB} has changed, the maximum limit for V_G is given by:

$$V_G < V_{DD} - 2V_{dsat,P} - V_{T,P} - \gamma_b \left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F} \right) \tag{59}$$

which can be combined with (57) to obtain (60) giving the allowable voltage range for V_G.

$$V_{dsat,N} + V_{T,N} + \gamma_b \sqrt{2\phi_F} - V_{T,P} < V_G < V_{DD} - 2V_{dsat,P} - V_{T,P} - \gamma_b \left(\sqrt{2\phi_F + V_{BS}} - \sqrt{2\phi_F} \right) \tag{60}$$

In a similar fashion to what was done for V_G, the range for V_{CM} can be obtained by using KVL in Fig. 37. The maximum V_{CM} is limited by the saturation of the tail source and V_G as can be seen in (59). As V_{CM} goes higher than the source voltage, V_S, the effective V_T increases therefore decreasing the tail source's voltage headroom. In practice, by setting V_G properly, V_{CM} can be allowed to swing up to V_{DD} and even higher without putting any transistors out of saturation.

The main concern for BD-OTAs is the negative swing at V_{CM}. As can be seen in Fig. 37, there is a parasitic diode between the source and the bulk, shown as D_{BS}, that needs to be kept OFF if proper operation is to be maintained. This can be mathematically expressed by:

$$V_{SB} < V_D \approx 0.7\ \text{V} \tag{61}$$

where V_D is D_{BS}' turn ON voltage, roughly approximated to 0.7 V.

Using KVL in Fig. 37, using (50) to replace $\Delta V_{T,P}$, and assuming the lowest $V_{T,P}$ to find V_{SB} in (61), the required limit is given by:

$$V_G + V_{dsat,P} + V_{T,P} - \gamma_b\sqrt{2\phi_F} - V_{CM} < 0.7\ \text{V} \tag{62}$$

Solving for V_{CM} in (62), the minimum V_{CM} is given by:

$$V_{CM} > V_G + V_{dsat,P} + V_{T,P} - \gamma_b\sqrt{2\phi_F} - 0.7\ \text{V} \tag{63}$$

and the V_{CM} voltage range in a BD-OTA is given by:

$$V_{DD} \geq V_{CM} > V_G + V_{dsat,P} + V_{T,P} - \gamma_b \sqrt{2\phi_F} - 0.7\ \text{V} \tag{64}$$

Eq. (64) shows that setting V_G helps to determine the BD-OTA's ICMR.

To compare, the ICMR for a GD-OTA can be analyzed by using Fig. 38, which represents a PMOS differential input pair half-side circuit. The worst side of a differential pair in terms of ICMR is the one with the diode connected transistor.

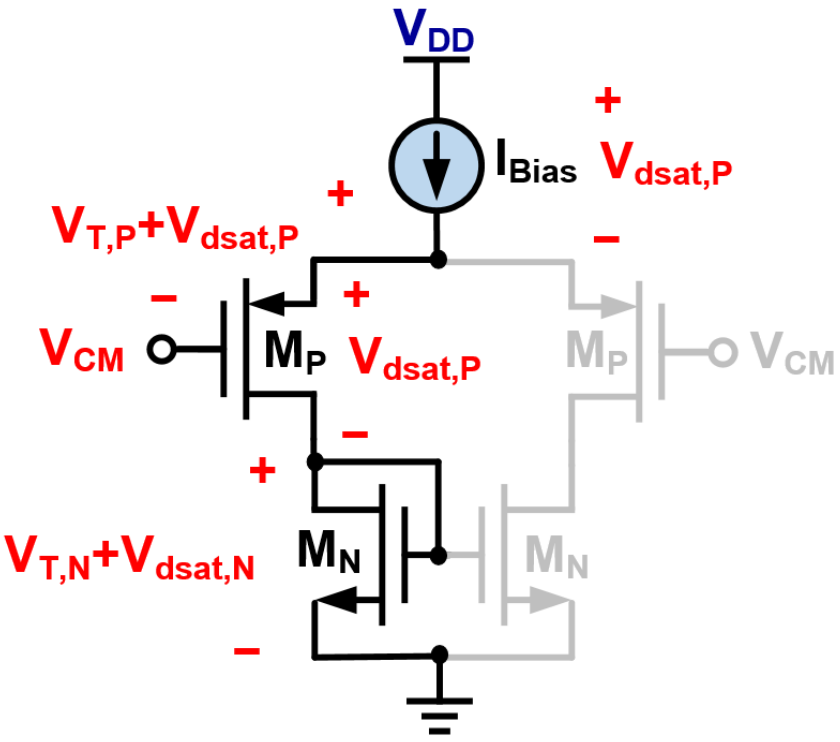


Fig. 38: Half-side single-ended GD-OTA circuit for ICMR analysis

Using KVL in Fig. 38 for the maximum V_{CM}, see (65), and minimum V_{CM}, see (66), at the limits of saturation, (67) can be obtained. Eq. (67) provides the limits for the input voltage so that all transistors remain in saturation.

$$V_{DD} - V_{dsat,P} > V_{CM} + V_{T,P} + V_{dsat,P} \tag{65}$$

$$V_{CM} + V_{T,P} + V_{dsat,P} > V_{T,N} + V_{dsat,N} + V_{dsat,P} \tag{66}$$

$$V_{DD} - 2V_{dsat,P} - V_{T,P} > V_{CM} > V_{T,N} + V_{dsat,N} - V_{T,P} \tag{67}$$

To determine the minimum V_{DD} required for a BD-OTA, KVL can be used in Fig. 37. Two paths need to be considered, the path from ground to V_{DD} and the path from V_G to V_{DD}. For the BD-OTA, V_{CM} has little impact in the minimum V_{DD}, its only contribution is through the bulk effect in the modulation of V_T. The minimum V_{DD} required for these two paths is given in (68) and (69), respectively.

$$V_{DD} > V_G + V_{T,P} - \Delta V_{T,P} + 2V_{dsat,P} \tag{68}$$

$$V_{DD} > V_{dsat,N} + V_{T,N} + 2V_{dsat,P} \tag{69}$$

To compare, KVL in Fig. 38 can be used to determine the minimum required V_{DD} for a GD-OTA. Two paths need to be considered, the path from ground to V_{DD} and the path from V_{CM} to V_{DD}. The minimum V_{DD} required for these two paths is given in (70) and (71), respectively.

$$V_{DD} > V_{CM} + V_{T,P} + 2V_{dsat,P} \tag{70}$$

$$V_{DD} > V_{dsat,N} + V_{T,N} + 2V_{dsat,P} \tag{71}$$

In a standard p-type substrate CMOS technology only PMOS devices can be used as BD devices without any additional mask or fabrication step. If an NMOS transistor is required to be used with a BD input it needs to be a triple-well device, which adds additional fabrication steps and cost.

The BD technique has been used extensively in analog circuits for OpAmps and OTAs [17-21, 32, 46], filters [17, 51], LDOs [2, 8, 13, 16], and several other circuit applications. Note that those are just some references and not all are included.

4.2.2 Bulk-Bias

BB uses the body terminal to apply a dc voltage and forward bias the MOSFET's D_{BS}. BB was used first in digital circuits to adjust their speed and power consumption after fabrication [52-55]. This was achieved by changing the V_T of transistors, usually that of a PMOS, to balance the trade-off between speed and power consumption. Similar to BD, PMOS devices can use bulk-biasing without any additional fabrication steps, but requires triple-well devices for NMOS if using a p-type substrate technology. The difference between BD and BB is that the former applies an ac signal in addition to a dc forward bias voltage to the bulk, whereas the latter only applies dc voltage. Forward biasing D_{BS} decreases the nominal V_T of a PMOS as shown in [56]:

$$V_T = V_{T0} + \gamma_b \left[\sqrt{2\phi_F - V_{SB}} - \sqrt{2\phi_F} \right] \tag{72}$$

where V_{T0} is V_T with a zero V_{SB}.

By decreasing V_T, transistors can operate at a lower V_{DD}. However, V_{SB} should be limited to $|V_{SB}| < 0.5$ V to prevent fully turning ON D_{BS} and causing increased power consumption, or turning ON the parasitic vertical BJT with the main substrate [57]. However, an OTA using BB cannot achieve rail-to-rail ICMR compared to a BD-OTA. BB only improves the ICMR due to γ_b being less than one, which decreases the effective V_T reduction for a given V_{SB}.

Assuming the BB is applied to a PMOS input pair, the effective g_m and g_{out} remain the same as a GD-OTA, as long as the bias current is constant. Therefore, the g_m of a BB-OTA ($g_{m,BB}$) can be expressed as:

$$g_{m,BB} = \sqrt{2\mu_p C_{OX} \frac{W}{L} I_D} \tag{73}$$

where μ_p is the hole mobility, C_{OX} is the gate oxide capacitance, W is the transistor's width, L is the transistor's length, and I_D is the drain current.

The output impedance of a BB-OTA is the same as GD-OTA, and is given by (42).

Using (42) and (73), the BB-OTA's DC gain, BW_{3dB}, and GBW can be obtained. The DC gain in V/V, BW_{3dB} in Hz, and GBW in Hz are given by (74), (75), and (76), respectively.

$$\text{DC Gain}_{BB} = \frac{g_{m,P}}{g_{ds,N} + g_{ds,P}} \tag{74}$$

$$BW_{3dB,BB} = \frac{g_{ds,N} + g_{ds,P}}{2\pi C_{out}} \tag{75}$$

$$GBW_{BB} = \frac{g_{m,P}}{2\pi C_{out}} \tag{76}$$

BB increases the noise in an OTA compared to a GD-OTA. The noise increase is due to the additional noise current through g_{mb}. Although this increase is small because g_{mb} is smaller than g_m, it should be taken into consideration in noise critical designs. In a BB-OTA, $\upsilon_{n,out}^2$ is given by:

$$\upsilon_{n,out,BB}^2 = 8kT\gamma_n \left(g_{m,N} + g_{m,P} + g_{mb,P}\right) \tag{77}$$

To get $\upsilon_{n,in,BB}^2$, $\upsilon_{n,out,BB}^2$ is divided by the square of the BB-OTA's transconductance, given by (73), to obtain:

$$\upsilon_{n,in,BB}^2 = \frac{8kT\gamma_n \left(g_{m,N} + g_{m,P} + g_{mb,P}\right)}{g_{m,P}^2} \tag{78}$$

Eq. (78) shows that the input-referred noise is higher than the GD-OTA's input-referred noise. If the BB-OTA's noise is normalized with respect to the GD-OTA, (79) can be obtained which can be used to determine the noise penalty paid compared to using a GD-OTA with similar characteristics to a BB-OTA.

$$\frac{\upsilon_{n,in,BB}^2}{\upsilon_{n,in,GD}^2} = 1 + \frac{g_{mb,P}}{g_{m,N} + g_{m,P}} \tag{79}$$

The output swing for the BB-OTA is the same as the BD-OTA, which is given by (51). Using (51), (75) and (77) into (53), the SNR of a BB-OTA is given by:

$$SNR_{BB} = \frac{V_{CM} + V_{T,P} - \Delta V_{T,P} - V_{dsat,N}}{8\sqrt{kT\gamma_n \left(g_{m,N} + g_{m,P} + g_{mb,P}\right)\left(\frac{g_{ds,N} + g_{ds,P}}{2\pi C_{out}}\right)}} \tag{80}$$

The ICMR for a BB-OTA can be analyzed by using Fig. 39, which represents a PMOS differential input pair half-side circuit. The worst side of a differential pair in terms of ICMR is the one with the diode connected transistor.

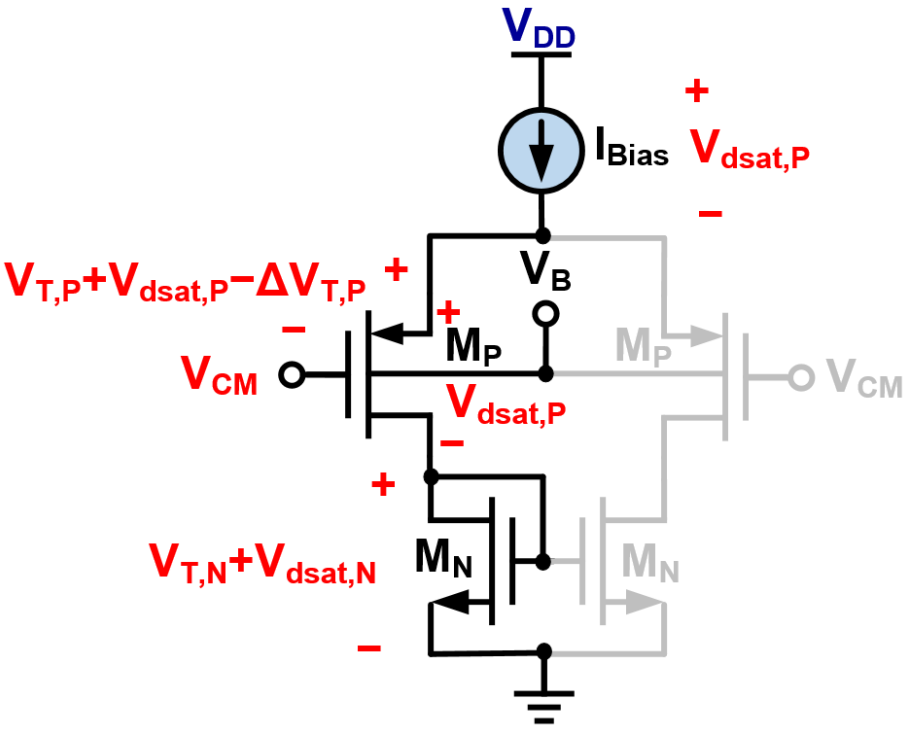


Fig. 39: Half-side single-ended BB-OTA circuit for ICMR analysis

Using KVL in Fig. 39 for the maximum V_{CM}, see (81), and minimum V_{CM}, see (82), at the limits of saturation, (83) can be obtained. Eq. (83) provides the limits for the input voltage so that all transistors remain in saturation.

$$V_{DD} - V_{dsat,P} > V_{CM} + V_{T,P} + V_{dsat,P} - \Delta V_{T,P} \tag{81}$$

$$V_{CM} + V_{T,P} + V_{dsat,P} - \Delta V_{T,P} > V_{T,N} + V_{dsat,N} + V_{dsat,P} \tag{82}$$

$$V_{DD} - 2V_{dsat,P} - V_{T,P} + \Delta V_{T,P} > V_{CM} > V_{T,N} + V_{dsat,N} - V_{T,P} + \Delta V_{T,P} \tag{83}$$

The BB-OTA increases its maximum swing voltage by the term given by $\Delta V_{T,P}$. This increase is due to the fact that the PMOS input pair decreases its V_T due to the BB effect. However, the same effect also increases the minimum V_{CM} allowed at the gate. Subtracting the maximum limit from the minimum limit in (83), the ICMR is given by:

$$ICMR_{BB} = V_{DD} - 2V_{dsat,P} - V_{T,N} - V_{dsat,N} \tag{84}$$

To determine the minimum V_{DD} required for a BB-OTA, KVL can be used in Fig. 39. Two paths need to be considered, the path from ground to V_{DD} and the path from V_{CM} to V_{DD}. The minimum V_{DD} required for these two paths is given in (85) and (86), respectively.

$$V_{DD} > V_{CM} + V_{T,P} - \Delta V_{T,P} + 2V_{dsat,P} \tag{85}$$

$$V_{DD} > V_{dsat,N} + V_{T,N} + 2V_{dsat,P} \tag{86}$$

In general, V_{SB} doesn't have to be generated with a voltage source. In [21], a fixed current is forced in the bulk terminal of a PMOS transistor to generate its V_{SB}. This also limits V_{SB} and avoids turning on the parasitic BJT of MOSFETs.

4.2.3 Floating-Gate MOSFETs

FG-MOSFETs are commonly used for erasable programmable read-only memory (EPROM), electrically EPROM (EEPROM), and flash memories. Because FG-MOSFETs work similar to conventional MOSFETs, applications in digital and analog circuits starting to appear in the late 1980s [48]. Conceptually, a FG-MOSFET works as a conventional MOSFET but instead of one gate, it can have multiple gates to control its behavior. Fig. 40 shows a two-input FG NMOS and PMOS, along with the small signal representation of the FG structure. Each input is capacitive coupled to the transistor's channel and is also attenuated by the capacitor divider between the two inputs [47]. CMOS processes with double polysilicon layers can make use of FG-MOSFETs without additional cost [48]. For simulation purposes, FG-MOSFETs can be emulated in conventional CMOS technologies. To properly emulate them, real capacitors are added in parallel with large resistors so that the proper dc operating point can be obtained. The extra capacitors emulate the two floating gate capacitances, C_{in} and C_{Bias} in Fig. 40, and have to be larger than the transistor's C_{GS}. In addition, the RC time constant for each real capacitor has to be equal.

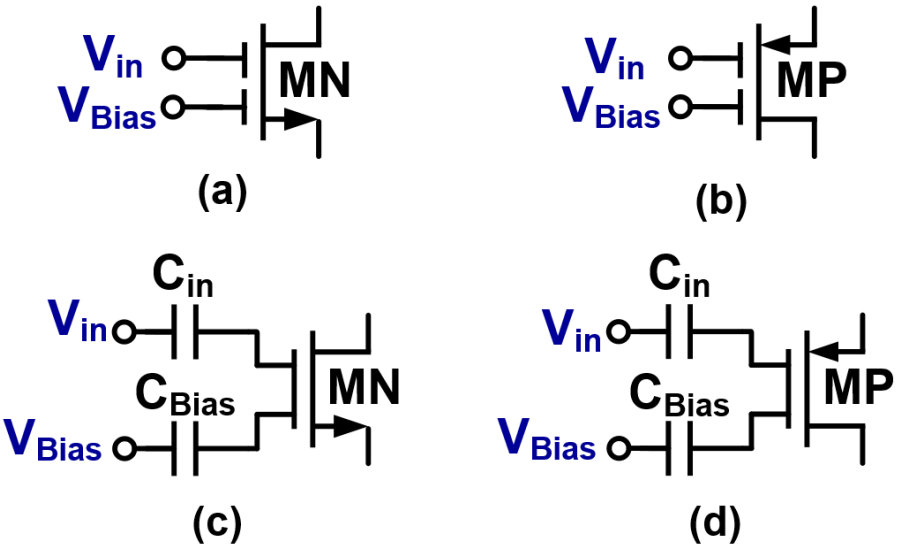


Fig. 40: Two-input floating-gate (a) NMOS, (b) PMOS devices and their small signal equivalent

FG-MOSFETs combine the voltage applied to both inputs to generate a potential at the FG, which is the terminal between the capacitors and the MOSFET channel. The voltage seen at the FG is given by [58]:

$$V_{FG} = \frac{C_{in} V_{in} + C_{Bias} V_{Bias}}{C_{in} + C_{Bias}} \tag{87}$$

Assuming one input is used as signal and the other as a voltage bias, this technique adds a degree of freedom for setting the input common-mode voltage at the transistor's gate. If V_{Bias} is set close to V_{DD} (GND) for an NMOS (PMOS) transistor, V_{CM} at the FG can be set at a higher (lower) voltage compared to the input signal's V_{CM} [58].

This can be used to increase the effective OTA's ICMR. Also, common-mode rejection ratio (CMRR) is improved. This increase in CMRR happens because now the effective input V_{CM}

at the FG-MOSFET's gate is less dependent on the input voltage compared to using conventional MOSFETs as input pairs. The input impedance of a floating-gate OTA (FG-OTA) is affected by the capacitor divider present at the two inputs. The FG-OTA's input impedance ($R_{in,FG}$) is given by:

$$R_{in,FG} = \frac{1}{s}\left(\frac{C_{in}+C_{Bias}}{C_{in}C_{Bias}}\right) \tag{88}$$

Due to the signal attenuation at the gate, the g_m of a FG-OTA is reduced compared to a GD-OTA. The FG-OTA's g_m is given by:

$$g_{m,FG} = \left(\frac{C_{in}}{C_{in}+C_{Bias}}\right) g_{m,N/P} \tag{89}$$

The output impedance remains the same as previous OTAs discussed in this chapter, and is given by (42).

Using (42) and (89), the FG-OTA's DC gain, BW_{3dB}, and GBW can be obtained. The DC gain in V/V, BW_{3dB} in Hz, and GBW in Hz are given by (90), (91) and (92), respectively.

$$\text{DC Gain}_{FG} = \frac{C_{in}}{C_{in}+C_{Bias}}\left(\frac{g_{m,N/P}}{g_{ds,N}+g_{ds,P}}\right) \tag{90}$$

$$BW_{3dB,FG} = \frac{g_{ds,N}+g_{ds,P}}{2\pi C_{out}} \tag{91}$$

$$GBW_{FG} = \frac{C_{in}}{C_{in}+C_{Bias}}\left(\frac{g_{m,N/P}}{2\pi C_{out}}\right) \tag{92}$$

Due to a decrease in g_m, FG increases the noise in an OTA compared to a GD-OTA. In a FG-OTA, $\upsilon_{n,out}^2$ is given by:

$$\upsilon_{n,out,FG}{}^2 = 8kT\gamma_n\left(g_{m,N}+g_{m,P}\right) \tag{93}$$

To get $\upsilon_{n,in,FG}^2$, $\upsilon_{n,out,FG}^2$ is divided by the square of the FG-OTA's transconductance, given by (89), to obtain:

$$\upsilon_{n,in,FG}{}^2 = \left(1+\frac{C_{Bias}}{C_{in}}\right)^2 \frac{8kT\gamma_n\left(g_{m,N}+g_{m,P}\right)}{g_{m,N/P}{}^2} \tag{94}$$

Eq. (94) shows that the input-referred noise is higher than the GD-OTA's input-referred noise. If the FG-OTA's noise is normalized with respect to the GD-OTA, (95) can be obtained which can be used to determine the noise penalty paid compared to using a GD-OTA with similar characteristics to a FG-OTA.

$$\frac{\upsilon_{n,in,FG}{}^2}{\upsilon_{n,in,GD}{}^2} = \left(1+\frac{C_{Bias}}{C_{in}}\right)^2 \tag{95}$$

The increased ICMR and CMRR due to the FG-MOSFETs comes with some trade-offs. The inherent capacitor divider in FG-MOSFETs attenuates the effective open-loop gain, increases input-referred noise, and decreases GBW and g_m. Eq. (89) shows that this trade-off can be adjusted by the capacitor sizing between C_{in} and C_{Bias}. A larger C_{Bias} would increase ICMR and CMRR at the cost of increased input-referred noise and decreased g_m.

The output swing for the FG-OTA is the same as the GD-OTA, which is given by (52). Using (52), (91) and (93) into (53), the SNR of a FG-OTA is given by:

$$SNR_{FG} = \frac{V_{CM} + V_{T,P/N} - V_{dsat,N/P}}{8\sqrt{kT\gamma_n \left(g_{m,N} + g_{m,P}\right)\left(\frac{g_{ds,N} + g_{ds,P}}{2\pi C_{out}}\right)}} \tag{96}$$

which is the same SNR a GD-OTA has.

The ICMR for a FG-OTA can be analyzed by using Fig. 41, which represents a PMOS differential input pair half-side circuit. The worst side of a differential pair in terms of ICMR is the one with the diode connected transistor.

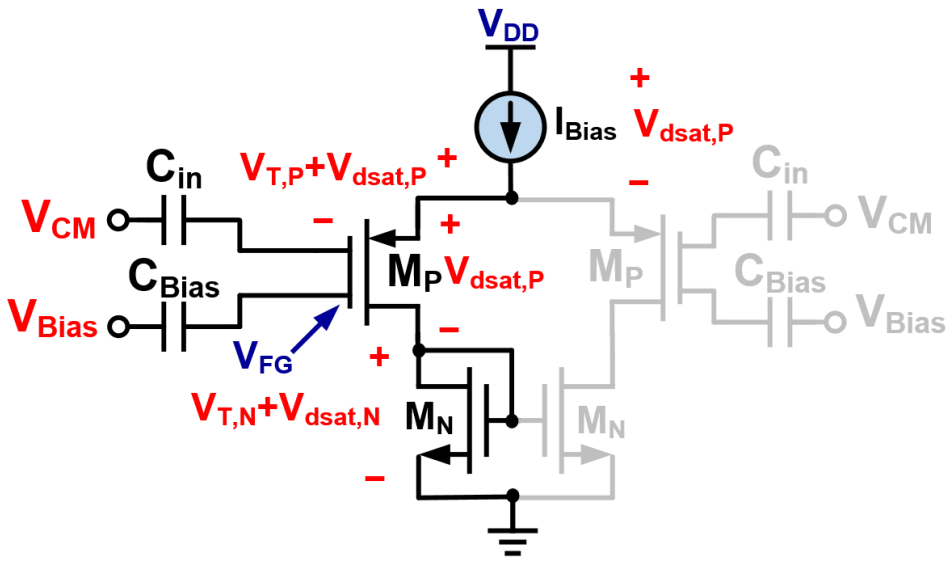


Fig. 41: Half-side single-ended FG-OTA circuit for ICMR analysis

Similar to the BD-OTA, the FG-OTA has an additional degree of freedom by using V_{Bias}. Therefore, the minimum and maximum conditions for both V_{CM} and V_{Bias} are discussed.

Using KVL in Fig. 41 for the maximum V_{FG}, see (97), and minimum V_{FG}, see (98), at the limits of saturation, (99) can be obtained, which provides the limits for the input voltage so that all transistors remain in saturation.

$$V_{DD} - V_{dsat,P} > V_{FG} + V_{T,P} + V_{dsat,P} \tag{97}$$

$$V_{FG} + V_{T,P} + V_{dsat,P} > V_{T,N} + V_{dsat,N} + V_{dsat,P} \tag{98}$$

$$V_{DD} - 2V_{dsat,P} - V_{T,P} > V_{FG} > V_{T,N} + V_{dsat,N} - V_{T,P} \tag{99}$$

Using (87) into (97) and (98), the maximum and minimum voltage can be found in (100) and (101) respectively, and then solved in terms of either V_{CM} or V_{Bias}.

$$C_{in}V_{CM}+C_{Bias}V_{Bias}<\left(V_{DD}-2V_{dsat,P}-V_{T,P}\right)\left(C_{in}+C_{Bias}\right) \tag{100}$$

$$C_{in}V_{CM}+C_{Bias}V_{Bias}>\left(V_{T,N}+V_{dsat,N}-V_{T,P}\right)\left(C_{in}+C_{Bias}\right) \tag{101}$$

Solving (100) and (101) for V_{CM}, (102) and (103) can be obtained.

$$V_{CM}<\left(V_{DD}-2V_{dsat,P}-V_{T,P}\right)\left(1+\frac{C_{Bias}}{C_{in}}\right)-\frac{C_{Bias}}{C_{in}}V_{Bias} \tag{102}$$

$$V_{CM}>\left(V_{T,N}+V_{dsat,N}-V_{T,P}\right)\left(1+\frac{C_{Bias}}{C_{in}}\right)-\frac{C_{Bias}}{C_{in}}V_{Bias} \tag{103}$$

Solving (100) and (101) for V_{Bias}, (104) and (105) can be obtained.

$$V_{Bias}<\left(V_{DD}-2V_{dsat,P}-V_{T,P}\right)\left(1+\frac{C_{in}}{C_{Bias}}\right)-\frac{C_{in}}{C_{Bias}}V_{CM} \tag{104}$$

$$V_{Bias}>\left(V_{T,N}+V_{dsat,N}-V_{T,P}\right)\left(1+\frac{C_{in}}{C_{Bias}}\right)-\frac{C_{in}}{C_{Bias}}V_{CM} \tag{105}$$

In addition to V_{Bias} as a tuning mechanism to increase ICMR, FG-OTAs also have C_{Bias} and C_{in} as degrees of freedom. All these degrees of freedom make FG-OTAs the most flexible in terms of input V_{CM} voltage range compared to all the other architectures. An FG-OTA can be made to tolerate rail-to-rail swing at the input with proper sizing of all parameters.

To determine the minimum V_{DD} required for a FG-OTA, KVL can be used in Fig. 41. Two paths need to be considered, the path from ground to V_{DD} and the path from V_{FG}, given in (87), to V_{DD}. The minimum V_{DD} required for these two paths is given in (106) and (107), respectively.

$$V_{DD} > \frac{C_{in}V_{CM} + C_{Bias}V_{Bias}}{C_{in} + C_{Bias}} + V_{T,P} + 2V_{dsat,P} \tag{106}$$

$$V_{DD} > V_{dsat,N} + V_{T,N} + 2V_{dsat,P} \tag{107}$$

Table 6 shows a comparison of the main performance metrics for GD, BD, BB, and FG OTAs that have been discussed in subsection 2.

Table 6: Analog Low-Voltage Techniques Comparison Table[1]

	Gate-Driven	Floating Gate	Bulk-Driven	Bulk-Bias
g_m (mS)	$\sqrt{2\mu_{n/p}C_{OX}\frac{W}{L}I_D}$	$\left(\frac{C_{in}}{C_{in}+C_{Bias}}\right)g_{m,N/P}$	$\frac{\gamma_b g_{m,P}}{2\sqrt{2\phi_F - V_{SB}}}$	$\sqrt{2\mu_p C_{OX}\frac{W}{L}I_D}$
Input imp. (Ω)	$\frac{1}{sC_{gg}}$	$\frac{C_{in}+C_{Bias}}{sC_{in}C_{Bias}}$	$\frac{V_t}{I_S}e^{-\frac{V_{SB}}{V_t}}$	$\frac{1}{sC_{gg}}$
Output imp. (Ω)	$g_{ds,N}+g_{ds,P}$	$g_{ds,N}+g_{ds,P}$	$g_{ds,N}+g_{ds,P}$	$g_{ds,N}+g_{ds,P}$
DC gain (V/V)	$\frac{g_{m,N/P}}{g_{ds,N}+g_{ds,P}}$	$\left(\frac{C_{in}}{C_{in}+C_{Bias}}\right)\frac{g_{m,N/P}}{g_{ds,N}+g_{ds,P}}$	$\frac{\gamma_b}{2\sqrt{2\phi_F - V_{SB}}}\left(\frac{g_{m,P}}{g_{ds,N}+g_{ds,P}}\right)$	$\frac{g_{m,P}}{g_{ds,N}+g_{ds,P}}$
BW (Hz)	$\frac{g_{ds,N}+g_{ds,P}}{2\pi C_{out}}$	$\frac{g_{ds,N}+g_{ds,P}}{2\pi C_{out}}$	$\frac{g_{ds,N}+g_{ds,P}}{2\pi C_{out}}$	$\frac{g_{ds,N}+g_{ds,P}}{2\pi C_{out}}$
GBW (Hz)	$\frac{g_{m,N/P}}{2\pi C_{out}}$	$\left(\frac{C_{in}}{C_{in}+C_{Bias}}\right)\frac{g_{m,N/P}}{2\pi C_{out}}$	$\frac{\gamma_b}{2\sqrt{2\phi_F - V_{SB}}}\left(\frac{g_{m,P}}{2\pi C_{out}}\right)$	$\frac{g_{m,P}}{2\pi C_{out}}$
$v_{n,out}^2$ (V^2/Hz)	$8kT\gamma_n(g_{m,N}+g_{m,P})$		$8kT\gamma_n(g_{m,N}+g_{m,P}+g_{mb,P})$	
$v_{n,in}^2$ (V^2/Hz)	$\frac{8kT\gamma_n(g_{m,N}+g_{m,P})}{g_{m,N/P}^2}$	$\left(1+\frac{C_{Bias}}{C_{in}}\right)^2\frac{8kT\gamma_n(g_{m,N}+g_{m,P})}{g_{m,N/P}^2}$	$\frac{32kT\gamma_n(2\phi_F - V_{SB})(g_{m,N}+g_{m,P}+g_{mb,P})}{(\gamma_b g_{m,P})^2}$	$\frac{8kT\gamma_n(g_{m,N}+g_{m,P}+g_{mb,P})}{g_{m,P}^2}$
V_{out} swing (V)	$V_{CM}+V_{T,P/N}-V_{dsat,N/P}$		$V_{CM}+V_{T,P}-\Delta V_{T,P}-V_{dsat,N}$	
Input V_{CM} range (V)	$V_{CM} > V_{T,N}+V_{dsat,N}-V_{T,P}$ $V_{CM} < V_{DD}-2V_{dsat,N}-V_{T,P}$	$V_{CM} > (V_{T,N}+V_{dsat,N}-V_{T,P})\left(1+\frac{C_{Bias}}{C_{in}}\right)-\frac{C_{Bias}}{C_{in}}V_{Bias}$ $V_{CM} < (V_{DD}-2V_{dsat,N}-V_{T,P})\left(1+\frac{C_{Bias}}{C_{in}}\right)-\frac{C_{Bias}}{C_{in}}V_{Bias}$	$V_{CM} > V_G+V_{dsat,P}+V_{T,P}-\gamma_b\sqrt{2\phi_F}-0.7V$ $V_{CM} \le V_{DD}$	$V_{CM} > V_{T,N}+V_{dsat,N}-V_{T,P}+\Delta V_{T,P}$ $V_{CM} < V_{DD}-2V_{dsat,N}-V_{T,P}+\Delta V_{T,P}$
SNR (V/V)	$\frac{V_{CM}+V_{T,P/N}-V_{dsat,N/P}}{8\sqrt{kT\gamma_n(g_{m,N}+g_{m,P})\left(\frac{g_{ds,N}+g_{ds,P}}{2\pi C_{out}}\right)}}$		$\frac{V_{CM}+V_{T,P}-\Delta V_{T,P}-V_{dsat,N}}{8\sqrt{kT\gamma_n(g_{m,N}+g_{m,P}+g_{mb,P})\left(\frac{g_{ds,N}+g_{ds,P}}{2\pi C_{out}}\right)}}$	
Min. V_{DD} (V)	$V_{DD} > V_{CM}+2V_{dsat,P}+V_{T,P}$ $V_{DD} > V_{T,N}+V_{dsat,N}+2V_{dsat,P}$	$V_{DD} > \frac{C_{in}V_{CM}+C_{Bias}V_{Bias}}{C_{in}+C_{Bias}}+V_{T,P}+2V_{dsat,P}$ $V_{DD} > V_{T,N}+V_{dsat,N}+2V_{dsat,P}$	$V_{DD} > V_G+2V_{dsat,P}+V_{T,P}-\Delta V_{T,P}$ $V_{DD} > V_{T,N}+V_{dsat,N}+2V_{dsat,P}$	$V_{DD} > V_{CM}+2V_{dsat,P}+V_{T,P}-\Delta V_{T,P}$ $V_{DD} > V_{T,N}+V_{dsat,N}+2V_{dsat,P}$

[1] All bulk-bias and bulk-driven OTA formulas assume a PMOS differential input pair with NMOS active load

The drawback of all of the previously mentioned approaches is that they require triple-well devices or additional fabrication steps, except for BD or BB PMOS input differential pairs. This makes these circuits and design techniques technology dependent, and prevents them from being used in conventional CMOS fabrication nodes.

4.3 Oscillator-based Amplifiers

As V_{DD} decreases, OTA gain also decreases. This makes the design of closed-loop systems hard in LV domains, since a high loop-gain is one of the critical specifications required from OpAmps or OTAs.

Oscillator amplifiers were first introduced in [59], where a voltage-controlled oscillator (VCO) was used as an OpAmp in an RF modulator.

Oscillators can be either voltage-controlled oscillators (VCOs) or current-controlled oscillators (CCOs). VCOs (CCOs) take an analog voltage (current) input and convert it to a phase domain analog signal. The output is a rail-to-rail voltage signal that now contains the information in the phase domain. The transfer function of a VCO is [59]:

$$\frac{\phi_{out}(s)}{V_{in}(s)} = \frac{K_{VCO}}{s} \tag{108}$$

where ϕ_{out} is the output phase, V_{in} is the input voltage, and K_{VCO} is the gain of the VCO. The most common VCO's symbol representation is shown in Fig. 42.

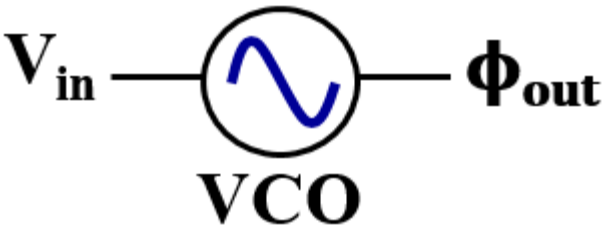


Fig. 42: VCO's symbolic representation

An oscillator works as an integrator and provides an ideally infinite gain at low frequencies independently of V_{DD}. This is their main advantage compared to conventional voltage-mode OpAmps or OTAs, where the gain tends to decrease as V_{DD} decreases.

Oscillator-based OpAmps' main building blocks are an oscillator and a phase-to-voltage or phase-to-current converter. Although any type of oscillators could be used, ring oscillators are the most popular [59-61] for their simplicity and scalability. The block diagram of a 3-stage voltage-controlled ring oscillator is shown in Fig. 43, along with its basic transistor-level implementation shown in Fig. 44. The control voltage ($V_{Control}$) is used to vary the oscillation frequency of the ring oscillator.

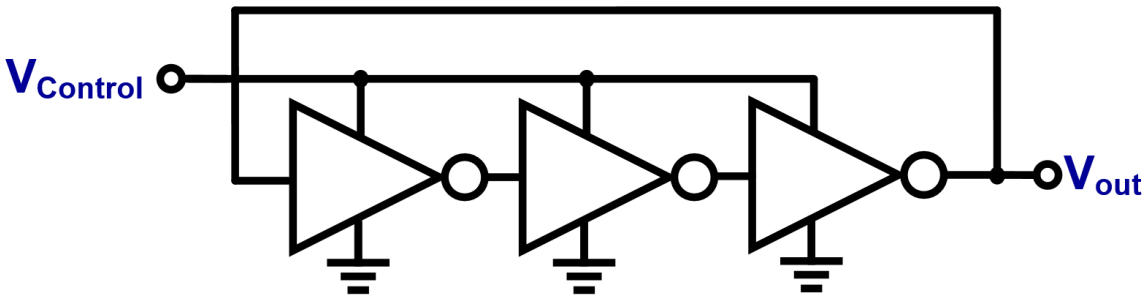


Fig. 43: 3-stage voltage-controlled ring oscillator block diagram

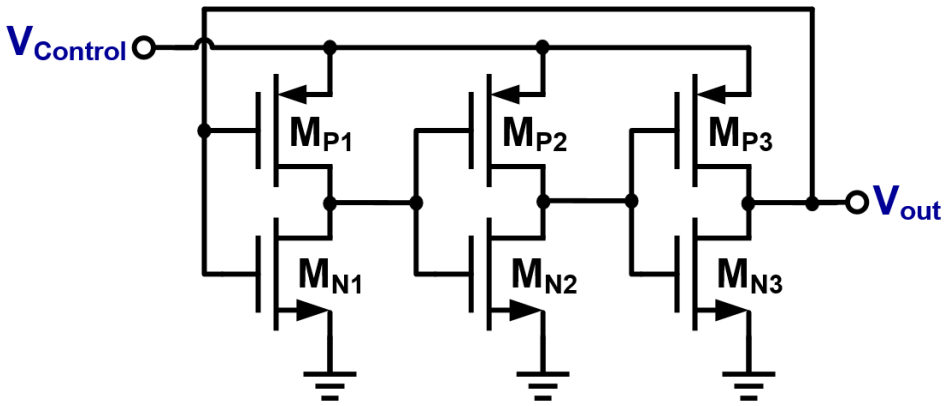


Fig. 44: 3-stage voltage-controlled ring oscillator transistor-level diagram

After the oscillator, a phase detector (PD) and a charge pump (CP) are commonly used to convert the phase signal back to an output current. The PD compares the VCO output with a reference clock (REF_{CLK}) and creates a pulse modulated signal that the CP converts to an output current. A phase-frequency detector (PFD) can also be used instead of the PD. Combining the VCO's transfer function, the PD/PFD, and CP, the transfer function of a VCO-based OpAmp can be expressed as [60]:

$$\frac{I_{out}(s)}{V_{in}(s)} = \frac{K_{VCO}K_{PD/PFD}K_{CP}}{s} \tag{109}$$

where $K_{PD/PFD}$ and K_{CP} are the PD/PFD gain and CP gain, respectively. For this particular VCO-based architecture, it can be seen that it resembles a transconductance stage similar to an OTA except for the infinite dc gain and low-frequency pole. The block diagram representation for the complete VCO-based OpAmp is shown in Fig. 45, along with a conventional SE transistor-level

diagram shown in Fig. 46. In Fig. 46, M_{BP}, M_{BN}, M_{SP}, and M_{SN} form the CP circuit, where M_{BP} and M_{BN} are the PMOS and NMOS bias current sources, respectively. M_{SP} and M_{SN} act as switches and function to choose the desired polarity of the output current (I_{out}).

Fig. 45: VCO-based OpAmp block diagram

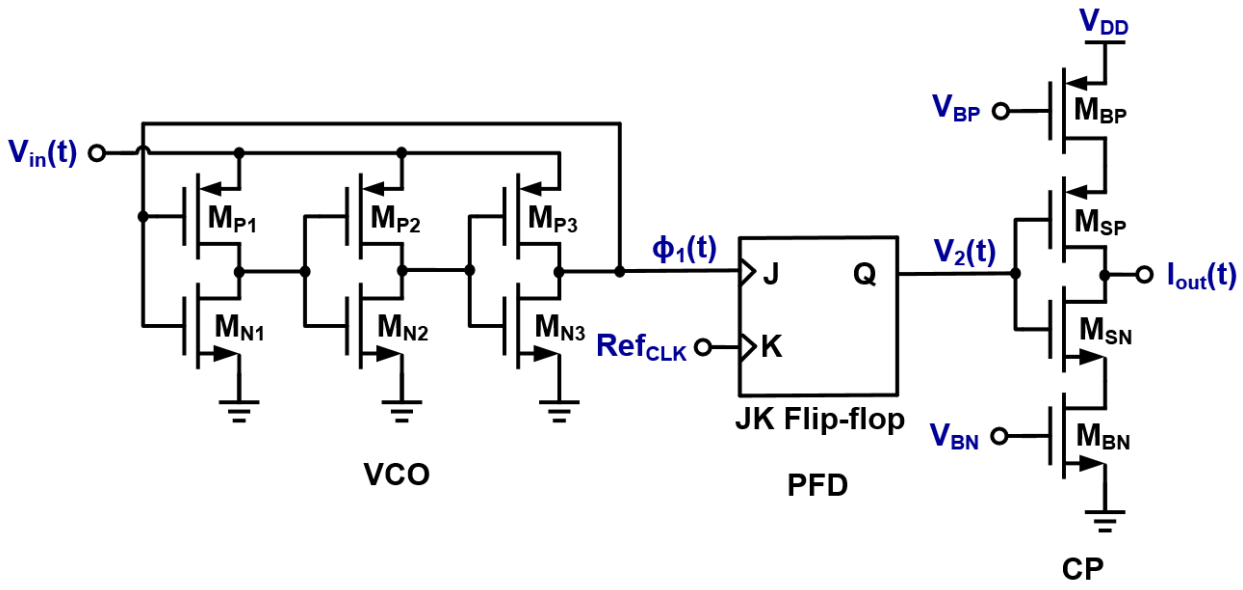


Fig. 46: VCO-based OpAmp transistor-level diagram

Ring oscillator amplifiers suffer from spurious tones due to the oscillator's switching behavior, non-linearities, noise, and additional phase shift due to parasitic poles [60]. The main oscillator, in oscillator-based OTAs, has to oscillate at frequencies higher than the highest frequency processed by the OTA. This adds complexity and power consumption and worsens as the filter's BW is increased to the tens of MHz range.

The RO-based architecture is voltage scalable and its digital-cell based implementation makes it a good candidate for further technology scaling. However, multiple clock phases and high oversampling ratios, compared to the filter's BW, are required. This RO time domain implementation achieves the required dc gain but adds significant complexity and power due to the multiple clock phase generation and clock frequency required to achieve high BWs.

4.4 Switched-Mode Operational Amplifiers

Another approach to LV operation is to use SMOAs, which were first introduced in [62, 63]. Instead of a Class-A or Class-AB output stage, SMOAs use a switched-mode output stage known as a Class-D output, similar to those used in switching dc-dc converters and audio amplifiers. Class-A and Class-AB linear amplifiers require the output transistors to remain in saturation to maintain good linearity performance [64]. This saturation voltage limits the maximum acceptable output voltage swing to keeps transistors in saturation. The decrease in V_{DD} makes this problem more dominant and troublesome. Due to the switching behavior of a Class-D output stage an almost rail-to-rail output swing is possible since no limitations in saturation voltage are required at the output node. However, the output stage's switching nature is not well suited for further analog processing since it consists of a signal that switches between V_{DD} and ground. This switching contains strong components at the modulation frequency (f_M) and its harmonics and

increases the dynamic range requirements of the coming circuits. The strength of these f_M and harmonic components are usually at full scale voltage (FSV). If the input signal is to be recovered with a good signal-to-noise and distortion ratio (SNDR) then these components need to be attenuated.

Fig. 47 shows a block level diagram of a SE SMOA. It consists of a linear amplifier, G_{M1} in Fig. 47, a pulse-width modulation (PWM) stage and a LPF. The linear amplification usually consist of an OTA structure, which could be implemented using current state-of-the-art techniques for LV linear amplification as the ones described previously in subsection 2. The first stage determines the ICMR and total SMOA's input-referred noise. The next block is a modulator that transforms the input voltage's signal information to a width modulated output waveform. After modulation, the signal contains strong components located at f_M and its harmonics. To remove those high frequency harmonics, and recover the input signal with a good SNDR, a LPF is required after the SMOA's output. It is assumed that the LPF, if designed correctly, will not affect the input signal's BW and only removes high frequency components at f_M and its harmonics. After filtering, once the high frequency harmonics are removed, only the original input signal remains within the BW of interest where it has been amplified by the linear and modulation stages.

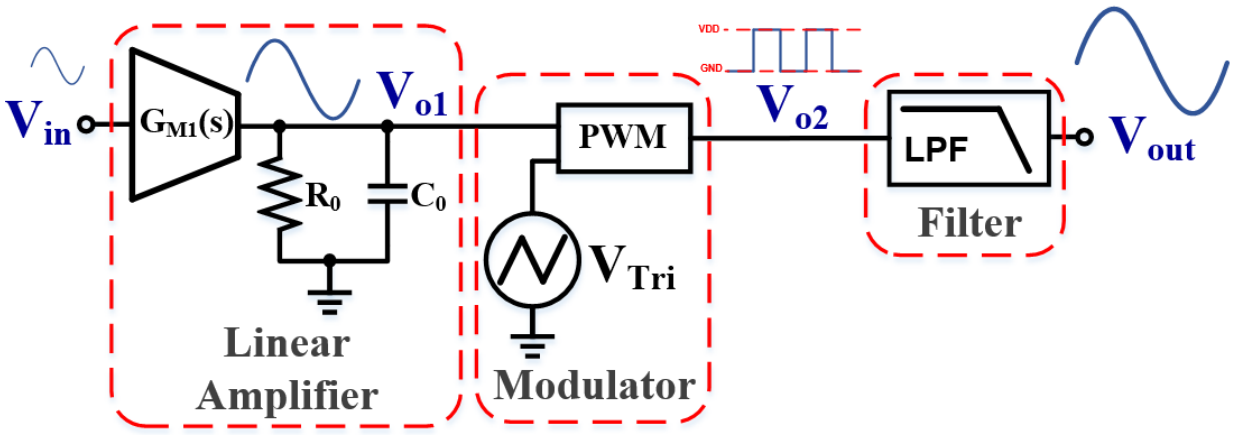


Fig. 47: Conventional SMOA architecture

The concept behind the operation of an SMOA can also be explained in the frequency domain with the help of Fig. 48. Fig. 48(a) shows the frequency domain representation of the signal at the SMOA's input, after which it is amplified by a linear amplification block, as seen in Fig. 48(b). It has been assumed that the linear stage introduces no harmonic distortion. After the amplification, the signal is width modulated with a high frequency f_M signal, this creates harmonic components at f_M and its harmonics along with $f_M \pm f_{in}$, as can be seen in Fig. 48(c). In general, PWM is performed so that the signal can be delivered with high efficiency. The implementation of PWM stages, mainly class-D amplifiers, is well-understood and its advantages on efficiency are the main reason for this modulation. Other areas such as audio amplification and switching dc-dc converters use extensive use of this type of output stages due to that reason. The harmonic content present along the amplified input signal, see Fig. 48(c), need to be removed so that the signal is recovered. A LPF is added after the PWM so that the high frequency harmonic contents can be removed as shown in Fig. 48(d).

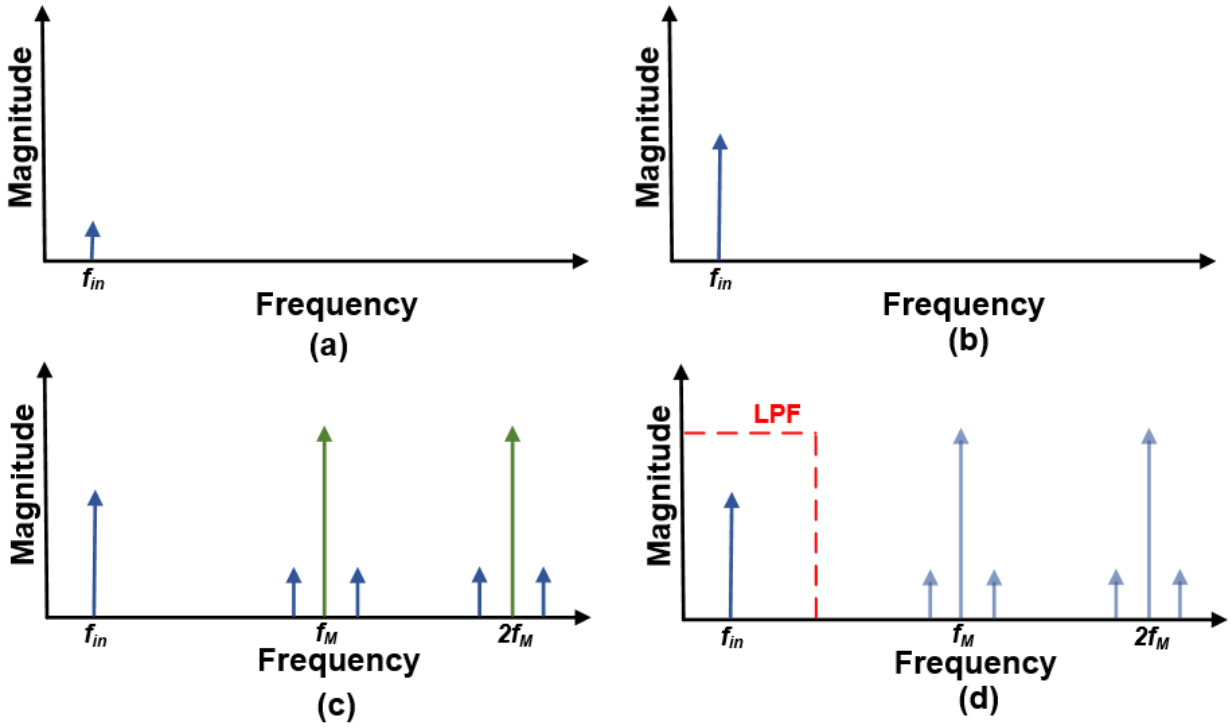


Fig. 48: Frequency domain operation of SMOA architectures: (a) input signal (V_{in}), (b) input signal after linear amplification (V_{o1}), (c) modulated signal after the PWM block (V_{o2}), (d) output signal after LPF (V_{out})

4.4.1 Modulation Background

Analog pulse modulation is characterized by the use of an analog reference as one of the inputs to the modulator [65]. The four basic pulse modulation techniques are Pulse Amplitude Modulation (PAM), PWM, Pulse Position Modulation (PPM) and Pulse Density Modulation (PDM) [65]. An analysis of advantages, disadvantages, and spectral properties of each modulation technique is done in [65]. Based on that analysis and due to its better spectral properties and low complexity over other forms of modulation, PWM is the preferred choice for the modulation used in SMOAs. Furthermore in [66], an extensive mathematical analysis and background in PWM is

provided. Table 7 shows the selection of parameters that a designer can chose for analog PWM. Proper combination of PWM parameters depends on a particular design and circuit architecture. Each set of parameters has different spectral properties and implementations.

The most common waveforms used in analog PWM are a sawtooth and a triangle waveform. Based on the parameters from Table 7, a sawtooth waveform is considered a constant-frequency trailing-edge modulation and a triangle waveform is considered a constant-frequency double-edge modulation. Examples of these waveforms are shown in Fig. 49, where the blue dashed-line represents the analog signal being sampled or compared.

Table 7: Analog PWM parameters

<table>
<tr><th>Implementation</th><th>Supply Voltage Reference</th><th>Frequency</th><th>Modulation Signal</th></tr>
<tr><td rowspan="6">Analog (Natural sampling)</td><td>Unipolar modulation</td><td rowspan="3">Constant</td><td>Trailing-edge</td></tr>
<tr><td rowspan="2">Bipolar modulation</td><td>Leading-edge</td></tr>
<tr><td>Double-edge</td></tr>
<tr><td>Unipolar modulation</td><td rowspan="3">Variable</td><td>Constant ON-time, variable OFF time</td></tr>
<tr><td rowspan="2">Bipolar modulation</td><td>Constant OFF-time, variable ON-time</td></tr>
<tr><td>Hysteretic Control</td></tr>
</table>

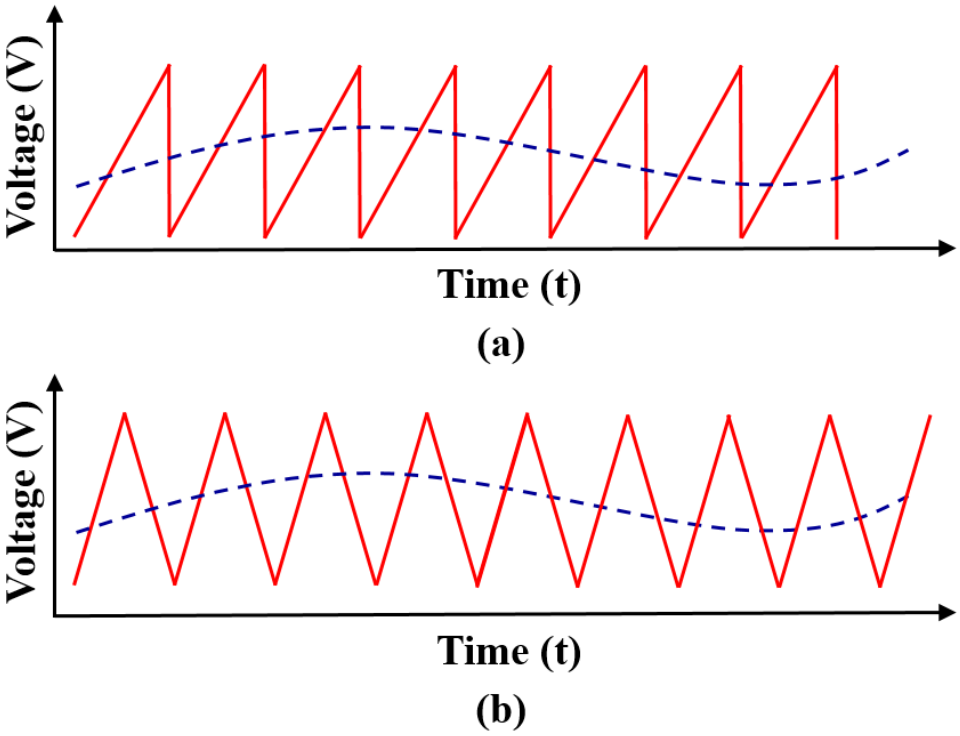


Fig. 49: Popular waveforms used in PWM systems: (a) sawtooth, (b) triangle

The low-frequency gain of a PWM modulator is given by:

$$A_{PWM} = \frac{V_{DD}}{V_{m,pk\text{-}pk}} e^{-sT_D} \tag{110}$$

where A_{PWM}, $V_{PWM,pk\text{-}pk}$, and T_D are the modulator's gain, modulation signal's peak-to-peak voltage, and modulators delay, respectively.

4.4.2 Non-linear versus linear output stage

A non-linear output stage offers several advantages over its linear counterpart. Since PWM is free of signal distortion [66], the output stage of an SMOA is theoretically linear. An OTA has harmonics of the signal frequency [62]. In terms of power consumption, a non-linear output stage requires no quiescent current due to the switching behavior of transistors, contrary to linear output stages where quiescent current needs to be flowing in the output stage. In a non-linear output stage the open loop signal component swing is limited only by the minimum pulse-width (t_{min}) that the modulator can handle, thus the output can vary from $V_{DD}t_{min}f_{PWM}$ to $V_{DD} - V_{DD}t_{min}f_{PWM}$ [62]. Therefore switching output stages benefit from a smaller and faster technology. The output stage's switching behavior allows an SMOA to be designed with a low open-loop output impedance. This allows to have minimum propagation delay, which pushes the output pole to high frequencies. The modulator's transfer function is given by $A_{PWM}e^{-st_d}$, where t_d is the PWM modulator's propagation delay [62].

Compared to a linear output stage, a non-linear output stage benefits in terms of speed, power consumption, and output swing from technology scaling. The major drawback is that a strong component at f_M is introduced. This component's amplitude is usually at FSV and needs to be effectively removed from the input signal before further processing.

4.4.3 Current disadvantages of SMOAs

The current disadvantages of SMOAs are going to be discussed in this section. Although the work presented in [62] claims that the voltage swing limitations are solved, this is only true for the output stage. The SMOA presented there still requires a LV analog linear amplification stage. It also uses a BB technique in its NMOS input differential pair, which requires triple well NMOS

devices. This linear stage comes with the same swing limitations as conventional LV analog amplifiers. However, the gain of the PWM block following the linear stage helps in this regard.

Due to the modulation process, the output of an SMOA is corrupted by the presence of a strong component at f_M and its harmonics, which also have spurious frequency components around them. To obtain a signal with good SNDR, these strong components have to be filtered. A straightforward approach is to introduce a passive LPF at the output; however, this puts stringent constraints in area to reduce the power located at f_M and its harmonics.

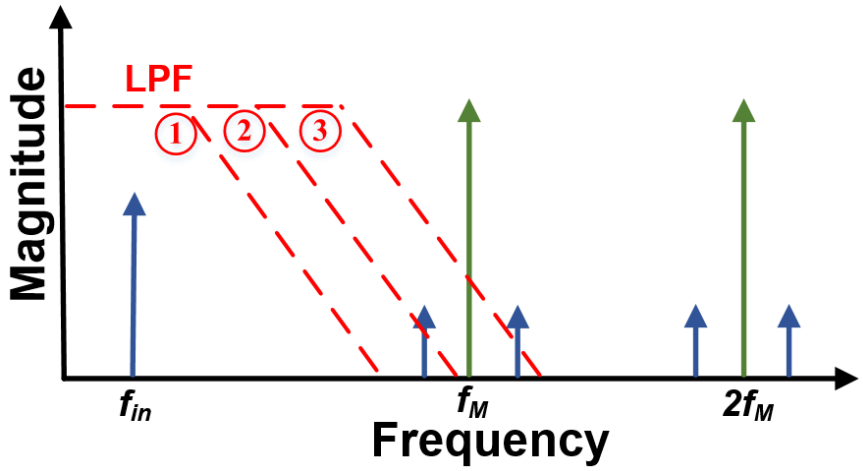


Fig. 50: SMOA's LPF effect on harmonic removal

Let's consider the behavior of a first-order passive LPF in the attenuation of the harmonic components. Fig. 50 shows the frequency domain representation of the signal with three different cases of LPF corner, the effect of a non-ideal 20 dB/decade roll-off is going to be considered. The first LPF is able to remove the components completely but the other two cases do not and a certain percentage of the harmonics is not removed. This appears at the output as spurious tone that can

corrupt the signal and decrease spurious-free dynamic range (SFDR). Fig. 51 shows the SMOA's output voltage after the LPF with the three different LPF examples. As the LPF's BW is increased more harmonics remain. The reader may be tempted to think that the best approach is to use a very low BW LPF, however this comes at a price. If the LPF is passive, having a very low BW implies large passive components, and therefore, large area. In addition, the LPF introduces an additional pole in the system which decreases UGF, if the LPF is the dominant pole, or decreases PM if the LPF is a non-dominant pole. For those reasons, the use of a passive LPF is problematic and may be the reason the SMOA presented in [62] used a digital finite impulse response (FIR) filter instead.

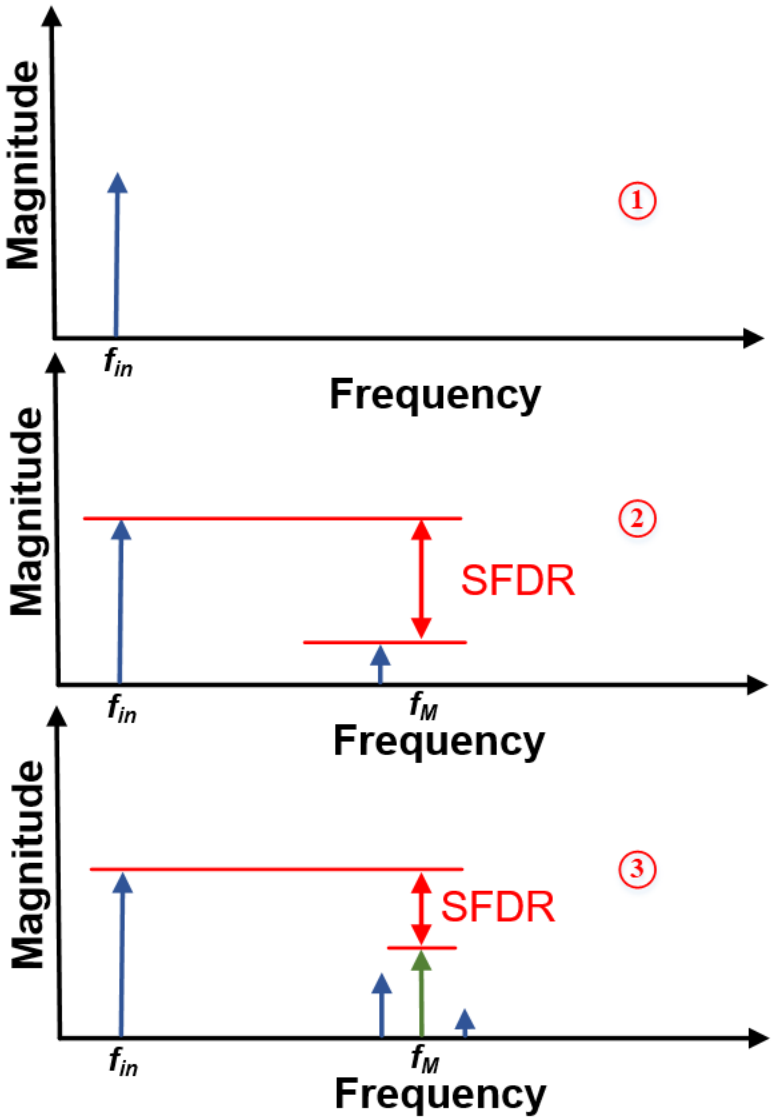


Fig. 51: SMOA's frequency-domain output voltage representation after using different LPFs in Fig. 50

Another drawback of state-of-the-art SMOAs is the high power consumption needed in the modulation stages due to the high f_M required. The higher the f_M, the easier it is to remove by using a LPF and the better it is the output signal after the LPF. Instead of increasing f_M, an option is to use multiple phases. By using multiple phases the effective f_M is increased by N times, where N is

the number of phases. The drawback is the increased complexity and area required for each additional phase generation and processing.

Alternative solutions that could potentially simplify the design process while achieving good f_M reduction are desired and may become an active area of research.

Finally, if we assume that the SMOA is going to be used in a big system, the introduction of a switching component adds to substrate noise and may interact with other analog circuits in the die. Although this problem is not unique to SMOAs since several other systems, i.e. RF receivers, audio amplifiers, and some analog-to-digital converters (ADCs) have the same problem.

4.5 Reported Filtering Applications using Low-voltage Techniques

The previously discussed techniques have been used for designing LV filters and other filtering applications. The first BD-OTA was used in a continuous-time (CT) g_m-C filter in [67], a PMOS input pair with BD is used as the main stage. The main reason for using the BD-OTA in [67] was to achieve a small g_m to allow for low cut-off frequencies (f_o) required in audio range applications while keeping the capacitance small.

Small transconductances are also required in medical electronics. FG and BD techniques, among others, were compared in [68] for the design of a low-g_m OTA. These OTAs were compared in terms of power, SNR, linearity, and area. The inherent g_m reduction that comes with these techniques was used as an advantage for designing low-g_m OTAs used in OTA-C filters. A filter with an f_o = 0.16 Hz using an OTA with a g_m = 10 nA/V, HD_3 = – 45 dB, and 8.2 μW of power consumption with V_{DD} = 2.7 V.

In [17], two LV OTAs are presented. The first topology is a PMOS input BD-OTA and the second an NMOS input GD-OTA with BB. The latter requires a triple-well process. In addition,

the GD-OTA with BB was used to construct a 5th order elliptic low-pass filter (LPF). The filter had a bandwidth (BW) of 135 kHz and consumed a total of 2.2 mA with V_{DD} = 0.5 V.

A FG-based LV CMOS OTA was used in a g_m-C band-pass filter (BPF) in [49]. The BPF achieves a center frequency that can be tuned between 6 MHz and 15 MHz with a V_{DD} = 1.4 V.

Techniques such as BB, BD, and FG are usually used to design voltage-mode OTAs. Current-mode approaches to OTA design, such as those presented in [69, 70], could also be used in combination with BB, BD, and FG to implement LV high-frequency filters.

A ring oscillator (RO) based filter is presented in [60], where a 4th-order Butterworth LPF was implemented. The filter achieved a BW = 7 MHz and THD = 60 dB while consuming 5.27 mA with V_{DD} = 0.55 V.

The solution proposed in [62] uses SMOAs. Each SMOA uses eight phases that push f_M eight times higher in frequency. However, eight modulators and eight modulation signals that are phase shifted by 2π/N, where N is the number of phases, are required. A 300 MHz clock is moved to a 2.4 GHz tone at high frequency that was later filtered with a 2-tap FIR filter to improve distortion. The complexity of the 8-stage phase modulator and FIR filtering, the 2π/N modulation phase shift generation and routing of those signals adds a trade-off between circuit performance, area, and system complexity to the implementation. For this architecture if a reduction in complexity is desired, then less phases could be implemented at the cost of increasing the filter constraints or decreased attenuation at f_M.

4.6 Low-voltage Filters Architecture Comparison

This section will describe and compare the different techniques presented in this chapter for the implementation of a first-order LPF, shown in Fig. 52, with a BW = 1 MHz and V_{DD} = 0.6

V in CMOS 130 nm. For comparison purposes, all OTAs using analog techniques (GD, BD, BB, and FG) are implemented as two-stage Miller OTAs with a PMOS input differential pair. In addition, all transistors will target a $V_{dsat} \leq 100$ mV and the same open-loop UGF ≈ 10 MHz, while driving a 1.6 pF output capacitor.

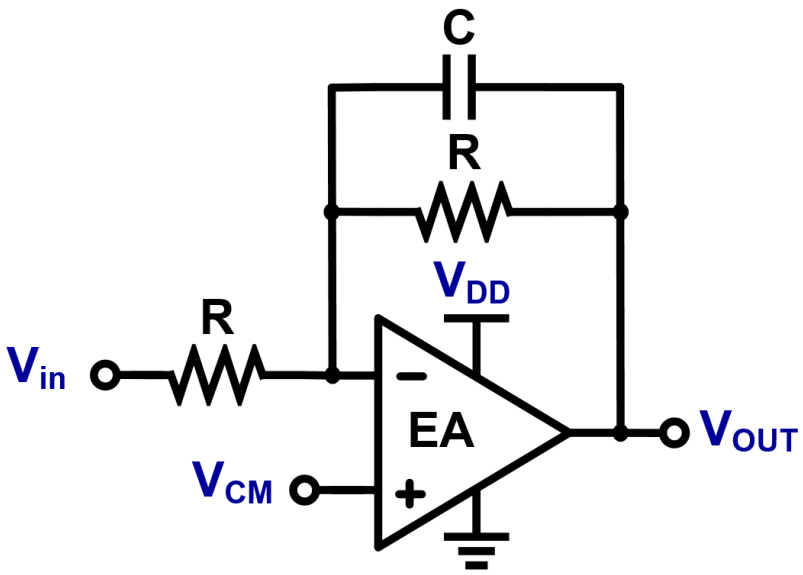


Fig. 52: First order LPF used for architecture comparison. R = 100 kΩ, C = 1.6 pF, V_{DD} = 0.6 V, and V_{CM} = 0.3 V.

4.6.1 Gate-Driven OTA based LV Filter

The two-stage Miller OTA designed using a GD approach is shown in Fig. 53. Due to the LV constraints all transistor's V_{dsat} are equal or lower than 100 mV. All design values, transistor sizes, voltages, and currents are given in Table 8.

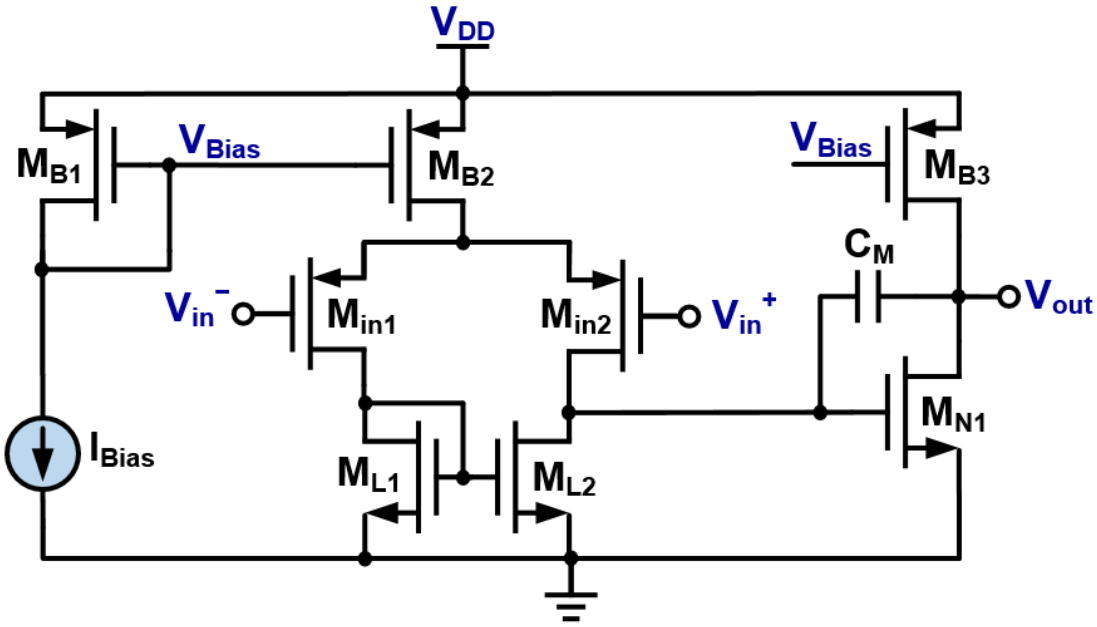


Fig. 53: Two-stage Miller OTA with Gate-Driven PMOS input pair

Table 8: Two-stage Miller OTA with Gate-Driven PMOS input pair design parameters

Parameters	Value	Transistor	Fingers	W/L
I_{Bias}	4 µA	M_{B1}	4	4 µm / 1 µm
V_{DD}	0.6 V	M_{B2}	4	4 µm / 1 µm
V_{CM}	0.3 V	M_{B3}	12	4 µm / 1 µm
C_M	450 fF	M_{in1}/M_{in2}	2	2.2 µm / 0.6 µm
		M_{L1}/M_{L2}	2	0.68 µm / 0.9 µm
		M_{N1}	8	0.95 µm / 0.9 µm

4.6.2 Bulk-Driven OTA based LV Filter

The two-stage Miller OTA designed using a BD approach is shown in Fig. 54. Due to the LV constraints all transistor's V_{dsat} are equal or lower than 100 mV. All design values, transistor sizes, voltages, and currents are given in Table 9.

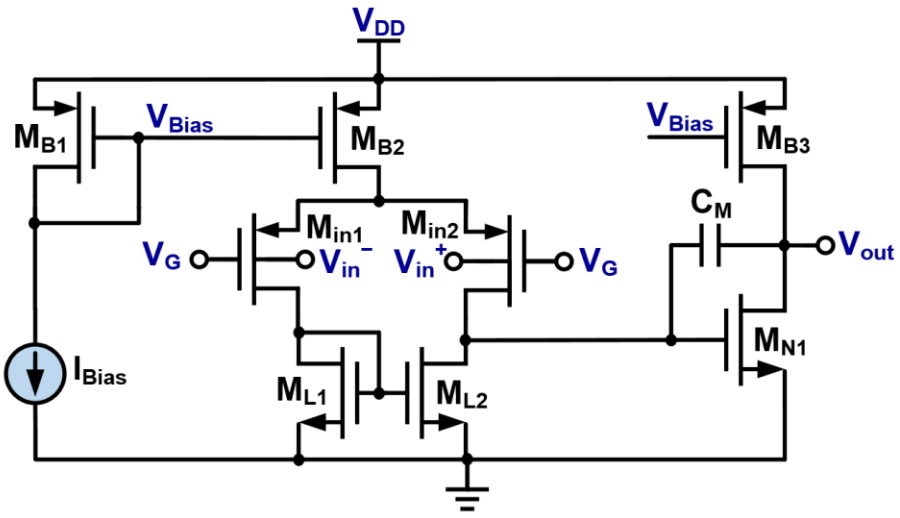


Fig. 54: Two-stage Miller OTA with Bulk-Driven PMOS transistors

Table 9: Two-stage Miller OTA with Bulk-Driven PMOS input pair design parameters

Parameters	Value	Transistor	Fingers	W/L
I_{Bias}	4 µA	M_{B1}	4	4 µm / 1 µm
V_{DD}	0.6 V	M_{B2}	4	4 µm / 1 µm
V_{CM}	0.3 V	M_{B3}	12	4 µm / 1 µm
V_G	0.2 V	M_{in1}/M_{in2}	2	2.2 µm / 0.36 µm
C_M	60 fF	M_{L1}/M_{L2}	2	0.68 µm / 0.9 µm
		M_{N1}	8	0.86 µm / 0.9 µm

4.6.3 Bulk-Bias OTA based LV Filter

The two-stage Miller OTA designed using a BB approach is shown in Fig. 55. Due to the LV constraints all transistor's V_{dsat} are equal or lower than 100 mV. In this design, all PMOS transistors are using BB. In addition to the advantages explained previously, see subsection 2.2, to using BB in the input differential pair, having BB applied to the current mirrors slightly decreases their size compared to the case with no BB. This happens because BB decreases their V_T so their

size needs to decrease to keep the same V_{dsat} for the same current. All design values, transistor sizes, voltages, and currents are given in Table 10.

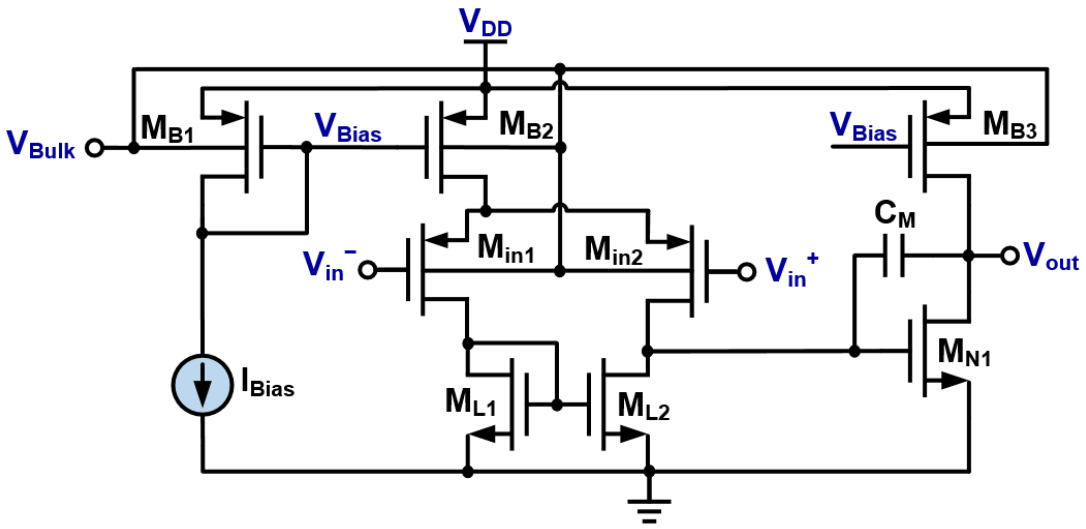


Fig. 55: Two-stage Miller OTA with Bulk-Bias PMOS transistors

Table 10: Two-stage Miller OTA with Bulk-Bias PMOS input pair design parameters

Parameters	Value	Transistor	Fingers	W/L
I_{Bias}	4 µA	M_{B1}	4	3.7 µm / 1 µm
V_{DD}	0.6 V	M_{B2}	4	3.7 µm / 1 µm
V_{CM}	0.3 V	M_{B3}	12	3.7 µm / 1 µm
V_{Bulk}	0.3 V	M_{in1}/M_{in2}	2	2.2 µm / 0.6 µm
C_M	450 fF	M_{L1}/M_{L2}	2	0.68 µm / 0.9 µm
		M_{N1}	8	0.8 µm / 0.9 µm

4.6.4 Floating-Gate OTA based LV Filter

The two-stage Miller OTA designed using a FG approach is shown in Fig. 56. Due to the LV constraints all transistor's V_{dsat} are equal or lower than 100 mV. The technology available for this implementation does not have FG devices, for that reason a simulation approach to emulate FG was used. Capacitors, C_{in} and C_{Bias}, were manually added in parallel with very large resistors to allow dc convergence without having an impact in transient performance. All design values, transistor sizes, voltages, and currents are given in Table 11.

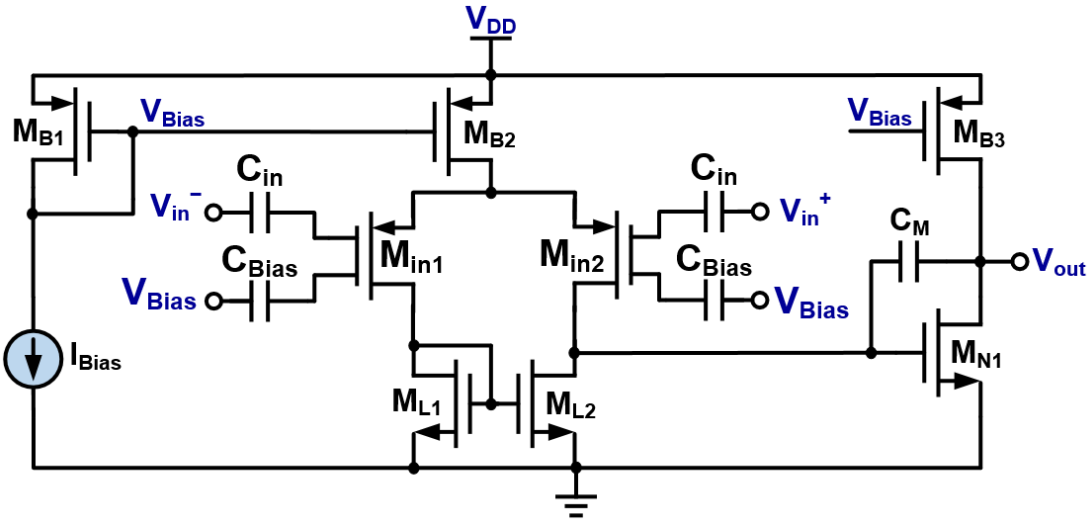


Fig. 56: Two-stage Miller OTA with Floating-Gate PMOS transistors

Table 11: Two-stage Miller OTA with Floating-Gate PMOS input pair design parameters

Parameters	Value	Transistor	Fingers	W/L
I_{Bias}	4 µA	M_{B1}	4	4 µm / 1 µm
V_{DD}	0.6 V	M_{B2}	4	4 µm / 1 µm
V_{CM}	0.3 V	M_{B3}	12	4 µm / 1 µm
V_{Bias}	50 mV	M_{in1}/M_{in2}	2	2.2 µm / 0.6 µm
C_M	230 fF	M_{L1}/M_{L2}	2	0.68 µm / 0.9 µm
C_{in}/C_{Bias}	2 pF	M_{N1}	8	0.86 µm / 0.9 µm

4.6.5 VCO-based LV Filter

The transistor-level VCO-based OTA is shown in Fig. 57. The architecture is similar to the one shown previously in Fig. 46, except with additional blocks to make the OTA functional. The additional stages include a level shifter and a dc bias circuit at the output voltage (V_{OUT}). The level shifter is required because the JK flip-flop operates at V_{DD} = 0.6 V, whereas the output of the RO varies with the input voltage (V_{in}). Therefore, it converts the RO's output voltage to a V_{DD} to GND switching signal. The reference clock is generated via a replica RO circuit with a common-mode voltage (V_{CM}) as the input. This is to allow both oscillators to track each other across PVT. The dc bias circuit and LPF create the dc operating point at V_{OUT} and filter the ripples coming from the CP, respectively. C_{LPF} should be properly sized to achieve a desired attenuation at the VCO's oscillation frequency. In addition, the LPF also creates the VCO-based OTA's dominant pole. Previous OTA structures usually are UGF limited by the additional poles in the system. In comparison, the VCO-based OTA UGF can be significantly higher due to the parasitic pole's location being at high frequencies for a given power. All design values, transistor sizes, and voltages are given in Table 12.

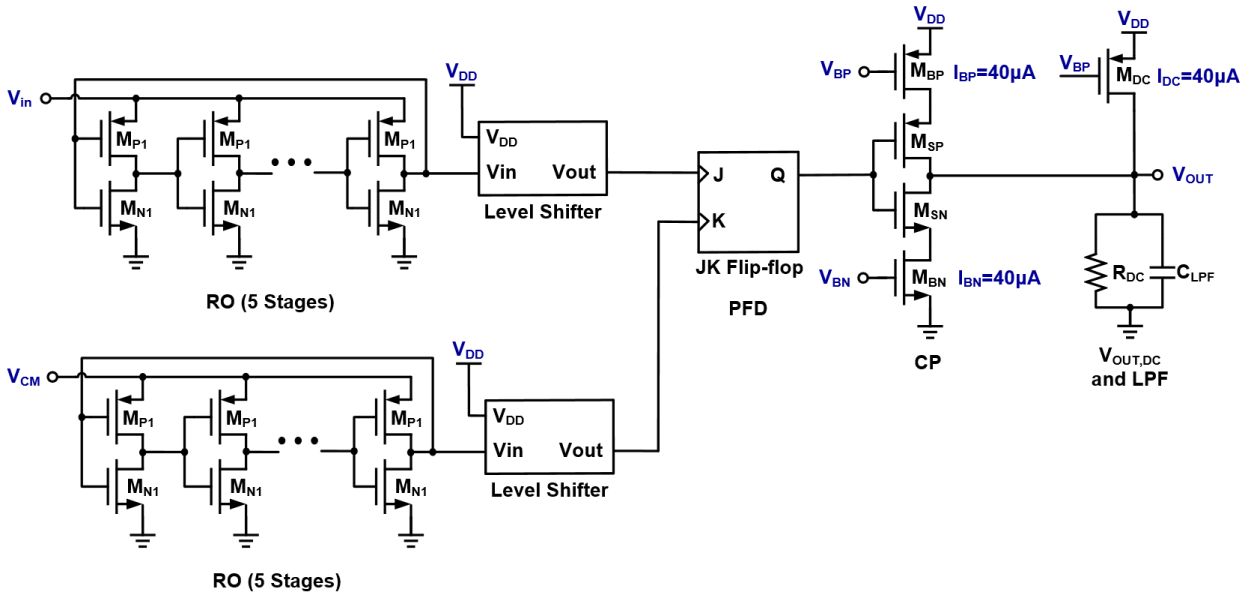


Fig. 57: VCO-based OTA

Table 12: VCO-based OTA design parameters

Parameters	Value	Transistor	Fingers	W/L
V_{DD}	0.6 V	M_{P1}	2	2.5 µm / 0.12 µm
V_{CM}	0.3 V	M_{N1}	2	1.65 µm / 0.12 µm
REF_{CLK}	81 MHz	M_{BP}/M_{DC}	16	7 µm / 0.8 µm
R_{DC}	7.5 kΩ	M_{SN}/M_{SP}	4	2 µm / 0.2 µm
C_{LPF}	200 pF	M_{BN}	16	1.5 µm / 0.8 µm

4.6.6 Switched-mode OpAmp based LV Filter

The transistor-level SMOA is shown in Fig. 58. Due to the LV constraints all transistor's V_{dsat} are equal or lower than 100 mV. In addition, all PMOS transistors use the BB technique to allow for better performance at such LV operation. The SMOA consists of three sections, a LV OTA linear stage, a comparator, and a passive LPF, not shown in Fig. 58. Transistors M_{in1}, M_{in2},

M_{L1}, M_{L2}, and M_{B2} form the LV OTA section, which is the same as the one used in the BB OTA presented in subsection 6.3. The comparator is formed by transistors M_{N1}, M_{N2}, and M_{L3}-M_{L6}, which is based in the architecture presented in [71], and a NOT gate to buffer the comparator's output voltage to allow rail-to-rail operation. V_{sw} is a triangle waveform, which in combination with the comparator form the PWM operation. V_{sw} has a 200 mV peak-to-peak voltage swing from 200 mV to 400 mV at a 100 MHz. The LPF sets the dominant pole and filters the PWM carrier frequency so that the analog signal can be recovered. An additional zero is added through resistor R_Z to increase the phase around UGF. All design values, transistor sizes, voltages, and currents are given in Table 13.

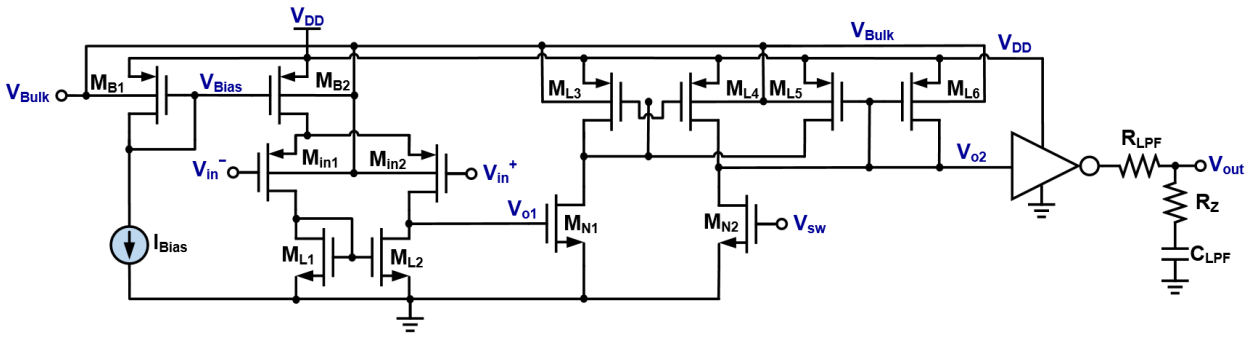


Fig. 58: SMOA with bulk-biased PMOS transistors

Table 13: SMOA with bulk-biased PMOS input pair design parameters

Parameters	Value	Transistor	Fingers	W/L
I_{Bias}	4 µA	M_{B1}	4	3.7 µm / 1 µm
V_{DD}	0.6 V	M_{B2}	32	3.7 µm / 1 µm
V_{CM}	0.3 V	M_{in1}/M_{in2}	8	4.4 µm / 0.6 µm
V_{Bulk}	0.3 V	M_{L1}/M_{L2}	2	2.36 µm / 1 µm
R_{LPF}	10 kΩ	M_{N1}/M_{N2}	4	6 µm / 0.4 µm
C_{LPF}	70 pF	M_{L3}/M_{L6}	8	5.2 µm / 0.26 µm
R_Z	75.8 Ω	M_{L4}/M_{L5}	8	4.8 µm / 0.26 µm
NOT gate		M_P	34	2.5 µm / 0.12 µm
		M_N	34	1 µm / 0.12 µm

4.6.7 Architecture Comparison

The five different LV OTA architectures are compared in Table 14. As expected, the two architectures that achieve rail-to-rail ICMR are the FG-OTA and BD-OTA. The VCO-based OTA has a higher UGF compared to other analog-based architectures because it does not require additional power to achieve such UGF. Also, since the VCO-based OTA has its non-dominant poles at higher frequencies compared to other OTA implementations a higher UGF can be achieved without a phase margin (PM) penalty.

Table 14: Performance Comparison for different LV OTA implementations

Parameters	GD-OTA	BD-OTA	BB-OTA	FG-OTA	VCO-based OTA	SMOA
V_{DD} (V)	0.6	0.6	0.6	0.6	0.6	0.6
Technology (nm)	130	130	130	130	130	130
dc gain (dB)	51.29	34.99	51.61	44.23	∞	32.53
Bandwidth (kHz)	30.52	219.8	31.49	67.79	0	227.36
UGF (MHz)	10	10.56	10.79	9.98	51.47	10
PM (°)	55.79	56.03	54.05	58.87	-	70
$V_{CM,max}$ (mV)	325	600	367	600	600	367
$V_{CM,min}$ (mV)	18	0	64	0	260	64
ICMR (mV)	307	600	303	600	340	303
Power (µW)	12.12	12.36	12.66	12.34	76.34	490.5

The five OTAs were used in a first-order filter implementation as shown in Fig. 52. All of them used the same resistor values, with the exception of the VCO-based OTA, which used R = 10 kΩ and C = 16 pF. The reason for this change was due to the fact that the VCO-based OTA is a current input device compared to a high-impedance input gate in all other OTA architectures. A lower resistor value in the integrator decreases the offset due to the input current going to the CCO. The capacitor was multiplied by 10x to keep the same integrator's RC time constant.

Fig. 59 and Fig. 60 show the total-harmonic distortion (THD) and spurious-free dynamic range (SFDR), respectively, for the different LV LPFs implemented with the different OTAs using the previously discussed LV techniques. As expected the VCO-based and SMOA OTAs show the worst THD and SFDR performance. The degradation in SFDR comes from the fact that their clocks are not attenuated enough with the passive LPF. More complicated LPF techniques may improve the SFDR performance up to certain extent. The VCO-based THD improves as the signal increases, usually the opposite is true in conventional analog OTAs, due to the inherent non-linearity of the system present even at low input signals.

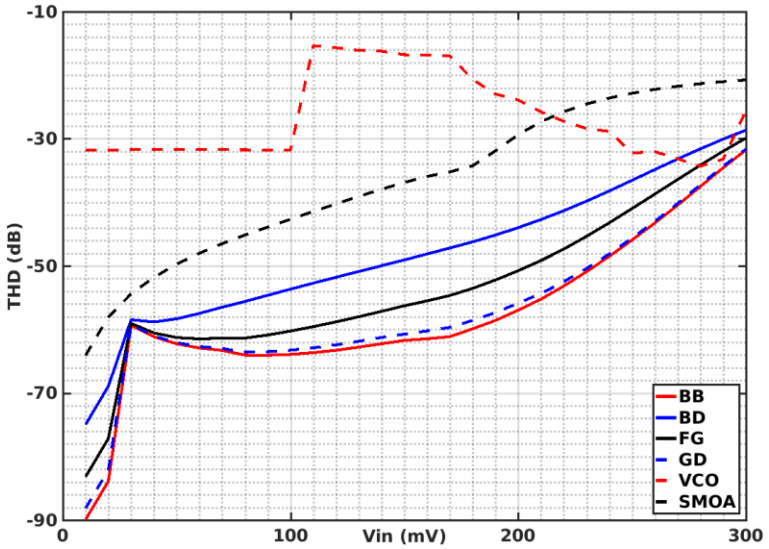


Fig. 59: THD for the first-order LPF using a bulk-bias (BB), bulk-driven (BD), floating-gate (FG), gate-driven (GD), VCO-based, and SMOA OTAs, respectively. V_{DD} = 0.6 V, V_{CM} = 0.3 V.

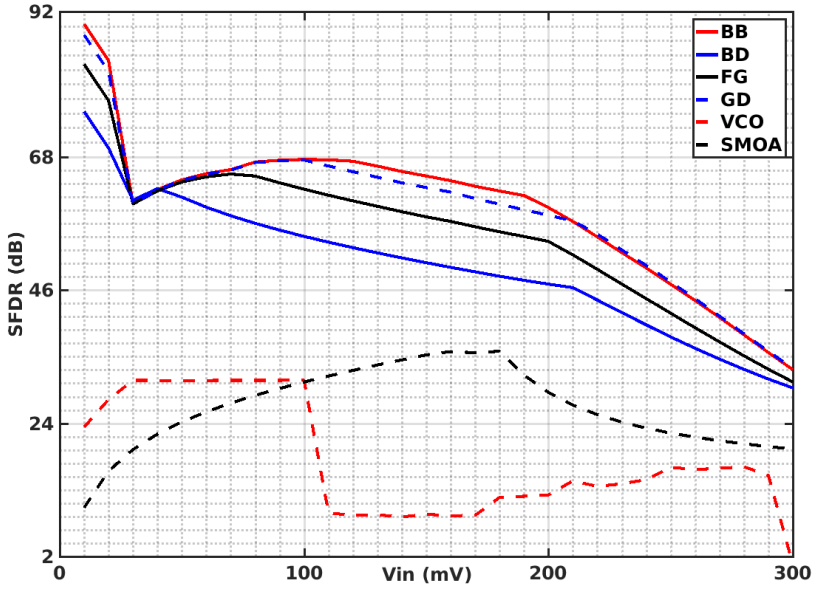


Fig. 60: SFDR for the first-order LPF using a bulk-bias (BB), bulk-driven (BD), floating-gate (FG), gate-driven (GD), VCO-based, and SMOA OTAs, respectively. V_{DD} = 0.6 V, V_{CM} = 0.3 V.

Table 15 shows the comparison results for the different LV LPFs implemented with the different OTAs using the previously discussed LV techniques. In general, the continuous time analog OTAs have better performance in terms of SFDR and THD compared to the time-domain OTAs. However, when it comes to noise, the VCO-based and SMOA OTAs have better performance, i.e. lower noise, due to the discrete nature of their operation. This improvement comes at the price of higher power consumption.

Table 15: Performance Comparison for different LV LPF implementations

Parameters	GD-OTA	BD-OTA	BB-OTA	FG-OTA	VCO-based OTA	SMOA
V_{DD} (V)	0.6	0.6	0.6	0.6	0.6	0.6
Technology (nm)	130	130	130	130	130	130
Power (μW)	12.12	12.36	12.66	12.34	76.34	490.5
Intg. Noise (μV_{RMS})	109.9	540.3	109.7	204.6	30.84	61.73
THD (dB)	−55.86	−43.98	−56.97	−50.76	−23.90	−29.36
SNR (dB)	65.71	51.88	65.73	60.31	76.75	70.72
SFDR (dB)	58.35	46.98	59.62	54.03	12.16	29.10

4.7 Conclusion

As V_{DD} decreases, novel techniques are required to continue designing analog filters required in current system-on-chip (SoC) circuits. The more relevant techniques to design LV OTAs are discussed in this chapter, along with the basic theory required for their implementation. The techniques discussed in this chapter were BB, BD, FG, VCO-based, and SMOAs. Some of these techniques can be used in combination with each other to further improve the performance and lower the minimum V_{DD} required for operation.

From the linearity point of view, the best performance is achieved with BB and GD architectures. This can be attributed to the fact that these architectures achieve the highest gain for a given power. In closed-loop systems, a high gain is proportional to good linearity.

The architecture that can achieve the minimum V_{DD} is the VCO-based OTA. This is because the VCO-based OTA is the only architecture that fully operates transistors in their linear region. This avoids having to have saturation voltages that decrease voltage headroom as their analog counterparts.

SMOAs suffer from very high power consumption. This architecture uses the highest amount of power consumption for a given BW. Power sensitive applications should use this architecture.

The only rail-to-tail architectures are BD and FG OTAs. The additional degree of freedom achieved with a PMOS bulk terminal or a FG device increases drastically the ICMR. The price to pay is a lower gain and therefore poor linearity compared to GD and BB architectures. If rail-to-rail is a must, then more power in the form of additional gain stages can improve the performance of BD and FG OTAs.

Further research in designing high-frequency, LV, and low-power filters is always going to be required for the ever increasing complexity in SoC circuits.

CHAPTER V

HIGH-BW POWER-ADJUSTABLE LOW-VOLTAGE ACTIVE-RC 4TH-ORDER LPF

5.1 Introduction

As technology scales down and supply voltage (V_{DD}) decreases, analog circuits tend to decrease their performance. Low voltage (LV) supplies in modern applications are usually less than 1 V. Designing operational amplifiers (OpAmps) or operational transconductance amplifiers (OTAs) in LV become complex without using costly techniques such as bulk-driven (BD) [17-20], bulk-bias (BB) [17, 21], or floating gate (FG) [47-49], which may require triple-well devices or additional fabrication steps. Achieving high loop gain decreases errors in closed-loop systems, and therefore, high dc gain is a desirable characteristic in OTAs.

To maintain the same dc gain, as high voltage circuits, new OTA architectures are required because LV operation prohibits the use of traditional high gain techniques such as cascoding. This has attracted interest in LV OTAs that can keep the same performance as their previous high voltage counterparts. Cascading multiple gain stages can be used to achieve the desired gain without using cascode structures.

Previously proposed advanced cascade structures offer several advantages and disadvantages, as thoroughly discussed in [72]. These cascade structures can be combined with LV techniques, like BD, BB, or FG, to create high-gain LV OTAs currently required for state-of-the-art LV systems. However, these LV techniques may reduce circuit performance, and require additional biasing circuits and/or fabrication steps. For those reasons, an LV OTA structure that still works under LV conditions but without employing previously mentioned LV techniques, or

without sacrificing performance, remains of great importance for the current trends in analog circuit design.

5.1.1 Low-Voltage Filter's Literature Review

Conventional LV filters in the literature [17, 60, 73, 74] usually target low cut-off frequencies (f_o), less than 20 MHz, applications, and so far only one targets high f_o [62], more than 20 MHz, which is the required f_o for applications like IEEE 802.11ac or others where high f_o are required.

In [17], two LV OTAs are presented. The first topology is a PMOS input bulk-driven OTA and the second an NMOS input gate-driven OTA with bulk bias. The latter requires a triple-well process. In addition, the gate-driven OTA was used to construct a 5^{th} order elliptic low-pass filter (LPF). The filter had a f_o = 135 kHz and consumed a total of 2.2 mA with V_{DD} = 0.5 V. However, the filter's f_o is too low for recent communication standards.

In [73], a low voltage OTA using the cross-forward common-mode (CM) cancellation, which provides cancellation of CM signals, and linear sub-threshold R-MOSFET resistor for frequency tuning were used to implement a 5^{th} order elliptic LPF. The filter had a f_o = 135 kHz and consumed a total of 1.2 mA with V_{DD} = 0.5 V. This filter decreased its power consumption compared to [17] but still lacks the required f_o for recent communication standards.

In [74], a low voltage active-Gm-RC topology is used to implement a 4th-order Butterworth filter that targeted a high linearity zero-IF receiver application. The filter had a f_o = 12 MHz and consumed a total of 6.18 mA with V_{DD} = 0.55 V. This filter's f_o is significantly higher than the previous ones and can be possibly used in the lower frequencies for the current LTE

standard, if frequency tuning or selection is added. However, it falls short for the required f_os for some current [75] and future communication standards [76].

Another approach to address the significant drawbacks of low voltage operation in analog design is doing the processing in the time domain. A ring oscillator (RO) based filter is presented in [60], where a 4th-order Butterworth filter was implemented. The filter achieved a f_o = 7 MHz and a total harmonic distortion (THD) of 60 dB while consuming 5.27 mA with V_{DD} = 0.55 V. The RO-based architecture is voltage scalable and its digital-cell based implementation makes it a good candidate for further technology scaling. However, multiple clock phases and high oversampling ratios, compared to the filter's BW, are required. This RO time domain implementation achieves the required dc gain but adds significant complexity and power due to the multiple clock phase generation and clock frequency required to achieve high f_os.

A nonlinear output stage using an analog based pulse-width modulation (PWM) generator, to convert the voltage information into the time domain, was recently explored in [62] to design a LV filter. A continuous-time (CT) 4th-order Butterworth LPF using CMOS 65 nm was presented. Eight multi phases increased the PWM carrier frequency (f_M) from 300 MHz to 2.4 GHz, and a 2-tap CT Finite Impulse Response (FIR) filter was used to remove the strong components at f_M. The filter achieved a f_o = 70 MHz and a THD = 60 dB while consuming 43.67 mA with V_{DD} = 0.6 V. Both time domain designs consume significant power for the designed filter's f_o and measurement results showed that tones at the switching frequency appear due to imperfect cancellation of the clock phases [60].

This chapter presents an enhanced LV fully-differential (FD) OTA with feedforward gain-boosting, an adjustable output stage, unity-gain frequency (UGF), and power consumption. The proposed LV OTA achieves a constant dc gain of 66 dB, an adjustable UGF of 330 MHz, 545

MHz, 666 MHz, and 759 MHz while using V_{DD} = 0.6 V, and consumes 1.48 mW, 2.36 mW, 3.48 mW, and 5.27 mW of power dissipation, respectively. The proposed OTA was used to implement a LV 4th-order active-RC Butterworth LPF capable of a f_o up to 160 MHz, with a THD of 63.2 dB, a signal-to-noise and distortion ratio (SNDR) of 54.63 dB, a 1 dB compression point (P_{1dB}) of +7 dBm, and 520 μV_{RMS} integrated noise over the filter's bandwidth (BW), while consuming 23.77 mA from V_{DD} = 0.6 V.

LV OTA designs with smaller technologies also benefit from the proposed LV OTA transistor-level architecture. Due to transistors' intrinsic gain decreasing as channel-lengths are reduced, high-gain OTA architectures without using cascodes are desirable. If the desired gain is still not achieved due to the transistors' intrinsic gain decrease, cascading two of the proposed OTAs, at the expense of UGF, may be a possible solution to explore.

Additionally, the advantages of higher speed at lower nodes, along with the proposed LV OTA may enable active-RC filter implementations with BWs higher than the ones presented here.

The chapter is organized as follows. Subsection 2 presents the proposed LV OTA and LV filter. Subsection 3 discusses circuit implementation. Measurement results are shown in subsection 4, and finally conclusions are given in subsection 5.

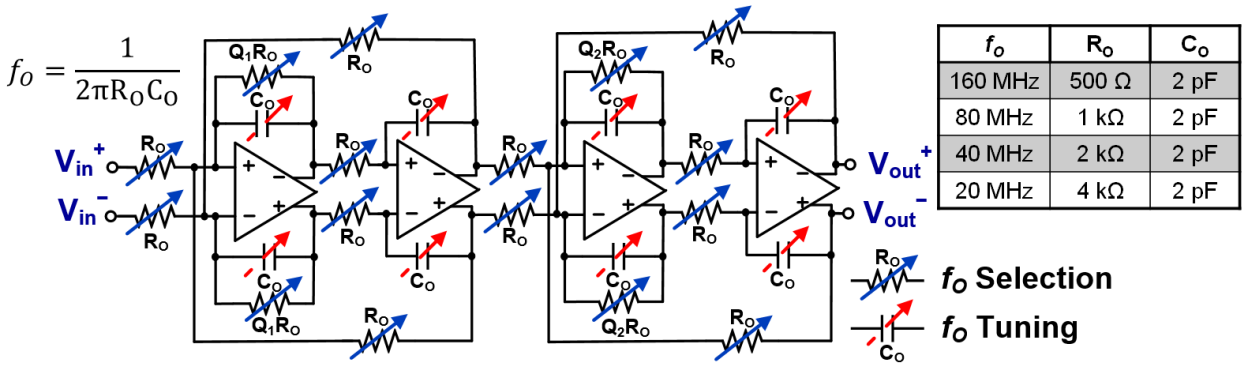
5.2 Proposed Low-Voltage Structures

5.2.1 Proposed LV Active-RC Filter

State-of-the-art LV filters in the literature [17, 60, 73, 74] usually target low-f_o applications, i.e., less than 20 MHz. Higher f_o is achieved at a high power consumption and complexity [62]. In addition, these filters have fixed f_o, whereas current [75, 77] and future [76] communication standards require both high and configurable f_o. These characteristics, if achieved with one filter,

would also save power and area. Although a sub-1V Gm-C open loop filter achieved high f_o [51], closed-loop filter architectures are often preferred because they offer better linearity over open-loop ones [62, 74]. To achieve these specifications, the filter requires, at the system level, a configurable f_o and, at the transistor level, a LV OTA architecture with high gain, high UGF, and power that can be properly adjusted such that both the power and UGF are decreased when required to keep power efficiency high. The proposed LV OTA meets all of these criteria, which are not unique to filters, and is used as the active component inside a prototype active-RC filter to prove the LV OTA's versatility. Although, the proposed LV OTA is used to implement a filter with specific f_o requirements, its implementation and design can be used, by those skilled in circuit design, to particularly tailor it to specific frequencies other than the ones shown here for demonstration purposes.

The filter is implemented with two active-RC Tow-Thomas biquads in cascade as shown in Fig. 61, where the component values for the f_o-selection resistor (R_O) and f_o-selection capacitor (C_O) for each f_o step are given inside the table located in the upper right side corner of Fig. 61. The filter's transfer function for a 4th-order Butterworth response was used, and the coefficients were taken from [22].



f_o	R_O	C_O
160 MHz	500 Ω	2 pF
80 MHz	1 kΩ	2 pF
40 MHz	2 kΩ	2 pF
20 MHz	4 kΩ	2 pF

Fig. 61: FD LV 4th-order Butterworth filter implementation

The Tow-Thomas biquad architecture was preferred over other biquad implementations as it offers independent control between the filter's Q and f_o. The filter's f_o is programmable from 20/40/80/160 MHz, where R_O is implemented as a resistor bank, whose values are 4/2/1/0.5 kΩ at each step, and is controlled digitally to select the proper filter's f_o. The resistors that determine the filter's Q, Q_1R_O and Q_2R_O, are also scaled properly with R_O to keep the Q constant. The same control signal adjusts the OTA's power and output impedance to drive the different resistors at each f_o step. Each capacitor, C_O, is implemented as a 4-bit binary weighted capacitor bank used to fine-tune the filter's f_o and compensate for process variations after fabrication. On-chip tuning techniques for filter's RC time constants can be found elsewhere [17, 73, 78, 79]. The filter's capacitor, C_O, has a nominal value of 2 pF and can be increased/decreased in 100 fF steps to fine-tune the filter's f_o. The biquads were ordered such that the first biquad has a Q_1 of 0.54 and the second a Q_2 of 1.3 to maximize the dynamic range (DR) [22].

Each biquad uses two OTAs to form a second order filter. These OTAs add non-idealities to the filter's transfer function due to their limited dc gain, finite gain-bandwidth product (GBW), intrinsic noise and nonlinear components due to transistors. The OTA's finite GBW would cause

Q-enhancement [80] in the filter thereby changing the filter's magnitude response as discussed in [80]. The filter's effective Q, Q_{Eff}, is given by:

$$Q_{Eff} = \frac{Q_d}{1+\frac{2Q_d}{A_0 f_{3dB}}\left(f_{3dB}-2f_o\right)} \approx \left.\frac{Q_d}{1-\frac{4Q_d f_o}{GBW}}\right|_{\substack{A_0>>1 \\ 2f_o>>f_{3dB}}} \tag{111}$$

where Q_d, A_0, and f_{3dB} are the filter's designed Q, OTA's dc gain and 3 dB BW, respectively.

Fig. 62 shows a plot of (111), where Q-enhancement in percentage is shown for different f_o/GBW ratios and Qs. It can be observed from (111), that small f_o/GBW ratios are desired if Q_{Eff} is to be kept within a small percentage deviation from Q_d, and that the higher the Q_d, the smaller the f_o/GBW ratio is required. However, for high f_o filters the f_o/GBW ratio is limited by power consumption, and ultimately, the technology's speed limit. Techniques to mitigate these effects, at the system level, such as passive and active compensation are discussed in [22, 80-82], where [82] discusses the advantages and disadvantages of each approach. To keep power consumption low, passive Q-enhancement compensation was used in this work to counterbalance the OTA's finite GBW, which was the same approach used by [82]. In passive compensation, each biquad's Q_d was intentionally implemented with a lower value to compensate for Q-enhancement introduced by finite GBW limitations. The starting point for the Q values, for the first and second biquad, were determined by using (111) along with the simulated OTA's f_o/GBW. Simulations were performed to verify the final values and make the necessary adjustments.

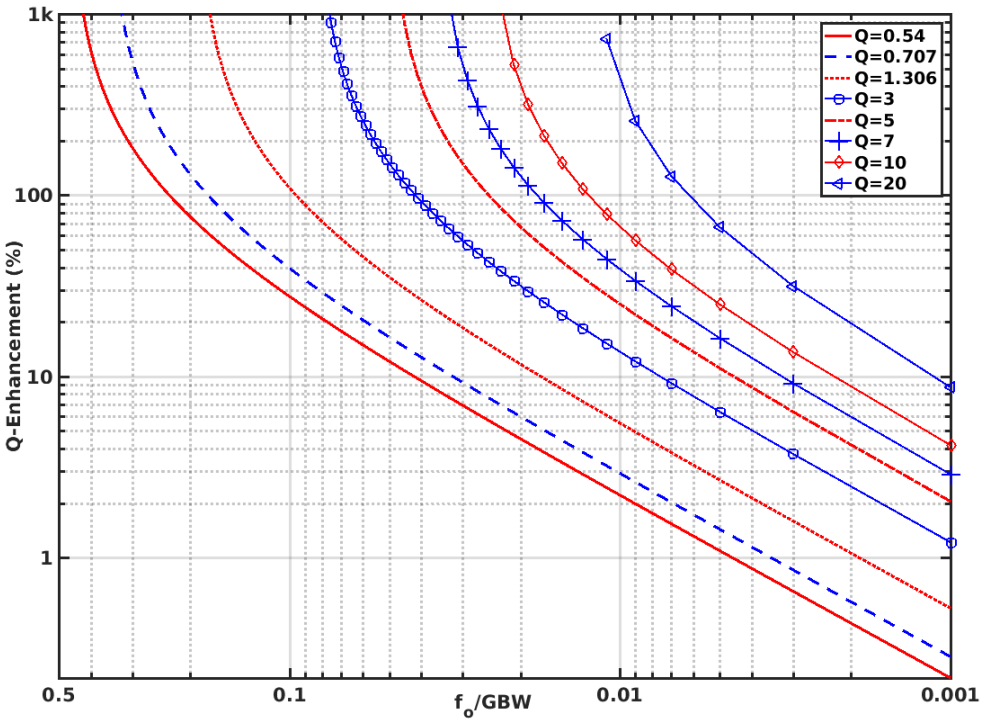


Fig. 62: Q-Enhancement (%) as a function of f_o/GBW ratio for different Qs

One of the advantages of changing the filter's f_o via a resistor bank is that the filter's tuning range after fabrication, determined by the capacitor bank, is constant independently of the filter's f_o. Another advantage is that resistors occupy less area compared to capacitors. The drawbacks are that resistor's matching is worse compared to capacitor's matching, and that low resistor values require an OTA with low output impedance. Matching was addressed by good layout techniques as explained in subsection 3.5. To achieve programmable low output impedance, the OTA was designed to have an output stage that is controlled by the filter's f_o control signals, as discussed in subsection 2.1. This programmable output stage saves power and improves performance, as explained further in subsection 3.2.

5.2.2 Filter's Low-Frequency Noise

The FD 4th-order Tow-Thomas biquad filter's low-frequency output noise spectral density is given by (112), where k, T, Q_1, Q_2, and $v^2_{n,in,OA}$ are the Boltzmann constant, temperature in degrees Kelvin, first biquad's Q, second biquad's Q, and OTA's input referred noise, respectively. The following assumptions were made: 1) All OTAs in Fig. 61 are the same, and 2) the filter's gain is 0 dB or 1 V/V. Details of the derivation can be found in the appendix B.

$$v^2_{n,out} = 2\left[\left(4+\frac{1}{Q_1}+\frac{1}{Q_2}+\frac{1}{Q_1^2}+\frac{1}{Q_2^2}\right)\left(4kTR_o + v^2_{n,in,OA}\right) + v^2_{n,in,OA}\left(\frac{1}{Q_1}+\frac{1}{Q_2}\right)\right] \qquad (112)$$

Following (112), the higher the Q, the better the low-frequency noise performance for this particular biquad implementation. However, a higher Q means more high-frequency noise being integrated around the filter's f_o. In general, and similar to other biquad implementations, the total integrated noise increases with Q. In addition, Q is a parameter determined by the system level requirements and the desired filter's response. Therefore, in order to decrease noise, low resistor values and low noise OTAs are required.

5.2.3 Proposed LV OTA

Cascode structures are not reliable due to the LV supply, V_{DD} = 0.6 V, used in this design. Cascading gain stages adds additional poles that may limit the maximum achievable OTA's UGF and phase margin (PM). It also increases power consumption, requires complicated compensation techniques, and reduces BW [72]. For that reason, the number of gain stages in cascade should be minimized.

The proposed LV FD OTA, whose small-signal model is shown in Fig. 63, consists of two gain stages, G_{MA} and G_{MB}, RC frequency compensation, implemented by R_{M1} and C_{M1}, and two local CM feedback (CMFB) loops. Fig. 63 shows the first stage's transconductance (G_{MA}) and output impedance (R_{OA}), second stage's transconductance (G_{MB}) and output impedance (R_{OB}), first CMFB loop's transconductance (G_{CM1}), first CMFB loop's CM sense capacitors (C_{CM1}) and resistors (R_{CM1}), second CMFB loop's transconductance (G_{CM2}), and second CMFB loop's CM sense capacitors (C_{CM2}) and resistors (R_{CM2}), and V_{CM} is the CM voltage.

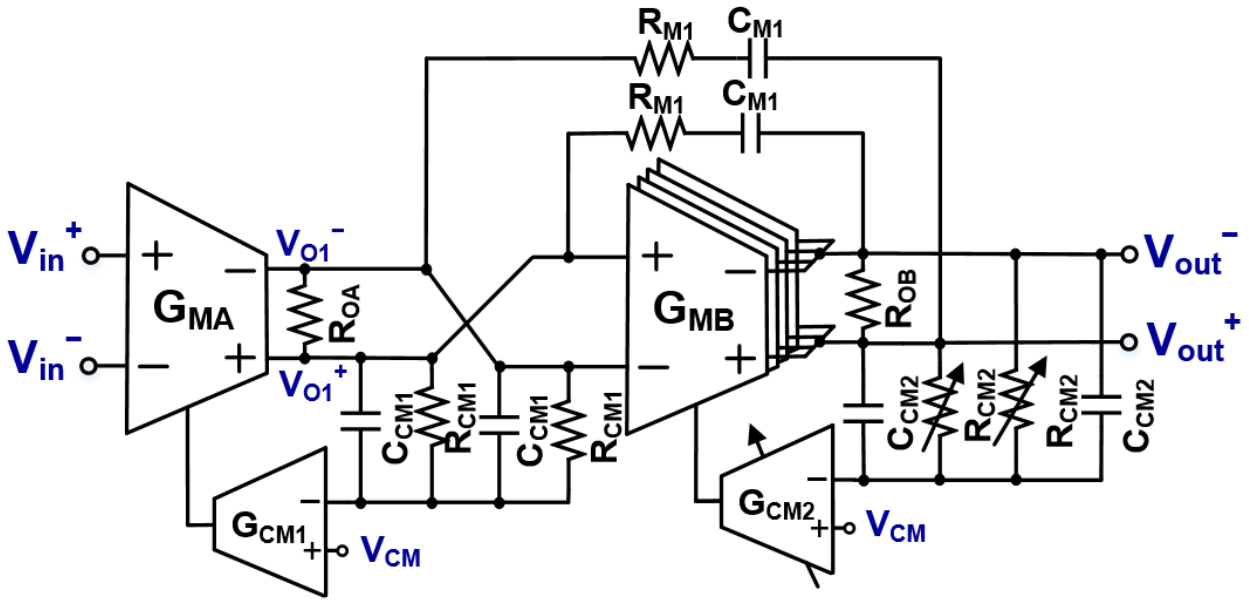


Fig. 63: Proposed LV OTA small-signal model

Only two gain stages were used to minimize power consumption and simplify the OTA's compensation complexity. This allowed the OTA's compensation, addressed in subsection 3.4, to use conventional Miller compensation. Both OTA gain stages contribute to gain; however, to

achieve a desired dc gain, higher than 60 dB at V_{DD} = 0.6 V, G_{MA} is implemented with an enhanced and compact LV gain-boosting transistor-level implementation, discussed in detail in subsection 3.1. The second stage, G_{MB} described further in subsection 3.2, is a programmable output stage that is configured to drive different low impedance resistive loads. These resistive loads determine the filter's f_o as explained in subsection 2.1. As sections of G_{MB} are turned ON/OFF, for different loads, the power consumption is kept low relative to the required filter's f_o. The next paragraphs describe this paper's proposed OTA individual stages (Fig. 63) in more detail.

The first stage, G_{MA}, is a high-gain FD OTA using feedforward gain-boosting and a local CMFB loop implemented through sense resistors (R_{CM1}) and a CMFB amplifier (G_{CM1}). The gain-boosted stage was designed such that it contributes to the majority of the gain. The FD high-gain OTA's small-signal representation is shown in Fig. 64, where the single-ended version is shown for illustration purposes. Additionally, g_{m1}, g_{m2}, and g_{m3} are the transconductances of the first, second, and third OTA, respectively. R_{o1}, R_{o2}, and R_{o3} are the output resistances seen by g_{m1}, g_{m2}, and g_{m3}, respectively. C_1 and C_2 are the capacitances seen by g_{m1} and g_{m2}, respectively.

The high-gain OTA used in the first stage, G_{MA} in Fig. 63, consists of two paths. The upper path formed by g_{m2} and g_{m3}, and lower path formed by g_{m1}. This creates a high-gain high-BW amplifier with a dc gain equivalent to a conventional two-stage amplifier but without the two low frequency poles, as previously reported in [83-85]. Therefore, the small-signal operation mode is different from those previously discussed, whose implementations require one or more compensation capacitors [72, 86, 87], or are focused on applications with high gain and low UGF [88].

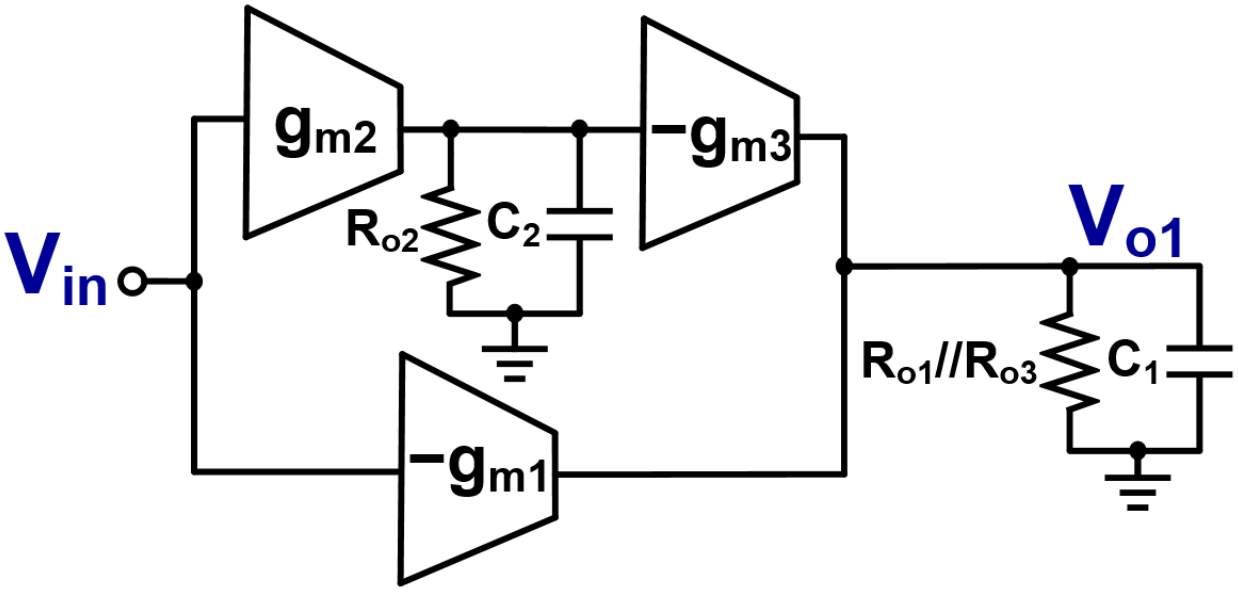


Fig. 64: G_{MA}'s single-ended small-signal representation

For the proposed design, the dominant pole is placed at G_{MA}'s output, instead of one of its internal nodes, by the Miller compensation capacitor around G_{MB}. Subsection 3.4 discusses stability and compensation, and subsection 3.1 presents an enhanced LV transistor-level architecture that implements G_{MA}'s transfer function by reusing the active load of a single differential pair as an additional gain stage.

G_{MA}'s small-signal transfer function is given in (113), where $A_{0,GMA}$, $\omega_{z1,GMA}$, $\omega_{p1,GMA}$, and $\omega_{p2,GMA}$ are G_{MA}'s dc gain, zero, first and second pole, respectively. The effective transconductance has been increased by an additional g_{m1}, compared to a two-stage amplifier, thereby boosting the dc gain while only having one low-frequency pole. This implementation also introduces a pole and a zero that are located at higher frequencies compared to the dominant pole. The additional pole and zero track each other since they both depend on capacitance C_2 and are not designed to be

cancelled perfectly compared to other feedforward compensation approaches [83-85]. G_{MA}'s complete transistor-level implementation is discussed in subsection 3.1.

$$\left|\frac{V_{o1}}{V_{in}}\right| = \frac{A_{0,GMA}\left(1+\frac{s}{\omega_{z1,GMA}}\right)}{\left(1+\frac{s}{\omega_{p1,GMA}}\right)\left(1+\frac{s}{\omega_{p2,GMA}}\right)} = \frac{\left(g_{m1}+g_{m2}g_{m3}R_{o2}\right)\left(R_{o1}//R_{o3}\right)\left(1+\frac{sg_{m1}C_2}{g_{m2}g_{m3}}\right)}{\left[1+s\left(R_{o1}//R_{o3}\right)C_1\right]\left(1+sR_{o2}C_2\right)} \tag{113}$$

The second stage, G_{MB} in Fig. 63, is a programmable output stage with its own CMFB loop, formed by sense resistors, R_{CM2}, and a CMFB amplifier, G_{CM2}. G_{MB}'s simplified single-ended representation is shown in Fig. 65, where G_{MB1}, G_{MB2}, G_{MB3}, and G_{MB4} are the four different sections implemented by four class-A gain stages in parallel; M_{6a}, M_{6b}, M_{6c}, and M_{6d} are the NMOS gain devices; I_{7a}, I_{7b}, I_{7c}, and I_{7d} are the bias currents for M_{6a}, M_{6b}, M_{6c}, and M_{6d}, respectively. The output stage drives the filter's passives; therefore, it requires low output impedance and enough current to drive the filter's resistors and capacitors for large signal operation without distortion.

The system level implementation requires the filter to switch between four different resistor values, 4/2/1/0.5 kΩ, to adjust the filter's f_o between 20/40/80/160 MHz, respectively. Therefore, G_{MB}'s output impedance is modified accordingly to drive the different resistances while keeping good power efficiency, high UGF, and constant dc gain.

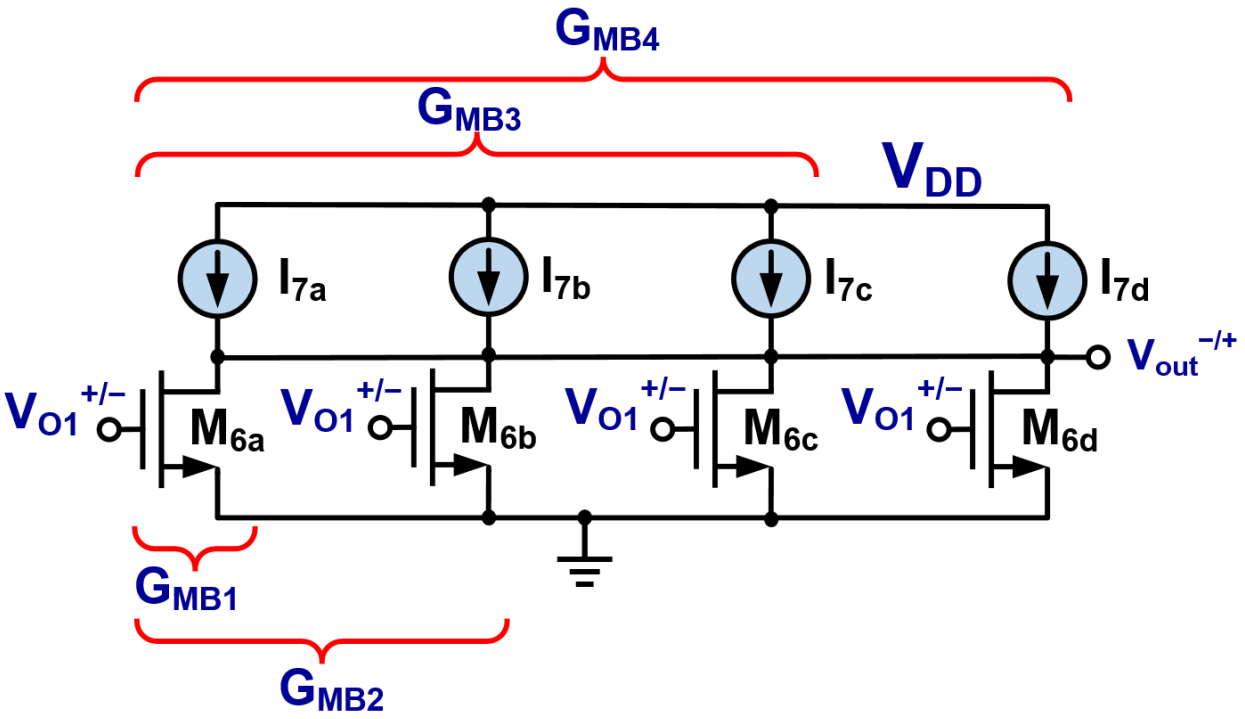


Fig. 65: G_{MB}'s simplified single-ended representation

G_{MB} is segmented in four different sections connected in parallel, which decreases the output impedance as they are turned ON. As the control signal changes the filter's f_o by decreasing (increasing) the resistance, G_{MB} also decreases (increases) its output impedance by turning ON (OFF) its segments, as explained in more detail in subsection 3.2. G_{MB} is controlled by the same digital signals that control the filter, which allows recycling of the control signals.

The noise is usually dominated by the first stage [42, 89]; therefore, in the proposed OTA only the second stage, G_{MB}, is adjusted to keep the OTA's input-referred noise constant throughout the different configurations.

The proposed LV FD OTA uses two CMFB loops. In FD implementations, the CMFB design represents a challenge in terms of stability and high frequency performance. The CMFB

loop usually consists of the main OTA gain stages, the CMFB sense circuit, and the CMFB amplifier. This means that the CMFB loop has at least two additional poles that would complicate its design and make stability even harder to maintain for high UGFs. Having only one CMFB, in this implementation, creates a system where three gain stages would need to be compensated.

Good stability for multi-stage amplifiers can be achieved with compensation techniques such as those discussed in [72, 86, 87]. However, these techniques usually require extra feedback capacitors and would limit the CMFB loop's BW. Low frequency applications are where these techniques find their best use. To achieve good PM and high UGF, two CMFB loops are proposed for this OTA instead of one. This comes at the price of additional power and area but relaxes the CMFB loop's design complexity. By splitting the CMFB, only two high gain stages are seen by each CMFB loop, which can be stabilized more easily and with less UGF sacrifice compared to having three or four gain stages inside the CMFB loop.

Another drawback of having two CMFB loops is that the offset and mismatch errors from the first loop affect the second CMFB loop. Assuming no mismatch or offset, the two CMFB loops set the CM output voltages to V_{CM}. However, since mismatch and offset errors exist, the actual CM voltage for the first and second CMFB loops are given by (114) and (115), respectively.

$$V_{cm1} = V_{CM} \pm V_{os,in,GCM1} \pm \frac{V_{o1,Diff}\,\Delta R_{CM1}}{4\left(1+A_{CMFB1}\right)R_{CM1}} \tag{114}$$

$$V_{cm2} = V_{CM} \pm V_{os,in,GCM2} \pm \frac{V_{out,Diff}\,\Delta R_{CM2}}{4\left(1+A_{CMFB2}\right)R_{CM2}} \pm \frac{G_{MB}R_{OUT}}{1+A_{CMFB2}}\left(V_{os,in,GCM1} + \frac{V_{o1,Diff}\,\Delta R_{CM1}}{4\left(1+A_{CMFB1}\right)R_{CM1}}\right) \tag{115}$$

Eq. (114) and (115) are expressed in terms of G_{MA}'s CM output voltage (V_{cm1}), G_{CM1}'s input-referred offset ($V_{os,in,GCM1}$), G_{MA}'s differential output voltage ($V_{o1,Diff}$), difference between

both R_{CM1} resistors (ΔR_{CM1}), G_{MB}'s CM output voltage (V_{cm2}), G_{CM2}'s input-referred offset ($V_{os,in,GCM2}$), G_{MB}'s differential output voltage ($V_{out,Diff}$), R_{CM2}'s error (ΔR_{CM2}), output resistance seen at V_{out} (R_{OUT}), second CMFB loop gain (A_{CMFB2}), and where R_{OUT} as given by:

$$R_{OUT} = R_{O7} // R_{O6} // R_{CM2} // R_{O} \tag{116}$$

where R_{O6} and R_{O7} are M_6's and I_7's output impedance, respectively. It can be seen from (115), that the error from the first CMFB loop affects the second CMFB loop's CM voltage. Although, if A_{CMFB2} is large enough compared to $G_{MB}R_{OUT}$ this contribution can be negligible.

5.3 Circuit Implementation

5.3.1 Gain-boosted differential pair (G_{MA})

G_{MA}'s simplified FD transistor-level and block-level implementation is shown in Fig. 66. This FD arrangement implements a high-gain high-BW OTA structure with CMFB, whose small-signal model is shown in Fig. 64 and described in subsection 2.3. The proposed OTA implements three transconductances but without using an extra transconductance stage. This configuration recycles the first stage's active loads, transistors M_3, as an additional feedforward gain path, thereby, achieving a LV high-gain stage in a compact transistor-level implementation.

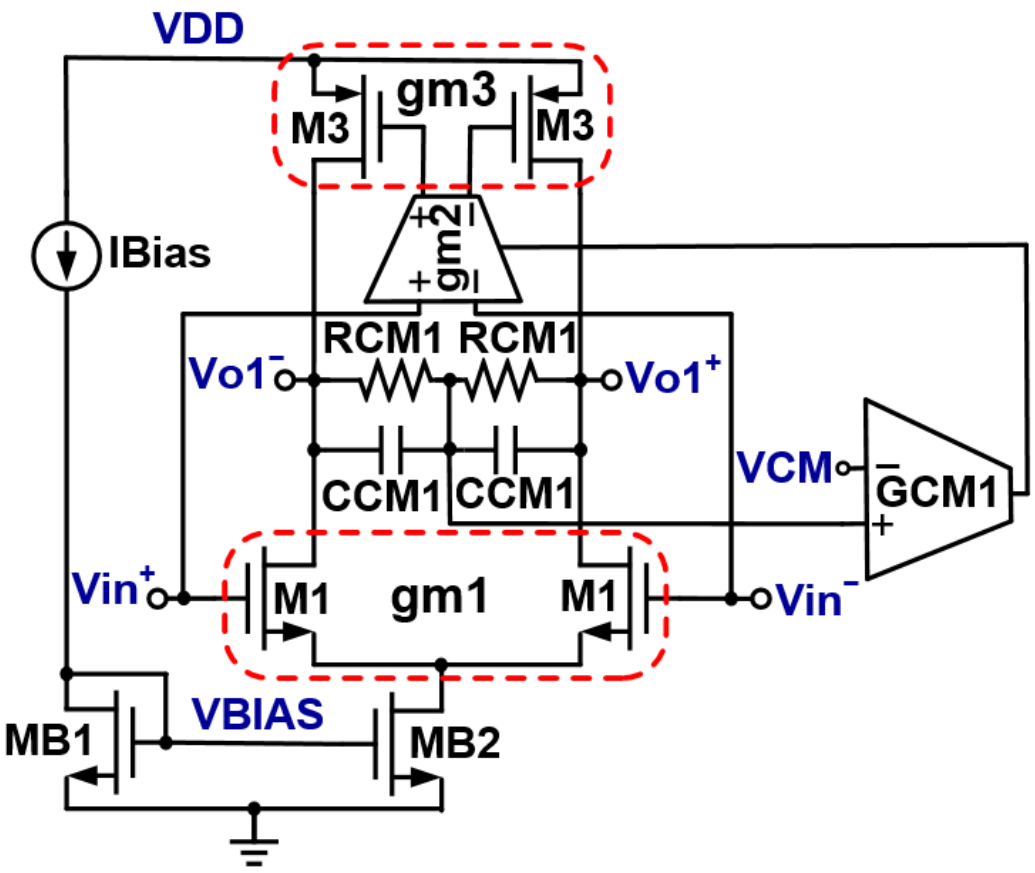


Fig. 66: G_{MA}'s simplified transistor-level and block-level implementation

G_{MA}'s full transistor-level implementation is shown in Fig. 67. Transconductances g_{m1}, g_{m2}, and g_{m3}, from Fig. 64, are implemented by transistor pairs M_1, M_2, and M_3, respectively. Note that g_{m3} is implemented by driving transistor M_3 while considering M_1 as active load. The gain-boosted differential pair consists of three NMOS differential pair amplifiers with active loads, one serving as the first stage, one as the gain boosting stage, and one as the CMFB stage. An RC passive CM sense circuit was used, instead of an active one, to have better linearity at such LV operation at the expense of area.

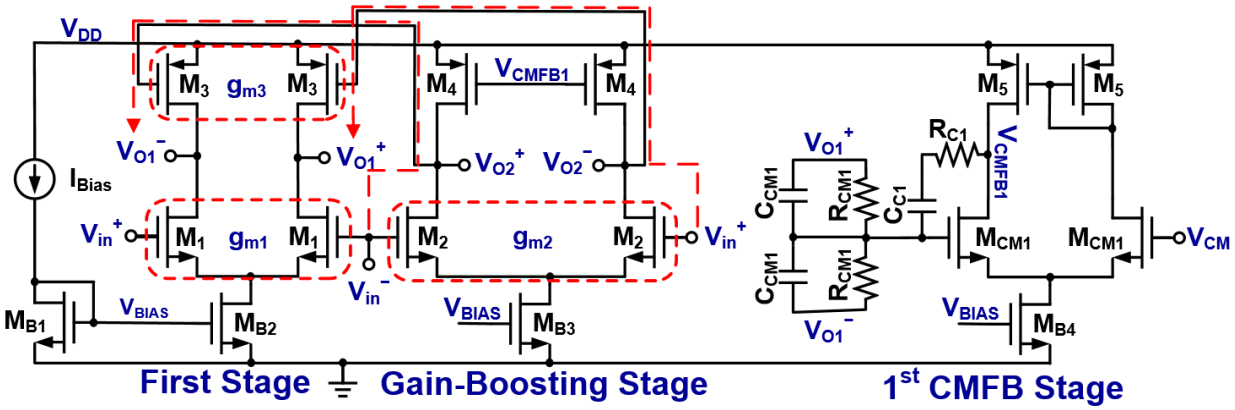


Fig. 67: G_{MA}'s transistor-level schematic with gain boosting and first CMFB loop

M_1 in Fig. 67 represent the main input differential pair NMOS transistors and M_3 are PMOS devices which form the active loads. The active loads, M_3, are differentially driven by the gain boosting stage formed by transistors M_2 and M_4, which form the second NMOS differential pair, g_{m2} in Fig. 66. This enhanced implementation increases the overall transconductance, as explained in subsection 2.3, and allows M_3 to act as an additional gain path instead of only as an active load, thereby increasing the small-signal gain without using extra transistors. The first stage's dc gain function is given by (117).

$$\frac{V_{o1}}{V_{in}} = G_{MA}R_{OA} = -\left(g_{m1} + \frac{g_{m2}g_{m3}}{g_{o2}+g_{o4}}\right)\left(\frac{1}{g_{o1}+g_{o3}+g_{CM1}}\right) = -\left[g_{m1} + g_{m2}g_{m3}\left(R_{o2}//R_{o4}\right)\right]\left(R_{o1}//R_{o3}//R_{CM1}\right) \quad (117)$$

where g_{m1}, g_{m2}, and g_{m3} are transistor's (M_1-M_3) transconductance; g_{o1}, g_{o2}, g_{o3}, and g_{o4} are transistor's (M_1-M_4) output conductance; R_{o1}, R_{o2}, R_{o3}, and R_{o4} are transistor's (M_1-M_4) output resistance; and g_{CM1} is R_{CM1}'s conductance.

CM sense resistors, R_{CM1}, and CM capacitors, C_{CM1}, form the passive CMFB sense circuit. In Fig. 67, transistors M_{CM1} and M_5 form the CMFB amplifier, who fixes the first stage's CM output voltage tfo the V_{CM} provided by an external reference voltage source, $V_{CM} = V_{DD}/2 = 0.3$ V in this design. The CMFB loop is stabilized by Miller compensation through C_{C1}. This sets the dominant pole at the sensing point. Additional high frequency zeros are introduced with R_{C1} in the Miller compensation network, and with C_{CM1} in the CM sense network. These zeros are required due to the high UGF required for the CMFB loop and to compensate the parasitic poles at V_{CMFB1} and V_{o2} in Fig. 67. The first CMFB loop transfer function is given by:

$$A_{CMFB1}(s) \approx \frac{g_{mcm1}R_{O,VCMFB1}\left(\frac{g_{m4}}{g_{o2}+g_{o4}}\right)\left(\frac{g_{m3}}{g_{o1}+g_{o3}}\right)\left[C_{C1}\left(R_{C1}-\frac{1}{g_{mcm1}}\right)s+1\right]\left(R_{CM1}C_{CM1}s+1\right)}{\left(g_{mcm1}R_{O,VCMFB1}R_{CM1}C_{C1}s+1\right)\left(\frac{C_{gg,M4}s}{g_{mcm1}}+1\right)\left(\frac{C_{gg,M3}s}{g_{o2}+g_{o4}}+1\right)\left(\frac{C_{M1}s}{g_{o1}+g_{o3}}+1\right)} \quad (118)$$

where g_{mcm1}, g_{m4}, $R_{O,VCMFB1}$, $C_{gg,M4}$, and $C_{gg,M3}$ are transistor's (M_{CM1} and M_4) transconductance, output impedance at node V_{CMFB1}, and transistor's (M_3 and M_4) gate capacitance.

The CMFB loop passive's values are $R_{CM1} = 200$ kΩ, $C_{CM1} = 0.3$ pF, $R_{C1} = 4.4$ kΩ, and $C_{C1} = 1$ pF. R_{CM1} was selected such that it only causes a 4% gain degradation in the first stage gain due to loading. C_{CM1}, R_{C1}, and C_{C1} were selected based on simulations to have the first CMFB loop's PM higher than 60°, in the worst-case scenario. M_{B1}-M_{B4} form conventional current biasing transistors since cascode current sources are impractical, due to the LV supply operation, and were avoided. The gain-boosted stage, G_{MA}, consisting of M_1, M_2, M_3, and M_4, achieves a dc gain of 46 dB, and consumes 540 μA from a $V_{DD} = 0.6$ V, where 240 μA are from the main stage, 240 μA from the gain boosting stage, and 60 μA from the CMFB amplifier.

5.3.2 Output stage (G_{MB})

G_{MB}, shown in Fig. 65, is a FD class-A programmable gain stage. It consists of four segments of a common source NMOS amplifier topology, formed by transistors M_6 and M_7, as shown in Fig. 68. Each segment is switched ON/OFF, in discrete steps, based on the filter's f_o requirements. Since the filter's f_o is changed by increasing or decreasing the filter's resistor values, G_{MB} is also modified to decrease or increase its output impedance and bias current. This allows to save power as the filter's f_o is decreased without sacrificing performance at high f_os.

G_{MB} shares the same control signals as the filter's resistor banks. During the OFF condition, transistors M_6 and M_7 are tied to ground (GND) and V_{DD}, respectively, and their gates are disconnected from the circuit by an open or high impedance switch. During the ON condition, M_6's and M_7's gates are connected by closing the switch between gate-and-bias, and gate-and-signal, respectively, and opening the V_{DD} and GND switches. To match the delay between G_{MB} sections, dummy switches that are always ON were added to the gates of the f_o = 20 MHz section, which is always active. The G_{MB} increments were chosen to keep the dc gain constant as R_O is changed for different f_os. This can be achieved by keeping the $G_{MB}R_{OUT}$ product constant.

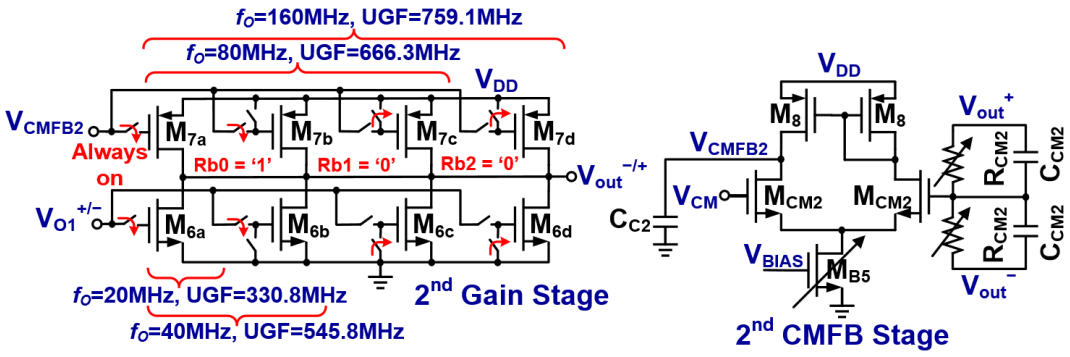


Fig. 68: G_{MB}'s single-ended transistor-level representation, with second CMFB loop

Keeping the dc gain constant helps to keep the filter's dc gain constant regardless of f_o. G_{MB}, without including its CMFB amplifier, consumes 1.48, 3.33, 5.18, and 8.15 mA for f_o = 20, 40, 80, and 160 MHz, respectively.

G_{MB} introduces a non-dominant pole, given by G_{MB}/C_O, into the OpAmp. Due to process variations this pole can vary widely and compromise the stability of the OpAmp, i.e. having a small G_{MB} due to a slow corner for NMOS transistors. For this particular architecture, two approaches can be used to address this problem. One is to design G_{MB} such that it will work even at the worst-case corner. This implies guaranteeing the minimum required G_{MB} during all corners such that the non-dominant pole does not affect its performance beyond what is desired. The drawbacks are larger area and power consumption for typical corners. However, no additional control circuitry or tuning is needed.

The second approach takes advantage of the fact that there are two CMFB loops. The first CMFB loop can be controlled independently of the second CMFB, therefore adjusting the first CMFB loop's V_{CM} to compensate for changes in G_{MB}. For example, in a slow NMOS corner, the V_{CM} voltage can be increased to increase the effective G_{MB}. The drawback is that an additional loop to control this voltage is needed, if a fully integrated solution is required. For this prototype, the two CMFB voltages were adjusted externally, and independently of each other.

The second CMFB stage is more complex than the first CMFB due to the varying resistive and capacitive load seen by the second CMFB, due to the programmable G_{MB}, which is required for the different f_o steps. The second CMFB loop, shown at the right side of Fig. 68, consists of programmable CM sense resistors, R_{CM2}, CM capacitors, C_{CM2} = 200 fF, and an NMOS differential pair with an adjustable bias current as the second CMFB amplifier. The second CMFB loop's transfer function is given by:

$$A_{CMFB2}(s) \approx \frac{\mathbf{g_{mcm2}R_{O,VCMFB2}}g_{m7}R_{O,VOUT}\left(\mathbf{R_{CM2}}C_{CM2}s+1\right)}{\left[\left(C_{C2}+\mathbf{C_{gg,M7}}\right)\mathbf{R_{O,VCMFB2}}s+1\right]\left(C_O\mathbf{R_{O,VOUT}}s+1\right)\left[\left(\frac{C_{gg,MCM2}}{2}+C_{CM2}\right)\mathbf{R_{CM2}}s+1\right]} \quad (119)$$

where g_{mcm2}, g_{m7}, R_{CM2}, C_{CM2}, C_{C2}, $C_{gg,M7}$, $C_{gg,MCM2}$, $R_{O,VCMFB2}$, and $R_{O,VOUT}$ are the transistors' (M_{CM2} and M_7) transconductance, second CMFB loop CM sense resistor and capacitor, second CMFB loop compensation capacitance, transistors' (M_7 and M_{CM2}) gate capacitance, and resistance seen at nodes V_{CMFB2} and V_{OUT}, respectively. In addition, parameters in bold are those changing as different sections of G_{MB} and R_{CM2} are being turned ON/OFF, and as the second CMFB circuit's bias is adjusted. The change in $g_{m7}R_{O,VOUT}$, numerator of (119), is ignored since M_7 was designed to keep the product constant independently of $R_{O,VOUT}$.

The second CMFB loop's dominant pole is located at CMFB amplifier's output, node V_{CMFB2} in Fig. 68. This is a high impedance node that forms a pole with M_7's parasitic gate capacitance, $C_{gg,M7}$, and compensation capacitor, C_{C2} = 400 fF, which is required to stabilize the CMFB loop when f_o = 20 MHz and capacitance $C_{gg,M7}$ is at its minimum. As G_{MB}'s sections are turned ON, the CMFB loop's dominant pole decreases due to the extra $C_{gg,M7}$ introduced by the additional M_7 sections. This decreases the CMFB loop's BW, and therefore, its UGF as the filter increases its f_o, decreasing the output stage's CM noise rejection. For that reason, the second CMFB amplifier increases its bias current as each section is turned ON, i.e. increasing g_{mcm2}, in order to increase the CMFB loop's BW and maintain good high-frequency CM noise rejection.

The two nondominant poles are located in the sense point at M_{CM2}'s gate and at the OTA's output. The latter is located at higher frequencies due to the OTA's low-output impedance, and as additional G_{MB} sections are turned ON, it increases its frequency even further.

The CM sense resistors, R_{CM2}, and CMFB NMOS transistor input pair's, M_{CM2}, gate capacitance form a parasitic pole that decreases the CMFB loop's PM. As the filter increases f_o, by decreasing the main filter's resistors, R_{CM2} also needs to be decreased to push the parasitic pole to higher frequencies, and improve the second CMFB loop's PM as the CMFB loop's UGF is increased. R_{CM2} is implemented with resistor banks and designed to always be 10x of R_O, or 40/20/10/5 kΩ, respectively for each f_o increment. This is to improve the second CMFB loop's PM without excessively loading the OTA's output node. C_{CM2} and R_{CM2} form a zero that boosts the PM and moves with the nondominant pole at M_{CM2}'s gate with the decrease in R_{CM2}.

G_{MB} achieves full programmability that tracks the system level filter's requirements, which maintain high performance for high f_os and save power for low f_os. R_{CM2}'s control signals are the same ones that control the filter's R_O and G_{MB} sections, so no additional control overhead is required. The second CMFB amplifier consumes 15, 30, 45, and 75 µA from a V_{DD} = 0.6 V when the filter's f_o is 20, 40, 80 and 160 MHz, respectively.

5.3.3 OTA's Input-Referred Noise and Offset

The proposed OTA's input referred noise and offset are analyzed in this section. The following assumptions have been made to simplify the analysis: 1) G_{MB}'s noise and offset have been neglected, since when input-referred, they are divided by the first stage's gain and become less significant compared to the first stage's noise and offset; 2) The noise contribution from bias transistors and CM circuits, with the exception of CM resistors, has been neglected. This is because due to the fully differential implementation those noise sources are CM signals and will produce no differential output [42].

The G_{MA}'s low-frequency output-noise spectral density, refer to Fig. 67, is given by:

$$\upsilon_{n,out}^{\ 2} \approx 8kT\gamma\left(g_{m2}+g_{m4}\right)\frac{g_{m3}^{\ 2}}{\left(g_{o1}+g_{o3}+g_{CM1}\right)^4} \tag{120}$$

where g_{m4} and γ are M_4's transconductance and noise coefficient, respectively. It can be observed from (120) that the dominant source of noise is due to transistors M_2 and M_4 in the gain boosting stage. This is because their current noise is amplified to the output by M_3's transconductance and the output impedance at node V_{o1}. Assuming G_{MA}'s noise dominates and input referring it, (120) becomes:

$$\upsilon_{n,in}^{\ 2} \approx 8kT\gamma\left(g_{m2}+g_{m4}\right)\left(\frac{g_{o2}+g_{o4}}{g_{m2}}\right)^2\left(\frac{1}{g_{o1}+g_{o3}+g_{CM1}}\right)^2 \tag{121}$$

where the first term is the noise contribution of M_2 and M_4, the second term is the inverse gain of the gain-boosting stage, and the third term is G_{MA}'s output impedance. As it can be observed in (121), the proposed OTA's noise is dominated by the transistors in the gain-boosting stage. Full derivations for both (120) and (121) can be found in appendix C.

The simulated OTA's integrated input-referred noise is 9.74 μV_{RMS} for all configurations. This confirms what was previously discussed in subsection 2.3 that changing the OTA's G_{MB} configuration does not affect the input-referred noise. Nevertheless, the overall filter's noise does change since the integration BW increases. It is important to notice that the increase in BW is obtained by decreasing in half R_O, therefore the noise due to the passive components stays constant. However, the OTA's noise contribution increases due to the increased filter's f_o.

To calculate the differential offset, it was assumed that all devices follow the square-law model for the current, and that there is no channel-length modulation. The procedure followed by [89] was used for the proposed LV OTA's input-referred offset derivations, as with noise, only G_{MA} was considered. It was assumed that the main contributions to offset were mismatch variations in threshold voltage ($\Delta V_{TN/P}$), gate-to-source voltage (ΔV_{GS}), and size ($\Delta W/L$) between matched transistor pairs. First, the current offset at the first stage's output, V_{o1}^{+} and V_{o1}^{-} in Fig. 67, due to transistors in the main stage and gain-boosting stage was obtained. The obtained output current offset was then input-referred by dividing it by G_{MA}, where G_{MA} is the first stage's transconductance and is given in (117). Following the above procedure and after some approximations, appendix D shows the complete derivation, the input-referred offset is given by:

$$\Delta V_{OS,in}{}^2 \approx \left(\frac{g_{m1}}{G_{MA}}\right)^2 \left\{ \Delta V_{TN1}{}^2 + \left(\frac{V_{GS1}-V_{TN}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_1}\right)}{\frac{W}{L_1}}\right]^2 \right\} + \left(\frac{g_{m3}}{G_{MA}}|A_{Boost}|\right)^2 \left\{ \Delta V_{TN2}{}^2 + \left(\frac{V_{GS2}-V_{TN}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_2}\right)}{\frac{W}{L_2}}\right]^2 \right\} \quad (122)$$

where ΔV_{TN1} and $(\Delta W/L_1)/W/L_1$ are the threshold voltage (V_T) mismatch and size mismatch ratio in M_1; ΔV_{TN2} and $(\Delta W/L_2)/W/L_2$ are the V_T mismatch and size mismatch ratio in M_2; $|A_{Boost}|$ is the gain-boosting stage's dc gain; and $\Delta V_{TN1}{}^2$, $[(\Delta W/L_1)/W/L_1]^2$, $\Delta V_{TN2}{}^2$, and $[(\Delta W/L_2)/W/L_2]^2$ represent standard deviations [89]. It can be observed from (122) that the mismatch from the gain boosting stage's input pair, the second term in the right side of (122), is the dominant source of input-referred offset. This comes from the fact that its mismatch is multiplied by $(g_{m3}|A_{Boost}|/G_{MA})^2$, which is close to one, whereas the offset from the first stage is multiplied by $(g_{m1}/G_{MA})^2$, which is smaller than one. Among the two dominant error sources, namely V_T mismatch and size mismatch

ratio, the dominant one comes from the V_T mismatch [90]. In order to decrease the V_T mismatch by half, the area has to increase by four times [90].

5.3.4 OTA's Compensation

Miller compensation was used for stabilization purposes between G_{MA} and G_{MB}, as shown in Fig. 63. Miller compensation was used since it does not require additional active circuitry, which saves power. C_{M1} and R_{M1} are 7.4 pF and 320 Ω, respectively. C_{M1} uses the Miller effect to create a dominant pole at G_{MA}'s output, while pushing the nondominant pole, at G_{MB}'s output node, to higher frequencies. R_{M1} is used to move the right-half plane zero, created by C_{M1}, to the left-half plane in order to improve PM. The simulated gain and phase vs. frequency, for all four OTA configurations, is shown in Fig. 69. The overall OTA's differential transfer function, including the pole and zero inside G_{MA}, is given by:

$$\frac{V_O(s)}{V_{in}(s)} = \frac{A_0\left(1+\frac{s}{\omega_{z1,GMA}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2,GMA}}\right)\left(1+\frac{s}{\omega_{p3}}\right)\left(1+\frac{s}{\omega_{p4}}\right)} \tag{123}$$

where using the location of the poles and zeros in terms of circuit parameters leads to:

$$\frac{V_O(s)}{V_{in}(s)} \approx \frac{G_{MA}R_{OA}G_{MB}R_{OUT}\left(\frac{g_{m1}C_2 s}{g_{m2}g_{m3}}+1\right)\left[C_{M1}\left(R_{M1}-\frac{1}{\mathbf{G_{MB}}}\right)s+1\right]}{\left(G_{MB}R_{OUT}R_{OA}C_{M1}s+1\right)\left(1+sR_{o2}C_2\right)\left(\frac{C_O s}{\mathbf{G_{MB}}}+1\right)\left(C_{OA}R_{M1}s+1\right)} \tag{124}$$

where R_{OUT} and C_O are the resistance, including loading from R_O, and capacitance seen at the OTA's output node. Parameters in bold are those that change as different configurations are used, the $G_{MB}R_{OUT}$ product is ignored since, by design, it remains constant and is independent of the OTA's configuration.

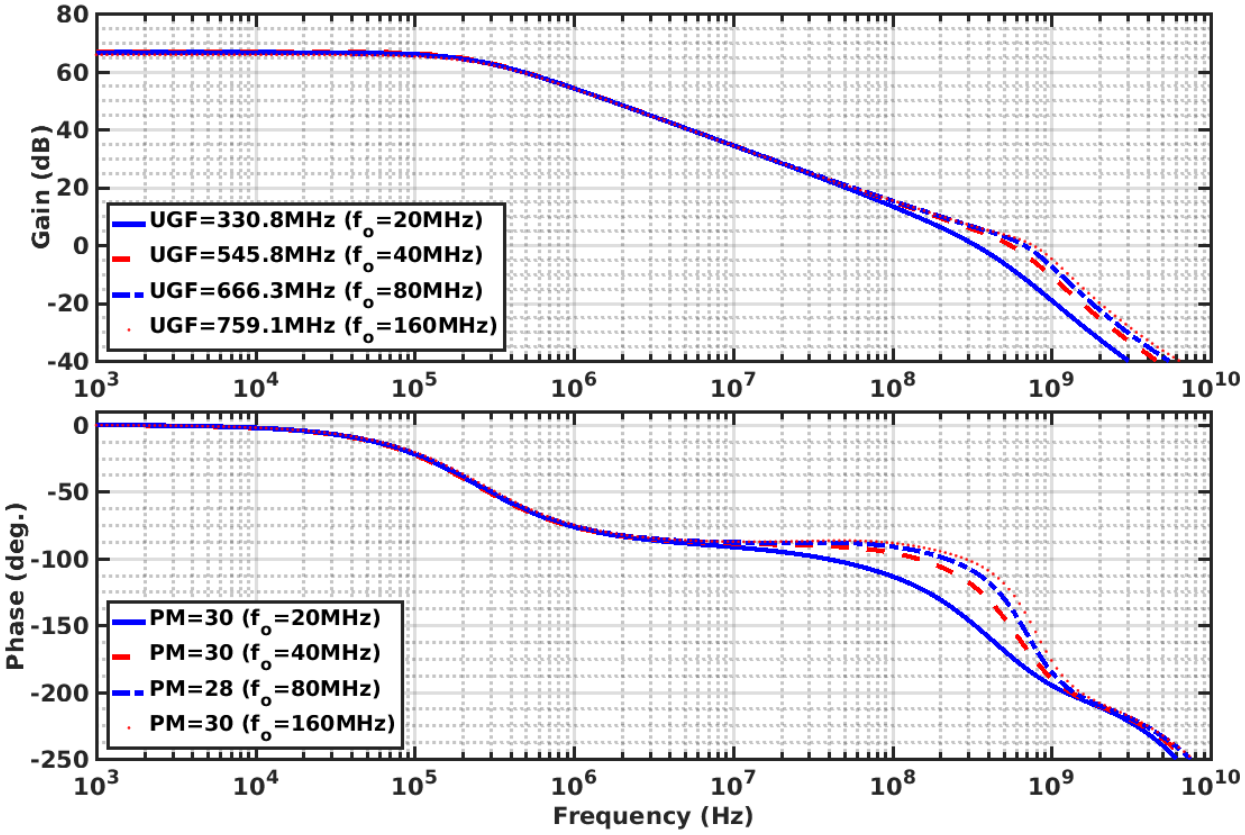


Fig. 69: Simulated OTA's gain and phase versus frequency

Including loading effects due to R_O and C_O, the OTA achieves a constant dc gain of 66 dB, a maximum UGF of 759 MHz, a minimum PM of 28°, and consumes a maximum power of 5.27 mW. Table 16 shows the ac parameters for all four OTA configurations, relevant

transconductances, the calculated pole and zero locations as given by (124), and the calculated UGF as given by (127). A minimum acceptable PM of 12° was found in [78] to be the minimum required PM for the Tow-Thomas biquad with a Q = 1.3 and f_o/UGF = 0.21, which represents the worst-case scenario. Therefore, an OTA's PM of only 28° has enough stability margin for the Tow-Thomas filter implementation with Butterworth response to be stable. In this design, some margin was added to account for additional phase degradation after layout and fabrication.

Table 16: OTA's simulated ac characteristics and calculated poles and zeros

Simulated Parameters	**f_o= 20 MHz**	**f_o= 40 MHz**	**f_o= 80 MHz**	**f_o= 160 MHz**
dc gain (dB)	66.56	66.90	66.33	65.72
UGF (MHz)	330.80	545.80	666.30	759.10
f_o/UGF	0.06	0.07	0.12	0.21
Phase Margin (°)	30	30	28	30
g_{m1} (mS)	2.216	2.216	2.216	2.216
g_{m2} (mS)	2.051	2.051	2.051	2.051
g_{m3} (mS)	1.51	1.51	1.51	1.51
G_{MA} (mS)	27.716	27.716	27.716	27.716
G_{MB} (mS)	10.32	23.09	48.96	74.82
$G_{MB}R_{OUT}$ (V/V)	10.26	10.58	10.72	9.88
Power G_{MA}[1] (mW)	0.33	0.33	0.33	0.33
Power G_{MB}[1] (mW)	0.90	2.03	3.15	4.94
Total power[1] (mW)	1.23	2.36	3.48	5.27
Calculated Parameters[2]	**f_o= 20 MHz**	**f_o= 40 MHz**	**f_o= 80 MHz**	**f_o= 160 MHz**
f_{p1} (MHz)	0.27	0.26	0.26	0.28
$f_{p2,GMA}$ (MHz)	50.84	50.84	50.84	50.84
f_{p3} (MHz)	246.25	550.96	1168.25	1785.30
f_{p4} (MHz)	687.91	687.91	687.91	687.91
$f_{z1,GMA}$ (MHz)	583.35	583.35	583.35	583.35
f_{z2} (MHz)	96.4	77.7	71.8	70.1
UGF (MHz)	302.14	503.30	762.59	953.75

[1] Including both CMFB circuits
[2] Using (124) for poles and zeros, and (127) for UGF

Equation (123) can be used to find an approximation for the OTA's UGF, which is given by:

$$\omega_{UGF}=\sqrt{\frac{A_0\omega_{p1}\omega_{p2,GMA}\omega_{p3}\omega_{p4}}{\omega_{z1,GMA}\omega_{z2}}} \tag{125}$$

which is only valid for transfer functions of the form as given by (123). The approach used to arrive at (125) can be found in appendix E. To mathematically explain the UGF effect, the poles and zeros as given in (124) are used into (125) to obtain:

$$\omega_{UGF}=\sqrt{\frac{\left(G_{MA}R_{OA}G_{MB}R_{OUT}\right)\left(\frac{1}{G_{MB}R_{OUT}R_{OA}C_{M1}}\right)\left(\frac{1}{R_{o2}C_2}\right)\left(\frac{\mathbf{G_{MB}}}{C_O}\right)\left(\frac{1}{C_{OA}R_{M1}}\right)}{\left(\frac{g_{m2}g_{m3}}{g_{m1}C_2}\right)\left[\frac{1}{C_{M1}\left(R_{M1}-\frac{1}{\mathbf{G_{MB}}}\right)}\right]}} \tag{126}$$

by simplifying, the proposed LV OTA's UGF is given by:

$$\omega_{UGF}=\sqrt{\frac{G_{MA}g_{m1}\left(\mathbf{G_{MB}}-\frac{1}{R_{M1}}\right)}{g_{m2}g_{m3}R_{o2}C_{OA}C_O}} \tag{127}$$

which is valid as long as $G_{MB} > 1/R_{M1}$. By increasing G_{MB} when additional G_{MB} sections are turned ON, the UGF is increased without changing the dominant pole's location. This can be observed in Fig. 69, where the dominant pole remains constant but the UGF is increased from 330 MHz to 759 MHz, as additional G_{MB} sections are turned ON. As G_{MB} is increased, the UGF increases due to the third pole, given by ~ G_{MB}/C_O, moving to higher frequencies. It is important to notice that in this design, the GBW, given by G_{MA}/C_{M1}, remains constant but the UGF, determined by the location of the nondominant poles and zeros, is modified as the third pole is pushed to higher frequencies for increasing G_{MB}. In this design, R_{M1} is used to move the right-half plane zero to the left-half plane in order to improve stability, which can be achieved as long as $R_{M1} > 1/G_{MB}$. However, as the zero goes to even lower frequencies, by further increasing R_{M1}, the UGF increases, see (127), and by consequence the PM decreases. On the other hand, as G_{MB} increases the impact of R_{M1} on UGF and PM decreases, relative to the impact of the change in G_{MB} itself. This can be observed mathematically if the derivatives of ω_{UGF} and ω_{z2} with respect to G_{MB} and R_{M1} are obtained. Equations (128)-(131) show the partial derivatives of ω_{UGF} and ω_{z2} with respect to G_{MB} and R_{M1}.

$$\frac{\partial \omega_{UGF}}{\partial G_{MB}} = \frac{1}{2}\sqrt{\frac{G_{MA} g_{m1}}{g_{m2} g_{m3} R_{o2} C_{OA} C_O \left(G_{MB} - \frac{1}{R_{M1}} \right)}} \tag{128}$$

$$\frac{\partial \omega_{UGF}}{\partial R_{M1}} = \frac{1}{2R_{M1}^{\,2}}\sqrt{\frac{G_{MA} g_{m1}}{g_{m2} g_{m3} R_{o2} C_{OA} C_O \left(G_{MB} - \frac{1}{R_{M1}} \right)}} \tag{129}$$

$$\frac{\partial \omega_{z2}}{\partial G_{MB}} = -\frac{1}{C_{M1}\left(G_{MB}R_{M1}-1\right)^2} \tag{130}$$

$$\frac{\partial \omega_{z2}}{\partial R_{M1}} = -\frac{G_{MB}{}^2}{C_{M1}\left(G_{MB}R_{M1}-1\right)^2} \tag{131}$$

Equations (128)-(131) show that:

$$\frac{\partial \omega_{UGF}}{\partial G_{MB}} > \frac{\partial \omega_{UGF}}{\partial R_{M1}} \tag{132}$$

$$\frac{\partial \omega_{z2}}{\partial G_{MB}} > \frac{\partial \omega_{z2}}{\partial R_{M1}} \tag{133}$$

For this reason, a fixed R_{M1} was used for all configurations to save additional circuitry and complexity required for a tuning scheme for R_{M1} that would not be as effective. In this design, R_{M1}'s value was selected primarily considering the case for the lowest G_{MB}, i.e. f_o = 20 MHz, and simulations were performed to verify that its impact on the other configurations was not detrimental. This is not to say that R_{M1} has no effect on UGF or PM even at the higher frequencies, other designers may still adjust R_{M1} for better UGF/PM performance at each configuration if the additional circuitry and time are available.

As the filter's f_o is increased, the f_o/UGF ratio, shown in Table 16, also increases creating additional Q-enhancement for higher frequencies. This can be solved by further increasing GBW, i.e., increasing G_{MA} or decreasing C_{M1}, along with increasing G_{MB} to further increase the UGF. However, this comes at the price of additional power consumption and makes the design not so

power efficient. The approach used in this design was to lower the Q resistors' value at the system level, as f_o is increased, to compensate the Q-enhancement introduced by the OTA's UGF.

5.3.5 Filter's Passive Components

Each resistor and capacitor inside the proposed filter in Fig. 61 are implemented via a resistor and capacitor bank. In the resistor banks, shown in Fig. 70's left side, all unit resistors have the same width so that they can be matched in layout. All resistor banks are implemented the same way, both the main resistor and the Q resistors, the only difference is the resistance value. The switches control the effective filter's resistor, R_O, which determine the filter's f_o. The resistors that determine the filter's Q also scale down with changes in R_O as to keep the Q constant. The value of every resistor for the different f_os, including the switch resistance, is given in Table 17. As explained previously in subsection 2.1, passive compensation was used to counteract the Q-enhancement effects due to the filter's f_o/GBW. The designed Q, Q_d, for each of the f_os is decreased as f_o is increased, as shown in Table 17. This is done by decreasing the value of Q_d until simulations match the Q_{Eff} with the desired one. Therefore, the values for Q_d presented in Table 17 lead to the desired Qs for both biquads, $Q_1 = 0.54$ and $Q_2 = 1.3$, respectively.

Each switch is implemented with an NMOS transistor that is controlled by an external 1.2 V supply to keep low resistance even with large signal swings. All the switches' parasitic capacitance, per resistor bank, amounts to 60 fF and does not contribute to added phase shift in the frequencies of interest. In more compact solutions, this supply can be integrated on-chip by using a low power charge pump or additional source since it only drives gates which do not consume quiescent power. The resistor bank can be configured between 4, 2, 1, and 0.5 kΩ, which correspond to the control signals given by R_b = '000', '001', '011' and '111', respectively. Matching

among differential resistors, as well as transistor pairs for that matter, is critical for even order linearity cancellation [89].

The right side of Fig. 70 shows the layout for each resistor pair in the FD filter, where the letter 'D' represents a dummy resistor. All resistor pairs were put in close proximity in the final layout to reduce variations between them.

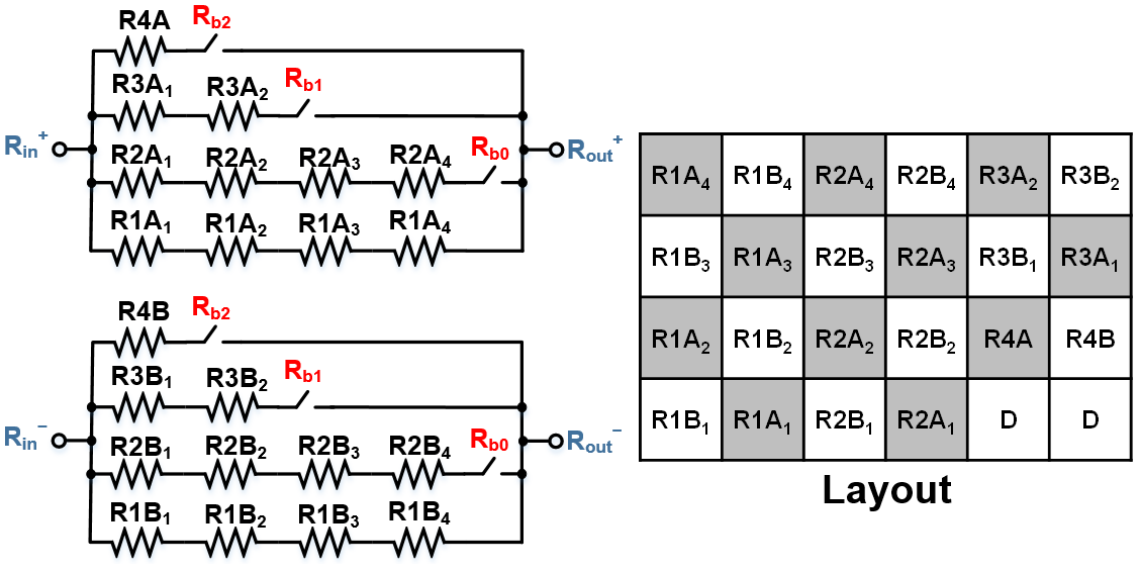


Fig. 70: Resistor bank implementation and layout

Table 17: Resistor values and designed Qs for R_O, Q_1R_O, and Q_2R_O

Resistor Name	Resistor Bank				Designed Qs (Q_d)		
	R_O (Ω)	Q_1R_O (Ω)	Q_2R_O (Ω)		f_o (MHz)	$Q_{d,1}$	$Q_{d,2}$
$R_{1,Total}$	3852	1956	4368		20	0.507	1.134
$R_{2,Total} + R_{b0}$	3472 + 167	1552 + 80	3240 + 167		40	0.475	1.023
$R_{3,Total} + R_{b1}$	1713 + 80.5	650 + 39	1292 + 80.5		80	0.424	0.873
$R_{4,Total} + R_{b2}$	845 + 39	272 + 19	511 + 39		160	0.370	0.724

The capacitor bank was implemented with a 4-bit binary weighted array as shown in Fig. 71. The nominal value, at the midway point in the binary code, was designed to be 2 pF. To implement the capacitor bank, a combination of metal-oxide-metal (MOM) comb structures below metal-insulator-metal (MIM) capacitors was used to save area. The MIM capacitors' bottom plates were all connected to the OTA's low-impedance output node. This was to prevent the MIM capacitor's bottom plate parasitic capacitance from contributing to the parasitic pole at the OTA's input once the OTA is connected in feedback. After fabrication, this capacitor bank can tune deviations in the RC time constant in steps of ±100 fF. The capacitor bank also allows for a constant −40/+35% f_o tuning in the filter regardless of the f_o being used. Similar to the resistor arrays, the capacitors were laid out in pairs and put in close proximity so that variations between the capacitors are minimized. Similar to the resistor banks, the switches that control the capacitor banks are implemented with NMOS switches controlled by 1.2 V.

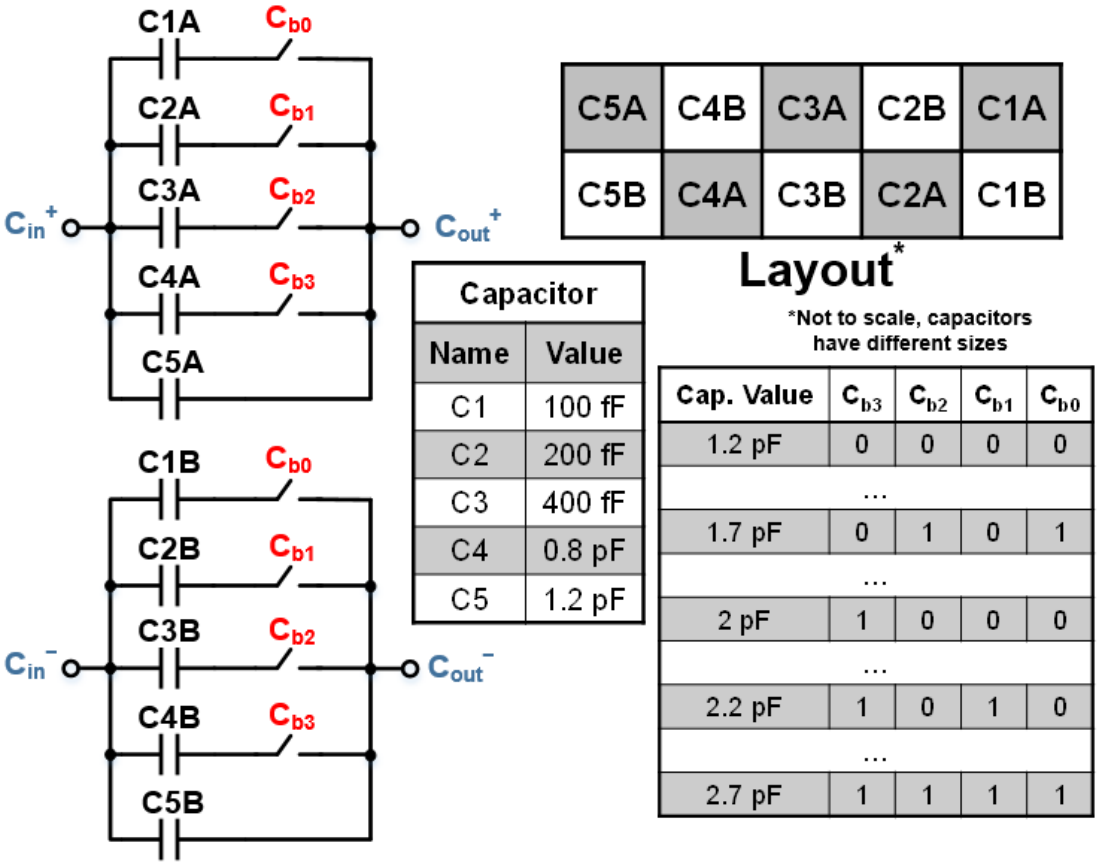


Fig. 71: Capacitor bank implementation and layout

5.3.6 Filter's Frequency and Step Responses

The 4th-order Butterworth filter can be configured for an f_o = 20/40/80/160 MHz. The filter's simulated ac frequency response for all f_os is shown in Fig. 72. The simulated f_os are at 19.7 MHz, 39.47 MHz, 79.5 MHz, and 154.7 MHz, also no peaking is observed in the frequency response. The capacitor bank, discussed previously in subsection 3.5, adjusts f_o after fabrication. To test the filter's transient behavior, a small input transient step, $V_{in,diff}$ = 0.1 V, is applied. The filter's simulated positive and negative step responses for all f_os are shown in Fig. 73, and Fig. 74, respectively.

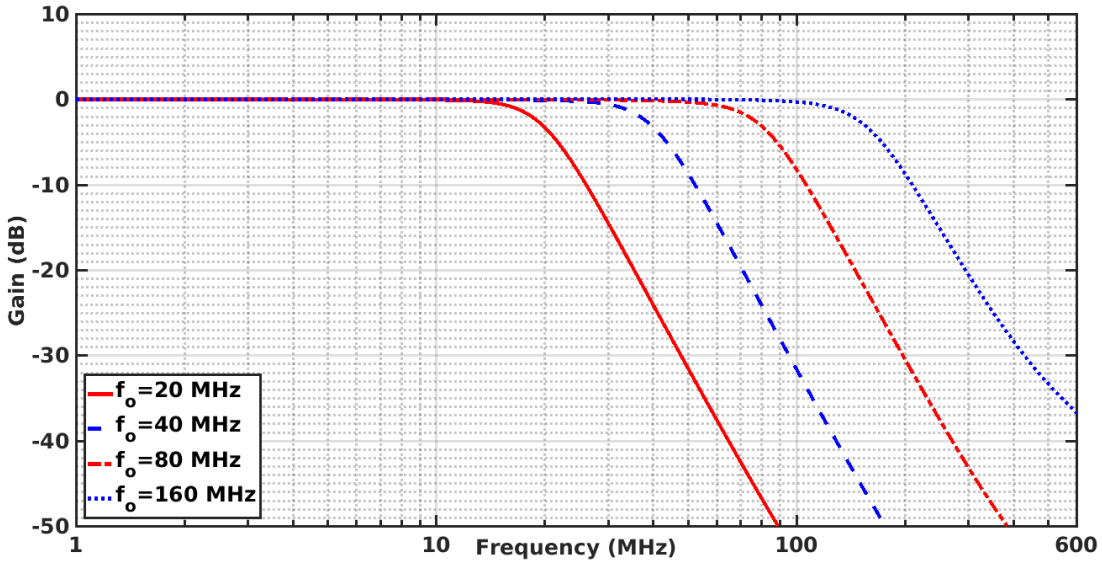


Fig. 72: Proposed filter's simulated ac frequency response. V_{DD} = 0.6 V, V_{CM} = 0.3 V.

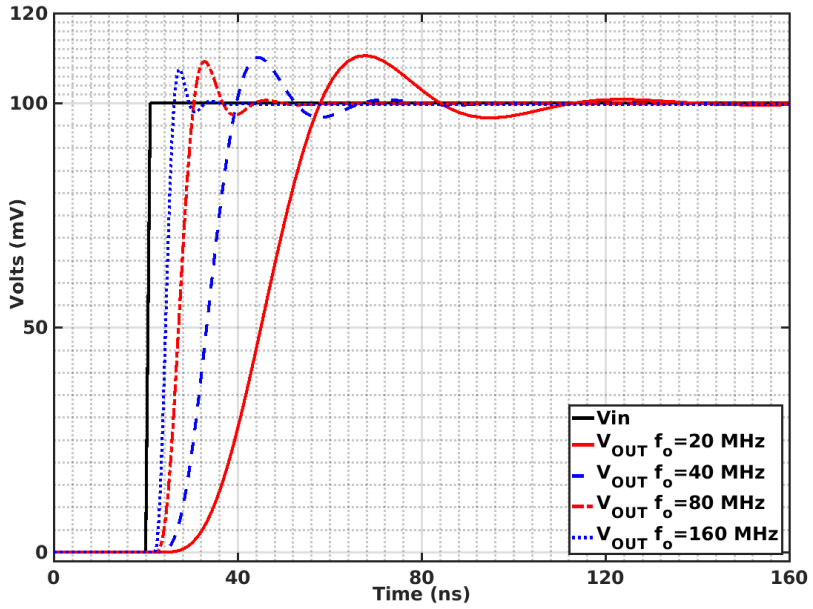


Fig. 73: Proposed filter's simulated positive step response. V_{DD} = 0.6 V, V_{CM} = 0.3 V, $V_{in,Diff}$ = 0.1 V.

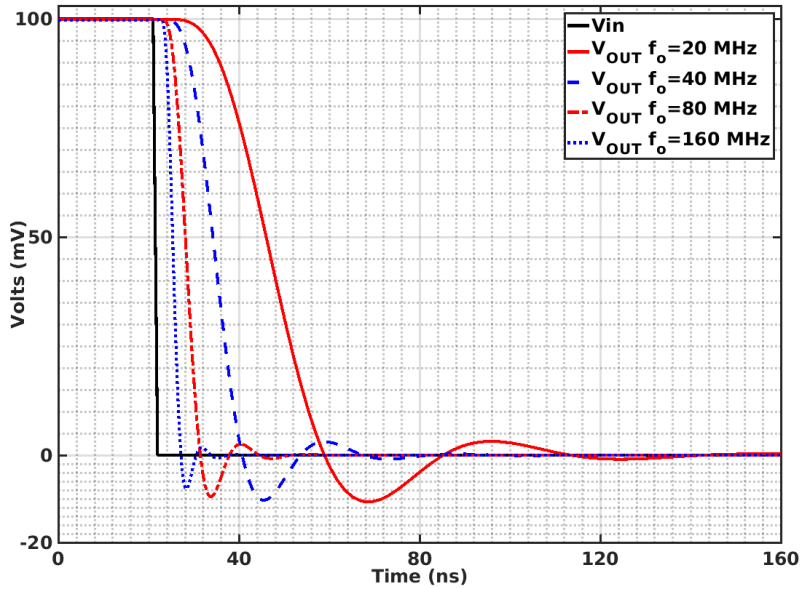


Fig. 74: Proposed filter's simulated negative step response. V_{DD} = 0.6 V, V_{CM} = 0.3 V, $V_{in,Diff}$ = 0.1 V.

5.4 Experimental Results

The 4th-order active-RC LV Butterworth LPF, using the proposed LV OTA, was fabricated in a CMOS 130 nm process through MOSIS. The NMOS and PMOS transistors have a V_T of 150 mV and 170 mV, respectively. Due to the LV constraints all transistor's saturation voltage (V_{dsat}) are equal or lower than 100 mV. The filter's passives and LV OTAs occupy 0.066 mm^2 and 0.192 mm^2, respectively, for a total chip area of 0.236 mm^2. The chip's microphotograph is shown in Fig. 75. The designed filter's f_o can be changed between 20/40/80/160 MHz, where f_o's control bits were implemented at the PCB level. However, in a complete system these signals would be generated internally based on the system's required f_o step and can be driven by digital logic circuits.

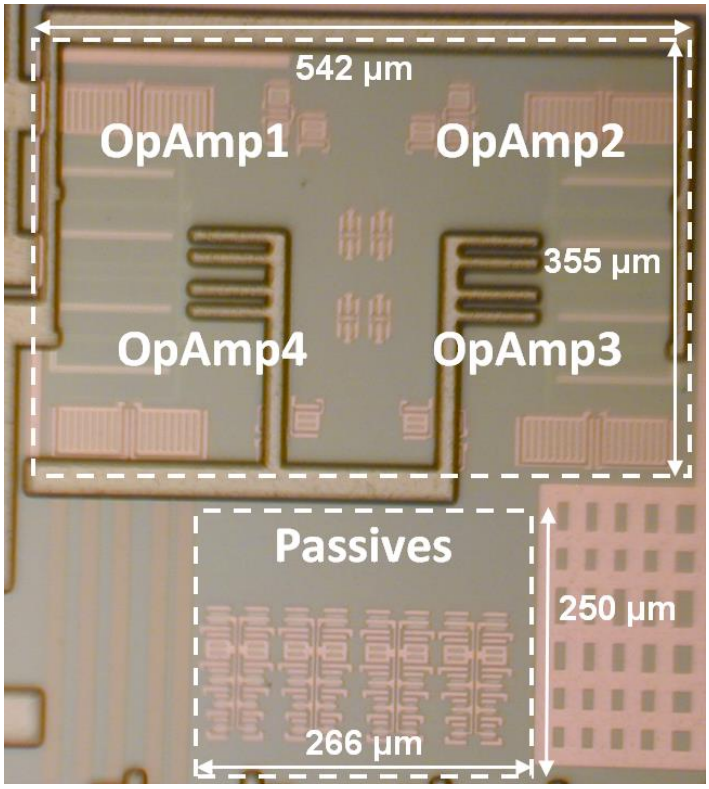


Fig. 75: 4th-order LV LPF microphotograph

The filter consumes a total of 5.56/10.6/15.64/23.77 mW when f_o = 20/40/80/160 MHz, respectively, with V_{DD} = 0.6 V. Two external voltage references are used for both V_{DD} = 0.6 V and V_{CM} = 0.3 V. The filter's measurement test-bench is shown in Fig. 76, where the input balun is used to convert the input signal from single ended to a FD signal. To decouple the dc voltage between the filter and the external 50 Ω FD output buffer, ac coupling capacitors are used at the filter's output. The output buffer drives the 50 Ω output balun connected to the measurement equipment.

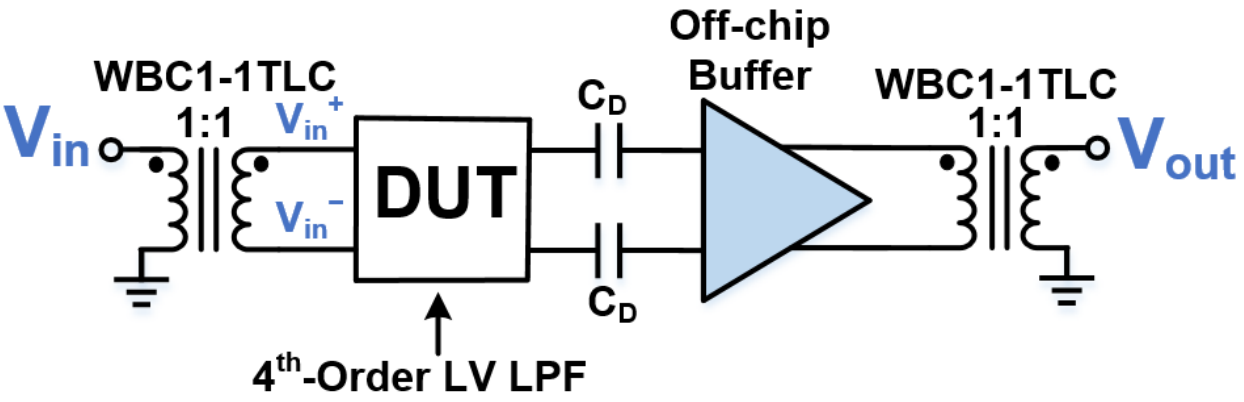


Fig. 76: 4th-order LV LPF measurement setup

The filter's frequency response for all four f_o configurations is shown in Fig. 77, where the input voltage used was a 100 mV peak-to-peak sinusoidal signal measuring between V_{in}^+ and V_{in}^- in Fig. 76. The binary word, which is controlled by off-chip digital signals, for the capacitor banks at each f_o configuration is '0111', '0111', '0101', and '0010' for 20/40/80/160 MHz, respectively. The filter's high-frequency f_o configurations were more susceptible to C_O's parasitic capacitance, and therefore, C_O was decreased as the high-f_o configurations were used. Some peaking can also be observed in the frequency response, see Fig. 77, for f_o = 160 MHz around the filter's f_o. The response peaks up to 3 dB above the desired gain, 0 dB, which is caused by Q-enhancement, described in subsection 2.1, due to a decrease in OpAmp's PM due to process variations. Active Q-tuning calibration schemes present in the literature, [91-94], can be used to compensate for this effect after the filter's fabrication.

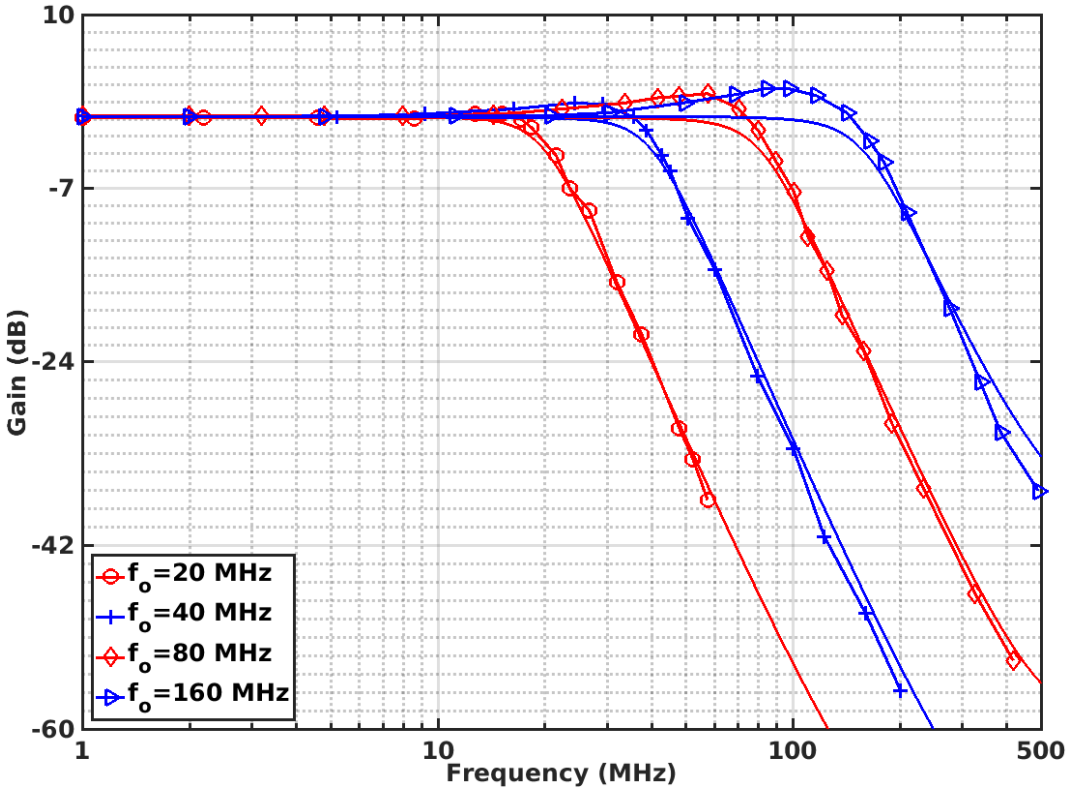


Fig. 77: Proposed LV filter's simulated (solid lines) and measured (marked lines) frequency response. V_{DD} = 0.6 V, V_{CM} = 0.3 V, and $V_{in,pk\text{-}pk}$ = 0.1 V.

The tuning range for each configuration is shown in Fig. 78, where only the maximum, minimum, and nominal f_o configurations are shown. This tuning range only needs to cover component variations and other PVT effects, it was not designed to be a continuous tuning scheme but a way to tune f_o to its predetermined value. The highest frequency configuration, f_o = 160 MHz, suffered a reduced tuning range due to the excessive loading due to C_O.

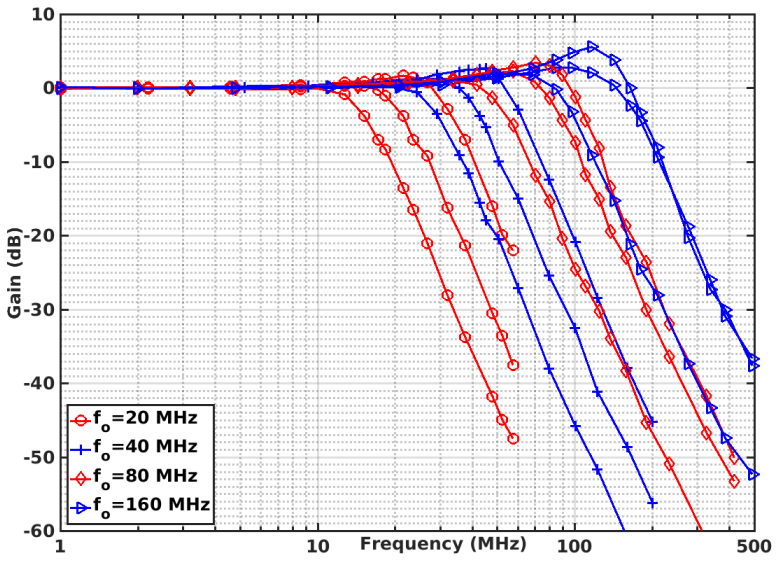


Fig. 78: Capacitor bank's tuning range: minimum (C=1111'b), maximum (C=0001'b), and nominal f_o. V_{DD} = 0.6 V, V_{CM} = 0.3 V, and $V_{in,pk\text{-}pk}$ = 0.1 V.

To measure the filter's dynamic performance along with THD, SNDR, spurious-free DR (SFDR) and P_{1dB}, a test input sinusoidal signal at 2/4/8/16 MHz, for f_o = 20/40/80/160 MHz, respectively, was increased in magnitude. Fig. 79 shows the measured dynamic performance where the THD at full-scale voltage (FSV) is 66.17/60.6/61.65/50.7 dB, SNDR = 59.26/55.59/54.4/45.37 dB, SFDR = 66.55/60.7/61.83/50.71 dB, and P_{1dB} = 6.96/7/6.81/4.26 dBm, for f_o = 20/40/80/160 MHz, respectively. The results are plotted against the differential input voltage (V_{in}) expressed in dBm. The measured peak-to-peak differential value of V_{in} was used to mathematically convert to dBm as if a 50 Ω impedance was present, although no 50 Ω impedance is seen at V_{in}. This allows for an easy comparison between other works, [62, 74], where V_{in} is shown in dBm.

SNDR is calculated as the ratio between the output voltage and the root-sum-square of the integrated noise and the distortion components. This can be mathematically expressed as:

$$\mathrm{SNDR}\left(\mathrm{V/V}\right)=\frac{\mathrm{V_{OUT,RMS}}}{\sqrt{\mathrm{V_{N,RMS}}^{2}+\mathrm{V_{Distortion,RMS}}^{2}}} \tag{134}$$

The proposed filter's performance metrics for all f_o configurations are shown in Table 18. The filter is noise limited by passive's noise at the low f_o configurations, 20 and 40 MHz; its noise is equally split between passive's and OTA's noise for f_o = 80 MHz, and dominated by the OTA's noise at f_o = 160 MHz.

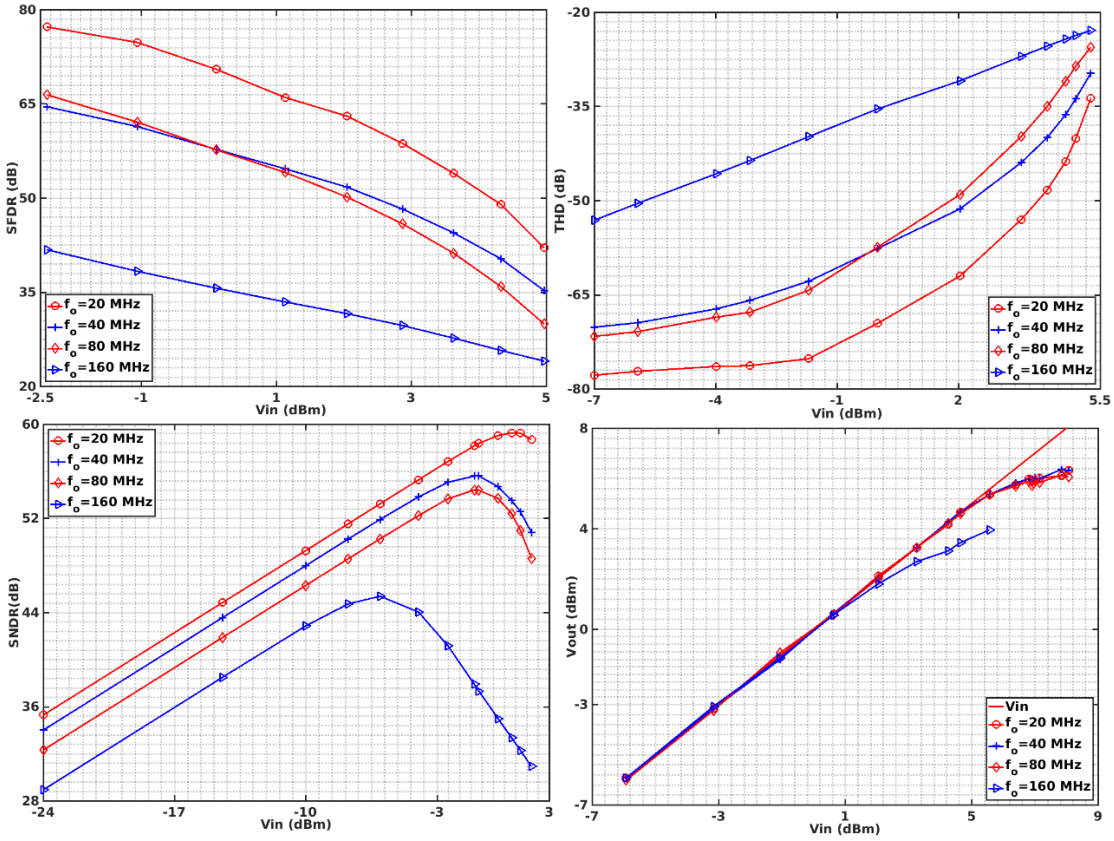


Fig. 79: Proposed LV filter's measured dynamic performance: THD (dB), SNDR (dB), SFDR (dB), and P_{1dB} (dBm) vs. V_{in} (dBm). V_{DD} = 0.6 V, V_{CM} = 0.3 V, and f_{in} = 2/4/8/16 MHz for f_o = 20/40/80/160 MHz, respectively.

Table 18: Measured filter's performance summary for different f_os

Technology (nm)	130			
Area (mm^2)	0.236			
Order-Type	4th-Butterworth			
Topology	Active-RC			
V_{DD} (V)	0.6			
Filter's f_o (MHz)	20	40	80	160
Power (mW)	5.56	10.6	15.64	23.77
Power/BW (mW/MHz)	0.28	0.27	0.20	0.15
Integrated Noise* (μV_{RMS})	243	282	359	520
Intg. Noise/f_o (μV_{RMS}/MHz)	12.15	7.05	4.49	3.25
In-band Frequencies (MHz)	6 + 7	12 + 14	24 + 28	48 + 56
In-band IIP3 (dBm)	+21	+21	+11.3	+9.56
Out-of-band Frequencies (MHz)	30 + 40	60 + 80	120 + 160	240 + 320
Out-of-band IIP3 (dBm)	+17.4	+12	+10.6	+9.7
Dynamic Range+ (dB, @1%THD)	64.2	62.2	59.4	51
Full-Scale Voltage (FSV, % of V_{DD})	60	48.33	47	26.33
SNR (dB) @FSV	60.24	57.23	55.3	46.87
SNDR (dB) @FSV	59.26	55.59	54.4	45.37
SFDR (dB) @FSV	66.55	60.7	61.83	50.71
THD (dB) @FSV	66.17	60.6	61.65	50.7
P_{1dB} (dBm)	6.96	7	6.81	4.26

* Input referred, from 1 Hz to f_o
+ fin = 2/4/8/16 MHz for fo = 20/40/80/160, respectively.

The measured in-band and simulated out-of-band third-order input intercept point (IIP3) results are shown in Fig. 80. Similar to Fig. 79, V_{in} is shown in dBm where the peak-to-peak differential value of V_{in} was used to mathematically convert to dBm as if a 50 Ω impedance was present at V_{in}, even though it was not.

The in-band and out-of-band IIP3 was measured with a two-tone test for all four filter's f_o configurations. The in-band frequencies were 6 and 7 MHz (f_o = 20 MHz), 12 and 14 MHz (f_o = 40 MHz), 24 and 48 MHz (f_o = 80 MHz), and 48 and 56 MHz (f_o = 160 MHz). The measured in-band IIP3 is +21/+21/+11.3/+9.56 dBm for f_o = 20/40/80/160 MHz, respectively. The out-of-band

frequencies were 30 and 40 MHz (f_o = 20 MHz), 60 and 80 MHz (f_o = 40 MHz), 120 and 160 MHz (f_o = 80 MHz), and 240 and 320 MHz (f_o = 160 MHz). The measured out-of-band IIP3 is +17.4/+12/+10.6/+9.7 dBm for f_o = 20/40/80/160 MHz, respectively. Table 19 compares the LV programmable filter against other state-of-the-art LV filter implementations.

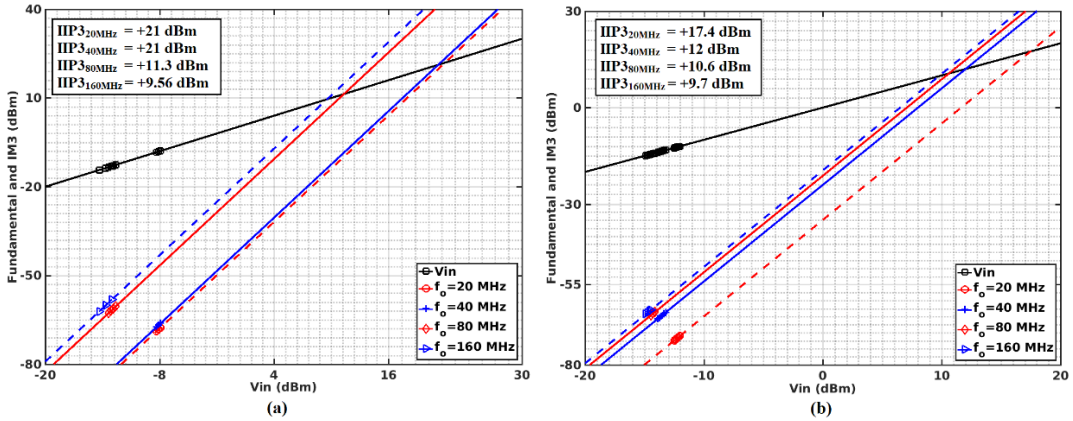


Fig. 80: Two-tone linearity test: (a) In-band and (b) out-of-band IIP3. V_{DD} = 0.6 V and V_{CM} = 0.3 V, in-band frequencies are 6 + 7 MHz (f_o = 20 MHz), 12 + 14 MHz (f_o = 40 MHz), 24 + 48 MHz (f_o = 80 MHz), and 48 + 56 MHz (f_o = 160 MHz), out-of-band frequencies are 30 + 40 MHz (f_o = 20 MHz), 60 + 80 MHz (f_o = 40 MHz), 120 + 160 MHz (f_o = 80 MHz), and 240 + 320 MHz (f_o = 160 MHz).

Table 19: State-of-the-art Low-voltage filter's Performance Comparison

Parameters	**[17]**	**[73]**	**[74]**	**[60]**	**[62]**	**This work**
Technology (nm)	180	180	130	90	65	130
Area (mm^2)	0.230	0.290	0.43	0.29	0.38	0.236
Order-Type	5th-E	5th-C	4th-B	4th-B	4th-B	4th-B
Topology	Active-RC	Active-RC	Active-Gm-RC	RO	PWM	Active-RC

Parameters	[17]	[73]	[74]	[60]	[62]	This work
V_{DD} (V)	0.6	0.5	0.55	0.55	0.6	0.6
Filter's f_o (MHz)	0.135	0.135	11.3	7	70	**160**
Power (mW)	2.6	0.6	3.5	2.9	26.2	23.77
Power/f_o (mW/MHz)	8.15	4.44	0.31	0.41	0.37	**0.15**
Intg. Noise (μV_{RMS})	65^{*}	195.4^{**}	110^{+}	-	365^{++}	520^{++}
Intg. Noise/f_o (μV_{RMS}/MHz)	481.48	1447.40	9.73	-	5.21	**3.25**
In-band Frequencies (MHz)	0.04 + 0.06	0.05 + 0.055	3 + 4	-	-	48 + 56
In-band IIP3 (dBm)	+10	+17	+10	-	-	+9.56
Out-of-band Frequencies (MHz)	0.18 + 0.46	0.2 + 0.35	15 + 19	-	-	240 + 320
Out-of-band IIP3 (dBm)	+18	+27	+13	-	-	+9.7
Dynamic Range# (dB, @1%THD)	57.7	61	60	61	58	51
Full-Scale Voltage (FSV, % of V_{DD})	12	-	25	28	73	26.33
SNR (dB) @FSV	-	-	-	61.4	55.8	46.87
SNDR (dB) @FSV	-	-	40	58	54.4	45.37
SFDR (dB) @FSV	-	53.7	-	67.5	65	50.71
THD (dB) @FSV	40	-	40	60	60	50.7
P_{1dB} (dBm)	-	-	0.5	-	-	**4.26**

* Input referred, integrated from 1 Hz to 150 kHz

** Input referred, integrated from 1 kHz to 1 MHz

\+ Integration limits unspecified

++ Input referred, integrated from 1 Hz to f_o

f_{in} = 100 kHz for [17] and [73], f_{in} = 1 MHz for [74], f_{in} unknown for [60, 62], f_{in} = 2/4/8/16 MHz for f_o = 20/40/80/160, respectively for this work

E – Elliptic, B – Butterworth, C – Chebyshev, FSV – Full-Scale Voltage

The filter's DR is the ratio between the largest and smallest signals that the filter can process. The smallest signal level is limited by noise and the largest is determined by distortion. Usually in filters, the smallest signal level is given by the integrated noise over the filter's BW. However, several different distortion limits are used to determine the largest voltage level. The output voltage level where integrated noise equals the third-order intermodulation product (IM3) from a two-tone test is used in [56]. The output voltage level where integrated noise equals THD is used in [95]. The output voltage level where THD reaches a 0.1 % or 1 % is proposed in [96]. For our purposes, the definition for a 1% THD, or −40 dB, is used to determine the filter's DR. This definition can be mathematically expressed as:

$$\mathrm{DR} = \frac{\mathrm{V_{out,RMS,THD=1\%}}}{\mathrm{V_{N,RMS}}} \tag{135}$$

where $V_{out,RMS,THD=1\%}$ represents the RMS output voltage at a THD = 1 %, and $V_{N,RMS}$ is the RMS output integrated noise.

The filter's FSV was determined to be the peak-to-peak input voltage at the maximum SNDR, similar to how it was reported in [62].

Previously reported filters [17, 60, 73, 74] achieve LV operation but target applications with a f_o lower than 20 MHz. The work presented in [62] achieves a f_o = 70 MHz but with an increased complexity due to the switching nature of the implemented OTAs inside the biquads. The LV OTA presented in [62] achieves a dc gain of 54 dB and a UGF = 450 MHz with an estimated power consumption of 6.55 mW per OTA. The proposed LV OTA achieves a dc gain =

66 dB and UGF = 666 MHz while consuming 3.91 mW per OTA when f_o = 80 MHz. This represents a 40% reduction in power consumption, with increased gain and UGF.

The filter achieves better performance for a comparable f_o, which is due to an improved LV OTA performance compared to the one presented in [62]. The proposed filter also achieves a maximum f_o = 160 MHz, which is the highest among the state-of-the-art LV active-RC filter implementations, and the best linearity and P_{1dB} reported in the literature with significantly less power consumption. Depending on the design constraints, better performance can be obtained if more power consumption is allowed or a more power-efficient design can be achieved, at the expense of linearity and f_o.

5.5 Conclusions

A power-efficient LV FD OTA with high gain and configurable UGF was presented. The LV OTA was used to implement a 4th-order active-RC LPF with f_o programmability and adaptive power consumption.

The filter's f_o can be selected at 20/40/80/160 MHz via a programmable resistor bank, at a V_{DD} = 0.6 V. A binary-weighted capacitor bank is used to adjust for deviations in f_o after fabrication. The filter uses a Tow-Thomas biquad that allows for independent control of f_o and Q. The proposed LV OTA achieves high gain and high UGF by using an enhanced high-gain transistor-level architecture as the main gain stage, and a power-adjustable output stage.

The proposed OTA's frequency response, noise, and mismatch, along with its design in a FD LPF are fully described in this work. The LV active-RC filter achieves the highest f_o, power efficiency, and THD among the state-of-the-art LV active-RC filters present in the literature.

CHAPTER VI

CONCLUSIONS

Trends towards miniaturization in CMOS technologies continue with current designs being developed at 7 nm nodes at the time of this writing, January 2019, with future plans to have 5 nm CMOS nodes. As these processes become more mature and its use more widespread, newer design approaches and transistor-level architectures are going to be required.

This thesis explored two circuits that will most likely still be present and required in future designs. One of them, a capacitor-less (CL) low-dropout (LDO) voltage regulator, is at the interface between the noisy off-chip supply voltage (V_{DD}) and the on-chip V_{DD}. The other, a low-voltage (LV) filter or any other sensitive high-performance signal processing circuit, will use this clean voltage as V_{DD} to perform its intended operation.

CL-LDOs are going to be required to provide stable, clean, and low-noise V_{DD}s to sensitive analog circuits. Some CL-LDOs would find their way into power management integrated circuits (PMICs) to drop the high off-chip voltages into voltages below 1 V for the sensitive on-chip circuitry. This LDOs are going to be preceded by an efficient switching regulator that comes with switching noise. For that reason, these LDOs are going to require high power supply rejection (PSR).

The CL-LDO's load is also going to be a dynamic load, one that powers ON only when required and stays OFF most of the time to save power and increase system's efficiency. This type of load requires a fast settling time (T_S) and small overshoot and undershoot values during load transient events at its supply. Therefore, CL-LDOs with fast T_S and reaction times are going to be needed to meet these requirements.

As a result of all these demands, CL-LDOs have stringent requirements in terms of PSR, T_S, efficiency, overshoot, undershoot, noise, and area. All of these requirements are both application dependent and load dependent; therefore, no two CL-LDOs are alike. Their design requires a deep understanding of the system they are being used, both the supply before them and the load after them set the adequate performance metrics required from that particular CL-LDO for that particular application.

Chapter II and III of this thesis addressed the basic design metrics for CL-LDOs and an approach for fast T_S and high-PSR CL-LDOs, respectively. A CL-LDO with a feedforward V_{DD} noise cancellation technique, adaptive bias and compensation were introduced in chapter III. These techniques allowed for a fast T_S and high PSR CL-LDO that was described, along with design equations, transistor-level implementations, and measured results from a fabricated prototype.

LV high-performance analog systems are going to require novel architectures to maximize the capabilities of the speed small technologies provide, along with the high gain required for closed-loop systems.

A circuit that stands to benefit from these advantages are LV fully-differential (FD) analog filters. Analog filters, closed-loop ones in particular, are often required in systems that demand high linearity, high speeds, configurability, and power-efficiency. These requirements need to be met with the current LV V_{DD}s used in state-of-the-art systems. At the time of this writing, $V_{DD} \leq$ 0.6 V are gaining traction.

The main building block, and often the bottleneck, in closed-loop analog filters are operational transconductance amplifiers (OTAs) or operational amplifiers (OpAmps). These blocks are required to have high gain, high unity-gain frequencies (UGFs), and power efficiency

at LVs. For those reasons, research in novel LV transistor-level OTA or OpAmp architectures that can provide with all those characteristics is going to continue to be an active area of research.

Chapter IV and V of this thesis addressed the state-of-the-art in LV analog filters, and the design of a highly configurable, power-efficient high-UGF LV OTA, respectively. The LV OTA was used to implement a 4th-order active-RC low pass filter (LPF) with cut-off frequency (f_o) programmability and adaptive power consumption. This filter, along with design equations, transistor-level implementations, and measured results from a fabricated prototype is presented in chapter V.

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APPENDIX A

BULK-DRIVEN FEED-FORWARD PSRBW COEFFICIENT DERIVATION*

Derivation of the small-signal model from Fig. 11. KCL is performed at V_{OUT} and V_A

$$V_{OUT}(s) = \frac{V_A(sC_{gd} - g_m) + V_{DD}(g_m + g_{ds} + g_{mb} - Kg_{mb})}{(C_L + C_{gd})s + g_L + g_{ds}} \tag{136}$$

$$V_A(s) = \frac{V_{out}[sC_{gd} + A(s)g_{oA}] + V_{DD}sC_{gs}}{(C_{gs} + C_{gd})s + g_{oA}} \tag{137}$$

Using V_A into V_{OUT}, and assuming a one pole amplifier for A(s) where the pole is given by ω_o, we get

$$V_{OUT}(s) = V_{DD}\left\{\frac{sC_{gs}(sC_{gd} - g_m) + (g_m + g_{ds} + g_{mb} - Kg_{mb})[(C_{gs} + C_{gd})s + g_{oA}]}{[(C_{gs} + C_{gd})s + g_{oA}][(C_L + C_{gd})s + g_L + g_{ds}]}\right\}$$
$$+V_{OUT}\frac{(sC_{gd} - g_m)\left(sC_{gd} + \frac{A_0\omega_o}{s + \omega_o}g_{oA}\right)}{[(C_{gs} + C_{gd})s + g_{oA}][(C_L + C_{gd})s + g_L + g_{ds}]} \tag{138}$$

Solving for V_{OUT} we obtain

$$\mathrm{PSR}(s) \approx \frac{C_{gd}C_{gs}s^3 + \left[(C_{gs}+C_{gd})(\Delta K - g_m) + g_m C_{gd}\right]s^2 + g_{oA}\Delta K s + g_{oA}\omega_o \Delta K}{C_L(C_{gs}+C_{gd})s^3 + \left[(g_{ds}+g_L)(C_{gs}+C_{gd}) + C_{gd}g_m + g_{oA}C_L\right]s^2 + g_{oA}(g_{ds}+g_L)s + A_0 g_m g_{oA}\omega_o} \quad (12)$$

In order to simplify the equation we made the following assumptions

$$\frac{g_m}{C_{gs}} >> \omega_o \quad \frac{g_{oA}}{C_{gs}+C_{gd}} >> \omega_o \quad \frac{g_{oA}}{C_{gd}} >> \omega_o \quad C_{gs}+C_{gd} >> C_{gs}C_{gd} \quad A_0 g_m >> g_{ds}+g_L$$

$$(g_m + g_L)C_{gd} >> g_L C_{gs} \qquad g_{oA}(g_{ds}+g_L) >> (g_m+g_L)C_{gd} \quad (139)$$

$$g_m C_{gd} >> C_L\omega_o(C_{gd}+C_{gs}) + \omega_o C_{gd}C_{gs} \quad (g_m+g_L)C_{gd} >> g_{oA}(C_L - A_0 C_{gd} + C_{gd})$$

PSR_{BW} is maximized when the zero introduced by the technique creates a complex conjugate with the PSR's non-dominant zero. It has been assumed that the dominant zero is due to the CL-LDO's dominant low-frequency pole, as in conventional internally compensated CL-LDOs, and the non-dominant zero is due to M_P's parasitic capacitances. If the dominant PSR zero is ignored, the complex conjugate zeros can be derived by starting with the first term in the right-hand side of (138), the section multiplied by V_{DD} that only includes the zero introduced by the feed-forward circuit and the PSR's non-dominant zero, by solving the quadratic equation arriving at (140) or (141).

$$\omega_{z2,3} \approx -\frac{1}{2}\left(\frac{\Delta K(C_{gs}+C_{gd})}{C_{gs}C_{gd}} - \frac{g_m}{C_{gd}}\right) \pm \frac{1}{2}\sqrt{\left(\frac{\Delta K(C_{gs}+C_{gd})}{C_{gs}C_{gd}} - \frac{g_m}{C_{gd}}\right)^2 - \frac{4g_{oA}\Delta K}{C_{gs}C_{gd}}} \quad (140)$$

$$\omega_{z2,3} \approx -\frac{1}{2}\left(\frac{\Delta K\left(C_{gs}+C_{gd}\right)}{C_{gs}C_{gd}}-\frac{g_m}{C_{gd}}\right)\pm\frac{1}{2}\sqrt{\frac{\Delta K^2\left(C_{gs}+C_{gd}\right)^2+\left(g_m C_{gs}\right)^2}{\left(C_{gs}C_{gd}\right)^2}-\frac{4\Delta K}{C_{gs}C_{gd}}\left[g_{oA}+\frac{gm}{2}\left(1+\frac{C_{gs}}{C_{gd}}\right)\right]} \quad (141)$$

The PSR zeros are imaginary if

$$\Delta K^2\left(C_{gs}+C_{gd}\right)^2+\left(g_m C_{gs}\right)^2 < 4\Delta K C_{gs}\left[g_{oA}C_{gd}+\frac{gm}{2}\left(C_{gd}+C_{gs}\right)\right] \quad (142)$$

and the maxima, which increases the PSR_{BW}, is obtained at the point where

$$\Delta K_{BW} = g_m + g_{ds} + g_{mb} - K g_{mb} \quad (143)$$

$$\Delta K_{BW} = \frac{2C_{gs}C_{gd}g_{oA}}{\left(C_{gs}+C_{gd}\right)^2}+\frac{g_m C_{gs}}{C_{gs}+C_{gd}} \quad (144)$$

Then using (143) into (144) and solving for K, we obtain (19), repeated below for convenience, which can also be expressed as in (145).

$$K_{BW} = 1+\frac{1}{\chi}+\frac{1}{\chi A_{PT}}-\frac{2C_{gs}C_{gd}g_{oA}}{g_{mb}\left(C_{gs}+C_{gd}\right)^2}-\frac{C_{gs}}{\chi\left(C_{gs}+C_{gd}\right)} \quad (19)$$

$$K_{BW} = 1+\frac{g_m+g_{ds}}{g_{mb}}-\frac{2C_{gs}C_{gd}g_{oA}}{g_{mb}\left(C_{gs}+C_{gd}\right)^2}-\frac{g_m C_{gs}}{g_{mb}\left(C_{gs}+C_{gd}\right)} \quad (145)$$

APPENDIX B

FILTER'S LOW-FREQUENCY NOISE DENSITY

Only low-frequency noise will be considered in this section. In order to analyze the filter's low-frequency noise spectral density, the single-ended biquad was used as shown in Fig. 81. The inversion around the loop is only to maintain negative feedback and is ignored for noise purposes since a fully differential (FD) filter was implemented. The following assumptions were made: 1) All OTAs in Fig. 81 are the same, and 2) the filter's gain is 0 dB or 1 V/V.

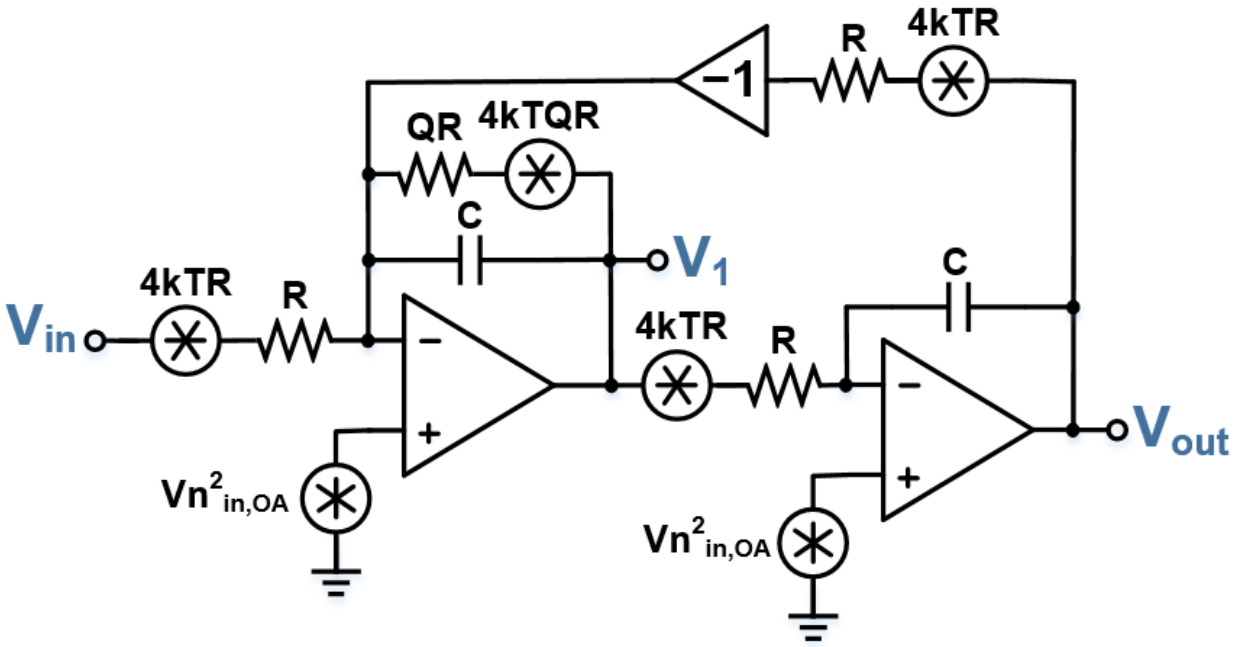

Fig. 81: Simplified biquad for noise analysis purposes

Superposition is used to obtain each individual noise contribution at the biquad's output. Because the gain was assumed to be 1 V/V, low-frequency input and output referred noise can be considered almost equal. The noise from the input and output connected resistors goes to the output unchanged. The intermediate and Q resistor's noise is referred to the output by multiplying it by the square of the transfer function from V_1 to V_{out}, which is 1/Q. Eq. (146) shows the output noise due to the resistors for the biquad shown in Fig. 81.

$$v_{n,out,R}^2 = 4\mathrm{kTR}\left[2+\left(\frac{1}{\mathrm{Q}}\right)^2\left(1+\mathrm{Q}\right)\right] \tag{146}$$

The FD biquad has twice the number of resistors; therefore, twice the amount of noise occurs. By adding the noise due to the second biquad, with a $Q = Q_2$, we can obtain (147) after some simplification.

$$v_{n,out,R}^2 = 8\mathrm{kTR}\left(4+\frac{1}{\mathrm{Q}_1}+\frac{1}{\mathrm{Q}_2}+\frac{1}{\mathrm{Q}_1^2}+\frac{1}{\mathrm{Q}_2^2}\right) \tag{147}$$

The noise transfer function from the lossy integrator to the output is given by:

$$v_{n,out,lossy}^2 = v_{n,in,OA}^2\left(2+\frac{1}{\mathrm{Q}}\right)^2 \tag{148}$$

The noise transfer function from the lossless integrator to the output is given by:

$$v_{n,out,lossless}^2 = v_{n,in,OA}^2 \left(\frac{1}{Q} \right)^2 \tag{149}$$

Considering the two biquads with different Qs, the total noise from the OTAs is given by:

$$v_{n,out,actives}^2 = v_{n,in,OA}^2 \left[\left(2 + \frac{1}{Q_1} \right)^2 + \left(\frac{1}{Q_1} \right)^2 + \left(2 + \frac{1}{Q_2} \right)^2 + \left(\frac{1}{Q_2} \right)^2 \right] \tag{150}$$

By combining (147) and (150), the total low-frequency output noise spectral density for the 4th-order Tow-Thomas is given by (112), which is repeated below for convenience.

$$v_{n,out}^2 = 2 \left[\left(4 + \frac{1}{Q_1} + \frac{1}{Q_2} + \frac{1}{Q_1^2} + \frac{1}{Q_2^2} \right) \left(4kTR_o + v_{n,in,OA}^2 \right) + v_{n,in,OA}^2 \left(\frac{1}{Q_1} + \frac{1}{Q_2} \right) \right] \tag{112}$$

APPENDIX C

OTA'S OUTPUT AND INPUT-REFERRED NOISE CALCULATIONS

The proposed OTA's output and input-referred noise are analyzed in this appendix. First, the following assumptions have been made: 1) G_{MB}'s noise has been neglected, since when input-referred, they are divided by G_{MA}'s gain and become less significant compared to G_{MA}'s noise; 2) The noise contribution from bias transistors and CM circuits, with the exception of CM resistors, has been neglected. In FD implementations those noise sources are CM signals and will produce no differential output [42]. Fig. 82 shows G_{MA}'s simplified transistor-level schematic used for noise analysis purposes.

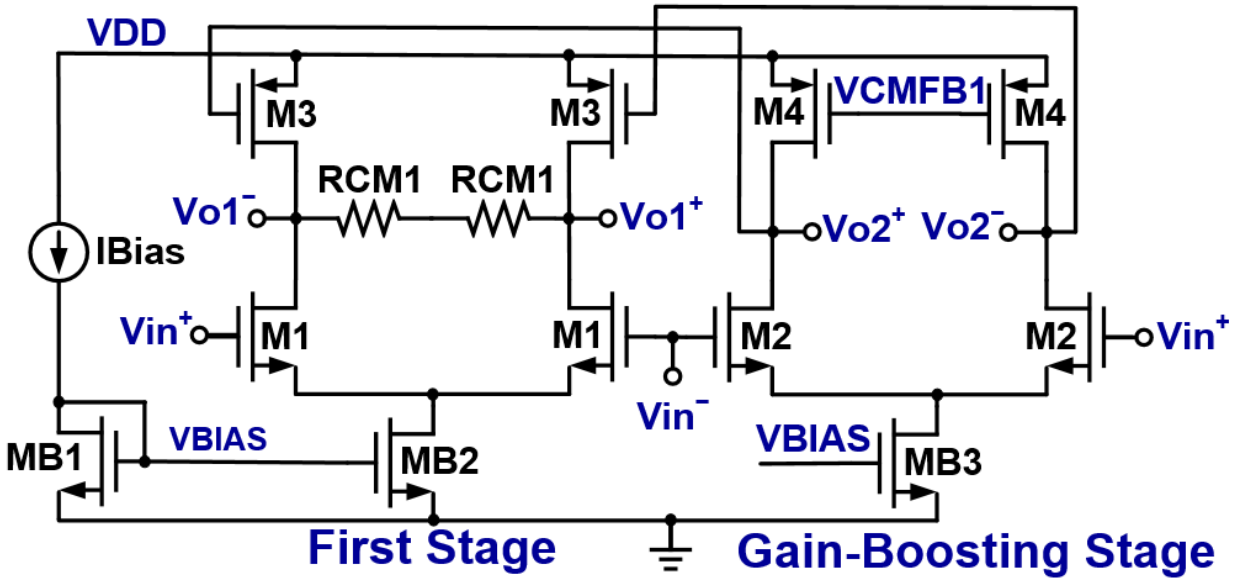

Fig. 82: G_{MA}'s simplified transistor-level schematic for noise analysis purposes

The differential output noise due to G_{MA} is given by:

$$v_{n,out}^2 = i_{n,out,GMA}^2 R_{out,GMA}^2 \tag{151}$$

where:

$$i_{\mathrm{n,out,GMA}}{}^2 = 8\mathrm{kT}\left[\gamma\left(\mathrm{g_{m1}}+\mathrm{g_{m3}}\right)+\gamma\left(\frac{\mathrm{g_{m3}}}{\mathrm{g_{o1}}+\mathrm{g_{o3}}+\mathrm{g_{CM1}}}\right)^2\left(\mathrm{g_{m2}}+\mathrm{g_{m4}}\right)+\frac{1}{\mathrm{R_{CM1}}}\right] \tag{152}$$

and:

$$R_{\mathrm{out,GMA}}{}^2 = \left(\frac{1}{\mathrm{g_{o1}}+\mathrm{g_{o3}}+\mathrm{g_{CM1}}}\right)^2 \tag{153}$$

Using (152) and (153) into (151), we obtain:

$$v_{\mathrm{n,out}}{}^2 = 8\mathrm{kT}\left[\gamma\left(\mathrm{g_{m1}}+\mathrm{g_{m3}}\right)+\gamma\left(\frac{\mathrm{g_{m3}}}{\mathrm{g_{o1}}+\mathrm{g_{o3}}+\mathrm{g_{CM1}}}\right)^2\left(\mathrm{g_{m2}}+\mathrm{g_{m4}}\right)+\frac{1}{\mathrm{R_{CM1}}}\right]\left(\frac{1}{\mathrm{g_{o1}}+\mathrm{g_{o3}}+\mathrm{g_{CM1}}}\right)^2 \tag{154}$$

where if we assume that:

$$1 << \frac{g_{m3}}{g_{o1}+g_{o3}+g_{CM1}} \tag{155}$$

then (154) can be simplified to (120), repeated below for convenience.

$$\upsilon_{n,out}{}^2 \approx 8kT\gamma\left(g_{m2}+g_{m4}\right)\frac{g_{m3}{}^2}{\left(g_{o1}+g_{o3}+g_{CM1}\right)^4} \tag{120}$$

The differential input-referred noise due to G_{MA} is given by:

$$v_{n,in}^2 = \frac{i_{n,out,GMA}^2}{G_{MA}{}^2} \tag{156}$$

where:

$$G_{MA} = g_{m1} + \frac{g_{m2}g_{m3}}{g_{o2}+g_{o4}} \tag{157}$$

Using (152) and (157) into (156), we obtain:

$$v_{n,in}^{\ 2} = \frac{8kT\left[\gamma\left(g_{m1}+g_{m3}\right)+\gamma\left(\frac{g_{m3}}{g_{o1}+g_{o3}+g_{CM1}}\right)^2\left(g_{m2}+g_{m4}\right)+\frac{1}{R_{CM1}}\right]}{\left(g_{m1}+\frac{g_{m2}g_{m3}}{g_{o2}+g_{o4}}\right)^2} \tag{158}$$

where if we assume that:

$$1 << \frac{g_{m3}}{g_{o1}+g_{o3}+g_{CM1}} \qquad\qquad g_{m1} << \frac{g_{m2}g_{m3}}{g_{o2}+g_{o4}} \tag{159}$$

then (158) can be simplified to:

$$v_{n,in}^{\ 2} \approx \frac{8kT\gamma\left[\left(\frac{g_{m3}}{g_{o1}+g_{o3}+g_{CM1}}\right)^2\left(g_{m2}+g_{m4}\right)\right]}{\left(\frac{g_{m2}g_{m3}}{g_{o2}+g_{o4}}\right)^2} \tag{160}$$

After rearranging the terms we can obtain (121), repeated below for convenience.

$$\upsilon_{n,in}^{\ 2} \approx 8kT\gamma\left(g_{m2}+g_{m4}\right)\left(\frac{g_{o2}+g_{o4}}{g_{m2}}\right)^2\left(\frac{1}{g_{o1}+g_{o3}+g_{CM1}}\right)^2 \tag{121}$$

APPENDIX D

OFFSET AND MISMATCH CALCULATIONS

To calculate the differential offset, it was assumed that all devices follow the square-law model with channel-length modulation effects ignored. A procedure similar to the one used in [89] was followed. The current mismatch between two matched transistors can be expressed as:

$$\Delta I^2 = g_m{}^2 \left\{ \Delta V_T{}^2 + \Delta V_{GS}{}^2 + \left(\frac{V_{GS} - V_T}{2} \right)^2 \left[\frac{\left(\Delta \frac{W}{L} \right)}{\frac{W}{L}} \right]^2 \right\} \tag{161}$$

where squared terms $\Delta V_T{}^2$, $\Delta V_{GS}{}^2$, and $[(\Delta W/L)/W/L]^2$ represent standard deviations. Using (161), the output current mismatch due to the main stage (by only considering M_1 and M_3 in Fig. 67 at the moment) can be expressed as:

$$\Delta I_1{}^2 = g_{m1}{}^2 \left\{ \Delta V_{TN1}{}^2 + \left(\frac{V_{GS1} - V_{TN}}{2} \right)^2 \left[\frac{\left(\Delta \frac{W}{L_1} \right)}{\frac{W}{L_1}} \right]^2 \right\} + g_{m3}{}^2 \left\{ \Delta V_{TP3}{}^2 + \Delta V_{GS3}{}^2 + \left(\frac{V_{GS3} - V_{TP}}{2} \right)^2 \left[\frac{\left(\Delta \frac{W}{L_3} \right)}{\frac{W}{L_3}} \right]^2 \right\} \tag{162}$$

where ΔV_{GS1} is zero and ΔV_{GS3} comes from the V_{GS} mismatch generated at M_3's gate due to mismatch in the gain-boosting stage. This $\Delta V_{GS3}{}^2$ can be expressed as:

$$\Delta V_{GS3}{}^2 = \left(\frac{\Delta I_2}{g_{m2}}\right)^2 \left|A_{Boost}\right|^2 \tag{163}$$

where ΔI_2 is the current mismatch in the gain-boosting stage alone, which is given by:

$$\Delta I_2{}^2 = g_{m2}{}^2 \left\{ \Delta V_{TN2}{}^2 + \left(\frac{V_{GS2} - V_{TN}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_2}\right)}{\frac{W}{L_2}}\right]^2 \right\} + g_{m4}{}^2 \left\{ \Delta V_{TP4}{}^2 + \left(\frac{V_{GS4} - V_{TP}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_4}\right)}{\frac{W}{L_4}}\right]^2 \right\} \tag{164}$$

Combining (163) and (164) with (162), dividing it by G_{MA}, and after some rearrangement the input referred offset can be obtained as follows:

$$\begin{aligned} \Delta V_{OS,in}{}^2 = {} & \left(\frac{g_{m1}}{G_{MA}}\right)^2 \left\{ \Delta V_{TN1}{}^2 + \left(\frac{V_{GS1} - V_{TN}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_1}\right)}{\frac{W}{L_1}}\right]^2 \right\} + \left(\frac{g_{m3}}{G_{MA}}\right)^2 \left\{ \Delta V_{TP3}{}^2 + \left(\frac{V_{GS3} - V_{TP}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_3}\right)}{\frac{W}{L_3}}\right]^2 \right\} \\ & + \left(\frac{g_{m3}}{G_{MA}}\left|A_{Boost}\right|\right)^2 \left\{ \Delta V_{TN2}{}^2 + \left(\frac{V_{GS2} - V_{TN}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_2}\right)}{\frac{W}{L_2}}\right]^2 + \left(\frac{g_{m4}}{g_{m2}}\right)^2 \Delta V_{TP4}{}^2 + \left(\frac{I_{D2}}{g_{m2}}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_4}\right)}{\frac{W}{L_4}}\right]^2 \right\} \end{aligned} \tag{165}$$

Assuming $A_{Boost} > 1$, $g_{m4}/g_{m2} < 1$ and $I_{D2}/g_{m2} < 1$, (165) can be simplified to obtain (122), which is repeated below for convenience.

$$\Delta V_{OS,in}{}^2 \approx \left(\frac{g_{m1}}{G_{MA}}\right)^2 \left\{ \Delta V_{TN1}{}^2 + \left(\frac{V_{GS1} - V_{TN}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_1}\right)}{\frac{W}{L_1}}\right]^2 \right\} + \left(\frac{g_{m3}}{G_{MA}}|A_{Boost}|\right)^2 \left\{ \Delta V_{TN2}{}^2 + \left(\frac{V_{GS2} - V_{TN}}{2}\right)^2 \left[\frac{\left(\Delta \frac{W}{L_2}\right)}{\frac{W}{L_2}}\right]^2 \right\} \quad (122)$$

APPENDIX E

OTA'S UGF APPROXIMATION

This appendix discusses the approach used to calculate the OTA's UGF. In general, this approach can be used for systems with a complex transfer function, i.e. multiple poles and zeros. The transfer function given by (123), repeated below for convenience, is used as a starting point.

$$\frac{V_O(s)}{V_{in}(s)} = \frac{A_0\left(1+\frac{s}{\omega_{z1,GMA}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2,GMA}}\right)\left(1+\frac{s}{\omega_{p3}}\right)\left(1+\frac{s}{\omega_{p4}}\right)} \tag{123}$$

Given (123), the gain across the frequency range can be expressed as:

$$\begin{aligned} 20\log\left[\frac{V_o(j\omega)}{V_{in}(j\omega)}\right] = {} & 20\log(A_0) - 20\log\left(\frac{\omega}{\omega_{p1}}\right) - 20\log\left(\frac{\omega}{\omega_{p2,GMA}}\right) - 20\log\left(\frac{\omega}{\omega_{p3}}\right) \\ & -20\log\left(\frac{\omega}{\omega_{p4}}\right) + 20\log\left(\frac{\omega}{\omega_{z1,GMA}}\right) + 20\log\left(\frac{\omega}{\omega_{z2}}\right) \end{aligned} \tag{166}$$

which comes from the graphical approach to plot a transfer function. By combining all the left-side logarithms, (166) can be simplified to:

$$20\log\left[\frac{V_o(j\omega)}{V_{in}(j\omega)}\right]=20\log\left(\frac{A_0\omega_{p1}\omega_{p2,GMA}\omega_{p3}\omega_{p4}}{\omega_{z1,GMA}\omega_{z2}\omega^2}\right) \quad (167)$$

By removing the logarithm from both sides and knowing that the UGF is the frequency at which the magnitude of $V_o(j\omega)/V_{in}(j\omega)$ is one we get:

$$1=\frac{A_0\omega_{p1}\omega_{p2,GMA}\omega_{p3}\omega_{p4}}{\omega_{z1,GMA}\omega_{z2}\omega_{UGF}^2} \quad (168)$$

Then solving for ω_{UGF} we get (125), repeated below for convenience.

$$\omega_{UGF}=\sqrt{\frac{A_0\omega_{p1}\omega_{p2,GMA}\omega_{p3}\omega_{p4}}{\omega_{z1,GMA}\omega_{z2}}} \quad (125)$$