POWER MANAGEMENT ICS FOR INTERNET OF THINGS, ENERGY HARVESTING AND BIOMEDICAL DEVICES

A Dissertation

by

XIAOSEN LIU

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Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	Prasad Enjeti
	Kamran Entesari
	Alexander G. Parlos
Head of Department,	Miroslav M. Begovic

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ABSTRACT

This dissertation focuses on the power management unit (PMU) and integrated circuits (ICs) for the internet of things (IoT), energy harvesting and biomedical devices. Three monolithic power harvesting methods are studied for different challenges of smart nodes of IoT networks. Firstly, we propose that an impedance tuning approach is implemented with a capacitor value modulation to eliminate the quiescent power consumption. Secondly, we develop a hill-climbing MPPT mechanism that reuses and processes the information of the hysteresis controller in the time-domain and is free of power hungry analog circuits. Furthermore, the typical power-performance tradeoff of the hysteresis controller is solved by a self-triggered one-shot mechanism. Thus, the output regulation achieves high-performance and yet low-power operations as low as 12 μW. Thirdly, we introduce a reconfigurable charge pump to provide the hybrid conversion ratios (CRs) as 1⅓× up to 8× for minimizing the charge redistribution loss. The reconfigurable feature also dynamically tunes to maximum power point tracking (MPPT) with the frequency modulation, resulting in a two-dimensional MPPT. Therefore, the voltage conversion efficiency (VCE) and the power conversion efficiency (PCE) are enhanced and flattened across a wide harvesting range as 0.45 to 3 V. In a conclusion, we successfully develop an energy harvesting method for the IoT smart nodes with lower cost, smaller size, higher conversion efficiency, and better applicability.

For the biomedical devices, this dissertation presents a novel cost-effective automatic resonance tracking method with maximum power transfer (MPT) for piezoelectric transducers (PT). The proposed tracking method is based on a band-pass filter (BPF) oscillator, exploiting the PT's intrinsic resonance point through a sensing bridge. It guarantees automatic resonance tracking and maximum electrical power converted into mechanical motion regardless of process variations and environmental interferences. Thus, the proposed BPF oscillator-based scheme was designed for an ultrasonic vessel sealing and dissecting (UVSD) system. The sealing and dissecting functions were verified experimentally in chicken tissue and glycerin. Furthermore, a combined sensing scheme circuit allows multiple surgical tissue debulking, vessel sealer and dissector (VSD) technologies to operate from the same sensing scheme board. Its advantage is that a single driver controller could be used for both systems simplifying the complexity and design cost. In a conclusion, we successfully develop an ultrasonic scalpel to replace the other electrosurgical counterparts and the conventional scalpels with lower cost and better functionality.

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NOMENCLATURE

BPF	Band-pass Filter
CP	Charge Pump
CR	Conversion Ratio
CLK	Clock
EH	Energy Harvesting
FSL	Fast Switching Limit
IC	Integrated Circuit
MFB	Multiple Feedback
PFM	Pulse-frequency Modulation
PMU	Power Management Unit
PT	Piezoelectric Transducer
PWM	Pulse-width Modulation
RF	Radio Frequency
SMPC	Switched Mode Power Converter
SSL	Slow Switching Limit
VCE	Voltage Conversion Efficiency
PCE	Power Conversion Efficiency
UVSD	Ultrasonic Vessel Sealing and Dissecting

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1 INTRODUCTION

1.1 Internet of Things and the Hardware Bottleneck

With recent developments in the Microelectromechanical Systems (MEMS) sensors and scaling-down of the silicon fabrication technology, the Internet of Things (IoT) has been proposed to uniquely identify objects and their virtual representations in an Internet-like structure [1]. Under such configuration, every object within the network can be tagged, analyzed, and managed to compose the event-driven mechanism of an IoT system [2]. As a leading topology and specific implementation of IoT, a Wireless Sensor Network (WSN) has been created to monitor, communicate, and process environmental information [3], [4]. In the WSN, the distributed sensors, also called smart nodes, should be integrated with SOC and wireless transceivers. The main practical challenge is how to power multiple electronic devices. Based on the self-sustaining operation scenario, the smart node is attached to objects without a power or signal wire connection. Since the occupied area of the harvesting system should also be minimized for monolithic integration, the available environmental energy is stringently limited, mandating the harvesting system to be highly energy-efficient. Another design challenge is the fact that the energy resource changes its power density depending on different environmental variables such as illumination intensity and temperature [5]. Thus, it requires the harvesting system to be adaptive to those environmental variations to achieve maximum power transfer.

Currently, radio-frequency (RF) electromagnetic waves are utilized to power radio-frequency identification devices (RFID) [6]-[8]. However, RFID acts as a passive transponder to the WSN only when RF power resides within a certain frequency range. Thus, the operation of a distributed smart node is not event-driven but scanned by an RF reader, resulting in passively monitoring. Trying to solve this issue, researchers have proposed a Battery Assisted Passive (BAP) RFID, which can actively transmit its sensed information using a small rechargeable on-board battery [9]. However, the reliability, size, and life-span of the on-board batteries are not satisfying and limit the development of the IoT [2].

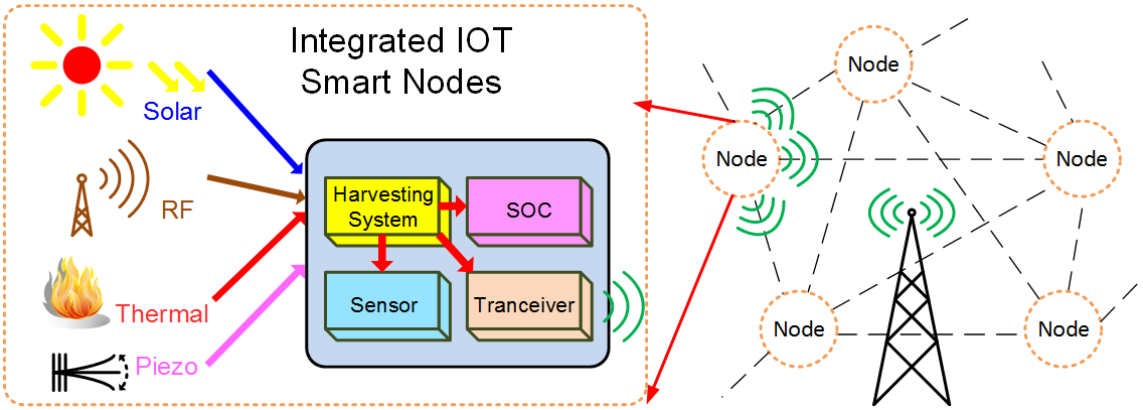


Figure 1. Conceptual block diagram of the IoT smart nodes with energy harvesting technique.

The IoT can be implemented by tagging objects as shown in Figure 1. The main difference from the conventional passive tag is that an IoT smart node includes a small size energy harvester, supercapacitor/battery, SOC, wireless transceiver, and sensor. The small energy sources embedded in the smart node, such as solar cells, RF, thermoelectric generators, and piezoelectric generators, can be a more flexible, robust, and efficient

power supply. Thus, the distributed nodes of Wireless Sensor Network can actively sense and exchange information with each other by low power communication technologies such as ZigBee or Bluetooth. The WSN can be widely applied in various applications, such as smart electrical grids, logistic flows, military or security wireless guards, and natural disaster sensor networks for forest fires, tsunamis, or earthquakes [3].

1.2 Characteristics of Energy Sources

1.2.1 Photovoltaic Cell

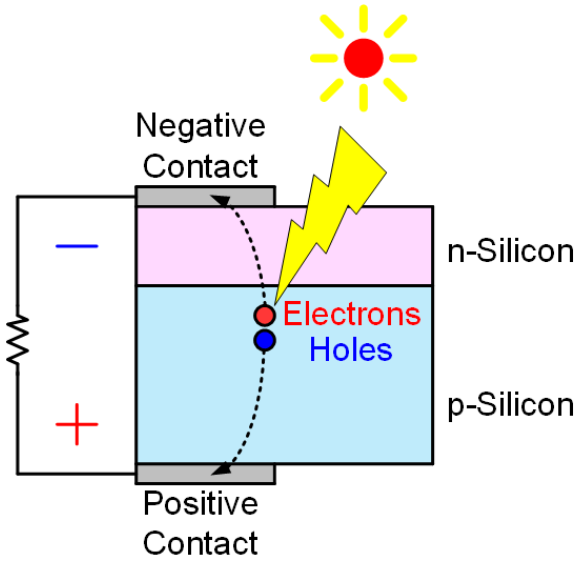


Figure 2. The physical structure of PV cells and their operating mechanism.

The photovoltaic effect is the generation of voltage or current in a material upon exposure to light. In principle, the photon excites the electrons in the valence band jumping to the conduction band as the free electrons with energy. Such a phenomenon

was firstly discovered by French physicist Alexandre-Edmond Becquerel in 1839. However, the applicable photovoltaic (PV) cell, also called solar cell, was initially proposed for powering the space satellites in later 1950s [10]. As shown in Figure 2, the fundamental mechanism is using the photon to excite a pair of electrons and protons in the vicinity of p-n-junction. The resulting electrons and protons will travel through the n-type and p-type materials to the electrodes respectively and this electricity is captured [11]. Therefore, the electrical behavior of PV cell could be modeled with current source, diode and passive components as illustrated in Figure 3 [12].

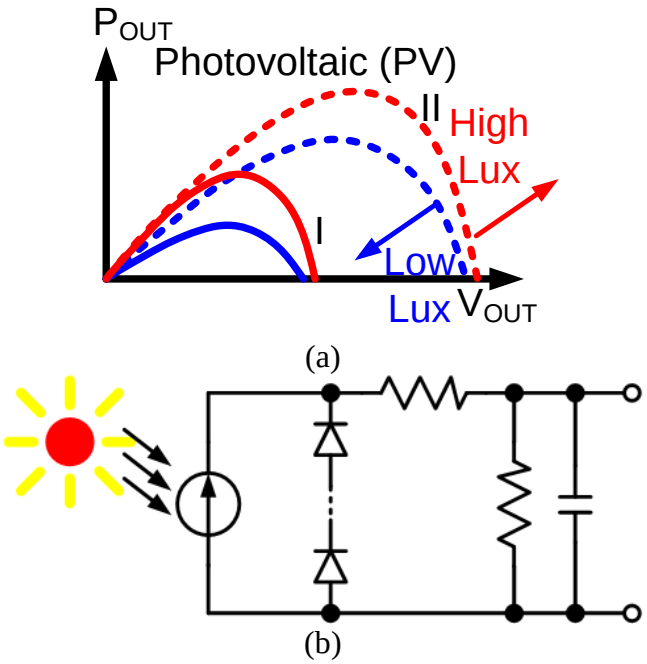


Figure 3. (a) The electrical characteristics of PV cells, and (b) the equivalent model.

With the advancement of semiconductor technology, nowadays PV cells have larger size and output power, and feasible for energy harvesting purposes. According to different fabrication technologies, the common PV cells in the nowadays market can be

categorized by crystalline silicon and thin film [13]. Their pros and cons are compared in Table 1. The crystalline silicon technology is similar with the conventional MOS technology and fabricates the PV cells as upon mono- or poly-silicon wafers. Its main advantage is premium quality and efficiency as high as 20% [14]. The energy conversion efficiency here is defined as the ratio between output electrical power and income light power. The disadvantage is the relatively expensive cost and limited physical size. Thus, less expensive substrate such as thin film technology was invented to conquer the cost and size problems. Basically, this technology fabricates the PV cells by depositing a thin semiconductor film upon glass or plastic substrates [15]. Due to the chemical vapor deposition (CVD) way of material deposition, the film is typically in the amorphous structure with worse quality compared with crystalline structure. Such an inferior characteristic cause a degenerated efficiency typically less than 15% [5], [16]. Also, the less expensive thin-film technology suffers a relatively short life-span and reliability issue [17], [18].

Table 1. Comparison table of crystalline and thin film PV cells.

PV type	Fabrication	Efficiency	Cost	Longevity & Reliability	Cell Size
Crystalline	Mono-Si	Very High	High	High	Small
	Poly-Si	High	Medium	High	Small
Thin-film	a-Si, CdTe, CIGS, DSC, flexible organic	Low	Low	Low	Large

1.2.2 Thermoelectric Generator

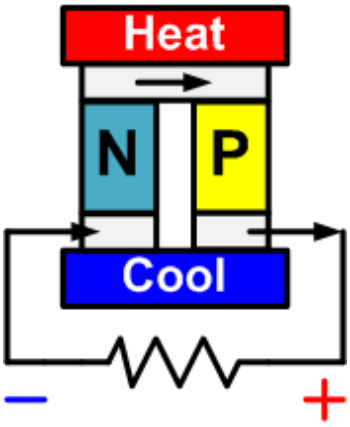


Figure 4. Physical structure of thermoelectric generators.

The thermoelectric generator (TEG) is another way of generating electricity. The physic principle is that the charge carriers, electrons and holes, will diffuse from the hot side to the cold side. Simultaneously, such massive moving generates current and electric power. To maximize the power generation capability, both electron and hole material are used as Figure 4 and called thermopile [19]. The relationship between heat and electricity was firstly identified by German Physicist Thomas Johann Seebeck [20]. It was later named Peltier-Seebeck effect and emphasized that such heat-electricity conversion is thermodynamically reversible. The energy accumulation, $\dot{e}$, could be fully defined by a thermoelectric equation as (1),

$$\dot{e} = \nabla \cdot (\kappa \nabla T) - \nabla \cdot (V + \Pi)\vec{J} + \dot{q}_{ext} \quad (1)$$

where κ is the thermal conductivity, Π is the Peltier coefficient, V is the local voltage, $\vec{J}$ is the local current density, and q_{ext} is the added heat from any external source. The second term of this equation represents the energy carried by currents.

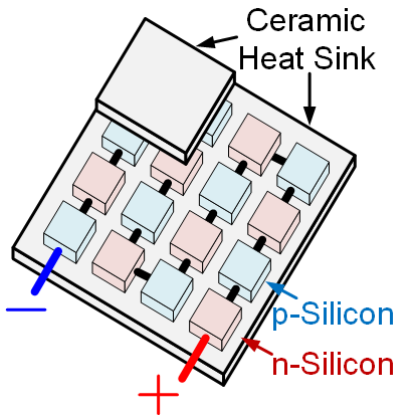
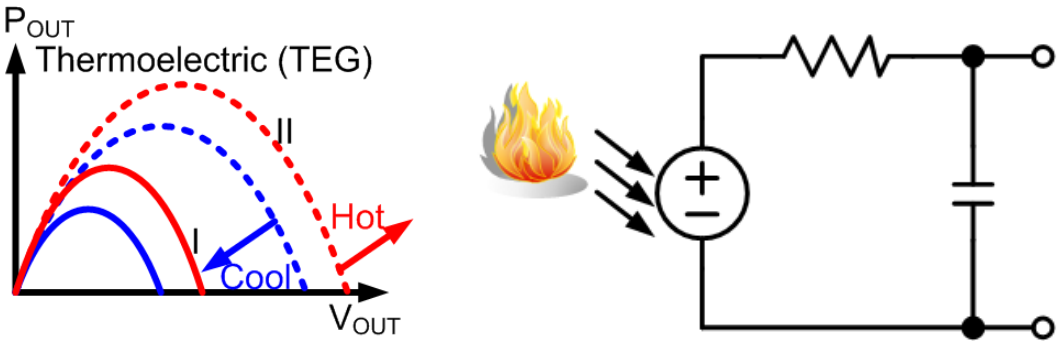


Figure 5. Architecture of commercial TEG products.

The typical structure of commercial TEG is demonstrated in Figure 5 [22]. Due to large temperature gradient is difficult to maintain, the thermovoltage of a single thermopile is typically lower than 1 mV in most applications. Therefore, tens or hundreds of thermopiles are cascaded as Figure 5 [23]. The top and bottom sides are fabricated by ceramic cases and function as the cold and hot faces.



(a) (b)

Figure 6. (a) Electrical model and (b) transfer curves of generic TEGs.

The electrical model and transfer curves of generic TEGs are demonstrated in Figure 6. Table 2 lists typical performances of TEG for energy harvesting purposes [24]. There are two rules of thumb for choosing the proper TEG for energy harvesting

purposes. Firstly, different from PV cells in Figure 3, the TEG shows linear resistance which is proportional to the temperature gradient. It implies that the maximum output point is simply the half of the open circuit voltage (OCV), and the resulting MPPT scheme can be as simple as sensing the OCV. Secondly, to achieve harvestable voltage, the more cascaded thermopiles the easier for the following boost converter. However, the increasing series resistance will compromise the available output power quadratically. The commercial products typically are given specifications for the thermal management application instead of energy harvesting purposes. The V_{max} and I_{max} are the maximum operating conditions when using the TEG as a Peltier cooler. Therefore, a good rule of thumb for selecting the right TEG is to choose the largest product of $V_{max} \times I_{max}$ for a specific size [23].

Table 2. Performance comparison of various TEGs.

Manufacturer ID	I_{max} (A)	V_{max} (V)	Q_{max} (Watts)	No. of Series Piles	L×W Size (mm)
HT9,3,F2,2525,TA,W6	9.6	3.6	20	N/A	29×25
HT6,12,F2,4040,TA,W6	6	14.4	51	127	44×40
HT8,12,F2,4040,TA,W6	8.5	14.4	72	127	44×40
HT4,6,F2,2143,TA,W6	3.7	7.2	16	63	43×21
HT2,12,F2,3030,TA,W6	2.3	14.4	20	N/A	34×30

1.2.3 Piezoelectric Transducer

The mechanic energy is one of the most universal form of energy, and is conventionally converted into electricity by generators [25]. Their bulky sizes are not feasible for the compact energy harvesting purposes. Therefore, as a solid-state way of harvesting, the piezoelectric transducer (PT) is much smaller and ideal for this application. Its principle, called piezoelectricity, is intrinsic characteristics of crystal. This phenomena was firstly identified by French physicists Jacques and Pierre Curie in 1880 [26]. One simple explanation is that every crystal material can be modeled as a massive combination of electric dipole [27]. In steady state, the material shows neutral charge. Once applying external stress, the dipole moment will be changed and generates uneven electrical field as,

$$\vec{D} = \sigma\vec{T} + \varepsilon\vec{E} \tag{2}$$

where $\vec{D}$ is electric charge density displacement, σ is coefficient of the piezoelectric effect, $\vec{T}$ is stress, ε is permittivity, and $\vec{E}$ is the electrical field strength. Typically, the applied stress $\vec{T}$ is limited by the physic capability of crystal and is always in the form of vibration. Thus, the generated electrical field, harvested voltage and current are in AC form. This is the major difference between PT and other DC energy sources as PV and TEG. Note that the piezoelectricity is also a reversible procedure. As a mechanic actuator, it widely used in nowadays MEMS and mobile devices [28]-[30]. One biomedical application will be introduced in Section 5.

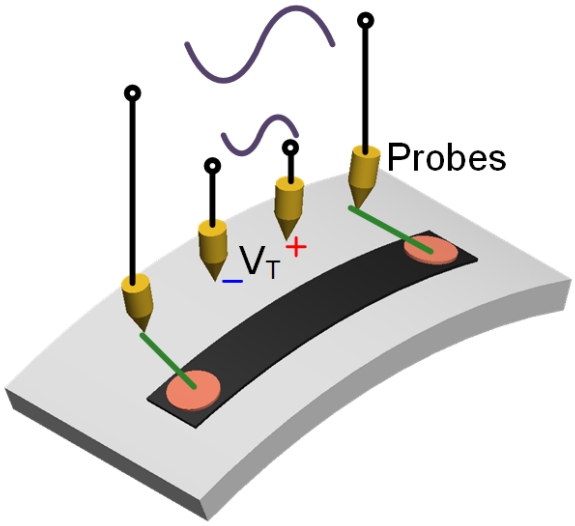


Figure 7. Structure of common piezoelectric transducers.

Table 3. Performance comparison of various piezoelectric transducers tested at 60Hz frequency and 1G acceleration amplitude.

Manufacturer ID	RMS Power (mW)	RMS Voltage (V)	Resistance (kΩ)	RMS OC Voltage (V)	Peak to Peak Displacement (mm)	L×W Size (mm)
PPA-1001	1.8	7.1	28.6	12.2	3.9	54.4×22.4
PPA-1011	3.2	7.9	19.5	13.8	7.0	71×25.4
PPA-1021	1.6	14.0	125.1	20.5	5.4	71×10.3
PPA-2011	4.3	7.9	14.7	14.8	4.3	71×25.4
PPA-4011	19.5	10.2	5.4	20.2	2.4	71×25.4

Although monocrystalline PT has stronger piezoelectric effect, its fabrication is difficult due to the high processing temperature. Therefore, low cost polycrystalline PT are more favorable for IoT energy harvesting [31]. A generic structure of commercial

PTs are illustrated in Figure 7. Various kinds of PTs and their characteristics are listed in Table 3. Due to the relative low frequency of mechanic vibration, the harvested power is below 10 μW.

1.2.4 Radio Frequency Electromagnetic Wave

Radio frequency wireless communication is used in billions of transmitters worldwide, such as cell phones, radio, television, and emerging IoT mobile devices. Similar to transmit signals, the RF electromagnetic wave can be harvested by a system as Figure 8. The collecting components are antenna. It needs to be carefully designed to optimize the receiving magnitude of RF signal. The second part is the RF-to-DC power converter, which is a combination of high speed full-wave rectifier and boost converter [32]. Two critical issues are the impedance matching between antenna and rectifier, and the conversion efficiency of the boost converter. The power conditioning module handles the harvested energy and regulates it for specific load requirements.

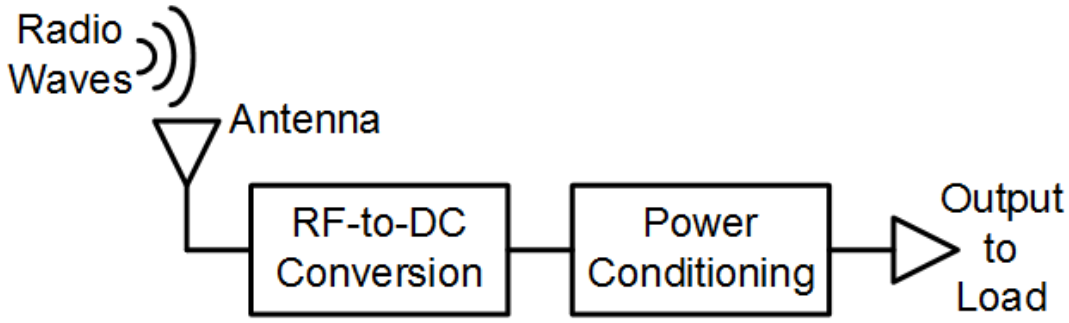


Figure 8. Block diagram of a RF energy harvester.

The main advantage of RF energy is its pervasive nature. The aforementioned energy sources highly depend on spacing and intermediary material. For example, the

PV energy is very sensitive to shading conditions [33]. The TEG depends on not only heat generation, but also the path of heat sinking [34]. The PT requires continuous mechanic motion, which is difficult to be guaranteed in practical application [35]. As a comparison, the RF wave is less sensitive to the environment changing such like cloud and rainy days. Another advantage is the RF energy harvesting does not require dynamic MPPT as PV or TEG [36], which is done by designing a fixed shape antenna with a good receiving efficiency. The disadvantage of RF energy harvesting is its relative smaller magnitude, which drastically decay with respect to the square of distance. For example, a local 5kW AM radio station can only deliver hundreds of microwatts RF energy at 2.4 kM distance [37].

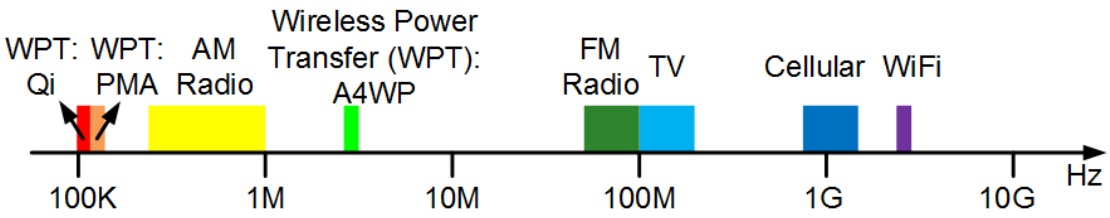


Figure 9. Available frequency bands for RF energy harvesting.

The RF candidate bands are broad from tens kHz AM radio up to GHz cell phone signals as shown in Figure 9. Generally, the higher frequency, the smaller antenna size and wave energy. The ideal antenna is an ultra-wide band (UWB) antenna for as many bands as possible; however, such design inevitably sacrifices performance in specific frequency to achieve a global optimization, and induces complex impedance matching in the following boost converter [38]. Therefore, for maximum harvested energy, nowadays

commercial products focus on a narrow band such as 850-950MHz of the P1100. Its specifications are listed in Table 4. Its minimum input power is -11.5dBm.

Table 4. Performances of the 915MHz RF energy harvester.

Manufacturer ID	Minimum Input Power (dBm)	Maximum Input Power (dBm)	Maximum Output Current (mA)	Output Voltage (V)
P1110	-5	23	100	4.3
P2100B	-12	23	100	6

1.3 Design Challenges of the Energy Harvesting

1.3.1 Maximum Power Point Tracking Technique

The most important challenge in a power harvesting design is the fact that a PV energy source can experience changes in its power density; thus, its MPP depends on different environmental variables such as illumination intensity and temperature [5]. Therefore, a maximum power point tracking (MPPT) technique is needed to dynamically match the output impedance and constantly achieve maximum power transfer under those environmental variations.

An MPPT circuit can be one of the most power hungry blocks in the harvesting system. MPPT circuits require complicated signal processing components such as a successive approximation register (SAR) or a digital signal processor (DSP) and can consume more than 100 μW in power [39], [40]. The hill-climbing MPPT algorithm features the simplest mechanism and minimum devices [41], which is favorable for

monolithic and low power purposes. [42] developed a practical sample-and-hold (S/H) structure for the hill-climbing MPPT; however, it required a power hungry analog current sensor and, thus, was not suitable for microwatt-level energy harvesting. To avoid such issues, [43] monitored the output power with a DAC; however, it also increased the circuit complexity, which consumed more power. In this work, a time-domain hill-climbing MPPT is proposed to reuse the power information from former output regulation. Such a scheme eliminates the need for a current sensor or other analog circuits, and significantly reduces power consumption.

1.3.2 Impedance Tuning

The selection of an impedance tuning variable for MPPT is also important for saving power. Theoretically, the input impedance of the charge pump relies on its switching frequency and capacitor value. Conventional approaches use a voltage-controlled oscillator (VCO) to continuously tune the switching frequency [42], [43]. However, such a frequency modulation scheme usually needs analog operational amplifiers (Op-Amps) with a quiescent power consumption that far exceeds the stringent power budget for these applications. On the other hand, a capacitor value modulation (CVM) does not require analog modules and can be implemented in digital-domain. Its drawback of consuming more chip area is relieved if the harvesting power is as low as tens of microwatts. For this IoT application, low power is more critical than large on-chip capacitors. CVM has been reported in [48]-[50] for dynamic output power scaling. In this work, we propose a CVM approach for impedance tuning in MPPT, which consumes no quiescent power.

1.3.3 Fully Integration

With recent developments in the Microelectromechanical Systems (MEMS) sensors and down-scaling of silicon fabrication technology, the concept of Internet of Things (IoT) has been proposed to uniquely identify objects and their virtual representations in an Internet-like structure [44], [45] as illustrated in Fig. 1(a). In such a network, individual nodes, also called smart nodes, are often implemented as system-on-chip (SOC) solutions, containing sensors, signal processors and wireless transceivers. To power the nodes, multiple possible energy sources are available such as photovoltaic [46], piezoelectric [47], thermoelectric [51], and RF [8]. Compared to these other candidates, photovoltaic (PV) cells potentially provide a higher power density and relatively smaller size. The output energy of PV cells is commonly managed by DC-DC converters with off-chip inductors or transformers, featuring high power throughput and efficiency [52]. However, full integration is preferable to the application of smart nodes, and high quality on-chip inductors are not widely available for the CMOS technology. Alternatively, the monolithic switched capacitor topology is chosen to eliminate the need for an off-chip inductor [53].

Summarily, classified by the demand of isolation or regulation and storage cap, C_{ST}, before pass transistor, there are four combinations as shown in Figure 10. The M_G is used to isolate the charge pump and the load, and prevents the loading condition. The C_{ST} is used to buffer and temporarily store the energy during M_G switching.

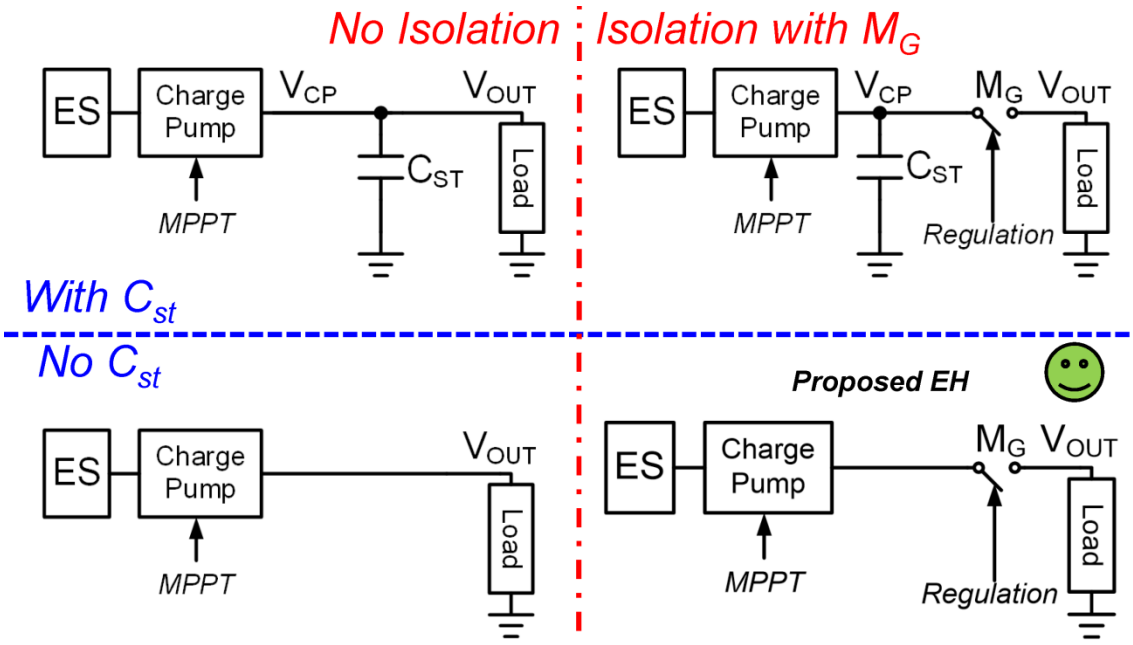


Figure 10. Four different topologies of general energy harvesters.

From Figure 10, the best case is in the right bottom corner, where the power converter and the load are isolated. The output voltage is regulated. And all the on-chip caps are used for switching power conversion.

1.3.4 Output Regulation

Creating an optimal output regulation for a harvesting system is a difficult design challenge. The conventional DC-DC power management theory, which assumes the energy source to be ideal with constant voltage and possessing infinitely available power, is not valid in the PV scenario [54]. In fact, the PV energy source normally has a weak power density and cannot sustain a stable output voltage under heavy loading conditions. To avoid a loading effect on the harvesting system, [43] proposed a gated output control based on a digital-to-analog converter (DAC) and comparators, which consumed quiescent current and greatly reduced power conversion efficiency. In Section

2, an architecture design is proposed to solve power conversion problems. As illustrated in Figure 10, this solution involves a hysteresis regulation to gate the conduction between a buffer capacitor C_{ST} and load, providing a constant output voltage. Here C_{ST} represents a supercapacitor or a battery. Thus, the hysteresis regulation guarantees adaptive maximum power point (MPP) harvesting over various light intensities. When the available PV power is low and not able to sustain its loads, the switch M_G will be turned off and prevent the loads from draining off the charge pump. Thus, the harvesting system is always operated under MPP condition regardless of the illumination intensities. It can power a host of applications in the smart nodes, including sensors, wireless transmitters and battery chargers [55].

1.3.5 Charge Redistribution Loss

The main disadvantage of charge pump topology is its inevitable loss with single conversion ratio (CR). Principally, the inductive DC-DC topology tunes the duty ratio of the pulse-width modulation (PWM) to provide a variable and continuous CR [54]. However, the CR of the capacitive DC-DC topology is intrinsic to its structure and induces a charge redistribution loss (CRL) [56]. Such a loss limits the optimal harvestable voltage to a narrow range and cannot accommodate the wide voltage range of multiple energy sources depending on environmental changes. The fixed CR becomes a bottleneck preventing highly efficient energy harvesting. Therefore, reconfigurable charge pumps are proposed to change its structure during operation. Thus, they provide multiple CRs and eliminate CRL. Nevertheless, they only provide either integral or fractional CRs [57]-[61], and do not have enough resolution across the wide harvesting

range. Thus, they are suboptimal for energy harvesting from various sources. In this work, a reconfigurable charge pump is proposed with hybrid integral and fractional CRs, which effectively improves the resolution of reconfiguration, reduces the CRL, expands the input voltage range, and enhances the harvesting efficiency [62].

1.4 IoT and Hardware Applications

In this section, several commercial solutions for low power energy harvesting are compared and analyzed. For DC energy harvesting as PV and TEG, the first topology is boost-LDO architecture with multiplexing outputs. One example is ADP5090 as shown in Figure 11 [78]. It consists of a boost DC-DC converter with two output channels. The SYS node is connected to a big buffer cap as typical DC-DC converters. Alternatively, if lithium battery is used and connected to the BAT node, the off-chip inductor of the boost converter could directly charge the battery. For high quality power supply, an additional LDO is cascaded as a second stage. It could powered by the boost converter when input available power are enough, or powered by the battery when the energy sources are weak and not sufficient. It uses open circuit voltage (OCV) approach as the MPPT. The main advantage of this product is its ultralow quiescent current as 260nA. The BQ25505 has similar architecture with ADP5090 [79].

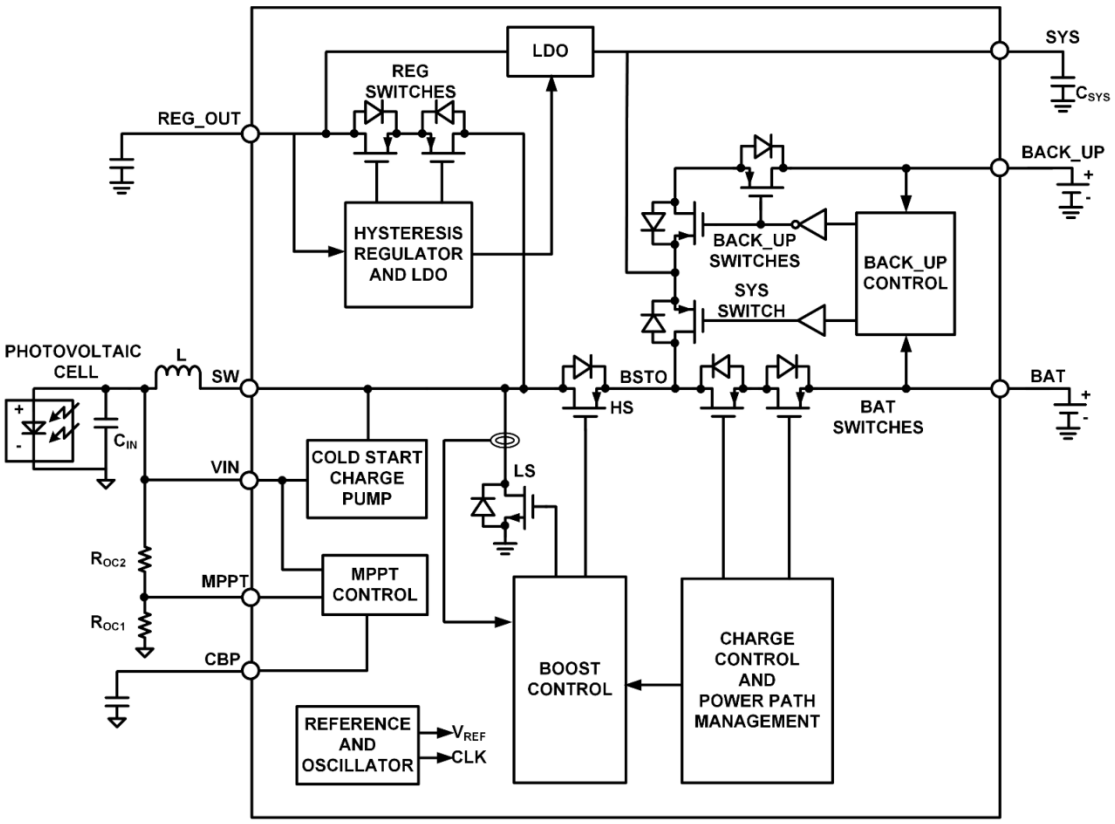


Figure 11. Functional block diagram of boost-LDO energy harvester.

When harvesting TEG voltage as low as 20mV, the conventional boost converter suffers from the V_{th} = 0.5~0.7 V of CMOS transistor and could not cold start up. Therefore, a transformer based forward converter with resonant switching is more feasible for this ultralow input voltage as shown in Figure 12 [80]. Instead of the inductor based topology, the winding number of transformer helps relax the skewed duty ratio of the DC-DC converter operating in discontinuous conduction mode (DCM). The resonant LC tank is formed by the transformer and off-chip capacitor. The effective switching voltage for the NMOS transistor is boosted by the winding number, which is 100 in LTC3107. Therefore, minimum input voltage to stimulate startup oscillating can

be as low as tens of millivolts level. Note that there is no MPPT function associated in this product.

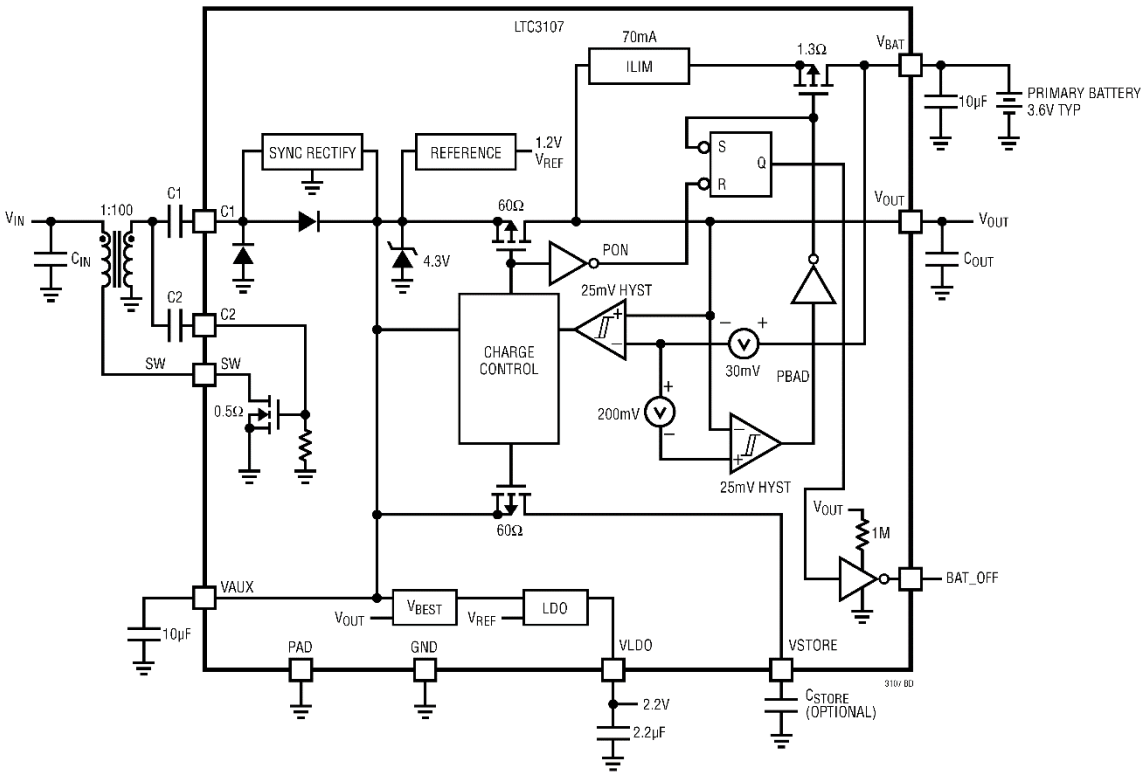


Figure 12. Functional block diagram of transformer-based energy harvester.

In various application scenarios, the harvesting voltage could be higher than the load requirement. Thus, SPV1050 integrates a noninverting buck-boost converter as shown in Figure 13 that can increase or decrease the harvested voltage [81]. It has cascaded LDO for better PSRR supply and OCV approach for MPPT.

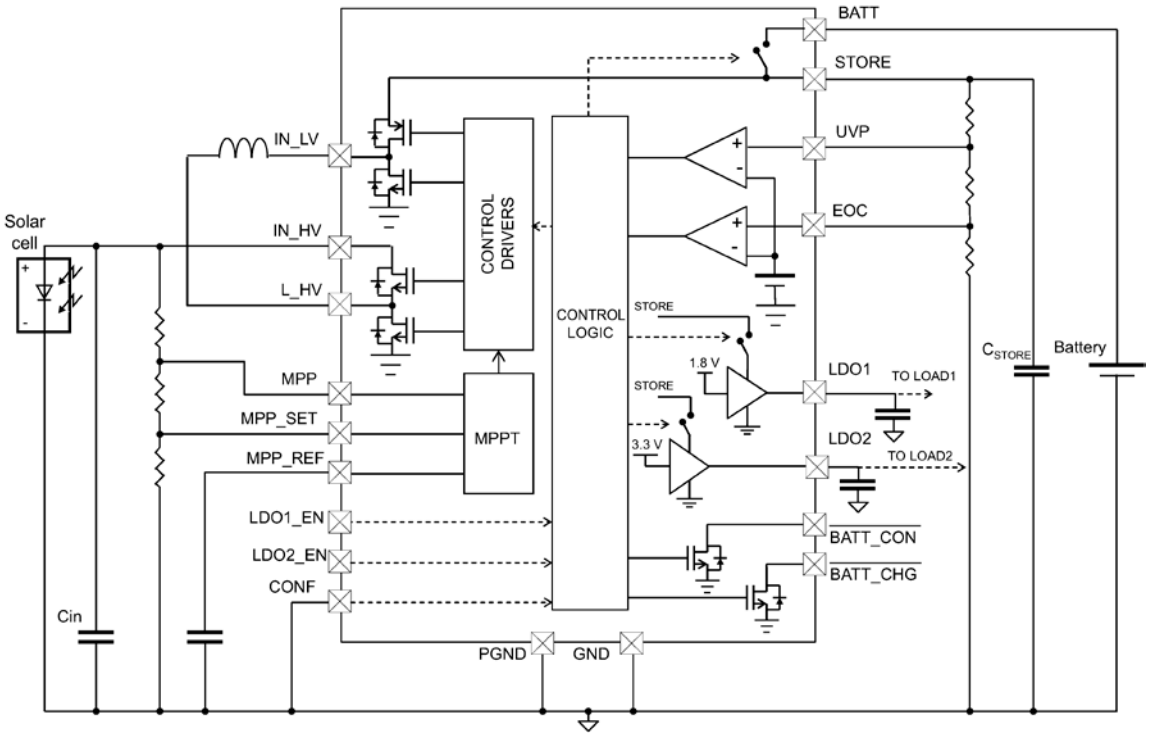


Figure 13. Functional block diagram of buck-boost energy harvester.

Besides the DC-DC energy harvesting, AC-DC conversion is also integrated on chip. MB39C811 is a boost/buck-boost converter in principle as shown in Figure 14 [82]. To accommodate the AC voltage from piezoelectric transducer, two channel of full-wave bridge rectifiers are alternatively cascaded in front of the buck converter. As a result, this product can harvest PV or Piezoelectric energy at the same time. There is no MPPT function or LDO regulators.

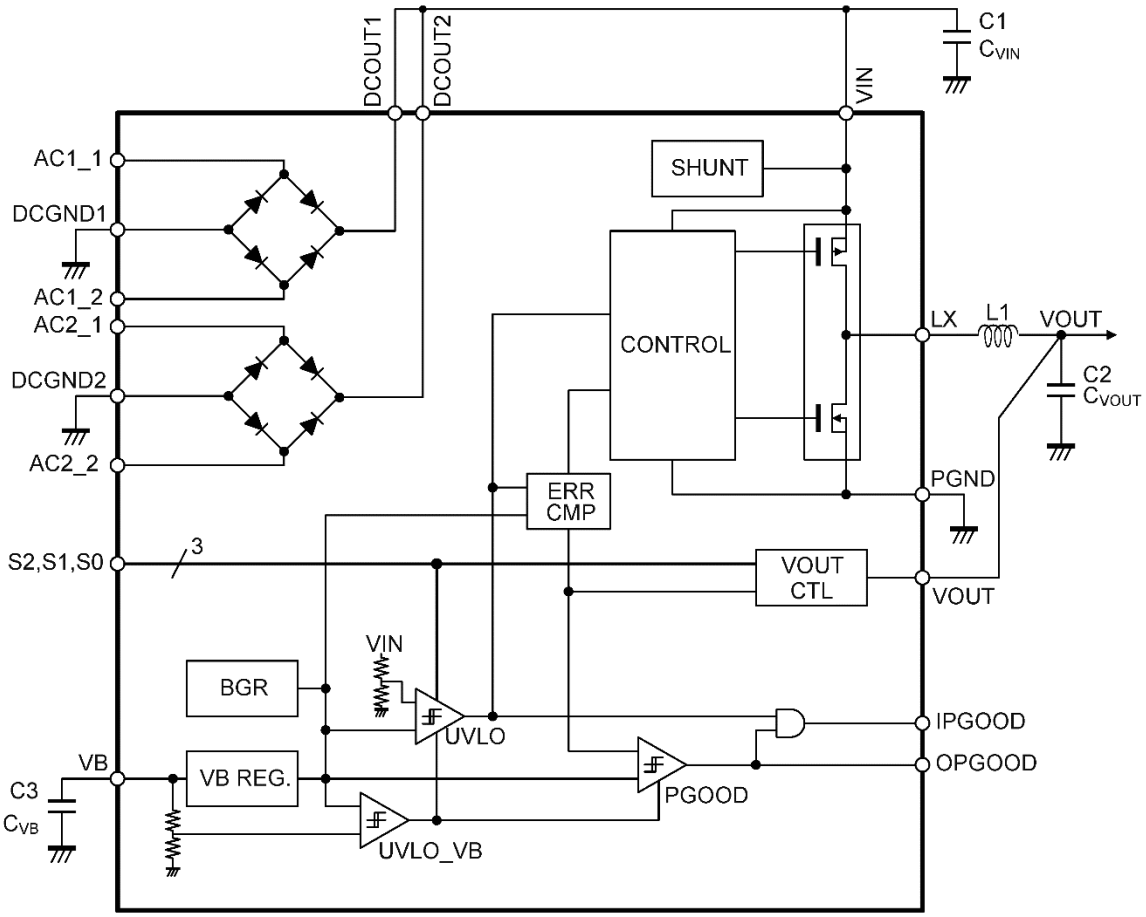


Figure 14. Functional block diagram of AC-DC energy harvester.

Summarily, the main utilized topologies and their commercial products are compared in Table 5. We can conclude that the boost DC-DC topology features simpler architecture, higher efficiency for medium and high throughput power. The transformer-based resonant DC-DC converter features ultra-low harvesting voltage. The noninverting buck-boost converter features flexible harvesting voltage range. The rectifier AC-DC converter is commonly used for AC energy sources.

Table 5. Comparison of various topologies of energy harvesters.

Manufacturer ID	Target Sources	Topology	MPPT	Battery Charger	Min Input Voltage (V)	Required Components
BQ2505	PV/TEG	Boost	Yes	Yes	0.1	L=22μH C=4.7μF
LTC3107	PV/TEG	Forward	No	Yes	0.02	C=2.2μF C=10μF
SPV1050	PV/TEG	Buck-Boost	Yes	Yes	0.075	L=22μH C=0.1μF
MB39C811	PV/PT	Rect/Buck-Boost	No	No	1.2	L=22μH C=47μF

1.5 Conclusion

The physical principles and performances of energy sources, such as PV cell, TEG, PT, and RF, are introduced for IoT applications. The equivalent resistance of the DC sources like PV and TEG are varied by the environmental parameters. Therefore, the MPPT is the most important function and several implementing methods are discussed. Furthermore, other application difficulties such as detailed impedance tuning approaches, integration capability, and output regulation are analyzed with conventional solutions. At the end of this section, commercial solutions for these various energy sources are listed and compared. In the following sections, I will present several basic concepts of the switching power converters for IoT energy harvesting.

2.1 Inductor-based SMPC

2.1.1 Principle and Electrical Model

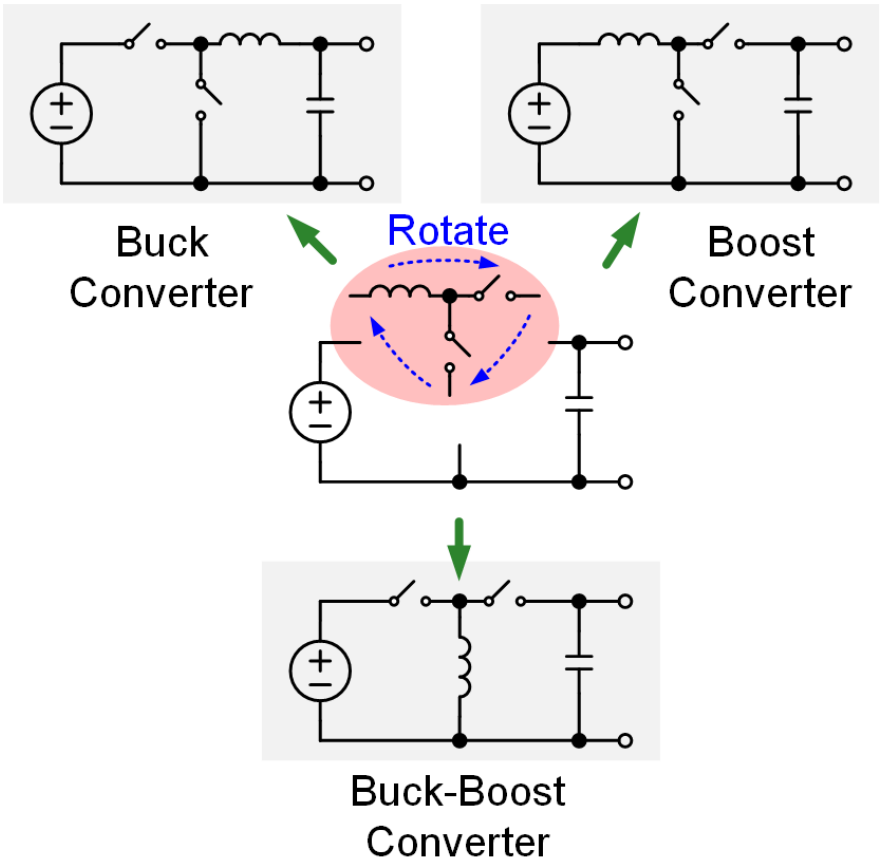


Figure 15. General structures of inductive DC-DC power converters.

The inductor based DC-DC power converter is the dominant topology used in power management and energy harvesting. It features less components and high conversion efficiency. An architecture survey with two active switches, two passive components is illustrated in Figure 15. For constant output voltage, the capacitor is

always parallel with the load as a filter. The remaining two switches and inductor can be connected as T network. By rotating the three terminals of the network, the circuits behavior buck, boost, and inverting buck-boost conversion ratio [54].

Take the buck converter as an example, the waveforms of the continuous conduction-mode (CCM) and the discrete conduction-mode (DCM) are shown in Figure 16. Under CCM, the load consumes small current and the inductor current, I_L, is always positive with small ripples. Under DCM, the load consumes relatively larger current and enforces I_L disconnected during an off time. The boundary condition between CCM and DCM is determined by the load resistance, inductor value and switching frequency,

$$I_{L,crit} = \frac{V_g D D' T_s}{2L} \tag{3}$$

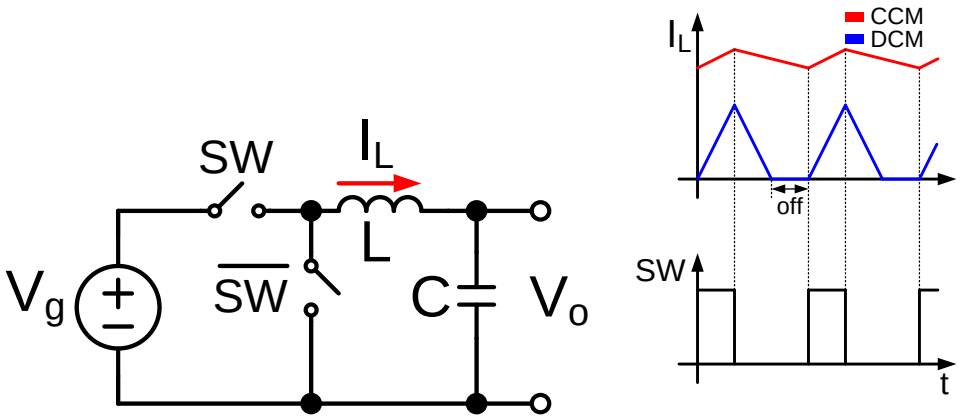


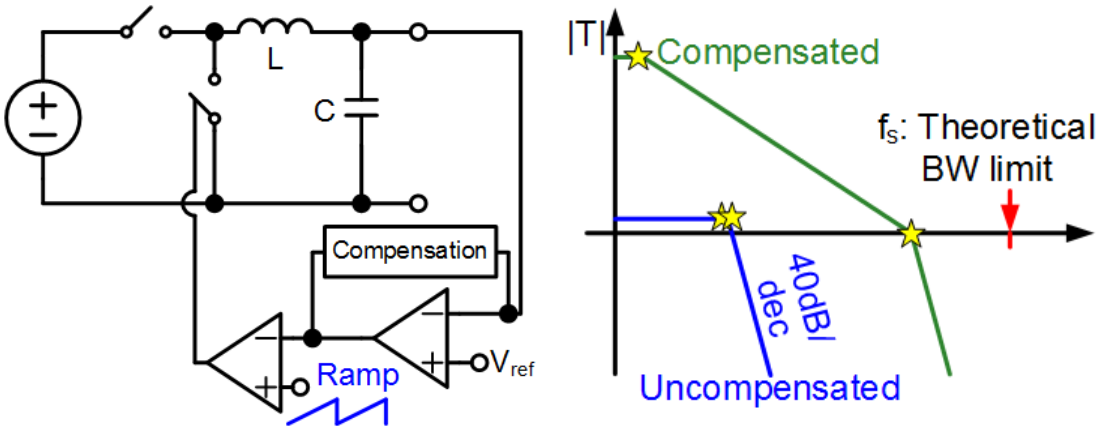
Figure 16. Buck converters operated in CCM and DCM.

This is the major difference between general DC-DC power converters and the one used in IoT applications. Due to the limited size requirement of IoT smart nodes, the implemented inductors are always relatively small, and the DC-DC converter is operated in DCM. There are two major issues should be taken care for the special feature:

efficiency and stability. The first consideration is that how to optimize the conversion efficiency. The theoretical efficiency of inductor-based SMPC can be as high as 100%. In practical applications, the energy losses are generally caused by switching losses and conduction losses [54]. In the DCM scenario, the switching frequency is relatively low and the associated switching loss is not significant. On the other hand, the conduction loss is more significant, because most of the time is charging the inductor with a weak energy source, and the duty ratio is highly skewed more than 90%. Under such a skewed switching clock, significant efficiency degeneration will happen as illustrated in Section 1.4. The transformer-based DC-DC converter can relieve the skewed waveform and save energy, but suffers from bulky size and expensive cost for the application of IoT smart nodes.

The stability issue of the DC-DC converter is detailed in the following paragraph with the pulse-width modulation (PWM) control scheme.

2.1.2 Pulse-width Modulation



(a) (b)

Figure 17. (a) Conceptual voltage mode negative feedback loop with PWM, and (b) its small signal analysis in s-domain.

The conventional design challenge of inductor-based SMPC is that how to build a fast but stable control loop [63]. The conceptual negative feedback for a buck converter is given in Figure 17. The pule-width modulation (PWM) is a topology to convert the voltage information into duty ratio with constant switching frequency and predictable output ripple [64]. Therefore, the load, especially supply noise-sensitive circuits such as transceivers, will accommodate to the harmonics of supply ripple and avoid this interferential frequency band. The two reactive components, L and C, generate a pair of complex poles at low frequency due to their large values. As a result, the uncompensated transfer function has narrow bandwidth and barely gain, which imply a slow response for dynamic output transient and a large error for static output voltage. In the s-domain, the Type-I, II, III active-RC filters are developed as voltage programmed approach to compensate the complex poles and provide enough phase margin and DC gain [65]. More advanced techniques like current programmed approach [66], [67], V^2 approach [68], quasi-V^2 approach [69], one-cycle approach [70], and etc. are developed to further split and compensate the complex poles. Besides of the PWM topology, pulse-frequency modulation (PFM) is a cost efficient scheme with better stability but unpredictable ripple frequency of the output voltage [71].

An analysis for a generic buck converter with CCM PWM controller is given here [63]. By simplifying the system in Figure 17, a block diagram can be established as Figure 18.

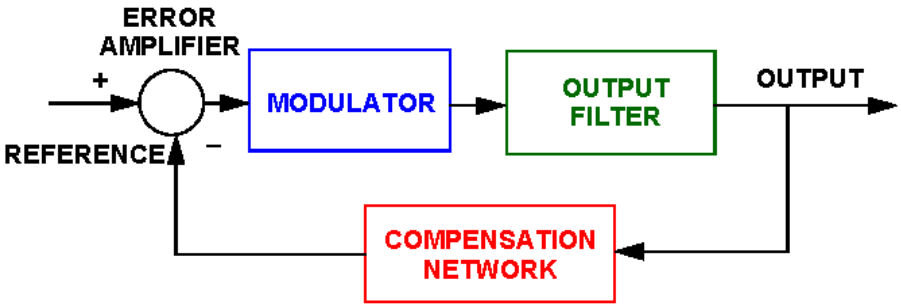


Figure 18. Basic block diagram of the buck converter.

The PWM modulator is detailed in Figure 19. Its small signal transfer function can be derived as,

$$H_{Modulator} = \frac{V_{IN}}{\Delta V_{OSC}} \tag{4}$$

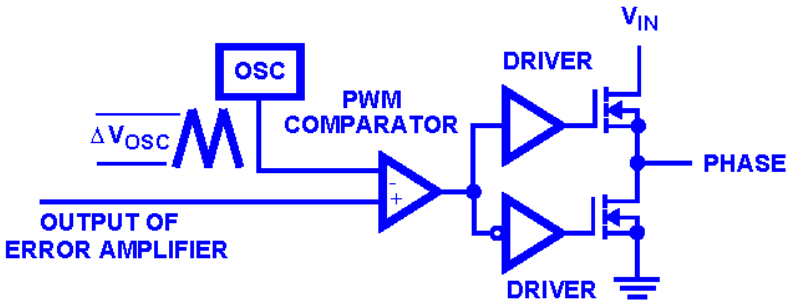


Figure 19. Detailed architecture of the PWM modulator.

The power stage, also called output filter, is detailed in Figure 20 and its mathematical expression is given as below,

$$H_{Filter} = \frac{1 + s \cdot ESR \cdot C_{OUT}}{1 + s \cdot (ESR + DCR) \cdot C_{OUT} + s^2 \cdot L_{OUT} \cdot C_{OUT}} \tag{5}$$

where ESR and DSR are the parasitic resistance of the power capacitor and inductor, respectively.

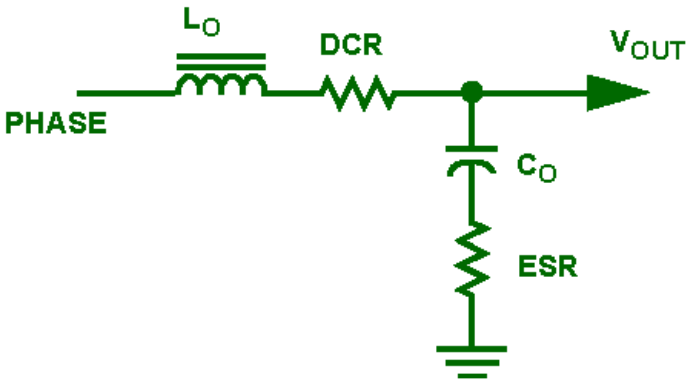


Figure 20. Detailed architecture of the output filter.

The third block of Figure 18, the error amplifier with the Type-III compensation, is detailed in Figure 21 and mathematically derived as,

$$H_{Filter} = \frac{R_1 + R_3}{R_1 \cdot R_3 \cdot C_1} \cdot \frac{\left(s + \frac{1}{R_2 \cdot C_2}\right) \cdot \left(s + \frac{1}{(R_1 + R_3) \cdot C_3}\right)}{s \cdot \left(s + \frac{C_1 + C_2}{R_2 \cdot C_1 \cdot C_2}\right) \cdot \left(s + \frac{1}{R_3 \cdot C_3}\right)} \tag{6}$$

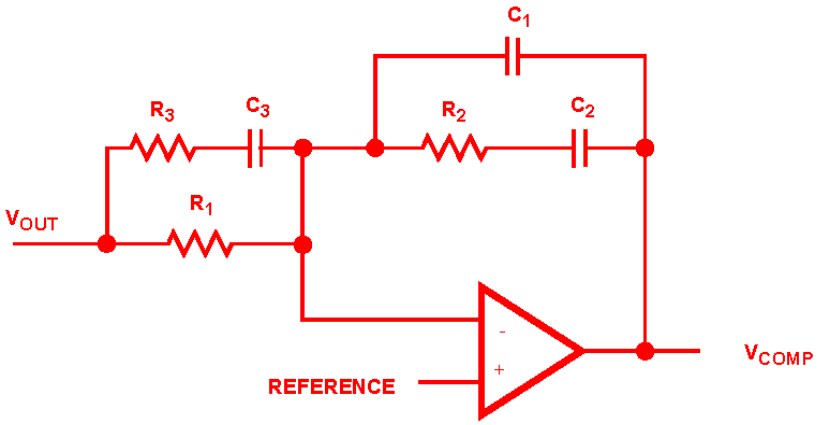


Figure 21. Detailed architecture of the error amplifier and the Type-III compensator.

The design tradeoffs of general DC-DC power converters can be summarized as Table 6.

Table 6. Design tradeoffs of general DC-DC power converters.

	Stability	GBW & Speed	Power Consumption	PSRR	Area & Cost
PWM	↓	↓	↓	↑	↓
PFM	↑	↑	↑	↓	↑
Quiescent Current I_Q ↑	↑	↑	↑	↑	—
Maximum Load Current $I_{out,max}$ ↑	↓	↑	—	—	↑
Error Amplifier Gain A_{EA} ↑	↓	↑	—	↑	↑
Output Cap C_{OUT} ↑	↑	↓	—	↑	↑

In the particular scenario of energy harvesting, the DC-DC converters are always operating in DCM due to the low available power. Therefore, the complex poles are split and the stability is not a concern anymore as shown in Figure 17.

2.2 Switched Capacitor SMPC

2.2.1 Principle and Electrical Model

Conventionally, the high voltage was generated by transformer and could only goes up to 200,000 volts. The switched capacitor SMPC is completely built with capacitors and switches. This topology was firstly invented by Swiss physicist Heinrich Greinacher in 1919 as Figure 22 [72]. In 1932, John Douglas Cockcroft and Ernest Thomas Sinton Walton used this topology with cascaded diode-capacitor stages in series to generate high voltage over 800,000 volts. This so-called Cockcroft-Walton

multiplying circuit helped accelerator particle for high energy physics experiments and won the 1951 Nobel Prize in Physics.

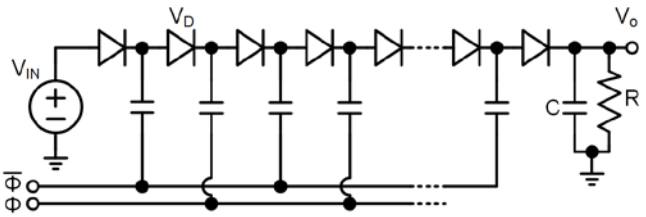


Figure 22. Switched capacitor SMPC composed of diodes and capacitors.

The conversion ratio of charge pump is defined as the ratio between the output and input voltage:

$$CR = \frac{V_o}{V_{in}} \tag{7}$$

If CR > 1, it is a step-up charge pump. If CR < 1, it is a step-down charge pump. If CR < 0, it is an inverting charge pump.

2.2.2 Equivalent Resistance of Switched Capacitor DC-DC Converters

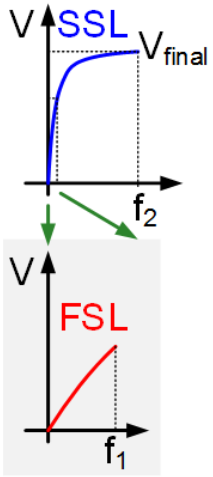


Figure 23. Slow-switching limit and fast-switching limit of charge pump.

The operation of charging and discharging capacitors can be defined as slow-switching limit (SSL) and fast-switching limit (FSL) [86]. The main criterion is the relationship between charging time constant and switching frequency. The time constant is defined by the product of the resistance along the charging path and the utilized capacitor value as shown in Figure 23. When the switching speed is significant lower than the time constant, the capacitor is finally charged to static value. The equivalent resistance of SSL condition can be expressed as,

$$R_{SSL} = -\frac{v_{out}}{i_{out}} = \sum_{i \in caps} \sum_{j=1}^{n} \frac{\left(a_{c,i}^{j}\right)^2}{2C_i f_{sw}} \tag{8}$$

where $a_{c,i}^{j}$ is the charge multiplier vector, which is the proportional between flowing current (charge) of each capacitors and total output current (charge).

The FSL condition happens when the switching frequency is so fast that the charging voltage of capacitor cannot stabilize to the final value. Therefore, the conduction resistance of switches, R_i, should be taken into account of the total equivalent resistance.

$$R_{FSL} = \sum_{i \in switches} \sum_{j=1}^{n} \frac{R_i}{D_j} \left(a_{r,i}^{j}\right)^2 \tag{9}$$

where D_j is the duty of each conduction time.

Considering both the two conditions, the total equivalent resistance of charge pump can be approximated as,

$$R_{OUT} \approx \sqrt{\mathrm{R}_{SSL}^2 + \mathrm{R}_{FSL}^2} \tag{10}$$

In most of applications, the charge pump is intentionally designed in either SSL or FSL modes depends on the available capacitor values and required efficiency. Thus, either (8) or (9) are selected to calculate the equivalent resistance instead of (10). Principally, the SSL mode has less dynamic loss, high efficiency but larger capacitors. The FSL mode has more dynamic loss, degenerated efficiency, but smaller capacitors and compact size.

2.2.3 Dickson Charge Pump & Gate Control

The two terminal switches in Figure 22, diodes, are easier to fabricate and utilize without control signals. It was firstly transferred to the form of state-of-the-art in 1976 and named as Dickson charge pump [73]. However, the relative large dropout voltage, V_D, compromises the output voltage and power, and is unacceptable for low voltage application. Mathematical proof shows that the output voltage cannot be further boosted even with increasing stages [72].

$$V_o = (n+1)V_{IN} - nV_D \tag{11}$$

With the emerging of MOS technology, NMOS switches are widely utilized to replace the diodes due to its feasibility for integration. A generic example can be shown in Figure 24. The NMOS transistors in diode-connection replace the diodes in Figure 22 and still suffer from the threshold voltage drop and furthermore the body effect as,

$$V_o = (n+1)V_{IN} - nV_{th} - \sum_{i=1}^{n} \Delta V_{th,i} \tag{12}$$

where $\Delta V_{th,i}$ is the voltage drift due to source-body voltage difference during boosting. According to the semiconductor physics, $\Delta V_{th,i}$ will get larger with higher boosted

voltage, and eventually stop CR increasing with more boosting stages. The worst case condition happens when $V_{IN} = V_{th} + \Delta V_{th,i}$.

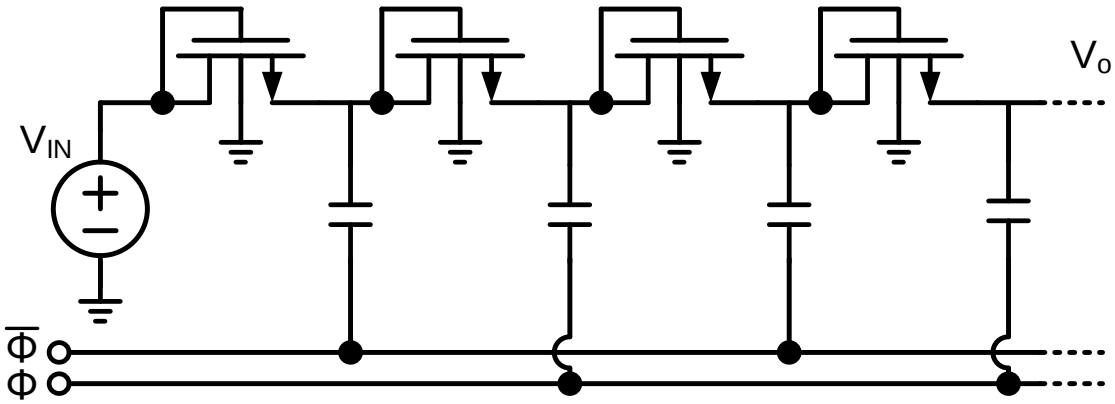


Figure 24. Architecture of the Dickson charge pump.

Therefore, to reduce the dropout voltage and conduction loss, the switches of the charge pump need fully turn on, in other words, the gate control signals need to increase with the stages. One solution is to independently drive the switches with higher voltages generated by following stages [74]. The detailed implementation is shown in Figure 25. $M_{D1,2...}$ transistors are configured in diode-connection and assisted the building up of $V_{1,2...}$. M_{N1} and M_{P1} are connected as an inverting gate driver. Its low supply rail is reused from the input of this stage and guarantees reliable shut down. Its high supply rail is reused from the output of this stage and guarantees fully turn on in the case of $V_{IN} >> V_{th}$. Generally, the swing of the gate control signal is listed as,

When Φ = 0: $V_1 = V_{IN}$ $V_2 = 3V_{IN}$ $V_4 = 5V_{IN}$

When Φ = 1: $V_1 = 2V_{IN}$ $V_2 = 2V_{IN}$ $V_4 = 4V_{IN}$

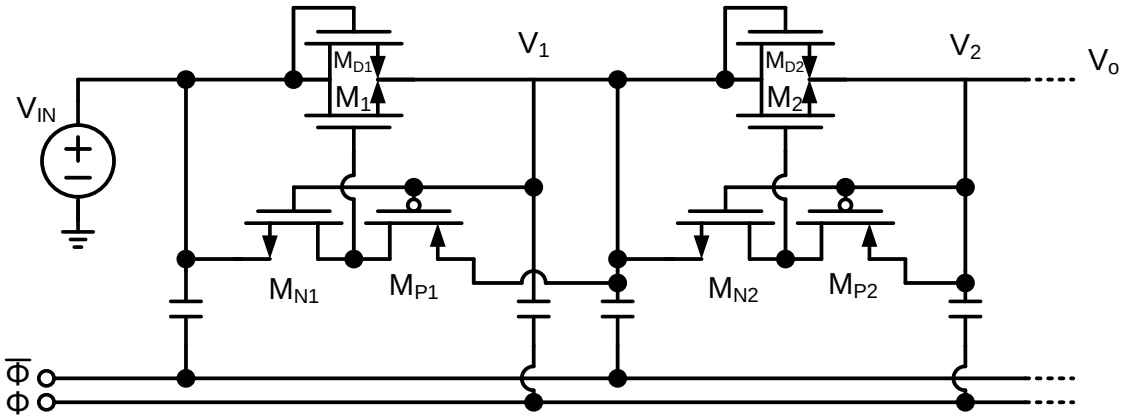


Figure 25. Reuse of the higher gate control voltage from the following stages.

From the list, the supply rail for each stage is leveled up by V_{IN} with increasing stage number. For further reducing the drop voltage upon each switch, their body bias can be dynamically switched [75], [76]. However, the switching body bias will induce potential latch-up hazard and need special Twin-well CMOS technology.

2.2.4 Serial-parallel, Fibonacci, and Doubler Charge Pump

Besides the classic Dickson charge pump, there are two other widely utilized topologies, serial-parallel topology and Fibonacci topology. The serial-parallel topology is illustrated in Figure 26. During phase 1, n capacitors are charged in parallel by the input voltage. During phase 2, n capacitors are cascaded with the input voltage sources in series and boosted the voltage as $V_o = (n + 1)V_{IN}$, where n represents the capacitor count. In the low power application scenario, the serial-parallel charge pump is not component efficient and consumes more active area for specific conversion ratio. In other words, the serial-parallel topology has similar device count with the Dickson charge pump.

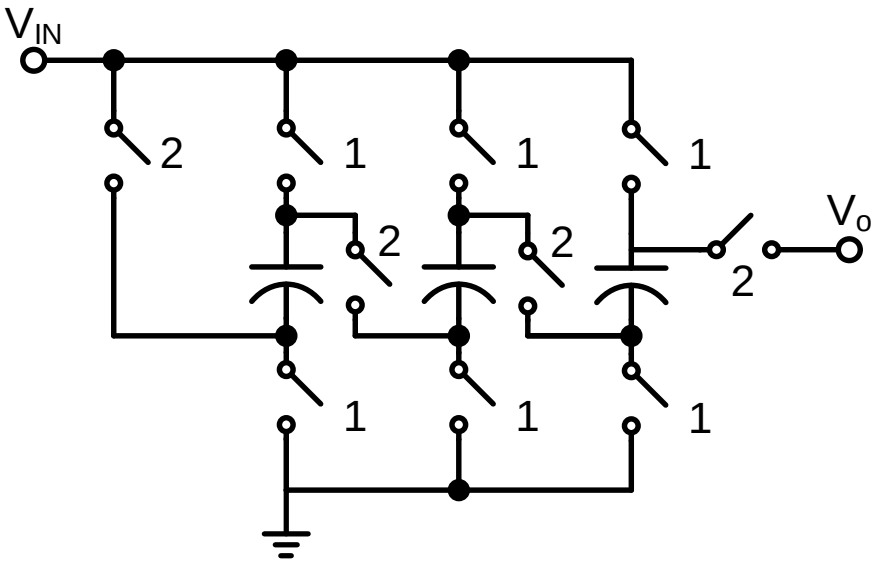


Figure 26. Architecture of the serial-parallel charge pump.

The Fibonacci charge pump is a hybrid topology of serial-parallel and Dickson architectures. Its details operating phases are shown in Figure 27. During phase 1, the odd stages are charged and the even stages are discharged. The resulting conversion ratio likes the Fibonacci sequence and can be calculated as,

$$CR = \frac{\sqrt{5}}{5}\left[\left(\frac{1+\sqrt{5}}{2}\right)^{n+2} - \left(\frac{1+\sqrt{5}}{2}\right)^{n+2}\right] \tag{13}$$

Depending on the increasing speed of the conversion ratio, the Fibonacci topology features exponential increase, which is much faster than the linear increase like Dickson or serial-parallel topologies. Therefore, the Fibonacci architecture uses less power devices, and is more hardware efficient for specific CR.

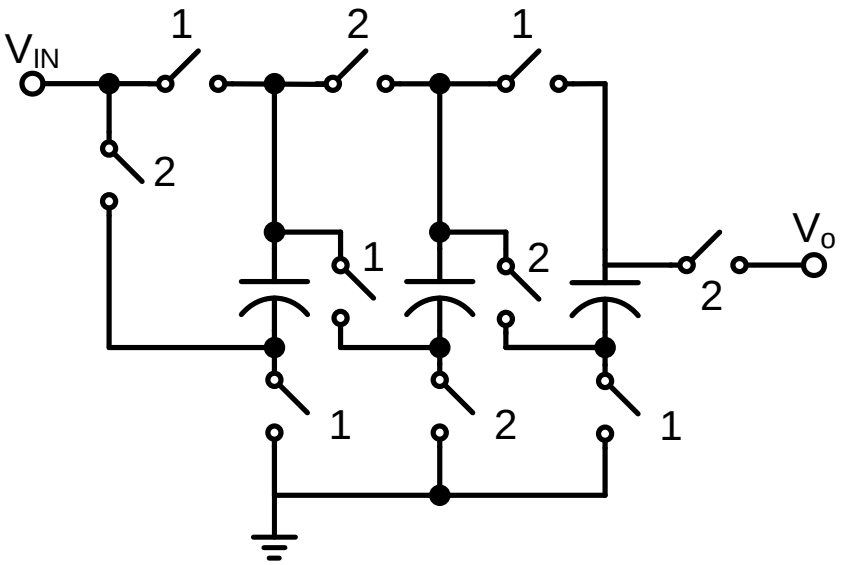


Figure 27. Architecture of the Fibonacci charge pump.

The last topology will be introduced is the doubler charge pump, which is abbreviated as voltage doubler. It is a derivative version of Dickson charge pump, that directly cascades a single stage with CR = 2 as shown in Figure 28. The resulting conversion ratio can be calculated as,

$$CR = 2^n \tag{14}$$

The increasing speed of the voltage doubler is the theoretically fastest as exponential growth with larger base number as 2 than the Fibonacci topology, and features the most compact size. This is the main reason that the voltage doubler is widely utilized in the state-of-the-art applications with limited chip area such as the non-volatile memory.

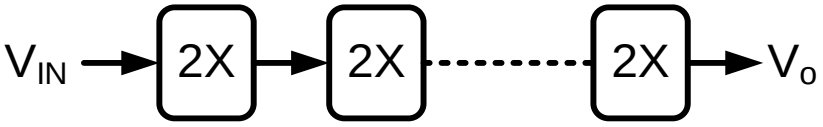


Figure 28. Architecture of the voltage doubler.

2.2.5 Mathematical Analysis and Dynamic Behavior

The behavior of generic charge pump is mathematically analyzed in this paragraph. Firstly, the energy stored at an ideal capacitor can be expressed as,

$$E(t) = \frac{1}{2} C v(t)^2 \tag{15}$$

If the capacitor is charged by a voltage source through a resistor R from initial voltage V_1 to final voltage V_2, the energy delivered to the capacitor is,

$$E_C = \frac{1}{2} C V_2^2 - \frac{1}{2} C V_1^2 \tag{16}$$

The energy consumed by the path resistor R can be calculated as,

$$E_R = \frac{1}{2} C (V_2 - V_1)^2 \tag{17}$$

The energy supplied by the voltage source can be expressed as,

$$E_S = C V_2 (V_2 - V_1) \tag{18}$$

If extend the analysis to general charge transfer in switched capacitor circuits, a generic model could be built as Figure 29. After settling with their initial voltage $V_1(0)$ and $V_2(0)$, the consumed charge redistribution aforementioned in Section 1.3.5 can be derived as,

$$E_{CRL} = \frac{1}{2} (C_1 \parallel C_2)(V_1 - V_2)^2 \tag{19}$$

Note that the CRL is only determined by the capacitor values and voltage ripples.

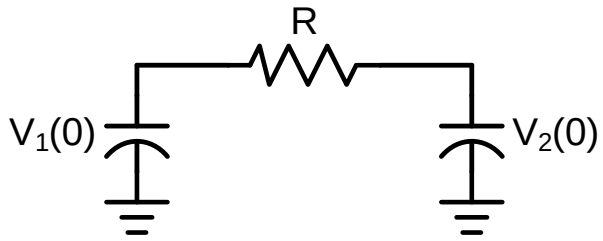


Figure 29. Generic model of the charge transfer in switched capacitor circuits.

2.2.6 Design Consideration and Procedure of Voltage Doubler

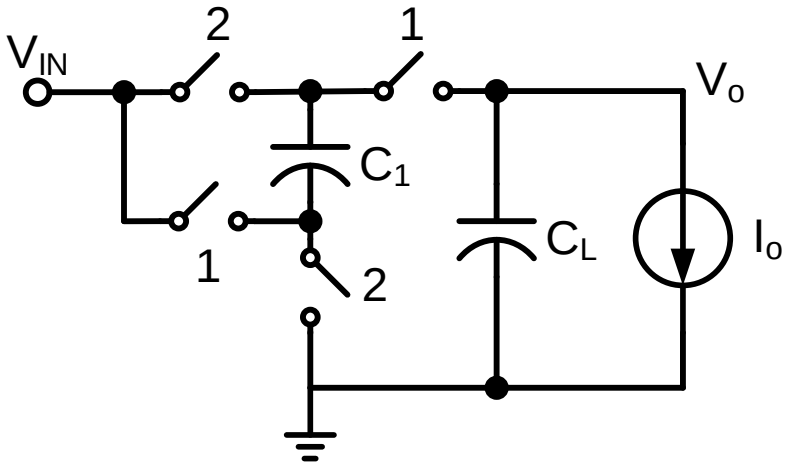


Figure 30. Generic model of the single phase voltage doubler with a current source load.

To relate the quantitative analysis with the circuit theory, a classic design example of single phase voltage doubler will be illustrated in the following. Its design principle is to find the minimum capacitor area for specific output power. The simplified voltage doubler is shown in Figure 30.

Considering the output voltage averaged by time,

$$\bar{V_o} = 2V_{dd} - \frac{I_o T}{C_1} + \frac{I_o T}{8(C_1 + C_L)} - \frac{I_o T}{8C_L} \tag{20}$$

The output impedance of the charge pump is,

$$R_o = -\frac{dV_o}{dI_o} = \frac{T}{C_1} + \frac{T}{8(C_1 + C_L)} - \frac{T}{8C_L} \approx \frac{T}{C_1 \parallel (8C_L)} \approx \frac{T}{C_1} \tag{21}$$

Because the CRL is related by the ripple voltage, it is firstly

$$\Delta V = \frac{I_o T}{C_1} - \frac{I_o T}{8(C_1 + C_L)} + \frac{I_o T}{8C_L} \tag{22}$$

By defining $C_L = kC_1$, a cost function can be establish to minimize the utilized capacitor area,

$$A = (C_1 + C_L)\left(\frac{1}{C_1} - \frac{1}{8(C_1 + C_L)} + \frac{1}{8C_L}\right) \tag{23}$$

The optimized value can be extracted by make its derivative value equal to zero,

$$\frac{dA}{dk} = 0 \rightarrow k = \frac{1}{2\sqrt{2}} \tag{24}$$

The result indicates the best capacitor ratio between the switched ones and the load capacitor: the utilized switched capacitor should be 0.3536 times of the load capacitor. The more complicated architecture can be designed by split into single cascaded stages and applied the methodology.

Table 7. Design tradeoffs of general charge pumps.

	Ripple Magnitude	Throughput Power	Charge Redistribution Loss (CRL)	Switching Loss	Area & Cost
Used Cap ↑	↓	↑	↓	—	↑
Size of Switches ↑	—	↓	—@SSL ↑@FSL	↓	↓
Switching Freq f ↑	↓	↑	↓	↑	—
Conversion Ratio CR ↑	—	↓	—	↑	↑

The aforementioned design tradeoffs of general charge pumps are summarized in Table 7.

2.3 Low Dropout Regulator

The low dropout regulator can linearly regulate the output voltage even when the supply voltage is very close to the output voltage. Its main advantage is that it can significantly suppresses the supply noises for many supply noise sensitive loads, such as wireless transceiver, small signal processing, filtering and etc. [77]. The generic architectures of LDO are shown in Figure 31. The NMOS pass transistor version features smaller conduction resistance, smaller chip size and related parasitic capacitances. Moreover, its drain is connected to the input, and naturally rejects the incoming ripples with high r_{ds} of M_N. Its source is connected to the output and behaves as a low impedance node. Therefore, the output pole could be non-dominant pole, and the change of load resistance will hardly affect the stability of LDO. Although with the efficiency and stability advantages, the main challenges is the gate control voltage should always be higher than output voltage by a V_{gs} = 0.5~0.7 V, which is unacceptable for nowadays submicron CMOS technology. In other words, the consuming of large headroom compromises the low dropout nature of this circuit. Some solutions such as charge pump LDO was proposed to generate a local high supply voltage for driving the NMOS pass transistor [77], but still suffers from PSRR, stability, and efficiency issues. The small signal representation of the output voltage of the LDO shown in Figure 31(a) can be derived as,

$$V_{out} \cong \frac{V_{ref}}{\beta} + \frac{V_{in}}{A_{EA}\beta} \tag{25}$$

where $\beta = \frac{R_2}{R_1+R_2}$ is the voltage feedback factor, A_{EA} is the voltage gain of the error amplifier.

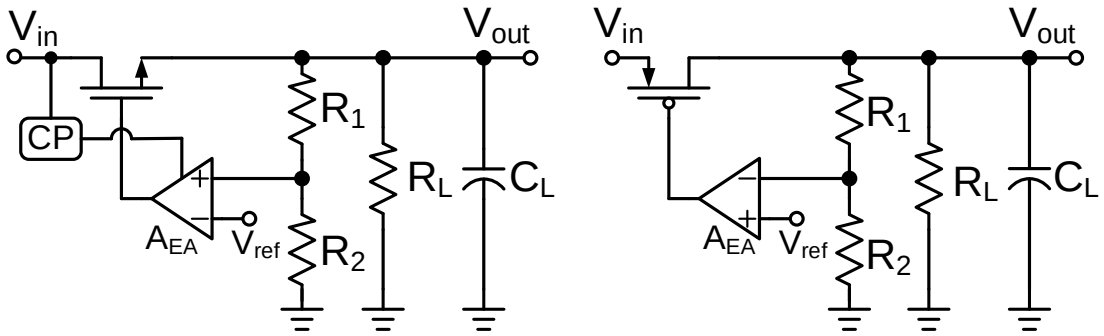


Figure 31. Low dropout regulators with (a) NMOS and (b) PMOS pass transistors.

Another solution to the limited gate driving of NMOS pass transistor is replacing it with PMOS pass transistor as Figure 31. According to the MOS principle, the gate signal is lower than V_{in} and compatible for small signal processing and driving circuits [77]. However, as implied in the former paragraph, the PMOS pass transistor suffers from higher conduction resistance, larger chip size and more related parasitic capacitances. Moreover, the source of M_N faces the input and suffers from noises. The feedforward noise cancellation technique was proposed to maintain constant V_{gs} but cause more power consumption and chip area. Another main disadvantage is that the high impedance drain node of M_N is connected to the output, which implies the output pole must be the dominant pole and complex compensation is needed for stability under

load changing. The small signal representation of the output voltage of the PMOS LDO shown in Figure 31(b) can be derived as,

$$V_{out} \cong \frac{V_{ref}}{\beta} + \frac{V_{in}}{A_{EA}A_{PT}\beta} \tag{26}$$

Comparing (25) and (26), the only difference is the A_{PT}, which is the voltage gain of common-source amplifier with the PMOS pass transistor and load resistors as R_1, R_2, and R_L. Such a gain boosting improves the loop gain and output error voltage, and theoretically suppresses the power supply ripple (PSR). However, compared with Figure 31(b), the PMOS LDO is intrinsically more susceptible to the PSR because its source faces the ripple, which is amplified by the aforementioned common-source amplifier and presents a worse power supply ripple rejection (PSRR) than the NMOS LDO.

Table 8. Design tradeoffs of the LDO.

	Loop Gain	Stability	GBW & Speed	Power Consumption	PSRR	Dropout Voltage	Area & Cost
Quiescent Current I_Q ↑	↑	↑	↑	↑	↑	—	—
Maximum Load Current $I_{out,max}$ ↑	↑	↓	↑	—	↑	↓	↑
Error Amplifier Gain A_{EA} ↑	↑	↓	↑	—	↑	—	↑
Load Cap C_L ↑	—	↑	↓	—	↑	—	↑

From the aspect of stability, the loop gain of PMOS LDO becomes more susceptible to the load variation. This is because its transfer function depends on the loading condition as (26) instead of (25). Therefore, at the heavy loading condition, A_{PT} is small, provides enough phase margin, and does not affect the stability. At the light loading condition, A_{PT} could be very large, sacrifices the loop phase margin, and impairs the stability. The design tradeoffs of the LDO are listed in the Table 8.

2.4 Conclusion

In this section, three generic topologies, inductor-based SMPC, switched capacitor SMPC, and LDO, are summarized and compared their pros and cons. The design consideration of the inductor-based DC-DC power converter is discussed and focused on the DCM scheme for IoT energy harvesting. For the charge pump, various topologies are compared and a design example is given for least cost. For the LDO, the principle of NMOS and PMOS pass transistor topologies are analyzed. In the following sections, I will introduce my solutions based those generic power converters for IoT energy harvesting and tackle the aforementioned various challenges in Section 1.4.

3 THE STATE-OF-THE-ART MAXIMUM POWER POINT TRACKING*

In this section, the major issues of the maximum power point tracking for energy harvesting ICs are analyzed as the order: the analog power sensing technique with capacitor value modulation method is introduced in Section 3.1, the digital power sensing with time-domain quantization is introduced in Section 3.2 for high harvesting efficiency and ultra-low power, and the two-dimensional MPPT technique is introduced in Section 3.3 for enhanced impedance matching and a wide harvesting range.

3.1 Current Sensing MPPT

3.1.1 Architecture of the Proposed Energy Harvesting System

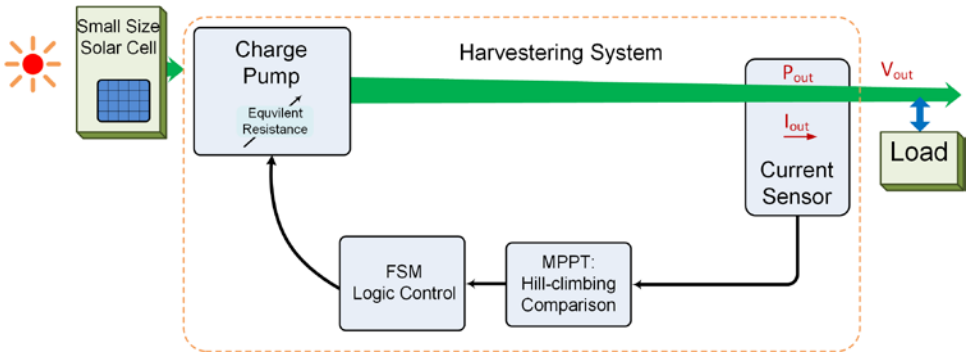


Figure 32. Block diagram of the proposed energy harvester with the MPPT technique.

* Part of this section is reprinted with permission from (1) X. Liu and E. Sanchez-Sinencio, "A highly efficient ultralow photovoltaic power harvesting system with MPPT for Internet of Things smart nodes," IEEE Trans. Very Large Scale Integration (VLSI) Systems, vol. 23, no. 12, pp. 3065-3075, Dec. 2015. Copyright [2015] by IEEE.

X. Liu and E. Sanchez-Sinencio, "An 86% efficiency 12 μW self-sustaining PV energy harvesting system with hysteresis regulation and time-domain MPPT for IOT smart nodes," IEEE J. Solid-State Circuits, vol. 50, no. 6, pp. 1424-1437, Jun. 2015. Copyright [2015] by IEEE.

X. Liu, L. Huang, K. Ravichandran, and E. Sanchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional MPPT for Internet of Things," IEEE Journal of Solid-State Circuits (JSSC), vol. 51, no. 5, pp. 1302-1312, May 2016. Copyright [2016] by IEEE.

The proposed structure of the adaptive harvesting system is shown in Figure 32 where FSM is a finite-state machine. Note that the switching-mode DC-DC power converter using an inductor or transformer, such as a boost converter, features high transferring power density and efficiency [51], [83]. However, the high quality on-chip inductors are not widely available for the CMOS technology. Therefore, to achieve monolithic integration, a charge pump, shown in Figure 32, is chosen for its compact on-chip capacitor. As a direct interface to the solar cell, the charge pump boosts the input PV voltage to the required level and delivers the PV energy to the supercapacitor and loads. A current sensor, MPPT module and digital controller compose the feedback path. To achieve smart control of IoT networks, an I/O communication interface is designed to exchange information with external WSNs.

The power conversion efficiency is the most crucial figure of merit (FOM) of the design of harvesting system topologies. With a PV cell size of 10 mm × 25 mm and 200 lux illumination, the available power is below 11 μW, which is a stringent power budget on the harvesting method. Therefore, the analog control schemes using several operational amplifiers are not feasible due to the quiescent power consumption [65].

Furthermore, the control strategy should extract as much energy as possible from the PV energy source. However, the photovoltaic maximum power point (MPP) or equivalent impedance are not constant, but are shifted with the environmental parameters such as illumination intensity and temperature. Thus, a dynamic MPPT algorithm is a must to track the output impedance of solar cell Z_{solar} and achieve maximum power transfer. Generally, the MPP decreases with lower light intensity and

higher temperature. Based on this topology, the straightforward hill-climbing algorithm of MPPT is chosen to minimize the hardware complexity and power consumption [40]. In order to dynamically track the MPP in Figure 32, information of the output power delivered from the charge pump to the loads needs to be extracted. Since output power P_{out} is filtered by the supercapacitor to maintain a constant voltage, output current I_{out} is proportional to Pout and can be monitored by a current sensor. Due to the ultra-low PV power, the entire load current is used for sensing. Therefore, to minimize its power consumption, the current sensor is only powered on during the short MPPT procedure. During other time, it is shut down and bypasses the harvested power to the load. The detailed MPPT mechanism will be discussed in 3.1.2.

Last but not least, the specific parameters that allow MPPT impedance tuning are also critical to the structure of the harvesting system. Ideally, the input impedance of a charge pump Z_{cp} is provided by the product of switching frequency fs and capacitor values C_u. Conventional solar energy harvesters employ various kinds of frequency modulation by tuning the switching frequency f_s or duty ratio D [42], [46], [51]. However, the power consumption of the frequency modulator is not negligible and strongly affects the overall energy harvesting efficiency. Thus, in the feedback path of Figure 32, a self-biased switch type current sensor with an energy-efficient capacitor value modulation scheme is proposed instead of the conventional PWM and PFM schemes. As a result, it avoids quiescent power consumption.

3.1.2 Energy Efficient MPPT with the Hill-Climbing Algorithm

To realize the hill-climbing algorithm with limited power budget, an energy efficient MPPT module is proposed in Figure 32. It compresses logic steps and applies minimum devices, including two sample-and-hold (S/H) channels, comparator, digital controller, and modulated capacitor bank.

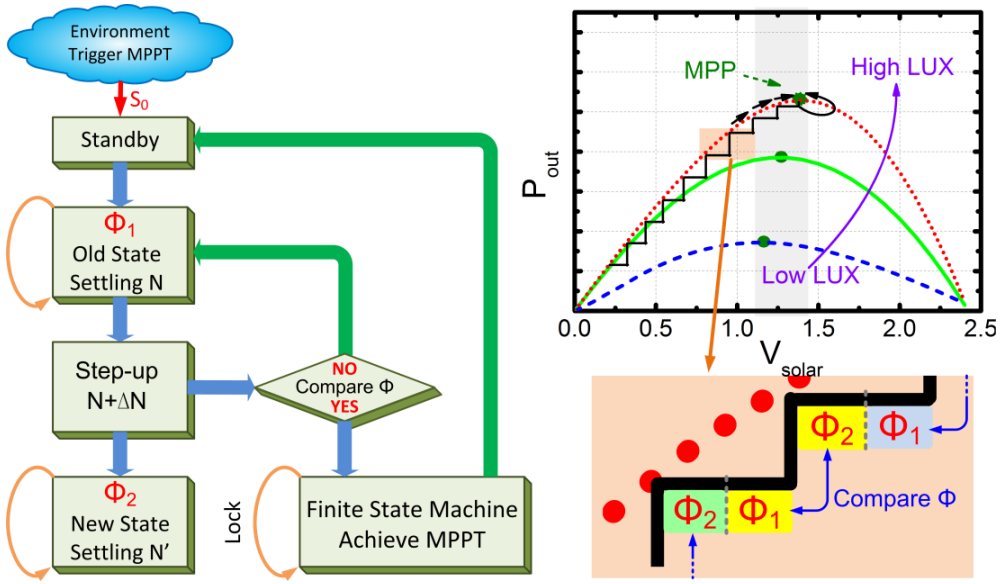


Figure 33. Flow chart of adaptive MPPT, and MPP moving curve during tracking procedure.

Their functional flow chart and conceptual hill-climbing procedure are illustrated in Figure 33. An enable signal S_0 triggers the MPPT procedure, which is provided by a periodic timer or an environmental sensor of the WSN. As shown in Figure 33, the sensing phases are divided into two, Φ_1 and Φ_2, by tracking the power information of old and new slots. Each phase requires several clock cycles to reach a steady state. After that, Φ_1 and Φ_2 are compared through the low power comparator. The comparator latches and indicates whether the new tentative tuning step is improving or not. A digital

controller is used to control the entire system, as well as to communicate with other IoT smart nodes.

3.1.3 Capacitor Value Modulation

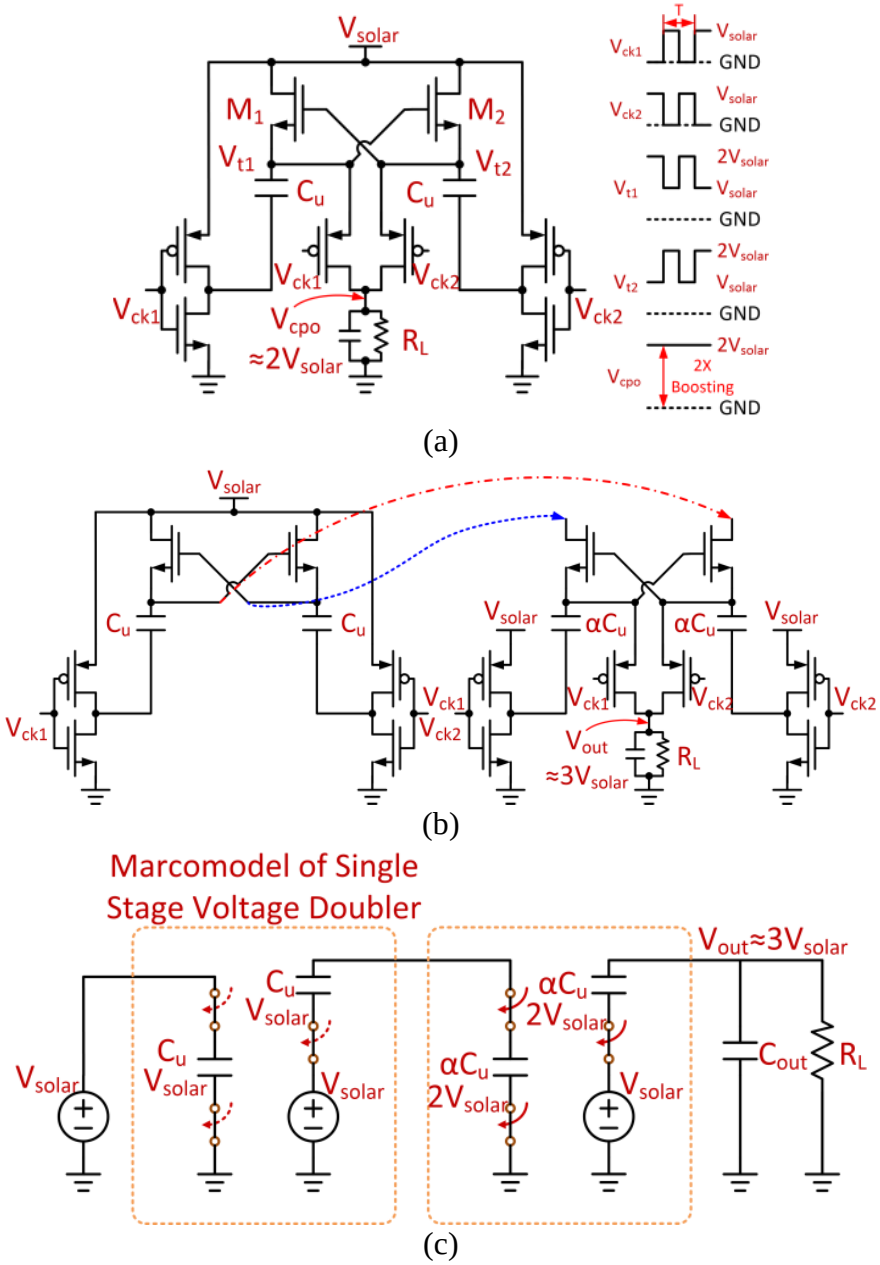


Figure 34. (a) Principle of the voltage doubler, (b) the nested voltage tripler built with 2 voltage doublers, (c) macromodel of the voltage tripler.

A voltage doubler shown in Figure 34(a) features minimum components for required conversion ratio (CR). With complementary switching clocks V_{ck1} and V_{ck2}, the converter charges the solar cell voltage V_{solar} across C_u then levels up its negative plate by the same potential. In a steady state, the resulting output voltage V_{cpo} is twice of the input voltage V_{solar}. However, only one stage with twice 2× CR is not enough between the photovoltage 1-1.5 V when the smart node loads such as SOC typically requires minimum 3 V supply. Thus, as shown in Figure 34(b), two voltage doublers are nested and the second doubler has one modified input from V_{solar}, resulting in a CR of 3. The steady state macromodel can be simplified by neglecting parasitics as shown in Figure 34(c). α is the capacitor ratio factor between the second and first stage. Applying the principle of charge conservation,

$$[2\mathrm{V_{solar}} - (\mathrm{V_{out}} - \mathrm{V_{solar}})] \times \alpha \mathrm{C_u} = \frac{1}{2} \times \frac{\mathrm{T} \times \mathrm{V_{out}}}{\mathrm{R_L}} \tag{27}$$

where the T, R_L stands for switching clock period and equivalent load resistance of SOC respectively. Due to the buffer and filter function of the supercapacitor, the load voltage V_{out} is DC. Thus V_{solar} can be expressed as a function of multiple variables, yielding

$$V_{solar} = \left(\frac{1}{2} \times \frac{T}{R_L} \times \frac{1}{\alpha C_u} + 1\right) \times \frac{1}{3} \times V_{out} \xrightarrow{Match} V_{MPP} \tag{28}$$

Without any loading effect, the theoretical ratio between input and output voltages is 1:3. With variable loads, the input voltage V_{solar} can be tuned by 2 parameters to match the maximum power point V_{MPP} of solar cell: switching frequency f_s=1/T and switching power capacitor C_u. Although firstly proposed in charge pump power converter, the capacitor value modulation was used for load regulation [84]. In this

energy harvesting system of IoT smart nodes, we propose the variable C_u to do the impedance tuning for MPPT. The generation of variable f_s usually needs complex auxiliary circuits and consumes a significant amount of power, thus affecting the efficiency of the harvester system [42]. Therefore, the approach of the power capacitor tuning with fixed fs is chosen for three major benefits. i) The power capacitor can be digitized into a bank of multiple value capacitors. The passive components do not consume quiescent power and its digital controller needs little dynamic power. Such intrinsic characteristics guarantee the high efficiency of the converter. ii) The constant switching frequency f_s gives predictable noise spectrum and alleviates the EMI problems on the sensor loads. iii) The increase of chip area due to the programmable capacitor is minimal, because the low harvested energy only requires small size on-chip capacitors, taking 1.03 mm^2 active area with IBM 0.18-µm process. It can also be scaled down with other CMOS technologies.

3.1.4 Efficiency Limit by the Charge Redistribution Loss

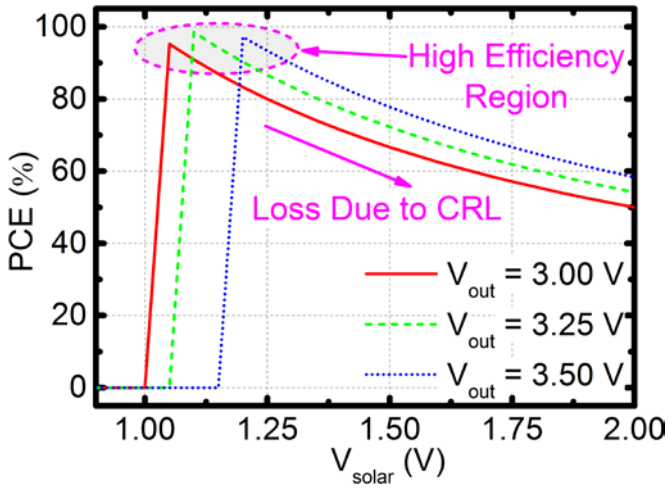


Figure 35. Power conversion efficiency (PCE) vs. V_{solar} with 3-3.5 V V_{out}.

The switched capacitor topology causes an inevitable charge redistribution loss (CRL) [85]. The affected power conversion efficiency (PCE) of the charge pump can be estimated as,

$$PCE = \frac{V_{out}}{V_{solar} \times CR} \times 100\% \quad (29)$$

where CR is the conversion ratio and equals to 3 for this specific topology. The PCE with various input and output voltages is shown in Figure 35. The result indicates that the ratio between V_{out} and V_{solar} should not deviates much from CR = 3 to avoid the CRL affecting the PCE. Because V_{out} is pinned to 3-3.5 V by the output supercapacitor or battery, the MPPT matched V_{solar} should be in the vicinity of 1-1.5 V to achieve a high PCE with minimum CRL.

3.2 Energy Efficient MPPT

3.2.1 Architecture of the Energy Harvester with Time-domain MPPT

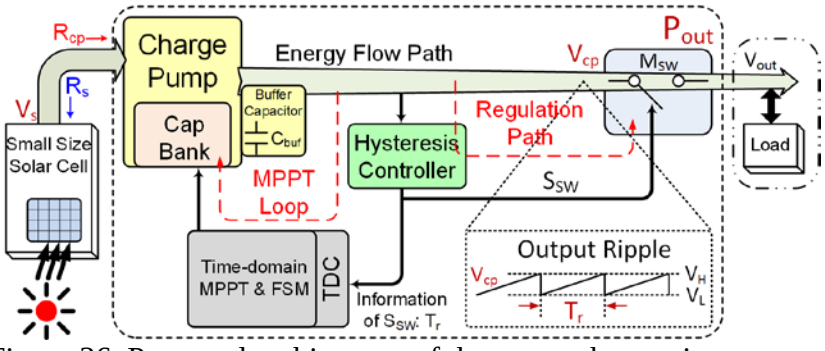


Figure 36. Proposed architecture of the energy harvesting system.

The architecture of the proposed adaptive energy harvesting system is shown in Figure 36. The system consists of one forward path for energy delivery and two control

paths: one for MPPT and one for regulation. In the forward path, as a direct interface to the PV cell, the charge pump boosts the PV output voltage V_s to the required level and delivers the harvested PV power Pout to the loads. To achieve maximum power transfer, a dynamic MPPT algorithm is necessary to track the variable output resistance R_s of the PV cell. The hill-climbing algorithm of MPPT, which is executed by the MPPT loop, as shown in Figure 36, is chosen to minimize the hardware complexity and power consumption [41]. Once the sensed power information is available, a finite-state machine (FSM) executes the hill-climbing algorithm to tune the equivalent resistance R_{cp} of the charge pump and searches for the MPP. As will be discussed in Section 3.2.2, R_{cp} is defined by the inverse product of switching frequency f_s and capacitor values C_u. To tune C_u, an energy-efficient CVM scheme is proposed instead of the conventional frequency modulation scheme, avoiding quiescent power consumption.

When illumination is weak, the PV source cannot continuously power the loads of the smart nodes. To avoid such a harmful loading effect, the loads are periodically turned on and off; thus, they cannot provide V_{out} as a continuously available parameter for sensing and regulation. As a solution, we propose to sense the pumped voltage V_{cp} of the charge pump as illustrated in Figure 36; hence, a feedforward path of hysteresis regulation is applied to directly manage V_{cp} to power the loads. The harvested PV energy is temporarily stored in a buffer capacitor C_{buf} at the output of the charge pump. By comparing its voltage V_{cp} with a high reference V_H and a low reference V_L, the regulation scheme turns on and off the M_{SW} switch, respectively, as shown in the inset of Figure 36. The values of V_H and V_L are determined by the requirement of the loads. As a

result, this feedforward path does not rely on V_{out}, preventing the loads from draining off the harvesting system.

As will be discussed later, the one-shot hysteresis controller in Figure 36 utilizes less complex circuits than conventional PWM schemes. Its quiescent power consumption can be eliminated and fitted for ultra-low power application. The controller can also be reused for time-domain MPPT, where the rising time T_r is inverse of the harvested PV power P_{out}. Thus, the power information of the PV cell can be quantified and efficiently processed in the time-domain through a time-to-digital converter (TDC), avoiding the power hungry current sensor. The sensing theory is detailed in Section 3.2.4.

3.2.2 3× Charge Pump with CVM

The 3.3 V LVTTL is a widely used standard in commercial ICs for the smart nodes. A one-stage doubler only boosts a PV voltage of V_s = 1.1-1.5 V to a maximum of 3 V, which is not enough to drive loads with standard LVTTL of 3.3 V. In principle, the voltage doubler is a circuit that adds two input voltages. We can use this fact to implement $2V_s+V_s$ by nesting two voltage doublers as shown in Figure 37(a). The second doubler has one modified input from the PV operating voltage, V_s, resulting in a total boosting gain of 3. Note that the structure can also be viewed as two 3× Dickson charge pumps driven by complementary clocks. Its operating waveforms are shown in Figure 37(a),

1) When CLK_1 = 0 (logic) and CLK_2 = 1 (logic): M_1, M_3, and M_{P2} are turned off. M_2, M_4, M_{P1} are turned on. $V_{t1} = 2V_s$, $V_{t2} = V_s$, and V_{out} is charged to $3V_s$ through M_{P1}.

2) When $CLK_1 = 1$ and $CLK_2 = 0$: M_2, M_4, and M_{P1} are turned off. M_1, M_3, M_{P2} are turned on. $V_{t1} = V_s$, $V_{t2} = 2V_s$, and V_{out} is charged to $3V_s$ through M_{P2}.

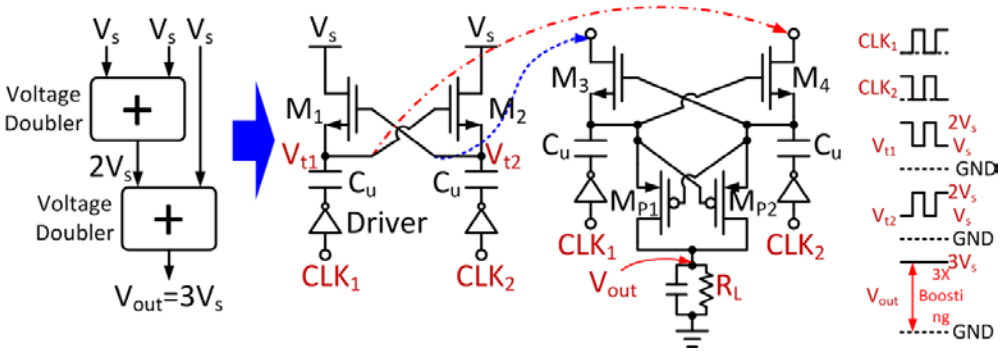


Figure 37. (a) Generic structure of the nested voltage tripler built with 2 voltage doublers, (b) macromodel of the 3× charge pump, and (c) the programmable capacitor bank.

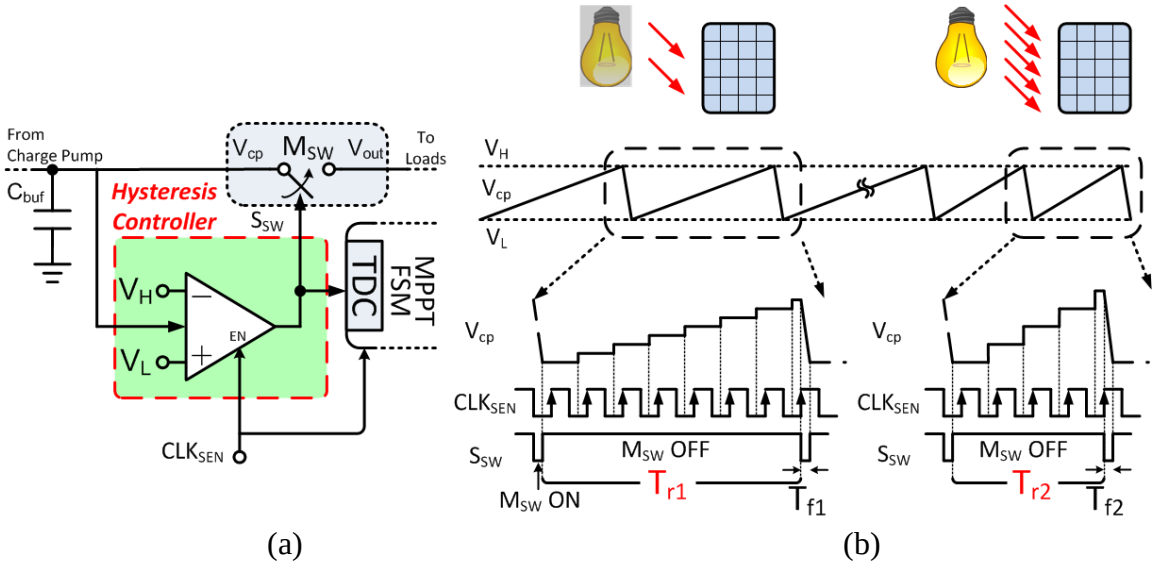
The charge pump can be modeled as an ideal 1:3 DC transformer in series with an equivalent resistor R_{cp} [50] as shown in Figure 37 (b). R_{cp} can be calculated as,

$$R_{cp} = \sum_{i \in caps} \frac{(\alpha_i)^2}{f_s C_i} = \frac{1}{f_s C_u} \tag{30}$$

where α_i is the charge multiplier coefficient [86] and equals to 0.5. According to (30), R_{cp} is determined by two parameters: the switching frequency f_s and the switching power capacitor C_u. The generation of variable fs usually needs complex auxiliary circuits and

consumes quiescent power, thereby affecting the efficiency of the harvester system [42]. Therefore, the CVM approach of C_u tuning is chosen to avoid quiescent power as shown in Figure 37(c), where C_u consists of a fixed part C_S and N parallel capacitors of value C_P. By switching the programmable capacitor bank, the C_u value changes from C_S up to (C_S+N×C_P).

3.2.3 Hysteresis Output Regulation



(a) (b)

Figure 38. (a) Architecture of the hysteresis controller and (b) the operating waveforms.

The block-level structure of the hysteresis controller in Figure 36 is depicted in Figure 38(a). Its operating waveforms are shown Figure 38(b). V_{cp} is connected to V_{out} through a passing switch M_{SW}. S_{SW} is the command signal given by the hysteresis regulation. Once V_{cp} is higher than V_H, M_{SW} is turned on to discharge the buffer capacitor C_{buf} toward the loads. Once V_{cp} is below VL, M_{SW} is turned off and C_{buf} is charged by the 3× charge pump.

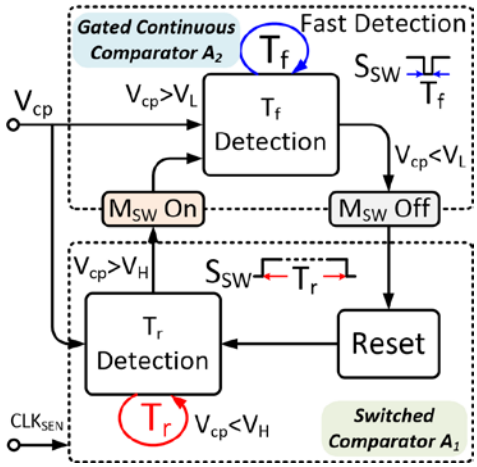


Figure 39. Self-triggered one-shot mechanism of the hysteresis controller.

Moreover, the conventional hysteresis detection in Figure 38(b) has a tradeoff between speed and power consumption. The rising time $T_{r1,2}$ is a slow moving signal, which can easily be detected by such a low speed latched comparator. However, the falling time $T_{f1,2}$ is a fast moving signal, which requires a fast comparator. Thus, we do not use the conventional comparator depicted in Figure 38(a). An architectural solution is proposed via a self-triggered one-shot mechanism to control M_{SW}. T_r detection is fulfilled by a switched comparator for better harvesting efficiency; T_f detection is achieved by a high speed comparator, which is gated by a one-shot mechanism to limit its energy cost. Its mechanism is illustrated in Figure 39. Firstly, M_{SW} is turned off. The charge pump output voltage is $V_{cp} < V_H$, and is compared with V_H to detect T_r in a switched comparator A_1 without quiescent current. Its strobe clock, CLK_{SEN}, is depicted in Figure 38(b). Once $V_{cp} > V_H$, a high speed comparator A_2 and M_{SW} are turned on for $V_{cp} > V_L$. Because V_{cp} is quickly discharged to V_{out} through M_{SW}, T_f is detected as a one-shot time for $V_{cp} < V_L$, and A_2 is immediately turned off to save power. The hysteresis controller turns off M_{SW} and resets for the next T_r detection. Such a self-

triggered one-shot mechanism forms a fast loop and avoids an overkilling GHz trigger clock.

3.2.4 Time-domain Quantization for MPPT

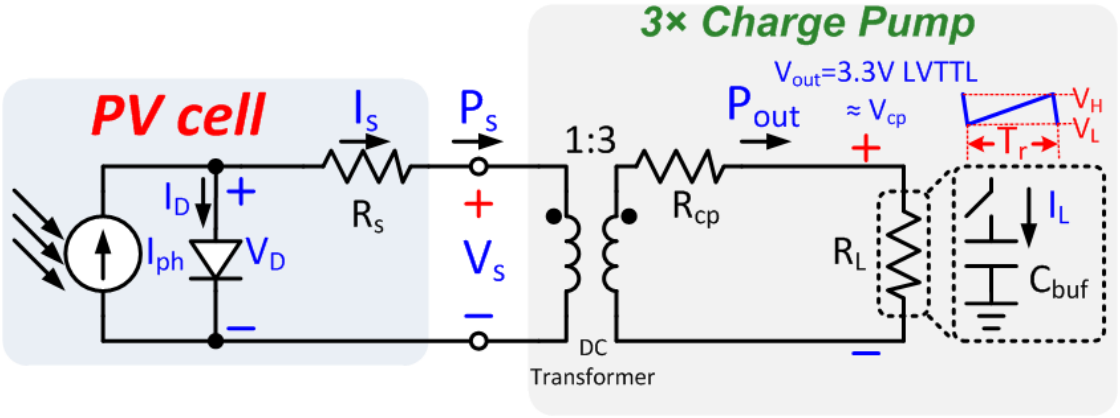


Figure 40. Pseudo-static model of a PV cell and charge pump power converter.

The signal S_{SW} from the regulation module in Figure 38(b) can be reused to indicate illumination intensity. Intuitively, high light intensity provides higher PV power and quickly charges C_{buf}. Its charging time T_{r2} is shorter than T_{r1} with low light intensity. $T_{r1,2}$ can be defined by S_{SW}. It can be counted and quantified by a TDC as shown in Figure 38(a) with the strobe clock CLK_{SEN}.

The quantitative relationship between the charging time T_r and P_{out} can be modeled via a steady-state assumption [87] as shown in Figure 40. The PV cell is characterized by the simplified single-diode model [88] as a light-controlled current source I_{ph} with a parallel diode and a series resistor R_s.

$$\begin{cases} KCL: I_{ph} - I_D - I_s = 0 \\ Diode: I_D = I_{sat}\left(e^{V_D/V_T} - 1\right) \\ KVL: V_s = V_D - R_s I_s \end{cases} \tag{31}$$

Notations are explained as follows:

I_{ph}: photocurrent, I_{sat}: diode saturation current, V_T: thermal voltage, R_s: PV series resistor provided by the manufacturer, I_D: diode current, V_D: diode voltage, I_s: PV output current.

An equivalent resistor R_L models the buffer capacitor C_{buf} and its gated switch with the charging current I_L. According to the steady-state assumption, the ripple of V_{cp} between V_H and V_L is neglected, and V_{cp} equals to V_{out} as a constant voltage. Moreover, I_L can be averaged during the entire charging period T_r and expressed as,

$$I_L = \frac{C_{buf}(V_H - V_L)}{T_r} \tag{32}$$

Applying Kirchoff's voltage law at the input node of the DC transformer,

$$V_s = V_D - 3I_L R_s = \frac{V_{out} + R_{cp} I_L}{3} \tag{33}$$

Solving (31) and (33) permits the equation to only have I_L,

$$I_{ph} - I_{sat}\left(e^{\frac{\frac{V_{out}+R_{cp}I_L}{3}+3I_L R_s}{V_T}} - 1\right) - 3I_L = 0 \tag{34}$$

Due to the PV's nonlinearity, such type of equation does not have a closed-form solution. A possible solution can be obtained using an iterative scheme [89]. Thus, we approach the solution in a different way. In the time-domain, the harvested power P_{out} can be simply represented by,

$$P_{out} = V_{out} I_L = V_{out} \cdot \frac{C_{buf}(V_H - V_L)}{T_r} \tag{35}$$

Note that P_{out} is inverse-proportional to the rising time T_r. Therefore, we use T_r to indicate the trend of P_{out}, and convert the MPPT power sensing problem into the time-domain without conventional power sensors [42]. The reused variable T_r can be simplified from (32) and (33) as,

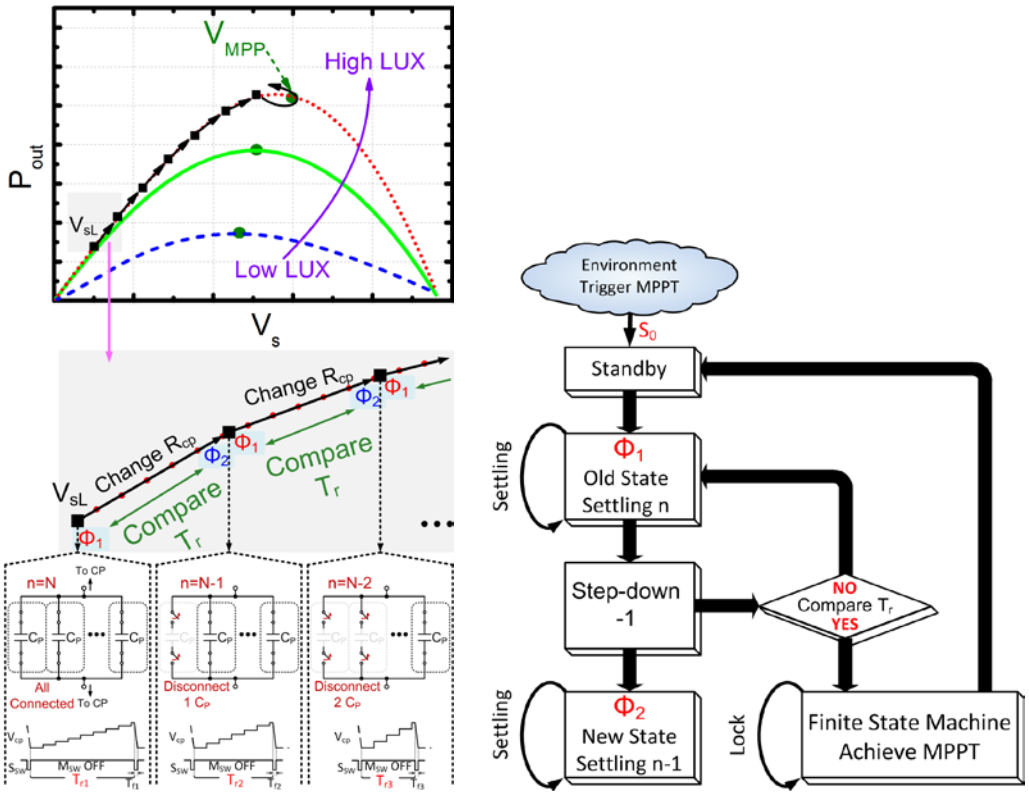
$$T_r = \left(\frac{R_{cp}}{3} + 3R_s\right) \times C_{buf} \times (V_H - V_L) \times \frac{1}{V_D - \frac{1}{3}V_{out}} \tag{36}$$

Note that V_D is still a non-closed-form expression of R_{cp}. By setting different C_u, R_{cp} is changed and results in different T_r. T_r will be recorded by the TDC in FSM, and reused by the hill-climbing MPPT as follows.

3.2.5 Hill-Climbing Algorithm

The operation of a PV cell is depicted in Figure 41(a). The maximum power point is determined by various factors including illumination conditions and fabrication technology. Generally, V_{MPP} increases with increasing light intensity. A FSM executes the hill-climbing tracking flow as shown in Figure 41(b). n represents the number of parallel connected capacitors in a programmable bank. Once the MPPT procedure is triggered, the FSM initializes the charge pump with a low boundary voltage V_{sL}. All capacitors in the bank are connected as n=N, and R_{cp} reaches its minimum value at $\frac{1}{f_s(C_S+N\times C_P)}$. The first sensing state Φ_1 records the power information in the form of T_{r1}. Then one programmable capacitor, CP, is tentatively disconnected as n=N-1, and R_{cp} is increased through (30) as $\frac{1}{f_s[C_S+(N-1)\times C_P]}$. The second sensing state Φ_2 records the new

T_{r2} with the tentative R_{cp}. Based on the characteristics of the PV cell, a different R_{cp} will cause different PV operating voltages, V_s through (33). It will also change the harvested power P_{out}, which is a function of T_r^{-1}, as shown in (35). By comparing T_r of neighboring two steps in Figure 41(a), the finite-state machine (FSM) gets the trend that the tentative R_{cp} tuning is improving or degrading P_{out}. If T_r keeps decreasing, MPP is not captured and the FSM examines the next value of the capacitor bank as n=N-2. Once T_r stops decreasing, MPP is achieved and the FSM stops the searching procedure. Finally, the charge pump is locked at the optimal operating state Φ_2 with minimum T_r and maximum P_{out}.



(a) (b)

Figure 41. (a) Electrical characteristics of a PV cell under different illumination conditions and (b) flow chart of the adaptive MPPT for the PV harvesting system.

Different from the conventional perturb & observe (P&O) approach, the developed hill-climbing algorithm is unilateral. Therefore, it does not have a common stability problem as oscillating around MPP [90]. Although the unilateral monotonic hill-climbing algorithm is not as accurate as the P&O approach and suffers a small power loss from the PV cell, it has less complexity and saves power consumption of control circuits.

3.3 Two-dimensional MPPT

3.3.1 Architecture of the Proposed Energy Harvester

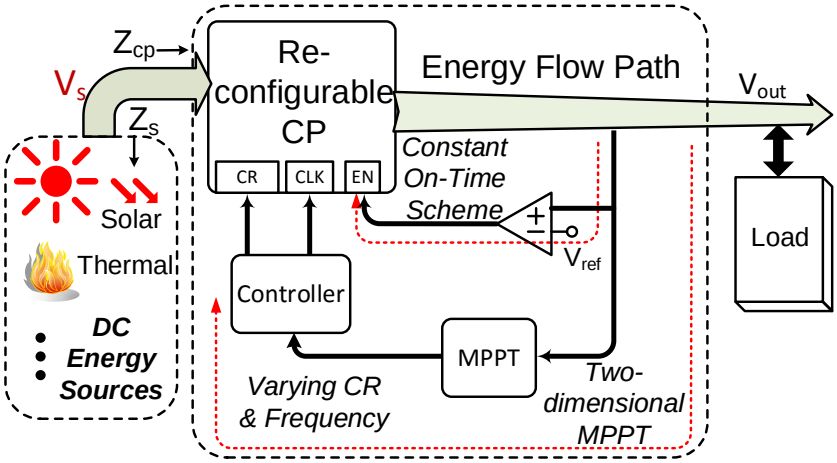


Figure 42. Proposed architecture of the reconfigurable energy harvester.

The architecture of the proposed 2-D energy harvesting system is shown in Figure 42. The input can be arbitrary DC energy sources such as the photovoltaic (PV) or thermoelectric generator (TEG). The output load consists of a storage capacitor and functional modules of IoT smart nodes, such as signal processor, sensors, and wireless transceiver.

In the proposed charge pump energy harvester, there are one forward path for energy delivery and two feedback paths: one for MPPT and one for output voltage regulation. In the forward path, the charge pump boosts the input voltage to the required level and delivers the harvested energy to the loads. The charge pump is reconfigured with different CRs for various input/output voltages and minimizes the CRL, which is discussed in Section 3.3.2.

The inner loop uses a COT topology to regulate the output voltage V_{out}. Compared with PWM or PFM, the COT scheme features a simpler structure, and its regulated output voltage V_{out} can be reused as the output power indicator. Such an architecture eliminates the conventional power hungry current sensor and significantly saves on power consumption, which is discussed in Section 3.3.3. The outer loop executes the hill-climbing algorithm to keep the energy harvester operating at optimal harvesting voltage V_s and ensure maximum power transfer. More specifically, the reconfigurable feature of the charge pump is incorporated in the MPPT with the switching frequency f_s tuning, and results in a two-dimensional MPPT procedure for wide input voltage range. Its principle is detailed in Section 3.3.4.

3.3.2 Charge Redistribution Loss and Reconfigurable Charge Pump

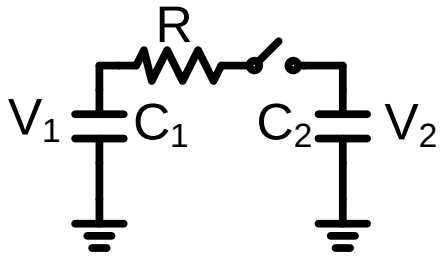


Figure 43. Macromodel for the charge redistribution loss.

The charge redistribution loss (CRL) is inevitable in switched capacitor type power converters [85]. To illustrate this principle, two capacitors, C_1 and C_2, with different initial voltages, V_1 and V_2, are connected with a switch as shown in Figure 43. The parasitic resistance of the switch is modeled as R. Once closing the switch, the CRL can be derived from the law of charge conservation as,

$$E_{loss} = \frac{1}{2}\frac{C_1 C_2}{C_1 + C_2}(V_1 - V_2)^2 \tag{37}$$

From (37), the CRL is irrelevant to R, but depends on capacitor values and voltage ripple, V_1-V_2. Therefore, minimizing the voltage ripple is the key issue of the charge pump power converter, which reduces the conversion loss and improves harvesting efficiency [49].

In energy harvesting for IoT, however, the voltage ripple is defined by the variable harvesting voltage V_s, the regulated output voltage V_{out}, and the CR of the power converter [91]. A voltage conversion efficiency (VCE) can be calculated as,

$$VCE = \frac{V_{out}}{CR \times V_s} \times 100\% \tag{38}$$

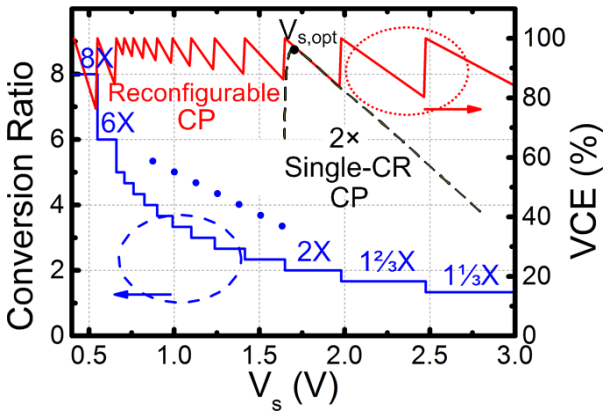


Figure 44. Influence of conversion ratios upon the harvesting efficiency.

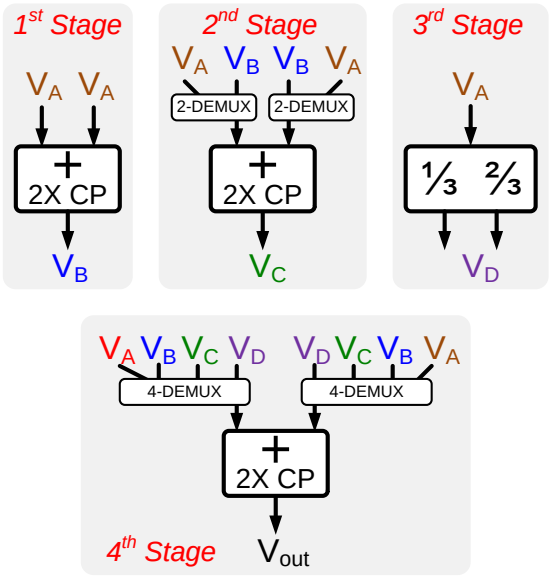


Figure 45. Conceptual diagram of the reconfigurable charge pump.

Figure 44 shows the general correlation between the CR and the VCE with a fixed 3.3 V load voltage. The black dashed line represents a fixed 2× charge pump, which shows a sole efficiency peak at an optimal input voltage $V_{s,opt} \approx V_{out}/CR$. Below $V_{s,opt}$, the VCE is zero, which means the input voltage is too small to be boosted to the required voltage level in any case. Above $V_{s,opt}$, the VCE decreases with increasing V_s due to the CRL. To solve the CRL for various harvesting voltages and achieve high harvesting efficiency over a wide range of V_s, the reconfigurable feature is proposed to dynamically tune the CR of charge pump. The proposed reconfigurable charge pump, as shown in Figure 45, stems from cascading basic voltage doublers. Such a structure features least the utilized capacitors for maximum CR; thus, it is favorable for a compact monolithic charge pump [92].

Note that each basic voltage doubler combines two input voltages to the output voltage as a voltage adder. By cascading three such doublers and properly selecting their input connections through a 2-way demultiplexer and 4-way demultiplexer, integral CRs as 1×, 2× up to 8× can be obtained at V_{out}. The fractional CR is realized by a reconfigurable step-down charge pump with CRs as ⅓× and ⅔×. Its output is included in the 4-way demultiplexer and results in mixed CRs as 1⅓×, 1⅔× up to 8× as the blue solid staircase shown in Figure 44. The resulting VCE is plotted with red solid line. The additional segments generate more VCE peaks and effectively guarantee a VCE higher than 80%. For low input V_s between 0.45 to 0.7 V, the integral CRs as 6×, 8× are fine enough for VCE > 78% and does not require fractional CRs, which increases circuit complexity and power consumption.

3.3.3 Constant-on Time Regulation and Power Sensing

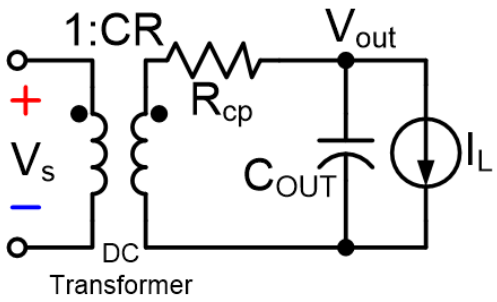


Figure 46. Pseudo-static macromodel of the charge pump.

The MPPT procedure ensures maximum power transfer from energy sources to the loads by changing the equivalent resistance of the power converter. In this particular application, the reconfigurable charge pump can be modeled as a DC transformer as shown in Figure 46 through the pseudo-static assumption [87], where R_{cp}, C_{OUT}, and I_L

represent the equivalent resistance of the charge pump, the output capacitance, and the load current consumption.

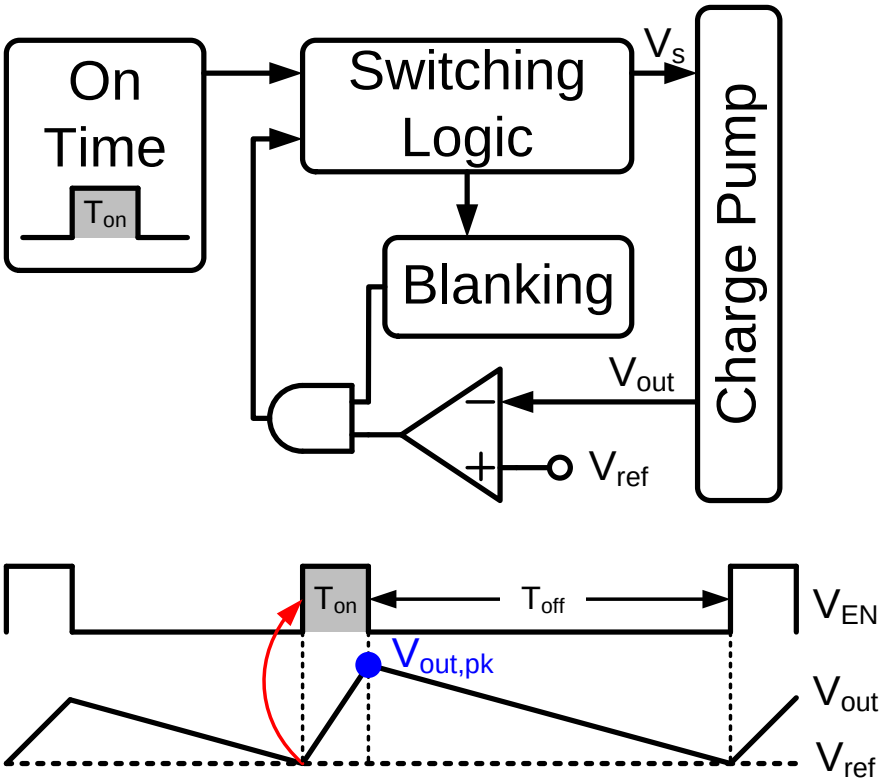


Figure 47. Conceptual diagram of the constant-on (COT) time regulation and waveforms.

The conceptual diagram and operating waveforms of the COT regulation is illustrated in Figure 47. The charge pump is firstly operated by T_{on} that is defined by a counter in Section 4.3.1.3. Then, V_{out} is compared with an external reference, V_{ref} = 3.3 V LVTTL. V_{ref} can also be internally generated by the monolithic IoT smart nodes. If $V_{out} > V_{ref}$, the charge pump is halted and waits until V_{out} discharged to the loads. If $V_{out} < V_{ref}$, the CP is enabled for switching and power conversion. The peak output voltage $V_{out,pk}$ at the end of T_{on} clocks can be derived as [54],

$$P_{out,avg} = \frac{0.5 \times C_{OUT}\left(V_{out,pk}^2 - V_{ref}^2\right)}{T_{on} + T_{off}} \tag{39}$$

where $P_{out,avg}$ represents the averaged output power. The Ton is defined by the COT regulation as $T_{on} = n/f_s$, where n is implemented as 16. This will be further discussed in Section 4.3.1.3. The variable off-time T_{off} can be calculated by disconnecting the primary stage of the macromodel in Figure 46 as,

$$T_{off} = \frac{C_{OUT}\left(V_{out,pk} - V_{ref}\right)}{I_L} \tag{40}$$

The on-time T_{on} can be related to $V_{out,pk}$ by considering the primary stage in Figure 46 and giving a weakly nonlinear ordinary differential equation (ODE) as,

$$C_{OUT}\frac{dV_{out}}{dt} + I_L = \frac{V_s \times CR - V_{out}}{R_{cp}} \tag{41}$$

Note that V_s is a nonlinear function due to the nature of energy sources. With a slow changing environment assumption and small ripple approximation, Vs can be viewed as constant and (41) becomes a linear ODE with below boundary conditions,

$$\begin{cases} V_{out}(0) = V_{ref} \\ V_{out}(T_{on}) = V_{out,pk} \end{cases} \tag{42}$$

The solution for T_{on} is given as,

$$T_{on} = ln\frac{V_s \times CR - V_{ref} - I_L R_{cp}}{V_s \times CR - V_{out,pk} - I_L R_{cp}} \times C_{OUT} R_{cp} \tag{43}$$

By rearranging (39), (40), and (43),

$$P_{out,avg} = \frac{0.5 \times C_{OUT}\left(V_{out,pk}^2 - V_{ref}^2\right)}{ln\frac{V_s \times CR - V_{ref} - I_L R_{cp}}{V_s \times CR - V_{out,pk} - I_L R_{cp}} \times C_{OUT} R_{cp} + \frac{C_{OUT}\left(V_{out,pk} - V_{ref}\right)}{I_L}} \propto \frac{V_{out,pk}^2}{ln\, V_{out,pk} + V_{out,pk}} \quad (44)$$

Thus, $P_{out,avg}$ monotonically increases with $V_{out,pk}$. In other words, the voltage information of the COT regulation indicates the trend of the harvested power and can be reused in the MPPT procedure.

3.3.4 Principle of the Two-Dimensional MPPT

The equivalent resistance [86] of the charge pump in Figure 46 is derived as,

$$R_{cp,prim} = \frac{1}{CR^2} \times \sum_{i \in caps} \frac{\left(a_{c,i}\right)^2}{f_s C_i} \quad (45)$$

where $a_{c,i}$ represents the charge multiplier. According to (45), $R_{cp,prim}$ is determined by three parameters: the conversion ratio CR, switching frequency fs, and used capacitor value C_i. Tuning utilized capacitor values typically requires a capacitor bank and a large chip area; thus, such tuning is not cost-efficient in full integration. Conventional MPPT schemes change $R_{cp,prim}$ by tuning f_s as a one-dimensional MPPT [42]. In this work, the proposed architecture has the added flexibility of CR tuning. Thus, it can be combined with the fs tuning as a two-dimensional MPPT procedure, resulting in an adaptive energy harvesting capability for wide input range.

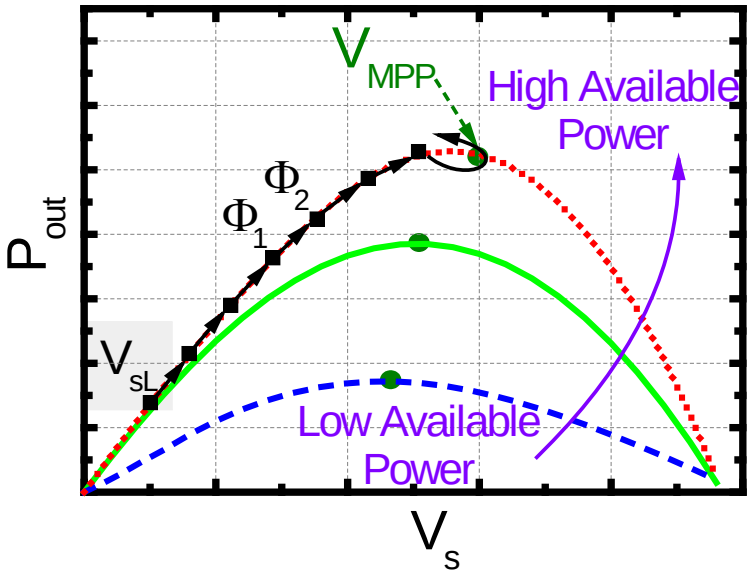


Figure 48. Generic nonlinear characteristics of energy sources and the hill-climbing MPPT algorithm.

Generic nonlinear characteristics of energy sources are demonstrated in Figure 48. For different input power, the harvested power Pout and optimal harvesting voltage V_{MPP} are shifted. A hill-climbing algorithm was developed to start searching from a low boundary voltage V_{sL} with maximum CR and f_s. Then $R_{cp,prim}$ was changed by reducing CR or fs according to (45). Before and after each tentative change, P_{out} of the two harvesting states, Φ_1 and Φ_2, are compared to determine whether the maximum P_{out} is achieved or not.

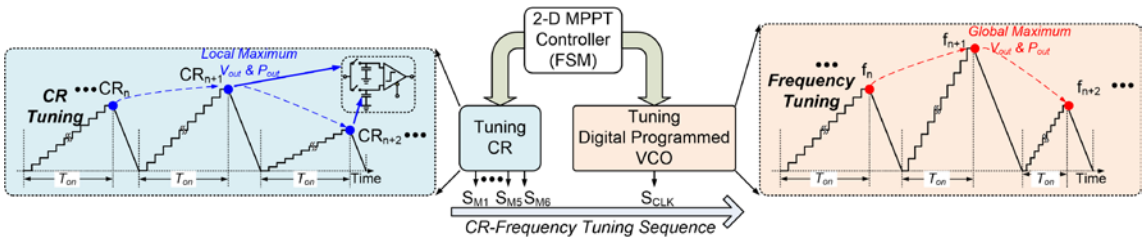


Figure 49. Flow chart of the two-dimensional MPPT with COT control.

The detailed two-dimensional MPPT procedure and waveforms are proposed as Figure 49. The MPPT is split into two periods. Due to the quadratic correlation between CR and $R_{cp,prim}$ in (45), the CR is firstly swept as one-dimensional coarse tuning. It was stepped from 8× down to 1⅓× with fixed f_s to find the local maximum P_{out}. Then, as another one-dimensional fine tuning, f_s is stepped from f_n down to f_{n+1} to find the global maximum P_{out}.

As discussed in Section 3.3.3, the magnitude of P_{out} is not directly sensed but indirectly monitored via V_{out}. Therefore, at the end of each T_{on}, $V_{out,pk}$ is detected by a 2-channel S/H circuit and compared by a low power latched comparator as shown in Figure 49. Such a sensing scheme reuses the information from the COT regulation, eliminates the power hungry current sensor, and effectively improves the harvesting efficiency.

3.4 Conclusion

In this section, three MPPT topologies are demonstrated for nonlinear energy sources. The PV cells are taken as example for the design. Firstly, originated from the conventional analog current sensing, an improved analog current sensor with switched control was developed for saving power. Instead of active impedance tuning, a CVM method was proposed to reduce the power consumption for better efficiency. Secondly, to further reduce the quiescent power consumption of the analog current sensor, a digital power sensor was developed to execute the MPPT in time-domain. Thirdly, the resistance variety of the nonlinear energy sources is taken into consideration. To better

match it, the switched capacitor power converter is tuned in both switching frequency and boosting architecture.

4 CIRCUIT DESIGN TECHNIQUES AND IMPLEMENTATIONS*

The three different MPPT topologies in Section 2 are implemented in Section 4.1, 4.2, and 4.3 separately. The Section 4.4 is an enhanced implementation for self-startup and self-sustaining capabilities. Moreover, a single-cycle regulation and MPPT scheme is developed for eliminating the on-chip storage capacitor and saving cost.

4.1 EH System with Current Sensor and CVM MPPT

4.1.1 Circuit Implementation & Design Procedure

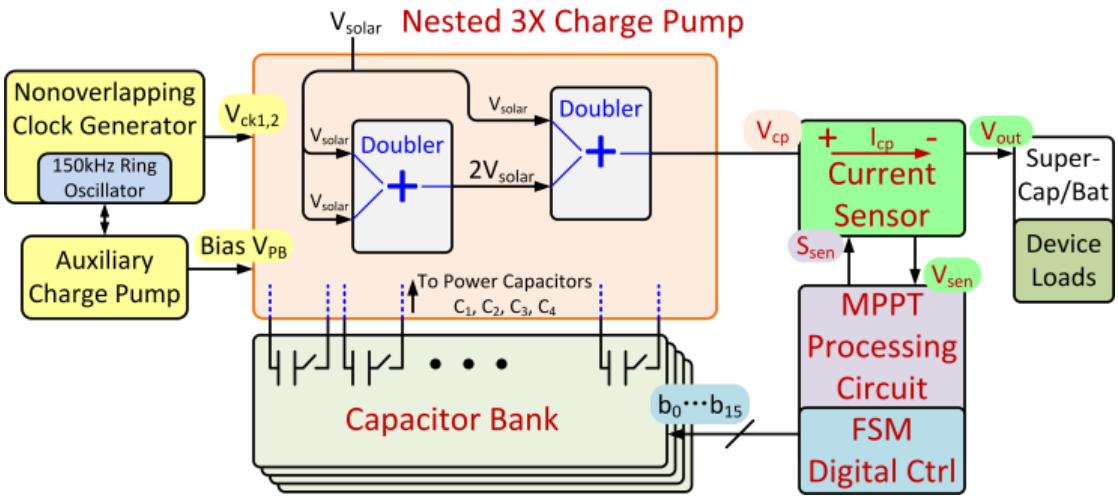


Figure 50. Conceptual block diagram of the proposed energy harvesting system.

The proposed energy harvesting system depicted in Figure 32 is implemented with conceptual blocks as Figure 50, and will be discussed block by block in following.

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4.1.1.1 Nested Voltage Tripler

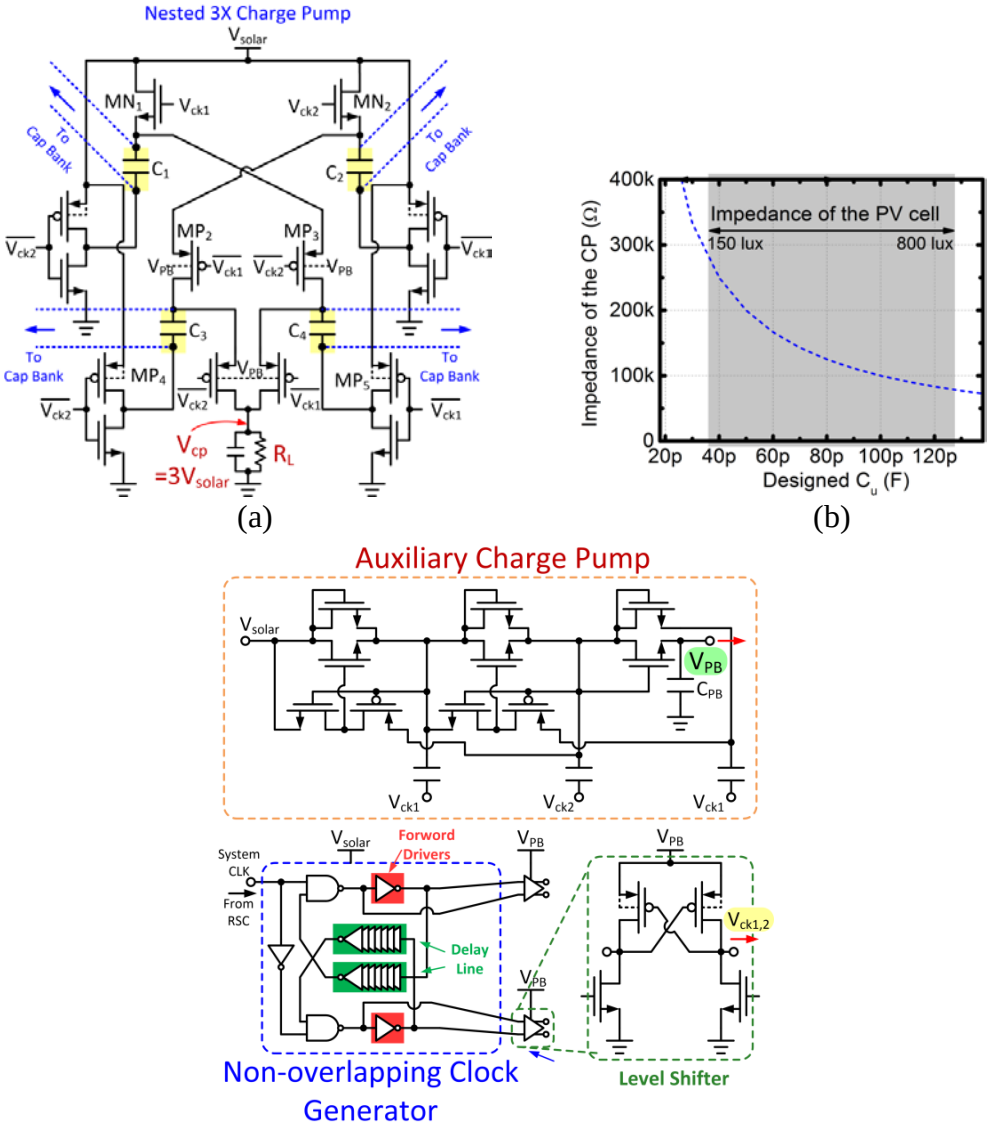


Figure 51. (a) Detailed structure of the nested voltage tripler, (b) impedance of the charge pump Z_{cp} with designed C_u values vs. impedance of PV cell Z_{solar} under different light intensities, and (c) auxiliary charge pump, non-overlapping clock generator, and level shifter.

The Dickson charge pump is widely used in solar energy harvesting. However, it provides a low voltage conversion ratio. Therefore, a CR-improved structure of nested

voltage tripler is chosen as shown in Figure 51(a). The first stage provides two times voltage boosting and the nested second stage provides 1.5 times voltage boosting, resulting in an overall CR of three. In Figure 34(a), the switch transistors M_1 and M_2 are cross-connected and self-switched. However, such architecture limits the turn-on voltage of NMOS transistors to less than V_{solar}, which ranges from 1 to 1.5 V. The low turn-on voltage drastically increases the conduction resistance and degrades the boosting efficiency. To generate enough gate overdrive, we propose to break the cross-connected gate and drive them with higher voltage separately. Moreover, the direct driving scheme does not have several coupled parasitic issues and the need for damping branch compared with the self-switching scheme [93].

The impedance of the proposed charge pump can be extracted from the model in Figure 34(c) as,

$$Z_{cp} = \frac{V_{solar}}{I_{in}} = \frac{1}{2f_s C_u} \frac{1+\alpha}{\left(3 - \frac{V_{out}}{V_{solar}}\right)\alpha} \tag{46}$$

which verifies that the impedance of the charge pump is inversely proportional to fs and C_u. Thus, Z_{cp} and Z_{solar} under different light intensities are plotted in Figure 51 (b) with f_s = 150 kHz, V_{out}/V_{solar} = 2.6, and α = 4. With programmable C_u between 18 and 138 pF, the proposed charge pump successfully matches the impedance of PV cell under 150 to 800 lux.

In Figure 51(c), an auxiliary charge pump is used as a level shifter to generate $3\times V_{solar}$ switching signal for the voltage tripler. As a result, the NMOS transistors $M_{N1,2}$ have a gate drive voltage of $2\times V_{solar}$ during turn-on period. Additionally, the auxiliary

circuit, in Figure 51(c), will provide $3\times V_{solar}$ to all control circuit as a power supply and body bias. Due to the minimal gate capacitance of switches, the auxiliary charge pump has only 1/8 the size of the main voltage tripler to minimize the parasitics. All the switching clocks are provided by a non-overlapping signal generator shown in Figure 51(c), which eliminates the shoot-through current and improves the converter efficiency. Different from the conventional NAND based non-overlapping clock generator, a delay line is placed in the feedback path. Therefore, the forward drivers are designed to maximize their fan-out capability and minimize their power consumption. The non-overlapping time is tuned by the delay line independently.

To realize the self-sustaining feature for the adaptive harvesting system, the entire control unit is powered by the circuits in Figure 51(c). Thus, they also function as a startup module to help the system wake up. Once the solar cell is connected to the harvester, the ring oscillator begins to generate a switching clock. The auxiliary charge pump, in Figure 51(c), will quickly charge the self-sustaining capacitor C_{PB} to V_{PB} as a startup.

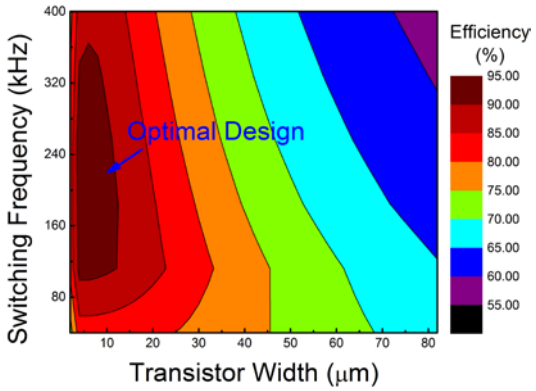


Figure 52. Efficiency trade-off between the power transistor gate width W_u and switching frequency f_s.

Detailed optimal design strategy can be derived for maximizing the efficiency. Referring to the steady state model, the total power loss of the power converter is determined by

$$P_{loss} = P_{cond} + P_{cap} + P_{CRL} \tag{47}$$

where P_{cond}, P_{cap}, and P_{CRL} stand for the conduction loss, the parasitic capacitor dynamic loss, and the charge redistribution loss, respectively. According to these boundaries, the optimized unit gate width can be calculated for the minimum total power loss. The optimal device dimension W_u is based on the switching frequency f_s and fabrication technology. Detailed efficiency tradeoff between f_s and W_u is simulated in Figure 52. Because the low harvested power only needs small active devices, the optimal f_s has a wide range due to their minimal parasitics. Referring to (5), the conduction loss of power transistors dominates. Thus, in the vicinity of maximum conversion efficiency, we choose f_s of 150 kHz as the design specification.

4.1.1.2 MPPT Mechanism and FSM Design

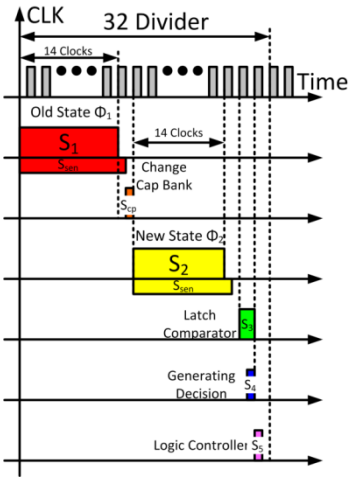


Figure 53. Designed time diagram of the MPPT controller.

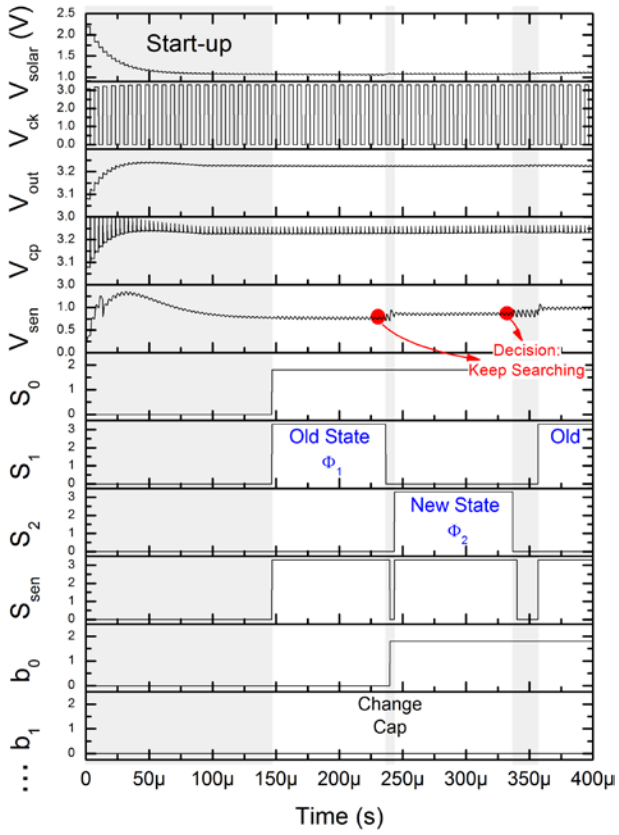


Figure 54. Simulated waveforms of the FSM for the MPPT procedure.

In Figure 50, the MPPT mechanism is implemented by 5 synchronous D-Flipflops and periphery logic gates. The clock timing diagram is shown in Figure 53, and its simulated operation is shown in Figure 54. One cycle of the MPPT procedure is executed during 32 clock periods. At the beginning of MPPT, all the capacitors in the bank are connected. The solar cell has the heaviest load and the FSM will disconnect those capacitors by the algorithm. After a number N is counted into the programmable capacitor bank, the harvesting system uses 14 cycles to settle down in this condition. At the end of the settling period, a power sensor captures the stabilized output current value, which is proportional to the harvested power P_n. A S/H circuit accurately samples P_n from power sensor during this period and holds the value by the falling edge of S_1. Half

a clock delay is given as the margin between sampling signal S_1 and sensing signal S_{SEN}. Once the value is held, the capacitor bank is configured to a new N' in the later half clock. Simultaneously, a reset and sample command S_2 is sent to another identical S/H circuit for another 14 clocks to follow the information of the new output power P_{n+1}. When Φ_2 for N' capacitor bank is finished, signal S_3 outputs the harvested power information for 2 clock periods, which means comparison ready. With signal S_4, the logic decision is generated through a latch. Finally, triggered by S_5, the FSM digital controller executes digital processing based on the result. As the signal flow chart shown in Figure 33, if P_{n+1} of the new state is larger than P_n of the old state, the FSM keeps searching the optimal point. Otherwise, the peak power has passed and the FSM goes back to state P_n so that the maximum power transfer is realized.

4.1.1.3 Ultra-Low Power Current Sensing Technique

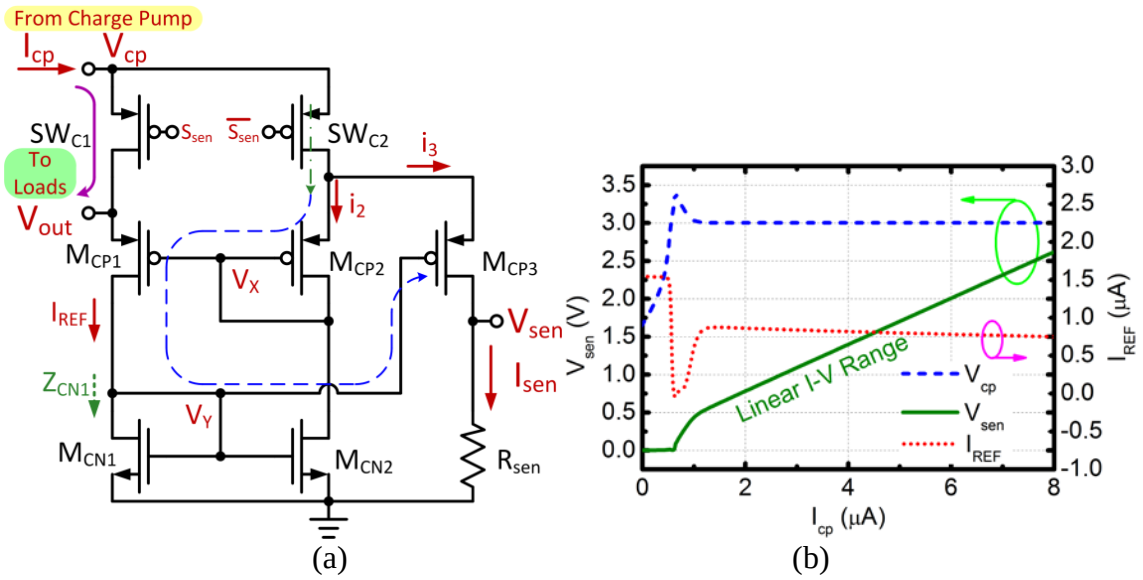


Figure 55. (a) Proposed structure of the current sensor, (b) characteristics of sensing voltage V_{sen}, reference current I_{REF} vs. throughput current I_{cp}.

As depicted in Figure 50, a current sensor instead of power sensor is used to monitor the harvested energy. However, most conventional current sensors are not specifically designed for ultra-low currents. By utilizing current mirrors and operational amplifiers, they cannot guarantee accurate current distribution against process variation and enough sensing sensitivity for this ultra-low PV energy scenario [42].

The low currents and high gain factor are the main challenges. The output current of the system is around several microamperes, which prevents the system to perform any current division or engage large bias currents. Therefore, we propose a power efficient current sensor as shown in Figure 55(a) where V_{cp} is the output voltage shown in Figure 35. To minimize the power consumption, sensing state S_{sen} and standby state $\overline{S_{sen}}$ are implemented by SW_{C1} and SW_{C2}. During the sensing phase with SW_{C2} turned on, all the current from the voltage tripler goes into the right branch while the reference branch is controlled by the supercapacitor voltage V_{out}. In order to make sure equal voltage potential between V_{out} and V_{cp} to be held, the self-biased current amplifier uses positive feedback through M_{CP1}, M_{CP2}, M_{CN1}, and M_{CN2} to boost its loop gain. The closed-loop transfer function from the output current of charge pump to the sensed voltage can be derived as

$$\frac{V_{sen}}{I_{cp}} = \frac{R_{SEN}}{1 + \frac{1}{g_{MCP3}} \cdot T_{FB}} \tag{48}$$

where T_{FB} represents the open-loop transconductance through the blue dashed path as

$$T_{FB} = \frac{i_2}{V_{cp} - V_Y} = \frac{1}{\frac{1}{g_{MCN2} \times (-g_{MCP1}) \times Z_{CN1}} + Z_{CP2} - \frac{1}{g_{MCN2}}} \tag{49}$$

With a symmetrical design, we have $Z_{N1} \approx 1/g_{MCN1}$ and $Z_{P2} \approx 1/g_{MCP2}$ at low frequencies. The above transfer function can be simplified as

$$\frac{V_{sen}}{I_{cp}} = \frac{R_{sen}}{1 - \frac{g_{MCN2}}{g_{MCP3}}} \tag{50}$$

From the denominator, both positive and negative feedback through g_{MCN2} and g_{MCP3} affect the overall current sensing gain. In this design, the width and transconductance of M_{CP3} is made much larger than M_{CN2}. Therefore, the negative feedback dominates to ensure the stability and eliminate potential startup difficulty. The transfer characteristic is shown in Figure 55(b). Once the small self-biased current is exceeded, the two node voltages V_{cp} and V_{out} are forced to be equal, and the current information I_{cp} is amplified and converted monotonically into V_{sen}.

4.1.1.4 MPPT Processing Circuit

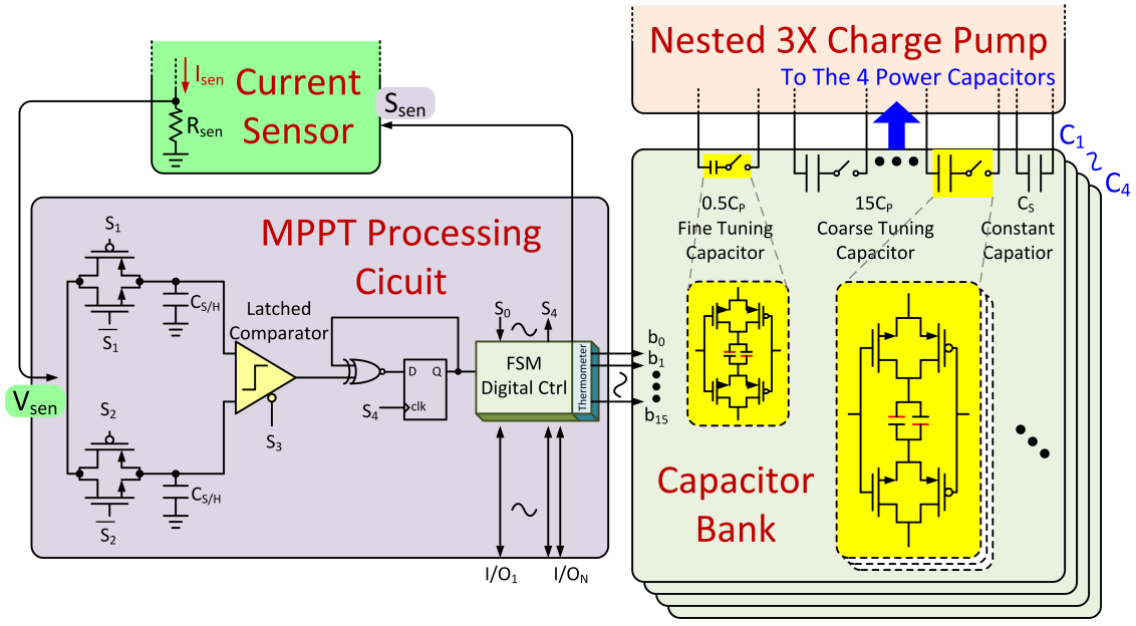


Figure 56. MPPT processing circuit and capacitor bank.

As illustrated in Figure 50, when the current sensor starts evaluating the output power, the S/H MPPT module is simultaneously triggered to record and compare the power information. As shown in Figure 56, the detailed MPPT processing circuit consists of two identical S/H channels, a comparator, a FSM, and a binary-to-thermometer decoder.

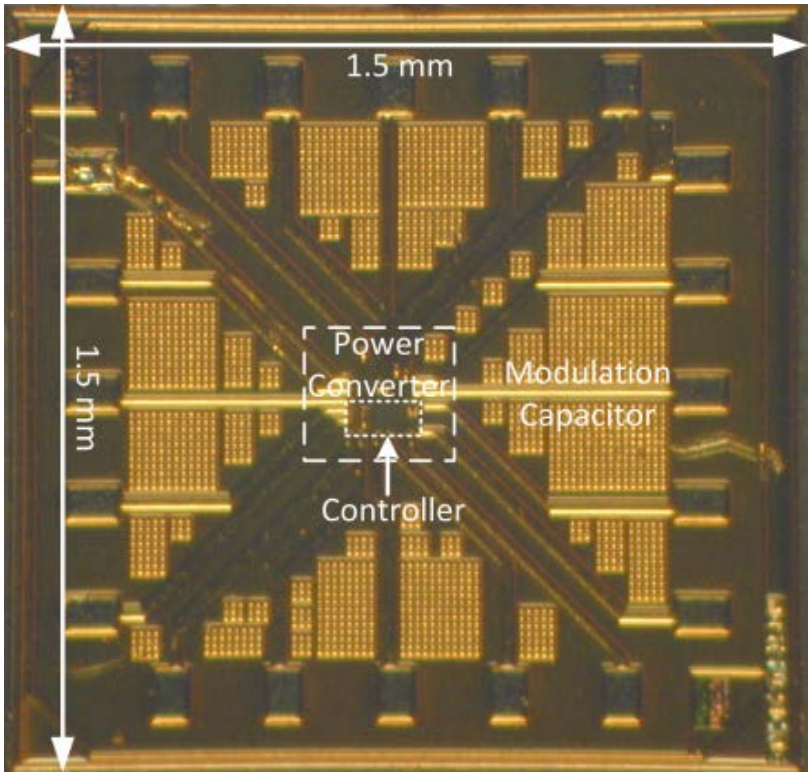
The two identical channels, in Figure 56, are controlled by complementary phase clocks S_1 and S_2. Defined by the digital controller, phase S_1 is set to capture the power information of the old state, and phase S_2 for that of the new state. Finally, the two states relating to different charge pump capacitor values are stored and aligned for latch comparison. During the current sensing period S_{SEN}, the voltage tripler is disconnected from the supercapacitor load to the current sensor, which induces noticeable voltage ripples. However, as shown in Figure 56, the combination of the sampling capacitor $C_{S/H}$ and the large resistor R_{SEN} act as a low-pass RC filter, thus extracting the DC value correctly. Due to the ultra-low power budget and one-time comparison requirement, we choose the latched comparator. A positive feedback of the latched comparator is used to boost the regeneration gain. The transistor size is minimized for low energy consumption. The proposed capacitor value modulation scheme replaces analog modules with digital modules such as the comparator, the FSM, and the decoder. The digital modules operate in low speed under low power supply, resulting negligible power consumption.

4.1.1.5 Digital Programmable Capacitor Bank of CVM

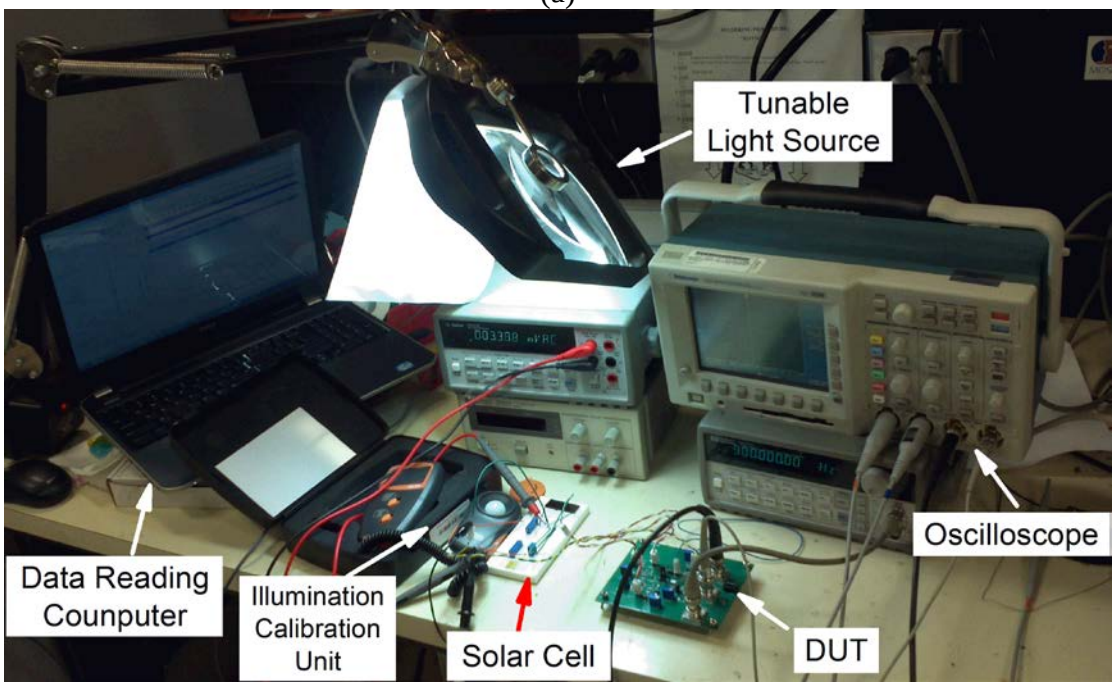
The digital programmable capacitor bank shown in Figure 50 is implemented in this section. With the manipulation from the MPPT module, the capacitor value of the bank, also as the input impedance of the charge pump, is modulated to track the MPP of a solar cell. As shown in Figure 56, the capacitor bank consists of a static part C_S and a programmed part C_P. The C_S delivers the minimum usable power. The C_P is split into coarse and fine impedance tunings. The coarse tuning uses 15 identical capacitors programmed by a 4-bit FSM controller. Instead of binary code, thermometer code is used for smoother transition during most significant bit (MSB) changing. The fine tuning resolution has ½ the value of the standard capacitor C_P and controlled by 1-bit additional binary code. During the MPPT procedure, the 4-bit coarse capacitor bank keeps being programmed. Once the maximum power transfer range is locked, the fine tuning is executed in the sub-loop to improve the tracking accuracy.

4.1.2 Measurement Results

The adaptive PV harvester system is designed and fabricated in standard 0.18-μm CMOS technology. The die photo of the fabricated chip is shown in Figure 57(a). The entire energy harvesting system occupies a silicon area of 1.5 mm × 1.5 mm. Dual layer Metal-Insulator-Metal on-chip capacitors are used for the monolithic integration of the capacitor bank. The testing setup is demonstrated in Figure 57(b). The indoor illumination environment was calibrated by a light meter.

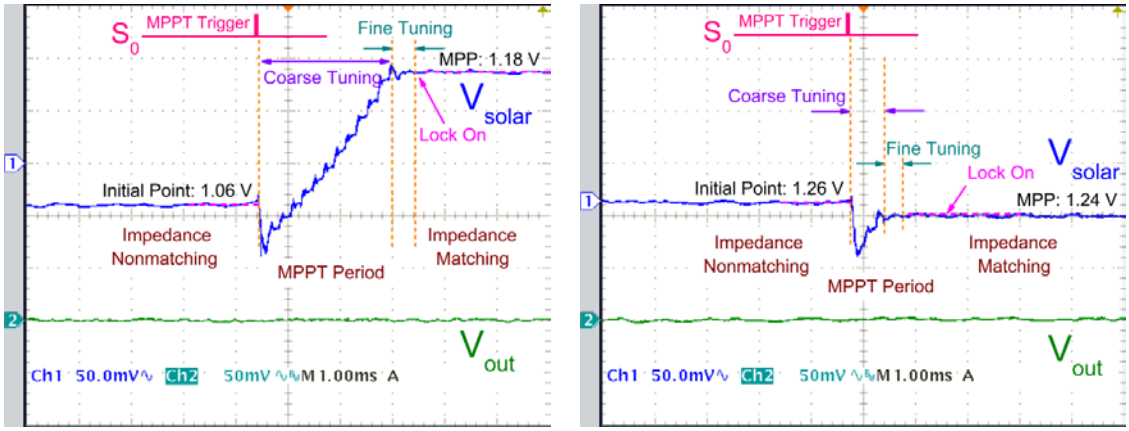


(a)



(b)

Figure 57. (a) Die photograph of the fabricated chip, (b) testing setup.

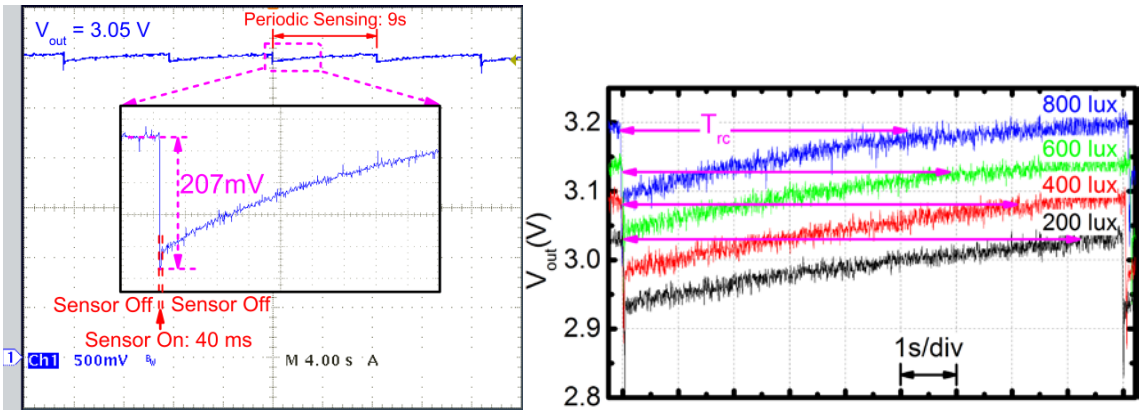


(a) (b)

Figure 58. Experimental transient results of the MPPT procedure under (a) 400 lux, (b) 800 lux light intensity.

The transient measurements were carried out to verify the correct behavior of the MPPT module. To emulate mild indoor illumination, a light intensity of 400 lux was given. The light acceptor was a small commercially available solar cell featuring 10×25 mm^2 in size. The load was characterized by a potentiometer from 200 kΩ to 10 MΩ paralleled with a 33 mF supercapacitor. The transient V_{solar}, V_{out} and S_0 are shown in Figure 58(a). In the beginning, the programmable capacitor bank of the harvesting system was externally preset to an unmatched condition with V_{solar} around 1.06 V. Once S_0 triggered the digital controller, the system began to execute the hill-climbing MPPT procedure step by step from the initial point. After 12 tentative steps, the coarse tuning interval was captured and the fine tuning process quickly narrowed down and locked onto the optimal V_{solar} of 1.18 V. Afterwards, the MPPT module was shut down and the controller worked in its minimum power consumption mode. The V_{out} is maintained at 3.1 V with reduced ripples smaller than 10 mV due to the supercapacitor value. As a comparison, a stronger light condition with 800 lux, which emulates plenty of indoor

fluorescence or overcast outdoor daylight, is measured with results presented in Figure 58(b). The programmable capacitor bank is preset to the same initial state, which results in a higher unmatched voltage as 1.26 V due to the stronger light condition. Actually, because Z_{cp} is designed to match Z_{solar} as (3), the required dynamic range of V_{solar} for high PCE in Figure 35 does not need as large as 1-1.5 V. For specific application conditions such as V_{out} = 3.25 V in Fig. 5, the necessary dynamic range of V_{solar} for PCE > 80% is 1.1-1.3 V, and is satisfied by the tuning of the programmable capacitor bank. The MPPT procedure only needs 2 coarse steps to converge at the MPP of 1.24 V. Note that even though the V_{solar} varies from 1.18 V to 1.24 V, the corresponding available power changes from 16 µW to 29 µW.



(a) (b)

Figure 59. Experimental transient performance (a) with a wireless temperature sensor operating, (b) comparing one sensing period with different light intensities.

The practical driving performance of the harvesting system for a temperature sensor and wireless transceiver CC2500, is shown in Figure 59(a). For saving energy, the loads are operated in a sample-per-seconds scheme. The sensor and transceiver are

turned on only 40 ms periodically. The CC2500 reads the monitored temperature data and transmits with a 2.4 GHz RF signal. A computer with a RF receiver reads the environmental temperature data around 27 ^{o}C with 0.1 ^{o}C sensitivity. The rest 9 seconds are scheduled as an idle mode. From the transient plot, the harvesting system provides a stable 3.05 V supply and 207 mV ripple voltage. For a comparison, the harvesting performance under different light intensities is demonstrated in Figure 59 (b), which shows higher light intensity yields higher V_{out} and faster recovering time T_{rc}.

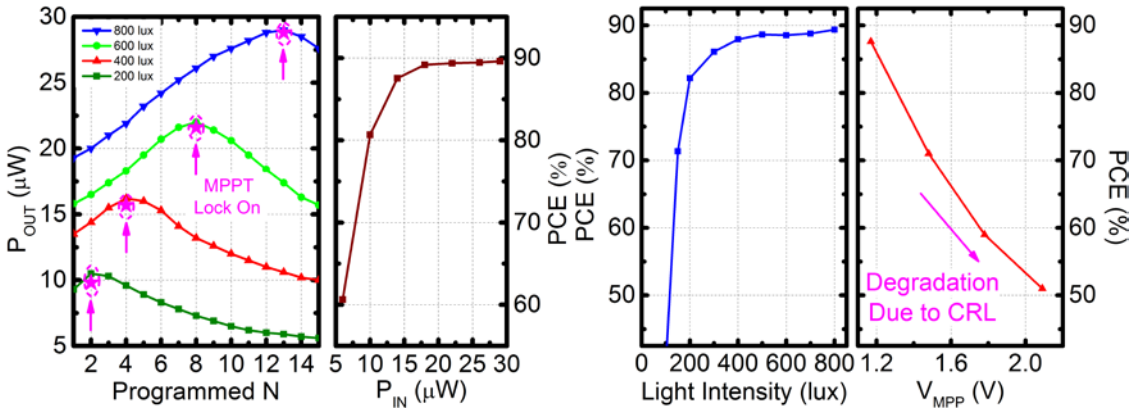


Figure 60. (a) Static output power with different programmed numbers of the capacitor bank under different light intensity, and end-to-end peak power conversion efficiency (PCE) with MPPT vs. different PV power or light intensities, (b) PCE vs. light intensity and PCE with different V_{MPP} and charge redistribution losses.

The accuracy of MPP tracking is observed through a static measurement. The MPPT module is disabled and the capacitor bank is programmed by an external computer through the I/O communication ports. With 3-3.5 V output voltages, the harvested power versus the programmed number N is depicted in Figure 60(a) under different light intensities from 200 lux up to 800 lux. The dynamically captured MPP

values are also annotated on the plot for comparison. For all 4 cases the harvesting system was able to converge at the global optimal point. The peak PCE without MPPT being activated achieves 92% at 800 lux with the minimized switching loss, the charge redistribution loss, and the conduction loss. The end-to-end peak PCE with active MPPT versus different PV sources is also demonstrated in Figure 60(a), in which the harvester maintains efficiencies greater than 80% with output power above 10 μW and output voltage within 3-3.5 V.

The PCE with different light intensities is plotted in Figure 60(b). The proposed energy harvesting with CR = 3 is designed specifically for the PV cell with nominal V_{MPP} = 1.2 V. For other type of PV cells with nominal V_{MPP} values as 1.5 V, 1.8 V, and 2.1 V, the PCE is measured in Figure 60(b). As analyzed in (3), the resulting V_{solar}×CR significantly deviates from 3-3.5 V. Therefore, the charge redistribution loss ruins the PCE with increasing nominal V_{MPP} or V_{solar}.

The PCE with different light intensities is plotted in Figure 60(b). The proposed energy harvesting with CR = 3 is designed specifically for the PV cell with nominal V_{MPP} = 1.2 V. For other type of PV cells with nominal V_{MPP} values as 1.5 V, 1.8 V, and 2.1 V, the PCE is measured in Figure 60(b). As analyzed in (3), the resulting V_{solar}×CR significantly deviates from 3-3.5 V. Therefore, the charge redistribution loss ruins the PCE with increasing nominal V_{MPP} or V_{solar}.

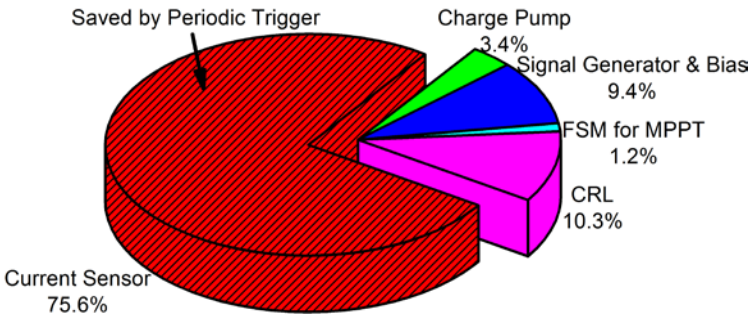


Figure 61. Detailed power consumption of the PV energy harvesting system.

The detailed power consumption of the proposed system during MPPT procedure is simulated as in Figure 61. The current sensor of for MPPT dominates the power consumption; however, it is not necessary to operate all the time. If the FSM initiates the MPPT module after a long time such as every several seconds, the energy loss during the small time of MPPT procedure is negligible. When the FSM triggers the MPPT module every 1 second, the output current begins to decrease and the system PCE is degraded to 89%, which can be regarded as the peak dynamic PCE. Further increasing the MPP tracking speed is detrimental to the harvesting system in terms of overall PCE.

Table 9 compares the performance of the proposed work with other state-of-the-art MPPT harvesters. This harvester uses on-chip switched capacitors and features monolithic integration. The peripheral circuits, including the FSM, the VCO, and the MPPT module, are all powered by the harvester and auxiliary charge pump. Thus, the entire harvesting system is self-sustaining and needs no external bias. The input voltage range is 1-1.5 V, aiming for a single solar cell. For specific V_{out} value between 3-3.5 V, the MPPT dynamic range is 200 mV such as V_{solar} = 1.1-1.3 V. The harvested power ranges from 0 µW to 29 µW depending on the illumination condition. Without MPPT operation under 800 lux intensity, the static end-to-end PCE is 92%. For ordinary

operation where the incoming dim indoor light is 400 lux and the MPPT module is operated in the active mode, the dynamic overall PCE can achieve a peak value of 89% with 16 µW of throughput power. The proposed harvester achieved a superior performance compared to reported results, which can only achieve good efficiencies with a large amount of PV power around hundreds of microwatts, or harvest a small amount of power below 20 µW but with poor PCE [42], [43], [46], [53], [94]. In summary, this PV energy harvesting system achieves both ultra-low operation capability under 20 µW and excellent self-sustaining PCE of 89% at the same time.

Table 9. Performance comparison of low energy harvesting systems with MPPT.

	[42]	[43]	[94]	[53]	[46]	This Work
Technology (µm)	0.35	0.35	0.25	0.13	0.35	0.18
Fully-integrated	Yes	Yes	No	Yes	No	Yes
Self-sustaining	No	No	Yes	Yes	Yes	Yes
Input Range (V)	2.1-3.5	1-2.7	0.5-2	1.8	1.5-5	1-1.5*
Output Range (V)	3.6-4.4	2	0-5	1.4	0-4	3-3.5
Power Throughput (µW)	100-775	0-80	5-1000	<10	800	0-29
Peak Dynamic PCE with MPPT	67% @529 µW	86% @35 µW	70% @16 µW	58% @10 µW	84.3% @800 µW	88.7% @16 µW

*For specific V_{out}, MPPT dynamic range is 200mV.

4.1.3 Conclusion

This work proposes a monolithic highly-efficient ultra-low PV power harvesting system for the smart nodes of IoT networks in 0.18-µm CMOS technology. Instead of commonly used passive RFID supply, the harvesting system offered higher output power with a compact PV cell as small as 2.5 cm^2. A switched capacitor DC-DC converter is chosen to eliminate the need for an off-chip inductor, making it a monolithic solution suitable for the fully-integrated IoT smart nodes. The MPPT function was developed through the hill-climbing algorithm in an energy-efficient approach, ensuring maximum power transfer under various illumination conditions. The capacitor value modulation approach was developed to tune the input impedances of the harvesting system. Compared with the conventional PFM scheme, this modulation scheme had no quiescent power consumption, thus resulting in a higher harvesting efficiency. Experimental results demonstrated the harvesting system achieves both ultra-low operation capability under 20 µW and excellent self-sustaining PCE at the same time. It was able to generate 0-29 µW output power and 3.0-3.5 V output voltages. Given dim indoor light of 400 lux and the MPPT module acting every 1 second, the harvesting system could deliver 16 µW with an end-to-end PCE of 89%. Thus, a temperature sensor, and wireless transceiver were fed by this power in an energy-efficient sample-per-seconds mode.

4.2 EH System with Hysteresis Regulation and Time-domain MPPT

The proposed energy harvesting system depicted in Figure 36 can be implemented as shown in Figure 62. Its building blocks will be discussed next.

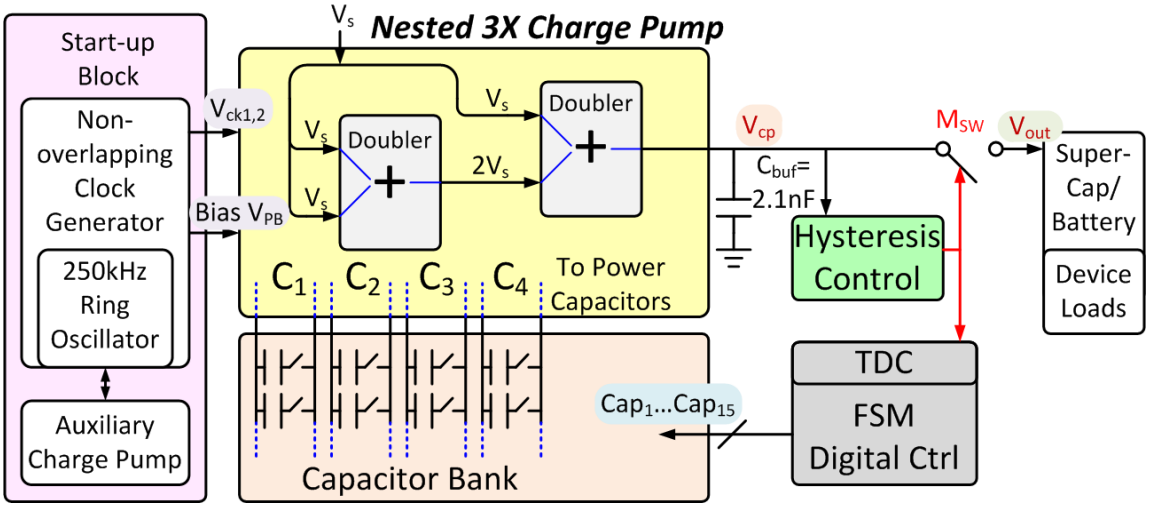


Figure 62. Detailed proposed architecture of the energy harvesting system.

4.2.1 Circuit Implementation & Design Procedure

4.2.1.1 Compact Nested Voltage Doubler

In Figure 37, the switch transistors M_1 and M_2 are cross-connected and self-switched. However, such architecture limits the turn-on voltage of NMOS transistors to less than V_s, which ranges from 1.1-1.5 V. The low turn-on voltage drastically increases the conduction resistance and degrades boosting efficiency. Furthermore, the self-switching transistors suffer from shoot-through current, which ruins the conversion efficiency. Other coupled parasitic capacitors also affect the self-switching and require additional damping branches [95]. To eliminate these problems, we propose to break the cross-connected gates of $M_{1,2,3,4}$ and $M_{P1,2}$, and drive them separately with the higher supply voltage non-overlapping clock $CLK_{1,2}$ as shown in Figure 63(a). The four drivers used in Figure 37(a) are implemented with transistor M_{D1} and M_{D2}. For the second stage, $M_{3,4}$ are replaced with PMOS switches to allow conducting voltage as high as $2V_s$. The operating waveforms of the 3× charge pump are depicted in Figure 63(b). When CLK_1 =

1 (logic) and CLK_2 = 0 (logic), C_1 and C_3 are charged to V_s and $2V_s$, respectively. C_4 is discharged to the output C_{buf} as $3V_s$. When CLK_1 = 0 and CLK_2 = 1, C_2 and C_4 are charged to V_s and $2V_s$, respectively. C_3 is discharged to C_{buf} as $3V_s$. When CLK_1 = 0 and CLK_2 = 0, all of the switches are turned off to prevent the shoot-through current. $CLK_{1,2}$ are generated by following auxiliary circuits.

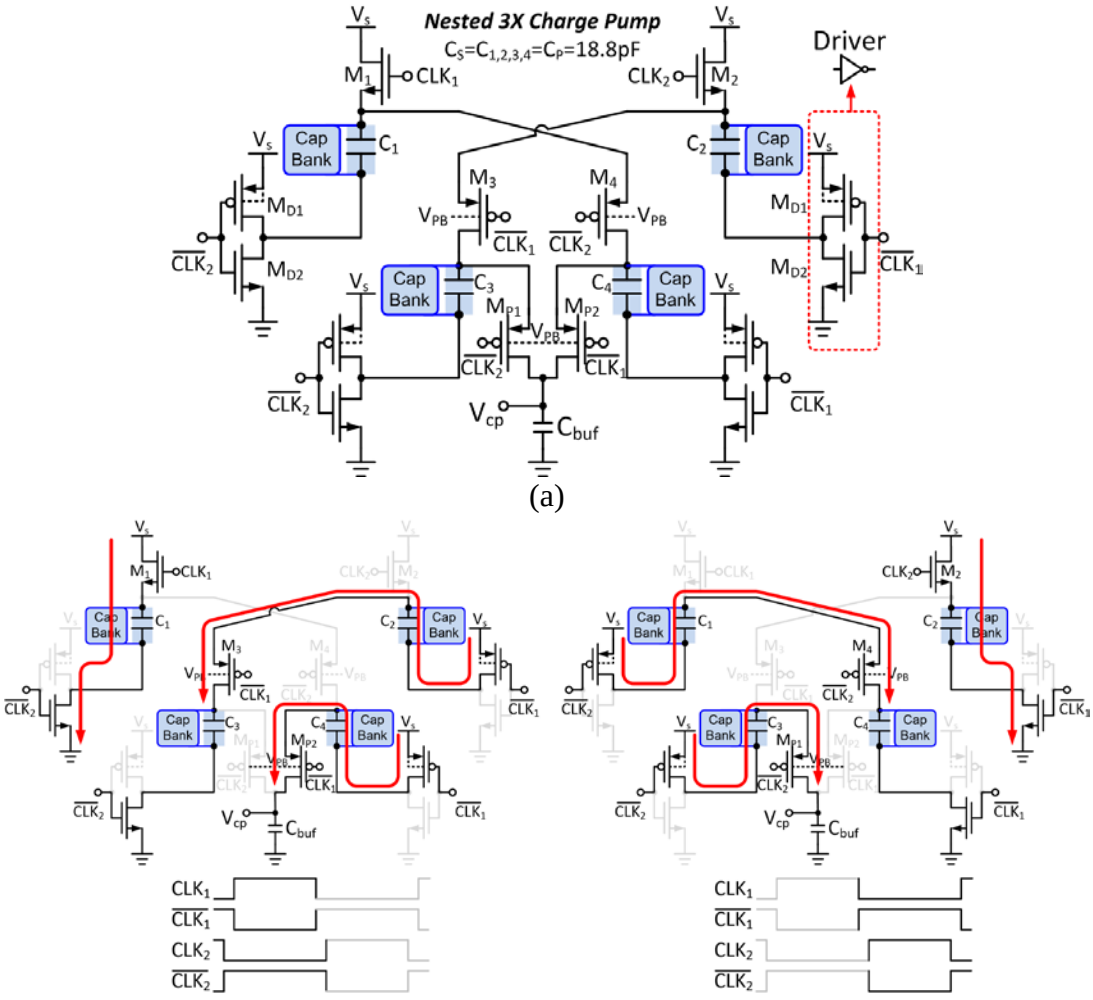


Figure 63. (a) Modified architecture of the nested 3× charge pump power converter and (b) its operation with the non-overlapping clocks in complementary phases.

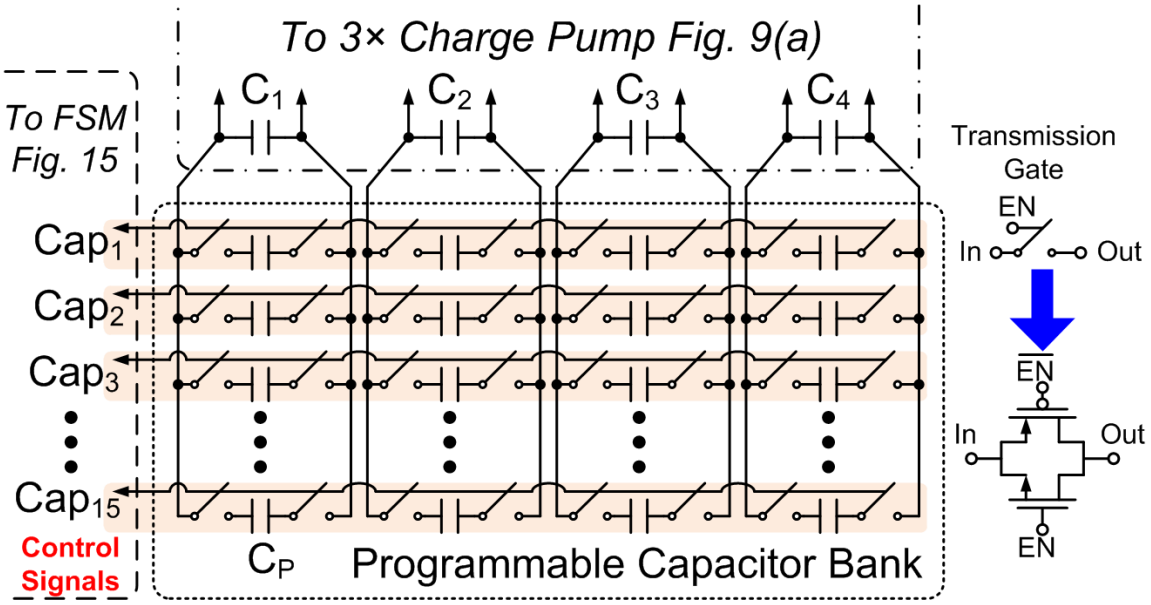


Figure 64. Schematic of the programmable capacitor bank.

As introduced in Section 3.2.2, the switched capacitors are programmable and split into fixed part C_S and N programmable capacitors CP [48]-[50]. In this design, $C_{1,2,3,4}$ represent C_S and its value is 18.8 pF. The programmable capacitor bank is implemented as Figure 64 with N = 15 and C_P = 18.8 pF. The switches are implemented by transmission gates. The 15 identical rows are controlled by thermometer code $Cap_{1\sim15}$ from a 4-bit FSM controller, which is introduced in Section 4.2.1.4.

4.2.1.2 Startup & Auxiliary Bias Circuit

To eliminate external biases and realize the self-sustaining feature for an energy harvesting system, a startup and auxiliary bias circuit is proposed to provide supply voltages and driving signals once the PV cell is connected to the harvester. In Figure 65, a current-starved 250 kHz ring oscillator operates with applied PV voltage V_s. Its output clock, V_{ax1}, drives a non-overlapping signal generator in the right side, which eliminates the shoot-through current and improves converter efficiency. Different from the

conventional non-overlapping clock generator [96], a delay line is placed in the feedback path. Therefore, the forward drivers are designed to maximize their fan-out capability and minimize their power consumption. The non-overlapping time is tuned by the delay line independently.

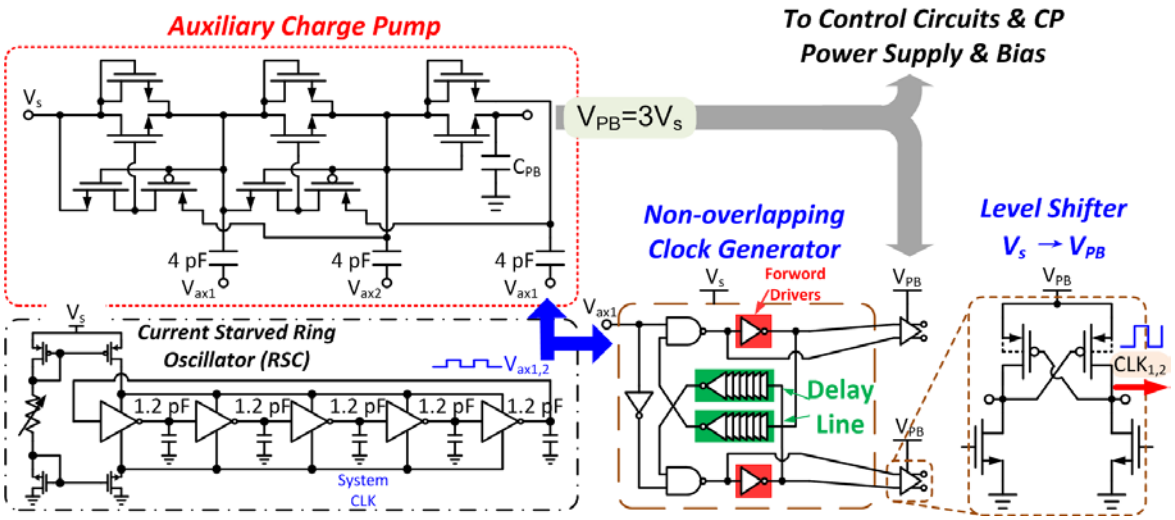
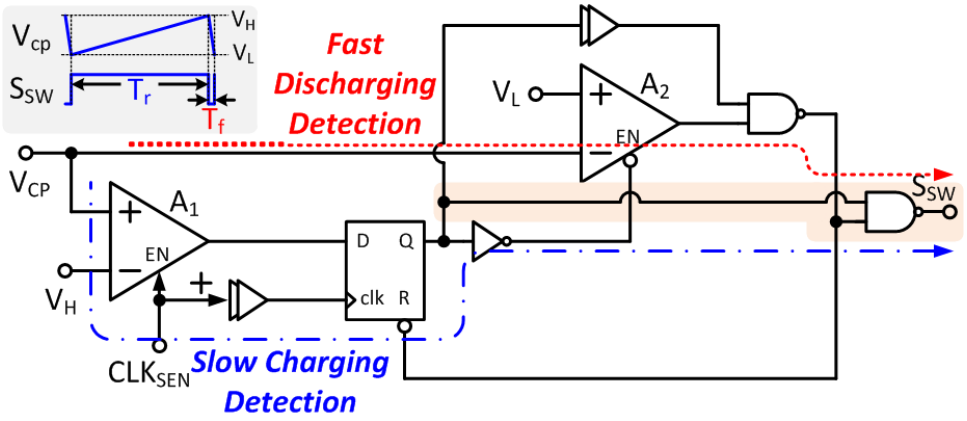


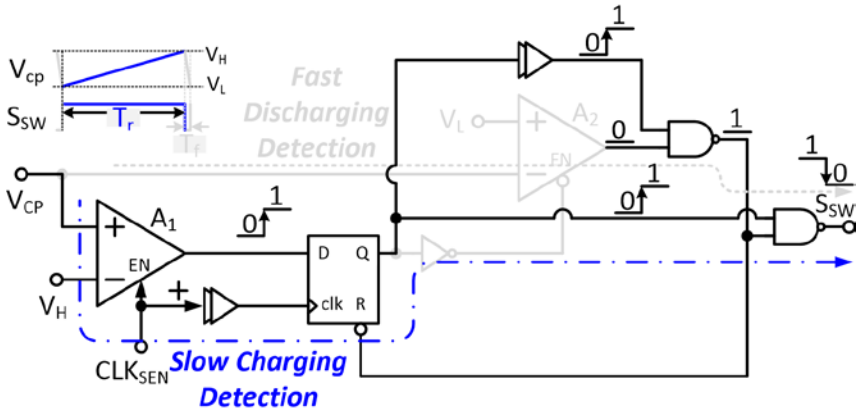
Figure 65. Startup circuits and auxiliary bias circuits for self-sustaining.

However, these circuits are directly supplied by V_s, which is not capable of driving the 3× charge pump. Thus, an auxiliary three-stage Dickson charge pump is used to generate a higher supply voltage as $V_{PB} = 3V_s$. It is driven by the $V_{ax1,2}$ from the ring oscillator. V_{PB} supplies a level shifter and generates $CLK_{1,2}$ with $3V_s$ amplitude. The shifted $CLK_{1,2}$ helps $M_{1,2}$ in Figure 63(a) to have a gate drive voltage of $2\times V_s$ during the turn-on period. Additionally, the auxiliary charge pump provides V_{PB} to all control circuits as a power supply and body bias.

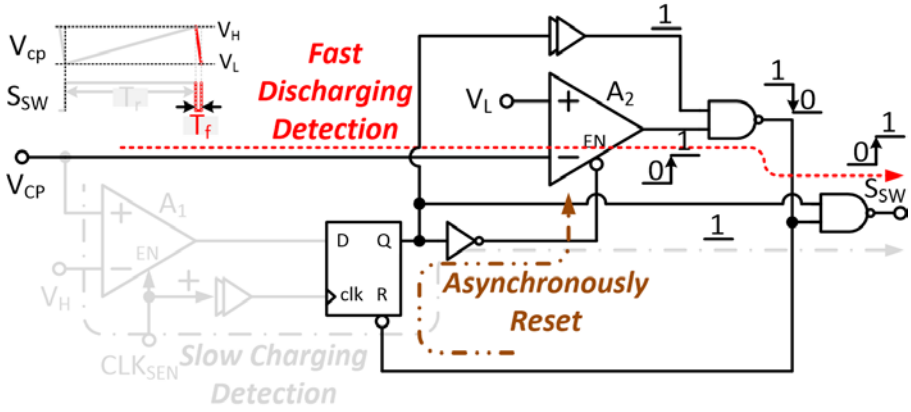
4.2.1.3 Hysteresis Controller



(a)



(b)



(c)

Figure 66. (a) Architecture of the self-triggered one-shot hysteresis controller, (b) when S_{SW} = 1 and the controller detects T_r, (c) when S_{SW} = 0 and the controller detects T_f.

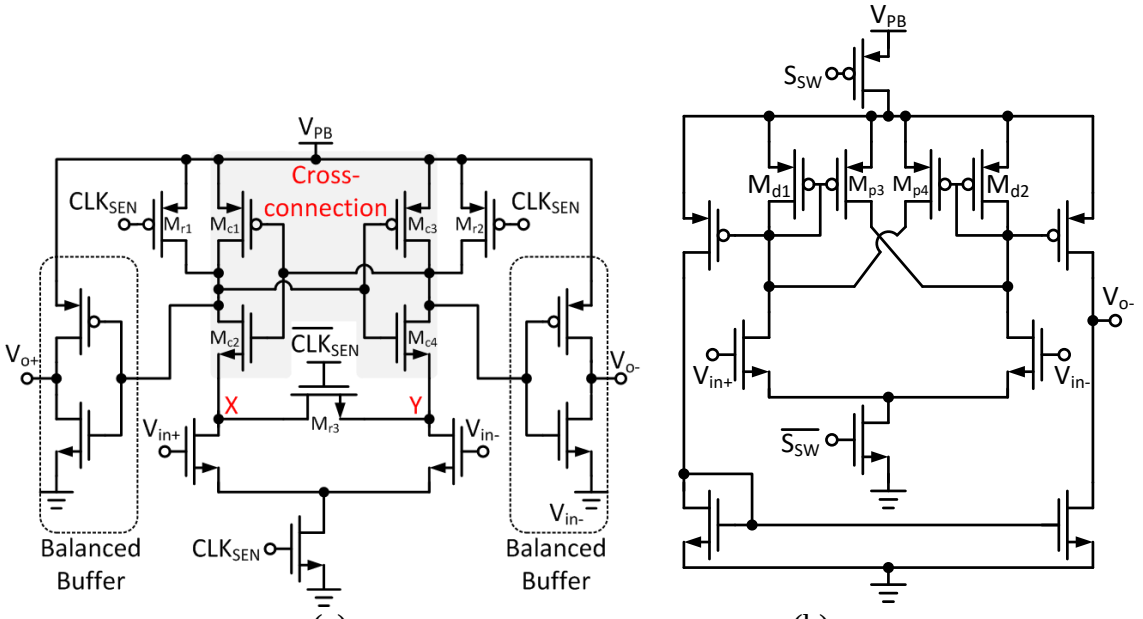


Figure 67. Structures of (a) the low power latched comparator A_1 and (b) the high speed amplifier A_2.

The one-shot hysteresis controller proposed in Figure 39 is implemented as shown in Figure 66(a). The utilized comparators A_1 (low power) and A_2 (high speed) are shown in Figure 67. For the LVTTL standard, V_L and V_H are set as 3.15 V and 3.3 V, respectively. In Figure 66(b), when $S_{SW} = 1$ and M_{SW} is off, the charge pump keeps charging C_{buf} and V_{cp} continues rising. A low power latched comparator, A_1, is clocked by a sensing clock CLK_{SEN} with a frequency that is twice that of the charge pump switching signal $CLK_{1,2}$. When V_{cp} is charged up to V_H, the period of T_r ends, $S_{SW} = 0$, and M_{SW} is turned on. As shown in Figure 66(c), C_{buf} is quickly discharged to the output. A high speed comparator, A_2, regulates the discharging time T_f as one-shot. Once $V_{cp} < V_L$, the T_f detecting circuit turns off M_{SW} and is asynchronously reset for next charging period.

4.2.1.4 Implementation of FSM and TDC Converter

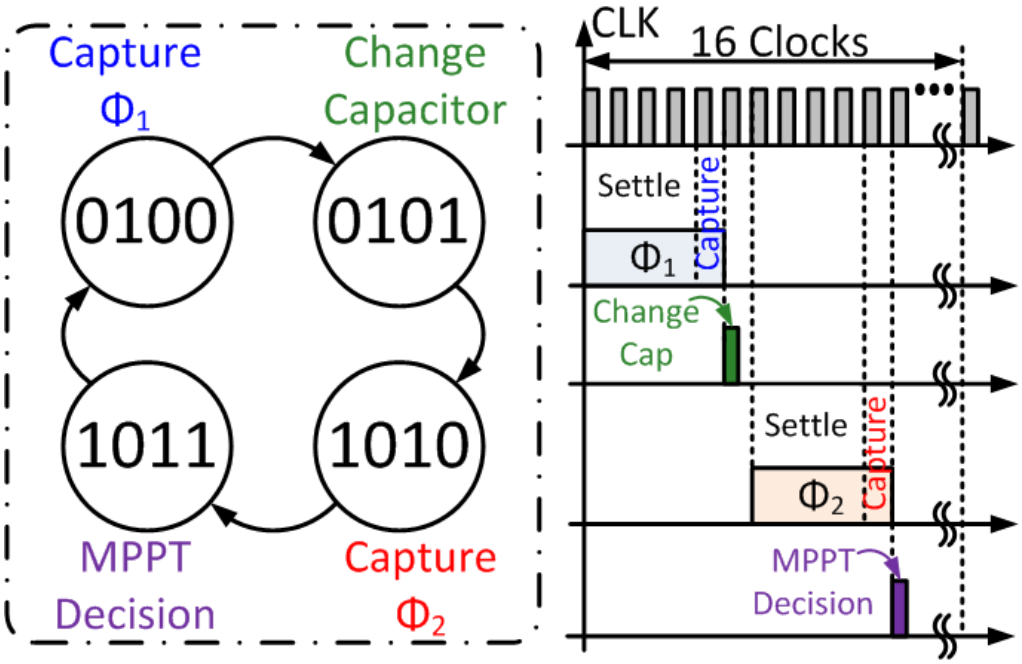


Figure 68. State transfer chart of the finite-state machine and its time diagram.

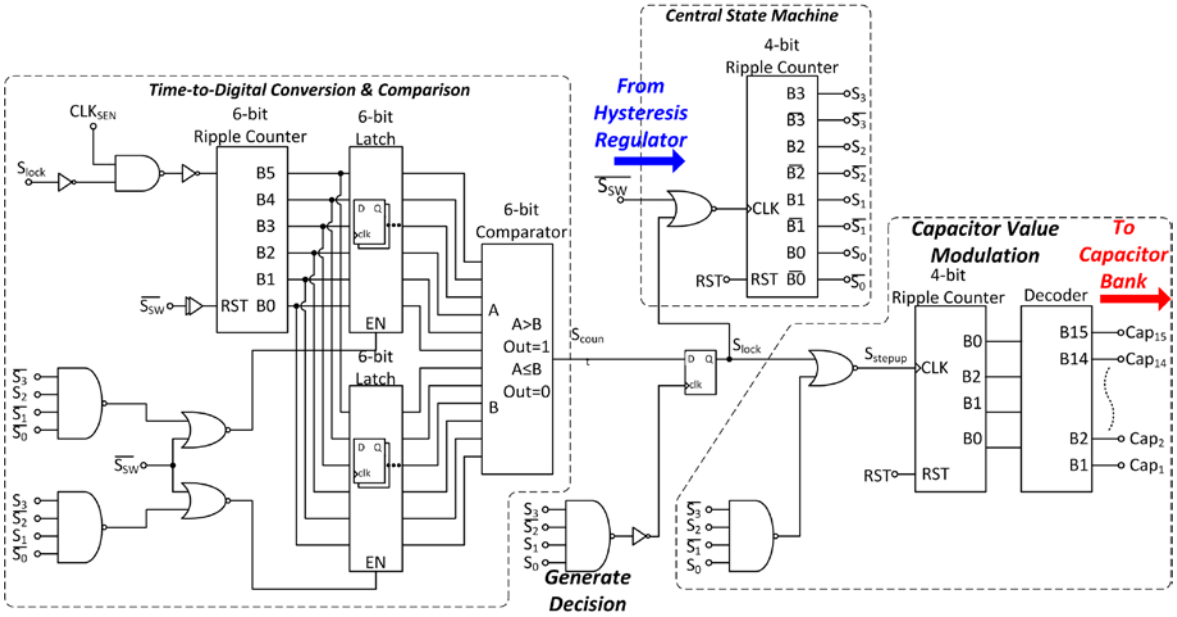


Figure 69. Simplified structure of the finite-state machine (FSM) with the TDC function.

As illustrated in Figure 36, the MPPT function is realized in a FSM. Its detailed state transfer chart and time diagram are shown in Figure 68. The structure of the FSM is demonstrated in Figure 69. It is clocked by S_{SW} from the hysteresis controller. On the top level, every tentative searching step is executed in 16 system clocks of a 4-bit FSM. Initially, four clock periods of the Φ_1 state are used to settle the harvesting transient of V_{cp} due to the capacitor value modulation. At the end of Φ_1 state, the binary code 0100 for the clock captures the quantized number of rising time T_{r1}. Then the binary code 0101 for clock tentatively disconnects one row of the capacitor bank in Figure 64 and increases R_{cp}. The Φ_2 state uses another four clock periods to settle with the new R_{cp}, and uses the binary code 1010 for the clock to capture the new T_{r2}. Subsequently, T_{r1} and T_{r2} are compared for MPPT decision in the binary code 1011 for the clock. If $T_{r1} > T_{r2}$, the controller should keep searching the MPP; if $T_{r1} \leq T_{r2}$, MPP is already achieved, and the controller locks in this state. The remaining four clocks are spared for I/O communication with smart nodes. The TDC counters are built with asynchronous-reset ripple counters for minimum device cost and dynamic power.

4.2.2 Measurement Results

The adaptive PV harvester system is designed and fabricated in standard 0.18-μm CMOS technology. The die photo of the fabricated chip is shown in Figure 70. The entire energy harvesting system occupies a silicon area of 1.5 mm × 1.5 mm. Dual layer metal-insulator-metal (MIM) on-chip capacitors are used for the monolithic integration of the capacitor bank. The measurement setup is illustrated in Figure 71. This smart node includes a temperature sensor, a microcontroller and a wireless transceiver CC2500. In

general, the proposed energy harvesting system can operate with a supercapacitor and/or a compact 3.3 V manganese silicon lithium battery, which are only used as storage components. When there is not enough PV energy, the harvesting system stops operating, and the battery or supercapacitor solely powers the smart node.

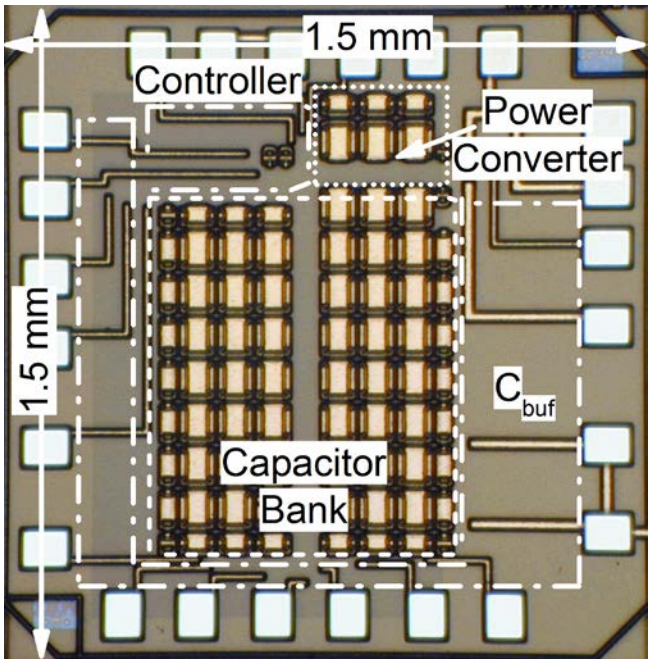


Figure 70. Die photograph of the fabricated chip.

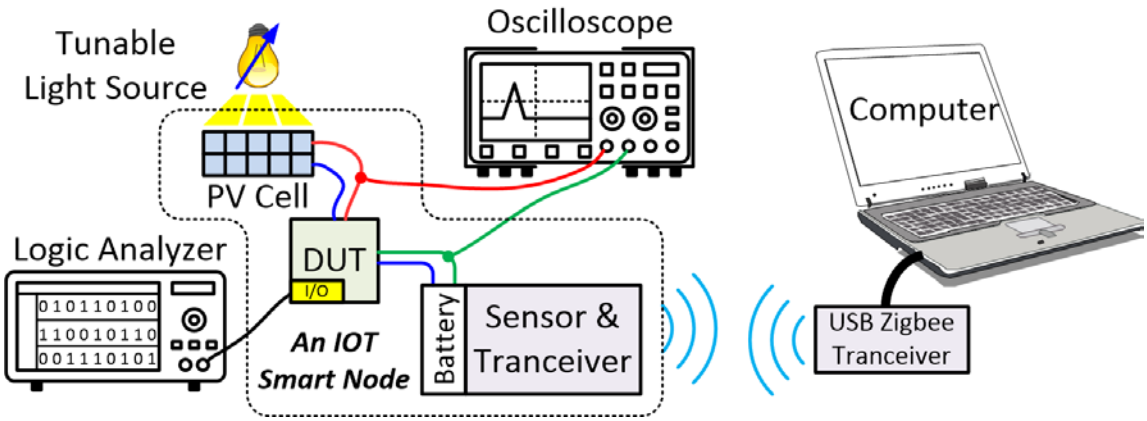
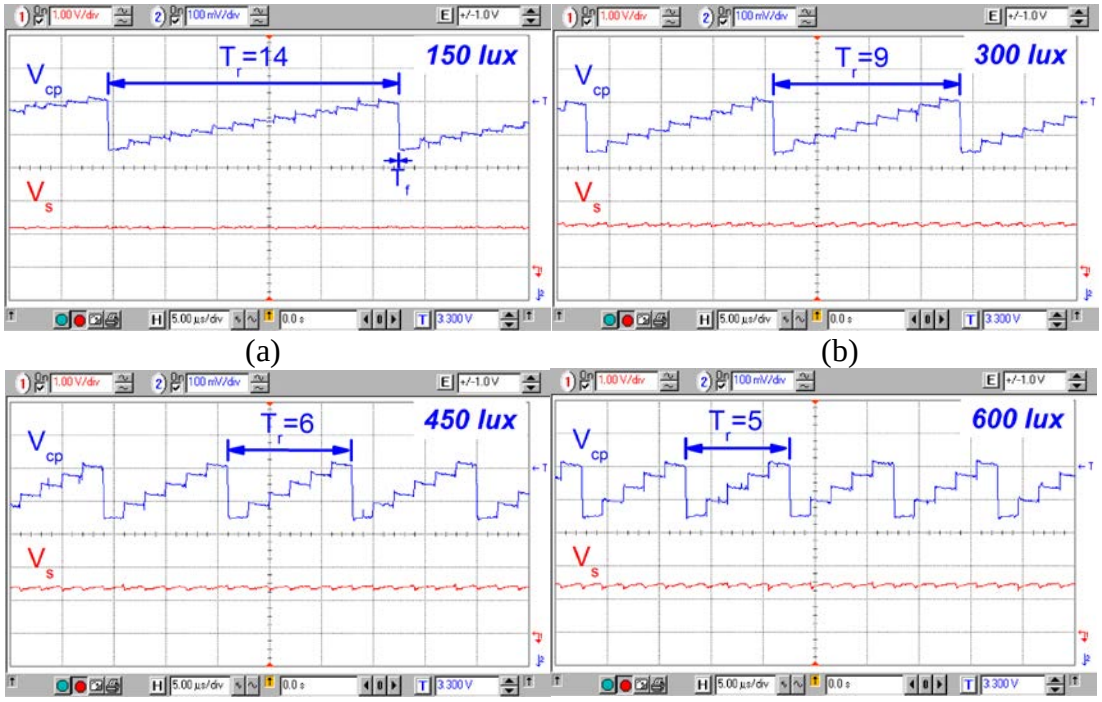


Figure 71. Testing setup for trickle charging an IoT smart node.



(a) (b)

(c) (d)

Figure 72. Different charging time T_r under (a) 150, (b) 300, (c) 450 and (d) 600 lux conditions.

The transient measurements were carried out to verify the behavior of the output regulation and the relationship between input light power and the time-domain variable T_r. To emulate indoor illumination, various light intensities from 150 to 600 lux were applied. The light acceptor was a small commercially available PV cell featuring a compact 2.5 cm^2 size. The load was characterized by a potentiometer from 200 kΩ to 10 MΩ paralleled with a 33 mF supercapacitor. The transient PV cell voltage Vs and buffering output voltage V_{cp} are shown in Figure 72. The relationship between light intensities and T_r is characterized as follows: With a weak light intensity of 150 lux, the system needs more time as there are 14 quantized steps for a full capacitor charge. With

a strong light intensity of 600 lux, the system only needs 5 quantized steps for a full capacitor charge.

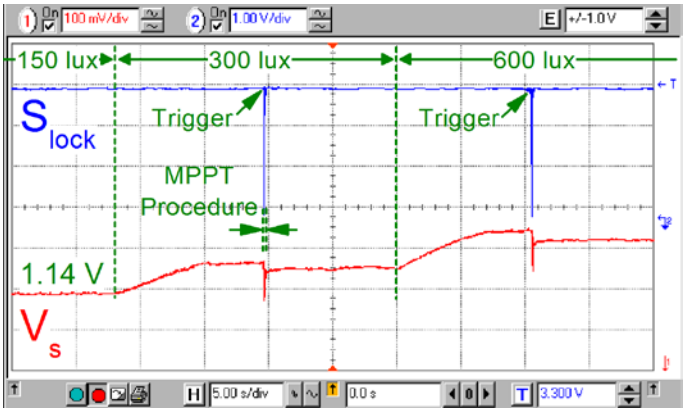


Figure 73. Transient MPPT with illumination changing from 150 lux to 600 lux.

When the light illumination is changing, the MPPT of V_s is shown in Figure 73. MPPT operation is indicated by S_{lock}: When S_{lock} is low, MPPT is turned on. Initially, the PV cell is given 150 lux and Vs is 1.14 V. Then the illumination is increased to 300 lux, and the MPPT is manually triggered with an initial value of V_{sL} = 1.13 V and quickly reaches the MPP. The achieved MPP for 300 lux is 1.21 V.

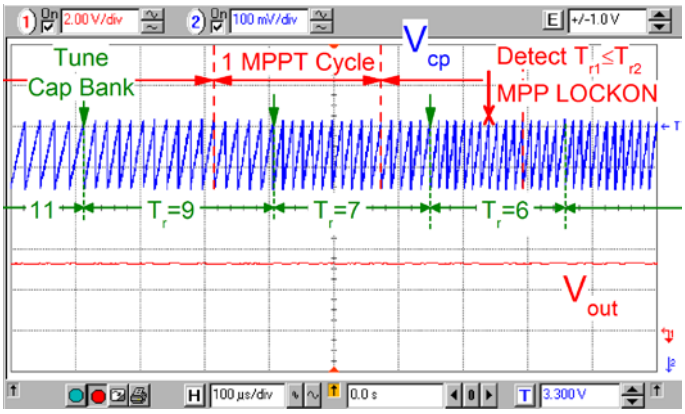


Figure 74. Transient V_{cp} and V_{out} waveforms during the MPPT procedure with 450 lux illumination.

The detailed dynamic MPPT performance was tested as shown in Figure 74 with 450 lux illumination. The external signal S_0 triggers the MPPT module and initializes the capacitor bank. The system begins to execute the hill-climbing MPPT procedure as shown in Figure 41. After seven tentative capacitor changes, the system detects that the charging time T_r cannot be shorter than six steps, which means the MPP is already captured. Thus, the capacitor bank is locked, the MPPT module is turned off, and the controller works in its minimum power consumption mode. The V_{out} is maintained around 3.3 V with reduced ripples smaller than 50 mV due to the 33 mF supercapacitor.

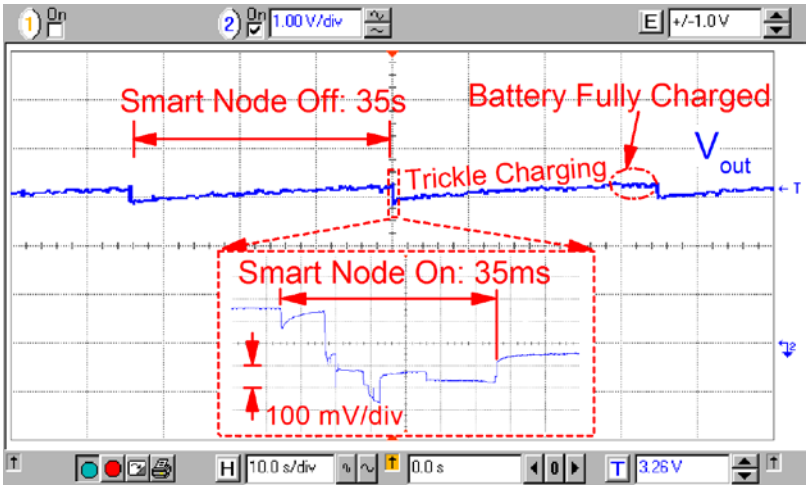


Figure 75. Driving performance for an IoT smart node operation.

The practical driving ability of the harvesting system is validated for an IoT smart node. For saving energy, the IoT smart node is operated in a periodic sample-per-seconds scheme. As shown in Figure 75, the sensor and transceiver are turned on for only 35 ms, which is set as a 0.1 % duty ratio of the whole period. The microcontroller reads the sensed environmental temperature around 27 ^{o}C with 0.1 ^{o}C sensitivity and

transmits it through CC2500 with a 2.4 GHz RF signal. A computer with a RF receiver captures the sensed data from the IoT smart node. The remaining 35 seconds are scheduled as an idle mode for the smart node circuits; however, the harvesting system keeps trickle charging the Lithium battery. From the transient figure, the harvesting system provides a 3.3 V supply with a 410 mV overshoot. Owing to the feedforward hysteresis regulation, the load overshoot cannot load the PV source and harvesting system.

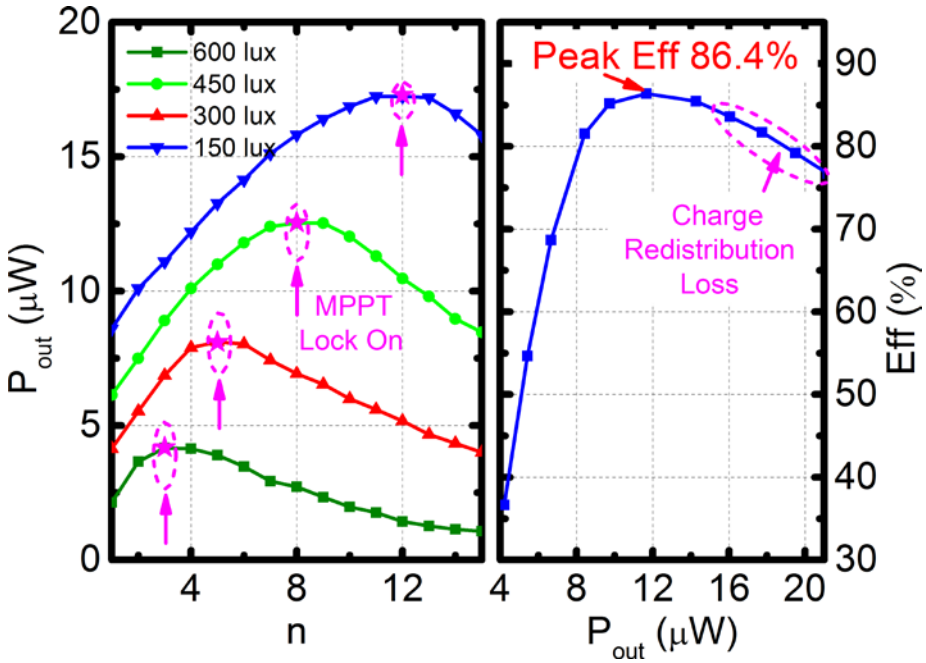


Figure 76. (Left) Output power with different capacitor values n under different light intensities and corresponding MPPs, and (Right) end-to-end peak efficiency with MPPT vs. different PV power.

The accuracy of MPP tracking was characterized through sweeping tests. The MPPT module was disabled, and the capacitor bank was programmed by an external computer through the I/O communication ports. The harvested power versus the

programmed number n is depicted in Figure 76 under different light intensities from 150 lux up to 600 lux. As a comparison, the dynamically captured MPP values are also annotated on the plot. For all four cases, the harvesting system successfully converges at the global optimal point. The MPPT tracking efficiency is 99%.

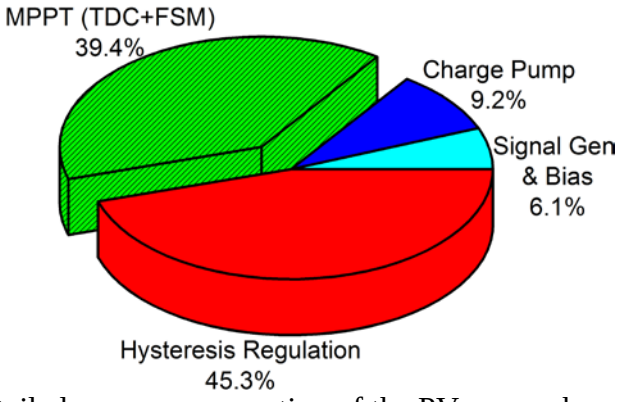


Figure 77. Detailed power consumption of the PV energy harvesting system.

Although the digital MPPT approach significantly reduces its power consumption, the overall efficiency mainly depends on the dynamic pattern of the MPPT procedure. If the FSM initiates the MPPT module after a long time, such as every several seconds, the energy loss during the fast MPPT procedure is negligible. When the FSM triggers the MPPT module every 0.3 second, the output power begins to decrease. However, the MPPT procedure can be dynamically triggered by the microcontroller and sensors in the load. When the sensors detect that the environmental illumination is rapidly changing, the triggering frequency is increased. If the illumination is stable or slow changing, the microcontroller seldom triggers the MPPT procedure to save power. The end-to-end peak efficiency with active MPPT versus different MPP is demonstrated in Figure 76, in which the harvester maintains efficiencies greater than 78% with output

power above 8 µW. Further increasing the illumination intensity will induce higher VMPP, which deviates from $V_{out}/3$ due to the use of the 3× charge pump and suffers the charge redistribution loss [85].

The detailed power consumption of the proposed system is shown in Figure 77. Due to the digital feature of the control circuits, the entire power consumption with active MPPT is as low as 294 nW.

Table 10. Performance comparison of PV energy harvesting systems with MPPT.

	[42]	[43]	[94]	[46]	[97]	[53]	This Work
Technology	0.35-µm	0.35-µm	0.25-µm	0.35-µm	65-nm	0.13-µm	0.18-µm
Fully-integrated	Yes	Yes	No	No	No	Yes	Yes
Self-sustainability	No	No	Yes	Yes	Yes	Yes	Yes
Output Regulation	No	Yes	No	No	No	Yes	Yes
Input Range (V)	2.1-3.5	1-2.7	0.5-2	1.5-5	>0.08	1.8	1.1-1.5
Output Range (V)	3.6-4.4	2	0-5	0-4	~1.3	1.4	3.3
Throughput Power (µW)	100-775	0-80	5-1000	800	<80	<10	<21
Peak Dynamic Efficiency with MPPT	67% @529 µW	86% @35 µW	70% @16 µW	84.3% @800 µW	72% @25 µW	58% @11 µW	86.4% @12 µW
Efficiency with Low PV Power @10 µW	N/A	33%	68%	54%	42%	57%	85%

Table 10 compares the performance of the proposed work with other state-of-the-art MPPT harvesters. This harvester uses on-chip switched capacitors and features monolithic integration. The peripheral circuits, including the hysteresis controller, FSM and the clock generator, are all powered by the harvester and auxiliary charge pump. Thus, the entire harvesting system is self-sustaining and needs no external bias. For controlled trickle charging, the output voltage is regulated at 3.3 V with a 150 mV ripple. The measured harvested power ranges from 0 to 21 µW depending on the illumination condition. For ordinary operation where the incoming dim indoor light is 420 lux and the MPPT module is operated in the active mode, the dynamic overall efficiency can achieve a peak value of 86.4% while delivering 12 µW of throughput power. The proposed harvester achieved a superior performance compared to reported results, which could only achieve good efficiencies with a large amount of PV power in the hundreds of microwatts, or harvest a small amount of power below 20 µW but with poor efficiency [8], [46], [47], [51]-[53], [97]. In summary, this PV energy harvesting system achieved both ultra-low power capability and excellent self-sustaining efficiency at the same time.

4.2.3 Conclusion

This work proposes a monolithic highly efficient µW-level photovoltaic energy harvesting system targeted for smart nodes in IoT networks capable of powering various loads such as sensors, signal processors and wireless transceivers. Due to the stringent power budget in IoT scenarios, the power consumption of the harvesting system was optimized by the proposed architecture and circuit level innovations. Firstly, the hill-

climbing MPPT mechanism reused and processed the information of the hysteresis controller in the time-domain and was free of power hungry analog circuits. Secondly, the power-performance tradeoff of the hysteresis controller was solved by the proposed self-triggered one-shot mechanism, allowing the output regulation to achieve high-performance and yet low-power operations. Thirdly, the CVM scheme was proposed instead of the conventional frequency modulation scheme, avoiding high quiescent power consumption. The harvesting system, fabricated in 0.18-µm CMOS technology, was tested on a temperature sensing smart node including a sensor, microcontroller, and a wireless transceiver. The system provided a 3.3 V regulated voltage and achieved an end-to-end efficiency of 86.4% with a throughput power as low as 12 µW. Startup and auxiliary bias circuits were also implemented to provide a self-sustaining operation when the system woke up from a completely dark environment.

4.3 EH System with Two-Dimensional MPPT

4.3.1 Circuit Implementation & Design Procedure

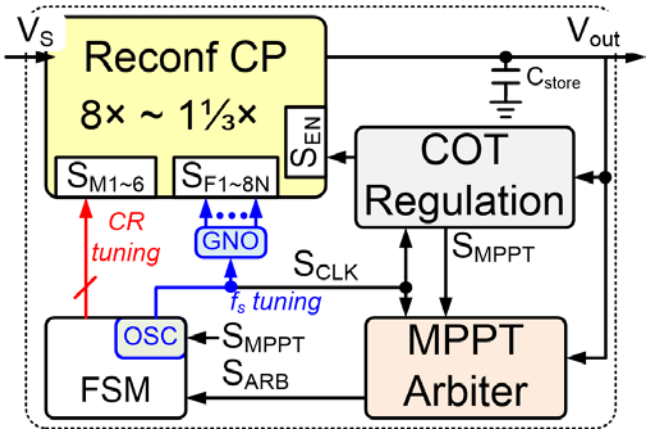
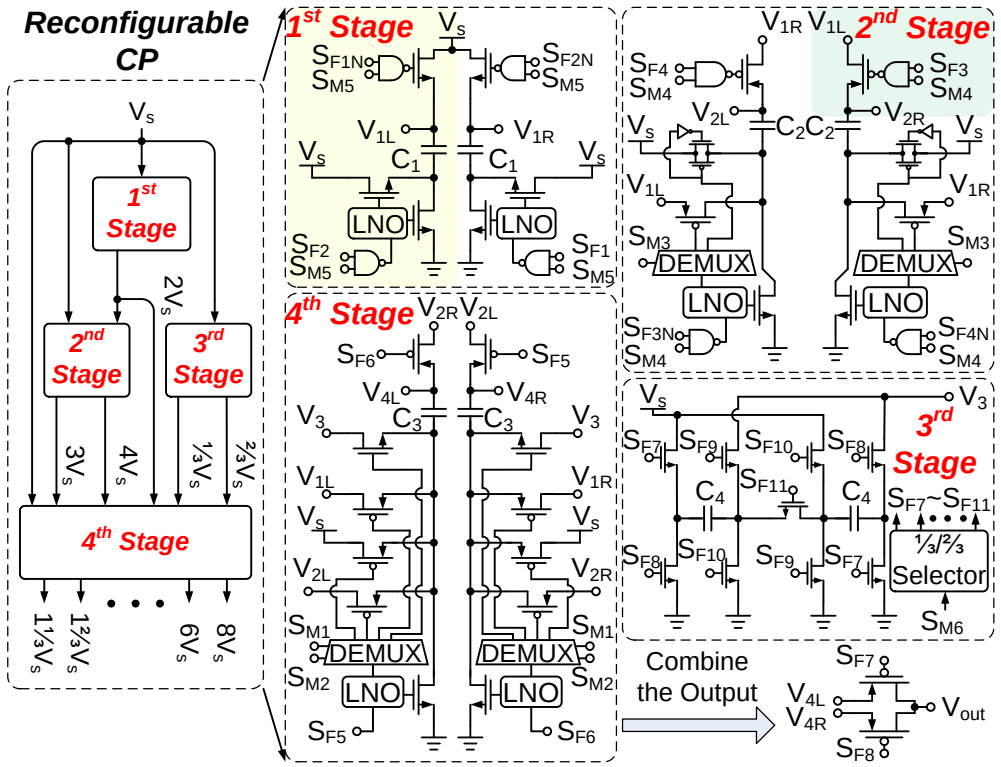


Figure 78. Implemented architecture of the reconfigurable energy harvester.

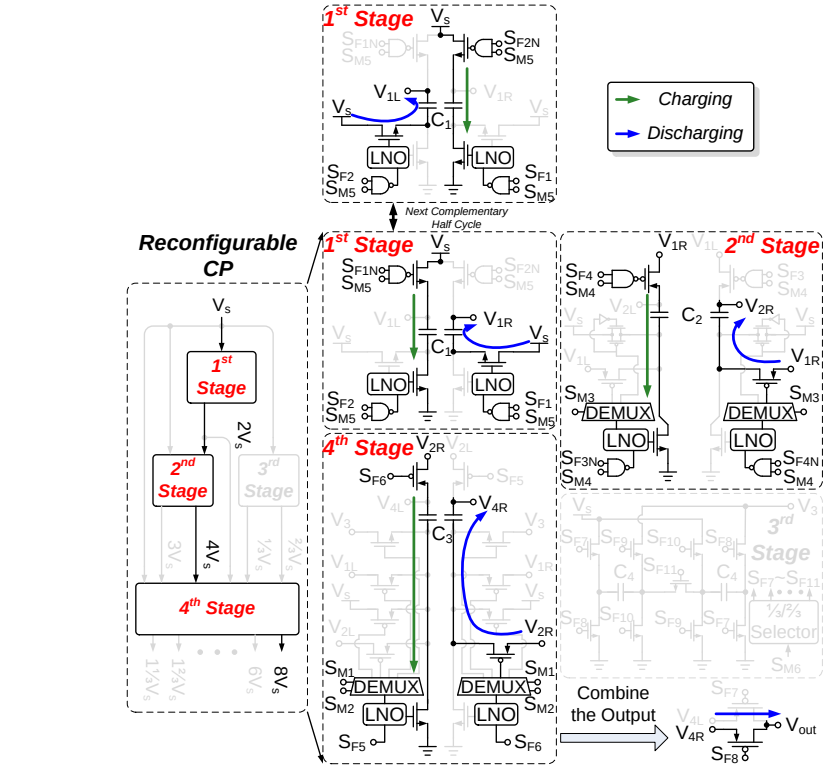
The proposed energy harvester depicted in Figure 42 was implemented as shown in Figure 78. Its building blocks will be discussed next.

4.3.1.1 Reconfigurable 3-stage Voltage Doubler

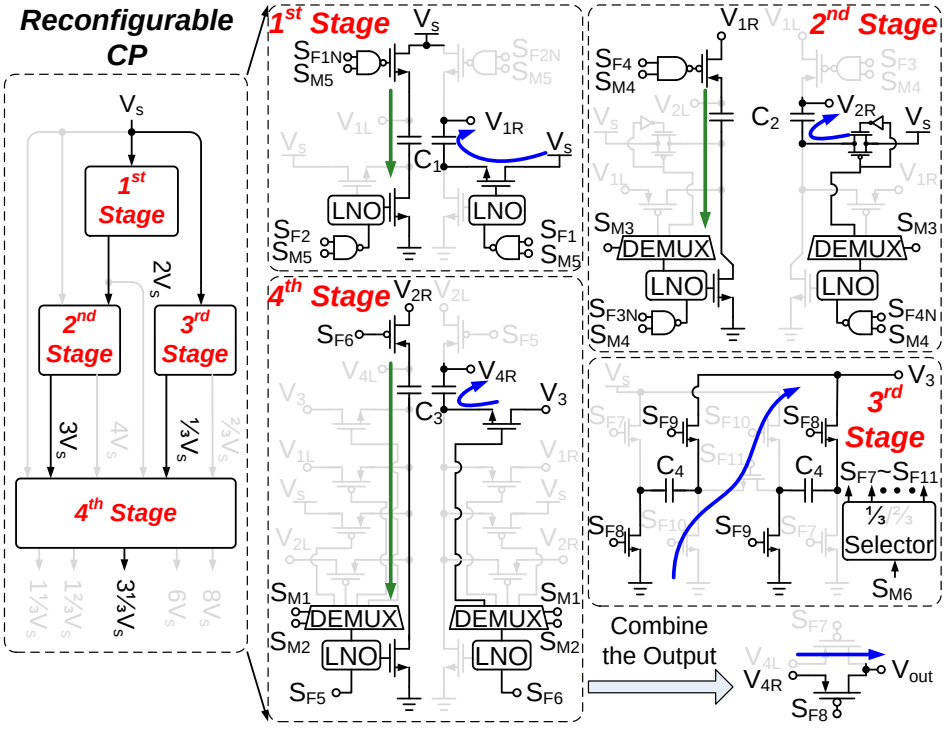


(a)

Figure 79. (a) Architecture of the reconfigurable charge pump, and its operation at (b) CR = 8×, (c) CR = 3⅓×, (d) CR = 1⅓×.

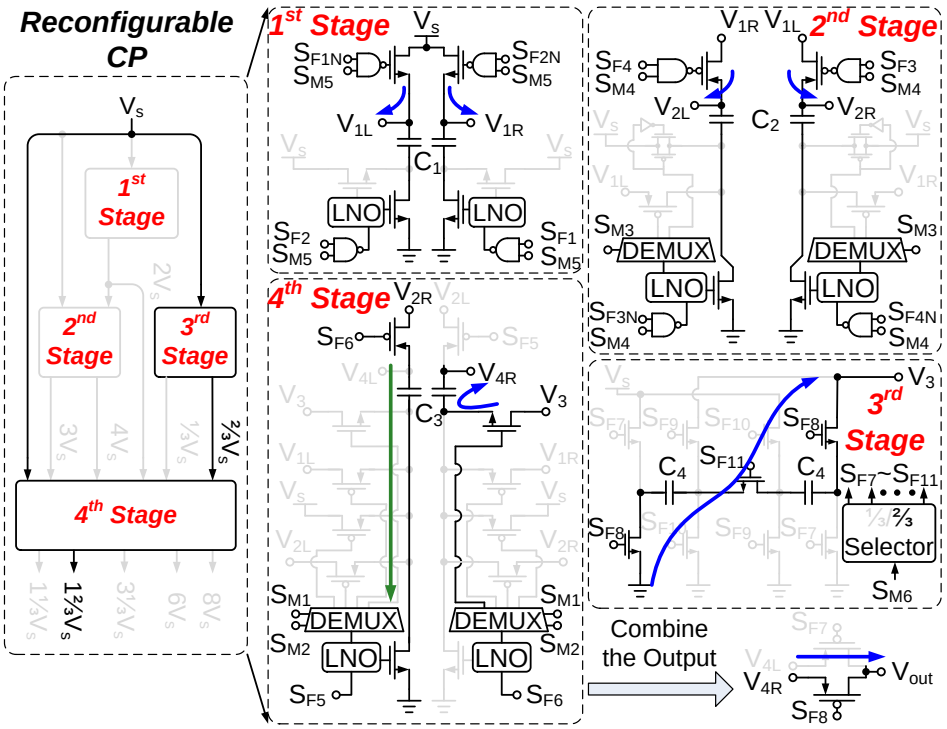


(b)



(c)

Figure 79. Continued.



(d)

Figure 79. Continued.

The reconfigurable charge pump proposed in Section 3.3.2 and Figure 45 is redrawn in the left block diagram of Figure 79(a). The nested structure features the least number of switches and capacitors for high CR [92]. The detailed schematics of its stages are illustrated in the right of Figure 79 (a). $C_{1,2,3,4}$ have an identical capacitance of 62.7 pF. The first stage boosts V_s up to $2V_s$. The second stage boosts the output of first stage, V_{1L} and V_{1R}, to $3V_s$ or $4V_s$. The different voltages are selected by S_{M3} and a 2-way selector, which is composed of a 1-bit demultiplexer, transmission gate and PMOS switches. The third stage is a ⅓× or ⅔× fractional charge pump. Its proper switching signals, $S_{F7\text{-}F11}$, are selected by S_{M6}. The fourth stage combines the former results together. Its top input is connected to V_{2R} and V_{2L}. Its bottom input is connected by $S_{M1,2}$

and 4-way selectors, which are composed of a 2-bit demultiplexer and switches. The final outputs of the charge pump, V_{4L} and V_{4R}, are complementarily combined with $S_{F7,8}$.

Table 11. Reconfiguring signals for the CR tuning.

CR	Reconfiguring Signals					
	S_{M1}	S_{M2}	S_{M3}	S_{M4}	S_{M5}	S_{M6}
8	H	L	L	H	H	L
6	L	H	L	H	H	L
5	L	L	L	H	H	L
4⅔	H	H	L	H	H	H
4⅓	H	H	L	H	H	L
4	L	L	H	H	H	L
3⅔	H	H	H	H	H	H
3⅓	H	H	H	H	H	L
3	L	L	H	H	L	L
2⅔	H	H	H	H	L	H
2⅓	H	H	H	H	L	L
2	L	L	H	L	L	L
1⅔	H	H	H	L	L	H
1⅓	H	H	H	L	L	L

To better illustrate the reconfigurable feature, CR = 8×, 3⅔×, and 1⅓× are shown in Figure 79(b)-(d). They show half cycle of the switching operation, where the green and blue arrows represent the charging and discharging currents, respectively. In the following half cycle, the right side and left side branches of the CP swapped their

functions. A subplot of next half cycle for the first stage is given in Figure 79(b). The complete control signals for reconfiguring, $S_{M1\text{-}6}$, are listed in Table 11.

1) When CR = 8×, the two-way selector in the second stage chooses $V_{1R,L}$, resulting in $V_{2L,R} = 4V_s$. The third stage is shut down to save power. The 4-way selector in the fourth stage chooses $V_{2R,L}$, resulting in $V_{4R,L} = 8V_s$.
2) When CR = 3⅓×, the two-way selector in the second stage chooses V_s, resulting in $V_{2L,R} = 3V_s$. The third stage provides $V_3 = ⅓V_s$. The 4-way selector in the fourth stage chooses V_3, resulting in $V_{4R,L} = 3⅓V_s$.
3) When CR = 1⅔×, $S_{M4,5}$ disables the switching signals and bypasses the first and second stages as $V_{2R,L} = V_s$. The third stage provides $V_3 = ⅔V_s$. The 4-way selector in the fourth stage chooses V_3, resulting in $V_{4R,L} = 1⅔V_s$.

4.3.1.2 Non-overlapping Switching Signal Planning

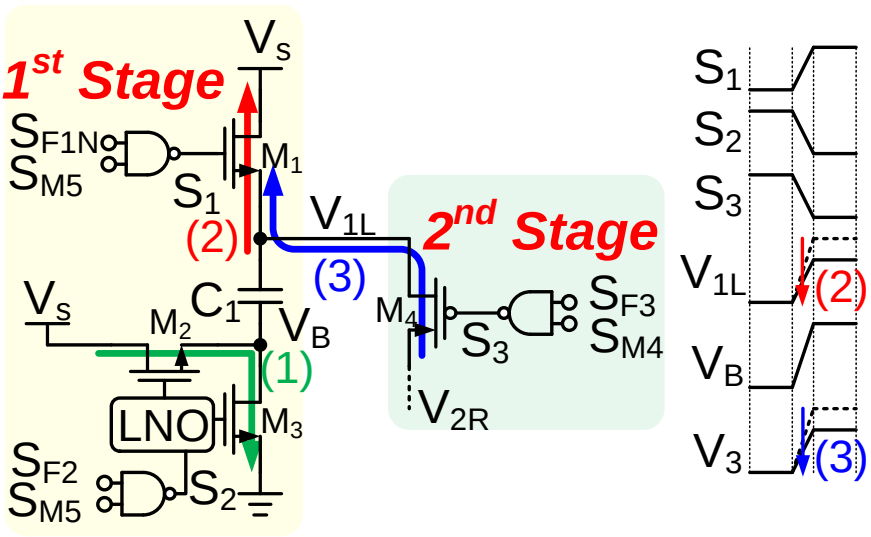


Figure 80. Principle of the shoot-through current during switching in the voltage doubler.

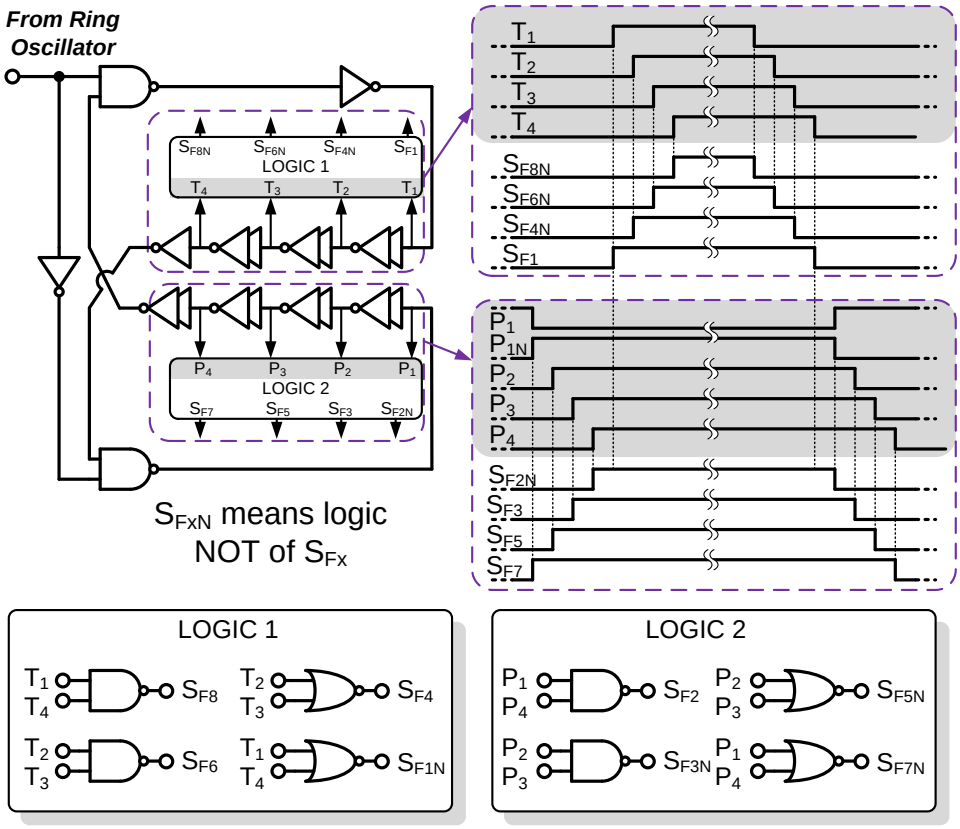
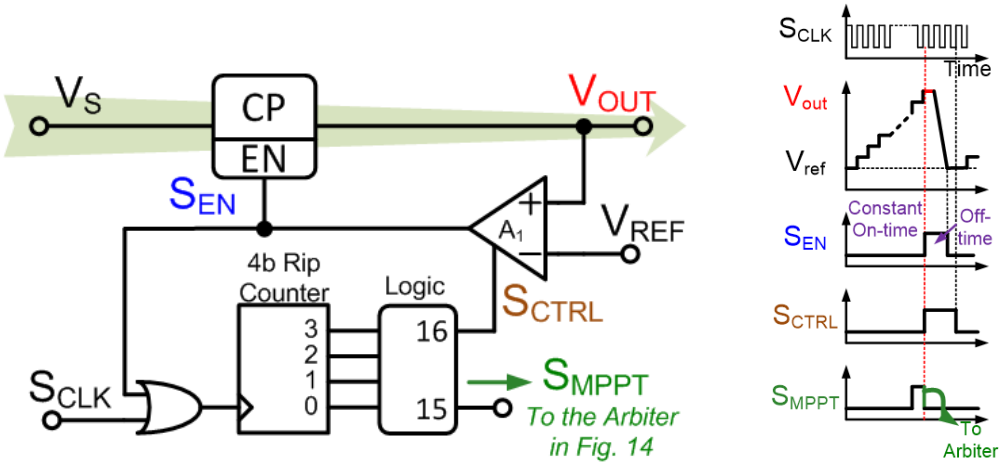


Figure 81. Generation of the global non-overlapping signals.

Shoot-through current and its energy loss increase quadratically with boosting voltages [95]. When the complementary switching clocks are overlapped, the cascaded voltage doublers suffer from three leakage paths. For an example, the first stage highlighted in Figure 79(a) is replotted in Figure 80. Path 1 happens when the high-side switch, M_2, and the low-side switch, M_3, are simultaneously turned on. It is prevented with 1.7 ns dead time by a NAND based local non-overlapping (LNO) signal generator [91]. Path 2 occurs at the beginning of charging phase: When M_1 and M_2 are both weakly turned on, the boosted V_{1L} will leak into the former stage. Path 3 occurs at the beginning of discharging phase: when M_1 and M_3 are both weakly turned on, the boosted high voltage from the following stage, V_3, will leak into the former stage.

Path 1 and path 2 are more complex because they involve multiple cascaded stages. Therefore, a global non-overlapping (GNO) generation scheme is proposed to tackle the shoot-through problem, which is shown in Figure 81. Different from the conventional approaches [96], the cascaded delay cells are placed in the feedback path and generate $T_{1\text{-}4}$ and $P_{1\text{-}4}$ with 6.1~9.5 ns dead time. Then, two combination logic circuits correctly combine them and generate the switching signals, $S_{F1\text{-}7}$, for the reconfigurable charge pump. They have cascaded and incorporated shapes, which ensure no shoot-through currents during boosting.

4.3.1.3 Constant-on Regulation



(a) (b)

Figure 82. (a) Schematic of the proposed constant-on time regulation, (b) its operating waveforms.

The implemented COT regulation and its operation waveforms are shown in Figure 82. The T_{on} is implemented with 16 system clock by a 4-bit ripple counter. Firstly, the charge pump is switched during T_{on} period and transfers charge from energy sources to the load. At the end of T_{on}, the low power latched [91] comparator A_1 is

turned on, and $V_{out,pk}$ is compared with V_{ref}. If $V_{out,pk} < V_{ref}$ and $S_{CTRL} = 0$, the available Pout is not large enough to supply the load at the regulated V_{ref} level. Such a loading effect disables the regulation function and starts the next Ton immediately with coming S_{CLK}. If $V_{out,pk} > V_{ref}$ and $S_{CTRL} = 1$, P_{out} is more than enough to supply the load, and the charge pump is shut down to let $V_{out,pk}$ be discharged and achieves the regulation purpose. Once $V_{out} < V_{ref}$, the charge pump is enabled again for the next Ton operation.

4.3.1.4 Two-channel S/H MPPT Arbiter

The hill-climbing MPPT algorithm proposed in Section 3.3.3 is executed by a two-channel sample and hold (S/H) MPPT arbiter as illustrated in Figure 83(a) and (b). The step-by-step hill-climbing algorithm is the simplest in complexity and facilitates minimum power consumption. However, its speed is relatively slow, but it can be accelerated by prior information detectors such as ADCs with the skip algorithm. The tradeoff is its additional power consumption which affects the stringent power budget of the IoT energy harvesting. Its driving clock, S_{MPPT}, comes from the COT regulation in Figure 82(b). Firstly, at the end of the first T_{on}, S_{MPPT} samples and holds the $V_{out,pk}$ at $C_{s1,2}$ as $V_{C1,2}$ in Figure 83(a). S_{MPPT} is asynchronous to reduce the complexity and power consumption. To detect the trend of P_{out}, V_{C1} is subsequently compared with V_{C2}. The relative values of C_{s1} and C_{s2} are not sensitive to the comparing accuracy, relaxing the matching requirement of the layout. According to the MPPT mechanism described in Section 3.3.3, if Pout starts decreasing, the maximum power point (MPP) has been captured, and $S_{ARB} = 0$ to lock the energy harvester working at current CR and f_s. If P_{out} keeps increasing, the MPP has not arrived, and $S_{ARB} = 1$ keeps tuning CR and f_s.

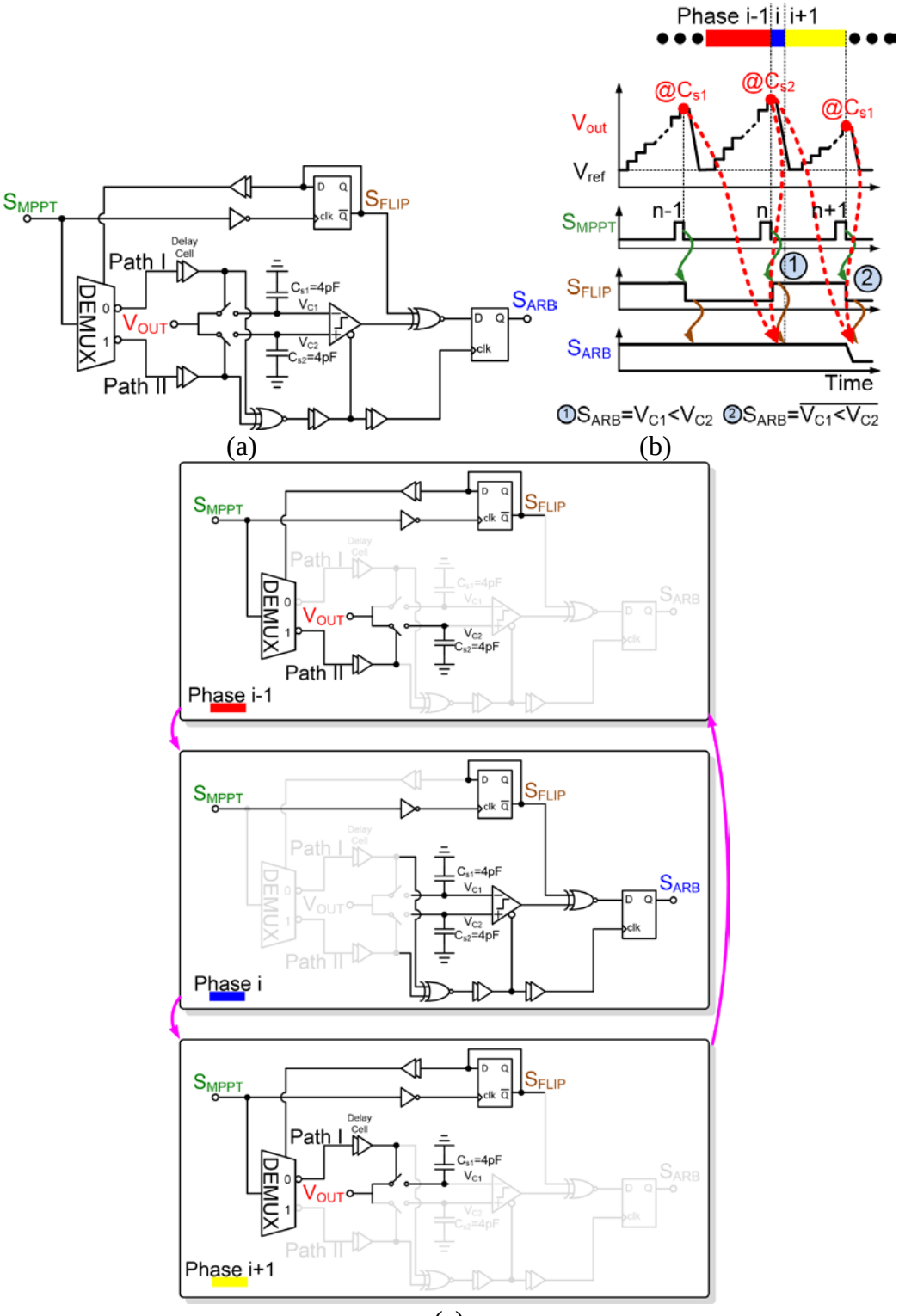


Figure 83. (a) Architecture of the two-channel S/H MPPT arbiter of Figure 78, (b) its operating waveforms, and (c) its operation in three periodic phases: i-1, i, and i+1.

To sample P_{out} only once and save logic gates, the S/H circuit is reused for each comparison. It can be decomposed into three periodic phases as shown in Figure 83(b) and (c). During phase i-1, the $V_{out,pk}$ is latched upon C_{s2} as V_{C2} and named as state n. During phase i, state n-1 (V_{C1} stored at C_{s1}) and n (V_{C2} stored at C_{s2}) are compared: if $V_{out,pk}$ keeps increasing, $S_{ARB} = V_{C1} < V_{C2} = 1$. If $V_{out,pk}$ begins decreasing, $S_{ARB} = V_{C1} > V_{C2} = 0$.

Simultaneously, S_{FLIP} is generated to flip sensing channels and the polarity of the previous comparison result. For the following n+1 state, the new $V_{out,pk}$ replaces the old V_{C1} during phase i+1. If $V_{out,pk}$ starts decreasing, S_{FLIP} corrects the logic by a XNOR gate as $S_{ARB} = \overline{V_{C1} < V_{C2}} = 0$ as illustrated in Figure 83(b). The arbiter detects that the new $V_{out,pk}$ is smaller, and a falling edge of S_{ARB} is generated.

4.3.1.5 Finite-state Machine

The MPPT procedure is conducted by a 2-bit finite-state machine (FSM) as shown in Figure 42 and Figure 78. Its detailed logic diagram is illustrated in Figure 84(a). It includes three states: idle, CR tuning and f_s tuning. As discussed in Section 3.3.2, in the idle state AB = 00, the MPPT is disabled and reduces power consumption. Once an external signal S_{TRIG} from the IoT smart nodes triggers the MPPT, FSM jumps to AB = 01 state and enables CR tuning. The driving pulse is S_{MPPT} from the regulation loop in Section 3.3.2. The output S_{CR} enables a 4-bit counter and a combinational logic block to sweep different CR values and generate $S_{M1\text{-}6}$ as implemented in Figure 84(b). Because the proposed hill-climbing algorithm stops at the status after optimal point as plotted in Figure 48, a 1-step back mechanism is proposed to calibrate the locked

operating point: a bidirectional asynchronous counter is utilized as the waveform in Figure 84(b). When one-dimensional tuning is finalized, S_{ARB} and S_{CR} are intentionally asynchronized as 0 and 1 separately. The coming S_{MPPT} pulse triggers the counter in a down direction, goes one step back to the optimal point, and subsequently quits the CR tuning.

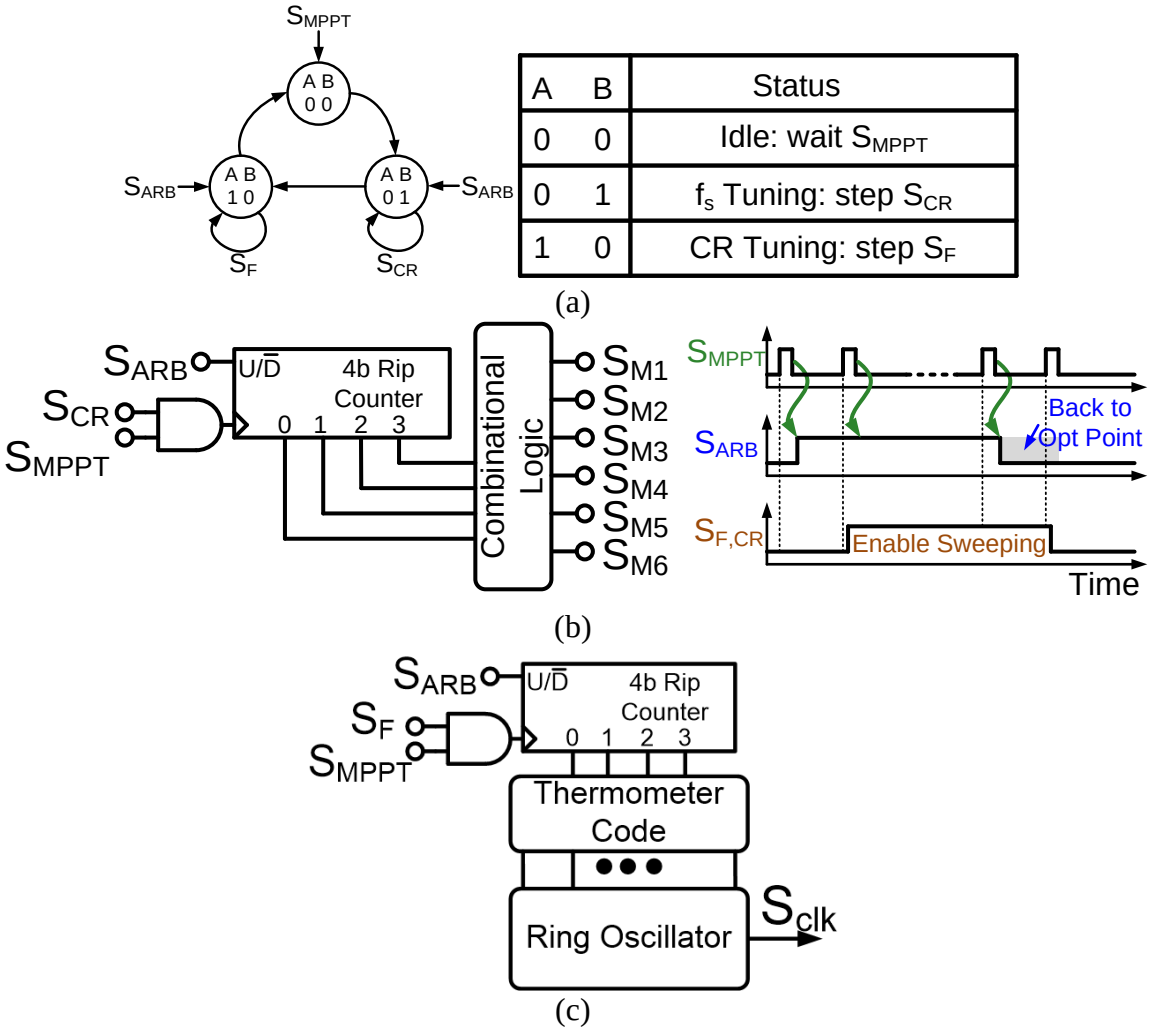


Figure 84. (a) State diagram of the finite state machine, (b) CR sweeping module, and (c) f_s sweeping module.

Once the local optimal point V_{out} is detected, the FSM falls into state AB = 10 and begins to tune the switching frequency with a current-starved ring oscillator [98] as shown in Figure 84(c). Similar to the CR tuning with 1-step back mechanism, S_F enables another bidirectional 4-bit counter and generates digitally programs the oscillator from 1 MHz down to 20 kHz in 13 steps. The 13 segments are enough for the f_s tuning; therefore, the 4 control bits are not fully decoded for saving hardware and power.

4.3.2 Measurement Results

The adaptive charge pump harvester is designed and fabricated in 0.18-μm CMOS technology. The die photo of the fabricated chip is shown in Figure 85. The entire energy harvesting system occupies a silicon area of 2 mm × 2 mm. Dual layer high density metal-insulator-metal (MIM) on-chip capacitors are used for the monolithic integration of the switched capacitors. The testing setup is illustrated in Figure 86(a). Two different PV cells and one TEG with 1.2 V, 2.5 V, and 0.6 V nominal values are tested with changing environment as shown in Figure 86(b) and (c).

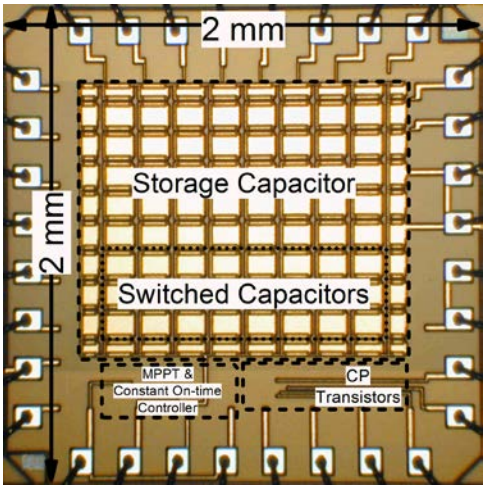


Figure 85. Die photograph of the fabricated chip.

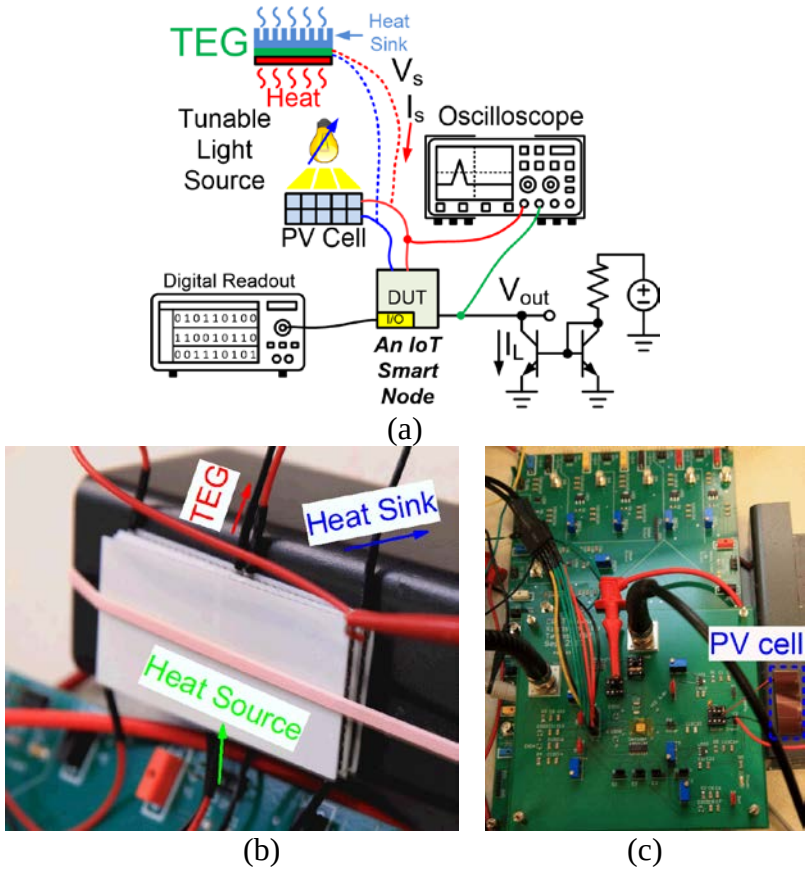


Figure 86. (a) Testing setup for the IoT smart node and detailed connection for (b) thermoelectric generator and (c) photovoltaic cell.

The transient measurements were carried out to verify the correct MPPT procedure with different energy sources. Figure 87(a), (b) and (c) illustrate different MPPT procedures for $P_s > P_{out}$ and $P_s < P_{out}$ conditions with identical P_{out} = 9.9 µW. As a generic switching DC-DC power converter, the COT scheme might induce output ripples larger than 100 mV, which does not affect the digital IoT loads [91], [99]. For the analog IoT loads, the ripple can be filtered by low-dropout (LDO) regulators [100] at the cost of conversion efficiency. Alternatively, the ripple can be passively dampened by increasing the on-chip C_{store}. In the case of $P_s > P_{out}$ as Figure 87(a), the optimal CR is firstly swept from 8× and captured as 4×. Then, f_s is tuned in six steps from 1 MHz

down to 286 kHz for a maximum peak V_{out}. In such a condition, an inevitable output ripple could be larger than 100 mV, make the COT regulation increase T_{off}, and waste redundant power between P_s and P_{out} due to the principle of energy conservation. One possible way to save that energy is using a much larger C_{store} as an off-chip supercapacitor or battery. They can dampen the ripple, decrease T_{off}, and save energy at the cost of a bulky capacitor size. For IoT loads as digital circuits, the ripple upon harvested voltage is acceptable. For analog and RF loads, an LDO is required with the corresponding dropout overhead.

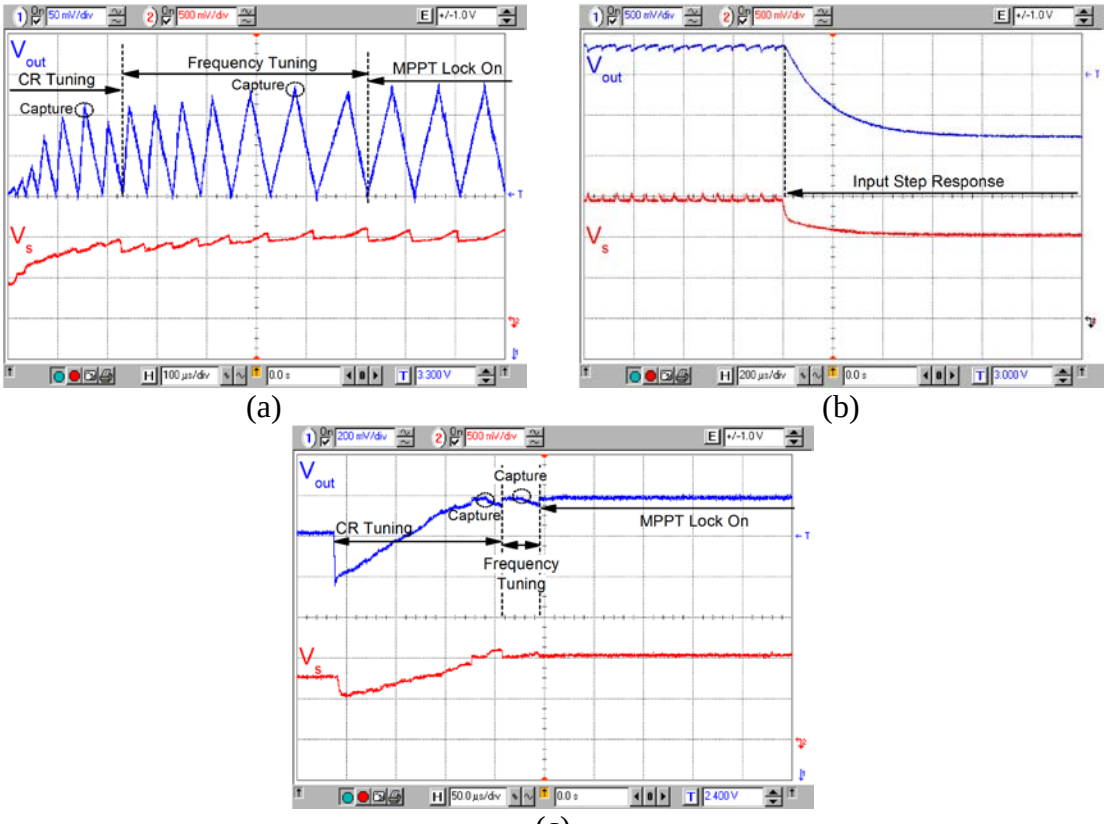


Figure 87. MPPT tracking performance with (a) light load condition with $P_s > P_{out}$, (b) a step change in V_s, and (c) heavy load condition with $P_s < P_{out}$.

In Figure 87(b), a step change in V_s was applied to the system, and the charge pump kept correctly harvesting but deviated from MPPT. In the case of $P_s < P_{out}$ as in Figure 87(c), the loading effect prevents the regulating function, skips the T_{off} period, and makes V_{out} lower than 3.3 V. However, the MPPT arbiter illustrated in Section III-E is not affected and searches the maximum $V_{out,pk}$ correctly. The captured CR is set as 3⅓× and then fs is tuned to 1 MHz for a maximum peak V_{out}. According to Figure 87(a) and (c), the entire MPPT transient is a fast procedure and can be done in less than 1 ms. On the other hand, the load is buffered by the 2.05 nF on-chip storage capacitor C_{store} in Figure 78, and its dynamics will not affect the MPPT procedure.

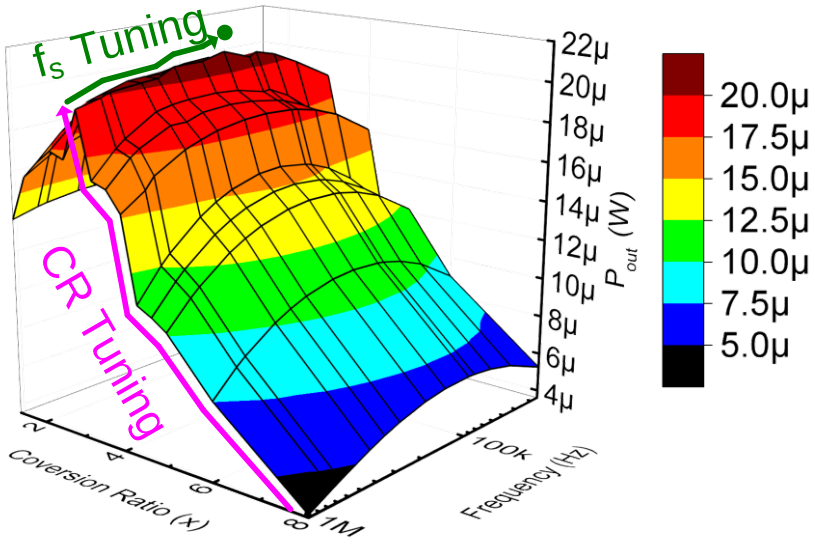


Figure 88. P_{out} vs. CR and f_s during the two-dimensional MPPT procedure.

To further reflect the procedure of the proposed two-dimensional MPPT, the output power is measured versus different conversion ratios and switching frequencies in Figure 88. Firstly, the pink CR tuning changes from small output power at 8× to the

local optimal point 3×. Then, the frequency tuning changes from high frequency at 1 MHz to the global optimal point at 140.6 kHz. Generally, CR tuning is much more sensitive than frequency tuning. This is because, as illustrated in (45), the quadratic of conversion ratio is related to the equivalent resistance.

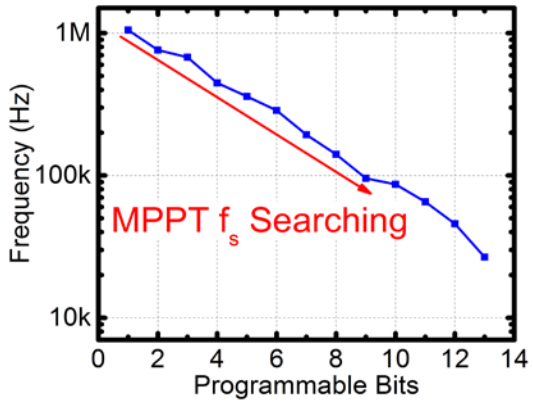


Figure 89. f_s tuning capability of the digital programmed oscillator.

The performance of the programmed ring oscillator is listed in Figure 89. The frequency is designed from 1 MHz down to 20 kHz with 13 steps. The VCE is the intrinsic performance of the charge pump and measured in Figure 90(a). To get the maximum output voltage, the load is removed as an open circuit. For characterizing the VCE, the COT regulation module and MPPT module were shut down, and the CR was manually swept from 8× down to 1⅓× for different V_s. The theoretical VCE limit is also attached to the plot as the dashed line. From the measured results, the reconfigurable charge pump successfully extends the range of harvesting voltage by combining multiple peaks together, and maintains most of it above 70%. The increased deviation from theoretical VCE value at high input voltages comes from their relative CR resolution as

1⅓×, 1⅔×, etc. When the input is as small as 0.5 V, the reconfigurable charge pump needs a high CR value as 8× as it becomes more susceptible to the threshold voltage V_{th} induced voltage drop across the switches. As a result, the VCE is largely degraded.

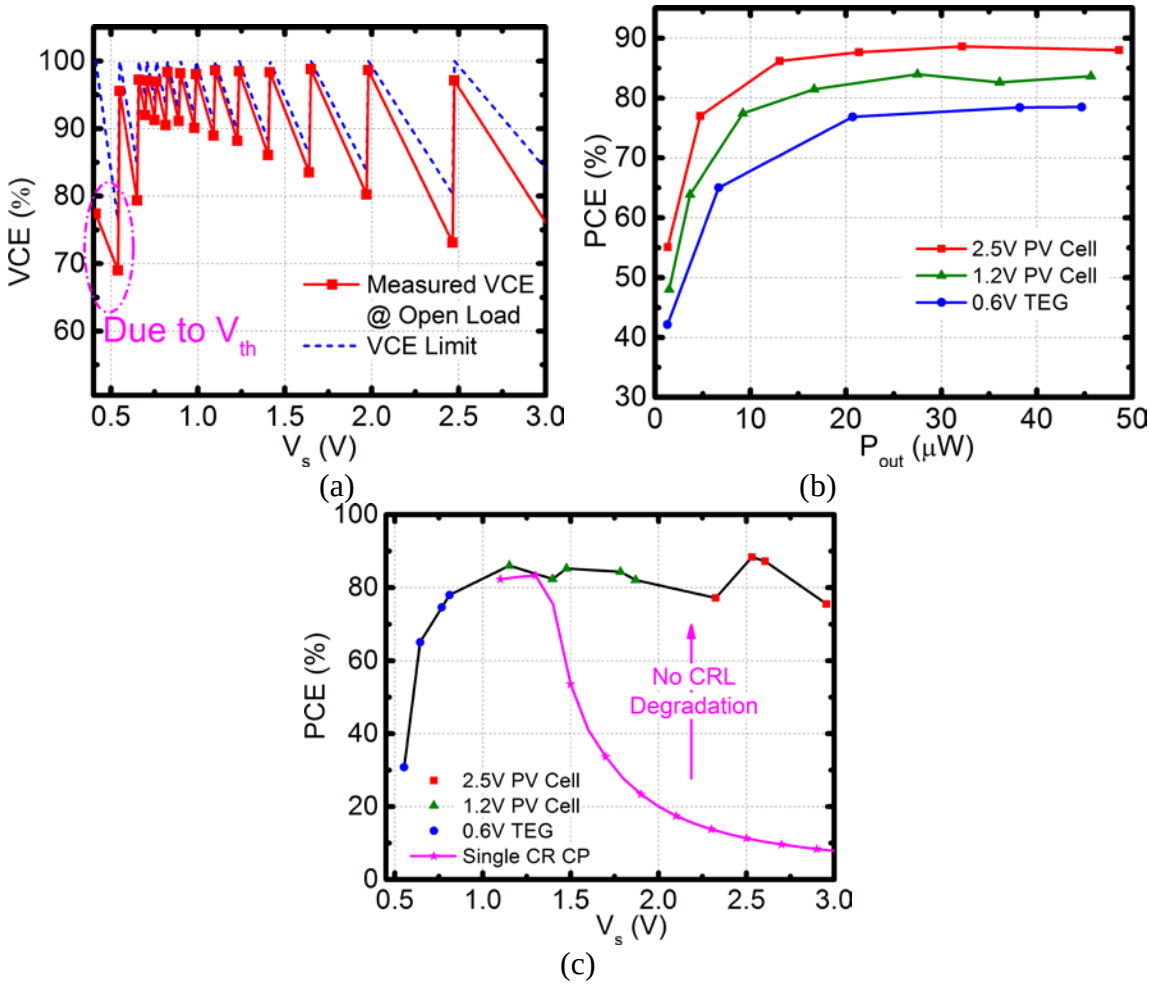


Figure 90. The measured (a) voltage conversion efficiency (VCE) between 0.45 V and 3 V; (b) power conversion efficiency (PCE) with three kinds of energy sources and various loading conditions; (c) PCE versus a wide input range and comparing with a 3× single CR CP.

The PCE is measured versus various loading conditions and two PV cells and one TEG pile with 1.2 V, 2.5 V, and 0.6 V nominal values as Figure 90(b). The power of

control circuits is self-supplied by the C_{store}. To startup the charge pump, the C_{store} needs to be precharged above 2.1 V. This can be guaranteed by replacing the C_{store} with an off-chip Li-battery and an undervoltage-lockout (UVLO) circuit. Alternatively, energy sources higher than 2.1 V will automatically charge the C_{store} and bootstrap it up to 3.3 V. However, for low voltage sources such as TEG, the startup issue has been solved by an auxiliary charge pump to precharge the C_{store} as reported in [98], [99]. These startup circuits operate only once at the beginning of normal harvesting. In this work, the design is focused on exploring the relationship between MPPT and switching variables. Thus, the auxiliary charge pump was not fabricated on-chip. The curves reflect that the reconfigurable feature successfully prevents the CRL and gives an extended and flattened harvesting efficiency up to 50 μW. For different energy sources, the higher harvesting voltage, such as the 2.5 V type PV cell, the less reconfigurable stages are stacked in Figure 79(a), and the higher achieved efficiency.

Based on the measured different energy sources, the PCE versus a wide input range is illustrated in Figure 90(c). The reconfigurable architecture combines the performance of multiple single CR CPs and maintains high efficiency across a wide harvesting voltage range. As a comparison, the PCE of a 3× charge pump is attached as the magenta line, which degrades at high V_s due to the CRL. According to Eq. (3), the harvested power is determined by the switching frequency and utilized capacitors. To increase the power density, higher switching frequency is needed. However, the dynamic power consumption will also increase and affect the harvesting efficiency. In this work,

with a stringent power budget, we used most of the chip area as capacitors and sacrificed the power density to guarantee the high conversion efficiency.

Table 12. Performance comparison of energy harvesting systems.

	[99]	[53]	[57]	[58]	This Work
Technology	0.18-µm	0.13-µm	0.18-µm	0.25-µm	0.18-µm
Topology	Boost	CP	CP	CP	CP
Fully-integrated	No	Yes	Yes	Yes	Yes
CR	Boost	Single	Reconf	Reconf	Reconf
Startup Condition	Internal Auxiliary CP	Self-supplied >0.27 V	Self-supplied >0.14 V	N/A	Self-supplied >2.1 V
MPPT Tuning	Manually	NA	1-D	1-D	2-D (Integrated)
Input Range (V)	20-70m	0.42-0.48	0.14-0.5	2.5	0.45-3
Output Range (V)	0.8-1.1	0.4-1.6	2.2-5.2	0-2.2	3.3
Throughput Power (µW)	<0.004	<10	<5	<1250	<50
PCE	53% @ Peak w/ controller	86% @ Peak w/ controller	40%-50% w/ controller	85% w/o controller	89% w/o controller 81% w/ controller

The benchmark is compared in Table 12. [99] achieves good efficiency at very low harvesting power. However, its boost converter topology relies on high quality off-

chip inductors and is not feasible for fully-integrated IoT applications. It also integrates an auxiliary charge pump with ESD diodes to provide the startup power supply. [53] utilizes the charge pump topology with on-chip capacitors, however, a MPPT function is not incorporated and is not fit for changing environment. [57] and [58] are reconfigurable charge pumps and have flattened PCE for various input voltages. [57] utilizes both the frequency modulation and reconfigurable feature but in separate loops and simple cascade connections, resulting in a complex circuits and low efficiency. Both [53] and [57] use self-supplied strategy to startup the power converter with the harvested energy. [58] focuses on step-down conversion with constant input voltage, thus it is not fit for the low harvesting voltages of energy sources. Our work proposes the energy harvester based on the monolithic charge pump topology. Its reconfigurable feature is applied by nesting voltage doublers with demultiplexers. The CR tuning is also combined with the frequency modulation as a two-dimensional MPPT mechanism. A constant-on time scheme was developed to regulate the output voltage, and its information is reused for the MPPT power sensing. The entire controller does not contain analog circuits that consumes quiescent current. When switching to maximum frequency at 1.05 MHz, the dynamic power consumption is 3.84 μW. With minimum switching frequency at 27 kHz, the dynamic power consumption can be as low as 0.4 μW. As a result, this work achieves an enhanced and flattened PCE as high as 89% without and 81% with counting the energy consumption of the controller over a wide input voltage range from 0.45 to 3 V.

4.3.3 Conclusion

This work proposes a monolithic highly efficient µW-level energy harvester targeted for smart nodes in IoT networks. Due to the variation of the available voltage and power in IoT scenarios, the charge pump was optimized by a proposed architecture and circuit level innovations. Firstly, a reconfigurable architecture was proposed to provide the hybrid CRs as 1⅓×, 1⅔× up to 8× CRs for minimizing the CRL. Secondly, the reconfigurable feature was also utilized in the maximum power point tracking with the frequency modulation, resulting in a two-dimensional MPPT. Therefore, the VCE and PCE were enhanced and flattened for wide harvesting voltage range as 0.45 to 3 V. Thirdly, the COT regulation scheme was reused with the proposed MPPT arbiter as a sensing approach, which eliminated the conventional power hungry analog circuits. The harvesting system was fabricated in 0.18-µm CMOS technology. With the help of the two-dimensional MPPT, the achieved PCE was as high as 89% without and 81% with counting the energy consumption of the controller for a throughput power below 50 µW.

4.4 EH System with a Single-cycle MPPT without Storage Capacitor

4.4.1 Motivation and Innovation

The switched capacitor power converter, also called charge pump (CP), features no off-chip components and is suitable for the monolithic smart nodes in the internet of things (IoT) [101]. To reduce the inevitable charge redistribution loss (CRL) from a fixed conversion ratio (CR), reconfigurable CPs have been proposed to dynamically change their CRs for optimized harvesting efficiency [102], [62]. However, they lacked

the startup and self-sustaining capability [103], which are vital to the power management unit for IoT. The clock generator of an energy harvester should oscillate with the initial low harvesting voltage. To realize the self-sustaining capability, the controller should rely on the harvested power of the CP, which implies an ultra-low power consumption. The conventional current-starved ring oscillator is not suitable for this microwatts power budget due to its correlated nature between speed, slew rate, and power consumption.

Another practical design challenge is the huge storage capacitor utilized at the output of charge pump. For ultra-low energy harvesting, a switch is used to isolate the charge pump and the loads, which prevents loading conditions. For the isolated CP, the storage capacitor is used to integrate and sense the output power for the maximum power point tracking (MPPT) [91]. For non-isolated CP, the storage capacitor is used to filter and dampen the output ripple [62], [103]. Such a capacitor does not help the conversion power density and wastes a lot of chip area.

In this work, a reconfigurable CP is designed for 1.8 V output. Its controller has MPPT for the input and hysteretic regulation for the output voltage. Eliminating the huge storage capacitor is accomplished by the regulation executed in one clock cycle. The regulation signals are analyzed in the frequency domain, resulting in a single-cycle MPPT that senses the output power based on digital clocking. Moreover, a thyristor-based voltage controlled oscillator (VCO) is proposed with local positive feedback for low voltage startup and reduced power consumption. The entire controller is supplied by the output of the CP, which allows it to achieve the self-sustaining capability.

4.4.2 Single-cycle Regulation and MPPT

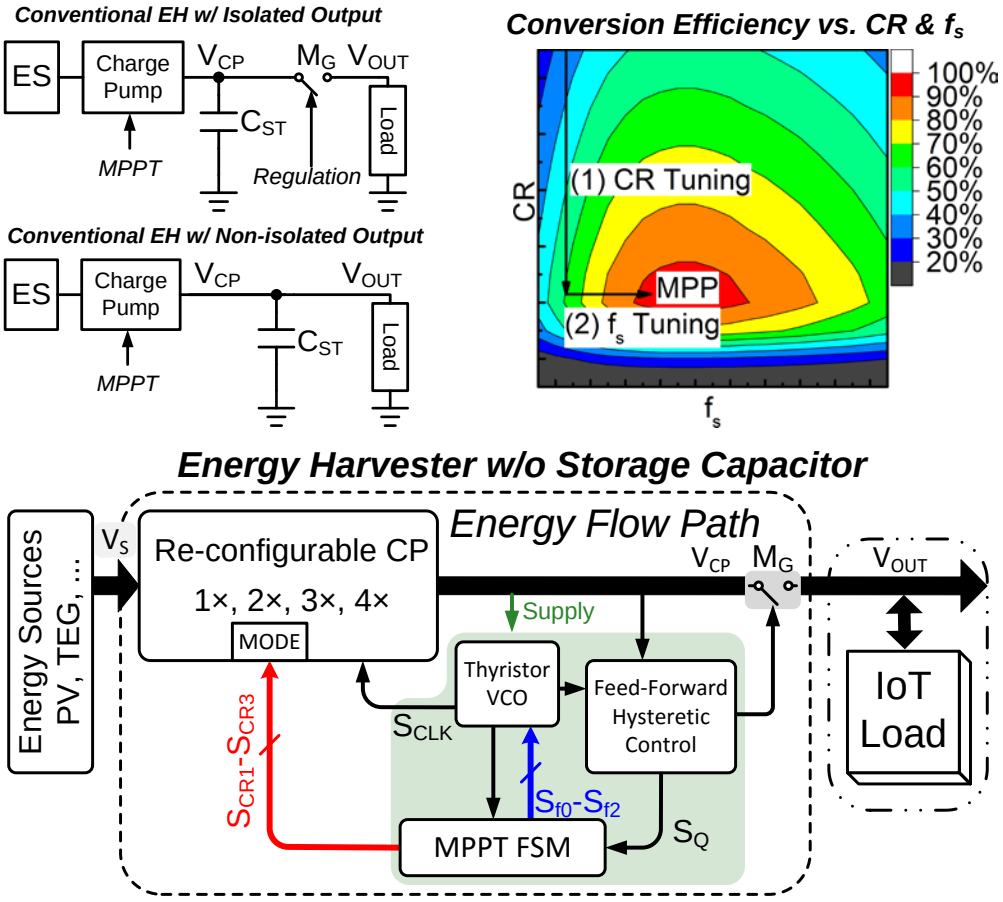


Figure 91. Architecture of the storage cap-free EH.

Figure 91 shows the conceptual architecture of the featured energy harvester. The conventional charge pump has a large storage capacitor C_{ST} for non-isolated and isolated structures, which is eliminated in this work. Two loops control the charge pump: the regulation loop works through a feed-forward hysteretic controller. Its gating signal S_Q is reused by the MPPT loop. The MPPT loop utilizes the two-dimensional hill-climbing algorithm to dynamically search the maximum power point (MPP) by tuning the CR and switching frequency f_s. A thyristor-based VCO is tuned by the MPPT controller. With

the isolation of M_G, the harvested voltage V_{CP} is not affected by the load voltage V_{OUT}, which ensures a trouble-free startup and operation even under heavy loading conditions.

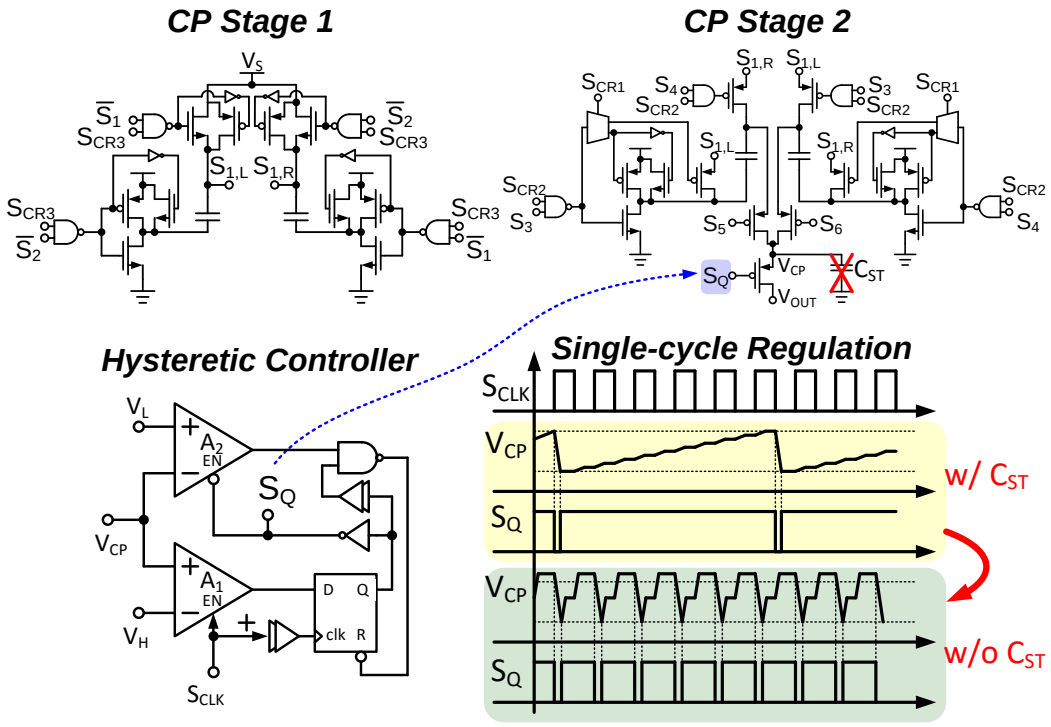
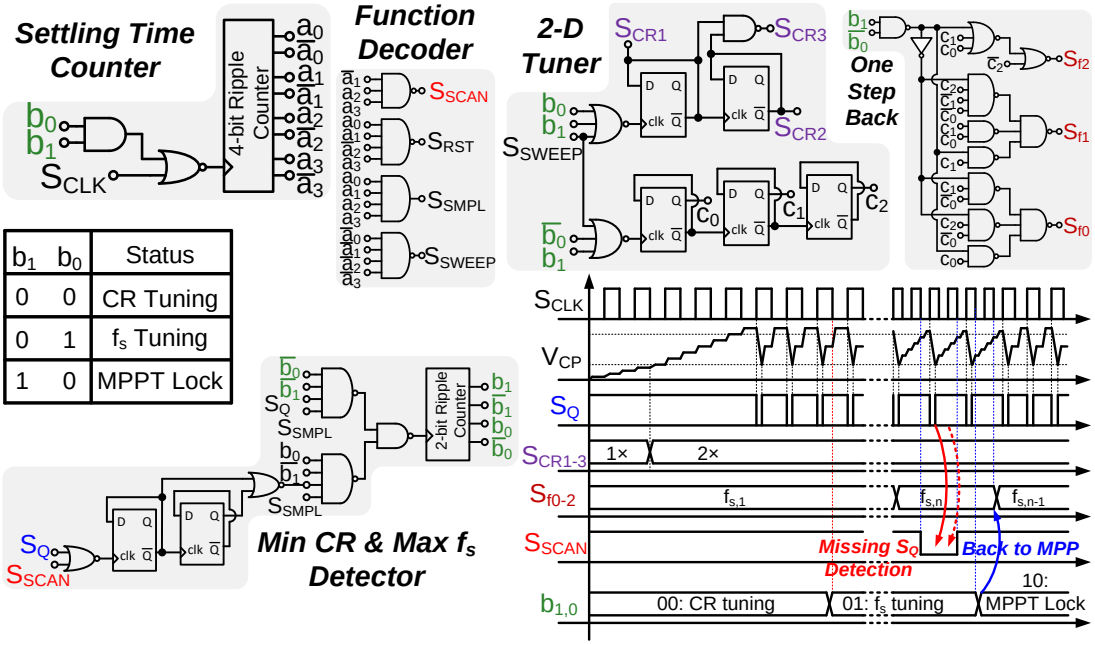


Figure 92. CP and hysteretic regulation w/o C_{ST}.

Figure 92 details the schematic of the reconfigurable CP and the regulation loop. The CP stems from cascading two voltage doublers. With a demultiplexer and proper control signals S_{CR1-3}, this structure provides a CR=1×, 2×, 3×, and 4×. The feed-forward hysteretic regulation senses V_{CP} and turns on/off the M_G. To solve the power-performance tradeoff, the window detection is split into two comparators. A_1 is an ultra-low power latched comparator and operates at each rising edge. The detection of $V_{CP}>V_H$ turns on the switch, M_G, and delivers the harvested energy to the load. Simultaneously, a high speed continuous time comparator A_2 is turned on to detect if

$V_{CP}<V_L$, S_Q will turn off M_G and A_2 to save power. Without C_{ST}, the V_{CP}'s rising period is so fast that it is finished in one switching cycle and unable to be quantized. However, in the frequency domain, the pattern of S_Q implies harvested power. When CR is low, the C_P cannot boost the input voltage to 1.8 V in any case; hence no S_Q is triggered. On the contrary, higher CR induces more CRL and decreases the power conversion efficiency (PCE). Thus, only the minimum available CR is needed for efficiently harvesting. Note that the single-cycle regulation condition causes a higher f_s; thus, more power is delivered to the load. However, when f_s is unnecessarily high, each S_Q regulation period will have more than one cycle. The CP cannot extract more power from the energy sources, it just passes over the MPP. The PCE begins to decrease due to dynamic loss of the unnecessarily high f_s.

Figure 93 illustrates the single-cycle MPPT controller to search the minimum CR and highest fs under single-cycle regulation. The finite-state machine (FSM) has three states: 1) CR tuning, 2) f_s tuning and 3) MPPT lock. Firstly, the controller starts sweeping CR from 1× with S_{CR1-3}. When S_Q appears, that means the CR is high enough to boost V_S to the required level. CR is locked and the FSM enters f_s tuning from minimum value $f_{s,1}$. With increasing f_s, S_{SCAN} searches the break condition of the single-cycle regulation, which shows only one S_Q during every two S_{CLK} and the other S_Q is missing. Once the $f_{s,n}$ with decreasing output power is detected, a one step back circuit put the switching frequency back to $f_{s,n-1}$ as the correct MPP.



b_1	b_0	Status
0	0	CR Tuning
0	1	f_s Tuning
1	0	MPPT Lock

Figure 93. FSM for a Single-cycle MPPT.

4.4.3 Thyristor-based VCO

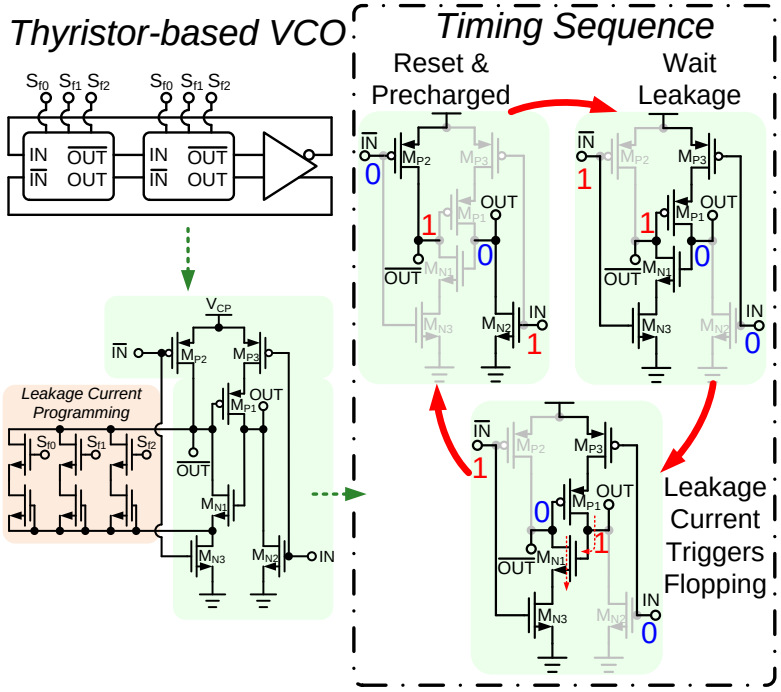


Figure 94. The thyristor-based VCO.

Figure 94 shows the schematic of the thyristor-based VCO. The conventional inverter-based topology has correlated power consumption, speed, and voltage swing. When developing for IoT energy harvesting under 1MHz, the current-starved topology simultaneously reduces gm and V_{pp}. Smaller V_{pp} and worse slew rate cause larger shoot-through current and microwatts-level power consumption when converting it into rail-to-rail clocks. On the contrary, the proposed VCO uses one inverter and two thyristors, which is emulated by $M_{P1\text{-}3}$ and $M_{N1\text{-}3}$. During the flopping period, the local positive feedback between M_{P1} and M_{N1} generates a rail-to-rail switching. Thus, no shoot-through current happens when using the generated clock. A small leakage current from the gate capacitors of $M_{N1,\,P1}$ defines the delay and power consumption. A binary weighted 3-bit resistor bank is added across M_{N1}. These branches add additional leakage paths, accelerate the discharge rate, and increase f_s.

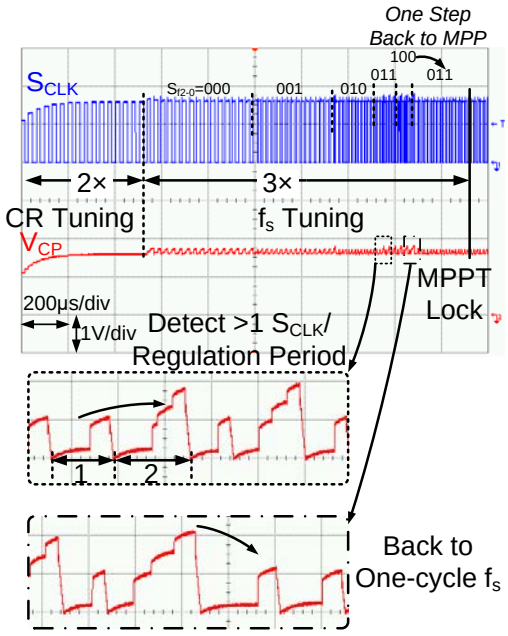


Figure 95. Startup and MPPT tuning transients.

Figure 95 demonstrates the startup and MPPT transients of the energy harvester with a modeled thermoelectric generator with 1.2 V open circuit voltage. Once starting up, the CP firstly starts the CR tuning. When CR=3×, the output voltage is boosted to the 1.8 V level, and the FSM locks the CR. The fs tuning follows and the FSM detects the missing S_Q happening at $S_{f2\text{-}0}$ = 100. Therefore, the FSM enters a MPPT lock state and corrects the control bits of fs back to the previous $S_{f2\text{-}0}$ = 011.

Figure 96 shows the characteristics of the VCO and the performance of the energy harvester. Compared with the reported works, this work simultaneously addresses the challenges of the energy harvesting for IoT, including the startup issue, the self-sustaining capability, the regulated output, and eliminating the storage capacitor.

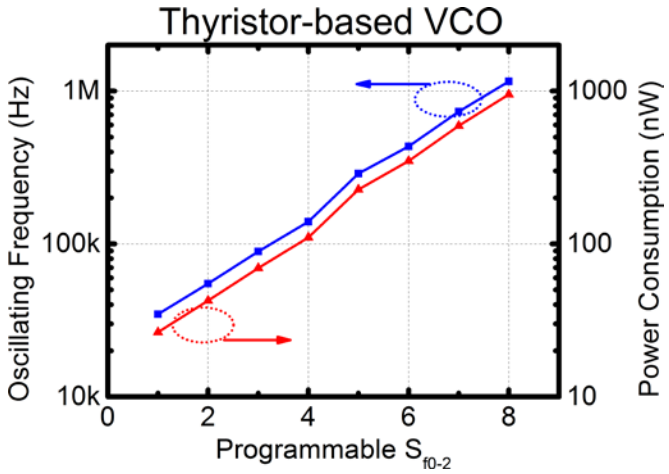


Figure 96. Performance of the thyristor-based VCO.

4.5 Conclusion

The analog current sensor with capacitor value modulation is developed for reduced power consumption and enhanced peak conversion efficiency 89% under 29

μW. Furthermore, a novel digital approach to execute the MPPT in time-domain and save the quiescent power consumption. Consequently, the entire harvesting efficiency is improved to 86.4% with a throughput power as low as 12 μW. The third implementation is focus on better matching the energy sources and achieving a wide harvesting range as 0.45 to 3 V. The fourth example applies the single-cycle regulation and MPPT for eliminating the on-chip storage capacitor and compact size.

5 POWER MANAGEMENT FOR ELECTRICAL SCALPEL*

5.1 Background of UVSD System

Vessel sealing and dissection using ultrasonic transducers provides good performance over conventional electrosurgery. The purely mechanical action of the ultrasonic actuator eliminates the passage of electric current through the patient. A good power regulation ensures great precision and proper surgical jobs. To achieve this, precise amplitude control is needed.

5.1.1 Characteristics of the PT

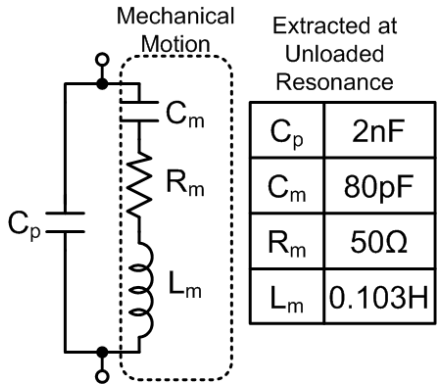


Figure 97. Electromechanical model of the piezoelectric transducer at resonance.

A number of equivalent circuits have been developed over the years for PT [104]. In the vicinity of resonant frequency, the most commonly used model is the Butterworth-Van Dyke (BVD) model [105]. The PT in resonant mode can be modeled as

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a band-pass filter with a high quality factor Q. The electromechanical model used is shown in Figure 97, where C_m, R_m, and L_m in the mechanical motion branch represent the compliance, loss, and mass of the PT. C_p represents the capacitance of the electrodes upon PT. With sufficient cooling and regulated output power, its temperature coefficient can be neglected. In this application, $C_p >> C_m$. R_m also indicates the mechanical loading. The impedance of the PT in resonance is expressed as,

$$Z_{in}(s) = \frac{1}{sC_p} \frac{\left(s^2 + s\frac{R_m}{L_m} + \frac{1}{L_m C_m}\right)}{\left(s^2 + s\frac{R_m}{L_m} + \frac{C_m + C_p}{L_m C_m C_p}\right)} \tag{51}$$

where two natural frequencies, resonance and anti-resonance, can be extracted as,

$$\omega_{0,R} = \sqrt{\frac{1}{L_m C_m}}; \quad \omega_{0,AR} = \sqrt{\frac{C_m + C_p}{L_m C_m C_p}} \tag{52}$$

where $\omega_{0,R}$ represents the correct longitudinal mechanical resonant frequency as shown in Figure 98. At this mechanical resonant frequency, the PT appears as a damping resistor R_m in parallel with the capacitor C_p, maximizing the amount of electrical power converted to mechanical motion.

5.1.2 Design Challenges

Piezoelectric transducers are widely used as mechanical actuators to convert electrical signals into precisely controlled physical displacements for various purposes, such as vibrating air, moving material, and generating heat [106]-[110]. The main challenge is to generate the mechanical power in the desired PT resonant mode with high electrical efficiency. Theoretically, the PT converts electrical real power into mechanical

motion; however, some energy can easily be dissipated due to the reactive elements of the transducer. Thus, for a high-efficiency system, the PT must be driven in the correct resonant mode to minimize its reactive power and realize maximum power transfer (MPT) [111]. There are multiple methods to drive the PT in resonance, including power factor correction (PFC)-based [106], [112]-[115], and phase-locked loop (PLL)-based [107]-[110], [116] solutions. PFC-based systems require additional reactive components and complicated compensation to minimize the reactive part of the PT impedance and thereby put the PT into resonance. PLL-based systems drive the PT in a closed-loop. However, they have a limited lock-in range and require a complex compensation to stabilize under large loading conditions [109].

The second challenge is that the PT has multiple resonant modes, which shift with load variation. For various loading conditions, the PT should be tracked in the designed resonant mode and not fall into other undesired resonant frequencies. Therefore, complex frequency or phase discriminators for driving signals are needed [115]. The third challenge is to precisely control the amplitude of the PT displacement and ensure proper mechanical functions. Thus, the electrical power delivered to the PT needs to be accurately regulated. Regulating schemes such as Burst-mode control have been proposed to achieve good efficiency at light load conditions. However, these regulating schemes did not sufficiently improve the PT wake-up time [117].

Different from the aforementioned solutions, this work proposes a band-pass filter (BPF) oscillator-based automatic resonance tracking scheme which is conventionally used in an atomic force microscope (AFM) [118]-[120]. In this

electrosurgical scenario, the tracking scheme utilizes the intrinsic mechanical characteristics of the PT as a BPF in the oscillator [121]-[122], providing automatic and accurate resonance tracking regardless of device variations and environmental interferences. Therefore, maximum electrical power is converted into mechanical motion. In addition, the reuse of the PT as the BPF prevents any undesired resonant modes, eliminates the frequency discriminator, and features much less complexity. A switching power stage with high power efficiency is proposed to regulate the output mechanical power. Its amplitude control is implemented by a closed-loop architecture with negative feedback [123]. The controlled signal is the resonant current corresponding to the mechanical motion of the PT.

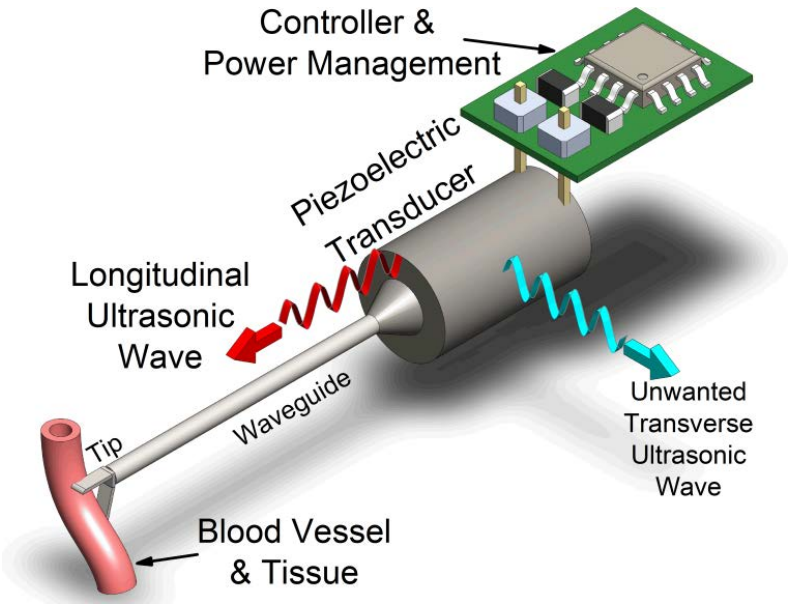


Figure 98. Architecture of the ultrasonic vessel sealing and dissecting (UVSD) system.

The proposed BPF oscillator-based scheme is illustrated for an ultrasonic vessel sealing and dissecting (UVSD) system as depicted in Figure 98, where accurate PT

displacement regulation over a wide range of loads is required. Unlike electrosurgery devices based on joule heating [124]-[126], the PT-based UVSD devices feature outstanding hemostasis and efficient dissections with minimal lateral thermal damage and low smoke generation. Furthermore, it has no risk of electrical current flowing through the patient [127]. The PT has both longitudinal and transverse resonance modes. Only the longitudinal ultrasonic wave can be transmitted by the waveguide and used for mechanical operation. Thus, the proposed controller automatically drives the PT in such mode and regulates the oscillating amplitude. The unwanted transverse mode is prevented by the BPF oscillator detailed in Section 5.2.2.2. The surgical sealing and dissecting for blood vessels and tissue are achieved by the tip at the other end of the waveguide as illustrated in Figure 98.

5.2 Discrete Version: Automatic Resonance Tracking Technique

5.2.1 Motional Current Sensing Bridge

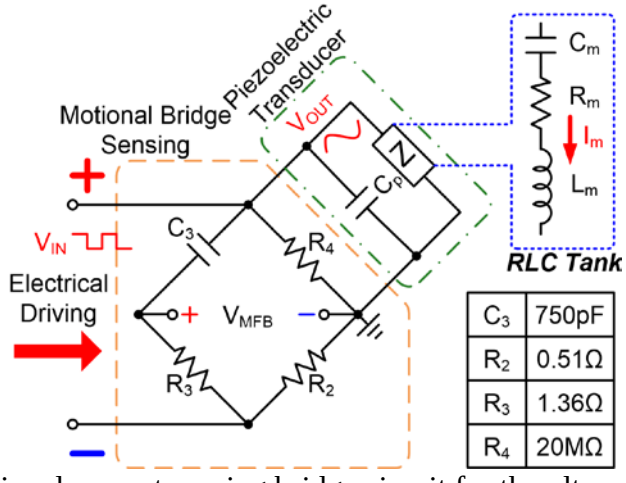


Figure 99. Motional current sensing bridge circuit for the ultrasonic oscillation.

Figure 97 shows two possible paths for the electrical output current to flow through the PT. However, only the right branch represents the mechanical motion, and the parallel capacitor C_p shunts some of the PT output current [128]. Thus, the PT needs an auxiliary circuit to extract that intrinsic information to build the resonance loop. A passive sensing bridge circuit, including C_3, R_3 and R_2 as show in Figure 99, is used to sense the motional current I_m [129]. Physically, I_m is equivalent to the tip velocity of the PT [104]. R_4 is a 20 MΩ resistor to provide a leakage path for the remnant DC voltage and protect the PT. R_4 can be neglected in the AC analysis due to its large value.

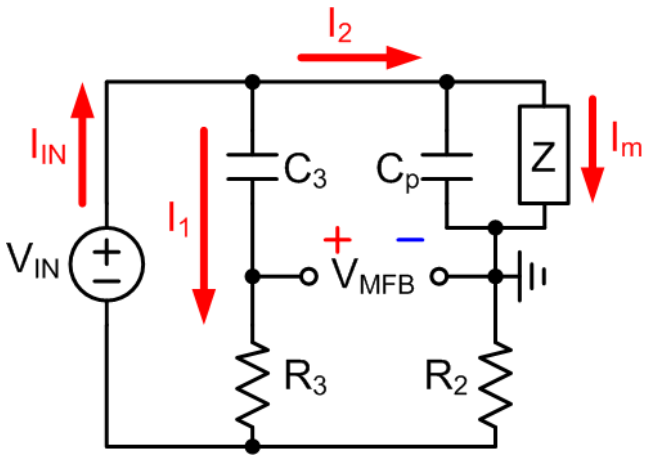


Figure 100. Simplified model of the motional current sensing bridge at resonance.

The principle of the sensing scheme can be obtained by a simplified model as shown in Figure 100 with the nodal analysis. Z represents the series impedance of components L_m, R_m and C_m in Figure 99 at resonance. The motional current I_m in the PT can be related to a motional feedback voltage V_{MFB},

$$V_{MFB} = I_1 R_3 - I_2 R_2 = \alpha(s) \cdot I_m \tag{53}$$

It can be noted that the resulting voltage V_{MFB} is proportional to I_m by an impedance factor of $\alpha(s)$, which can be expressed as,

$$\alpha(s) = \frac{\left[Z \cdot s\left(R_3C_3 - R_2C_p\right)\right] - R_2}{1 + sR_3C_3} \tag{54}$$

From (53), the motional sensing bridge circuit directly measures the motional current I_m. However, α is frequency dependent and a function of load Z. To correctly operate as a bridge network, the selections of components R_2, R_3 and C_3 need to take into account variations in Z, different loading conditions, and the parallel capacitor C_p over a wide range of frequencies. In order to make the sensing bridge load independent, as can be observed in the numerator of (54), R_3C_3 needs to match R_2C_p, completely cancelling the effect of the load Z on the sensing signal V_{MFB}. The resulting $\alpha(s) = -\frac{R_2}{1+sR_3C_3} \approx -R_2$ is valid for $\omega \ll \frac{1}{R_3C_3}$. This selection makes V_{MFB} more robust against variations of the load, ensuring good tracking over wide load transients.

5.2.2 Automatic Resonance Tracking Scheme

5.2.2.1 Architecture of the Proposed Scheme

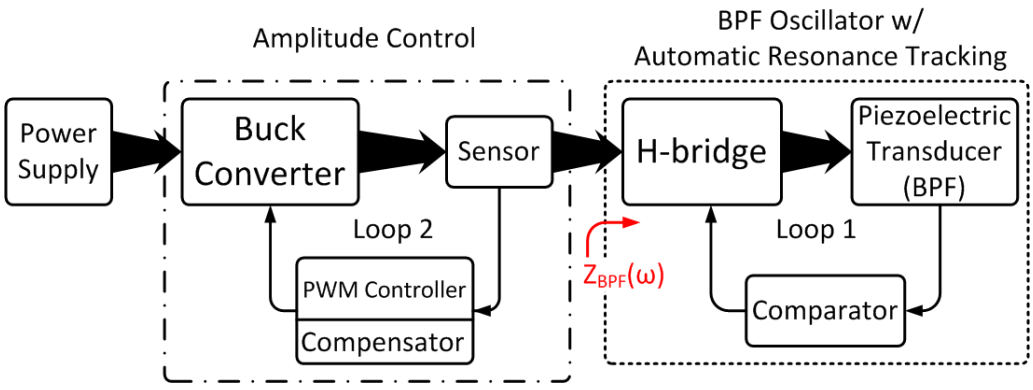


Figure 101. Dual loop automatic resonance tracking scheme with a BPF oscillator and power regulation.

The architecture of the proposed automatic resonance tracking scheme is demonstrated in Figure 101. It operates two loops for resonance tracking and amplitude control, respectively. Loop 1, including the PT, H-bridge driver, and comparator, acts as a BPF oscillator and automatically tracks the resonance frequency regardless of variations. Loop 2, including a power sensor, buck converter, and pulse-width modulation (PWM) controller, provides regulated output levels for different applications.

5.2.2.2 Automatic Resonance Tracking with the BPF Oscillator

For an energy efficient system, the PT needs to be driven in resonance by Loop 1. Based on (51), the PT has minimum reactance, and the power factor gets closer to unity by reducing the reactance at the resonant frequency. Thus, most electrical power is consumed as real power and maximally converted into mechanical motion. The required resonance can be constructed from a BPF oscillator. The Barkhausen criteria require the following conditions to ensure a stable oscillation in any closed-loop system [130].

$$|\beta \cdot A| = 1; \quad and \quad \angle\beta \cdot A = 2\pi n, n \in 0,1,2, \ldots \tag{55}$$

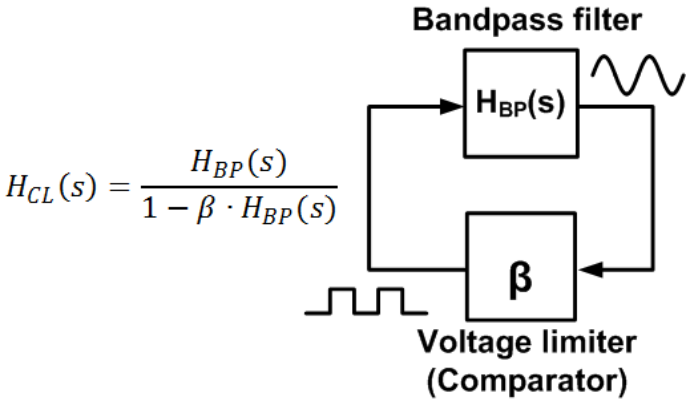


Figure 102. Conceptual block diagram of the BPF oscillator.

The Loop 1 tracking scheme shown in Figure 101 can be modeled as a band-pass filter in series with a voltage limiter, which applies the signal back to its input as shown in Figure 102, where A is the band-pass filter transfer function $H_{BP}(s)$ and β is the gain of the comparator. The comparator, also called a voltage limiter, controls the resonant amplitude with the H-bridge discussed in Section 5.2.2.3.

From (54), the motional current sensing bridge cancels the effect of C_p. Thus, in the vicinity of $\omega_{0,R}$, the PT behaves as a RLC band-pass filter with a transfer function given by,

$$H_{BP}(s) = \frac{V_{MFB}(s)}{V_{IN}(s)} = \frac{\alpha(\omega_{0,R}) \cdot I_m}{V_{IN}(s)} = \frac{K_1 \cdot s}{s^2 + \frac{\omega_{0,R}}{Q} s + \omega_{0,R}^2} \tag{56}$$

where $K_1 = \alpha(\omega_{0,R}) K_{BR}/L_m$, $\alpha(\omega_{0,R})$ is $\alpha(s)$ value at resonance and approximately equals $-R_2$ as shown in Figure 100 and (54). $K_{BR} = -1$ is the phase inversion of H-bridge in Figure 101. Although $V_{MFB}(s)$ and $V_{IN}(s)$ are frequency dependent in (56), we use V_{MFB} and V_{IN} elsewhere for simplicity. Due to the correct sensing of the motional bridge as (53) and (54), the PT's quality factor, $Q = \sqrt{L_m/C_m}/R_m$, is introduced as the quality factor of the BPF and lies between 72~718 under various loading conditions. The intrinsic high Q of the PT guarantees the accuracy of the automatic frequency tracking as,

$$Q \approx \omega_{0,R}/\omega_{0,\Delta} \tag{57}$$

where $\omega_{0,\Delta}$ represents the half-power bandwidth. Therefore, for the 55.4 kHz longitudinal mode, the resonant frequency should vary between 55.1 kHz to 55.8 kHz under worst-case loading. The closed-loop transfer function $H_{CL}(s)$ can be derived as,

$$H_{CL}(s) = \frac{H_{BP}(s)}{1 - LG(s)} = \frac{H_{BP}(s)}{1 - \beta \cdot H_{BP}(s)} \tag{58}$$

where LG(s) is the loop gain. Thus, the intrinsic BPF of the PT can be applied to the oscillator, and does not need an independent BPF or other filters. Besides saving hardware resources, the intrinsic BPF also has an automatic resonance tracking feature. Under practical applications, the PT suffers from environmental variations such as load or temperature changes, which can induce a shift of resonance frequency. From (56), the oscillating center frequency locates exactly at the natural frequency of the PT in (52), which guarantees that the proposed oscillator automatically tracks the resonance of the PT. Additionally, its stability feature is as simple as that of an ordinary 2nd-order system and analyzed as follows: At the center frequency of the band-pass filter, the magnitude of the loop gain needs to satisfy the Barkhausen criteria (55) (e.g., |LG| = 1), to make the magnitude of (58) large enough to ensure oscillations. Therefore, the denominator of $H_{CL}(s)$ needs to be zero, which will yield the following equation:

$$s^2 - s\left(\beta \cdot K_1 - \frac{\omega_{0,series}}{Q}\right) + \omega_{0,series}^2 = 0 \tag{59}$$

From this equation, the voltage limiter requires a minimum gain β to ensure oscillation at the resonant frequency (e.g., $s=j\omega_{0,R}$),

$$\beta > \frac{\omega_{0,R}}{K_1 \cdot Q} \quad \rightarrow \quad \beta > \frac{R_m}{R_2} \tag{60}$$

Furthermore, the unwanted transverse resonance mode is prevented by the phase part of the Barkhausen criteria as (55). Referring to the characteristics of PT, the longitudinal mode differs from the mode by 180° phase shift [105]. Therefore, the polarity

configuration for longitudinal resonance in this work will naturally reject the other mode.

5.2.2.3 Amplitude Control

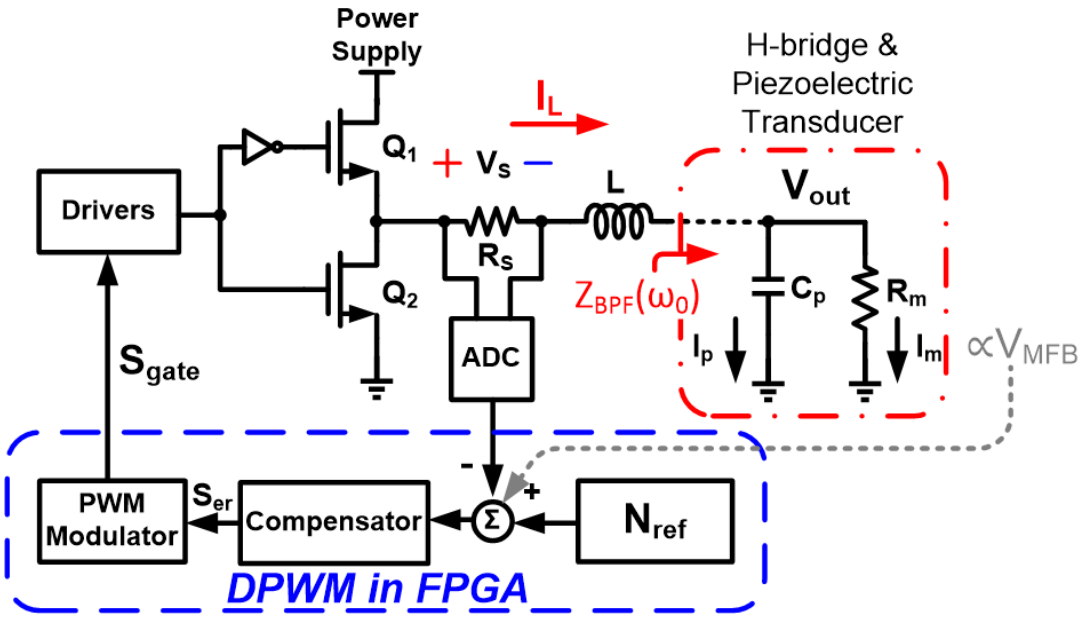


Figure 103. Block diagram of the amplitude control loop in resonance.

Amplitude control is achieved in Loop 2 as shown in Figure 101. It utilizes a PWM scheme to regulate output power and stabilize the system under various loading conditions. The block diagram of the amplitude controller is shown in Figure 103. The feedback variable, amplitude of the output current I_L, contains both the motional current I_m and the shunt capacitance current I_p. It is extracted in a current sensor and converted into digital-domain by an analog-to-digital converter (ADC). The input of the amplitude controller is the difference between a digital reference number, N_{ref}, and the quantized I_L. Its output is connected to a digital PWM (DPWM) modulator, which controls the high-side and low-side switches of a buck converter. Loop 2 acts as a simple second-order

system and can be easily compensated. The detailed implementation is discussed in Section 5.2.3.3.

As a comparison, another extracting point from V_{MFB} is shown in Figure 103. Although such a sensing scheme directly detects I_m and regulates the mechanical power more accurately, it has startup and reliability problem. During startup period, the PT is not in resonance and has little energy. As a result, the motional bridge does not sense V_{MFB} correctly, and Loop 2 is operated in open-loop and may be saturated. Therefore, we utilize the former feedback scheme with I_L.

In conventional DPWM, N_{ref} is defined as,

$$N_{ref} = I_{L,ref} \times G_{ADC}(0) \times \frac{2^{ADC\ bits} - 1}{ADC\ Sensing\ Range} \tag{61}$$

where $G_{ADC}(0)$ is the DC sensing gain of the ADC and is analyzed in Section 5.2.3.3, and $I_{L,ref}$ is the regulated reference of I_L. However, the relationship between $I_{L,ref}$ (or N_{ref}) and achieved functions (sealing and dissecting) is a complicated and multidisciplinary problem, which suffers hardware variation and involves biology, mechanics, and electronics. Therefore, to mimic the practical surgeries, after building up the system, we directly swept the N_{ref} value by programming different numbers in the FPGA, tested the tip upon tissues and characterized proper N_{ref} values versus achieved functions as demonstrated in Section 5.2.4.

5.2.3 Ultrasonic VSD System Implementation

The proposed scheme shown in Figure 101 can be implemented by using two parts designed for the ultrasonic vessel sealing and dissecting system: 1) the BPF

oscillator and 2) the amplitude controller. They are detailed and the stability of the UVSD system is analyzed as follows.

5.2.3.1 BPF Oscillator Implementation

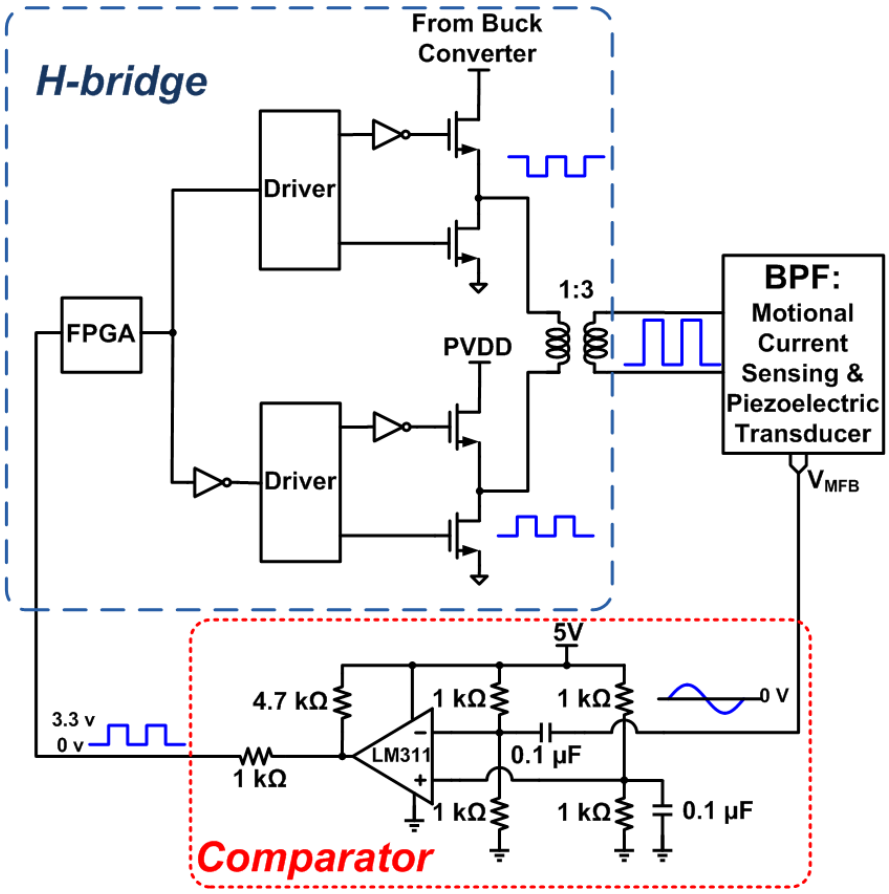


Figure 104. Implementation of the BPF based oscillator.

The complete BPF based oscillator system is shown in Figure 104. A comparator with a high open-loop gain is typically used to provide β. For the motional current in the desired system, the β factor needs to be higher than R_m/R_2 in (60), which is around 980 V/V in the worst case, to ensure oscillations. This requirement is easily achieved in most comparators.

To minimize the signal delay, V_{MFB} is directly detected by the comparator. The input of the comparator is AC coupled and uses a single 5 V supply. Its output is feedback to the FPGA, which drives the H-bridge switches. A 1 kΩ resistor is added at the output of the comparator to limit the current flowing into the FPGA.

5.2.3.2 Amplitude Control Circuits

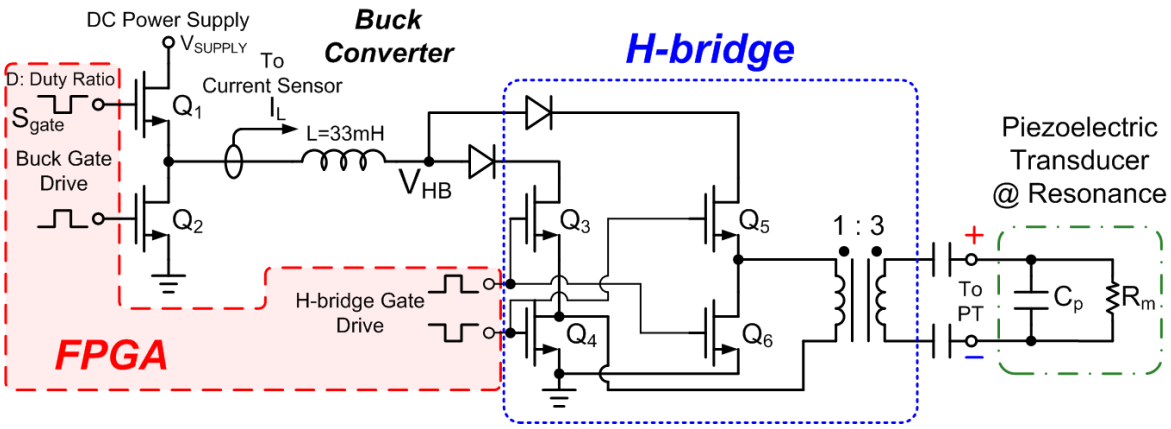


Figure 105. Detailed structure of the buck converter and H-bridge.

The amplitude of the mechanical motion is controlled by a buck converter ahead of the BPF oscillator as shown in Figure 105. The switches Q_1 and Q_2 operate as a buck converter stage, and the switches Q_3, Q_4, Q_5, and Q_6 operate as an H-bridge inverter. The output voltage of the buck converter is controlled by the duty ratio of the driven signal, S_{gate}, at Q_1 and Q_2 gates. It also modulates the signal swing of the H-bridge. A 1:3 step-up transformer is used to boost three times the output voltage of the H-bridge applied to the PT. After the transformer, two capacitors couple the output AC signal to the PT.

Since the H-bridge and the PT in Figure 105 are operated with a fixed 50% duty ratio gate signal switching at the resonant frequency, the entire BPF oscillator could be modeled as a resistive load R_m in parallel to the output capacitance C_p by a first-order approximation.

The buck converter drives the H-bridge and PT in resonance, and forces the average I_L to be almost constant [125]. The resulting LC_p filter splits its two complex poles and can be approximated as a first-order system H(s),

$$H(s) = \frac{D \times V_{SUPPLY}}{I_L} = \frac{1}{L} \frac{s + \frac{1}{R_m C_p}}{s^2 + \frac{1}{R_m C_p} s + \frac{1}{LC_p}} \approx \frac{1}{L} \frac{1}{s + \frac{R_m}{L}} \tag{62}$$

where D represents the duty ratio of S_{gate} in Figure 105. The dominant pole is $\omega_p = R_m/L$. Therefore, the compensation requirement of the buck converter is significantly relaxed.

5.2.3.3 Stability of the UVSD with the PI Compensator

Referring to Figure 101 and Figure 103, we note that the overall loop gain transfer function for the amplitude controller is given by,

$$LG_c(s) = H(s) \cdot G(s) \cdot G_{ADC}(s) \cdot M \tag{63}$$

where G(s) is the transfer function of the compensator, $G_{ADC}(s)$ is the transfer function of the sensing path, and M is the gain of the PWM modulation. M can be approximated as [54],

$$M = \frac{V_{SUPPLY}}{V_{ramp}} \tag{64}$$

V_{ramp} is the amplitude of the ramp signal used in PWM and is set as 1.1 V to cover the dynamic range of compensated error signal S_{er} in Figure 103. In the FPGA, V_{ramp} is a part of the DPWM, and is generated and implemented by a programmable counter [131], which is 18-bit in this design, to directly generate S_{gate}.

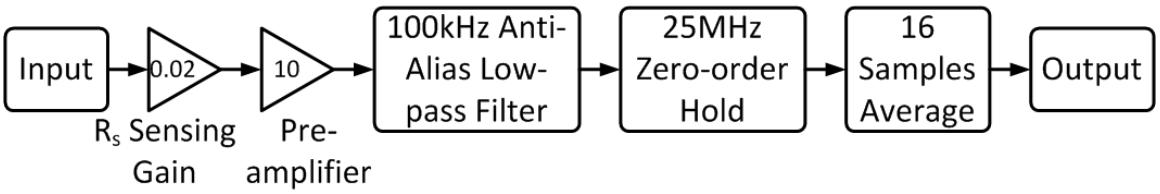


Figure 106. Block diagram of the inductor current sensing scheme.

I_L, as shown in Figure 103, is measured with a sensing resistor and a 14-bit ADC. The detailed sensing path is modeled in Figure 106. The sensing resistor of 0.02 Ω is modeled as a constant sensing gain $V_s/I_L = R_s$. The ADC has a preamplifier with a gain of 10. A second-order low-pass filter with a cutoff frequency of 100 kHz is utilized in the model. To include the effects of the ADC, a zero-order sample and hold (ZOH) is included with the 25 MHz sampling frequency. Moreover, the resulting feedback signal is processed through a periodic moving average filter with 16 samples to reduce the glitches or noise in the I_L sampling. Thus, the overall gain of the sensing scheme can be expressed as,

$$G_{ADC}(s) = 0.2 \times \frac{(2\pi \times 100k)^2}{s^2 + \frac{2\pi \times 100k}{0.7} s + (2\pi \times 100k)^2} \tag{65}$$

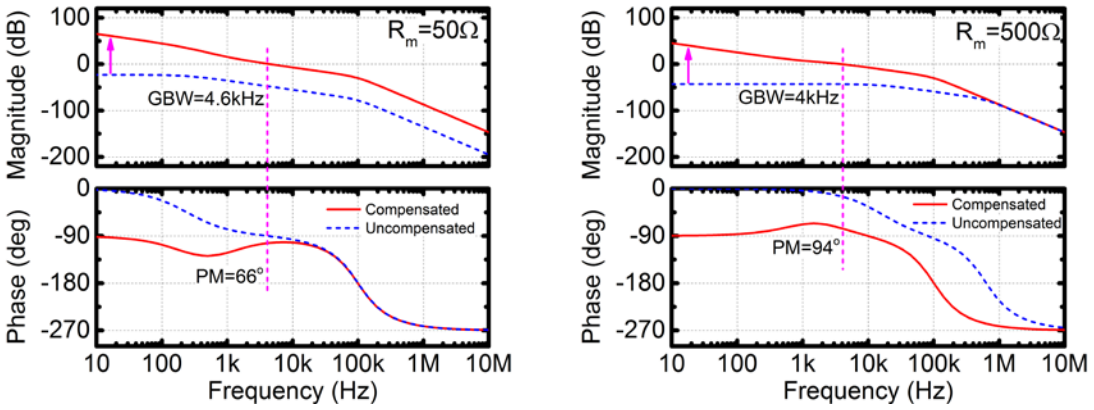
The two poles of the current sensing ADC anti-alias filter are assumed at high frequency, so as not to affect the stability. To avoid the switching frequency sampling deviation, the

chosen switching frequency F_s is 100 kHz. The desired BW of the closed-loop scheme is less than $F_s/20$ [54].

According to (63), $LG_c(s)$ has two dimensions needing compensation: 1) $\omega_p = R_m/L$ is not fixed since R_m typically changes from 50~500 Ω for various surgical jobs, varying the bandwidth (BW) of the system by one decade. 2) The uncompensated DC gain of $H(s) \cdot G_{ADC}(s) \cdot M = 1/R_m \cdot 0.2 \cdot 18$ is too low to achieve accurate amplitude regulation. Therefore, the compensator needs to boost the DC gain. This boost will also extend and fix the BW against R_m variation. A proportional-integral (PI) compensation is added to the DPWM in the FPGA depicted in Figure 103 as,

$$G(s) = K_p + \frac{K_i}{s} \tag{66}$$

where $K_p = 64$ is the proportional gain, and $K_i = 1.6\times106$ is the integral gain.



(a) (b)

Figure 107. Bode plot for the compensated and uncompensated loop gain of the proposed scheme with compensation for (a) minimum R_m = 50 Ω, and (b) maximum R_m = 500 Ω load.

The Bode plot for the loop gain of the scheme is shown in Figure 107 for two cases: 1) Minimum R_m = 50 Ω load and 2) Maximum R_m = 500 Ω load. At low frequency, the compensator provides high gain to $LG_c(s)$ and ensures accurate regulation. At high frequency, although Rm changes the location of ω_p, the compensator extends the bandwidth above 4 kHz and fixes it with $\omega_z = K_i/K_p$ in (66).

5.2.4 Experimental Results

5.2.4.1 Power Regulation with Various References

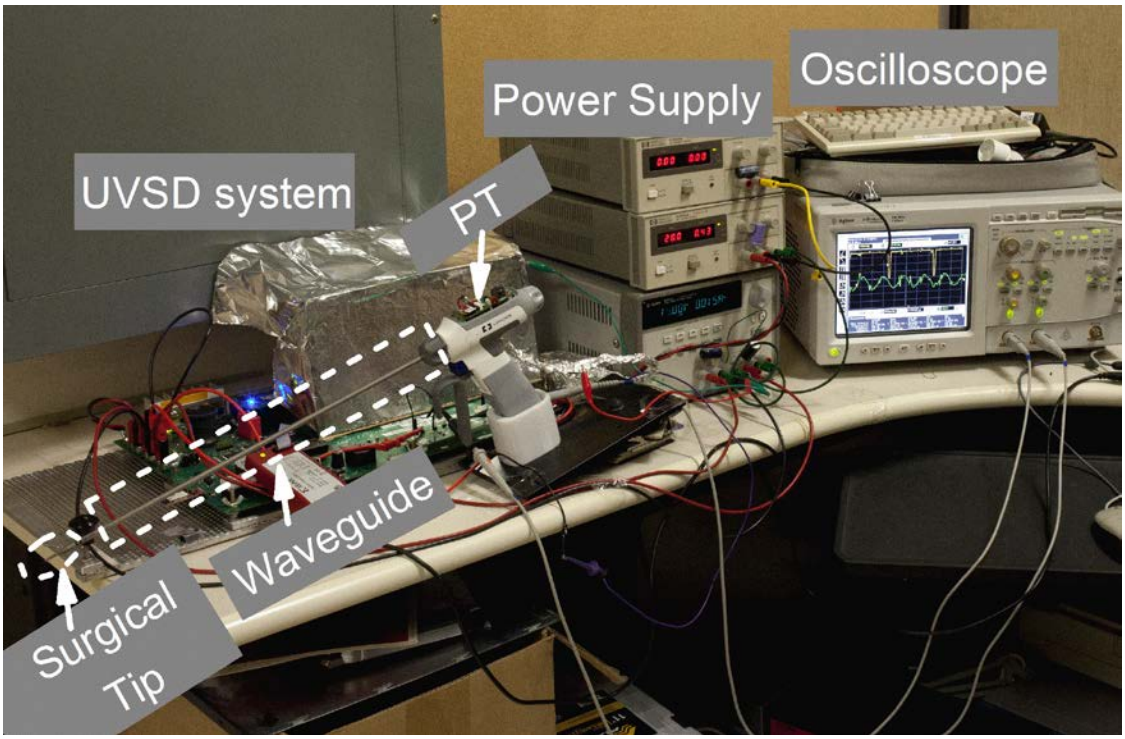


Figure 108. Measurement setup for the UVSD system.

The measurement setup of the proposed UVSD system is shown in Figure 108. The power regulation capability with various N_{ref} is tested first as shown in Figure 109. The aforementioned discussion and analysis demonstrate the linear relationship between

input current and output mechanical power under resonance. By tuning the digital reference number N_{ref} of the DPWM in Figure 103, users can change the input current I_{in} of the entire system, ultimately regulating the output mechanical power of the PT. The input voltage was selected as 20 V from a DC power supply. The PT consumes current from 0.26 A to 0.68 A with N_{ref} from 1800 to 2300 linearly. Further increasing N_{ref}, the DPWM will suffer a limited dynamic range and saturation due to the limited voltage of the DC power supply.

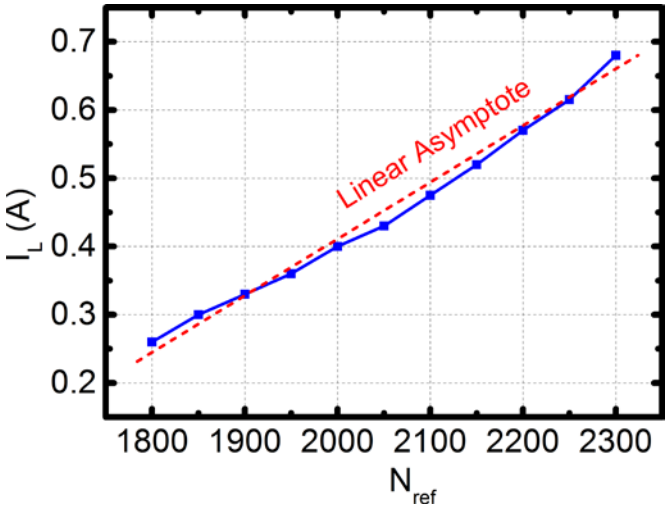


Figure 109. Unloaded input current I_{in} vs. reference values N_{ref} of DPWM.

5.2.4.2 Experimental Results in Glycerin

Transient behavior is also crucial to the performance of a UVSD system. During real application, the surgical tip frequently contacts different tissues, which requires a fast settling time to avoid thermal spread in the surrounding tissues. Additionally, the transient behavior also indicates system stability under various loading conditions. Because pure glycerin is commonly used to mimic blood and tissues, the load settling

time is measured by changing the mechanical load. The surgical tip is quickly plugged into glycerin and captures V_{MFB} with a single trigger in the oscilloscope. The step response of V_{MFB} is demonstrated in Figure 110. In the zoomed-in plot, the PT resonates with a 55.4 kHz sinusoidal wave. It takes 10 ms to converge to a higher value, which is longer than the compensated Loop 2 in Section 5.2.3.3. This is because the PT is non-ideal. Parasitics will affect the buildup of the amplitude, taking additional time to settle the transient response.

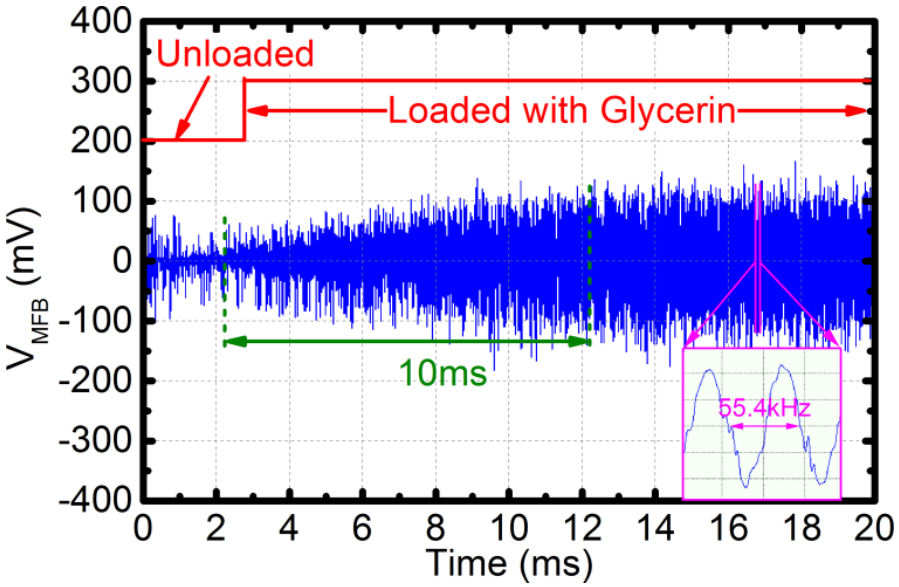


Figure 110. Step settling time of the V_{MFB} signal.

The UVSD system was also tested in the unloaded and loaded conditions at different output power levels. The measured V_{MFB} and duty ratio D are shown in Figure 111. To emulate the viscous blood environment, the surgical tip was merged into pure glycerin liquid under different N_{ref}. Compared with the unloaded condition in Figure

111(a) and (c), the motional current, indicated by V_{MFB}, dipped in glycerin was reduced by 23% in steady-state as shown in Figure 111(b) and (d), respectively.

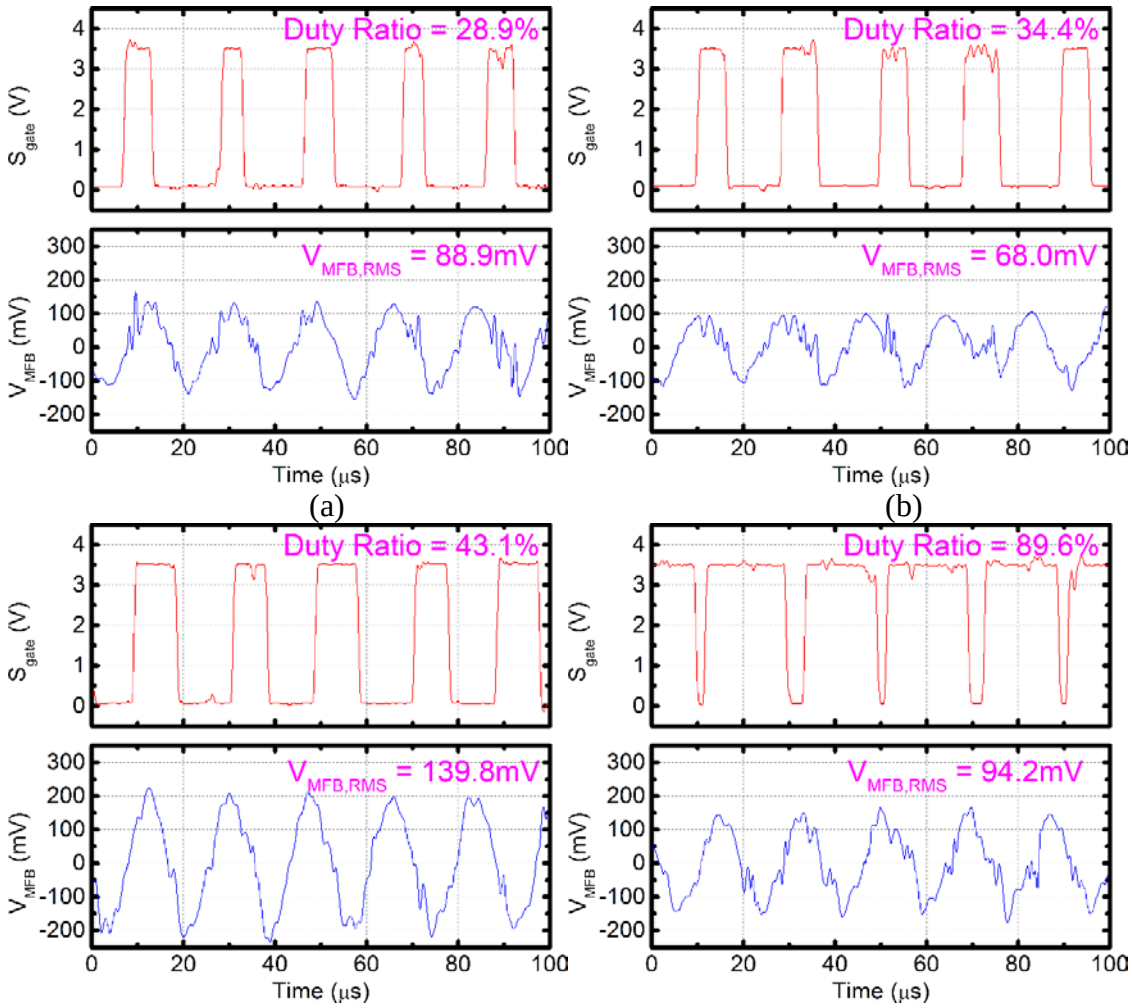


Figure 111. Measured waveforms for four cases: (a) unloaded operation with N_{ref} = 1800, (b) glycerin-loaded operation with N_{ref} = 1800, (c) unloaded operation with N_{ref} = 2100, and (d) glycerin-loaded operation with N_{ref} = 2100.

The variations observed between the unloaded and loaded cases are analyzed as follows: We monitored the desired mechanical current indirectly by using the inductor current I_L. It has two components: 1) the shunt current I_p flowing through C_p, and 2) the

desired mechanical current I_m, as shown in Figure 103. During the loaded condition, as R_m increases, I_m tends to decrease. Since the buck converter regulates I_L, the amplitude of V_{out} will be increased to keep I_L constant and indirectly increase $I_p = \frac{V_{out}}{\omega_0 C_p}$. Since $I_m = I_L - I_p$, the regulated I_L and increased I_p will force I_m to decrease, introducing a small error. This is a consequence of choosing I_L as the feedback signal, as explained in Section 5.2.2.3. Moreover, the observed higher frequency ripples shown in Figure 111 come from the harmonics of the longitudinal resonance and the waveguide non-idealities. Due to their smaller amplitude, the harmonics do not affect the fundamental resonant frequency for this application.

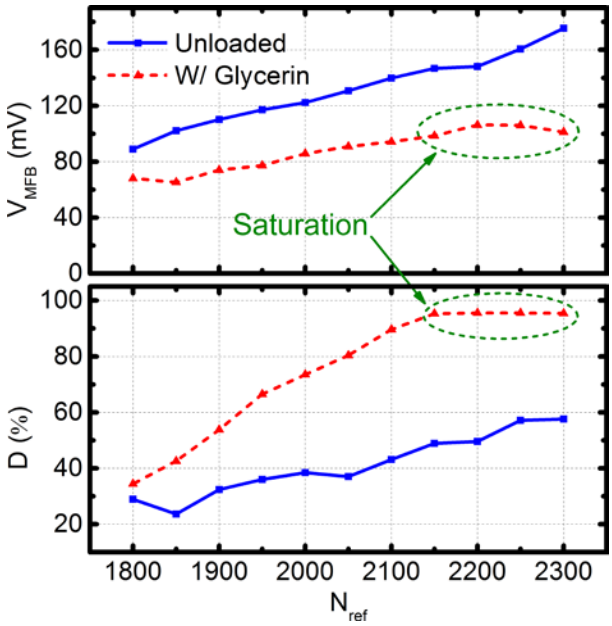


Figure 112. Sensed motional magnitude V_{MFB} and duty ratio D vs. different control references N_{ref} of the power regulator.

Detailed V_{MFB} and duty ratio results are shown in Figure 112. When a large mechanical load is applied to the surgical tip, the duty ratio should increase. However,

there is a limit to the amount of power that the system can deliver for large mechanical loads, which induces a low quality factor Q of the PT. If the mechanical load is very large, the system will saturate as shown in Figure 112.

5.2.4.3 Accuracy of the Automatic Resonance Tracking

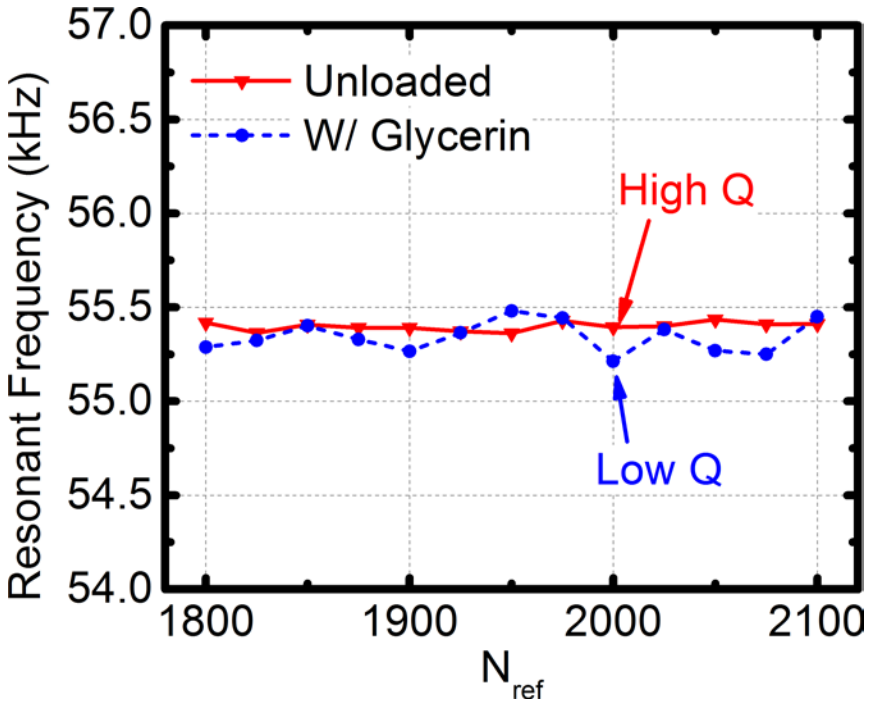
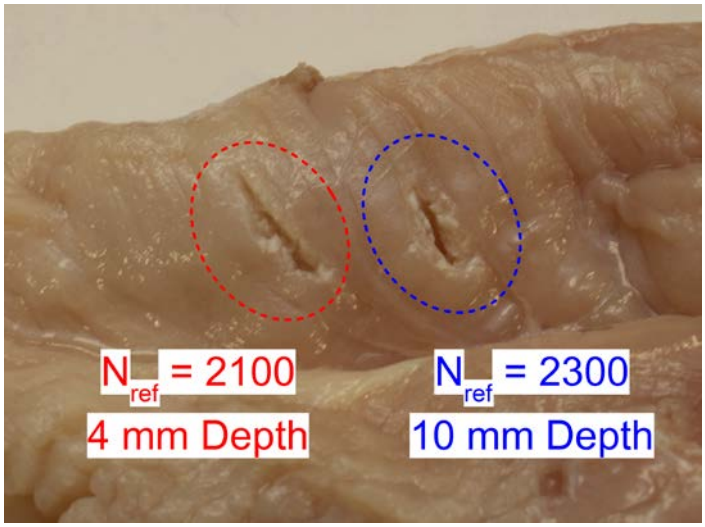


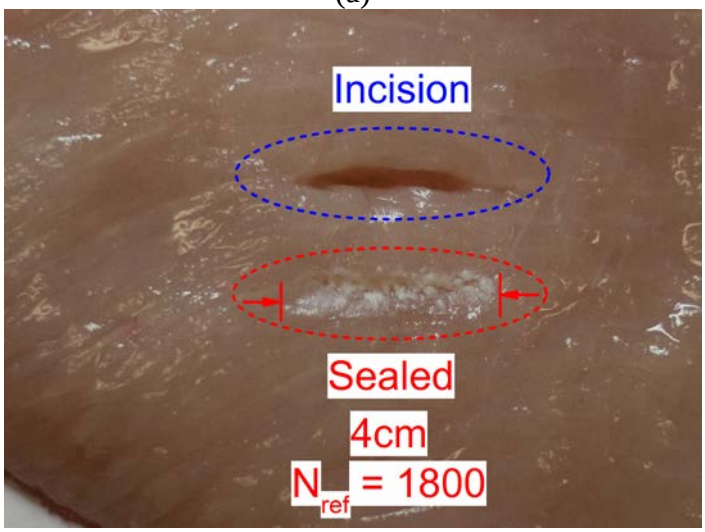
Figure 113. Automatic tracked resonant frequencies vs. reference values N_{ref} of DPWM.

The oscillating frequencies with various N_{ref} are plotted in Figure 113 to verify the accuracy of the proposed automatic resonance tracking. For an unloaded condition, the tracked frequency variation is smaller than 80 Hz. For a glycerin loading condition, the variation range is smaller than to 250 Hz. This is because the motional bridge accurately senses the PT as a BPF. The PT's high Q is introduced as the quality factor of the BPF oscillator-based system and guarantees the excellent tracking accuracy.

5.2.4.4 Experimental Results in Chicken Tissue



(a)



(b)

Figure 114. Tested samples: (a) different dissecting power and resulting depths with N_{ref} = 2100 and 2300, and (b) a sealing function setting N_{ref} = 1800.

To test the UVSD capabilities of the designed system, a piece of chicken breast tissue was cut as shown in Figure 114(a). The high power tends to vaporize the tissue at a uniform rate of speed, resulting in a clean dissection. When N_{ref} = 2100, the cutting

depth is 4 mm. With a higher N_{ref} such as 2300, the increased mechanical power gives a deeper cutting at 10 mm. The sealing function was measured with low N_{ref}. The low mechanical power provided a gentle heat procedure and sealed the tissue. Figure 114(b) shows a 4 cm incision sealed by setting N_{ref} at 1800.

5.3 Integrated Version: IC Implementation

5.3.1 Sliding-mode Power Management Architecture

Piezoelectric transducer (PT) is an emerging energy-based technology for electrosurgery. With proper driving signals, the PT is utilized as a mechanical actuator. It converts electrical signal into physical displacements for various electrosurgical functions, such as ultrasonic vessel sealing and dissecting (UVSD) [132]. The main design challenge is to precisely regulate and quickly build up a mechanical power when changing between various load requirements. The pulse-width modulation (PWM) mainly bases its design on the small signal model; thus, PWM does not often fit for the large signal transient satisfactorily. This problem becomes even worse with changing load impedance due to pressure upon the surgical tip. The self-oscillating hysteretic controller (SOHC) has simple structure, reliable and fast performance for nonlinear large signal applications [133]. However, it cannot be simply applied since the proposed UVSD system has significant differences from generic DC-DC converters.

A PT has multiple resonant vibration modes and renders the highest mechanical power generation exclusively at these resonant frequencies, which are shifted by load conditions. In worst conditions, a heavy loaded PT may shift the vibrating frequency into

an unwanted resonant mode and cause a malfunction. Therefore, another challenge is to track and lock the PT into the desired resonant frequency for maximum power conversion. There are multiple methods to drive the PT into resonance, but these methods have poor tracking capability: the power factor correction (PFC)-based method [115] requires additional reactive components and complicated compensation. The PLL-based system has a limited lock-in range and requires a complex compensation to stabilize for large signal load variations and power mode changing [109]. All reported approaches were fabricated with bulky discrete components, increasing the size and cost of the solution.

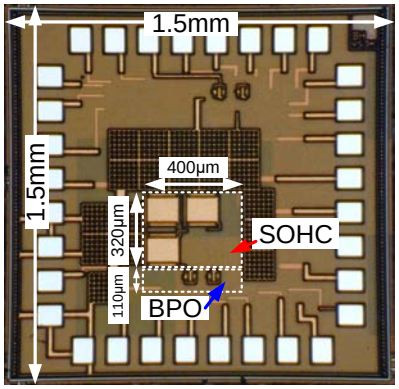


Figure 115. Die micrograph with 0.18-µm CMOS technology.

In this work, a monolithic controller for a UVSD system is introduced for the first time, which features compact size, automatic resonance tracking, high power conversion efficiency, and a fast response for electrosurgical operation. For power regulation, a current-fed DC-AC converter with a frequency compensated SOHC guarantees a fast response for large output power changing. For power generation, the PT is driven by a band-pass filter-based oscillator (BPO), which relies on the intrinsic

reactance of the PT and self-tracks the targeted resonant frequency. Thus, the unwanted modes are excluded and the maximum mechanical power is achieved.

5.3.2 Monolithic Integration and Measurement Results

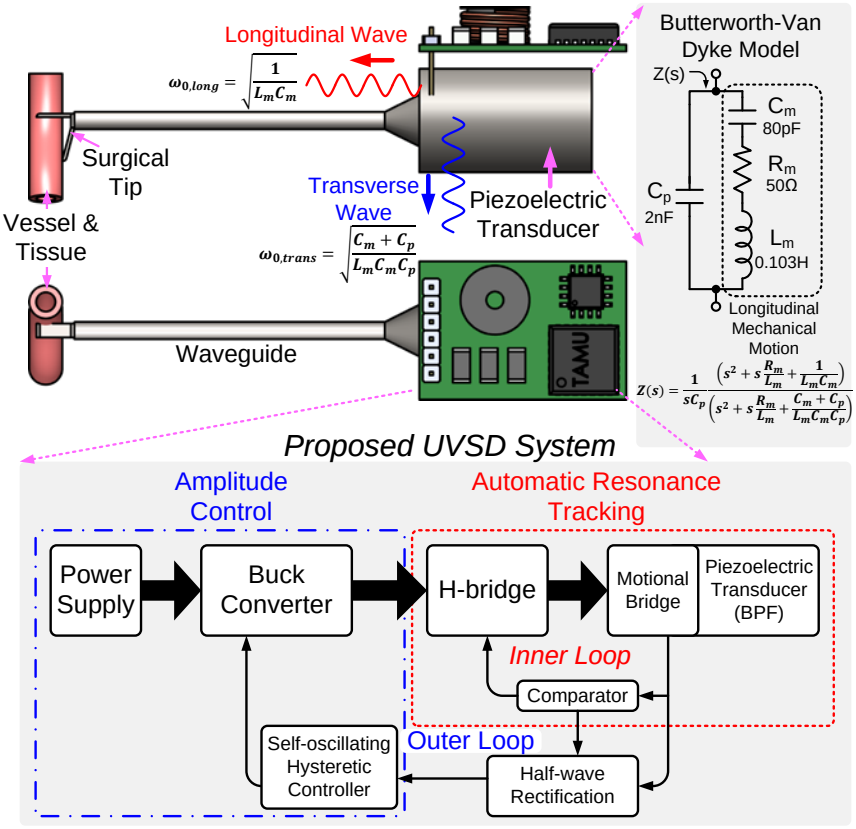


Figure 116. Conceptual architecture of the UVSD system.

Figure 116 shows the architecture of the UVSD system. The PT has both longitudinal and transverse resonant modes. In the vicinity of these resonant frequencies, the PT could be modeled by the Butterworth-Van Dyke (BVD) model. The PT is designed in such a position that only the longitudinal resonance $\omega_{0,long}$ = 55.5 kHz is transmitted by a metal waveguide to the surgical tip, which executes the sealing and dissecting operations. The $R_mL_mC_m$ branch represents the loss, compliance, and mass of

the longitudinal resonance. On the other hand, the transverse resonance $\omega_{0,trans}$ is unwanted and simply wastes energy inside the PT, which is represented by the C_p branch. The control block diagram is illustrated at the bottom of Figure 116. There are two nested loops: the inner loop is a BPO. It utilizes the PT's intrinsic nature as the band-pass filter, automatically tracks the longitudinal resonance, and rejects the transverse resonance against load variation. The outer loop is a SOHC that achieves high regulation accuracy for the steady-state and a fast response for large load transition.

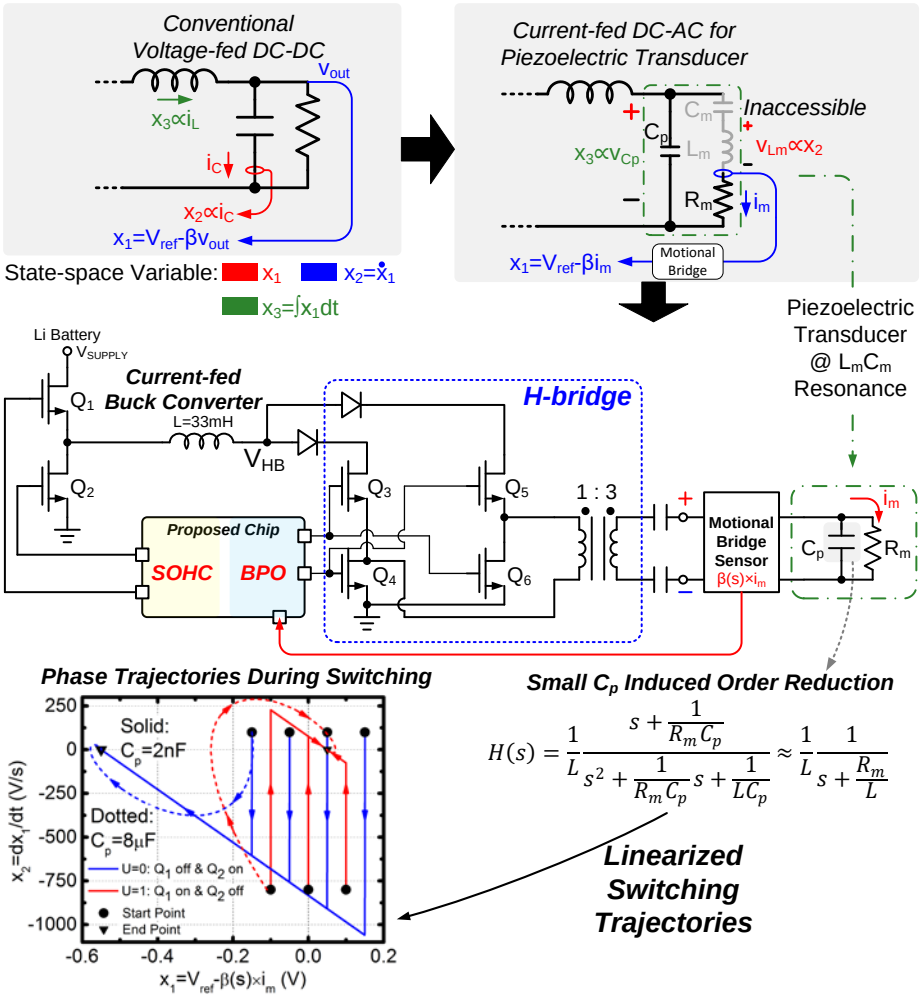


Figure 117. Power stage of the UVSD system.

Figure 117 illustrates the conventional SOHC for voltage-fed DC-DC converters with three possible feedback variables: x_1, its derivative x_2, and integral x_3. The UVSD system focuses on the output motional current $x_1=i_m$ that can be sensed by the motional bridge [129]. Its integral x_3 is the output voltage of the PT, which has a peak value over 200 V and is difficult to be sensed. Its derivative x_2 is the equivalent inductor voltage of the PT but inaccessible. The proposed system is shown in Figure 117. The outer loop consists of a current-fed DC-AC converter. The inner loop includes an H-bridge to convert the DC current from the buck converter into an AC. The BPO tracks the PT's longitudinal resonance; thus, the PT is modeled as parallel R_m and C_p. Due to the C_p's small value, the second-order DC-AC converter is approximated to a first-order. Its phase trajectories are linearized from the generic spiral shape. Compared with large C_p = 8 μF, this C_p = 2 nF PT shows simpler responses under different start points, which are crucial to the large signal operation.

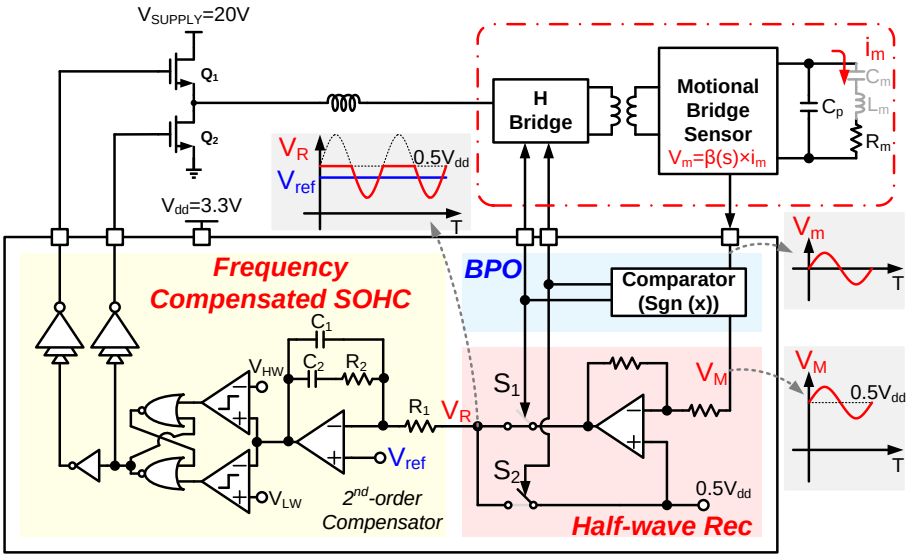


Figure 118. The SOHC with direct half-wave rectification input.

Figure 118 details the schematic of the frequency compensated SOHC. A type-II compensator is developed to improve the SOHC performance in three aspects: a pole at the origin integrates and removes the steady state error [134]. A zero $z = 1/R_2C_2$ relieves the phase delay in the middle frequency. At high frequency, another pole $p_2 = \frac{1}{R_2C_2}\left(1+\frac{C_2}{C_1}\right)$ determines the bandwidth as 74 kHz. For the sole feedback variable, i_m is sensed as V_m and regulated as an RMS value with respect to V_{ref}. However, the conventional RMS detector has a phase delay from integration and slows down the control speed. Instead, a fast half-wave rectifier is developed to generate a semi-AC signal V_R. It reuses V_M from the comparator of the inner loop. The high-order harmonics of the resonant frequency are directly filtered out by the bandwidth of the compensator.

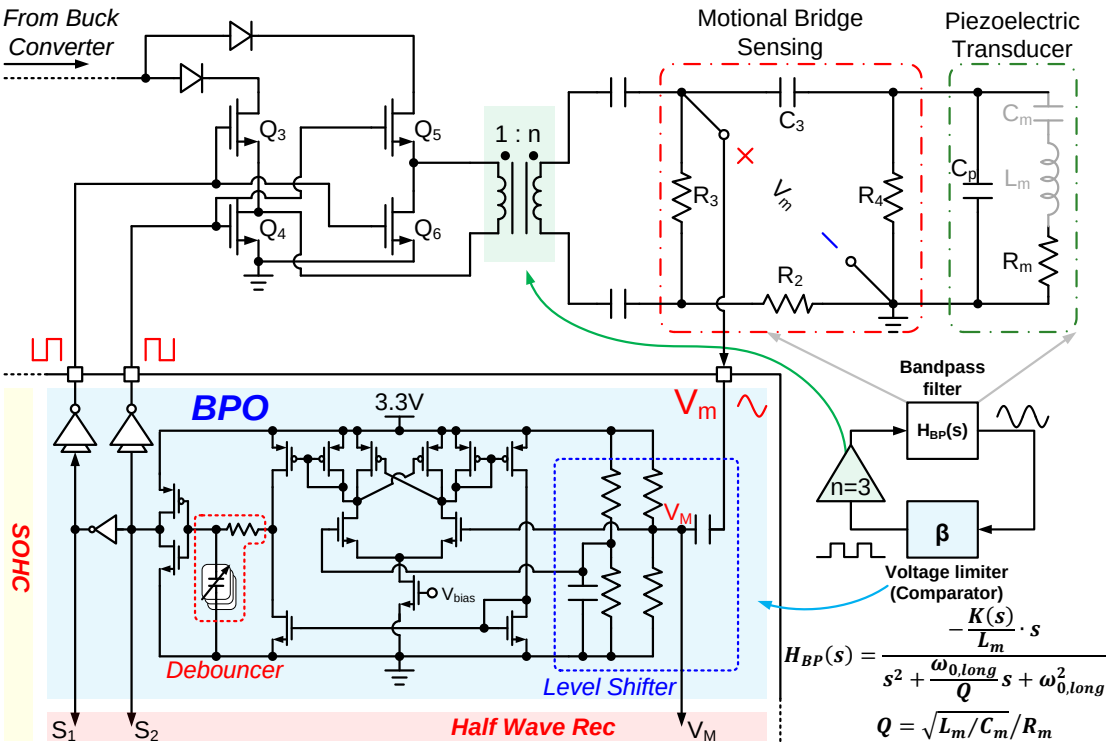


Figure 119. The BPO with a debouncer for automatic resonant tracking.

Figure 119 illustrates the detailed schematic of the BPO inner loop. A motional bridge is inserted before the PT to extract its motional current i_m as $V = \beta(s) i_m$, where $\beta(s) = \frac{[Z \cdot s(R_3 C_3 - R_2 C_p)] - R_2}{1 + s R_3 C_3} \approx 0.5$ for a wide frequency range [132]. As a result, C_p is neglected in the inner loop and the BVD model is simplified to a series $R_m L_m C_m$. Putting the bridge and PT as the band-pass filter of the BPO, its oscillating frequency is exactly the resonant frequency of the PT and guarantees self-tracking. Moreover, the reactance of L_m and C_m cancels each other at resonant frequencies, implying maximum electrical power converted into the mechanical motion modeled by R_m. The comparator has two stages and positive feedback to enhance the gain. At its input, a level shifter matches the AC signal V_m and elevates it to $V_M = 0.5V_{dd} + V_m$. Due to the high switching voltage of the H-bridge, the strong electromagnetic (EM) noise will affect the positive feedback loop and cause chattering. Thus, a RC debouncer is placed at the output. Its bandwidth is three times that of the 55.5 kHz resonant frequency and only filters the zero-crossing chattering.

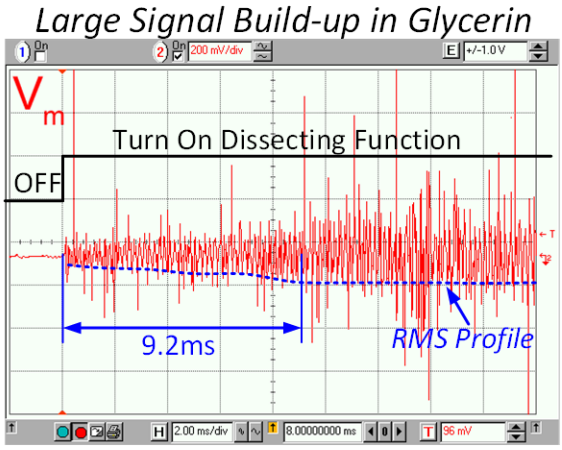


Figure 120. The resonance tracking, large signal build-up.

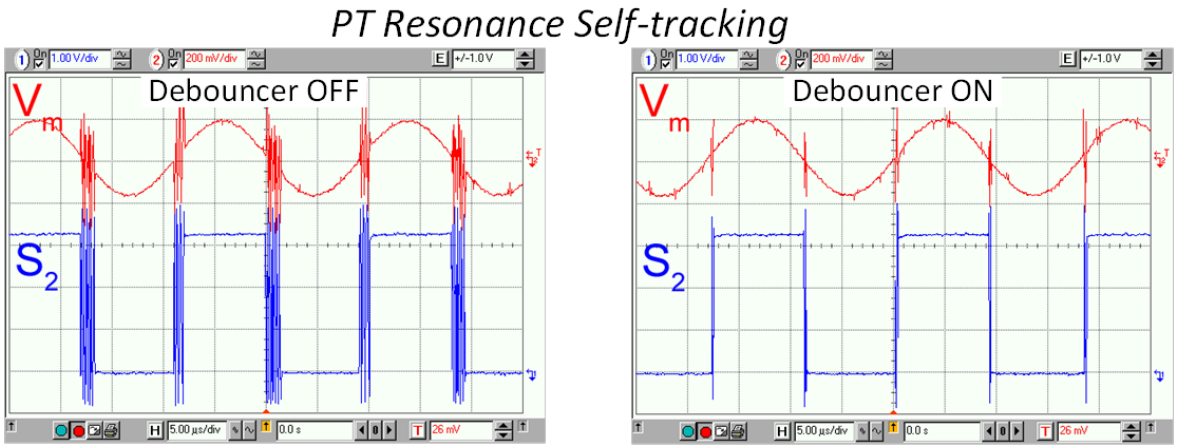


Figure 121. Performance of the debouncer.

Table 13. Performance comparison of this integrated version.

	Medtronic Sonicision™	Ethicon ACE+7™	[132]	This Work
Resonant Tracking Technology	PLL	PFC	BPO	BPO
Regulation	PWM	PWM	PWM	SOHC
Controller Form	Discrete Components	Discrete Components	Discrete Components	Monolithic 0.18-μm ASIC
System Outline	Cordless	Corded	Cordless	Cordless
System Size	Median	Bulky	Median	Small
Mean Dissection Speed (mm/sec)	5.75 @ MAX 90 W	4.52 @ MAX 90 W	3.2 @ MAX 20 W	4.8 @ MAX 17.5 W
Mean Seal Time on 5mm vessels (sec)	7.2	6.8	6.5	6.1
Large Signal Build-up Time	Slow >18ms	N/A	Fast 10ms	Fast 9.2ms

Figure 120 shows the automatic resonance tracking of the BPO. The unloaded operating frequency is self-locked at 55.5 kHz. The loaded frequency deviation is smaller than 220 Hz due to the PT's intrinsic high Q. The debouncer effectively filters the EM noise as illustrated in Figure 121. The large signal build-up transient is characterized by suddenly powering up the UVSD system. The surgical tip is dipped in glycerin that mimics blood and tissues. The measured build-up time is as short as 9.2 ms that is a great improvement over other PT-driven technologies.

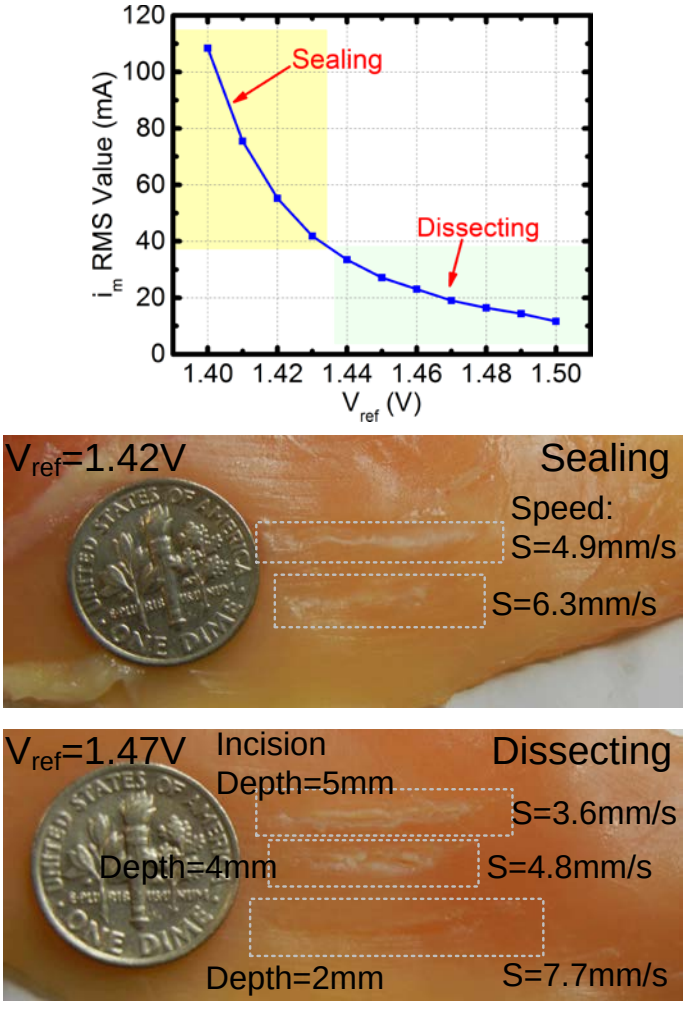


Figure 122. Sealing and dissecting in vitro testing.

Figure 122 illustrates the UVSD system in vitro testing. With high output power as V_{ref} = 1.42 V, the tissue is vaporized and the incision is sealed. With relatively low output power as V_{ref} = 1.47 V, the generated mechanical power gives a gentle heat procedure and effectively dissects the tissue. The faster dissecting speed, the less burned tissue and a shallower cut.

5.4 Conclusion

This work presents a novel cost-effective automatic resonance tracking scheme for PTs with MPT. Different from conventional approaches, this scheme is based on a BPF oscillator, which exploits the PT's intrinsic resonant point through a sensing bridge. It guarantees automatic resonance tracking and maximum electrical power converted into mechanical motion regardless of process variations and environmental interferences. An amplitude control for a switching power stage is developed to regulate the output mechanical motion and provide different power levels.

The proposed scheme is applied to a UVSD system for electrosurgical purposes. The system is implemented both in discrete components form and monolithic ASICs form. The sealing and dissecting functions were verified in chicken tissue and glycerin. The PT showed outstanding hemostasis and efficient dissections with minimal lateral thermal damage and low smoke generation. The system provided good stability and fast settling performance as small as 10 ms under glycerin loading conditions.

6 SIGNAL PROCESSING FOR UNIFIED RF AND UVSD SYSTEM

6.1 Background

6.1.1 Motivation

The goal of this research project is for TEES and Covidien to co-develop a combined sensing scheme circuit that allow multiple surgical tissue debulking, vessel sealer and dissector (VSD) technologies to operate from the same sensing scheme board. The energy research team at Covidien wants to combine Covidien Sonicision Ultrasonic VSD technology with Covidien radio frequency (RF) electrosurgery technology including, especially, RF vessel sealing called LigaSure (LS). The target application is a smaller hand-held-like family of US/LS devices with no more than about 50 W average for both modes.

The advantage of having both VSD systems working with the same sensing scheme is that a single driver controller could be used for both systems simplifying the complexity and design cost. Including the ability to handle more than one resonant frequency provides the latitude to develop ultrasonic tissue debulking capabilities. Tissue debulking requires operation at resonant frequencies form 20 kHz to 60 kHz. Further benefits include reduced parasitics and delays, resulting in a higher performance VSD system.

6.1.2 Challenges of the Conventional V and I Sensing

The main challenge in combining both the LS with the US technologies is that the LS system operates at a higher frequency, around 500 kHz, compared with the US

system operated around 50 kHz. Therefore, the sensing scheme needs to have high selectivity in two frequency bands for proper operation of both systems.

To realize regulated output power, the LS system requires the magnitude and phase information to calculate the effective power, and apply this information to the switched power converter as a feedback signal for the controller. For the US system only the motional current is needed for the operation of the controller and the motional bridge could successfully detect the motional current across the ultrasonic transducer. Moreover, the output signal applied to both systems should be sine or square wave. Based on these requirements, the functions needed are accurate current sensing, phase sensing, and passband selecting.

6.2 Sensing Scheme for VSD System with RF & US Transducers

The proposed combined VSD system is composed of three parts as shown in Figure 123: the US transducer and driver, the signal processing module in FPGA, and the voltage and current sensing paths for RF.

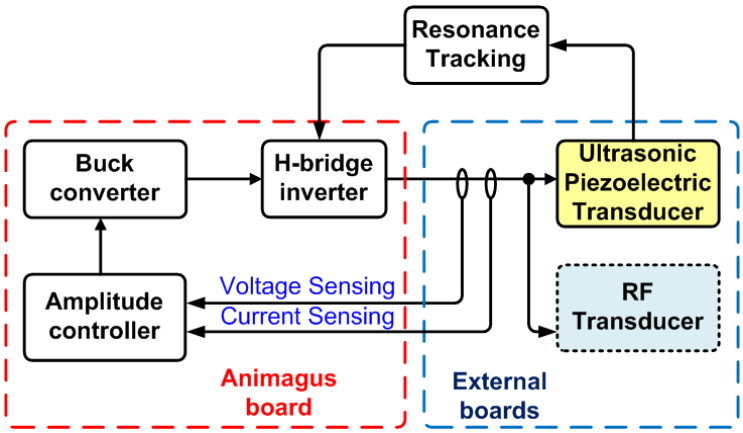
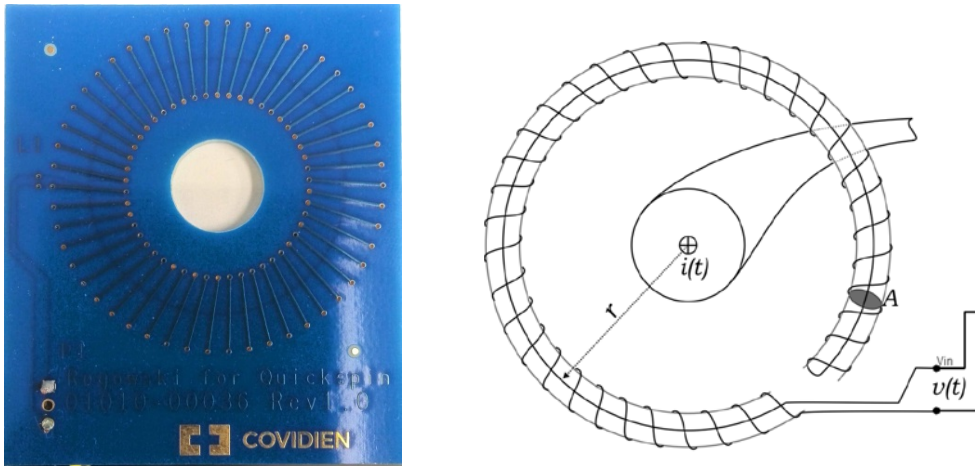


Figure 123. VSD system block diagram.

6.2.1 Rogowski Coil Current Sensor



(a) (b)

Figure 124. (a) Rogowski coil for current sensing, and (b) its conceptual structure.

Rogowski coil is a widely used topology for measuring alternating current (AC) or high speed current pulses [135]-[137]. Its structure is demonstrated in Figure 124, which consists of a helical coil of wire with the lead from one end returning through the center of the coil to the other end. Its main advantage is that the Rogowski coil shows low inductance, thus can respond to fast-changing currents. Another advantage is that it has excellent linearity, which is crucial for matching with the other voltage sensing chain.

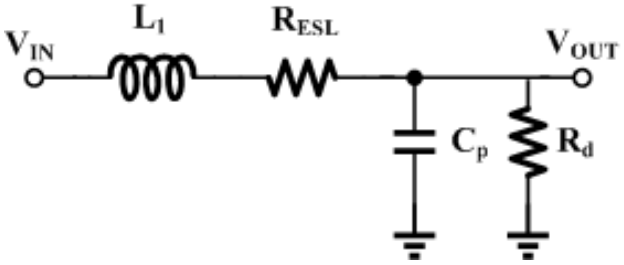


Figure 125 Electrical model of the Rogowski coil.

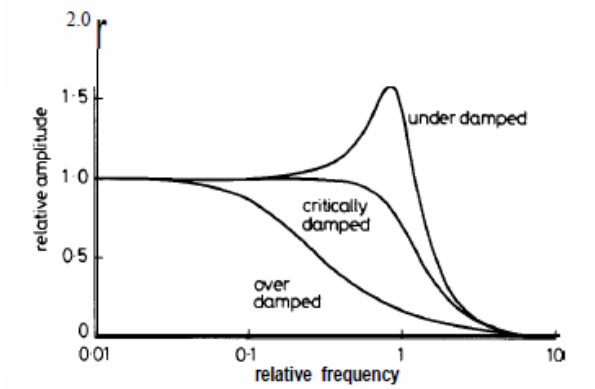


Figure 126. Frequency responses of Rogowski coil with different Q values.

The Rogowski coil can be modeled as a RLC high pass filter as shown in Figure 125. The L_1 represents the inductance of the coil. The R_{ESL} represents the equivalent series resistance of L_1. C_p represents the output parallel capacitor. R_d represents the termination resistor which determines the quality factor Q of the sensor. For different Q values, the frequency responses are compared in Figure 126. Smaller R_d induces higher Q, wider bandwidth, and peaking at the L_1C_p resonant frequency. Larger R_d induces lower Q, narrower bandwidth, and flattened gain. Generally, R_d is tuned for different application scenarios.

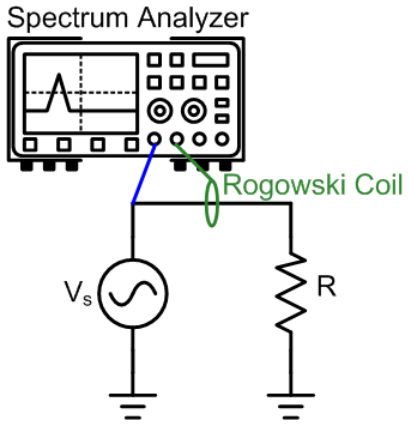


Figure 127. Testbench for the Rogowski coil.

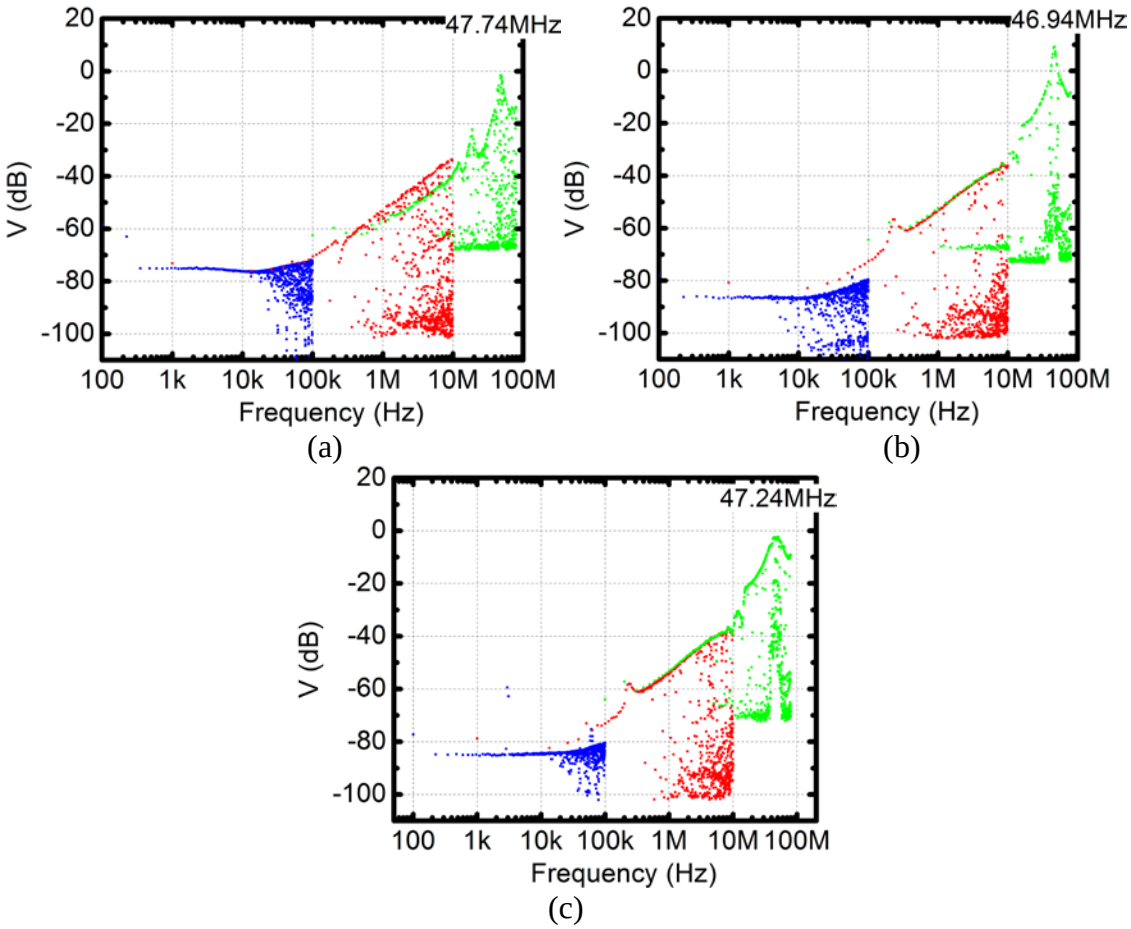


Figure 128. Frequency responses of the Rogowski coil with three samples: (a), (b), and (c).

There are three Rogowski samples, which are tested with spectrum analyzer as shown in Figure 127. A signal generator V_s sweeps the frequency. The loading resistor R converts the voltage into a current signal. Then, the spectrum analyzer is used to capture the voltage information from the current sensor, then plot its frequency response. The frequency responses of the Rogowski coils are shown in Figure 128.

Based on the peak in the plots, the location of the complex poles can be averaged as $(47.24 + 47.74 + 46.94)/3 = 47.31\ MHz$. Based on this value, the extracted electrical model of the Rogowski coil is refined as below,

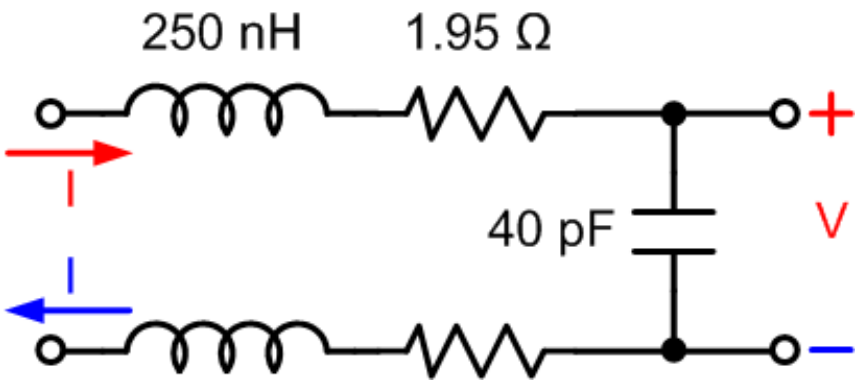


Figure 129. Extracted electrical model of the Rogowski coil.

6.2.2 Capacitive Voltage Divider

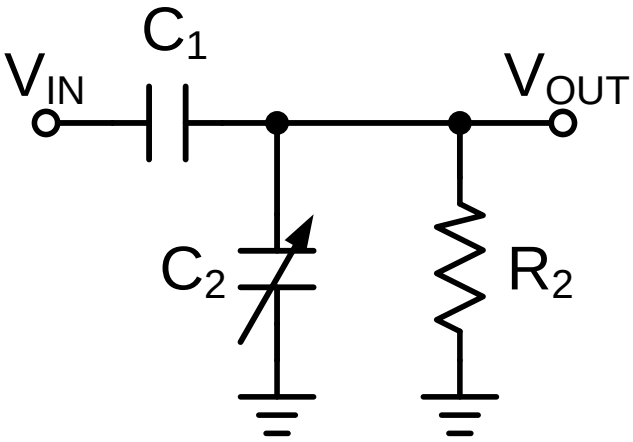


Figure 130. Electrical model of the capacitive voltage divider.

The AC voltage sensing is implemented by a capacitor divider topology as Figure 130. The load transducer is parallel with two series capacitors, C_1 and C_2. Their ratio, $C_1/(C_1+C_2)$, defines the voltage sensing gain. Here, C_1 = 1.61 pF and C_2 = 441 pF, which results in a dividing gain as 1:275 or -48.8dB. A resistor, R_2, is added to match the high pass frequency characteristics of current sensor, which will be discussed in next section.

6.3 I Sensing with 2nd-order Active-RC Filter

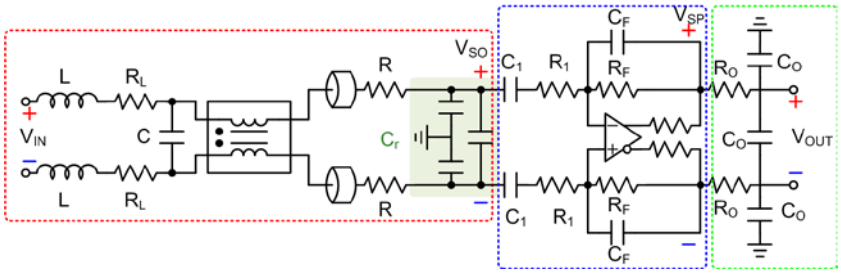


Figure 131. Current sensing chain with three functional blocks.

The current sensing chain is characterized by three functional blocks as observed in Figure 131: the Rogowski coil and input integrating in the red box, the signal processing circuit in the blue box, and the output RC filter in the green box. The signal processing circuit equalizes and band-passes the sensed signal. The output RC filter further limits the high frequency noise and anti-alias for following analog-to-digital converters.

The input stage in the red box is called passive termination for Rogowski coil. Its benefits is that the R-C_r pair gives limited bandwidth upon Rogowski coil as,

$$H_{I\_Passive} = \frac{V_{SO}}{V_{IN}}$$

$$= \frac{1 + sC_rR}{s^3LC_rCR + s^2[L(C_r + C) + C_rCRR_L] + s[R_L(C_r + C) + C_rR] + 1} \quad (67)$$

$$= \frac{1 + \frac{s}{\omega_z'}}{\left(s^2 + \frac{\omega_{p1,2}'}{Q}s + {\omega_{p1,2}'}^2\right)\left(1 + \frac{s}{\omega_{p3}'}\right)}$$

However, the Rogowski coil becomes a 3rd-order system, and its nature is very hard to match with analog circuits.

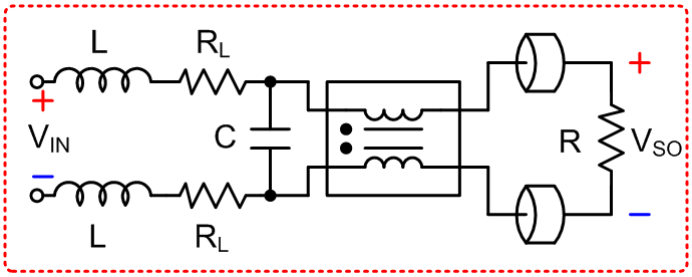


Figure 132. Self-integrating termination for the Rogowski coil.

An alternative structure is called self-integrating and depicted in Figure 132. The Rogowski coil is terminated with a single resistor R. Thus, its transfer function is simplified as,

$$H_{I\_Self} = \frac{V_{SO}}{V_{IN}} = \frac{s}{LCs^2 + \left(\frac{L}{R} + CR_L\right)s + \frac{R_L}{R} + 1} = \frac{s + \omega_z}{s^2 + \frac{\omega_{p1,2}}{Q}s + {\omega_{p1,2}}^2} \tag{68}$$

where

$$\omega_z = 0, \qquad \omega_{p1,2} = \sqrt{\frac{\frac{R_L}{R} + 1}{LC}} \tag{69}$$

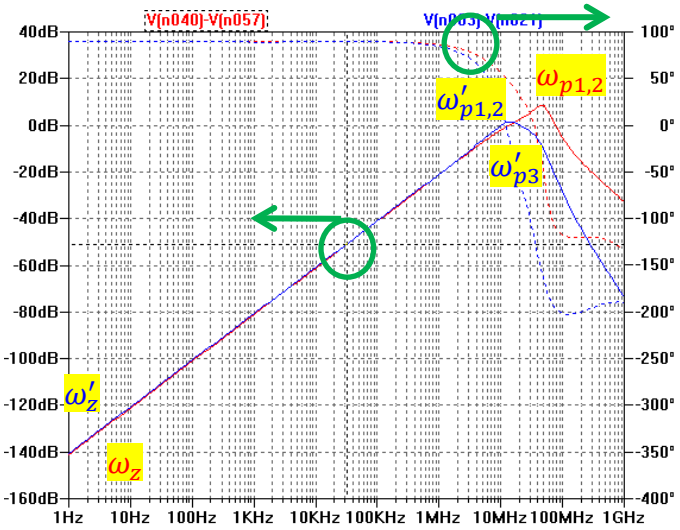


Figure 133. Simulated performance of (blue) passive integrating sensor, and (red) self-integrating sensor.

The sensor and entire sensing chain with integrating and self-integrating are simulated in Figure 133. Apparently, the self-integrating scheme has less order and much wider bandwidth. In other applications, the uncontrolled bandwidth will cause stability problem, however, in this scenario, the high frequency signal can be truncated by following filters. Its main advantage is that the 2nd-order complex poles can be mimicked by analog circuits discussed in Section 6.4.

The signal processing block in blue box in Figure 131 is a 2nd-order BPF. It provides the required passband and stops the DC fluctuation and high frequency noise. Its transfer function is,

$$H_{I\_BPF} = \frac{V_{SP}}{V_{SO}} = \frac{sC_1R_F}{(1+sC_FR_F)(1+sC_1R_1)} = \frac{s+\omega_{BP\_z}}{\left(1+\frac{s}{\omega_{BP\_pF}}\right)\left(1+\frac{s}{\omega_{BP\_p1}}\right)} \qquad (70)$$

where

$$H_{I\_BPF} = \frac{V_{SP}}{V_{SO}} = \frac{sC_1R_F}{(1+sC_FR_F)(1+sC_1R_1)} = \frac{s+\omega_{BP\_z}}{\left(1+\frac{s}{\omega_{BP\_pF}}\right)\left(1+\frac{s}{\omega_{BP\_p1}}\right)} \qquad (71)$$

$$\omega_{BP\_z} = 0, \qquad \omega_{BP\_pF} = \frac{1}{C_FR_F}, \qquad \omega_{BP\_p1} = \frac{1}{C_1R_1} \qquad (72)$$

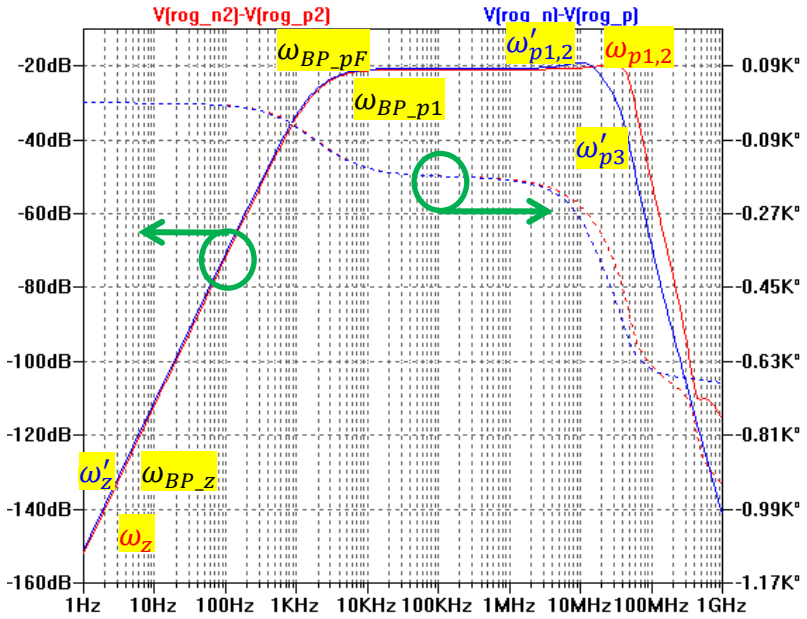


Figure 134. Simulated performance of the entire current sensing with (blue) passive integrating, and (red) self-integrating.

The entire frequency responses of the current sensing chain with passive/self-integrating are compared in Figure 134. From the results, the self-integrating scheme has wider bandwidth and less poles.

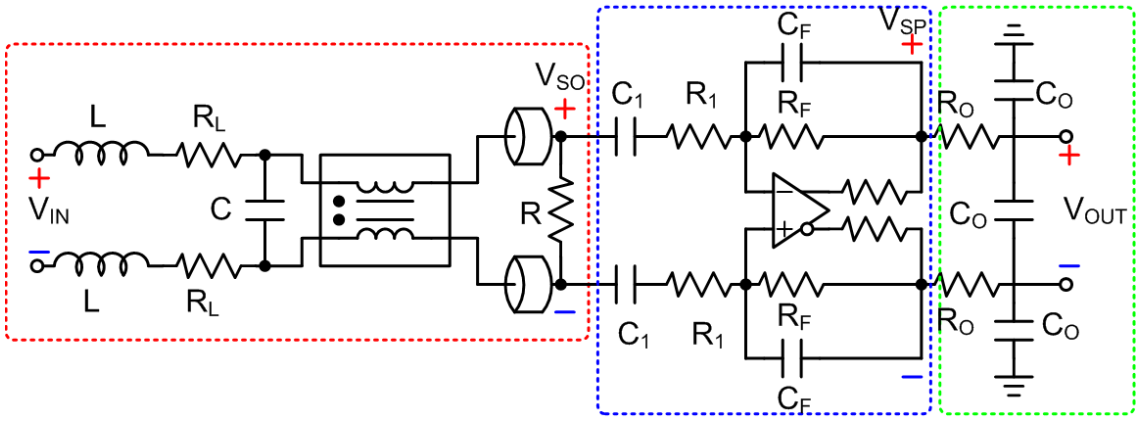


Figure 135. Rogowski sensing chain with self-integrating termination.

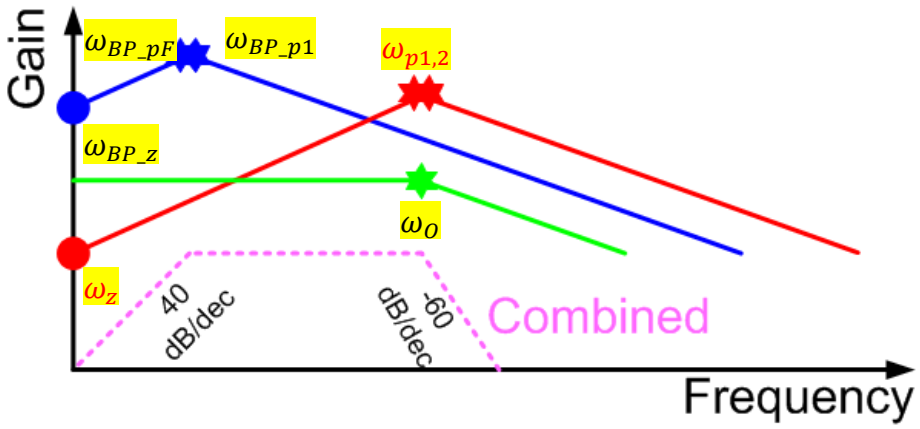


Figure 136. Frequency responses from the three functional blocks, and (bottom pink) the combined signal chain.

Summarily, the entire current sensing chain is depicted in Figure 135. Its transfer function of the passive integrating Rogowski coil can be estimated as Figure 136. The 1st order RO-CO filter with ω_O in the green box further limits the high frequency noise and anti-alias for following analog-to-digital converters.

The entire response is estimated as the bottom pink dashed line. It demonstrates a wide BPF performance. There are 2 zeros at the origin, 2 complex poles at the low frequency, 2 real poles at the high frequency.

6.4 V Sensing with 2nd-order Tom-Thomas Filter

6.4.1 Real Zeros/Poles Matching

To finely drive the RF transducer, the output voltage and current should be extracted to calculate the impedance of the RF transducer and consumed its active power. However, the voltage and current are sensed with different sensing structures, and have different frequency response and are distorted.

Therefore, the gain and phase matching between voltage and current sensing chains is the main challenge. The reason is that the calculation of AC output power is not only depends on the magnitude, but also depends on the phase angle. Thus, an ideal voltage and current sensor have same gain and phase across the operating frequency.

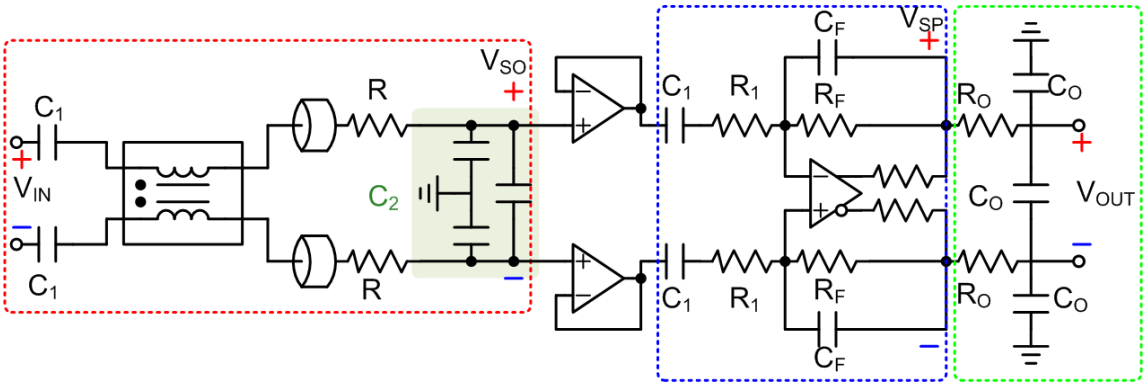


Figure 137. Frequency responses of the voltage sensing chain.

The initial idea is to build an analog filter for voltage sensing chain, which matches its frequency response with the current sensing counterpart as Figure 137. It is composed of three blocks and discussed as following. Note that its main difference from Figure 135 is that the voltage sensor is capacitive instead of inductive.

6.4.1.1 Input Stage

The input stage in the red box consists of a zero and pole as,

$$H_{V\_input} = \frac{V_{SO}}{V_{IN}} = \frac{sC_1R}{1 + s(C_1 + C_2)R} = \frac{s + \omega_{V\_z1}}{1 + \frac{s}{\omega_{V\_p1}}} \tag{73}$$

where

$$\omega_{V\_z1} = 0, \qquad \omega_{V\_p1} = \frac{1}{(C_1 + C_2)R} \tag{74}$$

The 1st-order HPF stops the DC fluctuation. It follows by two voltage buffer.

6.4.1.2 Signal Processing Stage

The signal processing stage is similar to the BPF in the current sensing chain. Its transfer function can be derived as,

$$H_{V\_BPF} = \frac{V_{SP}}{V_{SO}} = \frac{sC_1R_F}{(1+sC_FR_F)(1+sC_1R_1)} = \frac{s-\omega_{V\_z2}}{\left(1+\frac{s}{\omega_{V\_p2}}\right)\left(1+\frac{s}{\omega_{V\_p3}}\right)} \quad (75)$$

where

$$\omega_{V\_z2} = 0, \qquad \omega_{V\_p2} = \frac{1}{C_FR_F}, \qquad \omega_{V\_p3} = \frac{1}{C_1R_1} \quad (76)$$

6.4.1.3 Output RC filter

The output 1st-order RC filter with ω_O is identical to the counterpart in the current sensing chain.

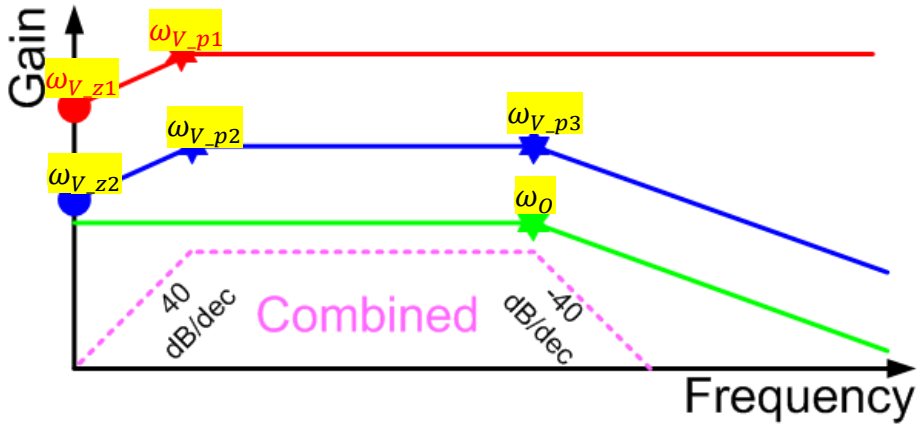


Figure 138. Frequency responses from the voltage sensing chain with real zeros/poles.

The resulting frequency response can be estimated as Figure 138. Although the low frequency corner with 40 dB/dec is same with Figure 136, the high frequency corner

only has 2 real poles and -40 dB/dec. Thus, 1 more pole is needed to balance the magnitude and phase shift.

However, even we add 1 more real pole, such as adding 1 RC stage at the output, there is significant difference between Figure 136 and Figure 138. This is because the high frequency corner in Figure 136 is composed of two complex poles. On the other hand, the corner in Figure 138 is composed of two independent real poles. Compared with multiple real poles in magnitude domain, the complex poles has peaking feature. In phase domain, the roll off of complex poles is much faster than overlapped real poles. Principally, the quality factor Q of the complex poles controls those differences.

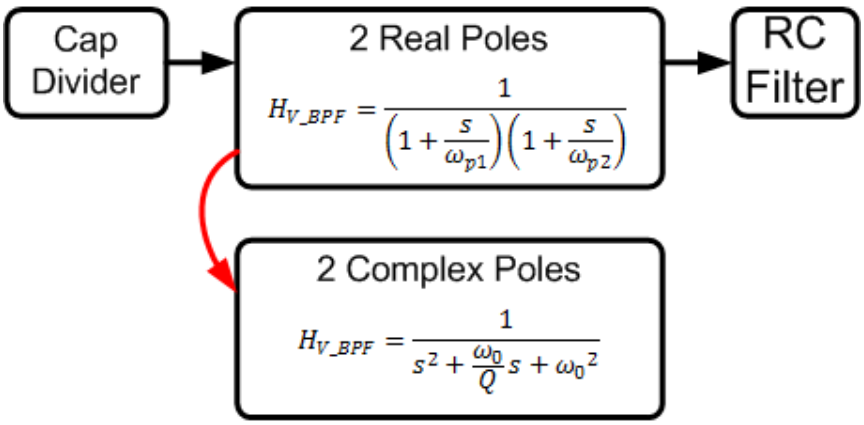


Figure 139. Proposed voltage sensing chain with 2 complex poles.

As discussed in Section 6.2.1, the complex poles come from the nature of Rogowski coil and inevitable. Thus, the approach that uses 2 real poles to match complex poles is not accurate both in magnitude and phase domain. As shown in Figure 139, we propose to replace the 2 real poles filter, and rebuild exactly the same complex poles through analog circuit theory.

6.4.1.4 Biquad BPF Matching

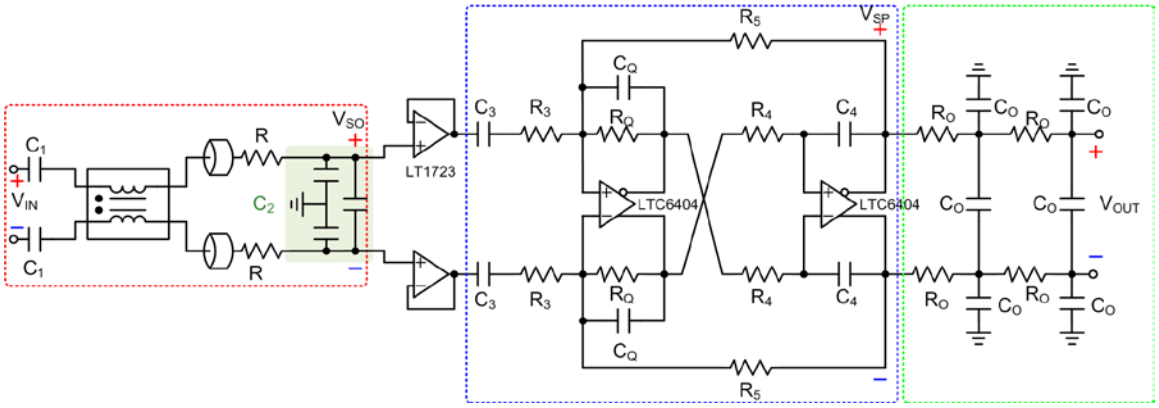


Figure 140. Proposed voltage sensing chain with biquad filter.

The first topology with 2nd-order complex poles we tried is biquad BPF. Its structure is proposed in Figure 140. The BPF transfer function can be derived as,

$$H_{V\_BPF} = \frac{V_{SP}}{V_{SO}} = \frac{\dfrac{1}{C_4 C_Q (R_3 + \dfrac{1}{sC_3}) R_4}}{s^2 + s\dfrac{1}{C_Q R_Q} + \dfrac{1}{C_Q C_4 R_4 R_5}}$$

$$= \frac{1}{(sR_3C_3 + 1)} \cdot \frac{s\dfrac{C_3}{C_Q} \cdot \dfrac{1}{R_4 C_4}}{s^2 + s\dfrac{1}{C_Q R_Q} + \dfrac{1}{C_Q C_4 R_4 R_5}} \tag{77}$$

$$= \frac{s + \omega_{V\_z2}}{\left(1 + \dfrac{s}{\omega_{V\_p2}}\right)\left(s^2 + \dfrac{\omega_{V\_p3,4}}{Q} s + {\omega_{V\_p1,2}}^2\right)}$$

where

$$\omega_{V\_z2} = 0, \qquad \omega_{V\_p2} = \frac{1}{R_3 C_3}, \qquad \omega_{V\_p1,2} = \sqrt{\frac{1}{C_Q C_4 R_4 R_5}} \tag{78}$$

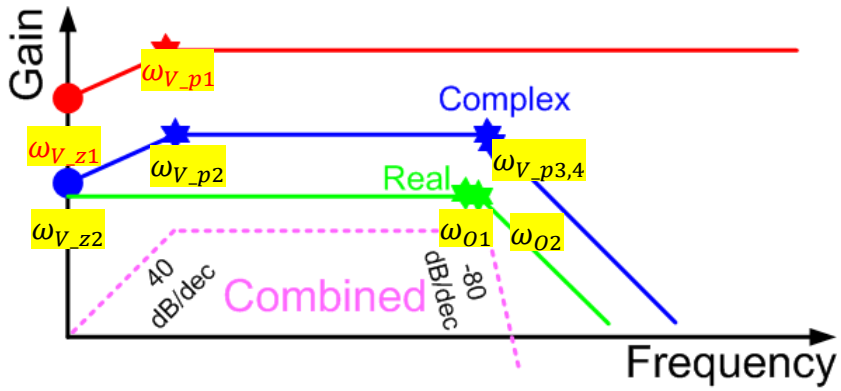


Figure 141. Estimated frequency response of the voltage sensing chain with biquad BPF.

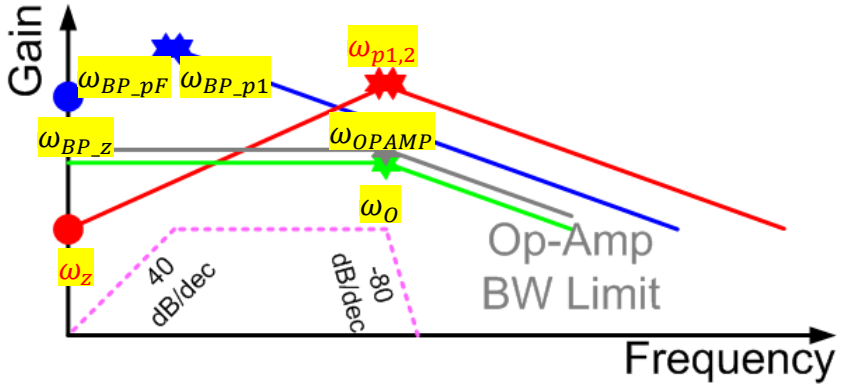


Figure 142. Estimated frequency response of the current sensing chain with Op-Amp bandwidth limit.

It has 1 real zeros ω_{V_z2}, 1 real pole ω_{V_p2}, and 2 complex poles $\omega_{V\_p3,4}$. The bode plot of the entire voltage sensing chain is depicted in Figure 141. There is an additional RC LPF with ω_{O2} at the end, which is used to compensate the additional op-amp bandwidth with ω_{OPAMP} in the current sensing chain. The practical frequency response of the current sensing chain is given in Figure 142.

Comparing the following two figures, the voltage sensing chain well matches the current sensing chain not only in number of zeros/poles, but also in the properties of them.

6.4.2 V Sensing with 2nd-order MFB Filter

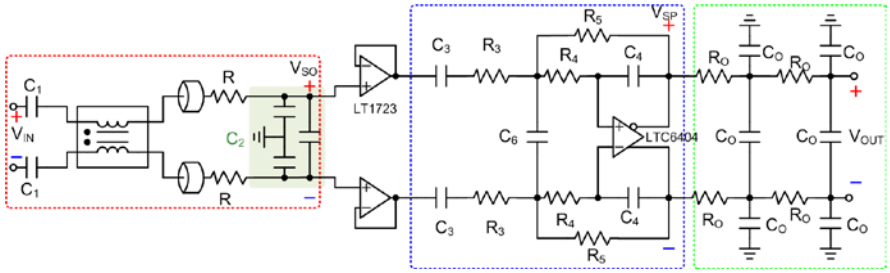


Figure 143. Proposed voltage sensing chain with MFB filter.

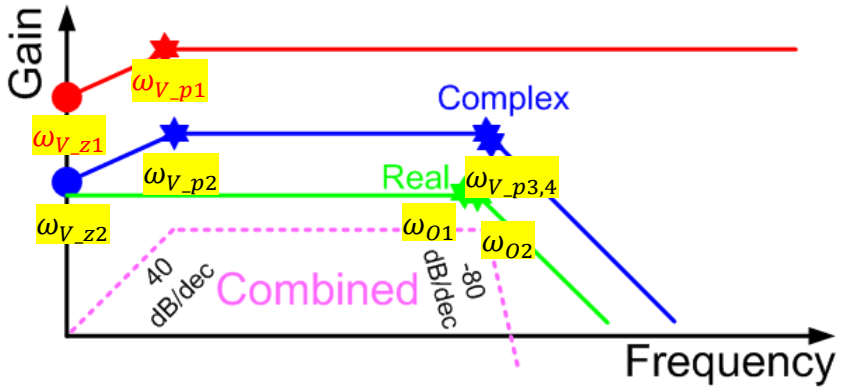


Figure 144. Estimated frequency response of the voltage sensing chain with biquad BPF.

The multiple feedback (MFB) filter is alternative topology for 2nd-order filter [138]. It is shown in the blue box in Figure 143. Its transfer function can be derived as,

$$H_{V\_BPF} = \frac{-\dfrac{1}{C_4 C_6 (R_3 + \dfrac{1}{sC_3}) R_4}}{s^2 + s\dfrac{1}{C_6}\left(\dfrac{1}{R_3 + \dfrac{1}{sC_3}} + \dfrac{1}{R_4} + \dfrac{1}{R_5}\right) + \dfrac{1}{C_4 C_6 R_4 R_5}} \tag{79}$$

$$= \frac{s + \omega_{V\_z2}}{\left(s^2 + \dfrac{\omega_{V\_p3,4}}{Q} s + {\omega_{V\_p1,2}}^2\right)\left(1 + \dfrac{s}{\omega_{V\_p2}}\right)}$$

Because the generic MFB topology can only generate LPF or HPF, we choose the LPF topology, and add an input R_3C_3 HPF to define the band-pass feature. Its frequency response is similar to the curves in Figure 141 and satisfies the signal processing requirement.

Comparing Figure 140 and Figure 143, the main difference between biquad and MFB filter is the cost of hardware:

1) The biquad topology uses 2 Op-Amps, more resistors and capacitors. However, the parameters such as natural frequency or quality factor can be independently tuned by R or C.
2) The MFB is more hardware efficient; however, its parameters are highly correlated and difficult to be modified. For example, $R_{3\text{-}5}$ can be tuned to change the natural frequency, but also affects Q.

6.5 Digital Frequency Discriminator in FPGA

6.5.1 Challenge in Frequency Discriminator

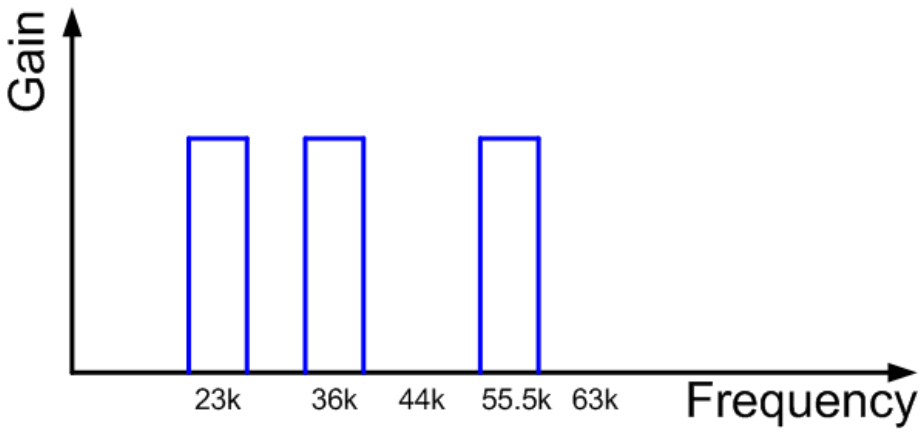


Figure 145. Required pass and stop frequencies of the frequency discriminator.

The original proposal intends to merge the ultrasonic transducer with RF transducer. However, there are several unwanted resonant modes for the ultrasonic transducer such as 44 kHz and 63 kHz. Also, the operating resonant modes should be selectable such as 23 kHz, 36 kHz and 55.5 kHz. The expected frequency response is depicted in Figure 145. There are several difficulties for using analog filters:

1) The stop frequencies and pass frequencies, such as 44 kHz, 63 kHz and 55.5 kHz, are too close to be differentiated. For high dampen gain such as 40 dB at 44 kHz and 63 kHz, a high Q BPF is needed.
2) The additional frequency discriminator requires hardware. In Figure 123, it should be included in the resonance tracking block. However, we have the voltage sensing & current sensing chain proposed in the hybrid system, and the auxiliary ADC and microcontroller (FPGA) in the amplitude controller block. Thus, the current information can be reused for the US resonance tracking.
3) Another advantage of the fully digital frequency discriminator is a substitute of the motional feedback bridge and reduces the cost. The tradeoff is the speed of real-time filtering highly depends on the sampling rate of the ADC and system clocks of the FPGA, which may induce more delay compared with the motional feedback bridge and degrade Q of the US resonance loop.

The original motional feedback back, which is depicted in Figure 99, establish the relationship between I_m and V_{MFB} as,

$$V_{MFB} = I_1 R_3 - I_2 R_2 = \alpha(s) \cdot I_m \tag{80}$$

$$\alpha(s) = \frac{\left[Z \cdot s\left(R_3C_3 - R_2C_p\right)\right] - R_2}{1 + sR_3C_3} \tag{81}$$

when $\omega \ll \frac{1}{R_3C_3}$,

$$\alpha(s) = -\frac{R_2}{1 + sR_3C_3} \approx -R_2 \tag{82}$$

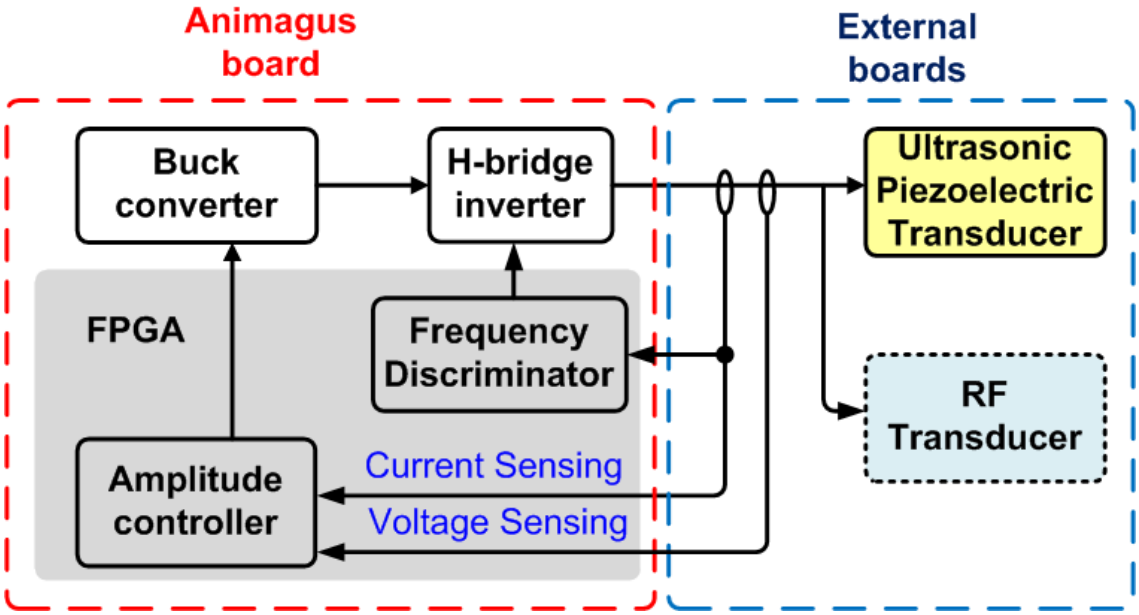


Figure 146. Proposed digital frequency discriminator in the FPGA module.

On the other side, the current sensing chain with the Rogowski coil also executes the current-to-voltage conversion as Section 6.2.1. Thus, we can reuse the information and leverage the filtering challenge. The only difference is that the motional bridge helps the piezoelectric transducer band-pass the 55.5 kHz. However, in the frequency discriminator approach, the digital filter should provide sharp selection for required frequency. The proposed architecture is demonstrated in Figure 146.

6.5.2 IIR Band-pass Filter

In FPGA, the infinite impulse response (IIR) filter is preferred due to its compact structure. Compared with finite impulse response (FIR) filter, the minimized number of registers gives minimum delay between input and output signals, and maintains the high Q feature of the resonance circuit.

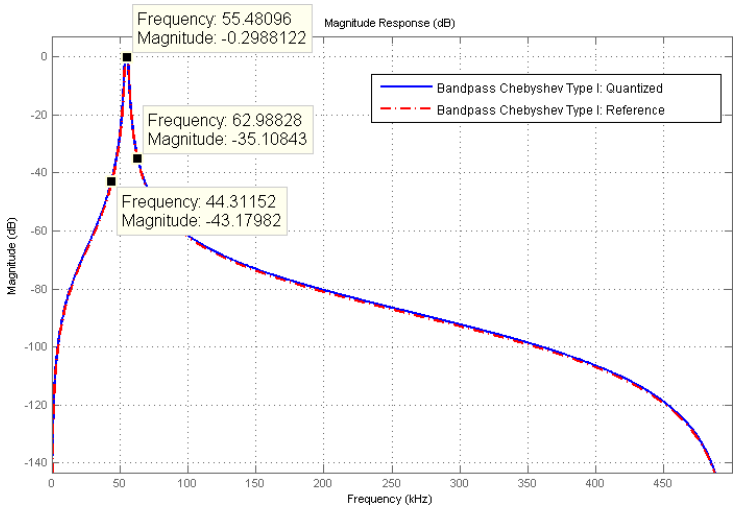


Figure 147. Simulated frequency discriminator programmed at 55.5 kHz.

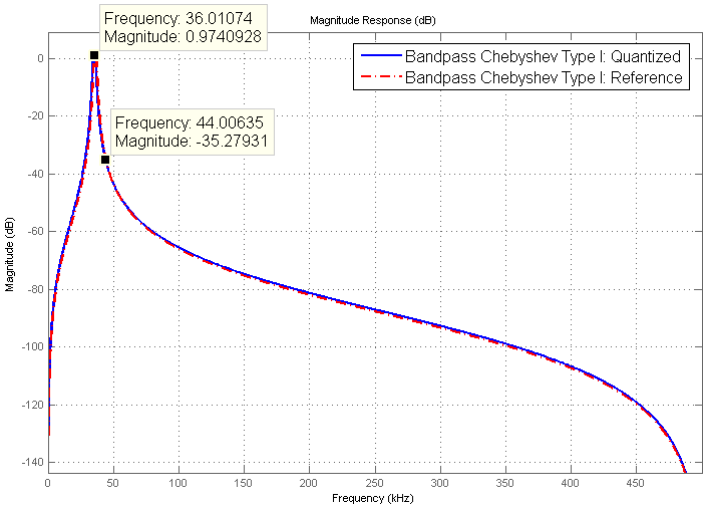


Figure 148. Simulated frequency discriminator programmed at 36 kHz.

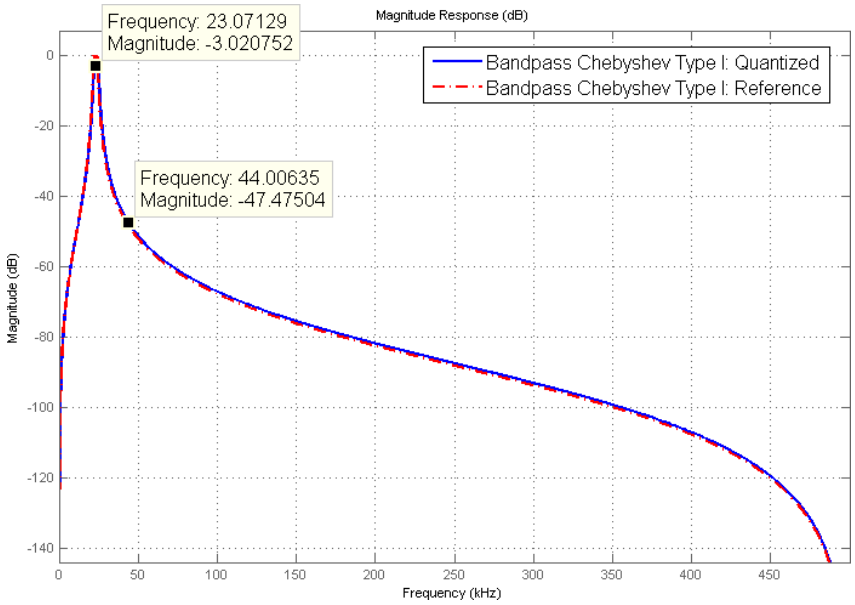


Figure 149. Simulated frequency discriminator programmed at 23 kHz.

The IIR is implemented as Chebyshev Type-I BPF with direct-form II [139]. The order is 4 with 2 sections of biquad. The coefficients are quantized into 16 bits signed number for FPGA programming. Their performances with theoretical model and quantized model are compared in Figure 147, Figure 148, and Figure 149.

For the 55.5 kHz US mode, the unwanted 44 kHz and 63 kHz are dampened by -43 dB and -35 dB, respectively. For the 36 kHz US mode, the unwanted 44 kHz is dampened by -35 dB. For the 23 kHz US mode, the unwanted 44 kHz is dampened by -47 dB. All of these dampen are large enough to guarantee the ultrasonic transducer is operated in desired resonant mode.

6.6 Measurement Results

6.6.1 Simulation & PCB Implementation

The sensing chains are implemented as Figure 150, Figure 151, and Figure 152.

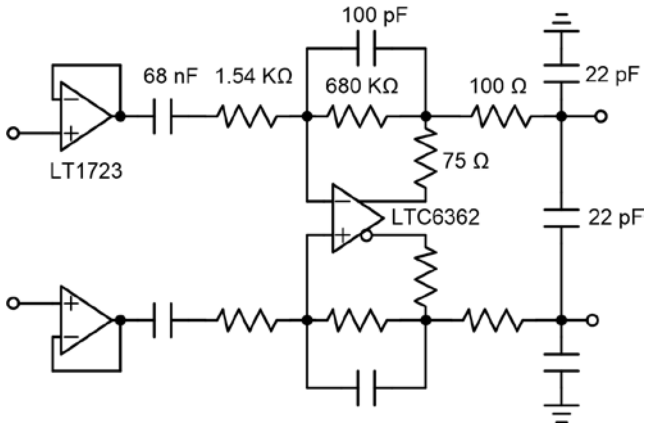


Figure 150. Proposed current sensing chain.

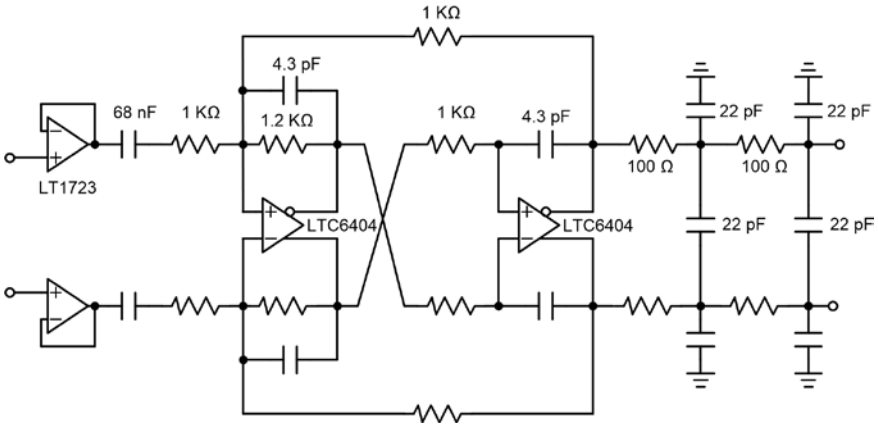


Figure 151. Proposed voltage sensing chain with biquad filter.

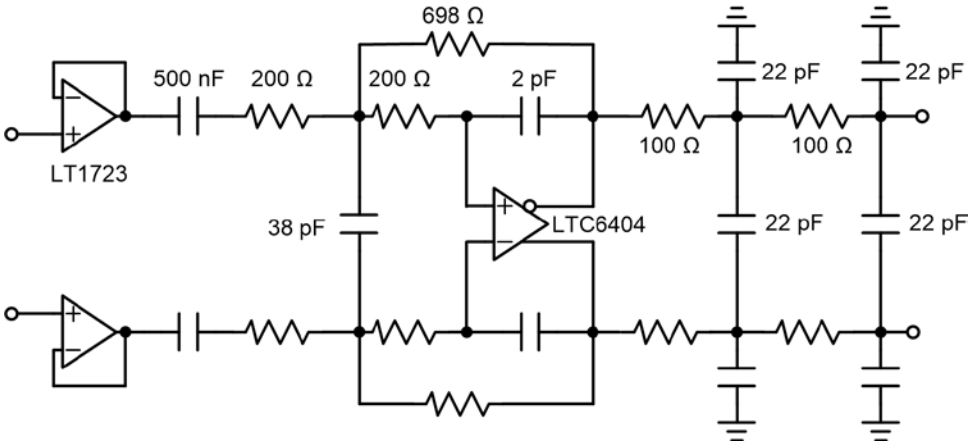


Figure 152. Proposed voltage sensing chain with MFB filter.

The gain and phase information are simulated across wide frequency range and listed in Table 14. Taking the 500 kHz performance as a reference, their gain error is calculated in Table 15. From these results, the proposed biquad and MFB voltage sensor well matches the Rogowski current sensor, especially in phase domain at high frequency. This is because the properties of complex poles are identical with similar Q values.

Table 14. Simulated gain and phase performances.

		Current Sensor	Original V Sensor	w/ Biquad	w/ MFB
15 KHz Low Corner	Gain (dB)	-28.12	-55.84	-55.78	-55.78
	Phase (deg)	-139.33	-142.64	-143.86	-143.86
55 kHz Ultrasonic	Gain (dB)	-26.97	-54.90	-54.90	-54.90
	Phase (deg)	-176.60	-176.91	-177.13	-177.14
500 kHz RF	Gain (dB)	-26.96	-54.89	-54.90	-54.90
	Phase (deg)	-183.62	-183.30	-184.19	-184.27
20 MHz High Corner	Gain (dB)	-26.46	-60.68	-59.21	-59.41
	Phase (deg)	-334.56	-352.36	-331.40	-337.65

Table 15. Gain error at different frequencies.

	Current Sensor	Original V Sensor	w/ Biquad	w/ MFB
5 KHz Low Corner	Gain (dB)	-0.95	-0.88	-0.88
	Phase Error (%)	-0.919	-1.258	-1.2583
55 kHz Ultrasonic	Gain (dB)	-0.01	0	0
	Phase Error (%)	-0.086	-0.147	-0.15
500 kHz RF	Gain (dB)	0	0	0
	Phase Error (%)	0.0889	-0.158	-0.1806
20 MHz High Corner	Gain (dB)	-5.79	-4.31	-4.51
	Phase Error (%)	-4.944	0.8778	-0.8583

The PCB was fabricated as Figure 153. The Rogowski current sensing chain locates in the middle. For best matching, the biquad voltage sensor is placed in the left side, and the MFB voltage sensor is placed in the right side. Their input can either external generated with BNC ports, but can also be given by a high current driver with 0.5 A capability in the top of the board. The Rogowski coil and cap divider are connected with pin socket for easily replacing. The fully differential output BNC ports locate in the bottom of the board as illustrated in Figure 153.

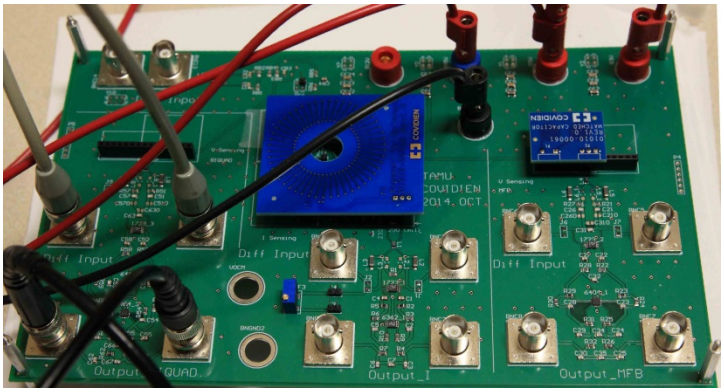


Figure 153. Tested PCB with voltage and current sensing chains.

6.6.2 Testing Setup & Approach

Because we don't have the equipment to simultaneously measure the gain and phase performance of the sensing chain, we manually input sinusoidal signal and measured output waveform. As Figure 154, the data was collected and fit with equation as,

$$y = y_0 + A * \sin(pi * (x - x_c)/w) \tag{83}$$

The extracted parameter A defines the magnitude. x_c/w defines the phase information.

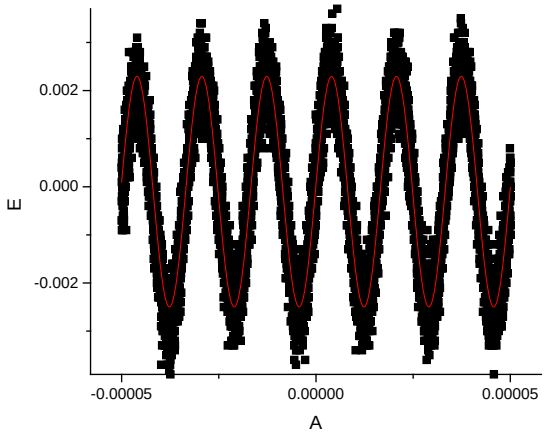


Figure 154. Measured data fitting for a sinusoidal model.

This model extraction approach provides accurate phase information; however, its extracted magnitude is affected by the measurement noise. Especially for common-mode testing at high frequency, the input and output signal is too smaller than noise to give a valid fitting as Figure 155. Thus, we use RMS value of the waveform for gain calculation.

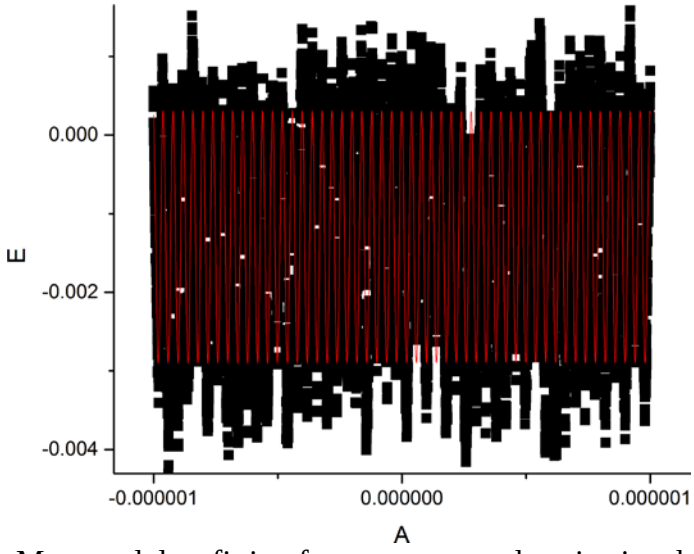
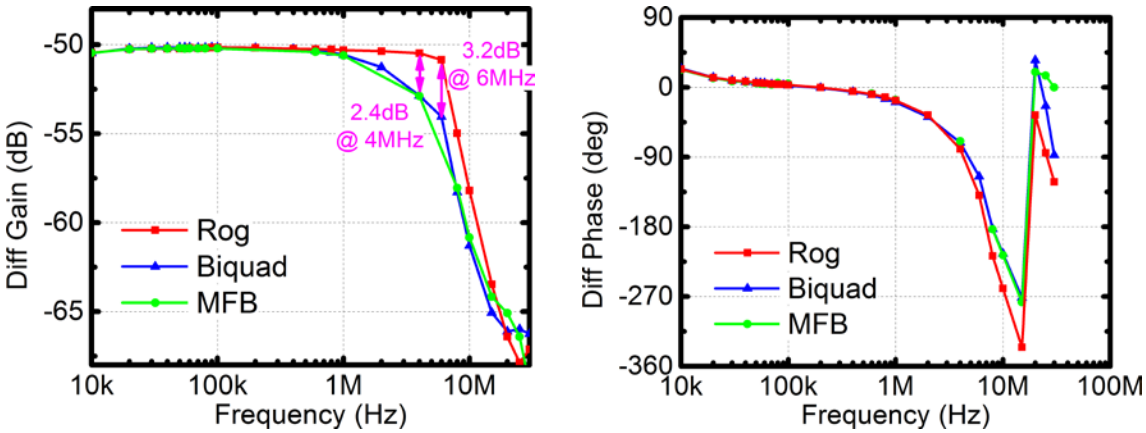


Figure 155. Measured data fitting for common-mode gain signal at 25 MHz.

6.6.2.1 Matched Sensing Performance

As shown in Figure 156, the biquad voltage sensing chain matches well with the MFB topology, both in magnitude and phase. Their magnitude difference with the Rogowski current sensor is 2.4 dB @ 4 MHz, and 3.2 dB @ 6 MHz, which is around the 5^{th}-order harmonic of 1 MHz RF signal.

The phase information is detailed in Figure 157. The worst phase mismatch happened between Rogowski current sensor and biquad voltage sensor as 22.6º @ 6 MHz, which satisfy the <45° specification.



(a) (b)

Figure 156. Measured (a) differential gain and (b) phase of the sensing chains.

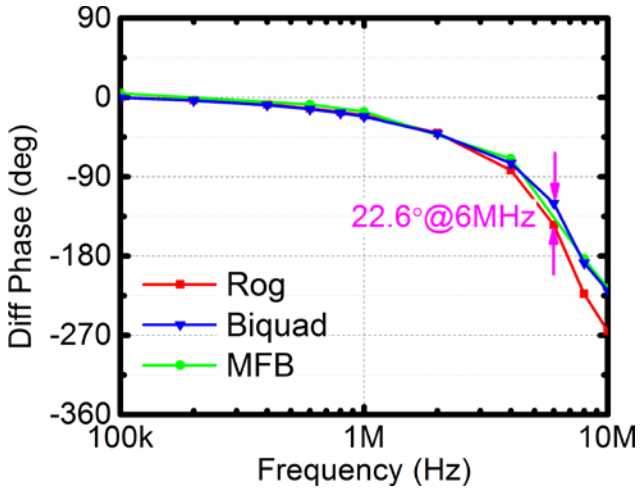


Figure 157. Detailed phase mismatch.

6.6.2.2 Matched Common-mode Performance

The common-mode performance was measured by shorting the input of sensor and manually swept the frequency. The proposed circuits feature excellent common-mode gain as -50 dB. Above 10 MHz, the common-mode gain becomes degradation.

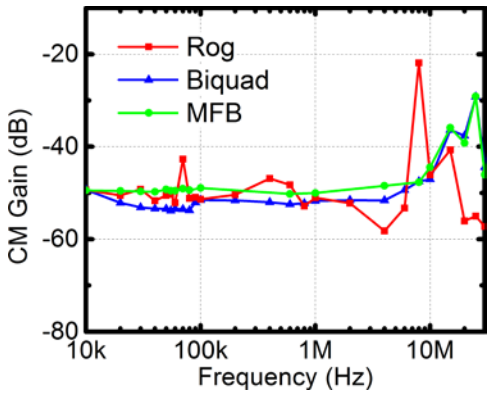


Figure 158. Common-mode gain of the voltage & current sensing chains.

6.7 Conclusion

The design and analysis of the sensing circuits for vessel sealing and dissection systems were reported. The sensing chain consisted in a voltage sensing path and a current sensing path. To ensure accurate average power calculation, the delay from both sensing paths has to be small. The goal of the presented design is to match this by ensuring that both sensing paths have the same frequency response up to the desired frequency of operation. This has been demonstrated by the implementation of the sensing signal chain in a PCB with satisfactory testing results.

Based on the matched voltage and current sensing chains, an improved sensing strategy is proposed to solve the wide rage frequency selection for US. An IIR based 4^{th}-order fully digital frequency discriminator is proposed in FPGA to guarantee the piezoelectric transducer resonating in required modes. Such topology also removes the motional feedback bridge, simplifies the resonance tracking loop and reduces hardware cost. The performance of the IIR based frequency discriminator was verified through simulations.

7 CONCLUSIONS

7.1 Energy Harvesting for Internet of Things

The first part of this dissertation discusses and presents the energy harvesting method for IoT smart nodes. Cost, efficiency, and applicability are the three main requirements for the IoT energy harvester. Therefore, four power management ICs are developed to solve those various harvesting challenges:

1) A switched capacitor DC-DC converter is chosen to eliminate the need for an off-chip inductor. The conventional MPPT approach is improved by replacing the frequency modulation with the capacitor value modulation, which eliminates the dynamic power consumption and enhanced peak conversion efficiency 89% under 29 μW.
2) The power consumption of the MPPT module gives a significant obstacle for ultra-low power IoT applications. Therefore, we propose a new MPPT method by reusing the regulation information, processing the algorithm in time-domain, and saving the quiescent power consumption. Consequently, the entire harvesting efficiency is improved to 86.4% with a throughput power as low as 12 μW.
3) The tracking accuracy and range of the conventional MPPT is limited by the dimension of modulation. Thus, we propose a two-dimensional MPPT method to extend the harvesting range as 0.45 to 3 V with flattened PCE as high as 89% for a throughput power below 50 μW.

4) The applicability of the IoT smart nodes is taken into account, and a new MPPT method with the single-cycle regulation is proposed to eliminate the bulky storage capacitor for lower cost. Moreover, a novel thyristor-based structure is proposed to squeeze the power consumption of the oscillator into nanowatt-level and enables self-startup and self-sustaining capabilities.

7.2 Power Management for Biomedical Devices

The second part of this dissertation discusses and presents the study of power management issues for biomedical devices. Vessel sealing and dissection using ultrasonic transducers provides good performance over conventional electrosurgery. Thus, a UVSD system with a novel cost-effective automatic resonance tracking scheme is developed to deliver precise surgical jobs. Different from conventional approaches, this scheme is based on a BPF oscillator, which exploits the PT's intrinsic resonant point through a sensing bridge. It guarantees automatic resonance tracking and maximum electrical power converted into mechanical motion regardless of process variations and environmental interferences.

Moreover, the compatibility between the UVSD system and the conventional RF system is studied for integration. The key challenge is to match the current and voltage sensing paths with same frequency response up to the desired frequency of operation. Thus, a biquad BPF and a MFB filter are developed to mimic the behavior of the Rogowski current sensing by zeros/poles matching. This has been demonstrated by the implementation of the sensing signal chain in a PCB with satisfactory testing results.

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APPENDIX

List of publications resulting from these research:

Patents:

- U.S.A. Patent No. 20,160, 023, 021, “Electrosurgical ultrasonic vessel sealing and dissecting system”, **X. Liu**, A. I. Collie-Menchi, J. A. Gilbert, D.A. Friedrichs, K. W. Malan and E. Sánchez-Sinencio, January 28, 2016.

Conferences:

- **X. Liu**, A. Colli-Menchi, and E. Sanchez-Sinencio, Student Research Preview, *IEEE International Solid-State Circuits Conference (ISSCC)*, Feb. 2016.
- **X. Liu** and E. Sanchez-Sinencio, “21.1 A single-cycle MPPT charge pump energy harvester using a thyristor-based VCO without storage capacitor”, *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 364-365, Feb. 2016.
- **X. Liu** and E. Sanchez-Sinencio, “A 0.45-to-3V reconfigurable charge-pump energy harvester with two-dimensional MPPT for Internet of Things,” *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 370-371, Feb. 2015.
- J. Amanor-Boadu, M.A. Abouzied, S. Carreon-Bautista, R. Ribeiro, **X. Liu**, E. Sanchez-Sinencio, “A switched mode Li-ion battery charger with multiple energy harvesting systems simultaneously used as input sources,” *IEEE 57th International Midwest Symposium on Circuits and Systems, pp. 330-333, Aug. 2014*.
- L. Ibarra, B. Hilton, M. Nawal, S. Carreon-Bautista, M. Abouzied, **X. Liu**, R. Ribeiro, J. Amanor-Badu, E. Miller, J. Vanegas, E. Sanchez-Sinencio, “SmartShelter: A Sustainable power system design using energy harvesting

techniques," *IEEE 57th International Midwest Symposium on Circuits and Systems*, pp. 467-470, Aug. 2014.

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Journals:

- **X. Liu**, L. Huang, K. Ravichandran, and E. Sanchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional MPPT for Internet of Things," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 51, no. 5, pp. 1302-1312, May 2016.
- **X. Liu** and E. Sanchez-Sinencio, "An 86% efficiency 12 μW self-sustaining PV energy harvesting system with hysteresis regulation and time-domain MPPT for IOT smart nodes," *IEEE Journal of Solid-State Circuits (JSSC),* vol. 50, no. 6, pp. 1424-1437, Mar. 2015.
- **X. Liu**, A. Colli-Menchi, J. Gilbert, D. Friedrichs, K. Malang, and E. Sanchez-Sinencio "An automatic resonance tracking scheme with maximum power transfer for piezoelectric transducers," *IEEE Transactions on Industrial Electronics (TIE),* vol. 62, no. 11, pp. 7136-7145, Nov. 2015.
- **X. Liu** and E. Sanchez-Sinencio, "A highly-efficient ultra-low photovoltaic power harvesting system with MPPT for Internet of Things (IOT) smart nodes," *IEEE Transactions on VLSI Systems*, vol. 23, no. 12, pp. 3065-3075, Dec. 2015.