A STUDY OF OZONE AS AN OXYGEN SOURCE FOR THE GROWTH OF HIGH-K DIELECTRIC FILMS FOR GATE DIELECTRIC ON GAN/ALGAN/GAN

A Thesis

by

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Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

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December 2016

Major Subject: Electrical Engineering

ABSTRACT

GaN is a promising alternative to silicon technology for the next-generation high-power and high-frequency electronics. The choice stems from the intrinsic properties of GaN of a wide bandgap and consequently high breakdown voltage, high saturation electron velocity and good thermal conductivity. Spontaneous and piezoelectric polarization effects cause accumulation of a high density of carriers at III-Nitride heterointerfaces enabling engineering of high mobility channels.

The primary factor inhibiting the further growth of GaN HEMTs is the high leakage current leading to device unreliability. The MIS-structure used in Si-CMOS processing has been adapted and shown to reduce leakage current in GaN technology. However, the introduction of an insulator adds another interface which suffers from poor quality due to innumerable traps with varying time constants. This leads to device threshold voltage instability and drain current collapse, while decreasing the device transconductance due to the increased gate-to-channel spatial separation. High-κ dielectrics have been shown to reduce leakage current with smaller decrease in transconductance in Si-CMOS technology and therefore, applied to GaN technology. ALD is recognized as a novel method for high-κ gate dielectric deposition, where H_2O is primarily used as the oxygen source for growth; excellent properties have been reported. However, ozone-grown films show further suppressed leakage current and offer better interfacial quality on silicon.

In this study, MOSCaps have been developed on GaN/AlGaN/GaN heterostructures with PECVD Si_3N_4 and ALD HfO_2 as the passivation layer and gate dielectric, respectively. HfO_2 was grown using *either* H_2O *or* ozone as the oxygen source. XPS analysis, capacitance-

voltage, conductance-voltage and leakage current-voltage characteristics have been used as probes to study the quality of the film and its interface with the III-N semiconductor.

It is observed that due to the sufficient supply of oxygen, ozone helps in the formation of a better bulk dielectric by more complete oxidation. However, the interface is degraded by uncontrolled surface oxidation of the barrier layer or/and penetration of oxygen impurities, creating shallow donor traps aiding in leakage. The overall leakage current with the ozone-grown dielectric is reduced by almost half-an-order of magnitude due to the better bulk dielectric achieved.

To my parents…

ACKNOWLEDGEMENTS

I, hereby, would like to express my immeasurable appreciation and deepest gratitude for the help and support extended by the people mentioned hereafter toward the accomplishment of my two-year journey at Texas A&M University.

My deepest and sincerest gratitude goes out to my research adviser and mentor, Professor H. Rusty Harris, who has constantly appreciated my potential and imbibed in me the spirit to adventure into this arduous journey, with his excellent motivation and advice. Thank you for the spellbinding introduction in ECEN 688, to the enchanting area of fabrication and microelectronics, which happened be to my first course-work for my Master's program. This course provided me with a direction and paved the way for a new journey under your responsible supervision.

Sincere regards are also due to two of my course-mentors: Professor Haiyan Wang and Professor Jun Kameoka (who also happens to be one of my committee members), for their immensely helpful course content. In addition, I would like to thank them for their useful and insightful discussions about concurrent topics related to research and for providing me with constant enthusiasm to do better.

I would also like to thank my esteemed committee members: Professor Aydin Karsilayan and Professor Rupak Mahapatra, for taking valuable time out of their schedules to go through my thesis and come up with ideas of betterment.

A big thank you is due to everyone at AggieFab. Special mention should be made of Larry Rehn and Jim Gardner, for their constant full-fledged lab-support; they assisted me in

developing the proper care and skill to work with new equipment. Without you people, this work would not have been this smooth.

My sincerest gratitude goes out to all the staff associated with the Department of Electrical and Computer Engineering for all their support. Special thanks are due to Tammy Carda and Melissa Sheldon for passionately guiding me through the procedural complications and allowing me to concentrate only on my work by taking the responsibility for all paperwork.

The assistance, cooperation and company of my fellow group members deserve special mention. The companionship and cooperation of Alex, Feyza, Jae Woo, Michael, Pranav, Sravani and William will always be remembered. Thank you for all your support, time and the respect you have shown me. Thank you Alex, for being so supportive through the moments of anxiety and the moments of joy. Useful discussions with you were always a source of knowledge and relief for me. Thanks to William for constantly hammering me to take care of my health, besides your help on numerous other occasions.

My dear friend, Mohammadreza Soleymaniha, deserves special mention here. Your support, company and friendship helped me through the thick and thin. It is hard to describe the help you extended in words.

I would like to take this opportunity to thank some of my very special friends who have laughed and cried with me and have been available whenever I needed them.

Finally, all of this would have only been a dream without the support, immense love, endless encouragement, wise counsel and support of my parents. It would be the best feeling for me if this work makes them proud of their efforts in bringing me up the way they have.

NOMENCLATURE

ε_0	Permittivity of vacuum
ε_r	Relative electric permittivity
μ_n	Mobility of electrons
2DEG	2-dimensional electron gas
ALD	Atomic layer deposition
CV	Capacitance-voltage measurements
CVD	Chemical vapor deposition
DI	Deionized
DRAM	Dynamic random access memory
FET	Field effect transistor
FG	Forming gas
GaN	Gallium nitride
GV	Conductance-voltage measurement
HEMTs	High electron mobility transistors
HFETs	Heterostructure field effect transistors
JFoM	Johnson figure-of-merit
MBE	Molecular beam epitaxy
MIS	Metal insulator semiconductor
MOCVD	Metal-oxide chemical vapor deposition
MOS	Metal oxide semiconductor
MOSCaps	MOS capacitors

PDA	Post-deposition anneal
PMA	Post-metallization anneal
RF	Radio frequency
RIE	Reactive ion etching
TEMAH	Tetrakis ethyl methyl amino-hafnium
TLM	Transfer length method
TMA	Trimethyl aluminum
v_{sat}	Saturation velocity of electrons
V_{TH}	Threshold voltage

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1. INTRODUCTION

1.1 GaN for RF applications

GaN has many attractive properties for being the choice for next-generation high-power and high-speed electronic applications. It is a wide bandgap material (E_g ~3.4eV) and has a high breakdown electric field, a high electron saturation velocity (higher than Si devices) and high density of states due to spontaneous polarization, all of which make it suitable for high output power density applications in communication technologies. Additionally, GaN is a direct bandgap material and finds immense usage in blue laser applications. When heterostructures are formed, for example with AlGaN, the induced strain in the film due to the differences in lattice parameters between GaN and AlGaN , added with the large potential barrier of the AlGaN on GaN causes a piezoelectric effect to add to the spontaneous polarization of AlGaN itself to accumulate a high density of carriers forming a well-confined channel called the 2-DEG at the interface, allowing vertical scaling engineering [5]. The high breakdown field and high mobility achieved allows for horizontal scaling which reduces the parasitic capacitance, increasing the potential for high cutoff frequencies (f_T). A compilation of different electronic properties of competing semiconductors, Si, Ge and GaN is enlisted in Table 1.

Table 1. Electronic properties of Si and GaN

	Si	GaAs	GaN
E_g (eV)	1.12 (indirect)	1.42	**~3.4 (direct)**
μ_n (cm^2/V-s)	1350	8500	**~1800**
$E_{breakdown}$ (MV/cm)	0.3	0.5	**3.3**
V_{sat} (10^7 cm/sec)	~1.0	~1.1	**2.5**
ε_r	11.9	12.9	8.9
Heat dissipation, Θ (W/cm-K)	1.3	~0.4	~1.3

From previous works, the Johnson figure of merit (JFoM) ($f_T \times E_{breakdown}$) of GaN-HEMTs can be seen to surpass the JFoM for the competing semiconductors namely GaAs and SiC, with an ultra-high f_T of 450GHz and simultaneous f_{MAX} of 440GHz [6]. The reduction of parasitic capacitances and delays allows for extreme parameters to be achieved using GaN-HEMTs. The channel in transistors made on Si work well till 140°C, beyond which external dopants cease to play any role, due to the small band-gap of Si. On the contrary, due to the larger band-gap of GaN, transistors made on GaN have been shown to withstand and work *well* up to temperatures of 300°C. These properties of GaN excited the research community to further study the potential of GaN to replace Si for high-speed and high output power devices.

1.2 Potential for market

Power semiconductors have long been in the game for the development of high-power and high-voltage semiconductors for various applications including space electronics and radio-frequency communication applications. However, as Si-based power devices are reaching their technical limits, newer materials are in the process of replacing them. Among these, GaN has immense potential to be used in high-power and high-speed circuits which make them suitable for use in aerospace electronics, renewable energy systems, advanced next-generation communication systems, RADAR and RF frequency applications. GaN Power Semiconductors market has been estimated to be worth $2.60 billion by the year 2022 [7].

However, according to a particular market research firm, Yole Développement, GaN still needs technical enhancements in the manufacturing process [8]. This mainly stems from the lack of high quality growth mechanisms for GaN, unlike its competing counterpart, Si. Transistors and RF-devices fabricated on GaN have proven to be excellent alternatives to their Si counterparts. The most important factor that can contribute to the exploding market of GaN

would be the ability to process GaN devices in a similar flow as the Si-CMOS processing. This would shorten the time needed for the maturity of the GaN processing, while reducing further research costs, development time and yield thereby reducing the cost per die. Additionally, the need for replacement of tools and equipment for the development of GaN technology would be minimal.

1.3 Schottky-contact HEMTs vs gated HEMTs

Over the previous decade, GaN HEMTs have been investigated rigorously for their excellent performance [6, 9-11]. In HEMTs, a Schottky contact is essentially used to modulate the already formed channel, i.e. the 2DEG. However, HEMTs have been shown to have high leakage current due to activation and field-assisted tunneling, leading to low gate voltage swing capabilities [12]. These issues can be addressed by the introduction of the MIS-structure famous in Si-CMOS processing. It has indeed been found by various research groups that the MIS-HEMT counterparts allow large gate voltage swings (described as 10% decrease from the maximum transconductance, g_{max}) without considerable increase in gate leakage current [13-15]. However, the introduction of a dielectric/insulator causes a negative shift in the threshold voltage, V_{TH}, due to increase in the spatial distance between the channel and the gate which translates to lesser transconductance than the HEMT counterparts. These effects might be taken care of by the use of high-κ dielectrics – a larger dielectric constant translates to larger electrical energy storage by the dielectric film – this could mean effective modulation by the gate due to relatively less decrease in transconductance than that achieved with low-κ dielectrics. High-κ dielectrics are generally referenced to the dielectric constant of the industry standard dielectric for all this while, SiO_2, which itself has a dielectric constant (κ) of 3.9. Various works have been reported on different insulators for the MIS-HEMT structures, namely HfO_2 [16, 17],

Al_2O_3 [14], Si_xN_y [18], Sc_2O_3 [19] and others. Amidst all the vast array of dielectrics, HfO_2 and Al_2O_3 have been studied extensively as alternatives for high-κ. It was shown by F Medjdoub *et. al.* that compared to unpassivated HEMTs, MISHEMTs with ALD Al_2O_3 showed an order of reduction in leakage current and a considerable increase in drain current density [20]. Similar results were achieved by YUE YuanZheng *et. al.* [14].

HfO_2 has a high dielectric constant of 20-25 and a relatively wide band gap (5.6-5.8 eV) that attracted its extensive study as a gate dielectric on Si-MOSFETs. The performance of HfO_2 has likewise been studied on GaN HEMTs as an alternative high-κ dielectric. The advantage of HfO_2 lies in its high dielectric constant which allows it to store more electric energy. Thus, for the same film thickness, HfO_2 can be a better choice for modulating the channel than its lower-κ counterparts. Various deposition methods for HfO_2 have been studied which includes the likes of ALD, reactive ion sputtering and pulsed-laser deposition (PLD), among which HfO_2 grown using ALD results in a much better uniformity of the film due to the self-limiting growth properties of ALD [16, 21, 22]. C Liu *et al*. studied the properties of reactive sputtered HfO_2 and showed the promising capability of suppressing the leakage current by an order of five compared to its HEMT counterpart while maintaining a very high drain current and a relatively high transconductance, presumably due to the high dielectric constant of HfO_2 with added current collapse immunity [23]. Lee *et al.* studied the impact of ALD HfO_2 on device reliability and performance concluding with the excellent suppression of leakage current [21]. Yue *et. al.* studied the properties of a laminated gate dielectric stack with HfO_2/Al_2O_3 (3nm/2nm) which resulted in an appreciable drain current and only single-digit percent decrease in transconductance, which was attributed mainly to the higher dielectric

constant of HfO_2 which allows it to store more charge for the same thickness of other dielectrics with lower dielectric constant [24].

ALD growth occurs over two cycles (binary reaction) – one cycle involves the introduction of the oxygen source, which prepares the surface by termination at –OH bonds when using H_2O as an oxygen source; in the subsequent cycle, metal precursors are introduced into the chamber, which break down the above mentioned bonds and form the desired oxide. More details about the principle of ALD growth and its benefits will be discussed in a later section. The most rigorously studied oxygen source for growth of high-κ dielectrics is H_2O. Good performance parameters of MIS-HEMTs with high-κ dielectrics grown using H_2O as oxygen source have been reported [25]. However, oxide films deposited by ALD with H_2O as oxygen source have been known to have impurities, namely residual carbon and hydroxyl (–OH) groups, which may facilitate the formation of an interfacial oxide layer degrading the EOT and leakage characteristics of the dielectric film. J. B. Kim *et. al.* compared the characteristics of ALD Al_2O_3 grown on Si substrates using either H_2O or O_3, in which case, growth done with O_3 showed lesser Al-Al clusters and –OH groups on the surface, groups which generally aid in leakage by degrading the interface and bulk properties of the film [26]. The reduction of –OH groups on the surface on O_3-grown Al_2O_3 enhanced the interfacial properties and resulted in a suppression of leakage current by one or two order(s) of magnitude compared to its H_2O-based counterpart. C-V characteristics showed similar EOT and much less pronounced shift in flatband voltage in the O_3-based Al_2O_3, which were again attributed to reduction of Al-Al clusters and removal of –OH groups from the surface. T Kobu *et. al.* extensively studied ALD Al_2O_3 on GaN using H_2O, O_3 and H_2O and O_3 combined as oxygen source, which revealed that H and C contamination could be reduced to an appreciable extent

by using both H_2O and O_3 precursors as oxygen source as compared to the films grown using individual precursors [27]. Moreover, similar reduction in Al-Al bonds was observed by inclusion of O_3, coupled with reduction of fixed charge that caused a positive shift in V_{TH}. Such reduction in –OH, C and H impurities is required for device reliability and good interfacial quality.

1.4 Purpose of this study

In this work, a gate-last process flow of fabricating metal oxide semiconductor capacitors has been developed for both Si and GaN/AlGaN/GaN-on-Si heterostructures. The gate dielectric, HfO_2, has been grown by ALD using either O_3 or H_2O as the oxygen source. Chemical analyses of the dielectric film grown on GaN/AlGaN/GaN using the two different oxygen sources have been performed using XPS. Electrical characterization in the form of capacitance-voltage, conductance-voltage and leakage current density have been used as probes to study the interfacial and bulk properties of the dielectric.

1.5 Outline of thesis

Section 1 has already dealt with a brief background and the need for MIS-HEMT structures with incorporation of high-κ dielectrics. Section 2 introduces important theoretical background required for reviewing the content of this work along with essential information about interface traps, their behavior and their measurement from electrical characterization of metal insulator semiconductor capacitor structures. Section 3 and 4 deal with the fabrication of the MOS-capacitors on Si and GaN/AlGaN/GaN-on-Si respectively, along with electrical characterization, measurement of trap densities and device performance parameters. Finally, the important inferences of this work have been summarized and any future study possible has been discussed in Section 5.

2. THEORETICAL BACKGROUND

2.1 GaN properties

Transistors fabricated on III-V semiconductors are called HEMTs. The high electron mobility and charge density comes from a combined effect of spontaneous and piezoelectric polarizations occurring in these materials. Due to the noncentrosymmetric structure of III-V compound crystals, they have two different crystallographic directions, which lie parallel to the basal plane (0001) and exhibit polarity along these axes [5]. In the hexagonal wurtzite GaN crystal, there can be termination at the surface with either Ga or N, forming Ga-face and N-face crystal respectively. By convention, a vector is denoted in the direction from a Ga atom to the nearest neighboring N atom. Hence, as shown in Fig. 1 [5], (0001) and (000$\bar{1}$) is the Ga-

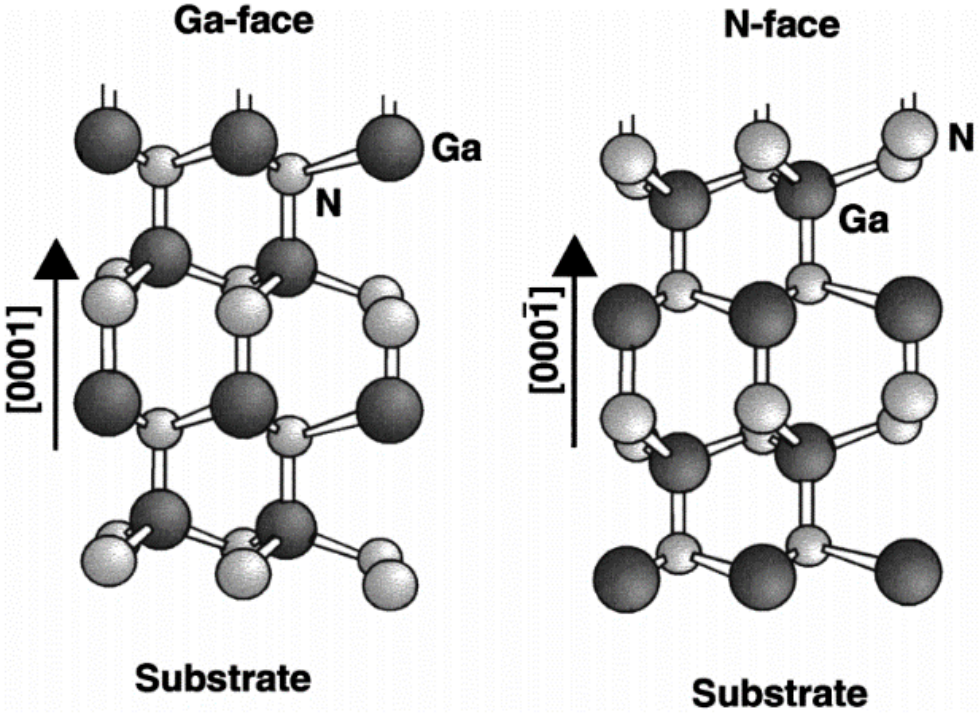


Figure 1. (a) Ga-faced and (b) N-faced GaN crystal structures. Reprinted from "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," by O. Ambacher *et. al,* 2000, *Journal of applied physics,* vol. 87, pp. 334-344, 2000. Copyright 2000 by American Institute of Physics. [5]

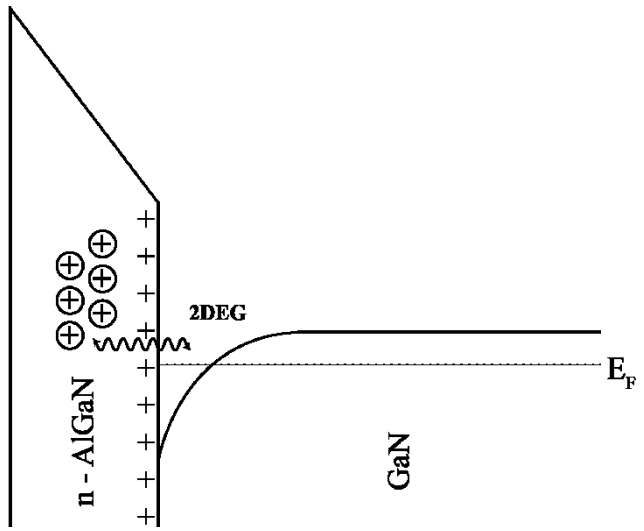


Figure 2. Band structure of n-AlGaN-GaN system showing the bending of the band and the presence of the 2DEG at the interface in equilibrium (Image shown here is not any simulated band diagram structure; it is used strictly for purpose of illustration)

face and N-face crystal respectively. The terminating atom decides the chemical and physical properties of these two different configurations.

When heterostructures are formed on Ga-faced GaN crystals, for example, AlGaN on GaN, the lattice mismatch between the two films causes a piezoelectric polarization which gives rise to a strong electrical field to the tune of 2MV/cm to be established and this strong field consequently induces a positive polarization charge at the AlGaN/GaN interface and the opposite negative polarization charge at the top of the AlGaN layer. Intuitively, the band tilts toward the interface, along with the Fermi level (see Fig. 2). For an n-doped AlGaN, which would then have donors in the bulk readily contributing conducting electrons, these electrons would then move toward the interface in order to compensate for the positive charge build-up at the interface and to restore local charge neutrality. The donors, now depleted, would have positive charges which reduces the overall intensity of the electric field in the AlGaN layer making the Fermi level flatter. These electrons would gather at the AlGaN/GaN interface,

forming the 2DEG, due to the Fermi level of GaN being lower than that of n-doped AlGaN. However, the whole concept of shifting intense research work toward heterostructure engineering was to avoid the various scattering effects associated with impurity doping in the channel material. Fortunately, for even an undoped AlGaN barrier layer, a 2DEG is formed at the interface of the AlGaN/GaN (see Fig. 3), which brings to question the origin of such electrons. In an undoped AlGaN layer, very few conducting electrons would be present and their concentration would not be enough to compensate for the large sheet of piezoelectric and spontaneous positive charge induced at the barrier interface with GaN. The possibility of electrons being supplied by the GaN bulk layer is almost absent because there exists a reverse electric field due to spontaneous polarization in the GaN bulk layer itself which would inhibit

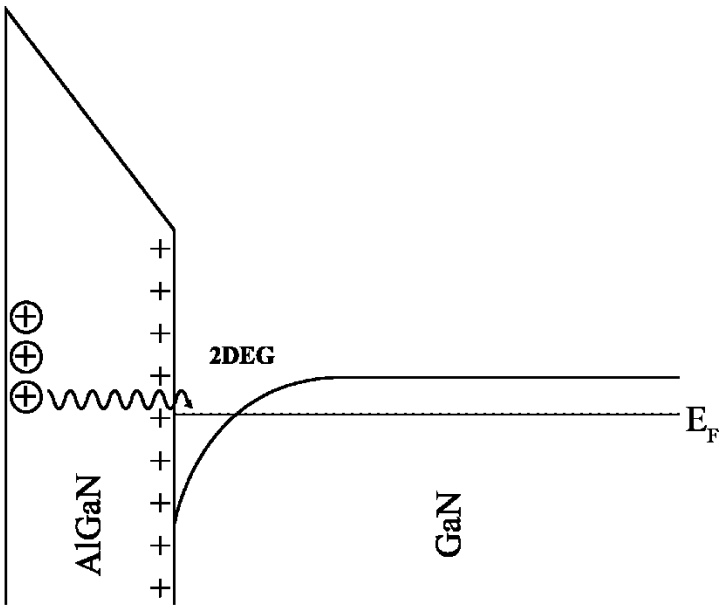


Figure 3. A schematic showing the presence of surface donors on an undoped-AlGaN layer surface providing electrons for the compensation of the polarization induced fixed positive charge at the AlGaN/GaN interface. These electrons are then trapped at the interface due to the high conduction band offset between GaN and AlGaN in what is known as a quantum well, forming the 2DEG at the interface (Image shown here is not any simulated band structure; it is used strictly for the purpose of illustration)

the flow of electrons. It is assumed that surface donors at the top surface of AlGaN provide with sufficient electrons to compensate for the induced positive charges at the interface [28]. All of the above discussion reverses when a N-faced GaN is used as the substrate material.

In contrast to a Si-based FET, where a potential is required to form the channel of carriers, the channel is always present due to the presence of the 2DEG in III-N semiconductor technology. In order to cut off the channel, a negative voltage is required to be applied. From the point of view of reliable, less leaky devices, normally-off transistors are preferred. Several methods have been studied to fabricate normally off transistors on AlGaN/GaN, which include the use of N-faced GaN as the substrate as explored by S. Sugiura *et.al.*[22] or the use of fluorine-based plasma treatment of the GaN or AlGaN as reported by Chen *et.al.* where the embedded fluorine ions essentially act like fixed negative charges thereby repelling the 2DEG and consequently enabling enhancement-mode operation [29]. However, plasma treatments have been known to facilitate defect generation at the barrier/III-N interface causing an increase in the scattering effects, failing the purpose of the 2DEG.

2.2 High-κ dielectrics

Introducing high-κ dielectrics in fabrication of MOS structures traces its way back to the infamous Si-MOSFETs. Gordon Moore, the co-founder of Intel and Fairchild Semiconductor, in his 1965 paper, now famously known as Moore's law, made an observation which essentially described the doubling of the number of components (transistors) per integrated circuit every year [30]. In 1975, this observation was revisited by Moore himself to adjust the pace to "doubling every two years". Indeed, for a long time till the 2000's, the observation Moore made was holding, and steadfast growth was made in semiconductor industry to meet the challenging prophecy.

To keep up with the pace, the physical size of the transistors had to be reduced significantly to allow the doubling of components. Si was the most common semiconductor those days essentially because of the high quality native oxide, SiO_2, and nitride, Si_3N_4, that could be formed by thermal treatments in an oxygen and a nitrogen environment respectively, followed by the quality of SiO_2 grown in a steam environment. These were excellent dielectrics for use in the capacitors required for DRAMs, because the quality of the interface between the semiconductor and its oxide was the best possible known to the semiconductor industry. The interface states density at the SiO_2/SI interface was found to be a record low at ~10^9 $cm^{-2}eV^{-1}$. The low interface states density allowed for further scaling of the dielectric down to a few nanometers helping to keep up with the pace of the Moore's law and exhibiting excellent leakage current performance parameters and admirable control of drain-to-source current via the gate. Classical mechanics ruled the mechanism of current control up to this point. The horizontal scaling led to dramatically decreasing the gate length (L_g) and the vertical scaling required drastic decrease in the oxide thickness (t_{ox}), leading to the thinning of the dielectric to a few nanometers (~1 nm), the thickness of a few monolayers. As a reference, the oxide thicknesses for the 90 nm and 70 nm gate technology nodes are 1.2 nm and 0.7 nm respectively, compared to the 3nm thickness for tunneling limit for SiO_2. This introduced a whole new world of issues with further scaling which called for an exponential increase in the amount of research and development for newer alternatives to SiO_2.

Quantum physical effects started dominating the mechanisms of these scaled devices, especially tunneling. Tunneling is a quantum mechanical effect where electrons, if provided enough thermal or field energy in the form of an electrical field, can tunnel through a thin oxide layer. Various tunneling models have been developed over the past two decades, a few being

Fowler-Nordheim (FN), Direct Tunneling (DT) and Poole-Frenkel (PF) tunneling. Tunneling increases leakage currents which results in heat generation in the integrated circuit, thereby introducing unreliability in the device operation. Another issue often encountered in ultra-thin oxide films is soft-breakdown or temporary breakdown. Voltage stress on the gate contact induces a current which in turn increases leakage current, also resulting in device unreliability. When all these effects are combined with temperature and bias stressing, the devices with ultra-thin oxide films exhibit detrimental levels of leakage currents, to the order of 100 A/cm^2 at gate voltage of 1V, which can cause true breakdown of the devices. With the billions of transistors on a single chip, this leakage would mean power drain as well as heat dissipation problems.

The technological industry had to make an important consideration and rethink the whole process to keep up with the pace set by Moore's law. This paved the way for the introduction of the high-κ dielectrics, where 'κ' refers to the dielectric constant. From a simple consideration of the parallel plate capacitance relation,

$$C_{equivalent} = \kappa \frac{\varepsilon_0 A}{t_{oxide}} \quad (1)$$

where ε_0 is the absolute permittivity of vacuum, A is the effective area of the capacitor, t_{oxide} is the effective thickness of the oxide and κ is the relative permittivity of the oxide, it can be seen that the capacitance is a multiple by a factor of 'κ'. Hence it is possible to maintain a thick dielectric, where the factor 'κ' compensates for the thickness by maintaining the capacitance as would be achieved using a thin SiO_2 layer. This introduces a concept namely 'effective oxide thickness (EOT)', which relates the thickness of the SiO_2, the semiconductor industry-standard dielectric thus far, that would be required to emulate the same capacitance as that of the corresponding thickness of high-κ dielectric and can be expressed as follows:

$$EOT = t_{high-\kappa} \cdot \left(\frac{\kappa_{SiO_2}}{\kappa_{high-\kappa}} \right) \quad (2)$$

Since SiO_2 has many of the desirable properties required for the operation of gated devices, it is imperative that similar properties are to be desired from the high-κ dielectrics that would replace SiO_2. Some of these property criteria are met by a few dielectrics, namely HfO_2, Al_2O_3, Ta_2O_5 and others. However, there are several issues related with these high-κ dielectrics. They have poorer interfacial properties and thermal properties when compared to SiO_2. The dielectric/semiconductor interface is characterized by at least two-to-three orders of magnitude more interfacial traps and oxide traps than SiO_2, which act as centers for trapping electrons. During the gate voltage excursion, these traps dynamically charge and discharge and hence cause instability in the threshold voltage (V_{TH}) of devices.

One of the most extensively studied oxides on Si is HfO_2, owing to its low interfacial states density at the oxide/semiconductor interface, a very high dielectric constant (20-25) and a moderately wide band-gap (5.6-5.8 eV). Prior work on HfO_2 on Si and GaN-based devices can be found in Section 1.3 Schottky-contact HEMTs vs gated HEMTs.

A similar approach is applied to III-V semiconductor-based transistors. Several works have already been published on different experimental dielectrics, as enlisted in Section 1.3 Schottky-contact HEMTs vs gated HEMTs, in the search for a high-κ dielectric with desirable properties such as low oxygen vacancies and fixed charge, a relatively high thermal stability to withstand the high temperatures required for the Ohmic contact anneals, a good dielectric/semiconductor interface, and most importantly, a high breakdown field to withstand high blocking voltages of 1kV meant for developing next-generation high-power and high-voltage switching circuits.

2.2.1 ALD of high-κ dielectrics

Several deposition techniques have been studied in the recent past like MOCVD, MBE, RF Sputtering, PECVD, HDPCVD, ALD and others, all of which aim at faithful deposition of the dielectrics such that they have the least interfacial states density and fixed oxide charge. The most famous, however, out of all of these deposition methods is ALD. Extensive studies on the mechanisms of ALD have already been performed and it is a well-developed process.

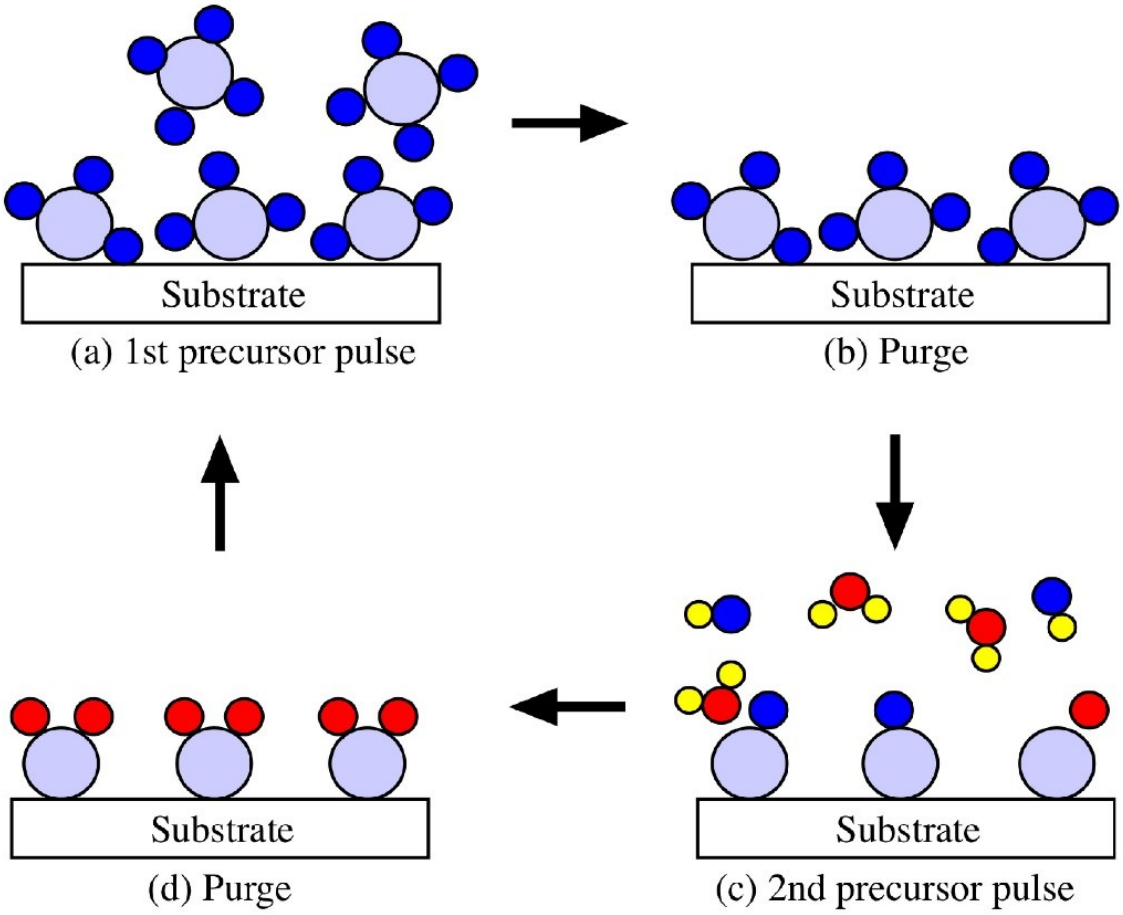


Figure 4. Schematic of ALD growth, reprinted from *Atomic Layer Deposition*, by Andrew R. Barron, July 2009, retrieved from http://cnx.org/contents/rimBK1xx@2/Atomic-Layer-Deposition. Copyright 2009 by Andrew R. Barron. [4]

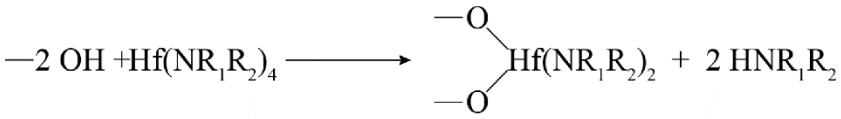
Realizing the potential for this deposition process, researchers and scientists are developing and synthesizing different organo-metallic compounds that can aid in the growth of alternative dielectrics using this process. It has been announced as the most preferred deposition process for growing high-κ dielectrics by the International Roadmap for Semiconductors (ITRS) [31].

ALD is a modified chemical vapor deposition system, which uses usually H_2O as the oxygen source in one cycle and organo-metallic compounds as the precursor for the metal component of the dielectric in the subsequent cycle to form the desired dielectric film on the substrate [31]. The surface of the substrate is activated by a chemical reaction in every cycle. The oxygen source, H_2O, causes termination of the surface with –OH groups which act as the reaction centers for the subsequent step. The most intriguing aspect of ALD is that it forms a saturated surface with –OH terminated bonds and no further reaction of the same species occurs. In other words, there is only one layer of –OH terminated surface formed. This is called the self-limiting growth property of the ALD. A purge step using either Argon or Nitrogen is usually performed after the first pulse. Moving on, in the next step, when the organo-metallic compound is introduced into the chamber, the –OH bonds break and react with the organo-metallic compounds to form the desired dielectric and some gaseous by-products which can be removed from the chamber by another purge step immediately after the introduction of the metal precursor. A schematic of the ALD process is shown in Fig 4 [4]. Note that the schematic only shows the concept behind the growth; the cartoon doesn't use any specific precursor structure. The above properties of the ALD growth process allows for extremely low temperatures of deposition to be attained. The thermal budget is important to be maintained. This attributes itself to the following reason. Usually, high-κ dielectrics are oxides of transition metals. These transition metals have a high affinity for oxygen and form oxides very easily.

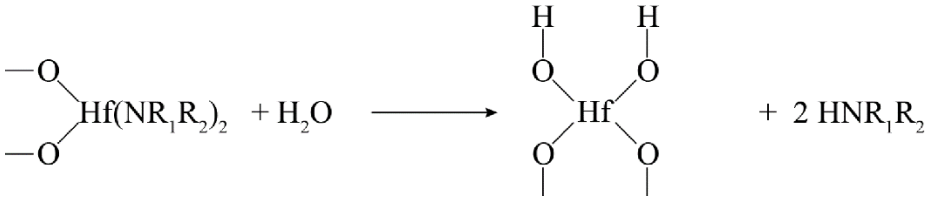
However, the transition metal oxides are easily crystallized at relatively low temperatures, which results in the formation of grain boundaries serving as percolation paths for leakage when a high transverse electric field is applied across the dielectric, ultimately leading to breakdown. Both of these properties are addressed by the ALD. Low temperature deposition is made possible by activating the surface chemically. Also, the low deposition temperature ensures the amorphous deposition of these transition metal oxides.

ALD growth of two of the most popular high-κ dielectrics, HfO_2 and Al_2O_3, have been studied extensively by the research fraternity. The organo-metallic precursors used for HfO_2 and Al_2O_3 are TEMAH and TMA respectively. A schematic of the possible chemical reaction for the growth of HfO_2 using H_2O can be summarized as follows:

Step 1: After introduction of TEMAH into the ALD chamber.

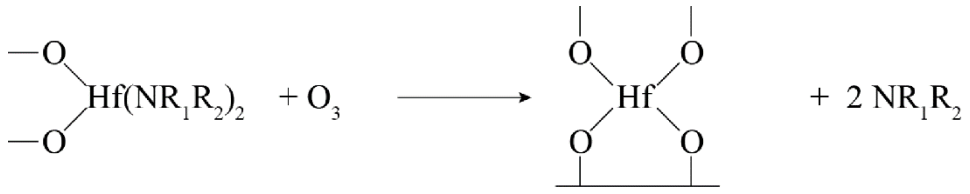


Step 2: After introduction of H_2O into the ALD chamber.

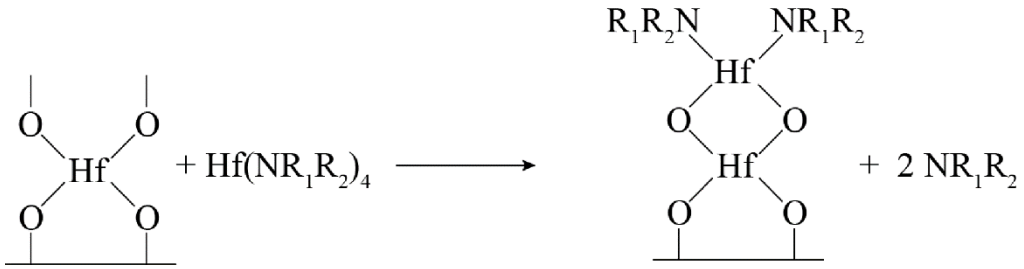


On the contrary, when using O_3 as an oxygen source, the following possible reactions can be summarized as follows:

Step 1: After introduction of O_3 into the ALD chamber.



Step 2: After introduction of TEMAH into the ALD chamber.



It was shown by T Kobu *et. al.* that compared to the Al_2O_3 film grown using H_2O as oxygen source, the film grown using O_3 features a decrease in H concentration and an increase in C concentration [27]. The above observation can be attributed to the highly reactive nature of O_3, which decomposes and forms more carbonates as compared to H_2O. On the other hand, the decrease in H concentration can be explained by the 'dehydration' or removal of the –OH groups from the surface which have long been thought to facilitate the formation of an interfacial layer at the oxide/semiconductor interface, which can act as the source of short-to-long duration traps and cause instability in the threshold voltage of the devices. It was also shown by Kim *et. al.* that the advantage of using O_3 as the oxygen source is it reduces the possibility of formation of Al-Al clusters which can serve as leakage paths degrading the quality of the film [26]. The reduction was attributed to the deficiency of oxygen when using H_2O as the source. Similar concepts can be applied to the deposition of HfO_2 using O_3. In this work, ALD has been used as the deposition process for HfO_2 using TEMAH as the metal

precursor and either H_2O or O_3 as the oxygen source on GaN/AlGaN/GaN and the interface properties thereof probed using chemical and electrical analysis techniques.

2.2.2 X-ray photoelectron spectroscopy (XPS)

As has already been discussed, the surface and the semiconductor/dielectric interface are essential for the study of reliability and performance of transistors. Over the years, many important surface analysis techniques have been developed which include the likes of time-of-flight secondary ion mass spectroscopy (TOF-SIMS), Auger electron spectroscopy (AES) and X-ray electron spectroscopy (XPS). Each tool has its own advantages and disadvantages. Out of these, XPS is the most sensitive chemical analysis tool that has been in use for quite some time. A brief background into the principle and working is discussed below.

XPS, also referred to as Electron Spectroscopy for Chemical Analysis (ECSA), is based on the photoelectric effect that was first explained successfully by Einstein, for which he was

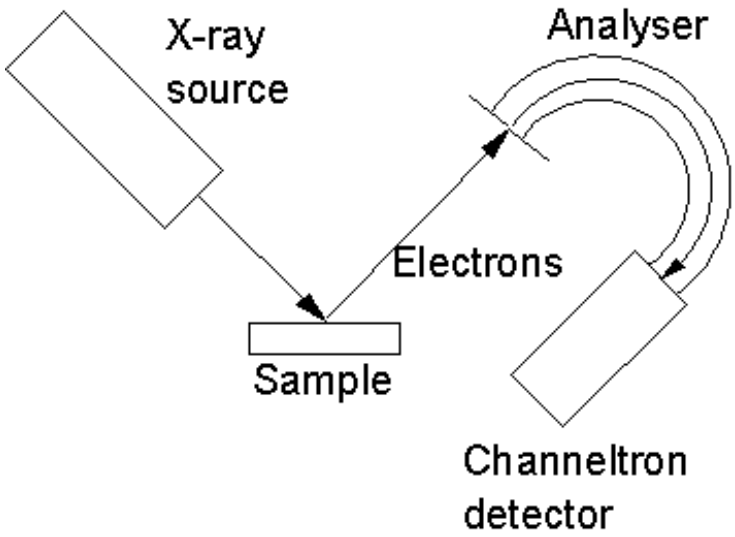


Figure 5. Schematic of an XPS system. Reprinted from *2. Film Analysis*, by James R Petherbridge, July 2002, retrieved from http://www.chm.bris.ac.uk/pt/diamond/jamespthesis/chapter2.htm. Copyright 2002 by James R Petherbridge. [2]

awarded the Nobel Prize in 1912. The sample under observation is subjected to a beam of photons of specific well-defined energies to energize the electrons bound in the atoms immediately below the surface of the sample (see Fig. 5) [2]. The monochromatic X-ray is formed by aiming a 10 keV electron gun at an Al or Mg target to produce Al K_α and Mg K_α X-rays, the spot size of the beam ranging from 20-200 μm. When the energy of the photons in the beam is almost equal to or larger than the binding energy of the electrons, the electrons are knocked off from the surface and collected by a detector. The kinetic energy (KE), binding energy (BE), the photon bean energy (E_{photon}) and the work function (ϕ) can be related as:

$$BE = E_{photon} - (\phi + KE) \tag{3}$$

Since the E_{photon} is known and the KE of the electron measured, the BE of the electrons can be measured by adjusting the ϕ, which is dependent on both the system and the material being analyzed. In a condensed matter, according to the band theory and Pauli's exclusion principle, all energy levels are quantized. Thus extracting the BE value from the XPS peaks can help study the presence of chemical species and their binding states. Even though it seems to be a qualitative technique, XPS can be used for quantitative analysis. The number of electrons knocked off from the surface in response to the photon beam is directly proportional to the number of atoms of the specific energy at the surface. Chemical stoichiometry can be estimated from the atomic concentration acquired from the data. However, it is sometimes challenging to produce results to the atomic concentrations. An essential parameter used to understand the chemical composition of the surface is full-width at half-maximum (FWHM). As a rule of thumb, broadening of the peak may indicate a change in the chemical bonding state. Sometimes broadening of the peak may also indicate a localized charging of the surface, which might be due to the continuous beam of photons hitting the surface.

A few disadvantages however make XPS a time-consuming and cumbersome analysis technique. There is no doubt about the potential of XPS producing almost precise data, but it comes at a price. Surface preparation is an important step for performing XPS. The background noise generated by electrons, with energy lesser than the measurement energy, can degrade faithful analysis of chemical species. Also, it is important that the XPS chamber be under ultra-high vacuum ($<10^{-9}$–10^{-10} Torr) such that the mean free path (λ) is essentially greater than the distance between the sample surface and the collector, to avoid collisions between residual chamber chemical species. The mean free path, λ, can be approximated by the following relation:

$$\lambda \approx \frac{5}{P\ (Torr)}\ cm \tag{4}$$

The XPS can be an excellent tool for chemical surface analysis for approximately 5–10 nm depth from the surface. The precision of the XPS has long served as a faithful tool for the study of surfaces.

2.3 Electrical characterization techniques and conductance method

Performance of gated transistors depends heavily on the quality of the interface between the dielectric and the semiconductor substrate. Interfacial quality depends on a lot of factors, including the density of interfacial states and the presence of any undesired interface, which can be a primary contributor of slow and/or fast traps, the dynamic charging and discharging of which can contribute further to the performance degradation of the transistors. The density and distribution of these interfacial and bulk dielectric traps can heavily alter the performance parameters and reliability of these transistors. For example, a high interfacial trap density, D_{it}, would result in a shift in the threshold voltage (V_{TH}) and hysteresis, exhibiting a memory effect. Therefore, it is imperative that test structures be developed and studied

thoroughly before these materials can be applied to the fabrication of transistors in the industry. MOS capacitors have been used for long as excellent test structures for the study of any semiconductor system owing to the simplicity of their fabrication, the absence of drain and source effects and the capability to study just the interface between the oxide and the semiconductor. As a matter of fact, it was rightly pointed out by Nicollian and Brews that a lot (about 20) of the properties about the MOS-system can be studied using MOSCaps [3]. Though most of the development of MOSCaps and the methods of studying the

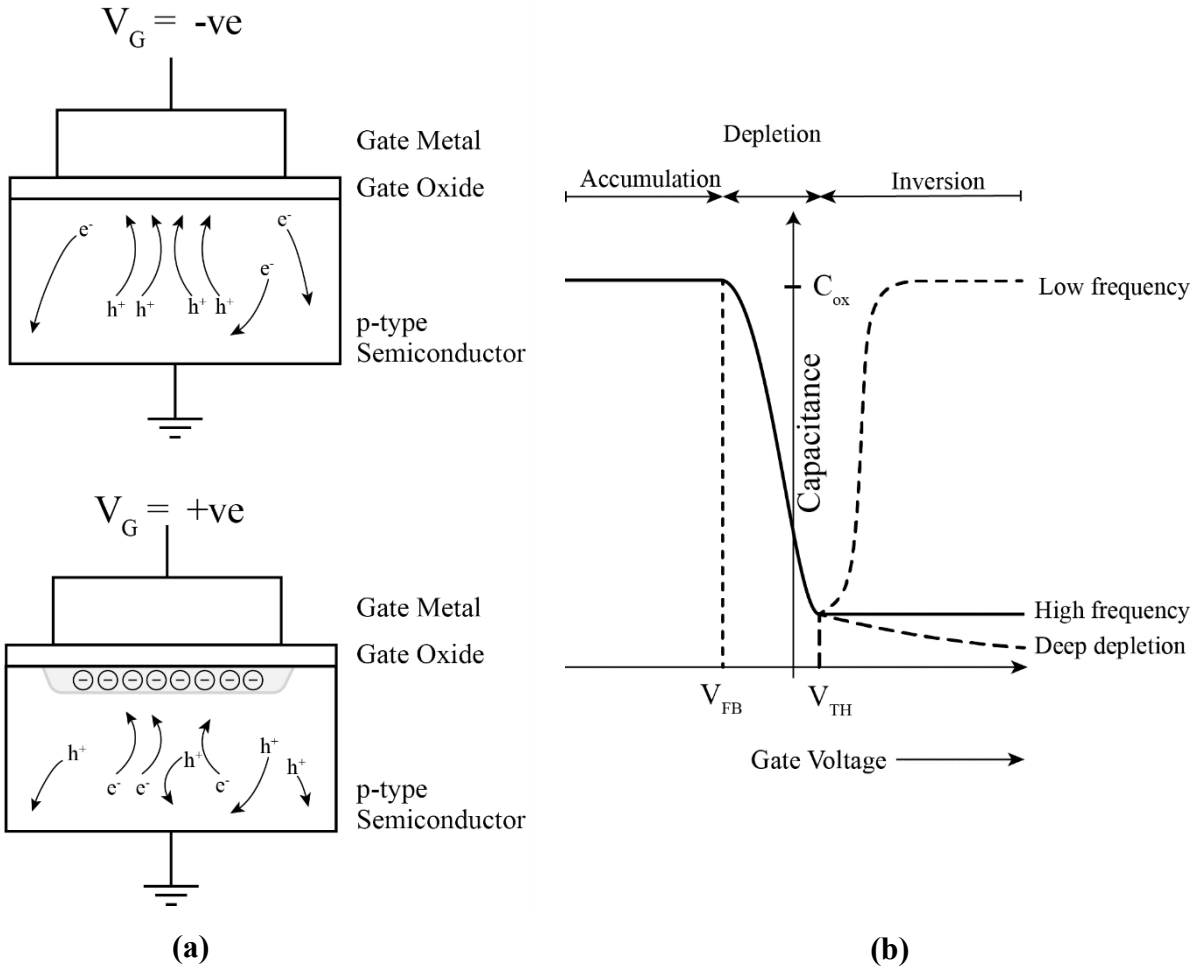


Figure 6. (a) Schematic of nMOSCap under accumulation (top) and inversion (bottom; grayed region shows the depletion region with immobile negative ions) (b) C-V characteristics of an ideal nMOS capacitor

insulator/semiconductor system was developed keeping SiO_2/Si in mind, most of the methods of analysis and modeling usually work for the newer insulator/semiconductor system with proper modifications and assumptions.

The capacitance-voltage and conductance-voltage measurement techniques have been the most famous electrical characterization techniques of all time. The oxides generally have a lot of defects such as interface traps owing to unsatisfied dangling bonds or due to the incompatibility between the oxide and the semiconductor substrate, fixed oxide charges, trapped charges in the oxide and oxide vacancies. All of these can be measured, with proper methodology, using the C-V and G-V technique. An MOS capacitor is essentially a structure comprising (from top-to-bottom) a gate metal, a gate oxide layer and a semiconductor substrate. Three regions of the C-V data extracted from an MOS capacitor are of immense aid for the systematic study of the MOS system – accumulation, depletion and inversion. Figure 6 shows an ideal C-V curve as expected from an n-type MOS (where the majority carriers are holes, i.e. p-doped substrate) capacitor with the different regions outlined. Figure 7 shows the contributions from different factors in an MOS system to capacitance, including interface traps (C_{it}), hole charge density (C_p), electron charge density (C_n), depletion region charge density (C_b) and oxide capacitance at strong accumulation (C_{ox}) due to majority carriers [1].

In accumulation at a negative voltage applied to the gate, a huge quantity of holes would gather at the dielectric/semiconductor interface. The admittance for C_p approaches a large number, which practically shorts it. Hence the only capacitance contribution in accumulation is due to C_{ox}, as shown in Fig. 7 (b) by the bold line.

Therefore, in accumulation,

$$C_{accumulation} = C_{oxide} \tag{5}$$

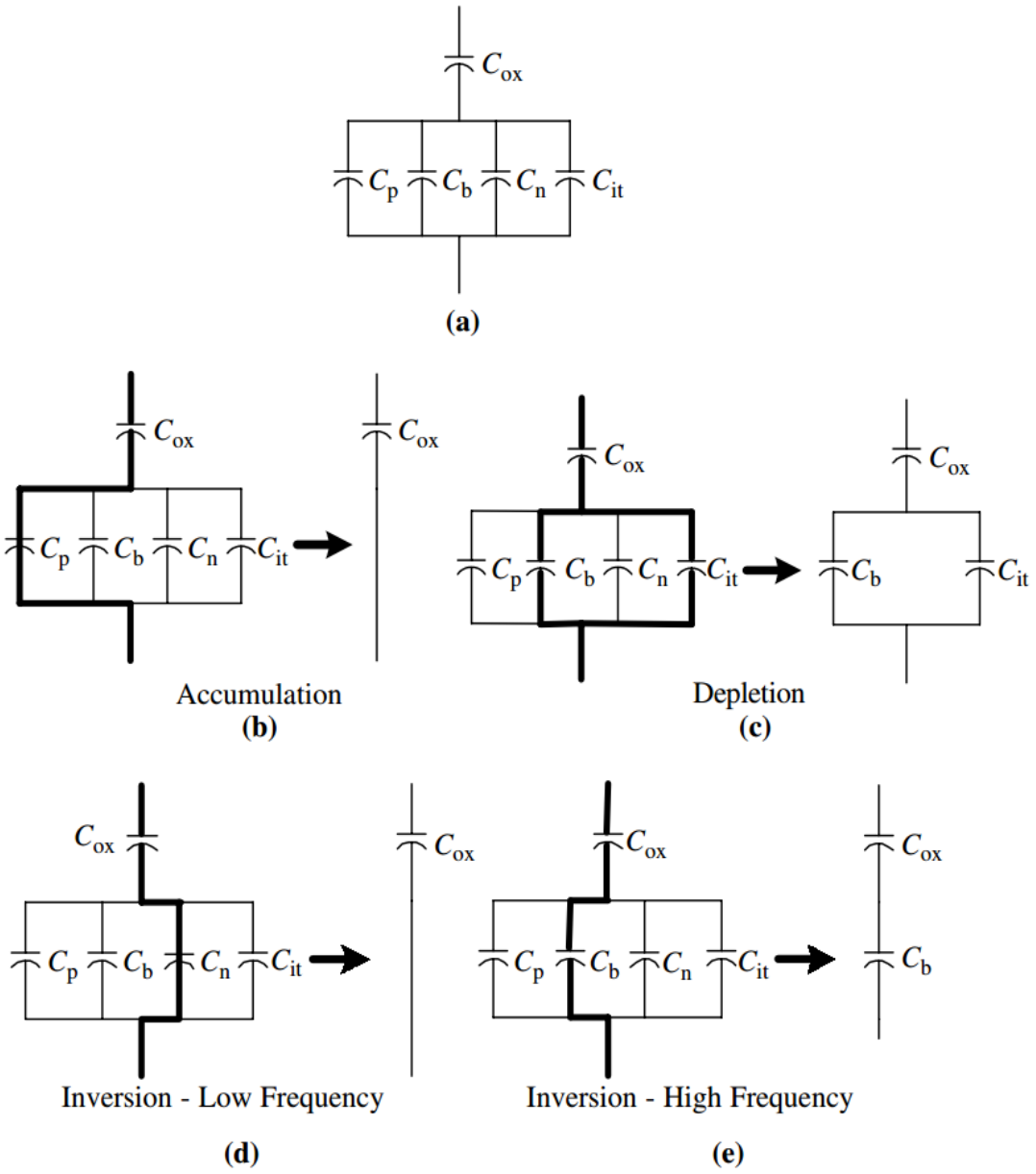


Figure 7. Contributions to capacitance of the n-MOS system during various stages of traversing the C-V curves. Reprinted from *Semiconductor material and device characterization* (p. 323), by D. Schroder, 2006, Hoboken, NJ: John Wiley & Sons, Inc. Copyright 2006 by John Wiley & Sons, Inc. [1]

As the gate voltage is increased slowly toward the positive bias, the holes are repelled by a transverse electric field that is set up in a direction from the gate to the substrate. The minority carriers, the electrons in this case, start getting attracted and the surface starts being

depleted of holes. A space-charge region, also called the depletion region, is developed near the surface by negatively charged immobile ions that have been ripped off of holes. The total charge contained in this region,

$$Q_b = -qN_A W_d \tag{6}$$

where, N_A is the number of immobile ions and W_d is the width of the depletion region.

Since this is a charged region, there would be contribution of capacitance, C_b, from this region. Not only that, any interface states or traps that might be present, will contribute to the capacitance, C_{it}, in parallel to C_b, and together in series with C_{ox}, as shown in Fig. 7 (c). Therefore, in depletion,

$$\frac{1}{C_{depletion}} = \frac{1}{C_{oxide}} + \frac{1}{C_{it} + C_b} \tag{7}$$

Further increase in the gate voltage causes an inversion in the type of carriers due to strong depletion of the holes and gathering of large quantity of electrons. Theoretically, this happens when the band bending causes the Fermi energy level (E_F) to go below the intrinsic Fermi level (E_{Fi}) and creates a 'well' for minority carriers to dwell and interact with the gate voltage at the surface. This process is known as 'inversion' and the MOS system works on the principle of formation of this inversion layer, which essentially acts like a channel. The depletion region reaches a maximum width, $W_{d\,(max)}$, which can be related as:

$$W_{d_{max}} = \sqrt{\frac{4\varepsilon\phi_b}{qN_A}} \tag{8}$$

where, ε is relative permittivity of the substrate, ϕ_b is the total band bending at inversion and N_A is the number of immobile acceptor ions.

The voltage at which inversion occurs is known as threshold voltage, V_{TH}, and is related to the total charge carried by the minority carriers as:

$$Q_{inversion} = -C_{ox}(V_G - V_{TH}) \quad (9)$$

Beyond this point, if V_G is further increased, there is not much appreciable change in the $Q_{inversion}$ or $W_{d(max)}$. In this region of operation, there are two possible outcomes. If the measurement of frequency of the AC signal has a time constant larger than or almost equal to that of the time constant of the $Q_{inversion}$ modulating (slightly expanding and contracting) $W_{depletion}$, then the surface charge is able to follow the AC signal and thereby contribute to equivalent capacitance. Otherwise, there is almost no additional capacitance contribution and it is this value of capacitance that is the final capacitance in this region of operation. The above two cases have been shown in Fig. 6 as low-frequency and high-frequency curves respectively. Similar considerations can be made for capacitors developed on the III-V semiconductor system. Since III-V semiconductor systems are always on due to the presence of the 2DEG, V_{TH} essentially refers to the voltage where the channel made by the 2DEG is cut off.

The ideal C-V curves are often a dream and seldom are these achieved even with the state-of-the-art technological tools and equipment. In nature, every other material is filled with impurities and defects, which alter the true characteristics of the material. In the semiconductor industry and research family, it has always been the ultimate goal and challenge to reduce the defect levels to the minimum achievable, for better device performance and reliability. A few of the defects that alter and degrade semiconductor device performance and pose a threat to reliability include fixed oxide charge (Q_f), oxide trapped charges (Q_{OT}) and interface trapped charges (Q_{it}). A brief description of the just mentioned defects have been touched upon before moving on to the effect these have on transistor performance and the methods to measure them.

Fixed oxide charges (Q_f) lend their origin to the process of deposition of the dielectric. It has been shown that a higher temperature of growth or an anneal at an elevated temperature can cause annihilation of these fixed charges. These are positive charged centers and do not exhibit any electrical characteristics. On the contrary, in ultra-thin oxides, trapped oxide

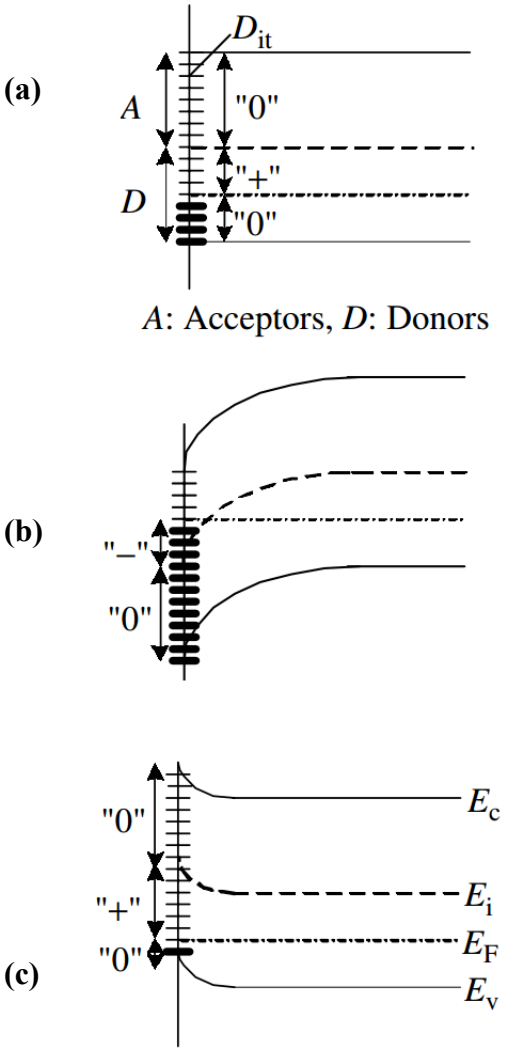


Figure 8. Band diagram showing effect of interface states. Reprinted from *Semiconductor material and device characterization* (p. 343), by D. Schroder, 2006, Hoboken, NJ: John Wiley & Sons, Inc. Copyright 2006 by John Wiley & Sons, Inc. [1]

charges can be present. They appear in the dielectric mainly after initiation of leakage, especially by Fowler-Nordheim tunneling, because the electrons or holes might lose energy after entering the dielectric and thereby rest inside the dielectric.

Interfacial defects state density (D_{it}) are defects located at the semiconductor/dielectric interface. These can either be positive or negative, which mainly arise due to incompatibility between the substrate and the dielectric, defects due to structural differences between them, impurities that might be deposited or adsorbed during the dielectric deposition process or due to dangling bonds at the termination of the underlying surface that might not be satisfied during the deposition process. They are active centers for charge trapping when an electrical field is applied across them. They can either charge or discharge, i.e. trap and emit carriers during a sweep of the gate voltage. These are termed 'fast charges' due to their ability to charge and discharge fast compared to the other types of dielectric defects, namely fixed charges and oxide trapped charges. The charge possessed by these defects (Q_{it}) can be equated from the slope of the C-V curves. The interface charges can have deleterious effect on the threshold voltage of transistors and thereby affect the reliability of transistors. A model predicts the nature of these interface states or traps as shown in Fig. 8 [1, 32]. Fig. 8 (a) shows the condition in which case $V_G = 0$ V. All states below E_F would be occupied by electrons and hence, neutral. However, states above E_F till E_i would be unoccupied donors and hence exhibit a positive charge; beyond E_i no states are occupied and hence they are neutral acceptors. Fig. 8 (b) shows the condition where $V_G > 0$V, in which case, the E_F is above E_i near the interface, which causes the states in the energy region ($E_F - E_i$) to be occupied acceptors and hence they exhibit a negative charge at flat-band condition. Finally, in Fig. 8 (c), for $V_G < 0$V, unoccupied donors up to E_i exhibit a positive charge, while unoccupied acceptors above E_i exhibit no residual charge.

These traps can be quantified by high and low-frequency C-V measurements. They can respond to the AC signal if the frequency of measurement is low and comparable to their time constants and they can capture carriers as well as emit carriers, thereby working as trapping centers. This phenomenon of trapping introduces reliability issues in semiconductors by causing shifts in V_{TH}. At relatively higher frequencies of measurement, these traps are unable to follow the AC signal due to the swing time constant of the measurement voltage being quicker than that of the traps time constants, τ_{it}. However, these traps can follow the slowly varying DC voltage and causes a stretching of the C-V curve in the transition region from

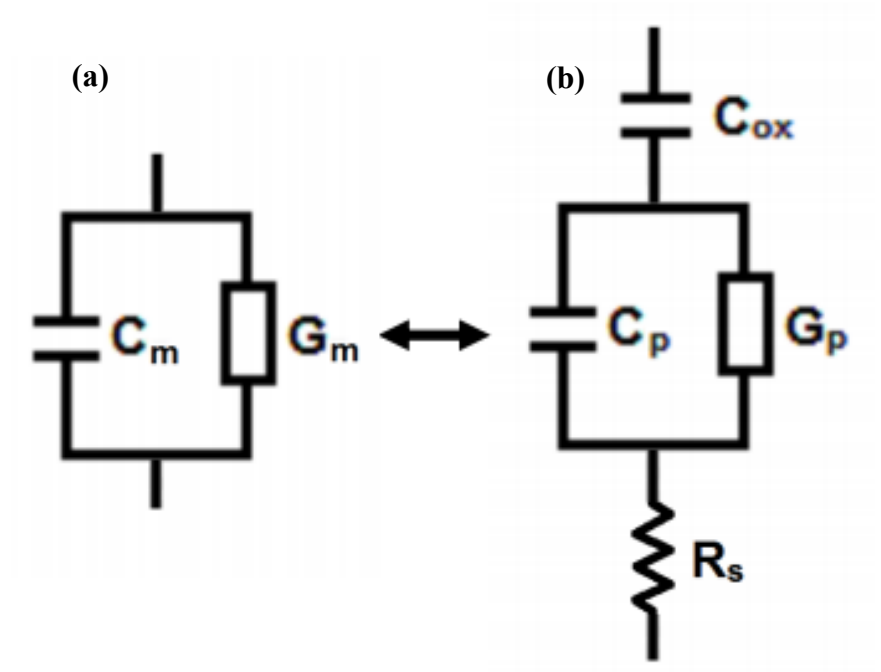


Figure 9. (a) Circuit configuration as measured by the LCR meter. (b) Equivalent circuit configuration as suggested by Nicollian and Brews for the measurement of interface traps. Reprinted from *MOS (Metal Oxide Semiconductor) Physics and Technology* (p. 212), by E.H. Nicollian and J.R. Brews, 1982, Murray Hill, NJ: John Wiley and Sons. Copyright 1982 by Bell Laboratories, Incorporated. [3]

accumulation to inversion, called "C-V stretch-out". The residual charge on these traps contribute a capacitance to the accumulation capacitance (C_{acc}) (see Eqn. 10).

These traps can be quantified by making capacitance and conductance measurements using the LCR meter, which assumes the circuit configuration as shown in Fig. 9 (a) and an equivalent circuit configuration for the measurement of traps was proposed by Nicollian and Brews [3], because some correction needs to be applied to the measurement due to the loss of signal by the frequency-dependent trapping. Also, the parasitic series resistance, R_S, plays a part in signal loss before being picked up by the LCR meter. This causes an anomaly in the measurement of the actual oxide capacitance, C_{ox} and underestimation of the interface states density. The following equations were proposed by Nicollian and Brews for the correction of R_S and C_{ox}:

$$R_S = \frac{Gma}{\left((Gma^2) + ((\omega)^2 * Cma^2)\right)} \tag{10}$$

and

$$Cox = Cma * \left(1 + \left(\frac{Gma}{\omega * Cma}\right)^2\right) \tag{11}$$

where $C_{m,a}$ and $G_{m,a}$ respectively are the capacitance and conductance measured in strong accumulation and ω is the angular frequency of measurement. The equivalent and corrected parallel conductance, G_p, can then be related in terms of C_{ox}, R_S, C_m, G_m and ω as shown in the following equation:

$$\frac{G_p}{\omega} = \frac{-\omega^2 {C_{ox}}^2 ({R_s {C_m}^2 \omega^2 + R_s {G_m}^2 - G_m})}{\omega^4 {C_{ox}}^2 {C_m}^2 {R_s}^2 + \omega^2 ({C_{ox}}^2 {R_s}^2 {G_m}^2 + {C_m}^2 + {C_{ox}}^2 - 2{C_{ox}}^2 R_s G_m - 2C_m C_{ox)} + {G_m}^2} \tag{12}$$

To quantify the frequency-dependent traps, the maximum value of $\frac{G_p}{\omega}$ is related to the trap density as follows:

$$D_{it} \approx \frac{2.5}{qA} * \left(\frac{G_p}{\omega}\right)_{max} \tag{13}$$

where 'A' is the effective capacitor area and 'q' is the electronic charge. The most famous technique developed by Nicollian and Goetzberger in their paper in 1967 is the "conductance method" [33]. For the conductance method to be able to measure the traps accurately, the measurements need to be taken over a wide frequency range, especially toward the lower frequency range, because the interface traps lose activity on the high frequency range and the conductance method is a direct method of measuring the conductance of the traps. It is one of the most sensitive methods of quantifying traps and can be used to determine trap quantity in the depletion and weak inversion regions along with their time constants and their distribution.

The conductance method is one of the most direct and sensitive methods of detecting trap density at the interface. Using the electrical equivalent circuit shown in Fig. 9 as proposed by Nicollian and Brews for the measurement of interface trap density, the parallel conductance component G_P can be calculated by the following relation:

$$\frac{\langle G_P \rangle}{\omega} = \frac{\omega {C_{ox}}^2 G_c}{{G_c}^2 + \omega^2 (C_{ox} - C_c)^2} \tag{14}$$

after correcting C_m and G_m, taking into account R_S and C_{ox} correction, where,

$$C_c = \frac{(Gm^2 + \omega^2 * Cm^2)Cm}{a^2 + \omega^2 * Cm^2} \tag{15}$$

and

$$G_c = \frac{(Gm^2 + \omega^2 * Cm^2)a}{a^2 + \omega^2 * Cm^2} \tag{16}$$

and

$$a = Gm - (Gm^2 + w^2 * Cm^2) * Rs \tag{17}$$

Then, the normalized $\frac{\langle G_P \rangle}{\omega}$ is plotted versus ω and D_{it} and τ_{it} are extracted by fitting the experimental data to the following models.

For single trap density model:

$$\frac{\langle G_P \rangle}{\omega} = \frac{qD_{it}\omega\tau_{it}}{1 + (\omega\tau_{it})^2} \tag{18}$$

For a continuum of states density model:

$$\frac{\langle G_P \rangle}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} * \ln\left(1 + (\omega\tau_{it})^2\right) \tag{19}$$

3. FABRICATION OF BASELINE MOSCAPS ON SILICON

3.1 Device structure

The top-view and cross-section of the baseline MOSCaps developed on n-type Si is shown in Fig. 10. The fabrication comprises the following modules – field dielectric module,

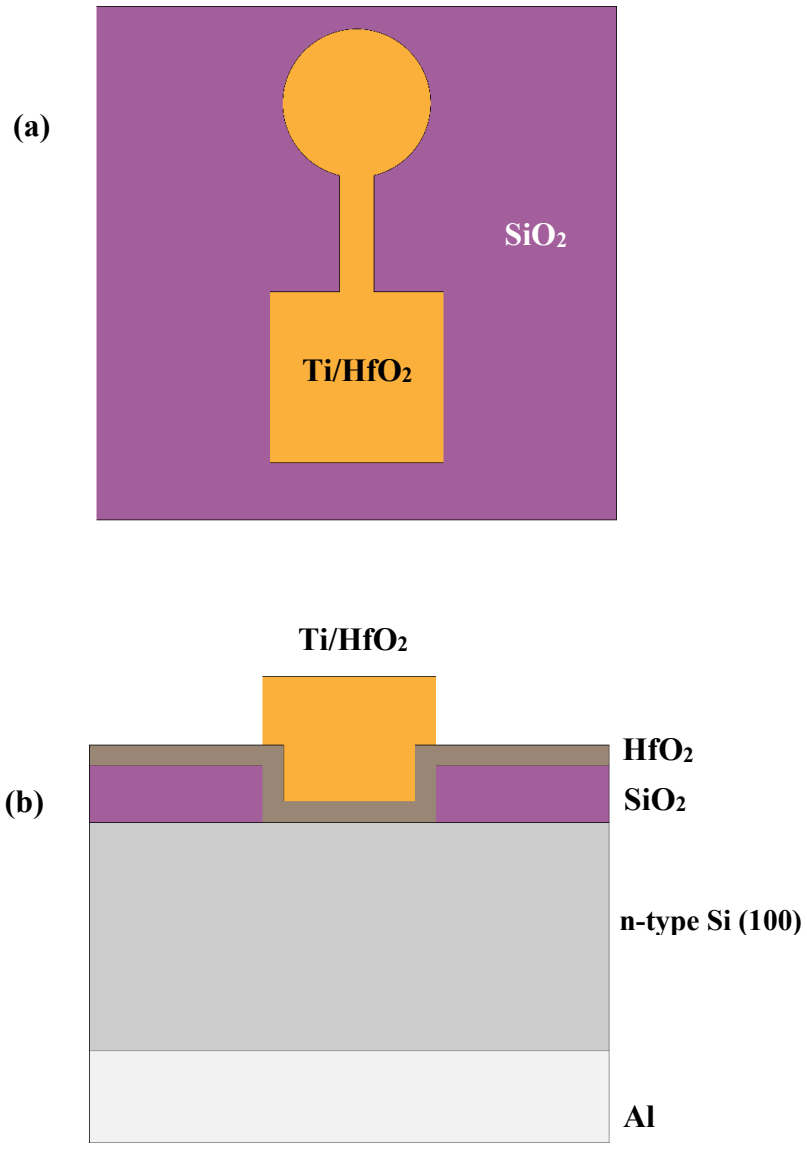


Figure 10. (a) Top-view and (b) cross-section of baseline MOSCaps developed on Si

gate stack module and finally the back contact module. The following sub-sections deal with the fabrication challenges and procedures.

3.2 Field dielectric module

The field dielectric module consists of the initial cleaning of wafers and field dielectric deposition for isolation. The process began with degreasing the wafer samples in Acetone, IPA and DI water for 1min each. Then, the wafer samples were treated with Piranha (H_2SO_4:H_2O_2 3:1) for 10min. Piranha solution is highly oxidizing and is used directly on the bare silicon wafer samples to clean organic and metal contaminants. After the Piranha treatment, the wafers are cleaned in running DI water for 2mins. Then, the wafers were dipped in an HF solution (1:20 HF: DI water) for 2mins to remove the poor quality interfacial oxide (SiO_2) that forms when the bare silicon surface is exposed to ambient air. This interfacial oxide layer usually reaches up to 5 Å in thickness and contains traps that act as charge trapping centers which contribute to leakage current. Complete removal of this layer is important for reliability of devices to be formed subsequently.

Following the HF solution treatment, the wafers were washed in running DI water for 2mins and blown dry using N_2 gun. Silicon is hydrophilic whereas SiO_2 is hydrophobic. The water droplets form beads on the surface of the wafers following the HF solution treatment, which is indicative of the fact that the SiO_2 layer has been removed.

A dehydration bake was performed on these wafers for 5mins in a dehydration oven set at 135°C, before transferring them to the PECVD chamber for deposition of the field dielectric. This step is necessary to keep the bare silicon wafers from being exposed to the ambient moisture.

PECVD employs a plasma to deposit thin films of various materials, depending on the introduced reactant gases, on the substrates at a temperature lower than that required for the conventional CVD system. The reactant gases are introduced into the chamber which has two parallel electrodes – an RF-energized electrode and a ground or charged electrode, in which case the potential applied on the bottom electrode is lesser than the RF-energized electrode. The plasma is formed in the chamber by the capacitive coupling of the electrodes (depending on the potential difference between the electrodes) and this in turn creates free electrons which excites the reactant gases, thereby dissociating them through a series of chemical reaction. The dissociated species, radicals, reach the surface of the substrate and through a chemical reaction, bond to the surface. The volatile species formed (if any) are removed from the chamber through exhaust.

An Oxford PlasmaPro 80 PECVD system was employed in this process flow to deposit a 600nm thick field-SiO_2 to provide isolation between devices formed on the same die. The process parameters were as follows: SiH_4/N_2 at 425 Sccm, N_2O at 355 Sccm, 350°C, 1000mTorr. The resulting field dielectric had a refractive index of 1.47, as measured by an Ocean Optics NanoCalc interferometer, which is very close to the ideal RI of 1.46 for SiO_2.

3.3 Gate stack module

After the previous module, the cleaned silicon wafers had a 600nm thick SiO_2 to provide good isolation between devices fabricated on the same die. The gate window module consists of lithography to pattern and etch the field dielectric. The next step was deposition of the gate dielectric using ALD, followed by a PDA in FG. Subsequently, the gate metal was deposited by DC Sputter technique, followed by patterning by lithography.

Lithography lies at the heart of the semiconductor industry, which is essentially a combination of two phrases; “litho” means light and “graph” means “drawing”. Lithography is essentially a process in which light is used to alter the chemical properties of a compound, usually a polymer, to transfer the desired pattern from the mask on to the wafer. The polymer used is called Photoresist (PR), and depending on the type of PR, different results are obtained after exposure to light. If a PR on exposure to light becomes soluble, it is called Positive PR. Conversely, when a PR on exposure to light becomes insoluble, it is called a Negative PR. Negative PR was the first PR to be developed and it did reign the semiconductor industry for quite a while. However, with advancements in materials processing, Positive PR became famous due to sharper and more reliable pattern transfer. The disadvantage of negative PR stems from the fact that on performing the soft bake, the negative PR swells up at the edges of the pattern transfer, which causes low resolution pattern transfer. Lithography was performed to open windows to the dielectric layer. Wet etch was performed using BOE to etch the field SiO_2. An etch rate of 150 nm/min was observed and the etch was done for 4:15 mins to make sure all the residual SiO_2 was gone, before transferring the wafers to the ALD chamber.

HfO_2 was deposited by a Cambridge NanoTech Savannah 100 Atomic Layer Deposition System using H_2O as oxygen source for the baseline MOSCaps. The purge gas used was N_2 at a flow rate of 20 Sccm with a chamber pressure of 200 mTorr. In the first pulse, the oxygen source H_2O was introduced into the chamber and in the second pulse, the metal precursor TEMAH was introduced into the chamber, with 10 secs and 15 secs of N_2 purge respectively after the precursor pulse. The deposition was done for 50 cycles. To confirm the grown thickness, a control Si sample was cleaned and put inside the ALD chamber alongside

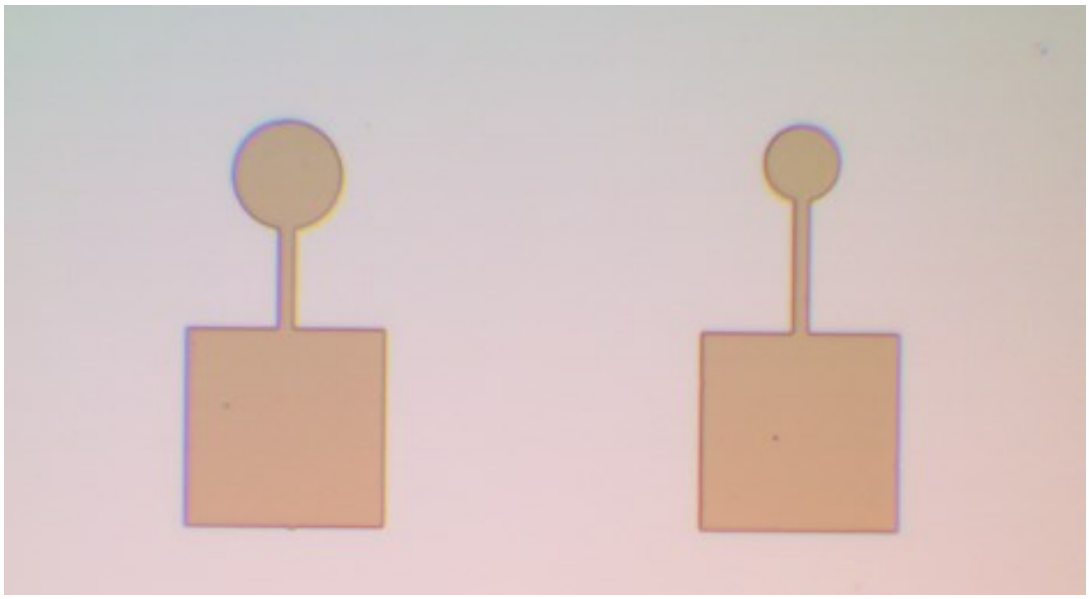


Figure 11. Micrograph of the final structure of MOSCaps with gate diameter of 100 µm (left) and 80 µm (right)

the actual sample. To measure the thickness, the ellipsometer was configured to use an ideal model for HfO_2, i.e. not taking into account any interfacial oxide that might be present at the oxide/silicon interface. The thickness was confirmed to be 5 nm ± 0.2 nm. With the model including an interfacial layer, i.e. HfO_2/SiO_2, the thickness was confirmed to be 4.9 nm/ 0.4 nm ± 0.2 nm.

Immediately after retrieving the samples from the ALD chamber, the samples were annealed in FG for a duration of 20min at 475°C. A PDA of high-k dielectrics on Si has been shown to reduce the interface states and therefore enhance leakage performance parameters [34]. After annealing the samples, the focus shifted to the deposition of the gate metal. A 100 nm thick Ti film was deposited using DC Sputter. The process pressure was 5×10^{-6} Torr to enable a good film with the least contamination, especially Ar, which can affect the Schottky junction, thereby resulting in a shift in the threshold voltage.

The gate metal was patterned by lithography, followed by a wet etch in BOE for 40secs (etch rate ~ 160nm/min). An additional 5sec dip in BOE was done to ensure complete removal of the gate metal from the non-patterned regions. This precautionary step was taken so that the gate metal is not of a larger effective area than the one used for calculations of C_{ox}. The final device structure is shown in Fig. 11.

3.4 Back contact module

Once the gate stack module was accomplished, back contact was made to the substrate. The back contact included coating the front surface of the wafer with photoresist, etching with BOE and finally deposition of 100nm of Al using DC Sputter technique. First of all, photoresist was spun on the top surface of the wafer (the side which had the MOSCaps). A hard-bake for 10mins was done to ensure the integrity and resilience of the photoresist during the next etch step. The wafer was immersed in BOE for 2mins to ensure complete removal of the native oxide that might have formed during the process flow. Immediately after this step, the wafers were transferred to the DC Sputter chamber. The process pressure was again 5×10^{-6} Torr and a 100nm thick Al layer was deposited.

3.5 Electrical characterization

After completion of the modules, electrical measurements were done on the developed MOSCap structures in the form of capacitance- and conductance-voltage measurements and leakage current density. C-V and G-V measurements were done using an Agilent E4980A precision LCR meter in parallel mode (C_P-G_P) of measurement with a step size of 0.1 V and a superimposed AC voltage of 20 mV on the gate voltage bias, which was swept from -2V → 1V. The I-V characteristics (leakage current density) measurements were done using an HP 4155B semiconductor parameter analyzer. All measurements mentioned here were done in the dark and at room temperature.

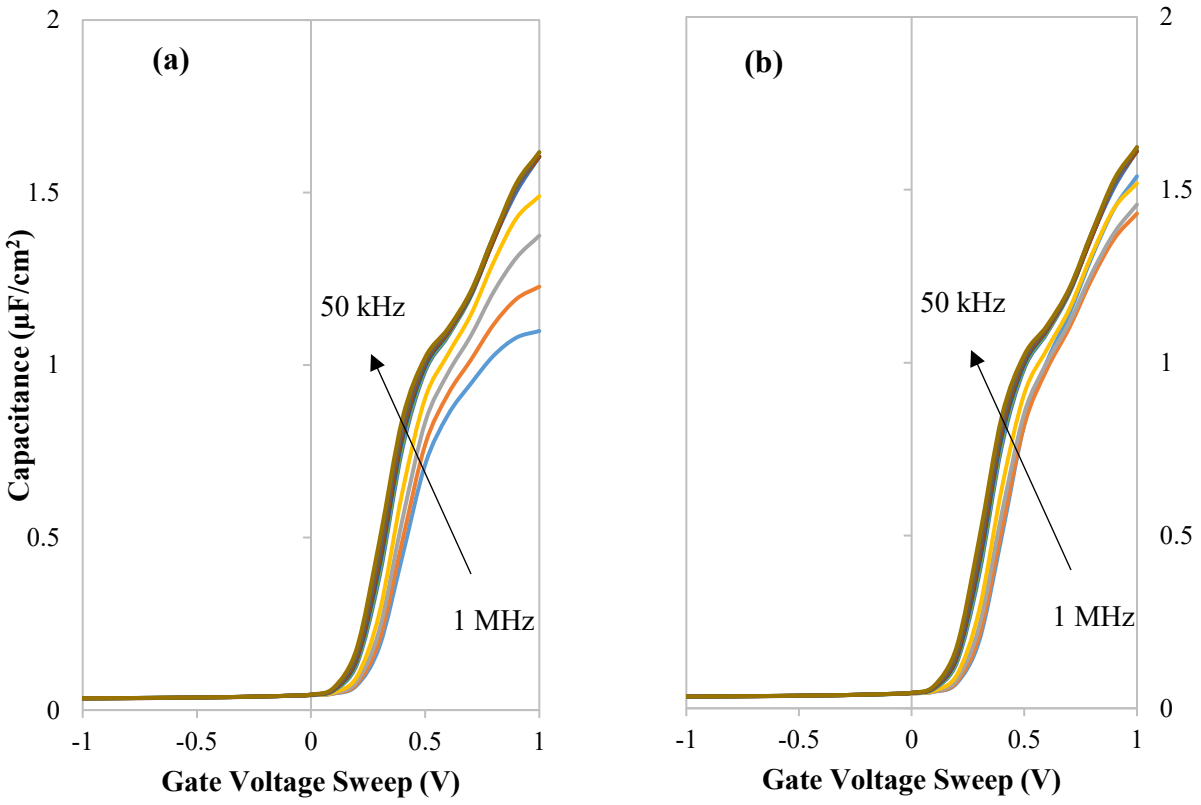


Figure 12. Measured capacitance-voltage characteristics (a) without and (b) with R_s correction

Figure 12 shows the capacitance-voltage characteristics of the developed MOSCap structures, measured from inversion to accumulation. Fig. 12 (a) shows the as-measured capacitance-voltage characteristics, which includes the effect of series resistance, R_s. The series resistance could be due to various factors, the major ones being the substrate resistance, the resistance of the probes and the resistance of the wires, which can cloud the actual measured capacitance and conductance due to the traps. The series resistance causes the wide frequency dispersion seen in the case of the uncorrected capacitance curves in the accumulation region. The R_S-corrected capacitance-voltage characteristics are shown in Fig. 12 (b). Comparing the two, the frequency dispersion in the accumulation region is, if not completely, greatly reduced. There is however a negative shift in the flat-band voltage with frequency and a negative shift as well in the threshold voltage, V_{TH}. The frequency-dependent shift can be explained by the presence of interface traps at the HfO_2/Si interface that can contribute to capacitance. When the AC signal applied to the gate voltage is oscillating at a frequency at which the traps can dynamically charge and discharge, these traps contribute to capacitance as well as conductance. The energy losses associated with the capture and emission of electrons by these traps are lost to or gained from phonons, ultimately leading to heating the lattice. A high interfacial trap density, D_{it}, causes a significant contribution to the capacitance (C_{it}) observed at depletion, and it can be equated as an equivalent series capacitance as:

$$\frac{1}{\boldsymbol{C}_{total}} = \frac{1}{\boldsymbol{C}_{oxide}} + \frac{1}{\boldsymbol{C}_{D_{it}} + C_{Depletion}} \tag{20}$$

If the frequency of measurement is higher than the time constant τ_{it} for these traps, then they are not able to follow the AC signal and hence their contribution to capacitance is reduced to a minimum. Figure 12 (b) shows a characteristic hump around the V_G = 0.5V, which is

indicative of a large number of interface traps. As explained above, the contribution of these traps to capacitance can be seen to decrease as the frequency of measurement increases.

The most sensitive parameter to understand the trap activity is the parallel conductance, G_P, which detects the AC signal loss due to the electrical activity of these traps. Series resistance can seriously hamper the determination of this signal loss thereby preventing the faithful detection of D_{it}. Usually local peaks indicate the dynamic capture and emission of traps. Only when the frequency of measurement and the time constant of the specific trap will match i.e. only when

$$\omega \tau_{it} = 1 \tag{21}$$

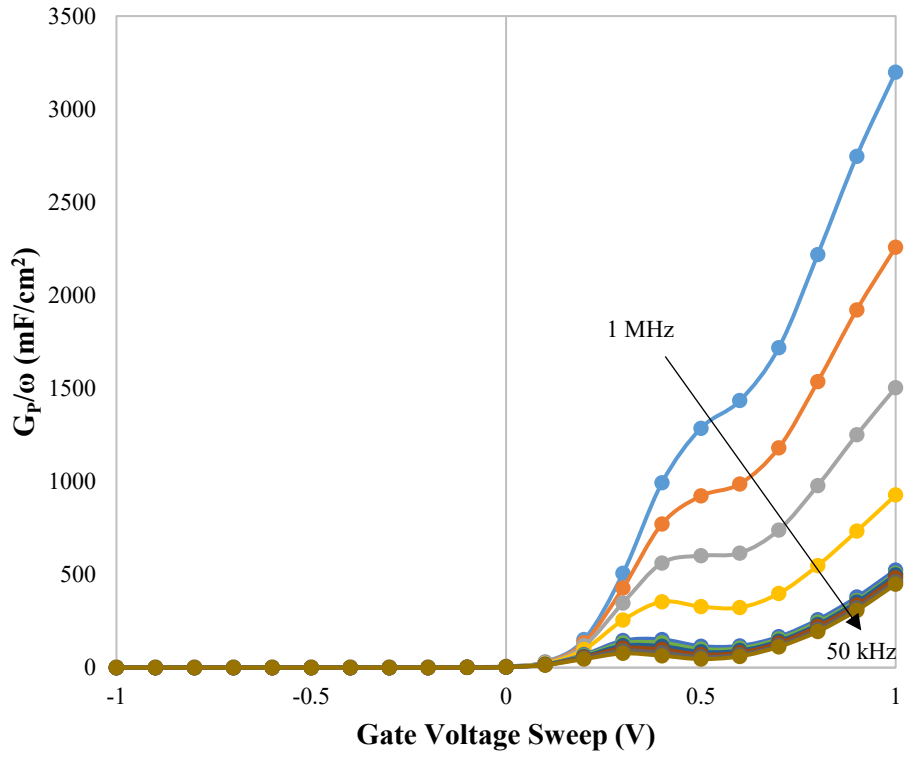


Figure 13. R_S-corrected normalized conductance G_P/ω plot for the developed MOSCaps

the contribution to conductance will be highest; on either side, i.e. when $\omega\tau_{it} < 1$ or $\omega\tau_{it} > 1$, there will be less contribution to conductance, hence a peak is supposed to be seen.

Figure 13 shows the series-resistance corrected normalized G_P/ω curves for the MOSCaps. There is evidence of a peak around $V_G = 0.5V$, which keeps on shifting to the negative voltage regime with decrease in frequency. This peak indicates the bias for the maximum activity of the interface traps at that particular frequency. The experimental G_P/ω vs frequency plots were used to extract the interface states density (D_{it}) and the trap time constants (τ_{it}) using the single state trap fitting equation. Figure 14 shows the density of interface states extracted at various gate bias voltages. There is a peak at $V_G = 0.5V$ – this is the bias at which the Fermi level lines up with the interface trap states and hence there is maximum activity of

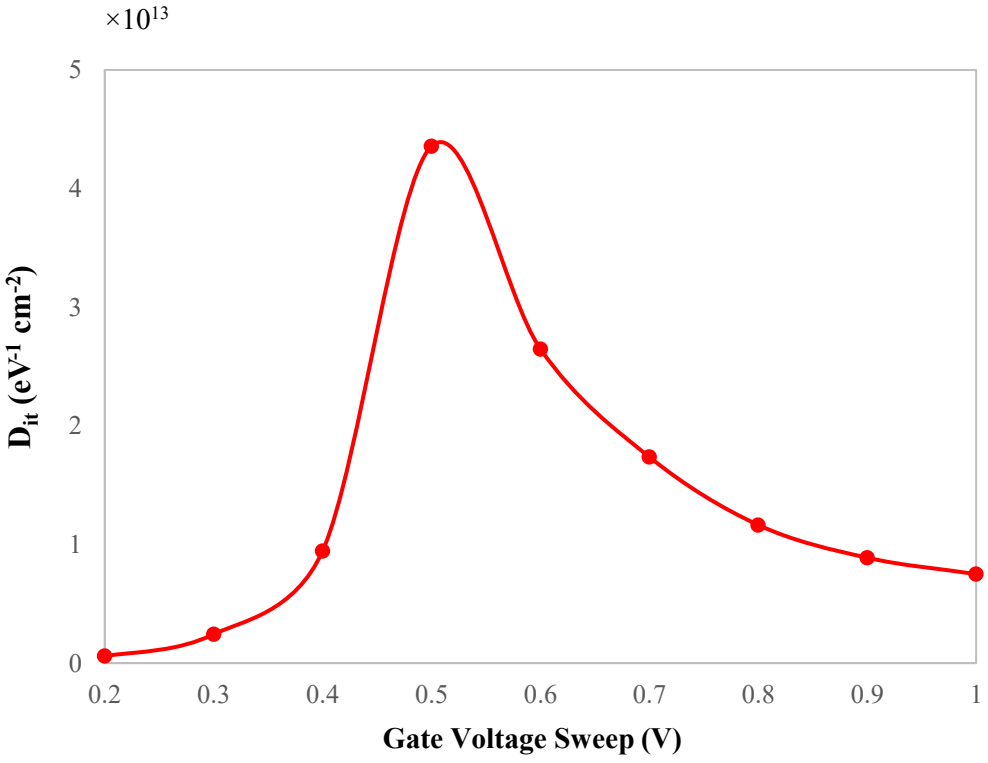


Figure 14. Extracted D_{it} vs. gate voltage

these traps. On either side of this bias, there is a decrease in the density of these traps. A maximum states density of 4.35×10^{13} $eV^{-1}.cm^{-2}$ was extracted.

Leakage current measurements were also done on other devices on the same wafer. Figure 15 shows the leakage current characteristics of the baseline MOSCaps. There is excellent leakage suppression by the dielectric under inversion. On the positive gate voltage side, there is almost a linear increase in the gate leakage current which could be due to direct tunneling of carriers through the dielectric. It is possible that the annealing at 475°C caused partial crystallization of the dielectric film. Grain boundaries are known to be deleterious for gate leakage because they act as percolation paths for carriers and increase leakage, with large grain boundaries causing more leakage [35]. A comparison was not made to the leakage current of a non-annealed sample, hence the exact phenomenon causing such a large leakage current cannot be ascertained.

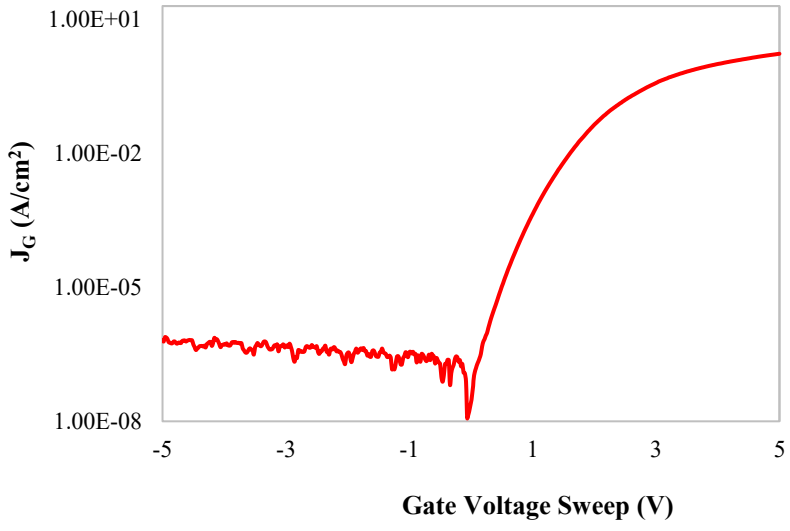


Figure 15. Leakage characteristics of Ti/HfO_2/Si circular MOSCap structures with a diameter of 100µm

4. FABRICATION OF MOSCAPS ON GAN/ALGAN/GAN HETEROSTRUCTURE

4.1 Device structure

The top-view and cross-section of the MOSCaps developed on GaN/AlGaN/GaN heterostructure is shown in Fig. 16 (a) and (b) respectively.

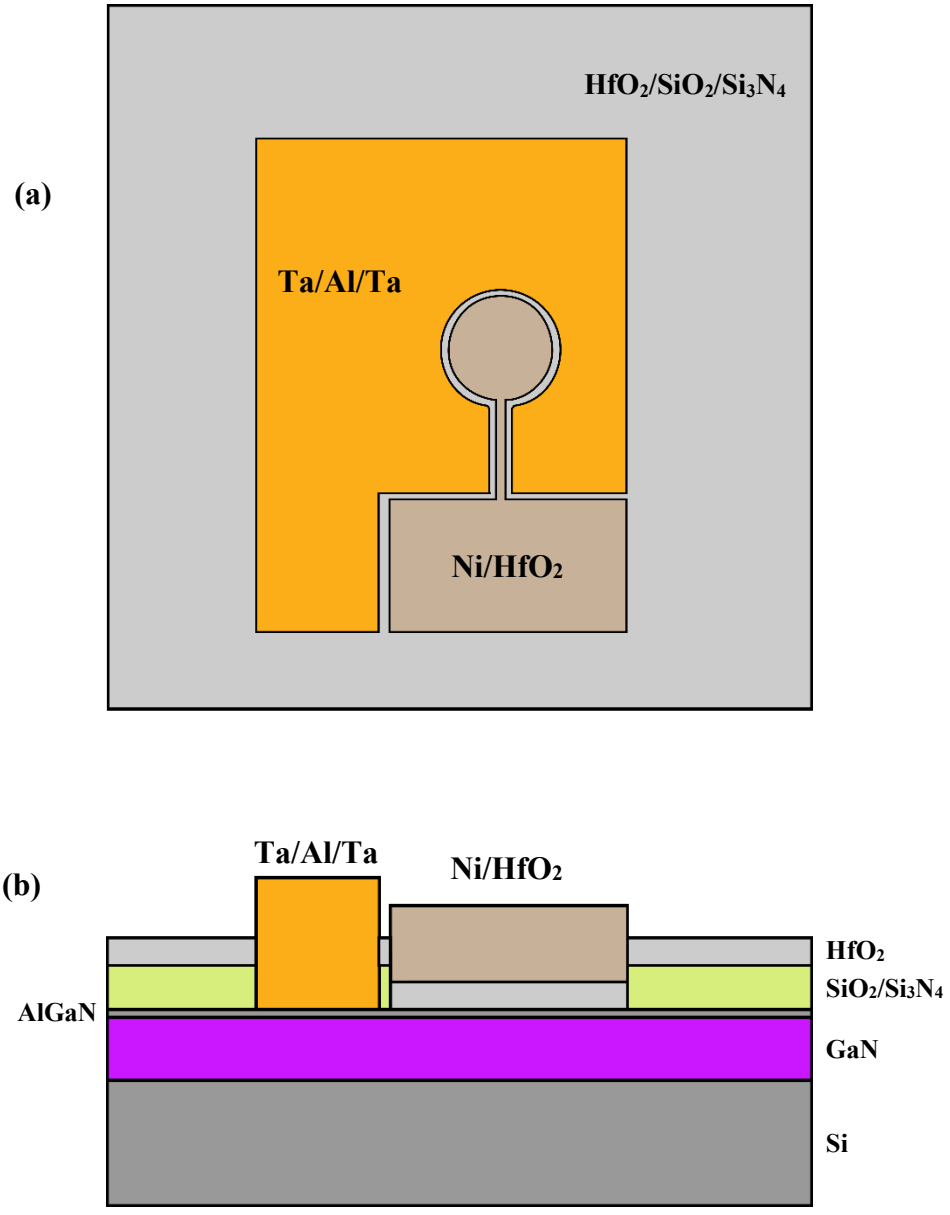


Figure 16. (a) Top and (b) cross-section view of MOSCaps

The development of MOSCaps on the heterostructure comprised the following modules – contact module and gate stack module. The following sub-sections deal with the process flow.

4.2 Contact module

The process began with cleaning the wafer samples in solvents, namely Acetone, IPA and DI water. The samples were put in beakers with the mentioned solvents and sonicated for 2 mins each. This is essentially a degrease process that removes most of the carbon-contaminants and other organic residues and contaminants on the GaN surface. The samples were then dipped in an HCl solution (10:1 DI water: HCl) for 10 mins to remove the Ga droplets and the native GaO_x. They were then dipped in BOE for 2 mins, which has been shown to act as a native oxide inhibitor for GaN [36].

The next step was the deposition of the field dielectric, SiN_x, using an Oxford PlasmaPro 80 PECVD. The purpose of the field dielectric was to avoid the gate contact pad being directly on the GaN surface, which would then contribute to the modulation of the 2DEG. A SiN_x film of 300nm was deposited using the following process parameters – 125 Sccm of SiH_4/N_2 and 700 Sccm of N_2 at 350°C and 600 mTorr chamber pressure. The next step was to perform lift-off lithography and patterning the SiN_x layer. Wet etch was used for accomplishing this task, namely BOE. However, the biggest challenge that was faced when performing wet etch was the formation of extreme lateral undercuts, to the tune of 3-5 μm, which was approximately 60% of the distance between the crescent-shaped contact pads left out for the gate contact pad. Different thicknesses were attempted to mitigate the undercut issue, namely 100 nm, 150 nm and 200 nm. Wet etch produced undercuts in each case, with a

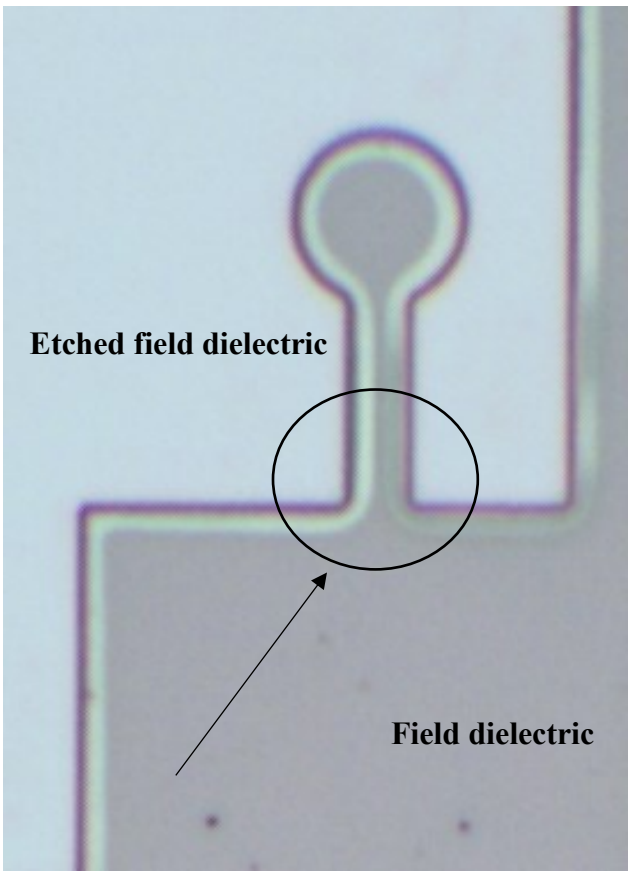


Figure 17. Zoomed-in area of the over-etch issue when using only wet etch

direct relationship between the undercut distance and the thickness of the dielectric. A generic schematic of the issue is shown in Fig. 17, showing a zoomed-in image of the issue.

There were two possible solutions to this issue:

(i) Dry etch (RIE): Keeping the thickness at 300 nm, dry etch would allow etching to be anisotropic and undercuts would be minimum. However, as pointed by Khan *et. al.* [37], plasma damage can reduce the 2DEG density and affect the mobility and transport characteristics of the HEMTs, which is undesirable.

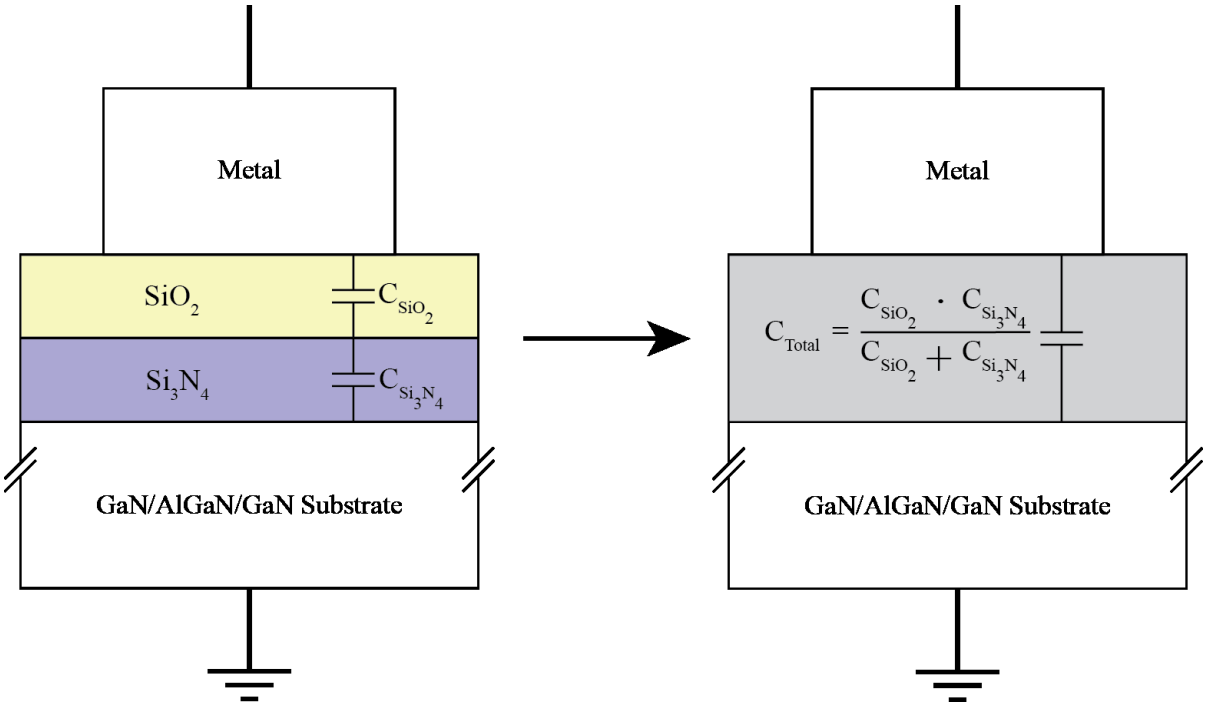


Figure 18. Capacitors in series can be combined into an equivalent capacitor

(ii) Wet and Dry Etch: A combination of both could be used to enhance the anisotropicity of the etch as well as reduce the undercut distance. Reduction of the thickness of the dielectric showed better results employing this technique. However, reduction of the thickness of the field dielectric would fail the purpose of having a thick dielectric under the gate contact pad to mitigate or make almost insignificant, the capacitance contribution from the gate pad. In other words, a field dielectric of 100 nm would allow the gate pad to contribute more capacitance as compared to a dielectric of thickness 200 nm.

To solve this issue, a dielectric stack of SiN_x and SiO_2 was used. SiN_x was mainly used due to its better interface properties with GaN as compared to SiO_2 [38]. From a simple calculation and concept of capacitance combination, as shown in Fig. 18:

$$\frac{1}{C_{Series}} = \frac{1}{C_{SiN_x}} + \frac{1}{C_{SiO_2}} \tag{22}$$

A few steps of simplification would modify the form of Eqn. 22 as follows:

$$\frac{1}{\kappa_{Series}} = \frac{1}{\kappa_{SiN_x}} + \frac{1}{\kappa_{SiO_2}} \tag{23}$$

where 'κ' denotes the dielectric constant.

The grown films, SiO_2 and SiN_x using PECVD ha1 refractive indices of 1.47 and 1.98 respectively, measured separately using an interferometer. Thus, using Eqn. 23, the overall capacitance contribution would be lesser when using a dielectric stack with a lower RI despite using a field dielectric of lesser thickness. The calculated overall dielectric constant of the stack came out to be, $\kappa_{stack} = 0.84$, as opposed to $\kappa_{SiN_x} = 1.98$, if only SiN_x was used.

Keeping in mind the damage induced by plasma to the 2DEG density, dry etch was first done on the dielectric stack to remove ~80nm of the stack. Photoresist was used as the mask, which was tested prior to the actual etching to withstand the RIE process quite well and even perform modestly for the subsequent lift-off process. The RIE recipe to etch the field dielectric stack used 200W ICP power and Ar and CF_4 were provided at 25 Sccm and 10 Sccm respectively, with the etching being done at room temperature. Individual etch rates for SiO_2 and SiN_x were found to be ~60nm/min and ~70nm/min respectively. The total etch time was 1min 15secs. BOE wet etch was followed by RIE to remove the residual SiN_x from the contact areas by etching for another 1 min.

Micrographs were taken and Profilometer measurements were done to confirm the complete removal of the dielectric from the contact regions. After the previous step, e-beam evaporation of the contact metal stack was done. A stack of Ta/Al/Ta (8/230/20 nm) was e-beam evaporated, with Ta being deposited at 0.7 Å/sec and Al being deposited at 1.5 Å/sec.

The low deposition rates were chosen to facilitate a faithful deposition of the contact metal stack. Once the deposition was done, lift-off was performed by stripping the photoresist. Micrographs confirmed the complete removal of the photoresist from the field region.

Next, the focus shifted to annealing the contact metal stack to achieve Ohmic contacts. Annealing was done at 575°C in an RTP in a N_2 environment at 30mTorr process pressure. Electrical measurements were done on the contacts to confirm that the contacts were Ohmic.

4.2.1 Ohmic contacts

TLM structures were developed on a separate sample using another mask, which was processed simultaneously while developing the MOSCaps to eliminate any possible manual handling errors, temperature variation (leading to variation in chemical reaction and etch behavior) and deposition thickness variation. TLMs are test structures which are developed to find the contact resistance of contact metals. A schematic of TLM test structures required to find contact resistance is shown in Fig. 19. A bright Ta/Al alloy is supposedly formed after annealing the samples. Electrical measurements were done on the TLM structures before moving forward to confirm the contacts were Ohmic.

Four-point probe measurements were done on the TLM structures using an HP4155B Semiconductor Parameter Analyzer (SPA), which has 4 Source/Monitor Units (SMUs) which can be configured to work either as a current source or a voltage source. For this measurement, one SMU was used as a current source, the current being driven through the inner contact pad, and another SMU was used to collect the current coming out of the outer contact pad.

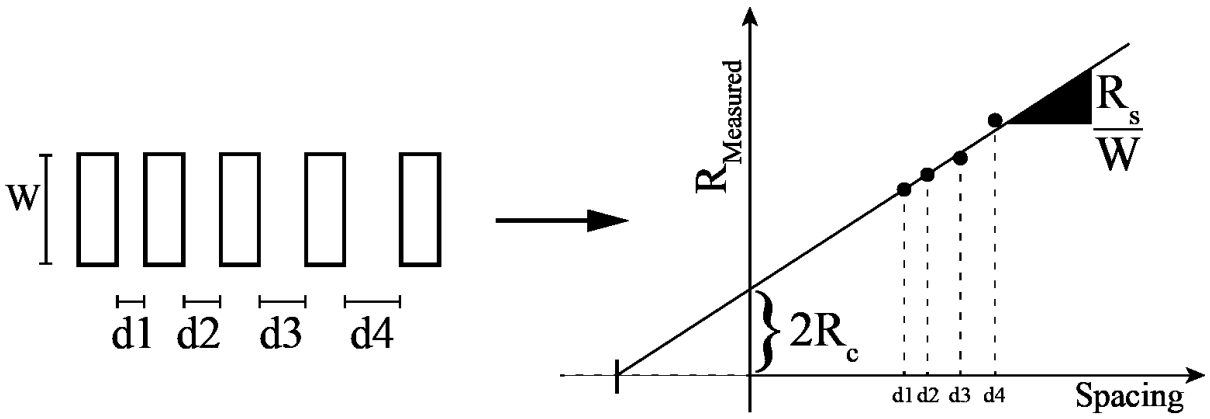


Figure 19. TLMs for contact resistance measurement (R_C)

The other two SMUs were used mainly to measure the potential difference. This scheme of measurement was used for a few reasons.

(i) First of all, using an SMU as a current source rather than a voltage source allows for bypassing the internal resistances of many components, namely the SPA, the probe tips and the tri-ax cables, which allowed for a true resistance measurement.

(ii) As a second benefit, it was possible to drive and collect the current from the outer edges of the contacts and the potential drop could be measured from the inner edges of the contact pads, which allowed for bypassing most of the potential drops occurring due to leakage and scattering.

Electrical measurements (I-V) were done on TLM structures where the as-fabricated spacing varied from 9 µm to 49 µm between the inner and outer contact pads. A voltage sweep from -1V to 1V was done and the current measured in a simple I-V measurement to confirm the Ohmic nature of the contacts, as shown in Fig. 20. Once the Ohmic nature was confirmed, the focus was shifted to extracting the contact resistance. For the four-point probe

measurement, a current of 10 mA was swept and the resultant potential drop measured. Since in III-V semiconductors, the channel is always present due to the presence of the 2DEG, I-V measurements reveal the resistance of the channel. The plot for normalized resistance versus as-fabricated spacing between the contact pads is shown in Fig. 21. A contact resistance (R_C) of 1.96 Ω-mm was extracted after suitable adjustments for the geometry of the TLM structures.

The importance of a low contact resistance to the GaN substrate is essential for eliminating the immense influence of the R_S factor during C-V and G-V measurements. The prominent presence of a high R_s value would indeed cause frequency dispersion in the C-V and G-V curves, which makes the accurate extraction of interface trap density and C_{acc} difficult.

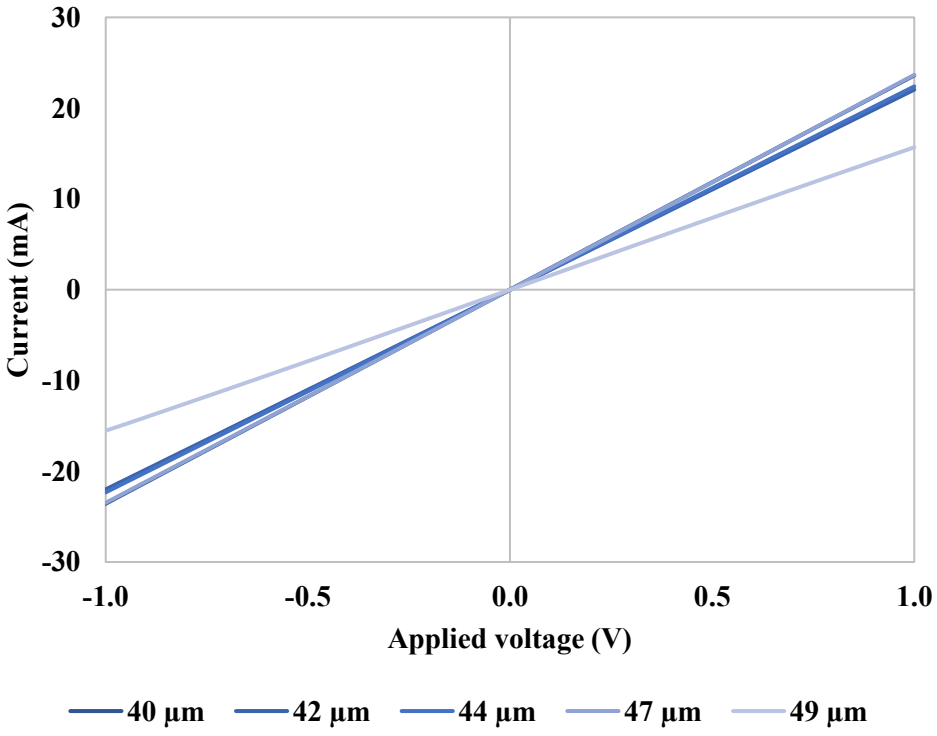


Figure 20. I-V measurements for TLM structures with increasing spacing

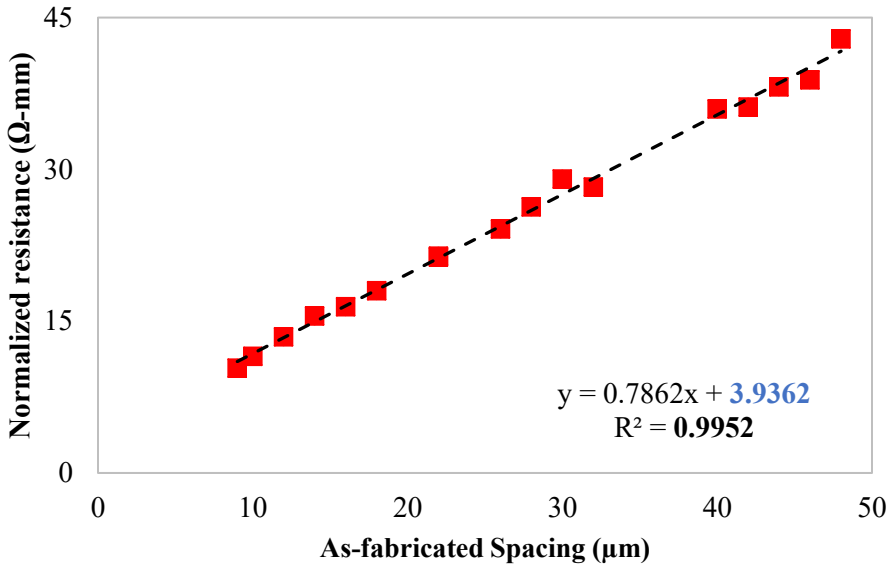


Figure 21. Plot of normalized resistance vs TLM spacing distance. As-fabricated spacing was used for retrieving true contact resistance data.

4.3 Gate stack module

The gate stack module consists of patterning the field dielectric by lithography, etching the field dielectric to the active GaN layer and finally, deposition of the gate dielectric using ALD. First of all, lithography was done to transfer the gate window pattern from the mask to the field dielectric layer. Alignment was done using a Karl Suss MA6 mask aligner and then exposed. After lithography, a similar combination etching technique was used as mentioned in a section before. The duration for the etching using both RIE and wet etch were the same as mentioned before. Again, micrographs were taken and Profilometer measurements (surface roughness and step height) were done to confirm the complete removal of the field dielectric from the gate region.

Immediately next, the wafers were dipped in HCl solution (10:1 DI water: HCl) to remove the native GaO_x that might have formed when the gate region was exposed to ambient air. This interfacial GaO_x layer has been known to be detrimental for device reliability. HCl

solution has also been known to remove Ga droplets from the surface, which were visible as a cloudiness in the gate windows after the field dielectric etching.

After the pre-gate deposition clean, the wafers were transferred to the ALD chamber, which was pumped down to 0.14 Torr at a N_2 purge rate inside the chamber of 20 Sccm. The deposition was carried out at a temperature of 200°C. The deposition, as explained earlier, took place in 2 cycles:

(i) The oxygen precursor, either H_2O or O_3, was pulsed for 0.015 sec followed by a N_2 purge for 10 secs.

(ii) The metal precursor for Hf, TEMAH, was pulsed for 0.2 sec followed by another N_2 purge 15 secs to remove the volatile by-products.

The deposition was done for 50cycles to get to a thickness of 5±0.2 nm, confirmed by measurement performed on an ellipsometer. Following the gate deposition, lift-off lithography was required to be performed to pattern the gate metal. The lift-off resist was spun before spinning the photosensitive resist for the lift-off lithography process.

Due to non-availability of the dark field mask required in this step to form the gate metal contacts, image reversal process had to be done along with lift-off process. As a first step toward image reversal and lift-off, the lift-off resist was spun on the wafer and the achieved thickness was 400 nm. Next, the image reversal photoresist, AZ5214-E IR (IR for image reversal) was spun on the wafer and a thickness of ~1.4 μm was achieved, the total being close to ~1.8 μm. After a soft-bake of 40 secs at 120°C, a half-dose exposure corresponding to AZ5214E was done, i.e. 60mJ/cm^2. The soft-bake procedure enhanced the cross-linking inside the polymer, and the exposure made soluble the places on the wafer not covered by the mask during exposure. The full strength of dosage generally required for proper development was

not used to ensure fidelity of the polymer for the next step to be performed. In the next step, another soft-bake, also known as the reversal bake, was done for 50 secs at 120°C again. The purpose of this bake is to harden the portion of the resist that was made soluble by exposure and thereby enhancing the cross-linking. On the other hand, there is minimal effect on the un-exposed regions on the photoresist till now. As a next step, a flood exposure of 250mJ/cm^{-2} was done, as found from the specification sheet for AZ5214-E IR. The purpose of this exposure step is to ensure that the portion on the photoresist that had been unexposed till now get the sufficient dosage to be soluble, whereas the already soluble resist hardens further, so much that they bind very well and cannot be developed by the developer. Thus, once the image reversal steps were done, all that was needed to be done was developing the samples to get an image exactly opposite to the pattern present on the mask, on the wafer. After the image reversal and lift-off lithography, the wafer samples were transferred to the e-beam evaporation chamber to deposit the gate metal, Ni, up to a thickness of 200nm. The process pressure was 5×10^{-6} Torr and no heating was done on the substrate. A slow evaporation rate of 1.3 Å/sec was used. Post evaporation, lift-off was achieved by stripping the photoresist in AZ400T for 10 mins. To complete the module, lithography was needed to be done to open contact windows by patterning the HfO_2. An Oxford Plasmalab 100 RIE system was chosen for this step. A flow of 20 Sccm of SF_6 and 10 Sccm of Ar with a combination of 50 W of RF power and 500 W of ICP power was used to etch the ALD-grown HfO_2, where the etch rate was found to be ~23 nm/min.

4.4 Characterization

Upon completion of the modules, electrical measurements were performed in the form of C-V, G-V and leakage current-voltage measurements. During each of the gate dielectric deposition by ALD using the two different oxygen sources, cleaned GaN/AlGaN/GaN control samples were placed in the chamber – chemical analysis was performed on these using XPS.

4.4.1 Chemical analysis

Before moving on to the electrical characteristics, some light needs to be shed on the chemical structure and composition of the films grown using the two different oxygen sources. Chemical analysis was performed using an Omicron XPS system equipped with Argus detector with Al K_α X-rays (E_{photon} = 1486.7 eV) being subjected at the sample at an angle of 45°. The chamber pressure was kept at 3.2×10^{-7} Torr all measurements were done at room temperature. All XPS spectra shown in this work have been shifted based on the adventitious carbon peak.

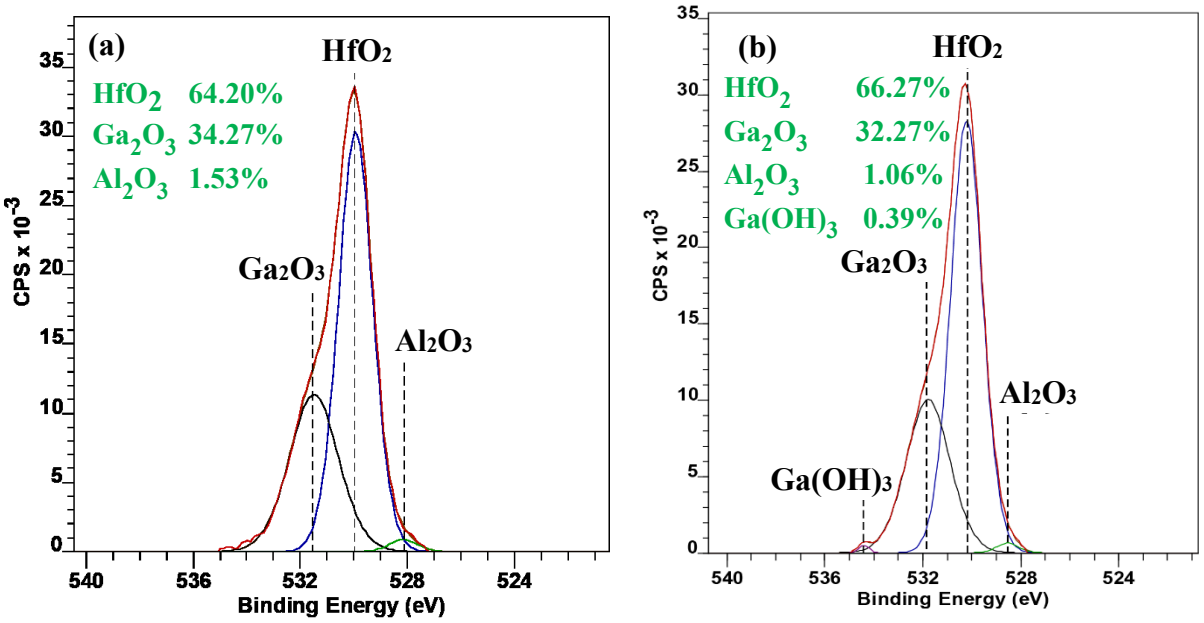


Figure 22. O 1s spectrum for (a) O_3-based and (b) H_2O-based HfO_2 film

Figure 22 shows the O 1s core-level spectrum for the two individual films. A sharp peak (low FHWM; lower is better) is seen at 529.93eV and 530.21eV for the O_3-based and H_2O-based samples respectively, which correspond well to the binding energy for HfO_2. A second peak at 531.79eV and 531.51eV respectively is evident from the two spectra which correspond to binding energy for GaO_x, essentially Ga_2O_3. The insets shown for both the spectra indicate the areal composition of the different components present at the interface. A shift toward the lower binding energy can be seen for the O_3-based HfO_2 sample. Kim *et.al.* confirmed a similar observation in the Al 2p and O 1s spectra for the O_3-based film when comparing Al_2O_3 films grown by ALD using either H_2O or O_3 as the oxygen source [26]. This was attributed to the reduction of –OH groups from the interface when using O_3 as the oxygen source that generally appear from exposure to moisture or during the early stages of ALD

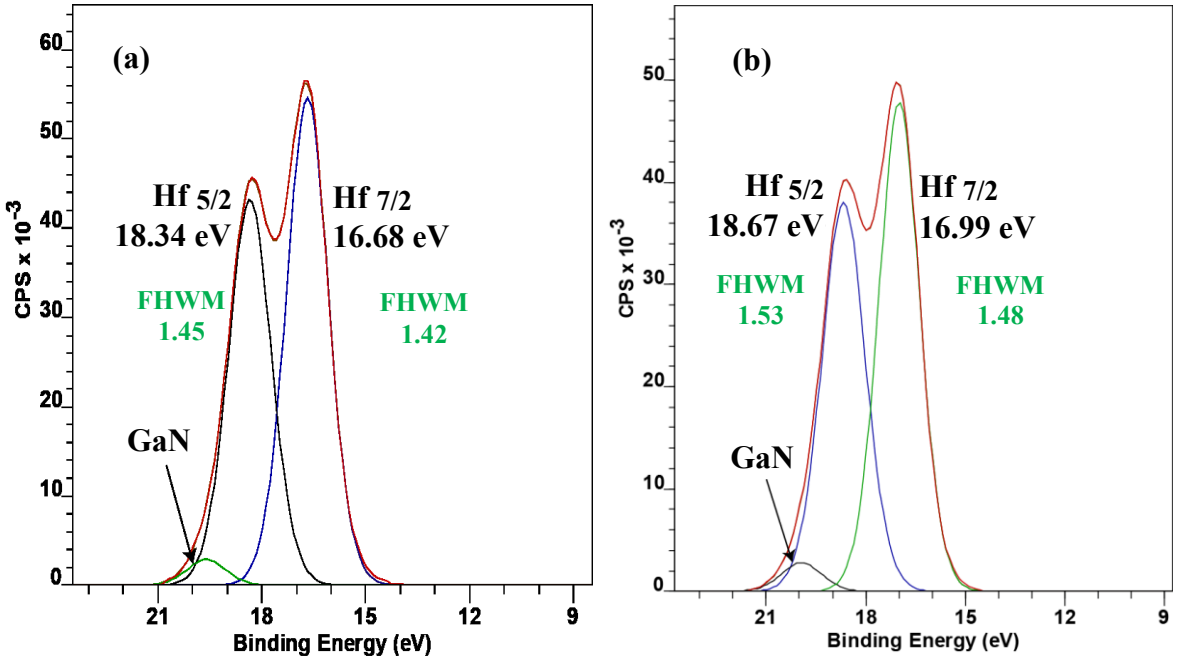


Figure 23. Hf 4f spectrum for (a) O_3-based and (b) H_2O-based HfO_2 film

growth by H_2O as oxygen source; the surface is terminated by these –OH bonds which act as the chemically active centers for the metal precursor in the next pulse to form the desired oxide. This confirms the removal of the –OH groups or "dehydration" effect with O_3 as oxygen source. Figure 23 shows the Hf 4f core level spectrum for both the films. The two peaks represent the splitting of the Hf 4f, which occurs due to the spin-orbital interaction resulting in a split into doublets. A difference of 1.7eV in binding energy (BE) is observed between the split states, Hf $4f_{7/2}$ (lower binding energy) and Hf $4f_{5/2}$ (higher binding energy), which has been reported elsewhere in literature [39]. The FHWM values for the peaks indicated in the insets for the two spectra confirm that with O_3 we get a consistent and more complete HfO_2, as was hinted by the O 1s spectrum. Also, a shift toward the lower binding energy seen in the Hf 4f spectra is consistent with the observation made in the O 1s spectra and inherits a similar explanation. It is possible that due to the increased supply of oxygen by the rapid decomposition of ozone compared to that of H_2O as oxygen source, there is a more complete and better bulk HfO_2 formed. The better (lower) FHWM values of the peaks in the Hf 4f spectra for the O_3-based sample is due to the same reason.

Figure 24 shows the Ga 3d spectra obtained for the two individual films. The primary peak seen at the lower binding energy (16.68eV and 17.01eV respectively for O_3-based and H_2O-based sample) corresponds to the binding energy for GaN, with the O_3-based sample showing a shift toward lower binding energy, which can be explained as done above. The second peak seen at a slightly higher binding energy (18.34eV and 18.61eV respectively for the O_3-based and H_2O-based sample) corresponds to the formation of Ga_2O_3 in the presence of an oxygen source. This is due to the oxidation of the thin GaN layer at the top or the AlGaN layer just beneath it. It can also be seen from the areal composition values as provided in the

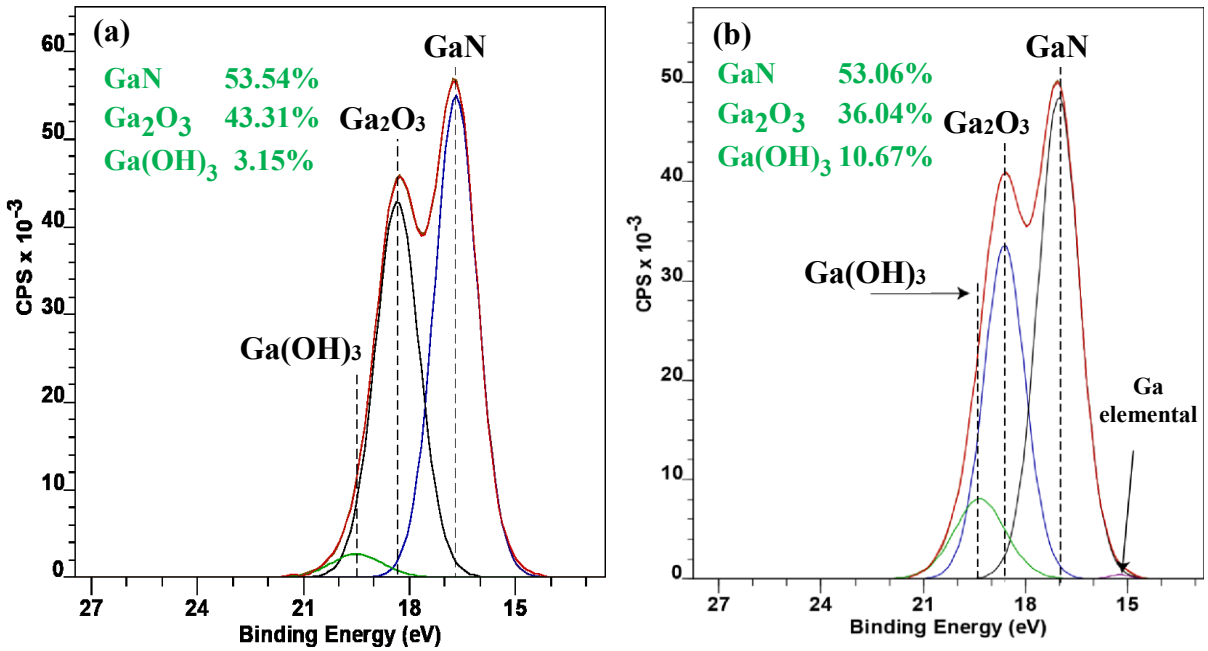


Figure 24. Ga 3d spectrum for (a) O_3-based and (b) H_2O-based HfO_2 film

insets that there is a significant increase in the Ga_2O_3 content when O_3 is used the oxygen source, which can solely be explained by the more reactive nature of O_3 than H_2O. Another peak can be seen toward a slightly higher binding energy for both the films (left most peak for both spectra) which corresponds to the binding energy for $Ga(OH)_3$ content at the interface. There is a marked decrease in the $Ga(OH)_3$ concentration at the interface when O_3 is used as the oxygen source. This could be a potential contributing factor toward reducing the through-gate leakage current; the –OH groups have been known to reduce the bulk and interfacial qualities of dielectric films because they act as active trapping centers thereby increasing leakage current. A very small peak can be seen in the H_2O-based sample (to the far right) which could indicate the presence of some elemental Ga in the H_2O-based sample, which seems to be absent in the O_3-based sample. The peak however is quite insignificant compared to the others and it could be appearing due to manual error in eliminating the background signal.

From the XPS analysis, it can be concluded that a better bulk HfO_2 dielectric can be achieved using O_3 as the oxygen source in ALD due to a reduction of the –OH groups and presumably by a more complete formation of HfO_2 due to sufficient amount of oxygen being available in the early stages of ALD growth. However, the downside of the growth with O_3 is that either the GaN or the AlGaN layer or both are affected by the diffusion of oxygen which oxidizes the GaN or AlGaN to form Ga_2O_3. The effect of the reduction of –OH groups at the interface and the increased growth of Ga_2O_3 on device performance is studied using electrical characterization in the form of capacitance-voltage, conductance-voltage and leakage current characteristics of the MOSCap structures developed.

4.4.2 Electrical characterization

C-V and G-V measurements were done using an Agilent E4980A Precision LCR meter in the parallel mode of measurement. A step size of 0.1 V with an AC signal magnitude of 20mV was used and measurement was done starting from high to low voltage and back to high voltage. All measurements were done in the dark to avoid any photoionization effect and to suppress contribution from deeper-in-the-bandgap traps and bulk traps.

Figure 25 and 26 shows the frequency-dependent C-V and normalized G_P/ω-V curves respectively derived from measurements performed on O_3- and H_2O-grown-HfO_2/GaN/AlGaN/GaN MOSCaps. Due to the high leakage current beyond accumulation, measurements were done only till V_G = 0V to avoid any misinterpretation of events. The measured MOSCaps had a diameter of 100 µm. There is a visibly stretched-out transition from the accumulation region of the 2DEG to depletion in the case of the O_3-based sample, when compared to the H_2O-sample. This is a clear indication of the presence as well as activity of interfacial traps at the AlGaN/GaN interface because the 2DEG is present only at the

AlGaN/GaN interface. The parallel conductance is the most sensitive parameter to detect interfacial trap activity (Section 3.2). Figure 26 shows the normalized parallel conductance G_P/ω curves which clearly show an increased conductance activity in the accumulation to

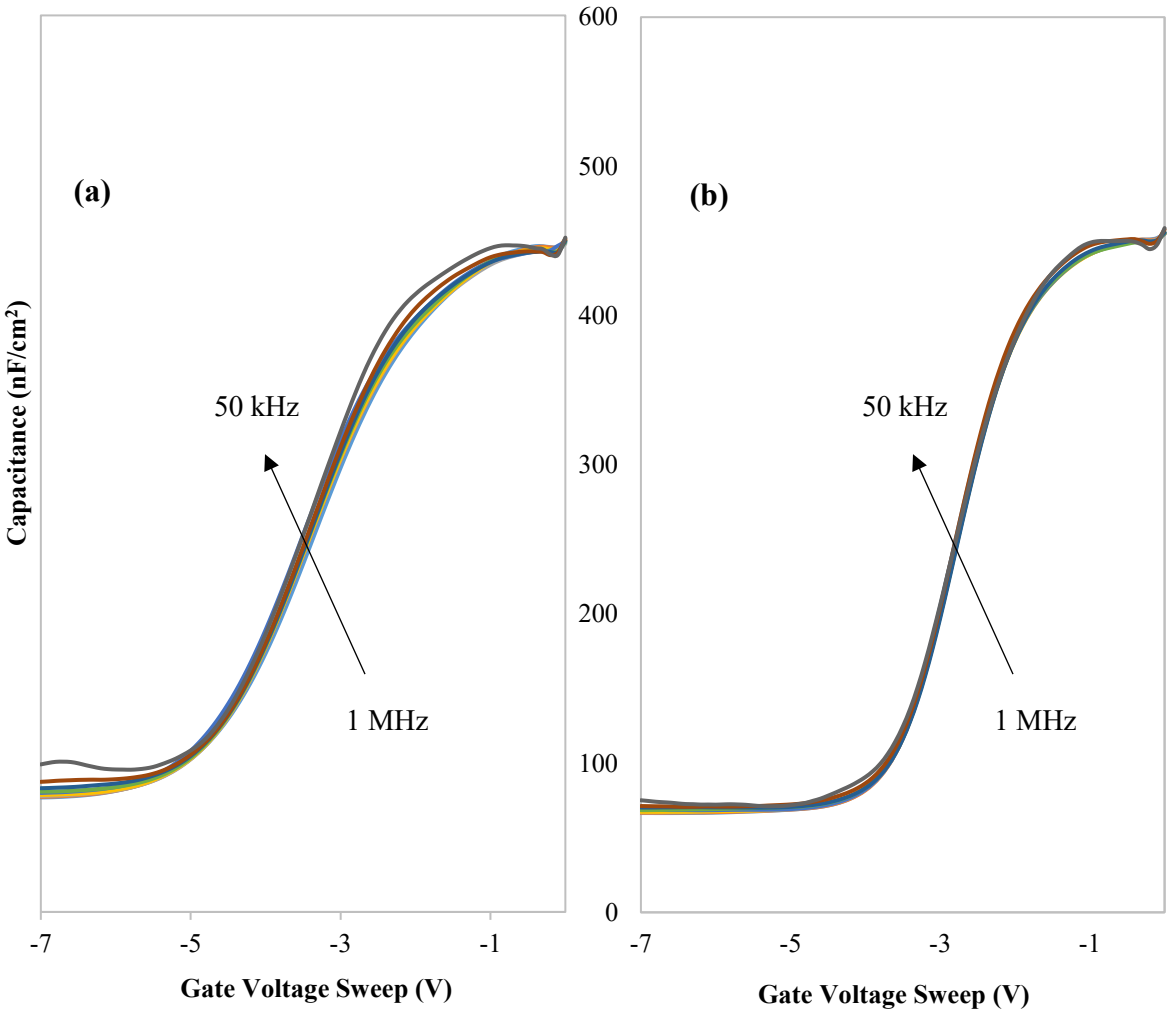


Figure 25. R_s corrected C-V curves for (a) O_3-grown and (b) H_2O-grown-HfO_2/GaN/AlGaN/GaN MOSCaps

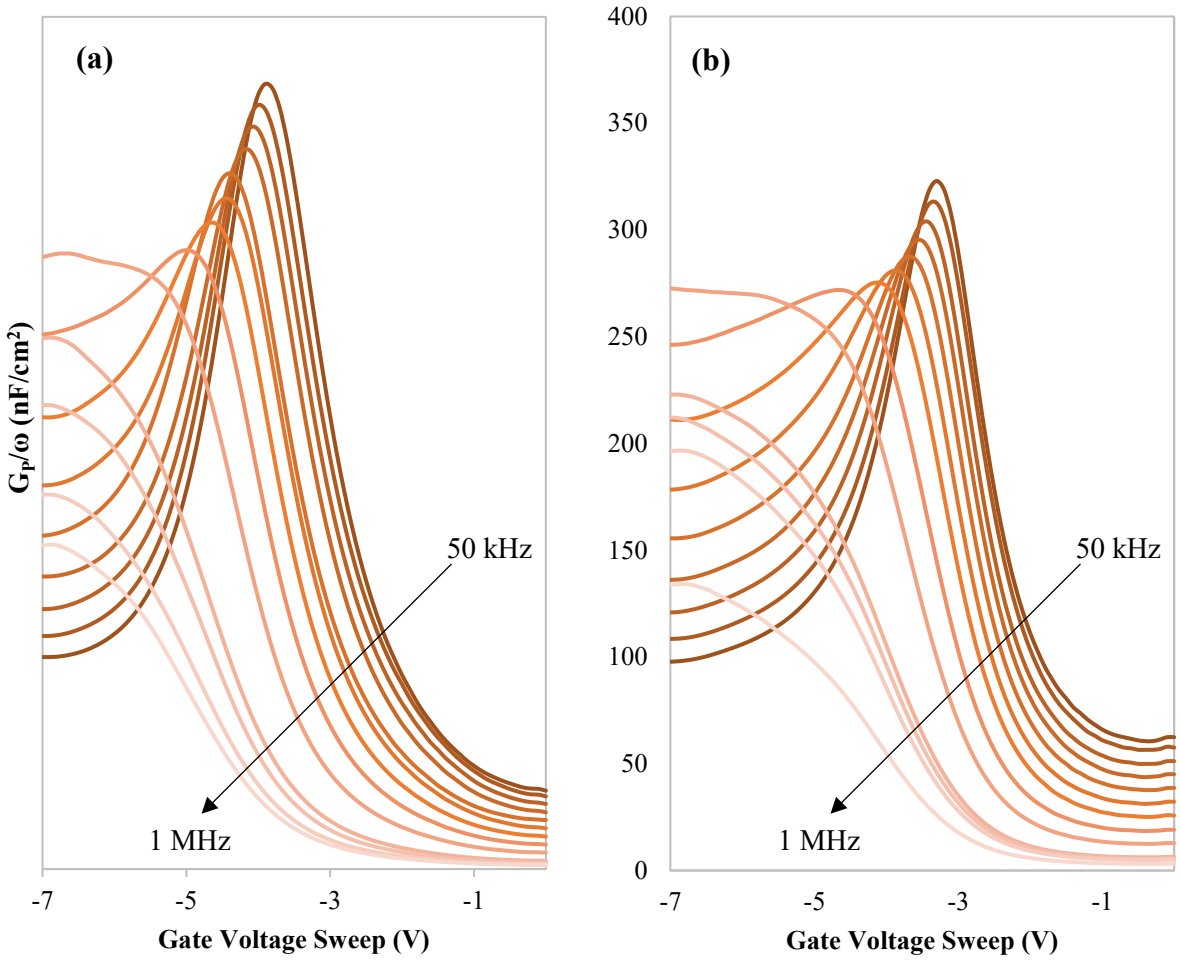


Figure 26. R_s corrected G_P/ω curves for (a) O_3-grown and (b) H_2O-grown-HfO_2/GaN/AlGaN/GaN MOSCaps

depletion transition region ($-4V < V_G < -3V$) for the O_3-based sample compared to the H_2O-based sample. The experimental G_P/ω curves were used to extract the interface states density (D_{it}) and interfacial traps constants (τ_{it}) using the single trap state fitting equation as follows:

$$\frac{\langle G_P \rangle}{\omega} = \frac{qD_{it}\omega\tau_{it}}{1 + (\omega\tau_{it})^2} \tag{24}$$

Figure 27 illustrates the normalized G_P/ω vs. ω plots at a particular range of gate bias voltage, where there is maximum conductance activity for both samples, which would be due

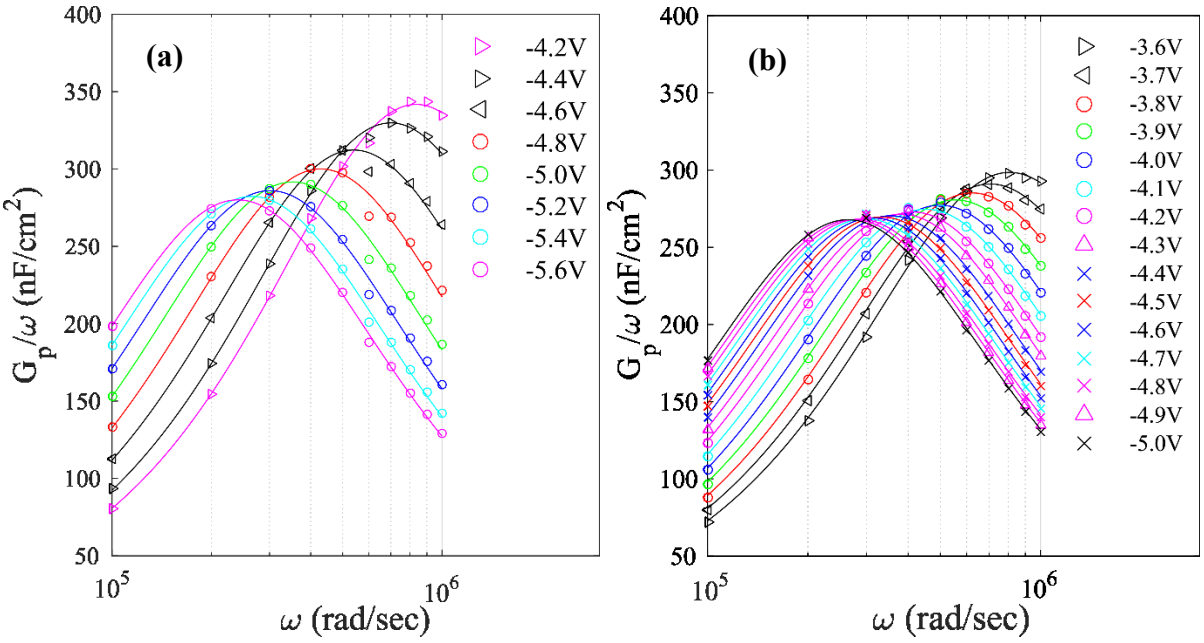


Figure 27. G_P/ω vs. ω plots showing the extraction of the trap parameters by fitting the single state trap equation for (a) O_3-based and (b) H_2O-based sample

to the modulation of the 2DEG by the gate as well as contribution to the conductance by the dynamic charging and discharging of the traps at the AlGaN/GaN interface. The fitted curves using Eqn. 24 are shown in Fig. 27 for both the samples.

As mentioned in Section 2.4, the interface trap density, D_{it}, is related to G_P/ω as follows:

$$D_{it} \approx \frac{2.5}{qA} * \left(\frac{G_p}{\omega}\right)_{max}$$

The extracted trap parameters for both the samples are shown in Fig. 28 and Fig. 29 for both the samples at a similar range of gate bias voltages. A higher trap density can be found for the O_3-based sample as compared to the H_2O-based sample, which accounts for the higher conductance peak observed in Fig. 26 for the O_3-based sample. The trap time constants were also extracted in a similar pattern and is shown in Fig. 28.

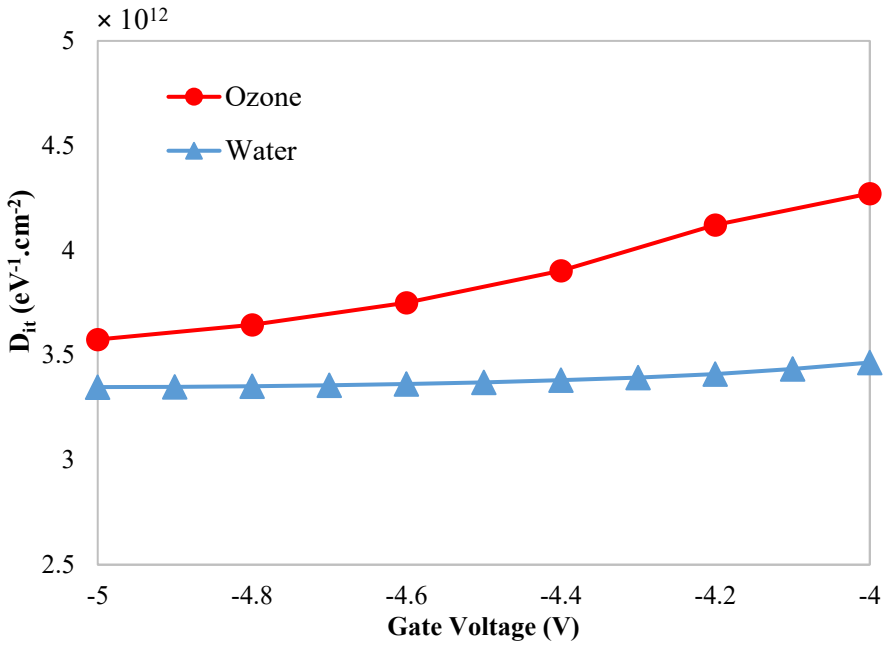


Figure 28. Extracted D_{it} from the normalized G_P/ω vs. frequency plots using Eqn. 24

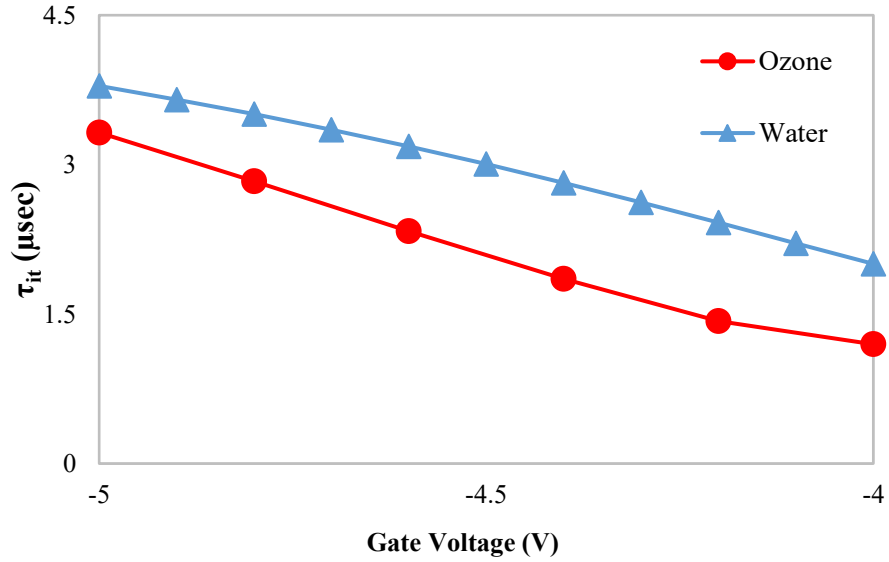


Figure 29. Extracted τ_{it} from the normalized G_P/ω vs. frequency plots using Eqn. 24

Compared to the H_2O-based sample, the traps in the O_3-based sample have relatively

lower τ_{it} (lesser time for charging and discharging) which means more of these traps can follow the AC signal used for measurement and thereby contribute to the parallel conductance.

This brings to question the origin of these traps. This could be an effect of surface oxidation of the barrier layer, AlGaN, or the GaN cap due to the rapid oxidation by ozone. It has already been reported in literature that oxygen impurities are present in abundance in GaN and AlGaN, which act mainly as shallow interface donor traps with an activation energy of 30 meV and presumably are the only residual donor species leading to the formation of the 2DEG at the heterointerface [40, 41]. The increased growth of Ga_2O_3 for the O_3-based sample could possibly indicate the formation of a shallow sheet of oxygen donor states of almost equal density as the 2DEG – this would lead to generation of a huge density of surface electronic states. The increased shallow oxygen donor states would then contribute to leakage by

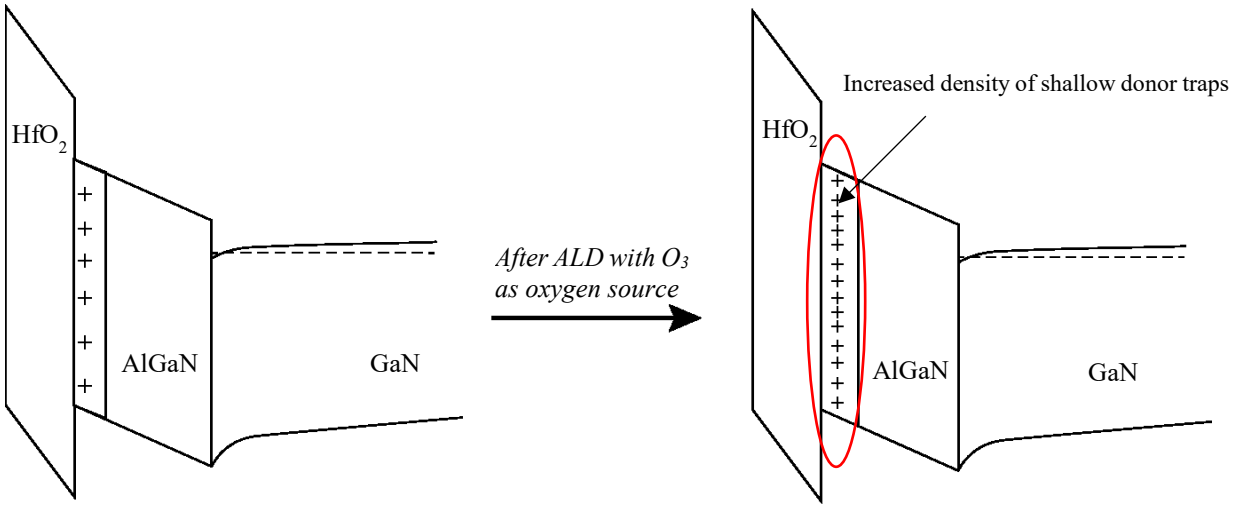


Figure 30. Possible mechanism for the increase in electrical trap activity for the O_3-based sample under strong negative bias. With the formation of Ga_2O_3 at the HfO_2/AlGaN interface, there is an increase in the number of positive surface donors, leading to transfer of electrons to these empty surface donors from the channel showing up as an increased electrical activity in the conductance plot

'donating' electrons when the Fermi level lines up with these traps to become positively charged empty donor states, as shown in Fig. 30. Consequently transfer of carriers from the channel to these traps could take place due to direct tunneling through the AlGaN barrier layer as indicated by the higher conductance peak for the O_3-based sample. Further investigation of the ozone-based degradation, however, is required to confirm the mechanism hypothesized here. There was also a hint in the XPS data of a better bulk dielectric HfO_2 being achieved using O_3. Figure 31 shows the leakage current characteristics of the MOSCaps with ALD HfO_2 being grown using the two different oxygen sources. As evident from the XPS data, the bulk quality of the HfO_2 grown using O_3 is indeed better, confirmed by the almost half-order of

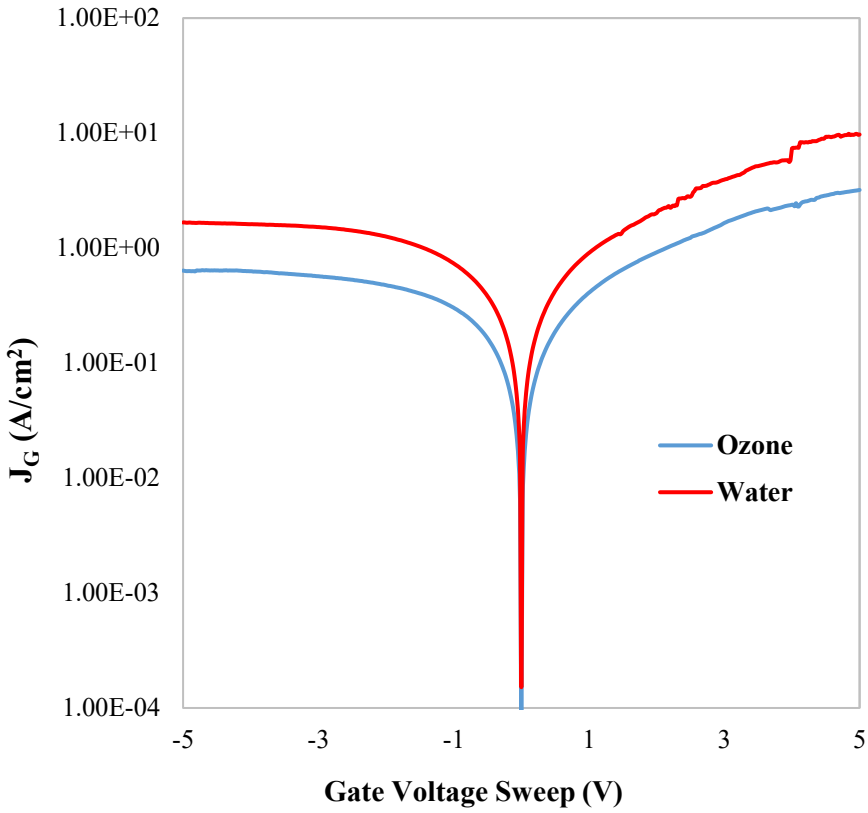


Figure 31. Leakage characteristic comparison of HfO_2 dielectric grown using either O_3 or H_2O

magnitude lower gate leakage current than the H_2O-based sample. The denser the bulk dielectric, the better it is able to prevent tunneling of electrons, which is evident from the leakage characteristics. There is probably a soft breakdown in the H_2O-based dielectric around $V_G = 4$ V where a step-like feature is seen. However, no such breakdown is observed in the case of the ozone-grown dielectric, confirming the superiority of the bulk property.

5. SUMMARY

This study explored the possibility of growth of high-κ dielectrics for use as gate dielectric by atomic layer deposition using ozone as oxygen precursor. The choice of dielectric in this work was HfO_2 due to its high dielectric constant (20-25) which can result in smaller decrease in transconductance, translating to better gate control over the channel. HfO_2 has been shown to crystallize at relatively low temperature anneals (500-700°C) which causes leakage current to increase by tunneling. Thus a lower temperature growth alternative for HfO_2 with good interfacial and bulk properties can benefit at large the device performance characteristics. Atomic layer deposition can be done at relatively low temperatures compared to other dielectric deposition methods. H_2O has been the most studied oxygen source for growth of dielectric by ALD. However, it has been shown already on silicon that –OH groups and metal clusters tend form at the initial stages of ALD growth due to insufficient supply of oxygen by H_2O that contribute to increase in leakage by degrading the interfacial and bulk dielectric properties. The effect of ozone on leakage on silicon has also been studied which has shown the potential for the reduction of –OH groups as well as metal clusters, thereby improving the interfacial and bulk dielectric properties.

To study the effect of ozone on the interfacial and bulk properties of HfO_2 grown on GaN/AlGaN/GaN heterostructures, a baseline fabrication flow for developing metal oxide semiconductors capacitors was developed on silicon, where the gate dielectric was grown by atomic layer deposition method using H_2O as the oxygen source. Electrical measurements were done on these metal oxide semiconductor capacitors to act as a reference for future experiments. Finally, a similar fabrication flow was set up for developing metal oxide semiconductor capacitors on GaN/AlGaN/GaN heterostructures, where the gate dielectric

HfO_2 was grown using either ozone or H_2O as the oxygen source in ALD. Electrical measurements and chemical analysis of the two kinds of films grown were used as probes for studying the effect of ozone against H_2O in the growth.

The increased reactivity of ozone stems from its rapid decomposition at 200°C (deposition temperature) and this provides sufficient supply of oxygen in the initial stages of atomic layer deposition to form a more complete bulk HfO_2. However, the rapid reactivity of ozone causes surface oxidation of the GaN-cap or the AlGaN barrier layer or both, which might be introducing excess electronic surface donor states that aid in leakage current. Electrical characterization in the form of capacitance– and conductance–voltage was done, where a higher peak in the conductance peak and a stretch-out in the capacitance curve could be seen, both of which could be attributed to the formation of shallow oxygen donor traps aiding in leakage, thereby degrading the HfO_2/AlGaN interface. The mechanism of ozone-based degradation however requires further investigation. Leakage current characteristic showed the superiority of bulk properties of ozone-grown HfO_2 in suppressing leakage current by almost half an order of magnitude compared to the H_2O-grown HfO_2, confirming the effectiveness of ozone in removing –OH groups and Hf-clusters and hence forming a better bulk dielectric.

The effectiveness of ozone in achieving a better bulk dielectric is observed here at the cost of a poor interface between the dielectric and the heterostructure, causing an instability in the threshold voltage, which could cause degradation of the devices. Further investigation needs to be done in order to take steps to enhance and better control the reactivity of ozone to avoid spurious oxidation damage to the barrier or cap layer. Keeping in mind the better bulk properties achieved in this study with ozone, effective control of ozone reactivity could result in both better interfacial and bulk properties of the dielectric and hence further suppress leakage

current for use in metal oxide semiconductor high electron mobility transistors catered to high-power, high-voltage and high-speed switching circuits successfully.

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