BICMOS POWER DETECTOR FOR PULSED RF POWER AMPLIFIERS

A Thesis

by

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MASTER OF SCIENCE

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ABSTRACT

A BiCMOS power detector for pulsed radio-frequency power amplifiers is proposed. Given the pulse waveform and a fraction of the power amplifier's input or output signal, the detector utilizes a low-frequency feedback loop to perform a successive approximation of the amplitude of the input signal. Upon completion of the successive approximation, the detector returns 9-bits representing the amplitude of the RF input signal. Using the pulse waveform from the power amplifier, the detector can dynamically adjust the rate of the binary search operation in order to return the updated amplitude information of the RF input signal at least every 1ms. The detector can handle pulse waveform frequencies from 50kHz to 10MHz with duty cycles in the range of 5- 50% and peak power levels of -10 to 10dBm. The signal amplitude measurement can be converted to a peak power measurement accurate to within $\pm$0.6dB of the input RF power.

DEDICATION

To Jesus.

”Commit your work to the Lord, and your plans will be established.”

Proverbs 16:3 (ESV)

ACKNOWLEDGMENTS

First, I would like to thank Dr. Aydin Karsilayan for his support throughout my graduate studies. He challenged me to reach further than I knew I could. I also greatly appreciate the many conversations that included Dr. Jose Silva-Martinez, as his experience in analog and mixed signal design shaped the course of my research significantly. I would also like to extend thanks to Dr. Steven Wright and Dr. Jay Porter for serving as members of my committee. Thank you to Sandia National Labs for their support in this research, and specifically to Mike Elsbury and Garth Kraus for their patience, kindness, and technical supervision throughout this project.

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CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supervised by a thesis committee consisting of Professor Aydin I. Karsilayan, Professor Jose E. Silva-Martinez, and Professor Steven M. Wright of the Department of Electrical and Computer Engineering and Professor Jay R. Porter of the Department of Engineering Technology and Industrial Distribution.

The comparator and buffers used in the BiCMOS power detection chip, as well as the binary weighted current source and counter in the sine wave generator in the same chip, were designed by James Lunsford of the Department of Electrical and Computer Engineering.

All other work conducted for the thesis was completed by the student independently.

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1. INTRODUCTION

RF power detectors are widely employed to optimize the performance of RF systems. These circuits find particular use in both the receive and transmit paths of modern communication systems. In the receive path, power detectors are often used in automatic-gain-control systems that boost the dynamic range of the receiver [1, 2]. In the transmit path, power detectors are used to aid in controlling the transmitted power to meet regulatory standards and to prevent damage to the power amplifier in fault conditions [3]. In general, the performance of RF power amplifiers depends on a few key adjustable parameters such as biasing conditions and input power. It is often critical to adjust these parameters in order to optimize RF power amplifier performance. The performance of the RF power amplifier can be characterized by observing several parameters including drain current, temperature, and gain- which is precisely where RF power detectors are utilized. The power detector must be able to make a detection quickly enough to prevent damage from occurring in the power amplifier should a fault condition occur. The demand for ever-increasing system integration calls for these power detectors to be integrated with or close to the RF power amplifier.

Many unique solutions exist to implement integrated RF power detectors. The majority of these solutions can be categorized into one of three groups: logarithmic detectors, root-mean-square detectors, or peak detectors. Logarithmic detectors employ a cascade of amplifiers in order to detect power across a wide dynamic range. Root-mean-square detectors output a voltage that is proportional to the rms value of the waveform, and are often used to measure the power of modulated RF signals with high peak-to-average ratios. Peak detectors output a dc voltage proportional to the peak amplitude of the signal, and are straightforward to implement.

Several logarithmic power detectors are proposed in [4–8]. All of these power detectors exhibit dynamic ranges equal to or greater than 40dB. However, none of these detectors achieve accuracies greater than $\pm 1dB$.

Several rms power detectors are proposed in [1, 9–11]. The detectors proposed in [9–11] each have insufficient accuracy for the specifications targeted for this design. The detector proposed in [1] does not achieve the bandwidth requirement specified for this project.

One unique amplitude measurement technique for built-in self-test is proposed in [12]. While achieving exceptional accuracy, this technique requires almost 500ms to complete, far longer than the necessary 1ms refresh period specified for the detector presented in this thesis.

Of all of the power detector types, the design of RF peak detectors is by far the simplest. Because of their simple design and low component count, these detectors have the advantage of wide bandwidth, low power, and small chip size [13]. Due to the lack of availability of fast diodes in standard silicon processes, bipolar transistors are often used to implement these RF peak detectors, such as in the Meyer detector [14]. The major disadvantage of this detector implementation is that it is traditionally very hard to predict input signal strength accurately in the crossover region, which is the region of operation between the detector high voltage linear and low voltage square law behaviors.

Utilizing a low-frequency calibration loop, the detector presented in this thesis utilizes bipolar RF peak detectors and the advantages that come with them while overcoming the crossover region limitation. In fact, with the proposed calibration technique, the peak detector response need only be monotonic, and not necessarily proportional to the input amplitude.

Discussion related to the design and performance of this proposed RF power detector will ensue in the remainder of this thesis. Section 2 gives an overview of the proposed

RF power detector. Section 3 describes a ”hybrid” power detector using CMOS peak detectors and discusses the limitations of those peak detectors. Measurement data of the hybrid power detector is presented. Section 4 describes the design and performance of a single-chip RF power detector with bipolar peak detectors that approaches the required target specifications for this project. Finally, section 5 summarizes the work completed.

2. OVERVIEW OF PROPOSED RF POWER DETECTOR

2.1 Target Specifications

The proposed RF power detector for pulsed RF power amplifiers was designed with certain target specifications in mind, which can be seen in table 2.1. The RF input frequency range defines the possible frequencies of the input sine wave. The pulse period range defines the possible periods at which the input sine wave can be pulsed. The duty cycle range defines the possible duty cycles at which the input sine wave can be pulsed. Figure 2.1 shows a conceptual drawing of a pulsed sine waveform, and serves to aid in describing the parameters of the waveform the power detector will receive as an input.

As figure 2.1 depicts, when the pulse is on, a sine wave with the period T_{sine} and zero-to-peak amplitude A is present. When the pulse is off, no waveform is present. The pulse on/off cycle is periodic with a period of T_{pulse}. The width of each of the pulse on times is specified by T_{pw}.

The following equations show the relationship between the parameters shown in figure 2.1 and the specifications for the power detector shown in table 2.1.

Parameter	Specification
Input Sine Frequency Range	2-4GHz
Pulse Period Range	100ns - 20μs
Pulse Duty Cycle Range	5 - 50%
Input Sine Peak Power Range	-10 - 10dBm
Maximum Power Detection Error	$\pm$0.5dBm
Minimum Power Detection Refresh Rate	1kHz

Table 2.1: Target specifications for the proposed RF power detector

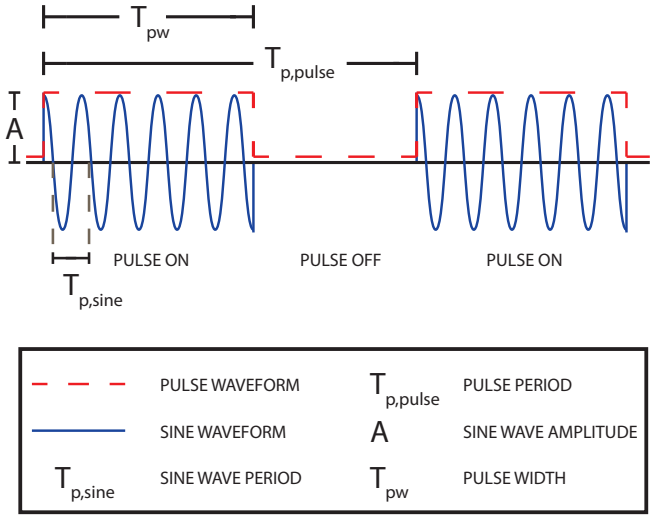


Figure 2.1: Conceptual depiction of pulsed sine waveform with parameter definitions

$$f_{sine} = \frac{1}{T_{sine}} \quad [Hz] \tag{2.1}$$

$$duty\ cycle = \frac{T_{pw}}{T_{pulse}} \times 100 \quad [\%] \tag{2.2}$$

$$P_{sine(peak)} = 10 \log \left(10 \cdot A^2\right) \quad [dBm] \tag{2.3}$$

where f_{sine} is the frequency of the sine wave, $duty\ cycle$ is the duty cycle of the pulse waveform, and $P_{sine(peak)}$ is the peak power[1] of the sine wave with respect to a 50-ohm load.

The power detection error is defined as $\Delta P = P_{sine,RF(peak)} - P_{sine,CAL(peak)}$, where $P_{sine,RF(peak)}$ is the peak power of the RF input wave and $P_{sine,CAL(peak)}$ is the peak power

[1]In this scenario, the peak power of the sine wave is obtained by calculating the power of the sine wave when the pulse is on. The average power, on the other hand, would be calculated using the duty cycle information from the pulse waveform, and would be lower than the peak power. The proposed power detector detects the peak power of the input waveform.

of the calibration reference waveform. The minimum power detection refresh rate is the minimum allowable frequency at which the power detector returns an updated power reading. Taking the inverse of this rate, we find that the peak detector must be able to return an updated power measurement at least every 1ms.

2.2 Power Detector Implementation

Given the target specifications discussed in section 2.1, a power detector is proposed with the architecture as shown in figure 2.2. The input of the RF peak detector is the pulsed RF sine wave whose power should be detected. The input of the calibration (CAL) peak detector is an intermediate frequency continuous wave sinusoid of some known amplitude (calibrated against the known voltage reference V_{REF} derived from a bandgap reference). Assuming the peak detector outputs are completely insensitive to the frequency of the input, and only depend on the peak voltages of the input (as is the case for an ideal peak detector), then the peak detector outputs will match when the amplitudes of the input sine waves match, if the dc level of both sine waves is the same. Therefore, the loop compares the RF and calibration peak detector outputs and adjusts the calibration sine wave amplitude until the difference between the two peak detector outputs is minimized via successive approximation. The difference between the peak detector outputs will be minimized when the difference between the amplitudes of the IF calibration sine wave and the RF input signal is minimized. Thus, when the loop is settled and the error between these two amplitudes is minimized, the amplitude of the calibration sine wave stored as n-bits can be read, which is assumed to match the amplitude of the RF input sine wave. Finally, once the amplitude of the RF input signal is detected, the peak power of the RF sine wave can be found by using (2.3).

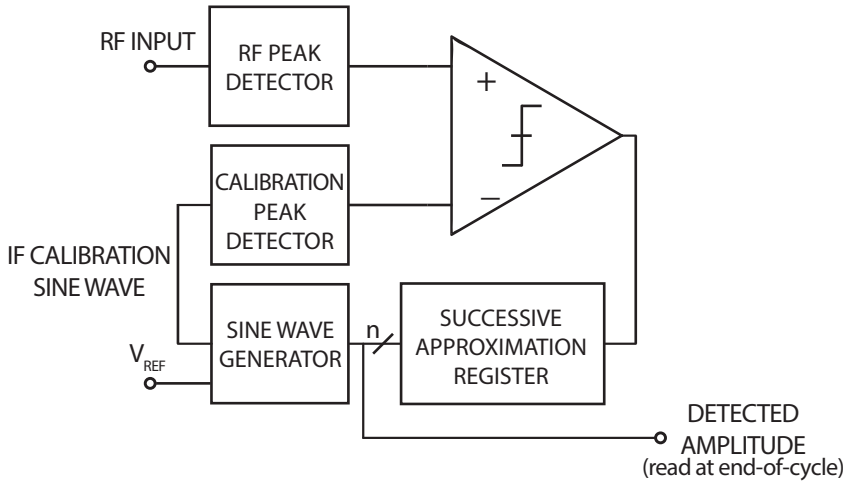


Figure 2.2: Block diagram of proposed power detector

2.2.1 Maximum Error Tolerance Analysis

In order to meet the maximum error tolerance of $\pm$0.5dB in the detected power, the error introduced in the power detection by each of the building blocks of the power detector should be budgeted accordingly. Figure 2.3 shows the block diagram of the power detector with ideal blocks and all of the major error sources moved to the outside of the blocks. $V_{E,SWG}$ is the error in the calibration sine wave amplitude relative to the ideal amplitude of this sine wave for a given digital word from the successive approximation register (SAR). $V_{E,QNT}$ is the quantization error from the successive approximation operation when the loop is in steady state. $V_{E,PD}$ is the summation of all of the errors introduced by the peak detectors (due to mismatch, voltage ripple, etc). V_{OFF} is the input referred offset of the comparator.

The error specification in power may be more useful if it is related to the amplitude difference between the RF input sinusoid and the calibration sinusoid. Assume that two sine waves have a peak power difference, ΔP, of 0.5dB (assuming 50-ohm loads). The

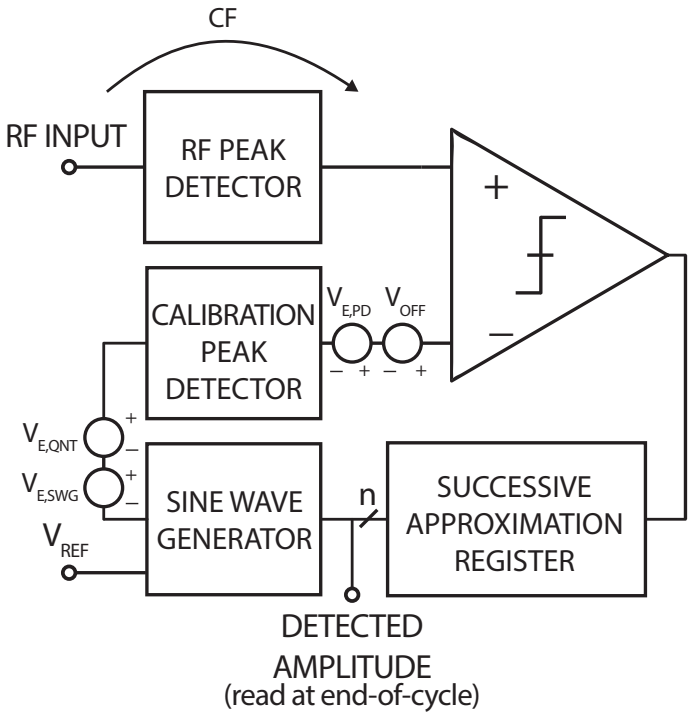


Figure 2.3: Block diagram of proposed power detector with major error sources

amplitude difference between the two sine waves can be determined as follows.

$$P_1 = 10log\left(10 \cdot A_1^2\right) \quad [dBm] \tag{2.4}$$

$$P_2 = 10log\left(10 \cdot A_2^2\right) \quad [dBm] \tag{2.5}$$

$$\Delta P = P_1 - P_2 \quad [dB] \tag{2.6}$$

$$= 10log\left(10 \cdot A_1^2\right) - 10log\left(10 \cdot A_2^2\right) \quad [dB] \tag{2.7}$$

$$= 10log\left(\frac{10 \cdot A_1^2}{10 \cdot A_2^2}\right) \quad [dB] \tag{2.8}$$

$$= 10log\left(\left(\frac{A_1}{A_2}\right)^2\right) \quad [dB] \tag{2.9}$$

$$= 20log\left(\frac{A_1}{A_2}\right) \quad [dB] \tag{2.10}$$

Solving (2.10) for A_1, it is determined that

$$A_1 = A_2 \cdot 10^{\left(\frac{\Delta P}{20}\right)} [V] \tag{2.11}$$

Then, solving (2.11) when $\Delta P = 0.5$, it is determined that

$$A_1 = A_2 \cdot 1.059 \tag{2.12}$$

When $\Delta P = 0.5$, A_1 is approximately 5.9% higher than A_2. It can be seen that at the smaller RF sine wave amplitudes (which of course occur at the smaller RF input power values), the difference between the calibration amplitude and RF amplitude must be smaller to meet the same $\pm$0.5dB maximum error specification. If the RF waveform power is -10dB, which corresponds to an amplitude of 100mV (again, assuming a 50-ohm load), it is found that the calibration waveform amplitude can be up to 5.9mV above the RF waveform amplitude or down to 5.59mV below the RF waveform amplitude for the the absolute value of the error in the power detection to remain less than 0.5dB.

Thus, it seems that the total error between the calibration waveform amplitude and the RF input amplitude should be less than 5.59mV in order to ensure that the power detection will be able to achieve the $\pm$0.5dB maximum error specification across the entire input power range. After 50-ohm matching, the total error between the calibration waveform amplitude and the RF input amplitude *at the PD inputs* should be less than $5.59mV \div 2 = 2.795mV$.

Obviously, the total difference in the amplitudes at the RF peak detector input and the calibration peak detector input arising from the four main error sources shown in figure 2.3 must be less than $2.795mV$. That is,

$$V_{E,total} = \frac{V_{E,PD} + V_{OFF}}{CF} + V_{E,SWG} + V_{E,QNT} \tag{2.13}$$

$$V_{E,total} \leq 2.795mV \tag{2.14}$$

where CF is the input amplitude to dc output voltage conversion factor of the peak detectors, described in more detail in section 3.2.

Assuming $A_{V,PD} = 0.8$, if $V_{E,PD} = 1mV$ and $V_{OFF} = 0.6mV$ then $V_{E,SWG} + V_{E,QNT} \leq 0.795mV$. If n=9, $V_{E,QNT} = 437.5\mu V$ and $V_{E,SWG} \leq 357.5\mu V$. 9 bits of resolution have been chosen to represent the calibration reference amplitude for this system as a balance between the quantization error and the cost and complexity of implementing additional bits.

2.2.2 Adjusting the Calibration Amplitude

The mechanism for adjusting the calibration amplitude based on the comparator decision has been defined as a successive approximation register. Another potential scheme would be to use a simple up/down counter to increase or decrease the amplitude of the calibration waveform based on the comparator output. For instance, if the comparator output is low, meaning the calibration amplitude is higher than the RF amplitude, then the counter should count down (decrementing the calibration waveform amplitude) until the comparator decision changes. The loop should reach a semi-steady state as the calibration amplitude is adjusted to within 1 step size of the RF amplitude. In theory, the comparator output would oscillate between HIGH and LOW every clock cycle after this point.

While straightforward to implement, this scheme does have its limitations. For one, the time required for the loop to reach a semi-steady state (and by extension the refresh period) may be relatively slow. As a useful example, imagine that a digital up/down counter is

chosen to increment the calibration amplitude based on the comparator decision. The minimum amplitude step size will be defined by the number of bits of the counter and the range of its output voltage. This minimum step size will be defined as the least-significant-bit (LSB), and is given by

$$LSB = \frac{A_{max} - A_{min}}{2^n} \ [V] \tag{2.15}$$

If n = 9, $LSB = 0.88 \ [mV]$.

This 9-bit counter will quantize the 450mV amplitude range into $2^9 = 512$ discrete steps of 0.88mV each. Assuming the power detection operation always starts with the calibration amplitude at the mid-point of the amplitude range, the counter could still require 255 steps to minimize the error between the calibration ampltiude and the input RF amplitude, which will take a fixed amount of time. After all, each counter increment or decrement will take a fixed amount of time (determined by the counter clock rate). Given the specification for the minimum power detection refresh rate (1kHz), the required clock rate of the counter can be determined. The period of the counter clock multiplied by the number of steps (times it must be clocked) in order to reach the minimum or maximum count value should be less than the maximum time allowed between power detection refreshes.

$$\frac{1}{f_{CK,counter}} \cdot (2^{(n-1)} - 1) \quad \leq \quad T_{refresh} \ [s] \tag{2.16}$$

where $f_{CK,counter}$ is the frequency of the counter clock, n is the number of bits in the counter, and $T_{refresh}$ is the period at which the power detector output is refreshed. Solving (2.16) for $f_{CK,counter}$, it can be determined that the clock counter frequency should be,

$$
\begin{aligned}
f_{CK,counter} &\geq \frac{1}{T_{refresh}} \cdot (2^{(n-1)} - 1) \quad [Hz] \\
&\geq f_{refresh} \cdot (2^{(n-1)} - 1) \quad [Hz] \qquad (2.17)
\end{aligned}
$$

where $f_{refresh}$ is the refresh rate of the power detector output, which should not be less than 1kHz according to the specifications listed in table 2.1. Substituting the number of bits and minimum refresh rate of the system into (2.17), it can be found that $f_{CK,counter} \geq 255\ [kHz]$. This means that the peak detector outputs must settle and the comparator must be able to reach a decision in less than $4\mu s$. While this constraint is not necessarily unfeasible, it does illuminate a design trade-off in the system: as the power detection refresh rate increases, the peak detector and comparator settling time must decrease, resulting in the need for more complex designs. While this design trade-off is inherent with most of the general topologies that implement the power detector functionality being discussed, an instant gain in power detection refresh rate or instant relaxation of the settling time requirements for the peak detectors and comparator can be acquired with a fairly simple change in the loop operation: rather than increment/decrement the calibration amplitude by the LSB each clock cycle, which could require up to 255 clock cycles, a successive approximation operation can be performed, which will minimize the error between the calibration and RF amplitudes in *just 10 clock cycles*.

The successive approximation operation still requires 9 bits to have the desired LSB, but it resolves one bit each clock cycle based on the comparator decision. Essentially, the calibration amplitude starts at the midpoint in the search range (the MSB is 1, all other bits are 0). If the comparator output during the first clock cycle is HIGH, the MSB will remain 1, and the next most-significant bit will switch to 1, putting the calibration amplitude at the midpoint of its previous value and the maximum value. On the other hand, if the

comparator output during the first cycle is LOW, the MSB will switch to 0, and the next most-significant bit will switch to 1, putting the calibration amplitude at the midpoint of its previous value and the minimum value. Therefore, in the first clock cycle, the successive approximation operation resolved the MSB (the decision to save the bit as a 1 or a 0 was made). In the same way, the successive approximation operation continues for nine more clock cycles, resolving the next-most-significant bit in each successive cycle.

The hardware required to implement a 9-bit successive approximation operation is comparable to that required to implement a 9-bit counter. A successive approximation register contains the logic required to take the information from the comparator ouput and implement the successive approximation algorithm. Therefore, a SAR and sine wave generator that can convert the bits from the SAR into a sinusoidal waveform with the correct amplitude are chosen to adjust the calibration waveform amplitude based on the comparator decision.

3. HYBRID RF POWER DETECTOR WITH CMOS PEAK DETECTORS

As a proof-of-concept system, a chip was fabricated with various CMOS peak detector structures, with the intention of completing the power detection loop off-chip. This ”hybrid” system, implementing the RF segments of the loop (the peak detectors) on-chip, and implementing all other loop blocks (the comparator, SAR, and sine-wave generator), off-chip, validates the successive approximation power detection scheme. This hybrid power detector also enables characterization of the CMOS peak detector performance as well as comparison of the loop operation using different peak detectors.

3.1 System Overview

The peak detectors are implemented on chip, while the off-chip portion of the hybrid power detector is realized using a combination of software and laboratory equipment. Given the flexibility of a software-based implementation, LabVIEW was chosen to function as the comparator and successive approximation register. Obviously, the hardware-software interfaces require analog-to-digital conversion and vice versa. Fortunately, the plethora of instrument drivers available for use with LabVIEW provides a simple solution: LabVIEW can read/write data from/to standard lab equipment, such as oscilloscopes and signal sources. In the hybrid power detector, an oscilloscope captures the analog peak detector output information and converts it to digital for processing in LabVIEW, while an RF signal source implements the sine wave generator. Figure 3.1 shows the block diagram of the hybrid power detector.

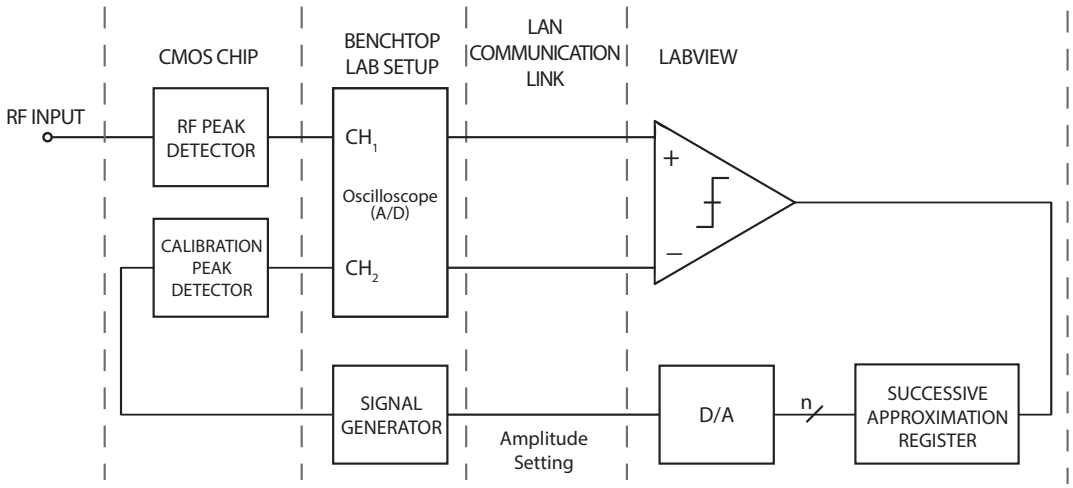


Figure 3.1: Block diagram of hybrid power detector

3.2 CMOS Peak Detectors

The peak detectors were implemented using a source-follower configuration with a capacitor at the output to hold the ”peak” value of the signal present at the gate. The peak detector schematic can be seen in figure 3.2, where C_1 serves as a dc blocking capacitor, while the dc voltage V_{G_BIAS} sets the dc level at the input of the peak detector. This dc level is set above the threshold voltage of M_1, V_{tn}, so that even small ac amplitudes at the input will produce a change in the output voltage. Assuming C_2 is initially completely discharged, when a voltage at the gate of M_1 exceeds V_{tn}, the transistor drain conducts current, charging C_2. As C_2 is charged, the output voltage, V_{out} rises. As V_{out} rises, $V_{gs} = V_g - V_{out}$ falls. Once V_{gs} falls below V_{tn}, the drain of M_1 stops conducting current, and V_{out} stops rising. Once the circuit reaches this steady state, C_2 has charged V_{out} to $V_g - V_{tn}$. The reason for *not* using a diode-connected transistor for M_1 is that designing a 50-ohm input impedance becomes more difficult when the impedance looking into the gate/drain of a diode-connected transistor is involved, versus the relatively high input impedance

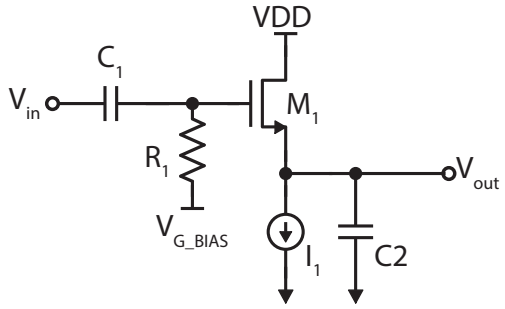


Figure 3.2: CMOS peak detector schematic

associated with the gate only. In this system, for example, a 50-ohm resistor hangs from the gate of the peak detector to ensure that the input impedance is 50-ohms. Note that R_1 should be large enough so to not affect the input matching.

The size of M_1 is constrained by the maximum frequency specification of the system. The 50-ohm output impedance of the previous stage and the parasitic capacitance at the input of the peak detector, C_p, form an RC lowpass filter which limits the peak detector's frequency of operation. As it is desirable to have a corner frequency at least 3 times higher than the maximum frequency of operation, the corner frequency for the peak detector would have to be $4\ [GHz] \times 3 = 12\ [GHz]$. Given the equation for corner frequency of an RC lowpass filter,

$$f_c = \frac{1}{2\pi RC} \quad [Hz] \tag{3.1}$$

and solving for C_p using the resistance and corner frequency values discussed previously,

$$C_p = \frac{1}{2\pi R f_c} \quad = \frac{1}{2\pi 50 \times 12 \times 10^9} \quad = 265 \quad [fF]$$

This means that the parasitic capacitance at the peak detector input should be less than $265[fF]$ to ensure that a 4GHz input signal is not attenuated significantly by the parasitic

filter. Such a small tolerance (at least in 180nm CMOS process nodes) for parasitics at the required operating frequencies for this application constrains M_1 to relatively small aspect ratios at close to minimum length in order to keep the parasitic capacitances of the device in the necessary range.

The value of the dc bias current I_1 will affect three key characteristics of the peak detector: ripple voltage, rise time, and the input amplitude to output dc conversion factor (CF). The peak detector rise time must be fast enough to reach the peak value (or sufficiently close to the peak value) during the minimum pulse width specified. In this case, that minimum pulse width occurs when the power amplifier being monitored is pulsed with a periodicity of $100ns$ at a 5% duty cycle. This equates to a pulse width of $5ns$, and therefore a rise time of less than $5ns$. The peak detector ripple and CF will both directly affect the accuracy of the power detector, particularly at low input power levels.

First, the impact of the value of I_1 on the peak detector rise time will be examined. As shown in figure 3.3 the voltage at the peak detector output takes some finite amount of time to settle as the output capacitor is charged. The relationship between the time required for the peak detector output to settle and the dc bias current can be mathematically cumbersome for hand analysis, and thus the dc bias current level decision based on the rise time requirement is best made with the help of simulation data. Figure 3.4 shows simulation results of the CMOS peak detector rise time for various bias currents with a $1pF$ output capacitor. Note that the dc bias current that supports a rise time in the $5ns$ range is close to $120\mu A$. The significance of this value will be seen once the ripple voltage is considered.

The peak detector ripple is defined as the difference between the maximum and minimum value of V_{out} when the peak detector output is in steady state. Figure 3.5 shows an example of the peak detector output voltage in steady state with some finite voltage ripple. Assuming a sine wave at the peak detector input, the voltage at V_{out} is a dc level with a

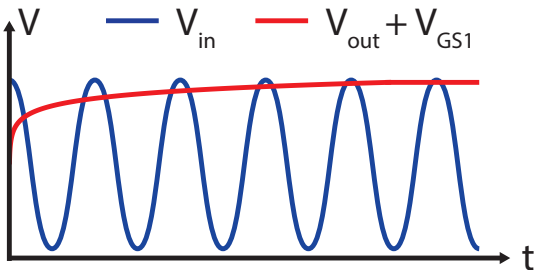


Figure 3.3: Conceptual graph of peak detector input and output transients depicting finite rise time of peak detector output

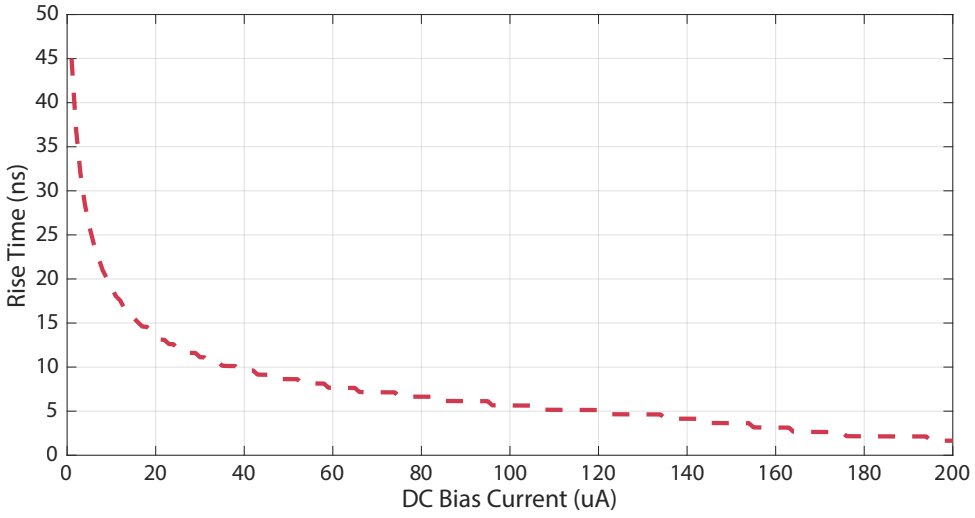


Figure 3.4: Simulation results of peak detector rise time versus dc bias current ($C_2 = 1pF$)

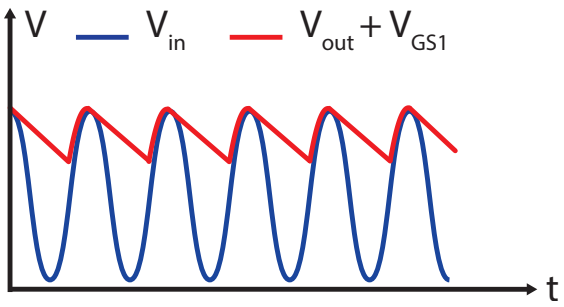


Figure 3.5: Conceptual graph of peak detector input and output transients depicting voltage ripple at peak detector output (when output is in steady state)

relatively small ac ripple. The output level "ripples" because the sinusoidal voltage at the gate of M_1 varies. Once the sine wave reaches its peak voltage, this voltage begins to drop, causing V_{gs} to fall below V_t, assuming C_2 was fully charged such that $V_{out} = V_{g,peak} - V_{tn}$ (the definition of steady state for the peak detector). I_1 now discharges the capacitor C_2. As the sine wave at the input of the peak detector approaches its peak value once again on its next cycle, $V_g - V_{out}$ will eventually exceed the threshold voltage, and the output capacitor will charge to the peak value again. This charge/discharge cycle will occur periodically at the rate of the input sine wave.

The value of the dc bias current directly impacts the voltage ripple at the peak detector output. Assuming the peak detector is in steady state, V_{out} is at its maximum value for the given input amplitude, and transistor M_1 has just turned off,

$$Q_{C2}(t) = C_2 V_{out}(t) \quad [C] \tag{3.2}$$

Given that current is charge per unit time,

$$I(t) = \frac{dQ(t)}{dt} \quad [A] \tag{3.3}$$

the derivative with respect to time can be taken of both sides of (3.2), and (3.3) can be

substituted in to arrive at

$$I_{C2}(t) = C_2 \frac{dV_{out}(t)}{dt} \quad [A] \tag{3.4}$$

Integrating both sides of (3.4), and dividing by C_2 yields,

$$\frac{1}{C_2} \int I_{C2}(t) = V_{out}(t) \quad [C] \tag{3.5}$$

Since $I_{C2} = -I_1$, which is a constant (dc) value with respect to time, (3.8) evaluates to

$$-\frac{I_1}{C_2} t + V_0 = V_{out}(t) \quad [C] \tag{3.6}$$

where V_0 is the output voltage at t=0, and $V_{out}(t)$ is the output voltage at time t. Solving for the difference $\Delta V_{out}(t) = V_0 - V_{out}(t)$, it is determined that

$$\Delta V_{out}(t) = \frac{I_1}{C_2} t \quad [V] \tag{3.7}$$

Thus, the output voltage will decrease linearly over time at the rate of $\frac{I_1}{C_2}$ volts per second. As stated previously, once the sinusoidal voltage at the input of the peak detector rises to its maximum again, the output capacitor will charge to V_0 once again. Therefore, the discharge cycle lasts approximately half of a single period of the sine wave input [14]. Therefore,

$$V_{ripple} = \Delta V_{out} = \frac{I_1}{2 C_2 f_{in}} \quad [V] \tag{3.8}$$

where f_{in} is the frequency of the sine wave at the peak detector input. Note that this is simply an approximation useful for initial hand-analysis, but is no substitute for consulting simulation data. The relationship described in (3.8) may be more useful if I_1 is solved for

in terms of V_{ripple}.

$$I_1 = 2V_{ripple}C_2 f_{in} \quad [A] \tag{3.9}$$

It can be proven that the ripple in the output must be less than $2.795mV$ to meet the $\pm 0.5dB$ error tolerance specification for the lowest (-10dBm) power level. In fact, the ripple and CF discussed here, the LSB error discussed in section 2.2.1, and the comparator offset all contribute to the total error in the power detection. Therefore, the maximum tolerable ripple is actually significantly less than $2.795mV$, but this value can serve as a ball-park value. Given the maximum tolerable ripple, it is insightful to choose a realistic value for C_2, choose f_{in} to be the minimum input frequency specified, and find out the maximum acceptable value of I_1. Choosing $C_2 = 1pF$, and given that the lowest input frequency is specified to be 2GHz, the maximum value of I_1 without exceeding the maximum tolerable ripple is found to be approximately $11.2\mu A$. That is an order of magnitude less than the minimum dc bias current necessary to support the required rise time! As can be seen, the ripple is proportional to $\frac{I_1}{C_2}$ while the rise time of the peak detector is *inversely* proportional to some nonlinear function of $\frac{I_1}{C_2}$. Seeing as how both of these parameters should be minimized to boost the performance of the power detector, the design trade-off between rise time and ripple becomes clear. In this case, it appears that a value of $\frac{I_1}{C_2}$ that satisfies both the rise time requirement and the ripple requirement *does not exist*. The implications of this will be discussed in section 3.5.

The input amplitude to output dc conversion factor of the peak detector is defined as

$$CF = \frac{\delta(V_{DC,ac\_on} - V_{DC,ac\_off})}{\delta V_{amplitude}} \tag{3.10}$$

where V_{DC,ac_on} is the dc output voltage of the peak detector when the input is an ac signal riding on top of some dc level, V_{DC,ac_off} is the dc output voltage of the peak detector when

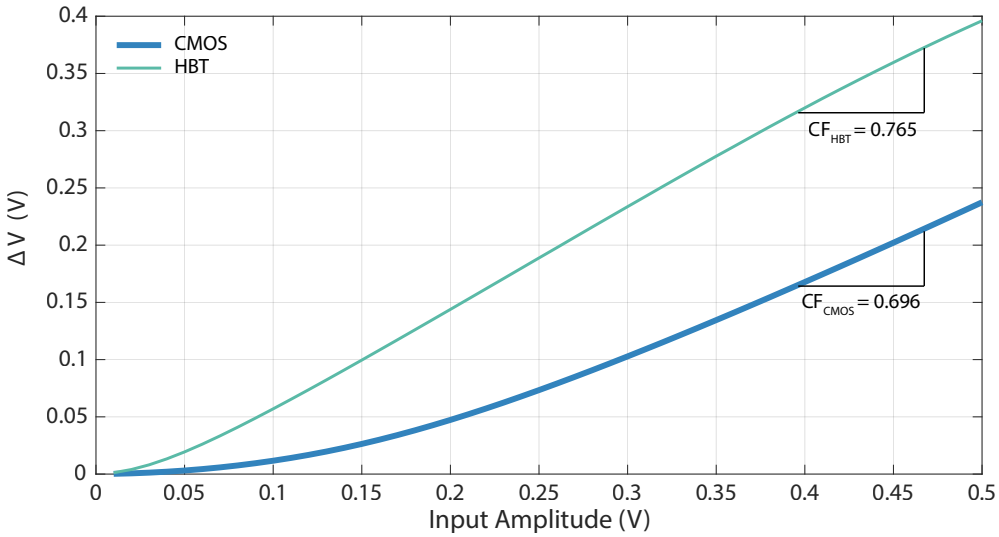


Figure 3.6: ΔV versus $V_{amplitude}$ ($C_2 = 1pF, f_{in} = 4GHz, I_1 = 30\mu A$)

the input is just the dc level with no ac signal, and $V_{amplitude}$ is the amplitude of the ac input signal. In other words, the is the gain of the relationship between the input amplitude and $\Delta V = (V_{DC,ac\_on} - V_{DC,ac\_off})$. Figure 3.6 shows the plot of ΔV versus $V_{amplitude}$ and the derivation of the conversion factor from this plot. Note that the relationship is not completely linear, but the gain is taken in the linear region of the plot as an approximation of the over the input amplitude range.

As the CF decreases (ideally it would be unity), the resulting amplitude difference at the peak detector inputs caused by the error sources at the peak detector outputs, namely $V_{E,PD}$ and V_{OFF}, increases. This can be seen in the total error equation in (2.13).

As can be seen, several design trade-offs are present in the design of the CMOS peak detectors. These trade-offs are highlighted in figure 3.7, where all three of the critical peak detector characteristics- rise time, ripple voltage, and CF- are plotted against a sweep of the dc bias current.

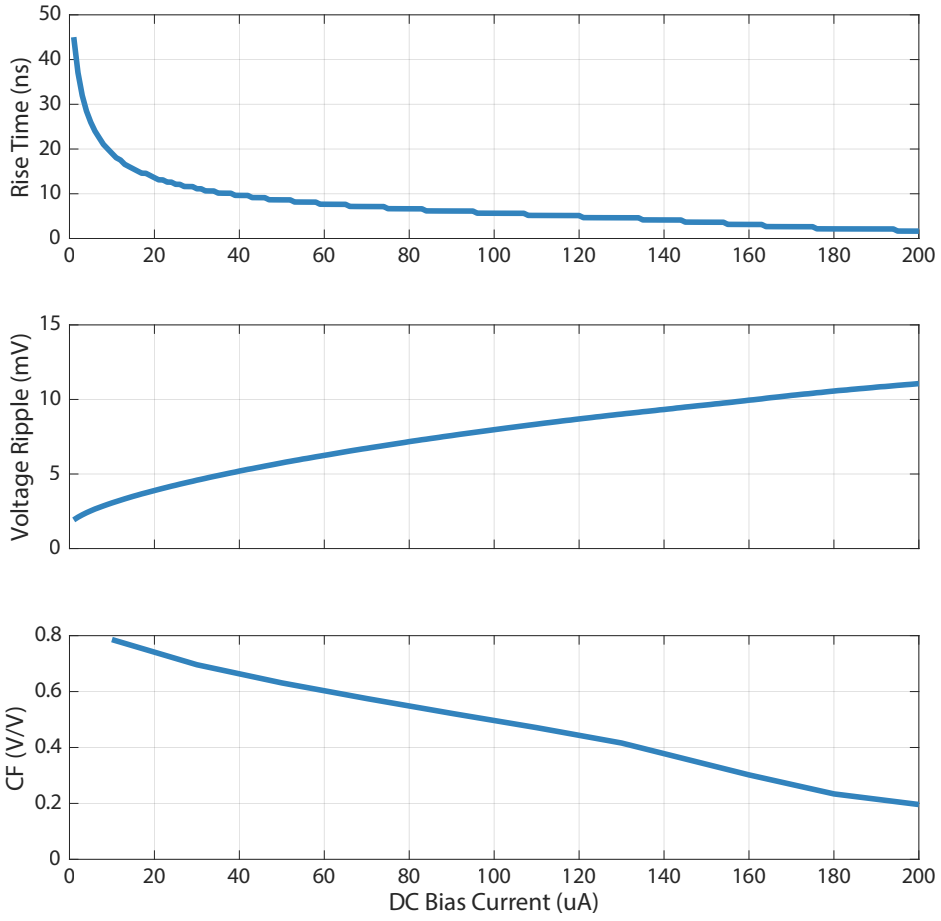


Figure 3.7: Peak detector rise time, ripple voltage, and CF versus dc bias current ($C_2 = 1pF, f_{in} = 2GHz$)

3.3 Layout and Fabrication

The CMOS peak detectors were fabricated in a 180nm SOI process. The chip layout can be seen in figure 3.8.

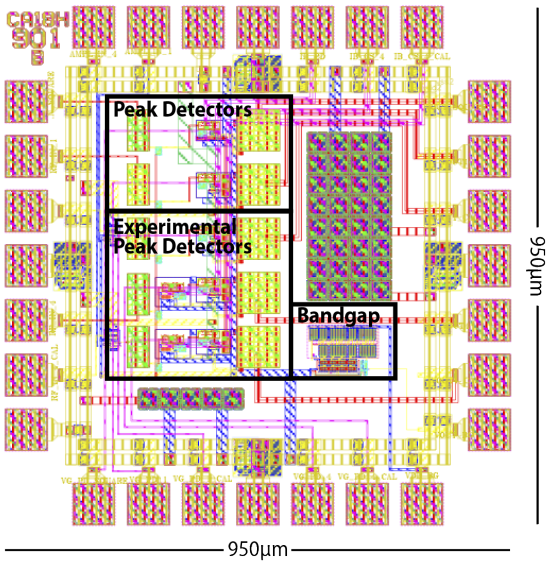


Figure 3.8: CMOS peak detector chip layout

3.4 System Results

Using the test setup shown in 3.1, measurement results were obtained by sweeping the input power to the hybrid power detector and observing the detected power. The detected versus input power plot is shown in figure 3.9. The error between the detected and input power is shown in figure 3.10. With the help of a calibration loop to remove dc offset in the CMOS peak detectors, along with averaging of the peak detector outputs, the $\pm 0.5dB$ maximum error tolerance specification was met over almost the entire 20dB dynamic range. Note that the dc bias current for the CMOS peak detectors was $120\mu A$ for the measurement results obtained. But it was discussed in section 3.2 that the bias current

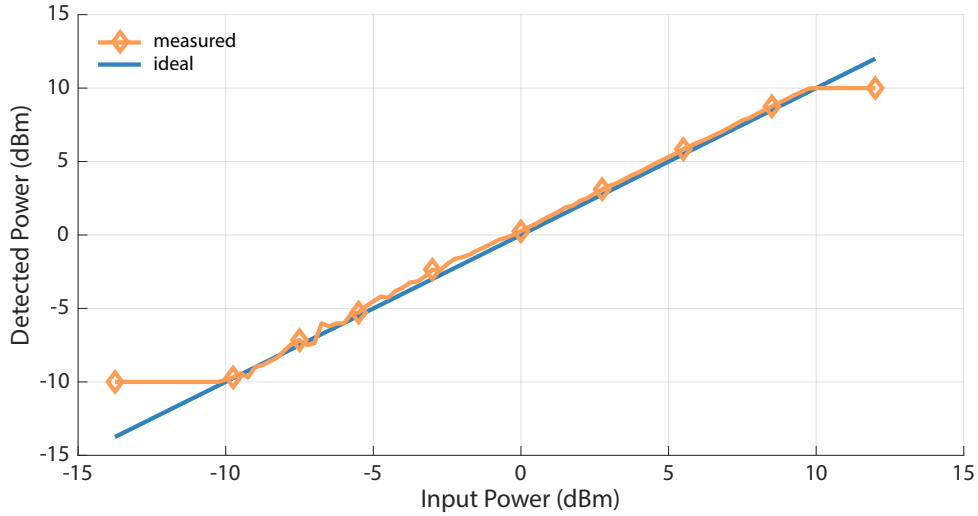


Figure 3.9: Detected power versus input power of hybrid power detector
($f_{in} = 100MHz,\ T_{p,pulse} = 2\mu s,\ T_{pw} = 1\mu s,\ I_1 = 120\mu A,\ C_2 = 20pF$)

would need to be much lower than this to ensure the voltage ripple did not exceed the maximum error specifications. The hybrid power detector manages to meet the error specification, even at the lowest power levels, by averaging many samples of the peak detector outputs so that the true dc value can be obtained, removing the ripple voltage error from the system. However, this averaging will decrease the power detection refresh rate, which must be considered if this technique is utilized in a fully integrated system.

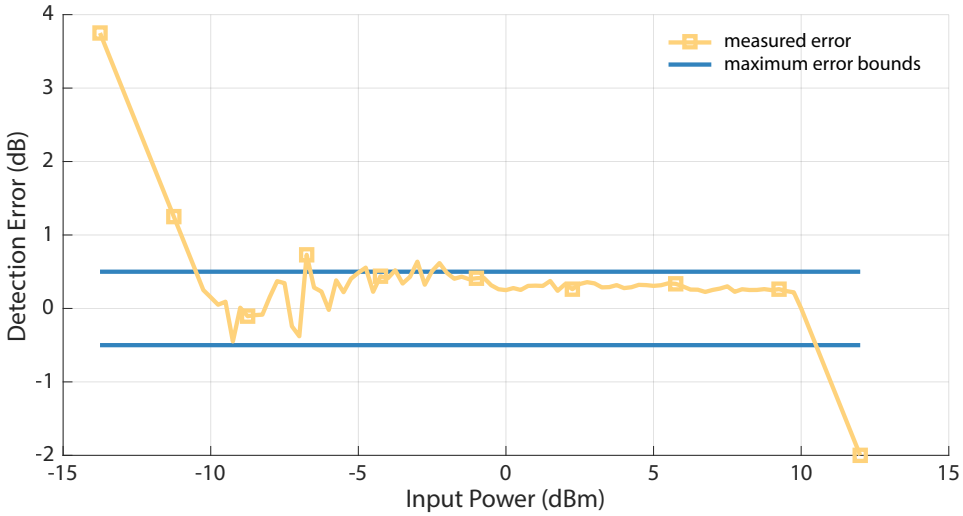


Figure 3.10: Detection error versus input power of hybrid power detector ($f_{in} = 100MHz,\ T_{p,pulse} = 2\mu s,\ T_{pw} = 1\mu s,\ I_1 = 120\mu A,\ C_2 = 20pF$)

3.5 System Limitations

The design trade-off between the peak detector rise time and ripple based on the value of $\frac{I_1}{C_2}$ was highlighted in section 3.2. The lack of a value for $\frac{I_1}{C_2}$ which can satisfy both the rise time and ripple requirements indicates that "faster" peak detectors with a faster rise time for a given $\frac{I_1}{C_2}$ are required. The CMOS peak detectors discussed in section 3.2 cannot meet the rise time and ripple requirements both. The f_t of this technology is not sufficient to perform reliable power detection in the $2 - 4GHz$ range with this particular architecture, which is why the results in section 3.4 were obtained for $f_{in} = 100MHz$. Despite these shortcomings, the hybrid power detector serves as a proof-of-concept for the proposed power detector topology and algorithm. The off-chip lab equipment also has minimum pulse width, maximum frequency, and communication-rate limitations which prevent testing of the system across the entire range of the target specifications listed in table 2.1. Despite these limitations, the intuition gained from the design of the CMOS

peak detector chip greatly aided in the design of the single-chip BiCMOS power detector discussed in the next section.

4. SINGLE-CHIP RF POWER DETECTOR WITH BIPOLAR PEAK DETECTORS

4.1 System Overview

As discussed in section 3.5, the CMOS peak detectors fabricated in the first version of the power detector could not support both the rise time and voltage ripple requirements necessary to meet the power detector system specifications. For this reason, heterojunction bipolar transistors (HBT) have been chosen to replace the inadequate CMOS transistors in the peak detectors. These HBTs have some favorable characteristics over the CMOS transistors, which will be explored more in section 4.2. While the power detector with bipolar peak detectors operates much the same as the power detector with CMOS peak detectors discussed in chapter 3, this updated system contains one important addition: the introduction of a timing circuit that will coordinate key events. Due to inherent constraints in the lab-based setup (LAN communication speeds and lab equipment limitations), the hybrid power detector was not operated at the target refresh rate (1kHz) or with the targeted minimum pulse width (5ns). This single-chip power detector, however, is designed to operate within all of the target specifications. As will be discussed in section 4.3, the pulse width and refresh rate specifications give rise to the need for the system timing circuit.

Figure 4.1 shows the block diagram of the single-chip power detector. By using the RF peak detector to convert the amplitude information of the RF input to a dc voltage early in the control loop, and ensuring that this amplitude to dc conversion does not depend significantly on the frequency of the input signal (for inputs below the cutoff frequency, of course), the necessary operating frequencies of the subsequent building blocks in the loop are greatly relaxed. For example, the sine wave generator produces a wave at a much lower frequency than that of the RF input, but because the amplitude-to-dc conversion is not dependent on the frequency of the input wave, the peak detector outputs will still match

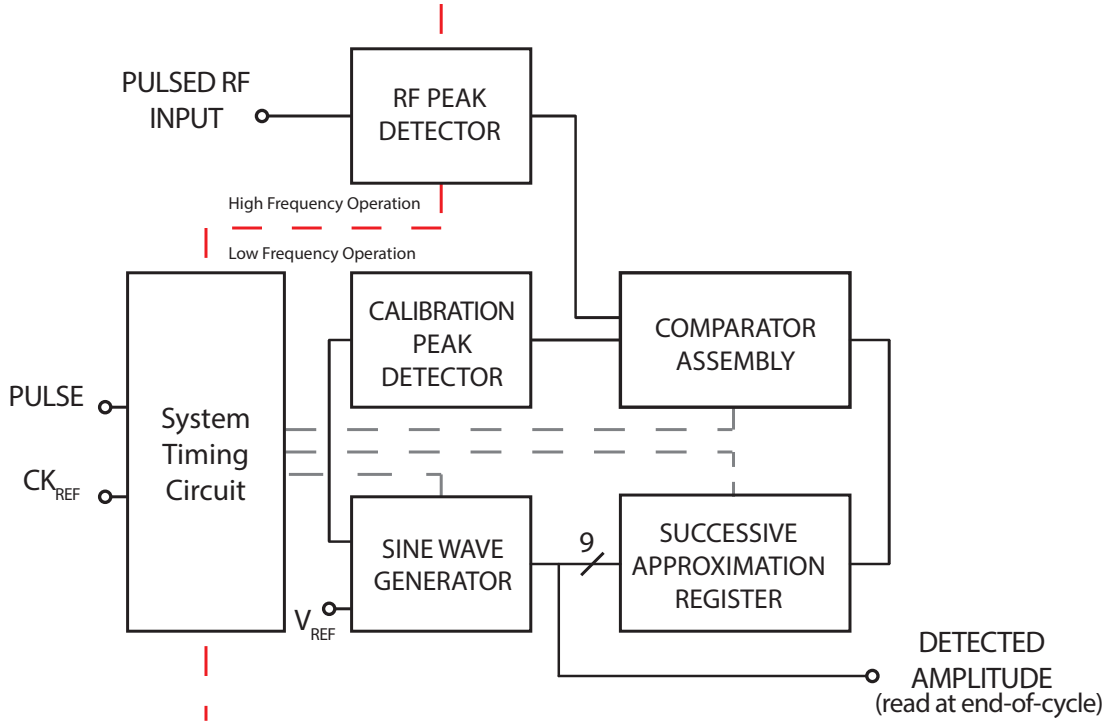


Figure 4.1: Block diagram of BiCMOS single-chip pulsed RF power detector

if the amplitudes of the inputs are equivalent. In fact, the power detector can theoretically operate at RF input frequencies as high as the RF peak detector will support, without making any changes to the rest of the system.

4.2 HBT Peak Detectors

The HBT peak detector utilizes the same topology as the CMOS peak detector discussed in section 3.2. The schematic of the HBT peak detector can be seen in figure 4.2. The design of the HBT peak detector is similar to that of the CMOS peak detector.

Comparing the performance of the HBTs against that of the CMOS transistors, figure 4.3 shows the rise time, voltage ripple, and CF simulations for both peak detectors over a sweep of the dc bias current.

As can be seen, the rise time of the HBT peak detector output is much faster than the

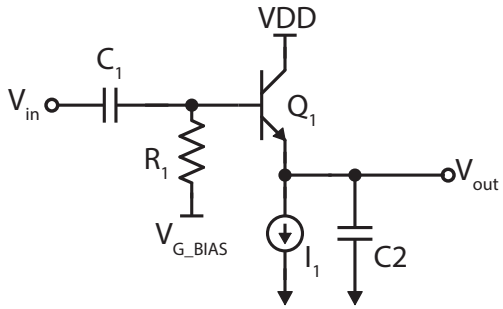


Figure 4.2: HBT peak detector schematic

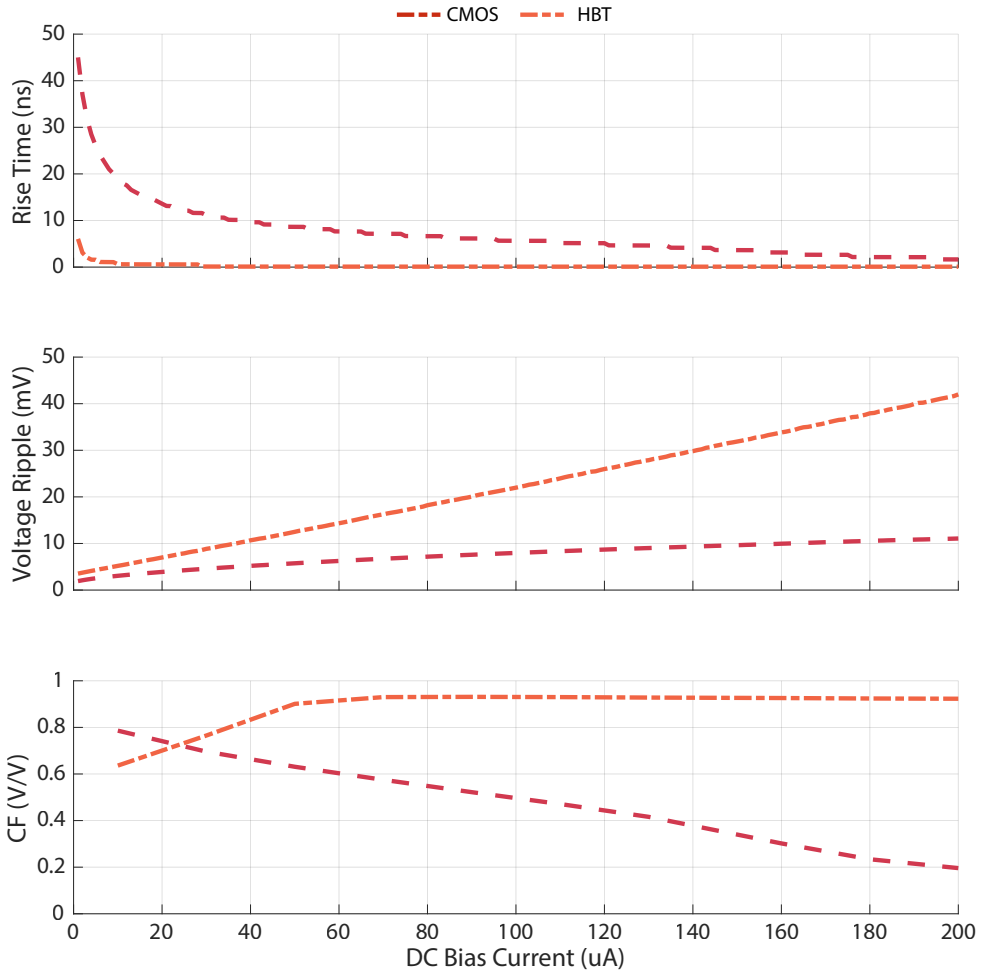


Figure 4.3: Peak detector rise time, ripple voltage, and CF versus dc bias current for HBT and CMOS transistors ($C_2 = 1pF,\ f_{in} = 2GHz$)

rise time of the CMOS peak detector output for a given bias current. And while the voltage ripple of the HBT is significantly larger than that of the CMOS transistor for a given bias current, the simulated voltage ripple of the HBT peak detector actually matches the approximate expression in (3.8) much more closely than the simulated voltage ripple of the CMOS peak detector does. Finally, the HBT peak detector's CF increases with increasing bias current (until it saturates at around 0.93 V/V) while the CMOS peak detector's CF *decreases* with increasing bias current. The order of the improvement in rise time far exceeds the small degradation in ripple voltage, overall, and the conversion factors of both peak detectors are comparable at the dc bias currents that support the required ripple voltage and rise times.

Note that the power detector system uses two peak detectors: one RF peak detector and one calibration peak detector. Because the sinusoid at the input of the calibration peak detector is a lower frequency than the sinusoid at the input of the RF peak detector, the voltage ripple will be greater at the output of the calibration peak detector than at the output of the RF peak detector. This could introduce significant power detection error, so the calibration peak detector must be modified to reduce its voltage ripple to the same value as the RF peak detector's voltage ripple. Considering the approximate expression for the voltage ripple values for both peak detectors,

$$V_{ripple,RF} = \frac{I_1}{2C_{2,RF}f_{in,RF}} \quad [V] \tag{4.1}$$

$$V_{ripple,CAL} = \frac{I_1}{2C_{2,CAL}f_{in,CAL}} \quad [V] \tag{4.2}$$

Now equating the voltage ripples of both peak detectors,

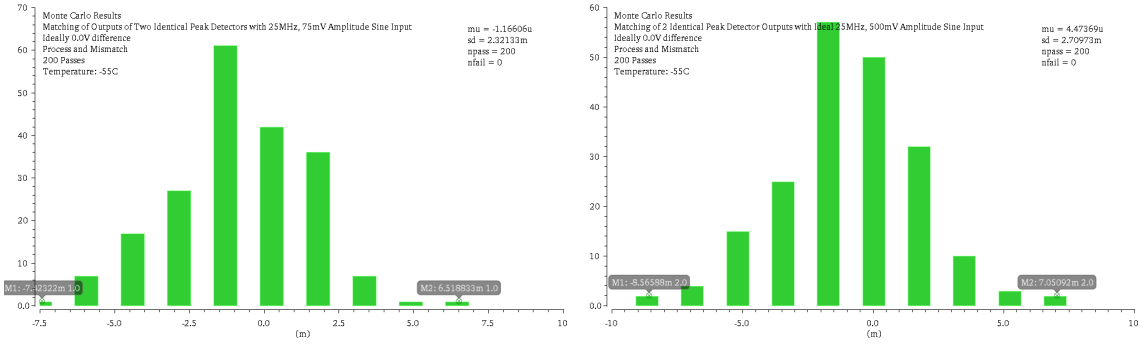
$$\frac{I_1}{2C_{2,CAL}f_{in,CAL}} = \frac{I_1}{2C_{2,RF}f_{in,RF}} \quad [V]$$

$$C_{2,CAL}f_{in,CAL} = C_{2,RF}f_{in,RF}$$

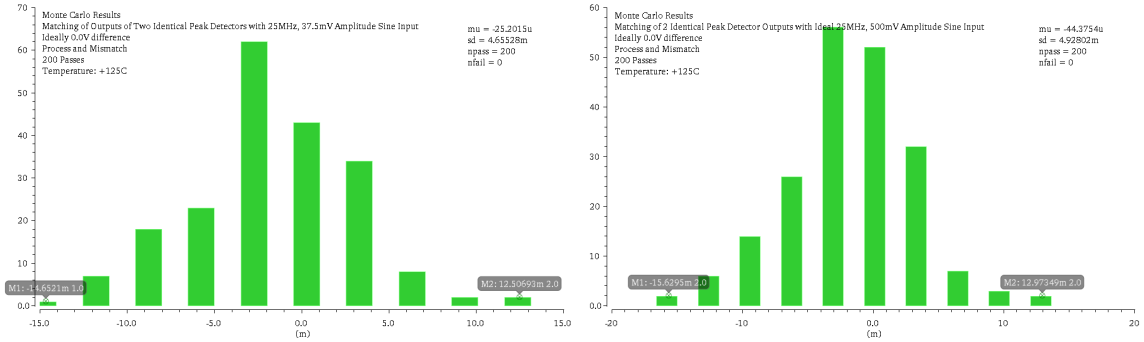
$$C_{2,CAL} = C_{2,RF}\frac{f_{in,RF}}{f_{in,CAL}} \tag{4.3}$$

Thus it can be seen that if the capacitance at the output of the calibration peak detector is scaled relative to the RF peak detector's output capacitance by the ratio of $\frac{f_{in,RF}}{f_{in,CAL}}$, then the voltage ripple at the output of both peak detectors will be equivalent. Other than the voltage ripple, the only other parameter the size of the output capacitor affects is the peak detector's rise time. Increasing the output capacitance increases the rise time. The calibration peak detector is detecting the peak of a continuous wave signal, and thus does not share the same rise time requirement as the RF peak detector. However, both peak detector outputs should be settled before the comparator makes a decision. This means that the rise time of the calibration peak detector will affect the amount of time it takes for each single bit in the binary search to be resolved, thereby impacting the refresh rate of the system. The RF peak detector also must be sampled by the comparator when its output is settled *and* the calibration peak detector output is settled. These conditions warrant the implementation of a timing circuit to ensure all of the key loop operations are occurring at the proper time. This timing circuit will be discussed in section 4.3.

Matching between the peak detector outputs for a given input amplitude is critical to ensure that the power detection is accurate. Thus, to verify the peak detector matching, Monte Carlo simulations were run, monitoring the peak detector outputs for the same 25MHz sinusoidal input. Figure 4.4 shows the error between the peak detector outputs for different temperature and input amplitude configurations.



(a) $f_{in} = 25MHz$, $T = -55°C$, $A = 37.5mV$ (b) $f_{in} = 25MHz$, $T = -55°C$, $A = 500mV$



(c) $f_{in} = 25MHz$, $T = +125°C$, $A = 37.5mV$ (d) $f_{in} = 25MHz$, $T = +125°C$, $A = 500mV$

Figure 4.4: Matching between outputs of identical peak detectors over 200 monte carlo process variation and mismatch passes

4.3 System Timing Circuit

The system timing circuit sets the clock speed of the successive approximation register and the sampling of the peak detector outputs. This circuit dynamically balances two key operations: (1) ensuring that the calibration peak detector output has enough time to settle before being sampled and (2) ensuring that the system refresh rate specification is met over the entire pulse period range.

The necessity of this circuit is best demonstrated by reasoning through the timing of the various operations of the power detector. First, the RF peak detector output must be sampled on the falling edge of the pulse signal. This is because (1) the peak detector output should to be given the maximum amount of time possible to settle (this is especially critical for a 5ns pulse width) and (2) the peak detector output voltage begins to fall quickly after the RF input signal is pulsed off. Thus, at the minimum pulse period, the peak detector output would be re-sampled every 100ns. The comparator output likely cannot reach a decision in 100ns, nor can the calibration peak detector output settle in this time (remember the output capacitance is $\frac{f_{in,RF}}{f_{in,CAL}}$ times larger than the output capacitance of the RF peak detector).

The following analysis demonstrates why the frequency of the pulse signal cannot simply be divided by a fixed value in order to allow the calibration peak detector and comparator outputs ample time to settle. From simulations it can be seen that the calibration peak detector needs about $4\mu s$ to settle adequately. The comparator is resolving a decision from sampled values of the previous peak detector outputs during this time, so the system will operate properly if the SAR is clocked every $4\mu s$. The divided pulse period then needs to be,

$$\frac{f_{pulse}}{x} = \frac{1}{4\mu s}$$

Solving for the divisor necessary to satisfy this equation, x, it can be found that

$$x = f_{pulse} \cdot 4\mu s$$

Assuming the pulse period is $100ns$ ($f_{pulse} = 10MHz$), $x = 40$. Rounding up to the nearest power of 2 to keep the frequency divider design simple gives a divisor of 64. Thus, at a 10MHz pulse rate, the SAR will clock every $64 \cdot 100ns = 6.4\mu s$. Because the system needs to clock the SAR 10 times in order to resolve all 9 bits and reach the end-of-cycle (EOC), the power detection refresh period is,

$$T_{p,refresh} = 10 \cdot 6.4\mu s = 64\mu s$$

This is well below the maximum period of $1ms$. Next consider when the frequency of the pulse signal is at its minimum, 50kHz. In this case the divided pulse period at which the SAR is clocked is $20\mu s \cdot 64 = 1.28ms$. The time required just to resolve a single bit of the successive approximation is greater than the maximum refresh period! In fact, with a pulse frequency of 50kHz, dividing the pulse frequency is completely unnecessary, as the SAR would be clocked every $20\mu s$ if the undivided pulse signal was used.

It is precisely this problem that leads to the requirement of a *dynamic* SAR clock speed based on the pulse rate. This is exactly what the addition of the system timing circuit enables. Essentially, when the pulse frequency is high, the division factor is highest (64). Then, as the pulse frequency drops, the division factor drops also at discrete intervals, first to 16, then to 4, and finally to 1 (no division) at the lowest pulse frequencies. Refer to the block diagram of the system timing circuit shown in figure 4.5 and the block diagram of the SAR clock generator shown in figure 4.6 for the ensuing dicsussion.

The system timing circuit performs its task by counting the number of pulses in a certain time period (using a slow, 50kHz reference clock). Then the circuit passes the pulse

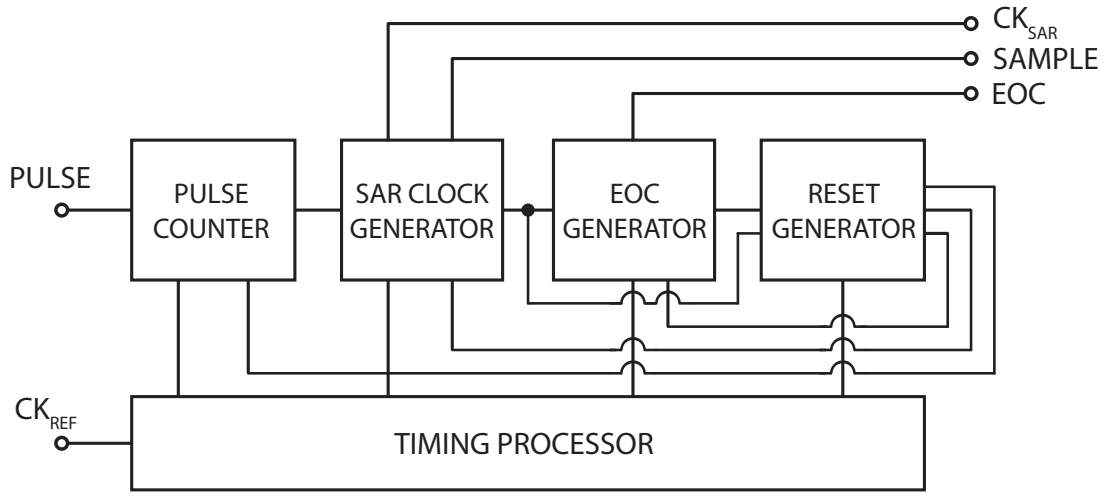


Figure 4.5: Block diagram of system timing circuit

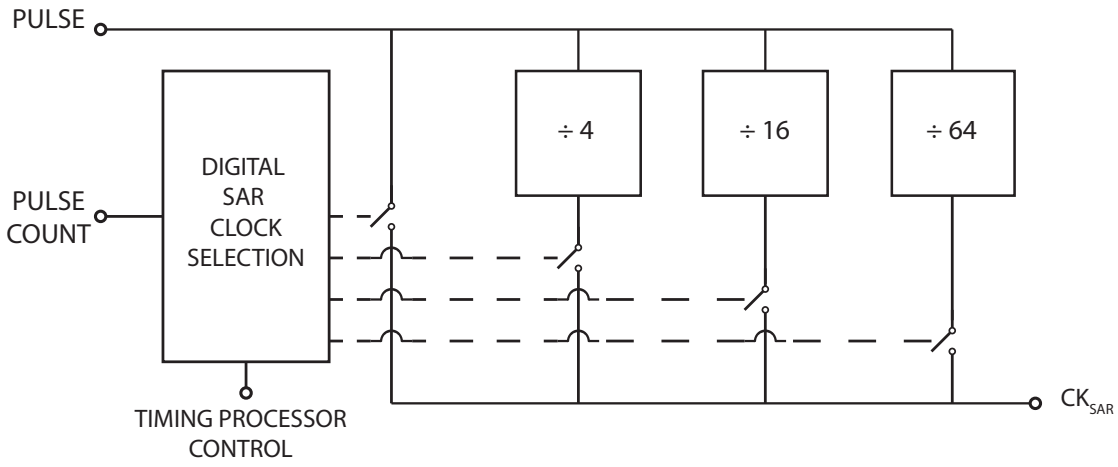


Figure 4.6: Block diagram of the SAR clock generator

count information to the SAR clock generator, which makes a decision on which division factor to use based on the pulse count information received from the pulse counter. The EOC generator counts the number of times the SAR has been clocked to generate an end-of-cycle (EOC) signal that indicates when the amplitude reading (the 9 bits output from the SAR) should be read. Upon receiving the EOC signal, the reset generator outputs all of the necessary signals to reset the various counters and digital logic and to indicate to the SAR when to switch to the division factor decided upon (this ensures that the SAR clock rate does not change in the middle of a cycle). The system timing circuit also generates the signal that triggers the comparator to begin making a decision. This ensures that the comparator only makes a decision based on settled peak detector outputs.

4.4 Comparator Assembly

The comparator assembly compares the output of the RF peak detector with the output of the calibration peak detector and sends the decision to the SAR. The block diagram of the comparator assembly is shown in figure 4.7. Conceptual transient waveforms of the comparator assembly are shown in figure 4.8.

As expressed in section 4.3, the RF peak detector output must be sampled on the falling

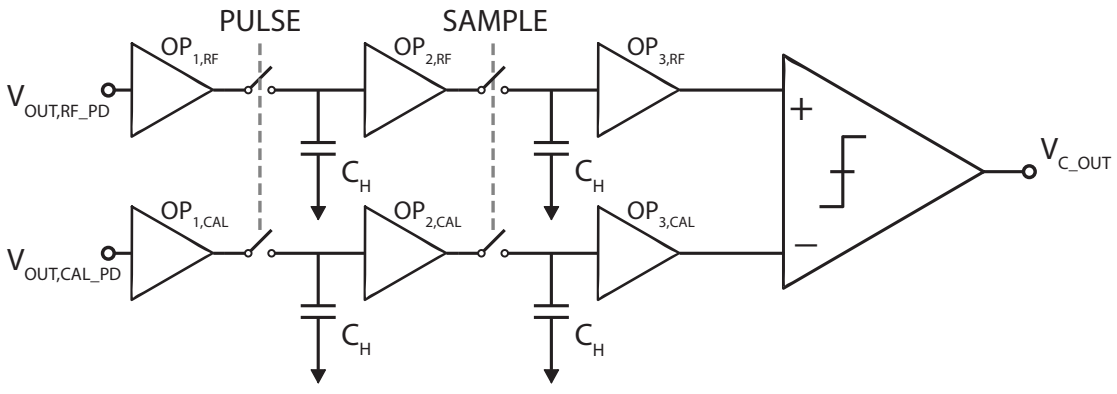


Figure 4.7: Block diagram of the comparator assembly

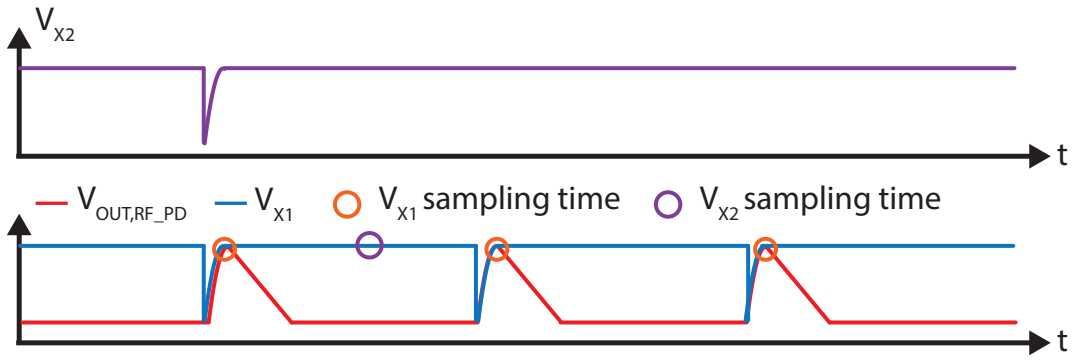


Figure 4.8: Conceptual transient response of the comparator assembly

edge of the pulse signal. However, the comparator needs a stable signal at its input for the entire time it is resolving a decision, which takes longer than the minimum pulse period of 100ns. Therefore, just like the SAR, the comparator must utilize dynamic clock rates as well to ensure proper operation across the entire pulse period range.

As shown in 4.8, the sample and hold at the output of the peak detector holds the output on the falling edge of the pulse signal. Because this sample and hold will continue to sample at the pulse rate, an additional sample and hold with a longer hold time (relative to the pulse rate, but dynamically set to stay around $4\mu s$) is required to maintain a stable signal at the comparator input as a decision is made. The first set of buffers ensure that the peak detector output is not loaded by the first sample and hold. The following two sets of buffers prevent charge injection effects from distorting the sample.

A single sample and hold that samples the RF peak detector output a single time and holds it until the comparator has reached a decision will introduce some system error due to the finite propagation delay between the time the pulse at the peak detector input turns off and the time the output is sampled. In order to implement a sample and hold with an additional condition, such as ”hold until the calibration peak detector output is settled”, the $\overline{PULSE}$ signal would have to be fed through some additional digital logic such as a

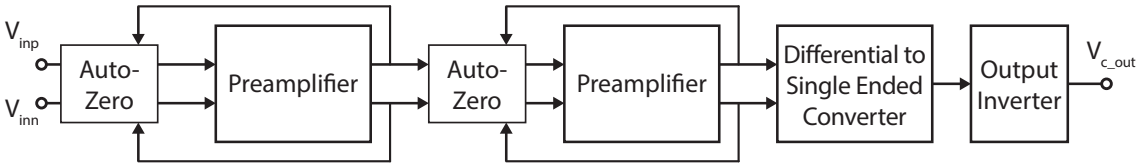


Figure 4.9: Block diagram of the dual auto-zero comparator

D flip flop, which would increase the delay between the pulse being turned off at the peak detector input and the sample being taken at the peak detector output. The peak detector output capacitor discharges relatively quickly due to the small capacitance value chosen to meet the rise time requirement. Thus, the propagation delay between the pulse being turned off at the peak detector input and the sample being taken at the peak detector output should be minimized, which leads to the two-stage sampling scheme shown in 4.7.

The comparator, shown in figure 4.9, is designed to have very low offset voltage through a dual auto-zero technique. Essentially, the offset of the preamplifier stages are sampled and subtracted from the input. Then the comparator converts the differential signal to a single-ended signal and drives it to the rail with the output inverter.

The schematic of the auto-zero circuit is shown in figure 4.10. During CK the auto-zero circuit samples the offset of the preamplifier A_1. Then during $\overline{CK}$ the auto-zero circuit sums the negative offset to the input, canceling it. Of course there is still some residual offset remaining due to the finite gain of the preamplifier, but the addition of the second auto-zero stage increases the gain, reducing this error further.

The schematic of the preamplifier is shown in figure 4.11. The preamplifier is a fully differential stage which uses a small amount of positive feedback to increase the gain. This will help decrease the input-referred offset of the blocks further down the line. This positive feedback is implemented in a pair of cross-coupled transistors. Both branches also include a diode-connected transistor to ensure that this positive feedback does not make

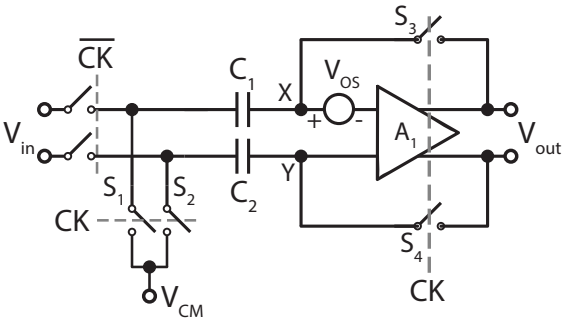


Figure 4.10: Schematic of the auto-zero circuit

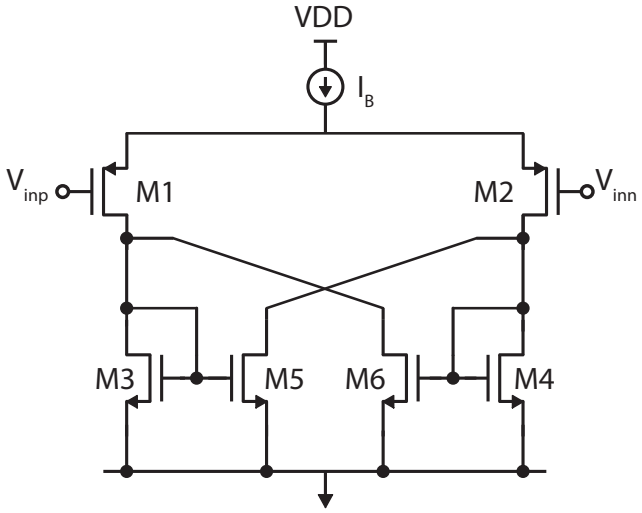


Figure 4.11: Schematic of the preamplifier

the preamplifier unstable during the auto-zero phase. This block provides a gain of about 10V/V.

Figure 4.12 shows the schematic of the differential to single ended converter. This circuit is a simple differential pair loaded by a current-mirror.

Table 4.1 shows the simulated parameters of interest for the dual auto-zero comparator.

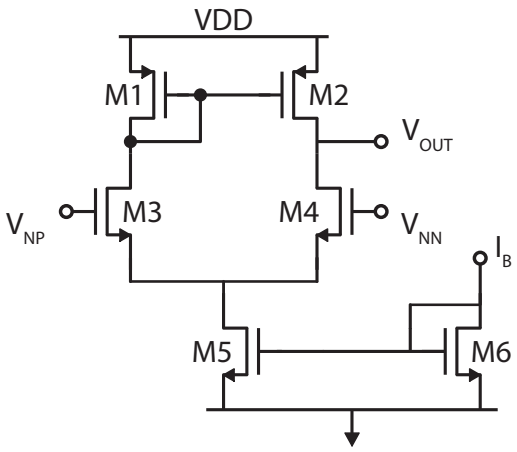


Figure 4.12: Schematic of the differential to single ended converter

Parameter	Value
Maximum Input Referred Offset	600μV
Maximum Decision Time	120ns
Power Consumption	2.76mW
Common-mode Input Range	100mV - 900mV

Table 4.1: Dual auto-zero comparator parameters of interest

4.5 Successive Approximation Register

The schematic of the successive approximation register is shown in figure 4.13. The top row of D flip flops propogates a logical one to the next flip flop every clock cycle, resetting to logical zero after passing the one [15]. This top row acts as the controller, ensuring that each bit from the MSB down to the LSB is "tested" successively. The bottom row of D flip flops store the output bits of the SAR, storing a logical one if the comparator output was HIGH (meaing the calibration amplitude needs to go higher), or changing the bit to 0 if the comparator output was LOW (meaing the calibration amplitude needs to go lower). Note that in this system a 9-bit SAR was used.

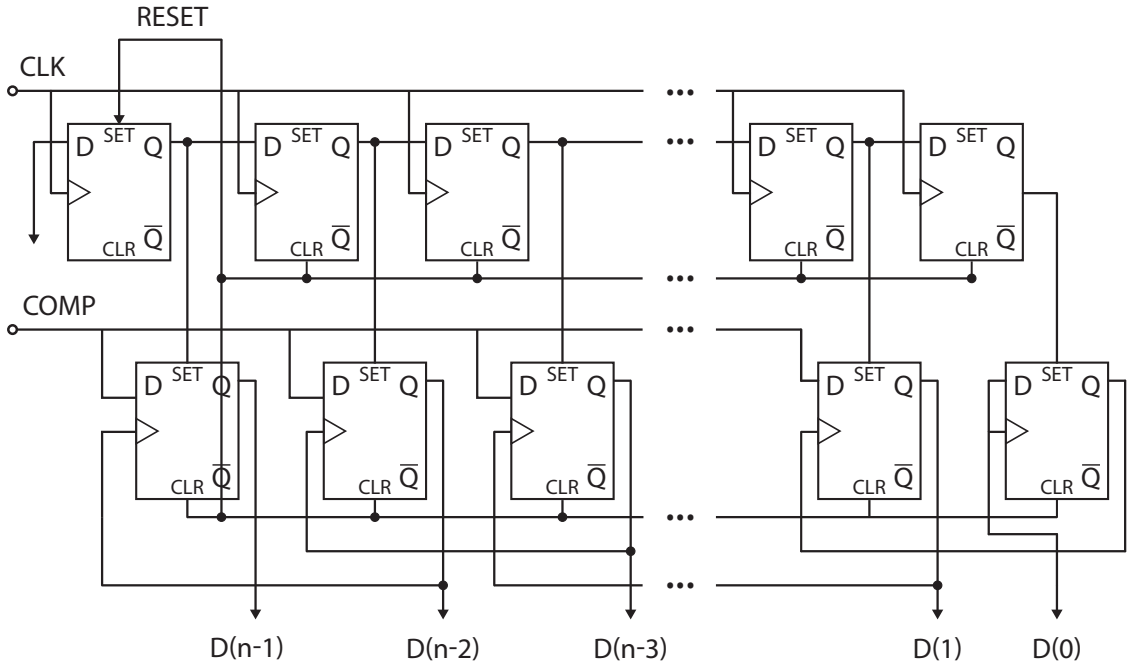


Figure 4.13: General schematic of the successive approximation register

4.6 Sine-Wave Generator

The schematic of the sine wave generator is shown in figure 4.14. The sine wave generator creates a sinusoidal waveform using $n_{pts} = 2 \cdot m$ discrete levels per period. In this design, $n_{pts} = 8$. Transistors M_1 through M_m are sinusoidally weighted according to the expression,

$$nf_{Mi} = \frac{nf_{total}}{2}\left[sin\left(\frac{2\pi i}{n_{pts}} - \frac{\pi}{2}\right) - sin\left(\frac{2\pi(i-1)}{n_{pts}} - \frac{\pi}{2}\right)\right] \tag{4.4}$$

where nf_{Mi} is the number of fingers of transistor Mi and $(1 \leq i \leq m)$. This expression requires that the number of fingers be rounded to the nearest integer, and then the designer must ensure that the desired total number of fingers is preserved ($nf_{M0} = nf_{M1} + nf_{M2} + ... + nf_{Mm}$). Note that in reality cascode current mirrors were used to reduce the effect of the varying gate-drain voltage on the drain currents.

The D flip flop based Johnson counter generates the proper control signals to connect the transistors to the summing resistor with the proper pattern. The variable current source sets the maximum current drawn through R_{SUM}, which controls the amplitude of the sine wave. The transistor-level schematic of the variable current source (essentially a DAC controllable via the 9 bits from the SAR) is shown in figure 4.15. Note that the negative feedback loops using the opamps set the low (all bits zero) voltage level and the middle (most significant bit one, all others zero) voltage level of the DAC, relative to a bandgap reference voltage. Transistors M_1 through M_n are binary weighted. Note once again that cascode current mirrors are employed here, though these are not shown in the schematic for the sake of clarity.

Simulations of the sine wave generator output waveform can be seen in figure 4.16. Monte Carlo analysis of variation in the sine wave generator output amplitude (peak-to-peak) over process variations, mismatch, and temperature is shown in figure 4.17.

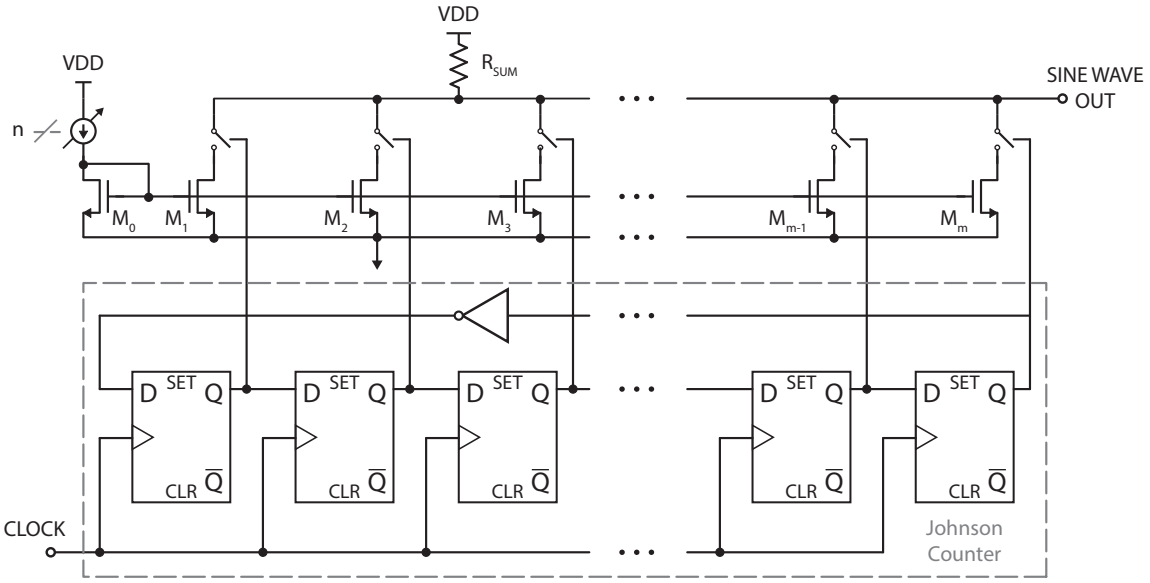


Figure 4.14: General schematic of the sine wave generator

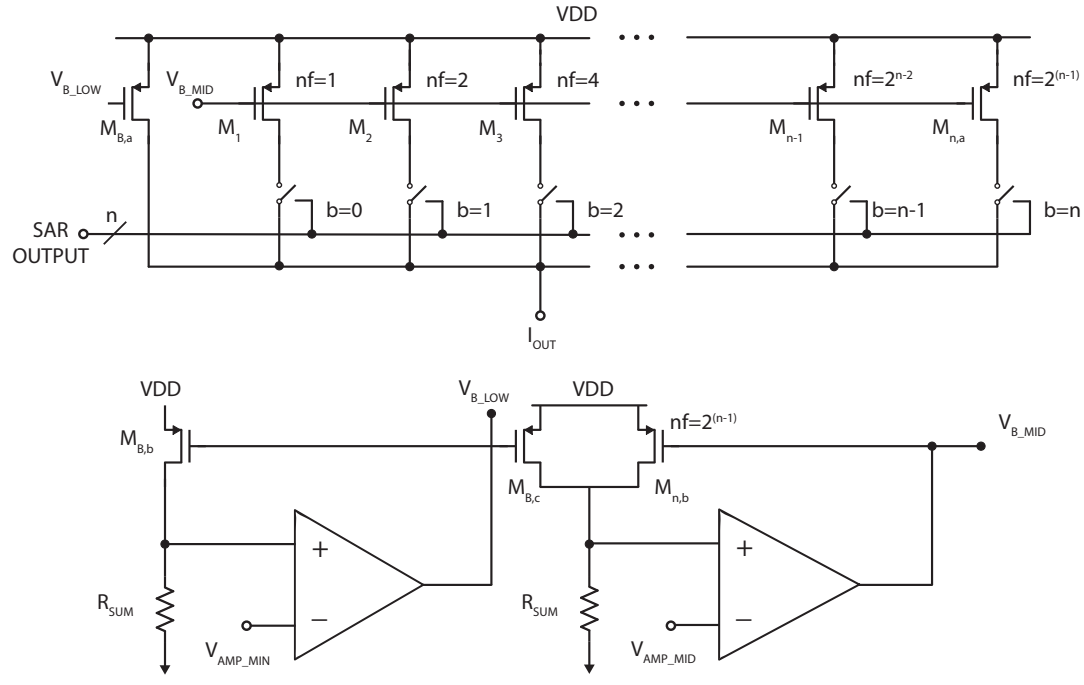
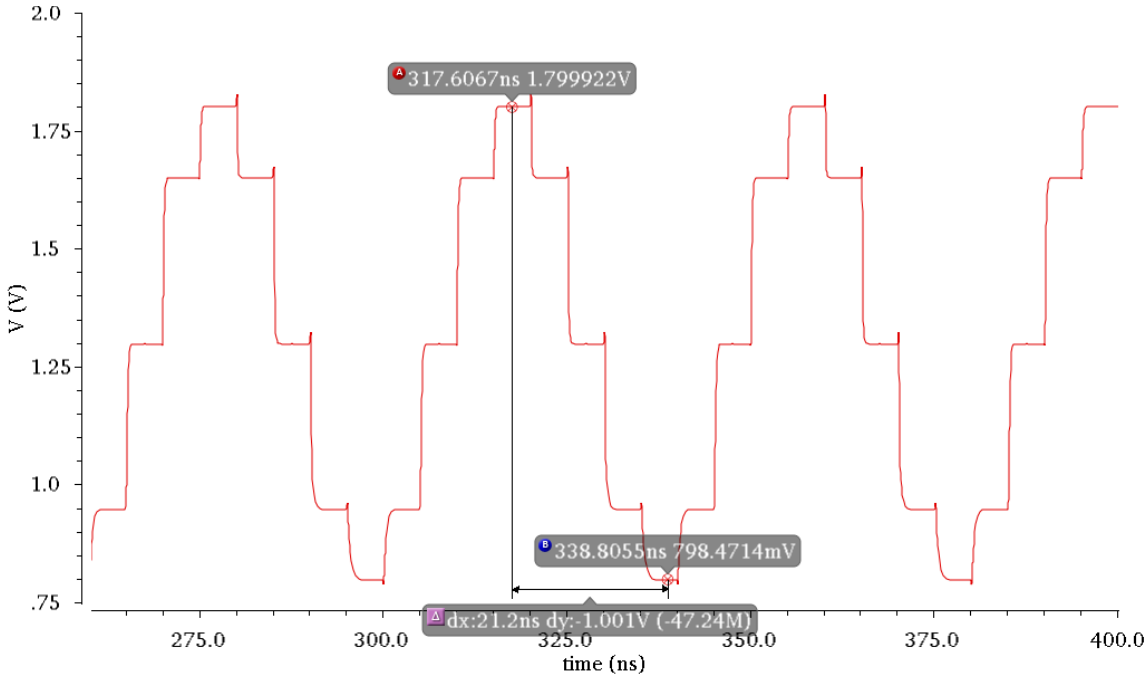
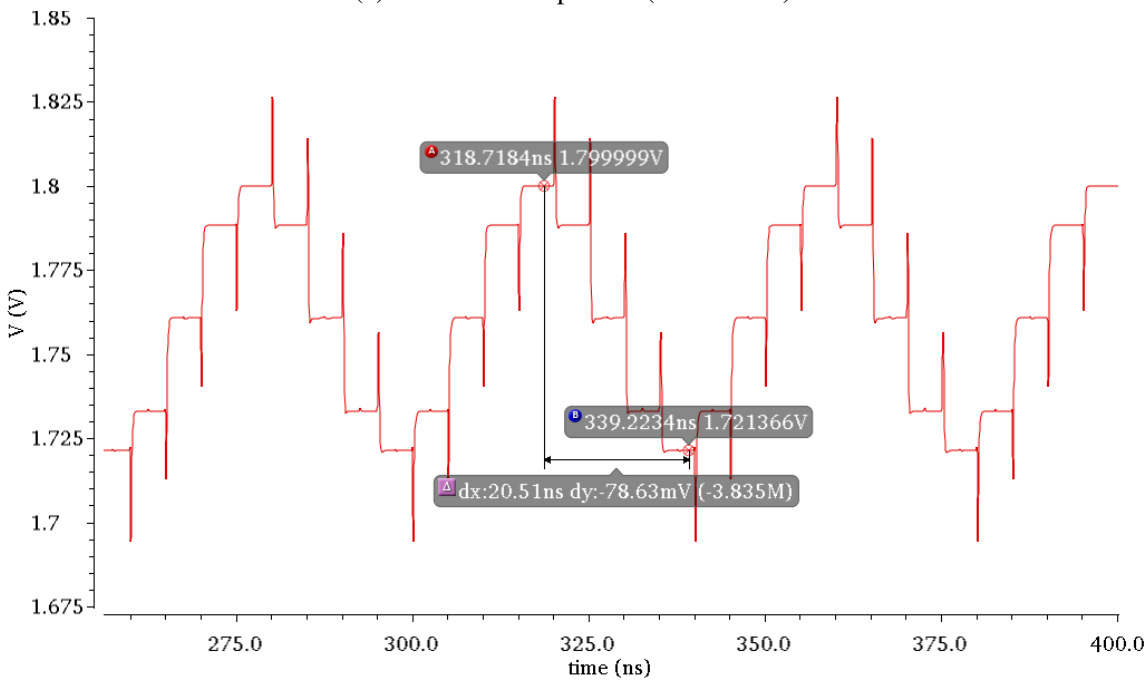


Figure 4.15: General schematic of the variable current source (DAC)

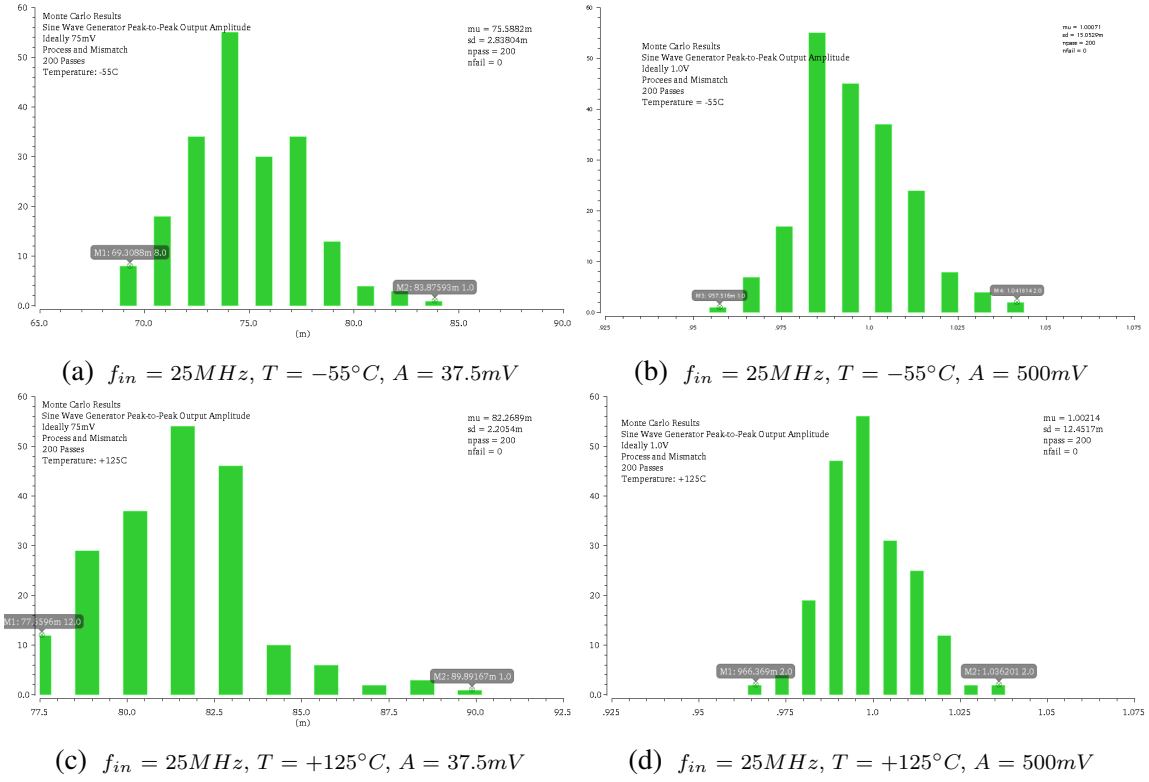


(a) Maximum amplitude (all bits one)



(b) Minimum amplitude (all bits zero)

Figure 4.16: Simulations showing sine wave generator output waveform



(a) $f_{in} = 25MHz$, $T = -55°C$, $A = 37.5mV$

(b) $f_{in} = 25MHz$, $T = -55°C$, $A = 500mV$

(c) $f_{in} = 25MHz$, $T = +125°C$, $A = 37.5mV$

(d) $f_{in} = 25MHz$, $T = +125°C$, $A = 500mV$

Figure 4.17: Variation in the sine wave generator output peak-to-peak amplitude over 200 monte carlo process variation and mismatch passes

4.7 System Layout and Fabrication

The single-chip power detector was submitted for fabrication in a 180nm SiGe BiCMOS process. The layout of the chip can be seen in figure 4.18. The chip was designed with ESD protection.

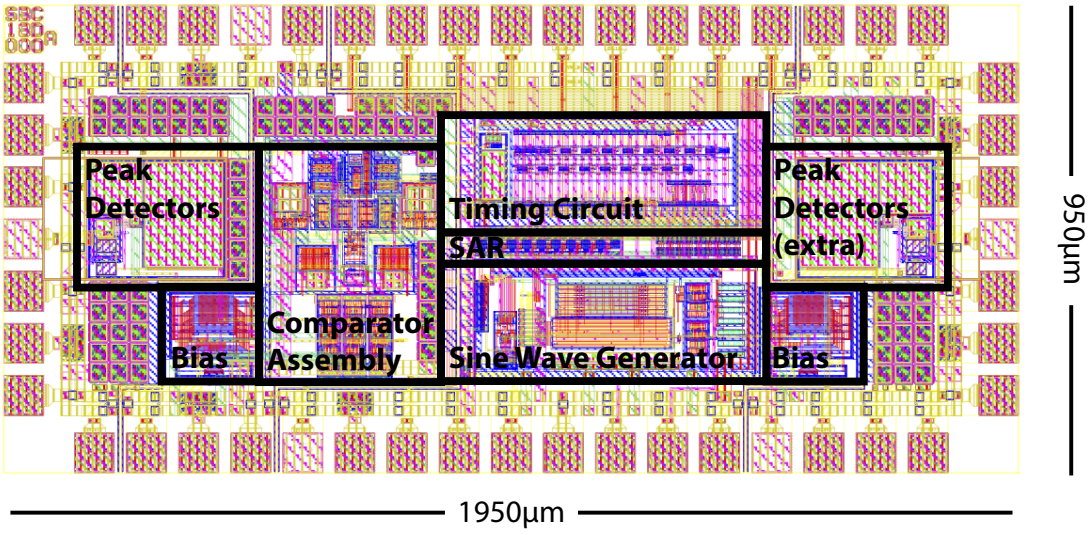


Figure 4.18: Layout of the single-chip BiCMOS power detector

4.8 System Results

While the single-chip power detector is currently still under fabrication, schematic-level simulations have been run to verify the system performance. Figure 4.19 shows a transient simulation of the detector searching for the input power level. The error is also plotted, and the end-of-cycle triggers are noted (these are the times when the detected power will be read).

Notice that the power detector detects the power within the $\pm 0.5dB$ error tolerance at a pulse period of 100ns with 50% duty cycle. The power detector takes approximately

$92\mu s$ to return an accurate power reading. Note also that the first EOC signal triggers after the SAR has been clocked 10 times at the pulse frequency. However, the system timing circuit, after measuring the fast pulse frequency, slows the SAR clock speed down so that the system can operate properly.

Figure 4.20 shows the simulation results of the detected power level over a sweep of input power levels at a pulse period of 100ns with 50% duty cycle. Figure 4.21 shows the error between the detected power and input power for this same test. Note that the error remains within $\pm$0.6dB over the entire dynamic range, and within $\pm$0.5dB for the majority of the dynamic range.

The single-chip power detector simulations require a vast amount of time to run, due predominantly to the combination of the very small time steps required to capture the 4GHz input signal and the relatively long simulation times required to capture the low frequency loop operation. A more complete characterization of the power detector will be performed via laboratory measurements, which will be far less time consuming (after all, it should take less than a millisecond for the loop to converge).

Table 4.2 shows the comparison of this work with various state of the art power detectors.

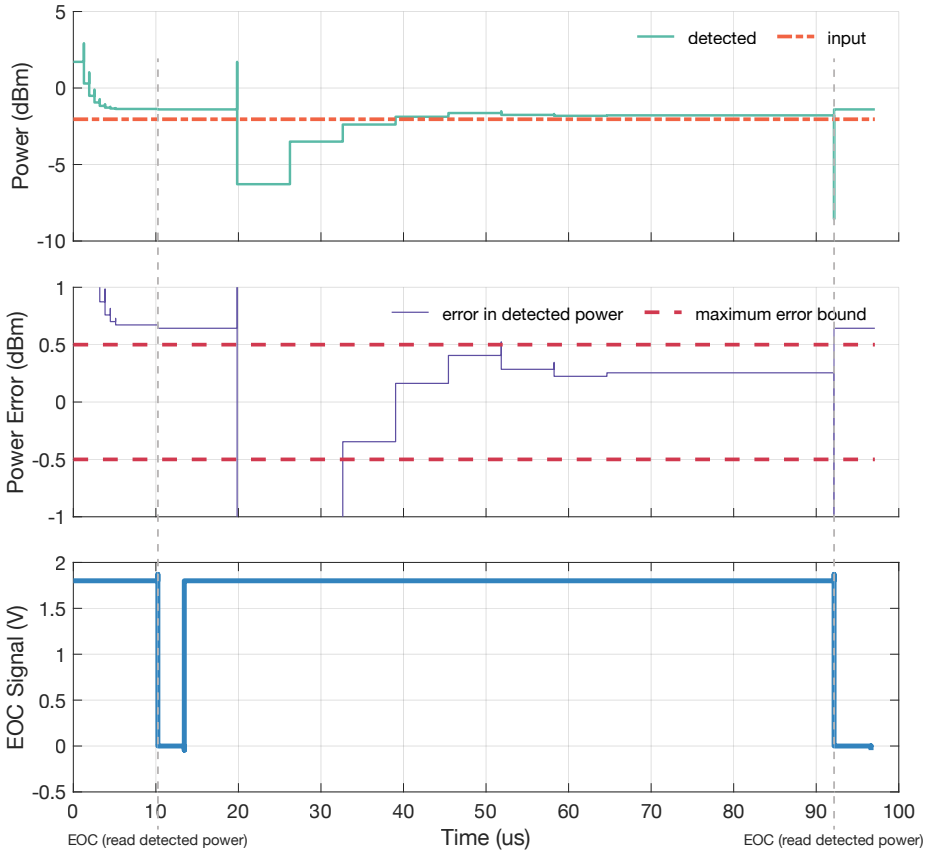


Figure 4.19: Transient simulation of the single-chip power detector ($P_{in} = -2dBm$, $T_{p,pulse} = 100ns$, $duty\ cycle = 50\%$, $f_{in} = 4GHz$)

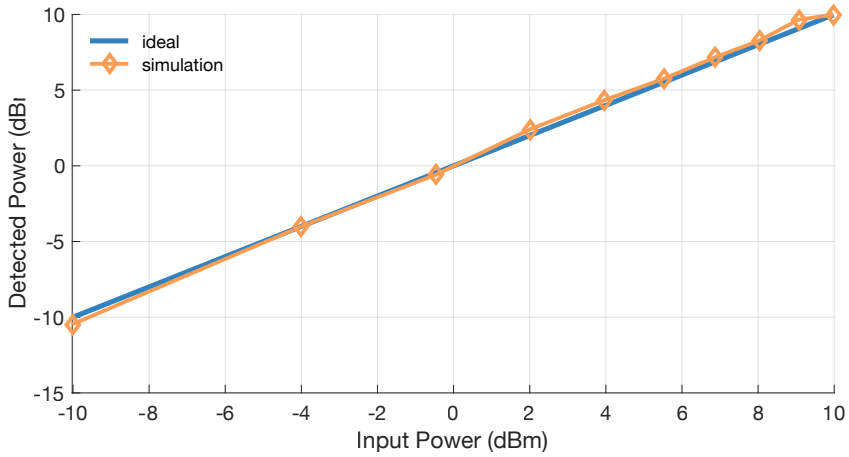


Figure 4.20: Detected power versus input power sweep ($T_{p,pulse} = 100ns$, $duty\ cycle = 50\%$, $f_{in} = 4GHz$)

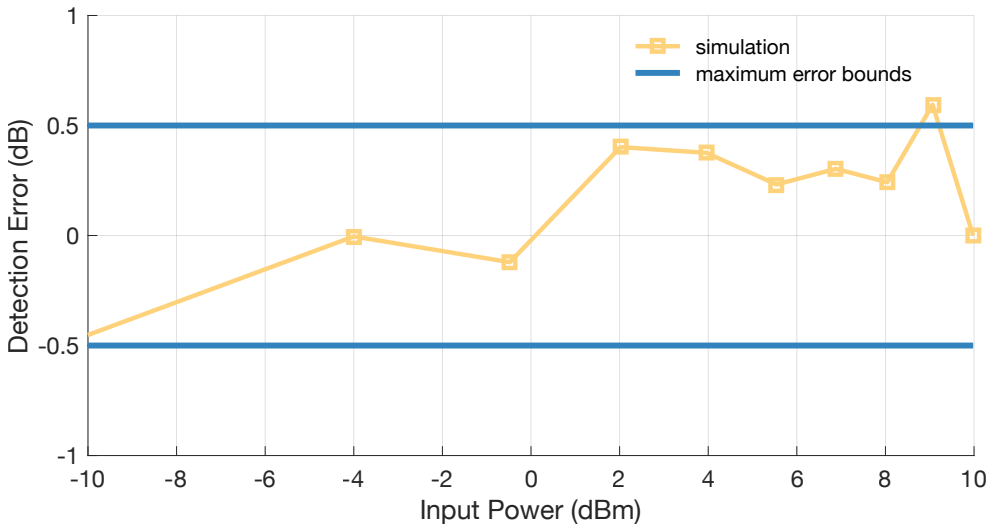


Figure 4.21: Detection error versus input power sweep ($T_{p,pulse} = 100ns$, $duty\ cycle = 50\%$, $f_{in} = 4GHz$)

Reference	ISCAS 2006 [8]	ISSCC 2005 [9]	MTT 2016 [10]	ISCAS 2015 [11]	LTC5596	This work
Technology	.250μm SiGe BiCMOS	.350μm BiCMOS	28nm CMOS	.180μm CMOS	Not specified	.180μm SiGe BiCMOS
Supply Voltage	2.5 V	2.7 V	1.8 V	3.3 V	3.8 V	1.8 V
Detector Architecture	log	rms	rms	rms	rms	peak
Band of Operation	up to 6 GHz	2 GHz	0.7 - 4 GHz	0.3 - 10 GHz	0.1 - 40GHz	2 - 4 GHz
Dynamic Range	45 dB	20 dB	40 dB	42 dB	35 dB	20 dB
Error	$\pm$1 - 2 dB	$\pm$1 dB	$\pm$0.8 dB	$\pm$1 dB	$\pm$1.5 dB	$\pm$0.6 dB
Refresh Rate	Not specified	Not specified	Not specified	Not specified	$\geq$ 1kHz	$\geq$ 1kHz

Table 4.2: Comparison of the proposed power detector with the state of the art

5. CONCLUSIONS

A BiCMOS power detector for pulsed RF power amplifiers was designed and fabricated. The power detector utilizes bipolar peak detectors to convert the amplitude information of the pulsed RF input signal into a dc level at the peak detector output. The detector compares this amplitude information with the amplitude information from a known amplitude, low frequency, continuous calibration sine wave created by an on-chip sine wave generator. The detector performs a successive approximation, attempting to match the amplitude information of the calibration sinusoid to that of the RF input. Once the successive approximation is complete, the known calibration amplitude should closely match the RF input amplitude. The matched calibration amplitude reading can then be converted into a peak power reading, which closely matches the peak power of the RF input signal. The power detector can support pulse rates from 50kHz to 10MHz with duty cycles from 5-50%. The power detector returns a power reading at least every 1ms, dependent on the pulse rate, with an accuracy of $\pm 0.6dB$.

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