DOPED METAL OXIDE HIGH-K GATE DIELECTRIC FOR NONVOLATILE MEMORY AND LIGHT EMITTING APPLICATIONS

A Dissertation

by

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ABSTRACT

The zirconium-doped hafnium oxide (ZrHfO) high-*k* thin film has excellent gate dielectric properties, such as a higher crystallization temperature, a lower defect density, and a larger effective *k* value. As a promising high-*k* material, ZrHfO has been utilized for both nonvolatile memory (NVM) and light emitting applications. Replacing the polycrystalline Si floating gate, the discrete nanocrystals embedded ZrHfO gate dielectric can achieve promising NVM performance. On the other hand, warm white light can be emitted from the thermal excitation of nano-resistors form from the dielectric breakdown of the ZrHfO Metal-Oxide-Semiconductor (MOS) capacitor. This novel solid state incandescent light emitting device (SSI-LED) unveils a new concept for the lighting device evolution.

Nanocrystalline cadmium sulfide (nc-CdS) embedded ZrHfO high-*k* NVMs have been fabricated to reduce the frequency dispersion problem caused by defects at the nanocrystal/dielectric interface. The nc-CdS embedded device can retain about 53% of originally trapped holes for 10 years and exhibit outstanding memory function at low operation voltage. The study on the nc-CdSe embedded ZrHfO NVMs shows that the high temperature enhances the hole trapping but decreases the electron trapping. Based on the different temperature dependences, the stored electrons release faster than stored holes. The raised temperature accelerates the dielectric breakdown process by increasing defect densities and defect effective conduction radii.

The post deposition annealing (PDA) atmosphere is critical to the electrical and light emission characteristics of ZrHfO SSI-LEDs. It affects the dielectric breakdown, light emission intensity and efficiency by changing compositions of the high-*k* stack and the nano-resistor. The electrical properties, i.e., effective resistances and Schottky barrier heights of nano-resistors have been estimated. The nano-resistor behaves neither like a conductor nor like a semiconductor. Moreover, the barrier height inhomogeneity is observed due to the random and complicated nano-resistor formation. The embedding method and the heavily doped *p*-Si substrate have been employed to enhance the light emission from ZrHfO SSI-LEDs.

Lastly, extensive applications of this novel nano-resistor device for on-chip optical interconnects and as diode-like anti-fuses have been discussed.

DEDICATION

Dedicated to my dearest father Shirong Zhang, mother Huibi Ji, brother Yumao Zhang, and my beloved wife, Yan Yang.

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CHAPTER I

INTRODUCTION

1.1 High-K Gate Dielectric

1.1.1 General Background

The rapid growth of the complementary metal oxide semiconductor (CMOS) integrated circuit (IC) technology keeps pushing the shrinking of silicon-based MOSFETs.[1] To achieve great performance with such a high transistor density on a chip, the channel length (L), i.e., the distance between the source and drain as shown in Figure 1,[2] has been reduced from micrometer scale to nanometer scale. The drive current (I_D) of a n-channel MOSFET can be expressed as the following equation:[3]

$$I_D = \frac{W}{L}\mu_n C_{ox}\left(V_G - V_T - \frac{V_D}{2}\right)V_D, \qquad [1]$$

where W is the width of the channel, μ_n is the effective mobility of electrons in the channel, C_{ox} is the gate capacitance associated with the gate dielectric when the underlying channel is in the accumulated state, V_D and V_G are the applied channel and gate voltage when the source is grounded, respectively, and V_T is the threshold voltage. According to the above equation, we can clearly figure out that the decrease of L can enhance the drive current and switch speed.

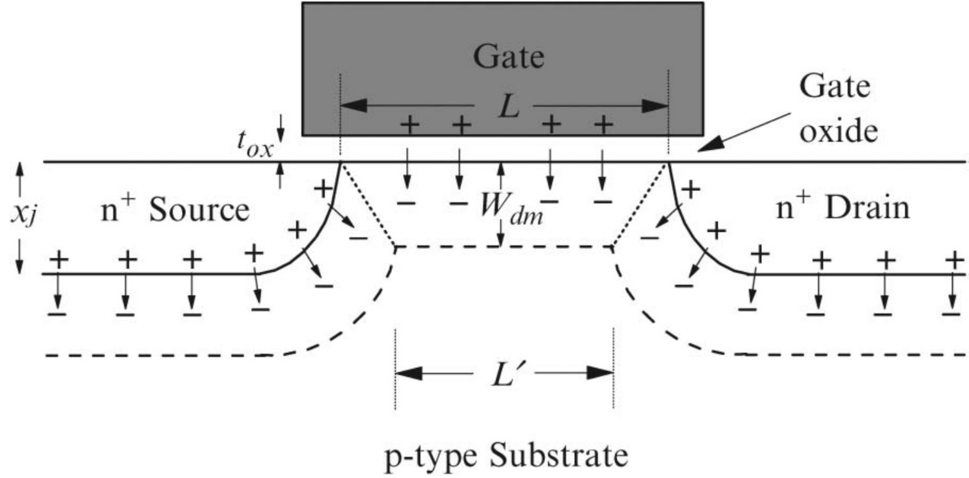

Figure 1. Schematic structure of a *n*-channel MOSFET. (Reprinted with permission from Ref. 2. Copyright 2012 IEEE.)

Nonetheless, when L decreases, the gate capacitance C_{ox} decreases following the parallel capacitance equation:[1]

$$C_{ox} = \frac{k\varepsilon_0 A}{t_{ox}} \qquad [2]$$

where ε_0 is the vacuum permittivity (8.854×10^{-12} F/m), k is the dielectric constant or the relative permittivity of the gate dielectric (a ratio of a material dielectric permittivity to ε_0), t_{ox} is the thickness of the gate dielectric oxide, and the gate area (A) is proportional to the channel length L. Since A decreases with the decrease of L, C_{ox} will also decrease, and according to Equation 1, it compensates for the improvement of the drive current. Based on Equation 2, there are two effective methods to maintain a larger C_{ox} with a smaller L to enhance the drive current: using a smaller t_{ox} or a larger k.

In current CMOS devices, the thermally-grown silicon dioxide (SiO_2) film has been commonly used as the gate dielectric for decades due to its excellent bulk and interfacial properties, such as a large energy band gap (E_g ~ 9 eV), a high dielectric breakdown strength (~ 15 MV/cm), a high crystallization temperature (> 1100 ºC), and a low interface state density ($D_{it} < 10^{11}$ $eV^{-1} \cdot cm^{-2}$).[1,4,5] For the device's scaling down, the SiO_2 thickness in a MOSFET keeps decreasing, but it will reach the limitation very soon. When the gate SiO_2 thickness is below 3 nm, the gate leakage current will become unacceptably large and several critical problems, e.g., power consumption and device reliability, will comes out.[6,7] In addition, the direct tunneling current through the SiO_2 gate dielectric will increase by 2 orders when the SiO_2 film thickness is reduced each 0.5 nm.[8] However, if we use a high-k material, e.g., to maintain the same C_{ox} as 15 Å thick SiO_2 does, we can reduce the gate leakage current and power consumption by 4 orders as shown in Figure 2. Therefore, the high-*k* material is needed for sub-3 nm thick gate dielectric devices.

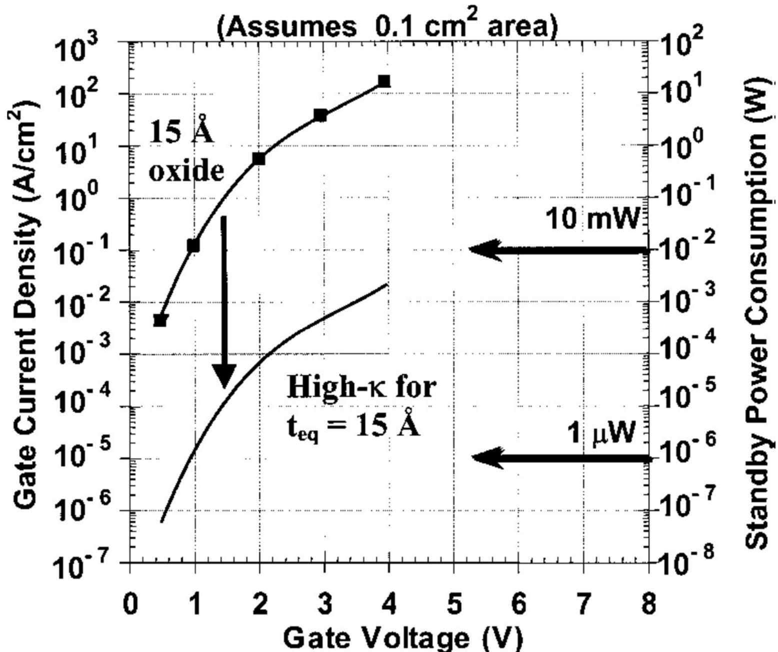

Figure 2. Power consumption and gate leakage current density for a chip which has a 15 Å thick SiO_2 gate dielectric or an alternate dielectric exhibiting the same capacitance. (Reprinted with permission from Ref. 1. Copyright 2001 AIP.)

1.1.2 HfO_2 High-K Gate Dielectric

Several high-*k* materials, such as Ta_2O_5, ZrO_2, HfO_2, Al_2O_3, La_2O_3, and so on, have been proposed to replace the conventional SiO_2 gate dielectric in MOSFETs.[9] The most favorable advantage of these high-*k* films is that they can use a larger physical thickness than that of the SiO_2 film to achieve the same C_{ox} and equivalent oxide thickness (*EOT*).[10] The *EOT* can be estimated by the following equation:[1]

$$EOT = \frac{k_{SiO_2}}{k_{high-k}} t_{high-k} . \quad [3]$$

Thus, a large k value is always desirable and preferable to reach a small EOT with a large physical thickness. Nevertheless, E_g values have a roughly inverse dependence on k values following the equation:[11]

$$E_g \sim k^{-0.65} \quad [4]$$

To prevent a large leakage current, E_g values should be larger than 5 eV and the k value has to be in the reasonable range of 20-30 accordingly.[11] Figure 3 shows that HfO_2, ZrO_2, and La_2O_3 are the most promising candidate high-k materials.[12]

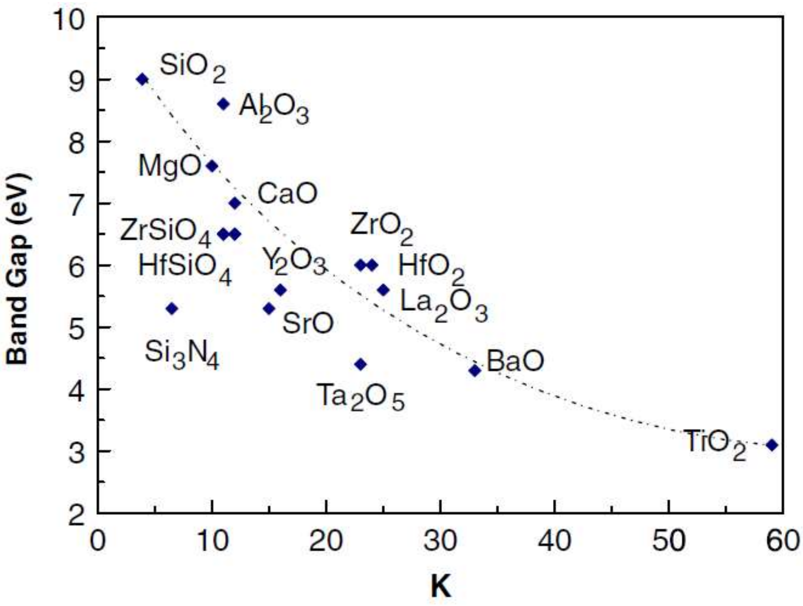

Figure 3. Static dielectric constant versus band gap for candidate high-k gate oxides. (Data from Ref. 1 and 12.)

Since a high temperature treatment is required in the MOSFET fabrication for the post deposition annealing and dopant activation, the thermal stability is critical for the high-*k* material.[13] In the thermally instable high-*k* film, the amorphous-to-polycrystalline phase transition may occur and a large number of grain boundaries generates and form diffusion paths.[14] In this case, the gate leakage current increases dramactically.[15-16] On the other hand, the interfacial quality at the high-*k*/Si interface affects the interface density states and the carrier mobility in the channel. For most high-*k* films, the interface layer can be generated by the metal silicate or slicide formation from the reaction of the diffused metal atoms with Si and O or the metal oxide with Si during the high temperature process.[17] The formed layer always has a relatively low *k* and causes a large D_{it}. Therefore, it has been a key step for the high-*k* application in the IC fabrication to suppress the interface layer formation and minimize the D_{it}.[18,19] Figure 4 shows the D_{it} of the HfO_2 and La_2O_3 films deposited on the Si substrate after the 500 ºC post deposition annealing (PDA) step.[20] Under the same PDA condition, the HfO_2 film has a lower D_{it} than the La_2O_3 film does, which excludes the latter to be the gate dielectric in this dissertation.

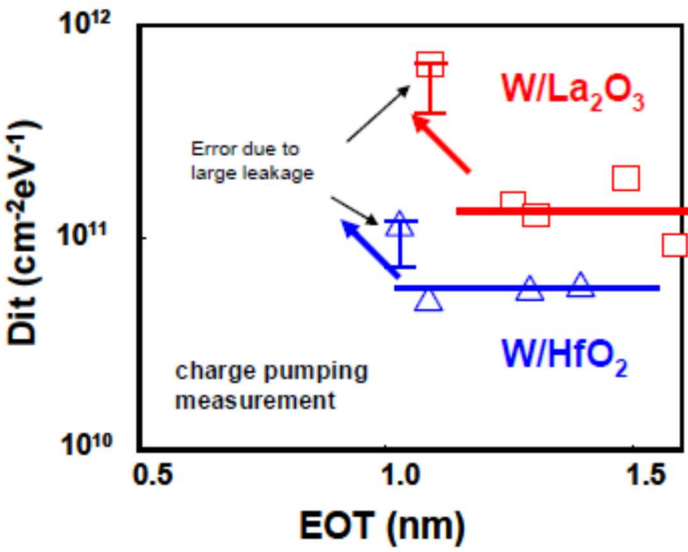

Figure 4. D_{it} of La_2O_3 and HfO_2 thin films annealed at 500 ºC. (Reprinted with permission from Ref. 20. Copyright 2008 IEEE.)

On the other hand, although the chemistries of HfO_2 and ZrO_2 are nearly identical,[21] the latter tends to form silicide with Si, which can degrade effective *k* values and increase gate leakage current.[22,23] Moreover, the conduction and valance band offsets of HfO_2 are 1.5 eV and 3.4 eV with respect to Si,[24] respectively, which are relatively larger than those of ZrO_2 and other high-*k* candidates with comparable *k* values as shown in Figure 5. Therefore, HfO_2 is more favorable to serve as the gate dielectric in a MOSFET.

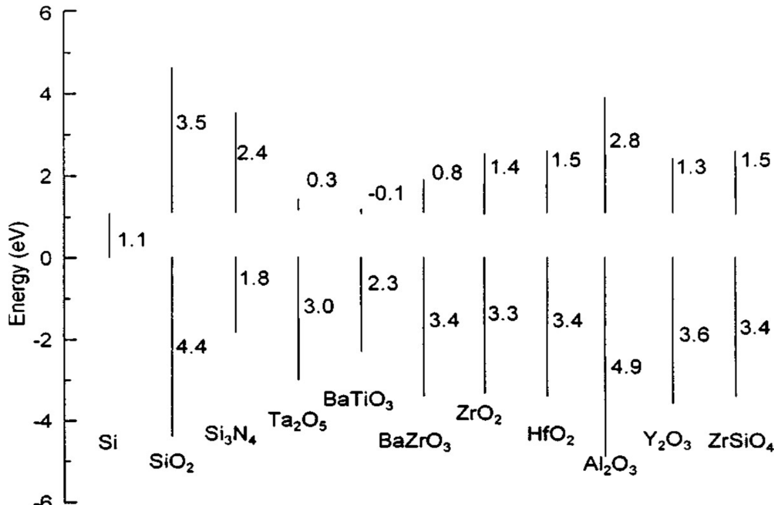

Figure 5. Conduction band and valence band offsets of various high-*k* oxides on Si. (Reprinted with permission from Ref. 24. Copyright 2000 AVS.)

1.1.3 Zr-doped HfO_2 High-K Gate Dielectric

As discussed before, the HfO_2 high-*k* gate dielectric has been extensively used in the advanced MOSFET devices for its high effect *k* value, large conduction and valence band offsets with respect to Si, and thermally stable contact with Si.[25] However, there exists a great drawback of HfO_2 films for the MOSFET application, i.e., low crystallization temperature (< 500 °C).[26] In common IC processes, it will be very easy to form crystalline in HfO_2 films and transfer charges through the oxide layer via grain boundaries, forming a large gate leakage current. Previously, it is reported that adding a small amount of Zr into the Ta_2O_5 high-*k* film can improve its amorphous-to-crystalline temperature, e.g., from 600 °C to 900 °C.[27,28] Since HfO_2 and ZrO_2 and have similar gate dielectric properties (i.e., *k* value, E_g, and band offsets) and are miscible as shown in Figure 6,[29] The Zr-doped HfO_2 (ZrHfO) high-*k* dielectric has been proposed to solve the low

crystallization temperature problem. By adding a small amount of Zr (12 wt%), into a Hf target, the ZrHfO gate dielectric can be deposited by sputtering the composite targe in Ar/O_2 atmosphere.[30] Compared to the undoped HfO_2 film, the ZrHfO film showed a much higher amorphous-to-polycrystalline transition temperature (> 900 ºC), a lower D_{it}, and a smaller *EOT*.[30,31] Furthermore, a sub-nanometer *EOT* (e.g., 0.97 nm) with low gate leakage current was achieved in the sputter-deposited ZrHfO high-*k* gate dielectric MOS capacitor as shown in Figure 7.[30] Therefore, ZrHfO is a good high-*k* gate dielectric material and will be applied in this dissertation for both nonvolatile memory and light emitting applications.

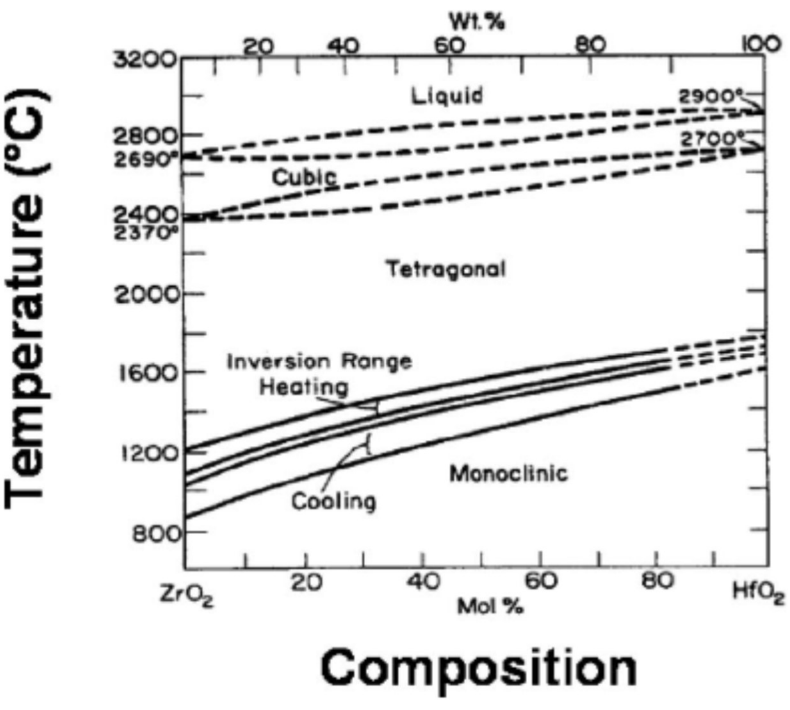

Figure 6. Temperature-composition phase of HfO_2-ZrO_2. (Reprinted with permission from Ref. 29. Copyright 2007 AIP.)

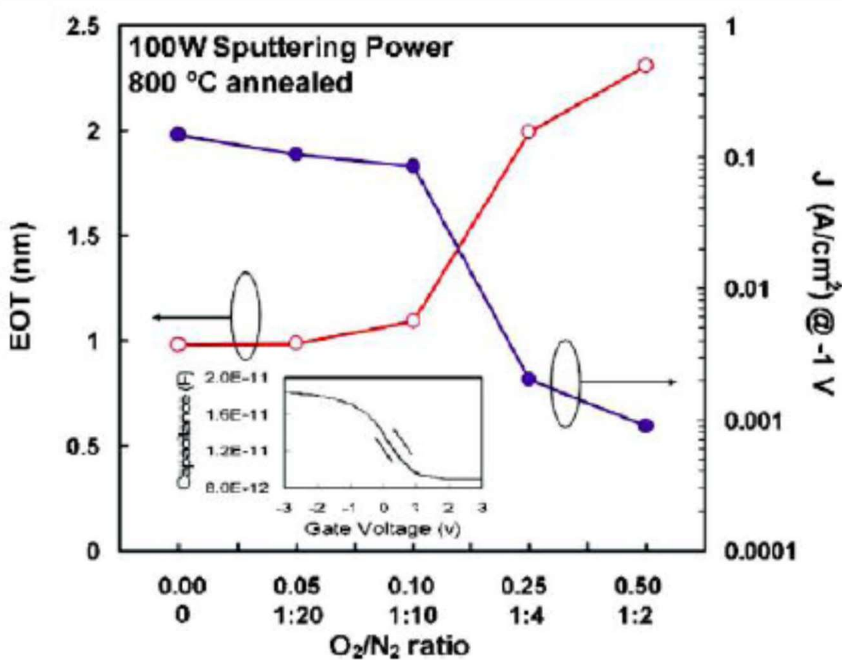

Figure 7. *EOT* and gate leakage current of ZrHfO films after the PDA under different O_2/N_2 ratios. (Reprinted with permission from Ref. 30. Copyright 2007 ECS.)

1.2 Nanocrystal Nonvolatile Memory

1.2.1 Conventional Flash Nonvolatile Memory

In 1980, the flash nonvolatile memory (NVM) was firstly proposed by Masuoka in Toshiba. Since then, the flash memory has been extensively investigated and widely exploited for the modern portable electronics. Currently, the NAND flash NVM dominates the market and production for its large capacities, fast write/erase speed, small erase units, and IC process compatibility.[32] The NVM is defined as a device that can maintain in two distinguished charged states, i.e., the written and erased states, for more than 10 years with power.

Figure 8 shows a typical structure of a flash memory core cell. This resembles a standard MOSFET with two gates, i.e., the control (CG) and floating (FG) gates.[33] The conventional FG layer is made from continuous poly-Si layer that functions as a potential well to trap charges. The device is written and erased by charges tunneling through the insulator 1, which therefore is named as "tunnel oxide"; the current leakage between FG and CG is blocked by the thicker insulator 2, which therefore is named as "control oxide". Normally, the cell represents the logic "0" by the written state and the logic "1" by the erased state, as shown in Figure 9.[34]

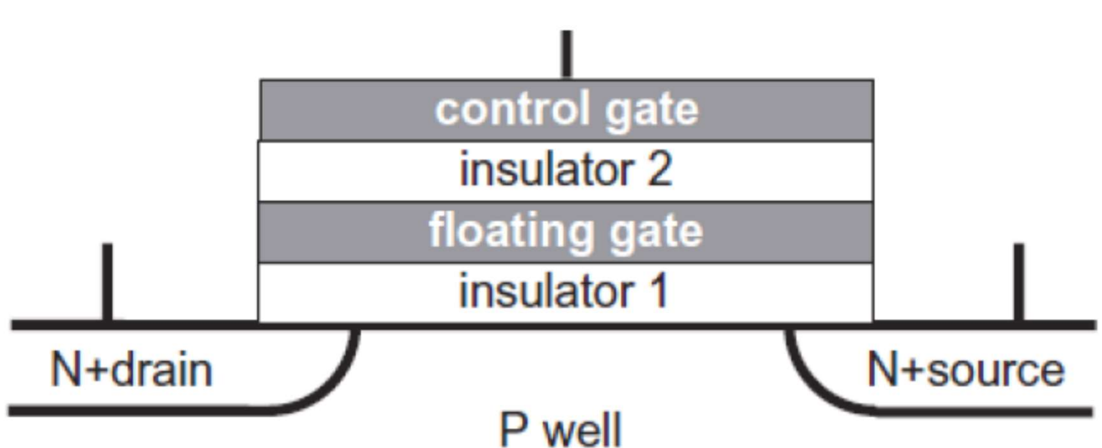

Figure 8. Schematic cross-sectional structure of a flash memory core cell. (Reprinted with permission from Ref. 33. Copyright 2007 Wiley.)

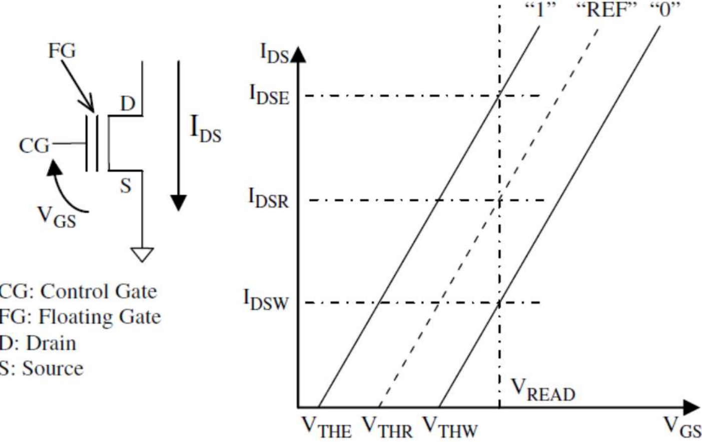

Figure 9. Current/voltage characteristics as a function of the threshold voltage of a flash cell. (Reprinted with permission from Ref. 34. Copyright 2008 Springer.)

Figure 10 shows a typical band energy diagram for a conventional FG flash NVM made of poly-Si CG/control SiO_2/poly-Si FG/tunnel SiO_2/Si.[33] In the conduction band, the poly-Si FG layer is isolated the high energy barriers of the control and tunnel SiO_2 layers to provide the nonvolatile retention of stored charges. In order to write/erase the device, i.e., storing or releasing charges, the potential difference between the FG and either SiO_2 layer needs to be altered until charges can overcome the barrier. During these processes, charges mainly follow two conduction mechanisms, i.e., Fowler-Nordheim (F-N) tunneling and channel hot electron (CHE) injection. F-N tunneling is induced by a high electrical field where electrons can easily tunnel through the triangular barrier.[35] CHE injection happens when an electron gains energy from an electric field and then collides with the lattice to redirect itself into the FG layer.[35] Typically, the NOR device is written

by CHE and erased by F-N tunneling; the NAND device uses F-N tunneling for both operation.

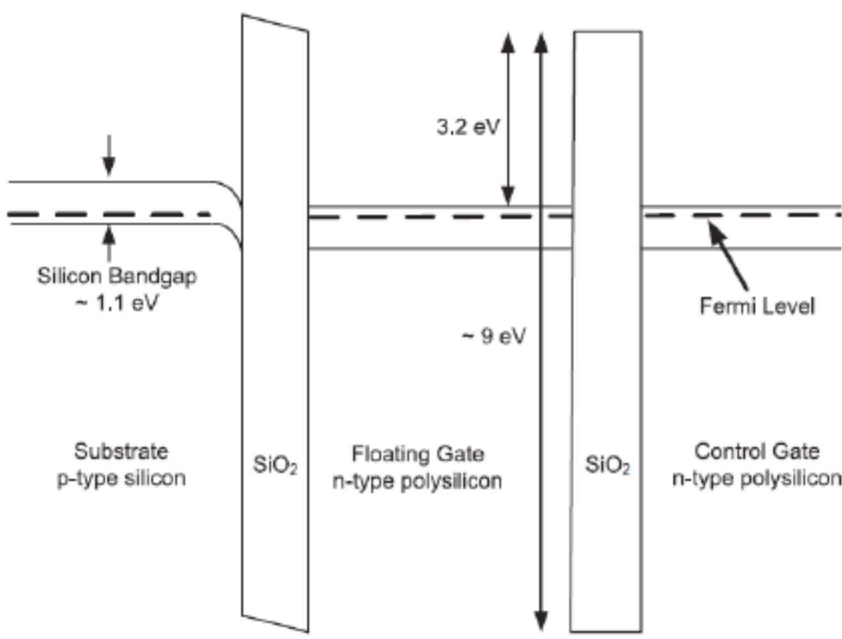

Figure 10. Energy band diagram for a typical FG structure. (Reprinted with permission from Ref. 33. Copyright 2007 Wiley.)

1.2.2 Nanocrystals Embedded FG Structure

Following the Moor's law that the transistor number in a dense IC chip doubles every two years,[36] the flash NVM has to scale down the tunnel oxide thickness to achieve the goals of ultra-high density, fast speed, and energy-saving. However, when the thickness of the SiO_2 layer is scaled down to 1.2 nm, the leakage current becomes unacceptably large and stored charges will easily tunnel back to the Si substrate.[1,6,35]

Moreover, all trapped charges can easily release from the conducive continuous poly-Si FG layer through a weak spot in the tunnel oxide layer, as shown in Figure 11.[37] This would cause a serious reliability issue for the memory application. Therefore, it was proposed by Tiwari in 1996 to use the discrete nanocrystalline Si (nc-Si) dots instead of the continuous FG layer.[38] In this structure, only part of the stored charges will be released when a leakage path forms through the tunnel oxide layer. Thus, this structure has drawn extensive attention as a promising candidate to replace the conventional FG NVM for the further scaling.

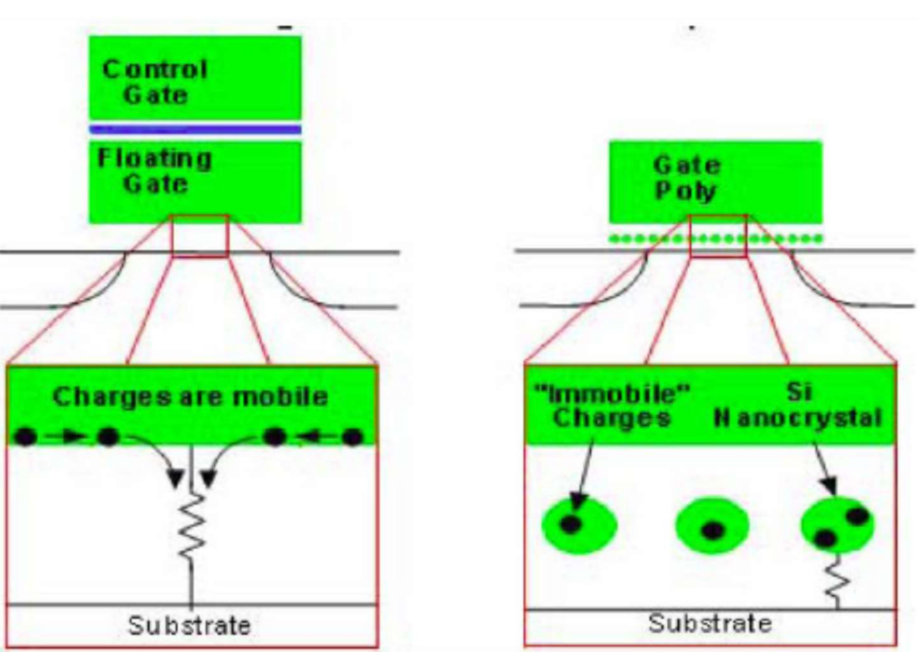

Figure 11. Schematic diagram illustrates how a defect chain affects the charge loss in conventional FG structure and nanocrystal embedded FG structure. (Reprinted with permission from Ref. 37. Copyright 2006 IEEE.)

1.2.3 Fabrication of Embedded Nanocrystals

The nanocrystals embedded in the FG structure can be prepared by numerous methods, such as self-assembly and precipitation.[35] The basic procedure of self-assembly for nanocrystal formation is shown in Figures 12(a) to 12(c). A 1-5 nm thick film, i.e., charge trapping layer (CTL), is deposited and then annealed at a temperature close to its eutectic temperature in an inert ambient gas, usually N_2, to convert the CTL into a discrete nanocrystalline form. The nanocrystal diameter is significantly influenced by the thickness of the embedded CTL as well as the annealing temperature and duration.[39-42] Fig. 12(d) shows the major driving forces driving this process, which is accomplished through the relaxation of film stress and limited by the surface energy. During the annealing, atoms can gain enough surface mobility and the film self-assembles into a more thermodynamically stable state with the minimum surface energy.[42] In the process, dispersion force and electrical double layer affect the nanocrystal size and location distributions.[42-44] This method is very popular for its easy operation and many kinds of materials, such as Si, cobalt (Co), gold (Au), tungsten (W), silver (Ag) and platinum (Pt), have been embedded into the FG by it.[40-42,45] On the other hand, Figure 13 shows the precipitation method that uses high injection energy (30-150 keV) ion implantation or co-deposit system to form nanocrystals.[35,46,47] This process is usually followed by the thermal treatment, e.g., at 950-1050 ^{o}C for 30-60 min in N_2 atmosphere. During the thermal process, reactants can gain enough energy to diffuse through the film and collide with other reactants to form nucleus.[48] At the high temperature, more reactants can bond to the nucleus and form discrete nanocrystalline dots in the CTL. However, the high-energy ion

implantation may damage the tunneling oxide and degrade the device performance. Additionally, this method cannot control the size and spatial distribution of nanocrystals in the gate dielectric. In this dissertation, the nc-CdS and nc-CdSe embedded ZrHfO gate dielectric stacks are fabricated based on the concept of the thin film self-assembly process. The thin embedded layer will be deposited by the sputtering technique and subjected to a rapid thermal process.

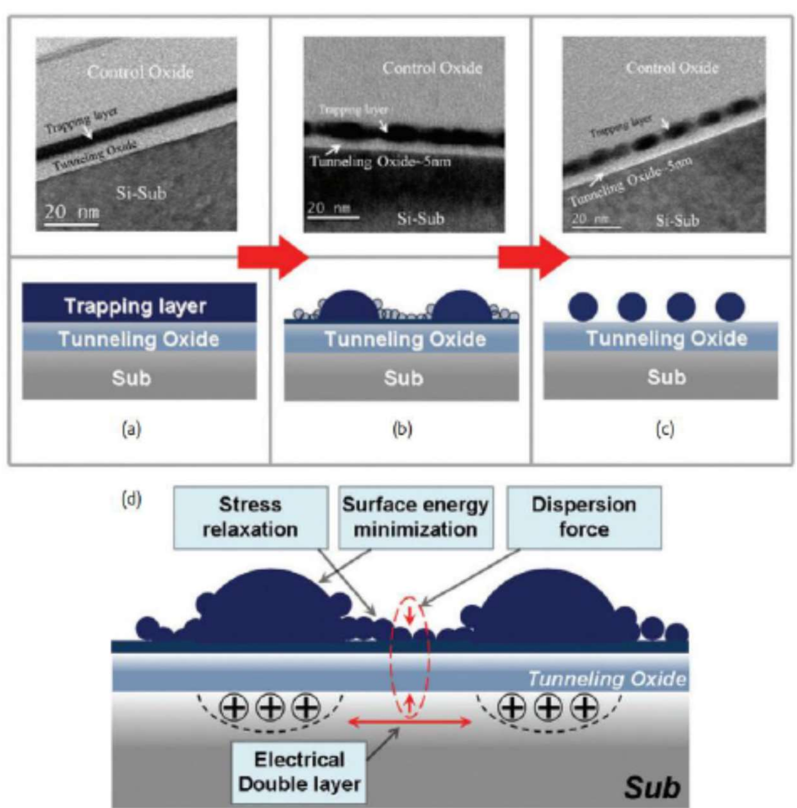

Figure 12. TEM image and schematic drawing of nanocrystal formation by self-assembly with increased duration of thermal treatment from (a) to (c); (d) Major driving forces in nanocrystal formation by self-assembly. (Reprinted with permission from Ref. 35. Copyright 2011 Elsevier.)

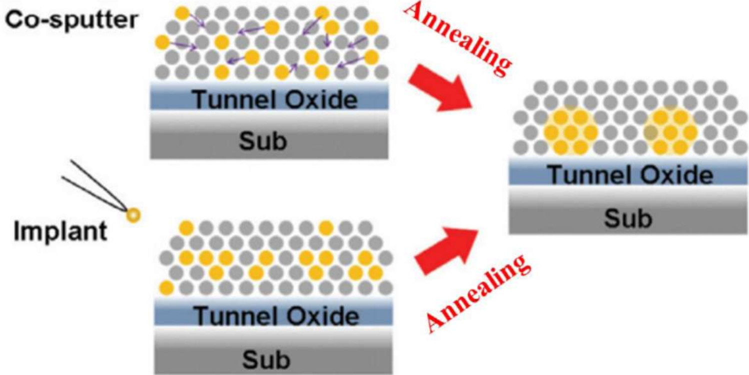

Figure 13. Schematic drawing of nanocrystal formation by precipitation. (Reprinted with permission from Ref. 35. Copyright 2011 Elsevier.)

1.2.4 Nanocrystals Engineering

The nc-Si is firstly used in the nanocrystal FG NVM by Tiwari in 1996 for its compatibility with the standard MOSFET technology.[38] However, the nc-Si embedded FG NVM suffers the degraded electron trapping capability and retention performance from two mechanisms, i.e., the Coulomb blockade and quantum confinement effects.[49,50]

Coulomb blockade effect describes the energy level increase due to the trap of multiple electrons in the nanocrystal. This effect becomes more pronounced when the nanocrystal size is below 3 nm.[51] The raise of electrostatic potential from the trap of an electron can be approximately calculated from the below equation:

$$\Delta E = \frac{q^2}{C} \quad [5]$$

where q is the electron charge, C is the self-capacitance of the nanocrystal ($C = 2\pi\varepsilon_0 d$ where ε_0 is the dielectric constant of the tunnel oxide and d is the nanocrystal diameter). The increase of the electrostatic potential is illustrated in Figure 14. For an electron trapped

in a nc-Si of 5 nm diameter, the self-capacitance is approximately 0.7 atto farads and the increase of electrostatic potential energy is about 0.074 eV.[38] Therefore, the increase of energy level lower down the barrier between the nc-Si and the tunnel oxide, which degrades the device's retention performance. Moreover, as electrons are trapped in the nanocrystal, the built electrostatic potential decreases the electric field across the tunnel oxide and prevent the subsequent electrons from injecting into the nanocrystal. Consequently, the number of trapped electrons in the nc-Si is limited.

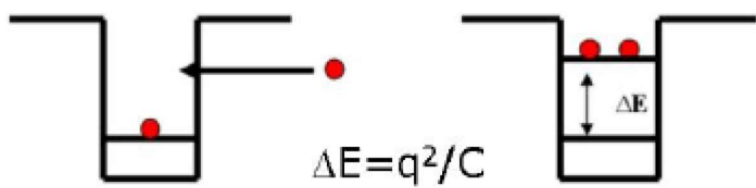

Figure 14. Illustrations of Coulomb blockade effect.

The quantum confinement effect is the enlargement of band gap as Si is prepared in the nanometer size. As a result, the energy band offset of nc-Si/tunnel oxide is reduced. The shift of the conduction band edge due to the quantum confinement effect can be estimated using the following equation,[51]

$$E_C\left(d_{Si}\right)-E_C\left(\infty\right)=\frac{1.39}{d_{Si}^2+1.788d_{Si}+0.668}\left(eV\right) \qquad [6]$$

where $E_C(d_{Si})$ is the conduction band edge of the nc-Si, $E_C(\infty)$ is the conduction band edge of the bulk Si, and d_{Si} is the nc-Si size in diameter. As shown in Figure 15, the increase of the conduction band edge for a 5 nm nc-Si is 0.04 eV.

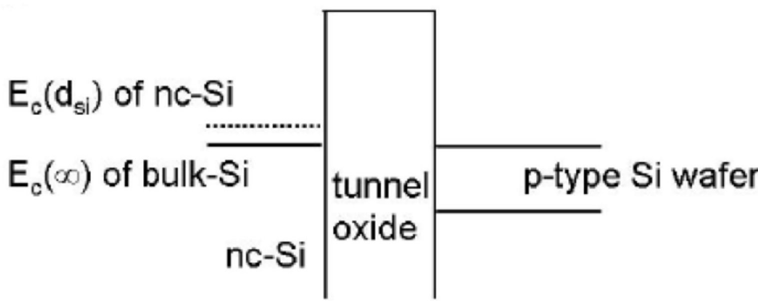

Figure 15. Illustrations of quantum confinement effect.

Due to the Coulomb blockade and quantum confinement effects, the stored charges in the nc-Si will be easily tunneled back to Si substrate because of the lower band offset between nc-Si and tunnel oxide. One way to solve this problem is to replace the nc-Si by another nanocrystal material with a large electron affinity or work function and a small band gap. This can create a deep potential well in the conduction or valence band for better retention performance.[52,53] Thus, in this dissertation, nanocrystalline cadmium sulfide (nc-CdS) and nanocrystalline cadmium selenide (nc-CdSe) have been embedded into the gate dielectric as the charge trapping media. CdS is an *n*-type semiconductor with a large electron affinity of 4.3 eV and a small band gap of 2.42 eV.[54] CdSe is another *n*-type II-VI group semiconductor with a large work function of 4.8-5.0 eV and a small band gap of

2.3 eV.[55] They both create deep potential wells in the conduction and valence bands. As mentioned in last section, the ZrHfO high-*k* dielectric is exploited as the tunnel and control oxide layers for its excellent material and electrical properties. Therefore, the nc-CdS and nc-CdSe embedded ZrHfO high-k gate dielectric capacitors have been fabricated and characterized for the NVM functions.

1.3 Light Emitting Device

1.3.1 Conventional Light Emitting Device

In 1879, the incandescent light bulb was invented to emit warm white light with a W filament heated to a high temperature by Joule heating.[56] The light has a color temperature close to that of sunlight and extremely high color rendering index (CRI) of nearly 100.[57] However, the device can only convert the less than 5% of electrical energy into the visible light. Approximately at the same time, the fluorescent lamp was invented to provide a more efficient lighting alternative of 50-60 lm/W than the incandescent light bulb (< 20 lm/W). The fluorescent lamp relies on inelastic collisions of electrons with mercury atoms to emit ultra violet (UV) photons, which are subsequently absorbed by the lamp's fluorescent coating and converted into visible light. Commercial fluorescent lamps can be as efficient as 100 lm/W but they is limited by their poor CRI and color temperature. Moreover, it contains mercury vapor that is an environmental pollutant once leak out.[58,59]

The light emitting device (LED) has a high conversion efficiency of ~80% and a long lifetime of ~50,000 hours. It is a promising lighting method to replace the incandescent light bulb and fluorescent lamp, which can reduce ~38% of the total lighting

energy usage in the United States.[60] The first visible-spectrum red LED was developed in 1962 by Nick Holonyak, Jr. while working at General Electric.[61] It emitted light from a III-V compound semiconductor material, i.e., Ga($As_{1-x}P_x$). The light emission principle of the LED is: under forward-biased condition, when carriers, i.e., electrons and holes are injected across the *p-n* junction, it emits incoherent light as shown in Figure 16.[62] The emitted photon energy is approximately equal to the bandgap energy as the following equation,[62]

$$h\nu = \frac{hc}{\lambda} \cong E_g \qquad [7]$$

where h is the Planck's constant of 6.626×10^{-34} J/s, v is the frequency of light, c is the speed of light of $3\text{x}10^8$ m/s, λ is the wavelength of light, and E_g is the band gap energy. Currently, commercialized LEDs are still made from III–V compound semiconductor materials. Different bandgap energies are used to produce different wavelengths of the emission lights, such as GaAlAs (red), AlInGaP (yellow-orange), InGaN (blue, green), AlInGaN (ultra violet).

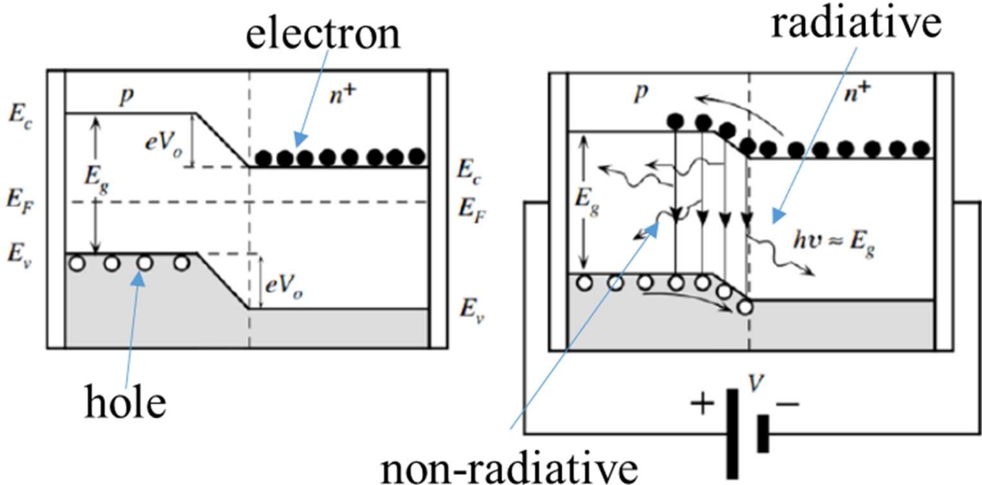

Figure 16. Energy band diagrams of a *p*-n^+ junction (a) without bias and (b) with applied bias *V*. (Adapted from Ref. 62.)

The electron-hole recombination process can be classified into two kinds: radiative and non-radiative recombination.

Radiative recombination is the band-to-band recombination that mainly happens in direct bandgap semiconductors. Figure 17(a) shows an example of a direct bandgap semiconductor, GaAs,[63] where the minimum energy of conduction band lies directly above the maximum energy of valence band in the momentum space energy. In this material, free electrons at the bottom of conduction band can recombine directly with free holes at the top of the valence band, as the momentum of the two carriers is the same. This transition from conduction band to valence band involves photon emission. Direct recombination occurs spontaneously.

Generally, the non-radiative recombination includes Auger recombination, surface recombination, or recombination at defects.[64] As shown in Fig. 17(b), the momentum

location of the minimum energy of conduction band is shifted by a k-vector compared to that of the maximum energy of valence band in an indirect bandgap semiconductor, e.g., GaP. Because of this momentum difference, the probability of direct recombination, i.e., radiative recombination is low. Additional dopants (impurities) are added in this kind of material to form shallow donor states. These donor states serve as the recombination centers that capture the free electrons locally and shift to the momentum location of the maximum energy of valence band for electron-hole recombination. Besides a photon emission, phonon emission or absorption has to take place, which should satisfy both energy and momentum conservations. This indirect recombination is called non-radiative recombination.

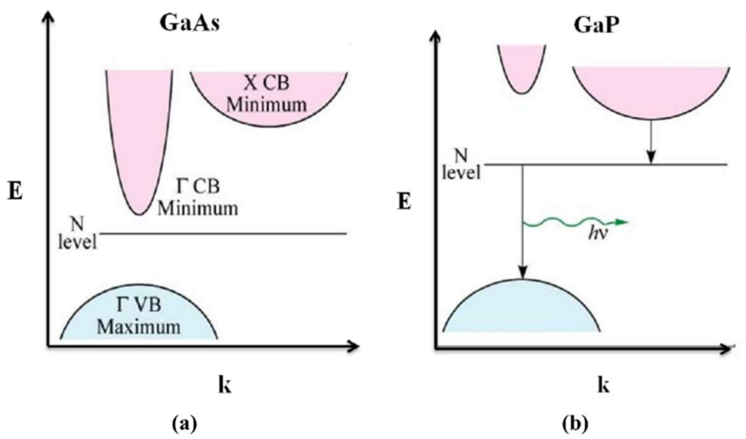

Figure 17. Schematic band structures of (a) GaAs and (b) GaP.

1.3.2 White Light Emitting Device

As discussed previously, the wavelength of light emitted from a *p-n* junction LED is decided by the bandgap energy of the semiconductor material, which has a very narrow band. For white light emission, there are two major methods as shown in Figure 18.[65] The first method is to combine red, green, and blue lights from three different LEDs.[66] However, a special driving circuit is required to balance the light colors.[67] The second method is to combine a blue or UV LED with a yellow phosphor or a tri-phosphor blend as shown in Fig. 18(b).[68] However, the light conversion of short wavelength to long wavelength always accompanies with the Stokes energy loss, which costs 10-30% of the overall power.[56] Therefore, a cheap single-chip white light LED is eagerly anticipated.

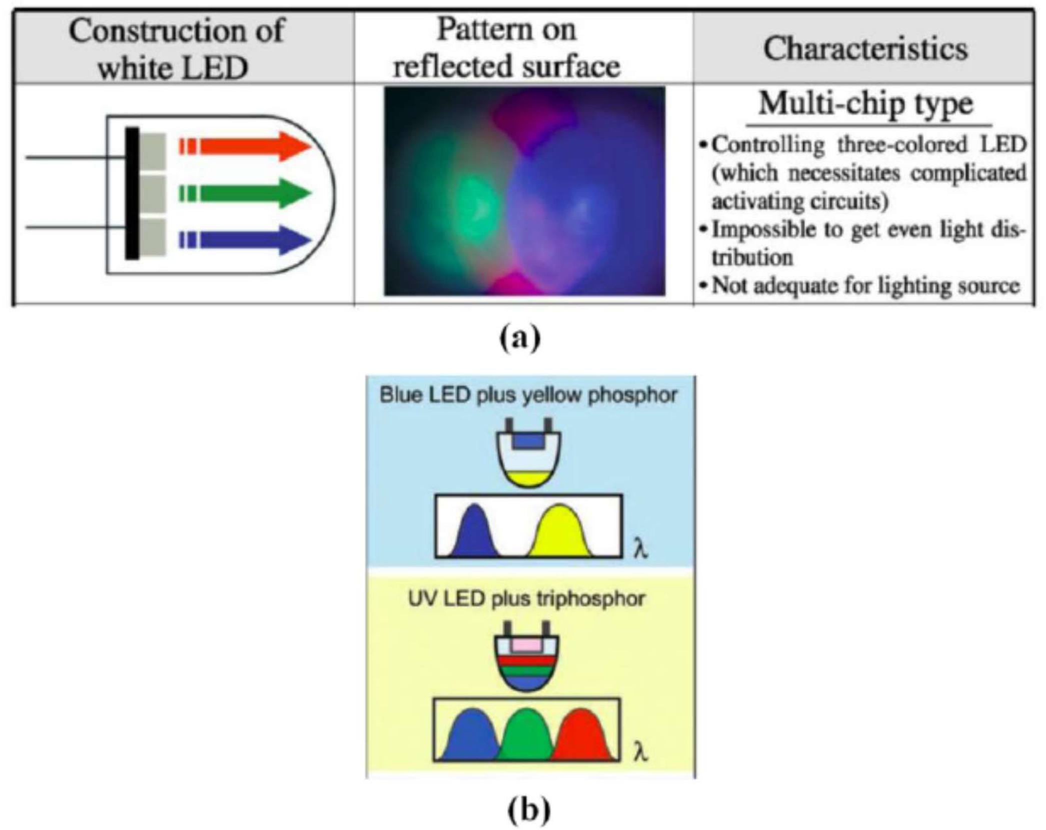

Figure 18. Construction and characteristics of white LED: (a) through colored RGB LEDs and (b) through blue/UV LED in combination with phosphors. (Reprinted with permission from Ref. 65. Copyright 2007 Wiley.)

On the other hand, the fabrication of these compound semiconductor epitaxy layers requires using the expensive molecular beam epitaxy (MBE) or the highly toxic metal organic chemical vapor deposition (MOCVD) processes. Moreover, the performance of these single crystal LEDs is critically affected by defect densities in *p-n* junction or WQ. They always suffer the poor lifetime problem from crystal defects during the mismatched growth.[69,70] Separately, the LED can be made with the structure of the quantum dot (QD) embedded dielectric thin films, like nc-Si embedded silicon oxide (SiO_x) or silicon nitride

(SiN_x).[71,72] The QDLED emits light from the electron-hole radiative recombination in the QD due to quantum confinement effects and exciton radiative recombination at defective bonds in the dielectric film.[71] Though, the QDLED is subject to the low power efficiency and the short lifetime, e.g., nc-Si embedded SiO_x or SiN_x matrix has a bad efficiency of <0.01% and a poor lifetime of <1,800 hr.[72]

1.3.3 Solid State Incandescent Light Emitting Device

It is desirable to have a LED that emits the broad band white light from a single device and can be fabricated with the low-cost, environmentally friendly, and IC-compatible processes with a long lifetime. Since 2011, Kuo's group proposed a new type of solid-state incandescent LED (SSI-LED) that emitted the warm white light similar to that of the incandescent bulb.[73-81] The light emitting principle of the SSI-LED is the thermal excitation of the nano-sized conductive path, i.e., nano-resistor, from the passage of a current.[73-81] Under the resistive heating, atoms in the nano-resistor are thermally excited and part of the thermal kinetic energy is transferred to electrons.[82] These excited electrons can relieve by photonic emission and it produces a continuous non-discrete spectrum due to the near-continuum of electron energy levels.[82] The light emission spectrum is close to that of the incandescent light bulb, i.e., blackbody radiation. This kind of device is made from a MOS capacitor composed of an amorphous high-*k* dielectric thin film, such as Zr-doped HfO_2 (ZrHfO), HfO_x, or WO_x, on a *p*-type Si wafer.[73-81] The nano-resistor is formed from the breakdown of the high-*k* dielectric thin film, which generates a bump above it.[79]

These high-k dielectrics are often used in the MOS field-effect transistors (MOSFETs) or capacitors. Upon the deposition of the high-k dielectric film, a PDA step is carried out to densify and to reduce defects in the film. The PDA condition is critical to the material and electrical properties of the final device.[1,30] For the SSI-LED, the PDA process influences the conductive path formation and therefore, characteristics of the emitted light.[75,77] In this dissertation, the effect of the PDA atmosphere on the electrical and optical properties of the ZrHfO high-k SSI-LED have been investigated.

On the other hand, there is lack of detailed information of electrical properties of nano-resistors in this new type of device. It was reported that when conductive paths were formed from the hard breakdown of the metal oxide MOS capacitor, contacts at the gate/conductive path and conductive path/Si could be taken as the ohmic and Schottky contacts, separately.[83] Therefore, the effective resistance and Schottky barrier height of nano-resistors in the ZrHfO high-k SSI-LED have been studied under different stress voltages and temperatures.

1.4 Outline of this Dissertation

Chapter II focuses on the experimental methods utilized in this dissertation. Their corresponding background knowledge and the related equipment operations will be described. At first, the process flow of fabricating the ZrHfO high-k MOS capacitor with or without the embedded layer will be described in detail. Then, the fundamental background of the thin film deposition and annealing methods will be reviewed, including the radio frequency (RF) magnetron sputtering technique, the rapid thermal annealing

(RTA) equipment, and the plasma enhanced chemically vapor deposition (PECVD). The instruments and the background knowledge of the material characterizations, e.g., profilometer, secondary ion mass spectrometry (SIMS), atomic force microscopy (AFM), and scanning electron microscope (SEM) will be introduced. The electrical and optical characterizations of the ZrHfO high-*k* based NVMs and SSI-LEDs, such as system setups, capacitance-voltage (*C*-*V*), conductance-voltage (*G*-*V*), current density-voltage (*J*-*V*), and light spectrum measurements, will be also discussed in this chapter.

Chapter III focuses on the NVM application of the nc-CdS embedded ZrHfO high-*k* gate dielectric stack. The detailed electrical investigations of this device will be presented. The discrete nc-CdS prefers to trap holes other than electrons due to its *n*-type nature. The device shows negligible frequency dispersion phenomena which indicates holes are mainly trapped in the CdS nanocrystals. Due to the good contact between the nanocrystals and the high-*k* film, this NVM device shows excellent low voltage operation performance, i.e., comparable or even better memory windows and hole retention capabilities. More than half of the originally trapped holes can remain in the high-*k* stack for 10 years. The nc-CdS embedded ZrHfO high-*k* stack is a viable dielectric structure for the low power operating NVM application.

Chapter IV describes the temperature effects on the charge trapping/detrapping and transfer mechanisms as well as the dielectric breakdown behavior and retention capabilities of the nc-CdSe embedded ZrHfO gate dielectric NVM. The hole-trapping capacity increases but the electron-trapping capacity decreases with the increase of temperature. The frequency dispersion result shows more holes are loosely trapped at the

nanocrystal/high-*k* interface and electrons are mainly trapped in the bulk nanocrystal at high temperatures. The temperature dependence and mechanisms of charge transfer have been discussed. At the same time, the high temperature accelerates the failure process of the device and the statistical breakdown distribution has been analyzed. The temperature dependent relaxation current study shows that releases of the trapped holes and electrons are dominated by two different mechanisms. This causes the faster degradation of the electron retention capability.

Chapter V discusses the PDA atmosphere effects on the electrical and optical properties of the ZrHfO based SSI-LED. The O_2 PDA step changes compositions of the original high-*k* stack and the nano-resistor formed from the dielectric breakdown. Therefore, it affects the device's interface state density, dielectric breakdown, leakage current, light emission intensity, light emission efficiency, and light chromaticity, which is an important factor for the performance of the SSI-LED.

Chapter VI describes the methods to estimate the electrical properties, i.e., the effective resistance and Schottky barrier height, of nano-resistors from the SSI-LED's current-voltage (*I-V*) curve. The temperature dependence of the nano-resistor effective resistance indicates the difference of nano-resistors from a conductor or a semiconductor. The effective barrier height increases with the increase of temperature, which is caused by the random and complicated formation of nano-resistors. The nano-resistor is fully developed after the 1 min stress.

Chapter VII focuses on two approaches to enhance the light emission characteristics of the SSI-LED, i.e., embedding the WO_x layer into the ZrHfO gate dielectric and using the heavily doped *p*-Si substrate for fabrication.

Chapter discusses the extensive applications of this novel nano-resistor device for the on-chip optical interconnect and the diode-like anti-fuse one-time programed NVM.

Chapter IX summarizes all studies in this dissertation and draws conclusions.

CHAPTER II

EXPERIMENTAL

2.1 Introduction

This chapter focuses on the experimental methods used in this dissertation. First, the process flow of fabricating the nanocrystal embedded high-*k* based NVM or the high-*k* based SSI-LED will be described in detail. Second, the background of RF magnetron sputtering, RTA, and PECVD will be introduced. Third, the material characterization instruments, such as profilometer, SIMS, AFM, and SEM will be discussed. Finally, the electrical and optical characterizations, such as, system setups as well as *C-V*, *G-V*, *J-V*, and light spectrum measurements, will be addressed.

2.2 Fabrication Process Flow

Figure 19 shows the process flow chart of fabricating a nanocrystal embedded high-*k* gate dielectric MOS capacitor, its corresponding control MOS capacitor, or a SSI-LED. In this dissertation, all the device will be fabricated on the <100> *p*-type Si substrate (resistivity 11-20 Ω·cm, doping concentration ~10^{15} cm^{-3}, supplied from MEMC). The sample size is about 1.5 inch×1.5 inch.

The bare Si wafer was pre-cleaned by a dilute hydrofluoric acid (DHF, 2 %) solution for 5 min to remove the native oxide on the Si surface. The Si surface changed from hydrophilic to hydrophobic after removal of native oxide. Then, the substrate was flushed with the deionized water (DI, resistivity > 18 MΩ·cm) for 5 min. After drying by

the N_2 blowing, the sample was immediately loaded into the load-lock chamber and transferred into the main chamber of the sputtering system.

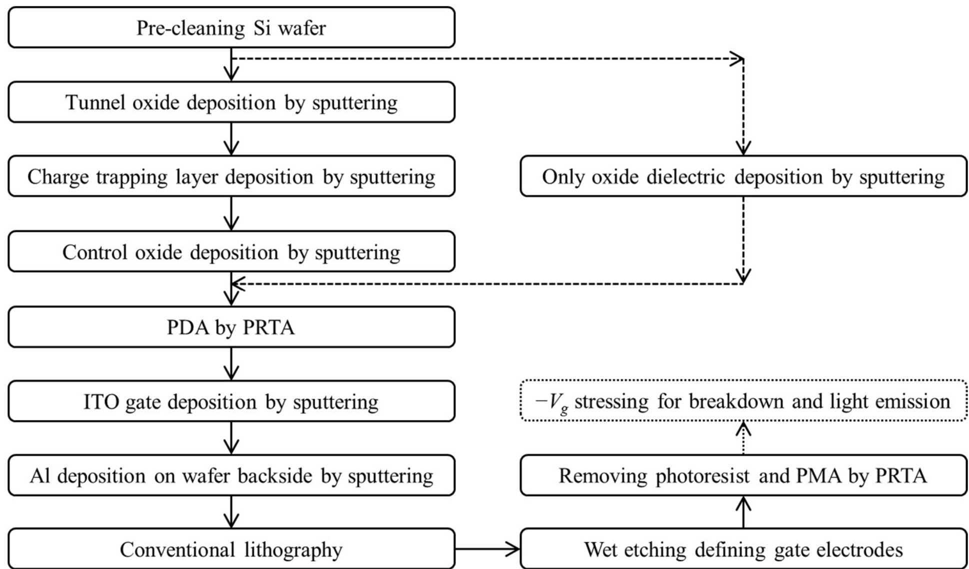

Figure 19. Fabrication process flow of a nanocrystal embedded high-*k* gate dielectric MOS capacitor, its corresponding control MOS capacitor, or a SSI-LED.

In this dissertation, the high-*k* stack was deposited by the RF (13.56 MHz) magnetron sputtering. The ZrHfO film was deposited by sputtering a Zr/Hf (12/88 wt %) composite target in Ar/O_2 (1:1) at 60 W and 5 mTorr. For the ZrHfO (tunnel) / CTL / ZrHfO (control) tri-layer structure, the sputtering deposition sequence was 2 min ZrHfO deposition for tunnel oxide layer, the CTL deposition, and finally 10 min for control oxide layer. The CTL deposition condition depended on the embedded material. For comparison, the control sample that contained only 12 min sputter-deposited ZrHfO high-*k* gate

dielectric film with the embedded CTL layer was prepared under the same condition. Or a simple high-*k* gate dielectric MOS capacitor was fabricated with only one step ZrHfO sputtering deposition for the SSI-LED investigation.

After the high-*k* stack deposition, the PDA step was carried out with a RTA equipment to densify the as-deposited film, passivate the defects, and transform the continuous CTL film into the discrete nanocrystal form. Two kinds of gases were in the PDA step, i.e., N_2 and O_2. The PDA condition varied from 800 ^oC to 900 ^oC for 1-3 min. After the PDA annealing, an 80 nm thick indium tin oxide (ITO) film was sputter-deposited from an ITO (99.99%) target in pure Ar at 80 W and 5 mTorr on top of the high-*k* stack. The ITO film was employed as the gate electrode due to its good conductivity and good interface contact with the metal oxide dielectric as well as the excellent transparency for the SSI-LED device. A 120 nm thick aluminum (Al) film was deposited, i.e., by sputtering an Al (99.999%) target in pure Ar at 80 W and 5 mTorr, on the backside of the Si substrate to form the ohmic contact.

The conventional lithography process was carried out to pattern the gate electrode. First, the positive photoresist (AZ Electronics, AZ 5214-E) was spin coated on the top of the ITO gate and the backside of the Al contact. The spin speed of the spin coater (Chemat Technology, KW-4A) was set as 3.5-4.0 krpm and a 1.5-1.8 μm thick photoresist was coated on the surface. Then, the sample was soft baked at 90 ^oC for 1 min on a hot plate to evaporate the solvent and increase the adhesion. After that, the sample was loaded to the Quintel Q4000 aligner, directly covered with a patterned quartz mask in the contact mode, and exposed to the UV light at 10 mW/cm^2 for 30 s. After the exposure, the

patterned photoresist film was developed in the MIF 300 developer (AZ Electronics) solution, which was composed of tetramethylammonium hydroxide that dissolved the UV-exposed photoresist. This process took 1-5 min. Next, the sample was hard baked at 125 ºC for 5 min in the oven to solidify the photoresist. After the hard baking, the ITO gate electrode was subsequently patterned by wet-etching non-photoresist-covered areas. The etching solution was aqua regia, i.e., HNO_3:HCl (1:3), and the average etching rate was about 1000 nm/min. The remaining photoresist was removed by the acetone ultrasonic bath for 1 min and the finished sample was washed by isopropyl alcohol (99.9999%) and DI. Finally, the complete device was annealed at 300-400 ºC in forming gas ($H_2/N_2 = 1:9$) for 5 min, i.e., the post metal annealing (PMA) treatment, to passivate the oxygen deficiencies and dangling bonds as well as facilitate the Al diffusion into Si for the ohmic contact formation.

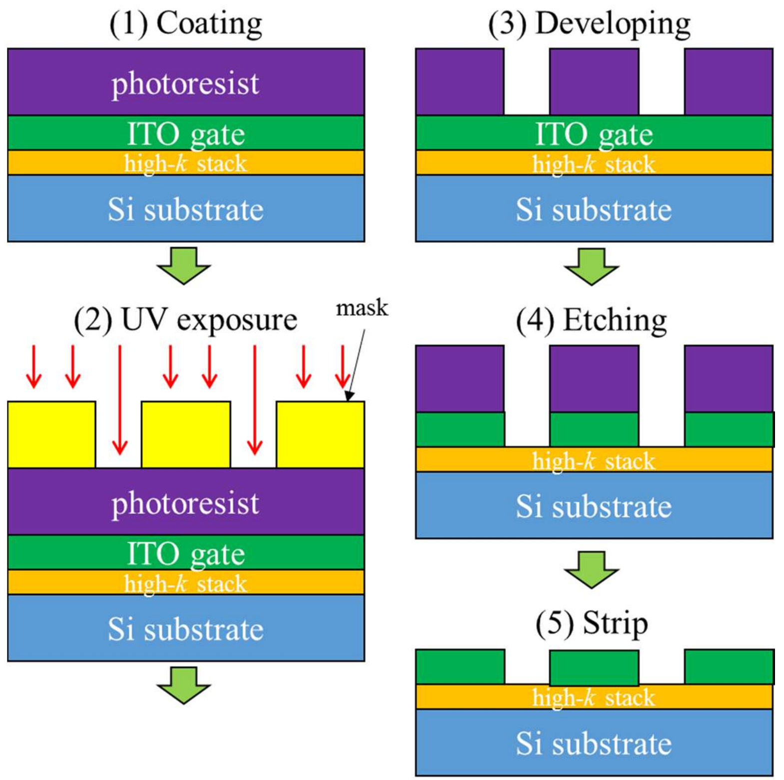

Figure 20. Illustration of the pattern transferring process.

2.3 Thin Film Deposition and Annealing

2.3.1 RF Magnetron Sputtering System

Figure 21 shows its schematic diagram of the sputtering system used in this dissertation, which is consisted of two chambers, i.e., load-lock and main chambers. Both chambers are made of the stainless steel, and vacuum sealed with the fluoroelastomers (Viton) O-rings and Cu gaskets.

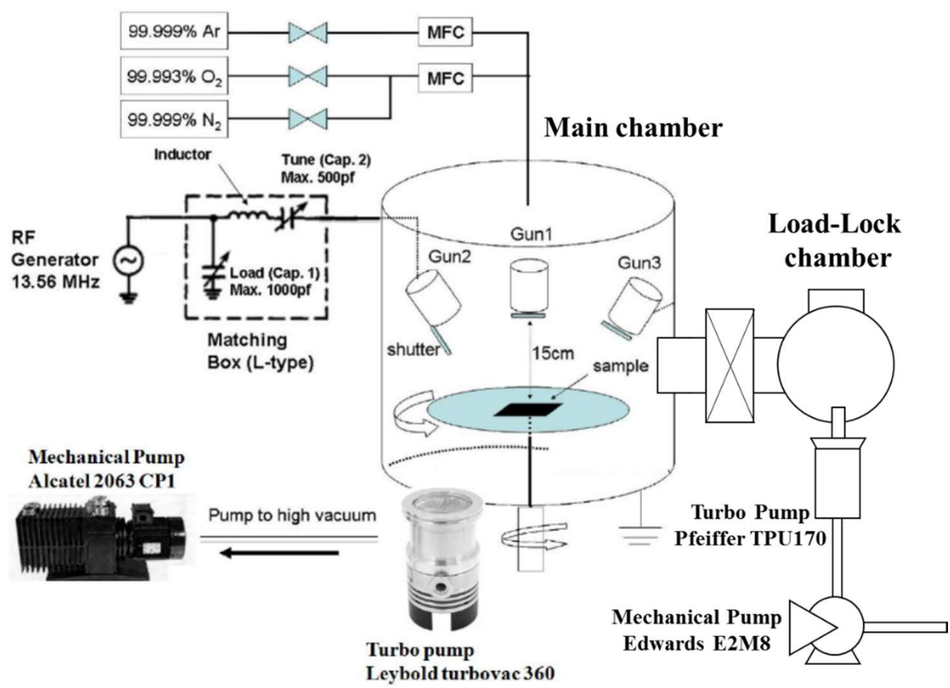

Figure 21. The illustration of the RF magnetron sputtering system.

After the sample loading into the load-lock chamber, it was subsequently pumped down to about 10^{-5} Torr by the combination of the mechanical pump (Edwards, E2M8) and turbo pump (Pfeiffer, TPU 170). This process takes about 20 min because of the chamber's small volume (15 L). Then, the sample was transferred into the main chamber of the sputtering system that was already in the high vacuum environment, i.e., $< 10^{-5}$ Torr. After the thin film deposition process, the sample was transferred back to the load-lock chamber without breaking the high vacuum environment in the main chamber. The main function of the load-lock system is to efficiently increase the sputtering deposition yield by avoiding the long pump down time of the main chamber and to minimize the exposure of the main chamber to the air contamination.

Before the deposition process, the main chamber was pumped down to the high vacuum condition, i.e., background pressure ~6×10^{-6} Torr, by the combination of the mechanical pump (Alcatel, 2063 CP1) and turbo pump (Leybold, Turbovac 360). This process takes a very long time i.e., > 4 hr, due to its large volume (65 L). There are three guns installed in the main chamber in which the target is 2 inch in diameter and 0.25 or 0.125 inch in thickness. Each gun is equipped with a permanent NdFeB magnet to magnetron control the plasma and with a shutter to mechanically start/shut off the deposition process. In addition, both the turbo pump and sputtering gun are water cooled by the cycling chiller system (Neslab, CFT-33). The sample holder can rotate at the speed of 10 rpm to improve the deposition uniformity. The distance between the sputtering gun and sample holder was about 15 cm. A RF generator and a matching box are connected to a gun to carry out the sputtering process. The matching box is consisted of two adjustable capacitors, i.e., load capacitor (Cap. 1, Max. 1000 pf) and tune capacitor (Cap. 2, Max. 500 pf), and one fixed inductor. By adjusting the load/tune capacitance, the impedance of the whole system can be matched to a certain value, e.g., 50 Ω, to minimize the reflected power. There are three kinds of gases supplied to the system, i.e., argon (Ar, 99.999%, research grade), oxygen (O_2, 99.993%), and nitrogen (N_2, 99.999%). Ar has its own MFC, while O_2 and N_2 share the same MFC. Therefore, the deposition can be done in three kinds of atmospheres, i.e., pure Ar, mixed Ar/O_2, and mixed Ar/N_2.

The RF sputtering system is also featured with the circularly-arranged magnetron control ability in this dissertation. Around the target, the magnetic field can greatly increase the ionization of the sputtering gas and the deposition rate.[84] The concept of the

magnetron enhancing sputtering is illustrated in Figure 22.[85] A magnetic field (B) is provided around the cathode (target) area, which is perpendicular to the electric filed (E). In this configuration, the electron movement is confined into the E×B direction, and its movement path changes from a linear style to a spiral one. Therefore, the magnetron control confines the plasma above the target in annular rings, which enhances the ionization of Ar atoms and in consequence, increases the sputtering efficiency.

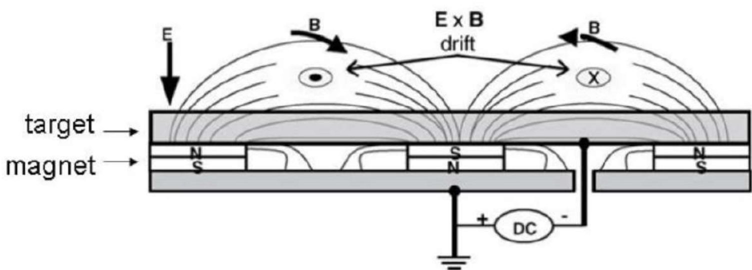

Figure 22. Schematic configuration of magnetron enhancement. (Reprinted with permission from Ref. 85. Copyright 2010 Elsevier.)

In this dissertation, the sputtering power was set to 60-100 W depends on the thin film material. This is because the high power process may cause the strong ion bombardment damage to the sample surface,[86] and the low power process may decrease the deposition rate and degrade the film quality due to the low energized sputtered atoms. On the other hand, the high process pressure can reduce the mean free path of sputtered atoms and atoms collide more times before reaching the substrate, which results in low deposition rate. Moreover, the plasma cannot be sustained in a too low process pressure.

Therefore, the process pressure is critical to the thin film quality. The sputtering process pressure in this work was set to 5 mTorr for all processes.

2.3.2 Rapid Thermal Annealing System

Figure 23 shows the schematic diagram of the RTA system (Modular, RTP 600-S) used in this dissertation.[87] The sample was placed on the 4 inch diameter Si wafer holder and heated in the quartz tube. The tungsten-halogen lamps combined with the closed-loop temperature control system and the water cooled assembly can provide a rapid heating and cooling speed. In addition, the temperature profile of the annealing process can be precisely controlled by this RTA system. Therefore, compared with the traditional furnace annealing, RTA process can greatly lower down the thermal budget. The RTA chamber was not vacuumed during the annealing process, however, a large gas flow, i.e., > 5 slpm, and a strong gas exhaust design can guarantee the purity of the annealing ambient. Three kinds of gases were used in the RTA system, i.e., N_2 (99.999%), O_2 (99.993%), and forming gas (H_2/N_2 = 1:9). O_2 has its own MFC, while N_2 and forming gas share the same MFC. Therefore, the mixed N_2/O_2 ambient is also available.

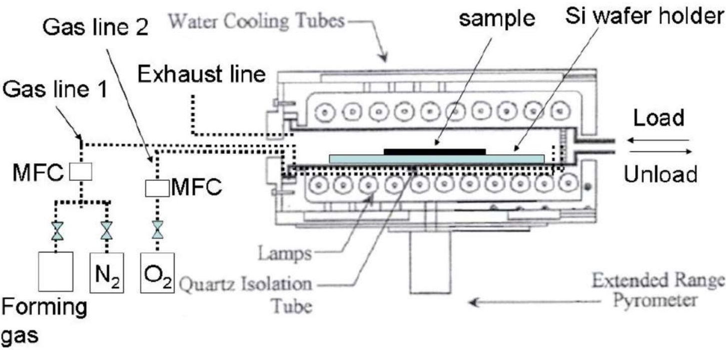

Figure 23. Schematic diagram of RTA system. (Adapted from Ref. 87.)

2.3.3 Plasma Enhanced Chemical Vapor Deposition

The hydrogenated amorphous silicon (*a*-Si:H) and SiN_x films in this dissertation were prepared by the Applied Materials AMP Plasma I PECVD. The PECVD system has a parallel-plate-electrode configuration with the electrode diameter of 65 cm and the electrode distance of 6.25 cm. The feed gases of SiH_4 (semiconductor, 99.999% Air Liquide), NH_3 (semiconductor, 99.999% purity, Matheson Tri-Gas), H_2 (semiconductor, 99.9999% purity, Praxair), and N_2 (semiconductor, 99.9999% purity, Praxair) are introduced into the PECVD and the gas flow rate is controlled by the independent MFCs. The pressure control system in PECVD includes an angle valve, a booster pump, mechanical pump, and capacitor manometer. The temperature system is made of three-zone heater and controllers that maintain the chamber at 260 ºC. The plasma system consists of a 13.56 MHz RF generator (OEM-12A, ENI), a pi-type matching network (MW-10, ENI), and a plasma controller. The top electrode of the PECVD chamber is

powered with the RF generator and the bottom electrode and the wall are grounded. The whole system is controlled by PC with LabWindow/CVI interface (National Instrument).

2.4 Material Characterization

Material properties of the bulk high-*k* films and interface layers were thoroughly investigated in this dissertation. The background knowledge of each equipment will be introduced in this section. The profilometer technique was used to measure the film thickness and the size of the gate electrode pattern. For precisely calculating the electrical characteristics, the device's gate area is critical and needs to be measured carefully. The SIMS provided depth profiles of elements from the ITO gate to the Si substrate of the device. The AFM scanned through the sample surface and exhibit the detail information of the device topography in high resolution. The SEM provided high resolution top-view micrographs of a sample surface.

2.4.1 Profilometer

The vertical profile of a sample surface can be obtained by the Dektak^3 stylus profilometer that utilizes a diamond stylus of 5 μm in radius to horizontally scan the sample surface. From the vertical profile, the thickness and diameter of the gate electrode pattern can be precisely determined. During the horizontal scan, the stylus is kept distant to the sample surface by a contact force. This force is in the micron newton (mN) range and can be maintained as constant due to the cantilever system operating on the spring mechanic principle. The resolution in the horizontal direction is governed by the scan

speed and stylus radius, while that in the vertical direction is governed by the stylus radius and cantilever system. This profilometer can accurately measure step heights from below 10 nm to over 50 μm with a resolution of 1 nm.

2.4.2 Secondary Ion Mass Spectrometry

The SIMS elemental depth profile was obtained from the CAMECA IMS 4f ion microprobe. Figure 23 shows the fundamental phenomenon in a SIMS.[88] This is based on ion-induced sputtering of a solid sample by an energetic primary ion beam, e.g., O^- or Cs^+ ions with the ipmact energy of 5-20 keV.[89] When these primary ions hit on the sample surface, they start collision cascade, i.e., multiple quasi-elastic collisions induced by the bombarding ions. In some collision, momentums exchange between the bombarding ions and the atoms in the sample. A very small fraction of surface atoms can acquire the momentum in the direction away from the bulk of the sample. As the gained energy is larger than the binding energy, then the atom or particle can be ejected from the surface. The ejected atoms or particles can be electrically neutral, as well as positively and negatively charged, i.e., secondary ions. With the aid of an electrical field, these secondary ions can be extracted from the sputtering area into a mass spectrometry. There, they are sorted by mass and finally counted in an ion detector, which give the composition information at the sputtering area. The SIMS can detect all elements in the depth profiling and surface mapping. Detection limits are in the ppb range with depth resolution of 10 nm and lateral resolution of ~ 3μm. In this dissertation, the elemental profile of the sample was measured from the top of the ITO electrode to the Si substrate with the SIMS using

the Cs^+ ion beam at 5.5 keV and the incident angle of 43° in the positive charge secondary ion mode. The signal was obtained from an area of 50 µm ×50 µm on the specimen.

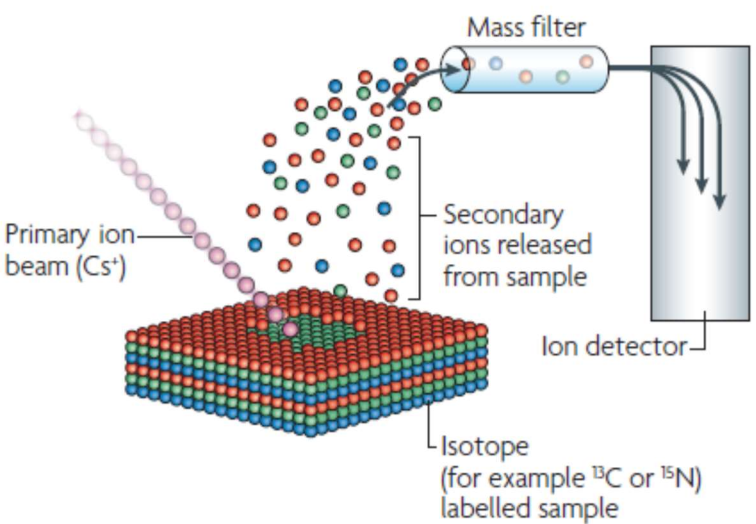

Figure 24. Schematic illustration of a SIMS. (Reprinted with permission from Ref. 88. Copyright 2007 Nature.)

2.4.3 Atomic Force Microscopy

The Dimension Icon AFM (Bruker) is primarily used to study surface morphology, topography, and interaction forces between the tip and sample. AFM consists of a sharp nanometer-sized probe attached to a springboard or V-shaped cantilever which is positioned over a surface deposited sample as shown in Figure 25.[90] Piezoelectric scanners control sub-nanometer movements in the x, y, and z dimensions, then images are compiled line-by-line as the sample is raster scanned. Additionally, a laser beam is focused on the

back-tip of the cantilever to measure changes in cantilever deflection. The deflection is caused either by sample topography changes or by interaction force changes. These changes are converted to force using Hooke's law, which allows for the quantification of forces on the pN scale and the employment of force spectroscopy. The tapping mode is used to prevent the possible damage from high local stress. In this mode, the cantilever is excited into oscillations near its resonant frequency and taps along the surface with constant oscillation amplitudes. Any displacement in the z dimension is a measure of the height variation on the sample.

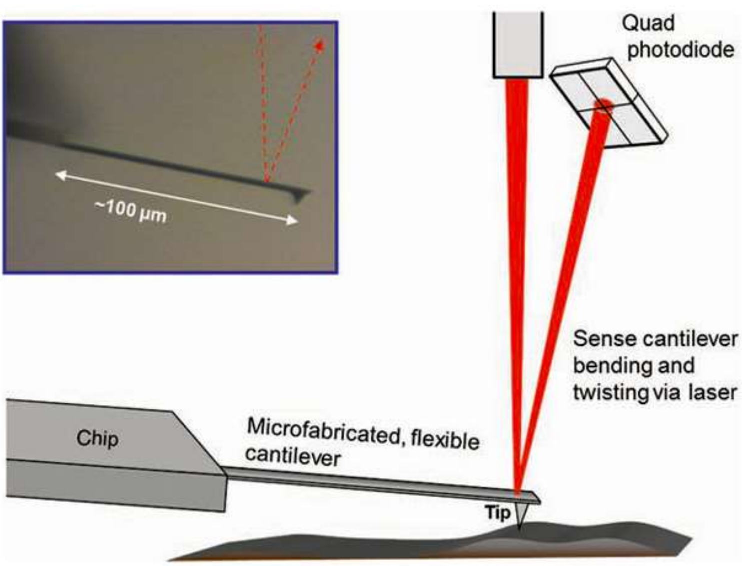

Figure 25. Schematic illustration of an AFM. (Reprinted with permission from Ref. 90. Copyright 2012 Wiley.)

2.4.4 Scanning Electron Microscope

SEM can provide high resolution images of a sample surface. The SEM used in this dissertation is a cold cathode analytical Field Emission (FE) SEM (JEOL, JSM-7500) system. High density electrons are emitted when a strong electric field is applied to a cathode with a sharpened tip. Compared to the thermal emission filament based SEM, the FE based SEM has some advantages such as the smaller diameter emitted beam and longer filament life because the emission is cool. The former can effectively increase the resolution.[91] However, the FE gun requires much higher vacuum, i.e., 10^{-7} Torr.[91] The highly coherent electron beam strikes the sample surface and results in the emission of backscattered and secondary electrons. The former is the high energy electrons that are ejected by an elastic collision of an incident electron. The latter is from the inelastic scattering of the lower energy electrons. Each of which can be detected by specialized detectors. The signal collected by the detector is amplified and converted into a digital image. Usually the secondary electron imaging mode provides high-resolution imaging of fine surface morphology and the backscatter electron imaging mode provides image contrast as a function of elemental composition and the surface topography. The SEM micrographs in this dissertation were all taken under the secondary electron imaging mode. Moreover, if the material of the sample is not highly conductive, the charges can be accumulated on the sample surface and block the interaction of the electron beam. Therefore, the samples used in this dissertation are all coated with a thin highly conductive platinum (Pt) film layer by a sputtering machine, which can effectively prevent the surface

charging and avoid the image distortion. Figure 26 shows the illustration of a basic SEM equipment.

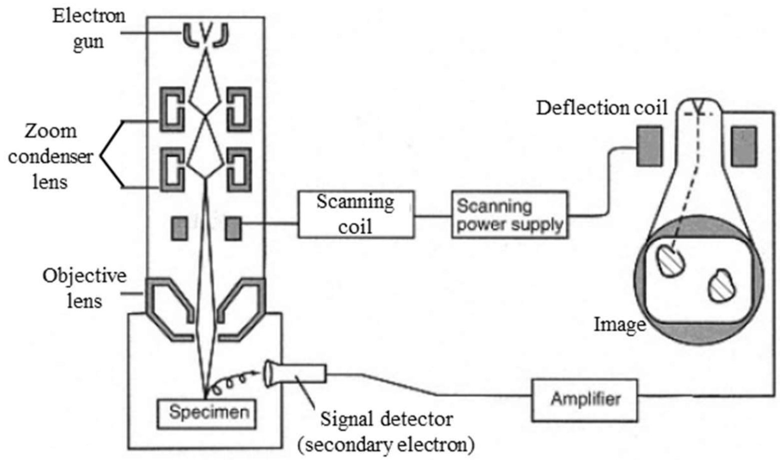

Figure 26. Schematic diagram of SEM. (Adapted from Ref. 91.)

2.5 Electrical Characterization

2.5.1 Electrical Characterization System Setup

Electrical characterizations of the nanocrystals embedded ZrHfO high-*k* MOS capacitors and SSI-LEDs, e.g., frequency dependent capacitance-voltage (*C-V*), conductance-voltage (*G-V*) measurements, current density-voltage (*J-V*), and constant voltage stress (CVS) were performed to investigate the gate dielectric properties and nonvolatile memory functions. The entire measurement process was carried out very carefully in a grounded box, which insulated the process from the outside environment disturbance, such as lights, noises, heats, and vibrations as shown in Figure 27. The box

is made of Al and painted to flat black in order to avoid any light radiation. Inside of the box, the measurement was performed on the probe station (Signatone, S-1160). The sample was placed on the gold alloy chunk and a vacuum was utilized to prevent from the sample shock during the measurement. A thermal probing system (Signatone, S-1060R) was wired to the chunk and heat it up to 600 ^{o}C (Max.) for the temperature-dependent electrical test. Additionally, the chunk was electrically floated to prevent from driving signals to the ground. The measurement probe tip is made of tungsten with a diameter of 1 μm. The chunk and the probe were connected to the measurement machine by biaxial or triaxial cables. *C-V* and *G-V* curves were measured with the Agilent 4284A LCR meter; *J-V* curves and CVS test were measured with the Agilent 4155C semiconductor parameter analyzer or the 4140B pA Meter / DC Voltage Source. The National Instruments LabVIEW 7 program was used to control the whole measurement process through the GPIB interface.

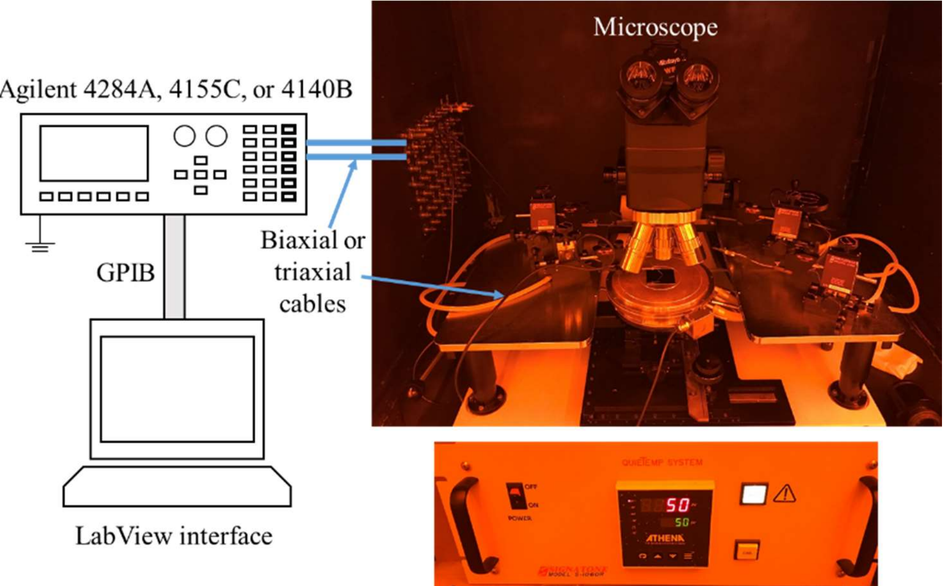

Figure 27. Schematic diagram of electrical characterization system setup.

2.5.2 *C-V and G-V Curves Measurement*

Many critical electrical properties of the device, such as EOT, flat band voltage (V_{FB}), D_{it}, and oxide trapping density (Q_{ot}) can be extracted from the *C-V* and *G-V* curve.[92] Moreover, the frequency-dependent (100 kHz to 1 MHz) measurement can be used to locate the charge trapping sites in the nanocrystals embedded high-*k* NVM devices. The measurement principle is: during a linear DC bias swept in the desired gate voltage range, a high frequency small sinusoidal AC signal of 0.25 V is superimposed simultaneously to extract the differential *C* and *G*, which can be expressed as the following equations,

$$C = \frac{dQ}{dV}, \quad [8a]$$

$$G = \frac{dI}{dV}. \quad [8b]$$

Usually, the CPG mode, i.e., *C* and *G* are parallel to each other in the G-C circuit, is selected to perform the *C-V* and *G-V* measurement. By measuring the impedance of the parallel *G-C* circuit, i.e., ratio of the output AC current to the input AC voltage, the capacitor's *G* and *C* values can be obtained at the same time.[92] The impedance (Z) of the *G-C* circuit can be expressed as the following equation,

$$Z = \frac{G}{G^2 + (\omega C)^2} - \frac{j\omega C}{G^2 + (\omega C)^2}, \qquad [9]$$

where is the angular frequency of $2\pi f$, and f is the frequency of the superimposed AC voltage signal.[92] The series resistance existed in the measurement system is unavoidable and needs to be minimized. A good electrical contacts is important to minimize the series resistance and moreover, the separate correction processes in the "open" mode (i.e., no contact between the probe tip and chunk) and in the "short" mode (i.e., the probe tip and chunk contact each other) were developed to further improve the accuracy of the measurement.[93] In the dissertation, the NCSU CVC program proposed by Hauser et al was used to extract V_{FB}, D_{it}, and Q_{ot}.[94] This program appropriately corrects the quantum confinement effect measurement errors when the high-*k* film is extremely thin, i.e., < 3 nm.

2.5.3 J-V Curve Measurement

The *J-V* curve measurement was performed to investigate the charge transport mechanism, such as Schottky emission (SE), Poole-Frenkel (P-F), and F-N tunneling, as well as the charge trapping/detrapping phenomena in the device. The basic principle of

the J-V measurement is to apply a DC bias on the capacitor via the probe tip, and then receive the current signals from the same probe tip. The voltage profile of the DC bias can be either in the ramp mode or in the stepwise mode. For the ramp mode, the measured current may be contributed by the gate leakage current and displacement current. In order to minimize the latter, therefore, the DC bias ramping with a very slow speed, i.e., 0.01 V/s, is usually used. For the stepwise mode, a relatively long delay time between each step, e.g., about 500 ms, can be also adopted to achieve the same purpose.

Furthermore, the dielectric breakdown mechanism of the ZrHfO high-k MOS capacitor can be investigated using the ramp-relax and CVS methods.[95,96] For the ramp-relax test, a stepwise ramp voltage (V_{ramp}) was firstly applied to the gate and at the same time, the leakage current, i.e., the ramp current (J_{ramp}), was measured. Then, the V_{ramp} was removed, which was followed by the immediate measurement of the gate current, i.e., the relaxation currents (J_{relax}), at the gate voltage (V_g) of 0 V. The above procedures were repeated from V_{ramp} = 0 V to −10 or −12 V with an interval of 0.05 or 0.1 V. On the other hand, The CVS test was done by stressing the gate with a constant voltage for a period of time, e.g., at of V_g = −7 V for 10,000 s. The breakdown of the high-k stack occurred at the time when the leakage current jumped by several orders of magnitude. The time-dependent dielectric breakdown (TDDB) was plotted with respect to the Weibull distribution based on the CVS measurements of multiple devices.

2.6 Optical Characterization

2.6.1 Optical Characterization System Setup

The optical characterization, i.e., measuring the light emission spectrum, was done on the same probe station in the black box as described in the section 2.5.1. Figure 28 shows the setup for the optical characterization. The SSI-LED was driven by a DC V_g supplied by the Agilent E3645A power supply with the maximum voltage of 65 V. An optical emission spectrometer (OES, StellarNet BLK-C-SR-TEC) connected by a 1 m long optical fiber with 1,000 μm core diameter receptor was used to record the light emission spectrum. As shown in Fig. 28, the receptor was set right above the ITO gate of the SSI-LED, i.e., its surface was parallel to the device surface, in the distance of 0.2 cm. The OES was cooled with fans for stable signal/noise ratio under long-time exposure. It was calibrated in the dark in the black box, i.e., taking the dark reference. The integration time was set at 30,000 ms and the average sampling was set at 1 for maximizing the collection of photons. The light emission spectrum was recorded in the "watts mode".

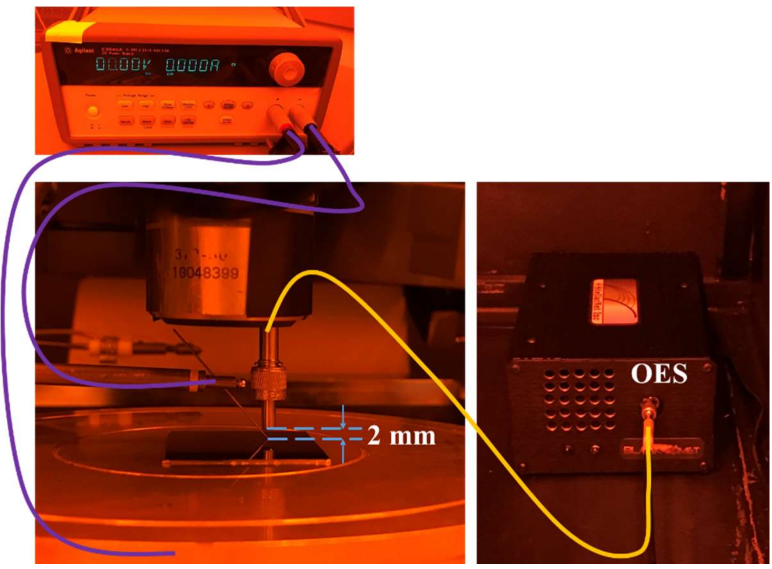

Figure 28. Schematic diagram of optical characterization system setup.

2.6.2 Light Chromaticity

Based on the light emission spectrum, the light color characteristics, such as the chromaticity coordinates on the International Commission on Illumination (Commission internationale de l'éclairage, CIE) chart, correlated color temperature (CCT), and CRI value were calculated using the NIST CQS 7.4 program to quantitatively compare the SSI-LED's light quality.[97] In the CIE 1931 chart, the chromaticity coordinates, x, y, and z represent the actual color as perceived by an average observer, which can be calculated using the following equations,[98]

$$x = \frac{X}{X+Y+Z}, \quad [10a]$$

$$y = \frac{Y}{X+Y+Z}, \quad [10b]$$

$$z = \frac{Z}{X + Y + Z}. \quad [10c]$$

These tristimulus values *X*, *Y*, and *Z* can be expressed as the equations below:

$$X = \int \bar{x}(\lambda) S(\lambda) d\lambda, \quad [11a]$$

$$Y = \int \bar{y}(\lambda) S(\lambda) d\lambda, \quad [11b]$$

$$Z = \int \bar{z}(\lambda) S(\lambda) d\lambda, \quad [11c]$$

where $S(\lambda)$ is the spectral power distribution as well as $\bar{x}$, $\bar{y}$, and $\bar{z}$ are the color matching functions that are similar to the spectral sensitivity of the cones in our eyes, as shown in Figure 29. The ideal chromaticity coordinates for a white-light source are x = 0.333, y = 0.333, which is known as the equal energy point. The Planckian locus (also named black body locus) is the locus that the color of an incandescent black body would take in the 1931 chromaticity space as the black body temperature changes, as shown in Figure 30.

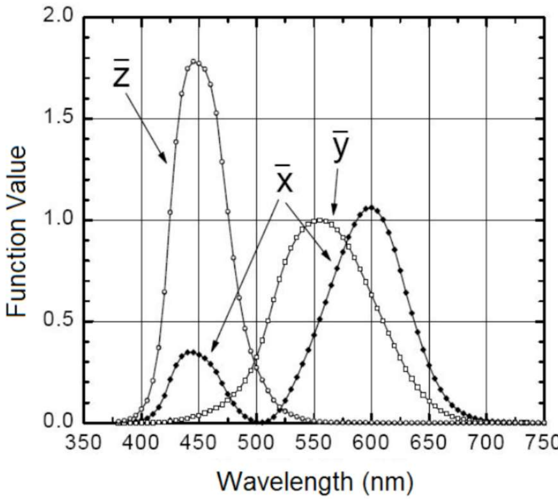

Figure 29. The 1931 CIE color-matching functions. (Reprinted with permission from Ref. 99. Copyright 2002 Wiley.)

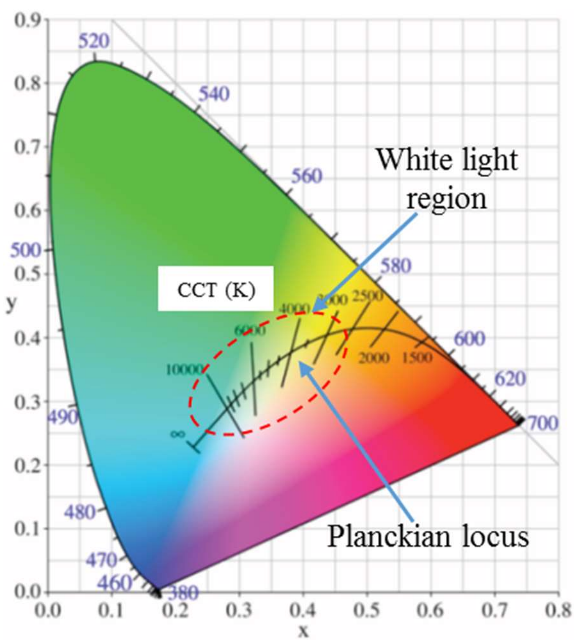

Figure 30. The 1931 CIE chart with the Planckian locus. (Adapted from Ref. 100.)

The CCT is a specification of the color appearance of the light emitted by a light source, relating its color to the color of light from a reference source (black body) when heated to a particular temperature. Generally, for the purpose of calculating the CCT, the color coordinates of CIE 1931 need to be transformed into the color coordinates of CIE 1960.[101] Then, the CCT of the emitted light is defined as the color temperature on the Planckian locus nearest to the color coordinates location on the CIE 1960 chart.[101] The light sources with the CCT below 3,200 K are considered as the "warm" sources, while those with the CCT above 4,000 K are considered as the "cool" sources. The conventional incandescent light has a CCT of 2,700 K.

The CRI is a value of the ability of an artificial light source to reproduce colors of an object illuminated by the light source. The CRI values scale from 0 to 100. The larger value represents a more natural and vivid artificial light source. The distance between the color coordinates location on the CIE 1960 diagram and the Planckian locus, i.e., chromaticity distance, is used to calculate the CRI.[102] The literatures usually report two kinds of CRI, i.e., R_a and R_9. R_a is usually referred as the "general CRI" that is the average value of R_1 to R_8.[103] The R_a of a black body light source, e.g., incandescent light bulb, is 100. R_9 corresponds to the color rendering of the deep-red region, is usually referred to the "special CRI". The R_9 value is critical to the biomedical and painting applications.[104] These two CRI values were reported as the reference in this dissertation.

2.6.3 Light Emission Efficiency

It is difficult to measure the light emission efficiency of a single SSI-LED because of the small size, i.e., 300 μm in diameter, and the lack of a proper characterization equipment. Assuming that light is emitted isotopically from the ITO electrode in the hemisphere shape,[61] the relative light emitting efficiencies of SSI-LEDs can be compared from their emission spectra because they are measured under the same condition. The external quantum efficiency (*EQE*) of a SSI-LED can be estimated by dividing the number of emitted photons (*NP*) with the total number of injected electrons using the following equations:

$$EQE = \frac{NP}{I/q}, \quad [12a]$$

$$NP = \frac{2\pi r^2}{A_{slit}} \int \frac{E(\lambda)}{hc/\lambda} d\lambda, \quad [12b]$$

where I is the current in amps (A), q is the charge of an electron, $2\pi r^2/A_{slit}$ is the factor of fraction of light collected by an entrance slit, $E(\lambda)$ is the irradiance of the light source.[105] There has a distance between the light source and the receptor of the optical fiber, i.e., r = 2 mm, and therefore, the light intensity will be underestimated. In this case, the factor of fraction of light collected needs to be considered. The light is emitted isotropically from the device and the irradiance should be equal at all points along a hemispherical distance from the SSI-LED. The reason why the hemisphere is used is because that there has no light emitted from the backside of the device. The cross-sectional area of the entrance slit, i.e., A_{slit}, is 1,000 μm × 100 μm.

CHAPTER III

CADMIUM SULFIDE EMBEDDED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K NONVOLATILE MEMORIES

3.1 Introduction and Motivation

Nanocrystals made of various materials, such as ZnO, ITO, RuO, MoO, and CdSe, have been embedded in the ZrHfO high-*k* gate dielectric to achieve the large memory window and long charge retention time.[95,106-113] However, electrical properties of these devices often deteriorate due to the frequency dispersion problem caused by defects located at the nanocrystal/dielectric interface.[109,110,112-114] CdS is an *n*-type semiconductor with a large electron affinity of 4.3 eV, which makes it a promising candidate for charge trapping in the dielectric layer.[54] Since CdS forms a good interface with the oxide dielectric,[115] which can potentially reduce the frequency dispersion phenomenon and improve the memory properties. In this chapter, MOS capacitors made of the CdS embedded ZrHfO gate dielectric were fabricated to investigate its nonvolatile memory characteristics.

3.2 Experimental

MOS capacitors with the tri-layer gate dielectric, i.e., ZrHfO (tunnel oxide)/embedded CdS/ZrHfO (control oxide), were fabricated on a *p*-type <100> Si (10^{15} cm^{-3}) wafer that was pre-cleaned with a DHF solution. The tri-layer gate dielectric was sputter-deposited in 3 steps in one pumpdown without breaking the vacuum. The ZrHfO

tunnel and control oxide layers were deposited from the Zr/Hf composite target in Ar/O_2 (1:1) at 5 mTorr and 60 W for 2 and 10 min, respectively. The CdS layer was deposited from a CdS target in Ar at 5 mTorr and 60 W for 3 or 5 min. Then, the PDA step was carried out at 900 °C in N_2 for 3 min. Then, the high-k stack was deposited with an 80 nm thick ITO film followed by wet etching into 100 µm-diameter gate electrodes. After the backside of the Si wafer was deposited with an Al ohmic contact layer, the sample was annealed at 400 °C in H_2/N_2 (1:9) for 5 min. In previous studies, it was observed that for the similar tri-layer structure, the originally amorphous embedded layer was transformed into discrete nanocrystals after the same PDA step. [109,110,112] At the same time, a Hf-silicate ($HfSiO_x$) interface layer (IL) was formed between the tunnel ZrHfO layer and the Si substrate. [109,110,112] Therefore, it is assumed that the embedded CdS film was also changed into nanocrystals, i.e., nc-CdS, in the final capacitor, as shown in Figure 31(a). For the comparison purpose, a control sample that contains the 12-min sputter deposited ZrHfO high-*k* gate dielectric film without the embedded CdS layer was prepared under the same above process condition, as shown in Fig. 31(b).

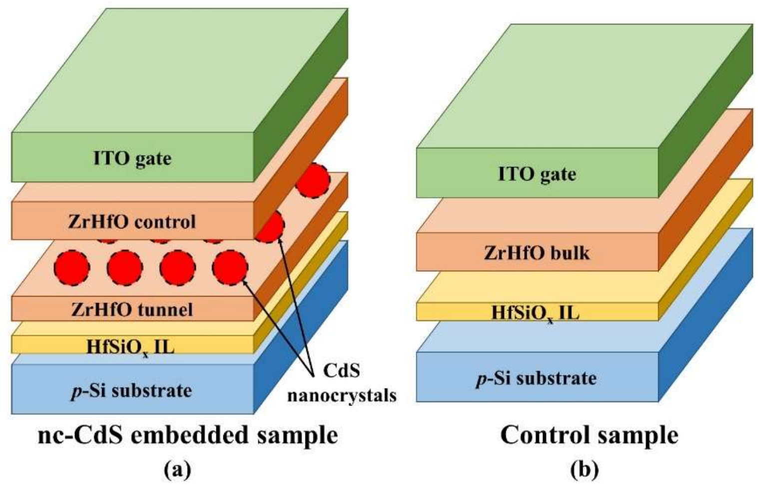

Figure 31. Drawing of the device structures of the (a) nc-CdS embedded and (b) control samples.

3.3 Nonvolatile Memory Functions of CdS Embedded ZrHfO Gate Dielectric MOS Capacitors

Figure 32 shows *C-V* hysteresis curves of the control and nc-CdS embedded samples that were measured with the V_g swept from −5 to +5 V (forward) and then back to −5 V (backward) at 1 MHz. The CdS-3min and CdS-5min represent samples containing the 3- and 5-min deposited CdS layers, separately. The control sample shows a very small *C-V* hysteresis window, which indicates the very small number of charge trapping sites in the bulk ZrHfO layer and the ZrHfO/Si interface.[116] However, when the nc-CdS layer is embedded in the high-*k* film, the hysteresis window becomes large and obvious. The memory window is defined as the difference of V_{FB}'s of the forward and backward curves, i.e., $\Delta V_{FB} = V_{FB,\text{ backward}} - V_{FB,\text{ forward}}$. The Q_{ot} of the device could be calculated using the following equation:

$$Q_{ot} = \frac{C \times \Delta V_{FB}}{q}, \qquad [13]$$

where C is the capacitance in the accumulation region.[116] The Q_{ot}'s of the control, CdS-3min, and CdS-5min samples are 2.39×10^{11} cm^{-2} , 2.63×10^{12} cm^{-2}, and 3.27×10^{12} cm^{-2}, separately. Therefore, the embedding of the nc-CdS layer increases the charge trapping capability of the capacitor. Table 1 summarizes parameters of samples extracted from C-V curves in Fig. 32. The inclusion of nc-CdS in the high-k stack should increase its physical thickness. However, the nc-CdS embedded samples show larger capacitances than the control sample does, i.e., 4.98×10^{-11} F (CdS-3min) and 5.54×10^{-11} F (CdS-5min) vs. 4.22×10^{-11} F (control). It was reported that the embedded CdS layer could hinder the diffusion of O from the control oxide through the high-k stack to reach the ZrHfO/Si interface,[117,118] which reduced the growth of $HfSiO_x$ interface layer. Therefore, the increase of the capacitance may be due to the reduced total thickness of the high-k stack, i.e., the summation of the high-k bulk and the $HfSiO_x$ interface layers. On the other hand, since less O can reach the ZrHfO/Si interface to passivate Si dangling bonds, the interface state density becomes larger. For example, D_{it}'s are 1.49×10^{10} cm^{-2}·eV^{-1} for the control sample vs. 2.31×10^{11} cm^{-2}·eV^{-1} and 4.55×10^{11} cm^{-2}·eV^{-1} for the nc-CdS embedded samples.

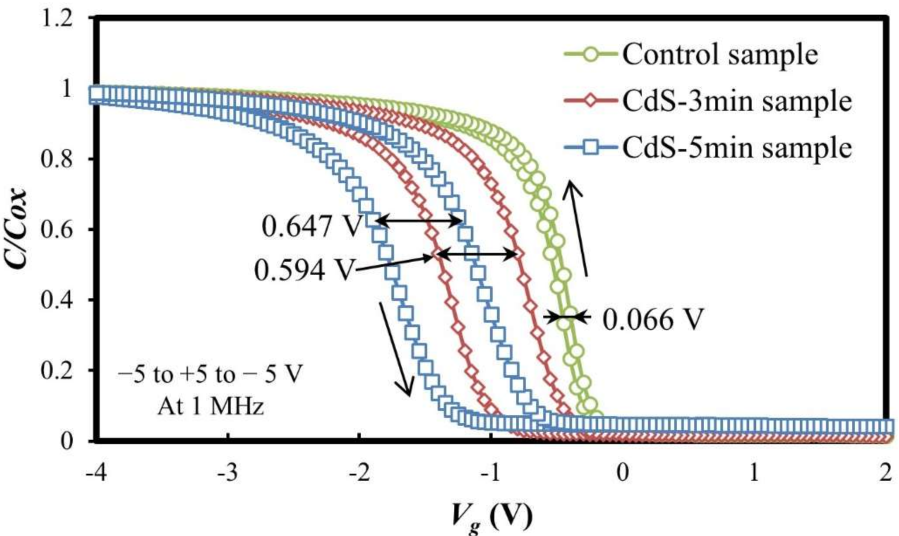

Figure 32. *C-V* hysteresis curves of the control and nc-CdS embedded samples. V_g swept from −5 to +5 to −5 V at 1 MHz.

Table 1. Parameters calculated from *C-V* hysteresis curves.

	C (F)	EOT (nm)	D_{it} ($cm^{-2}\cdot eV^{-1}$)	ΔV_{FB} (V)	Q_{ot} (cm^{-2})
Control	4.22×10^{-11}	6.13	1.49×10^{10}	0.066	2.39×10^{11}
CdS-3min	4.98×10^{-11}	5.21	2.31×10^{11}	0.594	2.63×10^{12}
CdS-5min	5.54×10^{-11}	4.70	4.55×10^{11}	0.647	3.27×10^{12}

To further investigate the charge trapping behavior of the nc-CdS embedded high-*k* stack, *C-V* curves were measured in two opposite V_g sweep procedures, i.e., one from −5 to +5 to −5 V and the other one from +5 to −5 to +5 V, as shown in Figure 33. The *C-V* curves of the "fresh" sample were measured in a small voltage range of V_g = −2 to +1 V, which can be assumed to trap a negligible amount of charges. Compared with the "fresh" sample, *C-V* curves swept from V_g = −5 to +5 V shift toward the negative V_g

direction due to the trap of holes.[113,118] When the sample is swept from V_g = +5 to −5 V, C-V curves either just overlap with those of the "fresh" sample or shift toward the negative V_g direction depend on the starting V_g. For the sample with the C-V sweep started at V_g = +5 V, no charges trapping is detected, which indicates the poor electron trapping capability.[116,118] For the sample with the C-V sweep starting at V_g = −5 V, the curve shifts toward the negative V_g direction even after the "backward" sweep, which indicates the strong trap of holes in the device.[116,119] There are several possible explanations of the preference of the hole trapping over the electron trapping. First, in the *p*-type Si substrate, it is easier to form the hole-rich accumulation layer than the electron-rich inversion layer when stressed with V_g's of the same magnitude but different polarity.[108] Second, the CdS is an *n*-type semiconductor which favor the trap of holes.[109,112] Furthermore, it was reported that the incorporation of O in CdS could shift the Fermi level to the conduction band, which enhanced the *n*-type characteristics.[120] Because of the strong hole trapping and poor electron trapping, memory windows of C-V curves swept from +5 to −5 to +5 V are larger than those from −5 to +5 to −5 V, i.e., 0.967 V vs. 0.594 V for the CdS-3min sample and 1.170 V vs. 0.647 V for the CdS-5min sample. The more CdS is embedded in the high-*k* stack, the more charges are trapped, which corresponds to a larger memory window.

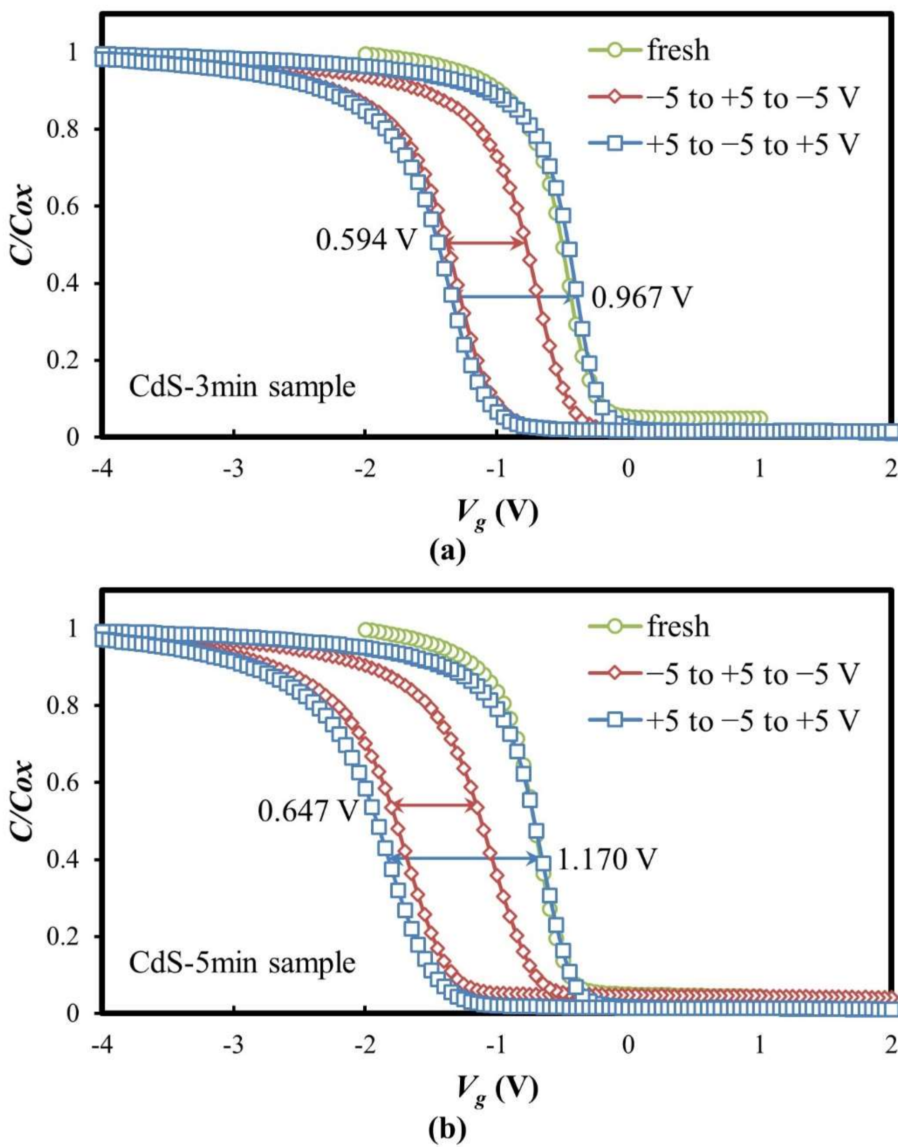

Figure 33. *C-V* hysteresis curves of the nc-CdS embedded samples. V_g swept from −5 to +5 to −5 V or +5 to −5 to +5 V at 1 MHz. Fresh: −2 to +1 V at 1 MHz.

There are two possible hole-trapping sites in the nc-CdS embedded device, i.e., within the bulk nc-CdS or at the nc-CdS/ZrHfO interface. These sites show different

retention characteristics. Figure 34 shows frequency-dependent *C-V* and *G-V* curves of the control and nc-CdS embedded samples measured from $V_g = -5$ to +5 V at different frequencies, i.e., 100 kHz, 500 kHz, and 1 MHz. For the control sample, all *C-V* curves almost overlap independent of the measurement frequency. Also, the *G-V* peak location and height change slightly with the frequency. This result can be contributed by the few defects at the $HfSiO_x$ interface layer.[110,121] The nc-CdS embedded samples also show negligible frequency dispersion on the *C-V* curve and the *G-V* peak. It was reported that, in the nanocrystal embedded high-*k* NVMs, those charges loosely trapped at the nanocrystal/high-*k* interface could keep pace with the low measurement frequency and tunnel back to the Si substrate.[109,110,112,113] This could cause a *C-V* curve shift, a *G-V* peak location shift, or a *G-V* peak height drop.[109,110,112,113] Since the above phenomenon does not occur on the nc-CdS embedded samples, the number of defects at the nc-CdS/ZrHfO interface must be low. The low number of nanocrystal interface defects may be due to the passivation effect of the S atoms released from CdS or O atoms during the annealing process.[122,123] On the other hand, the nc-CdS embedded samples have higher *G-V* peak heights than that of the control sample. A larger amount of holes are strongly trapped in the nc-CdS bulk. This causes a larger energy loss and the higher *G-V* peak.[121,124] Furthermore, the more CdS are embedded in the high-*k* film, the more hole tapping sites exist, which results in the increase of the *G-V* peak height.

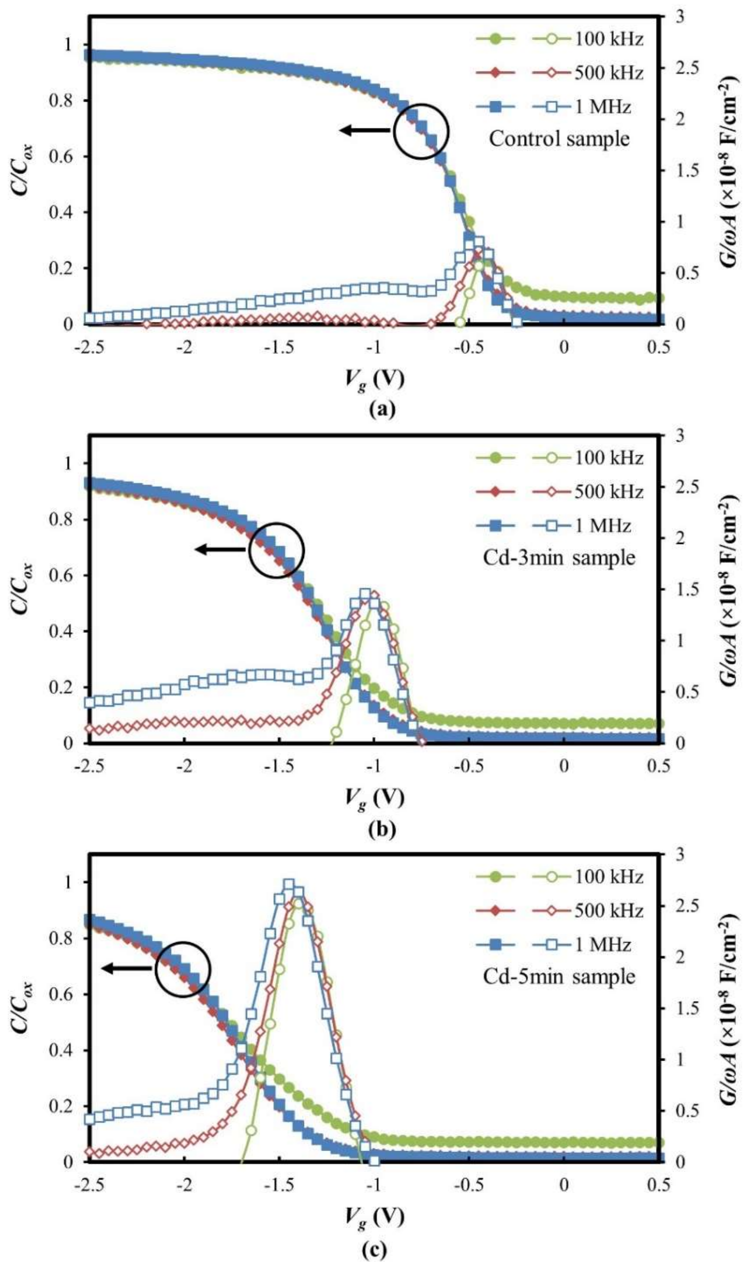

Figure 34. Frequency-dependent *C-V* and *G-V* curves of the (a) control and (b)(c) nc-CdS embedded samples. V_g swept from −5 to +5 to −5 V at 100 kHz, 500 kHz, and 1 MHz.

Figure 35 shows energy band diagrams of the nc-CdS embedded sample under the a) unbiased and (b) negative V_g stress conditions. Assuming that the work function and band gap energy of the nc-CdS are the same as those of the bulk CdS,[125] the conduction and valence band offsets of the nc-CdS to the ZrHfO dielectric are different, as shown in Fig. 35(a). Instead of interface states, a thin interface layer at the nc-CdS/ZrHfO contact region is included, of which the work function and band gap energy are assumed to be the same as those of CdO.[125] Under the negative V_g stress, holes tunnel through both the ZrHfO/Si interface and the tunnel oxide layers to reach the nc-CdS sites where they are trapped. As discussed in the last paragraph, there are few holes trapped at the nc-CdS/ZrHfO interface probably because of the good passivation effect of S or/and O. Figure 36 shows (a) *C-V* hysteresis windows and (b) charge trapping densities of the nc-CdS embedded capacitor and other nanocrystals embedded capacitors prepared under the same condition. These devices were made of the ZrHfO high-*k* stacks embedded with nc-ZnO,[106] nc-ITO,[107,108] nc-RuO,[109,110] nc-MnO,[111] and nc-CdSe,[112] which were deposited by RF magnetron sputtering following with the similar PDA step. All the memory windows and charge trapping densities were measured with the symmetrical *C-V* sweep loop. The comparison was based on the maximum magnitude of the sweep voltage, i.e., *C-V* sweep voltage. The nc-CdS embedded capacitors have larger hysteresis windows and higher charge trapping densities than other capacitor at the low *C-V* sweep voltage. This demonstrates the excellent low-voltage-operating memory characteristics of the nc-CdS embedded ZrHfO stack.

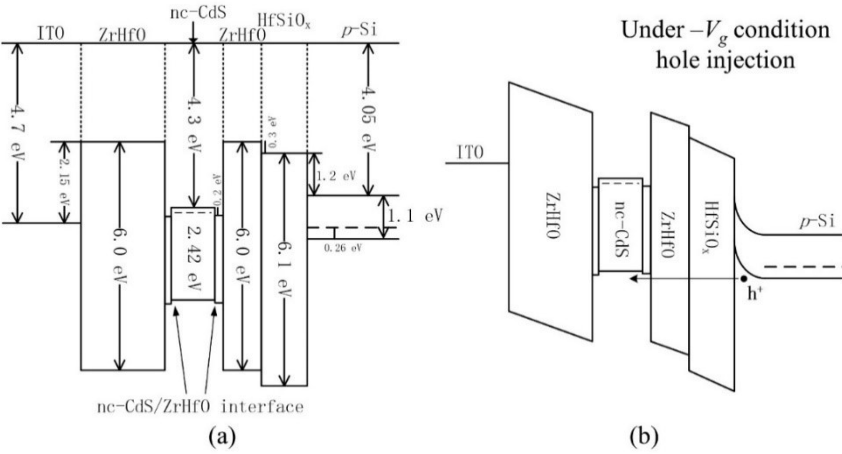

Figure 35. Energy band diagrams of the nc-CdS embedded sample under the (a) unbiased and (b) negative V_g stress conditions.

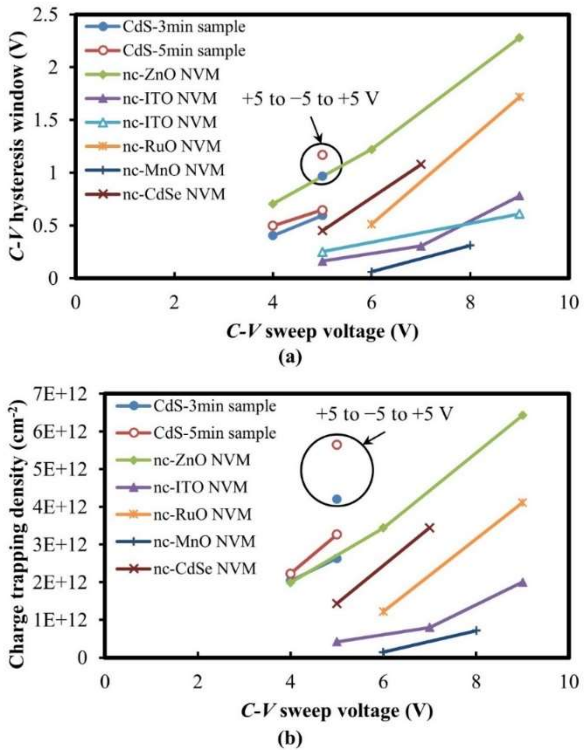

Figure 36. Comparisons of (a) memory windows and (b) charge trapping density of the nc-CdS embedded samples and various nanocrystal embedded NVMs, i.e., ZnO,[106] nc-ITO,[107,108] nc-RuO,[109,110] nc-MnO,[111] and nc-CdSe,[112] embedded NVMs.

The hole-trapping and -detrapping phenomena can be delineated from the change of the shape of the *J-V* curve.[109-113] Figure 37 shows *J-V* curves of the control, CdS-3min, and CdS-5min samples with V_g swept from −4 to + 4 V. The polarity of the current is defined as negative when it flows toward the gate and positive when it flows toward the substrate. At $V_g = -4$ V, a large number of holes are accumulated in the *p*-type Si and injected into the high-*k* stack.[109,112,113] With the decrease of the magnitude of V_g ($|V_g|$), fewer holes are injected into the high-*k* stack. At the same time, some of loosely trapped holes cannot be retained in the high-*k* stack and gradually release back to the Si substrate.[112,113] When more holes are detrapped from than injected into the high-*k* stack, the leakage current changes the polarity. The polarity change occurs at −3.1 V for the control sample, −2.15 V for the CdS-3min sample, and −1.55 V for the CdS-5min sample, respectively. This is consistent with the previous result that Q_{ot} increased with the increase of the amount of CdS embedded in the ZrHfO film. As the V_g is close to 0 V, a jump of *J* is observed. For the control sample, a small jump occurs at point A, which is due to the quick release of the remaining trapped holes.[109,112,113] For the nc-CdS embedded samples, two peaks are observed in the *J-V* curve. The peak at point B is contributed by the sudden detrap of the loosely trapped holes and that at point C is due to the release of the remaining trapped holes upon the polarity change of the applied V_g.[109]

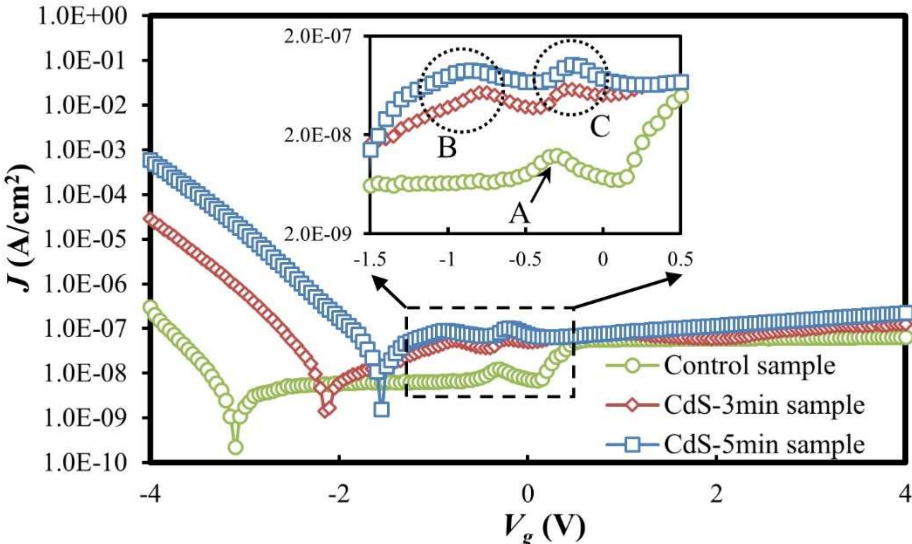

Figure 37. J-V curves of the control and nc-CdS embedded samples. V_g swept from −4 to +4 V. The inset is the magnified J-V curves in the range of V_g = −1.5 to +0.5 V.

The mechanism of charge transfer through the nc-CdS embedded ZrHfO dielectric structure is dependent on the electric field. According to literature reports,[111,113] charges are transferred through the ZrHfO high-k stack following the SE mechanism at the low electrical field and then the P-F mechanism at the high electrical field. Figure 8 shows the fitting of the J-V curves of the control and nc-CdS embedded samples to the following SE and P-F equations,

$$\text{(SE)} \quad J = A^* \times T^2 \exp[\frac{-q(\Phi_B - \sqrt{qV/4\pi\varepsilon d})}{kT}], \qquad [14a]$$

$$\text{(P-F)} \quad J \sim V \times \exp[\frac{-q(\Phi_B - \sqrt{qV/\pi\varepsilon d})}{kT}], \qquad [14b]$$

where V is the applied voltage, d is the dielectric thickness, T is the temperature, ε is the insulator dynamic permittivity, Φ_B is the barrier height, m^* is the carrier effective mass, k is the Boltzmann constant, and A^* is the effective Richardson constant.[126] A^* is a function of the effective mass ratio to the free carrier effective mass (m_0), i.e., $A^* = 4\pi q(m^*)k^2/h^3 = 120(m^*/m_0)$ ($A/cm^2 \cdot K^2$).[126]

For all samples, the SE relationship holds well at the low voltage and the P-F relationship holds well at the high voltage. All SE curves in Fig. 38(a) almost have the same y-axis interception. Therefore, the embedding of the nc-CdS layer in the ZrHfO high-k does not affect the ITO/ZrHfO interface.[127] On the other hand, P-F curves in Fig. 38(b) have different y-axis interceptions, i.e., −52.313, −48.398, and −46.465 for the control, CdS-5min, and CdS-3min samples, separately. The embedding of the CdS layer decreases the magnitude of the y-axis interception of the P-F curve, which indicates the decrease of P-F barrier height for the charge transfer.[112,113] This can be explained by the different locations of the P-F traps, i.e., at the $HfSiO_x$ interface layer of the control sample and at the CdS nanocrystal sites of the embedded samples.

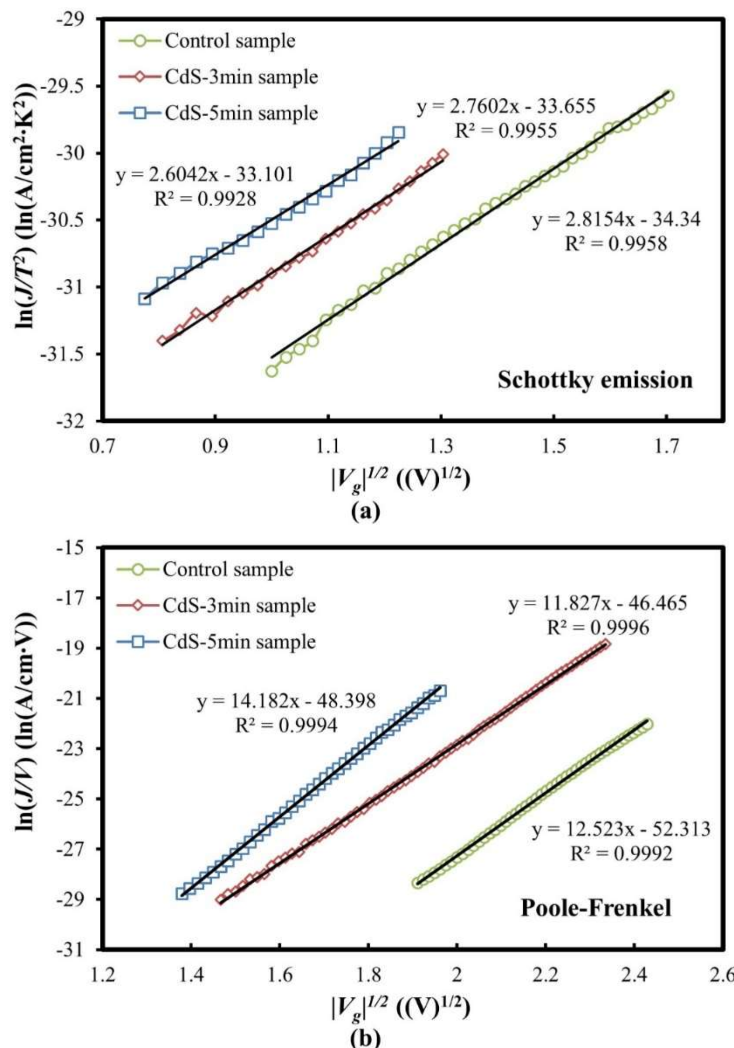

Figure 38. (a) Schottky emission and (b) Poole-Frenkel fittng of *J-V* curves of the nc-CdS embedded samples.

Dielectric breakdowns of the CdS embedded samples were investigated using the ramp-relax method described in refs. 95 and 96. Figure 39 shows the J_{ramp}-V_{ramp} and J_{relax}-V_{ramp} curves of the control and nc-CdS embedded samples. The "+" sign of J_{relax} means the current flowing toward the substrate; the "–" sign of J_{relax} means the current flowing

toward the gate. For all samples, at the beginning, the J_{ramp} increases slowly and smoothly with the increase of the magnitude of V_{ramp} ($|V_{ramp}|$) following the SE relationship. After V_{ramp} reaches −2 V, the J_{ramp} increases quickly following the P-F relationship. In this stage, charges are stacked up gradually in the high-*k* stack to form spot-connected paths.[112] The embedding of nc-CdS can induce extra defects in the high-*k* stack, which is responsible for the faster increase of J_{ramp} in this region.[110,112] At the same time, the J_{relax} increases dramatically from the detrap of holes trapped in the CdS nanocrystals. Upon the further increase of $|V_{ramp}|$, the dielectric breakdown occurs, which shows as an abrupt jump of the J_{ramp}. The breakdown voltages (V_{BD}'s) are −6.4 V, −5.5 V, and −5.25 V for the control, CdS-3min, and CdS-5min samples, respectively. The lower breakdown voltage of the nc-CdS embedded sample is also due to the larger number of defects in the high-*k* stack. After the dielectric breakdown, conductive paths are formed in the high-k stack.[95] For the control sample, the polarity of the J_{relax} changes. However, for the nc-CdS embedded sample, the magnitude of the J_{relax} decreases but the polarity remains the same, which is due to the gradual release of the trapped holes from the nc-CdS sites.[95]

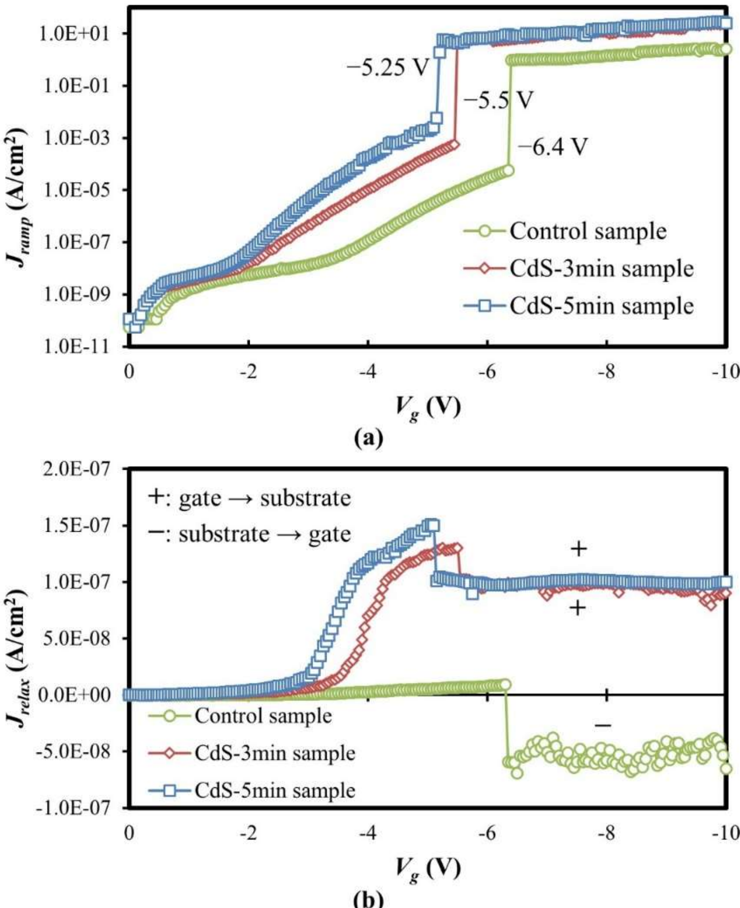

Figure 39. (a) J_{ramp} and (b) J_{relax} vs. V_{ramp} curves of the control and nc-CdS embedded samples.

The hole retention characteristics of the nc-CdS embedded samples were studied by measuring the percentage of charges remained in the device after the removal of the stress voltage, using the following equation,[116]

$$\text{charge remaining } (\%) = \frac{V_{FB}(t) - V_{FB,fresh}}{V_{FB}(t=0) - V_{FB,fresh}}, \qquad [15]$$

where $V_{FB,\ \mathrm{fresh}}$ is the V_{FB} of the fresh sample before the V_g stress, $V_{FB}(t=0)$ is the V_{FB} immediately after the stress, and $V_{FB}(t)$ is the V_{FB} after releasing the stress voltage for a period of time t. All V_{FB}'s were extracted from *C-V* curves measured from $V_g = -2$ to $+1$ V at 1 MHz. The *C-V* curve was recorded every 1,800s for a period of 10 hrs. Figure 40(a) shows hole retention curves of the nc-CdS embedded samples stressed at $V_g = -5$ V for 10 s. In the first 1,800 s, 18% (CdS-3min) and 17% (CdS-5min) of the originally trapped holes are quickly released from shallow trapping sites.[95,112] Since the CdS-5min sample has more deeply trapped holes than the CdS-3 min sample has, the former drops trapped holes slower than the latter does. After this stage, the deeply trapped holes are gradually released. From 1,800 s to 36,000 s, the CdS-3min sample releases 8% of the originally trapped holes but the CdS-5min sample releases 12% of the trapped holes. The faster detrapping rate of the CdS-5min sample may be related to the higher defect density in its $HfSiO_x$ interface layer, which can easily tunnel charges back to the Si substrate.[95,128] The inset of Fig. 40(a) shows the extrapolations of the retained charges to 10 years. About 53% and 48% of the originally stored holes can be retained in the CdS-3min and CdS-5min samples, respectively. Fig. 40(b) shows the comparison of hole retention capabilities of the nc-CdS embedded samples and other nanocrystal embedded high-*k* capacitors, such as, nc-ITO,[107] nc-RuO,[109] nc-MnO,[111] and nc-CdSe,[112] embedded NVMs. Although charges stored in the nc-CdS embedded samples were from the low voltage stress, their 10-year retention capacities are comparable or higher than those of the nc-ITO, nc-RuO, nc-MnO, and nc-CdSe embedded samples stressed at the voltages, e.g., −8 V for 10 s. This

was because the defects around nanocrystals could assist the release of the stored charges. However, CdS has fewer nanocrystal interface defects due to the O or S passivation.[122,123]

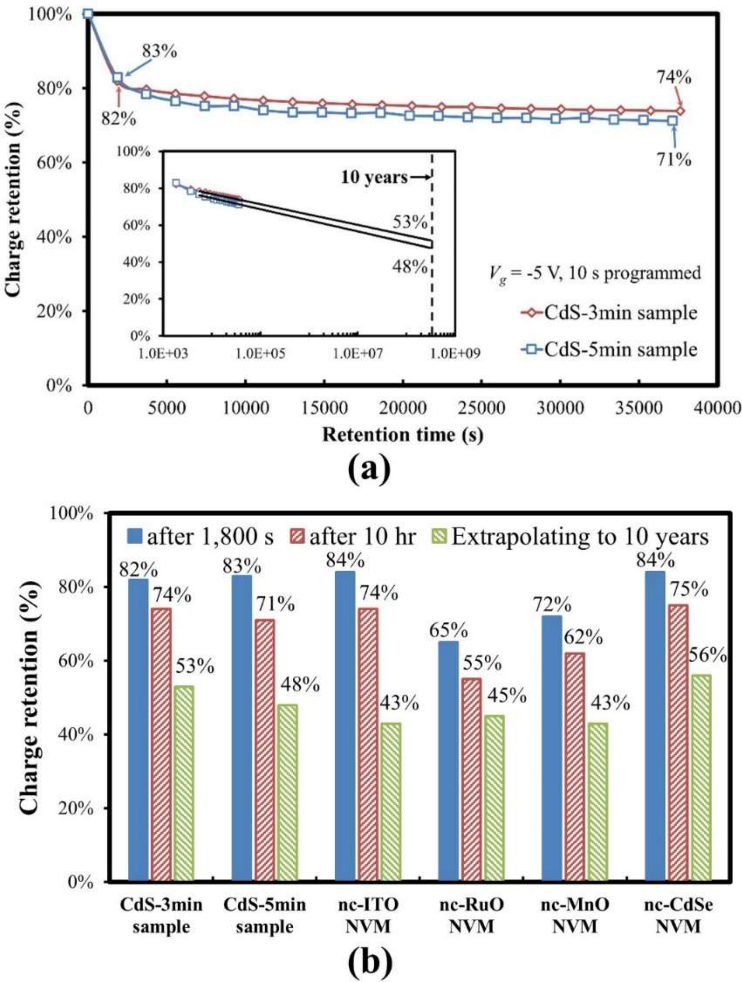

Figure 40. (a) Hole retention characteristics of the nc-CdS embedded samples. Inset: 10-year extrapolation. (b) Comparisons of hole retention capabilities of the nc-CdS embedded samples and various nanocrystal embedded NVMs, i.e., nc-ITO,[107] nc-RuO,[109] nc-MnO,[111] and nc-CdSe,[112] embedded NVMs.

3.4 Summary

In summary, the memory functions and charge trapping/detrapping mechanisms of the nc-CdS embedded ZrHfO high-*k* dielectric NVMs have been investigated. The embedded CdS layer could suppress the growth of $HfSiO_x$ interface layer by reducing the O diffusion to the ZrHfO/Si contact. This decreased the capacitor's total thickness but increased the interface states density. Because of the *n*-type properties of the embedded CdS, the capacitor preferred to trap holes other than electrons. The more CdS is embedded in the high-*k* stack, the more hole trapping sites were generated. No frequency dispersion phenomenon was observed in this device. There were fewer defects at the nc-CdS/ZrHfO interface due to the passivation of O or S. Thus, holes were mainly trapped in the nanocrystals. On the other hand, the embedding of CdS induced a larger leakage current due to the formation of excess defects in the high-*k* stack. The charge transfer through the nc-CdS embedded high-*k* stack followed SE relationship at the low voltage and P-F mechanism at the high voltage. The fitting showed that the embedding of CdS didn't affect the SE barrier at the ITO/ZrHfO interface but reduced the P-F traps in the high-*k* stack. After the dielectric breakdown of the high-*k* stack, the CdS nanocrystals still could retain holes. About 53% of the originally trapped holes could remain in the nc-CdS embedded capacitors for 10 years. Although operated at the low voltage, the device's memory windows and hole retention capabilities were comparable with and even better than those of other nanocrystal embedded NVMs operated at the high voltage. Therefore, the nc-CdS embedded ZrHfO high-*k* stack is a viable dielectric structure for the low power operating NVM application.

CHAPTER IV

TEMPERATURE EFFECTS ON NANOCRYSTALLINE CADMIUM SELENIDE EMBEDDED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K NONVOLATILE MEMORIES*

4.1 Introduction and Motivation

Currently, most studies on the nanocrystals embedded high-*k* NVMs have been focused on the room temperature performance. Very few publications discuss the temperature effect on this kind of device.[129] However, the temperature of a high-density IC chip during the operation can be much higher than the room temperature.[130] Therefore, it is necessary to understand the influence of temperature on the performance of this kind of device especially the charge trapping/detrapping and transfer mechanisms as well as the dielectric breakdown behavior. For example, the embedded nanocrystals can accelerate the degradation of the high-*k*/Si interface at the high temperature.[111] On the other hand, the nc-CdSe embedded ZrHfO gate dielectric NVM shows excellent charge trapping and retention capabilities for both electrons and holes.[112] Therefore, in this

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chapter, the author investigated the temperature effect on the performance of the nc-CdSe embedded ZrHfO high-*k* MOS capacitor.

4.2 Experimental

MOS capacitors with the ZrHfO (tunnel oxide)/nc-CdSe/ZrHfO (control oxide) gate dielectric stack were fabricated on the *p*-type (10^{15} cm^{-3}) Si <100> wafer pre-cleaned with a DHF solution. The dielectric stack was sputter-deposited in one-pumpdown without breaking the vacuum. The tunnel and control oxide layers were deposited from the Zr/Hf composite target in Ar/O_2 (1:1) at 5 mTorr and 60 W for 2 min and 10 min, separately. The embedded CdSe layer was deposited from a CdSe target in pure Ar at 5 mTorr and 60 W for 3 min. A control sample containing a 12 min deposited ZrHfO gate dielectric film without the embedded CdSe layer was fabricated under the same sputtering condition. After the gate dielectric deposition, the sample was treated with a PDA step, i.e., at 800 ^{o}C in pure N_2 for 3 min. According to a previous study,[112] under the same PDA condition, the as-deposited amorphous CdSe film was transferred into discrete nc-CdSe dots while the surrounding ZrHfO film remained amorphous. In the ZrHfO high-*k* MOS capacitors, a $HfSiO_x$ interface layer was always formed between the bulk ZrHfO and the Si substrate after the PDA step.[109,112,116] It was reported that the thicknesses of the bulk ZrHfO and $HfSiO_x$ interface layers were 3.8 nm vs. 3.3 nm for the control sample, and 6.2 nm vs. 4.7 nm for the nc-CdSe embedded sample.[112] An 80 nm thick ITO film was deposited on top of the high-*k* stack and subsequently wet etched into 100 µm diameter gate electrodes through lithography defined patterns. An Al film was deposited on the backside of the Si

substrate to form the ohmic contact. Finally, the sample was treated with a PMA step at 400 ºC in H_2/N_2 (1:9) for 5 min.

4.3 Temperature Effects on Charge Trapping and Transfer Mechanisms

Figure 41 shows *C-V* curves of the control and nc-CdSe embedded samples measured at 1 MHz at various temperatures with the V_g swept from −6 V to +6 V (forward) and then back to −6 V (backward). The inset of the figure shows *C-V* curves of the control sample measured under the same conditions. The very small hysteresis curves of the control sample at each temperature indicates the negligible amount of charges trapped in the bulk ZrHfO file or at the ZrHfO/Si interface.[116] However, the nc-CdSe embedded sample shows obvious *C-V* hysteresis phenomenon. The V_{FB} difference (ΔV_{FB}) between the forward and backward curves can be taken as the memory window. For the nc-CdSe embedded sample, the ΔV_{FB}'s are 0.72 V at 20 ºC, 0.70 V at 70 ºC, and 0.64 V at 120 ºC, which correspond to charge trapping densities (Q_{ot}'s) of 1.79×10^{12} cm^{-2}, 1.75×10^{12} cm^{-2}, and 1.63×10^{12} cm^{-2} estimated from the Equation 13. As the temperature is increased, *C-V* curves in the forward and backward sweep directions shift toward the negative V_g direction. The shift in the backward sweep direction is larger than that in the forward sweep direction, which results in the reduction of both ΔV_{FB} and Q_{ot}. This phenomenon can be explained by the competitive trapping and retention of holes and electrons in the high-*k* stack,[131] which will be discussed in detail later.

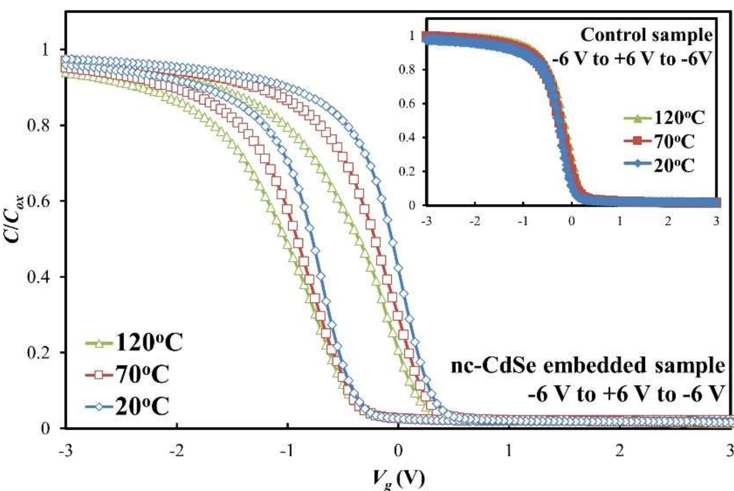

Figure 41. *C-V* hysteresis curves of nc-CdSe embedded sample at 1 MHz at 20 ºC, 70 ºC, and 120 ºC, respectively. V_g swept from −6 V to +6 V to −6 V. Inset: control sample.

Separately, the inset of Fig. 41 shows that the slope of the control sample's *C-V* curve changes slightly with temperature. For example, the D_{it}'s are 6.77 $\times 10^{10}$ $cm^{-2}\cdot eV^{-1}$ at 20 ºC, 7.38 $\times 10^{10}$ $cm^{-2}\cdot eV^{-1}$ at 70 ºC, and 1.09 $\times 10^{11}$ $cm^{-2}\cdot eV^{-1}$ at 120 ºC. However, the slope of the *C-V* curve of the nc-CdSe embedded sample decreases obviously with the increase of temperature, i.e., the D_{it} changes from 3.15×10^{11} $cm^{-2}\cdot eV^{-1}$ at 20 ºC to 3.93×10^{11} $cm^{-2}\cdot eV^{-1}$ at 70 ºC and 6.91×10^{11} $cm^{-2}\cdot eV^{-1}$ at 120 ºC. Because of the stress mismatch, the embedding of nanocrystals can induce defects in the high-*k* stack.[111] This effect becomes more obvious with the increase of temperature. Injections of charges from the Si wafer and the gate electrode also increase with the temperature, which accelerate the deterioration of the ZrHfO/Si interface.[111,132]

To further investigate the temperature effect on the hole or electron trapping in the nc-CdSe embedded ZrHfO sample, *C-V* curves were measured in two opposite V_g

directions, i.e., one from −6 V to +6 V and the other one from +6 V to −6 V. Figure 42 shows the result which is drawn in a small V_g range of −2 V to +1 V to better exhibit the difference. The "fresh" sample's *C-V* curves, which were measured from $V_g = -2$ V to +1 V, are included for comparison. Compared with the "fresh" sample, the *C-V* curve of the sample swept from −6 V to +6 V shifts toward the negative V_g direction due to the trap of holes.[131] When the sample is swept from the opposite direction, i.e., from +6 V to −6 V, the *C-V* curve shifts toward the positive V_g direction due to the trap of electrons.[131] The amount of charges trapped in the V_g sweep can be quantified by comparing the V_{FB} of the nc-CdSe embedded sample with that of the "fresh" sample. For example, under the −6 V to +6 V sweep condition, the magnitude of the negative V_{FB} shift increases with the increase of temperature, i.e., from 0.49 V at 20 ºC to 0.63 V at 70 ºC and 0.76 V at 120 ºC. At the high temperature, more holes can be accumulated and injected from the Si substrate to the high-*k* stack.[131,133] On the other hand, under the +6 V to −6 V sweep condition, the magnitude of the positive V_{FB} shift decreases from 0.49 V at 20 ºC to 0.43 V at 70 ºC and 0.31 V at 120 ºC, which corresponds to the decrease of electrons trapping. This result on be explained from the difference of the band gap energy diagram. The conduction band offset between ZrHfO and Si is much smaller than the valence band offset.[112] At the high temperature, electrons can obtain more energy to transfer through the high-*k* stack without being retained by the nc-CdSe related trapping sites.[131] Moreover, the electron concentration in the *n*-type CdSe is increased with the increase of temperature, which can inhibit the trap of electrons.[134,135] The above principle can be used to explain the result of Fig. 41, i.e., the decrease of ΔV_{FB} with the increase of temperature. At the

high temperature, the increase of the hole-trapping is more pronounced than the decrease of the electron-trapping.

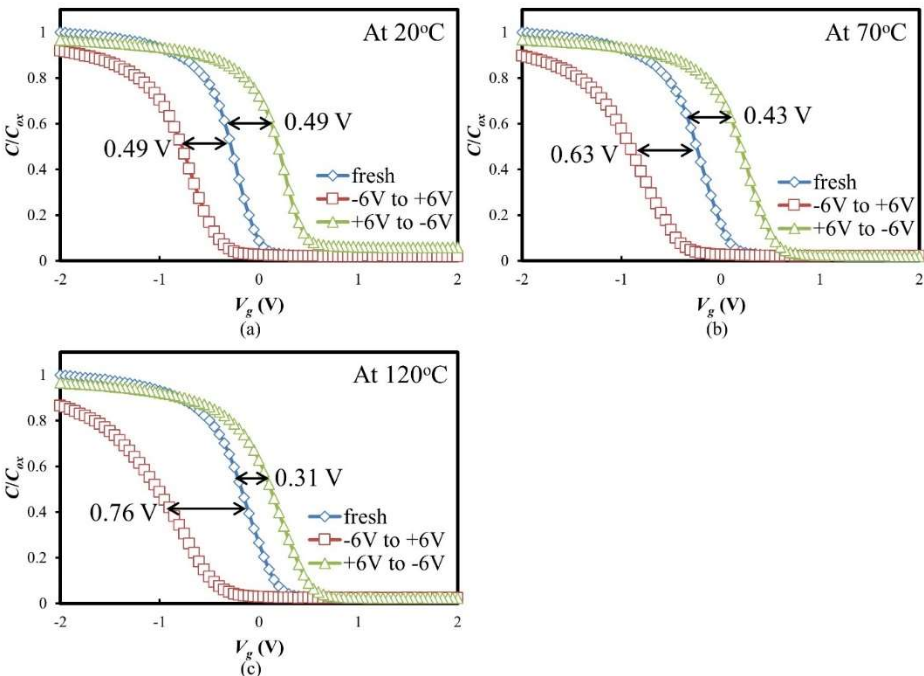

Figure 42. *C-V* curves of the nc-CdSe embedded sample measured from $V_g = -6$ V to +6 V and from +6 V to −6 V at 1MHz at (a) 20 ºC, (b) 70 ºC, and (c) 120 ºC, respectively. Fresh: fresh sample measured from $V_g = -2$ V to +1 V.

In the nc-CdSe embedded sample, charges may be stored in the bulk nc-CdSe or at the nc-CdSe/ZrHfO interface, which can be differentiated with the frequency dispersion method.[112] *C-V* curves with V_g swept from $V_g = -6$ V to +6 V were measured at various frequencies, i.e., 100 kHz, 500 kHz, and 1 MHz, and temperatures, i.e., 20 ºC, 70 ºC, and 120 ºC. Figure 43(a) shows that for the control sample, the *C-V* curve does not change its

shape or location with the change of the measurement frequency at 20 ºC. The same result was observed at 70 ºC and 120 ºC, which are not shown here. Therefore, the few holes trapped in the bulk ZrHfO or at the ZrHfO/Si interface do not respond to changes of the measurement frequency or temperature. However, for the nc-CdSe embedded sample, the *C-V* curve shifts toward the positive V_g direction with the decrease of the measurement frequency. This phenomenon can be explained by the response of the shallow-trapped holes at the nc-CdSe/ZrHfO interface to the low measurement frequency.[109,112] In the depletion region, the loosely trapped holes can tunnel back to the Si substrate to cause the positive shift of the *C-V* curve.[112] The *C-V* curve shifts further with the increase of temperature because the amount of the shallow-trapped holes increases with the increase of temperature.[111] Fig. 43(d) shows an obvious hump near the V_{FB} in the 100 kHz, 120 ºC curve. It can be attributed by a group of near interface traps (NITs), which have different life times and capture cross-sections, existing at the nc-CdSe/ZrHfO interface.[133,136] They do not respond to the measurement frequency at the low temperature. However, at 120 ºC, they are activated and become responsive to the measure frequency. Also, the mobility of the charge carrier in the inversion layer is strongly influenced by the temperature.[136,137] On the other hand, no frequency dispersion was observed under the electron-trapping condition in both the control and nc-CdSe embedded samples at all temperatures, as shown in Figure 44. For the control sample, the amount of electrons trapped in bulk ZrHfO or at the ZrHfO/Si interface are negligibly small to cause the *C-V* curve shift or shape change at the low frequency.[111] For the nc-CdSe embedded ZrHfO sample, electrons are mainly

trapped in the bulk nc-CdSe, which are little responsive to the frequency variation.[109,112] Therefore, no C-V curve shift or hump was observed.

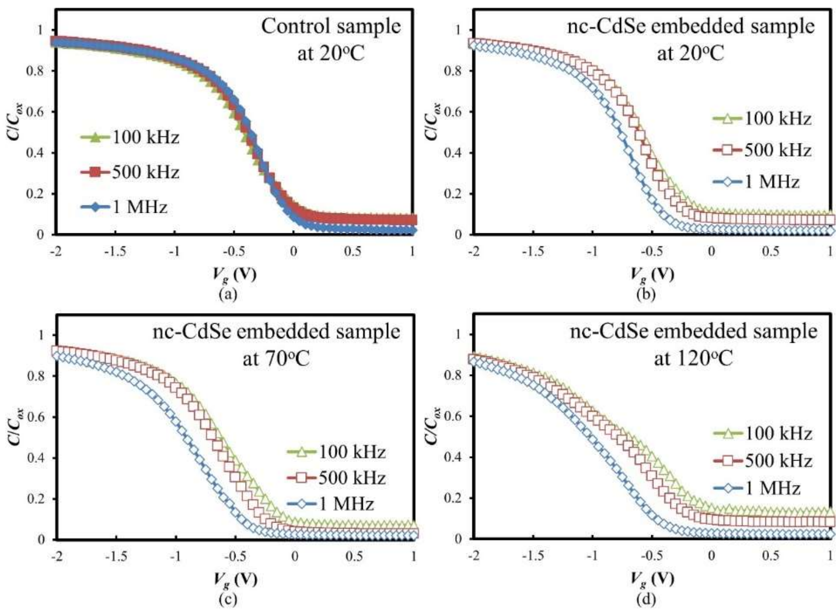

Figure 43. C-V curves of (a) control and (b)(c)(d) nc-CdSe embedded samples at 20 ºC, 70 ºC, and 120 ºC, measured from $V_g = -6$ V to +6 V at 100 kHz, 500 kHz, and 1 MHz.

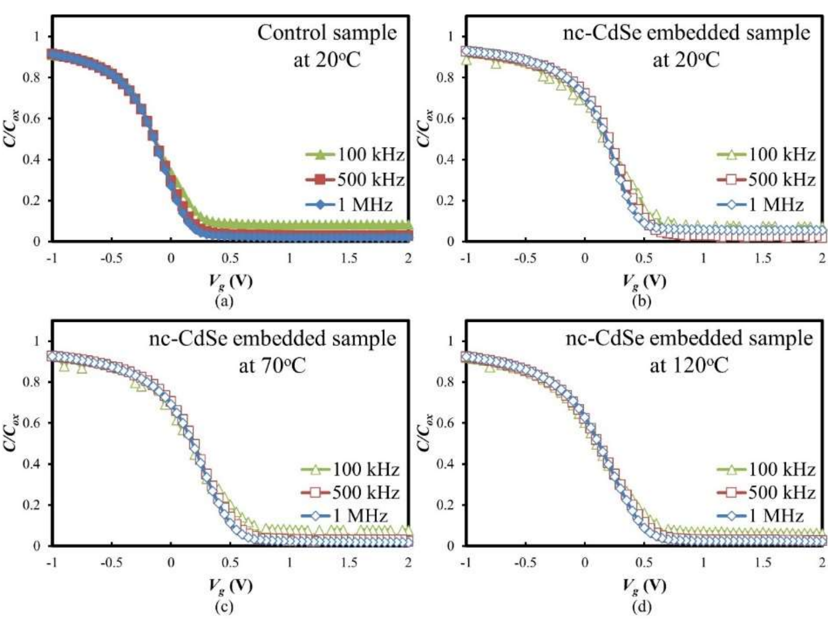

Figure 44. *C*-*V* curves of (a) control and (b)(c)(d) nc-CdSe embedded samples at 20 ºC, 70 ºC, and 120 ºC, measured from V_g = +6 V to −6 V at 100 kHz, 500 kHz, and 1 MHz.

Figure 45 shows *J*-*V* curves of the (a) control and (b) nc-CdSe embedded samples with V_g swept from −6 V to +6 V at different temperatures. Starting from V_g = −6 V, holes are accumulated near the ZrHfO/Si interface and then injected through the high-*k* stack toward the gate electrode direction. As the V_g is moved to the 0 V direction, the supply of holes is reduced, which reduces the leakage current. Gradually, the loosely trapped holes in the gate dielectric stack tunnel back to the Si substrate.[116] When the amount of detrapped holes is larger than that of injected holes, the polarity of the *J* changes. The polarity change occurs earlier in the control sample than in the nc-CdSe embedded sample, e.g., −4.45 V vs. −2.55 V at 20 ºC, which is due to the poor hole-retention of the former.[119] For both samples, the magnitude of the V_g where the *J* changes its polarity decreases with the

increase of temperature because of the increase of the supply of holes in the *p*-type Si.[111] As V_g is near 0 V, i.e., at point A, the J suddenly jumps. This is due to the quick release of the remaining trapped holes upon the transition of the energy band gap structure to the flat band state.[109,112] At the high temperature, more holes can gain enough thermal energy to be detrapped from the high-k stack and, therefore, the jump of J is small.[111,131] For the nc-CdSe embedded sample, a second jump of J, i.e., at point B, is observed at 20 ºC. This is a negative differential resistance (NDR) peak caused by the Coulomb blockade effect, which is often observed in nanocrystals embedded high-k devices.[107,109,111,112,133] The NDR peak vanishes at the high temperature, i.e., 70 ºC and 120 ºC, because the trapped charges have energy large enough to overcome the Coulomb blockade effect.[138,139] Separately, the J increases with the increase of temperature in both negative and positive V_g ranges. When the temperature is increased, more high-energy holes and electrons are provided by the Si substrate.[111] Also, the conductivity of the high-k film increases with the rise of temperature.[111] Therefore, more charges are transferred through the high-k stack at the high temperature.[109,129]

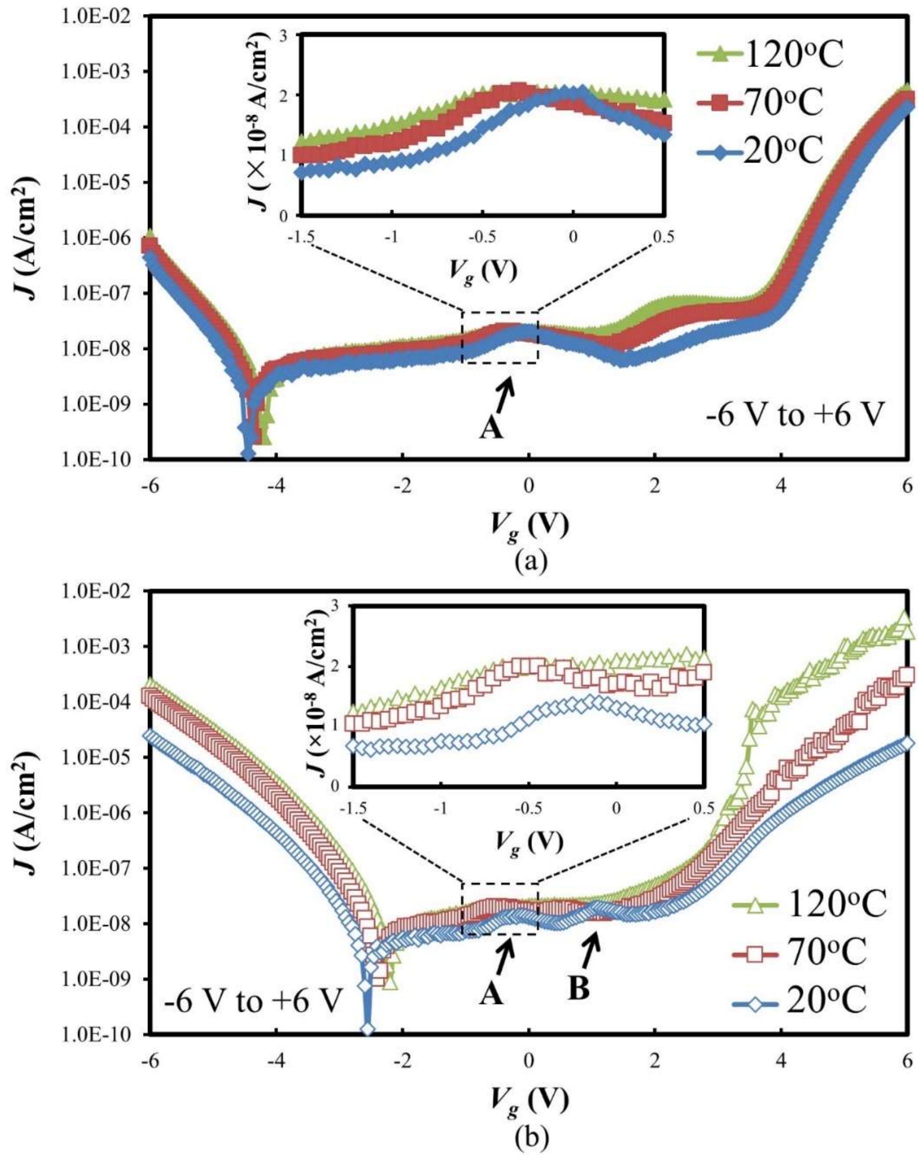

Figure 45. J-V curves of (a) control and (b) nc-CdSe embedded samples. V_g swept from −6 V to +6 V at 20 ºC, 70 ºC, and 120 ºC, respectively. Inset: magnified curves in V_g = −1.5 V to +0.5 V.

Charges transferred through the nc-CdSe embedded sample at different temperatures can be through various mechanisms. For example, the *J-V* curves can be fitted with the following SE, P-F, or F-N tunneling equations:

$$\text{(SE)} \quad J = A^* \times T^2 \exp[\frac{-q(\Phi_B - \sqrt{qE/4\pi\varepsilon})}{kT}], \qquad [16a]$$

$$\text{(P-F)} \quad J \sim E \times \exp[\frac{-q(\Phi_B - \sqrt{qE/\pi\varepsilon})}{kT}], \qquad [16b]$$

$$\text{(F-N)} \quad J \sim E^2 \exp[-\frac{8\pi\sqrt{2m^*}(q\Phi_B)^{3/2}}{3qhE}], \qquad [16c]$$

where E is the electric field.[126]

Previously, it was reported that charges were transferred through the ZrHfO high-*k* film following SE mechanism at the low electric field and P-F mechanism at the high electric field in the negative V_g region.[127] Generally, these relationships are still applicable to the nc-CdSe embedded sample at different temperatures. Figure 46 shows the SE ($\ln(J/T^2)$ vs. $E^{1/2}$) and P-F plots ($\ln(J/E)$ vs. $E^{1/2}$) of the nc-CdSe embedded sample at 20 ºC, 70 ºC, and 120 ºC. In Fig. 46(a), the J follows the SE equation in the low electric field range, i.e., 1700 to 2100 $(V/cm)^{1/2}$. Assuming $m^*/m_0 = 0.4$ for the hole,[140] SE barrier heights extracted from the y-axis intercepts are 1.31 eV at 20 ºC, 1.50 eV at 70 ºC, and 1.64 eV at 120 ºC. The SE barrier height increases with the increase of temperature, which is similar to the case of the HfO_2 film.[140,141] Since the SE process is temperature-activated, more holes can obtain sufficient energy to overcome the higher barrier when the temperature is increased.[140,141] On the other hand, the P-F mechanism occurs in the high electric field region, i.e., 2200 to 2700 $(V/cm)^{1/2}$. From the linear fitting of the P-F curve

intercept vs. $1/T$, the barrier height of the conduction traps is estimated to be 0.34 eV. It is smaller than that of P-F conduction traps of the ZrHfO thin film without any embedding layer, i.e., 0.46 eV.[127] Thus, these shallow traps are probably located at the nc-CdSe/ZrHfO interface.

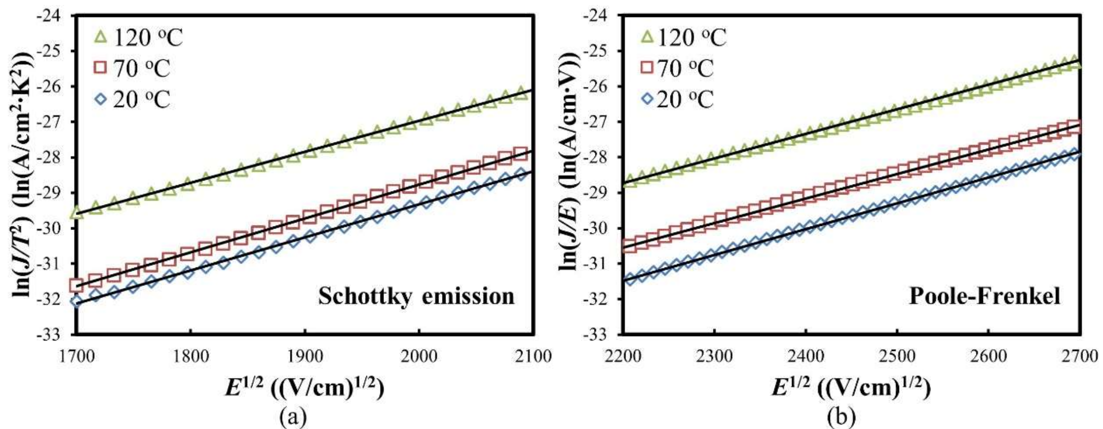

Figure 46. Fitting of (a) Schottky emission and (b) Poole-Frenkel mechanisms in negative V_g region at 20 ºC, 70 ºC, and 120 ºC, respectively.

In the positive V_g range, the SE relationship still holds in the low electric field regime, as shown in Figure 47. Assuming $m^*/m_0 = 0.18$ for the electron,[140] the SE barrier height increases from 1.17 eV at 20ºC to 1.30 eV at 70 ºC and 1.38 eV at 120 ºC. This also can be explained by the enhanced emission of electrons near the Si conduction band at the raised temperature, as discussed in the last paragraph. However, the acceptable SE fitting range shifts toward the lower electric field with the increase of temperature, i.e., 1800 to 2200 $(V/cm)^{1/2}$ at 20 ºC, 1450 to 1950 $(V/cm)^{1/2}$ at 70 ºC, and 1200 to 1700

$(V/cm)^{1/2}$ at 120 ºC. The similar shift of the SE fitting range was observed in the Cu/HfO_2/Pt capacitor.[141] Beyond these regions, the electron transfer changes from the P-F mechanism at 20 ºC to the F-N tunneling at 120 ºC. Figure 48 shows the (a) P-F and (b) F-N fittings in the region of 2200 to 2600 $(V/cm)^{1/2}$ at 20 ºC and 1700 to 2100 $(V/cm)^{1/2}$ at 120 ºC, respectively. A barrier height of 1.39 eV is obtained from Fig. 48(b) using Equation 16c, which is very close to the SE barrier height of 1.38 eV at 120 ºC. The good fitting of both mechanisms indicates that a transition of electron transfer from the P-F mechanism to the F-N tunneling occurs at the high temperature. The P-F mechanism can be taken as a process that traps near the band edge restrict the current flow by a capture-emission process.[142] The electron trapping capability of the nc-CdSe embedded sample decreases dramatically at the high temperature. With the increase of temperature, there are fewer traps to capture electrons. At the high temperature and high electric field condition, electrons may transfer through the high-*k* stack without experience the capture-and-emission process. Then, the electron transfer is similar to the F-N tunneling mechanism.

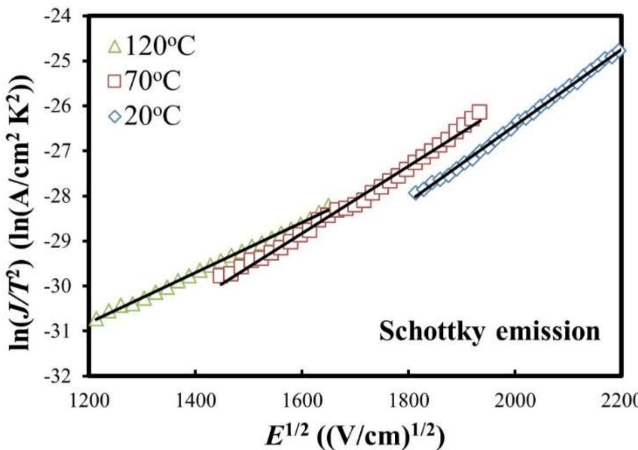

Figure 47. Fitting of Schottky emission in positive V_g region at 20 ºC, 70 ºC, and 120 ºC, respectively.

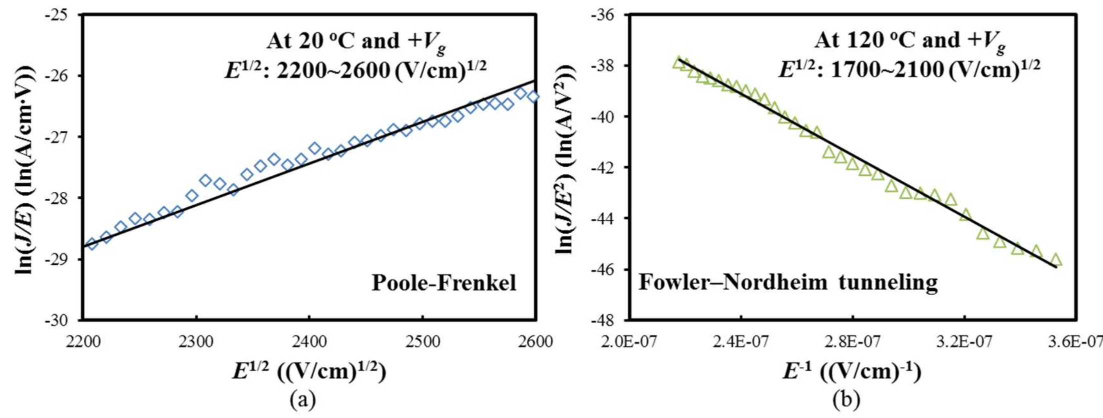

Figure 48. Fitting of (a) Poole-Frenkel mechanism at 20 ºC and (b) Fowler-Nordheim tunneling at 120 ºC in negative V_g region.

4.4 Temperature Effects on Dielectric Breakdown and Charge Retention Capabilities

Figure 49 shows ramp-relax curves of the control and nc-CdSe embedded samples at 20 ºC, 70 ºC, and 120 ºC, respectively. The "+" sign of the relaxation current density J_{relax} means the direction of the leakage current flowing toward the Si substrate and the "–" sign means the opposite current flow direction. In the low voltage range, J_{ramp} increases slowly and smoothly with the increase of the magnitude of V_{ramp} following the SE mechanism.[112] At the same time, the relaxation current flows toward the substrate direction due to the release of the trapped charges upon the removal of the stress voltage.[96] When the stress voltage is increased, charges are stacked up gradually in the high-k stack to form spot-connected paths. At this stage, J_{ramp} increases with the increase of the magnitude of voltage following the P-F mechanism.[112] Upon the further increase of V_{ramp}, the dielectric breakdown phenomenon is observed, as shown in Fig. 49(a) and (b). For the control sample, a large jump of J_{ramp} is observed, which is typically referred to as the hard breakdown (HBD).[143] At the same time, J_{relax} drops abruptly accompanied with the change of polarity, which is due to the loss of the integrity of the high-k film.[143,144] The bulk ZrHfO and interface layers break down simultaneously, which is shown as the one-step breakdown in Figure 50(a).[143,144] However, for the nc-CdSe embedded sample, it breaks down in two steps. At the first breakdown step, J_{ramp} fluctuates with the increase of voltage, which is the soft breakdown (SBD) phenomenon.[143,145,146] Eventually, the HBD is observed where the high-k stack is broken permanently and J_{ramp} jumps abruptly.[143] At the first breakdown, with the further increase of the voltage, J_{relax} remains the same

without changing the polarity. In this period, the $HfSiO_x$ interface layer is broken while the bulk ZrHfO film maintains its integrity.[143,144] During the second breakdown, the bulk ZrHfO film is broken at a high V_g as shown in Fig. 50(b). However, the embedded CdSe nanocrystals still retain a large portion of the trapped holes. They are slowly released, which shows as a small positive J_{relax}.[112] It was reported that the breakdown of the ZrHfO high-k stack was related to the defect generation and propagation.[143,144] Without the embedded nanocrystals, the control sample has a much lower defect density than the nc-CdSe embedded sample has, which leads to a much smaller leakage current.[112] When the interface layer of the control sample is broken, the voltage drop through the bulk ZrHfO layer is large enough to simultaneously cause its breakdown. On the other hand, the two-step breakdown phenomenon of the nc-CdSe embedded sample is contributed by its unique film structure. First, its interface layer is thicker and more SiO_x-like than that of the control sample.[112] Under same V_{ramp} bias condition, this interface layer is subject to a larger voltage stress, which accelerates the defect generation and causes the early breakdown.[144] Second, the inclusion of the nc-CdSe layer increases the thickness of the bulk ZrHfO film.[112] When the interface layer is broken, the voltage drop across the bulk ZrHfO layer is not large enough to cause its immediate breakage.[143] The applied voltage needs to be increased further until the breakdown of the bulk ZrHfO layer occurs.

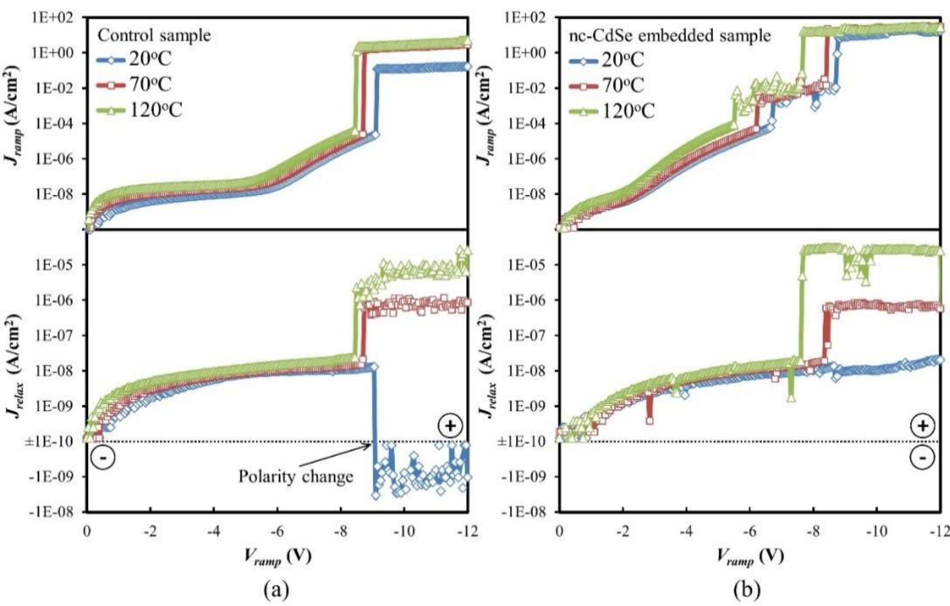

Figure 49. J_{ramp}-V_{ramp} and J_{relax}-V_{ramp} curves of the (a) control and (b) nc-CdSe embedded samples at 20 ºC, 70 ºC, and 120 ºC, respectively. V_g swept from 0 to −12 V. Polarity of J_{relax} is positive above the dash line and negative below the dash line.

When the temperature is increased, the breakdown strength of both samples decreases. Fig. 49(a) shows that, for the control sample, the magnitude of V_{BD} ($|V_{BD}|$) decreases from −9.15 V at 20 ºC, to −8.75 V at 70 ºC to −8.50 V at 120 ºC. Fig. 49(b) shows that, for the nc-CdSe embedded sample, the V_{BD}'s of the first- and second-step breakdowns are −6.70 V vs. −8.75 V at 20 ºC, −6.25 V vs. −8.45 V at 70 ºC, and −5.75 V vs. −7.70 V at 120 ºC, respectively. The free carrier concentration in the Si substrate increases with the increase of temperature.[147] Under the $-V_g$ condition, the raise of temperature increases the concentration of holes accumulated at the high-k/Si interface. These holes are subsequently injected into the high-k stack, which accelerates the degradation of bulk and interface layers.[131] In the last paragraph, it was discussed that at

20 ºC, after the HBD, the J_{relax} of the control sample changed the polarity but that of the nc-CdSe embedded sample did not change the polarity because nanocrystals in the latter retained a large portion of the trapped charges. However, at 70 ºC and 120 ºC, the polarity change of J_{relax} in the control sample disappeared. After the HBD, the polarity of J_{relax} remains the same and at the same time, its magnitude increases. After the breakdown of the whole high-*k* stack, permanent conductive paths are formed between the gate electrode and the Si substrate.[79] Since, at zero bias voltage, the concentration of free electrons remaining near the Si interface at the high temperature is higher than that at the low temperature, they are easily conducted through the conductive paths toward the gate direction. Therefore, the polarity of J_{relax} remains the same after the HBD and the magnitude increases.

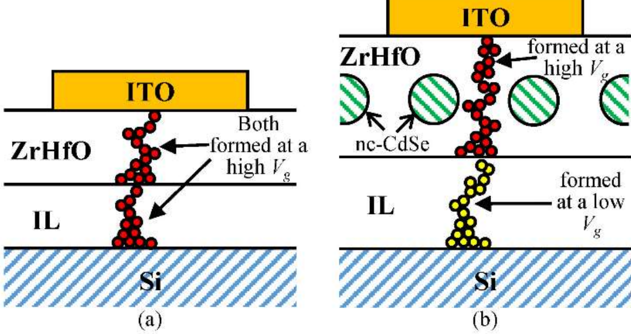

Figure 50. Cross-sectional views of structures of the (a) control and (b) nc-CdSe embedded samples with breakdown paths. IL: the $HfSiO_x$ interface layer.

Figure 51(a) shows *J-V* curves of the nc-CdSe embedded sample at 20 ºC, 70 ºC, and 120 ºC, respectively. At each temperature, the sample was firstly swept with the V_g from 0 V to a specific voltage that was high enough to cause the first-step breakdown, i.e., the damage of the $HfSiO_x$ interface layer, but not high enough for the second-step breakdown. Then, the second sweep was carried out from $V_g = 0$ V to −15 V. The leakage current *J* in the second curve is larger than that in the first sweep curve until the V_g reaches the point where the first breakdown occurs. Above the first breakdown point, holes are quickly transferred through the high-*k* stack via multiple traps.[145,148] When the temperature is increased, more holes can be supplied by the Si substrate to transfer through the high-*k* film,[147,149] which causes the larger leakage current. Fig. 51(b) shows that after the first breakdown, the *J-V* curve can be fitted with the power law of:

$$J = a \cdot V^{b}, \qquad [17]$$

where *a* is the area pre-factor constant which is related to the current density at $V_g = -1$ V and *b* is the normalized differential conductance.[150] The *a* value increases from 9×10^{-9} at 20 ºC to 1×10^{-7} at 70 ºC to 8×10^{-7} at 120 ºC, which is contributed by the increase of the supply of holes to pass through the high-*k* stack.[79] At the same time, the *b* value decreases with the increase of temperature, i.e., 9.39 at 20 ºC, 7.93 at 70 ºC, and 7.25 at 120 ºC. This result is consistent with the literature report on the statistical correlation between parameters *a* and *b*.[150]

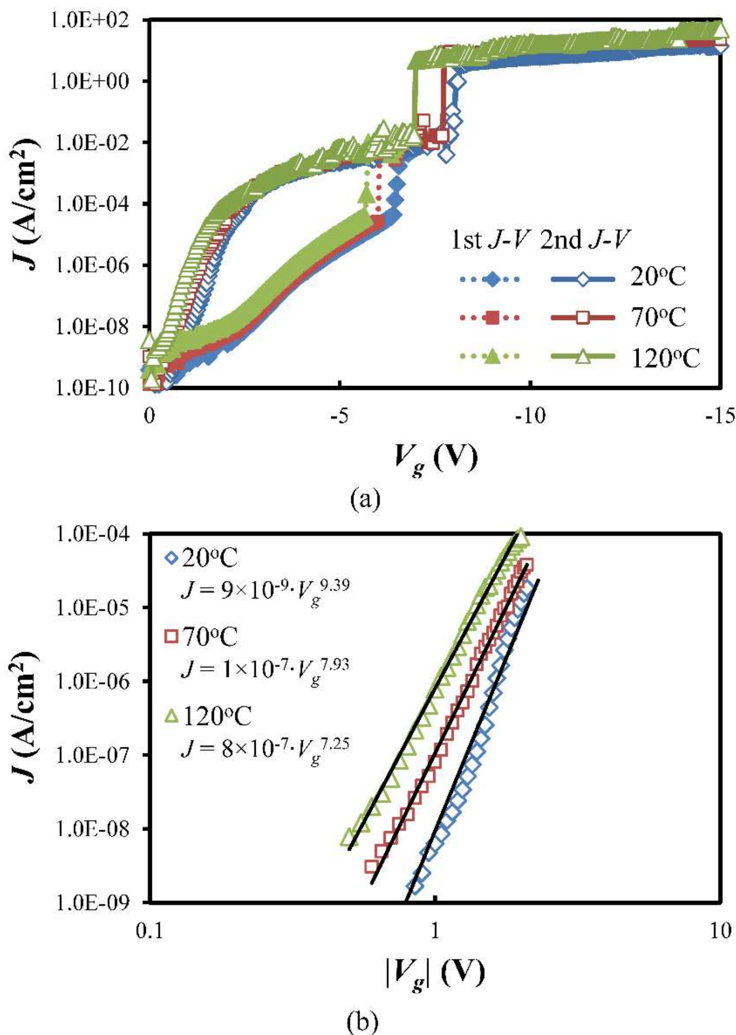

Figure 51. (a) *J-V* curves of the nc-CdSe embedded sample at 20 ºC, 70 ºC, and 120 ºC, respectively. 1st curves were measured from V_g = 0 V to immediately after the first-step breakdown. 2nd curves were measured from V_g = 0 V to −15 V. (b) Power law fitting of 2nd *J-V* curves.

Figure 52 shows *J-V* curves of the nc-CdSe embedded samples that were totally broken down previously. All curves were measured from V_g = 0 to −15 V. Above the $|V_{BD}|$, the leakage current increases linearly with the increase of the magnitude of voltage, i.e.,

following Ohm's law, which is due to the formation of nano-sized conductive paths in the high-k stack.[79,143,151] With the increase of temperature, the leakage current increases and the corresponding resistances (R's) decreases from 7360 Ω at 20 ºC to 5199 Ω at 70 ºC to 3093 Ω at 120 ºC. This trend is similar to the temperature dependence of a polysilicon resistor, i.e., the resistance decreases with the increase of temperature.[152]

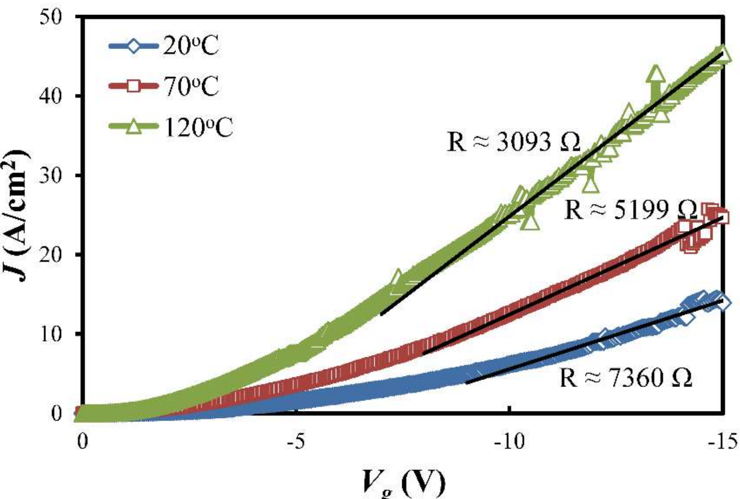

Figure 52. J-V curves of the nc-CdSe embedded sample at 20 ºC, 70 ºC, and 120 ºC, respectively. All samples were completely broken down previously. Ohm's law fitting of linear region of the curve.

The time-to-breakdown (t_{BD}) is an important parameter used to evaluate the reliability of a device, which can be described by the Weibull distribution:[153]

$$F\left(t_{BD}\right)=1-\exp\left[-\left(\frac{t_{BD}}{\alpha}\right)^{\beta}\right], \quad [18]$$

where F is the cumulative fraction of the failed devices, α is the characteristic t_{BD} for the cumulative failure fraction of 63.2%, and β is the shape factor of Weibull distribution, i.e., the Weibull slope. In the TDDB study, the Weibull distribution is usually plotted in the form of $W = \ln\{-\ln[1-F(t_{BD})]\} = \beta\cdot\ln(t_{BD}) - \beta\cdot\ln(\alpha)$ vs. $\ln(t_{BD})$ with a slope β, which is a measurement of the breakdown behavior.[153] Figure 53 shows the Weibull distribution of the nc-CdSe embedded sample stressed at $V_g = -7$ V and 20 ºC, 70 ºC, and 120 ºC, respectively. Each curve exhibits two distinct regions with different slopes, i.e., two β values can be extracted from the linear fitting of W vs. $\ln(t_{BD})$ at separate regions. The β in the low t_{BD} region is larger than that in the high t_{BD} region, which indicates the coexistence of extrinsic and intrinsic breakdown modes.[153] The former corresponds to the early extrinsic breakdown of the film from the process-induced defects.[153] The pre-existing traps in the film can form spots that require a low critical defect density (N_{BD}) to breakdown.[153] On the other hand, the long-term breakdown is related to the intrinsic properties of the film.[153] The β value in the high t_{BD} region is lower than that of SiO_2 in the intrinsic breakdown region (i.e., $\beta > 1$). The high-k film contains a large number of electrically active traps, which enhances the dielectric breakdown process. The trap-assisted charge transfer mechanism in the high-k film also accelerates its degradation.[154] Fig. 53 shows that the β value decreases with the increase of temperature. According to the percolation breakdown model, the N_{BD} value decreases with the increase of temperature, which therefore shows as the low β value.[130] With the increase of temperature, the trapped charges gain more energy to overcome the trapping state to transfer across a longer distance. Therefore, the fraction of defects with large effective

conduction radii, i.e., “defect size” increases with the temperature.[130] Then, fewer defects are needed to create percolation paths through the high-*k* stack. Eventually, the transition from the extrinsic breakdown mode to the intrinsic breakdown mode occurs quicker at the high temperature than at the low temperature. Previously, it was reported that the effect of process-induced defects could be suppressed at the high temperature.[153] So, the intrinsic breakdown of the nc-CdSe embedded ZrHfO film affects the TDDB process sooner with the increase of temperature.

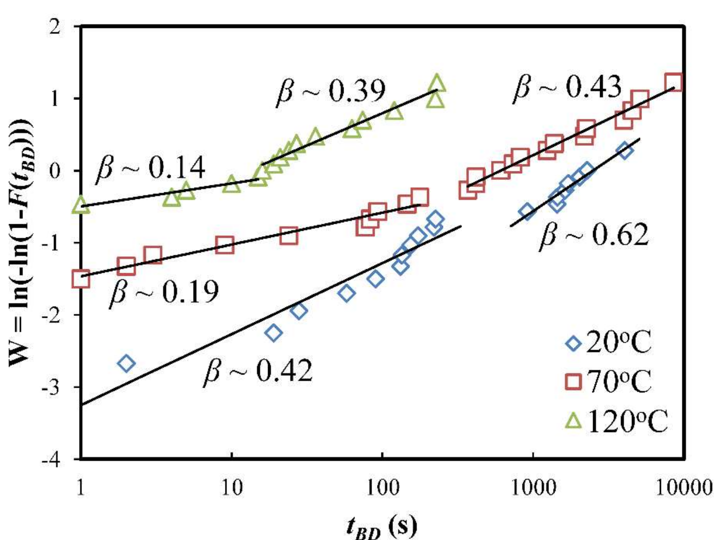

Figure 53. TDDB Weibull distribution of the nc-CdSe embedded sample stressed at V_g = −7 V 20 ºC, 70 ºC, and 120 ºC, respectively. β values are shown next to individual curves.

The charge-to-breakdown (Q_{BD}) parameter is an effective tool for the investigation of the N_{BD} and defect generation rate (R_{gen}) in the dielectric breakdown process. Figure 54

shows the Weibull function vs. Q_{BD} curves at $V_g = -7$ V and 20 ºC, 70 ºC, and 120 ºC, separately. The Q_{BD} was calculated by integrating J vs. time from the CVS curves until the high-k stack was totally broken down. When the temperature is increased, the Weibull function vs. Q_{BD} curve shifts to the lower Q_{BD} direction, which indicates the accelerated deterioration of the film by the temperature.[154] According to the percolation breakdown model, Q_{BD} can be expressed by the following equation:[153,154]

$$Q_{BD} = q\frac{N_{BD}}{R_{gen}}. \quad [19]$$

Since the high temperature enhances the generation of defects with large effective radii,[130,154] the N_{BD} required to form conductive paths can be reduced accordingly. The high temperature can also weaken the metal-oxide bonds in the high-k stack for easy generation of defects.[153] Therefore, the reduction of N_{BD} and the enhancement of R_{gen} with temperature consequently cause the decrease of Q_{BD}. The inset of Fig. 54 is the plot of Q_{63}, i.e., Q_{BD} at 63.2% failure fraction, vs. the inverse of temperature (1/T), which follows the Arrhenius relationship with an activation energy of 0.597 eV. This number is close to the observed activation energy of 0.5-0.6 eV in the TiN/HfO_2 MOS device.[155]

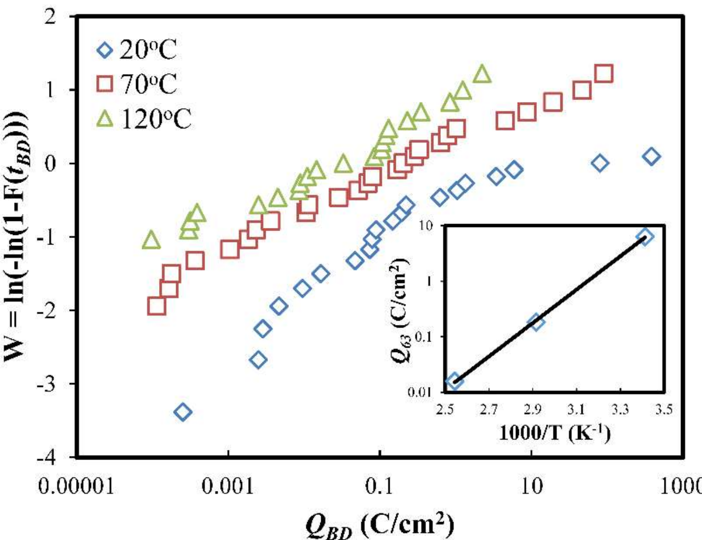

Figure 54. Weibull distribution of Q_{BD}'s of the nc-CdSe embedded sample stressed at V_g = −7 V and 20 ºC, 70 ºC, and 120 ºC, respectively. Inset: Arrhenius plot of Q_{BD} at 63.2% failure fraction (Q_{63}).

The J_{relax} is mainly contributed by two simultaneous mechanisms, i.e., the dielectric relaxation and charge detrapping.[143] Figure 55 shows the J_{relax}-t curves of the nc-CdSe embedded sample after the release of the stress voltage, i.e., V_g = −5 and +5 V for 120 s, respectively. For the first 20 s, the magnitude of J_{relax} ($|J_{relax}|$) decreases quickly in both cases. Then, the decrease rate of $|J_{relax}|$ is reduced gradually. When the temperature is raised, the initial J_{relax} is increased because of the gaining of thermal energy of the trapped charges.[157,158] The decay of J_{relax} with time follows the Curie-von Schweidler law:[96]

$$J_{relax}/P = a \cdot t^{-n}, \quad [20]$$

where P is the total polarization or surface charge density (V·nF/cm^2), t is the relaxation time after the removal of the stress voltage, a is a constant, and n is a real number close to 1. The n value corresponds to the J_{relax} decay over time, i.e., the smaller the n value is, the smaller the decay rate of J_{relax} is.[158] The n value can be obtained by replotting the J_{relax}-t curves in the log-log scale as shown in Figure 56. After the removal of $-V_g$ stress voltage (in the case of hole detrapping), the n value decreases from 0.839 at 20 ºC to 0.817 at 70 ºC to 0.772 at 120 ºC. Previously, two possible charge detrapping mechanisms were proposed to explain the temperature dependent n value change, i.e., thermal activation and quantum tunneling.[128,157] When the temperature is increased, the hole-trapping capacity of the nc-CdSe embedded sample is enhanced and the total amount of trapped holes increases. Since the hole detrapping is dominant by the tunneling mechanism, its detrap rate increases slightly with the temperature. Then, at certain time of the relaxation process, more holes are retained in the high-k stack at the high temperature, which are shown as the slow drop of the J_{relax} and the decrease of n.[157] On the other hand, in the case of the $+V_g$ stress, i.e., electron detrapping, the n value increases with the increase of temperature, i.e., 0.759 at 20 ºC to 0.836 at 70 ºC to 0.861 at 120 ºC. This shows that the electron detrapping is dominated by thermionic emission and trapped electrons are easy to release from the CdSe nanocrystals at the high temperature.[157] In addition, since there are fewer electrons trapped in the CdSe nanocrystals at the raised temperature, they are detrapped faster at the high temperature, which corresponds to the quick drop of the J_{relax} and the increase of n.

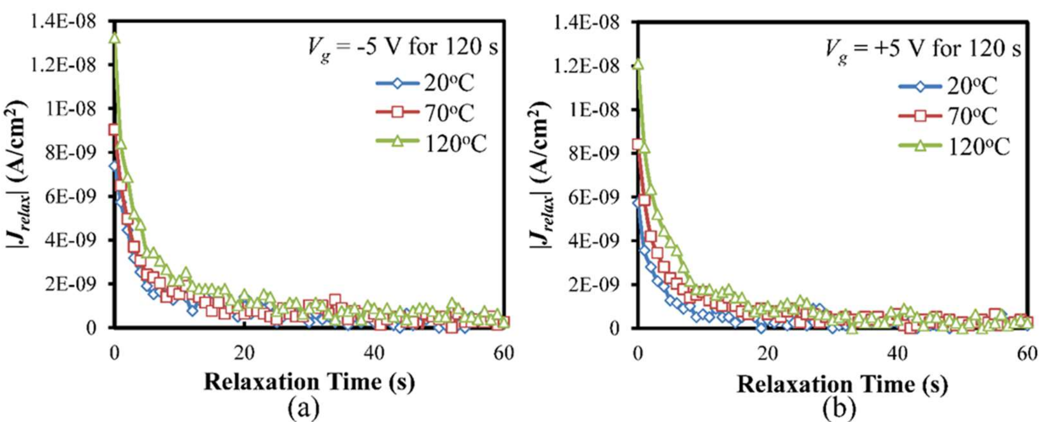

Figure 55. J_{relax}-t curves of nc-CdSe embedded sample after removal of stress voltage of V_g = (a) −5V and (b) +5 V for 120s at 20 ºC, 70 ºC, and 120 ºC, respectively.

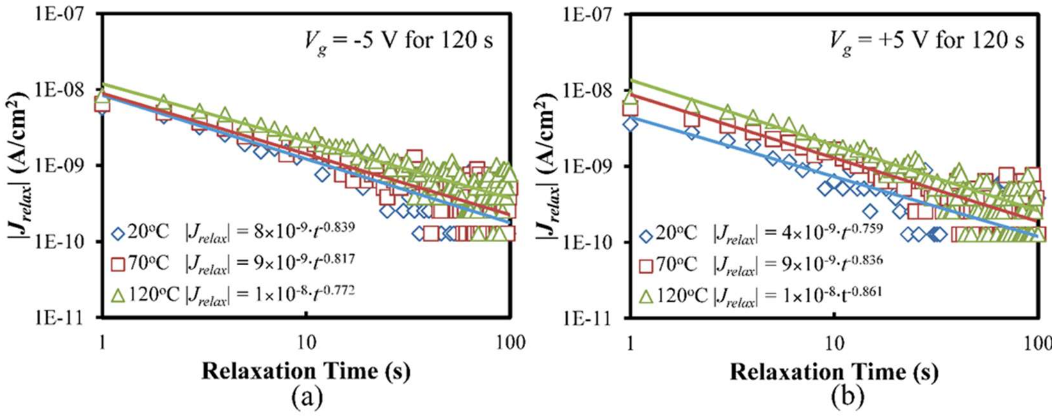

Figure 56. Log-log plot of J_{relax}-t curves of the nc-CdSe embedded sample after removal of stress voltage with Curie-von Schweidler fitting. Stress at V_g = (a) −5 V and (b) +5 V for 120 s at 20 ºC, 70 ºC, and 120 ºC, respectively.

The charge retention capability of the nc-CdSe embedded ZrHfO sample can be determined by the percentage of charges remaining in the device after releasing the stress

voltage, as calculated from Equation 15. Figure 57 shows the charge retention characteristics of the nc-CdSe embedded samples after being stressed at $V_g = -6$ V and +6 V for 20 s, separately. As shown in Fig. 57(a), some of the trapped holes were detrapped from the nc-CdSe embedded sample within the first 1,800 s independent of the temperature. These holes are loosely trapped at the nc-CdSe/ZrHfO interface.[112] The percentage of the loss of the loosely trapped holes decreases from 34% at 20 ºC to 29% at 70 ºC to 25% at 120 ºC. This is consistent with the *C-V* result that the high temperature enhances the trapping of holes. Subsequently, the remaining holes are strongly retained and slowly detrapped,[112] e.g., the percentages of lost trapped holes between 1,800 s and 36,000 s are 10% at 20 ºC, 13% at 70 ºC, and 16% at 120 ºC. The high temperature provides more thermal energy to the trapped holes to facilitate their detrapping.[131] As shown in the inset of Fig. 57(a), after 10 years, the percentage of remaining trapped holes decreases from 30% at 20 ºC to 23% at 70 ºC and 15% at 120 ºC. Unlike the detrapping of holes, the detrapping of electron from the nc-CdSe embedded sample does not show the two-stage phenomenon. Only few originally trapped electrons are lost in the first 1,800 s, i.e., 3% at 20 ºC, 4% at 70 ºC, and 10% at 120 ºC, and the detrapping rate decreases with time. Since electrons are only trapped in the nc-CdSe bulk, they are gradually released without drastic change of the detrapping curve.[112] Between 1,800 s and 36,000 s, the electron loss percentages are 18% at 20 ºC, 22% at 70 ºC, and 38% at 120 ºC, respectively, which are larger than those of holes loss in the same period of time. This is contributed by the *n*-type property of the nc-CdSe, which prefers to retain holes than electrons.[112] At 20 ºC, 29% of originally trapped electrons can remain in the nc-CdSe bulk

after 10 years. However, since the detrapping of electrons is greatly enhanced at the high temperature, the electron retention capability deteriorates more seriously than the hole retention capability does. For example, at 70 ºC, 16% of the trapped electrons are retained after 10 years while at 120 ºC, all the trapped electrons are lost after 763 days.

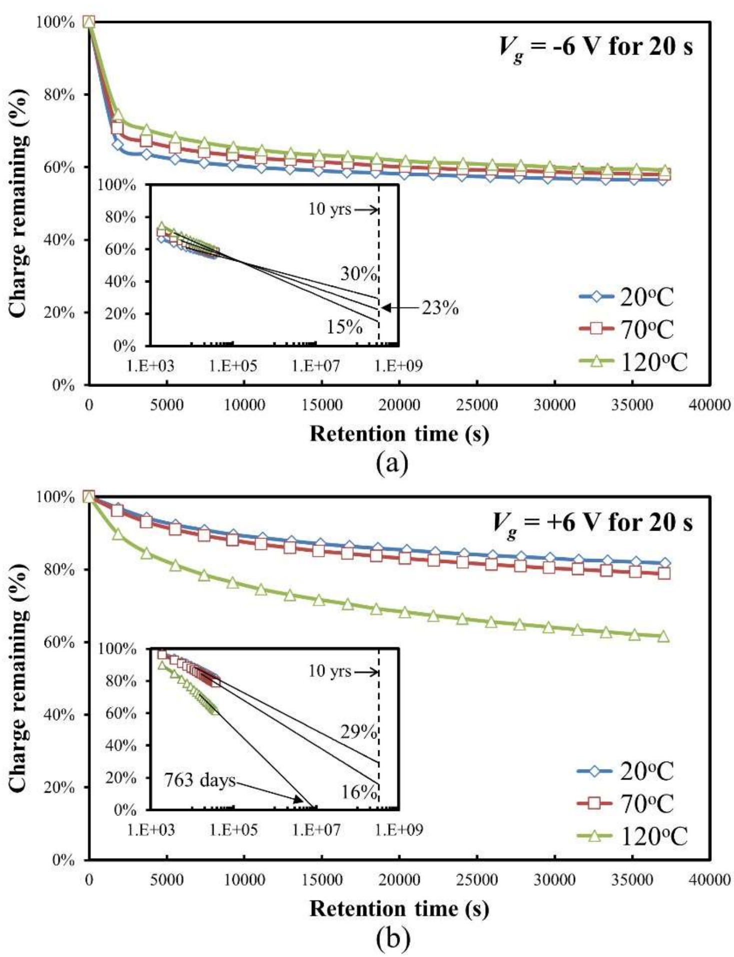

Figure 57. Charge retention characteristics of the nc-CdSe embedded sample after stress at V_g = (a) −6 V and (b) +6 V. Stress time: 20 s. Temperature: 20 ºC, 70 ºC, and 120 ºC, respectively. Inset: 10-year extrapolation curve.

4.5 Summary

The temperature effects on the charge trapping/detrapping and transfer mechanisms as well as the dielectric breakdown behavior and retention capabilities of the nc-CdSe embedded ZrHfO high-*k* dielectric MOS capacitor on the *p*-type Si wafer have been investigated.

In the first part, the *C-V* result showed that the hole trapping capacity increased with an increase of temperature but the opposite effect was observed on the electron trapping, which was contributed by the valence and conduction band offsets between ZrHfO and Si, the *n*-type property of CdSe, and the charge supply from the *p*-type Si substrate. The combination of the increase of hole-trapping and the decrease of electron-trapping caused a slight decrease of *C-V* hysteresis window with an increase of temperature, which indicated that the device still had large memory windows at high temperatures. At high temperatures, holes loosely trapped at the nc-CdSe/ZrHfO interface were more sensitive to the measurement frequency. However, electrons strongly trapped in the bulk nc-CdSe were independent from the measurement frequency at all temperatures. The *J-V* study showed that the Coulomb blockade effect was suppressed at high temperatures. The leakage current increased with an increase of temperature through the increase of the charge supply, charge detrapping, and conductivity of the high-*k* film. The charge transfer showed a strong temperature dependence. Under the negative V_g bias condition, a consistent description of hole transfer was found over the temperature range of 20-120 ºC: holes were transferred following the SE mechanism at the low electric field

and the P-F mechanism at the high electric field. Under the positive V_g bias condition, the electron transfer still followed the SE mechanism at the low electric field. However, the electron transfer became more complex at the large electric field: it changed from following the P-F mechanism at a low temperature to following the F-N tunneling at a high temperature.

In the second part, the two-step breakdown phenomenon was observed in the device due to the different failure mechanisms in the interface and the bulk ZrHfO layers. The breakdown process were accelerated by the raise of temperature due to the enhanced defect generation and the enlarged defect conduction radii. When only the interface layer was broken, the leakage current followed the power law. On the other hand, when both interface and bulk ZrHfO layers were broken, the charge transfer followed the ohmic law, which increased with the increase of temperature. The TDDB distribution of the nanocrystals embedded high-*k* sample was controlled by the process-induced defects and the intrinsic behavior of the high-*k* film. The high temperature enhanced the defect generation and reduced the N_{BD} through enlarging the effective radii of defects, which accelerated the aging of the device. At the same time, Q_{BD} showed an Arrhenius temperature dependence with an activation energy of 0.597 eV. The relaxation current study showed that the hole and electron detrapping were dominated by the tunneling and thermal activation, respectively. Since the electron trapping was weakened and the electron detrapping was enhanced at the elevated temperature, the retention capability for electrons degraded faster than that for holes.

In summary, the charge trapping/detrapping and transfer mechanisms as well as the breakdown process and retention capabilities of the nc-CdSe embedded ZrHfO capacitor are strongly influenced by the temperature, which is important for its memory application. This device can maintain its memory functions over a large temperature range with a consistent predictable current leakage model in the negative V_g range.

CHAPTER V

POST DEPOSITION ANNEALING ATMOSPHERE EFFECTS ON PERFORMANCE OF SOLID STATE INCANDESCENT LIGHT EMITTING DEVICES*

5.1 Introduction and Motivation

In the MOS capacitor, the PDA conditions PDA condition is critical to the material and electrical properties of the oxide bulk and interface.[1,159] For example, annealing in N_2 and O_2 at different temperatures can change the device's capacitance and leakage current.[159] Moreover, the PDA temperature has significant influence on the breakdown and light emission characteristics of SSI-LEDs.[75,77,160] Therefore, the PDA atmosphere can be another critical factor on electrical and optical properties of this new-type SSI-LED. In this chapter, we fabricated two ZrHfO gate dielectric SSI-LEDs with different PDA gases, N_2 and O_2, to investigate the effect of the PDA atmosphere on the electrical and optical properties of the SSI-LED.

5.2 Experimental

MOS capacitors composed of the same ZrHfO high-*k* dielectric thin film but different PDA atmospheres were fabricated on DHF cleaned *p*-type (10^{15} cm^{-3}) <100> Si wafers. The ZrHfO film was sputter-deposited from the Zr/Hf target in Ar/O_2 (1:1)

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atmosphere at 5 mTorr and 60 W for 12 min. Subsequently, the sample was processed with a PDA step at 800 ºC for 3 min under the N_2 or O_2 atmosphere using the RTA equipment. A $HfSiO_x$ interface layer was formed between the amorphous bulk ZrHfO layer and the Si substrate, which was confirmed from the electron spectroscopy for chemical analysis (ESCA) and the high resolution transmission electron spectroscopy (HRTEM).[30,116] Then, an 80 nm thick ITO film was deposited on top of the ZrHfO film and wet-etched into 300 μm diameter gate electrodes. An Al film was deposited on the backside of the wafer to form the ohmic contact. The complete sample was annealed at 400 ºC under H_2/N_2 (1:9) atmosphere for 5 min. The sample's electrical properties were extracted from the C-V and J-V measurements. To form the SSI-LED, the capacitor was first applied with a V_g larger than the V_{BD} to form conductive paths. Subsequently, when a V_g was applied to the ITO gate electrode, the conductive paths were excite to emit light.

5.3 PDA Atmosphere Effects on Electrical Properties

Figure 58 shows C-V hysteresis curves of N_2 and O_2 PDA capacitors with V_g swept from −2 to +1 V (forward) and then back to −2 V (backward) at 1 MHz. Table 2 lists electrical parameters calculated from these C-V curves. Both samples show negligibly small hysteresis windows, i.e., ΔV_{FB} = 0.0031 V and 0.0025 V for the N_2 and O_2 PDA conditions, separately. In the accumulation region, the N_2 PDA sample has a larger capacitance than the O_2 PDA sample does, i.e., 2.01×10^{-10} F vs. 1.87×10^{-10} F. Since the EOT of the former is smaller than that of the latter, i.e., 11.12 nm vs. 12.03 nm, there are two possible explanations for this result. First, since the $HfSiO_x$ interface layer of the O_2

PDA sample is more SiO_x-rich than that of the N_2 PDA sample, the former has a lower effective *k* value than the latter.[30] Second, the larger total physical thickness of the O_2 PDA sample contributes to the its lower capacitance.[160] Furthermore, the D_{it} and Q_{ot} of the O_2 PDA sample, i.e., 1.61×10^{11} $cm^{-2}\cdot eV^{-1}$ and 5.21×10^{9} cm^{-2}, separately, are smaller than those of the N_2 PDA sample, i.e., 1.80×10^{11} $cm^{-2}\cdot eV^{-1}$ and 7.13×10^{9} cm^{-2}, separately. The same trend was observed in other similar devices.[30] The annealing process can reduce defect densities in the bulk ZrHfO and $HfSiO_x$ interface layers, e.g., by removing oxygen vacancies or passivating dangling bonds.[30,161] Therefore, the PDA atmosphere is an important factor in determining the dielectric properties of the capacitor that will be broken down to form the SSI-LED.

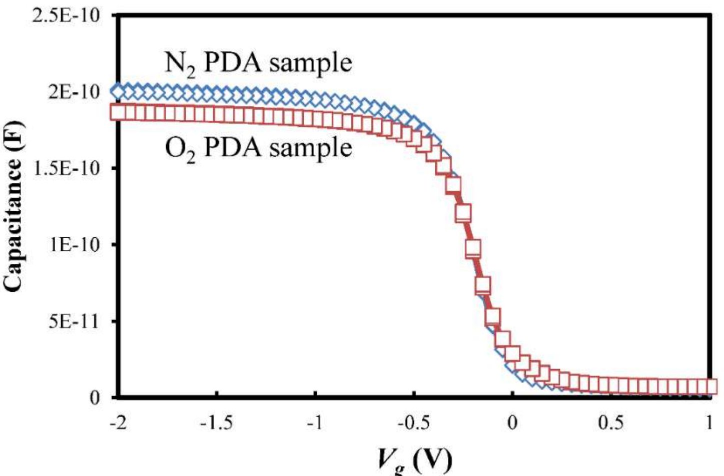

Figure 58. *C-V* hysteresis curves of N_2 and O_2 PDA capacitors. V_g swept from −2 to +1 to −2 V at 1 MHz.

Table 2. Parameters calculated from *C-V* hysteresis curves of the N_2 and O_2 PDA samples.

Condition	C (F)	EOT (nm)	ΔV_{FB} (V)	D_{it} (cm^{-2}·eV^{-1})	Q_{ot} (cm^{-2})
N_2 PDA	2.01×10^{-10}	11.12	0.0031	1.80×10^{11}	7.13×10^{9}
O_2 PDA	1.87×10^{-10}	12.03	0.0025	1.61×10^{11}	5.21×10^{9}

Figure 59 shows *I-V* curves of N_2 and O_2 PDA capacitors with V_g swept from 0 to −10 V. Each curve shows the apparent breakdown phenomenon, i.e., the current jumps abruptly by several orders of magnitude at V_{BD}. The $|V_{BD}|$ of the N_2 PDA sample is smaller than that of the O_2 PDA sample, i.e., −5.65 V vs. −6.1 V, which may be contributed by the difference in their physical thicknesses.[77,160] Also, the breakdown strength of the ZrHfO stack is related to the defect density in the original film.[160,162] Since the O_2 PDA sample has fewer defects in the ZrHfO bulk and $HfSiO_x$ interface layers than the N_2 PDA sample has, the former is more difficult to break down to form conductive paths than the latter is. Fig. 59 shows that after breakdown, the leakage current of the device increases almost linearly with the increase of $|V_g|$, i.e., following Ohm's law. Also, the leakage current of the O_2 PDA sample is smaller than that of the N_2 PDA sample. Previously, it was observed that the former contained fewer conductive paths that the former.[162] In addition, conductive paths in the former are longer and less conductive than those in the latter. These factors contribute to the lower leakage current of the after-breakdown O_2 PDA sample.

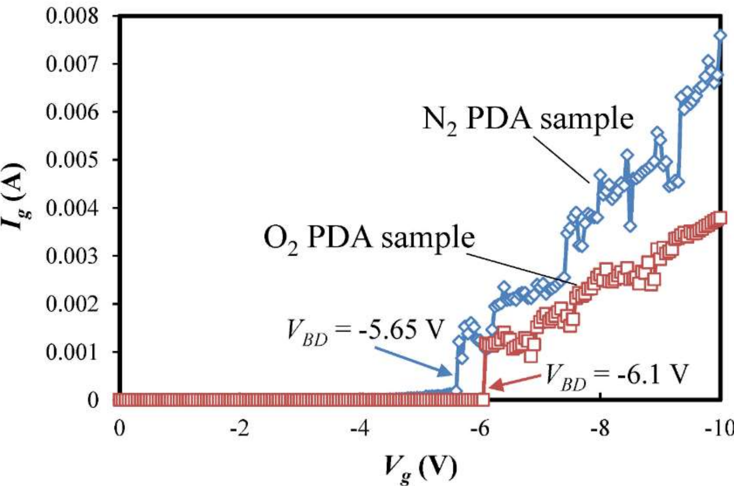

Figure 59. *I-V* curves of the N_2 and O_2 PDA capacitors stressed with V_g swept from 0 to −10 V.

To further study the function of the conductive path in the ZrHfO high-*k* stack, samples at three different process steps were characterized: (a) fresh MOS capacitors before breakdown, (b) devices immediately after breakdown, i.e., with a quick V_g sweep from 0 V to −10 V, and (c) devices after being stressed at V_g = −20 V for 20 min. Figure 60 shows *C-V* curves of (a) N_2 and (b) O_2 PDA samples, separately, measured by sweeping V_g from −2 to +1 V at 1 MHz. After the initial breakdown, the shape of the *C-V* curve is similar to that of the fresh capacitor except the negative shift and the lower capacitance. Immediately after the breakdown, the conductive path is not fully developed, i.e., the resistance is still high in the low V_g range. Therefore, the complete device behaves like a low-quality capacitor.[163] The negative shift of the *C-V* curve is due to the generation of

hole-trapping defects in the breakdown process.[95] The original O_2 PDA capacitor has better electrical properties than those of the original N_2 PDA capacitor. For example, in addition to a larger V_{BD} as shown in Fig. 59, the former has a smaller D_{it} than the latter, i.e., 4.16×10^{11} $cm^{-2}\cdot eV^{-1}$ vs. 1.29×10^{12} $cm^{-2}\cdot eV^{-1}$. Immediately after the breakdown, the O_2 PDA sample remains a better capacitor than the N_2 PDA sample does, e.g., a smaller *C-V* shift of 0.5 V instead of 0.85 V. This result is consistent with the smaller leakage current of the former compared with that of the latter, as shown in Fig. 59. After the sample is stressed with a voltage much larger than the V_{BD} for a long period, i.e., at −20 V for 20 min, conductive paths are fully developed and the high-*k* stack loses the insulating capability.[163] The *C-V* curve of the N_2 PDA sample is more flat than that of the O_2 PDA sample because of the formation of more conductive paths in the former.

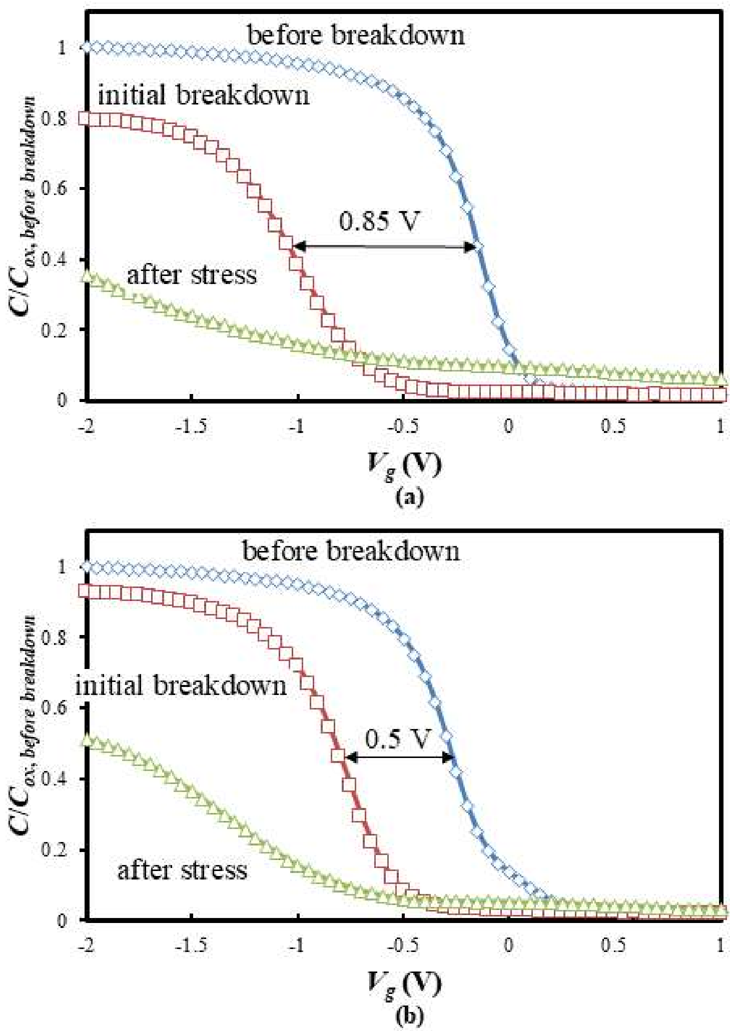

Figure 60. *C*-*V* curves of (a) N_2 and (b) O_2 PDA samples before breakdown, after initial breakdown, and after $V_g = -20$ V, 20 min stress. V_g swept from −2 V to +1 V at 1 MHz.

Since electrical properties of the MOS capacitor vary with the PDA atmosphere, the composition of the high-*k* stack should change accordingly. Figure 61 shows SIMS profiles of In, O, Zr, Si, and SiO elements in (a) N_2 and (b) O_2 PDA capacitors before the breakdown. For both samples, the $^{115}In^+$ signal drops sharply at the ITO/ZrHfO interface.

Therefore, the PDA atmosphere has little effect on the reaction between ITO and ZrHfO. On the other hand, the $^{16}O^{+}$ signal drops gradually across the ZrHfO layer until the Si substrate. Currently, it is difficult to identify the source of $^{16}O^{+}$, which can come from ITO, ZrHfO, or the O_2 PDA gas. The $^{90}Zr^{+}$ signal is only detected in the ZrHfO high-*k* stack. The $^{28}Si^{16}O^{+}$ and $^{28}Si^{+}$ signals are located at the ZrHfO/Si interface because their peaks are closer to the Si substrate than the $^{90}Zr^{+}$ peak is. Therefore, the $^{28}Si^{16}O^{+}$ component must be from the $HfSiO_x$ interface layer formed between the bulk ZrHfO and the Si substrate.[30,116] The above elements are good references for the comparison of the O_2 and N_2 PDA samples. The peak ratio of $^{28}Si^{16}O^{+}$ in the interface layer to $^{28}Si^{+}$ in the Si substrate of the O_2 PDA sample is larger than that of the N_2 PDA sample, i.e., 2.21 vs. 1.59. Therefore, the $HfSiO_x$ interface layer in the former is more SiO_x-rich than that in the latter, which is consistent with the ESCA result on similar samples.[30] Moreover, the $^{28}Si^{16}O^{+}$ signal in the O_2 PDA sample is slightly broader than that in the N_2 PDA sample, which can be explained by the former's thicker interface layer. During the annealing, O_2 could diffuse through the high-*k* film to reach and react with the Si substrate to facilitate the growth of the interface layer.[164]

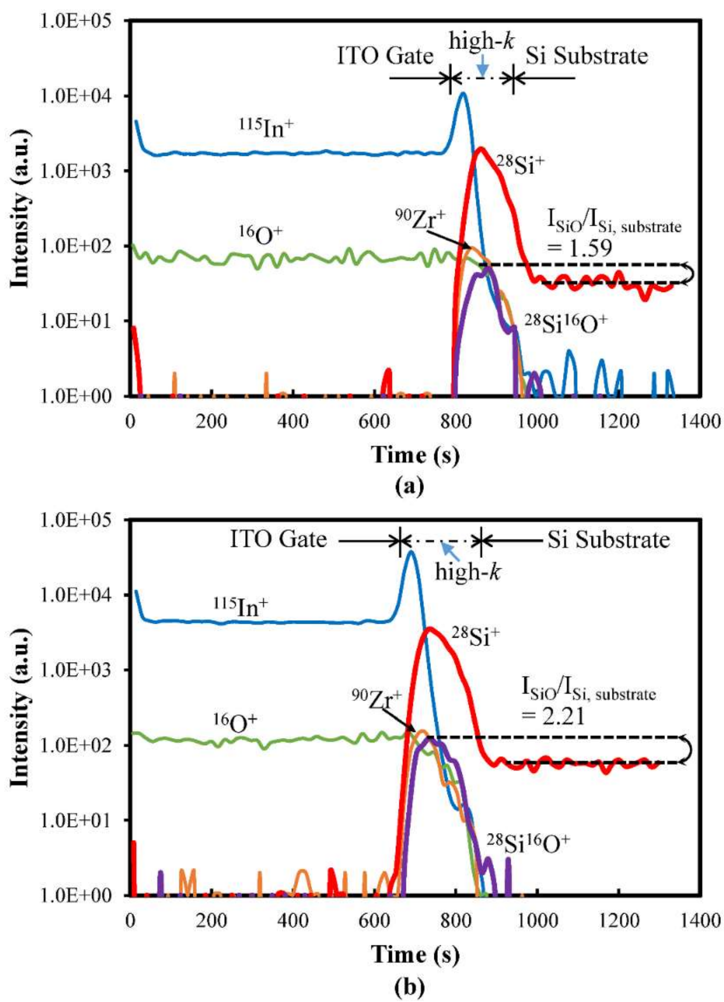

Figure 61. SIMS elemental profiles of (a) N_2 and (b) O_2 PDA capacitors. I_{SiO}: peak intensity of $^{28}Si^{16}O^+$ signal. $I_{Si, substrate}$: average intensity of the $^{28}Si^+$ signal in Si substrate.

5.4 PDA Atmosphere Effects on Light Emission Characteristics

Figure 62 shows high magnification photos of lights emitted from (a) N_2 and (b) O_2 PDA SSI-LEDs. For both samples, lights are emitted from tiny and discrete dots evenly distributed across the ITO electrode surface. This light emitting pattern is different from the uniform light emission from the conventional semiconductor-based LED. Light

emitted from the SSI-LED is the thermal excitation of nano-sized conductive paths surrounded by the high-k dielectric film,[73-80] while light emitted from the conventional LED is from the electron-hole or exciton-exciton recombination.[60-63] The brightness and number of light emitting dots in Fig. 62 samples increase with the increase of $|V_g|$. At the same V_g, there appears to be a larger number of smaller light emitting dots in Fig. 62(a) than that in Fig. 62(b) except on the edge. However, the dots in the O_2 PDA sample look brighter than most of those in the N_2 PDA sample, except a few larger dots in the latter randomly distributed in the central and edge area. This phenomenon may be due to the difference in sizes and compositions of the conductive paths which determine the thermal excitation efficiency.[73-76,79]

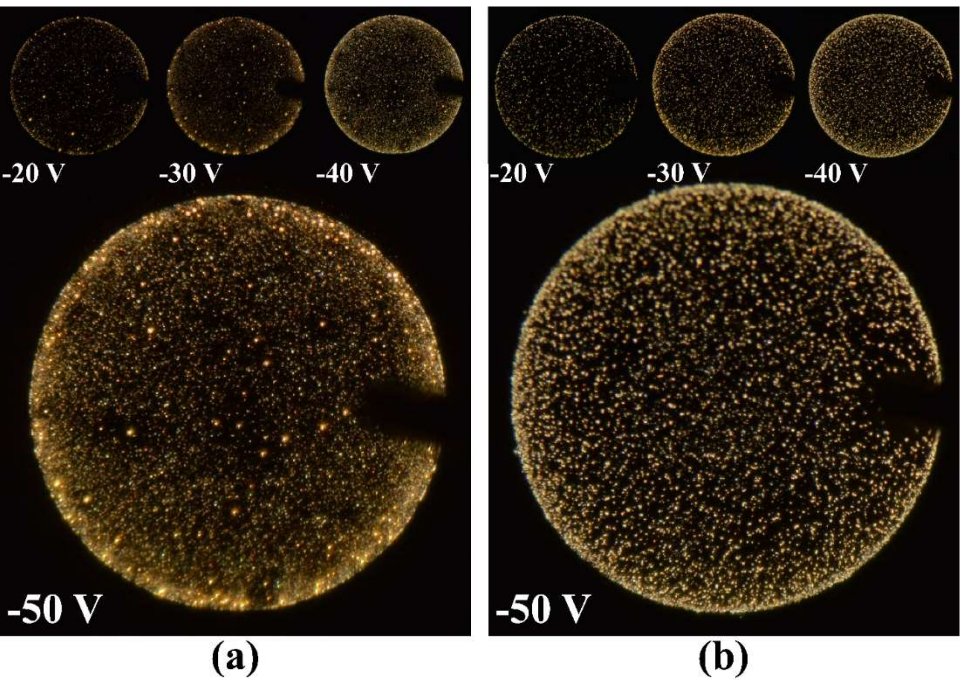

Figure 62. High-magnification photos of light emissions from (a) N_2 and (b) O_2 PDA SSI-LEDs at $V_g = -20$ to -50 V.

Figures 63 shows light emission spectra of (a) N_2 and (b) O_2 PDA SSI-LEDs, separately. The light intensity increases with the increase of $|V_g|$, which is consistent with the trend of brightness change in Fig. 62. The higher $|V_g|$ induces a larger leakage current to excite the conductive path for stronger light emission.[77,165] At the same V_g, the light intensity of the O_2 PDA sample is higher than that of the N_2 PDA sample. This result is consistent with the observation in Fig. 62. However, Fig. 63(c) shows that the leakage current of the O_2 PDA sample is lower than that of the N_2 PDA sample. Therefore, conductive paths in the O_2 PDA sample are more effectively excited than those in the N_2 PDA sample.

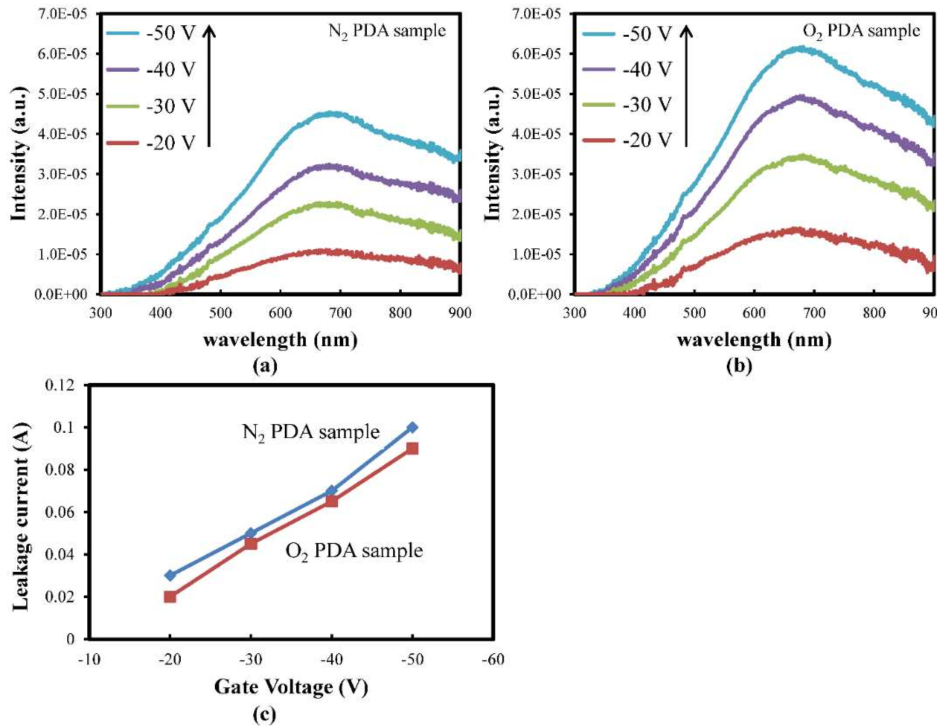

Figure 63. Emission spectra of (a) N_2 and (b) O_2 PDA SSI-LEDs, and (c) leakage currents at $V_g = -20$ to -50 V.

Figure 64 shows relative *EQE*'s of SSI-LEDs (in arbitrary unit) of the O_2 and N_2 PDA SSI-LEDs calculated from Equation 12a and 12b. The actual *EQE*'s of these devices should be much larger than those in the figure because the spectra were collected through the tip of an optical fiber about 2 mm above the surface of the ITO electrode. At the same V_g, the *EQE* of the O_2 PDA sample is consistently higher than that of the N_2 PDA sample. Since the light emission efficiency of a SSI-LED is a complicated function of the composition, size, and distribution of conductive paths, more studies are required to identify the actual factors contributing to the *EQE* difference.

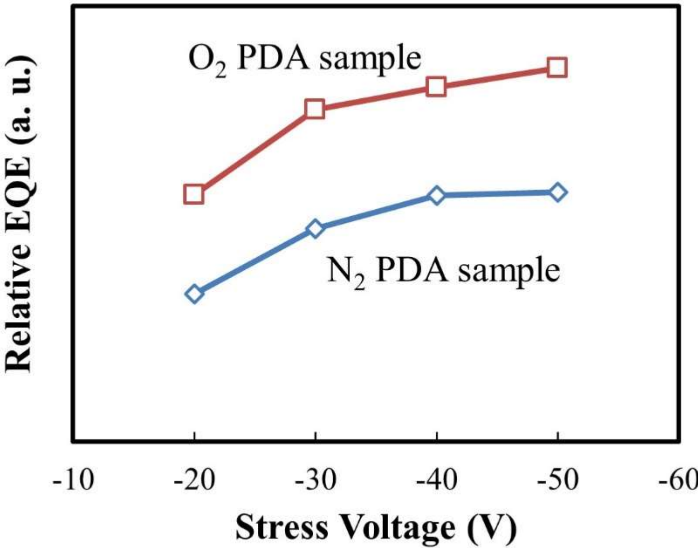

Figure 64. Relative *EQE*s of N_2 and O_2 PDA SSI-LEDs at $V_g = -20$ to -50 V.

Figure 65 shows emission spectra of the SSI-LEDs in Fig. 63 normalized with the peak intensities. They almost overlap except the very slight blue shift of the O_2 PDA sample and the very small red shift of the N_2 PDA sample. This phenomenon is consistent with the previous observation that dots in Fig. 63(b) appeared to be brighter and whiter than those in Fig. 63(a). It also indicates that the same light emission principle, i.e., thermal excitation of the conductive path, is applicable to both N_2 and O_2 PDA samples.[73]

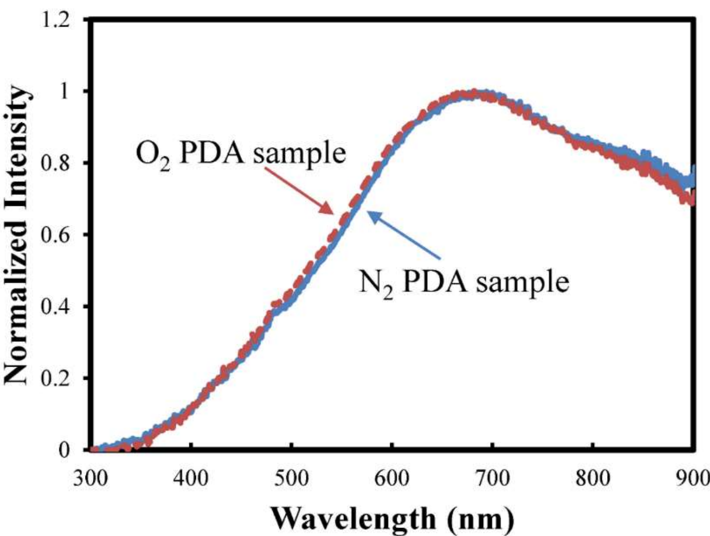

Figure 65. Normalized light emission spectra of N_2 and O_2 PDA SSI-LEDs at $V_g = -50$ V. $\lambda_{peak} = 682$ nm.

The CCT's and CRI's of emission spectra of Fig. 64 samples stressed at different V_g's have been calculated and summarized in Table 3. Both samples have high CRI R_a's, i.e., 94.4-98.6 for the N_2 PDA SSI-LED and 93.9-98.3 for the O_2 PDA SSI-LED. They are close to those of the incandescent light bulb that emits light based on black body emission.[77] The R_a values also increase with the increase of $|V_g|$. Figure 66 shows changes of CIE coordinates of these two samples with the increase of $|V_g|$ in the chromaticity chart. Lights emitted from the N_2 and O_2 PDA SSI-LEDs are located in the warm white light region close to the location of the incandescent light bulb.[166] The chromaticity distance between the sample and the Planckian locus decreases with the increase of $|V_g|$. Therefore, the light emission characteristics of the SSI-LED approach those of the black body emission with the increase of the applied voltage.[165,166] At the same time, the CCT

increases with the increase of $|V_g|$, which is also consistent with the phenomena of thermal excitation generated light emission.[167] Compared with the N_2 PDA SSI-LED at the same V_g, the O_2 PDA SSI-LED has a slightly higher CCT and the color coordinate is closer to the blue light region. Therefore, conductive paths in the O_2 PDA SSI-LED have a higher local temperature and emit the light with higher energy than those in the N_2 PDA SSI-LED do. The smaller CRI R_9 values of the O_2 PDA SSI-LED also reflect the rendering of light in the red color region.

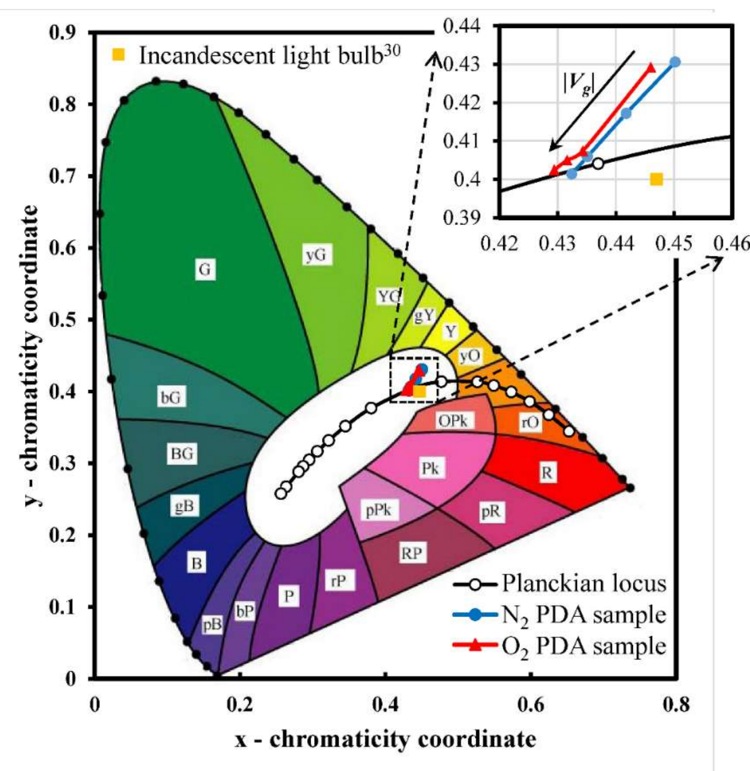

Figure 66. Color coordinates of N_2 and O_2 PDA SSI-LEDs at $V_g = -20$ to -50 V in the CIE chromaticity chart. Planckian locus and color coordinates of an incandescent light are included for references.[166]

Table 3. CIE characteristics of the N_2 and O_2 PDA SSI-LEDs.

PDA condition	V_g (V)	CCT (K)	CRI R_a	CRI R_9
N_2 PDA	-20	2994	94.4	82.7
	-30	3026	96.4	85.4
	-40	3046	98.6	93.1
	-50	3056	98.5	92.3
O_2 PDA	-20	3049	93.9	77.9
	-30	3073	97.6	87.8
	-40	3101	97.9	88.7
	-50	3118	98.3	91.1

Previously, it was proved that conductive paths were physically formed in the high-*k* stack after the dielectric breakdown process.[79] Therefore, compositions of the high-*k* stack before and after the formation of conductive paths can be different. Figure 67 shows SIMS depth profiles of $^{28}Si^+$, $^{16}O^+$, $^{115}In^+$, $^{28}Si^{16}O^+$, and $^{90}Zr^+$ in (a) N_2 and (b) O_2 PDA samples before, i.e., fresh MOS capacitors, and after formation of conductive paths, i.e., from $V_g = -20$ V, 20 min stress. Since the size of the SIMS spot is large, i.e., 50 μm × 50 μm, signals in the SSI-LED are contributed by both conductive paths and non-conductive path areas. For the N_2 PDA SSI-LED, $^{28}Si^+$ is detected in the ITO layer after the stress, which indicates the diffusion of the substrate material through the conductive paths to the gate electrode.[79] The similar phenomenon of Si atoms migration from the substrate to the gate electrode during the dielectric breakdown of a MOSFET was observed.[168] There are no major changes in $^{115}In^+$, $^{16}O^+$, $^{90}Zr^+$, and $^{28}Si^{16}O^+$ signal distributions before and after the V_g stress in the N_2 PDA samples. The intensity of $^{28}Si^+$ in the ITO film of the O_2 PDA SSI-LED is 15 times larger than that in the original MOS

capacitor. It is also much larger than that in the N_2 PDA SSI-LED, which can be explained by the higher local temperature of the conductive path in the O_2 PDA SSI-LED sample.[79] After the stress, the O_2 PDA sample has broad tails of the $^{28}Si^{+}$, $^{16}O^{+}$, $^{115}In^{+}$, $^{28}Si^{16}O^{+}$, and $^{90}Zr^{+}$ signals, which can also be contributed by the high temperature of the conductive path.[79,169-172] The higher temperature of the conductive path in the O_2 PDA SSI-LED is also responsible for its higher light emission efficiency.

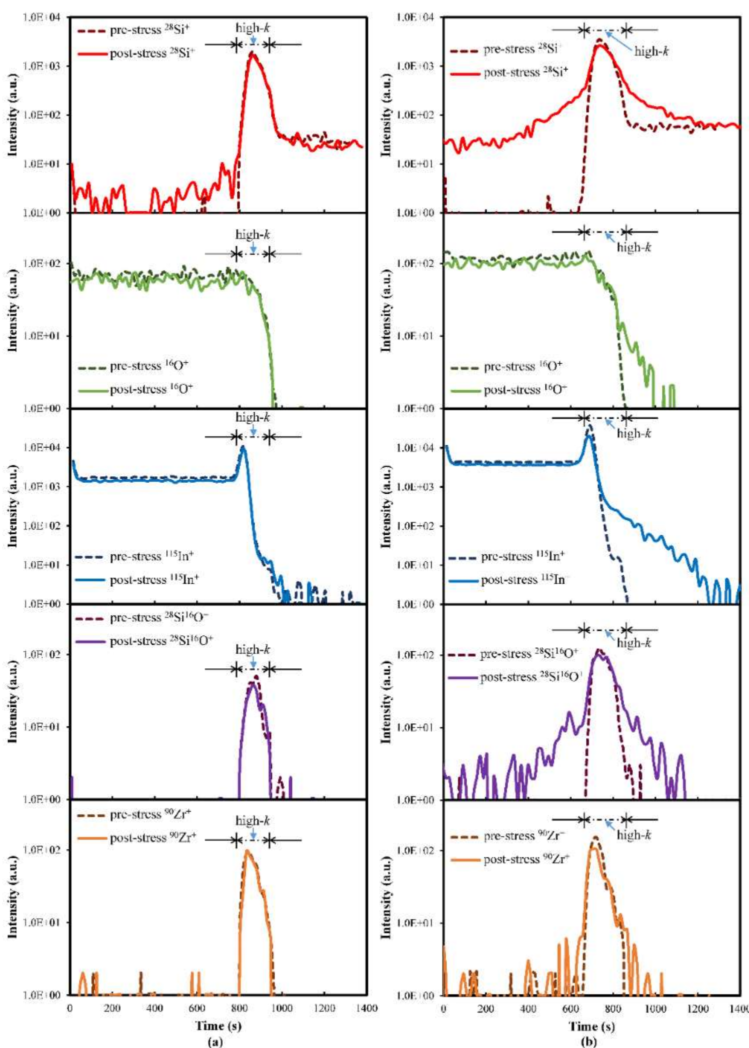

Figure 67. SIMS profiles of $^{28}Si^+$, $^{16}O^+$, $^{115}In^+$, $^{28}Si^{16}O^+$, and $^{90}Zr^+$ of (a) N_2 and (b) O_2 PDA samples before and after breakdown with $V_g = -20$ V for 20 min.

5.5 Summary

Electrical and light emission characteristics of SSI-LEDs made from MOS capacitors of the same sputter-deposited ZrHfO high-*k* film but different PDA atmospheres have been studied. The O_2 PDA capacitor contains a thicker and more SiO_x-

rich $HfSiO_x$ interfacial layer as well as lower defect densities than those of the N_2 annealed capacitor. Therefore, the former has a lower leakage current and a higher dielectric breakdown strength, which makes it more difficult to form conductive paths. When stressed at the same V_g, conductive paths in the O_2 PDA SSI-LED are more effectively excited to emit stronger light than those in the N_2 PDA SSI-LED. The CIE chromaticity coordinates, CRI's, and CCT's of the N_2 and O_2 PDA SSI-LEDs are close to those of the conventional incandescent lamp. The emission spectrum of the O_2 PDA SSI-LED is lightly more bluish than that of the N_2 PDA SSI-LED because of the higher local temperature in the conductive path. The SIMS elemental analysis result shows higher concentrations of Si and O in the high-*k* stack of the O_2 PDA SSI-LED probably due to the faster diffusion of these elements through the conductive paths. In summary, the PDA atmosphere affects the high-*k* stack's physical and material properties in the original capacitor, which influences the formation mechanism, composition, and number of conductive paths and eventually the electrical and optical characteristics of the SSI-LED.

CHAPTER VI

ELECTRICAL PROPERTIES OF NANO-RESISTORS IN ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K THIN FILMS*

6.1 Introduction and Motivation

In the SSI-LED, the light is emitted from the thermal excitation of nano-resistors during the passage of a large current.[73-80] However, there is lack of detailed information of electrical properties of these novel nano-resistor in the device. In this chapter, the author investigated the effective resistance and Schottky barrier height of the nano-resistors formed in the ZrHfO-based SSI-LED under different voltage stresses at different temperatures.

6.2 Experimental

The ZrHfO SSI-LED in this chapter was made from a metal-oxide-semiconductor (MOS) capacitor fabricated on a *p*-type <100> Si (10^{15} cm^{-3}) wafer. The 10 nm thick gate dielectric was a ZrHfO high-*k* film sputter-deposited from the Zr/Hf target in Ar/O_2 (1:1) at 5 mTorr and 60 W. Then, the sample was treated with a PDA step at 800 °C in N_2 for 3 min. After the process, the ZrHfO film remained amorphous and a $HfSiO_x$ IL was formed at the contact with the Si substrate, which was confirmed in the HRTEM.[116] Subsequently,

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* Reprinted with permission from "Resistivity and Barrier Height of Nano-Resistors Made from Zr-Doped HfO_2 High-*k* Dielectric on Si Wafer," by Shumao Zhang and Yue Kuo, 2017. *ECS Trans.*, **77** (2), 63-68, Copyright 2017 by the Electrochemical Society

an 80 nm thick ITO film was deposited on top of the ZrHfO thin film and wet etched into 300 μm-diameter gate electrodes. An Al film was deposited on the backside of the wafer to form the ohmic contact. Eventually, the complete sample was annealed at 400 °C in H_2/N_2 (1:9) for 5 min. Nano-resistors were formed after the HBD of the MOS capacitor with the applying a V_g that is larger than the V_{BD} for a period of time.

6.3 Bump Formation above the Nano-Resistor During Stress

Figure 68 shows (a) AFM and (b) SEM micrographs of the surface of the sample after being stressed at $V_g = -30$ V for 20 min. There are many tiny bumps evenly distributed on the electrode surface. Each bump corresponds to a conductive path, i.e., nano-resistor, formed from the breakdown of the high-*k* dielectric film.[79] Fig. 68(c) shows the cross-sectional view of the nano-resistors formed from the process. The SIMS study showed that the nano-resistor contained Si, Hf, Zr, In, and other elements.[79,81] Bumps in Fig. 68(a) and (b) are formed from the melting of the ITO layer due to the high local temperature in nano-resistors during the passage of the large current.[79,173] The actual size of the nano-resistor in the high-*k* film is much smaller than that of the bump.[76] Fig. 68(d) shows the influence of the stress voltage on the bump size. The bump numbers were counted from SEM micrographs over a 5 μm × 6 μm area. Due to the resolution limit, it is difficult to estimate numbers of bumps with less than 20 nm in diameter. It is clear that the total bump number increases with the increase of the magnitude of the stress voltage. Most bumps have the small diameter of 20-60 nm, i.e., 71.0%, 84.3%, and 85.3% for the $V_g = -20$ V, -30 V, and -40 V stressed samples, separately. The area ratio of all bumps

to the ITO electrode increases from 4.44% for the −20 V stress sample to 5.02% for the −30 V stress sample to 5.91% for the −40 V stress sample. Therefore, the number and size of nano-resistors on the sample surface increase with the increase of stress voltage.

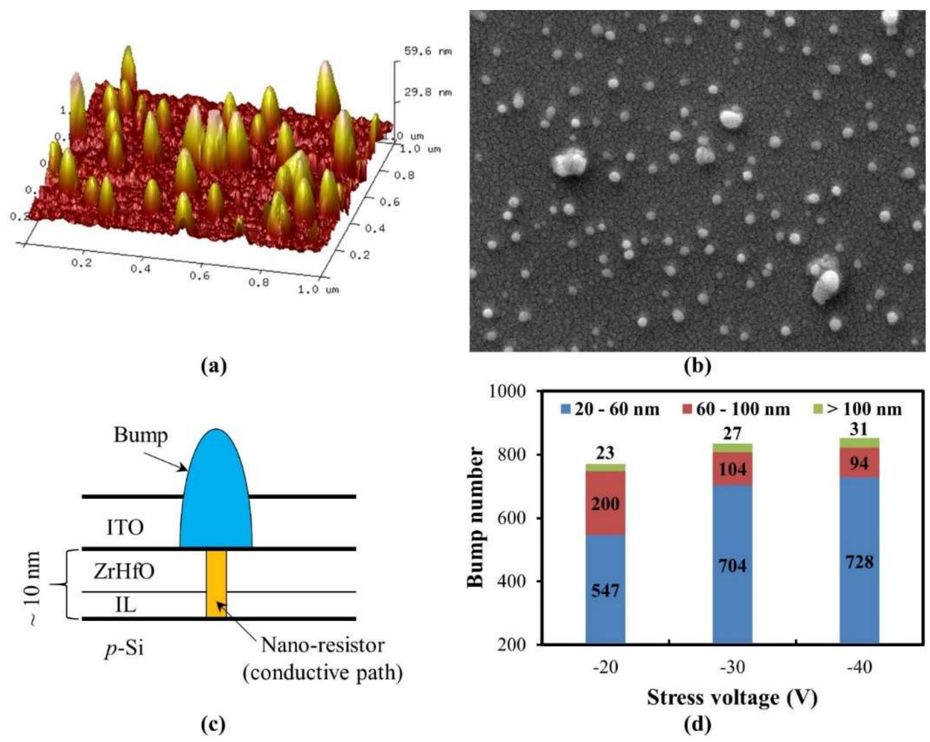

Figure 68. (a) AFM and (b) top-view SEM micrographs of bumps formed on the ITO gate surface of the sample after the $V_g = -30$ V, 20 min stress. (c) Cross-sectional view of a nano-resistor with a bump above it. (d) Distributions of bump diameter of bumps on gate surfaces of samples after being stressed at $V_g = -20$, -30, and -40 V for 20 min.

6.4 Estimation of Effective Resistance and Schottky Barrier Height

Figure 69 shows the *I-V* curve of a sample after the $V_g = -30$ V, 20 min stress. The current conduction mechanism in the sample varies with the magnitude of the applied

voltage.[163] In the high $|V_g|$ range, i.e., $|V_g| > 8$ V, the current increases linearly with the increase of the magnitude of V_g, following the Ohm's law. A constant resistance (R_s) of 353 Ω is extracted from the slope of the *I-V* curve. It is contributed by all resistances in the device, including the resistance of all nano-resistors in parallel, the spreading resistance (R_{sp}) of the Si substrate, the resistance of the ITO gate electrode, ITO/nano-resistor contact resistances, and nano-resistor/Si contact resistances. It was reported that when conductive paths were formed from the hard breakdown of the metal oxide MOS capacitor, contacts at the gate/conductive path and conductive path/Si could be taken as the ohmic and Schottky contacts, seperately.[83,163] Since R_s is extracted at the large $|V_g|$, the Schottky contact resistance is negligibly small compared with other resistances, such as the nano-resistor effective resistance and the Si substrate resistance.[174] Since the ohmic contact and gate electrode resistances are very small, they can be further neglected. Then, the effective resistance of the nano-resistors, i.e., contributed by all nano-resistors in the device connected in parallel, can be estimated by deducting the R_{sp} from R_s. R_{sp} of the Si substrate is a function of its resistivity ρ, thickness h, and the diameter of the device d, following the equation of[163,175]

$$R_{sp} = \frac{\rho}{\pi d} \tan^{-1}\left(\frac{4h}{d}\right), \qquad [21]$$

For the Si wafer used in this study, the R_{sp} is 199 Ω at room temperature. The effective resistance of the nano-resistors of the device in Fig. 69 is 154 Ω. Therefore, in the large $|V_g|$ range, the resistance of the Si substrate is comparable to that of the nano-resistors.

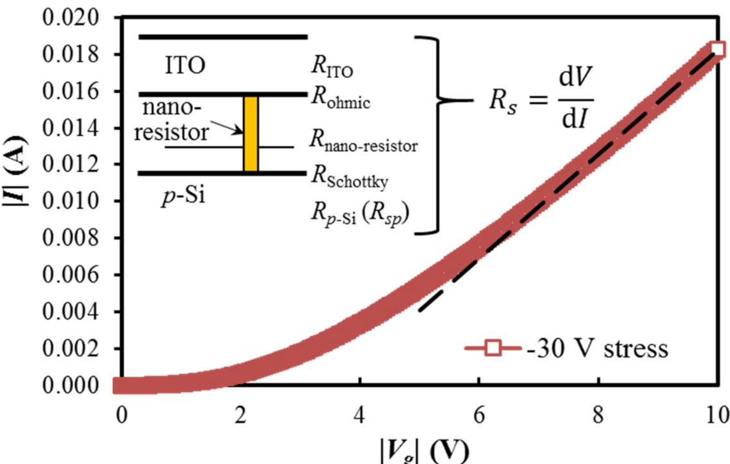

Figure 69. *I-V* curve of a sample after the $V_g = -30$ V, 20 min stress at room temperature.

On the other hand, in the low $|V_g|$ range, the Schottky barrier at the nano-resistor/Si interface is critical to the total resistance of the device. The influence of Schottky barrier on the current flow can be expressed by the following two equations,[163,176]

$$I = \phi A \cdot A^* T^2 \exp\left(\frac{-q\Phi_B}{kT}\right)\exp\left(\frac{q\sqrt{qE_m/4\pi\varepsilon_s}}{kT}\right), \quad [22a]$$

$$E_m = \sqrt{\frac{2qN}{\varepsilon_s}\left(V - IR_s + \Psi_{bi} - \frac{kT}{q}\right)}, \quad [22b]$$

where ϕ is the cross-sectional area ratio of all nano-resistors to the gate, A is the gate area, ε_s is the permittivity of the substrate, Ψ_{bi} is the built-in potential, and N is the accumulated hole density at the nano-resistor/Si interface, which is assumed to be constant. More detail about the Schottky barrier equations and fitting are discussed in Appendix A. Due to the random formation and the tiny size of the nano-resistor,[177,178] it is difficult to measure the

exact cross-sectional area of the nano-resistor. Since each nano-resistor forms a bump, we assume that the cross-sectional area of a nano-resistor is 10% of the cross-sectional area of the bump above it. Figure 70 shows that the experimental data fits the Schottky barrier equation well except at the 0 V. The effective barrier height at the nano-resistor/Si interface estimated from the I vs. (V–IR_s) curve is 0.57 eV. This number is close to the barrier height of the *p*-type Hf-silicide (HfSi) on the Si substrate.[179]

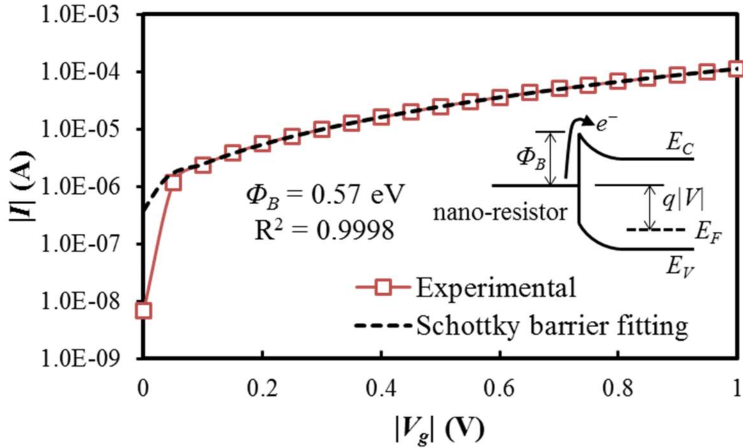

Figure 70. Schottky barrier fitting of the I-V curve of a sample after the V_g = -30 V, 20 min stress from V_g = 0 to −1 V at room temperature.

6.5 Stress Effects on Electrical Properties of Nano-Resistors

To further study the nano-resistor's electrical properties, the effective resistance of the nano-resistors were calculated from I-V curves of samples stressed at V_g = −20 V, −30 V, or −40 V, separately, for 20 min at different temperatures. Figure 71(a) shows the stress

voltage effect on the resistance of the nano-resistors at room temperature. The resistance decreases with the increase of the magnitude of the stress voltage, which can be explained by the increasing number of nano-resistors with the stress voltage. Assuming that the cross-sectional area of a nano-resistor is proportional to the cross-sectional area of the bump above it, the effective resistivity of nano-resistors can be estimated from the measured resistance. For example, the effective resistivities of nano-resistors are 499 Ω·cm, 551 Ω·cm, and 601 Ω·cm for the −20 V, −30 V, and −40 V stress samples, respectively. These numbers are within the range of semiconductor resistivity.[180] Fig. 71(b) shows the temperature dependence of the effective resistance of nano-resistors. In this temperature range, the carrier concentration in the *p*-Si substrate remains constant but the carrier mobility decreases with the increase of temperature.[181] The R_{sp} was calculated using the Klaassen's mobility model.[181,182] In spite of the difference in stress voltages, the effective resistance of nano-resistors increases as the temperature increases from 20 °C to 60 °C. The effective resistivity also follows the same trend of the temperature dependence of the resistivity of metals, silicides, or *p*-Si.[183-185] However, the effective resistance of the nano-resistors drops dramatically when the temperature is increased to 90 °C. Currently, the reason of this phenomenon is not clear. It may be due to the larger number of carriers in the nano-resistors or the dynamic formation of nano-resistors at the high temperature.[186] Therefore, the behavior of the nano-resistor is different from that of a conductor or a semiconductor material. More studies are required to verify the mechanism.

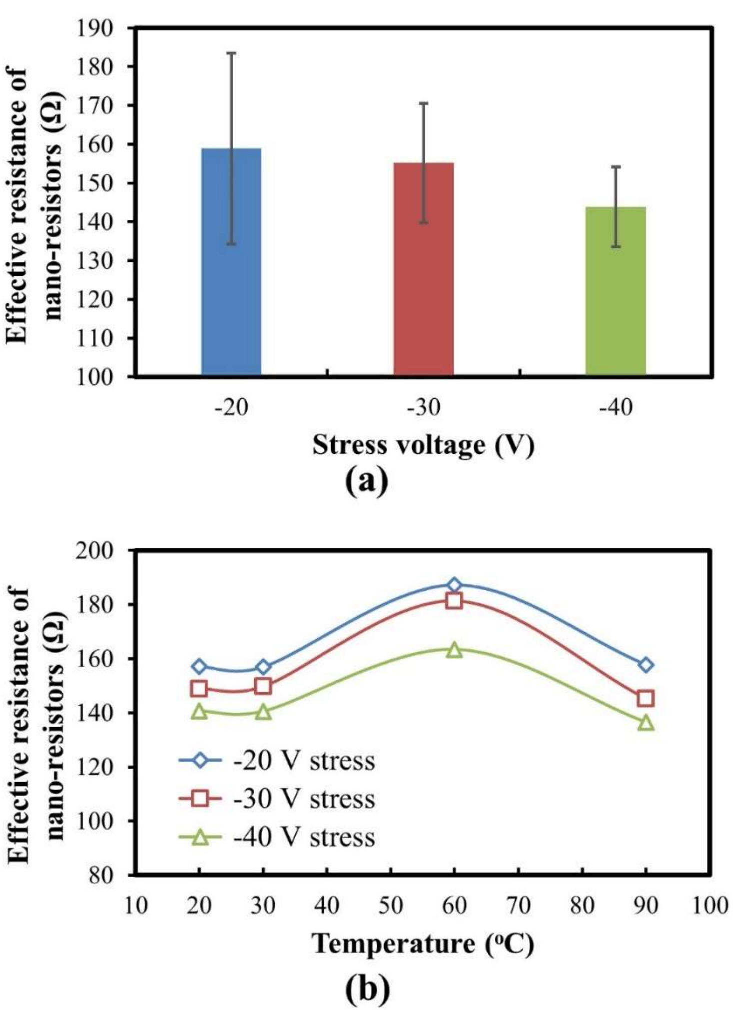

Figure 71. (a) Effective resistances of nano-resistors connected in parallel of samples stressed at $V_g = -20$ V, −30 V, or −40 V, separately, for 20 min at room temperature. (b) Temperature dependence of effective resistances of nano-resistors.

Effective Schottky barrier heights of nano-resistors formed from different stress voltages have been investigated using Equations 22a and 22b. Figure 72(a) shows that the Schottky barrier height decreases with the increase of the magnitude of the stress voltage, i.e., 0.60 eV, 0.58 eV, and 0.56 eV for the −20 V, −30 V, and −40 V stress samples,

respectively. With the increase of the magnitude of stress voltage, the current passing through the nano-resistor increases. The local temperature increases accordingly and more elements from the Si substrate and the ITO electrode can migrate into the nano-resistor.[79,81] The change of the composition of the nano-resistor probably influences the effective Schottky barrier with respect to the Si substrate. Fig. 72(b) shows the temperature dependence of the effective Schottky barriers of nano-resistors formed by different stress voltages. For all samples, the Schottky barrier height increases with the increase of temperature. This phenomenon is in agreement with literature reports on the metal/semiconductor interfaces, which is caused by the spatially inhomogeneous Schottky barriers.[140,187-190] Since the formation of the nano-resistor is random and complicated,[79,177] there exists spatial fluctuations of Schottky barrier heights at the nano-resistor/Si interfaces.[187,188] Since charge transport across the nano-resistor/Si interface is a temperature-activated process, current flowing through the nano-resistor structure prefers to pass the low barrier height site at the low temperature.[187] When the temperature is raised, charges gain enough energy to overcome the difference of the barrier height.[188] On the other hand, the increase of the barrier height with temperature of the sample stressed at −20 V stress is faster than those of samples stressed at −30 V and −40 V. For example, the barrier height of the former increases from 0.60 eV at 20 ºC to 0.71 eV at 90 ºC, while that of the −30 V stress sample increases from 0.58 eV at 20 ºC to 0.62 eV at 90 ºC and that of the −40 V stress sample increases from 0.56 eV at 20 ºC to 0.61 eV at 90 ºC. The fast raise of the barrier height was observed in the O-involved interface.[140,190] The existence of O at the interface can raise the Schottky barrier height, which enhances the

difference between the lower and higher barrier heights with the increase of temperature.[140,190]

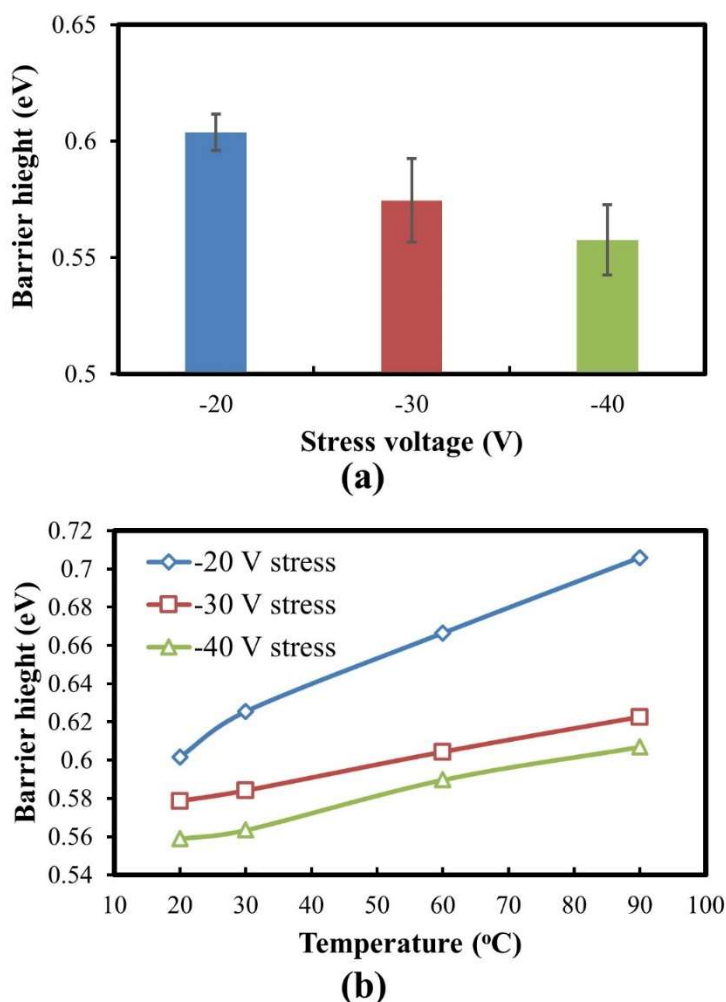

Figure 72. (a) Schottky barrier heights of nano-resistors of samples stressed at $V_g = -20$ V, −30 V, or −40 V, separately, for 20 min at room temperature. (b) Temperature dependence of Schottky barrier heights of nano-resistors.

To further study the nano-resistor's effective Schottky barrier, fresh devices were stressed at $V_g = -20$ V for different periods of time, i.e.., 0 min, 1 min, 20 min, and 60 min, respectively. Then, the *I-V* curves were measured and fitted with Equations 22a and 22b to calculate the effective barrier heights of the nano-resistor. Figure 73 shows the barrier heights of after different stress times. After 0 min stress, the nano-resistor has a large barrier height of 0.8 eV with a large deviation of 0.05 eV. At this stage, the formation of the nano-resistor was in the initial stage. Not all nano-resistors were fully developed. The diffusion of Si from the substrate and the formation of silicide, silicate, and other materials in the nano-resistor was not complete.[79] After 1 min stress, the nano-resistors were fully developed. For example, the same barrier height of 0.65 eV with very small deviations was obtained independent of the stress time. The composition of the nano-resistors did not change with the increase of the stress time.

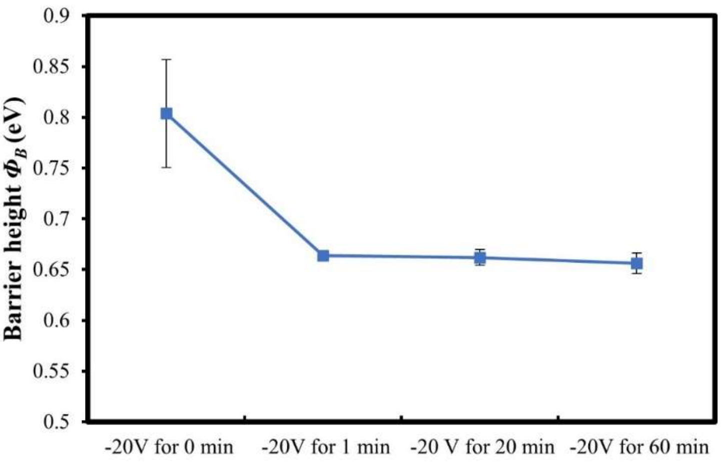

Figure 73. Barrier heights of nano-resistors after being stressed at $V_g = -20$ V for different periods of time.

6.6 Summary

In summary, electrical properties, i.e., the effective resistance and the Schottky barrier height, of nano-resistors formed from the breakdown of MOS capacitors composed of the ZrHfO high-*k* gate dielectric have been studied under different bias voltages and temperatures. A large number of bumps each of which corresponded to a nano-resistor in the high-*k* film were observed. The total number and cross-sectional area of the nano-resistors increased with the increase of stress voltage. The effective resistance of the nano-resistors was estimated by neglecting small resistances and deducting the Si substrate resistance from the total resistance. The change of the effective resistance of the nano-resistors with the temperature was different from that of a conductor or a semiconductor. In the low voltage range, the current through the nano-resistors was controlled by the Schottky barrier. The effective barrier height increased with the increase of the stress voltage that changed the nano-resistor composition. Moreover, the increase of the barrier height with the increase of temperature was observed, which could be attributed to the barrier inhomogeneity among nano-resistors. Furthermore, the stress time effect on the effective barrier height showed that nano-resistors were fully formed with stable electrical properties after the 1 min stress at $V_g = -20$ V. The effective resistance and Schottky barrier height of the nano-resistors are important parameters for the application of this kind device in many electronic and optoelectronic applications.

CHAPTER VII

LIGHT EMISSION ENHANCEMENT ON SOLID STATE INCANDESCENT LIGHT EMITTING DEVICES*

7.1 Introduction and Motivation

Since the SSI-LED emits light from the thermal excitation of nano-resistors formed in the high-*k* gate dielectric thin film, the composition and structure can affect the light emission characteristics of the device.[73-80] The embedding of the nc-CdSe layer in the ZrHfO thin film greatly increased the light emission intensity.[79] Moreover, the WO_x gate dielectric SSI-LED showed excellent light emission performance.[78] Therefore, in this chapter, the WO_x layer was embedded into the ZrHfO gate dielectric to investigate the light emission enhancements. On the other hand, as the discussed in last chapter, the Si substrate had the spreading resistance comparable to the effective resistance of all nano-resistors. During the light emission process, more than half of the voltage would be taken by the Si substrate. Thus, using a heavily doped Si substrate to fabricate the SSI-LED and reduce the power dissipation in Si substrate can be another potential method to increase the light emission intensity and efficiency.

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7.2 WO_x Embedded Zr-Doped HfO_2 High-*K* SSI-LEDs

7.2.1 Experimental

The device has a MOS capacitor structure that contains a ZrHfO (bottom oxide)/WO_x/ZrHfO (top oxide) tri-layer stack gate dielectric deposited on a DHF cleaned *p*-type <100> Si wafer. The tri-layer stack was sputter deposited sequentially in three steps in one pumpdown process without breaking the vacuum. The ZrHfO layers were deposited from the Zr/Hf composite target in Ar/O_2 (1:1) at 60 W and 5 mTorr, i.e., 2 min for the bottom oxide and 10 min for the top oxide, separately. The WO_x layer was deposited from a W target in Ar/O_2 (1:1) at 60 W and 5 mTorr for 3 min. The control sample, i.e., containing the 12-min deposited ZrHfO gate dielectric film without the embedded WO_x layer, was prepared for the comparison purpose. After the high-*k* stack deposition, the sample was annealed at 800 ºC for 3 min in N_2 by the RTA. The 80 nm thick ITO film was deposited on top of the high-*k* stack and wet etched into 300 µm diameter dots as the gate electrodes. The backside of the wafer was deposited with an Al film to form the ohmic contact. The complete sample was annealed at 400 ºC in H_2/N_2 (1:9) for 5 min.

7.2.2 Increased Light Emission Intensities and CRI

Figure 74 shows the *I-V* curves of the control and WO_x embedded samples with the V_g swept from 0 to −20 V. The abrupt breakdown of the dielectric film occurs at −6.1 V for the control sample and −7.9 V for the WO_x embedded sample. The latter has a larger $|V_{BD}|$ than the former probably due to the thicker film.[162] The EOT of the WO_x embedded sample is 7.36 nm and that of the control sample is 6.30 nm. On the other

hand, the breakdown strength of the high-*k* stack can be related to the defect density in the original film.[78] The Q_{ot} of the WO_x embedded sample is much higher than that of the control sample, i.e., 5.51×10^{10} cm^{-2} vs. 4.91×10^{9} cm^{-2}, which favors the easier breakdown of the former. Since the WO_x embedded sample has a larger $|V_{BD}|$ than that of the control sample, the defect density is less important than the film thickness in this case. After the dielectric breakdown, the leakage current increases almost linearly with the increase of $|V_g|$, i.e., following the Ohm's law. Therefore, the leakage path functions like a resistor, which can be thermally excited to emit light upon the passage of a large current. The average resistance of the WO_x embedded sample in the light emission region is smaller than that of the control sample, i.e., 5093 Ω vs. 28585 Ω, which is probably due to the inclusion of W in the leakage path.

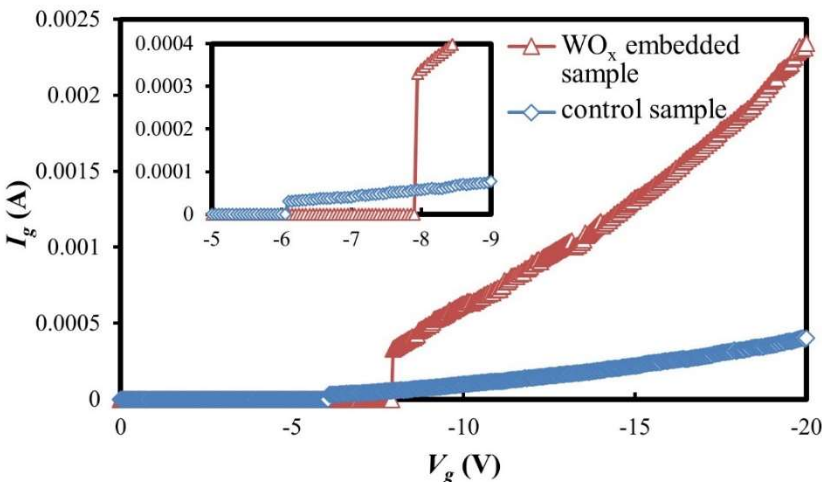

Figure 74. *I-V* curves of the control and WO_x embedded samples with V_g from 0 to −20 V.

Figure 75 shows the high magnification photos of the (a) control and (b) WO_x embedded samples stressed with the same V_g of −60 V. The dark region in the photo is from the light blocking of the probe needle. For both samples, the light is emitted from many discrete nano dots evenly distributed across the gate electrode. This is different from the uniform light emission from the semiconductor based LED. In the conventional LED, light is emitted from the electron-hole or exciton-exciton recombination. In the SSI-LED, light is emitted from the thermal excitation of the nano size conductive paths surrounded by the dielectric film during the passage of a large current.[73-80] The excitation efficiency is related to the size, e.g., the cross-sectional area and the length, and the composing material of the conductive path.[77,78] Each bright dot in the figure corresponds to one excited conductive path. The control sample in Fig. 75(a) appears to contain more bright dots than the WO_x embedded sample in Fig. 75(b) does. The size of the bright dot in the latter is larger than that in the former. The light pattern in the WO_x embedded sample is similar to that of the SSI-LED with the WO_x gate dielectric.[78]

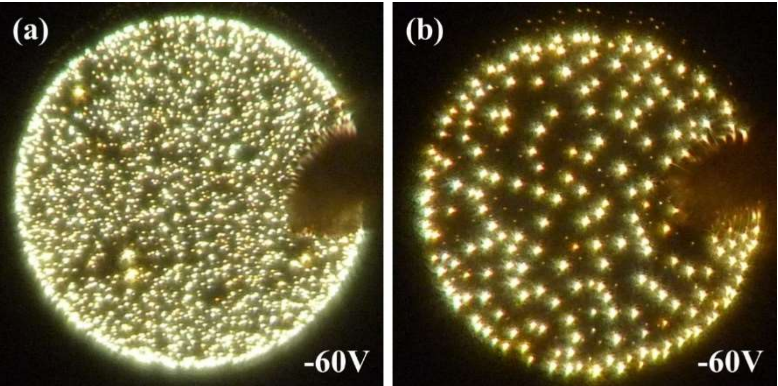

Figure 75. High-magnification photos of the (a) control and (b) WO_x embedded samples stressed at $V_g = -60$ V.

Figure 76 shows the emission spectra of the control and WO_x embedded samples at $V_g = -60$ V. Both samples emit broad band lights covering the whole visible and part of the near IR wavelengths. Therefore, the principle of light emission of the SSI-LED is different from that of the conventional LED. In the above 550 nm region, the light emitted from the WO_x embedded sample is stronger that of the control sample. For example, the intensity at 700 nm of the WO_x embedded sample is about 1.5 times that of the control sample. However, the latter has a slightly higher intensity below 550 nm, i.e., in the UV to green range. Consequently, the light emitted from the control sample appears to be whiter than that of the WO_x embedded sample, as shown in Fig. 75. The emission spectrum difference is probably related to the composition difference, e.g., with or without the W component, of the conductive paths in the two samples.

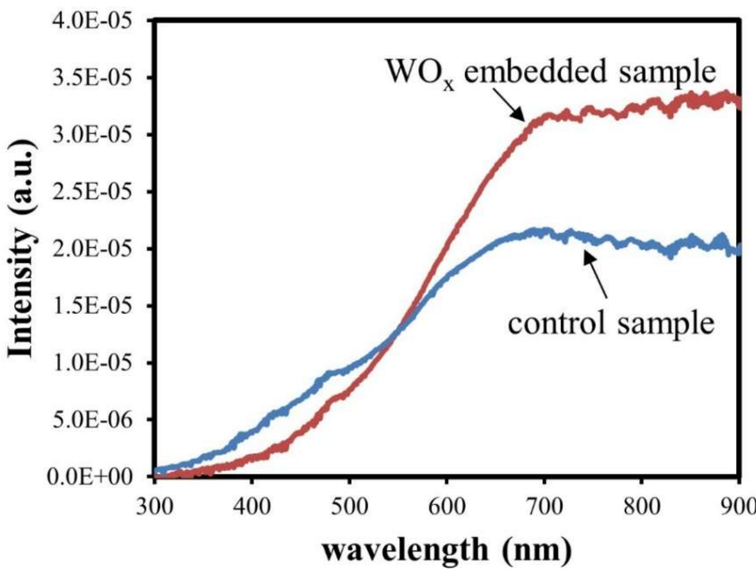

Figure 76. Emission spectra of the control and WO_x embedded samples at $V_g = -60$ V.

Figure 77 shows the emission spectra of the control and WO_x embedded samples stressed at $V_g = -20$, -40, and -60 V, respectively. The light intensity increases with the increase of $|V_g|$, which corresponds to the increase of the leakage current. A larger leakage current can induce more heat in the conductive path to emit stronger light. Separately, when the $|V_g|$ increases, the peak wavelength (λ_{peak}) of the control sample shifts to the blue direction, i.e., from 736.5 nm at −20 V to 735 nm at −40 V to 689.5 nm at −60 V. However, the λ_{peak} of the WO_x embedded sample shifts to the opposite direction from 815.5 nm at −20 V to 817 nm at −40 V to 886.5 nm at −60 V, which is similar to that of the WO_x SSI-LED.[77] This is another indication that the conductive path of the WO_x embedded sample may contain W. It was reported that ZrO_2 and HfO_2 can dissolve WO_3 at around 1400 K.[191] During the light emission process, the embedded WO_x film can be dissolved into the

conductive paths at the high local temperature due to the Joule heating from the large leakage current, which modifies the composition of the conductive paths and causes the above phenomenon.

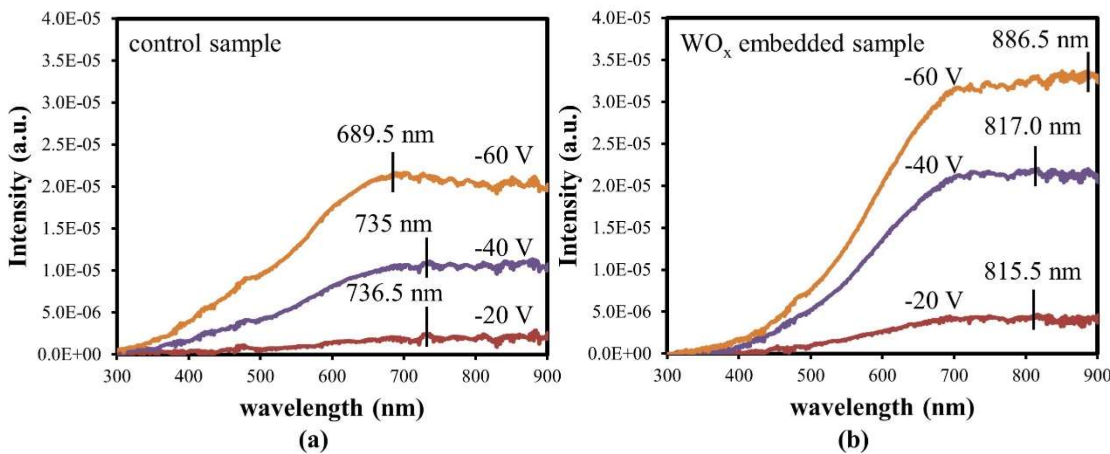

Figure 77. Emission spectra of the (a) control and (b) WO_x embedded samples stressed at $V_g = -20$, -40, and -60 V.

Based on the spectra in Fig. 77, the CIE coordinates, CCT's, and CRI's of the control and WO_x embedded samples were calculated and listed in Table 4. For the control sample, the CCT increases with the increase of the $|V_g|$. This is contributed by the blue shift of the spectrum, which is consistent with the decrease of the λ_{peak} number in Fig. 76(a). The similar trend of the CCT change has been observed previously.[78] Additionally, the CRI R_a increases as the $|V_g|$ increases, which is contributed by the reduction of the CIE coordinate distance to the Planckian locus.[78] All above results indicate that when the $|V_g|$

is increased, the characteristics of the light emission move toward those of the blackbody emission light. On the other hand, the WO_x embedded LED shows different trends on $|V_g|$ effects on the CCT and R_a. When the $|V_g|$ increases, the WO_x embedded sample emits much stronger light in the red/IR range but the blue/green portion increases very slightly. The red shift of the spectrum of the WO_x embedded sample corresponds to the decrease of the CCT.[77] At the same time, the CIE coordinate distance to the Planckian locus increases, which leads to the slight decrease of the R_a. At each $|V_g|$, the WO_x embedded sample has a large CRI of > 98, which is close to that of the blackbody emission light. Furthermore, the WO_x embedded LED has a large CRI R_9 number of around 97 in the V_g range, which corresponds to the color rendering of the deep-red region. The large R_9 value this kind of device makes it adequate for the biomedical and painting appreciation applications.[104]

Table 4. CIE color coordinates, CCT, and CRI values for the control and WO_x embedded samples at $V_g = -20$, -40, and -60 V.

Sample	V_g (V)	CIE x	CIE y	CCT (K)	CRI R_a	CRI R_9
control sample	−20	0.4217	0.3706	2980	87.3	75.0
	−40	0.4227	0.3836	3081	96.5	94.2
	−60	0.4174	0.3840	3187	97.0	96.0
WO_x embedded sample	−20	0.4701	0.4172	2612	98.8	98.0
	−40	0.4687	0.4100	2576	98.5	96.7
	−60	0.4698	0.4087	2552	98.4	97.0

7.3 SSI-LEDs Fabricated on Heavily-Doped *p*-Si Substrates

7.3.1 Experimental

The ZrHfO dielectric MOS SSI-LED was fabricated on a dilute HF cleaned *p*-type <100> Si wafer in a one pumpdown process without breaking the vacuum. Si wafers of two different dopant concentrations, i.e., *p* (~10^{15} cm^{-3}) and p^+ (~10^{17} cm^{-3}), were used. The ZrHfO film was sputtered from the Zr/Hf target in Ar/O_2 (1:1) at 5 mTorr and 60 W for 12 min. Then, samples were annealed at 800 ºC for 3 min in N_2 using the RTA equipment. After that, an 80 nm thick ITO film was deposited on top of the ZrHfO film and wet etched into 300 µm diameter dots as gate electrodes. An Al film was deposited on the backside of the wafer to form ohmic contact. The complete sample was annealed at 400 ºC in H_2/N_2 (1:9) for 5 min.

7.3.2 Enhanced Light Emission Intensities and Efficiencies

Figure 78 shows *C-V* hysteresis curves of the samples deposited on the *p* and p^+ substrates (the *p* and p^+ substrate samples) that were measured with the V_g swept from −2 V to +1 V and then back to −2 V at 1 MHz. The *p* substrate sample shows a negligible small hysteresis window, but the p^+ substrate sample has a large window of 0.16 V. Moreover, the forward curve of the p^+ substrate sample shifts toward the negative V_g direction by 1.01 V. The V_{FB} of a MOS capacitor can be determined by the following equation,

$$V_{FB} = \phi_{MS} - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}}, \qquad [23]$$

where ϕ_{MS} is the work function difference between the metal gate and the Si substrate, Q_f is the fixed charge density, Q_m is the mobile ionic density, and C_{ox} is the capacitance of the oxide dielectric.[126] For both samples, the ϕ_{MS} difference due to the dopant concentration is only 0.12 V from Ref. 147. Therefore, the negative V_g shift and the large hysteresis window of the p^+ substrate sample are contributed by the large defect density in the high-k stack. This was caused by the defect generation from the excess Boron diffusion from the heavily doped substrate to the high-k stack.[192,193] Accordingly, the Q_{ot} and D_{it} of the p^+ substrate sample are larger than those of the p substrate sample, i.e., 6.31×10^{11} cm^{-2} and 1.56×10^{11} cm$^{-2}\cdot$eV^{-1} vs. 2.05×10^{10} cm^{-2} and 1.02×10^{11} cm$^{-2}\cdot$eV^{-1}. The sample deposited on the heavily doped substrate has a worse interface and a larger density of defects in the high-k stack.

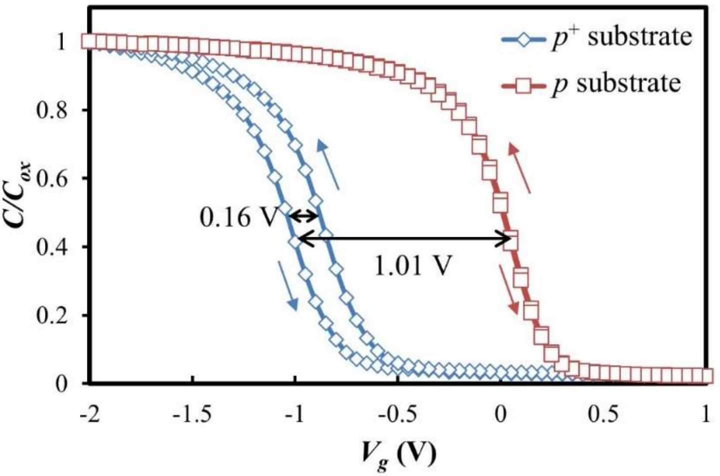

Figure 78. C-V hysteresis of the p and p^+ substrate samples with V_g swept from −2 to +1 to −2 V at 1 MHz.

Figure 79 shows *I-V* curves of the *p* and p^+ substrate samples with V_g swept from 0 to −10 V. The abrupt breakdown of the high-*k* stack occurs at −5.5 V for the *p* substrate sample and −4 V for the p^+ substrate sample. Since the p^+ substrate sample has a larger defect density than that of the *p* substrate sample, the former's high-*k* stack is easier to be broken down.[162] Moreover, the heavily doped substrate of the p^+ substrate sample can offer more holes to inject into the high-*k* stack, which accelerate the breakdown process of the high-*k* stack.[194] The similar phenomenon was observed in Ref. 195. After breakdown, leakage currents of both samples increase almost linearly with the increase of $|V_g|$. At the same $|V_g|$, the p^+ substrate sample has a larger leakage current than the *p* substrate does. This is because the former is easier to breakdown the high-*k* dielectric and there are more conductive paths formed through the high-*k* stack to conduct current.

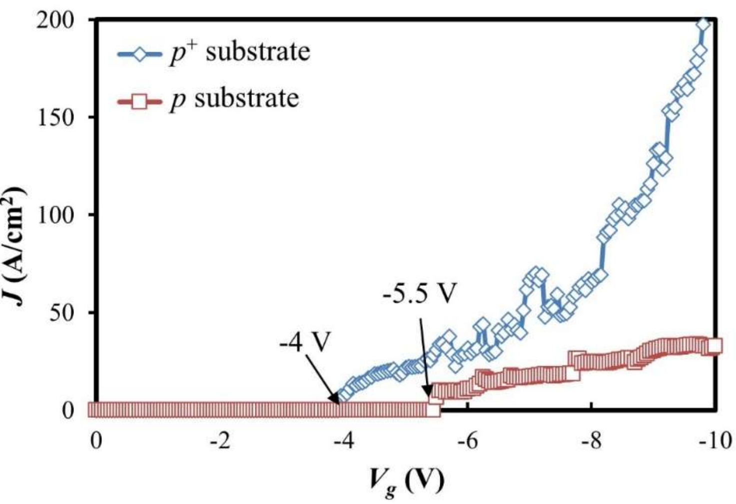

Figure 79. *I-V* curves of the *p* and p^+ substrate samples with V_g swept from 0 V to −10 V.

Figure 80 shows high magnification photos of the p and p^+ substrate SSI-LEDs stressed at $V_g = -25$ V. For both samples, the lights are emitted from many tiny, discrete, evenly spread bright dots. This discrete-dot light pattern is different from the uniform light emission from the conventional semiconductor based LED. The light emission principle of the SSI-LED is the thermal excitation of nano-size conductive paths during the passage of a large current.[73-80] Each dot corresponds to a conductive path, i.e., a nano-resistor that is emitting light. The p^+ substrate SSI-LED contains many more dots than the p substrate SSI-LED does. In the former, the bright dots are almost distributed everywhere across the ITO gate. This is because the breakdown strength of the dielectric decreases markedly with the increase of the doping concentration in the substrate.[194,195] Therefore, at the same V_g, the p^+ substrate forms more conductive paths than the p substrate does. Then, the light emission photo of the former in fig. 80(b) looks brighter than that of the latter in Fig. 80(a).

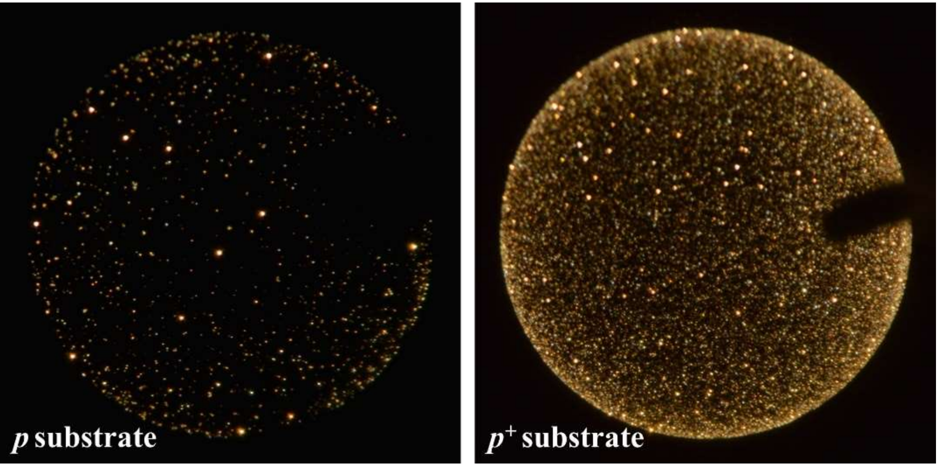

Figure 80. High-magnification photos of the p and p^+ substrate SSI-LEDs at $V_g = -25$ V.

Figure 81(a) shows the emission spectra of the p and p^+ substrate SSI-LEDs at $V_g =$ −25V. Both spectra cover the same broad range from the whole visible to the near IR wavelengths. The p^+ substrate SSI-LED has a much higher light intensity than the p substrate SSI-LED does, which is consistent with the observation of Fig. 80. This is due to the larger leakage current and the more formed nano-resistors in the former. Furthermore, these spectra are also normalized by the maximum intensity at the peak, as shown in Fig. 81(b). The normalized spectra of both devices almost overlap with each other all over the wavelength range. The peak wavelengths of both devices are very close, i.e., 707 nm for the p^+ substrate SSI-LED and 700 nm for the p substrate SSI-LED.

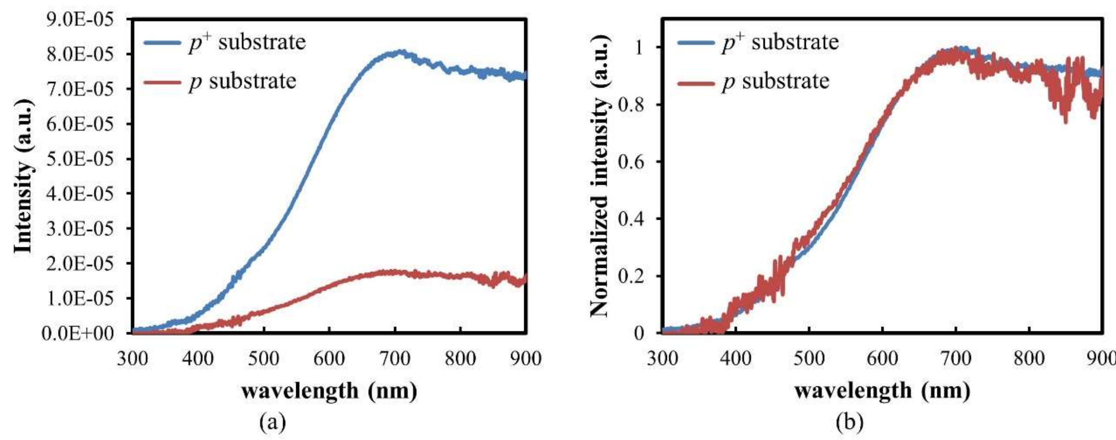

Figure 81. (a) Light emission spectra and (b) normalized spectra of the p and p^+ substrate SSI-LEDs at $V_g = -25$ V. (b) Normalized by the maximum intensity at the peak.

To further compare their light color, the CIE coordinates, CCT's, and CRI's of

both SSI-LEDs were calculated and listed in Table 5. The p^+ substrate SSI-LED has a lightly smaller CCT than the *p* substrate SSI-LED does, i.e., 3704 K vs. 2851 K. This is because, as shown in Fig. 81(b), the light emitted from the former shows slightly smaller blue/green portion but somewhat larger red/IR portion than that of the latter. The CIE coordinates of both SSI-LEDs are near the Planckian locus. For example, the CRI R_a values are 98.7 for the *p* substrate SSI-LED and 98.2 for the p^+ substrate SSI-LED. These values are close to that of the black body emission of the incandescent light bulb.[77] This indicates the similar light emission principles of the SSI-LED and the light bulb.

Table 5. CIE color coordinates, CCT, and CRI values of the *p* and p^+ substrate SSI-LEDs at $V_g = -25$ V.

Substrate	CIE x	CIE y	CCT (K)	CRI R_a
p	0.4487	0.4091	2851	98.7
p^+	0.4569	0.4059	2704	98.2

Due to the lack of the adequate measurement equipment and the small size of the SSI-LED, i.e., 300 µm, the accurate *EQE*'s were not available. The relative *EQE*'s of both device were roughly estimated with the assumption of the isotopic light emission hemisphere, as shown in figure 82. From $V_g = -10$ V to -25 V, the *EQE*'s of the p^+ substrate SSI-LED are consistently higher than those of the *p* substrate SSI-LED. This result can explain the higher light emitting intensity of the former in Fig. 81(a). For both devices, the light emission efficiency increases with the increase of $|V_g|$ but the p^+ substrate SSI-LED's efficiency rises slower. However, the cause of the efficiency difference is

related to compositions, sizes, and distributions of conductive paths in these devices, which need further studies.

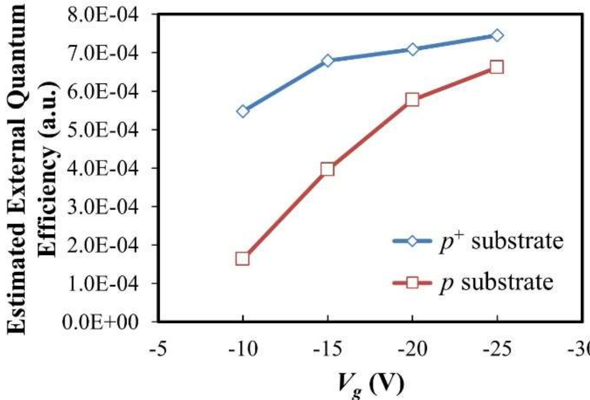

Figure 82. Estimated *EQE*'s of the p and p^+ substrate SSI-LEDs at $V_g = -10$ to -25 V.

7.4 Summary

In this chapter, the enhancement of white light emission from ZrHfO-based SSI-LEDs were investigated. The first method was to insert a WO_x layer into the ZrHfO high-*k* dielectric MOS capacitor. The embedding of the WO_x layer in the gate dielectric caused the increase of the breakdown voltage and the inclusion of W in the conductive path. The light emission spectrum, e.g., strong component in the red to IR region, and the dependence of the intensity on the leakage current all indicate the important influence of the existence of W in the dielectric film. The optical characteristics of the WO_x embedded sample are close to those of the incandescent light. All in all, the embedding of the

WO_x layer increases the device's light emission intensity and shifts the light spectrum toward the short wavelength direction, i.e., warmer light emission. On the other hand, the SSI-LED made of the amorphous ZrHfO dielectric on the heavily doped *p*-type Si substrate was fabricated to investigate the electrical and light emission characteristics. The excess boron diffusion from the heavily doped substrate could generate a lot of defects in the high-*k* stack, which caused a larger hysteresis window, a negative V_g shift of the *C*-*V* curve, and a degraded breakdown strength. Due to the easier breakdown, the p^+ substrate sample had more conductive paths, i.e., nano-resistors, to conduct current and emit light. Therefore, the p^+ substrate SSI-LED had more bright dots and higher light emission intensity than the *p* substrate SSI-LED did. The doping concentration of the substrate had little effect on the shape of the emission spectrum. Both SSI-LEDs had close light color characteristics. The p^+ substrate SSI-LED had a better light emission efficiency. In summary, the substrate doping concentration influences the dielectric properties and breakdown strength of the original MOS capacitor, which enhances the light emission intensities and efficiencies of nano-resistors.

CHAPTER VIII

EXTENSIVE APPLICATIONS OF NANO-RESISTOR DEVICES*

8.1 Introduction and Motivation

In addition to the white light emission for lighting, the unique properties of nano-resistors make this new kind of device potentially applicable in many fields.[76,186] For example, this kind of device is a potential Si-based light source for on-chip optical interconnects. However, narrow band light around 850-980 nm is preferred because the Si photodiode has the maximum optical responsivity in this range.[76,196] One way to achieve the narrow band light is to apply a thin optical filter above the SSI-LED or nano-resistor device. The *a*-Si:H and SiN_x films have been widely employed in the Si-based IC devices. The former has a strong absorption in the below 600 nm wavelength range.[197] The latter absorbs the UV light. Its refractive index can be varied by changing the deposition condition.[198] Since both *a*-Si:H and SiN_x thin films can be easily deposited by the low-temperature PECVD method, they are potentially suitable optical filter materials for the SSI-LED light. On the other hand, the nano-resistor device shows the diode-like *I-V* characteristics that only allow the current to flow from the substrate to the gate.[199] In addition, this new device can function as an anti-fuse one-time-programmed NVM, which has a 8-order-high current ratio of the "programmed" state to the "unprogrammed"

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state.[199,200] In this chapter, the author investigated the light filtration of the nano-resistor device using the *a*-Si:H and SiNx thin films as well as the thickness and size effects on the application as a diode-like anti-fuse device.

8.2 Light Filtration on SSI-LEDs

8.2.1 Experimental

Figure 83 shows the structure of a SSI-LED with an *a*-Si:H or SiN_x thin film filter. The top ITO gate electrode is connected with a Mo/Al line extended to the edge of the substrate for the easy application of the driving voltage. First, a 200 nm thick SiN_x insulating layer was deposited on a *p*-type (10^{15} cm^{-3}) <100> Si wafer using a parallel plate PECVD reactor (Applied Material, AMP Plasma I) equipped with a 50 kHz RF power generator with the feed gas of $SiH_4/NH_3/N_2$ (20/80/600 sccm) at 500 mTorr, 300 W, and 260ºC. Then, the film was wet-etched with a DHF solution into 250 µm diameter holes to define the light emitting area. Second, a 10 nm thick ZrHfO film was sputter-deposited on the substrate using a Zr/Hf (12/88 wt. %) target in Ar/O_2 (1:1) at 5 mTorr and 60 W. Third, an 80 nm thick ITO film was deposited on top of the ZrHfO film and wet etched into gate electrodes through a lithography defined pattern. Fourth, the Mo (200 nm) and Al (120 nm) films were sequentially deposited on the substrate and etched into lines to connect the ITO electrodes to contact pads. Fifth, a 100 nm thick Mo film was deposited on the wafer backside to form the ohmic contact. Sixth, the sample was treated with a PMA step at 250 ºC in H_2/N_2 (10/90) for 5 min. The SSI-LED was complete after the dielectric breakdown process, which was done by applying a negative V_g larger than

the V_{BD}.[73-80] Subsequently, a PECVD *a*-Si:H or SiN_x film was deposited on top of the SSI-LED as an optical filter. The 6.5 nm thick *a*-Si:H film was deposited using SiH_4/H_2 (50/200 sccm) at 500 mTorr and 500 W. Three different types of SiN_x films, i.e., SiN_x-300, SiN_x-400, and SiN_x-500, with corresponding thicknesses of 170 nm, 163 nm, and 161 nm, respectively, were deposited using SiH_4 (20 sccm) /NH_3 (80 sccm) /N_2 (300, 400 or 500 sccm) at 500 mTorr and 300 W. The light emitted from the SSI-LED with or without the thin film filter layer was measured using an OES at $V_g = -30$ V. Separately, individual *a*-Si:H and SiN_x films were deposited on a Corning 1737 glass to measure the light transmittance.

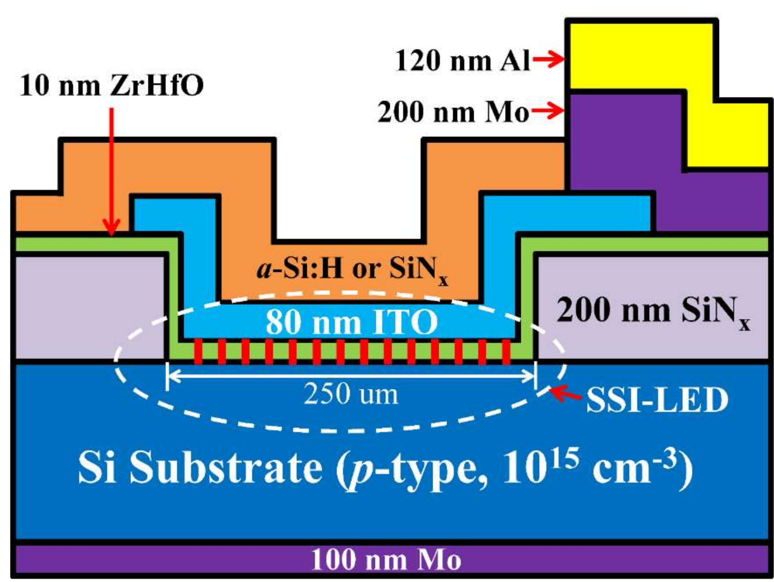

Figure 83. Cross-sectional view of a ZrHfO SSI-LED with a coated thin film of *a*-Si:H or SiN_x.

8.2.2 Light Filtration of a-Si:H and SiN_x Thin Films

Figure 84 shows normalized spectra of lights emitted from SSI-LEDs with and without a coated *a*-Si:H thin film. Without the *a*-Si:H film, the light emitted from the SSI-LED covers a broad range of wavelengths spanning from 450 nm to 950 nm with a peak located at around 700 nm, which is similar to that reported previously on the same kind of SSI-LED.[73-80] However, for the *a*-Si:H coated sample, the light below the 530 nm wavelength disappears and the peak of the spectrum is located at 810.5 nm. The inset shows the transmittance spectrum of an *a*-Si:H film in the wavelength range of 450 nm to 950 nm. The *a*-Si:H film has a lower transmittance which increases monotonically from 31% at 450 nm to 80% at 700 nm and 91% at 950 nm. The strong absorption of light in the short wavelength range is consistent with literature reports.[197,201] Therefore, the shift of the peak location in Fig. 84 is due to the strong absorption of the short wavelength portion of the SSI-LED emitted light by the coated *a*-Si:H film.

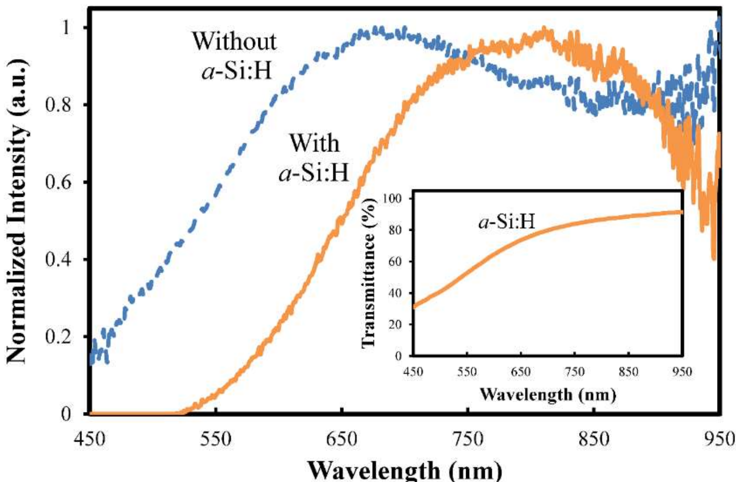

Figure 84. Normalized light emission spectra of SSI-LEDs with and without a coated *a*-Si:H thin film. Stressed at $V_g = -30$ V. Inset: Light spectral transmittances of the coated *a*-Si:H film.

Figure 85 shows normalized spectra of lights emitted from SSI-LEDs with and without being coated with individual SiN_x thin films. For all SiN_x coated samples, the intensity of the light in below 550 nm or above 750 nm drops drastically. At the same time, the peak shifts toward the short wavelength direction with the increase of the N_2 flow rate in the SiN_x deposition process, i.e., from 694 nm in the uncoated sample to 682 nm in the SiN_x-300 sample, 675 nm in the SiN_x-400 sample, and 665 nm in the SiN_x-500 sample. The change of the spectrum is consistent with the light transmittance of the SiN_x film, as shown in the inset. The SiN_x films have low light transmittance below 550 nm and above 750 nm. The transmittance peaks are located at 669.5 nm for the SiN_x-300 film, 617 nm for the SiN_x-400 film, and 596 nm for the SiN_x-500 film, which are in the same order as peaks in lights emitted from the coated SST-LEDs. The light transmittances of all SiN_x

films are high, i.e., >80% in the whole wavelength range. When a light is incident on a thin film, it is reflected at two interfaces, i.e., at the top and bottom contacts with the adjacent media.[201] At a specific wavelength, when the two reflected lights are in same phase, the reflected light is maximized and the transmitted light is minimized. However, when the two reflected lights shift by half wavelength, the transmitted light is maximized. The constructive and destructive interference phenomena can cause multiple transmittance maxima and minima, as shown in the following equation, [198]

$$2nt = m\lambda \, , \quad [24]$$

where n is the refractive index of the SiN_x film, t is the film thickness, λ is the light wavelength, m is the interference order that is an integer or a half-integer.[201] Therefore, this interference phenomenon is affected by the film's thickness and refractive index. The SiN_x thin films in Fig. 85 are N-rich and have refractive indices of 1.8-2.0.[202] Their thicknesses are around 160-170 nm. Since the left side of Equation 24 is estimated to be approximately 576-680 nm, the m value for those peaks in Fig. 85 should be 1. Refractive indices of SiN_x samples calculated from Eqn. 24 are: 1.969 for the SiN_x-300 sample, 1.893 for the SiN_x-400 sample, and 1.851 for the SiN_x-500 sample, which are consistent with those reported in the literature.[202] In the PECVD process, with the increase of N_2 gas in the feed gas, the N content, e.g., in the NH or NH_2 form, is increased and the Si content, e.g., in the SiH or SIH_2 form, is reduced.[203,204] Accordingly, the refractive index of a SiN_x film decreases with the increase of the N_2 concentration in the feed stream.[205,206] Therefore, the SiN_x film's refractive index can be adjusted by the deposition condition to obtain the maximum light transmittance at a specific wavelength.

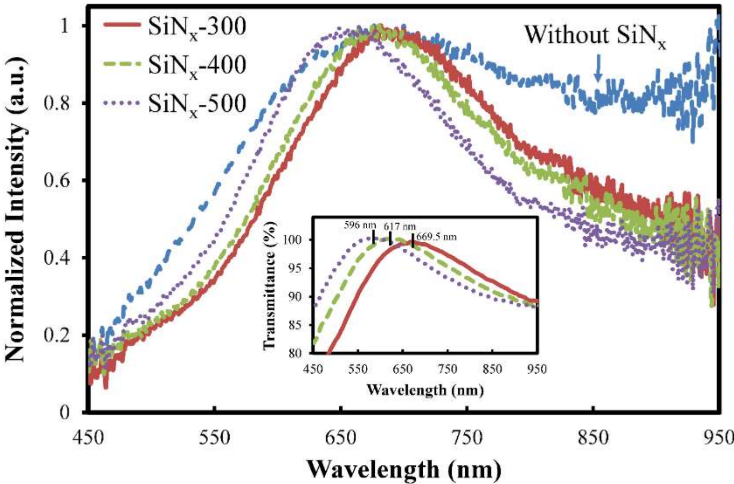

Figure 85. Normalized light emission spectra of SSI-LEDs with and without being coated with three types of SiN_x thin films. Stressed at $V_g = -30$ V. Inset: Light spectral transmittances of the coated SiN_x films.

8.2.3 Fabry-Perot Filters for Solid State Incandescent Light Emitting Devices

According to the Fabry-Perot interference effect,[207-209] a multilayer stack of high- and low-refractive index thin films can be used as an optical filter to narrow down the broad band light to a specific wavelength. It is usually composed of two Bragg reflector stacks of alternating high-refractive index (H) and high-refractive index (L) layers with quarter-wavelength optical thickness at the desired wavelength (λ_0). The two stacks are separated by a thin spacer layer of dielectric material with a half-wavelength optical thickness.[207-209] For example, Figure 86 shows that the broadband light emitted from the ZrHfO SSI-LED can be transformed into a major narrow peak at 850 nm with a full width

at half maximum (FWHM) of ~8 nm and a minor peak at 650 nm using a nine-layer structure of $(HL)^2HH(LH)^2$ where H is a-Si:H (52.0 nm thick) and L is SiN_x (105.9 nm thick). The latter peak can be greatly suppressed by the absorption of *a*-Si:H films.[197,208] The narrow band spectrum in Fig. 86 was calculated based on the recursive matrix derived from Maxwell's equations for a multilayer dielectric structure.[210] Detailed data sets of refractive indices and extinction coefficients of *a*-Si:H and SiN_x over the 300-1000 nm wavelength range were used in the calculation.[211] The multilayer *a*-Si:H/SiN_x stack has a high transmittance peak of 95% at 850 nm and a small transmittance of 12.2% at 650 nm. The bandwidth of the major peak in Fig. 85 could be further narrowed down when more pairs of alternating H and L layers were used.[209]

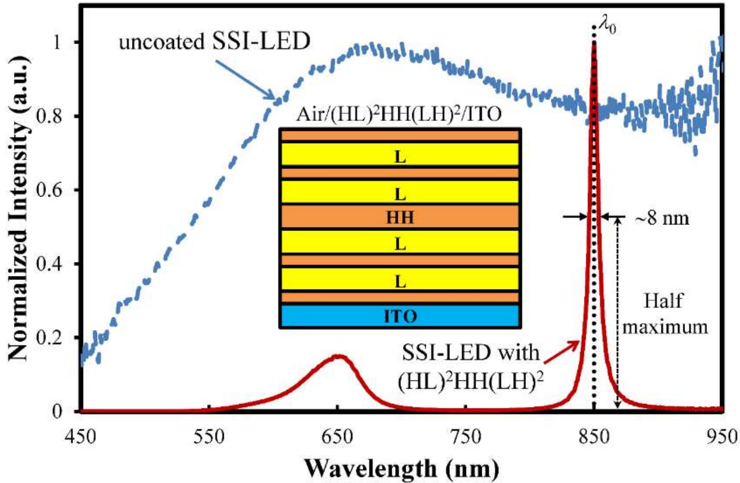

Figure 86. Calculated light emission spectra of SSI-LEDs with and without being coated with a $(HL)^2HH(LH)^2$ Fabry-Perot filter. Normalized by the maximum intensities. λ_0 = 850 nm. H: 52.0 nm thick *a*-Si:H. L: 105.9 nm thick SiN_x. Inset: cross-sectional view of the $(HL)^2HH(LH)^2$ filter on SSI-LED.

8.3 Diode-Like Anti-Fuse Application

8.3.1 Experimental

MOS capacitors composed of ZrHfO high-*k* dielectric films of different thickness were fabricated on DHF cleaned *p*-type (10^{15} cm^{-3}) <100> Si wafers. The ZrHfO film was sputter-deposited from the Zr/Hf target in Ar/O_2 (1:1) atmosphere at 5 mTorr and 60 W for 3, 6, 12, 20, 40, or 60 min, respectively. Subsequently, the sample was processed with a PDA step at 800 °C for 3 min under the N_2 or O_2 atmosphere using the RTA equipment. A $HfSiO_x$ interface layer was formed between the amorphous bulk ZrHfO layer and the Si substrate, which was confirmed from the ESCA and the HRTEM.[30,116] Then, an 80 nm thick ITO film was deposited on top of the ZrHfO film and wet-etched into 50, 100, 150, 200, 250, 300, 350, or 400 μm diameter gate electrodes, respectively. An Al film was deposited on the backside of the wafer to form the ohmic contact. The complete sample was annealed at 400 °C under H_2/N_2 (1:9) atmosphere for 5 min. The sample's electrical properties were extracted from the *C-V* and *J-V* measurements. To program the device, the capacitor was applied with a V_g larger than the V_{BD} to form conductive paths. The 4-channel digital oscilloscope (Seeed Studio, DSO Quad v2.6) was used to monitor the voltage over the capacitor driven by the pulsed voltage.

8.3.2 Diode-Like I-V and Anti-Fuse Functions

Figure 87 shows the diode-like *I-V* curve of the 12-min-deposited ZrHfO MOS capacitor with the anti-fuse function. Before the dielectric breakdown, the leakage current

follows the SE equation at the low voltage and the P-F relation at the high voltage in the $-V_g$ range.[113] At certain voltage, e.g., –5.05 V, the spot-connected paths, i.e., conductive paths or nano-resistors, are formed through the high-*k* stack and the gate dielectric breakdown happen.[95] The magnitude of the leakage current jumps several orders. At the same $-V_g$, the post-breakdown leakage current is much higher than the pre-breakdown leakage current. This is similar to the operation principle of the one-time-programmed antifuse.[212] The "unprogrammed" state can be defined as the pre-breakdown state; the "programmed" state can be defined as the post-breakdown state; the program process can be done by applying with a V_g larger than the V_{BD}, which transform the insulating dielectric thin film into the conductive state with nano-resistors penetrating through the film. On the other hand, the leakage current in the $+V_g$ range doesn't change the magnitude after the breakdown and is still much lower than that in the $-V_g$ range. This *I-V* curve is similar to that of a diode, i.e., the current flows from the substrate to the gate but not the opposite direction.

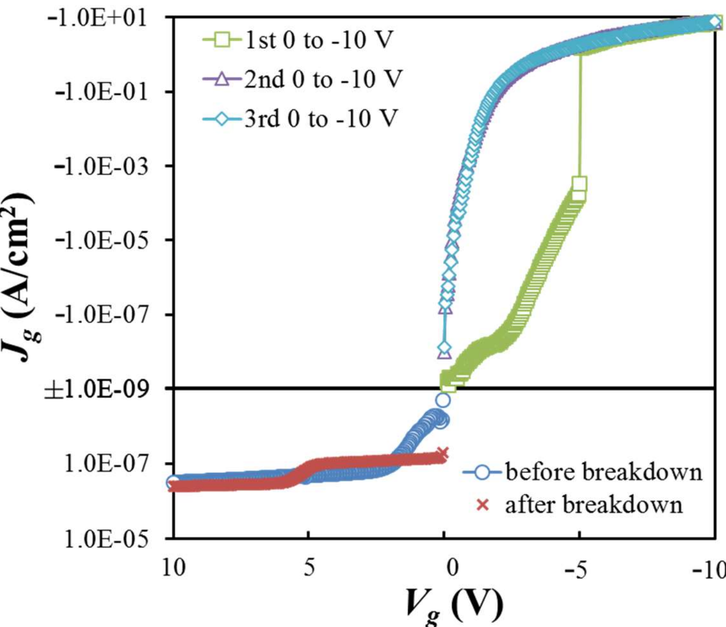

Figure 87. Diode-like *I-V* curve of the 12-min-deposited ZrHfO MOS capacitor with the anti-fuse function.

The diode-like function was further verified using the circuit as shown in Figure 88. The pulsed input voltage (V_{input}) is –10 or +10 V of 100 Hz and 50 % duty cycle. A small resistor of 10 Ω is included in the circuit to read the reference voltage (V_r) and calculate the current from $I = V_r / r$. The device under test (DUT) is the post-breakdown 12-min-deposited ZrHfO MOS capacitor, which has a resistance of 240 Ω. As shown in Fig. 88(c) and (d), the I through the device changes with the change of V_{input} in the $-V_g$ range but changes little in the $+V_g$ range. It is clear that the device conducts current from the substrate from the gate but not in the opposite direction. Furthermore, the pulse frequency changes from 10 Hz to 1000 Hz. Figure 89 shows that the diode-like *I-V* characteristics of the device still functions with the change of the pulse frequency.

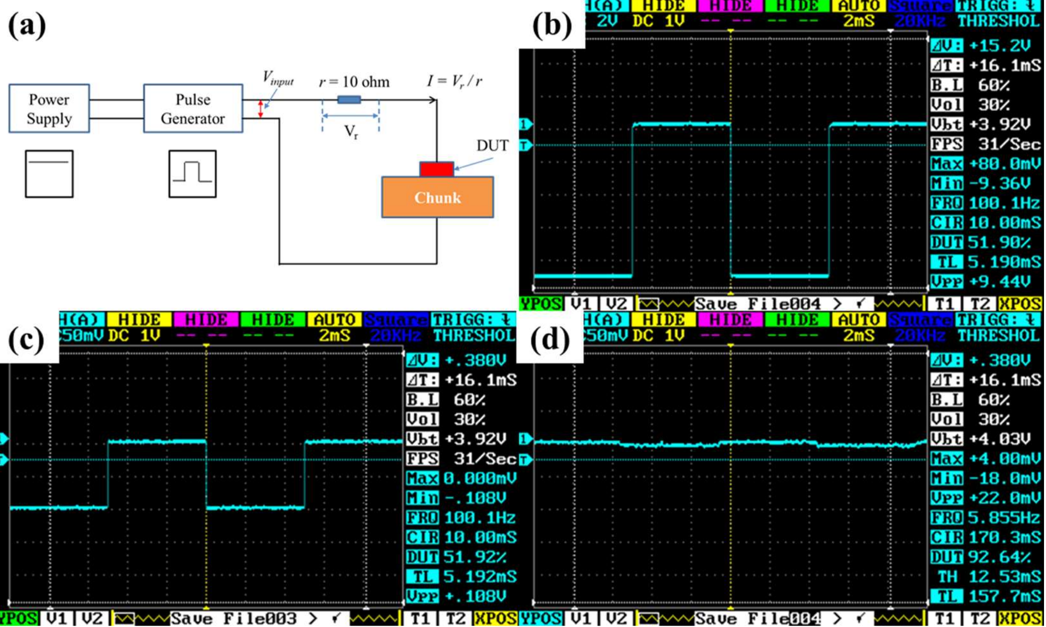

Figure 88. (a) The circuit used to read the current through the DUT driven by a pulsed voltage. (b) The pulsed voltage input with –10 or +10 V of 100 Hz and 50 % duty cycle. The V_r reading under the (c) –10 V and (d) +10 V pulsed voltage input.

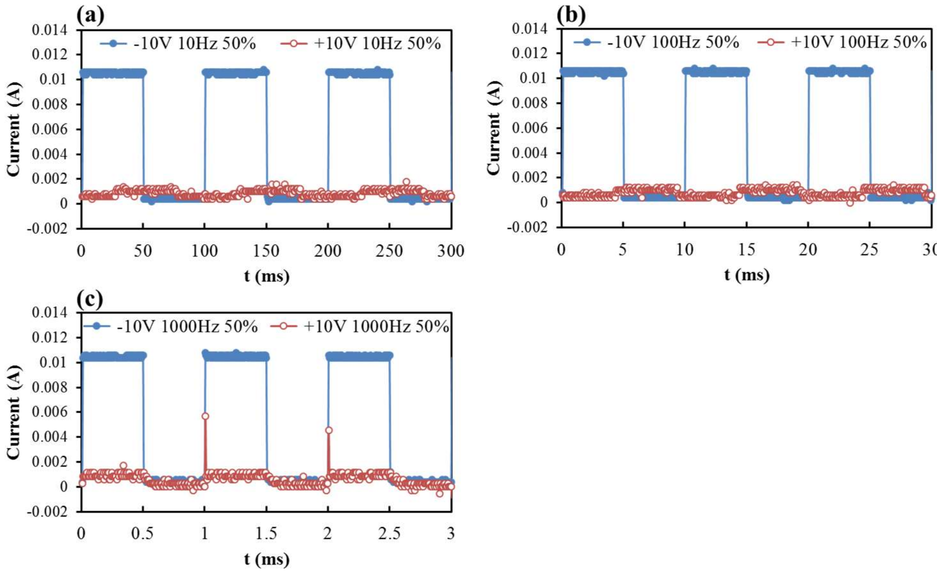

Figure 89. The current through the DUT driven by the pulsed voltage input with –10 or +10 V of 10-1000 Hz and 50 % duty cycle.

8.3.3 Dielectric Thickness Effects on Anti-Fuse Functions

Table 6 lists electrical parameters of the ZrHfO MOS capacitors with different ZrHfO deposition times calculated from *C-V* curves. The *EOT* increases with the increase of the ZrHfO deposition time due to the increase of the ZrHfO film thickness. At the same time, the longer exposure to the Ar/O_2 plasma generates more O to passivate the defects in the high-*k* stack, which shown as the decrease of D_{it} and Q_{ot}.[81] Therefore, the dielectric thickness increases but the defect density decreases with increase of the sputtering deposition time.

Table 6. Parameters calculated from *C-V* curves of the ZrHfO MOS capacitors with different ZrHfO deposition times from −2 to +1 to −2 V at 1 MHz.

time	*C* (F)	EOT (nm)	ΔV_{FB} (V)	D_{it} ($cm^{-2}\cdot eV^{-1}$)	Q_{ot} (cm^{-2})
3 min	2.75×10^{-10}	7.72	0.043	3.35×10^{11}	2.47×10^{11}
6 min	2.40×10^{-10}	9.24	0.055	2.18×10^{11}	1.82×10^{11}
12 min	2.30×10^{-10}	9.42	0.016	1.90×10^{11}	5.67×10^{10}
20 min	2.19×10^{-10}	9.94	0.012	1.40×10^{11}	4.32×10^{10}
40 min	2.15×10^{-10}	10.54	0.008	1.22×10^{11}	1.94×10^{10}
60 min	2.10×10^{-10}	10.63	0.002	1.03×10^{11}	4.85×10^{9}

The dielectric thickness effects on the pre- and post-breakdown *I-V* curves of the ZrHfO MOS capacitor were studied. Figure 90(a) shows that the pre-breakdown leakage current decreases with the increase of the deposition time. Less than 6 min deposition, the ZrHfO film has so many defects that the current transfers the film by the trap-assisted tunneling.[128] With the increase of the dielectric thickness and quality, the current transfer changes to the P-F and SE mechanisms and the leakage current decreases.[113] Accordingly, the $|V_{BD}|$ increases with the increase of the deposition time. On the other hand, Fig. 90(b) shows that the post-breakdown leakage current of device decreases as the dielectric thickness increases. Therefore, the ZrHfO anti-fuse device has a large on/off current ratio of $>10^5$ and its program voltage can be adjusted by the dielectric thickness as shown in Figure 91.

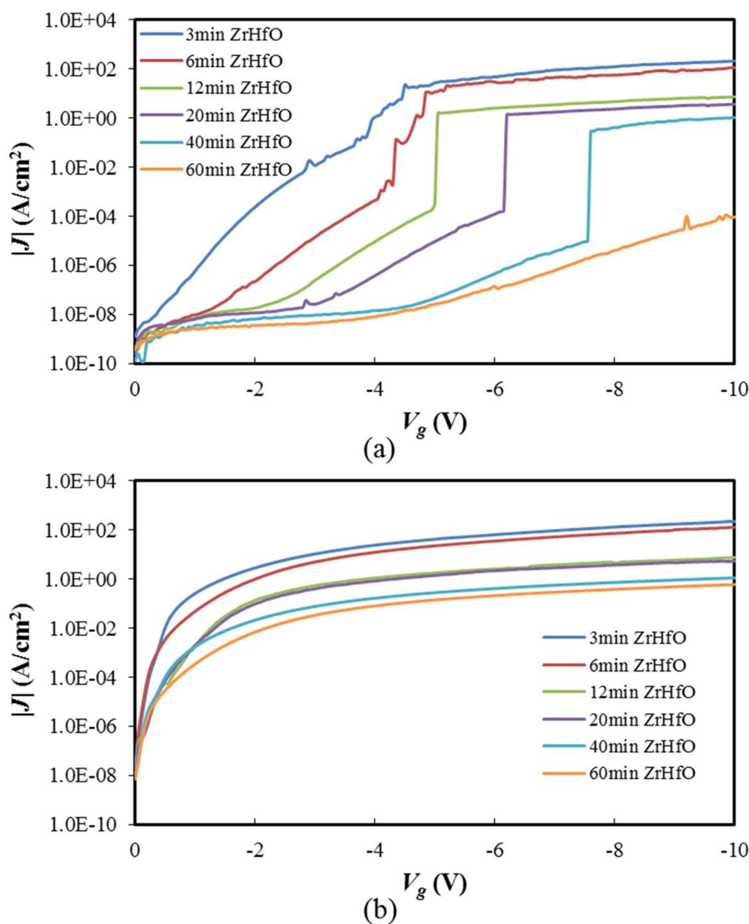

Figure 90. *I-V* curves of the ZrHfO MOS capacitors with different dielectric thickness (a) before and (b) breakdown from 0 to −10 V.

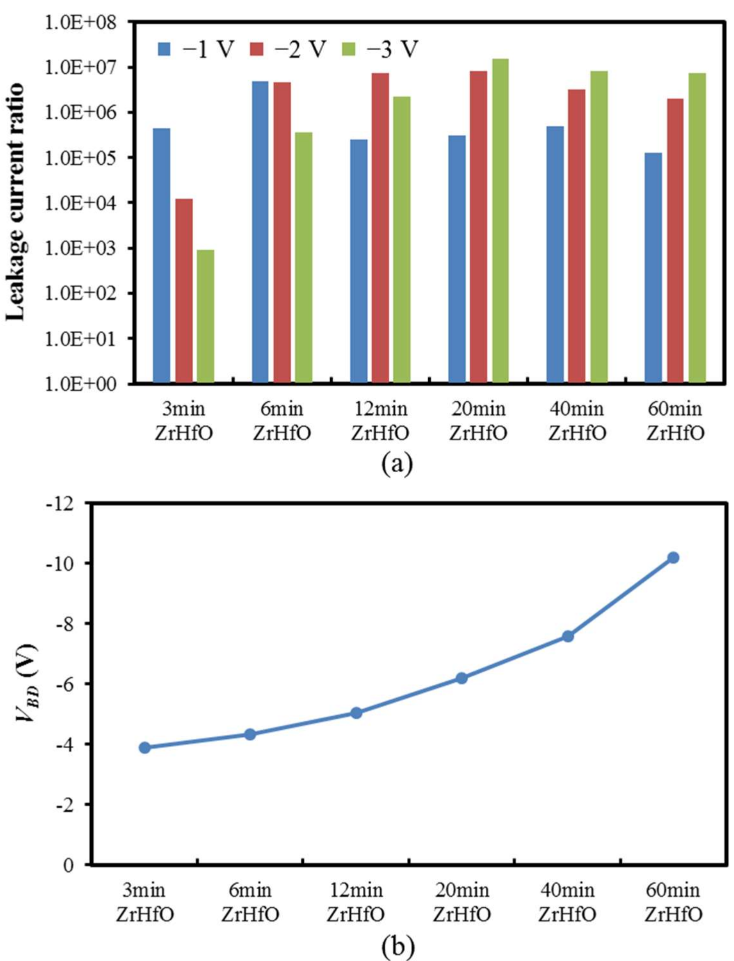

Figure 91. Dielectric thickness effects on the (a) ratio of pre- to post-breakdown leakage current and (b) the breakdown voltage of ZrHfO anti-fuse devices.

8.3.4 Device Size Effects on Anti-Fuse Functions

Figure 92 shows leakage currents of the 12-min-deposited ZrHfO anti-fuse devices with different gate diameters. Before the dielectric breakdown, the leakage currents of all the devices have the magnitude where the charges transfer through the high-*k* stack following the SE and P-F conduction mechanisms.[113] After the breakdown, the leakage

current density decreases with the increase of gate diameter. This is caused by the decrease of the number of nano-resistors formed in the devices. As shown in Figure 93, the bright dots in the same sample stressed at $V_g = -30$ V decreases with the increase of gate diameter. Since each bright dot corresponds to a nano-resistor, the total number of nano-resistors also decreases. This may be caused by the poor conductivity of the ITO gate that generates a larger electrical field different through the device with larger size. Additionally, the smaller device can have more supply of holes from the surrounding substrate, which forms more nano-resistors. Therefore, the smaller device size can enhance the anti-fuse function.

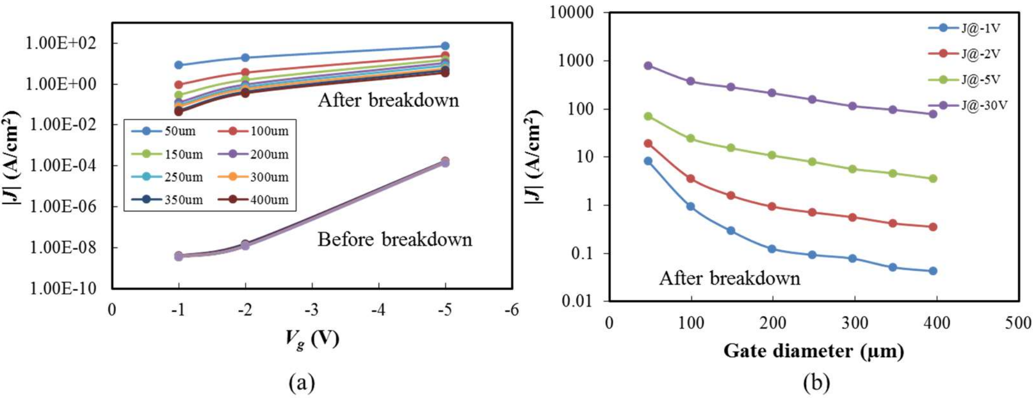

Figure 92. Leakage currents of the 12-min-deposited ZrHfO anti-fuse devices with different sizes before and after breakdown.

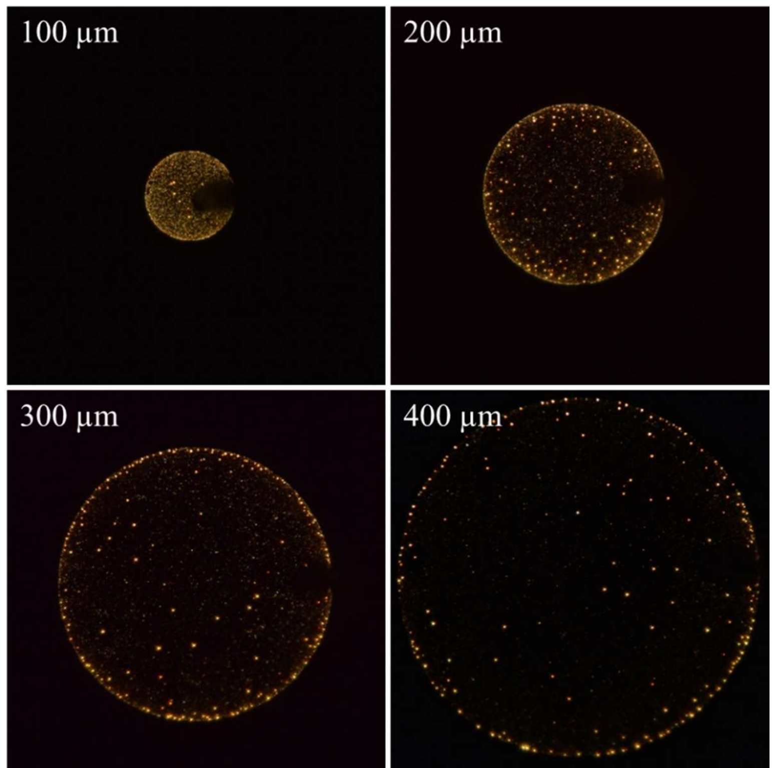

Figure 93. Light emission photos of the 12-min-deposited ZrHfO SSI-LEDs with different sizes. Stress at $V_g = -30$ V.

8.4 Summary

In this chapter, the light filtration effect of the *a*-Si:H and SiN_x thin films on the broadband light emitted from the ZrHfO SSI-LED has been investigated. The *a*-Si:H film strongly absorbed the light below 600 nm wavelength. The SiN_x film showed interference effect of which the wavelength of the peak transmittance was dependent on its refractive index and thickness. The refractive index of the film was adjustable from the N_2 flow rate in the deposition process. The light emitted from the SSI-LED could narrowed to a sharp peak at 850 nm when a multilayer stack of the *a*-Si:H and SiN_x films was used as the light

filter. The complete SSI-LED with the *a*-Si:H/SiN_x light filter can be made by the IC compatible processes and materials. It can be used as the Si-based light source for the on-chip optical interconnects. On the other hand, the nano-resistor device shows unique diode-like and anti-fuse functions. The current through the device is only allowed to flow from the substrate the gate but not in the opposite direction. The device has a dielectric thickness dependent program voltage and a large on/off current ratio of $>10^5$, which is applicable as the one-time-programed NVM.

CHAPTER IX

SUMMARY AND CONCLUSIONS

This dissertation investigated the nonvolatile memory, light emitting device, and other extensive applications of the doped metal oxide high-*k* gate dielectric, i.e., ZrHfO, with or with an embedded layer. All the devices had a simple MOS capacitor structure composed of the amorphous high-*k* thin films, which were prepared by the RF magnetron sputtering deposition in one pumpdown process and subsequently treated with the RTA method. Material and chemical properties of the ZrHfO high-*k* thin films were characterized by SIMS, AFM, and SEM. Electrical and optical characteristics of were investigated by frequency-dependent *C-V*, *G-V*, *J-V*, ramp-relax, CVS, and relaxation current measurements.

The nc-CdS embedded ZrHfO high-*k* dielectric NVM has been fabricated and investigated for its memory functions and charge trapping/detrapping mechanisms. The embedding of CdS layer inhibited the O diffusion to the high-*k*/Si interface layer, which reduced the growth of $HfSiO_x$ interface layer. This reduced the total capacitance of the capacitor and increased the density interface states. The device preferred to trap holes rather than electrons due to the *n*-type nature of the embedded CdS. There was no frequency dispersion of this device because the O or S passivated defects at the nanocrystal/high-*k* interface. Combined with the capacitance-voltage result, a large number of trapping sites were generated in the bulk CdS layer nanocrystals where holes were mainly trapped. On the other hand, the hole trapping/detrapping mechanism was

verified with the current-voltage measurement. The charge transfer followed SE and P-F mechanisms through the nc-CdS embedded high-k stack. The lifetime study showed that about 53% of the originally trapped charges could be retained after releasing the stress voltage for 10 years. Compared with other nanocrystal memories, the device showed excellent memory functions and charge retention capabilities at the low voltage operation. Therefore, the CdS layer embedded ZrHfO gate dielectric is suitable for the low voltage nonvolatile memories.

The influence of temperature on the charge trapping/detrapping and transfer mechanisms as well as the dielectric breakdown and charge retention characteristics of the nc-CdSe embedded ZrHfO high-k dielectric NVMs have been investigated. With an increase of temperature, the hole-trapping capacity was increased but the electron-trapping followed the opposite trend, which caused a small reduction of the memory window. From the frequency dispersion measurement result, more holes are loosely trapped at the nanocrystal/high-k interface and electrons are mainly trapped in the bulk nanocrystal at high temperatures. The high temperature induced a larger leakage current by increasing the charge supply from the Si substrate and transfer in the high-k stack. The increasing temperature dependence of the SE barrier height for was observed in both electron and hole transfers. In the $-V_g$ range, a P-F barrier height of 0.34 eV was estimated in the nc-CdSe embedded sample, which was probably located at nanocrystal/high-k interface. In the $+V_g$ range, the electron transfer changed to follow the F-N mechanism at the high temperature. On the other hand, the two-step breakdown phenomenon was observed in the device that corresponded to failures of the interface and the bulk high-k layers, separately.

The failure process was accelerated by the raise of temperature due to increases of defect states and defect effective conduction radii. The device's TDDB distribution involved two mechanisms, i.e., the process-induced defects and the intrinsic behavior of the high-*k* film. The Q_{BD} had an Arrhenius temperature dependence with an activation energy of 0.597 eV. The relaxation currents from the hole and electron detrapping showed different temperature dependences due to the different detrapping mechanisms, i.e., the tunneling and thermal emission, respectively. Therefore, the retention capability for electrons degraded faster than that for holes. In summary, temperature is an important factor in the operation of the nanocrystals embedded high-*k* memory device because it affects the charge storage/transfer mechanisms as well as the device reliabilities.

Electrical and optical properties of SSI-LEDs made from MOS capacitors of the same ZrHfO high-*k* film but two different PDA atmospheres have been investigated. Compared with the N_2 PDA sample, the O_2 PDA sample had a thicker and more SiO_x-rich interface layer and lower defect densities. These induced a larger dielectric breakdown strength and a lower leakage current in the O_2 PDA device, which therefore caused a less generation of nano-resistors during the stress. Light emitted from the O_2 PDA SSI-LED has a higher intensity and a slightly bluer component than that from the N_2 PDA SSI-LED due to the higher local temperature in nano-resistors. The SIMS study showed that the former contained more Si and O elements in nano-resistors than the latter did, which explained the difference in their electrical and optical characteristics. All in all, the PDA atmosphere affects the original high-*k* stack's material and physical properties, which

influences the formation and material composition of nano-resistors and eventually the light emission characteristics.

Electrical properties of nano-resistors made from the HBD of the amorphous high-*k* thin film MOS capacitor have been investigated. The formation of bumps each of which corresponded to a nano-resistor in the gate dielectric thin film was confirmed in AFM and SEM. Judged from bumps, the number and total area of nano-resistors increased with the increase of the stress voltage. The estimation methods for the effective resistance and the Schottky barrier height of nano-resistors were proposed. The temperature-dependent study of the effective resistance showed that the nano-resistor did behave like a conductor or a semiconductor. On the other hand, the effective barrier height decreased with the increase of the stress voltage, which was probably caused by the change of the composition of the nano-resistor. Separately, it was observed that the barrier height increased with the increase of temperature, which was due to the random and complicated formation process of nano-resistors. The stress time effect on the effective barrier height showed that nano-resistors were fully formed with stable electrical properties after the 1 min stress. In summary, the understanding of the electrical characteristics of this unique type of nano-resistors is important for its many electronic and optoelectronic applications.

Two methods have been employed to enhance white light emission from ZrHfO-based SSI-LEDs. First, the WO_x embedded ZrHfO high-*k* dielectric MOS SSI-LED was fabricated based on the embedding method. The embedding of the WO_x layer into the high-*k* stack increased the breakdown voltage due to the larger physical thickness. The emission showed larger bright dots due to the existence of W in the dielectric film and

nano-resistors. The inclusion of the W component in the nano-resistor enhanced the emission of the red to IR portion of the light, which overall increased the light emission intensity and shifted the light toward the warm color. Second, the amorphous ZrHfO dielectric was deposited on the heavily doped *p*-type Si substrate to reduce the substrate power dissipation and improve the light emission characteristics. The high-*k* dielectric deposited on the heavily doped substrate had higher defect densities in bulk and interface layers, a smaller breakdown strength, a larger leakage current, more light emission dots, and a higher light emission intensity. The spectrum shape and color of the emitted light were little influenced by the doping concentration, but the light emission efficiency was greatly enhanced by the heavy doping.

At last, the extensive application of nano-resistor devices were discussed. For the optoelectronic application, the broad band white light emitted by the ZrHfO based SSI-LED has been narrowed down by the addition of a PECVD *a*-Si:H or SiN_x thin film. The *a*-Si:H film absorbed the short wavelength portion, i.e., < 600 nm, of the light but transmitted the longer wavelength portion. The SiN_x film showed interference effect on the incident light, i.e., including peaks and valleys in the transmittance spectrum. The interference effect was dependent on the film's refractive index and thickness, which could be controlled by the deposition condition. Based on this idea, a multilayer stack of the *a*-Si:H and SiN_x films light filter was proposed to reduce the broad band light into a sharp peak at 850nm. The narrow band light emitted from the SSI-LED could be used as a unique Si-based light source for the on-chip optical interconnect. For the electronic application, the unique *I-V* characteristics of the nano-resistor device, i.e., allowing the

current to flow in one direction but not in the opposite direction, made it possible to function as a diode. The device had excellent anti-fuse functions, such as a high current ratio of >10^5 between on the “programed” and “unprogrammed” states and an on-set adjustable with the dielectric thickness.

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APPENDIX A

After the nano-resistor is formed in the high-k dielectric, the device allows the only allow the current to flow from the substrate to the gate. Here, only the electron transfer from the gate to the substrate is considered. The contact between the nano-resistor and the Si substrate can be taken as the Schottky contact.[83] The original equation for a Schottky barrier can be described with the consideration of image-force lowering:[176]

$$I = A \cdot A^* T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \exp\left(\frac{q\sqrt{qE_m / 4\pi\varepsilon_s}}{kT}\right), \qquad \text{[A-1]}$$

where E_m is the maximum electrical field across the barrier. The image-force lowering is also known as Schottky-barrier lowering that is caused by the attraction force caused by the positive charge on the metal surface, which is induced by the transfer of electrons across the barrier.[176] Since most of the current flows through the nano-resistor, the area ratio of all nano-resistors to the gate electrode is included:

$$I = \phi A \cdot A^* T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \exp\left(\frac{q\sqrt{qE_m / 4\pi\varepsilon_s}}{kT}\right). \qquad \text{[A-2]}$$

The E_m can be calculated with the following equation:

$$E_m = \sqrt{\frac{2qN}{\varepsilon_s}\left(V + \Psi_{bi} - \frac{kT}{q}\right)}. \qquad \text{[A-3]}$$

Here, we use $V-IR_s$ to represent the voltage drop across the Schottky barrier, i.e., V in Equation A.3, and therefore, the equation can be written as:

$$E_m = \sqrt{\frac{2qN}{\varepsilon_s}\left(V - IR_s + \Psi_{bi} - \frac{kT}{q}\right)}. \qquad [A-4]$$

where N is the accumulated hole density at the nano-resistor/Si interface, which is assumed to be constant.

When we put Equation A.4 into Equation A.2, the equation can be written as:

$$I = \phi A \cdot A^* T^2 \exp\left(\frac{-q\Phi_B}{kT}\right)\exp\left[\frac{q\sqrt{q/4\pi\varepsilon_s}}{kT}\sqrt[4]{\frac{2qN}{\varepsilon_s}\left(V - IR_s + \Psi_{bi} - \frac{kT}{q}\right)}\right]. \qquad [A-5]$$

This equation can be transformed into:

$$V = \frac{8\pi^2\varepsilon_S^3 k^4 T^4}{q^7 N}\left[\ln(I) - \left(\ln\left(\phi A \cdot A^* T^2\right) - \frac{q\Phi_B}{kT}\right)\right]^4 + IR_S - \left(\Psi_{bi} - \frac{kT}{q}\right). \qquad [A-6]$$

Therefore, the equation can be further simplified as:

$$V = a\left[\ln(I) + b\right]^4 + IR_S + c \text{ or } y = a\left[\ln(x) + b\right]^4 + R_S \cdot x + c. \qquad [A-7]$$

Once we obtain the number b from the fitting of the experimental data, we can calculate the effective barrier height:

$$\Phi_B = \frac{kT}{q}\left[b + \ln\left(\phi A \cdot A^* T^2\right)\right]. \qquad [A-8]$$

The Schottky barrier fitting was done in Matlab using the following codes:

```
%Create the input vector i and v
i=0;
v=0;
%Input the I and V data into the vectors i and v with an interval of 0.05 V
%Calculate the series resistance R from the I-V from -8 to -10 V
c=polyfit(i(161:200),v(161:200),1);
R=c(1);
%Choose the iteration parameters
```

```
fo = fitoptions('Method','NonlinearLeastSquares',...
            'Robust','Bisquare',...
            'Lower',[0 0 -Inf],...
            'Upper',[Inf Inf Inf],...
            'StartPoint',[1e-5 20 0],...
            'Algorithm','Trust-Region',...
            'DiffMinChange',1e-8,'DiffMaxChange',0.1,...
            'MaxFunEvals',3000,'MaxIter',2000,...
            'TolFun',1e-8,'TolX',1e-8);
%Create the fitting equation
ft = fittype('a*(log(x)+b)^4+R*x+c','problem','R','options',fo);
%Fit the I-V from 0 to -1 V
[f,gof] = fit(i(1:21),v(1:21),ft,'problem',R);
%Output the result to the vector result
result = [f.a f.b f.c gof.sse gof.rsquare gof.adjrsquare gof.rmse];
```

The goodness of the fitting is evaluated based on four statistics, i.e., the sum of squares due to error (SSE), the R-square (R^2), the Adjusted R-square (Adjusted R^2), and the root mean squared error (RMSE). The smaller the SSE and RMSE numbers are, or the closer to 1 the R^2 and Adjusted R^2 numbers are, the better the fitting is.