HYBRID ROUTER DESIGN FOR HIGH PERFORMANCE PHOTONIC NETWORK-ON-CHIP

A Thesis

by

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Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

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August 2015

Major Subject: Computer Engineering

ABSTRACT

With rising density of cores in Chip-Multiprocessors, traditional metallic interconnects won't be able to cater to the high demand in communication bandwidth at lower power consumption. Photonic interconnects are emerging as a very competitive and promising alternative to address these bottlenecks in recent times. The infrastructure for realizing such a communication architecture comprises of Micro Ring-resonator based silicon nano-photonic routers and waveguides. We propose a novel 5×5 photonic router microarchitecture employing mode-division-multiplexing along with wavelength-division-multiplexing and time-division-multiplexing. It increases the aggregate bandwidth almost four times in a network consuming almost 30% less power as compared to other recent photonic routers and laying the foundation of a high performance photonic network-on-chip(PNoC). We validated the feasibility of the proposed architecture and developed a new circuit switched based network simulator(PhotoNoxim) based on the router microarchitecture proposed by us to validate it under various synthetic traffics and benchmark applications.

DEDICATION

I dedicate this thesis to my parents, Mr. Duryodhan Patra and Mrs. Bijayalaxmi Swain and my brother, Mr. Plaban Patra for their unconditional love and support.

ACKNOWLEDGEMENTS

I would like to thank my academic supervisor, Dr. Rabi Mahapatra for his brilliant guidance and constant motivation. I would also like to extend my gratitude to my committe members, Dr. Eun Jung Kim and Dr. Samuel Palermo for their invaluable feedback and suggestions. I am also extremely thankful to Dr. Suman Kumar Mandal and Dr. Ayan Mandal from Intel Corporation for their insightful opinions which helped me in finishing this thesis successfully. I am grateful to Dr. Martin Fiers and the entire team of Luceda Photonics for providing IPKISS to validate and simulate photonic components. My heartfelt thanks to Mr. Dharanidhar Dang who has been a constant support and guide throughout this research. I am grateful to my parents, friends and colleagues at the Embedded System and Co-design Lab for their support and encouragement.

Finally I would like to thank the Department Of Computer Science & Engineering at Texas A&M University for providing me this wonderful opportunity.

NOMENCLATURE

MRR	Micro-Ring Resonator
PNoC	Photonic Network-on-Chip
J	Joules
CMP	Chip-Multiprocessor
MDM	Mode Division Multiplexing
WDM	Wavelength Division Multiplexing
TDM	Time Division Multiplexing
NI	Network Interface

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1. INTRODUCTION

1.1 Motivation

In the contemporary era, information is generated in abundance. In order to process those information, various efforts have been made to increase the processor performance. According to Moore's law the processor performance doubles up every two years. But until 2000 according to the law the processor speed kept on increasing. After that it was tough to increase the overall performance by increasing the efficiency of a single processor. This limitation or in other words constraint was overcome with the dawn of the era of chip multiprocessors(CMP). As was stated in [13][38] performance gain was to be derived by increase in the number of processor cores on chip. This approach has enhanced the throughput performance in CMPs by exploiting paralleilism with less power requirements. Semiconductor roadmap[23] predicts that in the next decade feature size will shrink to sub-10-nm regime. This leap in the process technology will scale the number of cores and threads per devices rather than increase speed or complexity of an indivdual core. This will result in faster processing with the help of thousands of threads running highly parallel codes. But this paradigm shift in the computing world poses newer challenges and issues which needs to be addressed.

Increasing density trend of CMPs involves considerable amount of interaction among the cores on chip. The cores will need to access data from local and distant caches as well as off-chip memory. As a result it requires higher bandwidth and a lower latency to support extensive communication among a large number of cores. Semiconductor NoCs would not provide such a large bandwidth while maintaining an acceptable level of power consumption[23]. The limitation of metallic interconnects

in terms of loss, dispersion, cross-talk and speed are becoming increasingly obvious as interconnect density rises. In order to address the growing communication requirements, alternative on-chip interconnect paradigms are required.

Recently, integrated photonic links are being adopted as reliable and attractive alternative to traditional metallic interconnects [26]. They hold promise to higher rate data transfer with minimal power dissipation [24]. Photonic links avoid capacitive, resistive and signal integrity constraints and allow efficient realization of physical connectivity. Also, *low loss in optical waveguides* [26] and *bit rate transparency* [32] are added advantages of photonic on-chip communication. The key power savings rises from the fact that once a photonic path is established, the data are transmitted end to end without the need for repeating, regenerating and buffering[25]. On the contrary in electrical NoCs messages are buffered, regenerated and transmitted over several router links en route to the destination. In addition to that over the past several years remarkable advances and breakthroughs have been made in the field of silicon photonics. All these support for a high performance, low power, and low cost photonic NoC (PNoC). PNoC is by far the most promising archetype to meet the needs of the next generation on-chip communication.

1.2 Related Works

In recent years several Photonic NoC architectures have been proposed using topologies like mesh [24], torus [26], crossbar[8], and clos[5]. We can classify photonic NoC architectures into two major categories based on the communication techniques used: (1) deterministic passive networks, and (2) dynamic switching networks. Wavelength selective passive networks utilize deterministic switching in which a fixed routing pattern is defined during the network design and the optical path between the source and destination is established by dynamically selecting a specific wave-

length at the source or the destination [5]. Passive networks offer limited scalability and complicated design[6]. Whereas optical networks using dynamic switching are circuit switching networks, where the routing pattern is dynamically set beforehand by an electronic controller [24][26]. It is imperative to combine microelectronic control technology and photonic transmission as it is difficult to realize signal processing in photonics.

Various crosbar topology based PNoC architecture has been examined by the researchers as in [26][5] and [8]. They have proposed several channel sharing crossbar architectures called Single-Write-Multiple-Read(SWMR) or Multiple-Write-Single-Read(MWSR) architectures. Batten et al.[8] implemented an opto-electrical global crossbar between small groups of cores and DRAM models[8]. Vantrease et al proposed Corona, a 3D MWSR channel sharing crossbar architecture where there is a dedicated channel for listening for each node, but several nodes compete to send messages on the same channel[9]. Pan et al also proposed a SWMR based crossbar design[16]. Though these designs correctly addredssed the latency issues faced by several other contenporary architectures they suffer from scalability as fully connected crossbars do not scale well[7].

Shacham et al. proposed a hybrid electrical-photonic NoC architecture[25]. They used a electrical control circuit for arbitration and a photonic message transmission circuit. Though the use of a hybrid architecture was a brilliant idea which we have also followed in our design, the placement of MRRs as photonic switching elements involved turning on more number of MRRs. Though their design provides a higher bandwidth than the electrical NoCs the average latency per throughput is not significantly improved.

Hendry et al. proposed a TDM based photonic arbitration circuit due to the absence of photonic buffers which addressed the issue of average latency[10]. But the

TDM based arbitration makes the whole communication more deterministic rather than adaptive. Also it results in unnecessary turning on of MRRs in setting up paths between a source and destination.

It is reported in [8] that the wavelength selective passive network exhibits low latency as the wavelength selecting time is much shorter than the network configuration time. On the contrary, switching networks offer higher aggregate bandwidth by adopting WDM technology. Also, circuit switching in optical domain is more compact and it offers good scalability [31]. So among the various architectures discussed above almost all of them prefer a hybrid opto-electronic network.

Router is a critical component of NoC. Several MRR based optical routers have been proposed in the literature [31][24][25][33]. In [31], a low power, low cost, and non-blocking 5X5 optical router has been proposed using 16 MRRs. The design appears to be non-scalable due to significant power consumption when network size increases. In [25], the authors have proposed a 4×4 hybrid, blocking router using 8 MRRs. This design is complex and the aggregate bandwidth is limited due to its blocking nature. M. Briere et al. proposed the λ router[12]. It uses a passive switching fabric and WDM technology. An $N \times N$ λ-router requires N wavelengths and multiple basic 2×2 switching elements to realize non-blocking switching function. In order to fully utilize all the components it prefers N to be even which may not be feasible in every case. The authors in [33] proposed a 4×4 λ-router using passive switching fabric with 30 MRRs incorporating Wave Division Multiplexing(WDM). Due to use of increasing number of waveguide crossings and MRRs, such a design results in higher insertion loss rendering it non-scalable. A. W. Poon et al. proposed a 5×5 optical router based on an optimized crossbar[18]. In this architecture each port of the router is aligned to its corresponding direction to reduce the waveguide crossings around the switching fabric. Therefore a high performance, low power, and

low cost photonic router is highly desirable for scalable NoC.

1.3 Contributions

The research corresponding to this thesis has the following contributions:-
(1) A new 5×5 non-blocking photonic router design has been proposed by integrating *mode-wavelength-time* division multiplexing for high performance. The proposed approach is the first of its kind to the best of our knowledge. (2) A logical layout of the photonic router has been presented to achieve reduced power and area leading to scalable NoC architecture. (3) To demonstrate and validate the proposed design, a detailed simulation platform was used to evaluate the proposed router micro-architecture. The results indicate an aggregate bandwidth of 40-Gbps which is 4 times higher than the recently reported results [24]. The proposed router consumes 55X-60X lesser power than a high performance electronic router. It shows an energy consumption of 3.2fJ/bit per optical path and 0.51fJ/bit per router which is about 32.9% less than the recently reported results.

The thesis is organized as follows. In chapter 2 we will give an overview of Silicon Photonics. The basic components and the terminologies used in silicon photonics will be described briefly for clarity before we dive into the details of the proposed PNoC architecture. In chapter 3 the architecture of the proposed photonic router is presented. It includes the layout, design and control mechanism. Various Experiments and the results corresponding to the proposed PNoC architecture and a comparative analysis between the existing designs are presented in chapter 4. We conclude the thesis in chapter 5 with some directions for future research.

2. BASICS OF SILICON PHOTONICS

Optical interconnects and routers are the building blocks of photonic NoCs. A photonic router consists of high speed Microring Resonator(MRR) based switches and extremely low-latency optical waveguides to provide photonic NoC as an alternative to electrical NoCs. Before diving into the details it is better to be familiar with some of the photonic components which are the building blocks of the proposed PNoC and the associated terminologies. It is also necessary to have an understanding of how a simple communication takes place between two cores in a PNoC.

2.1 Silicon Photonic Components

2.1.1 Silicon Photonic Waveguide

Silicon photonic waveguide is the building block of several photonic components and lays the foundation for integrating photonics with a Silicon substrate. They are the basis of many optical devices such as MRRs, Directional Couplers, Multiplexers and De-multiplexers, communication channel etc. It basically consists of a Si core having an extremely small cross-section surrounded by SiO_2 cladding material. Due to the difference in refractive index of the core and the cladding the light travels being confined within the waveguide due to total internal reflection.

2.1.2 MRR

Micro-ring resonator is one of the principal components of a photonic network-on-chip. As quoted in the Laser and Photonics Reviews[15], a generic ring resonator consists of an optical waveguide which is looped back onto itself such that a resonance occurs when the optical path length of the resonator is exactly a whole number of wavelengths. So in this way an MRR is capable of supporting multiple resonances

with a gap equal to the free spectral range(FSR) which in turn depends on the resonator length. The practical application of MRR is always along with a coupler which is necessary for it to interact with the outside world. It is basically an accessing mechanism. When in the loop the round trip phase shift equals the integer times 2π , resonance occurs and the wave is coupled successfully to or from the MRR.

2.1.3 Silicon Photonic Laser

Laser sources can be of different types depending upon the need of transmission. In the proposed design we have used Mode-Locked Lasers. The important fact is that they are the major source of power consumption in a PNoC.

2.1.4 Photo Detector

At the receiver end, the light passing through the silicon waveguide must be detected in order to reconvert the modulated data into electronic form. Photo-detectors contain PIN photodiodes to convert optical power into electric current. Recently, graphene is said to be a promising material for ultra-broadband photo-detectors[37].

2.1.5 Silicon Optical Modulator

It is used to modulate a light beam propagating in the optical waveguide with electrical data signals. The most common method of achieving modulation in silicon devices so far has been to exploit the plasma dispersion effect, in which the concentration of free charges in silicon changes the real and imaginary parts of the refractive index[19]. Micro-Ring modulators has been widely explored due to its compact footprint and low drive voltage. The nature resonant frequency of a micro-ring can be shifted by an index change and thus a large modulation depth occurs near the resonance.

2.1.6 Optical Coupler

It is a challenge in silicon photonics to obtain efficient coupling between highly confined mode in a waveguide and the large diameter mode in optical fiber to couple light in and out of the chip. Recently several solutions like surface gratings and tapers are proposed in which the thickness and width of silicon layer are increased.

2.1.7 Silicon Photonic Transmitter

The silicon photonic transmitter comprises of a laser source, an optical modulator that modulates the light signal with electric signal data and a multiplexer that multiplexes the signal light of multiple wavelengths or modes to be transmitted on a single transmission line.

2.1.8 Mode Locked Laser

Mode-locked-laser consists of an active laser resonator, and an optical mirror. Laser resonator produces ultra fast optical pulse circulating around it. Each time the pulse hits the optical mirror, a pulse is emitted out of the laser. As a result, an optical pulse train of specific wavelength and time period is generated. This phenomenon is called mode-locking as all the modes are trapped inside the laser resonator as a single pulse and hence the term mode-locked-laser.

2.2 Multiplexing

As mentioned in the introduction, the advent of silicon photonics as an alternative to conventional CMOS chips was imperative owing to its superior bandwidth capability and lower power dissipation. In order to facilitate such a higher aggregate bandwidth several multiplexing techniques have been proposed. The goal of multiplexing is to boost the aggregate throughput by utilizing the existing communication infrastructure on a chip. Over the recent years, with the increase in technical finesse

of fabrication technology, researchers have been able to exploit unique features of light to come up with several multiplexing techniques.

2.2.1 Wavelength-Division-Multiplexing

Wavelength-Division-Multiplexing(WDM) is the most commonly used technology to increase the bandwidth of the optical communication system. In this scheme multiple wavelengths are employed to carry optical signals from the source to destination. The data rate in optical communication is limited to the modulation speed but the overall bandwidth can be scaled with the no of wavelengths used in a system acting as parallel communication channels.

Dense WDM(DWDM) technology has been used to enable tens of channels with varying carrier wavelengths over single mode optical fibers in long optical networks. But due to its sensitivity to temperature, the emission wavelengths of the laser need to be aligned and stabilized properly. It makes the switching and routing in DWDM systems complicated, power hungry and expensive rendering it unsuitable for on-chip communication[2]. The alternative is coarse WDM(CWDM) which has less requirements in terms of alignment/control. A 4 -channel CWDM link with 400 GHz channel spacing has been used to realize 50 Gbps communication link between two chips[3].

2.2.2 Mode-Division-Multiplexing

A mode can be defined as an electromagnetic field distribution that satisfies the theoretical requirements for propagation in a waveguide or oscillation in a cavity or in other words an electromagnetic wave traveling in a fiber. Exploiting spatial mode as an independent channel in conjunction with WDM would increase the bandwidth density of an-chip interconnect by manifolds, reduce the number of waveguide crossings and add an additional design degree of freedom in next generation pho-

tonic networks. Earlier there have been efforts of implementing mode multiplexing based on Mach-Zehnder interferometers[39][21], Multi-mode interference(MMI) couplers[29][20] etc. But they had larger footprints and supported a limited number of optical modes.

In 2014 Luo et al. came up with a micro-ring resonator based on-chip WDM-compatible mode-division multiplexing (and demultiplexing scheme)[28]. They demonstrated the capability of the design to be multiple co-propagating 10Gb/s high-speed communication signals reaching up-to 60Gb/s of aggregate bandwidth.

On the basis of propagation constant matching, an optical mode in a single mode waveguide can be evanescently coupled to a specific spatial mode in an adjacent multimode waveguide, in which the coupling strength to the node depends on the width of the multimode waveguide[28]. The propagation constants of different spatial modes can vary significantly due to the high core-cladding index contrast. In Fig.2.1 taken from [28], the arrangement of the ring resonators and waveguides for facilitating mode multiplexing is shown.

The Ring resonators are formed from a 450-nm wide waveguide. They are designed to support only the fundamental TE mode with effective refractive index(R_{eff}) of 2.46. The multimodal transfer waveguide is tapered at several places. When the waveguide width corresponds to 450 nm, 930 nm, or 1.41 μm, the effective indexes of TE_0, TE_1 or TE_2 modes respectively, match the effective index of TE_0 mode of the microring to the TE_0, TE_1 or TE_2 modes in the multimode waveguide. By adjusting the coupling gap and coupler length between microrings and waveguides, the insertion loss for the desired mode and the power coupled to other modes can be minimized. All these features along with an integrated heater on top of each microring to tune the microring resonances to align to the WDM channels optimizes the performance of the whole device.

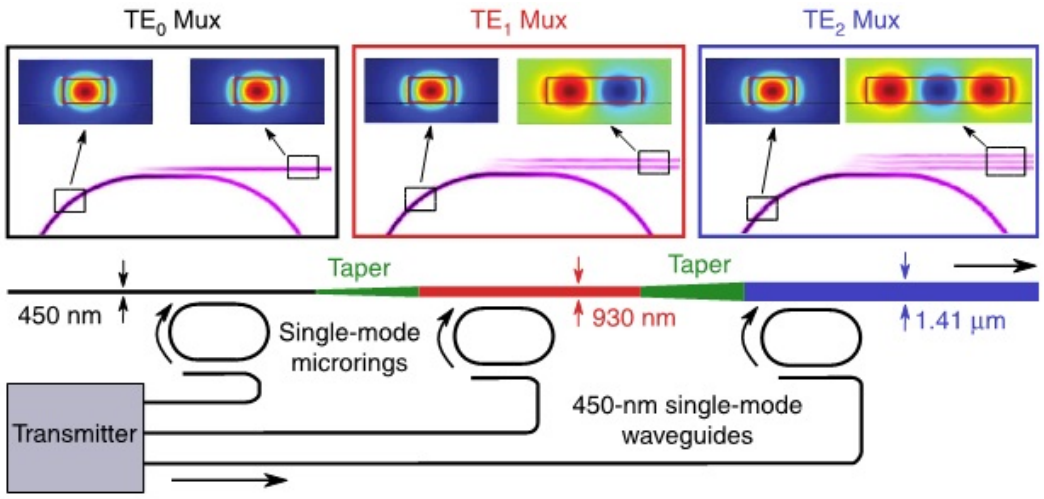

Figure 2.1: Selective coupling of the single-mode microrings to a specific spatial mode in multimodal waveguide *Courtesy:*[28]

Looking at the bigger picture, each microring resonator can support 87 WDM channels over the entire C-band(1530-1565nm) keeping the channel spacing as 50GHz. Luo et al. demonstrated that tapering the multimode-waveguide upto 2.37µm, 5 spatial modes can be supported. With the above setup, potentially an amazing 4.35Tbps aggregate data rate can be supported.

2.2.3 Proposed Adaptive Multiplexing

In our proposed design we adopt the aforementioned WDM-compatible MDM arrangement to design a high throughput and low power consuming photonic router. For our experiments we used two modes each of the two wavelengths we used for communication. The respective MRRs are turned on with the help of an electrical controller whose functional algorithm will be properly described in chapter 3.

2.3 Communication Flow

The process of optical communication(Fig.2.2) starts with the laser source producing the light which is coupled with the waveguide on chip with the help of a

silicon optical coupler. The Ring modulator modulates the electronic signal from the core on to the appropriate channel. The multiplexer's job is to couple the modulated signal onto the desired wavelength and mode in the multimodal transmission fibre. Data is then transmitted along the waveguide till the destination. The propagation path can be changed or switched by appropriate photonic switches along the path made by the combination of MRRs and waveguides. At the destination the light signal is detected by the photo-detector and is demodulated to feed the information to the destination processor core. The whole process is depicted as a symbolic diagram in the following figure.

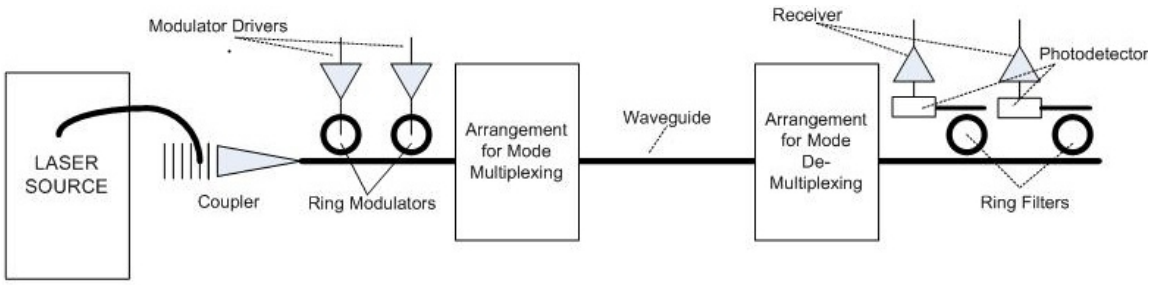

Figure 2.2: Communication flow in silicon photonics

3. PHOTONIC ROUTER*

The proposed photonic router is a fully non-blocking 5×5 photonic router for NoC design. A photonic router in a PNoC consists of a number of I/O ports, a switching fabric connecting the input ports to the output ports, and injection/ejection ports connected to the local IP core via the network interface(NI). Fig.3.1 shows a 2D-mesh PNoC architecture consisting of five-port photonic routers. We zeroed on using a 2D mesh topology due to the same reasons that made them popular in electronic NoCs. Their appropriateness to handle a large variety of work-loads and their good layout compatibility with a tiled CMP chip[40] apply in photonic NoCs too.

3.1 Router Micro-architecture

The hybrid photonic router consists of mainly two circuits :-

1- Photonic circuit switching circuit

2- Electronic packet switching circuit

The PNoC microarchitecture adopts a hybrid design. It combines a photonic switching fabric for circuit-switched bulk data transmission and an electronic packet-switched network for distributed control through *control packet* transmission. Hence the term 'hybrid' refers to the concept of combining electronic and photonic components as well as to the idea of combining a packet-switched network and a circuit-switched network.

This takes advantage of both the technologies i.e. photonic and electronic. Photonic technology provides superior advantages in terms of low power, large bandwidth

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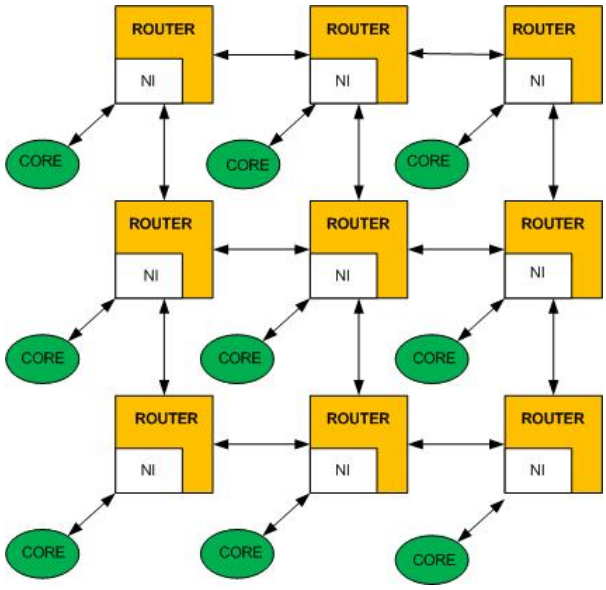


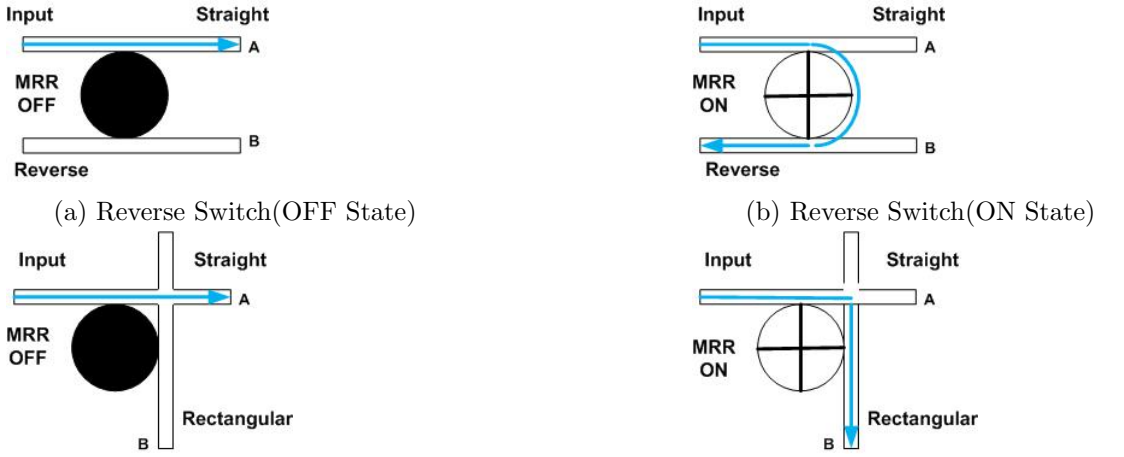
Figure 3.1: 2D PNoC architecture

and high speed communication. On the other hand, electronic control technology offers flexibility to adopt packet-switching. Packet switching requires buffering which is difficult to implement with photonic components. The main objective of employing a hybrid scheme is to address the higher power consumption in electronic NoCs, that scales up with the bandwidth[38].

The photonic interconnection network consists of MRR and waveguide based routers and links to communicate large data packets. The electronic control network, comprising of an electronic controller integrated with each photonic router controls the operation of the photonic network. In this research we mainly focus on the photonic router micro-architecture rather than the electronic controller. In the following subsections we discuss the detailed switching elements and router layout. We will go through the infrastructure responsible for boosting the performance of the photonic router.

3.1.1 Switching Fabric

A switching element in a fabric is composed of MRRs and waveguides as shown in Fig.3.2. The switching fabric consists of a set of parallel and rectangular 1×2 switching elements unlike 2×2 conventional electrical switches where each 1×2 switching element serves the purpose of parallel or orthogonal routing using fewer MRRs. We introduce in brief the working principles of 1×2 switching elements used in router micro-architecture.



(a) Reverse Switch(OFF State)

(b) Reverse Switch(ON State)

(c) Rectangular Switch(OFF State)

(d) Rectangular Switch(ON State)

Figure 3.2: MRR switching

3.1.1.1 Basic 1×2 Switching Element Using MRR

The basic switching element of a photonic router is a micro-ring resonator. A MRR is a circularly coiled waveguide which has the property of rotating the optical signal in the clock-wise direction. During 'OFF' state of MRR, optical signal with wavelength λ_{on} propagates from the input port to the straight port(refer: Fig.3.2a and Fig.3.2c). When turned 'ON' it couples the resonating optical signal (indicated

by arrow) in waveguide A and transmits it by coupling it to waveguide B as shown in Fig.3.2b and Fig.3.2d. One can see that, in Fig.3.2d as the waveguide B is placed orthogonal to the waveguide A, the MRR helps in turning the optical signal in the rectangular direction. However it involves crossing of the two waveguides which may lead to loss due to cross-talk while passing multiple optical signals. It also results in higher insertion loss. To reverse the direction of propagation of the optical signal, one has to use combination of two rectangular switching circuits resulting in two waveguide crossing points. So, in order to decrease the number of crossing points of waveguides and usage of MRRs, a reverse parallel switching arrangement is made as shown in Fig.3.2b. In this arrangement when the MRR is 'ON', it helps in coupling the optical signal from waveguide A to waveguide B in reverse direction. This mechanism makes MRR an 1×2 switching element. With the help of these two types of switching arrangements, we were able to reduce the number of MRRs being used while reducing the no. of waveguide crossing points.

In the proposed scheme, we have incorporated WDM. Hence optical signal of multiple wavelengths can be coupled together through MRR. This will enhance the overall bandwidth of the network communication. The fundamental difference between the two basic 1×2 switches is the position of the two waveguides. The reverse switching element does not have any waveguide crossing unlike the rectangular-switching element. The insertion loss per waveguide crossing is 0.12dB[18]. MRR needs a DC current to switch ON and it consumes power less than 20μW [18]. In the OFF state, there is negligible power consumption by the MRR [12]. The switching time of the MRR is very small and it is 10ps in our case.

3.1.1.2 Router Layout

The 5X5 router layout which is adapted from [24], has been depicted in Fig.3.3. This uses suitable placement of 16 identical MRRs along with various waveguides.The router has five bi-directional ports, viz. East, West, North, South, and NI port. East, West, North, and South ports are connected with other routers to form a 2D NoC whereas the NI port is connected to the network interface. Each photonic router has a controller within NI for selecting wavelength and mode for optical signal transmission. The router can operate on multiple wavelengths simultaneously using WDM with wavelength spacing equal to the free spectrum range of the MRR. As shown in Fig.3.3, there are optical paths for each of the input-output combination. Complex routing in a 2D photonic layer is possible due to MRR based switches and waveguide crossings. However, waveguide crossing incurs optical insertion loss. Hence it's important to design an efficient layout of MRRs in a photonic router with least number of waveguide crossings. The proposed 5×5 non-blocking router consists of 14 waveguide crossings and 16 MRRs as in Fig.3.3 resulting in an optimized design. Apart from that, there are 2 more MRRs within network-interface to facilitate MDM which is explained in the later sections. Insertion loss and crosstalk limit the scalability of the photonic router [4][17]. Analytical results on number of MRRs and various performance parameters of photonic router are discussed in detail in the later sections.

3.1.2 Network Interface

Use of WDM in photonic circuits offers limited performance gain because of its comparatively higher power consumption [28]. MDM in conjunction with WDM and TDM can provide potentially larger performance gains and higher aggregate bandwidth [28]. Use of MDM technology does not require increasing the number

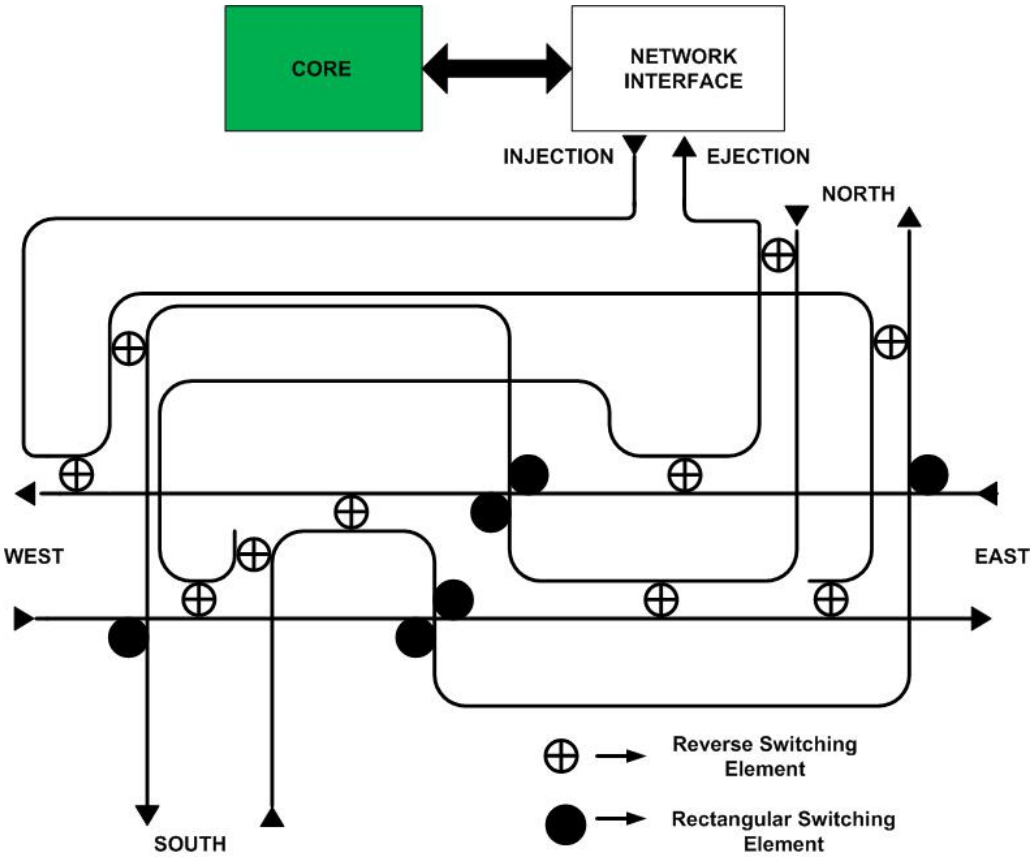


Figure 3.3: Logical layout of 5×5 photonic router

of waveguides which leads to fewer wave-guide crossings. As mentioned in Mode-Division-Multiplexing in chapter 2 by tapering a 2.37μm multimodal waveguide upto 5 spatial modes can be supported. It also uses least area on chip and power. In this design the Network-interface [NI] is deployed with WDM compatible MDM (de)multiplexing technique which provides higher aggregate band-width.

The NI comprises of electrical to optical(E/O) and optical to electrical(O/E) converter, adaptive multiplexer and an electronic controller(Fig.3.4). The E/O converter and the O/E converter are simply ring based modulators and receivers. The Adaptive multiplexer includes the modelocked laser along with the MRR and waveguide arrangement facilitating (Fig.3.5) mode division multiplexing [28]. We have shown

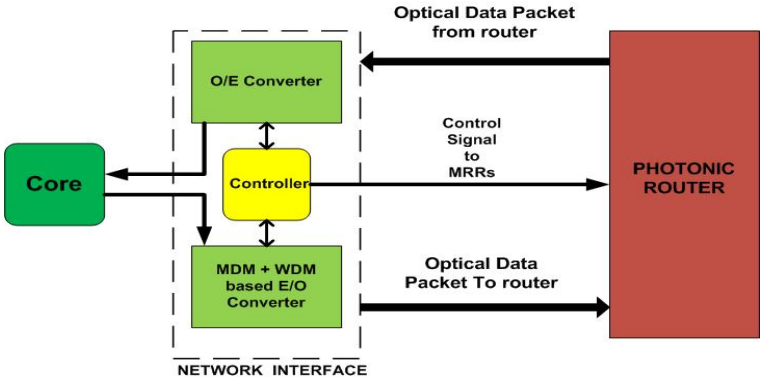


Figure 3.4: MDM integrated network-interface

two MRRs for MDM as we are using two modes per wavelength in our experiments. As we have mentioned in the previous section the electronic controller controls the adaptive multiplexing too. It controls which MRR need to turn on in the MDM arrangement to send the message along the preferred mode. The electrical controller works on the basis of algorithm depicted in Algorithm 1. The algorithm controls the wavelength and mode selection mechanism during message passing as follows. When the route to be followed is empty i.e it is not occupied by any other optical signal, the controller switches on MRR_0 which selects wavelength λ_0 and mode TE_0 transmitted by mode-locked laser for communication. When the route is occupied by certain mode of a specific wavelength then with the help of time-division-multiplexing a certain amount of time lag is incorporated while transmitting the next signal in a different mode so that it won't interfere in the transmission of the previous optical signal occupying the route.

Fig.3.6 illustrates how signals of different modes are transmitted with a time lag as determined by the algorithm, hence facilitating *mode-wavelength-time* division multiplexing. All the signals are carried by the same multimodal transmission waveguide with modulated signals coming from a common single mode fiber. So

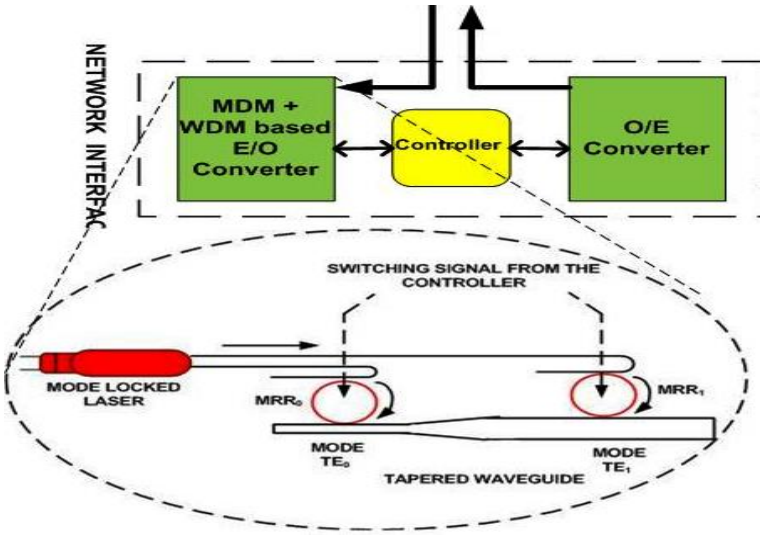


Figure 3.5: Modelocked laser employing MDM

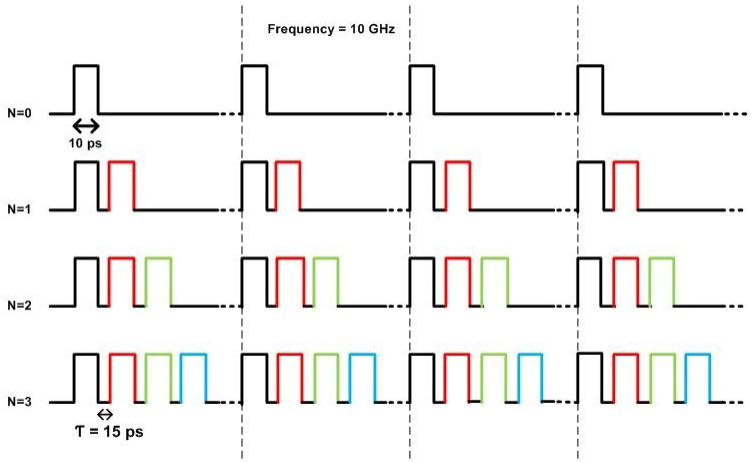


Figure 3.6: Black pulse=TE_0 of λ_0, red pulse=TE_1 of λ_0, green pulse=TE_0 of λ_1, blue pulse=TE_1 of λ_1. Timing diagram of TDM integrated mode-division-multiplexing

while selecting the appropriate combination of wavelength and mode it provides a time delay in turning on the corresponding multiplexing MRR. In our proposed design we have taken this time lag to be approx. 15ps as the switching delay of MRR is 5-10ps.

Algorithm 1 Controller Algorithm for adaptive mode division multiplexing

procedure CORE1 WANTS TO SEND DATA TO CORE2
N = no. of signals transmitting fully or partially along the path
Control packet checks for the shortest available path using electrical routing
if (N=0) **then**
Switch ON MRR_0 with λ_0
Send signal from Mode-Locked Laser
if (N=1) and (mode = TE_0) **then**
Switch ON MRR_1 with λ_0
Send signal from Mode-Locked Laser with a (τ+pulse-width) delay
if (N=2) **then**
Switch ON MRR_0 with λ_1
Send signal from Mode-Locked Laser with a 2(τ+pulse-width) delay
if (N=3) and (mode = TE_0) **then**
Switch ON MRR_1 with λ_1
Send signal from Mode-Locked Laser with a 3(τ+pulse-width) delay

4. EXPERIMENTS AND RESULTS*

4.1 Experiment

IPKISS [41] platform has been used for the design and simulation of the photonic router. The tool allows the photonic component layout design, virtual fabrication of components in different technologies, physical simulation of components, and optical circuit design and simulation. We custom-designed some photonic components such as MRR, waveguide, mode-locked laser, tapered waveguide, and photodiode required for the router. After checking the design rules, we proposed the design of photonic NoC in this work. In order to validate the proposed micro-architecture we built a cycle accurate network simulator with required infrastructure to run both synthetic workloads and PARSEC benchmark traffic.

4.1.1 Microarchitecture Simulation on IPKISS

We optimized the desired parameters of the optical components and validated them prior to using them in the experiments. The design parameters adopted to carry out various experiments are depicted in TABLE 4.1. We restricted the width of the multimodal transmission waveguide such as to support two optical modes TE_0 and TE_1 along with multiple wavelengths. Though with varying width the waveguide can support more no. of modes, but we're considering modes TE_0 and TE_1 as the proposed MDM scheme supports 2 modes (Fig.3.5).Using the fundamental optical components, we built the router in IPKISS and performed the physical simulation.

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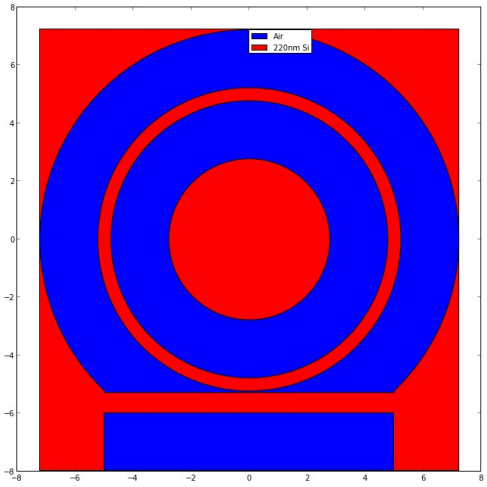
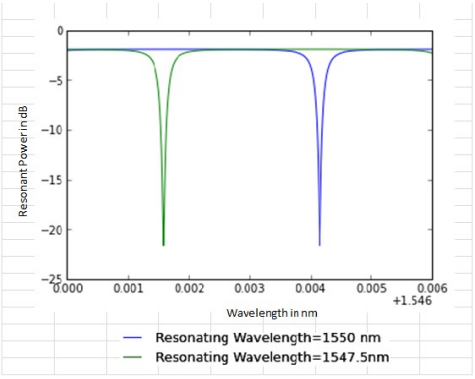
Table 4.1: Design parameters for experimental setup

Design Parameters	Value
MRR diameter(D)	5μm
Waveguide(MRR) width	1.5μm
Photodetector Area(A_{det})	20μm^2
Refractive index Of waveguides	2.46
Pulse-width of Optical Signal	10ps
Frequency(mode-locked laser)	10GHz
Wavelength	1547.5nm and 1550nm

Virtual fabrication of various optical components e.g the MRR(Fig.4.1a) were done taking into consideration the design rules. MRRs and waveguides were integrated to virtually fabricate the router. After fabrication, we carried out simulation using CAMFR [41]. It provided the refractive index profile and optical transmission profile of the fabricated design. Uniform refractive index across the router is a must for ripple free photonic transmission. After testing the uniformity of refractive index across the router, we simulated the router in CAPHE [41]. CAPHE is an optical circuit simulator for time-domain and frequency-domain analysis. It is also used to evaluate insertion loss in an optical circuit. The insertion loss in the MRR was found to be 0.12dB. Each MRR can be tuned to multiple wavelengths. The proposed router takes into account the wavelengths of 1547.5nm and 1550nm(Fig.4.1b) for MRR switching as these are the most suitable wavelengths(in terms of performance) for silicon photonic waveguides [11].



(a) Virtually fabricated MRR



(b) Resonating wavelengths

Figure 4.1: IPKISS simulation results

4.1.2 Micro-architecture Validation Under Traffic

In order to validate the proposed router microarchitecture we built a systemC based cycle accurate network simulator inspired from widely used Noxim simulator[35]. We implemented the MDM+WDM+TDM based photonic router along with circuit switching scheme in the simulator called Photonoxim. We took 2D mesh as the network topology to study the behavior of the network architecture under various kinds of synthetic traffics. We also validated our micro-architecture under PARSEC benchmark traces. We fixed the PNoC chip frequency at 1GHz. We compared our circuit-switched proposed PNoC with packet-switched 45nm electronic NoC in a 2D mesh topology for same amount of simulation cycles under various kind of synthetic as well as benchmark traffics.

4.2 Comparative Analysis and Results

A comparative analysis of the proposed router with the most recent designs such as the λ-router, crossbar router, cygnus router [24], and the columbian router [27] was

carried out. We analyzed important parameters of all these routers like the required number of MRRs, optical insertion losses, and power consumptions. We adopted the information on crossbar router from [24]. 2D topology based NoCs generally require 5×5 routers. But λ-router does not support odd number of input and output ports. Hence we have considered a 6×6 λ-router in which one pair of input output ports remain idle.

4.2.1 Number of MRRs

The number of MRRs used in a router microarchitecture determines the area overhead of router. Reducing the number of MRRs will lower the chip area and also decrease the resultant energy consumption. This will eventually reduce the chip cost. We compared the number of MRRs used to design each of the photonic routers. The proposed router uses 18 MRRs [16 for routing and 2 for MDM]. It is

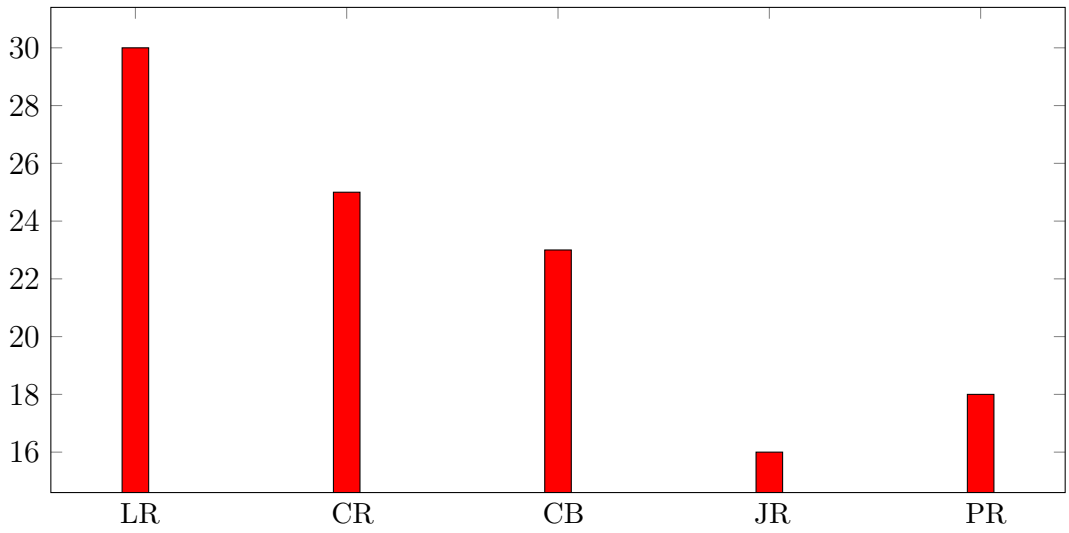


Figure 4.2: Comparing number of MRRs/router for different PNoC architectures; LR=λ-Router, CR=Columbian Router, CB=Crossbar Router, JR= Ji-Router, PR=Proposed Router

40% lesser than the λ-router. Fig.4.2 represents the number of MRRs used in each of the routers. We have denoted router proposed in [31] as Ji-router for simplicity. The graph clearly shows that the proposed router outperforms all its counterparts except Ji-router in-terms of number of MRRs. Though Ji-Router uses fewer number of MRRs than the proposed architecture, it is not scalable because of its higher insertion loss due to more no. of waveguide crossings and it does not support higher throughput performance.

4.2.2 Photonic Area Overhead

There are several optical components involved in silicon photonics NoC. These includes modulators, waveguides, switches, filters and photodetectors. The area occupancy of a given photonic NoC can be calculated as the sum of the area of each of the individual component on the silicon die. For our analysis we assume the following :-

1- All the ring resonators are of the same size

2- The ring modulators in the transmitter are made up of one active ring resonator

3- The (de)multiplexers consist of two active ring resonators(as for our experiments we have taken two modes into consideration)

4- The reciever includes a passive ring resonator based filter and a photodetector.

We used the area overhead calculation formula proposed by Abadal et al in [14]. According to it the area of a given PNoC architecture given the previous assumptions can be approximated as:

$$A \approx N_{ring}A_{ring} + N_{det}A_{det} + \sum_{i} A_{wg,i} \tag{4.1}$$

Here, A represents area of chip occupied by photonic components, N_{ring} represents total number of MRRs, A_{ring} is the area of each MRR, N_{det} is the total number of

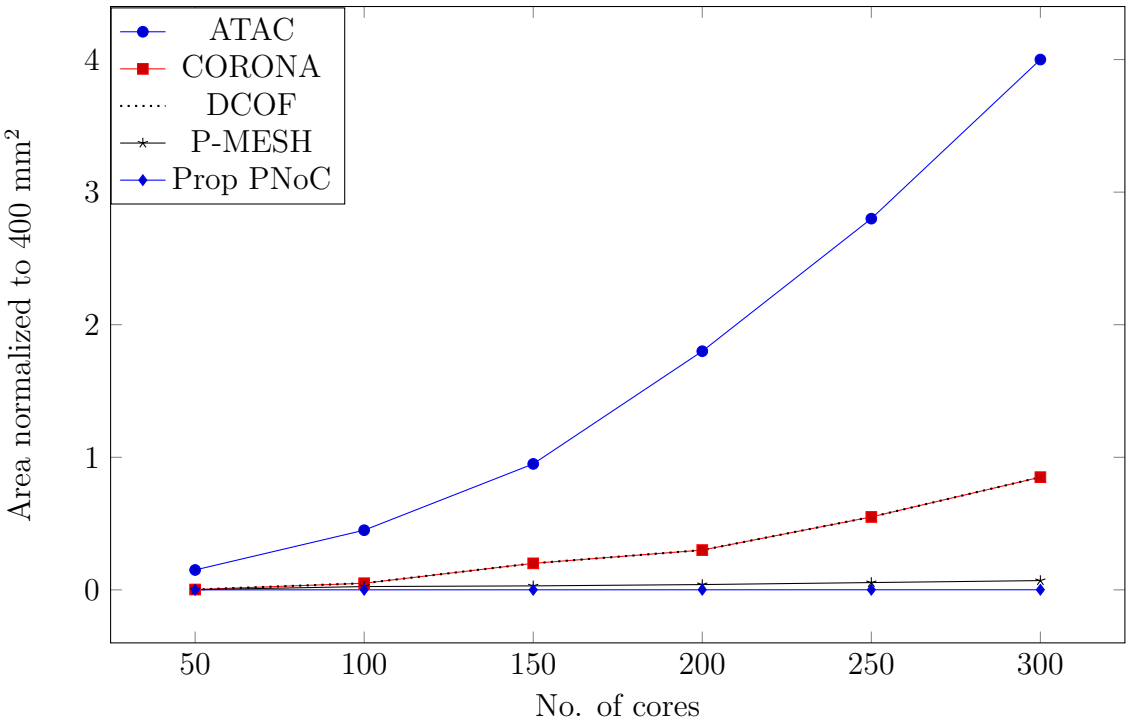


Figure 4.3: Area overhead of different PNoC architectures with varying sizes

photodetector, A_{det} represents area of each photodetectors, and A_{wg} is area of each waveguide. A_{ring} can be calculated using equation 4.2. We took the parameter values mentioned in Table.4.1 for calculating the area overhead.

$$A_{ring} = \frac{\pi D^2}{4} \tag{4.2}$$

Table 4.1 shows the design parameters used for this analysis. We have taken into account ATAC[1], CORONA[9], DCOF[30] and P-MESH[26] along with the proposed design for area-overhead analysis. Fig.4.3 shows the area footprint of each configuration evaluated as a function of the number of cores. It has been normalized to the area of a 400 mm^2 chip. From the graph, it is clearly evident that the proposed

PNoC architecture is the most scalable in terms of area evolution as compared to all others. The number of modes which we can support in a multimode fiber for increasing the aggregate bandwidth depends on the width of the transmission waveguide. So with increase in the no of modes, the area overhead increases too, but we can always make a trade off between the area overhead and the performance we seek.

4.2.3 Average Throughput

Throughput is a parameter that measures the rate at which message traffic can be sent across a communication network. According to [34] it is defined as:-

$$Average\ Throughput = \frac{(number\ of\ messages\ transmitted)*(message\ length)}{(number\ of\ IP\ blocks)*(total\ time)} \quad (4.3)$$

In order to validate the performance of the proposed PNoC against other NoC architectures, we simulated some synthetic traffics and PARSEC benchmark applications in Photonoxim.

4.2.3.1 Comparison Between Electrical NoC and Proposed PNoC

As mentioned before for transmission of messages we adopt WDM+MDM+TDM based circuit switching photonic circuit. Since electrical signals are fundamentally limited with their bandwidth, a larger capacity can be achieved only by increasing no of parallel wires between the source and destination. With the help of mode division multiplexing in photonic circuits we can have multiple channels with the help of multiple modes and wavelengths. From the analysis it is quite clear that from the average throughput point of view electrical NoCs are easily trumped by photonic circuits. We still ran some synthetic traffics both through a packet switching 45nm electrical NoC and the proposed PNoC. We kept the number of simulation cycles, packet injection rate and the no of cores same for both experiments.

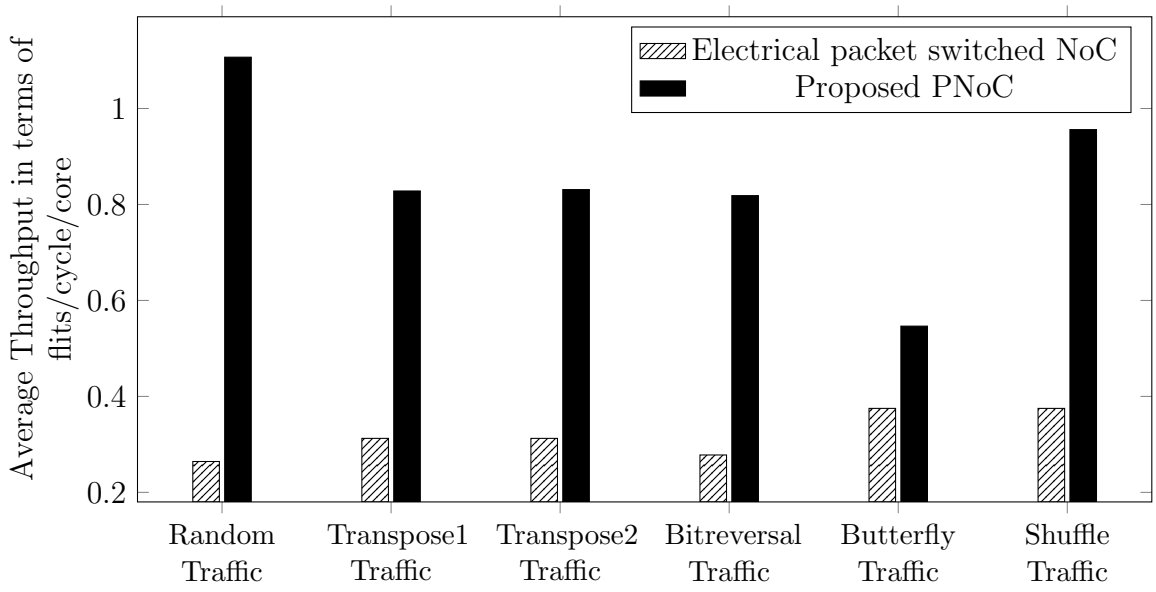


Figure 4.4: Comparison of average throughput between electrical NoC and proposed PNoC with various synthetic traffics

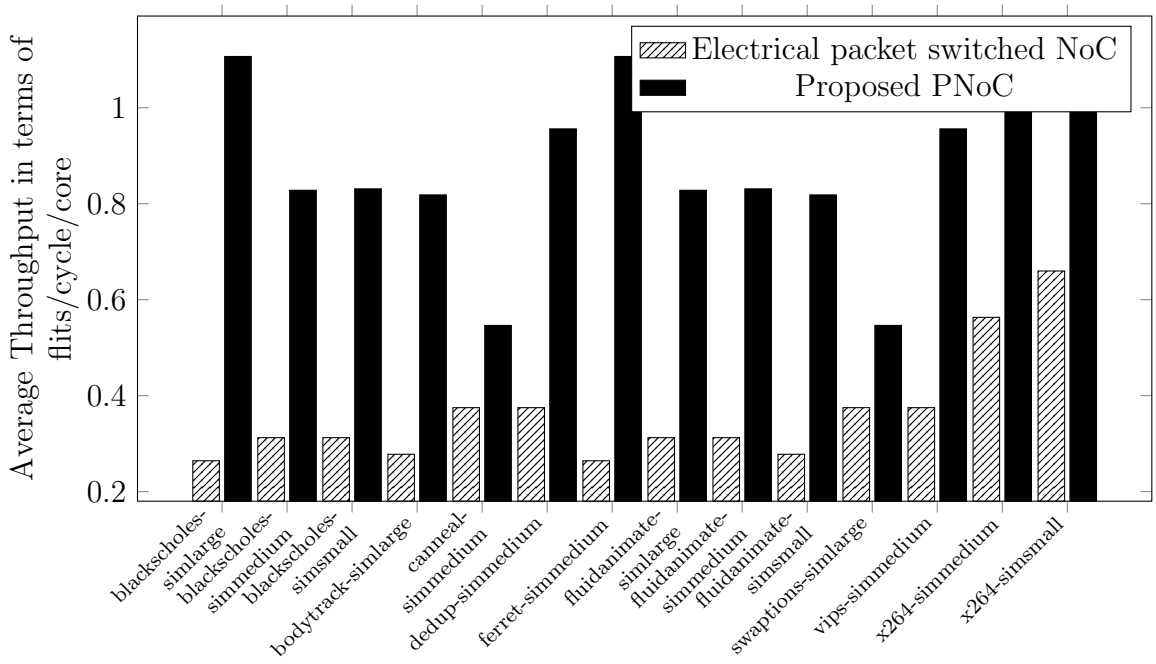


Figure 4.5: Comparison of average throughput between electrical NoC and proposed PNoC with PARSEC benchmark

Fig.4.4 represents the Average Throughput/cycle/core for different types of synthetic traffics. From Fig.4.4 it is quite evident that the average throughput of proposed PNoC is about 4 times better than that of electrical NoCs. It is not only for the fact that there are more parallel channels(modes) but also that the average latency of the proposed PNoC is less than the traditional electrical NoC. For testing under some real world traffic we built the infrastructure in both NOXIM and PHOTONOXIM to run some PARSEC benchmark applications. Fig.4.5 reiterates the fact that we inferred from running synthetic traffics earlier. This proves photonic NoCs to be the biggest contenders in replacing electrical NoCs for high throughput on-chip communication.

4.2.3.2 Proposed PNoC Architecture vs Other PNoC Architectures

Several PNoC architectures have been proposed in the recent past[26][5][8]. But none of them have demonstrated detailed simulation results except [36].

4.2.3.3 Bandwidth Comparison

The comparison metric bandwidth/Area-overhead quantifies the performance in terms of design efficiency. The crossbar architecture performance can be boosted with an increase in the no. of photonic components. But a high performance scalable architecture is necessary to cater to the needs of future generation CMPs. The proposed PNoC architecture can provide multiple transmission channels within the same multimodal waveguide facilitating higher bandwidth with a smaller footprint as compared to other proposed PNoC architectures.

4.2.4 Energy Consumption

The total energy consumption in a PNoC architecture is the sum of power consumed by the electrical controller and the power dissipated in the photonic switching

fabric. The total power can be expressed as follows:

$$E_{PNoC-total} = E_{Electrical} + E_{Optical} \tag{4.4}$$

The total optical energy over a full network can be governed by Equ.4.5.

$$E_{Optical} = E_{Laser} + \sum_{j=1}^{N}[(E_{E/O_i} + E_{O/E_j}) + K_i \times E_M] \tag{4.5}$$

Here, E_{Laser} is the total laser energy consumption over the full network cycles, K_i denotes total number of MRR switched on for packet 'i', and E_M represents energy consumed to swicth on an MRR. E_{Laser} and E_M are given by Equations 4.6 and 4.7 respectively.

$$E_{Laser} = \sum_{j=1}^{N} P_{Laser_j} \times T_j \tag{4.6}$$

$$E_M = P_M \times T_M \tag{4.7}$$

T_j in Equation. 4.6 refers to total ON time of $Laser_j$ whereas T_M represents time to switch on an MRR.

In order to compare different photonic routers we need to compare the energy consumption per bit of communication. The power calculation without taking into the laser power into consideration is as follows :-

1) E/O converter - It is basically a ring modulator

2) Mode (de)multiplexing MRR

3) Switching MRR - The MRR on a path need to be turned on to bend the propagation of light

4) O/E converter - It is also a ring based demodulator or receiver

We take E/O and O/E conversion time as 50 ps. Though we can take a lesser time but they will be bottlenecked by the electrical components of the control circuit. So we took a longer time duration in order to compensate for that.

ON duration for Mode (de)multiplexing MRR: 20ps

ON duration for Switching MRR: 20ps

Energy consumption in E/O and O/E : 2*[50ps * 20μJ] = 2.0 fJ

One MRR turning on each for multiplexing and demultiplexing = 2* 20ps * 20μJ = 0.8 fJ

One MRR switching in XY: 20ps * 20μJ = 0.4 fJ

Total energy consumption in communicating one bit of data: 2.0+0.4+0.4=3.2 fJ

Laser is the most significant power consuming unit in a PNoC architecture. While ensuring the power of the laser we have to take into consideration all the losses that an optical signal incurs while propagating from source to the destination. We have to ensure a reasonable strength of the signal at the receiver end after signal degradation. The losses include on-chip coupling loss, MRR coupling loss and pass loss and waveguide bending and propagation loss. The various loss values and the Photodetector sensitivity is given in Table 4.2. We won't be considering waveguide propagation loss as it is negligible.

Table 4.2: Optical losses

Parameters	Value	Units
MRR drop loss	1	dB
MRR pass loss	0.01	dB
Waveguide bending loss	0.15	dB/bend
(De)modulation loss	3	dB
On-chip coupling loss	1	dB
Photodetector sensitivity	-30	dBm
Laser efficiency	8	%

$$Loss\ in\ dB = 10 \log \frac{P_{in}}{P_{out}} \tag{4.8}$$

$$P_{in} = P_{out} * 10^{\frac{Loss\ in\ dB}{10}} \tag{4.9}$$

For the whole trasmission path, in Equation.4.8 P_{in} is the laser power and P_{out} is the receiver power. The photodetector sensitivity is -30 dBm = 1μW. From the router layout, in the worst case scenario on an optical path there will be 16 waveguide bendings, 3 drop MRRs, 42 pass MRRs(for a 8×8 network), one MRR each for modulation and demodulation. After calculations and taking into consideration the worst case scenario, in a 8×8 mesh network the laser power needed to transmit a signal from source to destination comes to 239.2875 μW.

4.2.4.1 Electrical NoC vs Proposed PNoC

The electrical global control and data wires consume significant power during signal communication and arbitration. In comparison to components used in electrical

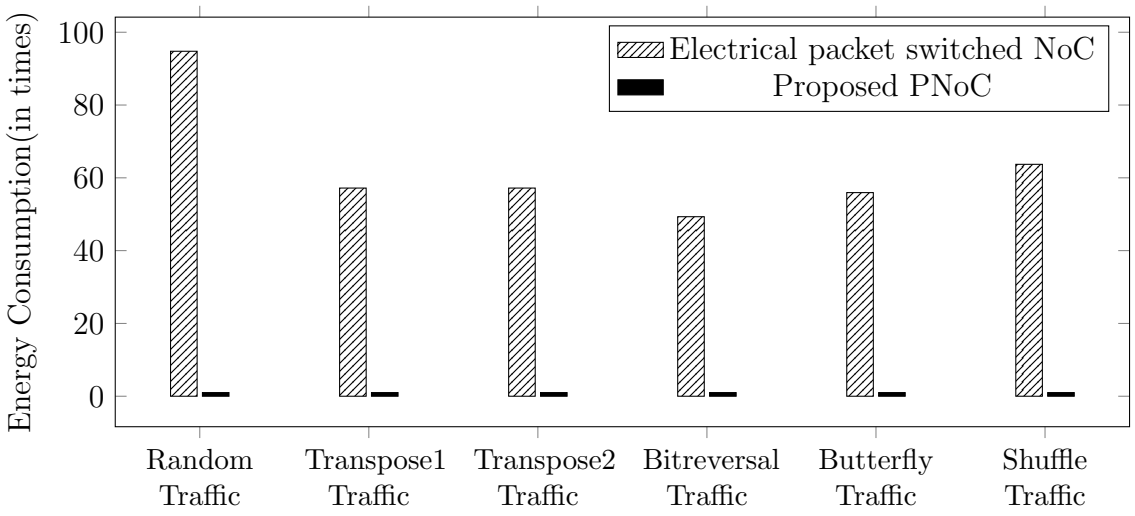


Figure 4.6: Energy consumption(synthetic traffic): electrical NoC vs proposed PNoC

NoC, optical components consume significantly less power. As we haven't taken into consideration the electrical arbitration power consumption in our proposed PNoC, it was justified not to let consider the arbitration power consumed in an electrical NoC while comparing the simulation results. We only measured the energy consumed during communication of the message packets. With a fixed packet injection rate and simulation cycles, we ran several synthetic as well as PARSEC benchmark application traffic through both electrical NoC and proposed PNoC. We plot the power consumed by the electrical NoC normal to the power consumed in the proposed PNoC for all the traffics. From Fig.4.6 and Fig.4.7 , it is clearly evident that the energy consumed in the proposed PNoC is about 55X-65X less than the electrical NoC under most of the traffic conditions.

4.2.4.2 Proposed PNoC Architecture vs Other PNoC Architectures

The other reported works on photonic router [24][31][27][33] lack details on electrical controller power analysis. Hence we have compared only the power consumption

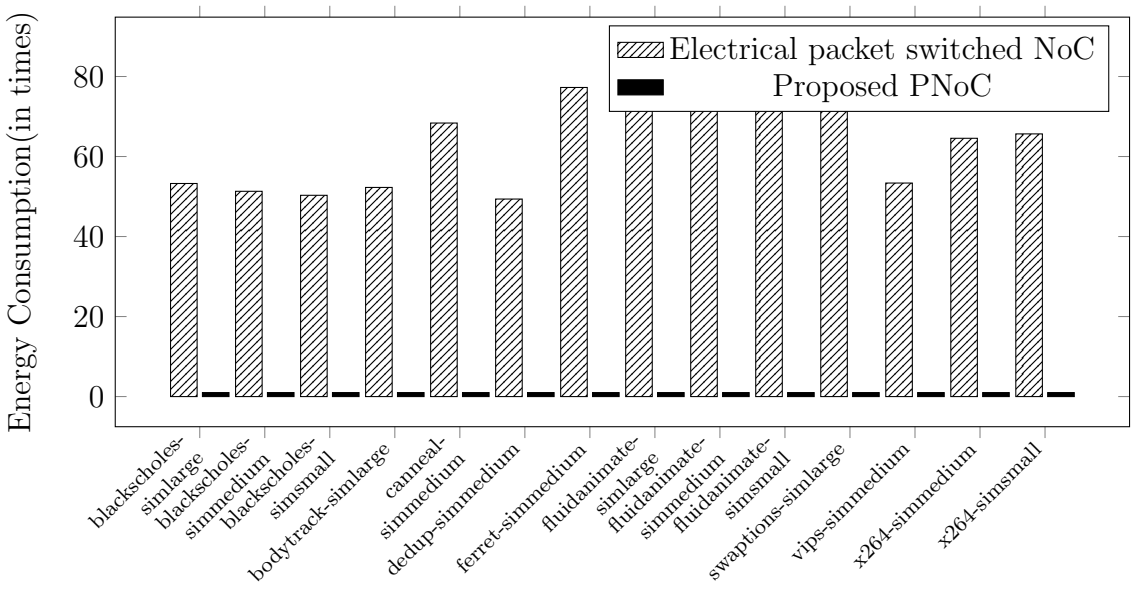


Figure 4.7: Normalized energy consumption(PARSEC benchmark): electrical NoC vs proposed PNoC

across the photonic switching fabric for a fair analysis. In the following, P_{router} represents power consumed by the photonic switching fabric. We are not considering the λ-router in the power analysis due to unavailability of data provided in the literature.

We analyzed the three other routers [24][31][27][33] as a part of 2D network and studied their impacts at network level. We analytically determined the energy consumption of the stated three photonic routers in a 8×8 2D mesh NoC using dimension order routing scheme. We evaluated the average energy consumption per optical path in the network [E_{path}] and also the average energy consumption per router [E_{router}]. We calculated E_{path} using equation(1). Here E_j represents the energy consumed on j-th path when the bandwidth is 'B'. 'P' represents the total number of photonic paths in the NoC. E_{router} is calculated using equation(2) where 'R' is the average number of photonic routers in all the optical paths.

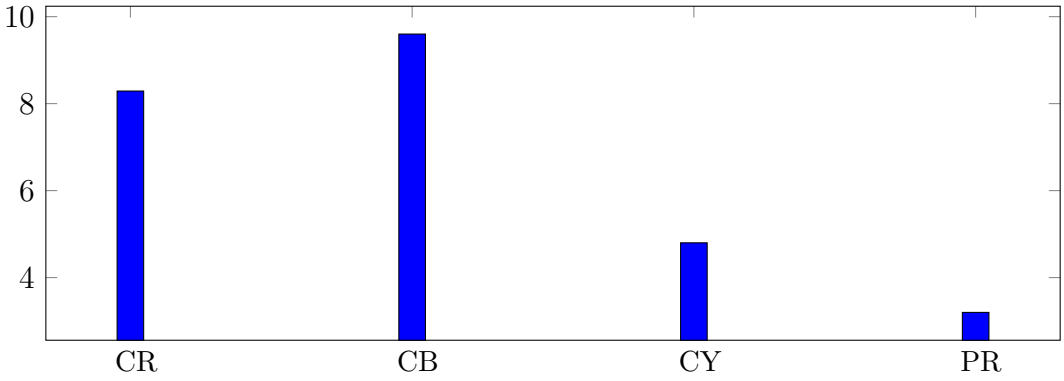


Figure 4.8: Comparison of average energy consumption per optical path, in fJ/bit

$$E_{path} = \frac{\sum_{j=1}^{P} E_j}{P \times B} \tag{4.10}$$

$$E_{router} = \frac{E_{path}}{R} \tag{4.11}$$

Network-level analysis shows that the proposed router consumes the lowest average energy per optical path, 3.2fJ/bit. It is 66.67% less than the crossbar router, 61.3% less than Columbian router and 33.3% less than Cygnus router as shown in Fig.4.8. According to network level analysis in[24], in the proposed router based 8×8 2D mesh network, the average no. of routers in an optical path is 6.315. Then from equation Eq.4.11 the average router energy consumption comes to be 0.51fJ/bit, which is 61.1% less than the crossbar router, 66.45% less than columbian router and 32.9% less than the cygnus router as shown in Fig.4.9. A deeper analysis shows that the maximum energy consumption of the proposed router is also 3.2fJ/bit irrespective of network size. As with dimension order routing the maximum no of MRRs to be turned on in order to transmit messages over a mesh network is closer to one. So the power consumption remains almost constant.

It was difficult to compare the simulation results of proposed PNoC architecture

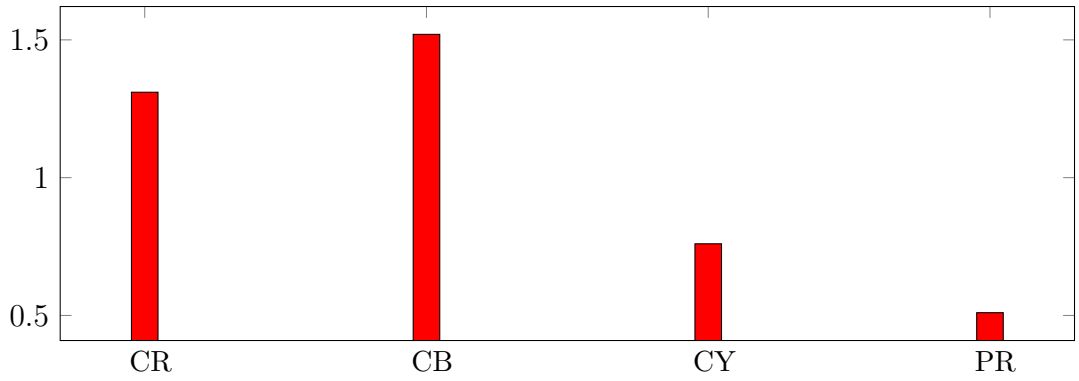


Figure 4.9: Comparison of energy consumption per router in fJ/bit

under synthetic and real benchmark traffics with other PNoC architectures such as Meteor and Corona due to lack of required information. As Meteor and Corona utilize electrical NoC both for local transfers and arbitration and the task distribution percentage is not mentioned in the corresponding papers for different traffics, it was difficult to figure out the normalization criteria and the actual energy consumption in photonic communication in each case.

The maximum power consumption of the proposed router based network on a given optical path is constant while using dimension order routing, regardless of the network size. The placement of the MRRs in the router takes care of the fact that no MRR is turned ON to transmit a message along a straight line. The router needs to switch on one MRR when a message enters the network from the NI, turns from a row to a column (and vice-versa), or exits the network to the NI. In the worst case, three MRRs need to be powered on to route a message in a network irrespective of the network size. This makes the proposed PNoC highly scalable without worrying about the power consumption in additional routers on a longer path. Fig.4.10 presents the average power consumption per optical path in NoC of different sizes.

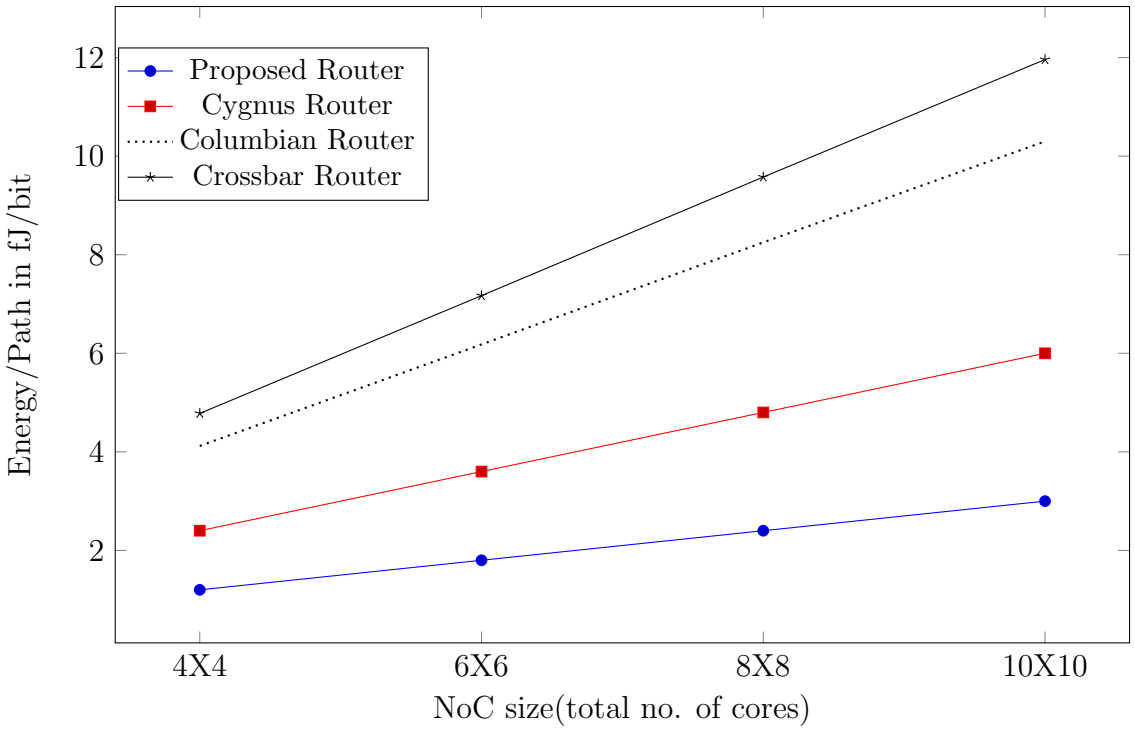


Figure 4.10: Average energy per path for different PNoC sizes

4.2.5 Optical Insertion Loss

Insertion loss plays a significant role in the amount of power consumption in a PNoC. Three major factors which contribute towards insertion loss are :-

1- Propagation loss- Signal power loss during propagation through waveguide.

2- Coupling Loss- It occurs during coupling of signals to and from MRRs.

3- Loss occurring due to waveguide crossing and bending.

Insertion loss of a router determines its feasibility and also the power required by the NI to transmit, and receive optical signals. We took MRR coupling loss equals 0.5dB[22]. A single waveguide crossing introduces an insertion loss of 0.12dB[24]. The waveguide propagation loss is 0.17dB/mm. As the hop length is of the order of µm, so it is negligible as compared to other losses.

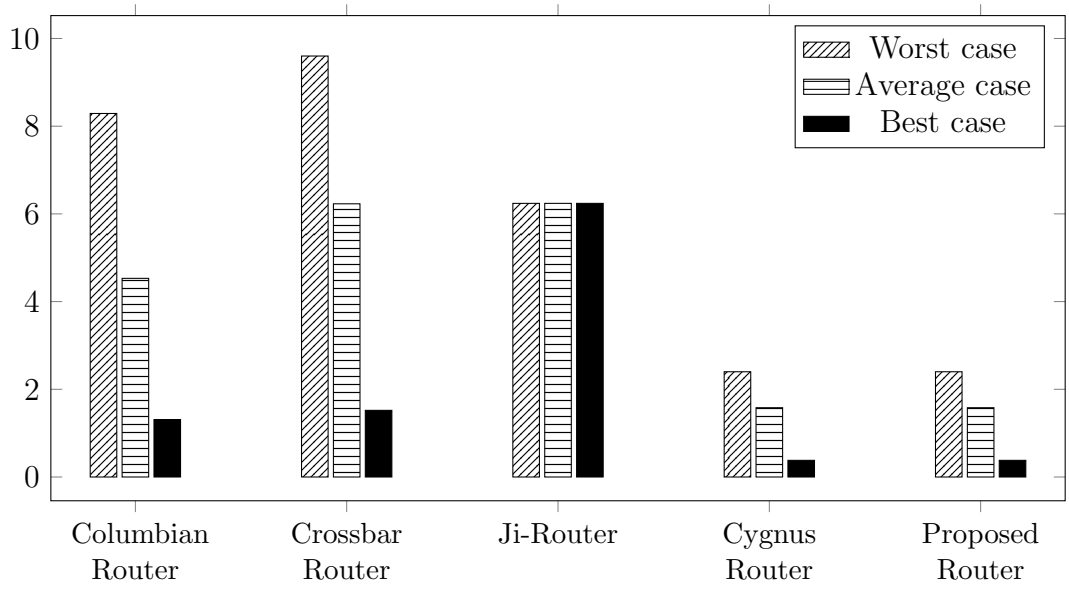


Figure 4.11: Insertion loss per router in dB

Insertion loss varies across input output pairs in a router. Hence we evaluated the best-case, average-case, and the worst-case insertion losses in all the routers. The results are shown in Fig. 4.11. It is clear from the figure that the proposed router has lowest insertion loss for all other cases except Cygnus router for which the insertion loss is same due to similar router layout. Compared to crossbar router, the proposed router has 61% lesser best-case loss, 43% lesser average-case loss, and 28% lesser worst-case loss. As the layout is based on the cygnus router layout, so the insertion loss for both the routers are same. In all the routers mentioned only loss during communication is taken into consideration. Losses are also encountered while modulating and multiplexing too. In mode division multiplexing the main cause of signal degradation is crosstalk. To reduce crosstalk we have to increase the coupling gap between multiplexing MRRs and transmission waveguide but it is done on the expense of performance. According to [28], it accounts for a very low($<$1.4dB) power penalty.

5. CONCLUSION AND FUTURE RESEARCH

The rising density of cores in the chip-multiprocessors era has reached a stage where widespread adoption of high performance PNoC is inevitable to facilitate the large demand for communication band-width with with low power consumption. The thesis implements a novel scalable, low-power, WDM- compatible mode division multiplexed, 5×5 non-blocking high performance MRR based photonic router.
We proposed a hybrid PNoC architecture which comprises of:-
1- a circuit switching photonic circuit for bulk data transmission
2- a packet switching based electronic control circuit for path set-up, (de)modulation and (de)multiplexing.

We designed a cycle accurate circuit switching simulator PHOTONOXIM, to validate the performance of the proposed PNoC under various traffic patterns. This thesis broadens the field of silicon photonic NoCs by introducing MDM along with WDM and TDM for the first time to increase the bandwidth about four times than the previous best reported results. By using minimal resources leading to a smaller footprint, it gives an insight into what the future NoC technologies have in store. The proposed design overpowers the traditional 45nm electrical NoC in almost every respect by providing a 4X boost in terms of bandwidth and a 55X-60X lesser power consumption depending on the traffic. As compared to other photonic routers, the proposed router provides almost 3 times higher throughput. The proposed hybrid router consumes 33.3% less energy per optical path and 32.9% less energy per router than the best reported results under uniform network traffic.

As silicon photonic components are susceptible to temperature change, further research is required to study the behavior of the PNoC under various traffics with

respect to temperature variations on chip. Multilayered PNoC architecures can be exploited to boost the performance while maintaining a smaller footprint. Laser is the most power hungry component in a PNoC. Research can be undertaken in terms of laser multiplexing or decreasing the no. of lasers in the proposed PNoC.

REFERENCES

[1] G. Kurian J. Miller J. Psota J. Eastep J. Liu J. Michel L. Kimerling & A. Agarwal. *"ATAC: A 1000-core cache-coherent processor with on-chip optical network"*, 19th International Conference on Parallel Architectures and Compilation Techniques, ACM, pages 477-488, 2010.

[2] D.Dai and J.E.Bowers. *"Silicon-based on-chip multiplexing technologies and devices for Peta-bit optical interconnects"*, Nanophotonics. Vol.3, Issue 4-5, pages 283-311, 2013.

[3] A.Alduino et al. *"Demonstration of a high speed 4-Channel integrated silicon photonics WDM link with hybrid silicon lasers in integrated photonics research, silicon and nanophotonics and photonics in switching"*, OSA Technical Digest (CD) (Optical Society of America, 2010), paper PDIWI5, 2010.

[4] A.Bianco et al. *"Scalability of optical interconnects based on microring resonators"*, IEEE Photon. Technol. Lett.22(15), pages 1081-1083, 2010.

[5] A.Joshi et al. *"Silicon-photonic clos networks for global on-chip communication"*, 3rd ACM/IEEE International Symposium on Networks-on-Chip, pages 124-133, 2009.

[6] A.Kazmierczak et al. *"Optimization of an integrated optical crossbar in SOI technology for optical networks on chip"*, Journal of Telecommunications & Information Technology, Vol. 2007 Issue 3, pages 109-114, 2007.

[7] A.Krishnamoorthy et al. *"Computer systems based on silicon photonic interconnects"*, Proceedings of the IEEE, Vol. 97, no. 7, pages 1337-1361, 2009.

[8] C.Batten et al. *"Building manycore processor-to-DRAM networks with monolithic silicon photonics"*, 16th IEEE Symposium on High Performance Interconnects, pages 21-30, 2008.

[9] D. Vantrease et al. *"Corona: system implications of emerging nanophotonic technology"*, 35th International Symposium on Computer Architecture, pages 153-164, 2008.

[10] G.Hendry et al. *"Time-division-multiplexed arbitration in silicon nanophotonic networks-on-chip for high-performance chip multiprocessors"*, Journal of Parallel and Distributed Computing, Vol.71, pages 641-650, 2011.

[11] G.Z.Mashanovich et al. *"Silicon photonic waveguides for different wavelength regions"*,Semicond. Sci. Technol. 23, 064002, 2008.

[12] M.Briere et al. *"System level assessment of an optical NoC in an MPSoC platform"*, Design, Automation & Test in Europe Conference & Exhibition, 2007.

[13] M.Horowitz et al. *"Scaling, power, and the future of CMOS"*, Electron Devices Meeting, IEDM Technical Digest. IEEE International , pages 7-15, 2005.

[14] S.Abadal et al. *"Area and laser power scalability analysis in photonic networks-on-chip"*, 17th International Conference on Optical Network Design and Modeling, pages 131-136, 2013.

[15] W.Bogaerts et al. *"Silicon microring resonators"*, Laser & Photonics Reviews 6, No. 1, pages 47-73, 2012.

[16] Y.Pan et al. *"Firefly: Illuminating future network-on-chip with nanophotonics"*, 36th International Symposium on Computer Architecture, 2009.

[17] Y.Xie et al. *"Crosstalk noise and bit error rate analysis for optical network-on-chip"*, 47th ACM/EDAC/IEEE Design Automation Conference, pages 657-660, 2010.

[18] A.W.Poon F.Xu and X.Luo. *"Cascaded active silicon microresonator array cross-connect circuits for WDM networks-on-chip"*, Proc. SPIE Int.Soc. Opt. Eng. 6898, 689812, 2008.

[19] G.T.Reed and A.P.Knights. *"Silicon photonics: An introduction"*, Ch. 4, pages 97-103 wiley, 2004.

[20] J.Leuthold R.Hess J.Eckner P.A.Besse & H.Melchior. *"Spatial mode filters realized with multimode interference couplers"*, Opt. Lett. 21, pages 836-838, 1996.

[21] H.Yingyan X.Guoyang & H.Seng-Tiong. *"An ultracompact optical mode order converter"*, Photonics Technology Letters, IEEE 18, pages 2281-2283, 2006.

[22] S.Xiao M.H.Khan H.Shen and M.Qi. *"Multiple channel silicon micro-resonator based filters for WDM application"*,Optics Express Vol 15 pages 7489-7498, 2007.

[23] http://www.itrs.net/. *"The international technology roadmap for semiconductors"*, 2011.

[24] H.X.Gu K.H.Mo J.Xu and W.Zhang. *"A low-power low-cost optical router for optical networks-on-chip in multiprocessor systems-on-chip"*, IEEE Computer Society Annual Symposium on VLSI, pages 19-24, 2009.

[25] A.Shacham K.Bergman and L.P.Carloni. *"On the design of a photonic network-on-Chip"*, International Symposium on Networks-on-Chip, NOCS 2007, pages 53-64, 2007.

[26] A.Shacham K.Bergman and L.P.Carloni. *"Photonic networks-on-chip for future generations of chip multiprocessors"*, IEEE Trans. Comput.57(9), pages 1246-1260, 2008.

[27] A.Shacham B.G.Lee A.Biberman K.Bergman and L.P.Carloni. *"Photonic NoC for DMA communications in chip multiprocessors"*, Hot Interconnects, 2007.

[28] L.Luo N.Ophir C.Chen L.Gabrielli C.Poitras K.Bergmen and M.Lipson. *"WDM-compatible mode-division multiplexing on a silicon chip"*, Nature Communications 5, Article number:3069, 2014.

[29] Y.Kawaguchi & K.Tsutsumi. *"Mode multiplexing and demultiplexing devices using multimode interference couplers"*, Electron Lett 38, pages 1701-1702, 2002.

[30] C.Nitta M.Farrens and V.Akella. *"DCOF-An arbitration free directly connected optical fabric"*, IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Vol.2, no.2, pages 169-182, 2012.

[31] R.Ji L.Yang L.Zhang Y.Tian J.Ding H.Chen Y.Lu P.Zhou and W.Jhu. *"Five-port optical router for photonic networks-on-chip"*, Optics Express, Vol. 19, Issue 21, pages 20258-20268, 2011.

[32] R. Ramaswami and K.N. Sivarajan. *"Optical networks:A practical perspective"*, IEEE Computer Society Annual Symposium on VLSI, 2002.

[33] G.F.Fan R.Orobtchouk and J.M.Fedeli. *"Highly integrated optical 8x8 lambda-router in silicon-on-insulator technology: Comparison between the ring and racetrack configuration"*,Silicon Photonics and Photonic Integrated Circuits II, 77190F, 2010.

[34] P.P.Pande C.Grecu M.Jones A.Ivanov & R.Saleh. *"Performance evaluation and design trade-offs for network-on-chip interconnect architectures"*, IEEE Trans-

action on Computers, Vol.54, no.8, 2005.

[35] NOXIM: Network Simulator. *"http://noxim.sourceforge.net/"*.

[36] S.Bahirat & S.Pasricha. *"METEOR: Hybrid photonic ring-mesh network-on-chip for multicore architectures"*, ACM Transactions on Embedded Computing Systems (TECS) - Special Issue on Design Challenges for Many-Core Processors,Vol. 13 Issue 3s, March 2014 Article no. 116, 2014.

[37] C.H.Liu Y.C.Chang T.B.Norris and Z.Zhong. *"Graphene photodetectors with ultra-broadband and high responsivity at room temperature"*, Nature Nanotechnology 9, pages 273-278, 2014.

[38] T.Mudge. *"Power: A first-class architectural design constraint"*, IEEE Computer, pages 684-689, 2001.

[39] S.Bagheri & W.Green. *"Silicon-on-insulator mode-selective add-drop unit for on-chip mode division multiplexing"*, 6th IEEE International Conference on Group IV Photonics, 2009.

[40] W.J.Dally and B.Towles. *"Route packets, not wires: on-chip interconnection networks"*, Design Automation Conference Proceedings, Vol.34, no.4, pages 52-58, 2001.

[41] www.ipkiss.org. *"IPKISS - a generic and modular software framework for parametric design"*.