A NOVEL SINGLE-PHASE GRID-CONNECTED PV INVERTER SYSTEM

A Dissertation

by

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ABSTRACT

Renewable energy sources, especially solar energy, continue to gain popularity and are ready to become a significant part of global energy portfolio. Grid-connected inverter based distributed generator is becoming increasingly popular due to its advanced control flexibility. Power quality and reliability are attracting much attention in such systems. In order to meet requirements of future applications and maximize the value of inverter system, advanced inverter functions are expected to provide more functionalities. This dissertation proposes a novel single phase inverter system combining proposed advanced control schemes and active power decoupling technique.

This dissertation firstly investigates the existing power control schemes for single phase grid-connected inverter and then proposed an independent power control scheme, which is implemented in stationary reference frame. The synchronization function is combined in power loop directly to eliminate the use of conventional phase locked loop. The proposed controller with double-loop current controller based on proportional resonant compensator is proved to achieve good power tracking performance even under distorted grid conditions. Active damping function for resonant peak problem is also implemented in controller.

Inverter based distributed generators may operate in different conditions and transition between different operating conditions may result into voltage spikes across the local loads and inrush currents into the grid due to the failure of synchronization on point of common coupling voltage. In this dissertation, a novel control scheme based on

model predictive control is proposed for grid connected inverter to enable the capability to operate in both grid-connected and island conditions and the capability to seamless transfer between different conditions through proposed synchronization and phase adjustment algorithm. The auto-tuning strategy of weight factor is presented as well as the stability analysis on the system. Compared with the conventional methods, the proposed seamless transfer control strategy has simpler structure and exhibits good transient performance.

Double line frequency ripple power is inherent in single phase rectifiers and inverters and can be adverse to system performance. Therefore, numerous active power decoupling techniques have been introduced to decouple that. All existing active topologies are investigated. Comprehensive comparison is conducted on the minimum required capacitance for power decoupling, the dc voltage utilizations, the current stresses, the modulation complexity and even application evaluations except for power rating and component counts. Based on the investigations and generalized comparison results, a new active power decoupling circuit composed of dual buck converters is proposed together with its control and modulation strategy. The ripple power is stored in split dc link capacitors with high energy utilization. The proposed power decoupling circuit could reduce the storage capacitance needed. The proposed power decoupling circuit does not have shoot-through concern, thus it could enhance the overall system reliability and decoupling performance.

DEDICATION

My father; Yuqi Li, My mother; Meizhen Ji, My sister; Yun Li

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1. INTRODUCTION

1.1 Background and PV system outlook

Global warming and environmental pollution are nowadays two of the main worldwide concerns. The world is running out of non-renewable energy resources, consequently the need of using green energy sources gains more importance. With the higher penetrations of renewable energy, the CO2 emissions and world electricity generation will start decoupling after 2016 [1]. Wind energy and solar energy are considered to be the most popular renewable energy sources. Research and development, focused on each of these areas, are being carried out globally, with solar energy playing a leading role given the fact that is one of the cleanest and least expensive sources of energy [2, 3].

According to the statistics, electricity generated from renewable energy sources is growing rapidly and increases by over 7,000 TWh from 2011 to 2035, making up almost half of the increase in total generation all over the world [4]. Only in European, the Photovoltaic (PV) market in 66 countries potentially could have 250GW installed PV capacity by 2020 and 1.1TW capacity by 2030 [5, 6]. It is estimated by GTM research that the cumulative PV installation worldwide will reach 402 GW in the year of 2017 as shown in Figure 1[4]. The electricity produced from solar PV, in 2035, can rise to 950 TWh and reach up to 690GW, according to Figure 2[2].The PV industry is experiencing rapid growth and solar energy is highly promoted.

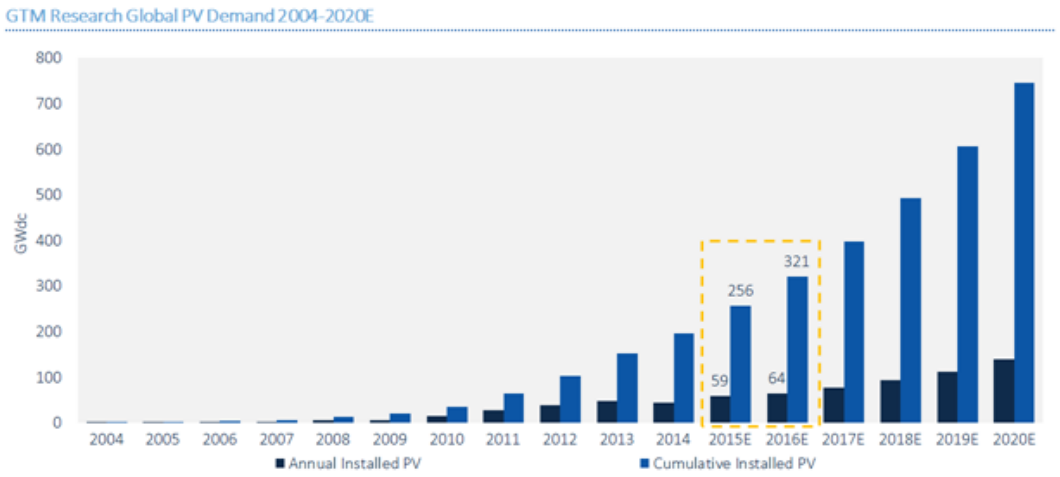


Figure 1: Research result on global PV demand (2004-2020) [4].

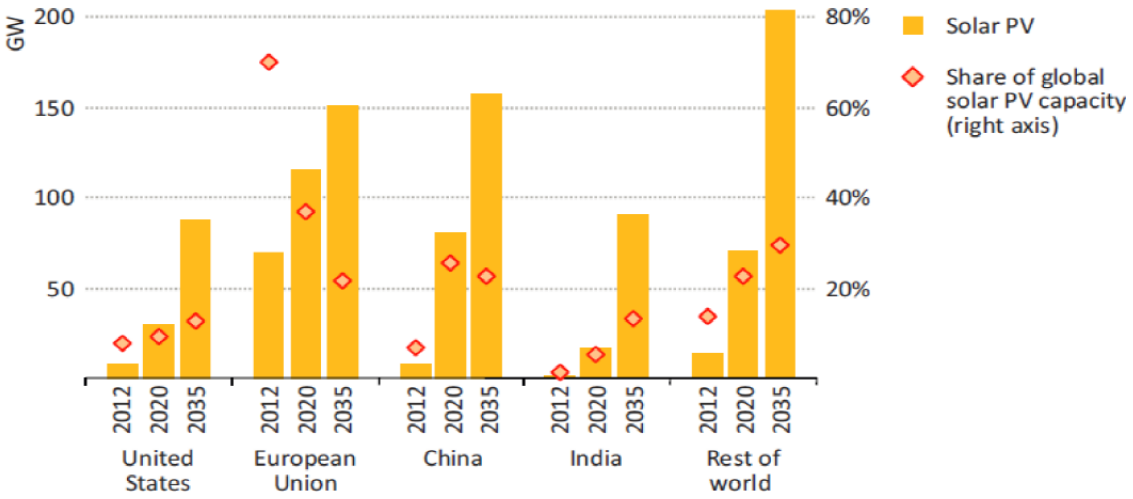


Figure 2: Installed solar PV capacity by region in New Policies Scenario of 2012, 2020 and 2035 [2].

Nevertheless, the high penetration level of PV systems especially imposes new challenges for the Distributed System Operators (DSO) and the end-consumers [5-8]. It may introduce significant impacts on the availability, quality and reliability of the

electrical grid, since it makes the distributed networks more decentralized, uncontrollable and heterogeneous[9-11], leading to discussions of appropriate adoption of PV power systems. Consequently, grid regulations are continuously updated so as to enhance the PV hosting capacity in distributed grids [8, 12]. On the other hand, it calls for an emerging development of advanced control strategies accordingly [13, 14].

Figure 3: The global PV inverter demand (2014-2020) [4].

Current active grid requirements are applied to both single phase and three-phase systems connected to grids for grid stability concern [5, 9]. The demands and new requirements are growing continuously with related standards newly updated and proposed. There are many demands on advanced functions in grid-connected power electronics facilities to improve power quality and reliability issues [13, 15-17]. Therefore, it is essential to explore the functions that inverter based power generating system can contribute to grid safety operation and assess the grid fault effects on the

control of grid-connected PV systems, and also to develop advanced control strategies to further enable an increase of the penetration degree of PV systems with cost-effective solutions. In addition, the basic requirements, related to active and reactive power output, frequency and voltage control, power quality and voltage stability, should also be fulfilled by every generating system [6, 10, 11, 14].

Grid-connected inverter plays the role of the interface between the renewable energy source or other distributed generation source and the grid, in order to best utilize the power and convert the voltage to the required level within specific requirements. Many topologies are proposed for this application [13, 18-24], including single stage, double stage and multi-stage topologies. In terms of isolation, it can be divided into isolated topology and non-isolated one. In terms of style of power source, it can be classified into voltage source inverter and current source inverter. Papers [13, 21, 23] summarize the present circuit topologies.

Since PV systems have a high penetration in residential applications with much lower power ratings (e.g. several kW) compared to wind turbine power systems, single-phase topologies are still widely-used solutions for PV applications at present, for distributed PV generator cases [24]. Notably, even for large-/utility- scale PV power plants, three single-phase configurations with center or string inverters are preferred by some industries for reliability concern [25-27].There continues to be a bright market for single phase PV inverter due to continuing increase in demand of micro-inverter and low power residential PV inverter. It is estimated by GTM research, as shown in Figure 3, PV inverter worldwide demand will reach 56000 MW in 2016[4].

Figure 4 and Figure 5 present the structure of two kinds of PV power systems structure for commercial or utility applications with central inverters. Figure 4 shows the conventional single-stage single-phase grid-connected PV power system with single phase voltage source inverter. This kind of system has simple structure, high efficiency

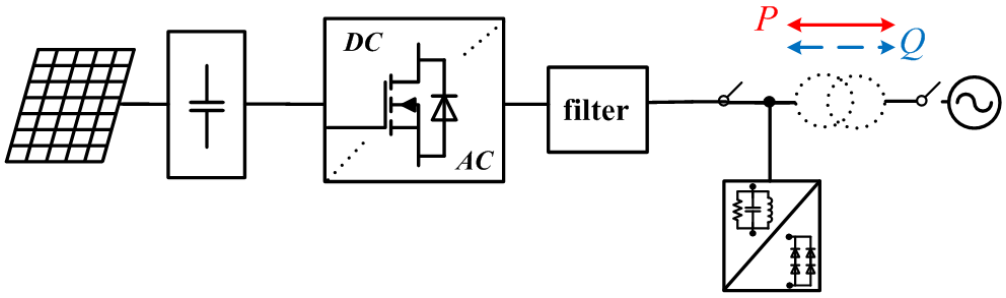


Figure 4: Single stage grid-connected PV generating system.

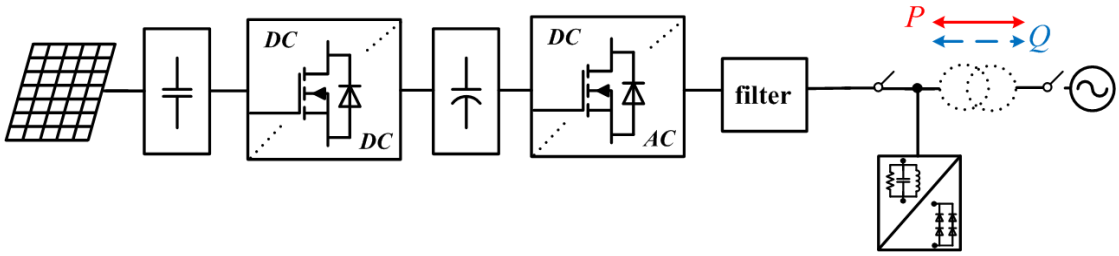


Figure 5: Double stage grid-connected PV generating system.

and dependent control between MPPT and inverter grid-connected control. Its required input dc voltage level is normally high, thus it is hard to use it with low voltage power source such as fuel cell, TEG and PV systems.

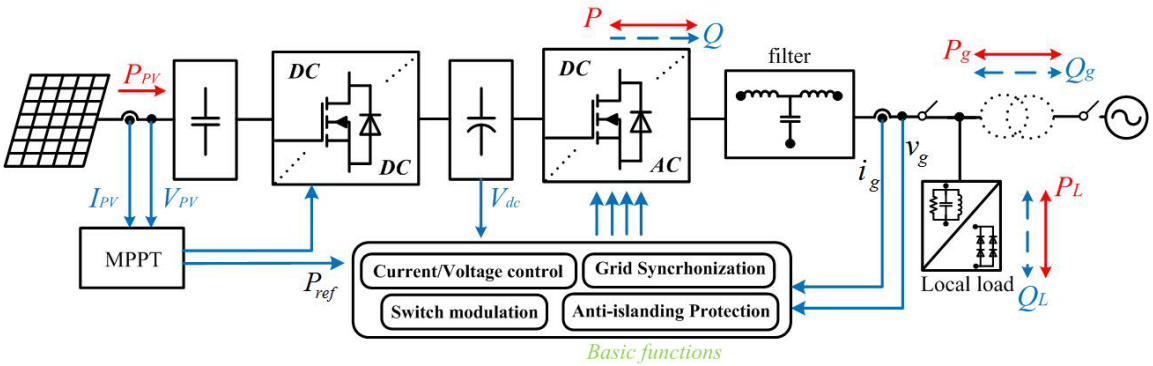


Figure 6: Structure of two stage PV generating system with basic control functions.

In PV or fuel cell system, the input voltage may have a relatively wide range. This single stage has no voltage boost front-stage. So it needs a big power rating to satisfy a wide range of operation points. The maximum power tracking strategy needed would be implemented directly through inverter to maximize output power of system.

Figure 5 shows another structure which is widely used as double stage power conditioner (dc-dc boost and dc-ac inverter). For the double stage configuration, the front stage can be boost converter, half bridge, full bridge, or other dc-dc converter. The front stage dc-dc converter can boost the input voltage to the required high DC link voltage, which allows the input voltage to vary in a wide range. In this case, the maximum power tracking strategy is normally implemented through front stage and the end stage is controlled with current (power) control with dc link regulation function to balance power flow.

A common central inverter is generally adopted for the residential or utility PV systems in order to achieve lower conversion losses and lower cost. Single phase topologies are more widely-used solutions for residential PV applications, where a DC-

DC converter is adopted to boost up the PV panel voltage to an acceptable range of the PV inverter, as it is shown in Figure 6. The boost converter also extends the operating time when the solar irradiation is very low, and offers the flexibility of extracting the maximum PV power (i.e. MPPT), which is an essential demand for PV systems. Single-phase grid-connected inverter is the main focus of this research. Its advanced control strategies and some inherent problems are studied and solved.

1.2 Opportunities and challenges

With more national objectives which have been initiated to solve the emerging energy crisis, more PV systems are expected to be installed and will be hooked up to the grid. The increased PV penetration makes the grid more decentralized and vulnerable. Power converter interface used in PV system provides high control flexibility and helps implement advanced functions with appropriate control. Control on power converter interface in distributed generator application comes to be important and attracts more attention, especially for those control functions to help maximize the system value and meet requirements of future application. Furthermore, in order to meet the grid code requirements, the future PV systems are expected to provide multiple functionalities similar to those of conventional power plants by means of offering ancillary services, such as reactive power support, peak power shaving, load leveling, frequency control through active power control, low voltage ride through during grid faults, and so on [28-41]. The power electronics interface of the PV systems enables an appropriate reactive power exchange with the grid, thus providing reactive power support and keeping the

bus voltages within operating limits. The control of voltages, reactive power and line flows represent one of the most important activities in the operation of modern electric utility system. This control is known as the "Voltage/Reactive Power" or "Voltage/Var" control. The main objective of this control can be generally regarded as an attempt to achieve an overall improvement of the system security, service quality and economy. The dynamic control on output reactive power of distributed generator is suggested and recommended in updated new standards, such as California Rule 21 [15] and IEEE 1547a Standard [42].

Power quality and reliability are attracting much attention in such systems. In order to meet the grid code requirements and maximize the value of inverter system, advanced inverter systems are expected to provide more functionality including ancillary services such as dynamic reactive power support [28-30]. The power electronics interface of the PV systems enables them to exchange reactive power with the utility grid. It is expected for the distributed generator (DG) system to supply continuous power to the local critical load, even in the abnormal grid conditions such as utility power outage [34, 35, 39]. When the grid recovers, the DG system should be able to reconnect to the grid and operate in grid-connected mode. Thus it is expected to enable the inverter system used for DG to have the capability to operate in both grid-connected condition and island condition. The transition between two aforementioned operating conditions may result in voltage spikes across the local loads and inrush currents into the grid due to mismatch in voltage frequency, phase, or amplitude [43, 44]. Therefore, it is important for the DG inverter system to be able to transfer seamlessly between operating

conditions to reduce voltage and current spikes. In order to synchronize the frequency and phase of grid voltage, phase locked loop (PLL) is commonly used [45-47]. PLL system needs extra efforts to design optimal parameters to get preferred performance and it could lead to adverse transient performance or bad distortion rejection capability if it is not designed specially [46, 48]. All these make PLL not suitable for the DG dual-mode inverters.

Many power control strategies for the single-phase inverter have been proposed [30-32]. Generally, the synchronous reference transformation and current component decoupling algorithm are used in control process, which complexes the control algorithm. It is highly expected to design a new control structure with simple structure and robust performance.

What's more, since single phase inverters are inherently subject to the double line frequency ripple power at both ac and dc sides, which could lead to adverse system performance. Active power decoupling techniques are desirable to replace bulky and short lifetime electrolytic capacitor with reliable film capacitor. Thus, different active power decoupling topologies, control and modulation strategies have been developed which show different characteristics on components counts, energy utilization and voltage/current ripple of energy storage components, dc voltage utilizations, and current stresses. Given the requirements of low cost, high reliability, high efficiency, high power density and easy-to-implement in the two stage PV micro-inverters, it is always necessary to evaluate the existing power decoupling techniques and find out appropriate solutions. For many existing active power decoupling circuits, at least one switching

phase leg with two separate power switches was used. It is known that cross conduction between switches could result into shoot through problem, which is the common failure mode of the circuit. Even though adding dead time could prevent its occurrence normally, but it may not work well in cases, especially during fault conditions. Thus, it would be better to find a way to overcome this problem to increase the reliability of the system.

1.3 Research motivation and objectives

Taking into account the new demands and challenges mentioned above mainly for single phase grid-connected inverter system, several issues will be addressed in this dissertation with proposed solutions and strategies. One objective of this dissertation is to improve the performance of single phase grid-connected inverter system and maximize its value in system, and consequently, advanced control strategies and active power decoupling circuit are proposed to further increase the penetration level of PV systems. The objectives and contributions of this dissertation are listed as follows.

- Propose an independent PQ control method without conventional PLL.
- Propose a grid-tied photovoltaic model predictive decoupled power control.
- Evaluated single phase grid-connected inverter operating in different modes and derived out a discrete power prediction model for MPC technique. Did the stability analysis on model predictive control for grid-tied inverter.
- Propose a controller with seamless transfer strategy for dual-mode inverter.

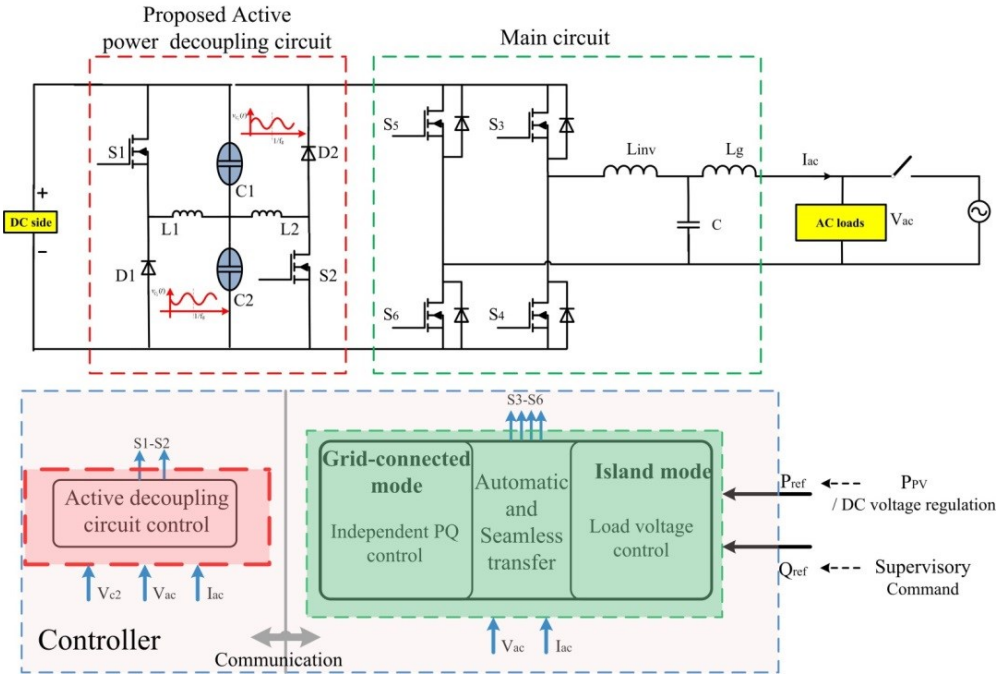


Figure 7: Structure of the proposed system.

- Reviewed existing active power decoupling topologies and compared in detail in many design aspects with a general structure.
- Proposed an active power decoupling circuit with its modulation and control strategy.

Figure 7 shows the structure of the proposed system combining these solutions. The main circuit is H-bridge grid-connected inverter. At the dc side, the proposed active power decoupling circuit is connected in parallel on the dc link. This kind of active power decoupling circuit is composed of dual buck circuit and split capacitors. In order

to achieve expected decoupling performance, a control strategy is proposed for this active power decoupling circuit. Moreover, a novel independent decoupled power control scheme is proposed for the single phase grid-connected inverter to control its output active and reactive power. Furthermore, a novel controller based on model predictive control is proposed to enable the single phase inverter to operate in both grid-connected condition and island condition with different control objectives based on system operation requirements and a newly proposed seamless transfer strategy to ensure its seamless transfer between different operating conditions. Analysis on each research part would be described and explained in detail in the dissertation. Their effectiveness is checked by both simulation and experiment, which is included in the dissertation.

1.4 Dissertation outline

The thesis consists of six sections.

In section 1, the research background, research motivation and objectives are introduced.

Section 2 studies power control methods for grid-connected inverter. Then, a simplified and robust controller for single-phase grid connected inverter with LCL filter is proposed. The synchronization function is directly combined in power loop to replace the function of PLL. A double-loop current controller with PR compensator and active damping function is implemented to achieve better dynamic performance and larger stability range in this paper. Reliable performance under various grid distortion cases, high-quality output current and decoupled real and reactive power control abilities of

inverter system are achieved in this way. The whole control system is implemented in stationary reference frame, which helps simplify the control algorithm.

Section 3 studies model predictive control (MPC) method and background of dual-mode grid-connected inverter and its seamless transfer operation. Then, a novel controller based on MPC method is proposed for grid-connected inverter with capability to operate in different conditions with different control objectives and capability to seamless transfer between conditions. In the grid-connected mode, the inverter system is controlled to regulate its output real and reactive power. This enables the decoupled and bidirectional power flow capability and suits for supporting ancillary service such as volt/var control. Compared to traditional method, this kind of direct power control method based on MPC has good dynamic performance and cycle-by-cycle current protection capability. With the SOGI module, the proposed controller can maintain reliable performance even under grid disturbances. Power prediction model was derived based on instantaneous power theory in stationary reference frame. At the same time, a synchronization algorithm is proposed to detect the phase angle of the grid voltage and produce the load voltage reference directly during the transfer process. A reconnection algorithm was proposed to ensure the seamless transfer during the transient from islanding mode to grid-connected mode. Compared with the conventional methods, the proposed seamless transfer control strategy is simpler and exhibits good transient performance. The impacts of weight factor in both islanding and grid-connected mode are analyzed as well as the stability issues. The effectiveness of the proposed seamless transfer control strategy is verified by both simulation and experimental results.

Section 4 studies the double line frequency ripple power problem in single phase system and numerous active power decoupling techniques. Comprehensive comparison on the minimum required capacitance for power decoupling, the dc voltage utilizations, the current stresses, the modulation complexity and even application evaluations except for power rating and component counts are conducted. All these aspects are critical considerations while choosing appropriate power decoupling techniques for different applications. In this section, the minimum capacitance to decouple the ripple power and the current stresses of power devices in the main circuit are derived in the light of different voltages across energy storage capacitors. By considering the ripple power paths, the dc voltage utilizations of both main circuit and power decoupling circuit are investigated. Combined other features towards component counts, modulation complexity, etc., the overall characteristics of different power decoupling techniques are compared and summarized to evaluate the performance in different applications effectively.

Section 5 presents a newly proposed active power decoupling circuit used for single phase system, which is composed of two separate buck converters operating in each half cycle and two split dc-link capacitors. The dc link capacitors can be used to store ripple power while supporting transient power to the main output. The capacitance needed is reduced largely by allowing high voltage fluctuation on capacitors, while the dc link voltage can be controlled with small fluctuation. The dc link capacitors can be fully charged and discharged with full energy utilization. The added power decoupling module does not need dead time, and totally eliminates the shoot through concerns,

which could enhance the system reliability. Another advantage of the proposed power decoupling method is that its control is independent with that of the main power stage. Modulation and control strategy are proposed for the power decoupling circuit. The operating principles together with parameters design are discussed in detail. Both simulation and experimental results prove the effectiveness of this method.

Section 6 presents the summary and future works.

Section 7 presents the references.

2. INDEPENDENT ACTIVE AND REACTIVE POWER CONTROL

2.1 Introduction

Interest in renewable energy resources like solar energy continues to gain popularity [5, 13]. However, higher penetration of these systems will likely necessitate the regulation of the active and reactive power produced to maintain high power quality and reliable operation of the electrical grid. Grid-connected inverters, especially those used in distributed generation (DG) system, are expected with independent active and reactive power control capability.

Figure 8 shows the model of power flow between two buses in the distribution system. Equation (1) and (2) represents the relationship of bus voltages and the active and reactive power flowing between them. Based on derived (3), it could be concluded that by changing the reactive power flowing between two buses, the bus voltage could be adjusted accordingly.

Dynamic reactive power output capability is also suggested and recommended in many newly updated standards, such as California rule 21 [15] and IEEE 1547a standard [42], for power converter interface of DG to help improve the power quality of local power system.

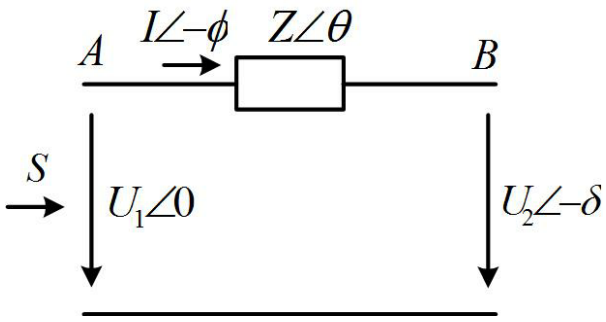


Figure 8: Model of power flow between two buses.

$$P = \frac{U_1^2}{Z}\cos\theta - \frac{U_1 U_2}{Z}\cos(\theta + \delta) \tag{1}$$

$$Q = \frac{U_1^2}{Z}\sin\theta - \frac{U_1 U_2}{Z}\sin(\theta + \delta) \tag{2}$$

$$U_1 - U_2 \cong \frac{XQ}{U_1} \tag{3}$$

Many power control strategies for the single-phase inverter have been proposed [28-32]. Figure 9 shows one kind of power control methods through calculation. This kind of power control method is implemented through current regulation. For this kind of method, the current reference value is calculated based on active and reactive power reference value. The modulation signal is created through combined inner current closed loop. This kind of method is simple to implement but has the drawback with large tracking error and weak distortion rejection capability [31]. Figure 10 shows the method called direct power control method. This kind of method is normally implemented through hysteresis control as shown in the Figure 10 or implemented by setting a look-up table about power reference values and switching vectors. But this kind of method

has drawbacks with variable switching frequency and lack of cycle by cycle current limiting capability [31].

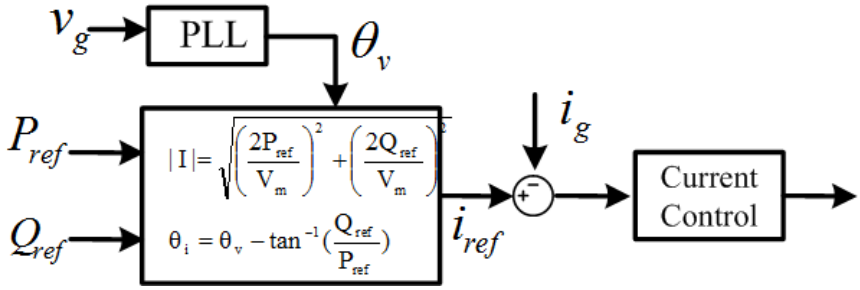


Figure 9: Power control method based on calculation.

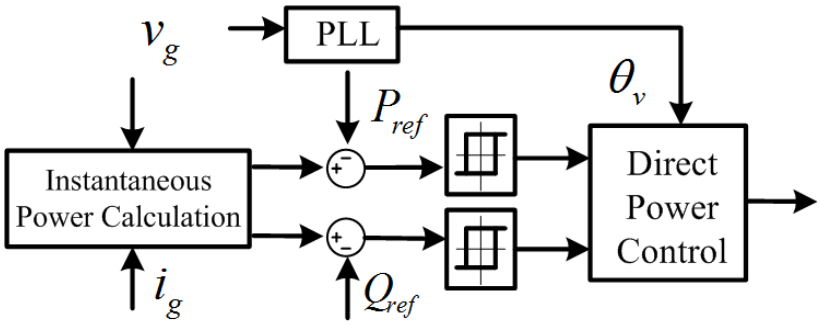


Figure 10: Direct power control method.

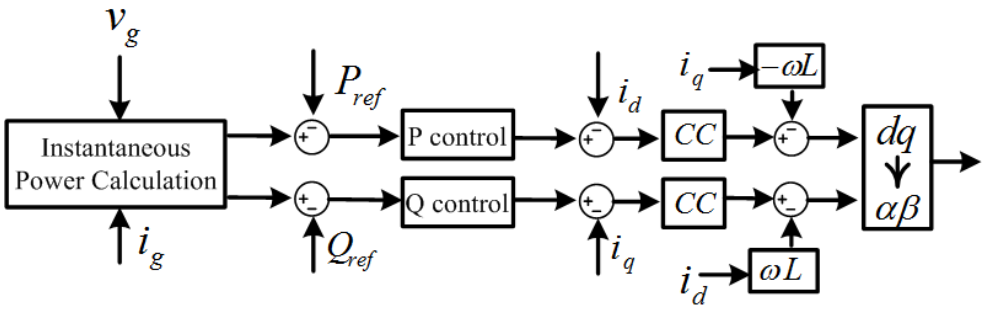


Figure 11: Power control method based on synchronous reference frame.

Figure 11 shows another method based on synchronization reference frame, which is also widely used for three phase application. Due to synchronous reference frame implementation, normally, transformations such as Park, Clark and their inverse transformations would be needed, which makes its implementation complex. Moreover, its power tracking performance depends highly on the exactness of detected phase angle of grid voltage. Generally, synchronous reference transformation and related decoupling algorithms are used in many existing methods. It comes with complex control algorithm [5-7]. And its performance depends largely on the exact amplitude and phase angle information of the AC mains voltage, which is normally captured by the Phase-Locked Loop (PLL). This creates additional drawbacks of the system and makes the system design complex due to the nonlinear loop control based characteristics of conventional PLL methods. Figure 12 shows the control block of a conventional PLL. It is composed of three parts, including phase detector, loop filter and voltage controlled oscillator. The literature combines filter in the loop to improve distortion rejection capability, but these filters normally introduce a delay [49]. To keep wide stability margins, the bandwidth should be reduced, degrading transient response. Thus, trade-off between dynamic response and distortion rejection capability would exist, as shown in Figure 13.

Furthermore, it is proved in [50, 51] that for a well-designed inverter control system, the PLL module decreases the phase margin of system, making the system to be less stable. This could be analyzed by deriving the block diagram of single phase inverter system with current loop as shown in Figure 15. The diagram of single phase grid-connected inverter with current control loop used for deriving process is show in

Figure 14. The equivalent circuit of system based on admittance model could be derived accordingly as shown in Figure 16. The grid inverter admittance can be equivalent to a model of the current loop admittance *Y_inv* in parallel with the negative admittance *Y_PLL*.

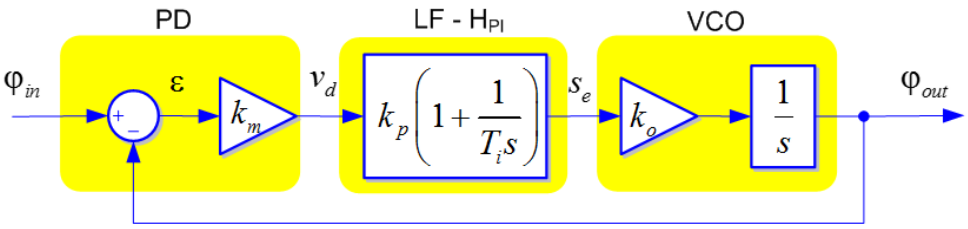


Figure 12: Control block of conventional PLL.

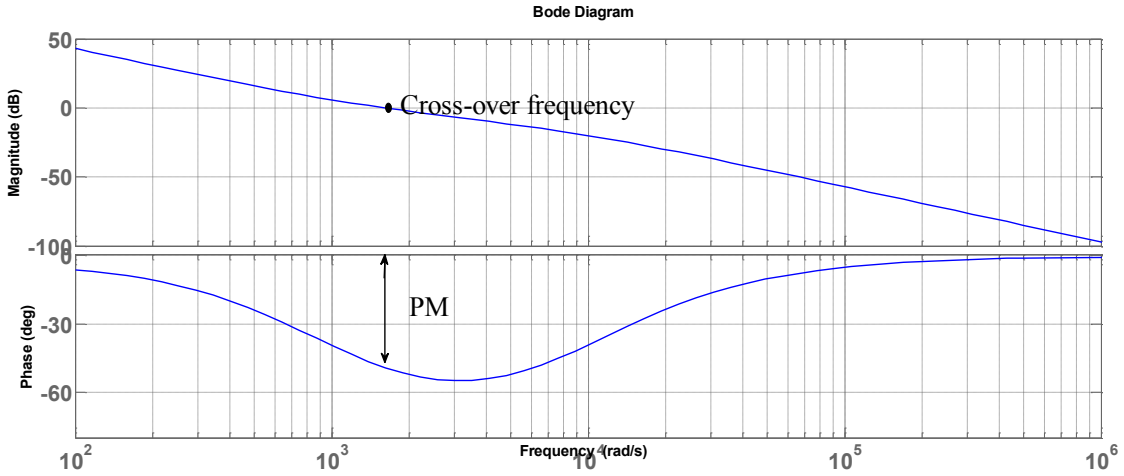


Figure 13: Frequency response of PLL.

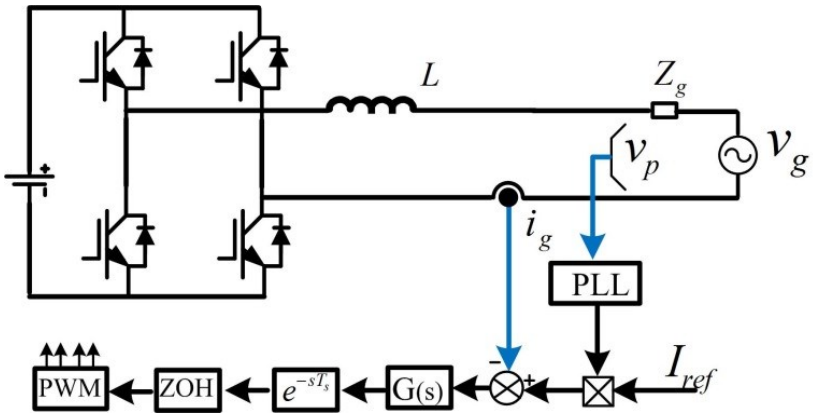


Figure 14: Diagram of single phase grid-connected inverter with current control loop.

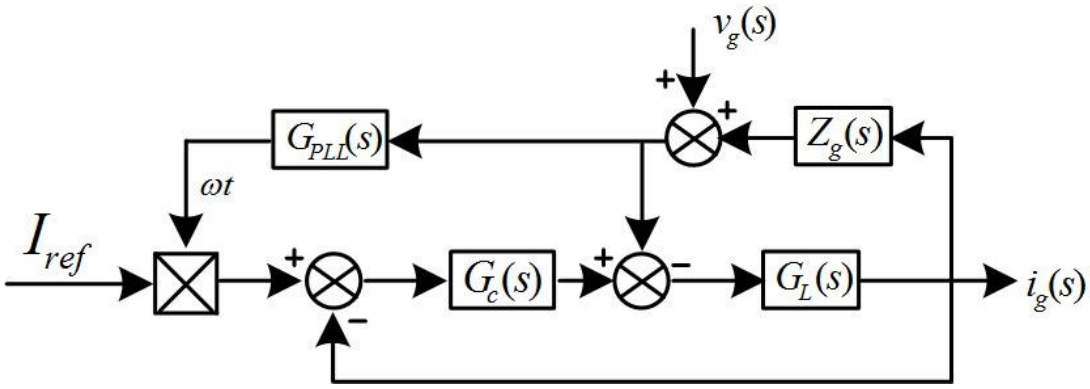


Figure 15: Block diagram of inverter system with current loop.

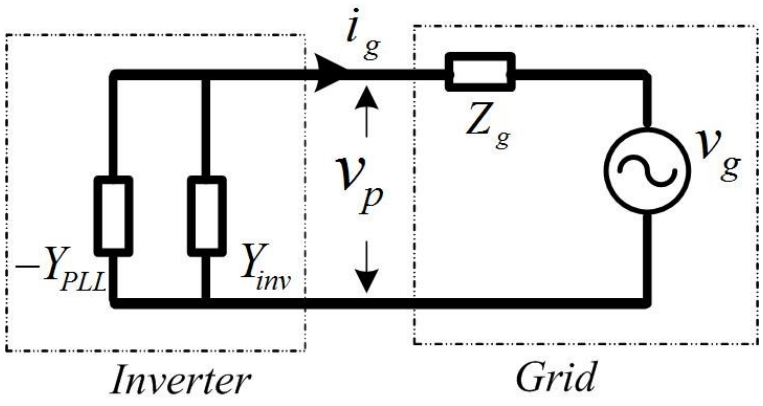


Figure 16: Equivalent circuit of system based on admittance model [50].

Considering the facts mentioned above, it would be good to consider a power control scheme without using conventional PLL. Moreover, due to the nature of weak grid, the grid voltage may have various disturbances such as sag, swell, frequency distortion, and contamination with voltage harmonics. The disturbances in grid can degrade the performance of PLL and whole system largely [49]. For the controller to be introduced in this section, the synchronization function is embedded into the power controller. In this way, the conventional PLL unit is not required, thus the complexity for designing the system can be decreased. Meanwhile, the proposed system keeps good performance of decoupled active and reactive power control with excellent grid current quality even under different conditions of grid disturbance.

Inverter system with LCL filter is a high order system and has high resonant peak value. To overcome the possible resonance problem, active damping technique with capacitor current feedback is applied into the controller design of this system. Traditional grid current controller for single phase inverter with LCL filter is based on PI controller, which is not able to follow a sinusoidal reference without steady state error due to the dynamics of the integral term. And its current tracking performance will be worse under non-ideal grid condition. Though using feedforward control of grid voltage can help resolve this problem to some extent, this could increase the complexity of system design. A power controller for single-phase grid connected inverter system with LCL filter in stationary reference frame without using conventional PLL would be presented in this section. In the designed inner current loop, Proportional & Resonant (PR) controller is used to provide the system with rapid response and high gain in wide

range of frequency. This control scheme has good power tracking performance with independent active and reactive power control ability, and it has robust performance even under distorted grid conditions. The control algorithm has simple structure due to stationary reference frame based implementation. The designed current controller, combining the active damping technique, helps restrain the high resonant peak value. Compared with traditional PI based current controller, the designed current controller, which is based on the Proportional & Resonant (PR) controller, provides the system with high gain to track given reference value fast and output excellent grid current with low THD. Reliable performance under various grid distortion cases and decoupled active and reactive power control abilities of inverter system are achieved through proposed control scheme.

2.2 Principle of proposed controller

Figure 17 shows the structure of single-phase grid-connected inverter system with the proposed controller.

The grid-connected inverter is controlled with a multi-loop controller composed of a power outer loop and a current inner loop with active damping technique. The power reference value could be provided directly by system operator or determined by system operating condition. For example, for single stage PV inverter system, the active power reference value could be equal to the output power of front PV arrays, which is normally determined by the MPPT algorithm output. For double stage PV inverter system, the power reference value could be determined by the output of dc link voltage

regulation loop based on the power balance of the system. The reactive power reference value is supposed to be given by supervisory command based on the dynamic power profile of the system or preferred operating power factor to set. This can be set to zero for unity power factor operation, negative for leading, and positive for the lagging power factor.

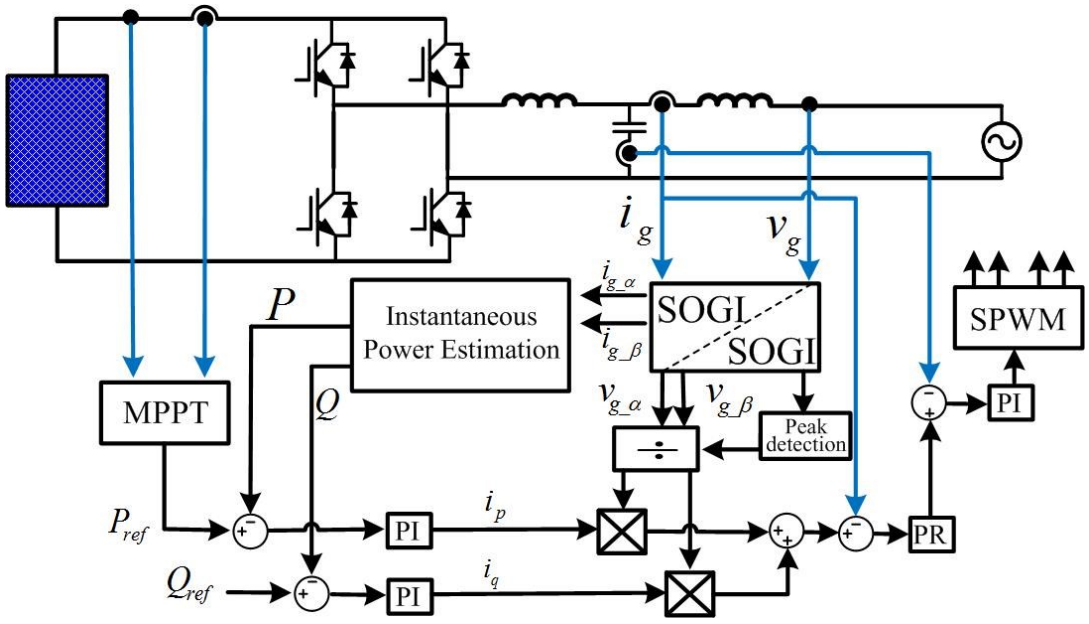


Figure 17: Block diagram of proposed controller.

In the proposed controller, the instantaneous output active power and reactive power are calculated based on the instantaneous power theory. By comparing the calculated instantaneous output values with corresponding references, two independent control values, I_p and I_q , can be obtained. Then I_p and I_q are multiplied with two unit sinusoidal signals coming from the second order general integrator. In this way, two new

signals, I_p' and I_q', will be achieved and it contains both angle and amplitude information, from which we can get the reference signal of grid current. In the proposed controller, the inner loop of the system is the current feedback loop, whose main function is to improve the dynamic performance and ensure that the output current can track the reference well with low tracking error and good distortion rejection capability. Capacitor current feedback is also added into the current loop to overcome the resonance problem introduced by LCL filter.

2.3 Model analysis and parameter design

Fig. 18 shows the topology of an LCL-filter-based grid-connected inverter. The DC bus could be connected with renewable energy resources, such as photovoltaic, wind generator or storage battery and super capacitor, etc. The inverter is used to convert electricity energy from DC to AC and the power flow through it could be bi-directional. The LCL filter restrains the high-frequency switching harmonics.

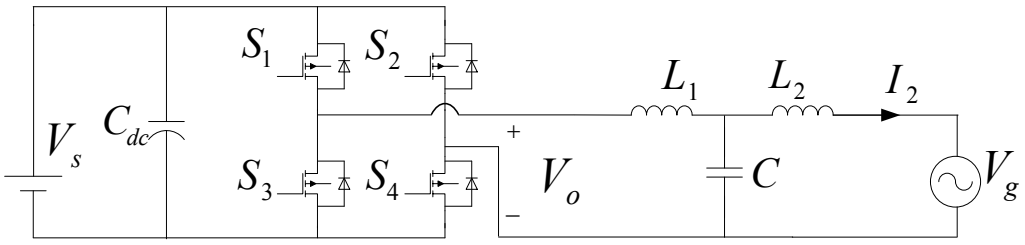


Figure 18: Power stage.

The relationship between V_o, V_g and I_2 in Figure 18 can be expressed in (4). Figure 19 shows the bode plot of the open-loop transfer function from V_o to I_2. Obviously, there exists a rather high resonant peak in the LCL filter, which is undesired for the control system design especially considering the stability regulation.

$$I_2 = V_O \frac{1}{L_1 L_2 C s^3 + (L_1 + L_2)s} - V_g \frac{L_1 C s^2 + 1}{L_1 L_2 C s^3 + (L_1 + L_2)s} \tag{4}$$

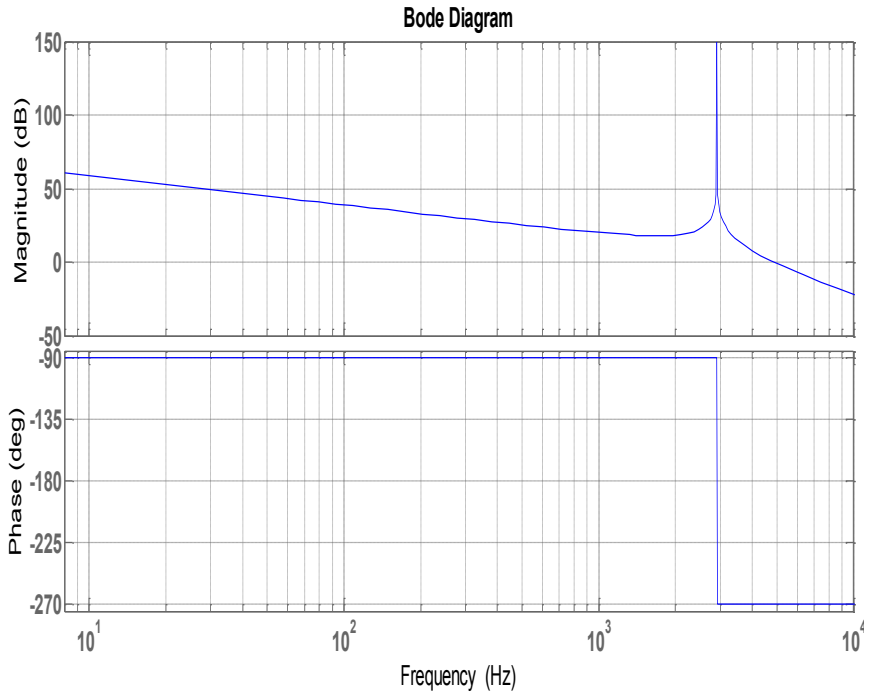


Figure 19: Bode plot of the transfer function from Vo to I2.

The resonance frequency of an LCL filter can be damped by passive methods such as connecting a resistor to the filter capacitor. But this would greatly reduce the efficiency of the system and degrade LCL filter performance in high frequency range.

Instead of using a real resistor, active method is considered. The transients can be damped with no extra power loss. This is implemented in the current inner loop with extra capacitor current feedback as shown in Figure 20. This is supposed to have similar damping performance as passive method by forming a virtual resistance in the system by the way of feedback control loop.

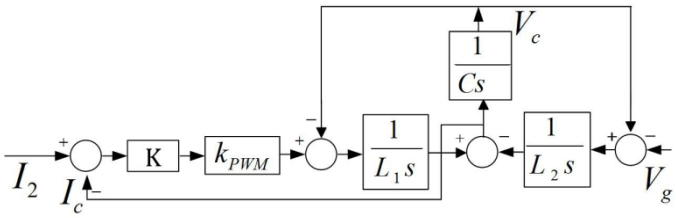


Figure 20: Block diagram of double loop control of current controller.

Figure 20 shows the block diagram of current controller.

The relationship between i_2 and v_o in Figure 20 is expressed in (5). k_{PWM} is the gain of switching modulator. In order to simplify control design, the compensator of capacitor current loop contains only proportional part, K. Comparing to (4), there is an added damping term in (5), which help damp the resonant peak problem. As shown in the bode plot of the open-loop transfer function, there is no resonant peak in the new control loop, which contributes from the added capacitor current inner loop in the current controller design.

$$\frac{i_2}{v_o} = \frac{k_{PWM} K}{L_1 L_2 C s^3 + K k_{PWM} L_2 C s^2 + (L_1 + L_2) s} \tag{5}$$

The current reference value can be derived based on Figure 17 as

$$I_{ref} = I_p^{'} + I_q^{'} = \frac{I_p V_{g-\alpha} + I_q V_{g-\beta}}{|V_g|} \tag{6}$$

where $$|V_g| = \sqrt{V_{g-\alpha}^2 + V_{g-\beta}^2}$$

Here, PR controller is used as compensator in grid current loop, which could provide extremely high gain at the resonance frequency ω_0 to reach almost zero steady-state error. The transfer function of PR controller is expressed as the following.

$$G_s(s) = K_P + \frac{2K_R s}{s^2 + \omega_0^2} \tag{7}$$

The dual closed loop current controller with capacitor current inner-loop and grid current outer-loop aims at current accuracy and acceptable distortion. The open-loop transfer function of current controller can be derived as

$$G_o(s) = \frac{B_1 s^2 + B_2 s + B_3}{A_1 s^5 + A_2 s^4 + A_3 s^3 + A_4 s^2 + A_5 s} \tag{8}$$

Where, $B_1 = K_P K K_{PWM}$,

$B_2 = 2K K_{PWM} K_R$,

$B_3 = K_P K K_{PWM} \omega_0^2$,

$A_1 = L_1 L_2 C$,

$A_2 = K K_{PWM} L_2 C$,

$A_3 = L_1 L_2 C \omega_0^2 + L_1 + L_2$,

$A_4 = L_2 C K K_{PWM} \omega_0^2$,

$A_5 = (L_1 + L_2) \omega_0^2$,

Based on the pole placement theory, the desired design parameters can be achieved. The stability of inner loop could also be checked by Routh's stability criterion to give critical range of parameters as the following.

$$\begin{cases} L - k_p L_1 > 0 \\ k_p(L - k_p L_1) - k L_2 k_{pwm} k_R C > 0 \end{cases} \tag{9}$$

In order to achieve the preferred dynamic and stability performance of proposed system, the following parameters were chosen finally: k_P=3.3, k_R=3091.7. Figure 21 shows related root locus plot.

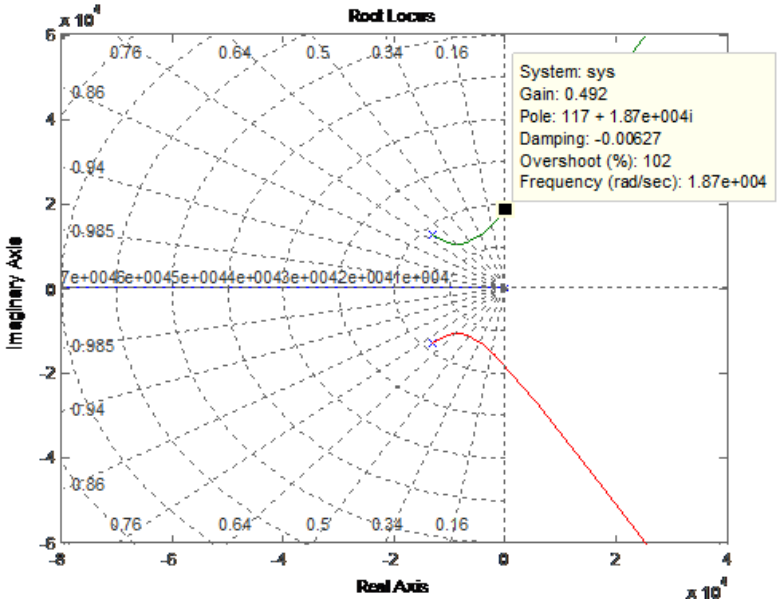


Figure 21: Root locus plot.

After designing the current loop, the power loop can be simplified by just considering delay characteristics of inner loop assuming the bandwidth of current loop is much higher than that of power loop. Then the block diagram of power loop can be

derived accordingly. In this way, the control delay introduced by inner loop could be considered and bandwidth of outer loop is supposed to be much smaller than that of inner loop.

The open-loop transfer function of the power controller can be expressed as

$$G_0(s) = \frac{k_P s + k_I}{s} \cdot V_g \cdot \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \cdot \frac{1}{T_c s + 1} \tag{10}$$

where k_p and k_I are the parameters of PI compensator of power loop. k and ω are two parameters of SOGI module, which will be introduced in detail in the following part. T_c is the control period of the whole system. It is the control delay introduced by current loop. It is normally a small value in real implementation.

For the power outer loop, the main two functions are to track the given power reference with small tracking error and ensure the stability of the system. Considering these two aims, the specific controller parameters can be designed through frequency response method. Normally, V_g, the amplitude of grid voltage, could be changeable in distorted grid conditions. As can be seen in (10), V_g is also a variable that may affect the system performance. In proposed controller, due to the existence of SOGI module, which offering a high gain at the working frequency, the change of V_g will not affect the system's performance heavily in a certain frequency range, which can be concluded from Figure 22. When V_g changes from 250 to 350V (peak value), the system response does not change a lot.

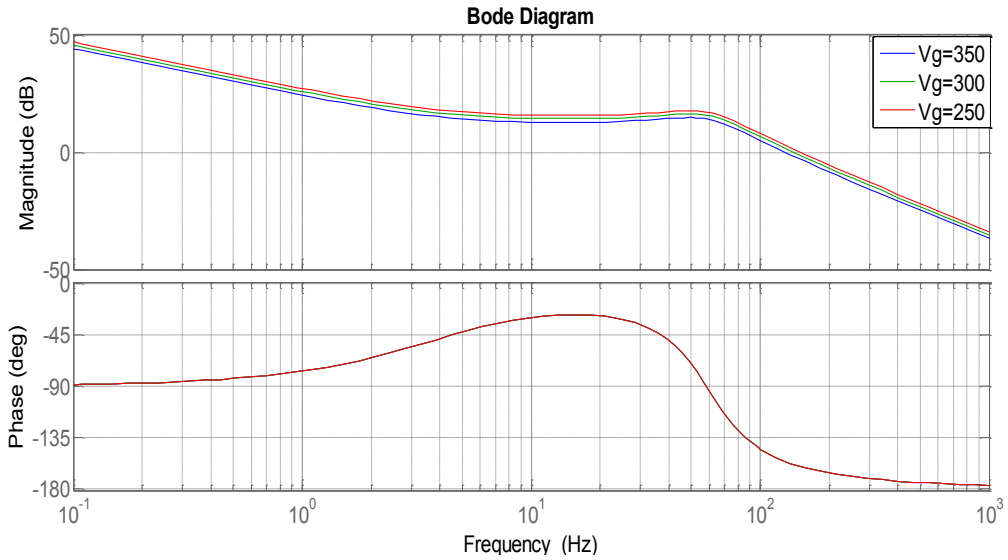


Figure 22: Frequency response of control system with different grid voltage amplitude (k_P=0.02,k_I=0.5).

This characteristic can not only improve the robust performance of system under distorted grid conditions, but also make it possible to apply the peak value detection method into the system. The peak value detection method is applied to get the maximum value of grid voltage, as shown in Figure 17. The peak detection method can be implemented by taking the detected peak value in one or two cycles as the maximum value of grid voltage. But this method may introduce delay in the implementation and tracking error under distorted grid condition. In the proposed controller, the second-order generalized integrator (SOGI) module outputs are utilized to get peak voltage value. The expression to calculate it is shown in (6).

To create an orthogonal signal from an original single-phase signal, different OSG techniques have been proposed in the literature. In the proposed controller, the

second-order generalized integrator (SOGI)-based OSG technique is applied. Its block diagram is shown in Figure 23.

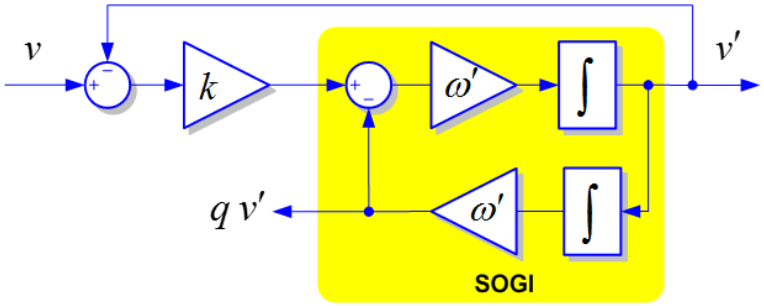


Figure 23: Block diagram of SOGI.

This approach prevents harmonics/ noises from reaching the controller and therefore is suitable for this kind of application. The input-to-output transfer function describing the dynamics of SOGI is shown in equations (11) and (12), where *w* is the fundamental angular frequency.

$$\frac{x_\alpha(s)}{x(s)} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{11}$$

$$\frac{x_\beta(s)}{x(s)} = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{12}$$

Based on given transfer function, the corresponding bode plots can be plotted out as Figure 26. The response of SOGI with various distorted input voltage is shown in Figure 24 and Figure 25.

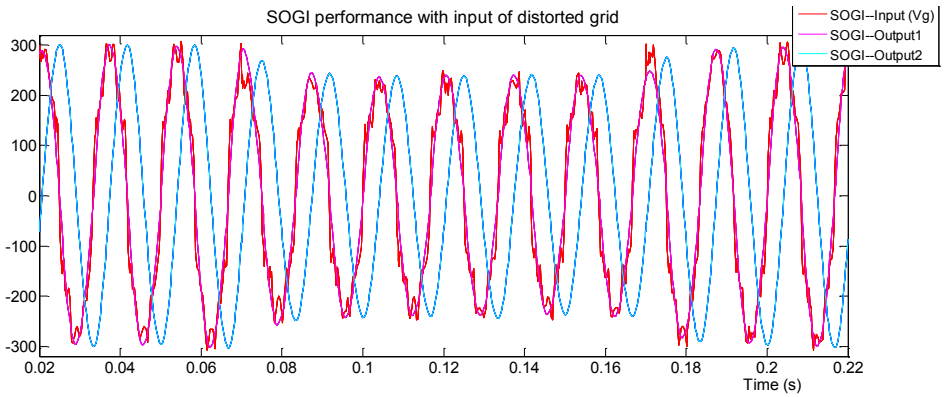


Figure 24: Input voltage with 10%THD harmonics sags by 20% at 0.07s.

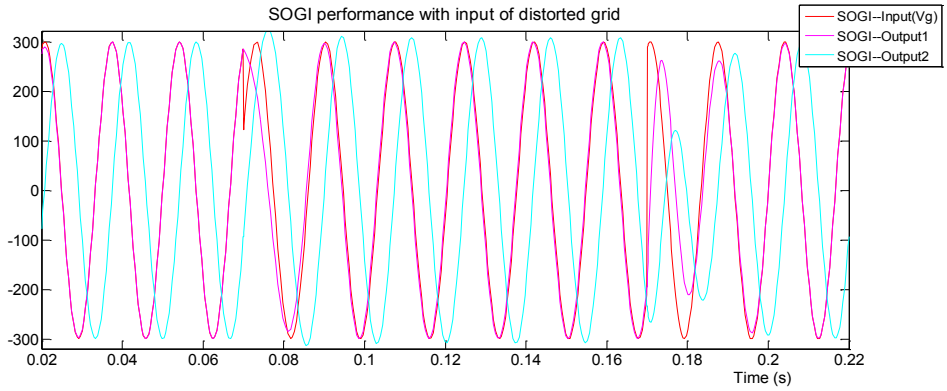


Figure 25: Input voltage frequency steps from 60Hz to 58Hz at 0.07s.

In Figure 24, input voltage (V_{in}=300V, f_{in}=60Hz) is designed to be combined with 8% 5^{th}, 8% 7^{th}, 8% 11^{th} harmonics. And it sags by 20% at time 0.07s and resume to

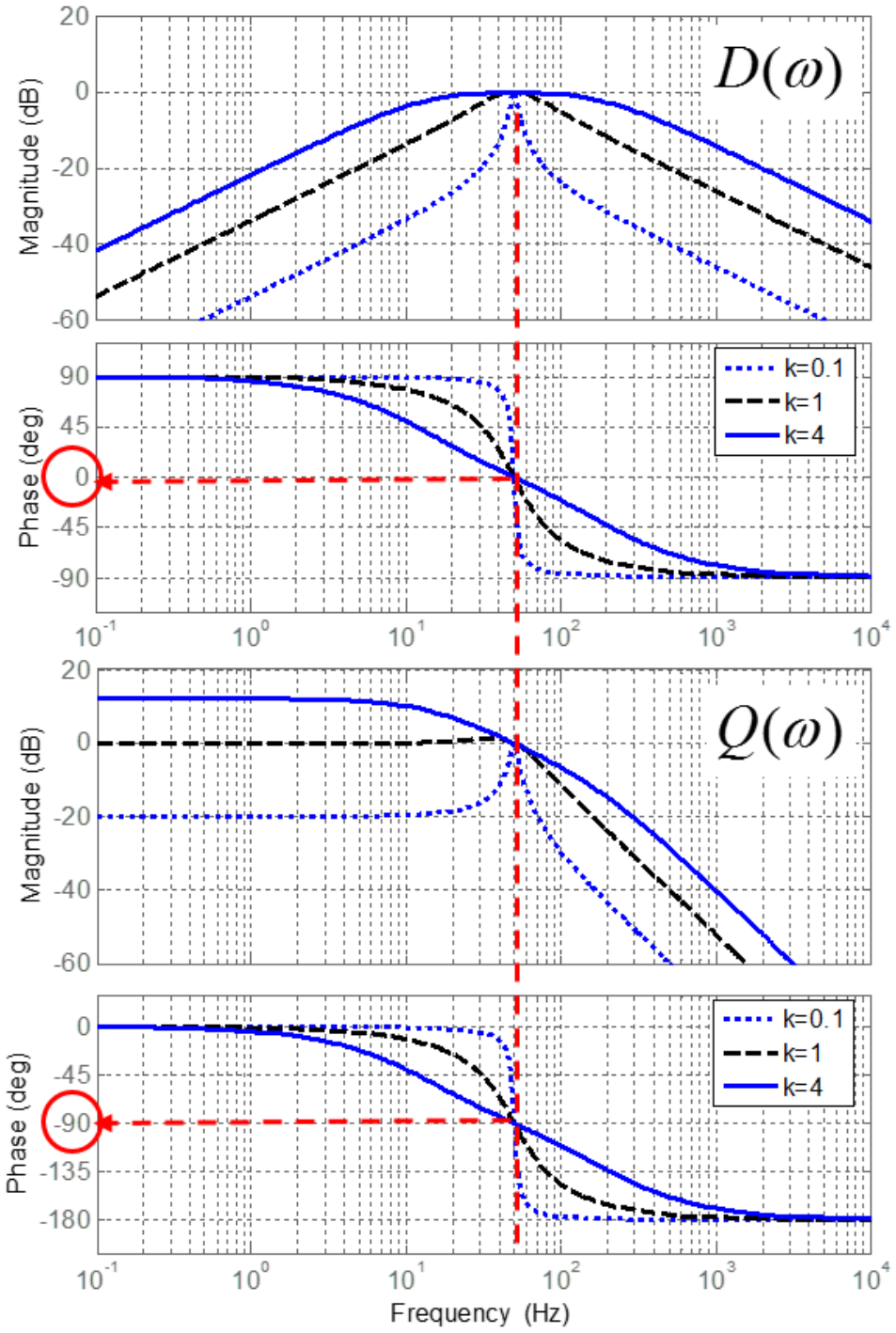


Figure 26: Bode plot of SOGI.

original condition at time 0.17s. In Figure 25, the frequency of input voltage changes from 60Hz to 58Hz at 0.07s. And it resume to original condition at time 0.17s. As shown in the results, the SOGI module has a good performance in various distortion conditions. Though the input signal could have various distortions, its output signals track input well with clean waveform and small distortion.

With the orthogonal signals created by SOGI modules, the instantaneous power values can be calculated based on instantaneous power theory. The corresponding calculation equations are shown in (13) and (14).

$$P = \frac{1}{2}(V_{g-\alpha} \cdot I_{g-\alpha} + V_{g-\beta} \cdot I_{g-\beta}) \tag{13}$$

$$Q = \frac{1}{2}(V_{g-\beta} \cdot I_{g-\alpha} - V_{g-\alpha} \cdot I_{g-\beta}) \tag{14}$$

where $V_{g-\alpha}, V_{g-\beta}$ are the derived orthogonal signals of grid voltage, and $I_{g-\alpha}, I_{g-\beta}$ are the derived orthogonal signals of grid current.

The following part describes the way to check the stability of proposed controller. Firstly, the state space function of system can be represented as

$$\dot{x} = Ax + Bu \tag{15}$$

$$A = \begin{bmatrix} 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & \frac{1}{C} \\ 0 & -\frac{1}{L_1} - \frac{1}{L_2} & 0 \end{bmatrix}, \quad B = \begin{bmatrix} 0 & -\frac{1}{L_2} \\ 0 & 0 \\ \frac{1}{L_1} & \frac{1}{L_2} \end{bmatrix}$$

$$x = \begin{bmatrix} i_{L1} & v_c & i_{L2} \end{bmatrix}^T, \quad u = \begin{bmatrix} V_1 & U_s \end{bmatrix}^T$$

The discrete state space representation of system can be derived accordingly as

$$X(k+1)=\phi(T)X(k)+GU(k)Y(k)=CX(k) \tag{16}$$

where the system and input matrices are shown as follows:

$$\phi=\begin{bmatrix} 1 & \dfrac{\sin\omega_r T}{\omega_r L_2} & \dfrac{1-\cos\omega_r T}{\omega_r^2 L_2 C} \\ 0 & \cos\omega_r T & \dfrac{\sin\omega_r T}{\omega_r C} \\ 0 & -\omega_r C\sin\omega_r T & \cos\omega_r T \end{bmatrix},\ G=\begin{bmatrix} \dfrac{\omega_r T-\sin\omega_r T}{\omega_r L}K_{PWM} & -\dfrac{L_1\sin\omega_r T+L_2\omega_r T}{\omega_r L L_2} \\ \dfrac{1-\cos\omega_r T}{\omega_r^2 L_1 C}K_{PWM} & \dfrac{1-\cos\omega_r T}{\omega_r^2 L_2 C} \\ \dfrac{\sin\omega_r T}{\omega_r L_1}K_{PWM} & \dfrac{\sin\omega_r T}{\omega_r L_2} \end{bmatrix}$$

The discrete transfer function of grid-side current versus controller output can be derived as

$$G(z)=\frac{\dfrac{(\omega_r T-\sin\omega_r T)K_{PWM}}{\omega_r L}(z^2+2\dfrac{\sin\omega_r T-\omega_r T\cos\omega_r T}{\omega_r T-\sin\omega_r T}z+1)}{(z-1)(z^2-2\cos\omega_r Tz+1)} \tag{17}$$

The open loop transfer function considering the delay introduced by sampling and switching modulation can be derived as

$$G(z)=(k_p+k_iT)b\frac{z-\dfrac{k_p}{k_p+k_iT}}{z-1}\frac{(z^2+2cz+1)}{z(z-1)(z^2-2\cos\omega_r Tz+1)} \tag{18}$$

where

$b=K_{PWM}(\omega_r T-\sin\omega_r T/\omega_r L)$

$c=(\sin\omega_r T-\omega_r T\cos\omega_r T)$

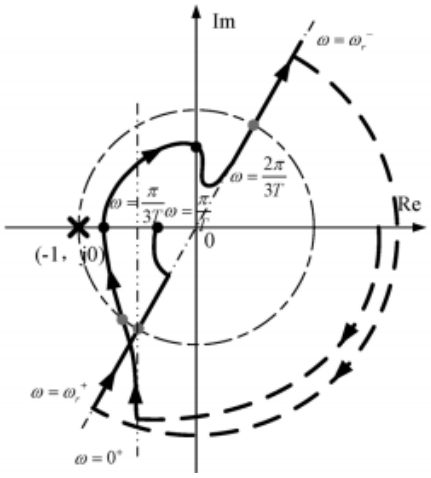
Setting $z=e^{j\omega t}=\cos(\omega T)+j\sin(\omega T)$, then the frequency response function can be derived as

$$G(j\omega) = -\frac{b(c+\cos\omega T)}{2(\cos\omega T-\cos\omega_r T)(1-\cos\omega T)} \cdot \{[k_p(\cos\omega T-\cos 2\omega T)+k_i T\cos\omega T] + \mathrm{j}[k_p(\sin 2\omega T-\sin\omega T)-k_i T\sin\omega T]\} \tag{19}$$

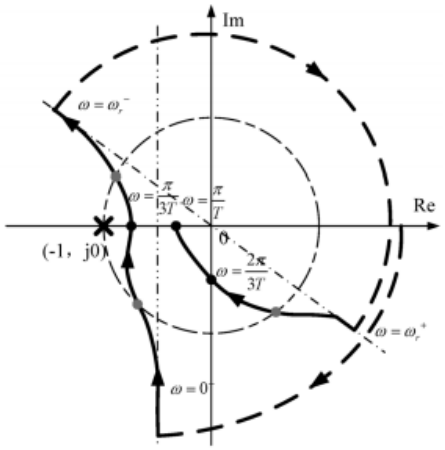
The Nyquist diagram of system in different cases is shown as Figure 27. The stability condition is then derived out as follows.

$$k_p < \frac{\frac{4L}{Tk_{PWM}}\omega_r T(1+\cos\omega_r T)}{[2\sin\omega_r T-\omega_r T(1+\cos\omega_r T)](2+\frac{k_i T}{k_p})} \tag{20}$$

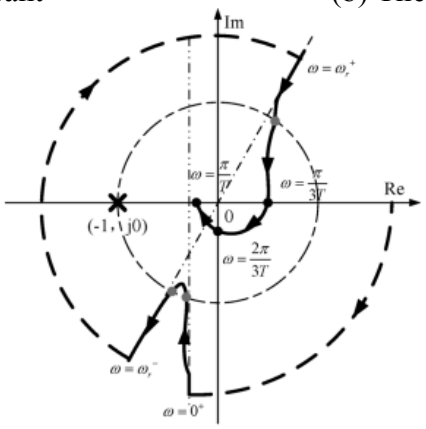
$$2\cos\omega_r T-1<\frac{k_i T}{k_p}<1 \tag{21}$$



(a) The first quadrant



(b) The second quadrant



(c) The third quadrant.

Figure 27: The Nyquist diagram of system.

2.4 Simulation and experimental results

The simulation model based on Figure 17 is built in Matlab/Simulink. The component parameters are listed in Table I.

Table 1: Circuit parameter

Dc	400 V	Grid frequency	60 Hz
L_1	6 mH	L_2	1.2 mH
C	10 uF	Power rating	500 W
V_g	170 V	f_s	20k Hz

2.4.1. Decoupled Real and Reactive Power Control & Dynamic Performance

Figure 28 shows the steady state performance of the proposed control system in the case when active power reference value is 500 W and reactive power reference value is 0 Var. As shown in the simulation results, both output active and reactive power track the reference well with less than 1% tracking error and the grid current is within clean sinusoidal waveform. In this case, the THD value of grid current is 1.8%.

Figure 29 shows the simulation results of system about dynamic performance. In this case, the reference values of active power and reactive power have a step change simultaneously at both 0.15s and 0.3s, the corresponding output performance of the system with given reference values and instantaneous output power is provided. As shown in Figure 29, the system keeps stable under different step-change conditions. And

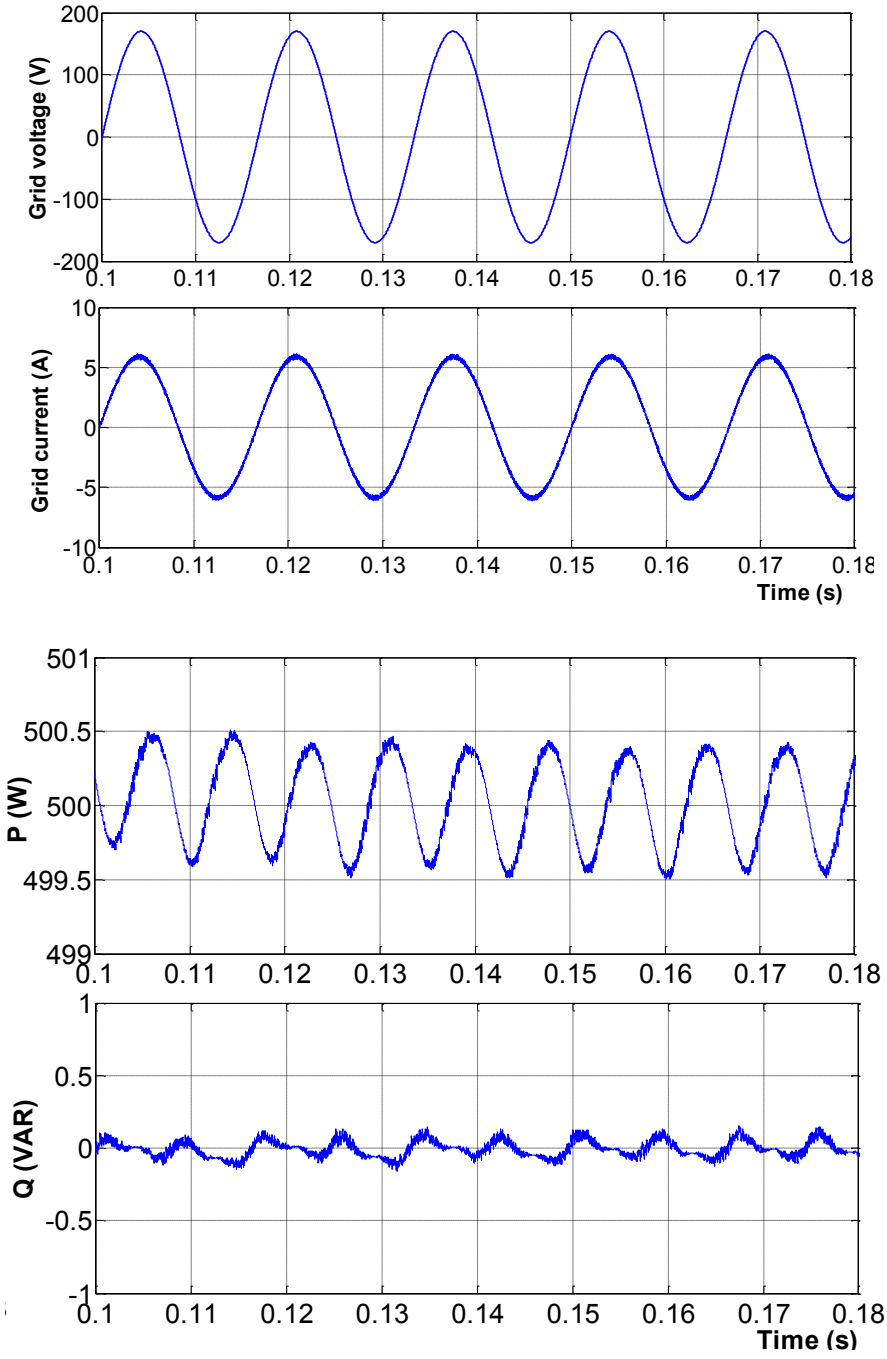


Figure 28: Steady state performance.
(active power reference of 500 W and unity power factor).

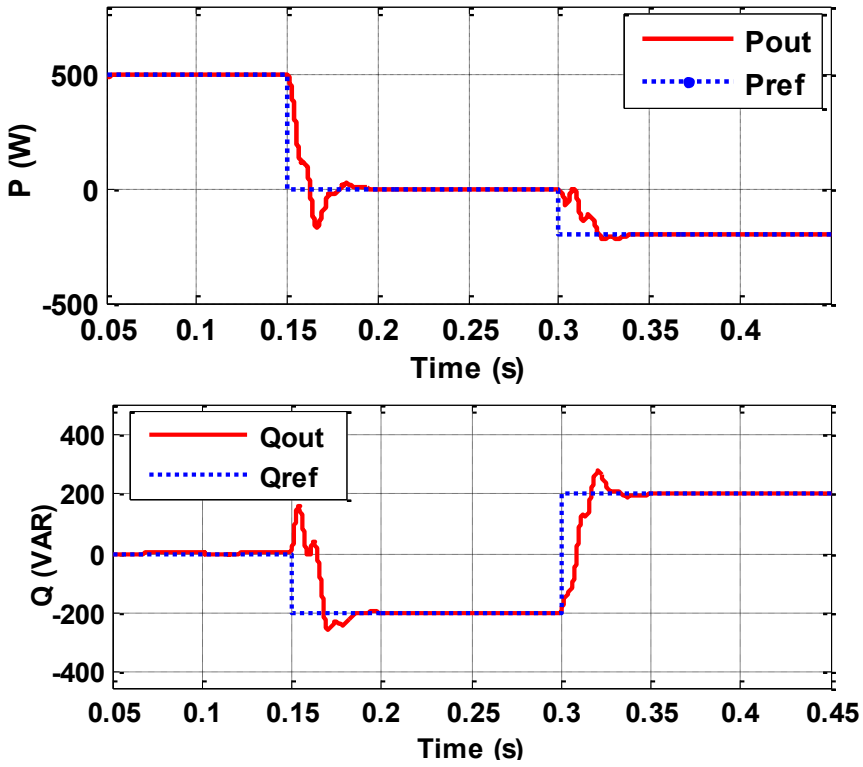


Figure 29: Step response of active and reactive power.

the output power of system is able to track the reference values well in less than 0.1 s with small tracking error within 1%, which proves a good dynamic performance. Moreover, the simulation results also prove the decoupled power control capability is achieved, which means that the active power and reactive power can be controlled independently with flexible power factor. The output power can be actually bidirectional, which means the inverter system has the capability that can not only support power as a source but also consume power as a load (in case there is energy storage or load at dc side in system) with four quadrant operation capability.

2.4.2. Performance under Various Distorted Grid Conditions

There are four distorted grid conditions considered, including grid voltage sag and swell, grid voltage frequency variation and harmonic distortion (with rich harmonic contents). Figures 30 to 33 show simulation results of proposed system under specific distorted grid conditions.

1) In the first case, the grid voltage ($V_g = 120\ V$) sags by 15% suddenly at 0.2 s and then resumes to original condition at time 0.3 s, the output performance of system can be seen in Figure 30. In this case, the proposed control method ensures the constant output power and perfect grid current even though the grid voltage sags. The THD of I_g is 1.01% in this case.

2) In the second case, the grid voltage ($V_g = 120\ V$) swells by 10% suddenly at 0.2 s and then resumes to original condition at time 0.3 s, the output performance of system can be seen in Figure 31. In this case, the proposed control method ensures the constant output power and perfect grid current even though the grid voltage sags. The THD of I_g is 1.01% in this case.

3) In the third case, the grid voltage is combined with 4% 3^{th}, 4% 5^{th}, 3% 7^{th} and 3% 11^{th} order harmonics beginning from 0.2 s and then resumes to the ideal condition without harmonic components at the instant of 0.3 s. Corresponding system output performance is shown in Figure 32. The output power keeps tracking reference well with small tracking error. The THD of I_g in this case is 2.49% even with harmonic distortion.

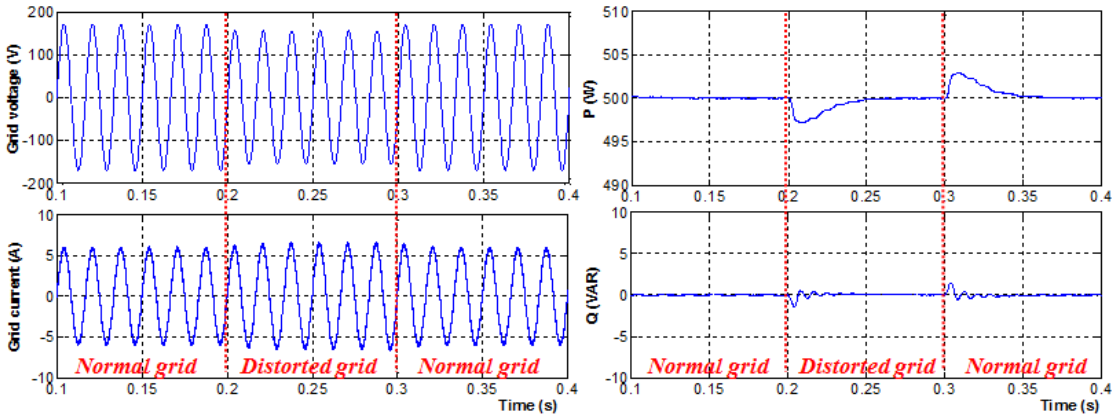


Figure 30: Grid-amplitude sag (sag 15% , 0.2-0.3 s).

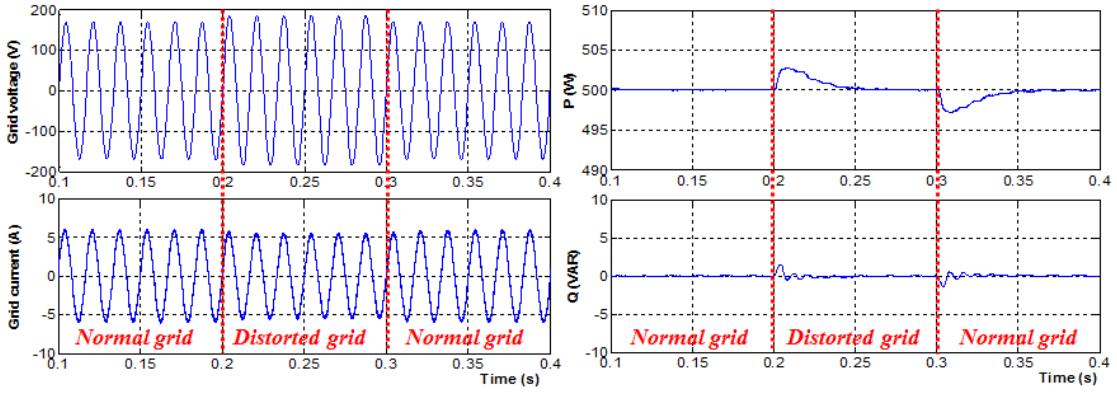


Figure 31: Grid-amplitude swell (swell 10% , 0.2-0.3 s).

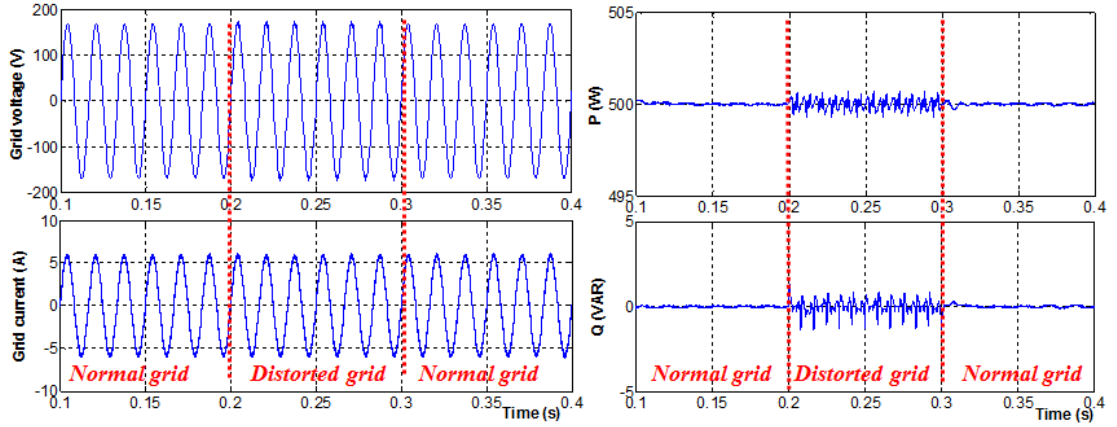


Figure 32: Distorted grid with harmonics (5% THD, 0.2-0.3 s).

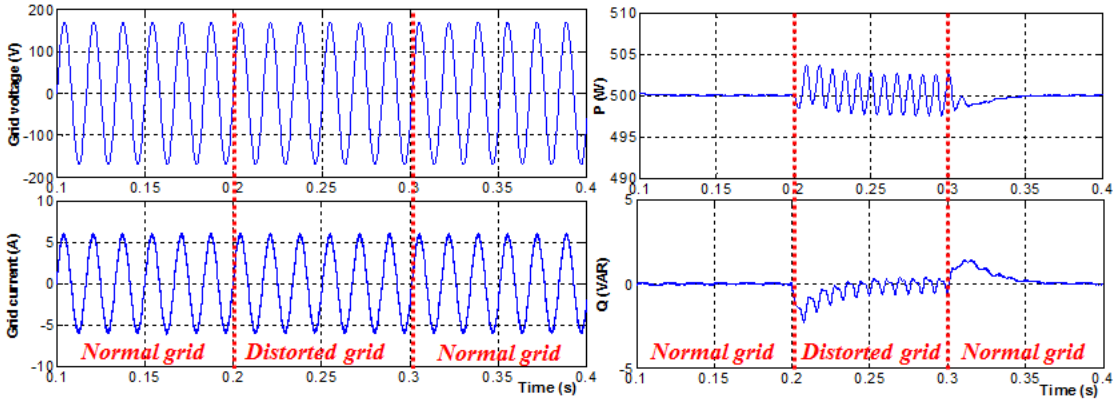


Figure 33: Frequency-distorted grid (59.3Hz, 0.2-0.3 s).

4) In the fourth case, the grid voltage frequency step changes from 60 Hz to 59.3 Hz at 0.2 s and then resumes to the original condition at 0.3 s, the output performance of system is shown in Figure 33. Proposed control method enforces grid current to synchronize grid voltage in order to have constant output power even though grid voltage frequency has variation. And the THD of I_g is 1.24% in this case and power tracking error is less than 1%.

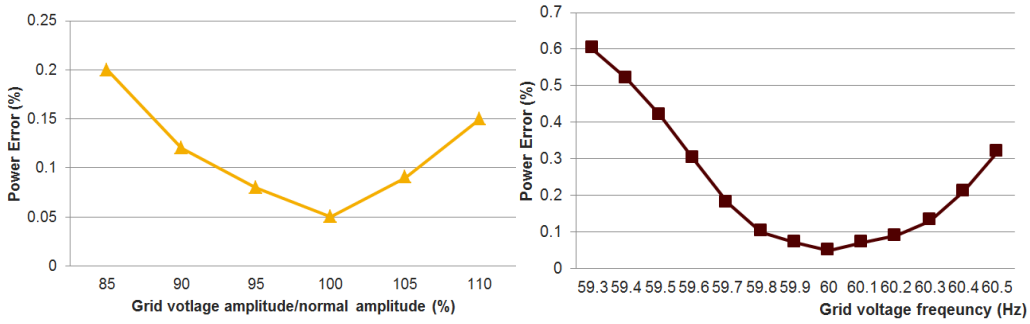


Figure 34: Power tracking performance with different grid voltage conditions.

Figure 34 shows the summary of simulation results about power tracking performance of proposed system in steady state under different grid conditions. The first plot in Figure 34 shows results with different grid voltage amplitude. As shown in this plot, when the grid voltage amplitude varies from nominal value with larger variation, the power tracking error would be higher. But the power tracking error keeps less than 0.5% when the grid voltage amplitude varies within range from 85% to 110%. The second plot in Figure 34 shows results with different grid voltage frequency. The power tracking error would always be less than 1% when the grid voltage frequency varies within range from 59.3Hz to 60.5Hz.

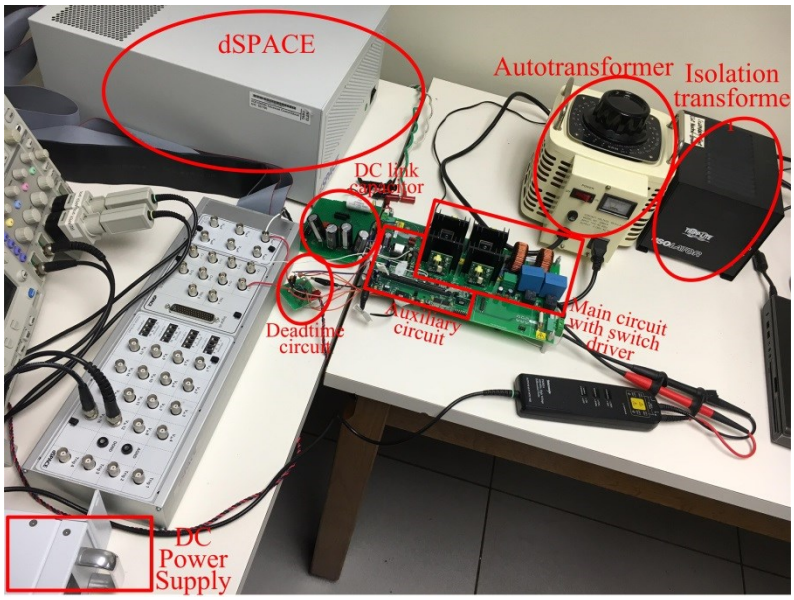


Figure 35: Testbed used in experiment.

In order to verify its effectiveness, the proposed control strategy is implemented with dSPACE1007 with the same parameters listed in Table 1. The setup of experiment is show in Figure 35.

Figure 36 presents the system performance under steady state condition when the active power reference value is set as 120 W and reactive power reference value is set as 30 Var. In this case, the output grid current tracks the reference well with good waveform as shown in results. The dynamic performance of the converter with the proposed scheme is presented in Figure 37, where the active power reference value step changes from 120 W to 0 W and reactive power reference value step changes from 70 Var to 30 Var at the same time. As seen from results, the output power came to a new steady state very fast. These results demonstrate the decoupled power control capability of the proposed control strategy with good dynamic performance.

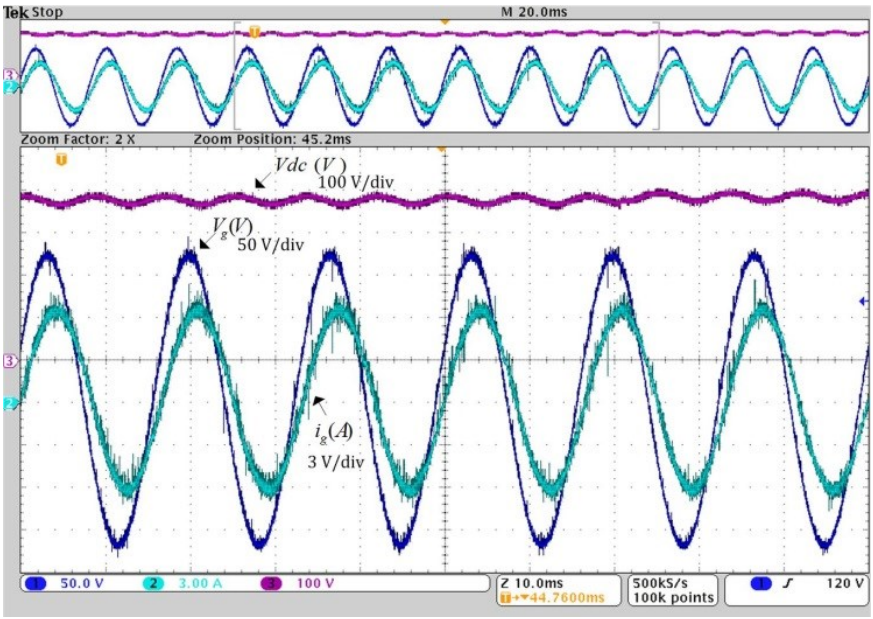


Figure 36: Steady-state Performance.
Pref (120 W) and Qref (30 Var).

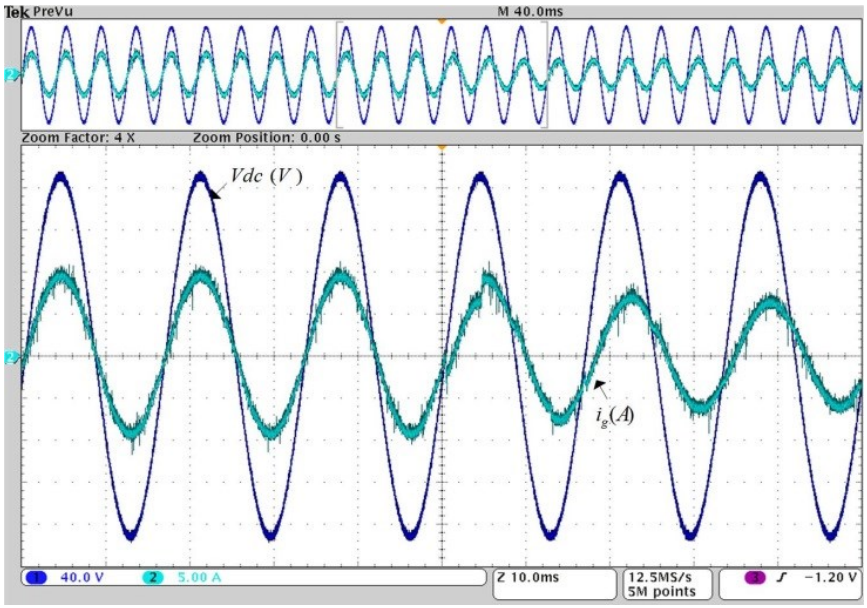
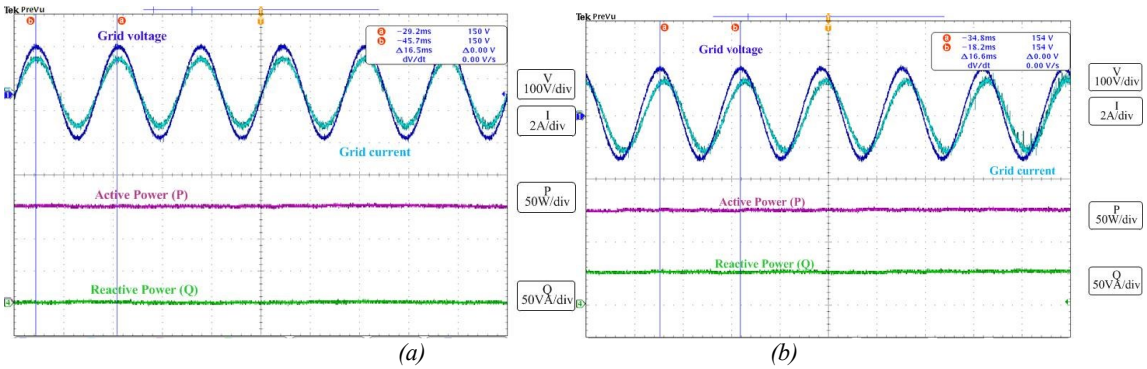
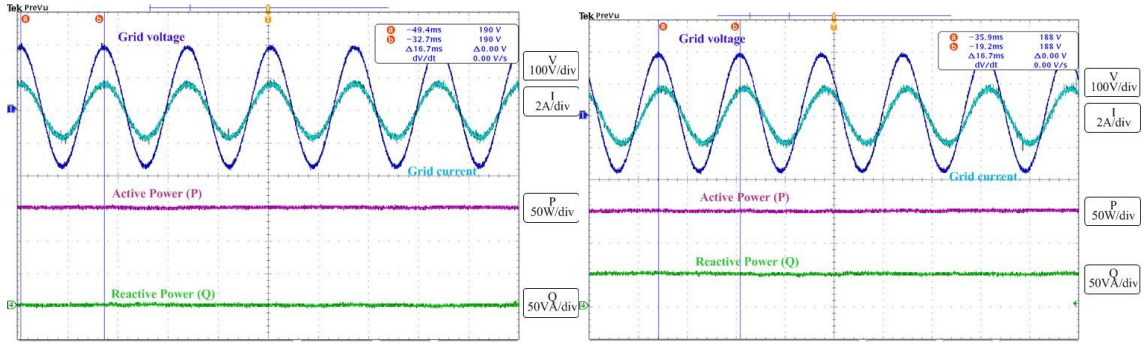


Figure 37: Dynamic performance.
(P and Q step change simultaneously representing a change in the load power factor).



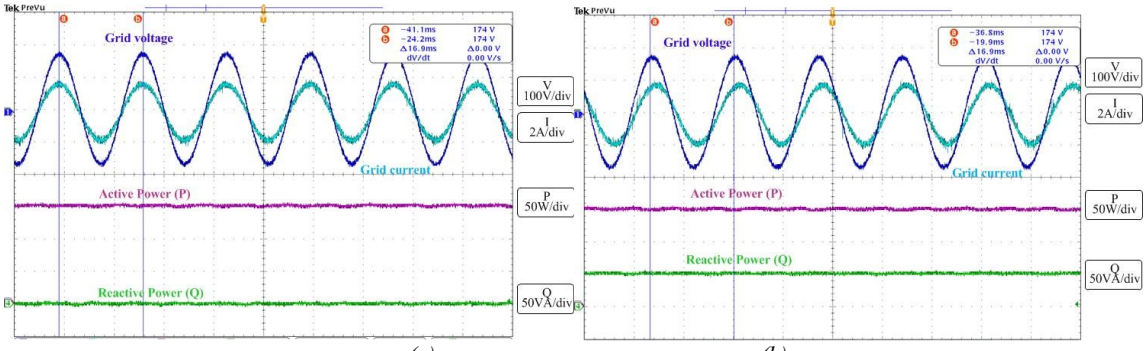
(a) *(b)*

Figure 38: Grid-amplitude sag (sag 15%).



(a) *(b)*

Figure 39: Grid-amplitude swell (swell 10%).



(a) *(b)*

Figure 40: Frequency-distorted grid (59.3Hz).

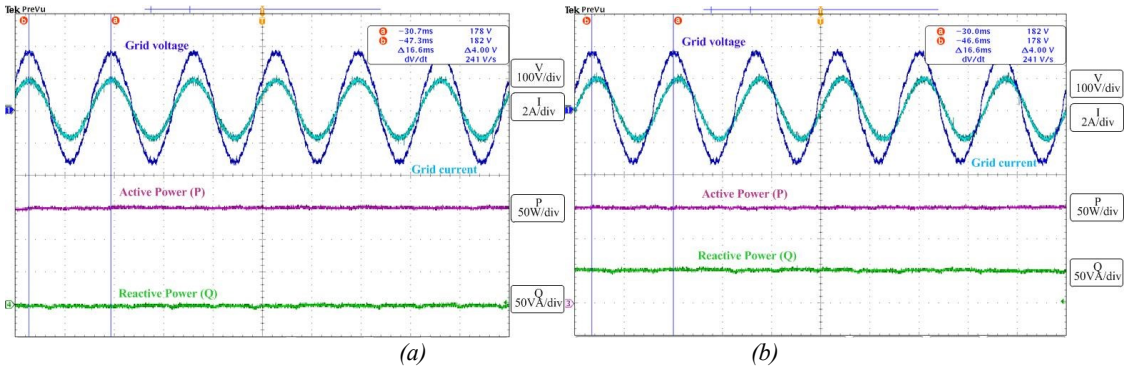


Figure 41: Distorted grid with harmonics (5% THD).

Figure 38 shows the output performance of system in the case when the grid voltage sags by 15% (to 102Vrms). In this case, the proposed control method ensures the constant output power and perfect grid current even though the grid voltage sags. Similarly, Figure 39 shows the output performance of system in the case when the grid voltage swell by 10% (to 132Vrms). Figure 40 shows the performance of system in the case when the grid voltage has a frequency distortion. In this case, the grid voltage is 59.3Hz instead of 60Hz. Another distorted grid condition is harmonic distortion case. Its performance is shown in Figure 41. In this case, the grid voltage is distorted with 4% 3^{th}, 4% 5^{th}, 3% 7^{th} and 3% 11^{th} order harmonics, the corresponding system output performance can be seen in Figure 41. The THD of I_g is as low as 2.49% under the distorted case. In all cases, two conditions are checked with different power reference: (a)Pref (150 W) and Qref (0 Var); (b) Pref (150 W) and Qref (50 Var). As shown in the results, in all cases, the proposed control method could have a exact power tracking performance with tracking error less than 1% and the grid current keeps in clean waveform with small distortion under standard even though the grid voltage is distorted.

2.5 Conclusion

Grid connected inverters, especially those used in distributed generating system, are expected with decoupled and flexible power control ability. Many existing power control methods are based on synchronous reference frame transformation, which requires the phase angle information provided by phase-locked loop. This creates additional drawbacks of the system and makes the system complex. This section presents a controller for single-phase grid connected inverter system with LCL filter in stationary reference frame. And conventional PLL is not necessary, which simplifies the controller design. Compared with traditional power control scheme for single phase grid-connected inverter controller, this control scheme has faster response, higher reliability and independent active and reactive power control capability. Moreover, the proposed controller has good robustness under various distorted grid conditions. Since the controller is totally implemented in stationary reference frame, the control algorithm is simpler and easier to implement. The designed current controller, combining the active damping technique, helps restrain the high resonant peak value. Compared with traditional PI based current controller, the designed current controller, which is based on the proportional & resonant controller, provides the system with high gain in wide range of frequency to track given reference value fast and output excellent grid current with low THD.

3 MODEL PREDICTIVE CONTROL OF VOLTAGE SOURCE INVERTER WITH SEAMLESS TRANSITION*

3.1 Introduction

Grid-connected inverter becomes increasingly important in distributed generation systems [52, 53] particularly when considering high penetration of roof-top photovoltaics (PV) [54] and other renewable energy sources [55]. Renewable energy based DG systems are mandated by grid codes to have a precise and independent control over active and reactive power and hence serve as ancillary support to grid [42]. It is expected for the DG system to supply continuous power to the local loads, even in the abnormal grid conditions such as utility power outage [56, 57]. When the grid recovers, the DG system should be able to reconnect to the grid and operate in grid-connected mode. Thus it is required to have a dual-mode inverter in DG systems with the reliable operation in both grid-connected and islanded mode. The transition between two aforementioned operating modes may result in voltage spikes across the local loads and inrush currents into the grid due to mismatch in voltage frequency, phase, or amplitude [58]. Therefore, it is important for the DG inverter system to be able to transfer seamlessly between operating modes to reduce voltage and current spikes. In order to

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achieve grid synchronization, phase locked-loop (PLL) is commonly used. PLLs are difficult to implement due to their nonlinear property and complex tuning for desired performance [47, 59, 60] and it could lead to adverse transient performance with limited distortion rejection capability in non-ideal grid condition [61]. All these make PLL not suitable for reliable operation of the DG dual-mode inverters. This paper uses a simple synchronization algorithm by utilizing the second-order generalized integrator (SOGI) [47], with proved harmonic distortion rejection capability. The proposed synchronization algorithm is detecting the phase angle of the grid voltage for purpose of grid synchronization and generating the local load voltage reference.

Many design and control methods for dual-mode inverters have been suggested in literature [44, 62-65]. In existing methods, several separate controllers were designed for different operation modes in order to implement the capability to operate in different conditions. This increases the complexity and decreases the reliability of the system. Some of these controllers [44, 64-66] only change the voltage reference amplitude, but the phase angle difference is not considered which may cause deviation in grid synchronization when re-connecting to grid. Some of these methods [65, 66] suffers from slow transient performance due to the use of nested loop structure. Most of the control strategies proposed did not consider grid abnormalities such as distorted grid voltage. Some methods [67, 68] suffers from big voltage spikes and rush grid current during transfer process. Furthermore, conventional methods based on cascaded multi-loop control structure in literature are difficult to implement due to their complex tuning.

In order to overcome these design challenges, this paper uses the characteristics of MPC to propose a new controller for grid-connected inverter with seamless transition between grid-connected and islanding modes of operation. The proposed controller uses just one cost function to achieve the control objectives for all modes of operation. This feature simplifies the controller algorithm comparing to classic linear multi-loop controllers. MPC is a powerful class of controllers that uses a model of a system to predict future behavior and choose control actuation to optimize performance objectives [44]. As such, the technique has numerous advantages over classical control methods including the easy inclusion of operational constraints and multi-objective in cost functions and fast dynamic response [69]. Recently MPC has gained high focus in power electronics and motor drive communities due to improvements in the performance and cost of DSPs for embedded systems [59, 70].

In the grid-connected mode of the proposed system, the inverter operates as controllable current source to control the output active and reactive power. This renders the capability of bidirectional power flow by either injecting decoupled active and reactive power to the grid or absorbing power from the grid. Power prediction model is derived based on instantaneous power theory in stationary reference frame. The proposed direct power control method based on MPC has promising dynamic performance. In the islanded mode, the inverter regulates the load voltage across either linear or non-linear loads. The load current is estimated from the predictive model of the system without an explicit current sensor. Concurrently, a synchronization algorithm is proposed to detect the phase angle of the grid voltage and generate the load voltage

reference during the transition process from grid-connected to islanded mode. With the SOGI module, the proposed algorithm can maintain reliable performance even under grid disturbances. When the grid is ready to reconnect, a phase adjustment algorithm runs first to ensure smooth transition. The seamless transition between two different operation modes is implemented to avoid the undesired load voltage and grid current overshoots. Control objectives in different operation modes are implemented using only one hybrid cost function. Furthermore, a new auto-tuning strategy is proposed for the MPC cost function weight factors. The stability of the proposed controller is evaluated in discrete z-domain for abnormalities in the system such as model parameter errors in model of the system.

The rest of this paper is organized as follows. Section II describes the system configuration, space model of the system, and prediction model of the system. Section III illustrates the proposed MPC based method for dual-mode inverter in DG systems. The operation modes and transition process of the system are discussed in detail. Section IV presents the proposed phase detection and adjustment algorithm, which is followed by the stability analysis of system in section V. In section VI, the simulation and experimental results are provided to verify the performance and effectiveness of the proposed control strategy.

3.2 System configuration and model

The block diagram of a single-phase dual-mode inverter with the proposed controller is illustrated in Figure 42. The dc bus of the H-bridge can be fed from energy sources such as such as photovoltaic, wind energy and energy storage systems.

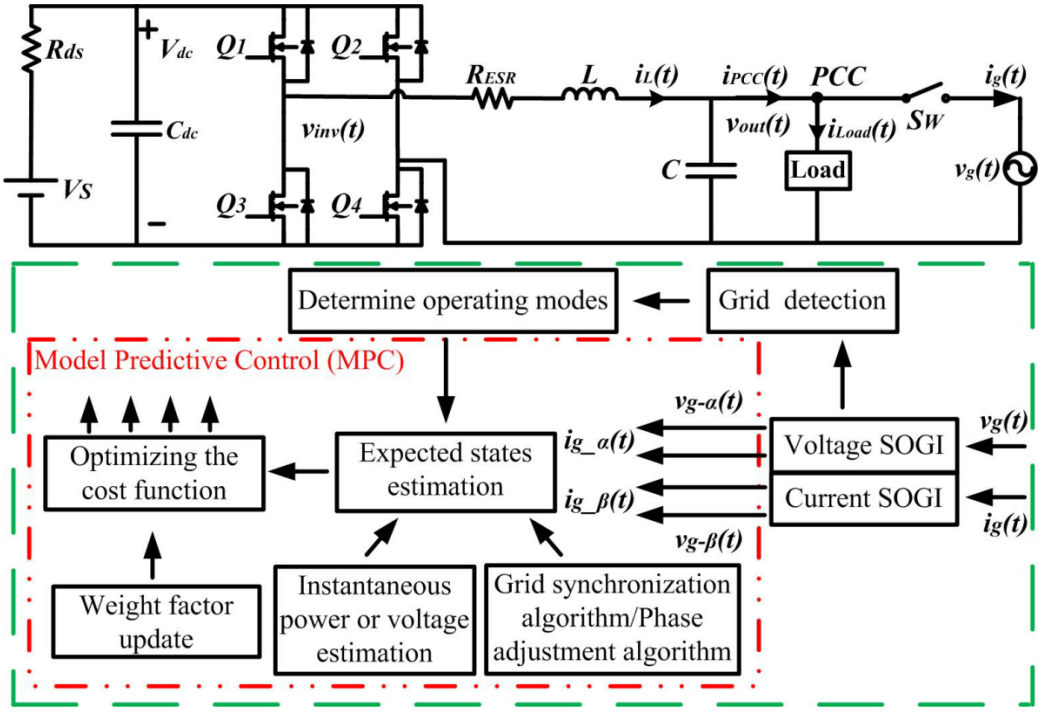


Figure 42: Block diagram of single phase dual-mode inverter with MPC algorithm [57].

The control objective of the system in the grid-connected mode is to regulate the active and reactive power injected or absorbed by inverter (bidirectional power flow). When the grid is disconnected from the system, the inverter operates in islanded mode. In this mode of operation, the control objective of the system is to regulate the local load voltage.

Table 2: The switching states of the single phase dual-mode inverter.

	S_1	S_2	S_3	S_4	$\psi(t)$	$V_{inv}(t)$
State 1	0	0	1	1	0	0
State 2	1	1	0	0	0	0
State 3	1	0	0	1	1	V_{dc}
State 4	0	1	1	0	-1	$-V_{dc}$

The system behavior is defined by the dynamic model consisting of the output filter inductor (L) current and capacitor (C) voltage given by:

$$\frac{d}{dt} i_L(t) = \frac{1}{L}(v_{inv}(t) - v_{out}(t) - i_L(t)R_{ESR}) \tag{22}$$

$$\frac{d}{dt} v_{out}(t) = \frac{1}{C}(i_L(t) - i_{PCC}(t)) \tag{23}$$

$$v_{inv}(t) = \psi(t) v_{dc}(t) \tag{24}$$

where $i_L(t)$ is the filter inductor current, $i_{PCC}(t)$ is the point of common coupling (PCC) current, R_{ESR} represents the total equivalent series resistor of the filter inductor L, $v_{inv}(t)$ and $v_{out}(t)$ are the output voltage of the inverter and the voltage at PCC respectively. In equation (24), $\psi(t)$ is a tri-state function based on the switching states:

$$\psi(t) = S_1(t)S_4(t) - S_2(t)S_3(t)$$

$$S_n = \begin{cases} 1, & \text{Q}_\text{n} \text{ is on} \\ 0, & \text{Q}_\text{n} \text{ is off} \end{cases} \tag{25}$$

State space model of the system is derived as

$$\dot{x} = Ax + Bu = \begin{bmatrix} -\frac{R_{ESR}}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix} x + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} u \tag{26}$$

$$y = C^T x = [0 \quad 1]x$$

where the states and inputs are $x^T = [i_L(\mathrm{t}) , v_{out}(t)]$ and $u^T = [v_{inv}(\mathrm{t}) , i_{PCC}(t)]$ respectively.

According to (22), the discrete-time model of the system is derived by using Euler forward method to predict the states of the system:

$$i_L(k+1) = \frac{T_s}{L}[v_{inv}(k) - v_{out}(k) - i_L(k)R_{ESR}] + i_L(k) \tag{27}$$

$$v_{out}(k+1) = \frac{T_S}{C}(i_L(k) - i_{PCC}(k)) + v_{out}(k) \tag{28}$$

The load current in islanded mode using (6) and (7) is given by:

$$i_{Load}(k+1) = i_L(k+1) - \frac{C}{T_s}(v_{out}(k+1) - v_{out}(k)) \tag{29}$$

In order to achieve a decoupled power control in grid-connected mode, the active and reactive power should be predicted. Assume the instantaneous grid voltage and current are given by:

$$v_g(t) = V_g \sin \omega t \tag{30}$$

$$i_g(t) = I_g \sin(\omega t + \theta) \tag{31}$$

The SOGI module is used to create orthogonal signal for grid voltage and current. The transfer function of the SOGI module is given by:

$$\frac{x_\alpha(s)}{x(s)} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{32}$$

$$\frac{x_\beta(s)}{x(s)} = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{33}$$

The bandwidth of SOGI can be adjusted by properly tuning gain k [47]. The orthogonal output signals of SOGI module can be represented as:

$$\begin{bmatrix} v_{g-\alpha}(t) \\ v_{g-\beta}(t) \end{bmatrix} = \begin{bmatrix} V_g \sin \omega t \\ V_g \sin(\omega t + \frac{\pi}{2}) \end{bmatrix} \tag{34}$$

$$\begin{bmatrix} i_{g-\alpha}(t) \\ i_{g-\beta}(t) \end{bmatrix} = \begin{bmatrix} I_g \sin(\omega t + \theta) \\ V_g \sin(\omega t + \theta + \frac{\pi}{2}) \end{bmatrix} \tag{35}$$

where $v_{g\text{-}\alpha}(t)$ and $v_{g\text{-}\beta}(t)$ are the quadrature time-varying output signals from the voltage SOGI module. $i_{g\text{-}\alpha}(t)$ and $i_{g\text{-}\beta}(t)$ are the quadrature output signals from the current SOGI module. Figure 43 illustrates the simulation results of the SOGI module with distorted input voltage. In Figure 43(a), the input signal to the SOGI module includes 4% 3rd, 6% 5th, 6% 7th, 6% 11th harmonics. At the same time, from 0.07s to 0.17s there is 20% input voltage sag. Figure 43(b) shows the performance of SOGI module with fluctuation in input voltage frequency. The input voltage frequency changed from 60Hz to 59Hz at 0.07 s and then resumes to 60Hz at 0.17s. As it is shown in simulation results of Figure 43, the orthogonal signals are generated from the SOGI module without significant affect by distorted input signal which shows the distortion rejection capability of SOGI module.

By using instantaneous power theory [47], the instantaneous active and reactive power of the inverter is calculated as:

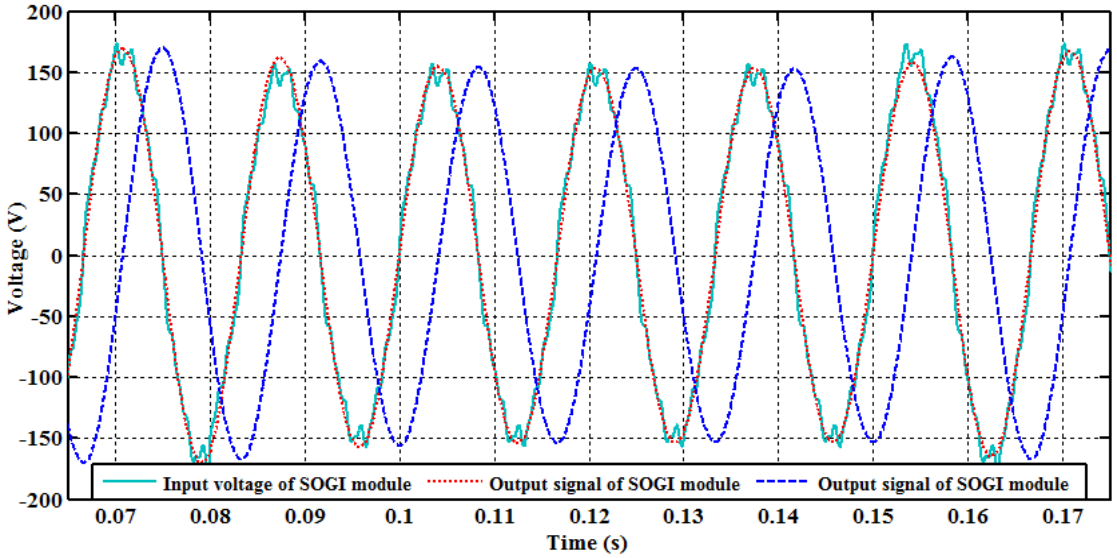
$$\begin{bmatrix} p(k) \\ q(k) \end{bmatrix} = \frac{1}{2}\begin{bmatrix} v_{g-\alpha}(k) & v_{g-\beta}(k) \\ v_{g-\beta}(k) & -v_{g-\alpha}(k) \end{bmatrix} \times \begin{bmatrix} i_{g-\alpha}(k) \\ i_{g-\beta}(k) \end{bmatrix} \tag{36}$$

According to (27), the inverter output active and reactive power can be expressed as:

$$\begin{bmatrix} p(k+1)-p(k) \\ q(k+1)-q(k) \end{bmatrix} = \frac{T_s}{L}\begin{bmatrix} v_{g-\alpha}(k) & v_{g-\beta}(k) \\ v_{g-\beta}(k) & -v_{g-\alpha}(k) \end{bmatrix} \times \left(\begin{bmatrix} v_{inv-\alpha}(k) \\ v_{inv-\beta}(k) \end{bmatrix} - \begin{bmatrix} v_{g-\alpha}(k) \\ v_{g-\beta}(k) \end{bmatrix} \right) \tag{37}$$

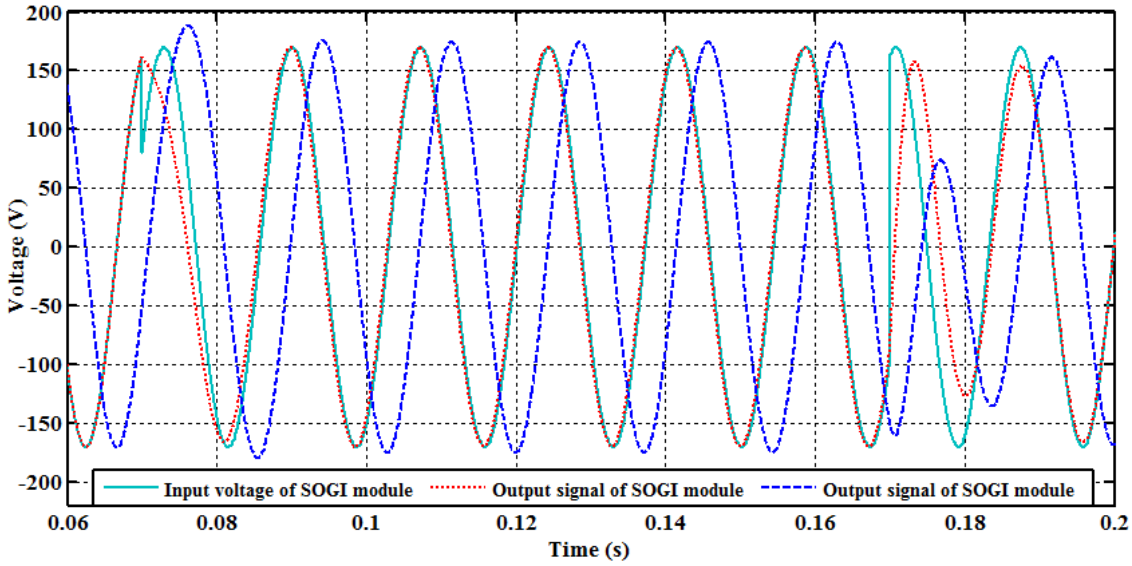
Thus, the predicted model of active and reactive power is derived as

$$\begin{aligned} p(k+1) &= \frac{T_s}{L}[v_{g-\alpha}(k)v_{inv-\alpha}(k) + v_{g-\beta}(k)v_{inv-\beta}(k) - v_{g-\alpha}^2(k) \\ &\quad - v_{g-\beta}^2(k)] + p(k) \\ q(k+1) &= \frac{T_s}{L}\left[v_{g-\beta}(k)v_{inv-\alpha}(k) - v_{g-\alpha}(k)v_{inv-\beta}(k)\right] + q(k) \end{aligned} \tag{38}$$



(a) Input voltage with harmonics and voltage sag.

Figure 43: Performance of SOGI module with distorted input voltage [57].



(b) Input voltage with frequency change.

Figure 43: Continued.

3.3 Control scheme and operation modes

3.3.1 Principle of model predictive control

Application of model predictive control (MPC) in power electronics dates back to the 1980's for high power, low switching frequency applications [71-76]. Since high switching frequencies for the MPC algorithm required fast computation, widespread adoption was not feasible at that time. In the past decade, improvements in high speed microprocessors spurred renewed interest in the application of MPC in power electronics with higher switching frequencies [77, 78].

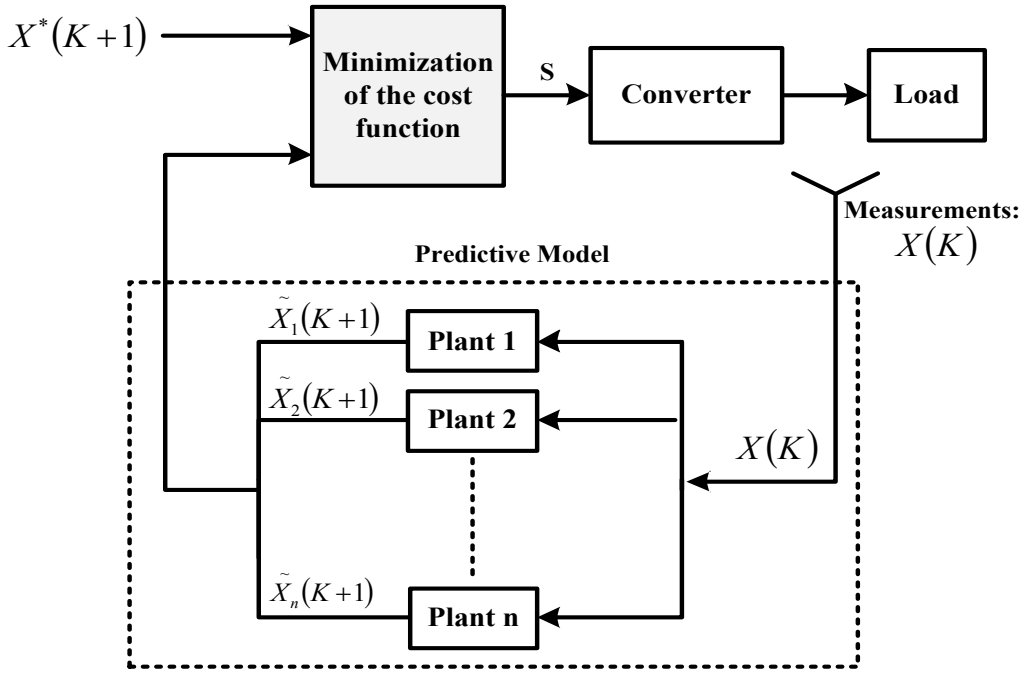


Figure 44: MPC general schematic for power electronics converters.

The main characteristic of MPC is in predicting the future behavior of the desired control variables [77, 79] until a specific time in the horizon. The predicted control variables are used to obtain the optimal switching state by minimizing a cost function. The discrete time model of the control variables used for prediction can be presented as a state space model as follows [79]:

$$x(k+1) = Ax(k) + Bu(k) \tag{39}$$

$$y(k) = Cx(k) + Du(k) \tag{40}$$

A cost function consider the future states, references, and future actuations can then be defined [79]:

$$g = f(x(k), u(k), \cdots, u(k+N)) \tag{41}$$

The defined cost function g should be minimized for a predefined length in the time horizon N; a sequence of N optimal actuations will be determined where the controller only applies the first element of sequence:

$$u(k) = \begin{bmatrix} 1 & 0 & \cdots & 0 \end{bmatrix} \arg\min_{u} g \tag{12}$$

At each sampling time the optimization problem is solved again by using a new set of measured data to obtain a new sequence of optimal actuation. The MPC for power electronics converters can be designed using the following steps [77]:

- Determine the power converter model to specify the input-output relation of the voltages and currents.
- Determine the discrete-time model of the control variables for predicting their future behavior.
- Design the cost function, subject to minimization, which demonstrates the preferred behavior of the power converter.

The general scheme of MPC for power electronics converters is illustrated in Figure 44 [80]. In this block diagram measured variables $X(K)$ are used in the model to estimate predictions $\tilde{X}(K+1)$ of the controlled variables for all of the n possible switching states. These predictions are then evaluated using a cost function which compares them to the reference values $X^*(K+1)$ by considering the design constraints. Finally the optimal actuation, S, is selected and applied to the converter. The general form of the cost function, g, subject to minimization can be formulated as:

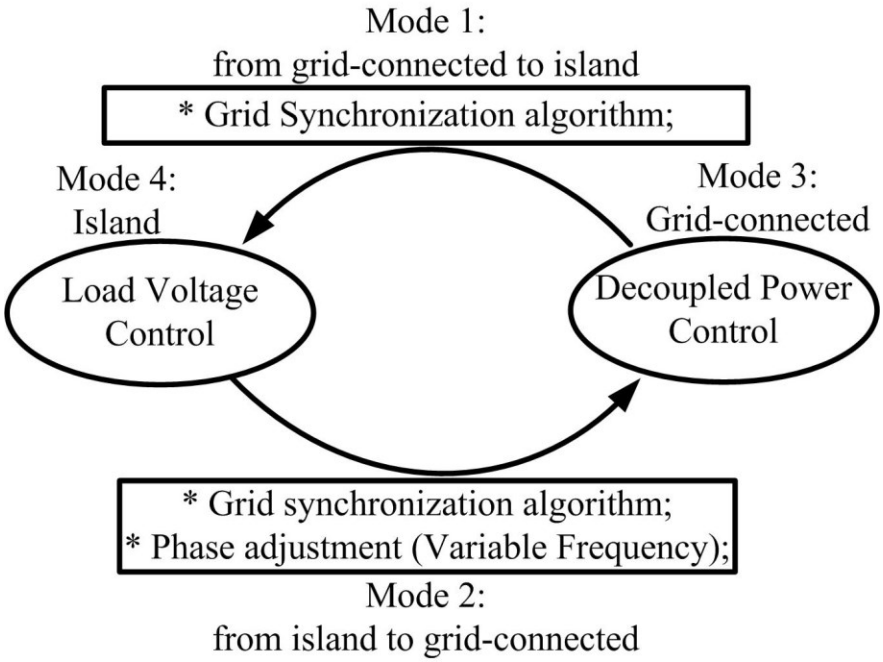


Figure 45: State diagram of different operating modes.

$$g = \left[\tilde{X}_1(K+1) - X_1^*(K+1)\right] + \lambda_1\left[\tilde{X}_2(K+1) - X_2^*(K+1)\right] + \ldots + \lambda_n\left[\tilde{X}_n(K+1) - X_n^*(K+1)\right] \quad (43)$$

where λ is the value or weight factor for each objective.

3.3.2 Operation modes

There are four operation modes in the proposed controller of single-phase dual-mode operation inverter: two steady-state modes (grid-connected and islanded mode) and two transition modes (transition from grid-connected to islanded mode and transition from islanded to grid-connected mode).The summary of the four operating modes and their corresponding control objectives are illustrated in Figure 45. In the MPC algorithm,

each control objective has a corresponding term in the cost function subject to minimization to determine optimal actuation [69]. In this paper a single hybrid cost function subject to minimization for all modes of operation is developed as following:

$$\min g = \begin{cases} \lambda_P g_P + \lambda_Q g_Q + \lambda_V g_V & \vartheta \in \{1-3\} \\ g_V & \vartheta \in \{4\} \end{cases}$$

$$\text{subject to} \quad \tilde{} \quad x(k) + T_S(Ax(k) + Bu(k))$$

$$g_P = \frac{1}{P_{rated}} \left| P_{ref}(k+1) - P_{out}(k+1) \right|$$

$$g_Q = \frac{1}{Q_{rated}} \left| Q_{ref}(k+1) - Q_{out}(k+1) \right| \tag{44}$$

$$g_V = \frac{1}{V_{rated}} \left| V_{ref}(k+1) - V_{out}(k+1) \right|$$

The cost function g includes three penalty terms for active power (P_{out}), reactive power (Q_{out}), and the output voltage (V_{out}). Each penalty term is multiplied by a weight factor (λ_P, λ_Q, λ_V) for purpose of prioritization in the proposed multi-objective predictive controller. The controller uses the proposed auto-tuning weight factor procedure to adjust the priority of the controller objectives based on their quantized tracking error, the detail procedure for auto-tuning of the weight factors will be explained in the next section. The hybrid cost function uses a mode detection algorithm to determine appropriate penalty term to minimize. The modes of operation is flagged by $\vartheta \in \{1-4\}$, where $\vartheta \in \{1\}$ and $\vartheta \in \{2\}$ represent the transition from grid-connected to islanded mode and vice versa respectively, and $\vartheta \in \{3\}$ and $\vartheta \in \{4\}$ represent the grid-connected mode and islanded mode respectively.

Mode 3 in Figure 45 represents grid-connected mode. In this mode, the inverter system is connected to the grid and controls the decoupled active and reactive power

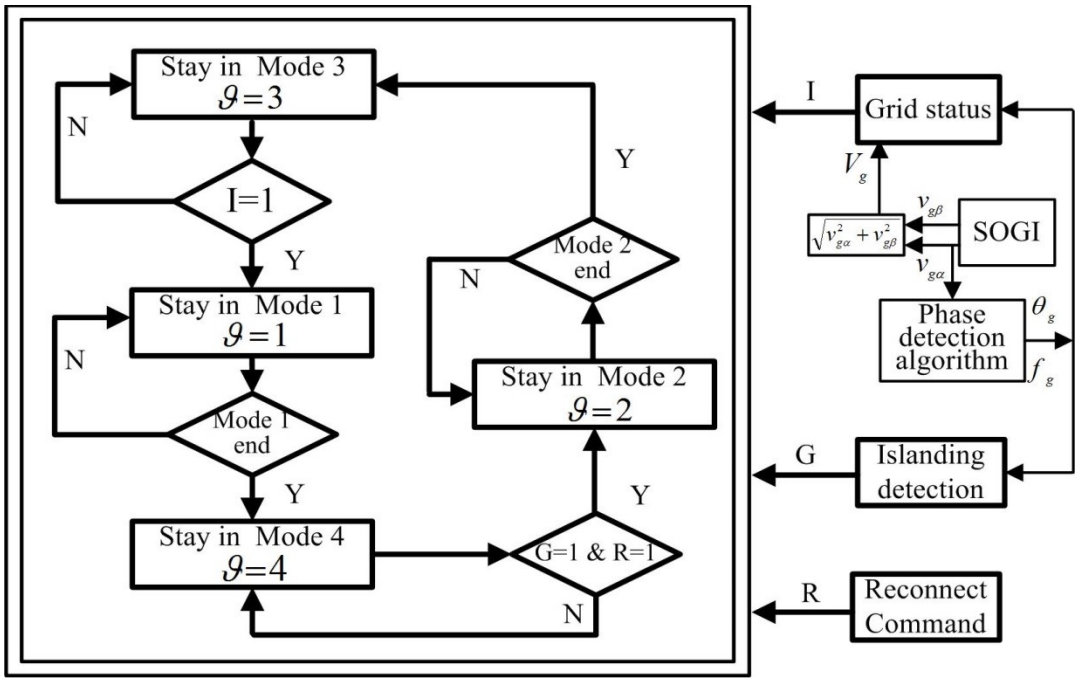


Figure 46: Mode detection and transfer routine.

absorbed from or injected into the grid. The cost function is shown in (44). g_P and g_Q terms determine the real and reactive power regulation in this mode with the help of power prediction model. The voltage regulation term in the cost function exists in this mode to help ensure voltage regulation function in the mode 1, which would be explained in the following part and the working process is shown with flowchart in Figure 54. When the grid is disconnected from the PCC, the single phase inverter system then operates in islanding condition as shown in mode 4 of Figure 45. In this mode, the

voltage across the local loads is regulated to exactly track the load voltage reference which is given by the synchronization algorithm. The cost function is shown in (44).

Based on the operation described above, a state machine has been built and implemented to facilitate the transition between the modes of operation illustrated in Fig. 45. Fig. 46 shows the summary of the mode detection and transition process. As illustrated in Fig. 46, several status indicators were used in the controller algorithm to indicate the operation mode of system. Mode indication is defined with flag. It could have a value from 1 to 4, representing different operation modes. G indicates the condition of the grid. If the grid voltage and frequency is within standard range as indicated in [42], then G will be given the value of 1 indicating the normal grid condition. Otherwise, it will be given a value of 0. Flag I indicates the detection result of islanding detection algorithm. Islanding detection is needed in order to achieve a smooth transition between modes of operation for an islanding scenario. The islanding detection technique proposed in [81] is used in this paper. This phase detection algorithm is estimating frequency of voltage at PCC. The detailed algorithm is available in [82]. When the islanding is detected, I is given the value of 1. Otherwise, it will be 0. The reconnection command from system operator is used to define the value of flag R to show the status of reconnection. R=1 indicates the system is required to get ready for reconnection to grid, otherwise, R remains 0.

When the grid is recovered from the abnormal conditions and the inverter system needs to reconnect to the grid, the controller of system would be triggered to enter into

transfer mode from islanding condition to grid-connected condition. When the transfer mode completed, the grid-connected mode would be triggered.

The implementation of the proposed controller is illustrated in the flowchart of Figure 54 and is summarized as:

- Sense the voltage at PCC, the grid current and the dc link voltage. Determine the operating condition of system according to Figure 46. Update specific flags and weight factor.
- Enter into transfer modes if needed and take related actions accordingly as shown in Figure 46.
- Compute the predicted future behavior of grid voltage and current and calculate the active and reactive power for each possible switching states of the inverter.
- Compute the cost function for each switching state.
- Determine the switching state that minimizes the cost function. Auto-tune weight factors and apply the associated switching signals to the inverter.

3.3.2.1 Grid-connected mode

This mode corresponds to the control mode 3 in Figure 45. When the grid operates normally, the transfer switch SW is kept closed. In this case, the inverter is connected to the grid and the controller works in the grid-connected mode to control the decoupled active and reactive power absorbed from or injected into the grid.

Control of active and reactive power using MPC is the objective for this paper. The instantaneous real and reactive power are defined as

$$P = \mathrm{Re}\left\{ v_g(t).\bar{i}_g(t) \right\}$$
$$Q = \mathrm{Im}\left\{ v_g(t).\bar{i}_g(t) \right\} \tag{45}$$

where $\bar{i}_g(t)$ is the complex conjugate of $i_g(t)$. The reactive power can be predicted using the OSG reference signals

$$\tilde{P}(k+1) = v_{g-\alpha}(k+1)i_{g-\alpha}(k+1) + v_{g-\beta}(k+1)i_{g-\beta}(k+1)$$
$$\tilde{Q}(k+1) = v_{g-\beta}(k+1)i_{g-\alpha}(k+1) - v_{g-\alpha}(k+1)i_{g-\beta}(k+1) \tag{46}$$

where α and β are the orthogonal signals and represent the real and imaginary components of the associated voltage and current. The value of $v_g(k+1)$ can be approximated to be $v_g(k)$ because the line voltage varies at low frequency compared to the switching frequency and thus is approximately constant from switch event to switch event.

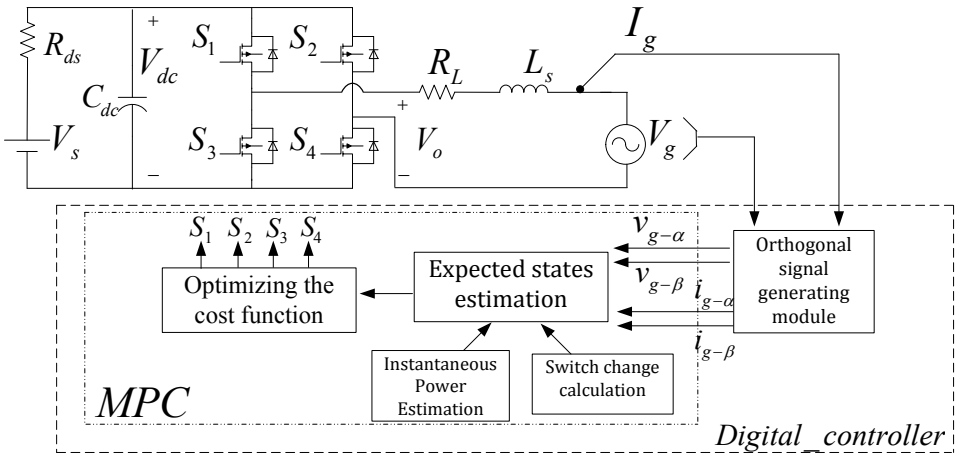


Figure 47: Block diagram of MPC for grid-tied inverter.

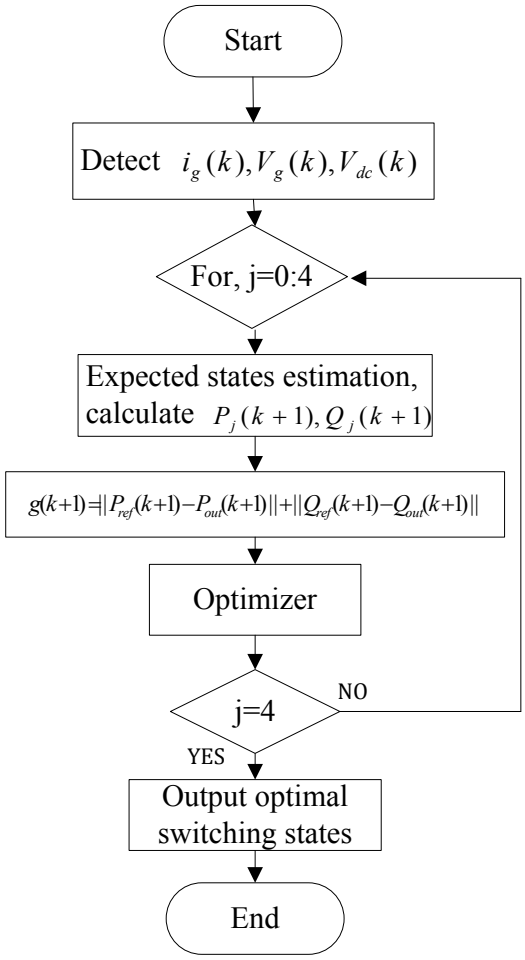


Figure 48: Structure of MPC controller for grid-tied inverter.

The block diagram of MPC for grid-tied inverter is illustrated in Figure 47. The summary of control algorithm is illustrated in Figure 48 and can be described as:

- Detect grid current and voltage.
- Use discrete-time model of the system to predict the grid current and voltage of the next sampling in horizon of time.

- Based on predicted grid current and voltage values, calculate the predicted active and reactive power for each possible switching state.
- Determine cost function *g* for each possible switching state.
- Determine the switching state that minimize the cost function *g*, and apply the optimal switching state to the inverter.

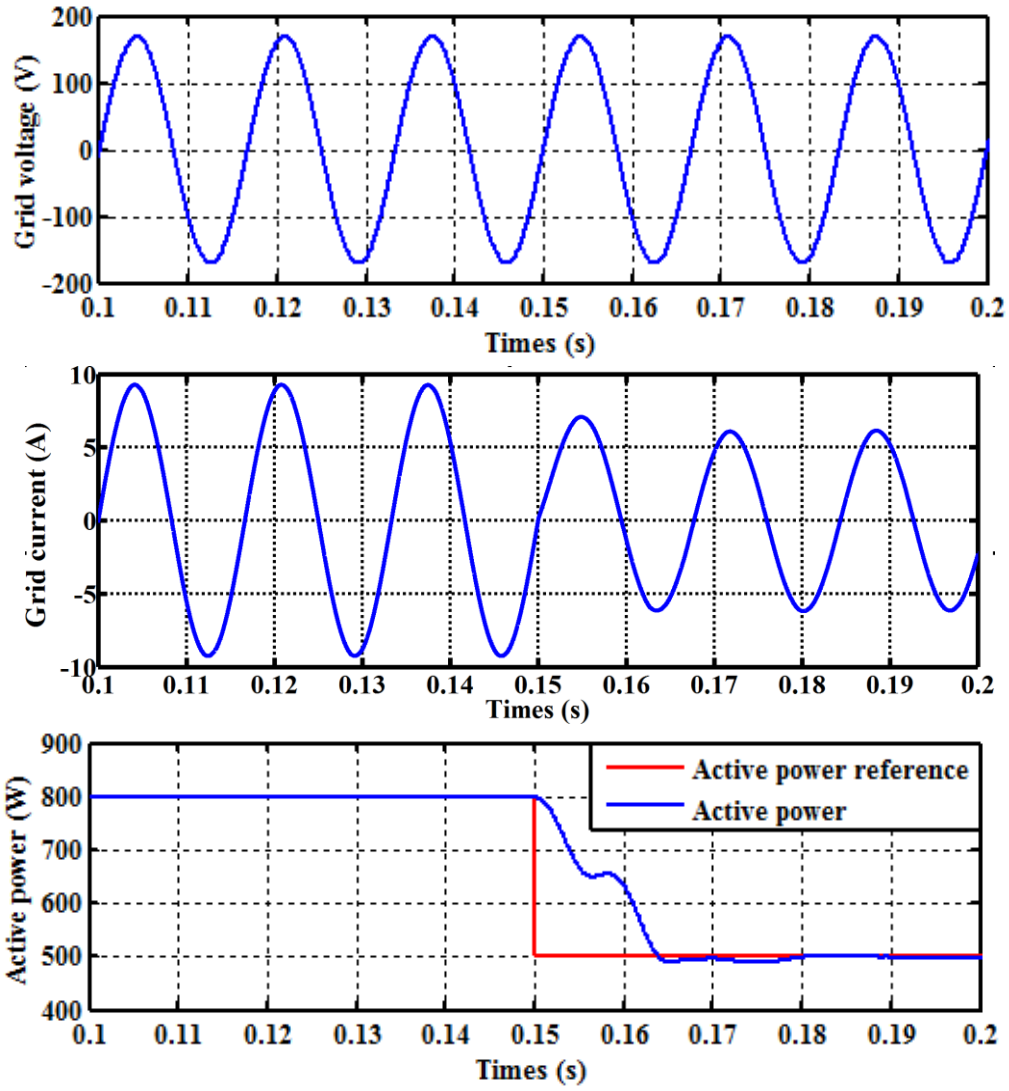


Figure 49: The dynamic performance in grid-connected mode.

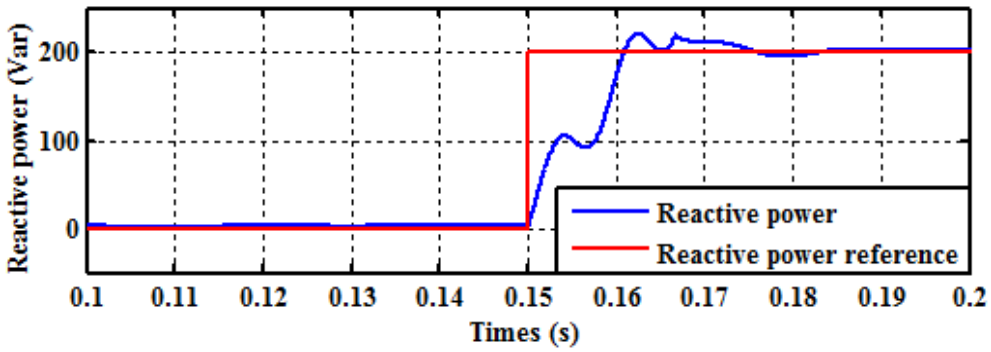


Figure 49: Continued.

This enables the inverter system with the capability of bidirectional power flow and decoupled active and reactive power control. In grid-connected mode ($\vartheta \in \{3\}$), the system is connected to the grid and the major control objectives are to regulate the active and reactive power injected into the grid. The terms g_P and g_Q in cost function are regulating the active and reactive power in this mode using power prediction model. The voltage regulation term in the cost function is to ensure voltage regulation during the transition modes which will be explained in the next section.

The dynamic performance of the proposed control algorithm in grid-connected mode with step change on active and reactive power (P and Q respectively) is presented in Figure 49. In this case, the references of active power and reactive power step changes at 0.15s simultaneously. The sampling time in this case is 10μs. As it is shown, the active and reactive power at the grid side are regulated in about 0.04s without significant overshoot. Also, the tracking error in steady state is less than 1% in this case study.

3.3.2.2 Island mode

When the system is disconnected from the grid at PCC, the inverter system operates in islanded mode which is Mode 4 ($\vartheta \in \{4\}$). In this mode, the voltage across the local loads is regulated using the cost function to track the load voltage reference which is given by a synchronization algorithm. The detail of synchronization algorithm will be presented in the following section.

Figures 50 and 51 show the dynamic performance of the proposed system in islanded mode. In Figure 50, the load resistance is changed from 30 ohm to 15 ohm at 0.2 s. As it is shown the output voltage is regulated and the load current responded to this load change smoothly. The performance of inverter system with non-linear loads in islanded mode is also evaluated as shown in Figure 51. It is observed that the output voltage has no distortion and the Total Harmonics Distortion (THD) of the output voltage for this case study is 2.3%. Benefitting from the nonlinear property of MPC method, the proposed controller could provide high impedance to reject the distortion from nonlinear load, which is challenging to achieve this with conventional linear control methods

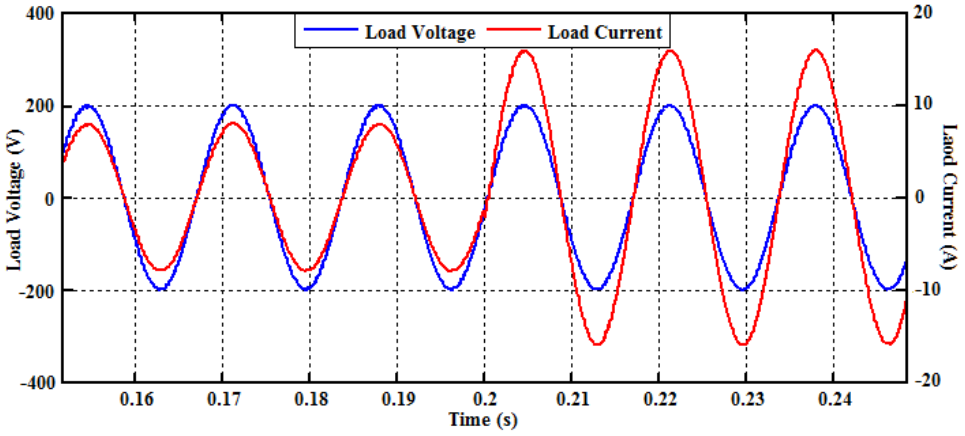


Figure 50: Dynamic performance of load current change in island mode.

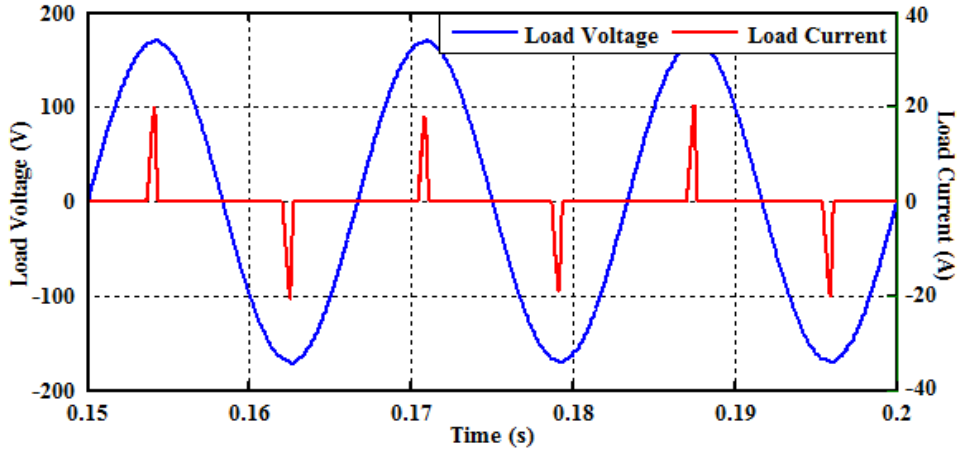


Figure 51: Steady state performance of non-linear loads in island mode.

Figure 50 shows simulation results about the dynamic performance of the proposed system in island mode. In this case, the load resistance step changes from initial value (30 Ohm) to one half of that at 0.2 s. The output voltage, as shown in the result, keeps continuous and regulated without big change. And the load current returns to the new stable state quickly and smoothly. Except the linear loads, the performance of

inverter system with non-linear loads in island mode is also evaluated as shown in Figure 51. It is observed that the output voltage has no distortion in this case. The THD of the output voltage in this case is 2.3%. It shows that the proposed controller could provide high impedance to reject the distortion from nonlinear load, which would not be implemented easily with conventional liner control methods and this contributes from the nonlinear property of MPC method.

3.3.2.3 Transfer mode 1: from grid-connected to islanding mode

This control mode corresponds to mode 1 in Figure 45. When the grid is under fault conditions such as voltage sag/swell or interrupts, the switch at grid side is tripped by the fault detection signal, and the inverter is subsequently disconnected from the grid. When the inverter detects the occurrence of islanding, the controller will work in this mode as shown in Figure 46.

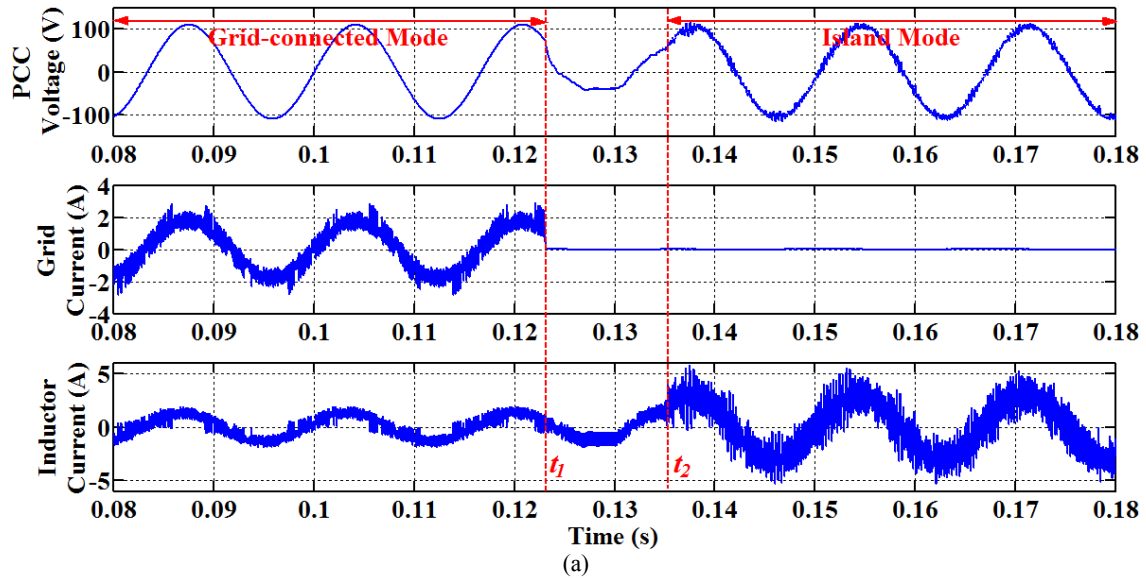
In order to have a seamless transfer from grid-connected to islanded mode, a fast and robust synchronization algorithm is needed. This synchronization algorithm is used to track the phase angle and magnitude of the grid voltage during the transition mode and provide voltage reference for islanded mode. The working principle of synchronization algorithm to determine the load voltage reference value for islanded mode is presented in following section. The transition process from grid-connected mode to islanded mode is as following:

- Islanding detection and choosing transition mode ($\vartheta \in \{1\}$),
- Synchronize the phase angle and magnitude of the PCC voltage,
- Calculate the load voltage reference according to synchronization algorithm,

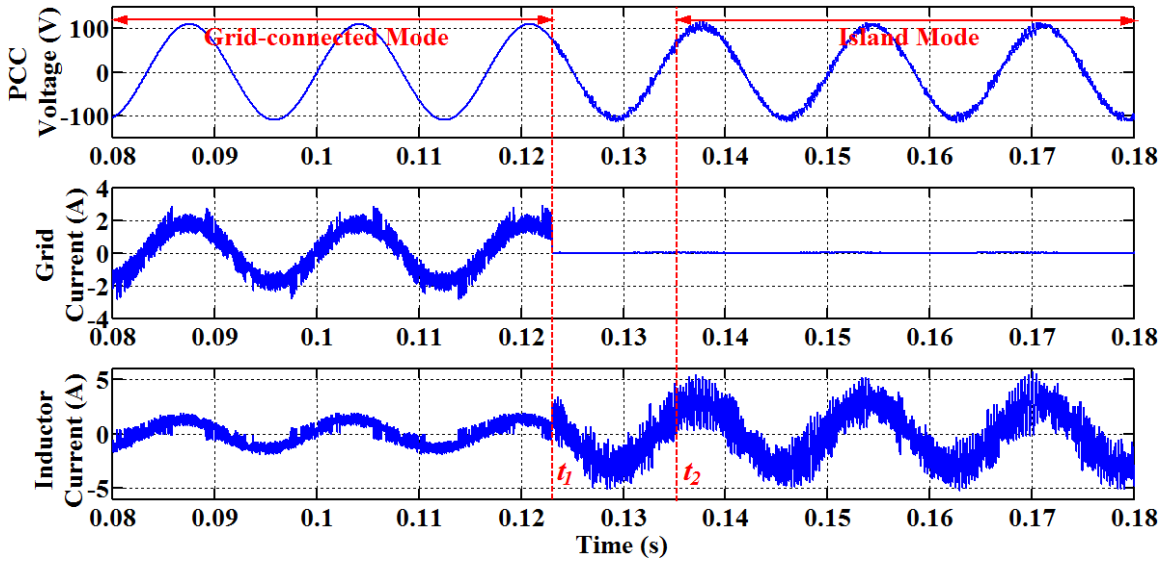
- Trigger mode 4 ($\vartheta \in \{4\}$) for islanding operation.

Figure 52 shows the simulation results in the transition mode 1 from grid-connected to islanded mode. Two cases are considered, the first case in Figure 52 (a) is not considering the voltage regulation over transition mode, but the second case in Figure 52 (b) is considering the voltage regulation over the transition mode. In both cases, the system operates in grid-connected mode initially, then islanded condition is emulated to happen at the time t_1 (0.123s). After the islanding detection, the controller enters into transition mode 1 and gets the reference value through synchronization process. The time t_1 (0.123s) to t_2 (0.135s) is representing the transition process. Then, the controller stays in islanded mode. The sampling time in both cases is 10μs.

If the voltage regulation corresponding term in the cost function is eliminated, there would be no voltage regulation function in transition process. Then the voltage at PCC will not be regulated well as shown in simulation results of Figure 52 (a). As shown in this figure, the PCC voltage is interrupted and highly distorted during the transition period. The proposed controller is regulating the PCC voltage during the transition mode. The simulation results in Figure 52 (b) show that the PCC voltage is continuously regulated in whole process without significant overshoot and distortion.



(a)



(b)

Figure 52: Results of seamless transfer from grid-connected to island mode (a) without voltage regulation (left). (b) with voltage regulation (right).

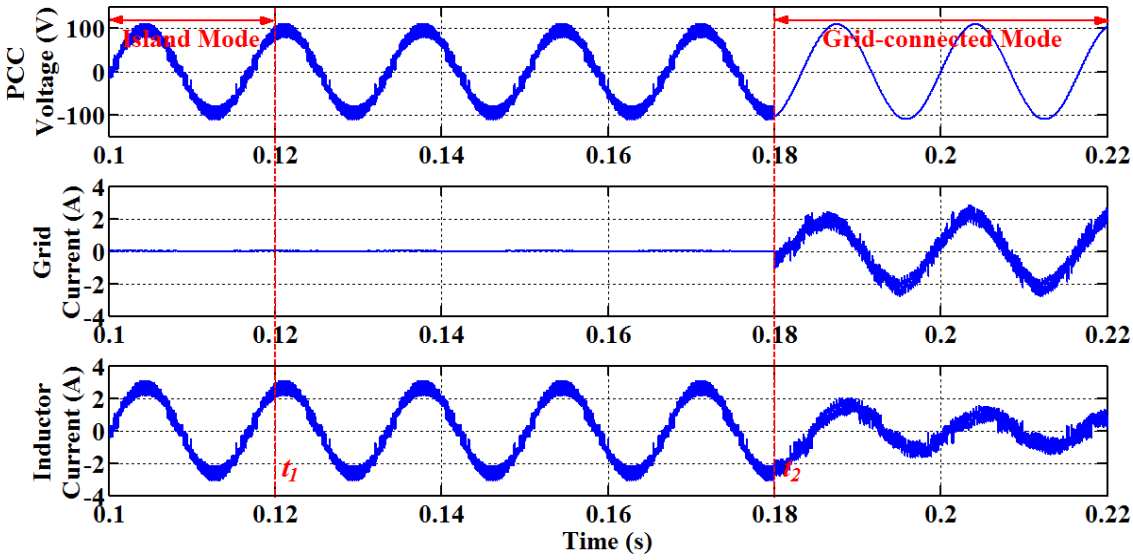


Figure 53: Results of seamless transfer from island to grid-connected mode.

3.3.2.4 Transfer mode 2: from islanding to grid-connected mode.

This control mode corresponds to mode 2 in Figure 45.

In order to have a seamless transition, the load voltage should match the phase of the grid voltage before the inverter is reconnected to the grid. In this mode, the controller firstly detects the phase difference between the grid voltage and the load voltage through the phase adjustment algorithm which will be presented in the following section. By smoothly adjusting the frequency of load voltage reference before grid re-connection, the output voltage of the inverter system can track the grid voltage during the transfer process. The transition process from islanded mode to grid-connected mode is as following:

- Grid-connected mode detection and choosing transition mode ($\vartheta \in \{2\}$),

- Adjust the phase of the inverter output voltage by phase adjustment algorithm to sync with the grid voltage,
- Reconnect system to the grid and trigger mode 3 ($\vartheta \in \{3\}$).

Figure 53 shows the simulation results in this transition mode from islanded to grid-connected mode. In this case, the system operates in islanded mode initially, then at time t_1 (0.12s), the grid is ready to reconnect to the system. During the phase adjustment from t_1 (0.12s) to t_2 (0.18s), the controller stays in islanded mode. As it is shown, the seamless transition is achieved with continuous and smooth regulation of PCC voltage during the whole transition process. Also, the grid current is smooth in whole process without significant overshoot and distortion.

3.3.2.5 Controller Flowchart

The flowchart of the proposed controller algorithm is illustrated in Figure 54. The algorithm starts by measuring the voltage at PCC, the dc-link voltage, and the grid current. Then, it detects the modes of operation accordingly. The corresponding system model and control variables prediction will be used according to the detected mode of operation. The cost function will be formulated according to modes of operation. Then the cost function is minimized to determine the optimal switching state for instant (k+1). During the minimization of cost function, the auto-tuning weight factor procedure presented previously is executed. At the end of the loop, the mode detection will be executed again. The synchronization and phase adjustment algorithm will be executed if the transition modes are detected.

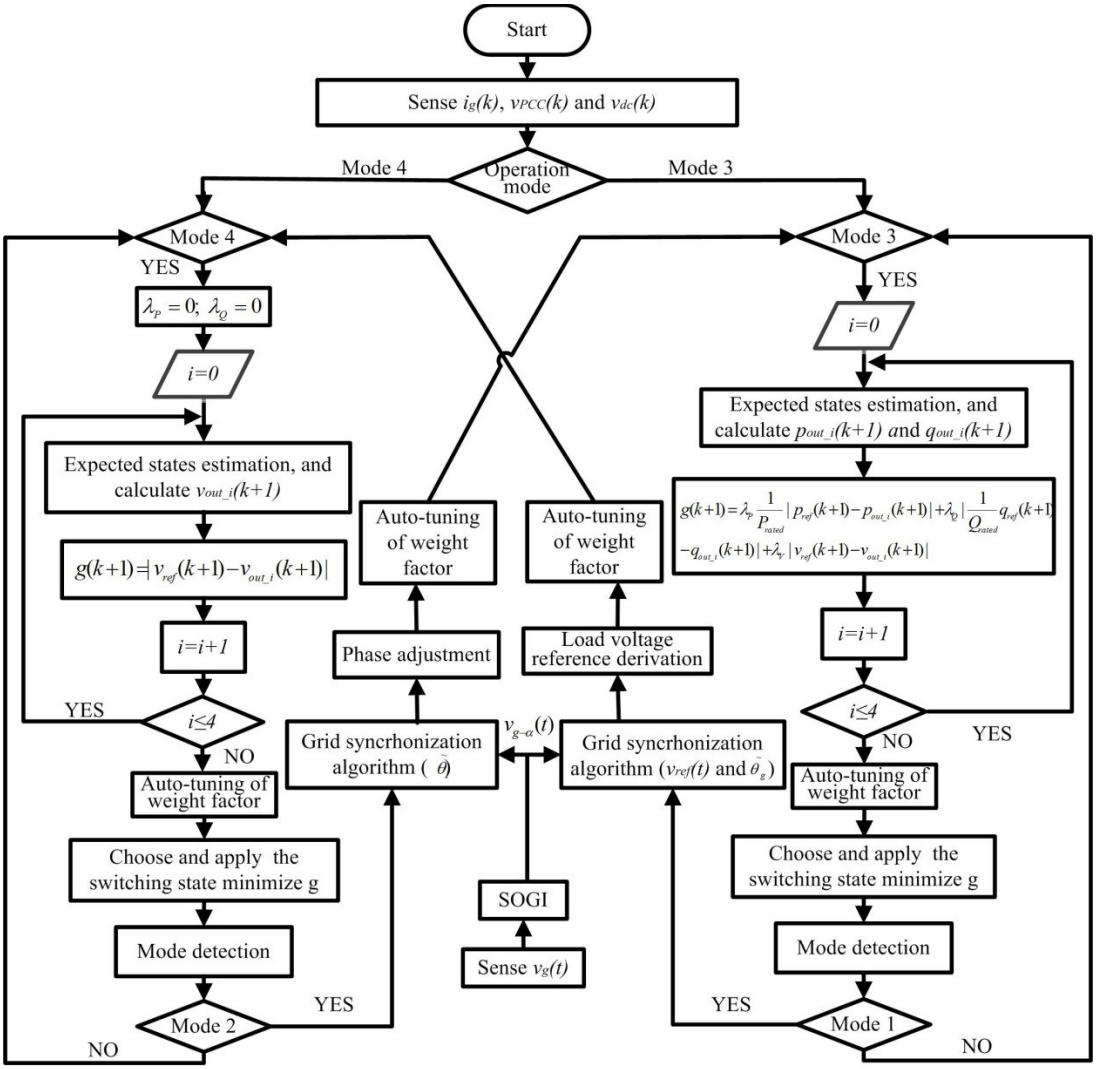


Figure 54: Flowchart of proposed seamless transfer control strategy [57].

3.4 Proposed synchronization and phase Adjustment algorithms

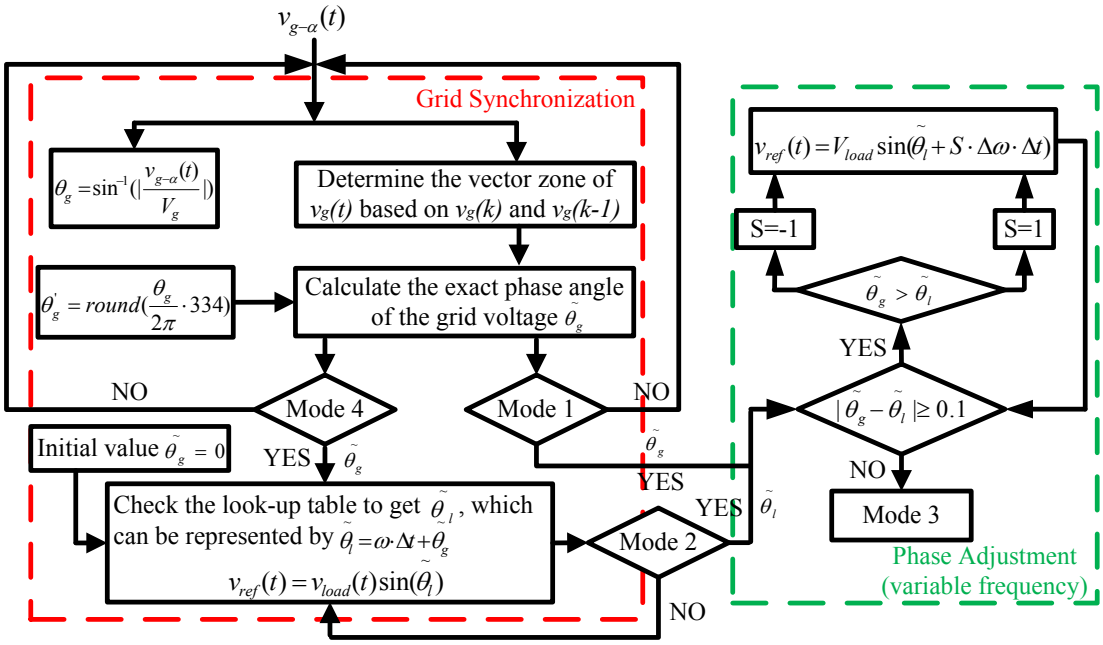


Figure 55: The flow chart of Synchronization and phase adjustment algorithm [57].

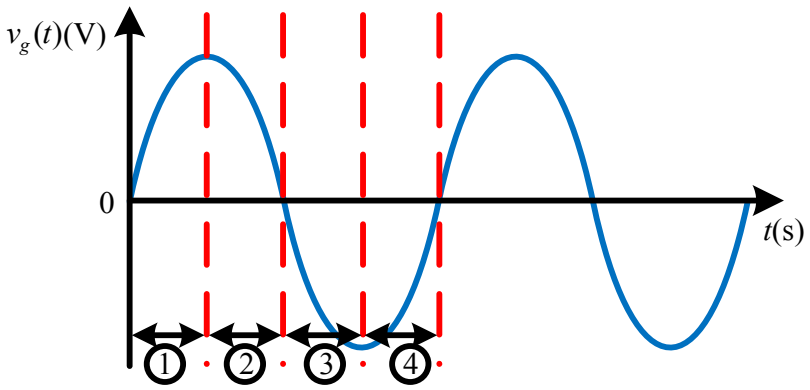


Figure 56: Zone definition of the grid voltage in the proposed synchronization algorithm.

This paper proposed an algorithm in order to achieve grid synchronization with fast response and simple structure during the transition modes. The proposed gird synchronization and phase adjustment is illustrated in Figure 55. The synchronization algorithm is calculating the phase angle of the grid voltage to determine the voltage reference for islanded mode. As it is shown in Figure 55, the input of synchronization algorithm is $v_{g\text{-}\alpha}(t)$, which is one of the SOGI output signals, thus the phase angle of the grid voltage is computed by

$$\theta_g = \sin^{-1}\left(\left|\frac{v_{g-\alpha}(t)}{V_g}\right|\right) \tag{48}$$

where $V_g = \sqrt{v_{g-\alpha}^2 + v_{g-\beta}^2}$.

A look-up table of a sine function with saved values is used to obtain the reference voltage for islanded mode. In order to get the appropriate point in look-up table with the right phase angle information of the grid voltage with the proposed detection method, four zones are defined in one fundamental period. The zones location are illustrated in Figure 56 and can be determined by using the following function:

$$\tilde{\theta}_g = \begin{cases} \theta_g^{'}, (Zone\_1) & if \quad v_g(k) > 0 \,\&\, v_g(k) > v_g(k-1) \\ \frac{n_T}{2} - \theta_g^{'}, (Zone\_2) & if \quad v_g(k) > 0 \,\&\, v_g(k) < v_g(k-1) \\ \frac{n_T}{2} + \theta_g^{'}, (Zone\_3) & if \quad v_g(k) < 0 \,\&\, v_g(k) < v_g(k-1) \\ n_T - \theta_g^{'}, (Zone\_4) & if \quad v_g(k) < 0 \,\&\, v_g(k) > v_g(k-1) \end{cases} \tag{49}$$

where $\theta_g^{'} = round(\frac{\theta_g}{2\pi} \cdot n_T)$.

The phase angle information of the grid voltage with the proposed detection method, four zones are defined in one fundamental period. The zone location could be determined by vg(k) and vg(k-1) as shown in Figure 56.

In transition mode 2, the synchronization algorithm executed along with the phase adjustment algorithm illustrated in Figure 55. The phase adjustment algorithm starts by comparing the grid voltage phase to the local load voltage phase. If the phase difference is within the preset acceptable range (which is normally determined by the system settings; in this paper it is set to 0.1 degree), the system will be connected to the grid. But if the grid voltage leads the load voltage, the controller will increase the load voltage frequency. Thus, the phase difference could be reduced before re-connecting to the grid. This procedure continues until the phase different will be within the preset value. If the grid voltage is lagging the load voltage, in this case the load voltage frequency will be decreased. The deviation frequency $\Delta\omega$ in Figure 55 determines the time required for this phase adjustment. Though the larger deviation frequency could reduce the adjusting time required, it could also introduce a frequency distortion into the system. So an engineering trade-off should be applied to determine the $\Delta\omega$.

The output performance of the proposed synchronization and phase adjustment algorithm is shown in Figure 57. In this case, the grid voltage with amplitude 170 V and frequency 60 Hz as normal is considered. The algorithm is evaluated with 4% 3^{rd}, 6% 5^{th}, 6% 7^{th}, 6% 11^{th} harmonic components from 0.07 s to 0.22 s. At time 0.22 s, the fundamental frequency of grid voltage is changed from 60Hz to 59Hz and then stays in

59 Hz condition. As it is shown in Figure 57, the detected phase angle from synchronization algorithm is not significantly affected by the grid distortions.

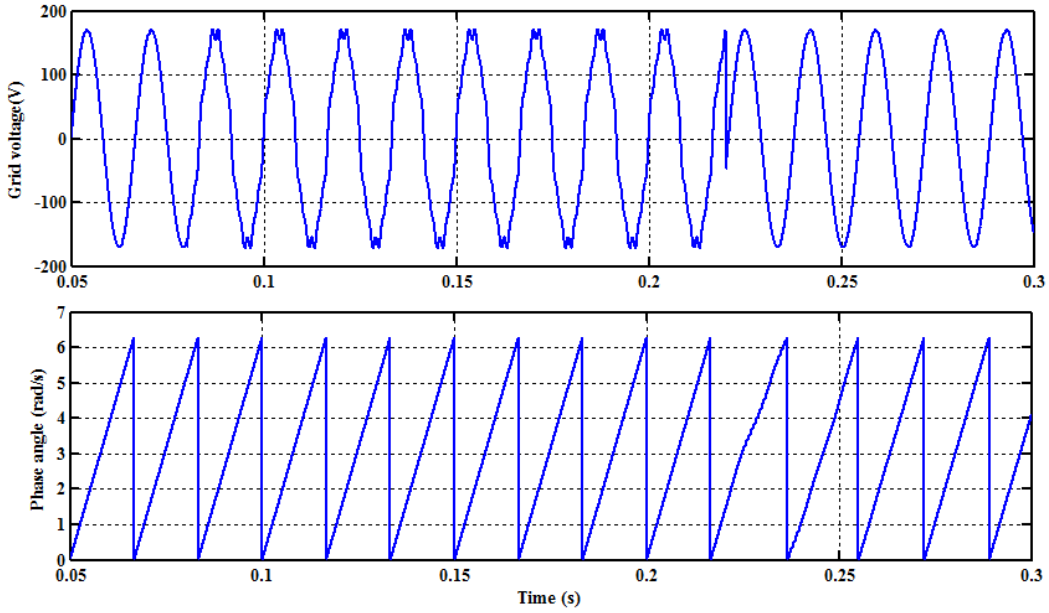


Figure 57: Synchronization performance with distorted grid voltage.

3.5 Auto-tuning of the weight factors

In this section presents an auto-tuning method for the online determination of the MPC cost function weight factors (λ_P, λ_Q, λ_V). The weight factors of the MPC cost

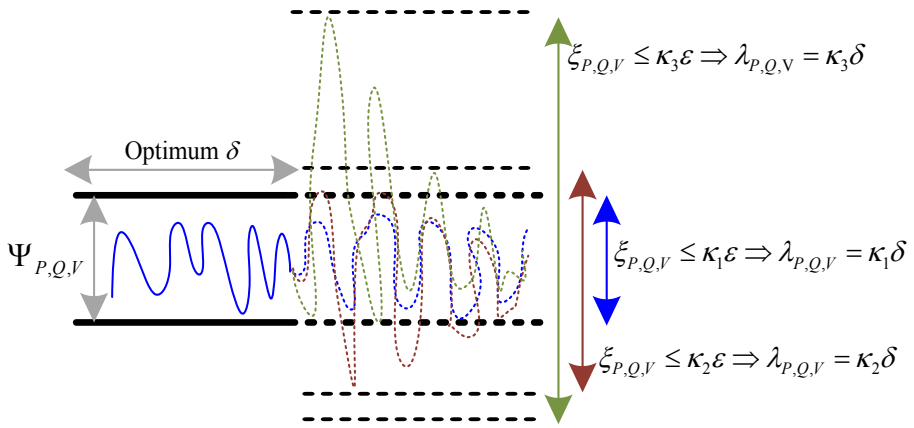


Figure 58: Tracking error quantization of the controller objectives for auto-tuning of the weight factors.

function directly affect the controller performance and robustness under abnormal operating conditions such as model parameter mismatch. The auto-tuning strategy in this section proposes an optimal weight factor selection over each sampling time sector. The optimal selection of weight factors is done by predicting the absolute tracking error of the all the controller objectives which are active power, reactive power, and output voltage in islanded mode. The summary of the weight factor auto-tuning is illustrated in Figure 59. After minimization of the cost function g, the switching that corresponds to the minimum g will be applied to the converter. Then the algorithm moves into auto-tuning of weight factor. The tuned weight factors will be used for the minimization of

(44) at next sampling period for sufficiently small sampling time. In practice, much of the evaluations for tuning of weight factor are based on the computations that have been already done. Thus, using the already computed cost function, we are able to split the cost function (44) into three parts where each corresponds to individual control objectives:

$$g_P = \frac{1}{P_{rated}} \left| P_{ref}(k+1) - P_{out}(k+1) \right| \le \Psi_P \tag{50}$$

$$g_Q = \frac{1}{Q_{rated}} \left| Q_{ref}(k+1) - Q_{out}(k+1) \right| \le \Psi_Q \tag{51}$$

$$g_V = \frac{1}{V_{rated}} \left| V_{ref}(k+1) - V_{out}(k+1) \right| \le \Psi_V \tag{52}$$

where Ψ_P, Ψ_Q, and Ψ_V are the acceptable tracking error values. The minimum value of all cost functions g_P, g_Q, and g_V for all possible switching states are selected

$$\xi_P = \min g_P \tag{53}$$

$$\xi_Q = \min g_Q \tag{54}$$

$$\xi_V = \min g_V \tag{55}$$

The next step is to evaluate the magnitude of (53)-(55) with a sufficiently small number ε as following

$$\begin{aligned} \xi_P \le \varepsilon &\Rightarrow \lambda_P = \delta \\ \xi_Q \le \varepsilon &\Rightarrow \lambda_Q = \delta \\ \xi_V \le \varepsilon &\Rightarrow \lambda_V = \delta \end{aligned} \tag{56}$$

The statement (56) is presenting that, if the optimal g_P, g_Q, and g_V are small enough (less than a defined small number ε), then the weight factors λ_P, λ_Q, λ_V are determined to be equal to a sufficiently small number δ as their initial value.

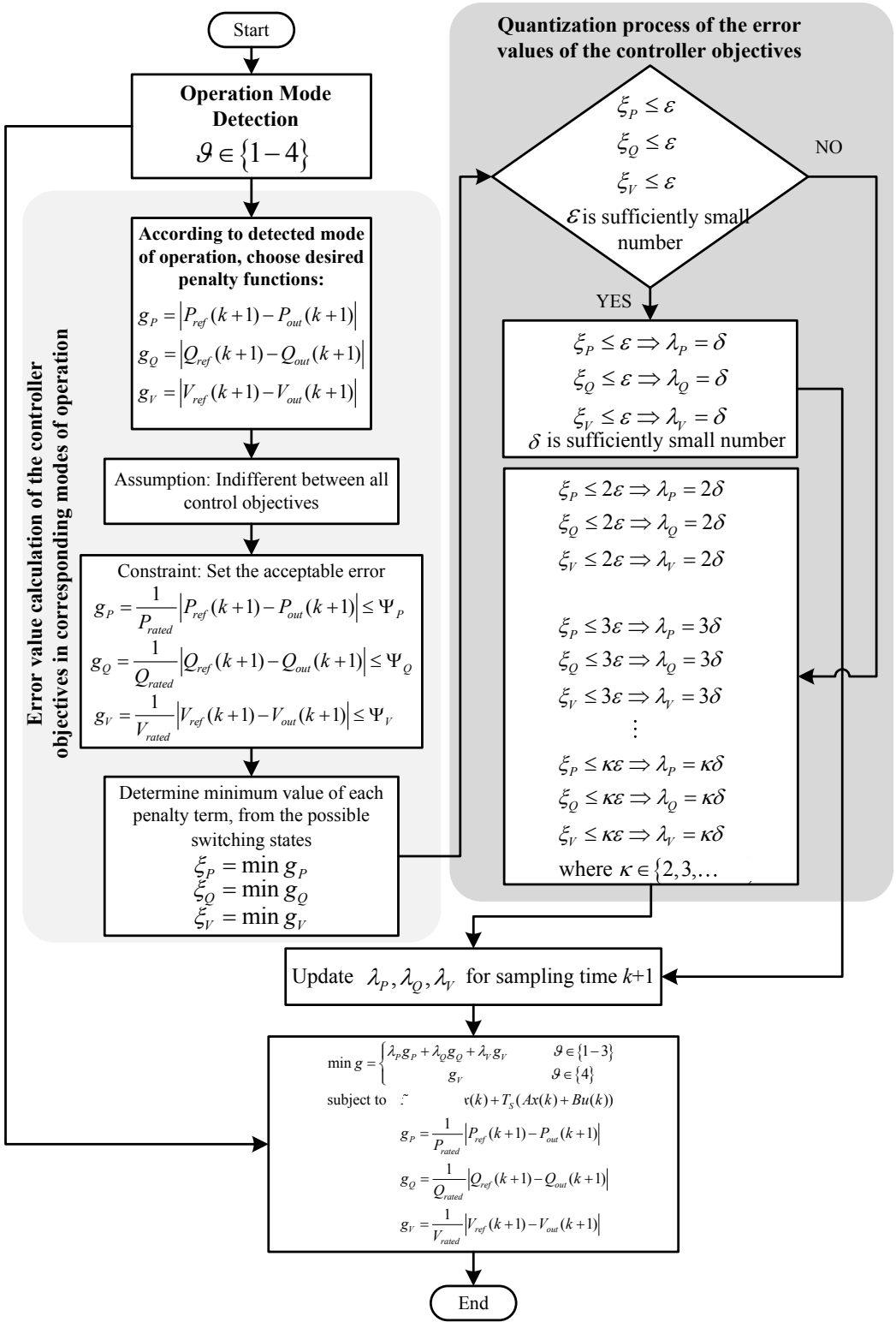


Figure 59: Auto-tuning algorithm of the weight factors in the hybrid cost function.

In case each line condition in (56) is not satisfied, a larger value for that weight factor (λ_P, λ_Q, or λ_V) should be selected in order to give higher gain to their corresponding cost function for minimization at the next sampling time k+1. The evaluation of ξ_P, ξ_Q, ξ_V when their values are more than ε is as following

$$\begin{aligned}
&\xi_P \le 2\varepsilon \Rightarrow \lambda_P = 2\delta \\
&\xi_Q \le 2\varepsilon \Rightarrow \lambda_Q = 2\delta \\
&\xi_V \le 2\varepsilon \Rightarrow \lambda_V = 2\delta \\
&\\
&\xi_P \le 3\varepsilon \Rightarrow \lambda_P = 3\delta \\
&\xi_Q \le 3\varepsilon \Rightarrow \lambda_Q = 3\delta \\
&\xi_V \le 3\varepsilon \Rightarrow \lambda_V = 3\delta \\
&\vdots \\
&\xi_P \le \kappa\varepsilon \Rightarrow \lambda_P = \kappa\delta \\
&\xi_Q \le \kappa\varepsilon \Rightarrow \lambda_Q = \kappa\delta \\
&\xi_V \le \kappa\varepsilon \Rightarrow \lambda_V = \kappa\delta \\
&\text{where } \kappa \in \{2,3,\ldots
\end{aligned} \tag{57}$$

The statements in (57) quantized the ξ_P, ξ_Q, ξ_V, the weight factors λ_P, λ_Q, λ_V are determined based on ξ_P, ξ_Q, ξ_V magnitude when comparing to κ multiples of ε till the statement in (56) is satisfied for each individual objectives. The corresponding values of λ_P, λ_Q, λ_V are multiplication of κ by ε. This error quantization method is graphically illustrated in Figure 58. In this figure $\kappa_3 > \kappa_2 > \kappa_1$ thus more weight will be given to the penalty term that has more ξ as illustrated. This strategy for selecting the weight factors, based on the absolute errors ξ_P, ξ_Q, ξ_V is illustrated in Figure 59. This procedure will be repeated every sampling time, thus during every sampling period the weight factor will

be tuned online and applied to the minimization procedure of the cost function (44) at next sampling time.

3.6. Stability analysis

There are four switching states for single phase inverter and three fixed inverter output voltage vectors to be chosen. Assume the optimal voltage vector $v_o(k)$ can be expressed with the continuous voltage and the quantization error vectors as

$$v_o(k) = v_{o\_c}(k) + \gamma(k) \tag{58}$$

where $v_{o\_c}(k)$ is the continuous-voltage vector that can make the tracking error in next sampling time converge to 0 and $\gamma(k)$ is the quantization error vector.

The current tracking error of the next sampling time can be calculated in discrete time

$$\begin{aligned} e(k+1) &= i_L^*(k+1) - i_L(k+1) \\ &= i_L^*(k+1) - \frac{1}{R_{ESR}T_s + L}[Li_L(k) + T_s v_o(k+1) - T_s v_{PCC}(k+1)] \end{aligned} \tag{59}$$

where $i^*(k+1)$ is the future reference load current vector.

According to discrete-time mode of system, the continuous-voltage vector at next sampling time can be calculated by

$$v_{o-c}(k+1) = -\frac{L}{T_s} i_L(k) + \frac{RT_s + L}{T_s} i_L^*(k+1) + v_{PCC}(k+1) \tag{60}$$

To analyze the stability of the control system, a discrete Lyapunov function is defined, which is definite positive, as

$$V[e(k)] = \frac{1}{2} e^T(k) e(k) \tag{61}$$

According to (60) and (61), the rate of change of Lyapunov function can be calculated as

$$\begin{aligned} \Delta V[k] = V[e(k+1)] - V[e(k)] = \frac{1}{2}(i_L^*(k+1) - \frac{1}{R_{ESR}T_s + L}\{Li_L(k) + \\ T_s v_{o\_C}(k+1) + T_s\gamma(k+1) - v_g(k+1)\})^T \times (i_L^*(k+1) - \frac{1}{R_{ESR}T_s + L}\{ \\ Li_L(k) + T_s v_{o\_C}(k+1) + T_s\gamma(k+1) - v_g(k+1)\}) - \frac{1}{2} e^T(k) e(k) \end{aligned} \tag{62}$$

Since the voltage vector $v_o(k+1)$ is constrained in the finite set, the current $i_L(k)$ is bounded, and thus the current control error is bounded. In addition, $v_{o\_c}(k)$ is bounded because of the boundedness of $i_L(k)$ and $v_g(k)$. Thus, for all $e(k) \in \Gamma$, there exists a constant $\zeta > 0$ satisfying $\|\gamma(k+1)\| \le \zeta$.

According to (62), the rate of change of Lyapunov function can be expressed as

$$\begin{aligned} \Delta V[k] &= -\frac{1}{2} e^T(k) e(k) + \frac{1}{2}(\frac{T_s}{R_{ESR}T_s + L})^2 \gamma^T(k)\gamma(k) \\ &\le -\frac{1}{2} e^T(k) e(k) + \frac{1}{2}(\frac{T_s}{R_{ESR}T_s + L})^2 \xi^2 \end{aligned} \tag{63}$$

On the other hand, according to (58)~(60), it can be obtained that

$$\|e(k+1)\| = \frac{T_s}{R_{ESR}T_s + L}\zeta \tag{64}$$

It implies that the control system is uniformly ultimately bounded, as time increases, the tracking errors converge in the compact set as

$$\Lambda = \{e \mid \|e\| \le \frac{T_s}{R_{ESR}T_s + L}\zeta\} \tag{65}$$

When the model error exists, (27) should be revised as:

$$i_{L\_real}(k+1) = \frac{1}{R_{ESR}T_s + L_{real}}[T_s v_o(k) - T_s v_g(k) + L_{real} i_L(k)] \tag{66}$$

According to (60), (65) and (66), we can get the actual current error vector at the *k+1th* sampling time as:

$$\begin{aligned} e_{real}(k+1) = i_{real}(k+1) - i_L^*(k+1) = \frac{L_{real} - L}{R_{ESR}T_s + L_{real}} i_L(k) - \\ \frac{L_{real} - L}{R_{ESR}T_s + L_{real}} i_L^*(k+1) + \frac{T_s}{R_{ESR}T_s + L_{real}}\gamma(k) \end{aligned} \tag{67}$$

Assuming the sampling time would be extremely small, and R_{ESR} is normally with a very small value. Thus the norm of error vector $e_{real}(k+1)$ satisfies

$$\begin{aligned} \|e_{real}(k+1)\| &\le \left\|(1 - \frac{L}{L_{real}})[i_L(k) - i_L^*(k+1)]\right\| + \left\|\frac{T_s}{L_{real}}\gamma(k)\right\| \\ &\le \left\|(1 - \frac{L}{L_{real}})e(k)\right\| + \left\|\frac{T_s}{L_{real}}\gamma(k)\right\| \end{aligned} \tag{68}$$

With the assumption that sampling time is very small, the reference value can be regarded as no change in two cycles.

According to (68),it can be concluded that, if $L_{real} > \frac{1}{2}L$,

$$0 < |1 - \frac{L}{L_{real}}| < 1 \tag{69}$$

Hence, the current errors can converge to the compact set

$$\Lambda = \{e \mid \|e\| \le \frac{T_s}{L_{real}} \zeta\} \tag{70}$$

3.7. Experiment results

Several experiments have been conducted to evaluate the performance and effectiveness of the proposed seamless transfer control strategy for the dual-mode inverters. The experimental hardware setup is illustrated in Figure 60. The experimental setup elements includes a 1.2 kW single phase H-bridge inverter with LC filter, a 400 V dc-link voltage, and a 120 V ac grid voltage. The filter inductor value is 5mH and the filter capacitor value is 10 μF. An isolation transformer is used for galvanic isolation between the dual-mode inverter and the grid. An autotransformer is used to adjust the grid voltage for the experimental setup. The proposed seamless transfer control algorithm is implemented using dSPACE 1007 platform. The sampling time is chosen as 25 μs and the dead-time is chosen to be 1 μs.

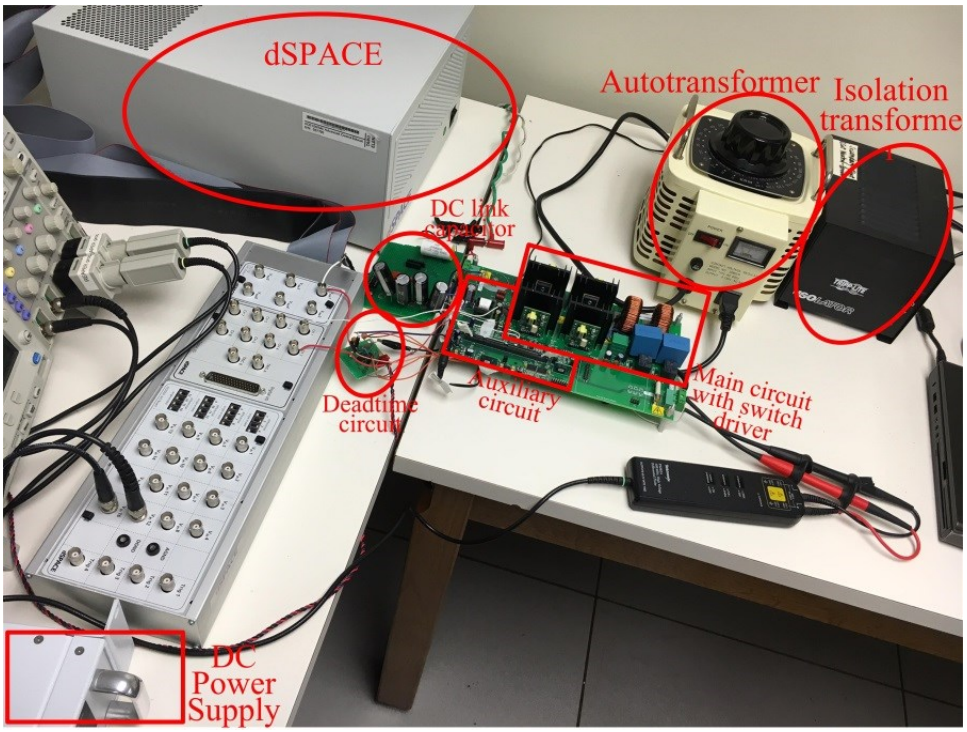


Figure 60: The experimental setup.

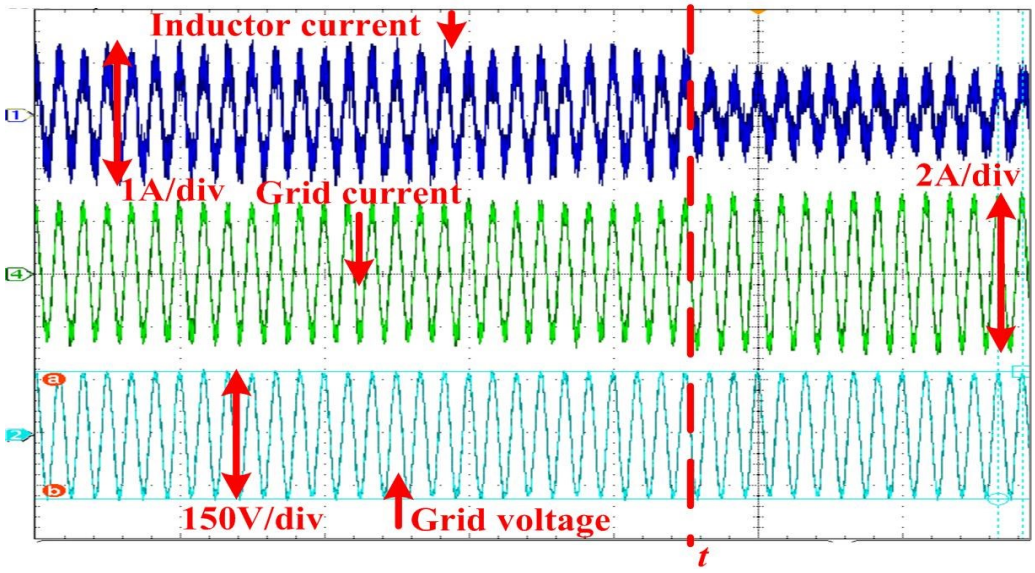


Figure 61: Experimental waveforms of active power step change in grid-connected mode.

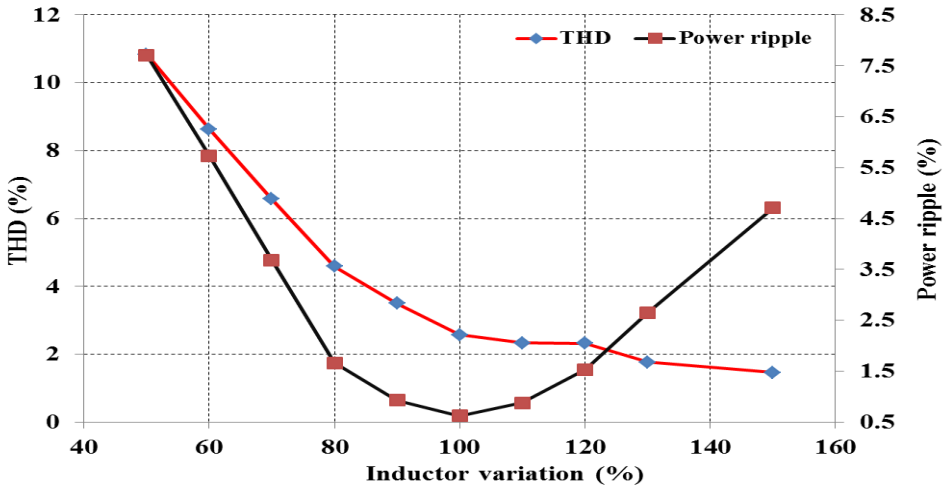


Figure 62: Error effect of inductance value on the THD and power ripple.

Figure 61 shows the experimental results of grid-connected mode with active power step changes assuming unity power factor (reactive power reference is zero). The experimental results with 120 V grid voltage are shown in Figure 61. In this case study, both the dual-mode inverter and the grid provide active power to the local load. At the time *t*, the active power reference is increased by 50% of its initial value. Thus the grid provides more power to the local load and the inductor current decreases. As it is shown, the grid and inductor currents are adjusted shortly after time *t* due to change in active power reference. Figure 62 shows the inductance parameter variation effect on system performance. Two criteria are considered to evaluate the system performance under inductor variation: THD and power tracking error. The 100% inductance means there is no error or variation in this parameter. Higher inductance value will result in smoother grid current. The results in Figure 62 demonstrate that even with large variation in the

inductor value such as ±50%, the controller has promising performance which shows the robustness of the proposed controller to uncertainties in the model of the system.

Figure 63 shows the experimental results of islanded mode with load step change. A resistive load is considered for the dual-mode inverter. The load is varied from 80 Ω to 160 Ω at time t when the transient process begins. As it is shown in Figure 63, the load voltage regulated without any interruption over step change in the load value. Figure 64 shows the experimental results of islanded mode with nonlinear load. The proposed control algorithm has a harmonic distortion rejection and voltage regulation capabilities under nonlinear load condition. As it is shown in Figure 64, the load voltage is regulated without significant distortion.

The experimental verification on seamless transfer from islanded to grid-connected mode is shown in Figure 65. where the dual-mode inverter operates in islanded mode initially. Then at time t_1, the grid is ready to reconnect and the phase adjustment algorithm is triggered. After the phase adjustment process, the load voltage is synchronized with grid voltage. It is observed that there is no overshoot or undershoot at either the PCC voltage or the inductor current during the seamless transfer as expected. Figure 66 shows the experimental verification in the case where there is 21 degree phase difference between load voltage and grid voltage before the grid is reconnected to the inverter system. Similarly, at the instant of t_1, the grid is ready to be reconnected to the rest of the system. Due to the phase difference between the load voltage and the grid, the inverter keeps working in islanded mode while the phase adjustment algorithm is adjusting the inverter output voltage phase to be synced with grid voltage. Thus, the

transition mode in this case study is longer due to execution of phase adjustment algorithm. At the instant of t_2, the phase difference between the grid voltage and the load voltage is adjusted to be within the preset acceptable value, thus the system is reconnected to the grid at this instant. As it is pictured, there is no significant deviation in PCC voltage or grid current, thus achieving a seamless transfer from islanded to grid-connected mode.

The experimental verification on seamless transition from grid-connected to islanded mode is shown in Figure 67 and Figure 68 where initially the dual-mode inverter operates in grid-connected mode with 120 V grid voltage and both dual-mode inverter and grid provide power to the local load. At time t_1, it is disconnected from the grid and the grid current goes to zero instantly. After islanding detection and transition mode, the dual-mode inverter starts operating in islanded mode at t_2. Figure 67 and 68 show two case studies where the grid disconnection occurred at two different instance over a cycle of the grid voltage waveform. As it is pictured, regulating the PCC voltage over this transition mode, the seamless transition is achieved during t_1 to t_2 without significant overshoot or interruption at either the PCC voltage or the inductor current.

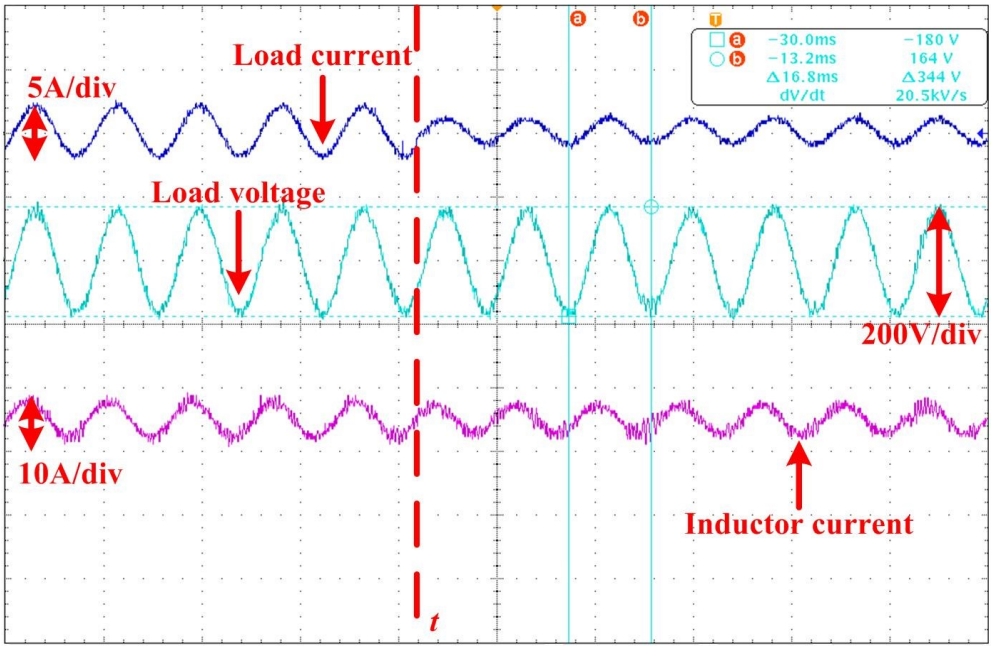


Figure 63: Experimental results in island mode with load step change.

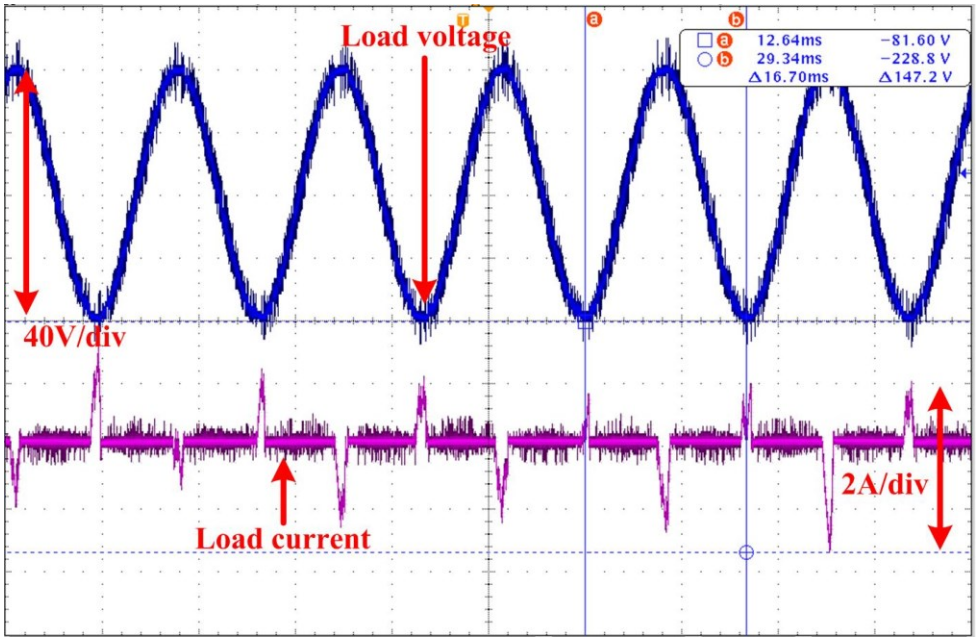


Figure 64: Experimental waveforms of dual-mode inverter in island mode with non-linear loads.

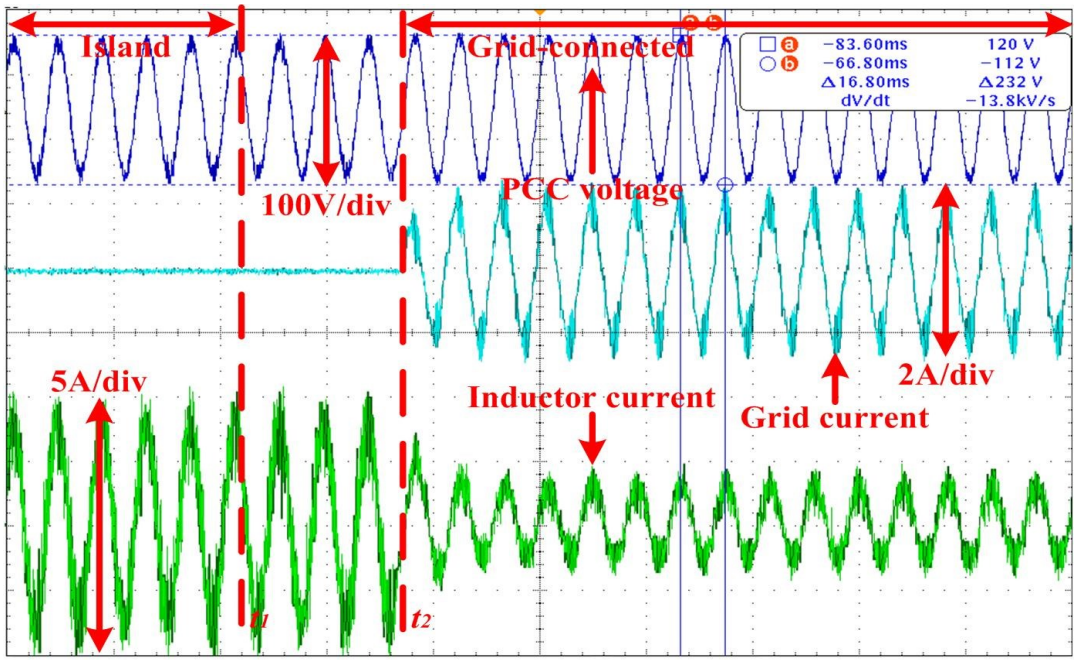


Figure 65: Experimental waveforms of seamless transfer from island to grid-connected mode. (Case 1).

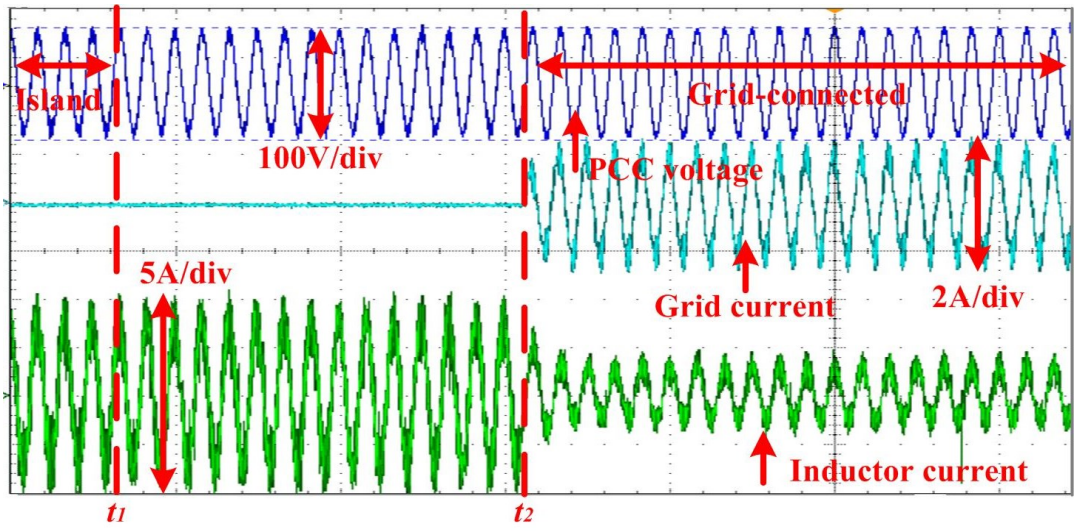


Figure 66: Experimental waveforms of seamless transfer from island to grid-connected mode. (Case 2)

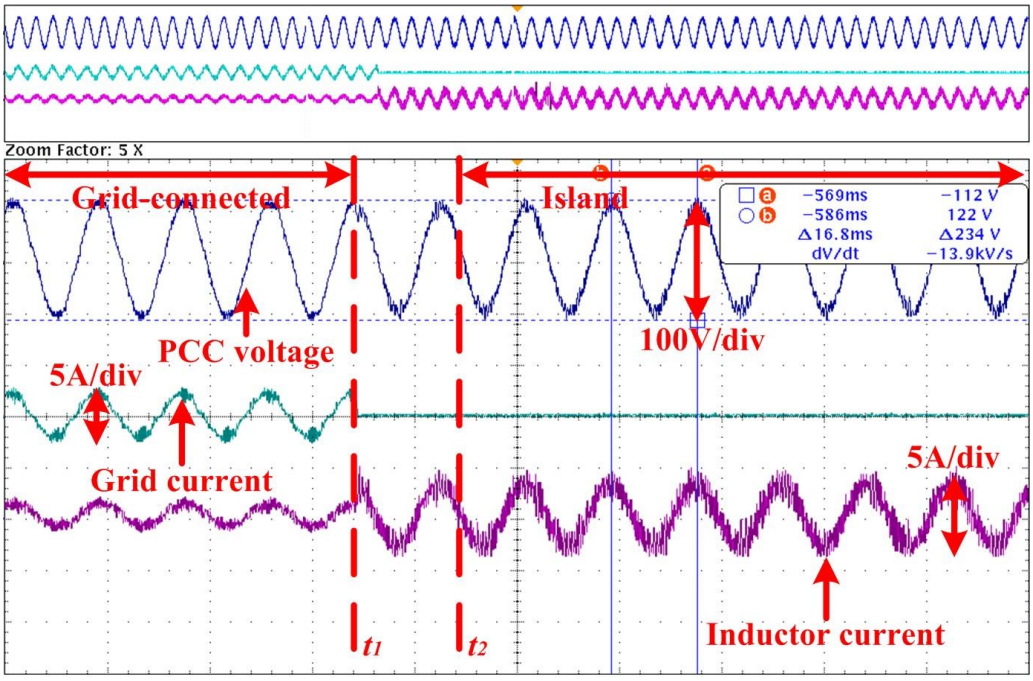


Figure 67: Experimental waveforms of seamless transfer from grid-connected mode to islanding mode (Case 1).

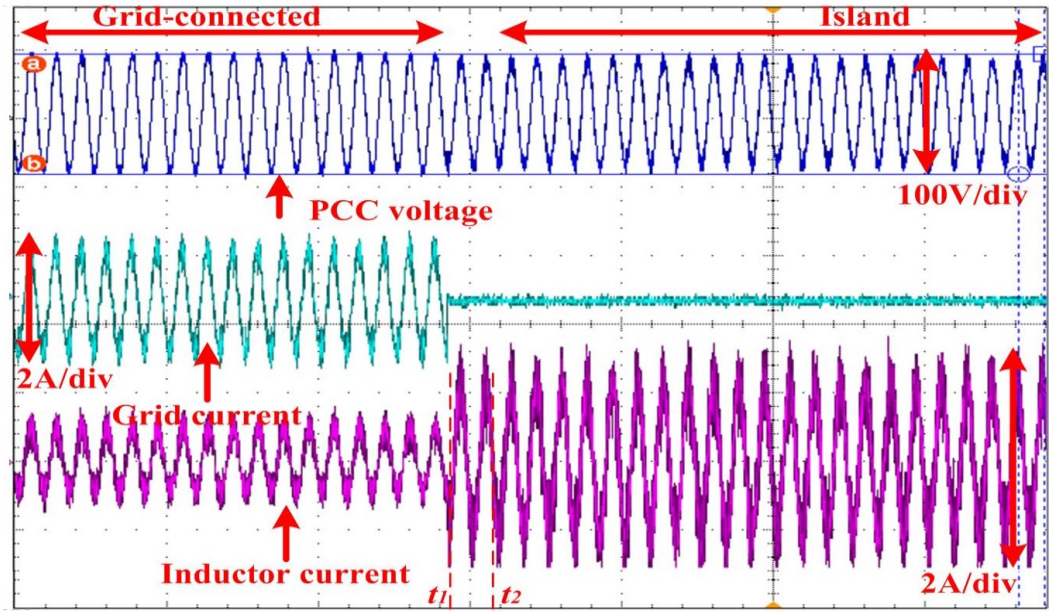


Figure 68: Experimental waveforms of seamless transfer from grid-connected mode to islanding mode (Case 2).

3.8 Conclusion

In this section, a novel controller using model predictive control framework is proposed for dual-mode inverters in DG systems with seamless transition between modes of operation. In the grid-connected mode, the system is controlled to regulate the active and reactive power at the PCC. This renders the capability of bidirectional decoupled power capability, which suits for supporting ancillary service such as volt/var control. By using the SOGI module, the proposed controller can maintain robust synchronization under grid disturbances.

Active and reactive power prediction model is derived based on instantaneous power theory in stationary reference frame. A synchronization and phase adjustment algorithm to detect the phase angle of the grid voltage and generate the load voltage references during the transition modes is proposed. The proposed method ensures seamless transition between steady state modes of operation.

A new auto-tuning strategy is proposed for the MPC cost function weight factors. The stability of the proposed controller is evaluated in discrete z-domain for abnormalities in the system such as model parameter errors in model of the system. The effectiveness of the proposed seamless transfer control strategy is verified by both simulation and experimental results. In comparison to conventional methods using multi-loop classical controllers, the proposed control strategy has simpler structure to implement with less tuning efforts.

4. INVESTIGATION AND COMPARISON OF DOUBLE LINE FREQUENCY RIPPLE POWER DECOUPLING FOR SINGLE PHASE SYSTEMS

4.1 Introduction

With the broader applications in residential, commercial and industrial power conditioning systems such as high brightness light-emitting diode (LED) drivers [83, 84], grid-connected inverters from renewable energy [85-87], uninterruptible power supplies (UPS), etc., the inherent double line frequency ripple power in single phase rectifiers and inverters has been paid more and more attentions [88]. Right now, due to the low cost and large capacitance, bulky electrolytic capacitors with short lifetime are still widely used in dc bus of single-phase rectifiers and inverters, which is hard to achieve high efficiency, high power density and high reliability [89, 90]. Therefore, a lot of researches are recently focused on active power decoupling techniques to overcome the disadvantages mentioned above [91-95]. In [66], since the dc bus voltage of two stage PV microinverters was high, film capacitors with low capacitance can be used to buffer the double line frequency ripple power without additional power decoupling circuit. The degradation of maximum power point tracking (MPPT) efficiency and the distortion of grid current, resulting from high dc bus voltage ripple, can be compensated through advanced control strategies by damping double line frequency ripple. Another type of active power decoupling techniques can be classified as parallel and series active power decoupling in terms of the ripple power paths. The series active power decoupling for voltage source and current source topologies were proposed in [96] and [97],

respectively. By connecting an independently controlled voltage compensator in series with the dc and ripple sources, the ripple voltage can be compensated by power devices and capacitors with low voltage ratings, and the capacitance of dc bus capacitor can be reduced. In [98], the parallel active power decoupling with inductor as energy storage component was introduced. By applying hysteresis control towards the dc bus voltage ripple, the compensating current of active filter was in opposite phase with the ripple current of main circuit. The large energy storage inductor and symmetric voltage blocking capability of power devices in active filter were required. Some parallel active power decoupling with capacitor as energy storage component were introduced in [99-101]. Even though no extra power devices were needed, the coupling between the main circuit and power decoupling circuit reduced the dc voltage utilization. In [102-107], the parallel active power decoupling with one or two phase legs added, were presented. Both capacitor and inductor can be used as the energy storage component, and the additional power devices can be modulated independently or dependently to buffer the double line frequency ripple power. Some other active power decoupling techniques like six-switch power decoupling [108, 109], ac-link power decoupling [110], decoupling using the center tap of isolated transformer [111], and power decoupling using active buffer [112], etc., were included in the literatures for different applications. Furthermore, by replacing the current-bidirectional two-quadrant switches with the voltage-bidirectional two-quadrant ones, similar power decoupling techniques can be applied in current source inverters [97, 113, 114].

Generally, as shown in Figure 69, the power decoupling techniques can be divided into parallel and series power decoupling based on ripple power paths. At the same time, according to the energy storage components, both series and parallel power decoupling techniques can be divided into inductive and capacitive power decoupling. To completely decouple the double line frequency ripple power and minimize introduced other frequency ripple powers, the general solution of voltage across energy storage capacitor (or current through energy storage inductor) can be derived first. By taking the locations of active power decoupling circuits, ripple power paths and the waveforms of the energy storage components into consideration, the general topological and electrical properties are analyzed, and all existing power decoupling topologies are derived. The relationships between energy utilization and voltage/current ripple of energy storage capacitor are evaluated in details and the characteristics of different power decoupling topologies are compared, to provide guidance on the selections of capacitor/inductor and topology for different applications. As mentioned in Figure 69, in principle, both capacitor and inductor, even LC resonant branch, can be used to decouple the double line frequency ripple power. However, the large inductance, heavy weight, low power density and high power losses of inductor limit its applications. While inductor is used as energy storage component, the similar results can be obtained as well.

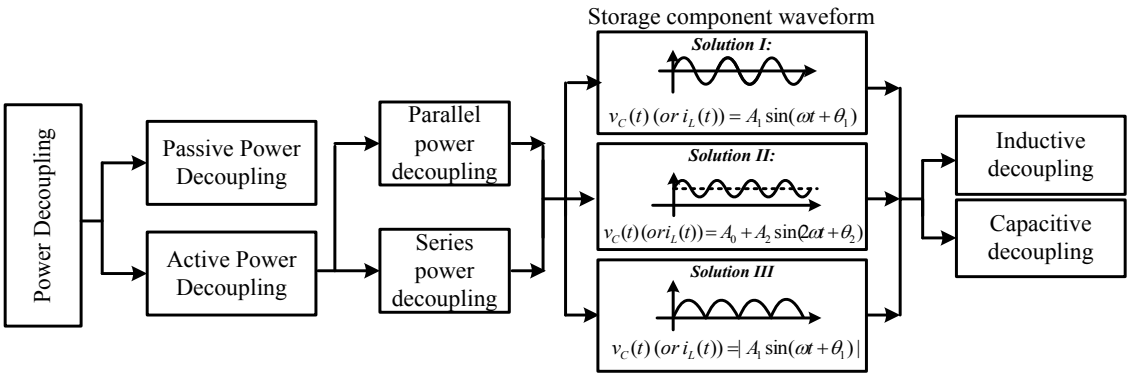


Figure 69: The classifications of power decoupling techniques.

Among numerous power decoupling techniques, it is necessary to clarify the respective pros and cons to satisfy different applications. For example, Hu, etc. [85], reviewed power decoupling techniques for micro-inverters in PV systems; Sun, etc. [115], provided review of active power decoupling topologies. However, all of them were focused on the topologies of power decoupling techniques. Even though they also compared the characteristics of various power decoupling techniques in terms of power ratings, component counts, the capacitance of power decoupling capacitor and even efficiency, there were no comprehensive comparison on the allowed minimum capacitance for power decoupling, the dc voltage utilization, the current stress, the modulation complexity and even application evaluations. Actually, all these aspects are critical while choosing appropriate power decoupling techniques for different applications. Therefore, this paper investigates and compares the minimum capacitances of energy storage capacitors, the current stress of power devices in the main circuit and the dc voltage utilization of both the main circuit and power decoupling circuit for

different power decoupling techniques. At the same time, the component counts, modulation complexity and other main features towards different applications are also summarized to weigh overall characteristics.

This section is organized as follows: firstly, the general solutions that unify all possible waveforms across energy storage capacitor based on power decoupling principle was derived. Based on that, the required capacitances to decouple the ripple power are derived. To effectively compare the minimum capacitance to achieve power decoupling among different power decoupling techniques, the dc voltage utilization of both the main circuit and power decoupling circuit are discussed. Then, the detailed investigations on the current stress of power devices in the main circuit were included. This section also combines with the component counts, modulation complexity, etc., summarizes the main features of different power decoupling techniques. A design example is given to verify the validity and feasibility of the minimum energy storage capacitance for power decoupling techniques.

4.2 General solutions of power decoupling techniques

A typical single phase voltage source H-bridge rectifier or inverter is shown in Figure 70. Generally, there is a large electrolytic capacitor at dc side to eliminate the double line frequency component.

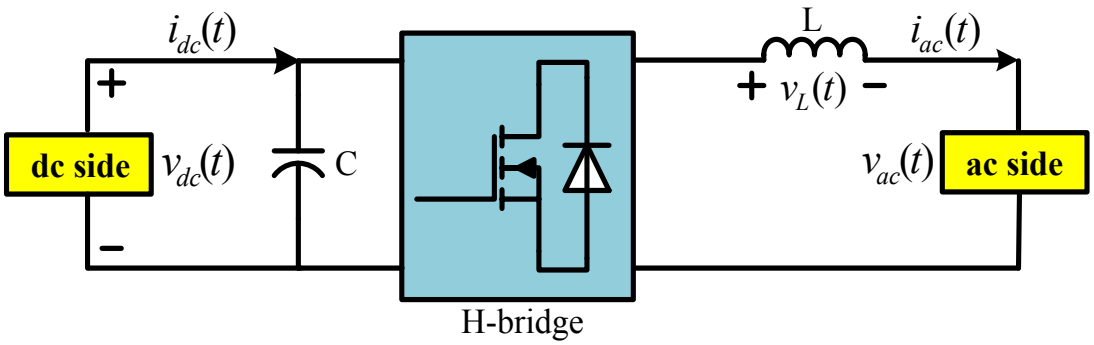


Figure 70: Typical single phase H-bridge rectifier or inverter.

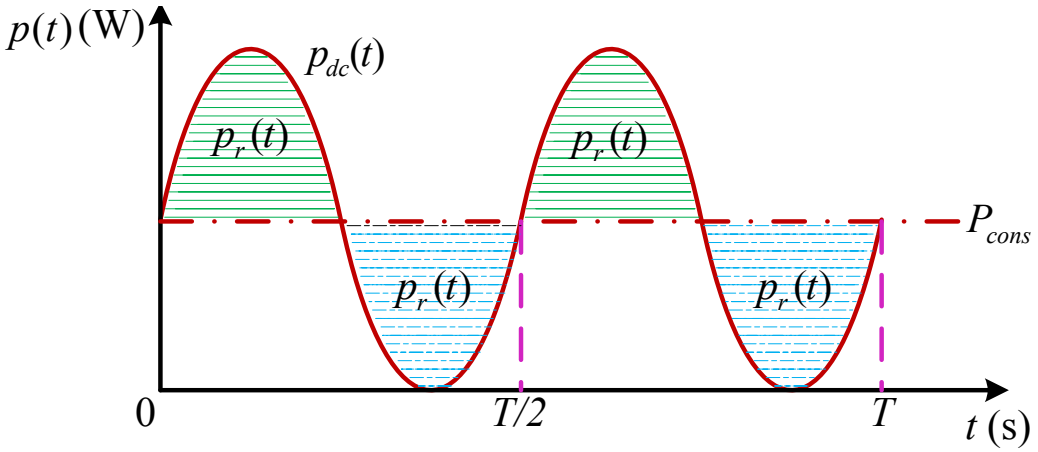


Figure 71: Instantaneous power between dc and ac sides in single phase rectifiers and inverters.

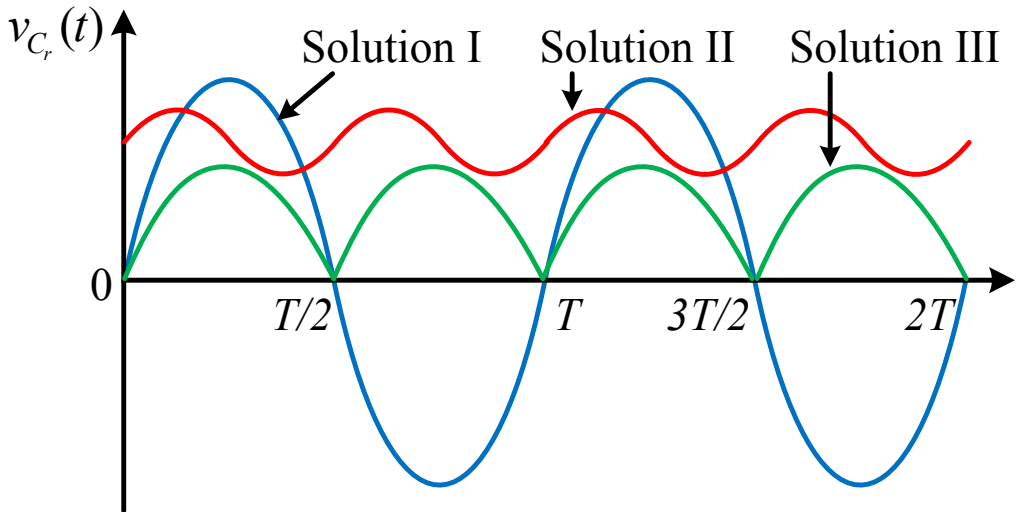


Figure 72: Three solutions on the voltage across energy storage capacitor.

It is assumed that the ac side voltage and current have the following equations:

$$v_{ac}(t) = V_{ac} \sin \omega t \tag{71}$$

$$i_{ac}(t) = I_{ac} \sin(\omega t + \varphi) \tag{72}$$

where V_{ac} and I_{ac} are the peak values of voltage and current at ac side respectively. ω is the angular frequency. φ is the phase difference between voltage and current at ac side. The instantaneous power at dc side without considering the power losses can be obtained as follows.

$$\begin{aligned} p_{dc}(t) &= p_{ac}(t) + p_L(t) = v_{ac}(t) i_{ac}(t) + v_L(t) i_{ac}(t) \\ &= \frac{V_{ac} I_{ac}}{2} \cos\varphi - \frac{V_{ac} I_{ac}}{2} \cos(2\omega t + \varphi) + \frac{1}{2} L \omega I_{ac}^{\ 2} \sin(2\omega t + 2\varphi) = P_{cons} + p_r(t) \end{aligned} \tag{73}$$

where L is the inductance of filter at ac side. From (73), it is observed that the instantaneous power at dc side consists of two terms: a constant power P_{cons} and a double line frequency ripple power $p_r(t)$ that is composed of ripple power from both ac side and

filter inductor. It is noted that the single phase system in Figure 70 operates in inverter mode when P_{cons} is positive, as shown in Figure 71; otherwise, the single phase system in Figure 70 operates in rectifier mode. For the inverter mode, P_{cons} flows from dc side to feed ac load. For the rectifier mode, P_{cons} flows from ac side to feed dc load. Regardless of the inverter or rectifier mode, the constant power P_{cons} feeds the dc power and the ripple power must be decoupled by energy storage components. For most single phase systems, since the ripple power $p_L(t)$ from filter inductor is normally less than 1/10 of that from ac side, it can be neglected to simplify the analysis.

Assuming $v_{Cr}(t)$ and $i_{Cr}(t)$ are the voltage and current of energy storage capacitor, respectively, the following equation should be satisfied to achieve power decoupling.

$$p_{C_r}(t) = v_{C_r}(t) \cdot i_{C_r}(t) = \frac{1}{2} C_r \frac{d(v_{C_r}(t)^2)}{dt} = p_r(t) \tag{74}$$

By solving this differential equation, it is obtained that

$$v_{C_r}(t)^2 = A + \frac{V_{ac} I_{ac}}{2\omega C_r} \sin(2\omega t + \varphi) \tag{75}$$

where A is a time-constant value. Due to $v_{Cr}(t)^2 \geq 0$, $A \geq V_{ac}I_{ac}/(2\omega C_r)$. When $A=V_{ac}I_{ac}/(2\omega C_r)$, the voltage across energy storage capacitor is supposed to be:

$$v_{C_r}(t) = A_1 \sin(\omega t + \theta_1) \text{ or } v_{C_r}(t) = \left| A_1 \sin(\omega t + \theta_1) \right| \tag{76}$$

When $A>V_{ac}I_{ac}/(2\omega C_r)$, it is found that the complete solution on the voltage across energy storage capacitor contains many harmonic components and can be expressed to be:

$$v_{C_r}(t) = A_0 + \sum_{k=2}^{n} A_k \sin(k\omega t + \theta_k) \tag{77}$$

where n=2, 3, etc. It is known that $v_{Cr}(t)$ contains rich harmonic components which will introduce other undesired ripple powers with different frequency components. To decouple the double line frequency ripple power completely and minimize the introduced ripple powers with other frequency components, the voltage across energy storage capacitor is supposed to be:

$$v_{C_r}(t) = A_0 + A_2 \sin(2\omega t + \theta_2) \tag{78}$$

In summary, there could be three solutions as shown in Figure 72: I) $v_{C_r}(t) = A_1 \sin(\omega t + \theta_1)$; II) $v_{C_r}(t) = A_0 + A_2 \sin(2\omega t + \theta_2)$ and $A_0 >> A_2$, III) $v_{C_r}(t) = \left| A_1 \sin(\omega t + \theta_1) \right|$.

Thus the voltage across energy storage capacitors in all existing power decoupling techniques such as passive/active power decoupling, series/parallel power decoupling or independent/dependent modulation, will either satisfy one of the general solutions or can be regarded as the equivalent one in the general solutions. For the solution I, the voltage across energy storage capacitor is line frequency sinusoidal waveform without dc offset. Combined with (73), (74) and (76), the capacitance to buffer the double line frequency ripple power can be expressed as:

$$C_r = \frac{V_{ac} I_{ac}}{\omega A_1^{\,2}} \tag{79}$$

Likewise, for the solution II, the voltage across energy storage capacitor is sinusoidal waveform with dc offset and double line frequency. The capacitance to buffer the double line frequency ripple power can be obtained by:

$$C_r = \frac{V_{ac} I_{ac}}{2\omega A_0 A_2} \tag{80}$$

For the solution III, since the voltage across energy storage capacitor behaves like full-wave rectified line frequency sinusoidal waveform, the capacitance to buffer the double line frequency ripple power is the same with that in the solution I.

Through the analysis above, it is revealed that for the same power rating in the ac side, the required capacitance to achieve power decoupling will decrease with the increase of voltage rating across energy storage capacitor. However there is always maximum available voltage in a specific power decoupling topology, which inevitably decides the allowed minimum capacitance. Next, the dc voltage utilization is discussed by combining different ripple power paths.

4.3 DC voltage utilization

Given different ripple power paths, the existing power decoupling techniques can be divided into series and parallel power decoupling.

For the former as shown in Figure 73 and 74 [96, 116], an extra controllable voltage source across C_r is in series with the ripple source $v_2(t)$ and desired dc source $v_1(t)$ to compensate the instantaneous voltage ripple. Since the voltage across C_r is the difference between $v_1(t)$ and $v_2(t)$, which usually is small, the components with low voltage stress can be used in the power decoupling circuit. But the required capacitance of C_b is large in order to get low voltage ripple. By adding additional phase leg and inductor, as shown in Figure 74, the allowed capacitance of C_b can be reduced compared

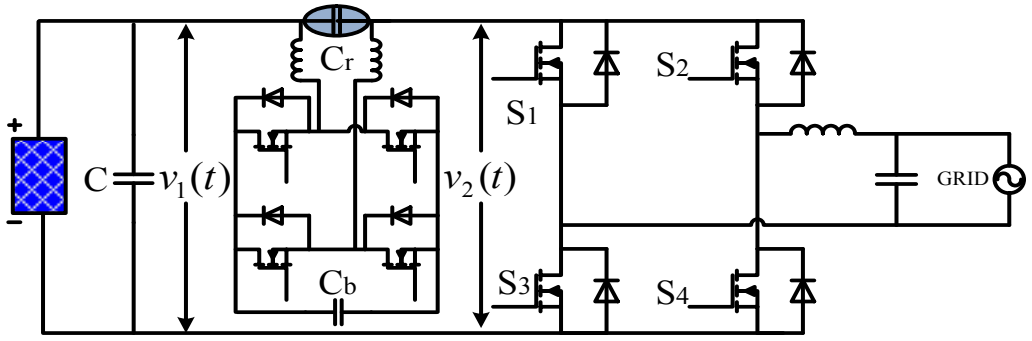


Figure 73: Series power decoupling circuit with two phase legs [96].

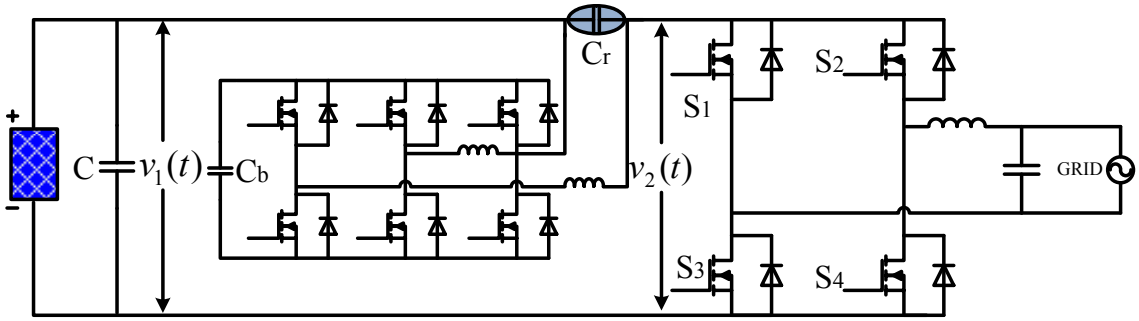


Figure 74: Series power decoupling circuit with three phase legs [116].

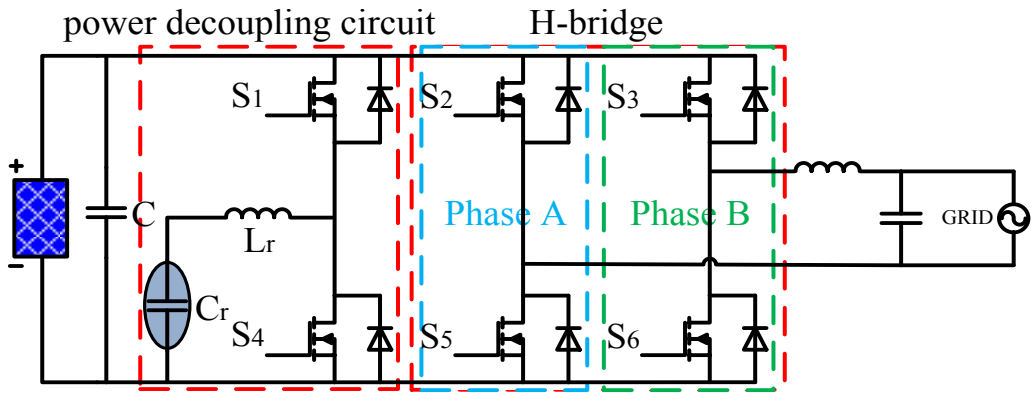


Figure 75: Buck-type parallel power decoupling circuit [117].

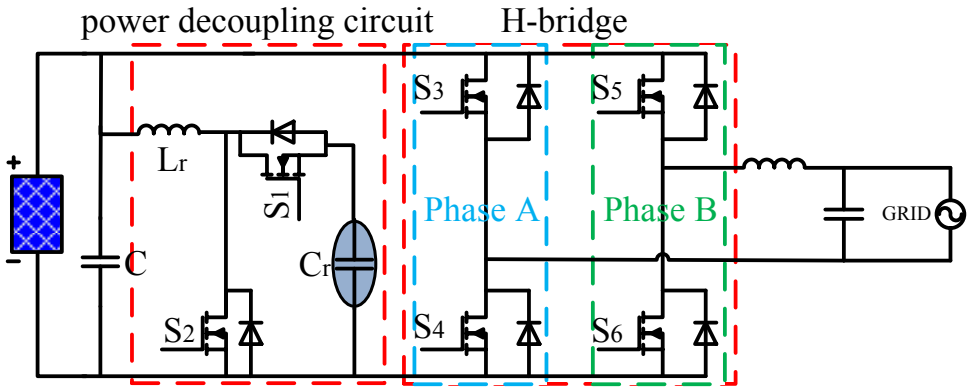


Figure 76: Boost-type parallel power decoupling circuit [104].

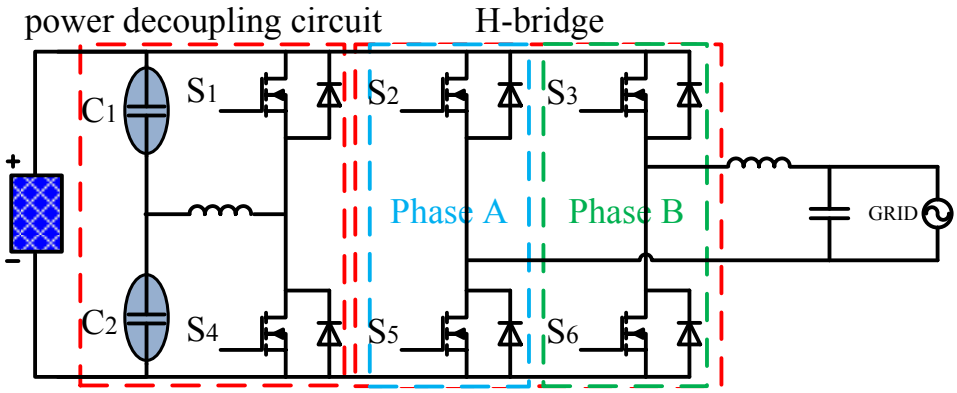


Figure 77: Half-bridge parallel power decoupling circuit [118].

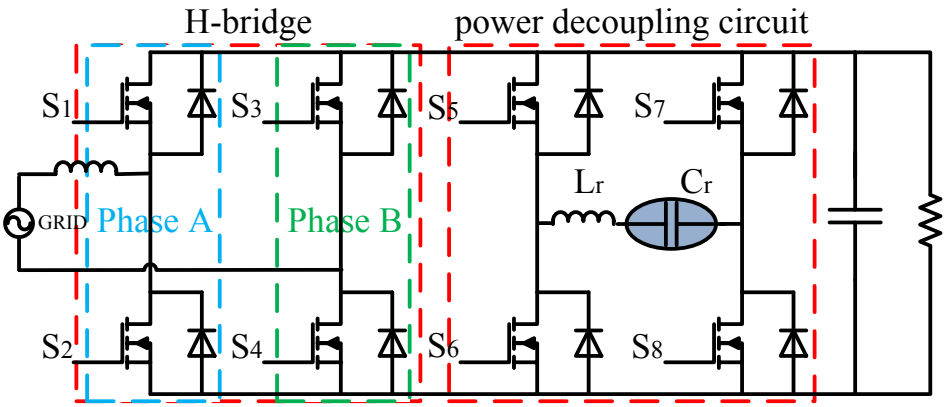


Figure 78: Full-bridge parallel power decoupling circuit [119].

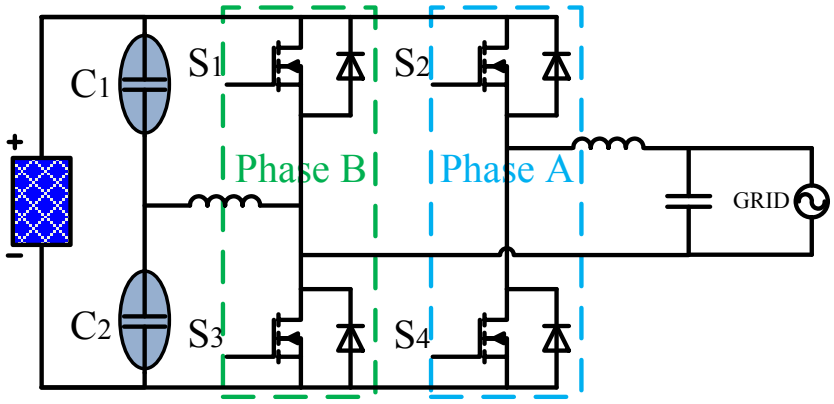


Figure 79: Dependent and two phase legs [99].

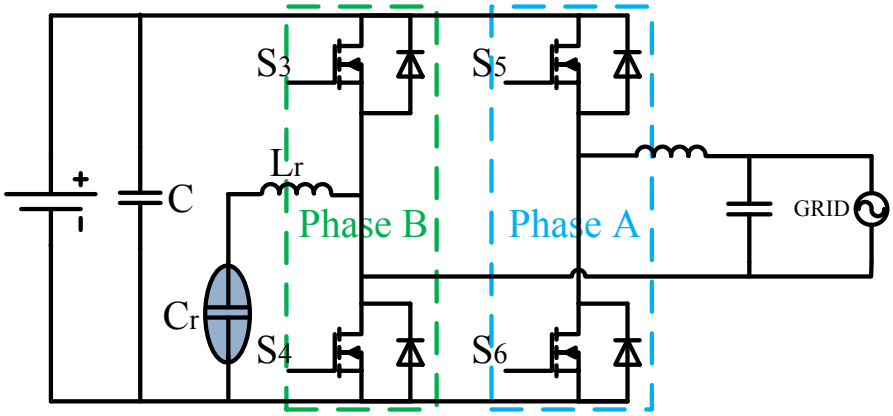


Figure 80: Dependent and two phase legs [101].

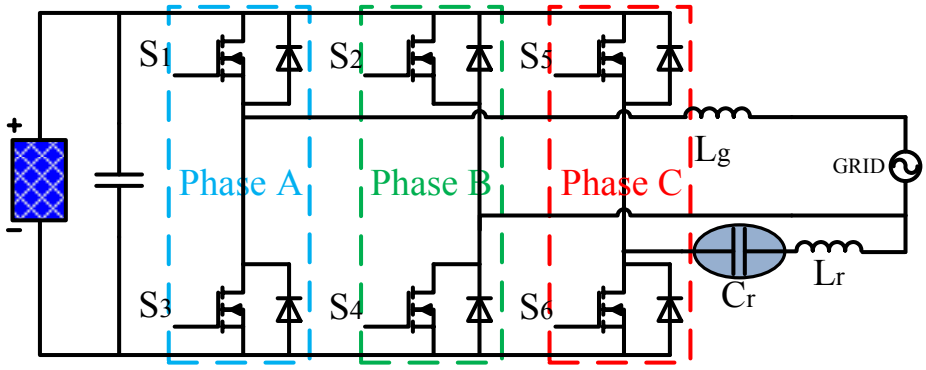


Figure 81: Dependent and three phase legs [103].

with that in Figure 73. For the parallel power decoupling, two, three or even four phase legs are used to achieve the function of both the main circuit and power decoupling circuit. At the same time, the modulation of power decoupling circuit can be either independent or dependent on that of the main circuit. In the following, the dc voltage utilization and allowed minimum capacitance for power decoupling will be investigated on the basis of existing typical power decoupling techniques.

4.3.1 Independent modulation strategy

Independent modulation strategy is always applied in power decoupling topologies with three or four phase legs as shown in Figure 75~78. To maximize the dc voltage utilization of the main circuit, it is desired to use two phase legs, for example, phase A and B, to modulate the main circuit like full-bridge structure. Thus the modulation signals m_A and m_B of phases A and B can be expressed as $M\sin\omega t$ and $-M\sin\omega t$, respectively, and the dc voltage utilization of the main circuit is 1. Then it is known that the remaining one or two phase legs can be constructed as buck-type, boost-type, half-bridge or full-bridge to achieve power decoupling function.

4.3.1.1 With three phase legs

For buck-type power decoupling circuit in Figure 75 [117], while it is modulated to be the solution II, there is $A_0+A_2 \le V_{dc}$. If defining η_r as the ratio of ac voltage ripple to the peak voltage across energy storage capacitor, the relationship of η_r, A_0 and A_2 can be expressed as:

$$\eta_r = \frac{2A_2}{A_2 + A_0} \le 1 \tag{81}$$

$$A_0 A_2 = \frac{(2-\eta_r)V_{dc}}{2}\frac{\eta_r V_{dc}}{2} \tag{82}$$

where, it is revealed that while η_r equals to 1, A_0A_2 has the maximum value of $V_{dc}^2/4$ and $A_0=A_2$. Thus from (80), it is known that the energy storage capacitance has minimum value. However, it is noticed that $A_0=A_2$ conflicts with $A_0>>A_2$ in the solution II, which means lots of undesired ripple powers will be introduced. To minimize those undesired ripple powers, the allowed minimum capacitance has to be increased. When it is modulated as the solution III, the minimum capacitance satisfies:

$$C_r = \frac{V_{ac}I_{ac}}{\omega V_{dc}^{\ 2}} \tag{83}$$

For boost-type power decoupling circuit as shown in Figure 76 [104], since $A_0+A_2 \geq V_{dc}$, it is totally possible to allow smaller energy storage capacitance than that in buck-type power decoupling circuit. But higher voltage also means higher voltage stress for the components of power decoupling circuit. At the same time, the dc resistance (DCR) of boost inductor limits the available maximum voltage across energy storage capacitor. Thus the available maximum voltage decides the minimum capacitance.

The power decoupling circuit can be also configured as half-bridge structure in Figure 77 [118] where the voltage across energy storage capacitor satisfies the solution I. Therefore, the dc voltage utilization of the power decoupling circuit is 0.5 and the minimum capacitor for power decoupling can be given by:

$$C_r = \frac{4V_{ac}I_{ac}}{\omega V_{dc}^{\ 2}} \tag{84}$$

Compared with (83), it is observed that for the same power rating and V_{dc}, the power decoupling techniques in Figure 77 has larger capacitance than that in Figure 75 with the solution III. However, the power decoupling techniques in Figure 77 will decouple the double line frequency ripple power completely without introducing other ripple powers. Furthermore, since the energy storage capacitor is divided into two equivalent capacitors in parallel and is used as dc link capacitors as illustrated in Figure 77, the minimum capacitance of each will be half of that in (84).

4.3.1.2 With four phase legs

With two full-bridge structures as shown in Figure 78 [105, 119], both the main circuit and power decoupling circuit can achieve unity dc voltage utilization. The capacitance can be minimized as (83) to buffer double line frequency ripple power completely at the cost of more power devices and driving circuits.

4.3.2 Dependent modulation strategy

Dependent modulation strategy can be applied in power decoupling topologies with two or three phase legs, in which at least one phase leg will be shared by both the main circuit and power decoupling circuit as shown in Figure 79~81 [99, 101-103].

4.3.2.1 With two phase legs

When the power decoupling topology includes two phase legs and the voltage across energy storage capacitor satisfies the solution I as shown in Figure 79, the modulation signal m_B of the shared phase leg can be expressed as:

$$m_B = \frac{2A_1}{V_{dc}} \sin(\omega t + \theta_1) \tag{85}$$

Thus the modulation signal of phase A can be obtained by:

$$m_A = \frac{2V_{ac}}{V_{dc}}\sin\omega t + \frac{2A_1}{V_{dc}}\sin(\omega t + \theta_1) \tag{86}$$

where $\theta_1 = \frac{\varphi}{2} + \frac{\pi}{4}$ or $\theta_1 = \frac{\varphi}{2} - \frac{3\pi}{4}$. Fig. 82(a) shows the vector diagram of modulation signals. It is observed that since the modulation index of phase A, B and the main circuit should be less than one to avoid over modulation, the maximum modulation index of both phase A and B can be 1 to maximize the dc voltage utilization of the main circuit. Thus the dc voltage utilization of power decoupling circuit in this case will be 0.5. At the same time, the minimum capacitance for power decoupling satisfies (84), which is the same with that in Figure 77.

When the voltage across energy storage capacitor satisfies the solution II as shown in Figure 80, it has a wide range from 0 to V_{dc}, which means that $A_0+A_2 \leq V_{dc}$. Similar to the analysis of Figure 75 with the solution II, when η_r equals to 1, A_0A_2 has the maximum value of $V_{dc}^2/4$ and $A_0=A_2$. Thus the minimum capacitance can be given by:

$$C_r = \frac{2V_{ac}I_{ac}}{\omega V_{dc}^{\ 2}} \tag{87}$$

Likewise, since $A_0=A_2$ conflicts with $A_0>>A_2$ in the solution II, larger capacitance are needed to minimize the introduced ripple powers with other frequency components. Furthermore, since the modulation signal of the shared phase leg B can be obtained from the solution II in (88), the modulation signal of phase A can be given by (89). From that, it is known that to avoid over modulation, the dc voltage utilization of the main circuit is always less than 0.5.

$$m_B = \frac{A_0}{V_{dc}} + \frac{A_2}{V_{dc}} \sin(2\omega t + \theta_2) \tag{88}$$

$$m_A = \frac{V_{ac}}{V_{dc}} \sin \omega t + \frac{A_0}{V_{dc}} + \frac{A_2}{V_{dc}} \sin(2\omega t + \theta_2) \tag{89}$$

When the voltage across energy storage capacitor satisfies the solution III, the minimum capacitance satisfies (83) and the dc voltage utilization of the main circuit is 0.5. Compared with other power decoupling techniques using dependent modulation with two phase legs, the dependent modulation with two phase legs and the solution III allows smaller capacitance.

4.3.2.2 With three phase legs

The power decoupling technique with three phase legs can be achieved through dependent modulation as shown in Figure 81, where the voltage across energy storage capacitor satisfies the solution I. To maximize the dc voltage utilization of the main circuit, the modulation signals m_A and m_B of phases A and B are defined as $M\sin\omega t$ and $-M\sin\omega t$. Then the modulation signal of phase C can be given by:

$$m_C = \frac{2A_1}{V_{dc}} \sin(\omega t + \theta_1) - \frac{V_{ac}}{V_{dc}} \sin \omega t \tag{90}$$

where $\theta_1 = \frac{\varphi}{2} + \frac{\pi}{4}$ or $\theta_1 = \frac{\varphi}{2} - \frac{3\pi}{4}$ and $M = \frac{V_{ac}}{V_{dc}}$. Since the modulation index of phase A, B and C should be less than one to avoid over modulation, the maximum voltage across energy storage capacitor is V_{dc} as illustrated in Figure 82(b). For unity power factor, due to the relationship between φ and θ_1, the maximum voltage across energy storage capacitor is $\sqrt{2}V_{dc}/2$. Thus the allowed minimum capacitance for unity power

factor satisfies (87), which is larger than power decoupling techniques with independent modulation, three phase legs and the solution III as shown in Figure 75.

According to the investigations above, the allowed minimum capacitance to decouple the double line frequency ripple power and the dc voltage utilization of the main circuit are summarized. Through that, it is concluded that for series power decoupling, even though the small voltage difference between $v_1(t)$ and $v_2(t)$ allows low voltage stress on power decoupling circuit, the large capacitance of C_b and the observed double line frequency ripple voltage in one side of the power decoupling circuit limit its applications. The parallel power decoupling techniques with two phase legs always have halved dc voltage utilization of the main circuit compared with those using three or four phase legs. The parallel power decoupling technique with four phase legs shows unity dc voltage utilization of the main circuit and smaller capacitance to decouple the ripple power completely by using more components. Therefore the parallel power decoupling techniques with three phase legs are always appropriate options for single phase rectifiers and inverters. Among them, the independent-modulated parallel power decoupling techniques with the solution III and the dependent-modulated parallel power decoupling techniques with the solution I are preferred. The former will inevitably introduces undesired ripple powers. But for unity power factor, the former allows smaller capacitance to decouple the double line frequency ripple power.

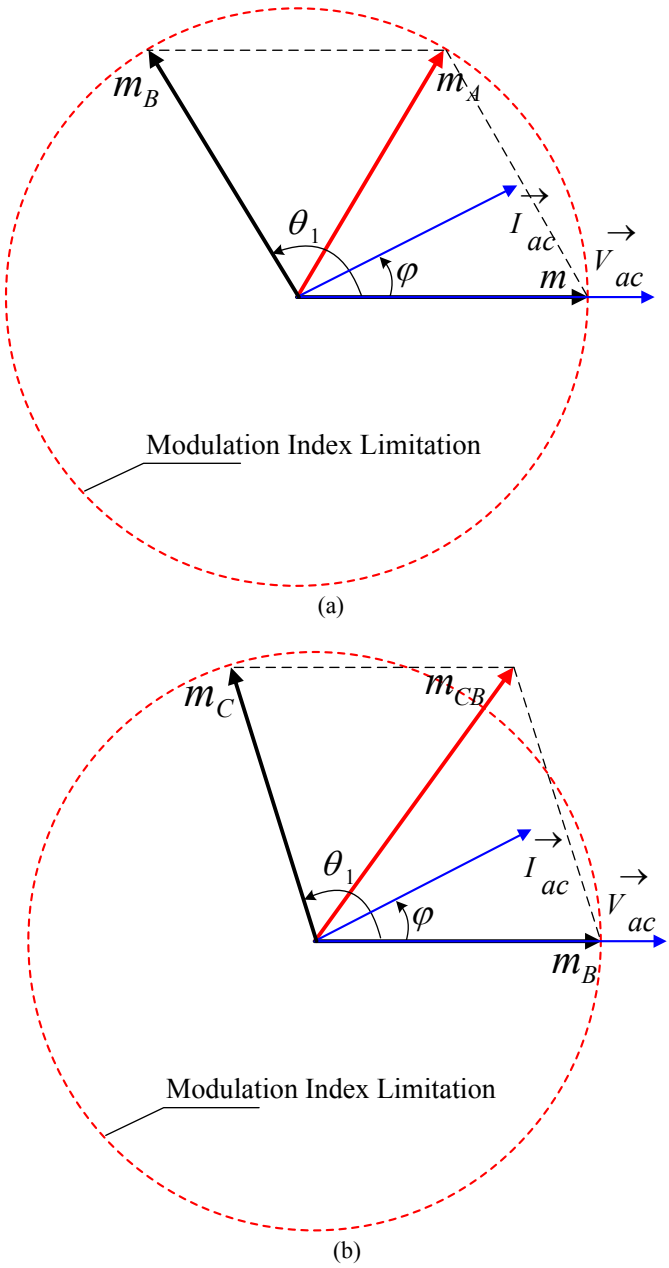
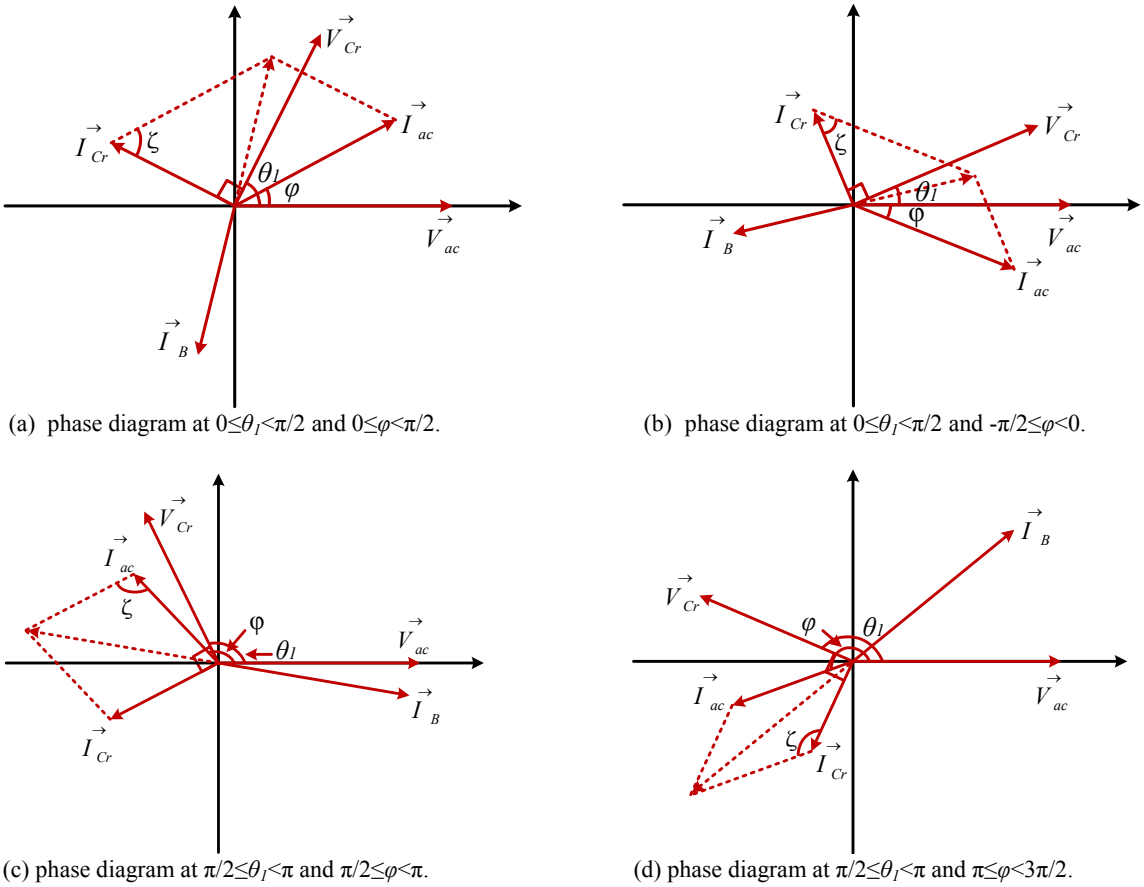


Figure 82: Vector diagram of modulation signals.
(a) Decoupling topology with two phase legs, the solution I and the dependent modulation.
(b) Decoupling topology with three phase legs, the solution I and the dependent modulation.

4.4 Current stress

For the independent modulation, the power decoupling circuits have no influence on the current stress of power devices in the main circuit. However, for the dependent modulation, due to the coupling between the main circuit and power decoupling circuit, at least one phase leg is shared by both of them. That will definitely change the current stress of power devices in the main circuit. Thus, it is necessary to investigate the current stress of the shared phase legs.



(a) phase diagram at $0 \le \theta_1 < \pi/2$ and $0 \le \varphi < \pi/2$.

(b) phase diagram at $0 \le \theta_1 < \pi/2$ and $-\pi/2 \le \varphi < 0$.

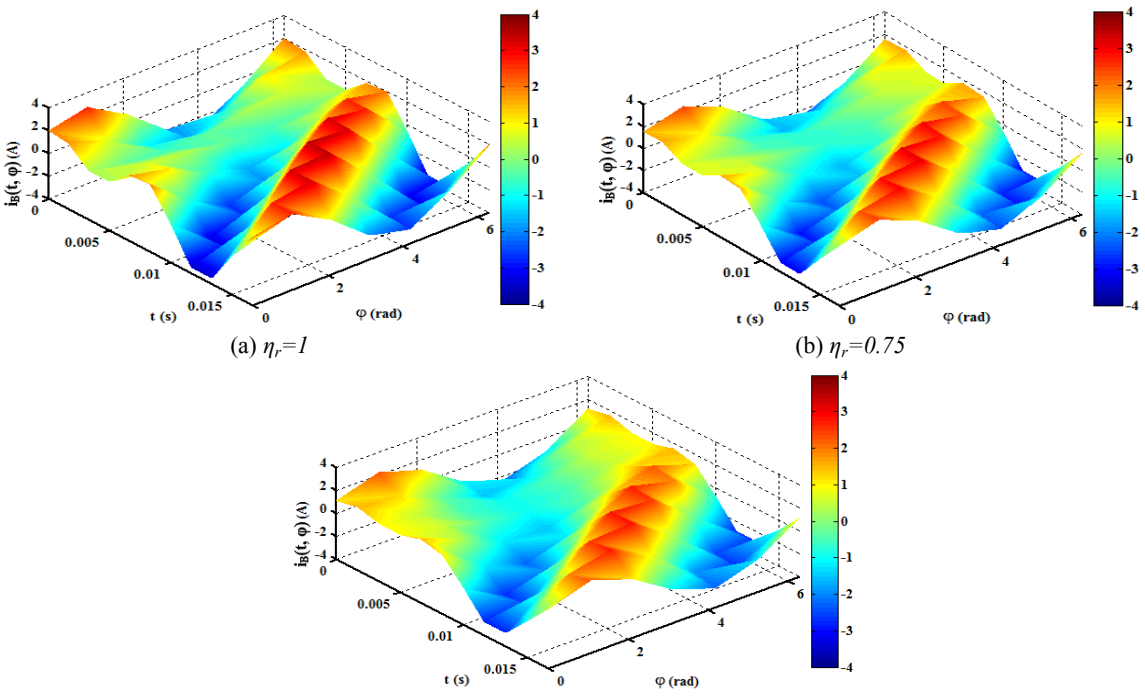
(c) phase diagram at $\pi/2 \le \theta_1 < \pi$ and $\pi/2 \le \varphi < \pi$.

(d) phase diagram at $\pi/2 \le \theta_1 < \pi$ and $\pi \le \varphi < 3\pi/2$.

Figure 83: Phase diagram illustrating the current stresses with the solution I.

Table 3: Summarization of the required minimum capacitance to decouple the double line frequency ripple power and the dc voltage utilization of the main circuit.

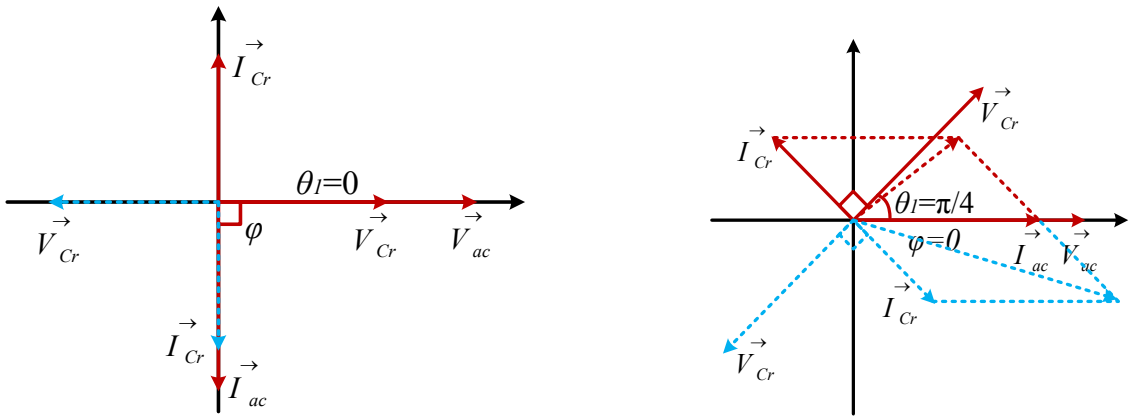
Power Decoupling Techniques			Minimum Capacitance to Buffer Ripple Power	Dc Voltage Utilization of the Main Circuit
Series Power Decoupling	Independent Modulation	Fig. 73 and 74	Large Capacitance of C_b	1
Parallel Power Decoupling	Independent Modulation with Three Phase Legs	Buck-type Power Decoupling Circuit and The Solution II, Fig. 75	$C_r = \frac{2V_{ac}I_{ac}}{\omega V_{dc}^2}$ larger capacitance to minimize the introduced other ripple power	1
		Buck-type Power Decoupling Circuit and The Solution III, Fig. 75	$C_r = \frac{V_{ac}I_{ac}}{\omega V_{dc}^2}$, the minimum capacitance is related to the maximum voltage gain	1
		Boost-type Power Decoupling Circuit and The Solution II, Fig. 76	$C_r < \frac{2V_{ac}I_{ac}}{\omega V_{dc}^2}$	1
		Half-bridge Power Decoupling Circuit and The Solution I, Fig. 77	$C_r = \frac{2V_{ac}I_{ac}}{\omega V_{dc}^2}$ for each	1
	Independent Modulation with Four Phase Legs	Full-bridge Power Decoupling Circuit and The Solution I, Fig. 78	$C_r = \frac{V_{ac}I_{ac}}{\omega V_{dc}^2}$	1
	Dependent Modulation with Two Phase Legs	The Solution I, Fig. 79	$C_r = \frac{2V_{ac}I_{ac}}{\omega V_{dc}^2}$ for each	0.5
		The Solution II, Fig. 80	$C_r = \frac{2V_{ac}I_{ac}}{\omega V_{dc}^2}$	Less than 0.5
	Dependent Modulation with Three Phase Legs	The Solution I, Fig. 81	$C_r = \frac{V_{ac}I_{ac}}{\omega V_{dc}^2}$ $C_r = \frac{2V_{ac}I_{ac}}{\omega V_{dc}^2}$ for unity power factor	1



(a) $\eta_r=1$ (b) $\eta_r=0.75$

(b) $\eta_r=0.5$

Figure 84: The 3D plot of current stresses through phase B in dependent modulation strategy with the solution II.



(a) phase diagram at $\theta_1=0$. (b) phase diagram at $\varphi=0$.

Figure 85: Phase diagram illustrating the current stresses with the solution III.

4.4.1 Three or two phase legs with the solution I

It is assumed that phase B is shared by both the main circuit and power decoupling circuit. For the dependent modulation with the solution I, there is $-\pi/2 \le \varphi < \pi/2$ and $\theta_1 - \varphi \ge 0$ is satisfied, while $0 \le \theta_1 < \pi/2$. When $0 \le \varphi < \pi/2$, the phasor diagram is shown in Figure 83(a), where $\zeta = \pi/2 - \theta_1 + \varphi \le \pi/2$. According to (73), (76) and (91), the current stress of power devices in phase B will increase when $V_{ac} > 2V_{Cr}\cos\zeta$.

$$I_{C_r}{}^2 + I_{ac}{}^2 - 2I_{C_r} I_{ac} \cos\zeta = I_B{}^2 \tag{91}$$

When $0 \le \theta_1 < \pi/2$ and $-\pi/2 \le \varphi < 0$, the phasor diagram is shown in Figure 83(b), where $\zeta = \pi/2 - \theta_1 - \varphi \le \pi/2$. Then combined with equation (73), (76) and (91), it is concluded that the current stress of power devices in phase B will increase when $V_{ac} > 2V_{Cr}\cos\zeta$. When $\pi/2 \le \theta_1 < \pi$, there is $\pi/2 \le \varphi < 3\pi/2$. If $\pi/2 \le \varphi < \pi$, there is $\theta_1 - \varphi \le 0$. The phasor diagram of this case is shown in Figure 83(c), where $\zeta = \pi/2 - \theta_1 + \varphi > \pi/2$. When $\pi/2 \le \theta_1 < \pi$ and $\pi \le \varphi < 3\pi/2$, the phasor diagram of this case is shown in Figure 83(d) where $\zeta = \pi/2 - \theta_1 + \varphi > \pi/2$. Therefore, for $\pi/2 \le \theta_1 < \pi$ the current stress of phase B will definitely increase.

4.4.2 Two phase legs with the solution II

For the dependent modulation with the solution II, the current flowing through phase B equals to the sum of the grid current and that through energy storage capacitor C_r. However, due to the double line frequency component in the current flowing through the capacitor C_r, it is not convenient to use the phase diagrams to analyze the current stress. Thus a 3D mesh grid on the basis of (92) is plotted in Fig. 84, where V_{ac}, I_{ac} and C_r are known. η_r represents the ratio of ac voltage ripple to the peak voltage across energy storage capacitor as defined in (81). At the same time, while keeping η_r constant,

the currents through phase B have different waveforms with different φ. Here, $\varphi=\theta_2$ is satisfied. Assuming that the grid current is 2 A in Figure 84, it is observed that the current stress are always higher than the gird current. While keeping φ constant, the larger η_r means larger peak value of the current through phase B. From (92), the peak value of $i_B(t)$ is minimum and equals to the grid current at η_r=0,. Therefore, it is concluded that the current stress of phase B will increase in this case.

$$\begin{aligned} i_B(t) &= i_{ac}(t) + i_{C_r}(t) = I_{ac}\sin(\omega t+\varphi) + 2A_2\omega C_r\cos(2\omega t+\theta_2) \\ &= I_{ac}\sin(\omega t+\varphi) + \sqrt{V_{ac}I_{ac}\omega C_r}\sqrt{\frac{\eta_r}{2-\eta_r}}\cos(2\omega t+\theta_2) \end{aligned} \tag{92}$$

4.4.3 Two phase legs with the solution III

For the dependent modulation strategy with the solution III, while $0\le\omega t+\theta_1\le\pi$, $v_{Cr}(t)=A_1\sin(\omega t+\theta_1)$; while $\pi\le\omega t+\theta_1\le 2\pi$, $v_{Cr}(t)=-A_1\sin(\omega t+\theta_1)$. To evaluate the current stress of the shared phase leg, phase diagrams are plotted by considering θ_1=0 and φ=0 separately. While θ_1=0, from $\theta_1=\varphi/2+\pi/4$ or $\theta_1=\varphi/2-3\pi/4$, the phase diagram is illustrated in Figure 85(a) where the solid red line and the dot blue line represent $0\le\omega t+\theta_1\le\pi$ and $\pi\le\omega t+\theta_1\le 2\pi$ respectively. From that, it is observed that while $0\le\omega t+\theta_1\le\pi$, $i_{ac}(t)$ and $i_{Cr}(t)$ has 180 degree phase shift, which means decreased current stress through shared phase leg. While $\pi\le\omega t+\theta_1\le 2\pi$, $i_{ac}(t)$ and $i_{Cr}(t)$ has 0 degree phase shift, which means increased current stress through shared phase leg. Therefore, the current stress will increase within one line cycle at θ_1=0. While φ=0 which means unity power factor, from $\theta_1=\varphi/2+\pi/4$ or $\theta_1=\varphi/2-3\pi/4$, it is obtained that $\theta_1=\pi/4$ or $-3\pi/4$. Through Figure 85(b), it is revealed that while $0\le\omega t+\pi/4\le\pi$, the current through the shared phase leg, marked by dot red line, can be increased or decreased. While $\pi\le\omega t+\pi/4\le 2\pi$, the current through the shared phase leg,

marked by dot blue line, will increase. Thus, the current stress through the shared phase leg will increase within one line cycle, $0 \leq \omega t + \pi/4 \leq 2\pi$. The similar results can be derived while $0 \leq \omega t - 3\pi/4 \leq 2\pi$. Based on this analysis, the current stress of the shared phase leg in power decoupling techniques with two phase legs and the solution III will increase at $\varphi=0$. Likewise, the analysis can be applied to the conditions that satisfy neither $\theta_1=0$ nor $\varphi=0$.

Based on the above discussions about current stress, it is concluded that for dependent modulation strategy, the power decoupling techniques with two phase legs will increase the current stress of the shared phase leg. Combined the discussions on dc voltage utilization in Section III, it is revealed that even though there are lower component counts, the power decoupling techniques with two phase legs have low dc voltage utilization and high current stress through the shared phase leg. Furthermore, the power decoupling techniques with three phase legs can have either increased or decreased current stress through the shared phase leg. Therefore, given the dc voltage utilization and current stress of the shared phase leg, the power decoupling techniques with three phase legs are always preferred to that with two phase legs.

4.5 Discussions

Benefiting from the independent modulation and series ripple power paths, series power decoupling techniques allow small capacitance of C_r, low voltage stress of power decoupling circuit. At the same time, series power decoupling techniques won't change the dc voltage utilization and current stress of the original single phase rectifiers or

inverters. However, the capacitance of C_b is still large. Even though additional single phase leg and inductor with low voltage stress can be added into power decoupling circuit to reduce the capacitance of C_b, the increased power devices and drive circuits limit its applications in low power single phase rectifiers or inverters like PV microinverters, LED drivers, etc. In contrast, parallel power decoupling techniques have broader applications in both voltage source and current source topologies. For low power and high dc bus voltage applications such as the two stage PV microinverters, the conventional passive capacitive power decoupling technique can be applied to mitigate the double line frequency ripple by combining advanced control strategies. Thus no extra components are needed, the dc bus capacitor can be replaced with reliable film capacitors, and the MPPT efficiency and the power quality of the grid current can be improved. Due to low dc voltage utilization of the main circuit, the power decoupling techniques with two phase legs are rarely used in practical applications. For the power decoupling techniques with four phase legs, even though full dc voltage utilization of both the main circuit and power decoupling circuit, and minimum power decoupling capacitance can be achieved, they are seldom used due to high component counts, especially at low power applications. Therefore, the power decoupling techniques with three phase legs are always the most popular options, which can be used as either independent or dependent modulation strategy. For the independent modulation with three phase legs, since the power decoupling circuit is totally decoupled with the main circuit, the current stress of the power devices in the main circuit will keep the same. Through analysis, it is known that buck-type power decoupling circuit with the solution

III allows minimum capacitance to decouple the ripple power. But it also introduces undesired ripple powers. To verify the validity of the minimum capacitance to buffer the ripple power, a design from grand prize winner the red electrical devils (CE+T Power), of google little box challenge is taken as example [120]. The independent modulation with buck-type power decoupling circuit shown in Figure 75 was applied in that design. The voltage across energy storage capacitor satisfied the solution II. Based on the specifications of 450 V dc input voltage, 240 V/60 Hz ac output voltage and 2 kVA power rating, the allowed minimum capacitance of energy storage capacitor can be calculated as 105 μF by (87). As discussed previously, the solution II can introduce undesired ripple powers while decoupling the double line frequency ripple power. To minimize those ripple powers, the capacitance was increased to 150 μF in the design example. Therefore, the dc bus capacitance was just 15 μF to satisfy input voltage ripple requirement (<3%). If the power decoupling technique weren't applied, the required dc bus capacitance should be at least 873 μF from (93) to limit the input voltage ripple. Through comparison, it is revealed that the power decoupling technique can greatly reduce the capacitance, and improve the power density and reliability of the single phase system. The feasibility had been verified by 100 hours test from google little box challenge.

$$C_{bus} = \frac{V_{ac} I_{ac}}{2\omega V_{dc} \Delta V_{dc}} \tag{93}$$

where C_{bus} represents the dc bus capacitance. For the dependent modulation with three phase legs, it can decouple the double line frequency ripple power completely. The minimum capacitance is the same with that of independent modulation at non-unity

power factor. At unity power factor, the minimum capacitance will be doubled. Due to the coupling between the main circuit and power decoupling circuit, the current stress of power devices through the shared phase leg can be increased or decreased as shown in Figure 83. What's more, the power decoupling techniques with dependent modulation and three phase legs can be regarded as three phase unbalanced circuits. Thus the concept of space vector pulse width modulation (SVPWM) [121] is also applicable other than the sinusoidal pulse width modulation (SPWM) mentioned previously. In that case, the dc voltage utilization of the power decoupling circuit can be increased at the cost of decreasing dc voltage utilization of the main circuit. The overall characteristics of different power decoupling techniques are summarized and compared in the main content. The comprehensive evaluations on the power decoupling techniques could be used to provide guidance on decoupling the double line frequency ripple power in different applications. Besides, some other power decoupling techniques including six-switch power decoupling, ac-link power decoupling, decoupling using the center tap of isolated transformer, and power decoupling using active buffer, etc., are also summarized in the main content.

4.6 Conclusion

The power decoupling techniques are very important to achieve the effective buffer of double line frequency ripple power in single phase rectifiers and inverters. In this paper, the general solutions I, II and III on power decoupling were derived first. Then the allowed minimum capacitance, the dc voltage utilization of the main circuit,

and the current stress of the shared phase leg for different power decoupling techniques were investigated in detail. Based on those, the comprehensive evaluations on different power decoupling techniques were summarized and compared. In general, given the component counts and the allowed minimum capacitance, parallel power decoupling techniques are always preferred to the series ones. For parallel power decoupling, the techniques with two phase legs mean coupling between the main circuit and power decoupling circuit, and the low dc voltage utilization of the main circuit. The techniques with three phase legs can be always applied in independent or dependent modulation strategies. For dependent modulation with three phase legs, both SPWM and SVPWM can be achieved with the tradeoff of dc voltage utilization between the main circuit and the power decoupling circuit. At the same time, there are some other power decoupling techniques including six-switch power decoupling, ac-link power decoupling, decoupling using the center tap of isolated transformer, and power decoupling using active buffer, etc., which satisfy different applications.

5. DUAL BUCK BASED ACTIVE POWER DECOUPLING CIRCUIT AND ITS CONTROL STRATEGY*

5.1 Introduction

For single phase inverter/rectifier, the inherent double line frequency ripple power created at ac side is adverse to the performances at both dc and ac sides. It can results in low-order harmonics at the ac side of inverter/rectifier system [83]. For grid-connected photovoltaic (PV) application, it could affect the maximum power point tracking (MPPT) efficiency of PV. For grid-tied energy storage system application, the ripple power can cause overheating and other deleterious effects on the batteries, including reduced service life span [122]. A bulky electrolytic capacitor is normally connected at dc side to store the ripple power [123-125]. But the electrolytic capacitor has the drawbacks of large volume, short lifetime and low reliability especially at high temperatures [83, 95]. To solve this problem, active methods are considered to transfer the ripple power to smaller storage components through added active circuit [99, 100, 102, 117, 126-129]. Due to the fact that the voltage of storage capacitor is allowed to vary in a much wider range without affecting the proper operation of the system, the capacitance needed can be considerably reduced. In many existing active power decoupling methods used in single phase system, at least one switching phase leg with

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two separate power switches is introduced.

Figure 86 shows the topology of single-phase H-bridge inverter system with the proposed power decoupling circuit. Two identical capacitors are employed and connected in series in the dc link. In this way, the dc-link capacitors can absorb the system ripple power. The voltages across two capacitors are controlled to have a dc

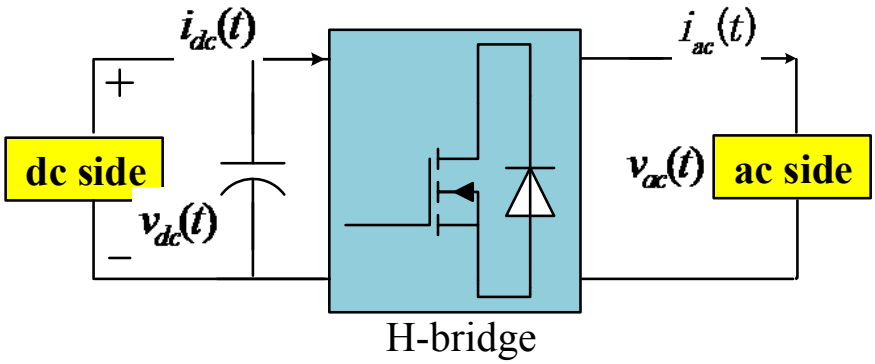
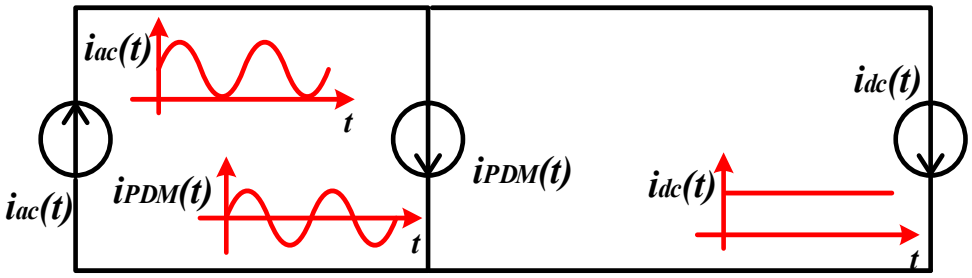


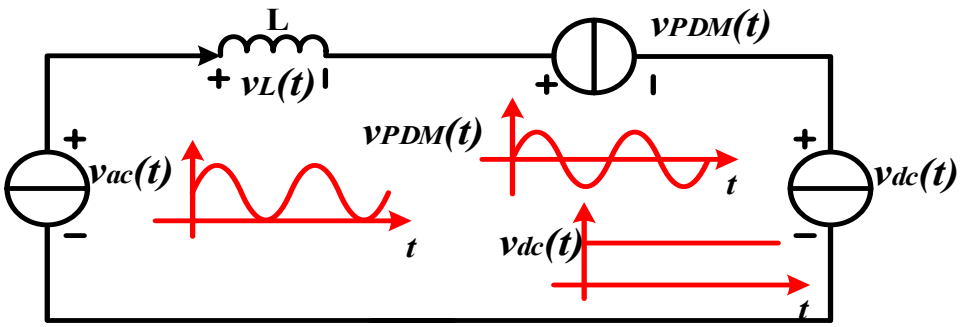
Figure 86: The typical single phase H-bridge rectifier or inverter [125].

component equal to half of dc link voltage and an ac component with the fundamental line frequency. The ac component of the two capacitors has complementary phase relationship such that the voltage ripple cancels out and the sum of voltages is constant. The capacitors can be alternatively discharged to zero in case that high ripple power compensation is required. Two capacitors exchange ripple power with the main circuit by charging and discharging action. The charging/discharging current is smoothed by the inductors.

It is known that cross conduction between switches could result into shoot through problem, which is the common failure mode of the circuit. Even though adding dead time could prevent its occurrence normally, but it may not work well in cases, especially during fault conditions. What's more, because of the dead time effect, the output waveforms can be distorted and the transferred equivalent energy of pulse-width modulation (PWM) will be reduced. Thus, it would be better to find a way to overcome this problem to increase the reliability of the system.



(a). Equivalent circuit of parallel power decoupling method.



(b). Equivalent circuit of series power decoupling method.

Figure 87: Equivalent circuit [125].

In order to achieve a simple and compact design with a high reliability, an active power decoupling circuit to eliminate the double line frequency ripple power in single phase inverter/rectifier is proposed in this section. The split dc link capacitors are directly utilized as energy storage components rather than a voltage stiffening component. The split dc-link capacitors may not merely provide the transient dc power to support ac/dc or dc/ac conversion, but can also absorb the system ripple power. The energy stored in the split capacitors can be fully charged and discharged with a high energy utilization. Thus, a smaller total capacitance value is needed. The added power switches does not need dead time during switching, which maximizes the energy transferred to storage components. It completely eliminates the shoot through concerns, thus leading to greatly enhanced system reliability. Moreover, the body diode of MOSFET never conducts due to the unidirectional current characteristics of each phase leg. The freewheeling diodes used can be independently selected to minimize the switch losses.

To fulfill the function of the proposed power decoupling circuit, a modulation and control strategy is proposed in this section. The working fundamental and system model is analyzed and derived to help design the circuit and to control system parameters. Finally, a prototype is fabricated in the laboratory to testify the proposed method. The experimental results and simulation results verified its effectiveness.

Typical structure of single phase voltage source rectifier or inverter is shown in Figure 86. Generally, there is a large electrolytic capacitor at dc side to provide transient power and store the double line frequency ripple power at dc side. Active power

decoupling circuit with high bandwidth could be introduced to improve the system power density. The added active power decoupling circuit could be placed in series or in parallel with the main circuit. Their corresponding equivalent circuits are shown in Figure 87. Parallel connection based methods are preferred due to its easiness in terms of switch modulation and control on power decoupling circuit [115, 130, 131].

5.2 Topology and operation

The proposed circuit is, in principle, two separate buck converters, which are made up of a left bridge leg (S_1,D_1,L_1) and a right bridge leg(S_2,D_2,L_2), terminated with a split dc link, which is operated as the energy storage device or the buffer for the ripple power.

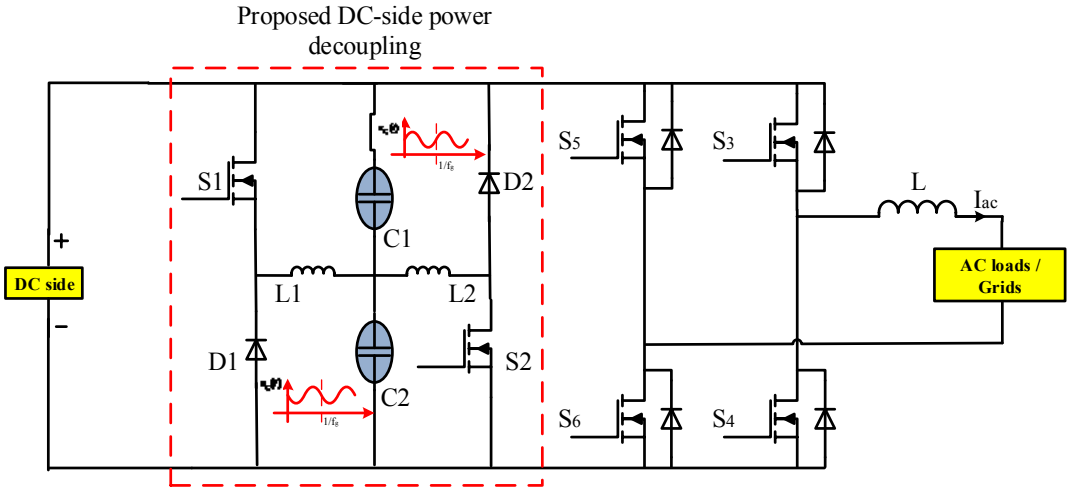


Figure 88: System configuration.

Due to the unidirectional inductor currents in both legs, each phase leg will only work in a half cycle. When current through inductor L_1 is positive, the left phase leg works. In this mode, S_2 is always OFF, and S_1 is driven by a PWM signal with the diode D_1 freewheeling the inductor current to the capacitor C_1 and C_2. Capacitor C_1 discharge its energy while capacitor C_2 works in charging mode. When current through inductor L_2 is positive, the right phase leg works. In this mode, S_1 is always OFF, and S_2 is driven by a PWM signal with the diode D_2 freewheeling the inductor current to the capacitor C_1 and C_2. Capacitor C_2 discharge its energy while capacitor C_1 works in charging mode.

As buck converter, each phase leg can operate in either continuous conduction mode (CCM) or discontinuous mode operation (DCM). To simplify the analysis of the operational principle, it is assumed that all inductors and capacitors are idea, $C_1=C_2$, $L_1=L_2$. Furthermore, power switches and diodes are thought to be ideal devices ignoring switching loss and conduction voltage drops in the analysis. The operating procedures of the right bridge leg are the same as those of the left bridge leg.

There are four operating modes for the proposed decoupling circuit. Each phase leg has two operating modes during every switching period, and only works in half cycle, which is determined by the capacitor current. The operating condition is illustrated in Figure 90. The following analysis is based on the CCM operating condition, while the operating principle and analysis are also applicable to DCM.

When S_1 is ON, S_2 is OFF. The circuit operation is shown as Figure 89(a), the inductor current increases linearly

$$L_1 \frac{di_{L1}}{dt} = V_{dc} - V_{C2} = V_{C1} \tag{94}$$

In this case, C_1 works in discharging condition and it sends energy to L_1. While current through C_2 is determined by condition of main circuit and the ripple power value. The voltage stress of the freewheeling diode D_1 is the input voltage.

When S_1 is OFF, S_2 is OFF and the current through inductor L_1 is nonzero. The current i_{L1} will continue to run through the freewheeling diode D_1. The circuit operation is shown as Figure 89(b), the inductor current decreases linearly

$$L_1 \frac{di_{L1}}{dt} = -V_{C2} \tag{95}$$

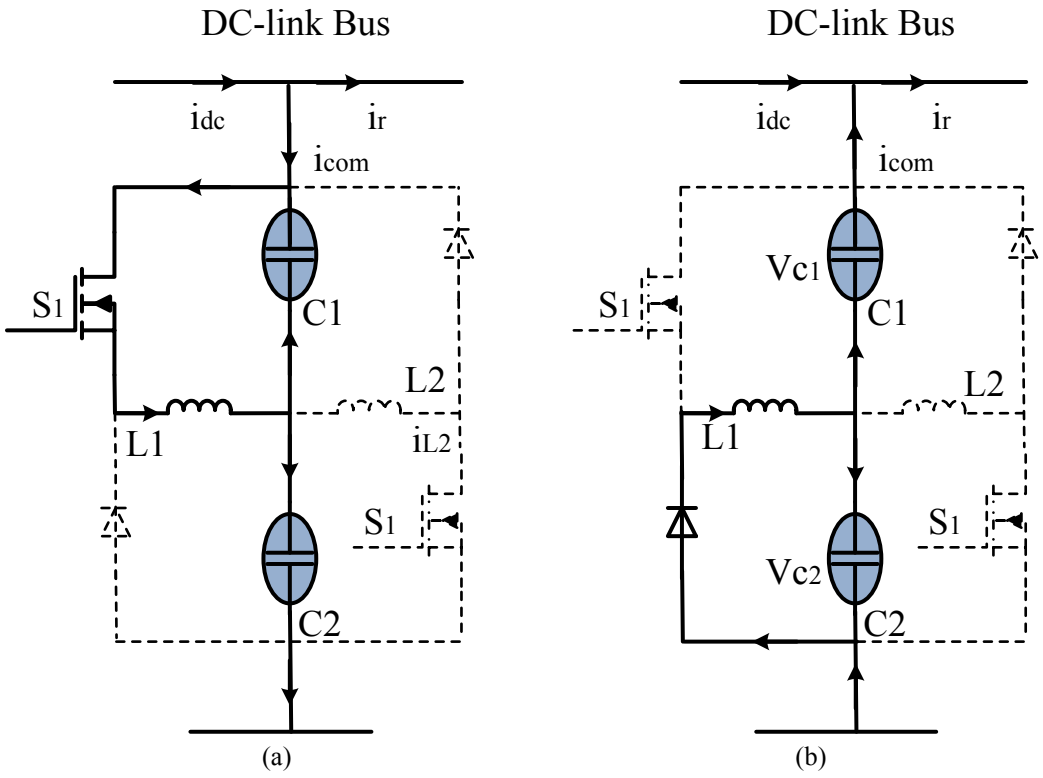


Figure 89: Different circuit operating conditions [125].

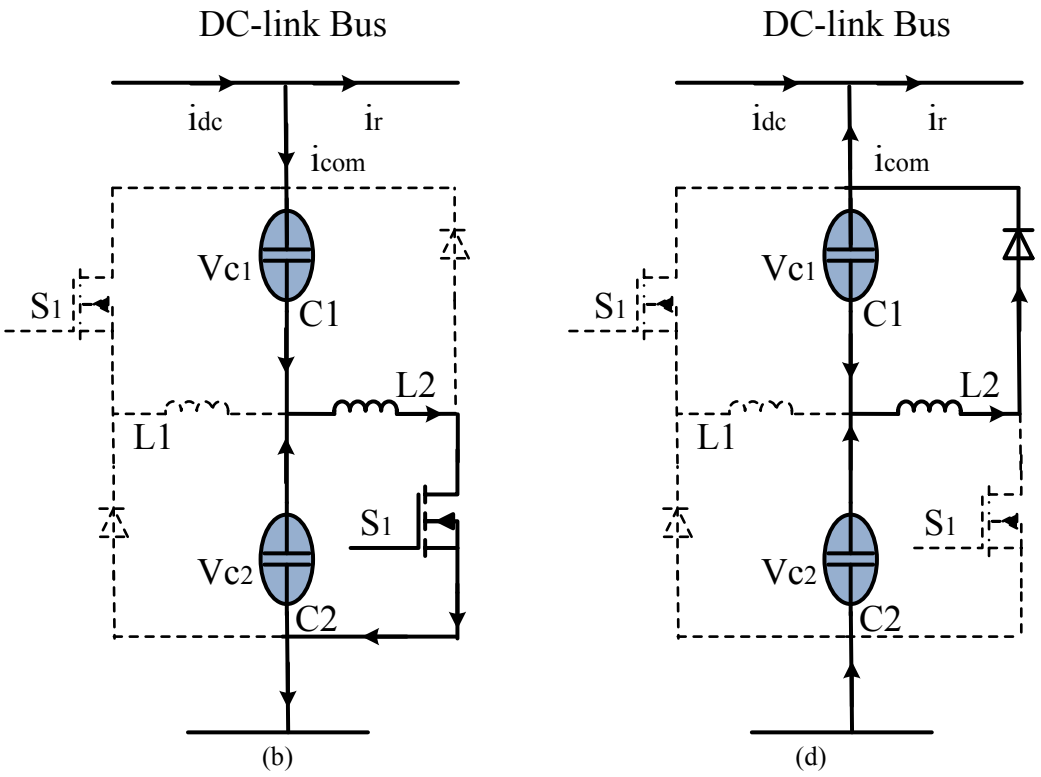


Figure 89: Continued.

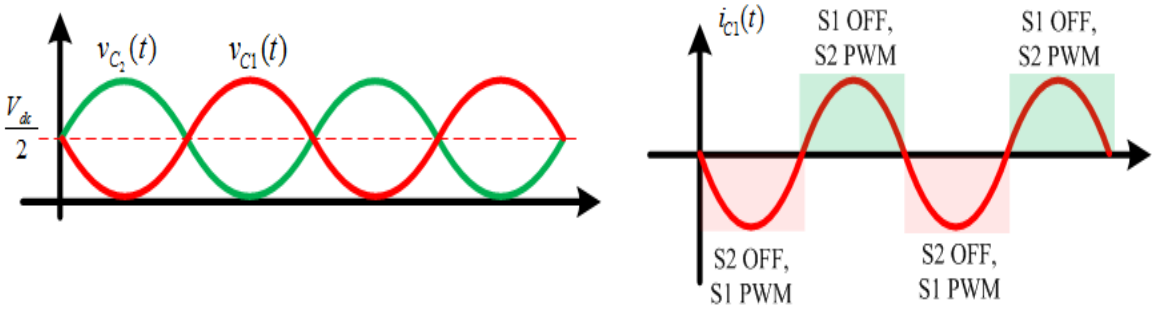


Figure 90: Operating waveform and conditions [125].

In this case, the current through C_1 is equal to i_{com}. While current through C_2 is equal to the sum of i_{com} and i_{L1}. The voltage stress of the switch S_1 is the input voltage.

When the capacitor current change the direction, another phase leg begins to operate and then the circuit operate in the other two modes. When the right phase leg operates, the switch in left phase leg will keep off.

When S_2 is ON, S_1 is OFF. The circuit operation is shown as Figure 89(3), the inductor current increases linearly

$$L_2 \frac{di_{L2}}{dt} = V_{dc} - V_{C1} = V_{C2} \tag{96}$$

In this case, C_1 works in discharging condition and sends energy to L_2. While current through C_1 is determined by condition of main circuit and the ripple power value. The voltage stress of the freewheeling diode D_2 is the input voltage.

When S_2 is OFF, S_1 is OFF and the current through inductor L_2 is nonzero. The current i_{L2} will continue to run through the freewheeling diode D_1. The circuit operation is shown as Figure 89(4), the inductor current decreases linearly

$$L_2 \frac{di_{L2}}{dt} = -V_{C1} \tag{97}$$

In this case, the current through C_2 is equal to i_{com}. While current through C_1 is equal to the sum of i_{com} and i_{L2}. The voltage stress of the switch S_2 is the input voltage.

5.3 Analysis and controller design

In order to select the control system parameters, the average small-signal model of the voltage balancer under CCM is derived. The duty cycles of S1 and S2 are defined as $d1$($d1 = D1 + d1$) and $d2$($d2 = D2 + d2$), respectively, where $D1$, $D2$, $d1$, and $d2$ are stable duty ratios and the perturbations of $d1$ and $d2$. Moreover, the voltage $u$in and $u$out2 are defined as $u$in = Uin + $\hat{u}$in and $u$out2 = U_{out2} + $\hat{u}$out2, respectively, where

*U*in, *U*out2, $u\hat{}$in, and $u\hat{}$out2 are the stable voltage values and the perturbations of *u*in and u_{out2}.

5.3.1 Average Small-Signal Model of Bridge Leg with switch S1

The following shows the average small-signal model derivation when switch S1 operates in PWM mode and S2 keeps off.

When S1 is on

$$\begin{cases} v_{L1} = L_1 \frac{di_{L1}}{dt} = v_{in} - v_{C2} \\ i_{C2} = C_2 \frac{dv_{C2}}{dt} = i_{L1} + C_1 \frac{d(v_{in} - v_{C2})}{dt} \end{cases} \tag{98}$$

When S1 is off,

$$\begin{cases} v_{L1} = L_1 \frac{di_{L1}}{dt} = v_{C2} \\ i_{C2} = C_2 \frac{dv_{C2}}{dt} = i_{L1} + C_1 \frac{d(v_{in} - v_{C2})}{dt} \end{cases} \tag{99}$$

According to the methods of building average model, the following equation could be derived out.

$$\begin{cases} L\dfrac{d\hat{i}_{L1}}{dt} = D_1\hat{v}_{in} + \hat{d}_1 v_{in} - \hat{v}_{C2} \\ 2C\dfrac{d\hat{v}_{C2}}{dt} = \hat{i}_{L1} + C\dfrac{d\hat{v}_{in}}{dt} \end{cases} \tag{100}$$

The transfer function of the output voltage versus the duty cycle can be represented as.

$$G(s) = \left.\frac{\hat{v}_{C2}(s)}{\hat{d}_1(s)}\right|_{\hat{v}_{in}(s)=0} = \frac{V_{in}}{2LCs^2 + Ls\dfrac{I_{ac}}{V_{ac}}} \tag{101}$$

5.3.2 Average Small-Signal Model of Bridge Leg with switch S2

The following shows the average small-signal model derivation when switch S2 operates in PWM mode and S1 keeps off.

When S2 is on

$$\begin{cases} v_{L2} = L_2 \frac{di_{L2}}{dt} = v_{C2} \\ i_{C1} = C_1 \frac{dv_{C1}}{dt} = i_{L2} + C_2 \frac{d(v_{in} - v_{C1})}{dt} \end{cases} \tag{102}$$

When S2 is off

$$\begin{cases} v_{L2} = L_2 \frac{di_{L2}}{dt} = v_{in} - v_{C2} \\ i_{C1} = C_1 \frac{dv_{C1}}{dt} = i_{L2} + C_2 \frac{d(v_{in} - v_{C1})}{dt} \end{cases} \tag{103}$$

According to the methods of building average model, the following equation could be derived out

$$\begin{cases} L \frac{d\hat{i}_{L2}}{dt} = \hat{v}_{C2} - (1 - D_2)\hat{v}_{in} + \hat{d}_2 v_{in} \\ 2C \frac{d\hat{v}_{C2}}{dt} = C \frac{d\hat{v}_{in}}{dt} \hat{i}_{L1} - \hat{i}_{L2} \end{cases} \tag{104}$$

The transfer function of the output voltage versus the duty cycle can be represented as

$$G(s) = \left. \frac{\hat{v}_{C2}(s)}{\hat{d}_2(s)} \right|_{\hat{v}_{in}(s)=0} = \frac{-V_{in}}{2LCs^2 + Ls\frac{I_{ac}}{V_{ac}}} \tag{105}$$

The critical value to make the circuit operate in CCM is as follows

$$L_{cri} = Tv_{C2}\left(1 - \frac{v_{C2}}{\sqrt{\frac{V_{ac}I_{ac}}{2C\omega}}}\right) / 2i_L \tag{106}$$

The current and voltage relationships are shown in Figure 91.

Assuming the voltage and current at AC side can be represented as

$$\begin{cases} v_{ac}(t) = V_{ac}\sin\omega t \\ i_{ac}(t) = I_{ac}\sin(\omega t + \theta) \end{cases} \tag{107}$$

Then the instantaneous power is

$$p_{ac}(t) = \frac{1}{2}V_{ac}I_{ac}\cos\theta - \left[\frac{1}{2}V_{ac}I_{ac}\cos(2\omega t - \theta) + \frac{\omega L I_{ac}^2}{2}\sin(2\omega t + 2\theta)\right] \tag{108}$$

In order to store the double-line frequency ripple power in two storage capacitors while holding the dc link voltage, the voltage of them are controlled to be sinusoidal

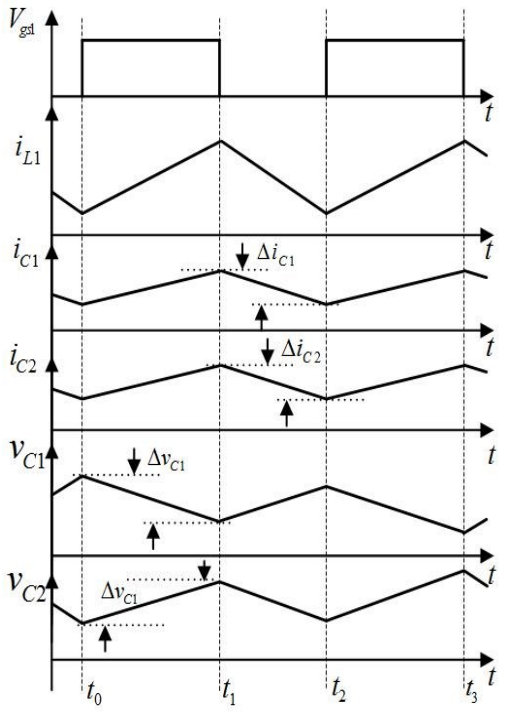


Figure 91: Main current relationship waveforms of the left bridge leg.

with fundamental frequency and an offset DC value that equals to half of the dc-link voltage $V_{dc}/2$. Their instantaneous value together with their individual currents can be represented as

$$\begin{cases} v_{C2}(t) = \dfrac{V_{dc}}{2} + V_c \sin(\omega t + \theta_c) \\ v_{C1}(t) = \dfrac{V_{dc}}{2} - V_c \sin(\omega t + \theta_c) \end{cases} \tag{109}$$

In this case, two identical capacitors are connected in series, $C_1=C_2=C$. The instantaneous power pc (t) provided by these two capacitors is

$$p_c(t) = v_{C1} i_{C1} + v_{C2} i_{C2} = C\omega V_c^2 \sin(2wt + 2\theta_c) \tag{110}$$

According to (108) and (110), and assuming the stored energy in the inductor is negligible, the following equations are derived:

$$\begin{cases} V_c = \sqrt{\dfrac{V_{ac} I_{ac}}{2C\omega}} \\ \theta_c = \theta - \dfrac{\pi}{4} \end{cases} \tag{111}$$

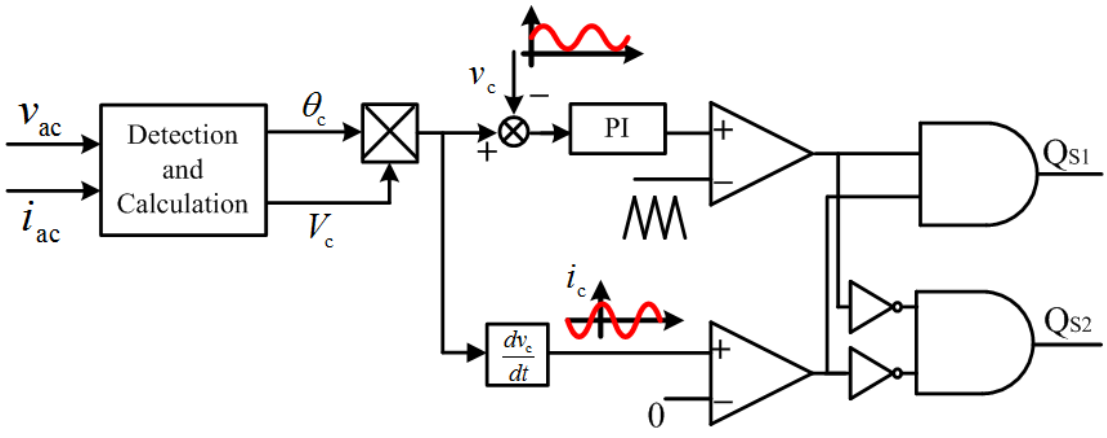


Figure 92: Control strategy of power decoupling circuit.

Equation (111) shows the condition to completely buffer ripple power through power decoupling circuit. Based on that, a control strategy is proposed to regulate the decoupling performance with feedback loop. The proposed control strategy is presented in Figure 92. A voltage loop is formed to regulate the capacitor voltage and ensure its value tracks the derived reference value which is determined by the voltage and current condition in ac side of main circuit. The output signal of the voltage regulator is directly sent to modulate the switches, and its differential value determine the conduction cycle of phase legs.

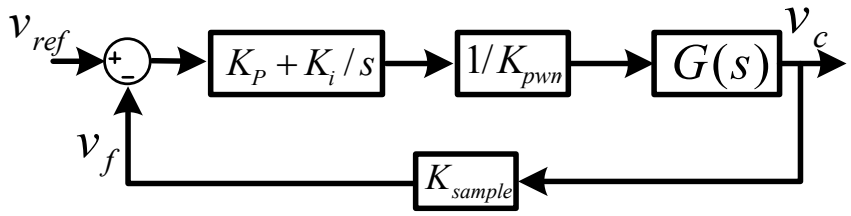


Figure 93: Block diagram of the controller.

The closed loop transfer function of the control system, $\phi(s)$, can be obtained based on block diagram as follows.

$$\phi(s) = \frac{(K_P + K_i / s) \cdot G(s)}{K_{pwm} + K_{sample}(K_P + K_i / s)G(s)} \tag{112}$$

$$G(s) = \frac{V_{in}}{2LCs^2 + s\, L/Z_m} \tag{113}$$

where, $Z_m = V_{ac}/I_{ac}$

$$\phi(s) = \frac{(K_P + K_i / s) \cdot \dfrac{V_{in}}{2LCs^2 + s\, L/Z_m}}{K_{pwm} + K_{sample}(K_P + K_i / s)\dfrac{V_{in}}{2LCs^2 + s\, L/Z_m}} \tag{114}$$

The main function of C_1 and C_2 is to store the ripple power. Large voltage ripple is allowed. Their capacitance value is mainly determined by storing capacity. They have to be large enough to store and transfer the ripple power completely. The minimum capacitance value needed considering the fully charged and discharged case can be represented as

$$C_1 = C_2 = \frac{P_{ac,\max}}{\omega V_{dc}^{\ 2}} \tag{115}$$

The main function of inductor L_1 and L_2 is to smooth the current ripple in each phase leg. Large inductor may lead to more energy stored in it, which would decrease the energy storing capability of the power decoupling module. On the other hand, small inductor may lead the circuit work in *DCM* mode. The critical value to make the circuit operate in CCM is listed as follows.

$$L_{cri} = T v_{c2}\left(1 - \frac{v_{c2}}{\sqrt{\dfrac{V_{ac} I_{ac}}{2C\omega}}}\right) / 2i_L \tag{116}$$

5.4 Simulation and experimental results

The proposed power decoupling circuit is evaluated based on single phase inverter prototype. Table 4 lists the system specifications in different cases. In order to show the effectiveness of the proposed power decoupling system, the comparative simulation and experimental results are given between single phase inverter systems with and without the proposed power decoupling circuit.

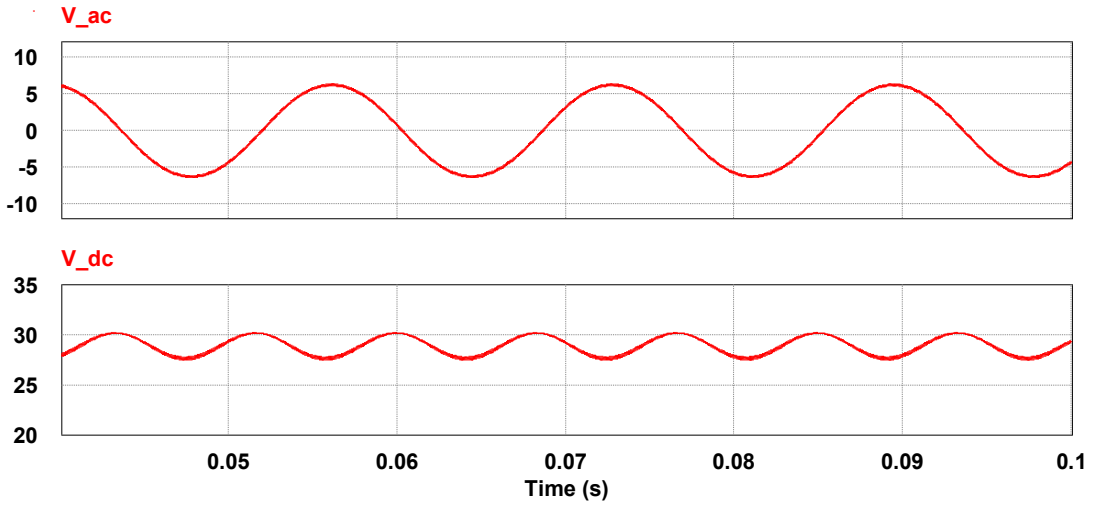
Table 4: Electrical specifications in simulation [125].

V_{dc}=30V $M_{(modulation\ index\ of\ inverter)}$=0.3, R_{load}=2Ω	C_{dc}=470 uF (without power decoupling circuit)	$\Delta V_{dc}/V_{dc}$=16% (without power decoupling circuit)
	C_1=C_2=220 uF (with power decoupling circuit)	$\Delta V_{dc}/V_{dc}$=4.7% (with power decoupling circuit)
V_{dc}=300V $M_{(modulation\ index\ of\ inverter)}$=0.6, R_{load}=10Ω	C_{dc}=470 uF (without power decoupling circuit)	$\Delta V_{dc}/V_{dc}$=9.3% (without power decoupling circuit)
	C_{dc}=1500 uF (without power decoupling circuit)	$\Delta V_{dc}/V_{dc}$=3% (without power decoupling circuit)
	C_1=C_2=90 uF (with power decoupling circuit)	$\Delta V_{dc}/V_{dc}$=3.3% (with power decoupling circuit)
	C_1=C_2=220 uF (with power decoupling circuit)	$\Delta V_{dc}/V_{dc}$=1.1% (with power decoupling circuit)

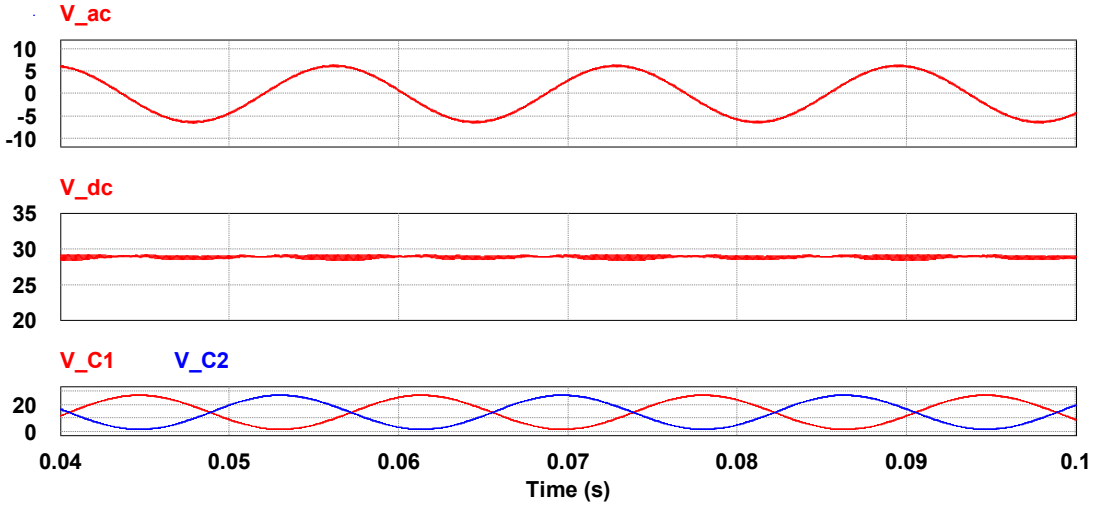
Figure 94 shows the comparative simulation results about steady state of single phase inverter system with and without proposed power decoupling circuit when the dc link voltage is 30V. As shown in figure 94(a), normally, though there is a 470 uF capacitor connected in dc-link., there still remains a big voltage ripple and current ripple

at dc side. With an active power decoupling circuit with smaller capacitors, the dc link voltage ripple could be reduced largely.

Figure 95 shows the comparative steady state simulation results of single phase inverter system with and without proposed power decoupling circuit when the dc link voltage is 300V. As shown in Figure 95, normally, though there is a big capacitor connected in dc-link, there still remains a big voltage ripple and current ripple at dc side. With an active power decoupling circuit with smaller capacitors, the dc link voltage ripple could be reduced largely. When the dc link voltage is 300 V, with a much smaller dc link capacitor, the dc link voltage ripple could be regulated well with the proposed power decoupling circuit as shown in Figure 96. The steady-state simulation results of dc link voltage and component waveforms are shown in details. Thanks to the smooth dc-link voltage, the output voltage of ac load can be regulated well with sinusoidal waveform and smaller THD value. The two film capacitors can provide the required double-line frequency ripple power, and the dc-link voltage has much smaller voltage variation. The comparative results can be seen in Figure 95(b) which presents the steady state for system without power decoupling circuit but with big dc link capacitor. It can be seen that the proposed power decoupling circuit has a significant reduction in 2ω ripple at dc link even with smaller capacitor.

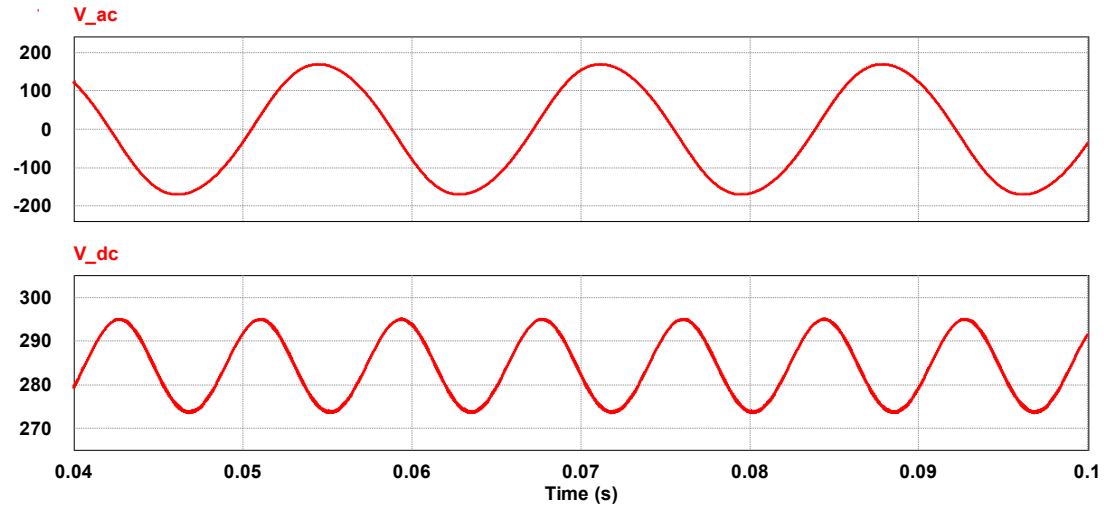


(a)

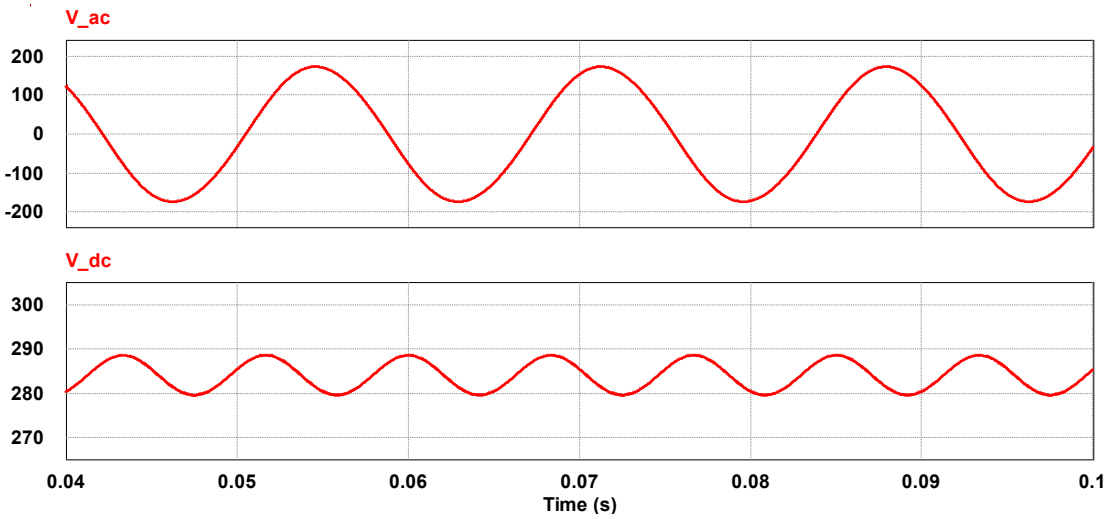


(b)

Figure 94: Simulation results in steady state when Vdc=30V.
(a) system without active power decoupling circuit, Cdc=470 uF
(b) system with active power decoupling circuit, C1=C2=220 uF.



(a) case with C_{dc}=470 uF



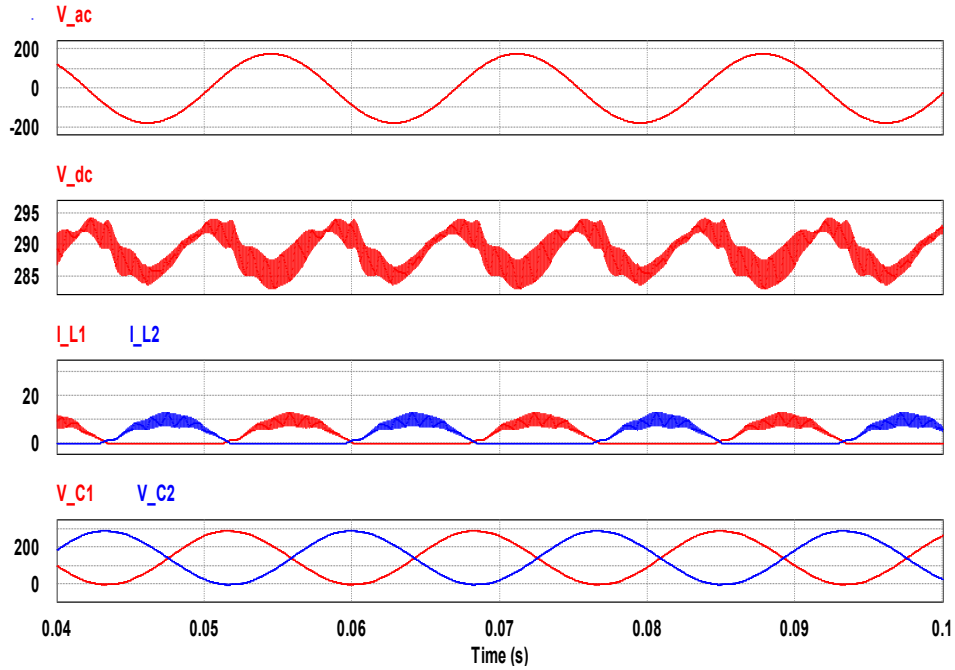
(b) case with C_{dc}=1500

Figure 95: Simulation results of system without proposed APD circuit but with big dc capacitor under two cases.

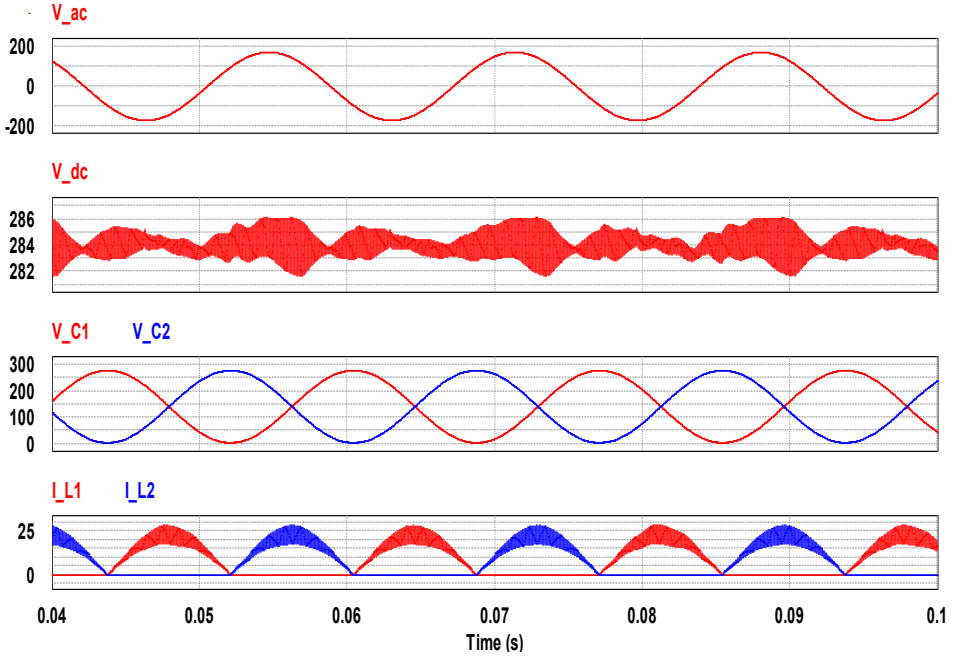
A prototype shown in Figure 97 was used to experimentally verify the performance of proposed power decoupling system and its operating principle. The system parameters are the same with those shown in Table 5. The control algorithm was implemented based

on TI Piccolo F28035 DSP, in which 3 different timer based tasks are scheduled to deal with the non-urgent tasks. Besides, 3 interrupt service routines are used as the front to deal with the urgent things, such as the close loop controllers, the capture event and protection. Three channels of ADC are used to sample three variables: output voltage main circuit (*Vac*), load current of main circuit (*Iac*) and voltage of decoupling capacitor C2(*Vc*). According to the flowchart in Fig. 98, there are mainly few parts in the main routine: a) sample variables; b) rms value of the reference voltage (V_{ref}) determination and mode selection; and c) loop compensation d) digital PWM to update pulse width of switch gate signal.

Figure 99 and 100 shows the comparative steady state experiment results of single phase inverter system with proposed power decoupling circuit when the dc link voltage is 30V. Figure 99 shows the system performance without proposed power decoupling module. The dc-link capacitor used in this case is 470 uF. Figure 100 shows experimental results after power decoupling module is added. Thanks to the smooth dc-link voltage, the output voltage of ac load can be regulated well with sinusoidal waveform and smaller THD value. The two film capacitors can provide the required double-line frequency ripple power, and the dc-link voltage has much smaller voltage variation.



(1) Case with C1= C2=90 uf



(2) Case with C_1= C_2=220 uf

Figure 96: Simulation results with proposed APD circuit under two cases.

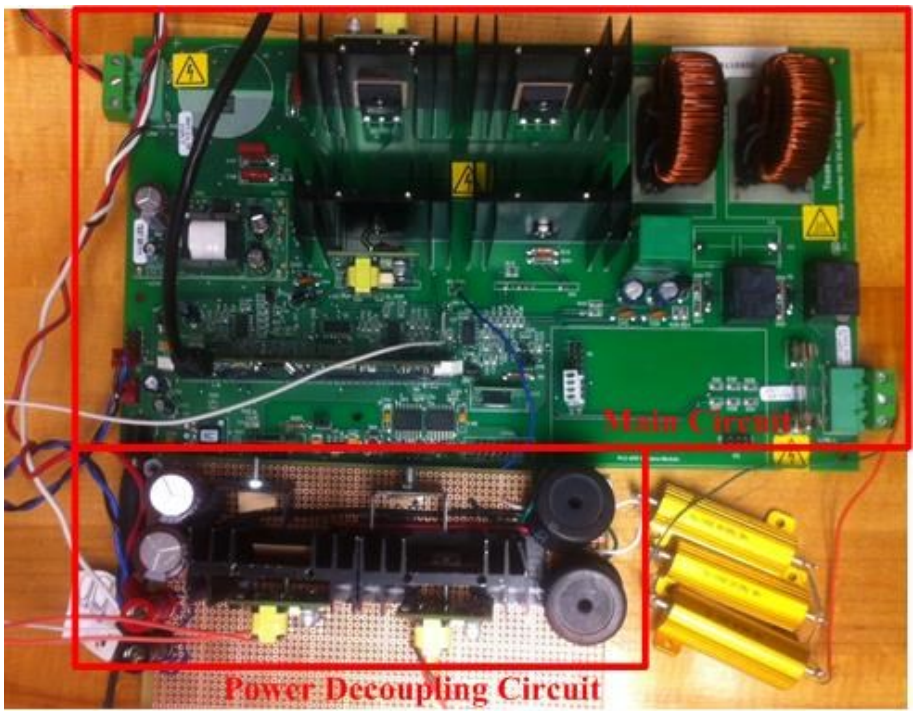


Figure 97: Experimental setup [125].

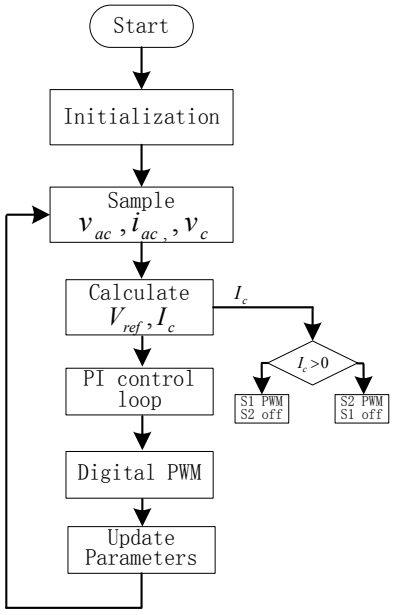


Figure 98: Flowcharts of the algorithms running on the DSP system.

Table 5: System parameter.

Vdc	200 V	**L**	1.2 mH
R_load	10 Ohm	**Cdc**	180 uF
P_load	500 W	**fsw**	20k Hz

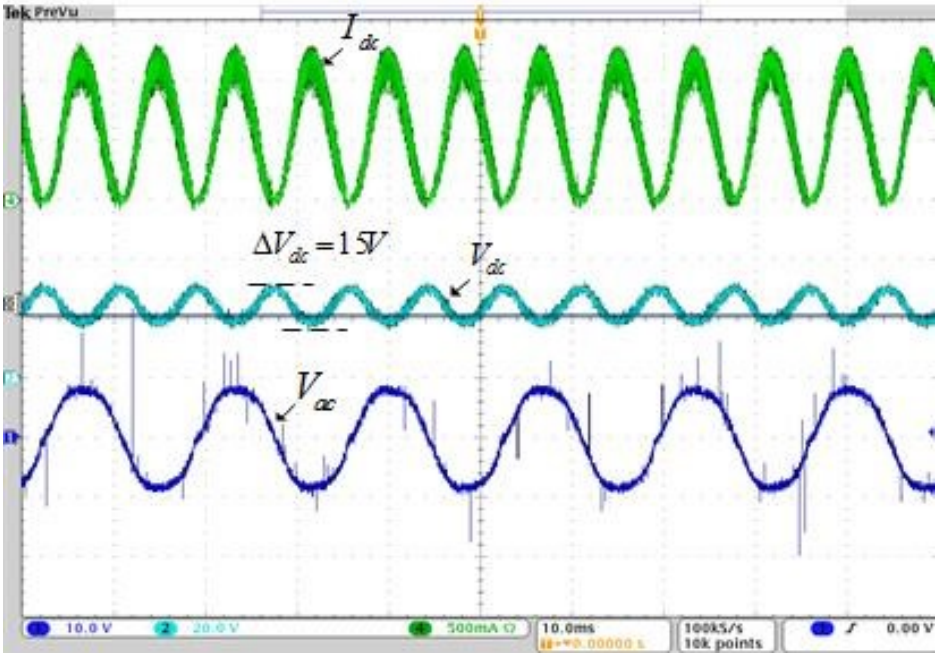
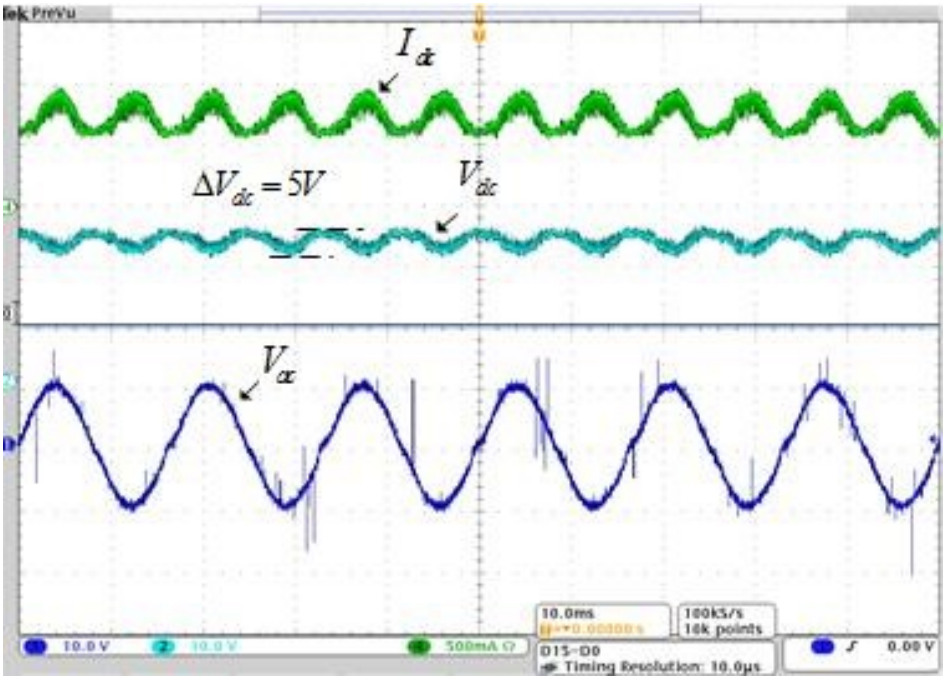
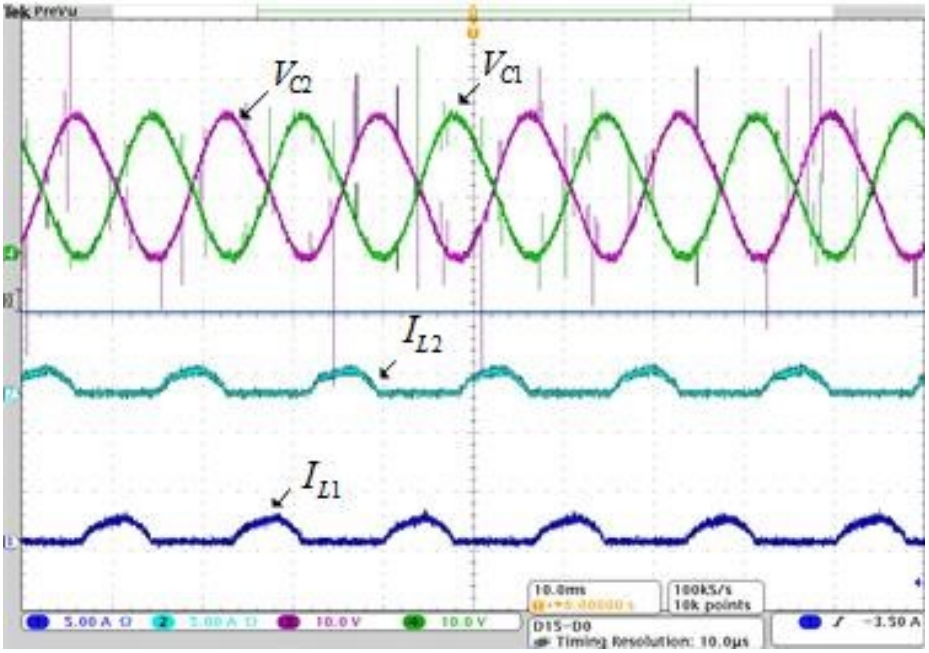


Figure 99: Steady state performance of main circuit without proposed circuit.

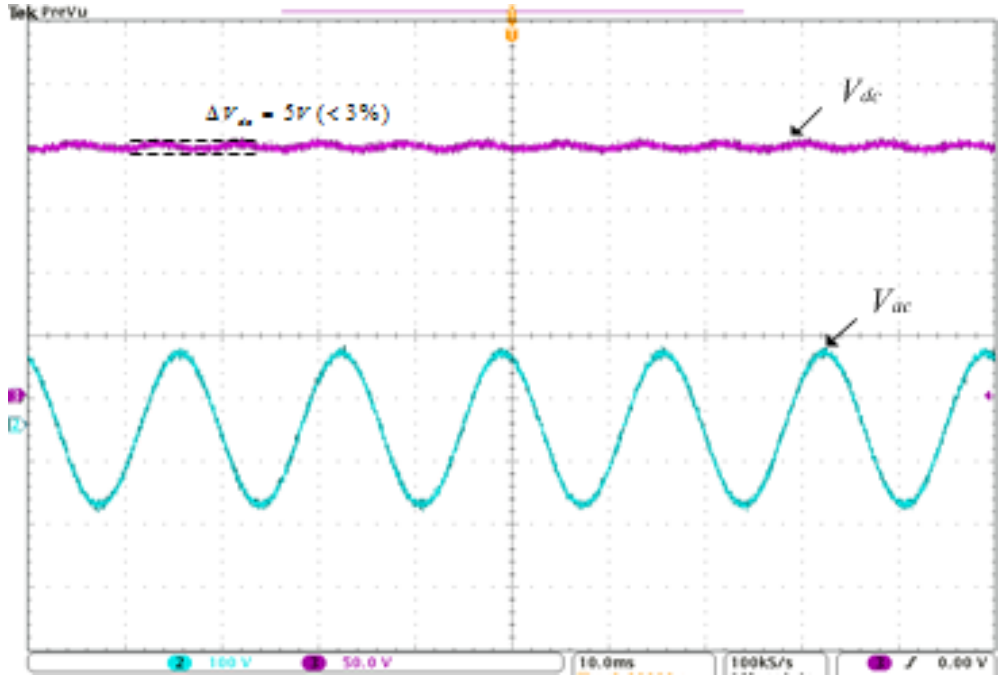


(a)

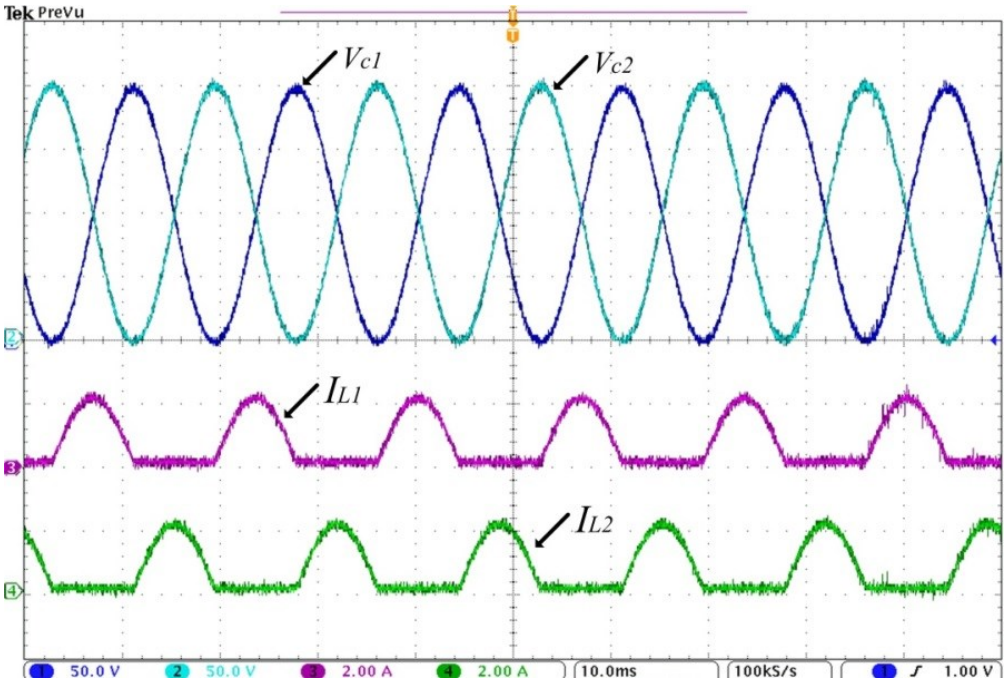


(b)

Figure 100: Steady state performance with proposed circuit.



(a)



(b)

Figure 101: Steady state performance with proposed circuit.

Figure 101 shows experimental results of system with proposed power decoupling module when the dc link voltage is 300V. It can be seen that the proposed topology and control method can eliminate double line frequency ripple power and diminish the voltage ripple at dc link greatly even with smaller capacitor. The voltage of dc link capacitors and current through smoothing inductors are shown in Figure 101(b). As shown in results, the voltage in two capacitors have complementary ac component, which ensures the small fluctuation on dc link voltage. Each phase leg in power decoupling module operates in half cycle. The experimental results coincide well with simulation results.

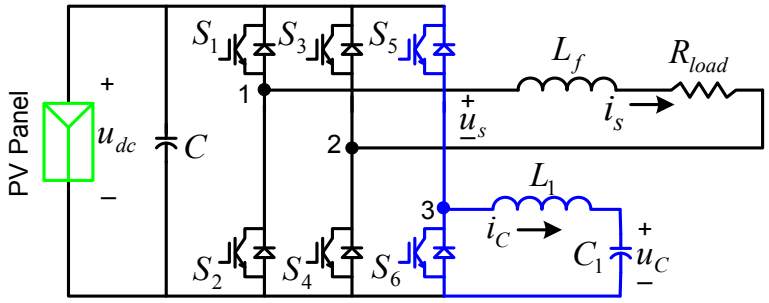


Figure 102: Convention topology 1.

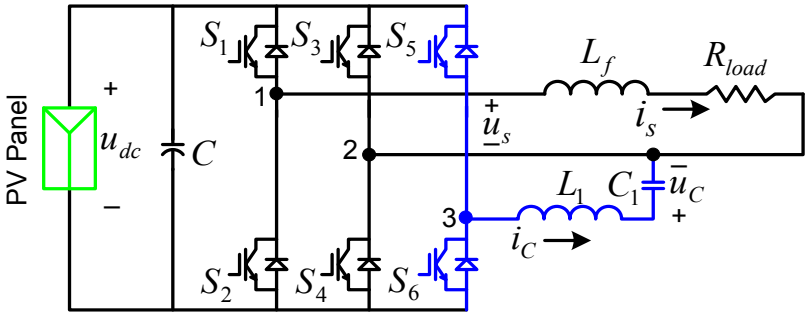


Figure 103: Conventional topology 2.

Table 6: Comparison with conventional topology.

	Topology 1	Topology 2	Proposed Topology
Total capacitance	$C_r = \frac{V_{ac} I_{ac}}{4\omega A_0 A_2}$	$C_r = \frac{V_{ac} I_{ac}}{\omega A_1^2}$	$C_r = \frac{V_{ac} I_{ac}}{\omega A_1^2}$
Capacitor voltage	$V_{C_r} = \sqrt{\frac{V_{ac} I_{ac} \cos\varphi - \omega L I_{ac}^2 \sin 2\varphi}{(2-\eta_r)\eta_r \omega C_r \cos\theta_2}}$	$V_{C_r} = \sqrt{\frac{V_{ac} I_{ac} \cos\varphi - \omega L I_{ac}^2 \sin 2\varphi}{\omega C_r (1-\omega^2 L_s) \sin 2\theta_1}}$	$V_{C_r} = \frac{V_{dc}}{2} + \sqrt{\frac{V_{ac} I_{ac} \cos\varphi - \omega L I_{ac}^2 \sin 2\varphi}{2\omega C_r (1-2\omega^2 L_s) \sin 2\theta_1}}$
Voltage utilization (main/decoupling circuit)	High	Low	High
Control complexity	Low (independent)	High	Low (independent)
Other ripple powers introduced	Fourth	None	None

Figure 102 and Figure 103 show two other topologies used to achieve the APF by employing the standard three-phase power module those are widely applied. Table 6 summaries the comparison between the proposed topology with the other two topologies in terms of total capacitance, capacitor voltage, voltage utilization, system control complexity and ripple composition. As shown in the comparison results, the proposed topology has several advantages compared to conventional topology. Smaller capacitance value needed and the voltage utilization of capacitor is higher. It has less control complexity and introduces no other power ripple.

5.5 Conclusion

In this section, a power decoupling circuit with dual buck converters and its control strategy are proposed. The ripple power is stored in split dc link capacitors with high energy utilization. The proposed power decoupling circuit does not need any external storage component except dc-link component. It does not have shoot-through problem, thus it could enhance the overall system reliability. There is no need of dead time, thus more energy can be transferred without introducing dead-time distortion into the current waveforms. Detailed description on circuit's working fundamental and its design process on circuit components and controller is presented. The proposed power decoupling circuit could heavily reduce the storage capacitance needed, which is validated through simulation and hardware results.

6. CONCLUSIONS AND FUTURE WORK

This dissertation focused on improving performance of single phase inverter with proposed advanced control strategies and active power decoupling circuit.

A novel independent PQ control method based on multi-loop control structure in stationary reference frame is presented and analyzed. A model predictive decoupled power control scheme for single phase grid-connected inverter is proposed based on model predictive control with different system constrains easily combined. Furthermore, a controller based on model predictive control method with capability to operate in both island condition and grid-connected condition and seamless transfer between them is presented and explained. Modeling and evaluation of grid-connected inverter operating in different modes were done and the discrete power prediction model for MPC technique application on grid-connected inverter was derived. The stability analysis on Model predictive control for grid-tied inverter was conducted.

At the same time, the double line frequency power decoupling techniques for single phase inverter system have been investigated with comprehensive analysis and comparison. Based on the comparison and conclusion derived generally, a new active power decoupling circuit with independent control and modulation with that of main circuit is proposed and analyzed in detail.

Effectiveness of proposed techniques and methods and their analysis is checked by simulation and experiment.

The studies in this dissertation opened new challenges and chances that require further investigation and could be the future work, which can be listed as:

Regarding the independent power control, its dynamic reactive power can be control and regulated based on the grid side condition and operator. It would be interesting to explore the possibility to apply proposed control method into specific application, such as low voltage ride-through control of single-phase PV systems, which can contribute to the grid voltage stability and the avoidance of energy losses during low-voltage grid fault.

Combining new control objectives and system constrains into the cost function of model predictive control applied for single phase grid-connected inverter to improve system performance in some aspects, such as harmonic reduction, efficiency and so on.

For the proposed active power decoupling circuit, its control and modulation is independent with that of main circuit. It would be interesting to explore novel ways to combine the modulation and control of both main circuit and proposed decoupling circuit to improve the reliability and efficiency of whole system.

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