LOW-DROPOUT REGULATOR WITH TRANSIENT RESPONSE ENHANCEMENT BASED ON A BANG-BANG TECHNIQUE

A Thesis

by

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ABSTRACT

The concept full chip integration of circuits has gained traction over the years with the push towards system-on-chip (SoC) designs which serve the niche for portable, low-power devices from the handheld category to wearables. As such, there is a growing trend towards the integration of Linear Dropout (LDO) regulators, which are a pivotal part of the power systems in such devices. However, removing the large output capacitor in LDOs to allow for full chip integration comes at a cost as it leads to higher overshoots and undershoots during load transients and degrades AC stability.

This work presents the design of an output capacitor-less LDO regulator which uses a bang-bang technique for reduction of overshoot and undershoot during load transients. This technique provides an alternate faster loop for transient compensation while keeping power consumption low. Also, an error amplifier which uses a combination of miller compensation and quality factor reduction technique is also employed to ensure AC stability across the load range. At an output voltage of 1.1 V, the regulator proves to be stable at loads ranging from 0-100 mA with a 100 pF load capacitance. A quiescent current consumption of 16.5 μA and a dropout voltage of 200 mV ensure a high power efficiency of 84.6%. From simulations, the worst case overshoot and undershoot of the regulator are 108 mV and 88 mV respectively with a 1% settling time of 3.2 μs and a load regulation of 0.11 mV/mA. The regulator is designed and implemented fully on-chip in IBM 130nm technology.

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Contributors

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All other work for this thesis was conducted and completed by the student independently.

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1 INTRODUCTION

The Low-dropout (LDO) voltage regulator is an integral part of SoC designs as they are lightweight and a source of cleaner power compared to switching regulators and therefore more suitable for feeding critical and sensitive blocks in the system. This being said, most power systems contain both types of regulators with LDOs placed after switching regulators to improve overall efficiency of the power supply. Figure 1.1 shows simplified diagram of a typical power subsystem for SoC.

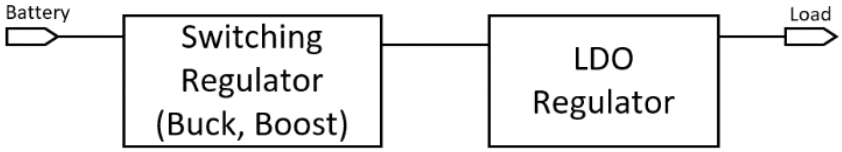


Figure 1.1: Typical SoC Power Subsystem

In order to provide both AC and transient compensation, conventional LDOs contain bulky capacitor usually in the range of microfarads which cannot be integrated because of size requirements [1] . The avoidance of the bulky off-chip capacitor allows for a more compact design and lower pin count [2]. This however comes with its own trade-offs as loop bandwidth, transient response, quiescent current and AC stability are compromised. Several techniques such as active-feedback compensation [3] damping-factor control [4] and Q-reduction compensation[5] have been proposed to address the

AC stability and quiescent current issues. Various transient response enhancement techniques have also been proposed in literature [6-8]. This works explores the performance trade-offs associated with capacitor-less LDOs and proposes a solution to alleviate them.

1.1 APPLICATIONS OF LDOs

LDO's are indispensable in most power systems and their applications are widespread and keep broadening in the circuit design world. Below is a summarized list of LDO regulator applications.

1.1.1 Hand-Held, Portable Electronics

LDOs are integral in the power systems of hand-held devices such as phones and tablets as well as wearable devices. Most of these devices are battery powered and may contain a Lithium-ion battery, whose output voltage dips with use as it discharges. An LDO is needed to provide regulated output voltage. Figure 1.2 shows the discharge profile of a typical lithium-ion battery compared to an LDO's regulated output. These LDOs are required to have very low noise, low quiescent currents and occupy little chip space. A low dropout voltage is necessary as well for high efficiency. Power supply noise reduction and transient performance are also crucial since the regulator may be supplying power to sensitive Radio Frequency and analog blocks.

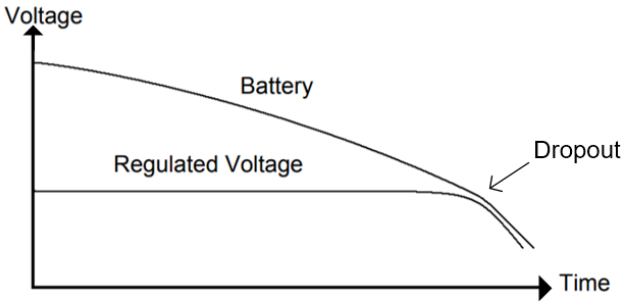


Figure 1.2: Discharge Profile of Typical Battery

1.1.2 Industrial and Automotive

Power management is a pivotal aspect in the nascent electric car industry. Apart from meeting strict industrial standards, these LDOs must have very high input voltage (up to 60V) in order to interface with car batteries and very good load transient capability. LDOs used for industrial applications should be able to handle large voltage and current transients and withstand process-voltage-temperature (PVT) variations.

1.1.3 Communications

LDO's are used in wireless communications and other networking equipment. These LDOs must provide clean power over a wide input and output voltage range. They must have high supple ripple rejection and ultra-low noise output in order not to degrade performance metrics such as signal-to-noise ratio (SNR), and jitter. Low power consumption is also required.

1.2 LINEAR REGULATOR BASICS

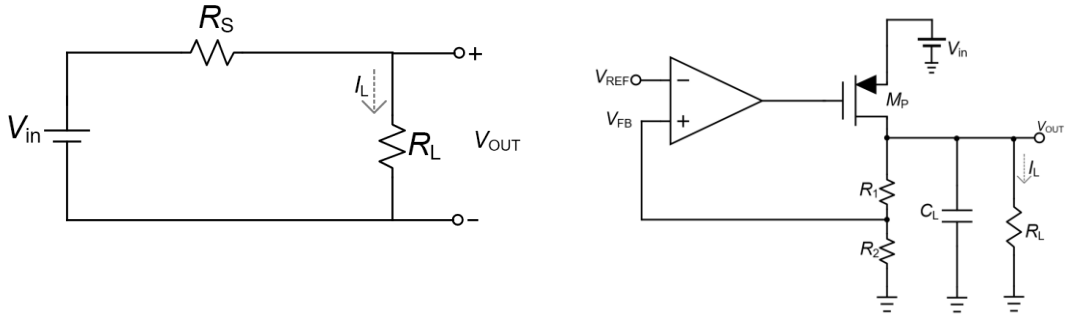
The most basic form of a linear regulator is a simple resistive divider as shown in figure 1.3a. With this arrangement, the output voltage, V_o is fixed for a given input voltage and is given by

$$V_o = \frac{R_L}{R_S + R_L} \cdot V_{in} \tag{1.1}$$

As can be seen from equation (1.1), the output voltage depends only on the voltage at the input and the ratio of resistors which is fixed. A change in load current will mean a corresponding change in input voltage which is not feasible because the goal is to provide a regulated output.

Another option will be to replace R_S with a variable resistor so that it can be varied based on the load current or input voltage to give as a constant regulated output voltage. We will need a device whose resistance can be controlled with a third terminal in order to regulate output current and therefore output voltage. A transistor fits this description perfectly. It could be a bipolar junction transistor (BJT) which is current controlled or a metal oxide semiconductor field effect transistor (MOSFET) which is voltage controlled. The transistor can be used in place of a variable resistor. Also, some sort of feedback has to be introduced to modulate the voltage or current controlled device when circuit conditions change. An operational amplifier with one input from the output (to sense the output voltage or current) and the other input from a stable reference is used to implement the negative feedback. A possible arrangement is shown in figure

1.3b and this is known as the low dropout regulator. The capacitor C_L is represents capacitance of the load.



a) b)

Figure 1.3: Linear Regulation a) Simple Linear Regulator b) Low Dropout Regulator

For an ideal op amp, gain is infinite and differential input is 0.

$$V_{FB} - V_{REF} \cong 0 \tag{1.2}$$

$$\left(\frac{R_2}{R_1 + R_2}\right) V_{OUT} - V_{REF} \cong 0 \tag{1.3}$$

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) V_{REF} \tag{1.4}$$

By choosing a resistive ratio and reference, we can obtain an output voltage. Granted that the operational amplifier has a high enough gain, we expect equation 1.4 to hold and thereby regulation to be maintained.

1.3 BASIC STRUCTURE/ BUILDING BLOCKS

In this section, the various components that make up a typical LDO regulator are discussed.

1.3.1 Error Amplifier

The error amplifier is the core of the regulator. It maintains regulation by comparing the voltage levels at its input and controlling the gate voltage of the pass transistor accordingly. It is usually designed as an operational amplifier with two or three stages. The error amplifier determines almost all the performance specifications of the LDO making its design very crucial. Some form of compensation must be employed in the error amplifier to guarantee LDO stability under different load conditions. The bandwidth also directly affects the transient performance of the LDO. Low bias current, low offset and high DC gain are also desirable characteristics of a good operational amplifier.

1.3.2 Pass Transistor

The pass transistor controls the current that is fed to the load. Its gate is controlled by the error amplifier. Pass transistors are usually very large (size of about $5000\mu/1\mu$). This is to reduce the on resistance (which is explained later in this work) to ensure a low dropout voltage. Large sizes for the pass transistor also affect AC and transient performance. These concepts are explained later in this work.

1.3.3 Resistive Divider

The resistive divider is usually made up of two resistors in series connected to the output. In a way, it level shifts the output voltage and provides a voltage that can be compared to to voltage reference at the inputs of the error amplifier. The feedback factor directly affects the loop gain and a higher value is desired for good power supply noise rejection. Most designs use a feedback factor of 0.5 (when the two resistors are equal).

1.3.4 Voltage Reference

The error amplifier in the LDO needs voltage reference to compare the output voltage to in order to maintain regulation. Most voltage references are provided by bandgap circuits. Bandgap circuits use complementary properties of semiconductor material to provide a voltage that is fairly constant under varying temperatures. A bandgap circuit was not designed in this work.

1.4 LDO TOPOLOGIES

LDOs can be identified by which kind of pass element is used. Figure 1.4 shows various configurations. The pass element may be a bipolar junction transistor or a MOSFET. The BJT is a current driven device while the MOSFET is voltage driven. BJTs deliver higher output currents than MOSFETs for a given supply voltage. The current capability can even be increased by cascading to BJTs to boost current gain. This configuration is known as the Darlington pair. Its drawback is that it requires a higher

dropout voltage. MOSFET pass elements are more popular as they allow for lower dropout voltage and quiescent current. MOSFETs are also easier to match during layouts.

Between PMOS and NMOS pass elements, PMOS pass elements are used more commonly. Using the PMOS pass elements allows for a higher output impedance. Also PMOS devices require a gate voltage which is lower than the input voltage. For NMOS devices, the required gate voltage should be higher than the output voltage. Generating this signal may not be feasible in low voltage applications[9]. In most cases, additional circuitry such as a charge pump is required to provide this signal as it may be higher than the input voltage. This reduces the compactness and overall efficiency. NMOS pass elements however have lower on resistance and therefore lower dropout voltages and higher current capability.

Digital LDOs have found a niche in applications that require very low supply voltages (below 0.5V) [10]. The operational amplifiers in analog LDOs cannot operate in such low voltage conditions and are therefore not suitable. In digital LDOs, the operational amplifier is usually replaced with a low voltage comparator the pass transistor with an array of switches. In addition to consuming very little quiescent current, digital LDOs are compact, easily synthesizable and very scalable. Digital LDOs however respond very slowly to load steps and have stability issues [11]. They also have low power supply ripple rejection. They are therefore not suitable for sensitive applications. There is a lot of ongoing research into hybrid LDOs, which combine features from analog and digital LDOs.

The LDO presented in this work can be considered as a hybrid. Its core is analog but has some elements of digital control.

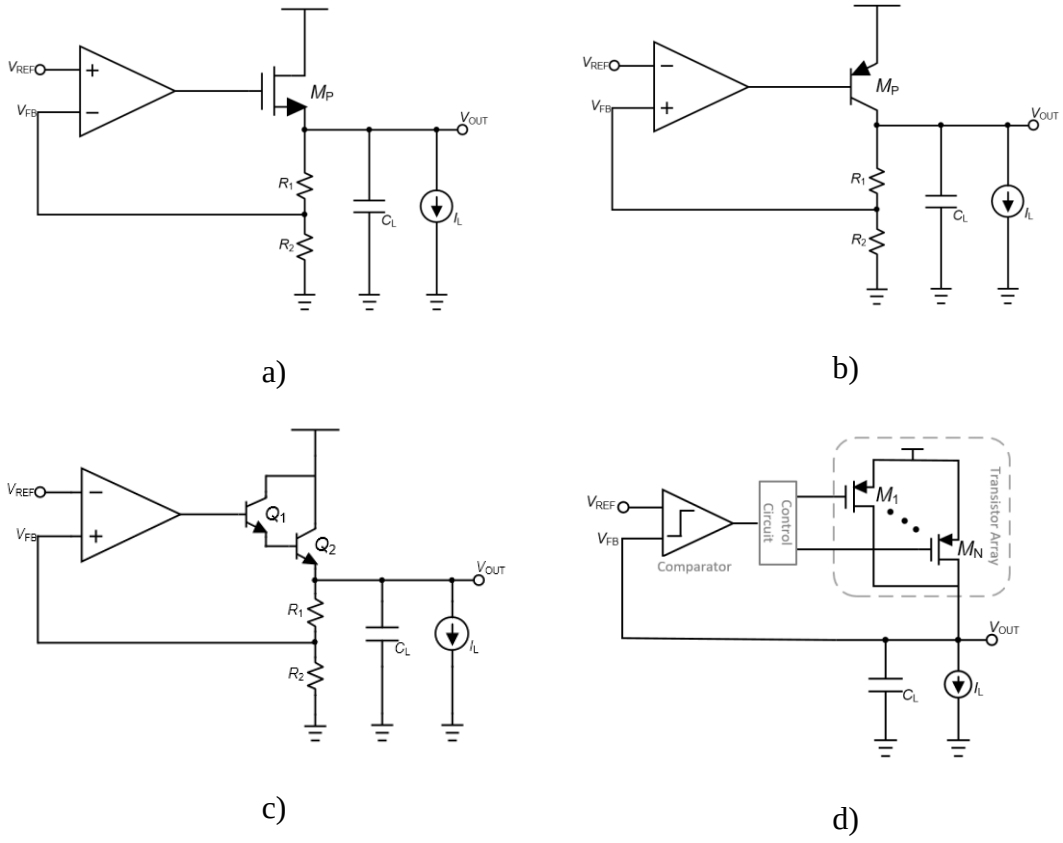


Figure 1.4: Linear Regulator Topologies a) NMOS LDO b) PNP LDO c) Darlington Pair LDO d) Digital LDO

Table 1.1 shows the comparisons and performance tradeoffs for each of the pass transistor configurations.

Specification	**PMOS**	**NMOS**	**NPN**	**PNP**	**Darlington Pair**
$I_{L,max}$	Medium	Medium	High	High	High
$I_{queiscent}$	Low	Low	Medium	Large	Medium
$V_{dropout}$	V_{sat}	$V_{sat} + Vgs$	$V_{sat} + V_{be}$	V_{sat}	$V_{sat} + 2V_{be}$
$Speed$	Medium	Medium	Fast	Slow	Fast

Table 1.1: Pass Transistor Configuration Comparison

1.5 LDO CHARACTERIZATION

LDO regulator performance is measured with certain metrics and specifications that designers work towards meeting. This section looks at the commonest LDO regulator specifications. These metrics are applicable to the various categories of LDO regulators but equations provided here are in the context of a PMOS LDO for simplicity and relevance to the work being presented.

1.5.1 Line Regulation

Line regulation indicates how much the output voltage changes with a given input voltage change. It is obtained by calculating the difference in steady state values of the output voltage and dividing by the change in input voltage. For an LDO with error amplifier gain, A_{EA}, feedback factor β, the line regulation can be approximated by equation 1.5.

$$\frac{\Delta V_{OUT}}{\Delta V_{IN}} \cong \frac{1}{A_{EA}\beta} \tag{1.5}$$

The line regulation is inversely proportional to the loop gain, $A_{EA}\beta$. A higher the loop gain leads to an improved line regulation performance.

1.5.2 Load Regulation

Load regulation indicates the variation at output with a change in the load current, measured in steady state. It measures the LDOs ability to maintain its output voltage with different loads. For an LDO with error amplifier gain, A_{EA}, feedback factor β, and pass transistor output impedance, R_{out}, the load regulation can be approximated by equation 1.6.

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} \cong \frac{R_{out}}{1 + A_{EA}\beta} \tag{1.6}$$

It can be seen that the load regulation improves with a smaller output resistance and larger loop gain.

1.5.3 Dropout Voltage

The dropout voltage, V_{do} indicates the smallest potential difference between the input and output that the regulator needs to maintain regulation. As the LDO approaches the dropout voltage, the pass transistor goes into the triode region. In triode region, there is a resistance between the source and drain of the pass transistor, known as the on resistance, R_{ON} which is inversely proportional to the aspect ratio of the pass transistor as shown in equation 1.7.

$$R_{ON} = \frac{1}{\mu_p C_{ox}(\frac{W}{L})(V_{gs} - V_{th})} \tag{1.7}$$

where μ_p is hole mobility, C_{ox} is oxide thickness of the oxide and $\frac{W}{L}$ is the aspect ratio of the transistor, V_{gs} is the gate-source voltage and V_{th} is the threshold voltage of the transistor.

Dropout voltage depends heavily on the on resistance of the pass device and sets the limit on the maximum load current. For modern designs, dropout voltage is between 200mV – 500mV.

The dropout voltage relates to the on resistance and load current as follows

$$V_{do} = I_{load} \times R_{ON} \tag{1.8}$$

1.5.4 Efficiency

The efficiency of the LDO depends mainly on the dropout voltage and quiescent current. The quiescent current, I_q is the current consumed by the regulator under no load conditions. It is the bias current needed to maintain the operation of the components such as the voltage reference, error amplifier, and resistive divider in the regulator.

The efficiency of the LDO can be expressed as

$$\rho = \frac{I_{load} V_o}{(I_{load} + I_q) V_{in}} \times 100 \tag{1.9}$$

1.5.5 Noise

The major sources of noise in LDO regulators are flicker noise from the input pair and thermal noise from the resistor in the divider. Noise is critical if the LDO feeds sensitive blocks such as radio frequency (RF) transceivers and voltage controlled oscillators (VCOs). Increasing the size of the input differential pair reduces the amount of flicker noise they generate. Also PMOS transistors generally have lower flicker noise than NMOS transistors [12]. Reducing the size of the resistors in the resistive divider reduces their noise contribution but increases quiescent current.

1.5.6 Power Supply Rejection (PSR)

PSR is the ability of the LDO regulator to reduce ripple from the input to its output. It is basically a measure of the amount of input ripple that is propagated to the output. PSR is similar to line regulation but PSR deals with high frequencies while line regulation is at DC. PSR is usually expressed as a ratio (known as PSRR) and is given by the expression in equation 1.10.

$$PSRR = 20\log\frac{V_{out,ripple}}{V_{in,ripple}} \tag{1.10}$$

The PSR can be improved by designing for a large loop gain and minimizing the size of the resistive ladder.

1.5.7 Transient Response (Settling Time and Ripple)

The response of the regulator to any change in the load current or input voltage is known as its transient response. Transient response is usually described in terms of the

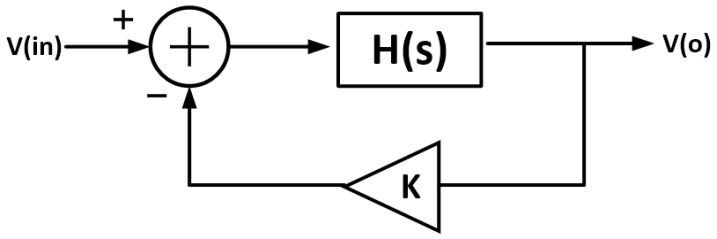
extent of variation from the specified output voltage (ripple) and how long it takes to reach steady state (settling time). It is desirable that a regulator exhibits very low output voltage ripple (overshoots and undershoots) and settle fast during transients. Transient responses are measured for low transients and line transients. The line transient is the response of the regulator when the input voltage is stepped. This is not very crucial as the supply to the LDO is often pre-regulated from a switching power supply or charge pump. The load transient, which occurs when the load current is stepped is much more critical since the current requirements of loads change often in circuits. For example, during start up and shut down of devices high amounts of currents are suddenly demanded or cut off. It is important to ensure that the power supply to the load (which are often sub circuits in a system) be stabilized before they begin to operate. Transient response of regulators is addressed in detail later as this is the main focus of this work.

2 CONVENTIONAL AND CAPACITOR-LESS LDO REGULATORS

In this section, the conventional and capacitor-less LDOs are introduced. The design considerations for each type are discussed.

2.1 AC STABILITY

AC stability is of utmost importance and it must be considered in designing every part of a voltage regulator. LDO regulators uses feedback mechanism to maintain a constant output voltage therefore stability needs to be considered during design[13]. As in all, feedback systems, Barkhausen's Criteria need to be satisfied to prevent the system from oscillating[14]. The phase shift around the loop should not exceed 180 while the loop gain is greater than unity. Figure 2.1 shows a typical feedback system.

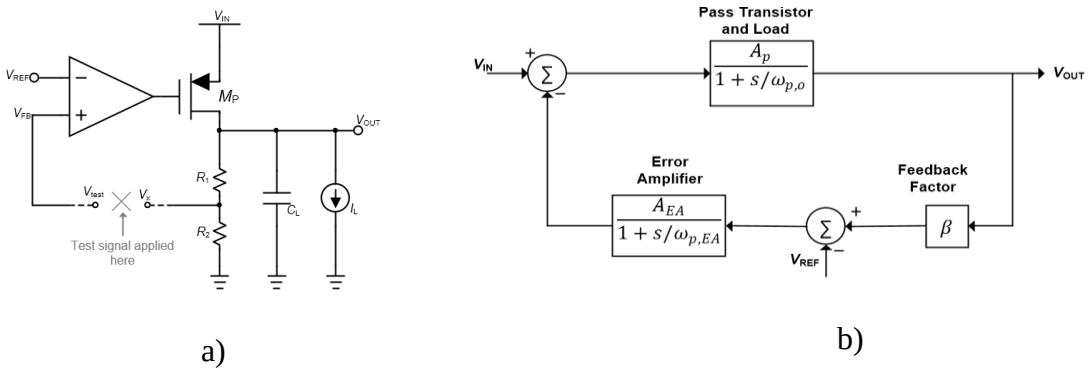


$$|KH(j\omega)| < 1 \qquad (2.1)$$

$$\angle KH(j\omega) = -180 \qquad (2.2)$$

Figure 2.1: Typical Feedback System

Since the LDO is a closed loop system, loop gain, gain bandwidth product and phase margins need to be considered. A high open loop gain optimizes load and line regulation. Bandwidth dictates the settling time of the system. These two specifications are a direct tradeoff of each other, and precedence must be given to one based on the application of the LDO. A phase margin of less than 45 will lead to instability and subsequently, oscillations which will not cause the output to settle. To simulate for open loop gain, the LDO loop is broken off at point X shown in figure 2.2a and the AC test signal is applied.



a) b)

Figure 2.2: LDO Stability Analysis a) Setup for Loop Gain b) LDO Small Signal Model

Figure 2.2b shows a small signal model of the LDO that can be used to study analyzing stability. It can be seen that the system is a negative feedback system. The signals V_{IN}, V_{REF}, and V_{OUT} are the input, reference and output voltages. The feedback factor, β is given by

$$\beta = \frac{R_2}{R_1 + R_2} \tag{2.3}$$

From figure 2.2b the transfer function can is given by equation 2.4.

$$A_{CL} = \frac{\left(\frac{A_p}{1 + s/\omega_{p,o}}\right)}{1 + \beta\left(\left(\frac{A_{EA}}{1 + s/\omega_{p,EA}}\right)\left(\frac{A_p}{1 + s/\omega_{p,o}}\right)\right)} \tag{2.4}$$

A_p represents the DC gain of the pass transistor and $\omega_{p,o}$ is the pole associated with the output of the LDO. The transfer function of the error amplifier is modelled by its DC gain, A_{EA} and a pole located at $\omega_{p,EA}$. In this example, the amplifier is a single stage and therefore has only one pole formed by the interaction of its output impedance and the pass transistor gate capacitance. Most error amplifier designs use a higher number of stages for higher gain and therefore have more poles.The loop gain can be extracted from equation (2.4) and given as

$$A_{OL} = \frac{V_X}{V_{test}} = \frac{\beta A_{EA} \cdot A_p}{(1 + s/\omega_{p,EA})(1 + s/\omega_{p,o})} \tag{2.5}$$

It can be seen from equation (2.5) that the system has two poles which makes it likely to be unstable. Most designs compensate for this by adding a zero to boost phase. Increasing the error amplifier and pass transistor DC gain maximizes the loop gain. As has been stated earlier, a high loop gain is essential for obtaining good load/line regulation and PSR performance. The feedback factor should also be taken into consideration as it directly proportional to the loop gain.

2.1.1 Conventional LDO Stability

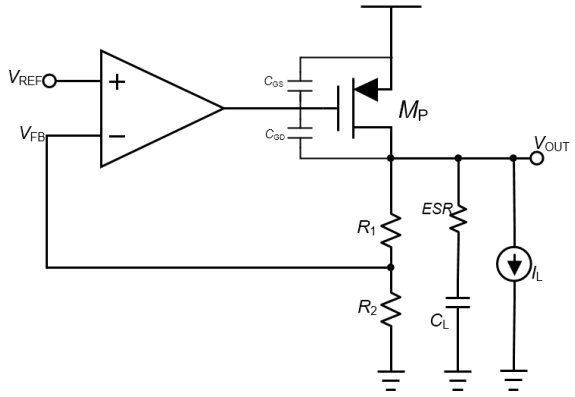


Figure 2.3: Conventional LDO (With Off-Chip Capacitor)

The schematic of a conventional LDO shown in figure 2.3 shows a. The large off-chip capacitor, C_L together with the output impedance of the pass transistor forms the dominant pole, ω_1 at the regulator output. The second pole, ω_2 is located at the error amplifier output node. In order to compensate the system, designers take advantage of the zero, ω_z created by the equivalent series resistance (ESR) of the output capacitor. The zero boosts the phase and should be placed before the unity gain frequency (UGF) to improve phase margin. The ESR is very important and it must be considered when selecting the output capacitor. Ceramic capacitors generally have lower ESR values than electrolytic capacitors. Also, a small resistor can be placed in series with the output capacitor to act as its ESR. The expression for the poles and zeros are given in equations (2.6-2.8)

$$\omega_1 \cong \frac{1}{[R_o||(R_1+R_2)]\,C_L} \tag{2.6}$$

$$\omega_2 = \frac{1}{(C_{GS}+(A_P+1)C_{GD})\cdot R_{EA}} \tag{2.7}$$

$$\omega_z = \frac{1}{C_L R_{ESR}} \tag{2.8}$$

where A_P is the pass transistor gain, R_o is the output impedance of the pass transistor, C_L is the load capacitance, C_{GD} and C_{GS} represent the gate-drain and gate-source capacitances respectively and R_{EA} is the output resistance of the error amplifier.

It must also be noted that the error amplifier may introduce a third pole

$$\omega_3 = \frac{1}{C_i R_i} \tag{2.9}$$

where C_i and R_i are internal node capacitance and resistance respectively. This pole is usually located at high frequencies and designed to be below the unity gain frequency[15]. The pole does not affect stability in low to moderate load conditions. However, in high load conditions, the dominant pole shifts to a higher frequency because of decrease in the output impedance of the pass transistor. This causes an increase in the UGF which can lead to instability as shown in figure 2.4.

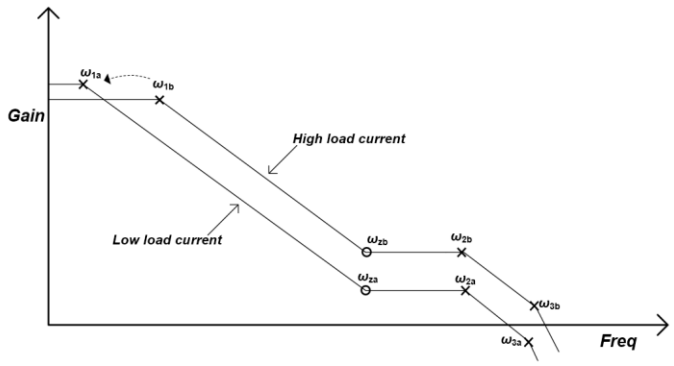


Figure 2.4: Conventional LDO Stability

2.1.2 Capacitor-less LDO Stability

Without the large output capacitor, most designers set the dominant pole at the gate of the pass transistor at node 1. The pole at the output becomes the second pole. Most error amplifiers are designed to have at least one pole, mostly located at high frequencies and so don't interfere too much with stability. The pole at ω_1 is formed by the output impedance of the error amplifier and the gate capacitance of the pass transistor. The C_{GS} of the pass transistor, as has been stated earlier, is huge because of the large aspect ratio of the pass transistor. The gate drain capacitance, C_{GD} is also amplified by the gain of the pass transistor by Miller effect. The location of the pole can be given by

$$\omega_1 = \frac{1}{(C_{GS} + (A_P + 1)C_{GD}) \cdot R_{EA}} \tag{2.10}$$

where A_P is the gain of the pass transistor, R_{EA} is the output impedance of the error amplifier

The second pole is given by

$$\omega_2 \cong \frac{1}{(R_o||(R_1+R_2))C_o} \tag{2.11}$$

where $R_o$is the output impedance of the pass transistor, and C_o is the load capacitance The transconductance of the pass transistor gm_p is dependent on the load current, I_o by the relationship shown in equation (2.12).

$$gm_p = \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)I_o} \tag{2.12}$$

where μ_p is the mobility, C_{ox} is the thickness of the oxide and $\frac{W}{L}$ is the aspect ratio of the transistor. This causes ω_1 to vary with load. The output impedance term, R_o in equation (2.11) also varies with load current and the relationship is shown in equation (2.13).

$$R_o = \frac{1}{\lambda I_o} \tag{2.13}$$

where λ is the channel length modulation coefficient.

As can be seen ω_2 is more sensitive to load current[16]. At low loads, the impedance of the pass transistor increases, causing the location of ω_2 to move lower and towards ω_1. This causes a sharp phase drop which leads to instability. Therefore, the worst case stability condition occurs at no load. Figure 2.5 shows an AC gain plot of an uncompensated capacitor-less LDO.

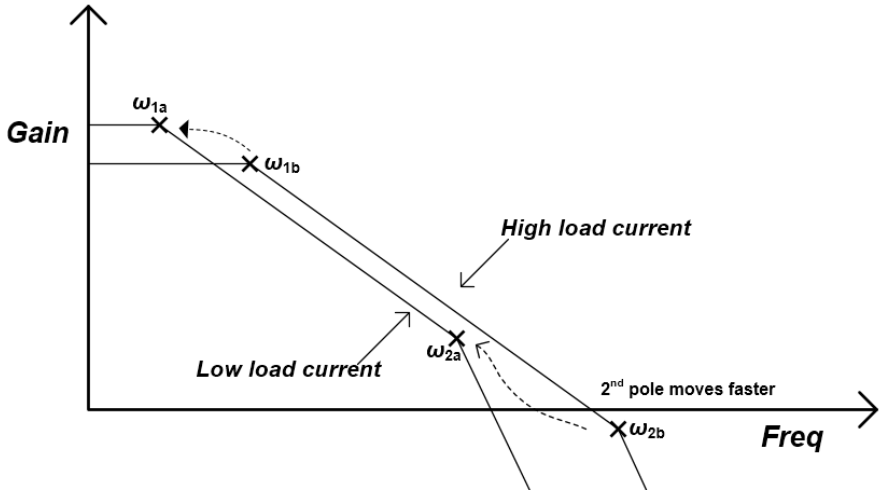


Figure 2.5: Capacitor-less LDO AC Stability

A popular way of compensating for capacitor-less LDOs is to place the dominant pole at the output of the first stage of a two-stage amplifier. This pole will be at a much lower frequency but is less dependent on load current. In this case, the whole LDO can be modeled as a three stage amplifier with the pass transistor being the third stage. The loop gain of such a system can be given as

$$A_L = \frac{\beta A_{EA} A_P}{\left(1 + \frac{s}{\omega_{p1}}\right)(s^2 + \frac{s\omega_o}{Q} + \omega_o^2)} \tag{2.14}$$

The first pole given by ω_{p1} and the two non-dominant poles are modeled as a biquad with natural frequency, ω_o and quality factor, Q [16]. These two poles are located at the output node and the gate of the pass transistor and must be placed above the unity gain frequency to ensure stability. The quality factor is related to the load current and pass transistor transconductance, g_{mp} by the equations (2.15) and (2.16) respectively.

$$Q \approx 1/\sqrt[4]{I_L} \tag{2.15}$$

$$Q = 1/\sqrt{g_{mp}} \tag{2.16}$$

As can be seen. The low load currents cause the two dominant poles to become a complex conjugate pair thereby increasing the Q. A high quality factor causes a sharp drop in phase leading to instability. A solution to this is proposed later in this work.

2.2 TRANSIENT RESPONSE OF LDOS

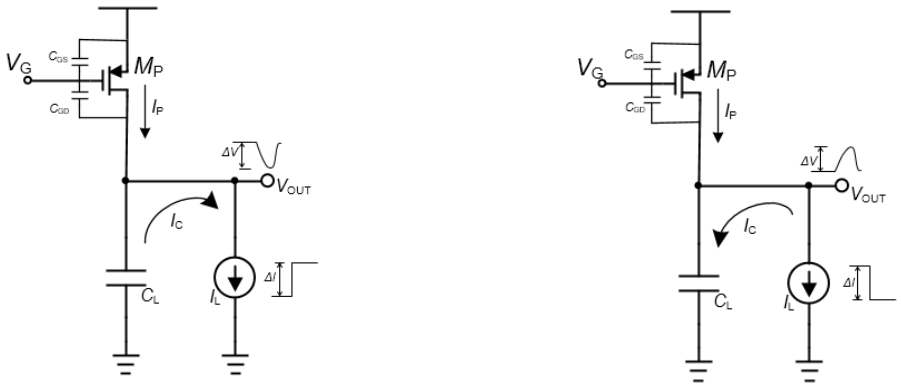
Transient response of LDOs is a very important specification which is measured in terms of how much variation is seen at the output and how long it takes for the output to reach a percentage of its steady state value after a load step is applied. Analog circuits such as those used in receivers, transceivers and VCOs are very sensitive to noise. Even though digital circuits typically have large noise margins, switching in between states requires large immediate current demands. This can lead to severe glitches and ultimately system failure[17]. The use of multilevel states for higher data rates even reduces the noise margin further, making digital circuits less robust against noise. The settling time of an LDO can also affect the start-up time of a whole system.

2.2.1 Formation of Undershoot and Overshoot

In the event of a large increase in load current, because of the LDO loop bandwidth limitations, the current supplied by the pass transistor cannot be adjusted fast enough to meet the demand. The output capacitor supplies the current needed during this

time. This causes a sharp drop in the voltage across the capacitor leading to a large undershoot. This is illustrated in figure 2.6a.

Similarly, in the case of a large step in load to a lower current, the pass transistor continues to supply large amounts of current in excess of the load current. The excess current is absorbed by the output capacitor and this causes the voltage across it to rise sharply, leading to an overshoot in output voltage. This is illustrated in figure 2.6b.



a) b)

Figure 2.6: Voltage Spike Formation a) Undershoot b) Overshoot

In both cases, the voltage variation, ΔV seen at the output is inversely related to the size of the capacitor as shown in equation 2.17 where Δt is the response time of the loop and I_L is the load current demand.

$$\Delta V = \frac{I_L}{C_L}\Delta t \tag{2.17}$$

The coefficient of $\Delta t, \frac{I}{C_L}$ is known as the charging/discharging rate and it determines the how sharp the voltage rises or falls.

A closer look at a typical LDO voltage ripple in figure 2.7 shows an initial region of constant slope. In this region, the output capacitor supplies all the current. The output voltage begins to move down with a slope given by $^{I}/_{C_L}$. The slope becomes less steep at point X. After this point, the pass transistor begins to supply some current but this is not enough to meet the load demand. This continues till point Y when pass transistor current equals the load demand. The capacitor stops discharging and the voltage begins to move back to its nominal value. The time taken for the loop to respond fully to load step, t_1 depends mainly on the closed loop bandwidth of the system and the slew rate of the pass transistor gate as shown in equation (2.18).

$$t_1 \approx \frac{1}{BW} + C_p \frac{\Delta V_p}{I_{sr}} \tag{2.18}$$

where BW is the closed loop bandwidth of the LDO, C_p is the lumped capacitance at the pass transistor gate, ΔV_p is the voltage variation at the pass transistor gate in response to the transient event and I_{sr} is the slew rate at the pass transistor gate

In general, for capacitor-less LDO regulators, the length of this period depends mainly on the slew rate of the pass transistor gate[18]. This is because C_p is typically large and I_{sr} is ideally kept low by design to reduce quiescent current. Typically, the voltage will oscillate around the stead state value and finally settle. The number of oscillations and settling time, t_2 is determined by the phase margin of the system's open loop frequency

response. The load step down ripple ΔV_2 is usually dominated by bandwidth and is given by equation 2.19.

$$\Delta V_2 \approx \frac{I_{max}}{C_L} \cdot \frac{1}{BW} \tag{2.19}$$

As observed in figure 2.7, the overshoot/undershoot response is often asymmetrical. This is mainly due to the differences in the pull-up/ pull-down slew rate which is from the output stage used in the error amplifier. A push pull output stage which is employed in this work is better for a symmetrical response.

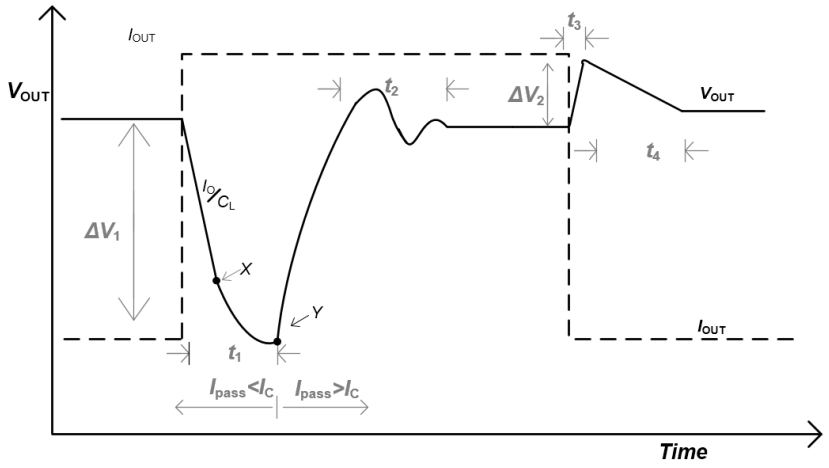


Figure 2.7: Up-close View of Undershoot and Overshoot

2.3 EXISTING SOLUTIONS

Various solutions have been proposed to improve the transient response of output capacitor-less LDOs. The approaches can be grouped into three main categories.

2.3.1 Using High Slew Rate Error Amplifiers

Designs such as [19] and [20] employ high slew rate error amplifiers for rapid charge/discharge of the parasitic capacitance of the pass transistor. A high slew rate at the pass transistor gate ensures that the node is moved in the right direction quickly in order to react to transients. In [19], common mode feedback is used to enhance the slew rate at the output. The drawback of using high slew rate amplifiers is that such amplifiers require high quiescent currents and the currents provided may not be high enough to effectively reduce the ripple.

2.3.2 Adaptive or Dynamic Biasing

Adaptive biasing is also a common approach to improving the transient performance. With such designs as in [21], the load current may be sensed and used to control the tail current of the input differential pair of the error amplifier. The design in [22] uses two comparators to adaptively bias the error amplifier after an overshoot/undershoot is sensed. The work in [23] uses dynamic biasing. The transient at the output is detected and amplified. The amplified signal is then fed into the bias-boosting circuitry which increases the tail current of the input differential pair thereby increasing the bandwidth during the transient. Even though this method addresses the problem of low bandwidth, it leaves out the slew boosting the gate of the pass transistor. This method has been tried with some success but it does not provide enough current drive for drastic load transients. Also there is still a reliance on the main LDO loop which may not be as fast as desired.

2.3.3 Slew-Boosting the Pass Transistor Gate

In view of this, there are a number of designs that have a spike detection circuit and a slew boosting circuit. Detection circuits are usually made of high pass filters or differentiators and most designs such as in [24-26] use an RC network to implement these. In these designs, the spike is sensed as a current in the capacitor. The size of the capacitor determines the magnitude of the current. This current must then be processes somehow by the slew boosting circuit to compensate for the spike. Designs in [24] and [27] use current mirrors to steer and provide the charge/ discharge current. The low impedance at the gate of the current mirror attenuates the current signal when it is being converted to voltage and may not be the best solution as fast spike detection is vital. The work in [24] employs this scheme. Owing to size of the gate node capacitance of the pass transistor and the speed of the transients, a good design must contain a circuit that detects the spike quickly and is able react independent of the main LDO loop, providing large currents to boost slewing at the pass transistor gate node.

3 PROPOSED SOLUTION

In this chapter, the proposed design is presented. A detailed description is given followed by the principle of operation and the design methodology.

3.1 OVERVIEW

The proposed design seeks to address the two main tradeoffs encountered in capacitor-less LDO regulators. As mentioned earlier, removing the output capacitor leads to ac stability issues especially at low loads and degradation in transient response. The major approach taken in the proposed solution is illustrated in figure 3.1. The deviation from the output voltage is detected as an error signal. This signal is then compared to a preset threshold voltage. If the level of the error is higher than the threshold, a mechanism is employed to correct this error. This forms an external loop which is designed to be faster than the main LDO loop.

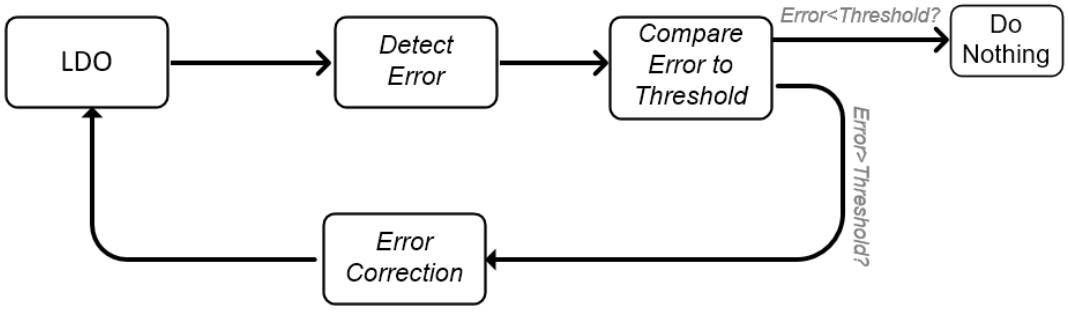


Figure 3.1: Concept of Proposed Design

A schematic representation of the design is shown in figure 3.2. The main highlights of the design are

- Bang-bang technique to improve the transient response.
- Q-reduction technique used in the error amplifier to improve AC stability

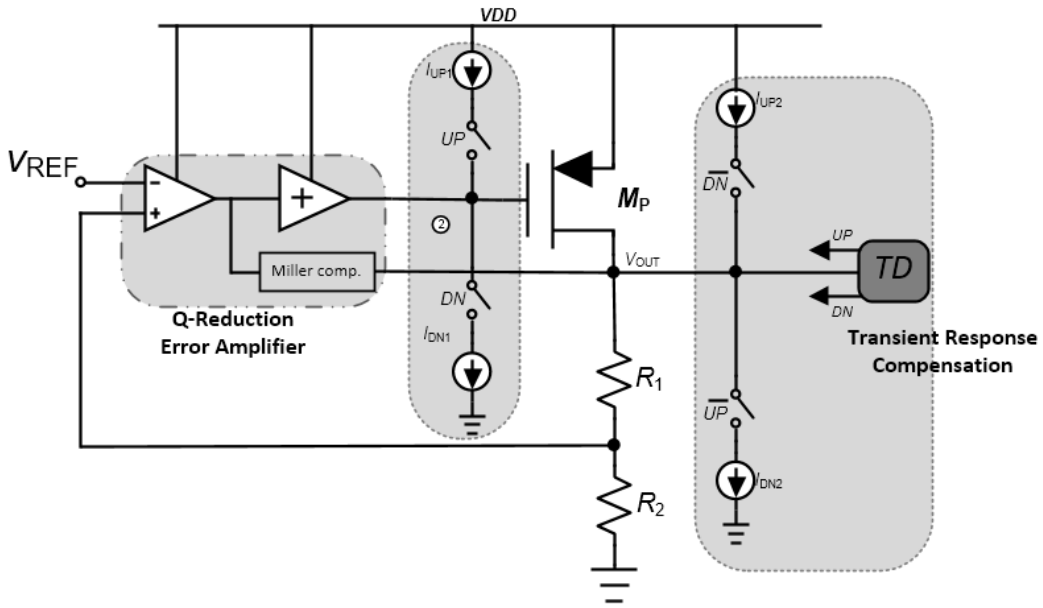


Figure 3.2: Proposed Design

3.1.1 Bang-Bang Technique

In order to reduce output voltage ripple and settling time during load transients, the error amplifier must be able to respond quickly enough, moving the gate of the pass transistor in the right direction in order to supply more current (in the event of a step up in load) or cut the supply current (in the event of a step down in load). The difficulty

here is that the lumped gate capacitance (C_{gd}, C_{gs}) associated with most pass transistors are huge because the transistor size is inversely related to the dropout voltage. Furthermore, the typical error amplifier is not able to provide enough current at its output stage to quickly charge/ discharge the gate of the pass transistor. The proposed design introduces an alternate loop that acts faster than the main loop and supplies more current to charge and discharge the pass transistor gate when there is a load transient. The loop is designed in such a way that it is only activated during transients and does not interfere the normal operation of the loop. In steady state conditions, the loop remains inactive and consumes very little current. The schematic diagram is shown in figure 3.2. It consists of the following

- Transient detector
- Decision Circuit
- Slew boosting circuit

3.1.1.1 Transient detector

The transient detector is the part which senses the changes in the output voltage. A schematic diagram is shown in figure 3.3. It is made up two passive first order high pass filters, (formed by R_1, C_1 and R_2, C_2) which connect to the output of the LDO regulator. The values of R_1, C_1, R_2 and C_2 are selected such that the circuits is very sensitive to transients and acts very quickly. The output of the high pass filters modulate the gates of the sense transistors $M_1 and\ M_2$ thereby turning them on or off. The sense transistors are biased with bias voltages $V_{b1}\ and\ V_{b2}$ so that in steady state conditions,

their gate to source voltages (V_{gs}) are just below their threshold (turn-on) voltages. The drains of the sense transistors (node V_{ctrl}) is connected to the one of the inputs of the comparators $CM1$ and $CM2$ in the decision circuit. In steady state, the voltage at node $V_{ctrl}$is set to the midrail value by the bias voltage V_{mid}. An overshoot causes the voltage to fall and an undershoot causes it to rise.

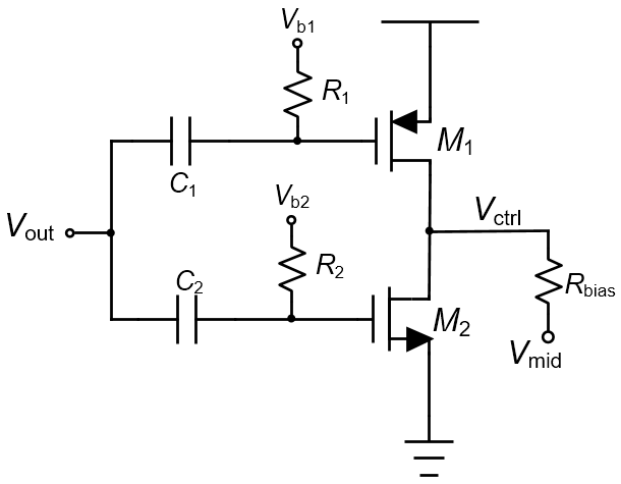
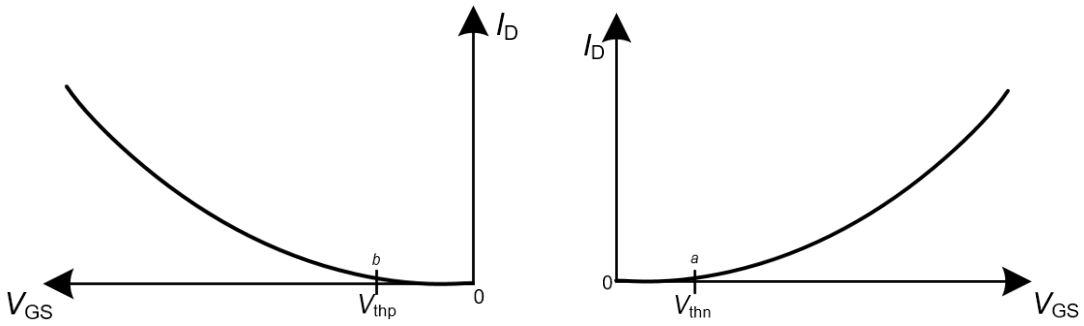


Figure 3.3: Transient Detector

Figure 3.4a shows the I-V characteristic of a pmos transistor. It also shows the point around which transistor M_1 is biased. Biasing at this point is ideal as very little bias current flows through the transistor.

Similarly, figure 3.4b shows the I-V characteristic of an nmos transistor. The sense transistor M_2 is biased around point a.



a) b)

Figure 3.4: MOSFET I-V characteristics a) PMOS b) NMOS

An undershoot causes current to flow from the high pass network into the output of the LDO. This causes the bias point in figure 3.4b to move towards the origin. There change in current is insignificant in this region and remains close to zero. However, it causes the bias point in figure 3.4a to move away from the origin as the gate-source voltage increases. The gate-source voltage of the pmos increases and this causes a large change in current in M_1 causing the voltage at node V_{ctrl} to move up.

An overshoot will cause current to flow into the capacitors, charging the parasitic capacitors at the gates of the sense transistors. This shifts the bias point in both figures 3.4a and 3.4b towards the right. The current in M_2 increases sharply while the current in M_1 stays close to zero. This causes the voltage at node V_{ctrl} to move down.

3.1.1.2 Decision Circuit

The next stage after the transient detector is the decision stage shown in figure 3.5. Here, the output of the transient detector stage is fed to one input of two

comparators CM_1 and CM_2. The second set of inputs are tied to two individual threshold voltages, V_{t1} and V_{t2}. These voltage levels are chosen such that CM_1 detects an upper threshold and CM_2 determines the lower threshold. The threshold voltage V_{t1} for CM_1 is chosen to be slightly above the midrail ($(V_{DD} - V_{SS})/2$) and V_{t2} is chosen to be slightly below the midrail value as shown in equations (3.1) and (3.2).

$$V_{t1} = V_{mid} + \Delta V \tag{3.1}$$

$$V_{t2} = V_{mid} - \Delta V \tag{3.2}$$

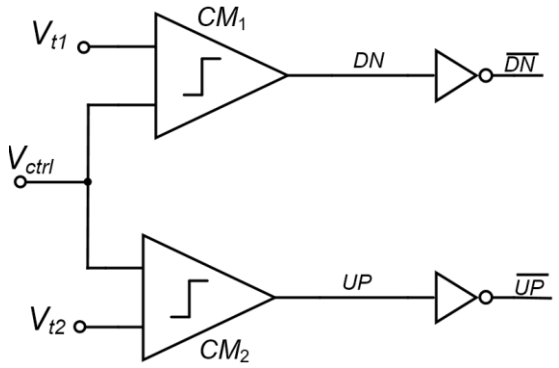


Figure 3.5: Decision Circuit

In the case of a voltage spike at the LDO regulator output, the voltage at V_{ctrl} moves lower/ higher than the midrail value and trips one of the comparators.
It must however be noted that the threshold voltages are chosen such that there is a voltage range around V_{mid}, where none of the comparators are tripped. This is discussed more in subsequent sections.

3.1.1.3 Slew boosting circuit

The slew boosting circuit is shown in figure 3.6. It is made up of current two sets of upper and lower current sources with switches in series with them. In steady state, all the switches are off. The upper current sources ($S_{2a}\ and\ S_{1b}$) supply current when their corresponding switches ($I_{2a}\ and\ I_{1b}$) are turned on by logic signals from the output of the comparators. In the same way, the lower current sources ($S_{1a}\ and\ S_{2b}$) sink current when the switches ($I_{1a}\ and\ I_{2b}$) are turned on. The current sources and sources and switches are set up similarly to a charge pump used in phase locked loops. The drains of the switches in branch A connect to the pass transistor gate and the drains of the switches in branch B are connected to the LDO regulator output.

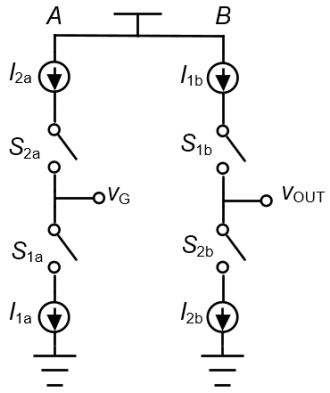


Figure 3.6: Slew Boosting Circuit

3.1.2 Modes of Operation

The transient compensation scheme can operate in three modes depending of the nature of the voltage spike at the LDO output. These are illustrated in figure 3.7.

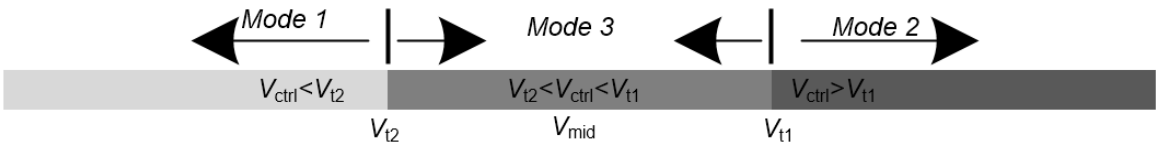


Figure 3.7: Modes of Operation

3.1.2.1 Mode 1 ($V_{ctrl}<V_{t2}$)

In the case of an overshoot, $Vout$ rises suddenly. This spike is picked up by the coupling capacitors $C_1 and\ C_2$. The gate-source voltage of M_2 rises and it conducts some current. This causes the voltage at node V_{ctrl} to move down and below V_{t2} and comparator CM_2 trips. Its output is applied to switches $S_{2a}\ and\ S_{2b}$. The output of comparator CM_1 remain unchanged and switches $S_{1b}\ and\ S_{1a}$ remain open. After S_{1a} turns on, current source I_{2a} supplies a large amount of current to the pass transistor gate, V_g, charging the large parasitic capacitor C_{gs}. This causes the gate voltage to rise, reducing the gate source voltage of the pass transistor. This causes a reduction in the current supplied by the pass transistor and thereby reducing the overshoot.

$$I_o - \Delta I = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[\left(V_{gs} - \Delta V\right) - V_{th}\right]^2 \tag{3.3}$$

The reduction in current can be extracted from equation 3.3 and given by

$$\Delta I \approx \mu_p C_{ox} \frac{W}{L}\left(V_{gs} - \frac{\Delta V}{2} - V_{th}\right)\Delta V \tag{3.4}$$

After switch S_{2b} is also turned on, the current source I_{2b} is connected directly to the output of the LDO and helps to sink excess current from the output. This further reduces the overshoot. This is illustrated in figure 3.8.

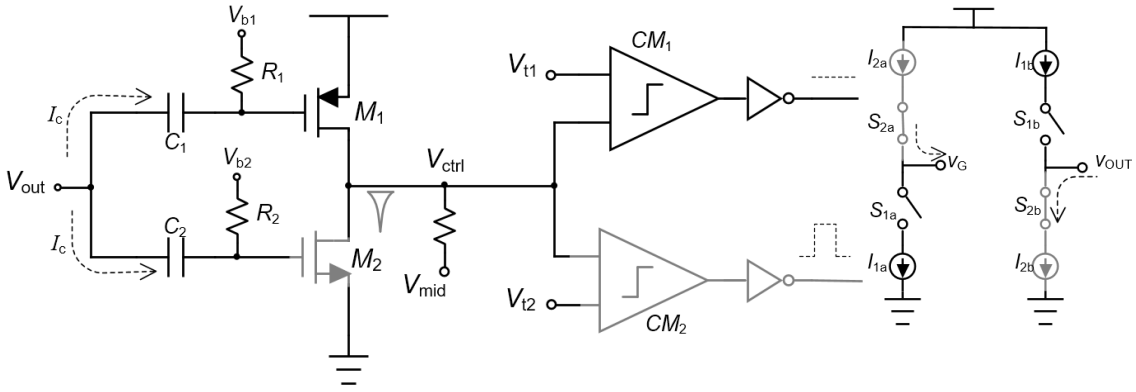


Figure 3.8: Mode 1 Operation

3.1.2.2 Mode 2 (V_{ctrl}>V_{t1})

In the case of an undershoot, M_1 picks up the spike and the node V_{ctrl} moves up and higher than V_{t1} and comparator CM_1 trips. Its output is applied to switches S_{1a} *and* S_{1b}. The output of comparator CM_2 remain unchanged and switches S_{2a} *and* S_{2b} remain open. After S_{1b}turns on, current source I_{1b} sinks a large amount of current from the gate of the pass transistor, discharging the large parasitic capacitor C_{gs}. This causes the gate voltage to rise, reducing the gate source voltage of the pass

transistor. This causes a reduction in the current supplied by the pass transistor and thereby reducing the overshoot. The rapid discharge of V_g pulls the gate of the pass transistor down to reduce the amount of overshoot.

$$I_o + \Delta I = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left[\left(V_{gs} + \Delta V\right) - V_{th}\right]^2 \tag{3.5}$$

The additional current can be extracted from equation 3.5 and given by

$$\Delta I \approx \mu_p C_{ox}\frac{W}{L}\left(V_{gs} - \frac{\Delta V}{2} - V_{th}\right)\Delta V \tag{3.6}$$

This is illustrated in figure 3.9.

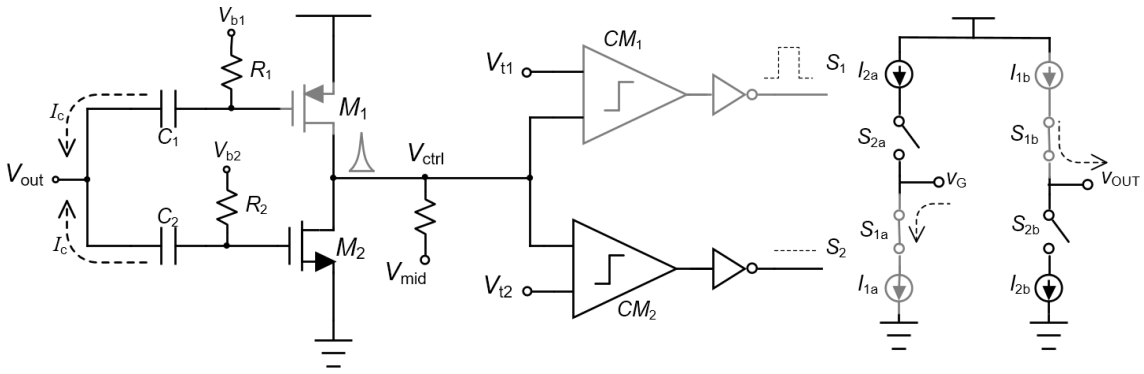


Figure 3.9: Mode 2 Operation

3.1.2.3 Mode 3 (V_{t2}<V_{ctrl}<V_{t1})

In this case, there could be an overshoot or undershoot that is picked up any of the two sensing transistors. The control voltage however does not exceed the threshold

value of the comparators. None of the comparators trips in this case and all the switches in the slew boosting circuit remain open. It is very necessary that this allowance is provided as it prevents unwanted tripping of the comparators.

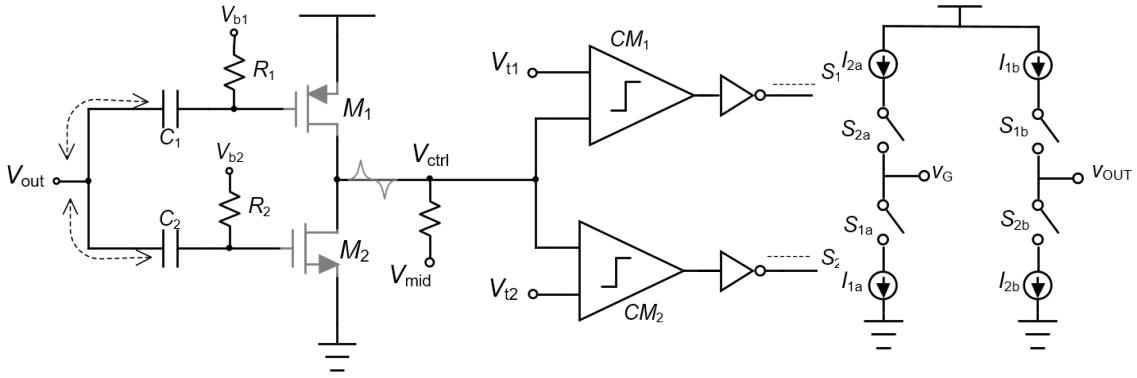


Figure 3.10: Mode 3 Operation

From the small signal point of view. The transient compensation scheme extends the bandwidth of the LDO regulator[28]. In this region, the spike is handled by the main loop. This is to make sure both the error amplifier and transient detection do not act together to overcompensate for the spike which can lead cause the system to have positive feedback and lead to oscillations. This is illustrated in figure 3.10

3.1.3 Error Amplifier

The error amplifier is the heart of the LDO and a good compensation scheme is necessary for decent transient and ac stability under varying load conditions. Figure 3.11

shows schematic of the proposed error amplifier. The proposed design is a two stage amplifier with a push-pull output stage. The first stage is a differential stage with active loads formed by $M_2 - M_5$. A PMOS input stage is chosen for lower noise[12]. The second stage is a common source amplifier stage (M_6, M_7) with its output fed into a current mirror formed by M_7, M_8. The slew rate is enhanced by the push-pull output stage. Also, a feedforward stage formed by $M_2, M_4\ and\ M_9$. The feedforward stage creates a low frequency zero to help with compensation. The dominant pole is placed at the first stage (node n1). The miller capacitor, C_1 together with the nulling resistor, R_1 also helps with pole splitting to improve stability.

Miller compensation is employed to improve stability and a nulling resistor is used to eliminate the associated right hand plane zero. Active capacitor multiplication is also employed in order to reduce the total compensation capacitance used.

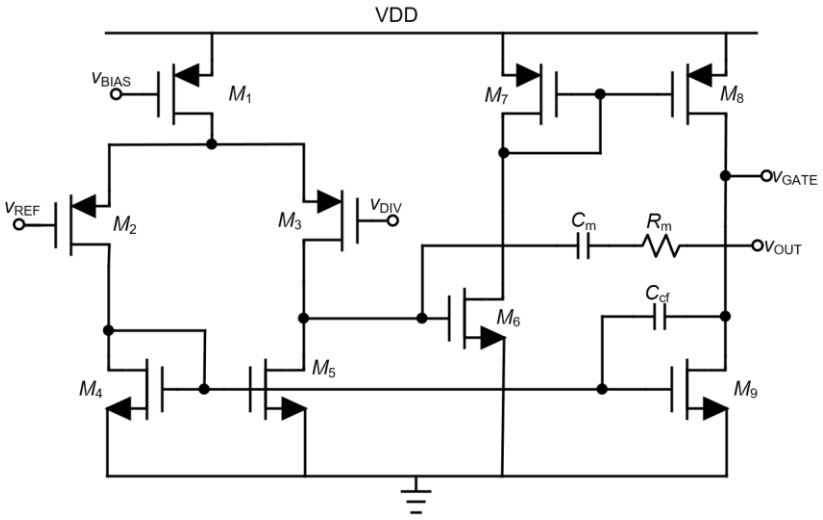
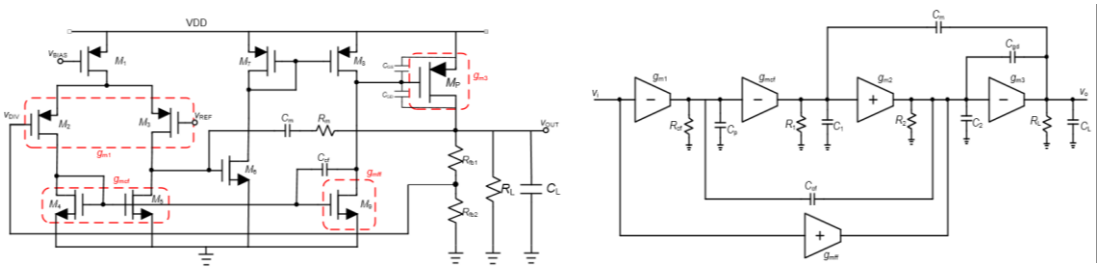


Figure 3.11: Proposed Error Amplifier

3.1.3.1 Stability Analysis

As has been discussed in section 2.1.2 during low to no load, the two non-dominant poles of the capacitor-less LDO move close to each other and this leads to a high quality factor, Q which causes a sharp drop in phase and consequently instability. The design implements a technique to reduce the Q at low loads by using a current buffer together with a capacitor.

A schematic of the LDO is shown in figure 3.12a and the open loop block diagram is shown in figure 3.12b. The feedback factor used in the analysis is 1 for simplicity.



a) b)

Figure 3.12: LDO stability a) LDO Schematic b) Open Loop Bock Diagram

gm_1 represents the transconductance of the first stage, gm_2 represents the transconductance of the second gain stage and gm_3 represents the transconductance of the pass transistor. gm_{cf} represents the transconductance of the current buffer. The current buffer is formed by M_4 and M_5. g_{mff} is the transconductance of the feedforward

stage. C_1, C_2 and R_1,R_2 are the lumped capacitances and resistances at output of the first and second stages respectively. R_{cf} is the input impedance of the current buffer C_L and R_L represents the lumped capacitance and resistance at the output node. The transfer function can be given as

$$A_{OL} \cong \frac{-g_{m1}g_{m2}g_{m3}R_1R_2R_L\left[1+s\left(C_{cf}R_{cf}+\frac{C_m g_{mff}}{g_{m1}g_{m2}}-\frac{C_{gd}}{g_{m3}}\right)-s^2\left(\frac{C_m(C_{gd}+C_2)}{g_{m2}g_{m3}}+\frac{C_{gd}C_{cf}R_{cf}}{g_{m3}}\right)\right]}{(1+sC_m g_{m2}g_{m3}R_1R_2R_L)\left[1+s\frac{C_mC_{gd}(g_{m3}-g_{m2})+C_{cf}C_Lg_{m2}+C_mC_{cf}g_{m2}g_{m3}R_{cf}}{C_mg_{m2}g_{m3}}+s^2\frac{(C_{gd}+C_2\,C_{cf})C_L}{g_{m2}g_{m3}}\right]} \quad (3.7)$$

For high loads, when gm_3 is large, equation 3.7 can be simplified as

$$A_{OL} \quad (3.8)$$

$$= \frac{-g_{m1}g_{m2}g_{m3}R_1R_2R_L\left(1+\frac{sC_m g_{mff}}{g_{m2}g_{m3}}\right)}{(1+sC_m g_{m2}g_{m3}R_1R_2R_L)\left[1+s\frac{(C_{gd}+C_{cf})}{g_{m2}}+s^2\frac{(C_{gd}+C_2+C_{cf})C_L}{g_{m2}g_{m3}}\right]}$$

From equation 3.8, the function has three separate poles and a zero.

The poles are given by $P_1 \approx \frac{1}{C_m g_{m2}g_{m3}R_1R_2R_L}$, $P_2 \approx \frac{g_{m2}}{(C_{gd}+C_{cf})}$ and

$P_3 \approx \frac{(C_{gd}+C_{cf})g_{m3}}{(C_{gd}+C_{cf}+C_2)C_L}$, and the zero is given by $z_1 \approx \frac{g_{m1}g_{m2}}{C_m g_{mff}}$.

At high loads, the transconductance of the pass transistor (gm_3) is large and P_3 is located at a very high frequency and does not affect stability. It can be seen that g_{mff} controls the position of the zero[29]. By setting $z_1 = p_2$ to cancel the effect of the second pole. The zero provides a phase boost for a stable system. However, at low loads, g_{m3} is small since the pass transistor passes very little current. The two non dominant poles become a pair of complex poles as a result. The dominant pole and the zero locations remain unchanged. The location of the complex pair is located at $p_2 =$

$\sqrt{\left(\frac{g_{m2}g_{m3}}{(C_{gd}+C_2)C_3}\right)}$. The quality factor, Q of the poles is high and this causes instability. The quality factor can be approximated by

$$Q = \sqrt{\frac{(C_{gd}+C_2)C_3}{g_{m2}g_{m3}}}\left[\frac{C_m g_{m2} g_{m3}}{C_{m1}C_{gd}(g_{m3}-g_{m2}) + C_{cf}C_L g_{m2} + C_m C_{cf} g_{m2} g_{m3} R_{cf}}\right] \quad (3.9)$$

As can be seen from equation 3.9 , the Q of the complex poles reduces with an larger R_{cf} and C_{cf}.

R_{cf} is the input impedance of the current buffer, given by $\frac{1}{gm_{4,5}}$. The Q of the poles can therefore be reduced by reducing the transconductance of $M_{4,5}$ and increasing the capacitance C_{cf}. The transconductance of $M_{4,5}$ can be reduced by reducing the aspect ratio of $M_{4,5}$.

The effectiveness of this compensation scheme is illustrated in figures (3.13-3.15). Pole-zero analysis was carried out on the LDO loop using Cadence. Figure 3.13 represents the pole and zero locations at max load ($I_L = 100\ mA$). It can be seen that the first three poles are all real and on the left hand plane. The first pole is located around 278 kHz. The second pole is located at 10.82 MHz which is beyond the unity gain frequency of the system. This guarantees that the system is stable.

Poles (Hz)

	Real	Imaginary	Qfactor
1	-2.77923e+05	0.00000e+00	5.00000e-01
2	-1.08239e+07	0.00000e+00	5.00000e-01
3	-1.87048e+07	0.00000e+00	5.00000e-01
4	-4.29709e+08	0.00000e+00	5.00000e-01
5	-7.10465e+08	+/- 1.43318e+07	5.00102e-01
6	-9.51156e+08	0.00000e+00	5.00000e-01
7	-1.48784e+09	0.00000e+00	5.00000e-01
8	-2.28073e+09	0.00000e+00	5.00000e-01
9	-3.90655e+09	0.00000e+00	5.00000e-01
10	-7.26150e+09	0.00000e+00	5.00000e-01
11	-1.81736e+10	0.00000e+00	5.00000e-01
12	-3.25762e+10	0.00000e+00	5.00000e-01
13	-4.32077e+10	0.00000e+00	5.00000e-01
14	-4.37103e+10	0.00000e+00	5.00000e-01
15	-4.42363e+10	0.00000e+00	5.00000e-01
16	-6.78058e+10	0.00000e+00	5.00000e-01
17	-1.61526e+11	0.00000e+00	5.00000e-01
18	-2.92089e+11	0.00000e+00	5.00000e-01
19	-3.25427e+11	0.00000e+00	5.00000e-01
20	-5.32204e+11	0.00000e+00	5.00000e-01
21	-1.15838e+11	+/- 5.55000e+11	2.44721e+00
22	-9.01631e+11	0.00000e+00	5.00000e-01

Zeros (Hz)
at V(net05,0)/V1

	Real	Imaginary	Qfactor
1	-6.67492e+05	0.00000e+00	5.00000e-01
2	-3.71774e+08	0.00000e+00	5.00000e-01
3	-3.35148e+08	+/- 3.70028e+08	7.44812e-01
4	8.03916e+08	0.00000e+00	-5.00000e-01
5	-7.45294e+07	+/- 1.50081e+09	1.00810e+01
6	-5.26384e+09	0.00000e+00	5.00000e-01
7	-2.94215e+10	+/- 3.28608e+10	7.49576e-01
8	-1.15024e+11	+/- -6.20729e+11	2.74418e+00

Figure 3.13: Poles and Zeros at Max Load ($I_L = 100\ mA$)

In figure 3.14, the load current is minimum ($I_L = 0\ mA$). The aspect ratio of $M_{4,5}$ is $1.28\mu/1.7\mu$ and the from dc simulation $g_{m4,5} = 29.5\ \mu S$. It can be seen that the two non-dominant poles become a complex conjugate pair. The q factor of the complex poles is 5.6. The high Q of the complex poles makes the system unstable because they cause a sharp drop in the phase of the system.

Poles (Hz)

	Real	Imaginary	Qfactor
1	-3.89266e+05	0.00000e+00	5.00000e-01
2	-7.43617e+04	+/- 8.31660e+05	5.61430e+00
3	-2.94653e+07	0.00000e+00	5.00000e-01
4	-4.15328e+08	0.00000e+00	5.00000e-01
5	-4.36843e+08	0.00000e+00	5.00000e-01
6	-7.64704e+08	0.00000e+00	5.00000e-01
7	-1.48780e+09	0.00000e+00	5.00000e-01
8	-2.29215e+09	0.00000e+00	5.00000e-01
9	-5.75330e+09	0.00000e+00	5.00000e-01
10	-1.17062e+08	+/- 9.33532e+09	3.98766e+01
11	-2.96665e+10	0.00000e+00	5.00000e-01
12	-4.32039e+10	0.00000e+00	5.00000e-01
13	-4.37025e+10	0.00000e+00	5.00000e-01
14	-4.42322e+10	0.00000e+00	5.00000e-01
15	-6.83174e+10	0.00000e+00	5.00000e-01
16	-1.60754e+11	0.00000e+00	5.00000e-01
17	-3.07559e+11	0.00000e+00	5.00000e-01
18	-1.31482e+11	+/- 3.61243e+11	1.46190e+00
19	-4.28389e+11	0.00000e+00	5.00000e-01
20	-6.34553e+11	0.00000e+00	5.00000e-01
21	-9.01631e+11	0.00000e+00	5.00000e-01

Zeros (Hz)
at V(net05,0)/V1

	Real	Imaginary	Qfactor
1	-1.22428e+06	0.00000e+00	5.00000e-01
2	6.18818e+06	0.00000e+00	-5.00000e-01
3	-1.20188e+08	0.00000e+00	5.00000e-01
4	-3.48135e+08	+/- 1.99938e+08	5.76592e-01
5	-7.45294e+07	+/- 1.50081e+09	1.00810e+01
6	-1.67357e+10	+/- 2.37516e+10	8.68072e-01
7	-3.07095e+11	0.00000e+00	5.00000e-01
8	-1.62161e+11	+/- 3.96972e+11	1.32219e+00
9	-5.46056e+11	+/- 1.00044e+11	5.08322e-01

Figure 3.14: Pole and Zero Locations at Minimum Load ($I_L = 0\ mA$) without Q Reduction

Poles (Hz)

	Real	Imaginary	Qfactor
1	-3.37193e+05	0.00000e+00	5.00000e-01
2	-1.01085e+06	+/- 7.26166e+05	6.15642e-01
3	-4.79126e+07	0.00000e+00	5.00000e-01
4	-4.33390e+08	0.00000e+00	5.00000e-01
5	-7.52366e+08	0.00000e+00	5.00000e-01
6	-1.48780e+09	0.00000e+00	5.00000e-01
7	-2.06106e+09	0.00000e+00	5.00000e-01
8	-2.28225e+09	0.00000e+00	5.00000e-01
9	-7.20191e+09	0.00000e+00	5.00000e-01
10	-1.20261e+08	+/- 9.33066e+09	3.87967e+01
11	-3.22099e+10	0.00000e+00	5.00000e-01
12	-4.32040e+10	0.00000e+00	5.00000e-01
13	-4.37024e+10	0.00000e+00	5.00000e-01
14	-4.42322e+10	0.00000e+00	5.00000e-01
15	-6.78705e+10	0.00000e+00	5.00000e-01
16	-1.61467e+11	0.00000e+00	5.00000e-01
17	-2.92249e+11	0.00000e+00	5.00000e-01
18	-3.25705e+11	0.00000e+00	5.00000e-01
19	-5.37567e+11	0.00000e+00	5.00000e-01
20	-1.15426e+11	+/- 5.54215e+11	2.45226e+00
21	-9.01631e+11	0.00000e+00	5.00000e-01

Zeros (Hz)
at V(net05,0)/V1

	Real	Imaginary	Qfactor
1	-5.12016e+05	0.00000e+00	5.00000e-01
2	1.46768e+07	0.00000e+00	-5.00000e-01
3	-2.72553e+08	0.00000e+00	5.00000e-01
4	-3.15810e+08	+/- 2.15862e+08	6.05639e-01
5	-7.45294e+07	+/- 1.50081e+09	1.00810e+01
6	-3.41736e+09	0.00000e+00	5.00000e-01
7	-3.30532e+10	+/- 3.14163e+10	6.89821e-01
8	-1.09276e+11	+/- 6.16577e+11	2.86515e+00

Figure 3.15: Pole and Zero Locations at Minimum Load ($I_L = 0\ mA$) with Q Reduction

In figure 3.15, the load current is still kept at its minimum ($I_L = 0\ mA$). The aspect ratio of $M_{4,5}$ is however reduced to $0.28\mu/1.7\mu$. From the dc simulations $g_{m4.5}$ is now $14.6\ \mu S$ The Q factor of the complex poles has reduced from 5.6 to 0.62. There's no peaking now since Q<0.717. The system can now be easily compensated by a zero. This shows the effectiveness of the Q-reduction technique used in the error amplifier.

3.2 DESIGN IMPLEMENTATION

In this section, the procedure and formulae used in the design of the LDO is presented. All designs were done with the Cadence IC design suite. The full load (100mA) preliminary specifications for the design are given in

Table 3.1.

Specification	**Value**
V_{IN}	1.3 V
V_{OUT}	1.1 V
V_{do}	200 mV
I_{max}	100 mA
Loop gain	50 dB
Quiescent current	15 uA
Max overshoot/undershoot	100 mV

Table 3.1: LDO Full Load (100mA) Preliminary Specifications

The design was started by characterizing the devices in the IBM 130 nm technology library. The parameters were extracted by simulation. Square law approximation is used for all calculations unless otherwise stated.

Table 3.2 shows the basic device models that were used in the design.

Device Parameter	NMOS	PMOS
V_{th}	$0.398\,V$	$0.420\,V$
μC_{ox}	$68.35\mu A/V^2$	$34.7\mu A/V^2$
$lambda$	$0.052V^{-1}$	$0.065V^{-1}$

Table 3.2: Device Characterization

3.2.1 Pass Transistor Design

The pass transistor determines the dropout voltage and the maximum load and is therefore very important to design well. According to initial specifications, the dropout voltage was chosen to be 200mV. This is decent as it allows for a reasonable efficiency without sacrificing too much chip space. The dropout voltage and efficiency are related by the following equation.

$$eff = 1 - \frac{V_{DO}}{V_{IN}} \tag{3.10}$$

Square law device models were used to calculate for initial device sizes. Equation 3.11 shows the relationship between the output current, dimensions and saturation voltage of a transistor.

$$V_{do} = V_{DSAT} = \sqrt{\frac{2I_{MAX}}{\mu_p C_{ox}\left(\frac{W}{L}\right)}} \tag{3.11}$$

The hole mobility, μ_p and oxide capacitance C_{ox} were determined models of the transistors.

For a maximum load current of 100mA and dropout voltage of 200mV, the aspect ratio was then calculated and found from equation 3.12. Also to achieve a dropout

voltage of 200mV and max load current of 100mA, the on resistance, R_{ON} at max load should at least be equal to

$$R_{ON} = \frac{V_{do}}{I_{MAX}} \tag{3.12}$$

Minimum length was chosen to maximize current and transconductance. The minimum length for the technology is $120nm$. Simulations were run to verify and tune the size. The finalized size used was $4.8mm/120nm$.

The size is very large as expected. This should lead to large parasitic capacitance at the gate. From DC simulations, the gate capacitances were obtained. The total lumped gate capacitance was also obtained.

Parameter	**Size**
W/L	$4.8mm/120\ nm$
C_{GS}	$2.43\ pF$
C_{GD}	$1.426\ pF$
C_{GG}	$3.86\ pF$

Table 3.3: Pass Transistor Parameters

Much attention was paid during the physical layout of the pass transistor to maximize current capability while keeping stray capacitances low. The transistor was split into 2400 fingers, each with a dimension of $2\ um/120\ nm$. The layout had to be compact in order to minimize parasitic capacitance and wire resistance. Good Matching

and symmetry for equal distribution of current was also considered. The layout occupies an area of $74\ \mu m\ x\ 45\ \mu m$ and is shown in figure 3.16.

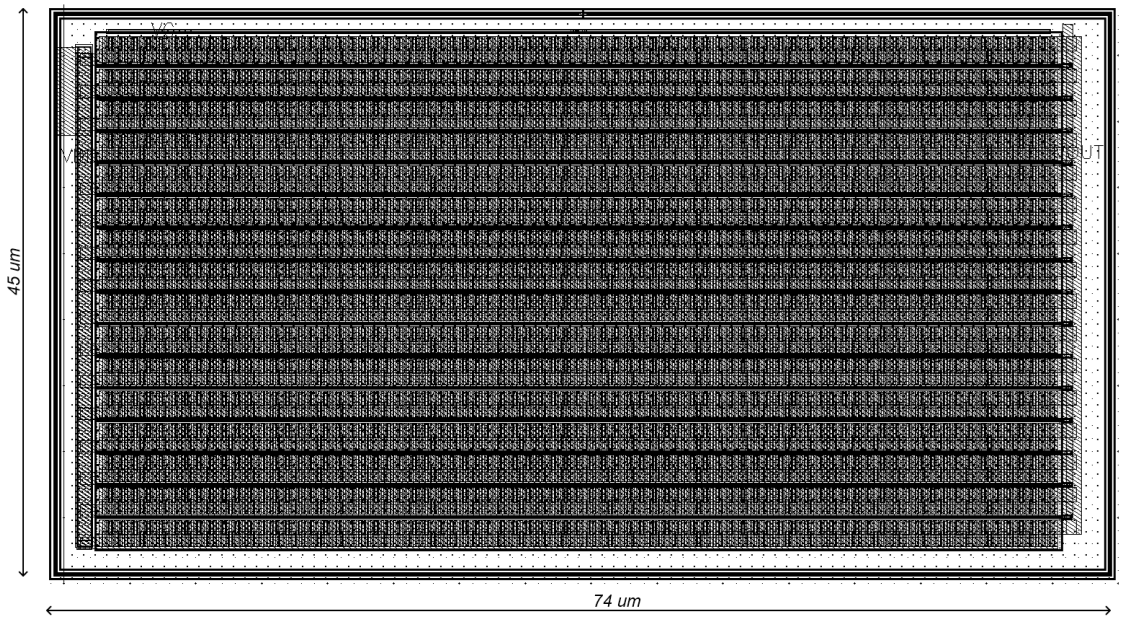


Figure 3.16: Layout of Pass Transistor

3.2.2 Feedback Resistors

The resistive divider determines the feedback factor. The feedback factor, β determines the voltage level of the feedback and the therefor the output voltage regulated and goes on to affect the loop gain of the system. The size of the resistors directly determine how much quiescent current passes through the pass transistor. It is expressed in the following equation.

$$I_{q,Mp} = \frac{V_{out}}{R_1 + R_2} \tag{3.13}$$

Even though using large feedback resistors reduces quiescent current, transient performance worsens as the RC time constant for charging and discharging become larger. This affects settling time as well as undershoot/overshoot. Power supply rejection is also seen to worsen as feedback resistors are made larger.

For a quiescent current of 2.2uA, the sum of the resistors according to equation 3.13 can be calculated.

$$R_1 + R_2 = 500k\Omega$$

The feedback ratio chosen for the design was 0.5. Therefore equal sized resistors were used.

$$R_1 =, R_2 = 250k\Omega$$

3.2.2.1 Layout

Each resistor was broken into 10 series segments to minimize parasitic capacitances. The various segments were interdigitized for good matching to even out the effects of process and temperature variations. Polysilicon resistors were used.

The nominal resistance, R_{nom} of each segment is calculated from equation 3.14.

$$R_{nom} = R_s\left(\frac{L}{W}\right) + 2 \cdot \frac{R_{con}}{W} \tag{3.14}$$

where R_s is the sheet resistance of the material, L and W are the length and width of the resistor and R_{con} is the contact resistance. Layout is shown in figure 3.17.

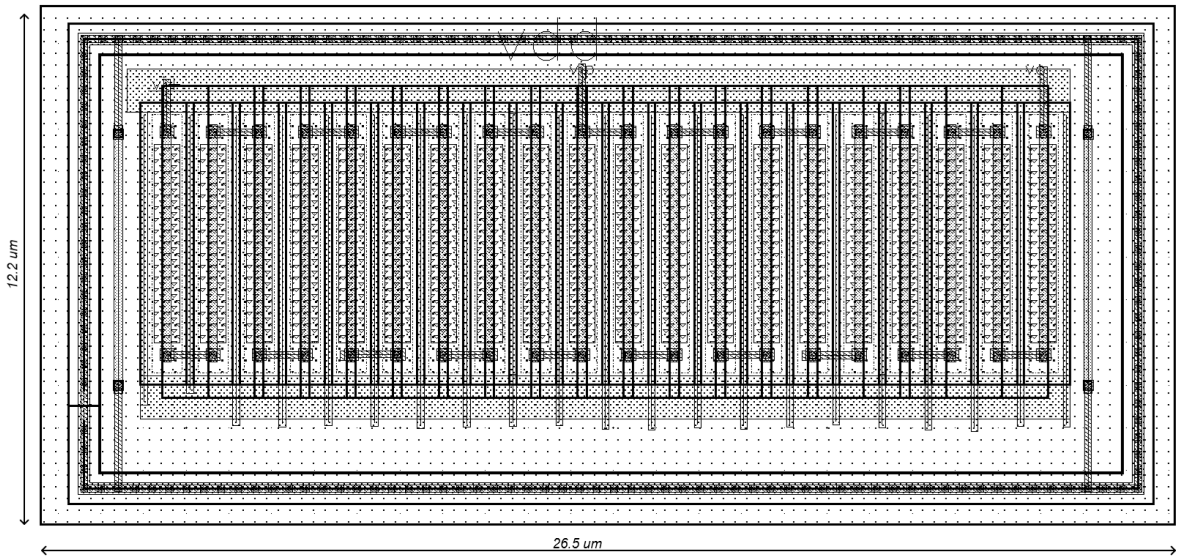


Figure 3.17: Layout of Resistive Ladder

3.2.3 Error Amplifier Design

Generally, for the purposes of AC analysis, the capacitor-less LDO can be considered to be a three-stage amplifier. As the output current reduces the two non-dominant poles become complex and thus have large quality factor, Q. This causes magnitude peaking, faster phase change which consequently leads to instability. The whole loop together with the amplifier was designed for the following specifications at full load (100 mA) with a 100pF load.

Specification	Value
DC gain	40 dB
GBW	8.5 MHz
Phase margin	90

Table 3.4: Error Amplifier Specifications

For the error amplifier (shown in fig 3.11), the first and second stage gains are given by the following.

First stage gain, $A_{v1} = gm_3 r_{o3} || r_{o5}$

Second Stage gain, $A_{v2} = \frac{g_{m6}}{g_{m7}} g_{m8} r_{o8} || r_{o9}$

where gm_3, g_{m6}, g_{m7} and g_{m8} are the transconductances of M_3, M_6, M_7 and M_8 respectively and r_{o3}, r_{o5}, r_{o8} and r_{o9} are the output impedances of M_3, M_5, M_8 and M_9 respectivley. The input pair tail current was design to be 0.8 μA with the second and third branches consuming 0.5 μA and 2μA respectively.

The pole and zero locations for the loop are given as follows

$$P_1 \approx {}^{1}/_{C_m g_{m2} g_{mp} R_1 R_2 R_L}$$

$$P_2 \approx {}^{g_{m2}}/_{(C_{gd} + C_{cf})}$$

$$P_3 \approx {}^{(C_{gd} + C_{cf}) g_{mp}}/_{(C_{gd} + C_{cf} + C_2) C_L}$$

$$z_1 \approx {}^{g_{m1} g_{m2}}/_{C_m g_{mff}}$$

where symbols have the same representation as in section 3.1.3.1

The loop was designed to have the following pole and zero locations at full load ($I_L = 100mA$).

$P_1 = 280kHz\,, P_2 = 10\ MHz,\ P_3 = 18.5\ MHz, z_1 = 7\ kHz$

The dominant pole is set by the first stage of the error amplifier and the two non-dominant poles are located at the pass transistor gate node and the output node of the LDO respectively. The device sizes and bias currents used in the amplifier (from Fig 3.11) are shown in table 3.5.

Device	**Size ($\mu m/\mu m$)**	**Bias Current (uA)**
M1	7.0/0.12	0.74
M2	5.0/0.12	0.37
M3	5.0/0.12	0.37
M4	0.28/1.7	0.37
M5	0.28/1.7	0.37
M6	0.28/0.12	0.43
M7	0.34/0.12	0.43
M8	2.72/0.12	1.96
M9	6.4/0.12	1.96

Table 3.5: Device Sizes and Bias Current Used in Error Amplifier

The passive component values used are shown in table 3.6.

Component	Value
R_m	$1\ k\Omega$
C_m	$5\ pF$
C_{cf}	$153\ fF$

Table 3.6: Error Amplifier Passive Component Values

Simulation plots for the loop are shown in figures 3.18 and 3.19. It is observed that the loop gain increases at lower loads. This is because, at low loads the output impedance of the pass transistor increases according to equation 2.13. This increases the gain of the pass transistor. It must be noted that the total gain is always multiplied by the feedback factor (which is 0.5 in most designs), hence, reducing it. In this design the feedback factor used was 0.5.

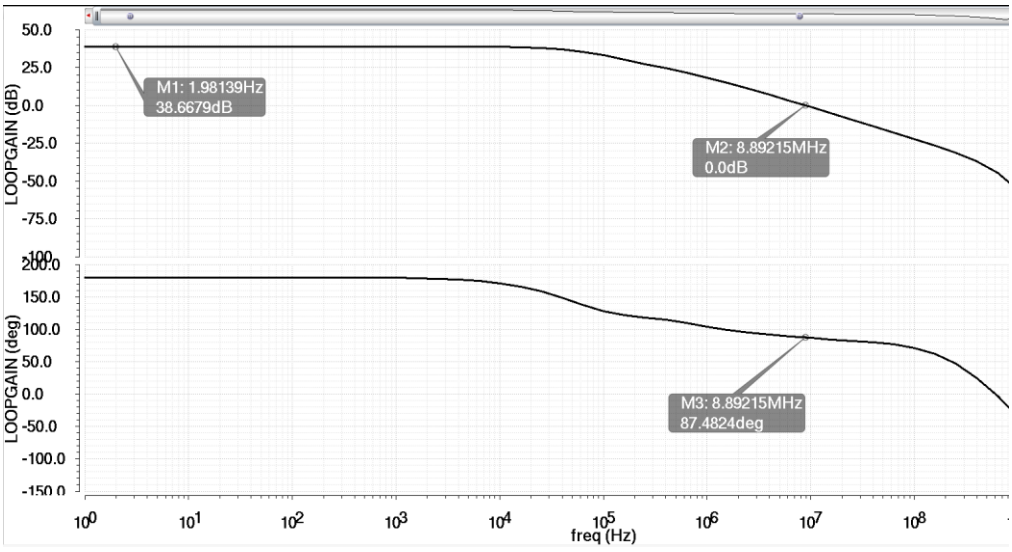


Figure 3.18: Loop Gain of LDO at Max Load ($I_L = 100\ mA$)

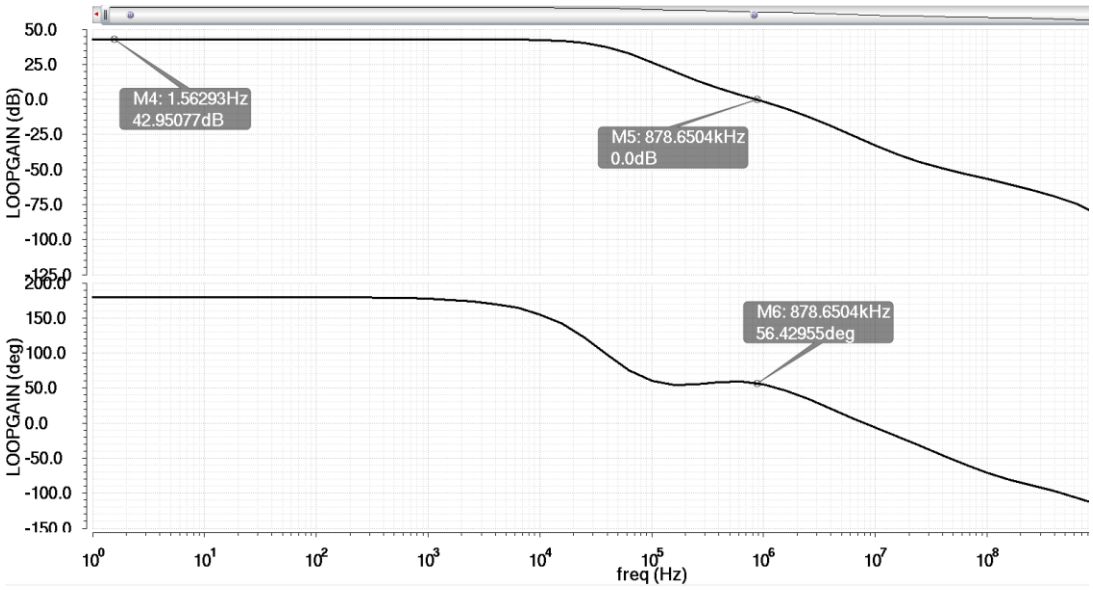


Figure 3.19: Loop Gain of LDO at Minimum Load ($I_L = 0\ mA$)

3.2.3.1 Layout

The layout is shown below in figure 3.20. Good matching was considered for the input pair and the current mirrors.

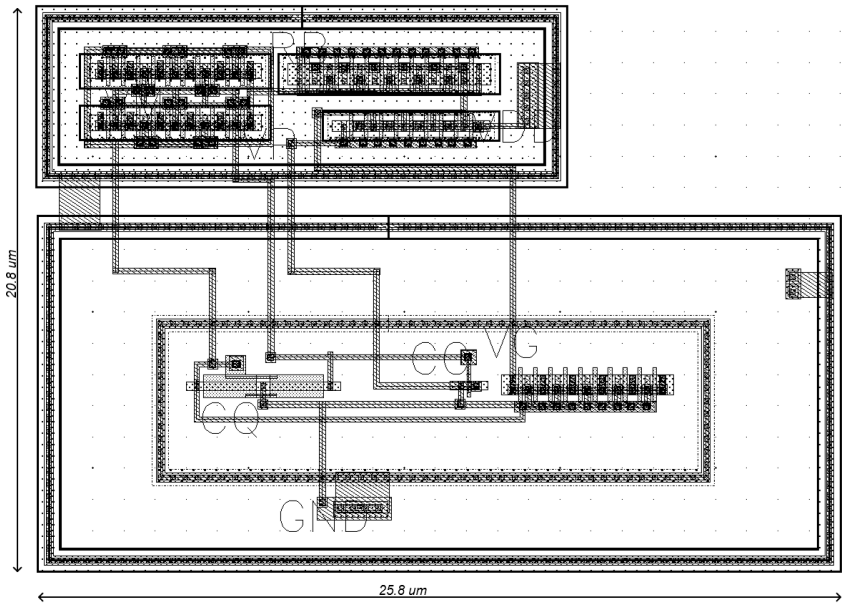


Figure 3.20: Layout of Error Amplifier

3.2.4 Transient Compensation Circuits

The transient detector is meant to detect the sharp transients in the output voltage by use of high pass filters. A transient simulation of the regulator was run for the worst case scenario (I_L 0-100mA). The transient response is shown in figure 3.21.

The specification required a maximum variation of 100 mV at the output. From figure 3.21, in order to meet this specification, the transient compensation circuit must react within 54.4 ns. The lower limit to frequency of operation of the circuit can therefore be determined.

$$f > \frac{1}{55 \times 10^{-9}} = 18.4\ MHz$$

This helps us to design the transient compensation circuit which is discussed in the next section.

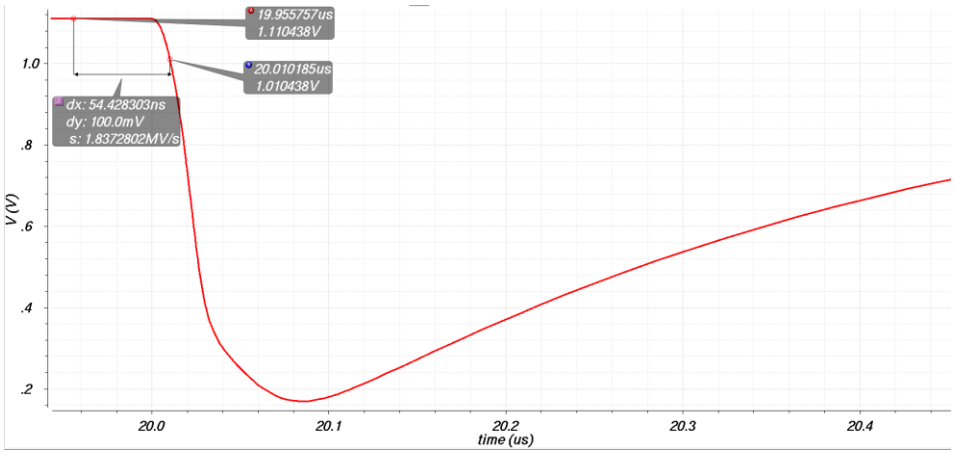


Figure 3.21: Close-up View of Transient Response

3.2.4.1 Transient Detector

Figure 3.22 shows a schematic of the transient detector.

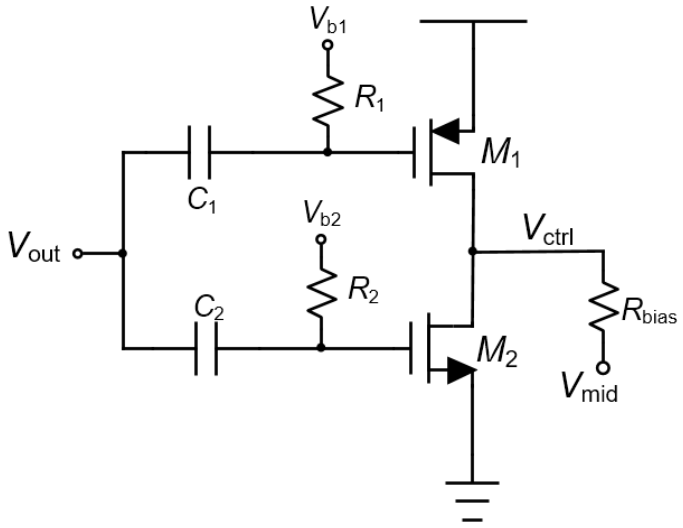


Figure 3.22: Schematic of Transient Detector

The transfer function of the high pass filter is given as

$$H(s) = \frac{sRC}{1 + sRC} \tag{3.15}$$

Since the bandwidth required is, the corner frequency of the filter should be greater.

Therefore we choose $R_1 = R_2 = 1.5\ k\Omega$ and $C_1 = C_2 = 6\ pF$.

From the values of $R_1, R_2\ and\ \ C_1, C_2$, the time constant can be calculated as

$$\tau = RC = 9\ ns$$

The size of R_{bias} used was $50\ k\Omega$.

Figure 3.23 shows the ac response of the filter. As expected, it has a high pass response and has corner frequency at $18\ MHz$. Since it is lower than $18.4\ MHz$, the signal will not be filtered out by the high pass filter.

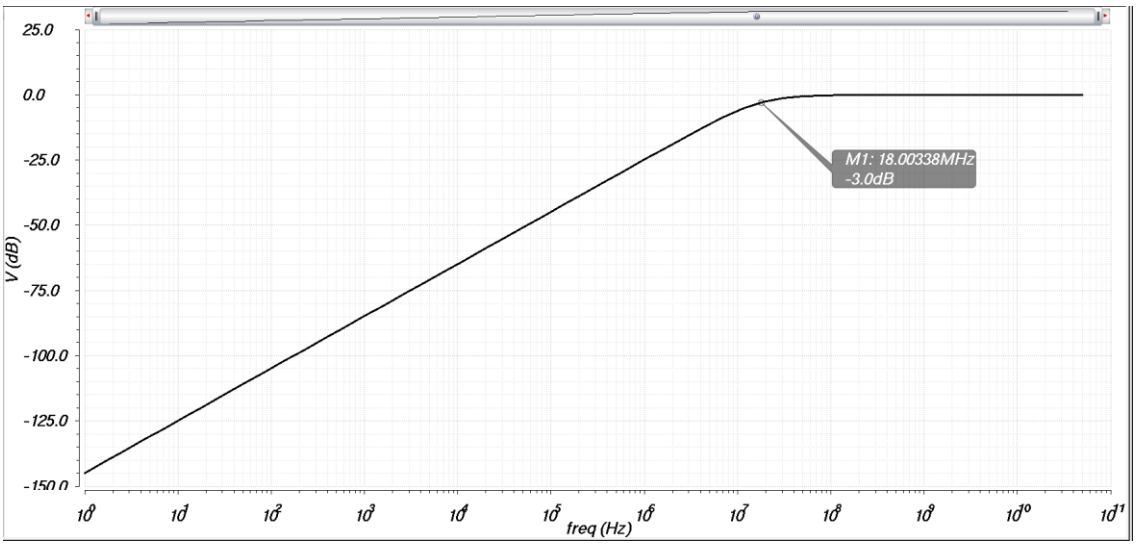


Figure 3.23: AC Response of High Pass Filter

The sense FETs M_1 and M_2 are biased at the edge of turn on. The bias current through the transistors in steady state is therefore very low. The size of $M_1$was made about three times the size of M_2 because of the difference between electron and hole mobilities. The sizes and bias currents in the transistors are shown in table 3.7 below.

Device	**Size ($\mu m/\mu m$)**	**Bias Current (μA)**
M1	0.36/0.12	0.24
M2	0.2/0.12	0.24

Table 3.7: Device Sizes and Bias Currents Used in Transient Detector

The layout of the transient detector is shown in figure 3.24.

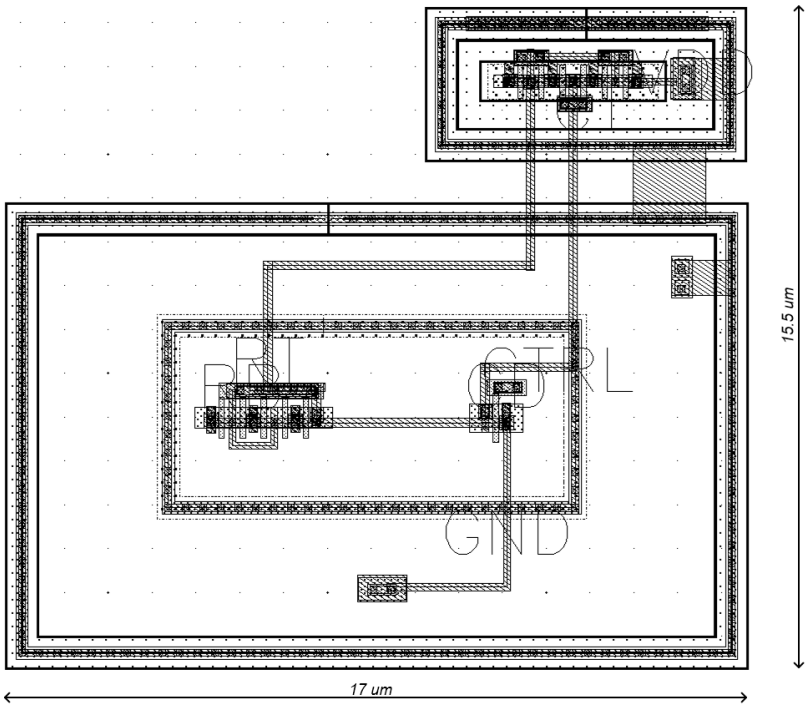


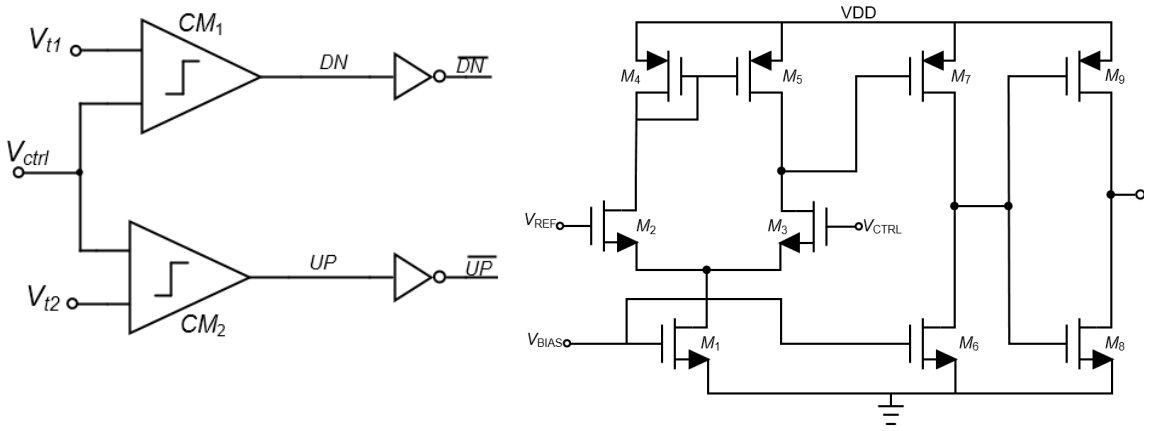
Figure 3.24: Layout of Transient Detector

3.2.4.2 Decision Circuit

Figure 3.25 shows a schematic of the decision circuit and the transistor level implementation of the comparators used.

In steady state, the voltage Vctrl is midrail 650 mV. The threshold voltages were chosen to be equal to $V_{ctrl} \pm 12\ mV$. Therefore $V_{t1} = 662\ mV$ and $V_{t2} = 638\ mV$. This leaves a voltage band of 24 mV in which none of the comparators trip. This value was determined by simulation.

An opamp in open loop is used to implement the comparator. Because the opamp is used in open loop, no compensation is required. The opamp has two gain stages followed by an inverter stage to increase drive strength and ensure a rail to rail signal.



a) b)

Figure 3.25: Decision Circuit a) Overview b) Comparator Schematic

The comparators were designed to meet the following specifications

$$Propagation\ delay\ (t_p) = 3.5\ ns$$

$$Resolution\ (V_{in,min}) = 12\ mV$$

For an output swing ($V_{OH} - V_{OL}$) of 600mV at the output of the first stage, the gain of the first stage can be calculated

$$A_{v1} = \frac{V_{OH} - V_{OL}}{V_{in,min}} = 50 = 34\ dB$$

The gain of the first and second stage is given by

$$\frac{A_{v1}A_{v2}}{(1+s/p_1)(1+s/p_2)} = \frac{g_{m2}r_{o4}g_{m7}r_{o6}}{(1+s/p_1)(1+s/p_2)} \tag{3.16}$$

For the design, the gain of the first stage must be large for good resolution. Since the circuit must be a high- speed, small –sized transistors were also used to minimize parasitic capacitances.

The first stage is designed to have a gain of 35 dB and second stage 15dB. The tail current of the input differential pair is 2.5 μA and the bias current in subsequent branches are 0.5μA each. The max propagation delay can be approximated as $t_p \approx 0.693\tau$, where $1/\tau$ is the location of the dominant pole.

Therefore $p_1 = \frac{0.693}{t_p} = 198\ Mrad/s \approx 32\ MHz$

Figure 3.26 shows the AC response of the comparator. The total DC gain is 50 dB and the 3-dB bandwidth is 35 MHz.

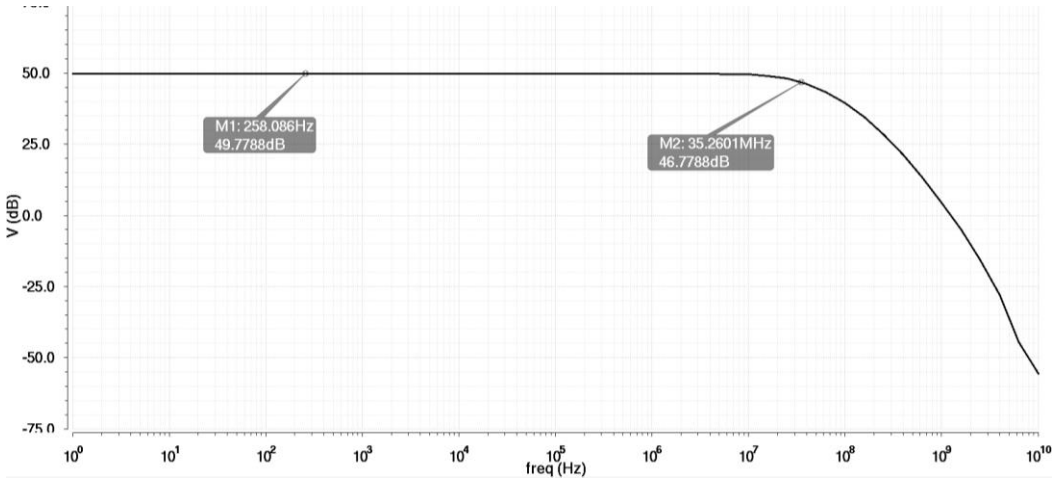


Figure 3.26: AC Response of Comparator

The sizes and bias currents of the transistor used are shown in table 3.8

Device	**Size ($\mu m/\mu m$)**	**Bias Current (μA)**
M1	2.2/0.12	4.48
M2	0.28/0.12	2.24
M3	0.28/0.12	2.24
M4	0.28/0.12	2.24
M5	0.28/0.12	2.24
M6	0.28/0.3	1.8
M7	0.28/0.12	1.8
M8	0.28/0.12	0.1
M9	0.6/0.12	0.1

Table 3.8: Device Sizes and Bias Currents Used in Comparator

The layout of the comparator is shown in figure 3.27.

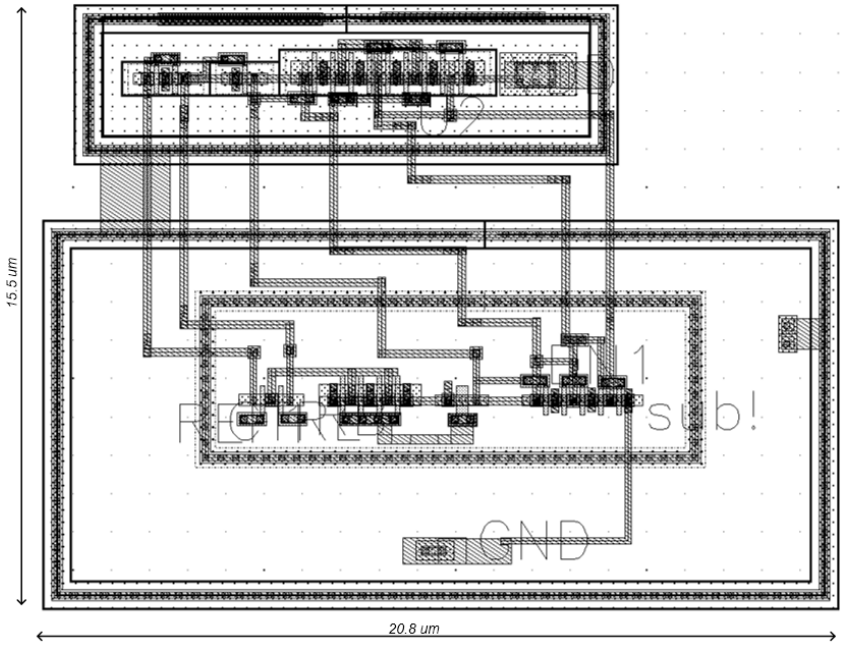


Figure 3.27: Layout of Comparator

3.2.4.3 Slew Boosting Circuit

The transistor level implementation of the slew boosting circuit is shown in figure 3.28 and layout in figure 3.29. Transistors $M_3 - M_6$ represent the current sources whose gates are biased by M_1 and M_2. The switches are implemented by $M_{3a} - M_{6a}$. During operation the switches operate either in cut-off or triode region according to the control signal they receive from the decision stage. From equation 1.7, the aspect ratio W/L has to be large in order to have a low on resistance. However, this may increase turn-on/turn-off time as the gate capacitance also increases. The turn on time for MOSFET according to [30] can be approximated by equation 3.17.

$$t \cong R_G C_{GG} \cdot \ln\left(\frac{1}{1-\frac{V_{gs}}{V_{GS}}}\right) \tag{3.17}$$

where R_G is the gate resistance,C_{GG} is the lumped gate capacitance, V_{GS} is the applied gate-source voltage and V_{gs} is the varying (transient dependent) gate-source voltage of the transistor.

For a 100 mA step in load current, the gate-source voltage required by the pass transistor can be calculated by square law approximation.

$$\Delta V_{gs} = \sqrt{\frac{2\Delta I_L}{\mu_p C_{ox}\frac{W}{L}}} + V_{th} \cong 1.26V$$

with $\mu_p C_{ox} = 24.7\mu A/V^2, \frac{W}{L} = 8000, V_{th} = 420\ mV\ and\ \Delta I_L = 100\ mA$

With the lumped gate capacitance, $C_{GG} = 3.86\ pF$, time period, $dt = 40\ ns$ and gate source voltage needed, $dV_{gs} = 1.26\ V$, the charge/discharge current, I_{chg} needed at the gate of the pass transistor can be calculated.

$$I_{chg} = C_{GG}\frac{dV_{gs}}{dt} \cong 120\ \mu A$$

The current sources have to provide about 120 uA to charge and discharge the capacitance at the pass transistor gate during a no-load to full load transient. Transistor sizing was determined by using square law approximation in equation 3.18.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}\left(V_{gs} - V_{th}\right)^2 \tag{3.18}$$

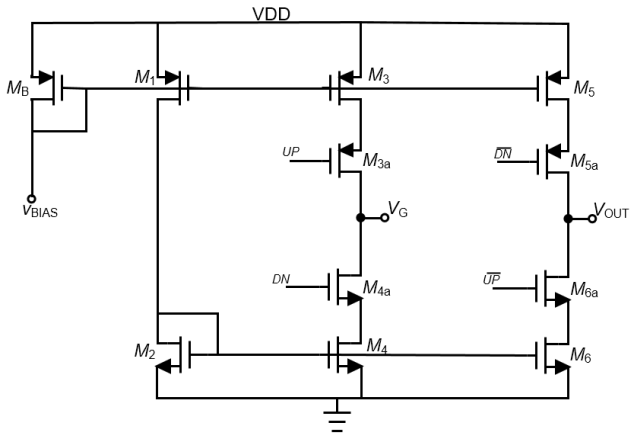


Figure 3.28: Schematic Diagram of Slew Boosting Circuit

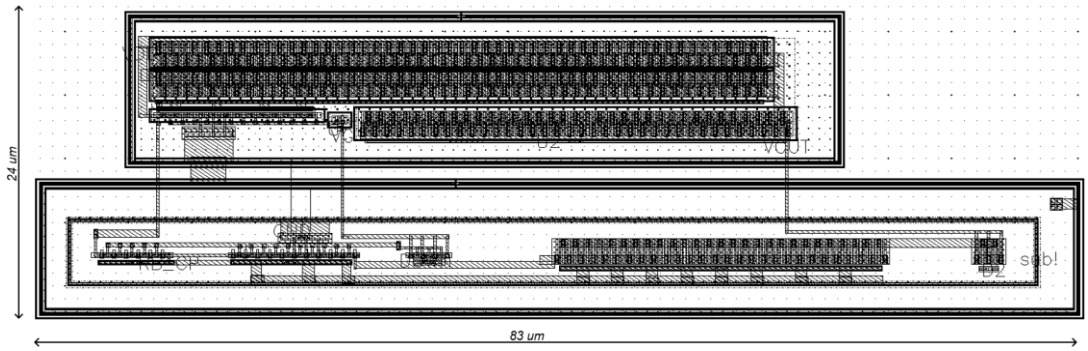


Figure 3.29: Layout of Slew Boosting Circuit

The device sizes and bias currents used in the slew boosting circuit is shown in table 3.9.

Device	Size ($\mu m/\mu m$)	Bias Current (μA)
MB	0.4/0.12	1.6
M1	0.4/0.12	1.6
M2	0.7/0.12	0.01
M3	10/012	0.01
M3a	0.6/0.12	0.01
M4	2.4/0.12	0.01
M4a	12/0.12	0.01
M5	400/0.12	0.01
M5a	140/0.12	0.01
M6	8/0.12	0.01
M6a	108/0.12	0.01

Table 3.9: Device Sizes and Bias Currents Used in Slew Boosting Circuit

The simulation in figure 3.30 shows the current that flows in current sources of the slew boosting circuit (M_3, M_4, M_5 and M_6). As can be seen, the currents are very low (in nanoamps) when the LDO is in steady state. Currents flow only during transients, when the switches are open. This feature ensures that the additional circuitry does not increase the power consumption of the LDO.

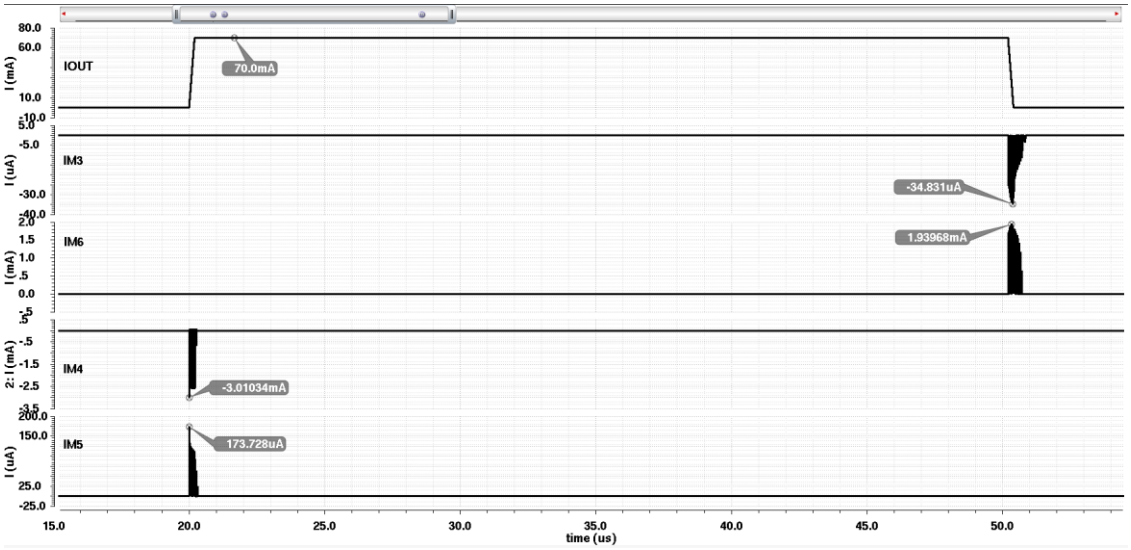


Figure 3.30: Slew Boosting Circuit Simulation Plot

3.2.5 Final LDO Layout

The final design for the voltage regulator was laid out in IBM 130 nm CMOS technology. The layout of the entire circuit with the pad frame is shown in figure 3.31. The actual LDO occupies an area of $370\mu m \times 295\mu m$ while the pad frame measures $1470\ \mu m \times 1470\ \mu m$. The area surrounding the LDO was filled with metal layers to meet density requirements.

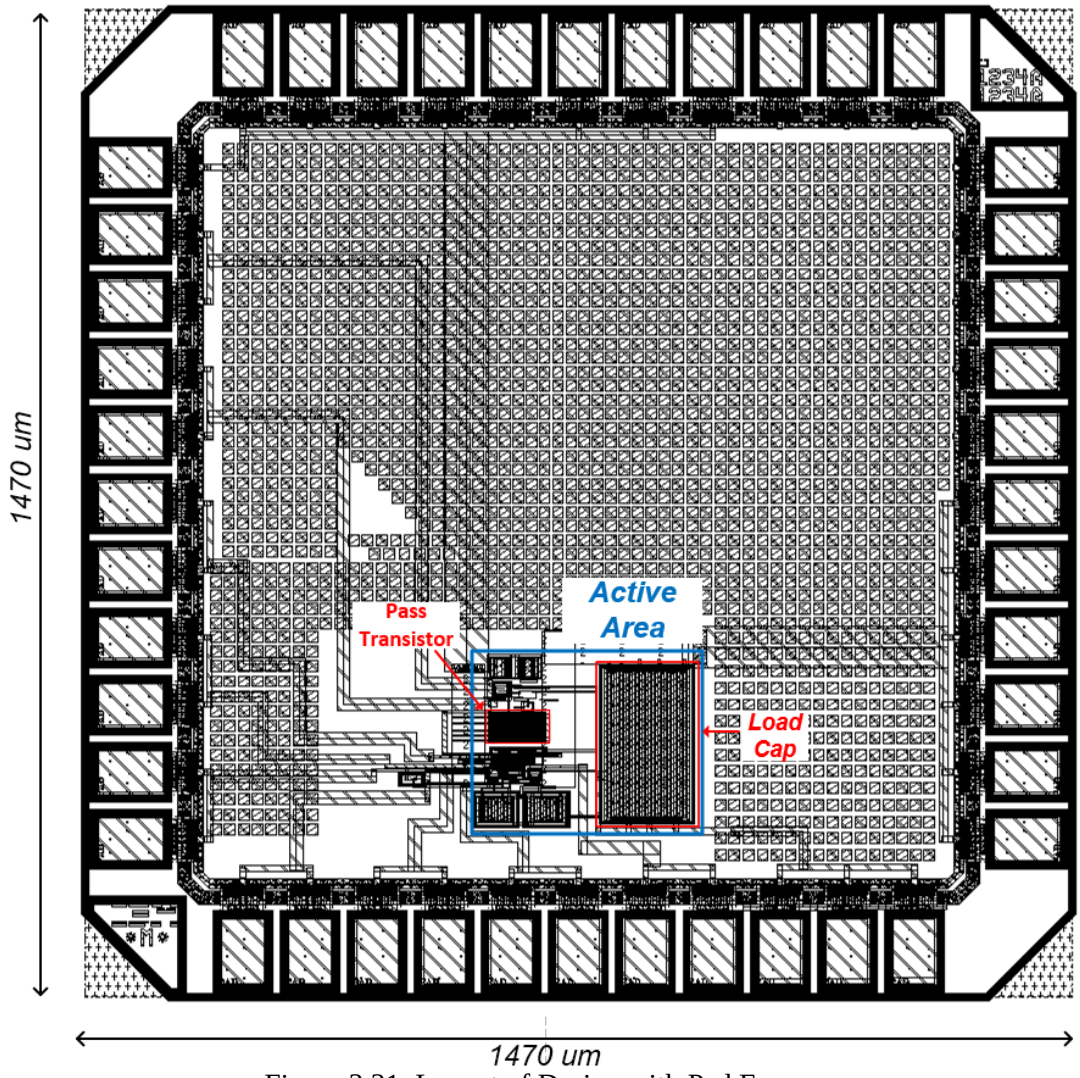


Figure 3.31: Layout of Design with Pad Frame

4 SIMULATION RESULTS

Simulation results are presented in this section. The simulations were carried out in the Analog Design Environment of the Cadence suite. A supply voltage of 1.3V and load capacitor of 100pF are used for the various simulations. A comparison of the results with state-of-the-art works is also shown in Table 4.1

4.1 SIMULATION PLOTS

4.1.1 Load Transient

This section shows the output voltage when a load transient is applied the LDO. The load current was stepped from no load (0 mA) to full load (100 mA) and vice versa with an edge time of 200 ns. The plots show the load transient with and without the use of the proposed techniques.

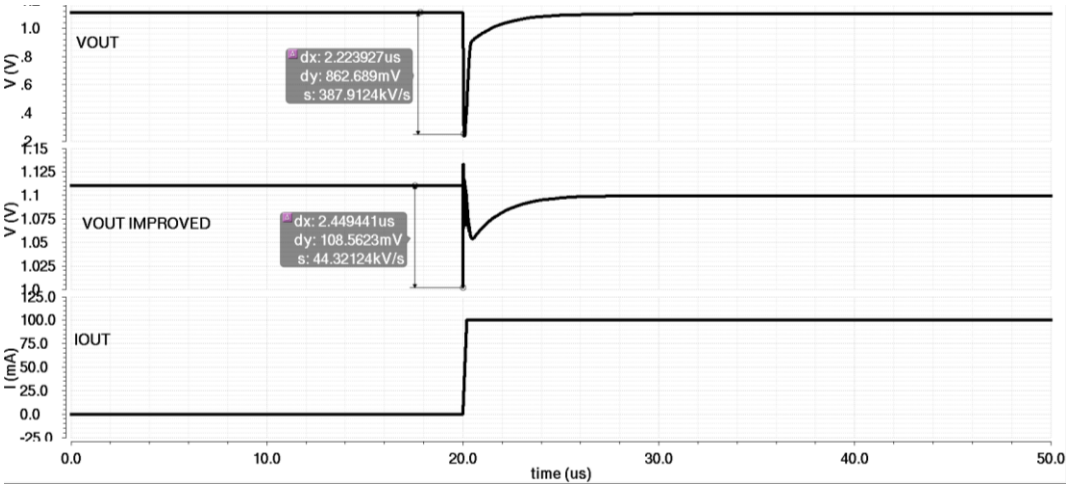


Figure 4.1: Transient Simulation Showing Worst-Case Undershoot

It can be seen from figure 4.1 that there is a marked improvement in the transient performance with the use of the transient compensation technique proposed in this work. The undershoot reduces from 862 mV to 108 mV.

Figure 4.2 shows the worst case overshoot case. Here again the overshoot is reduced from 199.8 mV to 81 mV by use of the proposed transient compensation technique.

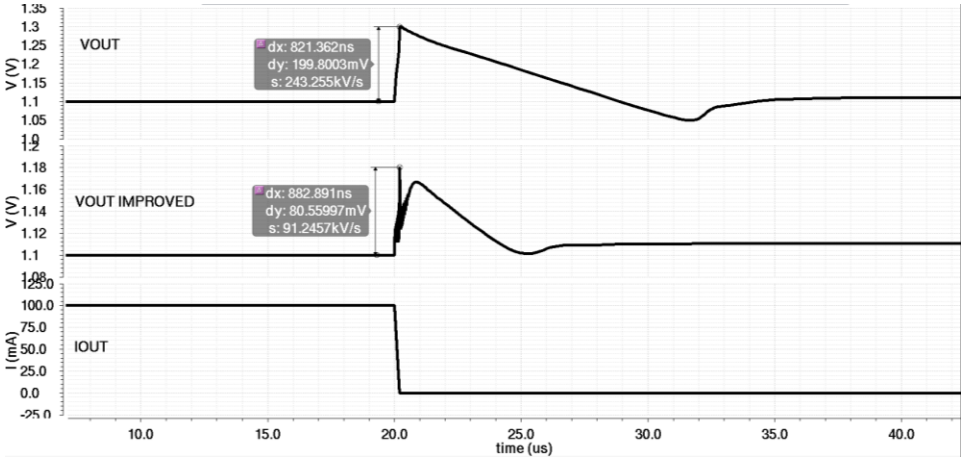


Figure 4.2: Transient Simulation Showing Worst-Case Overshoot

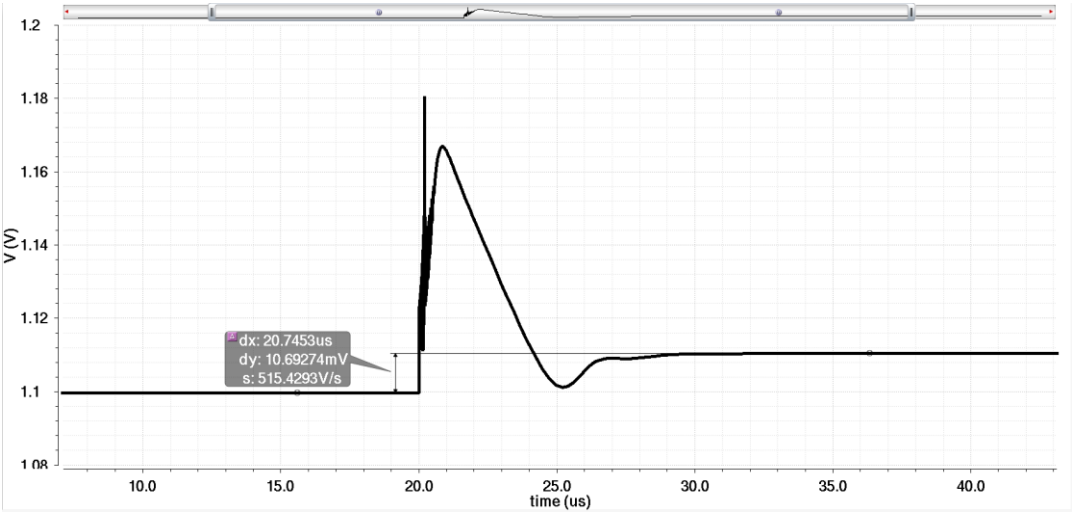


Figure 4.3: Transient Simulation Showing Load Regulation

Figure 4.3 shows that the output voltage varies by 10.7 mV over the entire load range (0-100 mA). This amounts to a load regulation of 0.11 mV/mA.

4.1.2 Line Transient

Line transient simulations are shown next. The input voltage was stepped from 1.3 V to 1.8V (with edge time of 1 μs) and vice versa and the variation in output voltage was measured. This was carried out for both 0 mA and 100 mA output. The results are shown in figures 4.4 and 4.5.

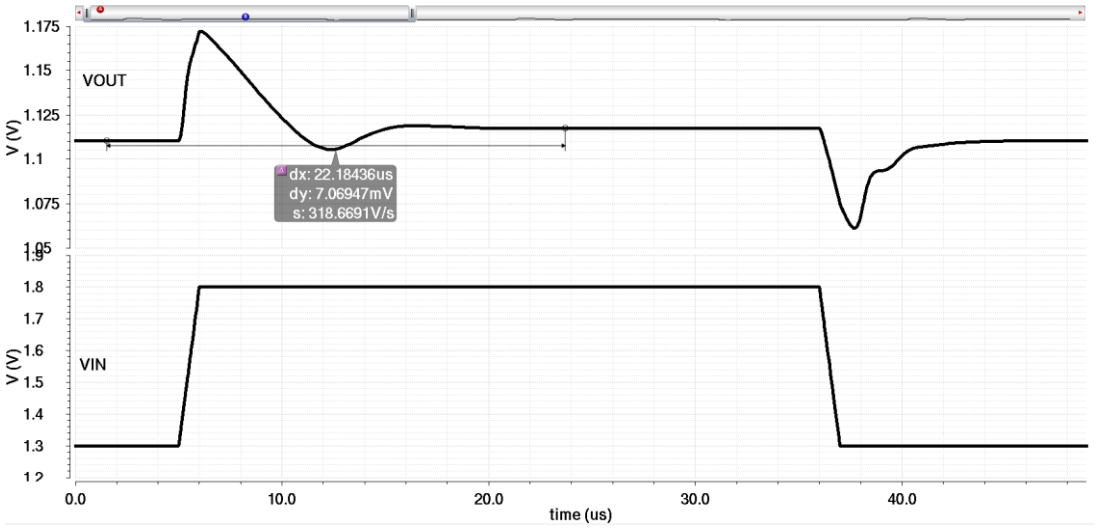


Figure 4.4: Output Voltage Variation at No Load (0 mA)

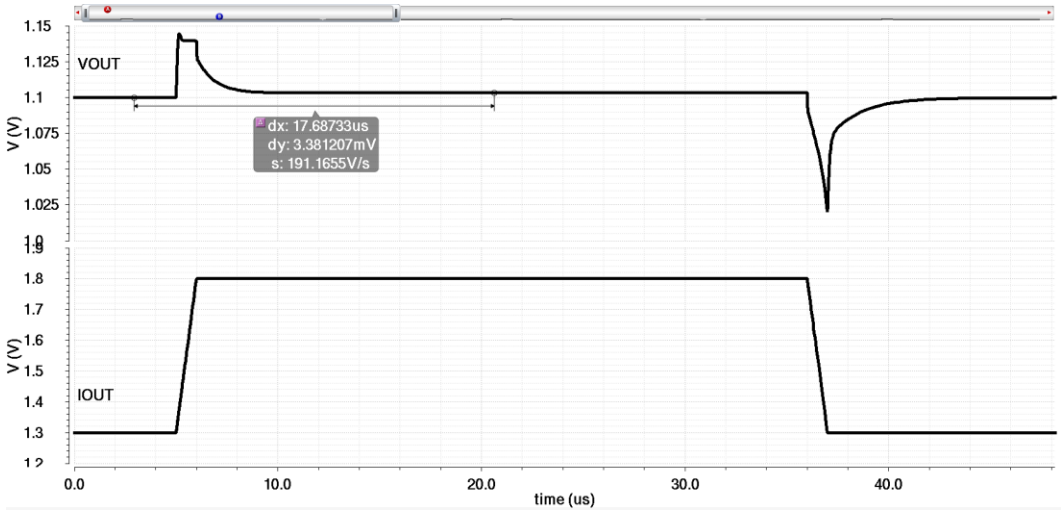


Figure 4.5: Output Voltage Variation at Full Load (100 mA)

4.1.3 Power Supply Rejection

Figure 4.6 shows a plot of the PSR of the LDO across various frequencies. The PSR values were measured at 1 Hz, 1 kHz, and 100 kHz and were found to be -46.6 dB, -46.3 dB and -19.5 dB respectively.

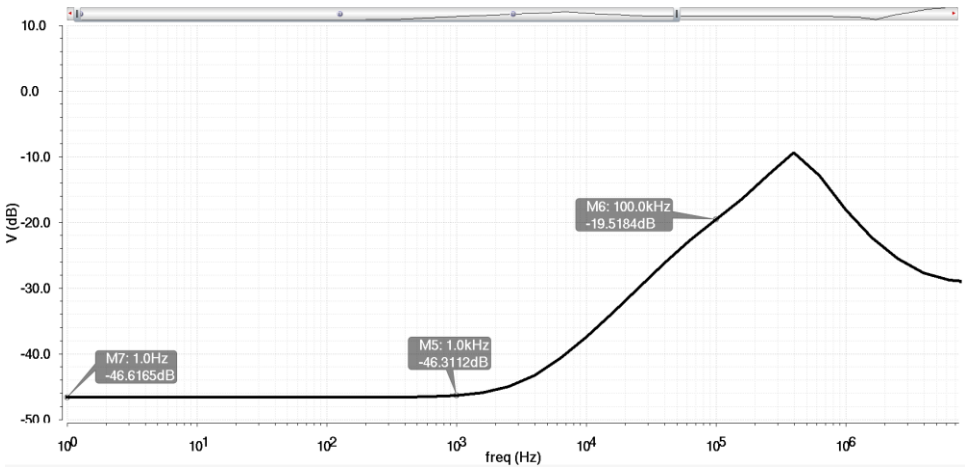


Figure 4.6: PSR Performance of LDO

4.2 PERFORMANCE COMPARISON

Specification	This work	[31]	[32]	[25]	[22]
Year	2017	2013	2014	2013	2016
Technology	0.13	0.35	0.065	0.18	0.35
Vout (V)	1.1	1.1	0.5	1.6	3.25
Dropout Voltage (mV)	200	180	250	200	450
Quiescent Current (uA)	16.5	25	16.2	18	26
Max load (mA)	100	100	50	50	50
Load Step (mA)	0-100	0-100	0-50	0-50	0.1-50
Rise/ Fall time(us)	0.2	0.5	0.1	1	0.1
Overshoot (mV)	108	80	100	75	200
Undershoot (mV)	88	-	103	-	-
C_L (pF)	100	100	100	100	100
Max Power Delivered(W)	0.11	0.11	0.025	0.08	0.1625
FOM*	1.4	0.56	1.19	0.185	0.21

Table 4.1: Comparison with Other Works

$$*\text{FOM}= \frac{\Delta I_{out}}{I_q \times V_{do} \times Ripple_{max} \times t_{rise/fall}} \times 10^{-12}$$

Table 4.1 shows the performance of the LDO designed in this work and compares the relevant performance metrics with those from other state-of-the-art designs. These designs are also use off-chip capacitor-less architectures and all have a small on-chip capacitor of 100 pF just like in this work. A figure of merit (FOM) is defined to capture the essential performance specifications of the circuit and consider the all tradeoffs. The results show that this work has decent transient response even with a small test signal rise time and low current consumption. The table shows that this work

is better in terms of general performance and particularly superior in terms of transient performance.

5 CONCLUSIONS

This work has presented a design which allows the large external capacitor of a conventional LDO to be removed without compromising its transient response. A transient detector together with a bang-bang scheme is employed in the capacitor-less regulator to slew boost the gate of the pass transistor in order to reduce undershoots and overshoots during load transients. This is implemented in an alternate loop which is designed to be faster than the main LDO loop. The loop consists of a transient detector, a decision circuit and a slew boosting circuit which work together to effectively reduce the overshoot and undershoot during load transients. The design also makes use of an error amplifier with Q-reduction to ensure stability during low load conditions. These techniques prove to be effective in improving the stability and transient performance of a capacitor-less LDO without consuming too much quiescent current (about 16.5 uA).

The proposed work has been designed and fabricated in IBM 130 nm CMOS technology through MOSIS educational service. A comparison of this work with other state-of-the-art designs shows the relevance and competitiveness of the techniques used. The techniques discussed and used in this design can be adopted in SoC designs to ensure good performance while saving power and area.

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