DESIGN OPTIMIZATION & CONTROL OF HIGH POWER DENSITY CONVERTERS USING WIDE BAND GAP DEVICES

A Dissertation

by

AHMED MOHAMED SLAHELDIN HASSAN MOHAMED MORSY

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Chair of Committee,	Prasad Enjeti
Committee Members,	Hamid A. Toliyat
	Jose Silva-Martinez
	Prabir Daripa
Head of Department,	Miroslav Begovic

August 2016

Major Subject: Electrical Engineering

ABSTRACT

In this dissertation various converter topologies are proposed and evaluated in view of the state of art solutions to optimize power density and converter efficiency for several applications including photovoltaic solar energy harvesting, energy storage, wind power generation, and medium voltage adjustable speed drives.

The first part of the dissertation, presents a comparison between mitigation techniques for double line frequency ripples in single phase micro-inverters based on Wide Band Gap devices. A topology based on an auxiliary DC-AC stage is adopted based on optimizing both power density and efficiency to achieve the pressing needs for the next generation of micro-inverters as announced by Google's Little Box Challenge. An accurate yet simple control algorithm is proposed that provides a ripple-free DC current. Experimental results demonstrate the effectiveness of the presented topology and control algorithm to achieve high power density (55.8 W/in^3) micro-inverter rated at 2kW.

In the second part of the dissertation a new class of multilevel converters, namely Interconnected Modular Multilevel Converter (IMMC), is introduced and studied in detail. The IMMC provides a new framework for DC-DC and DC-AC conversion exploiting Wide Band Gap devices in a modular structure, achieving high power density in high voltage applications. The performance of the proposed IMMC is evaluated through theoretical analysis and experiments.

ACKNOWLEDGEMENT

I would like to thank my advisor Prof, Prasad N. Enjeti for his guidance during my PhD period. I am privileged and lucky to be one of his students. Despite his overwhelming schedule, he was always generous with his time and guided me to overcome all technical challenges that I faced through my work. He was also a great mentor and gave the best advice for my career.

I would like also to thank my committee members Prof, Hamid A. Toliyat, Prof, Jose Silva Martinez and Dr. Prabir Daripa for their time and guidance. Their technical feedback and recommendations improved my work outcome.

I would like also to express my heartfelt thanks to my colleagues and friends Bahaa Hafez, Yong Zhou, Jorge Ramos, Michael Bayern, Harish Sarma, Teayong Kang and all PQ Lab team members.

I owe every achievement in my life to God, my parents and to my wife who gave me their unconditional love and ultimate support to be the person I am today.

TABLE OF CONTENTS

Page

LIST OF FIGURES

Page

LIST OF TABLES

Page

1 INTRODUCTION [*]

Researchers in power electronics field are constantly striving towards developing higher power density and higher efficiency converters. This work focuses on developing high power density converter topologies/control techniques for low voltage single phase applications as well as high voltage multilevel converters.

1.1 High Density in Single Phase Converters

Inverters are the essential devices converting direct current from Photovoltaic solar panels or batteries to alternating current suitable for use in homes, cars or for utility interface. The problem with conventional inverters is there big size (about the size of a cooler). That is why, in 2014, Google has announced its "Google Little Box Challenge" offering a US $1 million prize to whoever design a power inverter that is about 10 times smaller than what is available today [1]. Google's vision is that building smaller and lighter inverters would allow a wide range of applications like more solar-powered homes especially for remote locations, uninterruptible power supplies UPS with battery energy storage supporting safer, more reliable and efficient data centers, or used for more efficient electric vehicles.

Achieving high power density for single phase inverter imposes a challenge when it is constrained by stringent limits on allowable double line frequency (120Hz)

---

[*] Reprinted with permission from:
"Wide-band gap devices in PV systems - opportunities and challenges" by C. Sintamarean, et al., 2014. International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), pp. 1912-1919. Copyright 2014 by IEEE.
"A Survey of Wide Bandgap Power Semiconductor Devices" by J. Mill, et al., 2014, IEEE Transactions on Power Electronics, vol. 29, pp. 2155-2163. Copyright 2014 by IEEE

ripples on input DC link voltage. These ripples have negative effects on the MPPT efficiency [2, 3] for Photovoltaic solar energy harvesting and reduced battery life in energy storage applications [4, 5].

Conventionally, large electrolytic DC link capacitors are installed to avoid severe voltage fluctuations due to design simplicity and cost effectiveness. However, these electrolytic capacitors have high losses due to their significant equivalent series resistance ESR. They also suffer from short life time compared to film capacitors. Additionally, full reliance on electrolytic capacitors to attenuate voltage ripple at double the line frequency requires excessively high capacitance which makes them bulky.

Consequently, replacing DC-link electrolytic capacitors with an active power decoupling APD circuit has been a hot research topic [6-13]. Adding a DC-DC or DC-AC stage with a capacitive storage element that cycles the AC ripple component addresses the aforementioned issues.

1.1.1 Wide Band Gap Devices and Power Density

One of the most straightforward methods to achieve high the power density is to increase the switching frequency inside the inverter to allow smaller inductive and capacitive filter requirements. Still this increase in switching frequency should coincide with high converter efficiency, otherwise thermal management of such converter will be prohibitive. Fortunately, the continuous improvement in the power semiconductor devices technology specially with the uprise of wide band gap WBG devices like Silicon Carbide SiC and Gallium Nitride GaN, enables high switching frequency combined with

lower losses and high reliability [14], hence penetrating various industrial markets as in Figure 1-1 [15].

Figure 1-2 and Table 1-1 present the superior physical characteristics for SiC and GaN materials over Silicon Si in terms of band gap energy, electron mobility, breakdown electric field and drift velocity, placing GaN on the forefront of switching speeds and lower specific drain-source ON resistance $R_{DS(ON)}$ [16]. Consequently, WBG semiconductor devices facilitate implementing such active power decoupling methods without sacrificing inverter efficiency.

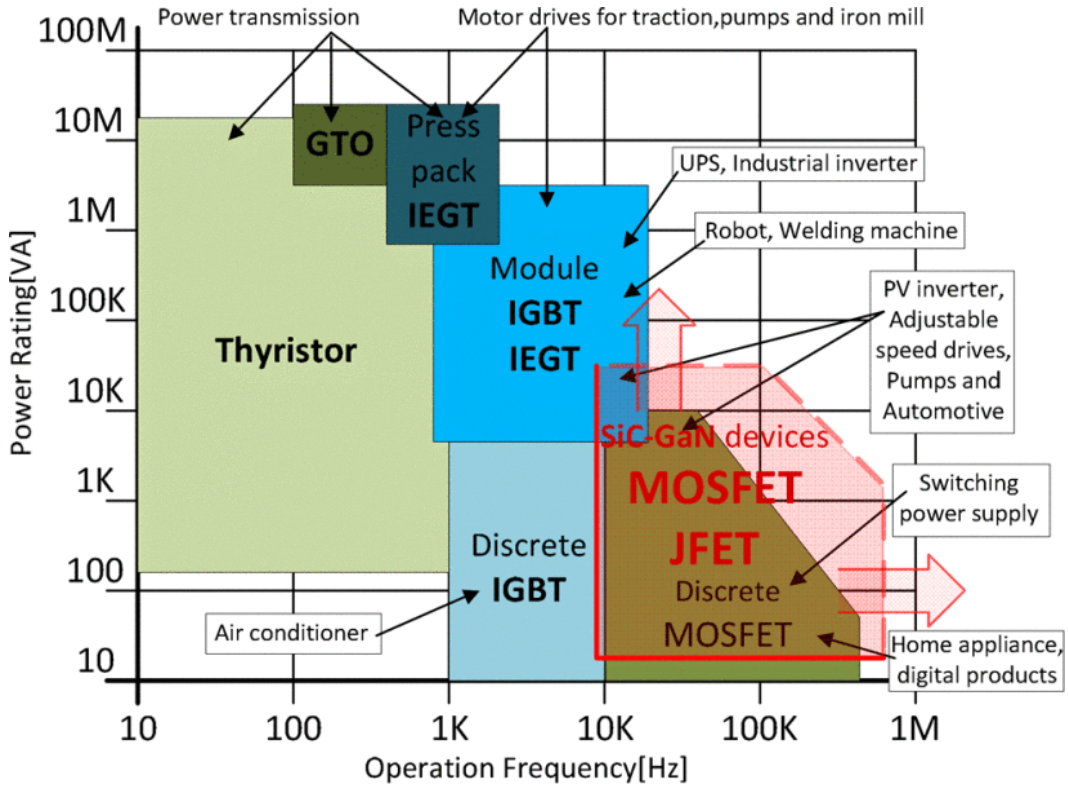


Figure 1-1. The integration on the market of SiC/GaN-based applications (© 2014 IEEE [15]– Adapted with permission from the IEEE)

Table 1-1 Material Properties for Si, SiC and GaN

Property	**Si**	**SiC**	**GaN**
Band gap (eV)	1.1	3.2	3.4
Electron Mobility (cm^2/Vs)	1350	700	1500
Electric Field for Breakdown (10^6 V/cm)	0.3	3.0	3.3
Saturated Electron Drift Velocity (10^7 cm/s)	1.0	2.0	2.5

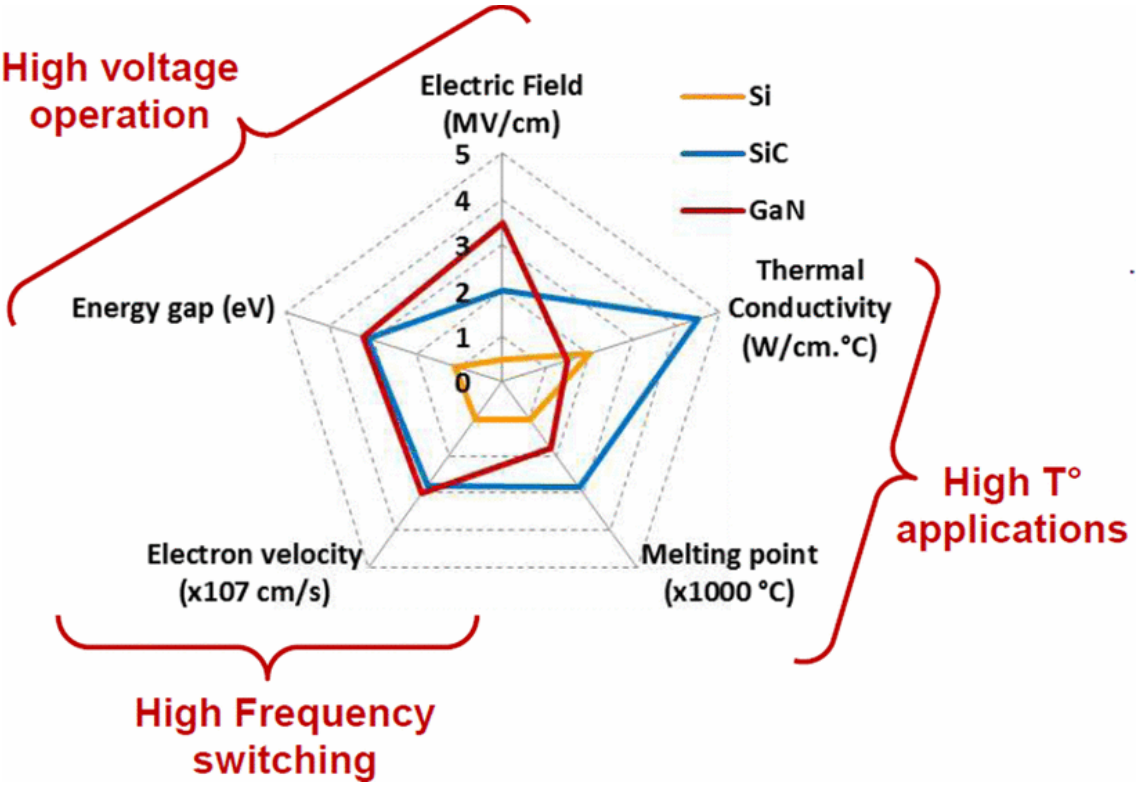


Figure 1-2. Summary of Si, SiC, and GaN relevant material properties
(© 2014 IEEE [16]– Adapted with permission from the IEEE)

1.2 High Power Density in High Voltage Applications

Multilevel converters are the key enabling power conversion technology for high voltage and high power applications. They have experienced a fast growing attention over the last few years [17-21]. Multilevel converters can process higher voltage magnitudes using semiconductor switching devices of smaller ratings. Their advantages include improved output voltage and current waveforms, i.e. power quality, and enhanced electromagnetic compatibility. More importantly they operate at low switching frequencies allowing lower losses, while minimizing the required filtering components. Therefore they can combine high power density with high efficiency.

The most common multilevel topologies are (a) Diode Clamped Multilevel Converter DCMC which came from the neutral-point clamped inverter invented in 1979 1981 by Nabae *et al*. [22], (b) Capacitor Clamped Multilevel Converter CCMC (flying capacitors) [23], (c) Cascaded Multilevel Converter that requires isolated DC supplies [24] and (d) the uprising Modular Multilevel Converters (MMCs) [25].

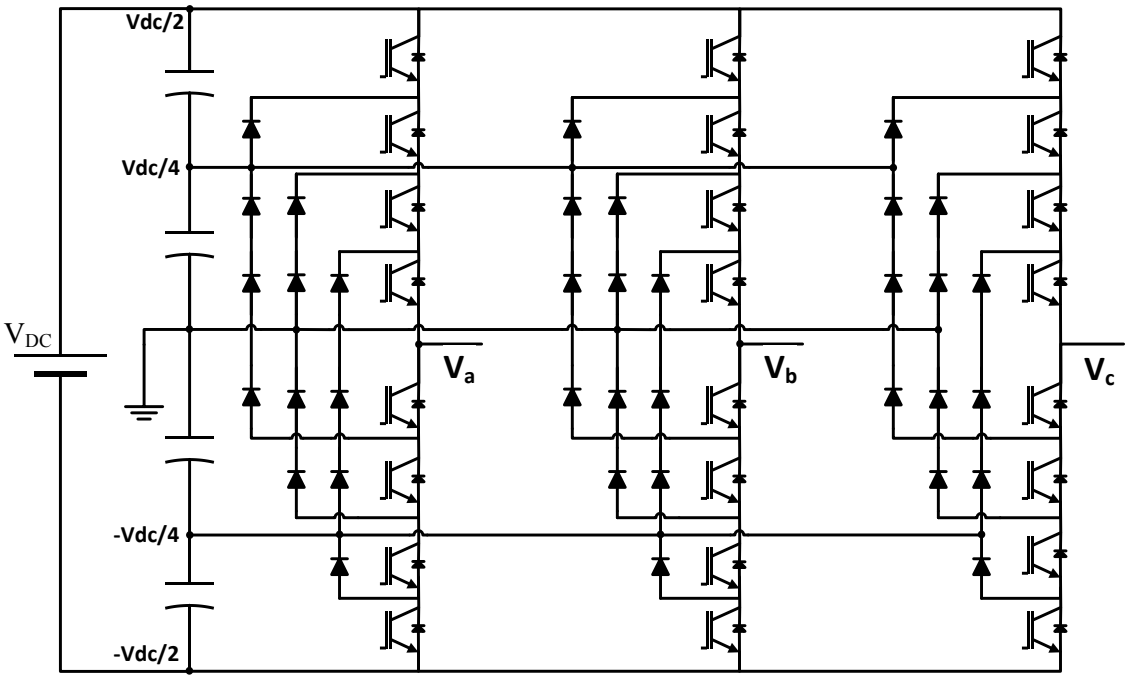
1.2.1 Review on Existing DC-DC and DC-AC Multilevel Converters

Following is a brief review on some of the most common Multilevel Converter topologies, that can be used for DC-AC, DC-DC, or both, highlighting some of their main strengths and weaknesses.

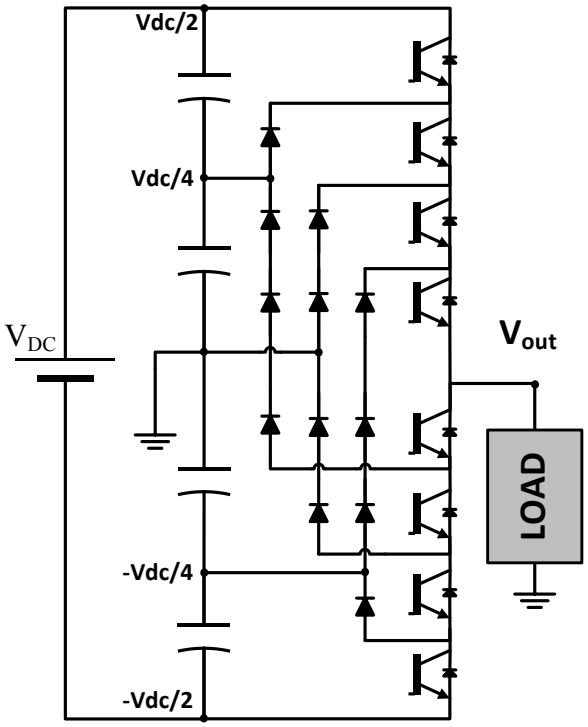
1.2.1.1 Diode Clamped Multilevel Converter DCMC

In Diode Clamped Multilevel Converter, Figure 1-3, the total number of semiconductor switches required, whether being active like IGBTs and MOSFTES or

passive like Diodes, increases quadratically with the number of levels [17-20]. Additionally the complexity of the control required to balance the DC link capacitor voltages, increases significantly with number of levels. Therefore, Diode Clamped Multilevel Converter, is only practical for low number of levels. That is the why the adoption of Diode Clamped Multilevel Converter in HVDC applications was limited to only three levels, while connecting a large number of IGBTs in series to withstand the high voltage bus.



a) DC-AC (3Phase – 5 level)
Figure 1-3. Diode Clamped Multilevel Converter

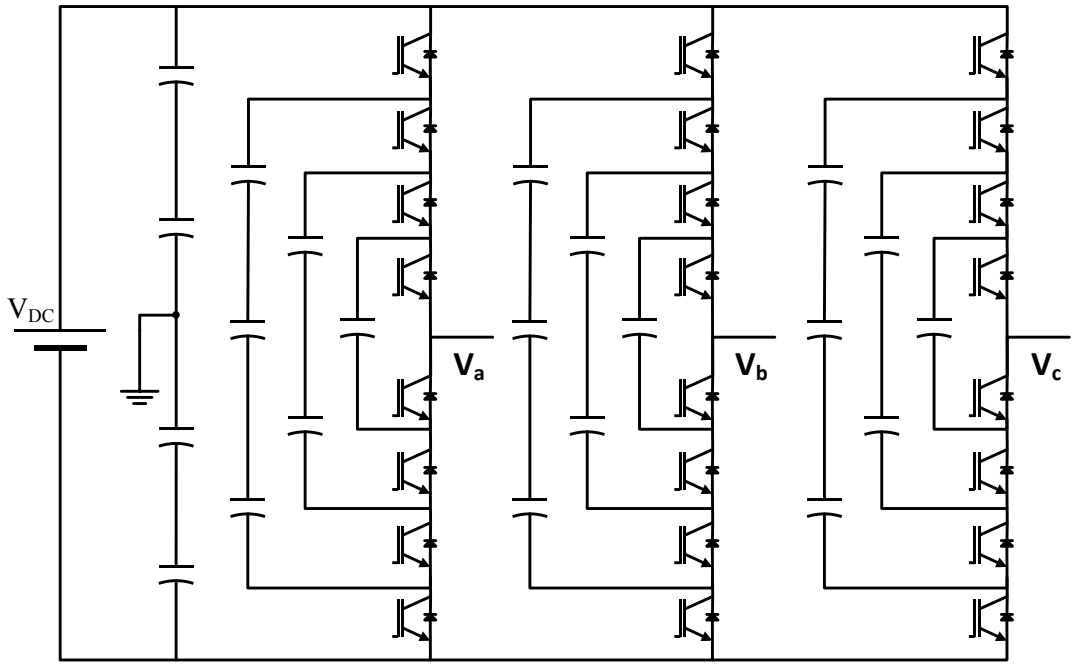


b) DC-AC (5 level)

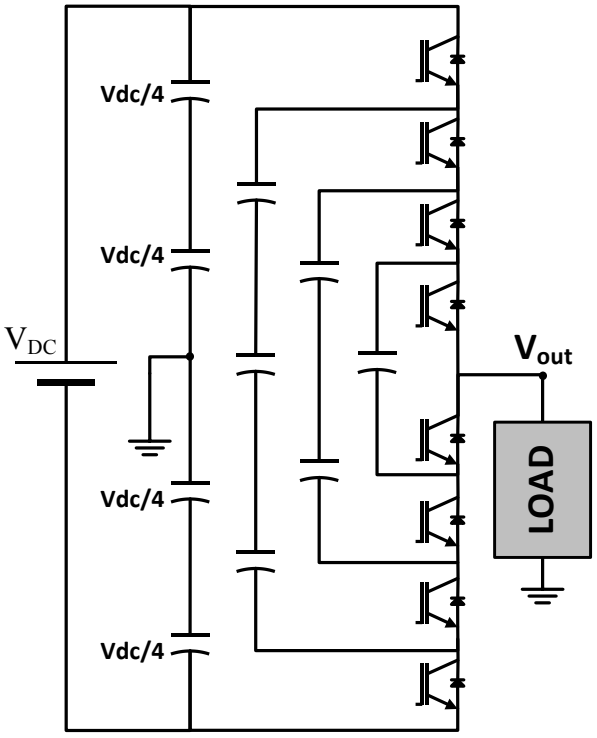
Figure 1-3. Continued

1.2.1.2 Capacitor Clamped Multilevel Converter CCMC

In Capacitor Clamped Multilevel Converter, Figure 1-4, the total number of semiconductor switches required is minimal [17-20]. However, the number of clamping capacitors increases quadratically with the number of levels. These clamping capacitors are connected in series to withstand the growing voltage; hence voltage sharing across them becomes problematic. Furthermore, voltage balancing of theses clamping capacitors is a challenging control objective especially with high number of levels. For these reasons Capacitor Clamped Multilevel Converter, are not feasible in high voltage applications.



a) DC-AC (3Phase – 5 level)



b) DC-AC (5 level)

Figure 1-4. Capacitor Clamped Multilevel Converter

1.2.1.3 Modular Multilevel Converters MMC

The foremost advantage of the Modular Multilevel Converter is true Modularity that enables its implementation at high voltage by increasing the number of levels as needed. Second it can be operated at low switching frequencies, thus achieving high efficiency. On the other hand, it has two major drawbacks, the first is the large capacitance required to minimize the voltage ripple on each submodule. These voltage ripples occur at the fundamental frequency of the output voltage and current (50 or 60 Hz) for the submodule based on half bridge, Figure 1-5(a), or double the fundamental frequency for the submodule based on half bridge, Figure 1-5(b). The amplitude of these voltage ripples is inverse proportional to the fundamental frequency of the output voltage and current, hence, capacitor size becomes extremely large if the target fundamental frequency becomes low. Consequently, MMC are not favorable in applications like adjustable speed drives where low frequency is needed because of the capacitance size prohibitive requirement. Obviously, the same limitation holds for DC-DC conversion, which can be overcome by using two MMC conversion stages with a high frequency isolation transformer as in [26], Figure 1-6, gaining isolation advantage at the expense of extra losses and larger structure. Another high step-up/down ratio isolated MMC DC-DC converter topology based on resonant operation is introduced in [27] for battery energy storage systems in microgrids.

In [28], a technique to control MMC to achieve DC-DC conversion without the use of transformers is proposed. It has bidirectional conversion ability and provides a

large step-up ratio. However, the MMC converter in [28] exhibits relatively high losses because of the high ac current due to the resonant operation in the submodules.

The second drawback of MMC is the complexity of the control algorithm responsible for balancing the capacitor voltages of all the submodules while minimizing the circulating current between the phases, especially with large number of levels, i.e. submodules.

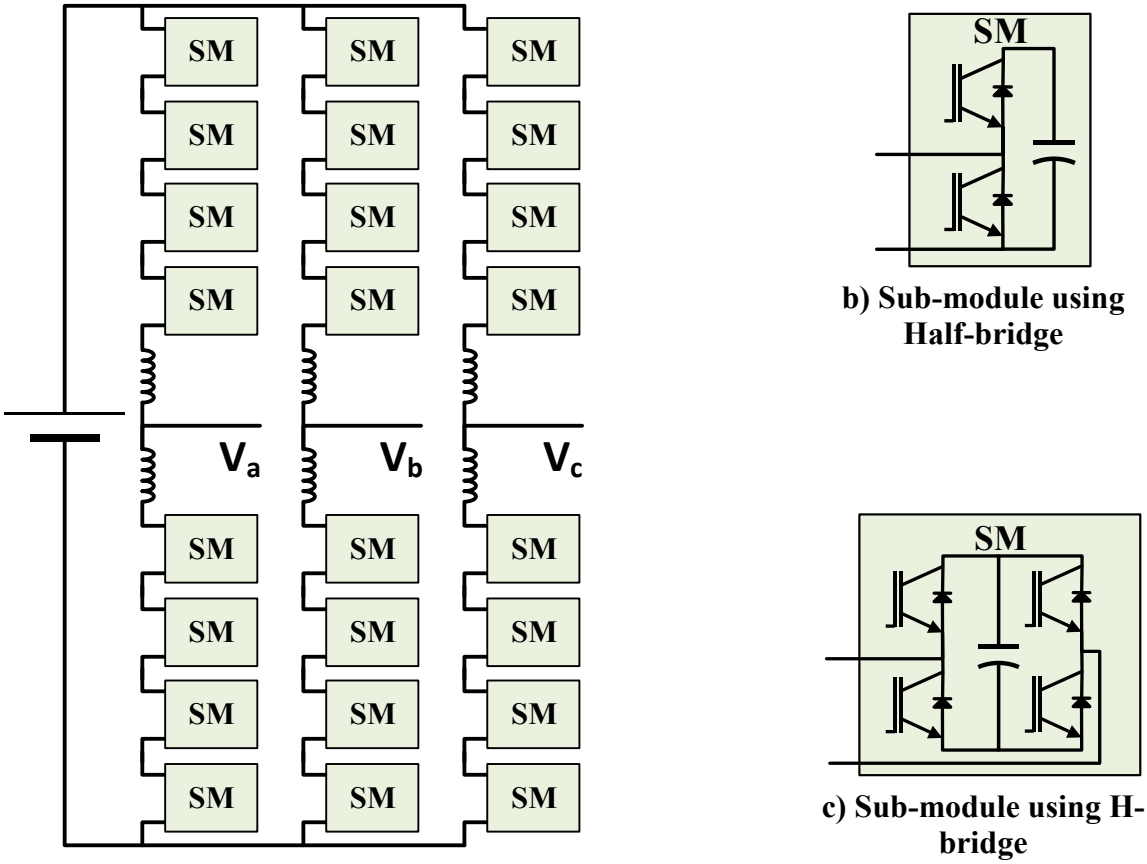


Figure 1-5. Modular Multilevel Converter (MMC) DC-AC (3 phase 5 level)

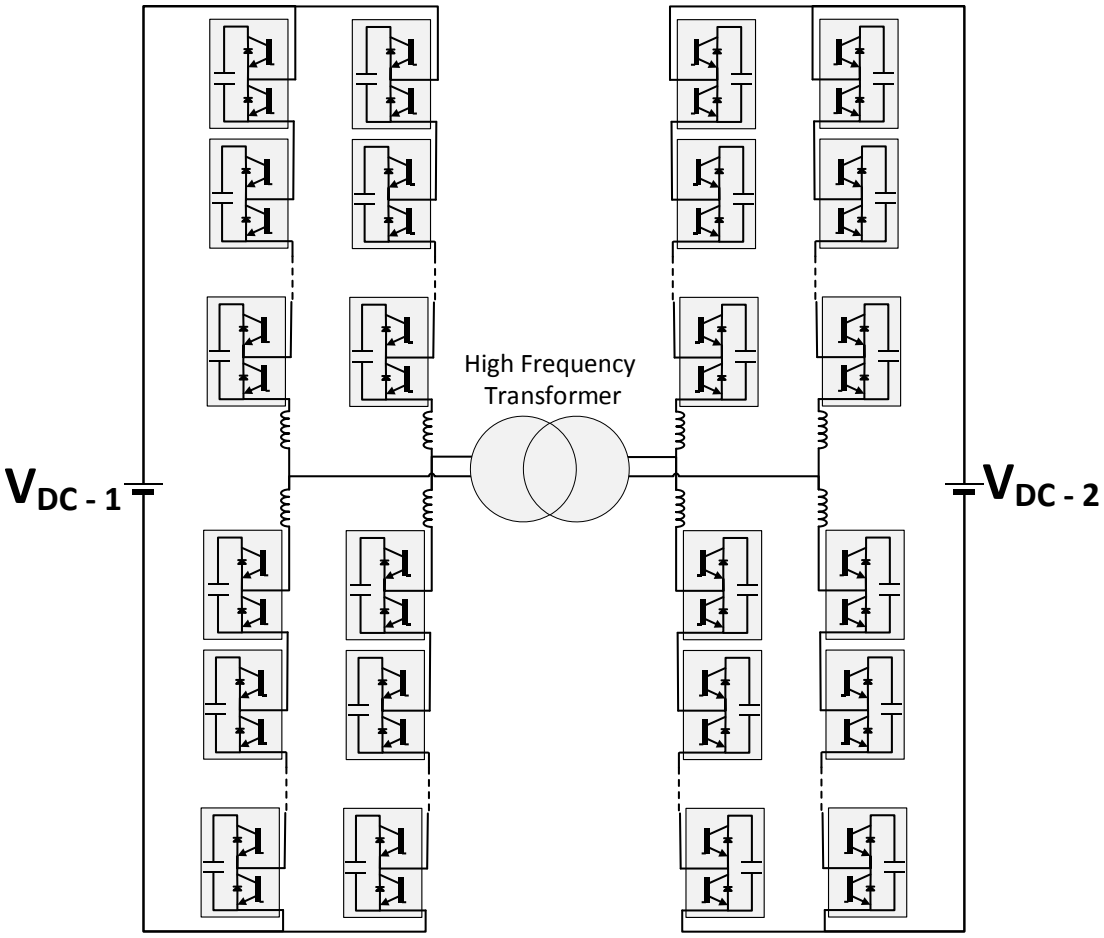


Figure 1-6. MMC-based DC transformer for high-voltage high-power applications.

1.2.1.4 Multilevel Modular Capacitor Clamped DC-DC Converter

A Multilevel Modular DC-DC inductor-free structure topology, based on combining capacitor-clamped and switched capacitor concepts, is proposed in [29-31], Figure 1-7. This converter has flexible conversion ratio which is suitable for power management of fuel cell or automotive applications. However, its switched capacitor operation makes it applicable for low power only. Additionally, capacitor voltages are

not equal, thus it does not have full Modularity/scalability and not suitable for high voltage.

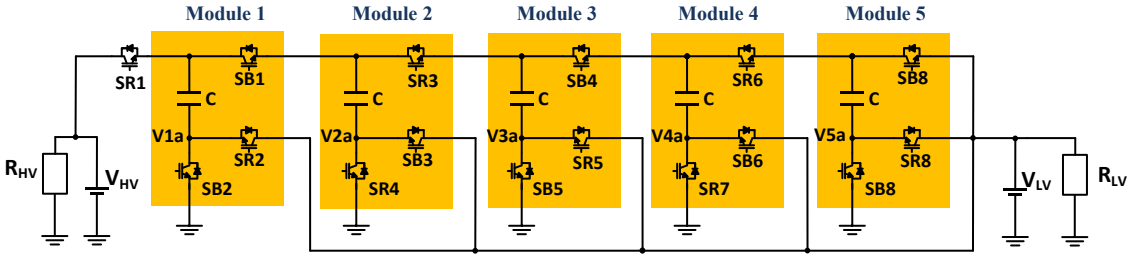


Figure 1-7. A Multilevel Modular Capacitor Clamped DC-DC Converter

1.3 Research Objective

The goal of this thesis is to overcome a set of roadblocks towards reaching power converters characterized by high efficiency and high power density; whether it be for single phase applications like Photovoltaic solar energy harvesting and uninterruptible power supplies UPS, or Multilevel converters essential for high voltage applications like DC-DC conversion in wind farms collection grids, or DC-AC conversion in medium voltage adjustable speed motor drives.

The first main objective of this research is to propose an active decoupling topology and control method in order to replace the bulky inefficient unreliable electrolytic capacitors conventionally used in single phase inverters/converters to minimize double line frequency ripples. Another related objective is to provide a comprehensive comparison with other active power decoupling methods in terms of semiconductor devices used, sizing of the decoupling capacitor and filter inductor, and

overall volume and losses. The comparison is projected on Wide Band Gap semiconductor devices available in market like SiC and GaN FETs. To validate the proposed topology and control method a 2kW single phase inverter prototype with a power density of 58W/inch^3 is presented.

The second objective is to introduce a new class of multilevel converters named Interconnected Modular Multilevel Converter (IMMC), befitting high voltage, high power applications with a blend of modularity, scalability, control simplicity, high efficiency and high power density. This IMMC is presented with two versions of submodules, which are theoretically analyzed and compared in terms of power density and dynamic behavior. A soft switching approach for the favored submodule version is then proposed and experimentally implemented demonstrating a combination of high power density with high efficiency. An experimental prototype of DC-DC IMMC with voltage scale ratio of 5:1 is built signifying the fast dynamic behavior in bidirectional power flow.

The third objective is to extend the operation of the proposed IMMC into DC-AC conversion. The proposed DC-AC IMMC diminishes the required bulky capacitors associated with the conventional MMC hence allowing unprecedented levels of power density in high voltage power converters. Modulation methods are presented and then experimentally verified showing smooth output voltages and currents without the installing additional output filters. The DC-AC IMMC prototype undergoes various testing scenarios of sudden changes in voltage, frequency and loading conditions.

1.4 Organization of the Thesis

The content of this dissertation are organized in five sections in the following manner. Section 1 introduces the need for high efficiency and high power density in single phase power converters and how Wide Band Gap semiconductor devices are one of the forefront players to fulfill this need. Then, multilevel converters are presented as a primary solution for high power density in high voltage high power applications. Some of the most important multilevel converter topologies are briefly reviewed. Finally, research objectives are presented.

Section 2 focuses on high power density for single phase converters exploiting Wide Band Gap Devices. First, traditional active and passive power decoupling methods to minimize/cancel DC current ripples are evaluated and then compared with the proposed alternative topology. The comparison entails semiconductor devices used, required size of decoupling capacitor for the different methods, required size by the magnetic components and overall size and losses. The control strategy for the proposed decoupling method is also presented. Moreover, the experimental results for 2kW single phase inverter with 58W/inch^3 prototype are presented.

Section 3 introduces a new multilevel converter concept named Interconnected Modular Multilevel Converter (IMMC), where it is applied in DC-DC conversion mode. Two submodule topologies are evaluated showing significant advantage of the later in terms of power density and fast dynamics. Additionally a soft switching algorithm for the selected submodule topology is proposed to combine high power density with high

efficiency. Finally, experimental validation of the proposed IMMC with a scaled down prototype is presented, showing bidirectional power flow capability.

Section 4 discusses the employing the proposed Interconnected Modular Multilevel Converter (IMMC) in DC-AC conversion mode. Modulation methods are then presented to control output voltage waveform arbitrarily. Additionally, the proposed topology is mathematically analyzed and modeled. Afterwards a comparison between Multilevel converter topologies is carried out highlighting the feasibility of the proposed IMMC in high voltage applications, thanks to combining low component count with high power density. Another experimental DC-AC IMMC prototype is presented illustrating its performance for arbitrary voltage waveforms and frequencies, and dynamic response under active and reactive loads.

2 HIGH POWER DENSITY SINGLE PHASE INVERTERS USING ACTIVE POWER DECOUPLING AND WIDE BAND GAP DEVICES [*]

2.1 Introduction

This section presents a comparison between mitigation techniques for double line frequency ripples in single phase micro-inverters based on Wide Band Gap FETS. A topology based on an auxiliary DC-AC stage is adopted based on optimizing both power density and efficiency to achieve the pressing needs for the next generation of micro-inverters as announced by Google's Little Box Challenge. An accurate yet simple control algorithm is proposed that provides a ripple-free DC current. Experimental results demonstrate the effectiveness of the presented topology and control algorithm to achieve high power density micro-inverter rated at 2kW.

2.2 Comparison Between WBG Devices Available in Market

Initially GaN based MOSFETs were commercially available for low voltage ratings (100-200V) like EPC-2010 (see Table 2-1), which restricts their use in low voltage applications or dictates utilizing them in multilevel topologies with intricate design and control complexity. Consequently, GaN FETS are not yet reported to be

---

[*] Reprinted with permission from:
"High power density single phase inverter using GaN FETS and active power decoupling for Google Little Box Challenge" by A. S. Morsy, M Bayern and P Enjeti, 2015. IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA), pp. 323-327. Copyright 2015 by IEEE.
"Comparison of Active Power Decoupling Methods for High Power Density Single Phase Inverters Using Wide band Gap FETS for Google Little Box Challenge," by A. Morsy and P. Enjeti, 2016, IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 4, pp. 790-798. Copyright 2016 by IEEE

utilized in multilevel topologies, to the best of the authors' knowledge. On the other hand, 600V GaN MOSFET from Transphorm was already available in market since 2012, but in standard packages that do not fully exploit the speed of GaN due to their relatively high inductance, in addition to their non-zero reverse recovery charge which is accomplished by other GaN MOSFET manufacturers. In 2014, 650V GaN FETS from GaN Systems reached the market in specially designed surface mount package minimizing inductance and facilitating thermal conductivity, hence placing them as the best candidates for higher voltage applications when cost is not the primary factor. GaN FETs present the best figure of merit (FOM = $R_{DS(ON)}$ x Q_{GD}), thus they achieve lowest conduction and switching losses, compared to traditional silicon transistors and other WBG devices like SiC, Table 2-1. Therefore, GaN FETS are the most favorable solution in order to achieve high power density for low voltage (110~240V) single phase inverters. This will tip the scale towards using 650V GaN FETS and will direct the selection of APD topology.

The third generation 900 V SiC-MOSFET C3M0065090J from Wolfspeed is a outstanding step after the second generation C2M0280120D and it is comparable to, if not better than, 600V GaN-HEMT TPH3205WS from Transphorm, especially because of C3M0065090J higher voltage rating. However, for the needed voltage operating range, the 650V eGaN-FET GS66508P from GaN Systems demonstrates the lowest FOM.

Table 2-1. Comparison between WBG Devices Available in Market

	SiC			**GaN**		
	ROHM Semiconductor SiC-MOSFET SCT2120AF	**Wolfspeed SiC-MOSFET C3M0065090J**	**Wolfspeed SiC-MOSFET C2M0280120D**	**Efficient Power Conversion eGaN-FET EPC-2010**	**Transphorm GaN-HEMT TPH3205WS**	**GaN Systems eGaN-FET GS66508P**
Datasheet	[32]	[33]	[34]	[35]	[36]	[37]
V_{DS}	650V	900V	1200V	200V	600V	650V
I_D Continuous (25°C)	29 A	35 A	10 A	12 A	36 A	30 A
Package	TO220AB	7L D2PAK	TO-247-3	Bare die 3.5x1.6 (mm)	TO-247	GaNPX™ 10x8.63 mm
$R_{DS(ON)}$ (T_J =25°C)	120 mΩ	65 mΩ	280 mΩ	18 mΩ	52 mΩ	52 mΩ
Input Capacitance C_{ISS}	1200pF	660 pF	259 pF	480pF	2150pF	260pF
Output Capacitance C_{OSS}	90pF	60 pF	23 pF	270pF	119pF	65pF
Reverse Recovery Charge Q_{RR}	53nC	131 nC	70nC	0	136 nC	0 nC
Total Gate Charge $Q_{G(TOT)}$	61nC	30 nC	20.4nC	5nC	27nC	6.5 nC
Gate Charge Q_{GD}	21nC	12nC	7.6nC	1.7nC	6nC	1.8nC
Thermal Resistance $R_{\Theta JC}$	0.7 °C/W	1.1 °C/W	1.8 °C/W	2.4 °C/W	1 °C/W	0.5 °C/W
Figure of Merit FOM (Q_{GD}×$R_{DS(ON)}$)	2520	780	2128	30.6	312	93.6

2.3 Passive and Active Power Decoupling Methods

2.3.1 Passive Decoupling

For 20% ripple voltage on the input VDC , the decoupling DC capacitor is 1.3mF at 500VDC. Its size is 12 inch3 (200cm3) using electrolytic capacitors, 1/3 of the total inverter volume (40 inch3) required by Google. Using active decoupling can reduce the volume by half.

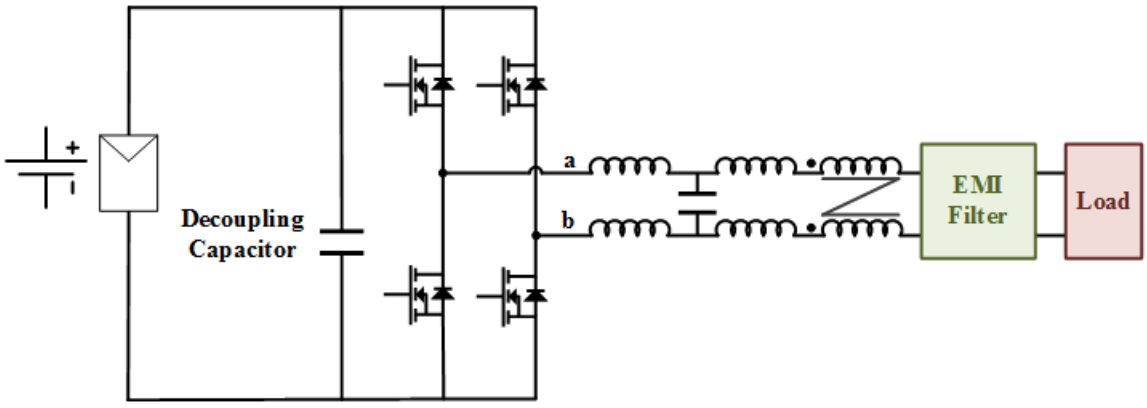


Figure 2-1. Single phase inverter with passive decoupling for double line frequency ripple compensation

2.3.2 Traditional Active Decoupling Methods in Literature

Active decoupling methods take several forms and they can be categorized into two main families; DC-DC converters [9, 11], or DC-AC converters [6, 8, 11-13] to name a few:

2.3.2.1 DC-DC buck converter (Figure 2-2(a))

The power ripple is trapped in low voltage decoupling capacitor [11]. The low voltage side capacitor is controlled to charge and discharge so that the second order ripple is cancelled. However, DC voltage offset is essential to facilitate closed loop control and tracking of high-order harmonics in such under-damped system [11]. Therefore, the capacitor voltage does not fully discharge every cycle, which means that the capacitor is not fully utilized.

It is shown in subsection 2.5 that the filter inductor used in DC-DC buck converter case does not provide the smallest volume; hence it is not the optimal solution for power density.

2.3.2.2 DC-DC Boost converter (Figure 2-2 (b))

The power ripple is cycled through high voltage decoupling capacitor [9]. The decoupling capacitor here carries a significant DC voltage in addition to the AC ripple component. This results in storing more energy than that is required to be cycled for power ripple which should increase the size of decoupling capacitor due to this large voltage offset. However, in practice, the physical size can be smaller than other alternatives due to the high energy density of high voltage capacitors compared to their lower voltage counterparts.

This, also, imposes higher voltage rating of the FETs comprising the decoupling stage which prohibits the use of GaN FETS that are characterized by the lowest conduction and switching losses even when compared to SiC based MOSFETs.

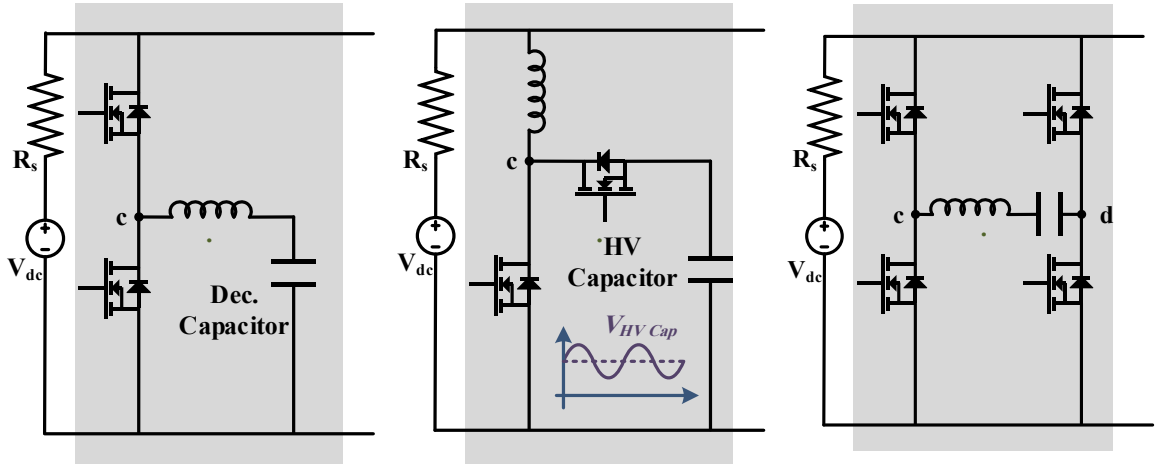
It is also reflected as additional size and losses of the inductor filter used because the switching frequency is reduced due to the use of SiC instead of GaN.

2.3.2.3 DC-AC inverter full H-Bridge (Figure 2-2 (c))

Adding a DC-AC inverter full H-Bridge with small filter and a decoupling AC Capacitor and controlling the reactive power on this port to match the power ripple on the main load [7].

The advantage here is that the decoupling capacitor only carries AC voltage to cycle the power ripple so the stored energy is minimal and is optimally matching the required power ripple.

The higher effective switching frequency of the full bridge allows minimizing the filter size in addition to the minimal energy storage requirement of decoupling capacitor.



a) DC-DC buck converter [11] **b) DC-DC Boost converter [9]** **c) DC-AC full bridge [7]**

Figure 2-2. Active decoupling methods in literature

The disadvantage is that this active decoupling method requires full bridge instead of two switches (in DC-DC cases 1,2), which means increased cost, complexity, and losses.

2.4 Proposed Active Decoupling Approach

This work [12, 13], proposes a simple and efficient approach to address the 120Hz ripple based on adopting a GaN-based three-phase inverter topology, as shown in Figure 2-3 similar to [8]. The main AC load is connected between lines a, b and decoupling capacitor is connected between lines b, c. The proposed approach combines the advantages of cases 1, 2 and 3:

- The decoupling capacitor is carrying AC voltage only, i.e. storing energy to cycle the power ripple only. Thus its size is minimal.
- Only two switches are used for the decoupling stage. These switches have the same voltage and current ratings as the switches used for the main DC-AC inverter, hence high efficiency GaN FETS can be utilized enabling faster switching with lower losses and higher density.
- By properly choosing the current (phase and amplitude) in the third leg (decoupling stage), the current in the three phases will be close to balanced case and this will evenly distribute the power dissipation on the switches as shown in subsection 2.7.
- The size of the filter inductor used for decoupling stage is also of minimal size thanks to the higher effective switching frequency seen be the filter inductor and low voltage stress, similar to DC-AC full bridge case.

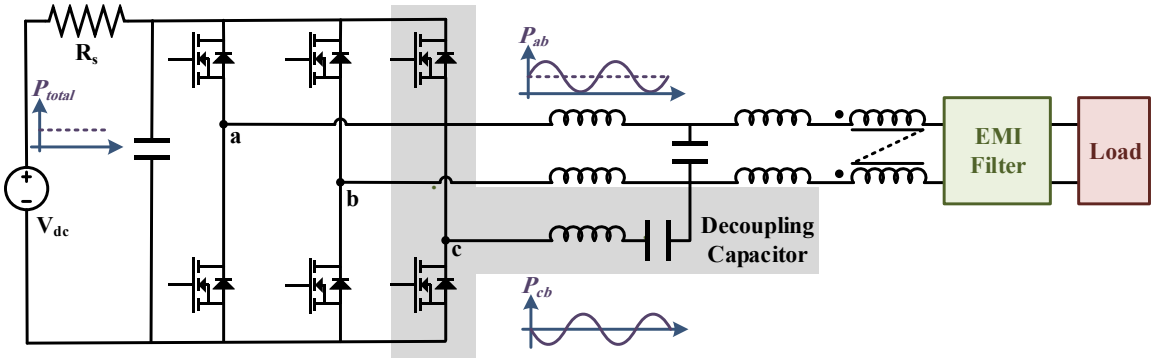


Figure 2-3. Proposed active power decoupling for Google Little Box Challenge GaN-Based Single Phase Inverter with Active Decoupling Stage for double line frequency Ripple Compensation

2.5 Comparison of Active Power Decoupling Methods

2.5.1 Semiconductor Devices

In this subsection detailed design steps are presented for the selected APD methods. The system specifications are based on Google Little Box Challenge [1], i.e. 450V DC Supply Voltage with supply series resistance of 10Ω and single phase load rated at 240V and 2kVA. Table 2-2 starts with the operating voltage range of the decoupling capacitor and the best semiconductor power MOSFET candidate that can combine high efficiency with fast switching, hence allowing high power density. 650V GaN MOSFET GS66508P can be used for all topologies except for the DC-DC boost case whose operating voltage reaches 800V, thus needs a high voltage device like the 1200V SiC C2M0280120D to allow for safer operation and accommodate for voltage overshoot that occurs during switching. Since GaN FETS have lower switching losses compared to SiC MOSFETs [38], they should be operated at different switching

frequencies so as to have comparable switching losses and fair sizing and loss comparison between all the topologies under study. As shown below, the selected GaN and SiC devices would experience similar switching losses when operated at 100kHz and 30kHz respectively.

Unlike GaN FETs, SiC MOSFETs have non-zero reverse recovery losses, thus the switching losses for SiC MOSFET (**C2M0280120D**) used in the DC-DC boost converter case can be calculated as $P_{switching} = (C_{oss}\, V_{in}^2 + Q_{rr}\, V_{in}) f_{sw} = \left(23pF \times 800^2 + 70nC\left(\frac{3A}{10A}\right) \times 800V\right) \times 30kHz = 1.45W.$

The switching losses for GaN (**GS66508P)** used in the rest of the active decoupling topologies at 100 kHz can be calculated as $P_{switching} = C_{oss}\, V_{in}^2\, f_{sw} = 65pF \times 450^2 \times 100kHz = 1.316W$. The power losses in gate drives in both devices are much lower and can be neglected here.

The peak decoupling current (excluding ripples) can be computed from equations (2-1) and (2-2) for DC-DC and DC-AC decoupling methods [9]. The boost converter APD minimizes the decoupling current and is advantageous in terms of semiconductor conduction losses over other APD methods. It is noted that the decoupling current is directly proportional to the power ripple in the DC-DC cases, but proportional to the square root of power ripple in the DC-AC cases, which allows lower conduction losses (2-3) at light loads in the DC-DC APD cases.

The selected devices are chosen such that their actual peak current is about 1/3 of their nominal current rating at room temperature. Therefore 10 A SiC MOSFET (**C2M0280120D**) is selected for DC-DC Boost converter whose actual operating peak

current is around 3A while 30 A GaN FET (**GS66508P**) is selected for an actual peak current of about 8 to 10A in the other decoupling cases as in Table 2-2.

Table 2-2. Comparison of APD Methods - Semiconductor Devices

Active Decoupling Topology	**DC-DC Buck converter [11]**	**DC-DC Boost converter [9]**	**DC-AC full bridge [7]**	**Proposed Active Power Decoupling [12, 13]**
Operating Voltage range	150V – 350V	480V – 800V GaN is not an option	0V – 350V	
Selected Semiconductor device for decoupling phase	650V GaN GS66508P	1200V SiC C2M0280120D	650V GaN GS66508P	650V GaN GS66508P
Switching frequency (kHz)	100	30	100	100
$R_{DS(ON)}$ (mΩ) (@T_J =25°C)	52	280	52	52
Number of devices	2	2	4	2
Peak decoupling current (A)	$I_{pk} \cong \frac{P}{V_{mean}} = \frac{P}{\frac{1}{2}(V_{max} + V_{min})}$ (2-1)		$I_{pk} = \sqrt{2}\sqrt{P\,\omega C}$ (2-2)	
$\boldsymbol{I_{pk}}$ **@ 100% load**	8	3.125	10.27	
$\boldsymbol{I_{pk}}$ **@ 25% load**	2	0.78125	5.13	
Semiconductor Condcution losses (mW)	$\frac{I_{pk}^2}{2}\Big\vert_{\%\,Load} \times R_{DS(on)} \frac{\#of devices}{2}$ (2-3)			
@ 100% load	1664	1370	5480	2740
@ 25% load	104	85	1370	684

2.5.2 Decoupling Capacitor

As discussed in subsections II and III, energy storage requirements in the decoupling capacitor of DC-DC APD cases are higher than in the DC-AC ones, primarily due to the DC offset voltage in the DC-DC converters specially the boost case where the offset is larger. However, the required physical size of the decoupling capacitor, as shown in the selected capacitors in Table 2-3, is smallest in case of DC-DC boost converter APD thanks to higher energy densities for high voltage capacitors compared to their lower voltage counterparts. This was the motivation in [9] to favor the boost converter APD over other methods to achieve high power density. However, the study in [9] lacked a comprehensive comparison that also take into account the size requirement for the filter inductor and how it affects the overall power density of the converter which is aimed in this work.

Table 2-3. Comparison of APD Methods - Decoupling Capacitor

Active Decoupling Topology	**DC-DC Buck converter [9]**	**DC-DC Boost converter [11]**	**DC-AC full bridge [9]**	**Proposed Active Power Decoupling [12, 13]**
Operating Voltage range	150V – 350V	480V – 800V	0V – 350V	
Required Capacitance (μF)	106	25.9	70	
Capacitor stored Energy $= \frac{1}{2} C V_{max}^{2}$ (J)	6.49	9.6	4.2875	
Actual capacitor selected	B32778G4107K 450V, 100μF	B32776E8306K 800V, 30μF	B32778G4756K 450V, 75μF	
Dimensions (mm)	57.5×35×50	42×30×45	57.5× 30.0× 45.0	
Volume occupied by C cm^3	100.625	56.7	77.6	

2.5.3 Inductor Filter Design and Losses

Table 2-4 demonstrates the design and sizing of the filter inductor in the four topologies under study for the same allowable percentage in ripple current. The inductance required for filtering in the DC-AC cases is the absolute lowest thanks to higher effective switching frequency and the low voltage stress seen by the inductors. On the other hand, the DC-DC boost converter suffers from the highest inductance which is directly reflected on the energy storage requirements in the filter inductor, hence, primarily defining its size. The same core material (Molypermalloy MPP with relative permeability of μ_r=60) is selected for all four topologies to provide a good venue of minimizing filter size and losses while ensuring fair comparison between them. The volume occupied by the filter inductor in DC-DC boost converter and buck converter APD topologies are 2.5 and 1.66 times larger than the filter inductor size in DC-AC APD cases as demonstrated in Table 2-4. This highlights the significance of the inductor filter size in addition to that of the decoupling capacitor in order to truly evaluate power densities of these alternative APD solutions.

The same current density is used in the selection of wire sizes for all inductor designs for a fair comparison. Coil winding resistance is then calculated based on the number of turns, core dimensions and wire size. Accordingly copper losses are estimated at 100% and 25% loading conditions. The winding copper loss for the boost converter and buck converter APD cases are 2.5 and 1.4 times higher compared to copper loss in DC-AC APD cases at full load. However, at 25% loading, winding copper loss in DC-DC APD cases becomes lower than that in DC-AC APD cases.

Although the semiconductor conduction losses were the lowest in DC-DC Boost converter case (Table 2-2), their winding copper losses are the highest among other decoupling options (Table 2-4), hence, the overall losses for DC-DC Boost converter case are similar to the proposed DC-AC decoupling case leaving the Boost case less competitive in terms of volume (Table 2-5).

Comparison between APD topologies in terms of core power losses is also demonstrated in Table 2-4. The flux density maximum ripple ΔB_{max} is calculated for all topologies (2-4), then the expected core power loss is estimated for each case (2-5) using Steinmetz Equation parameters of MPP (μ_r=60) as in [39].

2.5.4 Overall Volume and Losses

Table 2-5 summarizes the total volume occupied by passive components of the four APD topologies under study in addition to the variable losses due winding copper loss and semiconductor conduction loss. The proposed APD topology achieves the smallest overall size of passives while using two GaN FETS. The overall size of DC-DC Boost and Buck converters APD methods are 23% and 40% larger. In terms of losses, DC-AC full bridge APD has the highest losses due to the increased number of semiconductor switches used, while the Buck converter APD case has the lowest losses. On the other hand, the Boost converter APD and the proposed topology have almost identical losses at full load. Therefore the proposed topology achieves the highest power density without sacrificing efficiency compared to other APD alternatives, thus further details on its control are discussed in the next subsection.

Table 2-4. Comparison of APD Methods - Inductor Filter Design and Losses

Active Decoupling Topology	**DC-DC Buck converter [11]**	**DC-DC Boost converter [9]**	**DC-AC full bridge [7]**	**Proposed Active Power Decoupling [12, 13]**
Required inductance L Where, $\Delta i = 20\%\, I_{pk}$	$L_{buck} = \frac{450V}{4\Delta i F_{sw}}$ Medium 703.125µH	$L_{boost} = \frac{800V}{4\Delta i F_{sw}}$ Largest 10.67mH	$L_{DC-AC} = \frac{450V}{8\Delta i F_{sw}}$ Smallest 273.86µH	$L = \frac{450V}{8\Delta i F_{sw}}$ Smallest 273.86µH
Inductor stored Energy $\frac{1}{2}L\, i^2$ (mJ)	22.5	52.1	14.44	
Selected MPP Core (µ=60) (2 stacked)	MPP 55083	MPP 55716	MPP 55076	
Dimensions D× (2×H) mm	40.77 × (2×15.4)	51.69 × (2×14.4)	36.71 × (2×11.4)	
Total Volume occupied by L (cm^3)	51.2	76.95	30.73	
Core cross-section A_e mm^2	107	125	67.8	
Core volume (cm^3)	10.6	15.9	6.09	
A_L ($nH/Turn^2$)	81 @0AT 60 @600AT	73 @0AT 40 @1100AT	56 @0AT 43 @513AT	
Number of turns	75	350	50	
Actual Inductance L (µH)	675	9800	215	
AWG (For 500A/cm^2)	15	19	14	
Coil Resistance (mΩ)	42.6	494	18.47	
Winding Copper loss (mW) (@ 100% load)	1363	2412	974	
(@ 25% load)	85.18	150.75	243	
Flux Density ripple ΔB_{max} (mT)	$\Delta B = \frac{NA_L}{A_e}\Delta i$ (2-4)			
	67	70	65	
Core power loss at ΔB_{max} (mW)	$P_{core} = 357.1\, B_{pk}^{2.05} f^{1.12}\, Volume_{core(s)}$ (2-5)			
	1245.85	530.8	672.7	

Since the overall calculated losses for all the topologies under study are comparable at full load, they have similar cooling requirements of the same added size. Therefore, for the sake of comparison between APD alternatives, the size of passive components becomes the deterministic factor, in spite of the fact that the size of the cooling system and auxiliary circuits contributes to the inverter size and affects the overall power density.

Table 2-5. Comparison of APD methods - Overall Volume and Losses

Active Decoupling Topology	**DC-DC Buck converter [11]**	**DC-DC Boost converter [9]**	**DC-AC full bridge [7]**	**Proposed Active Power Decoupling [12, 13]**
Total volume occupied by passives L + $C_{Decoupling}$ (cm^3)	151.825	133.65	108.33	
Winding + Cond. loss (mW) @ 100% load	3027	3782	6454	3714
@ 25% load	189.18	235.75	1613	927

2.6 Control Strategy for Double-Line Frequency Harmonic Compensation

The function of the proposed active decoupling control is to match the power ripple of the load (across lines a, b) to the reactive power of the decoupling capacitor (across lines b, c). In this subsection, the voltage and current relationships that govern this power ripple compensation is derived. First, voltage, current and power on the load

connected to lines a,b are defined in (2-6), (2-7) and (2-8) taking the load voltage v_{ab} as the reference phase angle.

$$v_{ab} = V_{ab,\,max} \sin(\omega t + 0) \tag{2-6}$$

$$i_a = I_{a,\,max} \sin(\omega t + \theta_1) \tag{2-7}$$

$$P_{ab}(t) = \frac{I_{a,\,max}\, V_{ab,\,max}}{2} \left(\cos\theta_1 - \cos(2\omega t + \theta_1)\right) \tag{2-8}$$

Similarly, voltage, current and power on the active compensation ripple port (decoupling capacitor) connected to lines c,b are defined as.

$$v_{cb} = V_{cb,\,max} \sin(\omega t + \theta_2) \tag{2-9}$$

$$i_c = I_{c,\,max} \sin(\omega t + \theta_3) \tag{2-10}$$

$$P_{cb}(t) = \frac{I_{c,\,max}\, V_{cb,\,max}}{2} \left(\cos(\theta_2 - \theta_3) - \cos(2\omega t + \theta_2 + \theta_3)\right) \tag{2-11}$$

In case of low switching frequency converters (as in [7]), the inductor impedance is significant and it affects the power ripple balance. However, operating at high switching frequency using WBG devices allows for very small inductor filter, thus its impedance ($j\omega L$) becomes negligible (less than 0.5%) compared to the impedance of decoupling capacitor $1/j\omega C$. Therefore, the relationship between v_{cb} and i_{cb} can be approximated as in (2-12) and (2-13) without the need to increase the complexity of control method.

However,

$$\theta_3 \approx \theta_2 + \frac{\pi}{2} \tag{2-12}$$

$$I_{c,\,max} \approx \omega C_{decoupling}\, V_{cb,\,max} \tag{2-13}$$

In order to achieve ripple cancellation, the total power should be constant, i.e. $P_{ab}(t) + P_{cb}(t) = const$

Thus the controller should adjust the voltage v_{cb} to achieve

$$\frac{I_{c,\,max}\, V_{cb,\,max}}{2} \cos(2\omega t + \theta_2 + \theta_3) \approx -\frac{I_{a,\,max}\, V_{ab,\,max}}{2} \cos(2\omega t + \theta_1) \tag{2-14}$$

Using (2-15), we get

$$V_{cb,\,max} \approx \sqrt{\frac{I_{a,\,max}\, V_{ab,\,max}}{\omega\, C_{decoupling}}} \tag{2-15}$$

$$\theta_2 \approx \frac{\theta_1}{2} + \frac{\pi}{4} + \pi k \tag{2-16}$$

where $k = 0,\ \pm 1,\ \pm 2,\ \ldots$

The current i_a is passed through two filters as shown in Figure 2-4 to generate the two orthogonal current components $i_{a,\,\alpha}$ and $i_{a,\,\beta}$. These filters smoothen sudden variations in load current while blocking unwanted harmonics and any possible DC drift from the signal conditioning and measurements. The bandwidth of these two filters defines the control dynamics and is set to give a response time of about two fundamental cycles.

The phase angle of current i_a is estimated sample by sample from these two filtered (90° apart) current components using $\tan^{-1}\left(\frac{i_{a,\,\alpha}}{i_{a,\,\beta}}\right)$. The estimated phase angle

of current i_a is then subtracted from the load voltage reference angle ωt and adjusted between ±180° to calculate the power factor angle θ_1 from which angle θ_2 is calculated as in equation (2-16) then the line voltage $v_{cb}$is found.

This power decoupling control is characterized by simplicity and requires one current sensor only but its accuracy depends on precise knowledge of the decoupling capacitance used.

Using the line voltages (v_{ab}, 0 , v_{cb}) the zero sequence voltage is calculated based on carrier based equivalency to Space vector modulation [40]. This zero sequence voltage is then subtracted from the three line-line voltages to generate the modulating signals used by PWM generation block.

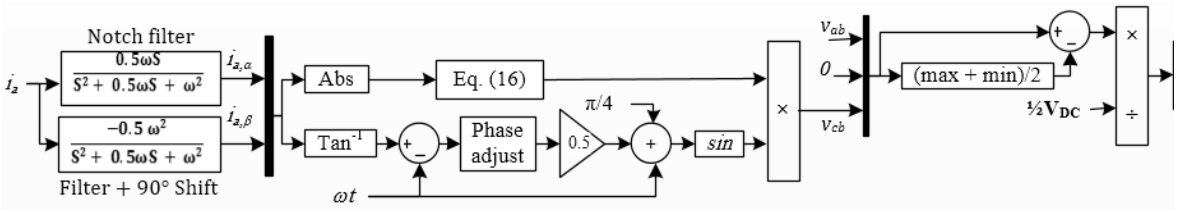


Figure 2-4. Block diagram for the proposed active decoupling control

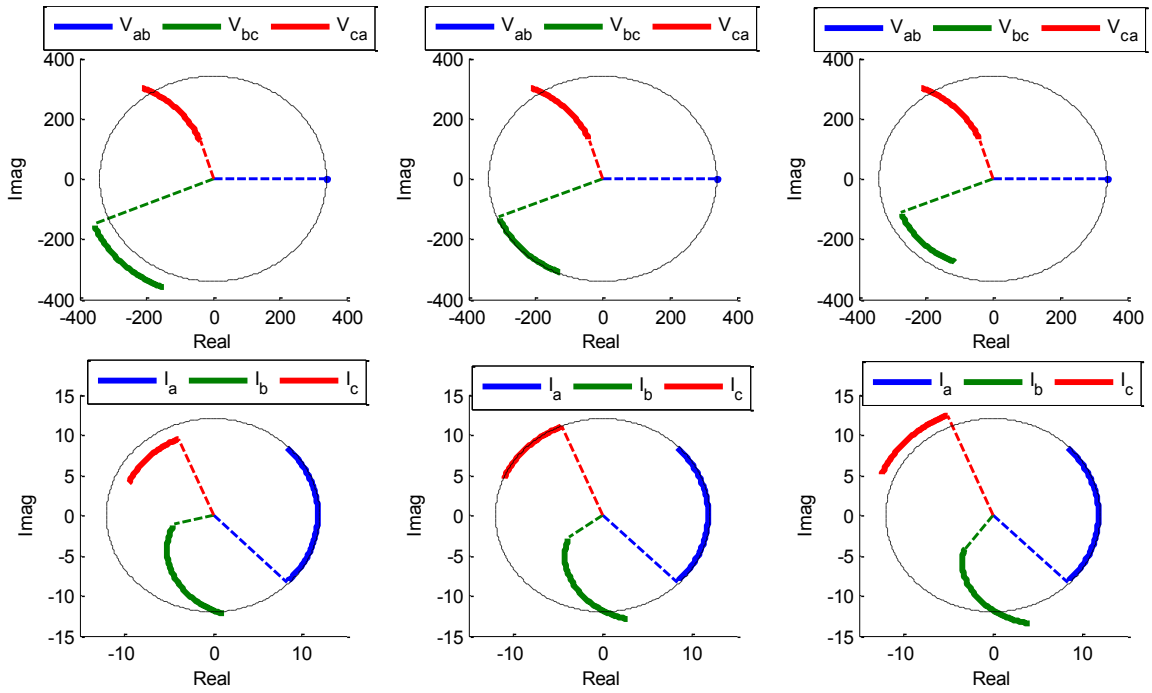
Following the relationships derived in (2-15) and (2-16), the line voltage across the decoupling capacitor can be controlled to cancel the power ripple on the DC side of the inverter. A block diagram of the proposed control is shown in Figure 2-4.

2.7 Selection of Decoupling Capacitor

The proposed topology is favored among other approaches since it allows the smallest size of passive components while keeping low voltage and current stress on the FETs of the decoupling stage. Therefore, it is important to select a decoupling capacitor that serves this good balance. Figure 2-5 shows voltage and current vector projections for the three phases with active power decoupling under rated loading (240V, 60Hz, 2kVA), while the load power factor is varied from 0.7 lag to 0.7 lead. It should be noticed that line voltages and currents demonstrate a decent level of balance with respect to their amplitudes and phase angles. This balance enables even distribution of conduction and switching losses across all three phases of inverter as well as losses associated with the inductor filters used. This balance also allows good utilization of DC link voltage without entering over-modulation region.

The selection process of the decoupling capacitor is based on optimizing the tradeoff between minimizing the conduction losses (by reducing current amplitude in decoupling phases) and reducing the required voltage on the decoupling phase to assure operation in the linear modulation region of the inverter based on available DC link voltage). This tradeoff is demonstrated in Figure 2-5 with three different values for the decoupling capacitor (70μF, 95μF, 120μF). Using low capacitance (as in 70μF case) for $C_{decoupling}$ allows low current amplitudes in phases 'b' and 'c' but this may incur over-modulation if the DC voltage supply is not high enough. On the other hand at higher values of $C_{decoupling}$ higher current are experienced but with lower DC supply voltage requirement. Based on the system rating under study at 95μF, balance is achieved

between voltages and current amplitudes across the three phases. In this particular example, the available DC link voltage is high enough (400-450V), so that lower decoupling capacitance (i.e. 80µF TDK B32778G4756K 450V as shown in Table 2-6) can still be used, while avoiding over modulation over the required power factor range of operation.



a) $C_{decoupling}$ = 70µF
Higher voltage/ lower current on the decoupling phase

b) $C_{decoupling}$ = 95µF
Good balance between voltage and current on the decoupling phase

c) $C_{decoupling}$ = 120µF
Lower voltage/ higher current on the decoupling phase

Figure 2-5. Real/Imaginary vector projection of 3 phase voltages and currents at rated loading (240V, 2kVA) while load power factor is varying between (0.7 lag to 0.7 lead). The dashed circles represent the rated load voltage and current limits.

2.8 Experimental Results

The inverter is designed and built according to the specifications set by Google Little Box Challenge [1]. Some of the key system parameters are summarized in Table 2-6. Figure 2-6 demonstrates the inverter, highlighting the GaN-based inverter, the passive filter components and the decoupling capacitor. The decoupling capacitor is only 4.74 $inch^3$ and the overall inverter size is 35.8 $inch^3$, resulting in a power density of 55.8W/ $inch^3$. The size of the cooling system and auxiliary circuits definitely contribute to the inverter size and affects the power density. The heat sink used in the proposed design is (60mm × 25mm × 24mm). The board area of the six GaN FETs and their gate drives is less than (60mm × 25mm) with minimal height (~3mm).

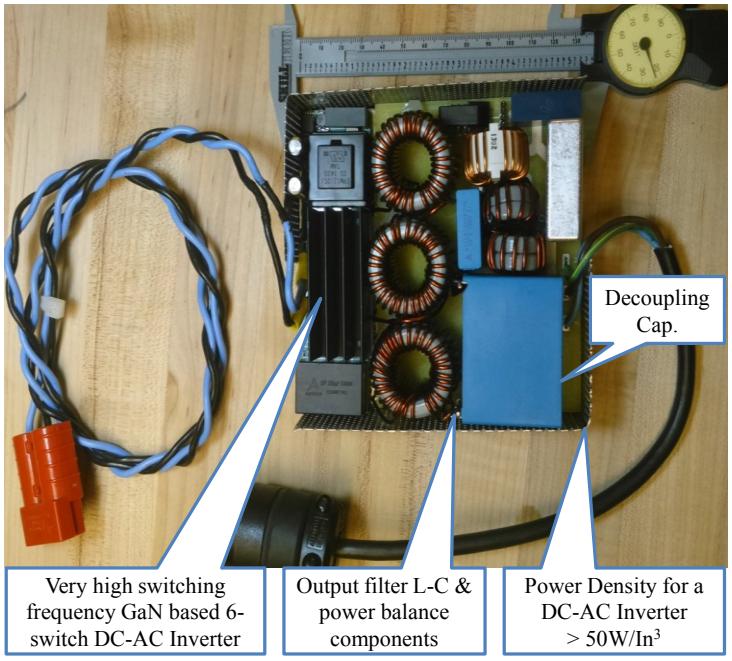


Figure 2-6. Inverter board based on the proposed APD method using GaN FETS

The steady state performance of the proposed active decoupling is shown in Figure 2-7 under 2kVA and 0.7 leading power factor, where it is clear that the DC current is ripple free and is exceeding the requirements set in [1]. The transient response is also shown in Figure 2-8 with an active load step change of (1kW to 2kW and back). Additionally, Figure 2-9 shows a reactive load step change (0 to 1kVAr and back) while feeding a constant active power of 1kW.

Table 2-6. System Parameters for Single Phase Inverter Experiment

Parameter	**Value**
DC Supply Voltage	450V
Supply series resistance	10Ω
Load voltage	240V
Load power	2kVA
GaN FETS	GS66508P-E03 650V, 30A
Decoupling capacitor	TDK B32778G4756K 450V, 80μF 57.5 x 30.0 x 45.0 (mm) = 77.6 cm^3
Inverter Side filter inductor	234μH (MPP 55076 x 2 cores) (μ=60) OD x HT = 36.71 × (2×11.4) mm
Inverter dimensions (inch)	5.3 x 5.2 x 1.3
Power density at 2 kW load	55.8 W/in^3.
Efficiency	98%

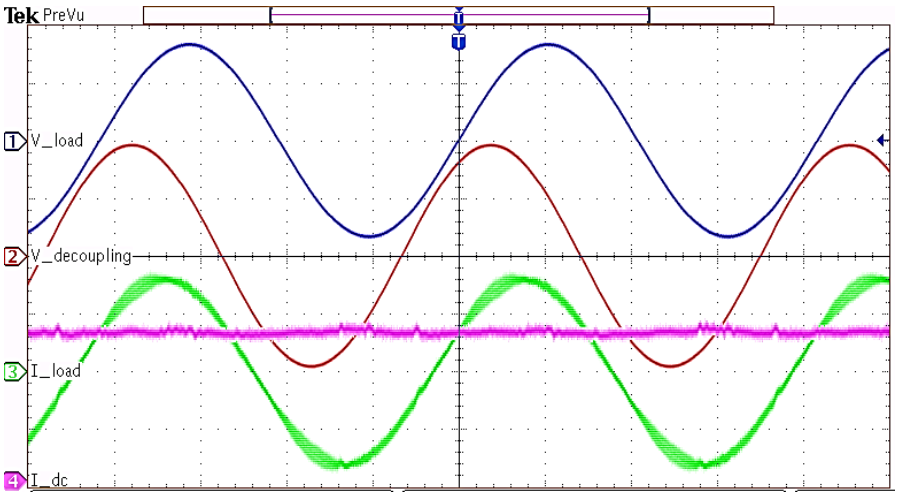


Figure 2-7. Steady state performance showing ripple free input DC current Ch. (1, 2) 200V/division, Ch. (3) 8A/division, Ch. (4) 2A/division. Time scale 4msec/division

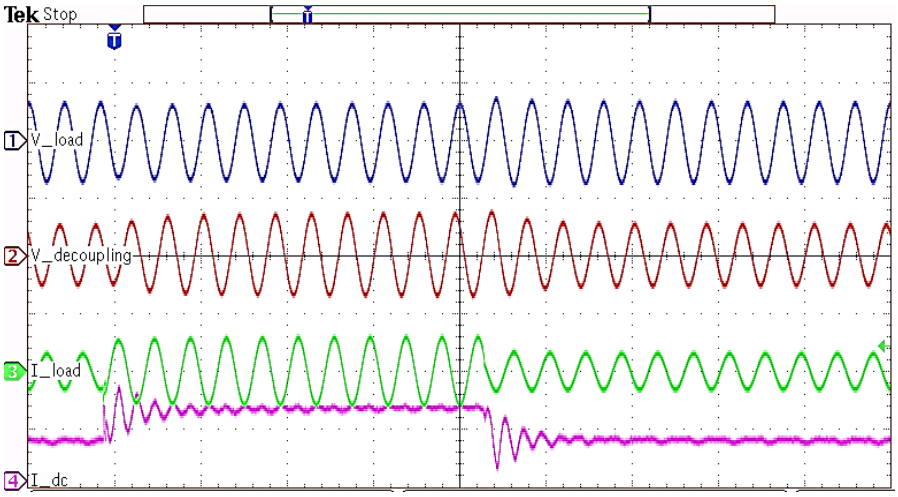


Figure 2-8. Transient response with active-load steps with the proposed active decoupling approach
Ch. (1, 2) 500V/division, Ch. (3) 20A/division, Ch. (4) 4A/division. Time scale 40msec/division

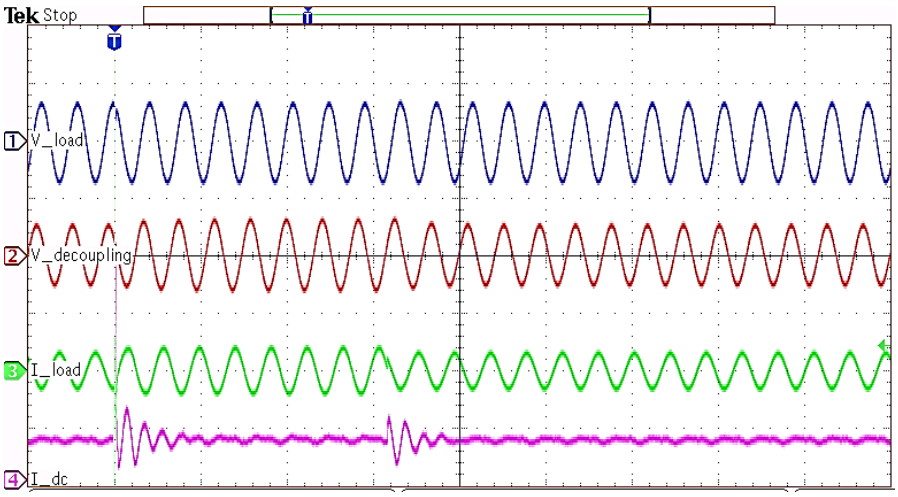


Figure 2-9. Transient response with reactive-load step with the proposed active decoupling approach
Ch. (1, 2) 500V/division, Ch. (3) 20A/division, Ch. (4) 4A/division. Time scale 40msec/division

2.9 Summary

This section has presented a comprehensive comparison between active power decoupling methods in view of power density and efficiency factors. The comparison was projected on wide band gap SiC and GaN FETS available in market. An active power decoupling topology is proposed, which achieves cancellation of the double line frequency ripples with minimal size of filter inductors and decoupling capacitors and active semiconductor components. The proposed topology better aligns with power density and efficiency constraints. A control method for active decoupling based on the selected topology has been proposed. Inverter design data and experimental results during active and reactive load transients validate the proposed topology and control. Irrespective of the nature of load transient, the controller demonstrated its capability of accurate and fast cancellation of DC current ripples.

3 HIGH POWER DENSITY DC-DC INTERCONNECTED MODULAR MULTILEVEL CONVERTER (IMMC) TOPOLOGY *

3.1 Introduction

Over the past few years, significant research efforts were directed towards developing modular multilevel DC-DC converters to address the increased adoption of DC power systems. As a result, some new configurations [21, 28-31, 41-45] of modular multilevel DC-DC converters have been proposed.

Some of these configurations like [29-31] have limited scalability and are not suitable for high power applications as mentioned in Section 1. Others, like [26, 27], are isolated DC-DC topologies which is beyond the scope of this work. On the other hand, [28] proposes a non-isolated DC-DC MMC, however, it exhibits relatively high losses because of the high ac current due to the resonant operation in the submodules.

In [41-43], a bidirectional Triangular Modular Multilevel DC-DC Converter (TMMC) based on half-bridge submodule is proposed as shown in Figure 3-1. The major limitation on [41-43] is the inherently low power density because of the significant dependence on filter inductors, as demonstrated later in this section.

An improved scheme of TMMC is hereby introduced and published in [44], Figure 3-2. The proposed scheme exploits coupled inductor structure with H-bridge that inherently minimizes the size requirement of magnetics as well as capacitive filters, thus

* Part of the data reported in this section is reprinted with permission from "A new high power density modular multilevel DC-DC converter with localized voltage balancing control for arbitrary number of levels" by A. S. Morsy, Y. Zhou and P. Enjeti, 2016. IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2567-2572. Copyright 2016 by IEEE.

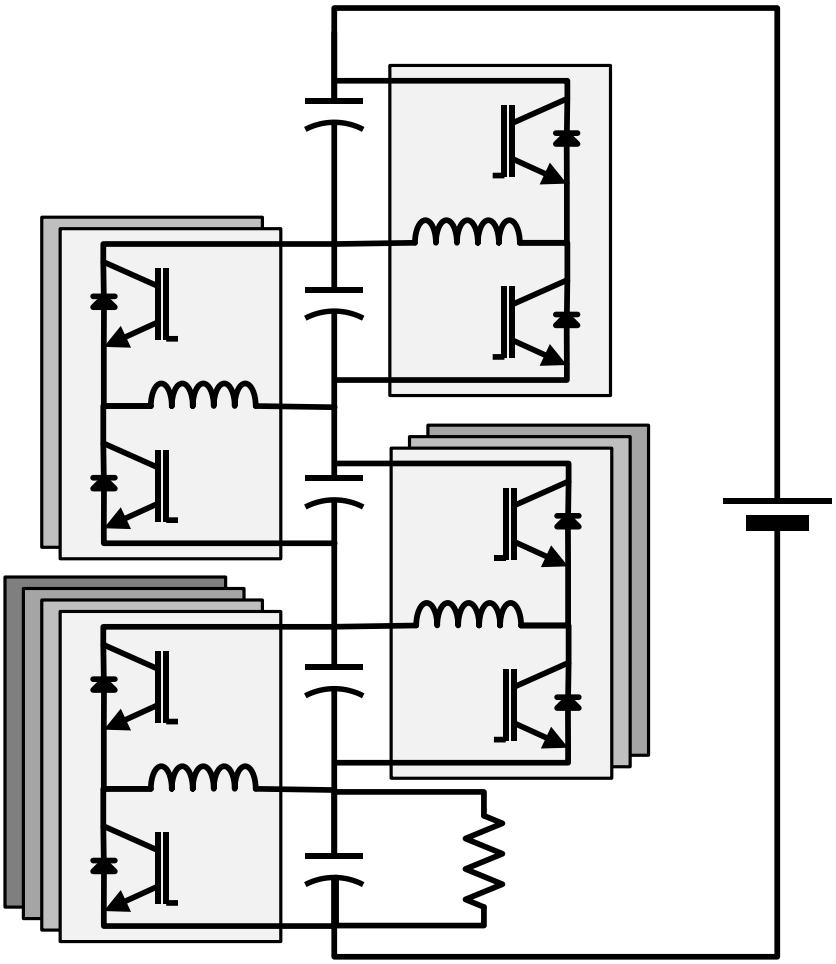
achieving high power density. Still, significant ripple reduction of inductor currents and capacitor voltages is attained. Moreover, [44] adopts a simplified localized voltage balancing control, which reduces overall system complexity and increases cost-effectiveness.

This work also introduces a zero voltage switching ZVS scheme for the proposed DC-DC IMMC, expanding the capabilities of [44]. The proposed ZVS scheme demonstrate high utilization of the semiconductor switches due to low rms current, thus, it substantially minimizes the switching and conduction losses. Additionally, the proposed ZVS scheme has low core losses due to low magnetic stresses on the coupled inductor.

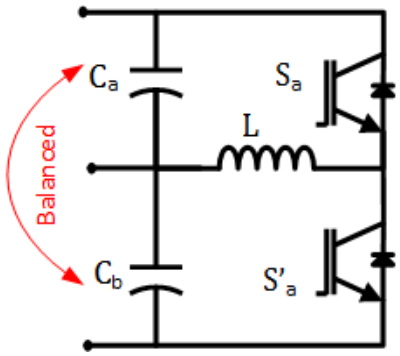
3.2 Proposed Topology

The topology of the proposed DC-DC Interconnected Modular Multilevel Converter (IMMC) is shown in Figure 3-2. Its basic concept of operation is to equally balance the voltages across the capacitors constituting the high voltage DC-link. Therefore every submodule is responsible for equalizing the voltage of the two capacitors to which it is connected. Hence all the modules are operated very close to 50% duty cycle with 180° phase shift between the two phase legs of a given submodule, making the choice of coupled inductor more feasible due to size reduction [44].

The configuration in Figure 3-1 and Figure 3-2 can be generalized to any number of levels, also the load can be tapped at any voltage level, and multiple loads/sources can be interfaced at different points. The submodules are stacked in parallel to accommodate the gradually increasing current from high voltage level to lower level.

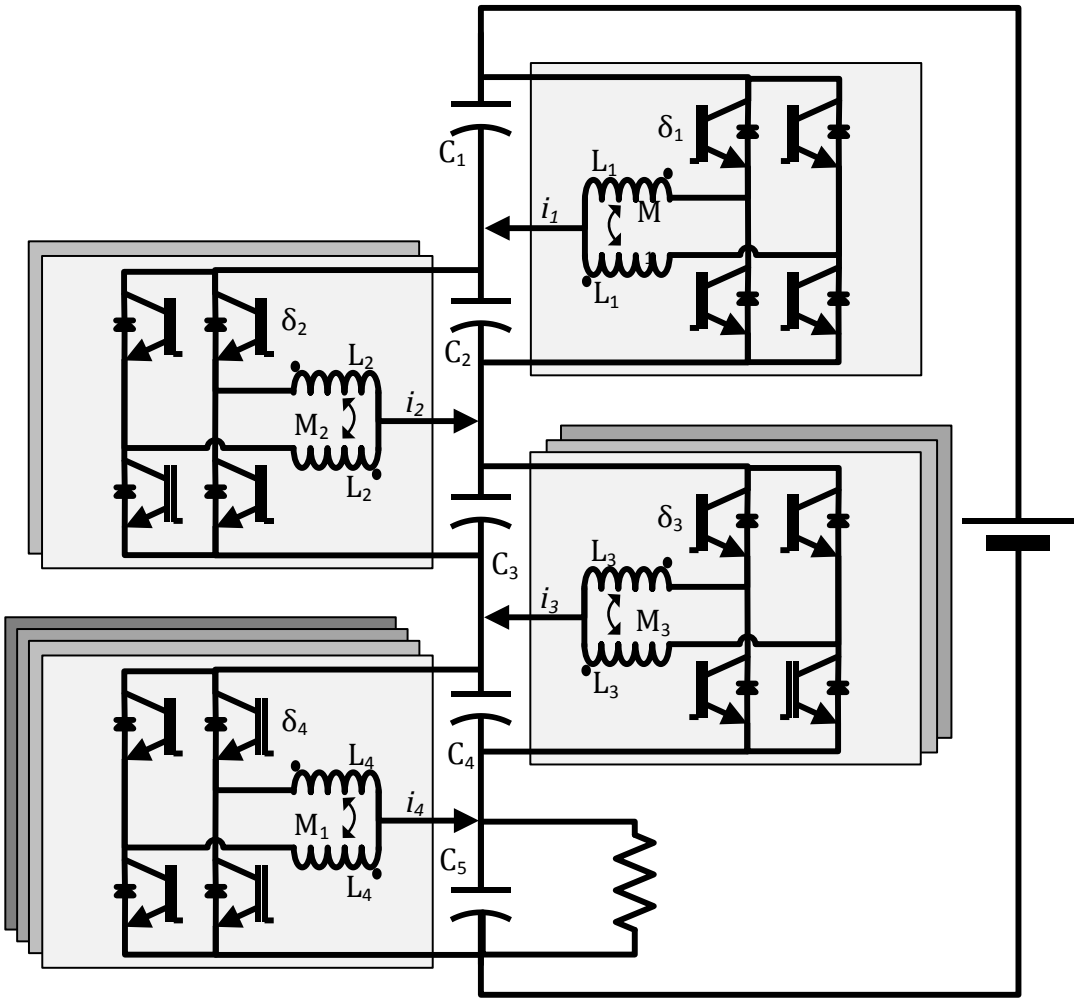


a) Overall Converter structure (Voltage ratio 5:1)

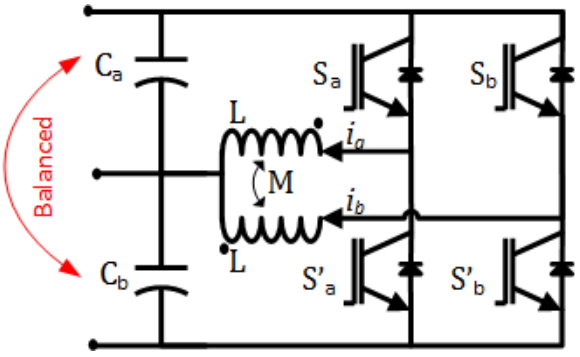


b) Sub-modules with Half-bridge and a single inductor

Figure 3-1. Triangular Modular Multilevel DC-DC Converter (TMMC) based on half-bridge submodules [41-43]



a) Overall Converter structure (Voltage ratio 5:1)



b) Sub-modules with H-bridge and mutually coupled inductors [44]

Figure 3-2. Proposed DC-DC IMMC based on H-bridge Sub-modules with mutually coupled inductors [44]

3.3 Modeling

As shown in the previous subsection, TMMC and the proposed DC-DC IMMC can be realized using different forms for the submodules used. Detailed converter modeling based on each of the two submodule concepts is presented in this subsection.

3.3.1 Modeling of Sub-Module Using Half Bridge with Single Inductor

Referring to Figure 3-1, the capacitor voltage differential equations can be written as:

$$\mathrm{C}\,\dot{v}_{c1} = I_s - \delta_1 i_{L1}$$

$$\mathrm{C}\,\dot{v}_{c2} = I_s + (1-\delta_1) i_{L1} - \delta_2 i_{L2} \quad \mathrm{C}\,\dot{v}_{c3} = I_s + (1-\delta_2) i_{L2} - \delta_3 i_{L3}$$

$$\dots \qquad \textbf{(3-1)}$$

$$\mathrm{C}\,\dot{v}_{cn} = I_s + (1-\delta_{n-1}) i_{L(n-1)} - \frac{v_{c\,n}}{R}$$

Similarly, inductor current differential equations

$$L_1\,\dot{i}_{L1} = \delta_1 v_{C1} - (1-\delta_1) v_{C2} - r_1 i_{L1}$$

$$L_2\,\dot{i}_{L2} = \delta_2 v_{C2} - (1-\delta_2) v_{C2} - r_1 i_{L2} \qquad \textbf{(3-2)}$$

… and so on

$$L_{(n-1)}\,\dot{i}_{L(n-1)} = \delta_{(n-1)} v_{C(n-1)} - (1-\delta_{(n-1)}) v_{C\,n} - r_{(n-1)} i_{L(n-1)}$$

Rewriting (3-1) and (3-2), we get showing the overall converter model in state space form (3-3).

The size of the inductance in each submodule is determined according to the allowable current ripple. However increasing this inductance, reduces the power density and limit the dynamic behavior for the overall converter in **(3-3)**.

$$\begin{bmatrix} \dot{v}_{c1} \\ \dot{v}_{c2} \\ \dot{v}_{c3} \\ \vdots \\ \dot{v}_{c\,n} \\ \\ \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \vdots \\ \dot{i}_{L\,(n-1)} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 & \frac{-\delta_1}{C} & 0 & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 & \frac{1-\delta_1}{C} & \frac{-\delta_2}{C} & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 & \frac{1-\delta_2}{C} & \frac{-\delta_3}{C} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{-1}{RC} & 0 & 0 & 0 & \cdots & \frac{1-\delta_{n-1}}{C} \\ \\ \frac{\delta_1}{L_1} & \frac{\delta_1-1}{L_1} & 0 & \cdots & 0 & \frac{-r_1}{L_1} & 0 & 0 & \cdots & 0 \\ 0 & \frac{\delta_2}{L_2} & \frac{\delta_2-1}{L_2} & \cdots & 0 & 0 & \frac{-r_2}{L_2} & 0 & \cdots & 0 \\ 0 & 0 & \frac{\delta_3}{L_3} & \cdots & 0 & 0 & 0 & \frac{-r_3}{L_3} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{\delta_{n-1}-1}{L_{n-1}} & 0 & 0 & 0 & \cdots & \frac{-r_{n-1}}{L_{n-1}} \end{bmatrix} \cdot \begin{bmatrix} v_{c1} \\ v_{c2} \\ v_{c3} \\ \vdots \\ v_{c\,n} \\ \\ i_{L1} \\ i_{L2} \\ i_{L3} \\ \vdots \\ i_{L\,(n-1)} \end{bmatrix} + \frac{1}{C} \begin{bmatrix} I_s \\ I_s \\ I_s \\ \vdots \\ I_s \\ \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad \textbf{(3-3)}$$

3.3.2 Modeling of Sub-Module Using H-Bridge with Mutually Coupled Inductors

Referring to Figure 3-2, the differential equations of the mutually coupled inductors can be written as:

$$L\,\dot{i}_a - M\,\dot{i}_b = S_a v_{C\,a} - S'_a v_{C\,b} - r\,i_a \quad \textbf{(3-4)}$$

$$L\,\dot{i}_b - M\,\dot{i}_a = S_b v_{C\,a} - S'_b v_{C\,b} - r\,i_b \quad \textbf{(3-5)}$$

Adding and subtracting **(3-4)** and **(3-5)**, result in

$$(L-M)\left(\dot{i}_a + \dot{i}_b\right) = (S_a + S_b)v_{C\,a} - (S'_a + S'_b)v_{C\,b} - r\,(i_a + i_b) \quad \textbf{(3-6)}$$

$$(L+M)\left(\dot{i}_a - \dot{i}_b\right) = (S_a - S_b)v_{C\,a} - (S'_a - S'_b)v_{C\,b} - r\,(i_a - i_b) \quad \textbf{(3-7)}$$

During normal operation, S_a & S_b are very close to 50% and 180° phase shifted, thus $\delta_a + \delta_b = 1$.

$$\dot{i}_t = \frac{v_{C\,a} - v_{C\,b}}{L_l} - \frac{r}{L_l} i_t \quad \textbf{(3-8)}$$

Here the total submodule current is governed by the leakage inductance of the mutually coupled coil, hence this leads to very fast dynamics for the submodules and the overall converter as well.

$$\Delta\dot{i} = \frac{(2\delta_a - 1)\left(v_{C\,a} + v_{C\,b}\right)}{2L - L_l} - \frac{r}{2L - L_l}\Delta i \quad \textbf{(3-9)}$$

Here the allowable current difference (small Δi) between the mutually coupled coils is governed by the self-inductance of the mutually coupled coil; hence very small magnetic core can be utilized. This leads to outstanding power density for the submodules and the overall converter as well.

$$
\begin{bmatrix} \dot{v}_{c1} \\ \dot{v}_{c2} \\ \dot{v}_{c3} \\ \vdots \\ \dot{v}_{c\,n} \\ \\ \\ \\ \\ \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \vdots \\ \dot{i}_{L\,(n-1)} \\ \\ \\ \\ \\ \Delta\dot{i}_{L1} \\ \Delta\dot{i}_{L2} \\ \Delta\dot{i}_{L3} \\ \vdots \\ \Delta\dot{i}_{L\,(n-1)} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 & \frac{-\delta_{a\,1}-\delta_{b\,1}}{2\mathrm{C}_1} & 0 & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 & \frac{2-\delta_{a\,1}-\delta_{b\,1}}{2\mathrm{C}_2} & \frac{-\delta_{a\,2}-\delta_{b\,2}}{2\mathrm{C}_2} & 0 & \cdots & 0 \\ 0 & 0 & 0 & \cdots & 0 & 0 & \frac{2-\delta_{a\,2}-\delta_{b\,2}}{2\mathrm{C}_3} & \frac{-\delta_{a\,3}-\delta_{b\,3}}{2\mathrm{C}_3} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{-1}{\mathrm{RC}} & 0 & 0 & 0 & \cdots & \frac{2-\delta_{a\,(n-1)}-\delta_{b\,(n-1)}}{2\mathrm{C}_n} \\ \\ \\ \\ \\ \frac{\delta_{a\,1}+\delta_{b\,1}}{L_{l\,1}} & \frac{\delta_{a\,1}+\delta_{b\,1}-2}{L_{l\,1}} & 0 & \cdots & 0 & \frac{-r_1}{L_{l\,1}} & 0 & 0 & \cdots & 0 \\ 0 & \frac{\delta_{a\,2}+\delta_{b\,2}}{L_{l\,2}} & \frac{\delta_{a\,2}+\delta_{b\,2}-2}{L_{l\,2}} & \cdots & 0 & 0 & \frac{-r_2}{L_{l\,2}} & 0 & \cdots & 0 \\ 0 & 0 & \frac{\delta_{a\,3}+\delta_{b\,3}}{L_{l\,3}} & \cdots & 0 & 0 & 0 & \frac{-r_3}{L_{l\,3}} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{\delta_{a\,(n-1)}+\delta_{b\,(n-1)}-2}{L_{l\,(n-1)}} & 0 & 0 & 0 & \cdots & \frac{-r_{(n-1)}}{L_{l(n-1)}} \\ \\ \\ \\ \\ \frac{\delta_{a\,1}-\delta_{b\,1}}{2L_1-L_{l\,1}} & \frac{\delta_{a\,1}-\delta_{b\,1}}{2L_1-L_{l\,1}} & 0 & \cdots & 0 & 0 & 0 & 0 & \cdots & 0 \\ 0 & \frac{\delta_{a\,2}-\delta_{b\,2}}{2L_2-L_{l\,2}} & \frac{\delta_{a\,2}-\delta_{b\,2}}{2L_2-L_{l\,2}} & \cdots & 0 & 0 & 0 & 0 & \cdots & 0 \\ 0 & 0 & \frac{\delta_{a\,3}-\delta_{b\,3}}{2L_3-L_{l\,3}} & \cdots & 0 & 0 & 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & \frac{\delta_{a\,(n-1)}-\delta_{b\,(n-1)}}{2L_{n-1}-L_{l(n-1)}} & 0 & 0 & 0 & \cdots & 0 \end{bmatrix}
$$

$$\begin{bmatrix}
\frac{-\delta_{a\,1}+\delta_{b\,1}}{2C_1} & 0 & 0 & \cdots & 0 \\
\frac{2-\delta_{a\,1}+\delta_{b\,1}}{2C_2} & \frac{-\delta_{a\,2}+\delta_{b\,2}}{2C_2} & 0 & \cdots & 0 \\
0 & \frac{2-\delta_{a\,2}+\delta_{b\,2}}{2C_3} & \frac{-\delta_{a\,3}+\delta_{b\,3}}{2C_3} & \cdots & 0 \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
0 & 0 & 0 & \cdots & \frac{2-\delta_{a\,(n-1)}+\delta_{b\,(n-1)}}{2C_n} \\
0 & 0 & 0 & \cdots & 0 \\
0 & 0 & 0 & \cdots & 0 \\
0 & 0 & 0 & \cdots & 0 \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
0 & 0 & 0 & \cdots & 0 \\
\frac{-r_1}{2L_1-L_{l\,1}} & 0 & 0 & \cdots & 0 \\
0 & \frac{-r_2}{2L_2-L_{l\,2}} & 0 & \cdots & 0 \\
0 & 0 & \frac{-r_3}{2L_3-L_{l\,3}} & \cdots & 0 \\
\vdots & \vdots & \vdots & \ddots & \vdots \\
0 & 0 & 0 & \cdots & \frac{-r_{n-1}}{2L_{n-1}-L_{l(n-1)}}
\end{bmatrix}
\cdot
\begin{bmatrix}
v_{c1} \\ v_{c2} \\ v_{c3} \\ \vdots \\ v_{c\,n} \\
i_{L1} \\ i_{L2} \\ i_{L3} \\ \vdots \\ i_{L\,(n-1)} \\
\Delta i_{L1} \\ \Delta i_{L2} \\ \Delta i_{L3} \\ \vdots \\ \Delta i_{L\,(n-1)}
\end{bmatrix}
+\frac{1}{C}
\begin{bmatrix}
I_s \\ I_s \\ I_s \\ \vdots \\ I_s \\
0 \\ 0 \\ 0 \\ \vdots \\ 0 \\
0 \\ 0 \\ 0 \\ \vdots \\ 0
\end{bmatrix}
\quad \textbf{(3-10)}$$

3.4 Comparison

In this subsection the two converter structures in Figure 3-1 and Figure 3-2 are compared to a base case which is the conventional two level buck converter with series switches stacked to withstand the high voltage as in Figure 3-3.

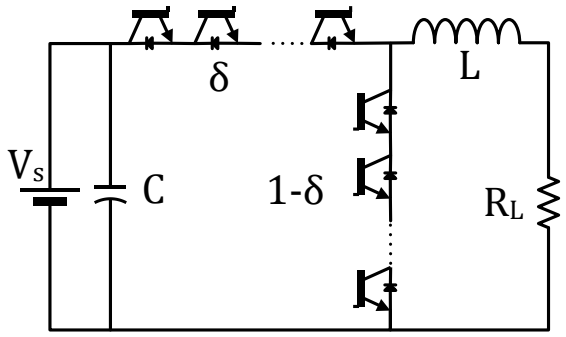


Figure 3-3. Buck converter
(Switching devices are stacked in series to withstand high voltage)

The comparison in Table 3-1 lists the needed number of modules, semiconductor switches, inductors and capacitors. It also includes the switch voltage and current ratings (Peak and average). Despite that the proposed IMMC and TMMC have large number of device and component counts, it should be highlighted that the total VA rating of the of all semiconductor switches is the same as the traditional buck converter case.

The required inductance for each case is also computed for a given current ripple ratio (k_i). Then the total inductive energy stored is compared. From the total inductive Energy stored ratio, it is noticed that the TMMC has by far the largest value indicating

poor power density. On the other side, the proposed IMMC has the lowest index, thus recognized as the highest power density solution under study.

Filter capacitors in the proposed IMMC using H-bridge Submodule can also be smaller than TMMC case because they are subject to only very small current ripples thanks to the interleaved operation of the mutually coupled coils, accordingly they are sized to provide enough Energy buffering to set the dynamic performance of the overall converter.

The advantages of the proposed IMMC include:

1) High power density
2) Fast converter dynamics
3) Modularity and Scalability
4) Low Electromagnetic Interference EMI, because the switching actions occur at lower voltages and high frequency voltages and currents are filtered within each submodule.
5) High utilization of semiconductor switches (low peak to average current ratio)
6) Series connection of capacitors is no longer required, hence, voltage sharing is achieved without resistors (i.e. lower losses)
7) No series connection of semiconductor switches, i.e. easier gating control and lower switching losses.
8) The proposed IMMC accepts bidirectional power flow and enables the interface of multiple DC lines at different voltage levels to one common DC bus [41, 44].

Table 3-1. Comparison between Proposed Multilevel DC-DC Converter and Buck Converter

	Buck converter Figure 3-3	**TMMC Half-bridge Submodule with single inductorFigure 3-1, [41-43]**	**Proposed DC-DC IMMC using H-bridge Submodule with mutually coupled inductors Figure 3-2, [44]**
Number of modules		$\frac{n}{2}(n-1)$	$\frac{n}{2}(n-1)$
Number of switches	$2n$	$n(n-1)$	$2n(n-1)$
Number of inductors	1	$\frac{n}{2}(n-1)$	$\frac{n}{2}(n-1)$ coil pairs
Number of capacitors	1 (i/p side)	n	n
Switch Voltage	$\frac{V_{DC}}{n}\left(\frac{n-1}{n}\right)$	$\frac{2\,V_{DC}}{n}$	$\frac{2\,V_{DC}}{n}$
Switch Peak current	$n\,I_s$	$2\,I_s$	I_s
Switch average current	I_s	I_s	$\frac{I_s}{2}$
Switch VA (peak)	$V_{DC}\,I_s$	$\frac{4\,V_{DC}\,I_s}{n}$	$\frac{2\,V_{DC}\,I_s}{n}$
Total VA (peak) of all Switches	$2\;V_{DC}\,I_s(n-1)$	$2\,V_{DC}\,I_s(n-1)$	$2\,V_{DC}\,I_s(n-1)$
Inductance L (ki is the current ripple ratio)	$V_{DC}\left(\frac{n-1}{n}\right)\;\frac{T_s}{n}\;\frac{1}{k_i\,n\,I_s}$	$\frac{V_{DC}}{n}\;\frac{T_s}{2}\;\frac{1}{k_i\,2\,I_s}$	$\frac{1}{(1+k_M)}\;\frac{V_{DC}}{n}\;T_s\;\frac{1}{k_i\,2\,I_s}$
Energy inductive stored $=\frac{1}{2}\mathbf{L\,i^2}$	$\frac{V_{DC}\,I_s\,T_s}{2\,k_i}\left(\frac{n-1}{n}\right)$	$\frac{V_{DC}\,I_s\,T_s}{2\,n\,k_i}$	$\frac{V_{DC}\,T_s\,I_s}{2\,n\,k_i}\;\left(2\frac{{k_i}^2}{(1+k_M)}\right)$
Total inductive Energy stored		$\frac{V_{DC}\,I_s\,T_s}{4\,k_i}(n-1)$	$\frac{V_{DC}\,T_s\,I_s}{4\,k_i}\;(n-1)\left(2\frac{{k_i}^2}{(1+k_M)}\right)$
Total Energy stored ratio	1	$\frac{n}{2}$	$\frac{n\;\;{k_i}^2}{(1+k_M)}$
	Assuming kM=0.99, ki=0.05, n=100		
	1	50	0.13

The major Disadvantage of the IMMC is the higher number of switches and component count which limits scalability to high number of levels, however, the total VA rating of all semiconductor switches is the same as in conventional buck converter case.

3.5 Switching and Control Method

In this subsection experimental verification of the hard switching and the proposed soft switching is discussed for the Sub-module based on H-bridge with mutually coupled inductors shown in Figure 3-4. The main components of the prototype are listed in Table 3-2.

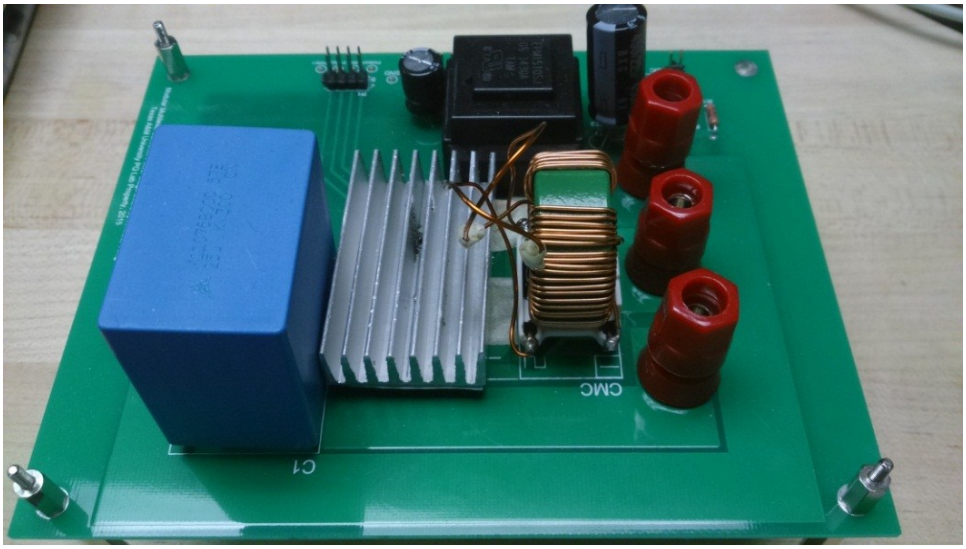


Figure 3-4. Experimental prototype of sub-module based on H-bridge with mutually coupled inductors

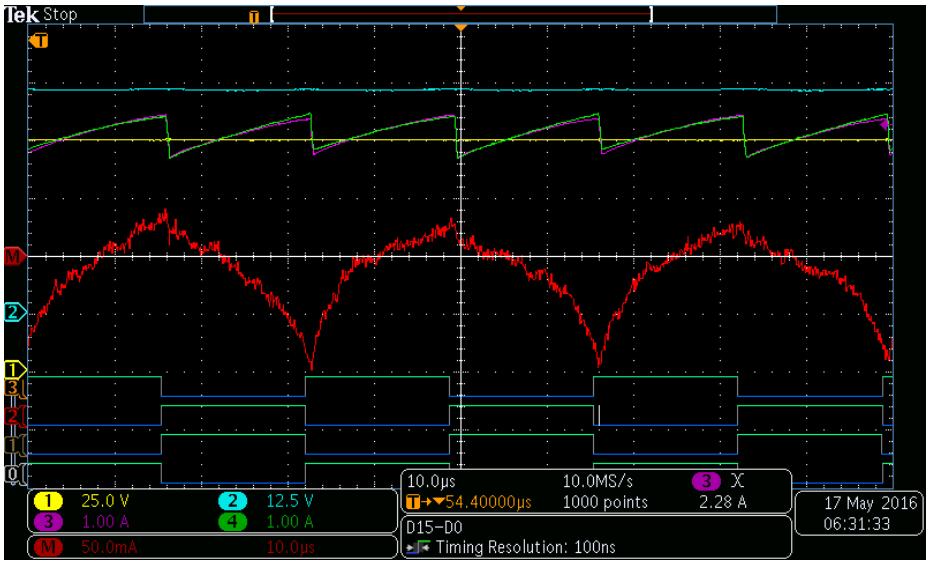
Table 3-2. Main Sub-module Components Used in Experiments Figure 3-4

Component	Value	Dimension	Description
Coupled Inductors	Self inductance = 8 mH Leakage inductance =50μH	1.45" × 1.35" × 0.8"	Triad Magnetics CMT-8112
DC Capacitor	25uF	1.65" × 1.1"	EPCOS (TDK) B32676E3256K
H-bridge	250V, 4.6A	1.14" × 0.67"	International Rectifier IRSM505-084

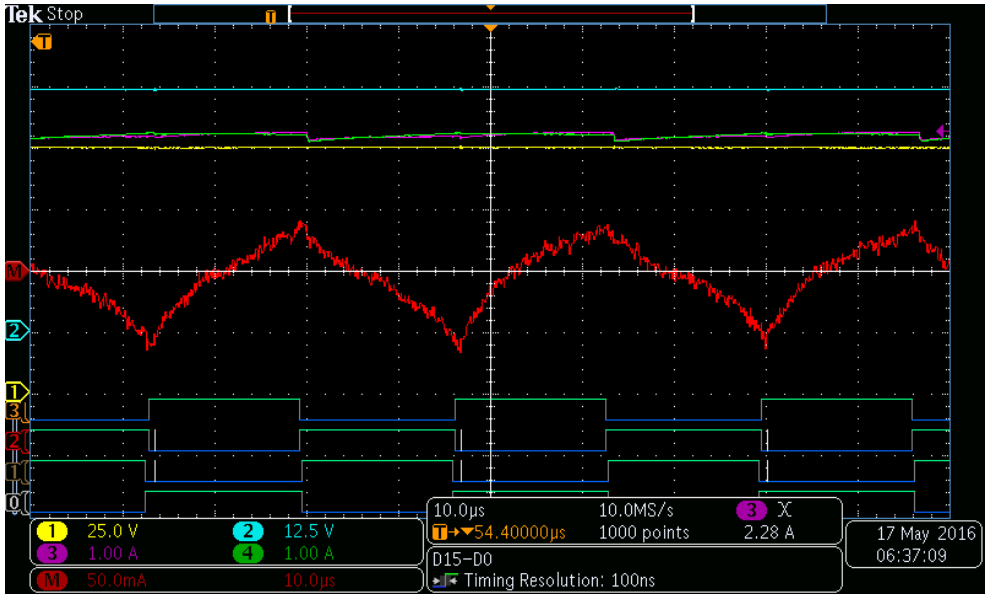
3.5.1 Hard Switching

As discussed in the topology and modeling subsections all the submodules are operated with a duty cycle very close to 50% and the two phase les are 180° phase shifted, so that minimum ripples occur on the output current according to **(3-8)** and also allows for very small current difference between the two coils due to the high self-inductance of the mutually coupled coils **(3-9)**.

It is noticed in Figure 3 5(a), which at 50% duty cycle, the current ripples is small but not minimal due to the inserted dead time in the hardware causing all the submodule switches to be turned off, thus the currents of both coils fall down rapidly due to the very low leakage inductance. However when this inserted dead time is compensated by slightly increasing the duty cycle as in Figure 3 5(a), the current ripple in both coils is diminished.



(a) Duty is 50%.
Current ripples occur due to inserted deadtime (400nSec)



(b) Duty is 51.8%
Current ripples are minimized after compensating for deadtime (+1.8%)

Figure 3-5. Pulse pattern and current waveforms for the hard switching for sub-module based on H-bridge with mutually coupled inductors.

Channel 1: Input Voltage (V_{C1}+ V_{C2}), Channel 2: Output Voltage (V_{C2}),
Channel 3, 4: Individual Currents in mutually coupled coils (i_{L1} and i_{L2})
Channel M: Current difference in mutually coupled coils (i_{L1}− i_{L2})
The digital channels D(0-3) represent the gating signals for the DSP control board.

Table 3-3 summarizes voltage, current and power readings for submodule Figure 3-4 under hard switching operation, showing max efficiency of 95.89%. The following subsection shows how the proposed soft switching attains higher efficiency.

Table 3-3. Experimental Results for Hard Switching

R_{load} Ω	V_{source} (V)	I_{source} (A)	P_{source} (W)	I_{load} (A)	V_{load} (V)	P_{load} (W)	**Efficiency %**
40	99.16	0.5874	58.24	1.159	47.88	55.49	95.27
20	99.25	1.145	113.64	2.287	47.65	108.98	95.89
10	99.33	2.24	222.5	4.503	47.09	212.04	95.3

3.5.2 Soft Switching

The aim of this subsection is to demonstrate a ZVS soft switching scheme based on a submodule consisting of H-bridge with coupled inductors as shown in Figure 3-2.

One of the best approaches to maximize the submodule efficiency is to minimize the switching loss by implementing soft switching techniques like Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS) techniques to reduce the overlap of current and voltage waveforms at switching transitions. However, this reduction in switching loss should not be at the expense of increased conduction losses to the extent that overall losses are increased. Conduction loss can generally be reduced by using better semiconductor devices with low effective resistance and by selecting

topologies/techniques to increase device utilization, i.e. requiring low (average and/or RMS) currents to convert a given amount of power.

Advantages of the proposed soft switching scheme are:

- Soft switching (ZVS) ➔ low switching loss, high frequency and small magnetics
- Low-rms / high-average current ➔ High switch utilization
- Low magnetic core stress ➔ Low core losses

From **(3-8)**, it is easily noticed that during balance the total current $(i_a + i_b)$ is only limited by the leakage inductance $(L - M)$ which is typically very small and controlled by $(S_a + S_b)$ or their complements $(S'_a + S'_b)$, hence the total current can be changed in a very fast manner by simultaneous switching of both top switches $S_a \& S_b$ or both bottom switches $S'_a \& S'_b$. From (3-9), it is also noticed that the current difference $(i_a - i_b)$, is limited by a large inductance $(L + M)$ and controlled by $(S_a - S_b)$ or their complements $(S'_a - S'_b)$, thus this current difference can be easily kept below the saturation limits of the coupled inductors by keeping $S_a \& S_b$ approximately out of phase except for short bursts of time to allow the proposed ZVS operation.

Figure 3-6 demonstrates how the current in the coupled inductor is shaped using the gating signals $S_a \& S_b$ to achieve negative current for brief period before turning ON the top switches, hence achieving ZVS in all cases as demonstrated in Figure 3-7 and Figure 3-8.

The trapezoidal shape of the current in Figure 3-6 maintains low rms current, hence reduces the conduction losses. The fast changes of the total (common mode)

current is not seen by the magnetic field strength over the core material thus core losses are kept low due to the small current difference $(i_a - i_b)$.

Table 3-4 summarizes voltage, current and power readings under the proposed soft switching operation, showing max efficiency of 98.35% significantly higher compared to 95.89% in the hard switching case Table 3-3.

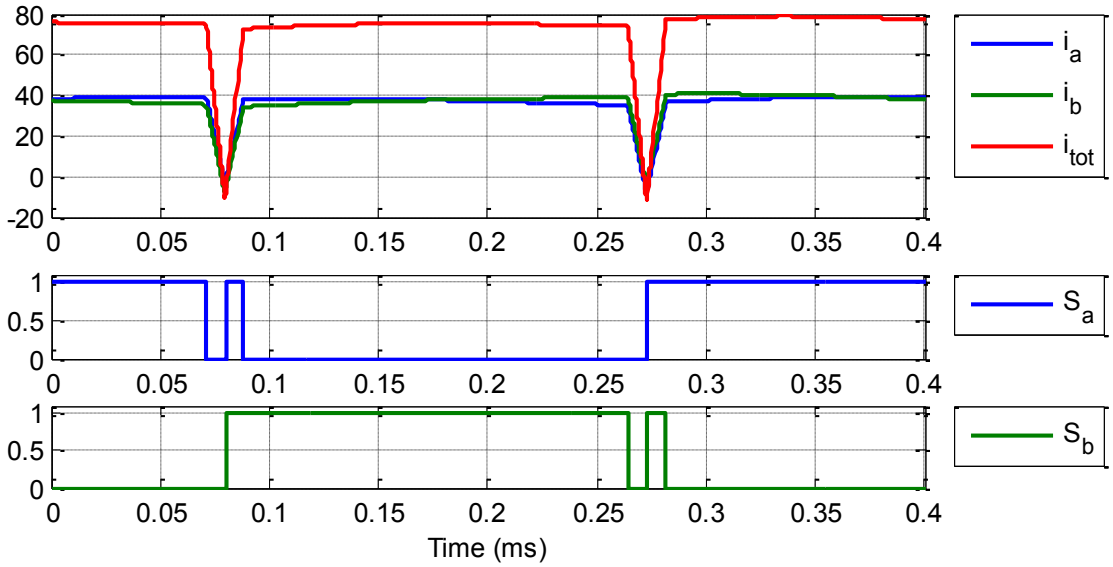
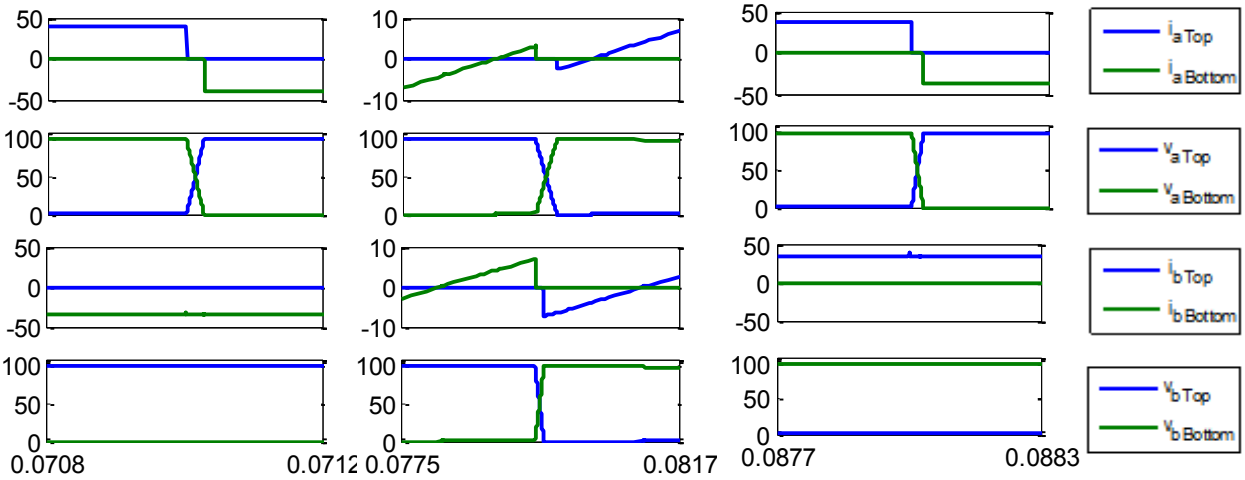


Figure 3-6. Pulse pattern and current waveforms for the proposed soft switching for sub-module based on H-bridge with mutually coupled inductors



a) S_a switches from 1 to 0, while S_b is kept 0

b) Both S_a and S_b switch from 0 to 1 simultaneously

c) S_a is kept 1, while S_b switches from 0 to 1

Figure 3-7. Current and voltage waveforms of top and bottom switches for the two phases a, b during Zero Voltage Switching at three different instants.

Table 3-4. Experimental Results for the Proposed Soft Switching

R_{load} Ω	V_{source} (V)	I_{source} (A)	P_{source} (W)	I_{load} (A)	V_{load} (V)	P_{load} (W)	Efficiency %
40	99.25	0.5928	58.84	1.185	48.83	57.86	98.35
20	99.19	1.171	116.15	2.34	48.33	113.09	97.37
10	98.64	2.366	233.38	4.643	48.08	223.24	95.65

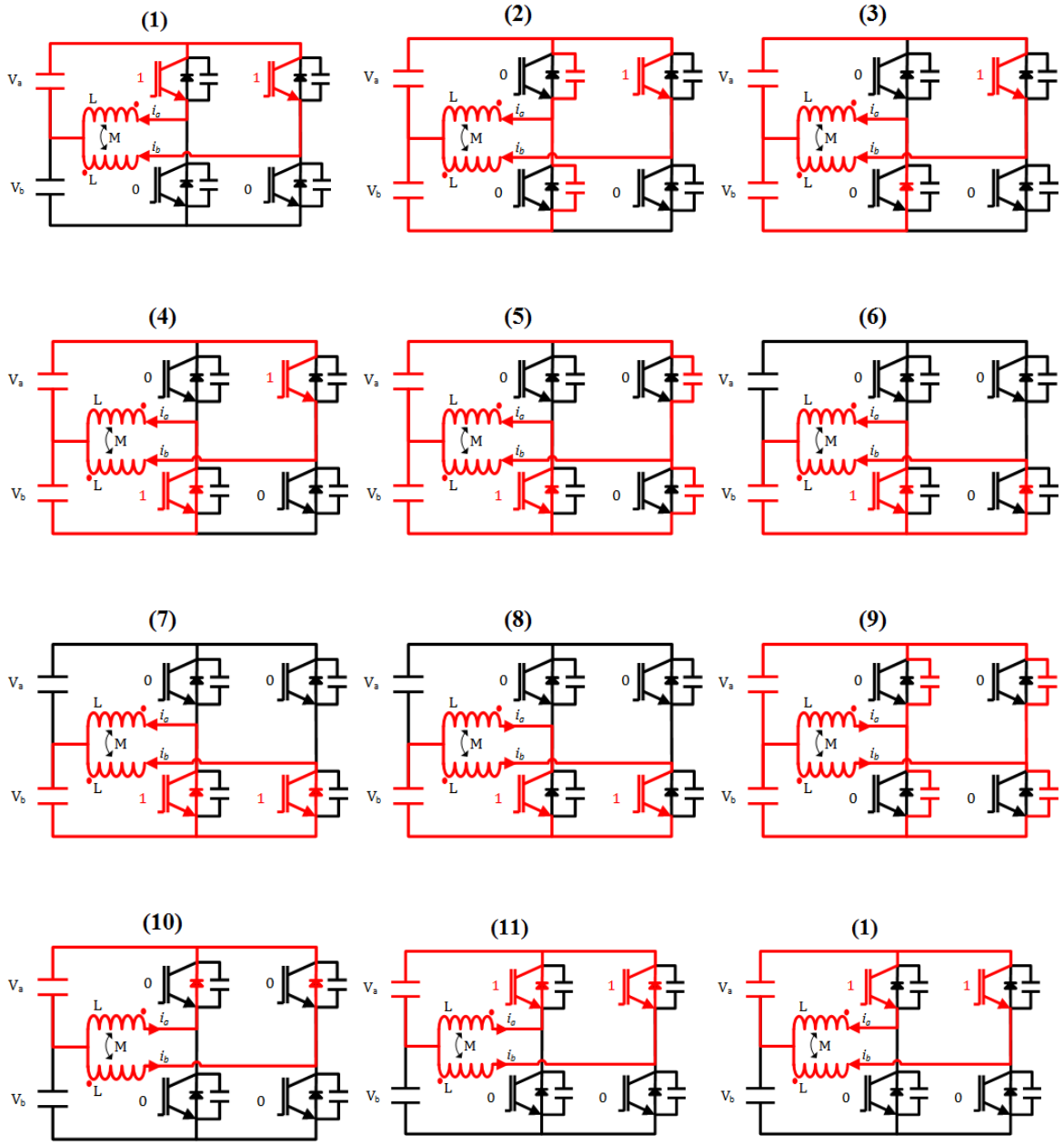
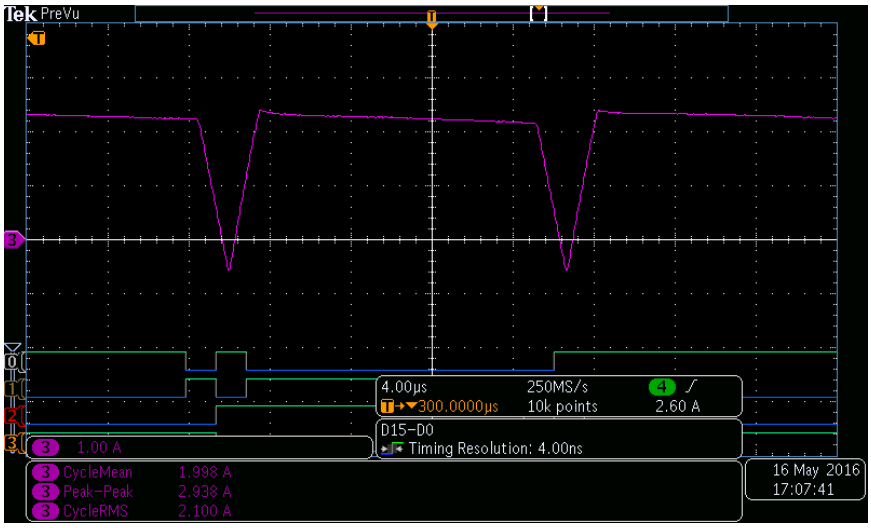
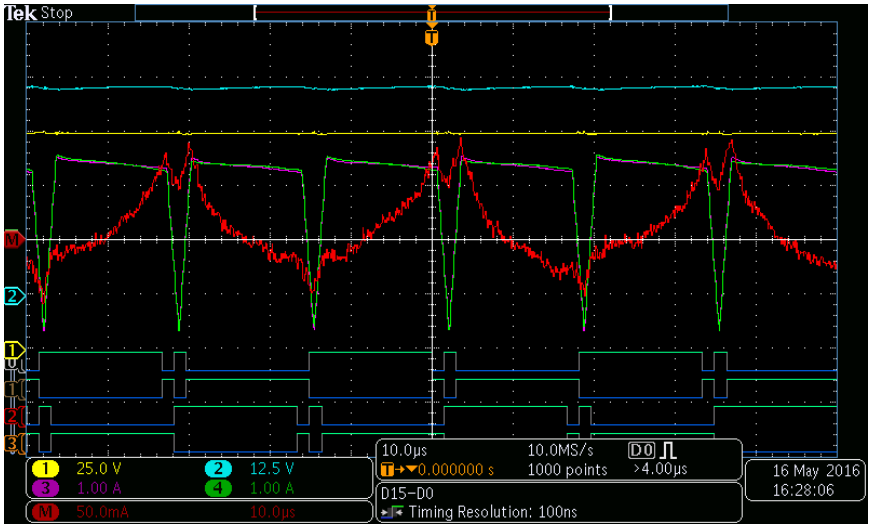


Figure 3-8. Soft switching steps highlighting current flow

3.5.2.1 Steady state experimental waveforms for the proposed soft switching



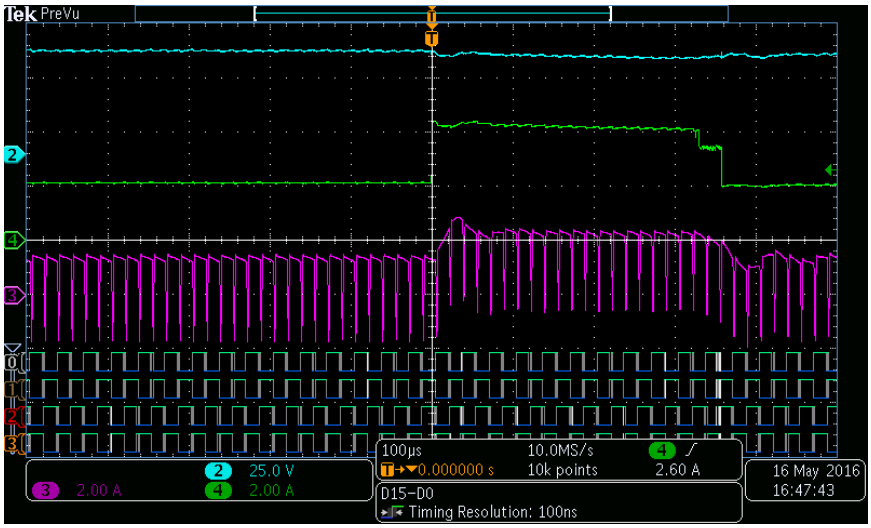
a) Coil current waveform showing very close values for average and rms (1.998A and 2.1A respectively)



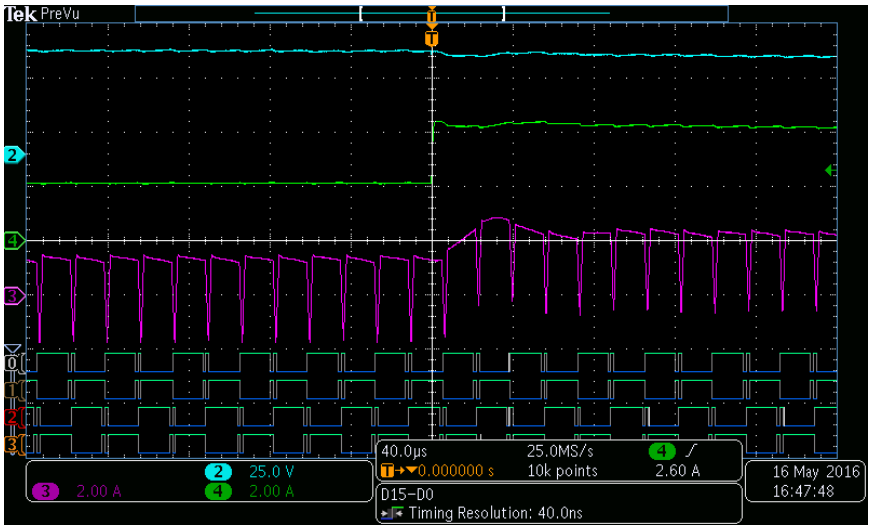
b) Currents in both coils are closely matched during steady state

Figure 3-9. Pulse pattern and current waveforms for the the proposed soft switching for sub-module based on H-bridge with mutually coupled inductors. Channel 1: Input Voltage (V_{C1}+ V_{C2}), Channel 2: Output Voltage (V_{C2}), Channel 3, 4: Individual Currents in mutually coupled coils (i_{L1} and i_{L2}) Channel M: Current difference in mutually coupled coils (i_{L1}− i_{L2}) The digital channels D(0-3) represent the gating signals for the DSP control board.

3.5.2.2 Dynamic response experimental results for the proposed soft switching

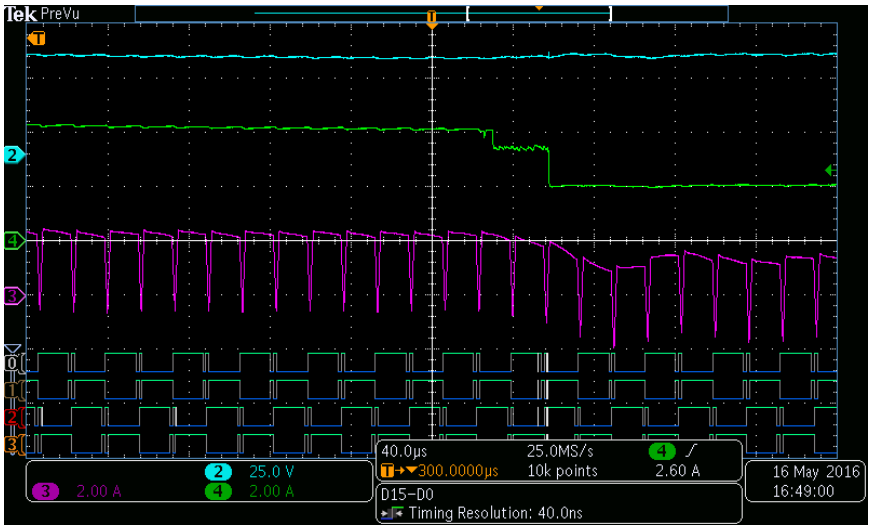


a) Dynamic Response during Load Pulse (2.34A ⇔ 4.643A)

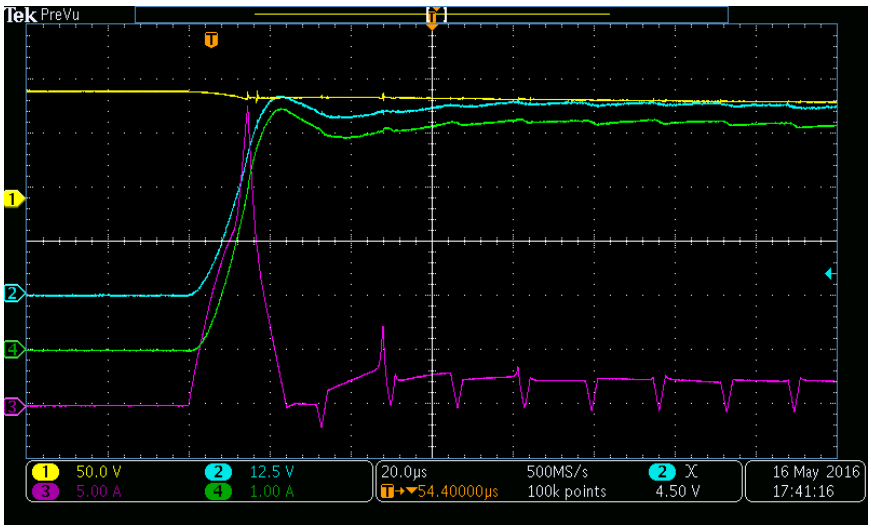


b) Dynamic Response during Load Pulse (rising edge) (2.34A ➔ 4.643A)

Figure 3-10. Dynamic response for the the proposed soft switching for sub-module based on H-bridge with mutually coupled inductors.
Channel 1: Input Voltage (V_{C1}+ V_{C2}), Channel 2: Output Voltage (V_{C2}),
Channel 3, 4: Individual Currents in mutually coupled coils (i_{L1} and i_{L2})
Channel M: Current difference in mutually coupled coils (i_{L1}− i_{L2})
The digital channels D(0-3) represent the gating signals for the DSP control board.



c) Dynamic Response during Load Pulse (falling edge) (2.34A ← 4.643A)



d) Dynamic response during startup (20µsec response time, 60µsec response time)

Figure 3-10 Continued
Channel 1: Input Voltage (V_{C1}+ V_{C2}), Channel 2: Output Voltage (V_{C2}),
Channel 3, 4: Individual Currents in mutually coupled coils (i_{L1} and i_{L2})
Channel M: Current difference in mutually coupled coils (i_{L1}− i_{L2})
The digital channels D(0-3) represent the gating signals for the DSP control board.

3.6 Converter Dynamic Performance

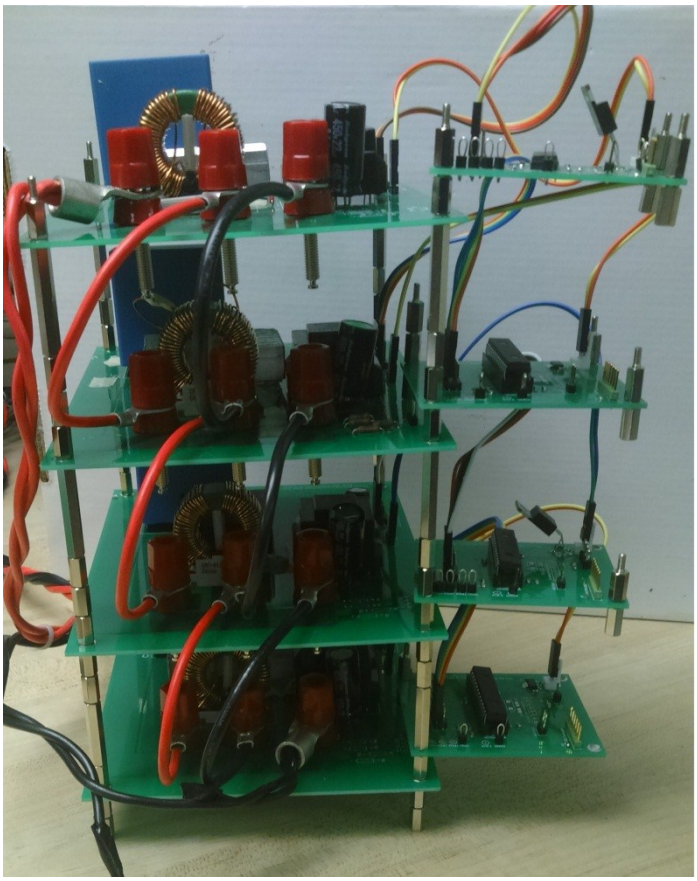
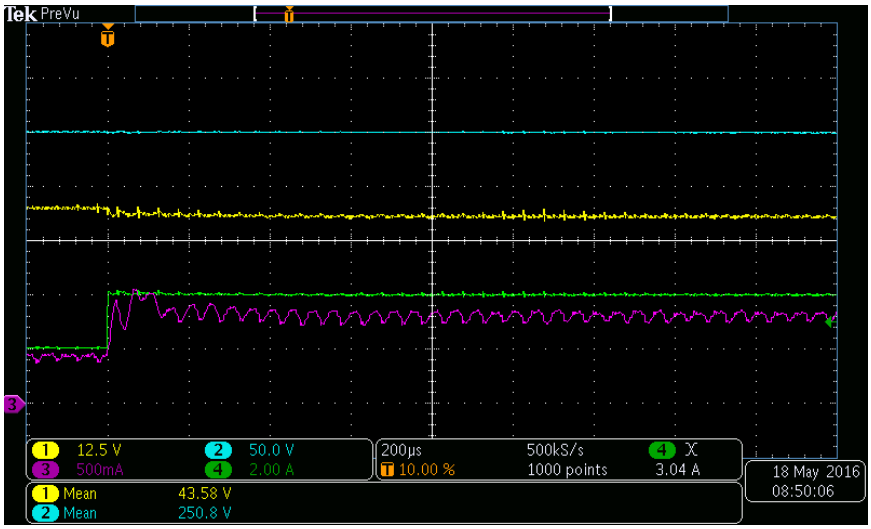


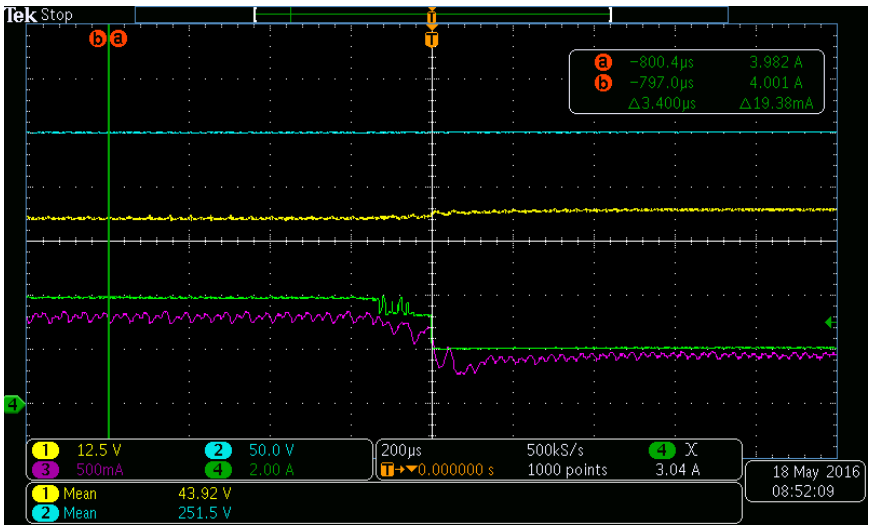
Figure 3-11. Hardware prototype for proposed DC-DC IMMC (5-levels without paralleling modules) using Sub-module based on H-bridge with mutually coupled inductors

3.6.1 Step Down (Buck) Mode

Figure 3-12 demonstrates the fast dynamic behavior (200μsec settling time) of the proposed converter when operating as a buck converter with a step down ratio of 1/5 (250V to 50V nominally).



(a) Load step change (2A ➔ 4A)



(b) Load step change (4A ➔ 2A)

Figure 3-12. Buck mode (250V to 50V) step change in load (2A to 4A)
Channel 1: Load Voltage (low side), Channel 2: Supply Voltage (high side),
Channel 3: Supply Current, Channel 4: Load Current.

3.6.2 Step Up (Boost) Mode

As previously highlighted, the proposed converter allows bidirectional power flow and thus the load and supply can be interchanged to construct a boost converter with a step up ratio of 5× (50V to 250V nominally). Figure 3-13, shows the steady state behavior when operating in a step up (boost) mode.

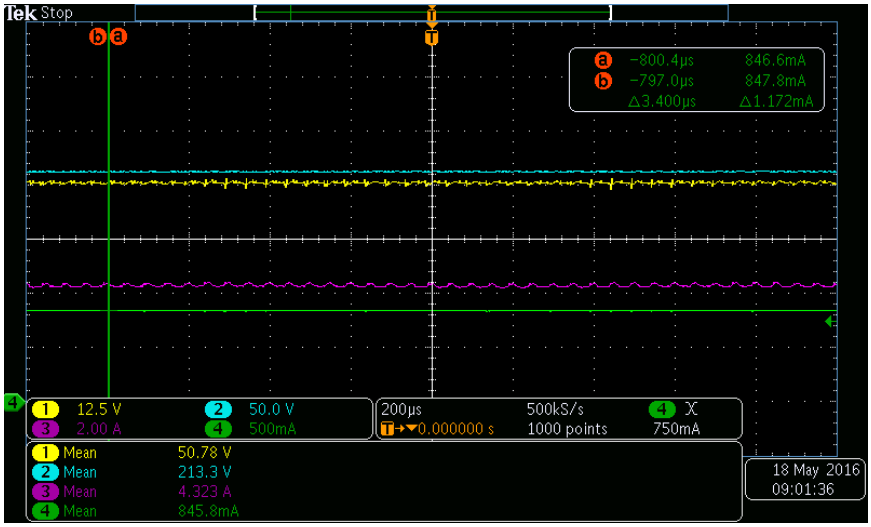
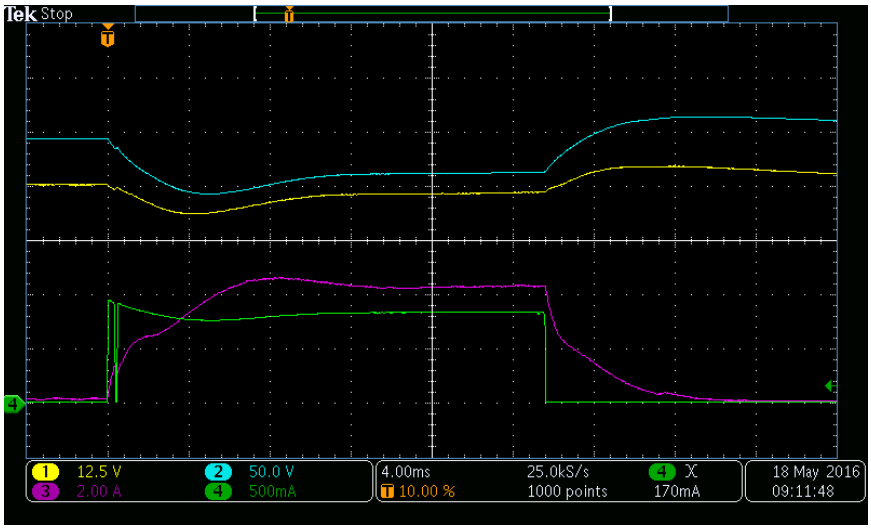
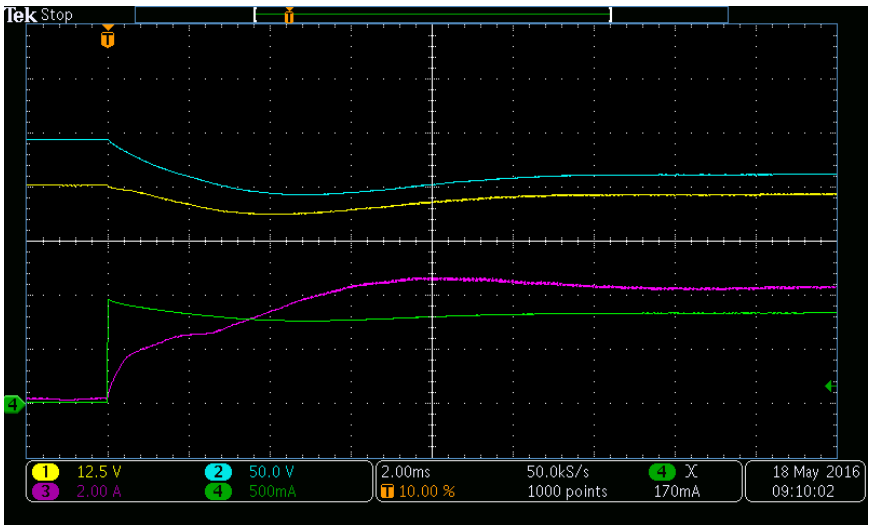


Figure 3-13. Boost mode (50V to 250V) steady state (180W)
Channel 1: Supply Voltage (low side), Channel 2: Load Voltage (high side), Channel 3: Supply Current, Channel 4: Load Current.

Despite the fast dynamic behavior of the proposed converter demonstrated in the transient response of the step down case (200µsec settling time) Figure 3-12, the step up case shows an increased settling time of (10msec) Figure 3-14, due to the limited bandwidth of the DC supply on the low voltage side (50V), that is taking around 10msec to regulate to its nominal value.

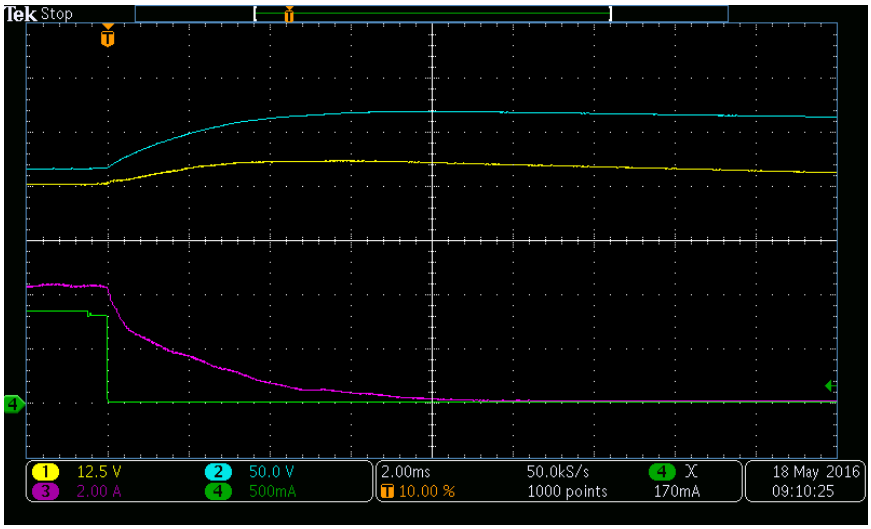


(a) Load step change (0A ⇔ 0.85A)



(b) Load step change (0A ➔ 0.85A)

Figure 3-14. Boost mode (50V to 250V) with step change in load (0⇔ 180W)
Channel 1: Supply Voltage (low side), Channel 2: Load Voltage (high side),
Channel 3: Supply Current, Channel 4: Load Current.



(c) Load step change (0.85A ➔ 0 A)

Figure 3-14. Continued
Channel 1: Supply Voltage (low side), Channel 2: Load Voltage (high side),
Channel 3: Supply Current, Channel 4: Load Current.

3.7 Summary

In this section, a New High Power Density Interconnected Modular Multilevel DC-DC Converter suitable for high voltage high power applications is proposed. Due to the fully modular design, this topology can be applied with arbitrary number of levels. Modeling of the presented topology is explained showing its advantages in terms of converter dynamics and size of the passive components. Additionally this work proposed a ZVS scheme for the introduced converter. Its advantages include high power density, high utilization of the semiconductor switches due to low rms current and low core loss due to low magnetic stresses on the coupled inductor. The proposed IMMC topology is experimentally validated showing superior power density and dynamic response. Additionally, the proposed ZVS scheme shows outstanding efficiency of 98.35%.

4 DC-AC INTERCONNECTED MODULAR MULTILEVEL CONVERTER (IMMC) TOPOLGY

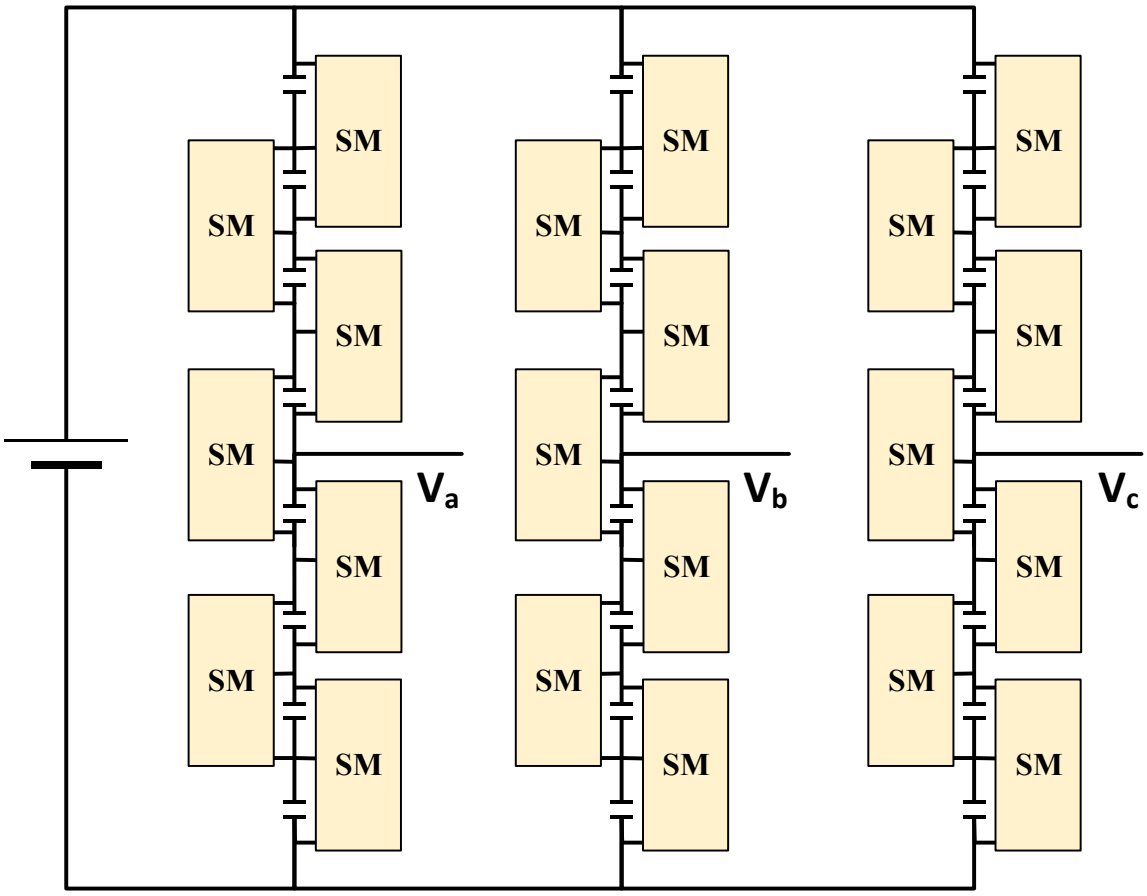
This Section presents DC-AC mode of operation of the proposed IMMC as an extension to Section 3 where DC-DC conversion is discussed.

The proposed DC-AC IMMC is introduced in this section as a substitute to conventional topologies reviewed in Section 1, like DCMC and CCMC in high voltage applications when higher number of levels is desirable, but without sacrificing power density as in conventional MMC case [21, 25]. Afterwards, the IMMC is analyzed in terms of topology, modulation and modeling. Finally, the IMMC performance is experimentally verified through comprehensive testing scenarios.

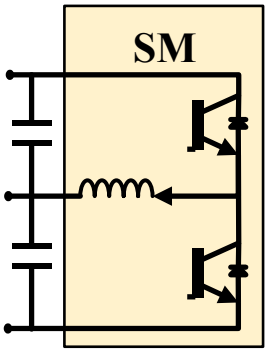
4.1 Proposed Interconnected Modular Multilevel Converter IMMC

4.1.1 Topology

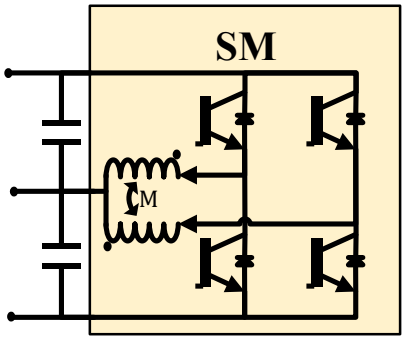
The topology of the proposed DC-AC Interconnected Modular Multilevel Converter (IMMC) is shown in Figure 4-1. Its basic concept of operation is to change the voltage distribution across the capacitors constituting the high voltage DC-link using the interleaved sub-modules. This change in capacitor voltages allows generating any arbitrary output voltage. The required capacitors are small since they are only needed for filtering high switching frequency. The configuration in Figure 4-1 can be generalized to any number of levels according to the DC link voltage.



a) Proposed DC-AC IMMC (3 Phase 5 level)



b) Sub-module using Half-bridge with single inductor



c) Sub-module using H-bridge with mutually coupled inductors

Figure 4-1. Proposed DC-AC IMMC

4.1.2 Modulation Method

The modulation of the proposed IMMC must satisfy the following conditions:

1) The DC link capacitors should share the total bus voltage without exceeding the voltage rating for any of them.
2) To assure deterministic voltages for all capacitors, only one given group of neighboring capacitors should share the total bus voltage, i.e. the bypassed capacitors can be either above or below this group. The selection of this given group of neighboring capacitors (towards the +ve DC rail or the –ve DC rail) defines the output voltage.

The following two subsections cover staircase modulation based on the realization of the main voltage levels.

4.1.2.1 Staircase modulation of IMMC

This subsection demonstrates an introductory concept of modulation for the proposed IMMC, based on the number of main voltage levels. The concept discussed here is applied on one phase leg of 5-level IMMC, however it is scalable to an arbitrary number of phases and levels. As shown in Figure 4-1, a 5-level IMMC comprises of 4 upper capacitors and 4 lower capacitors. At any of the 5 voltage levels required, only four out of the eight DC link capacitors of a given leg, are equally balanced to share the bus voltage, while all other capacitors are bypassed. According to the required output voltage level, i.e. the modulating signal in Figure 4-2(a), the normalized reference voltages of the DC link capacitors are calculated Figure 4-2(b) while maintaining the aforementioned modulation conditions.

In the staircase modulation case, the duty ratio is either 0 (to bypass the lower capacitor of a given submodule), 1 (to bypass the upper capacitor of a given submodule), or 0.5 to equally balance the upper and lower capacitors of a given module, Figure 4-2(c). This 0.5 duty ratio enables the exploitation of the submodule based on H-bridge with coupled inductors, hence, minimizing the size of the passive components as detailed in Section 3.

Lastly, the voltages across the seven submodules, constituting the 5-level IMMC phase leg, are depicted in Figure 4-2(d) by adding the reference voltages of each pair of neighboring capacitors.

Figure 4-3 demonstrates how the 5 main voltage levels $\left(\frac{V_{DC}}{2}, \frac{V_{DC}}{4}, 0, \frac{-V_{DC}}{4}, \frac{-V_{DC}}{2}\right)$ are realized by balancing a group of neighboring capacitors while bypassing the others. For instance, in Figure 4-3(b) the three upper most capacitors (V_{C1}, V_{C2}, V_{C3}) are bypassed by the top switches of submodules (1, 2 and 3), whereas the lowermost capacitor V_{C8} is bypassed by the bottom switch of submodule 7. The remaining four capacitors (V_{C4}, V_{C5}, V_{C6}, V_{C7}) are balanced at $\left(\frac{V_{DC}}{4}\right)$ by operating submodules (4, 5 and 6) at a duty ratio of 0.5. Therefore the output voltage is set to $\frac{V_{DC}}{4}$. Similarly, the remaining four voltage levels $\left(\frac{V_{DC}}{2}, 0, \frac{-V_{DC}}{4}, \frac{-V_{DC}}{2}\right)$ are achieved following the same logic as in Figure 4-3(a, c, d, e) respectively. However, smooth transitioning between these levels to attain low distortion on the output voltage is presented in the following subsection.

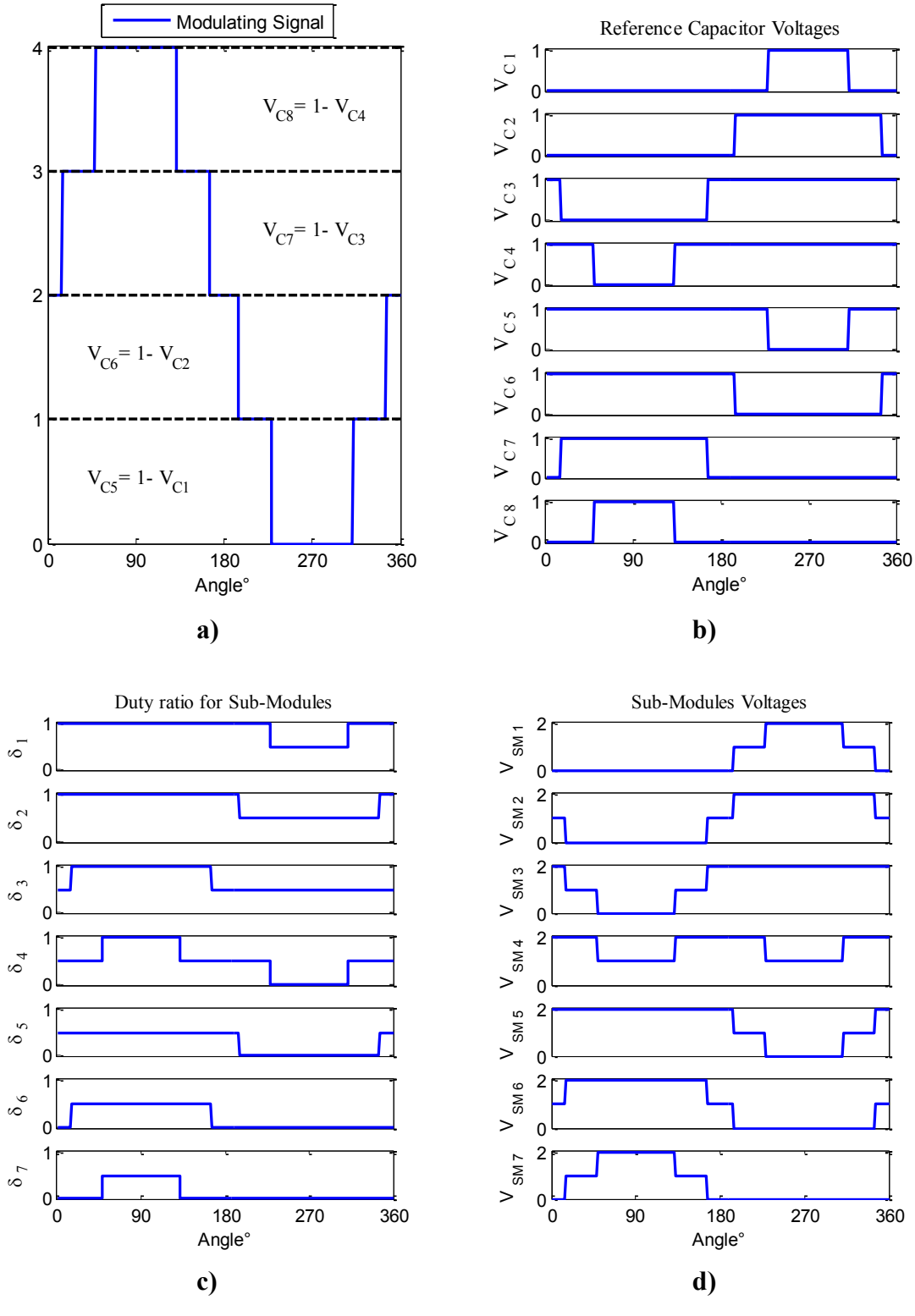


Figure 4-2. Staircase modulation of 5 level IMMC (for one Phase leg)

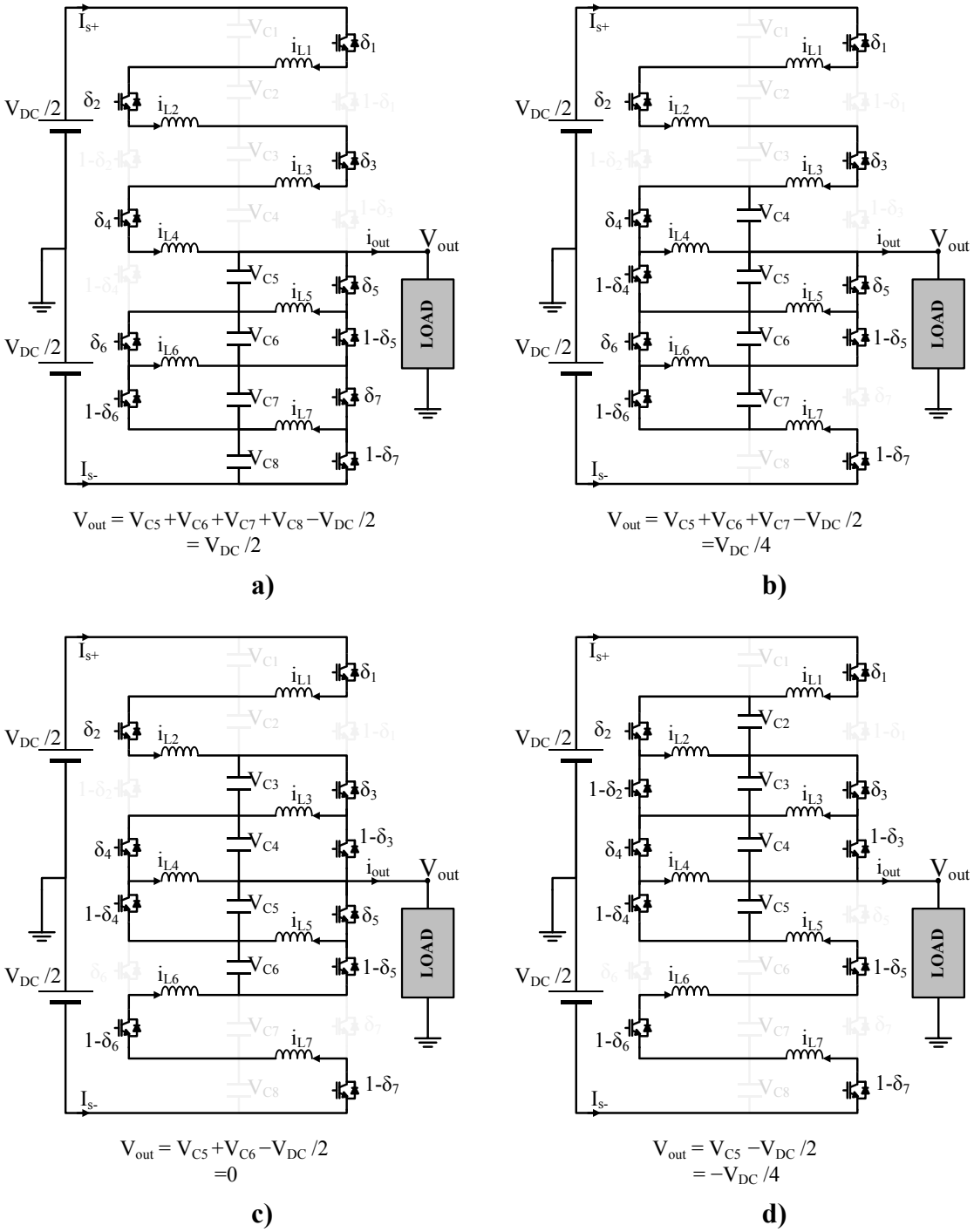
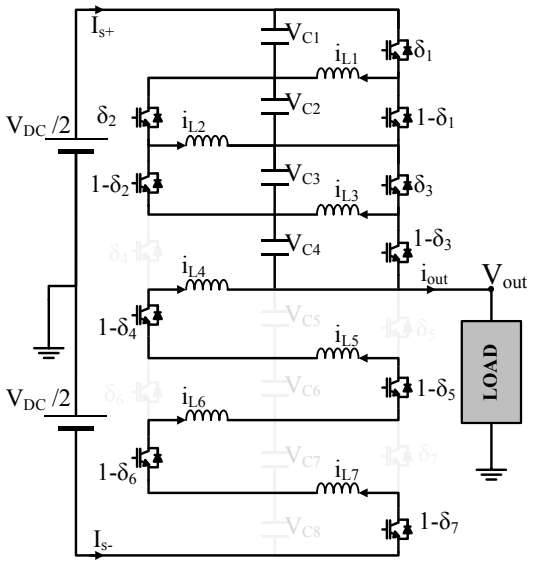


Figure 4-3. Realization of main voltage levels of IMMC (ex. 5-level)



$$V_{out} = -V_{DC}/2$$

e)

Figure 4-3. Continued

4.1.2.2 Sinusoidal modulation for the proposed IMMC

The staircase modulation in the previous subsection described only how to realize the main voltage levels, however, this subsection shows how to realize a continuous i.e. sinusoidal output voltage with very low distortion.

By slicing the sinusoidal modulating signal in Figure 4-4(a) according to the number of upper (or lower) capacitors, the normalized reference voltages of the DC link capacitors are calculated as in Figure 4-4(b) while maintaining the aforementioned modulation conditions. Afterwards, the duty ratio of each Sub-module is calculated based on the ratio of the reference voltages of the two capacitors attached to the sub-module. To avoid division by zero and singularity, an infinitesimally small value ϵ is added to the denominator.

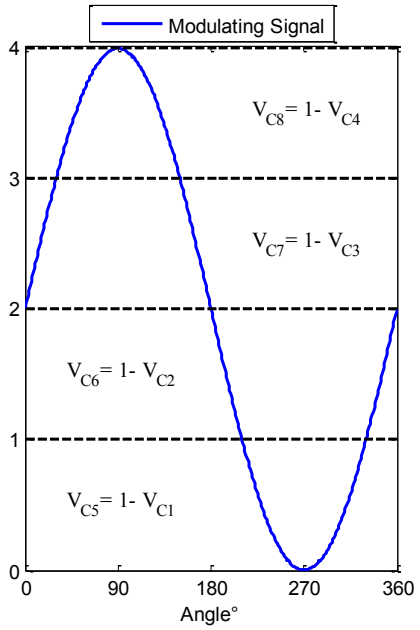
For the top sub-modules,

$$\delta_n = 1 - \frac{v_{c,\ n+1}}{v_{c,\ n} + v_{c,\ n+1} + \epsilon}, \quad \text{where } 0 \le n \le \frac{N}{2} \tag{4-1}$$

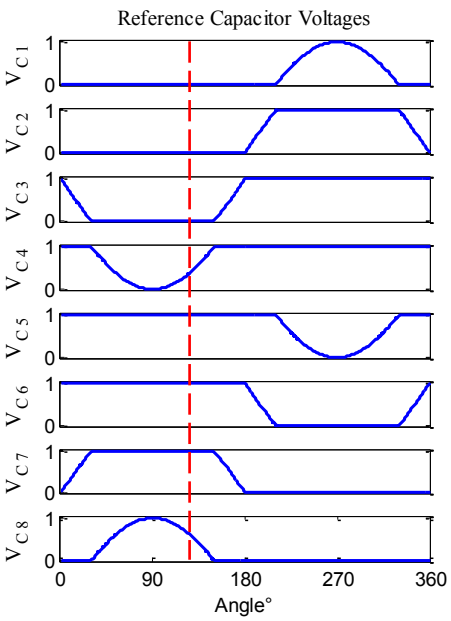
For the bottom sub-modules

$$\delta_n = \frac{v_{c,\ n}}{v_{c,\ n} + v_{c,\ n+1} + \epsilon}, \quad \text{where } \frac{N}{2} \le n \le N - 2 \tag{4-2}$$

Consequently, in the sinusoidal modulation case, the duty ratio varies smoothly between 0 (bypassing mode) to 0.5 (balancing mode) for the upper submodules, and between 1 (bypassing mode) to 0.5 (balancing mode) for the lower submodules, Figure 4-4(c). The voltages across the seven submodules constituting the 5-level IMMC phase leg, are depicted in Figure 4-4(d) showing the smooth variation in voltage.

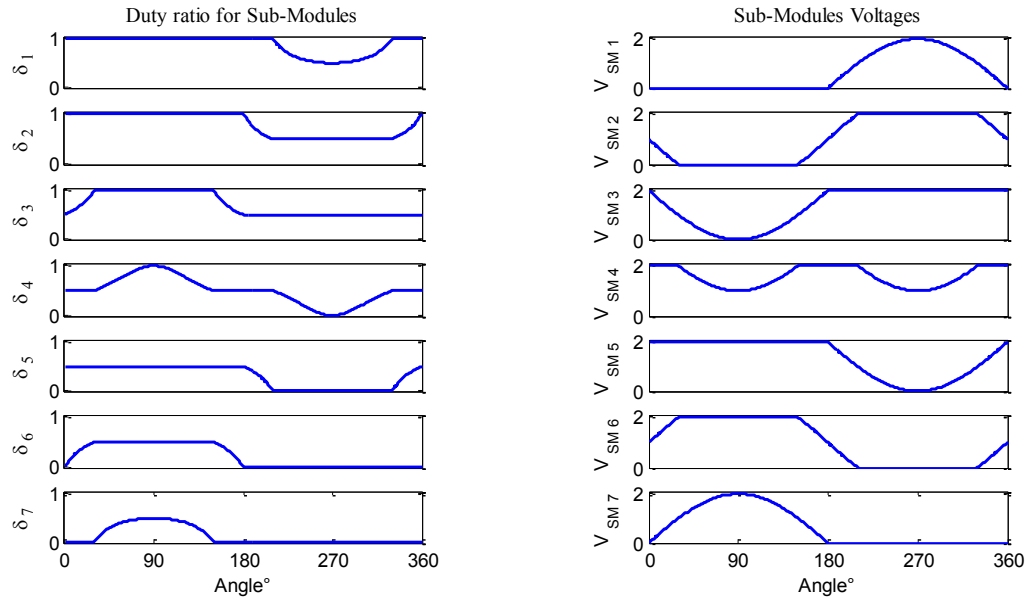


a) Adjusted modulating signal $=(1+m)\frac{N}{4}$, where m is from (4-21)



b)

Figure 4-4. Sinusoidal modulation of 5 level IMMC (for one Phase leg)



c) **d)**

Figure 4-4. Continued

Figure 4-5 demonstrates realization of transitioning between the 5 main voltage levels $\left(\frac{V_{DC}}{2}, \frac{V_{DC}}{4}, 0, \frac{-V_{DC}}{4}, \frac{-V_{DC}}{2}\right)$ by allowing continuous variation of duty ratios of the submodules. For instance, in Figure 4-5(a) shows transitioning between $\left(\frac{V_{DC}}{4} < V_{out} < \frac{V_{DC}}{2}\right)$, where the three upper most capacitors (V_{C1}, V_{C2}, V_{C3}) are bypassed by the top switches of submodules (1, 2 and 3), whereas the remaining five capacitors (V_{C4}, V_{C5}, V_{C6}, V_{C7}, V_{C8}) share the bus voltage according to the duty ratios of submodules (4, 5, 6 and 7). As highlighted in Figure 4-4(a), V_{C4} and V_{C8} complement each other such that they add up to $\frac{V_{DC}}{4}$. Therefore, when (V_{C4}, V_{C8}) approach $\left(0, \frac{V_{DC}}{4}\right)$ respectively, the output voltage approaches $\frac{V_{DC}}{2}$, Figure 4-3. Continued(a), and when (V_{C4}, V_{C8}) approach $\left(\frac{V_{DC}}{4}, 0\right)$ respectively, the output voltage approaches $\frac{V_{DC}}{4}$, Figure 4-3(b). Similarly the

remaining three voltage transitioning ranges $\left(0 < V_{out} < \frac{V_{DC}}{4}\right)$, $\left(\frac{-V_{DC}}{4} < V_{out} < 0\right)$ and $\left(\frac{-V_{DC}}{2} < V_{out} < \frac{-V_{DC}}{4}\right)$ are achieved following the same logic as in Figure 4-5(b, c, d) respectively.

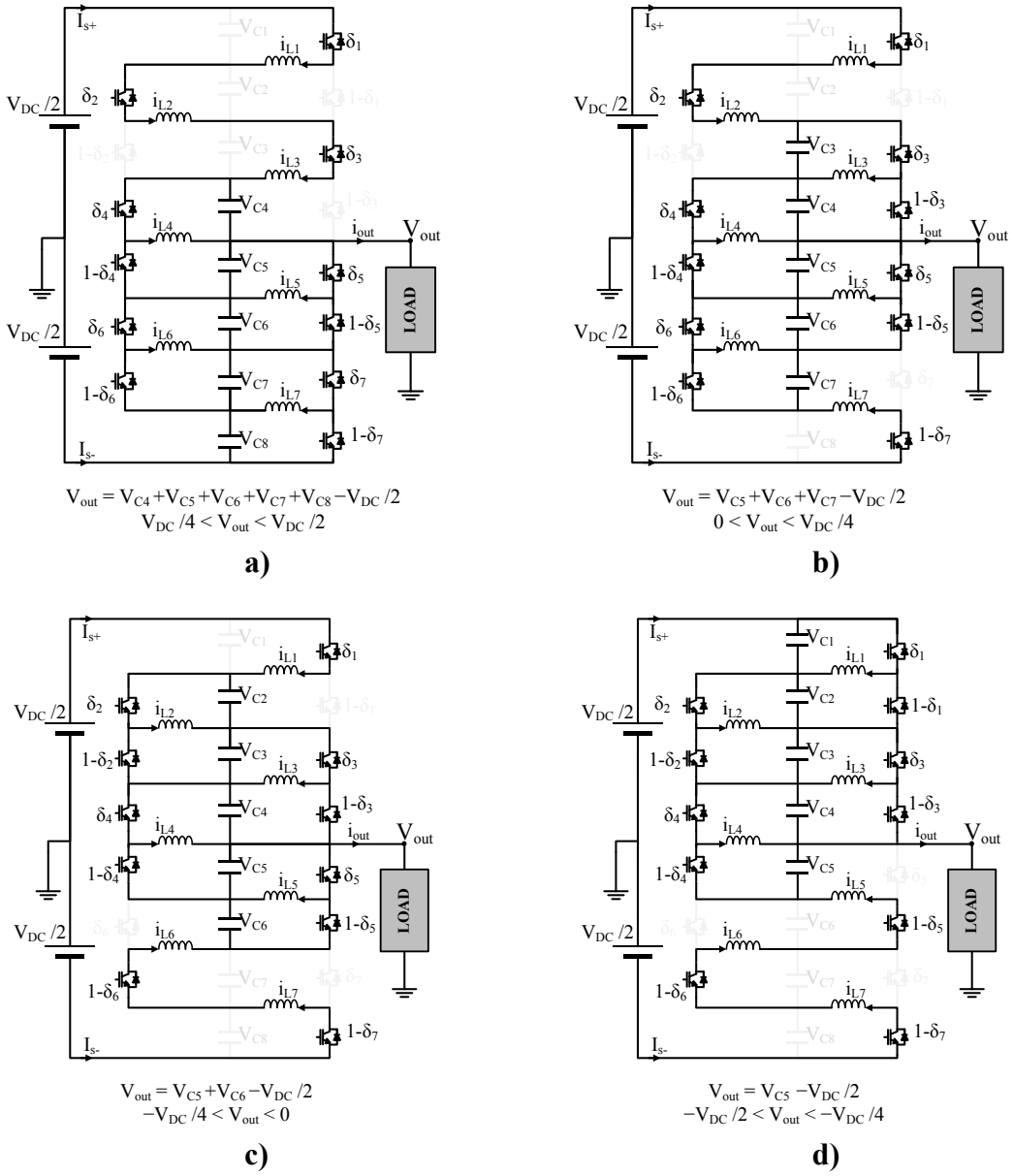


Figure 4-5. Realization of sinusoidal voltage levels of IMMC (ex. 5-level)

4.1.3 Modeling

The detailed configuration of five level step down (5:1) MMC DC-DC converter by using building block of half-bridge with single inductor is shown in Figure 2-3. For

4.1.3.1 Capacitor voltages equations

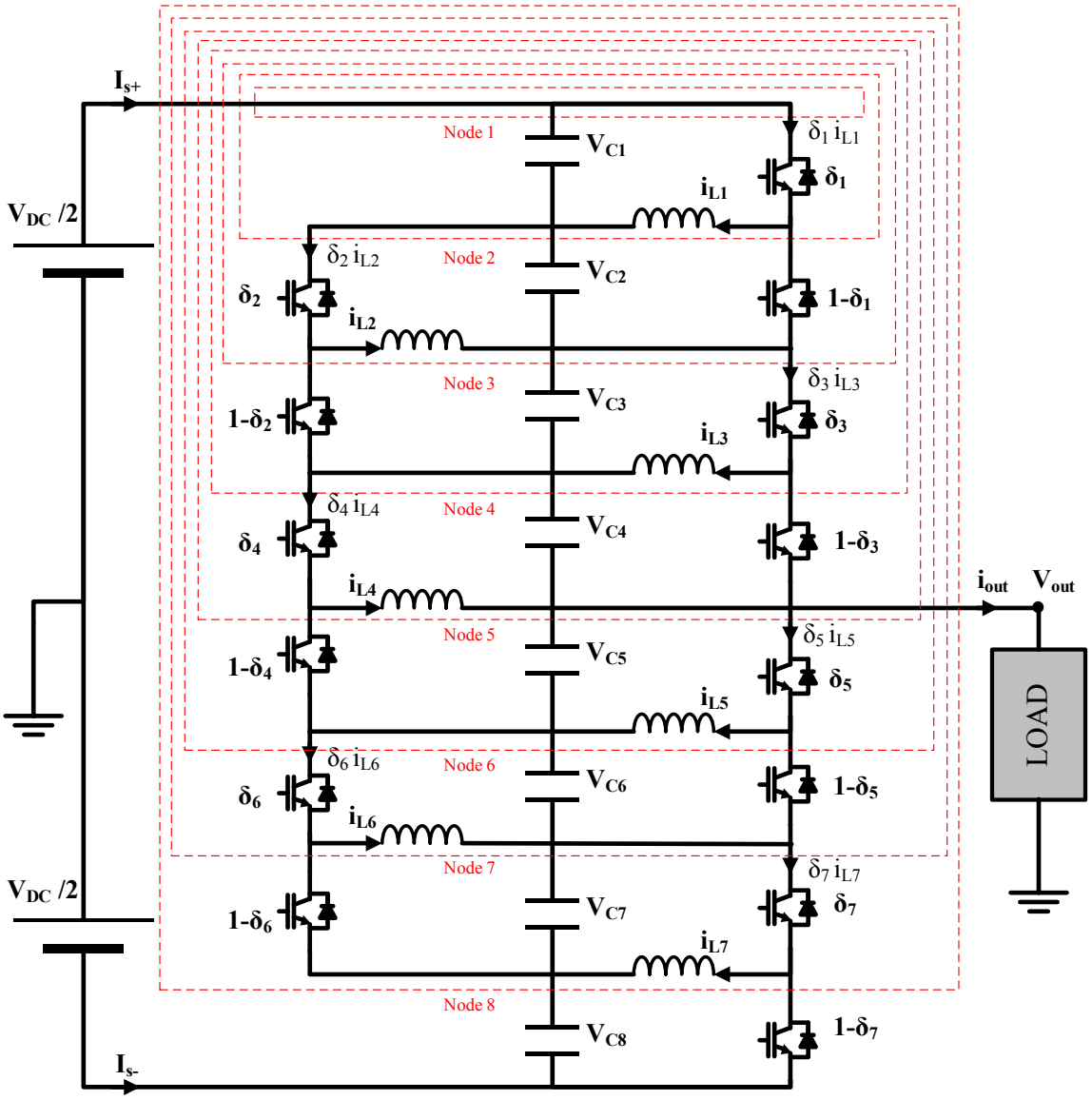


Figure 4-6. Current nodes used for capacitors differential equations

By following the super-nodes (red dashed lines), the current equations for the capacitors can be written as in the following matrix form.

$$C\begin{bmatrix} \dot{v}_{c1} \\ \dot{v}_{c2} \\ \dot{v}_{c3} \\ \dot{v}_{c4} \\ \dot{v}_{c5} \\ \dot{v}_{c6} \\ \dot{v}_{c7} \\ \dot{v}_{c8} \end{bmatrix} = \begin{bmatrix} -\delta_1 & & & & & & & \\ 1-\delta_1 & -\delta_2 & & & & & & \\ & 1-\delta_2 & -\delta_3 & & & & & \\ & & 1-\delta_3 & -\delta_4 & & & & \\ & & & 1-\delta_4 & -\delta_5 & & & \\ & & & & 1-\delta_5 & -\delta_6 & & \\ & & & & & 1-\delta_6 & -\delta_7 & \\ & & & & & & 1-\delta_7 & \end{bmatrix} \cdot \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ i_{L5} \\ i_{L6} \\ i_{L7} \end{bmatrix} + \begin{bmatrix} I_{s+} \\ I_{s+} \\ I_{s+} \\ I_{s+} \\ -I_{s-} \\ -I_{s-} \\ -I_{s-} \\ -I_{s-} \end{bmatrix}$$

(4-3)

For an arbitrary number of sub-modules, the differential equations for the capacitors voltages can be expressed as:

$$C\begin{bmatrix} \dot{v}_{c,\ 1} \\ \dot{v}_{c,\ 2} \\ \dot{v}_{c,\ 3} \\ \vdots \\ \dot{v}_{c,\ \frac{N}{2}} \\ \dot{v}_{c,\ \frac{N}{2}+1} \\ \vdots \\ \dot{v}_{c,\ N-2} \\ \dot{v}_{c,\ N-1} \\ \dot{v}_{c,\ N} \end{bmatrix} = \begin{bmatrix} -\delta_1 & & & & & & & & & \\ 1-\delta_1 & -\delta_2 & & & & & & & & \\ & 1-\delta_2 & -\delta_3 & & & & & & & \\ & & \ddots & \ddots & & & & & & \\ & & & 1-\delta_{\frac{N}{2}-1} & -\delta_{\frac{N}{2}} & & & & & \\ & & & & 1-\delta_{\frac{N}{2}} & -\delta_{\frac{N}{2}+1} & & & & \\ & & & & \ddots & \ddots & & & & \\ & & & & & 1-\delta_{N-3} & -\delta_{N-2} & & & \\ & & & & & & 1-\delta_{N-2} & -\delta_{N-1} & & \\ & & & & & & & 1-\delta_{N-1} & & \end{bmatrix} \cdot \begin{bmatrix} i_{L,\ 1} \\ i_{L,\ 2} \\ i_{L,\ 3} \\ \vdots \\ i_{L,\ \frac{N}{2}} \\ \vdots \\ i_{L,\ N-3} \\ i_{L,\ N-2} \\ i_{L,\ N-1} \end{bmatrix} + \begin{bmatrix} I_{s+} \\ I_{s+} \\ I_{s+} \\ \vdots \\ I_{s+} \\ -I_{s-} \\ \vdots \\ -I_{s-} \\ -I_{s-} \\ -I_{s-} \end{bmatrix} \quad \textbf{(4-4)}$$

At steady state $v_{c,\ n}^{\circ} = 0$, From which the current equations can be written as

$$i_{L1} = \frac{I_{s+}}{\delta_1} \tag{4-5}$$

If $2 \leq n \leq \frac{N}{2}$

$$i_{L,\ n} = \frac{I_{s+} + (1 - \delta_{n-1})\, i_{L,\ n-1}}{\delta_n} \tag{4-6}$$

For $n > \frac{N}{2}$, δ_n reaches zero

$$i_{L,\ N-1} = \frac{I_{s-}}{1 - \delta_{N-1}} \tag{4-7}$$

For $\frac{N}{2} \leq n \leq N - 2$

$$i_{L,\ n} = \frac{I_{s-} + \delta_{n+1}\, i_{L,\ n+1}}{1 - \delta_n} \tag{4-8}$$

4.1.3.2 Inductor current equations

The differential equations for the inductor current of the IMMC shown in Figure (), can be found by considering the two loops adjacent to the given inductor within each sub-module.

When $S_1 = 1$, from Loop 1

$$L\, i_{L1}^{\circ} = v_{c1} \tag{4-9}$$

Similarly, when $S_1 = 0$, from Loop 1*

$$L\, i_{L1}^{\circ} = -v_{c2} \tag{4-10}$$

Taking the state average over a switching period with a duty ratio of δ_1 is

$$L\, i_{L1}^{\circ} = \delta_1 v_{c1} - (1 - \delta_1) v_{c2} \tag{4-11}$$

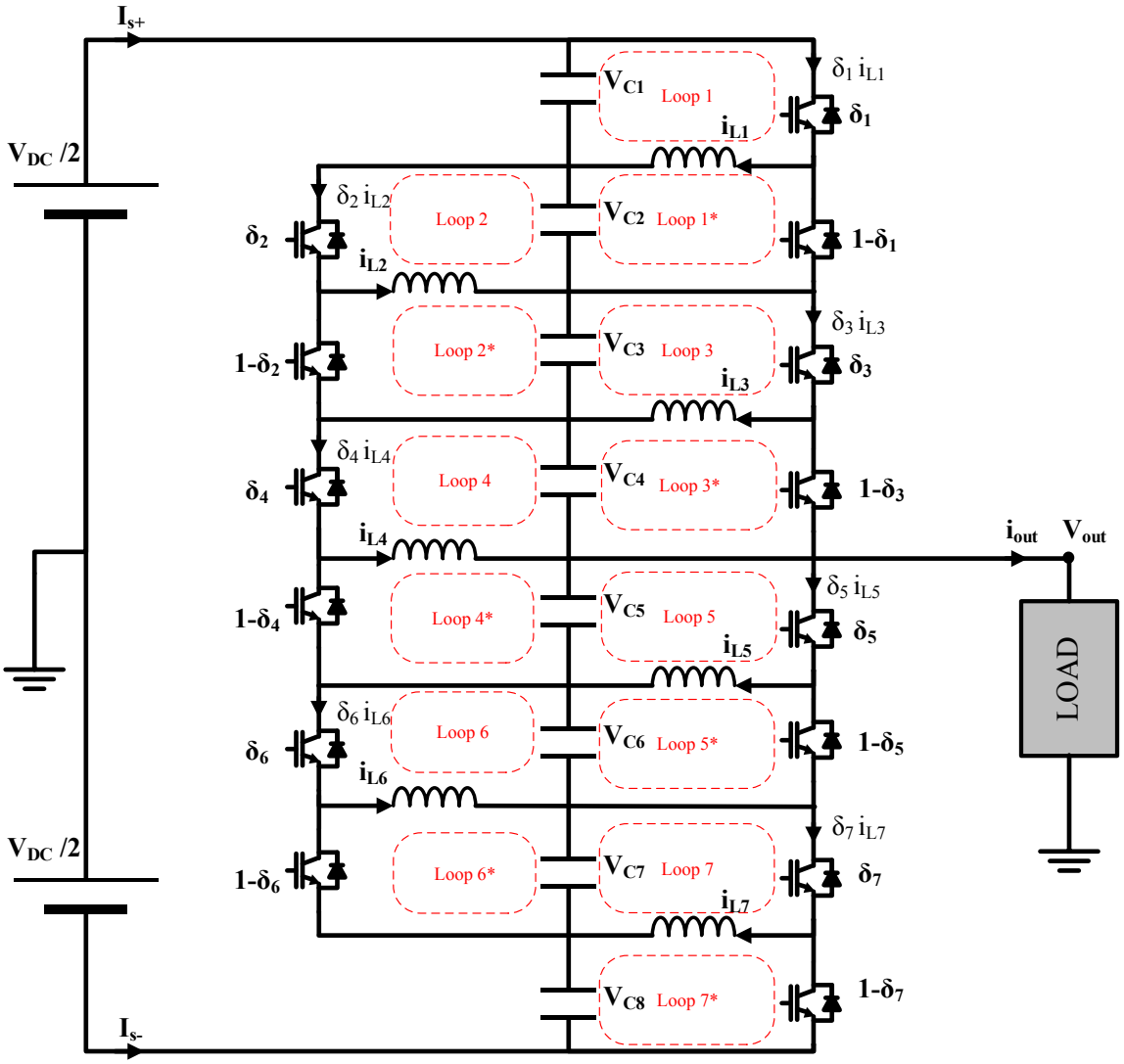


Figure 4-7. Voltage loops used for inductor differential equations

Similarly the differential equation of the inductor current of the rest sub-modules can be derived in the same way.

$$L\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \dot{i}_{L4} \\ \dot{i}_{L5} \\ \dot{i}_{L6} \\ \dot{i}_{L7} \end{bmatrix} = \begin{bmatrix} \delta_1 & \delta_1 - 1 & & & & & & \\ & \delta_2 & \delta_2 - 1 & & & & & \\ & & \delta_3 & \delta_3 - 1 & & & & \\ & & & \delta_4 & \delta_4 - 1 & & & \\ & & & & \delta_5 & \delta_5 - 1 & & \\ & & & & & \delta_6 & \delta_6 - 1 & \\ & & & & & & \delta_7 & \delta_7 - 1 \end{bmatrix} \begin{bmatrix} v_{c1} \\ v_{c2} \\ v_{c3} \\ v_{c\,4} \\ v_{c\,5} \\ v_{c\,6} \\ v_{c\,7} \\ v_{c\,8} \end{bmatrix} + r_L \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \\ i_{L5} \\ i_{L6} \\ i_{L7} \end{bmatrix} \quad \textbf{(4-12)}$$

$$V_{DC} = \sum_{n=1}^{8} v_{c,\ n} \quad \textbf{(4-13)}$$

For an arbitrary number of sub-modules, the differential equations of the inductor current can be expressed as

$$L\begin{bmatrix} \dot{i}_{L,\ 1} \\ \dot{i}_{L,\ 2} \\ \dot{i}_{L,\ 3} \\ \vdots \\ \dot{i}_{L,\ \frac{N}{2}} \\ \vdots \\ \dot{i}_{L,\ N-3} \\ \dot{i}_{L,\ N-2} \\ \dot{i}_{L,\ N-1} \end{bmatrix} = \begin{bmatrix} \delta_1 & \delta_1 - 1 & & & & & & & & & \\ & \delta_2 & \delta_2 - 1 & & & & & & & & \\ & & \delta_3 & \delta_3 - 1 & & & & & & & \\ & & & \ddots & \ddots & & & & & & \\ & & & & \delta_{\frac{N}{2}} & \delta_{\frac{N}{2}} - 1 & & & & & \\ & & & & & \ddots & \ddots & & & & \\ & & & & & & \delta_{N-3} & \delta_{N-3} - 1 & & & \\ & & & & & & & \delta_{N-2} & \delta_{N-2} - 1 & & \\ & & & & & & & & \delta_{N-1} & \delta_{N-1} - 1 \end{bmatrix} \begin{bmatrix} v_{c,\ 1} \\ v_{c,\ 2} \\ v_{c,\ 3} \\ \vdots \\ v_{c,\ \frac{N}{2}} \\ v_{c,\ \frac{N}{2}+1} \\ \vdots \\ v_{c,\ N-2} \\ v_{c,\ N-1} \\ v_{c,\ N} \end{bmatrix} + r_L \begin{bmatrix} i_{L,\ 1} \\ i_{L,\ 2} \\ i_{L,\ 3} \\ \vdots \\ i_{L,\ \frac{N}{2}} \\ \vdots \\ i_{L,\ N-3} \\ i_{L,\ N-2} \\ i_{L,\ N-1} \end{bmatrix} \quad \textbf{(4-14)}$$

$$V_{DC} = \sum_{n=1}^{N} v_{c,\ n} \quad \textbf{(4-15)}$$

Using the capacitor voltage state space equation for an arbitrary number of capacitors, by adding the rows:

$$0 = \sum_{n=1}^{N} \mathrm{v}_{\mathrm{c,\ n}}^{\circ} = \left(\sum_{n=1}^{N-1} (1 - 2\delta_{\mathrm{n}})\, \mathrm{i}_{\mathrm{L,\ n}} \right) + N I_{s+} - \frac{N}{2} I_{out} \tag{4-16}$$

$$I_{s+} = \frac{I_{out}}{2} + \frac{1}{N} \left(\sum_{n=1}^{N-1} (1 - \delta_{\mathrm{n}})\, \mathrm{i}_{\mathrm{L,\ n}} \right) \tag{4-17}$$

4.1.3.3 Deriving the relation between I_{s+} , I_{s-} and I_{out}

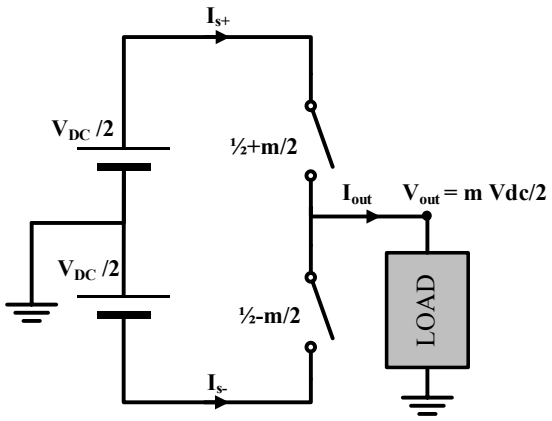


Figure 4-8. Simplified average model for single leg converter

Assuming lossless power conversion and neglecting the power cycling (charging and discharging) through capacitive and inductive components, the instantaneous load power is assumed equal to the supplied power i.e.

$$\frac{V_{DC}}{2} (I_{s+} - I_{s-}) = I_{out}\, V_{out} = (I_{s+} + I_{s-})\, V_{out} \tag{4-18}$$

$$I_{s+} + I_{s-} = I_{out} \tag{4-19}$$

Substituting in (4-18), using the node equation in (4-19)

$$I_{s+} - I_{s-} = \frac{V_{out}}{\frac{V_{DC}}{2}} I_{out} \tag{4-20}$$

The reference modulating signal is defined as

$$m = \frac{V_{out}}{\frac{V_{DC}}{2}} \tag{4-21}$$

Hence,

$$I_{s+} - I_{s-} = mI_{out} \tag{4-22}$$

Solving (4-19) and (4-22)

$$I_{s+} = I_{out}\left(\frac{1+m}{2}\right) \tag{4-23}$$

$$I_{s-} = I_{out}\left(\frac{1-m}{2}\right) \tag{4-24}$$

Figure 4-9 shows I_{s+} and I_{s-} for different load power factor angles of I_{out}.

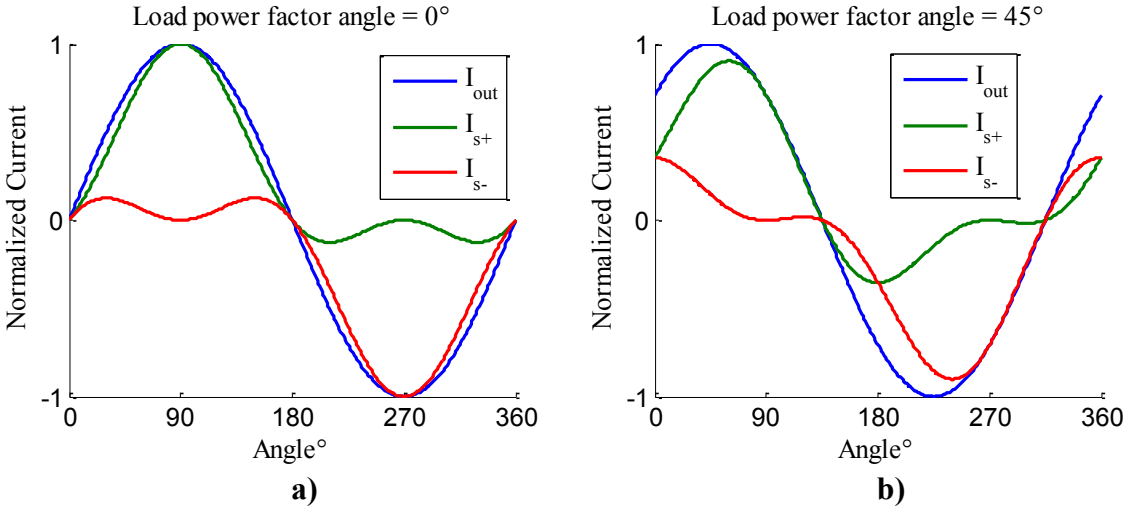
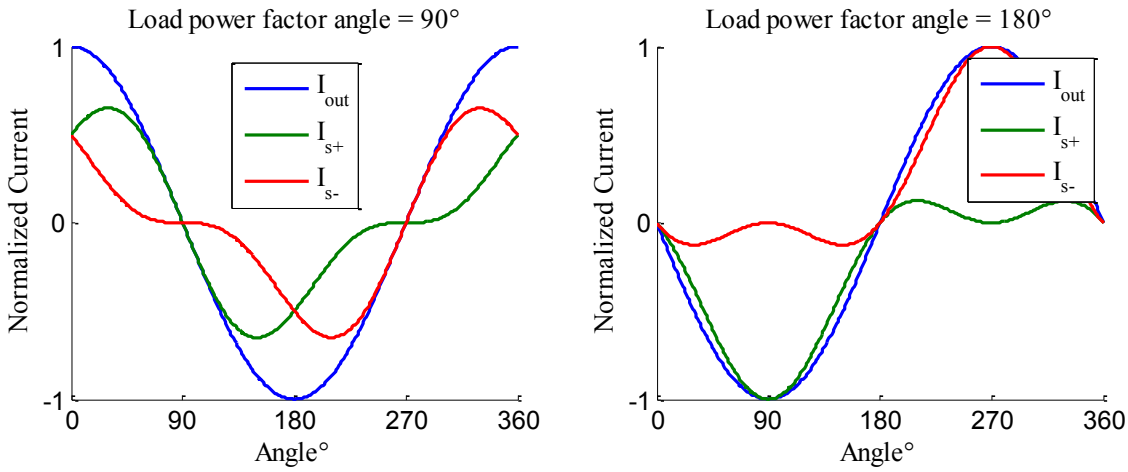


Figure 4-9. DC bus currents I_{s+} and I_{s-} for different load power factor angles



c) d)

Figure 4-9. Continued

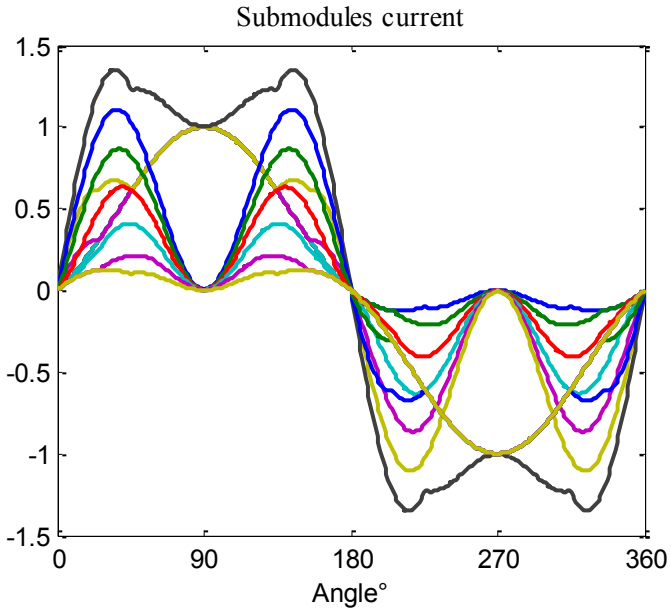


Figure 4-10. DC-AC IMMC submodule currents w.r.t. output current

4.1.4 Comparison between Various Multilevel Converter Topologies

Table 4-1 lists the number of semiconductor switching devices, and passive components required for the four topologies under study: Diode Clamped Multilevel Converter, Capacitor Clamped Multilevel Converter, Modular Multilevel Converter MMC and the Proposed DC-AC IMMC. Table 4-1 also estimates the total capacitive size requirement ratio between the four solutions based on [21-23, 25]. This data is then plotted in Figure 4-11 and Figure 4-12

From the comparison chart of Multilevel converters in Table 4-1 and Figure 4-11, it is noticed that Diode Clamped Multilevel Converter with 7 levels or more requires the highest number of components which makes it an unviable solution especially with its non-modular complex structure. On the other hand, Diode Clamped Multilevel Converter is the most favorable solution for low number of levels (3 or 4) because of low compotes count and simple control as compared to Capacitor Clamped Multilevel Converter as outlined in subsections 1.2 and 1.2.1.2.

MMC requires the least number of components for 7 levels or more which facilitates its employment in high voltage applications, however, at the expense of the complexity of capacitor voltage balancing control and extensive capacitor size requirement.

The proposed IMMC falls between MMC and conventional diode clamped and capacitor clamped converters in terms of component count, along with simple open loop control of capacitor voltages, and reduced size of passive components maintaining higher density as opposed to MMC.

Table 4-1. Comparison between Multilevel Converter Topologies (3 Phase) for "n" Level

Number of levels = n	**Diode Clamped Multilevel Converter [22]**	**Flying Capacitor Multilevel Converter [23]**	**Modular Multilevel Converter MMC [21, 25]**	**Proposed IMMC**
Number of modules	-	-	$6(n-1)$	$6(n-1.5)$
Number of switches	$6(n-1)$	$6(n-1)$	$12(n-1)$	$12(n-1.5)$
Number of Clamping Diodes	$3(n-1)(n-2)$			
Number of capacitors	$n-1$	$\frac{3}{2}\mathrm{n}(n-1)$	$6(n-1)$	$6(n-1.5)$
Number of inductors	-	-	6	$6(n-1.5)$
Total Components count	$(n-1)(3\mathrm{n}+1)+3$	$3(n-1)\left(\frac{\mathrm{n}}{2}+2\right)$+3	$18(n-1)+6$	$24(n-1.5)$
Capacitance ratio index	10	1	100	1
Capacitor Overall size index	$10(n-1)$	$\frac{3}{2}\mathrm{n}(n-1)$	$600(n-1)$	$6(n-1.5)$
Inductance ratio index			100	1
Inductance Overall size index			600	$6(n-1.5)$

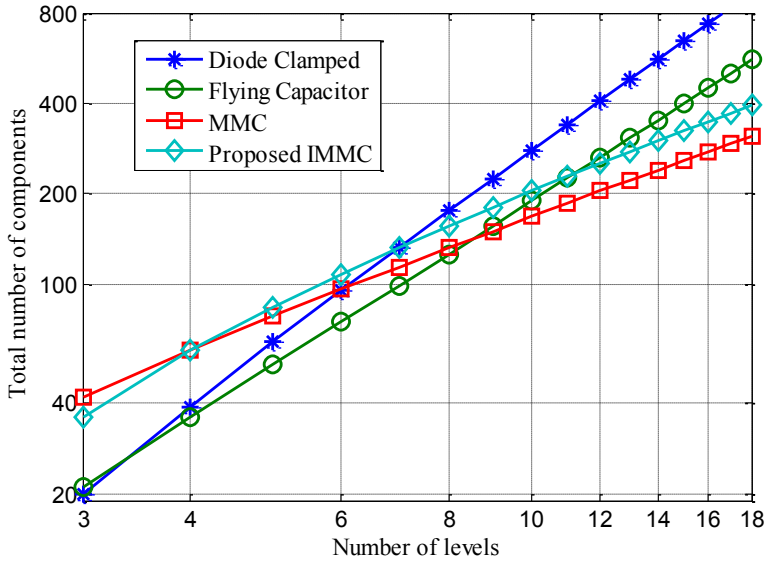


Figure 4-11. Total number of components for various multilevel converter topologies vs. number of levels (3 phase) based on Table 4-1

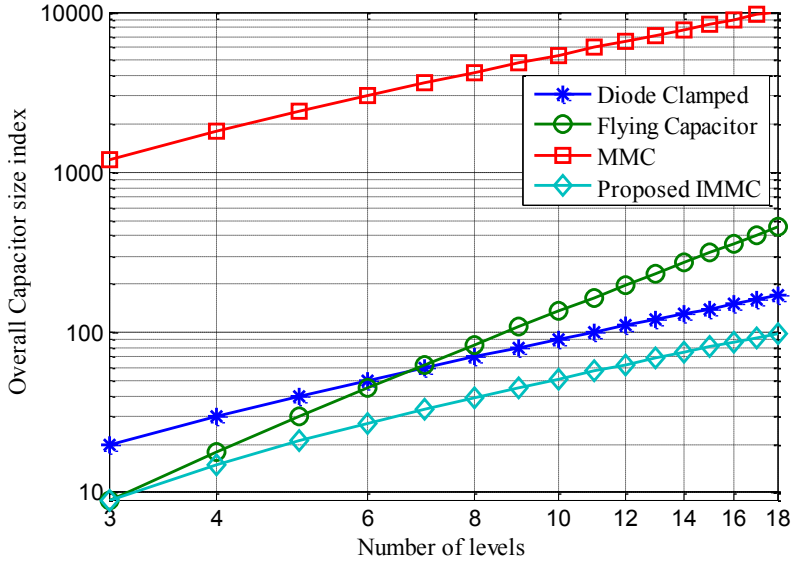
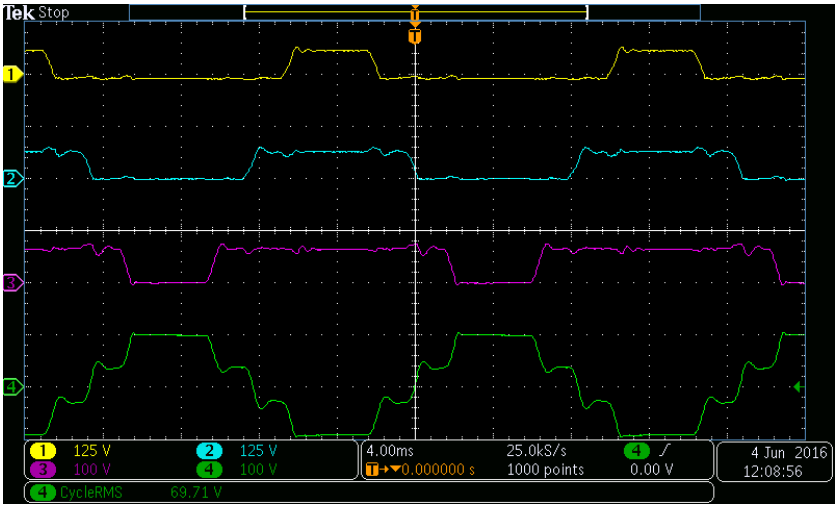


Figure 4-12. Overall capacitor size index

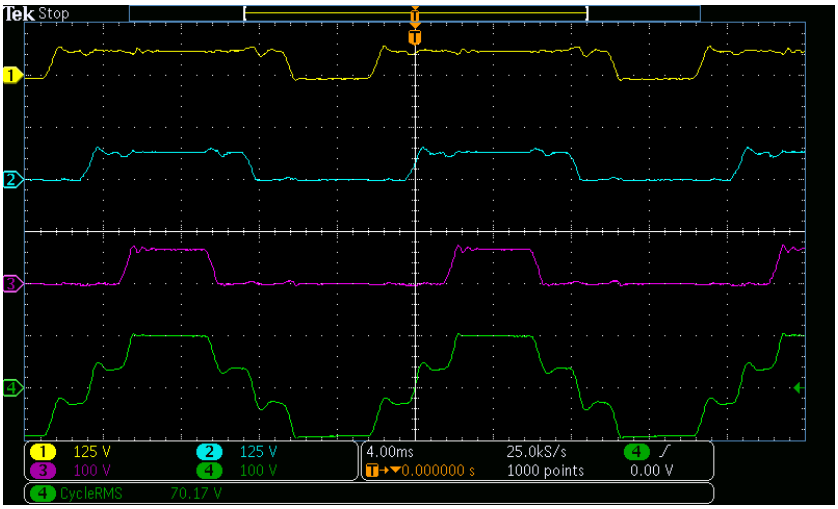
4.2 Experimental Results

4.2.1 Staircase Sinusoidal Reference (Submodule Duty = 0% , 50% or 100%)



a) Upper capacitor voltages

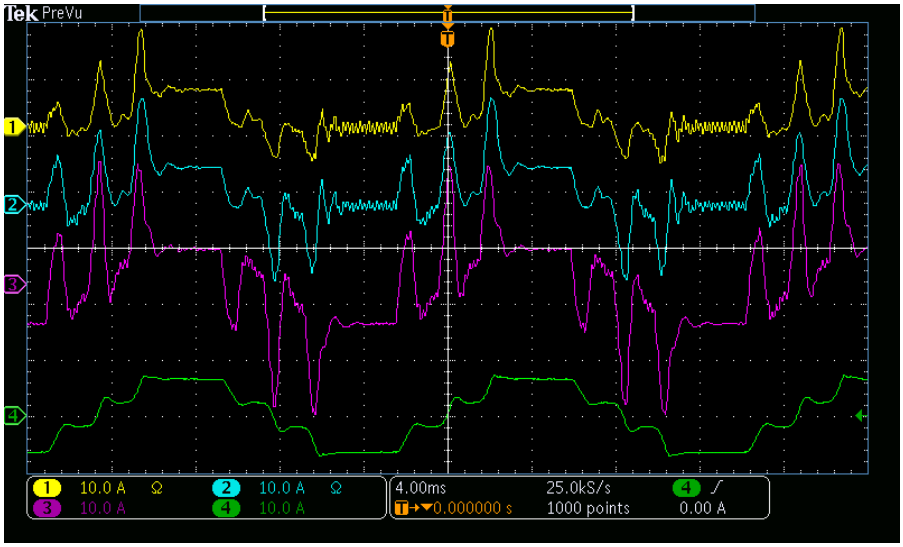
Channel 1: V_{C1}, Channel 2: V_{C2},
Channel 3: V_{C3}, Channel 4: Load Voltage V_{out}.



b) Lower capacitor voltages

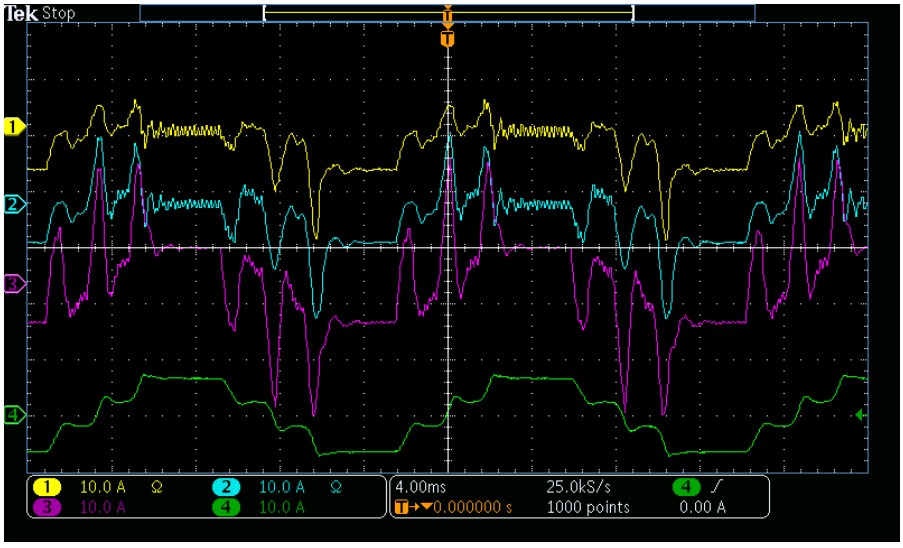
Channel 1: V_{C4}, Channel 2: V_{C5},
Channel 3: V_{C6}, Channel 4: Load Voltage V_{out}.

Figure 4-13. Submodules voltages and currents using staircase modulating reference



c) Lower submodule inductor currents

Channel 1: i_{SM1}, Channel 2: i_{SM2},
Channel 3: i_{SM3}, Channel 4: Load Current i_{out}.

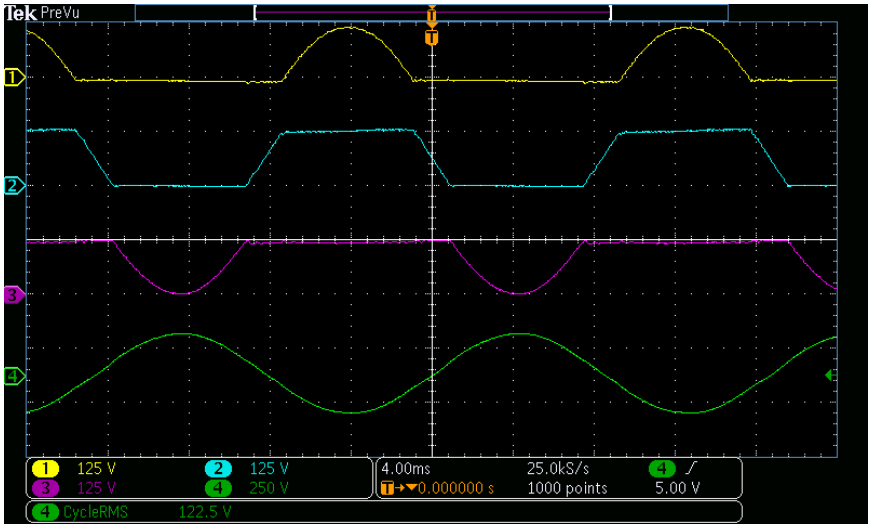


d) Lower submodule inductor currents

Channel 1: i_{SM5}, Channel 2: i_{SM4},
Channel 3: i_{SM3}, Channel 4: Load Current i_{out}.

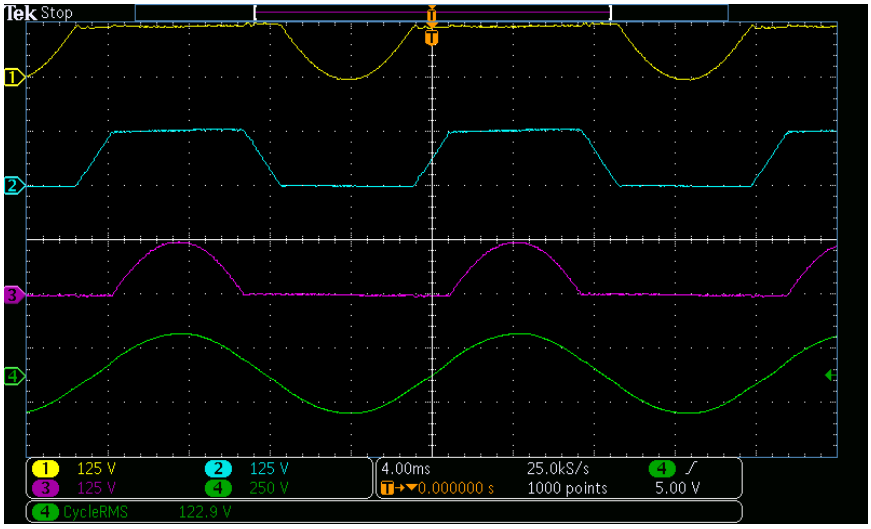
Figure 4-13. Continued

4.2.2 Sinusoidal Modulation Scheme (Duty Ratios are Calculated Based on Reference Voltages)



a) Upper capacitor voltages

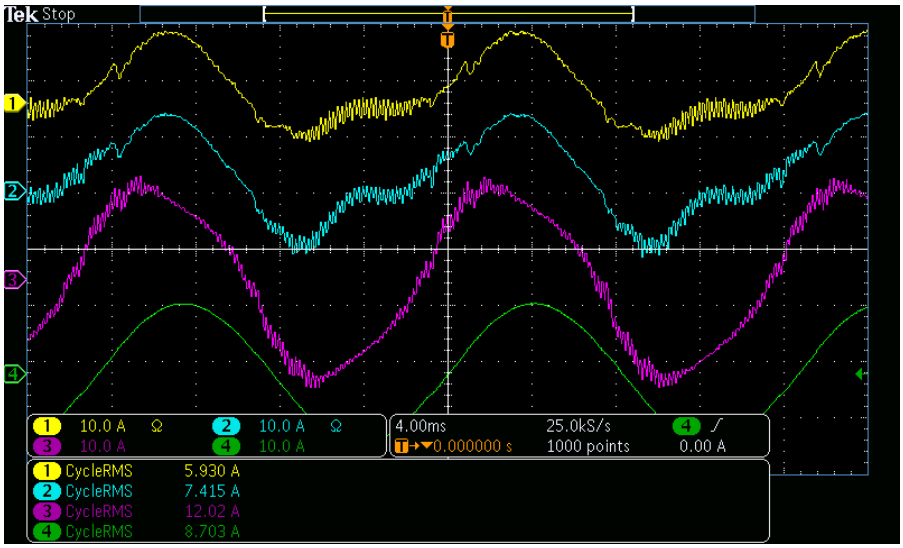
Channel 1: V_{C1}, Channel 2: V_{C2},
Channel 3: V_{C3}, Channel 4: Load Voltage V_{out}.



b) Lower capacitor voltages

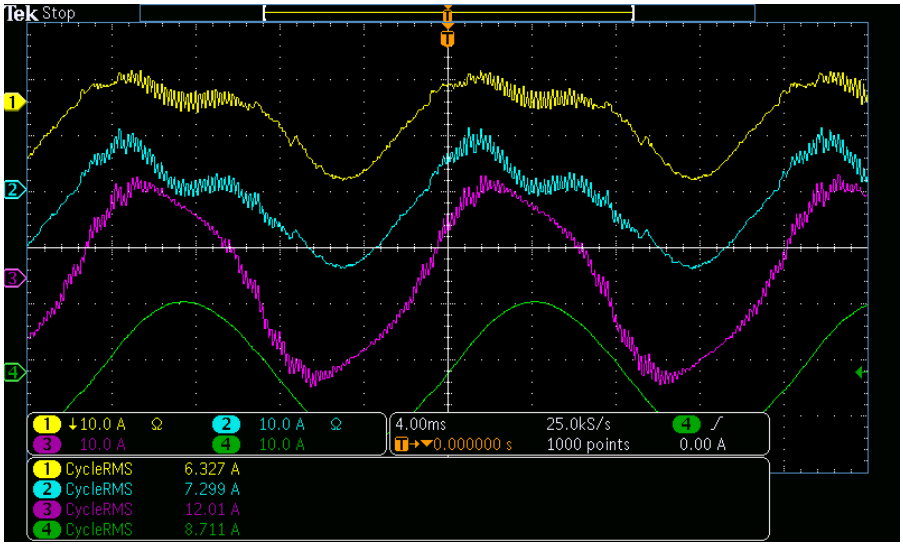
Channel 1: V_{C4}, Channel 2: V_{C5},
Channel 3: V_{C6}, Channel 4: Load Voltage V_{out}.

Figure 4-14. Submodules voltages and currents using sinusoidal modulating reference



c) Lower submodule inductor currents

Channel 1: i_{SM1}, **Channel 2:** i_{SM2},
Channel 3: i_{SM3}, **Channel 4:** Load Current i_{out}.



d) Lower submodule inductor currents

Channel 1: i_{SM5}, **Channel 2:** i_{SM4},
Channel 3: i_{SM3}, **Channel 4:** Load Current i_{out}.

Figure 4-14. Continued

4.2.3 V/F Operation (Ramp Up/Down) with Constant Resistive Load

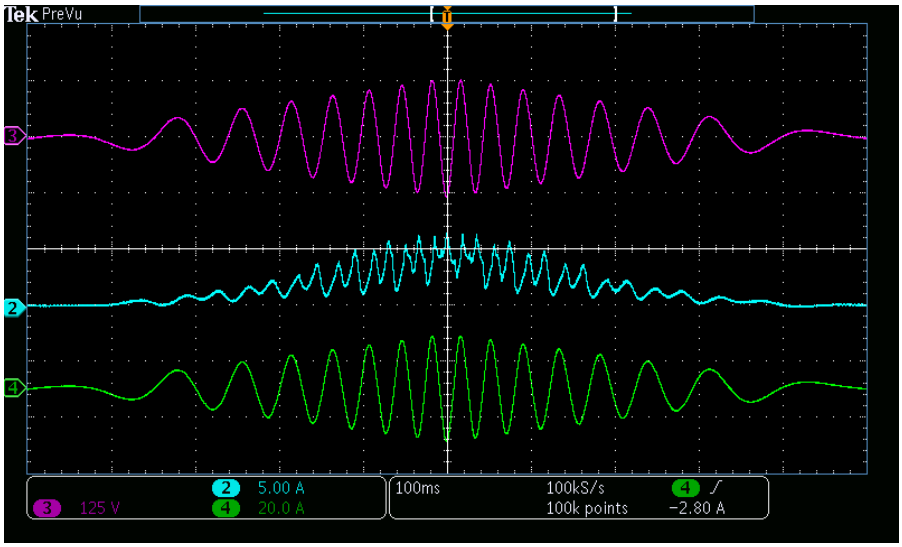


Figure 4-15. Ramp up down V/F

Channel 1: --, Channel 2: Supply Current i_{s+},
Channel 3: V_{out}, Channel 4: Load Current i_{out}.

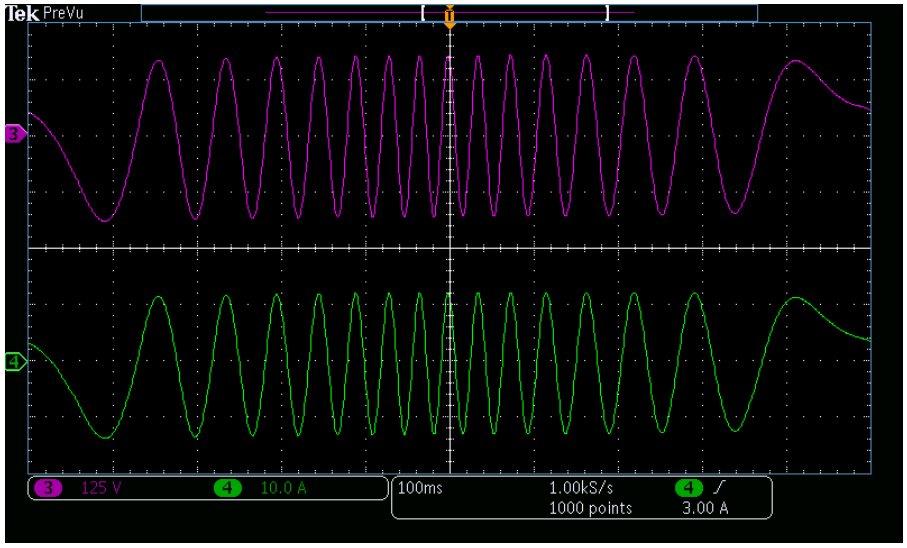


Figure 4-16. Ramp up down frequency, at constant reference Voltage

Channel 1: --, Channel 2: --,
Channel 3: V_{out}, Channel 4: Load Current i_{out}.

4.2.4 Third Harmonic Injection

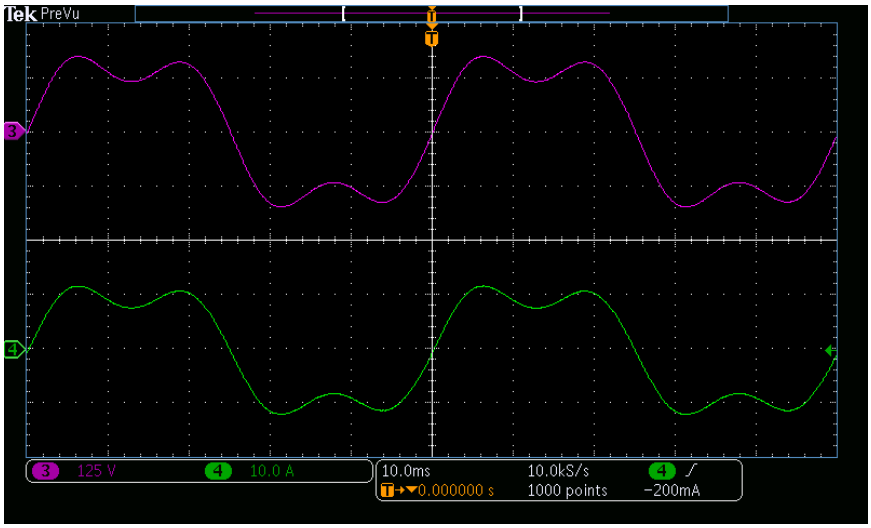


Figure 4-17. Third Harmonic Injection
Channel 3: V_{out}, Channel 4: Load Current i_{out}.

4.2.5 Step in Reference Voltage and Frequency

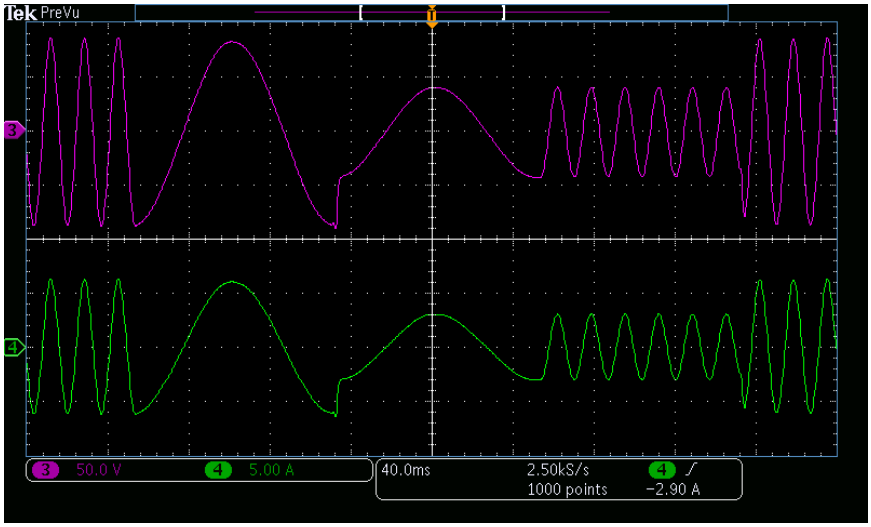
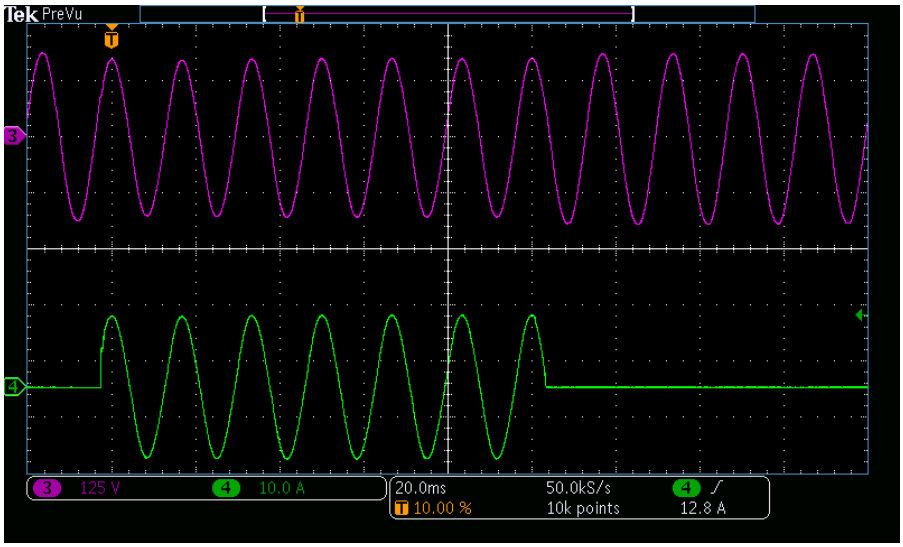
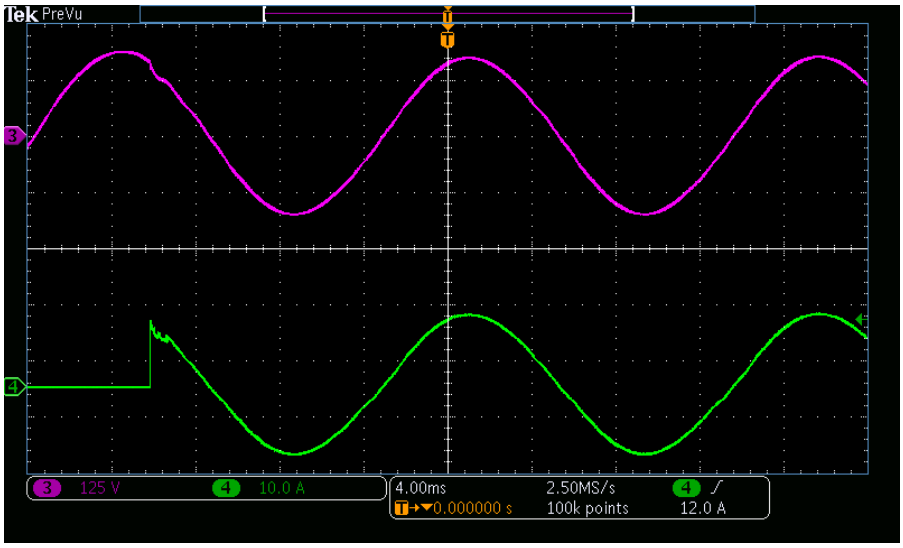


Figure 4-18. Step changes in reference voltage and frequency
Channel 3: V_{out}, Channel 4: Load Current i_{out}.

4.2.6 Step Change in Active Load



a)

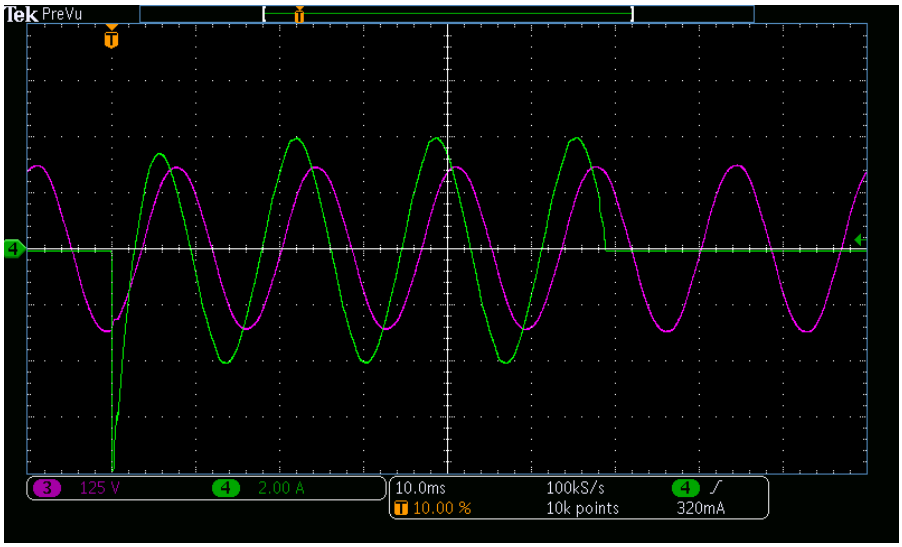


b)

Figure 4-19. Step change in active load
Channel 3: V_{out}, Channel 4: Load Current i_{out}.

4.2.7 Step Change in Reactive Load

a)



b)

Figure 4-20. Step change in reactive load
Channel 3: V_{out}, Channel 4: Load Current i_{out}.

4.3 Summary

In this section, the DC-AC IMMC concept was introduced as an extension for the DC-DC IMMC discussed in Section 3. The proposed DC-AC IMMC lends itself as a high density multilevel converter nullifying the need for the bulky capacitors associated with conventional MMC. The principles of the operation and the modulation technique were detailed achieving a smooth sinusoidal output voltage without any output filters.

Finally, the converter was evaluated through several experiments of sudden changes in voltage, frequency and loading conditions, which verified its performance.

5 SUMMARY AND FUTURE WORK

This dissertation is primarily concerned with improving power density aspects of power converters for low voltage single phase applications as well as high voltage multilevel converters. Three different converter schemes have been introduced, and experimental prototypes have been built to demonstrate the feasibility of the proposed topologies and control strategies.

In Section 1, a brief overview of Wide Band Gap semiconductor devices and their role in opening new venues for high efficiency and high power density in power conversion has been presented. Next, several multilevel converters topologies as the key enabling technology for high voltage and high power applications have been reviewed. Finally research objectives and dissertation outlines are clearly delineated.

In Section 2, a DC-AC single phase inverter with active power decoupling topology and control technique has been proposed. Furthermore, it was comprehensively compared to other active power decoupling methods in view of power density, efficiency and wide band gap SiC and GaN FETS available in market. The proposed method has been shown to be capable of cancelling the double line frequency ripples with minimal size passive and active components. The proposed topology better aligned with power density and efficiency constraints. The proposed active decoupling method has been prototyped for 2kW single phase inverter achieving a power density of 58W/inch^3 and experimentally tested under various loading conditions demonstrating its capability of accurate and fast cancellation of DC current ripples with active and reactive load transients.

In Section 3, a New High Power Density Interconnected Modular Multilevel DC-DC Converter suitable for high voltage high power applications has been proposed. The proposed topology has been shown to be fully modular, scalable and advantageous in terms of converter dynamics and size of the passive components. Full state space dynamic model of the presented topology has been derived. Moreover, this section proposed a ZVS scheme well suited for the introduced converter. This ZVS scheme enabled high efficiency of 98.35%, high power density and high utilization of the semiconductor switches. Experimental validation of the proposed IMMC topology, has demonstrated superior power density and dynamic response.

In Section 4, DC-AC IMMC has been proposed and its principle of operation has been discussed. Unlike the conventional MMC where bulky capacitors are indispensible, the proposed DC-AC IMMC has been shown to rely on very small filter capacitors, hence, allowing unprecedented levels of power density in high voltage power converters. Modulation methods have been presented and then experimentally validated demonstrating smooth output voltages and currents without installing additional output filters. Additionally the DC-AC IMMC prototype exhibited high performance under various testing scenarios of sudden changes in voltage, frequency and loading conditions.

5.1 Suggestions for future work

Continuation of the work in this dissertation would be to employ Wide Band Gap devices in the proposed IMMC. Then, create a detailed loss breakdown model for the proposed submodule using H-bridge with mutually coupled coils that includes

conduction, switching and gate drive losses in semiconductor devices, and copper and magnetic core losses in used inductors. This loss breakdown model will help to better optimize the submodule efficiency and power density.

The second suggestion is to perform a case study for implementation of DC-AC IMMC for medium voltage adjustable speed drives as a substitute for conventional industrial technologies, to confirm its feasibility in terms of reliability and fault tolerance.

REFERENCES

[1] *Little Box Challenge "Detailed Inverter Specifications, Testing Procedure and Technical Approach and testing Applicaition Requirements for the Little Box Challenge," https://www.littleboxchallenge.com/pdf/LBC-InverterRequirements-20150717.pdf [Online accessed 1-Oct-2015]*.

[2] W. Kim*, et al.*, "Analysis of the effects of inverter ripple current on a photovoltaic power system by using an AC impedance model of the solar cell," *Renewable Energy,* vol. 59, pp. 150-157, 2013.

[3] S. B. Kjaer and F. Blaabjerg, "Design optimization of a single phase inverter for photovoltaic applications," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual*, 2003, pp. 1183-1190 vol.3.

[4] S. Bala*, et al.*, "The effect of low frequency current ripple on the performance of a Lithium Iron Phosphate (LFP) battery energy storage system," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 3485-3492.

[5] D. V. d. l. Fuente*, et al.*, "Photovoltaic Power System With Battery Backup With Grid-Connection and Islanded Operation Capabilities," *IEEE Transactions on Industrial Electronics,* vol. 60, pp. 1571-1581, 2013.

[6] H. Hu*, et al.*, "A Review of Power Decoupling Techniques for Microinverters With Three Different Decoupling Capacitor Locations in PV Systems," *IEEE Transactions on Power Electronics,* vol. 28, pp. 2711-2726, 2013.

[7] P. T. Krein*, et al.*, "Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port," *IEEE Transactions on Power Electronics,* vol. 27, pp. 4690-4698, 2012.

[8] H. Li*, et al.*, "Active Power Decoupling for High-Power Single-Phase PWM Rectifiers," *IEEE Transactions on Power Electronics,* vol. 28, pp. 1308-1319, 2013.

[9] Z. Qin*, et al.*, "Benchmark of AC and DC Active Power Decoupling Circuits for Second-Order Harmonic Mitigation in Kilowatt-Scale Single-Phase Inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 4, pp. 15-25, 2016.

[10] I. Serban, "Power Decoupling Method for Single-Phase H-Bridge Inverters With No Additional Power Electronics," *IEEE Transactions on Industrial Electronics,* vol. 62, pp. 4805-4813, 2015.

[11] R. Wang, *et al.*, "A High Power Density Single-Phase PWM Rectifier With Active Ripple Energy Storage," *IEEE Transactions on Power Electronics,* vol. 26, pp. 1430-1443, 2011.

[12] A. S. Morsy, *et al.*, "High power density single phase inverter using GaN FETS and active power decoupling for Google Little Box Challenge," in *Wide Bandgap Power Devices and Applications (WiPDA), 2015 IEEE 3rd Workshop on*, 2015, pp. 323-327.

[13] A. Morsy and P. Enjeti, "Comparison of Active Power Decoupling Methods for High Power Density Single Phase Inverters Using Wide band Gap FETS for Google Little Box Challenge," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. PP, pp. 1-1, 2016.

[14] T. Ueda, "Reliability issues in GaN and SiC power devices," in *2014 IEEE International Reliability Physics Symposium*, 2014, pp. 3D.4.1-3D.4.6.

[15] C. Sintamarean, *et al.*, "Wide-band gap devices in PV systems - opportunities and challenges," in *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, 2014, pp. 1912-1919.

[16] J. Mill, *et al.*, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics,* vol. 29, pp. 2155-2163, 2014.

[17] J. Rodriguez, *et al.*, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics,* vol. 49, pp. 724-738, 2002.

[18] J. Rodriguez, *et al.*, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Transactions on Industrial Electronics,* vol. 54, pp. 2930-2945, 2007.

[19] F. Z. Peng, *et al.*, "Recent advances in multilevel converter/inverter topologies and applications," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 492-501.

[20] A. Marzoughi, *et al.*, "Design and comparison of cascaded H-bridge, modular multilevel converter and 5-L active neutral point clamped topologies for drive application," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 4033-4039.

[21] S. Debnath, *et al.*, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Transactions on Power Electronics,* vol. 30, pp. 37-53, 2015.

[22] A. Nabae, *et al.*, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Transactions on Industry Applications,* vol. IA-17, pp. 518-523, 1981.

[23] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, 1992, pp. 397-403 vol.1.

[24] P. Fang Zheng, *et al.*, "A multilevel voltage-source inverter with separate DC sources for static VAr generation," *IEEE Transactions on Industry Applications,* vol. 32, pp. 1130-1138, 1996.

[25] M. Hagiwara, *et al.*, "A Medium-Voltage Motor Drive With a Modular Multilevel PWM Inverter," *IEEE Transactions on Power Electronics,* vol. 25, pp. 1786-1799, 2010.

[26] I. A. Gowaid, *et al.*, "Analysis and Design of a Modular Multilevel Converter With Trapezoidal Modulation for Medium and High Voltage DC-DC Transformers," *IEEE Transactions on Power Electronics,* vol. 30, pp. 5439-5457, 2015.

[27] H. Mhiesan, *et al.*, "High Step-Up/Down Ratio Isolated Modular Multilevel DC-DC Converter for Battery Energy Storage Systems on Microgrids," in *2016 IEEE Green Technologies Conference (GreenTech)*, 2016, pp. 24-28.

[28] X. Zhang and T. C. Green, "The Modular Multilevel Converter for High Step-Up Ratio DC-DC Conversion," *IEEE Transactions on Industrial Electronics,* vol. 62, pp. 4925-4936, 2015.

[29] F. H. Khan and L. M. Tolbert, "A Multilevel Modular Capacitor Clamped DC-DC Converter," in *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, 2006, pp. 966-973.

[30] F. H. Khan and L. M. Tolbert, "A 5 kW Bi-directional Multilevel Modular DC-DC Converter (MMCCC) Featuring Built in Power Management for Fuel Cell and Hybrid Electric Automobiles," in *2007 IEEE Vehicle Power and Propulsion Conference*, 2007, pp. 208-214.

[31] F. H. Khan and L. M. Tolbert, "Bi-directional power management and fault tolerant feature in a 5-kW multilevel dc-dc converter with modular architecture," *IET Power Electronics,* vol. 2, pp. 595-604, 2009.

[32] *Rohm SCT2120AF MOSFET,* http://rohmfs.rohm.com/en/products/databook/datasheet/discrete/sic/mosfet/sct2120af-e.pdf *[Online accessed 20-May-2016]*.

[33] *Wolfspeed, C3M0065090J Silicon Carbide Power MOSFET, http://www.wolfspeed.com/downloads/dl/file/id/145/product/1/c3m0065090j.pdf [Online accessed 20-May-2016]*.

[34] *Wolfspeed, C2M0280120D Silicon Carbide Power MOSFET, http://www.wolfspeed.com/downloads/dl/file/id/171/product/12/c2m0280120d.pdf [Online accessed 20-May-2016]*.

[35] *EPC, EPC2010 GaN FET [Online accessed 20-May-2016] http://epcco.com/epc/Portals/0/epc/documents/datasheets/EPC2010_datasheet.pdf [Online accessed 20-May-2016]*.

[36] *Transphorm, TPH3205WS GaN FET http://www.transphormusa.com/sites/default/files/public/TPH3205WS%20v6.pdf [Online accessed 20-May-2016]*.

[37] *GaN Systems, GS66508P enhancement mode GaN transistor, http://www.gansystems.com/datasheets/20150904/GS66508P%20DS%20Rev%20151016.pdf [Online accessed 20-May-2016]*.

[38] D. C. Sheridan*, et al.*, "Ultra-Low Loss 600V - 1200V GaN Power Transistors for High Efficiency Applications," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, 2014, pp. 1-7.

[39] *"2015 Magnetics Powder Core Catalog" www.mag-inc.com/.../2015-Magnetics-Powder-Core-Catalog.pdf [Online accessed 1-Oct-2015]*.

[40] Z. Keliang and W. Danwei, "Relationship between space-vector modulation and three-phase carrier-based PWM: a comprehensive analysis [three-phase inverters]," *IEEE Transactions on Industrial Electronics,* vol. 49, pp. 186-196, 2002.

[41] K. Filsoof and P. W. Lehn, "A Bidirectional Multiple-Input Multiple-Output Modular Multilevel DC-DC Converter and its Control Design," *IEEE Transactions on Power Electronics,* vol. 31, pp. 2767-2779, 2016.

[42] K. Filsoof and P. W. Lehn, "A Bidirectional Modular Multilevel DC–DC Converter of Triangular Structure," *IEEE Transactions on Power Electronics,* vol. 30, pp. 54-64, 2015.

[43] M. Kasper*, et al.*, "Novel high voltage conversion ratio "Rainstick" DC/DC converters," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 789-796.

[44] A. Morsy, *et al.*, "A new high power density modular multilevel DC-DC converter with localized voltage balancing control for arbitrary number of levels," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2567-2572.

[45] K. Kesarwani, *et al.*, "A multi-level ladder converter supporting vertically-stacked digital voltage domains," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, 2013, pp. 429-434.