INTEGRATED CIRCUIT DESIGN FOR SILICON PHOTONICS INTERCONNECTS

A Dissertation

by

KUNZHI YU

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Chair of Committee,	Samuel Palermo
Committee Members,	Kamran Entesari
	Christi K. Madsen
	Eun Jung Kim
Head of Department,	Miroslav M. Begovic

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ABSTRACT

For next generation interconnects which implement in datacenter and high-performance computing system, silicon photonic interconnect provides a high bandwidth, low power efficiency solution. Optical interconnect architectures based on microring resonator devices offer a low-area and energy-efficient approach to realize both high-speed modulation and high bandwidth density via wavelength division multiplexing. This paper presents a multi-channel hybrid-integrated photonic receiver based on microring drop filters and waveguide photodetectors implemented in a 130nm SOI process and high-speed optical front-ends designed in 65nm CMOS. When tested with a waveguide photodetector with 0.45A/W responsivity, the receiver achieves -8.0 dBm OMA sensitivity at a BER=10-12 with a jitter tolerance corner frequency near 20MHz and a per-channel power consumption of 17mW including amortized clocking power. In order to stabilize the microring drop filter resonance wavelength, a peak-detector-based thermal tuning loop is implemented with a 0.7nm range at 43µW/GHz efficiency.

Mach–Zehnder-based modulator provides a high bandwidth, high linearity, good thermal insensitivity solution for silicon photonics transmitters design. This paper presents a 56Gbps PAM4/NRZ reconfigurable Si-photonics transmitter design which consists a 16nm FinFET CMOS transmitter flip-chip bonded to a 130nm SOI Mach–Zehnder modulator. The Mach–Zehnder modulator consists total 14 segmented phase shifter pairs which 5 segments works as LSB and 9 segments works as MSB in order to

generate 4-level Pulse-Amplitude Modulation (PAM4) optical signal in optical domain combination. The CMOS transmitter implements 28 push-pull drivers to achieve dual arm, dual differential driving scheme and independently digital control delay lines to achieve delay match between optical and electrical signal propagation. The MZM transmitter achieves 7ps eye-width and 0.963 RLM at 56Gbps data rate.

DEDICATION

To my wife, Weinan Zhu.

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I feel so lucky that I could join analog and mixed signal group in Texas A&M University since 2013. Five years study and research with so many wonderful professors, students, visit researchers, and staffs makes my Ph.D. research and this dissertation happens.

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1. INTRODUCTION

There has been a tremendous rise in the amount of data traffic which could be human-driven, due to increased video content and the rise of social media, and machine-driven due to cloud computing and IoT. It results in a projected total data center traffic of over 19 Zettabytes in 2019. The solution of 100Gbps data rate with varied link distance from 20inch backplane electrical to 100m VCSEL based link and long-haul coherent optical link is well developed nowadays. The data center interconnects now are upgrading 100Gbps to a need for 400Gbps and even 1Tb/s data rate which require higher bandwidth and better power efficiency [1]. Meanwhile, the high-performance computing (HPC) system are currently limited by interconnect bandwidth. The network-on-chip [2, 3] needs high throughput, low power on-chip interconnects [4] to transfer data between multiprocessor cores. This rapid expansion in data communication also necessitates improvements in optical receiver circuitry's bandwidth and power efficiency.

Silicon photonic interconnects offer a high bandwidth and high-density solution using wavelength division multiplexing (WDM) and a scalable solution to meet growing bandwidth demand. As show in figure 1.1, a typical silicon photonics transceiver design is described. More common in silicon photonics design, the optical modulator [5,6] can modulate the external laser source to generate modulated optical signal. And the modulated optical signal will route through the optical channel, such as single mode fiber, on-chip single mode waveguide and optical interposer waveguide. The optical filters at receiver side are implemented for WDM application and on-chip waveguide

photodiodes [7-8] will convert optical signal to electrical domain. The receiver front-end consists of transimpedance amplifier and linear amplifier to recover the modulated electrical signal. Furthermore, clock and data recover (CDR) module will de-serialize the signal from analog front end.

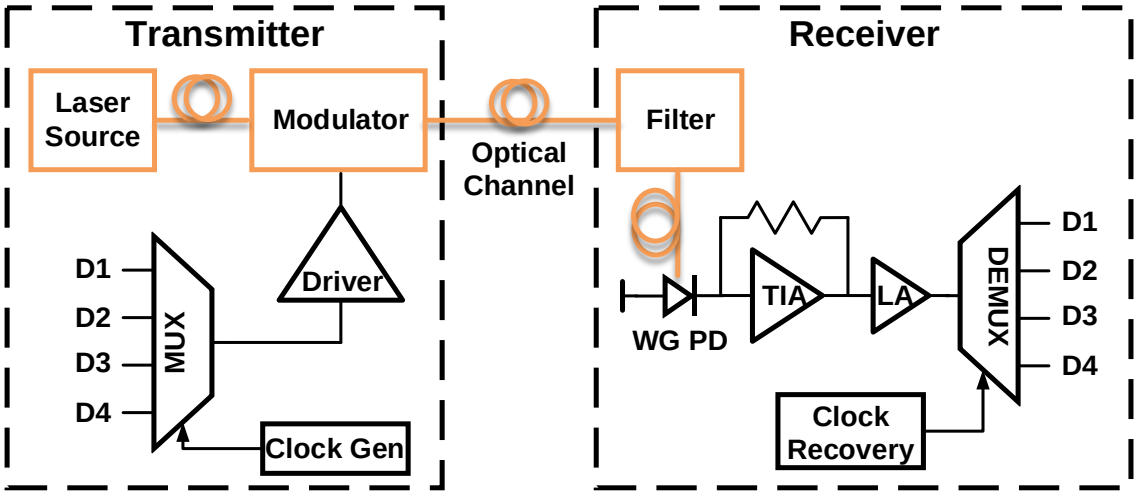

Figure 1.1. A typical structure of silicon photonics interconnects.

While there is a challenge to increase single channel baud rate due to either optical or electrical bandwidth limitation, further boosting data rate of the interconnect system could be realized by increasing the number of wavelengths per fiber. Chapter 3 introduces a silicon photonics receiver design based on WDM microring drop filter. The CMOS circuit and photonics integration circuit (PIC) enables a 4 channel WDM with one common bus waveguide and single mode fiber as optical channel. The CMOS receiver design implemented source synchronous receiver structure to minimized clocking complexity and low noise analog front end to improve system sensitivity.

Besides increasing number of wavelengths per fiber, the use of multilevel signaling instead of non-return to zero (NRZ), allows the use of a smaller bandwidth optical transceiver to relax the both optical device and circuitry frequency constraints. For example, 4-level pulse amplitude modulation (PAM-4) scheme provides 2 transmitted bits per symbol and increases the throughput at a given bandwidth. In this dissertation, chapter 4 illustrates a configurable PAM4 silicon photonics transmitter to achieve 56Gbps data rate per wavelength which double the most NRZ transceiver design [9-10].

Silicon photonics technology are highly developed recently, however, there are still some major issues on integration between electronics and photonics and system performance degradation introduced by process and environment change. The monolithic integration is an approach which the optical devices and electronics circuits are fabricated on the same chip. However, this approach faces the difficult because of the design conflicts in optimized optical and electrical design. The heterogeneous or hybrid integration complexity will be increased dramatically due to huge number of IO footprint. The signal integrity would be a critical part in system design due to the package parasitic capacitance and inductor. In chapter 4, the transmitter design implements a 2.5D integration which use die to die flip-chip bonding to minimize the parasitic parameter. In the WDM system, the working wavelength need stable alignment from laser, modulator to optical filter. The process and environment variation need carefully calibrated and compensated in system level design. Chapter 3 described a

wavelength stabilization loop design which can be used to compensate process mismatch and temperature changes.

Overall, silicon photonics provide high bandwidth density and power efficiency solution for short-middle ranch optical interconnects. The dissertation focuses on the design techniques in both electrical circuitry and optical device optimization. The dissertation is organized as follow. Chapter 2 describes the background knowledge of silicon photonics interconnects including the optical devices which are used in different silicon photonics interconnects system, and an overview of system level integration method of silicon photonics transceivers. Then two silicon photonics interconnects design are discussed. Chapter 3 presents a multi-channel hybrid-integrated silicon photonics receiver based on the microring filter and waveguide photodiode. And a reconfigurable Si-photonic transmitter which consists a 16nm FinFET CMOS IC flip-chip bonded to a 130nm SOI Mach–Zehnder modulator is proposed in chapter 4. Finally, chapter 5 concludes the thesis.

2. BACKGROUND

This chapter provides an overview of silicon photonics interconnects system, from optical devices to system level integration methodology. The chapter begins with brief introduction of silicon photonics devices such as laser sources, fiber coupler, waveguide photodiode, optical filter and optical modulator. Two type of modulator which are commonly used in silicon photonics interconnect system, micro-ring resonator modulator (MRM) and Mach-Zehnder modulator (MZM), are also compared. Then, this section gives an introduction of the system integration of optical devices and advanced circuit design.

2.1 Integrated Photonics Devices for Interconnects

2.1.1 Laser Sources

The transmitter design of optical interconnects can either be direct modulated laser source or external modulation of continuous wave (CW) laser source with optical modulator. Vertical-cavity surface-emitting lasers (VCSEL) are commonly used in high speed optical communication system as direct modulated lasers source due to good power efficiency and high modulation data rate. Distribute Feedback Lasers (DFBs) sometimes are used as external laser source of silicon photonics because single frequency can be easily achieved and single mode laser generation.

However, in order to achieve wavelength-division-multiplexing (WDM) both VCSELs and DFBs have some big challenges in multiplexing multi wavelength laser source in a compact and low-loss manner. Quantum-Dot Comb Laser can generate a set of wavelength lasers which can enable WDM link requirement as reference [11]

described. The comb laser output power level can reach 1-2mW per wavelength with 10% Wall-plug efficiency and stable channel spacing. Meanwhile, directly modulated heterogeneous/hybrid microring lasers consists of an InP-based III-V epitaxial layer structure on a silicon-on-insulator (SOI) substrate can provide direct modulated laser sources in micro-ring aspect [12-13]. Both approaches provide potential solution for WDM silicon photonics interconnects.

2.1.2 Waveguide and Fiber Coupler

Waveguide is the fundamental optical device of Si photonics platform, and it is used in routing the laser on the photonics integrated circuit (PIC). As shown in figure 2.1, the Si-waveguide consists a core with high index of fraction, and cladding materials with lower index of refraction. Typically, there are two types of waveguides, rib waveguide and strip waveguide. The rib waveguide is mostly used in the electro-optic devices such as optical modulators, the rib can be used as electrical connection to change the index and generate phase shift. The strip waveguide, also known as channel waveguide, is mostly used for optical routing since it offers tight bend radii [14]. Different insertion loss and phase shift requirement in different require different material design for both waveguide core and cladding. The waveguide losses are related with several different aspects such as absorption loss, scattering loss introduced by either side-wall etch roughness or surface roughness and bending loss [15]. Besides the optical loss, the phase shift and propagation delay introduced by waveguide are also important in MZM modulator design.

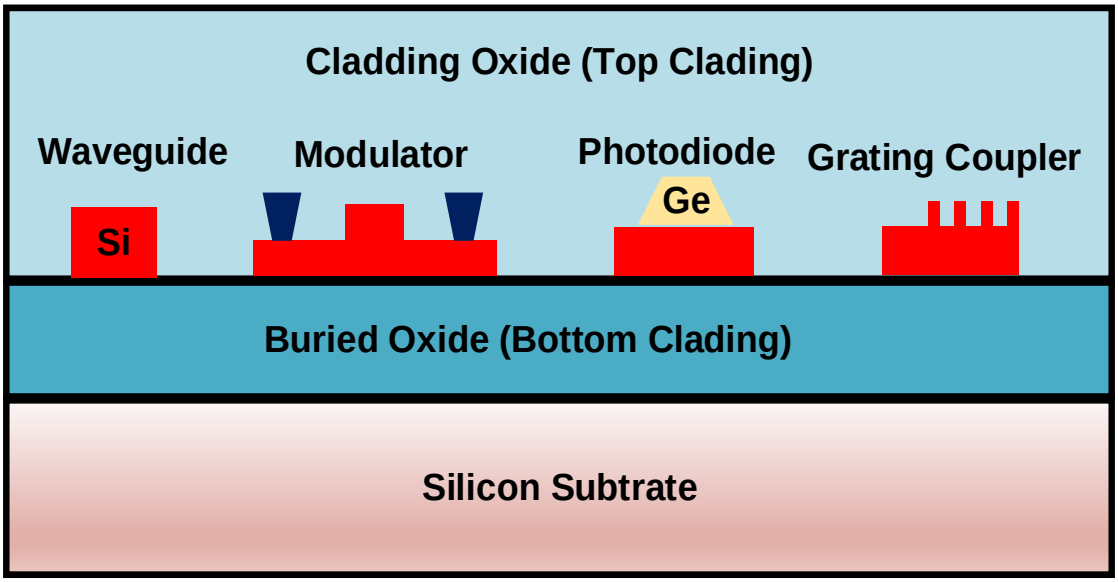

Figure 2.1 Si-photonics platform with grating coupler, waveguide, waveguide photodiode, modulator.

Fiber coupler is the passive optical device direct the laser from optical fiber into or out of photonic integration circuit (PIC). Most commonly used in silicon photonic system is vertical grating coupler [16]. The vertical grating coupler is a passive device with periodic structure, and fiber aligned with grating coupler with static angle. The coupler efficiency is a key parameter in link budget analysis, and it is related with three main factors: insertion loss, mode mismatch, back reflection.

2.1.3 Waveguide Photodiode

Optical link uses photodetector to convert optical signal to electrical domain to further amplification and decision circuit. The photodiode which are mostly used photodetector absorbs optical energy and generates accumulated charge carriers in junction. At the telecom application wavelength, silicon could not absorb the light

efficiently, some other material with narrower bandgap than silicon need to be integrated as the absorption medium. Germanium or SiGe can be grown on SOI substrate and absorb light at the specific wavelengths [17]. III-V materials such as INP and InGaAs are also used for photoreaction. In silicon photonics fabrication technology, extra wafer bonding process is required for III-V materials [18]. The III-V materials have better quantum efficiency than Germanium, however, wafer bonding would introduce high device capacitance which degrade the O/E bandwidth of photodiode.

Avalanched photodiode (APD) is a high sensitivity photodiode due to the internal gain amplification of photocurrent. The internal gain of an APD comes from the following semiconductor impact ionization property: at high enough electric field, high kinetic energy carriers bombard electronic bounds, losing their energies and creating multiple carriers [19]. The avalanched photodiode enables a break though the trade-off of O/E bandwidth and responsivity.

2.1.4 Mach-Zehnder Modulator

One effective mechanism for changing the effective index of a silicon waveguide is called plasma dispersion effect [14]. Plasma dispersion effect is an electro-optic effect that can change the refraction index and waveguide loss by changing the carrier density of a waveguide. At 1550nm wavelength, the change of effective index and waveguide loss due to the change of carrier density can be describe by equation 2.1 and 2.2

$$\Delta n\ (@1550nm) = -8.8 * 10^{-22}\Delta N - 8.5 * 10^{-18}\Delta P^{0.8} \quad (2.1)$$

$$\Delta \alpha\ (@1550nm) = -6.2 * 10^{-22}\Delta N - 6 * 10^{-18}\Delta P^{0.8} \quad (2.2)$$

where ΔN and ΔP represents the change of electrons density and holes density, respectively.

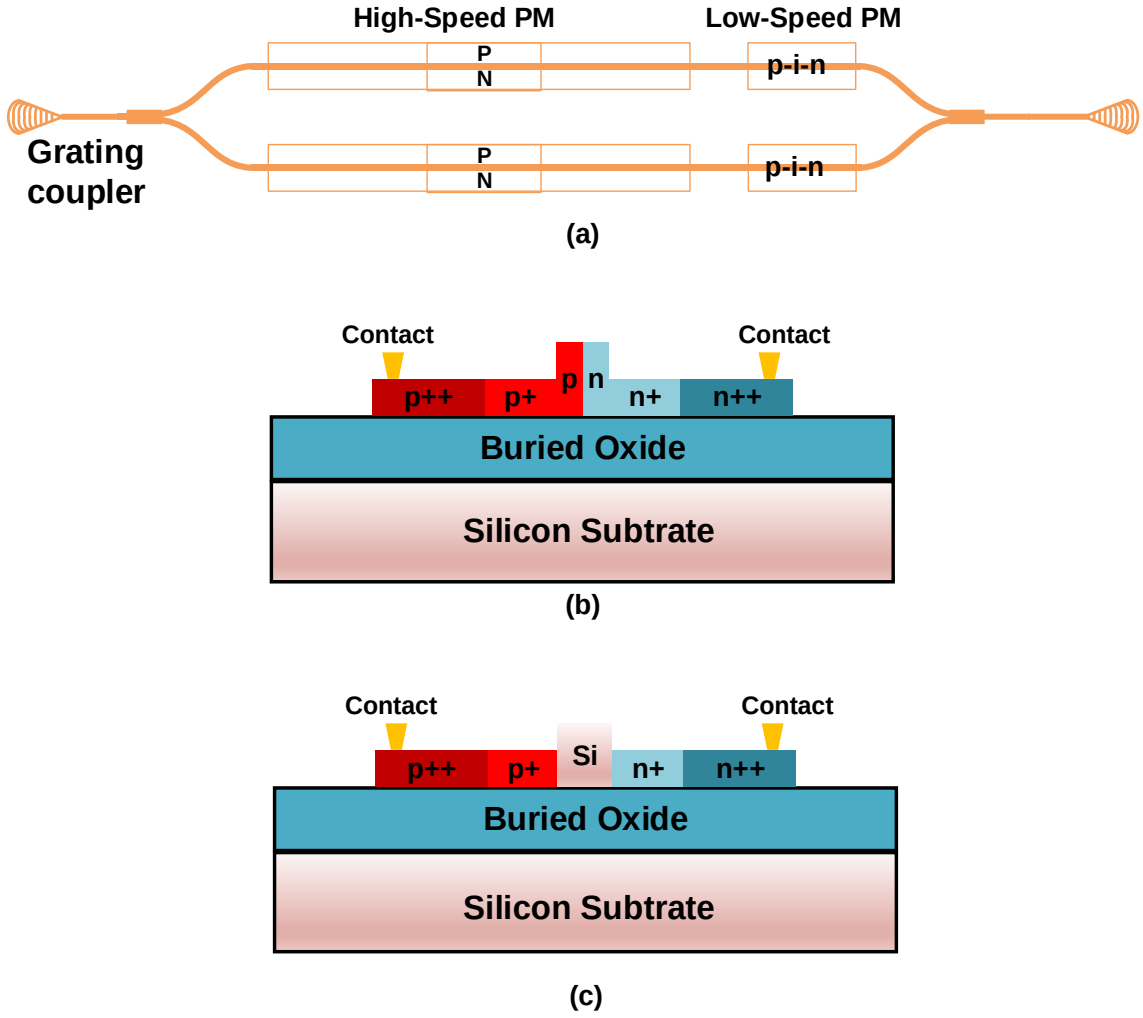

Figure 2.2 (a) Mach-Zehnder modulator top-view schematic (b) cross section view of HSPM (c) cross section view of LSPM

As shown in figure 2.2, a Mach-Zehnder modulator device consists of optical components including high speed phase modulator (HSPM), low speed phase modulator (LSPM), Y Branch and grating couplers [20]. As illustrated in the cross-section in Figure

2.1(b), HSPM is a lateral p-n diode ridge waveguide which is the key optical component that determines the O/E bandwidth of MZM device. The doped ridge waveguide consists of lightly doped p-n junction and heavily doped p++ and n++ implant for contact [21]. With reverse bias voltage applied on p-n diode region, the refractive index change can generate dynamic optical phase shift modulation at the depletion region. The low-speed phase modulator (LSPM) is developed to tuning the MZM optical properties, for example, the optical phase for MZM device quadrature phase bias and resonance wavelength tuning for MRM. One commonly used LSPM in silicon photonic platform is the p-i-n phase modulators (p-i-n PM) [22]. The p-i-n phase modulator is used in forward biased condition at carrier injection mode to create the change of refractive index. Thus p-i-n has relative high modulation power efficiency and low modulation speed.

The amplitude modulation (AM) mechanism of MZM could be explained as following statement. With the continuous-wave light source being split evenly into two phase shifter arms, while an electrical field forced by the reverse-biased voltage applied on each of the HSPM arms inducing a change in the carrier density, which, in turn induces a phase shift as the optical wave propagates in the arms. Depending on the relative E-field polarity applied on the HSPM arms, the two paths of lights interfere either constructively or destructively when they combine together at the output. The phase modulation is converted into intensity modulation at the combiner.

The output optical power can be derived as shown in Equation 2.3.

$$P_{out} = P_{in} * \frac{1}{2} * [1 + \cos(\varphi_1 - \varphi_2)] \qquad (2.3)$$

Pin and Pout are the input laser power and MZM output power, respectively. Here, φ1 and φ2 are the absolute phase shift of the two arms

$$\varphi_1 - \varphi_2 = \Delta\varphi + \varphi_{mod} \tag{2.4}$$

The phase-shift difference can be realized by a static phase shift $\Delta\varphi$ plus a modulation component φ_{mod} . The static phase shift difference $\Delta\varphi$ is introduced by means of a low-speed phase modulator (LSPM). And φ_{mod} is introduced by HSPM modulated by external voltage signal with equation 2.5

$$\varphi_{mod} = \pi * \frac{V_m * L_{HSPM}}{V_\pi * L_\pi} \tag{2.5}$$

Where VπLπ in the units of V -cm, is defined as the product of the driver voltage height and the MZM length to generate a phase shift of π. Vm is the modulation voltage swing of HSPM and L_{HSPM} is the effective length of the HSPM.

2.1.5 Microring Resonator

Microring resonator provide a potential solution for large scale integration of optics and electronics. It can be configured as optical modulator and WDM drop filter. Compare with MZM, it offers small footprint size and intrinsic WDM solution. Figure 2.3 presents the structure of an add-drop Si photonics microring. A straight though waveguide is coupled with a circle waveguide. Meanwhile. the drop port is introduced by adding another straight waveguide coupled to the other side of circle waveguide.

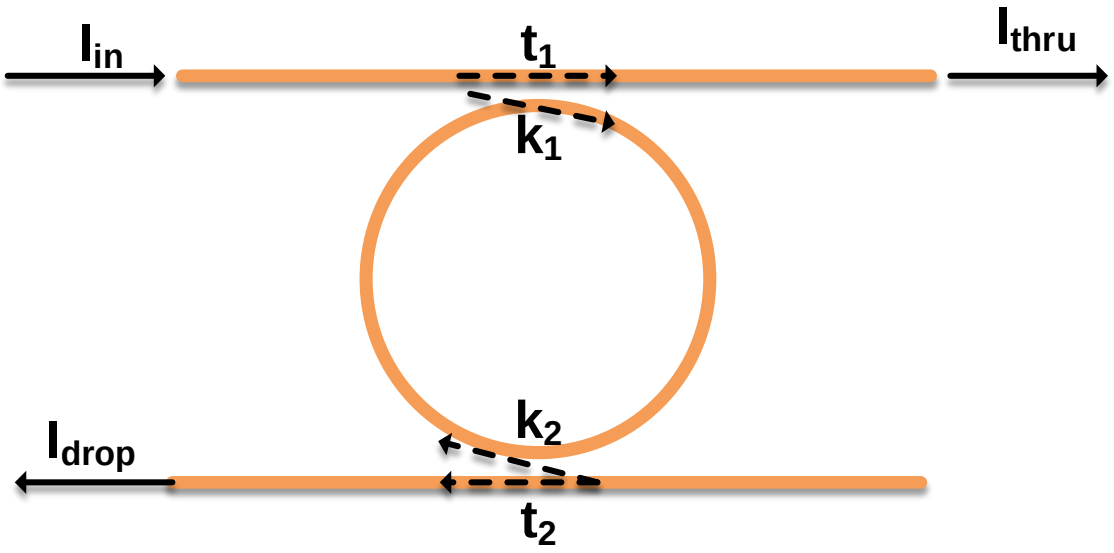

Figure 2.3 Structure diagram of a microring resonator with add-drop port

Assuming all couplers are lossless, the normalized transfer function of through-port and drop-port are given by Eq 2.6 and 2.7 [14]

$$H_{thru} = \frac{I_{thru}}{I_{in}} = \frac{\tau_2^2 * a^2 - 2\tau_1 * \tau_2 * a cos\varphi_{rt} + \tau_1^2}{1 - 2\tau_1 * \tau_2 * a cos\varphi_{rt} + \tau_1^2 * \tau_2^2 * a^2} \tag{2.6}$$

$$H_{drop} = \frac{I_{drop}}{I_{in}} = \frac{\kappa_1^2 * \kappa_2^2 * a}{1 - 2\tau_1 * \tau_2 * a cos\varphi_{rt} + \tau_1^2 * \tau_2^2 * a^2} \tag{2.7}$$

$$\left|\kappa_{1,2}\right|^2 + \left|\tau_{1,2}\right|^2 = 1 \tag{2.8}$$

Where φ_{rt} and a represent the round trip optical phase shifter and power attenuation which can be derived from Eq 2.9 and Eq 2.10, where $\kappa_{1,2}$ and $\tau_{1,2}$ are the coupling coefficient of cross coupling and through coupling, respectively.

$$\varphi_{rt} = \beta * L_{rt} \tag{2.9}$$

$$a = \sqrt{e^{-\alpha * L_{rt}}} \tag{2.10}$$

Where L_{rt} represents the round-trip length of the microring waveguide, β is the propagation constant and α is the waveguide loss of ring.

Table 2.1 presents the comparison between the MZM and MRM figure of merit. Typically, MZMs have a length of millimeter phase shifter, but ring modulator only need tens of micrometers, which microring have less insertion loss than MZM.

TABLE 2.1 Comparison of MZM and MRM

	MZM	Carrier depletion MRM	Carrier injection MRM
Footprint	Large	Small	Small
Extinction ratio	Small	Small	Large
Insertion loss	High	High	Low
Wavelength sensitivity	Low	High	High
Modulation bandwidth	High	High	Low

2.2 Silicon Photonics Integration

The silicon photonics integration of optical devices with electrical circuit remains to be a challenge. As several research and industrial group have developed several different technologies about integration process. Here, the integration strategies can be classified as monolithic integration which develop the optical devices and transistors both on the same chip and heterogeneous integration, with separate silicon photonic and electrical dies assembled in a multi-chip solution.

In the monolithic integration system, the platform simplifies the packaging through a single chip solution which consists of both optics and electronics design. It provides a compact device to circuit model and the simplified connection model between optical devices and circuit with on chip metal connection. The monolithic platform enables both high density interconnection to optical device and low interconnects parasitic. Also, this approach provides very high pack yield due to less complexity and high I/O density. However, as both optical device and CMOS circuit design are now on the same chip, the performance optimization cannot be independently achieved as the different process flow [23].

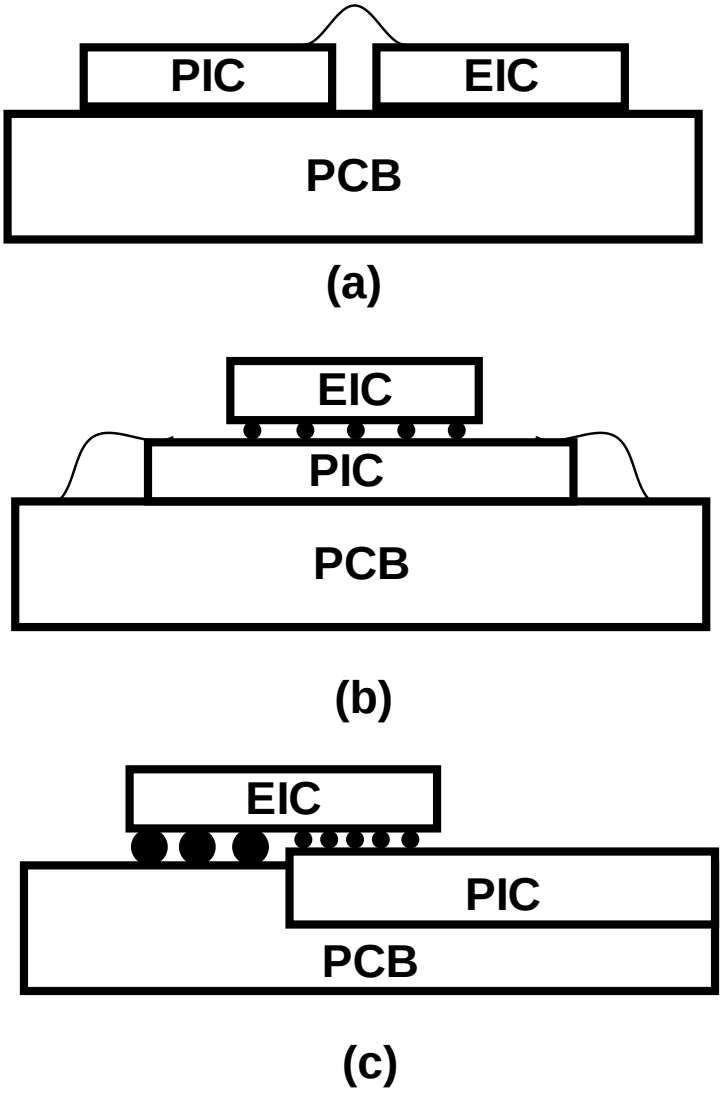

Figure 2.4 Integration technology for heterogeneous integration

In the heterogeneous integration system, the electrical wafer and silicon photonics wafer are fabricated in different processes. Since the silicon photonics are mainly focus on the SOI process, this separation makes the possibility for electrical using more advanced CMOS technology, such as FinFET CMOS. As shown in figure 2.4, server assemble technologies are illustrated. Die to die wire-bonding as figure 2.4(a)

shows, has good yield and less bonding complexity. However, large pad size and long bonding wire inductance will significant degrade the system performance. The interface number between electrical integrated circuit (EIC) and photonics integrated circuit (PIC) are also limited [24]. Die to die flip chip bonding are more populated nowadays due to high density IO and good reliability. However, even with micro-bump technique, the bonding interface size is over 50um, the parasitic capacitance will affect system power consumption and link budget. Extra routing for EIC need be done on PIC, both design complexity and signal integrity could be affected. And die size of PIC has to be much bigger than EIC in order to have enough space for PCB wire bonding and optical fiber coupler. In order to solve these two issues, a hybrid interposer design is developed in figure 2.4(c). A cavity PCB for PIC is design to compensate the PIC die thickness. The IO pads between EIC and PIC are using micro bump technique and the rest of pads of EIC can use C4 bump for higher current density. The optical fiber array for grating coupler can be located by the right side of PIC.

3. HYBRID-INTEGRATED Si PHOTONIC RECEIVER WITH MICRORING WAVELENGTH STABILIZATION *

An increasing number of mega data centers are emerging to support the ever-growing data processing and transmission demands from cloud computing, video streaming, and Internet of Things (IoT) applications. Given that the scale of these mega data centers translates into interconnect distances that can exceed 1km, efficient interconnect architectures are necessary to support per-channel data rates in excess of 20Gb/s. While multimode vertical-cavity surface-emitting laser (VCSEL)-based links have been the dominant optical interconnect technology for data centers [25-27], modal dispersion limits performance as distances and data rates climb. This motivates single-mode wavelength-division multiplexing (WDM) solutions that allow for increases in both transmission distances and bandwidth density [28].

Silicon photonics is an attractive technology for this due to the ability to integrate many photonic circuits on a single die and also leverage the manufacturing infrastructure of CMOS technologies [29]. Optical interconnect components have been realized in monolithic platforms which include both silicon photonic devices and CMOS circuitry [30-32] and with hybrid integration approaches where the silicon photonic die is connected to the CMOS driver or receiver chip via flip-chip bonding [33-35] or short

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wire bonds [36-37]. While monolithic integration allows for reduced interconnect parasitic and simplified packaging and testing, the optical elements can consume significant active layer area and the performance of the optical devices is potentially limited by the CMOS device processing. In contrast, implementing optical interconnects with a hybrid integration approach allows for independent optimization of the photonic device performance and decouples the cost of the electronic and photonic process development.

As shown in the hybrid-integrated optical link of Figure 3.1, silicon photonic microring resonator devices have the potential to enable low-area and energy efficient WDM optical interconnects. Due to their high-Q response, transmit-side ring modulators can independently modulate specific wavelengths on a common bus waveguide and receive-side ring drop filters can realize compact wavelength de-multiplexing by routing a desired wavelength to a specific receiver channel [30,31,33-35]. This inherent WDM functionality offered by the silicon photonic microring resonator modulators and drop filters offers significant photonic integrated circuit area savings, as it obviates the requirement of high-area arrayed waveguide grating multiplexers [29,38]. Further improvements in area and data rate are possible with the ability to integrate low-capacitance waveguide photodetectors (PDs) with lengths near 10μm directly at the end of the drop waveguides for optical-electrical conversion [30, 35, 39].

Optical receiver performance is critical because it sets the maximum link budget and the required laser power, and there are several challenges which must be addressed in a multi-channel microring WDM system. One is an efficient transceiver clocking

architecture. While CMOS optical front-ends have been previously developed that support data rates in excess of 20Gb/s, these designs often do not offer the retiming and deserialization functions required to form a complete link [30, 34, 35, 40]. Another challenge is achieving the required sensitivity in the presence of hybrid-integration interconnect parasitic variations. Finally, wavelength stabilization control is necessary to compensate for the fabrication tolerances and thermal sensitivity of microring drop filters.

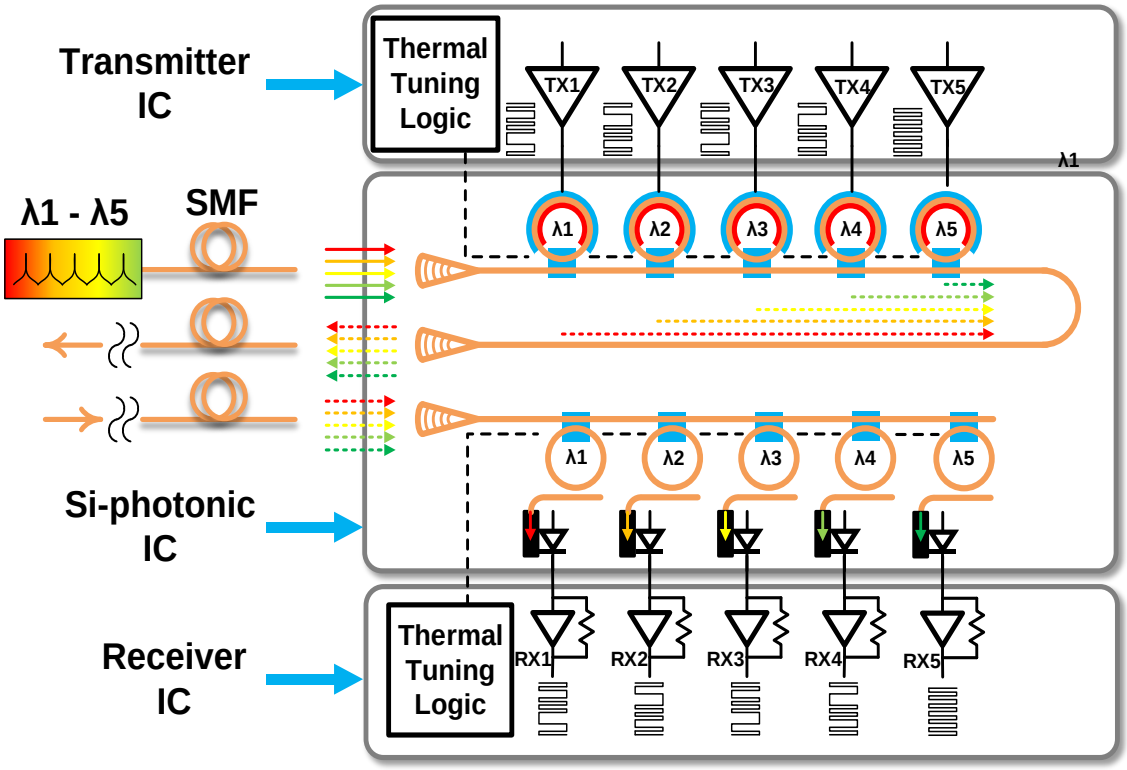


Figure 3.1. Hybrid-integrated WDM Si-photonic microring-based link block diagram

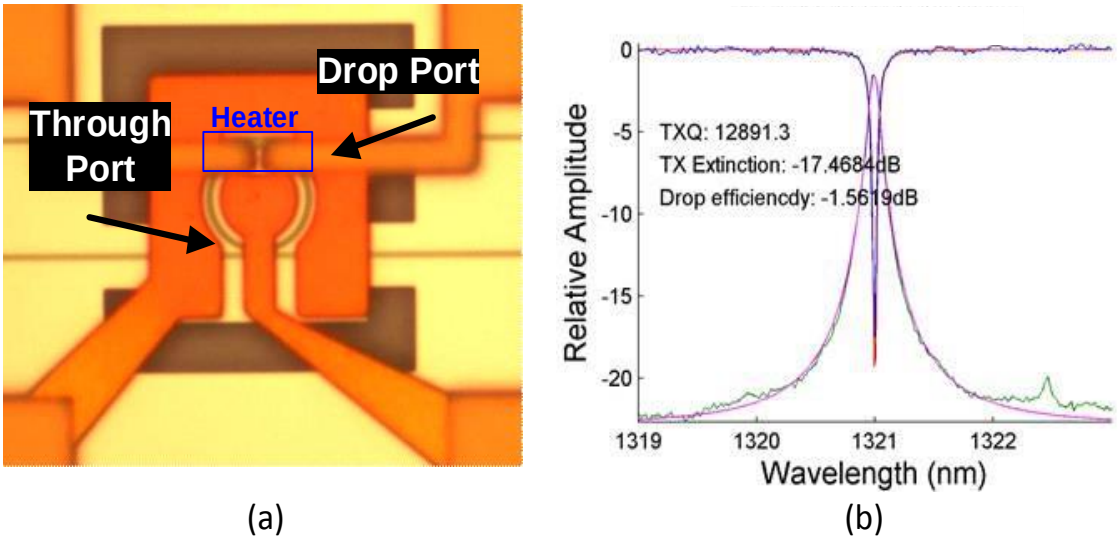
This paper presents a multi-channel 25Gb/s silicon photonic microring-based receiver operating in the 1310nm wavelength range which addresses these challenges

[39, 41]. The receiver achieves low-complexity clocking with a source-synchronous architecture with LC injection-locked oscillator (ILO) jitter filtering. Sensitivity is improved with a large input-stage feedback resistor transimpedance amplifier (TIA) cascaded with an adaptively-tuned continuous-time linear equalizer (CTLE) that accounts for variations in interconnect parasitics. In order to stabilize the microring drop filter resonance wavelength, a peak-detector-based thermal tuning loop is implemented which has minimal impact on receiver sensitivity.

3.1 Silicon Photonic Devices

The key silicon photonic devices in a microring-based WDM receiver are the drop filter which selects a specific wavelength from the common bus waveguide and the waveguide photodetector which performs optical-electrical conversion. This section provides key details on these silicon photonic devices [39, 41, 42].

3.2.1 Microring Drop Filter



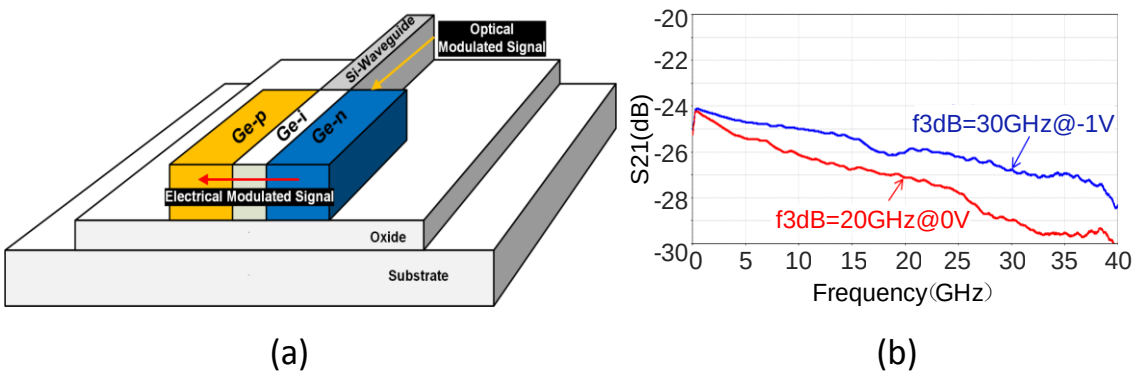
(a) (b)

Figure. 3.2 Microring drop filter: (a) Micrograph, (b) measured optical spectrum.

Figure 3.2(a) shows a microring resonator device which consists of a bottom "through" waveguide that couples a portion of the incoming light into the ring waveguide which then couples light into the top "drop" waveguide. The majority of the light is coupled out of the through waveguide and into the drop waveguide at the device's resonance wavelength. As shown in Figure 3.2(b), this results in a high-Q notch and bandpass response at the through- and drop-ports, respectively. The 5μm radius microring drop filters used in this work have greater than 10,000 quality factor, drop-port loss less than 1.6dB, and are designed for 160GHz channel spacing in the WDM system. In order to compensate for fabrication tolerances and the thermal sensitivity of the resonant wavelength, thermal tuning is implemented with a polysilicon resistor placed near the microring drop filter.

3.2.2 Waveguide Photodetector

The waveguide photodetector shown in Figure 3.3 is realized by forming a Germanium p-i-n junction at the end of the waveguide. The device displays near 10nA dark current in the absence of light. As the light propagates through the intrinsic region, it is absorbed with a responsivity of 0.45A/W. This somewhat low responsivity is due to the trade-off between absorption length and device capacitance. The waveguide photodetector is designed to have a low 40fF capacitance, including the high-speed signal pad, and a 10Ω contact resistance. This allows the device to achieve 20GHz and 30GHz bandwidth at 0V and -1V bias, respectively.



(a) (b)

Figure. 3.3 Waveguide Germanium p-i-n photodetector: (a) Cross-sectional view, (b) measured frequency response.

3.2 Source-Synchronous Receiver Circuits

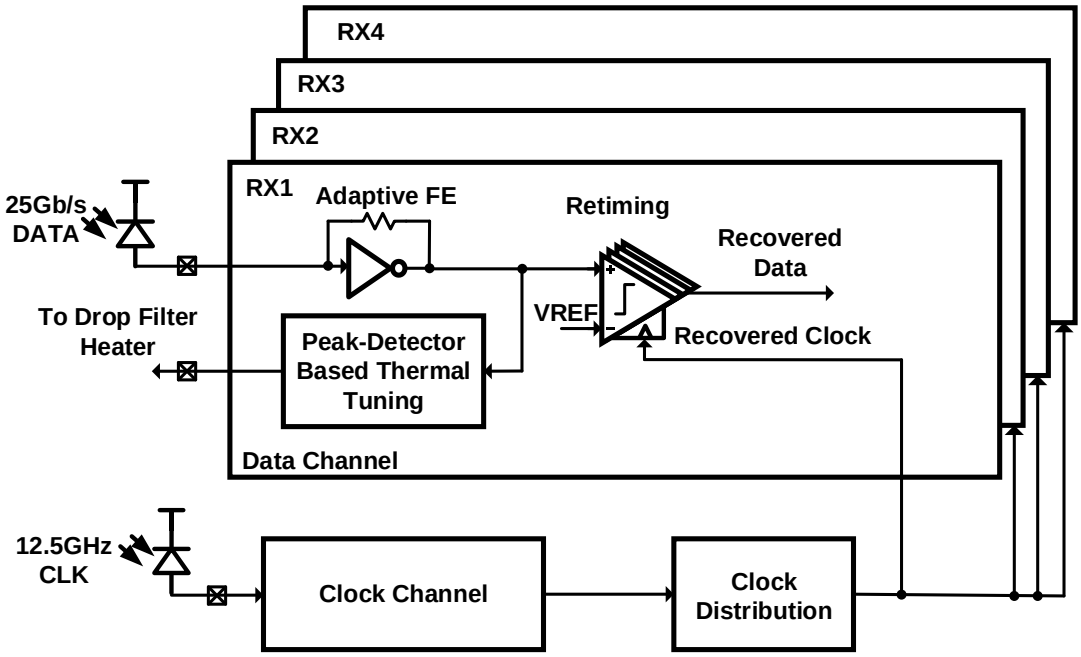


Figure 3.4. CMOS source-synchronous optical receiver chip block diagram.

Figure 3.4 shows a block diagram of the CMOS optical receiver chip, with one forwarded-clock receiver channel providing a synchronous 12.5GHz differential clock to

the four 25Gb/s data channels for reduced complexity per-channel de-skewing. As the received optical power for the clock signal can be degraded by channel losses, this clock channel includes an LC injection-locked oscillator that filters jitter induced by the clock receiver's input-referred noise. Each data channel operates at quarter-rate, with the differential 12.5GHz clock divided to produce four 6.25GHz quadrature clocks which pass through independently-controlled delay lines for de-skewing. The adaptive optical front-end consists of a large input-stage feedback resistor TIA, which improves the input-referred noise, and a subsequent adaptively-tuned CTLE which allows sufficient overall bandwidth for 25Gb/s operation. A peak detector monitors the TIA output level to provide information to a tuning finite state machine (FSM) that controls a thermal digital-to-analog converter (DAC) to stabilize each channel's drop filter resonance wavelength independently.

3.2.1 LC-ILO-Based Clock Channel, Distribution, and De-Skew

Forwarded-clock systems offer the potential for correlated jitter tracking up to high-frequencies. However, a potential issue in optically interconnect systems is poor signal-to-noise ratio at the clock receiver input due to channel losses. Thus, a balance between jitter filtering, high-frequency jitter tolerance, and power consumption must be struck. Two common approaches to jitter filtering in forwarded-clock systems include utilizing a clean-up PLL [43] or an injection-locked oscillator [36, 44], which can be approximated as a simple first-order PLL. A standard second-order clean-up PLL has the advantage of straight-forward bandwidth control via programmable loop filter elements. However, achieving high jitter tracking bandwidth to improve jitter tolerance implies a

wide PLL bandwidth, which translates into more power in the high-speed phase detector and filter logic. For example, a recent clean-up PLL for an 8Gb/s forwarded-clock electrical I/O that was implemented in a 32nm SOI process consumes 20mW [43]. Utilizing an injection-locked oscillator offers a low-complexity approach to jitter filtering, while also allowing for bandwidth programmability via adjustment of the injection strength and/or the oscillator's free-running frequency.

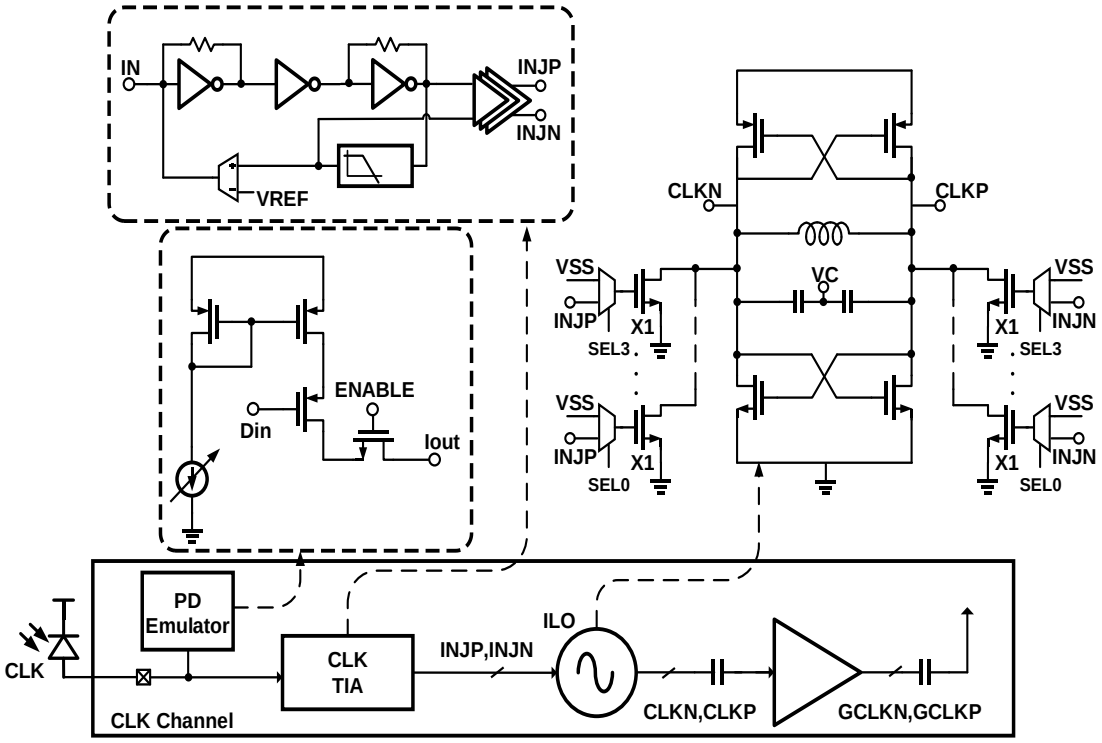
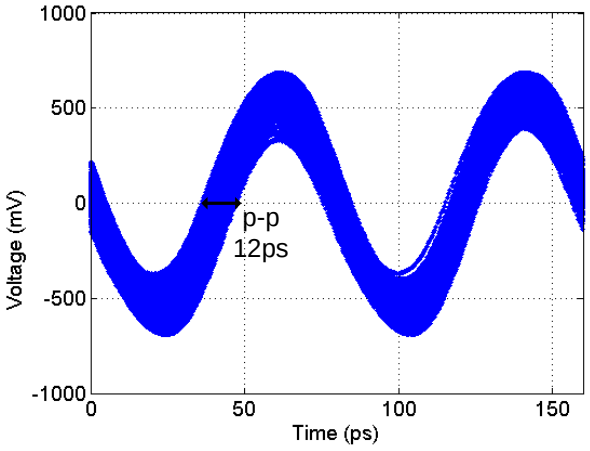


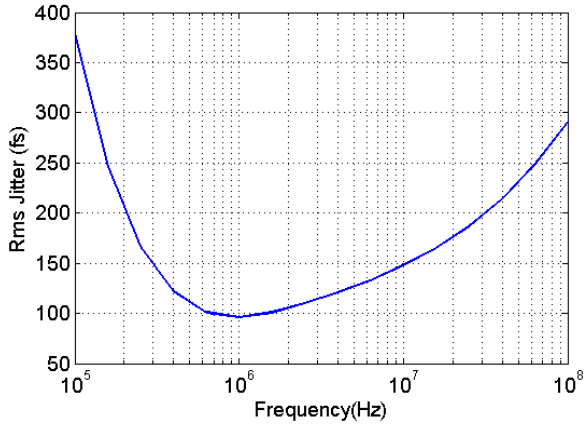
Figure 3.5 Clock channel block diagram.

While previously an optically-forwarded clock receiver was demonstrated at 8Gb/s with an injection-locked ring oscillator [36], at data rates in excess of 20Gb/s the wideband clock receiver input-referred noise can induce unacceptable output jitter that is not sufficiently filtered with a wide-bandwidth ring oscillator. This design utilizes a

12.5GHz LC injection-locked oscillator which allows for improved jitter filtering, while maintaining correlated jitter tracking with the data channels. As shown in Figure 3.5, the forwarded optical clock signal is amplified by an inverter-based TIA front-end and subsequent CML buffer stages before being injected into the LC oscillator. Also at the input to the clock channel is a photodetector emulator current source [36], which allows emulation of an optical clock with an electrical input signal. The LC-oscillator achieves a free-running frequency tuning range of 11.3GHz-13.3GHz via varactor control, has 4-bit thermal code injection-strength control for bandwidth adjustment, and achieves a 100MHz simulated peak jitter transfer bandwidth. The impact of the LC-oscillator jitter filtering is shown in the simulation results of Figure 3.6. Assuming a 12.5GHz -10dBm input clock, a jitter of 2psrms is observed at the wideband optical receiver output (Figure 3.6(a)). This noisy clock is then applied to the ILO, where Figure 3.6(b) shows that the output jitter decreases as the jitter tracking is reduced until reaching a minimum near 1MHz, after which the output jitter rises due to the VCO phase noise. Utilizing both the ILO injection strength and free-running frequency control, this jitter tracking bandwidth can be optimized to trade-off the jitter tolerance corner frequency and high frequency performance. Figure 3.6(c) shows that when the ILO bandwidth is set to 40MHz, the output jitter is reduced to 200fsrms. Supply-noise induced jitter is also reduced by utilizing a separate oscillator power supply. While not implemented in this prototype, a periodically activated control loop could set VC such that the ILO free-running frequency is equal to the injection clock [45] to reduce output phase errors and provide increased robustness to PVT variations.



(a)



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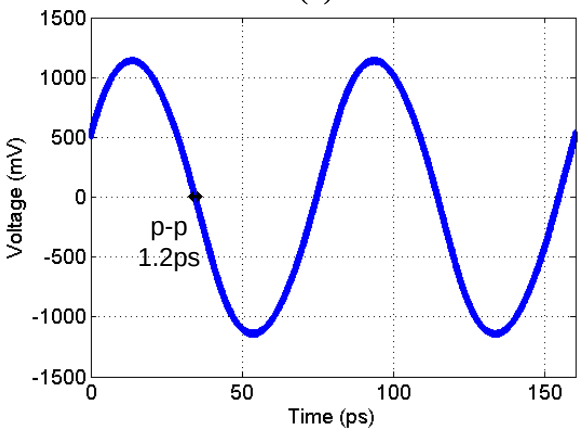


(c)

Figure 3.6 Simulated LC-ILO jitter filtering. (a) 12.5GHz forwarded-clock waveforms at LC-ILO input. (b) ILO output rms jitter versus ILO jitter tracking bandwidth. (c) 12.5GHz forwarded-clock waveforms at LC-ILO output with 40MHz bandwidth settings.

There are two reasonable approaches for global clock distribution to the quarter-rate data channels, either employing one global divider at the clock channel output and distributing four quarter-rate clocks globally or distributing a differential half-rate clock and utilizing per-channel dividers to locally generate the four-phase quarter-rate data clocks. While employing a global divider allows for the distribution of lower frequency clocks, both the per-phase skew due to mismatches in the global clock distribution and the correlated de-skew for optimal timing margin must be compensated for at each data channel. Utilizing per-channel injection-locked dividers (ILDs) driven by a differential half-rate clock compensates for both of these issues by providing some reduction in differential skew built up through the distribution network and also the ability to provide independent per-channel correlated de-skew through adjustment of the ILD free-running frequency.

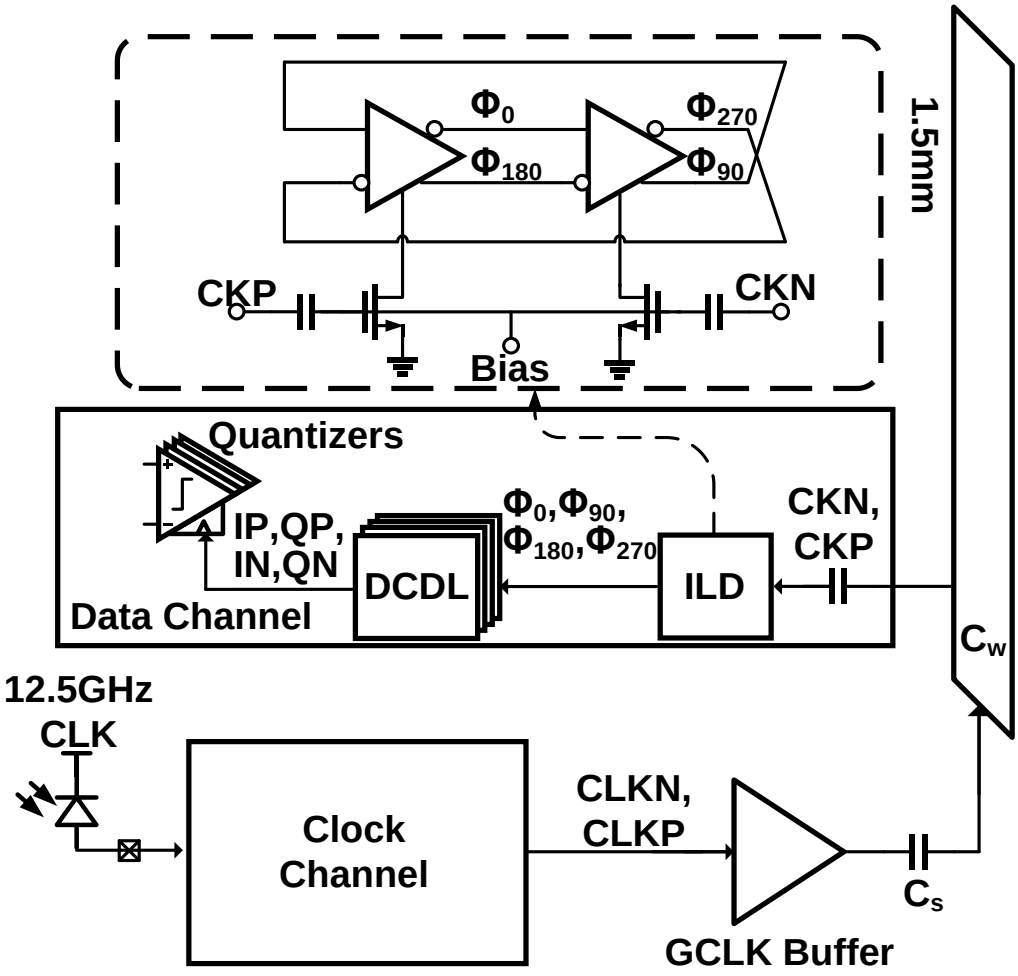


Figure 3.7 Global clock distribution and per-channel de-skew circuitry.

Figure 3.7 shows the global clock distribution and per-channel de-skew scheme. The LC-ILO differential outputs are AC-coupled to a global clock buffer which produces full CMOS-level signals to capacitively drive a 1.5mm differential wire. As discussed in [46], the distributed voltage swing is determined by the ratio of AC-coupling capacitance CS and the clock wire capacitance CW.

$$V_{swing} = \frac{C_s}{C_s + C_w} * V_{DD} \quad (3.1)$$

This ratio is set to distribute 600mVppd to every data channel. After distribution, this 12.5GHz differential clock is super-harmonically injected into the tail current sources of a ring-oscillator-based injection-locked divider (ILD) [47] to generate quadrature CMOS-level clocks for the quarter-rate data quantizers. The ILD delay cells, which are CMOS inverters that are current-starved by the shared nMOS tail current sources, produce near CMOS-level outputs. AC-coupling of the injection signal is employed in order to not impact the ILD DC biasing which controls the divider's free-running frequency. Tuning of this analog bias signal can introduce an offset in the free-running and injection frequencies, inducing a programmable phase shift on the four output phases. The ILD has a wide locking range and can provide near 40ps of correlated skew compensation. Per-phase digital-controlled delay lines (DCDLs) provide additional skew compensation to optimize the timing for the quarter-rate data samplers.

3.2.2 Data Channel Receiver

Figure 3.8 shows the quarter-rate data channel receiver that consists of a three inverter-stage TIA followed by a CTLE, which are both powered by an LDO for improved supply noise rejection, followed by the four main data slicers and an additional eye monitor slicer. Also at the input of each data channel is a photodetector emulator current source which allows emulation of either a 12.5GHz clock or a 2^7-1 PRBS input signal. Between the TIA front-end and CTLE, a low-pass filter extracts the TIA common-mode output which both serves as the reference input to the differential CTLE and drives a transconductance amplifier which subtracts the average photocurrent from

the input node. This RC filter bandwidth is set to be 170 kHz, which is estimated to support a 2^{17}-1PRBS pattern at 25 Gb/s. Both the main data and eye monitor slicers utilize 6-bit current-mode DACs to correct/adjust their offsets over a ±105mV range with a resolution less than 4mV. This design leverages a low-noise TIA design technique [40] to break the direct trade-off between sensitivity and bandwidth by utilizing a large input-stage feedback resistor (RF) in the input TIA and allowing the subsequent CTLE peaking to compensate for the increased input pole. The proposed design also introduces adaptive control to adjust the front-end peaking to accommodate variations in hybrid integration parasitic, with information from the programmable-offset eye monitor slicer utilized to tune the CTLE RC-degeneration.

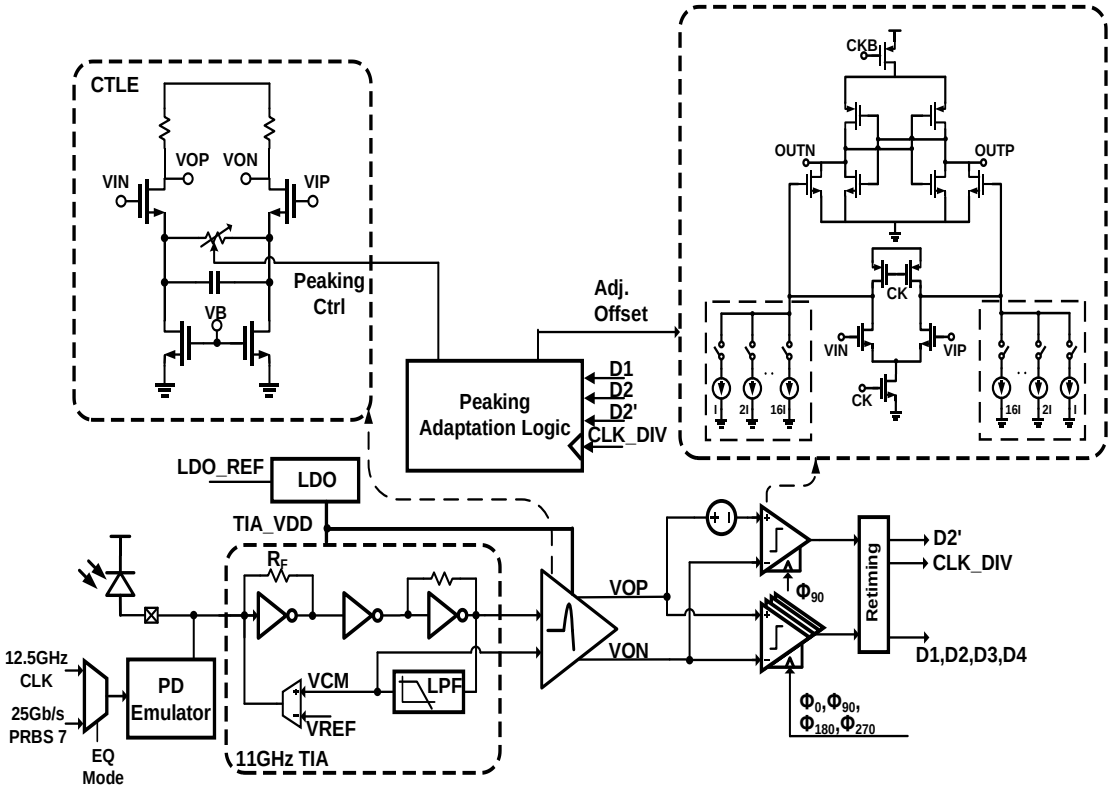


Figure 3.8. Quarter-rate data channel block diagram.

Two 17GHz front-end designs are compared to show how the input-referred noise is reduced, with the simulation results shown in Figure 3.9 assuming 0.5mm bond wire inductors separating 40fF on the silicon photonic chip side (photodetector and high-speed pad) and 50fF on the CMOS chip side (high-speed pad, routing, and PD emulators). While a low-RF input stage TIA followed by a simple wideband buffer can achieve 17GHz, the input-referred noise current spectral density is over 20pA/$\sqrt{\text{Hz}}$. The same overall bandwidth is achieved with a high-RF input stage TIA with 11GHz bandwidth followed by a CTLE that provides up to 6dB of peaking over 8 settings. However, now the larger feedback resistor has lower noise which is integrated over a smaller bandwidth, resulting in a reduction in input-referred noise current spectral density to between 10-15pA/$\sqrt{\text{Hz}}$. While there is some midband 1.4dB peaking in the high-RF input stage TIA due to the discrete CTLE settings, this results in a group delay variation less than 15ps.

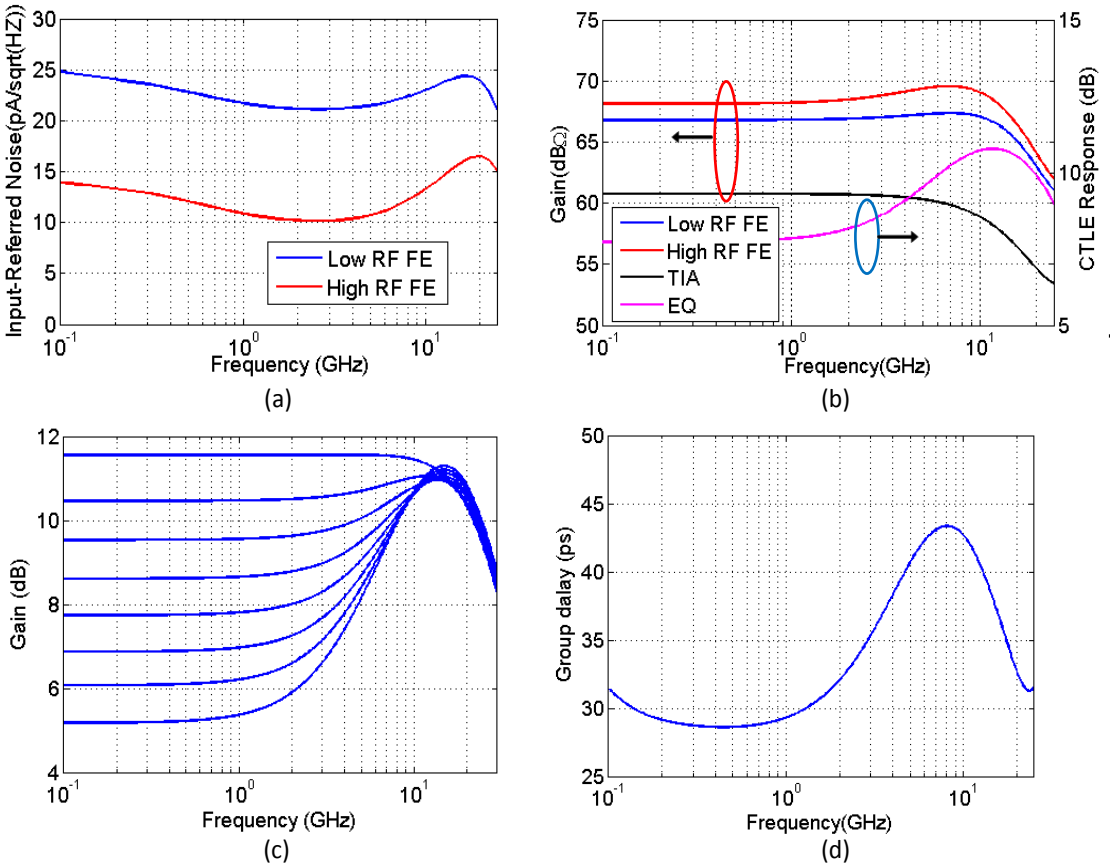


Figure 3.9. Simulated comparison of two 17GHz optical front-ends, one with a low-R_F input stage TIA and wideband buffer and the other with a high-R_F input stage TIA and CTLE. (a) Input-referred current noise density. (b) Frequency response. (c) CTLE frequency response with different peaking settings. (d) Group delay of high-R_F front-end.

Figure 3.10 illustrates the implemented two-step equalization adaptation procedure, where information from the additional eye monitor slicer (D2') with a programmable offset is utilized. The adaptation loop attempts to provide equal gain to both high and low frequency signals. In order to achieve this, the first step is to set the CTLE to minimum peaking and adjust the eye monitor offset to find the gain with a 1010… 12.5GHz calibration input produced with the photodetector emulator (Figure 3.

10(a)). Here the FSM logic is simplified by only considering D2’ when the data comparator on the same phase (D2) is high. The FSM utilizes a 10-bit counter clocked at the data rate divided by 256, which at 25Gb/s is approximately 100MHz, and the eye monitor offset converges in just over 10µs. After this, the state machine transitions to step two for peaking optimization with the 25Gb/s PRBS7 input data (Figure 3.10(b)). Now two consecutive data bits D1 and D2 are monitored, with again the FSM logic simplified by only acting when D2 is high. If D1 is low, this implies a “01” transition occurs. For this case, the peaking should be increased if D2’ is low, as this implies an undershoot during the transition, and decreased if D2’ is high, as this implies an overshoot. If D1 is high, this implies two consecutive ones. For this case, the peaking should be decreased if D2’ is low, as this implies that the steady-state value is too low, and increased if D2’ is high, as this implies too high a steady-state value. Note that the peaking settings are not incremented for each valid observation. Instead, after a certain amount of error statistics are captured, the peaking settings are then incremented by adjusting the digitally-controlled resistor in the CTLE degeneration network if the positive (Err1) or negative (Err2) signals exceed a nominal threshold of N=630. This prevents excessive dithering in the equalization convergence process. The CTLE settings are updated at just over a 20µs period with nominal data statistics, which allows the peaking optimization loop to converge in under 150µs for the worst-case situation with maximum peaking. Figure 3.11 shows how the deterministic jitter and eye height improves from the initial response with minimal CTLE peaking after the adaptive equalization loop converges.

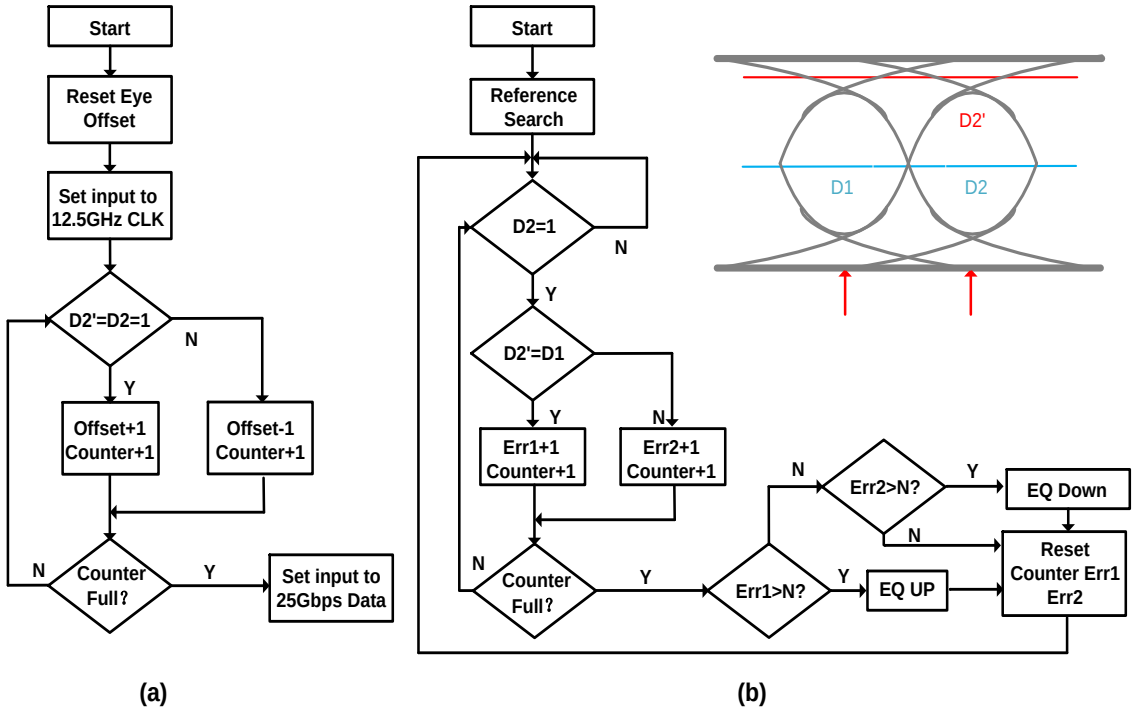


Figure 3.10 CTLE peaking adaptation algorithm. (a) Step 1: High-frequency gain search. (b) Step 2: Peaking optimization.

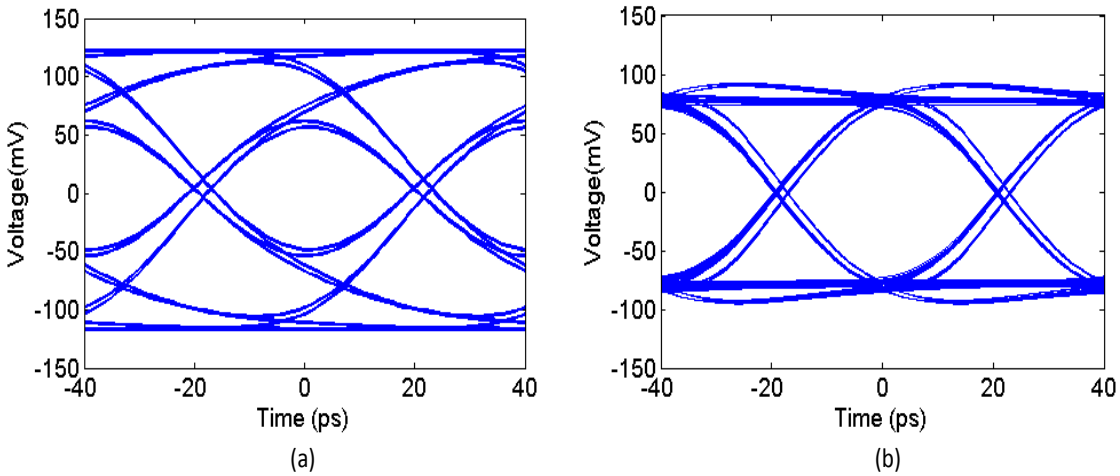


Figure 3.11 Simulated 25Gb/s TIA eye diagrams (a) before the adaptive equalization loop is enabled and (b) after the adaptive equalization loop converges.

3.2.3 Automatic Thermal-Based Wavelength Stabilization

Microring drop filters are susceptible to fabrication tolerances and thermal variations due to their high quality factors, necessitating wavelength stabilization control loops. While efficient average-power-based monitoring loops have been demonstrated for CMOS microring resonator transmitters [36, 37], the offset-correction feedback loop in the high-speed TIA prevents this from being a viable approach at the receiver. As shown in Figure 3.12, this design introduces a peak detector at the TIA output to monitor if the drop filter is locked to the input wavelength. The peak detector, consisting of an NMOS source follower and a 100fF hold capacitor, has its output sampled at 100MHz. This 100fF hold capacitor value allows for the peak value to settle sufficiently and be reset quickly during the 10ns period, while also limiting the peak ripple to within 3mV. The peak detector output is compared with a 6-bit reference DAC voltage to provide information to the tuning FSM which controls a 12-bit ΔΣ current DAC connected to the 1kΩ microring drop filter thermal resistor. Utilizing a 2.5V supply for the current DAC, which is designed with thick-oxide I/O transistors, allows for over 2V tuning range across the thermal resistor. As discussed in more detail in the experimental results of Section IV, this 2mA thermal DAC dynamic range provides 0.7nm wavelength shift, which translates into a stand-alone heater efficiency of 5.7mW/nm and a 1 LSB shift of 0.17pm. Given that the ring drop filters have quality factors over 12,000, this LSB value is much smaller than both the 110pm full-width half-maximum (FWHM) and 20pm 0.5dB bandwidth. The microring drop filters have a measured thermal sensitivity near 60pm/K or 10GHz/K at the operation wavelength, which is similar to other reported

silicon microring devices [31, 48]. Thus, compensation of up to 11K temperature variation of the microring drop filters is possible with the 0.7nm tuning range. This range could be extended by increasing the maximum DAC current and reducing the 1kΩ thermal resistor value in subsequent silicon photonic prototypes.

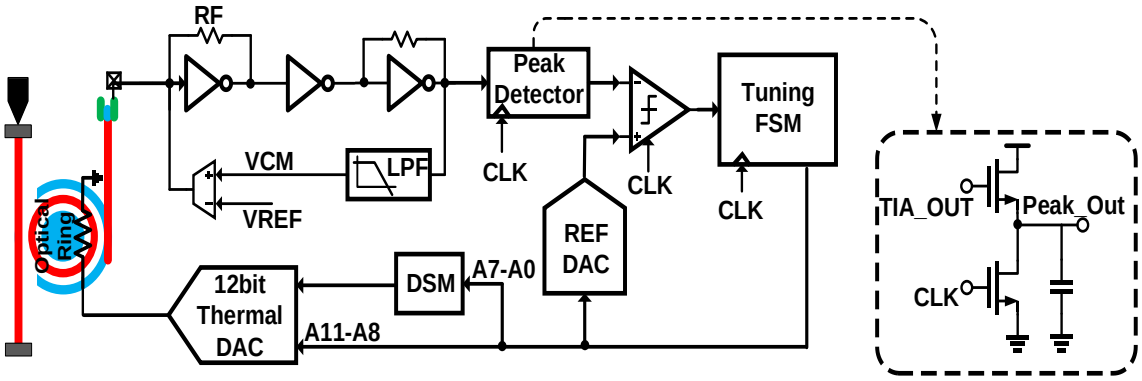


Figure 3.12. Microring drop filter tuning circuitry.

Figure 3.13 details the thermal-based wavelength stabilization algorithm for the control loops at each receiver channel. Before tuning it is assumed that the microring drop filter is not aligned with the laser wavelength, and thus the received optical power at the drop-port is very small (point 1). Similar to the control algorithm presented in [36], the peak detector output is compared with the reference DAC and the thermal DAC is then incremented to lock onto an initial conservative reference level (point 2). This reference DAC code is then saved as a successful lock point and subsequently adjusted in order to maximize the drop-port power. The control loop iterates to lock onto increasing reference DAC levels until the loop can no longer lock, or has "over-searched" (point 3). When this occurs, the FSM then steps back to the previous locked state (point 4). After this initial lock has been achieved, the loop can then track changes

in temperature and input optical wavelength by incrementing the thermal DAC through bang-bang negative feedback to maintain lock to the saved reference point [37]. Note that if the input power drops below the saved reference point, then the reference point will need to be recalibrated. While this feature is not in the current FSM, it could easily be added in subsequent prototypes.

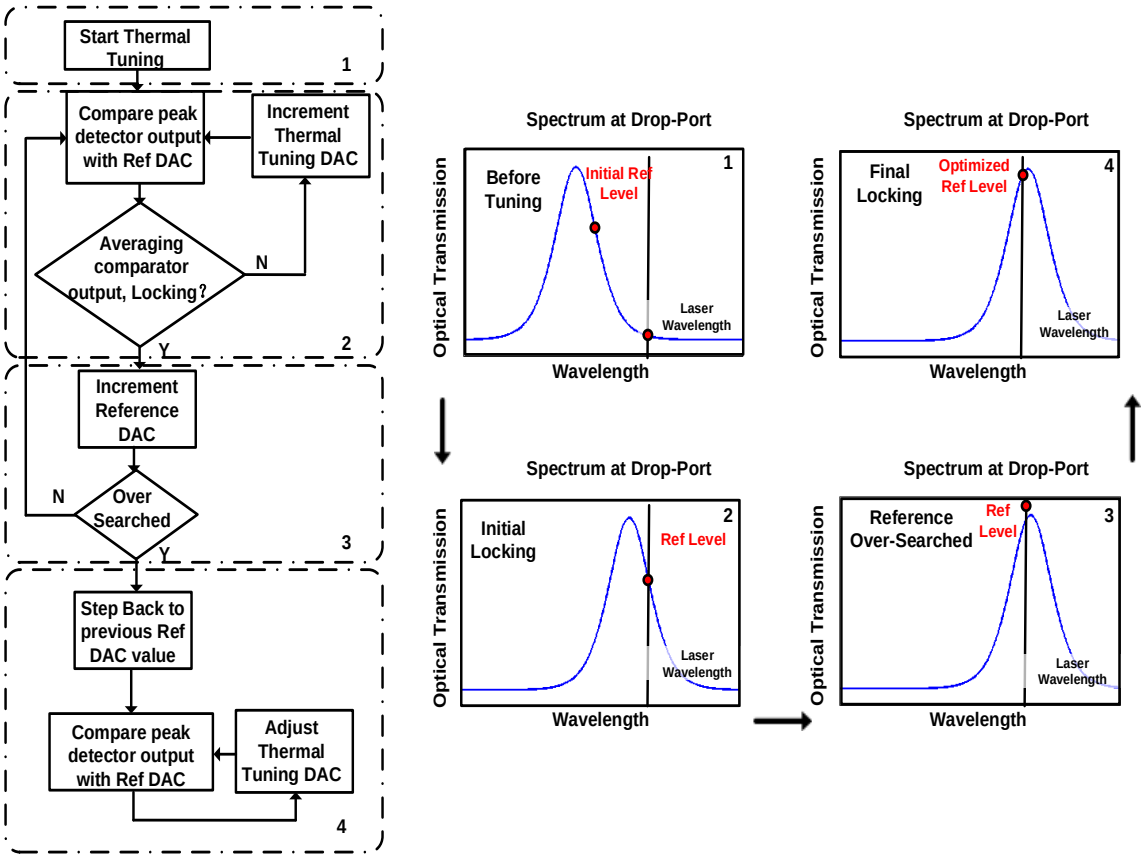


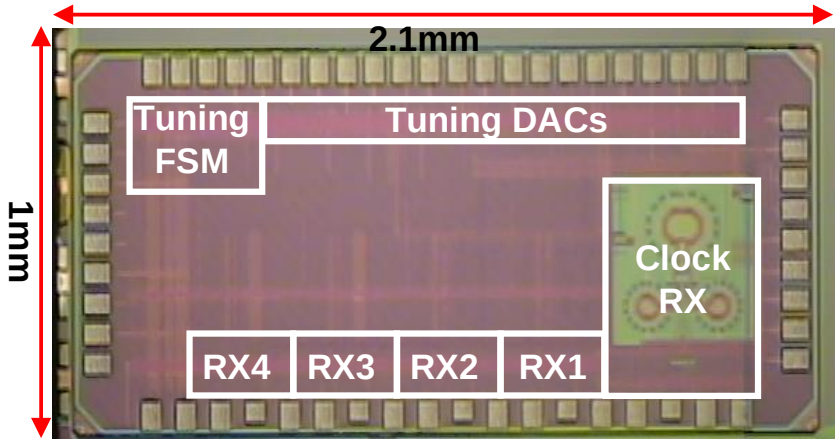
Figure 3.13 Microring drop filter thermal-based tuning algorithm with observed drop-port optical spectrum.

In a WDM system, sequential tuning of the rings would be performed starting from the ring closest to the input coupler. Instead of tuning a specific ring to an assigned wavelength, a ring shuffling technique allows tuning to the nearest available wavelength

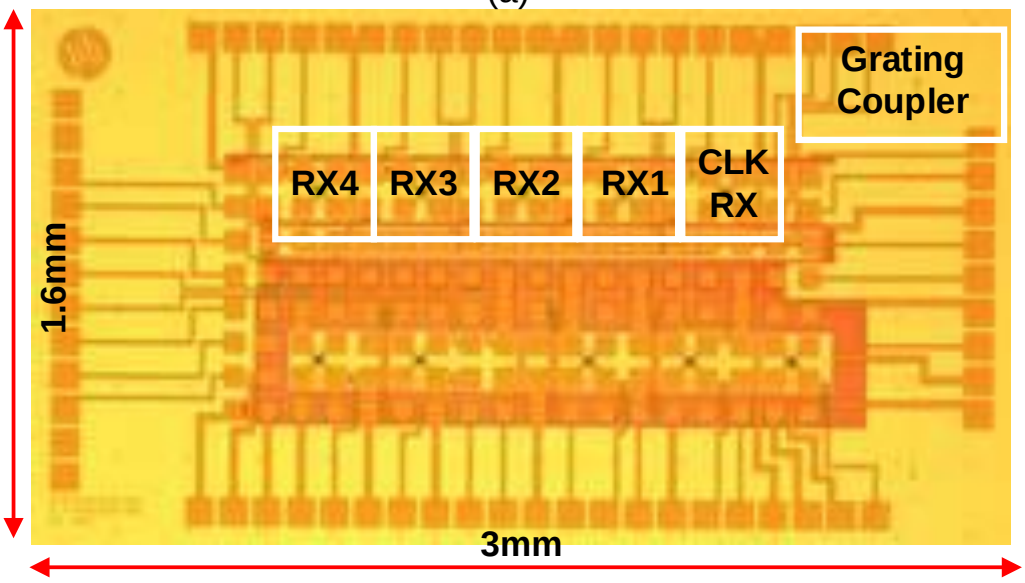
with minimal tuning power [48, 49]. After the first ring is tuned and drops this wavelength, the tuning procedure continues down the bus waveguide until all the rings are tuned. While there is the potential for channel disorder with this scheme, this can be resolved at the system level by utilizing specific training patterns on the individual WDM channels and employing a channel mux in digital back-end of the receiver channels [48].

3.3 Experimental Results

The multi-channel optical receiver prototype was fabricated in the TSMC GP 65nm CMOS process. Total chip area is 2.1mm^2 (Figure 3.14(a)), with each optical receiver data channel occupying 0.06mm2 and the clock channel occupying 0.35mm^2. The silicon photonics IC was fabricated in the CEA-LETI 130nm SOI process and contains five microring drop filters on one common bus waveguide, with each drop-port terminated with a waveguide PD (Figure 3.14(b)). Figure 3.15 shows the hybrid-integration chip-on-board approach utilized for the multi-channel receiver prototype, with the two chips adjacently placed and short wire bonds connecting the waveguide PD outputs to the receiver channel inputs. In order to minimize the bonding on the high-speed edges, the thermal tuning pads are placed on separate dies edges on both the CMOS and silicon photonic chips and bonded directly to the PCB for routing between the chips. Grating couplers on both ends of the common bus waveguide provides both coupling in of the modulated laser signal and the ability to monitor the through-port power.



(a)



(b)

Figure 3.14 Chip micrographs. (a) 65nm CMOS optical receiver IC. (b) 130nm SOI silicon photonic IC.

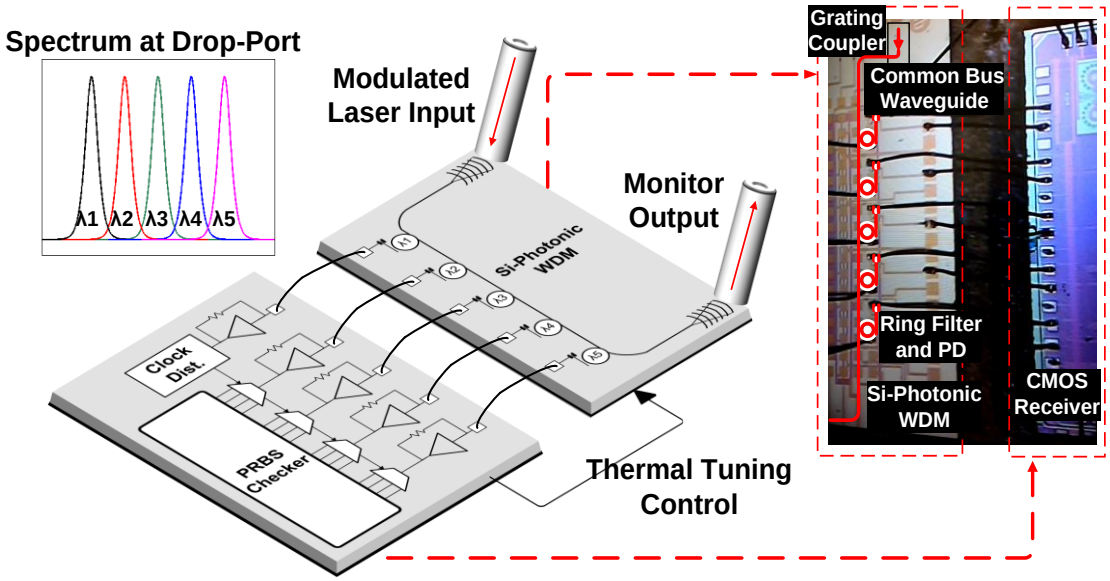


Figure 3.15 Hybrid integrated silicon photonic receiver prototype.

Figure 3.16 shows the receiver measurement setup. 25Gb/s PRBS data from a pattern generator is amplified to drive an MZM to produce the high-speed modulated optical signal which is coupled onto the silicon photonic IC. There a microring filter drops the modulated wavelength for O/E conversion by a waveguide photodetector and the CMOS front-end amplifies and deserializes the data. The pattern generator also generates the 12.5GHz clock which is input into the receiver's clock channel photodetector emulator in order to provide the sampling clock for the data channels. A Keysight 86100C oscilloscope is used to monitor the receiver outputs and an Anritsu MP1800A signal quality analyzer is used to verify system BER. An optical power meter is also placed at the end of the common bus waveguide to monitor the through-port power. Due to optical testing constraints, only one optical input signal is applied to the

receiver during testing. While this prevents characterization of optical crosstalk, on-die electrical crosstalk in the multi-channel receiver is present with all channels always being clocked and the photodetector emulators active on the other channels not receiving the optical signal.

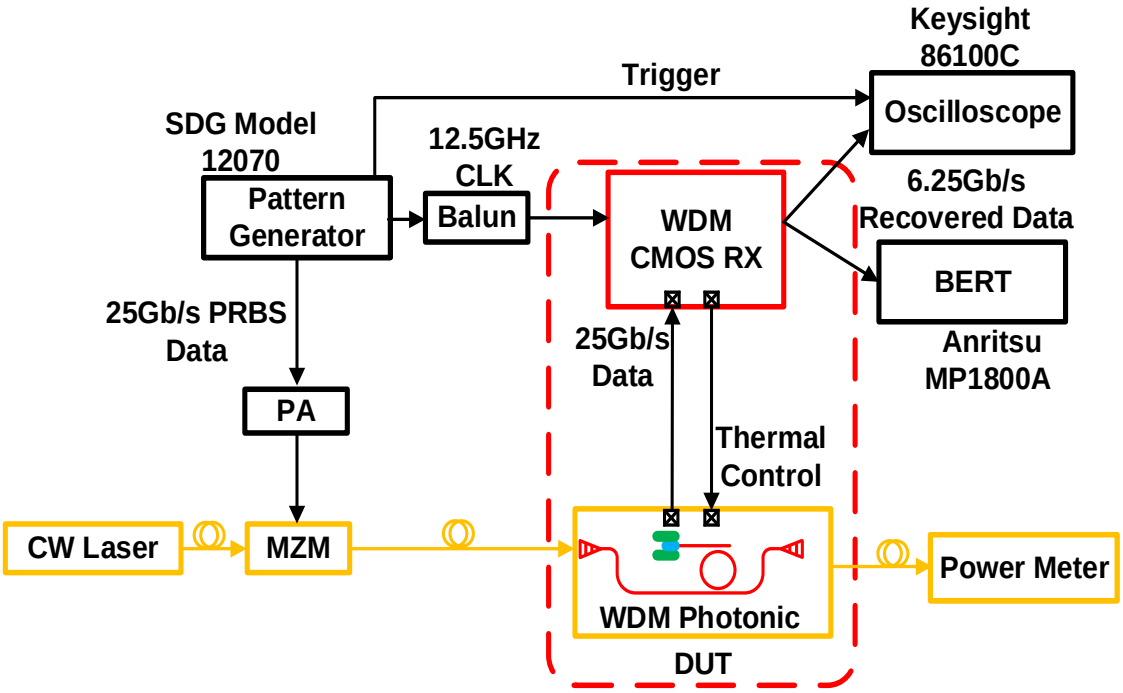
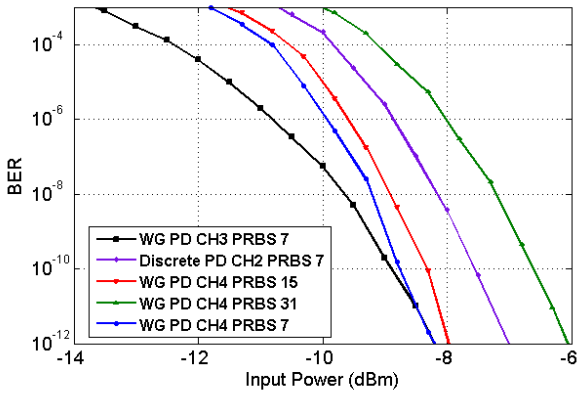


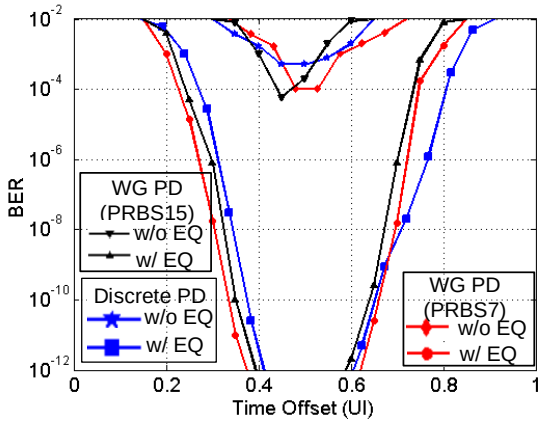
Figure 3.16 Silicon photonic receiver test setup.

In order to verify the utility of the adaptive equalization loop, receiver performance is verified with two test setups: 1) a discrete p-i-n photodetector with 70fF capacitance and 0.5A/W responsivity bonded only to channel 3 and 2) the silicon photonic IC with waveguide PDs with 40fF capacitance and 0.45A/W responsivity bonded to the CMOS IC. The receiver BER vs input optical power curves of Figure 3. 17(a) show that at a 25Gb/s data rate with PRBS7 inputs, the receiver achieves an OMA

sensitivity of -7 and -8.2dBm for the discrete p-i-n (channel 2) and waveguide PD (channels 3 and 4), respectively, at a BER=10^{-12}. Considering the photodetectors' responsivity, these OMA values convert to minimum modulated currents of 100µA and 68µA for the discrete p-i-n and waveguide PD, respectively. Measurements are also performed with PRBS15 and PRBS31 data. A minimal power penalty of only 0.2dB is observed with the PRBS15 input signal. However, due to the low frequency cut-off in the receiver data path and also some degradation from the external MZM modulator, a 2dB power penalty is present with the PRBS31 input signal. If a system is required to support longer run-length data patterns, such as PRBS31, the design can be easily modified with a larger time constant loop filter [26] to reduce this power penalty. As shown in the 25Gb/s BER bathtub curves of Figure 3.17(b), the optical receiver is unable to achieve an acceptable BER when the equalizer is set to its default minimal peaking value. When the adaptive equalizer loop is activated, the optical receiver achieves near 0.2UI timing margin at a BER=10^{-12} for both cases, with the waveguide PD achieving slightly larger timing margin due to its smaller capacitance. Figure 3.17(c) shows that the data channel can achieve a BER=10^{-12} for a minimum emulated forwarded-clock input OMA power of -10.3dBm. As with all the reported measurements, this is done with optical data signal coupled into data channel while the clock channel utilizes the photodetector emulator. The clock input power is then estimated from the photodetector emulator current setting and waveguide PD responsivity.



(a)



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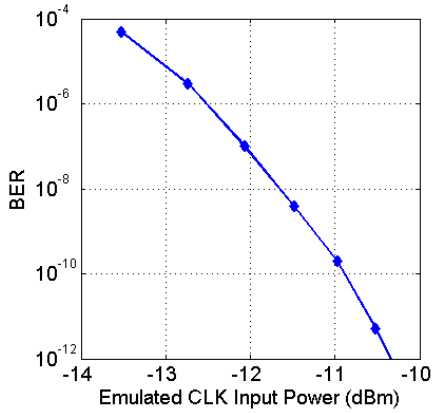


(c)

Figure 3.17 25Gb/s BER data. (a) OMA sensitivity curves. (b) Timing margin with and without CTLE peaking activated with -7dBm and -6.5dBm OMA input for the waveguide PD and discrete PD receivers, respectively. (c) Data channel BER versus emulated optical clock OMA power with -7dBm OMA input to a waveguide PD receiver.

The jitter tolerance of the source-synchronous receiver is tested by adding sinusoidal jitter to both the data and forwarded-clock signals. While the LC-ILO-based clock channel filters out high-frequency jitter induced by receiver input-referred noise, it allows the desired tracking of low-frequency jitter that is correlated with the transmitted data. As shown in Figure 3.18, this allows the receiver to tolerate a large amount of low-frequency jitter. Programmability of the jitter tracking bandwidth via the injection strength and the free-running oscillator frequency provides the flexibility to optimize for a higher jitter tolerance corner frequency or better timing margin. The system has a high frequency jitter tolerance of 0.15UI at 60MHz ILO settings, while dropping the bandwidth to 20MHz improves this to 0.2UI.

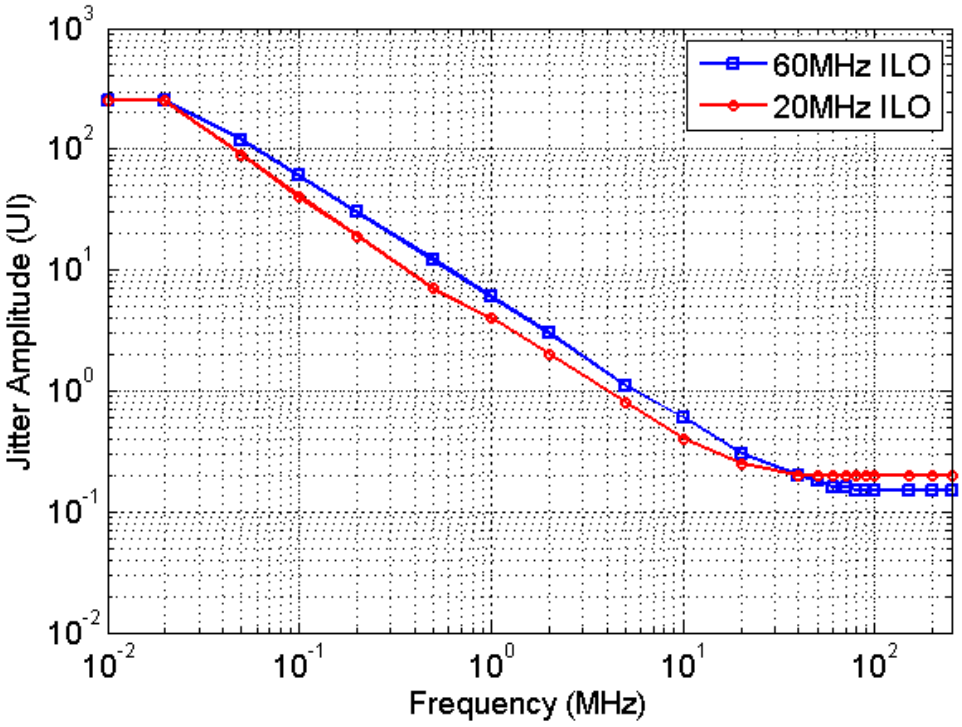


Figure 3.18 25Gb/s receiver sinusoidal-jitter tolerance with two ILO bandwidth settings.

As the drop-ports of the microring drop filters are terminated by the waveguide photodetectors, the through-port power spectrum is monitored for verification of the wavelength stabilization loop functionality. Figure 3.19(a) shows the microring wavelength shift for different thermal DAC current settings, with a 0.7nm tuning range achieved. As shown in Figure 3.19(b), enabling the wavelength stabilization loop allows for tuning of a microring drop filter to the desired 1336nm wavelength from its initial 1335.4nm value. The maximum tuning power is 5.1mW to cover the full 0.7nm range, which results in a tuning efficiency of 43µW/GHz.

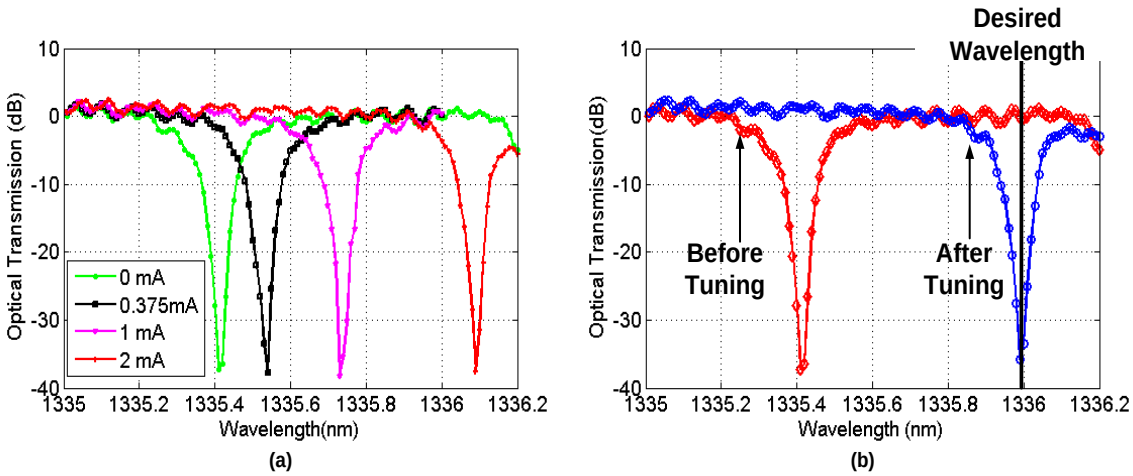


Figure 3.19 Drop filter resonance curves observed from the through-port. (a) Resonance shift versus thermal DAC current. (b) Tuning loop locking a drop filter to 1336nm.

Table 3.1 summarizes the key details of the silicon photonic and CMOS chips and provides a power breakdown. The majority of the data and clock channel circuitry employ a 1V supply, except for the LC-ILO which utilizes a dedicated 1.2V supply for improved noise performance. Each 25Gb/s data channel consumes 13.5mW. Amortizing

the 14mW clock channel and distribution power over the four data channels results in a receiver power efficiency of 0.68pJ/b. Table 3.2 compares this work with other 25Gbps optical receivers [30, 34, 40, 50, 51]. The hybrid-integration approach and presented design techniques allow the proposed 65nm design to achieve superior sensitivity and power consumption relative to the 130nm SOI monolithic-integrated design [30] and the 28nm CMOS hybrid-integrated design [34]. Relative to [40] [50] [51], while the relatively low PD responsivity resulted in degraded sensitivity, superior power consumption is achieved while also adding adaptive equalization, data retiming/ deserialization, and microring wavelength stabilization functionality.

TABLE 3.1 RECEIVER PERFORMANCE SUMMARY AND POWER BREAKDOWN

<table>
<tr><th colspan="2">Si-Photonic IC</th><th colspan="2">CMOS IC</th></tr>
<tr><td>Technology</td><td>CEA-LETI
130nm SOI</td><td>Technology</td><td>TSMC GP
65nm CMOS</td></tr>
<tr><td>Ring Radius</td><td>5µm</td><td>Data Rate</td><td>25Gbps</td></tr>
<tr><td>PD Responsivity</td><td>0.45A/W</td><td>Sensitivity</td><td>-8.0dBm</td></tr>
<tr><td>Integration Method</td><td colspan="3">Hybrid Wire Bonding</td></tr>
<tr><td rowspan="4">Power Consumption</td><td colspan="3">17mW Per Channel w/o Tuning Power</td></tr>
<tr><td>Data Channel</td><td colspan="2">13.5mW</td></tr>
<tr><td>Clock Channel</td><td colspan="2">14mW</td></tr>
<tr><td>Tuning Circuit</td><td colspan="2">5.1mW</td></tr>
</table>

TABLE 3.2 25Gb/s OPTICAL RECEIVER PERFORMANCE COMPARISON

	[30]	[34]	[40]	[50]	[51]	This Work
Technology	130nm SOI	28nm CMOS	65nm CMOS	0.13µm BiCMOS	65nm CMOS	65nm CMOS
Photodiode Type	Monolithic WG PD	Hybrid WG PD	Discrete PD	Discrete PD	Discrete PD	Hybrid WG PD
Input Capacitance	20fF	50fF	160fF	65fF	NA	90fF
Clock Structure	NA	NA	NA	NA	NA	Forward CLK + IL LCVCO
EQ	NA	NA	CTLE	NA	CTLE	CTLE
PRBS Pattern	NA	31	31	31	9	15
Input-Referred RMS Noise Current	NA	5.4µA	1.8µA	2.4µA	2.6 µA	1.8µA
Transimpedance Gain	59dBΩ	NA	83dBΩ	76.5dBΩ	76.8dBΩ	66dBΩ
Receiver Power/Channel	48mW	50mW	93mW	67.5mW	137.5mW	17mW
Sensitivity/ PD Responsivity	-6dBm /0.8A/W*	-8dBm /0.8A/W	-11.9dBm /0.91A/W	-12dBm /0.75A/W	-9.7dBm /0.8A/W	-8.0dBm /0.45A/W
Modulation Current	NA	127µA	59µA	47µA	86µA	72µA

* Average Power

3.4 Summary

This section has presented a 25Gb/s hybrid-integrated silicon photonic receiver design with 130nm SOI microring drop filters and waveguide photodetectors and 65nm CMOS source-synchronous receiver front-ends. An LC-ILO was implemented in the clock receiver to improve the recovered clock jitter, while in the data channels a large input-stage feedback resistor TIA is cascaded with an adaptively-tuned CTLE to break the direct trade-off between receiver sensitivity and bandwidth. Compensation of microring drop filter fabrication tolerances and temperature variations is achieved with per-channel thermal tuning loops that stabilize the drop filters' resonance wavelength. Overall, the proposed multi-channel silicon photonic microring-based receiver architecture has the potential to enable efficient implementation of single-mode WDM systems for data center applications.

4. A PAM4 56 GBPS SILICON PHOTONICS TRANSMITTER BASED ON MACH–ZEHNDER-MODULATOR WITH 2.5D INTEGRATION

Although the data rate of recent Si-Photonics MZM transmitter designs, including travelling-wave MZMs [52] and segmented MZMs [53], have excessed over 25Gbps, the interconnects speed requirement is still increasing due to more and more data in people daily life. The 4-level Pulse-Amplitude Modulation (PAM4) is the potential solution to increase the data rate by transmitting two bit data by using one symbol. Without increasing the baud-rate, PAM4 transmitter lower the requirement of bandwidth of the optical device of both E/O and O/E conversion. This section proposed a NRZ/PAM4 reconfigurable Si-photonic transmitter design which can achieve over 56Gbps data rate and 12pJ/bit power efficiency.

4.1 E/O Co-Design of Mach–Zehnder-Modulator

4.1.1 Travelling-wave MZM VS Segmented Electrode MZM

Two mainly design of MZM transmitter architectures are introduced and compared in this part. Travelling-wave structure is commonly used in the discrete InP or LiNbO3 MZM. Typically, the transmission line design is developed in this TW electrode, such as coplanar waveguide (CPW) as shown in figure 4.1(a). The far-end of the transmission line could be either differential or single-end terminated with a match resistor. The transmission design could extend the electrical bandwidth of electrode due to the low characteristic impedance of the transmission line. With carefully designed driver termination, the electrical signal integrity could be highly improved since the electrical reflection can be minimized.

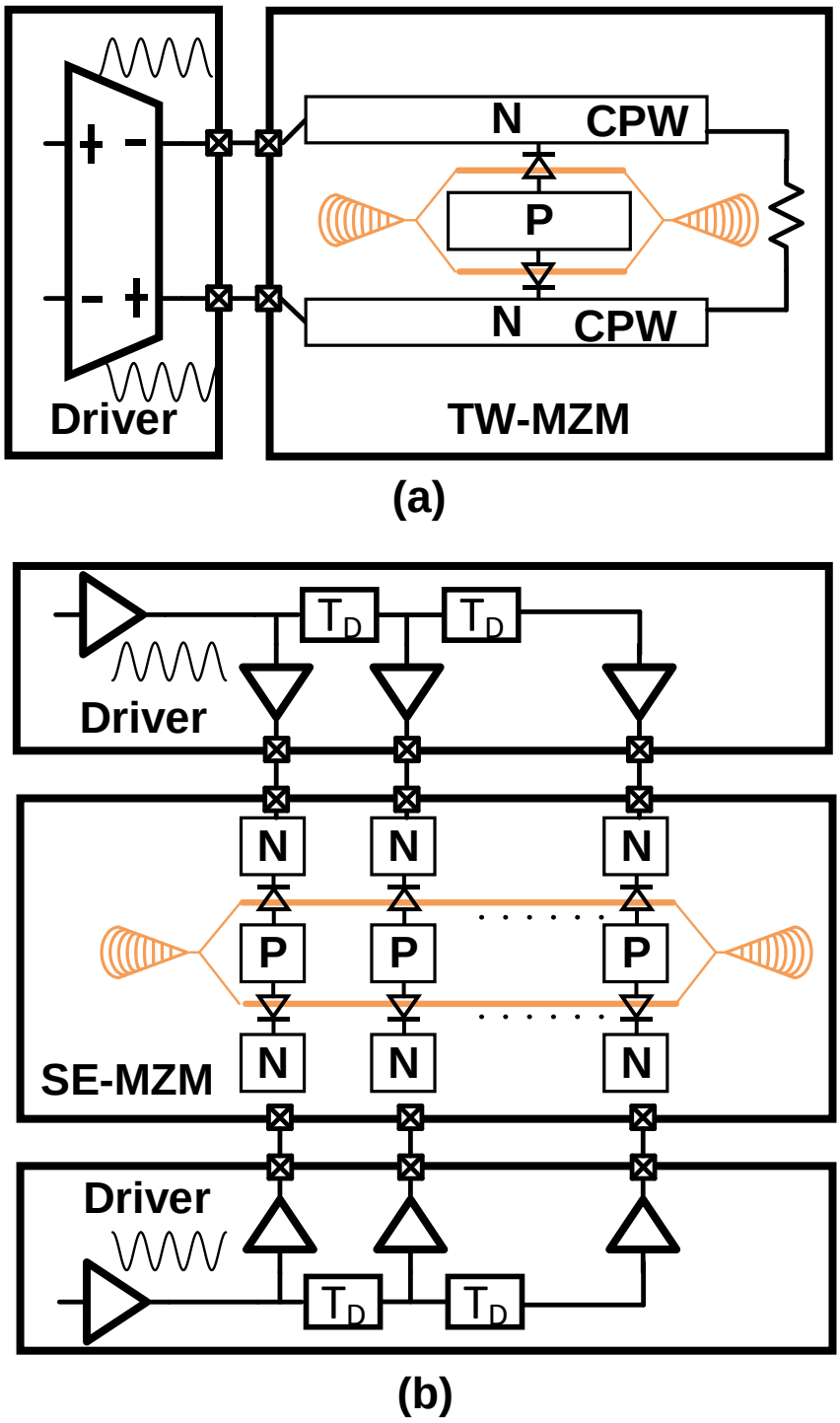


Figure 4.1 (a) TW MZM schematic (b) SE MZM schematic

Another advantage of TW MZM is the optical and electrical propagation velocity are matched naturally. However, this approach suffers several drawbacks, on chip transmission line introduce lossy channel due to large metal resistance. In order to achieve high extinction ration (ER) optical output, driver circuit need to provide high swing for the MZM. In commercial MZM design, over 5V driving swing are required because of lossy transmission line. The high voltage driver could be very challenge design in advanced CMOS technology. Meanwhile in order to achieve high bandwidth, the characteristic impedance and termination resistor are relative lower, as typical value 50ohm. In order to achieve high voltage swing over 50ohm load, huge modulation current is needed. Both power consumption and layout parasitic could be the major issue in circuitry design [54].

An alternative MZM structure which is named as segmented electrode MZM is shown in figure 4.1(b). Two long arms of MZM phase shifters are separated into several short phase shifters [55]. And each phase shifter has diode connection for modulation. Since each driver only need driver a short-length phase shifter which could be modeled as lumped capacitance, full swing push-pull transmitter can be implanted in order to achieve both high modulation speed and high optical extinction ration. Another advantage of SE-MZM is highly reconfigure in CMOS driver design. With different configuration setup, multi-level pulse-amplitude modulation can be achieved in optical domain. The major design challenge in the SE MZM is the electrical propagation velocity may not match with the optical propagation delay. Additional delay control circuit is required in driver design. The velocity match will be discussion in following

section. Another challenge in SE MZM design is the multiple pins integration. Since there is no impedance match between driver and the modulator, long bonding wire might introduce unwanted reflection and crosstalk. Meanwhile, multiple connection between the driver and the modulator increase the integration complexity compare with TW MZM.

Overall, TW MZM design is more rust in discrete MZM design due to less driver design complexity. As the rapid development in silicon photonics, the SE MZM can be benefit from advanced integration techniques such as monolithic and 3D integration and well development environment for E/O co-design.

4.1.2 Dual-differential, Dual-arm Push-pull Driving

As discussed in chapter 2, the MZM optical transfer function is determined by the phase shift of PN diode junction. In order to achieve enough phase-shift for certain extinction ratio, the electrical driver need to generate certain voltage swing with proper DC-biasing voltage. In discrete MZM design, the driver need provide over 5V single-end Vpp voltage swing, and those drivers are mainly fabricated in SiGe or other III-V technology. However, such single-ended drive is not compatible for CMOS-based drivers, due to the lower supply voltage VDD and breakdown stress [56].

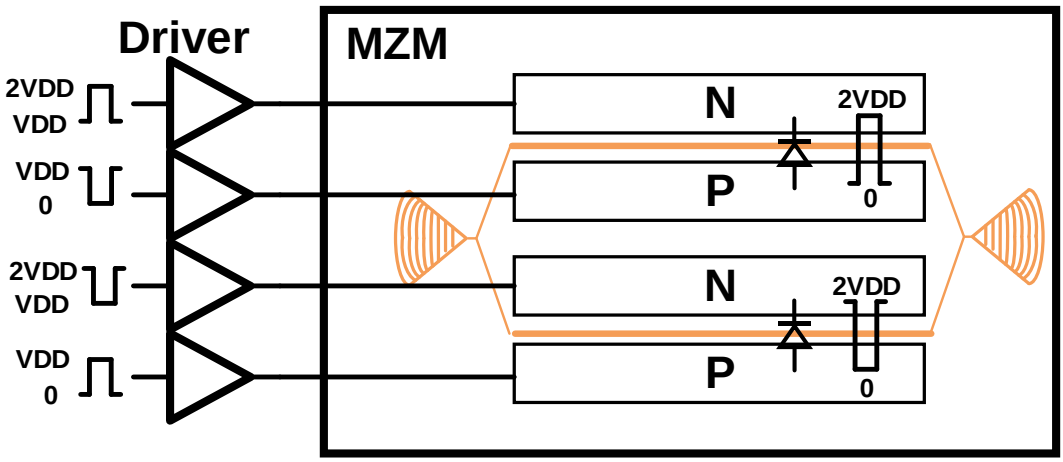


Figure 4.2 Dual-differential, dual-arm push-pull Driving

Figure 4.2 illustrates a Dual-differential drive, dual-arm push-pull driving method. Total 4 single end drivers, also can be considered as two differential drivers, which could drive both arms of the MZM simultaneously. To maintain the reverse bias of the diode, the CMOS driver circuit which drive the cathode of diode should operate in higher voltage domain, from VDD to 2VDD. In this driving scheme, the overall voltage swing over each arm diode is 2VDD, and the total Mach-Zehnder modulator could be affected by 4VDD due to two arm modulations. In 16nm Finfet CMOS design, the general power supply voltage is 0.9V. The proposed driver which implemented two power supply domains 0.9V and 1.8V, ideally can achieve 3.6V peak-peak swing for MZM optical transfer function calculation.

4.1.3 Advanced Modulation Implementation

There are two different approaches to generate multi-level PAM4 optical modulation with a MZM device. One approach is the electrical DAC design where a

level voltage/current DAC combines the least significant bit (LSB) and the most significant bit (MSB) and generates four different electrical modulation signals.

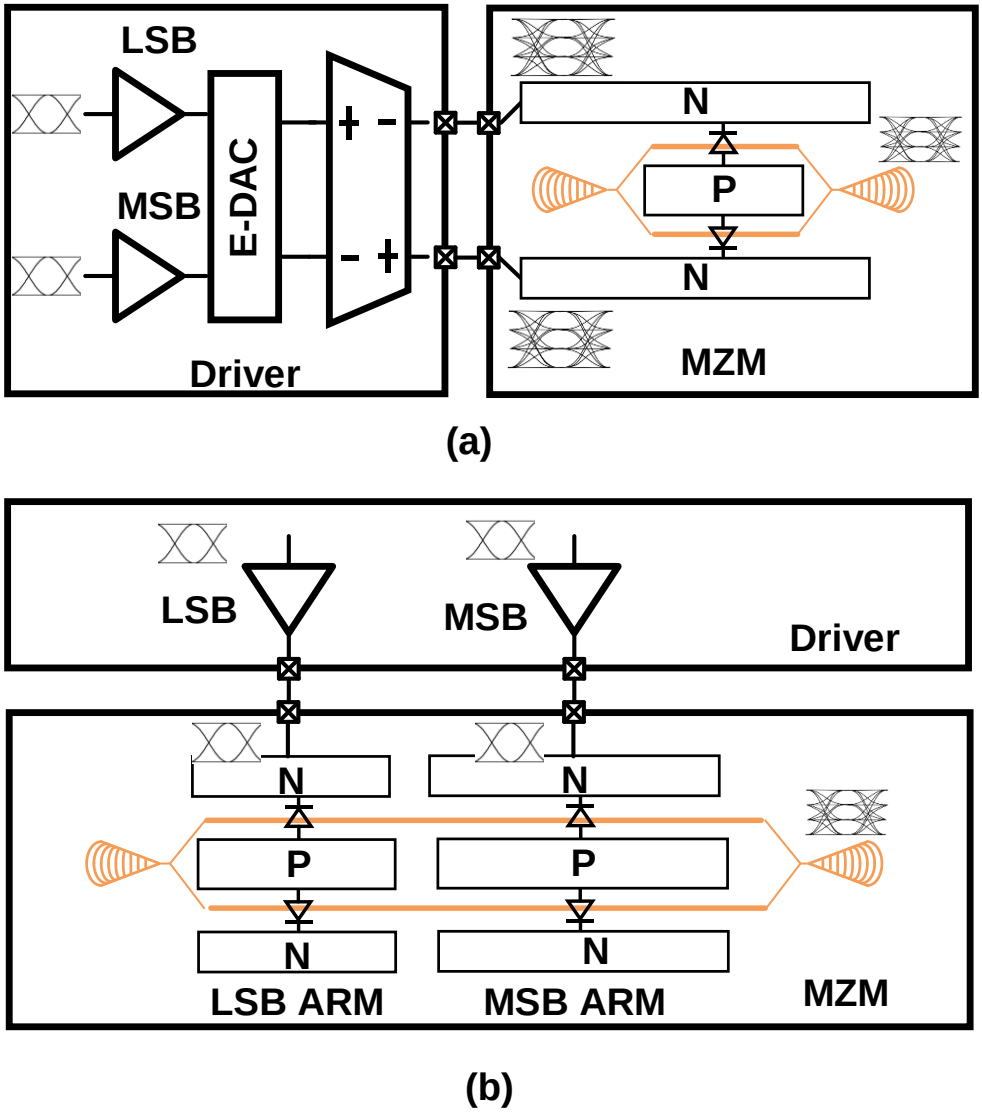


Figure 4.3 (a) Electrical DAC based PAM-4 transmitter (b) Optical DAC based PAM4 transmitter

As shown in figure 4.3 (a) The output driver directly drives the MZM device with electrical PAM4 signal in order to achieve optical PAM4 modulation [57]. This

approach which requires more complex CMOS driver design and higher bandwidth requirement of the driver circuit, are often used in travelling wave MZM design [52]. The other approach shown in figure 4.3 (b) is based on optical domain combination. In the MZM design, each arm has two phase shifters with different total length. Every phase shifter could be driven by 2 level NRZ driver without increase the circuit complexity. This approach which requirement more driver numbers and lower bandwidth requirement, can be used in both TW MZM [59] and segment MZM [58].

4.1.4 Velocity Mismatch

Microwave propagation delay must be matched to the optical propagation delay. Otherwise, the bandwidth of the optical link will be degraded, especially when the device is operating at higher data rate [60]. As mentioned in previous section, the precision delay cells are required for multiple segments lumped-element MZM device. This phenomenon is studied with electrical-optical (EO) behavioral simulation for a multi-segment lumped-element MZM device [61]. As shown in figure 4.4, the SE MZM design consists of 14 segments electrode where five segments are using as LSB phase shifter and 9 segments are using as MSB phase shifter, and p-i-n based low speed phase shifter is used as MZM phase calibration. The length of the waveguide can be tuned to meet the delay cell design requirement and the mismatch introduced by difference of the large and small waveguide turns will be compensated by the turns for routing the next segment.

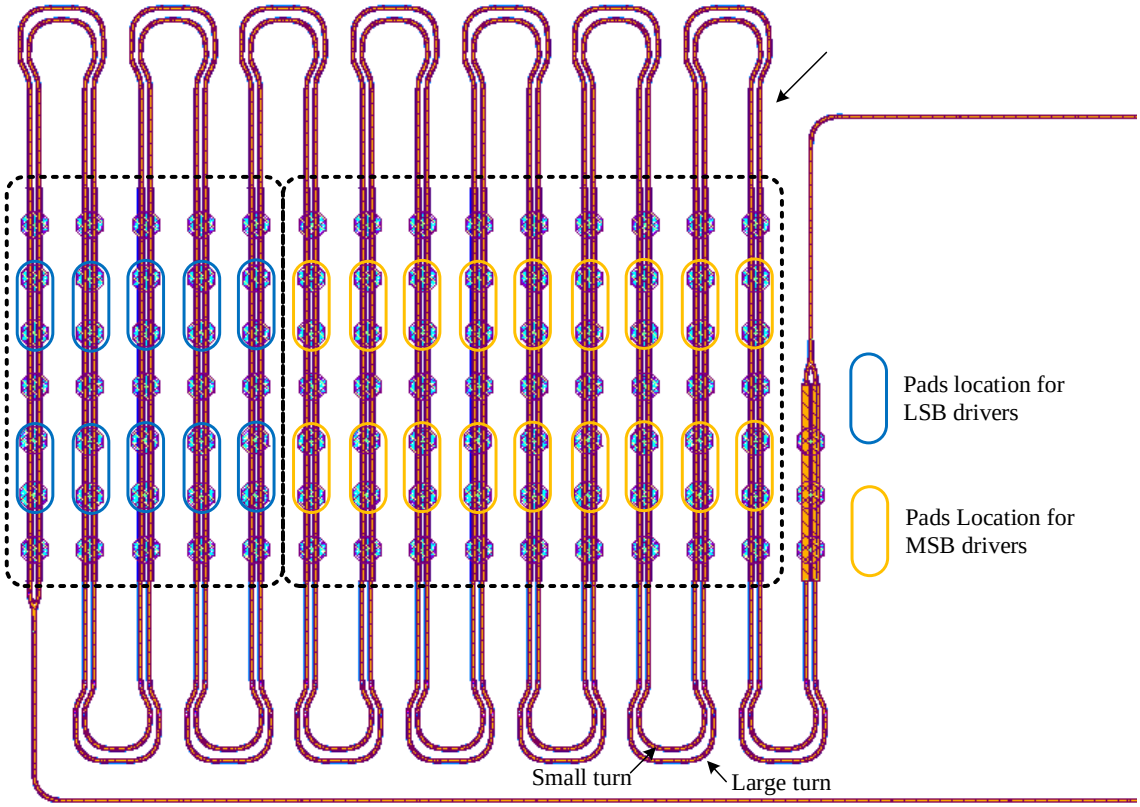


Figure 4.4 Layout diagram of the SE MZM

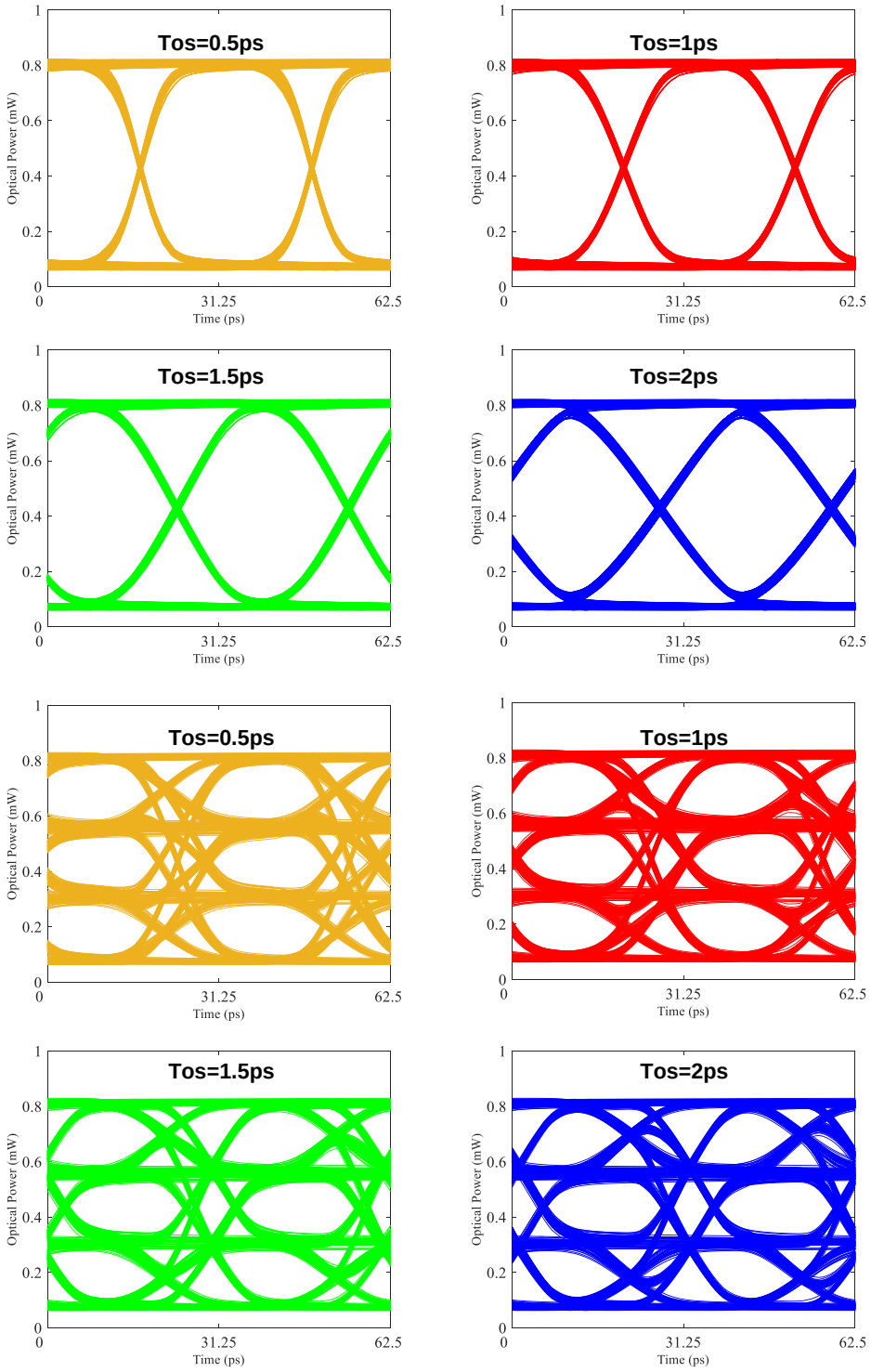


Figure 4.5 Velocity mismatch simulation of NRZ and PAM-4 signaling at 32GHZ symbol rate

Both NRZ and PAM4 working mode are simulated with every segment phase shifter design is driven by ideal push pull driver at 32Gbps data rate with certain delay. The NRZ and PAM-4 eye are plotted in figure 4.5. With different time offset (tos) of electrical delay and optical propagation delay varying from 0.2ps to 2ps per segments, the overall bandwidth degradation could be easily observed in the simulation result. In the NRZ simulation, the optical signal rising and falling time are significant increased from 0.5ps tos to 2ps tos. Meanwhile, in PAM4 simulation, large delay match causes skew for 3 eyes pattern and smaller eye width of each eye due to slow rising/falling edge.

4.2 Reconfigurable MZM Transmitter Architecture

Figure. 4.6 shows the block diagram of the NRZ/PAM4 reconfigurable transmitter. The silicon photonics chip design contains total 14 high speed phase shifter segments where 5 segments are modulated as LSB and 9 segments are modulated as MSB and a low speed phase shifter for MZI phase calibration. Each segments phase shifter is dual-differential, dual arm push-pull driven by a driver which input delay can be carefully tuned by a delay cell to match the optical propagation delay. The push-pull driver design implemented an output enable function circuit, the effective length of MZM modulator and modulation schemes can be configured. The clocking circuit provides induvial clock signals for LSB serializer and MSB serializer in order to match the optical propagation delay.

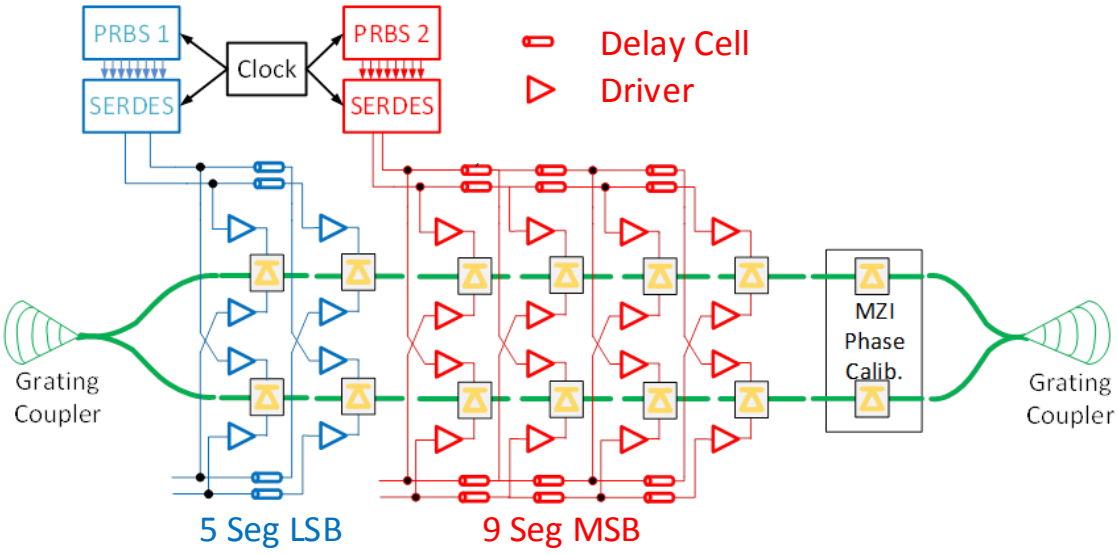


Figure 4.6 Proposed NRZ/PAM4 reconfigurable transmitter architecture

The transmitter could be configured as NRZ modulation by completely power down either all 5 LSB segments or 9 MSB segments. The NRZ eye diagram results are shown in Figure 4.7. With 10 dBm (10 mW) laser power coupled into the PIC and the MZM is biased at quadrature point, the MZM transmitter achieves about 2.94 dB and 5.55 dB extinction ratio, respectively.

In the PAM4 modulation mode, the two PRBS generator output two un uncorrelated data pattern to LSB and MSB channel. The simulated PAM4 eye diagrams which use different segments configurations are shown in figure 4.8. When all the segments are enable, the optical output can achieve 9.38dB extinction ratio and 0.96 ratio of level mismatch (RLM). The performance of MZM ER and RLM could be degradation when fewer segments are enabled for low power consumption purpose.

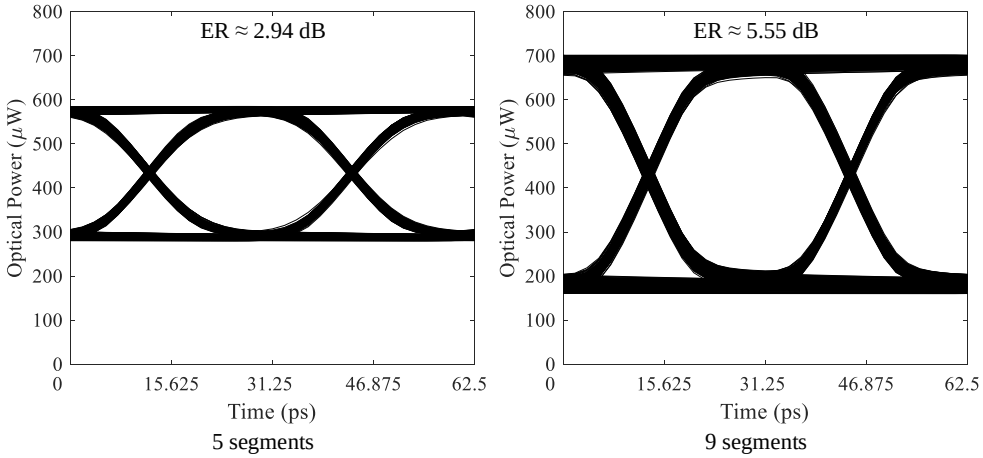


Figure 4.7 NRZ eye diagrams at 32Gbps data rate with 5 LSB segments and 9 MSB segments respectively

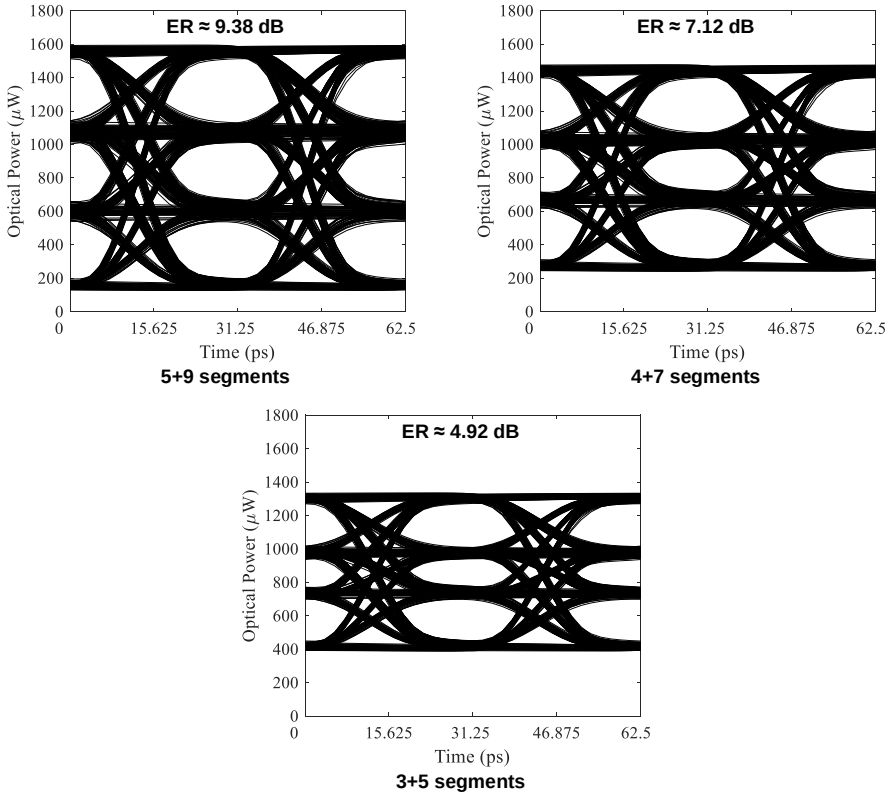


Figure 4.8 PAM4 eye diagrams at 32GHz baud rate with different segment configuration

Figure 4.9 presents the schematic of CMOS transmitter design. MSB and LSB data path serialize 32 parallel data to one high speed 20Gbps data, the optical propagation delay of the LSB and MSB could be calibrated by phase interpolator design. Both LSB and MSB data path are connected to a digital control delay line to generated delay matched electrical signal for final driver. The final push-pull driver design can generate 0 to 2VDD voltage swing for higher transmitter ER.

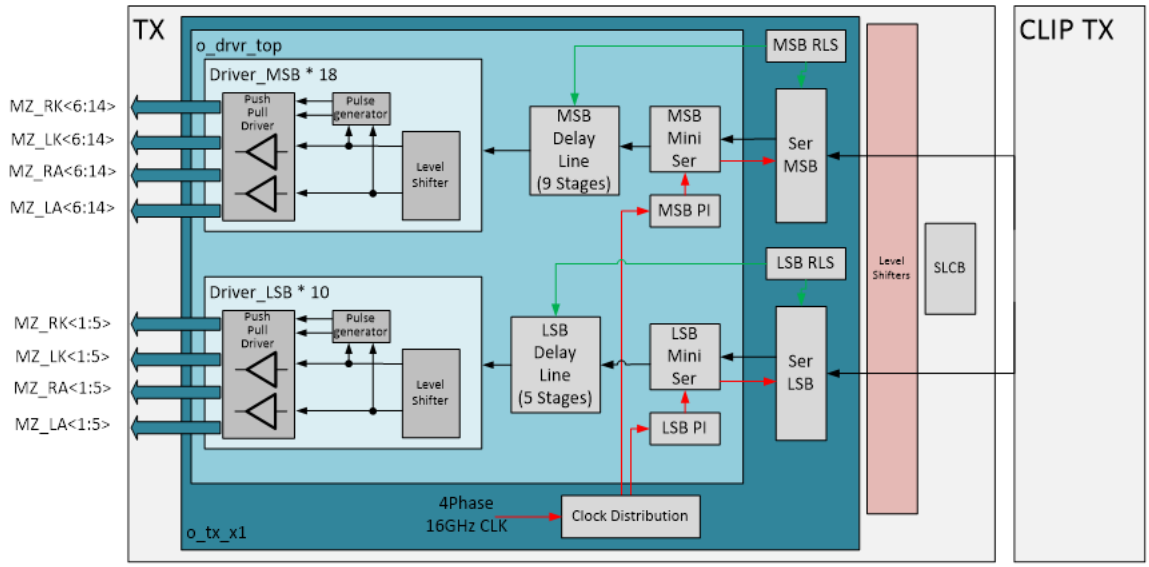


Figure 4.9 Proposed CMOS TX schematic

4.3 Circuit Design

4.3.1 Segment Driver

Optical phase shifter need certain voltage swing to generate enough optical phase changing. However, this inevitably requires circuit techniques to design high voltage driver with low power supply MOSFETs technology. A complete segment push-pull driver schematic is shown in Figure 4.10. The push-pull driver design consists of level

shifters, positive & negative pulse generation circuit, push-pull out stage with fast discharge path. The level shifter with two power supply domain enables a voltage swing from 0 to VDDH (2xVDD) for the phase shifter diode junction. In order to compensate the dynamic nonlinearity caused by junction capacitance variation in large signal analysis, a fast discharge path is added in final output stage design. The MZM electrode has larger junction capacitance when the reverse bias is 0, so extra charging current is implemented by MP3 and MN3. At the rising edge of the differential signal which from 0 to 2VDD, two short pulses are generated by the delayed line based OR/AND gate. The MP3 and MN3 will be on and an extra current path will accelerate the charge speed.

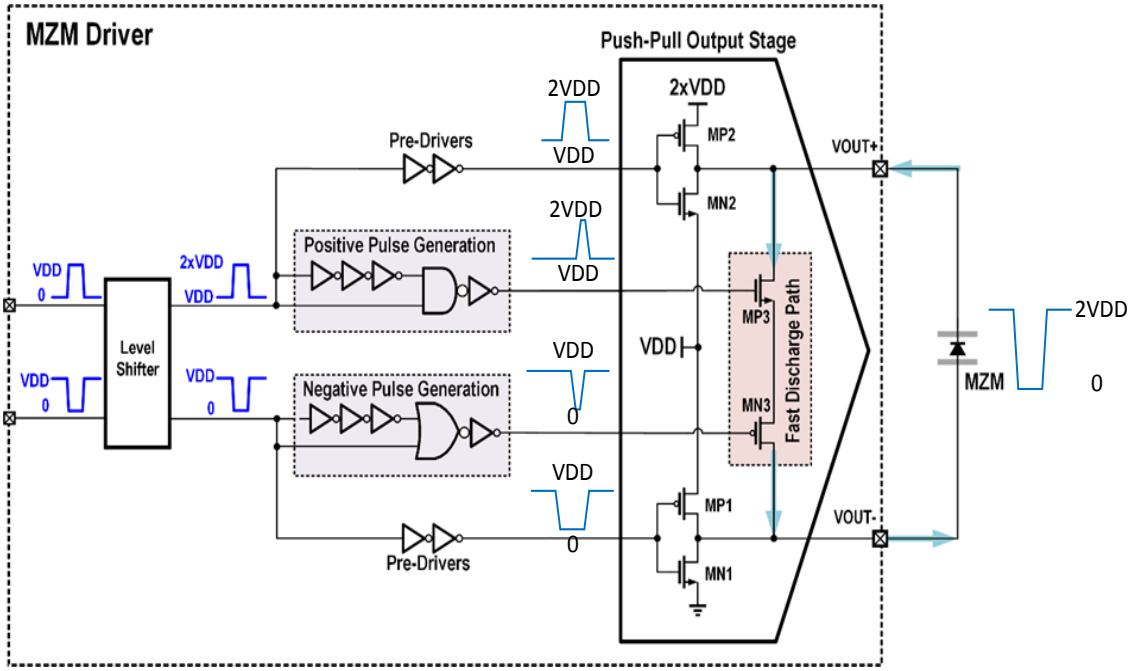


Figure 4.10 Segment driver schematic

In the driver design, latch-based level shifter couples the signal from low voltage domain to a higher voltage domain. Comparing with the traditional passive AC coupling

level shifter design, the biggest advantage of the topology shown in figure 4.11 is that there is no dc wandering issue, no pattern length (PRBS7 PRBS31) and bit rate dependency and much smaller capacitance required. However, this latch-based level shifter design has some potential voltage overshoot or undershoot issue. The overshoot or undershoot could happen at the initial signal toggling situation.

In figure 4.11, the proposed level shifter design developed a start and reset circuit in order to prevent the overshoot/undershoot in latch-based level shifter. The input complementary signal vip and vin are in the same low voltage domain, meanwhile the output complementary signals vouth and voutl are working at the high voltage domain and low voltage domain, respectively. When pd (power down) or the rst (reset) is set to be high, the node 1 before the capacitor and node 3 after the capacitor, could be set down to the low voltage (either 0 at lower voltage domain or VDD at high voltage domain) at the respective voltage domain. In order to pull down the node 1 voltage, an output enable buffer is implemented in the data path. While the OE=1, node 1 is determined by buffer's input, while OE=0, buffer output is in high impedance state. The pull down NMOS could easily set the output to voltage low. The initial reset and power-down function can share the output enable circuit. So the power down signal can disconnect the signal path from delay cell to segment driver.

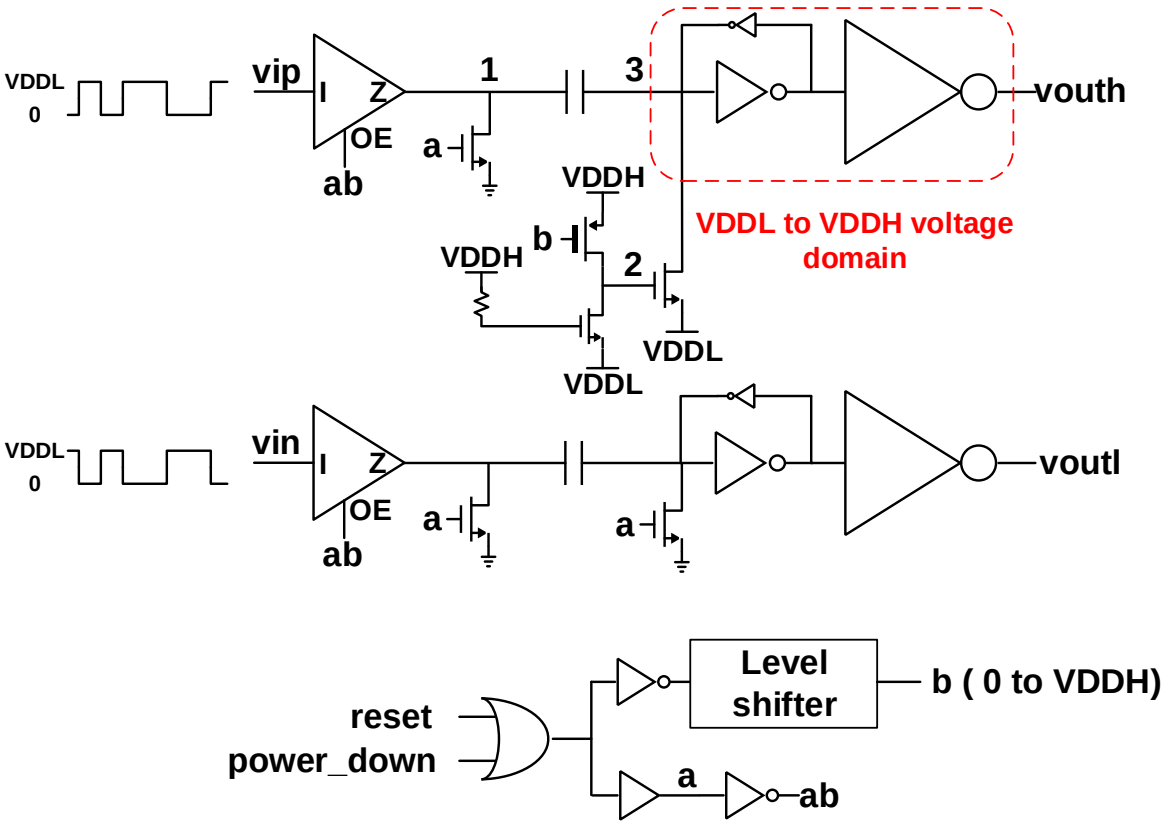


Figure 4.11 Latch based level shifter schematic

4.3.2 Delay Line

Since the MZM design is based on segmented electrode design, optical propagation delay has to match the electrical delay for every segment driver. A digital controlled delay line module is implemented for both LSB and MSB drivers. Figure 4.12 presents the top level of digital controlled delay line schematic. The delay line design consists of a truck inverter chain which provides the static delay between two segment drivers, and 5 or 9 pairs of branches where a configurable delay cell is added in order to fine tune the delay between two segments. Consider the footprint of MZM design, every

stage needs to have enough driving ability to maintain high signal quality at 32Gbps data rate. In the post layout simulation with different corner, the max variation from node A to node D is 5.5ps and delay from node B to mode E is about 12.5ps for the max delay value. Thus, the optical propagation delay of MZM segments need to be modified to 13ps by changing the waveguide routing.

In order to compensate the delay mismatch from node A to node D introduced by PVT variation, a fine-tuning delay cell is developed in every branch of the delay line. The schematic of delay cell is shown in figure 4.13 (a), total 11 different delay path is controlled by decoder for 12 step outputs, every delay path is a transmission gate with different open resistor value by change the size of the transistors. Also shown in figure 4.13 (b), the total range of the delay cell is 5.85ps with roughly 0.5ps step size. And the data dependent jitter introduced by the delay cell is about 80fs which ignorable compare with the jitter introduced by long distance driver are.

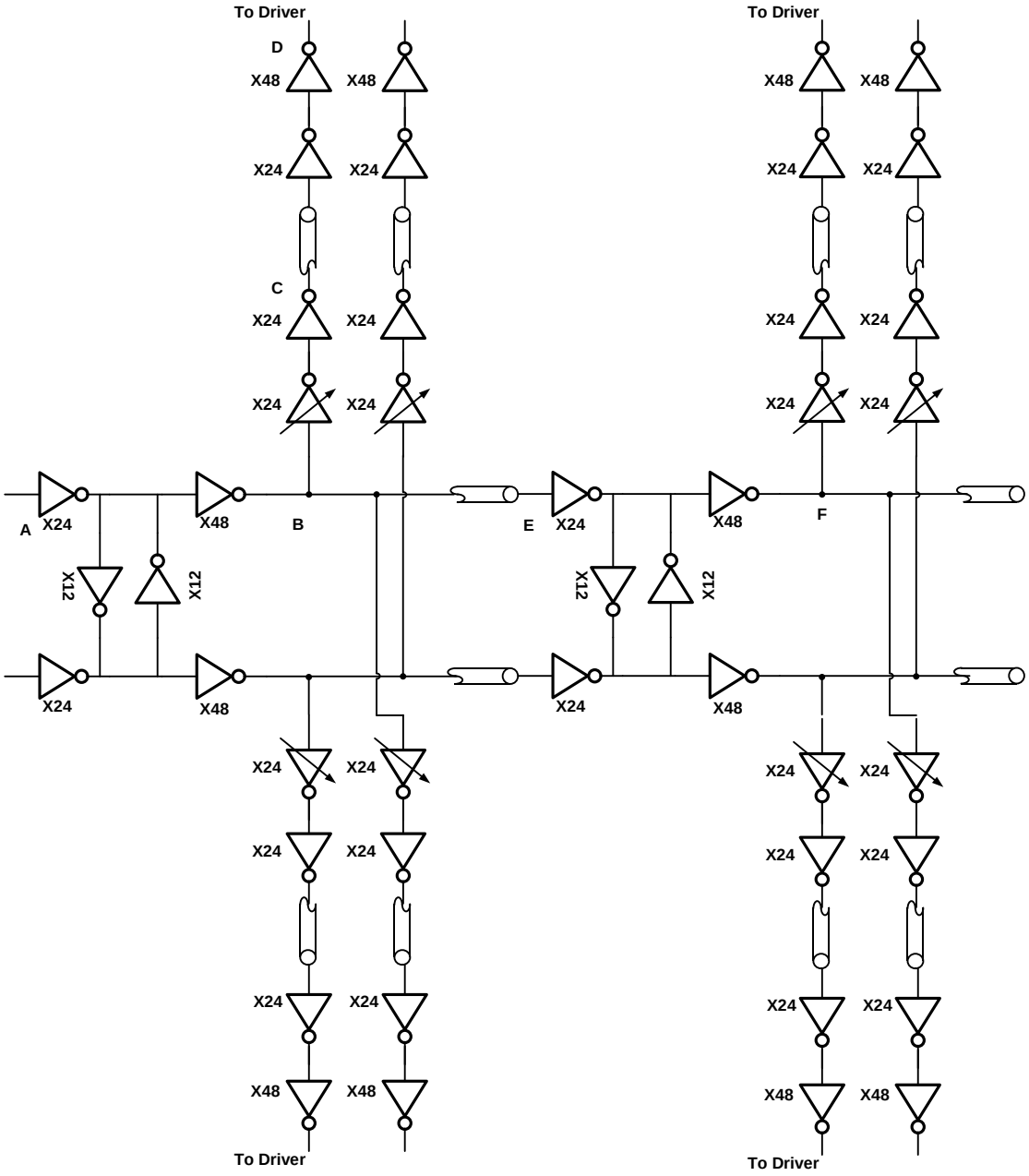


Figure. 4.12 Digital controlled delay line schematic

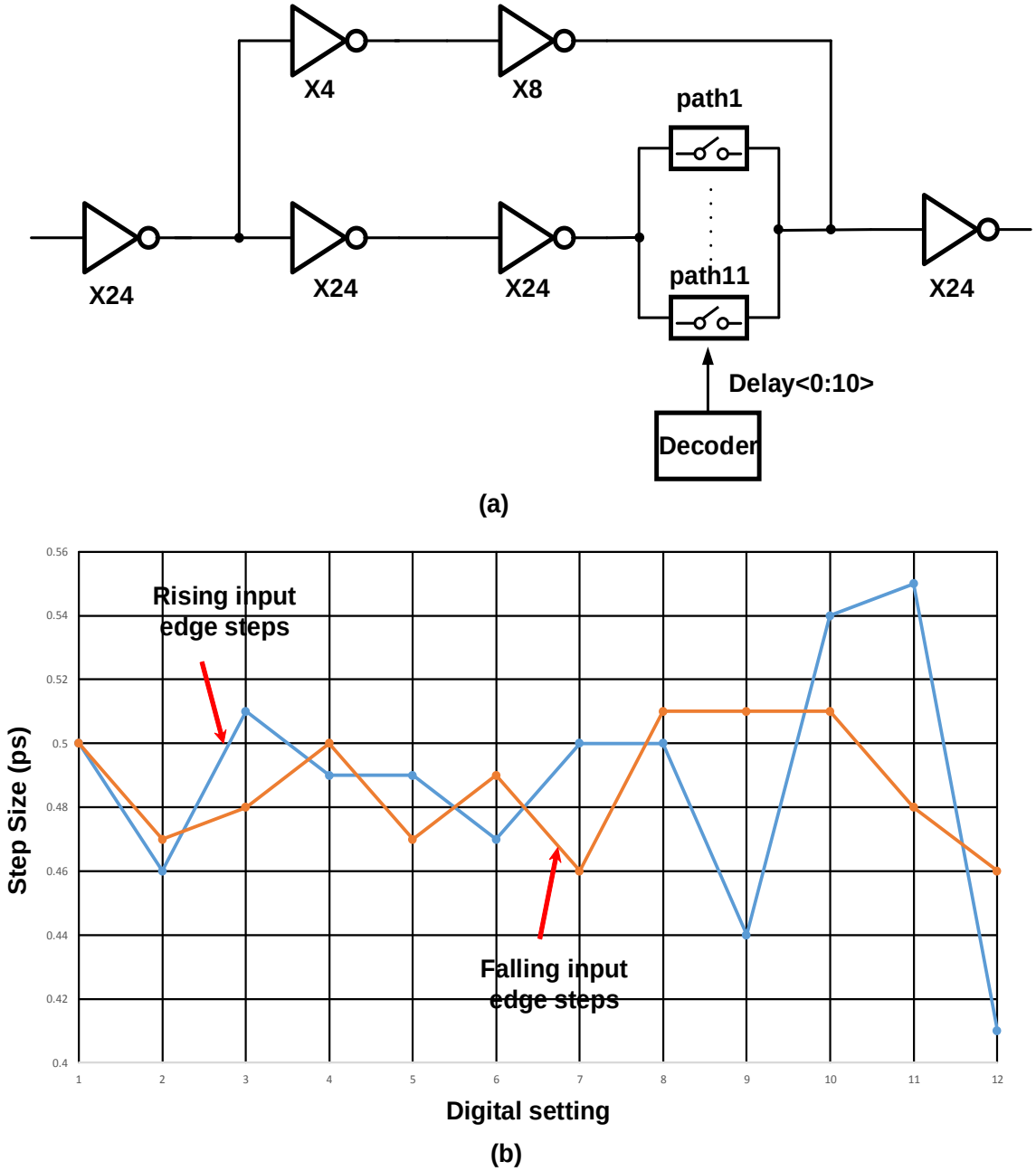


Figure. 4.13 (a) Delay cell schematic (b) Delay cell step size and total tuning range

4.3.3 Phase Interpolator

The phase interpolator (PI) module is used to compensate the optical propagation mismatch between LSB phase shifter and MSB phase shifter. Ideally, the LSB and MSB

driver share with same clocking design, the optical propagation delay for LSB and MSB is 65ps. Since the clocking delay might be different in different clock frequency, the phase interpolator provides a full tuning range from 0 to 1 total clock period. Thus, the PI could compensate the propagation delay under all working data rate.

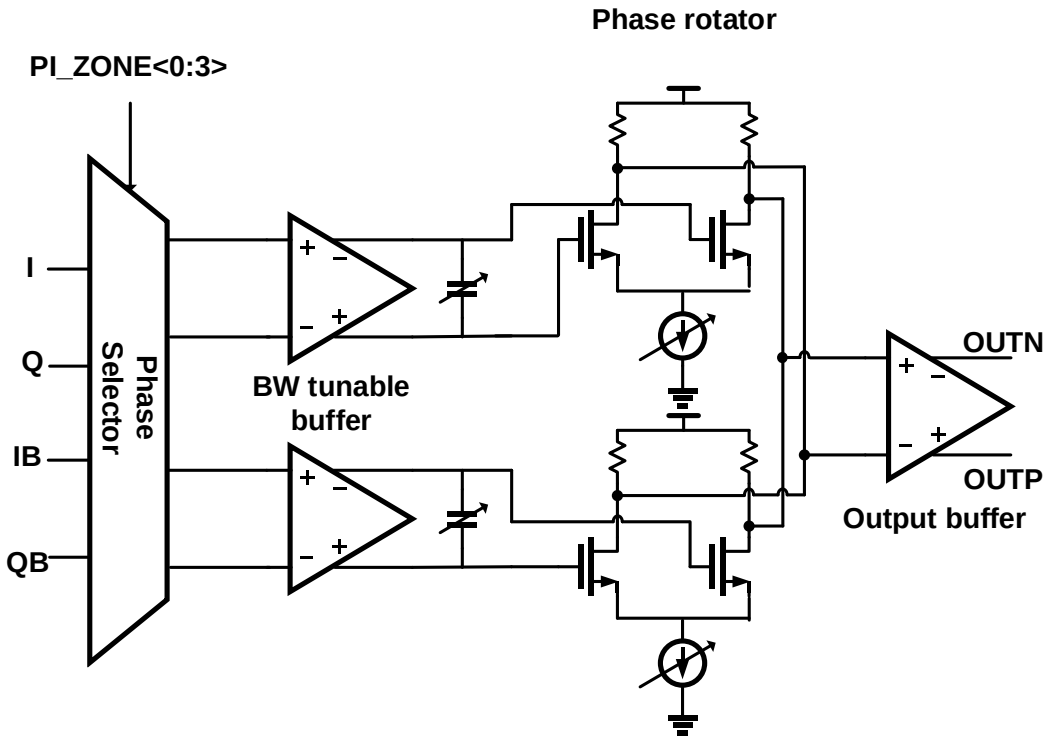


Figure. 4.14 Phase interpolator schematic

Figure 4.14 shows phase interpolator schematic that consists of a phase selector followed by bandwidth tunable buffers which always generate sinusoid waveform at any clock frequency, followed by two CML buffer with tunable current weight. The output of two CML buffer are connected to a buffer to output. The phase selector chooses one out of four interpolation domains based on PI_ZONE<0:3> control. A 4bit

complementary differential current DAC is used to control the phase rotator tail current weight. Overall, phase interpolation could have total 64 phase steps.

4.4 Experiment Results

The Mach–Zehnder modulator was fabricated in Lextera platform 130nm SOI process. The whole Si photonics chip, which is shown in figure 4.15, include a SE-MZM transmitter and 4 channel waveguide photodiode receivers. The CMOS chip was fabricated in TSMC 16nm FINFET CMOS process, which consists for 8 electrical transceivers, 4 optical receivers and 1 segment MZM driver design. The pad dimension of flip chip bonding pads is 36um by 36um which is enabled the copper pillar bump bonding. As shown in Figure 4.16, the prototype developed a die to die flip-chip bonding between the CMOS IC and silicon photonics IC (PIC). The CMOS IC flips on top of the PIC and is bonded with copper pillar bump. On the right side of PIC is the fiber array, all the grating couplers are well aligned and fixed connected with a proper angle.

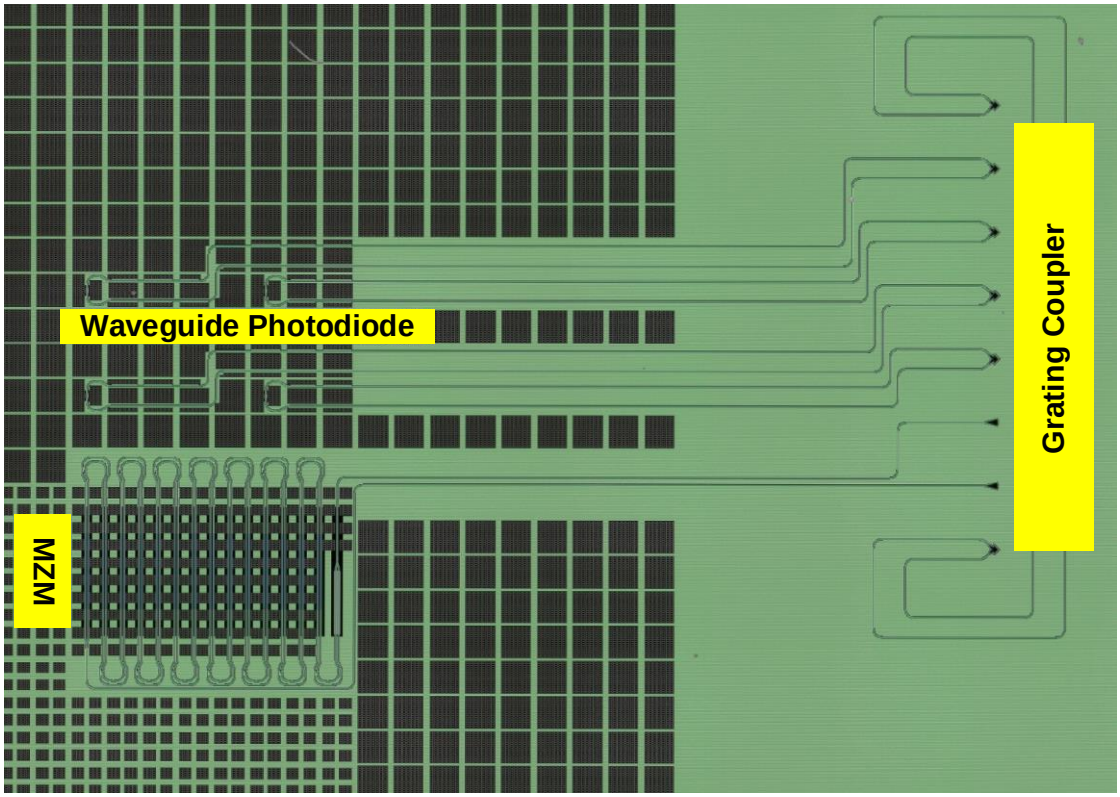


Figure 4.15 Silicon photonics chip die photograph

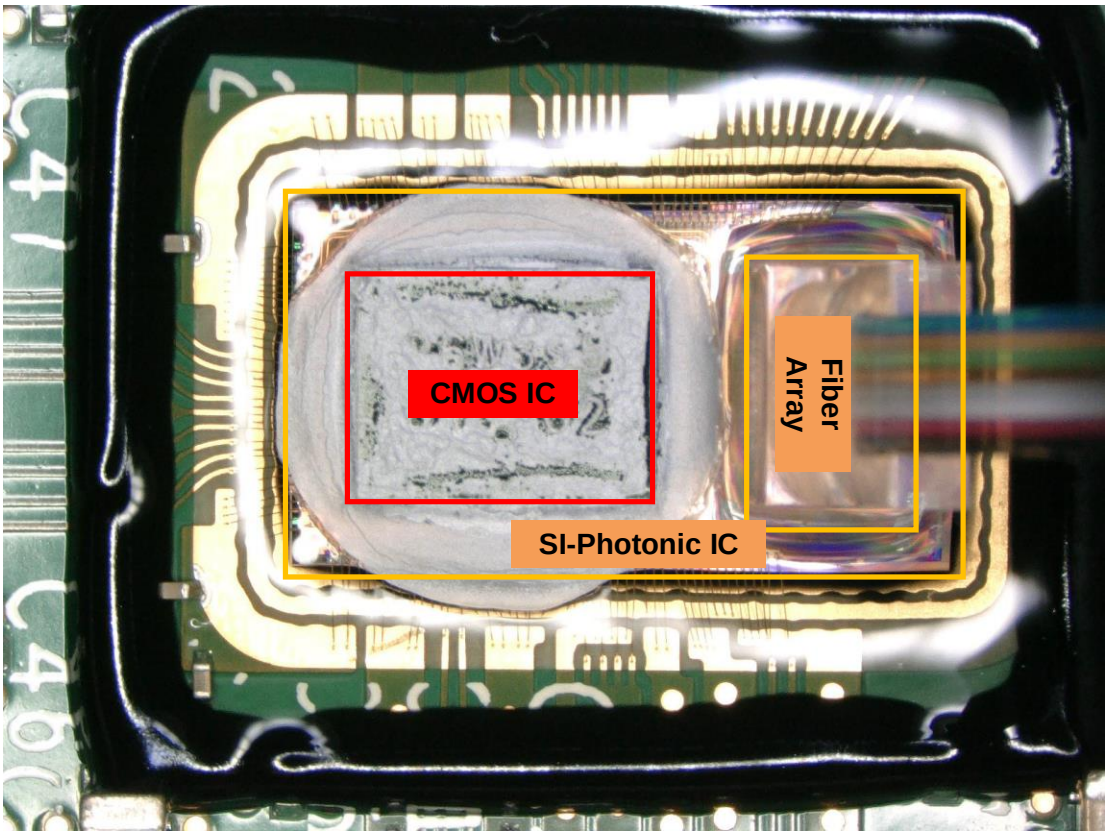


Figure 4.16 System integration photograph

Figure 4.17 shows the PAM4 transmitter measurement setup. External CW laser is connected with a semiconductor optical amplifier (SOA) and followed by polarization controller. Usually erbium-doped fiber amplifier (EDFA) provide better noise performance than SOA, however, the working wavelength of this MZM design is 1490nm which not suitable with common EDFA functional wavelength. Polarization controller can change the polarization mode of the SOA output to make sure most of light can be coupled into Si-photonic IC through grating coupler. The output of MZM is connected with Keysight 86100D, the optical module for measurement could support over 32GHZ E/O bandwidth and the input refer rms noise is about 15uW. The pattern

generator is only used to generate low speed reference clock for on chip PLL and provide a trigger signal for sampling scope. The SE MZM driver chip could generate PRBS 23 pattern for both LSB and MSB at 28Gbps data rate. With optical domain combination, the oscilloscope could observer PAM4 signals.

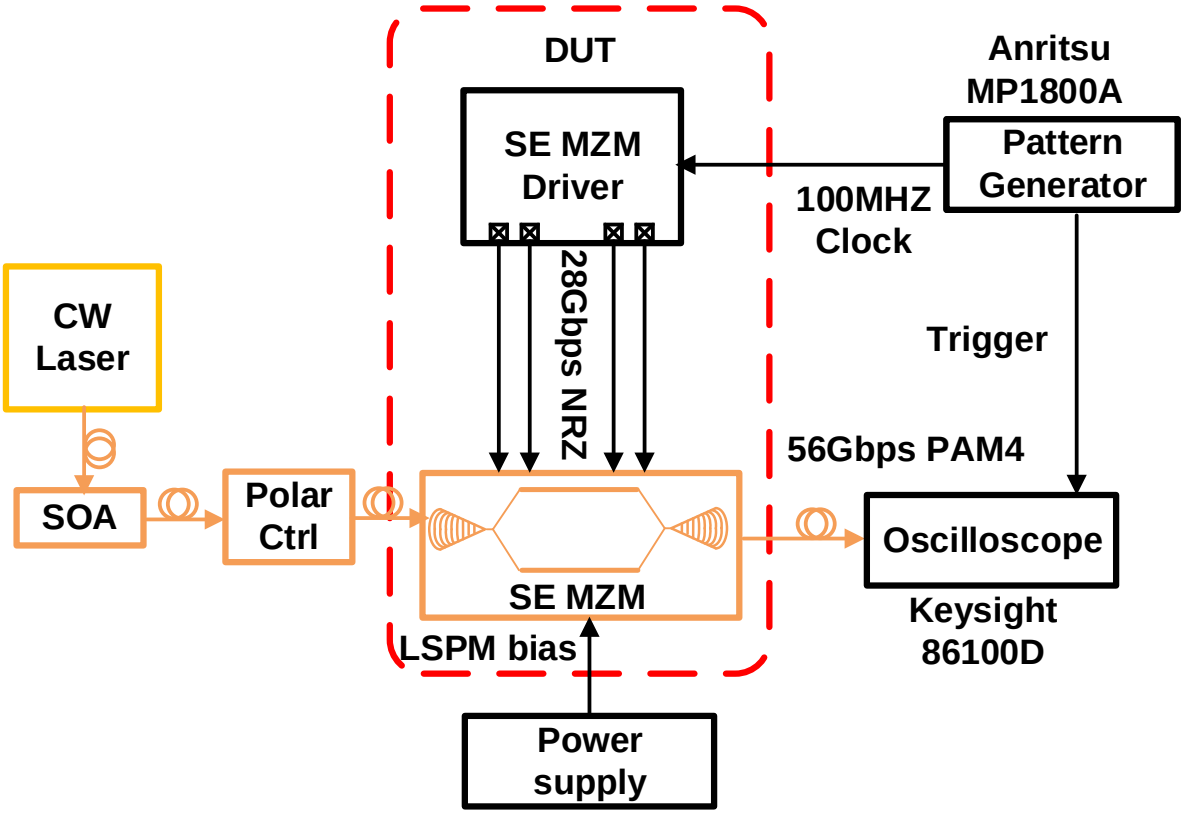


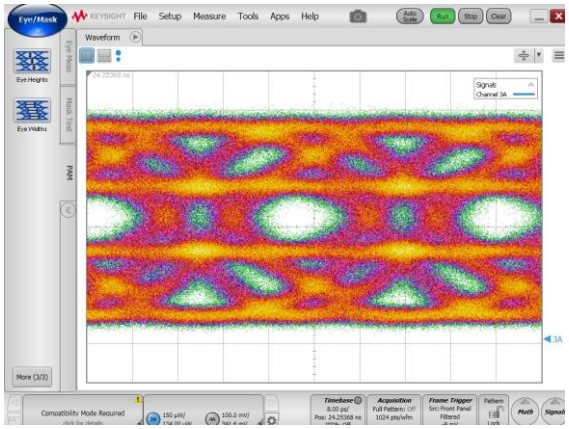
Figure. 4.17 Optical measurement setup

In order to verify the velocity mismatch compensation function, the MZM transmitter is set to working at 40Gbps and 56Gbps. As shown in the figure 4.18(a) and figure 4.18 (d), both 40Gbps and 56Gbps PAM4 optical output eye diagrams have obvious skew and very limited eye height and width for the top and bottom eye. When the phase interpolator is enabled to compensate the mismatch between LSB and MSB

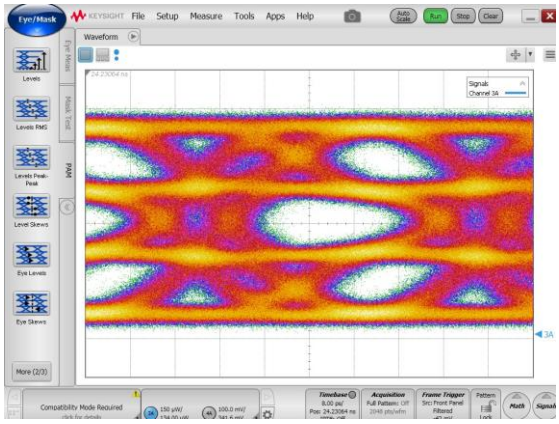
driver, both eye diagram quality is improved significantly. In figure 4.18 (b), a skew between middle eye and the other two eyes are still over 2ps and the ratio of level mismatch (RLM) is 0.941 which does not meet the IEEE standard requirement. With both PI and delay line enabled, eye diagram shows a linear and clean eye shape at both 40 and 56Gbps data rate.

TABLE 4.1 56Gbps PAM4 eye quality summary

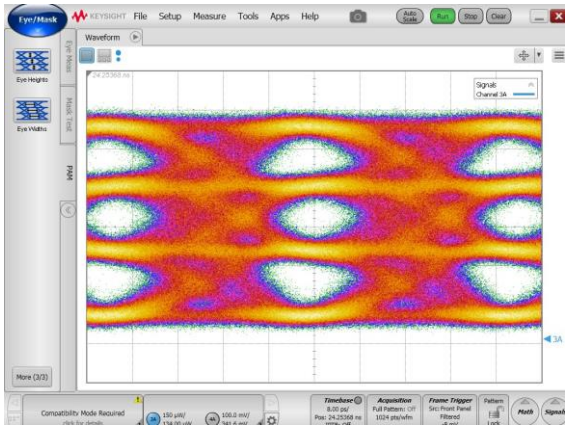
	RLM	**EYE Width**	**Eye Height**
Free run	NA	NA	NA
PI	0.941	6.83ps	18.4uW
PI+DL	0.963	7.04ps	39.2uW



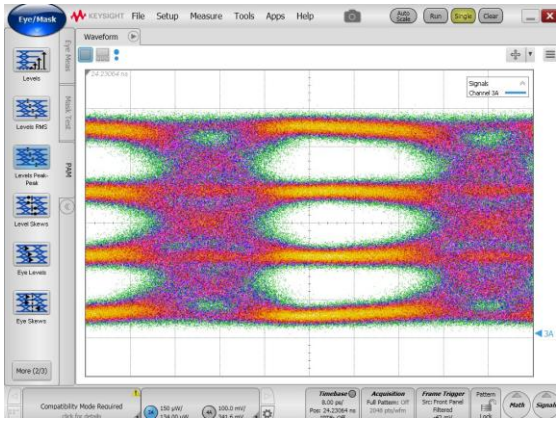
(a)



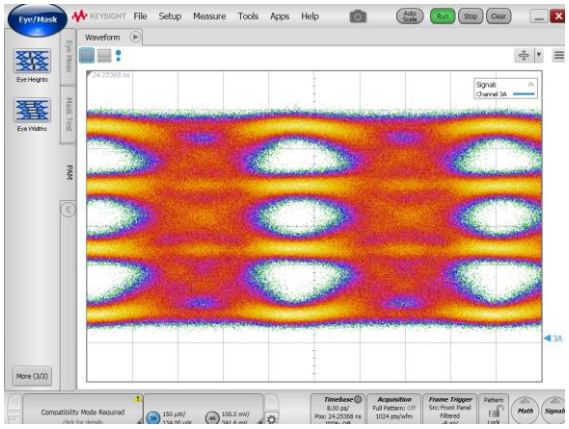
(d)



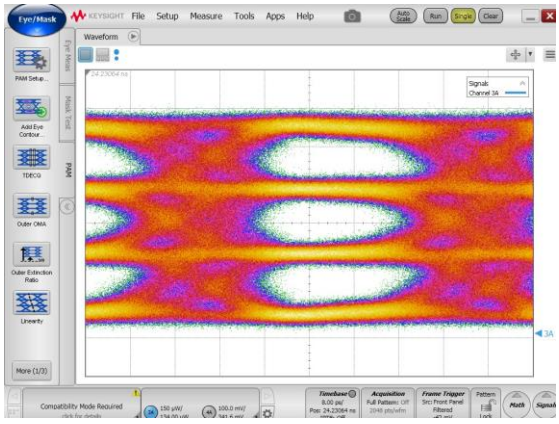
(b)



(e)



(c)



(f)

Figure. 4.18 (a) 56Gbps PAM4 eye diagram with no delay compensation (b) 56Gbps PAM4 eye diagram with PI enabled. (c) 56Gbps PAM4 eye diagram with PI & delay line enabled (d) 40Gbps PAM4 eye diagram with no delay compensation (e) 40Gbps PAM4 eye diagram with PI enabled. (f) 40Gbps PAM4 eye diagram with PI & delay line enabled

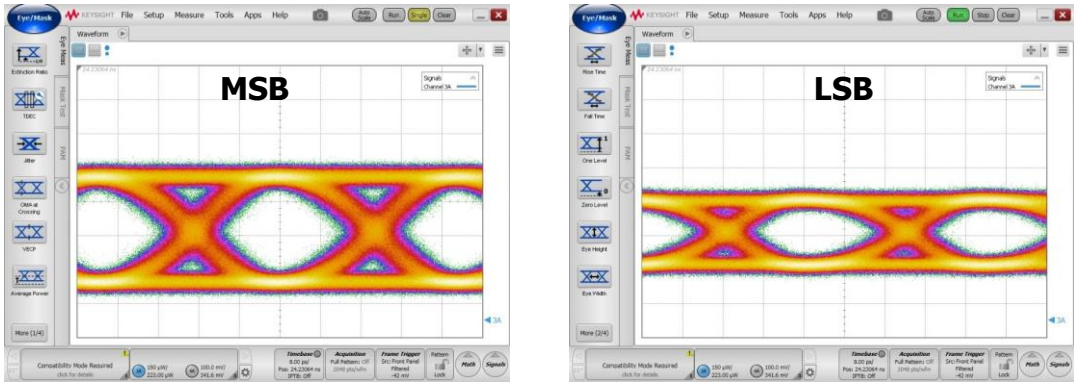
Figure 19 and figure 20 presents the segments configuration ability of the MZM transmitter design. In NRZ mode, the transmitter design could achieve high quality eye diagram in both MSB only and LSB only mode. The transmitter extinction ration is 5.7dB and 3.35dB respectively. At 28Gbps data rate, the eye width of NRZ eye is 21.68ps which is about 0.6UI eye opening consider the clocking rms jitter and data dependent jitter (ISI). In PAM4 mode, besides 5LSB+9MSB, another three configuration setting eye diagrams are shown in figure 4.20. The transmitter design could achieve 6.35dB ER and 0.942 RLM with only 3LSB and 6MSB enabled, which could save over 30% power consumption.

TABLE 4.2 28Gbps NRZ eye quality summary

	ER	**SNR**	**EYE Width**	**Eye Height**
MSB Only	5.7dB	11.63	21.68ps	342.6uW
LSB Only	3.35dB	8.55	20.96ps	184.8uW

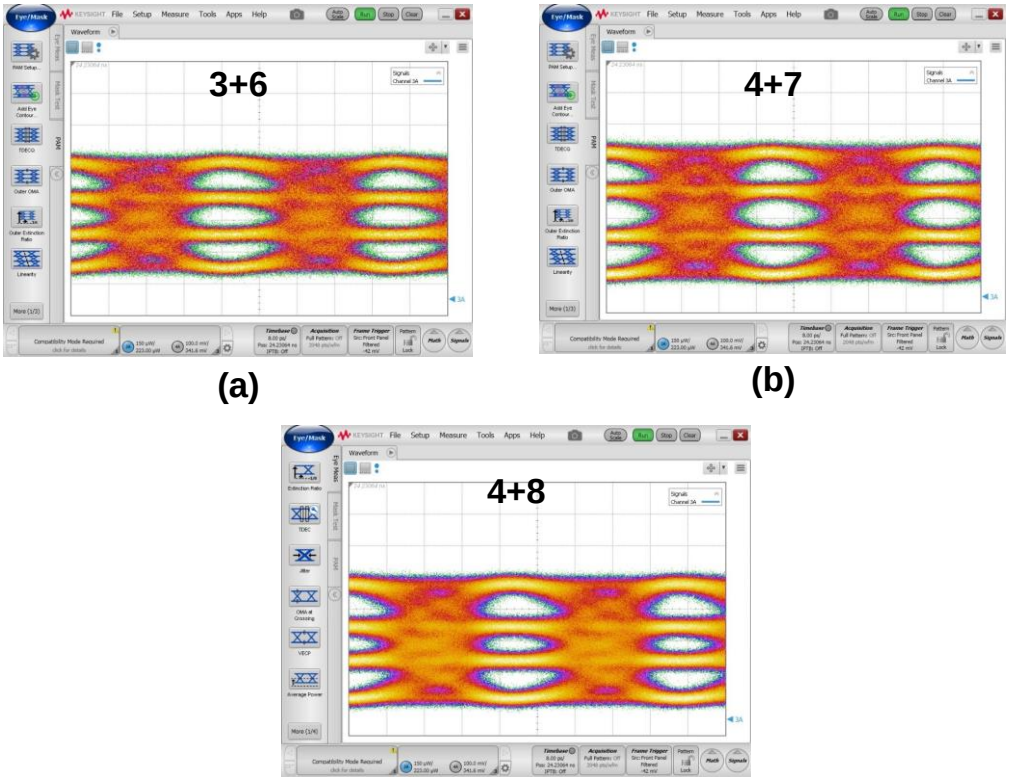
TABLE 4.3 Eye quality summary for different segment setting

	ER	**RLM**	**EYE Width**	**Eye Height**
3+6	6.35dB	0.942	5.12ps	11.6uW
4+7	8.14dB	0.896	5.01ps	4.6uW
4+8	8.46dB	0.944	5.7ps	18.4uW



(a) (b)

Figure. 4.19 NRZ eye diagram (a) MSB driver enable only (b) LSB driver enable only



(a) (b)

(c)

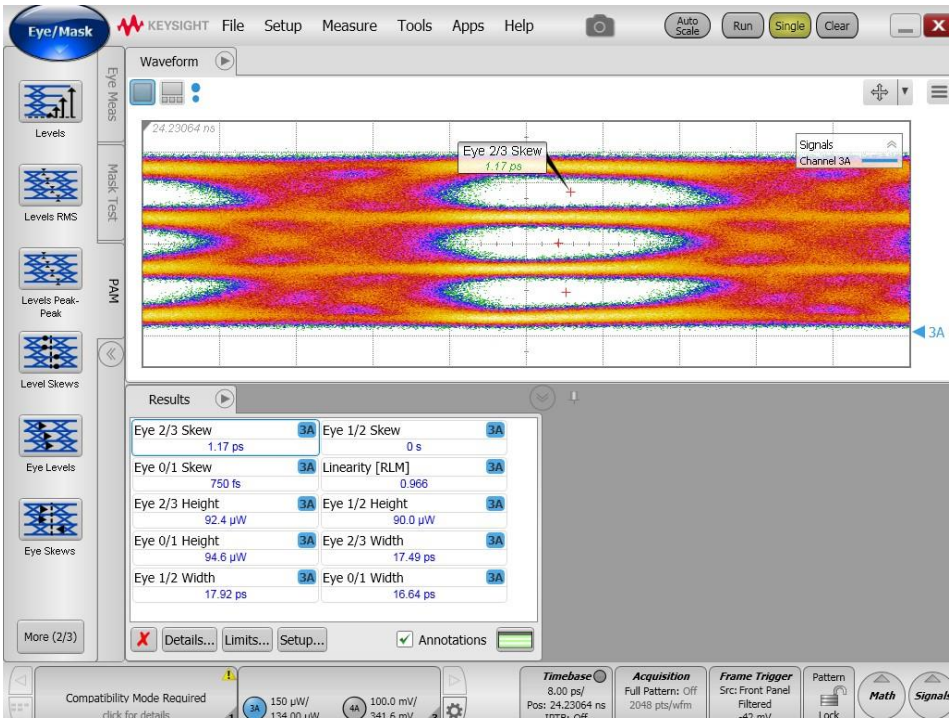
Figure. 4.20 PAM4 eye diagram with different segment configuration (a) 3LSB+6MSB (b) 4LSB+7MSB (c) 4LSB+8MSB

With the BER analysis software embedded in oscilloscope, the eye height and eye width can be measured under certain BER performance. As shown in figure 4.21 (a), the MZM transmitter achieves 16.94ps (33.9% UI) eye width opening and over 90uW eye height opening at 40Gbps data rate. The extinction ratio is over 10dB and PAM4 eye RLM is 0.966. After boosting the data rate to 56Gbps, the optical eye width opening is 7.04ps (19.7% UI) for middle eye, 9.81ps (27.4% UI) for bottom eye, and 8ps (22.4% UI) for top eye. The extinction ratio at 56Gbps is 9.5dB and PAM4 eye RLM is 0.963.

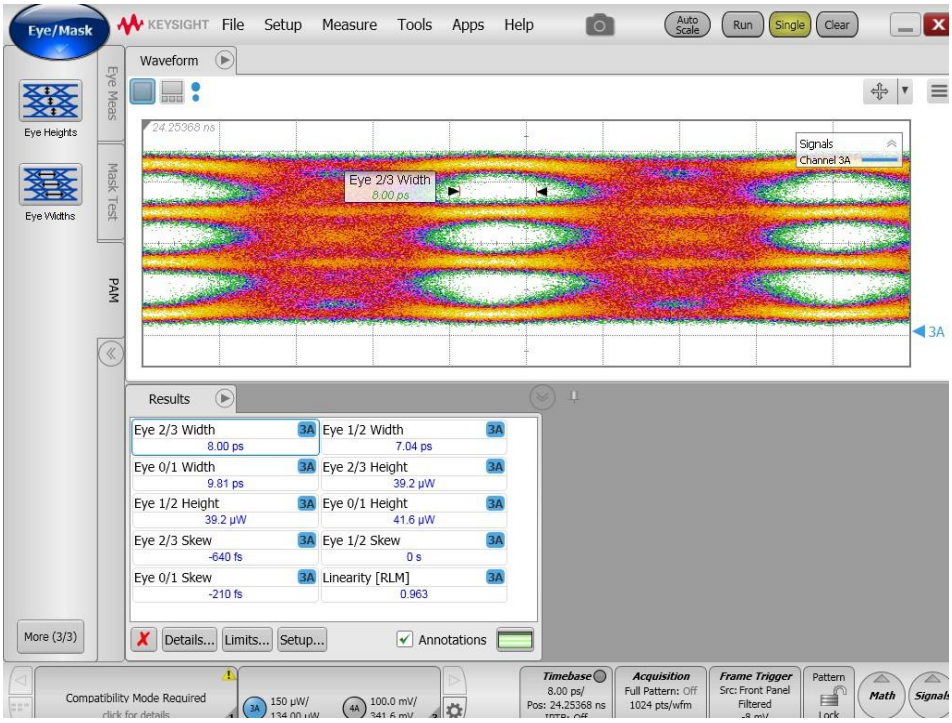
TABLE 4.4 Eye quality summary for 40Gbps and 56Gbps

	ER	**RLM**	**EYE Width**	**Eye Height**
40Gbps	10.07dB	0.966	16.64ps	90uW
56Gbps	9.5dB	0.963	7.04ps	39.2uW

Table 4.5 compares this work with other high speed MZM transmitters [52], [59], [64], [65]. Compared with all other reference work, proposed transmitter has longest MZM design and highest extinction ratio value. The power consumption of this transmitter design includes the clocking distribution and data serialization power, where the velocity mismatch circuity power consumption is also included.



(a)



(b)

Figure. 4.21 PAM4 eye diagram with BER analysis

TABLE 4.5 MZM based optical transmitter performance comparison

	[65]	[64]	[52]	[59]	This Work
CMOS Technology	65nm CMOS	55nm BiCMOS	65nm CMOS	90nm CMOS CMOS9WG	16nm CMOS
Data rate	25Gbps	56Gbps	50Gbps	56Gbps	56Gbps
Modulation Scheme	NRZ	NRZ	NRZ/PAM4	PAM4	NRZ/PAM4
Modulator Structure	SE	TW	TW	TW	SE
Integration Technology	Copper Pillar	Copper Pillar	Wire bond	Monolithic	Copper Pillar
MZM length	3mm	3mm	NA	3mm	7mm
Test Pattern	PRBS7	PRBS31	PRBS 31	PRBS23	PRBS23
ER	4-6dB	2.5dB	5.6dB	6dB	9.5dB
Power Consumption	275mW	300mW	613mW	135mW@ 50Gbps	708mW*
Power efficient	11pJ/bit	5.35pJ/bit	12.26pJ/bit	2.7pJ/bit	12.6pJ/bit

*include clocking and serialization circuit

4.5 Summary

This chapter has presented a 56Gbps PAM4 silicon photonics transmitter design. The prototype uses 3D integration technique to assemble the 130nm SOI silicon photonics IC and 16nm FinFET CMOS reconfigurable transmitter design. The optical modulator is 14 segment SE MZM design, where 5 segments working as LSB phase shifter and 9 segments working as MSB phase shifter. With 0.9V and 1.8V power supply, the MZM optical could achieve over 9dB extinction ratio at 56Gbps. In the

CMOS design, total 28 segments drivers are implemented for dual-differential dual-arm driving scheme. A latch-based level shifter and fast discharge path final stage enable driver design high bandwidth and high voltage swing solution. In order to compensate velocity mismatch between LSB and MSB, digital control delay line for both LSB and MSB need cooperate with phase interpolator in order to achieve best PAM-4 eye diagram width and linearity. The MZM transmitter achieves 7ps eye-width and 0.963 RLM at 56Gbps data rate.

5. CONCLUSION

As the high-speed I/O standards scales from 100Gb/s to 400Gb/s and higher, highspeed optical link becomes one of the most important research areas for next generation internet and cloud computing. Specifically, the development of Si Photonic devices such as microring based transceiver and MZM transmitter brings a unique solution for the research on a compact and power-efficient optical transceiver.

This dissertation has covered, most from the circuit designer's perspective which focused on high speed optical interconnects circuit design, such as TIA, push pull driver, samplers. Meanwhile also introduces optical device modeling and optical device characterization. The dissertation contents are mainly discussed my two CMOS electrical IC design during Ph.D study, one receiver chip in TSMC 65nm and one transmitter chip in TSMC 16nm.

In this work, this prototype provides a 25Gb/s hybrid-integrated silicon photonic receiver design with 130nm SOI microring drop filters and waveguide photodetectors and 65nm CMOS source-synchronous receiver front-ends. The receiver achieves low-complexity clocking with a source-synchronous architecture with LC injection-locked oscillator (ILO) jitter filtering. Sensitivity is improved with a large input-stage feedback resistor transimpedance amplifier (TIA) cascaded with an adaptively-tuned continuous-time linear equalizer (CTLE) that accounts for variations in interconnect parasitic. Compensation of microring drop filter fabrication tolerances and temperature variations is achieved with per-channel thermal tuning loops that stabilize the drop filters' resonance wavelength. The receiver achieves -8.0 dBm OMA sensitivity at a BER=10-

12 with a jitter tolerance corner frequency near 20MHz and a per-channel power consumption of 17mW including amortized clocking power.

Another prototype studies the high-speed silicon photonics transmitter design based on Mach–Zehnder-modulator. The prototype uses 3D integration technique to assemble the 130nm SOI silicon photonics IC and 16nm FinFet CMOS IC. With 0.9V and 1.8V power supply, the MZM optical could achieve over 8dB extinction ratio at 56Gbps.

In conclusion, the proposed transmitter and receiver design can be further extended to higher bandwidth and lower power with more advanced CMOS technologies and Si photonics technology for future datacenter and telecommunication applications.

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