SOFT-SWITCHING HIGH-FREQUENCY LINK CONVERTERS WITH REDUCED VOLTAGE STRESS

A Dissertation

by

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ABSTRACT

Power converters with stacked cells or stacked semiconductor switches have the widely-known advantage of achieving higher voltage or current levels by using standard low-voltage or low-current switches. This dissertation presents several galvanically isolated power electronic converters for various applications and is mainly focused on reducing voltage stress on the semiconductor switches. The proposed topologies convert power in a single stage and achieve soft-switching throughout their range of operation without utilizing snubbing or auxiliary networks. The proposed topologies are divided into three categories; DC-DC, DC-AC, and AC-AC. In each category, two power conversion topologies are presented. All proposed converters include at least one multiple-winding transformer and a resonant capacitor on each winding to form a partial-resonant AC-link which facilitates soft turn-on and turn-off transitions for all semiconductor devices. The magnetizing inductance of the transformer is the key component in energy transfer. Due to non-appearance of a DC link, the proposed converters do not require bulky electrolytic capacitors to convert power. Since the AC-link operates at several kilo-hertz, the transformer size and weight are significantly smaller than the conventional line-frequency transformer.

Reduction of switch voltage stress is achieved through a sequential connection of *cells*. Each cell is composed of one transformer winding, one resonant capacitor, and one or more semiconductor devices. The reduction factor in the voltage stress is directly proportional to the number of cells. The energy stored in winding leakage inductances is

fed to the AC capacitors to mitigate switching spikes without using auxiliary snubbing switches. The transformer design is simple because the inverter operation and soft-switching are not affected by the transformer non-idealities.

DEDICATION

To my beloved family and my dearest grandmother and grandfather…

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1 INTRODUCTION

Hard-switching Pulse-Width-Modulated (PWM) Power converters are the most common power electronic converters in the industry because of their ruggedness and simplicity [37]. These advantages usually come at the cost of an efficiency drop due to high switching losses and severe Electromagnetic Interference (EMI) due to high *dv/dt* and *di/dt*. Soft-switching schemes and multi-cell structures have been proposed over the past several years to address these implications [37][48][49][52][67]-[77]. Soft-switching converters rob the switch of its current and/or voltage at the switching instant to create a soft-transition and eliminate or reduce switching losses. This is often achieved by creating a resonant behavior in the waveforms, which results in a ripple in the switch voltage and current and necessitates higher ratings for the switches, especially at high power ranges [48]. Multi-cell structures and specifically multi-level schemes arrange a plurality of components in a way that the switching stress is divided and switch ratings, *dv/dt*, and/or *di/dt* are reduced. The list of multi-cell structures includes, but is not limited to, the cascaded H-bridge [49], diode clamped converters [67], and flying capacitor [69].

A converter can combine the soft-switching and multi-cell features. A significant amount of attention has been given to three-level dc-dc and dc-ac soft-switching converters [71]-[76]; however, a large advantage in terms of reduction of voltage stress on switches cannot be obtained with only three levels. In [48], a soft-switching dual-active bridge dc-dc converter uses two series-connected half-bridges to achieve a high voltage on the output. In [70], a resonant high step-down dc-dc converter is proposed that has

several half-bridge modules on the input side to accept a high voltage, but it is non-isolated. A multi-level flying capacitor inverter is introduced in [42]. Although this non-isolated inverter benefits from soft-switching for all switches and diodes, each phase leg requires auxiliary circuitry that includes two coupled inductors to lower the semiconductor ratings. Another soft-switching approach that can be applied to multi-cell inverters is the use of the Auxiliary Resonant Command Pole (ARCP) [51][52], but cell voltage balancing analysis of the ARCP inverter is rather complicated. Also, the operation of the auxiliary devices at light and full load conditions are different, and this method requires current zero-crossing detection [37].

This dissertation proposes several DC-DC, DC-AC, and AC-AC isolated power converters. The proposed converters utilize a partially resonating LC link to achieve soft-switching throughout their range of operation. Several of these converters offer a method to split the voltage stress among their switching devices to facilitate utilization of low-voltage semiconductors.

Since the proposed topologies are usable in different application, each chapter of this dissertation has a dedicated introduction and conclusion that focuses solely on that specific topology.

2 DC-DC TOPOLOGIES

This chapter proposes two soft-switching DC-DC converters. The fist topology is based on a three- or four-winding push-pull structure. The second topology is a soft-switching flyback converter with stacked output cell which provides a high voltage gain.

2.1 Push-Pull Converter[1]

2.1.1 Introduction

The need for power conversion through power electronic converters has been increasing rapidly over the past decades [1-4]. The push-pull converters are a popular candidate where dc-dc conversion is required. The push-pull converters are capable of processing higher power levels compared to the Forward converters. They can provide a high voltage gain and galvanic isolation through a three- or four-winding transformer. However, the conventional push-pull converter suffers from hard switching losses and spikes due to the leakage inductance of the primaries, which necessitates dissipating snubber circuits. Extensive research has been devoted to tackle this issue by creating soft-switching conditions. In [1], an LC resonant tank is used for each of the input switches to create Zero Voltage Switching (ZVS) at turn-on. Soft-switching is achieved in the ac module of [5] through a parallel LC resonant tank on the secondary side of the transformer. The leakage

[1] © 2016 IEEE. Reprinted, with permission, from M. Moosavi and H. A. Toliyat, "Soft-switching push-pull converter with parallel resonant link and buck-boost capability," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

inductance acts as the resonant inductor. Input switches turn on with ZVS and turn off with Zero Current Switching (ZCS). Reverse recovery on the rectifying diodes is claimed to be eliminated due to the fact that the current through the secondary leakage inductance approaches zero. This converter requires a boost inductor on the input side. A three-transistor Push-Pull topology is proposed in [6], in which ZVS at a certain power range is achieved. Compared to a conventional three-winding push-pull converter, this topology requires one additional transistor, three capacitors, a saturable inductor, and a free-wheeling diode. Research carried out in [7] has led to a two stage bidirectional inverter with ZCS for primary switches and ZVS for secondary switches. It uses a voltage doubler to decrease the transformer turns ratio. An input inductor is installed in series with the source to supply the current-fed converter. In [8], a high-frequency link half-bridge converter with ZCS is presented. In addition to the series resonant tank, the converter uses a pair of assistive inductors and a snubbing capacitor to facilitate the soft-switching. This converter can achieve high efficiencies due to using only a few semiconductor devices in the current path. However, its control and operation is rather complicated.

An innovative class of universal (ac-ac and dc-dc) isolated converters with an ac link was invented in [9], comprised of two legs of switches on each side of the transformer. The converters have a parallel inductive-capacitive ac link and operate with ZVS. In [10], two isolated dc-dc converters with a partial resonant LC link are proposed. However, the single-ended converters utilize the magnetic core only in one polarity of flux due to the dc offset in the magnetizing inductance current. In [11], although the isolated buck-boost dc-

dc converter operates the core in both half-cycles, the current has to pass through multiple semiconductor devices on the input and output sides which increases conduction loses.

The partial resonant push-pull converter proposed in this section also uses a parallel LC link, but requires only two bottom-side switches on the primary and a three-winding transformer. The link current and voltage are fully ac, eliminating the need for bulky electrolytic capacitors. Turn-on transitions for all switches occur at ZVS. Turn-off transition for all switches is soft and losses are reduced by limiting the rate of rise of voltage using three capacitors. The three capacitors operate together and can be considered one capacitor during the design and analysis. Since the transformer magnetizing inductance is used as the resonant link, no extra inductor is required. This inherently buck-boost converter maintains the soft-switching features for all load current and voltage ranges and does not require any dissipating snubbers on the input or output sides. The proposed control strategy is simple and easy to implement. The rest of this section explains the topology and its operation, provides an analytical approach to converter's operation, and presents the experimental results.

2.1.2 The Proposed Converter

2.1.2.1 The Topology

Figure 1 depicts the proposed partial-resonant Push-Pull converter. The three capacitors, C_1, C_2, and C_3, together with the magnetizing inductance L form a parallel resonant link. The converter is different than the conventional Push-Pull in the sense that the magnetizing inductance transfers the energy by charging from the source and discharging into the output. All switches conduct unidirectional current. However, the input switches

should block voltages of both polarities. This can be achieved by using a reverse-blocking switch or simply by putting a diode in series with each switch. Table I lists the naming conventions for variables and parameters of the converter.

2.1.2.2 Operating Modes

Each link cycle T_{Link} is comprised of eight modes as shown in Figure 2 (a) and (b) for boost ($V_{in} < V_o/N$) and buck ($V_{in} > V_o/N$) operations, respectively. However, the principle of operation and the implementation of the converter are the identical for boost and buck schemes. The rest of this sub-section elaborates the eight modes, assuming that all components are ideal.

Mode 1: The link is charged by the source through switch S_1 as shown in Figure 2(a,b). The link current i_L increases almost linearly in this mode. All other semiconductors are in

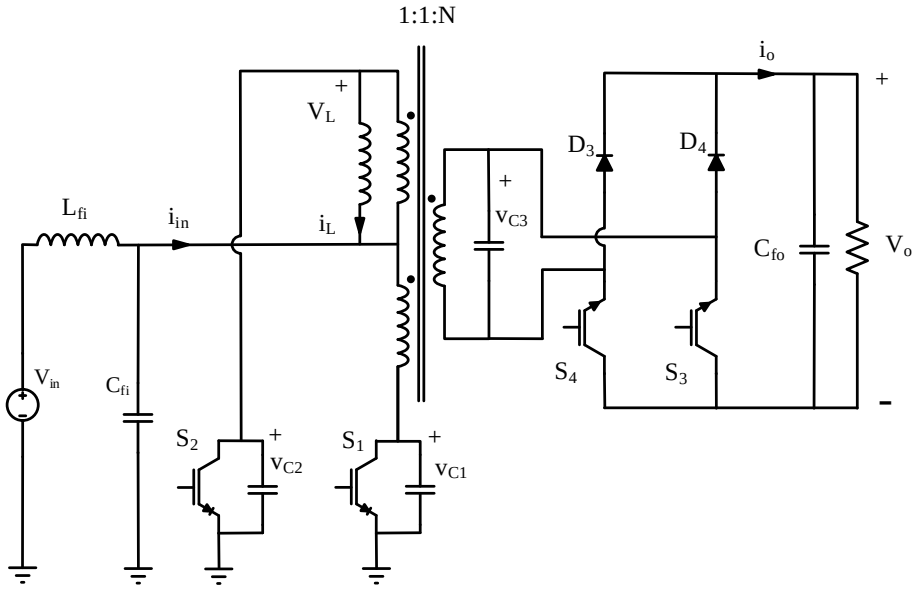


Figure 1 - The proposed push-pull converter [26].

TABLE I. NAMING CONVENTIONS [26]

Symbol	Description
L	Magnetizing and link inductance as seen on primary
C_{tot}	Link equivalent inductance
L_{fi}. C_{fi}, C_{fo}	Input and output filters
$v_{L,}$ i_L	Link voltage and inductor current as seen on primary
m	Mode number, m=1,..,8
$I_{m,0}$	Link Current at beginning of mode m
$V_{m,0}$	v'_{C3} at beginning of mode m
$E_{m,0}$	Energy stored in link at beginning of mode m
T_m	Duration of mode m
ω_{res}	Link angular resonant frequency
f_{Link},ω_{Link}, T_{Link}	Link frequency, angular frequency, and period
$E_{desired}$, V_{peak}	Link energy and peak voltage, in modes 4 & 8
I_{peak}	Link peak current, in modes 2 & 6

their blocking state. Voltages v_{C1}, v_{C2}, and v_L are *0*, $2V_{in}$, and V_{in}, respectively. Since winding resistances are ignored, v_L is equal to v_{C3}/N. Once one half of the input current reference $I_{in,ref}$ is met, switch S_1 is gated off. The other half of the input reference is to be met in mode 5. Due to the presence of a capacitor in parallel with the switch S_1, the rate of rise of switch voltage at turn-off is limited. The capacitor is a loss-less snubber and effectively reduces the switching loss at turn-off. As it will be explained later in this section, this capacitor, although connected in parallel with the switch, does not cause a current inrush into the switch at turn-on.

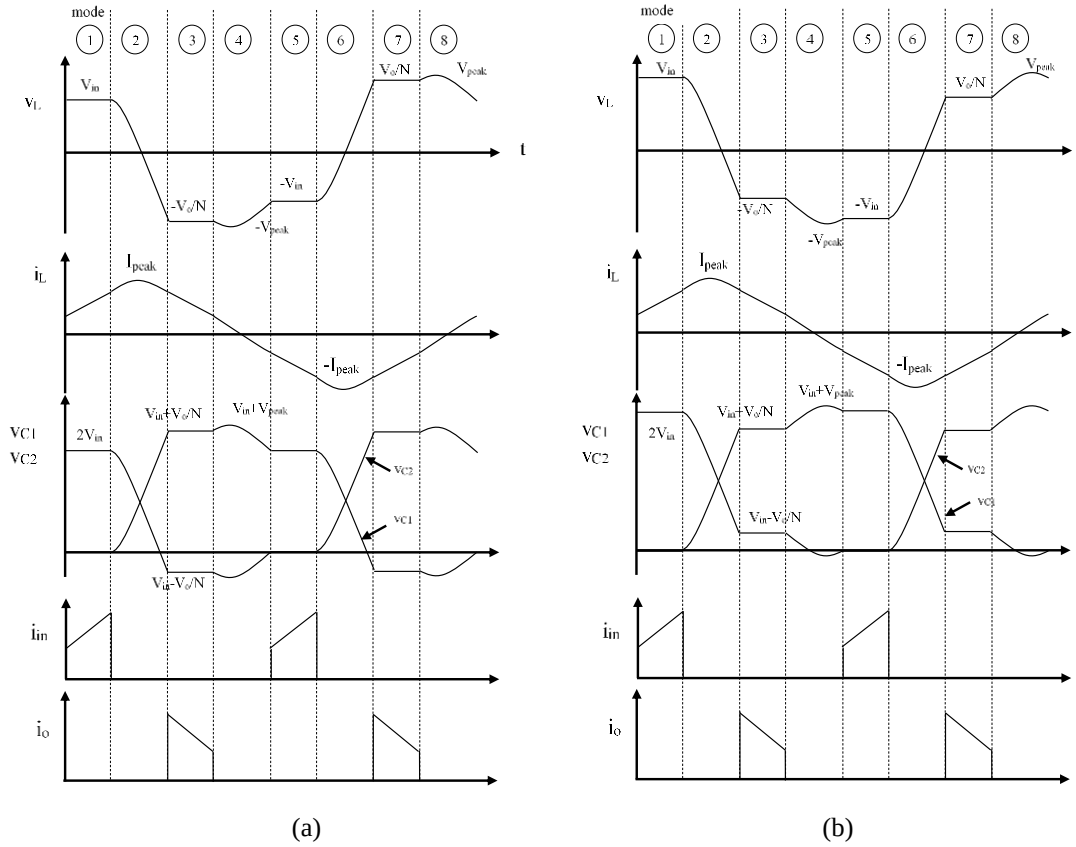


Figure 2 - Converter waveforms; a) Boost mode where $V_o/N > V_{in}$; b) Buck mode where $V_o/N < V_{in}$ [26].

Mode 2: None of the switches conduct in this mode. It will be proved later in Section 2.1.3 that the link inductor together with the three capacitors form a second-order resonating LC tank. During resonance in mode 2, v_{C1} increases in the positive direction, while v_{C2} and v_{C3} go negative. The link voltage v_L changes polarity in this mode and becomes negative, and the link current has its peak value, $+I_{peak}$, as shown in Figure 2(a,b).

This mode goes on until the reflected link voltage Nv_L matches the output voltage V_o in magnitude. At this point, the output switch S_3 and diode D_3 start conducting. The voltage

on the switch is zero, leading to a ZVS condition and eliminating turn-on losses on the switch.

Mode 3: The link inductor is connected to the load through S_3 and D_3. The link current reduces almost linearly as its energy is transferred to the output filter capacitor. Link voltage v_L in this mode is $-V_o/N$. S_3 is gated off by the controller as soon as the total energy stored in the link reduces to a desired level $E_{desired}$. This ends mode 3. The reason why such a condition is chosen to end mode 3 and selection of a proper value for $E_{desired}$ is elaborated later in this section. Because C_3 and C_{fo} have the same voltage, voltage rise on S_3 and D_3 happens slowly and turn-off losses are effectively reduced.

Mode 4: None of the switches carry current in this mode. With the leftover energy from mode 3, the LC link resonates. As shown in Figure 2(a,b), the link current crosses zero in this mode, causing the link voltage to have its negative peak $-V_{peak}$. This mode continues until the voltage on S_2 and C_2 reaches zero. This is a perfect moment to switch on. This guarantees ZVS for S_2 and eliminates turn-on loss on the switch.

Mode 5: As in mode 1, power is transferred from the input to the link. The link, however, is charged with negative current and voltage since S_2 conducts. Considering the fact that half the input current $I_{in,ref}$ was met in mode 1, switch S_2 is gated off as soon as the other half of the input current is met. Similar to mode 1, the rate of rise of voltage on S_2 is limited by its parallel capacitor C_2, and the loss associated with switch turn-off is reduced.

Mode 6: This resonant mode is essentially similar to mode 2, except that link voltage and current polarities are reversed. Since neither the input nor the output is connected to

the link, the link resonates. As soon as the reflected link voltage Nv_L increases to V_o, the output switches S_4 and diode D_4 start conducting, creating ZVS on the switch.

Mode 7: Similar to mode 3, the link is discharged into the output. However, link voltage and current polarities are reversed. S_4 and D_4 carry the link current in this mode. This mode continues until the link energy reduces to a desired level $E_{desired}$. Since the reflected link voltage matches the output filter capacitor voltage, soft-switching is achieved at turn off for S_4.

Mode 8: Similar to mode 4, none of the switches conduct in this mode. The link resonates and the link current changes polarity to become positive. At zero crossing of the link current, the link voltage peaks at $+V_{peak}$. Once the reflected link voltage equals the input voltage, S_1 and D_1 start conducting. Similar to mode 4, turn-on happens under ZVS condition. After mode 8, the converter starts from mode 1 and repeats the cycle.

The above description of modes indicates that all resonant modes are even-numbered, and all power transfer modes are odd-numbered. There is one resonant mode between every two power transfer modes. Resonant modes are meant to provide soft-switching conditions for all turn-on and turn-off transitions, and play no role in transferring power between terminals. Therefore it is important to select minimal values for link inductors and capacitors to minimize the resonant periods. Too small link values, however, increase the resonant frequency of the LC network and therefore necessitate a very high sampling rate on the digital controller, complicating the hardware implementation. The alternating "push-pull" nature of the switching sequence provides bipolar utilization of the magnetic core. As for all double-ended converters, this increases the power density of the magnetic

device and eliminates the need for any core resetting scheme. Since the amount of link energy at the end of modes 3 and 7 are forced by the controller to be equal, the unwanted dc offset of the magnetizing inductor (which is a major problem for the push-pull topology) is automatically eliminated.

2.1.2.3 Selection of $E_{desired}$

It was mentioned earlier in this section that the requirement to end modes 3 and 7 is to have the energy left in the link reduced to a desired level $E_{desired}$. This condition guarantees that the same amount of energy that was delivered to the link in mode 1 (or 5), is taken from the link in mode 3 (or 7). In other words, it assures that the link energy content at the beginning of mode 1 equals the link energy content at the end of mode 3, thereby indirectly balancing the input and output powers. Also, the parameter $E_{desired}$ determines the link energy level during resonant modes 4 and 8. Since the link energy during these two modes remains essentially unchanged, and bearing in mind that at peak voltage the link current is zero, one can find the link peak voltage as a function of $E_{desired}$:

$$E_{desired} = \frac{1}{2} C_{tot} V_{peak}^2. \tag{1}$$

It is recommended to use the lowest possible value for $E_{desired}$ because large values lead to a large peak voltage that may damage the converter. Also, they make modes 4 and 8 too lengthy, thereby unnecessarily reduce the link frequency. Too small values, on the other hand, may make modes 4 and 8 too short to such an extent that the digital controller cannot detect the end of modes 4 and 8. Care must be taken on selection of $E_{desired}$ when the converter operates in buck mode, i.e., when $V_{in} > V_o/N$. According to Figure 2(a), in

modes 4 and 8 the link voltage should travel from a smaller value ($\pm V_o/N$) to a larger value ($\pm V_{in}$). If there is not enough energy in the link, it can never reach $\pm V_{in}$, and ZVS will not be achieved at the turn-on of the corresponding input switch.

To summarize, the energy condition in modes 3 and 7 brings the following advantages:

- Indirectly provides input-output power balance, hence eliminating the need for output power measurement and converter loss calculation;
- Controls link peak voltage;
- Provides ZVS at the beginning of mode 1 and 5 in buck mode (when $V_{in} > V_o/N$).

2.1.3 Analysis and Design

2.1.3.1 Derivation of Converter Equations

This section aims to establish an analytical approach to the converter's operation. Especially, the relations between link parameters, transformer turns ratio, link frequency, and link peak voltage and current are derived. Results of this section can be used to select values for inductance, capacitance, and turns ratio. The following assumptions are made during this analysis:

- In charge and discharge modes (odd-numbered modes) the transformer winding resistances are factored into the equations. However, since the link capacitor voltages are almost constant in this mode as shown in Figure 2, all link capacitor currents are almost zero and thereby ignored. This removes three capacitors from the circuit model and reduces the circuit order from 4 to 1 at the expense of causing a highly negligible error.

- Winding resistors are entirely ignored in resonant modes. This is because during resonant periods, the impedance of link capacitors is larger than the resistances by at least two orders of magnitude. This reduces the circuit order from 4 to 2.
- The voltage ripples on the input and output filter capacitors are ignored.
- Voltage drops on semiconductors are ignored.
- Variable *t* in the equations is the time elapsed since the start of the ongoing mode.

According to Figure 2, and benefiting from the fact the link voltage and current have half-wave symmetry, one can write:

$$T_{Link} = \frac{2\pi}{\omega_{Link}} = 2 \times (T_1 + T_2 + T_3 + T_4) \tag{2}$$

Since modes 5 to 8 are essentially identical to modes 1 to 4 except for a polarity inversion, it is sufficient to analyze only the first four modes. Because S_1 conducts in mode 1, with reference to Figure 1, the link voltage and current in this mode are readily derived as follows:

$$\begin{cases} v_L(t) = V_{in} - R_{in} i_L & (3) \\ i_L(t) = \dfrac{V_{in}}{R_{in}} + \left(I_{1,0} - \dfrac{V_{in}}{R_{in}}\right).e^{-\frac{R_{in}}{L}t} & (4) \end{cases}$$

Since no switches conduct during resonant modes 2 and 4, the equivalent circuit for resonant modes reduces to that of Figure 3. Taking the link current i_L and the link voltage v_L as state variables, the following equations are derived from the equivalent circuit:

$$i_L + C_{tot} L \frac{d^2 i_L}{dt^2} = 0 \tag{5}$$

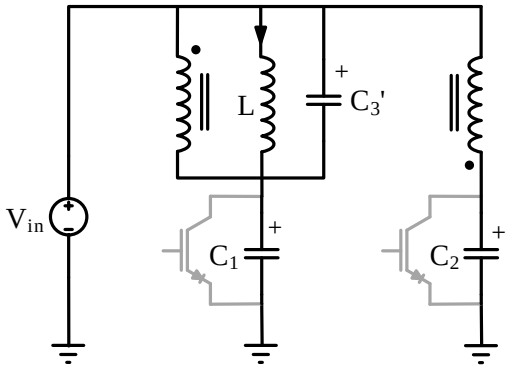


Figure 3 - Converter equivalent circuit during resonant modes [26].

$$v_L(t) = L\frac{di_L}{dt}, \tag{6}$$

where

$$C_{tot} = (C_1 + C_2 + N^2 C_3). \tag{7}$$

C_{tot} is the effective link capacitor measured from one of the primary windings. Equations (77) and (78) together with mode initial conditions $I_{m,0}$ and $V_{m,0}$ completely describe the link during resonant modes. According to (77) and (78), one can verify that the equivalent circuit of the converter during the resonant modes is reduced to a simple second-order LC circuit and that no current passes through the input source in resonant modes. The source voltage is not present in resonant equations. The link resonant frequency is defines as:

$$\omega_{res} = \frac{1}{\sqrt{LC_{tot}}}. \tag{8}$$

It bears mentioning that ω_{Link} is the frequency of the link current, and equals the switching frequency, and it is different than ω_{res}. From (77) and (78), the solution to link variables during resonant modes is:

$$\begin{cases} i_L(t) = I_{m,0}\cos(\omega_{res}t) + V_{m,0}\sqrt{\dfrac{C_{tot}}{L}}\sin(\omega_{res}t) & (9) \\ v_L(t) = -L\omega_{res}I_{m,0}\sin(\omega_{res}t) + V_{m,0}\cos(\omega_{res}t)\,. & (10) \end{cases}$$

Similar to mode 1, in modes 3 the link equations are:

$$\begin{cases} v_L(t) = -\dfrac{V_o}{N} - \dfrac{R_o}{N^2}i_L & (11) \\ i_L(t) = \dfrac{-V_oN}{R_o} + \left(I_{3,0} + \dfrac{V_oN}{R_o}\right).e^{-\frac{R_o}{N^2L}t}. & (12) \end{cases}$$

A set of five simultaneous equations (49-53) is to be solved. Unknowns are $I_{1,0}$, T_1, T_2, T_3, T_4. Variables $I_{2,0}$ and $I_{4,0}$ are functions of the unknowns and can be found from (44) and 48, respectively.

$$\begin{cases} \dfrac{I_{in.ref}}{2} = \dfrac{V_{in}}{R_{in}} T_1 + \dfrac{L}{R_{in}} \left(I_{1,0} - \dfrac{V_{in}}{R_{in}} \right) . \left(1 - e^{-\frac{R_{in}}{L} t} \right) & (13) \\ \dfrac{-V_o}{N} = -L\omega_{res} I_{2,0} \sin(\omega_{res} T_2) + V_{in} \cos(\omega_{res} T_2) & (14) \\ \dfrac{1}{2} \times \left(L I_{4,0}^2 + C_{tot} \dfrac{V_o^2}{N^2} \right) = E_{desired} & (15) \\ -V_{in} = -L\omega_{res} I_{4,0} \sin(\omega_{res} T_4) - \dfrac{V_o}{N} \cos(\omega_{res} T_4) & (16) \\ -I_{1,0} = I_{4,0} \cos(\omega_{res} T_4) - \dfrac{V_o}{N} \sin(\omega_{res} T_2) & (17) \end{cases}$$

Equations (49-53) are in order: current reference requirement at mode 1, voltage requirement at the end of mode 2, link energy requirement at the end of mode 3, voltage requirement at the end of mode 4, and current symmetry at start of mode 1 and end of mode 5.

Once a solution is obtained, the link peak current can be derived from (54).

$$\frac{1}{2} L i_{peak}^2 = \frac{1}{2} \times \left(C_{tot} V_{in}^2 + L I_{2,0}^2 \right) \quad (18)$$

2.1.3.2 Selection of Component Values

Using the set of equations developed above, a boost converter with V_{in}=100 V, V_o=200 V, nominal power of 350 W, and minimum switching frequency of $f_{Link,min}$=24 kHz is designed in this section. The transformer turn ratio is selected to be N=1 to demonstrate

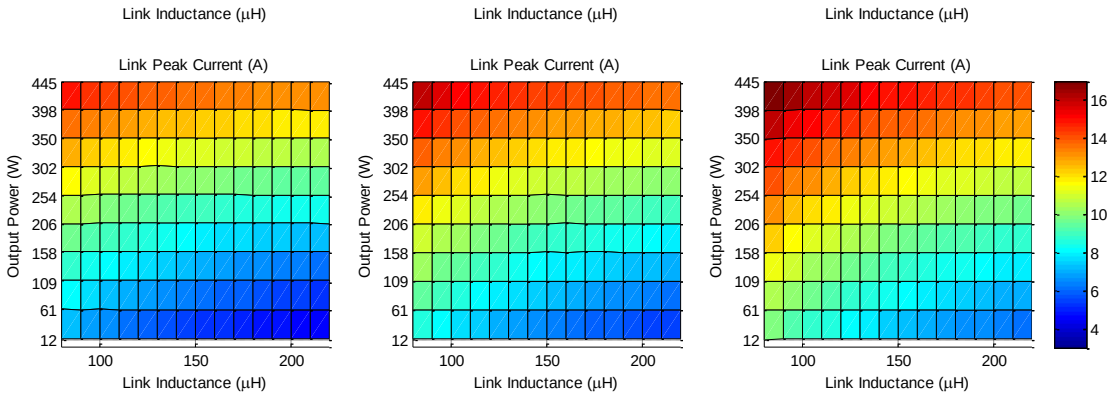
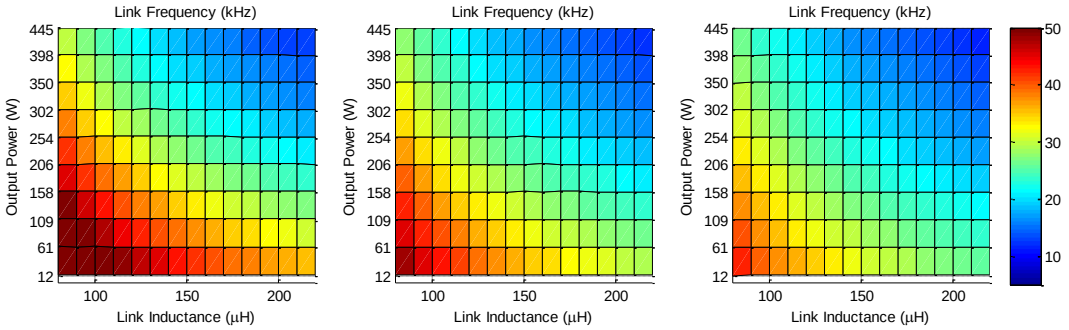


Figure 4 - Calculated peak current at V_{in}=100 V and V_o=200V for various values of link inductance, link equivalent capacitance and output power; a) C_{tot} = 90 μF; b) C_{tot} = 130 μF; c) C_{tot} = 170 μF [26].

the boost and buck capabilities of the converter. Figure 5 is a plot of link frequency f_{Link} as a function of link inductance L, link equivalent capacitance C_{tot}, and output power. The link frequency f_{Link} is the key variable of the converter mainly because it determines the sampling time of the digital controller, controls transformer core loss, and affects the design of terminal filters. Although the rated converter power is 350 W, Figure 5 presents the calculated variables for output powers of up to 445 W. An inspection of any of the three plots in Figure 5 reveals that the f_{Link} decreases as the output power increases.

This is expected because at fixed terminal voltages, as the output power rises the link inductor requires more time to charge and discharge. At power levels close to zero, the duration of the power transfer modes, i.e., odd-numbered modes approaches zero and the f_{Link} will almost be equal to the link resonant frequency f_{res}. Also, the three plots in Figure



(a) (b) (c)

Figure 5 - Calculated link frequency at V_{in}=100 V and V_o=200V for various values of link inductance, link equivalent capacitance and output power; a) C_{tot} = 90 μF; b) C_{tot} = 130 μF; c) C_{tot} = 170 μF [26].

5 indicate that the f_{Link} decreases as the link equivalent capacitor and link inductance increase. This is due the fact that the duration of resonant modes (even-numbered modes) depends directly on f_{res}, which is decided by the link parameters as in 37.

Figure 4 is a plot of link peak current I_{peak} as a function of link inductance L, link equivalent capacitance C_{tot}, and output power. Link peak current is important particularly due to the fact that it determines the maximum flux in the transformer core. According to Figure 4, I_{peak} increases as the output power rises. Also, smaller link capacitors result in smaller values for I_{peak} as suggested by (54). However, since the energy stored in the capacitors is much smaller than that of the inductor, the effect of C_{tot} on I_{peak} is not significant. Examination of any of the three plots in Figure 4 also reveals that I_{peak} is smaller when the link inductance is bigger.

The above discussion suggests that smaller values for link parameters L and C_{tot} are more favorable as they lead to smaller I_{peak} and higher f_{Link}. Specifically, higher switching

TABLE II. FOUR DESIGN CASES AND THEIR PEAK LINK CURRENT [26]

Case	L (μH)	C_{tot} (nF)	f_{Link} (kHz)	I_{peak} (A)
1	101	120	24.2	13.9
2	80	200	24.04	16.8
3	120	65	23.5	12.5
4	110	90	24.3	13.3

frequencies are welcome thanks to the soft-switching capability of the converter. Nonetheless too small values for L and C_{tot} necessitate a digital controller very high sampling frequency. Table II contains four design cases with almost the same link frequency that lead to different link peak currents. Case three results in the smallest link current and is considered superior to other designs.

2.1.4 Experimental Results

A hardware setup is fabricated to demonstrate the operation of the converter as shown in Figure 6. Transformer magnetizing inductance L and link equivalent capacitance C_{tot} are selected to be 101 μH and 120 nF, respectively. Turns ratio for the transformer is 1:1:1 to demonstrate the boost and buck capabilities of the converter. A larger than necessary core is intentionally used to construct the link so that a relatively large leakage inductance of 3.27 μH is achieved. This is done to show that the leakage inductance does not interfere with the operation of modes or the soft-switching of semiconductors. The rated power for this setup is 350 W. The TMS320F28335 Digital Controller by TI is used to implement the digital controller. A sampling time of 1μs on the digital controller result in about 40

Figure 6 - The experimental setup [26]

samples per link cycle, which is enough for practical implementation. The rest of this section presents the experimental results for boost and buck modes.

In the first experiment, the converter is operated in boost mode at an output power of 350 W with input and output voltages of 100 V and 200 V, respectively.

Figure 7 shows the link current, voltage, and their peak values. The measured link frequency is 23 kHz. From (49-53), the predicted values for V_{peak}=230 V are I_{peak}=13.9 A and f_{link}=24.2 kHz, which closely match the experimental measurements. Voltage and current waveforms for the input switch S_1 and output switch S_3 are depicted in Figure 7.

A 50 MHz Tektronix current probe is used to measure the switch currents. For both switches, the voltage is reduced to zero before the switches starts conducting, creating a ZVS condition and thereby eliminating the turn-on loss. At turn-off for both switches, the link capacitors limit the rate of rise of voltage on the switch, and keep the voltage close to

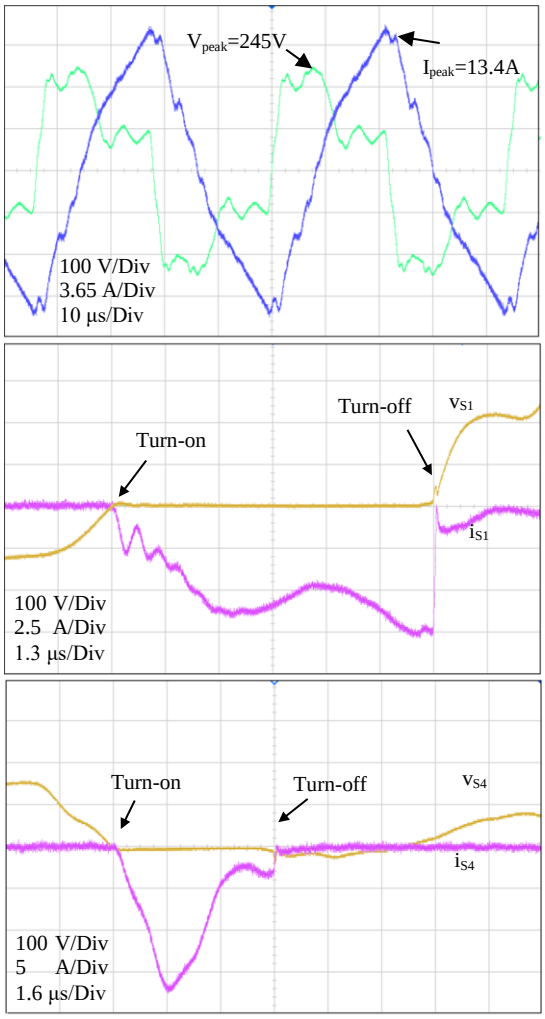


Figure 7 - Boost operation at 350 W ($V_{in}<V_o/N$); top: link waveforms; middle: input switch waveforms; bottom: output switch waveform [26]

zero. This effectively reduces the turn-off switching loss. The measured efficiency of the converter is 92.0%. The efficiency in this experimental setup is relatively low due to the fact that we have used 1200 V 45 A IGBTs that are significantly oversized for this voltage and current range. Specifically, the switch and diode conduction losses are needlessly

high. Future implementations of the converter should employ lower rating switches and diodes.

In the second experiment, the converter operates in buck mode at an output power of 75 W, with input and output voltages of 100 V and 48 V, respectively. Link waveforms

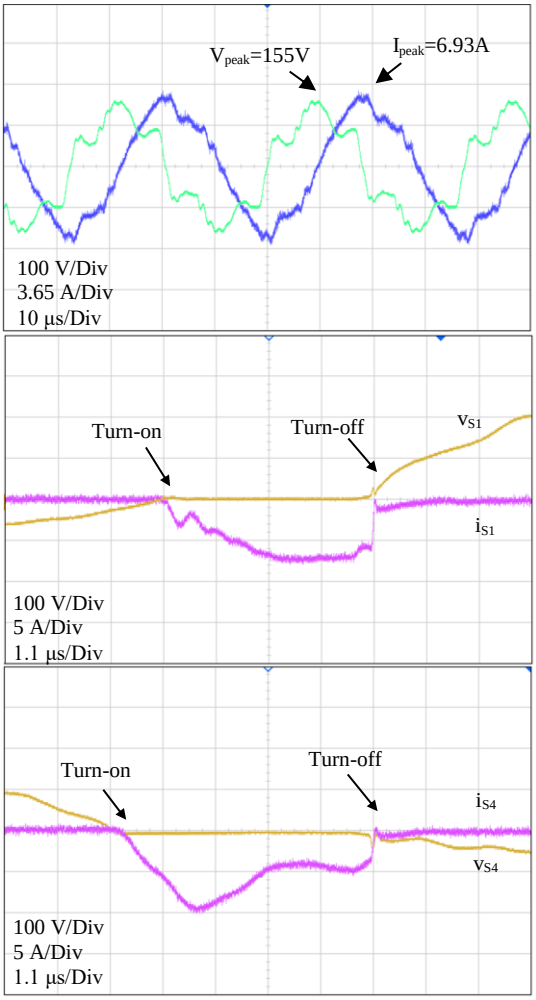


Figure 8 - Buck operation at 75 W (V_{in}>V_o/N); top: link waveforms; middle: input switch waveforms; bottom: output switch waveform [26].

are presented in Figure 8. Link peak values are labeled on the figure. The measured link frequency is 26.7 kHz. Predicted values from equations for V_{peak}= 145 V are I_{peak}=6.85 A and f_{link}=28.5 kHz, which are in good agreement with the experiment. Figure 8 depicts the input and output switch waveforms as well. Similar to the previous experimental test, the soft-switching conditions are achieved for both switches at turn-on and turn-off.

2.2 High Step-Up Flyback Converter[2]

2.2.1 Introduction

With the rapid increase in integration of renewable energy sources into the power grid, the need for electronic power converters is rising significantly. The dc output voltage of a solar panel is often collected and boosted by an electronic power converter. Fuel cells, batteries, and supercapacitors are other sources and storage elements that require a dc boost [12]-[15]. In grid-connected and stand-alone systems, a high boost factor is required when the output voltage of the source is relatively low, e.g., 50V. Uninterruptable Power Supplies (UPS) are another example of a system that requires a high boost factor. Regulated by local or national standards, the harvested power is to be galvanically isolated prior to grid injection. While this is mostly required for safety purposes, it brings along the advantage of mitigation of ground currents as well.

[2] © 2017 IEEE. Reprinted, with permission, from M. Moosavi and H. A. Toliyat, "A low-cost soft-switching high step-up flyback converter with stacked output cells," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017, pp. 1700-1705.

Because the output voltage of a high step-up converter is several times the input voltage, the input current is relatively high. When hard switching of the input semiconductor is involved, the leakage inductance of the transformer becomes a significant problem and often necessitates snubber circuitry that takes a toll on the conversion efficiency. The use of a transformer with a high turn ratio may escalate this problem further; however, this is not the case for soft-switching converters. Many high step-up topologies proposed in the literature use auxiliary circuitry to rob the semiconductors of the current and/or voltage during switching transitions, and therefore eliminate or significantly reduce the switching losses [16]-[23]. For instance, in [20] the isolated high step-up converter has a clamp circuit on the input side consisting of two auxiliary switches and two snubbing capacitors. The isolated converter of [21] uses two switches and two diodes on the input side to achieve soft-switching and recycle the leakage energy. On the output side, this converter boosts the voltage through two capacitors and two voltage-doubler diodes. An additional diode is also needed on the output side to prevent the discharge of output filter capacitor on the transformer. However, the reverse recovery of the diodes is not addressed clearly in that section. The isolated converter of [22] utilizes a voltage quadrupler to achieve a high voltage boost. Although this resonant converter provides soft-switching, it utilizes six active switches and four diodes. Moreover, the value of leakage inductance of this converter is a parameter that needs to be considered during the design of the transformer. A multiple output flyback converter with Zero Current Switching (ZCS) on the input switch and reduced reverse recovery loss on the output diodes is presented in [23]. The

converter requires an additional winding and switch to facilitate the extended quasi-resonant period, a method used to reduce switching loss and switch stress.

A Zero Voltage Switching (ZVS) converter with a parallel LC link is proposed in [24]. Although this converter is ac-ac, similar link waveforms can be used in dc-dc conversion as well. A class of universal (ac-ac and dc-dc) isolated converters with an ac link was invented in [9]. These soft-switching converters achieve ZVS and effectively suppress the diode turn-off transients. In [10],[26], and [11] several dc-dc converters with a partial resonant LC link are proposed. Although the converters can amplify the input voltage, they cannot be considered high step-up converters since the lengthy resonant modes will degrade their performance in terms of efficiency, switching frequency, and voltage stress on the input switch.

The high step-up partial-resonant isolated dc-dc converter proposed in this section has a parallel *LC* link, and uses only one low-side switch and no auxiliary switches or windings [27]. This makes the control and implementation of the converter straight-forward and reduces the overall cost of the converter. A high boost factor is achieved by charging and discharging the magnetizing inductance of a transformer. Also, due to the fact that the output cells of the converter are connected in series, the output voltage can be increased furthermore without imposing voltage stress on the input or output semiconductors. The input switch is turned on and off at ZVS, and the output diodes are turned off without reverse recovery losses. The input and output leakage inductances of the windings do not create voltage spikes on the switch because of the capacitors that are connected in parallel to the windings. The leakage inductances do not play a role in power conversion, and their

values do not affect the operation or voltage gain of the converter. Unlike a conventional multiple-winding flyback converter power, sharing among the output cells is provided inherently, even when the leakage inductances of the output windings are considerably different. This makes the converter robust to transformer non-idealities and reduces the transformer fabrication costs. The rest of this section explains the topology and its operation, provides an analytical approach to converter's operation, and presents the experimental results.

2.2.2 The Proposed Converter

2.2.2.1 The Topology

Figure 9 depicts the proposed partial-resonant dc-dc converter with K output cells ($K \geq 1$). The transformer has a total of $K+1$ windings and a turn ratio of $1:N$. The capacitors C_0 to C_K together with the magnetizing inductance L form a parallel resonant link, hereinafter referred to as the link. The link capacitors as referred to the primary side and added together, are named C_{tot}. Also, the voltage and current through the inductor are hereafter referred to as the *link voltage* (v_L) and *link current* (i_L), respectively. The input switch S_0 conducts unidirectional current. However, it should be able to block voltages of both polarities. This can be achieved by using a reverse-blocking switch or simply by putting a

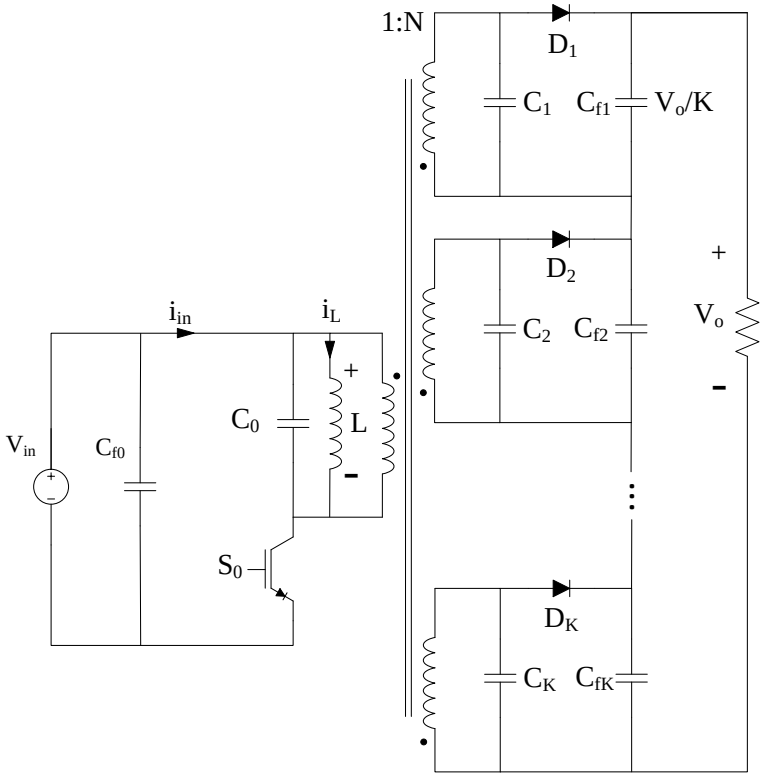


Figure 9 - The proposed converter [27].

diode in series with the switches. Each output module is connected to an output filter denoted by C_{fk}, $1 \leq k \leq K$.

2.2.2.2 The Modes of Operation

A link cycle T_{Link} is comprised of four modes as shown in Figure 10. They cycle begins by delivering power to the link inductor in Mode 1, then the link resonates in Mode 2, and in Mode 3 the power is delivered to the output. Mode 4 is a resonant mode similar to Mode 2. Since the total output voltage is V_o, the output voltage of each cell is V_o/K.

Mode 1: The link inductor L is charged by the source through S_0 as shown in Figure 10. The link current i_L increases almost linearly in this mode. All diodes are reverse biased in this mode. Once the input current reference $I_{in,ref}$ is met, S_0 is gated off. Due to the fact that prior to switch turn-off the capacitors C_{f0} and C_0 have the same voltage, the rate of voltage rise on S_0 at turn-off is limited. This allows the switch current to decrease while the switch voltage is still zero, and significantly decreases the switching loss.

Mode 2: All diodes are still in their blocking state and the switch is off. With the energy that was delivered to the link in Mode 1, the link resonates. During resonance in Mode 2, the link voltage v_L changes polarity and becomes negative. At the zero-crossing of the link voltage, the link current has its positive peak value, I_{peak+}, as shown in Figure 10. This mode continues until the reflected link voltage Nv_L reaches the cell output voltage V_o/K in magnitude. At this point, the output diodes D_1 through D_K become forward biased softly and start conducting.

Mode 3: The link inductor is connected to the load via diodes D_1 through D_K, each carrying the current i_L/NK. The link current reduces almost linearly while its energy is being transferred to the output filters. This mode continues until the link inductor completely discharges to the output filters and both the diode currents and i_L naturally reduce to zero. On each output cell, because C_k and $C_{fo,k}$ have the same voltage, the blocking voltage on D_k rises slowly. The natural decay of the diode current to zero and the slow voltage rise almost entirely eliminate the reverse recovery transients and losses, and increase the conversion efficiency.

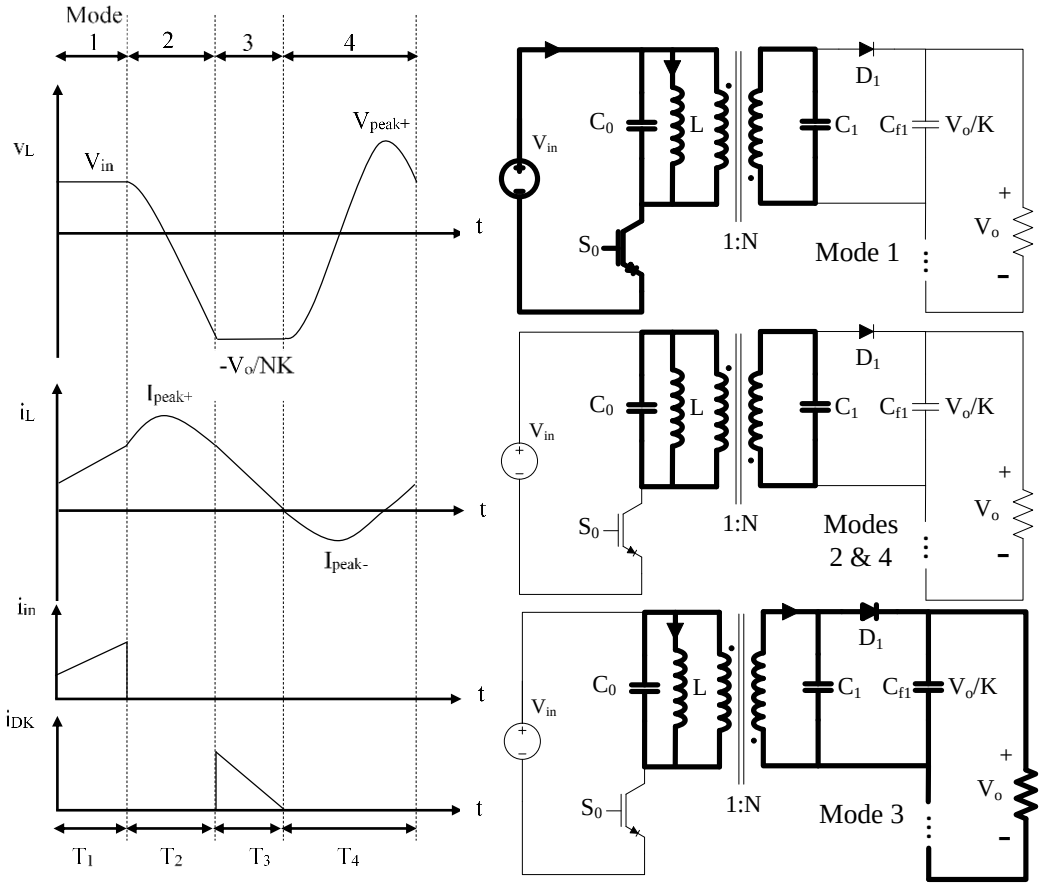


Figure 10 - Converter waveforms and main current paths in each mode [27].

Mode 4: All diodes are in their blocking state and the switch is off. Since the link voltage at the end of Mode 3 is a non-zero value, there is still energy stored in the link so it can resonate. As shown in Figure 10, v_L crosses zero in this mode and becomes positive, causing i_L to have its negative peak I_{peak-}. The negative peak value is much smaller than the positive, because the total energy stored in the link in Mode 4 is smaller than that of Mode 2. This mode continues until the link voltage reaches the input voltage V_{in}. At this moment, the voltage on the switch S_0 is zero, and it can turn on at ZVS. This elimintes the

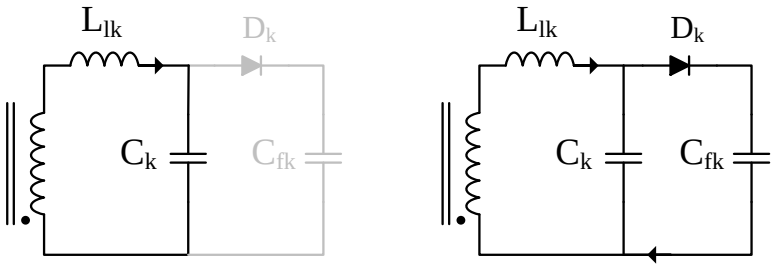
switching loss almost entirely. To elaborate further, prior to the moment when the switch starts conducting, it is reverse biased and cannot conduct even if it is gated on. Therefore the controller can send an early gate signal to the swith without having an unwanted early conduction. This makes the implementation of the contoller very simple by removing the need for synchronizing the switch gate signal with link voltage.

According to the above paragraphs, the resonant modes are even-numbered, and the energy transfer modes are odd-numbered. There is a resonant mode between every two energy transfer modes. However, a conventional flyback converter does not have such resonant modes and directly switches from a charge mode into a discharge mode and/or vice versa. The resonant modes provide ZVS conditions for all turn-on and turn-off transitions, and do not take part in transferring energy between terminals. Therefore, it is recommended to minimize the duration of such modes by selecting small link components. This will be explained in more details in section 2.1.3.

2.2.2.3 Inherent Power Balancing Among Cells

Usually when a converter is constructed of several cells or modules that are connected in series or parallel, balancing the power processed by them becomes an issue due to second order factors such as gate signal propagation delays, component manufacturing discrepancies, or stray inductances and capacitances [26][28][29]. For example, in a conventional flyback converter with more than two output windings, it is very likely that the leakage inductances of the output windings are unequal. Since the output diode of a cell is connected in series to its winding leakage inductance, the amount of current that flows through the diode to the output is directly affected by the leakage inductance. This

stray effect disturbs the load regulation of a multiple-output flyback converter by the cells with a smaller leakage to process more power that other cells [29]. To elaborate further, in a conventional flyback converter the output diodes have to conduct immediately after the input switch is turned off so that the continuity of the magnetizing current is maintained. This rapid rise in the diode current is opposed by the winding inductance. However, this is not the case for the proposed multiple-winding converter due to the presence of the link capacitors between the diodes and the leakage inductances. In this converter, the diodes do not conduct immediately after the input switch is turned off. Instead, there is a resonant period, i.e., Mode 2, placed between the charge and discharge modes in which the leakage inductances can be pre-charged by the magnetizing current as shown in Figure 11. In Mode 2, the leakage current in the cells are almost equal because they are based on the link capacitors and not on the leakage inductances. This is because the impedances of the link capacitors are much greater than the impedances of the leakage inductances.



(a) Mode 2 (b) Mode 3

Figure 11 - Simplified circuit diagram of an output cell in Modes 2 and 3 [27].

2.2.3 Analysis and Design

2.2.3.1 Derivation of Converter Equations

This section aims to establish an analytical approach to the converter's operation. Especially, the relations between link inductance, link capacitance, transformer turn ratio, link frequency, and link peak current are derived. Results of this section can be used design the converter. The following assumptions are made during this analysis:

- In power transfer modes (odd-numbered modes), the winding resistances are included in the equations. However, because the link capacitor voltages change only slightly in these modes as shown in Figure 10, the capacitor currents are negligible and will be ignored.
- In resonant modes (even-numbered modes), winding resistances are not factored in. The reason for this is that during resonant periods, the impedance of link capacitors is higher than the winding resistances by a factor of 100 or more.
- It is assumed that the filter capacitors are ripple-free.
- Voltage drops on the switch and diodes are neglected.
- Variable t is the time passed since the start of the mode under study. Also, $I_{m,0}$ and $V_{m,0}$ denote the link initial conditions at the start of Mode m.

According to Figure 10, a link cycle is:

$$T_{Link} = \frac{2\pi}{\omega_{Link}} = T_1 + T_2 + T_3 + T_4. \tag{19}$$

In Mode 1 the link inductor is charged by the source. Since the link capacitors are ignored, the link equivalent circuit in this mode reduces to an *RL* circuit. Letting R_{in} denote the input winding resistance, the solution to this circuit is:

$$\begin{cases} v_L(t) = V_{in} - R_{in} i_L & (20) \\ i_L(t) = \dfrac{V_{in}}{R_{in}} + \left(I_{1,0} - \dfrac{V_{in}}{R_{in}}\right).e^{-\frac{R_{in}}{L}t} & (21) \end{cases}$$

In resonant Modes 2 and 4, none of the semiconductor devices carry current as shown in Figure 10. Since the winding resistances are ignored in these modes, all link capacitors are connected in parallel to the link inductor. This reduces the link to a second order *LC* circuit that resonates, therefore the link equations are:

$$i_L + C_{tot} L \frac{d^2 i_L}{dt^2} = 0, \tag{22}$$

$$v_L(t) = L \frac{di_L}{dt}, \tag{23}$$

where

$$C_{tot} = C_0 + N^2 \sum_{k=1}^{K} C_k \,. \tag{24}$$

C_{tot} is the total link capacitor as measured at the input winding. The link resonance frequency is readily defines as:

$$\omega_{res} = \frac{1}{\sqrt{LC_{tot}}}. \tag{25}$$

It should be noted that $\omega_{Link} = 2\pi f_{Link}$ is the frequency of the link current, and equals the switching frequency. Moreover, ω_{Link} it is different than ω_{res}. From (22) and (23), the solution to link circuit during resonant modes is:

$$\begin{cases} i_L(t) = I_{m,0}\cos(\omega_{res}t) + V_{m,0}\sqrt{\dfrac{C_{tot}}{L}}\sin(\omega_{res}t) & (26) \\ v_L(t) = -L\omega_{res}I_{m,0}\sin(\omega_{res}t) + V_{m,0}\cos(\omega_{res}t)\,. & (27) \end{cases}$$

Similar to Mode 1, the link in Modes 3 reduces to an *RL* circuit because the link capacitors are ignored. The link equations are:

$$\begin{cases} v_L(t) = -\dfrac{V_o}{N} - \dfrac{R_o}{N^2}\,i_L & (28) \\ i_L(t) = -\dfrac{V_o N}{R_o} + \left(I_{3,0} + \dfrac{V_o N}{R_o}\right).e^{-\frac{R_o}{N^2 L}t}. & (29) \end{cases}$$

Equations (20, 21, 26-29) describe all four modes of a link cycle. In order to find the duration of each mode it is required to use these equations along with the definition of the modes that was presented in an earlier is section. This leads to a set of five equations given by (12-16). Unknowns are $I_{1,0}$, T_1, T_2, T_3, T_4.

$$\begin{cases} \dfrac{I_{in.ref}}{f_{Link}} = \dfrac{V_{in}}{R_{in}}T_1 + \dfrac{L}{R_{in}}\left(I_{1,0} - \dfrac{V_{in}}{R_{in}}\right)\left(1 - e^{-\frac{R_{in}}{L}T_1}\right) & (30) \\ \dfrac{-V_o}{N} = -L\omega_{res}I_{2,0}\sin(\omega_{res}T_2) + V_{in}\cos(\omega_{res}T_2) & (31) \\ 0 = \dfrac{V_o}{R_o}NK + \left(I_{3,0} + \dfrac{V_o}{R_o}NK\right)e^{-\frac{R_o}{LN^2K}T_3} & (32) \\ -V_{in} = -L\omega_{res}I_{4,0}\sin(\omega_{res}T_4) - \dfrac{V_o}{N}\cos(\omega_{res}T_4) & (33) \\ -I_{1,0} = I_{4,0}\cos(\omega_{res}T_4) - \dfrac{V_o}{N}\sin(\omega_{res}T_2) & (34) \end{cases}$$

Equation (30) is the current reference requirement at the end of Mode 1. Equations (31,33) are the link voltage requirements at the end of Modes 2 and 4, respectively.

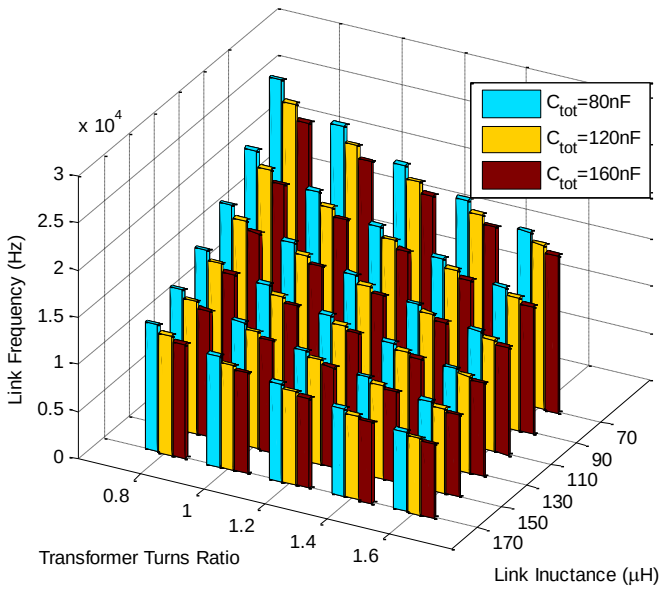


Figure 12 - Link frequency for various converter parameters at 250 W [27].

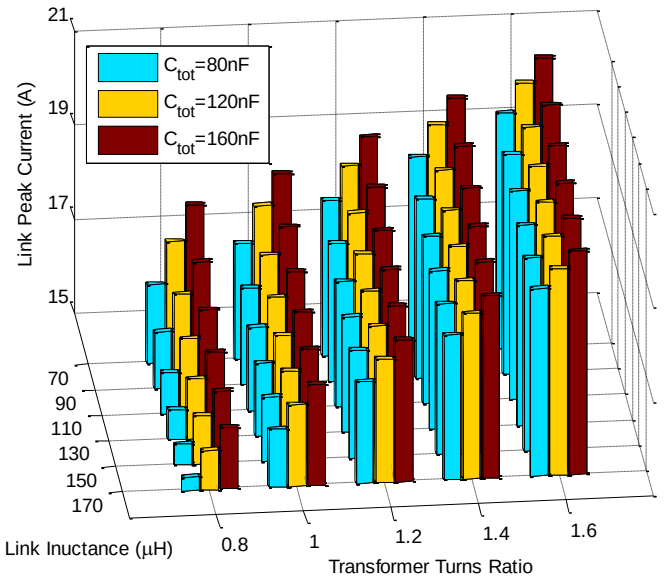


Figure 13 - Link peak current for various converter parameters at 250 W [27].

Equation (32) denotes that the link current should be zero at the end of Mode 3. Finally, (34) is the current symmetry requirement at the end of Mode 4, i.e.; $I_{5,0} = -I_{1,0}$.

Once a solution is obtained, the link and switch peak current can also be derived from (35).

$$\frac{1}{2}Li_{peak+}^2 = \frac{1}{2} \times \left(C_{tot}V_{in}^2 + LI_{2,0}^2\right) \tag{35}$$

2.2.3.2 Selection of Component Values

Using the set of equations developed above, a high step-up boost converter with V_{in} = 60 V, V_o = 600 V, and nominal power of 250 W is designed in this section.

Figure 12 is a plot of link frequency f_{Link} as a function of link inductance L, link equivalent capacitance C_{tot}, and transformer turn ratio N at 250 W. The link frequency f_{Link}

is the key variable of the converter, primarily because it determines the sampling time of the digital controller, controls transformer core loss, and affects the design of terminal filters. The figure indicates that f_{Link} decreases as the link equivalent capacitor and link inductance increase. This is due the fact that the duration of resonant modes (even-numbered modes) depends directly on the link natural frequency ω_{res}, which is decided by the link parameters.

Figure 13 is a plot of the link's positive peak current I_{peak+} as a function of L, C_{tot}, and N. The link peak current is important because it determines the maximum flux in the transformer core. According to the figure, smaller link capacitors result in smaller values for I_{peak+}. However, since the energy stored in the capacitors is much smaller than the inductor, the effect of C_{tot} on I_{peak+} is not as significant as that of L. Examination of any of the three plots in Figure 13 also reveals that I_{peak} is smaller when the link inductance is higher.

The above discussion suggests that smaller values for link parameters L and C_{tot} are more favorable as they lead to a higher f_{Link}. Specifically, higher switching frequencies are encouraged due to the soft-switching capability of the converter. Nonetheless, excessively small values for L and C_{tot} necessitate a digital controller with a very high sampling frequency.

2.2.4 Experimental Results

A hardware setup is constructed to demonstrate the operation of the converter as shown in Figure 15. The TMS320F28335 Digital Signal Controller by TI is used to implement the digital controller. Transformer magnetizing inductance, L, and the link total

Figure 15 - The high step-up converter [27].

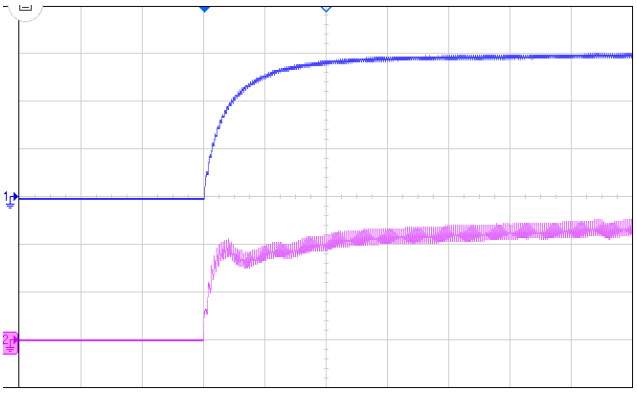


Figure 14 - Converter start-up; Top: (200V/div) output voltage; Bottom: (2 A/div) filtered input current (2ms/div) [27].

capacitance, C_{tot}, are selected to be 110 μH and 120 nF, respectively. Turn ratio of the seven-winding transformer is chosen to be $N=1$ to demonstrate the boost capability of an individual cell. All experiments of this section are performed at an output power of 250 W with V_{in} = 60 V and V_o = 600 V. Among of the six output windings, the largest and smallest total leakage inductances as measured from the primary side are 5 and 2.82 μH,

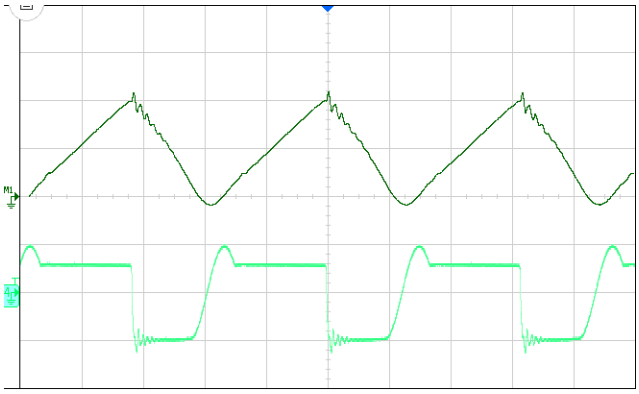


Figure 16 - Link waveforms at 250 W; Top: (8.25 A/div) link current; bottom: (100 V/div) link voltage (20 μs/div) [27].

respectively. Although the leakage inductances are relatively large and unequal, they do not interfere with the soft-switching of the semiconductors. The output voltage of the cells are between 98 and 103 V. The link voltage and current are depicted in Figure 16. Measured values for f_{Link} and I_{peak+} are 15.9 kHz and 18.1 A, respectively. Values derived from (12-16) for the same operating point are 16 kHz and 17.39 A. Measured efficiency is recoded as 93%.

Figure 14 shows the output voltage and input current of the converter at start-up under open-loop control (fixed input current reference). The input switch current and voltage are depicted in Figure 17. Prior to the conduction, the voltage on the switch S_0 decays to zero to provide a ZVS condition. Similarly, the rate of rise of voltage on S_0 is limited by the link capacitors, thereby reducing the turn-off losses significantly. The current and voltage on one of the output diodes is reported in Figure 18. Slightly before the diodes starts conducting, the diode voltages drop to zero (Mode 2). This facilitates soft turn-on of the diodes. During their conduction, the diodes discharge the link current slowly to zero to

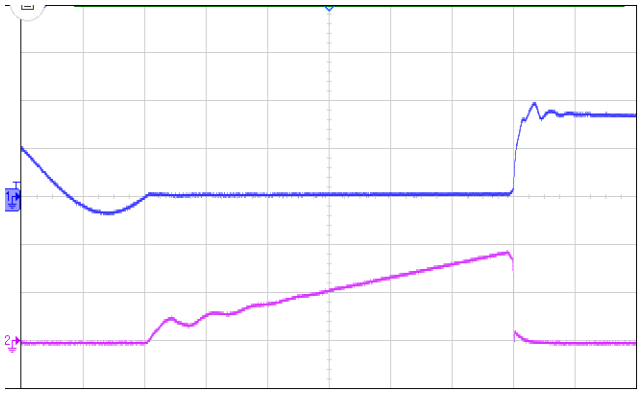


Figure 17 - Input switch waveforms; Top: (100 V/div) switch voltage; Bottom: (10 A/div) switch current (5µs/div) [27].

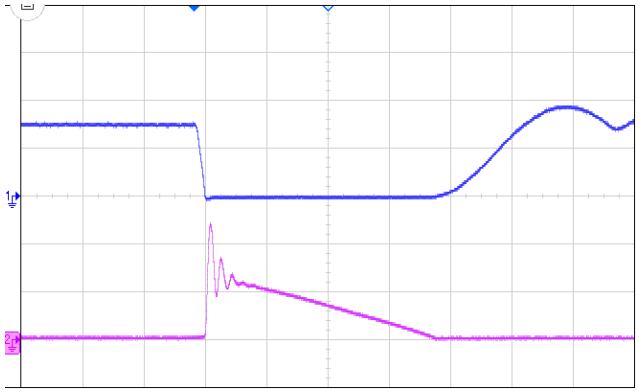


Figure 18 - Output diode waveforms; Top: (50 V/div) diode voltage; Bottom: (2 A/div) diode current (5µs/div) [27].

suppress the reverse-recovery losses. After their turn-off, the voltage on the diodes starts increasing slowly.

2.3 Conclusion

This chapter proposed two isolated soft-switching DC-DC converter. Initially, a partial resonant push-pull buck-boost converter with galvanic isolation is proposed. Soft-switching is achieved at all operating points. The converter benefits from ZVS for all

semiconductor devices at turn-on. Also, soft-switching is achieved at turn-off by limiting the rate of rise of voltage for all switches. The converter is comprised of an inductive-capacitive ac link, which eliminates the need for any bulky electrolytic capacitor. The double-ended converter utilizes the magnetizing inductance of the transformer as a resonant inductor. Voltages and magnetizing current into the transformer are free of any dc component, allowing the topology to utilize the magnetic core in both positive and negative half cycles. Equations governing the operation of the converter were derived. From the equations, the important variables of the converter, i.e., the link frequency and peak current, are obtained. Using an analytical approach, proper values for link inductance and capacitance were selected, leading to a desired switching frequency. Empirical results were in good agreement with the analyses. It was shown experimentally that soft-switching is maintained even when the leakage inductance of the transformer is large.

The second topology proposed in this chapter is an isolated high step-up converter. The high output voltage is made by using a cascaded structure of output cells. Advantages of the proposed converter include soft recovery of the diodes, soft-switching of the input switch at turn-on and turn-off transitions, inherent power balancing among the cells, and robustness to transformer non-ideality. Also, the converter does not required any auxiliary circuitry to achieve soft-switching. The design and operation of the converter was studied analytically to provide a basis for parameter selection.

3 DC-AC TOPOLOGIES

3.1 Double-Ended Inverter[3]

3.1.1 Introduction

The current market trend and the new global and national energy roadmaps significantly foresee the integration of renewable sources of energy in small and large power systems. The world total Photovoltaic (PV) capacity was estimated to be 134 GWp in 2013 [31]. As the production costs are decreasing, solar panels are being vastly integrated in power systems through power electronic inverters. Regardless of series or parallel connection of the solar panels, their dc voltage often needs to be amplified to meet the ac-side voltage levels. In multi-stage PV inverters, a boost type dc-dc stage provides this amplification, and an inverter stage carries out the dc-ac conversion. In single-stage inverters, the amplification and conversion take place in a single step, potentially allowing for a smaller inverter footprint and a higher efficiency [32][33]. Some single-stage configurations, on the other hand, eliminate the need for voltage amplification by serially connecting several PV panels to achieve a large enough dc voltage [34]. Although such configurations require a small number of switches, they are prone to power degradation in case of partial shading [35]. Depending on the grounding and isolation requirements, PV inverters may need to be galvanically isolated. Inverters with a built-in high-frequency transformer are

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considered advantageous over conventional line-frequency isolation methods on grounds of cost, size, and volume.

Since efficiency is a major concern in the design of PV inverters, soft-switching techniques based on resonance or partial resonance of an LC network have received a great amount of attention in the past decades [35][37]. Such techniques often reduce or virtually eliminate the switching losses by creating a ripple in the waveforms to obtain a Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS) at the switching instance [38]. The implementation of the LC network may require additional circuitry that increases control complexities. For example, the flyback inverters of [39][40][41] use an active clamp consisting of a capacitor and an additional switch to achieve soft-switching, and the multilevel inverter of [42] requires a coupled inductor and four auxiliary switches. Auxiliary Resonant Commutated Pole (ARCP) is another method of creating soft-switching conditions that adds to the complexity of control and modulation [43]. There have also been partial resonant inverters and converters that do not need auxiliary components such as the parallel partial resonant converter proposed in [9][24][26][44][45], bus these inverters require switches with a relatively large voltage rating. A high step-up push-pull inverter for PV applications is presented in [7] that offers soft-switching in a wide range of input voltage and power. But it is not scalable to higher voltage or power levels. The single-phase grid-connected inverter incorporating a high-frequency transformer in [46] can achieve soft-switching for some of its switches, but it is composed of a Dual Active Bridge (DAB) dc-dc stage, an intermediate dc bus, and a dc-ac stage. While such a configuration takes advantage of the transformer leakage

inductance to eliminate the need for a snubber, it requires three full bridges. A three-phase inverter based on DAB is proposed in [47]. This LLC converter can obtain soft-switching in a certain range, but no prospects for scalability or modularity are claimed.

Other than the need for extra components, the switches of a (partial) resonant inverter may experience additional voltage or current stress due to the resonance of the LC network [48]. This often calls for utilization of semiconductor devices with higher ratings. Particularly, if the inverter operates at high terminal voltages, MOSFETs may need to be replaced by IGBTs that have a higher on-state resistance (Rds,on) and longer switching intervals. Since stacked and multi-cell inverters are capable of synthesizing a high terminal voltage by using only standard low-voltage devices [49], the idea of having a soft-switching multi-cell inverter/converter has been intriguing to a number of researchers [48][50][51][52][57]; which is the focus of this section as well.

This section proposes a non-scalable and scalable variants of a three-phase isolated PV inverter with stacked H-bridge cells, as illustrated in Figure 19 and Figure 20. Isolation is provided through one or more high-frequency, multiple-winding transformers. The difference between the non-scalable and scalable embodiments is that the former uses one central transformer that feeds all cells, whereas the latter uses several transformers. Each transformer winding is connected in parallel to a small ac capacitor to achieve a ZVS at turn-on and a near-ZVS condition at turn-off of all switches. No auxiliary circuitry is required to achieve soft-switching. The magnetizing inductance of the transformer(s) and the winding capacitors make a parallel ac link that replaces the electrolytic dc link of conventional inverters. The proposed inverter is inherently buck-boost and can achieve a

high voltage gain using only standard low-voltage semiconductors and without relying on transformer turn ratio. Unlike the DAB-based topologies, there is no intermediate dc bus present in this inverter. No measures are needed to maintain the voltage and current balance among the cells. Soft-switching is achieved throughout the range of operation. The rest of this section explains the operation of the inverters, offers a design method, and demonstrates the performance of a 750 W prototype.

3.1.1.1 The Proposed Topologies

The schematics diagrams of the two variations of the proposed cascaded soft-switching inverter are depicted in Figure 19 and Figure 20. Each output phase is composed of K serially-connected H-bridge cells. The very first cell of the phases meet at the neutral point, n. In the single-transformer embodiment of Figure 19, one transformer with $3K+1$ windings provides the galvanic isolation, whereas in the scalable multiple-transformer embodiment of Figure 20, a total of K four-winding transformers provide the isolation. The input winding of all transformers are connected in parallel. The operation and control of the converter is identical in both embodiments. The descriptions hereinafter apply to both embodiments unless otherwise mentioned. Let us use the symbol $x \in \{i, A, B, C\}$ to refer to the input stage, phase A, phase B, and phase C, respectively. The transformer turn ratio is $1:N$, i.e.; an output winding has N times the number of turns of an input winding.

In reference to Figure 19 and Figure 20, each transformer winding is connected in parallel to an ac capacitor, C_{xk}, $k \in \{1,2,\ldots,K\}$, which has a small capacitance (see Table IV). The magnetizing inductance of a transformer as referred to the input stage is denoted by L_k. When the winding non-idealities are ignored, the magnetizing inductance(s) and ac

capacitors are connected in parallel and form a second- order *LC link* that is referred to as *the link* throughout this section. The *total link inductance* for the single-transformer and multiple-transformer embodiments are $L_{tot} = L_1$, and $L_{tot} = L_1 \| L_2 \| \ldots \| L_K$, respectively. The voltage on the link inductor(s) is hereinafter referred to as the *link voltage*, v_L, and the summation of magnetizing current(s) is referred to as the *link current*, i_L. Assuming the value of C_{i1} for all input link capacitors, and C_{A1} for all output link capacitors, the *total link capacitance* is:

$$\begin{cases} C_{tot} = C_{i1} + 3KN^2 C_{A1}, & \textit{Single-transformer} \\ C_{tot} = KC_{i1} + 3KN^2 C_{A1}, & \textit{Multiple-transformer embodiment}. \end{cases} \tag{36}$$

In Figure 19 and Figure 20, switches that have the same name receive the same gate signal. The link inductor, L_{tot}, which is the main energy transfer element, is connected to the dc source through the input H-bridge cell. The input switches S_{i+} and S_{i-} conduct current in one direction only; however, they should be capable of blocking positive and negative voltages. For example, a reverse blocking IGBT or an IGBT/MOSFET in series with a diode can be used. On the other hand, the output switches S_{x+} and S_{x-}, $x \in \{A, B, C\}$, are four-quadrant semiconductors. Depending on the design requirements, the inverter may need capacitive or inductive-capacitive filters on its input and output terminals as shown in Figure 19 and Figure 20. When using an inductive-capacitive filter, the filter capacitors should face the inverter. As labeled in Figure 19 and Figure 20, the unfiltered terminal currents are denoted by $\{i_i, i_A, i_B, i_C\}$, and the filtered currents are denoted by $\{i_{if}, i_{Af}, i_{Bf}, i_{Cf}\}$.

3.1.1.2 Operation Principle and Soft-Switching

As stated before, the total link inductance, L_{tot}, and capacitance, C_{tot}, make a parallel link that partially resonates during a link cycle. A full link cycle, $T_{Link}=1/f_{Link}$, is made up

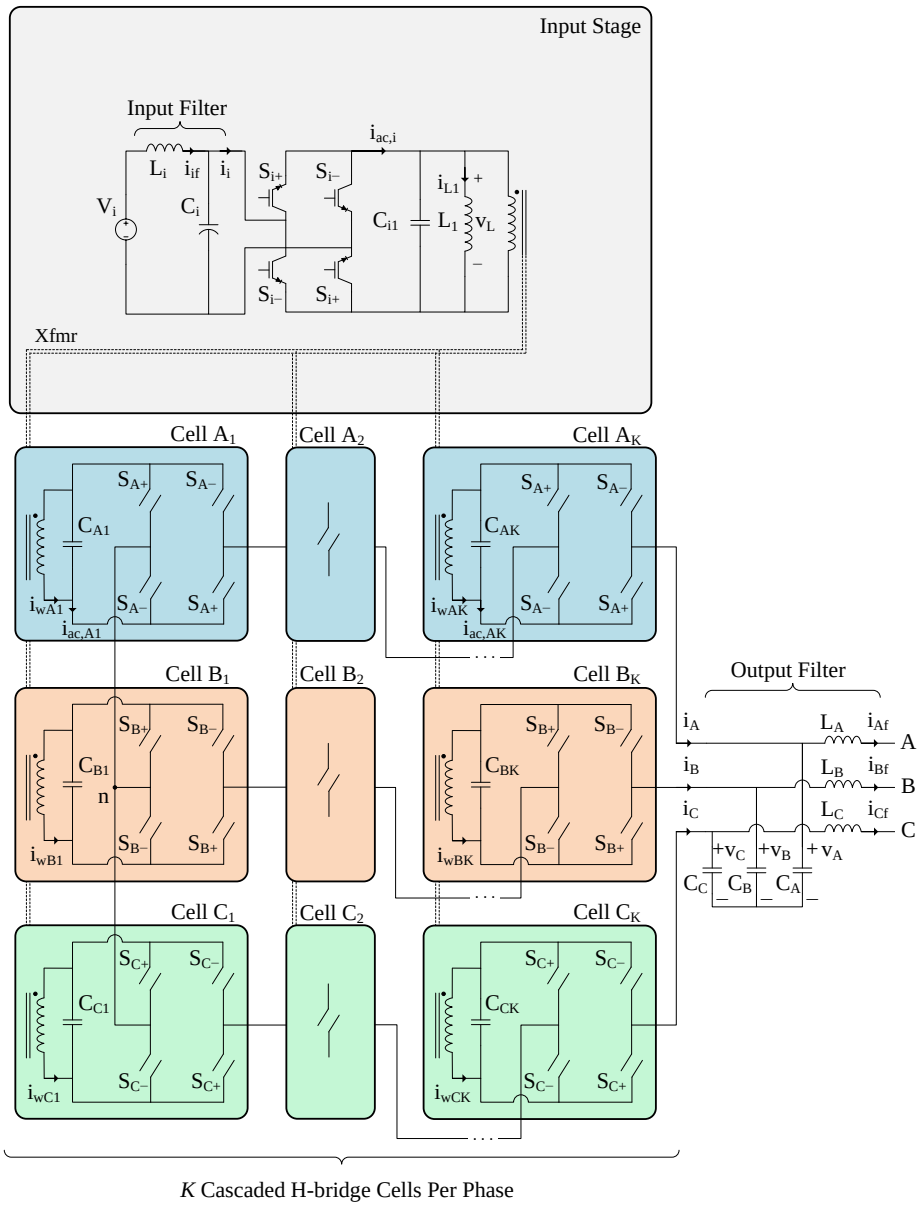


Figure 19 - The proposed single-transformer embodiment having K transformers. Each output phase is composed of *K* cascaded H-bridge cells.

of twelve modes as labeled in Figure 21, and f_{Link} is much higher than the inverter line frequency. The link receives energy from the dc source in Modes 1 and 7, and delivers the

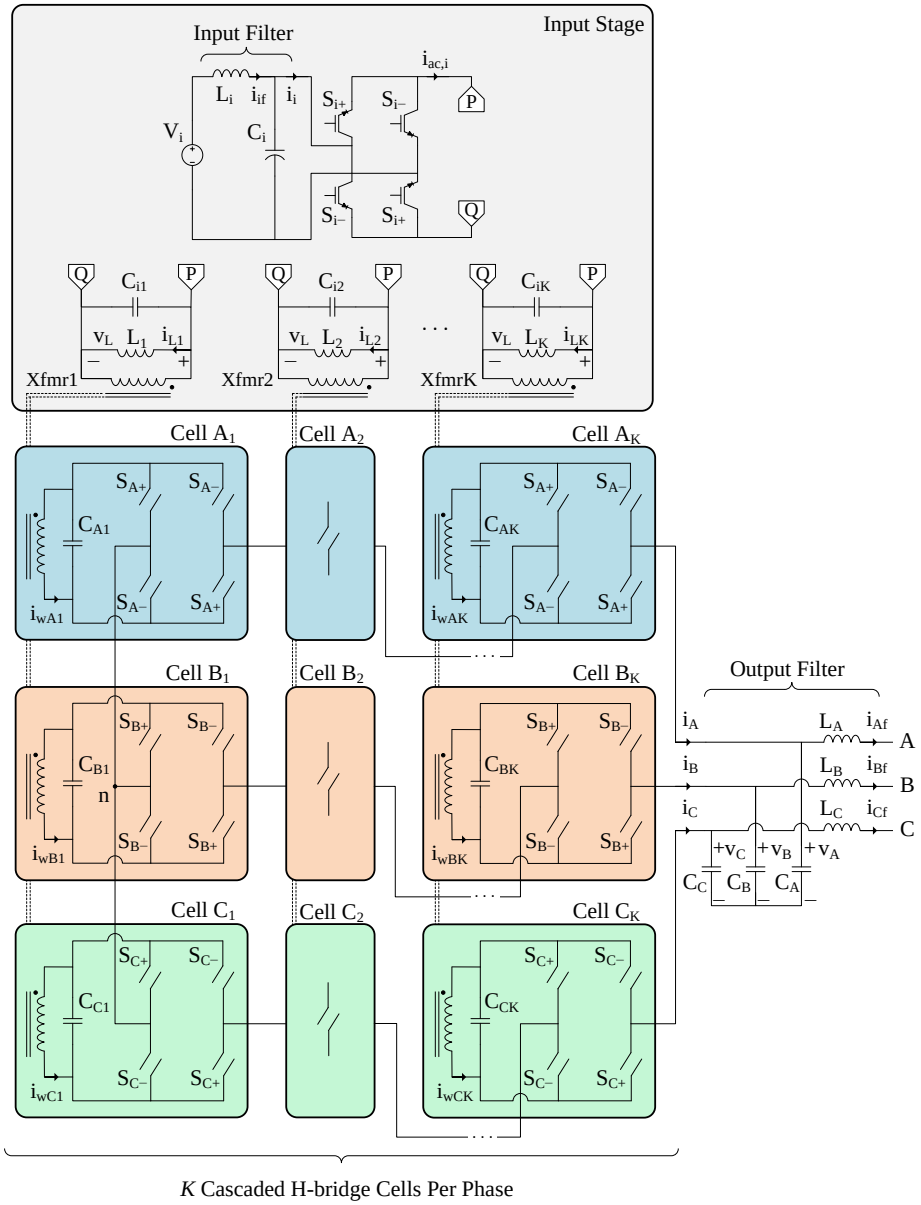


Figure 20 - The proposed scalable multiple-transformer embodiment having K transformers. Each output phase is composed of *K* cascaded H-bridge cells.

energy to the output in Modes 3, 5, 9, and 11. The even-numbered Modes 2, 4, 6, 8, 10, and 12 are short resonant modes that provide soft-switching conditions and do not take

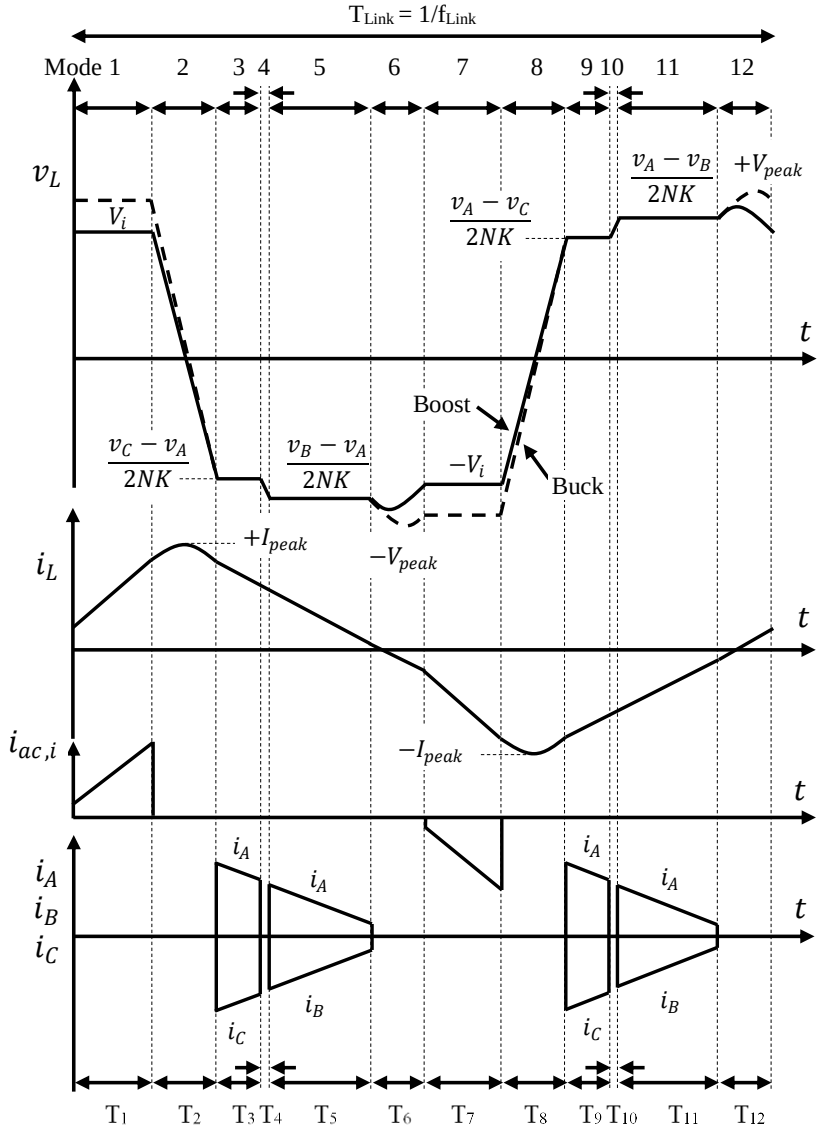
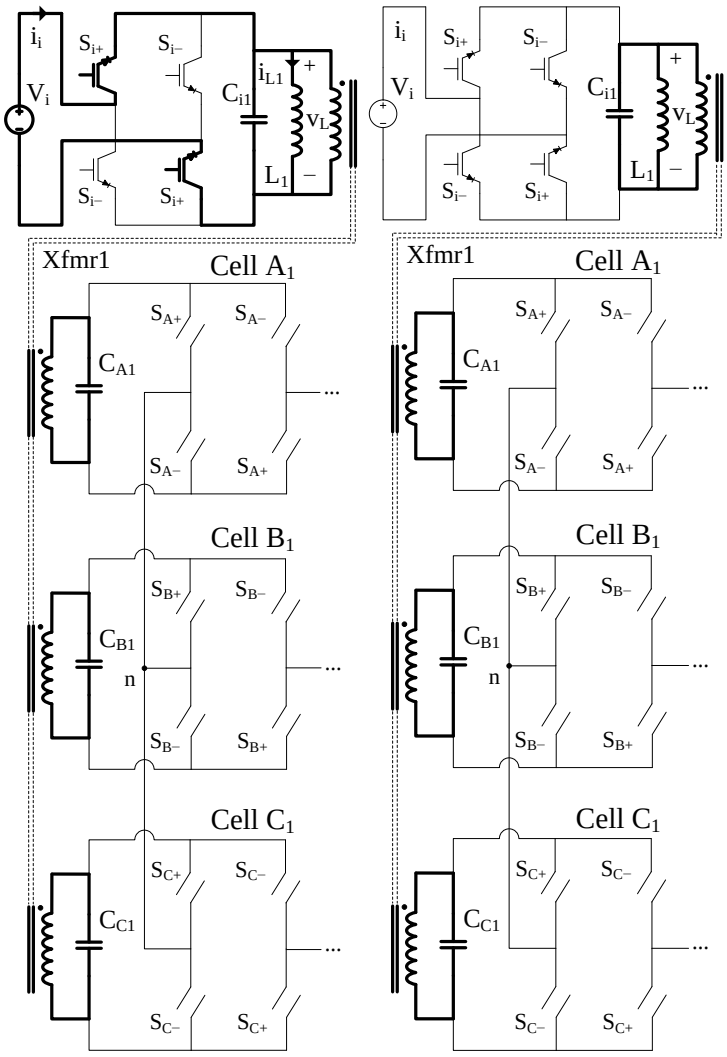


Figure 21 - Inverter waveforms during a full link cycle. Voltage and current labels for modes 3, 5, 9, and 11 correspond to an example in which $i_{ABC,ref} = \{0.8, -0.2, -0.6\}$ pu and $v_{ABC} = \{0.7, -0.8, 0.1\}$ pu. In boost operation, v_L of Mode 5 is larger than V_i.

part in the power transfer. During the odd-numbered modes, the digital controller monitors the unfiltered terminal currents i_i, i_A, i_B, and i_C, and adjusts the switch conduction times



(a) Charge Mode 1 (b) Resonant modes 2, 4, & 6

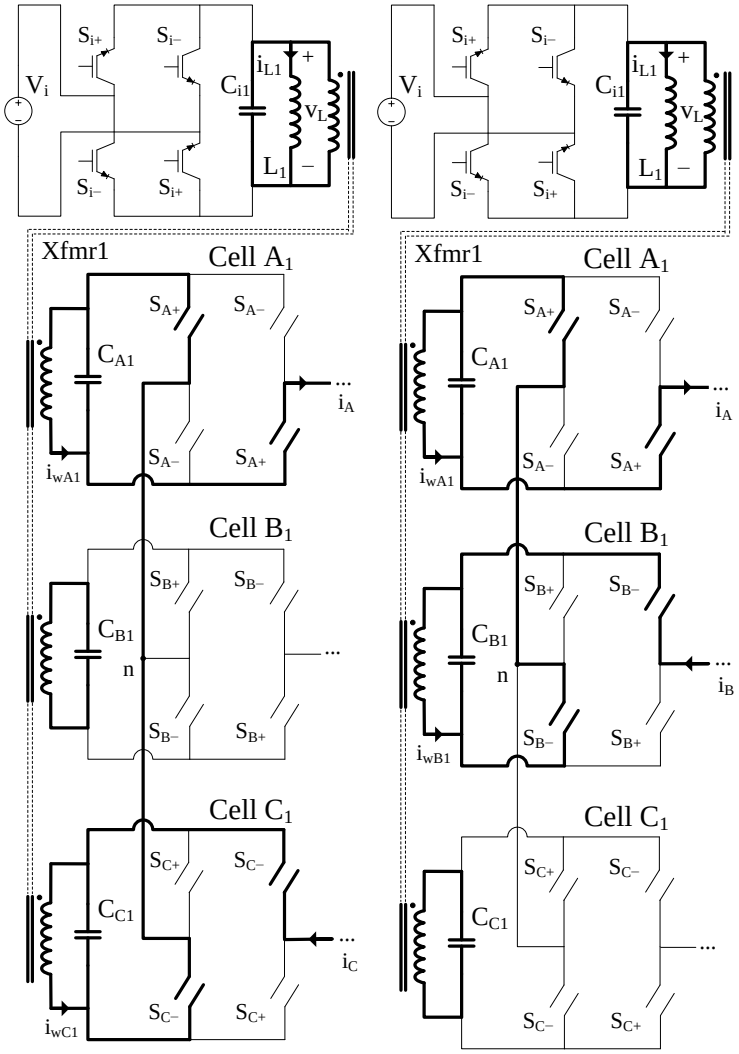
Figure 22 - Current path in different modes. Only one cell per phase is shown. Modes 3, and 5 correspond to an example in which $i_{ABC,ref}$ = {0.8,−0.2,−0.6} pu and v_{ABC} = {0.7,−0.8,0.1} pu.

to meet the input current reference, $I_{i,ref}$, and the sinusoidal output references $i_{A,ref}$, $i_{B,ref}$, and $i_{C,ref}$. The below paragraphs explain the operation of the modes and ignore the component non-idealities. Figure 22 and Figure 23 show the equivalent circuits of the first six modes. Since the cells of a phase operate identically, only cells A_1, B_1, and C_1 are shown in Figure 22 and Figure 23.

Charge Mode 1- Figure 22(a): Switches S_{i+} conduct and i_L increases linearly as depicted in Figure 21. When the average input current meets the reference $I_{i,ref}$, the S_{i+} switches stop conducting. The averaging method will be explained later. Since S_{i+} switches are located between the two capacitors C_i and C_{i1}, voltage on S_{i+} rises slowly. This near-ZVS condition significantly reduces the turn-off loss.

Resonant Mode 2 - Figure 22(b): All switches are off and the parallel link resonates. At the zero-crossing point of v_L, the link current has its positive peak $+I_{peak}$. The energy that was received by the link in Mode 1 should be delivered to the output phases in Modes 3 and 5. Out of the three pairs *AB*, *BC*, and *CA*, those pairs that include the phase with the largest instantaneous current reference are candidates to receive energy in Modes 3 and 5. For example, consider an instant when the sinusoidal current references are $i_{ABC,ref} = \{0.8,-0.2,-0.6\}$ pu and the phase voltages are $v_{ABC} = \{0.7,-0.8,0.1\}$ pu. In this case, phase pairs *AB* and *CA* are the candidates because phase *A* has the largest current reference. Between these two candidates, the pair with the smallest instantaneous line-to-line voltage will conduct in Mode 3, and the other pair is chosen for Mode 5. Therefore in our example, pairs *CA* and *AB* are selected for Modes 3 and 5, respectively. This results in a descending

order in link voltage in Modes 1, 3, and 5 as indicated in Figure 21, which is a necessity in obtaining ZVS at turn-on.



(a) Discharge Mode 3 (b) Discharge Mode 5

Figure 23 - Current path in different modes. Only one cell per phase is shown. Modes 3, and 5 correspond to an example in which $i_{ABC,ref}$ = {0.8,−0.2,−0.6} pu and v_{ABC} = {0.7,−0.8,0.1} pu.

Discharge Mode 3 - Figure 23(a): The selected phase pair receives energy in Mode 3. The directions of the winding currents $\{i_{wA1}, i_{wB1}, i_{wC1}\}$ are shown in Figure 23. Switches in this pair should conduct such that: 1) the current direction in a conducting phase matches the direction of its reference; and 2) the link voltage stays negative to discharge the link. Therefore in our earlier example, switches named S_{A+} and S_{C-} conduct. A total of $2K$ H-bridge cells receive energy in Mode 3, each having a link capacitor voltage of Nv_L. Since they are all connected in series, the total link voltage is $2KNv_L$. The switches do not conduct until they are forward-biased, that is when the total link voltage reaches the pair's instantaneous line-to-line voltage. This results in a ZVS turn-on for all conducting switches. In our example, S_{A+} and S_{C-} conduct when the total link voltage, $2KNv_L$, reaches the value $(v_C - v_A)$ as shown in Figure 21. As the switches conduct, the link current decreases linearly in Mode 3. When the average current in one of the conducting phases meets its reference, the switches are gated off and the converter will start Mode 4. The averaging method plays a key role in sinusoidal current shaping of the inverter, which will be explained later. Due to the presence of the link capacitors, the switch voltages rise slowly after turn-off. This near-ZVS condition reduces the turn-off losses considerably. Larger values for the link capacitances lead to a slower voltage rise and further reduce the turn-off losses.

Resonant Mode 4 - Figure 22(b): None of the switches conduct, letting the parallel link resonate as illustrated in Figure 21. The link voltage reduces in Mode 4. This mode ends as soon as the total link voltage $2KNv_L$ reaches the instantaneous line-to-line voltage of the pair that was chosen for Mode 5.

Discharge Mode 5 - Figure 23(b): As described earlier in Mode 2, the selected phase pair for Mode 5 receives energy from the link. Similar to Mode 3, the switches of this pair should conduct so that: 1) the current direction in a conducting phase matches the direction of its reference; and 2) the link voltage remains negative to discharge the link. Therefore in the earlier example, switches labeled S_{A+} and S_{B-} conduct. The switches are turned off when the total energy store in the link inductor(s) and capacitors decreases to a pre-determined level, $E_{desired}$, which will be explained later in this section. Similar to Mode 3, the switch voltages rise slowly after turn-off. This near-ZVS condition reduces the turn-off losses considerably. Larger values for the link capacitances tend to lower the switches' *dv/dt* and further reduce the turn-off losses and *dv/dt* -related problems.

Resonant Mode 6 - Figure 22(b): None of the switches conduct. Since there is still energy left in the link after Mode 5, the link can resonate. The magnitude of the link peak voltage in this mode, V_{peak}, depends on the predetermined $E_{desired}$. As soon as the link voltage reaches the input voltage $-V_i$, the switches S_{i-} start conducting at zero-voltage.

During the first six modes, the link current is almost entirely in its positive half cycle. Following Mode 6, the inverter starts the second six Modes 7-12 in which the link current experiences its negative half cycle. Operation of the converter in Modes 7-12 is similar to that of Modes 1-6, except that the voltage and current polarities are reversed. The fact that there is no interval in which the link inductor is connected to the input and output terminals at the same time makes this converter a buck-boost inverter. In reference to Figure 21, the inverter is said to operate in boost mode when the link discharge voltage, i.e., v_L in discharge Mode 5, is greater in magnitude than the input voltage, V_i. The reverse is true

about buck mode. The control algorithms of the converter in both cases are identical. It should not escape notice that the link frequency is different than the link *resonant* frequency, ω_{res}:

$$\omega_{res} = \sqrt{\frac{1}{L_{tot} C_{tot}}}. \tag{37}$$

3.1.1.3 Buck-Boost Operation, Selection of $E_{desired}$, and Soft-Switching Range

The proposed inverter charges and discharges the link inductor in completely separate intervals. Therefore it inherently has the ability to buck or boost the input votlage. The inverter is considered to operate in buck mode when the link discharging votlage in mode 5, is smaller in magnitude than the link charging voltage in mode 7. Such a case is shown by the dashed waveform of in Figure 21. One should notice that the charging and discharging voltages are viewed from the primary side of the transformer. Similarly, the converter operates in boost mode if the link discharging voltage in mode 5 is greater in magnitude than the link charging voltage, V_i, as shown by the solid waveform for v_L in Figure 21.

The energy stored in the link at a point in time, E, is given by:

$$E = \frac{1}{2} C_{tot} v_L^2 + \frac{1}{2} L_{tot} i_L^2. \tag{38}$$

As stated earlier, Mode 5 ends when E drops to a pre-determined level, $E_{desired}$. This guarantees that the link energy at the end of Mode 5 is the same in all cycles. Therefore, it indirectly ensures that the summation of the losses and outgoing energy of Modes 3 and 5 equals the energy input of Mode 1. Moreover, since all switches are in their blocking

state in Mode 6, the link energy in this mode does not change. From (38), one can derive the link peak voltage as:

$$V_{peak} = \sqrt{\frac{2E_{desired}}{C_{tot}}}. \tag{39}$$

Small values for $E_{desired}$ (and V_{peak}) are generally preferred since a large V_{peak} not only imposes a greater voltage stress on the components, it also prolongs resonant Mode 6 and decreases the link frequency.

By examining v_L in Figure 21, one can notice the descending order of link voltage in modes 1, 3, and 5 (and similarly the ascending order in modes 7, 9, and 11). It is this arrangement of link voltages that creates a ZVS condition for all output switches. Since the descending arrangement is always achievable regardless of the input voltage, output voltage and input current reference, ZVS is maintained for the output switches at every operating point. As shown in Figure 21, the link voltage in Mode 6 should start from the discharging voltage (v_L of Mode 5) and reach the charging voltage, $-V_i$ by way of resonance. In buck operation, the link discharging voltage is smaller than the charging voltage by definition. Therefore one should carefully select the value for $E_{desired}$ large enough so that V_{peak} be greater than V_i, otherwise the link voltage can never reach $-V_i$ and soft-switching will not be achieved at the turn-on of the input switches in Mode 7. As long as $E_{desired}$ is large enough, soft-switching for the input switch is achieved throughout the range of operation. In boost mode of operation, on the other hand, the link discharging voltage is greater than the charging voltage by definition. Thus, the V_{peak} criterion for selection of $E_{desired}$ is needless.

In the multiple-transformer embodiment, the link inductance is composed of the parallel connection of the magnetizing inductances of all transformers. Similarly, the total link capacitance is composed of the parallel connection of all link capacitors. Therefore, in case of unequal magnetizing inductances or link capacitances, all transformers resonate at the same frequency and in synchronism, without loss of soft-switching. However, the power processed by each transformer is inversely proportional to its magnetizing inductance value simply because the input current is distributed among the transformers based on their magnetizing inductance values. Therefore it is recommended to have balanced inductance values.

3.1.2 Control and Current Shaping

The overall control block diagram of the proposd inverter is depicted in Figure 24. The is composed of three major blocks, namely the *State Machine*, the *Current Integrators*, and the *Output Current Reference Generator*. The State Machine identifies the operating mode of the converter (modes 1 thru 12) and generates appropriate commands to the switches. As shown in Figure 25, the operation of the State Machine is completely based on the description of modes which was explained earlier. The operation of the other two blocks will be explained here.

According to the description of modes in subsection 2.1.2.2, the input reference and terminal currents are dc ($I_{i,ref}$ and i_{if}), while output references, $\{i_{A,ref}, i_{B,ref}, i_{C,ref}\}$, and terminal currents, $\{i_{Af}, i_{Bf}, i_{Cf}\}$, are the sinusoidal. The unfiltered terminal currents i_i, i_A, i_B, i_C assume a trapezoidal shape as indicated in Figure 21. The goal of the overall controller is to regulate the switch conduction times so that the *average* unfiltered terminal currents

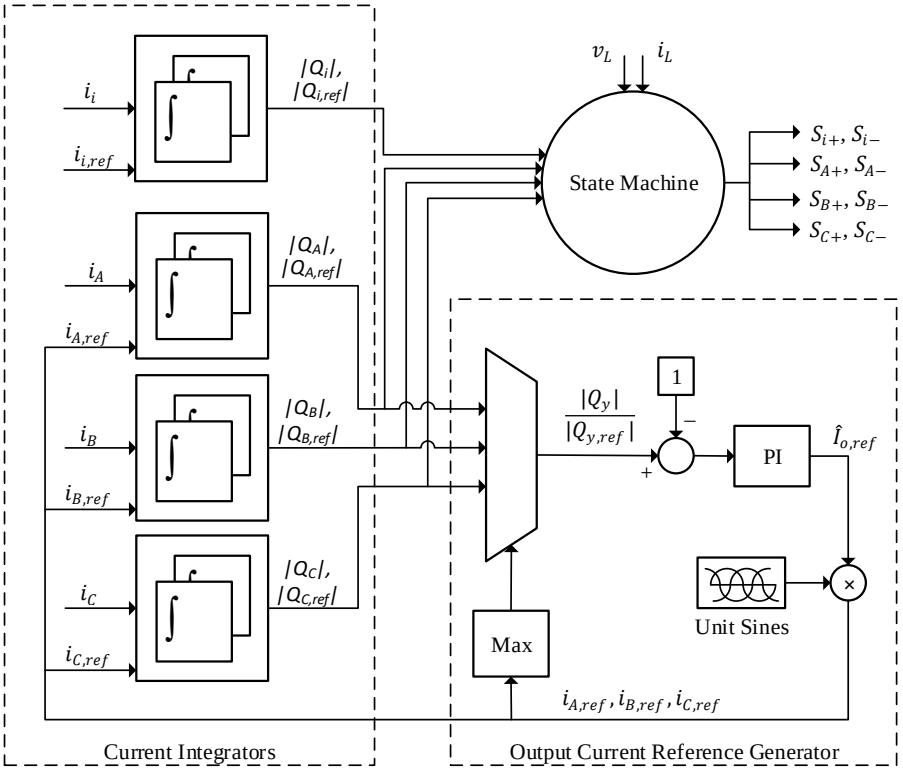


Figure 24 - Detailed control block diagram of the proposed inverter.

track their references. The *average* is defined as the area under a curve in a link cycle divided by the link period. However, since the link period is the same for all waveforms, the division is not required. This will in turn reduce the computational burden on the controller. It is important to note that no frequency or pulse-width modulation [64][65][66] is required in the proposed inverter due to the fact that switch conduction times are controlled based on average currents.

Figure 26 shows the unfiltered input and output currents and their integral values in a link cycle. The symbols Q_x and $Q_{x,ref}$ denote the outputs of the current integrators as functions of time, where $x \in \{i,A,B,C\}$. The waveforms are depicted for an example case

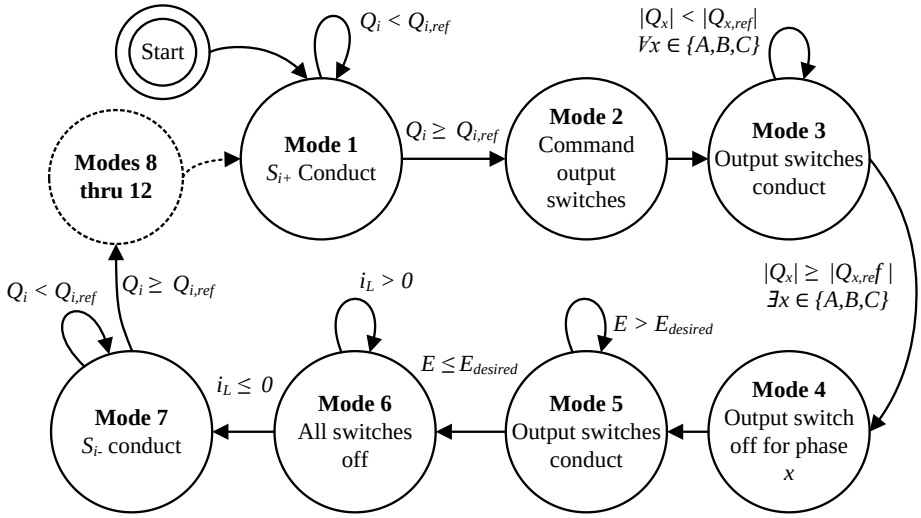


Figure 25 – State machine block diagram of the proposed inverter.

in which $i_{ABC,ref} = \{0.8,-0.2,-0.6\}$ pu and $v_{ABC} = \{0.7,-0.8,0.1\}$ pu. There is an averaging integrator associated with each reference and each unfiltered current, totaling to eight integrators as shown in Figure 24.

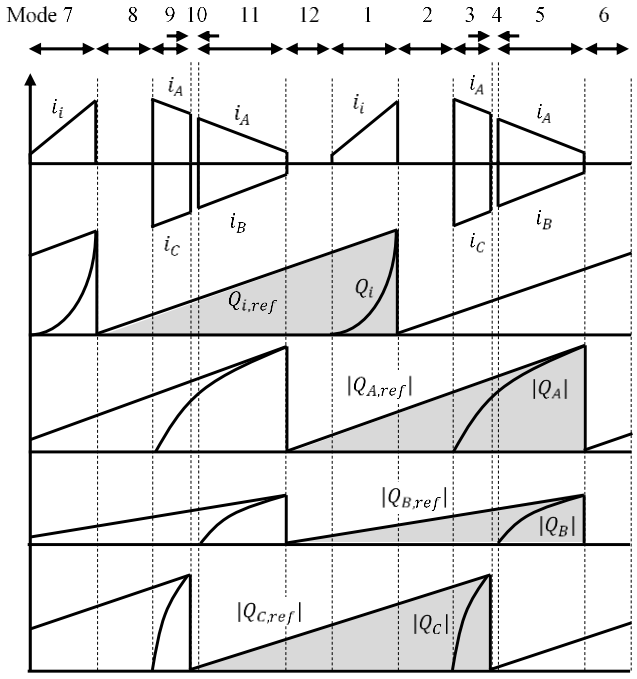
In charge mode 1 (or 7) when the input switches conducts, the State Machine constantly compares Q_i with $Q_{i,ref}$. As soon as the two values match, the input reference current is satisfied and the input switches are commanded off. As indicated in Figure 26, both integral values, Q_i and $Q_{i,ref}$, are reset at the end of mode 1 (or 7) to prepare for the next half-cycle. One may notice that $Q_{i,ref}$ increases linearly because it is the integral value of the dc reference, $I_{i,ref}$.

According to the description of mode 3 (or 9) in subsection 2.1.2.2, the requirement to end this mode is to have one of the conducting phases meet its reference. In the example of Figure 26, it would be phase C that meets its reference. The current integrators associated with this phase are reset at the end of mode 3 (or 9). In mode 5 (or 11), in contrast, the end criterion is based on link energy rather than current regulation. However, this end criterion is equivalent to current regulation criterion provided that the input and output current references satisfy the following power balance equation:

$$V_i I_{i,ref} = P_{loss} + \frac{3}{2}\hat{V}_o \hat{I}_{o,ref} \cos\varphi_o \quad , \tag{40}$$

where P_{loss} is the inverter power loss at the point of operation, $\hat{V}_o$ is the output phase voltage amplitude, $\hat{I}_{o,ref}$ is the output current reference amplitude, and $cos\varphi_o$ is the output power factor. It is the controller's responsibility to adjust $\hat{I}_{o,ref}$ so (40) is satisfied, otherwise the output current references for the two phases that conduct in mode 5 (or 11) will not be met and the phase currents will deviate from their expected sinusoidal shapes. An example of such a case is shown in Figure 27, in which the right-hand side of (40) outweighs the left-hand side. In this figure, the current references for phases *A* and *B* cannot be met simply because the link does not have enough energy stored in its inductor. Reference [44] proposes to estimate P_{loss} and calculate PV array power to find $\hat{I}_{o,ref}$, but such a scheme requires samples of all variables used in (40) as well as an estimation method for P_{loss}.

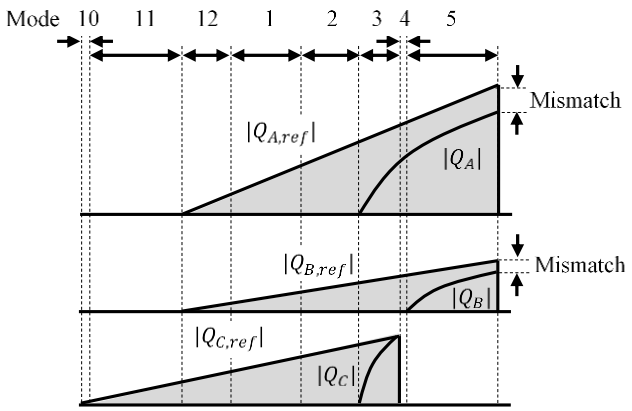
In this section, a simple method that takes advantage of the mismatch at the end of mode 5 (or 11) and a PI controller is proposed to calculate $\hat{I}_{o,ref}$ without using (40). This method



Current integration when (40) is satisfied

Figure 26 - Input and output current regulation in the proposed inverter, corresponding to an example in which $i_{ABC,ref} = \{0.8, -0.2, -0.6\}$ pu and $v_{ABC} = \{0.7, -0.8, 0.1\}$ pu. Zones of interest are shaded for clarity.

is implemented by the *Output Current Reference Generator* block in Figure 24. Taking the power-balanced operating point of the example of Figure 26, the moment that the link energy reaches $E_{desired}$ in mode 5, coincides with the moment that the ratios $Q_A/Q_{A,ref}$ and $Q_B/Q_{B,ref}$ become unity. $Q_A/Q_{A,ref}$ is a better indicator in this example because phase *A* has the largest current reference and its current signal is less susceptible to noise. In the power-unbalanced case of Figure 27, however, the ratio $Q_A/Q_{A,ref}$ at the end of mode 5 is not unity. The error signal $1-|Q_y/Q_{y,ref}|$ is used by the PI controller to generate $\hat{I}_{o,ref}$. Subscript



Current integration when (40) is not satisfied due to excessively large $\hat{I}_{o,ref}$

Figure 27 - Input and output current regulation in the proposed inverter, corresponding to an example in which $i_{ABC,ref}$ = {0.8,−0.2,−0.6} pu and v_{ABC} = {0.7,−0.8,0.1} pu. Zones of interest are shaded for clarity

y indicates the phase with the largest current reference. The PI controller operates at twice the link frequency so that it can compensate the power imbalance promptly.

According to the inverter operation set forth, the control principle requires samples of i_L, v_L, i_i, i_A, i_B, and i_C. Voltage sensors on input and output terminals may be needed by the application for secondary purposes such as Maximum Power Point Tracking (MPPT), grid synchronization, protection, or output voltage regulation. Although the transformer has *3K+1* windings (single-transformer embodiment) or four windings (multiple-transformer embodiment), measurement of the magnetizing current i_L can be carried out using only one current sensor on the input winding and one open-aperture current sensor on all output. In case of unity turn ratio (*N=1)*, only one current sensor would be sufficient to measure all winding currents. When using multiple transformers, current measurement on only one transformer is necessary because all transformers operate in synchronism.

3.1.3 Inverter Analysis and Design

3.1.3.1 Mathematical Modeling

The link frequency of the proposed partial-resonant inverter, f_{Link}, is a function of the circuit parameters and the operating point. This sub-section formulates the effect of various inverter parameters on important variables, such as f_{Link} and I_{peak}. This modeling makes the below assumptions:

- Due to the half-wave symmetry in the link waveforms, it is sufficient to analyze the first six modes only.
- The link capacitors are not factored in the equations of charge and discharge modes because the current through the link capacitors is negligible in these modes.
- The transformer copper resistances are not factored in the equations of resonant modes. This because at the resonant frequency they have a much smaller impedance than the link capacitors (see Table IV).
- Voltage ripples of the filter capacitors and voltage drops on the filter inductors are ignored.
- Unless mentioned otherwise, variable t in the equations of a mode is the time passed since the start of the mode. Let $I_{m,0}$ and $V_{m,0}$ denote the initial conditions for i_L and v_L at the start of Mode m, respectively. Similarly, T_m is the duration of Mode m.
- As indicated in Figure 21, T_4 is significantly shorter than the duration of other modes. Therefore Modes 3 and 5 can be combined in to a single mode, ignoring Mode 4. The link voltage in Modes 3 and 5 is made of the output line-to-line

voltage and repeats every π/3 radians. The average v_L in the combined mode, $V_{3,5}$, is given by (41):

$$\begin{aligned} V_{3,5} &= \frac{3}{2\pi Nk}\hat{V}_o \int_{-\frac{\pi}{6}}^{+\frac{\pi}{6}} \left[\cos\theta - \frac{\cos(\theta + 2\pi/3) + \cos(\theta - 2\pi/3)}{2} \right] d\theta \\ &= \frac{1.432}{2\pi NK}\hat{V}_o \end{aligned} \tag{41}$$

where $\hat{V}_o$ is the phase peak voltage. As shown in Figure 21, the link period is:

$$T_{Link} \approx 2\times\left(T_1 + T_2 + T_3 + T_5 + T_6\right) \tag{42}$$

Let the equivalent resistance of the parallel-connected input windings be R_i, and the on-state resistance of an input switch be $R_{ds,i}$. Then the link voltage and current for Mode 1 are readily given as:

$$\begin{cases} v_L(t) = V_i - \left(R_i + 2R_{ds,i}\right) i_L, & (43) \\ i_L(t) = \dfrac{V_i}{R_i + 2R_{ds,i}} + \left(I_{1,0} - \dfrac{V_i}{R_i + 2R_{ds,i}} \right) e^{-\frac{R_i + 2R_{ds,i}}{L_{tot}} t}. & (44) \end{cases}$$

During resonant modes, all link capacitors and inductor(s) are connected in parallel. The solution to this *LC* network is:

$$\begin{cases} v_L(t) = -L_{tot}\omega_{res} I_{m,0} \sin\left(\omega_{res} t\right) + V_{m,0} \cos\left(\omega_{res} t\right), & (45) \\ i_L(t) = I_{m,0} \cos\left(\omega_{res} t\right) + V_{m,0} \sqrt{\dfrac{C_{tot}}{L_{tot}}} \sin\left(\omega_{res} t\right). & (46) \end{cases}$$

With reference to Figure 23(a,b) and assuming that resistance of an output-side winding is R_o and the on-state resistance for an output switch is $R_{ds,o}$, the link equations in the combined Modes 3 and 5 are:

$$\begin{cases} v_L(t) = -\dfrac{V_{3,5}}{2NK} - \dfrac{R_o + 2R_{ds,o}}{2N^2K} i_L, & (47) \\ i_L(t) = \dfrac{-V_{3,5}N}{R_o + 2R_{ds,o}} + \left(I_{3,0} - \dfrac{V_{3,5}N}{R_o + 2R_{ds,o}} \right) e^{-\frac{R_o + 2R_{ds,o}}{2N^2 K L_{tot}} t}. & (48) \end{cases}$$

Equations (43-48) for i_L and v_L in all modes are derived. When these equations are combined with the description of the modes, they result in a system of equations given in (49-53). Unknowns to be solved for are T_1, T_2, T_3+T_5, T_6, and $I_{1,0}$. Equations for $V_{m,0}$ and $I_{m,0}$ are reported in the Appendix.

$$\begin{cases} \dfrac{1}{2} I_{i,ref} T_{link} = \dfrac{V_i}{R_i + 2R_{ds,i}} T_1 + \dfrac{L_{tot}}{R_i + 2R_{ds,i}} \left(I_{1,0} - \dfrac{V_i}{R_i + 2R_{ds,i}} \right) \left(1 - e^{-\frac{R_i + 2R_{ds,i}}{L_{tot}} T_1} \right), & (49) \\ V_{3,0}(t) = -L_{tot} \omega_{res} I_{2,0} \sin(\omega_{res} T_2) + V_{2,0} \cos(\omega_{res} T_2), & (50) \\ E_{desired} = \dfrac{1}{2} C_{tot} V_{6,0}^2 + \dfrac{1}{2} L_{tot} I_{6,0}^2, & (51) \\ V_{1,0}(t) = -L_{tot} \omega_{res} I_{6,0} \sin(\omega_{res} T_6) + V_{6,0} \cos(\omega_{res} T_6), & (52) \\ -I_{1,0} = I_{6,0} \cos(\omega_{res} T_6) + V_{6,0} \sqrt{\dfrac{C_{tot}}{L_{tot}}} \sin(\omega_{res} T_6). & (53) \end{cases}$$

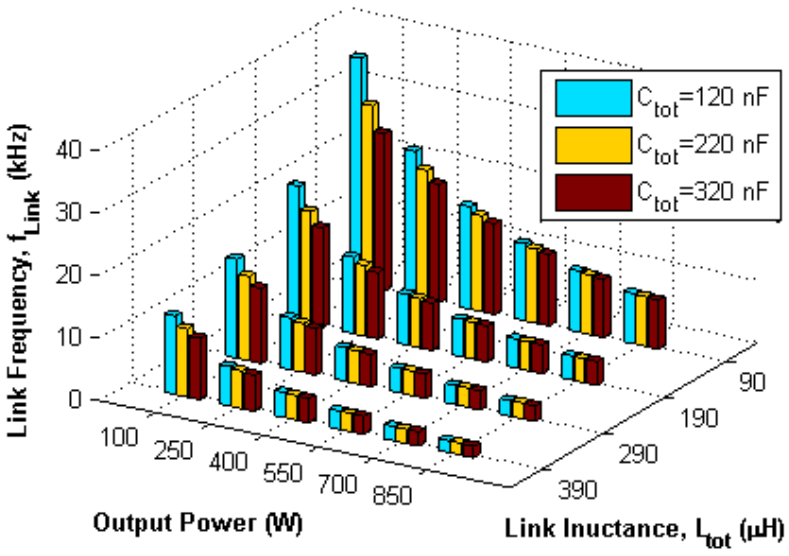
The above system of equations can be solved numerically. Once the unknowns are solved for, I_{peak} can be obtained from (54).

$$\frac{1}{2} L_{tot} I_{peak}^2 = \frac{1}{2} C_{tot} V_{2,0}^2 + \frac{1}{2} L_{tot} I_{2,0}^2 \quad (54)$$

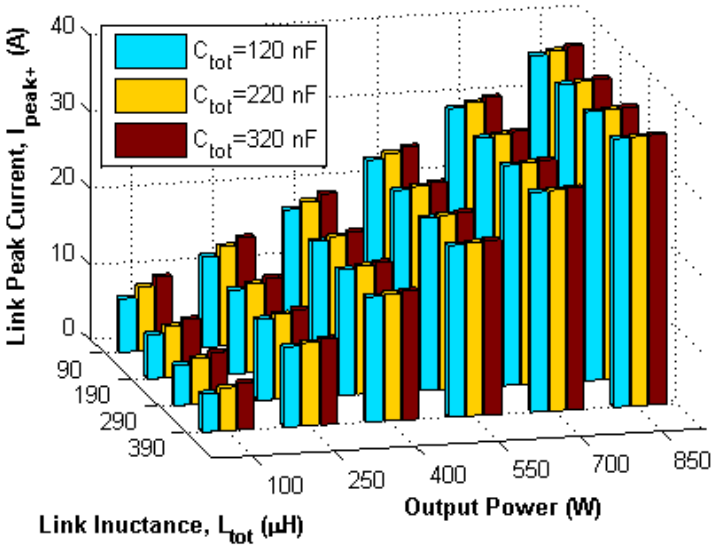
3.1.3.2 Inverter Design

The link frequency, f_{Link}, is an important variable because is determines the switching frequency, filter size, transformer core loss, and the digital controller sampling rate. The link peak current, I_{peak}, plays a major role in determining the switch conduction losses, transformer copper and core loss, switch ratings, and transformer design. In this sub-section, a 750 W prototype at an input voltage of V_i = 100 V and output voltage of V_{LL} = 380 V is analyzed.

Figure 28 shows f_{Link} and I_{peak} as a function of the output power, L_{tot}, and C_{tot}. The turn ratio is N = 1 in this figure. As displayed in Figure 28(a), f_{Link} reduces as the link parameters, L_{tot} and C_{tot}, increase. This is expected because greater values for L_{tot} and C_{tot} result in a smaller resonant frequency, ω_{res}, and lengthen the resonant modes, see (37,42). C_{tot} has a small effect on f_{Link} because it does not affect the duration of the charge and discharge modes. However, this is not true with L_{tot}. Due to the fact that the link inductor is the main energy transfer element in the inverter, the durations of the charge and discharge modes depend directly on how fast the link can charge and discharge to meet the current reference requirements. By the same token, the link frequency is a decreasing function of the output power. It is noteworthy that at an output power close to zero, the duration of the charge and discharge modes shrink to such an extent that the link frequency approaches the link resonant frequency. In reference to Figure 28(b), the link peak current, I_{peak}, increases with the output power as anticipated. During resonance in Mode 2 where the link peak current happens, the link capacitors totally discharge into the link inductor. Therefore, considering that the energy stored in the link capacitors is typically much lower



(a) Link frequency, f_{Link}



(b) Link peak current, I_{peak}

Figure 28 - Link frequency and link peak current as a function of output power and L_{tot}, for different values of C_{tot}. The turn ratio (N), input and output voltages are 1, 100 V and 380 V^{rms}, respectively.

than that of the link inductor(s), higher values for C_{tot} lead to slightly higher values for

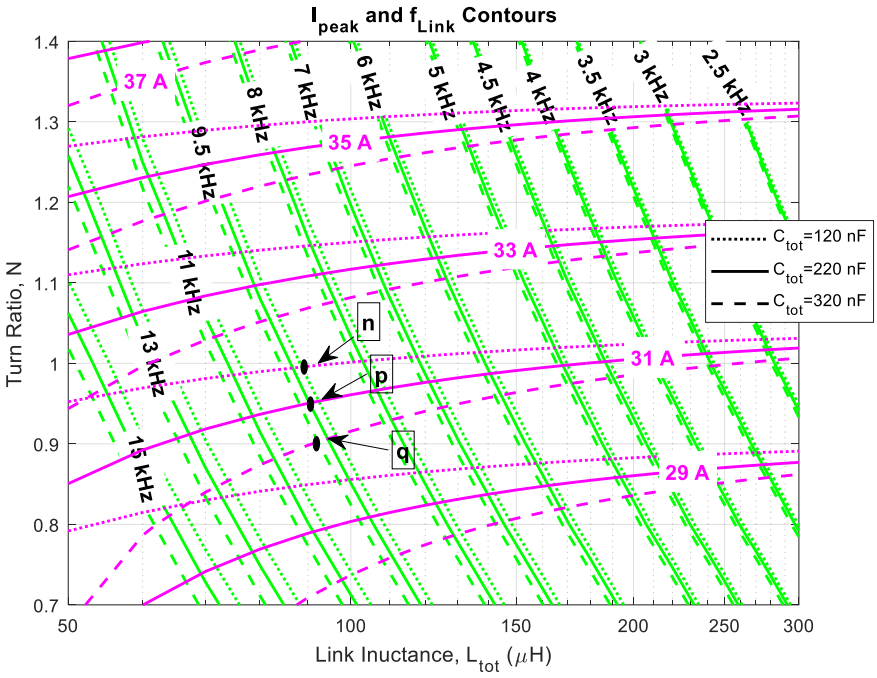


Figure 29 - The contours of link frequency and peak current at 750 W for selecting values for L_{tot}, C_{tot}, and N.

I_{peak}. According to Figure 28, the inverter can switch at a high frequency when L_{tot} and C_{tot} are small, but it would require a digital controller with a high sampling rate to implement the twelve modes. The main role of the link capacitors is to provide ZVS at turn-on transitions and to control the *dv/dt* on the switches at turn-off to achieve near-ZVS conditions.

Due to the importance of f_{Link} and I_{peak}, they can be used as targets during the design phase. Figure 29 shows the contour paths of f_{Link} and I_{peak} at an output power of 750 W on the same plot for various values of L_{tot}, C_{tot}, and N. This single plot can serve as a very useful tool to select inverter parameters. Given the target values for the link frequency and

TABLE III. SUMMARY OF INVERTER DESIGN EQUATIONS

Maximum Stress	Boost Operation†	Buck Operation†	Eq.
Output Switch Voltage Stress	$\frac{1}{2K}\hat{V}_o\left(\frac{N\sqrt{3}}{2}+1\right)$	$\frac{1}{2K}\hat{V}_o+\frac{N}{2}V_i$	(55)
Input Switch Current Stress	I_{peak}		(56)
Fundamental Equations (49-53)	Represented by contour plots of Figure 29		
Output Switch Current Stress	$\frac{I_{peak}}{2NK}$		(57)
Input Switch Voltage Stress	$\frac{\sqrt{3}}{4NK}\hat{V}_o+\frac{1}{2}V_i$	V_i	(58)
Output Switch *dv/dt*	$N\frac{I_{peak}}{C_{tot}}$		(59)
Input Switch *dv/dt*	$\frac{I_{peak}}{C_{tot}}$		(60)

†Whether the inverter operates in buck or boost mode can be determined by comparing V_i with $V_{3,5}$.

peak current, the intersection points of the f_{Link} and I_{peak} contours denote the required values for L_{tot}, C_{tot}, and N.

While a certain design may have various targets such as minimizing switch stress, minimizing *dv/dt*, maximizing efficiency, or a weighted combination of several targets, a straightforward approach to select components for the proposed inverter is presented here. Selection process for L_{tot}, C_{tot} should be based on a worst-case operating point, namely at rated power, rated output voltage, and lowest solar panel voltage (corresponding to the hottest panel temperature for a majority of PV technologies). The equations governing the

design process are summarized in Table III. The number of cells per cell, *K*, may be chosen according to inverter construction constraints such as the number of transformer windings etc. Alternatively, one may use an initial value for *K* and modify it during the design upon need.

The goal in the design process to find appropriate values for L_{tot}, C_{tot}, and *N*. The design can be started off by assuming values for input switch current stress, output switch voltage stress, and link frequency. According to (56), the link peak current is directly determined by the input switch current stress. Given the values for f_{Link} and I_{peak}, the contour plots of Figure 29 suggest infinite sets of answers for *N*, L_{tot}, and C_{tot}. For example, in a design that targets 11 kHz and 31 A for f_{Link} and I_{peak}, points *n*, *p*, and *q* on Figure 29 are possible sets of answers. In order to find unique values for *N*, L_{tot}, and C_{tot}, one may use another expression from Table III.

3.1.3.3 Inverter Loss Calculation

The proposed inverter maintains ZVS and near-ZVS conditions at all switch turn-on and turn-off transitions, respectively. Therefore the dominant factors that contribute to the power loss are the semiconductor conduction loss, transformer conduction loss, and transformer magnetization loss. This subsection, takes advantage of the steady-state equations of (49-53) to calculate these loss values. Letting $I_{sw,i}^{av}$ and $I_{sw,i}^{rms}$ denote the average and RMS values of the current through an input switch, $V_{d,i}$ denote the dc drop across an input switch, and $R_{ds,i}$ denote the on-state resistance of an input switch, the total conduction loss associated with the input switches in the single-transformer embodiment is:

$$P_{sw,i} = 4 \times \left[I_{sw,i}^{av} V_{d,i} + (I_{sw,i}^{rms})^2 R_{ds,i} \right]. \quad (61)$$

The equations for all average and RMS currents in (61-64) are included in the appendix. In order to obtain $P_{sw,i}$ in the multiple-transformer embodiment, one can simply modify the above equation. Using similar notations for the output switches, the total conduction loss in the output switches in both embodiments is given by:

$$P_{sw,o} = 8K \times \left[I_{sw,o}^{av} V_{d,o} + (I_{sw,o}^{rms})^2 R_{ds,o} \right]. \quad (62)$$

The conduction loss in the transformer windings is caused by the contributions of the active (odd-numbered) modes and the resonant (even-numbered) modes. The input winding(s) do not experience losses in discharge mode. Likewise, the output windings do not carry current in charge modes. However, all windings share the link current during the resonant modes and therefore experience conduction loss. The input winding loss in the single-transformer embodiment is:

$$P_{w,i} = 2R_{wi,dc} F_{r,wi}(f_{Link}) \times \left[(I_{sw,i}^{rms})^2 + f_{Link} \times \frac{C_{i1}^2}{C_{tot}^2} \times (U_1 + U_2) \right], \quad (63)$$

where $R_{wi,dc}$ is the dc resistance of the input winding. The terms U_1 and U_2 are described in the appendix. The dimension-less factor $F_{r,wi}(f_{Link})$ accounts for the skin and proximity effects and is a function of frequency and transformer geometry. While there are several papers dedicated to account for skin and proximity effects in magnetic components [59][60], an interested reader may use the method developed in [61] to calculate $F_{r,wi}$. This method is properly applicable here because the performance of the multiple-winding transformer in the proposed topology is similar to that of a multiple-

winding inductor. The equation for the input winding loss in the multiple-transformer embodiment can be readily identified by modifying the above equation.

The total conduction loss in the output windings of the single-transformer embodiment is:

$$P_{w,o} = KR_{wo,dc}F_{r,wo}(f_{Link}) \times \left[4(I_{sw,o}^{rms})^2 + 6 f_{Link} \times \frac{C_{A1}^2}{N^2 C_{tot}^2} \times (U_1 + U_2) \right], \tag{64}$$

where $R_{wo,dc}$ is the dc resistance of an input winding, and $F_{r,wo}(f_{Link})$ factors in the skin and proximity effects [61].

The power loss in the transformer ferrite core is a function core volume V_{core}, link frequency f_{Link}, peak magnetic flux density $\hat{B}$, and core material. The Modified Steinmetz Equation discussed in [62] is an appropriate method to calculate losses in ferromagnetic cores with a non-sinusoidal excitation. This method introduces an equivalent frequency, f_{eq}, based on the average rate of change of the magnetic flux density,$\dot{B}_{av}$. Letting B denote the flux density waveform in the core during a link cycle, quantities $\dot{B}_{av}$ and f_{eq} are given by:

$$\dot{B}_{av} = \hat{B} \int_{\frac{T_{Link}}{2}} \left(\frac{dB}{dt} \right)^2 dt, \tag{65}$$

$$f_{eq} = \frac{\dot{B}_{av}}{\hat{B}\pi^2}. \tag{66}$$

The core power loss is calculated using the Modified Steinmetz Equation [62]:

$$P_{core} = V_{core} C_m f_{eq}^{X_m - 1} \hat{B}^{Y_m} f_{Link}, \tag{67}$$

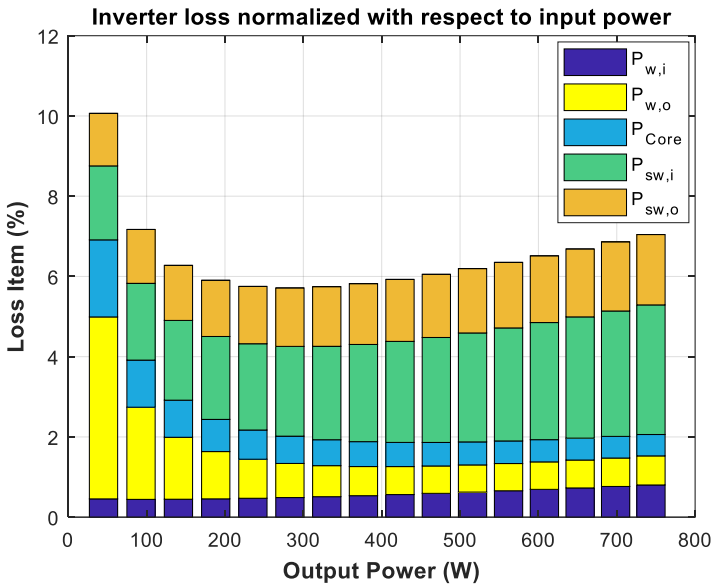


Figure 30 - Calculated loss items for the single-transformer inverter of Table II. The input and output voltages are 00 V and 380 V^{rms}, respectively.

where C_m, X_m, and Y_m are the same parameters used in the original Steinmetz Equation and are based on empirical core loss measurements provided by the core manufacturer. Based on the above discussion, the total inverter loss is calculated in (68). It should be mentioned that (68) slightly underestimates the total loss because it does not account for the negligible near-ZVS turn-off losses. The plot of calculated power loss for the converter of Table IV is presented in Figure 30. This figure indicates that at power points closer to the nominal power, a substantial contributor to the total loss is the conduction loss in the

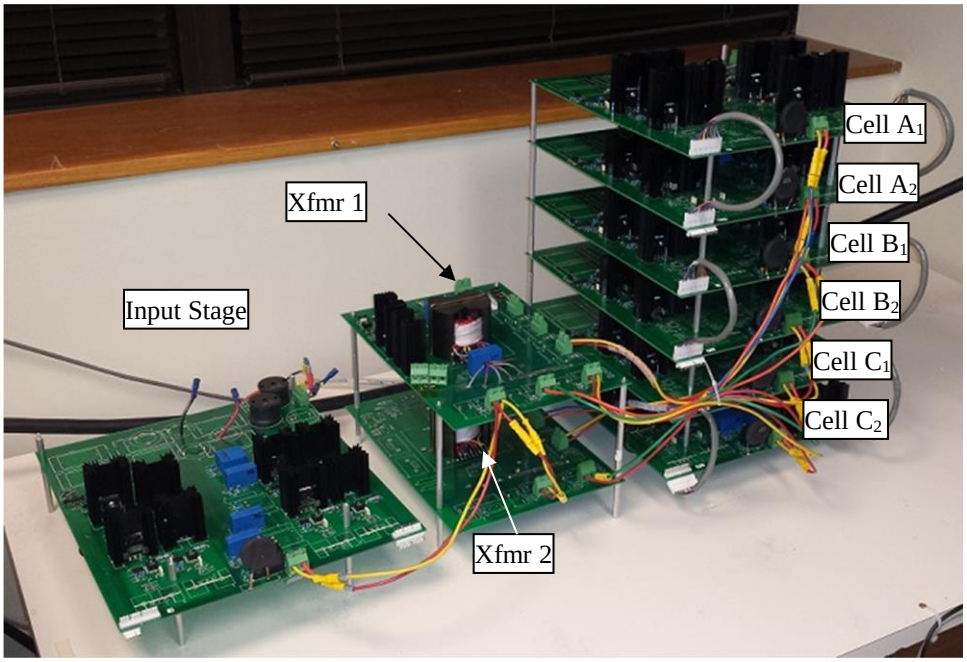


Figure 31 - Photograph of the proposed inverter.

input switches. Therefore employment of wide band-gap devices on the input side can significantly increase the conversion efficiency [63]. At lower power points, however, the transformer core and conduction losses outweigh other losses. This is attributed to the increased link frequency at low powers (*c.f.* Figure 28) which in turn amplifies the terms $F_{r,wo}$, and f_{eq} in (64) and (67), respectively. If a design requires higher efficiency at low power, it can utilize *litz* (bundled) wires with finer strands to keep $F_{r,wo}$ small.

$$P_{loss,tot} = P_{sw,i} + P_{sw,o} + P_{w,i} + P_{w,o} + P_{core} \tag{68}$$

3.1.4 Experimental Validation

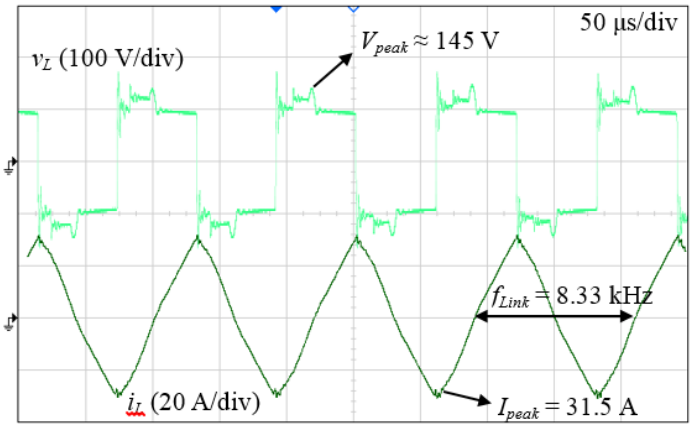
A laboratory setup has been designed and built to test the validity of the design. The photo of the setup and the specifications are shown in Figure 31 and Table IV,

TABLE IV. INVERTER AND COMPONENT SPECIFICATIONS

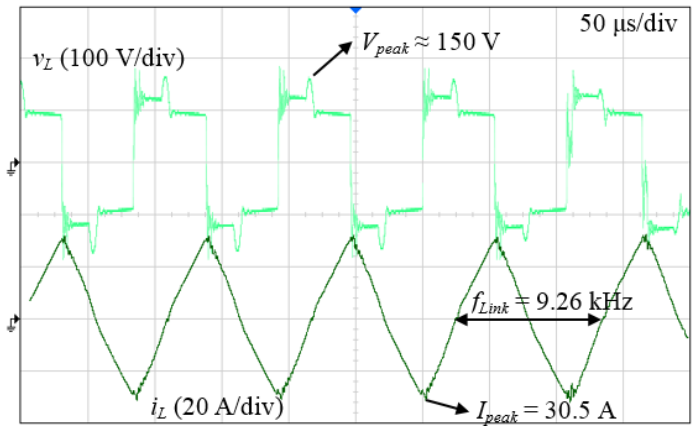
Output Power	750 W		
Input Voltage (V_i)	100 V		
Line Output Voltage (V_{LL})	380 V^{rms}		
Line Frequency	60 Hz		
	Single-Trans.	Multiple-Trans.	
	Xfmr1	Xfmr1	Xfmr2
Magnetizing Inductance	110 µH	176 µH	184 µH
Min and Max Leakage Ind†. (L_{lxk})	5, 2.82 µH	4.1, 7 µH	4.2, 8.2 µH
Turn Ratio (N)	1	1	1
Total Link Inductance (L_{tot})	110 µH	90 µH	
Total Link Capacitance (C_{tot})	120 nF	120 nF	
Link Resonant Freq. ($\omega_{res}/2\pi$)	41.8 kHz	51 kHz	
Input Filter (L_i, C_i)	10 µH, 1 mF		
Output Filter (L_x, C_x)	Zero µH, 5 µF		
Input Switch (S_{i+} S_{i-})	STW72N60DM2AG (MOSFET)		
Output Switches (S_{x+}, S_{x-})	IRG7PH42UD (IGBT)		
Transformer Cores	PM-74×59 (N27)		
Digital Controller	TMS320F28335		

†Measured at 10 kHz while input winding shorted.

respectively. There are two cascaded H-bridge cells per phase ($K=2$). Transformers *Xfmr1* and *Xfmr2* are used in the multiple-transformer implantation. Small modifications are performed on *Xfmr1* to use it in the single-transformer implementation as well. No particular care is taken regarding the symmetry of the winding leakage inductances. The



(b) Multiple-transformer embodiment



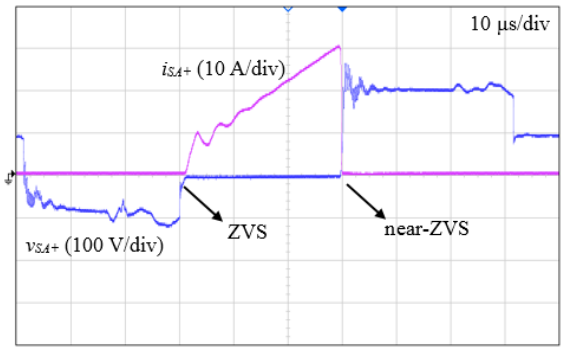
(a) Single-transformer embodiment

Figure 32 - Link voltage and link current at the operating point of Table IV.

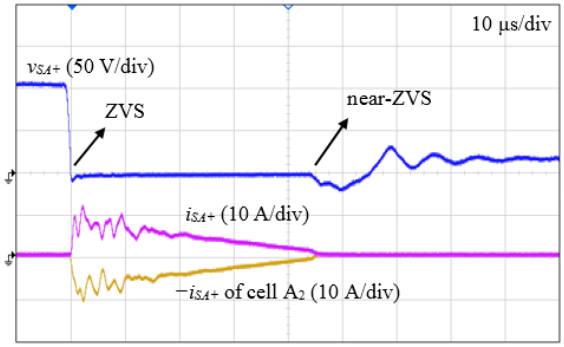
turn ratios are selected to be *N=1* to demonstrate the buck and boost capabilities of the inverter.

In the first experiment, both embodiment are tested at the terminal conditions listed in Table IV. The link waveforms, link frequency, and link peak values are shown in Figure 32 for both embodiments. Calculated values based on the analysis of section 3.1.3 for the

single-transformer inverter are I_{peak} = 31 A and f_{Link} = 8 kHz, and for the multiple-transformer inverter are I_{peak} = 31.2 A and f_{Link} = 9.4 kHz. As indicated by the v_L waveforms, the selected values for L_{tot} and C_{tot} result in very short resonant modes, so that most of the link period is spent on the charge and discharge modes that transfer real power. The transformer leakage inductances create fluctuations in the link voltage. However, as it will be illustrated later in this section, the leakages do not interfere with the soft-switching.



(a) Input switch



(b) Output switches of cells A_1 and A_2

Figure 33 - Switch stress.

The waveforms of an input and an output switch of the single-transformer embodiment are shown in Figure 33. Switching waveforms of the multiple-transformer embodiment are not included as they are similar to Figure 33. The ZVS at turn-on of both switches is achieved because the switches only conduct when they are forward-biased. At turn-off, the rate of voltage rise on the switches is limited, leading to a near-ZVS condition. Figure 33(b) and Figure 34 are included to demonstrate that in the single-transformer embodiment, the link current is shared almost equally among the cells of a phase. Figure 33(b) shows the current through the switches of cells A_1 and A_2, whereas Figure 34 presents the ac bus currents of the two cells. The time scale of the Figure 33(b) and Figure 34 are selected to be very different to better demonstrate the current sharing capability. The windings associated with the two cells have leakage inductances of 5 and 2.82 μH. Even though there is a relatively large difference between the leakages, the cell currents

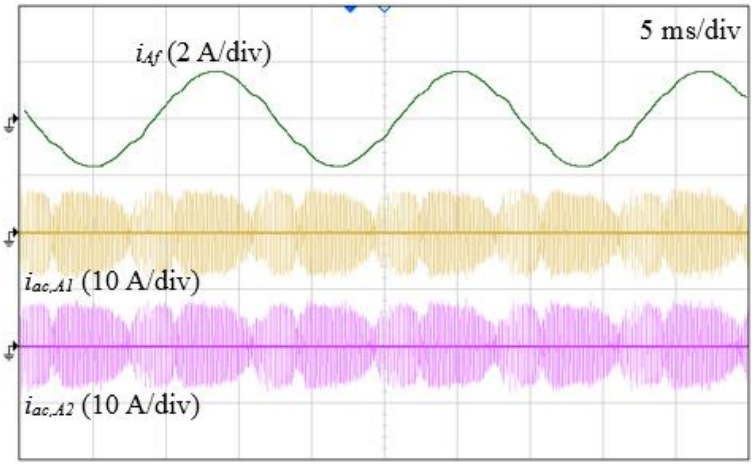
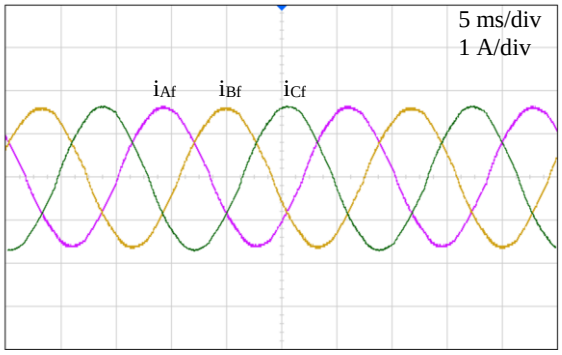
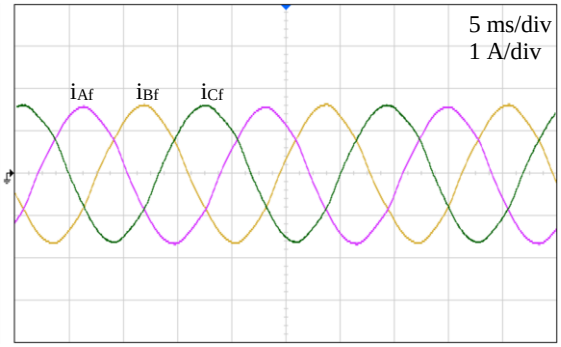


Figure 34 - Current sharing between the cells A_1 and A_2; i_{Af} is included as a time reference.



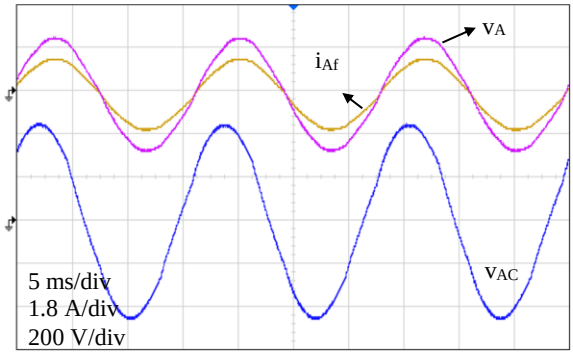
(a) Single-transformer embodiment



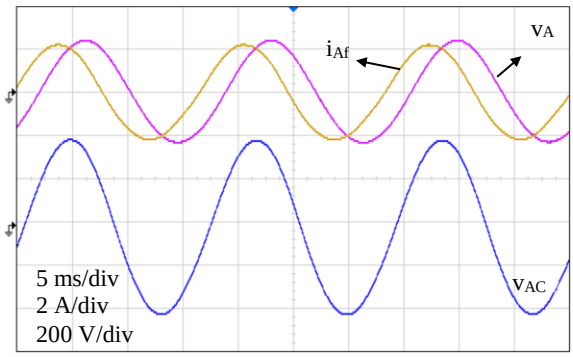
(b) Multiple-transformer embodiment

Figure 35 - Three-phase currents.

are almost equal throughout a line-to-line period. The sinusoidal output currents for the single-transformer are illustrated in Figure 35(a) at 750 W and unity power factor. The measured THD is 3.8 %. Figure 35(b) shows the output current of the multiple-transformer embodiment at 750 W and a lagging power factor of 0.87. The measured THD is 2.7 %. The American Weighted Efficiency of the multiple-winding transformer at an input voltage of 100 V and output voltage of 380 V^{rms} is 86 %. This efficiency is relatively low due to a non-optimum choice for the semiconductors in the prototype. The plots of phase current, phase voltage, and line voltage waveforms for two cases with unity and leading



(a) Power factor of unity



(b) Leading power factor of 0.6

Figure 36 - Three-phase currents.

power factors are shown in Figure 36. The waveforms in Figure 35 and Figure 36 show that the proposed converter is capable of regulating the output sine currents at lagging, unity, and leading power factors successfully.

The outputs of the current integrators of phase *A* are shown in Figure 37. These variables are internal to the digital controller and have been plotted on an oscilloscope using a digital to analog conversion method. While all integrator outputs originally have the dimension of electric charge, the values plotted here are normalized with respect to an arbitrary base.

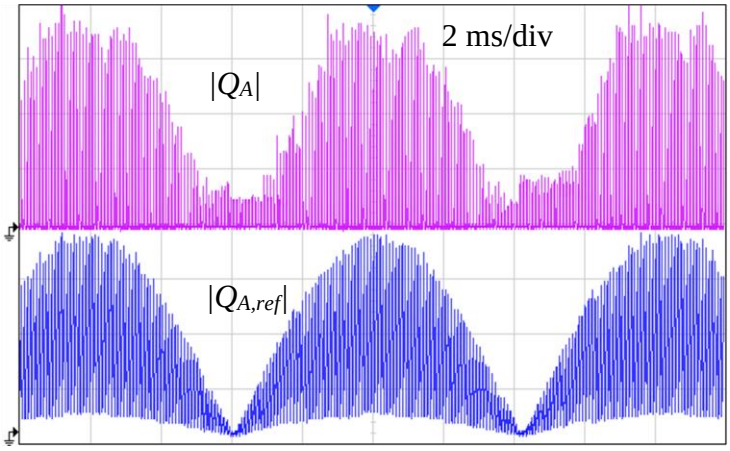
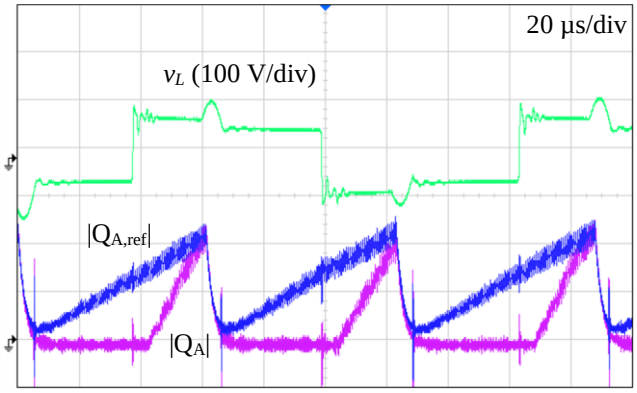


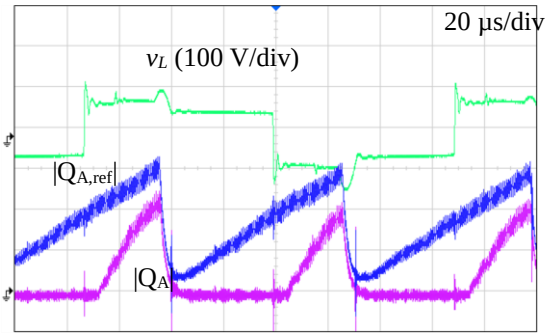
Figure 37 - Current shaping in the proposed inverter. The controller's task is to make the integrator output Q_A follow $Q_{A,ref}$ by adjusting the output switch conduction times.

The $|Q_{A,ref}|$ waveform is composed of several right triangles whose heights are proportional to the instantaneous value of phase *A* current reference, $i_{A,ref}$. The controller shapes the output phase currents by adjusting the output switch on-state durations so that $|Q_A|$ tracks $|Q_{A,ref}|$ as show in Figure 37. The plots of Figure 38 demonstrates $|Q_A|$ and $|Q_{A,ref}|$ in greater detail for a time span in which phase *A* has the largest current reference among all phases. The link voltage is included in the plots for clarity. As it was explained earlier is subsection 3.1.2, the link energy requirement at the end of mode 5 (and 11) is equivalent to the current regulation requirement provided that (40) is satisfied. Such a case is visible in Figure 38(a), in which $|Q_A|$ and $|Q_{A,ref}|$ meet at the end of mode 5 (and 11). In Figure 38(b), the output current reference is too large so that the right-hand side of (40) is greater than the left-hand side. Even though the link energy requirement is met at the end of mode 5 (and 11) by design, the current regulation is not. Figure 38(c), on the other hand, the converter

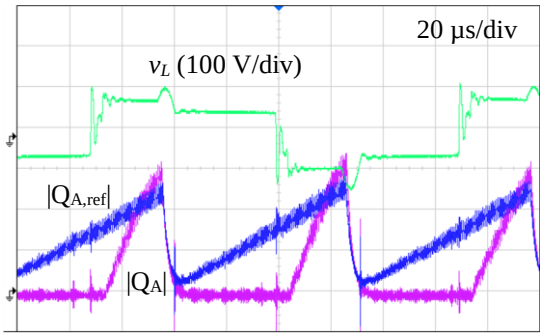
suffers from a too small output reference current. The mismatch between the integral values at the end of mode 5 (or 11) is used by the Output Current Reference Generator block to guarantee satisfaction of (40). As one can see in Figure 38, the link energy requirement successfully regulates the peak link voltage, V_{peak}, regardless of the status of (40). Without this requirement, the link energy may either be too large, which may exceed the components voltage ratings; or too small which may prevent soft-switching on the



(a) $|Q_A|$ meets $|Q_{A,ref}|$

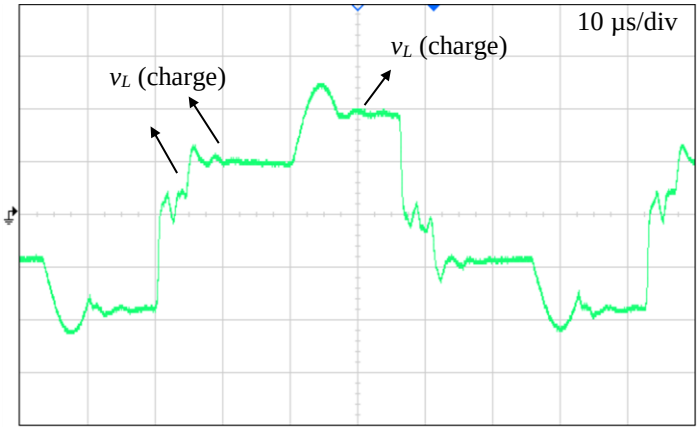


(b) $|Q_A|$ does not meet $|Q_{A,ref}|$, $\hat{I}_{o,ref}$ too large

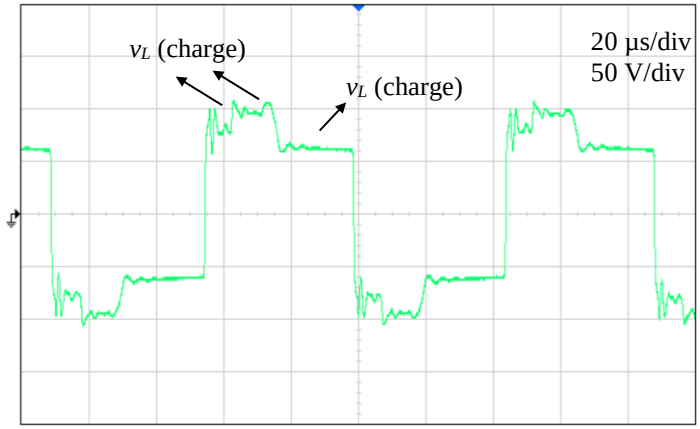


(c) $|Q_A|$ does not meet $|Q_{A,ref}|$, $\hat{I}_{o,ref}$ too small

Figure 38 - Current integrators outputs for phase *A*; a) Equation (40) is satisfied; b) Right-hand side in (40) outweighs left-hand side; c) Left-hand side in (40) outweighs right-hand side.



(a) Buck mode of operation



(b) Boost mode of operation

Figure 39 - Link voltage in buck and boost modes of operation; a) Vi = 100 V, V_{phase} = 80 V_{rms} at 125 W; b) Vi = 70 V, V_{phase} = 160 V_{rms} at 250 W.

input switches in buck mode of operation. As stated earlier, the proposed inverter may operate in buck or boost modes, as shown in in Figure 39.

The proposed inverter has a rapid current transient because there are no dc links included in the design. Figure 40 shows the phase current i_{Af}, link voltage v_L, and input current i_{if}

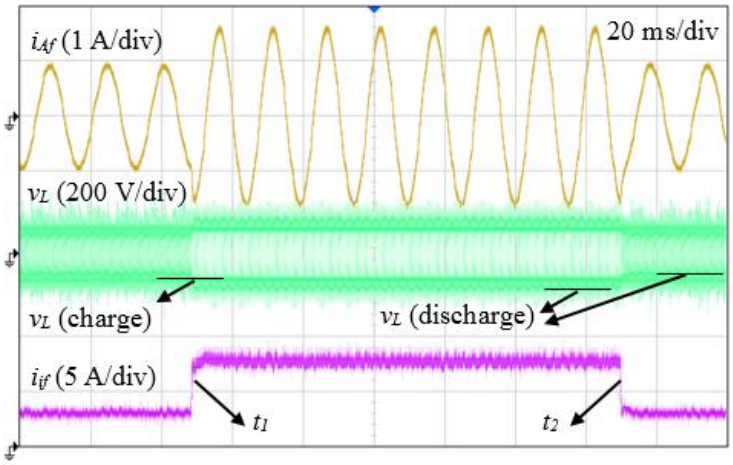
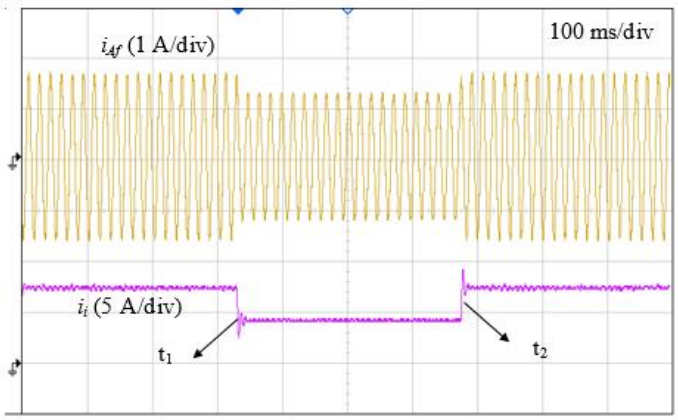


Figure 40 - Transient response of the inverter. In $[t_1,t_2]$ the converter works in boost mode. At other times operates in buck mode.

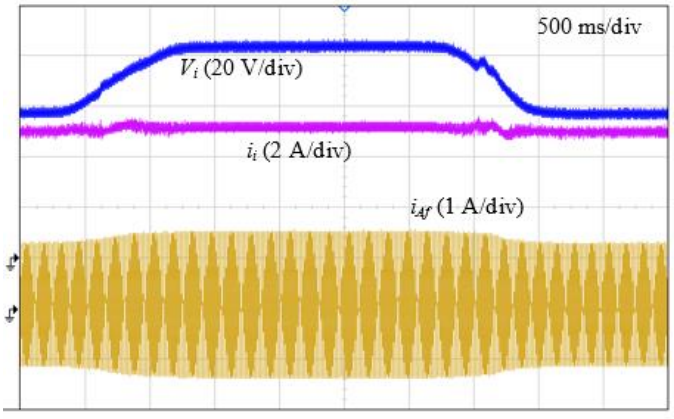
during transient operation of the single-transformer inverter. Prior to time t_1, the inverter operates in buck mode with V_i = 100 V and V_{LL} = 220 V at 250 W. At t_1, the input and output current references are stepped up manually so that the output voltage and power increase to V_{LL} = 380 V and 750 W, respectively. Between t_1 and t_2 the inverter operates in boost mode as labeled on Figure 41. Unlike a conventional dc-link inverter, the voltage of the ac link can change rapidly in response to a step change.

The final experimental tests verify the operation of the Current Reference Generator block of Figure 24. In a photovoltaic inverter, the input power to the inverter is subject to change due to voltage and current variations imposed by the solar irradiance or MPPT operation [55] [56]. The proposed inverter re-adjusts its output current reference magnitude, $\hat{I}_{o,ref}$, so that the power-balance equation presented by (40) is satisfied. In Figure 41(a), the input voltage is fixed at V_i = 100 V. The inverter initially operates at 390

W. At t_1 and t_2 the input current reference is rapidly increased and decreased by about 75%, respectively. Between t_1 and t_2 the inverter outputs 700 W. This test may simulates a severe change in the solar irradiance or a sudden change in the MPPT's decision. The output phase current successfully adapts to the change in the power as indicated in the figure. In Figure 41(b), the input reference current is maintained at 5.2 A, while the input



(a) Input current varies at fixed input voltage



(b) Input voltage swells to 104 V, sags to 78V at fixed input current

Figure 41 - Output current reference regulation in face of input current or input voltage variations.

voltage changes from 78 V to 104 V and back to 78 V. Despite the swell and sag in the input voltage, the inverter input current is able to track its reference. Moreover, the output current is dynamically regulated to maintain the input-output power balance.

3.2 Single-Ended Inverter[4]

3.2.1 Introduction

The multi-cell soft-switching inverter proposed in this section uses a high-frequency *LC* link as shown in Figure 42. Galvanic isolation is realized through a multiple-winding high-frequency transformer that can significantly reduce the overall size and weight of the system. The multi-cell structure on the secondary side allows the output switches to share the current as well as voltage stress. The need for bulky dc link components is eliminated by operating the ac link at a high frequency. The ac voltages on cell capacitors are inherently balanced by the transformer windings. This converter maintains ZVS conditions at every switch turn-on and near-ZVS conditions at every switch turn-off throughout the operating range, thereby decreasing the switching losses and *dv/dt*-induced EMI emissions.

[4] © ____ IEEE. Reprinted, with permission, from M. Moosavi and H. A. Toliyat, "A Multi-Cell Cascaded High Frequency Link Inverter with Soft-Switching and Isolation," in IEEE Trans. on Industrial Electronics, Submitted Sep 2016, **Revision Submitted.**

3.2.2 The Proposed Inverter

The schematic diagram of the proposed inverter is presented in Figure 42 [54]. There is one low-side semiconductor switch, S_i, on the input side which connects the input source to a winding of a multiple-winding transformer. On the output side, each phase is comprised of K series-connected H-bridge cells, each coupled to a transformer winding. All switches conduct unidirectional current and block voltages of both polarities. This can be achieved by using a reverse-blocking switch or simply by putting a diode in series with each switch. The high-frequency transformer has $3K+1$ windings, and the turn ratio from the input to an output winding is $1:N$. Each winding is connected in parallel to an ac capacitor, C_{xj}, where x denotes the terminal to which the winding belongs, and j is an index number. For example, C_{i1} is the only ac capacitor on the *input* side, and C_{AK} is the ac capacitor connected to the K^{th} winding of *phase A*. The magnetizing inductance L and the $3K+1$ ac capacitors C_{xj} form a parallel ac link, hereinafter referred to as *the link*. The inductor current i_L and voltage v_L are named the link current and link voltage, respectively. Except for a turn ratio multiplier, the voltage v_L represents the voltage on all link capacitors. Depending on the design requirements, the inverter may have a capacitive or inductive-capacitive filter on its input and output terminals. The latter is the case in Figure 42 with filter components L_x and C_x. Variable i_i denotes the unfiltered input current as well as the input switch current.

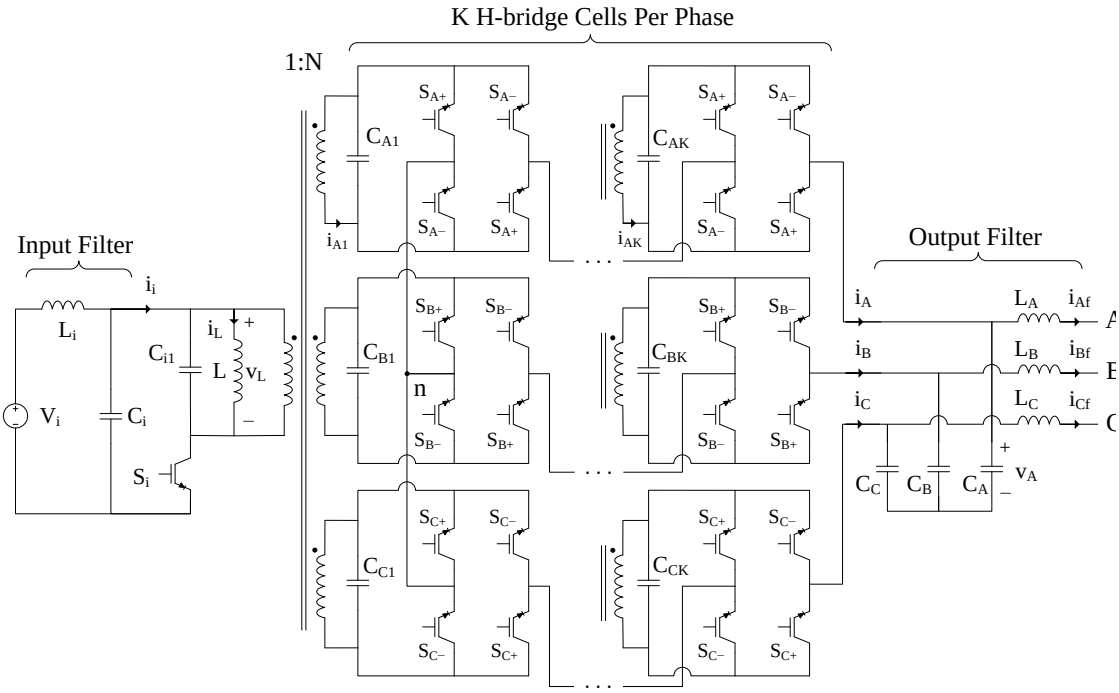


Figure 42 - The proposed soft-switching inverter with cascaded output cells.

Referring to the output side in Figure 42, i_x denotes the unfiltered current of phase x and v_x denotes the voltage on filter capacitor C_x. Switches in phase x are named either S_{x+} or S_{x-}. There are only two switch command lines per phase, and switches that receive the same command are given the same name. When S_{x+} (S_{x-}) switches in phase x conduct, the unfiltered phase current, i_x, is positive (negative). As shown in Figure 42, the leftmost H-bridge cells in the phases are connected to a common point n.

3.2.3 Operation of the Inverter

3.2.3.1 Description of the Modes

It was mentioned earlier that the inductance L and the $3K+1$ link capacitors, C_{xj}, form a parallel resonant link. An operation cycle of the proposed inverter, $T_{Link}=1/f_{Link}$, is composed of six modes as shown in Figure 43. The link charges from the input in mode 1, and discharges onto the output phases in modes 3 and 5. The even-numbered modes 2,

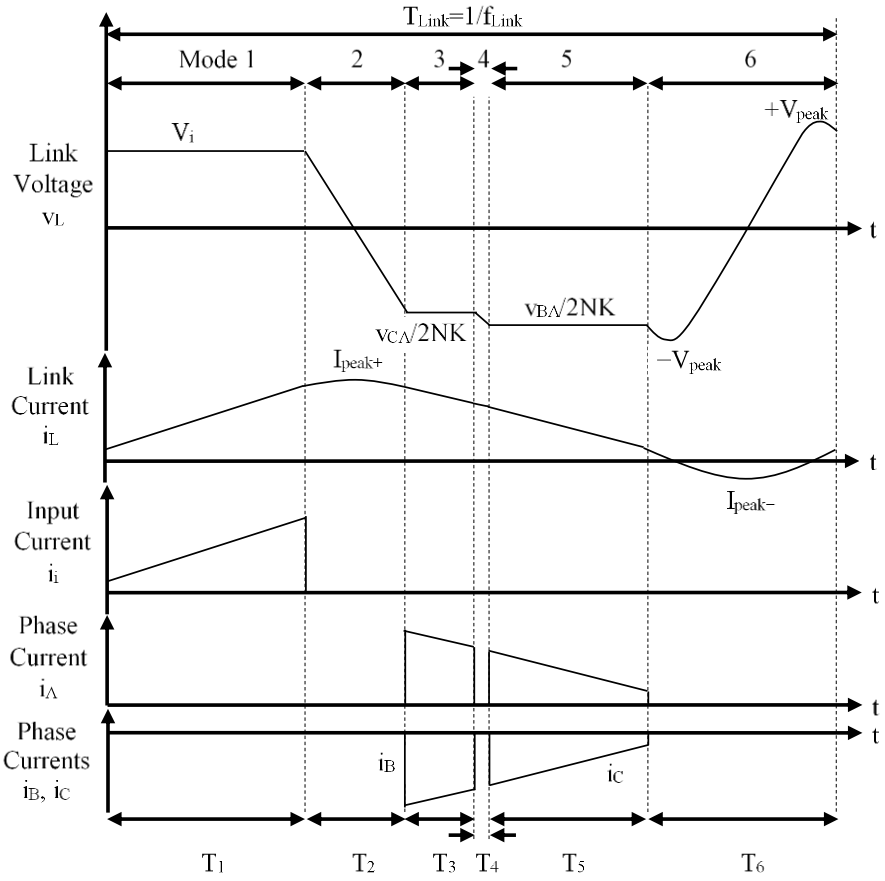
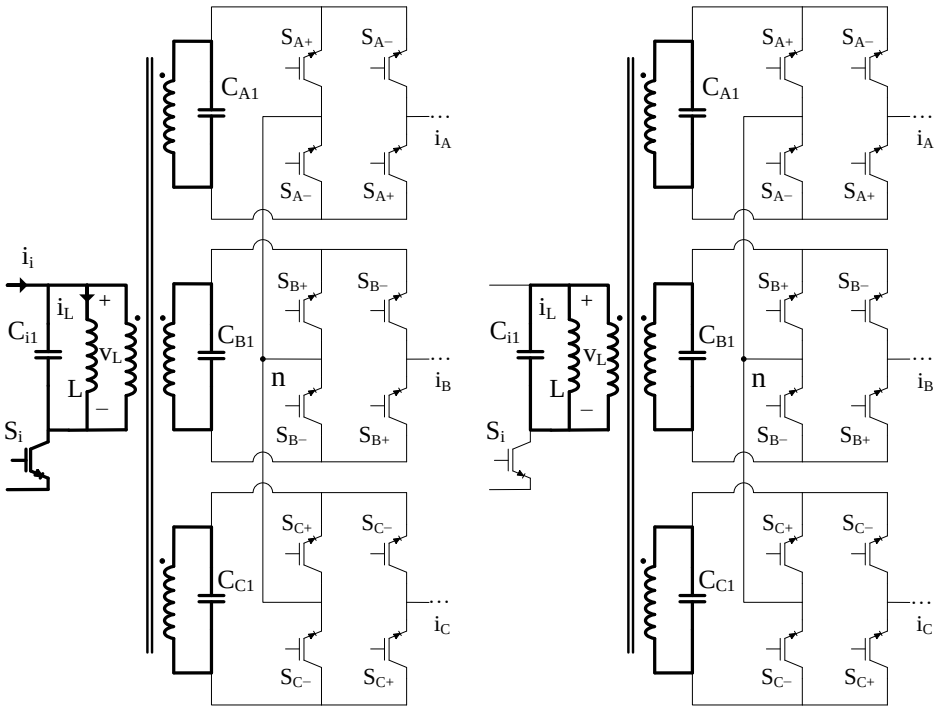


Figure 43 - Operating waveforms and six modes of the proposed inverter. Voltage labels for modes 3 and 5 show an example where $i_{ABC,ref}$= {0.9,−0.1,−0.8} pu and v_{ABC}={0.6,−0.9,0.3} pu.



(a) Charge mode 1 (b) Resonant modes 2, 4, & 6

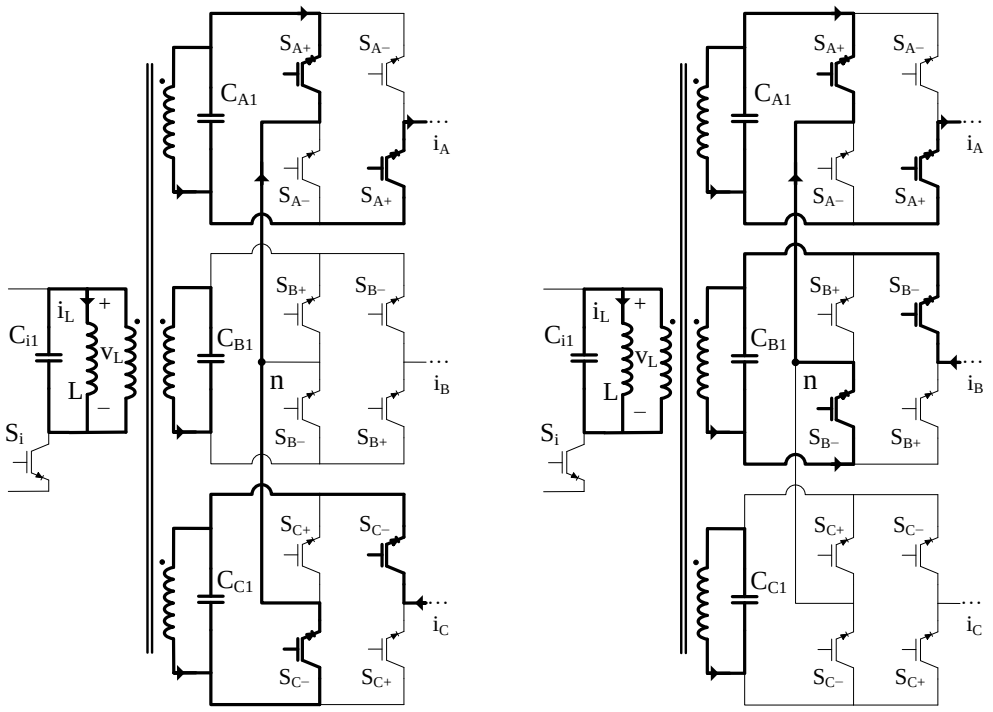
Figure 44 - Current path in different modes. Only one cell per phase is shown. Modes 3 and 5 are shown for an example where $i_{ABC,ref}$= {0.9,−0.1,−0.8} pu and v_{ABC}={0.6,−0.9,0.3} pu.

4, and 6 are resonant modes in which no energy transfer occurs. In each link cycle, the controller tries to meet the input dc current reference, $I_{i,ref}$, and the sinusoidal output references $i_{A,ref}$, $i_{B,ref}$, and $i_{C,ref}$. Therefore, the input current, i_i, and the three output currents i_A, i_B, and i_C should be monitored by the controller. With reference to Figure 43, these four current waveforms are unfiltered currents with a trapezoidal shape. Therefore, the goal for the controller is to operate the switches in a way that the *average values of these currents* track their references. The controller samples the currents at several points in a switching

cycle so that it can calculate the average values and compare them with their references. The following paragraphs describe the modes. For the sake of simplicity, all components are assumed to be ideal.

Mode 1: In reference to Figure 44(a), the link inductor is charged by the source through S_i. All other switches are in their blocking state. The link voltage, v_L, equals V_i, and the link current, i_L, increases linearly, as shown in Figure 43. Once the average input current reference is met, S_i is gated off. In this section, the *average* value of a variable is calculated over a switching cycle of length T_{link} as indicated in Figure 43. Due to the presence of S_i between two capacitors C_i and C_{i1}, the rate of voltage rise on S_i at turn-off is effectively limited. Therefore, the switch current reduces before its voltage can rise. This near ZVS condition significantly reduces the turn-off loss.

Mode 2: No switches conduct in this mode, therefore the link resonates and v_L changes polarity, as depicted in Figure 43. The current i_L experiences its positive peak I_{peak+} in this mode. The path of link current is shown in thick lines in Figure 44 (b). On the output side, two phases should be selected to receive energy in mode 3. Out of the three possible phase pairs AB, BC, and AC, the pairs which accommodate the phase with the largest current reference magnitude are candidates for conduction in mode 3. Out of these two pairs, the one with the smaller voltage difference magnitude is selected for mode 3, and the other pair is selected for conduction in mode 5. This leads to a descending link voltage sequence in modes 3, 4, and 5 as shown in Figure 43, which is an essence in having zero-voltage turn-on. For example, when $i_{ABC,ref}$= {0.9,−0.1,−0.8} pu, and v_{ABC}={0.6,−0.9,0.3} pu, then the pair AC conducts in mode 3, and pair AB conducts in mode 5.



(c) Discharge mode 3 (d) Discharge mode 5

Figure 45 - Current path in different modes. Only one cell per phase is shown. Modes 3 and 5 are shown for an example where $i_{ABC,ref}$= {0.9,−0.1,−0.8} pu and v_{ABC}={0.6,−0.9,0.3} pu.

Mode 3: The link is to be discharged on the output pair selected in mode 2. Switches in the selected phase pair should conduct in a way that the polarity of current in the conducting phases matches the polarity of their references. Figure 45(a) shows the current path for the example made in mode 2. Switches named S_{A+} and S_{C-} conduct in Figure 45(a) because the current references for phases A and C are positive and negative, respectively. A quick glimpse of Figure 44 (a) proves that a total of *2K* H-bridge cells are connected in series in mode 3, each having a capacitor voltage of Nv_L. Therefore, their

aggregate link voltage is $2NKv_L$. The switches of mode 3 start conducting only when they are forward biased, i.e., when their aggregate link voltage matches the pair's instantaneous line-to-line voltage. This means in our earlier example, the switches do not conduct until the negative link voltage, v_L, reaches the value $(v_C - v_A)/2NK$. This ensures zero-voltage turn-on for all conducting switches. i_L reduces linearly as shown in Figure 43. This mode goes on until one of the conducting phases, namely the phase with the smaller current reference, meets its current reference. In our example, it would be phase C. This means that mode 3 ends when the average value of the current i_C in Figure 43, i.e., the area under the i_C trapezoid divided by the cycle length, meets its sinusoidal reference. It is worth mentioning that even though the sinusoidal references change in time, it is reasonable to assume that they are constant within a switching cycle because the switching period is much shorter the sine period. This carefully designed *end criterion* for mode 3 shapes phase *C* current into a sine wave because the reference current is a sinusoidal. At the end of this mode the switches are gated off. Following the turn-off, the link starts resonating. The voltage rise on the switches happens slowly because of the link capacitors. This allow the switch currents to fall at a near zero voltage and significantly reduces the turn-off loss.

Mode 4: No switches carry current and the link resonates as shown in Figure 43 and Figure 44(b). The negative v_L increases in magnitude, until the aggregate link voltage $2NKv_L$ equals the instantaneous line-to-line voltage of the selected output pair of mode 5. In our example, the switches conduct as soon as the negative link voltage, v_L, reaches the value $(v_B - v_A)/2NK$. Again this guarantees a zero voltage turn-on for the conducting switches. This ends mode 4 and starts mode 5.

Mode 5: The switches corresponding to the selected pair discharge the link, as shown in Figure 43. The selection process of the output pair was explained earlier in mode 2. Similar to mode 5, switches in the conducting phase pair should be selected in a way that the polarity of current in the conducting phases matches their references. Figure 45(b) shows the current path for the example set forth in mode 2. Switches named S_{A+} and S_{B-} conduct in Figure 45(b) because the current references for phases A and B are positive and negative, respectively. Mode 5 continues until the energy in the link drops to a pre-determined level, $E_{desired}$, which will be elaborated later. This mode ends by turning off all switches. Similar to mode 3 following the turn-off, the voltage rise on the switches happens slowly because of the link capacitors. This allow the switch currents to fall at a near zero voltage and significantly reduces the turn-off loss.

Mode 6: No switches carry current in this mode. With the left-over energy from mode 5 the link resonates and experiences its negative and positive peaks $\pm V_{peak}$, as shown in Figure 43 and Figure 44(b). This mode ends when the link voltage equals the input voltage V_i. This is a perfect moment for S_i to turn on at zero voltage. After mode 6, the converter starts mode 1 and repeats the cycle.

The control block diagram of the proposed inverter is depicted in Figure 46. The controller's main task is to monitor the *end criteria* that were explained in the above paragraphs and identify the moment in which a mode should end so that the following mode can begin. The Moving Average blocks in the diagram calculate the area below their input waveform, therefore they are simple digital integraters. These integrators are re-set to zero periodically at the end of their corresponding modes to prepare for the next link

cycle. The block diagram also indicates the controller requires samples of five currents, namely i_i, i_A, i_B, i_C, and i_L. However, it does not imply that five current sensors are required. This is because the waveforms of i_i, i_A, i_B, i_C are actually included in the waveforms of i_L, as indicated in Figure 43. For example, one can verify that the input current i_i matches i_L in mode 1, and the phase current i_A matches the link current i_L in modes 3 and 5.

3.2.3.2 Considerations

Since the link inductor is separated from the output terminals during the charge mode and is separated from the input terminal during the discharge modes, it is inherently a buck-boost converter. The inverter is considered to be a buck inverter when v_L in mode 5

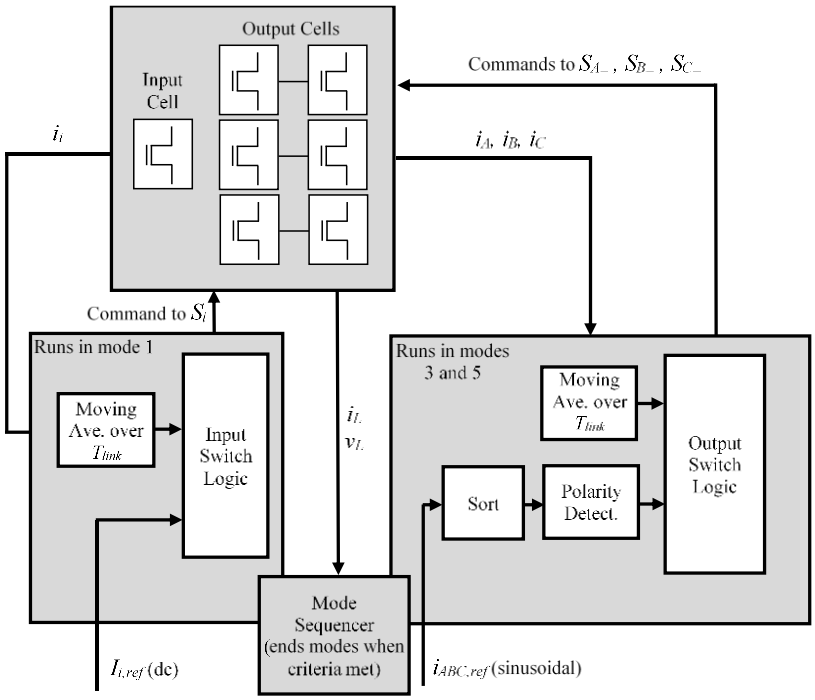


Figure 46 - Control block diagram of the proposed inverter.

is smaller in magnitude than the V_i. Otherwise it is considered a boost inverter. The six modes and the control of the converter in both cases are exactly the same.

From the above paragraphs, it can be inferred that the input switch, S_i, switches at the link frequency f_{Link}. The output switches that belong to the phase with the largest current reference switch at $2f_{Link}$ because they conducts in modes 3 and 5, whereas the output switches corresponding to the other two phases switch at f_{Link} because they conduct in mode 3 or 5.

The link energy at a point in time, E, is defined as:

$$E = \frac{1}{2} C_{tot} v_L^2 + \frac{1}{2} L i_L^2, \tag{69}$$

where C_{tot} is the total link capacitance as seen from the input-side winding. Assuming that all output-side link capacitors have the same value of C_{A1}, C_{tot} is:

$$C_{tot} = C_{i1} + 3KN^2 C_{A1}. \tag{70}$$

It was mentioned earlier in the description of mode 5 that the requirement to end this mode is that the total link energy in the link reduce to a desired level $E_{desired}$. This guarantees that the same amount of energy that was delivered to the link in mode 1 leaves the link in modes 3 and 5, thereby indirectly balancing the input and output power in every cycle.

Following mode 5, the link resonates in mode 6 at the link resonant frequency, ω_{res}:

$$\omega_{res} = \frac{1}{\sqrt{LC_{tot}}}. \tag{71}$$

Since no power is transferred to the output in mode 6, the link energy in this mode remains essentially constant. Noting that at peak voltages, $\pm V_{peak}$, the link current is zero, one can find the link peak voltage as a function of $E_{desired}$:

$$V_{peak} = \sqrt{\frac{2E_{desired}}{C_{tot}}}. \tag{72}$$

It is recommended to use the lowest possible value for $E_{desired}$ and V_{peak}. This is because a large V_{peak} requires a higher voltage rating for the components, makes modes 6 too lengthy, and unnecessarily reduces the link frequency. A very small V_{peak}, on the other hand, may make mode 6 too short to such an extent that the digital controller cannot detect the end of mode 6. Care must be taken on selection of $E_{desired}$ when the inverter operates as a buck inverter. In this case according to mode 6 in Figure 43, v_L should travel from a smaller value to a larger value, V_i. If there is not enough energy in the link, it can never reach V_i, and ZVS will not be achieved at the turn-on of S_i. In boost mode, however, V_{peak} is greater than V_i by definition. Therefore regardless of buck or boost operation, V_{peak} should not be smaller in magnitude than the bigger of V_i and v_L of mode 5.

3.2.4 Inverter Design Considerations

3.2.4.1 Analysis of the Inverter

The link frequency, f_{Link}, is a function of the circuit parameters and the operating point. This section presents a detailed analysis of the converter and can be employed during the design phase. Specifically, this analysis establishes a relation between the link parameters,

the point of operation, transformer turn ratio, and key variables such as f_{Link} and I_{peak+}. The following assumptions are made during this analysis:

- In the charge and discharge modes (odd-numbered modes) the transformer winding resistances are factored into the equations. However, since the link capacitor voltages are essentially constant in this mode as shown by v_L in Figure 43, all link capacitor currents are almost zero and thereby ignored. This removes the capacitors from the circuit model and reduces the circuit order to 1, but causes a highly negligible error.
- In resonant modes, winding resistances are ignored because the impedances of link capacitors are larger than the winding resistances by at least three orders of magnitude (See Table IV). This reduces the circuit order to 2.
- Voltage ripples on the input and output filter capacitors and voltage drop on the switches are ignored.
- Unless mentioned otherwise, variable t in the equations of a mode is the time elapsed since the start of the mode. Initial conditions for i_L and v_L at the start of mode m are denoted by $I_{m,0}$ and $V_{m,0}$, respectively.
- As shown in Figure 43, mode 4 is very short. Therefore it is not factored in the equations and modes 3 and 5 are combined. The link voltage in modes 3 and 5 is a function of time and repeats every $\pi/3$ radians. However, the average v_L in the combined mode, $V_{3,5}$ is derived in (41).

$$V_{3,5} = \frac{3}{2\pi K}\hat{V}_o \int_{-\frac{\pi}{6}}^{\frac{\pi}{6}} [\cos\theta - \frac{\cos(\theta + 2\pi/3) + \cos(\theta - 2\pi/3)}{2}]\, d\theta$$
$$= \frac{1.432}{2K}\hat{V}_o, \tag{73}$$

where $\hat{V}_o$ is the output peak phase voltage. According to Figure 43, the link period is:

$$T_{Link} = \frac{1}{f_{Link}} \approx T_1 + T_2 + (T_3 + T_5) + T_6. \tag{74}$$

Assuming that the resistance of the input winding is R_i, the link voltage and current for mode 1 are readily derived.

$$\begin{cases} v_L(t) = V_i - R_i i_L & (75) \\ i_L(t) = \frac{V_i}{R_i} + \left(I_{1,0} - \frac{V_{in}}{R_i}\right) e^{-\frac{R_i}{L}t} & (76) \end{cases}$$

Since no switches conduct during resonant modes 2 and 6, the link reduces to a second order LC circuit. Taking i_L and v_L as state variables, the following equations are derived from the equivalent circuit:

$$i_L + C_{tot} L \frac{d^2 i_L}{dt^2} = 0 \tag{77}$$

$$v_L(t) = L\frac{di_L}{dt}. \tag{78}$$

From (77) and (78), the solution to link variables during resonant modes is:

$$\begin{cases} i_L(t) = I_{m,0}\cos(\omega_{res}t) + V_{m,0}\sqrt{\frac{C_{tot}}{L}}\sin(\omega_{res}t) & (79) \\ v_L(t) = -L\omega_{res} I_{m,0}\sin(\omega_{res}t) + V_{m,0}\cos(\omega_{res}t). & (80) \end{cases}$$

Similar to mode 1, and assuming winding resistance of R_o for each output-side winding, in the combined modes 3 and 5 the link equations are:

$$\begin{cases} v_L(t) = -\dfrac{V_{3,5}}{2NK} - \dfrac{R_o}{2N^2K}\, i_L & (81) \\ i_L(t) = \dfrac{-V_{3,5}N}{R_o} + \left(I_{3,0} + \dfrac{V_{3,5}N}{R_o}\right) e^{\frac{-R_o}{2N^2KL}t}. & (82) \end{cases}$$

So far the equations for i_L and v_L in every mode are obtained. These equations, together with the description of modes lead to a set of simultaneous equations presented by (49-53). Unknowns are T_1, T_2, T_3+T_5, T_6, and $I_{1,0}$.

$$\begin{cases} I_{i.ref}T_{Link} = \dfrac{V_i}{R_i}T_1 + \dfrac{L}{R_i}\left(I_{1,0} - \dfrac{V_i}{R_i}\right)\left(1 - e^{-\frac{R_i}{L}T_1}\right) & (83) \\ V_{3,0} = -L\omega_{res}I_{2,0}\sin(\omega_{res}T_2) + V_{2,0}\cos(\omega_{res}T_2) & (84) \\ \dfrac{1}{2} \times \left(LI_{6,0}^2 + C_{tot}V_{6,0}^2\right) = E_{desired} & (85) \\ V_{1,0} = -L\omega_{res}I_{6,0}\sin(\omega_{res}T_6) + V_{6,0}\cos(\omega_{res}T_6) & (86) \\ -I_{1,0} = I_{6,0}\cos(\omega_{res}T_6) - V_{6,0}\sqrt{\dfrac{C_{tot}}{L}}\sin(\omega_{res}T_6) & (87) \end{cases}$$

Equations for the undefined $V_{m,0}$ and $I_{m,0}$ are listed in the Appendix. Equations (49-53) are in order: current reference requirement at mode 1, voltage requirement at the end of mode 2, link energy requirement at the end of the combined modes 3 and 5, voltage requirement at the end of mode 6, and current symmetry at start of mode 1 and end of mode 6. Once a solution is obtained, I_{peak+} can be derived from (54).

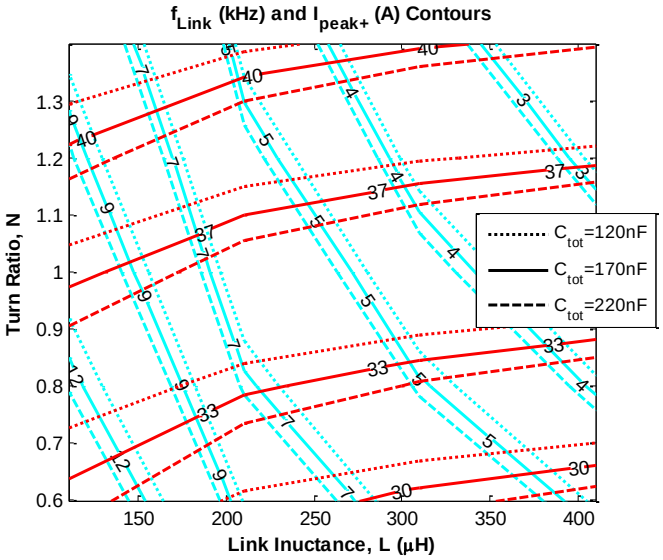


Figure 47 - Contours of f_{Link} in blue at {3,4,5,7,9,12} kHz and contours of I_{peak+} in red at {30,33,37,40} A for V_i=100 V, V_{LL}=380 V at 780 W.

$$\frac{1}{2}LI_{peak+}^2 = \frac{1}{2} \times \left(C_{tot}V_{2,0}^2 + LI_{2,0}^2\right) \tag{88}$$

Figure 48 presents the converter design plots at the input voltage of 100 V, output line to line voltage of 380 V^{rms}, and output power of 780 W. Selected values for C_{tot} in the plots are 120, 170, and 220 nF. The plots in this figure are valuable during the design phase because they show the effects of three parameters, namely L, N, and C_{tot} on link peak current, I_{peak+}, and link frequency, f_{Link}. The link peak current is an important variable as it determines the transformer's maximum flux, transformer core loss, and the current rating of the input and output switches. I_{peak+} changes only slightly as C_{tot} increases. This is expected because the link capacitors are only in charge of providing soft-switching conditions for the semiconductors. A larger value for C_{tot} results in a slightly larger I_{peak+}

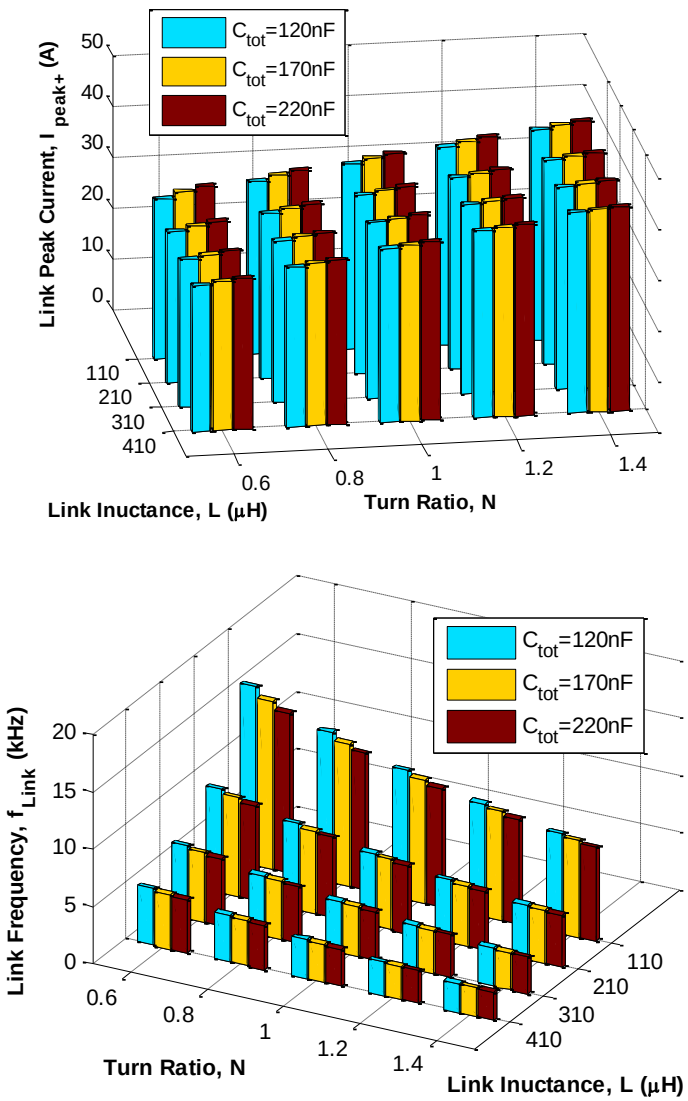


Figure 48 - Link peak current (top) and link frequency (bottom) for various values of N, L, and C_{tot} for V_i=100 V, V_{LL}=380 V at 780 W.

because it supplies more energy to the link inductor during mode 2. N and L affect I_{peak+} as well; however, the effect of N is more significant. As long as current rating of the input switch (and therefore I_{peak+}) is the concern, smaller values of N are more favorable.

Figure 48 also depicts f_{Link} against L and N for three different values of C_{tot}. f_{Link} is the key variable of this inverter mainly because it determines the sampling time of the digital controller, controls transformer core loss, and affects the size of terminal filters. The effect of C_{tot} is considerable only on the duration of the resonant modes, i.e., T_2, T_4, and T_6. That is why the link frequency is not sensitive to the variation in C_{tot}. L, on the other hand, has a substantial effect on f_{Link} due to its active role in determining the duration of every mode. A larger L lengthens every mode and reduces the link frequency. In addition, an increase in N prolongs the discharge modes 3 and 5 and reduces the link frequency because the link discharge voltage in these modes, $V_{3,5}/2NK$, is inversely proportional to N.

The above discussion suggests that smaller values for L, N, and C_{tot} are generally more favorable as they lead to higher values for f_{Link} as well as the switching frequency. An increase in the switching frequency, especially in a soft-switching converter, is welcome because it reduces the size of filter components and results in smoother terminal waveforms. Nonetheless too small values for L, C_{tot}, and N necessitate a digital controller with a very high sampling frequency. Also a small N increases the reflected voltage on the input-side switch and calls for a higher voltage rating for that switch. Figure 47 shows the contour plots of I_{peak+} and f_{Link} for different values of C_{tot} at the same terminal values as that of Figure 48. The significance of this plot is that it offers almost all important parameters and variables of the inverter within the same graph. One can quickly select the values for L, C, and N for a design that targets a specific link frequency and switch current rating.

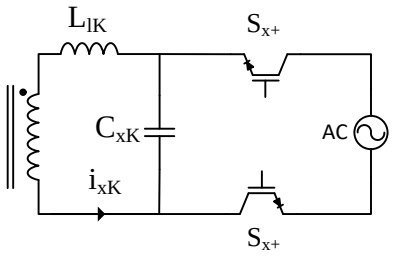


Figure 49 - Simplified equivalent circuit of a cell *K* of phase *x* to consider the effect of output winding leakage inductance of cell power sharing.

3.2.4.2 Switch Voltage and Current Stress

Although resonant and partial resonant converters exhibit a superior performance over hard-switching converters in terms of switching losses and EMI emissions, they often result in a higher stress on the components and semiconductor devices. The most notable advantage of having a cascaded series of H-bridge cells on the output side of the proposed inverter is the reduction on the output side switch ratings. This reduction happens on the voltage rating as well as current rating.

The maximum current through an output switch happens in mode 3 simply because the link current in this mode is larger than in mode 5. According to Figure 45(a), the link inductor is discharged through *2K* H-bridge cells. Each cell receives one over $2K^{th}$ (*1/2K*) of the link current. Making a conservative assumption that the current at the start of mode 3, $I_{3,0}$, is almost equal to the link peak current I_{peak+}, the maximum current that an output switch has to conduct, I_{stress}, is:

$$I_{stress} = \frac{I_{peak+}}{2NK}. \tag{89}$$

The maximum voltage stress on an output-side switch, V_{stress}, happens in mode 6 because this mode accommodates the link peak voltage. A KVL equation on the loop shown in thick lines in Figure 45(a) finds this voltage as a function of time:

$$\begin{aligned} V_{stress} &= \frac{1}{2N} V_{peak} + \frac{1}{2K} \hat{V}_o \sin(\omega_o t)\,, 0 < \omega_o t < \pi, \\ V_{stress} &= \frac{-1}{2N} V_{peak} + \frac{1}{2K} \hat{V}_o \, sin(\omega_o t)\,, -\pi < \omega_o t < 0. \end{aligned} \tag{90}$$

where ω_o is the phase angular frequency and t is time elapsed after an appropriate reference. It was mentioned earlier that under boost operation, V_{peak} can be equal to v_L of mode 5. In reference to Figure 43, the maximum absolute value for v_L in mode 5 is the one over $2K^{th}$ ($1/2K$) of the peak line-to-line voltage. Therefore one can rewrite (90) for boost mode as:

$$\begin{aligned} V_{stress} &= \frac{1}{2K} \hat{V}_o \left(\frac{\sqrt{3}}{2N} + \sin(\omega_o t) \right), 0 < \omega_o t < \pi, \\ V_{stress} &= \frac{1}{2K} \hat{V}_o \left(-\frac{\sqrt{3}}{2N} + \sin(\omega_o t) \right), -\pi < \omega_o t < 0. \end{aligned} \tag{91}$$

Equations (89, 91) show that the voltage and current stress on the output-side switches decrease linearly as the number of cells per phase, K, increases.

3.2.4.3 Leakage Inductances and Current Sharing

In certain multiple-winding topologies where the magnetizing inductance has to discharge onto several output windings, the leakage inductances may disturb the balance

in current sharing among the windings. For example, an ideal conventional multiple winding fly-back converter with equal number of turns on the output windings has an inherent tendency to balance the cell output voltages equally. This is because the diodes in the cells with lower voltages start conducting sooner than other cells, receiving a bigger share of the magnetizing current. However, in a practical case this beneficial tendency is severely fought against by the unequal leakage inductances of the output windings. This is because at the moment the diodes in a conventional fly-back converter start conducting, the leakage inductances of the output windings are supposed to start carrying the link peak current. Therefore, the leakage inductances currents at turn-on of the diodes have to suddenly rise from zero to their peak value. This sudden change in current is resisted by the leakage inductances and the cells with larger leakages will receive a smaller share of current. This problem, however, does not exist in the inverter proposed in this section due to the presence of the link capacitors. Prior to conduction of the output switches, the leakage inductances are softly pre-charged to their peak current by the magnetizing inductance, and as soon as the switches conduct, the current flows to the output filter capacitors. Prior to conduction of the output switches, current in the leakage inductances match closely, because these currents are mainly determined by the large impedances of the link capacitors and not by the small impedances of the leakage inductances. For example, Figure 49 shows a simplified schematic of output cell K of phase x at a moment prior to conduction of switches S_{x+}. In the experiments of this section the typical values for the output winding leakage impedance, $\omega_{res}L_{lK}$, and the link capacitor impedance, $1/\omega_{res}C_{xK}$, are 1.1 Ω and 1333 Ω, respectively.

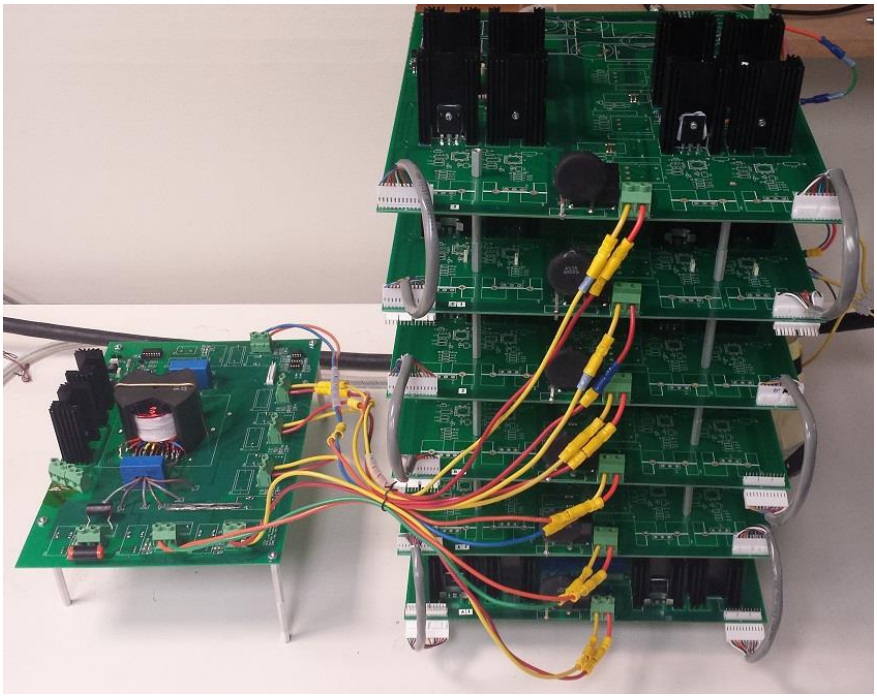


Figure 50 - Photograph of the inverter.

3.2.5 Experimental Results

A 780 W setup with two H-bridge cells per phase (K=2) is built and tested to verify the operation of the proposed inverter as depicted in Figure 50. The inverter specifications and component values used in the inverter are listed in Table I. The link current and voltage along with the unfiltered input current are shown in Figure 51. The selected link peak voltage is 135 V. The measured link frequency and link peak current are 12.1 kHz and 36 A, respectively. The values predicted by Figure 48 are 11.6 kHz and 35.8 A, which are in agreement with the experimental results. By examining the waveform v_L, one can

TABLE V. INVERTER AND COMPONENT SPECIFICATIONS AND NOMINAL VALUES

Output Power	780 W
Input Voltage (V_i)	100 V
Line Output Voltage (V_{LL})	380 V^{rms}
Output Frequency	60 Hz
Link Inductance (L)	110 µH
Total Link Capacitance (C_{tot})	120 nF
Link Resonant Frequency ($\omega_{res}/2\pi$)	43.8 kHz
Input Filter (L_i, C_i)	10 µH, 1 mF
Output Filter (L_x, C_x)	0 µH, 5 µF
Input Switch (S_i)	IXFH60N65X2 (MOSFET)
Output Switches (S_{x+}, S_{x-})	IRG7PH42UD (IGBT)
Transformer Core	PM-74×59 (N27)
Transformer Turn Ratio (N)	1
Digital Controller	TMS320F28335

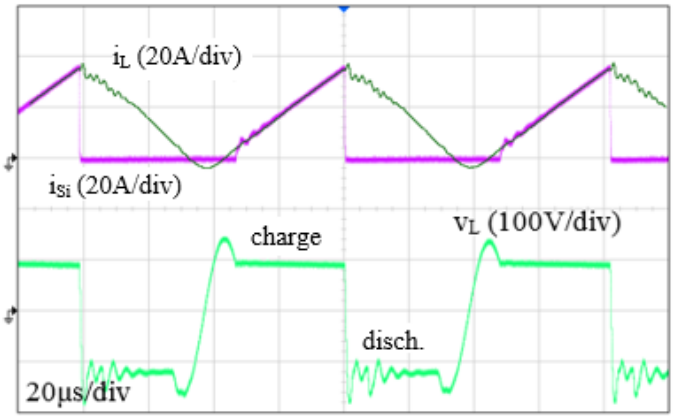
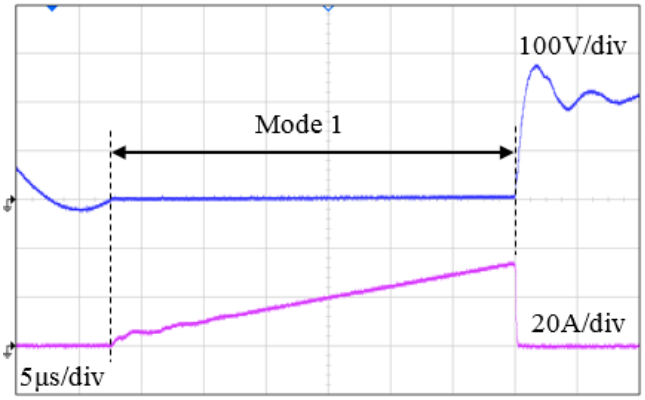
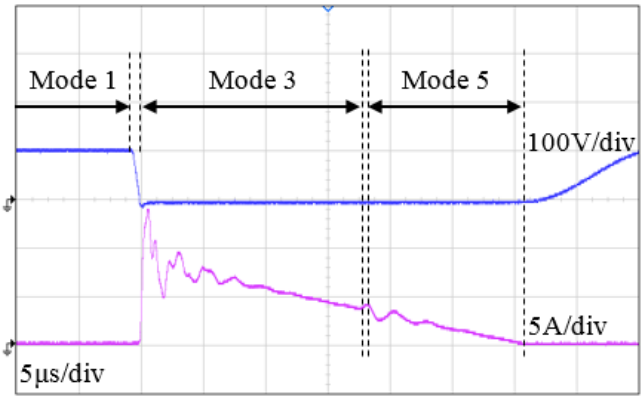


Figure 51 - Link current, link voltage and unfiltered input current at operating conditions of Table V (boost mode).

verify that the link discharge voltage is greater in magnitude than the link charge voltage.



(a) input switch voltage and current

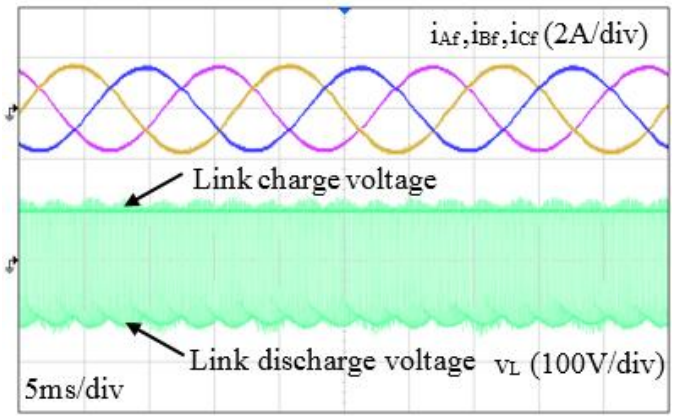


(b) output switch voltage and current

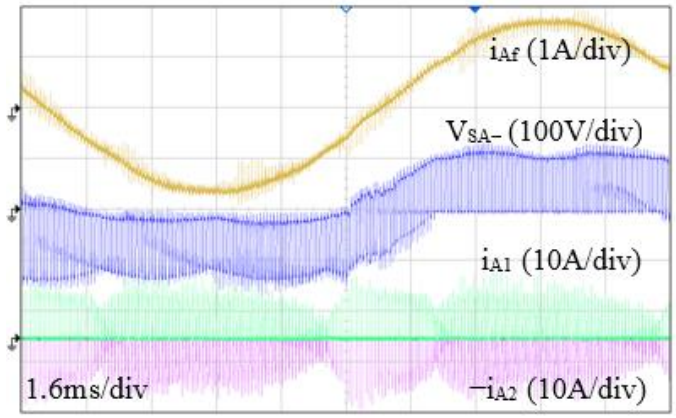
Figure 52 - Switching waveforms

This indicates that individual cells are operating in *boost mode*. An example of the *buck mode* will be presented later in this section.

Figure 52 shows the input and output switch waveforms. Due to the resonance of the link in even-numbered modes, all switches turn on at zero voltage. Also, the presence of link capacitors in parallel with every winding creates near ZVS conditions at turn-off of all switches. The leakage inductances of the transformer result in oscillations in the link



(a) Inverter output currents and link voltage



(b) Inverter output current, output switch voltage stress, and output winding current sharing.

Figure 53 - Overall performance of the inverter at unity power factor and operating conditions of Table V.

and switch waveforms. However, they do not interfere with the soft-switching of the semiconductor devices.

The sinusoidal currents generated by the inverter are presented in Figure 53(a). The high-frequency link voltage is shown in this figure to verify the average link discharge voltage predicted by (41). At the output line-to-line voltage of 380 V^{rms}, the value for $V_{3,5}$

from (41) is 111 V which is corroborated by Figure 53(a). The measured efficiency of the inverter is 92.5%. (The authors would like to mention to the reviewers that this efficiency is a little lower than the expected efficiency of the proposed topology because in this prototype 1200 V IGBTs are used as output side switches. Such switches contribute significantly to the conduction losses).

Figure 53(b) shows the phase A output current and switch S_{A-} voltage. The predicted value for maximum output switch voltage from (90) for V_{peak}=135 V is 142 V which closely matches the experimental results. On the same figure, the winding currents through cells 1 and 2 of phase A are plotted for a period of output current. The leakage inductances for these two cells are measured to be 5 and 2.82 μH, respectively. Although the leakages are significantly different, Figure 53(b) shows that the current is divided equally between the cells. Therefore, the output cells share the power equally.

It was mentioned earlier that in Figure 51, the cells operate in boost mode. If the requested output voltage by the load is small, the cells may operate in buck mode individually (the total output voltage may still be greater than the input voltage due to existence of more than one cell per phase). Figure 54 shows the link variables while the inverter operates in buck mode. The operation and control of the converter in boost and

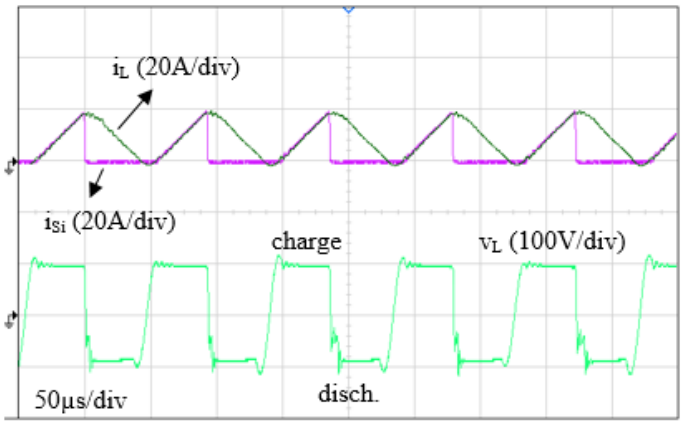


Figure 54 - Link current, link voltage and unfiltered input current at V_{in}=100 V, V_{LL} = 230 V^{rms} at 310 W for L=188 µH and C_{tot} = 110 nF.

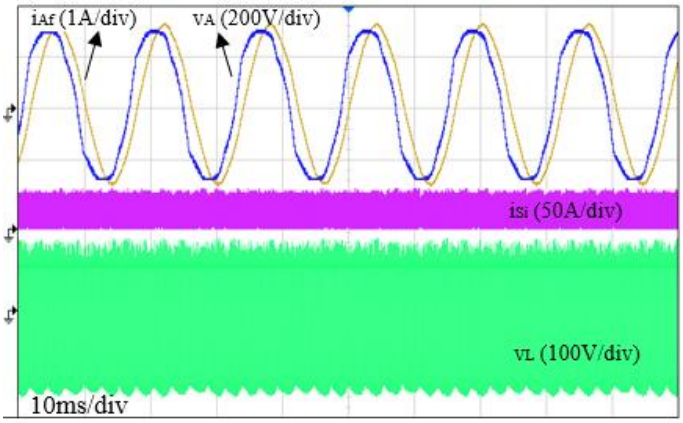


Figure 55 - Phase voltage, phase current, unfiltered input current, and link voltage at V_{in}=100 V, V_{LL} = 400 V^{rms} at 640 W for L=170 µH and C_{tot} = 110 nF.

buck modes are identical and as a results there are no transition glitches. The measured values for f_{Link} and i_{peak+} in this figure are 10.65 kHz and 18.22 A which are very close to the calculated values of 10.8 kHz and 18.75 A, respectively.

In order to further validate the operation of the inverter, Figure 55 shows the inverter waveforms while it supplies power to a series RL load with a fundamental power factor of 0.86. The load inductor is slightly saturated and creates a voltage distortion. Figure 55 indicates that the proposed converter is capable of injecting sine current to the load even if the load exhibits a benign non-linear behavior. This is because the controller in the proposed inverter shapes the current on a cycle-by-cycle basis as described earlier.

3.3 Conclusion

This chapter proposed two isolated DC-AC power converters. The first topology is an isolated inverter that utilizes a parallel ac link between its input and output semiconductors to achieve soft-switching throughout the operating range. The multiple winding transformer allows for series connection of output cells to achieve a high terminal voltages. Input and output currents are controlled by a digital controller on a cycle-by-cycle basis. An in-depth analysis of the converter's operation is peresnted, including mathematical modeling, design guidelines, loss calculation, and current shaping. Experimental results on single-transformer and multiple-transformer prototypes are carried out to cover several modes of operation, including leading and lagging power factor loads, buck and boost modes of operation, and converter response to input voltage and current variations.

The second proposed topology is a single-ended inverter with a single input-side switch and cascaded output-side switch cells. The cascaded output cells allow for the utilization of switches with smaller current and voltage ratings to achieve higher powers. Isolation is

provided through a high-frequency multiple-winding transformer. Details of the operation were studied and the experimental results were included.

4 AC-AC TOPOLOGIES

4.1 Introduction

One of the key contributions of modern power electronics to the industry is the elimination of the need for bulky energy storage elements and large transformers. Energy storage elements such as capacitors and inductors are often used to filter out unwanted components in voltages or currents; and bulky transformers are used to change voltage levels and/or provide galvanic isolation. Modern power electronics relaxes the filtering requirements either by proposing power conversion methods that avoid or decrease unwanted harmonic bi-products, or by pushing the problematic harmonic content to a higher range in the frequency spectrum. Similarly, modern power electronics helps reduce or eliminate bulky line-frequency transformers by increasing the power conversion frequency, which in turn reduces the transformer core volume by one or two orders of magnitude.

Since more than a century ago, line-frequency transformers have been actively incorporated in the power transfer and distribution system to change the voltage level. Such transformers are very reliable, but provide no other function [81]. Solid-state transformers, however, can offer the same function along with several more, including VAR compensation, power flow management, dynamic voltage level control and sag/swell compensation, frequency alteration even to/from DC, increased power quality, fault isolation, active filtering, etc. [82]-[85].

Areas of applicability of solid-state transformers is quite wide. Solid-state transformers are expected to be a key component in future traction systems due to their high efficiency

and low weight and volume [86]-[88]. Solid-state transformer are also anticipated to be an important component in smart grids due to their controllability [77][89]-[91].

A widely used criterion to categorize solid-state transformer topologies is the number of stages [83]:

- AC-DC followed by DC-HFAC, followed by HFAC-DC, followed by DC-AC conversions;
- AC-HFAC followed by HFAC-DC, followed by DC-DC, followed by DC-AC conversions;
- AC-HFAC, followed by HFAC-AC conversions.

The third option in the above list does not require bulky DC capacitors. As a result it results in a higher power density at the cost of simplicity of control and protection. In this chapter, two single-stage AC-AC conversion topologies are proposed. Neither of the proposed topologies require dc capacitors. In both topologies, voltage stress is split equally among the semiconductors. This allows in converter input or output terminals to interface medium voltage sources/loads without utilization of high-voltage semiconductor.

4.2 The Proposed AC-AC Topologies

Figure 56 is a circuit diagram of the proposed Cascaded H-Bridge three-phase buck boost AC-AC converter. The three-phase AC-AC converter includes an input side V_a, V_b, V_c, and an output side V_A, V_B, V_C. Each input phase and each output phase include a modular H-Bridge switch cell. On either the output or the input side, there could be 1 or

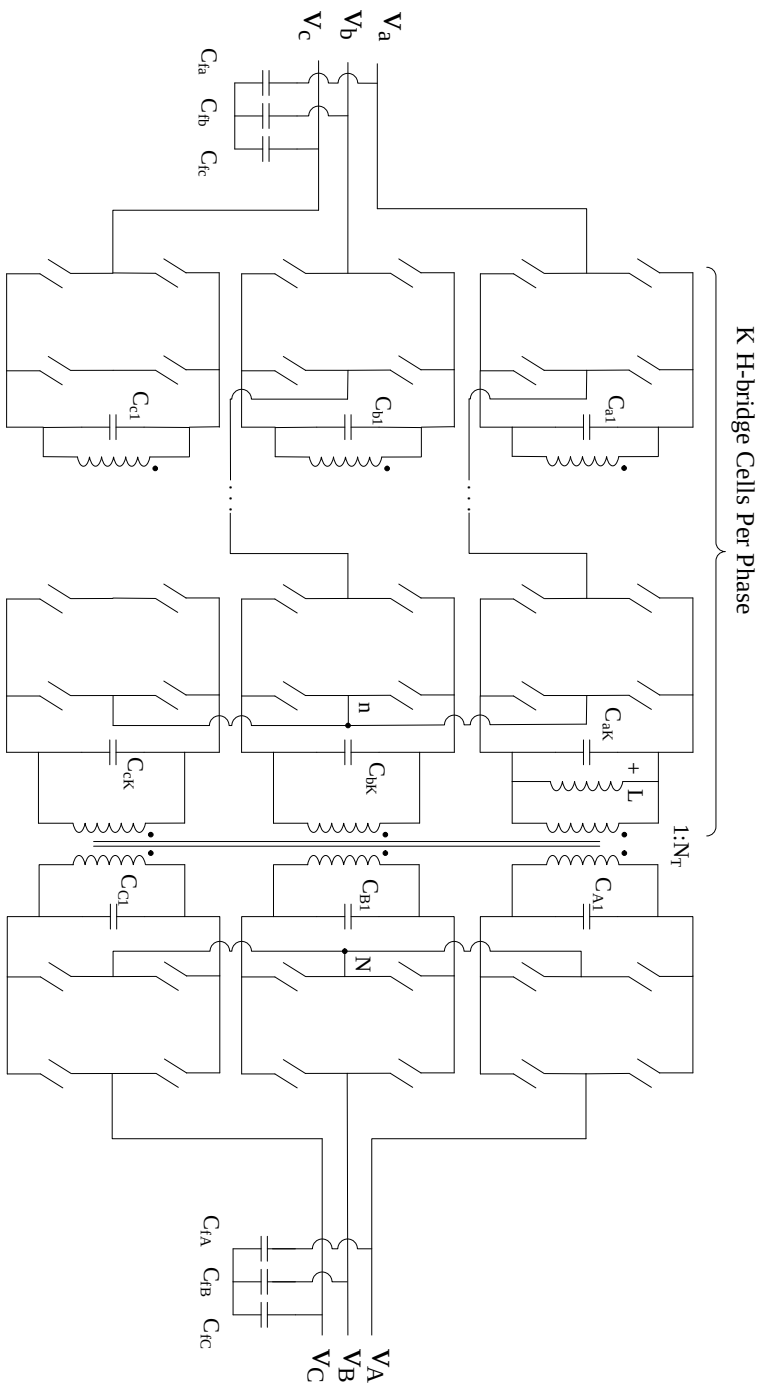


Figure 56 - Cascaded H-Bridge AC-AC Converter

more H-Bridges connected in series. In Figure 56, each input phase includes *K* cells. Each

cell is composed of four switches and is connected across a winding of a multiple winding transformer. In a typical embodiment, the multiple-winding transformer provides galvanic isolation between the input and the output. Each cell includes a link capacitor, C_{xk}. In a typical application, the resonant capacitors are rated at approximately a few tens or hundreds of nano-Farads, which is considerably smaller than capacitors utilized in conventional power-conversion applications, which could range from a few hundred micro-Farads to several thousand micro-Farads. The decreased size of the capacitor reduces the need for external heating or cooling systems for the three-phase buck boost AC-AC converter. Compared to conventional power-conversion applications [9], the proposed three-phase buck boost AC-AC converter exhibits a reduction factor of 1/2 in the voltage stress on output switching devices, and a reduction factor of 1/2K on input switches. The link capacitors C_{xk} together with the magnetizing inductance of the multiple winding transformer, L, form a parallel resonant tank that partially resonates during operation of the three-phase buck boost AC-AC converter. In a typical embodiment, the inductor may be the magnetizing inductance of the multiple-winding transformer or an external or parasitic inductor. The multiple-winding transformer is illustrated by way of example in Figure 56 as including six windings; however, in various other embodiments, any other arrangement of multiple-winding transformers may be utilized provided that a winding of each transformer is coupled to a winding of another transformer. Additionally, the input and output terminals of the three-phase buck boost AC-AC converter may be connected to a filter network such as a three-phase capacitive or capacitive/inductive filter.

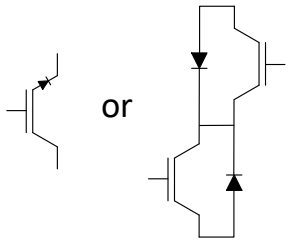


Figure 57 – Switch realization in the proposed AC-AC converter.

The three phase AC-AC converter bidirectional. In Figure 56, the left side of the three-phase AC-AC converter has been illustrated to be the input side; however, the right side could as the input side and the left side.

The switching device in the three-phase AC-AC converter can either be four-quadrant devices or two quadrant devices as shown in Figure 57, depending on which the converter can be double-ended or single ended. In the single-ended embodiment, the two-quadrant switching device is a bidirectional blocking semiconductor switching device such as, for example, a reverse-blocking IGBT, and IGBT in series with a diode, or a MOSFET in series with a diode. In double-ended embodiment, the switching device could be any bidirectional blocking and conducting semiconductor switching device. For example, the bidirectional blocking and conducting semiconductor switching device in Figure 57 includes two single semiconductor switching devices and two diodes. Generally, the double-ended converter is utilized in applications involving higher power such as, for example, applications involving at least a few kilo-Watts to several hundred kilo-Watts. In an application, if the voltage ratio between the input and output line-to-line voltages are

significantly different than 1, the converter of Figure 58 may be more appropriate. In this converter, one side is composed of several cascaded H-Bridge cells, while the other side is based on the conventional three-leg structure of [9].

Figure 59 is a circuit diagram of a three-phase buck boost AC-AC converter with voltage balancing windings. The three-phase AC-AC converter includes a multiple-winding transformer disposed between the input and output sides. The transformer has *3×(K-1)+1* windings on the input side and four windings on the output side.

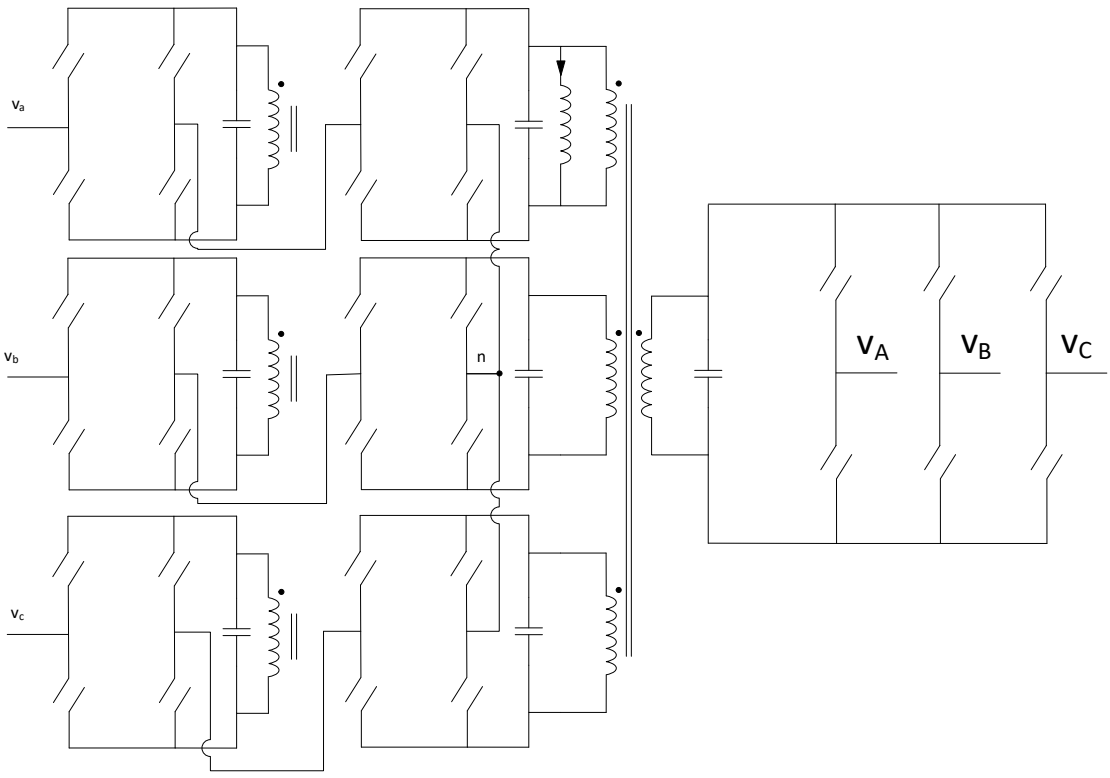


Figure 58 – Three-phase AC-AC converter with cascaded H-Bridge cells on one side only.

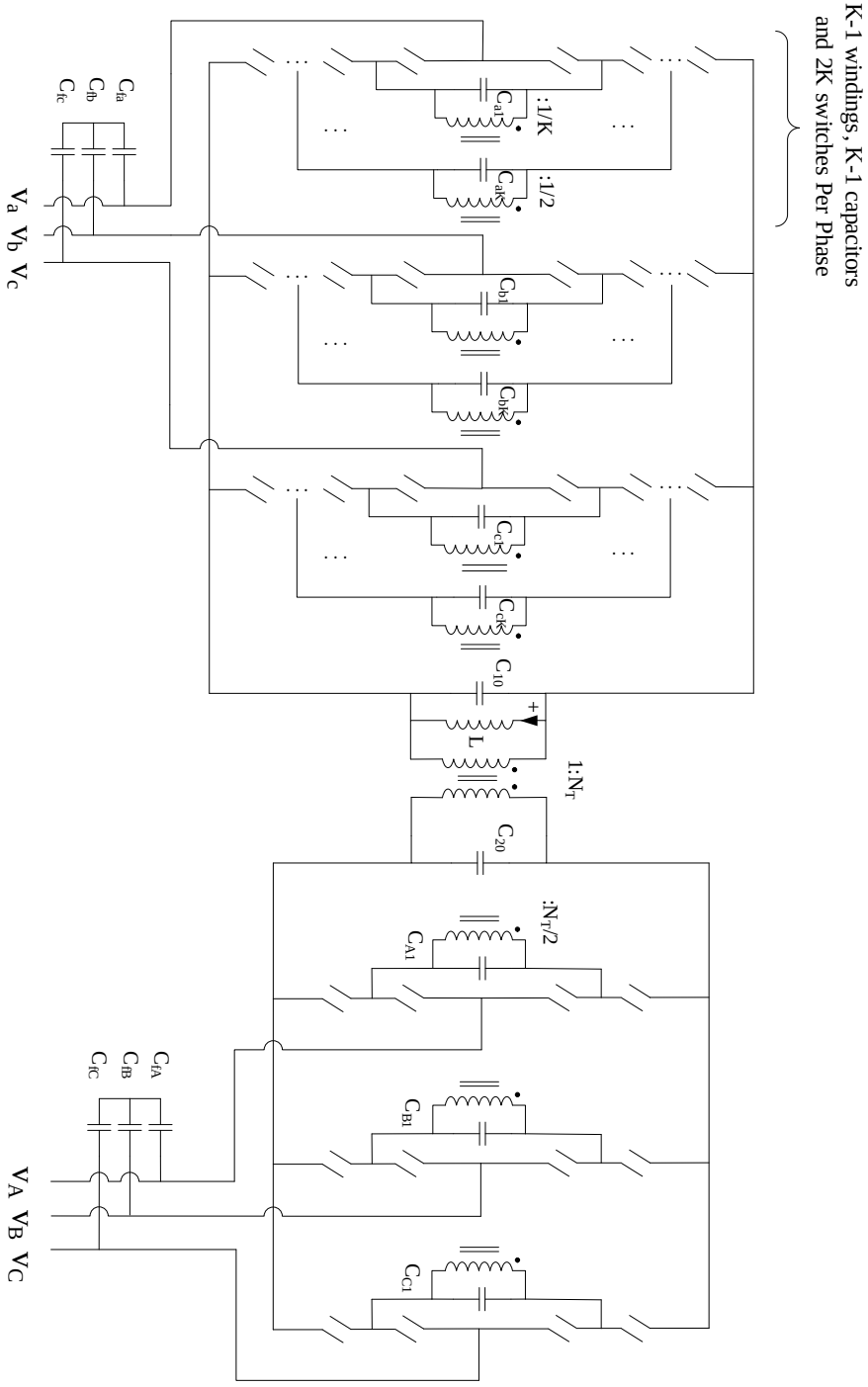


Figure 59 – AC-AC converter with voltage balancing windings

Each input and output phase is assigned to a leg. Each input leg includes *K-1* auxiliary

transformer windings, *K-1* link capacitors C_{xk}, and *2K* switching devices. Each winding is connected in parallel to a resonant capacitor. The switching devices are either four-quadrant or two-quadrant devices, as shown in in Figure 57, which will result in a double-ended or single-ended converter, respectively. The windings mounted on the converter legs do not take part in power transfer. The role of the leg windings is to distribute voltage stress on the semiconductor devices equally. Power flows through the main two windings shown at the center of Figure 59. The turn ratio between the two main windings is $1{:}N_T$. On each of the input legs, the number of turns in the voltage balancing windings reduces by a factor of 1/2. For example, when the outermost winding on the input phases, i.e., the main input winding, has 1 turn, the innermost windings of the input legs have $1/2^{k-1}$ turns. Similarly, if the main output winding has N_T turns, the innermost windings of the output phases have $N_T/2$ turns. The converter of Figure 59 exhibits a reduction factor of 1/K and 1/2 in the voltage stress on the input side and output side semiconductors, respectively, when compared to the conventional power-conversion systems of [9]. Generally, the link capacitors are rated at approximately a few hundred nano-farads, which are considerably smaller than capacitors utilized in conventional power-conversion applications. This converter is bidirectional.

The multiple-winding transformer is illustrated by way of example in Figure 59 as including several windings; however, in various other embodiments, any other arrangement of multiple-winding transformers may be utilized provided that a winding of each transformer is coupled to a winding of another transformer. Additionally, the input and output terminals of the three-phase buck boost AC-AC converter may be connected

to a filter network such as a three-phase capacitive or capacitive/inductive filter. In an application, if the voltage ratio between the input and output line-to-line voltages are significantly different than 1, the converter of Figure 60 may be more appropriate. In this converter, one side includes several voltage-balancing windings, while the other side is based on the conventional three-leg structure of [9].

Operation of the Proposed AC-AC Converters

In reference to AC-AC converters of Figure 56 and Figure 59, as stated before, each converter has a parallel resonant that partially resonates during the converter's operation. The link inductor in these converters transfers energy by charging from the selected input phase pair and discharging into the selected output phase pairs. The link inductor current

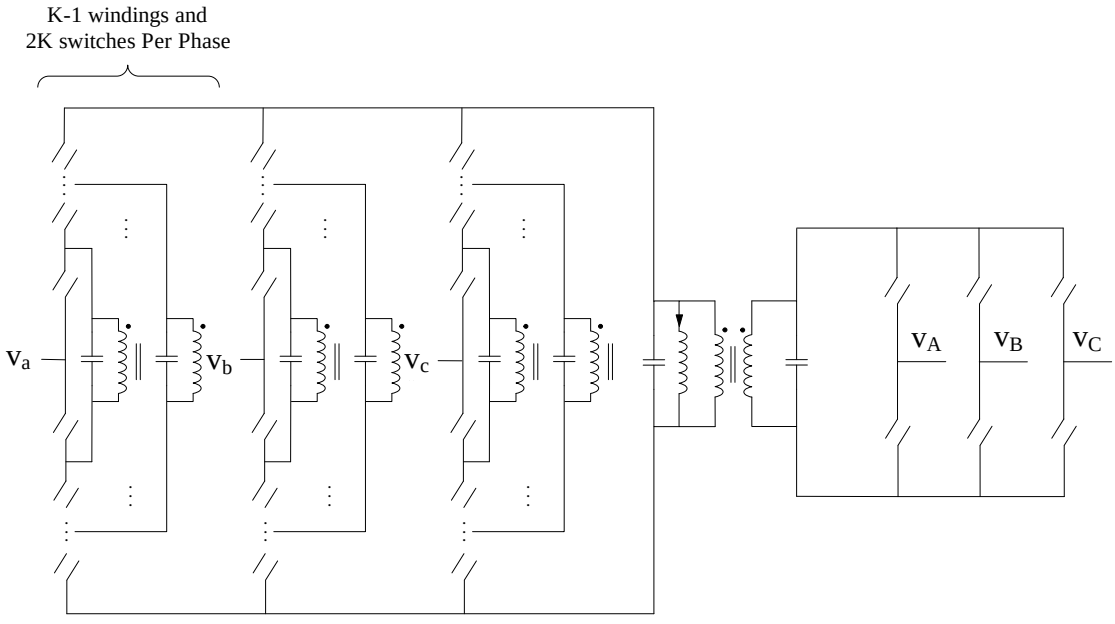


Figure 60 – Three-phase AC-AC converter with voltage-balancing windings on one side only.

and voltage are hereinafter referred to the link current and link voltage, respectively. Depending on the choice of first or second embodiment for the converters (two-quadrant or four-quadrant switch realizations), each link cycle is comprised of eight or sixteen operating modes as elaborated in the rest of this section. By no way of limitation and for the sake of brevity and simplicity of naming conventions, it is assumed that components are ideal. There are periods when all semiconductor switches are in blocking mode and the link is not connected to either of the terminals, and therefore is allowed to resonate until the link voltage meets certain requirements. The resonant periods provide ZVS for every switch turn-on, and near-ZVS for every switch turn-off transition.

Due to similarities between the proposed cascaded H-Bridge converter and the voltage-balancing converter, the description of modes and operating waveforms are combined in this section. In the single ended embodiment of converters of Figure 56 and Figure 59 with two-quadrant switches, each link cycle is comprised of eight modes. Two modes charge the link from the input, and two modes discharge the link into the output. Partial resonance happens at the remaining four modes (even-numbered modes). Without loss of generality, unity power factor is assumed at the input terminals in this section.

Operation of single-ended embodiment

The operating waveforms are shown in Figure 61.

Mode 1: The link charges with positive current through the two input phases whose current reference difference (and therefore voltage difference) has the biggest magnitude. Figure 62 show an example of mode 1. The thick lines in Figure 62 show the path and switches that current goes through. In these figures, input phases *a* and *b* current references have the largest difference and are selected to carry current. Phases *a* and *b* in these figures have positive and negative current references, respectively, therefore the switches in thick lines are selected to carry current. In case current references of phases *a* and *b* were negative and positive respectively, then opposite switches of phase *a* and *b* would conduct to have positive current in the link. Assuming that the link frequency in much higher than input frequency, the voltage on the link inductor in this mode is almost constant and the

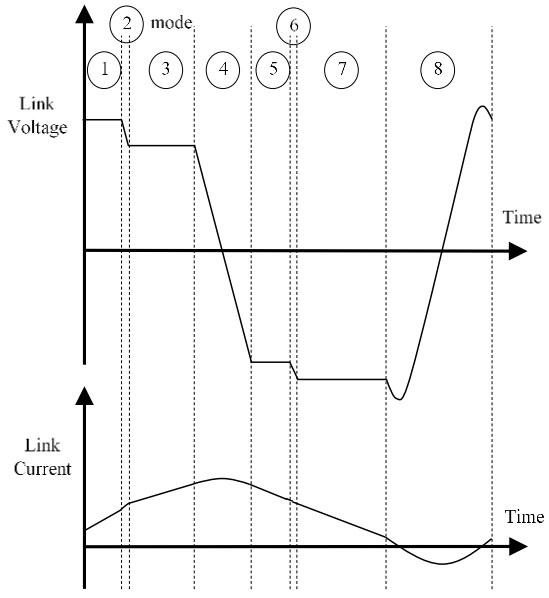


Figure 61 - Operating waveforms of single-ended embodiments

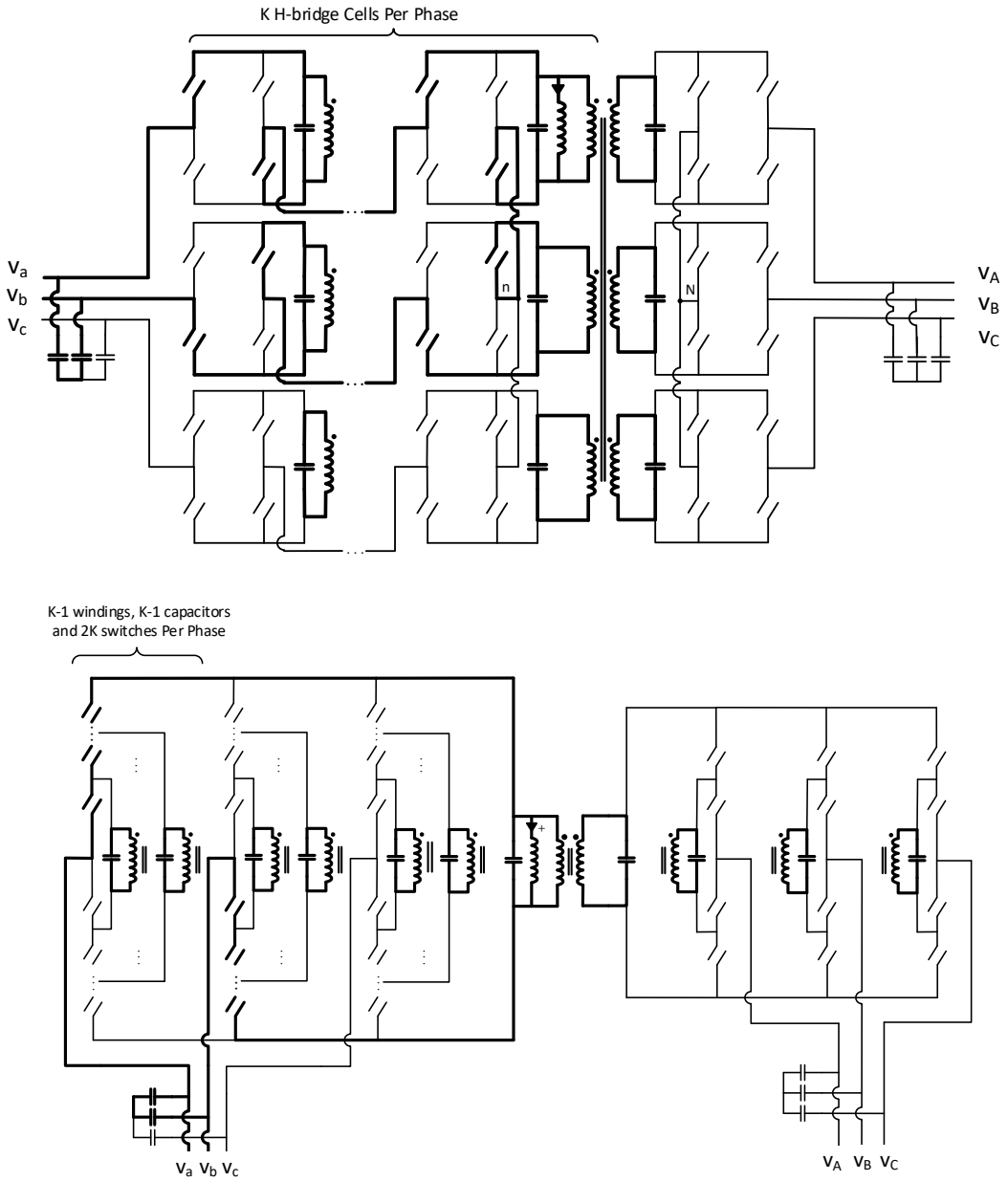


Figure 62 - Current path in charging mode 1.

link current increases almost linearly, as shown in Figure 61. This mode goes on until one

of the phases in the input pair meets its current reference.

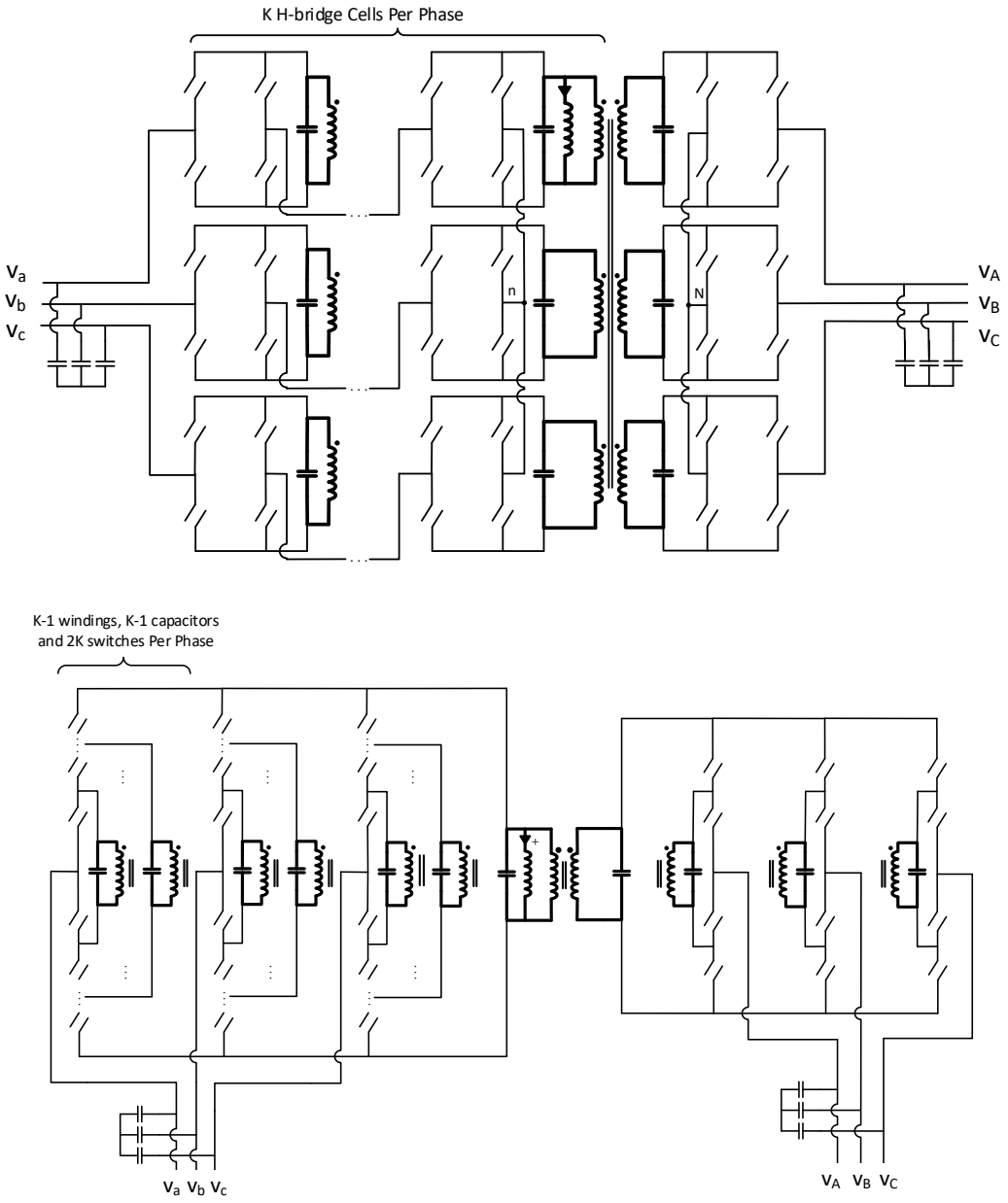


Figure 63 - Current path in resonant modes 2, 4, 6 and 8.

Mode 2: None of the switches conduct. The link resonates as and its voltage drops in magnitude, as shown in Figure 61. The path of current is shown in thick lines in Figure 63. At the instant when the link voltage matches the input phase pair whose current reference difference has the second highest magnitude of all, the switches on that pair start conducting. Similar to mode 1, switches in the conducting phase pair should be selected in a way that the polarity of current in the conducting phases matches their references and positive current flows through the link inductor. For example, Figure 64 show conducting switches for the case where phases *a* and *c* have positive and negative current references, respectively. Voltage on the conducting switches at the instant they turn on is approximately zero. This results in zero-voltage at turn-on and significantly reduces switching losses.

Mode 3: The selected input phase pair from mode 2 charges the link with positive current, as shown in Figure 61. This mode goes on until the conducting phases meet their current reference. This should happen at the same time on both phases since phase currents sum to zero at every instant. Soft switching at turn-off is achieved because the winding capacitors and the input filter capacitors limit the rate of rise of voltage on the switches. The same phenomenon happens at the end of mode 1 as well. At the end of mode 3 all switches are gated off.

Mode 4: No switches carry current in this mode, therefore the link resonates and link voltage changes polarity, as shown in Figure 61. The path of current is shown in Figure 63. On the output side, out of the three output phase pairs *AB*, *BC*, and *AC*, the two pairs which accommodate the phase with the largest current reference magnitude are candidates

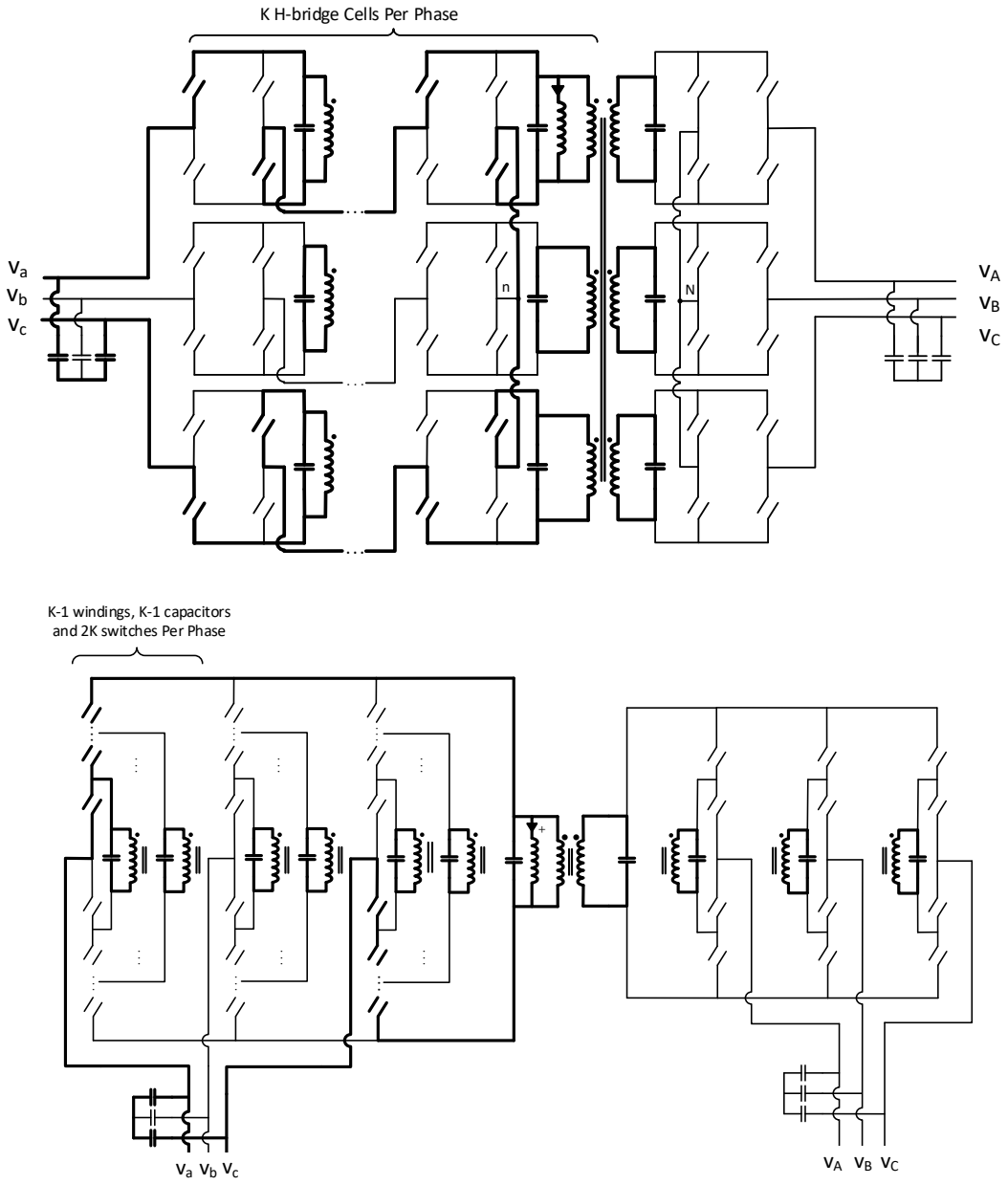


Figure 64 - Current path in mode 3.

for conduction in mode 5. Out of these two pairs, the one with the smaller voltage

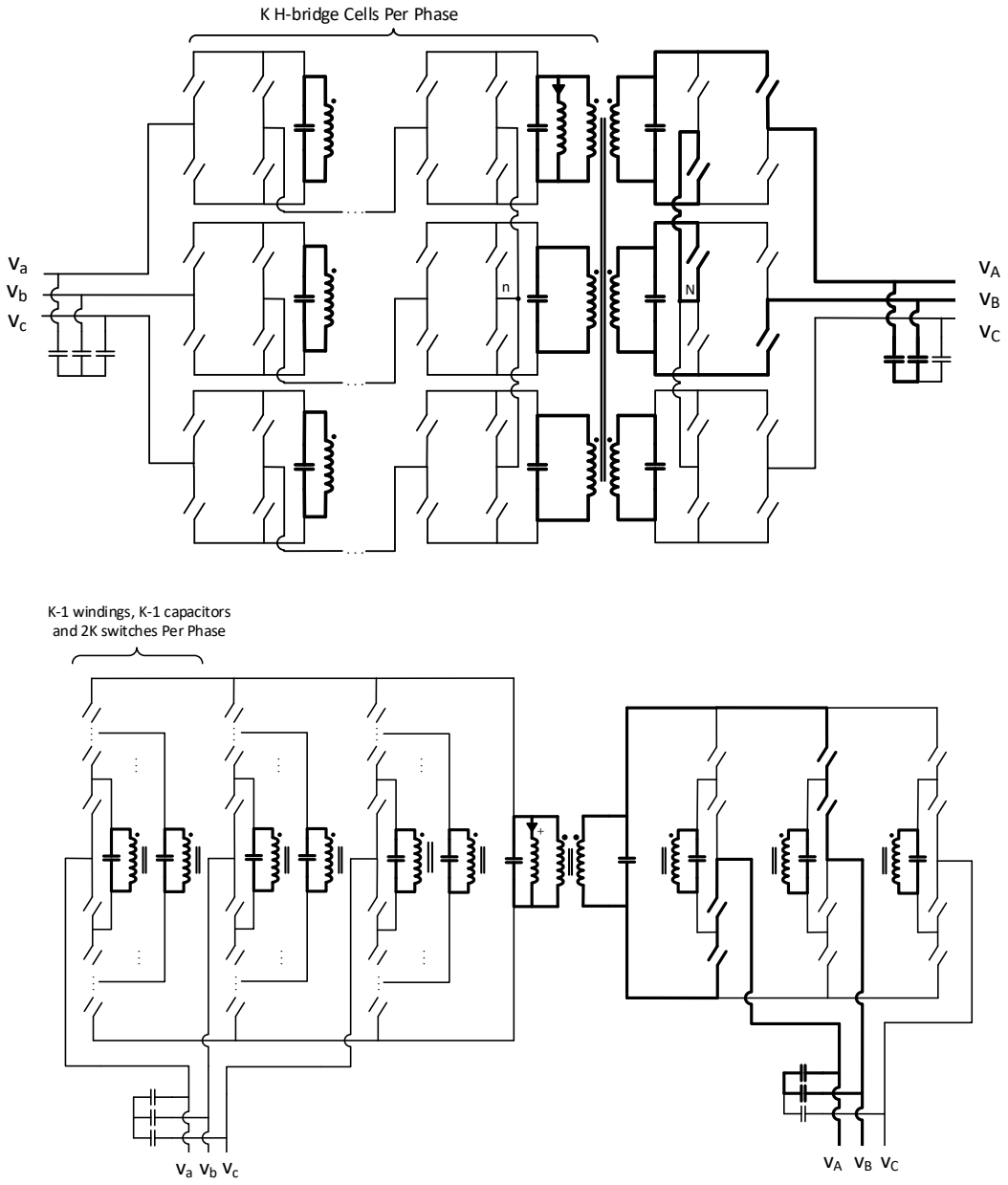


Figure 65 - Current path in mode 5.

difference magnitude is selected for mode 5, and the other is selected for conduction in

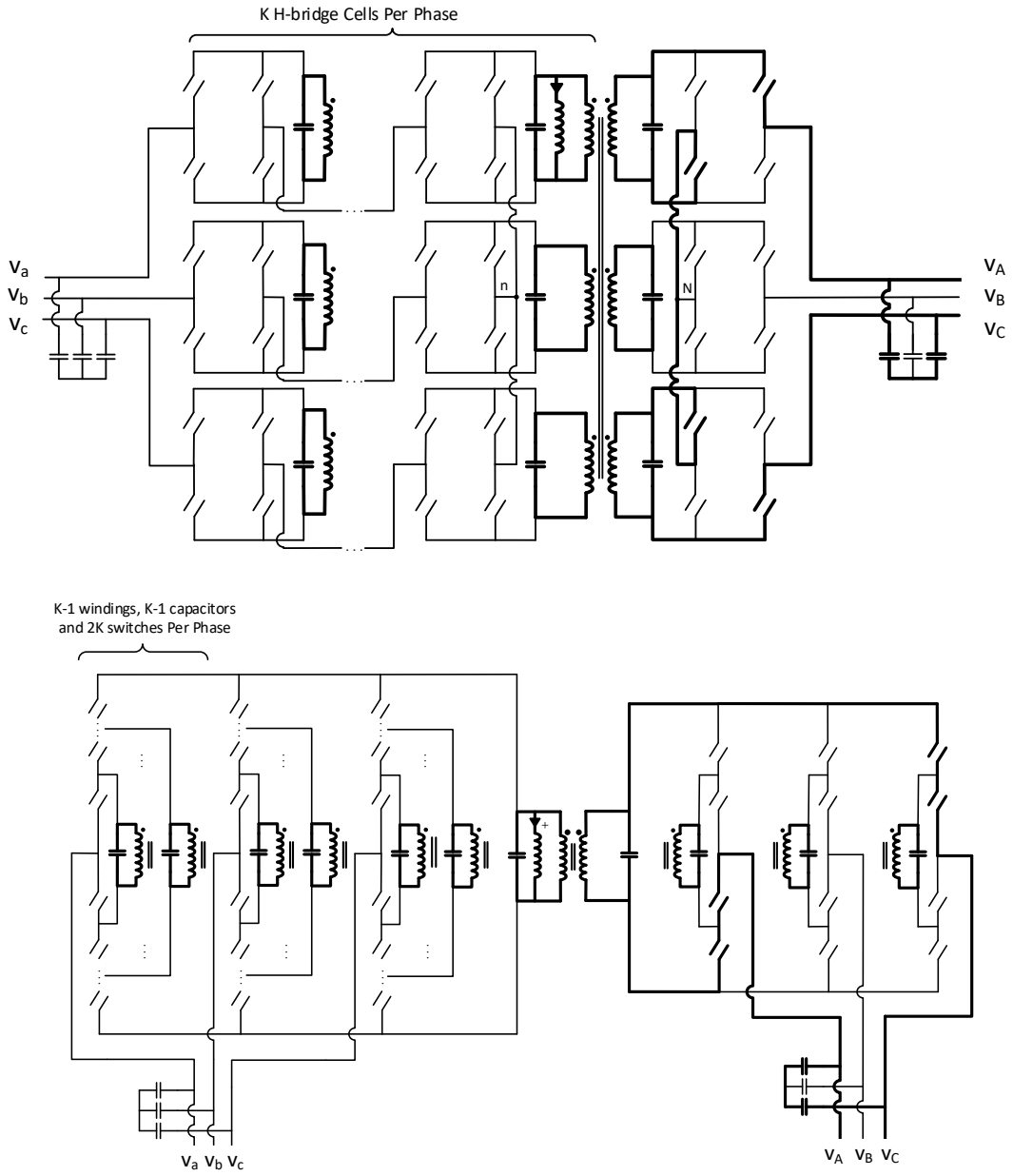


Figure 66 - Current path in mode 7.

mode 7. This leads to a descending voltage sequence as shown in Figure 61, which is an essence in having zero-voltage turn-on. Switches corresponding to the chosen pair start

conducting only when the reflected link voltage through the transformer turns ratio matches the pair voltage difference. As in mode 2, this ensures zero-voltage turn-on for all conducting switches.

Mode 5: The link is discharged on the output pair and its current reduces almost linearly as shown in Figure 61. Switches in the conducting phase pair should be selected in a way that the polarity of current in the conducting phases matches their references and the positive link current ramps down. For example, Figure 65 show the path and the conducting switches for the case where phase pair *AB* conducts. Current references for phases *A* and *B* in Figure 65 are positive and negative, respectively. This mode continues until one of the phases in the pair, namely the phase with the smaller current reference, meets its current reference. At this moment the switches are gated off and mode 5 ends.

Mode 6: No switches carry current and the link resonates as shown in Figure 61. The negative link voltage increases in magnitude, until it equals the reflected voltage difference of the selected output pair for mode 7. At this point, the switches corresponding to the pair start conducting to carry the positive link current. Selection of a proper phase pair for mode 7 was explained above in the discussion of mode 5. Similar to other resonant modes, zero-voltage switching at turn-on is achieved.

Mode 7: The selected output pair discharges the link, as shown in Figure 61. Similar to mode 5, switches in the conducting phase pair should be selected in a way that the polarity of current in the conducting phases matches their references and the positive link current ramps down. For example, Figure 66 show the path and the conducting switches for the case where phase pair *AC* conducts. Current references for phases *A* and *B* in Figure 66 is

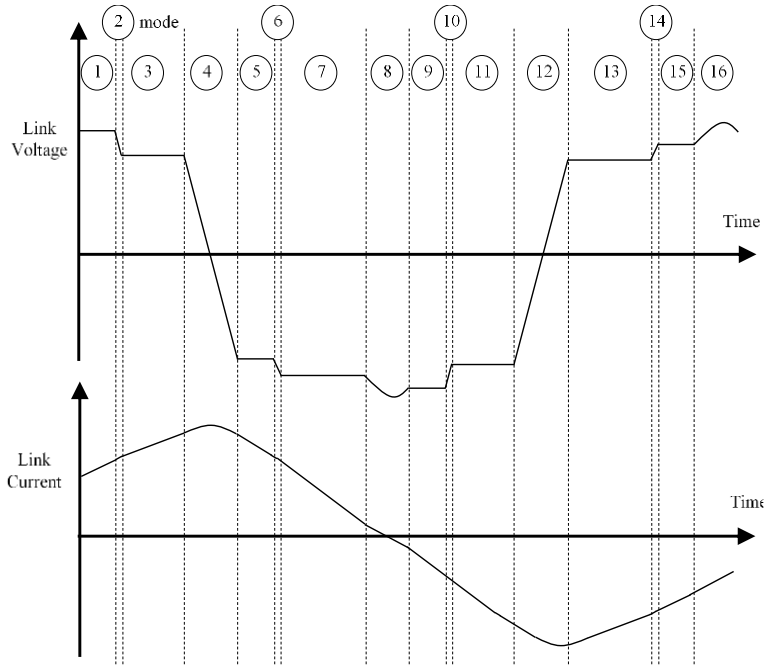


Figure 67 - Operating waveforms of double-ended embodiments

positive and negative, respectively. This mode continues until the energy in the link drops to a pre-determined level $E_{desired}$. This will be elaborated in a later section. This mode ends by turning all switches off.

Mode 8: No switches carry current in this mode. With the left-over energy from mode 7 the link resonates and the link voltage goes positive, as shown in Figure 61. At this point, the link current changes direction. This mode ends when the link voltage equals the input phase pair with the largest current reference difference. The proper switches on the input are gated on at zero voltage to prepare the converter for mode 1.

Operation of the double-ended embodiments

The operating waveforms for the double ended embodiments are shown in Figure 67. Comparing with the single-ended waveforms of Figure 61, one can verify that the operations of both embodiments are identical in the first 7 modes. Therefore, only mode 8 will be described here.

Mode 8: No switches carry current in this mode. With the left-over energy from mode 7 the link resonates and the negative link voltage grows in magnitude to have its peak, as shown in Figure 67. At this point the link current changes direction. This mode ends when the link voltage equals the input phase pair with the largest current reference difference. The proper switches on the input are gated on at zero voltage to prepare the converter for mode 9.

As shown in Figure 67, modes 9-16 follow essentially the same concept set forth in the discussion of modes 1-8. However, the link current and voltage have reversed polarities as compared to modes 1-8. In modes 9-16, the link current experiences its negative half cycle. This allows bipolar utilization of the magnetic device and makes the converter capable of transferring power through both polarities of the link current, as is the case for all double-ended converters.

It was mentioned earlier in description of modes that the requirement to end mode 7 (and 15) is to have the energy left in the link reduced to a desired level, $E_{desired}$. This condition guarantees that the same amount of energy that was delivered to the link in modes 1 and 3 (and 9 and 11), is taken from the link in modes 5 and 7 (and 13 and 15), thereby indirectly balancing the input and output powers. Since $E_{desired}$ is the link energy content, it also determines the link peak voltage in mode 8 (and 16).

TABLE VI. COMPONENT SPECIFICATIONS AND NOMINAL VALUES FOR CONVERTER OF FIGURE 58

Output Power	1.4 kW
Line Input Voltage	85 V^{rms}
Line Output Voltage	380 V^{rms}
Input Frequency	60 Hz
Output Frequency	50 Hz
Link Inductance (L)	110 μH
Total Link Capacitance (C_{tot})	168 nF
Link Resonant Frequency ($\omega_{res}/2\pi$)	37.0 kHz
Input Filter (L_i, C_i)	820 μH, 40 μF
Output Filter (L_x, C_x)	10 μH, 10 μF
Transformer Turn Ratio (N)	1

4.3 Simulation Results

The converter of Figure 58 is simulated in this section as a step-up three-phase AC-AC converter with single-ended operation. The input phases *A, B,* and *C* are supplied through an 85 V three-phase line. On the output side, each phase includes two cascaded H-Bridge cells ($K=2$). The output phases feed a three-phase resistive load of 180 Ω per phase. The output current reference is generated using the same method that was described in section 3.1.2. The inverter nominal values and component specifications are shown in Table VI.

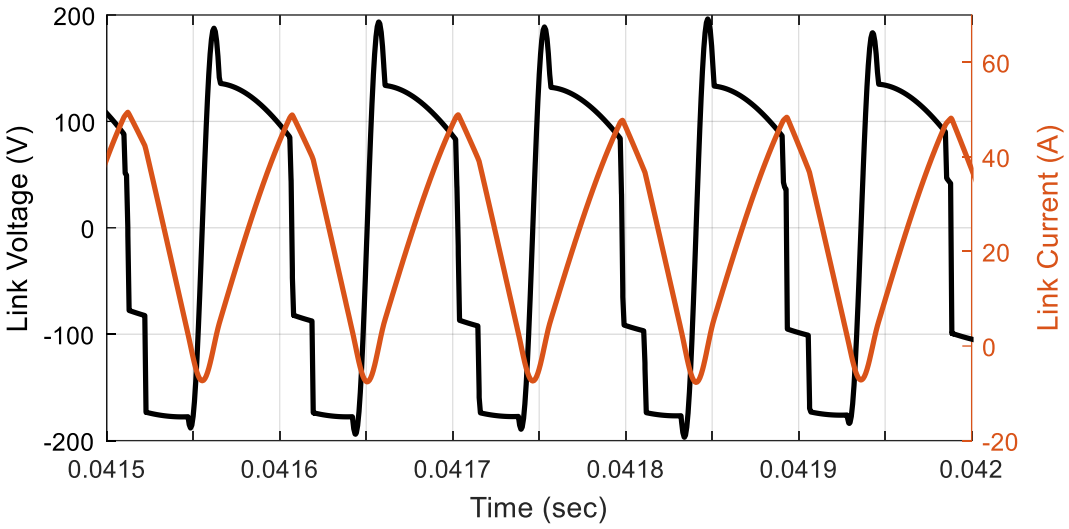


Figure 68 - Link voltage and current in the AC-AC converter of Figure 58

Figure 68 depicts the link voltage and current waveforms as seen on the input-side winding. The converter in this figure operates at a link frequency of 10.5 kHz at an output power of 1.38 kW. The input current and output voltages of this converter are shown in Figure 69. Prior to the instant of 0.036 seconds the converter outputs 690 W to the resistive load at an output line voltage of 350 V^{rms}. At 0.036 seconds the input reference is doubled by the upper-hand controller. In response, the converter's output current reference increases to maintain power flow balance between the input and output terminals. Between 0.036 seconds and 0.074 seconds the converter operates at 1.38 kW. At 0.074 seconds the input current reference is changed back to its original value. Figure 69 shows that the proposed converter is capable of regulating the input and output currents successfully. The link current is also visible in this figure.

The voltage stress on an output switch while the converter operates at an output voltage of 492 V^{rms} is illustrated in Figure 70 for a full period of output voltage. Even though the

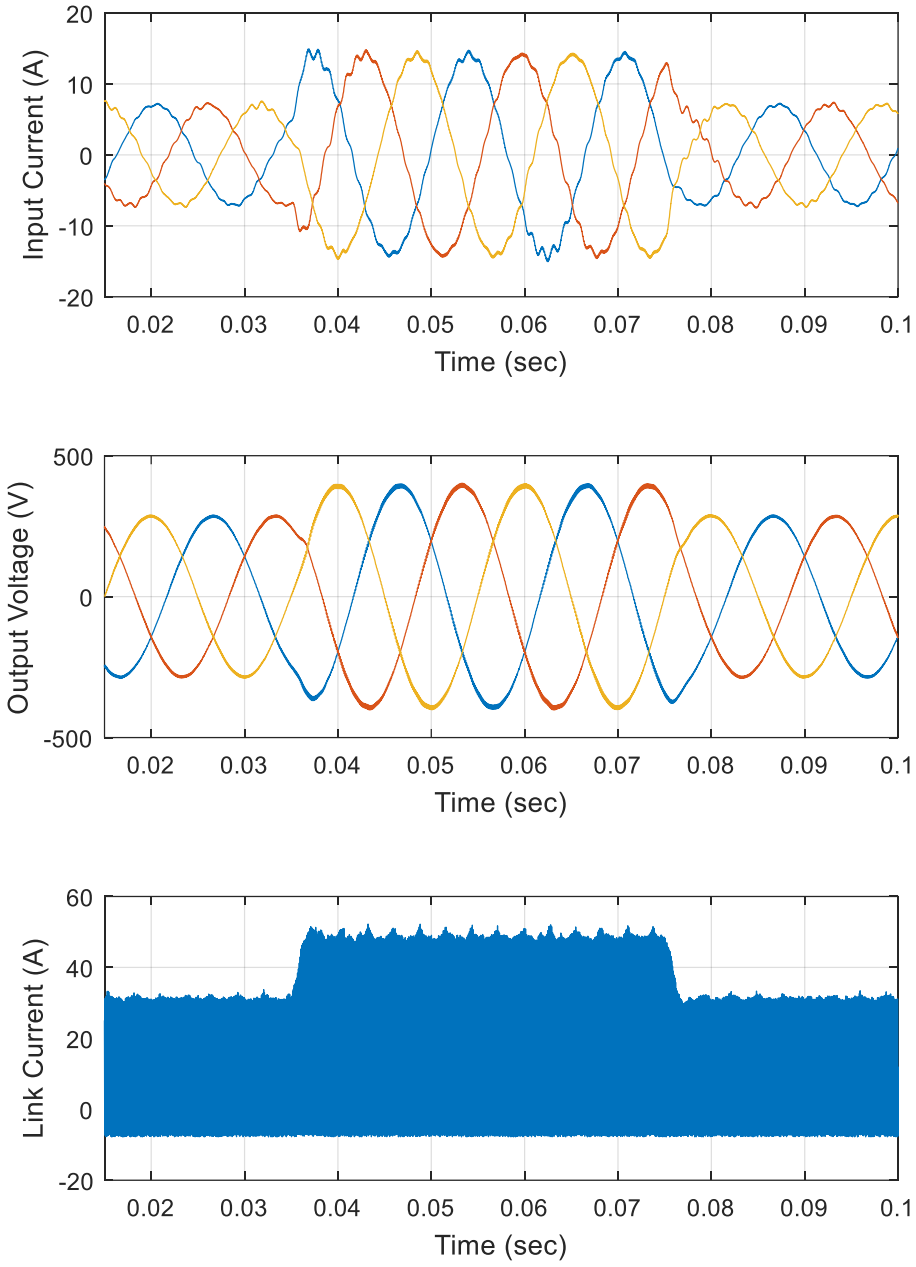


Figure 69 - Operating waveforms of the AC-AC converter of Figure 58
Top: Input currents; Middle: Output voltage; Bottom: Link current

instantaneous outout line votlage at this point of operation is as big as 700 V, the switch

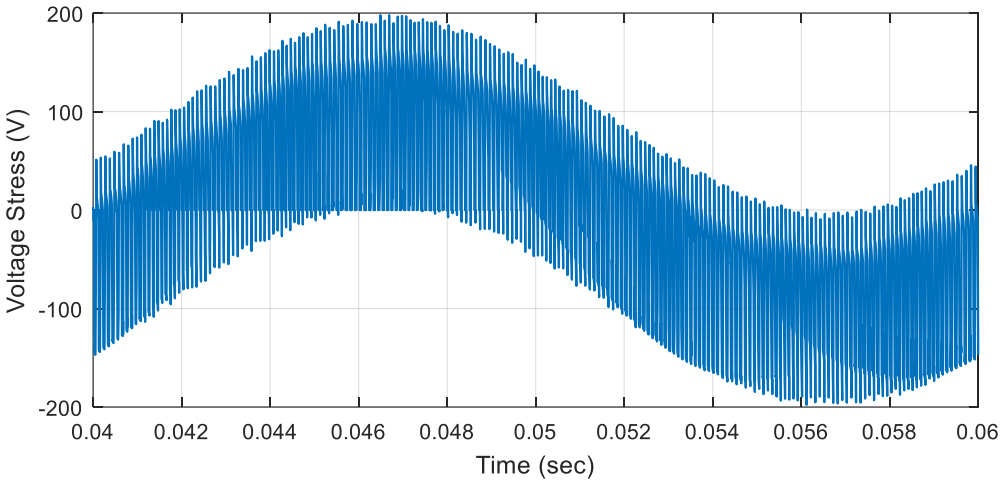


Figure 70 - Output switch voltage stress in the converter of the AC-AC converter of Figure 58

TABLE VII. COMPONENT SPECIFICATIONS AND NOMINAL VALUES FOR CONVERTER OF FIGURE 60

Output Power	5.4 kW
Line Input Voltage	1200 V^{rms}
Line Output Voltage	208 V^{rms}
Input Frequency	60 Hz
Output Frequency	50 Hz
Link Inductance (L)	350 µH
Total Link Capacitance (C_{tot})	65 nF
Link Resonant Frequency ($\omega_{res}/2\pi$)	33.0 kHz
Input Filter (L_i, C_i)	7 mH, 4 µF
Output Filter (L_x, C_x)	30 µH, 30 µF
Transformer Turn Ratio (N_T)	0.5

voltage stress does not exceed 200 V. The is because the voltage stress is split equally amount four H-Bridge cells (2×K).

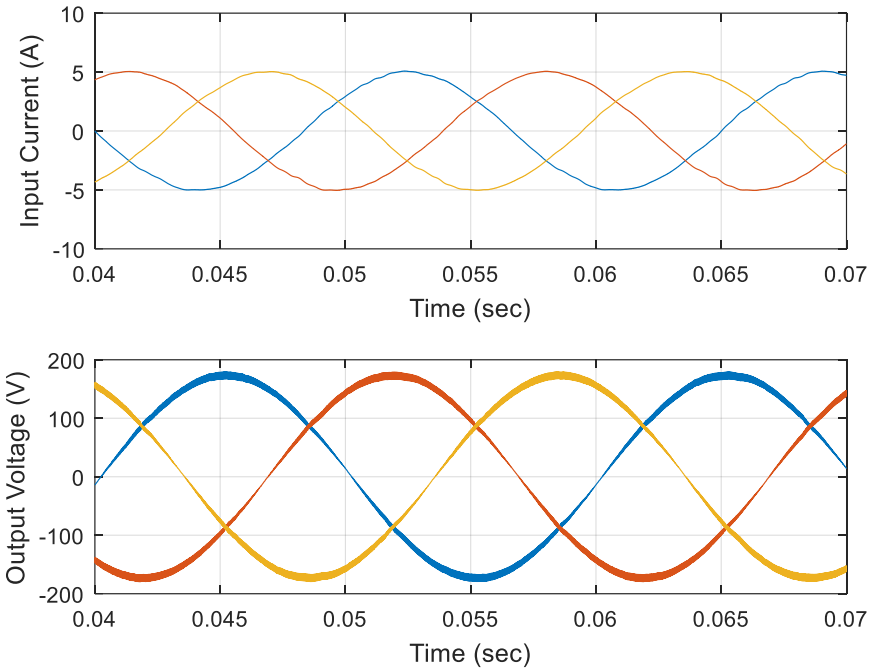


Figure 71 - Input current and output voltage of the converter of Figure 60

The three-phase AC-AC converter of Figure 60 is simulated as step-down converter to convert a 60 Hz, 1.2 kV^{rms} votlage to a 50 Hz, 208 V^{rms} voltage. In addition to the shared main winding on the input side, each of the input phases A, B, and C includes two votlage balancing windings ($K = 3$). This reduces the voltage stress on the input switches by a factor of 1/3. The input switches in this converter are chosen to be four-quadrant devices to demonstrate the operation of the converter in double-ended mode. The turn ration between the main input and output windings is 1:0.5, i.e., $N_T = 1$. The specifications of the simulated inverter are shown in Table VII.

The input current and output votlages of the AC-AC converter while it supplies a resistive load of 8 Ω per phase are depicted in Figure 71. This figure verifies that the three-phase converter is capable of shaping the input and output currrents successfully. The link

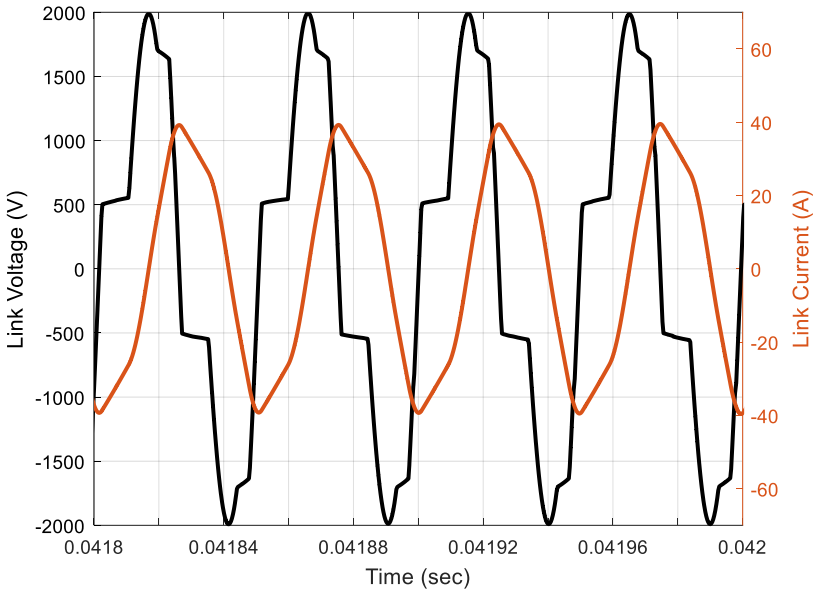


Figure 72 - Link voltage and current waveforms of the converter of Figure 60

voltage and current waveforms are shown in Figure 72. The link current and voltage are symmetrical in their positive and negative half cycles and no dc offset is present on the link current. The converter at this point of operation is in buck mode because the link charging votlage of about 1650 V is greater than the link discharging voltage of about 500 V. The link frequency and link peak currents are 20 kHz and 39 A, respectively.

It was stated previously that in the AC-AC converter with voltage balancing windings, only the main two windings are in charge of power transfer and the voltage balancing windings carry current in resonant modes only. The current waveforms for the main winding and the innermost voltage-balancing winding for phase A on the input side are shown in Figure 73. As showin the figure, the voltage balancing winding carries only a negligible amount of current in charging mdoes 1 and 3.

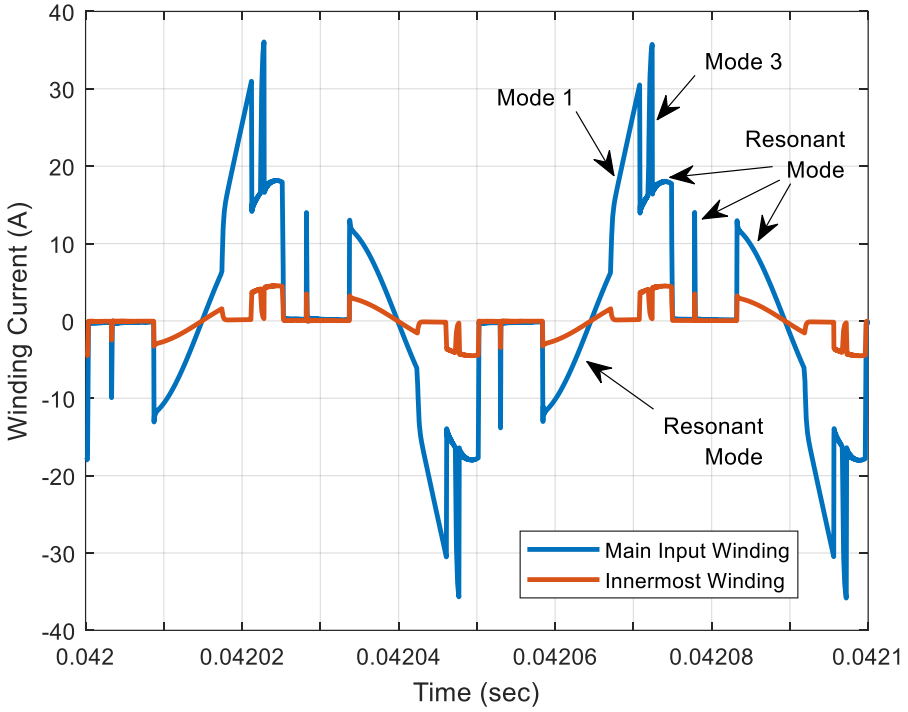


Figure 73 - Current through the main and the voltage balancing windings of the converter of Figure 60

4.4 Conclusion

This chapter of the disertation proposed two thre-phase AC-AC power converters with reduced votlage stress on the switches. As expected of most AC-AC converters, the proposed topologies are bidirectional in terms of power flow. The first topology uses several H-Bridge cells on each phase to achieve a high voltage rating at the terminal without rasing a need for high-voltage semiconductors. The second toplogy takes advantage of several voltage balancing windings in each phase to split the voltage stress equally among the switches. Both topologies could be implemented as either a single-

eneded converter or a double-ended one, depending on the cost and application. Simulation results for both topologies are presented.

5 CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

This dissertation proposes two DC-DC converters in chapter 2, namely a Push-Push toplogy and a high step-up Flyback toplogy. The former requries active switches on the input and output side while the latter has only one switch in the input side. Two DC-AC inverters that include series-connected cascaded H-Bridge cells on their AC side are prposed in chapter 3. Both converter maintain soft-switching throughout their range of operation and are able to achieve a high voltage boost ratio due to their buck-boost nature and serially connected output cells. In chapter 4 two single-stage AC-AC power converter with isolation and soft-switching are presented. One topology uses cascaded H-Bridge cells while the other uses voltage-balancing windings to split the voltage stress among the switches.

While all of the proposed topologies provide certain advantages, the analysis carried out in this dissertation brings to attention the following items.

- The majority of power loss in the proposed converters is attributed to the switch conduction dissipation. Future implementations of the converters may take advantage of wide band-gap devices to increase the conversion efficiency [92][93][94]. Such devices are commercially available in two classes, namely Silicon-Carbide and Gallium-Nitride. Since all of the proposed switches offer a limited rate of voltage change during switching transients, and because voltage stress is reduces among the switches, use of low-voltage wide band-gap devices is anticipated to result in significant advantages in terms of efficiency. Such devices offer a small on-state voltage drop. Specifically, the input-side switches

in the proposed inverters of chapter 3 could take great advantage of Gallium-Nitride devices.

- The proposed topologies in chapters 3 and 4 of this dissertation benefit from the reduced voltage stress, reduced rate of voltage change, and scalability of their structure, all of their input (or output) switches toggle at the same time. A future line of research may be dedicated to discover a scheme to interleave the switching transitions. This could increase the frequency on the unwanted terminal ripples by an integer factor, which in turn reduces the size of the required terminal components.

REFERENCES

[1] S. Arulselvi, C. Subashini, and G. Uma, "A New Push-Pull Zero Voltage Switching Quasi-Resonant Converter: Topology, Analysis and Experimentation," INDICON, 2005 Annual IEEE, pp.482-486, 11-13 Dec. 2005.

[2] H. Mahmoudi, M. Aleenejad, and R. Ahmadi, "Topology exploration and control of a filter-less Z-source inverter," *2016 IEEE Power and Energy Conference at Illinois (PECI)*, Urbana, IL, 2016, pp. 1-5.

[3] A. Marzoughi, RP. Burgos, D. Boroyevich, K. Uchida, T. Hiyoshi, M. Sakai, K. Wada, M. Furumai, T. Tsuno, and Y. Mikamura, "Static and Dynamic Performance Characterization of 3.3-kV 30-A Discrete SiC MOSFETs," 12th annual conference of Center for Power Electronics Systems (CPES), Blacksburg, VA, 2016.

[4] M. Moosavi, G. Farivar, H. Iman-Eini, and S. M. Shekarabi, "A voltage balancing strategy with extended operating region for cascaded H-bridge converters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 5044-5053, Sept. 2014.

[5] Y. H. Kim, S. C. Shin, J. H. Lee, Y. C. Jung, and C. Y. Won, "Soft-Switching Current-Fed Push–Pull Converter for 250-W AC Module Applications," in *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 863-872, Feb. 2014.

[6] Y. Yuan, and Q. Wu, "One zero-voltage-switching three-transistor push-pull converter," in *IET Power Electronics*, vol. 6, no. 7, pp. 1270-1278, August 2013.

[7] P. Xuewei and A. K. Rathore, "Current-Fed Soft-Switching Push–Pull Front-End Converter-Based Bidirectional Inverter for Residential Photovoltaic Power System," in *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 6041-6051, Nov. 2014.

[8] T. Mishima and M. Nakaoka, "A Novel High-Frequency Transformer-Linked Soft-Switching Half-Bridge DC–DC Converter With Constant-Frequency Asymmetrical PWM Scheme," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 2961-2969, Aug. 2009.

[9] W. Alexander, “Universal Power Converter.” U.S. Patent EP2025051 B1, issued December 31, 2014.

[10] H. Keyhani and H. A. Toliyat, "Partial-Resonant Buck–Boost and Flyback DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4357-4365, Aug. 2014.

[11] T. Wang, S. Sen, and M. Amirabadi, "Soft switching high frequency AC-link DC-DC buck-boost converters," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte, NC, 2015, pp. 57-64.

[12] S. V. Araujo, R. P. Torrico-Bascope and G. V. Torrico-Bascope, "Highly Efficient High Step-Up Converter for Fuel-Cell Power Processing Based on Three-State Commutation Cell," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 6, pp. 1987-1997, June 2010.

[13] X. Zhang and T. C. Green, "The Modular Multilevel Converter for High Step-Up Ratio DC–DC Conversion," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4925-4936, Aug. 2015.

[14] H. Wu, Y. Lu, L. Chen, P. Xu, X. Xiao and Y. Xing, "High step-up/step-down non-isolated BDC with built-in DC-transformer for energy storage systems," in *IET Power Electronics*, vol. 9, no. 13, pp. 2571-2579, 10 26 2016.

[15] H. Jafarian *et al*., "Design and implementation of distributed control architecture of an AC-stacked PV inverter," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 1130-1135.

[16] W. Li, W. Li, M. Ma, Y. Deng and X. He, "A non-isolated high step-up converter with built-in transformer derived from its isolated counterpart," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, Glendale, AZ, 2010, pp. 3173-3178.

[17] A. Rahnamaee, A. Mojab, H. Riazmontazer, S. K. Mazumder and M. Zefran, "Soft-switched discontinuous pulse-width pulse-density modulation scheme," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2016, pp. 1989-1994.

[18] Y. Li; X. Lyu; D. Cao, "A Zero-Current-Switching High Conversion Ratio Modular Multilevel DC-DC Converter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics* , In press.

[19] Y. Lu, H. Wu, K. Sun and Y. Xing, "A Family of Isolated Buck-Boost Converters Based on Semiactive Rectifiers for High-Output Voltage Applications," in *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6327-6340, Sept. 2016.

[20] M. Delshad and H. Farzanehfard, "High step-up zero-voltage switching current-fed isolated pulse width modulation DC-DC converter," in *IET Power Electronics*, vol. 4, no. 3, pp. 316-322, March 2011.

[21] T. J. Liang, J. H. Lee, S. M. Chen, J. F. Chen and L. S. Yang, "Novel Isolated High-Step-Up DC–DC Converter With Voltage Lift," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1483-1491, April 2013.

[22] H. Wu, T. Xia, X. Zhan and Y. Xing, "High step-up isolated resonant converter with voltage quadrupler rectifier and dual-phase-shift control," in *IET Power Electronics*, vol. 8, no. 12, pp. 2462-2470, 12 2015.

[23] H. S. H. Chung, S. Y. R. Hui and Wei-Hua Wang, "A zero-current-switching PWM flyback converter with a simple auxiliary switch," in *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 329-342, Mar 1999.

[24] I. D. Kim and G. H. Cho, "New bilateral zero voltage switching AC/AC converter using high frequency partial-resonant link," *Industrial Electronics Society, 1990. IECON '90., 16th Annual Conference of IEEE*, Pacific Grove, CA, 1990, pp. 857-862 vol.2.

[25] M. Biglarbegian, N. Kim and B. Parkhideh, "Boundary Conduction Mode Control of a Boost Converter With Active Switch Current-Mirroring Sensing," in *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 32-36, Jan. 2018.

[26] M. Moosavi and H. A. Toliyat, “Soft-Switching Push-Pull Converter with Parallel Resonant Link and Buck-Boost Capability”, in *Proc. IEEE Energy Conversion Congress and Exposition*, 2016, In press.

[27] M. Moosavi, A. Morya and H. A. Toliyat, "A low-cost soft-switching high step-up flyback converter with stacked output cells," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 1700-1705.

[28] A. Moeini, H. Iman-Eini and A. Marzoughi, "DC link voltage balancing approach for cascaded H-bridge active rectifier based on selective harmonic elimination-pulse width modulation," in *IET Power Electronics*, vol. 8, no. 4, pp. 583-590, 4 2015.

[29] L. H. Dixon, Jr, Design of Flyback Transformers and Filter Inductors. Lexington, Massachusetts: Unitrode Corporation, ____, Topic 2.

[30] A. Pressman, Switching Power Supply Design, 3rd ed, McGraw-Hill, Inc.; April 2009, Chap. 4.

[31] S. Bacha, D. Picault, B. Burger, I. Etxeberria-Otadui, and J. Martins, "Photovoltaics in Microgrids: An Overview of Grid Integration and Energy Management Aspects," in *IEEE Industrial Electronics Magazine*, vol. 9, no. 1, pp. 33-46, March 2015.

[32] A. Abramovitz, B. Zhao, and K. M. Smedley, "High-Gain Single-Stage Boosting Inverter for Photovoltaic Applications," in *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3550-3558, May 2016.

[33] Y. Zhou, W. Huang, F. Hong and C. Wang, "Modelling analysis and power loss of coupled-inductor single-stage boost inverter based grid-connected photovoltaic power system," in *IET Power Electronics*, vol. 9, no. 8, pp. 1664-1674, July 2016.

[34] F. A. S. Neves, M. Carrasco, F. Mancilla-David, G. M. S. Azevedo, and V. S. Santos, "Unbalanced Grid Fault Ride-Through Control for Single-Stage Photovoltaic Inverters," in *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3338-3347, April 2016.

[35] G. Hua and F. C. Lee, "Soft-switching techniques in PWM converters," in *IEEE Trans. on Ind. Electron.*, vol. 42, no. 6, pp. 595-603, December 1995.

[36] I. R. Balasubramanian, S. I. Ganesan, and N. Chilakapati, "Impact of partial shading on the output power of PV systems under partial shading conditions," in *IET Power Electronics*, vol. 7, no. 3, pp. 657-666, March 2014.

[37] M. D. Bellar, T. S. Wu, A. Tchamdjou, J. Mahdavi, and M. Ehsani, "A review of soft-switched DC-AC converters," in *IEEE Trans. on Ind. Appl.*, vol. 34, no. 4, pp. 847-860, July-Aug. 1998.

[38] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, Second Edition. Springer, 2001, Chap. 19.

[39] M. A. Rezaei, K. J. Lee, and A. Q. Huang, "A High-Efficiency Flyback Micro-inverter With a New Adaptive Snubber for Photovoltaic Applications," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 318-327, January 2016.

[40] Y. H. Kim, J. W. Jang, S. C. Shin, and C. Y. Won, "Weighted-Efficiency Enhancement Control for a Photovoltaic AC Module Interleaved Flyback Inverter Using a Synchronous Rectifier," in *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6481-6493, December 2014.

[41] J. Zhang, X. Huang, X. Wu, and Z. Qian, "A High Efficiency Flyback Converter With New Active Clamp Technique," in *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1775-1785, July 2010.

[42] B. M. Song, J. Kim, J. S. Lai, K. C. Seong, H. J. Kim, and S. S. Park, "A multilevel soft-switching inverter with inductor coupling," in *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 628-636, March/April 2001.

[43] R. Teichmann and J. Oyama, "ARCP soft-switching technique in matrix converters," in *IEEE Trans. on Ind. Electron.*, vol. 49, no. 2, pp. 353-361, April 2002.

[44] H. Keyhani and H. A. Toliyat, "Single-Stage Multistring PV Inverter With an Isolated High-Frequency Link and Soft-Switching Operation," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3919-3929, August 2014.

[45] M. Amirabadi, A. Balakrishnan, H. A. Toliyat, and W. C. Alexander, "High-Frequency AC-Link PV Inverter," in *IEEE Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 281-291, January 2014.

[46] M. Cacciato, A. Consoli, R. Attanasio and F. Gennaro, "Soft-Switching Converter With HF Transformer for Grid-Connected Photovoltaic Systems," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 5, pp. 1678-1686, May 2010.

[47] L. Chen, A. Amirahmadi, Q. Zhang, N. Kutkut and I. Batarseh, "Design and Implementation of Three-Phase Two-Stage Grid-Connected Module Integrated Converter," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3881-3892, Aug. 2014.

[48] M. N. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge DC-to-DC converter," in *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294-1301, November/December 1992.

[49] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A Survey on Cascaded Multilevel Inverters," in *IEEE Trans. on Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, July 2010.

[50] X. Zhang, T. C. Green, and A. Junyent-Ferré, "A New Resonant Modular Multilevel Step-Down DC–DC Converter with Inherent-Balancing," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 78-88, January 2015.

[51] C. Turpin, L. Deprez, F. Forest, F. Richardeau, and T. A. Meynard, "A ZVS imbricated cell multilevel inverter with auxiliary resonant commutated poles," in *IEEE Transactions on Power Electronics*, vol. 17, no. 6, pp. 874-882, November 2002.

[52] R. W. De Doncker and J. P. Lyons, "The auxiliary resonant commutated pole converter," in *Proc. IEEE Industry Applications Society Annual Meeting*, 1990, vol. 2, pp. 1228-1235.

[53] M. Moosavi and H. A. Toliyat, "A Scalable Soft-Switching Photovoltaic Inverter with Cascaded H-Bridge Cells and Galvanic Isolation*," in IEEE Trans. on Power Electronics*, Submitted Mar 2017, Under Review.

[54] M. Moosavi and H. A. Toliyat, "A Multi-Cell Cascaded High Frequency Link Inverter with Soft-Switching and Isolation*," in IEEE Trans. on Industrial Electronics*, Submitted Sep 2016, Under Review.

[55] H. Jafarian, S. Bhowmik and B. Parkhideh, "Hybrid Current/Voltage-mode Control Scheme for Distributed AC-stacked PV Inverter with Low Bandwidth Communication Requirements," in *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1-1.

[56] A. Kouchaki, H. Iman-Eini, B Asaei, "A new maximum power point tracking strategy for PV arrays under uniform and non-uniform insolation conditions," *in Solar Energy*, vol 91, 2013, pp 221-232,

[57] Y. Shi, R. Li, Y. Xue and H. Li, "High-Frequency-Link-Based Grid-Tied PV System With Small DC-Link Capacitor and Low-Frequency Ripple-Free Maximum Power Point Tracking," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 328-339, Jan. 2016.

[58] H. A. Toliyat and M. Moosavi “Method and Apparatus for Medium Voltage Electronic Power Conversion” Provisional U.S. Patent Application No. 62371027, August, 2016.

[59] P. L. Dowell, "Effects of eddy currents in transformer windings," in *Electrical Engineers, Proceedings of the Institution of*, vol. 113, no. 8, pp. 1387-1394, August 1966.

[60] A. Reatti and M. K. Kazimierczuk, "Comparison of various methods for calculating the AC resistance of inductors," in *IEEE Transactions on Magnetics*, vol. 38, no. 3, pp. 1512-1518, May 2002.

[61] M. Bartoli, N. Noferi, A. Reatti and M. K. Kazimierczuk, "Modeling Litz-wire winding losses in high-frequency power inductors," *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, Baveno, 1996, pp. 1690-1696 vol.2.

[62] J. Reinert, A. Brockmeyer and R. W. A. A. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation," in *IEEE Transactions on Industry Applications*, vol. 37, no. 4, pp. 1055-1061, Jul/Aug 2001.

[63] A. Kouchaki, R. Lazar, J. L. Pedersen and M. Nymand, "5 kW bidirectional grid-connected drive using silicon-carbide switches: Control," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 640-645.

[64] Park, J. B.; Moosavi, M.; Toliyat, H. A.; “Electromagnetic-Thermal Coupled Analysis Method for Interior PMSM,” *in International Electric Machines & Drives Conference (IEMDC)*, May 2015.

[65] S. Pakdelian, M. Moosavi, H. A. Hussain and H. A. Toliyat, "Control of an Electric Machine Integrated With the Trans-Rotary Magnetic Gear in a Motor Drive Train," *in IEEE Transactions on Industry Applications*, Jan./Feb. 2017.

[66] Moosavi, M.; Farhangi, S.; Iman-Eini, H.; Haddadi, A.; "An LCL-based interface connecting photovoltaic back-up inverter to load and grid," *in Power Electronics, Drive Systems and Technologies Conference (PEDSTC)*, Feb 2013.

[67] J. Rodriguez, S. Bernet, P. K. Steimer and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7, pp. 2219-2230, Jul. 2010.

[68] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[69] P. Lezana and R. Aceiton, "Hybrid Multicell Converter: Topology and Modulation," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 3938-3945, Sep. 2011.

[70] X. Zhang, T. C. Green and A. Junyent-Ferré, "A New Resonant Modular Multilevel Step-Down DC–DC Converter with Inherent-Balancing," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 78-88, Jan. 2015.

[71] Z. Guo, D. Sha and X. Liao, "Hybrid Three-Level and Half-Bridge DC–DC Converter With Reduced Circulating Loss and Output Filter Inductance," in *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6628-6638, Dec. 2015.

[72] Z. Guo, D. Sha and X. Liao, "Hybrid Phase-Shift-Controlled Three-Level and LLC DC–DC Converter With Active Connection at the Secondary Side," in *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 2985-2996, Jun. 2015.

[73] Jie Chang and Jun Hu, "Modular design of soft-switching circuits for two-level and three-level inverters," in *IEEE Transactions on Power Electronics*, vol. 21, no. 1, pp. 131-139, Jan. 2006.

[74] J. Li, J. Liu, D. Boroyevich, P. Mattavelli and Y. Xue, "Three-level Active Neutral-Point-Clamped Zero-Current-Transition Converter for Sustainable Energy Systems," in *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3680-3693, Dec. 2011.

[75] J. Li, J. Liu, D. Dong, P. Mattavelli, D. Boroyevich and Y. Xue, "A transformer assisted zero-voltage soft-switching three-level active neutral-point-clamped converter," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2421-2427.

[76] D. Y. Kim, J. K. Kim and G. W. Moon, "A Three-Level Converter With Reduced Filter Size Using Two Transformers and Flying Capacitors," in *IEEE Transactions on Power Electronics*, vol. 28, no. 1, pp. 46-53, Jan. 2013.

[77] C. Turpin, L. Deprez, F. Forest, F. Richardeau and T. Meynard, "A new ZVS imbricated cell multilevel inverter with auxiliary resonant commutated poles," in *Proc. Power Electronics Specialists Conference (PESC)*, 2001, vol. 2, pp. 1159-1164.

[78] H. Keyhani and H. A. Toliyat, "Isolated ZVS High-Frequency-Link AC-AC Converter With a Reduced Switch Count," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4156-4166, Aug. 2014.

[79] M. Amirabadi, H. A. Toliyat and W. C. Alexander, "A Multiport AC Link PV Inverter With Reduced Size and Weight for Stand-Alone Application," in *IEEE Transactions on Industry Applications*, vol. 49, no. 5, pp. 2217-2228, Sep./Oct. 2013.

[80] H. Keyhani, M. Johnson and H. A. Toliyat, "A soft-switched highly reliable grid-tied inverter for PV applications," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 1725-1732.

[81] A. Q. Huang, "Medium-Voltage Solid-State Transformer: Technology for a Smarter and Resilient Grid," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 29-42, Sept. 2016.

[82] E. R. Ronan, S. D. Sudhoff, S. F. Glover and D. L. Galloway, "A power electronic-based distribution transformer," in *IEEE Transactions on Power Delivery*, vol. 17, no. 2, pp. 537-543, Apr 2002.

[83] F. Briz, M. Lopez, A. Rodriguez and M. Arias, "Modular Power Electronic Transformers: Modular Multilevel Converter Versus Cascaded H-Bridge Solutions," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 4, pp. 6-19, Dec. 2016.

[84] Jih-Sheng Lai, A. Maitra, A. Mansoor and F. Goodman, "Multilevel intelligent universal transformer for medium voltage applications," *Fourtieth IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, 2005.*, 2005, pp. 1893-1899 Vol. 3.

[85] J. E. Huber and J. W. Kolar, "Applicability of Solid-State Transformers in Today's and Future Distribution Grids," in *IEEE Transactions on Smart Grid*, vol. PP, no. 99, pp. 1-1.

[86] J. Kolar and G. Ortiz, “Solid-state-transformers: Key components of future traction and smart grid systems,” presented at the Int. Power Electronics Conf. (IPEC), Hiroshima, Japan, 2014.

[87] M. Steiner and H. Reinold, "Medium frequency topology in railway applications," *2007 European Conference on Power Electronics and Applications*, Aalborg, 2007, pp. 1-10.

[88] J. E. Huber and J. W. Kolar, "Solid-State Transformers: On the Origins and Evolution of Key Concepts," in *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 19-28, Sept. 2016.

[89] L. Ferreira Costa, G. De Carne, G. Buticchi and M. Liserre, "The Smart Transformer: A solid-state transformer tailored to provide ancillary services to the distribution grid," in *IEEE Power Electronics Magazine*, vol. 4, no. 2, pp. 56-67, June 2017.

[90] X. She, X. Yu, F. Wang and A. Q. Huang, "Design and Demonstration of a 3.6-kV–120-V/10-kVA Solid-State Transformer for Smart Grid Application," in *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3982-3996, Aug. 2014.

[91] J. E. Huber and J. W. Kolar, "Applicability of Solid-State Transformers in Today’s and Future Distribution Grids," in *IEEE Transactions on Smart Grid*, vol. PP, no. 99, pp. 1-1.

[92] A. Morya, M. Moosavi, M. C. Gardner and H. A. Toliyat, "Applications of Wide Bandgap (WBG) devices in AC electric drives: A technology status review," *2017 IEEE International Electric Machines and Drives Conference (IEMDC)*, Miami, FL, 2017, pp. 1-8.

[93] A. Marzoughi, J. Wang, R. Burgos and D. Boroyevich, "Characterization and Evaluation of the State-of-the-Art 3.3-kV 400-A SiC MOSFETs," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8247-8257, Oct. 2017.

[94] M. Biglarbegian and B. Parkhideh, " Characterization of SenseGaN Current-Mirroring for Power GaN with the Virtual Grounding in a Boost Converter," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 5915-5919.

APPENDIX

Equations for $V_{m,0}$ and $I_{m,0}$ used in (49-53) for the double-ended DC-AC converter are included below.

$$I_{2,0} = \frac{V_i}{R_i + 2R_{ds,i}} + \left(I_{1,0} - \frac{V_i}{R_i + 2R_{ds,i}} \right) e^{-\frac{R_i + 2R_{ds,i}}{L_{tot}} T_1} \tag{92}$$

$$V_{2,0} = V_i - \left(R_i + 2R_{ds,i} \right) I_{2,0} \tag{93}$$

$$I_{3,0} = I_{2,0} \cos\left(\omega_{res} T_2 \right) + V_{2,0} \sqrt{\frac{C_{tot}}{L_{tot}}} \sin\left(\omega_{res} T_2 \right) \tag{94}$$

$$V_{3,0}(t) = -L_{tot} \omega_{res} I_{2,0} \sin\left(\omega_{res} T_2 \right) + V_{2,0} \cos\left(\omega_{res} T_2 \right) \tag{95}$$

$$I_{6,0} = \frac{-V_{3,5} N}{R_o + 2R_{ds,o}} + \left(I_{3,0} - \frac{V_{3,5} N}{R_o + 2R_{ds,o}} \right) e^{-\frac{R_o + 2R_{ds,o}}{2N^2 K L_{tot}} (T_3 + T_5)} \tag{96}$$

$$V_{6,0} = -\frac{V_{3,5}}{2NK} - \frac{R_o + 2R_{ds,o}}{2N^2 K} I_{6,0} \tag{97}$$

The equations for a switch average and RMS currents in the above equations are:

$$I_{sw,i}^{av} = f_{Link} \times \left[X T_1 + \frac{L_{tot}}{R_i + 2R_{ds,i}} \left(I_{1,0} - X \right) \left(1 - e^{-\frac{R_i + 2R_{ds,i}}{L_{tot}} T_1} \right) \right] \tag{98}$$

$$I_{sw,i}^{rms} = \sqrt{f_{Link} \times \left[\begin{array}{l} X^2 T_1 + \frac{2 L_{tot} X}{R_i + 2R_{ds,i}} \left(I_{1,0} - X \right) \left(1 - e^{-\frac{R_i + 2R_{ds,i}}{L_{tot}} T_1} \right) + \\ \left(I_{1,0} - X \right)^2 \times \frac{L_{tot}}{2\left(R_i + 2R_{ds,i} \right)} \left(1 - e^{-2 \times \frac{R_i + 2R_{ds,i}}{L_{tot}} T_1} \right) \end{array} \right]} \tag{99}$$

$$X = \frac{V_i - 2V_{d,i}}{R_i + 2R_{ds,i}} \tag{100}$$

$$I_{sw,o}^{av} = \frac{f_{Link}}{2NK} \times \left[Y \times (T_3 + T_3) + \frac{2N^2 KL_{tot}}{R_o + 2R_{ds,o}} \left(I_{3,0} - Y \right) \left(1 - e^{-\frac{R_o + 2R_{ds,o}}{2N^2 KL_{tot}} (T_3 + T_5)} \right) \right] \tag{101}$$

$$I_{sw,o}^{rms} = \sqrt{\frac{f_{Link}}{4N^2 K^2} \times \left[\begin{array}{l} Y^2 \times (T_3 + T_5) + \frac{4N^2 KL_{tot} Y}{R_o + 2R_{ds,o}} \left(I_{3,0} - Y \right) \left(1 - e^{-\frac{R_o + 2R_{ds,o}}{2N^2 KL_{tot}} (T_3 + T_5)} \right) + \\ \left(I_{e,0} - Y \right)^2 \times \frac{N^2 KL_{tot}}{R_o + 2R_{ds,o}} \left(1 - e^{-\frac{R_o + 2R_{ds,o}}{N^2 KL_{tot}} (T_3 + T_5)} \right) \end{array} \right]} \tag{102}$$

$$Y = -\frac{N}{2K} \times \frac{V_{3,5} - 2V_{d,o}}{R_o + 2R_{ds,o}} \tag{103}$$

U_1 and U_2 in (63) and (64) are defined below.

$$\begin{aligned} U_1 = {} & \frac{1}{2} \left(I_{2,0}^2 + V_{2,0}^2 \frac{C_{tot}}{L_{tot}} \right) \times \\ & \left[\begin{array}{l} T_2 + \frac{1}{2\omega_{res}} \sin \left(2 \tan^{-1} \frac{I_{2,0}}{V_{2,0} \sqrt{C_{tot} / L_{tot}}} \right) - \\ \frac{1}{2\omega_{res}} \sin \left(2\omega_{res} T_2 + 2 \tan^{-1} \frac{I_{2,0}}{V_{2,0} \sqrt{C_{tot} / L_{tot}}} \right) \end{array} \right] \end{aligned} \tag{104}$$

$$\begin{aligned} U_2 = {} & \frac{1}{2} \left(I_{6,0}^2 + V_{6,0}^2 \frac{C_{tot}}{L_{tot}} \right) \times \\ & \left[\begin{array}{l} T_6 + \frac{1}{2\omega_{res}} \sin \left(2 \tan^{-1} \frac{I_{4,0}}{V_{4,0} \sqrt{C_{tot} / L_{tot}}} \right) - \\ \frac{1}{2\omega_{res}} \sin \left(2\omega_{res} T_6 + 2 \tan^{-1} \frac{I_{6,0}}{V_{6,0} \sqrt{C_{tot} / L_{tot}}} \right) \end{array} \right] \end{aligned} \tag{105}$$

Equations for $V_{m,0}$ and $I_{m,0}$ used in (49-53) for the single-ended DC-AC converter are listed below.

$$I_{2,0} = \frac{V_i}{R_i} + \left(I_{1,0} - \frac{V_i}{R_i}\right) e^{-\frac{R_i}{L}T_1} \tag{106}$$

$$V_{2,0} = V_i - R_i I_{2,0} \tag{107}$$

$$I_{3,0} = I_{2,0}\cos(\omega_{res}T_2) + V_{2,0}\sqrt{\frac{C_{tot}}{L}}\sin(\omega_{res}T_2) \tag{108}$$

$$V_{3,0} = -L\omega_{res}I_{2,0}\sin(\omega_{res}T_2) + V_{2,0}\cos(\omega_{res}T_2) \tag{109}$$

$$I_{6,0} = \frac{-V_{3,5}N}{R_o} + \left(I_{3,0} + \frac{V_{3,5}N}{R_o}\right) e^{-\frac{R_o}{2N^2KL}(T_3+T_5)} \tag{110}$$

$$V_{6,0} = -\frac{V_{3,5}}{2NK} - \frac{R_o}{2N^2K} I_{6,0} \tag{111}$$