MILLIMETER-WAVE CONCURRENT DUAL-BAND BICMOS RFIC FRONT-END MODULE FOR COMMUNICATION AND SENSING SYSTEMS

A Dissertation

by

YOUNGMAN UM

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Chair of Committee,	Cam Nguyen
Committee Members,	Robert D. Nevels
	Chin B. Su
	Binayak Mohanty
Head of Department,	Miroslav M. Begovic

May 2017

Major Subject: Electrical Engineering

ABSTRACT

This dissertation presents new circuit architectures and techniques for improving several key performances of BiCMOS RFIC building blocks that are used in wireless communication and sensing systems operating at millimeter-wave frequencies. The developed circuits and front-end module can be employed in concurrent dual-band transceivers for communication and sensing systems such as phased array and RFID systems.

New 0.18-μm CMOS dual-bandpass filtering single-pole double-throw (SPDT) and transmit/receive (T/R) switches have been developed, and they operate in two different frequency bands centered at around 40 and 60 GHz (Design 1) and 24 and 60 GHz (Designs 2, 3 and 4). Design 1 is a concurrent dual-bandpass filtering T/R switch consisting of three SPDT switches based on a 3rd order band-pass filter with shunt nMOS transistors as the switching function. Design 2 is a 24/60-GHz concurrent dual-bandpass T/R switch consisting of dual-band $\lambda/4$ LC networks and resonators with shunt nMOS transistors as the switching function. Design 3 is a dual-band SPDT and T/R switches, which are capable of band-pass filtering as well as separate and concurrent switching operations in single/dual-band and transmission/reception. These components can act as diplexers with switching functions. Design 4 is a wideband concurrent dual-band SPDT switch with integrated dual-bandpass filtering, which is configured to make it approximately equivalent to a dual-band resonator in the on-state operation.

A fully integrated 24/60-GHz concurrent dual-band LNA utilizing a dual-band LC circuit has been proposed. The LNA is based on a two-stage cascode topology with inductive degeneration. The dual-band LC circuit has the quarter-wavelength characteristic at two different frequencies, and it shows the dual pass-band and single stop-band characteristics when it is connected to the ground in shunt. Due to the cancellation of the stop-band signal and low-pass response by the LC circuit connected to the cascode nodes of the 1st and 2nd stages in the LNA, the LNA presents high stop-band rejection and good gain balance at 24 and 60 GHz.

A concurrent dual-band front-end module (FEM) consisting of a 24/60-GHz dual-band antenna, a five-port T/R switch, two LNAs and one PA has been proposed. The FEM can be employed in systems with dual-polarization, for instance, phased array and RFID reader systems.

DEDICATION

To my beloved my wife Yeomyeong Jeon, son Jisung Joseph Um, daughter Jooah Sophia Um, and my heavenly father

for all their love and the unbelievable support

ACKNOWLEDGEMENTS

This dissertation would have not been completed without many people's help. First of all, I would like to thank my committee chair and advisor, Prof. Cam Nguyen for his guidance, support, and encouragement throughout my doctoral degree period at Texas A&M University.

I sincerely thank my committee members, Prof. Robert Nevels, Prof. Chin Su, and Prof. Binayak Mohanty for their comments and support. I am also grateful to Prof. Kai Chang for his kind encouragement.

I would like to send my thanks to Prof. Jaehoon Choi at Hanyang University, Seoul, Republic of Korea for his encouragement and help.

I would like to express my thanks to Mr. Cody Hale, design engineering manager at Qorvo Inc. He offered me an internship opportunity and I had an excellent experience and he gave me many technical advices during the internship period.

I would like to thank my former and current laboratory colleagues, Dr. Cuong Huynh, Dr. Jaeyoung Lee, Dr. Kyoungwoon Kim, Dr. Donghyun Lee, Dr. Sunhwan Jang, Dr. Chadi Geha, Juseok Bae and Meng-Jie Hsiao for their technical discussions, help, and friendship. I wish them all the best and great success in their careers and life.

I would like to send my thanks to Prof. Byul Hur in the Department of Engineering Technology and Industrial Distribution at Texas A&M University. In spite of the short time, he has given me encouragement and support.

I would like to express my special and deepest appreciation to my family members. I thank my parents, Chonggook Um and Hongsuk Lee for their love, prayers, and support not only during my doctoral degree period but also during my entire life. And, I would like to thank my sister, Jayoung Um for her encouragement. Also, I would like to show my appreciation to my father-in-law and mother-in-law, Insuk Jeon and Boknam Yoon for their constant prayers and support.

I would like to show my thanks to my beloved wife, Yeomyeong Jeon, and two children, Jisung Um and Jooah Um for their love, support and encouragement. I should express my sincere appreciation for their sacrifice. I will give back what they have given me.

Finally, I would like to express all gratitude and appreciation to my heavenly father. He has given me the strength to finish my doctoral degree. I am so grateful for his love, guidance, and support.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

Part 1, faculty committee recognition

This work was supervised by the dissertation committee consisting of Professor Cam Nguyen, Robert D. Nevels and Chin B. Su of the Department of Electrical and Computer Engineering and Professor Binayak Mohanty of the Department of Biological and Agricultural Engineering.

Part 2, student/collaborator contributions

The 24- and 60-GHz power amplifiers (PAs) and 24/60-GHz diplexer depicted in Chapter IV was developed by Dr. Kyoungwoon Kim of the Department of Electrical and Computer Engineering and the 24-GHz PA was published in 2014.

All other work conducted for the dissertation was completed by Youngman Um independently.

Funding Sources

This work was made possible in part by the National Priorities Research Program (NPRP) under Grant Number 6-241-2-102.

Its contents are solely the responsibility of the authors and do not necessarily represent the official views of the Qatar National Research Fund (a member of Qatar Foundation).

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER I

INTRODUCTION

1.1 Introduction and Background

The rapid emergence of numerous applications of radar, sensing, and wireless communications in many areas such as public communications, item management, transportation safety, health care, military and etc. has resulted in a substantial movement toward novel circuit topologies and techniques with improved performances, low cost and high level of integrations using CMOS and BiCMOS technologies. Meanwhile, increasing interests in larger bandwidths lead integrated circuits to move toward higher frequencies [1]. Also, there are huge amounts of applications in low frequencies, and most of the frequencies have been already allocated and used. Furthermore, the needs of 5-G wireless frequency bands have been looming large. Therefore, applications at higher frequencies such as millimeter-wave (mmW) frequencies have more interests in researches. Industrial, Scientific and Medical (ISM) bands such as those around 24-GHz band (22–29 GHz), 60-GHz band (57–64 GHz) and 77-GHz bans (77–81 GHz) at mmW frequencies have been allocated as unlicensed frequency bands. Table 1.1 shows advantages, disadvantages, and possible applications at the frequencies. Increased bandwidth leads to high data rate communication, which is calculated as [2]

$$C = B * \log_2\left(1 + \frac{S}{N}\right) \text{ [bps]} \tag{1.1}$$

Table 1.1
24, 60 and 77 GHz Frequency Characteristics

Operating Frequency	Advantages	Disadvantages	Possible Applications
24 GHz (22–29 GHz)	-Low attenuation in air -High isolation between floors -Higher data rate -Long range possible	-Less possible antenna on-chip	-Vehicle anti-collision -Vehicle identification -Parking management -Electronic toll collection
60 GHz (57–64 GHz)	-High data rate -Possible antenna on-chip -Spatial isolation -Higher implicit security	-High attenuation in air -Only indoor application -Interference with home networking system -High power consumption	-Indoor application -Short range communication
77 GHz (77–81 GHz)	-High directivity possible -Possible antenna on-chip -Long detection range -can be used with car radar -Less interference	-High power consumption	-Vehicle anti-collision -Vehicle identification

, where C is maximum capacity of the channel, B is bandwidth of the channel, S/N is signal-to-noise ratio (SNR).

Also, the shorten wavelength at mmW frequencies can lead to the miniaturization of the entire communication system. Especially, for antenna design, not only an on-chip antenna but also an array antenna can be implemented, and this feature can be an important advantage to implement communication systems at mmW frequencies beyond the systems implemented at low frequencies. As shown in Table 1.1, these inherent characteristics of the mmW frequencies can be employed in a variety of applications, e. g. short- and long-distance communication systems, vehicle radar system

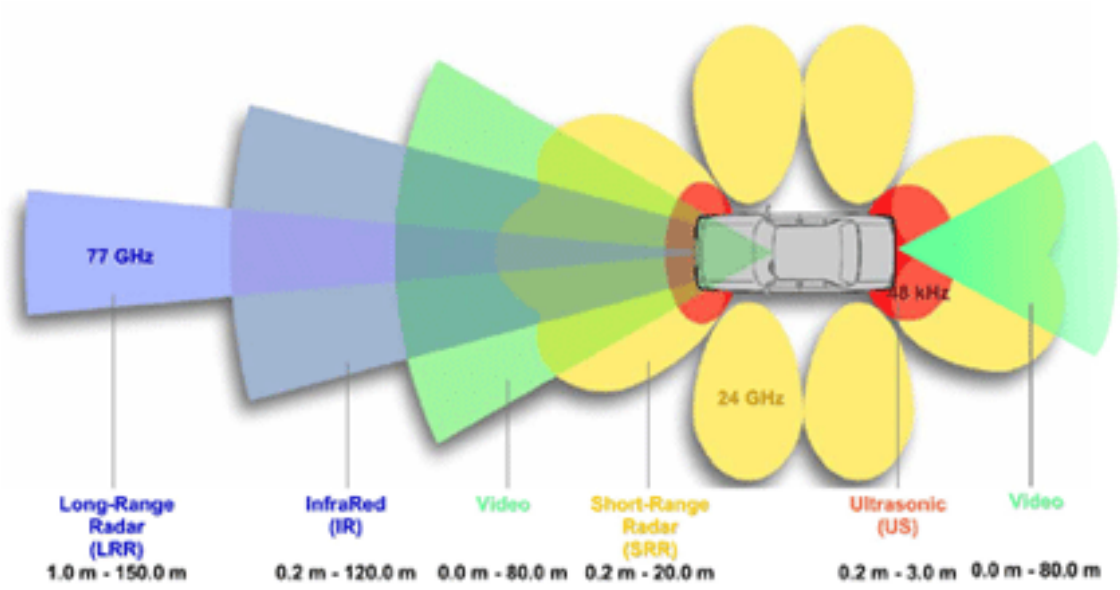


Fig. 1.1. Vehicle radar system.

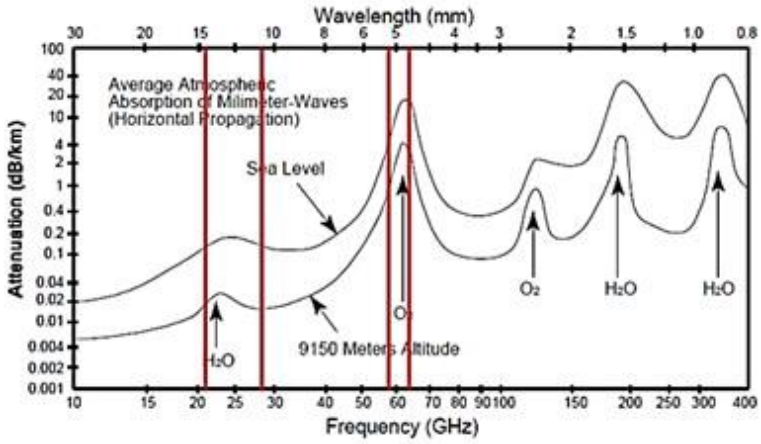


Fig. 1.2. Air attenuation at microwave and millimeter-wave frequencies.

(also called Vehicle anti-collision system), and 60-GHz indoor network system. Fig. 1.1 shows the vehicle radar system and the functions of operating frequencies. In the system, 24 and 77-GHz frequencies are utilized as short- and long-distance radar

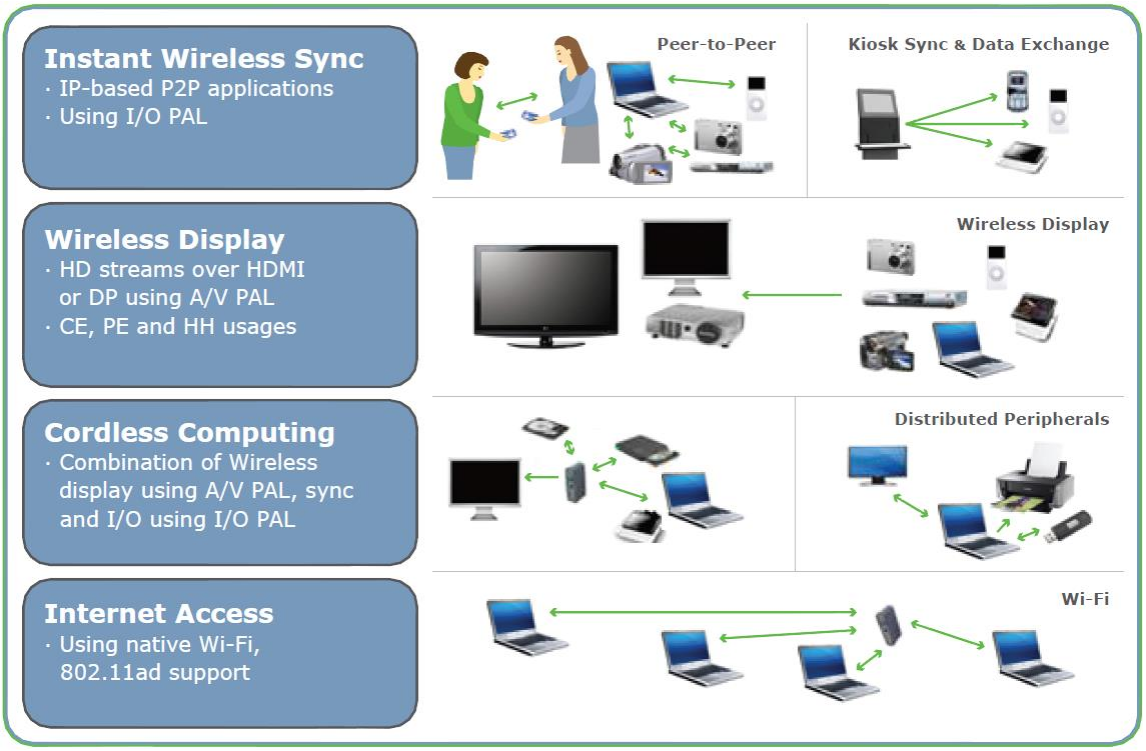
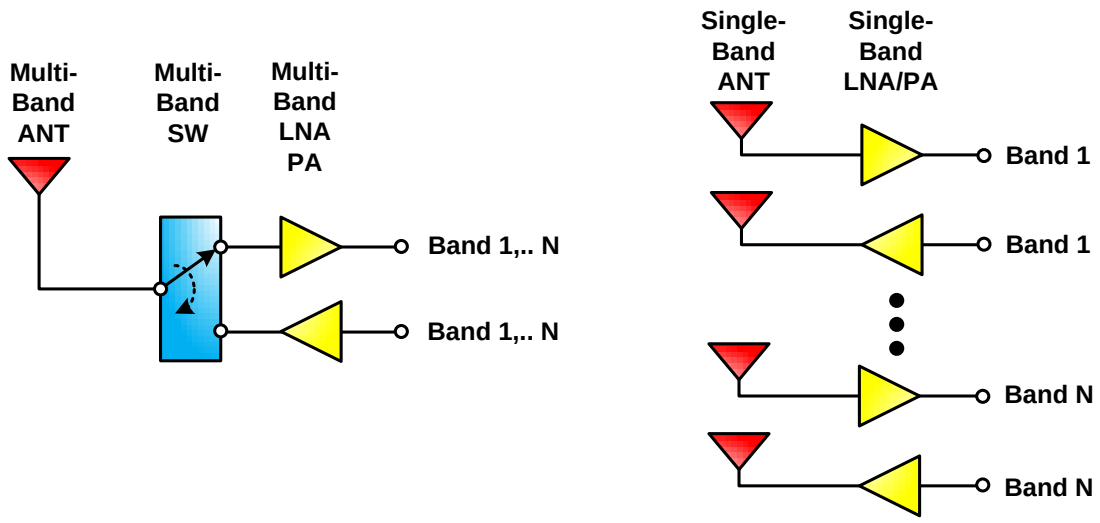


Fig. 1.3. Applications for 60-GHz communication systems.

communications, respectively, and for anti-collision systems. The 60 GHz band is a very interesting frequency band that has high air attenuations as shown in Fig. 1.2. Due to this fact, it is mainly used as short-distance or indoor communications and security solutions as shown in Fig. 1.3. Since the bandwidth (BW) of the 60-GHz communication band is 7 GHz (57–64 GHz), the data rate reaches up to several Gbps. It means that high definition uncompressed streaming video, interactive gaming, digital photography, digital home movies and data and file transfer are possible, which can lead to a connector free platform and a muti-gigbit cloud connectivity.



(a) (b)

Fig. 1.4. Block diagram of a multi-band system: (a) One multi-band system and (b) multiple and parallel system operating at different operating frequency bands.

Table 1.2
Characteristic Summary of Dual-Frequency Combinations

Frequency Combination	Advantages	Disadvantages
24 / 60 GHz	- Long and short range communication - Direct conversion system (Simpler architecture)	- Difficult on-chip 24-GHz Antenna
24 / 77 GHz	- Long range communication	- Already used for vehicle anti-collision (co-channel interference) - Heterodyne structure (complex structure) - Difficult on-chip 24-GHz Antenna
60 / 77 GHz	- Long and short range communication	- Already used for vehicle anti-collision (co-channel interference) - Heterodyne structure (complex structure) - Very high-Q BPF(Switch) required at 77 GHz

Also, the huge 7-GHz BW is used as a high-data rate wireless connectivity such

as IEEE 801.11ad for the next-generation WiFi (also call WiGig) and IEEE 802.15.3c standards for Wireless Personal Area Network (WPAN) [3].

Multi-band RF systems in Fig. 1.4(a) have provided numerous advantages and have more capabilities as compared to single-band counterparts in Fig. 1.4(b). The ability of operating multiple bands increases the diversity of RF systems for sensing and communication functions at multiple frequencies. Moreover, achieving concurrent functions over multiband enables a single RF system to be used at multiband simultaneously – avoiding the need of physically combining separate RF systems, each working in an individual band, together, which is difficult (and expensive) to realize in practice – particularly when many bands are involved. This leads to improvement in size, cost and power consumption. Table 1.2 shows advantages, disadvantages and possible applications for possible dual-frequency combinations for dual-band systems. Among the frequency combinations, 24- and 60-GHz frequency combination has been selected due to their simplicity and versatility for this research.

In this dissertation, a 24/60-GHz concurrent dual-band BiCMOS front-end module applicable to RFID, phased array and communication systems has been proposed. Especially, the designs of a switch, a LNA and a front-end module, which consists of switch, LNA and PA, will be described in the following sections.

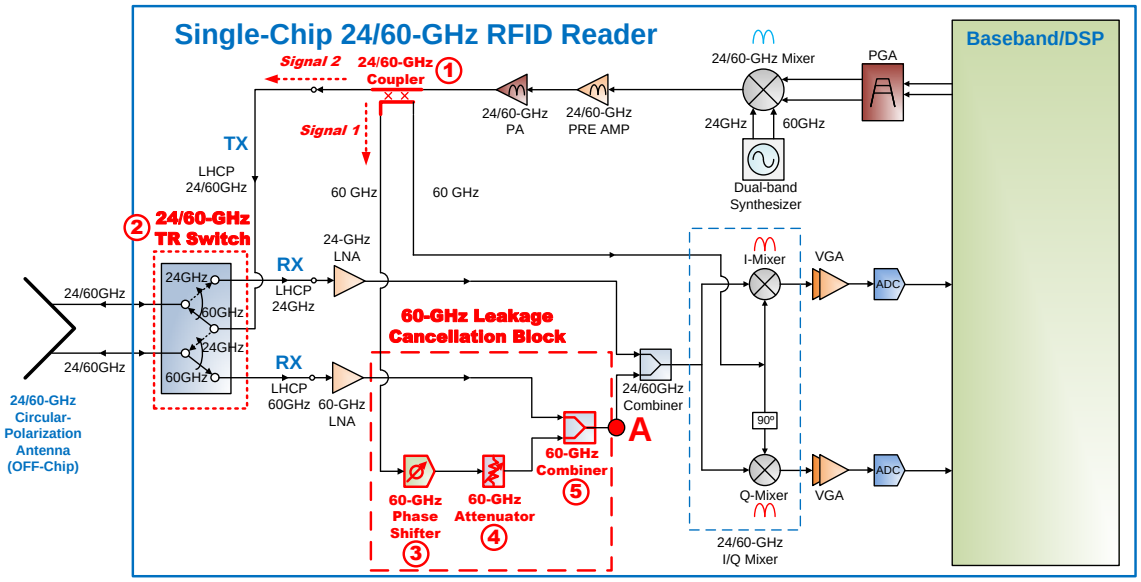


Fig. 1.5. Block diagram of the proposed 24/60-GHz dual-band RFID reader system.

1.2 System Description

1.2.1 A 24/60-GHz Dual-Band Dual-Mode RFID Reader System

A RFID system fundamentally consists of a RFID reader and a tag. A RFID reader transmits signals to a tag, then, the tag back-scatters its information to the reader. According to with or without battery in the tag, active and passive RFIDs are classified, respectively [4]. In this chapter, the RFID system using dual circular polarization, e. g. left- and right-handed circular polarizations, and dual modes, e. g. active and passive modes, has been proposed. Operating frequencies are 24 and 60 GHz that are employed for active and passive RFID systems, respectively.

Fig. 1.5 shows the block diagram of the proposed 24/60-GHz dual-band RFID reader system with a shared two-port antenna for receiving and transmitting operations. While the 24-GHz active RFID system works in separate transmitting (TX) and

receiving (RX) operations, the 60-GHz passive RFID system operates in simultaneous TX and RX operations. In passive RFID system, circulator, in which a signal entering any port is transmitted to the next port in rotation, is used as a front-end component and the circulator should have a low insertion loss and noise figure, and high linearity and isolation. Even though on-chip circulators show good isolation, they show poor linearity and noise figure [5], [6] and are not desirable for fully integration. Furthermore, signal leaked from TX port to RX port can be problematic in passive RFID systems.

To solve this problem, a TX leakage cancellation (TLC) technique has been proposed in the system. The TLC system consists of 24/60-GHz coupler (①), 24/60-GHz T/R switch (②), 60-GHz phase shifter (③), 60-GHz attenuator (④) and 60-GHz combiner (⑤) as shown in Fig. 1.5. The T/R Switch consists of two 24-GHz and two 60-GHz SPST switches, which are placed alternately, and has five ports. The T/R switch will be described in Sec. 2.4. In the 60-GHz passive RFID operation, transmitted signals from PA output are classified as two signals: one is a coupled signal (***signal 1*** in Fig. 1.5) by a coupler (①) and another is a thru signal (***signal 2*** in Fig. 1.5) via the coupler (①), respectively. Although the ***signal 2*** can be leaked from TX port to 60-GHz RX port in the T/R switch (②), the signal is attenuated due to high isolation by off-state 24-GHz SPST switch between TX port and 60-GHz RX port. Since, however, some of the ***signal 2*** can also be leaked into the receiver through antenna's another port without radiating at antenna and the signals are amplified by LNA, which can be harmful to the receiver, and

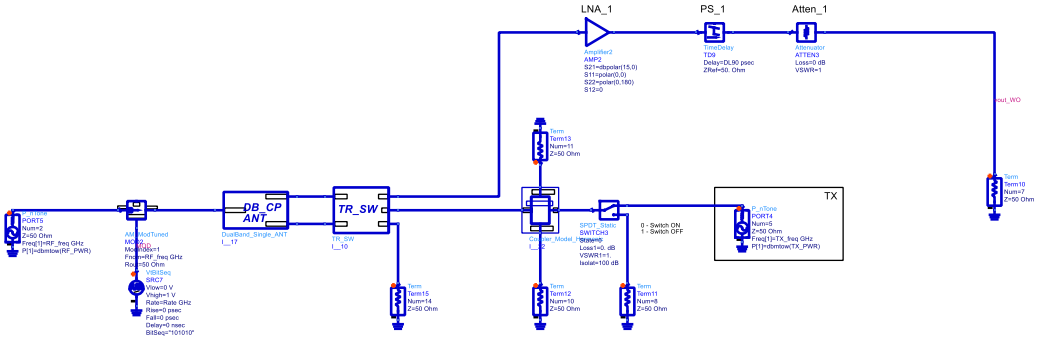


Fig. 1.6. ADS Simulation setup to verify the TX leakage cancellation technique.

Table 1.3
Simulation Setup Parameters

TX output power (PA output)	10 dBm
RX input power (T/R switch input)	-30 dBm
TX, RX carrier frequency	60 GHz
Modulation	ASK, modulation index: 1

the hence leaked signals should be canceled out. To cancel out the leaked signals, the ***signal 1*** is directed to go through the 60-GHz phase shifter (③) and attenuator (④), and meet the ***signal 2***, which is leaked from antenna and amplified by LNA, at node '***A***' in Fig. 1.5. Eventually, the two signals will be canceled out due to their same magnitude and 180-deg out of phase.

To evaluate the performance of the TLC technique, Fig. 1.6 shows the ADS [7] simulation setup consisting of antenna, T/R switch, coupler, LNA, phase shifter and attenuator with simulation setup parameters listed in Table 1.3. Fig. 1.7 shows the simulated result of the signals at input (***Combiner_IN1*** and ***Combiner_IN2***) and output (***Combiner_OUT*** at node 'A') of 60-GHz combiner (⑤).

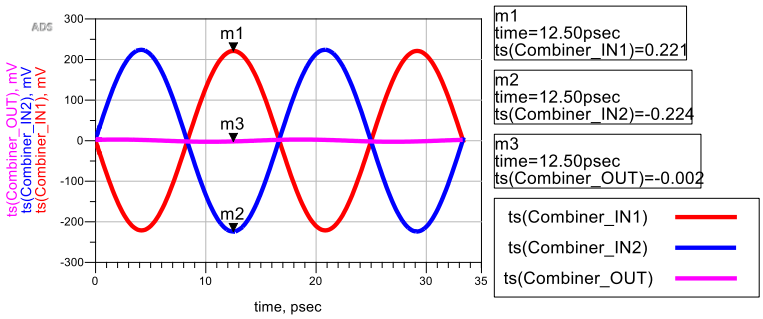


Fig. 1.7. Simulated results of the signals' cancellation at 60-GHz Combiner's output.

Two input signals have the same magnitude and 180-deg out of phase, and then the signals are canceled out at the output. The cancellation ratio is calculated as

$$Cancellation\_ratio = -20\log_{10}\left(\frac{Combiner\_OUT}{Combiner\_IN2}\right) \tag{1.2}$$

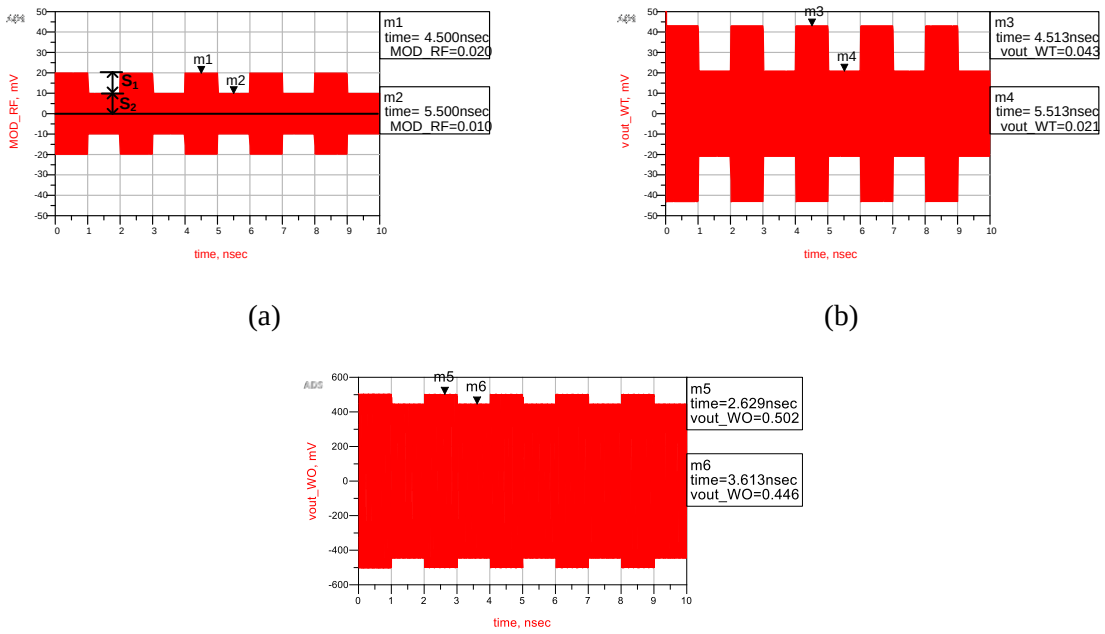
The simulated cancellation ratio is around 40 dB.

Fig. 1.8 shows the simulated results of an ASK modulation index in Fig. 1.8(a) defined as

$$Modulation\_index = \frac{S_2}{S_1} \tag{1.3}$$

Figs. 1.8(a), (b) and (c) show the modulated incoming RF signal at the antenna and the signals at the combiner output (node 'A' in Fig. 1.5) with and without TLC technique, respectively.

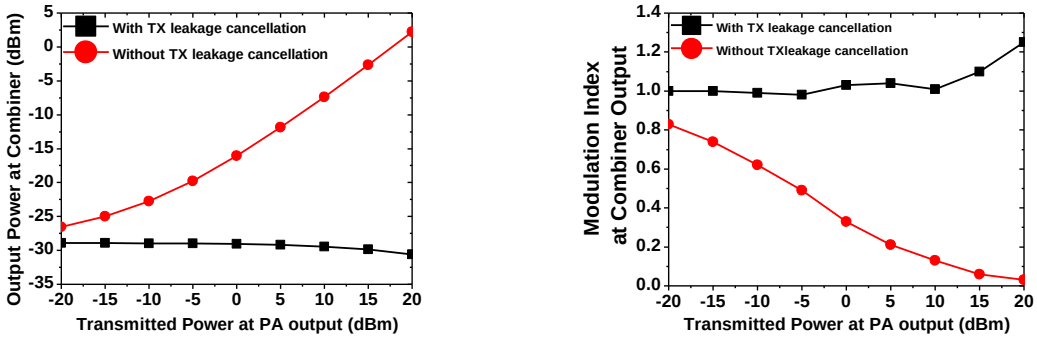
With TLC technique, while the modulation index is kept as around 1, the modulation index deteriorates due to leaked TX signal without TLC technique.



(a) (b)

(c)

Fig. 1.8. Simulated result comparison for modulation index at the combiner's output: (a) ASK modulation RX input signal, (b) output signal at the combiner's output with TX leakage cancellation block, and (c) output signal at the combiner's output without TX leakage cancellation block.



(a) (b)

Fig. 1.9. Simulation results comparison for signal power and modulation index at combiner's output: (a) output powers at combiner's output and (b) modulation index at combiner's output.

Fig. 1.9 shows the signal power level at combiner output (node 'A' in Fig. 1.5)

with respect to the transmitted power at PA output, which will be potentially expected as the signal power leaked from the antenna, with and without TLC technique. With TLC technique, the modulation index and the signal power are kept stable regardless of transmitted power at the PA output. However, without TLC technique, the signal power leaked from the antenna increases, and the modulation index significantly decreases as the transmitted power increases. Therefore, the TLC technique prevents TX leakage signals from coming to the receiver effectively.

1.2.2 A 24/60-GHz Concurrent Dual-Band Phased Array System

Phased array system has some advantages beyond single antenna systems. Representative features are to improve the signal to interference plus noise ratio (SINR), to increase output power by increased antenna gain, and to implement beamforming [8], thus the phased array system is often employed in a radar system. The total transmitted output power is calculated as equivalent isotopically radiated power (EIRP) as

$$EIRP[dB] = P_t - L + G\,,\ G_{array}[dB] \cong G_s + 10\log n \tag{1.4}$$

, where P_t is the transmitted power at PA output, L is the loss by antenna mismatch, and G is the antenna's gain, G_{array} is the array antenna's gain consisting of n-single antenna, n is the number of single antennas and G_s is the single antenna's gain.

In the array system, equation (1.4) says that the gain of total array antenna increases compared to that of single antenna, and total transmitted output power is higher than that of single-antenna system [9].

In the phased array system, beam scanning angle (or main lobe angle) can be determined according to the phase difference by a phase shifter and an array antenna structure. For instance, the scanning angle of a sixteen-element linear array in the same distance can be calculated as [9]

$$\theta = \sin^{-1}\left(\frac{\psi}{2\pi\left(d/\lambda\right)}\right) \tag{1.5}$$

, where θ is the scanning angle, ψ is the phase shift across the array, d is the distance between each antenna. Since the main lobe of the radiation pattern is generated at the angle (θ), directive communication at θ is possible.

Fig. 1.10 shows a block diagram of the proposed 24/60-GHz concurrent dual-band transceiver for a phased array system. The system consists of sixteen-identical front-end modules, which constitute an antenna, a T/R switch, a LNA, a PA, an attenuator and a phase shifter. Also, the system employs a dual polarization such as a vertical and horizontal polarization, and it can lead to improve object detection accuracy. In this dissertation, the 24/60-GHz concurrent dual-band T/R switch, which is shown inside the dashed box in Fig. 1.10, has been designed, fabricated and measured. It will be described in Sec. 2. 3.

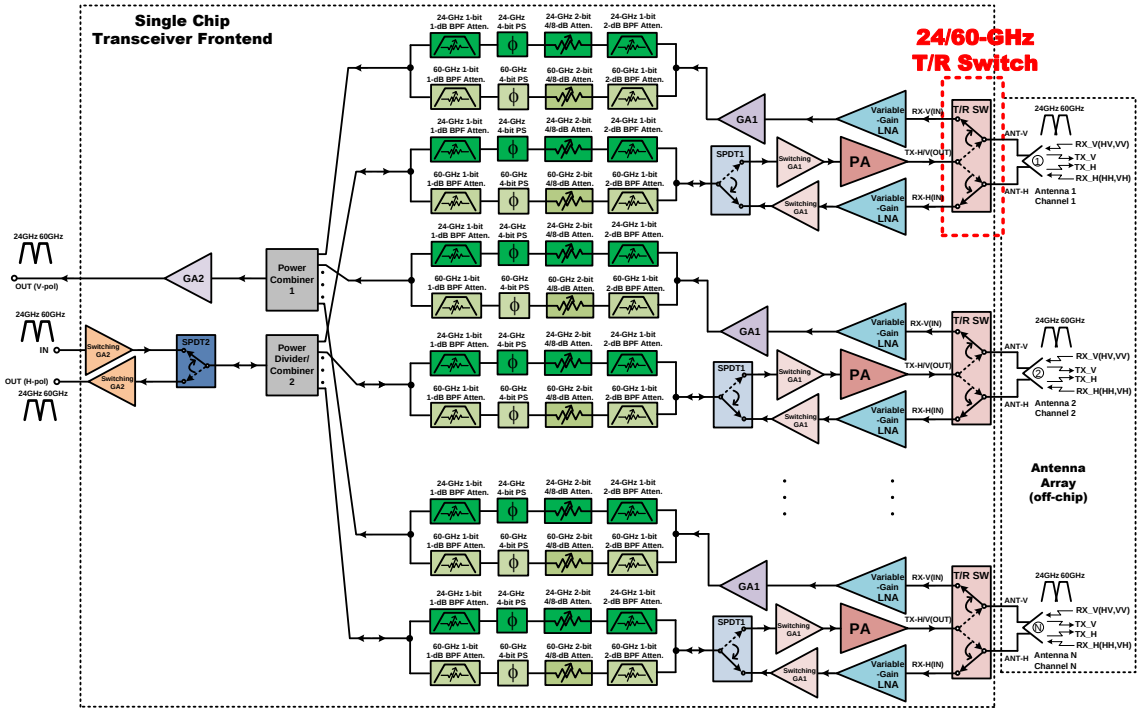
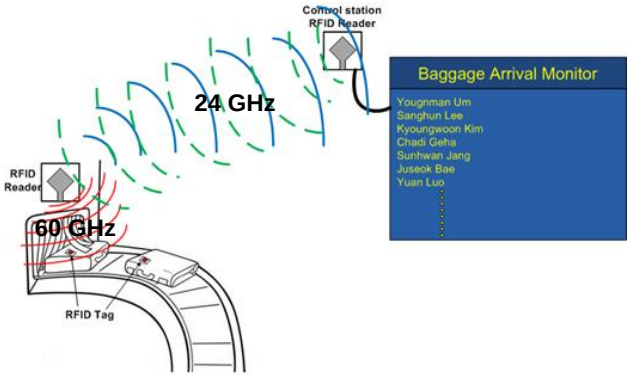


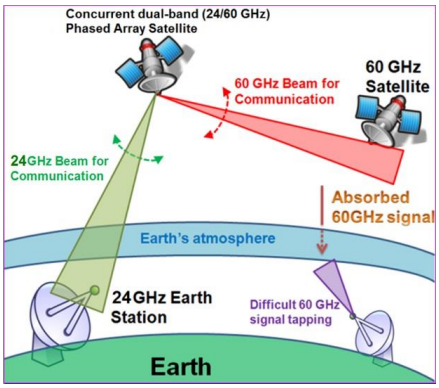
Fig. 1.10. Block diagram of the proposed 24/60-GHz concurrent dual-band transceiver for phased array system.

1.2.3 Possible Applications

Using the dual frequencies, some applications can be implemented as shown in Fig. 1.11. Fig. 1.11(a) shows a RFID baggage tracking system employing 24-GHz long- and 60-GHz short-distance communication characteristics. Since there are a lot of similar-sized, -colored and -shaped bags on the baggage claim conveyor belt in airports, it is difficult to find one's own bag easily. Therefore, the dual-band RFID system can be applicable to this situation. Baggage tags (having RFID tags) communicate with a RFID reader installed on the baggage conveyor via 60 GHz, and the RFID reader communicates with another RFID reader connected to a baggage arrival monitor via 24



(a)



(b)

Fig. 1.11. Possible applications: (a) 24/60-GHz RFID baggage tracking system and (b) 24/60-GHz satellite communication system.

GHz to show the passengers whose baggage arrives. Fig. 1.11(b) shows the radar application for a satellite communication system, and it utilizes air attenuation rate's difference at 24 and 60 GHz. Because the 60-GHz signal is easily absorbed by the earth's air, 60 GHz is only used for satellites' inter-communication. On the other hand, satellites communicate with the radar station on the earth via 24 GHz.

1.3 Dissertation Organization

This dissertation presents several new circuits and techniques to improve performances of some essential CMOS and BiCMOS RFIC components operating at millimeter-wave frequencies (K, Ka and V bands), and the integration of concurrent dual-band front-end module operating at K and V bands applicable to phase array and RFID communication systems.

Chapter II begins with the fundamentals of RF switches, and then introduces four different dual-band switches with band-pass filtering function. Their design, analysis and measurement results are presented. In Chapter III, a concurrent dual-band LNA is described. To obtain dual-band characteristic, dual-band quarter-wavelength LC network has been employed. Chapter IV presents the concurrent dual-band front-end module consisting of dual-band T/R switch described in Chapter II, dual-band LNA proposed in Chapter III and dual-band PA contributed by a lab colleague. Finally, in Chapter V, the conclusion and summary of this dissertation is provided.

CHAPTER II

CMOS DUAL-BAND BAND-PASS FILTERING SWITCH*

2.1 Background and Motivation

A RF switch is an important component in RF/millimeter-wave communication and radar systems. Moreover, it is important due to the switch functions as a circuit that selects one among several branches, e. g. transmitting and receiving branches. The RF switch can be generally employed in Time Division Duplexing (TDD) systems consisting of transmitter, receiver, switch, and one shared antenna [10]. In Frequency Division Duplexing (FDD), the switch can be implemented with branches operating at different frequency bands.

For the switch design, traditionally, Gallium arsenide (GaAs) switches have been used because of their low on-resistance and off-capacitance, and high linearity at high frequencies [11]. Since Silicon-On-Insulator (SOI) technology reduces capacitive coupling with substrate due to a buried oxide layer and is implemented on high resistivity substrate, the switches on SOI have shown low-insertion loss and high-isolation characteristics [12]–[15]. However, due to the improvement of CMOS process, the performance of CMOS switches has been improved. As a result, CMOS switches became an alternative solution that can replace expensive GaAs and SOI switches in low cost, low power applications [11].

* Copyright 2017 Reproduced by permission of the Institution of Engineering & Technology, from Um Y, Nguyen C. High-Isolation Multi-Port Millimetre-Wave CMOS Dual-Band T/R Switch with Integrated Band-Pass Filtering Function. IET Microwaves, Antennas & Propagation. 2017 Jan 29; 11(2):253-9, and Y. Um and C. Nguyen, "A Millimeter-Wave CMOS Dual-Bandpass T/R Switch with Dual-Band LC Network," *IEEE Microw. Wireless Compon. Lett*., in progress

Transmit/receive (T/R) and single-pole double-throw (SPDT) switches are often being used in RF transceivers. For receiving operation, RF signals pass through (on-chip or off-chip) band-pass filter (BPF), switch and LNA to receiver. For transmitting operation, the RF signals amplified by PA pass through the switch and BPF. In RF transceivers, external band-pass filters are normally used together with T/R switches to reduce undesired out-of-band signals. While these separate band-pass filters can be implemented as off- or on-chip components, they tend to increase the size and cost of the overall system. A more effective approach is to integrate the band-pass filter function with switches to make a dual-function (switching and filtering) simultaneously.

In this chapter, new 0.18-μm CMOS dual-band band-pass filter SPDT and T/R switches are proposed. They can operate in two different frequency bands centered at around 40 and 60 GHz, as well as 24 and 60 GHz.

2.1.1 MOSFET with Deep N-Well

Body-floating technique and deep *n*-well transistors are used to prevent RF signals from the *p*-substrate leaking into the bulks of the transistors. Hence, they can isolate the bulks of the transistors from the *p*-substrate and, in turn, increasing the isolation of the transistors [16], [17]. Fig. 2.1 shows a cross sectional view and equivalent circuits of nMOS transistors with deep *n*-well (DNW). In order to maximize the isolation, the isolated *p*-well and DNW are biased at 0 V and 1.8 V (V_{dd}) through large resistors, R_{ip} (10 *k*Ω) and R_d (20 *k*Ω), respectively. If the high voltage (higher than threshold voltage, Vth) is applied to the gate, the transistor connects (ON-state) the

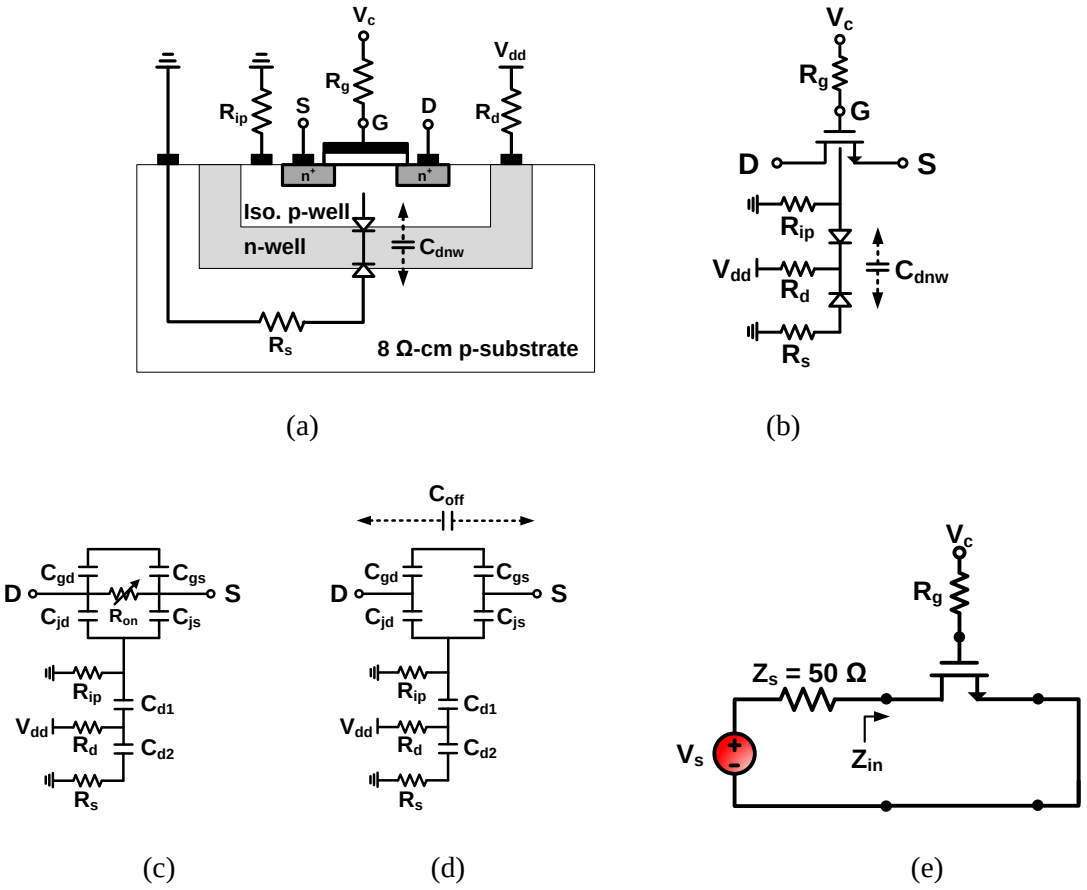


Fig. 2.1. Cross sectional view of a deep n-well transistor: (a) schematic (b) equivalent model when V_c = 1.8 (c) and 0 V (d), and (e) simulation set-up to obtain R_{on} and C_{off}.

source and the drain together. On the other hand, the transistors disconnect (OFF-state) the source and the drain if low voltage is applied to the gate [18]. Fig. 2.1(c) and (d) show the on- and off-state nMOS transistors with DNW that are approximately equivalent to the on-resistor (R_{on}) and equivalent capacitor (C_{eq}), respectively. The R_{on} and C_{eq} can be calculated as

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{th}\right)} \tag{2.1}$$

, where μ_n is the majority-carrier mobility of the nMOS transistor with DNW, C_{ox} is the gate oxide capacitance, W is the width of the transistor, L is the length of the transistor, V_{GS} is a voltage between the gate and source, V_{th} is threshold voltage [18].

The equivalent capacitance C_{eq} of the on- and off-state nMOS transistor with DNW consists of the gate-source (C_{gs}), gate-drain (C_{gd}), junction (C_{js} and C_{jd}), and deep n-well (C_{dnw} consisting of C_{d1} and C_{d2}) capacitances [19].

Fig. 2.1(e) also shows the schemetic to simulate R_{on} and C_{off} of on- and off-state nMOS transistors with DNW, where they can be determined as

$$R_{on} = real(Z_{in\_on}) \text{ and } C_{off} = \frac{1}{2\pi f * imag\left(Z_{in\_off}\right)} \tag{2.2}$$

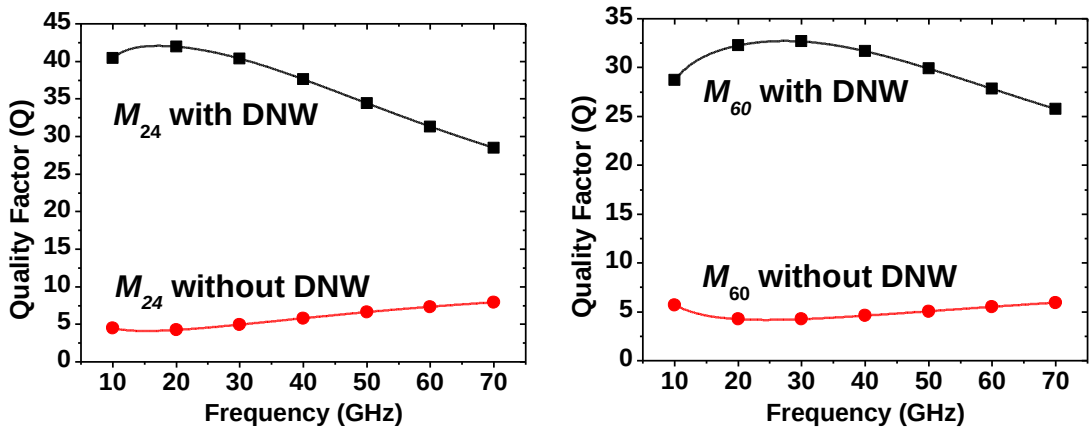
, where Z_{in_on} and Z_{in_off} are the input impedances when the nMOS transistor with DNW is on and off state, respectively.

The nMOS transistor with DNW is biased in off-state and the quality (Q) factor of their equivalent off-capacitor C_{off} affects the switch performance. Fig. 2.2 shows the simulated Q-factor of the off-state transistors (M_{24} and M_{60}) with and without DNW using the simulation setup in Fig. 2.1(e) and obtained as

$$Q = \frac{1}{2\pi f * real\left(Z_{in\_off}\right) * C_{off}} \tag{2.3}$$

, where Z_{in_off} and C_{off} are again the input impedance and off-capacitance when nMOS transistor with/without DNW is off state, respectively.

Widths/lengths of the M_{24} and M_{60} are 420 µm/0.18 µm and 240 µm/0.18 µm, respectively. The simulated Q-factors are 41.5/4.5 and 27.8/5.5 at 24 and 60 GHz



(a) (b)

Fig. 2.2. Simulated Q for off-state nMOS transistors: (a) M_{24} and (b) M_{60} with/without DNW.

with/without DNW, respectively. As shown in Fig. 2.2, it is verified that the Q-factor of the off-state transistors with DNW is much higher than that of off-state transistor without DNW, and nMOS transistor with DNW structure can be used to achieve the low insertion loss for the switch design.

2.1.2 Trade-Off for Typical Switch Topology

Performances of the switch can be evaluated as its insertion loss (IL), isolation (ISO), figure of merit (FOM) such as R_{on}*C_{off}, P_{1dB} and IP_3. They will be described in the following sub-sections.

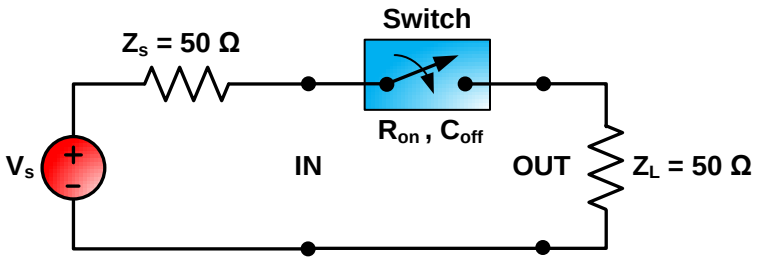


Fig. 2.3. RF switch model in a 50-Ω network.

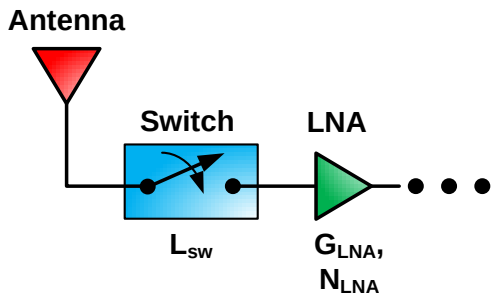


Fig. 2.4. Typical RF receiver chain for total noise figure (NF) calculation.

Insertion Loss

Insertion loss (IL) is the attenuation between input and output ports of the on-state switch. Since the R_{on} of the switch is a loss factor of the switch, the IL of the switch in Fig. 2.3 can be calculated as

$$IL = -20\log_{10}\left|\frac{Z_L + Z_s}{Z_L + Z_s + R_{on}}\right| \text{ [dB]} \qquad (2.4)$$

From (2.4), in order to get lower IL, R_{on} should be as low as possible. Fig. 2.4 shows a typical RF receiver chain, and equation (2.5) is the total noise figure (NF) calculation of the receiver chain. The IL and NF of the switch and LNA directly effects on the total NF of the receiver according to

$$NF_{total} = L_{sw} + \frac{N_{LNA} - 1}{L_{sw}^{-1}} + ... = L_{sw} \cdot N_{LNA} + ... \quad (2.5)$$

Therefore, to reduce the total NF of the receiver, the IL of the switch should be as low as possible or the switch should be located after a LNA amplifier with a high gain.

Isolation

Isolation (ISO) is defined as the attenuation not only between the input and output in the off-state SPST switch, but also between the on- and off-state outputs in a SPDT or a multi-port switch. The ISO of the switch can be calculated as

$$ISO = -20\log_{10}\left|\frac{Z_L + Z_s}{Z_L + Z_s + 1/j\omega C_{off}}\right| \text{ [dB]} \quad (2.6)$$

From (2.6), in order to get higher ISO, C_{off} should be as low as possible.

Figure of Merit (FOM)

Figure of Merit (FOM) is a performance factor to evaluate the switch. In general, FOM of the switch is defined as

$$FOM = R_{on} * C_{off} \text{ [s]} \quad (2.7)$$

, where R_{on} and C_{off} are the on-resistance and off-capacitance of the nMOS transistor, respectively. Equation (2.7) says that lower FOM can be obtained by lower R_{on}, which means lower insertion loss, and lower C_{off}, which means higher isolation.

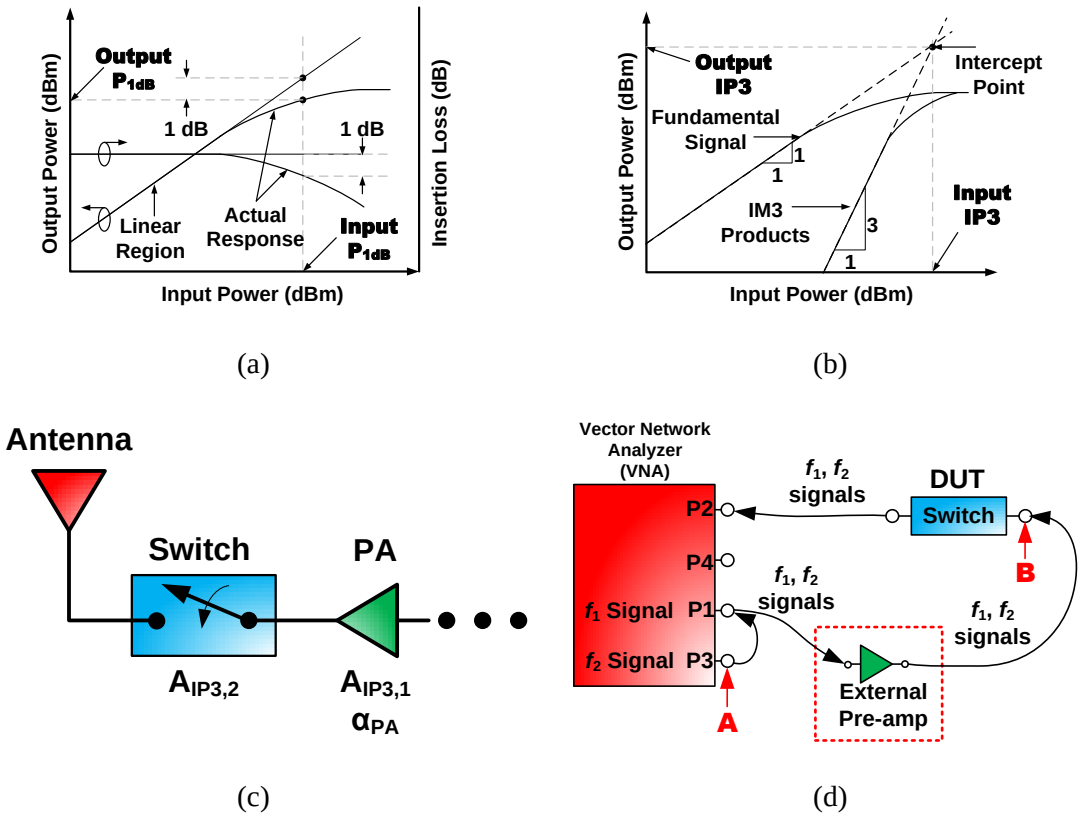


Fig. 2.5. Descriptions of (a) P_{1dB}, (b) IP_3, (c) cascaded nonlinear stages, and (d) measurement set-up for dual-tone signal.

Power Handling Capability and Nonlinearity

Power handling capability and nonlinearity of the switch can be evaluated as P_{1dB} and IP_3 of the switch. Figs. 2.5(a) and (b) show the descriptions of the input and output P_{1dB}, and the input and output IP3 with respect to input power levels, respectively. P_{1dB} is the gain (or loss) 1-dB compression point. As the power level of the fundamental tones injected to the device under test (DUT) increases, the DUT maintains constant gain or loss. However, the gain or loss starts to drop or increase at certain power level. The P_{1dB} is the 1-dB gain drop point or 1-dB loss increment

point and means how much power the DUT can handle. IP_3 is the third order intercept point. When two closely spaced fundamental tones (f_1 and f_2) are injected into the DUT, the DUT generates inter-modulation products due to its nonlinearity characteristic. Among the products, the 3rd order inter-modulation products (also called as IM3 products in Fig. 2.5(b)) such as $2*f_1-f_2$ and $2*f_2-f_1$ can be serious because they can be located close to the fundamental tones and distort them. As the fundamental tones' power level increases, the IM3 products' power level also increases by three times of the fundamental signal's increment. The two signals' power levels are same at certain power level. This power level is the IP_3 point that measures how linear the DUT is. Since the switch is typically located after PA in transmitter as shown in Fig. 2.5(c), the nonlinearity of the latter components becomes more critical [20], [21], hence the power handling capability of the switch should be as high as possible and equation (2.8) explains the reason.

$$\frac{1}{A_{IP3}^2} \approx \frac{1}{A_{IP3,1}^2} + \frac{\alpha_1^2}{A_{IP3,2}^2} \tag{2.8}$$

, where A_{IP3} is the total IP_3 magnitude of the cascaded nonlinear stage in Fig. 2.5(c), $A_{IP3,1}$, $A_{IP3,2}$ are the IP_3 magnitudes of the PA and the switch, respectively, and α_{PA}^2 is the gain of PA.

Fig. 2.5(d) shows the simplest two-tone (f_1 and f_2) measurement setup for P_{1dB} and IP_3. To generate the two-tone signals, f_2 signal from Port 3 is combined with f_1 signal at Port 1 through an internal combiner in the VNA as shown in Fig. 2.5(d) and then the combined signal (f_1 and f_2) is injected to the DUT (switch). While the input

power level at 'B' in Fig. 2.5(d) injected to the switch could reach higher level than the anticipated power handling capability of the switch, the output power level at 'A' in Fig. 2.5(d) can be limited at millimeter-wave frequencies. In order to increase the input power level for the DUT, additional external pre-amp is normally used as shown in Fig. 2.5(d).

2.1.3 Basic Switch Topology

A switch can be classified as Single Pole Single Throw (SPST), Single Pole Double Throw (SPDT), Single Pole Multi Throw (SPxT), Multi Pole Multi Throw (xPxT), Transmit and Receive (T/R) switches and etc. Most fundamental structure is SPST switch and other switches are generally implemented by combining several identical SPST switches together with one common input port.

Fig. 2.6 shows two fundamental topologies for SPDT switches. Figs. 2.6(a) and (b) show series switch and its equivalent circuit. When V_{c1} is biased at 1.8 V in Fig. 2.6(a), the IL and ISO of on- and off-state branches are derived as

$$IL = -20\log_{10}\left|\frac{2*Z_0}{2*Z_0 + R_{on\_M1}}\right| \text{ and } ISO = -20*\log_{10}\left|\frac{2*Z_0}{2*Z_0 + 1/j\omega C_{off\_M2}}\right| \quad (2.9)$$

, where Z_0 is the terminating impedance of ports 1, 2 and 3.

According to (2.9), in this switch, increasing the width of the series nMOS (M_1 and M_2) improves the insertion loss of the switch as R_{on} decreases according to (2.1). However, it can deteriorate the isolation of the switch because of the increased parasitic capacitance

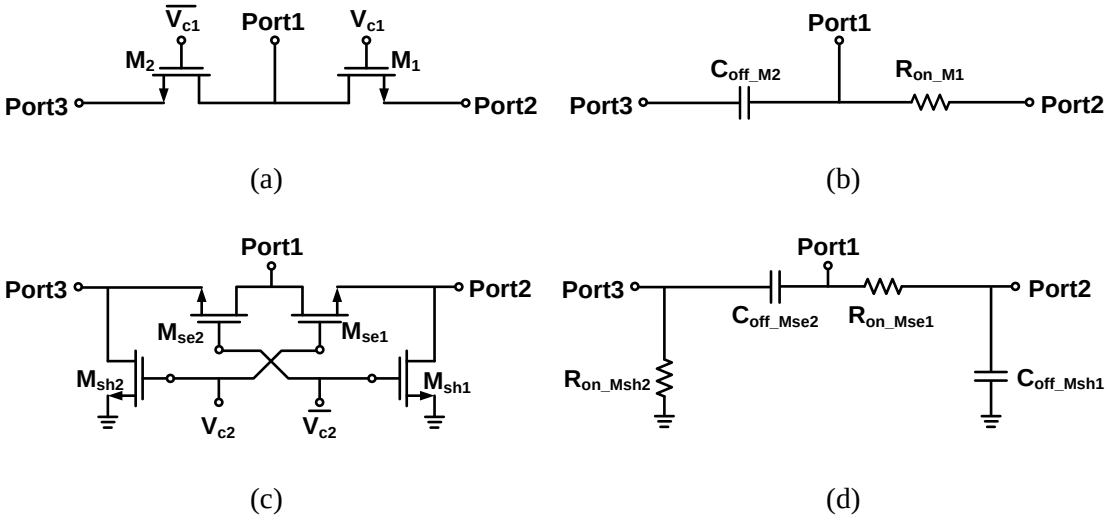


Fig. 2.6. Fundamental SPDT switch topologies: (a) series switch, (b) equivalent circuit of (a) when V_{c1} = 1.8 V, (c) series-shunt switch, and (d) equivalent circuit of (c) when V_{c2} = 1.8 V.

that results from the widened widths, which results in more signal leakage from the input to output.

On the other hand, Fig. 2.6(c) shows series-shunt SPDT switch topology. This switch is implemented to achieve not only lower IL but also higher ISO compared to series SPDT switch topology as shown in Fig. 2.6(a). When V_{c2} is biased at 1.8 V in Fig. 2.6(c), the SPDT switch, which is on-state in Port 2, can be equivalent to the circuit in Fig. 2.6(d). On-state Port 1–Port 2 and off-state Port 1–Port 3 can be seen as simple RC circuits with their cut-off frequency (3-dB frequency) obtained as

$$f_{c\_on-state} = \frac{1}{2\pi R_{on\_Mse1} C_{off\_Msh1}} \text{ and } f_{c\_off-state} = \frac{1}{2\pi R_{on\_Msh2} C_{off\_Mse2}} \text{ [Hz]} \qquad (2.10)$$

In on state, from (2.10), higher 3-dB cut-off frequency (f_c) and wider operating frequency (DC to f_c) can be obtained by lower the FOM described in Sec. 2.1.2.3.

And, the IL and ISO of the switch are derived as

$$IL = -20\log_{10}\left|\frac{2*Z_0}{2*Z_0 + \dfrac{1}{1/R_{on\_Mse1} + j\omega C_{off\_Msh1}}}\right| \text{ and}$$

$$ISO = -20\log_{10}\left|\frac{2*Z_0}{2*Z_0 + \dfrac{1}{R_{on\_Msh2} + j\omega C_{off\_Mse2}}}\right| \quad (2.11)$$

, where Z_0 is terminating impedance of ports 1, 2 and 3.

Equation (2.11) verifies that series-shunt SPDT switch can achieve lower IL and higher ISO compared to series SPDT switch assuming of the same size of the transistors (M_1=M_2=M_{se1}=M_{se2}). That is, series nMOS (M_{se1} and M_{se2}) and shunt nMOS (M_{sh1} and M_{sh2}) are employed to enhance the insertion loss and isolation of the switch, respectively.

In the series-shunt switch, similarly to series switch, increasing the width of series nMOS (M_{se1} and M_{se2}) enhances IL of the switch, but reduces isolation due to the increased parasitic capacitance. On the other hand, increasing the width of the shunt nMOS (M_{sh1} and M_{sh2}) can improve the ISO, but it can also result in signal leakage from input to ground. Therefore, a trade-off between series and shunt nMOS transistors needs to be considered, and each optimum width needs to be found for the best performance of the switch.

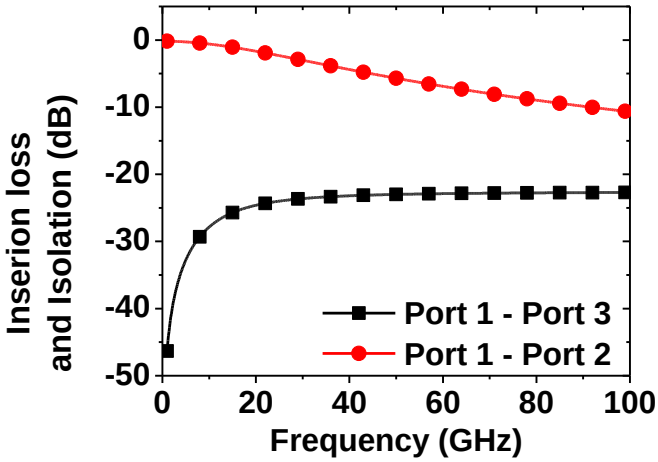


Fig. 2.7. Simulated IL and ISO for Port 1 – Port 2 and Port 1 – Port 3 of the series-shunt SPDT switch in Fig. 2.6(c).

Fig. 2.7 shows the low-pass and high-pass responses of IL and ISO in the series-shunt switch and it can be seen that the IL increases and ISO decreases, respectively, as frequency increases. Therefore, the switch is more suitable to DC–several-GHz switch.

2.1.4 Motivation for Multi-Band Band-Pass Filtering Switch

As mentioned in Sec. 2.1.3, since the IL and ISO of the typical series-shunt switch show the low-pass and high-pass responses by its structural characteristic, it is difficult to design a switch having single or multi-band band-pass filtering function.

The reasons that multi-band filtering function is needed for the switch will be followed. T/R switches and band-pass filters (BPFs) are widely employed in communication and radar systems as transmitting and receiving, and frequency selective circuits, respectively. To achieve both switching and band-pass filtering in systems, external BPF and wideband switch are commonly utilized together as depicted in Fig.

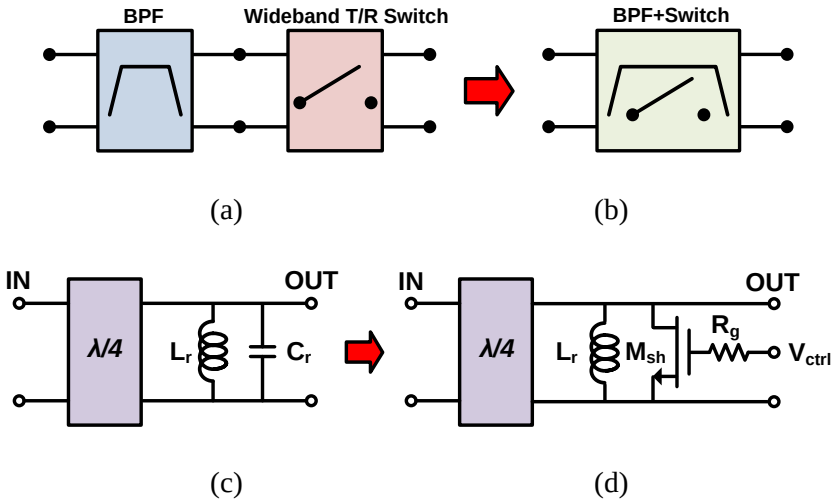


Fig. 2.8. Band-pass filtering switch design concept: (a) conventional BPF and switch structure, (b) the proposed BPF + switch structure, (c) quarter-wavelength circuit and parallel resonator, (d) quarter-wavelength circuit and parallel resonator replaced with nMOS transistor.

2.8(a). This conventional architecture, utilizing two individual components, leads to a larger circuit size which can cause cost problems. Therefore, a more effective approach is to integrate the band-pass filtering function into switches to make a dual-function (switching and filtering) simultaneously as shown in Fig. 2.8(b).

To achieve the band-pass function, Figs. 2.8(c) and (d) shows the switch design concept. The design concept consists of quarter-wavelength (λ/4) circuit and parallel resonator operating at the frequency of interest [22]. The capacitor (C_r) of the resonator is replaced with shunt transistor (M_{sh}) as shown in Fig. 2.8(d) and the width of the M_{sh} is determined by the off-capacitance, which is the same as the capacitance of C_r, considering trade-off between IL and ISO and operating bandwidth. According to the control voltage (V_{ctrl}) applied to the gate of the nMOS, their equivalent circuits can be

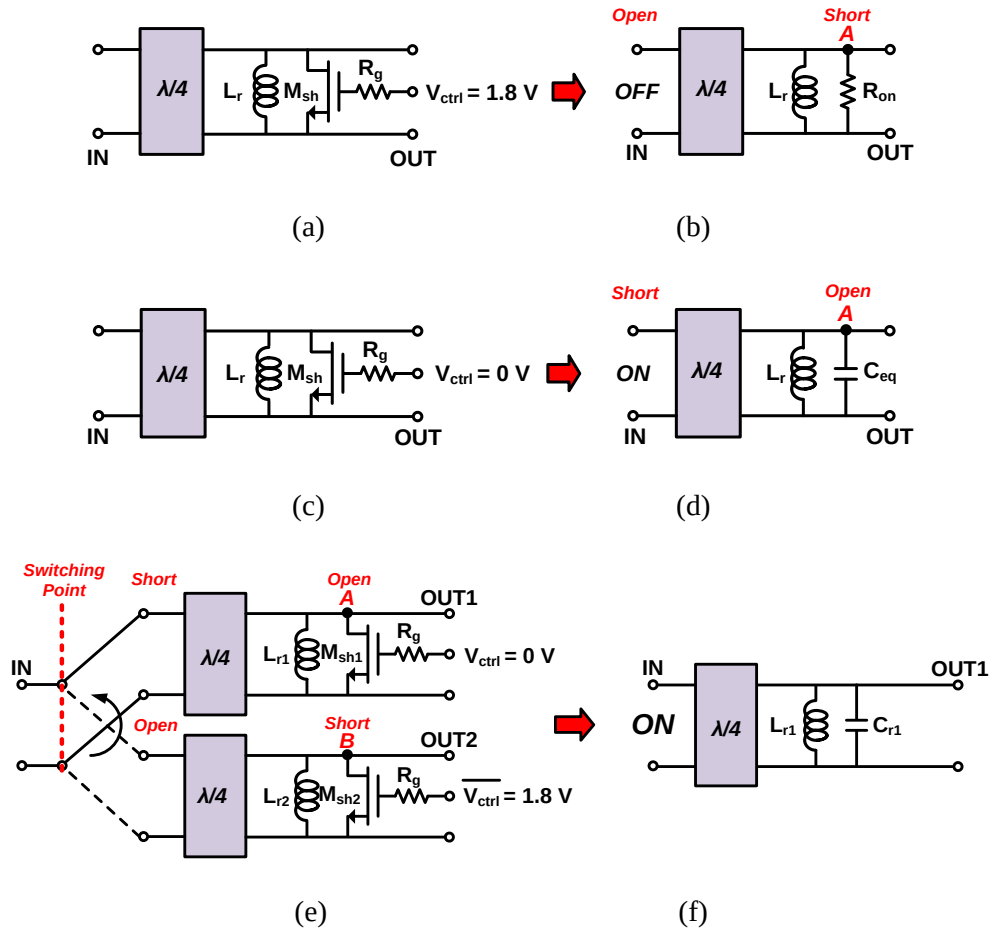


Fig. 2.9. Operations of the proposed band-pass filtering switch design concept: (a) band-pass filtering switch when V_{ctrl} =1.8 V, (b) equivalent circuit of (a), (c) band-pass filtering switch when V_{ctrl} = 0 V, (d) equivalent circuit of (c), (e) SPDT switch, and (f) equivalent circuit of (e).

shown in Figs. 2.9(b) and (d). We may assume R_{on} is negligibly small for simplicity. For ideal case, we may assume the circuit at node A is short or open to ground in Figs. 2.9(b) or (d), respectively. Through the λ/4 circuit, the impedance at the input will become open and short status, which means OFF and ON states of the switch, respectively. The circuits also show band-pass characteristic due to the parallel resonator. Thus, shunt nMOS can function not only as switching but also as band-pass circuits.

The switch design concept can be applicable to SPDT switch as shown in Fig. 2.9(e). It consists of two identical SPST switches. The SPDT switch can be equivalent to SPST switch according to control voltages (V_{ctrl}) as shown in Fig. 2.9(f). The common node of two SPST switches before two λ/4 circuits can be defined as the '**switching point**.' This switch design concept is also applicable to multi-band band-pass filtering and multi-port switch. However, the λ/4 circuit has been generally designed with transmission line (TL). The TL is not desirable for silicon RFICs due to the large size of the required TL even at millimeter-wave frequencies. Considering this issue, the switch design concept can be found in band-pass filter consisting of admittance inverters (J-inverter) and parallel resonators because J-inverter has λ/4 characteristic.

In this dissertation, switches with integrated single- and dual-band band-pass filter have been proposed. The switches have not only switching but also filtering function. And, the design of switch is based on not only the switch design concept described before but also band-pass filter theory. Therefore, theory of the band-pass filter is described first followed by description of the proposed band-pass filtering switches.

2.1.5 Band-Pass Filer Theory

The proposed switches were designed based on the second-order and third-order BPF with J-inverters and parallel resonators. Let's recall band-pass filter theory. Fig. 2.10 shows the 3rd order ladder circuit for low-pass filter (LPF) prototype. The values of

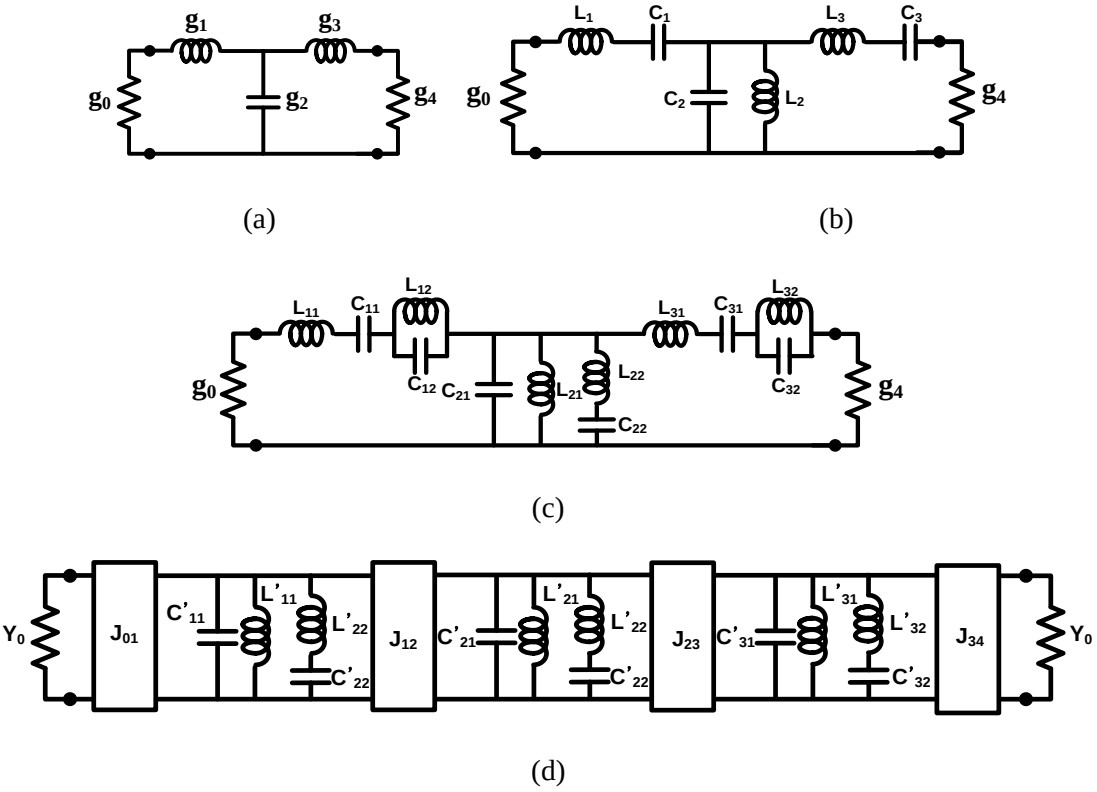


Fig. 2.10. (a) LPF prototype, (b) BPF prototype, (c) dual-band BPF prototype, and (d) dual-band BPF with J-inverter and parallel resonator.

g_0, g_1, g_2, g_3 and g_4 are determined by the LPF prototypes. And, the LPF prototype filter designs can be transformed the BPF prototype as shown in Fig. 2.10(b). Each value is calculated as

$$L_1 = \frac{g_1 Z_0}{\omega_0 \Delta},\ C_1 = \frac{\Delta}{\omega_0 g_1 Z_0},\ L_2 = \frac{\Delta Z_0}{\omega_0 g_2},\ C_2 = \frac{g_2}{\omega_0 \Delta Z_0},\ L_3 = \frac{g_3 Z_0}{\omega_0 \Delta} \text{ and } C_3 = \frac{\Delta}{\omega_0 g_3 Z_0} \quad (2.12)$$

, where ω_0 is the center frequency of the BPF and Δ is fractional bandwidth.

It shows that the transformation can transform series inductor and shunt capacitor into series and shunt LC resonators, respectively [23], [24].

A single-band bandpass filer can be transformed to a dual-band BPF prototype as shown in Fig. 2.10(c). The values are calculated as

$$L_{11}=\frac{g_1 Z_0}{\Delta\left(\omega_{c2}-\omega_{c1}\right)},\ L_{12}=\frac{g_1\left(\omega_{c2}-\omega_{c1}\right)Z_0}{\Delta\omega_0^2},\ L_{21}=\frac{\Delta\left(\omega_{c2}-\omega_{c1}\right)}{g_2\omega_0^2 Z_0},\ L_{22}=\frac{\Delta}{g_2\left(\omega_{c2}-\omega_{c1}\right)},$$

$$L_{31}=\frac{g_3 Z_0}{\Delta\left(\omega_{c2}-\omega_{c1}\right)} \text{ and } L_{32}=\frac{g_3\left(\omega_{c2}-\omega_{c1}\right)Z_0}{\Delta\omega_0^2} \tag{2.13}$$

$$L_{11}C_{11}=L_{12}C_{12}=L_{21}C_{21}=L_{22}C_{22}=L_{31}C_{31}=L_{32}C_{32}=\frac{1}{\omega_0^2} \tag{2.14}$$

, where ω_{c1} and ω_{c2} are 1st and 2nd pass-band center frequencies.

Series and parallel branches in Fig. 2.10(c) consist of both series and parallel LC resonators. Since such a circuit is difficult to be realized by using distributed transmission lines, the series branches can be replaced with parallel branches as shown in Fig. 2.10(d) using admittance inverter (J-inverter) [24].

The elements' values can be obtained as

$$L_{11}^{'}=\frac{g_0 Y_0}{J_{01}^2}C_{11},\ L_{12}^{'}=\frac{g_0 Y_0}{J_{01}^2}C_{12},\ L_{21}^{'}=\frac{J_{01}^2}{g_0 Y_0 J_{12}^2}L_{21},\ L_{22}^{'}=\frac{J_{01}^2}{g_0 Y_0 J_{12}^2}L_{22},\ L_{31}^{'}=\frac{J_{12}^2}{g_0 Y_0 J_{23}^2}L_{31},$$

$$L_{32}^{'}=\frac{J_{12}^2}{g_0 Y_0 J_{23}^2}L_{32} \tag{2.15}$$

$$L_{11}^{'}C_{11}^{'}=L_{12}^{'}C_{12}^{'}=L_{21}^{'}C_{21}^{'}=L_{22}^{'}C_{22}^{'}=L_{31}^{'}C_{31}^{'}=L_{32}^{'}C_{32}^{'}=\frac{1}{\omega_0^2} \tag{2.16}$$

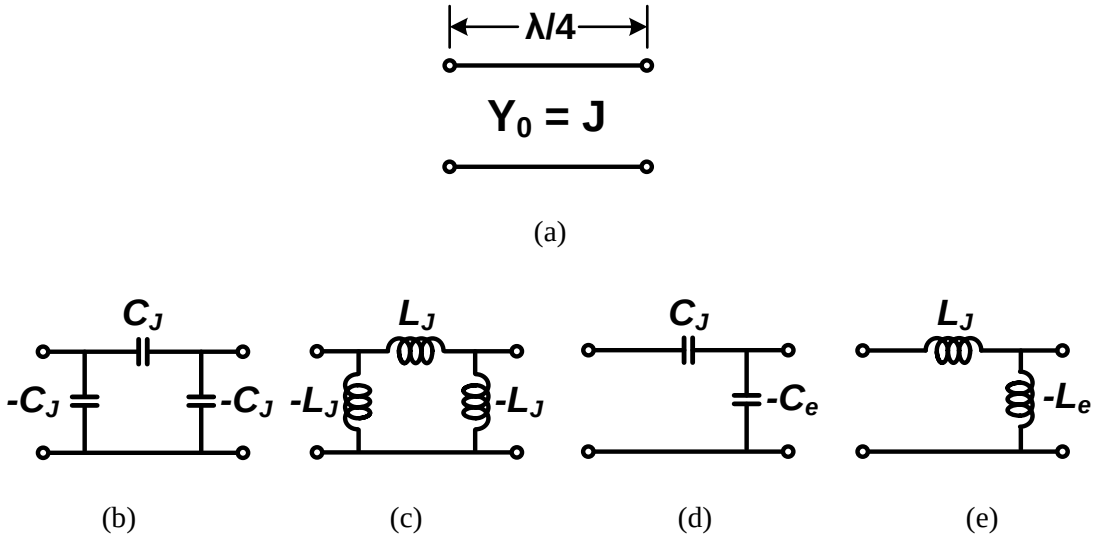


Fig. 2.11. (a) J-inverter implementation as quarter-wavelength transformer, (b), (c), (d) and (e) equivalent lumped-element circuits of J-inverter.

Admittance Inverter (J-Inverter) Implementation

Figs. 2.11(a), (b) and (c) show an implementation of the J-inverters as quarter-wavelength transformer, and some lumped-element equivalent circuits of the J-inverters, which contain series positive and shunt negative inductors and capacitors, respectively, obtained as [25]

$$J = \frac{1}{Y_0} = \omega C_J = \frac{1}{\omega L_J} \text{ and } J^2 = \frac{C_J}{L_J} \tag{2.17}$$

The negative inductor or capacitor can be absorbed into the inductor or capacitor of the resonators preceding and following the middle J-inverters in Fig. 2.10(d). The J-inverters in Figs. 2.11(b) and (c), however, are not suitable for the first and last J-inverters due to the difficulty in absorbing the negative inductors and capacitors. To overcome this problem, the inverters in Figs. 2.11(b) and (c) are transferred into

other lumped-element inverters as shown in Figs. 2.11(d) and (f), respectively, in which L_e and C_e are derived as

$$L_e = \frac{1+\left(\omega_0 L_J Y_0\right)^2}{\omega_0^2 L_J Y_0^2} \tag{2.18}$$

$$C_e = \frac{C_J}{1+\left(\frac{\omega_0 C_J}{Y_0}\right)^2} \tag{2.19}$$

, where ω_0 is the design frequency and Y_0 is the source admittance. The negative inductor L_e and capacitor C_e of these inverters can be conveniently absorbed into the adjacent inductor and capacitor of the preceding or following resonator. And, selection of the lumped-element circuits of J-inverter depends on their innate characteristics (low and high pass response) and simplicity of layout.

Dual-Band Parallel Resonator

Fig. 2.12 shows a dual-band resonator operating at two distinctive frequencies. C_n, L_n, C_r and L_r can be calculated as [26]

$$C_n = 2\Delta_s / Z_0 \omega_s \tag{2.20}$$

$$L_n = 1/\omega_s^2 C_n \tag{2.21}$$

$$C_r = \frac{1}{\left[\omega_{c1}^2 + \omega_{c2}^2 - \omega_s^2 - \frac{\left(\omega_{c1}^2 + \omega_{c2}^2\right)^2 - \left(\omega_{c2}^2 - \omega_{c1}^2\right)^2}{4\omega_s^2}\right] L_n} \tag{2.22}$$

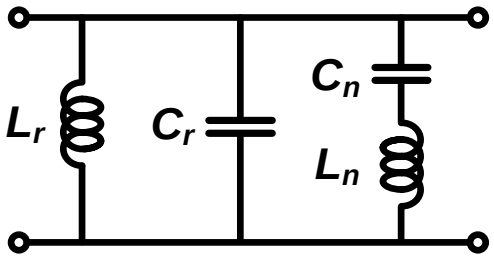


Fig. 2.12. Conventional dual-band parallel resonator.

$$L_r = \frac{1}{\left[\omega_{c1}^2 + \omega_{c2}^2 - \omega_s^2 - \frac{1}{L_n C_r}\right] C_r} \tag{2.23}$$

where Z_0 is the terminating impedance, ω_s is the stop-band center frequency, Δ_s is the stop-band fractional bandwidth, and ω_{c1} and ω_{c2} are the 1st and 2nd pass-band center frequencies, respectively.

2.2 High-Isolation Multi-Port Millimetre-Wave CMOS Dual-Band T/R Switch with Integrated Band-Pass Filtering Function (Design 1)

In this section, we report the development of a new 0.18-μm CMOS dual-band band-pass filtering transmit/receive (T/R) switch operating simultaneously in two different frequency bands of 35.5–43.7 GHz in Ka-band and 56.5–63 GHz in V-band centered about 40 and 60 GHz, respectively. The switch has multiple ports with concurrent dual-band characteristics at each port and high isolation between them, enabling its versatile implementation in multi-band RF systems. These frequencies are used in a multi-band system for possible long-range (at Ka-band) and short-range (at V-band) operations at the same time, considering the relatively low and high atmospheric attenuations at these respective frequencies, hence extending the application range for multi-band systems at millimetre-wave frequencies.

2.2.1 40/60-GHz Dual-Band Band-Pass Filter

The architecture, design and operation of the 40/60-GHz dual-band band-pass filtering T/R switch are based on those of 40/60-GHz dual-band band-pass filter and single-pole double-throw (SPDT) switch. Therefore, the filter and SPDT switch are described first followed by the T/R switch.

The design of the 40/60-GHz dual-band band-pass filtering SPDT switch is based on a dual-band band-pass filter using admittance (*J*) inverters and dual-band resonators. Fig. 2.13 shows the evolution of the dual-band resonator, starting from a conventional dual-band resonator in Fig. 2.13(a) to the modified dual-band resonator in Fig. 2.13(c). The

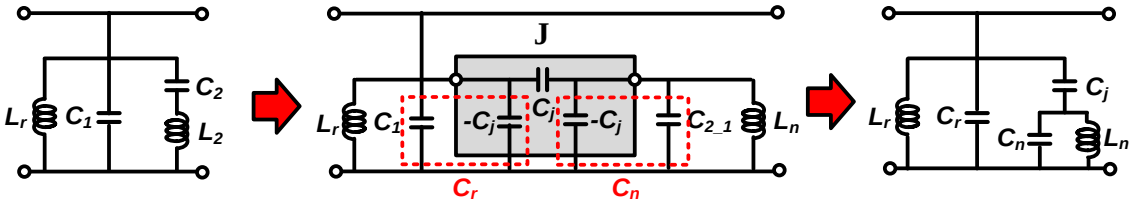


Fig. 2.13. Evolution of dual-band resonator: (a) conventional dual-band resonator, (b) modified dual-band resonator implementing J-inverter and (c) modified dual-band resonator.

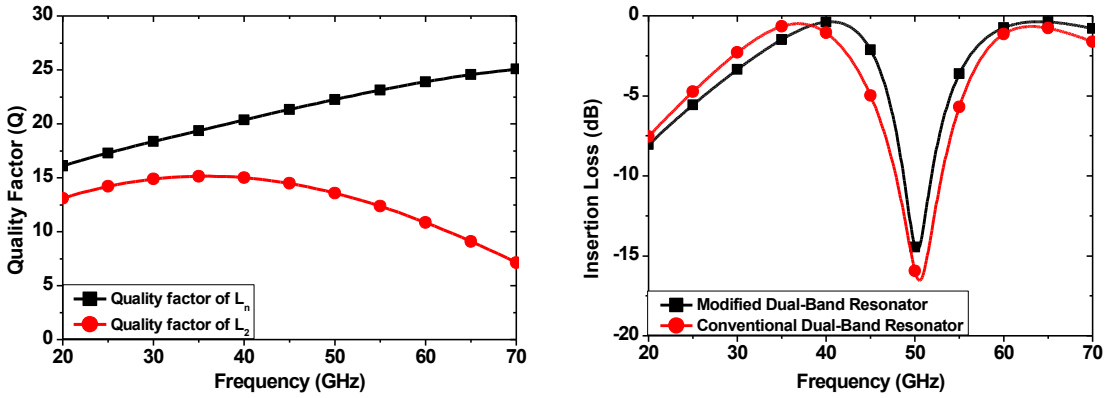
conventional dual-band resonator is designed with C_2 = 26 *f*F, L_2 = 450 *p*H, C_1 = 250 *f*F and L_r = 45 *p*H calculated from (2.20)–(2.23).

The conventional dual-band resonator is transformed into another resonator in Fig. 2.13(b) using a J-inverter consisting of a pi network of capacitors as shown in Fig. 2.11(b), Sec. 2.1.5.1. This circuit transformation is needed to obtain L_n of lower inductance and higher quality factor (Q) than L_2. Using such a transformed resonator with smaller L_n helps ease the layout and reduce the size. Finally, the modified dual-band resonator in Fig. 2.13(c) can be obtained as shown. The series L_2-C_2 in Fig. 2.13(a) is equivalent to the combined J-inverter and parallel $C_{2\text{-}1}$-L_n in Fig. 2.13(b), leading to [24]

$$C_n = C_{2\_1} - C_j = L_2 J^2 - \frac{J}{\omega_0} \tag{2.24}$$

$$C_r = C_1 - C_j = C_1 - \frac{J}{\omega_0} \tag{2.25}$$

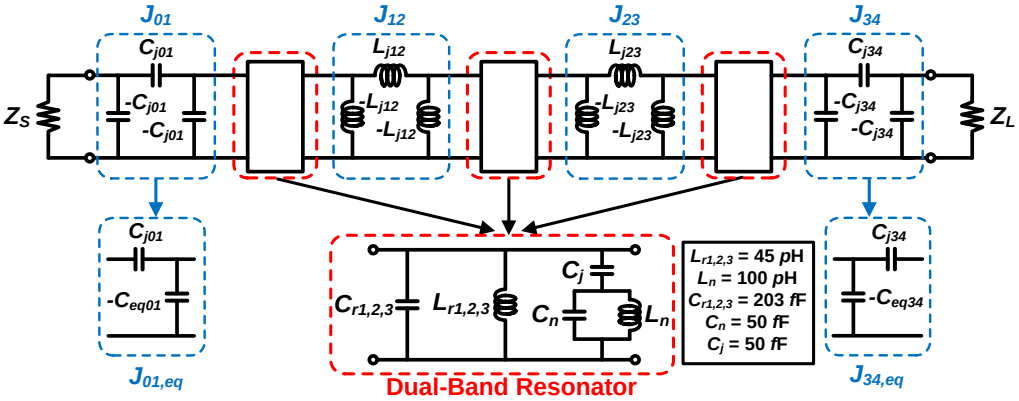
$$L_n = \frac{C_2}{J^2} \tag{2.26}$$



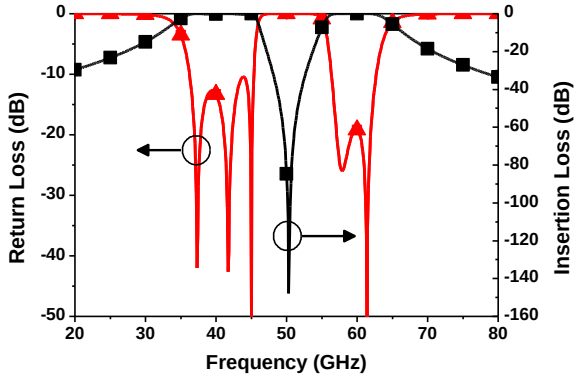
(a) (b)

Fig. 2.14. Comparison of simulated quality factor (Q) of inductors L_n and L_2, and insertion losses of modified and conventional dual-band resonators: (a) quality factors (Q) of inductors L_n and L_2 and (b) insertion losses of modified and conventional dual-band resonators.

where $J = 1/Z_0$ and ω_0 is the center frequency of the two pass-band frequencies. From (2.24)–(2.26), C_n, C_r, L_n and C_j of the modified dual-band resonator can be calculated. It is noted that L_n of the modified dual-band resonator is smaller than L_2 of the conventional one, facilitating its design for higher Q, which leads to possibly lower insertion loss for the dual-band resonator, as shown in Figs. 2.14(a) and (b), respectively. Figs. 2.15(a) and (b) show the schematic of the dual-band band-pass filter employing the dual-band resonator shown in Fig. 2.13(c) and its simulated return loss and insertion loss. The dual-band band-pass filter is realized by the third-order Chebychev approximation with 0.01-dB ripple, which is chosen for optimal results considering trade-off between insertion loss, out-of-band rejection ratio and isolation of the switch, and 20% fractional bandwidth at both center frequencies of 40 and 60 GHz. The corresponding elements values are listed in Fig. 2.15(a), where the source (Z_S) and load (Z_L) impedances are 50 Ω.



(a)



(b)

Fig. 2.15. (a) Schematic of the 3rd order dual-band band-pass filter using dual-band resonator and J-inverter and (b) its return loss and insertion loss.

The identical J-inverters (J_{01}=J_{34}) and (J_{12}=J_{23}) are implemented using the pi networks of capacitors and inductors as shown in Fig. 2.11(b) and (c), respectively. To facilitate the implementation of J_{01} and J_{34}, these inverters are replaced by equivalent L-type networks of capacitors, which are derived from the pi-type network of capacitors in Fig. 2.11(b), as shown in Fig. 2.15(a). C_{eq01} and C_{eq34} are combined with C_{r1} and C_{r3}, respectively, and the total capacitances (C_{T1} and C_{T3}) are obtained by

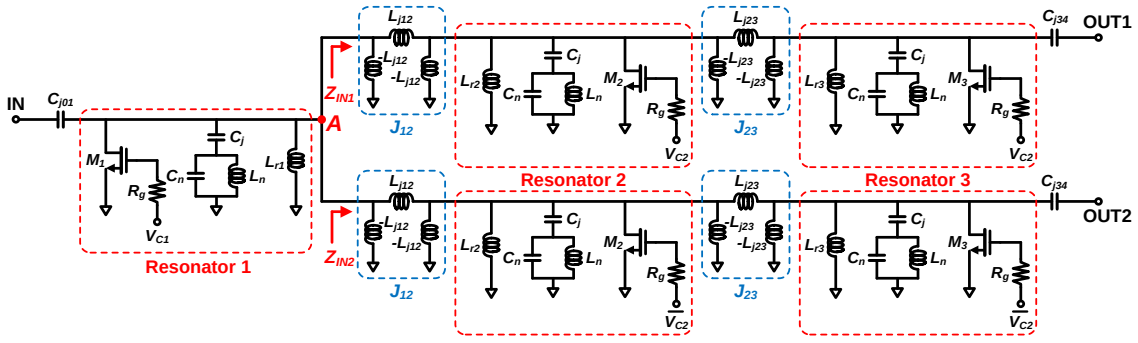


Fig. 2.16. Schematic of the 40/60-GHz dual-band band-pass filtering SPDT switch.

$$C_{eq01} = C_{eq34} = \frac{C_{j01}}{1+\left(\omega_0 C_{j01}/Y_0\right)^2} = \frac{C_{j34}}{1+\left(\omega_0 C_{j34}/Y_0\right)^2} \tag{2.27}$$

$$C_{T1} = C_{T3} = -C_{eq01} + C_{r1} = -C_{eq34} + C_{r3} \tag{2.28}$$

where Y_0 is the reference admittance. Due to the high-pass (J_{01} and J_{34}) and low-pass (J_{12} and J_{23}) responses of the employed J-inverters, the filter can achieve similar degree of out-of-band rejection ratio at both lower (40 GHz) and upper (60 GHz) frequency bands.

2.2.2 40/60-GHz Dual-Band Band-Pass Filtering SPDT Switch

Fig. 2.16 shows the SPDT switch with integrated dual-band band-pass filtering function, in which the signal path from the port IN to the port OUT1 (or OUT2) is designed based on the designed dual-band band-pass filter described in Sec. 2.2.1. Shunt nMOS transistors (M_1, M_2, M_3) in Fig. 2.16 not only provide the switching function, but also replace the capacitors (C_{T1}, C_{r2}, C_{T3} obtained in Sec. 2.2.1) constituting the band-pass filter. Body-floating technique with deep *n*-well is employed for all the nMOS transistors to decrease the parasitic capacitance of the transistors [19]. Point A represents

the switching point at which the SPDT switch turns ON for one output port (e.g., from IN to OUT1) and OFF for another port (e.g., from IN to OUT2). The detailed switching operation is explained as follows.

The switching function is executed through J_{12}, J_{23}, M_2 and M_3. For instance, when M_1 is biased at V_{C1} = 0 V (off-state) and M_2 and M_3 on the OUT1 and OUT2 paths are biased at V_{C2} = 0 V (off-state) and $\overline{V_{C2}}$ = 1.8 V (on-state), the OUT1 port is approximately matched to the IN port via the switching point A, while A appears as an approximate open circuit looking toward the OUT2 port through the J-inverters and on-state shunt transistors. Note that the J-inverter behaves as a quarter-wavelength transmission line and hence can transform a low impedance caused by an on-state shunt transistor to a high impedance and a high impedance by an off-state shunt transistor to a low impedance at A in Fig. 2.16. When V_{C2} = 0 V in Fig. 2.16, the path from IN to OUT1 is in on-state with Z_{IN1} at A to be 41 and 56 Ω simulated at 40 and 60 GHz, respectively. On the other hand, OUT2 becomes isolated from OUT1, and the simulated impedances (Z_{IN2}) looking into OUT2 at A are 236 and 538 Ω at 40 and 60 GHz, respectively. Therefore, the SPDT switch in Fig. 2.16 is equivalent to a SPST switch (upper path), which is equivalent to the dual-band band-pass filter with off-state shunt transistor as shown in Fig. 2.15(a), while the lower path at the switching point A is in off-state.

This SPDT switch architecture facilitates extension for dual-band band-pass filtering single-pole multi-throw switches by adding extra output paths, while maintaining desired filtering and switching functions with simplicity and compactness.

The isolation between the output ports primarily depends on the impedance looking into the OFF-output port at the switching point, which is proportional to the numbers of J-inverters and shunt transistors in the OFF output path. The proposed SPDT switch having one common resonator (Resonator 1) for both OUT1 and OUT2 paths with switching right before J_{12} hence gives higher isolation than that using two common resonators (Resonator 1 and 2) with switching before J_{23}. This design arrangement is useful as it enables high isolation with less number of sections. It is noted that using less resonators would improve the insertion loss, yet decreasing the isolation and possibly degrading the switch's performance. For instance, removing the resonators right before ANT1 and ANT2 results in not only a reduction of the isolation, but also a deterioration of the 3rd dual-band band-pass filter performance and out-of-band rejection ratio.

2.2.3 40/60-GHz Dual-Band Band-Pass Filtering T/R Switch

Fig. 2.17 shows the schematic of the 40/60-GHz dual-band band-pass filtering T/R switch, which is realized using a combination of three SPDT switches described in Section 2.2.2: one between Ports 1, 2 and 3; one between Ports 3, 1 and 5; and another between Ports 2, 1 and 4. It consists of five ports that are working for both 40- and 60-GHz signals simultaneously: Port 1 (TX) is the transmitting port; Port 2 (ANT1) and Port 3 (ANT2) are the antenna ports; and Port 4 (RX1) and Port 5 (RX2) are the receiving ports. The equivalent shunt inductances (L_{eq1}, L_{eq2}, L_2) can be obtained by

$$L_{eq1} = \left(\frac{1}{L_{r1}} + \frac{1}{-L_{j12}} + \frac{1}{-L_{j12}} \right)^{-1} = \left(\frac{1}{L_{r3}} + \frac{1}{-L_{j23}} + \frac{1}{-L_{j23}} \right)^{-1} \tag{2.29}$$

$$L_{eq2} = \left(\frac{1}{L_{r1}} + \frac{1}{-L_{j12}} \right)^{-1} \tag{2.30}$$

$$L_2 == \left(\frac{1}{L_{r2}} + \frac{1}{-L_{j12}} + \frac{1}{-L_{j23}} \right)^{-1} \tag{2.31}$$

where L_{r1}, L_{r2} and L_{r3} are the inductors of the 1st, 2nd and 3rd dual-band resonators, respectively, and $-L_{j12}$ and $-L_{j23}$ are the negative inductors of J_{12} and J_{23}, respectively. Part of L_{eq1} and L_{eq2} is used for J_{12} and J_{23} along with the series elements L_{j12} and L_{j23} and part is used for the 1st and 3rd dual-band resonators, respectively. Also, part of the capacitor representing the transistor right after C_{j01} and right before C_{j34} is used for J_{01} and J_{34}, respectively. All the element values for the final design are listed in Table 2.1.

The T/R switch operates in two different operation modes, transmission and reception, each can be inferred from that of the constituent SPDT switches. The receiving operations between ANT1–RX1 and ANT2–RX2 occur simultaneously and happen when M_R, M_{R1}, M_{A1} and M_{A2} of the receiving paths between ANT1–RX1 and ANT2–RX2 are turned off and M_T, M_{T1} and M_{T2} of the transmitting paths between TX–ANT1 and TX–ANT2 are turned on. The 40/60-GHz signals coming from ANT1 and ANT2 are directed into RX1 and RX2 via the switching points B and C, respectively. The transmission between TX–ANT1 (or between TX–ANT2) is obtained when M_T, M_{T1} and M_{A1} between TX–ANT1 (or M_T, M_{T2} and M_{A2} between TX–ANT2) are turned off, while M_{T2}, M_{A2} between TX–ANT2 (or M_{T1}, M_{A1} between TX–ANT1), M_R and M_{R1} are turned on. The 40/60-GHz signals from TX are directed into ANT1 or ANT2 via the switching points A, B or A, C, respectively.

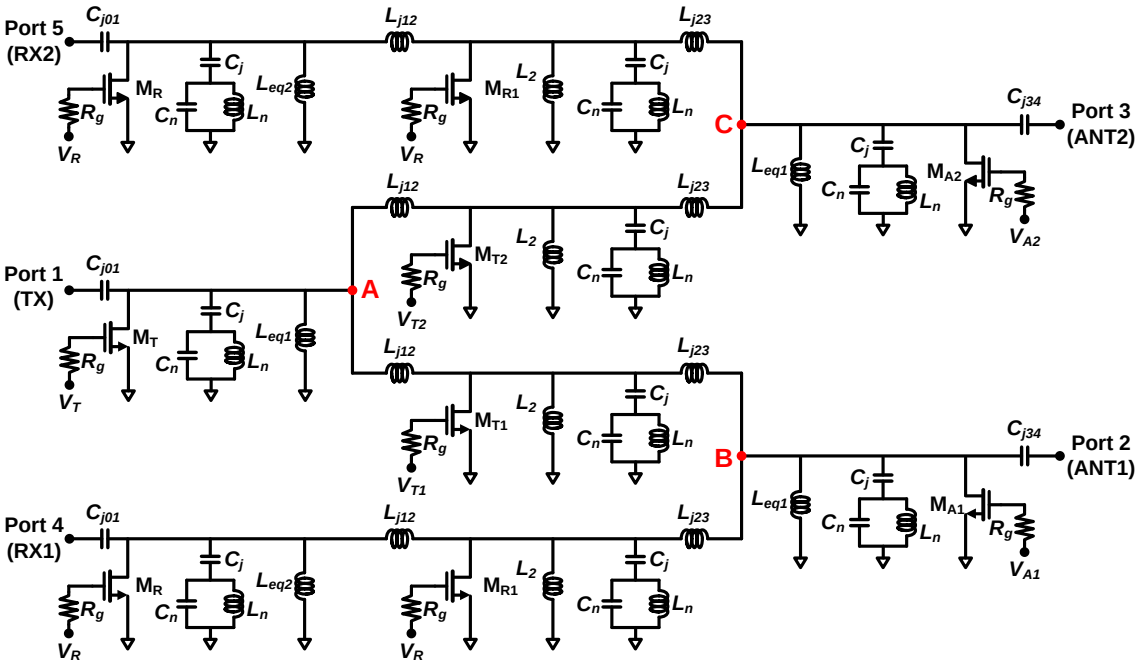


Fig. 2.17. Schematic of the 40/60-GHz dual-band band-pass filtering T/R switch.

Table 2.1
Dual-Band Band-Pass Filtering T/R Switch's Parameters

C_j	50 *f*F	C_n	50 *f*F
C_{j01} , C_{j34}	540 *f*F	L_2	60 *p*H
L_n	100 *p*H	L_{eq1}	180 *p*H
L_{eq2}	90 *p*H	L_{j12} , L_{j23}	176 *p*H
R_g	1 kΩ	V_T, V_R, V_{A1}, V_{A2}	0, 1.8 V
M_T, M_{A1}, M_{A2}, M_R	0.18 μm / 208 μm	M_{T1}, M_{T2}, M_{R1}	0.18 μm / 312 μm
C_{off} of M_T, M_{A1}, M_{A2}, M_R	172 *f*F	C_{off} of M_{T1}, M_{T2}, M_{R1}	253 *f*F

The relations of the isolations between different ports can be deduced from the

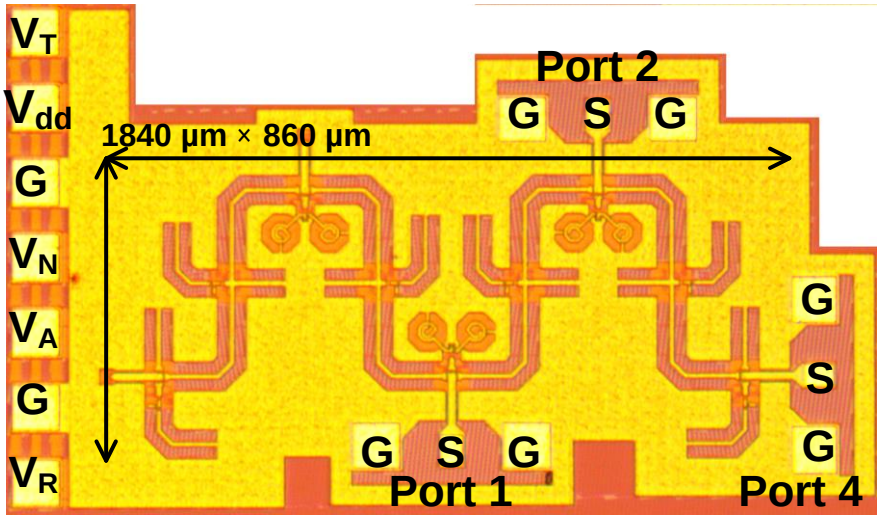


Fig. 2.18. A microphotograph of the 40/60-GHz dual-band band-pass filtering T/R switch.

symmetry of the T/R switch as shown in Fig. 2.17. For instance, the isolations from TX–RX1 (TX–RX2) under transmission from TX–ANT1 (TX–ANT2) and during receptions from ANT1–RX1 and ANT2–RX2 should be similar because of the same numbers of the J-inverters and shunt transistors in the off-state path. Similarly, it is expected that the isolation between ANT1–ANT2 is comparable during transmission from TX–ANT1 or TX–ANT2 and is equal to that of TX–RX1 or TX–RX2.

The 40/60-GHz dual-band band-pass filtering T/R switch was designed and fabricated on a TowerJazz 0.18-μm SiGe BiCMOS process [27]. Fig. 2.18 shows a microphotograph of the fabricated T/R switch that occupies 1840 μm × 860 μm excluding all the testing pads. To facilitate the measurement using a 3-port vector network analyzer, making use of the switch's symmetry, RF test pads are placed only on a half section of the switch as shown in Fig. 2.18 (Port 1, Port 2, Port 4) with Port 3 and

5 terminated with 50-Ω. The fabricated T/R switch allows the transmitting and receiving operation at 40/60 GHz to be measured between Port 1, Port 2 and Port 4, and the results can be deduced for the operations between other ports.

2.2.4 Simulation and Measurement Results

Fig. 2.19 shows the measured and simulated insertion loss, return loss and isolation of the T/R switch in the transmitting and receiving modes. The ports corresponding to the measurement parameters are denoted in Fig. 2.18. Figs. 2.19(a) and (b) show the return loss/insertion loss and isolation results for the reception operation, respectively. The insertion losses (S_{42}) are 8.9 and 12.5 dB at 40 and 60 GHz, respectively. The measured 3-dB bandwidths based on the insertion loss in each passband are 35.1–43.7 GHz and 56.5–63 GHz. The measured input (S_{22}), output (S_{44}) return losses are 12, 14 dB at 40 GHz and 9.4, 7.8 dB at 60 GHz, respectively. The drift of the resonance frequency around 40 GHz was due to possible capacitance and inductance variation from the fabrication. The measured isolations (S_{41}) are 56 and 51 dB at 40 and 60 GHz, respectively. The measured stop-band rejection ratio from the lowest insertion loss at 40 GHz to the highest rejection at 52 GHz is 30 dB. Figs. 2.19(c) and (d) show the return loss/insertion loss and isolation results for the transmission operation, respectively. The insertion losses (S_{21}) are 10 and 12.7 dB at 40 and 60 GHz, respectively. The measured 3-dB bandwidths based on the insertion loss in each passband are 35.5–44.2 GHz and 56.4–63.7 GHz. The 3-dB bandwidths in the transmitting operation are similar to those in the receiving operation. The measured

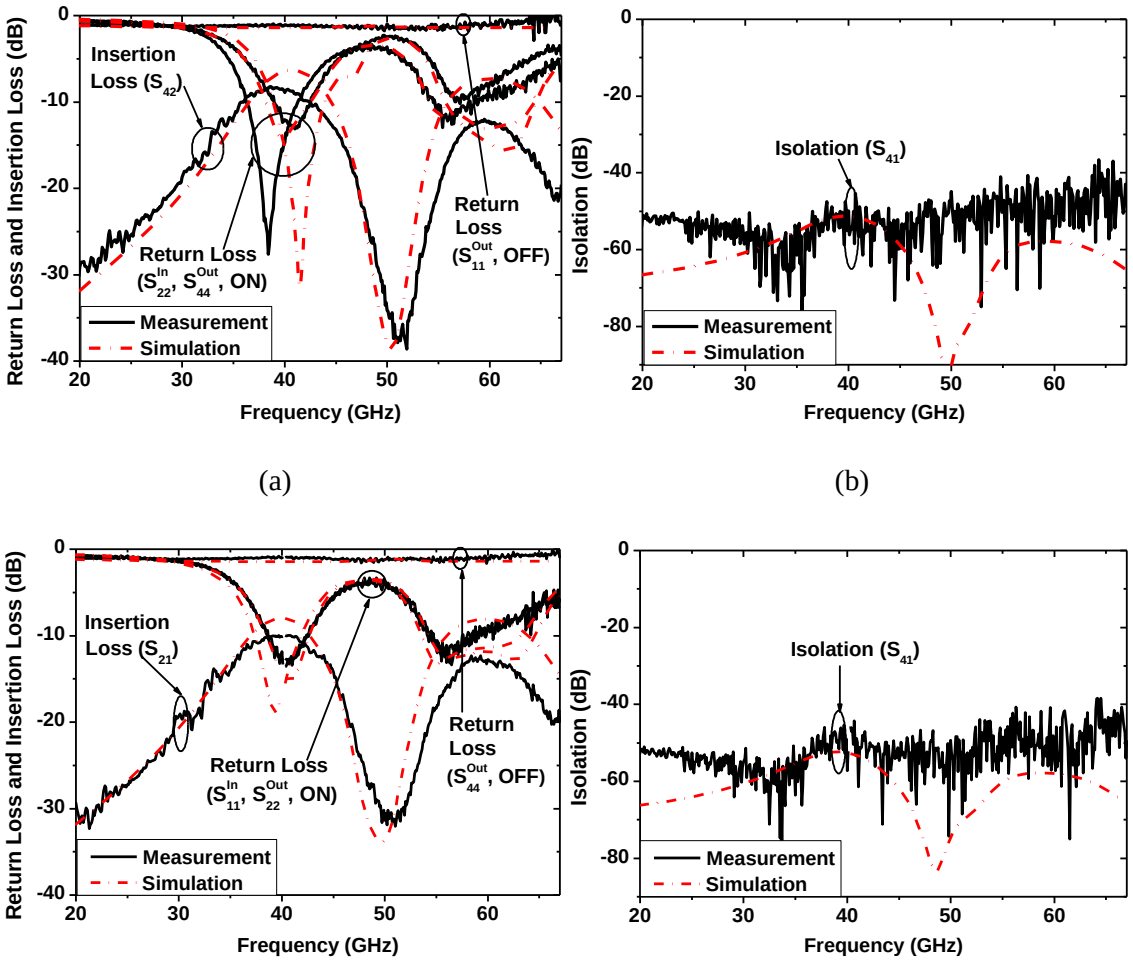
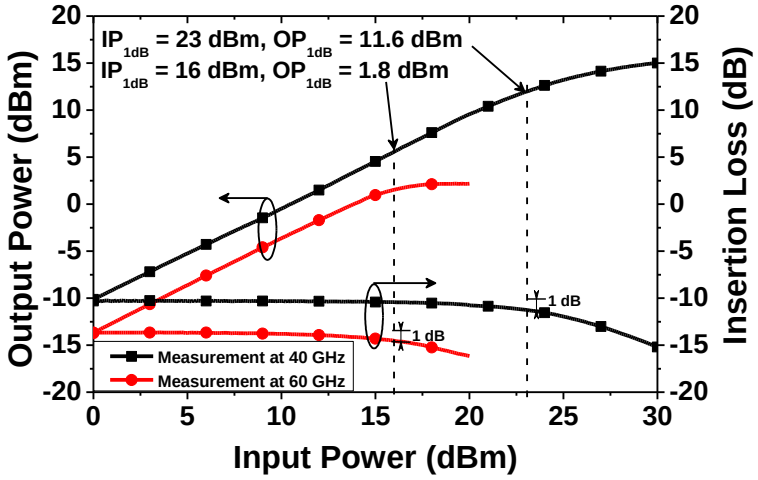


Fig. 2.19. Measured and simulated results of the 40/60-GHz dual-band band-pass filtering T/R switch: (a) return loss and insertion loss, and (b) isolation for receiving operation mode, (c) return loss and insertion loss, and (d) isolation for transmitting operation mode.

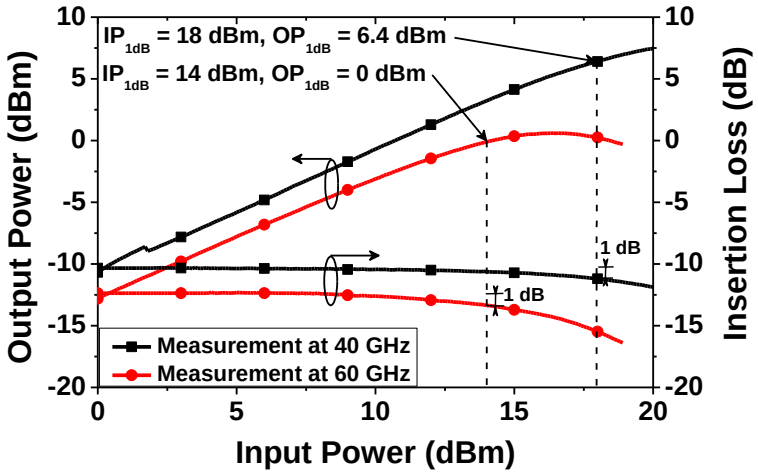
input (S_{11}), output (S_{22}) return losses are 12.7, 12 dB at 40 GHz and 9.4, 8.8 dB at 60 GHz, respectively. The measured isolations (S_{41}) are 57 and 51 dB at 40 and 60 GHz, respectively. The measured stop-band rejection ratio between 40 and 51 GHz is 22 dB. It is verified that the T/R switch has similar TX–RX1 isolation (S_{41}) in the transmission and reception modes, as discussed earlier. The isolation between ANT1–ANT2 should

be similar to the measured TX–RX1 isolation. Moreover, the performance at Port 3 (ANT2) and Port 5 (RX2) in Fig. 2.17 can be estimated accurately from these measured results due to the symmetry of the T/R switch.

Figs. 2.20(a) and (b) show the measured output power and insertion loss versus input power of the switch for three cases in transmitting operation: a 40-GHz input signal, a 60-GHz input signal, and concurrent 40- and 60-GHz input signals. For the 40-GHz input signal, the measured 1-dB compression points (IP_{1dB} and OP_{1dB}) are 23 and 11.6 dBm, respectively, while for the 60-GHz input signal, they are 16.5 and 2.8 dBm, respectively. For the concurrent power measurement, two 40- and 60-GHz signals with identical input power level are simultaneously injected from the vector network analyzer into the input of the switch, and the output powers at 40 and 60 GHz are measured accordingly. With the concurrent 40/60-GHz signals, the IP_{1dB} and OP_{1dB} are 18 and 6.4 dBm at 40 GHz and 14 and 0 dBm at 60 GHz, respectively. For the concurrent 40 and 60-GHz power measurement, the measured IP_{1dB} at 60 GHz is lower than that at 40 GHz because of the higher nonlinear parasitic capacitance of the off-state shunt transistor at 60 GHz. Also, compared to the non-concurrent 40- and 60-GHz single input signals, the P_{1dB} decreases due to 40 and 60-GHz signals' intermodulation when they are injected concurrently.



(a)



(b)

Fig. 2.20. Measured P_{1dB} of the 40/60-GHz dual-band band-pass filtering T/R switch: (a) individual 40- or 60-GHz input signal (b) concurrent 40 and 60 GHz input signals.

2.3 A Millimeter-Wave CMOS Dual-Bandpass T/R Switch with Dual-Band LC Network (Design 2)

This section presents a new CMOS dual-bandpass T/R switch operating simultaneously in two different frequency bands of 17.2–27.3 and 52.5–66.5 GHz, which cover the unlicensed bands around 24 and 60 GHz, realized in a 0.18-μm SiGe BiCMOS process [27]. The T/R switch consists of dual-band LC networks and dual-band resonators with shunt nMOS transistors, and it shows not only switching but also band-pass filtering functions. Moreover, the switch has multiple ports with concurrent dual-band characteristics at each port and can be employed in multi-band RF systems.

2.3.1 Dual-Band Quarter-Wavelength LC Circuit

Fig. 2.21(a) shows a transmission line (Z_b and θ_b) loaded with shunt open stubs (Z_a and θ_a) at both ends, which behaves equivalently as a quarter-wavelength TL at two different desired frequencies (f_1 and f_2) [28], where Z_a, Z_b, θ_a and θ_b represent the characteristic impedance and the electrical lengths of the shunt and series sections.

By setting that the matrix of the three sections in Fig. 2.21(a) is equal to that of conventional quarter-wavelength (λ/4) transmission line (TL) at two desired frequencies (f_1 and f_2), the matrix can be expressed by cascading the sections as

$$\begin{bmatrix} 1 & 0 \\ \dfrac{j\tan\theta_{a\_f1,f2}}{Z_a} & 1 \end{bmatrix} \cdot \begin{bmatrix} \cos\theta_{b\_f1,f2} & jZ_b\sin\theta_{b\_f1,f2} \\ \dfrac{j\tan\theta_{b\_f1,f2}}{Z_b} & \cos\theta_{b\_f1,f2} \end{bmatrix} \cdot \begin{bmatrix} 1 & 0 \\ \dfrac{j\tan\theta_{a\_f1,f2}}{Z_a} & 1 \end{bmatrix} = \begin{bmatrix} 0 & \pm jZ_c \\ \pm j\dfrac{1}{Z_c} & 0 \end{bmatrix} \quad (2.32)$$

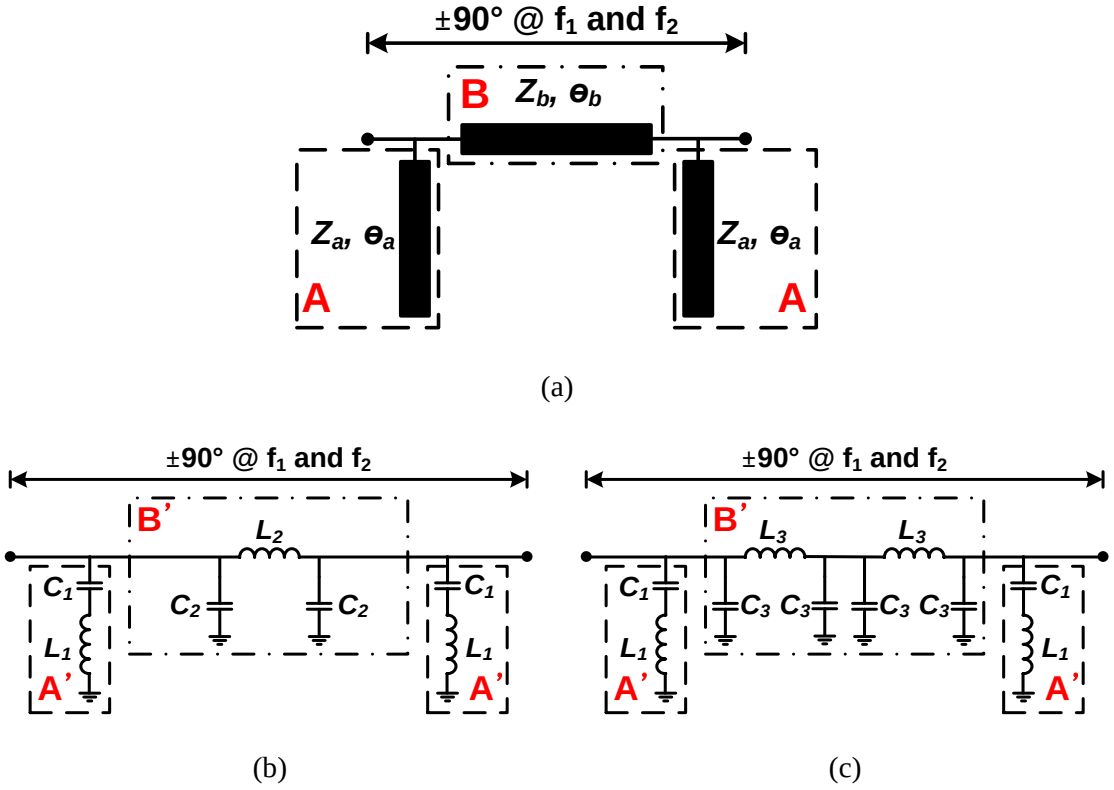


Fig. 2.21. (a) Quarter-wavelength transmission line at two different frequencies (Model 1), (b) and (c) proposed equivalent dual-band LC networks (Model 2 and 3).

, where Z_c is characteristic impedance of a conventional λ/4 TL.

From (2.32), relation of Z_a, Z_b, θ_a and θ_b can be obtained as

$$Z_{b\_f1} = \frac{\pm Z_c}{\sin\theta_{b\_f1}} \text{ and } Z_{b\_f2} = \frac{\pm Z_c}{\sin\theta_{b\_f2}} \tag{2.33}$$

$$Z_{a\_f1} = Z_{b\_f1}\tan\theta_{a\_f1}\tan\theta_{b\_f1} \text{ and } Z_{a\_f2} = Z_{b\_f2}\tan\theta_{a\_f2}\tan\theta_{b\_f2} \tag{2.34}$$

, where the subscripts f_1 and f_2 denote the corresponding frequencies.

Solving (2.33) yields a relation of θ_{b_f1} and θ_{b_f2} as

$$\theta_{b\_f2} = n\pi - \theta_{b\_f1} \tag{2.35}$$

, where n = 1, 2, 3, …, and with the relation of θ_{b_f1}, θ_{b_f2}, f_1 and f_2 obtained as

$$\frac{\theta_{b\_f1}}{\theta_{b\_f2}} = \frac{f_1}{f_2} \tag{2.36}$$

It can be deduced that

$$\theta_{b\_f1} = \frac{n\pi f_1}{f_1 + f_2} \text{ and } \theta_{b\_f2} = \frac{n\pi f_2}{f_1 + f_2} \tag{2.37}$$

And, when n = 1 for the shortest length,

$$\theta_{b\_f1} = \frac{\pi f_1}{f_1 + f_2} \text{ and } \theta_{b\_f2} = \frac{\pi f_2}{f_1 + f_2} \tag{2.38}$$

And, the solution of (2.34) in order to obtain θ_{a_f1} and θ_{a_f2} is

$$n\pi \pm \theta_{a\_f1} = \theta_{a\_f2} \tag{2.39}$$

, where n = 1, 2, 3, …, and with the relation of θ_{a_f1}, θ_{a_f2}, f_1 and f_2 obtained as

$$\frac{\theta_{a\_f1}}{\theta_{a\_f2}} = \frac{f_1}{f_2} \tag{2.40}$$

It can also be deduced that

$$\theta_{a\_f1} = \frac{n\pi f_1}{f_1 + f_2} \text{ and } \theta_{a\_f2} = \frac{n\pi f_2}{f_1 + f_2} \tag{2.41}$$

And, when n = 1 for the shortest length,

$$\theta_{a\_f1} = \frac{\pi f_1}{f_1 + f_2} \text{ and } \theta_{a\_f2} = \frac{\pi f_2}{f_1 + f_2} \tag{2.42}$$

From (2.38), (2.42) and desirable f_1 and f_2, θ_{a_f1}, θ_{a_f2}, θ_{b_f1}, θ_{b_f2}, Z_a and Z_b

can be obtained.

This TL circuit is not suitable for silicon RFICs due to the large size of the required TLs even at millimeter-wave frequencies. This issue, however, can be overcome by implementing the equivalent lumped-element network as shown in Figs. 2.21(b) and (c), where the series L-C (A') and the 1st and 2nd order LC pi networks (B') replace the open stub (A) and series TL section (B), respectively.

The required inductance (L_1) and capacitance (C_1) can be obtained by equating its input impedance to the input impedance of the open stub as

$$Z_{in}^{sh} = Z_a \frac{Z_L + jZ_a \tan\theta_a}{Z_a + jZ_L \tan\theta_a} = \frac{Z_a}{j\tan\theta_a} \tag{2.43}$$

$$Z_{in}^{1} = j\omega L_1 + \frac{1}{j\omega C_1} = \frac{1-\omega^2 L_1 C_1}{j\omega C_1} \tag{2.44}$$

$$\frac{1-\omega^2 L_1 C_1}{j\omega C_1} = \frac{Z_{a\_f1}}{j\tan\theta_{a\_f1}} \tag{2.45}$$

from which

$$C_1 = \frac{\tan\theta_{a\_f1}}{\omega Z_{a\_f1}}\left[1-\left(\frac{\omega}{\omega_0}\right)^2\right] \tag{2.46}$$

$$L_1 = \frac{1}{C_1\omega_0^2} = \frac{1}{\tan\theta_{a\_f1}} \cdot \frac{\omega Z_a}{\omega_0^2 - \omega^2} \tag{2.47}$$

where ω_0 is the center frequency between the dual-band frequencies (f_1 and f_2).

For the 1st order LC pi network in Fig. 2.21(b), each half of it should behave equivalently to a half of the TL in Fig. 2.21(a). Equating the corresponding ABCD-parameters as

$$\begin{bmatrix} \cos\theta_{b\_f1} & jZ_b \sin\theta_{b\_f1} \\ \dfrac{j\tan\theta_{b\_f1}}{Z_b} & \cos\theta_{b\_f1} \end{bmatrix} = \begin{bmatrix} 1+\dfrac{L_2}{C_2} & j\omega L_2 \\ j\omega C_2\left(2-\omega^2 L_2 C_2\right) & 1+\dfrac{L_2}{C_2} \end{bmatrix} \tag{2.48}$$

gives

$$C_2 = \frac{1-\cos\theta_{b\_f1}}{\omega Z_b \sin\theta_{b\_f1}} \tag{2.49}$$

$$L_2 = \frac{Z_b \sin\theta_{b\_f1}}{\omega} \tag{2.50}$$

For the 2nd order LC pi network in Fig. 2.21(c), each half of it should behave equivalently to a half of the TL in Fig. 2.21(a). Equating the corresponding ABCD-parameters as

$$\begin{bmatrix} \cos\dfrac{\theta_{b\_f1}}{2} & jZ_b \sin\dfrac{\theta_{b\_f1}}{2} \\ \dfrac{j\tan\dfrac{\theta_{b\_f1}}{2}}{Z_b} & \cos\dfrac{\theta_{b\_f1}}{2} \end{bmatrix} = \begin{bmatrix} 1+\dfrac{L_3}{C_3} & j\omega L_3 \\ j\omega C_3\left(2-\omega^2 L_3 C_3\right) & 1+\dfrac{L_3}{C_3} \end{bmatrix} \tag{2.51}$$

gives

$$C_3 = \frac{1-\cos\dfrac{\theta_{b\_f1}}{2}}{\omega Z_b \sin\dfrac{\theta_{b\_f1}}{2}} \tag{2.52}$$

$$L_3 = \frac{Z_b \sin\dfrac{\theta_{b\_f1}}{2}}{\omega} \tag{2.53}$$

Fig. 2.22 shows the simulated return loss, insertion loss, phase and input admittance of the dual-band transmission line and the proposed lumped-element 24/60-

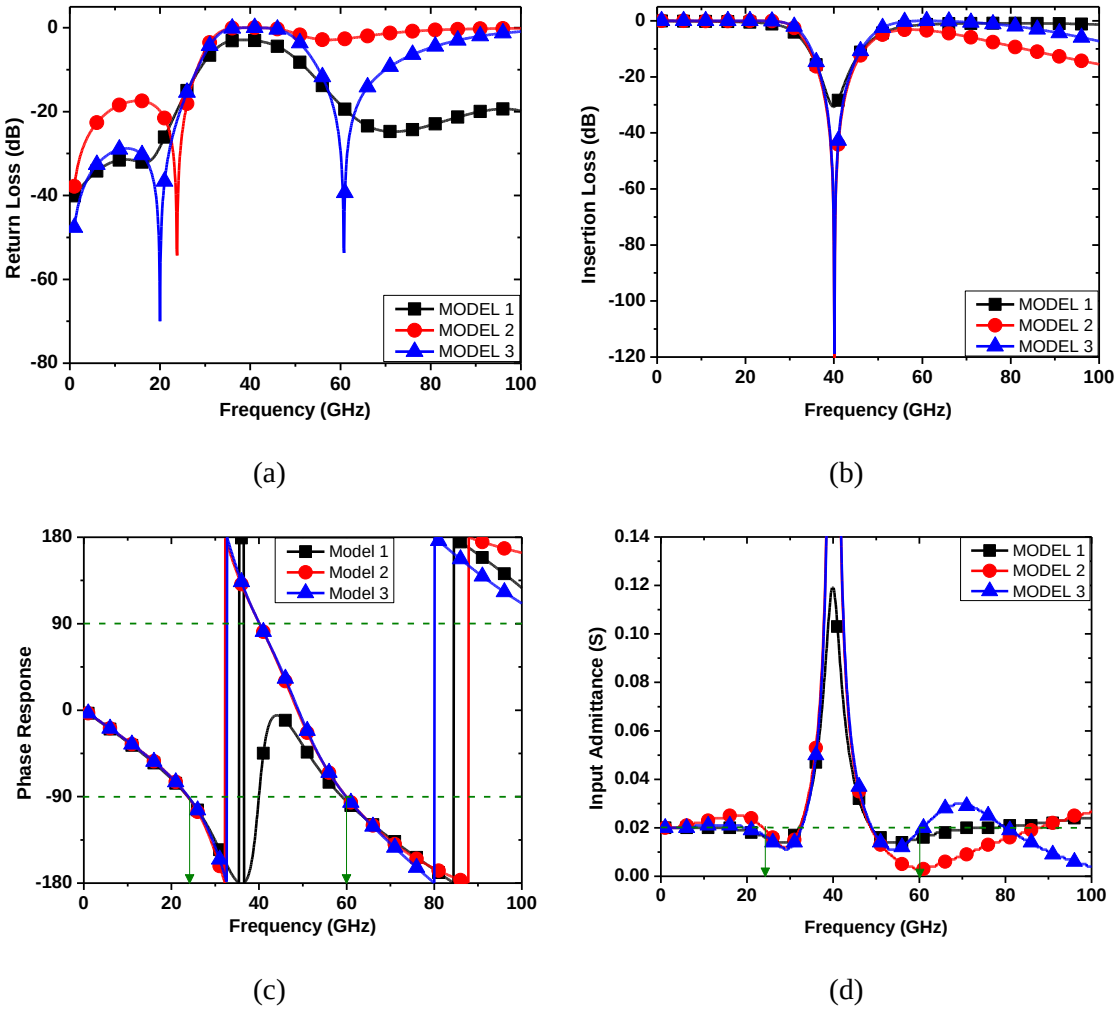


Fig. 2.22. Simulated return losses (a), insertion loss (b), phase response (c) and input admittance (d) of the 24/60-GHz dual-band transmission line and LC networks (Model 1, 2 and 3) shown in Fig. 2.21.

GHz dual-band networks. Models 1 and 3 clearly shows two pass and one stop bands, and λ/4 property (±90º) and the same input admittance at 24 and 60 GHz when the output ports of Models 1 and 3 are terminated with 50 Ω. However, even though Model 2 shows λ/4 property (±90º) at 24 and 60 GHz, it does not show two clear pass bands and the same input admittance at 24 and 60 GHz. To summarize, Model 3 is proposed as equivalent LC network of Model 1.

2.3.2 24/60-GHz Dual-Bandpass Filtering T/R Switch

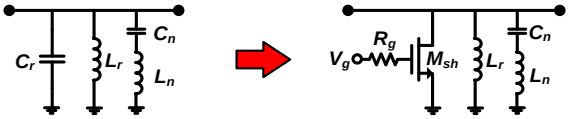
Fig. 2.23(a) shows the conventional dual-band resonator (left) and the implementation of the shunt switch by replacing C_r with an nMOS transistor (M_{sh}) (right) for switching function. The transistor is approximately equivalent to the channel resistance (R_{on}) and off-capacitance (C_{off}) when 1.8 and 0 V are applied to gate, respectively. Body-floating technique with deep *n*-well is applied to all the nMOS transistors not only to increase the isolation, but also to decrease the parasitic capacitances associated with the transistors. Fig. 2.23(b) shows the designed T/R switch with one transmitter (TX) port, two receiver (RX) ports, and two antenna (ANT) ports, where the two identical TX-ANT-RX sections are symmetrically placed with respect to the TX port. All the element values for the final design are listed in Table 2.2. The dual-band resonator with the nMOS transistor shown in Fig. 2.23(a) is connected in shunt at the end of each port and the dual-band LC network connects ANT ports to the TX and RX ports. In Fig. 2.23(b), C_{eq1} and L_{eq1} at A, B and C, and C_{eq2} and L_{eq2} at ports 4 and 5 are obtained as

$$C_{eq1} = C_1 + \frac{C_n}{2} \tag{2.54}$$

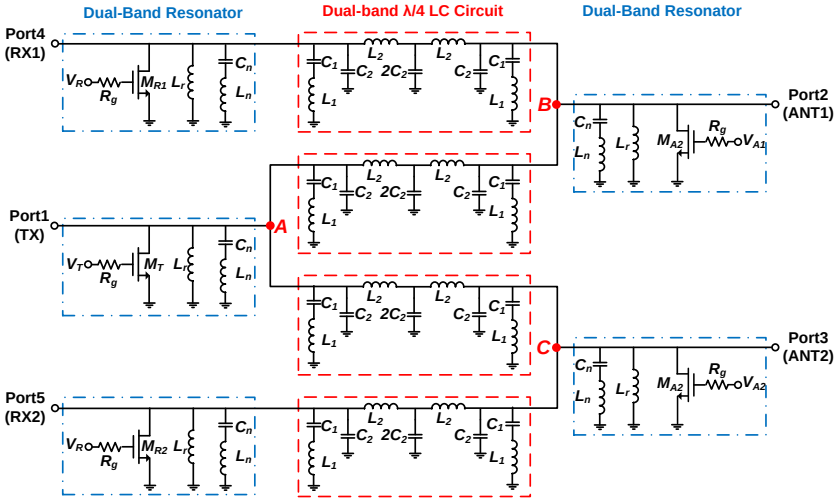
$$L_{eq1} = \left(\frac{1}{L_1} + \frac{1}{2L_n} \right)^{-1} \tag{2.55}$$

$$C_{eq2} = C_1 + C_n \tag{2.56}$$

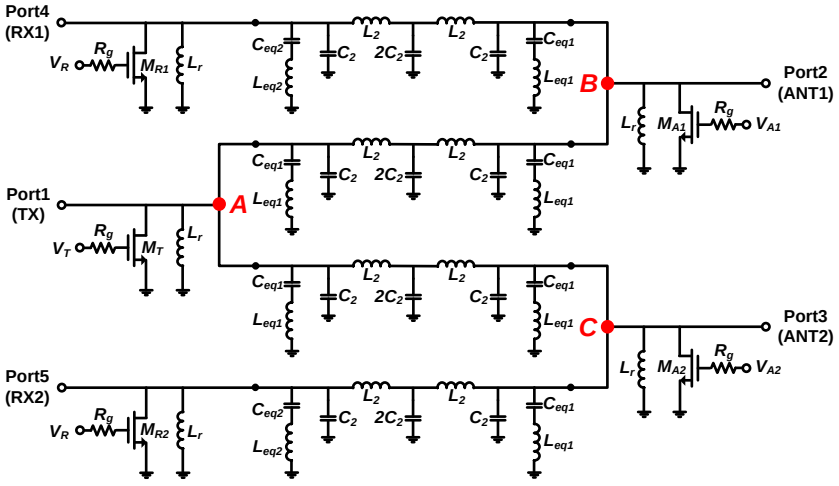
$$L_{eq2} = \left(\frac{1}{L_1} + \frac{1}{L_n} \right)^{-1} \tag{2.57}$$



(a)



(b)



(c)

Fig. 2.23. Schematics of the 24/60-GHz dual-band resonator (a) and dual-bandpass T/R switch (b) and (c).

, where C_n, L_n are elements of the dual-band resonator and C_1, L_1 are of the dual-band

Table 2.2
Dual-Band Band-Pass Filtering T/R Switch's Parameters

C_2	20 *f*F	C_{eq1}	84 *f*F
C_{eq2}	103 *f*F	L_2	165 *p*H
L_r	230 *p*H	L_{eq1}	193 *p*H
L_{eq2}	138 *p*H	Z_a	82 Ω
Z_b	52 Ω	Θ_a, Θ_b	2π/7
R_g	1 kΩ	V_T, V_R, V_{A1}, V_{A2}	0, 1.8 V
M_T, M_{A1}, M_{A2}, M_R	0.18 μm / 102.4 μm	R_{on}	10 Ω
C_{off}	61.5 *f*F		

LC circuit.

The designed T/R switch has two different operation modes: receiving and transmitting. In the receiving mode inferred from Fig. 2.23(c), M_T at TX port is turned on while all other transistors are turned off. Under this condition, switching points B and C appear as on-state looking toward the RX1, RX2 ports and off-state looking into the TX port at the two pass-bands' frequencies through the dual-band LC networks and off-state (M_R) and on-state (M_T) transistors, respectively. For the transmitting mode deduced from Fig. 2.23(c), M_T and M_{A1} (or M_{A2}) are turned off while the rest of the transistors are turned on. The TX port to ANT 1 (or ANT 2) port via the A and B (or C) is in on-state; on the other hand, the ANT 1 and 2 ports to RX 1 and 2 ports are in off-state at the two pass-bands' frequencies through the dual-band LC network and on-state transistors (M_R). This T/R switch is configured for use in a particular phased-array system in which vertically and horizontally polarized signals are transmitted separately and received simultaneously. It can be implemented in a front-end module similar to that proposed in [29].

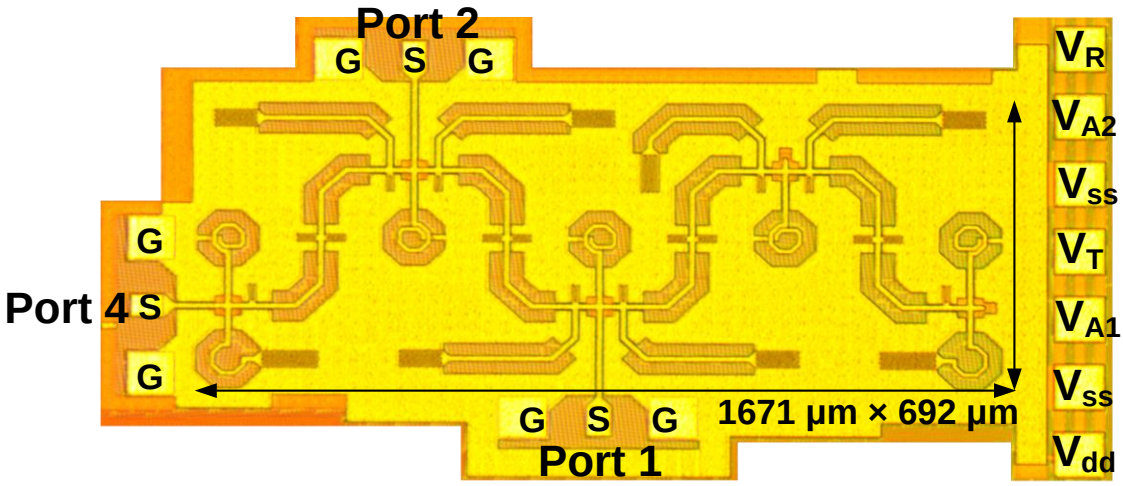


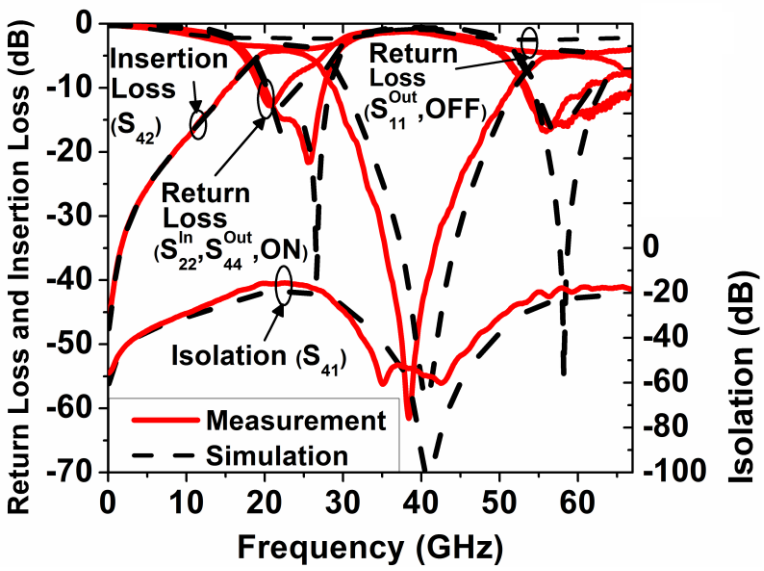
Fig. 2.24. Microphotograph of the fabricated 24/60-GHz dual-bandpass T/R switch. The port numbers correspond to those in Fig. 2.23(c).

The CMOS T/R switch was fabricated using a TowerJazz 0.18-μm SiGe BiCMOS process [30]. Due to the limited ports on the network analyzer, only three ports (TX, ANT1, RX1) of the T/R switch could be measured to verify its performance. The un-measured ports (Port 3 and 5 in Fig. 2.23(c)) are terminated with 50-Ω. Fig. 2.24 shows a microphotograph of the fabricated T/R switch that occupies 1671 μm × 692 μm excluding all the test pads.

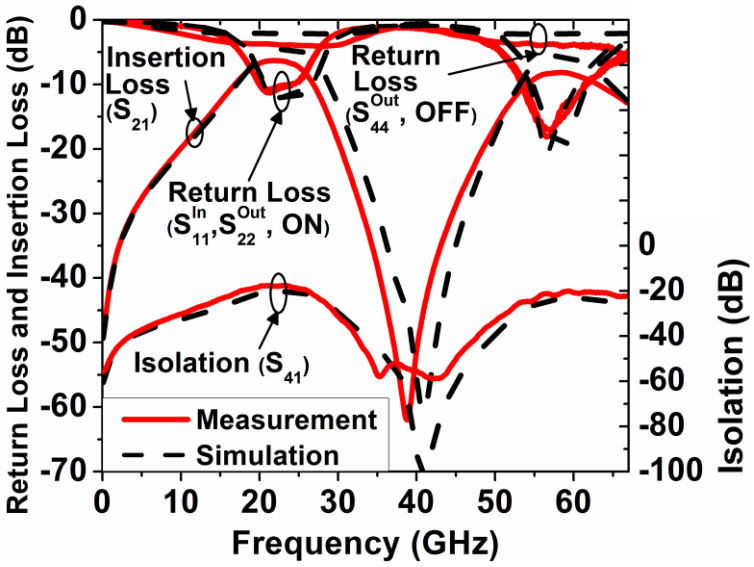
2.3.3 Simulation and Measurement Results

Fig. 2.25 shows the measured and simulated insertion loss (IL), return loss (RL), and isolation (ISO) of the designed T/R switch for the receiving and transmitting operating modes. The measured and simulated results show good agreement. For the receiving mode as shown in Fig. 2.25(a), the measured ILs (S_{42}) are 4.5 and 5 dB at 24 and 60 GHz, respectively. The measured 3-dB bandwidths (BW) are from 17.2 to 27.3 GHz and from 52.5 to 66.5 GHz. The measured input (S_{22}), output (S_{44}) RLs are 16 and 8 dB at 24 GHz, and 11.5 and 14 dB at 60 GHz. The measured ISOs between the TX (Port 1) and RX (Port 4) are 16 and 18.3 dB at 24 and 60 GHz, respectively. Stop-band rejection of over 40 dB is from 36.2 to 40.8 GHz and the peak rejection is 61.5 dB at 38.4 GHz. For the transmitting mode as shown in Fig. 2.25(b), the measured ILs (S_{21}) at 24 and 60 GHz are 6.7 and 8.5 dB, respectively. The measured 3-dB BWs are 17.1–26.7 and 52.8–65.2 GHz. The measured input (S_{11}), output (S_{22}) RLs are 10, 10.2 dB at 24 GHz and 12.7, 12.6 dB at 60 GHz, respectively. The TX–RX measured ISOs (S_{41}) are 18.2 and 20.8 dB at 24 and 60 GHz, respectively. Stop-band rejection exceeding 40 dB is from 35.8–41.3 GHz and the peak rejection is 65.5 dB at 38.3 GHz. The ILs at 24 and 60 GHz in the transmitting mode are little bit higher than those in the receiving mode because of two switching points (A, B or A, C in Fig. 2.23(c)) in the transmitting path as compared to only one switching point (B or C in Fig. 2.23(c)) in the receiving path.

Fig. 2.26(a) and (b) show the measured output power and IL versus input power of the designed T/R switch for different transmitting modes. When single tones at 24 and 60 GHz are applied, the measured input and output 1-dB compression points (IP_{1dB} and



(a)



(b)

Fig. 2.25. Measured and simulated results of the 24/60-GHz dual-bandpass T/R switch: (a) receiving and (b) transmitting operations.

OP_{1dB}) are 23.3 and 15.4 dBm at 24 GHz, and 18.4 and 9.1 dBm at 60 GHz, respectively,

as shown in Fig. 2.26(a). For concurrent dual-tone (24-/60-GHz) input, the IP_{1dB} and OP_{1dB} are 19 and 11.3 dBm measured at 24 GHz, and 16.8 and 7.8 dBm measured at 60 GHz, respectively. The measured P_{1dB} 60 GHz is lower than those at 24 GHz due to higher nonlinear parasitic capacitances of the off-state shunt transistors at 60 GHz. The increased IL occurred beyond the IP_{1dB} point is due to the loss compression resulted from the power compression.

Fig. 2.26(c) and (d) show the measured third-order intercept point (IP_3) for single-band transmitting modes with two tones spaced 100 MHz apart. At 24 GHz as shown in Fig. 2.26(c), the measured IIP_3 and OIP_3 are 31.5 and 24 dBm, respectively. At 60 GHz, the measured IIP_3 and OIP_3 are 31.5 and 24 dBm, respectively, as shown in Fig. 2.26(d).

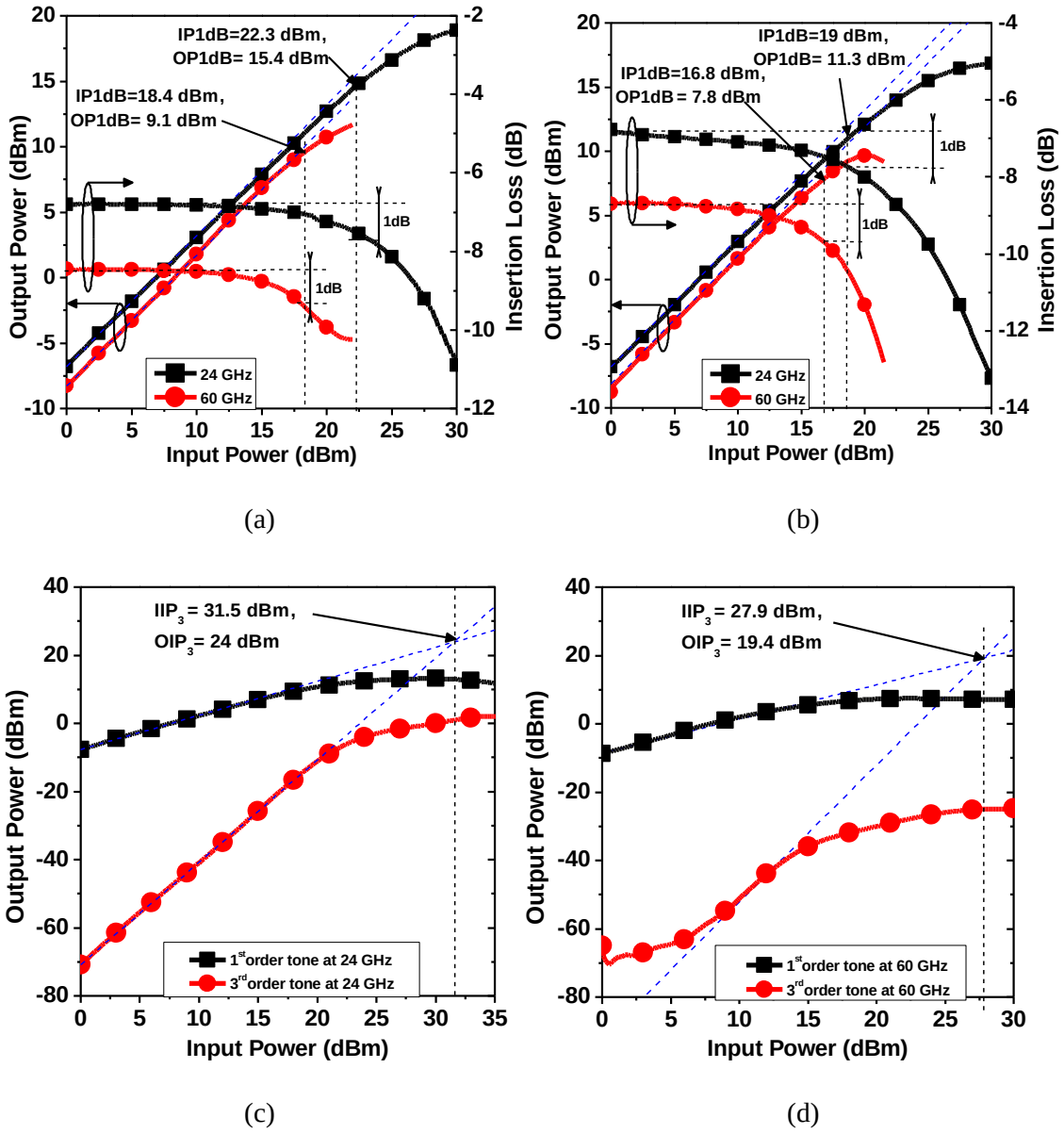


Fig. 2.26. Measured P_{1dB} of the designed T/R switch with 24-GHz and 60-GHz single-tone input (a) and 24-/60-GHz concurrent dual-tone input (b), and measured IP_3 for single-band mode at 24 GHz (c) and 60 GHz (d).

2.4 High-Isolation Multi-Mode Multi-Function 24/60-GHz CMOS Dual-Band Band-Pass Filtering SPDT and T/R Switches (Design 3)

In this chapter, we report the development of new 0.18-μm CMOS dual-band band-pass filtering SPDT and T/R switches operating in two different frequency bands centered around 24 and 60 GHz. These switches can operate in a variety of separate and concurrent modes, either in single-band, dual-band, transmission, reception, or simultaneous transmission and reception, with band-pass filtering and enhanced isolation. They can also function as a diplexer with switching capability. The T/R switch, especially, allows the transmission and reception in multi-band to be carried out simultaneously with a single antenna – a highly desirable feature for multi-band RF systems, which cannot be achieved with conventional T/R switch that can only transmit and receive signals at different times – which could help expand the usage or applications of RF systems. The designs of the 24/60-GHz dual-band band-pass filtering SPDT and T/R switches involve the designs of the individual single-band 24- and 60-GHz band-pass filtering SPST switches. The architectures, designs, and analyses of these single-band band-pass filtering SPST switches and dual-band band-pass filtering SPDT and T/R switches are described in this chapter. Analytical equations for the switches' insertion losses and isolations are derived and can be used for possible trade-off between the insertion loss and isolation in a design.

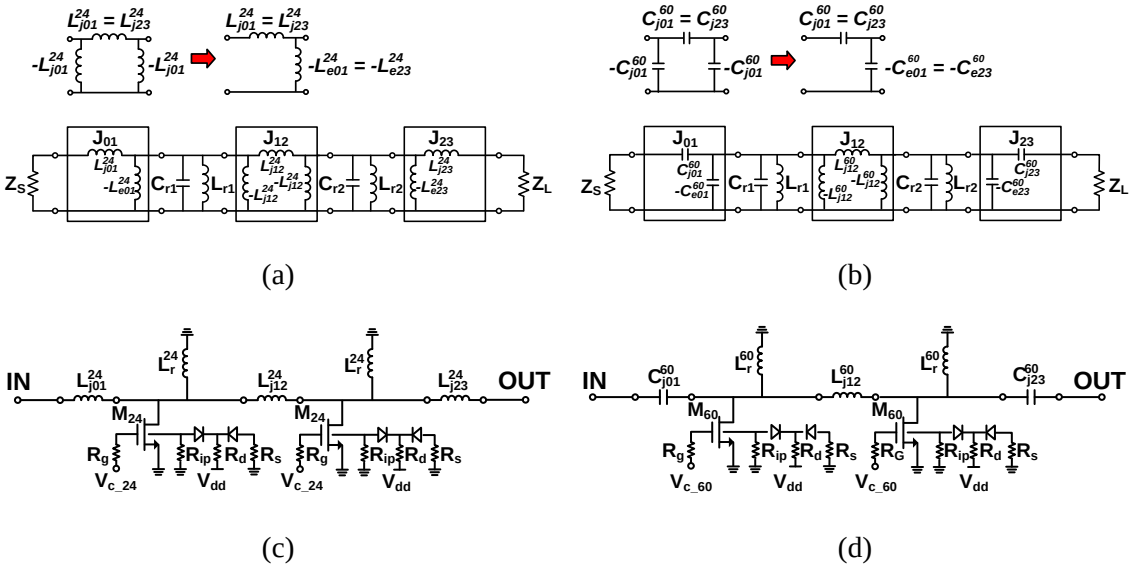


Fig. 2.27. Schematics of the band-pass filtering SPST switches: (a) 24-GHz band-pass filter and J-inverter implementation, (b) 60-GHz band-pass filter and J-inverter implementation, (c) 24-GHz band-pass filtering SPST switch, and (d) 24-GHz band-pass filtering SPST switch.

2.4.1 Single-Band 24- and 60-GHz Band-Pass Filtering SPST Switches

The single-band 24- and 60-GHz band-pass filtering SPST switches are designed based on a second-order band-pass filter (BPF) with admittance inverters (J-inverters) and parallel resonators as shown in Figs. 2.27(a) and (b), respectively. The BPF design procedure was already described in Sec. 2.1.5. The 24- and 60-GHz filters have 0.01 dB ripple with a fractional bandwidth of 30 % centered at 24/60 GHz and more than 50-dB rejection at 60/24 GHz, respectively. The elements' values for the 24- and 60-GHz filters are $C_{r1,\,r2}$ = 343, 165 *f*F and $L_{r1,\,r2}$ = 120, 40 *p*H at 24, 60 GHz, respectively, and Z_S, Z_L = 50 Ω. The filter would behave as a SPST switch with band-pass filtering characteristics when the capacitors of the filter's resonators are replaced with transistors biased for on- and off-state operations.

Figs. 2.27(c) and (d) show the schematics of the 24- and 60-GHz band-pass filtering SPST switches, respectively. The series inductor $L_{j01,j23}^{24}$ and capacitor $C_{j01,j23}^{60}$ in J_{01} and J_{23} of the 24- and 60-GHz band-pass filtering SPST switches have low- and high-pass responses, respectively, prohibiting the 60- and 24-GHz signals from passing through them, respectively. This useful feature, achieved by unique arrangements of the SPST topologies, enables the dual-band band-pass filtering 24/60-GHz SPDT and T/R switches formed by these SPST switches to separate the input signals at 24 and 60 GHz to produce the dual-band band-pass filtering responses.

The ABCD matrices of the 24- and 60-GHz SPST switch in Figs. 2.27(c) and (d) can be derived as

$$ABCD = \begin{pmatrix} 1 & Z_{j01} \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & 0 \\ Y_{nMOS} + Y_{L_r} & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & Z_{j12} \\ 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & 0 \\ Y_{nMOS} + Y_{L_r} & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & Z_{j23} \\ 0 & 1 \end{pmatrix} \quad (2.58)$$

where $Z_{j01} = j\omega L_{j01}^{24}$ or $1/j\omega C_{j01}^{60}$, $Z_{j12} = j\omega L_{j12}^{24}$ or $j\omega L_{j12}^{60}$, and $Z_{j23} = j\omega L_{j23}^{24}$ or $1/j\omega C_{j23}^{60}$ are the impedances of J_{01}, J_{12} and J_{23} in the 24- or 60-GHz SPST switch, respectively; $Y_{nMOS} = 1/\left(1/j\omega C_{eq}^{M24,M60} + R_{ch}^{M24,M60}\right)$ is the admittance of shunt transistor M_{24} or M_{60}, respectively, with R_{ch}^{M24}, C_{eq}^{M24} and R_{ch}^{M60}, C_{eq}^{M60} being the equivalent resistance, capacitance of M_{24} and M_{60}, respectively; and $Y_{L_r} = 1/j\omega L_r^{24,60}$ is the respective admittance of inductors $L_r^{24,60}$.

The transmission coefficient (T) of the 24- and 60-GHz SPST switch can be derived from (2.58) as

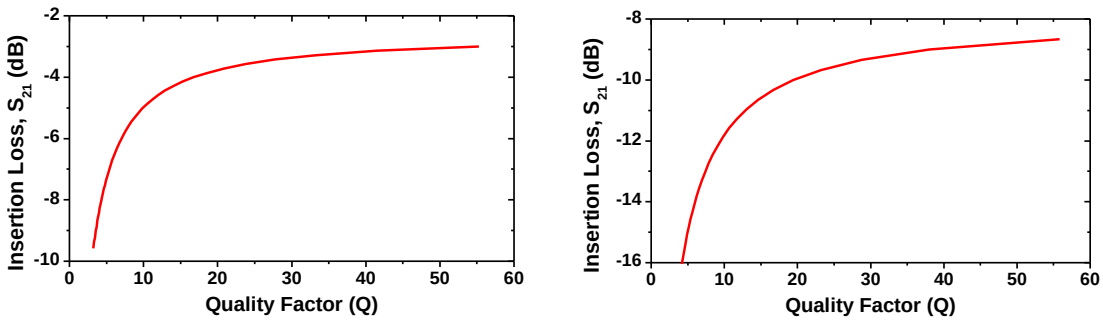
$$T = \left| \frac{2Z_0\omega^2 L_r^2 \left(1 + jR_{ch}C_{eq}\omega\right)^2}{\left(A\omega^2 + B\omega + C\right)\left(D\omega^2 + E\omega + F\right)} \right| \tag{2.59}$$

where $A = -C_{eq}L_r\left(R_{ch} + Z_0 + Z_{j01}\right)$, $B = j\left[L_r + R_{ch}C_{eq}\left(Z_0 + Z_{j01}\right)\right]$, $C = Z_0 + Z_{j01}$

$D = -C_{eq}L_r\left[R_{ch}\left(2Z_0 + Z_{j01} + Z_{j12}\right) + Z_{j12}\left(Z_0 + Z_{j01}\right)\right]$,

$E = j\left[L_r\left(2Z_0 + 2Z_{j01} + Z_{j12}\right) + R_{ch}C_{eq}L_rZ_{j12}\left(Z_0 + Z_{j01}\right)\right]$, $F = Z_{j12}\left(Z_0 + Z_{j01}\right)$ and Z_0 is the source impedance. Note that there are two different values for C_{eq} (C_{eq}^{M24} or C_{eq}^{M60}), R_{ch} (R_{ch}^{M24} or R_{ch}^{M60}), L_r (L_r^{24} or L_r^{60}), Z_{j01} ($j\omega L_{j01}^{24}$ or $1/j\omega C_{j01}^{60}$), Z_{j12} ($j\omega L_{j12}^{24}$ or $1/j\omega L_{j12}^{60}$) and Z_{j23} ($j\omega L_{j23}^{24}$ *or* $1/j\omega C_{j23}^{60}$) corresponding to the 24- or 60-GHz SPST switch. T represents the insertion loss (T_{on}) or isolation (T_{off}) of the on- and off-state SPST switches, respectively.

Fig. 2.28 shows the insertion loss of the off-state transistors M_{24} ($C_{eq}^{M24} = 340\,fF$) and M_{60} ($C_{eq}^{M60} = 190\,fF$) at 24 and 60 GHz with respect to the quality factor ($Q = 1/\omega R_{ch}^{M24}C_{eq}^{M24}$ and $1/\omega R_{ch}^{M60}C_{eq}^{M60}$), calculated using (2.59) Fig. 2.28 shows that the *Q* of the off-state transistors employed in the SPST switches affects substantially the switches' insertion loss and causes a relatively high insertion loss at 60 GHz, where the *Q* is around 28 as seen in Fig. 2.28. Equation (2.59) will be used to derive the insertion loss and isolation of the SPDT and T/R switches to be described in Sec. 2.4.2 and 2.4.3.



(a) (b)

Fig. 2.28. Simulated insertion losses of the 24- and 60-GHz SPST switches versus Q of the off-state transistors: Transistor M_{24} at 24 GHz (a) and Transistor M_{60} at 60 GHz (b).

2.4.2 24/60-GHz Dual-Band Band-Pass Filtering SPDT Switch

Unlike conventional single-band SPDT switches consisting of two identical SPST switches operating at same frequencies, the 24/60-GHz dual-band band-pass filtering SPDT switch is comprised of two band-pass filtering SPST switches operating at two different frequency bands centered at 24 and 60 GHz as shown in Fig. 2.29. This SPDT switch is part of the T/R switch to be described in Sec. 2.4.3. Due to two different pass-bands inherently created by the constituent 24- and 60-GHz band-pass filtering SPST switches, whose topologies are especially configured as described in Sec. 2.4.1, the 24/60-GHz dual-band band-pass filtering SPDT switch can also be used as a diplexer with switching function for the 24- and 60-GHz bands. The 24/60-GHz dual-band band-pass filtering SPDT switch can operate in three different modes as follows:

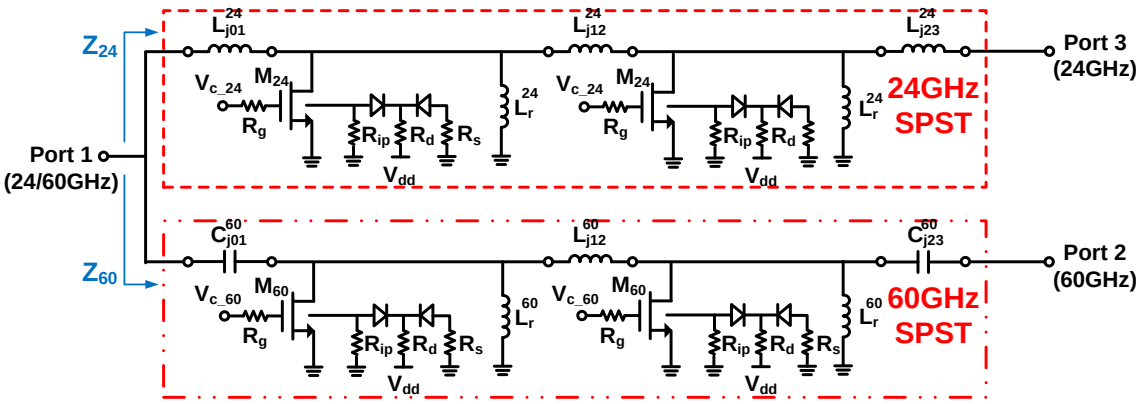


Fig. 2.29. Schematic of the 24/60-GHz dual-band band-pass filtering SPDT switch.

24-GHz Single-Band Operation Mode

The 24-GHz operation mode is described in the equivalent circuits of the 24/60-GHz dual-band band-pass filtering SPDT switch as shown in Fig. 2.30(a). It is obtained when transistors M_{24} in the 24-GHz SPST are biased in off-state, which are represented by equivalent capacitors C_{eq}^{M24}, and transistors M_{60} in the 60-GHz SPST are in on-state represented by equivalent channel resistors R_{ch}^{M60}. Under these bias conditions at 24 GHz, the 24-GHz path is approximately matched to the input of the SPDT while the 60-GHz path approaches an approximate open circuit through the J-inverters J_{01} and J_{23}. Consequently, most of the 24-GHz input signal is transmitted through the 24-GHz SPST switch.

The insertion loss S_{31} and isolation between the two output ports S_{23} can be derived as

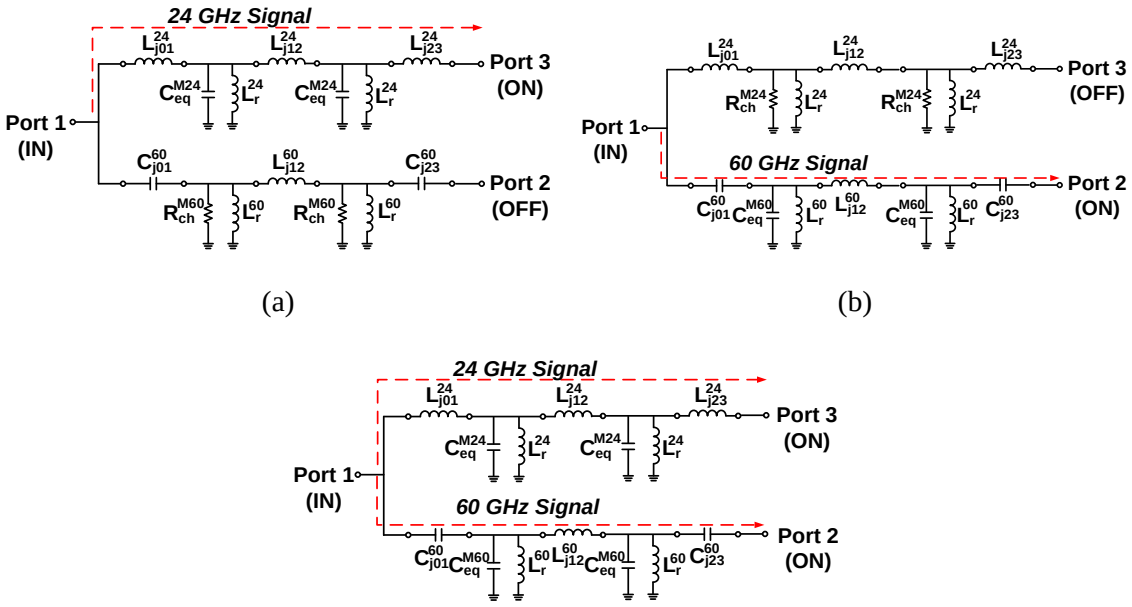


Fig. 2.30. Operations of the 24/60-GHz dual-band band-pass filtering SPDT switch: (a) 24-GHz single-band operation, (b) 60-GHz single-band operation, and (c) 24/60-GHz concurrent dual-band operation.

$$S_{31} = \frac{Z_{60}^{off}}{Z_{24}^{on} + Z_{60}^{off}} T_{on}^{24} \tag{2.60}$$

$$S_{23} = T_{on}^{24} T_{off}^{60} \tag{2.61}$$

, where Z_{24}^{on} and Z_{60}^{off} are the corresponding input impedances Z_{24} and Z_{60} (shown in Fig. 2.29) looking into the on-state 24-GHz path (with M_{24} off) and off-state 60-GHz path (with M_{60} on), respectively, and $T_{on(off)}^{24(60)}$ denotes the insertion loss (T_{on}) or isolation (T_{off}) from (2.59) at 24(60) GHz, respectively.

60-GHz Single-Band Operation Mode

The 60-GHz operation mode can be inferred from Fig. 2.30(b) corresponding to transistors M_{24} in on-state, represented by equivalent channel resistors R_{ch}^{M24}, and transistors M_{60} in off-state characterized with equivalent capacitors C_{eq}^{M60}. The 60-GHz path is approximately matched to the input of the SPDT at 60 GHz while the 24-GHz path presents an approximate open circuit, hence forcing the majority of the 60-GHz input signal to traverse the 60-GHz SPST switch.

The insertion loss S_{21} and isolation between the two output ports S_{32} are obtained as

$$S_{21} = \frac{Z_{24}^{off}}{Z_{24}^{off} + Z_{60}^{on}} T_{on}^{60} \tag{2.62}$$

$$S_{32} = T_{off}^{24} T_{on}^{60} \tag{2.63}$$

, where Z_{24}^{off} and Z_{60}^{on} are the corresponding input impedances Z_{24} and Z_{60} (shown in Fig. 2.29) looking into the 24-GHz path with M_{24} on and 60-GHz path with M_{60} off, respectively.

24/60-GHz Concurrent Dual-Band Operation Mode

The 24/60-GHz concurrent dual-band operation mode is described in the equivalent circuit as shown in Fig. 2.30(c). In this operation, transistors M_{24} and M_{60} are biased off-state represented by C_{eq}^{M24} and C_{eq}^{M60}. The 24-GHz path simultaneously presents approximate matching and open circuit to the input of the SPDT at 24 and 60 GHz,

respectively. On the other hand, the 60-GHz path concurrently provides approximate matching and open circuit to the SPDT's input at 60 and 24 GHz, respectively. As a result, the 24- and 60-GHz signals are routed separately, yet concurrently, through the 24- and 60-GHz SPST switches, respectively.

The insertion losses, S_{31} and S_{21}, and isolation S_{32} can be derived as

$$S_{31} = \frac{Z_{60}^{on}}{Z_{24}^{on} + Z_{60}^{on}} T_{on}^{24} \tag{2.64}$$

$$S_{21} = \frac{Z_{24}^{on}}{Z_{24}^{on} + Z_{60}^{on}} T_{on}^{60} \tag{2.65}$$

$$S_{32} = T_{on}^{24} T_{on}^{60} \tag{2.66}$$

The foregoing qualitative analysis gives the operation principles of the 24/60-GHz dual-band band-pass filtering SPDT switch in three different operating modes and verifies that it can support both concurrent dual-band and single-band operations.

2.4.3 24/60-GHz Dual-Band Band-Pass Filtering T/R Switch

Fig. 2.31 shows the schematic of the 24/60-GHz dual-band band-pass filtering T/R switch implemented using four SPST switches (or three SPDT switches). It has five different ports: Port 1 is the transmitting (*TX*) port for both 24- and 60-GHz signals; Port 2 (*ANT1*) and Port 3 (*ANT2*) are the antenna ports for both 24 and 60 GHz; and Port 4 (*RX1*) and Port 5 (*RX2*) are the receiving (*RX*) ports for 24- and 60- GHz signals, respectively. The antenna (*ANT*) ports could belong to a single antenna with two ports operating concurrently at 24 and 60 GHz or two different antennas operating

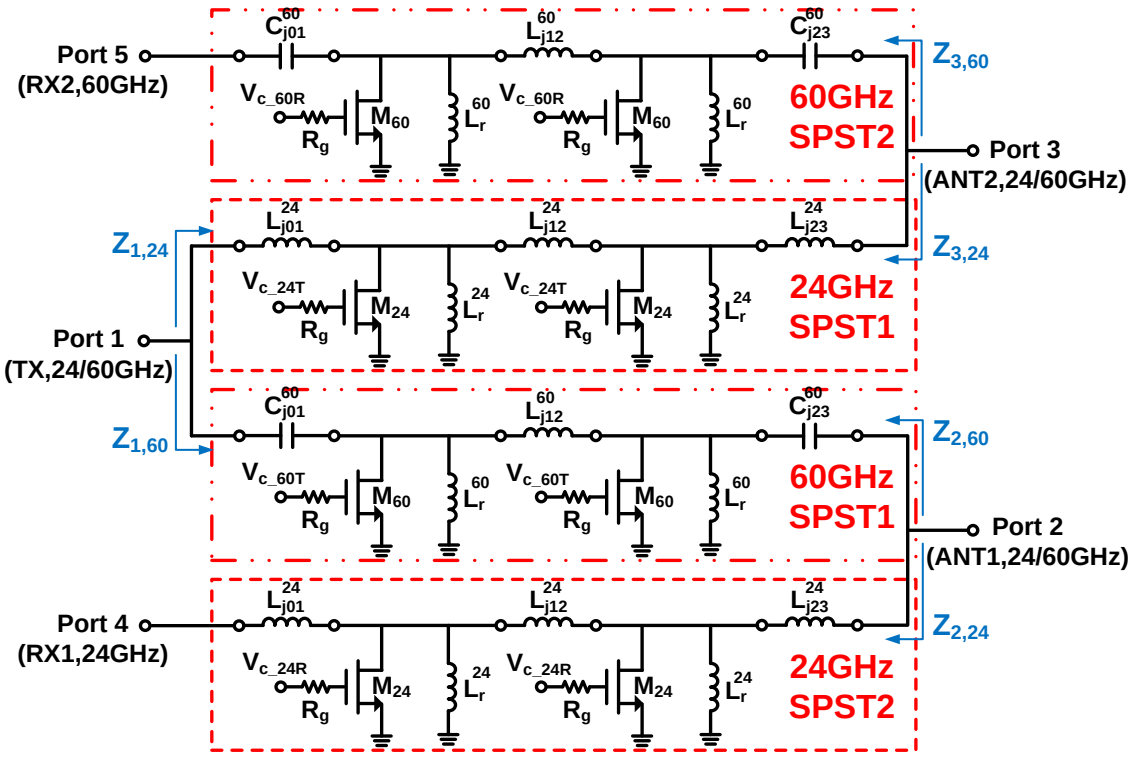


Fig. 2.31. Schematic of the 24/60-GHz dual-band band-pass filtering T/R switch.

Table 2.3
Dual-Band Band-Pass Filtering T/R Switch's Parameters

M_{24}	420 μm / 0.18 μm	M_{60}	280 μm / 0.18 μm
R_{ch_M24}	1.42 Ω	R_{ch_M60}	2.15 Ω
L_{j01_24}, L_{j23_24}	330 pH	L_{j12_24}	360 pH
C_{j01_60}, C_{j23_60}	60 fF	L_{j12_60}	220 pH
L_{24}	248 pH	L_{60}	35 pH
R_{ip}	10 kΩ	R_d	20 kΩ
R_g	1 kΩ	V_{dd}	1.8 V

concurrently at 24 and 60 GHz. Table 2.3 shows the T/R switch's design parameters and their values.

The 24/60-GHz dual-band band-pass filtering T/R switch can function in various

operating modes consisting of three transmitting modes (24-GHz TX, 60-GHz TX and 24/60-GHz concurrent TX), three receiving modes (24-GHz RX, 60-GHz RX and 24/60-GHz concurrent RX), and four concurrent transmitting and receiving modes (24-GHz TX/RX, 60-GHz TX/RX, 24-GHz TX/60-GHz RX and 24-GHz RX/60-GHz TX). Fig. 2.4.6 shows the concurrent operation modes at 24 GHz (24-GHz TX/RX), 60 GHz (60-GHz TX/RX), and 24/60 GHz (24-GHz RX/60-GHz TX) of the T/R switch and their equivalent circuits. Other operating modes can also be illustrated similarly.

One of the most crucial requirements in multi-band T/R switches designed for concurrent TX and RX operations with a single antenna is the isolation between the TX and RX ports under the concurrent operation. Conventional T/R switches, either single- or multi-band operation, are not suitable for concurrent TX and RX operations at the same frequency due the need of turning both the TX and RX paths on at the same time. The proposed 24/60-GHz dual-band band-pass filtering T/R switch overcomes the isolation problem and enables concurrent transmitting and receiving operations due to two reasons. First, different frequency bands are used in adjacent TX and RX ports, hence facilitating increased isolation between TX and RX ports - for example, between the TX port at Port 1 and RX port at Port 5 in Fig. 2.31, in which the 24GHz SPST1 between Port 1 and Port 3 is operated at 24 GHz, while the 60GHz SPST2 between Port 3 and Port 5 is operated at 60 GHz. Second, the actual isolation is provided by a combination of the isolation caused by the off-state of the SPST switch and the stop-band rejection of the band-pass filter of the off-state SPST switch. This is particularly useful for CMOS switches at millimeter wave frequencies since increased parasitic

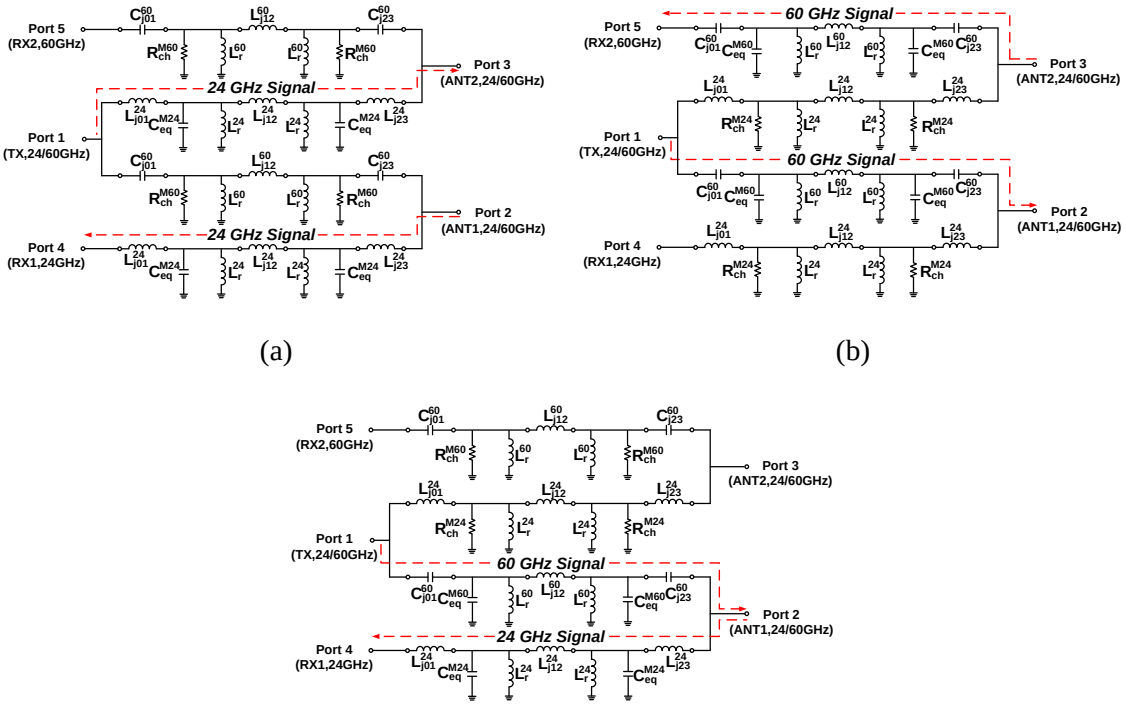


Fig. 2.32. Operations of the 24/60-GHz dual-band band-pass filtering SPDT switch: (a) 24-GHz single-band operation, (b) 60-GHz single-band operation, and (c) 24/60-GHz concurrent dual-band operation.

capacitances of off-state MOSFETs at these frequencies could limit the isolation [19]. For illustration purpose, we examine the TX/RX concurrent operations at 24 and 60 GHz as shown in Fig. 2.32 in view of the TX-RX isolation.

24-GHz TX/RX Concurrent Operation

The 24-GHz TX/RX concurrent operation mode is described in the equivalent circuit, shown in Fig. 2.32(a), which corresponds to the 24GHz SPST1 and SPST2 and the 60GHz SPST1 and SPST2 in Fig. 2.31 being on and off, respectively. In this

operation, the isolation between Port 1 (*TX* port) and Port 4 (*RX1* port) is primarily due to the isolation at 24 GHz caused by the 60GHz SPST1 being in off-state and the rejection at 24 GHz of the band-pass function of the 60GHz SPST1.

The insertion losses S_{31}, S_{42} and isolation (S_{41}) between Port 1 (*TX* port) and Port 4 (*RX1* port) can be derived as

$$S_{31} = \left(\frac{Z_{1,60}^{off}}{Z_{1,24}^{on} + Z_{1,60}^{off}} \right) \left(\frac{Z_{3,60}^{off}}{Z_{3,24}^{on} + Z_{3,60}^{off}} \right) T_{on}^{24} \tag{2.67}$$

$$S_{42} = \left(\frac{Z_{2,60}^{off}}{Z_{2,24}^{on} + Z_{2,60}^{off}} \right) T_{on}^{24} \tag{2.68}$$

$$S_{41} = S_{42} S_{21} = S_{42} \left(\frac{Z_{1,24}^{on}}{Z_{1,24}^{on} + Z_{1,60}^{off}} \right) \left(\frac{Z_{2,24}^{on}}{Z_{2,24}^{on} + Z_{2,60}^{off}} \right) T_{off}^{60} \tag{2.69}$$

, where $Z_{1(2,3),24(60)}^{on(off)}$ are the impedances denoted in Fig. 2.31 looking into the on (off)-state 24(60GHz) path at Ports 1, 2 and 3, respectively.

60-GHz TX/RX Concurrent Operation

60-GHz TX/RX concurrent operation mode is described in the equivalent circuit as shown in Fig. 2.32(b) corresponding to the 60GHz SPST1 and SPST2 and 24GHz SPST1 and SPST2 in Fig. 2.31 being on and off, respectively. In this operation, the isolation between Port 1 (*TX* port) and Port 5 (*RX2* port) is mainly contributed by the off-state of the 24GHz SPST1 at 60 GHz and the rejection at 60 GHz of the 24GHz SPST1's band-pass filter.

The insertion losses S_{21}, S_{53} and isolation S_{51} between Port 1 (*TX* port) and Port 5

(*RX2* port) can be derived as

$$S_{21} = \left(\frac{Z_{1,24}^{off}}{Z_{1,24}^{off} + Z_{1,60}^{on}} \right) \left(\frac{Z_{2,24}^{off}}{Z_{2,24}^{off} + Z_{2,60}^{on}} \right) T_{on}^{60} \tag{2.70}$$

$$S_{53} = \left(\frac{Z_{3,24}^{off}}{Z_{3,24}^{off} + Z_{3,60}^{on}} \right) T_{on}^{60} \tag{2.71}$$

$$S_{51} = S_{53} S_{31} = S_{53} \left(\frac{Z_{1,60}^{on}}{Z_{1,24}^{off} + Z_{1,60}^{on}} \right) \left(\frac{Z_{3,60}^{on}}{Z_{3,24}^{off} + Z_{3,60}^{on}} \right) T_{off}^{24} \tag{2.72}$$

24-GHz RX/60-GHz TX Concurrent Dual-Band Operation

The 24-GHz RX/60-GHz TX concurrent dual-band operation mode is described in the equivalent circuit shown in Fig. 2.32(c), which corresponds to the 24GHz SPST2, 60GHz SPST1 and 24GHz SPST1, 60GHz SPST2 in Fig. 2.31 being on and off, respectively. In this operation, the isolation between Port 1 (*TX* port) and Port 4 (*RX1* port) is mostly determined by the rejections at 24 and 60 GHz of the 60GHz SPST1 and 24GHz SPST2's band-pass filters.

24-GHz RX/60-GHz TX concurrent dual-band operation mode is described in the equivalent circuit shown in Fig. 2.32(c), which corresponds to the 24GHz SPST2 in Fig. 2.31 being on and off, respectively. In this operation, the isolation between Port 1 (*TX* port) and Port 4 (*RX1* port) is mostly determined by the rejections at 24 and 60 GHz of the 60GHz SPST1 and 24GHz SPST2's band-pass filters.

The insertion losses S_{21}, S_{42} and isolation S_{41} between Port 1 (*TX* port) and Port 4 (*RX1* port) can be derived as

$$S_{21} = \left(\frac{Z_{1,24}^{off}}{Z_{1,24}^{off} + Z_{1,60}^{on}} \right) \left(\frac{Z_{2,24}^{on}}{Z_{2,24}^{on} + Z_{2,60}^{on}} \right) T_{on}^{60} \tag{2.73}$$

$$S_{42} = \left(\frac{Z_{2,60}^{on}}{Z_{2,24}^{on} + Z_{2,60}^{on}} \right) T_{on}^{24} \tag{2.74}$$

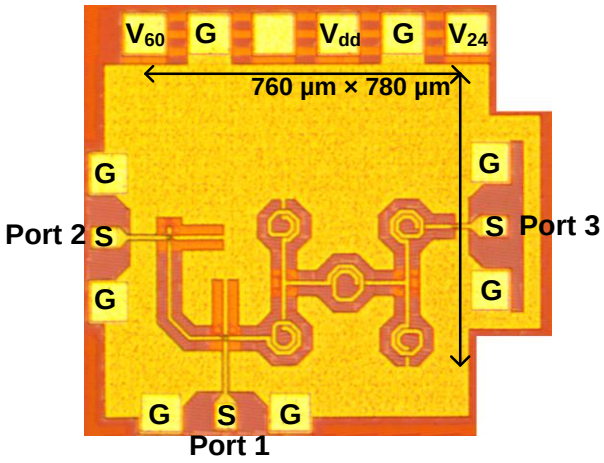
$$S_{41} = S_{42} S_{21} = S_{42} \left(\frac{Z_{1,24}^{off}}{Z_{1,24}^{off} + Z_{1,60}^{on}} \right) \left(\frac{Z_{2,24}^{on}}{Z_{2,24}^{on} + Z_{2,60}^{on}} \right) T_{on}^{60} \tag{2.75}$$

The 24/60-GHz dual-band band-pass filtering SPDT and T/R switches were designed and fabricated on a TowerJazz 0.18-μm SiGe BiCMOS process [27]. Fig. 2.33 shows the microphotographs of the SPDT switch and a part of the T/R switch. The fabricated partial T/R switch with 3 ports shown in Fig. 2.33(b) allows the 60-GHz transmitting and 24-GHz receiving modes to be measured using a 3-port vector network analyzer, and the results can be used to estimate accurately the performance for the 60-GHz receiving and 24-GHz transmitting modes due to the symmetrical structure of the T/R switch.

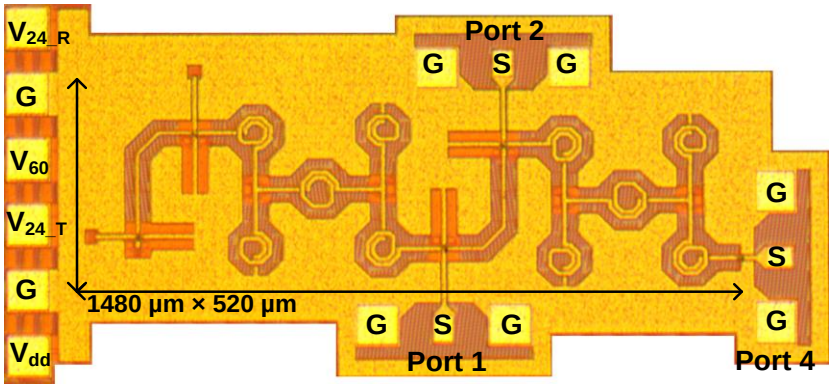
2.4.4 Simulation and Measurement Results

The fabricated 24/60-GHz dual-band band-pass filtering SPDT and T/R switches were measured on-wafer using Rhode & Schwarz vector network analyzer and Cascade probe station.

Fig. 2.34 shows the measured and simulated insertion losses, return losses and isolations of the SPDT and T/R switches. The ports corresponding to the measurement



(a)



(b)

Fig. 2.33. Microphotographs of the 24/60-GHz dual-band band-pass filtering SPDT switch (a) and T/R switch's part (b). The port numbers in (a) and (b) correspond to those in Fig. 2.31, respectively.

parameters are denoted in Fig. 2.33. The results of the SPDT switch are for the 24-GHz and 60-GHz single-band operation modes and the 24/60-GHz concurrent dual-band operation mode as described in Sec. 2.4.2.

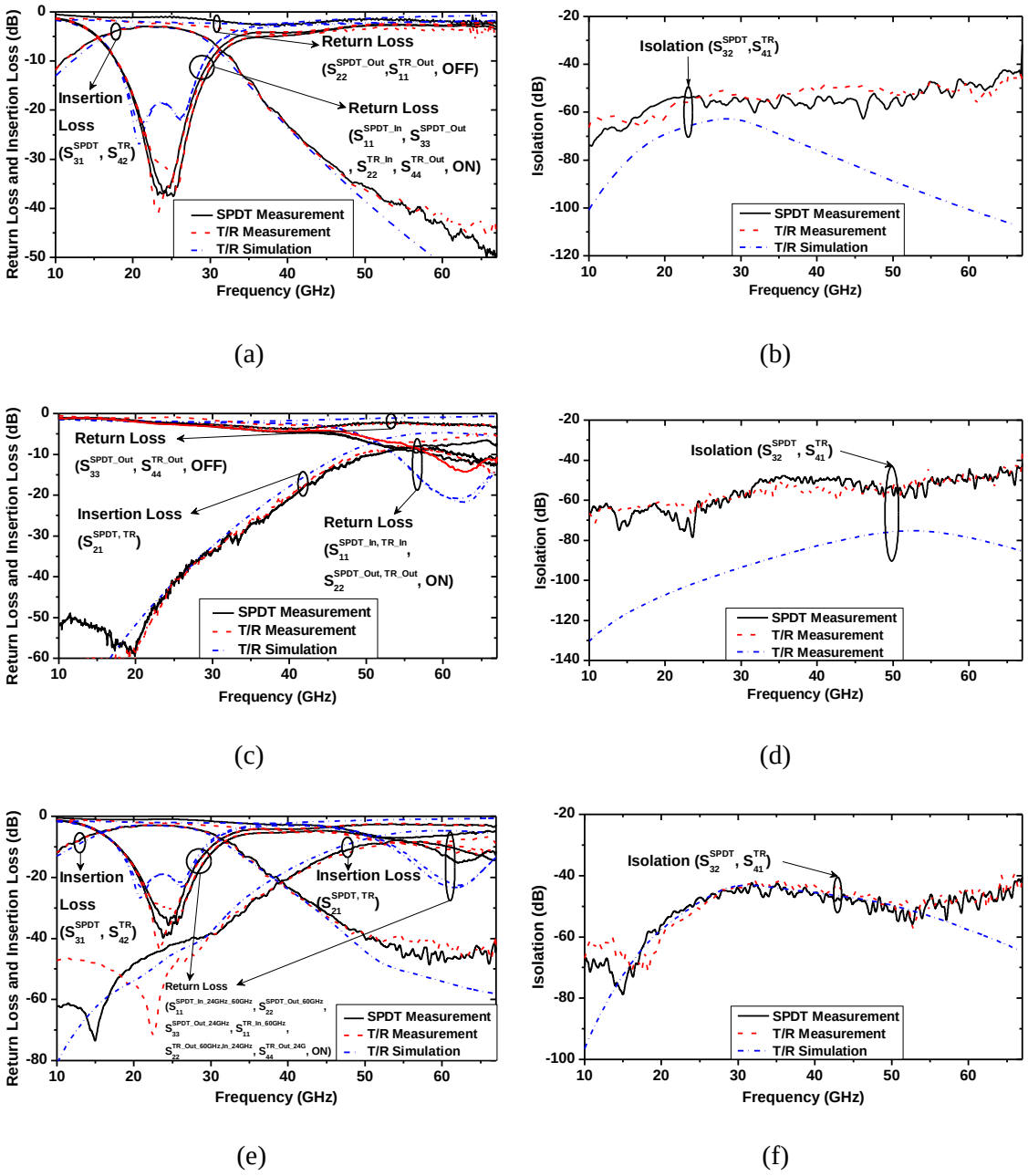


Fig. 2.34. Measured and simulated results of the 24/60-GHz dual-band band-pass filtering SPDT and T/R switches: (a) and (b) 24-GHz operation, (c) and (d) 60-GHz operation, and (e) and (f) 24/60-GHz concurrent operation.

The results of the T/R switch are for the 24-GHz RX operation, 60-GHz TX operation,

and the concurrent dual-band operation of 24-GHz RX (with 2 and 4 as input and output ports, respectively) and 60-GHz TX (with 1 and 2 as input and output ports, respectively) as described in Sec. 2.4.3. As mentioned in Chapter II, the results of the concurrent 24-GHz TX and 60-GHz RX operation are similar to those of the 24-GHz RX and 60-GHz TX operation. As can be seen, the results show good agreement between simulations and measurements.

Figs. 2.34(a) and (b) shows the results for the 24-GHz operation mode. The measured insertion losses of the SPDT (S_{31}^{SPDT}) and T/R (S_{42}^{TR}) switches are 3 and 2.9 dB at 24 GHz, respectively. The measured 3-dB bandwidths of the SPDT and T/R switches are from 14.7–30.3 GHz and 14.6–30.3 GHz, respectively. The measured input (S_{11}^{SPDT}, S_{22}^{TR}), output (S_{33}^{SPDT} , S_{44}^{TR}) return losses of the SPDT and T/R switches under on-state are 32, 32 dB and 32, 35 dB at 24 GHz, respectively. The measured isolations between the output ports of the SPDT (S_{32}^{SPDT}) and the TX and RX ports of the T/R (S_{41}^{TR}) switches are 56 and 53 dB at 24 GHz, respectively.

Figs. 2.34(c) and (d) shows the measured and simulated results for the 60-GHz operation mode. The measured insertion losses of the SPDT (S_{21}^{SPDT}) and T/R (S_{21}^{TR}) switches are 9.4 and 8.7 dB at 60 GHz, respectively. The measured 3-dB bandwidths of the SPDT and T/R switches are 48.5–64.3 GHz and 46.8–62.8 GHz, respectively. The measured input (S_{11}^{SPDT}, S_{11}^{TR}), output (S_{22}^{SPDT}, S_{22}^{TR}) return losses of the SPDT and T/R switches under on-state are 7.5, 12 dB and 7, 11.5 dB at 60 GHz, respectively. The measured isolations between the output ports of the SPDT (S_{32}^{SPDT}) and the TX and RX

ports of the T/R (S_{41}^{TR}) switches are 43 dB at 60 GHz.

Figs. 2.34(e) and (f) shows the measured and simulated results for the 24/60-GHz concurrent operation mode. The measured insertion losses of the SPDT ($S_{31}^{SPDT\_24GHz}$, $S_{21}^{SPDT\_60GHz}$) and T/R ($S_{42}^{TR\_24GHz}$, $S_{21}^{TR\_60GHz}$) switches are 3, 9.4 dB and 3, 8.8 dB at 24 and 60 GHz, respectively. It is worth to note that these switches incur no additional loss in the concurrent operating mode as compared to the separate individually operating modes, which validates the concurrent design technique and dictates how well it was executed. The dual-band 3-dB bandwidths of the SPDT and T/R switches are 14.6–30.4 GHz, 48–62.4 GHz and 14.6–30.3 GHz, 48.4–64.8 GHz, respectively. The measured input ($S_{11}^{SPDT\_24GHz\_60GHz}$), output ($S_{33}^{SPDT\_24GHz}$, $S_{22}^{SPDT\_60GHz}$) return losses of the SPDT switch under on-state are 34, 35 dB at 24 GHz and 12, 6.8 dB at 60 GHz, respectively. The measured input ($S_{11}^{TR\_60GHz}$, $S_{22}^{TR\_24GHz}$), output ($S_{22}^{TR\_60GHz}$, $S_{44}^{TR\_24GHz}$) of the T/R switches under on-state are 30, 36 dB at 24 GHz and 11, 7.8 dB at 60 GHz, respectively. From the results ($S_{11}^{SPDT\_24GHz\_60GHz}$ and $S_{22}^{TR\_24GHz\_In}$, $S_{22}^{TR\_60GHz\_Out}$) of the SPDT and T/R switches in Figs. 2.34(e) and (f), it is confirmed that the SPDT and T/R switches have the 24/60-GHz concurrent characteristics. The measured isolations between the output ports of the SPDT (S_{32}^{SPDT}) and the TX and RX ports of the T/R (S_{41}^{TR}) switches are 49, 50 dB at 24 GHz and 50, 57 dB at 60 GHz, respectively. All the results show that the SPDT and T/R switches have similar S-parameter performances as expected.

Figs. 2.35(a) and (b) show the measured output power and insertion loss versus input power of the SPDT and T/R switches with one tone at 24 GHz and 60 GHz, and

two tones at 24 and 60 GHz, respectively. For the single-band 24-GHz operation, the measured input (IP_{1dB}), output (OP_{1dB}) 1-dB power compression points of the SPDT and T/R switches are 20.6, 15.5 dBm and 20.6, 16 dBm at 24 GHz, respectively. For the single-band 60-GHz operation, the measured IP_{1dB}, OP_{1dB} of the SPDT and T/R switches are 16.4, 6.7 dBm and 16.4, 7.5 dBm at 60 GHz, respectively. For the 24/60-GHz concurrent operation, the measured IP_{1dB}, OP_{1dB} of the SPDT and T/R switches are 15.2, 11.3 dBm and 15.9, 11.4 dBm at 24 GHz, and 12.7, 2.7 dBm and 13, 4.5 dBm at 60 GHz, respectively. The reduction in the P_{1dB} at 60 GHz is mainly due to the increased nonlinear parasitic capacitances of the off-state shunt transistors of the switches. Figs. 2.35(c) and (d) show the measured input IP_3 (IIP_3) and output IP_3 (OIP_3) with two tones spaced 100-MHz apart at 24 and 60 GHz, respectively. At 24 GHz, the measured IIP_3, OIP_3 of the SPDT and T/R switches are 23, 23.2 dBm and 20, 20.2 dBm, respectively. At 60 GHz, they are 22.5, 22.5 dBm and 14.4, 14.5 dBm, respectively. As expected, the SPDT and T/R switches have similar linearity performance from the P_{1dB} and IP_3 measurements.

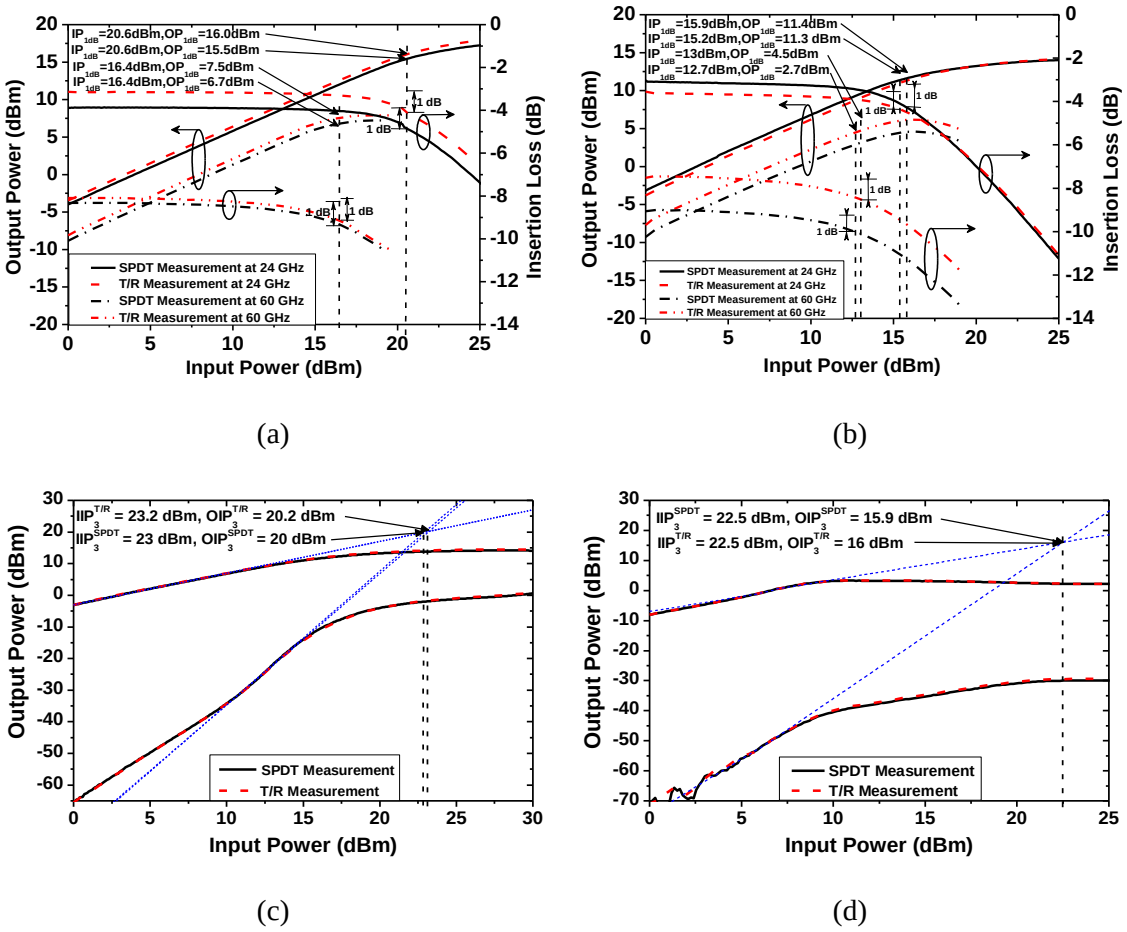


Fig. 2.35. Measured linearity (P_{1dB} and IP_3) of the 24/60-GHz dual-band band-pass filtering SPDT and T/R switches: (a) Measured P_{1dB} at 24 GHz and 60 GHz for single-band operation (b) Measured P_{1dB} at 24 and 60 GHz for concurrent operation (c) Measured IP_3 at 24 GHz, and (d) Measured IP_3 at 60 GHz.

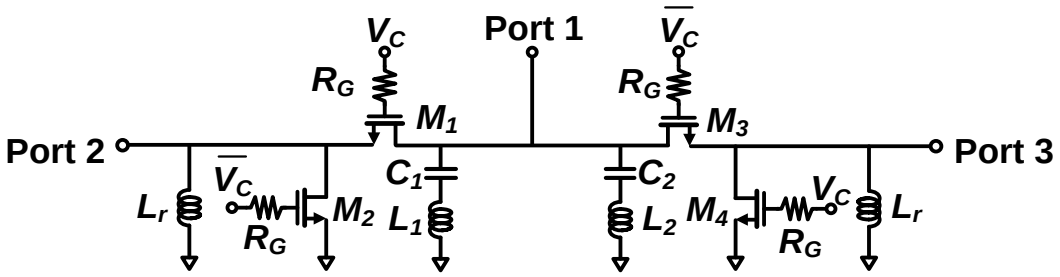
2.5 A Wideband Dual-Bandpass 0.18-µm CMOS SPDT Switch Utilizing Dual-Band Resonator Concept (Design 4)

This section presents a new concurrent dual-band SPDT switch realized in a 0.18-μm SiGe BiCMOS process that operates concurrently in two different wide bands of around 24 and 60 GHz. The SPDT switch is especially configured to operate as a dual-band resonator in the on-state operation for each output path and shows not only switching but also dual-bandpass filtering function. The concurrent dual-wideband switch provides decent insertion losses, good power handling, and compact size, even though it operates with integrated band-pass filtering at both 24 and 60 GHz concurrently.

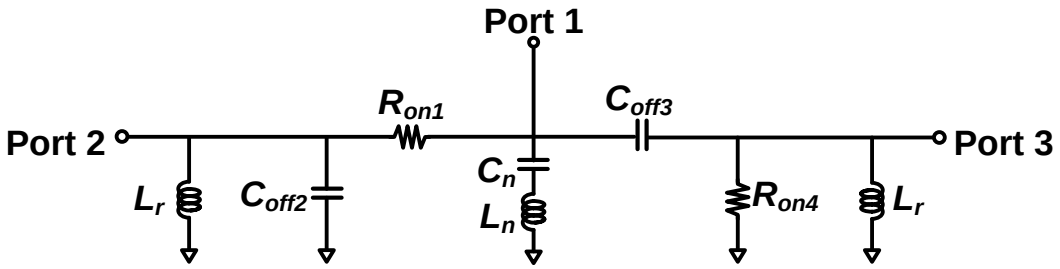
2.5.1 Switch Architecture, Design and Analysis

Fig. 2.36(a) shows the schematic of the concurrent dual-wideband SPDT switch. It is realized by two symmetric switching branches, each consisting of series (M_1 or M_3) and shunt (M_2 or M_4) transistors, shunt inductor L_r, and shunt L_1-C_1 or L_2-C_2. Body-floating technique is applied to all the *n*MOS transistors designed with deep *n*-well for enhanced isolation and reduced transistors' parasitic capacitances [16], [17]. L_1-C_1 and L_2-C_2 are combined into L_n-C_n connected in shunt at Port 1 between the two switching branches, where $C_n = C_1 + C_2$ and $L_n = L_1 // L_2$, as shown in Fig. 2.36(b).

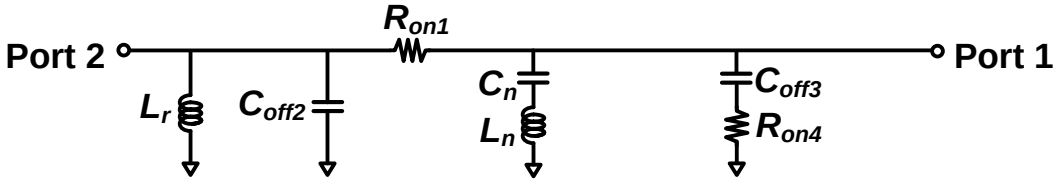
Fig. 2.36(b) shows the equivalent circuit of the concurrent dual-wideband SPDT switch when V_c and $\overline{V_c}$ are biased at 1.8 and 0 V, respectively, where R_{on1} and R_{on4} are the on-resistance representing M_1 and M_4 under on-state, respectively, and C_{off2} and C_{off3}



(a)



(b)



(c)

Fig. 2.36. Concurrent dual-wideband SPDT switch: (a) schematic, (b) equivalent circuit when V_c = 1.8 V and $\overline{V_c}$ = 0 V, and (c) simplified network between Ports 1 and 2.

are the off-state capacitances of M_2 and M_3, respectively. In this operation, ports 2 and 3 are on and off, respectively.

Fig. 2.36(c) shows a simplified network between Ports 1 and 2 transformed from the three-port network in Fig. 2.36(b). Fig. 2.36(c) is approximately equivalent to a dual-band resonator operating at two distinctive frequencies. To simplify the calculation of

the values of the elements, the on-resistances R_{on}'s are neglected, and C_n, L_n, total off-state capacitance $C_{offT} = C_{off2} + C_{off3}$ and L_r can be calculated as [26]

$$C_n = 2\Delta_s / Z_0 \omega_s \tag{2.76}$$

$$L_n = 1/\omega_s^2 C_n \tag{2.77}$$

$$\begin{aligned} C_{offT} &= C_{off\,2} + C_{off\,3} \\ &= \frac{1}{\left[\omega_{c1}^2 + \omega_{c2}^2 - \omega_s^2 - \frac{\left(\omega_{c1}^2 + \omega_{c2}^2\right)^2 - \left(\omega_{c2}^2 - \omega_{c1}^2\right)^2}{4\omega_s^2}\right] L_n} \end{aligned} \tag{2.78}$$

$$L_r = \frac{1}{\left[\omega_{c1}^2 + \omega_{c2}^2 - \omega_s^2 - \frac{1}{L_n C_{offT}}\right] C_{offT}} \tag{2.79}$$

where Z_0 is the terminating impedance, ω_s is the stop-band center frequency, Δ_s is the stop-band fractional bandwidth, and ω_{c1} and ω_{c2} are the 1st and 2nd pass-band center frequencies, respectively.

From (2.76)–(2.79), with Z_0 = 50 Ω, ω_s = 42 GHz, Δ_s = 0.6, ω_{c1} = 24 GHz, and ω_{c2} = 60 GHz, C_n = 92 *f*F, L_n = 153 *p*H, C_{offT} = 120 *f*F and L_r = 170 *p*H. With the calculated C_{offT}, the total width of transistors M_2 and M_3 can be obtained as 136 μm. When V_c = 0 V and $\overline{V_c}$ = 1.8 V, C_{offT} is obtained as $C_{off1} + C_{off4}$ from the off-state transistors M_1 and M_4. Since C_{offT} has the same capacitance in the two bias conditions, it can be seen that the total width of M_2 and M_3 is the same as that of M_1 and M_4. Furthermore, due to the symmetrical structures between ports 1-2 and ports 1-3, the widths of the series transistors M_1 and M_3 are the same as well as those of the shunt transistors M_2 and M_4.

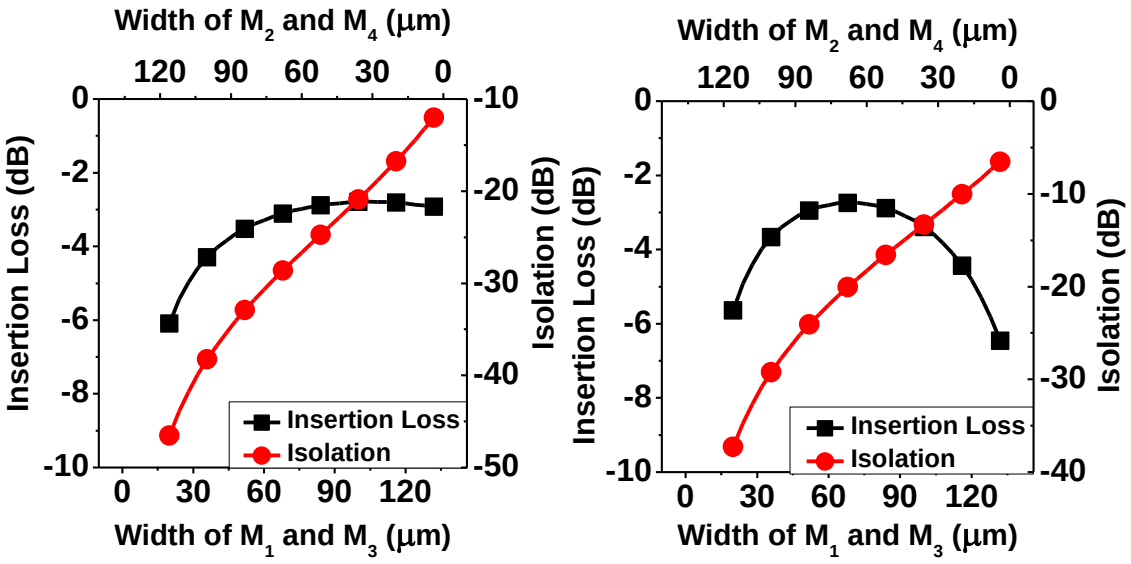


Fig. 2.37 Simulated insertion loss and isolation with respect to the width of M_1 and M_3 (or M_2 and M_4) at 24 GHz (a) and 60 GHz (b).

Fig. 2.37 presents the trade-off between the insertion loss (IL) and isolation (ISO) at 24 and 60 GHz with respect to the widths of the transistors (M_1, M_3 and M_2, M_4). From Figs. 2.37(a) and (b), the widths of M_1, M_3 and M_2, M_4 for optimal IL and ISO at 24 and 60 GHz are chosen as 64 and 72 μm, respectively. Using these widths, the off-capacitances ($C_{off1} = C_{off3}$ and $C_{off2} = C_{off4}$) are found to be around 55 and 65 fF at 24 and 60 G Hz, respectively, and the on-resistances ($R_{on1} = R_{on3}$ and $R_{on2} = R_{on4}$) are around 9.8 and 8.8 Ω at 24 and 60 GHz, respectively. The simulated ILs of the switch are 3.2 and 2.8 dB at 24 and 60 GHz, and the simulated ISOs of the switch are 30 and 21 dB at 24 and 60 GHz, respectively. All the parameters' values are listed in Table 2.4.

The concurrent dual-wideband SPDT switch was fabricated using a TowerJazz

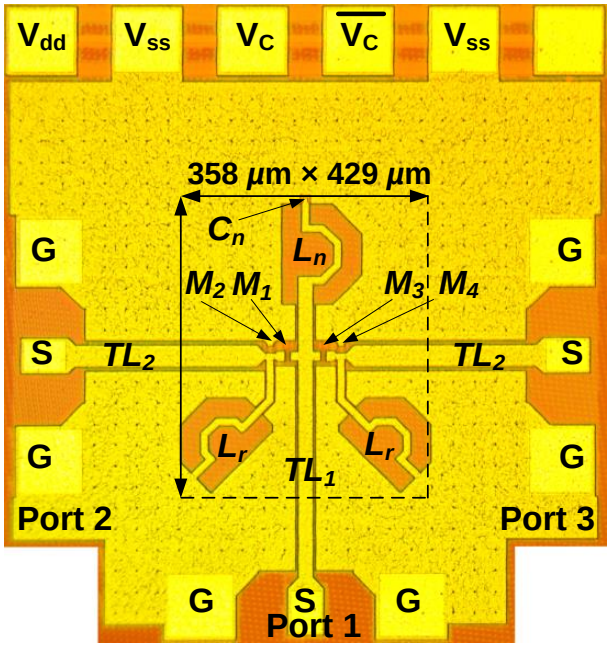


Fig. 2.38 Microphotograph of the fabricated concurrent dual-wideband SPDT switch. Port numbers correspond the numbers in Fig. 2.36(a).

Table 2.4.
Dual-Band Band-Pass Filtering SPDT switch's Parameters

M_1, M_3	0.18 μm / 64 μm	M_2, M_4	0.18 μm / 72 μm
C_n	92 *f*F	L_n	153 *p*H
L_r	170 *p*H	R_G	10 kΩ
C_{off1} , C_{off3}	55 *f*F	C_{off2} , C_{off4}	65 *f*F
R_{on1} , R_{on3}	~ 9.8 Ω	R_{on2} , R_{on4}	~ 8.8 Ω

0.18-μm SiGe BiCMOS process [30]. Fig. 2.38 shows a microphotograph of the fabricated SPDT switch. The core area occupies 358 μm × 429 μm of the chip space, and the entire chip size including all the test pads is 850 μm × 907 μm. In the photograph shown in Fig. 2.38, an extra 50-Ω transmission line (TL_1, TL_2) is added to every port to avoid the collision between the RF ports.

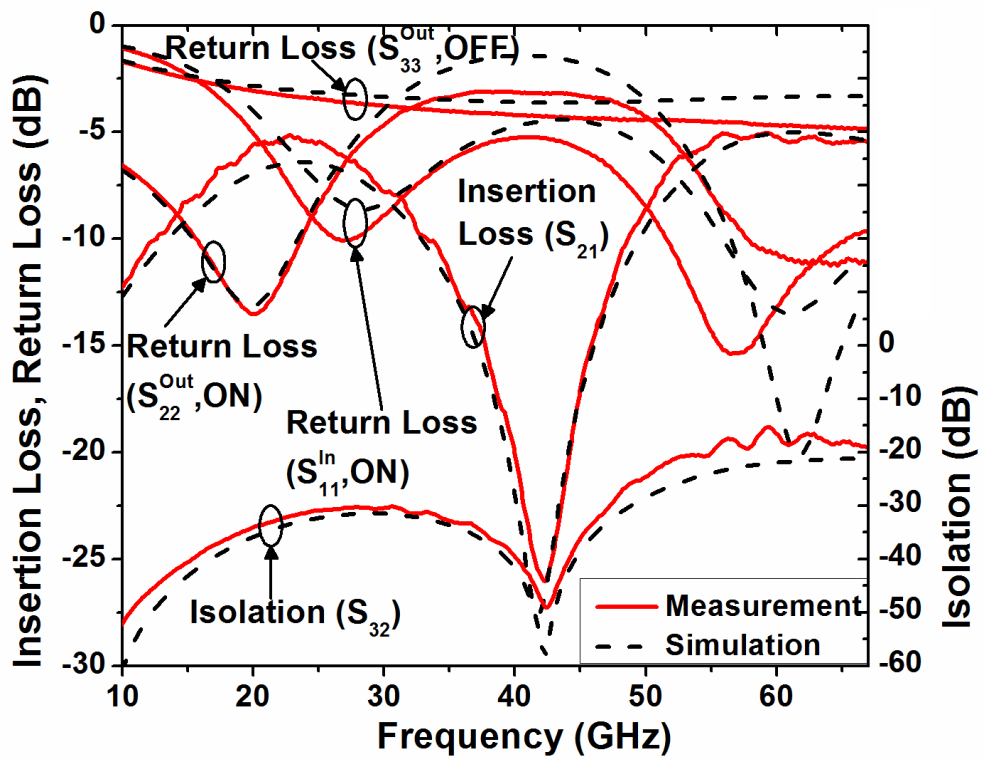


Fig. 2.39. Measured and post-layout simulated results of the concurrent dual-wideband SPDT switch.

2.5.2 Simulation and Measurement Results

Fig. 2.39 shows the measured and post-layout simulated insertion loss, return losses, and isolation of the concurrent dual-wideband SPDT switch, which show good agreement between them. Due to the symmetrical structure of the switch, the results of the on-state ports 2 and 3 are the same. The measured insertion losses (S_{21}) are 5.4 and 5.2 dB at 24 and 60 GHz, respectively. The measured input (S_{11}) and output (S_{22}) return losses are 9.5 and 8.5 dB at 24 GHz, and 10.6 and 13.2 dB at 60 GHz, respectively. The isolation measured between ports 2 and 3 is 31.4 and 16.5 dB at 24 and 60 GHz,

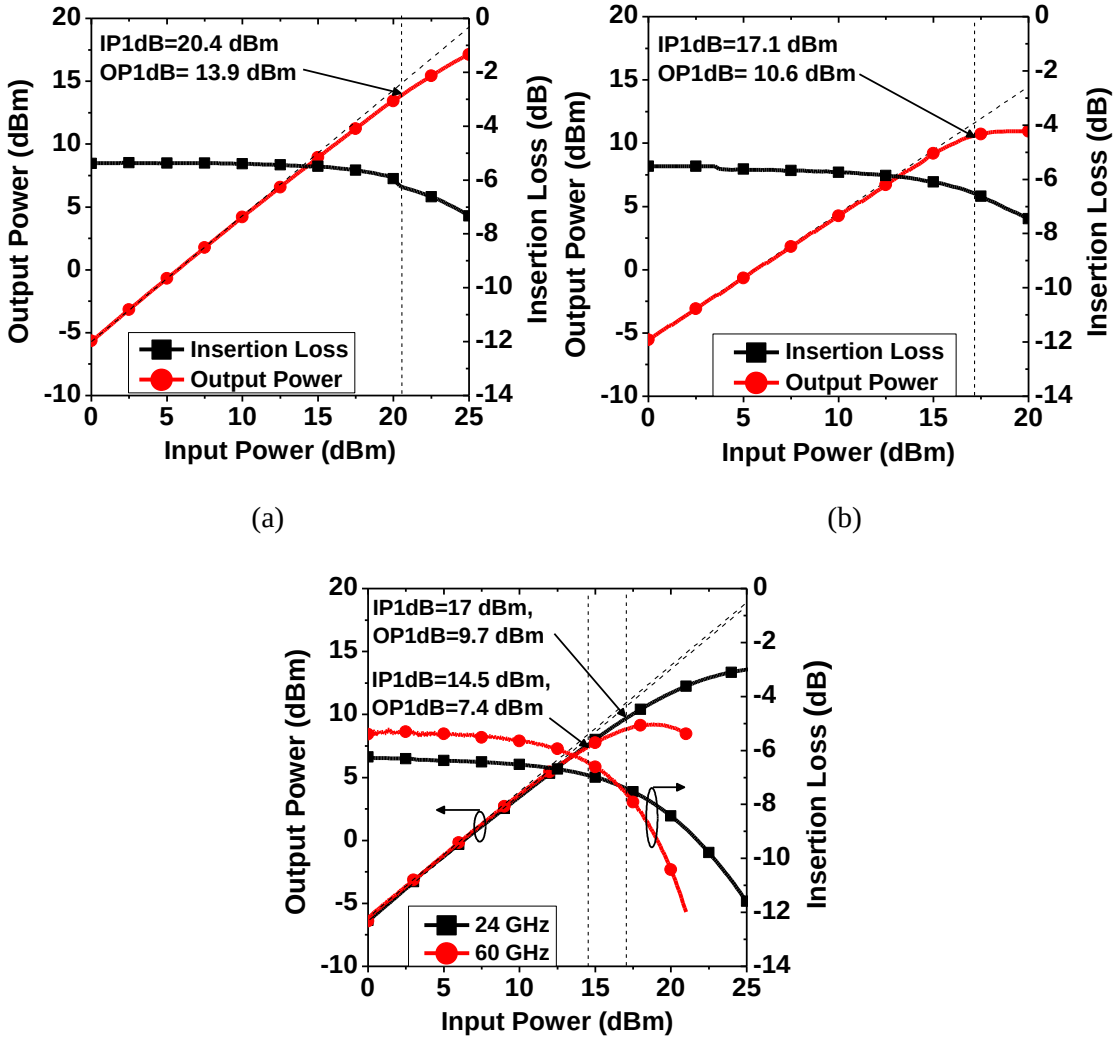
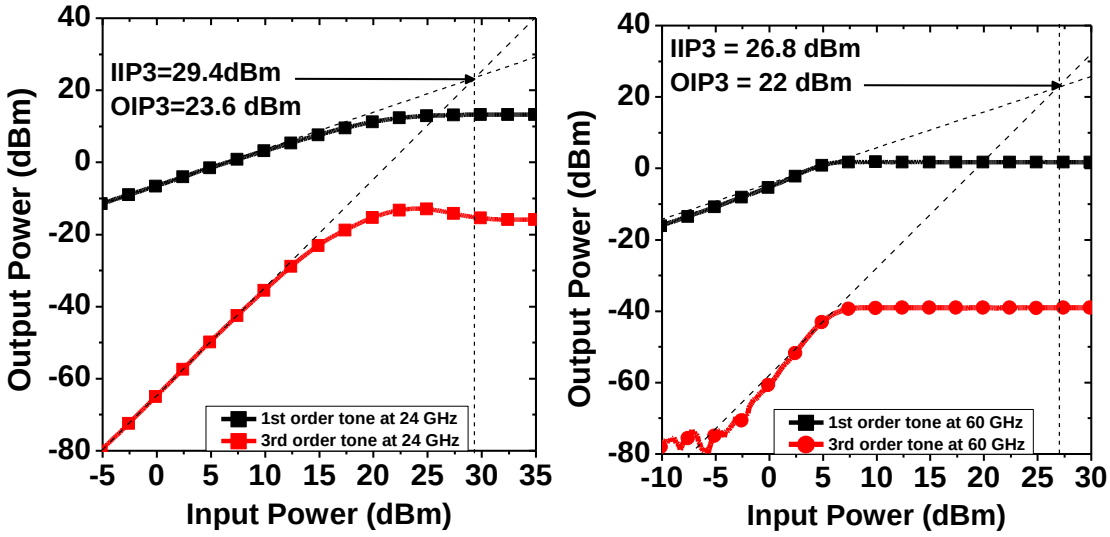


Fig. 2.40. Measured P_{1dB} of the concurrent dual-wideband SPDT switch with 24-GHz single-tone input (a), 60-GHz single-tone input (b), and 24-/60-GHz concurrent dual-tone input (c).

respectively. The peak stop-band rejection is 26 dB at 42.3 GHz.

Fig. 2.40 shows the measured output power and insertion loss versus input power of the concurrent dual-wideband SPDT switch. In the case of the 24-GHz single-tone input shown in Fig. 2.40(a), the measured input (IP_{1dB}) and output (OP_{1dB}) 1-dB



(a) (b)

Fig. 2.41. Measured IP_3 for single-band modes at 24 GHz (a) and 60 GHz (b).

compression points are 20.4 and 13.9 dBm, respectively. For the single tone 60-GHz input, the IP_{1dB} and OP_{1dB} are 17.1 and 10.6 dBm, respectively, as shown in Fig. 2.40(b). When the concurrent dual-tone (24-/60-GHz) input is injected, the measured IP_{1dB} and OP_{1dB} are 17 and 9.7 dBm at 24 GHz, and 14.5 and 7.4 dBm at 60 GHz, respectively, as seen in Fig. 2.40(c).

Fig. 2.41 shows the measured third-order intercept points (IP_3) for single-band modes with the two tones spaced 100 MHz apart. At 24 GHz, the measured input IP_3 (IIP_3) and output IP_3 (OIP_3) are 29.4 and 23.6 dBm, respectively, as shown in Fig. 2.41(a). At 60 GHz, as seen in Fig. 2.41(b), the measured IIP_3 and OIP_3 are 26.8 and 22 dBm, respectively.

2.6 Summary of the Developed Switches

In the Chapter II, the four switches (**Design 1, 2, 3 and 4**) have been proposed. Table 2.5 and 2.6.2 summarize the measured performances of the proposed four switches with those the published 24-, 40- and 60-GHz single-band [22], [31]–[37] and 24.5/35-

Table 2.5
Performance Summary of the Developed Dual-Band SPDT and T/R Switches

	Design 1		**Design 2**		**Design 3**						**Design 4**	
Process	CMOS on 0.18-μm BiCMOS											
Switching Function	TR		TX		SPDT			TR			SPDT /TR	
	TX	RX	TX	X								
Operating Freq (GHz)	Dual		Dual		Single		Dual	Single		Dual	Dual	
	40/60	40/60	24/60	24/60	24	60	24/60	24	60	24/60	24	60
3-dB BW (GHz)	35.5–44.2 /56.4–63.7	35.1–43.7 /56.3–63	17.2–27.3 /52.5–66.5		14.7–30.3	48.5–64.3	14.6–30.4 /48–62.3	14.6–30.3	46.8–62.8	14.6–30.3 /48.4–64.8	-	
IL (dB)	10 /12.7	8.9 /12.5	>6.7 />8.5	>4.5 />5	3	9.4	3 /9.4	2.9	8.7	3 /8.8	5.4	5.2
ISO (dB)	57 /51	56 /51	>18.2 />20.8	>16 />18.3	56	43	49 /50	53	43	50 /57	31.4	16.5
ISO-IL (dB)	47 /38.3	47.1 /38.5	>11.5 />12.3	>11.5 />13.3	53	31.6	46 /40.6	50.1	32.3	47 /48.2	26	11.3
Stop-Band Rej (dB)	33 at 51GHz	38 at 52GHz	> 40 (36.2–40.8 GHz)	> 40 (35.8–41.3 GHz)	23 at 38 GHz			21 at 39 GHz			26 at 42.3GHz	
OP1dB (dBm)	11.8 (40GHz input) 1.8 (60GHz input) 6.4 at 40GHz, 0 at 60 GHz (40/60GHz inputs)		15.4 (24GHz input) 9.1 (60GHz input) 11.3 at 24GHz 7.8 at 60GHz (24/60-GHz inputs)		15.5	6.7	11.4 /2.7	16	7.5	11.3 /4.5	13.9 (24GHz input) 10.6 (60GHz input) 9.7 at 24GHz, 7.4 at 60GHz (24/60-GHz inputs)	
IIP3 (dBm)	-		31.5 at 24 GHz 27.9 at 60 GHz	-	23	22.5	-	23.2	22.5	-	29.4	26.8
Circuit Function	**Switching and Filtering**											
Operation Mode	TX/RX		TX/RX		**<u>Multiple Single Modes:</u>** 24GHz TX/24GHz RX; 60GHz TX/60GHz RX **<u>Multiple Concurrent Modes:</u>** 24GHz TX/RX; 60GHz TX/RX; 24GHz TX/60GHz RX; 24GHz RX/60GHz TX; 24GHz TX/60GHz TX; 24 GHz RX/60GHz RX						TX/RX	
Size*	1840 μm × 860 μm		1671 μm × 692 μm		760 μm × 780 μm			1480 μm × 520 μm			358 μm × 429 μm	

*Estimated size not including the pads.

Table 2.6
Performance Summary of the Existing Single-Band 24-, 40- and 60-GHz, and Dual-Band 24.5/35 GHz Switches

Ref.	[31]	[32]	[33]	[34]	[35]	[36]	[37]	[22]	[29]
Process	0.13-μm CMOS	0.13-μm CMOS	0.13-μm CMOS	0.13-μm CMOS	0.18-μm CMOS	90-nm CMOS	0.18-μm CMOS	90-nm CMOS	0.18-μm CMOS
Switching Function	SPDT /TR	SPDT /TR	SPDT	SPDT /SP4T	SPDT /TR	SPDT /TR	SPDT	SPDT	T/R/C (8 ports)
Freq (GHz)	40	60	60	60	24	24	60	60	24.5 /35
3-dB BW (GHz)	-	-	30–76	50–70	-	-	45–64	-	24–28 /31–39
IL (dB)	4.4(TX) 2.7(RX)	5	<2	<2.5 /<2.8	6.0	3.4(TX) 3.5(RX)	3.2–3.6	1.6	>9.2/>4.9(TX) >9.4/>9.1(RX)
ISO (dB)	14(TX) 26(RX)	25	>21.1	>30 />20	32.8(RX) 25.5(TX)	22(TX) 16(RX)	>20	>25	>55/>60(TX) >55/>45(RX)
ISO-IL (dB)	9.6(TX) 23.3(RX)	26.4	>19.1	>27.5 />17.2	26.8(RX) 19.5(TX)	18.6(TX 12.5(RX)	>16.4	>23.4	>45.8 />55.1(TX) >45.6 />35.9(RX)
Stop-Band Rej. (dB)	-	-	-	-	-	-	6.5at35 GHz	-	>50 at 30 GHz
OP1dB (dBm)	8.4(TX) 7.8(RX)	-1.9	10.8	9.5–10.5	14.5	24.2	>16.4	10.9	1 at 24.5GHz /4 at 35GHz
IIP3 (dBm)	-	-	-	-	32.6	-	-	-	23.3 at 24.5GHz /21.7 at 35GHz
Circuit Function	Switch-ing	Switch-ing	Switchin g	Switch-ing	Switch-ing	Switch-ing	Filter-ing Switch-ing	Switch-ing	Filtering Switching
Operation Mode	TX/RX	TX/RX	TX/RX	-	TX/RX	TX/RX	-	-	TX/RX/CAL
Size*	800 μm × 500 μm	680 μm × 325 μm	222 μm × 90 μm	390 μm × 320 μm /590 μm × 450 μm	670 μm × 610 μm	-	270 μm × 100 μm	500 μm × 550 μm	-

*Estimated size not including the pads.

GHz dual-band switches [29].

It is noted that there has been no work reported on 40/60-GHz and 24/60-GHz concurrent dual-band T/R switches with dual-bandpass filtering, making it inconclusive in the performance comparison of the developed dual-bandpass T/R switches. In the proposed designs 1, 2 and 3 having 5 ports to accommodate concurrent dual-band and dual-polarization with an integrated dual-band filtering function, the T/R switches have

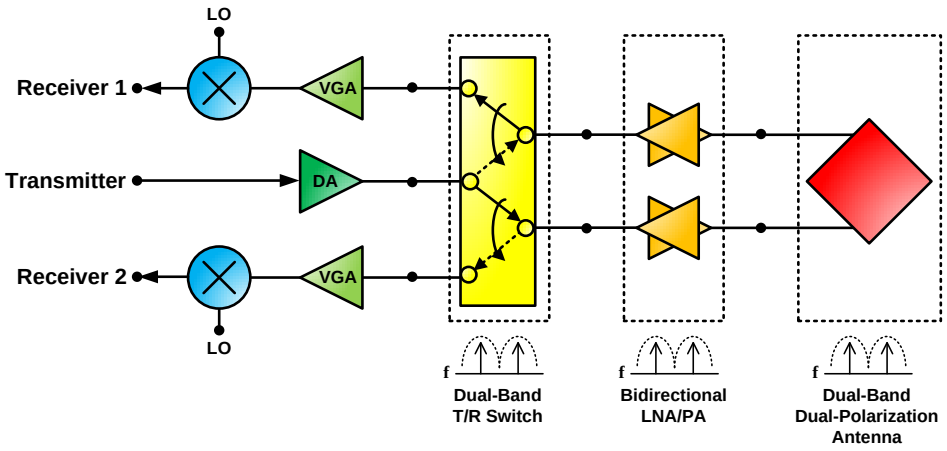


Fig. 2.42. Block diagram of the possible dual-band front-end module.

limited design freedom in choosing proper switch's constituent elements, inevitably leading to poorer insertion loss (IL) and isolation (ISO) than those of single-band switches having no filtering and single polarization at 24, 40 or 60 GHz.

And also, it is noted that the insertion losses at 24, 40 and 60 GHz are high even though the return losses are reasonable. The high insertion loss is due to the two reasons. One is the low *Q* of the shunt off-state transistors, which were selected to provide the compromise between insertion loss and isolation for both 24/60 and 40/60 GHz simultaneous operations. Another is due to the switch architecture, which provides both concurrent dual-band operation and concurrent switching and filtering functions in a single circuit. The high insertion loss is unfortunately inevitable and is the price to pay for designing a multi-function (switching and filtering) and multi-band (concurrent operation in two separate bands) component, especially at such high frequencies as 24, 40 and 60 GHz. This seemed acceptable in view of system implementation advantages with multi-function over multi-band for the reduced size and cost using integrated

circuits, especially expensive silicon-based RFICs. Nevertheless, the insertion loss problem at 24, 40 and 60 GHz could be mitigated with the proposed dual-band front-end module described in Fig. 2.42, which consists of the T/R switch, two bidirectional low-noise amplifiers/power amplifiers (LNA/PA), and an antenna. By employing dual-band bidirectional amplifiers similar to that presented in [38], which operate as PA and LNA in the transmitting and receiving modes, respectively, between the T/R switch and the dual-band dual-polarization antenna, enabling high-power and low-noise signals to be transmitted and received in these modes, respectively, the high insertion loss of the T/R switch can be alleviated.

Design 1: The designed dual-band T/R switch with band-pass filtering has higher insertion loss than the single-band switches without band-pass filtering in [31]–[34] due to the inclusion of many lumped elements for J-inverters and resonators to embed the dual-band filtering function in the switch as explained earlier. However, the designed T/R switch supports the switching operations at the two distinct 40 and 60-GHz pass-bands concurrently with the stop-band rejection of 30 and 22 dB at 51 GHz for the transmitting and receiving modes, respectively. Also, the isolations at 40 and 60 GHz are all higher than 50 dB both in the transmitting and receiving modes, which are the highest among the reported single-band switches operating at 40 or 60 GHz. Moreover, to the best of my knowledge, the developed switch is the first reported concurrent 40 and 60 GHz band-pass filtering T/R switch.

The developed switch has multi-port, with each port handling dual-band signal concurrently, and high isolation between ports, making it attractive for use in dual-band

RF systems demanding multi-port and dual-band concurrent operation with band-pass filtering and high isolation. The successful development of this millimetre-wave dual-band band-pass filtering SPDT and T/R switches demonstrates potentials for designing other millimetre-wave multi-pole multi-throw switches capable of filtering functions for silicon-based multi-band RF systems.

Design 2: The developed T/R switch has multi-port, with each port being capable of handling dual bands concurrently, making it attractive for use in multi-band RF systems demanding multi-port and multi-band concurrent operation with band-pass filtering function.

Compared to [29] operating at 24.5/35 GHz, the IL of the developed T/R switch is competitive. Compared to the combined ILs of a dual-band 24/60GHz band-pass filter [39] and single-band switches [33]–[35], the dual-band T/R switch has lower and higher insertion loss at 24 and 60 GHz, respectively. However, this comparison is not conclusive as the T/R switch operates concurrently in dual bands and dual polarizations with integrated filters while [33], [34] operate only in single band and single polarization without filtering. The high insertion loss can be overcome with a front-end module similar to that in [29]. Moreover, the developed T/R switch has very high stop-band rejection (higher than 40 dB) over 36.2–40.8 GHz, as compared to that of [37], and good power handling capabilities.

Design 3: Compared to the switches in [35], [36] and [22], [33] which only operate over a single band, either 24 or 60 GHz, and do not have band-pass filtering functions, the dual-band band-pass filtering SPDT and T/R switches can operate in

single-band mode at 24 or 60 GHz as well as concurrent dual-band modes at 24 and 60 GHz. The dual-band band-pass filtering T/R switch's operation is more versatile and can be used for various individual and concurrent switching functions. It can operate in single-band transmitting or receiving mode at 24 and 60 GHz and concurrent dual-band transmission or reception at 24 and 60 GHz. It can work completely in concurrent modes including single-band concurrent transmission and reception at 24 or 60 GHz and dual-band concurrent transmission and reception at 24 and 60 GHz. The developed T/R switch makes it possible simultaneous transmission and reception with a single antenna, which is desirable in RF systems yet not feasible with conventional T/R switches. The SPDT and T/R switches can also function as diplexers with switching functions. They also have high isolation between the output ports due to the rejection of the off-state switch as well as the suppression provided by the inherent filtering function. The unique features of the dual-band band-pass filtering SPDT and T/R switches make them attractive for multi-band RF systems requiring single- and multi-band concurrent operations with band-pass filtering.

Design 4: The concurrent dual-wideband SPDT switch has a distinctive dual-bandpass filtering function with good stop-band rejection (26 dB) at 42.3 GHz, decent insertion losses at 24 and 60 GHz, and good power handling capability. Moreover, while its size is similar to that of other single-band 60-GHz SPDT switches, the concurrent dual-wideband SPDT switch can operate in an even lower frequency band (24 GHz).

CHAPTER III

MILLIMETER-WAVE CONCURRENT DUAL-BAND LOW-NOISE AMPLIFIER

In this chapter, a fully integrated concurrent dual-band low noise amplifier (LNA) using 0.18-μm SiGe BiCMOS process has been proposed, which utilizes a dual-band LC circuit. The LNA is based on a two-stage cascode topology with inductive degeneration to achieve a high forward gain, reverse isolation, and simultaneous noise and input matching. The dual-band LC circuit has a quarter-wavelength characteristic at two different frequencies and, it shows a dual pass-band and single stop-band characteristics when it is connected to the ground in parallel. Due to the stop-band signal canceled out through the dual-band LC circuit connected to the cascode nodes of 1st and 2nd stages in the LNA, the LNA presents high stop-band rejection. Furthermore, the dual-band LC circuit reduces the gain imbalances at 24 and 60 GHz due to its inherent low-pass response. The proposed LNA shows the simulated gains of 20.7 and 18.8 dB, noise figure (NF) of 4.25 and 6.6 dB at 24 and 60 GHz, and 3-dB bandwidths of 21–29 GHz and 59–65 GHz, respectively. The simulated input P_{1dB} and IP_3 are -21.5 and -11.7 dBm at 24 GHz and -19.5 and -9.3 dBm at 60 GHz, respectively. The total chip size is 1150 μm × 580 μm including RF pads.

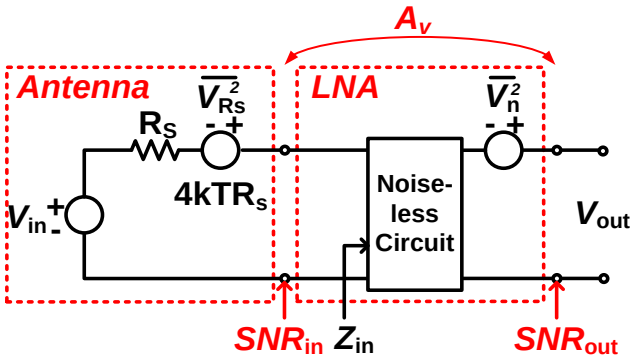


Fig. 3.1. Block diagram of the LNA for simple NF calculation.

3.1 Fundamentals of Low-Noise Amplifier (LNA)

A low-noise amplifier (LNA) is essential and the first active component in a receiver chain; and it should amplify small wanted signals only without amplifying noise. For the LNA design, noise figure (NF), band selection, gain, linearity and stability should be considered together.

3.1.1 Noise Figure (NF) of the LNA

Firstly, the LNA is an active component that can generate noise. The noise sources of the LNA are normally passive elements' loss and transistor's channel and gate thermal noise, flicker (1/f) noise, shot noise and etc. [18]. The noise of the LNA plays an important role in the overall NF of the receiver, which can control the receiver's sensitivity and output Signal-to-Noise (SNR) [40]. Fig. 3.1 shows a block diagram of the LNA for a simple NF calculation. In Fig. 3.1, the source and the LNA are equivalent to the noise models of the antenna and LNA, respectively. The NF is derived as the input to output SNRs as

$$NF = \frac{SNR_{in}}{SNR_{out}} \tag{3.1}$$

In (3.1), SNR_{in} can be calculated as

$$SNR_{in} = \frac{\left|\frac{Z_{in}}{Z_{in}+R_s}\right|^2 V_{in}^2}{\left|\frac{Z_{in}}{Z_{in}+R_s}\right|^2 \overline{V_{R_s}^2}} = \frac{|\alpha|^2 V_{in}^2}{|\alpha|^2 \overline{V_{R_s}^2}} \tag{3.2}$$

, where $\overline{V_{R_s}^2}$ is antenna thermal noise (= $4kTR_s$) with source resistor R_s, k is Boltzmann's constant, T is absolute temperature in kelvins degree, Z_{in} is input impedance of the LNA, V_{in} is voltage source and $\alpha = \frac{Z_{in}}{Z_{in}+R_s}$.

SNR_{out} can be calculated as

$$SNR_{out} = \frac{A_v^2 \alpha^2 V_{in}^2}{A_v^2 \alpha^2 \overline{V_{R_s}^2} + \overline{V_n^2}} \tag{3.3}$$

, where $A_v^2 \alpha^2 V_{in}^2$ is output signal power of the LNA, $A_v^2 \alpha^2 \overline{V_{R_s}^2}$ is the antenna noise amplified by the LNA, and $\overline{V_n^2}$ is the output noise of the LNA, A_v is the LNA gain.

Finally, NF can be obtained as

$$NF = \frac{SNR_{in}}{SNR_{out}} = 1 + \frac{\overline{V_n^2}}{A_v^2 \alpha^2} \cdot \frac{1}{\overline{V_{R_s}^2}} = \frac{1}{4kTR_s} \cdot \frac{\overline{V_{n\_out}^2}}{A_o^2} \tag{3.4}$$

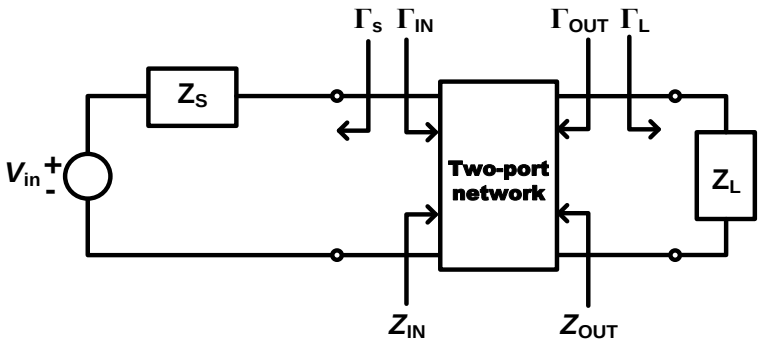


Fig. 3.2. Two-port network [40].

3.1.2 Stability of the LNA

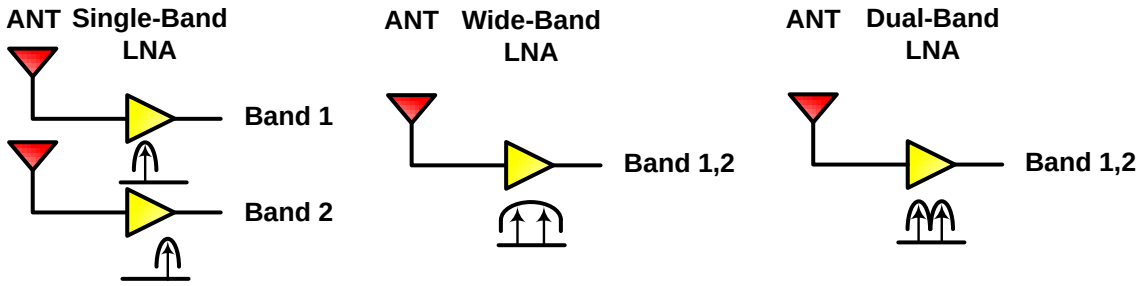
Secondly, the stability of the amplifier is an essential factor because the amplifier may oscillate, and the stability can be obtained from *S*-parameters of the two-port network, the matching networks and the terminations. In a two-port network shown in Fig. 3.2, an oscillation can be generated if a negative resistance is presented at the input or output port [41]. This occurs when $|\Gamma_{IN}|>1$ or $|\Gamma_{OUT}|>1$, which is the same as $|S_{11}|>1$ or $|S_{22}|>1$ for a unilateral transistor.

Therefore, the conditions for an unconditional stability in the amplifier are as follows

$$|\Gamma_s|<1 \text{ and } |\Gamma_L|<1 \tag{3.5}$$

$$|\Gamma_{IN}|=\left|S_{11}+\frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right|<1 \text{ and } |\Gamma_{OUT}|=\left|S_{22}+\frac{S_{12}S_{21}\Gamma_s}{1-S_{11}\Gamma_s}\right|<1 \tag{3.6}$$

By using (3.4) and (3.5), stability circles can be obtained at a certain frequency on Smith chart. For an unconditional stability, the stability circles on Γ_s and Γ_L plane



(a) (b) (c)

Fig. 3.3. Dual-band system consisting of: (a) LNAs operating in each band of interest, (b) wideband LNA operating in bands of interest and (c) LNA operating in dual bands of interest concurrently.

should be located outside of the Smith chart under the condition such as $|S_{22}|<1$ and $|S_{11}|<1$. Other necessary and sufficient conditions for an unconditional stability in the two-port network can be defined as

$$K=\frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}>1 \text{ and } B_1=1+|S_{11}|^2-|S_{22}|^2-|\Delta|^2>0 \tag{3.7}$$

, where $\Delta=S_{11}S_{22}-S_{12}S_{21}$.

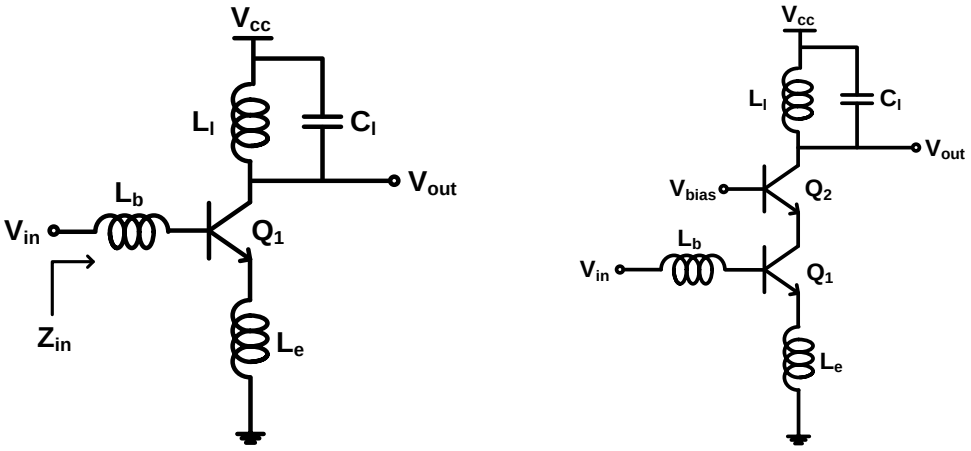
3.1.3 Concurrent Dual-Band LNA

Thirdly, the LNA, which is one of the components in a front-end module, can determine the receiver's operating frequency bands, which could be single- or dual-band. Fig. 3.3 shows a dual-band system configuration consisting of two separate (one wideband and one concurrent) components. In Fig. 3.3(a), the system consists of two independent LNAs operating in each band of interest. However, it can suffer from high

power consumption and large die size, cost, and etc. Using wide-band LNA in Fig. 3.3(b) leads to the amplification of the unwanted blocker together at the wanted frequency bands and the degradation of the receiver's sensitivity. Therefore, more effective implementation approach of the dual-band LNA operating at every desirable band concurrently is shown in Fig. 3.3(c). In order to achieve the dual-band characteristic, generally, a dual-band LC resonator is employed at the input, output, and load of the LNA [40], [42] as well as a variety of techniques for the band selection [43].

3.1.4 Power Handling Capability and Nonlinearity of the Concurrent Dual-Band LNA

Fourthly, in the concurrent dual-band LNA, P_{1dB} and IP_3 in each band are still significant factors. Furthermore, due to the concurrent dual-band characteristic, two more nonlinearity factors need to be considered. One is the cross-band compression and the other one is the cross-band intermodulation [40]. In Fig. 3.3(c), the cross-band compression is a gain compression at Band 1 (or 2), when much larger power signal is injected at Band 2 (or 1), and the cross-band intermodulation is intermodulation generated by two signals in each pass band (Band 1 and 2 in Fig. 3.3(c)) due to the nonlinearity of dual-band LNA. For instance, the n-th order intermodulation signal by two signals in the two pass bands can be located in one of the two pass bands. Therefore, these two nonlinearity factors need to be considered.



(a) (b)

Fig. 3.4. Commonly used single-band BJT LNAs: (a) common-emitter LNA with an inductive degeneration and (b) cascode LNA with an inductive degeneration.

3.1.5 Topologies for the LNA Design

Several different topologies have been proposed for LNA design, and the commonly used common emitter and cascode topologies are shown in Fig. 3.4, which are described in [40], [44].

In typical common-emitter LNA, since an input impedance is imaginary and capacitive, the topology has input matching problem [18]. In order to resolve this problem, the inductive degeneration technique is employed as shown in Fig. 3.4(a), and it generates the real part of the input impedance that is needed to match the LNA input to the preceding switch or antenna [1], [8], and it can provide simultaneous noise and input matching [45].

Input impedance (Z_{in}) in Fig. 3.4(a) is calculated as

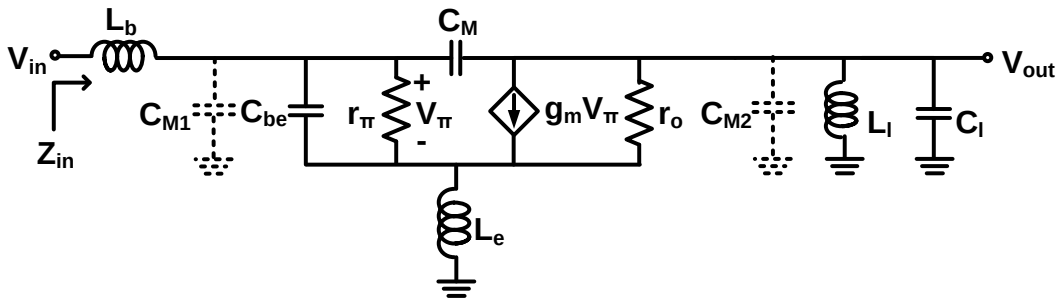


Fig. 3.5. Small-signal model of the common-emitter LNA with inductive degeneration.

$$Z_{in} = j\omega\left(L_b + L_e\right) + \frac{1}{j\omega C_{be}} + \frac{L_e g_{m1}}{C_{be}} \tag{3.8}$$

, where g_{m1} and C_{be} are transconductance and capacitance between the base and emitter of Q_1, respectively.

From (3.8), a resonant frequency (f_c) is obtained as

$$f_c = \frac{1}{2\pi\sqrt{\left(L_b + L_e\right)C_{be}}} \tag{3.9}$$

At f_c, the input impedance becomes purely resistive $\left(\frac{L_e g_{m1}}{C_{be}}\right)$ and can be matched to the source resistance with the proper values of L_e, g_{m1} and C_{be}.

3.2 Challenge for the Dual-Band LNA at Millimeter-Wave Frequencies

Fig. 3.5 shows a small signal model of the common-emitter amplifier with an inductive degeneration at high frequencies. Common-emitter topology suffers from miller effect [44], [20]. The miller effect is generated due to parasitic capacitance (C_{bc}) between base and collector and the capacitor is called as miller capacitor (C_M). It is due

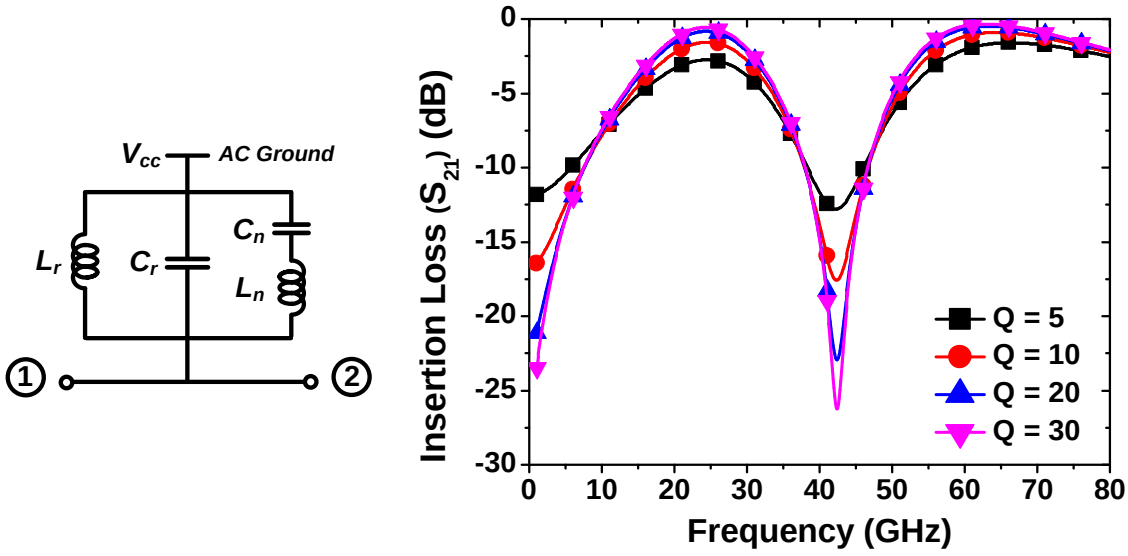
to the feed-back connection between base and collector causes the effect to appear to the amplifier like a large capacitor, and also results in instability. Due to the C_M, additional parasitic capacitors (C_{M1} and C_{M2} in Fig. 3.5) are generated at the input and output of the amplifier, and calculated as

$$C_{M1} = (1-A)C_M \text{ and } C_{M2} = \left(\frac{1-A}{A}\right)C_M \tag{3.10}$$

, where A is gain of the amplifier.

The generated C_{M1} leads to a narrow band input matching and lower resonance frequency. In order to avoid this issue, cascode structure as shown in Fig. 3.4(b) is used to reduce the miller effect on the input matching [46]. Moreover, it features a higher gain and reverse isolation due to the combination of common-emitter and common–base stages compared to a common-emitter topology.

A conventional heterodyne receiver using the wide-band LNA shown in Fig. 3.2(b) has an image signal problem, and an image reject filter is located after the LNA [21]. Thus, the LNA needs a high rejection at image frequency bands or out of bands, and for dual-band LNA, this problem can be solved by locating the stop band of the dual-band LNA at the image frequency band [40]. However, dual-band LNAs employing an integrated passive dual-bandpass filter can suffer from the poor stopband rejection, which mainly depends on the low quality (Q) factor of the inductor in the integrated band-pass filter [43]. Fig. 3.6 shows a conventional dual-band load and its insertion loss with respect to the Q factor of the integrated inductors. As shown in the Fig, 3.2.2(b), a gain balance and a stop-band performance become worse as the Q factor of the inductors



(a) (b)

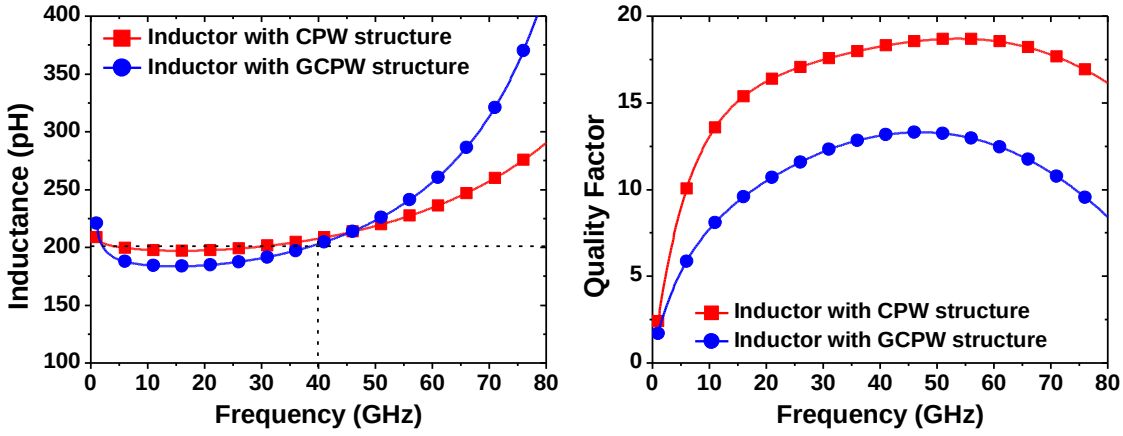
Fig. 3.6. (a) Conventional dual-band load and (b) simulated insertion loss of the conventional dual-band load as the Q factor of the integrated inductors is varied from 5 to 30.

is reduced. Given that Q factor is around 20 from 24 to 60 GHz, it is impossible to obtain a good stopband rejection ratio over 30 dB. In order to overcome this problem, a dual-band LC circuit will be proposed in Sec. 3.3 and it will be applied to the proposed LNA in Sec. 3.4.

For LNA design, integrated passive components and inter-connection lines are frequently used for input, inter-stage and output matching, which can enhance both noise and gain performances of the LNA [46]. To design them, microstrip structure, which is implemented with a top metal as the signal line and bottom metal as the ground plane, is typically utilized, but the short distance (~10 μm) between the signal line and the ground plane can increase parasitic capacitances between them, which can result in loss increment due to increased signals leaked into ground [46], [47]. As frequency increases,

the values of inductor and capacitor for input or output matching and interconnection decrease. It can lead to smaller size of the inductor and capacitor and the closer distance between components. A problem is that the parasitic capacitances are not negligible and relatively large compared to the values of an inductor and capacitor at millimeter-wave frequency. Since the parasitic capacitances may allow more RF signals from the signals path to ground, circuit's performance becomes worse. Furthermore, shortened distance between elements such as inductors and capacitors results in mutual coupling and isolation problems. Thus, the parasitic capacitances should be carefully considered not only in the schematic design but also layout design, and careful EM simulation is required when designing the LNA at millimeter-wave frequencies.

To resolve the parasitic capacitance issue, a coplanar waveguide (CPW) structure is preferred in the layout design. The CPW structure is implemented with one signal line surrounded by adjacent ground planes [46] and can help to enhance isolation due to the ground between elements, and easy integration. The distance between the signal line and ground can be varied [46], and parasitic capacitances can decrease. Grounded (also called shielded) CPW (GCPW) is also utilized due to similar reasons mentioned above. Although the structure may have more isolation by the ground below each element, the structure increases parasitic capacitances between each element and the grounds, and signal leakage and insertion loss increases. Figs. 3.7(a) and (b) show inductances and Q factors of inductors (~200 pH at 40 GHz) designed using CPW and GCPW structures, respectively. For GCPW structure, a self-resonant frequency (SRF) is shifted down due to the increased parasitic capacitance of the inductor, and Fig. 3.7(a) shows that the



(a) (b)

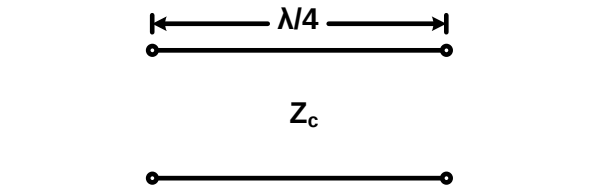
Fig. 3.7. (a) Simulated inductance of and (b) quality factor comparison of inductors with CPW and GCPW structures.

inductance variance is higher compared to the CPW structure. Furthermore, the Q factor is lower than that in the CPW structure due to the increased signal leakage as shown in Fig. 3.7(b). Therefore, the CPW structure is employed in the proposed LNA layout.

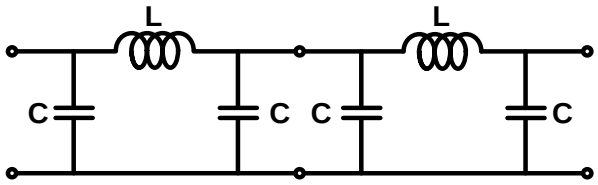
3.3 Dual-Band Quarter-Wavelength LC Circuit

Fig. 3.8 shows the conventional quarter-wavelength transmission line model and the proposed 2nd order pi-type LC equivalent circuit.

By setting the ABCD matrix of the LC equivalent circuit in Fig. 3.8(b) equal to that of a conventional quarter-wavelength transmission line in Fig. 3.8(a) at two desired frequencies (f_1 and f_2), the ABCD matrix of the LC equivalent circuit in Fig. 3.8(b) can be expressed by cascading the sections as



(a)



(b)

Fig. 3.8. (a) Quarter-wave length transmission line and (b) 2nd order equivalent LC circuit.

$$\begin{bmatrix} 1-\omega^2 LC & j\omega L \\ -j\left(\omega^3 LC^2 - 2\omega C\right) & 1-\omega^2 LC \end{bmatrix} \cdot \begin{bmatrix} 1-\omega^2 LC & j\omega L \\ -j\left(\omega^3 LC^2 - 2\omega C\right) & 1-\omega^2 LC \end{bmatrix} = \begin{bmatrix} 0 & \pm jZ_c \\ \pm j\dfrac{1}{Z_c} & 0 \end{bmatrix} \tag{3.11}$$

, where Z_c is characteristic impedance of a conventional quarter-wavelength transmission line.

From the (3.11), further equations can be obtained as

$$\left(1-\omega^2 LC\right)^2 + \omega L\left(\omega^2 LC^2 - 2\omega C\right) = 0 \tag{3.12}$$

$$\left(\omega^2 LC - 1\right) = \pm\frac{1}{\sqrt{2}} \text{ and } LC = \left(\frac{\sqrt{2}+1}{\sqrt{2}}\right)\frac{1}{\omega_2^2} = \left(\frac{\sqrt{2}-1}{\sqrt{2}}\right)\frac{1}{\omega_1^2} \tag{3.13}$$

From (3.13), the relationship between the two frequencies can be obtained as

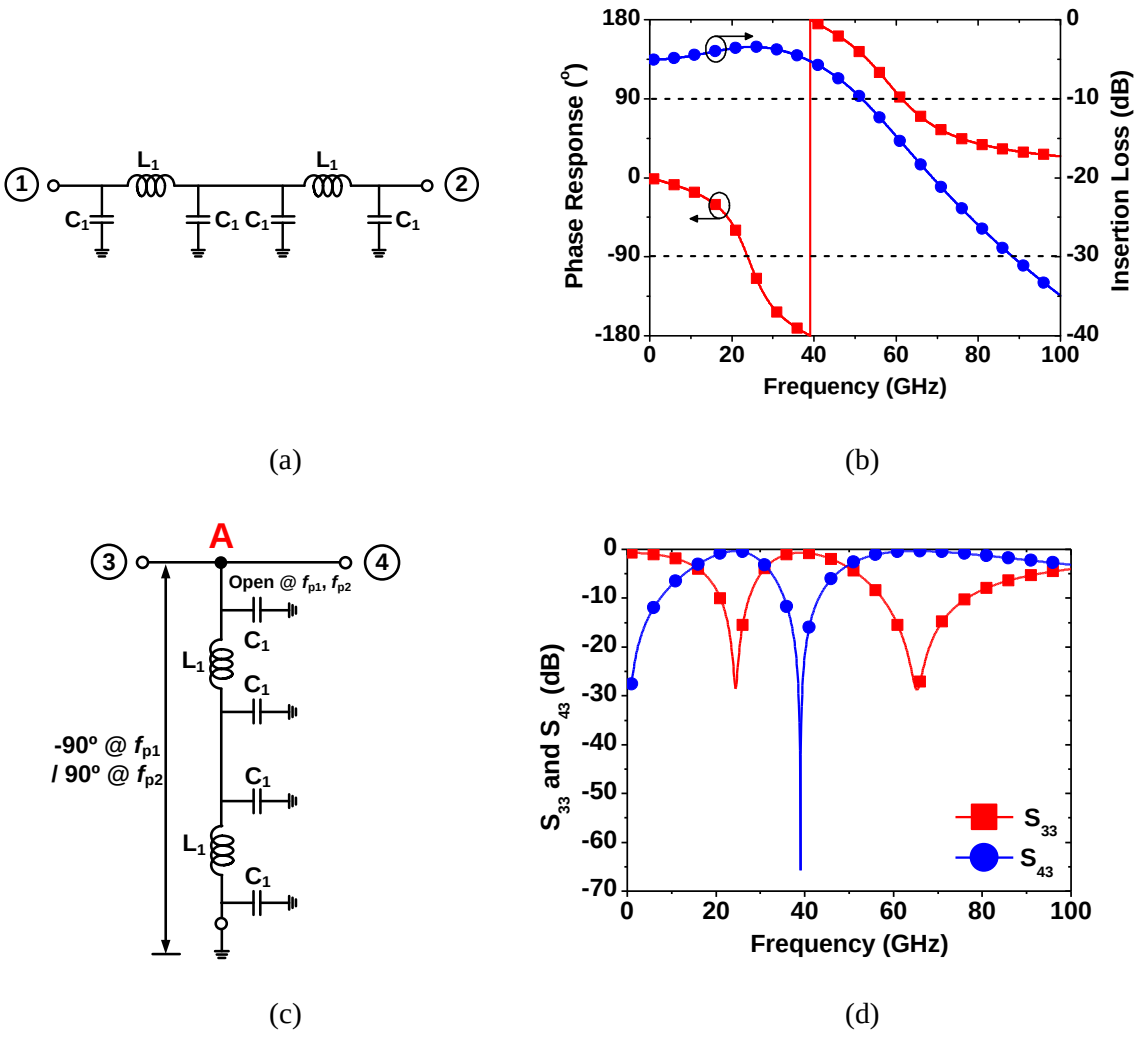


Fig. 3.9. Quarter-wavelength dual-band LC circuit: (a) series LC circuit, (b) simulated phase response and insertion loss of (a), (c) parallel LC circuit, and (d) simulated return loss and insertion loss of (c).

$$\frac{\omega_2}{\omega_1} = 2.41 \tag{3.14}$$

With two frequencies (f_1 (= 24 GHz) and f_2 (= 24 GHz * 2.41 = 57.84 GHz)) and the proper inductance of L as a degree of freedom, capacitance of C can be obtained as

$$C = \left(\frac{\sqrt{2}+1}{\sqrt{2}} \right) \frac{1}{L\omega_2^2} = \left(\frac{\sqrt{2}-1}{\sqrt{2}} \right) \frac{1}{L\omega_1^2} \tag{3.15}$$

And, in order to get the quarter-wavelength characteristic (±90º) at 24 and 60 GHz, the values of L and C are obtained as 85 *p*H and 100 *f*F after some optimizations and tuning of the values of C and L. Fig. 3.9 shows the 2nd order LC circuit and the simulated results of the circuits. Figs. 3.9(a) and (b) show the dual-band LC circuit in series and its phase response. It clearly shows the quarter-wavelength property (±90º) at 24 and 60 GHz and low-pass response. And, Figs. 3.9(c) and (d) show the dual-band LC circuit connected in shunt and its return and insertion losses. Through the LC circuit grounded in shunt, the circuit at node 'A' in Fig. 3.9(c) ideally becomes an open circuit at 24 and 60 GHz. It means that only two frequency signals at f_1 and f_2 pass from port 3 to port 4. Fig. 3.9(d) clearly shows two pass bands and one stop band performances.

3.4 Design of the 24/60-GHz Concurrent Dual-Band LNA

Fig. 3.10 shows the schematic of the proposed 24/60-GHz concurrent dual-band LNA employing the dual-band LC circuit described in Sec. 3.3. The dual-band LNA is based on a two-stage cascode topology to enhance the gain and isolation of the LNA. Transistors (Q_1, Q_2) and (Q_3, Q_4) used in 1st and 2nd stages of the dual-band LNA have two-finger emitter having 0.15-μm width and 5- and 3.5-μm length, respectively. And, they have three-finger base and two-finger collector. Simulated total current consumptions in the 1st and 2nd stages are 6.03 and 4.75 mA, respectively, at a 1.8-V supply voltage. And, the simulated transconductances are g_{m1} = 210.7 mS, g_{m2} = 210.4

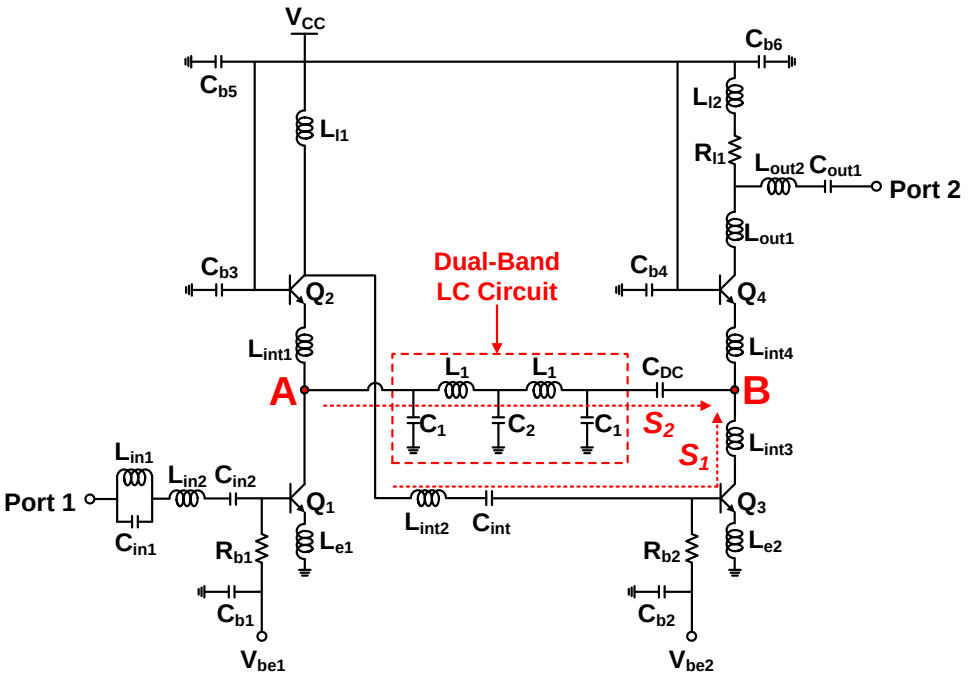


Fig. 3.10. Schematic of the 24/60-GHz concurrent dual-band LNA.

Table 3.1
24/60-GHz Concurrent Dual-Band LNA's Parameters Values

Q_1, Q_2	5 μm / 0.13 μm	Q_3, Q_4	3.5 μm / 0.13 μm
L_{in1}	160 pH	C_{in1}	100 fF
L_{in2}	200 pH	C_{in2}	500 fF
L_{int1}, L_{int3}, L_{int4}	20 pH	L_{int2}	350 pH
C_{int}	300 fF	L_{e1}, L_{e2}	35 pH
C_{b1}, C_{b2}, C_{b3}, C_{b4}	2 pF	C_{b5}, C_{b6}	5 pF
L_{l1}, L_{l2}	400 pH	R_{l1}	9 Ω
L_{out1}	80 pH	L_{out2}	200 pH
C_{out1}	90 fF	L_1	85 pH
C_1	100 fF	C_2	370 fF
C_{DC}	1.5 pF	R_{b1}, R_{b2}	2 kΩ
V_{be1}, V_{be2}	0.87 V	V_{CC}	1.8 V

mS, g_{m3} = 4.9 mS and g_{m4} = 164.9 mS, respectively. The load at the first stage consists of L_{l1} and the load at the second stage consists of L_{l2} and R_{l1} to avoid the potential

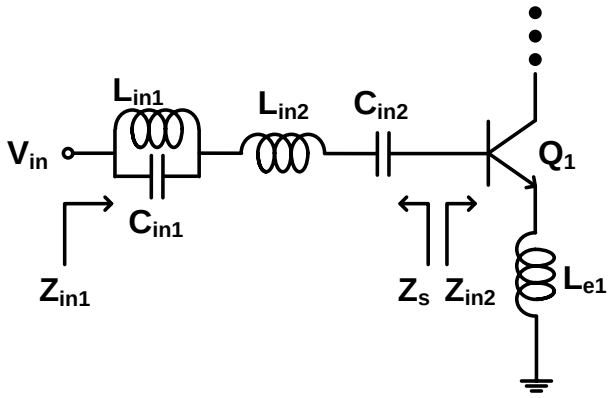


Fig. 3.11. Input matching of the proposed 24/60-GHz concurrent dual-band LNA.

instability and the output matching network consists of L_{out1}, L_{out2} and C_{out1}. Inter-stage matching consists of L_{int1}, L_{int2}, L_{int3} and C_{int1} to enhance the gain. C_{in2}, C_{out2} and C_{DC} are used as DC blocks and C_{b1}, C_{b2}, C_{b3}, C_{b4}, C_{b5} and C_{b6} are bypass capacitors, respectively. The design parameter values are listed in Table 3.1.

In the LNA, simultaneous noise and input matching (SNIM) for the dual-band input matching [45] is obtained by using the inductive degeneration as shown in Fig. 3.11. The input impedance is derived as

$$Z_{in} = j\omega\left(L_{in2} + L_{e1}\right) + \frac{1}{j\omega C_{be}} + \frac{1}{j\omega C_{in2}} + \left(j\omega L_{in1} \,//\, \frac{1}{j\omega C_{in1}} \right) + \frac{L_{e1} g_m}{C_{be}} \tag{3.16}$$

At two frequencies, f_1 and f_2,

$$j\omega\left(L_{in2} + L_{e}\right) + \frac{1}{j\omega C_{be}} + \frac{1}{j\omega C_{in2}} + \left(j\omega L_{in1} \,//\, \frac{1}{j\omega C_{in1}} \right) = 0 \text{ and } \frac{L_{e1} g_m}{C_{be}} = 50\Omega \tag{3.17}$$

Two ports of the dual-band LC circuit are located between transistors Q_1 and Q_2, and Q_3 and Q_4 in the 1st and 2nd stage amplifier as shown in Fig. 3.10. The capacitances

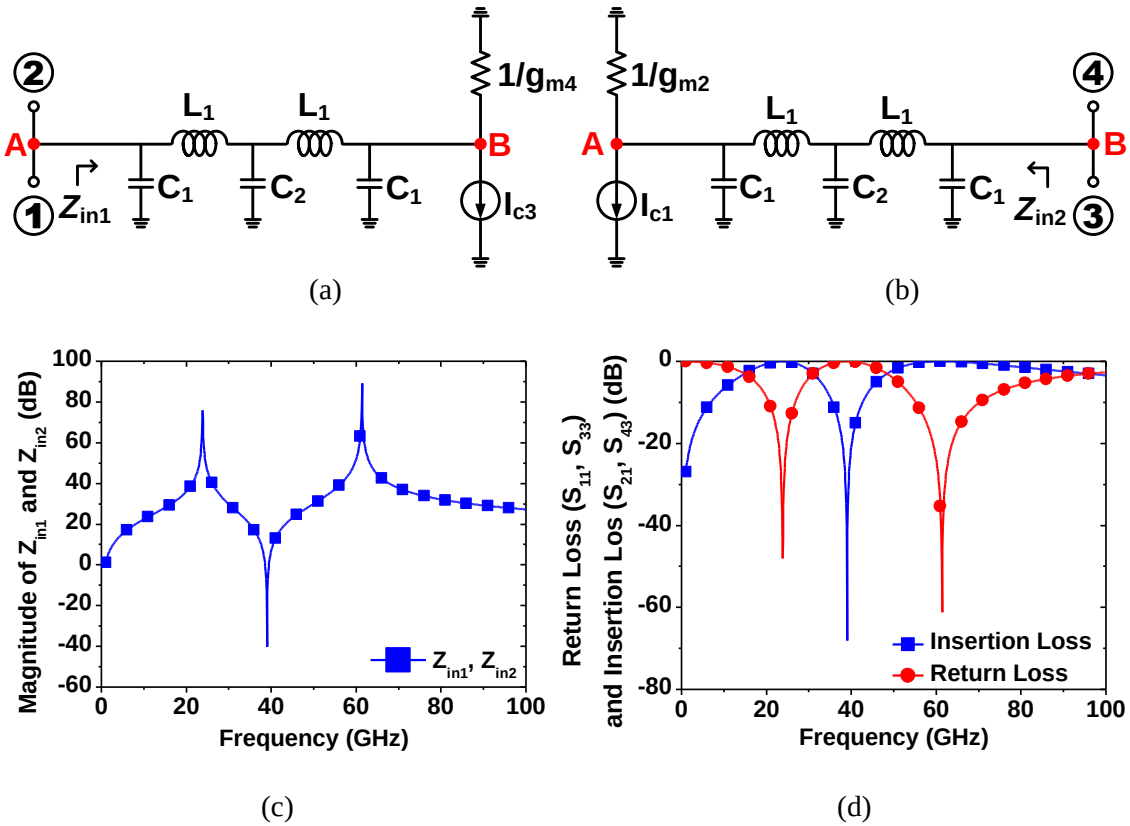
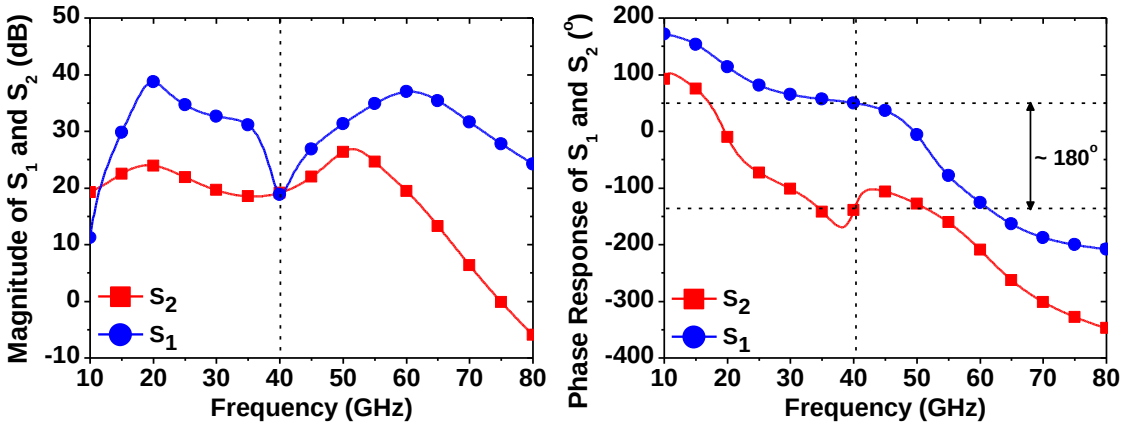


Fig. 3.12. Equivalent circuit models of the dual-band LC circuit in the LNA (a) looking into node 'B' at node 'A', (b) looking into node 'A' at node 'B', (c) simulated impedance magnitude of Z_{in1} and Z_{in2} in Figs. 3.12(a) and (b), and (d) simulated return losses (S_{11} and S_{33}) and insertion losses (S_{21} and S_{43}) of Figs. 3.12(a) and (b).

generated by Q_1, Q_2 and Q_3, Q_4 can increase the noise contribution of the cascade topology [45], [48].

To reduce this effect, the dual-band LC circuit utilizes the capacitances as a part of the dual-band LC circuit.

To recognize the function of the dual-band LC circuit for the LNA, Figs. 3.12(a) and (b) show the equivalent circuits models looking into the dual-band LC circuit at node 'A' and 'B' in Fig. 3.10, respectively. Fig. 3.12(c) shows the simulated impedance



(a) (b)

Fig. 3.13. (a) Simulated magnitude and (b) phase response of the 'S_1' and 'S_2' in Fig. 3.10.

magnitudes of the two equivalent circuits at nodes 'A' and 'B'. Magnitudes of $1/gm_2$ and $1/gm_4$ are assumed to be small enough and negligible. Input impedances (Z_{in1} and Z_{in2} in Figs. 3.12(a) and (b)) at node 'A' looking into node 'B' and vice versa show two high impedances at two pass bands (24 and 60 GHz) and a low impedance at one stop band frequency (~40 GHz). And, Fig. 3.12(d) shows clearly two pass bands and one stop and it is same as the results in Fig. 3.9(d).

For the analysis of the signals' flow, two kinds of signals ('S_1' and 'S_2' from node 'A' to node 'B' in Fig. 3.10) can be considered as: 'S_1' is the signal through Q_2 and Q_3 transistors, and 'S_2' is the signal via dual-band LC circuit, respectively. Fig. 3.13 shows the simulated magnitude and phase response of the two signals ('S_1' and 'S_2') at node 'B' from node 'A' in Fig. 3.10. The 'S_1' and 'S_2' show similar magnitudes and out of phase (~180° phase difference) at the stop-band frequency (~40 GHz). Also, Fig. 3.14 shows the simulated magnitude and phase response of the combined signal ('S_1' + 'S_2')

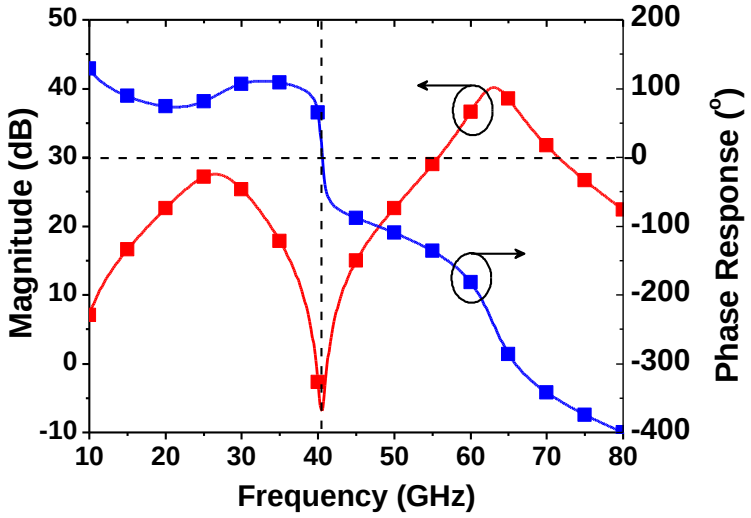


Fig. 3.14. Simulated magnitude and phase response of the combined signal ('S_1'+'S_2') at both ends (nodes 'A' and 'B') of the dual-band LC circuit in Fig. 3.10 when the 'S_1' and 'S_2' meet.

at node 'B' from 'A' in Fig. 3.10, and it also shows one stop band and two pass bands. These results in Figs. 3.13 and 3.14 mean that the stop-band signals in the 'S_1' and 'S_2' meet together and cancel each other out at node 'B'. Furthermore, Fig. 3.14 shows different magnitudes (also called gain) at the two pass bands from node 'A' to 'B', which it is due to inherent low-pass characteristics of the dual-band LC circuit.

The foregoing discussion means that the majority of the stop-band signal and some of low frequency band signals including the first pass band at node 'A' flows into the dual-band LC circuit to node 'B' ('S_2' in Fig. 3.10). On the other hand, most of the two pass-band signals and few of the stop-band signals and low frequency bands signals go through the transistors Q_2 and Q_3 ('S_1' in Fig. 3.10). Thus, it can be seen that the stop band signals of 'S_1' and 'S_2' cancel out each other at node 'B', and the low-frequency

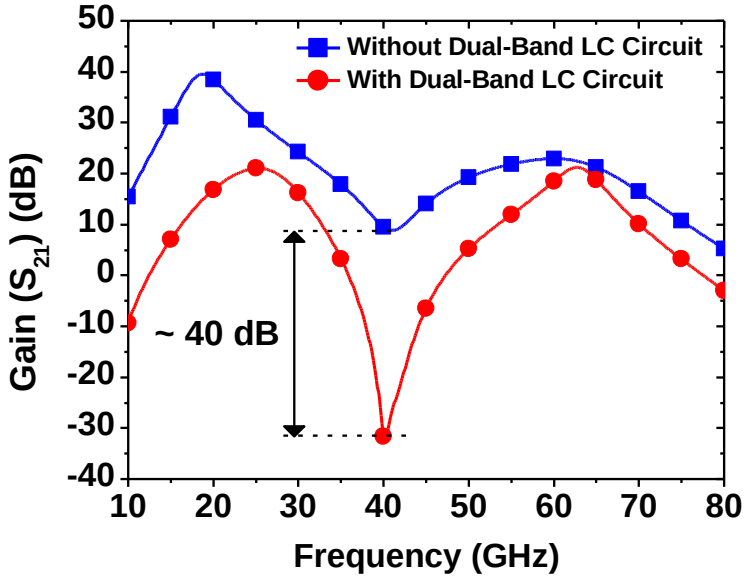


Fig. 3.15. Simulated gain (S_{21}) of the proposed LNA with and without the dual-band LC circuit.

signals including the first pass band of 'S_1' and 'S_2' also meet and some of them cancel out. As a result, lower gain at 24 GHz is obtained.

Fig. 3.15 shows the simulated gain (S_{21}) comparison of the proposed LNA with and without dual-band LC circuit. Since an amplifier normally has higher gain at a lower frequency such as 24 GHz than at higher frequency like 60 GHz because the maximum available gain decreases as the frequency increases [41], Fig. 3.15 shows that the LNA has higher gain at 24 GHz without dual-band LC circuit. With the proposed dual-band LC circuit, however, the LNA at low frequency bands including 24 GHz has lower gain compared to the gain at 60 GHz as shown in Fig. 3.14. As a result, similar gains at 24 and 60 GHz are obtained as shown in Fig. 3.15. Fig. 3.15 shows the improved stop-band rejection by around 40 dB due to the dual-band LC circuit. To summarize, using the

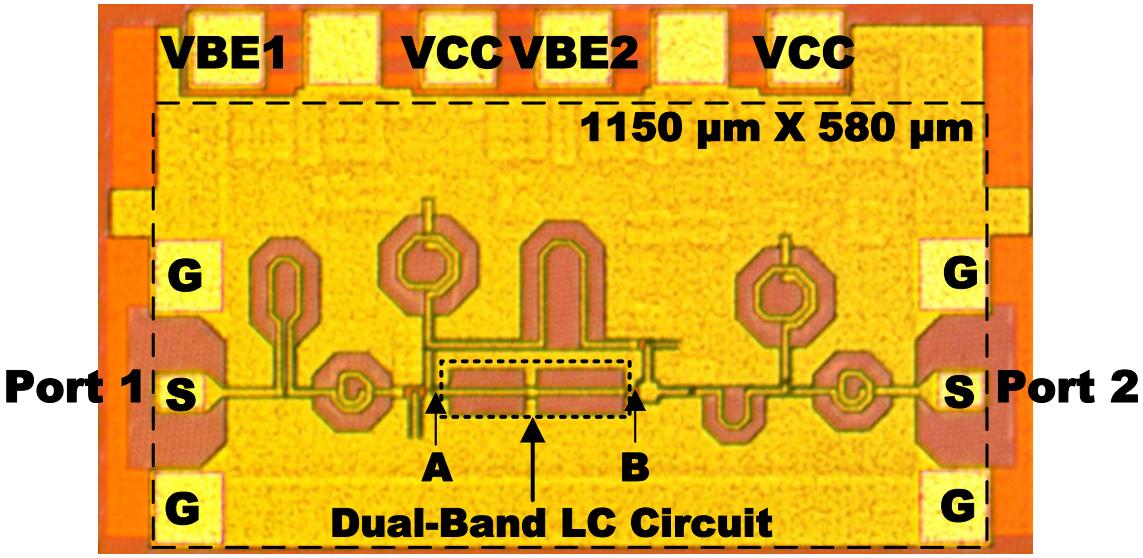


Fig. 3.16. Microphotograph of the 24/60-GHz dual-band LNA. Locations for node 'A' and 'B' correspond to those in Fig. 3.10.

proposed dual-band LC circuit, the LNA has improved stop-band rejection and the gain balance at 24 and 60 GHz is achieved.

3.5 Simulation Results

The concurrent dual-band LNA, whose photograph is shown in Fig. 3.16, was designed and fabricated using 0.18-µm SiGe BiCMOS process [49]. All the inductors and inter-connection lines were designed using CPW structures and simulated using EM simulator IE3D [50]. The total chip sizes are 1150 μm × 580 μm including RF pads.

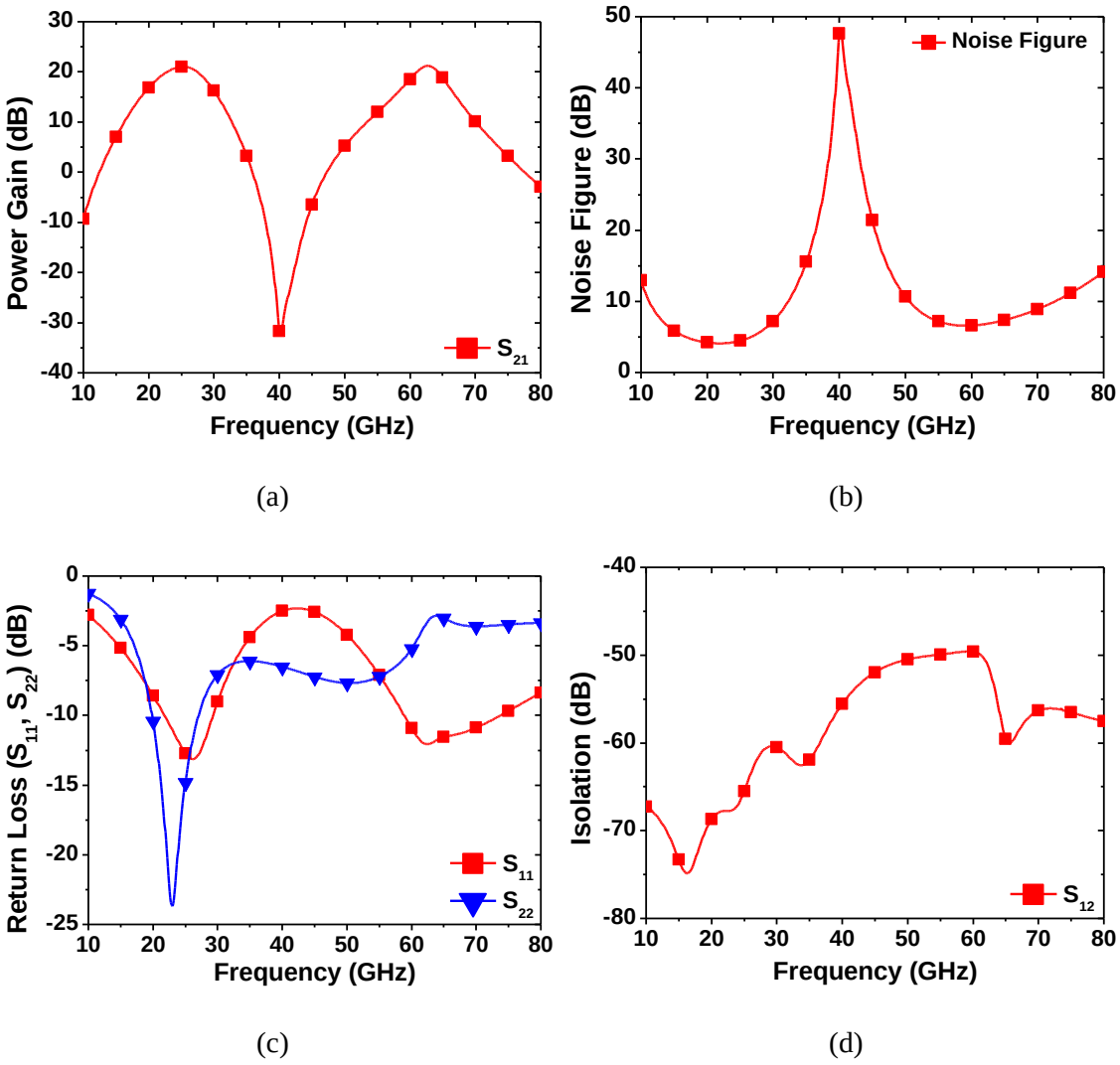


Fig. 3.17. Simulated results for: (a) gain, (b) NF, (c) S_{11} and S_{22} and (d) isolation (S_{12}).

Fig. 3.17 shows the simulated results for gain, NF, return loss, and isolation. As can be seen in Fig. 3.17(a), the dual-band LNA exhibits simulated gains of 20.7 and 18.5 dB at 24 and 60 GHz, and peak gains are 21 dB at 25 GHz and 21 dB at 63 GHz, respectively. The simulated stopband rejection ratio from the peak gain at 25 GHz to the

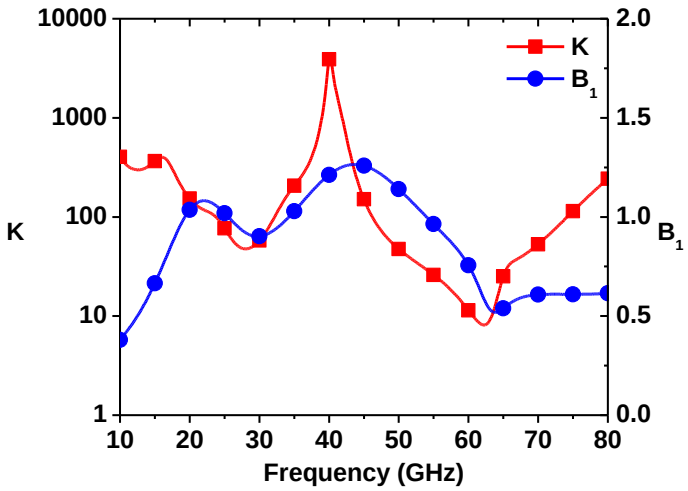
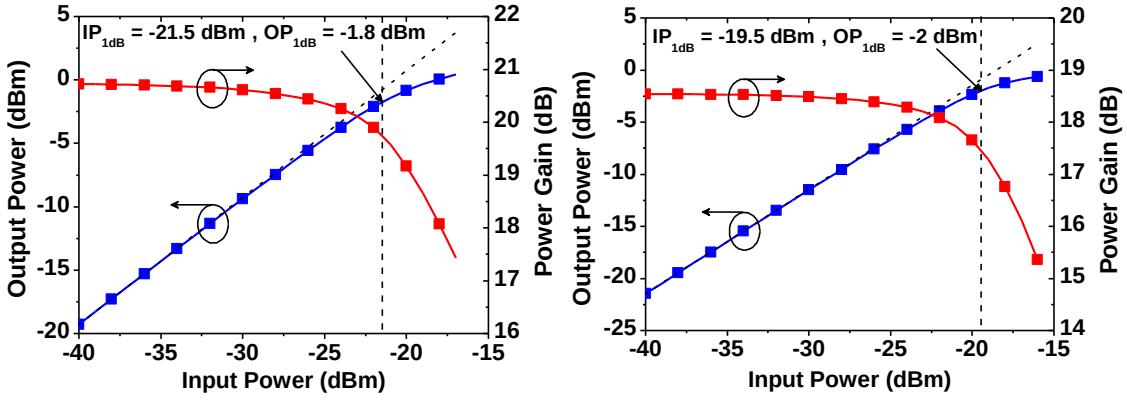


Fig. 3.18. Simulated stability factors K and B_1.

attenuation at 40 GHz is 53 dB. The simulated 3-dB passbands are 21 – 29 and 59 – 65 GHz.

Fig. 3.17(b) shows the simulated NFs are 4.25 and 6.6 dB at 24 and 60 GHz, respectively. The simulated input and output return losses are more than 10 and 3 dB, respectively, as seen in Fig. 3.17(c), and the simulated reverse isolation remains more than 50 dB across the entire dual-band, as shown in Fig. 3.17(d). Fig. 3.18 shows the stability factors, which meet the necessary and sufficient conditions for unconditional stability ($K > 1$ and $B_1 > 0$) as described in Sec. 3.1.2 [41]. Fig. 3.19 shows the simulated 1-dB compression point (P_{1dB}) for single-band modes at 24 GHz and 60 GHz. The dual-band LNA achieves input and output P_{1dB}s of -21.5 and -1.8 dBm at 24 GHz, -19.5 and -2 dBm at 60 GHz and the simulated input and output IP_3s of -11.7 and 9 dBm at 24 GHz and -9.3 and 9.2 dBm at 60 GHz, respectively. It consumes 19.4 mW with a supply voltage of 1.8 V.



(a) (b)

Fig. 3.19. Simulated P_{1dB}s at: (a) 24 GHz and (b) 60 GHz.

3.6 Summary

Table 3.2 summarizes the simulated performances of the concurrent dual-band LNA and those of published concurrent dual-band LNAs. Considering that NF results of the developed dual-band LNA are the simulated ones, the LNA exhibits comparable NF performance compared to the dual-band LNAs reported in [51]–[54]. It also has the best gain flatness than the most of the reported dual-band LNAs in the 10- to 60-GHz frequency regime. Also, the developed tri-band LNA achieves the best stopband rejection ratios among the reported dual-band LNAs. Therefore, the proposed concurrent dual-band LNA can be a good candidate for a dual-band receiver operating at millimeter-wave frequencies.

Table 3.2
Performance Summary of the Developed Concurrent Dual-Band LNA and Existing Concurrent Dual-Band LNAs

Ref	Process	Freq (GHz)	Gain (dB)	NF (dB)	IIP_3 (dBm)	S_{11} (dB)	Pass-band Gain Imbalance (dB)	Stop-band Rejection Ratio (dB)	Power (mW)	Area (mm^2)
[51]	0.18-µm CMOS	18	9.2	5.7	-2	-23	2.8	9	8	0.33
		24.5	12	6.4	-3	-24				
[52]	0.13-µm CMOS	10	25.3	5.3	N/A	-24.4	13.2	44	12	1.14
		24	12.1	10.4	N/A	-17.9				
[53]	65-nm CMOS	24	15.9	5.5	N/A	N/A	4.6	32	85	0.6
		60	11.3	7.4	N/A	N/A				
[54]	0.18-µm SiGe BiCMOS	24	21.9	5.1	-10.4	<-10	5.3	22	-	0.19
		35	16.6	7.2	-8.3	<-10				
***This Work**	0.18-µm SiGe BiCMOS	24	20.7	4.25	-11.7	<-10	1.9	53	19.4	0.67
		60	18.8	6.6	-9.3	<-10				

*Results are simulated results.

CHAPTER IV

DESIGN OF A SIGE BICMOS CONCURRENT DUAL-BAND FRONT-END MODULE

4.1 Introduction

An RF front end module (FEM) is part of an RF receiver-transmitter or transceiver subsystem, and it consists of components between the antenna and base-band subsystem. As the components in the RF transceiver, the noise figure, insertion loss, isolation, power handling capability and nonlinearity of the FEM are important factors to determine the performance of the entire RF system [55], [56].

In this chapter, a 24/60-GHz concurrent dual-band FEM consisting of a dual-band T/R switch, a dual-band LNA and dual-band PA, and they are fully integrated using 0.18-μm SiGe BiCMOS process.

4.2 Design of a Concurrent Dual-Band Front-End Module (FEM)

The proposed concurrent dual-band FEM consists of the 24/60-GHz dual-band antenna, five-port T/R switch, two LNAs, and one PA as shown in Fig. 4.1. Each component operates at 24 and 60 GHz bands concurrently. In view of system's total size, even though the positions of LNA and PA are interchangeable in the FEM, the configuration consisting of one PA and two LNAs can have an advantage of size than that consisting of two PAs and one LNA because the size of PA is normally much larger than that of LNA. The FEM can be employed for applications involving dual-

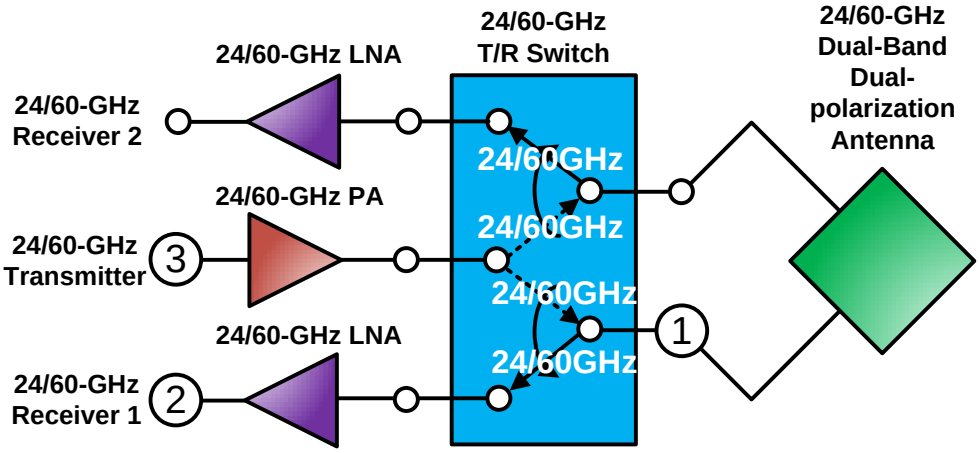
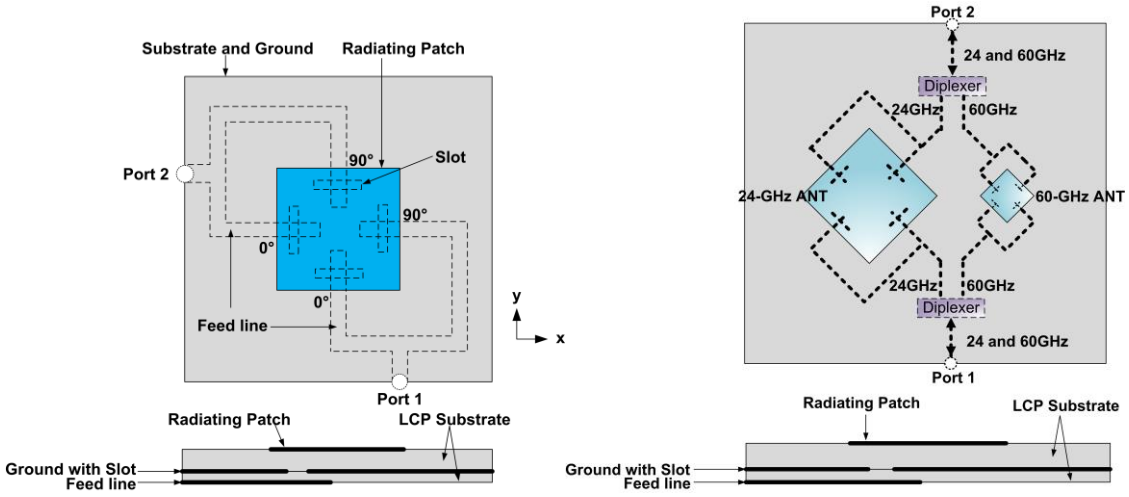


Fig. 4.1. Block diagram of the 24/60-GHz concurrent dual-band front-end module (FEM).

polarization (left- and right-handed circularly polarization). Dual polarization can lead to enhancement of isolation between two signals due to the orthogonal characteristic of dual polarized signals [9]. As the components of the FEM, the T/R switch described in Sec. 2.3 and the LNA described in Chapter III are employed. The PA [57] was designed by our laboratory's colleague, and it was integrated with others. The antenna has been designed but not been fabricated yet.

Fig. 4.2 shows the conceptual antenna structure, and it is designed as a two-port concurrent dual-band multi-layered aperture coupled microstrip antenna operating in both transmitting and receiving modes. Two ports generate right- and left-handed circularly polarized (RHCP and LHCP) signals. To achieve a dual circular polarization, the feed-line structures from each port generate 90° phase difference between x-axis and y-axis components from ports 1 and 2 as shown in Fig. 4.2(a). For instance, the y-axis component of signals from port 1 are 90° phase leading, on the other hand, the x-axis



(a) (b)

Fig. 4.2. Conceptual antenna structures of dual-polarized circular antenna for: (a) single-frequency band and (b) dual-frequency bands.

component of signals from port 2 are 90° phase leading. Thus, LHCP and RHCP signals are radiated at ports 1 and 2, respectively. To operate at dual-band frequency, two patches operating at separate operating frequencies are considered and feed-line structures are identical to the structure presented in Fig. 4.2(a). Fig. 4.2(b) shows the entire conceptual dual-band antenna structure, and ports 1 and 2 operate at the dual frequency simultaneously.

Fig. 4.3 shows a microphotograph of the proposed FEM fabricated using 0.18-µm SiGe BiCMOS process [52]. All the inductors and inter-connection lines were designed using a CPW structure and simulated using EM simulator IE3D [53]. The total chip sizes are around 4073 μm × 3215 μm including all the RF and DC pads. The circuits ‘A’, ‘B’ and ‘C’ marked in Fig 4.2.3 are the T/R switch, LNA and PA,

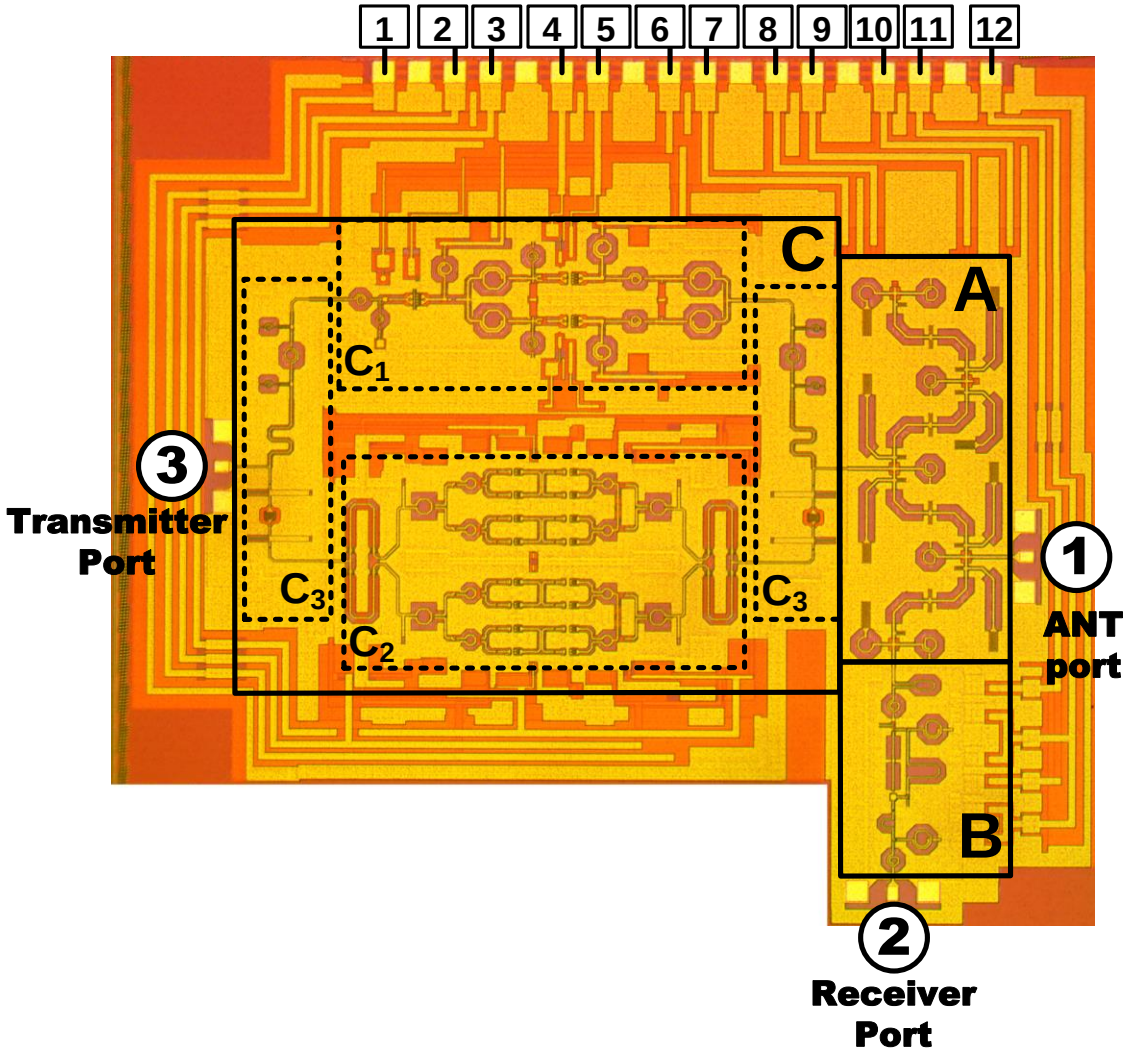


Fig. 4.3. Microphotograph of the proposed 24/60-GHz concurrent dual-band FEM. Port numbers correspond to those in Fig. 4.1.

respectively, and the port numbers correspond to those in Fig. 4.1. Since each port of all the components is designed with 50-Ω terminations, additional matching networks between them are not necessary. The PA is designed with the combined 24-GHz ('C_1' in Fig. 4.3), 60-GHz PAs ('C_2' in Fig. 4.3) and two 24/60-GHz duplexer ('C_3' in Fig. 4.3),

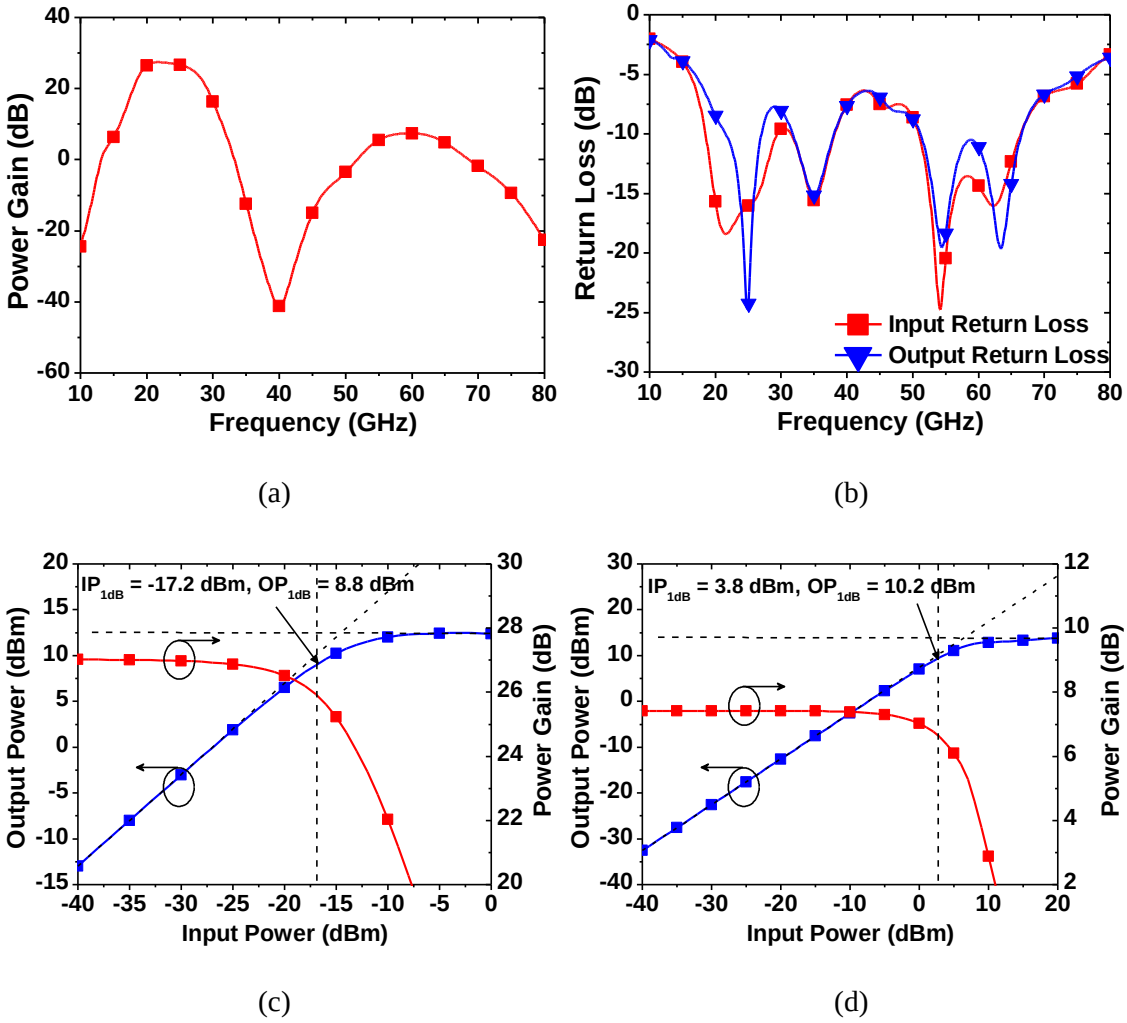


Fig. 4.4. Simulated results of the 24/60-GHz concurrent dual-band PA [57] for: (a) power gain, (b) input and output return losses, (c) P_{1dB} and P_{out} at 24 GHz, and (d) P_{1dB} and P_{out} at 60 GHz.

and it has concurrent dual-band characteristic. Fig. 4.4 shows the simulated gain, return losses, P_{1dB}s and P_{out} of the 24/60-GHz concurrent dual-band PA.

The 24/60-GHz PA exhibits simulated gains of 27 and 7.4 dB at 24 and 60 GHz including two 24/60-GHz diplexers (each having the simulated insertion losses of around 8 dB at 24 and 60 GHz) at the input and output of the PA in Fig. 4.3. Fig. 4.4(c) and (d)

Table 4.1
DC Bias Setup for Receiving and Transmitting Operations

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12
	PA 60 V_{B2}	PA 60 V_{B1}	PA 60 V_{CC}	PA 24 V_{BB1}	PA 24 V_{BB2}	PA 24 V_{CC}	SW V_{DD}	SW V_T	SW V_R	SW V_A	LNA V_{BE}	LNA V_{CC}
RX Operation	0 V	0 V	0 V	0 V	0 V	0 V	1.8 V	1.8 V	0 V	0 V	0.87 V	1.8V
TX Operation	2V	1 V	2 V	1 V	2 V	2 V	0 V	0 V	1.8 V	0 V	0 V	0 V

shows the simulated input and output P_{1dB}s of -17.2 and 8.8 dBm at 24 GHz, and 3.8 and 10.2 dBm at 60 GHz, respectively. The simulated saturated output powers (P_{out}) are 12.3 dBm at 24 GHz and 13.8 dBm at 60 GHz, respectively.

4.3 Simulation Results

The FEM works in separate receiving (RX) and transmitting (TX) operations, and it is applicable to a Time Division Duplexing (TDD) system. The bias setup for each operation is listed in Table 4.1. Simulated results for each operation of the FEM are as follows.

4.3.1 Receiving (RX) Operation

Receiving operation is conducted in the reception path (T/R switch and LNA). Fig. 4.5 shows the simulated results of the FEM in the receiving operation for gain, NF, return losses, and TX–RX isolation. The FEM exhibits the simulated gains (insertion loss of T/R switch + gain of the LNA) of 16.7 and 12.9 dB at 24 and 60 GHz, and peak gains are 16.8 dB at 24.4 GHz and 17.2 dB at 64.3 GHz, respectively. The simulated stop-band

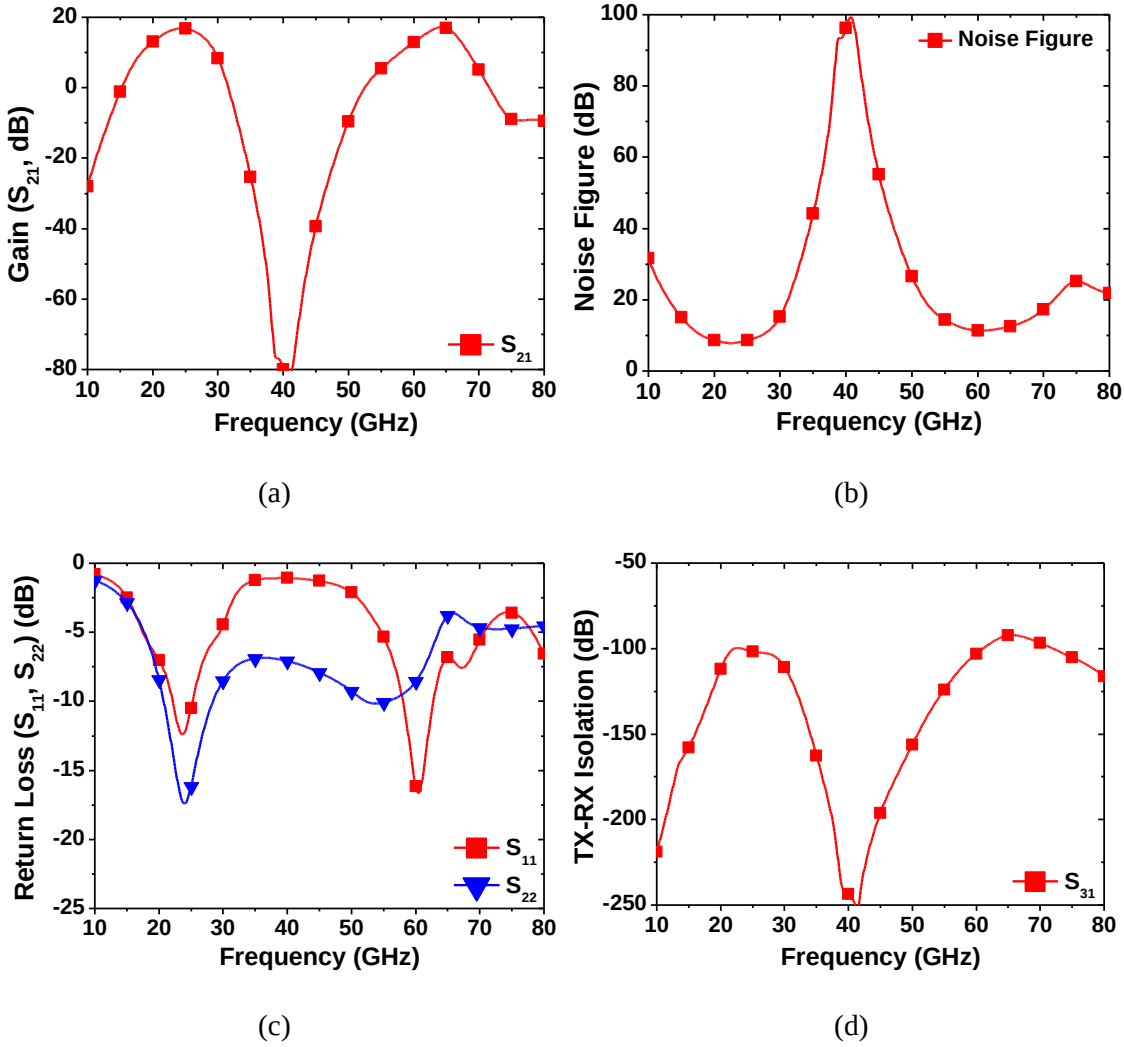
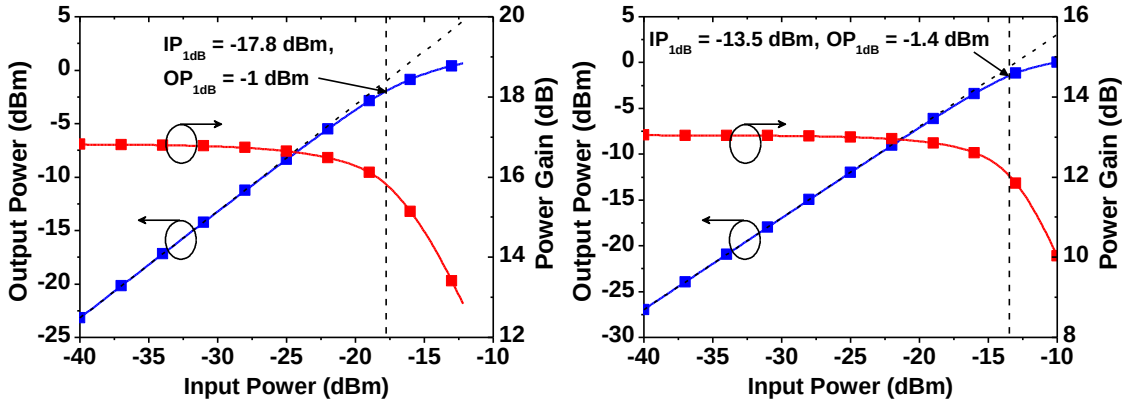


Fig. 4.5. Simulated results of the FEM in the receiving operation for: (a) gain (S_{32}), (b) NF, (c) S_{11} and S_{22} and (d) TX–RX isolation (S_{13}). Port numbers correspond to those in Fig. 4.3.

rejection ratio from the peak gain at 64.3 GHz to the loss at 40.7 GHz is around 100 dB. The simulated 3-dB passbands are 20.6–27.5 and 61–66.7 GHz. Fig. 4.5(b) shows the simulated NFs are 8.14 and 11.38 dB at 24 and 60 GHz, respectively. The simulated input and output return losses are more than 10 and 5 dB, respectively, as seen in Fig. 4.5(c), and the simulated TX Port–RX port isolation (Port 2 to Port 3 in Fig. 4.3) remains



(a) (b)

Fig. 4.6. Simulated input and output P_{1dB}s at: (a) 24 GHz and (b) 60 GHz.

more than 90 dB across the entire dual-band, as shown in Fig. 4.5(d). Fig. 4.6 shows the simulated 1-dB compression point (P_{1dB}) of the FEM in the receiving operation at 24 GHz and 60 GHz. The dual-band LNA achieves the input and output P_{1dB}s of -17.66 and -1.7 dBm at 24 GHz, -15.4 and -1.79 dBm at 60 GHz. And, the simulated input and output third-order intercept points (IP_3) for single-band modes with the two tones spaced 1 MHz apart are -11.7 and 9 dBm at 24 GHz and -9.3 and 9.2 dBm at 60 GHz, respectively.

4.3.2 Transmitting (TX) Operation

Transmitting operation is conducted in the transmission path (T/R switch and PA). Fig. 4.7 shows the simulated results of the FEM in transmitting operation for gain, return loss, and isolation. In Fig. 4.7(a), the FEM presents simulated gains of 22 at 24 GHz and 1.8 dB at 60 GHz, respectively. The simulated stopband rejection ratio from

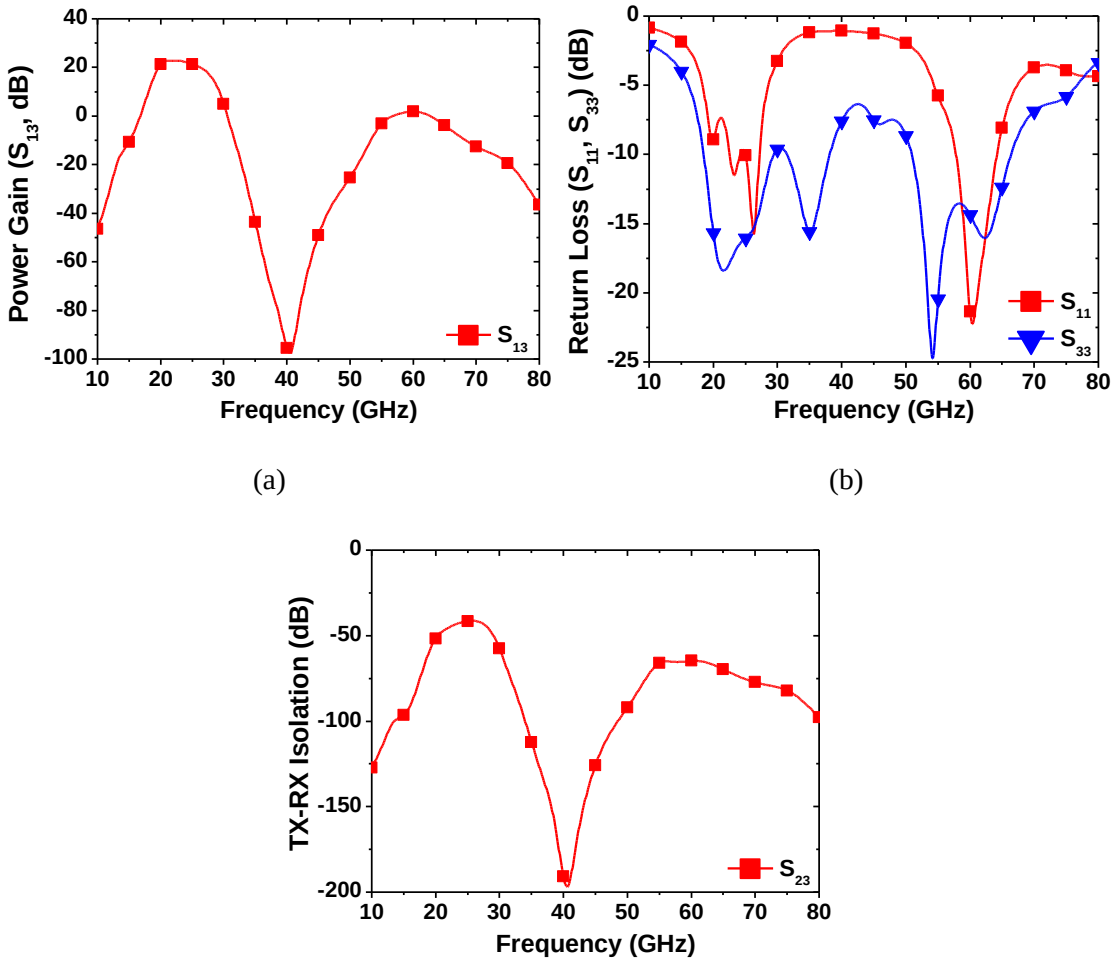
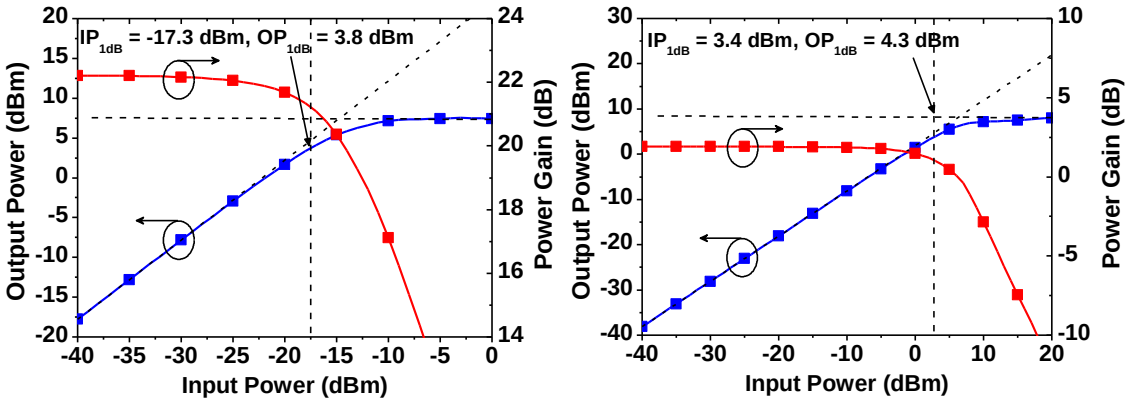


Fig. 4.7. Simulated results of the FEM in transmitting operation for: (a) power gain (S_{13}), (b) input and output return losses, and (c) TX–RX isolation (S_{23}).

the peak gain at 22 GHz to the loss at 40.5 GHz is around 118 dB. The simulated 3-dB passbands are 19.7–26.4 and 55.9–63.5 GHz. The simulated input and output return losses are more than 10 dB at 24 and 60 GHz, respectively, as seen in Fig. 4.7(b), and the simulated TX–RX port isolation (Port 3 to Port 2 in Fig. 4.3) is more than 43 dB across



(a) (b)

Fig. 4.8. Simulated input and output P_{1dB}s and P_{out} of the FEM in the transmitting operation at: (a) 24 GHz and (b) 60 GHz.

the entire dual-band, as shown in Fig. 4.7(c). Fig. 4.8 shows the simulated P_{1dB} of the FEM in the transmitting operation for single-band modes.

The dual-band LNA achieves input and output P_{1dB}s of -17.3 and 3.8 dBm at 24 GHz, 3.4 and 4.3 dBm at 60 GHz, and input and output IP_3s of -11.7 and 9 dBm at 24 GHz and -3 and 9.2 dBm at 60 GHz, respectively, with the two tones spaced 1 MHz apart at 24 GHz and 60 GHz. The saturated output powers (P_{out}) are 7.4 and 8 dBm at 24 and 60 GHz, respectively.

4.4 Summary

A fully integrated 24/60-GHz concurrent dual-band front-end module (FEM) consisting of the dual-band T/R switch, dual-band LNA and dual-band PA has been proposed. Simulated result summaries are listed in Table 4.2. Since all the components of the FEM have a concurrent dual-band characteristic, a distinctive dual-band

Table 4.2
Simulated Performance Summary of the 24/60-GHz Concurrent Dual-Band Front-End Module (FEM)

	24 GHz Band				60 GHz Band				
RX Operation	Gain (dB)	NF (dB)	TX–RX ISO (dB)	IP_{1dB} /OP_{1dB} (dBm)	Gain (dB)	NF (dB)	TX–RX ISO (dB	IP_{1dB} /OP_{1dB} (dBm)	Stop Band Rej. (dB)
	16.7	8.14	90	-17.66 /-1.7	12.9	11.38	102	-15.4 /-1.79	100
TX Operation	Gain (dB)	P_{out} (dBm)	TX–RX ISO (dB)	IP_{1dB} /OP_{1dB} (dBm)	Gain (dB)	P_{out} (dBm)	TX–RX ISO (dB)	IP_{1dB} /OP_{1dB} (dBm)	Stop Band Rej. (dB)
	22	7.4	42	-17.3 /3.8	1.8	8	64	3.4 /4.3	118

characteristic, very high stop-band, and out of band rejection are shown in both of the RX and TX operations. For example, as locating image signal's frequency at stop-band frequency using proper LO frequency in view of receiver system configuration, the image signal can be attenuated by the very high stop-band rejection. Thus, potential image signal problem can be solved in a RX operation. And also, high stop-band and out of band rejection can lead to attenuation of the harmonic elements of two pass-band signals; thus, nonlinearity problem can be improved in the TX operation. Therefore, the FEM can be good candidate for multi-band communication systems like phased array and RFID reader systems.

CHAPTER V

SUMMARY AND CONCLUSION

This dissertation presents the research of concurrent dual-band RF switches, LNAs and front-end modules for communication and sensing systems such as phased array, radar and RFID reader systems using two ISM bands around 24 and 60 GHz. They are fully integrated using a 0.18-μm SiGe BiCMOS process and they are implemented using different techniques to achieve the dual-band characteristics.

5.1 Dissertation Summary

Chapter II introduces four different dual-band SPDT and T/R switches (Designs 1, 2, 3 and 4) with dual-band band-pass filtering functions that the conventional RF switches do not have. The proposed switches show not only switching but also band-pass filtering functions.

Design 1 presents a new dual-band T/R switch having a band-pass filtering function working concurrently at 35.5–43.7 GHz and 56.5–63 GHz. The developed switch has multiple ports, with each port handling a dual-band signal concurrently, and a high isolation (more than 50 dB over two pass bands) between ports, which making it attractive for the use of the dual-band RF systems. It is also demanded in systems having multi-port and dual-band concurrent operation with band-pass filtering and high isolation. The switch is designed based on the 3rd dual-band band-pass filter with its capacitors replaced with a shunt nMOS transistor for switching function.

Design 2 describes a new CMOS concurrent 24/60-GHz T/R switch having dual-bandpass filtering function. The switch is implemented with dual-band quarter-wavelength LC networks and dual-band resonators with their capacitor replaced with shunt nMOS transistor. On/off states of the switch are determined through a quarter-wavelength characteristic of the dual-band LC network and off/on states of the shunt transistor. The developed T/R switch has multiple ports, with each port being capable of handling dual bands concurrently, making it attractive for the use in multi-band RF systems, and it is demanded by the multi-port and multi-band concurrent operation with band-pass filtering function.

Design 3 shows new 24/60-GHz dual-band SPDT and T/R switch architectures having band-pass filtering function. The switch is based on 2^{nd} order band-pass filter. The dual-band band-pass filtering SPDT can operate in single-band mode at 24 or 60 GHz as well as concurrent dual-band modes at 24 and 60 GHz. The dual-band band-pass filtering T/R switch's operation is more versatile, and it can be used for various individual and concurrent switching functions. It can operate in single-band transmitting or receiving mode at 24 and 60 GHz, and concurrent dual-band transmission or reception at 24 and 60 GHz. It can work completely in concurrent modes including single-band concurrent transmission and reception at 24 or 60 GHz and dual-band concurrent transmission and reception at 24 and 60 GHz. The developed T/R switch makes it possible simultaneous transmissions and receptions with a single antenna, which is desirable in RF systems yet not feasible with conventional T/R switches.

Design 4 explains a new concurrent dual-band CMOS SPDT switch operating

over two distinctive wide bands around 24 and 60 GHz. In case of on-state of the switch, the SPDT switch is equivalent to a dual-band resonator. The concurrent dual-wideband SPDT switch has a decent insertion loss, compact size, and good power handling capability.

Chapter III presents a development of a concurrent dual-band LNA operating at 24 and 60 GHz bands. To achieve dual-band characteristic, a dual-band quarter-wavelength LC circuit has been proposed. It shows a quarter-wavelength characteristic at two pass bands and dual band performance, when it is connected to ground in parallel. And, it is connected to cascode nodes of 1^{st} and 2^{nd} stage of the LNA. With the dual-band LC circuit, two pass-band signals are amplified and stop-band signals are attenuated. Moreover, as a gain imbalance decreases, a high stop-band rejection is achieved.

Chapter IV depicts the concurrent dual-band front-end module (FEM) consisting of the designed concurrent dual-band T/R switch, LNA and PA. The FEM shows distinctive dual-band characteristics in view of gain, return loss and noise figure in the receiving (RX) and transmitting (TX) operations. The FEM shows high TX–RX port isolation (gain–isolation ratio) of over 60 dB in RX and TX operations. Furthermore, the FEM shows very high stop-band rejection and out of band rejection ratio over 100 dB, and it can potentially help to reduce the image signal problem that is one of the receiver's problems, and the nonlinearity problem can be also be improved in the transmitter.

5.2 Recommendations for Future Work

Even though the proposed millimeter-wave switches show a good dual-band characteristic, isolation and power handling capability, additional works are still remained to improve the performance of the proposed switch. The proposed switches do not have low insertion losses. Insertion loss of the switch directly influences the receiver's total noise figure. This problem, however, can be alleviated in view of system architecture. One possible suggestion is that, a bidirectional amplifier (PA/LNA) can be placed between the antenna and the RF switch. In this configuration, the influence on the noise of the switch's high insertion loss decreases due to the gain of the amplifier. Nevertheless, the development of multiband switches having not only a multi-band filtering function but also lower insertion loss is still left as open to more research.

Due to the high insertion loss of the proposed switch, the proposed FEM does not also show a good noise figure. This, however, can also be overcome with a system architecture mentioned above. With low NF, the proposed concurrent dual-band FEM would be used for numerous multi-functional applications such as short- and long-range high-data-rate communications, sensing, imaging, radar and RFID systems.

In conclusion, this research and study have shown the depth of this subject, and they also open up great possibilities of further research and development to be done in future in the area of multi-band integrated communication and sensing systems.

REFERENCES

[1] X. Guan and A. Hajimiri, "A 24GHz CMOS Front-End," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368–373, Feb. 2004.

[2] K. Finkenzeller, *RFID Handbook: Fundamentals and Application in Contactless Smart Cards and Identification 2nd ed.*, New York: Wiley, 2003.

[3] C. Shannon, "A Mathematical Theory of Communication," *The Bell System Technical Journal*, vol. 27, pp. 379423, 623-656, July-October 1948.

[4] IEEE 802.15 Working Group for WPAN; http://www.ieee802.org/15/.

[5] C. –H. Chang, Y. –T. Lo, and J. –F. Kiang, "A 30GHz Active Quasi-Circulator With Current-Reuse Technique in 0.18um CMOS Technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 12, pp. 693–695, Dec. 2010.

[6] H. –S. Wu, C. –W. Wang, and C. –K. C. Tzuang, "CMOS Active Quasi-Circulator With Dual Transmission Gains Incorporating Feedforward Technique at K-Band," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 8, pp. 2084–2091, Aug. 2010.

[7] Agilent (Keysight) ADS, Agilent Technologies, 1400 Fountaingrove Parkway, Santa Rosa, CA 95403-1799, 2011.

[8] K.-J. Koh, J. W. May, and G. M. Rebeiz, "A millimeter-wave (40–45 GHz) 16-element phased-array transmitter in 0.18-μm SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1498–1509, May 2009.

[9] C. A. Balanis, *Antenna Theory, Analysis and Design 3rd ed*., New Jersey: Wiley, 2006.

[10] X. J. Li and Y. P. Zhang, "Flipping the CMOS Switch," *IEEE Microwave Mag*., vol. 11, no. 1, pp. 86–96, Jan. 2010.

[11] R. Goggin, Th. Corrigan, "CMOS Switches Offer High Performance in Low Power, Wideband Applications", High Frequency Electronics, Feb. 2004.

[12] D. Im, B. –K. Kim, D. –K. Im, and K. Lee, "A Stacked-FET Linear SOI CMOS Cellular Antenna Switch With an Extremely Low-Power Biasing Strategy," *IEEE Trans. Microw. Theory Tech*., vol. 63, no. 6, pp. 1964–1977, Jun. 2015.

[13] X. S. Wang and C. P. Yue, "A Dual-Band SP6T T/R Switch in SOI CMOS With 37-dBm for GSM/W-CDMA Handsets," *IEEE Trans. Microw. Theory Tech*., vol. 62, no. 4, pp. 861–870, Apr. 2014.

[14] C. Tinella, J. M. Fournier, D. Belot, and V. Knopik, "A High-Performance CMOS-SOI Antenna Switch for the 2.5-5-GHz Band," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp.1 279–1283, Jul. 2003.

[15] A. Tombak, M. S. Carroll, D. C. Kerr, J. –B. Pierres, and E. Spears, "Design of High-Order Switches for Multimode Applications on a Silicon-on-Insulator Technology," *IEEE Trans. Microw. Theory Tech*., vol. 61, no. 10, pp. 3639–3649, Oct. 2013.

[16] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K. Y. Lin, Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body floating technique to improve power performance," *IEEE Trans. Microw. Theory Tech*., vol. 54, no. 1, pp. 31–39, Jan. 2006.

[17] J. Bae, J. Lee, C. Nguyen, "A 10–67-GHz CMOS Dual-Function Switching Attenuator With Improved Flatness and Large Attenuation Range," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 12, pp. 4118–4129, Dec. 2013.

[18] B. Razavi, *Design of Analog CMOS Integrated Circuits*, New York, NY, USA: McGraw-Hill, 2001.

[19] C. Huynh and C. Nguyen, "New Ultra-High-Isolation RF Switch Architecture and Its Use for a 10–38-GHz 0.18-μm BiCMOS Ultra-Wideband Switch," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 2, pp. 345–353, Feb. 2011.

[20] D. M. Pozar, *Microwave Engineering* 3rd ed, New York: Wiley, 2005.

[21] B. Razavi, *RF Microelectronicss*, New York, NY, USA: McGraw-Hill, 2001.

[22] M. Uzunkol and G. M. Rebeiz, "A Low-Loss 50–70 GHz SPDT Switches in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2003–2006, Oct. 2010.

[23] X. Guan, Z. Ma, P. Cai, Y. Kobayashi, T. Anada, and G. Hagiwara, "A dual-band bandpass filter synthesized by using frequency transformation and circuit conversion technique," in Proceedings of the IEEE Asia-Pacific Microwave Conference (APMC '05), vol. 4, Yokohama, Japan, December 2005.

[24] X. Guan, Z. Ma, P. Cai, Y. Kobayashi, T. Anada, and G. Hagiwara, "Synthesis of dual-band bandpass filters using successive frequency transformations and circuit conversions," *IEEE Microw. Wireless Compon. Let*t., vol. 16, no. 3, pp. 110–112, Mar. 2006.

[25] G. L. Matthaei, L. Young and E. M. T. Jones, *Microwave Filters, Impedance-Matching Networks, and Coupling Structures*, Artech House, Dedham, Mass., 1980.

[26] S. –G. Mao and M. –S. Wu, "Design of Artificial Lumped-Element Coplannar Waveguide Filters With Controllable Dual-Passband Responses," *IEEE Trans. Microw. Theory and Tech.*, vol. 56, no. 7, pp. 1684–1692, Jul. 2008.

[27] SBC18H2 Design Manual, Newport Beach, CA, USA: Jazz Semiconduct., 2013.

[28] K. M. Cheng and F. Wong, "A Novel Approach to the Design and Implementation of Dual-Band Compact Planar 90° Branch-Line Coupler," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 11, pp. 2458–2463, Nov. 2004.

[29] D. Lee, J. Lee, and C. Nguyen, "Concurrent Dual K/Ka-Band T/R/Calibration Switch Module With Quasi-Elliptic Dual-Bandpass Frequency Response Implementing Metamaterial Transmission Line and Negative Resistance," *IEEE Trans. Microw. Theory and Tech.*, vol. 64, no. 2, pp. 585–598, Feb. 2016.

[30] TowerJazz Semiconductor, 4321 Jamboree Road, Newport Beach, CA 92660-3095.

[31] M. C. Yeh, Z. M. Tsai, R. C. Liu, K. Y. Lin, Y. T. Chang, and H. Wang, "A millimeter-wave wideband SPDT switch with traveling-wave concept using 0.13-m CMOS process," in *IEEE MTT-S Int. Dig*., Jun. 2005, pp. 53–56.

[32] C. M. Ta, E. Skafidas, and R. J. Evans, "A 60-GHz CMOS transmit/ receive switch," in *IEEE RFIC Symp. Dig*., Jun. 2007, pp. 725–728.

[33] J. He, Y.-Z. Xiong, and Y. P. Zhang, "Analysis and design of 60-GHz SPDT switch in 130-nm CMOS," *IEEE Trans. Microw. Theory and Tech*., vol. 60, no. 10, pp. 3113–3119, Oct. 2012.

[34] Y. A. Atesal, B. Cetinoneri, and G. M. Rebeiz, "Low-Loss 0.13-µm CMOS 50–70 GHz SPDT and SP4T Switches," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig.*, Jun. 2009, pp. 43–46.

[35] C.-Y. Ou, C.-Y. Hsu, H.-R. Lin, and H.-R. Chuang, "A High-Isolation High-Linearity 24-GHz CMOS T/R Switch in the 0.18-µm CMOS Process," in *Eur. Microw. Conf*., Sep. 2009, pp. 250–253.

[36] P. Park, D. H. Shin, and C. P. Yue, "High-linearity CMOS T/R switch design above 20 GHz using asymmetrical topology and AC-floating bias," *IEEE Trans. Microw. Theory and Tech.*, vol. 57, no. 4, pp. 948–956, Apr. 2009.

[37] K. Ma, S. Mou, and K. S. Yeo, "A Miniaturized Millimeter-Wave Standing-Wave Filtering Switch With High P1dB," *IEEE Trans. Microw. Theory and Tech.*, vol. 61, no. 4, pp. 1505–1514, Apr. 2013.

[38] J. Kim and J. F. Buckwalter, “A switchless, Q-band bidirectional transceiver in 0.12-μm SiGe BiCMOS technology,” *IEEE J. Solid-State Circuits*, vol. 47, no. 2, pp. 368–380, Feb. 2012.

[39] L.-K. Yeh, C.-Y. Hsu, C.-Y. Chen, and H.-R. Chuang, “A 24-/60-GHz CMOS on-chip dual-band bandpass filter using trisection dual-behavior resonators,” *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1373–1375, Dec. 2008.

[40] H. Hashemi and A. Hajimiri, “Concurrent Multiband Low-Noise Amplifiers—Theory, Design and Applications,” *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 288–301, Jan. 2002.

[41] G. Gonzalez, *Microwave Transistor Amplifier Analysis and Design*. Upper Saddle River, NJ, USA: Prentice-Hall, 1997.

[42] S. Wang and B.-Z. Huang, "A high-gain CMOS LNA for 2.4/5.2-GHz WLAN applications," *Progress In Electromagnetics Research C*, Vol. 21, 155-167, 2011.

[43] J. Lee and C. Nguyen, “A concurrent tri-band low-noise amplifier with a novel tri-band load resonator employing feedback notches,” *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 12, pp. 4195–4208, Dec. 2013.

[44] M. Zargari *et al*., “A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g wireless LAN,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2239–2249, Dec. 2004.

[45] T. -K. Nguyen *et al*., “CMOS low noise amplifier design optimization techniques,” *IEEE Trans. Microwave Theory Tech.*, vol. 52, no. 5, pp. 1433–1442, May 2004.

[46] C. H. Doan, S. Emami, A. M. Niknejad, and R. W. Brodersen, “Millimeter-wave CMOS design,” *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144–155, Jan. 2005.

[47] H. Fouad, “An RF Cascode BJT-LNA with Shunt-series Input Matching”, URSI Twenteith national Radio Science Conference, 2003.

[48] B. Razavi, “A Millimeter-Wave CMOS Heterodyne Receiver With On-Chip LO and Divider,” *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 477–485, Feb. 2008.

[49] *SBC18H3 Design Manual*, Newport Beach, CA, USA: Jazz Semiconduct. 2013.

[50] IE3D, HyperLynx 3-D EM. Mentor Graphics, Wilsonville, OR, USA, 2013.

[51] H.-S. Jhon, I. Song, J. Jeon, H. Jung, M. Koo, B.-G. Park, J. D. Lee, and H. Shin, “8mW 17/24 GHz dual-band CMOS low-noise amplifier for ISM-band application,” *Electron. Lett*., vol. 44, no. 23, pp. 1353-1354, Nov. 2008.

[52] K. Hsieh, H. Wu, K. Tsai, and C. C. Tzuang, “A dual-band 10/24-GHz amplifier design incorporating dual-frequency complex load matching,” *IEEE Trans. Microwave Theory Tech*., vol. 60, no. 6, pp. 1649–1657, Jan. 2012.

[53] L.-W. Chu, C.-Y. Lin, and M.-O. Ker, “Design of dual-band ESD protection for 24-/60-GHz millimeter-wave circuits,” *IEEE Trans. Device and Materials Reliability*, vol. 13, no. l. pp. 110-118, Mar. 2013.

[54] J. Lee and C. Nguyen, "A Concurrent Dual-band Low-Noise Amplifier for K- and Ka-band Applications in SiGe BiCMOS Technology,” in *Microwave Conference Proceedings (APMC)*, 2013 Asia-Pacific, Nov 2013, pp. 258-260.

[55] X. Guan, H. Hashemi, and A. Hajimiri, “A fully integrated 24-GHz 8-path phased-array receiver in silicon,” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2311–2320, Dec. 2004.

[56] B. Razavi, “A 60-GHz CMOS receiver front-end,” *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17–22, Jan. 2006.

[57] Kyoungwoon Kim, “Microwave and millimeter-wave multi-band power amplifiers, power combining networks, and transmitter front-end in silicon germanium bicmos technology”, *PhD. Dissertation, Texas A&M Univ.*, May 2016.