# A LOW PHASE NOISE WIDE–TUNING RANGE CLASS–F VCO BASED ON A DUAL–MODE RESONATOR IN 65NM CMOS

A Thesis

by

NAUSHAD DHAMANI

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

| | |
|---|---|
| Chair of Committee, | Kamran Entesari |
| Committee Members, | Samuel Palermo |
| | Jun Zou |
| | Debjyoti Banerjee |
| Head of Department, | Miroslav M. Bigovic |

May 2017

Major Subject: Electrical Engineering

## ABSTRACT

A Voltage Controlled Oscillator (VCO) is a critical building block in the design of current frequency synthesizers for RF system applications. State-of-the-art operation defines that an oscillator should have the best spectral purity while consuming low amount of power for a wide tuning range.

With this in mind, this work presents a low phase noise wide tuning range Class-F VCO using a dual-mode resonator. In comparison to other conventional wideband oscillators, the proposed capacitively/inductively-coupled resonator will integrate the benefits of Class-F voltage control oscillators and dual-mode switching networks to obtain simultaneous low phase noise and wide-tuning range. The proposed structure, prototyped in 65nm TSMC CMOS technology, shows a 2.14 – 4.22GHz continuous tuning range, phase noise figure-of-merit (FoM) of 192.7dB at 2.3GHz and better than 188dB across the entire operating frequency range. The oscillator consumes 15-16.4mW from a 0.6V supply and occupies an active area of 0.7mm$^2$. In conclusion, the proposed resonator achieves 2-3dB phase noise improvement while achieving 65% overall tuning range when compared to a typical class-F VCO architecture.

**DEDICATION**

To Dad

## ACKNOWLEDGEMENTS

Every successful thesis requires the constant help and support of others. Firstly, I would like to deeply thank Dr. Kamran Entesari, my research advisor, for giving me an opportunity to work in the Analog domain and guiding me throughout the endeavor. His valuable guidance, commitment and encouragement and his patience are the reason behind the successful completion of my thesis.

I would also like to thank Dr. Samuel Palermo, Dr. Jun Zou, and Dr. Debjyoti Banerjee for serving on my committee and devoting their valuable time to review my thesis.

Being a student of Dr, Kamran Entesari, I had the pleasure of working with Masoud Moslehi Bajastan, Paria Sepidband, Ali-Abbas Pourghorban Saghati, and Vahid Dabbagh Rezaei, each of whom, have helped me in various aspects of design, layout and testing. I am indebted to them and extremely grateful for their help and guidance.

A special thanks to my parents and friends for all the inspiration, encouragement, support, love and sacrifice throughout all these years, without whom I wouldn't have been able to complete this work.

## CONTRIBUTORS AND FUNDING SOURCES

This work was supervised by a thesis committee consisting of Dr. Kamran Entesari and Dr. Samuel Palermo, and Dr. Jun Zou of the Department of Electrical and Computer Engineering and Dr. Debjyoti Banerjee of the Department of Mechanical Engineering

All work for the thesis was completed by the student, under the advisement of Dr. Kamran Entesari of the Department of Electrical and Computer Engineering.

There are no outside funding contributions to acknowledge related to the research and compilation of this document.

## TABLE OF CONTENTS

Page

## LIST OF FIGURES

Page

## LIST OF TABLES

Page

# 1. INTRODUCTION

It is well said that if Alexander Graham Bell, founding father of the first practical telephone, returns from heaven, it would be impossible for him to completely understand the way in which humankind communicates today. The past few decades has seen a stupendous growth in wireless communication. People have moved from the traditional use of landline telephones to wireless smartphones. Tablets have replaced traditional desktop computers. Today, it is possible to do more on the internet than we could have ever imagined. Your home, your car, your photographs, and your videos, everything is connected wirelessly, and can be accessed through your smart phone, within no time, irrespective of your physical location. Such high-speed data requirements forces companies to develop power-efficient multi-standard communications systems for complete customer satisfaction, which in turn accelerates their growth. These standards encompassing but not limited to GSM/3G/WIFI/LTE require frequency synthesizers occupying considerable chip area. An LC – tank based voltage controlled oscillator (VCO) is typically used in such frequency synthesizers which in turn is one of the most power-hungry blocks in an integrated transceiver. Furthermore, these synthesizers must meet the stringent spectral purity requirements for a wide spectrum of frequencies. For example, GSM TX application, demands that the VCO has a phase noise better than -162dBc/Hz at 20MHz offset frequency for a 915MHz carrier. A challenging task to achieve if concurrent extended battery life is required.

Therefore, designing an area-efficient voltage controlled oscillator (VCO) of high spectral purity with low power consumption for a wide spectrum still remains to be a challenging task in high-performance wireless communication systems. A typical configuration of a generic receiver/transmitter (transceiver) chain [1] is shown in Figure 1.

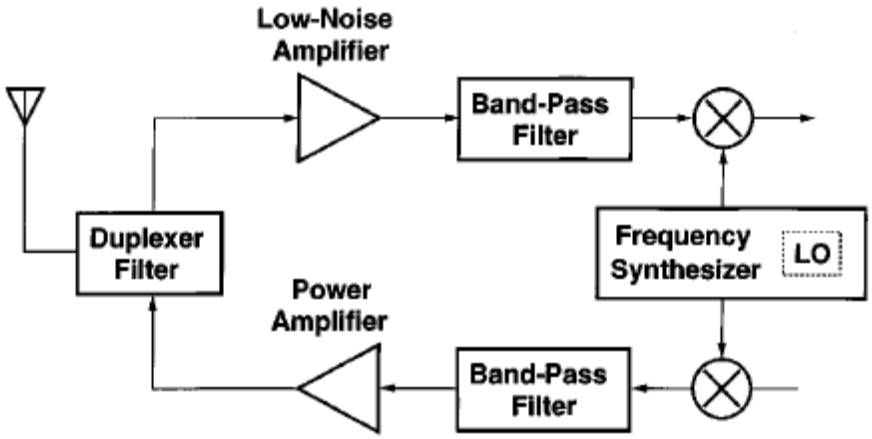



Figure 1: A common wireless transceiver system [1]

In the receiver path, an RF signal reaches the base-band by traversing the low noise amplifier, through the band-pass filter and finally crossing down-conversion mixer. In the transmitter path, the signal travels from the baseband to the antenna while passing an up-conversion mixer, band-pass filter and a power amplifier. The LO signal for the mixers is generated by the frequency synthesizers. Any phase noise in this synthesizer would corrupt both the receiver and transmitter signal. For example, the receiver path experiences reciprocal mixing, if the LO exhibits significant phase noise, i.e., the wanted signal band gets corrupted by an interferer band on down-conversion at the mixer due to LO's spectral

impurity. Similarly, on the transmitter end, amplification of the significant oscillator phase noise will desensitize a nearby noiseless receiver.

Even though, extensive research has been conducted to improve the overall performance for a high figure-of-merit (FoM) [1] – [66], one still has to dabble with the trade-offs. For example, the traditional Class-B architecture is widely prevalent in the market due to its simple and robust design. For an optimum phase noise performance, a Class-B oscillator is usually biased at the current and voltage limited boundary regions [5]. However, just by replacing the ideal current source with a real one, its phase noise (PN) and power efficiency significantly deteriorates when the cross-coupled gm- devices enter deep triode region for part of the oscillation period [5], [15].

The Class-C approach seems to be a good alternative due to its high dc-to-RF power conversion efficiency along with the prevention of gm-devices from entering the triode regions [17], [18]. Nevertheless, the latter constraint limits a Class-C to achieve its lowest possible PN performance due to a limited output voltage swing. M. Babaie et al' [34] Class-F VCO obtains a better PN with higher power efficiency but the use of varactors and switched capacitor banks limits the overall tuning range for state-of-the-art PN performance. To have a comprehensive understanding of what the problem is, let us review Leeson's phase noise equation for an LC Oscillator. Leeson's equation [8] predicts the phase noise of an oscillator as

$$L(\Delta\omega) = 10log\left(\frac{R_p k_B T}{2Q^2 V_p^2}.F.\left(\frac{f_0}{\Delta f}\right)^2\right) \tag{1.1}$$

In which F is a noise factor modelling the noise contribution of the active devices, $\Delta f$ is the frequency offset, $f_0$ is the carrier frequency, Q is the tank's equivalent quality factor, $V_p$ is the maximum oscillation voltage swing and $R_p$ is parallel resistance of the LC tank. When switched capacitors are used to improve the tuning range of an oscillator, the CMOS switches introduce parasitic capacitances, when they are OFF, which limits the frequency tuning range, or resistance when they are ON, which degrades Q and PN. Thus, to obtain a wide tuning range one needs narrow MOS switches, while low phase noise would necessitate wide ones. As a result, it becomes extremely difficult to simultaneously meet both PN and tuning range requirements. Several ideas have been proposed to alleviate this issue in Class-B VCO architectures [37] – [55]. Of one particular interest, is the use of magnetic (inductive) and electric (capacitive) coupling resonant-mode switching scheme that significantly increases tuning range without degrading PN in Class-B [54]. Such a scheme of coupling N oscillators also has the benefit of improving PN since the effective phase noise factor is reduced by a factor of N by maintaining the same FoM [25]. A class -F Oscillator implementation [34] can further reduce the effective noise factor. Thus, by proper integration of inductively/capacitively coupled resonant mode switching [54] in a Class-F operation [34], a low phase noise wide tuning oscillator can be designed.

### 1.1.Research Objective

As mentioned above, simultaneously meeting the phase noise requirements for a wide tuning range such that phase noise FoM improves or at least remains the same is a challenging task. Before we delve into solving this particular issue, first, it is vital to intuitively analyse the working of different classes of oscillators available in the market,

more importantly, their limitations to achieve low phase noise performance for a wide range of operating frequencies. Second, understanding the operation of various wide-band oscillators topologies at our disposal is also required to obtain the most optimal integration of the state-of-the-art oscillators.

With this in mind, a dual-mode resonator has been proposed to integrate the advantages of resonant-mode switching with Class-F operation to achieve simultaneous wide-tuning range and low phase noise performance. The primary objective of this thesis would be to design, implement and finally test the functionality of the proposed wide-band Class-F VCO.

### 1.2.Thesis Organization

Following the introduction, Section 2 briefly presents and discusses different classes of oscillators and their fundamental limitations, specifically highlighting the requirements of wideband oscillators.

Section 3, discusses the proposed low phase noise wide-tuning range Class-F based on a dual-mode resonator. This section will illustrate the working of a Class-F structure followed by the design and implementation of the dual-mode resonator and the transistor switching network.

Section 4, provides measurement results of the fabricated wide-band VCO followed by a comparison between different state-of-the-art oscillator topologies, and

Section 5, presents the conclusion of the thesis.

## 2. LC OSCILLATOR ARCHITECTURES

The voltage controlled oscillator is a key block used in GSM/WCDMA/LTE frequency synthesizers, where phase noise requirements are demanding and the oscillator as such is one of the most power-hungry blocks [1], [2] and [3]. For this reason, VCO research has gained momentum to introduce different topologies. aimed at improving phase and frequency tuning range while reducing power consumption. Therefore, understanding and modelling phase noise is crucial for improving overall system efficiency.

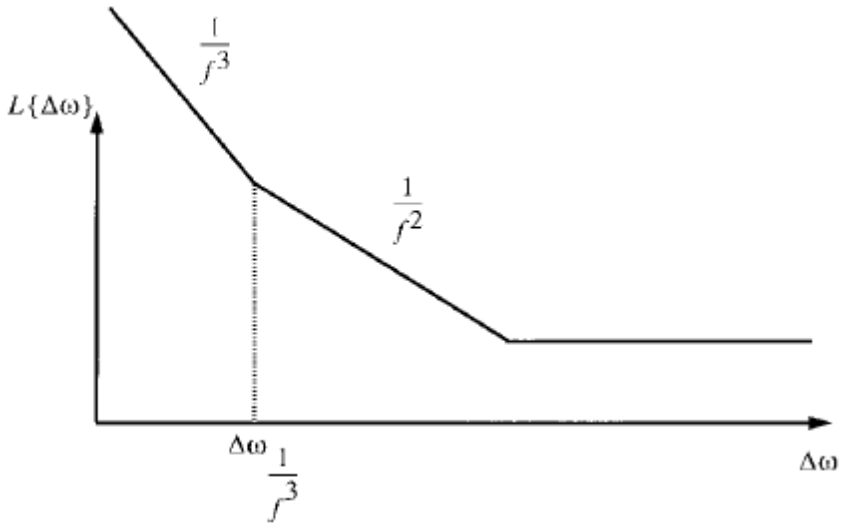



Figure 2: Phase noise of an oscillator vs. carrier offset Δω [7]

Various studies have been conducted to model phase noise of an oscillator [4] – [15]. Figure 2. demonstrates the plot of phase noise of an oscillator versus carrier offset Δω. The Leeson-Cutler phase noise model is an LTI model for a tank oscillator given by

$$L\{\Delta\omega\} = 10.log\left\{\frac{2FkT}{P_s}.\left[1 + \left(\frac{\omega_0}{2Q_L\Delta\omega}\right)^2\right].\left(1 + \frac{\Delta\omega_{1/f3}}{|\Delta\omega|}\right)\right\} \quad (2.1)$$

where $F$ is the device noise factor, T is the absolute temperature, $k$ is Boltzmann′s constant, $P_s$ is the average power dissipated by the resistor, $Q_L$ is the loaded quality factor of the tank, and $\omega_{1/f^3}$ is the $1/f^3$ and $1/f^2$ regions corner frequency, shown in Figure 2. $F$ and $\omega_{1/f^3}$ are empirical parameters which are occasionally known during the initial oscillator design. $F$ represents noise contributed by the active transistors in the oscillator. Equation (2.1) accurately models the graph shown in Figure 2, if F and$\omega_{1/f^3}$ are accurately known. However, such a scenario is seldom possible since F does not incorporate the nonlinear frequency conversion effects and $\omega_{1/f^3}$ is not same as the $1/f$ device noise corner. Accurate predictions of phase noise using Leeson's equations have been restricted to relatively high Q, discrete oscillator designs.

One widely accepted and mostly accurate approach, is the use of a linear time variant model which introduces the concept of an impulse sensitivity function (ISF) for each noise source of an oscillator [7]. As shown in Figure 3, if a current impulse is injected into a tank, it can change the oscillation amplitude and/or phase depending on when the impulse was injected. Injecting an impulse at the peak, would result in only oscillation amplitude change. However, if a current impulse is injected at the zero crossing, it would have maximum effect on the phase with minimum amplitude disturbance.

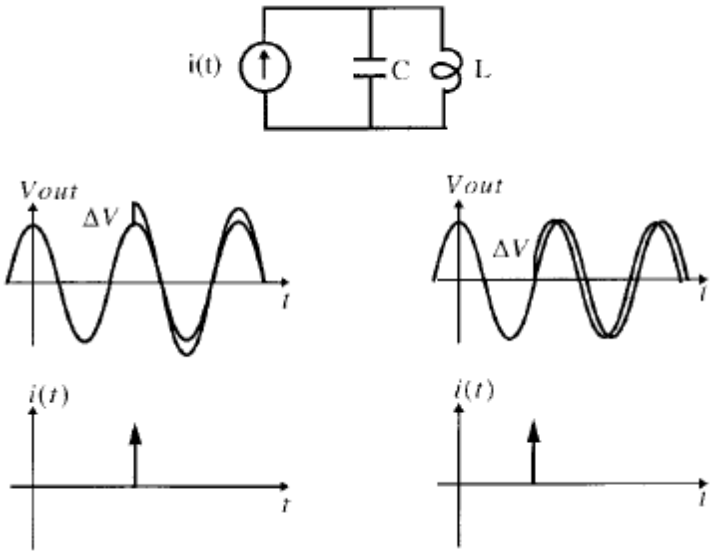



Figure 3: Amplitude and phase response to an injected current [7]

The impulse response is a periodic function whose amplitude depends on the time when the current is injected. The unit impulse response for a step function is defined as

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau) \tag{2.2}$$

where $\Gamma(\omega_0\tau)$ is the impulse sensitivity function, due to its periodic nature, can be defined as

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n) \tag{2.3}$$

and $q_{max}$ is the maximum charge displacement across the capacitor on the node where the impulse was injected. ISF is a dimensionless, frequency and amplitude independent periodic function with a period of $2\pi$ that describes the oscillator phase shift caused by introducing an impulse at $t= \tau$. It is an oscillator-waveform dependent function. The

oscillator waveform is in turn depended on the nonlinearities and the topology of the oscillator. The excess phase is then calculated by convolving the ISF with any current source, $i(t)$, as

$$\phi(t) = \frac{1}{q_{max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(n\omega_0\tau)\,d\tau\right] \tag{2.4}$$

Eqn. (2.4) suggests that $\phi(t)$ can be calculated for any random current source $i(t)$ inserted into any circuit node. Consequently, if we inject a current $i(t) = I_n \cos[(n\omega_0 + \Delta\omega)\,t]$ close to any integral multiple of the oscillation frequency, the excess phase is approximately given by

$$\phi(t) \approx \frac{I_n c_n \sin(\Delta\omega t)}{2q_{max}\Delta\omega} \tag{2.5}$$

This excess phase would show itself in the sideband power spectrum relative to the carrier. Therefore, an injected current $i(t)$ at $n\omega_0 + \Delta\omega$ would result in two equal sidebands at $\omega_0 + \Delta\omega$ with the sideband power calculated as

$$P_{SBC}(\Delta\omega) = 10.\log\left(\frac{I_n c_n}{4q_{max}\Delta\omega}\right)^2 \tag{2.6}$$

The above method can be utilized for the case of random input current noise sources $i_n(t)$, to obtain the phase noise for a white power spectral density, $\overline{\imath_n^2}/\Delta f$, given by

$$L(\Delta\omega) = 10.\log\left(\frac{\Gamma_{rms}^2}{q_{max}^2}.\frac{\overline{\imath_n^2}/\Delta f}{4.\Delta\omega^2}\right) \tag{2.7}$$

where $I_n^2/2 = \overline{i_n^2}/\Delta f$ , since $I_n$ in Eqn. (2.6) represents the peak amplitude, and $\Gamma_{rms}$ is the rms value of Γ(x), given by

$$\Gamma_{rms}^2 = \frac{1}{2\pi}\int_0^{2\pi} |\Gamma^2(x)|^2 dx \tag{2.8}$$

In order to obtain the $\Gamma_{rms}^2$ of each noise source, the most accurate methodology would be to directly calculate ISF of each noise source from their impulse response simulations. First, an impulse current is injected at the node of interest at a certain time. Second, the time shift is measured after a few cycles, which then, is converted to its phase shift and finally, by sweeping the injection time over one oscillation cycle, the ISF can be calculated.

For a typical LC-tank based oscillator, the phase noise is given by [18]

$$L(\Delta\omega) = 10log\left(\frac{R_p k_B T}{2Q^2 V_p^2}.F.\left(\frac{f_0}{\Delta f}\right)^2\right) = 10\log\left(\frac{k_B T}{2Q^2\alpha_I\alpha_V P_{DC}}.F.\left(\frac{f_0}{\Delta f}\right)^2\right) \tag{2.9}$$

where Δ f is the frequency offset, $f_0$ is the carrier frequency, Q is the tank's equivalent quality factor, $V_p$ is the maximum oscillation voltage swing, $P_{DC}$ is power consumption, $R_p$ is parallel resistance of the LC tank, $\alpha_I = I_{\omega 0}/I_{DC}$ and $\alpha_V = V_p/V_{DC}$ are the current and voltage efficiencies and F is the noise factor.

Before comparing different LC oscillator structures, let us define a simple phase noise figure of merit to fairly compare different VCO topology performances. The FoM metric given by (2.10) normalizes the phase noise performance to the power consumption and oscillation frequency. Therefore, by reducing the phase noise and power consumption can significantly improve the overall FoM of the oscillator.

$$FoM = 10\log_{10}\left[\frac{1}{P_{DC|\,mW}}\left(\frac{f_0}{\Delta f}\right)^2\right] - L(\Delta f) \tag{2.10}$$

For a typical LC tank-based oscillator, the phase noise reduces by increasing the tank's quality factor, In the vicinity of resonance, the overall tank quality factor is given by

$$\frac{1}{Q} = \frac{1}{Q_C} + \frac{1}{Q_L} \tag{2.11}$$

where $Q_L$ is the inductor's quality factor which is predominately technology dependent and doesn't improve with CMOS scaling. On the other hand, $Q_C$ trade's- off with the tuning range of the oscillator. For example, a switch capacitor bank, typically used for tuning, entails a large width for the MOS switches to reduce the switch's on-resistance which although improves the phase noise, reduces the tuning range of the oscillator due to increased parasitic capacitance when the switch is off.

Another approach to improve phase noise is to trade power for phase noise by reducing the tank's inductance L while keeping the $Q_L$ constant. For example, if L is reduced by half, $R_p = 2\pi Q_L L$, reduces by half which lowers PN by 3dB but doubles power consumption ($P_{DC}$), where $P_{DC}$ is given by

$$P_{DC} = \frac{V_p^2}{\alpha_I \alpha_V R_p} \tag{2.12}$$

### 2.1. Class-B Oscillator

A traditional Class-B oscillator has become a dominant choice in real life applications due to its simple and robust design. Figure 4 shows a simple NMOS Class-B

oscillator topology where in the negative Gm presented by the two ross-coupled NMOS transistors cancel the loss of the LC tank in order to sustain periodic oscillations at resonance. In other words, the Barkhausen criterion for oscillation i.e., unity feedback loop-gain and 360-degree phase shift, is satisfied. The placement of tail current source $M_T$ provides additional flexibility to the designer in order for them to obtain the best FoM.

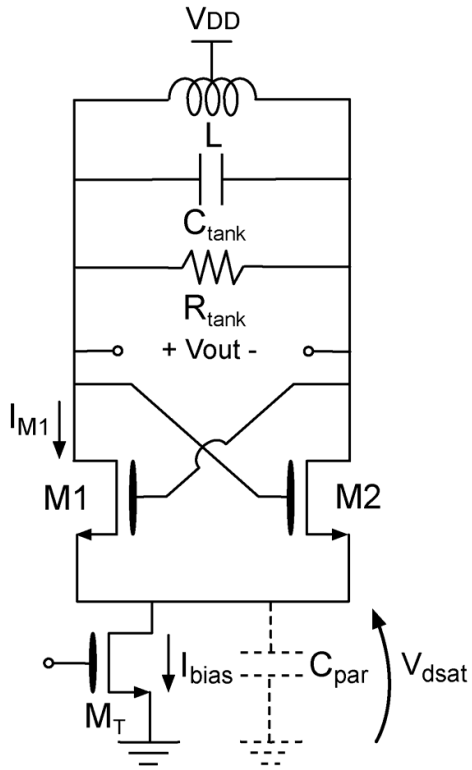



Figure 4: Traditional Class-B VCO [18]

For an ideal case, the Class-B oscillator has a noise factor of 1+ ϒ [11]. This value is based on the assumption that the current source $M_T$ is ideal i.e., noiseless and provides high impedance for the complete oscillation period. However, in reality, the oscillator's

maximum voltage amplitude has a trade -off with the noise contribution of $M_T$. Consequently, affecting the best possible PN performance (Figure 5)

A typical Class-B structure shows best PN performance when it operates in the boundary of voltage and current limited regime [14], [15], and [22] i.e., $\alpha_V = 1$, and $\alpha_I = 2/\pi$. However, for a non-ideal current source, $\alpha_V$ is much lower than 1, due to the minimum $V_{dsat}$ required to keep $M_T$ in saturation. A large $M_T$ can increase $\alpha_V$ but at the cost of a higher noise contribution. The overall phase noise for a typical Class-B is given by

$$L(\Delta\omega) = -10log\left[\frac{k_B T}{2Q^2\alpha_I\alpha_V}(\gamma + 1 + \eta\gamma_T gm_T R_p)\right] \tag{2.13}$$

in which $\gamma(\gamma_T)$ are the channel noise factor for $M_1$-$M_2$ ($M_T$), $\eta$ is an oscillation amplitude depended factor and $gm_T$ is $M_T$ transconductance.

The parasitic capacitance $C_{par}$ at the common source of $M_1$ and $M_2$ (Figure 6) also reduces the current efficiency when $M_1$-$M_2$ enter the triode region. Since $C_{par}$ tends to maintain a constant common source voltage, the current consumption experiences a dimple (as shown in Figure 6) which reduces $\alpha_I$ from the ideal $2/\pi$ value. Furthermore, to reduce the $1/f^3$ phase noise corner, $M_T$ should be large. Therefore, $C_{par}$ creates a discharge path to ground when $M_1$-$M_2$ enter deep triode, dramatically degrading the tank Q and thus, phase noise.

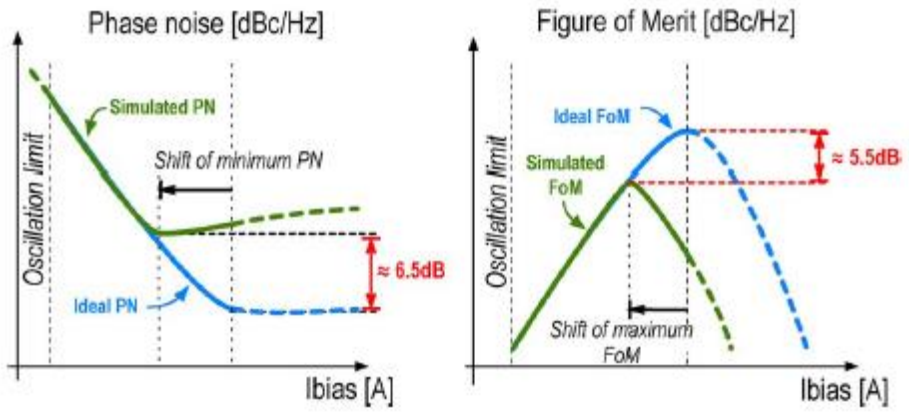
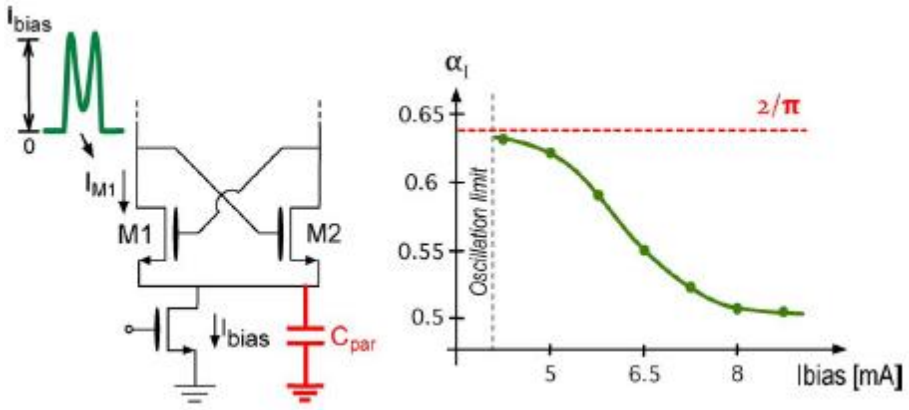



Figure 5: Phase Noise and FoM comparison between ideal and real Class-B VCOs [18]




(a) (b)

Figure 6: (a) Effect of tail parasitic capacitance $C_{par}$ on current waveform; (b) current efficiency $\alpha_I$ vs. bias current [18]

Various solutions have been proposed to improve the phase noise of a Class-B oscillator. Subsequently, new classes of oscillators have been proposed to improve trade-offs between power consumption and phase noise. The noise filtering technique proposed in [16] is another interesting technique to improve phase noise. In this technique, an inductor is placed between $M_1$ – $M_2$ and $M_T$ which resonates with $C_{par}$ at twice the

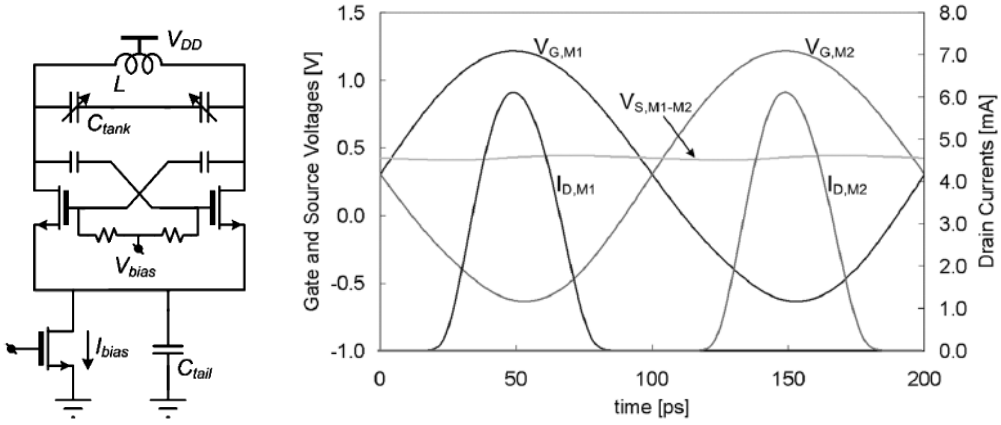
oscillation frequency. Thus, the structure preserves the intrinsic Q of the tank by creating a high impedance path. However, using an extra resonator significantly increase the die area, complexity and cost. In the following sections, we review other classes of oscillators which try to minimize the phase noise/ power consumption trade-off.

### 2.2. Class-C Oscillator

A Class-C oscillator [17] is shown in Figure 7(a). To obtain, the best phase noise performance, the core transistors should always remain in saturation for the entire oscillation period. Moreover, use of low $V_{bias}$ and a large current source shunt capacitance ($C_{tail}$) ensures that the drain currents of $M_1$- $M_2$ are composed of narrow and tall pulses, resulting in $\alpha_I$ close to 1. (Figure 7(b)), while maximizing the oscillation amplitude. Furthermore, since a large $C_{tail}$ naturally filters out high frequency noise, a large $M_T$ can be used to increase oscillation amplitude, further increasing $\alpha_V$. However, a very large shunt capacitance may result in squegging i.e., modulation of oscillation amplitude [17]. The expression for $C_{tail}$ is derived as,

$$C_{tail} = \frac{6}{k}.\frac{\sin(\phi) - \phi\cos(\phi)}{\sin^3(\phi)}.C_{tank} \tag{2.14}$$

where, k represents the voltage gain from the tank to the MOS gate and $\phi$ is the current conduction angle. Assuming a practical value of k = 1, and $\phi = 1$ would allow the choice of $C_{tail} = 3C_{tank}$. Whereas, even for the limiting case of $\phi = 0$, will allow $C_{tail} = 2C_{tank}$, a reasonable value to avoid squegging. Therefore, proper choice of $C_{tail}$ is one of the critical aspects of this design.




(a) (b)

Figure 7: (a) Class-C VCO; (b) it's voltage and current waveforms [17]

The phase noise expression for a typical Class-C VCO [17], can be calculated as

$$L(\Delta\omega) = 10\log\left(\frac{k_B T}{2\Delta\omega^2 C^2 I_{bias}^2 R^2}\left(\frac{1}{R}+\frac{\gamma}{k}.\frac{1}{R}\right)\right) \quad (2.15)$$

This phase noise expression shows that a Class-C structure benefits with 36% power saving in comparison to a typical Class-B having the same phase noise performance. In other words, for the same power consumption, theoretically, a Class-C topology can achieve 3.9dB PN improvement when compared to a Class-B VCO. Nevertheless, the constraint of $M_1$- $M_2$ to remain in saturation limits the maximum oscillation amplitude to $V_{DD}/2$, if the transistors are biased close to the threshold voltage, translating to 6dB phase noise penalty [34].

Furthermore, if the transistors enter triode, $\alpha_I$ drastically deteriorates, resulting in poor PN performance. Several attempts have been made to resolve this issue [18] – [24]. Of one particular interest is the use of dynamically biased Class-C VCO (Figure 8). In

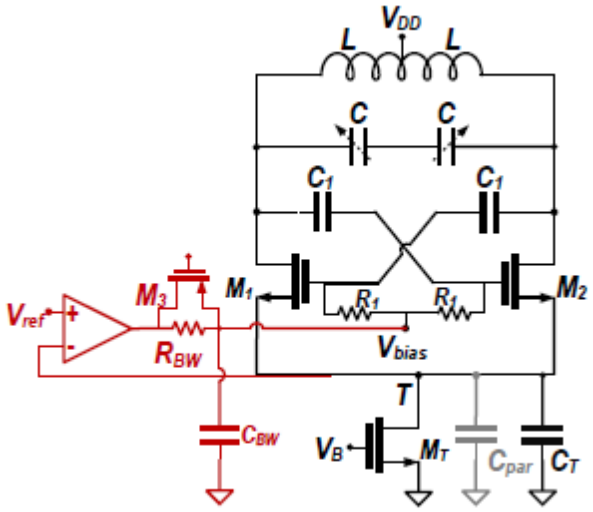



Figure 8: (a) Class-C VCO with dynamic generation of $V_{bias}$ [18]

this topology, $V_{bias}$ is dynamically adjusted in a negative feedback loop to ensure a robust start-up, while keeping $\alpha_I$ close to 1 at steady states, maximizing the oscillation amplitude [18].

The bandwidth and the DC gain of the operational amplifier decides the stability, settling time and the steady state error between the common mode voltage and the reference voltage. Additionally, the op-amp AM-to-PM noise conversion is suppressed due to the high impedance seen at the current source at low frequencies [16], if the oscillator operates in a Class-C manner. Therefore, the current consumption of the operation amplifier can be made negligible small, compared to $M_T$ current bias.

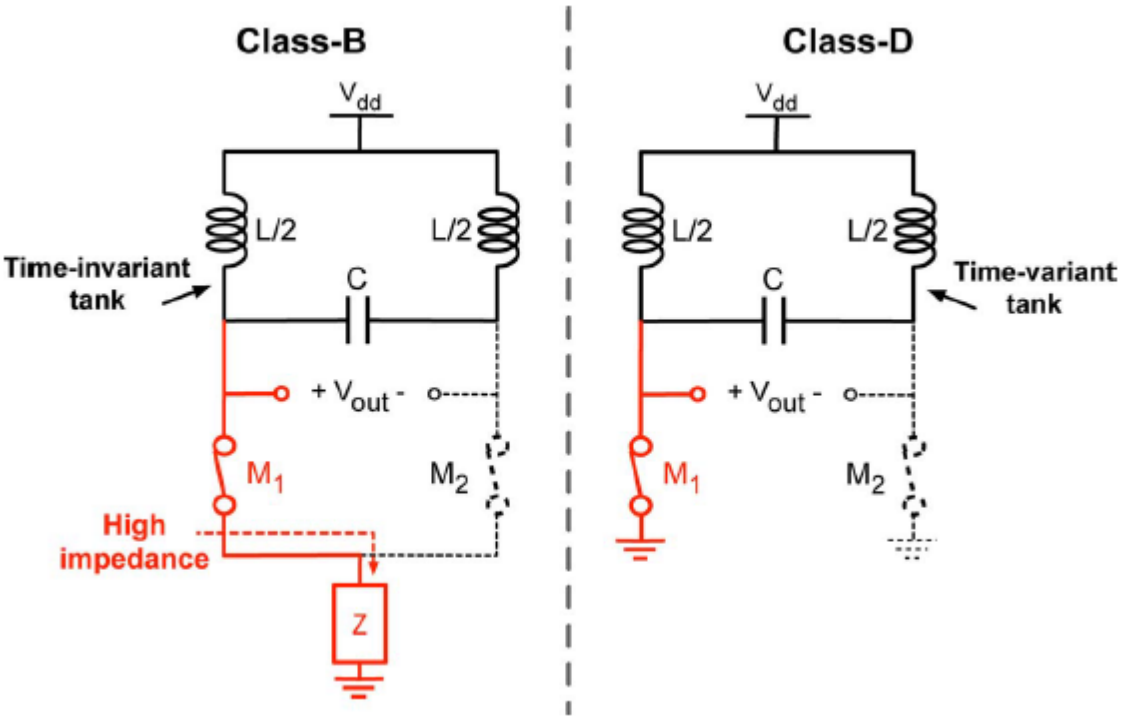



Figure 9: Class-B vs. Class-D oscillator tank comparison [27]

### 2.3. Class-D Oscillator

The dramatic scaling of CMOS technology has dropped the maximum voltage that MOS devices can handle without undergoing breakdown which even though saves power, makes it difficult to achieve a good phase noise performance. The overdrive voltage consumed by the current source of Class-B VCO limits the maximum oscillation amplitude, which for a lower supply voltage would make it impossible to obtain the desired phase noise level. A Class-D oscillator is a good alternative for low supply voltage design. A Class-D VCO makes it possible to combine low phase noise, low supply

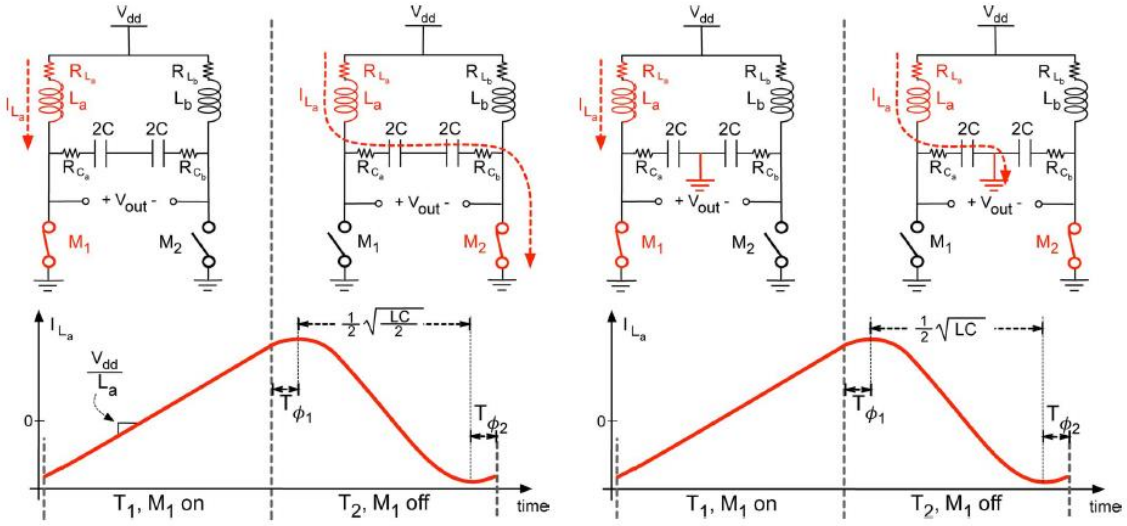



Figure 10: Time-domain analysis of (a) floating tank; (b) single-ended tank [27]

voltage, and high efficiency simply by increasing the size of cross-coupled MOS switches of a typical Class-B VCO [27].

It is interesting to note that Class-D oscillator topology was first proposed in 1959 by Baxandall [30] but its development was stalled in RF applications due to the unavailability of MOS switches with acceptable parasitic capacitance and excellent conductance, which the current CMOS technologies have begun to offer. The operation of a Class-D LC tank is shown in Figure 9. The LC tank in a Class-D behaves quite differently when compared to a Class-B LC tank. As can be seen, a Class-D tank displays a time varying nature which differentiates it from the time invariant Class-B LC tank. While in a Class-B, the capacitor and inductor are always parallel to each other for the complete oscillation period, in a Class-D tank, the switches $M_1$-$M_2$, by virtue of shorting the output to ground, decouples the respective inductor and capacitor for half of the oscillation period.

This time variant nature of the tank, as seen in Figure 10, makes a Class-D oscillator exhibit two different oscillation frequencies, $\omega_{osc,\ float}$ and $\omega_{osc,\ se}$ depending on whether the tank capacitance behavior is floating or single ended.

The oscillation frequencies are given by

$$\omega_{osc,se} = \frac{1}{\alpha}\sqrt{\frac{1}{LC}} \qquad \omega_{osc,float} = \frac{\sqrt{2}}{\alpha}\sqrt{\frac{1}{LC}} \tag{2.16}$$

where the calculated α is approximately equal to 1.3. Detailed analysis can be found in [13]. Therefore, in real-life scenarios, the Class-D VCO actual frequency of operation will be in between these two oscillations, combining the floating tank capacitance with the parasitic capacitance of $M_1/M_2$ switches to ground.

The peak amplitude of this topology is given by,

$$V_p = V_{DD}\left(1 + \sqrt{\frac{\alpha^2\pi^2}{4} + 1}\right) \approx 3.27\ V_{DD} \tag{2.17}$$

which shows that the oscillation amplitude is approximately three times the supply voltage, necessitating a low supply voltage for the safety of MOS switches. Such high $V_p$ has the advantage of forcing the large $M_1/M_2$ switches to ground. Thus, eliminating the large phase noise generated by theses switches to be up-converted to phase noise due to an almost zero ISF i.e., the ISF waveform is shaped to reduce the overall noise to phase noise conversion when $M_1 – M_2$ enter triode. Furthermore, this behavior also improves the power efficiency to go beyond 90% [27] making it suitable for low power low phase noise applications [28], [29]. Nevertheless, such a low VDD would entail higher supply frequency pushing [27].

The simplified current consumption and phase noise expressions for floating and single ended capacitance cases are

$$L_{C_{float}}(\Delta\omega) \approx 10\log\left[\frac{\omega_{osc,float}^2}{\Delta\omega^2}\frac{k_B T}{V_{DD}^2}(0.104R_L + 0.141R_C)(1+\gamma_{MOS})\right]$$

$$L_{C_{se}}(\Delta\omega) \approx 10\log\left[\frac{\omega_{osc,se}^2}{\Delta\omega^2}\frac{k_B T}{V_{DD}^2}\left(0.104R_L + \frac{0.141}{2}R_C\right)(1+\gamma_{MOS})\right]$$

$$I_{DC,float} \approx (7.1 - 2.0k)\frac{(R_C + R_L)V_{DD}}{\omega_{osc,float}^2 L^2}$$

$$I_{DC,se} \approx (3.6 + 1.6k)\frac{(R_C + R_L)V_{DD}}{\omega_{osc,se}^2 L^2} \quad (2.18)$$

where $R_L$ and $R_C$ are the inductive and capacitive losses, and $k = \frac{R_L}{R_C+R_L}$. From the above equations, it can be seen that implementing a floating capacitance Class-D tank can achieve lower current consumption, lower PN (individual contributions of $R_C$ and $\gamma_{MOS}$ is different for single-ended and floating capacitance implementations) and higher oscillation frequency when compared to a single-ended implementation. However, such an implementation is not always possible.

Thus, sensitivity to supply voltage plus the specific implementation of floating capacitance tank, makes a Class-D design a challenge in itself. Although, an on chip LDO implementation in [31] tries to mitigate this problem but doings so, increase the overall power consumption. Therefore, a solution has yet to be found to use Class-D for practical applications.

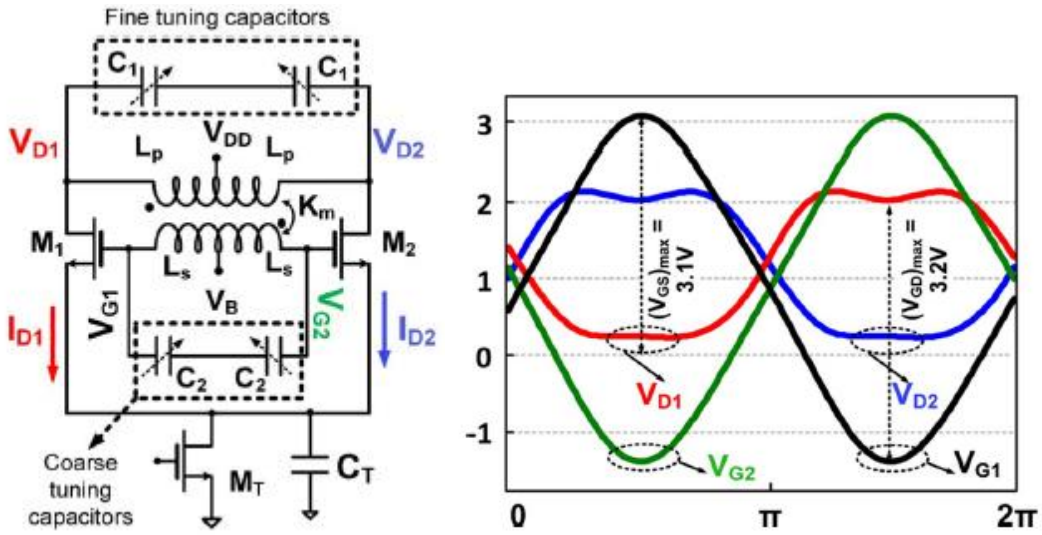



Figure 11: (a) Class-$F_3$ VCO design (b) it's oscillation voltage waveforms [34]

### 2.4. Class-F Oscillator

If ISF of a certain oscillation voltage waveform is minimal for a certain interval of an oscillation period due to the zero derivative of the oscillation voltage, the circuit noise does not up-convert to phase noise during that interval. Thus, reducing the oscillator phase noise. This is the concept behind Class-F oscillators design, where oscillator waveforms are shaped by injecting second or third order harmonics of the fundamental frequency to reduce phase noise.

#### 2.4.1. Class-$F_3$ Oscillator

As the name suggest, a Class-F oscillator (Figure 11) enforces a pseudo square wave waveform across the LC tank ($V_{D1}$-$V_{D2}$) by self-injecting a third harmonic at the fundamental oscillation voltage ($\omega_1$) through an additional impedance peak at that frequency. $L_p$, $L_s$, $C_2$, $C_1$ correspond to the respective primary and secondary inductance

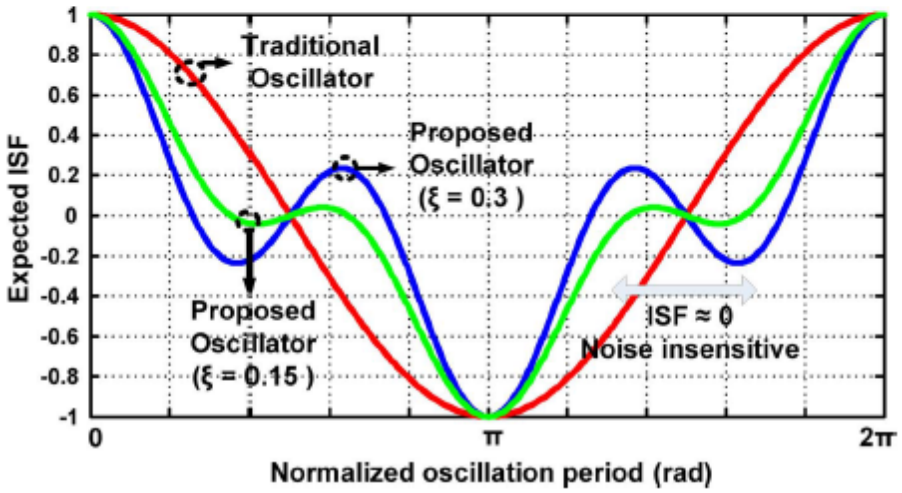



Figure 12: ISF function of a Class-F VCO [34]

and capacitance. Figure 12 illustrates the respective ISF for various ξ values, where ξ is defined as the magnitude ratio of the third-to-first harmonic oscillation voltage component given by

$$\xi = \frac{V_{p3}}{V_{p1}} = \left(\frac{R_{p3}}{R_{p1}}\right)\left(\frac{I_{DH3}}{I_{DH1}}\right) \approx 0.33\left(\frac{R_{p3}}{R_{p1}}\right) \tag{2.19}$$

For $V_{in} = V_{p1}\sin(\omega_0 t) + V_{p3}\sin(3w_0 t + \Delta\phi)$. In which, $R_{p3}$ and $R_{p1}$ represent the first and third harmonic impedance peaks for first and third harmonic currents $I_{DH3}$ and $I_{DH1}$ respectively and the ISF rms value, for $-\frac{\pi}{8} < \Delta\phi < \frac{\pi}{8}$ is estimated as,

$$\Gamma_{rms}^2 = \frac{1}{2}\frac{1+9\xi^2}{(1+3\xi)^2} \tag{2.20}$$

The square waveform has sharper zero crossings and flatness when the transistor turns on/off respectively, which effectively reduces the rms value of the ISF and noise

contribution to the phase noise. The third harmonic voltage is realized by introducing another impedance resonant peak at $\omega_2 = 3\omega_0$ such that filtering of third harmonic drain current is prevented. A separate LC resonator could be used for the $3\omega_0$ realization [32]. However, such an implementation increase area and cost of the oscillator. M. Babaie et al. [34] presents an alternative to implement such a peak by using a transformer (Figure 11). The input impedance of a transformer based tank has two resonant peaks whose ratio is given by

$$\frac{\omega_2}{\omega_1} = \sqrt{\frac{1 + X + \sqrt{1 + X^2 + X\,(4k_m^2 - 2)}}{1 + X - \sqrt{1 + X^2 + X\,(4k_m^2 - 2)}}} \tag{2.21}$$

where,

$$X = \left(\frac{L_s}{L_p} \cdot \frac{C_2}{C_1}\right) \tag{2.22}$$

If properly designed, a transformer can show the second peak at the third harmonic point, resulting in a pseudo square waveform. Reiterating Eqn. (2.9), the phase noise of an oscillator is expressed as

$$L(\Delta\omega) = 10log\left(\frac{R_p k_B T}{2Q^2 V_p^2} . F . \left(\frac{f_0}{\Delta f}\right)^2\right) \tag{2.23}$$

where the effective tank quality factor at the fundamental resonance point, Q, of the resonator having primary and secondary quality factor, $Q_p$ and $Q_s$, is derived as,

$$Q = \frac{(1 + X^2 + 2k_m X)}{\left(\frac{1}{Q_p} + \frac{X^2}{Q_s}\right)} \tag{2.24}$$

and maximum oscillation voltage amplitude is calculated as,

$$V_p = \left(\frac{1}{3} + \xi\right)\sqrt{\left(1 + \frac{1}{3\xi}\right)}.\alpha_I.R_p.I_B, \quad \frac{1}{9} \le \xi \le 1$$

$$V_p = (1 - \xi).\alpha_I.R_p.I_B, \quad 0 < \xi \le \frac{1}{9} \tag{2.25}$$

The effective noise factor for a general Class-F, B, C oscillator calculated using [7] linear time variant model can be expressed as,

$$F = 2\Gamma_{rms}^2.\left(1 + \frac{\gamma}{A}\right).\left(1 + R_p G_{DS\_EF}\right) \tag{2.26}$$

in which, A is the voltage gain of the feedback path from the tank ($V_{D1}$) to the MOS gate ($V_{G2}$) in Figure 11. $G_{DS1EF}$ is the effective drain-source transconductance of $M_1/M_2$ expressed as

$$G_{DS\_EF} = G_{DS}[0] - G_{DS}[2] \tag{2.27}$$

where $G_{DS}[k]$ represents the $k_{th}$-order Fourier coefficient of the instantaneous conductance $G_{ds}(t)$ [11], and $\gamma$ is the effective channel noise factor proving that a change in $\Gamma_{\mathrm{rms}}^2$ can significantly improve the overall phase noise performance.

In summary, a choice of 0.3 for $\xi$ results in a 3dB phase noise reduction, when compared to a traditional Class-B VCO. At the same time, a high voltage and current efficiency equal to $\alpha_V = 0.8$ and $\alpha_I = 2/\pi$ can also be obtained. Table I summarizes a performance comparison of Class-B, dynamically biased Class-C [18], and Class-$F_3$ VCO.

Table I: Comparison of different oscillator classes for the same $V_{DD}$ (1.2V), Tank Q-Factor (15), $R_p$ (220Ω), and carrier frequency (7GHz) at 3MHz offset frequency [34]

| | Theoretical expression | Class-B | Dynamic biased Class-C | Class-$F_3$ |
|---|---|---|---|---|
| F(dB) | $F = 2\Gamma_{rms}^2 \cdot \left(1 + \frac{\gamma}{A}\right) \cdot \left(1 + R_p G_{DS\_EF}\right)$ | 5.5 | 3.9 | 2.8 |
| $\alpha_I$ | $I_{\omega 0}/I_{DC}$ | 0.55 | 0.9 | 0.63 |
| $\alpha_V$ | $V_p/V_{DD}$ | 0.8 | 0.7 | 0.8 |
| PN (dBc/Hz) | $L(\Delta\omega) = 10log\left(\frac{R_p k_B T}{2Q^2 V_p^2} . F . \left(\frac{f_0}{\Delta f}\right)^2\right)$ | -133.5 | -134 | -136 |
| FoM (dB) | $L(\Delta\omega) = -10log\left(\frac{10^3 k_B T}{2Q^2 \alpha_I \alpha_V} . F . \left(\frac{f_0}{\Delta f}\right)^2\right)$ | 191.2 | 194.5 | 194.2 |

### 2.4.2. Class-$F_2$ Oscillator

Class-$F_2$ (shown in Figure 13) [36, 59] is yet another interesting topology where even though the MOS switches ($M_1$ – $M_2$) go into triode, the ISF is negligible due to the oscillation voltage waveform shaping, resulting in better phase noise performance compared to Class-B. This topology is realized by enforcing a second harmonic voltage over the fundamental harmonic oscillation to have sharper zero crossings. The even harmonics appear as a common mode input for the tank and odd harmonics appear as differential mode input.

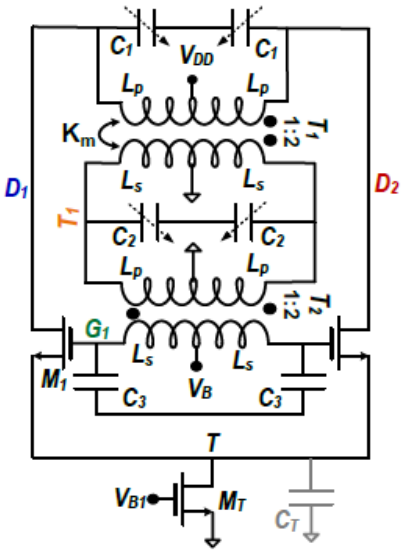



Figure 13: Schematic of a Class-$F_2$ VCO [36]

Fig. 14 illustrates the oscillation voltage and its respective ISF for various $\xi_V$ values, where $\xi_V$ is defined as the magnitude ratio of the second-to-first harmonic oscillation voltage component given by

$$\xi_V = \frac{V_{p2}}{V_{p1}} = \left(\frac{R_{CM}}{R_{in}}\right)\left(\frac{I_{DH2}}{I_{DH1}}\right) \tag{2.28}$$

In which, $R_{CM}$ and $R_{in}$ are the common mode ($2\omega_0$) and differential mode ($\omega_0$) input impedance respectively. Choosing $\xi_V$ = 0.3 has a 1.5dB phase noise improvement when compared to a Class-B oscillator due to decrease in the ISF rms value of the tank. Such an oscillator is implemented by using a back-to-back connected transformer as illustrated in Fig 13. A high voltage and current efficiency comparable to an ideal Class-B VCO can be achieved with $\alpha_V$ = 0.9 and $\alpha_I = 2/\pi$. Moreover, using a 1:2 back -to-back transformer

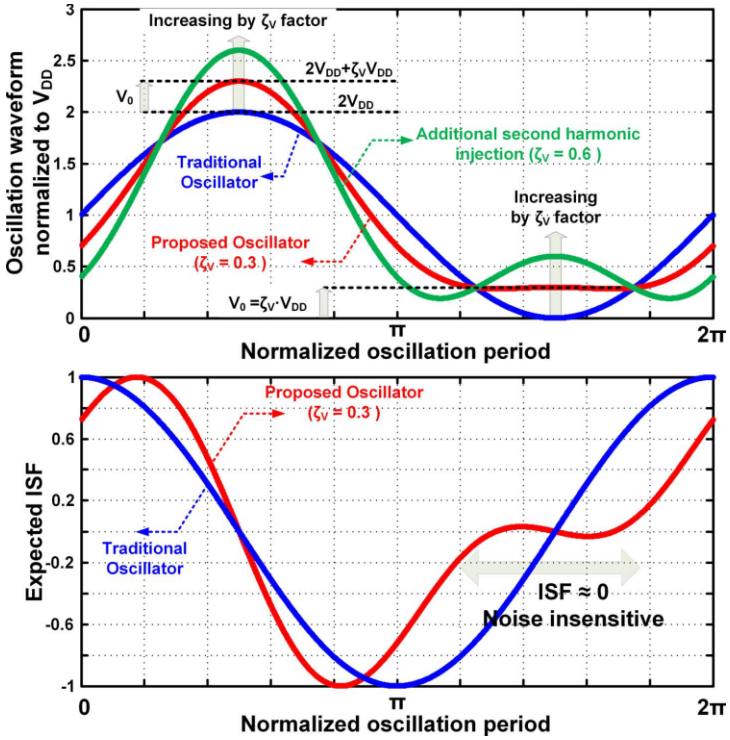



Figure 14: Effect of adding 2nd harmonic to the oscillation voltage waveform(top) and its respective ISF (bottom) [36]

scales down the input impedance of the tank which results in a phase noise improvement by a factor of 5 at the cost of higher power such that the FoM remains same, when compared to a Class-B. However, such an implementation requires larger area.

### 2.5. Wideband Oscillators

In all the previous VCO structures discussed before, our main focus was on improving the phase noise with little regard to the oscillator's frequency tuning range. However, current standards for various RF applications necessitate the need for simultaneous low phase noise and wide tuning range. Several studies have been conducted to operate oscillators for multiple frequency bands without impairing phase noise [37-55].

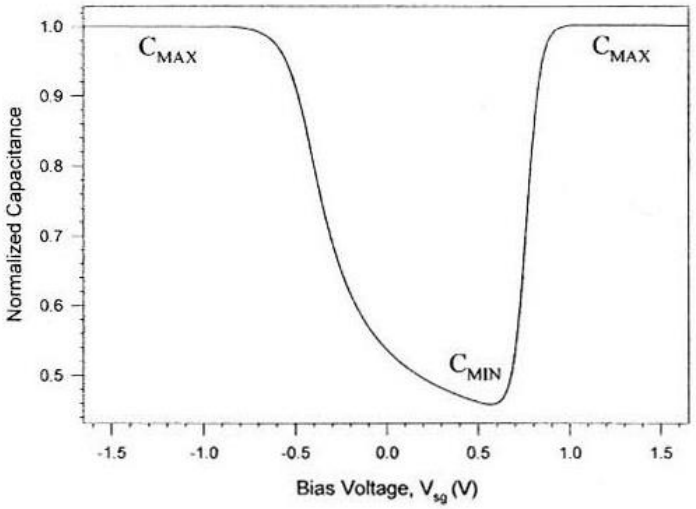



Figure 15: C-V characteristic plot of a typical pMOS varactor [52]

Phase noise-tuning range trade-off limits the use of varactors without degrading the stringent phase noise requirement [37]. A typical C-V characteristic of a MOS varactor is shown in Figure 15 [52]. As seen from the plot, a typical MOS varactor shows a large VCO gain ($K_V$ Hz/V). This maximum-to minimum capacitance ratio of the varactor ( $C_{max}/\ C_{min}$ ) determines the complete tuning range of a cross-coupled VCO which is limited to at-most 30% for a standard CMOS process [38 – 40]. Additionally, varactors show a 20% capacitance process variation. Therefore, a large $K_V$ is advantageous to incorporate such process spreads. However, abrupt voltage fluctuations on the control terminal modulate the VCO frequency, resulting in increased phase noise [1]. Thus, increasing $K_V$ would further raise phase noise demonstrating the tuning range-phase noise trade-off.

The employment of a switch capacitor bank in an LC-resonator makes an effort to improve tuning range by reducing the VCO gain. However, trade-off between power

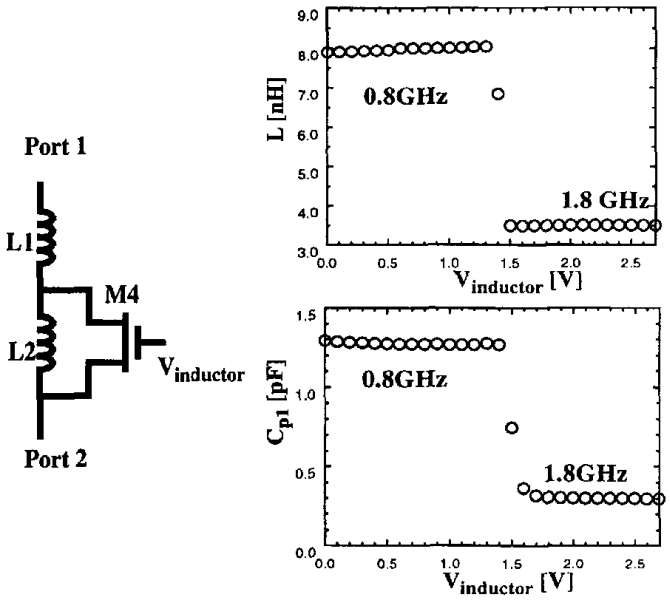



Figure 16: Schematic of a switched inductor with its simulated inductance (L) capacitance ($C_p$) [41]

consumption and phase noise for a wide-tuning oscillator limits their use. For instance, consider an LC-tank VCO composed of an inductor L with a series resistance, $R_S$ and quality factor, $Q_{L,}$ which has a trans-conductance of $G_m$. If the capacitor Q is relatively high, the equivalent parallel resistance $R_p$ of the tank for a fairly high inductor Q can be approximated to $\omega^2 L^2/R_s$ or $Q_L^2 R_s$ ,where ω is the desired oscillation frequency. Sustainable oscillation is maintained if

$$G_M R_p > 1 \tag{2.29}$$

Eqn. (2.29) shows that, for a given CMOS process, on the assumption that $Q_L$ roughly remains same, if the inductance is scaled up by a definite proportion, then its series resistance also scales up similarly, such that a smaller $G_m$ can be used, resulting in reduced

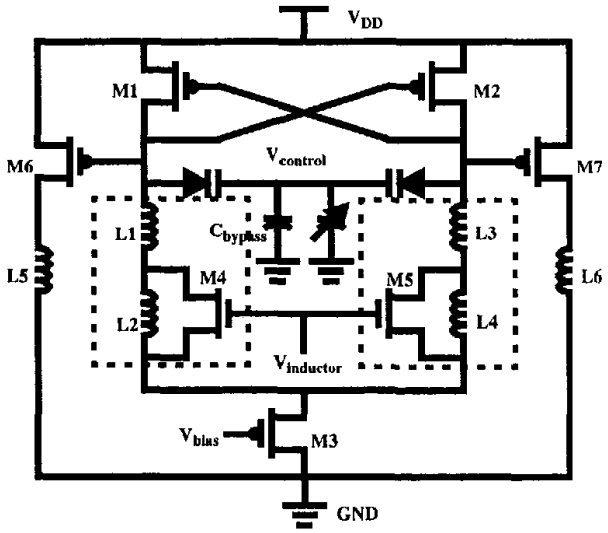



Figure 17: Complete schematic of a switch inductor based dual-mode oscillator [41]

power consumption. At the same time, recalling Eqn. (2.9), phase noise can be rewritten as

$$L(\Delta\omega) = 10\log\left(\frac{R_s k_B T}{2V_p^2}.F.\left(\frac{f_0}{\Delta f}\right)^2\right) \tag{2.30}$$

Since noise factor, F, is inversely proportional to $G_m$, phase noise can be reduced by increasing $G_m$ or decreasing $R_s$. If L is set for the high frequency band, using the same inductance for low frequency band by employing a switch capacitor bank, the power consumption required to push the lower band into voltage-limited regime (setting $G_m$) would be unreasonably high for high band. On the contrary, if L is set for the low band, using the same inductance for high band would result in phase noise deterioration due to the $\omega^2$ dependency of $R_p$. Scaling L and C simultaneously can resolve this issue [41] by using an inductor switching resonator topology as shown in Figure 16.

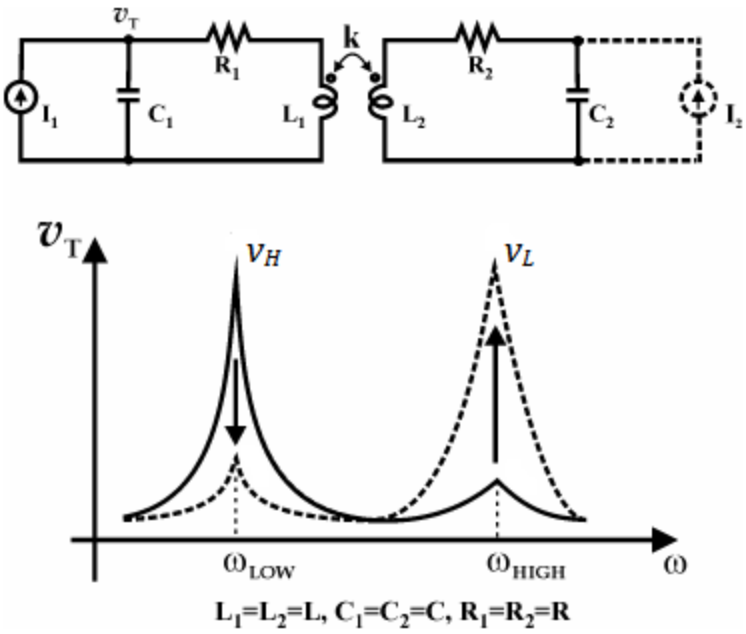



Figure 18: Transformer based resonator and effects of $I_1$ and $I_2$ on the oscillation amplitude [45]

The inductance between port1 and port2 can be tuned by switching the M4 on and off. When M4 is on, L2 is shorted and the complete inductance of the resonator decreases. The capacitance ($C_{p1}$) looking into port1 also changes due to the change in $C_{GD}$, $C_{GS}$ and $C_{DB}$ of the transistor. The complete circuit topology is shown in Figure 17 [41]. However, losses in the switch can degrade the quality factor of the resonator limiting the achievable phase noise and tuning range. Use of active inductors has also been reported to improve the tuning range [51]. Nevertheless, such implementation does not obtain simultaneous low phase noise and power consumption.

There has been active research to use switchless dual-band transformers to generate multiple frequency bands [42]- [50]. Figure 18 shows an example of such an implementation.

The resonator consists of a transformer whose primary and secondary windings, $L_1$ and $L_2$ with series resistance $R_1$ and $R_2$, are tuned by capacitance, $C_1$ and $C_2$. If we assume, that $L_1 = L_2 = L$, $C_1 = C_2 = C$, and $R_1 = R_2 = R$, then the two resonant mode frequencies can be derived as

$$\omega_{L,H} = \frac{1}{\sqrt{LC(1 \mp k)}} \tag{2.31}$$

with the quality factor at each resonant mode calculated to be

$$Q_{L,H} = \frac{1}{R}\sqrt{\frac{L}{C}(1 \mp k)} \tag{2.32}$$

Current sources, $I_1$ and $I_2$, connected to the primary and secondary windings control the oscillation amplitudes at the two resonant frequencies, where the oscillation amplitudes for each resonant mode are given as

$$v_L = \frac{(I_1 + I_2)(1 + k)L}{2RC} \tag{2.33}$$

and,

$$v_H = \frac{(I_1 - I_2)(1 - k)L}{2RC} \tag{2.34}$$

If $I_2 = 0$, then the oscillations at the higher resonant mode are suppressed, while if a $I_2 = -I_1$, then the oscillation amplitude at the lower resonant mode is completely suppressed. Consequently, simultaneous dual-mode oscillations can be successfully avoided. The complete circuit topology of the transformer-coupled VCO is shown in Figure 19 [45]. $M_1 – M_4$ connected to the resonator, with primary inductance $L_{p1}$ and $L_{p2}$ tuned by MOS varactors $C_{p1}$ and $C_{p2,}$ realize the negative resistance required to sustain

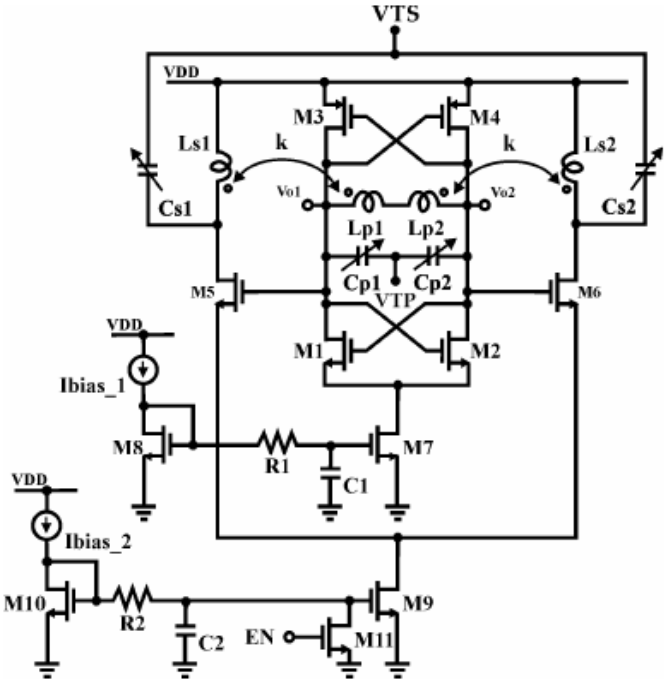



Figure 19: Complete schematic of a transformer base dual-band oscillator [45]

balanced oscillations. $M_5 – M_6$ differential pair feeds the secondary winding with current $I_2$ whose magnitude is equal to $I_I$ but with a completely opposite polarity. Turning on/off $M_{11}$ (enables/disables $I_2$) controls the dual-mode oscillations for this architecture.

Although a transformer coupled VCO seems to be a better solution to resolve the phase noise-tuning range trade-off, high dependence of the resonant frequencies on the resonant mode's quality factor limits the achievable tuning range of this oscillator since the quality factor and impedance of the resonator changes drastically from one mode to the other, degrading the phase noise in one or more resonant modes.

Capacitive coupling reported in [53] uses two identical LC tanks that are coupled by capacitors to create two resonant frequencies and reduce phase noise. However, the capacitor loads the resonator as a fixed capacitor in one of the modes limiting the complete

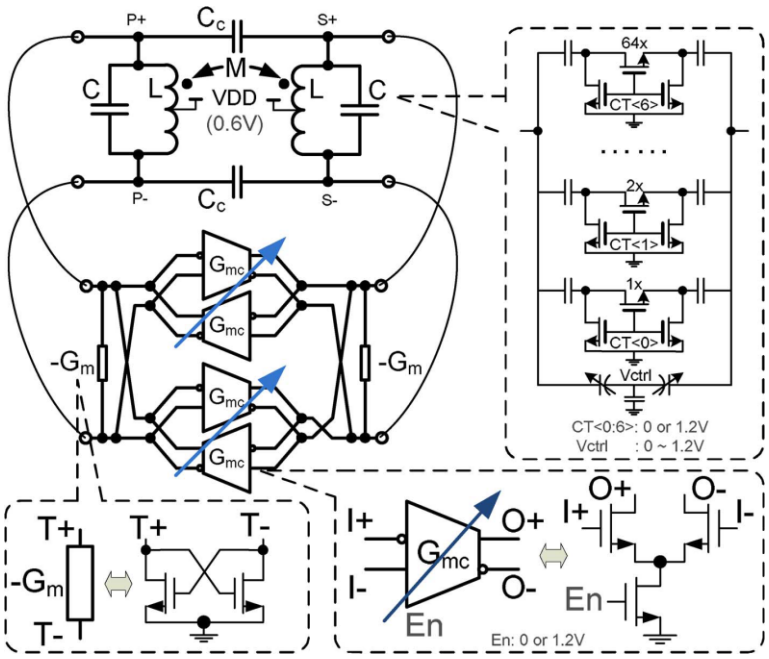



Figure 20: Complete schematic of capacitively/ inductively coupled resonant mode switching VCO [54]

tuning range. Another study reported in [54] uses the benefits of transformer and capacitive coupling to generate two resonant modes which when properly coupled show equal impedance at the two modes resulting in equivalent phase noise performance due to same Q and $R_p$ at the two resonant modes.

As illustrated in Figure 20, the oscillator design consists of a coupled LC resonator tank and a transistor based resonant mode switching network. Proper selection of M (inductive coupling) and $C_C$ (capacitive coupling) would give use the freedom to have a wide tuning range with a balanced phase noise performance due to the same input impedance as shown in Fig. 21. The two oscillation frequencies are given by

$$\omega_{even} = \frac{1}{\sqrt{(L+M)C}} \tag{2.35}$$

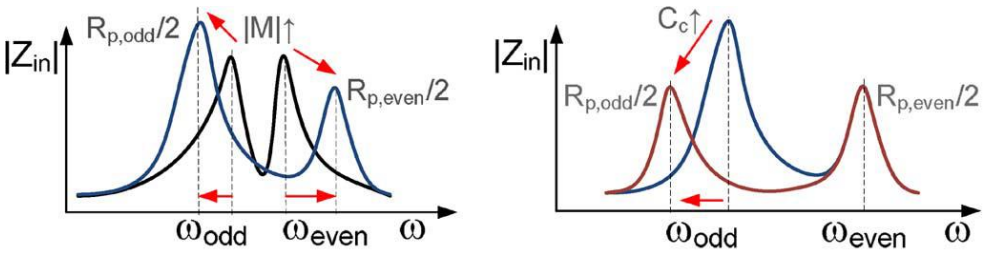


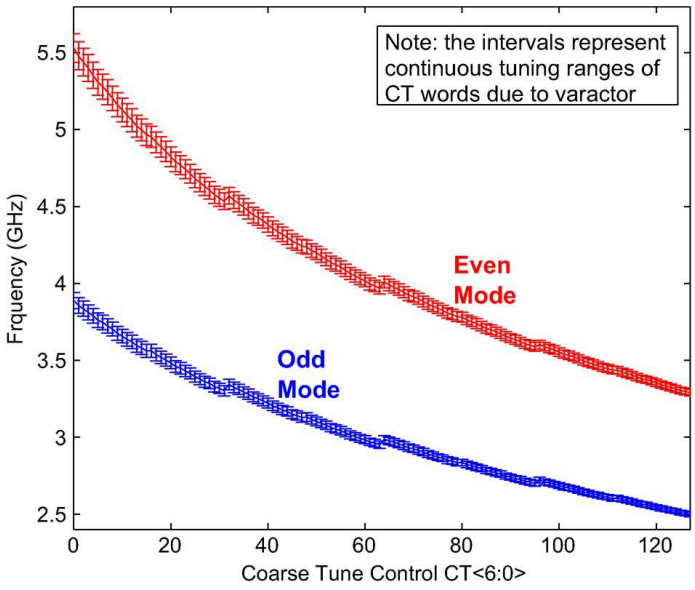

Figure 21: Input impedance tuned by M and $C_c$ (a) effect of M; (b) effect of $C_c$ [54]

and,

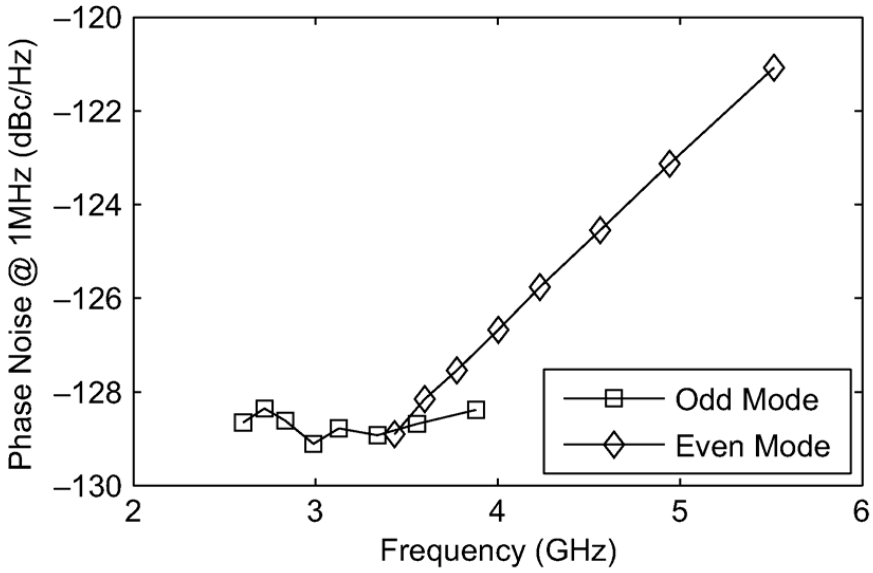
$$\omega_{odd} = \frac{1}{\sqrt{(L-M)(C+C_c)}} \tag{2.36}$$

The transistor network ($G_{mc}$ and $G_m$) stimulates one resonant mode while damping the other to eliminate concurrent dual-mode oscillations. As one can clearly notice, the difference between the top and bottom pair is the polarity. The resulting dual-mode configuration, if properly coupled achieves a 3dB phase noise improvement due to the coupling of two oscillators at the cost of twice the power consumption resulting in the same FoM when compared to a traditional Class-B VCO. Figure 22 plots the measured odd/even mode frequency tuning range, and phase noise at 1MHz for the entire tuning range from 2.48 – 5.2 GHz.

In conclusion, Table II summarizes the performances of different classes discussed above, while Table III summarizes the performance of different wideband VCOs.




(a)




(b)

Figure 22: (a) Measured tuning range; (b) Measured phase noise across the entire tuning range; [54]

Table II: Performance comparison of different LC oscillator topologies

| | [33] | [17] | [27] | [34] | [36] |
|---|---|---|---|---|---|
| Oscillator Structure | Class-B | Class-C | Class-D | Class-$F_3$ | Class-$F_2$ |
| Technology | 90nm | 130nm | 65nm | 65nm | 65nm |
| Supply $V_{DD}$ | 1.4 | 1 | 0.4 | 1.25 | 1.3 |
| Power | 25.2(mW) | 1.4(mW) | 4(mW) | 15(mW) | 41.6(mW) |
| Tuning range (GHz) | 3.2-4.1(25%) | 4.9-5.65(14%) | 3-4.8(46%) | 2.9-3.8(25%) | 3.6-4.4(19%) |
| Frequency | 915MHz | 5.2GHz | 4.8GHz | 3.7GHz | 4.35GHz |
| Phase Noise (dBc/Hz) | -149 @ 3MHz | -141.2 @ 3MHz | -135 @ 3MHz | -142.2 @ 3MHz | -144.8 @ 3MHz |
| Norm. PN[1] (dBc/Hz) | -149 | -147.5 | -149.4 | -154.3 | -158.3 |
| Figure of Merit(FOM) | 183 | 195 | 191.5 | 192.2 | 191.8 |
| Type | Single-Band | Single-Band | Single-Band | Single-Band | Single-Band |

[1] phase noise at 3MHz offset frequency normalized to 915MHz carrier

Table III: Performance comparison of different wideband LC VCO

| | [33] | [49] | [51] | [44] | [54] |
|---|---|---|---|---|---|
| Oscillator Structure | Class-B | Switched Inductor | Active Inductor | Transformer Coupled | Capacitively/ Inductively-coupled |
| Technology | 90nm | 130nm | 180nm | 130nm | 65nm |
| Supply Voltage | 1.4 | 1.2 | 1.8 | 1 | 0.6 |
| Power consumption | 25.2(mW) | 6.5-15.4(mW) | 6-28(mW) | 1-8(mW) | 9.8-14.2(mW) |
| Tuning range (GHz) | 3.2-4.1(25%) | 3.28-8.35(87.2%) | 0.5-3(143%) | 3.6-7(69%) | 2.48-5.62(76.5%) |
| Frequency | 915MHz | 3.28GHz | 2.9GHz | 4.6GHz | 3.7GHz |
| Phase Noise (dBc/Hz) | -149 @ 3MHz | -122 @ 1MHz | -102 @ 1MHz | -119 @ 1MHz | -151.4 @ 10 MHz |
| Figure of Merit(FOM)[1] | 183 | 180.5 | 174.3 | 183.8 | 192.5 |
| Type | Single-Band | Dual-Band | Dual-Band | Dual-Band | Dual-Band |

# 3. PROPOSED OSCILLATOR DESIGN

As mentioned earlier, for an optimum phase noise performance, LC oscillator is usually biased at the current and voltage limited boundary regions, where the oscillation amplitude reaches an upper limit set by the supply voltage [5]. H. -C. Chang et al [25] shows that by coupling N oscillators, the effective phase noise factor can be reduced by a factor of N by maintaining the same FoM. This theory has been utilized in the resonant mode switched oscillator design [54]. A class -F Oscillator implementation [34] can further reduce the effective noise factor. Thus, by proper integration of dual-mode resonance switching [54] with Class-F operation [34], a low phase noise wide tuning oscillator can be designed.

This chapter is organized as follows: Section 3.1 shows the implementation of a single-band Class-F oscillator. Section 3.2 presents the dual-mode resonator and proposes the effectiveness of the resonator to make the Class-F operation for a wide operating frequency range. Section 3.3 demonstrates the working of a transistor switching network to activate the desired resonant mode while damping the other. Section 3.4 reveals the complete circuit implementation.

## 3.1. Class-F Oscillator

As discussed in the previous section, a Class-F oscillator requires the use of two impedance resonance peaks to have a ratio of 3. However, using two separate inductors for such an implementation would be cost- inefficient and require extra area. A more

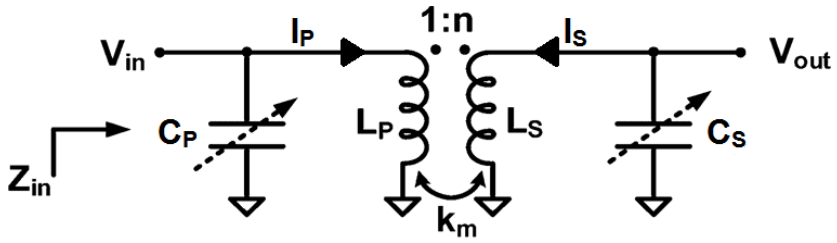



Figure 23: Schematic of a 4th order Class-F resonator i.e., a transformer-coupled resonator [34]

suitable option would be to implement a transformer based resonator as shown in Figure 23, where $C_p$ and $C_s$ are the respective tuning capacitors at the primary and secondary winding. $L_p$ and $L_s$ are the primary and secondary self-inductances. M is defined as the mutual inductance between the primary and secondary inductance of the 4th-order Class-F resonator. The magnetic coupling strength, $k_m$ is defined by

$$k_m = \frac{M}{\sqrt{L_p . L_s}} \tag{3.1}$$

The magnetic flux created by a time-varying current $I_p$ flowing into the primary will cause a time-varying induced current $I_s$ in the secondary winding. The terminal current and voltage of this ideal transformer are related as

$$\begin{bmatrix} V_{in} \\ V_{out} \end{bmatrix} = \begin{bmatrix} j\omega L_p & j\omega M \\ j\omega M & j\omega L_s \end{bmatrix} \begin{bmatrix} I_p \\ I_s \end{bmatrix} \tag{3.2}$$

The turn ratio n relating to the voltage and current transformation of the secondary and primary is given by

$$n = \sqrt{\frac{L_s}{L_p}} \approx \frac{V_{out}}{V_{in}} \approx \frac{I_p}{I_s} \tag{3.3}$$

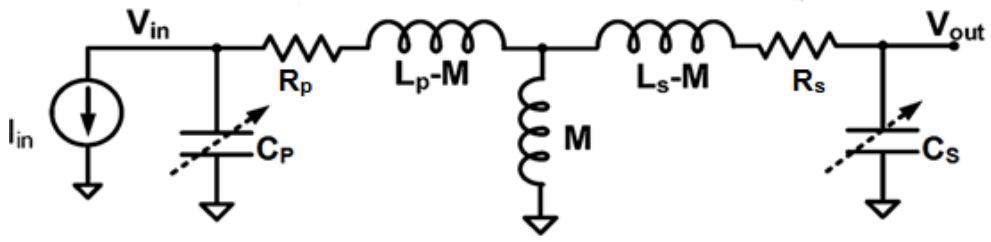



Figure 24: Equivalent circuit of the transformer-based resonator [34]

Neglecting the substrate losses, an equivalent T-model for this resonator is shown in Figure 24, where the equivalent input impedance $Z_{in}$ can be calculated as

$$Z_{in} = \frac{s^3\left(L_pL_sC_s(1-k_m^2)\right) + s^2\left(C_s\left(L_sR_p + L_pR_s\right)\right) + s\left(L_p + R_pR_sC_s\right) + R_p}{s^4\left(L_pL_sC_pC_s(1-k_m^2)\right) + s^3\left(C_pC_s\left(L_pR_s + L_sR_p\right)\right) + s^2\left(L_pC_p + L_sC_s + R_pR_sC_pC_s\right) + s\left(R_pC_s + R_sC_s\right) + 1} \tag{3.4}$$

in which $R_p$ and $R_s$ denote the corresponding primary and secondary series resistance. Eqn. (3.4) demonstrates the presence of two conjugate pole pairs, provided $k_m < 1$. Equating the denominator of (4) to zero, the two resonant frequencies are given as,

$$\omega_{1,2}^2 = \frac{1 + X \pm \sqrt{1 + X^2 + X(4k_m^2 - 2)}}{2L_sC_s(1-k_m^2)} \tag{3.5}$$

where,

$$X = \left(\frac{L_s}{L_p} \cdot \frac{C_s}{C_p}\right) \tag{3.6}$$

If $0.5 \leq k_m \leq 1$, then fundamental resonant peak can be approximated as

$$\omega_1^2 = \frac{1}{(L_pC_p + L_sC_s)} \tag{3.7}$$

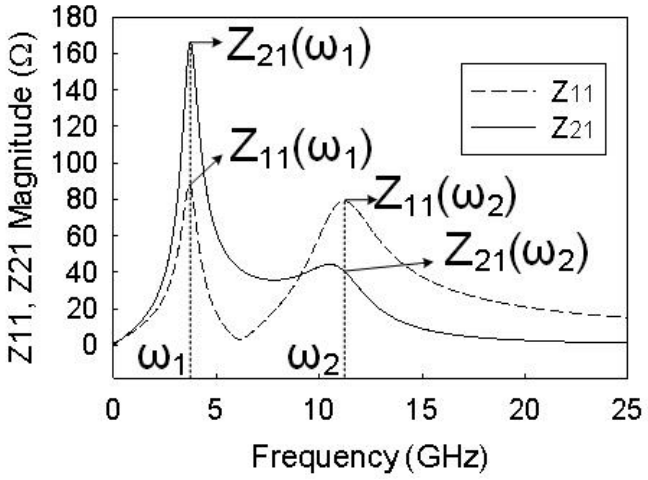


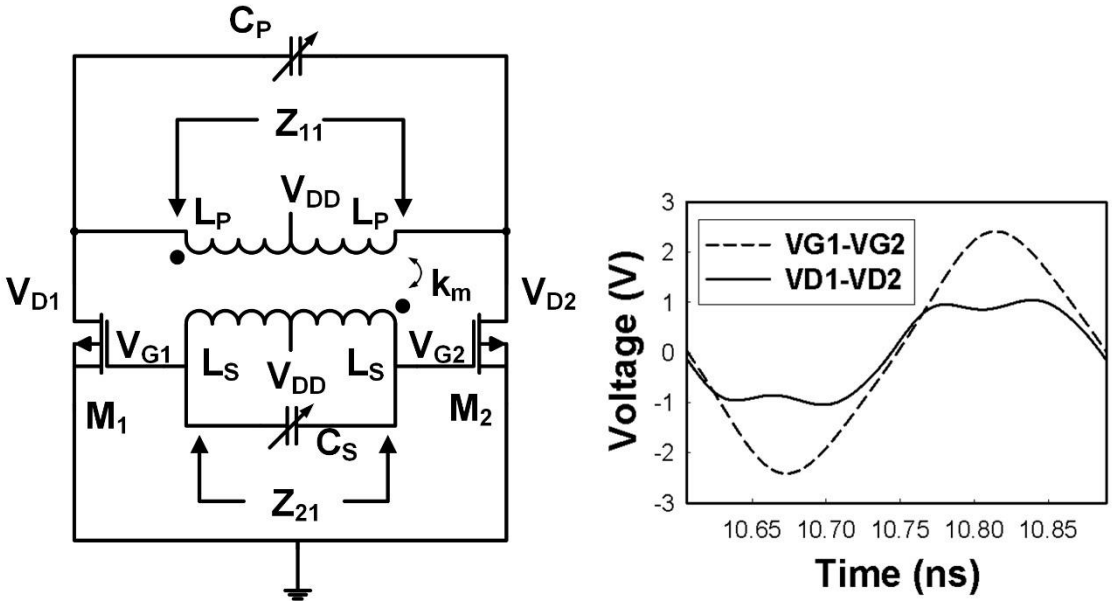

Figure 25: Input impedance and trans-impedance magnitude ($Z_{11}$, $Z_{21}$) [34]

The ratio of the two resonant frequencies for oscillations is given by

$$\frac{\omega_2}{\omega_1} = \sqrt{\frac{1 + X + \sqrt{1 + X^2 + X\,(4k_m^2 - 2)}}{1 + X - \sqrt{1 + X^2 + X\,(4k_m^2 - 2)}}} \tag{3.8}$$

From (3.8), it can be seen that $\omega_2/\omega_1$ solely is a function of tuning inductance and capacitors ratio (X), and the coupling coefficient $k_m$, and as a result is independent of process variations. To adjust $\omega_2/\omega_1$ =3, a $k_m$ of 0.7 lowers sensitivity to X and increases voltage gain. ($Z_{21}$ in Figure 25).

Figure 26 shows the implemented transformer-coupled Class-F oscillator. As per the linear time variant model [7], better phase noise and power efficiency can be achieved by shaping the output waveform of an oscillator. A Class-F oscillator enforces a pseudo square wave waveform across the LC tank ($V_{D1}$-$V_{D2}$) by self-injecting a third harmonic at the fundamental oscillation voltage through an additional impedance peak at that frequency. This square wave has sharper zero crossings and flatness when the transistor




(a) (b)

Figure 26: Transformer-coupled Class-F oscillator and its characteristics: (a) schematic of the oscillator; (b) Oscillation voltage waveform; [34]

turns on/off respectively, which effectively reduces the rms value of the ISF and noise contribution to the phase noise [7].

Although a class -F can be implemented as a cross coupled oscillator with a floating secondary winding, connecting the secondary winding to the gate of the gm-device has the advantage of generating higher amount of third harmonic currents at the gm-devices which lowers the ISF rms value, and eliminates the possibility of oscillation at the third harmonic [34]. Section 3.4 explains the design considerations regarding transistor sizing in detail.

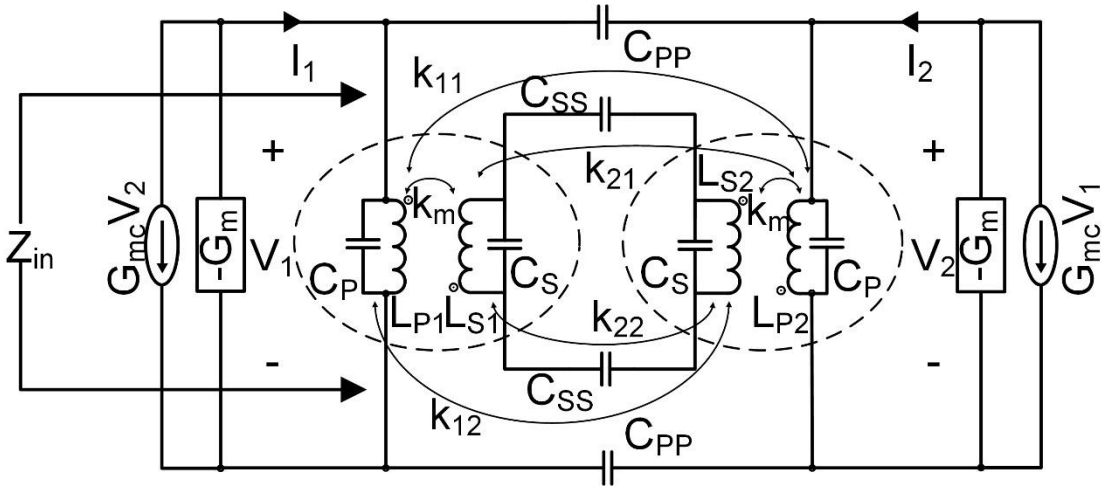



Figure 27: Proposed dual-mode resonator with the addition of trans-conductors for simulating the desired oscillation mode.

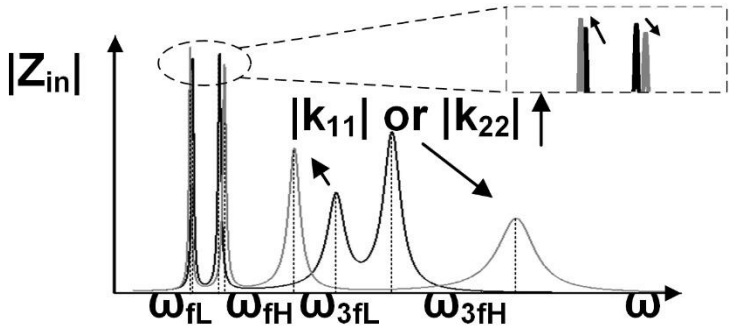
### 3.2. Dual-Mode Resonator

As illustrated in Figure 27, the proposed resonator consists of two identical 4$^{th}$-order resonators ($L_{p1}$=$L_{p2}$, $L_{s1}$=$L_{s2}$, $C_p$=$C_s$) which are inductively and capacitively coupled. Coupling values, $k_{11}$, $k_{22}$, $k_{12,}$ and $k_{21}$ represents the magnetic coupling coefficients for the sets ($L_{p1}$, $L_{p2}$) ($L_{s1}$, $L_{s2}$), ($L_{p1}$, $L_{s2}$) and ($L_{s1}$, $L_{p2}$), respectively. $C_{pp}$ and $C_{ss}$ represent capacitive coupling between the primary and secondary tanks. Each of the 4$^{th}$-order resonators consist of two magnetically coupled LC tanks satisfying oscillation conditions for a Class-F VCO. Intuitively, capacitive couplings ($C_{pp}$ and $C_{ss}$) provide resonance at two different frequencies depending on whether the polarity of the voltages and currents are in phase, or out of phase across the coupled capacitors [54]. It should be noted, that the third harmonic frequency component accompanies its respective first order harmonic content due to the Class-F operation.

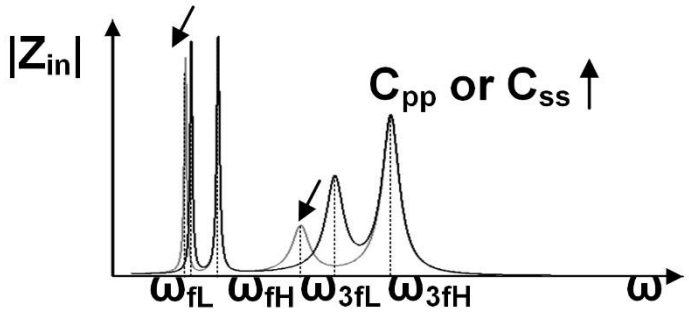
Figure 28 shows the effects of magnetic and electric coupling on the input impedance ($Z_{in}$) seen from each port of the primary winding ($L_{p1}$, $L_{p2}$) using simulations. As expected, this figure shows four impedance peaks. $\omega_{fH}$ and $\omega_{3fH}$ for higher resonant mode, and $\omega_{fL}$ and $\omega_{3fL}$ for the lower resonant mode. At the fundamental harmonic, by only increasing $k_{11}$ (or $k_{22}$), it can be seen that the two resonant frequencies move apart such that the impedance peak ($|Z_{in}|$) at $\omega_{fL}$ increases, while decreasing at $\omega_{fH}$. On the other hand, $C_{pp}$ (or $C_{ss}$) pushes down $\omega_{fL}$, without affecting $\omega_{fH}$. Changing $k_{12}$ (or $k_{21}$) doesn't impact the position of $\omega_{fL}$ (or $\omega_{fH}$). At the third harmonic, one can see that $C_{pp}$ (or $C_{ss}$) and $k_{11}$ (or $k_{22}$) increases the separation between the two $|Z_{in}|$ peaks at $\omega_{3fL}$ and $\omega_{3fH}$, while changing $k_{12}$ (or $k_{21}$) brings these peaks closer. Moreover, wider impedance bandwidth, i.e., lower tank Q, at the 3$^{rd}$ harmonic frequency, makes the design less susceptible to the positon of $\omega_2$, or the $C_p/C_s$ ratio change, such that the integrity of the Class-F waveform is maintained with negligible degradation in the phase noise performance. Detailed implementation of the dual-mode resonator topology is explained in section 3.4.

### 3.3.Mode Switching Network

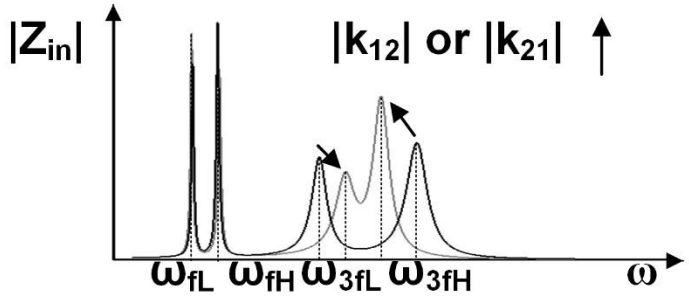
Negative-Gm cells can be added to each of the 4$^{th}$-order Class-F resonators to achieve sustainable oscillations and compensate for the losses in the system. However, the proposed resonator is designed such that input impedance has the same value for both modes to obtain similar phase noise and power consumption. Hence, use of only Gm cells can make the circuit unstable or possibly result in concurrent dual-mode oscillations. Therefore, additional circuitry is required to activate the desired resonant mode while




(a)




(b)




(c)

Figure 28: Input impedance $|Z_{in}|$ tuned by magnetic and electric coupling. (a) effect of $k_{11}$; (b) effect of $C_{pp}$; and (c) effect of $k_{12}$. We assume that $k_{11}$, $k_{22}$, $k_{12}$, $k_{21} < 0$.

damping the other. To implement a solution between the two modes, one needs to understand how the network in Figure 27 responds to $f_H$ and $f_L$ mode excitations. The system can be modelled as a two port Y network. It should also be noted that due to symmetry, the effective conductance $I_1/V_1$ and $I_2/V_2$ are equal. Now, assume a current of $I_{inj} = G_{mc} \cdot V_2$ is injected into the first port of the resonator, as shown in Figure 27. Since $V_1$ and $V_2$ have the same amplitude but a difference of phase ($\theta$ = 0° or 180° depending on the oscillation mode), this injected current can be replaced with an admittance of

$$Y_C = \frac{I_{inj}}{V_1} = \frac{G_{mc}V_2}{V_1} = \cos(\theta) \cdot G_{mc} \tag{3.9}$$

Cos ($\theta$) is negative when the resonator operates at $\omega_{fL}$ (lower mode) while it becomes positive at $\omega_{fH}$ (higher mode). Consequently, when $G_{mc} > 0$, the effective conductance seen from port 1 is $-G_m + G_{mc}$, increasing the total loss of the resonator at higher mode. On the other hand, at lower mode, $Y_C = -G_m - G_{mc}$. Thus, a sufficiently positive $G_{mc}$ can excite oscillation at $\omega_{fL}$ mode while damping it at $\omega_{fH}$. Similarly, negative $G_{mc}$ will show a completely opposite behaviour and can make the oscillator work at $\omega_{fH}$. Therefore, only by changing the polarity of $G_{mc}$, it is possible to switch between the two modes.

## 3.4. Circuit Implementation

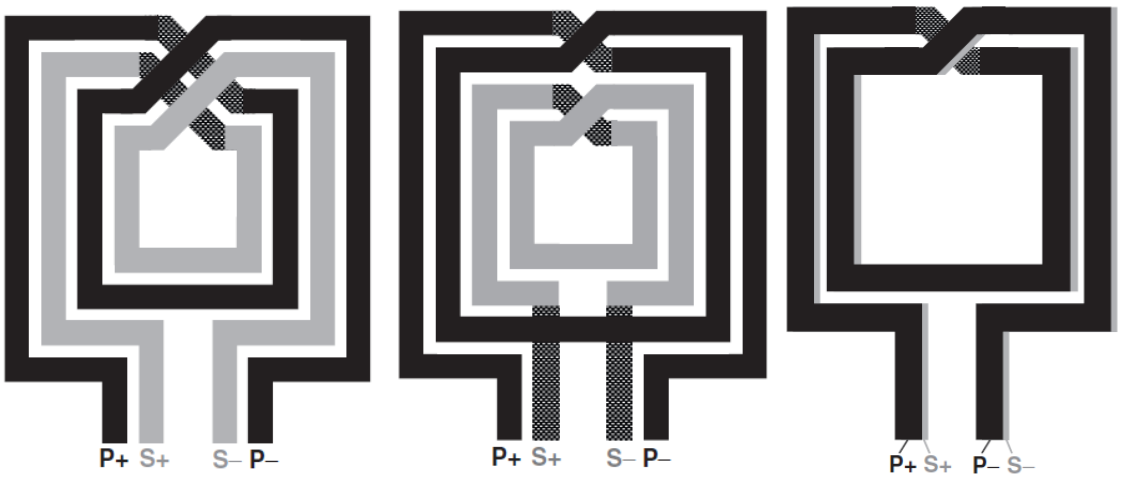
### 3.4.1. Transformer Design

Since the inception of integrated or monolithic silicon based transformers, there has been tremendous research in the design, analysis, modelling and optimization of a

transformer [58, 60-64]. A transformer, as one already knows, is nothing but a combination of two mutually coupled inductors. A fundamental comprehension of the inductor characteristics will assist in the optimum design of a transformer. Essentially, quality factor and self-resonance frequency are the two metrics on which the performance of an inductor is characterized. A higher self-resonant frequency will extend its inductive behaviour for a larger span of operating frequency range and high Q would result in a less lossy inductor. From an oscillator perspective, a high Q also improves the phase noise performance while reducing power consumption. However, substrate and metal layer losses are the two major contributors which limit the best Q that a silicon integrated inductor can achieve. Conduction current flowing from the metal layers to the low resistive silicon substrate, and the current induced into the substrate by the current carrying inductor as well as eddy current losses in the metal layer, dramatically impact the overall performance of an inductor. Since a transformer is a stack of mutually coupled inductors, these losses will still hold true.

Various topologies have been proposed in the recent decade related to transformer design. However, since a differential VCO would require a transformer with a symmetric differential output, the transformer topologies available can be vastly categorized into three different categories: a), interleaved b), tapered and c) stacked transformers as shown in Figure 29. [64].

An interleaved transformer as shown in Figure 29(a), as the name suggests, consists of the primary winding intertwined within the secondary winding, such that every primary metal trace section (or secondary) is neighboured by secondary metal trace




(a) (b) (c)

Figure 29: Differential transformer topologies: (a) Interleaved; (b) tapered; (c) stacked; [64]

sections (or primary) resulting in a reasonably high mutual coupling (km ≈ 0.7), but at the cost of reduced self-inductances and inter-winding capacitance (cross-coupled capacitance between the primary and secondary). An interleaved transformer is usually laid on the topmost thick metal layer of the Si process technology to obtain a high self-resonant frequency and inductor Q. Both the secondary and primary windings are present on the same layer while cross-over of metal traces of the same winding is performed by using lower metal layers.

Figure 29(b) shows the layout of a tapered transformer. In this topology the primary (or secondary) inductor is placed inside the secondary (or primary) winding resulting in a higher self-inductance and reduced inter-winding capacitance but at the cost of reduced mutual coupling coefficient. $K_m$ usually lies in the range of 0.2-0.7 depending on the spacing between these two inductors.

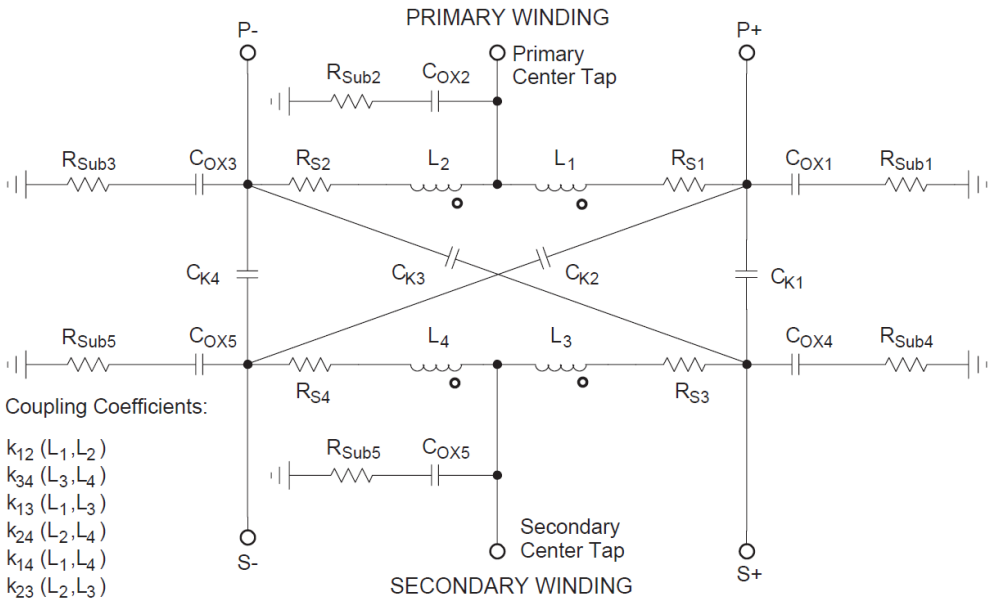



Figure 30: Lumped electrical model of a differential transformer, including center-taps [61]

In a stacked transformer as illustrated in Figure 29(c), primary and secondary windings are present on the adjacent metal layers to utilize both lateral and vertical magnetic coupling resulting in higher self-inductance, higher mutual coupling and lesser area but at the cost of lower self-resonance frequency, higher inter-winding and substrate coupling capacitance. A combination of stacked and interleaved capacitance can further boost the coupling coefficient but at the cost of higher parasitic capacitance and lower self-resonant frequency.

However, design, simulation and optimization of circuits require accurate broadband transformer models which imitates the process technology and physical layout conditions. Incorporating substrate and ohmic losses for a wide range of frequencies is a necessary requirement for its accuracy. An example of such a lumped electric model of

the transformer is shown in Figure 30 [61]. Figure 30 models a balanced transformer with a primary and secondary centre-taps. Self-inductances of the primary are modelled by $L_1$, $L_2$ and of the secondary are modelled by L3, L4. Each of the inductors are mutually coupled and their respective coupling coefficients are represented by $k_{12}$, $k_{13}$, $k_{14}$, $k_{23}$, $k_{24}$, $k_{34}$.

$R_{P1}$, $R_{P2}$ and $R_{S1}$,$R_{S2}$ are the respective primary and secondary metal layer ohmic losses due to finite conductivity, skin effect, proximity effect. Skin effect manifests itself due to the vertical current density redistribution along the metal trace thickness. Proximity effect accounts for the horizontal current density redistribution due to the changing magnetic fields around a metal trace. In other words, these effects represent the eddy current losses in the metal trace. Eddy current loss can be due to the current flowing in the same metal trace, or due to induced magnetic field from current flowing in adjacent metal traces of the same inductor, or from the other mutually coupled inductor of a transformer. Skin and proximity effects manifest themselves at high frequencies and the product of these two result in an increased resistance. The total series resistance from [63] is given by

$$R_{total} = R_{DC} + R_{RF} \approx R_{DC} real(\xi \coth(\xi)).\left[1 + r_{RF}\frac{\left(\frac{f}{f_o}\right)^2}{1+\left(\frac{f}{f_0}\right)^2}\right] \tag{3.10}$$

where $R_{total}$ represents the total series resistance of a primary and secondary winding such that $R_{total} = 2R_{P1} = 2R_{P2} = 2R_{S1} = 2R_{S2}$ , $R_{DC}$ represents the finite conductivity of the

metal trace. $R_{RF}$ accounts for the high frequency losses due to skin and proximity effects. ξ accounts for the skin effect given by

$$\xi = \frac{(1+i)t}{2\delta} \tag{3.11}$$

In which t, is the metal trace thickness and δ defines the skin depth represented by

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}} \tag{3.12}$$

where ρ, μ are the metal trace's resistivity and permeability respectively. ω is the operating frequency. $r_{RF}$ and $f_0$ account for the increase in resistance caused by proximity effect. $r_{RF}$ is a technology and geometry dependent coefficient whose values lies between 0.1 to 0.2. $f_0$ is the frequency factor given as

$$f_0 = \frac{2R_{sh}(1+3q)}{\mu_0 W(1-q^2)} \tag{3.13}$$

where $R_{sh}$ represents the sheet resistance of the metal trace, $\mu_0$ is free space permeability, W is the overall width of the metal trace, q factor is a ratio which represents width reduction due to eddy current loss. $R_{RF}$ tends to show a $f^2$ dependency at lower frequencies while at higher frequencies it follows a $\sqrt{f}$ dependency [63].

$C_{K1}$, $C_{K2}$, $C_{K3}$, and $C_{K4}$ model the cross-coupling capacitances between the primary and secondary winding, including the under-pass and fringing capacitance. $C_{OX1}$ – $C_{OX6}$ model the metal-oxide parallel plate capacitance from the metal layer winding to the substrate.

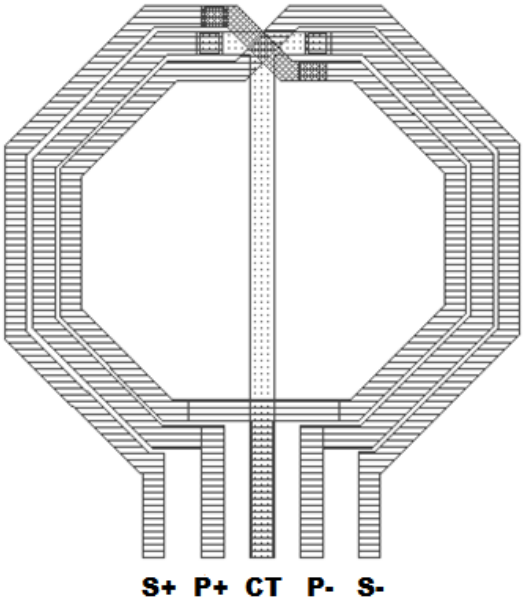



Figure 31: Symmetrical octagonal shaped interleaved transformer layout for a single

$$C_{OX_i} = \frac{1}{4}\frac{\varepsilon_{OX}}{t_{OX}}.W_i.l_i;\ i = 1,3,4,5$$

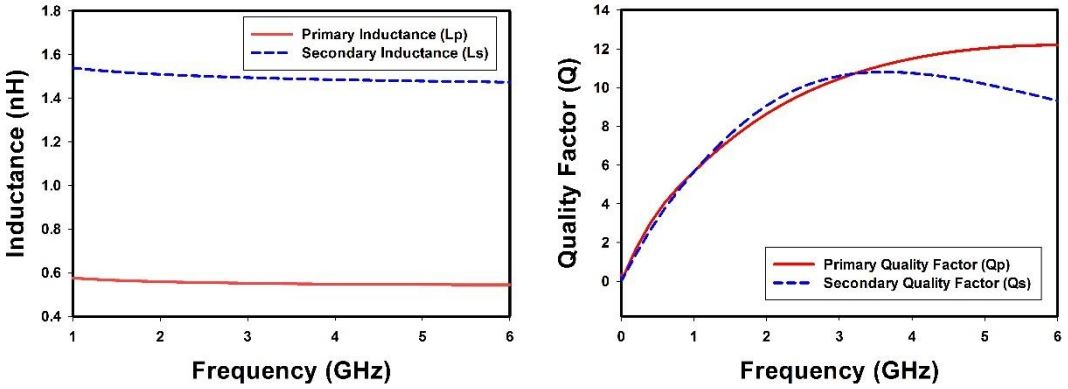
$$C_{OX_i} = \frac{1}{2}\frac{\varepsilon_{OX}}{t_{OX}}.W_i.l_i;\ i = 2,6 \tag{3.14}$$

$R_{sub1}$ – $R_{sub6}$ denote the parasitic substrate resistances calculated in [61] as

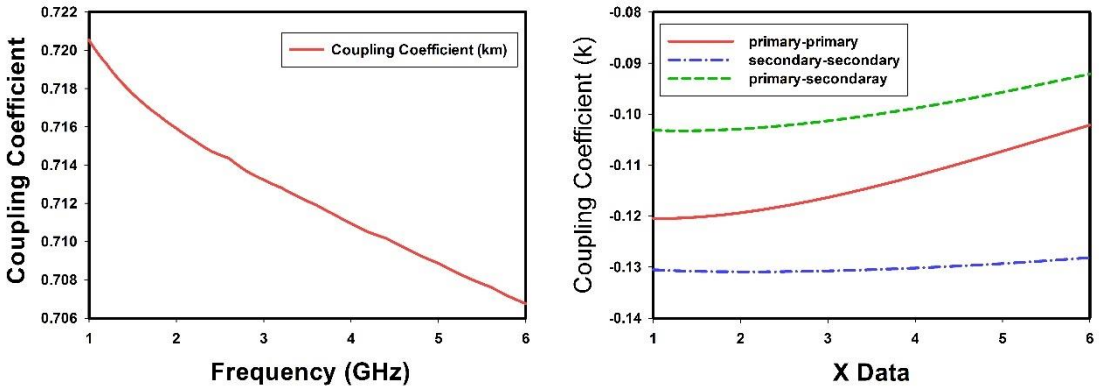
$$R_{sub} = \frac{\rho}{\pi l_M} ln\left[2coth\left(\frac{\pi}{8}.\frac{W_{eff}}{H_{sub}}\right)\right] \quad for\ \frac{W_{eff}}{H_{sub}} < 1$$

$$R_{sub} = \frac{\frac{\rho}{\pi l_M}}{ln\left[2\ e^{\frac{\pi W_{eff}}{4\ H_{sub}}}\right]} \quad for\ \frac{W_{eff}}{H_{sub}} > 1 \tag{3.15}$$

where $R_{sub}$ denotes the substrate resistance of single metal trace placed on the substrate, ρ defines the specific resistivity of the substrate, $l_M$ is the mean perimeter of the primary or




(a) (b)




(c) (d)

Figure 32: Electromagnetic simulation results using Sonnet: (a) Primary and secondary inductance; (b) Primary and secondary quality factor; (c) Coupling coefficient of a single transformer; (d) Inter-transformer coupling coefficients

secondary winding, $H_{sub}$ is the thickness of the substrate material and $W_{eff}$ is the effective width of the primary and secondary winding given as

$$W_{eff} = W + 6H_{OX} + t \tag{3.16}$$

in which W is the width of the metal trace, $H_{OX}$ is the oxide thickness, and t represents the conductor thickness. The overall substrate resistance of the primary and secondary winding would indeed depend on the number of turns and geometry of the transformer.

Unfortunately, as mentioned before, the proposed resonator consists of two inductively coupled transformers. The complexity of such a topology makes it extremely challenging to accurately model the complete electric behaviour of the proposed resonator. However, current EM solvers (such as Sonnet, HFSS, etc.) have the power to solve Maxwell equations using finite element method with greater accuracy providing a faster solution before compact models are developed.

Prior to designing the complete resonator, it is necessary for the transformer to meet the requirements of a single-band Class-F oscillator design, where the primary and secondary inductance were chosen to be approximately 0.5nH and 1.5nH with a coupling coefficient of 0.71. An interleaved 1:2 octagonal shaped transformer topology was selected to meet the above specifications. Figure 31 shows the implemented transformer laid out using the top metal layer in TSMC 65nm technology. The primary and secondary windings share the same centre-tap connection. An octagonal structure makes the transformer layout more area efficient and improves the quality factor, Q, of the inductor. The spacing between adjacent windings (2um) was minimized to increase the mutually coupling between the two winding. The optimum width of the metal trace was chosen to be 13um for both primary and secondary so as to maximize Q, while minimizing ohmic losses for the desired operating frequency range. Figure 32. shows the inductance, quality factor and coupling coefficient ($k_m$) simulated using the Sonnet EM solver. The complete

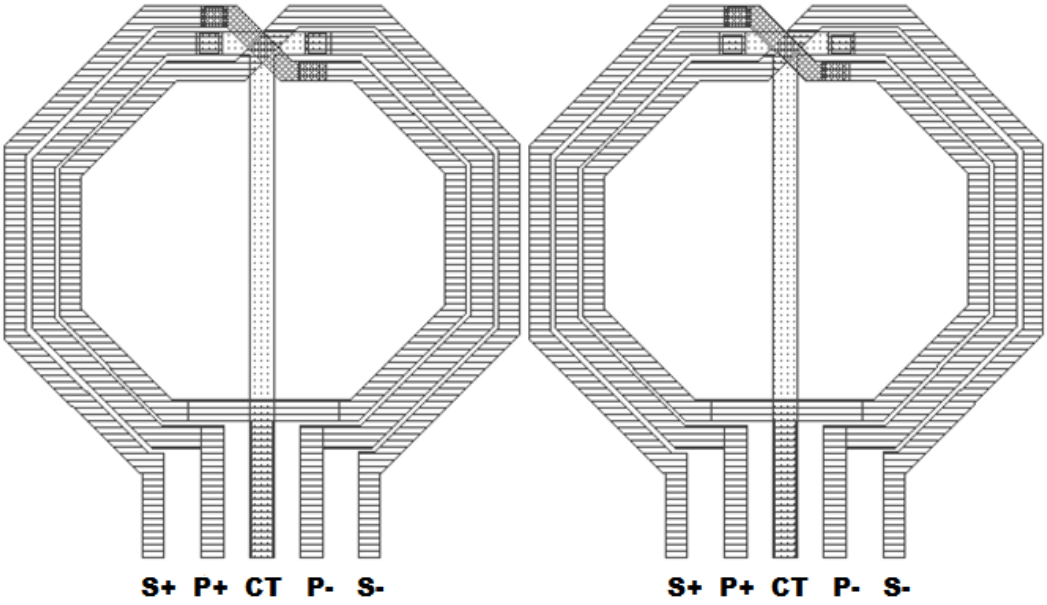
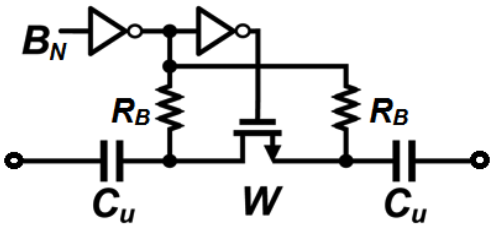



Figure 33: Inductively-coupled transformer layout for the proposed dual-mode resonator

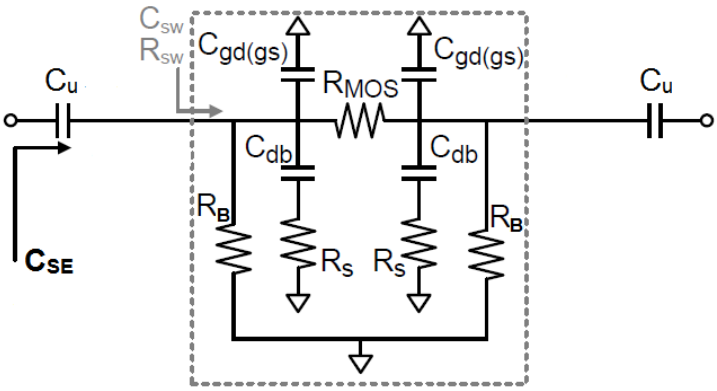
inductively coupled transformer implementation for the proposed resonator is shown in Figure 33. The two transformers are placed adjacent to each other to maximize inter-transformer coupling. Both these transformers are placed on the same layer to obtain equivalent performance for individual 4$^{th}$-order Class-F resonators i.e., similar $L_p$, $L_s$, $Q_p$, $Q_s$ and $k_m$. The inter-transformer coupling coefficient is shown in Figure 32 (d).

### 3.4.2. Capacitor Design

In the design of the Class-F VCO, a 6-bit binary weighted switched metal-insulator-metal (MIM) capacitor array is used for coarse tuning [ 55, 65]. Figure 34 shows the implementation of a single-switch capacitor and its equivalent electrical model. The implemented design sets the source and drain junction to the power supply voltage via a




(a)




(b)

Figure 34: Single-switch capacitor for coarse-tuning: (a) schematic; (b) equivalent electrical model [65]

high impedance resistance (R) when the switch is OFF warranting that the switch is complete turned off when a high voltage is applied to the MOS gate. The high impedance also eliminates ac current flowing into the switch.

If the parasitic capacitance and resistance of the MIM cap is negligible, the complete single-ended capacitance derived from the model can be calculated as

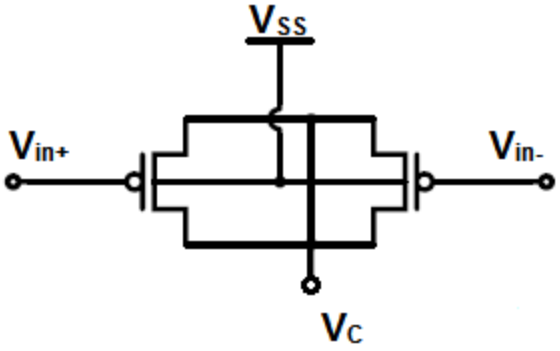



Figure 35: Schematic of a PMOS varactor design for fine tuning [57]

$$C_{se} = C_u || \frac{1 + \omega^2 R_{sw}^2 C_{sw}^2}{\omega^2 R_{sw}^2 (C_{sw})} \tag{3.17}$$

where $R_{sw}$ and $C_{sw}$ are given by

$$\frac{1}{R_{sw}} = \frac{1}{R_B} + \frac{2}{R_{MOS}} + \frac{\omega^2 R_s C_{db}^2}{1 + \omega^2 R_s C_{db}^2}$$

$$C_{sw} = \frac{C_{db}}{1 + \omega^2 R_s C_{db}^2} + C_{gd} \tag{3.18}$$

When the switch is ON. It operates in triode. Hence, $R_{MOS}$ can be derived as

$$R_{MOS} = \frac{L}{\mu C_{ox} W (V_{gs} - V_{th})} \tag{3.19}$$

If the width of the transistor switch is large, $R_{MOS}$ is small and the equivalent on-capacitance $(C_{se\_on})$ can be approximated as $C_u$. When the switch is OFF, $R_{sw}$ is high, and the equivalent off-capacitance can be approximated as $C_{se\_off} = C_u || C_{sw}$. Therefore, the overall tuning range of a single capacitor bank is given as

$$TR_{se} = \frac{C_u}{C_u || C_{sw}} \tag{3.20}$$

A 6-bit binary weighted capacitor array can satisfy the requirement for the desired operating tuning range [55].

Fine tuning is achieved by implementing a MOS varactor available in the TSMC65nm technology library in a differential operation as shown in Figure 35. This MOS capacitor operates in similar to a parallel plate capacitor where the plates are formed by the MOSFET channel and polysilicon gate. Although such an implementation shows a nonlinear capacitance variation with change in $V_{C.}$

### 3.4.3. Complete Circuit Integration

Figure 36 shows the complete schematic of the dual-mode Class-F oscillator. Each $4^{th}$-order Class-F tank consists of a transformer-coupled Gm cell which remains on in both resonant modes. The large voltage swing transitions at the gate ($V_{G1} – V_{G2}$ in Figure 26) of the M1-M2 switches of a single-band Class-F necessitate the need for thick-oxide $G_m$ devices. The $G_m$ cells of M1-M2 can be thought of as negative resistance that negates the input impedance looking into the primary winding of the $4^{th}$-order Class-F tank. $G_m$ must be at least 12.5mS to overcome the parallel resistance, $R_{in}$ = 80 Ω. A $G_m$ of 15mS was chosen such that as long as $R_{in} > 66.6Ω$, the oscillator would still function properly.

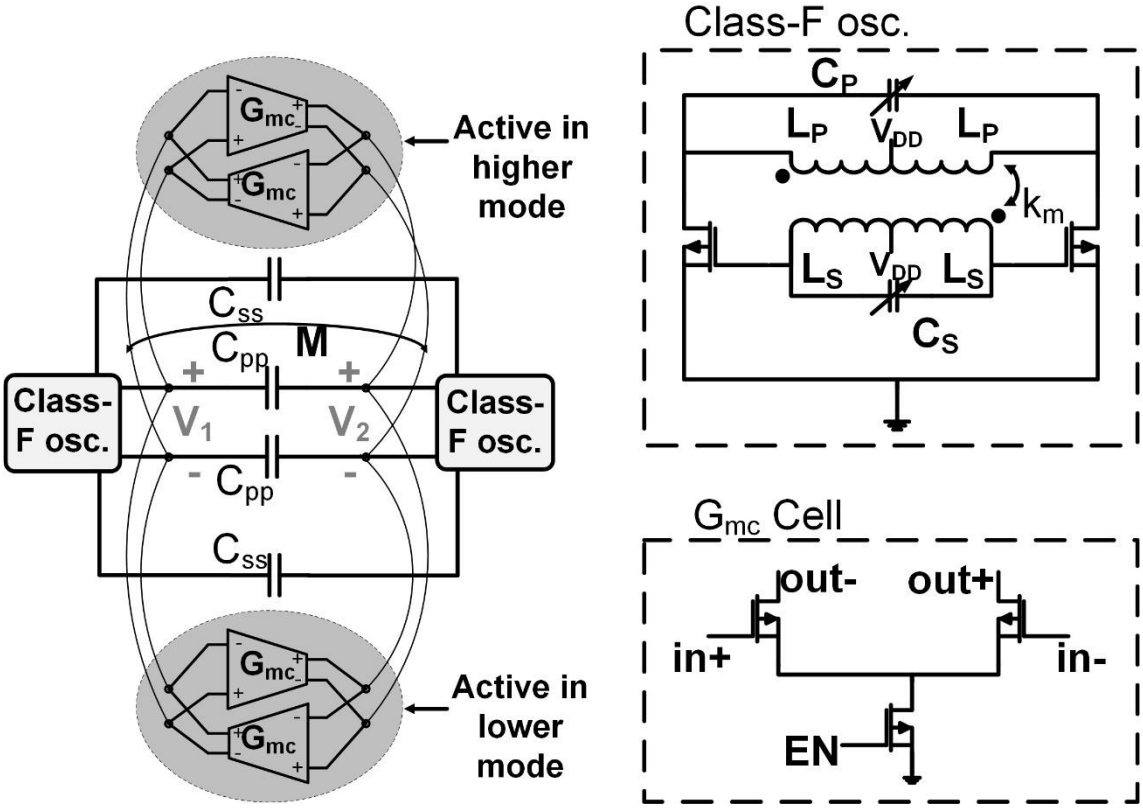



Figure 36: Complete schematic of the dual-mode Class-F VCO

Proper sizing of $G_m$ can be thought of as an iterative process. Initially, the primary and secondary inductance of the 4$^{th}$ order Class-F tank are chosen based on Eqn. (3.8) to guarantee a Class-F operation for more than half of the desired tuning range. In order to maintain $\omega_2/\omega_1=3$, the primary and secondary self-inductance are chosen to be approximately 0.5nH and 1.5nH respectively with a magnetic coupling coefficient of $k_m=0.71$. Also, since the oscillation at the secondary winding is a sinusoid ($V_{G1}$-$V_{G2}$ from Fig.25), the transformer is designed to maximize Q at the secondary in order to desensitize the phase noise of the oscillator to the circuit noise at the secondary winding in comparison to the primary, having a pseudo- square wave. Nevertheless, it should be noted that $C_p$ and

$C_s$ are course tuned simultaneously to sustain $X = L_p C_s / L_s C_p$ ratio warranting that $\omega_2 = 3\omega_1$. $G_m$ cells i.e., cross coupled MOS devices are inserted to cancel the inductive and capacitive losses in the single-band Class-F oscillator. $C_p$ and $C_s$ should be resized to account for the respective parasitic capacitances introduced by $G_m$ cells and 4th-order Class-F tank. Simulations are performed to determine if the voltage swing, phase noise, power consumption specifications are met.

$G_{mc}$ cells are voltage-controlled current sources which control the resonant modes of operation. For operation in the lower mode, the positive polarity for $G_{mc}$ is maintained by the bottom pair while the top $G_{mc}$ pair is switched off. Similarly, for enabling the higher mode, the top negative polarity $G_{mc}$ cells are switched on while the bottom pairs are off. Variations in polarity can be seen easily by noting the change in connections made across the two 4th order Class-F tanks.

If the top $G_{mc}$ network in Figure 36 is active in the higher mode, the oscillator should satisfy the conditions given by

$$\begin{aligned} \left|G_{m,higher}.R_{in,higher}\right| > 1 \quad and \quad G_{m,higher} < 0 \\ \left|G_{m,lower}.R_{in,lower}\right| < 1 \quad or \quad G_{m,lower} > 0 \end{aligned} \tag{3.21}$$

where $R_{in,higher}$ and $R_{in,lower}$ represent the fundamental input impedance peaks of the of the higher and lower mode respectively and,

$$\begin{aligned} G_{m,higher} = -G_m - G_{mc} \\ G_{m,lower} = -G_m + G_{mc} \end{aligned} \tag{3.22}$$

Whereas if the bottom $G_{mc}$ network is active in Figure 36, the lower mode gets enable satisfying the conditions given by

$$\left|G_{m,higher}.R_{in,higher}\right| < 1 \quad or \quad G_{m,higher} > 0$$

$$\left|G_{m,lower}.R_{in,lower}\right| > 1 \quad and \quad G_{m,lower} < 0 \tag{3.23}$$

where,

$$G_{m,higher} = -G_m + G_{mc}$$

$$G_{m,lower} = -G_m - G_{mc} \tag{3.24}$$

A choice of $G_{mc}$ = 25mS satisfies the above oscillatory conditions. Final simulations are performed to determine if the voltage swing, phase noise, power consumption specifications are met.

Selecting proper values for the inductive ($k_{11}$, $k_{22}$, $k_{12}$, $k_{21}$) and capacitive coupling ($C_{pp}$, $C_{ss}$), and $G_{mc}$ cells between the two Class-F tanks is one of the major hurdles in this design, because (a) tuning range of the lower mode is restricted by the choice of $C_{pp}$ and $C_{ss}$. In order to obtain a wide tuning range across each band, these capacitors must be kept small, (b) coupling between the two 4$^{th}$-order tanks should be sufficiently strong in order to avoid frequency mismatch i.e., damping one frequency mode when the other is operating, and (c) maintaining $\omega_2/\omega_1$ =3 for each of the two bands is necessary to guarantee Class-F operation. In summary, proper selection of magnetic coupling coefficients, $C_{pp}$ and $C_{ss}$ can make the two fundamental harmonic peaks of $Z_{in}$ have the same amplitude to achieve a balanced operation in the two modes, while extending the operating bandwidth. Meanwhile, this choice of magnetic/electric coupling should guarantee Class-F operation ($\omega_2/\omega_1$ =3). Thus, in order to cover a tuning range of around 40-45 % in each mode while achieving Class-F operation, M ($k_{11} = k_{12} = k_{21} = k_{22}$), $C_{pp}$ and $C_{ss}$ were chosen to be -0.1,

300f and 400f, respectively. $C_{pp}$ and $C_{ss}$ are fixed, and implemented using metal-insulator-metal (MIM) capacitors. $C_p$ (or $C_s$) is a 6-bit binary weighted capacitor array for coarse tuning [8]. Fine tuning is achieved by employing a pair of MOS varactors in $C_p$ (or $C_s$). The centre-taps of each transformer is connected to a 0.6V power supply. The MOS switches are enabled by a 0/1.2V bias. Also, the control voltage of the varactors is varied between 0-1.2V.

# 4. FABRICATION AND MEASUREMENT RESULTS

The proposed VCO was fabricated using TSMC 65nm CMOS technology. A die microphotograph of the chip is shown in Figure 37, occupying an active area of 0.7 $mm^2$, while consuming 15-16mW power from a 0.6V supply. The die was boxed in a 6mm x 6mm 40- lead QFN package and tested on a custom-designed PCB.

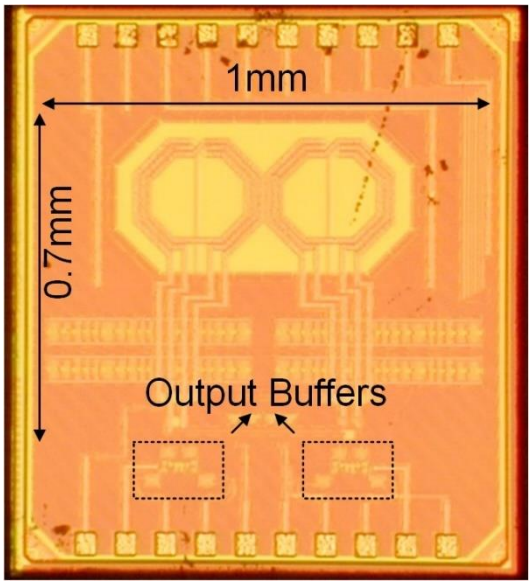



Figure. 37: VCO die photo

## 4.1.Current Consumption Measurements

Figure 38 shows the DC current consumption in each resonant mode from a constant 0.6V supply for different frequencies. The VCO consumes similar amount of power in the two modes as predicted by the same input impedance magnitude requirement

mentioned before. The variation in current is small when compared to other state-of-the-art wideband oscillator design in Table III.

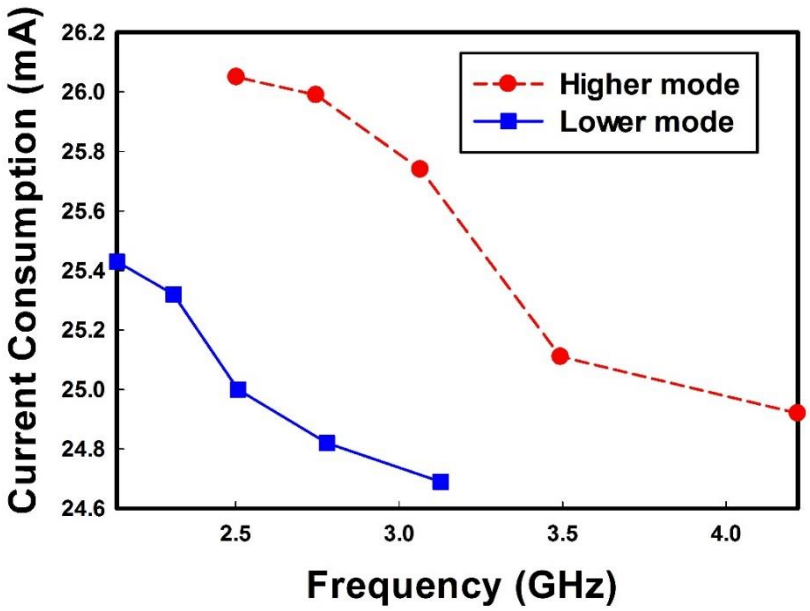



Figure 38: Measured current consumption

### 4.2. Phase Noise and Tuning Range Measurements

The tuning range and phase noise were measured using Agilent E4446A spectrum analyser. Figure 39 shows the measured tuning range, in which B<5:0> is the 6-bit digital control word of the switched capacitor banks. The lower resonant mode covers a frequency band from 2.14-3.13GHz, while the higher resonant mode covers frequencies ranging from 2.5-4.22GHz, therefore, this wideband Class-F VCO successfully covers a continuous tuning range from 2.14-4.22GHz with enough overlap (=620MHz) between the two modes promising its functionality even in the presence of worst case PVT variations. Each red/blue bar represents the fine-tuning frequency range covered by the

PMOS varactors. Figure 40 shows the measured phase noise at 1MHz offset frequency throughout the tuning range. Figure 41 shows a sample of measured phase noise curve at 2.3GHz in lower mode. The FoM of the VCO ranges from 188-193dB which is comparable to state-of-the-art designs [1]-[55].

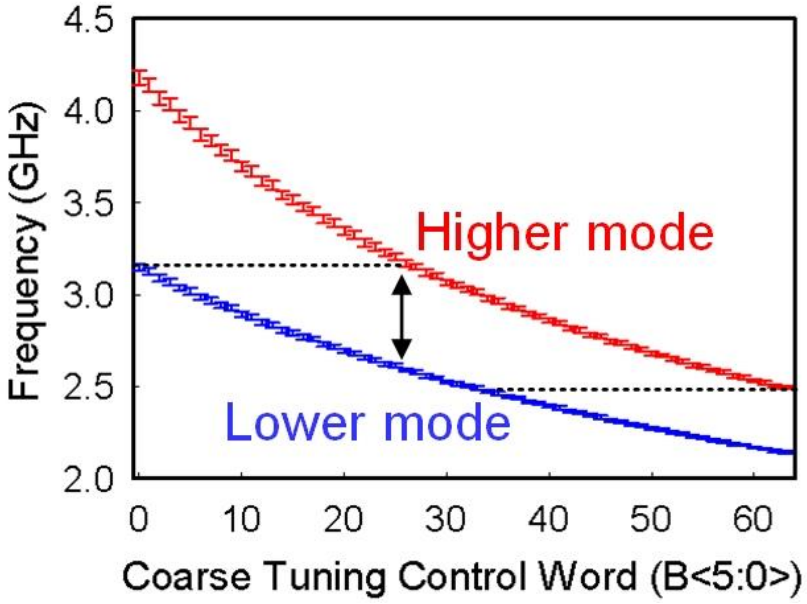



Figure 39: Measured tuning range

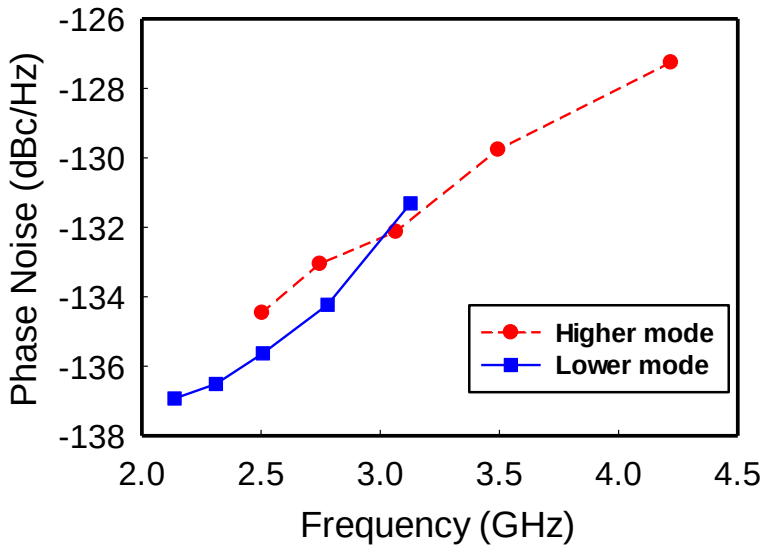



Figure 40: Measured phase noise at 1MHz offset frequency across the tuning range

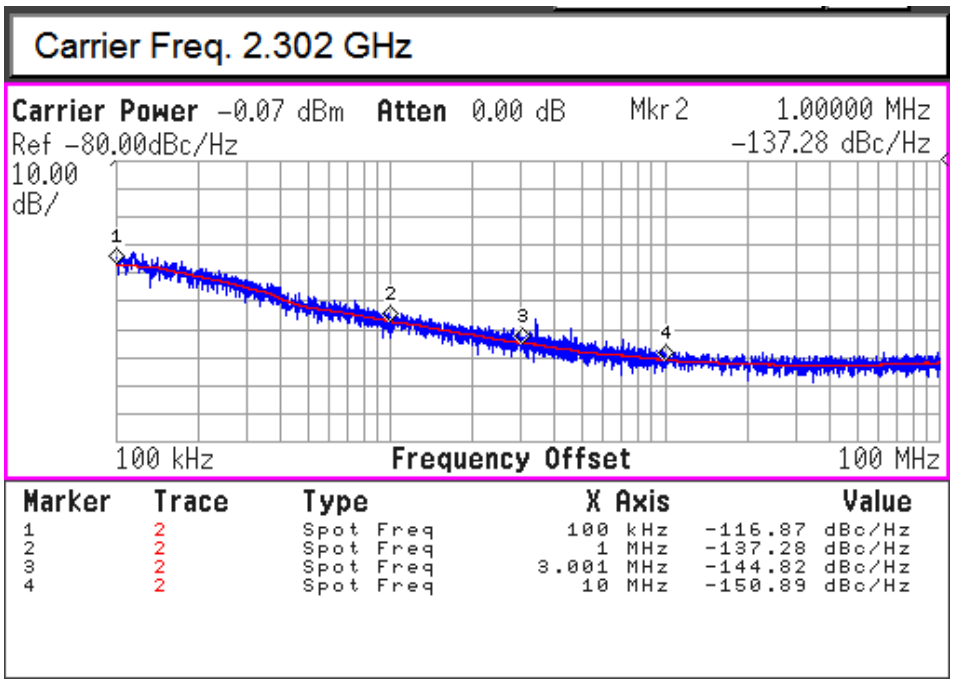



Figure 41: Measured phase noise at 2.3GHz

The oscillator performances are summarized in Table IV and compared with other state-of-the-art oscillators. The presented oscillator shows an excellent average FoM while covering a wide tuning range.

Table IV: Performance summary and comparison chart for a wide-band Class-F VCO

| | **[5]** | **[7]** | **This Work** |
|---|---|---|---|
| Type | Single-Band | Dual-Band | Dual-Band |
| Technology | 65nm CMOS | 65nm CMOS | 65nm CMOS |
| VDD (V) | 1.25 | 0.6 | 0.6 |
| Core Power (mW) | 15 | 9.8-14.2 | 15-16.4 |
| Tuning range (GHz) | 5.9-7.6 (25%) | 2.5-5.6 (76.5%) | 2.14-4.22(65 %) |
| Frequency | 3.7 | 3.7 | 3.7 |
| Phase Noise (dBc/Hz) | -131 @ 1MHz | -128.3 @ 1MHz | -132.93 @ 1MHz |
| FOM[1] (dB) | 190.5-192.5 | 188-192.5 | 188-192.7 |
| Area ($mm^2$) | 0.12 | 0.294 | 0.7 |

$$FoM^1 = 10\log_{10}\left[\frac{1}{P_{diss|\,mW}}\left(\frac{f_0}{\Delta f}\right)^2\right] - L(\Delta f)$$

# 5. CONCLUSION AND FUTURE WORK

In this dissertation, working of different classes of oscillators and their tuning range limitations have been identified and analyzed. A low phase noise wide-tuning range Class-F oscillator based on a dual-mode resonator was finally presented. In comparison to other conventional wideband oscillators, the proposed capacitively/inductively-coupled resonator integrates the benefits of Class-F voltage control oscillators and dual-mode switching networks to obtain simultaneous low phase noise and wide-tuning range. The proposed structure, prototyped in 65nm TSMC CMOS technology, shows a 2.14-4.22GHz continuous tuning range, phase noise figure-of-merit (FoM) of 192.7dB at 2.3GHz and better than 188dB across the entire operating frequency range. The oscillator consumes 15 – 16.4mW from a 0.6V supply and occupies an active area of $0.7mm^2$.

Revisiting Table IV, the proposed VCO shows a 2dB phase noise improvement at the same carrier frequency (3.7GHz) when compared to a single-band Class-F VCO [34]. Ideally, this proposed VCO should have displayed a 3dB phase noise improvement since two identical oscillators were coupled together [25]. Therefore, in the future, defining an accurate broadband electrical model for the two inductively-coupled transformers which imitates the process technology and physical layout by incorporating the substrate and ohmic losses, as well as the mutual coupling between the various primary and secondary windings, can assist in accurately predicting the position and amplitude of the four resonant peaks (two each of the first-order and third-order harmonics) resulting in optimizing the performance of the design to attain the lowest achievable phase noise performance while simultaneously meeting the wide tuning range requirement.

Additionally, this VCO can be integrated into a frequency synthesizer for various wireless applications utilizing Bluetooth, unlicensed ISM applications, or 802.11 WLAN in the 2 – 5GHz frequency band to investigate the improvement in the performance of the PLL (jitter), resulting in the development of an attractive alternative to the existing incorporated VCO designs.

## REFERENCES


[1] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 331–343, Mar. 1996.

[2] M. Mikhemar, D. Murphy, A. Mirzaei and H. Darabi, "A cancellation technique for reciprocal-mixing caused by phase noise and spurs," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3080–3089, Dec. 2013.

[3] J. Borremans, G. Mandal, V. Giannini, Bjorn Debaillie, Mark Ingels et al., "A 40nm CMOS 0.4-6GHz receiver resilient to out of band blockers," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, Jul. 2011.

[4] E. J. Baghdady, R. N. Lincoln, and B. D. Nelin, "Short-term frequency stability: Characterization, theory, and measurement," in *Proc. IEEE*, vol. 53, pp. 704–722, Jul. 1965.

[5] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in Colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[6] L. S. Cutler and C. L. Searle, "Some aspects of the theory and measurement of frequency fluctuations in frequency standards," in *Proc. IEEE*, vol. 54, pp. 136–154, Feb. 1966.

[7] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[8] D. B. Leeson, "A simple model of feedback oscillator noises spectrum," in *Proc. IEEE*, vol. 54, pp. 329–330, Feb. 1966.

[9] J. Rutman, "Characterization of phase and frequency instabilities in precision frequency sources; Fifteen years of progress," in *Proc. IEEE*, vol. 66, pp. 1048–1174, Sept. 1978.

[10] A. Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise in oscillators: a unifying theory and numerical methods for characterization," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 5, pp. 655–674, May 2000.

[11] D. Murphy, J. J. Rael, and A. A. Abidi, “Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 6, pp. 1187–1203, June 2010.

[12] A. Hajimiri, “Distributed integrated circuits: An alternative approach to high frequency design,” *IEEE Commun. Mag.*, vol. 40, no. 2, pp. 168–173, Feb. 2002.

[13] B. Razavi, “Design considerations for direct-conversion receivers,” IEEE Transaction on Circuits and Systems II: Analog and Digital Signal Processing, vol. 44, pp. 428—435, June 1997.

[14] A. Hajimiri and T. Lee, “Design issues in CMOS differential LC oscillators,” *IEEE Journal. Solid-State Circuits*, vol. 34, no. 5, pp. 717-724, May 1999.

[15] J. Rael and A. Abidi, “Physical processes of phase noise in differential LC oscillators,” in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2000, pp. 569–572.

[16] E. Hegazi, H. Sjoland, and A.A.Abidi, “A filtering technique to lower LC oscillator phase noise,” *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.

[17] A. Mazzanti and P. Andreani, “Class-C harmonic CMOS VCOs, with a general result on phase noise,” *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

[18] L. Fanori and P. Andreani, “Highly efficient Class-C CMOS VCOs, including a comparison with Class-B VCOs,” *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1730– 1740, Jul. 2013.

[19] M. Tohidian, A. Fotowat-Ahmadi, M. Kamarei, and F. Ndagijimana, “High-swing Class-C VCO,”’ in *Proc. IEEE Eur. Solid-State Circuits Conf.*, Sep. 2011, pp. 495–498.

[20] W. Deng, K. Okada, and A. Matsuzawa, “A feedback Class-C VCO with robust startup condition over PVT variations and enhanced oscillation swing,” in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2011, pp. 499–502.

[21] J. Chen, F. Jonsson, M. Carlsson, C. Hedenas, and L. R. Zheng, “A low power, start-up ensured and constant amplitude Class-C VCO in 0.18$\mu$m CMOS,” *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 8, pp. 427–429, Aug. 2011.

[22] K. Okada, Y. Nomiyana, R. Murakami, and A. Matsuzawa, “A 0.114 mW dual conduction Class-C CMOS VCO with 0.2 V power supply,” in *Proc. IEEE Symp. Circuits*, Jun. 2009, pp. 228–229.

[23] A. Mazzanti and P. Andreani, "A Push–Pull Class-C CMOS VCO," in *IEEE Journal of Solid-State Circuits*, vol. 48, no. 3, pp. 724-732, March 2013.

[24] L. Fanori, A. Liscidini, and P. Andreani, “A 6.7-to-9.2 GHz 55 nm CMOS hybrid Class-B/Class-C cellular TX VCO,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2012, pp. 354–356.

[25] H. Chang, X. Cao, U. K. Mishra, and R. A. York, “Phase noise in coupled oscillators: Theory and experiment,” *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 5, pp. 604–615, May 1997.

[26] L. Fanori and P. Andreani, “A 2.5-to-3.3GHz CMOS Class-D VCO,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 346–347.

[27] L. Fanori and P. Andreani, “Class-D CMOS oscillators,” *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.

[28] A. G. Roy, S. Dey, J. B. Goins, T. S. Fiez, and K. Mayaram, “350 mV, 5 GHz Class-D enhanced swing differential and quadrature VCOs in 65 nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 50, no. 8, pp. 1833–1447, Aug. 2015.

[29] Y. Yoshihara, H. Majima, and R. Fujimoto, “A 0.171 mW, 2.4 GHz Class-D VCO with dynamic supply voltage control,” in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2014, pp. 339–342.

[30] P. J. Baxandall, “Transistor sine-wave LC oscillators. Some general considerations and new developments,” *Proc. IEEE – Part B: Electron. and Commun. Eng.*, vol. 106, no. 16, pp. 748–758, 1959.

[31] L. Fanori, T. Mattsson, and P. Andreani, “A class-D CMOS DCO with an on-chip LDO,” in *IEEE Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2014, pp. 335–338.

[32] H. Kim, S. Ryu, Y. Chung, J. Choi, and B. Kim, "A low phase-noise CMOS VCO with harmonic tuned LC tank," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 7, pp. 2917–2923, Jul. 2006.

[33] R. B. Staszewski, J. L. Wallberg, S. Rezeq, C-M Hung, O.E. Eliezer *et al.*, "All-digital PLL and transmitter for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469–2482, Dec. 2005.

[34] M. Babaie, and R. B. Staszewski, "A Class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[35] F. W. Kuo, R. Chen, K. Yen, H. Y. Liao, C. P. Jou, F. L. Hsueh, M. Babaie, R. B. Staszewski, "A 12mW all-digital PLL based on Class-F DCO for 4G phones in 28nm CMOS," in *Proceedings of IEEE VLSI Circuits Symposium*, 2014, pp. 1–2.

[36] M. Babaie and R. B. Staszewski, "An ultra-low phase noise Class-F2 CMOS oscillator with 191 dBc/Hz FOM and long term reliability," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 679–692, Mar. 2015.

[37] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS oscillators with switched tuning," in *Proc. IEEE Custom Integr. Circuits Conf.*, May 1998, pp. 555–558.

[38] R. S. Rana, X. D. Zhou, and Y. Lian, "An optimized 2.4 GHz CMOS *LC*-tank VCO with 0.55%/V frequency pushing and 516 MHz tuning range," in *IEEE Int. Circuits Syst. Symp.*, May 2005, pp. 4811–4814.

[39] B. De Muer, N. Itoh, M. Borremans, and M. Steyaert, "A 1.8-GHz highly-tunable low-phase-noise CMOS VCO," in *IEEE Custom Integr. Circuits Conf.*, May 2000, pp. 585–588.

[40] B. Min and H. Jeong, "5-GHz CMOS *LC* VCOs with wide tuning ranges," *IEEE Microw. Wireless Compon. Lett.*, vol. 15, no. 5, pp. 336–338, May 2005.

[41] Y. Seong-Mo and K. K. O, "Switched resonators and their applications in a dual-band monolithic CMOS LC-tuned VCO," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 1, pp. 1705–1711, Jan. 2006.

[42] L. Geynet, E. De Foucauld, P. Vincent, and G. Jacquemod, "Fully-integrated multistandard VCOs with switched *LC* tank and power controlled by body voltage

in 130 nm CMOS/SOI," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. Dig. Papers*, Jun. 2006, pp. 129–132.

[43] M. Demirkan, S. P. Bruss, and R. R. Spencer, "11.8 GHz CMOS VCO with 62% tuning range using switched coupled inductors," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. Dig. Papers*, Jun. 2007, pp. 401–404.

[44] A. Bevilacqua, F.P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "Transformer-based dual-mode voltage-controlled oscillators," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 54, no. 4, pp. 293–297, Apr. 2007.

[45] B. Catli and M. Hella, "A dual band, wide tuning range CMOS voltage controlled oscillator for multiband radio," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. Dig. Papers*, Jun. 2007, pp. 595–598.

[46] J. Borremans, S. Bronckers, P. Wambacq, M. Kuijk, and J. Craninckx , "A single-inductor dual-band VCO in a 0.06 mm 5.6 GHz multiband front-end in 90 nm digital CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2008, pp. 324–325.

[47] A. Goel and H. Hashemi, "Frequency switching in dual-resonance oscillators," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 571–582, Mar. 2007.

[48] A N. T. Tchamov, S. S. Broussev, I. S. Uzunovand, and K. K. Rantala, "Dual-band *LC* VCO architecture with a fourth-order resonator," *IEEE Trans. Circuits Syst. II, Expr. Briefs*, vol. 54, no. 3, pp. 277–281, Mar. 2007.

[49] B. Sadhu, J. Kim, and R. Harjani, "A CMOS 3.3–8.4 GHz wide tuning range, low phase noise LC VCO," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2009, pp. 559–562.

[50] Z. Safarian and H. Hashemi, "Wideband multi-mode CMOS VCO design using coupled inductors," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 56, no. 8, pp. 1830–1843, Aug. 2009.

[51] L. H. Lue, H. Hsieh-Hung, and L. Yu-Te, "A wide tuning-range CMOS VCO with a differential tunable active inductor," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 9, pp. 3462–3468, Sep. 2006.

[52] R. L. Bunch and S. Raman, "Large-signal analysis of MOS varactors in CMOS - $G_m$ LC VCOs," in *IEEE Journal of Solid-State Circuits*, vol. 38, no. 8, pp. 1325-1332, Aug. 2003.

[53] G. Li and E. Afshari, "A distributed dual-band LC oscillator based on mode switching," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 1, pp. 99–107, Jan. 2011.

[54] G. Li, L. Liu, Y. Tang and E. Afshari, "A low-phase-noise wide-tuning-range oscillator based on resonant mode switching," in *IEEE Journal of Solid-State Circuits*, vol. 47, no. 6, pp. 1295-1308, June 2012.

[55] M. M. Bajestan, V. D. Rezaei and K. Entesari, "A low phase-noise wide tuning-range quadrature oscillator using a transformer-based dual-resonance LC ring," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 4, pp. 1142-1153, April 2015.

[56] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.

[57] R. L. Bunch, "A fully monolithic 2.5GHz LC voltage controlled oscillator in 0.35 $\mu$m CMOS technology", M.S. Thesis, Virginia Polytechnic Institute and State University, Blacksburg, 2001.

[58] A. S. Klein, "Design and characterization of RFIC voltage controlled oscillators in silicon germanium HBT and submicron MOS technologies", M.S. Thesis, Virginia Polytechnic Institute and State University, Blacksburg, 2003.

[59] M. Shahmohammadi, "RF CMOS oscillators for cellular applications" Ph.D. Thesis, Delft University of Technology, Netherlands, 2016.

[60] A. M. Niknejad, "Analysis, design, and optimization of spiral inductors and transformers for Si RFIC", M.S. Thesis, University of California, Berkeley, 1997.

[61] D. Kehrer, "Design of monolithic integrated lumped transformers in silicon-based technologies up to 20 GHz", Ph.D. Thesis, Technischen Universit¨at Wien Fakult¨at f¨ur Elektrotechnik, Hacklweg, 2000.

[62] J. C. Costa, “Analysis of integrated transformers and its application to RFIC design”, Ph. D. Thesis, University of Barcelona, Barcelona, 2002.

[63] H. Gan, “On-chip transformer modeling, characterization, and applications in power and low noise amplifiers”, Ph. D. Thesis, Stanford University, Stanford, 2006.

[64] H. C. Luong, and J. Yin (2016), “Transformer design and characterization in CMOS process”, in Transformer-based design techniques for oscillators and frequency dividers, Cham, Springer International Publishing, pp. 7-19.

[65] Q. Wu, “Analysis and design of wide tuning range low phase noise mm-wave LC-VCOs”, M.S. Thesis, Ohio State University, 2013.