DESIGN, SIMULATION AND IMPLEMENTATION OF A HIGH STEP-UP Z-SOURCE DC-DC CONVERTER WITH FLYBACK AND VOLTAGE MULTIPLIER

A Thesis

by

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ABSTRACT

Nowadays, because of pollution problems of the fossil fuels and their unpleasant effects on the earth planet and people life, renewable energy sources such az photovoltaic (PV) cells and fuel cells are considered to produce electrical energy. These sources directly convert solar energy and chemical energy to electrical energy, respectively. Since the output voltage of PV cells is low, a high step-up dc-dc converter is needed to increase this low voltage to meet inverter input required voltage.

In this thesis, a novel high step-up dc-dc converter (which is the derivation of z-source converter) is introduced. This converter has a higher voltage gain in comparison to the conventional converters. This advantage makes this converter a suitable choice for high step-up applications, such as boosting the low output voltage of solar panels. Also, by choosing appropriate turns ratio of the coupled inductors, the proposed converter can be used for a wide range of voltage gain.

First, the z-source converter is analyzed and the conventional high step-up converters are discussed. Then, the new high step up converter is proposed and analyzed. The converter is simulated and the results are compared to the theoretical results. The proposed converter is then experimentally tested. The experiment results verify the theoretical and simulation results. Finally, the proposed converter is compared to the conventional ones and it's advantages such as having higher voltage gain are confirmed.

DEDICATION

To my parents, Maryam and Hassan

To my grandmothers

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Several basis converters can be used for increasing voltage gain. In this project, z-source converter is used as a basis converter because of it's advantages over the conventional converters. Our goal is to increase the voltage ratio of this converter for some applications like fuel cells and PV cells (photo voltaic cells) where the output DC voltage is limited.

In this chapter, z-source converter topology, it's principle and operation modes are presented. Also the ways of charging and discharging inductors and capacitors are showed. furthermore steady state expressions are indicated and finally important current and voltage waveforms are depicted.

1.1 Introduction

Nowadays, the pollution issues caused by fossil fuels has adverse influences on the planet. Climate change imposes a global threat to the economic and social development of the societies. The Kyoto Protocol was one of the first environmental acts to reduce the rate of carbon emissions due to human activities [37]. The main reason behind the excessive carbon emissions is the excessive combustion of fossil fuels [33–35]. Moreover, the recent volatility of the oil prices since 2014 has also added a force behind the shift from fossil fuels towards the renewable resources [3,36,38–41]. Therefore, fossil fuels problems can be counted as following :

✓Giant amounts of carbon dioxide are released into the atmosphere.

✓Carbon dioxide leads to greenhouse effect or the global warming.

✓Coal-burning stations release Sulfur dioxide gas which causes to acid rain.

✓Fossil fuels supplies are limited and are not renewable.

Therefore, as it is shown in figure 1.1, the usage of renewable energy sources is

increased to produce energy over past years.

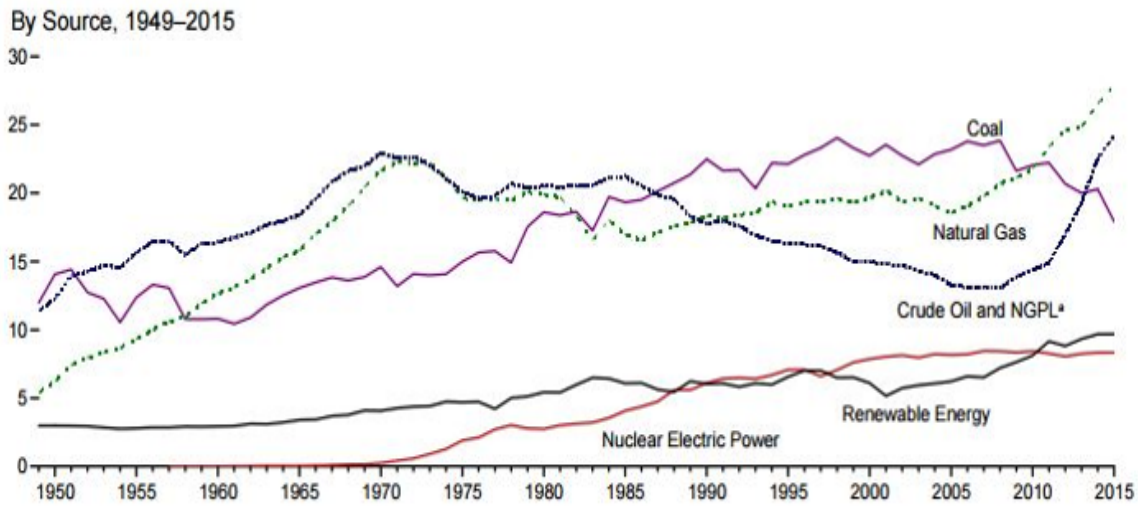

Figure 1.1: Primary energy production in U.S.A. [1]

Therefore, renewable energy sources such as fuel-cells and solar panels are employed to generate electrical energy. PV cells are attractive since they solar energy directly to electrical energy. However, they generate the low output voltage and the higher voltage is needed for grid-connected inverters, so the demand of using high step-up dc-dc converters is increased [6], [10], [14], [17], [23], [24].

The conventional solution was to use the several PV cells in series, However, because of the module mismatch and shadow effect of PV cells, the output power is decreased. Furthermore since several solar panels need to be used in this method, the total cost is increased and the efficiency is decreased. Another solution to this problem is to use a high step-up dc-dc converter to boost the output voltage of solar panels [42].

Traditional isolated converters such as flyback and full-bridge converters, have

low efficiency because of usage of high turn ratio transformers. So non-isolated converters is preferred. Conventional boost converter voltage gain can be infinite in theory, but, the efficiency is decreased largely in high voltage gain. Moreover it has the output diode reverse recovery problem [32].

Z-source converter has been proposed by Fang Zheng Peng in 2002. It can be used for DC-to-DC, DC-to-AC, AC-to-DC and AC-to-AC power conversion purposes [31]. In this thesis, z-source DC-DC converter is considered for the applications that need a high step up DC-DC converter to boost up the DC voltage. Figure 1.2 indicates the general structure of z-source converter.

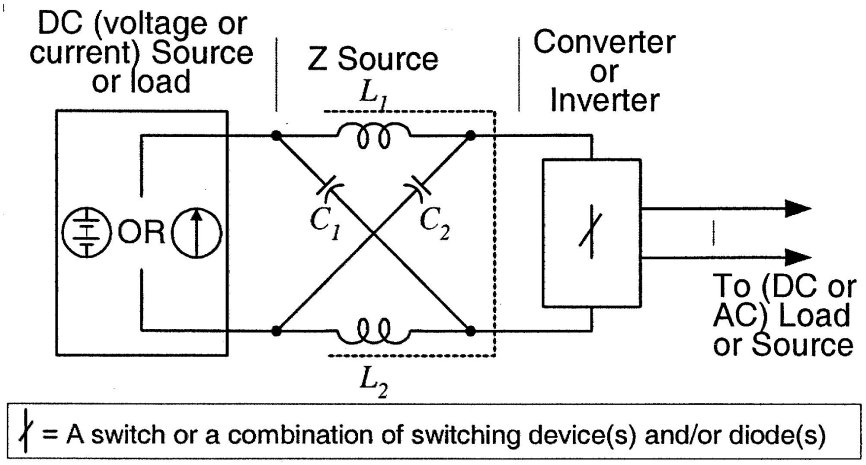

Figure 1.2: Z-source converter structure. [31]

Low output voltage energy sources like fuel cells and PV cells, need a high step up DC-DC converter to boost the voltage and also to provide a protection buffer between the load and energy source [8, 9, 16, 49]. Figure 1.3 shows the general block diagram of the traditional power conversion method for fuel cell applications.

Therefore, z-source converter can be used instead of using traditional dc-dc boost

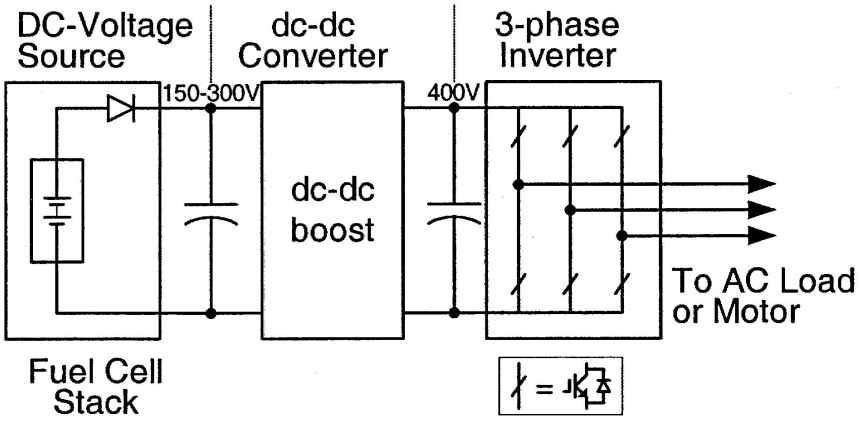

Figure 1.3: Traditional power conversion for fuel cell applications [31].

converter. Figure 1.4 indicates the z-source DC-DC inverter that is used to boost a low output voltage of fuel cell to meet the voltage required for inverter.

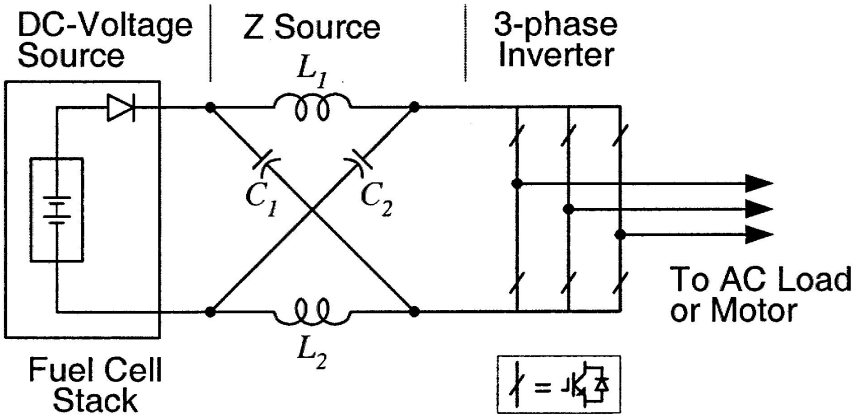

Figure 1.4: Z-source inverter to boost the low output voltage of fuel cell [31].

Figure 1.5 shows z-source converter topology. Some of z-source converter advantage in comparison to the conventional boos converter are as below :

✓Z-source dc-dc converter voltage gain in more than boost converter

✓Energy source and load side are isolated from each other for the situation that

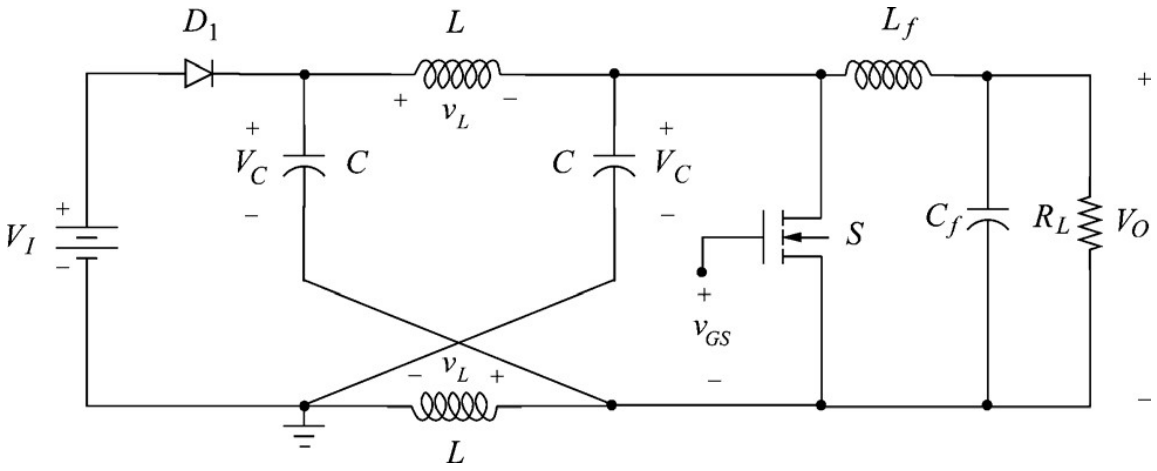

Figure 1.5: Z-source converter topology. [15]

short-circuit or any disturbance is happened in the load side, since the input diode (D_1) is off when the switch S is on. It is awesome for converter safety in case that the input energy source, fuel or PV cell, is expensive.

✓It has second order filter at the output. [15]

✓Based on the voltage gain expression, for $D > 0.5$, the output voltage is inverted, so it can be used where such a feature is needed. [15]

These advantages make the z-source converter the suitable option for renewable energy applications.

Pulse width modulation (PWM) method is employed for controlling this converter. In other words, switch on-time and off-time can be controlled with this method. Therefore, voltage gain can be changed with having control over duty cycle. Duty cycle is defined az $\frac{ton}{T}$. Where t_{on} is the switch on time and T is indicated as switching period. Voltage gain expression of this converter is the function of duty cycle, it means with controlling duty cycle, voltage gain can be controlled [2,7,15,48]

PWM z-source converter can be used in inverter mode with combining z-source switch with inverter switches. Figure 1.6 shows the z-source inverter. The advantage

of z-source inverter in comparison to the traditional ones is that the output voltage of the z-source inverter can be any value between zero to infinity regardless of the PV cell or fuel cell output voltage. It means that it acts like a buck-boost inverter [31].

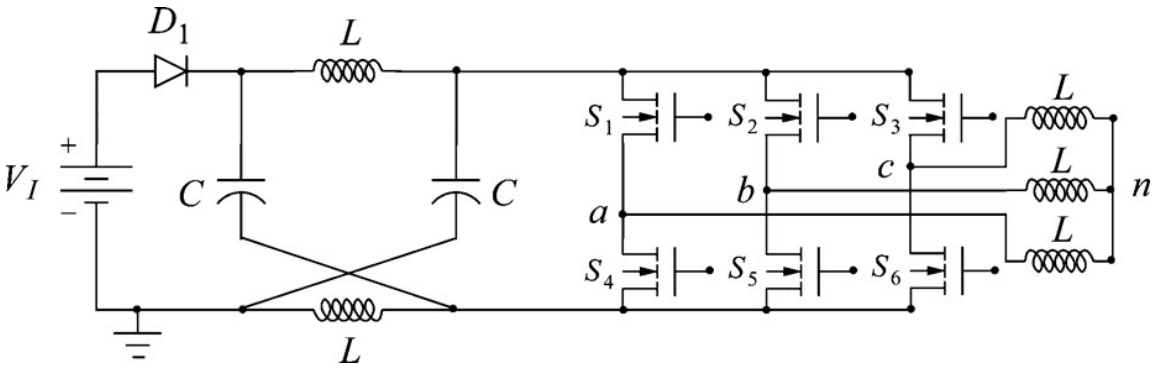

Figure 1.6: Z-source inverter topology. [15]

1.2 Operation Principles of Z-source Converter

As you see in figure 1.5, Z-source DC-DC converter consists of two identical capacitor ($C_1 = C_2 = C$) and two identical inductors ($L_1 = L_2 = L$). This set of components is called z-source network. Because of the network symmetry, inductors current are equal ($i_{L1} = i_{L2} = i_L$) and also the inductors voltage ($v_{L1} = v_{L2} = v_L$). Furthermore, capacitors currents ($i_{C1} = i_{C2} = i_C$) and capacitors voltage ($v_{C1} = v_{C2} = v_C$) are equal to each other. Also it has a input diode (D_1), an active switch (S) that can be IGBT or MOSFET and output inductor (L_f) and capacitor (C_f) that form output second order low-pass filter. Output voltage pulses are produced by turning the active switch on and off. DC output voltage can be produced by filtering these pulses with second order low-pass filter at the output [15]. Active switch S and diode D_1 operate at the complementary manner. It is assumed that duty ratio

of switch S is denoted by D, therefore, duty cycle of diode D_1 is $1 - D$. Also the switching frequency is the constant value of $f_S = \frac{1}{T}$.

It is assumed that all the components are ideal in these analysis. So switch and diodes turn on voltages are ignored. Also it is assumed that capacitors voltage ripple and inductors current ripple are small enough and so capacitors voltage and inductors current are constant. Furthermore, all the components are linear, independent of time and frequency.

In the steady state, z-source converter switching period can be divided to two time intervals.

1) $0 \leq t < DT$

This operation mode is started when switch S is turned on and lasts till the switch S is turned off. At the beginning of this mode, diode D_1 is turned off since the voltage across it is negative. ($V_{D1} = V_I - 2V_C$). Figure 1.7 indicates the equivalent circuit of this operation mode.

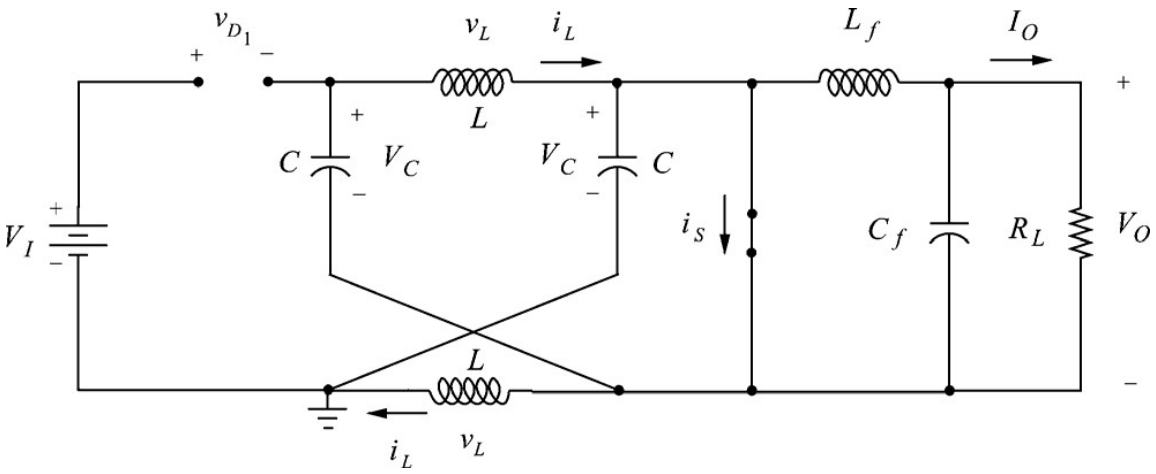

Figure 1.7: Z-source converter equivalent circuit when switch S is on. [15]

When the switch S is turned on, inductors L voltage and capacitors C voltage will be equal ($V_L = V_C$) and because the the current and voltage of the inductors (L) are positive, these two inductors are being charged and store energy and their currents are supplied by the capacitors current. Because the inductors voltage is positive and constant, their currents are being increased linearly and by the constant slope, however, the capacitors (C) are being discharged.

In this time interval, the filter inductor voltage is equal to $-V_O$, so it's current being decreased linearly and by the constant slope. Therefore filter inductor (L_f) energy is being lost [15].

As it was mentioned earlier, the input source is isolated from the load, because of the input diode in this operation mode and this feature is the advantage of z-source converter in comparison to conventional boost converter.

2) $DT \leq t \leq T$

This operation mode is started when switch S is turned off and lasts till the switch S is turned on. At the beginning of this mode, diode D_1 is turned on. Therefore, based on these two operation modes, diode D_1 and switch S operate in complementary manner. Figure 1.8 indicates the equivalent circuit of z-source converter in the second mode of operation.

When diode D_1 is turned on, the input source supplies power to the converter. So it is indicated that input current is not continuous and it includes several pulses. switch S stress voltage can be calculated In this operation mode. It is the voltage across switch when the switch is off. Therefore, $V_S = 2V_C - V_I$. Therefore, diode and switch stress voltage are equal to $2V_C - V_I$.

In this operation mode, inductors L voltage is equal to $V_I - V_C$. Since it is constant and negative, inductors L current is being decreased linearly and with the constant slope and their energy is being lost. In this time interval, capacitors C

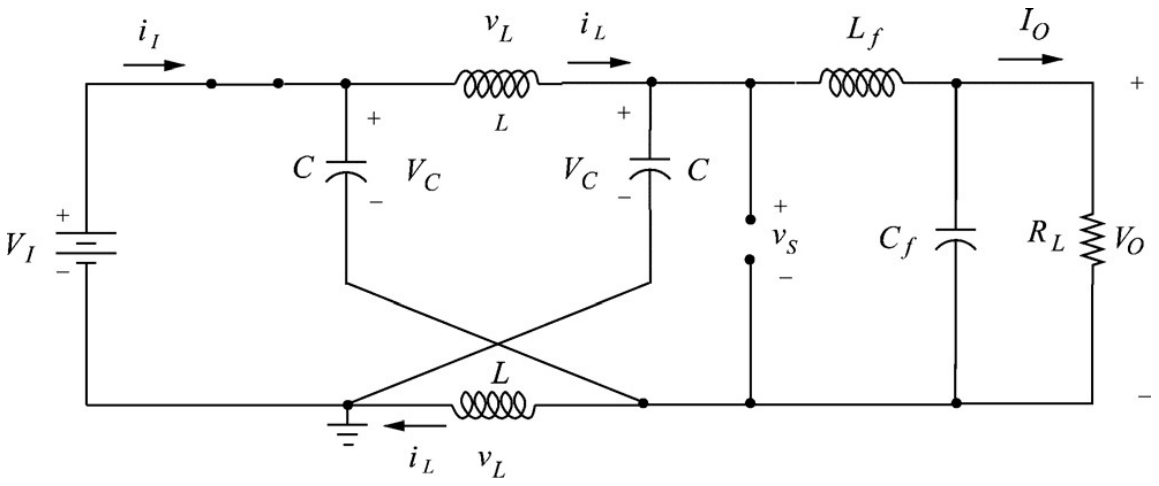

Figure 1.8: Z-source converter equivalent circuit when switch S is off [15].

are being charged by the input current. Filter inductor voltage (V_{Lf}) is equal to $2V_C - V_I - V_O$ and because this is the positive and constant value, this inductor is being charged and store energy.

It can be proved that $V_C = V_O$, therefore $V_{Lf} = V_O - V_I$. The filter inductor current (I_{Lf}) is the ripple current and it's average value is equal to I_O. It means output capacitor (C_f) absorbs the inductor L_f ripples and passes the DC value to the output.

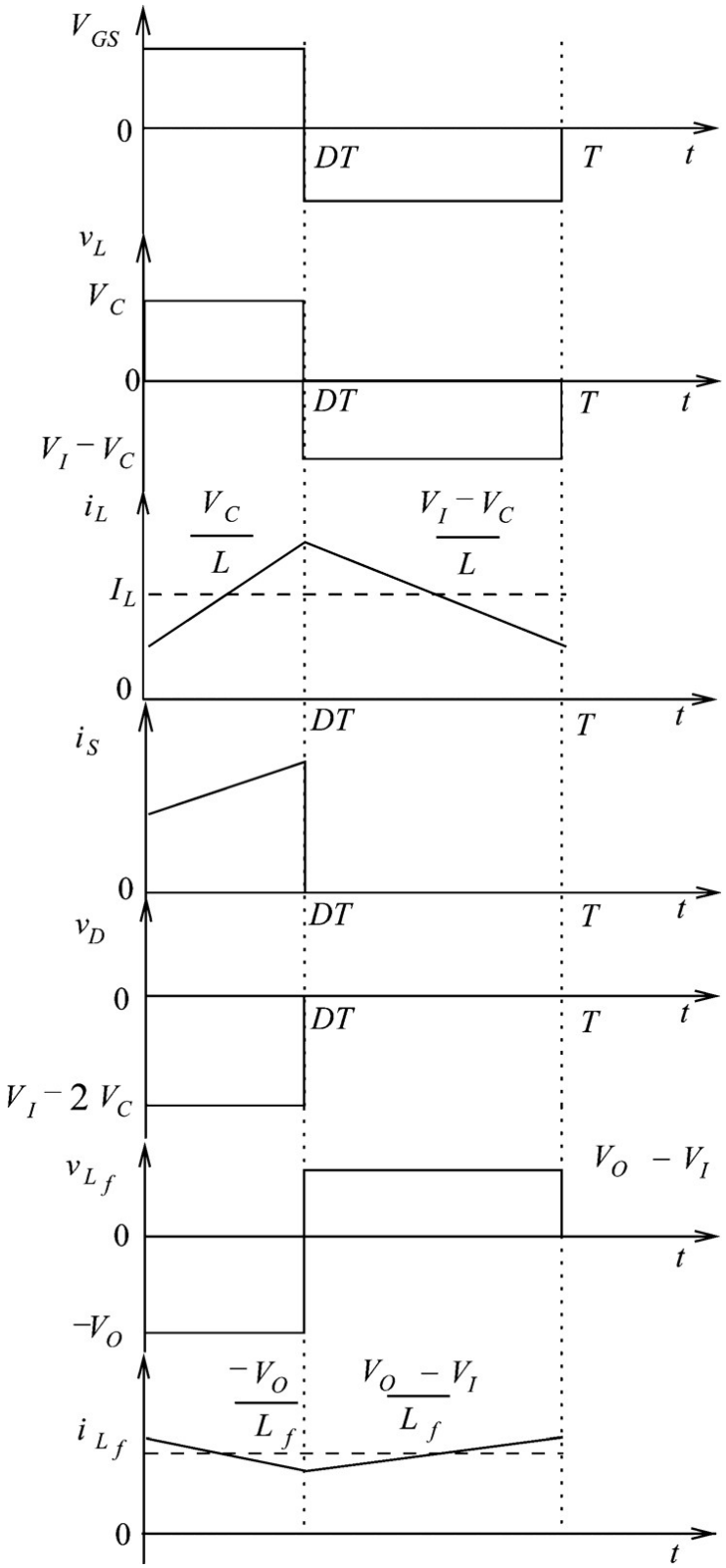

Figure 1.9: Importsnt z-source converter current and voltage waveforms in CCM [15].

1.3 Voltage Gain Expression Derivation

In this section, z-source voltage gain expression is calculated. The voltage gain of DC-DC converter is defined as the ratio of the output voltage to the input voltage. Inductors volt-second balance is used to calculate the voltage ratio. Inductor volt-second balance indicates that the integral of the inductor voltage should be zero in one switching period. So :

$$V_L = L\frac{di_L}{dt} \Longrightarrow \triangle i_L = \frac{1}{L}\int_0^T V_L(t)dt \tag{1.1}$$

Since inductor current is periodic, so $\triangle i_L = 0$. Then : $\int_0^T V_L(t)dt = 0$ Therefore we equation 1.1 can be simplified as bellow :

$$\int_0^{DT} V_L(t)dt = -\int_{DT}^{T} V_L(t)dt \tag{1.2}$$

$$\Longrightarrow V_C.DT = -(V_I - V_C)(1-D)T \tag{1.3}$$

$$\Longrightarrow (1-D)V_I = (1-2D)V_C \tag{1.4}$$

$$\Longrightarrow V_C = \frac{1-D}{1-2D}.V_I \tag{1.5}$$

Also volts.second balance for filter inductor L_f can be calculated as bellow:

$$\Longrightarrow -V_O.DT = -(2V_C - V_I - V_O)(1-D)T \tag{1.6}$$

$$\Longrightarrow 2(1-D)V_C = (1-D)V_I + V_O \tag{1.7}$$

Therefore, voltage gain expression of z-source DC-DC converter can be calculated

Based on two equations 1.5 and 1.7 as bellow :

$$\mathbf{M = \frac{V_O}{V_I} = \frac{1 - D}{1 - 2D}} \tag{1.8}$$

So the voltage gain expression is the function of duty cycle (D) Therefore voltage gain of z-source converter can be controlled with changing the duty cycle. With comparing two equations 1.5 and 1.8, it is proved that capacitors voltage (V_C) is equal to output voltage V_O.

Moreover, the output DC current to input DC current ratio can be calculated as bellow :

$$V_O I_O = V_I I_I \tag{1.9}$$

$$\Longrightarrow M_I = \frac{1 - 2D}{1 - D} \tag{1.10}$$

1.4 CCM Operation Mode

In this section, the minimum inductor (L) value is calculated. It is a inductor (L) value that is needed for operating in the continuous conduction mode (CCM).

$$i_L(t) = \frac{1}{L} \int_0^t v_L dt + i_L(0) \tag{1.11}$$

Therefore, following equations are for the first time interval of a switching period :

$$v_L = L\frac{di_L}{dt} = V_C \tag{1.12}$$

$$\Longrightarrow i_L(t) = \frac{V_C}{L}t + i_L(0) \tag{1.13}$$

$$\Longrightarrow i_L(DT) = \frac{V_C}{L}(DT) + i_L(0) \tag{1.14}$$

$$\Longrightarrow \Delta i_L = i_L(DT) - i_L(0) = \frac{V_C D}{f_s L} \tag{1.15}$$

It was proved earlier that $V_C = V_O$, therefore based on equation 1.14 :

$$i_L(DT) = \frac{V_O}{L}(DT) + i_L(0) \tag{1.16}$$

$$\Longrightarrow i_L(DT) = \frac{V_O D}{f_s L} + i_L(0) \tag{1.17}$$

So in the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM), $i_L(0)$ is equal to zero. Therefore, the peak inductor current can be calculated as bellow :

$$i_L(DT) = \Delta(i_L) = \frac{V_O D}{f_s L} \tag{1.18}$$

Then, dc input current can be calculated. It is equal to dc inductor (L) current, so at the boundary of CCM/DCM :

$$I_{IB} = I_{LB} = \frac{\Delta i_L}{2} = \frac{V_O D}{2 f_s L} \tag{1.19}$$

Subscript (B) denotes the boundary characteristic. Based on equations 1.10 and 1.19 :

$$I_{OB} = \frac{D(1-2D)V_O}{2(1-D)f_sL} \tag{1.20}$$

$$\Longrightarrow R_{LB} = \frac{2(1-D)f_sL}{D(1-2D)} \tag{1.21}$$

So the output DC current and output load resistance are calculated at the boundary of CCM/DCM. Now it is need to calculate the maximum output DC current at the boundary :

$$\frac{dI_{OB}}{dD} = \frac{V_O}{2f_sL}(2D^2 - 4D + 1) = 0 \tag{1.22}$$

The root of this equation is $D = 0.292$ and therefore the maximum output DC current is equal to :

$$I_{OBmax} = 0.0858\frac{V_O}{f_sL_{min}} \tag{1.23}$$

$$\Longrightarrow L_{min} = 0.0858\frac{V_O}{f_sI_{OBmax}} \tag{1.24}$$

$$\Longrightarrow I_{OBmax} = I_{Omin} = \frac{V_O}{R_{Lmax}} \tag{1.25}$$

Therefore, the minimum inductance value for being in CCM mode [15] can be calculated as bellow : :

$$L > L_{min} = 0.0858\frac{R_{Lmax}}{f_s} \tag{1.26}$$

This is the minimum inductor (L) value required for being in the CCM mode.

2. LITERATURE REVIEW

In this chapter, increasing DC-DC converter voltage gain methods, that have been used in another converters, are extracted. These methods are classified and analysed. Then, They are used to propose a novel DC-DC converters based on z-source converter in next chapters and they will be analyzed. Also, comparison results between the conventional converters and proposed converter are provided in next chapters.

2.1 Conventional Boost DC-DC Converter

Boost DC-DC Converter, is the most basic converter to increase the dc voltage. Figure 2.1 indicates the dc-dc boost converter topology. As it is shown in this figure, it contains one active switch S and a diode D_0. The switch and diode operate in complementary manner and switch S can be controlled with PWM method.

Therefore, when switch S is turned on, the diode is turned off . The energy is being stored in inductor L in this operation mode and in the next mode of operation, switch S is off and diode D_0 is on and the energy is being transferred to the output. Ripples are ignored in the inductor L current and capacitor C voltage, since it is assumed that the inductor and capacitor are large enough.

Therefore it is assumed that inductor L current and capacitor C voltage is constant. The input current is continuous, since inductor is located at the input of this converter.

Figure 2.2 shows the completed block diagram of using boost converter to increase the input voltage. As it is shown in this block diagram, a feedback is gotten from the output voltage and it is converted to digital value with (ADC) module, then based on the error of the output voltage, PWM signal is generated with microcontroller

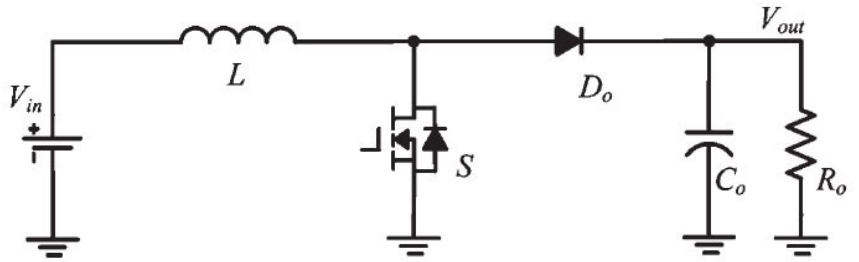

Figure 2.1: Boost dc-dc converter topology

and this signal is commanded to the gate of the active switch S.

Boost converter operation principle is divided to two modes. One for the on time of active switch S and one is for it's off time.

1) $0 \leq t < DT$

This operation mode is started when switch S is turned on and then diode D_0 is turned off, since it's voltage is equal to $(-V_O)$. The energy is stored in inductor L and because it's voltage is constant (inductor L voltage is equal to V_{in}), it's current is being increase linearly. In this mode of operation, output capacitor (C) is being discharged and it supplies current to the load.

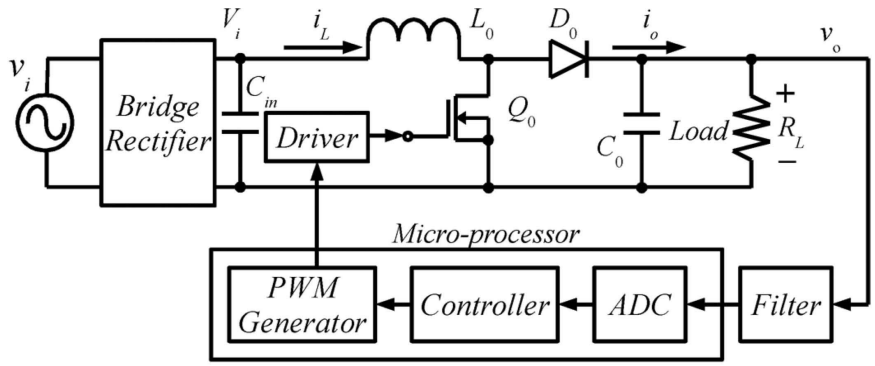

Figure 2.2: Conventional boost converter with control loop [30].

2) $DT \leq t \leq T$

This operation mode is started when active switch S is turned off, then diode D_0 is turned on. When switch S is turned off, the drain to source voltage is being increased, so it leads to get the diode to be turned on. The inductor L voltage is equal to $(V_{in} - V_O)$ and because this is the negative and constant voltage, inductor current is being decreased linearly in this operation mode. So the energy is being transferred to the output and the capacitor C_O is charged because the diode current supplies the capacitor and the load. So the energy is transferred to the output in this mode. Transfer time can be decreased by increasing duty cycle (D).

Figure 2.3 shows the important waveforms of conventional boost converter. Voltage gain expression of the boost converter can be calculated with using volts.second balance of inductor (L). Therefore :

$$V_{in}.DT = -(V_{in} - V_{out})(1 - D)T \tag{2.1}$$

$$\Rightarrow V_{in} = (1 - D)V_{out} \tag{2.2}$$

$$\Rightarrow M_v = \frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \tag{2.3}$$

As it is shown in equation 2.1, the input voltage just can be increased by the conventional boost converter and it can not be decreased. Stress voltage of the main switch S can be calculated in the second operation mode when switch S is off and stress voltage of diode D_0 can be calculated in first operation mode, when diode D_0 is off. Therefore :

$$\Rightarrow V_S = V_{D_0} = V_{out} \tag{2.4}$$

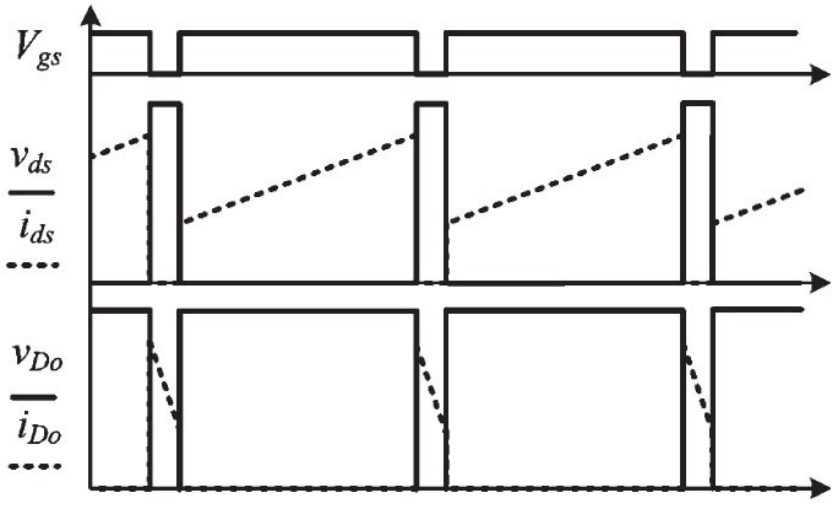

Figure 2.3: Important waveform of conventional boost converter. [30]

Based on equation 2.4, the stress voltage of semiconductor devices is high in the conventional boost dc-dc converter and this feature is one of the disadvantages of dc-dc boost converter.

Figure 2.4 indicates current bidirectional boost converter. The energy can be transferred from input to output or from output to the input in this converter.

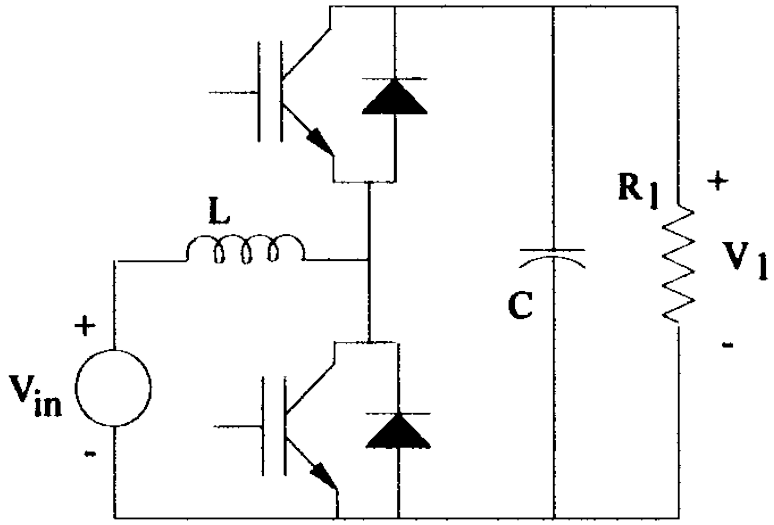

Figure 2.4: Bidirectional current boost converter [5]

2.2 Three Level Boost Converter

Three level boost converter is derived from the conventional boost converter and has more switches in comparison to conventional dc-dc boost converter. The advantage of this converter is that the voltage stress of switches and diodes is half of the semiconductor devices in the conventional boost converter. It includes two switches S_1 and S_2, two diodes D_{o1} and D_{o2}, two output capacitors C_{o1} and C_{o2} and the input inductor L_1 [26], [27]. Figure 2.5 shows the topology of this converter.

The operation principle of this converter can be divided to 4 modes of operation, since it includes two main switches.

1) $t_0 \leq t \leq t_1$

In this operation mode, both switches S_1 and S_2 are on, so the voltage across the diodes is the negative value (because of the output capacitors voltage) and that is why the diodes D_{o1} and D_{o2} are off. Because the inductor L_1 voltage is constant and positive, this inductor current is being increased linearly and with the constant slope.

The output capacitors are discharged and their current supplies the load current.

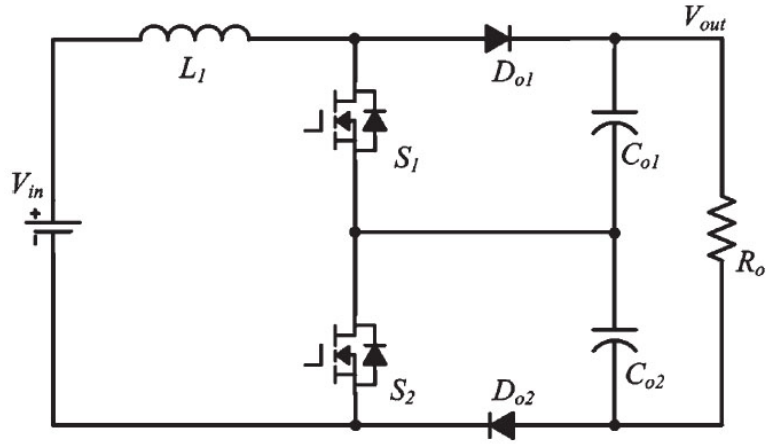

Figure 2.5: Three level boost converter

Therefore, these set of equations can be written for this operation mode :

$$V_{Do1} = V_{Co1} = \frac{V_{out}}{2} \tag{2.5}$$

$$V_{Do2} = V_{Co2} = \frac{V_{out}}{2} \tag{2.6}$$

$$V_{L1} = V_{in} \tag{2.7}$$

2) $t_1 \leq t \leq t_2$

This operation mode is started when switch S_1 is turned off and so diode D_{o1} is turned on. In this operation mode, the capacitor C_{o1} is charged through diode D_{o1} and inductor L_1 is discharged. Since it's voltage is negative and constant, so it's current is being decreased linearly and with a constant slope. So these set of

equations can be written for this operation mode.

$$V_{S1} = V_{Co1} = \frac{V_{out}}{2} \tag{2.8}$$

$$V_{Do2} = V_{Co2} = \frac{V_{out}}{2} \tag{2.9}$$

$$V_{L1} = V_{in} - \frac{V_{out}}{2} \tag{2.10}$$

3) $t_2 \leq t \leq t_3$

In this operating mode, switch S_1 is turned on again and operation principle of this mode is the same as mode one. Therefore :

$$V_{Do1} = V_{Co1} = \frac{V_{out}}{2} \tag{2.11}$$

$$V_{Do2} = V_{Co2} = \frac{V_{out}}{2} \tag{2.12}$$

$$V_{L1} = V_{in} \tag{2.13}$$

3) $t_3 \leq t \leq t_4$

This operation mode is started when switch S_2 is turned off, so output capacitor C_{o2} is charged through diode D_2 and like the second operation mode. Input inductor L_1 in discharged and it's current is being decreased linearly, because it's voltage is negative and constant. Therefore these set of equations can be written for this operation mode :

$$V_{Do1} = V_{Co1} = \frac{V_{out}}{2} \tag{2.14}$$

$$V_{Do2} = V_{Co2} = \frac{V_{out}}{2} \tag{2.15}$$

$$V_{S1} = V_{in} - \frac{V_{out}}{2} \tag{2.16}$$

Voltage gain of this converter can be calculated base on inductor L_1 volts.second balance, Therefore :

$$V_{in}(2D-1)T = (V_{in} - \frac{V_{out}}{2}) \times 2(1-D)T \tag{2.17}$$

$$\Longrightarrow V_{in} = (1-D)V_{out} \tag{2.18}$$

$$\Longrightarrow M_v = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{2.19}$$

So the voltage gain expression is the same as conventional boost converter, the advantage of this converter is the lower stress voltage of semiconductor devices in comparison to conventional boost converter [26], [27]. Therefore, smaller size of switches and diodes can be used to design and build this converter.

2.3 Integrated Cascade Boost Converter

The boost dc-dc converter is used to increase input voltage. If two boost converters are used in series, output voltage can be increased more than conventional boost converter. It is called cascade boost converter. The main problem of this converter is that two switches are used instead of one main switch. So it makes the circuit more complex and it has complex PWM control module.

Figure 2.6 shows the topology of the cascade boost converter. As it is shown, two active switch S_1 and S_2 are used to make this converter. This feature makes gate drive circuits hard to control in general.

The other solution is to combine these two active switches and make the converter simpler. It still includes several components but one switch need to be controlled. This converter is called integrated cascade boost converter. Figure 2.7 shows the topology of this converter.

The operation principle of this converter is divided to two time intervals like another one switch converters. Generally in this converter, energy is stored in inductors L_1 and L_2 when switch S is on and the energy is transferred to the output when switch S is off.

Switch S and diode D_2 are turned on and off simultaneously and diodes D_0 and D_1 are turned on and off simultaneously. Also the input current is continuous sine we have inductor in the input. So we have two operation modes.

1) $0 \leq t < DT$

First mode is started when active switch S is turned on, so diode D_2 will be turned on. In this mode, inductors L_1 and L_2 are being charged because of their positive voltage. Also because of the constant and positive voltage, their current are being increased linearly and with the constant slope. In this mode, diodes D_0 and D_1 are

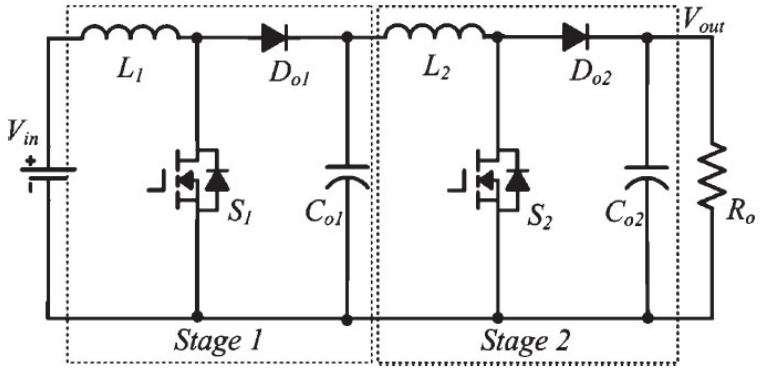

Figure 2.6: Cascade boost converter

off because of their negative voltage. Also capacitors C_1 and C_o are being discharged. Capacitor C_1 transfers it's energy to inductor L_2 and capacitor C_o supplies the load current. Therefore, these set of equations can be written for this operation mode :

$$v_{L1} = V_{in}, v_{L2} = V_{C1} \tag{2.20}$$

$$v_{D1} = v_{C1}, v_{Do} = V_{out} \tag{2.21}$$

2) $DT \leq t \leq T$

This operation mode is started when active switch S is turned off and simultaneously diode D_2 is turned off and diodes D_0 and D_1 are turned on. When switch S and diode D_2 are turned off, the anode voltage of diodes D_0 and D_1 are increased so they will be turned on. In this operation mode inductors L_1 and L_2 are being discharged because their voltage is negative, also their current are being decreased linearly. In this mode the energy is transferred to the output, so with increasing duty ratio, transfer time can be decreased. Therefore, these set of equations can be written for

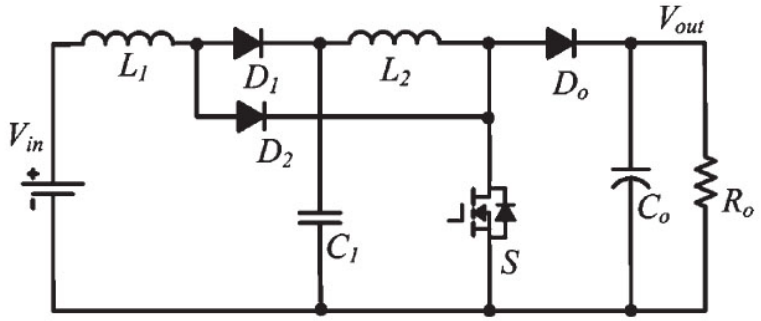

Figure 2.7: Integrated Cascade Boost Converter

this operation mode :

$$v_S = V_{out} \tag{2.22}$$

$$v_{D2} = v_{out} - V_{C1} \tag{2.23}$$

$$V_{L1} = V_{in} - V_{C1} \tag{2.24}$$

$$V_{L2} = V_{C1} - V_{out} \tag{2.25}$$

So voltage gain expression can be calculated with volts.second balance of inductors L_1 and L_2, so for inductor L_1 :

$$V_{in}.DT = (V_{in} - V_{C1})(1 - D)T \tag{2.26}$$

$$\Longrightarrow V_{in} = (1 - D).V_{C1} \tag{2.27}$$

$$\Longrightarrow V_{C1} = \frac{1}{1 - D}.V_{in} \tag{2.28}$$

Based on volts.second balance of inductor L_2 :

$$V_{C1}.DT = (V_{C1} - V_{out})(1 - D)T \tag{2.29}$$

$$\Longrightarrow V_{C1} = (1 - D).V_{out} \tag{2.30}$$

$$\Longrightarrow V_{out} = \frac{1}{1 - D}.V_{C1} \tag{2.31}$$

$$\Longrightarrow M_v = \frac{V_{out}}{V_{in}} = \frac{1}{(1 - D)^2} \tag{2.32}$$

So the voltage gain is increased in comparison to conventional boost converter for the same duty cycle. However, the converter became more complex and it has more number of components. Also the main switch S stress voltage is the same as boost converter. So the decision to choose one of them can be made by comparing them base on cost and the gain value [18], [50].

2.4 High Step-up Converters with Coupled Inductors

In this section, the converters are analyzed that use coupled inductor for increasing voltage gain. Therefore, these methods are extracted and used in z-source converter.

2.4.1 High Step-up Converter with a Coupled Inductor

Figure 2.8 shows this converter topology. As it is shown in this figure, a coupled inductor is used to increase voltage gain. So with increasing turn ratio of transformer, voltage gain can be increased. It includes an active switch S, two diodes D_c and D_o, two capacitors C_c and C_o and a coupled inductors. Two diodes and switch are turned off and on in complementary manner in each switching period. Inductor L_{LK} is the leakage inductance off coupled inductor.

The general operation principle of this converter is that the energy is stored in Inductor L_1 when switch S is on and this energy is transferred to the output when switch S is off. So it is similar to conventional boost converter.

However, the difference is that when switch S is turned off, a voltage is induced across inductor L_2 and output voltage is increased, since inductor L_2 is located in the

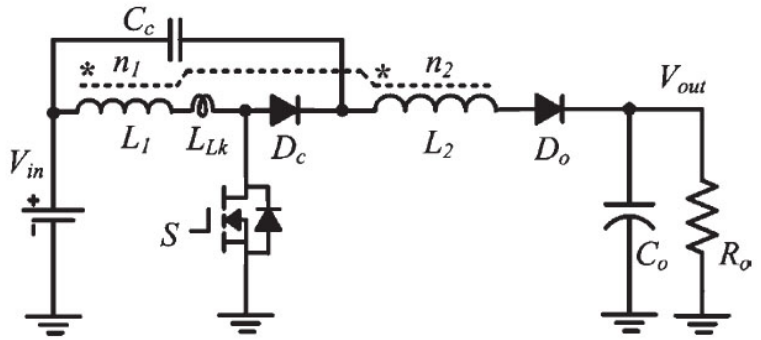

Figure 2.8: High step up converter with one coupled inductor topology

main loop of this converter. So the higher voltage gain is expected than conventional boost converter. Capacitor C_c is used to clamp the active switch S voltage when it is off.

Since this converter includes a main active switch, each switching period can be divided to two time intervals.

1) $0 \leq t < DT$

This operation mode is started when switch S is turned on. So the input voltage is applied across inductor L_1(leakage inductance L_{LK} can be ignored in the calculations since it is small) and n times of this voltage is induced across inductor L_2. In this time interval, diodes D_c and D_o are off since their voltage is negative. Since diode D_o is off, there is no current through inductor L_2 and so the energy just is stored in it's magnetizing inductance. So these two inductors store energy and capacitor C_o supplies load current and is being discharged. So these set of equations can be written in this time interval.

$$V_{Dc} = V_{in} + V_{Cc} \tag{2.33}$$

$$V_{L1} = V_{in}, V_{L2} = n.V_{in} \tag{2.34}$$

$$n = \frac{n_2}{n_1} \tag{2.35}$$

Where n_1 is the number of inductor L_1 turns and n_2 is the number of inductor L_2 turns.

2) $DT \leq t \leq T$

This operation mode is started when active switch S is turned off. Then switch voltage is increased and so diode D_c is turned on and switch voltage is clamped to $V_S = V_{in} + V_{Cc}$. In this operation mode, Inductor L_1 voltage is negative so it is discharged and because diode D_o is on, capacitor C_o is charged [51].

The voltage gain of this high step up converter can be calculated by using inductors volts.second balance and simple KVL when switch S is off. Therefore :

$$V_{in}.DT = -(-V_{Cc}).(1-D)T \tag{2.36}$$

$$\Longrightarrow V_{Cc} = \frac{D}{1-D}.V_{in} \tag{2.37}$$

$$KVL \Longrightarrow V_{out} = V_{in} + V_{Cc} + n.V_{Cc} \tag{2.38}$$

$$\Longrightarrow V_{out} = V_{in} + (n+1).\frac{D}{1-D}.V_{in} \tag{2.39}$$

$$\Longrightarrow M_v = \frac{V_{out}}{V_{in}} = \frac{1+n.D}{1-D} \tag{2.40}$$

As it is shown in equation 2.40, the voltage gain is more than conventional boost converter for the same duty ratio and it can be increased by increasing turn ratio n.

2.4.2 Flyback-Boost Converter with a Coupled Inductor

A transformer is used in flyback converter to achieve high voltage gain. It includes an active switch S, a diode in secondary side and an output capacitor. Generally speaking, the energy is stored in primary side when switch S is on. Then in the second mode of operation, the diode in the secondary side is turned on and the

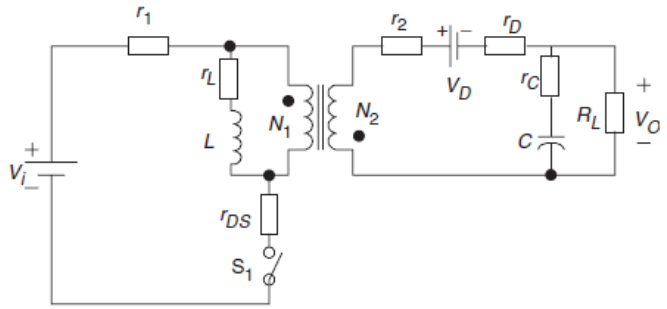

Figure 2.9: Flyback converter topolgy with parasitic components [25]

energy is transferred to the output. Figure 2.9 shows the flyback converter topology with parasitic components.

So for increasing voltage gain of flyback converter, it can be combined with conventional boost converter. Figure 2.10 shows this converter topology. As it is shown in this figure, flyback converter transformer is combined with output filter inductor of boost converter. It includes two diodes D_{o1} and D_{o2}, one active switch S and two output capacitors C_{o1} and C_{o2}.

Generally it works like the conventional boost or flyback converter. The energy is stored in the mutual core of transformer when switch S in on and it is transferred to the output when switch S is off and diodes D_{o1} and D_{o2} are on. Since it just has one active switch, the operation principle of this converter can be divided to two time interval.

1) $0 \leq t \leq DT$

This operation mode is started when switch S is turned on.

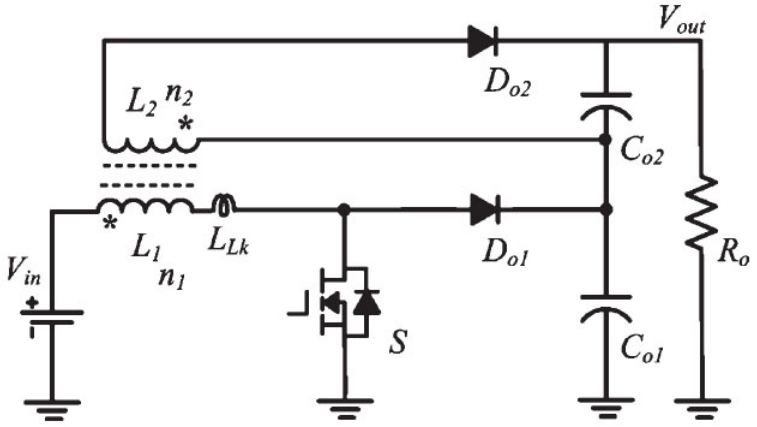

Figure 2.10: Flyback-boost converter topology

Then the input voltage is applied across inductor L_1 and n times of this voltage

is induced across inductor L_2, so diode D_{o2} is reverse biased and no current flows through secondary side of transformer. So the energy is stored in the magnetizing inductance of inductor L_2. In this time interval, the output capacitors supply the output current. So this set of equations can be written for this time interval :

$$v_{L1} = V_{in}, v_{L2} = n.V_{in} \tag{2.41}$$

$$n = \frac{n_2}{n_1} \tag{2.42}$$

$$V_{Do1} = V_{o1} \tag{2.43}$$

$$V_{Do2} = n.V_{in} + V_{o2} \tag{2.44}$$

2) $DT \leq t \leq T$

This operation mode is started when switch S is turned off. Then the diode D_{o1} is turned on. A negative voltage is applied across inductor L_1 and si Inductor L_2, so the diode D_{o2} is turned on. So in this time interval capacitors C_{o1} and C_{o2} are being charged and the diodes current supply the load current. This set of equations can be written for this time interval :

$$V_S = V_{o1} \tag{2.45}$$

$$v_{L1} = V_{in} - V_{o1} \tag{2.46}$$

Volts.second balance of coupled inductors and a simple KVL when switch S is off, are used to find the voltage gain. So this set of equations can be written for volts.second

balance of inductor L_1 :

$$V_{in}.DT = -(V_{in} - V_{o1})(1 - D)T \tag{2.47}$$

$$\Longrightarrow V_{in} = (1 - D).V_{o1} \tag{2.48}$$

$$\Longrightarrow V_{o1} = \frac{1}{1 - D}.V_{in} \tag{2.49}$$

Using the simple KVL when switch S is off :

$$V_{o2} = -v_{L2} = n.(V_{o1} - V_{in}) \tag{2.50}$$

So based on equations 2.49 and 2.50 :

$$V_{out} = V_{o1} + V_{o2} = V_{o1} + n.V_{o1} - n.V_{in} \tag{2.51}$$

$$V_{out} = (1 + n).\frac{1}{1 - D}.V_{in} - n.V_{in} \tag{2.52}$$

$$M_v = \frac{V_{out}}{V_{in}} = \frac{1 + n.D}{1 - D} \tag{2.53}$$

As it is shown, the voltage gain of this converter is equal to the converter with a coupled inductor [25] [47], but more than conventional boost converter. The stress voltage of semiconductor devices is almost the same.

2.4.3 Flyback-Boost Converter with Voltage Multiplier

This converter principle is very similar to flyback-Boost converter with a coupled inductor that we hade in previous section, just a voltage multiplier is added to the output for increasing voltage gain. As it is shown for the flyback-Boost converter with a coupled inductor, positive and negative voltage pulses has been applied across inductor L_1 when active switch S is turned on and off. Therefore,

Figure 2.11 shows the converter topology. As you see for the flyback-Boost converter with a coupled inductor, positive and negative voltage pulses has been applied across inductor L_1 when active switch S is turned on and off. Therefore, the similar voltage pulses were induced across inductor L_2, then these pulses were rectified with a output diode and then this rectified voltage was used to charge the output capacitor. So negative pulses was just used to charge the output capacitor in previous converter. However, in this converter, both positive and negative pulses are used to charge output capacitors.

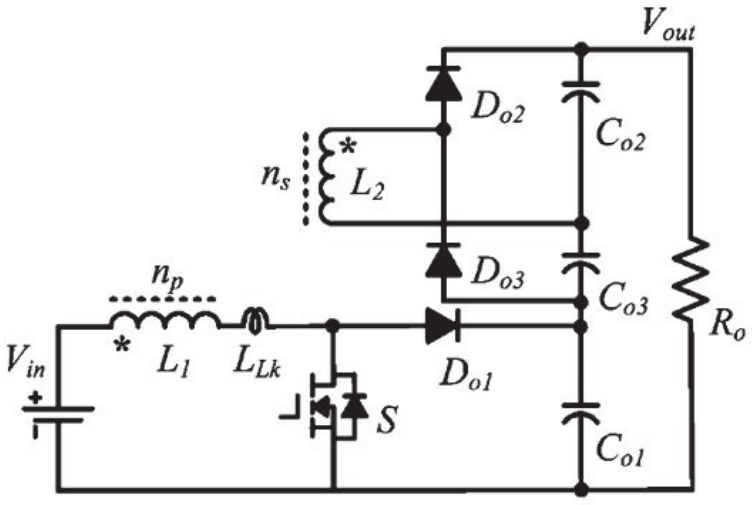

Figure 2.11: Flyback-boost converter with voltage multiplier topology

So in this converter positive voltage pulses charge capacitor C_{o2} through diode D_{o2} and negative voltage pulses charge capacitor C_{o3} through diode D_{o3}. Generally speaking, energy is stored in the mutual core of coupled inductors when switch S is on and part of this energy is transferred to the capacitor C_{o2} simultaneously and rest of the energy is transferred to the output when switch S is off. Therefore switch S and diode D_{o2} are turned on and off simultaneously and switch S and diodes $D_{o1}$and D_{o3} are turned off and on in complementary manner.

The operation principle of this converter is divided to two modes since it includes one active switch. So :

1) $0 \leq t \leq DT$

This operation mode is started when switch S is turned on. Then, input voltage is applied across inductor L_1 and then n times of this voltage is induced across inductor L_2.

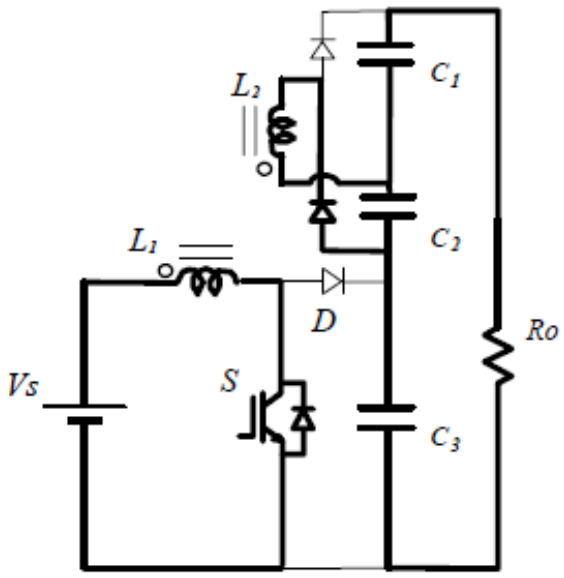

Figure 2.12: Flyback-boost converter with voltage multiplier first mode of operation. [4]

n is the turn ratio of coupled inductors. So diode D_{o2} is turned on because of the positive voltage across it and diode D_{o3} is reverse-biased because of negative voltage across it. Also since the active switch S is on, diode D_{o1} is reverse-biased. So in this operating mode, Inductor L_1 current is being increased linearly and energy is stored in the mutual core of coupled inductors and capacitor C_{o2} is charged and capacitors C_{o1} and C_{o3} are discharged and supply current to the load. Figure 2.12 shows the equivalent circuit of this mode. These are the sets of equations for this operation mode :

$$V_{L1} = V_{in}, V_{L2} = n.V_{in} \tag{2.54}$$

$$V_{Do1} = V_{o1}, V_{Do3} = V_{o2} + V_{o3} \tag{2.55}$$

2) $DT \leq t \leq T$

This operation mode is started when switch S is turned of. Then the anode voltage of diode D_{o1} is increased so this diode is turned on and capacitor C_{o1} is charged. A negative voltage is applied across inductor L_1 and so L_2 then diode D_{o2} is reverse-biased and diode D_{o3} is turned on. Therefore the rest of input energy is transferred to the output and capacitor C_{o3} is charged. Figure 2.13 shows the equivalent circuit of this mode. These are the set of equations of this mode :

$$V_{L1} = V_{in} - V_{o1}, V_{L2} = n.(V_{in} - V_{o1}) \tag{2.56}$$

$$V_s = V_{o1}, V_{Do2} = V_{o2} + V_{o3} \tag{2.57}$$

Voltage gain of this converter can be calculated by using the volts.second balance of inductor L_1 and two KVLs when switch S is on and off. Therefore, this set of

equations can be written :

$$V_{in}.DT = -(V_{in} - V_{o1})(1 - D).T \tag{2.58}$$

$$\Rightarrow V_{o1} = \frac{1}{1 - D}.V_{in} \tag{2.59}$$

$$S = on \Rightarrow V_{o2} = V_{L2} = n.V_{in} \tag{2.60}$$

$$S = off \Rightarrow V_{o3} = -V_{L2} = n.(V_{o1}V_{in}) \tag{2.61}$$

$$\Rightarrow V_{out} = V_{o1} + V_{o2} + V_{o3} = (n + 1)V_{o1} \tag{2.62}$$

$$\Rightarrow M_v = \frac{V_{out}}{V_{in}} = \frac{1 + n}{1 - D} \tag{2.63}$$

As it is shown, the voltage gain is increased in comparison to previous converter [4]. Therefore, this idea will be used to combine our base converter with flyback converter

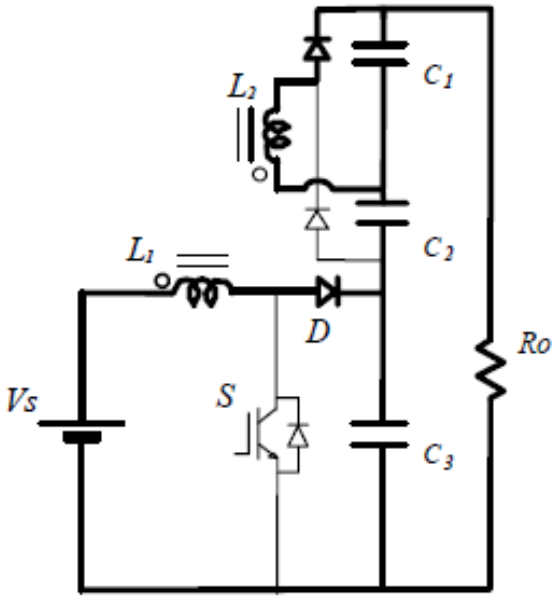

Figure 2.13: Flyback-boost converter with voltage multiplier second mode of operation [4].

and voltage multiplier and coupled inductor in next chapters to achieve high voltage gain for z-source converter and then, it will be analyzed.

2.4.4 Improved Flyback-Boost Converter with Coupled Inductors

This converter topology is derived from flyback-boost converter with a coupled inductor. It includes two coupled inductors and four diodes. Those diodes are turned on and off with active switch S in the complementary manner.

Operation principle of this converter is like that when switch S is turned on, energy is stored in the mutual core of coupled inductors and it transferred to the output when switch S is turned off and output capacitors will be charged. Turn ratio of the coupled inductors can be defined as following equations :

$$n_1 := \frac{n_{s1}}{n_{p1}} \tag{2.64}$$

$$n_2 := \frac{n_{s2}}{n_{p2}} \tag{2.65}$$

Since this converter includes a main active switch, operation principle of this converter can be divided to two operation modes :

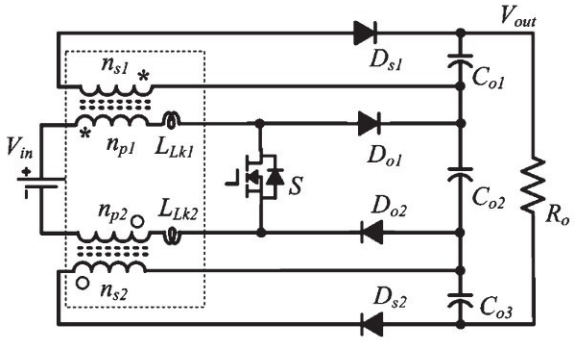

Figure 2.14: Improved flyback-boost converter with coupled inductors.

1) $0 \leq t < DT$

This operation mode is started when the active switch S is turned on, then all the diodes are turned off. In this mode, if it is assumed that inductors L_{p1} and L_{p2} are equal, the half of input voltage will apply across each inductor and so their magnetizing current is increased and the energy is stored in their core. In this mode, output capacitors are discharged and they supply the load current.This set of equations can be written for this operation mode :

$$V_{Lp1} = V_{Lp2} = \frac{V_{in}}{2} \tag{2.66}$$

$$V_{Do1} = V_{Do2} = \frac{V_{o2}}{2} \tag{2.67}$$

2) $DT \leq t \leq T$

This operation mode is started when switch S is turned off. Then, the diodes are turned on and output capacitors will be charged. In this operation mode, the stored energy in the inductors, are being transferred to the output. Therefore, this set of equations canbe written for this time interval :

$$V_s = V_{o2} \tag{2.68}$$

$$V_{Lp1} = V_{Lp2} = \frac{V_{in} - V_{o2}}{2} \tag{2.69}$$

Voltage gain of this converter can be calculated by using the coupled inductors volts.second balance and also two KVLs when switch S is off and on. Therefore :

$$Volts.second \Longrightarrow L_{p1} \Longrightarrow \frac{V_{in}}{2}.DT = \frac{V_{in} - V_{o2}}{2}(1-D).T \tag{2.70}$$

$$\Longrightarrow V_{o2} = \frac{1}{1-D}.V_{in} \tag{2.71}$$

We use two KVLs for the switch off time and on time:

$$KVL \Longrightarrow S = off \Longrightarrow V_{o1} = -V_{Ls1} = n_1.\frac{V_{o2} - V_{in}}{2} \tag{2.72}$$

$$KVL \Longrightarrow S = on \Longrightarrow V_{o3} = -V_{Ls2} = n_2.\frac{V_{o2} - V_{in}}{2} \tag{2.73}$$

$$\Longrightarrow V_{out} = V_{o1} + V_{o2} + V_{o3} = (\frac{n_1 + n_2}{2} + 1).V_{o2} - \frac{n_1 + n_2}{2}.V_{in} \tag{2.74}$$

$$\Rightarrow M_v = \frac{V_{out}}{V_{in}} = \frac{2 + (n_1 + n_2).D}{2 \times (1 - D)} \tag{2.75}$$

So if it is assumed that turn ration for both coupled inductors are the same :

$$n_1 = n_2 \Rightarrow M_v = \frac{V_{out}}{V_{in}} = \frac{1 + n.D}{1 - D} \tag{2.76}$$

So the same voltage gain is achieved as what was gotten for the flyback-boost converter with a coupled inductor. Some advantages of this converter in comparison to previous one are as following :

✓Common mode conducted EMI is reduced.

✓Higher voltage gain can be achieved with changing coupled inductors turn ratio. [12]

2.5 High Step-Up Converters with Switched Capacitors

The capacitor is used as a voltage supply in this kind of converters and so higher voltage gain can be achieved. Also another advantage of these converters are that no inductor or transformer is used in this kind of converters, Therefore, frequency can be increased by several mega Hertz and therefore power density can be increased. Also the input current is pulsating. Another disadvantage of these converters is that the output regulation is weak due to the variation of load. In these kind of converter, output voltage will be proportional to the input voltage.

capacitor is used to achieve high voltage gain in several kind of high step-up converters, however, because their operation principle is nearly similar to each other, one of them is analyzed.

In this section, N-Stage Switched Capacitor Resonant Converter is analyzed. As it is shown in figure 2.15, this cell includes two diodes D_{1n} and D_{2n} and two capacitors C_{1n} and C_{2n}. Series set of these cells can be used to achieve high voltage gain. Figure 2.16 shows this converter topology. As it is shown, n switching capacitor cells can be used in this converter.

Because of the resonance characteristic of this converter, all the switches and diodes are switched at ZCS (zero current switching) and so the loss will be decreased and efficiency will be increased. Also, current spikes are removed with this method. There are current spikes in the converters that use capacitor for increasing voltage gain, when the capacitor is charged or discharged, current spikes is appeared. However, in these resonant converters, they will be disappeared. Small inductance L_r is used not for storing energy but for the resonance. So because this is a small inductance, the frequency can be increased and also our converter weight and size are decreased.

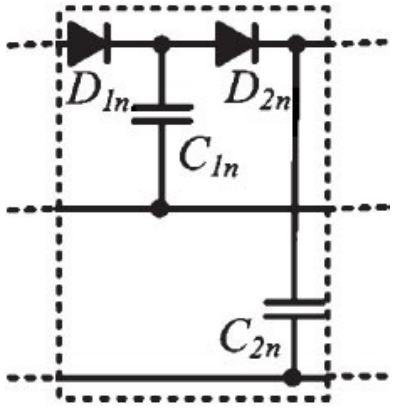

Figure 2.15: Switching capacitor cells that are used in n-Stage switched capacitor resonant converter

Another advantage of these converters is that various output voltages can be gotten across each of the capacitors C_{1a}, C_{1b} ... C_{1n} and each one has different voltage gain but the output voltage will be proportional to input voltage.

For analyzing these kind of converters, it is assumed that there exists two switching capacitor cells(double mode) or three capacitor cell (triple mode). The triple one is analyzed and it's operation modes is explained. Figure 2.17 shows the double-mode resonant converter. Figure 2.18 shows the triple mode case.

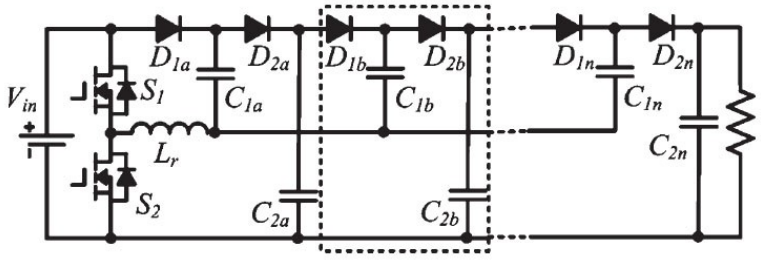

Figure 2.16: N-Stage switched capacitor resonant converter topology

Therefore, triple-mode switched capacitor resonant converter will be analyzed.

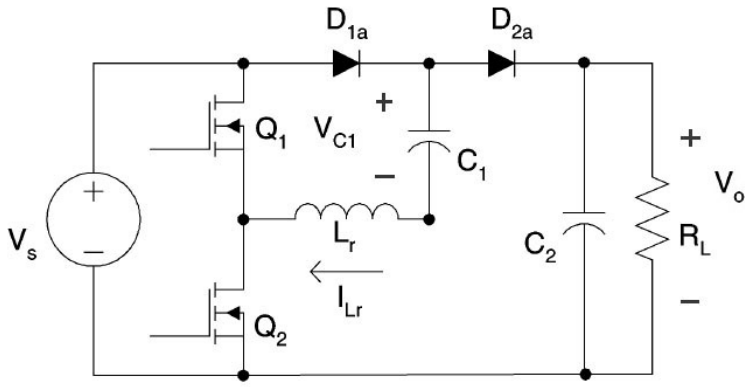

Figure 2.17: Double-mode switched capacitor resonant converter

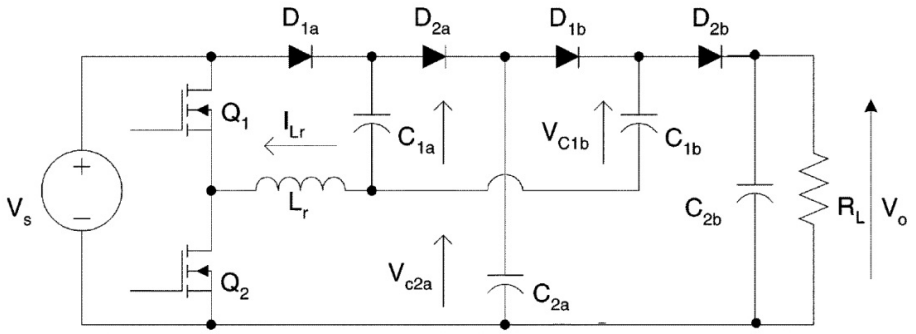

Figure 2.18: Triple-mode switched capacitor resonant converter

As it is shown in figure 2.18, it includes two active switches Q_1 and Q_2. Just one of these two switches is on at a time or both of them are off. Active switch Q_2 and diodes D_{1a} and D_{1b} are turned on and off simultaneously and also switch Q_1 and diodes D_{2a} and D_{2b} are turned on and off simultaneously.

Generally speaking, the operation principle of this converter is that two capacitors C_{1a} and C_{1b} are charged through diodes D_{1a} and D_{1b} and capacitors C_{2a} and C_{2b} are discharged when switch Q_2 is on and capacitors C_{2a} and C_{2b} are charged through diodes D_{2a} and D_{2b} and capacitors C_{1a} and C_{1b} are discharged when switch Q_1 is off.

Since this converter includes two active switches, it's operation principle can be divided to four operation modes :

1) $t_0 \leq t \leq t_1$

This operation mode is started when switch Q_2 is turned on. Then Capacitor C_{1a} is charged through diode D_{1a} and with resonant with inductor L_r. Since inductor L_r is small, the voltage of capacitor C_{1a} will be the input voltage. Also Capacitor C_{1b} is charged through diode D_{1b} ans it's voltage will be equal to capacitor C_{2a}, so capacitor C_{2a} is being discharged. Also capacitor C_{2b} is discharged in this operating mode and it supplies the load current.

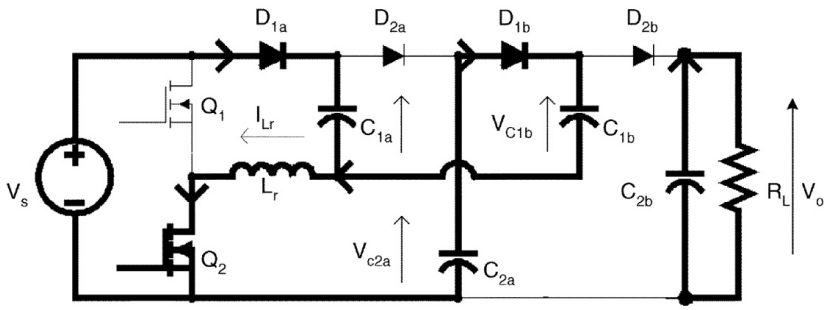

Figure 2.19: Equivalent circuit for the first mode

The following equation expresses the semiconductor devices stress voltage :

$$V_{Q1} = V_{D2a} = V_{D2b} = V_S \tag{2.77}$$

2) $t_1 \leq t \leq t_2$

This operation mode starts when the switch Q_2 is turned off. So in this operation mode both switches Q_1 and Q_2 and all the diodes D_{1a}, D_{1b}, D_{2a} and D_{2b} are off. So

the capacitor C_{2b} is discharged and supplies the load current in this operation mode. Figure 2.20 indicates the equivalent circuit of this mode.

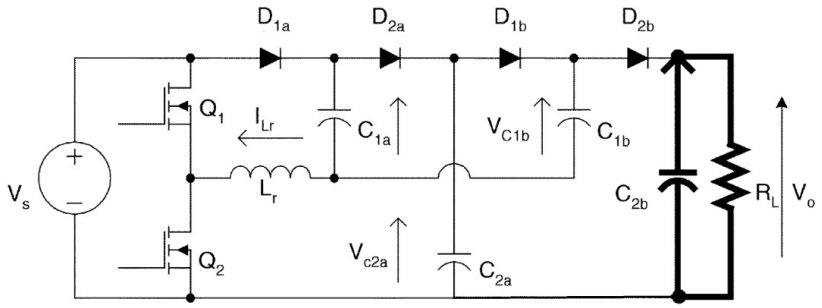

Figure 2.20: Equivalent circuit for the second mode

The following equation expresses the semiconductor devices stress voltage :

$$V_{Q1} = V_{D2a} = \frac{V_S}{2} \tag{2.78}$$

3) $t_2 \leq t \leq t_3$

This operation mode is started when switch Q_1 is turned on. Then Capacitor C_{2a} is charged through diode D_{2a} and with resonant with inductor L_r. Also Capacitor C_{2b} is charged through diode D_{2b} and it's voltage will be equal to capacitor C_{1b} plus the input voltage, so capacitor C_{1a} is being discharged. Also capacitor C_{1b} is discharged in this operating mode. So the capacitors voltage can be calculated by following

equations :

$$V_{C1a} = V_S \tag{2.79}$$

$$V_{C2a} = V_S + V_{C1a} = 2 \times V_S \tag{2.80}$$

$$V_{C1b} = V_{C2a} = 2 \times V_S \tag{2.81}$$

$$V_{C2a} = V_S + V_{C1b} = 3 \times V_S \tag{2.82}$$

Also the following equation expresses the semiconductor devices stress voltage :

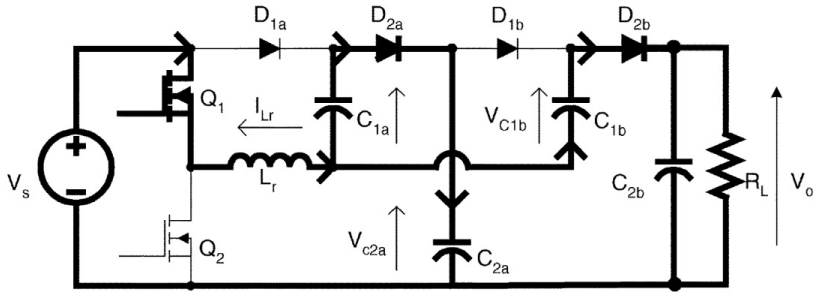

Figure 2.21: Equivalent circuit for the third mode

$$V_{Q2} = V_{D1a} = V_{D1b} = V_S \tag{2.83}$$

3) $t_3 \leq t \leq t_4$

This operation mode is started when switch Q_2 is turned off. The equivalent circuit and operation principle of this mode is very similar to the second mode. So all the switches and diodes are off in this operation mode and capacitor C_{2b} supplies the load current.

Therefore, two times or three times of input voltage can be applied across two capacitors C_{2a} and C_{2b} and the more can be applied if more switching capacitor cells are used in the network for this converter.

As it is shown in equation 2.82, continuous voltage gain can not be achieved like previous converter with changing duty ratio for this converter [11]. The semiconductor devices stress voltage is equal to input voltage. So it is less than conventional converters like boost converter and it is one of the advantages of this converter.

2.6 High-Step-Up Converters with Inductor and Switched Capacitor

In this section, the converters are analyzed that use both inductor and switched capacitor cell for increasing voltage gain. So we will analyze their operation principles and derive a important equations and voltage gain expression.

2.6.1 Integrated Cascade boost Converter Mixed with Switched Capacitor Cell

Integrated Cascade boost converter topology was shown in figure 2.7. This new converter is very similar to that converter, however, a switched capacitor cell just is added to increase the voltage gain. As it is shown in the topology of this converter in figure 2.22, a LC high pass filter is added to the output of integrated cascade boost.

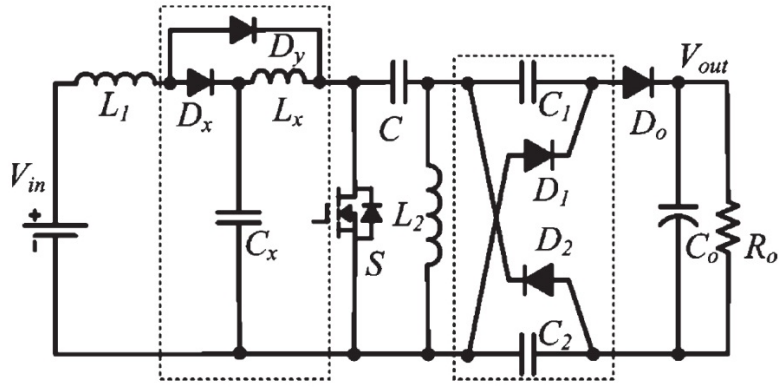

Figure 2.22: Combination of Integrated Cascade boost Converter with Switched Capacitor Cell Topology

Generally speaking when active switch S is turned off and on, positive and negative voltage pulses will be created across the switch, so the DC part of these pulses is deleted when they are passed through LC high pass filter and so these negative and positive pulses charge the capacitors C_1 and C_2.

As it is shown in the figure 2.22, this converter includes five diodes and one main active switch. Switch S is switched with diodes D_Y,D_1 and D_2 simultaneously and

switch S operates with diodes D_X and D_o in complementary manner. Therefore, when switch S is turned on, the energy is stored in inductors L_1 and L_X and the capacitors C_1 and C_2 are charged and when switch S is turned off, these energies are transferred to the output by the output diode D_o .

Since it includes one main switch, the operation principle of this converter can be divided to two time intervals :

1) $0 \leq t < DT$

This operation mode is started when switch S is turned on. Then diode D_Y is turned on and diode D_X is reversed-biased. So the capacitor C_X voltage is applied across inductor L_X and the input voltage is applied across inductor L_1. So these to inductors are charged and their current is increased linearly. Also capacitors C_1 and C_2 are charged and the diode D_o is reverse-biased. So the output capacitor C_o supplies the load current. So this set of equations can be written for this operation mode :

$$V_{L1} = V_{in}, V_{L2} = -V_C, V_{Lx} = V_{Cx} \tag{2.84}$$

$$V_{Dx} = V_{Cx}, V_{Do} = V_{out} - V_C \tag{2.85}$$

2) $DT \leq t \leq T$

This operation mode is started when active switch S is turned off. Then diode D_X is turned on and diodes D_Y, D_1 and D_2 are reversed-biased. So Capacitor C_X is charged through diodes D_X and because the inductors L_X and L_1 voltage is negative, their energy are transferred to the output. The output capacitor C_o is charged through diode D_o. As it is shown, because an inductor is located in the input of this converter, the input current is continuous and this is one of the advantages of this converter.

In this operation mode, capacitors C_1 and C_2 are discharged to the output. Therefore, this set of equations can be written for this operation mode :

$$V_{L1} = V_{in} - V_{Cx} \tag{2.86}$$

$$V_{L2} = -V_{out} - 2 \times V_C \tag{2.87}$$

$$V_{Lx} = V_{Cx} + V_C - V_{out} \tag{2.88}$$

$$V_S = V_{out} - V_C \tag{2.89}$$

$$V_{D1} = V_{D2} = V_{out} - V_C \tag{2.90}$$

so for calculating the voltage ratio expression, volts.second balance of inductors L_1, L_2 and L_X are used. Therefore :

$$Volts.second\ Balance \rightarrow L_1 \rightarrow V_{in}.DT = -(V_{in} - V_{Cx})(1-D)T \tag{2.91}$$

$$\Longrightarrow V_{in} = (1-D).V_{Cx} \tag{2.92}$$

$$Volts.second\ Balance \rightarrow L_2 \rightarrow -V_C.DT = -(V_{out} - 2V_C)(1-D)T \tag{2.93}$$

$$\Longrightarrow V_{Cx} = (1-D).V_{out} - (1-D).V_C \tag{2.94}$$

$$Volts.second\ Balance \rightarrow L_x \rightarrow V_{Cx}.DT = -(V_{out} + V_C + V_{Cx})(1-D)T \tag{2.95}$$

$$\Longrightarrow (2-D).V_C = (1-D).V_{out} \tag{2.96}$$

So based on two equations 2.94 and 2.96 :

$$\Longrightarrow V_{Cx} + (1-D).V_C = (2-D)(V_C) \tag{2.97}$$

$$\Longrightarrow V_{Cx} = V_C \tag{2.98}$$

So based on equations 2.92, 2.94 and 2.98 :

$$\Longrightarrow (1-D).V_{out} = V_{Cx} + (1-D).V_{Cx} = (2-D).V_{Cx} \tag{2.99}$$

$$\Longrightarrow V_{out} = \frac{2-D}{1-D}.V_{Cx} = \frac{2-D}{1-D}.\frac{1}{1-D}.V_{in} \tag{2.100}$$

$$\Longrightarrow M_v = \frac{V_{out}}{V_{in}} = \frac{2-D}{(1-D)^2} \tag{2.101}$$

As it is shown in the voltage gain expression, higher voltage gain than the integrated cascade boost converter can be achieved. So this is the proper method and topology for increasing voltage gain. Therefore, these switched capacitor cell and coupled inductors will be used in the next chapters for increasing z-source voltage gain [20].

2.6.2 High Step Up Converters with Four Terminal High Step Up Switch Cell

In this section, the converters are analyzed that use high step up switch cell for increasing voltage ratio. This cell includes two identical capacitors C, tow diodes D_1 and D_2 and active switch S. Figure 2.23 shows this cell topology. So it is used to increase voltage gain.

The converters that use this cell are divided two three kind of converters. Type 1, type 2 and type 3. Type 1 and type 2 converters are analyzed in this section. Type 1 converter has two different topology, however, because their operation principles are the same, just one of them is analyzed.

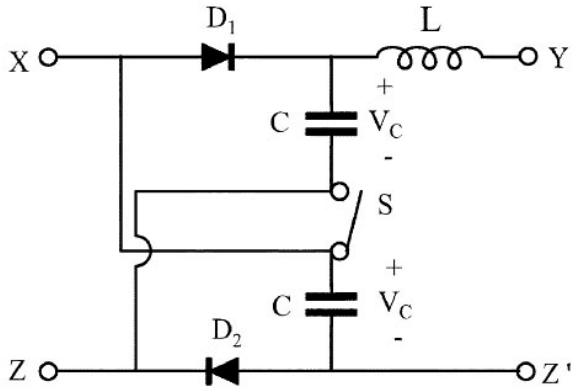

Figure 2.23: Four Terminal High Step Up Switch Cell. [19]

Some of advantage of these kind of converters are as below:

✓The higher output voltage can be achieved in comparison to conventional converters (like boost converter) with the same input voltage and less duty ratio. So if your duty cycle is to high, it means very high current goes through output diode for the short time and it results in severe reverse recovery problem for the output diode and also it causes the electromagnetic interference (EMI) problems.

✓Stress voltage of the semiconductor devices is decreased, so conduction losses can be decreased.

✓The important advantage of these kind of converters is that the input and output current is continuous. [19]

Therefore, as it is shown, two different topologies for type 1 converter can be assumed. One of them has positive output voltage and one of them negative output voltage. Figures 2.24 and 2.25 shows these converters topology. Also Figure 2.26

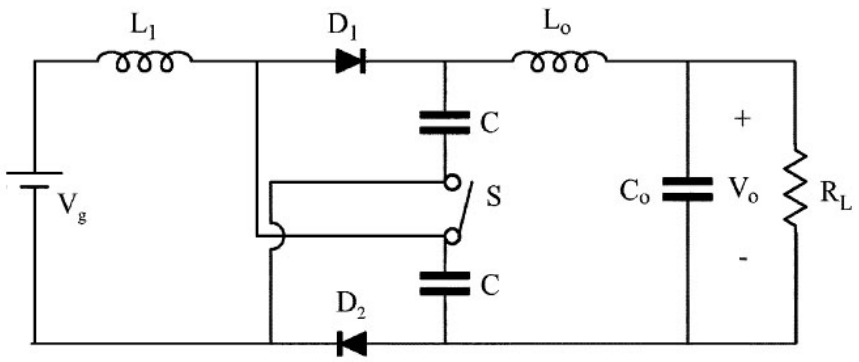

Figure 2.24: Type 1 converter with positive output voltage topology . [19]

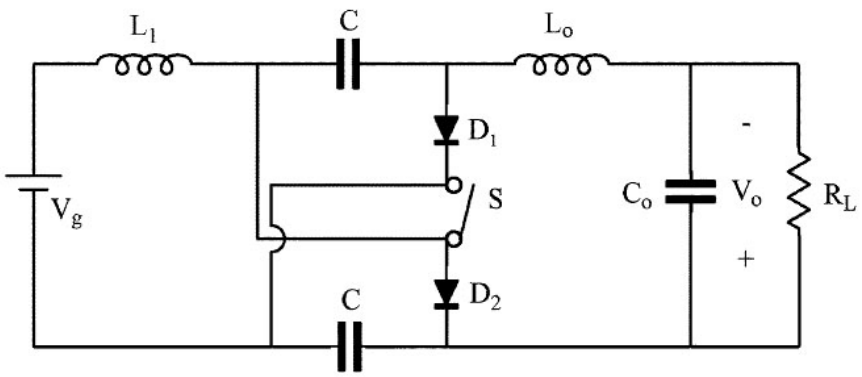

Figure 2.25: Type 1 converter with negative output voltage topology. [19]

shows the type 2 converter topology. As it was mentioned earlier, one of the main

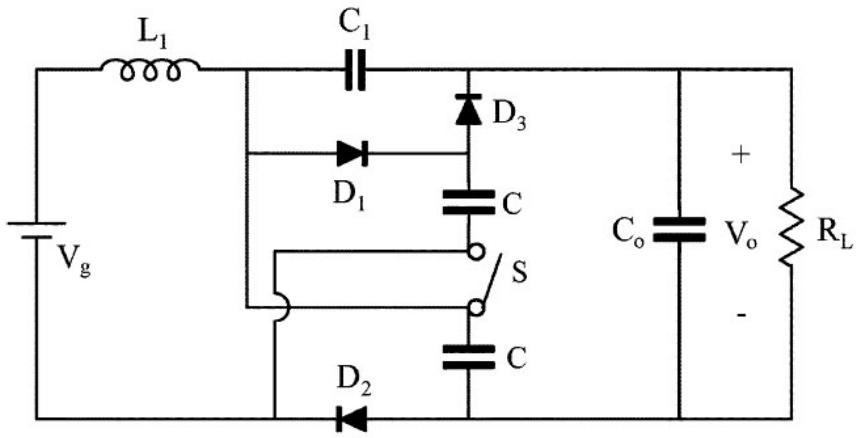

Figure 2.26: Type 2 converter topology. [19]

advantages of these kind of converters is the low stress voltage of semiconductors devices like switch and diode. So it is very proper choice for the high step up application and where we need the high voltage gain. Therefore, the conduction losses will be decreased and the efficiency of the converter will be increased [19].

Therefore, type 1 converter with negative output voltage and type 2 converter will be analyzed in next sections.

2.6.2.1 Type 1 High Step Up Converter

Figure 2.25 indicates the converter topology. As it is shown in this figure, it has the negative output voltage if we assume the input voltage is positive. Type 1 high step up converter includes a main switch S and two diodes D_1 and D_2 and two identical capacitors C. Also it has a low pass filter at the output.

Generally speaking the operation principle of this converter is that two identical capacitors C are charged in parallel when switch S is off and these two capacitors

energy is transferred two the output when switch S is on.

Therefore, with switching the main switch S, voltage pulses are created and with passing through the output low pas filter LC, the DC value is transferred to the output.

1) $0 \leq t < DT$

This operation mode is started when switch S is turned on. So the input voltage is applied across input inductor L_1 and it's current is decreased linearly. Also the output inductor L_o stores energy. Also D_1 and D_2 are reverse-biased since their voltage is negative. In this operation mode, capacitors C are being discharged. Figure 2.27 shows the equivalent circuit off this converter in the first mode of operation. So this set of equations can be written for this operation mode :

$$V_{D1} = V_{D2} = V_C \tag{2.102}$$

$$V_{L1} = V_G, V_{Lo} = 2V_C - V_o \tag{2.103}$$

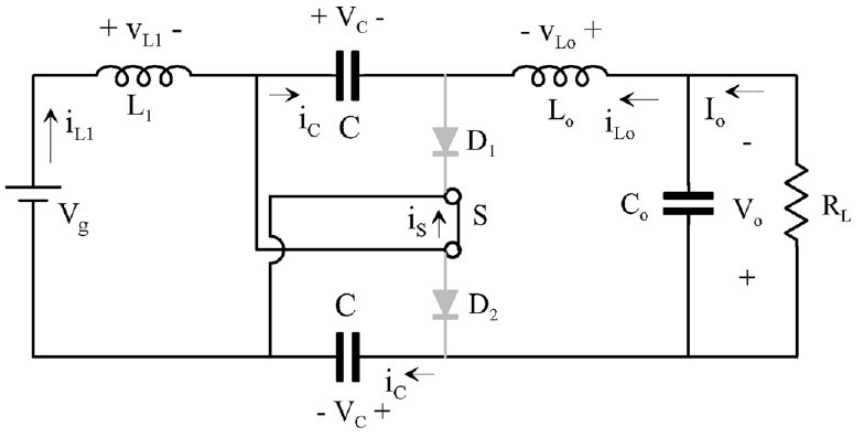

Figure 2.27: Equivalent circuit of type 1 converter(1) [19].

2) $DT \leq t \leq T$

This operation mode is started when switch S is turned off. Then, diodes D_1 and D_2 are turned on. In this operation mode identical capacitors C are charged through the input inductor L_1 and inductors L_1 and L_o are discharged, since their voltage is negative and so their current are being decreased. Figure 2.28 shows the equivalent circuit of this operation mode. So this set of equations can be written for this operation mode :

$$V_S = V_C \tag{2.104}$$

$$V_{L1} = V_G - V_C \tag{2.105}$$

$$V_{Lo} = V_C - V_o \tag{2.106}$$

This converter is analyzed for the current continuous mode(CCM), however, if it is

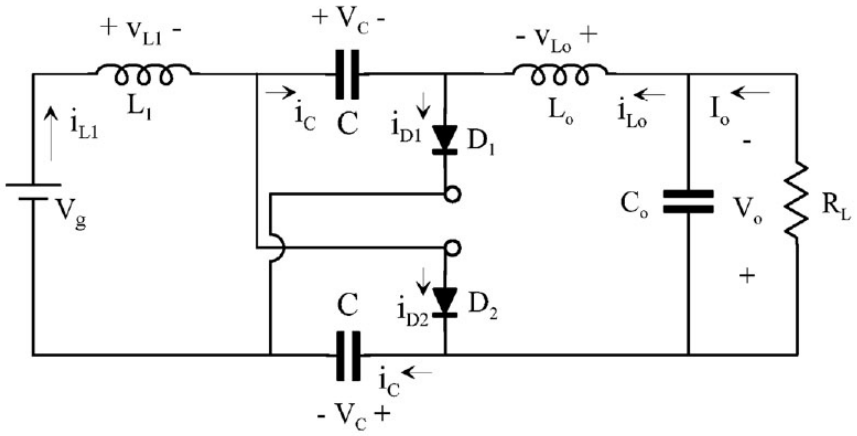

Figure 2.28: Equivalent circuit of type 1 converter (2) [19].

analyzed for discontinuous inductor current mode(DICM), one more operation mode would be added. Figure 2.29 shows the last operation mode of this converter in

DICM mode. As it is shown in this figure, both switch and diodes are off So this set of equations can be written for this operation mode. The voltage ratio of this

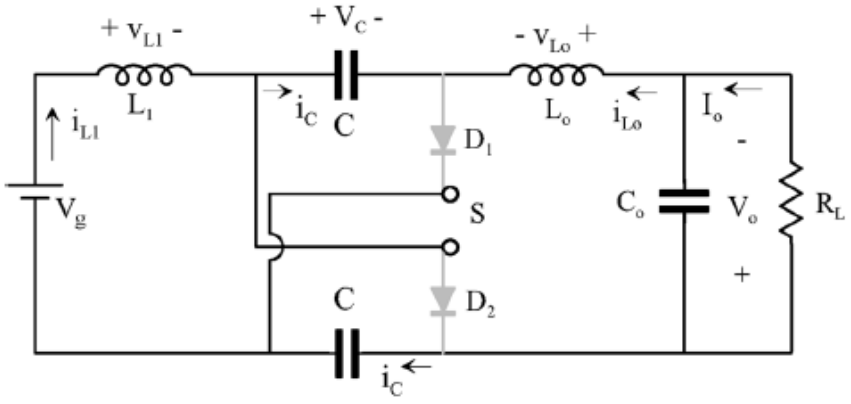

Figure 2.29: Equivalent circuit of type 1 converter (3) [19].

converter is calculated in CCM mode. So volts.second balance of inductors L_1 and L_o are used to achieve the voltage gain. Therefore :

$$Volts.second \Longrightarrow L_1 \Longrightarrow (V_g).DT = -(V_g - V_C)(1-D).T \tag{2.107}$$

$$\Longrightarrow V_g = (1-D).V_C \tag{2.108}$$

$$Volts.second \Longrightarrow L_o \Longrightarrow (2V_C - V_o).DT = -(V_C - V_o)(1-D).T \tag{2.109}$$

$$\Longrightarrow V_o = (1+D).V_C \tag{2.110}$$

So based on equations 2.108 and 2.110 we have:

$$\Longrightarrow V_o = (1+D).\frac{1}{1-D}.V_g \tag{2.111}$$

$$\Longrightarrow M_V = \frac{V_o}{V_g} = \frac{1+D}{1-D} \tag{2.112}$$

Therefore stress voltage of switch and diodes are calculated. As it is shown, the stress voltage of diodes and switch are equal to each other and therefore:

$$\Longrightarrow V_{stress} = V_C = \frac{V_o}{1+D} \tag{2.113}$$

$$\Longrightarrow M_S = \frac{V_{stress}}{V_o} = \frac{1}{1+D} = \frac{1+M_v}{2M_v} \tag{2.114}$$

So as it is shown in equation 2.114, switch and diodes stress voltage is normalized based on the output voltage. So as it is indicated in this equation, as the voltage ratio (M_v) of this converter is increased, the stress voltage of the semiconductor devices will be decreased and this the important advantage of this converter [19]. Figure 2.31 indicates the key waveforms of the type 1 high step up converter with the negative voltage and figure 2.30 shows the current waveforms of the DICM mode.

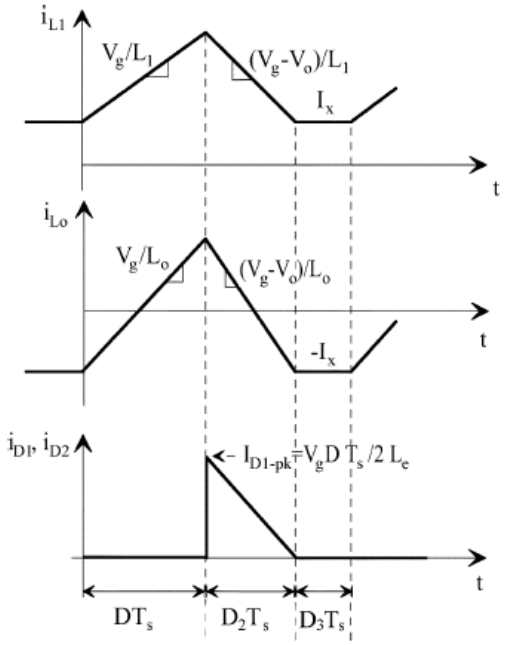

Figure 2.30: Current waveforms of the type 1 high step up converter in DICM mode. [19]

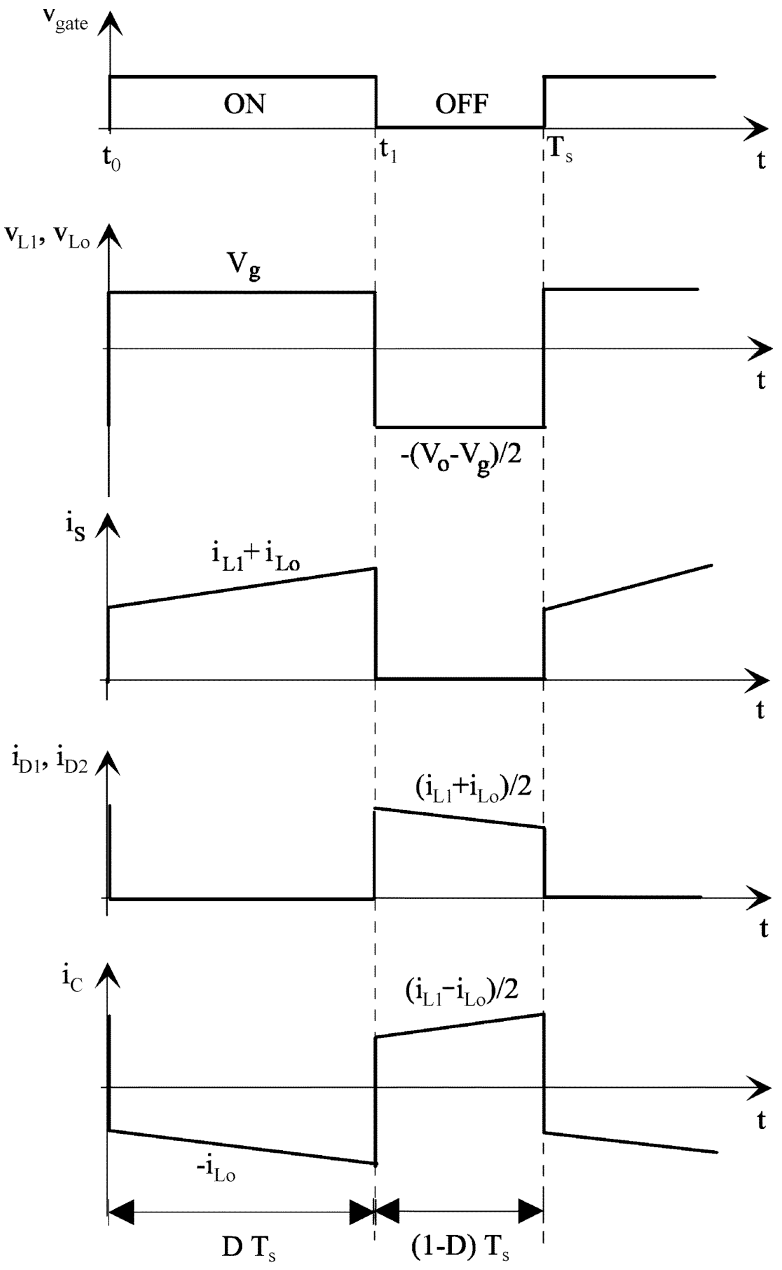

Figure 2.31: Important waveforms of the type 1 high step up converter. [19]

2.6.2.2 Type 2 High Step Up Converter

Figure 2.26 indicates the topology for this converter. As it is shown in this figure, this converter includes the main switch S and three diodes(D_1, D_2 and D_3). The

operation principle of that is very similar to the type 1 converter, however, just a capacitor is added to the main loop. That causes the gain to be higher in comparison to the type 1 converter. So the operation principle of this converter is analyzed in CCM mode. Also the equivalent circuit of operating in DICM(discontinuous inductor current mode) is provided. So it includes a main switch S, hence the operation principle of this is divided to two time intervals.

1) $0 \leq t < DT$

This operation mode is started when active switch S is turned on. Then diodes D_1 and D_2 are reversed-biased because their voltage is negative. When switch S is on, input voltage is applied across inductor L_1 and this inductor is being charged and it's current is increased linearly. Also capacitors C_2 and C_3 are discharged in series. But the capacitor C_1 is charged in this operation mode and it's current is increased linearly. Figure 2.32 shows the equivalent circuit of this mode.

So in this operation mode the capacitors C_2 and C_3 energy is transferred to the output. This set of equations can be written for this operation mode :

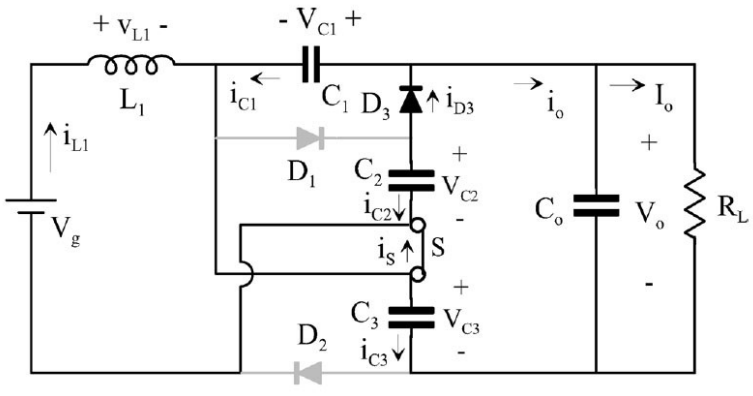

Figure 2.32: Equivalent circuit of type 2 converter (1) [19].

$$V_{C1} = V_{C2} = V_{C3} := V_C \tag{2.115}$$

$$\Longrightarrow V_{C2} = V_{D1} = V_C \tag{2.116}$$

$$\Longrightarrow V_{C3} = V_{D2} = V_C \tag{2.117}$$

$$V_{L1} = V_g \tag{2.118}$$

2) $DT \leq t \leq T$

This operation mode is started when switch S is turned off. Then diodes D_1 and D_2 are turned on but diode D_3 is reverse-biased. Inductor L_1 voltage is negative in this operation mode so it's current is decreased linearly. Capacitors C_2 and C_3 are charged in this operation mode but capacitor C_1 is discharged. So the energy also is transferred to the output in this operation mode.

Figure 2.33 shows the equivalent circuit of the type 2 converter in the second mode of operation. This set of equations can be written in this operation mode :

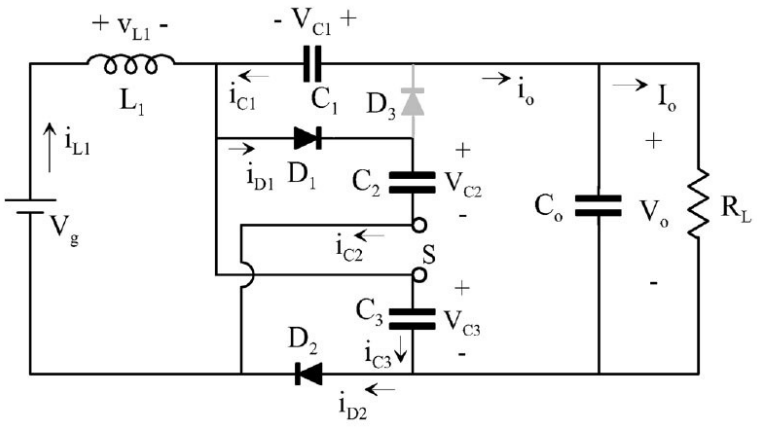

Figure 2.33: Equivalent circuit of type 2 converter (2) [19].

$$V_{C1} = V_{D2} = V_C \tag{2.119}$$

$$V_{C2} = V_{C1} = V_C = V_S \tag{2.120}$$

$$V_{L1} = V_g - V_C \tag{2.121}$$

So based on the previous equations, the difference between the semiconductor devices stress voltage of the type 1 and type 2 converter can be seen. Therefore, this converter is also analyzed in DICM(discontinuous inductor current mode). One more operation mode will be added. Figure 2.34 shows the equivalent circuit of this mode. As it is shown all the semiconductor devices are off in this operation mode and the inductor L_1 current reaches zero.

Figure 2.35 indicates the important waveforms of the type 2 high step up converter.

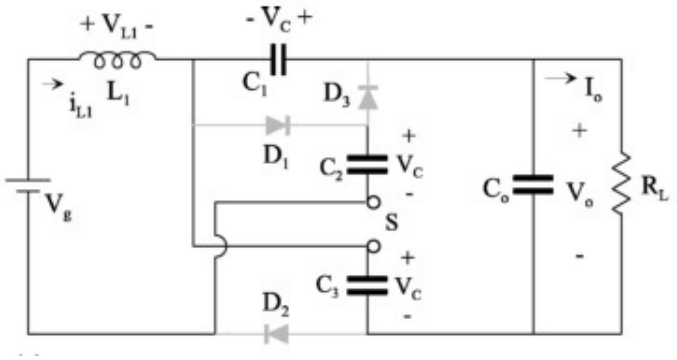

Figure 2.34: Equivalent circuit of type 2 converter in the DICM. [19]

Volts.second balance of the inductor L_1 and a KVL when switch S is on, are used for calculating the voltage ratio. Therefore :

$$Volts.second \Longrightarrow L_1 \Longrightarrow V_g.DT = -(V_g - V_C)(1 - D).T \tag{2.122}$$

$$\Longrightarrow V_g = (1 - D).V_C \tag{2.123}$$

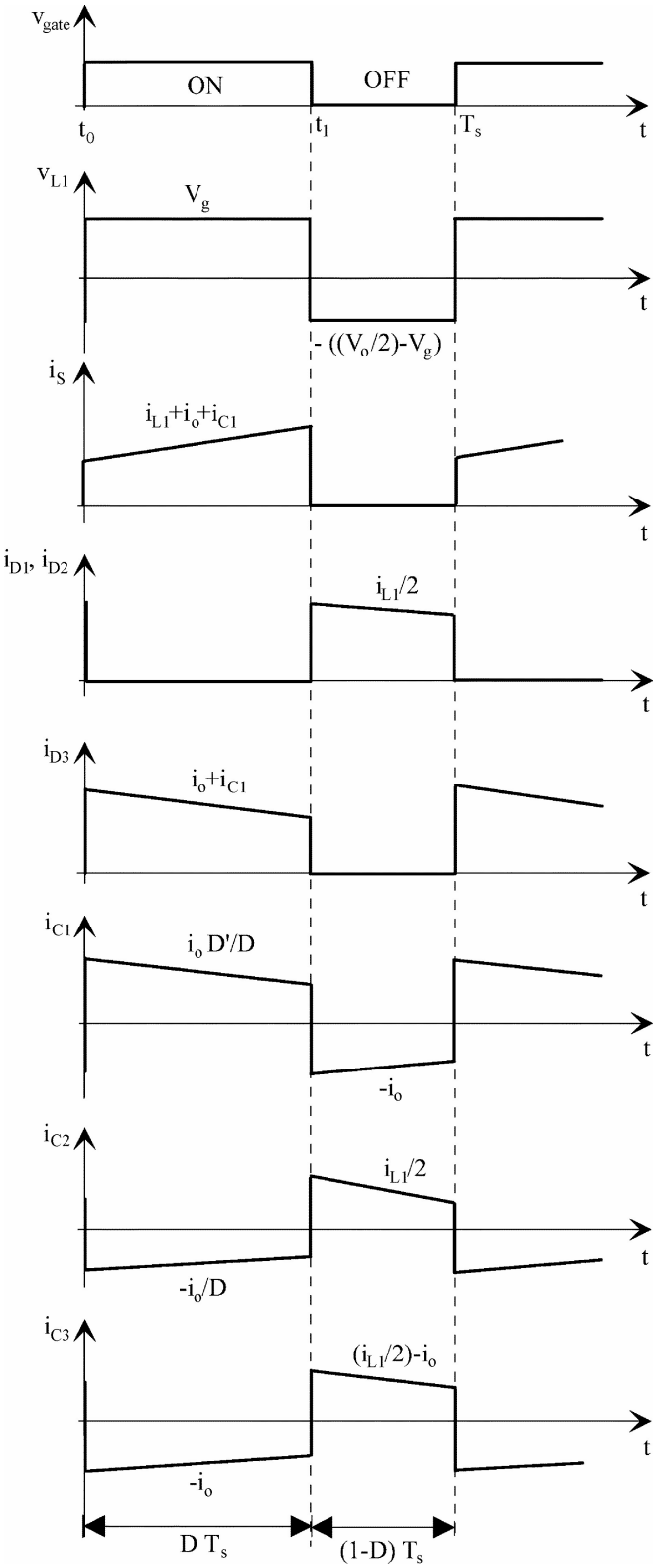

Figure 2.35: Key waveforms of type 2 converter in CCM. [19]

$$KVL \Longrightarrow S = on \Longrightarrow V_o = V_{C2} + V_{C3} = 2V_C \tag{2.124}$$

$$\Longrightarrow V_o = 2 \times \frac{1}{1-D}.V_g \tag{2.125}$$

$$\Rightarrow M_v = \frac{V_o}{V_g} = \frac{2}{1-D} \tag{2.126}$$

Also the semiconductor devices stress voltage can be calculated :

$$\Longrightarrow V_{stress} = V_C = \frac{V_o}{2} \tag{2.127}$$

$$\Longrightarrow M_S = \frac{V_{stress}}{V_o} = \frac{1}{2} \tag{2.128}$$

Therefore, the voltage gain of the type 2 converter is more than type one converter and it is two times than the conventional boost converter and also the stress voltage of the semiconductor devices in the type 2 converter is less than type one converter and it is half of the semiconductor devices stress voltage in the conventional boost converter. So generally speaking, therefore this is the proper method to increase voltage gain for the high step up converters.

3. HIGH STEP-UP Z-SOURCE DC-DC CONVERTER WITH FLYBACK AND VOLTAGE MULTIPLIER

In this chapter a novel high step-up converter is proposed. It is formed by combining the z-source converter with the methods that was explained in chapter two. Actually for increasing the voltage gain, the combination of the fly-back and z-source converter with coupled inductors and voltage multiplier is used. In other words the method that was described in the section 2.4.3 is used to form this converter.

In this chapter the proposed converter topology is indicated, then the operation principle of this converter will be explained and the it's operation modes will be analyzed, moreover, the voltage ratio expression and other important expressions are derived. Furthermore, the key waveform of this converter are indicated and the theoretically comments and expressions are confirmed with the simulation results. Finally, the proposed converter is experimentally tested. The experiment results verified the theoretical and simulation results.

3.1 Introduction

Figure 3.1 shows the proposed converter topology. As it is shown in this figure, this converter is formed by combining the z-source converter with the fly-back converter and voltage multiplier method. So two coupled inductors are used instead of the z-source network inductors. Also the voltage multipliers are used in the output to increase the voltage gain.

In the proposed converter, the voltage pulses across the coupled inductors are used to increase the output voltage of the converter and therefore to increase the voltage ratio. So these pulses charge the output capacitors $C_{o2} - C_{o5}$ through diodes

$D_{o2} - D_{o5}$ and it causes to increase the output voltage since these capacitors are settled in series at the output.

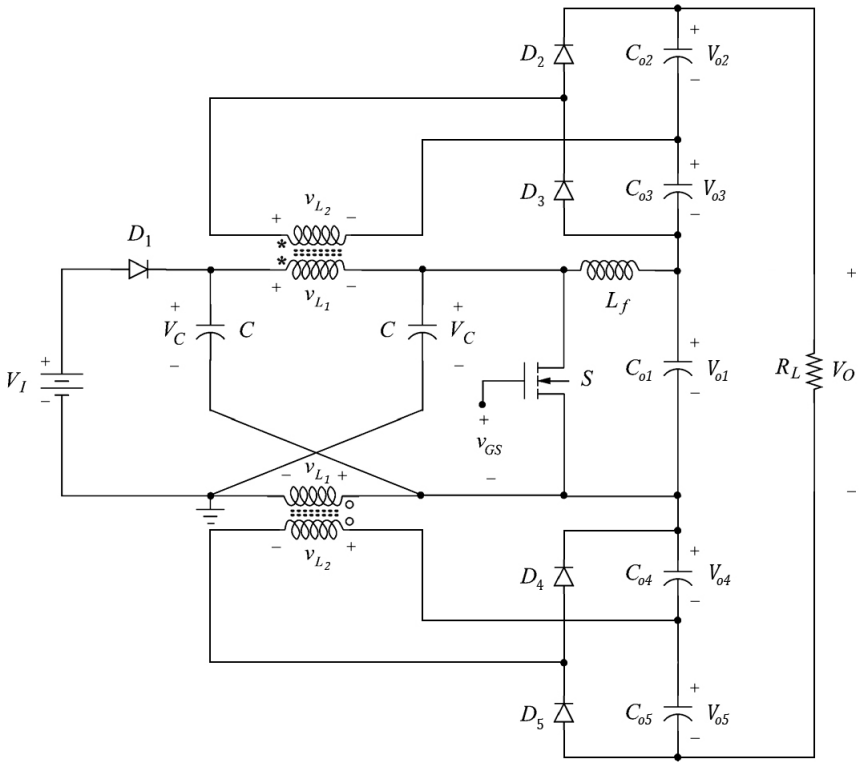

Figure 3.1: Proposed Converter Topology

3.2 Operation Principle of the Proposed Converter

Operation principle of the z-source part of the proposed converter is similar to the operation principle of the z-source converter that was explained in the chapter one. So it is focused on the parts that have been added to form the proposed converter. Since it includes one main switch, the operation principle of this converter is divided to two time intervals. One of them for the switch on time and the other one for the switch off time. First, the operation principle of the proposed converter is analyzed

for the time that switch is on, then switch off time. Capital letter D indicates duty cycle of the main switch S.

1) $0 \leq t < DT$

This operation mode is started when active switch S is turned on. Then the input diode D_1 is turned off. So the main active switch S and the input diode of the proposed converter operate in the complementary manner. Then, the capacitors C voltage is applied across the inductors L_1 and since this voltage is positive and constant, inductors L_1 current are increased linearly and with a constant slope.

The turn ratio of the couple inductors L_1 and L_2 is defined as $n := \frac{n_2}{n_1}$. therefore, n times of the voltage across inductors L_1 is applied across inductors L_2. This causes the D_2 and D_5 to be turned on. So the capacitors C_{o2} and C_{o5} are charged in this time interval. When the diodes D_2 and D_5 are turned on, the negative voltage is applied across diodes D_3 and D_4 and make these diodes to be turned off. Since the filter inductor L_f voltage is negative in this operation mode, the inductor current is decreased linearly and it's energy is lost.

Figure 3.2 shows the proposed converter equivalent circuit in the first operation mode when the active switch S is on. These sets of equations can be written for this operation mode :

$$V_{L1} = V_C, V_{L2} = n.V_C \tag{3.1}$$

$$V_{Lf} = -V_{o1} \tag{3.2}$$

$$V_{o2} = V_{L2} = n.V_C \tag{3.3}$$

$$V_{o5} = V_{L2} = n.V_C \tag{3.4}$$

$$V_{D1} = 2V_C - V_I \tag{3.5}$$

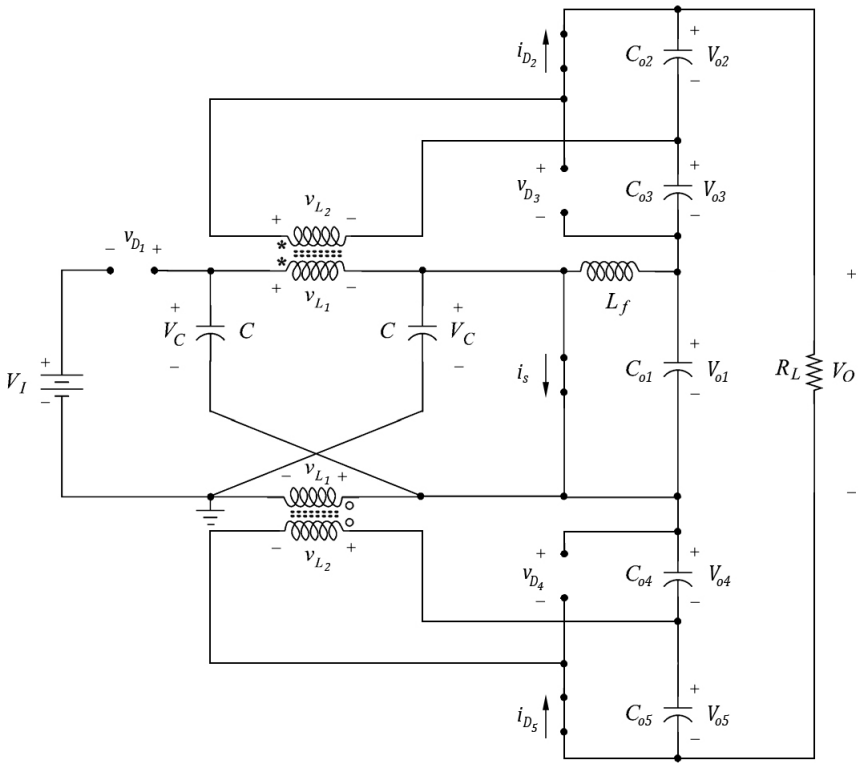

Figure 3.2: The equivalent circuit of the proposed converter when the switch S is on

$$V_{D3} = V_{o2} + V_{o3} \tag{3.6}$$

$$V_{D4} = V_{o4} + V_{o5} \tag{3.7}$$

$$\tag{3.8}$$

2) $DT \leq t \leq T$

This operation mode is started when the active switch S is turned off. Then the voltage across it keep increasing till the input diode D_1 is turned on. So the voltage across the switch(the switch stress voltage) is clamped. As it is mentioned earlier, the input diode D_1 and switch S operate in complementary manner. Since the input diode D_1 is on, the input source supplies energy, therefore the power is supplied to

the converter in this operation mode. Also since the proposed converter has a input diode, the input current of this converter is not continuous.

In this operation mode, the voltage across inductors L_1 is negative, so this negative voltage is induced across inductors L_2 and then diodes D_3 and D_4 are turned on. Therefore, capacitors C_{o3} and C_{o4} are charged in this operation mode. The

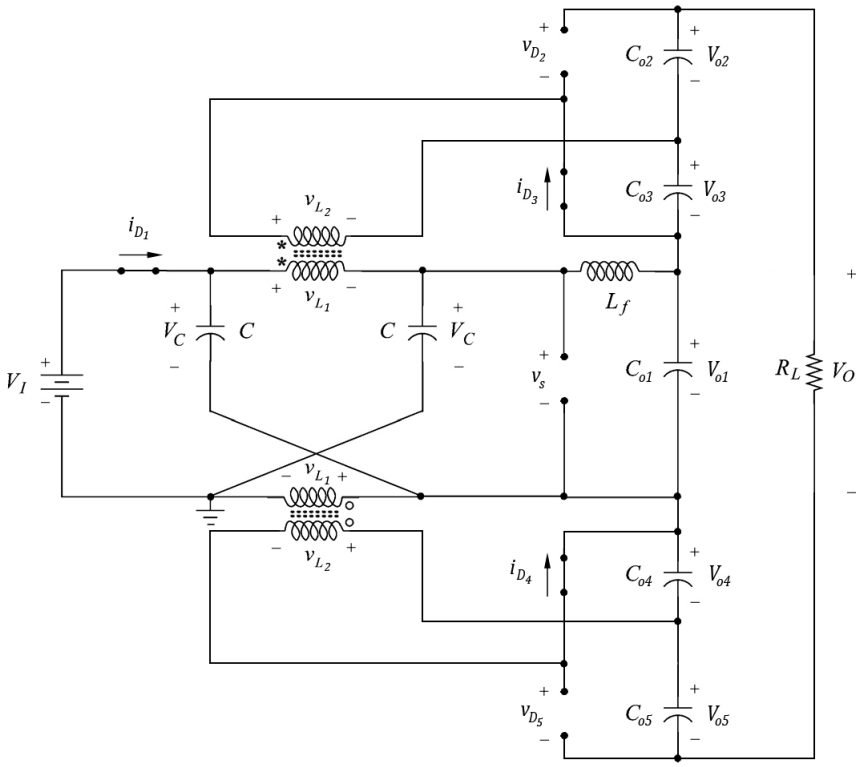

Figure 3.3: The equivalent circuit of the proposed converter when the switch S is off

voltage across diodes D_1 and D_5 is negative, so they are off in this operation mode. Furthermore capacitors C and the filter inductor L_f are charged in this mode. These

sets of equations can be written for this operation mode :

$$V_{L1} = V_I - V_C \tag{3.9}$$

$$V_{L2} = n.(V_I - V_C) \tag{3.10}$$

$$V_{o3} = -V_{L2} = n.(V_C - V_I) \tag{3.11}$$

$$V_{o4} = -V_{L2} = n.(V_C - V_I) \tag{3.12}$$

$$V_S = 2V_C - V_I \tag{3.13}$$

$$V_{D2} = V_{o2} + V_{o3} \tag{3.14}$$

$$V_{D5} = V_{o4} + V_{o5} \tag{3.15}$$

$$V_{Lf} = 2V_C - V_I - V_{o1} \tag{3.16}$$

Also the stress voltage of the semiconductor devices is demonstrated by these equations. As it is shown, the main switch stress voltage is decreased as the input voltage is increased and it is one of the advantages of this converter.

3.3 Voltage Ratio Expression

Volts.second balance for the inductors L and L_f is used to find the voltage gain. Based on volts.second balance theory :

$$\int_0^T V_L(t)dt = 0 \tag{3.17}$$

$$\int_0^{DT} V_L(t)dt = -\int_{DT}^T V_L(t)dt \tag{3.18}$$

Therefore, these equations can be written for both inductors L_1 and L_f. Then :

$$Volts.second \Longrightarrow L \Longrightarrow V_C.DT = -(V_I - V_C)(1-D).T \tag{3.19}$$

$$\Longrightarrow (1-D).V_I = (1-2D).V_C \tag{3.20}$$

$$\Longrightarrow V_C = \frac{1-D}{1-2D}.V_I \tag{3.21}$$

$$Volts.second \Longrightarrow L_f \Longrightarrow -V_{o1}.DT = -(2V_C - V_I - V_{o1})(1-D).T \tag{3.22}$$

$$\Longrightarrow 2(1-D).V_C = (1-D).V_I + V_{o1} \tag{3.23}$$

So based on equations 3.21 and 3.23 we have :

$$V_{o1} = \frac{1-D}{1-2D}.V_I \tag{3.24}$$

Based on two equations 3.21 and 3.24, it is proved that :

$$V_{o1} = V_C \tag{3.25}$$

Now output voltages expression that we calculated for switch on time and off time in previous section, are used to calculate the voltage gain. Therefore :

$$V_{o2} = V_{o5} = n.V_C \tag{3.26}$$

$$V_{o3} = V_{o4} = n.(V_C - V_I) \tag{3.27}$$

$$V_o = V_{o1} + V_{o2} + V_{o3} + V_{o4} + V_{o5} \tag{3.28}$$

$$\Rightarrow V_o = V_{o1} + 2V_{o2} + 2V_{o3} \tag{3.29}$$

$$\Rightarrow V_o = \frac{1-D}{1-2D}.V_I + 2n.\frac{1-D}{1-2D}.V_I + 2n.(\frac{1-D}{1-2D}.V_I - V_I) \tag{3.30}$$

$$\Rightarrow V_o = \frac{1-D}{1-2D}.V_I + 4n.\frac{1-D}{1-2D}.V_I - 2n.V_I \tag{3.31}$$

$$\Rightarrow M_v = \frac{V_o}{V_I} = \frac{(2n+1) - D}{1 - 2D} \tag{3.32}$$

So it is shown that our voltage ratio is increased in comparison to z-source converter. For the z-source converter . Voltage ratio expression of z-source converter wa equal to $M_v = \frac{1-D}{1-2D}$, so for $D = 0.4$ and $n = 1$, voltage gain of (3) can be achieved for z-source converter, however, voltage gain of (13) can be achieved for the proposed converter.

So with having control over the turn ratio of the coupled inductors, the desired gain can be achieved.

Following equations can be written for thr lossless converter :

$$P_I = P_O \Longrightarrow V_I I_I = V_o I_o \Rightarrow M_I = \frac{I_o}{I_I} = \frac{1 - 2D}{(2n+1) - D} \tag{3.33}$$

It should be considered that with increasing the turn ratio n, the primary side of the coupled inductors current will be increased since $n = \frac{i_{L1}}{i_{L2}}$. It causes the semiconductors specially input diode and the main switch current to be increased, so their turn on voltage is increased. So the voltage ratio is decreased and the efficiency is decreased since the semiconductor devices losses are increased. So based on this fact, turn ratio of the coupled inductors should be optimized.

Semiconductor devices stress voltage can be calculated when thay are off. Base on equations 3.24 and 3.25 :

$$V_S = V_D = 2V_C - V_I \tag{3.34}$$

$$V_S = V_D = 2 \times V_{o1} - V_I = 2 \times \frac{1-D}{1-2D}.V_I - V_I \tag{3.35}$$

$$\Longrightarrow V_S = V_D = \frac{1}{1-2D}.V_I \tag{3.36}$$

Based on equation 4.29, the ratio of main switch and input diode stress voltage over the output voltage can be calculated :

$$M_S = \frac{V_{stress}}{V_o} = \frac{1}{(2n+1)-D} \tag{3.37}$$

Therefore, if $n = 1$, it can be written in this way :

$$M_S = \frac{V_{stress}}{V_o} = \frac{1}{3-D} \tag{3.38}$$

This ratio is equal to 0.38 for $D = 0.4$. It means, the main switch and input diode stress voltage is much lower than the output voltage. This ratio was 1 for boost converter.

Lower stress voltage leads to less switch conduction resistance and finally less conduction loss for semiconductor devices.

Other diodes stress voltage can be calculated by following equations. Based on equations 3.7, 3.15, 3.27, 3.28, 3.35 and 3.36 :

$$V_{D_2} = V_{D_3} = V_{o_2} + V_{o_3} \tag{3.39}$$

$$V_{D_2} = V_{D_3} = n.(2V_C - V_I) = n.\frac{1}{1-2D}.V_I = n.V_S = n.V_{D_1} \tag{3.40}$$

And based on equations 3.8, 3.16, 3.27 and 3.28 :

$$V_{D_4} = V_{D_5} = V_{o_4} + V_{o_5} \tag{3.41}$$

$$V_{D_4} = V_{D_5} = n.(2V_C - V_I) = n.\frac{1}{1-2D}.V_I = n.V_S = n.V_{D_1} \tag{3.42}$$

3.4 Non-ideal Elements Analysis of the Proposed Converter

In this section, the effect of non-ideal elements in on the proposed converter is analyzed. Efficiency and non-ideal voltage gain expression are studied and calculated.

The equivalent circuit of the proposed converter with non-ideal elements are shown in figure 3.4. As it is shown in this figure, the equivalent series resistor (ESR) of the capacitors, forward voltage drop of the diodes, on-resistance of the main switch and winding resistance of the coupled inductors are depicted.

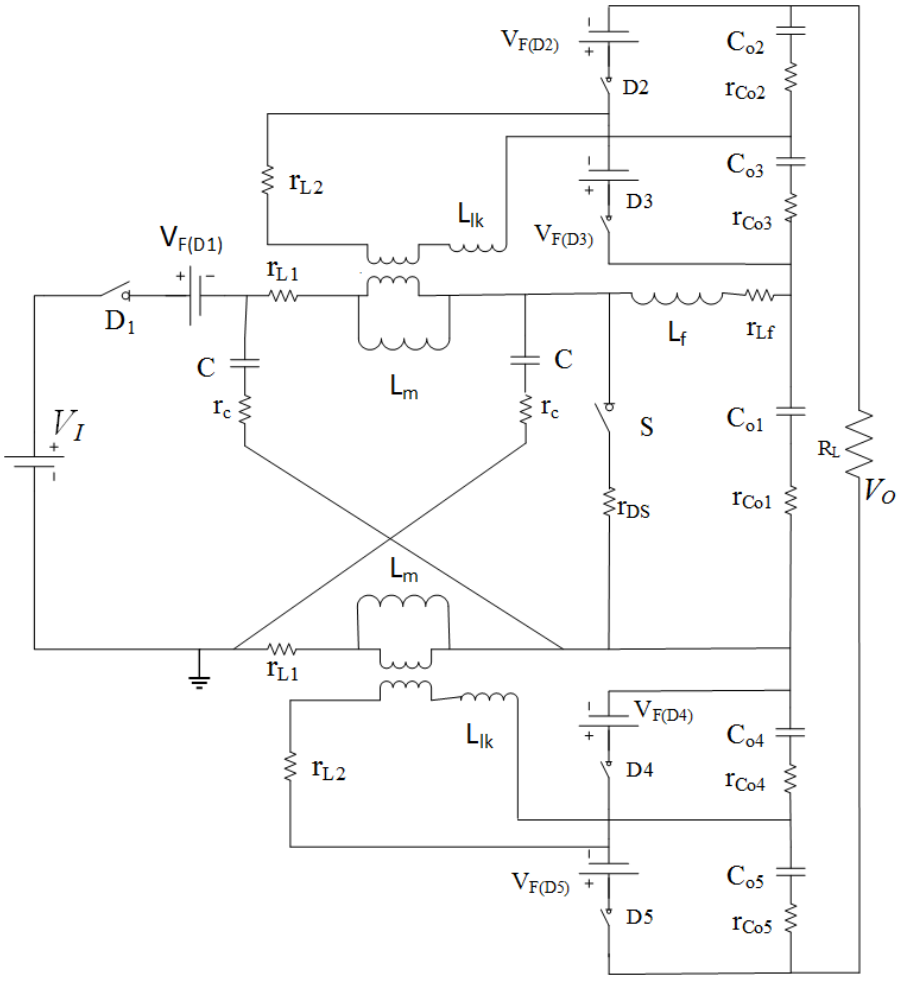

Figure 3.4: The equivalent circuit of the proposed converter with all non-ideal elements

3.4.1 Efficiency and Power Losses

To calculate the efficiency, the power losses including parasitic resistances and the conduction losses of the semiconductor devices are studied and analyzed.

The conduction loss of the main switch S depends on the on-resistance of the switch and root-square-mean (rms) value of the switch current. The switch current can be approximated by :

$$i_S = \begin{cases} 2I_L - I_o = 2I_I - I_o, & \text{if } 0 < t \leq DT \\ 0, & \text{if } DT < t \leq T \end{cases} \tag{3.43}$$

Using 3.33 and 3.43, the (rms) value of switch current is :

$$\begin{aligned} I_{s(rms)} = \sqrt{\frac{1}{T}\int_0^T i_S^2 dt} = \frac{(4n+1)I_o}{1-2D}\sqrt{\frac{1}{T}\int_0^{DT} dt} \\ = \frac{(4n+1)I_o}{1-2D}\sqrt{D} \end{aligned} \tag{3.44}$$

Therefore, the conduction loss in the MOSFET is :

$$\begin{aligned} P_{r_{DS}} = r_{DS} I_{s(rms)}^2 = \frac{(4n+1)^2 I_o^2 D r_{DS}}{(1-2D)^2} \\ = \frac{(4n+1)^2 D r_{DS} P_o}{(1-2D)^2 R_L} \end{aligned} \tag{3.45}$$

Where r_{DS} is the switch on-resistance, P_o is the output power and R_L is the load resistance. Assuming the switch output capacitance C_o is linear and using 3.24, 3.32 and 3.33, the MOSFET switching loss is expressed as :

$$P_{sw} = \frac{f_s C_o V_{o1}^2}{2} = \frac{f_s C_o (1-D)^2 V_o^2}{2(1-2D)^2 M_v^2} \tag{3.46}$$

$$= \frac{f_s C_o (1-D)^2 P_o R_L}{2(1-2D)^2 M_v^2}$$
$$= \frac{f_s C_o (1-D)^2 P_o R_L}{2((2n+1)-D)^2}$$

Therefore, using 3.46 and 3.47, the total power loss in the main switch is :

$$P_{FET} = P_{r_{DS}} + P_{sw} = (\frac{(4n+1)^2 D r_{DS}}{(1-2D)^2 R_L} + \frac{f_s C_o (1-D)^2 R_L}{2((2n+1)-D)^2}) P_o \tag{3.47}$$

Also conduction losses of the diodes depend on their forward voltage drop and the average current passing through them. The input diode D_1 current may be approximated by :

$$i_{D_1} = \begin{cases} 0, & \text{if } 0 < t \leq DT \\ I_I, & \text{if } DT < t \leq T \end{cases} \tag{3.48}$$

Therefore, using 3.33, the average value of input diode D_1 current is :

$$I_{D_1} = \frac{1}{T}\int_0^T i_{D1} dt = I_I(1-D) \tag{3.49}$$
$$= \frac{((2n+1)-D)(1-D)I_o}{1-2D}$$
$$= M_v(1-D)I_o$$

Therefore, the power loss associated with input diode drop of voltage V_F is :

$$P_{D1} = V_F I_{D1} = V_F M_v (1-D) I_o \tag{3.50}$$
$$= \frac{V_F M_v (1-D) P_o}{V_o}$$

The current through diode D_2 may be approximated by :

$$i_{D_2} = \begin{cases} I_o, & \text{if } 0 < t \leq DT \\ 0, & \text{if } DT < t \leq T \end{cases} \tag{3.51}$$

Therefore, the average value of diode D_2 current is :

$$I_{D_2} = \frac{1}{T}\int_0^{DT} i_{D2}dt = I_o D \tag{3.52}$$

Therefore, the power loss associated with diode D_2 drop of voltage V_F is :

$$P_{D2} = V_F I_{D2} = V_F D I_o = \frac{V_F D P_o}{V_o} \tag{3.53}$$

Similarly, the diode D_5 power loss can be calculated. Since it's average current is the same as diode D_2, their power loss is equal to each other. Therefore :

$$P_{D5} = P_{D2} = V_F D I_o = \frac{V_F D P_o}{V_o} \tag{3.54}$$

The current through diode D_3 may be approximated by :

$$i_{D_3} = \begin{cases} 0, & \text{if } 0 < t \leq DT \\ \dfrac{-I_L}{n} = \dfrac{-I_I}{n}, & \text{if } DT < t \leq T \end{cases} \tag{3.55}$$

Therefore, using 3.33, the average value of diode D_3 current is :

$$I_{D_3} = \frac{1}{T}\int_{DT}^{TT} i_{D3}dt = \frac{-M_v(1-D)I_o}{n} \tag{3.56}$$

Therefore, the power loss associated with diode D_3 drop of voltage V_F is :

$$P_{D3} = V_F I_{D3} = \frac{V_F M_v (1-D) I_o}{n} = \frac{V_F M_v (1-D) P_o}{n V_o} \tag{3.57}$$

Similarly, the diode D_4 power loss can be calculated. Since it's average current is the same as diode D_3, their power loss is equal to each other. Therefore :

$$P_{D4} = P_{D3} = \frac{V_F M_v (1-D) I_o}{n} = \frac{V_F M_v (1-D) P_o}{n V_o} \tag{3.58}$$

Power loss in inductors can be divided to core loss and winding(conduction) loss. Core losses are negligible for PWM converters and can be ignored. Conduction loss is based on (rms) value of Inductors current and their parasitic resistances. Since the coupled inductors secondary and filter current are small, their power loss can be ignored to simplify the equations, Therefore, the current flowing through inductors L_1 can be approximated by :

$$i_{L_1} = \begin{cases} nI_o, & \text{if } 0 < t \leq DT \\ I_I, & \text{if } DT < t \leq T \end{cases} \tag{3.59}$$

Therefore, using 3.33 and 3.32, the (rms) value of inductors L_1 current is :

$$\begin{aligned} I_{L_1(rms)} &= \sqrt{\frac{1}{T}\left(\int_0^{DT} n^2 I_o^2 dt + \int_{DT}^{T} I_I^2 dt\right)} \\ &= I_o \sqrt{n^2 D + M_v^2 (1-D)} \end{aligned} \tag{3.60}$$

So using 3.61, the conduction loss in resistors r_{L1} is given by :

$$P_{r_{L1}} = 2 r_{L1} I_{L_1(rms)}^2 = 2 r_{L1} (n^2 D + M_v^2 (1-D)) I_o^2 \tag{3.61}$$

$$= 2r_{L1}(n^2D + M_v^2(1-D))\frac{P_o}{R_L}$$

It should be noted that the inductors conduction losses multiplied by two, since there are two resistance r_{L1}. Similarly, capacitors resistance conduction losses can be calculated. Since the output capacitors (rms) currents are small, their power losses can be ignored. Therefore, the current flowing through capacitors C can be approximated by :

$$i_C = \begin{cases} nI_o, & \text{if } 0 < t \leq DT \\ I_I - nI_o, & \text{if } DT < t \leq T \end{cases} \tag{3.62}$$

Therefore, using 3.33 and 3.32, the (rms) value of capacitors C current is :

$$\begin{aligned} I_{C(rms)} &= \sqrt{\frac{1}{T}(\int_0^{DT} n^2 I_o^2 dt + \int_{DT}^{T} (M_v - n)^2 I_o^2 dt)} \\ &= I_o\sqrt{n^2D + (M_v - n)^2(1-D)} \end{aligned} \tag{3.63}$$

So using 3.61, the conduction loss in resistors r_c is given by :

$$\begin{aligned} P_{r_c} = 2r_c I_{C(rms)}^2 &= 2r_c(n^2D + (M_v - n)^2(1-D))I_o^2 \\ &= 2r_c(n^2D + (M_v - n)^2(1-D))\frac{P_o}{R_L} \end{aligned} \tag{3.64}$$

Therefore the total power loss of the proposed converter is given by :

$$\begin{aligned} P_{loss} &= P_{r_{DS}} + P_{sw} + P_{D1} + 2P_{D2} + 2P_{D3} + P_{r_{L1}} + P_{r_C} \\ &= \frac{(4n+1)^2 I_o^2 D r_{DS}}{(1-2D)^2} + \frac{f_s C_o (1-D)^2 V_o^2}{2(1-2D)^2 M_v^2} \\ &+ V_F M_v (1-D) I_o + 2V_F D I_o + \frac{2V_F M_v (1-D) I_o}{n} \\ &+ 2r_{L1}(n^2D + M_v^2(1-D))I_o^2 + 2r_c(n^2D + (M_v - n)^2(1-D))I_o^2 \end{aligned} \tag{3.65}$$

$$
\begin{aligned}
&= (\frac{(4n+1)^2 D r_{DS}}{(1-2D)^2 R_L} + \frac{f_s C_o (1-D)^2 R_L}{2((2n+1)-D)^2} \\
&+ \frac{V_F M_v (1-D)}{V_o} + \frac{2V_F D}{V_o} + \frac{2V_F M_v (1-D)}{nV_o} \\
&+ \frac{2r_{L1}}{R_L}(n^2 D + M_v^2 (1-D)) + \frac{2r_c}{R_L}(n^2 D + (M_v - n)^2 (1-D)) P_o \\
&= (\frac{(4n+1)^2 D r_{DS}}{(1-2D)^2 R_L} + \frac{f_s C_o (1-D)^2 R_L}{2((2n+1)-D)^2} \\
&+ \frac{(n+2) V_F M_v (1-D) + 2nV_F D}{nV_o} \\
&+ \frac{2r_{L1}}{R_L}(n^2 D + M_v^2 (1-D)) + \frac{2r_c}{R_L}(n^2 D + (M_v - n)^2 (1-D)) P_o
\end{aligned}
$$

Therefore, the proposed converter efficiency is :

$$\eta = \frac{P_o}{P_o + P_{loss}} = \frac{1}{1 + \frac{P_{loss}}{P_o}} \tag{3.66}$$

$$\gamma := \frac{P_{loss}}{P_o} \Rightarrow \eta = \frac{1}{1+\gamma} \tag{3.67}$$

$$
\begin{aligned}
\Longrightarrow \gamma &= \frac{(4n+1)^2 D r_{DS}}{(1-2D)^2 R_L} + \frac{f_s C_o (1-D)^2 R_L}{2((2n+1)-D)^2} \\
&+ \frac{(n+2) V_F M_v (1-D) + 2nV_F D}{nV_o} \\
&+ \frac{2r_{L1}}{R_L}(n^2 D + M_v^2 (1-D)) + \frac{2r_c}{R_L}(n^2 D + (M_v - n)^2 (1-D))
\end{aligned}
$$

There is a relationship between the load resistance and output power, also between input and output voltage as :

$$P_o = \frac{V_o^2}{R_L} \tag{3.68}$$

$$V_o = M_v V_I \tag{3.69}$$

$$\Longrightarrow R = \frac{V_o^2}{P_o} = \frac{M^2 V_I^2}{P_o} \tag{3.70}$$

Therefore, proposed converter efficiency can be written based on input voltage and output power as :

$$\eta = \frac{P_o}{P_o + P_{loss}} = \frac{1}{1 + \frac{P_{loss}}{P_o}} \tag{3.71}$$

$$\gamma := \frac{P_{loss}}{P_o} \Rightarrow \eta = \frac{1}{1+\gamma} \tag{3.72}$$

$$\begin{aligned} \Longrightarrow \gamma = & \frac{(4n+1)^2 D r_{DS} P_o}{(1-2D)^2 M_v^2 V_I^2} + \frac{f_s C_o (1-D)^2 V_I^2}{2(1-2D)^2 P_o} \\ & + \frac{(n+2) V_F M_v (1-D) + 2n V_F D}{n M V_I} \\ & + \frac{2 r_{L1} P}{M_v^2 V_I^2}(n^2 D + M_v^2 (1-D)) + \frac{2 r_c P}{M_v^2 V_I^2}(n^2 D + (M_v - n)^2 (1-D)) \end{aligned}$$

Efficiency plot versus input voltage and output power is shown in figure 3.5.

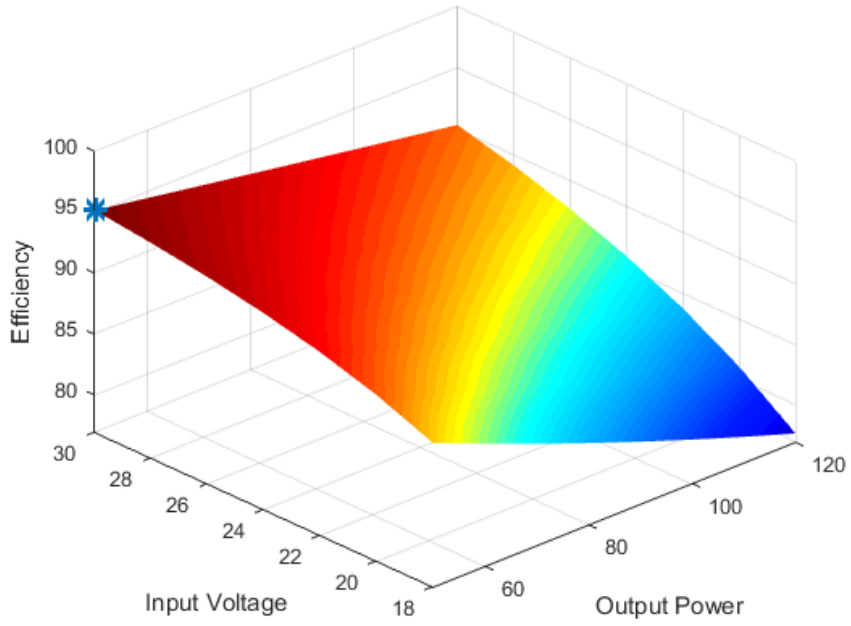

Figure 3.5: Proposed converter efficiency versus input voltage and output power

3.4.2 DC Voltage Conversion Factor of the Non-Ideal Proposed Converter

Based on equation 3.32, voltage conversion ratio of the ideal proposed converter is equal to :

$$M_v = \frac{V_o}{V_I} = \frac{(2n+1) - D}{1 - 2D} \tag{3.73}$$

3.67 However, voltage ratio of proposed converter using non-ideal elements is less than this value, because of the semiconductor devices voltage drop and parasitic resistance. Based on 3.33, current transfer function of proposed converter is :

$$M_I = \frac{I_o}{I_I} = \frac{1 - 2D}{(2n+1) - D} \tag{3.74}$$

This equation is true for both lossless and lossy converter. Therefore the converter efficiency can be written as :

$$\eta = \frac{P_o}{P_I} = \frac{V_o I_o}{V_I I_I} = M_{V(non-ideal)} M_I = M_{V(non-ideal)} \frac{1 - 2D}{(2n+1) - D} \tag{3.75}$$

Therefore the non-ideal voltage transfer function of proposed converter can be written as :

$$\begin{aligned} M_{V(non-ideal)} &= \frac{(2n+1) - D}{1 - 2D} \eta \\ &= \frac{(2n+1) - D}{1 - 2D} \frac{1}{1 + \gamma} \\ \gamma &= \frac{(4n+1)^2 D r_{DS}}{(1-2D)^2 R_L} + \frac{f_s C_o (1-D)^2 R_L}{2((2n+1) - D)^2} \\ &+ \frac{(n+2) V_F M_v (1-D) + 2n V_F D}{n V_o} \\ &+ \frac{2 r_{L1}}{R_L}(n^2 D + M_v^2 (1-D)) + \frac{2 r_c}{R_L}(n^2 D + (M_v - n)^2 (1-D) \end{aligned} \tag{3.76}$$

3.5 Simulation Results

The theoretical results and expressions are confirmed with the simulation results and these results are compared with each other in this section. The proposed converter is simulated in two different softwares, Simulink and PsPice. Moreover, key waveforms of the proposed converter are indicated.

3.5.1 Simulated Proposed Converter in Simulink

A single solar cell is called PV cell. A collection of single solar cells connected together is called PV panel. PV panels usually have nominal voltage of 24 volts and power of 100 watts.

Also for 110 volts AC of utility, 300 volts DC input voltage is needed for half-bridge inverter and for 220 volts AC of utility, 300 volts DC input voltage is needed for full-bridge inverter.

Figure 3.6 shows the half bridge inverter. Therefore, if AC (rms) voltage of 110 Volts is need at the output of the inverter, half bridge inverter should be used with the input DC voltage of 300 Volts.

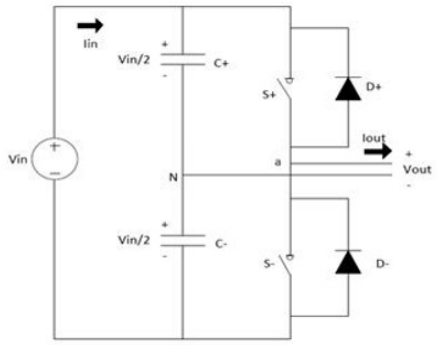

Figure 3.6: Single-phase half bridge inverter

Also Figure 3.7 shows the full bridge inverter. Therefore, if AC (rms) voltage of 220 Volts is needed at the output of the inverter, full bridge inverter should be used with the input DC voltage of 300 Volts.

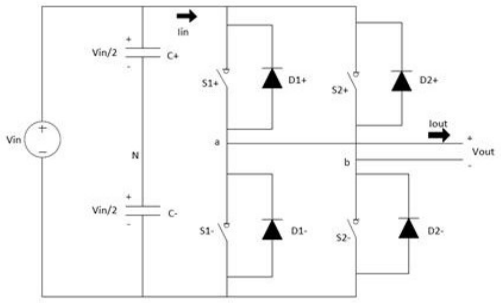

Figure 3.7: Single-phase full bridge inverter

Based on these facts, Proposed DC-DC converter is designed for converting 24 volts to 300 volts. Table 3.1 indicates the component values that are used in the simulated converter and figure 3.8 shows the schematic of simulated converter in simulink.

Table 3.1: Components values that are used in the simulated converter

V_I	24 Volts
L_1 and L_2	330 μH
L_f	600 μH
C	220 μF
$C_{o1} - C_{o5}$	47 μF
R_L	893 Ω

Therefore, the proposed converter is simulated in Simulink software for frequency

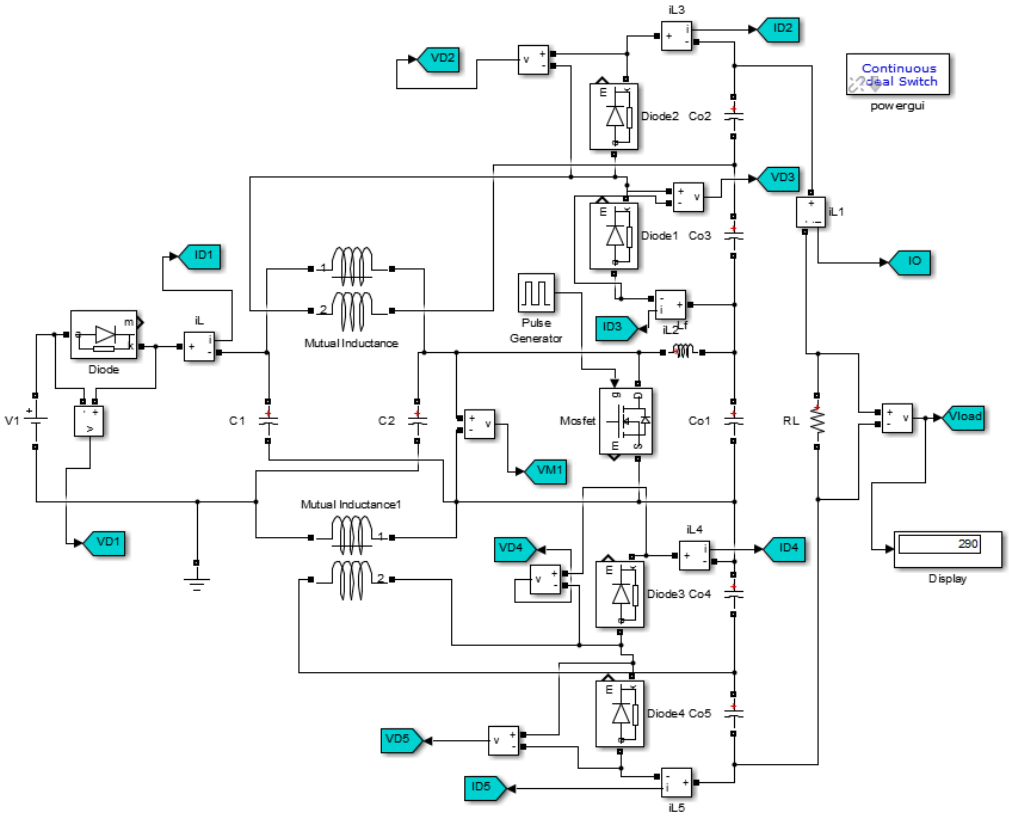

Figure 3.8: Simulated converter schematic in simulink

of 100 KHz ($f_S = 100$ KHz) and active switch duty cycle of (D=0.4). Also the turn ratio is considered to be one ($n = 1$) and for considering the leakage inductance of the coupled inductors, the coupling coefficient is considered to be 0.99.

So as it is shown in table 3.1, input voltage is set to 24 Volts and following result is gotten for the output voltage :

$$\Longrightarrow V_o = 290.1 \qquad Volts \tag{3.77}$$

So the voltage ratio (boosting factor) of the proposed converter in the simulation

is :

$$\Rightarrow V_I = 24 \quad Volts \Rightarrow M_v = \frac{V_o}{V_I} = \frac{290.1}{24} = 12.09 \tag{3.78}$$

Based on equation 4.29, the voltage ratio expression of the proposed converter in the theory is : $M_v = \frac{V_o}{V_I} = \frac{(2n+1) - D}{1 - 2D}$, So with substituting the D and n values :

$$\Rightarrow n = 1, D = 0.4 \Longrightarrow M_v = 13 \tag{3.79}$$

As it is shown, the voltage ratio of the simulated converter is less than the theoretical gain value. This discrepancy is because of the semiconductor devices (diode and switch) voltage drop when they are on. Specially in this proposed converter, because the boosting factor is huge, the semiconductor devices current is high, so the voltage drops are considerable.

However, semiconductor devices are considered to be ideal and without any voltage drop when they are on in the theoretical calculations.

Furthermore the turn ratio (n) is considered to be equal to 1 in theoretical calculation, however, it will be less than 1 in the simulation results. Those reasons make a little bit difference between the theoretical and simulation results.

The z-source network capacitor and output capacitors voltage are shown in table 3.2 :

Table 3.2: Z-source network capacitor and the output capacitors voltage.

V_C	69.69 Volts
V_{o1}	69.5 Volts
V_{o2}	66.59 Volts
V_{o3}	43.69 Volts
V_{o4}	43.69 Volts
V_{o5}	66.59 Volts

Also these values can be calculated base on theoretical expressions and equations, therefore :

$$V_C = V_{o1} = \frac{1-D}{1-2D}.V_I = \frac{(1-0.4)}{1-2\times 0.4} \times 24 \quad Volts = 72 \quad Volts \tag{3.80}$$

$$V_{o2} = V_{o5} = n.V_C = 1 \times 72 \quad Volts = 72 \quad Volts \tag{3.81}$$

$$V_{o3} = V_{o4} = n.(V_C - V_I) = 1 \times (72-24) \quad Volts = 48 \quad Volts \tag{3.82}$$

So the reasons of small differences between the theoretical and simulation results has been already explained.

Next figures indicate the key waveforms of the proposed converter from simulated schematic. In these plots, the dotted line shows the PWM (pulse width modulation) voltage that has been applied to the gate-source of active switch S. Switch S voltage waveform is shown in figure 3.9.

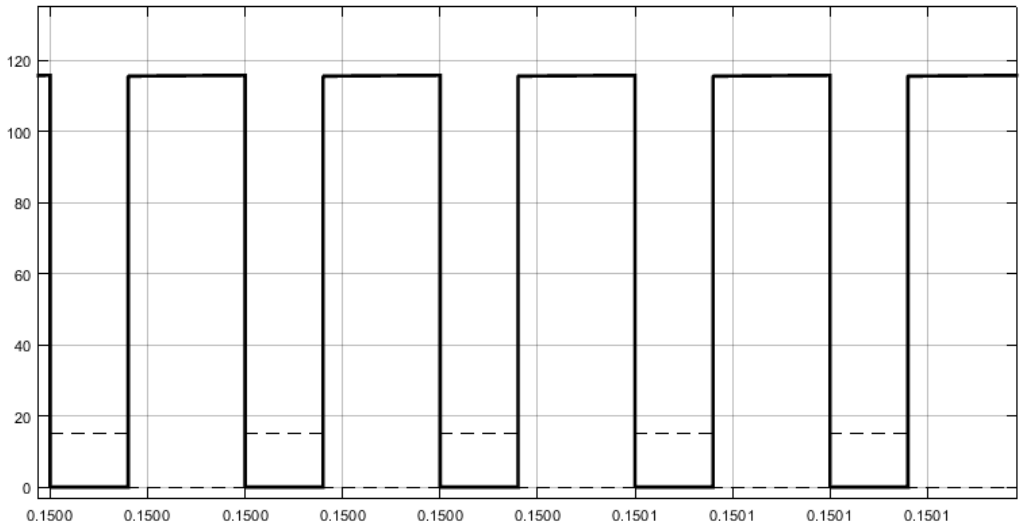

Figure 3.9: Active switch S voltage waveform (V_S)

The active switch S current waveform is indicated in figure 3.10 indicates .

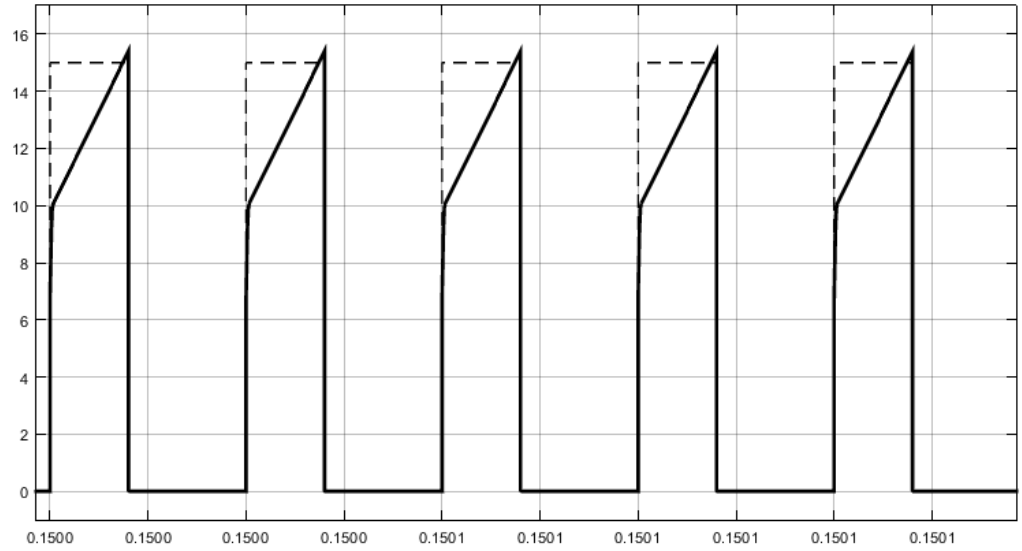

Figure 3.10: Active switch S current waveform (i_S)

The secondary side of the coupled inductors current is shown in figure 3.11.

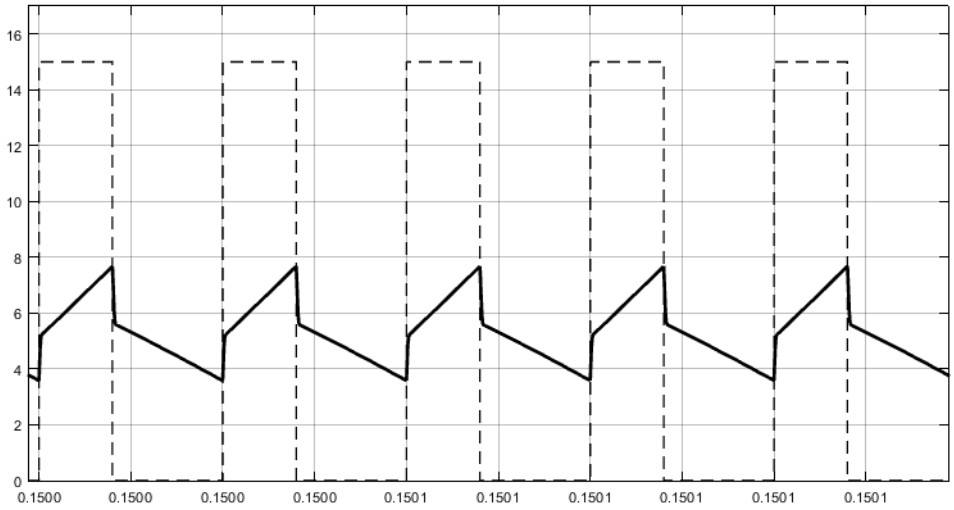

Figure 3.11: Secondary side of coupled inductors current waveform (i_{L2})

The secondary side of the coupled inductors current is displayed in 3.12.

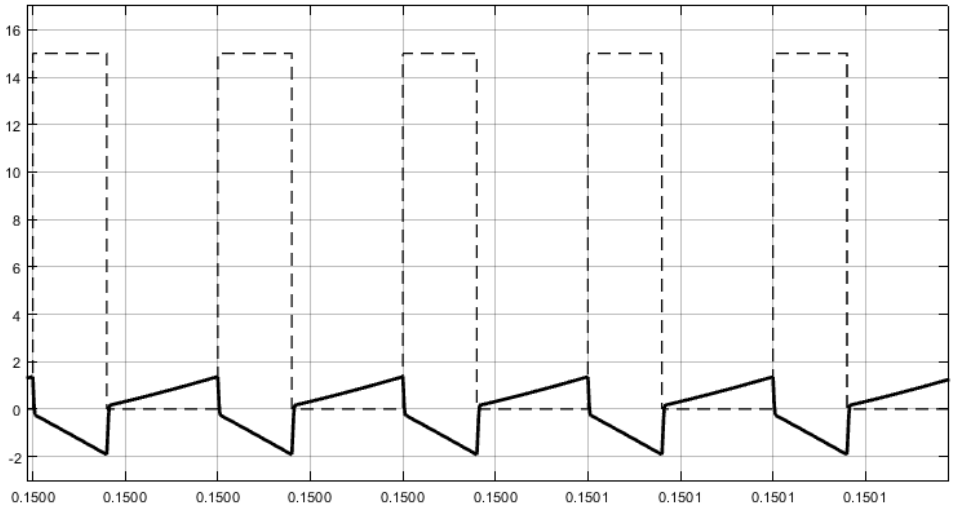

Figure 3.12: Primary side of coupled inductors current waveform (i_{L1})

Magnetizing current waveform of the coupled inductors is shown in figure 3.13.

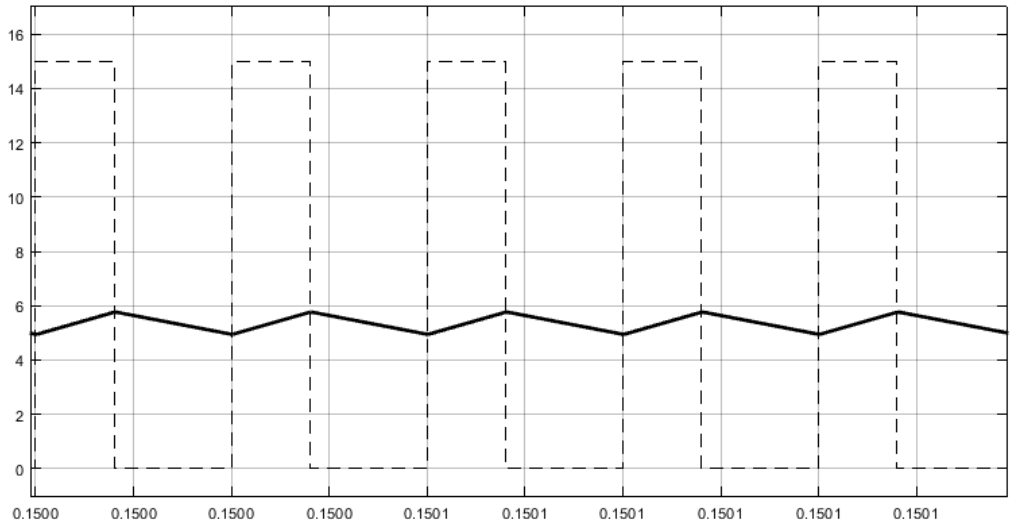

Figure 3.13: Magnetizing inductance current waveform of coupled inductors (i_{Lm})

Input diode voltage waveform is indicated in figure 3.14.

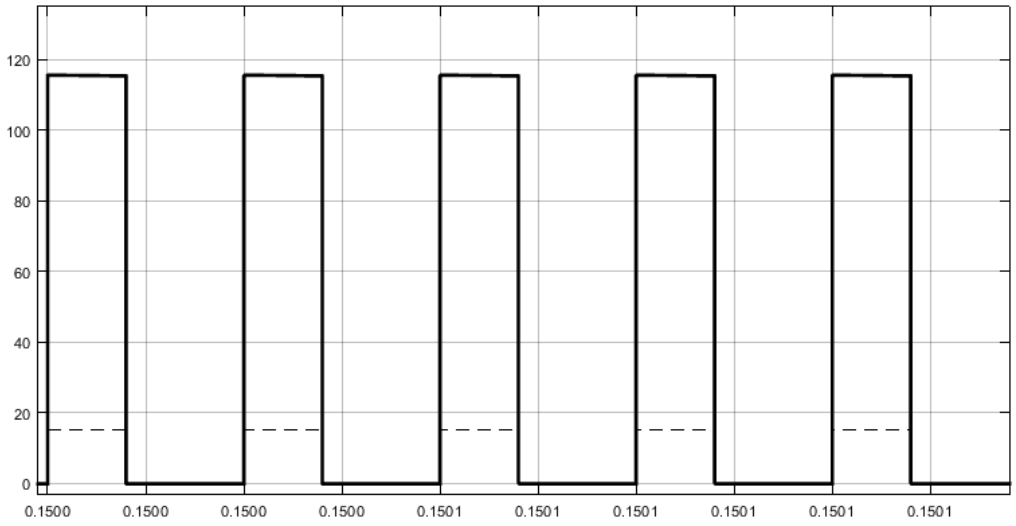

Figure 3.14: Input diode voltage waveform (v_{D1})

The voltage waveform across diode D_2 or D_5 is shown in figure 3.15.

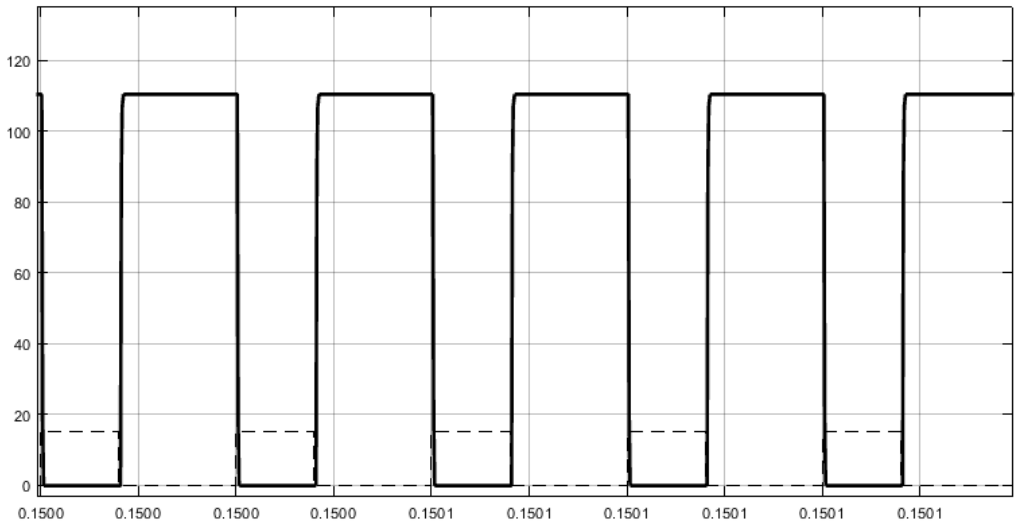

Figure 3.15: Diode D_2 or D_5 voltage waveform (v_{D2} or v_{D5})

The voltage waveform across diode D_3 or D_4 is indicated in figure 3.16.

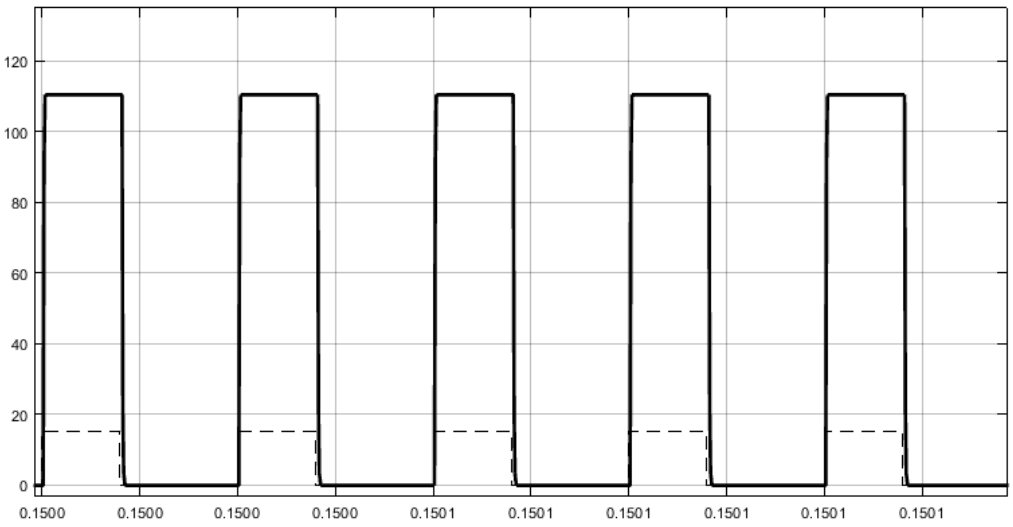

Figure 3.16: Diode D_3 or D_4 voltage waveform (v_{D3} or v_{D4})

The input diode current waveform is shown in figure 3.17. The primary and

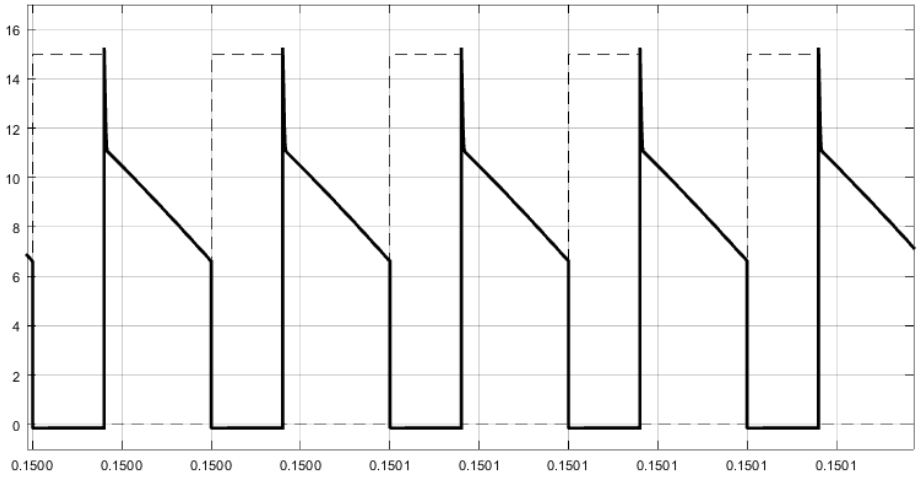

Figure 3.17: Input diode current waveform (i_{D1})

secondary side of coupled inductors voltage waveforms are shown in figure 3.18. indicates .

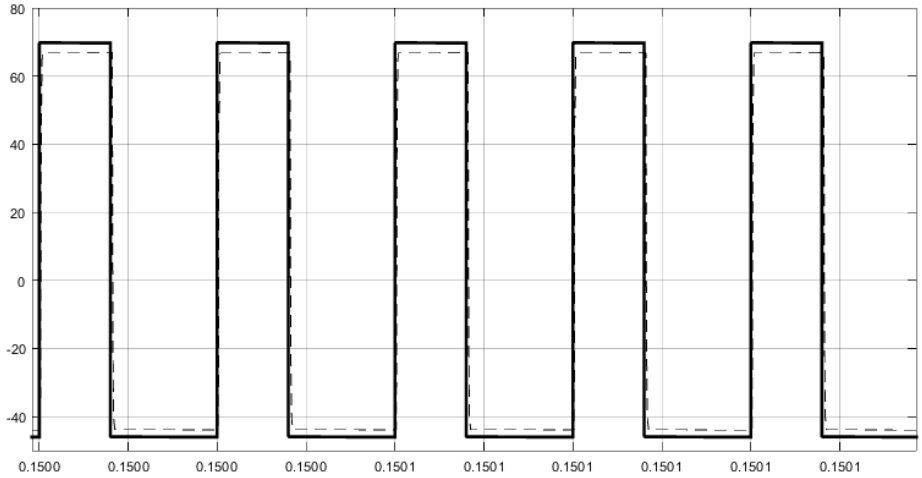

Figure 3.18: Coupled inductors primary and secondary voltage waveforms(v_{L1} and v_{L2})

The output filter current waveform is indicated in figure 3.19.

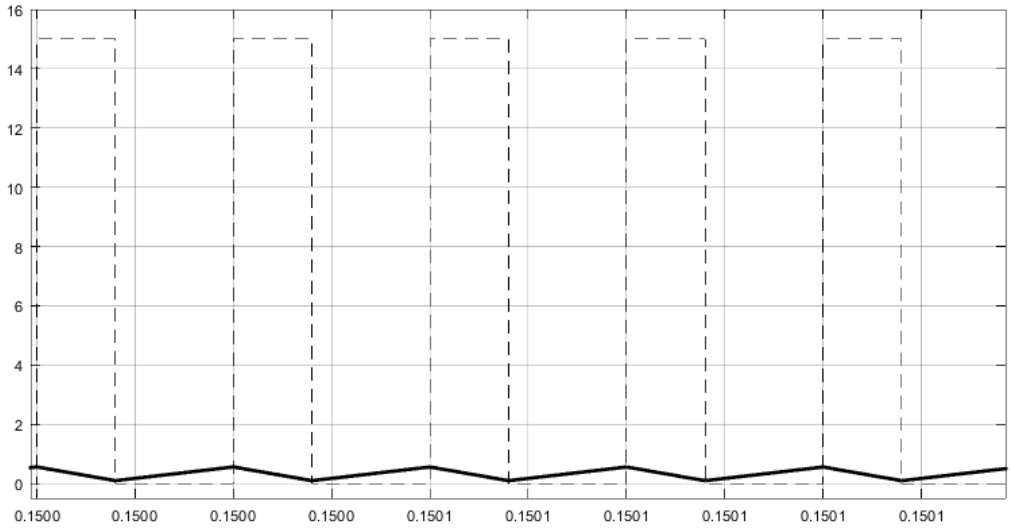

Figure 3.19: Output filter inductor current waveform(i_{Lf})

As it is shown in figure 3.18, the primary side of coupled inductor voltage is $v_{L1} = 69.6$ Volts when the switch is on and this voltage is $v_{L1} = -46.8$ Volts when the switch is off. The following values are the calculated primary side voltage of the coupled inductors based on the theoretical equations.

$$S = on \Longrightarrow v_{L1} = v_C = 72 \ Volts \tag{3.83}$$

$$S = off \Longrightarrow v_{L1} = v_I - v_C = 24 - 72 = -48 \ Volts \tag{3.84}$$

As it was already explained, the coupled inductors turn ratio is a little bit less the 1 as it can be seen in the figure 3.18.

When the active switch S is on, diodes D_1, D_3 and D_4 are reverse-biased and so

they are off. Based on figures 3.14 and 3.16, their voltages are :

$$v_{D1} = 118\ Volts \tag{3.85}$$

$$v_{D3} = v_{D4} = 112\ Volts \tag{3.86}$$

In the other hand, diodes D_2 and D_5 are reverse-biased when the switch S is off. So the voltage across them can be measured based on figures 3.9 and 3.16. Therefore :

$$v_S = 118\ Volts \tag{3.87}$$

$$v_{D2} = v_{D5} = 112\ Volts \tag{3.88}$$

Based on theoretical expressions :

$$v_S = v_{D1} = 2V_C - V_I = 2(72) - 24\ Volts = 120\ Volts \tag{3.89}$$

$$v_{D2} = v_{D3} = v_{D4} = v_{D5} = v_{o2} + v_{o3} = v_{o4} + v_{o5} = (72 + 48)\ Volts = 120\ Volts \tag{3.90}$$

As it was prove, theoretical calculations are confirmed with the simulation results. Little differences are because of switch and diode turn on voltage that has been ignored in theoretical calculations.

3.5.2 Simulated Proposed Converter in PSpice

Also, the proposed converter is simulated in PSpice software for frequency of 100 KHz (f_S = 100 KHz) and active switch duty cycle of (D=0.4). moreover, the turn ratio is considered to be one ($n = 1$) and for considering the leakage inductance of the coupled inductors, the coupling coefficient is considered to be 0.99. The schematic of simulated converter in PSpice is shown in figure 3.20.

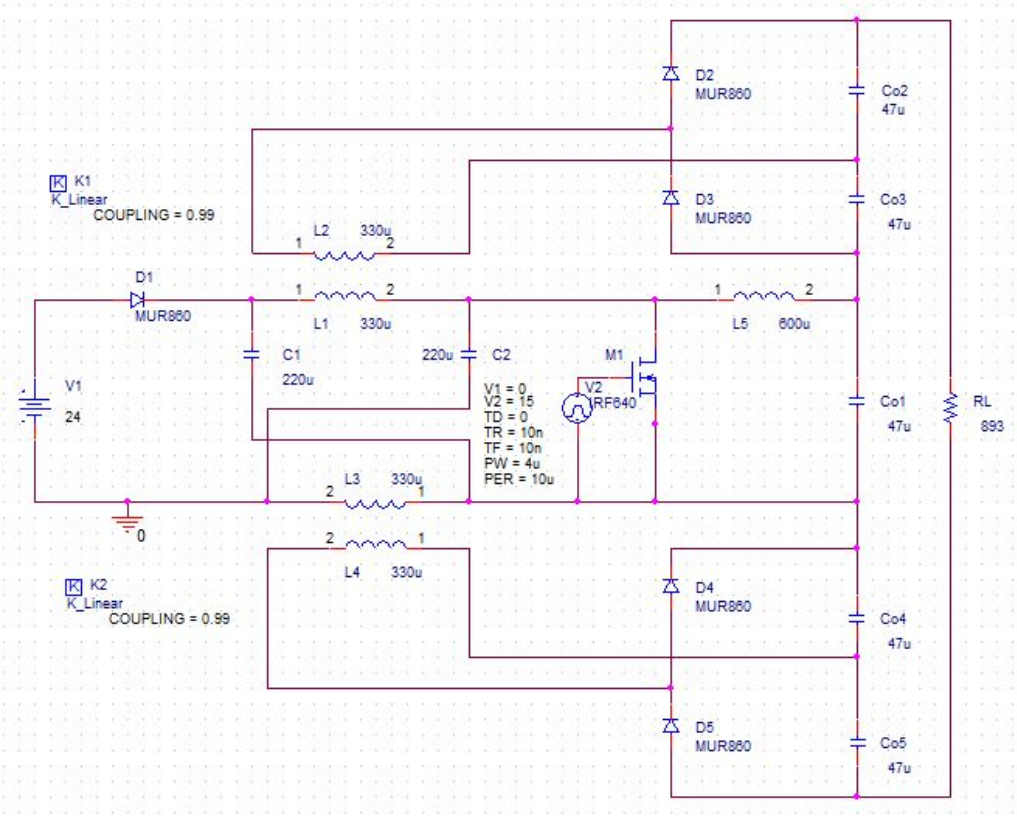

Figure 3.20: Simulated converter schematic in simulink

So as it is shown in table 3.1, input voltage is set to 24 Volts and following result

is gotten for the output voltage :

$$\Longrightarrow V_o = 286.2 \qquad Volts \tag{3.91}$$

So the voltage ratio (boosting factor) of the proposed converter in the simulation is :

$$\Rightarrow V_I = 24 \quad Volts \Rightarrow M_v = \frac{V_o}{V_I} = \frac{286.2}{24} = 11.925 \tag{3.92}$$

Based on equation 4.29, the voltage ratio expression of the proposed converter in the theory is : $M_v = \dfrac{V_o}{V_I} = \dfrac{(2n+1) - D}{1 - 2D}$, So with substituting the D and n values :

$$\Rightarrow n = 1, D = 0.4 \Longrightarrow M_v = 13 \tag{3.93}$$

As it was shown for simulated converter in simulink, the voltage ratio of the simulated converter is less than the theoretical gain value. This discrepancy is because of the semiconductor devices (diode and switch) voltage drop when they are on. Specially in this proposed converter, because the boosting factor is huge, the semiconductor devices current is high, so the voltage drops are considerable.

However, semiconductor devices are considered to be ideal and without any voltage drop when they are on in the theoretical calculations.

Furthermore the turn ratio (n) is considered to be equal to 1 in theoretical calculation, however, it will be less than 1 in the simulation results. Those reasons make a little bit difference between the theoretical and simulation results.

The z-source network capacitor and output capacitors voltage are shown in table 3.3 :

Table 3.3: Z-source network capacitor and the output capacitors voltage.

V_C	69.69 Volts
V_{o1}	68.73 Volts
V_{o2}	65.82 Volts
V_{o3}	42.92 Volts
V_{o4}	42.92 Volts
V_{o5}	65.82 Volts

Also these values can be calculated base on theoretical expressions and equations, therefore :

$$V_C = V_{o1} = \frac{1-D}{1-2D}.V_I = \frac{(1-0.4)}{1-2\times 0.4} \times 24 \quad Volts = 72 \quad Volts \tag{3.94}$$

$$V_{o2} = V_{o5} = n.V_C = 1 \times 72 \quad Volts = 72 \quad Volts \tag{3.95}$$

$$V_{o3} = V_{o4} = n.(V_C - V_I) = 1 \times (72-24) \quad Volts = 48 \quad Volts \tag{3.96}$$

So the reasons of small differences between the theoretical and simulation results has been already explained.

Next figures indicate some of the key waveforms of the proposed converter from simulated schematic. In these plots, the dotted line shows the PWM (pulse width modulation) voltage that has been applied to the gate-source of active switch S. Based on previous figures, almost same results were achieved with simulating the proposed converter in PSpice software.

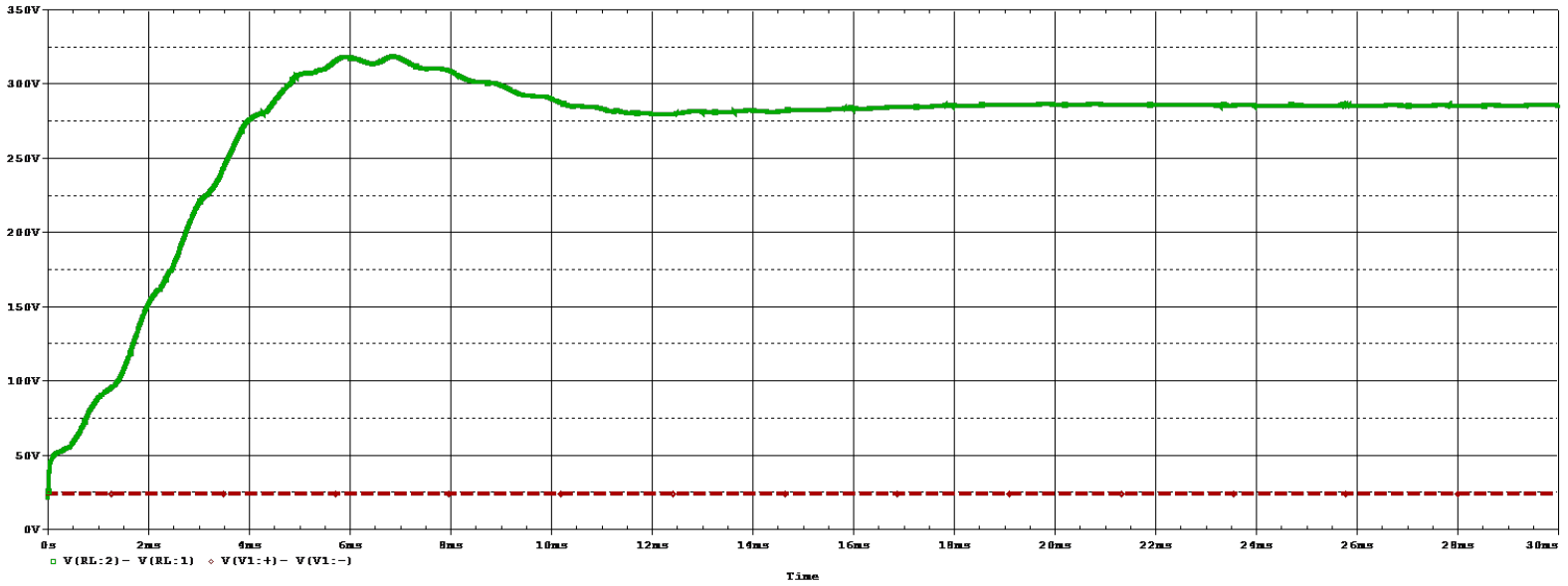

Figure 3.21: Output (green) and input (red) voltage waveforms

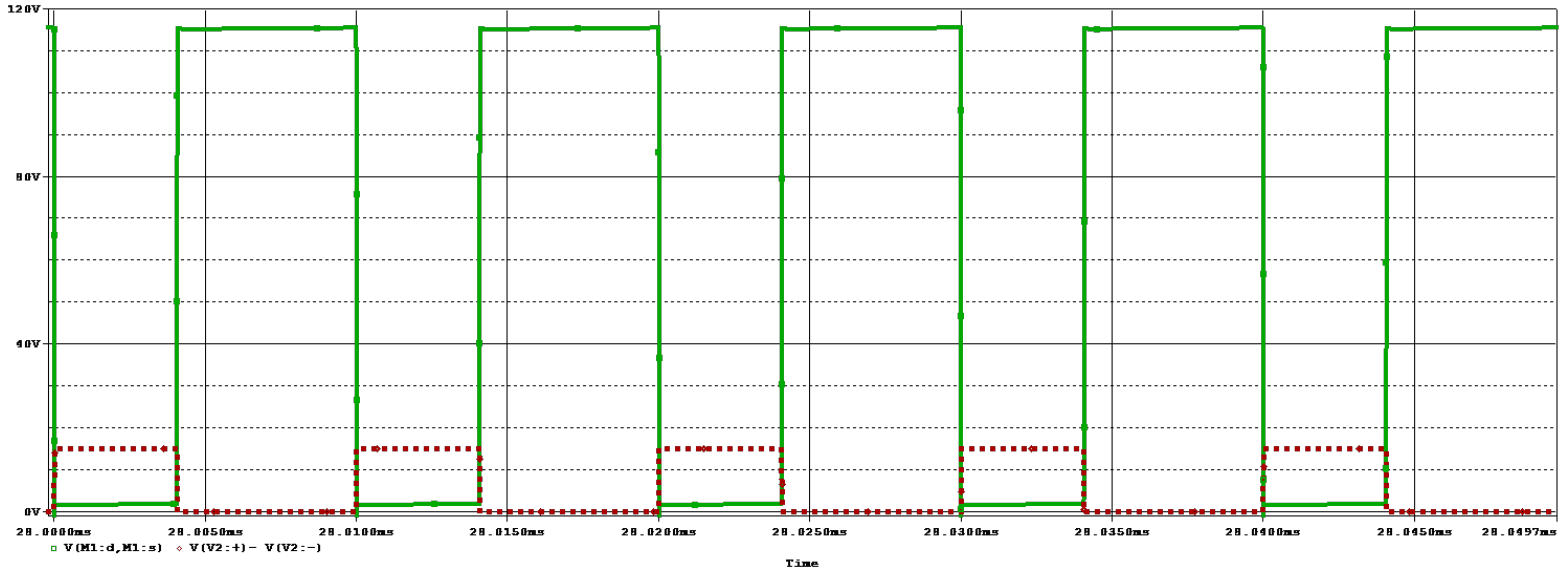

Figure 3.22: Active switch S voltage waveform (V_S)

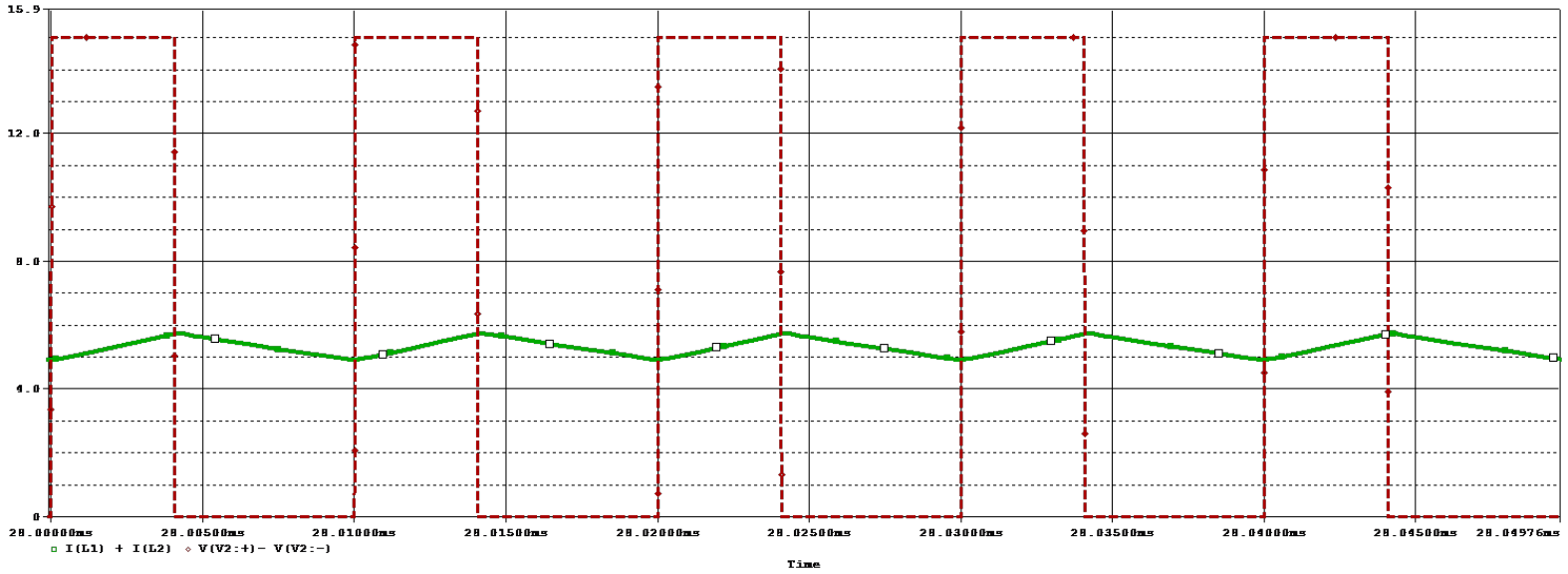

Figure 3.23: Magnetizing inductance current waveform of coupled inductors (i_{Lm})

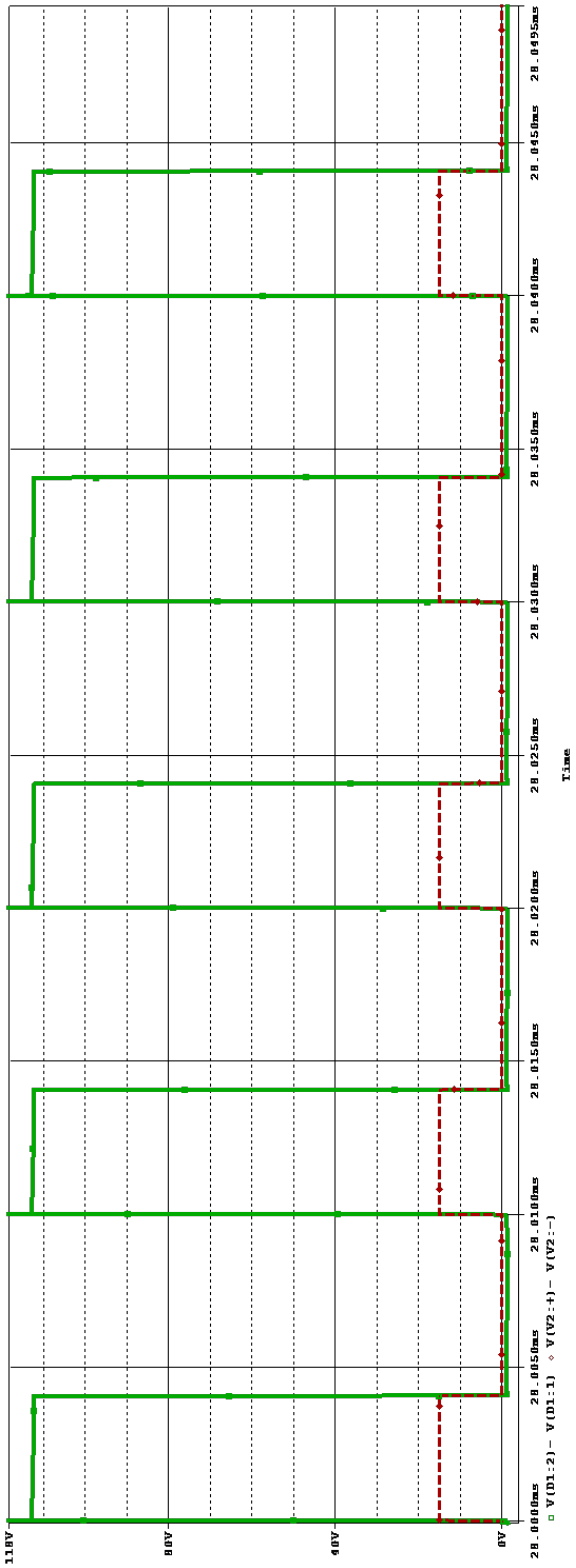

Figure 3.24: Input diode voltage waveform (v_{D1})

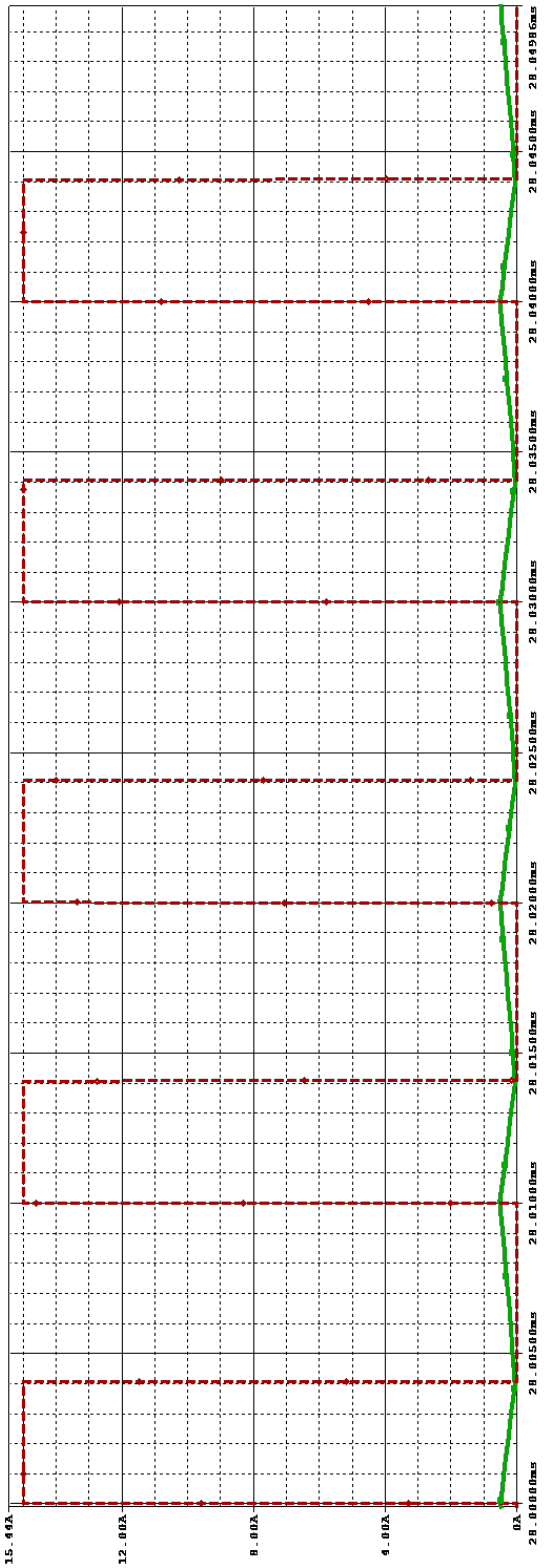

Figure 3.25: Output filter inductor current waveform(i_{Lf})

3.5.3 Design Guidelines

In this section, the design guidelines for choosing the right elements for proposed converter. Based on following equations, inductor (L) can be designed.

$$i_L(t) = \frac{1}{L}\int_0^t v_L dt + i_L(0) \tag{3.97}$$

Therefore, following equations are for the first time interval of a switching period :

$$v_L = L\frac{di_L}{dt} = V_C \tag{3.98}$$

$$\Longrightarrow i_L(t) = \frac{V_C}{L}t + i_L(0) \tag{3.99}$$

$$\Longrightarrow i_L(DT) = \frac{V_C}{L}(DT) + i_L(0) \tag{3.100}$$

$$\Longrightarrow \Delta i_L = i_L(DT) - i_L(0) = \frac{V_C D}{f_s L} \tag{3.101}$$

Therefore, according to the desirable current ripple of the magnetizing inductances, L_m is calculated as :

$$\Longrightarrow L_m = \frac{V_C D}{f_{sw}\Delta i_L} \tag{3.102}$$

Moreover, according to the desirable current ripple of the filter inductances, L_f is calculated as :

$$\Longrightarrow L_f = \frac{V_{C_{o1}} D}{f_{sw}\Delta i_{L_f}} \tag{3.103}$$

During on time of the switch, the currents of the primary windings are provided by capacitors C. Therefore these capacitors can be designed according to their desirable

voltage ripple as following equations :

$$v_C(t) = \frac{1}{C}\int_0^t v_C dt + v_C(0) \tag{3.104}$$

Therefore, following equations are for the first time interval of a switching period :

$$i_{L_m} = i_{L_1} + i_{L_2} \tag{3.105}$$

$$i_C = C\frac{dv_C}{dt} = I_{L_m} \tag{3.106}$$

$$\Longrightarrow v_C(t) = \frac{I_{L_m}}{C}t + v_C(0) \tag{3.107}$$

$$\Longrightarrow v_C(DT) = \frac{I_{L_m}}{C}(DT) + v_C(0) \tag{3.108}$$

$$\Longrightarrow \Delta v_C = v_C(DT) - v_C(0) = \frac{I_{L_m}D}{f_s C} \tag{3.109}$$

$$\Longrightarrow C = \frac{I_{L_m}D}{f_{sw}\Delta v_C} \tag{3.110}$$

The same equations can be used for designing output capacitors. For example for designing capacitor C_{o1}, following equation can be used :

$$\Longrightarrow C_{o1} = \frac{I_{L_f}D}{f_{sw}\Delta v_{C_{o1}}} \tag{3.111}$$

The proper diode and switches can be selected base on their voltage and current stresses. The main switch S and diodes D_1, D_2, D_3, D_4 and D_5 stress voltages are given in equations 3.36, 3.40 and 3.42.

3.5.4 Experiment Results

As it was mentioned in the introduction section, a prototype of the proposed converter is implemented. It is tested for converting 24 V input voltage to 300 V output voltage and 100 W output power. Implemented prototype is shown in figure 3.26. It is implemented for coupled inductors turn ratio $n = 1$ and switching frequency of $f_S = 100$ KHz. Based on output power of 100 W and output voltage of 300 Volts and resistance availabilities, load resistance of 893 Ω is chosen for load resistance. Important parameters of the implemented prototype is shown in table 3.4.

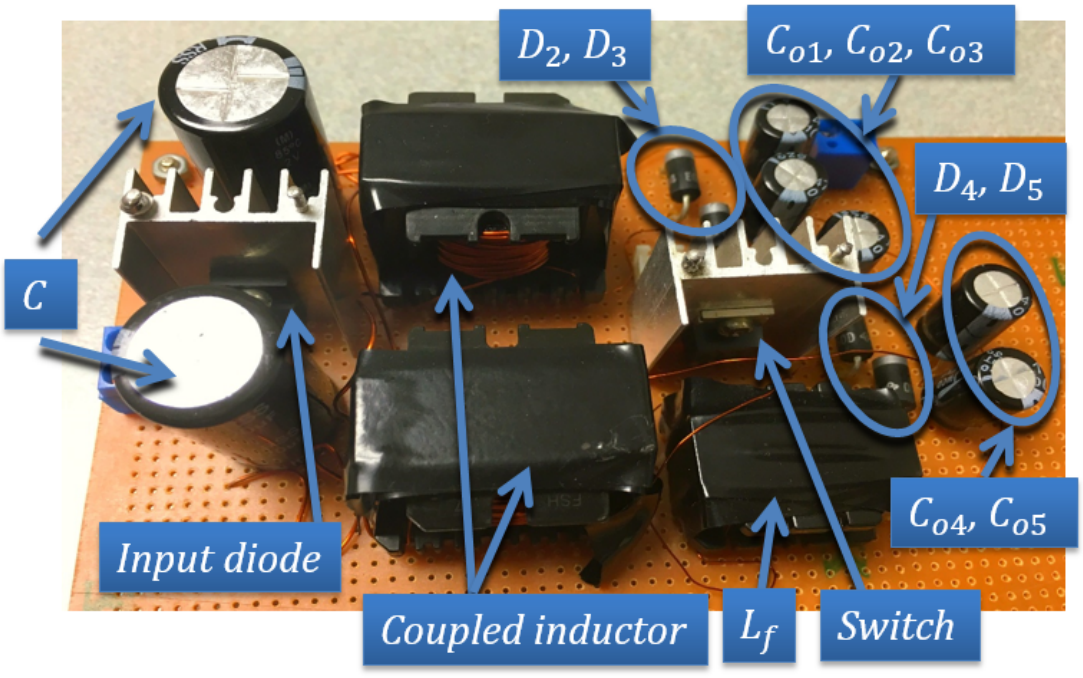

Figure 3.26: Implemented prototype of proposed converter

The implemented prototype has efficiency of 93 percent under full load. Key

Table 3.4: Important parameters of the implemented prototype.

S	IRF3710
D_1	MBR20150
D_2, D_3, D_4, D_5	EGP50D
L_1, L_2	357 μH
C	220 μF
L_l	10.8 μH
$C_{o1}, C_{o2}, C_{o3}, C_{o4}, C_{o5}$	47 μ F

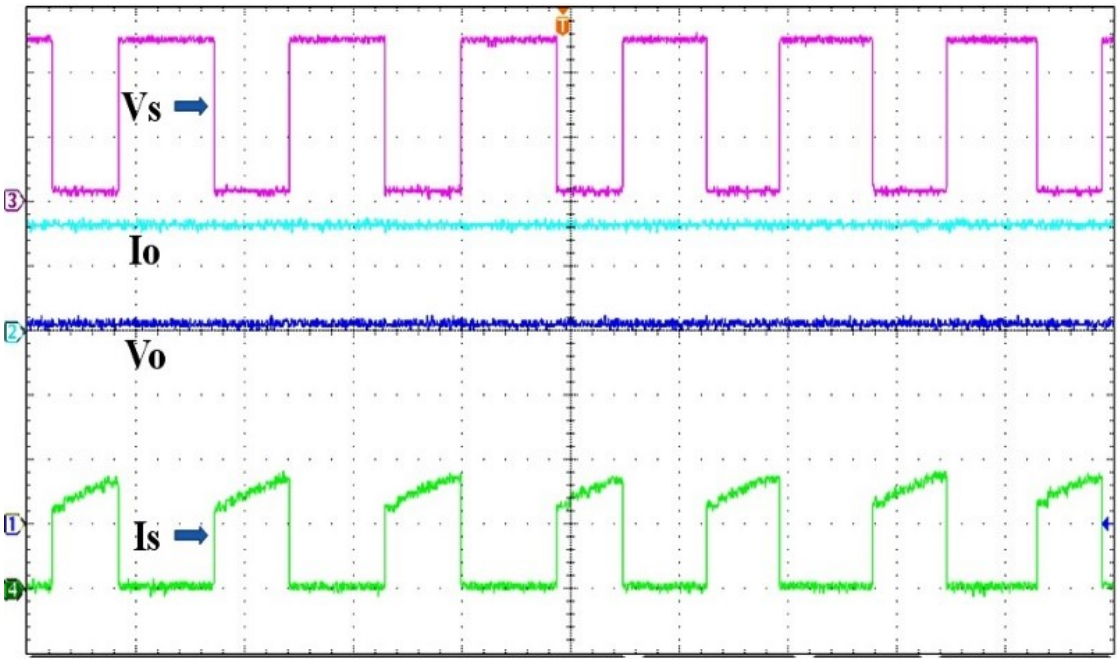

Figure 3.27: Key waveforms of the implemented prototype (a) V_o (Ch. 1, 100 V/div) and I_o (Ch. 2, 200 mA/div), V_S (Ch. 3, 50 V/div) and I_S (Ch. 4, 10 A/div), Time scale: 2.5 μs/div

waveforms of the tested prototype are shown in figure 3.27 and 3.28.

Parameter D can be measured by looking at the switch on time. It can be seen that for having voltage ratio of 13 in experiment, duty cycle of gate-source voltage of the main switch, must be greater than 0.4. I t should be about 0.406 in experiment.

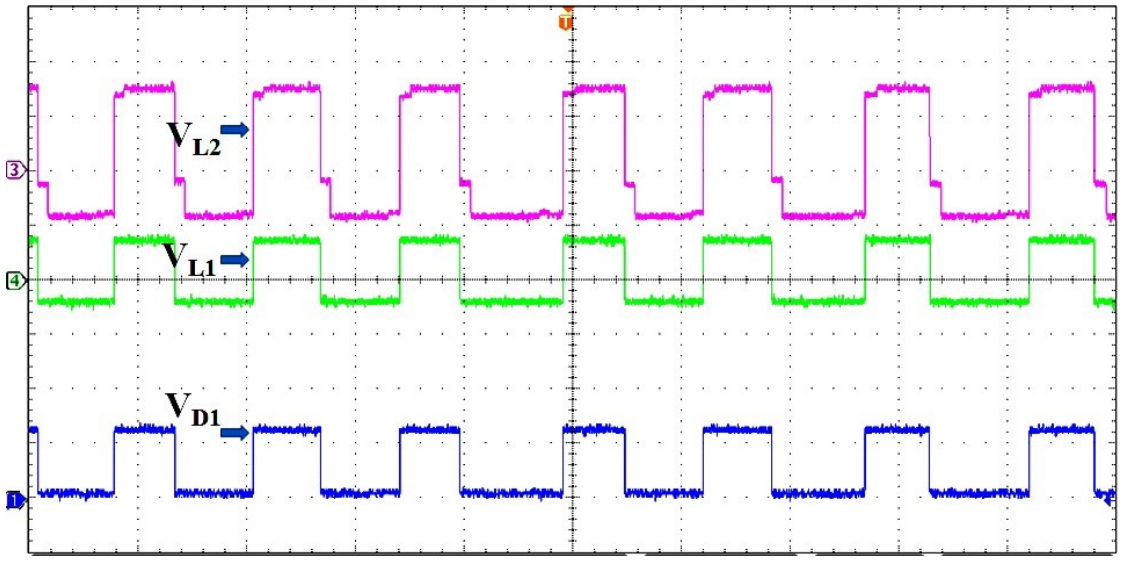

Figure 3.28: Key waveforms of the implemented prototype (b) V_{D1} (Ch. 1, 100 V/div), V_{L2} (Ch. 3, 50 V/div), V_{L1} (Ch. 4, 100 V/div), time scale: 2.5 μs/div

Therefore, for D=0.406, theoretical voltage gain would be more than 13.

Main switch S and input diode D_1 stress voltage when they are off and coupled inductors voltage when switch is off and on, are measured based on experimental waveforms. Moreover, the theoretical results are calculated. It should be considered that teh experimental D is a bit larger than 0.4.

$$v_S = 124 \ Volts \tag{3.112}$$

$$v_{D1} = v_{D5} = 121 \ Volts \tag{3.113}$$

$$S = on \Longrightarrow v_{L1} = 71 \ Volts \tag{3.114}$$

$$S = off \Longrightarrow v_{L1} = -44 \ Volts \tag{3.115}$$

Based on theoretical equations :

$$V_C = \frac{1-D}{1-2D}.V_I = 3 \times 24 = 72 \ Volts \tag{3.116}$$

$$\Longrightarrow V_S = 2V_C - V_I = 120 \ Volts \tag{3.117}$$

$$\Longrightarrow V_S = 2V_C - V_I = 120 \ Volts \tag{3.118}$$

$$v_{D1} = v_{D5} = 121 \ Volts \tag{3.119}$$

$$S = on \Longrightarrow v_{L1} = V_C = 72 \ Volts \tag{3.120}$$

$$S = off \Longrightarrow v_{L1} = V_I - V_C = 24 - 72 = -48 \ Volts \tag{3.121}$$

Therefore, a novel high step up z-sorce dc-dc converter with flyback and voltage multiplier is introduced in this thesis. Derived equations indicate that voltage gain of conventional z-source converter is increased greatly. The proposed converter eliminates the problem of complexity and great duty cycle in conventional high step up converters [46]. Moreover, low stress voltage, high efficiency and wide range of voltage gain by choosing turn ratio, make it a good candidate for high step up applications, such as boosting low output voltage of solar panels. This converter also can be used for maximum power point tracking and droop control in micro grid applications [28, 29, 43–45]. The experiment results verified the theoretical and simulation results.

4. COMPARISON RESULTS

In this section, the proposed converter is compared with other DC-DC converters. As it is shown in figure 4.1, the output voltage of a 100 W PV panel (24 V DC) is converted to 120 V AC with the power processing unit (PPU). Therefore, a high step-up DC-DC converter is needed to convert 24 V DC to 300 V DC for the half bridge inverter input. So the gain of 12.5 is needed.

This comparison is made between single switch DC-DC converters. Due to the single switch, an easy control and efficient MPPT will be achieved.

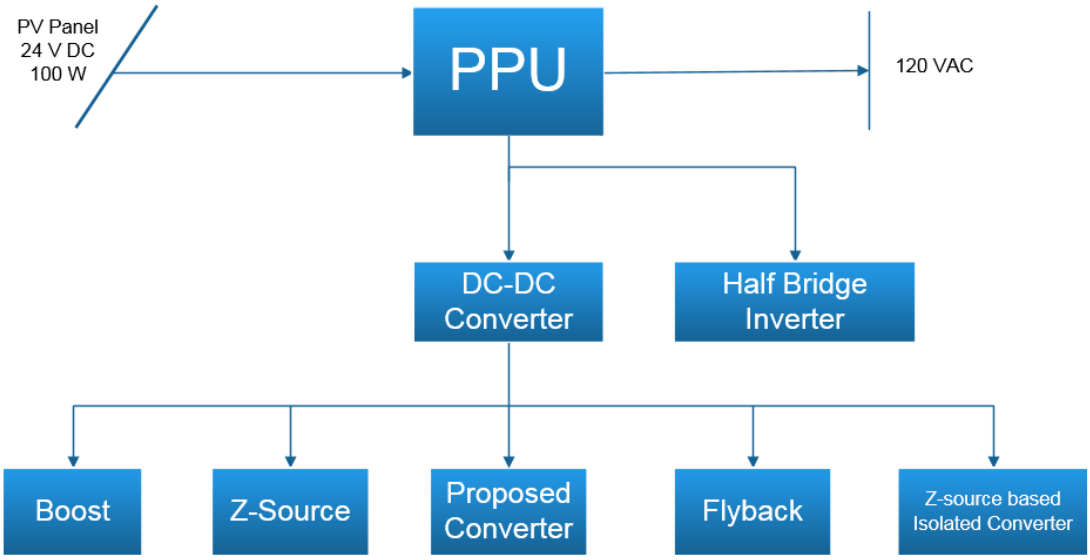

Figure 4.1: Comparison structure of single switch DC-DC converters

4.1 Conventional Boost Converter

The conventional DC-DC boost converter is shown in figure 4.2. It can not be used to achieve practical gain of 12.5.

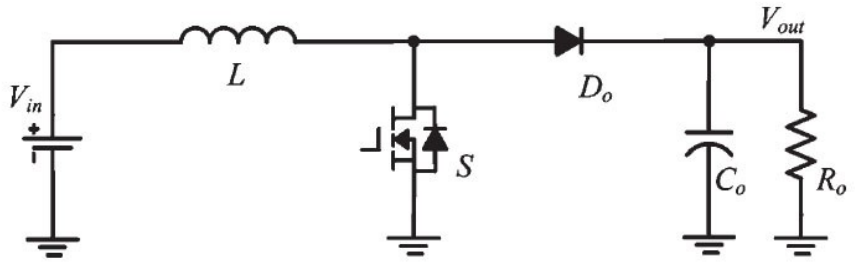

Figure 4.2: Boost dc-dc converter topology

As it was discussed in section 2, voltage gain ratio of the ideal conventional DC-DC boost converter can be calculated as :

$$M(D) = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{4.1}$$

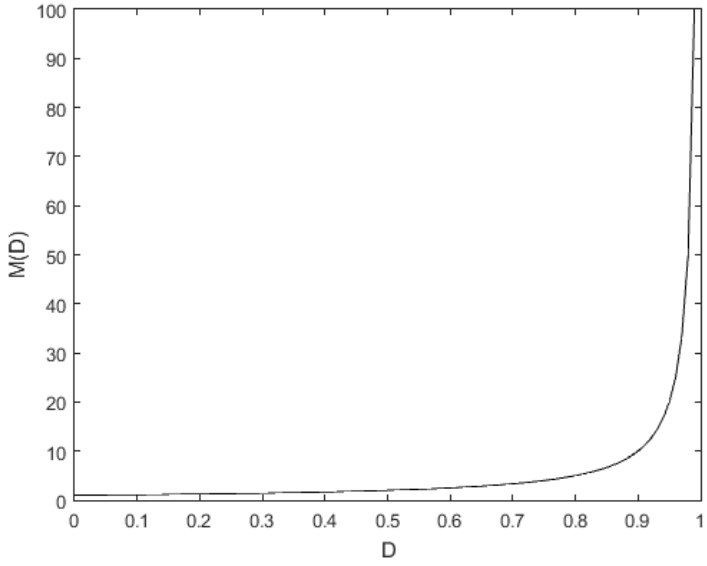

Figure 4.3: Ideal Boost dc-dc converter voltage ratio

Based on equation 4.1 and figure 4.3, voltage ratio of ideal boost converter can be infinite theoretically.

However, a non-ideal boost converter has resistance R_L in series with the inductor, to model the resistance of the inductor winding. Therefore, the non-ideal boost voltage ratio and efficiency can be calculated by following equations :

$$M_{(non-ideal)} = \frac{V_{out}}{V_{in}} = \frac{1}{1-D} \times \frac{1}{1 + \frac{r_L}{(1-D)^2 R_o}} \tag{4.2}$$

$$M_{I(DC)} = \frac{I_o}{I_I} = 1 - D \tag{4.3}$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_o I_o}{V_I I_I} = M_{(non-ideal)}.(1-D) \tag{4.4}$$

$$\eta = \frac{1}{1 + \frac{r_L}{(1-D)^2.R_o}} \tag{4.5}$$

$$k := \frac{r_L}{R_o} \tag{4.6}$$

As it is shown in figure 4.4, inductor winding resistance R_L (and also other loss elements) limits the output voltage and the maximum gain of about 2 can be achieved for reasonable duty ratio. Moreover, based on figure 4.5, efficiency is decreased greatly in higher duty ratio [13], [22]. Therefore, boost converter can not be used to achieve high step-up gain like 12.5.

4.2 Flyback Converter

Flyback dc-dc converter topology is shown in figure 4.6. It is an example of using high turn ratio transformer in high step-up converters for high voltage gain. Voltage

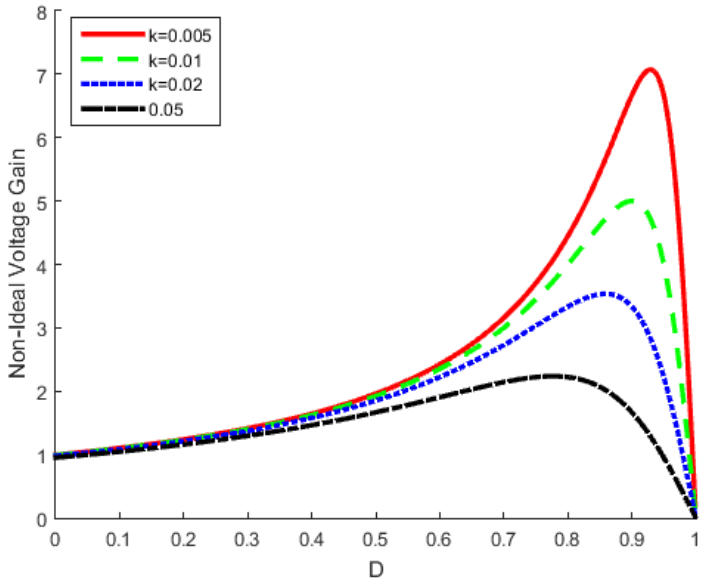

Figure 4.4: Voltage gain VS. duty cycle, non ideal boost for different K.

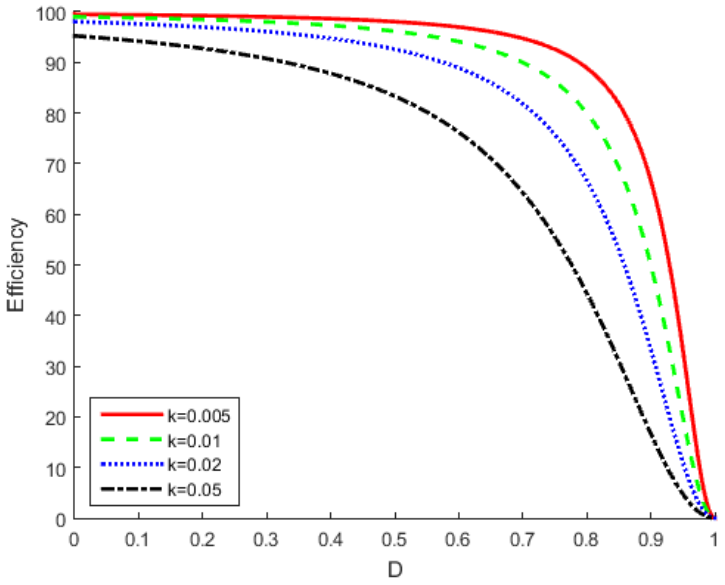

Figure 4.5: Efficiency VS. duty cycle, non-ideal boost

gain expression for an ideal flyback converter is shown in equation 4.7.

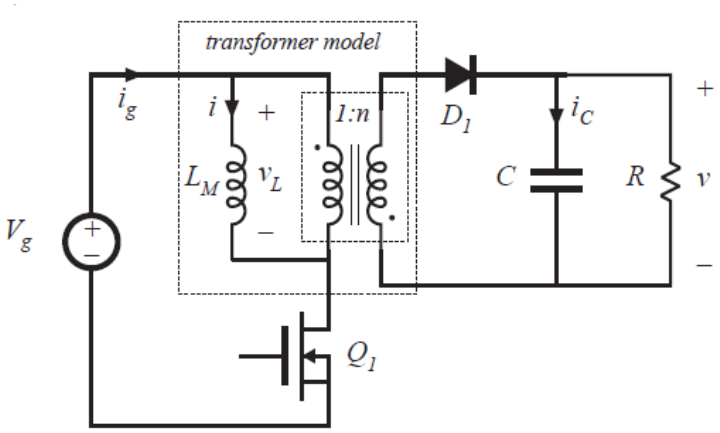

Figure 4.6: Flyback dc-dc converter topology

$$M(D) = \frac{V}{V_g} = n.\frac{D}{1-D} \tag{4.7}$$

Voltage gain graph versus duty cycle of the main switch is shown in figure 4.7 for different transformer turn ratio.

Based on equation 4.7 and figure 4.7, voltage ratio of ideal flyback converter can be infinite for high duty ratio theoretically.

However, a non-ideal flyback converter has resistance R_L in series with the transformer, to model the resistance of the inductor winding. Therefore, the non-ideal flyback voltage ratio and efficiency can be calculated by following equations :

$$M_{(non-ideal)} = \frac{V_{out}}{V_{in}} = \frac{nD}{1-D} \times \frac{1}{1 + \frac{n^2 D r_L}{(1-D)^2 R_o}} \tag{4.8}$$

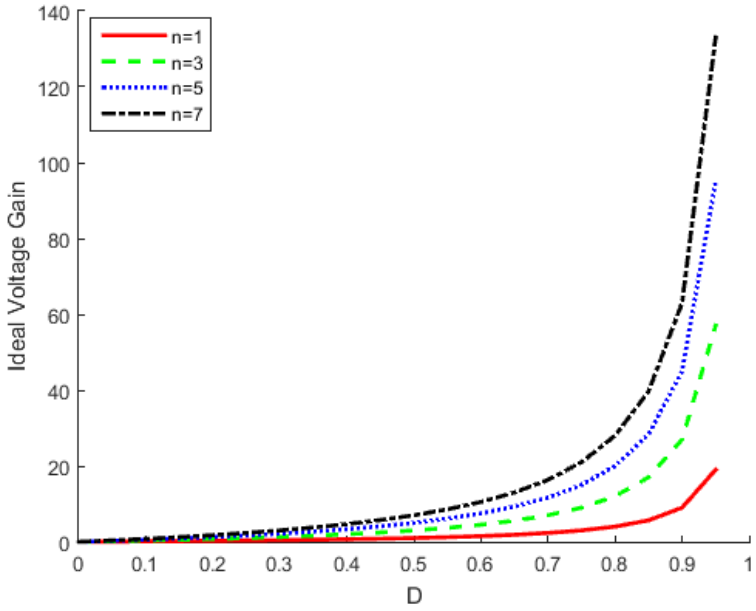

Figure 4.7: Flyback converter voltage gain versus duty cycle for different transformer turn ratio

$$i_{Q1} = I_I + n.I_o = \frac{nIo}{(1-D)} \tag{4.9}$$

$$I_I = \frac{1}{T}\int_0^T i_{Q1}dt = \frac{1}{T}\int_0^{DT} \frac{nIo}{(1-D)}dt = \frac{nI_oD}{(1-D)} \tag{4.10}$$

$$M_{I(DC)} := \frac{I_o}{I_I} = \frac{(1-D)}{nD} \tag{4.11}$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_oI_o}{V_II_I} = M_{(non-ideal)}.\frac{(1-D)}{nD} \tag{4.12}$$

$$\eta = \frac{1}{1+\dfrac{n^2Dr_L}{(1-D)^2R_o}} \tag{4.13}$$

$$k := \frac{r_L}{R_o} \tag{4.14}$$

Voltage gain graphs versus duty ratio for non-ideal flyback converter are shown in figures 4.8 and 4.9.

Duty ratio of 0.6 or less should be used in order to keep instantaneous current of

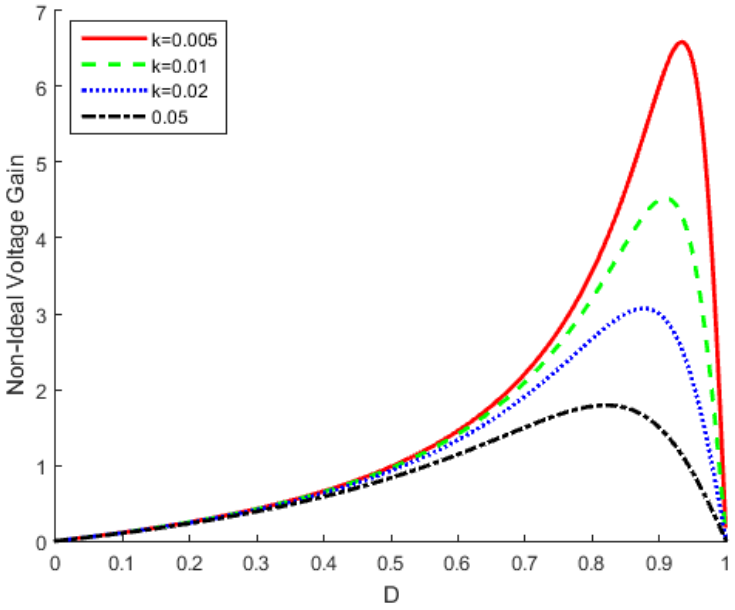

Figure 4.8: Non-ideal flyback converter voltage gain versus duty cycle for different k and transformer turn ration of 1

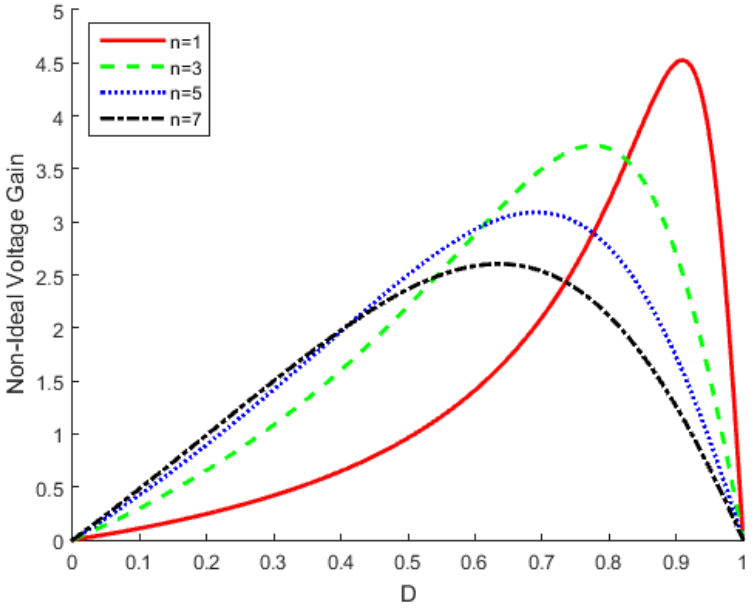

Figure 4.9: Non-ideal flyback converter voltage gain versus duty cycle for different n and k=0.01

the main switch and diode in the reasonable value.

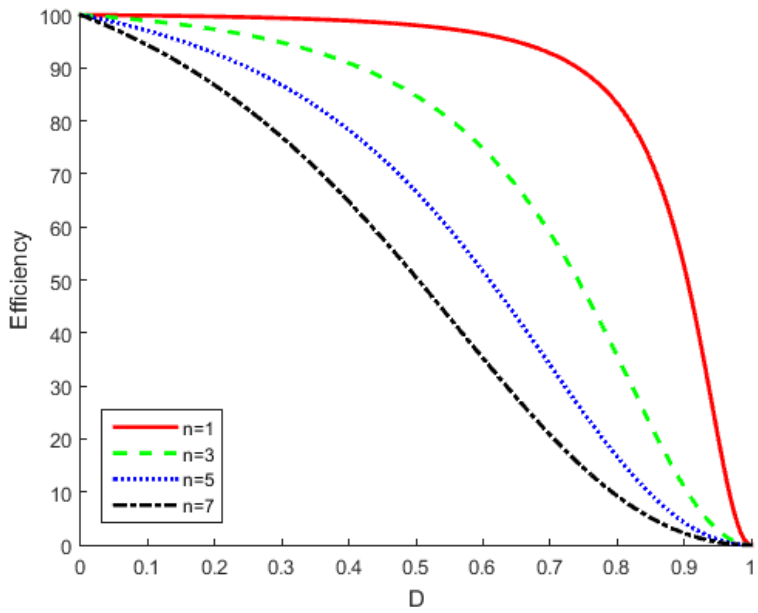

Figure 4.10: Flyback converter efficiency versus duty cycle for k=0.01

Flyback converter has normally the efficiency between 70 to 90 percent. Turn ratio of it's transformer is chosen around 2. As it is shown in figure 4.10, the higher turn ratio, the higher leakage inductance and it leads to less efficiency. That is why it can be used to achieve the gain around 3 with proper efficiency [21]. So for high step-up applications, high turn ratio transformer of flyback converter must be used and it leads to low efficiency.

4.3 Conventional Z-source Converter

Z-source DC-DC converter topology is shown in figure 4.11. It also can not be used practically to achieve voltage gain of 12.5. As it was discussed in section 1, voltage gain ratio of the z-source DC-DC converter can be calculated as :

$$M(D) = \frac{V_O}{V_I} = \frac{1-D}{1-2D} \tag{4.15}$$

As it is shown in figure 4.12, z-source voltage ratio can be infinite for duty cycle close

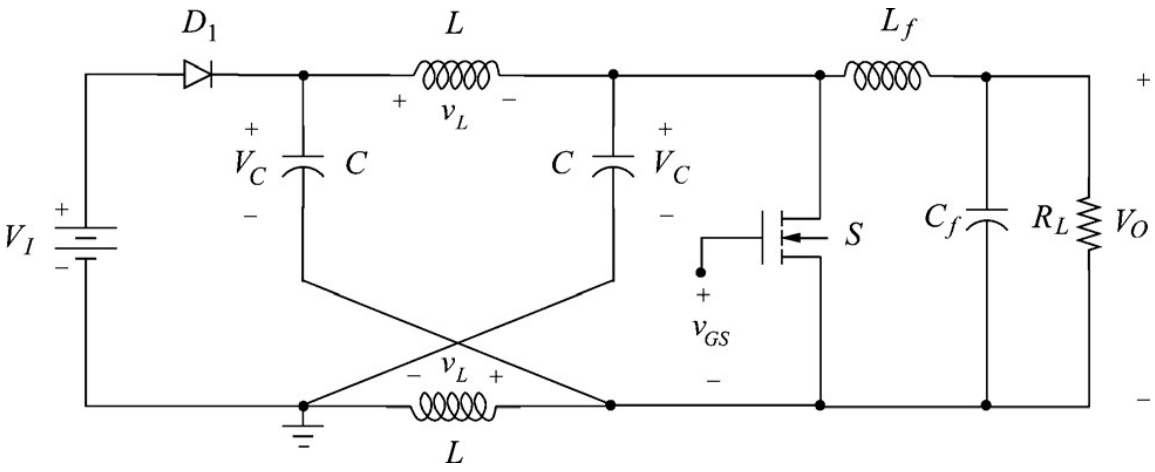

Figure 4.11: Z-source converter topology. [15]

to 0.5 theoretically, however, the high gain can not be achieved in non-ideal z-source converter. A non-ideal z-source dc-dc converter with parasitic components is shown in figure 4.13. To calculate the non-ideal voltage ratio and efficiency, resistance r_L in series with the transformer, to model the resistance of the inductor winding are considered to simplify the calculations. therefore, the non-ideal flyback voltage ratio

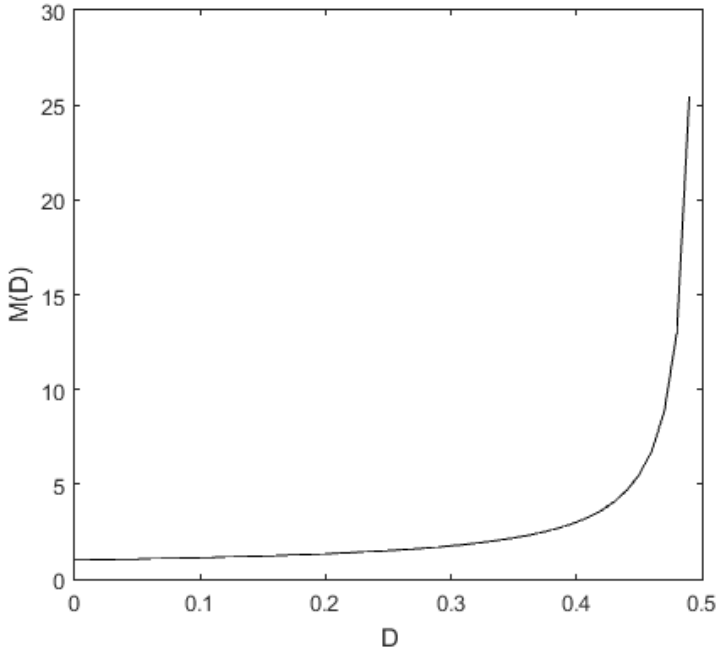

Figure 4.12: Ideal z-source voltage gain VS. duty cycle.

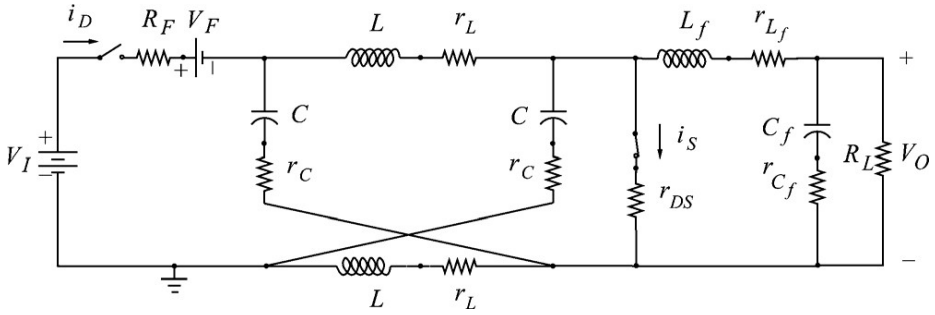

Figure 4.13: Non-deal z-source converter topology. [15]

and efficiency can be calculated by following equations :

$$M_{(non-ideal)} = \frac{V_{out}}{V_{in}} = \frac{1-D}{1-2D} \times \frac{1}{1+\dfrac{2(1-D)r_L}{(1-2D)^2 R_o}} \tag{4.16}$$

The efficiency of the z-source converter can be calculated az following :

$$M_{I(DC)} := \frac{I_o}{I_I} = \frac{(1-2D)}{1-D} \tag{4.17}$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_o I_o}{V_I I_I} = M_{(non-ideal)} \cdot \frac{(1-2D)}{1-D} \tag{4.18}$$

$$\eta = \frac{1}{1 + \frac{2(1-D)r_L}{(1-2D)^2 R_o}} \tag{4.19}$$

$$k := \frac{r_L}{R_o} \tag{4.20}$$

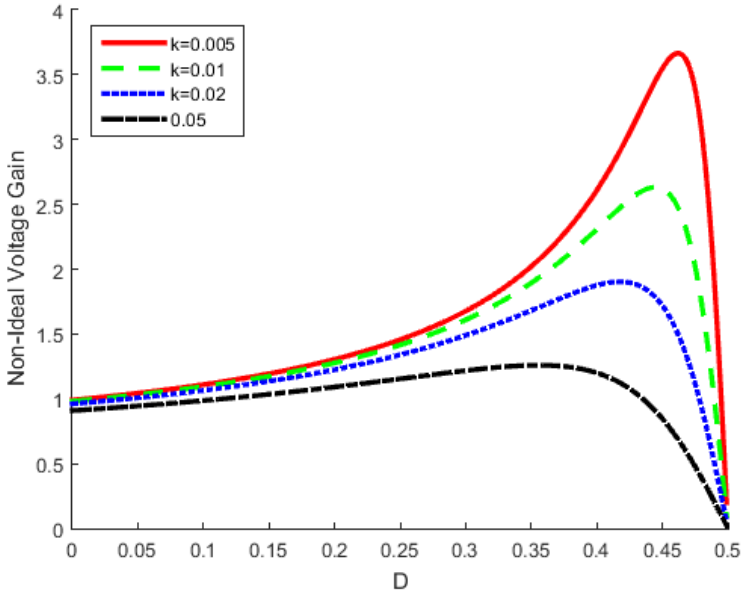

Figure 4.14: Non-deal z-source gain VS. duty cycle for different k

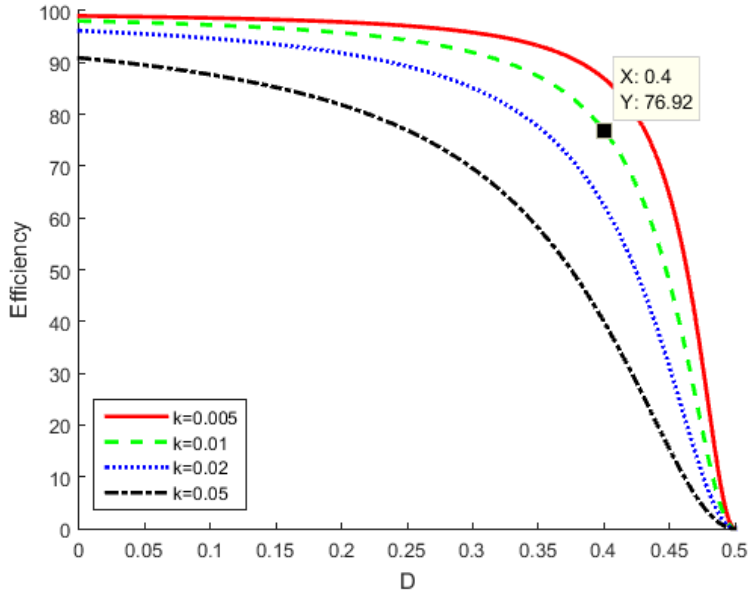

Figure 4.15: Non-deal z-source efficiency VS. duty cycle for different k

As it is shown in figure 4.14, z-source converter maximum gain in limited because of the parasitic components.

Based on figure 4.15, efficiency is decreased greatly for high duty cycles like the conventional boost converter. Therefore z-source converter also can not be used to achieve high voltage gain like 12.5.

4.4 Z-source Based Converter in [14]

Z-source based Isolated converter has been proposed in [14]. This is the last converter that is compared with the other high step up converters in this section. This high step up converter schematic is shown in figure 4.16.

The voltage ratio of this converter can be calculated as :

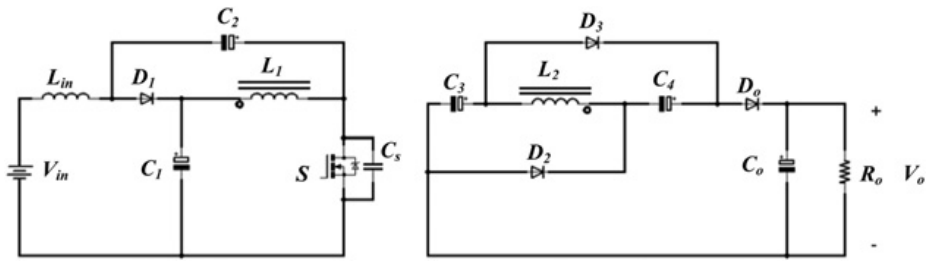

Figure 4.16: Z-source based isolated converter schematic [14]

$$M(D) = \frac{V_o}{V_{in}} = (\frac{1+D}{1-2D})n \tag{4.21}$$

Conversion ratio of coupled inductor is indicated by n. Voltage ratio graph versus duty cycle of the main switch is shown in figure 4.17. The voltage gain theoretically can be infinite, however, parasitic components make limitations for the gain and efficiency. The max duty ratio for this converter is 0.5 .

The stress voltage of the converter diodes are shown in following equations :

$$V_{D0} = V_{D2} = V_{D3} = (\frac{n}{1-2D})V_{in} \tag{4.22}$$

Therefore, diode stress voltages are in direct relationship with coupled inductor turn ration. The other limitation to choose coupled inductor turn ratio is about the leakage inductances.

To calculate the non-ideal voltage gain and efficiency, a parasitic resistance is considered with primary side of coupled inductors, like other converters. So magnetizing

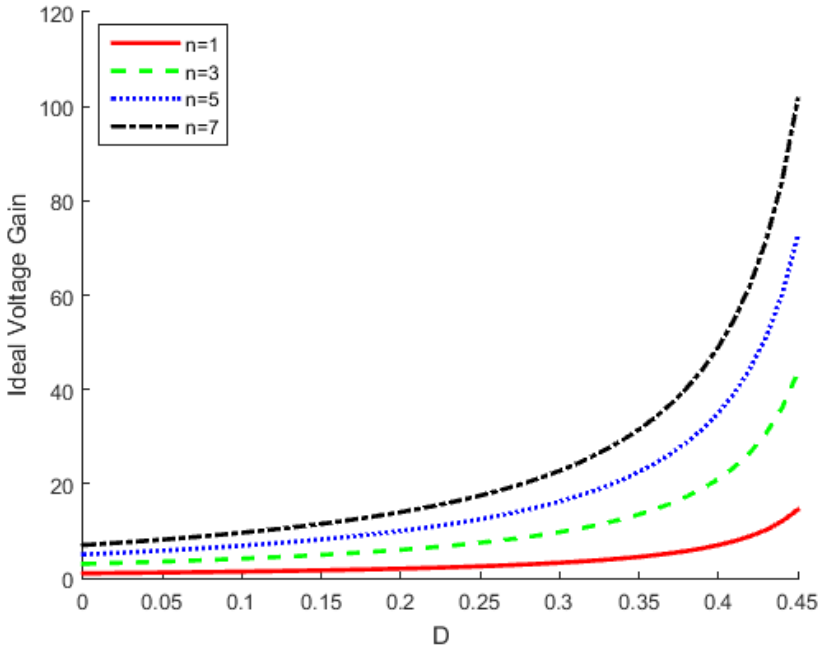

Figure 4.17: Z-source based isolated converter gain graph versus duty cycle

current of coupled inductors can be approximated by :

$$i_{L_m} = \begin{cases} nI_o, & \text{if } 0 < t \leq DT \\ I_I, & \text{if } DT < t \leq T \end{cases} \tag{4.23}$$

$$\begin{aligned} I_{L_{m(rms)}} &= \sqrt{\frac{1}{T}\left(\int_0^{DT} n^2 I_o^2 dt + \int_{DT}^{T} I_I^2 dt\right)} \\ &= I_o\sqrt{n^2 D + M_v^2(1-D)} \end{aligned} \tag{4.24}$$

$$\begin{aligned} P_{r_L} = r_L I_{L_{m(rms)}}^2 &= r_L(n^2 D + M_v^2(1-D))I_o^2 \\ &= r_{L_m}(n^2 D + M_v^2(1-D))\frac{P_o}{R_L} \end{aligned} \tag{4.25}$$

Therefore, non-deal voltage ratio and efficiency of this converter can be expressed by :

$$M_{(non-ideal)} = \frac{V_{out}}{V_{in}} = \frac{n(1+D)}{1-2D} \times \frac{1}{1+\frac{r_L}{R_o}(n^2D + M_V^2(1-D))} \tag{4.26}$$

$$M_V = \frac{n(1+D)}{1-2D} \tag{4.27}$$

$$\eta = \frac{1}{1+\frac{r_L}{R_o}(n^2D + M_V^2(1-D))} \tag{4.28}$$

Non-ideal voltage ratio and efficiency of z-source based converter versus duty ratio are shown in figures.

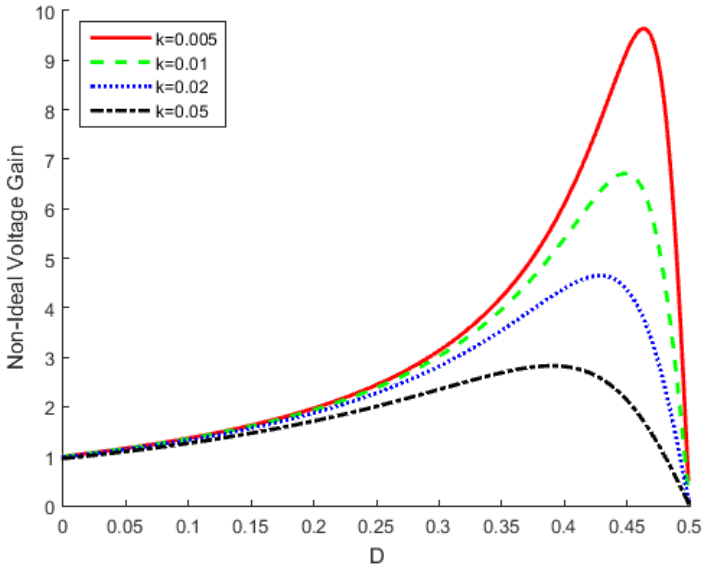

Figure 4.18: Non-ideal z-source based voltage gain VS. duty cycle.

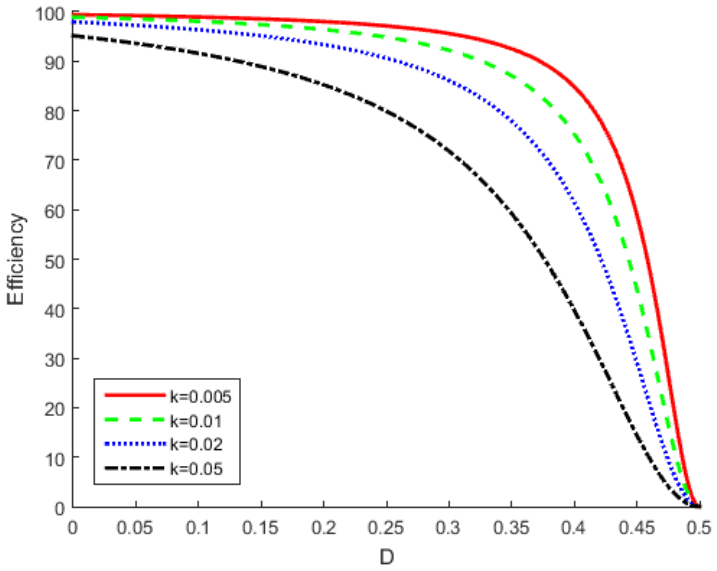

Figure 4.19: Z-source based efficiency VS. duty cycle.

4.5 Proposed Converter

The proposed z-source converter gain ratio is as following :

$$M_v = \frac{V_o}{V_I} = \frac{(2n+1) - D}{1 - 2D} \tag{4.29}$$

As it is shown in figure 4.20, proposed converter voltage ratio can be infinite for duty cycle close to 0.5 theoretically, however, the high gain can not be achieved in the non-ideal converter.

To calculate the non-ideal voltage ratio and efficiency, resistance r_L in series with the transformer, to model the resistance of the inductor winding are considered to simplify the calculations. Therefore, based on 3.67 in chapter (3), the non-ideal proposed converter voltage ratio and efficiency can be calculated by following equations

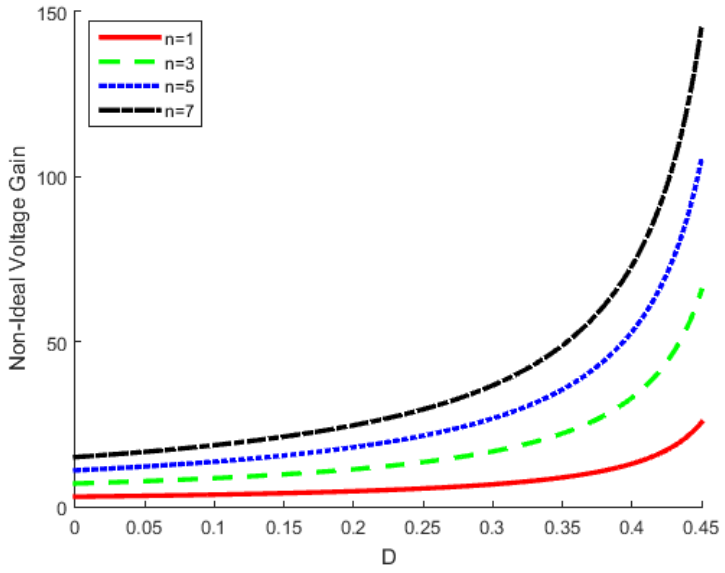

Figure 4.20: Ideal z-source voltage gain VS. duty cycle.

:

$$M_{(non-ideal)} = \frac{V_{out}}{V_{in}} = \frac{(2n+1)-D}{1-2D} \times \frac{1}{1+\frac{r_L}{R_o}(n^2D + M_V^2(1-D))} \tag{4.30}$$

$$M_V = \frac{(2n+1)-D}{1-2D} \tag{4.31}$$

$$\eta = \frac{1}{1+\frac{r_L}{R_o}(n^2D + M_V^2(1-D))} \tag{4.32}$$

As it is shown in figure 4.21, proposed converter maximum gain in limited because of the parasitic components.

Based on figure 4.22, efficiency is decreased for high duty cycles, however, efficiency is reasonable for desired duty cycle. Therefore high gain can be achieved with proper efficiency for the proposed converter.

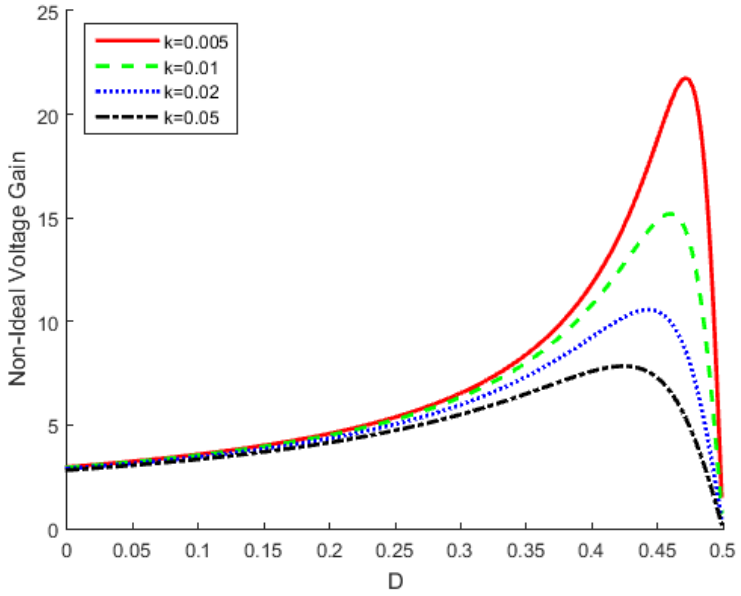

Figure 4.21: Non-deal proposed converter gain VS. duty cycle for different k

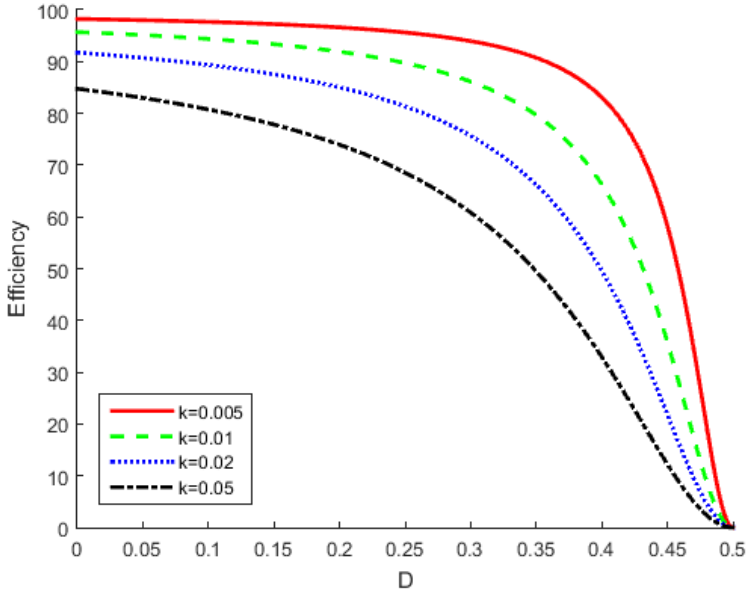

Figure 4.22: Proposed converter efficiency for different k and n=1

The gain comparison versus duty cycle is shown in figure 4.23 for conventional boost converter, flyback converter, conventional z-source converter, z-source based converter in [14] and our proposed converter.

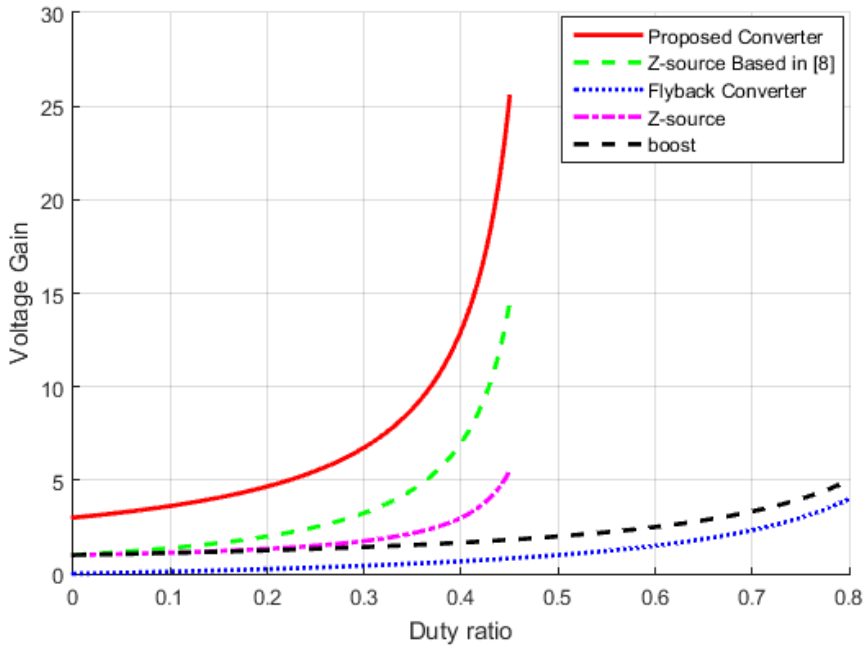

Figure 4.23: Comparison of voltage gain of proposed converter and two other converters for $n = 1$

The comparison of the different single switch converters efficiency versus various output power for the input voltage of 24 V, output voltage of 300 V and gain of 12.5. Moreover, characteristic comparison between single switch power converters are done in table 4.1.

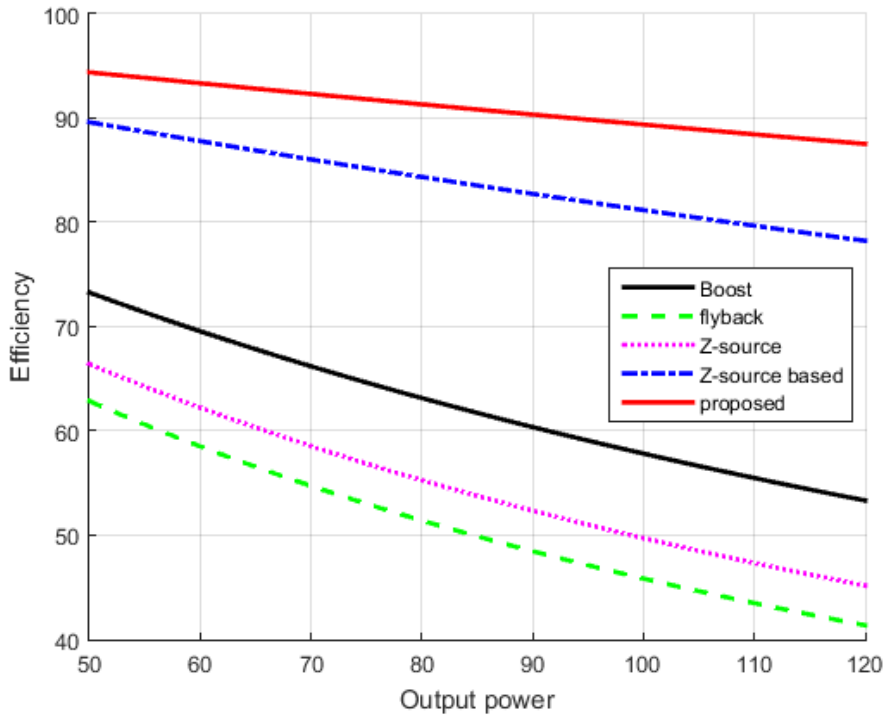

Figure 4.24: Comparison of the different single switch converters efficiency versus various output power for fixed gain

Table 4.1: Comparison between converters with single power switch.

Converter	Voltage Gain	Switch Voltage Stress	Input current	Reverse-recovery problem
conventional boost	$\frac{1}{1-D}$	$\frac{V_{in}}{1-D}$	continuous	large
flyback	$n.\frac{D}{1-D}$	$V_{in}(\frac{D}{1-D}+n)$	discontinuous	large
conventional Z-source	$\frac{1-D}{1-2D}$	$\frac{V_{in}}{1-2D}$	discontinuous	large
Z-source based in [14]	$n.\frac{1+D}{1-2D}$	$\frac{V_{in}}{1-2D}$	continuous	small
proposed converter	$\frac{(2n+1)-D}{1-2D}$	$\frac{V_{in}}{1-2D}$	discontinuous	small

5. CONCLUSION AND FUTURE WORK

In this thesis, a novel high step up z-source dc-dc converter with flyback and voltage multiplier is introduced. Derived equations indicate that voltage gain of conventional z-source converter is increased greatly. The proposed converter eliminates the problem of complexity and great duty cycle in conventional high step up converters. Moreover, low stress voltage, high efficiency and wide range of voltage gain by choosing turn ratio, make it a good candidate for high step up applications, such as boosting low output voltage of solar panels. The main advantages of the proposed converter can be counted as following:

- The converter has high voltage gain without increasing the turn ratio of coupled inductors.
- Four output diodes of the converter turn off under zero current switching (ZCS) and two of them turn on under zero voltage switching (ZVS).
- The reverse recovery problem of output diodes is eliminated.
- High voltage gain can be achieved for the low duty cycle. ($D < 0.5$)
- The semiconductor devices have Low stress voltage(the switch voltage is clamped).

A prototype of the proposed converter is implemented and tested. It is designed to convert 24 V input voltage to 300 V output voltage and 100 W output power. There is good agreement between simulation and experimental results.

Proposing this converter opens new challenges for future work. The potential future works can be listed as :

- Analyzing proposed converter in discontinuous conduction mode(DCM) for applications that such features are required.
- Analyzing proposed converter for high power and high frequency applications.

- Evaluating proposed converter for maximum power point tracking (MPPT) and droop control in micro grid applications.
- Analyzing the proposed z-source converter in inverter mode.

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