LOW-VOLTAGE, LOW-POWER CIRCUITS FOR DATA COMMUNICATION SYSTEMS

A Dissertation

by

MINGDENG CHEN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2003

Major Subject: Electrical Engineering

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Approved as to style and content by:

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ABSTRACT

Low-Voltage, Low-Power Circuits for Data Communication Systems.

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There are growing industrial demands for low-voltage supply and low-power consumption circuits and systems. This is especially true for very high integration level and very large scale integrated (VLSI) mixed-signal chips and system-on-a-chip. It is mainly due to the limited power dissipation within a small area and the costs related to the packaging and thermal management.

In this research work, two low-voltage, low-power integrated circuits used for data communication systems are introduced. The first one is a high performance continuous-time linear phase filter with automatic frequency tuning. The filter can be used in hard disk driver systems and wired communication systems such as 1000Base-T transceivers. A pseudo-differential operational transconductance amplifier (OTA) based on transistors operating in triode region is used to achieve a large linear signal swing with low-voltage supplies. A common-mode (CM) control circuit that combines common-mode feedback (CMFB), common-mode feedforward (CMFF), and adaptive-bias has been proposed.

With a 2.3V single supply, the filter's total harmonic distortion is less than –44dB for a $2V_{PP}$ differential input, which is due to the well controlled CM behavior. The ratio of the root mean square value of the ac signal to the power supply voltage is around 31%, which is much better than previous realizations.

The second integrated circuit includes two LVDS drivers used for high-speed point-to-point links. By removing the stacked switches used in the conventional structures, both LVDS drivers can operate with ultra low-voltage supplies. Although the Double Current Sources (DCS) LVDS driver draws twice minimum static current as required by the signal swing, it is quite simple and achieves very high speed operation. The Switchable Current Sources (SCS) LVDS driver, by dynamically switching the current sources, draws minimum static current and reduces the power consumption by 60% compared to the previously reported LVDS drivers. Both LVDS drivers are compliant to the standards and operate at data rates up to gigabits-per-second.

DEDICATION

To my Parents,

To my brothers and my sisters,

To my dearest wife Ju,

And to my lovely daughter Annie

For their love and support

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I would like to express my sincere appreciation to my advisor, professor Jose Silva-Martinez, for his guidance, support, and encouragement during my studies at Texas A&M University. His creativity and insight into circuit design helped me a lot in my research. His energy and love of what he is doing inspires me a lot. I feel very grateful for his supervision both on the technical and the personal levels during my stay at College Station.

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CHAPTER I

INTRODUCTION

1.1. Low-Voltage, Low-Power Mixed-Signal Circuits and Systems

There are growing industrial demands for low-voltage supply and low-power consumption circuits and systems [1]. From modern portable computers and communication devices to more traditional applications such as medical devices, the need for circuits and systems that operate with smaller supply voltages and consume minimum power is immense and endless. This is specially true for very high integration level and very large scale integrated (VLSI) mixed-signal chips and system-on-a-chip. It is mainly due to the limited power dissipation within a small area and so the costs related to the packaging and thermal management. Also portable applications require to extend the battery life as well.

This trend has forced designers to develop new approaches more amenable to low-voltage and low-power integrated circuits and it poses lots of challenges for all involved: processes, devices, circuits, and system architectures [1]. Low-voltage and low-power electronic systems have been pursued continuously; recently we have been seeing continuous advances in process technologies, in device modeling for computer simulation, in circuit design techniques, and in approaches to system design--all aim at

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This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits*.

the production of electronic systems that operate from very low supply voltages and that dissipate very low power.

In mixed-signal systems, the analog circuits are combined with digital circuits in order to get the best performance with low-voltage supply and low-power consumption. This combination should be in an optimal way and the optimization process is application dependent.

1.2. Types of Filters

Filters are systems that can be used to manipulate the frequency spectrum of signals and they are essential in many different applications. Filters are usually used to get ride of the unwanted noise and reject the surrounding interference. For example, they can be used to band-limit signals and noise in data conversion systems and communication systems; provide magnitude and phase equalization in hard disk driver systems, transmission lines, and cables; select band, reject image, and detect signals in RF communication systems. Figure I.1 shows a simplified 1000Base-T receiver which includes a continuous-time filter. The signal coming from the cable is amplified to a certain level through the variable gain amplifier (VGA). The low-pass continuous-time filter is used to limit signal and noise bandwidth and provide anti-aliasing prior sampling. The analog-to-digital converter (ADC) digitizes the filtered output to take the advantages of the Digital Signal Processing (DSP) unit. The equalizer provides the equalization and the equalized signal goes to the decoder. The gain/timing control module is used to adjust the gain of the VGA. Although we are living in a digital age,

many digital systems interfacing with the real analog world might use continuous-time filters.

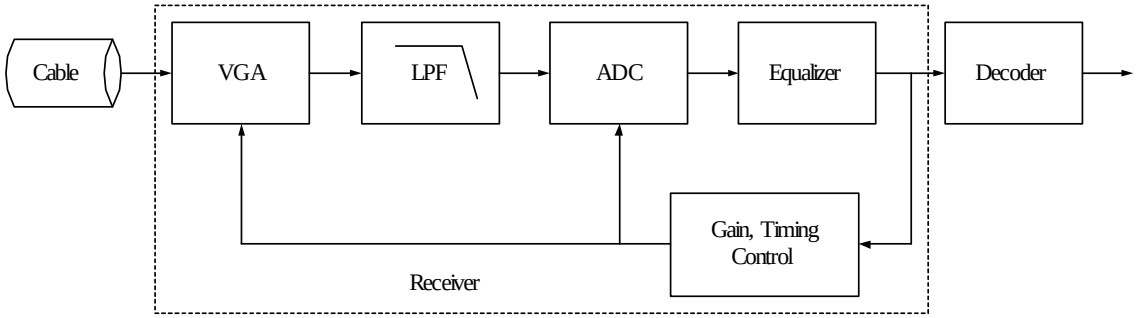

Figure I.1 Simplified 1000Base-T receiver block diagram

There are mainly two types of filters: digital filters and analog filters. While the data samples are discrete for digital filters, analog filters process continuous signals. Analog filters can be further divided into passive filters and active filters. While passive filters comprise passive components only such as resistors, capacitors, and inductors, active filters use active devices such as operational amplifiers (OPAMP) and/or operational transconductance amplifiers (OTA). Active filters can also be classified into Active-RC, Switched-Capacitor (sampled-data filters), OTA-C/Gm-C, and LC filters. Passive filters do not employ amplifiers and usually they are off-chip filters and are not suitable for integrated circuits. Active-RC and Switched-Capacitor filters are suitable for low to medium frequency applications, but they are not suitable for high frequency applications. This is mainly due to the very wide bandwidth and very large unity-gain frequency requirements for the used operational amplifiers. OTA-C/Gm-C filters use the

whole frequency range up to the unity-gain frequency of the operational transconductance amplifiers and they can be used in medium to high frequency systems. But due to the sensitivity to the parasitics and that operational transconductance amplifiers are power hungry for frequencies in the GHz frequency range, OTA-C filters are not suitable for very high frequency systems. For GHz frequency systems, LC filters become feasible because the required values for Ls and Cs are small so that they can be used for IC solutions. Because of the low quality factor of the on-chip inductors, Q-enhancement is usually needed for LC filters.

Another important issue associated with high performance filters is the automatic tuning. Because of the process, supply, and temperature (PVT) variations, the frequency response and the quality factor of the filter deviates from the desired ones; hence efficient and cost effective automatic tuning systems are needed for high performance systems.

1.3. Operational Transconductance Amplifiers (OTAs)

Operational transconductance amplifiers (OTAs) are the key active building blocks of continuous-time filters. They can be generally classified into three types: single-ended, fully-differential (FD), and pseudo-differential (PD) OTAs. Most modern high performance analog integrated circuits make use of fully differential signal paths [2]. With OTAs, this technique results in differential outputs as well as differential inputs; hence they are referred to as fully differential OTAs. Fully differential OTAs are preferred because they provide better dynamic range over their single-ended counter

parts, this is mainly due to their larger signal swing, better distortion performance, and better common-mode noise and supply noise rejection. For symmetrical circuits, the common-mode noise appears in both outputs and can be easily rejected. For example, fully differential structures reject noise from the substrate as well as from pass-transistor switches turning off in switched-capacitor applications. If the circuit is built in a symmetric manner, then ideally the noise will affect both signal paths identically, and will be rejected, since only the difference between signals is of importance. In other words, the noise will not affect the differential signal, which is the signal of interest, since both sides of the differential signals see the same noise. In reality, the rejection only partially occurs since the mechanism introducing the noise are usually nonlinear with respect to voltage levels. One example is the substrate noise, which feeds in through junction capacitors and they are nonlinear. However, the noise rejection of a fully differential design will be much better than that for a single-ended output design.

The main drawback of using fully differential OTAs is that a common-mode feedback (CMFB) circuit must be added. This extra circuit is needed to establish the common-mode output voltage. This CMFB circuit is also used to suppress the common-mode signal components over the whole band of differential operation that tends to saturate the different stages [3]. The design of a good CMFB circuit is nontrivial. The speed of the common-mode path should be comparable to that of the differential path, otherwise the common-mode noise (e.g., power supply noise) may be significantly amplified such that the output signal becomes distorted. Also, the CMFB circuit is often a source of noise injection and increases the load capacitance that needs to be driven.

Regardless of the limitations described above, fully differential OTAs work very well and can substantially improve the system's quality, especially in very unfriendly environments such as mixed-mode applications. However, at lower supply voltages, pseudo-differential operation transconductances could be used to avoid the voltage drop across the tail current source used in the fully differential structures. Removing the tail current source achieves a larger signal swing, but it also results in larger common-mode gain. So it requires to carefully control the common-mode response for pseudo-differential OTAs. In some cases, the CMFB requirements may be relaxed [3]. For example, if the common-mode gain is small, the CMFB speed might be reduced (e.g., for a pseudo-differential OTA with common-mode feedforward, the requirements of the CMFB can be relaxed).

1.4. High Order Filters

Usually a second-order filter can not provide the required selectivity required in many practical systems. So high order filters are necessary to provide enough selectivity. There are three main approaches to achieve high order filters: cascade of biquadratic sections without feedback [4], cascade of biquadratic sections with feedback [5], and LC ladder filter emulation [6].

In the cascade of biquadratic sections approach, high order functions are achieved by the direct connection of second-order biquadratic sections. This method provides the simplicity of the filter design and tuning scheme design. But its disadvantage is that the overall filter transfer function is sensitive to the biquad's parameter variations, which are

caused by the inevitable process, supply voltage, and temperature (PVT) variations. So its sensitivity performance is not good enough.

Cascaded biquadratics with feedback loops are also based on biquadratic sections, but with some negative feedback [7]. This approach provides better overall filter transfer function sensitivity performance compared to the corresponding cascade of biquadratic sections without feedback [8].

There are mainly two methods to emulate LC ladder filters: emulating the LC ladder filter functionally by realizing the currents and node voltages of the ladder [9] or implementing the inductors using active elements. These approaches provide the best sensitivity performance over the cascaded approaches without/with feedback.

1.5. Linear Phase Filter Approximations

Integrated continuous-time filters used for hard disk driver systems and some digital communication systems such as 1000Base-T are good examples for linear phase filters. The primary purpose of this kind of filters is to limit the signal and noise bandwidth. In general, there is no stringent magnitude response requirements in the passband or stopband, but it must have a linear phase or a constant group delay for all signal frequencies to maintain the data integrity. Non-uniform group delay causes phase distortion and leads to detection problems. In practice, a small group delay deviation or a ripple of about 5% is permitted and a filter with an order of 4-7 maybe used.

1.5.1 Bessel-Thomson and Equiripple Linear Phase Filter Approximations

Bessel-Thomson approximation (maximally flat delay) and equiripple delay approximation are the two main filter approximations used for the design of filters with approximately constant group delay [10-11]. For a fourth-order linear phase filter, the normalized frequencies ω_is and Q_is for both Bessel-Thomson and 0.05^o Equiripple linear phase filters are shown in Table I.1 and Table I.2.

Table I.1 4^{th}-order Bessel-Thomason linear phase filter parameters

Filter Section	ω_i, rad/sec	Q_i
Biquad 1	ω_1=1.419	Q_1=0.522
Biquad 2	ω_2=1.591	Q_2=0.806

Table I.2 4^{th}-order 0.05^o equiripple linear phase filter parameters

Filter Section	ω_i, rad/sec	Q_i
Biquad 1	ω_1=1.007	Q_1=0.573
Biquad 2	ω_2=1.599	Q_2=1.148

From Tables I.1 and I.2, we can see that for the Bessel-Thomson filter, the biquad section's Q_is are smaller, and the ω_is are more closely clustered. However, the group delay for the 0.05^o equiripple filter is flat up to $1.5F_c$ vs. $1.0F_c$ for the Bessel-Thomson

filter. Also, equiripple filter has a better selectivity than the Bessel-Thomson filter with the same order.

1.5.2 Gain Boosting and Group Delay Shaping

In addition to the basic functions, some times additional magnitude and group delay shaping functions are added to facilitate the detection process (e.g., read channel filters). Magnitude boost is provided within the appropriate frequency band in order to remove the undesired effect of bit shift due to the influence of the neighboring pulse [12]. This pulse slimming must not distort the group delay. Also in order to compensate for the non-uniform group delay of the components, or simply to provide flexibility in detection, the group delay may be modified in some frequency bands.

These additional requirements of magnitude and group delay shaping are provided by modifying the basic linear phase filters, and the overall transfer function H(s) takes the form

$$H(s) = \frac{N(s)}{D(s)} \tag{1}$$

where D(s) corresponds to the basic, classical linear phase filter transfer function, and N(s) is the added polynomial that incorporates the modifications stated above.

The numerator N(s) provides the magnitude and group delay shaping via two transmission zeroes:

$$N(s) = \left(1 + K_1 \frac{s}{\omega_1} - K_2 \frac{s^2}{\omega_1^2}\right) \tag{2}$$

—If $K_1=0$, and $K_2>0$, then $N(j\omega)=1+K_2\omega^2/\omega_1^2$, and it provides magnitude shaping without affecting the group delay response.

—If $K_1\neq0$, and $K_2=0$, then $N(s)=1+K_1s/\omega_1$, and it provides group delay shaping without affecting the magnitude response significantly.

—If K_1 and K_2 are properly selected, then N(s) might provide two asymmetrical zeroes and it provides both magnitude and group delay shaping. The interaction between the magnitude and group delay is very small—magnitude boost is pronounced at high frequencies around ω_o and group delay shaping is more effective at low frequencies. For all practical purposes, K_1 and K_2 are used to independently program group delay and magnitude shaping.

1.6. Group Delay Sensitivity

A second-order low-pass biquadratic transfer function can be written as

$$H(s)=\frac{\omega_0^2}{s^2+s\cdot\frac{\omega_0}{Q}+\omega_0^2} \tag{3}$$

For real frequencies, s = jω, H(s) can be partitioned into a gain component G(ω) and a phase component Θ(ω) as given by

$$H(j\omega)=G(\omega)\cdot e^{j\Theta(\omega)} \tag{4}$$

The gain sensitivities of the biquad to ω_0 and Q are [13]:

$$S_Q^{G(\omega)} = \left[1 + Q^2\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)^2\right]^{-1} \tag{5}$$

$$S_{\omega_0}^{G(\omega)} = S_Q^{G(\omega)} \cdot \left[1 + 2Q^2\left(\frac{\omega^2}{\omega_0^2} - 1\right)\right] \tag{6}$$

As shown in [14], the group delay sensitivities to ω_0 and Q can be expressed as

$$S_Q^{\tau(\omega)} = -1 + 2 \cdot S_Q^{G(\omega)} \tag{7}$$

$$S_{\omega_0}^{\tau(\omega)} = -3 + \frac{2}{1 + \frac{\omega^2}{\omega_0^2}} + 2 \cdot S_{\omega_0}^{G(\omega)} \tag{8}$$

For a transfer function composed of N second-order low-pass biquads, the group delay variation can be written as

$$\frac{\Delta\tau}{\tau} = \sum_{i=1}^{N}\left(S_{Q_i}^{\tau_i}\frac{\Delta Q_i}{Q_i} + S_{\omega_i}^{\tau_i}\frac{\Delta\omega_i}{\omega_i}\right)\frac{\tau_i}{\tau} \tag{9}$$

Expressions (7)-(9) can be used to find the integrator's specifications such as the DC gain and excess.

For the fourth-order equiripple linear phase filter designed in this dissertation, its transfer function is

$$H(s) = \frac{\omega_1^2}{s^2 + s \cdot \frac{\omega_1}{Q_1} + \omega_1^2} \cdot \frac{\omega_2^2}{s^2 + s \cdot \frac{\omega_2}{Q_2} + \omega_2^2} \tag{10}$$

where ω_1=1.0075, Q_1=0.5734, ω_2=1.5987, and Q_2=1.1481. Figure I.2 and Figure I.3 show the group delay sensitivity functions for the two biquadratic sections. While the group delay sensitivities to both the quality and resonant frequency are less than 1 for the

first biquad, the sensitivity to the resonant frequency for the second biquad is larger than 1. So it is important to minimize the resonant frequency variations to reduce the group delay ripple. In this dissertation, the quality factor Q_i is implemented as the ratio of two scaled operational transconductance and the resonant frequency ω_i is implemented as the ratio of transconductance to capacitance. While the quality factor Q_i is well controlled by the scaling, the resonant ω_i can vary significantly. So an automatic frequency tuning scheme is used to reduce the group delay variations.

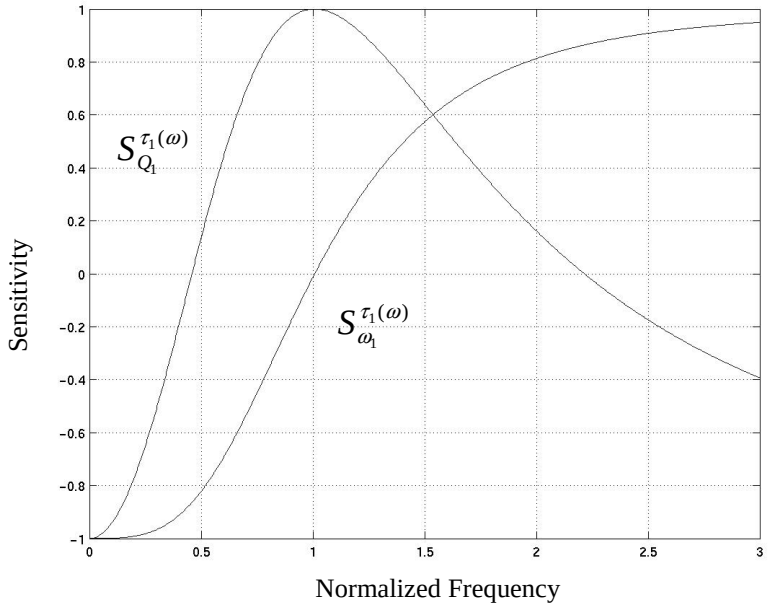

Figure I.2 Group delay sensitivities for the first biquad

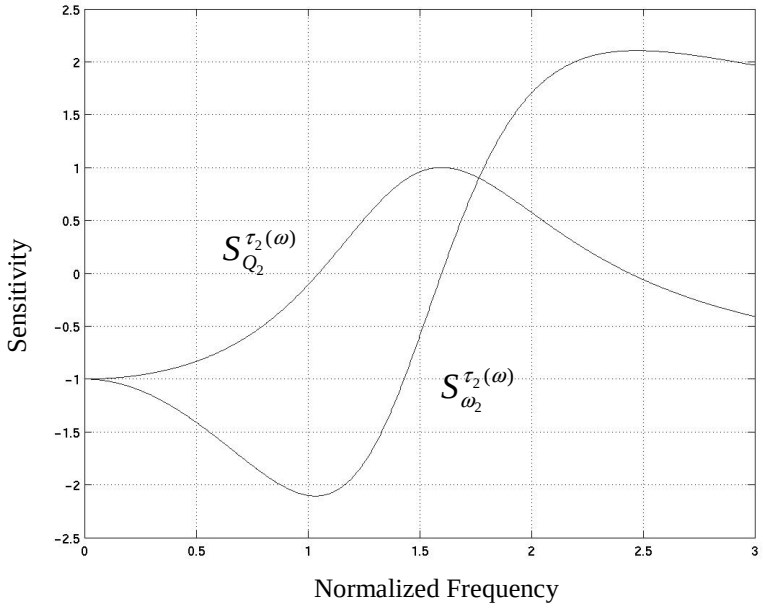

Figure I.3 Group delay sensitivities for the second biquad

1.7. Low-Voltage Differential Signaling (LVDS) Drivers

The ever-increasing processing speed of microprocessor motherboards, optical transmission links, chip-to-chip communications, etc., is pushing the off-chip data rate into the gigabits-per-second range. While scaled CMOS technologies continue to enhance the on-chip operating speeds, off-chip data rates have gained little benefit from the increased silicon integration. This is primarily due to the excessive power consumption necessary for driving impedance-controlled electrical interconnects, which leads to an increase in the costs related to packaging and thermal management [15].

In the past, off-chip high data rates were achieved by massive parallelism, with the disadvantages of increased complexity, excessive pins needed, and increased cost for the

IC package and the printed circuit board (PCB). So it is beneficial to move the off-chip data rate to the range of Gb/s-per-pin or above. Also reducing the power consumption is critical for battery-powered portable systems as well as some other systems in order to extend the battery life and reduce the cost related to packaging and additional cooling systems.

Scalable Coherent Interface (SCI) is a high-speed packet transmission protocol that efficiently provides the functionality of bus-like transactions (read, write, lock, etc.), but it uses a collection of fast point-to-point links instead of physical buses to reach higher speeds. The initial physical implementations are based on emitter coupled logic (ECL) signal levels [16], which consume more power than is practical in the low-cost workstation environment and are inconvenient for some applications.

Low voltage differential signaling (LVDS) is a standardized data transmission format that is widely used for serial data transmissions [17]. It is a technology developed to provide a low-power and low-voltage alternative to ECL and other high-speed I/O interfaces for point-to-point transmissions. LVDS achieves higher speed and significant power savings by means of a differential scheme for transmission and termination, in conjunction with low voltage swing.

1.8. Main Contributions

A low-voltage, low-power, high performance continuous-time linear phase filter with automatic frequency tuning is designed. The optimal design of a pseudo-differential transconductor using transistors operating in triode region is discussed. A common-mode

control circuit that combines CMFB, common-mode feedforward (CMFF), and adaptive-bias has been presented. A large linear signal swing ($2V_{ppd}$) has been achieved due to the well controlled common-mode (CM) behavior. The ratio of the root mean square value of the ac signal to the power supply voltage is around 31%, which is much better than previous realizations.

Two low-voltage, low-power, and high speed LVDS drivers are designed. The Double Current Sources (DCS) LVDS driver is simple and fast, but the drawback is that its static current consumption is as twice as the minimum required by the voltage swing. The Switchable Current Sources (SCS) LVDS driver, by dynamically switching the current sources, draws minimum static current and reduces the power consumption by 60% compared to the previously reported LVDS drivers. While the previous realizations can not operate properly with low-voltage supplies, both the DCS and SCS LVDS drivers are suitable for low-voltage supply applications. The two LVDS drivers are compliant to the standards and can operate at data rates up to gigabits-per-second.

1.9. Organization

Two low-voltage, low-power integrated circuits used for data communication systems are presented in Chapter II and Chapter III, respectively. In each chapter, the background and motivations for each design are introduced first. Following the discussion of the current status of the research on those topics, the new ideas and the circuit designs are presented. The difference among these designs and the previously reported works are pointed out and emphasized. The detailed design issues associated with these designs are also discussed. Some of the simulation results and the silicon experimental results are included to verify the new ideas and designs. Specifically, Chapter II discusses a low-voltage, low-power, high performance continuous-time linear phase filter with automatic frequency tuning. The filter can be used for wired communication systems such as 1000Base-T and hard disk driver systems. Chapter III presents a low-voltage, low-power differential signaling (LVDS) driver, which is used for point-to-point links such as chip-to-chip communications. Finally, Chapter IV draws some conclusions and summarizes the main contributions of this research work.

CHAPTER II

A $2V_{pp}$, 80-200MHZ FOURTH-ORDER CONTINUOUS-TIME LINEAR PHASE FILTER WITH AUTOMATIC FREQUENCY TUNING

2.1. Background and Motivation

The growing demand of portable electronic equipment and system-on-a-chip has been pushing the industry to design efficient circuits for low power supply voltages and low power consumption. In analog/mixed signal processing, fully differential structures are often used due to their better dynamic range (larger signal swing, better distortion performance, and better common-mode noise and supply noise rejection) over single-ended structures. For applications of low power supply voltages and large signal swings, pseudo-differential structures become attractive since they avoid the voltage drop across the tail current source. But inherently pseudo-differential structures have the same low frequency transconductance for both differential and common-mode signals. Therefore, the use of pseudo-differential structures requires a careful and efficient control over the common-mode behavior of the circuits.

Continuous efforts have been made to control the common-mode (CM) behavior of pseudo-differential architectures [18-22]. The common-mode control circuit should not only stabilize the OTA output common-mode voltage, but also reject the input common-mode signals and supply noises. So usually it is not enough to control the CM behavior

of pseudo-differential architectures by using a common-mode feedback (CMFB) only. We also need a common-mode feedforward (CMFF) to suppress CM signals. For tunable filters and other differential systems, an adaptive mechanism is also needed to control the CM behavior over the tuning range. In the standalone CMFF scheme [19], the CM current is partially cancelled at the output stage of the transconductor, but the CM voltage at the output nodes is not always properly controlled. In [20], the authors use a fully-balanced (FB) architecture based on single-ended blocks to suppress the CM components. The efficiency of this approach depends on good matching between two single-ended transconductors which is usually difficult to satisfy, especially for high frequency applications. Both CMFB and CMFF were used in [21]. The cancellation of the CM components relies on good matching among the triode transistors in the Gm cell, CMFB, and CMFF. It also relies on good matching among several transistors (the current sources and the current mirrors). In [22], an adaptive-bias mechanism to improve the stability of the CM voltage over the tuning range is proposed; its efficiency depends on the performance of the CMFB only.

In a 1000Base-T receiver, a continuous-time low-pass filter is needed to limit the signal and noise bandwidth and provide anti-aliasing prior to sampling. The main specifications of this filter for the original project are:

- The THD must be less than –40dB for a $2V_{ppd}$ input signal;
- The bandwidth of the filter is tunable from 45MHz to 105MHz;
- Single 1.8V supply;
- The process is 0.18μm CMOS.

The most challenging specification is the large linear signal swing. Since we do not have access to the 0.18μm CMOS process, we used 0.35μm CMOS process and a single 2.3V supply. Later on, we also modified the bandwidth requirements to that the tunable range of the filter is from 80MHz to 200MHz, with a nominal bandwidth of 150MHz in order that this filter can also be used for other higher speed applications. This filter can also be used for hard-disk read channel systems.

2.2. Pseudo-differential OTAs and Their Characteristics

The topology of a generic fully-differential transconductor is shown in Figure II.1a [19]. While M1 and M2 are shown as simple NMOS transistors here, they can represent arbitrary unilateral active devices with transconductance of G_m. The input signal can be expressed as

$$v_i^+ = v_{icm} + \frac{v_{id}}{2} \tag{1a}$$

$$v_i^- = v_{icm} - \frac{v_{id}}{2} \tag{1b}$$

where v_{icm} is the input common-mode signal, and v_{id} is the input differential signal. In the fully-differential configuration, the rejection of the common-mode signal is achieved by the large output impedance Z_p ($Z_p=R_p||C_p$) of the tail current source, especially at relatively low frequencies.

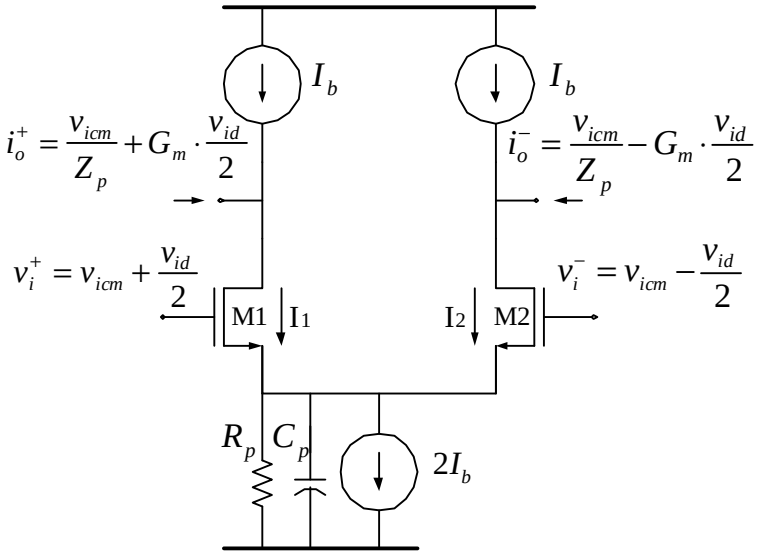

Figure II.1a Fully-differential structure

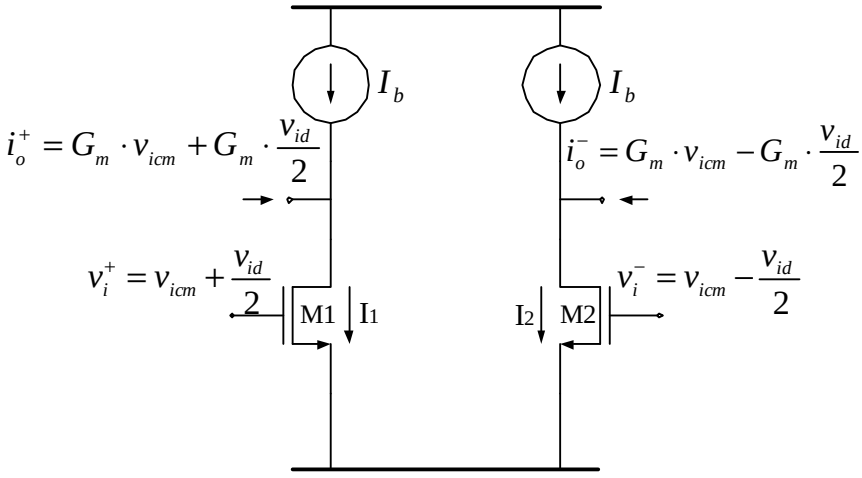

Figure II.1b Pseudo-differential structure

At lower supply voltages, a pseudo-differential architecture, Figure II.1b, could be used to avoid the voltage drop across the tail current source. This solution usually

achieves a larger signal swing, but it requires to carefully control its response to common-mode signals. Actually, for this circuit, the transconductance for the input common-mode signal is exactly equal to that for the differential input signal.

Besides the large common-mode gain, we also need to consider another important characteristics for transconductors: linearity.

The pseudo-differential transconductor shown in Figure II.1b can be seen as a combination of two parallel single-ended branches. If we consider the non-linear voltage-to-current conversion, the drain currents of transistors M1 and M2 (I_1 and I_2) can be generally expressed as

$$I_1 = I_b + \alpha_1\left(v_i^+\right) + \alpha_2\left(v_i^+\right)^2 + \alpha_3\left(v_i^+\right)^3 \tag{2a}$$

$$I_1 = I_b + \alpha_1\left(v_i^-\right) + \alpha_2\left(v_i^-\right)^2 + \alpha_3\left(v_i^-\right)^3 \tag{2b}$$

where I_b is the bias current, and ν_i^+ and ν_i^- are the input signals as expressed in equations (1a) and (1b). α_1, α_2, and α_3 are the coefficients of the polynomial, where α_2 and α_3 are used to represent the OTA non-lineariiesy. Notice that higher order harmonics (greater than third-order) are neglected here.

The output differential current ($i_{o,PD}$) for the pseudo-differential structures can then be calculated as

$$i_{o,PD} = \alpha_1 v_{id} + 2\alpha_2 v_{id} v_{icm} + \alpha_3 (3 v_{id} v_{icm}^2 + v_{id}^2 / 4) \tag{3a}$$

If the same expression is derived for the fully-differential structure (I_1+I_2 = constant), the output differential current ($i_{o,FD}$) is

$$i_{o,FD} = \alpha_1 v_{id} - \left(\alpha_2^2 / \alpha_1 - \alpha_3 / 4 \right) v_{id}^3 \quad (3b)$$

Comparing the expressions for the two output differential currents, we have the following observations:

- The pseudo-differential structure presents additional distortion terms which arises from the common-mode signal. In particular, even-order terms can appear in a perfectly symmetrical structure due to the product of the differential and common-mode signals (which is not the case for fully-differential structures).

To minimize the importance of this effect, when using a pseudo-differential structure, the transconductance must be designed to be as linear as possible. Also the common-mode signal must be minimized, i.e., a strong and efficient common-mode control circuit is needed for pseudo-differential structures. As a consequence, the combination of common-mode feedforward (CMFF) and common-mode feedback (CMFB) is essential for high performance systems based on pseudo-differential structures.

2.3. Common-Mode Control Techniques for Pseudo-Differential OTAs

2.3.1 Pseudo-Differential OTAs with Common-Mode Feedforward

As discussed in section 2.2., strong and efficient common-mode control circuits are needed for high performance systems based on pseudo-differential structures. A common-mode feedforward scheme was first proposed in [19]. Its basic idea is to use

some transconductor to detect the input common-mode signal, convert it into current, mirror the current to the main transconductor, and partially cancel the input common-mode signal. The configuration of the idea with simple CMOS implementation is shown in Figure II.2.

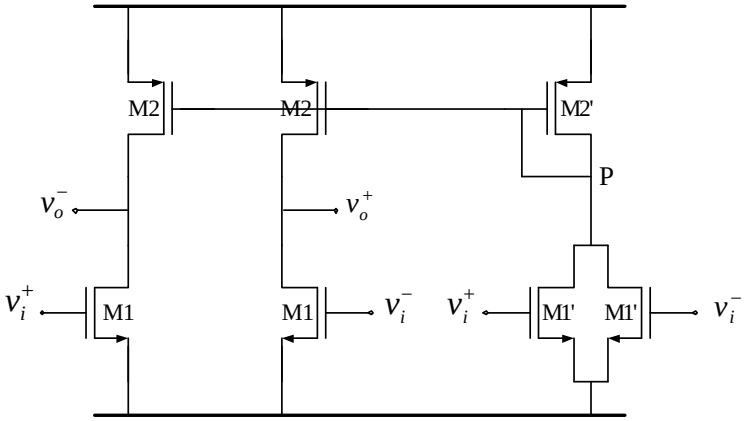

Figure II.2 Common-mode feedforward scheme

Transistors M1 and M2 are the core of the transconductor. Transistors M1' have the half dimensions as M1 and they are used to detect the input common-mode signal and convert it into common-mode current. This current flows through transistor M2' and it is mirrored into the main transconductor. This current cancels the common-mode current generated by transistors M1 and reduces the common-mode gain. In particular, the current flowing into the output nodes of the transconductor can be expressed as

$$i_{ocm} = g_{m1} v_{icm} - g_{m1} v_{icm} \cdot \frac{g_{m2}}{g_{m2} + g_{o1} + g_{o2} + sC_p}$$

$$= v_{icm} \cdot \frac{g_{m1}(g_{o1} + g_{o2} + sC_p)}{g_{m2} + g_{o1} + g_{o2} + sC_p} \tag{4}$$

where C_p is the parasitic capacitance associated with the mirroring node P. The common-mode gain is

$$A_{CM} \equiv \frac{v_{ocm}}{v_{icm}} = \frac{g_{m1}(g_{o1} + g_{o2} + sC_p)}{g_{m2} + g_{o1} + g_{o2} + sC_p} \cdot \frac{1}{g_{o1} + g_{o2}} \tag{5}$$

At DC, it can be seen from (4) that the output common-mode current i_{ocm} is non-zero, which is caused by the finite output transconductance of the transistors. The DC common-mode gain is approximated by

$$A_{CM}(0) = \frac{g_{m1}}{g_{m2} + g_{o1} + g_{o2}} \approx 1 \tag{6}$$

Equation (6) says that the common-mode feedforward reduces the low frequency common-mode gain to approximately 1. At very high frequencies, the common-mode gain is approximated by

$$A_{CM}(\infty) = \frac{g_{m1}}{g_{o1} + g_{o2}} >> 1 \tag{7}$$

which means that the CMFF does not work well at very high frequencies. At high frequencies, the mirroring node P is AC grounded and the common-mode feedforward path is disabled.

While the CMFF scheme reduces the common-mode gain, it does not set the output common-mode voltage. Lossy-integrators can be used to control the output common-mode voltages. In fact, a pseudo-differential transconductor closed in negative feedback

creates a low impedance node for both the differential and common-mode signals. Also CMFF schemes add loads to the driving stages.

2.3.2 Fully-Balanced Transconductor Based on Single-Ended OTAs

Figure II.3 shows a balanced transconductor [23] based on two singled-ended (SE) OTAs. For each of the SE OTA, its common-mode gain is also given by equation (5). The SE OTA subtracts the common-mode components from M1 and cancels them out at the output, while it sums the differential-mode component at the output. Therefore, SE transconductor inherently has a small common-mode gain and a large differential gain.

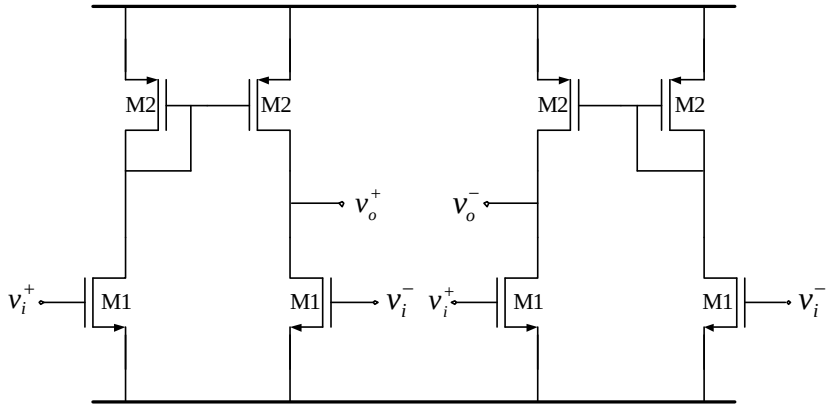

Figure II.3 Balanced transconductor based on single-ended OTAs

In the balanced transconductor based on SE OTAs, the output common-mode voltage is not defined and it depends on the input common-mode signal (common-mode gain is 1 at low frequencies). So a common-mode feedback is necessary to fix the proper operating point. Since the common-mode gain is small (approximately 1), the CMFB

circuit does not require a wide bandwidth; therefore, the CMFB circuit does not consume much power.

A fully balanced CMOS transconductor was proposed in [20]. The conceptual implementation is shown in Figure II.4. This fully-balanced transconductor uses two single-ended transconductors with same transconductance. Besides taking advantage of the small common-mode gain of SE transconductors, this fully-balanced configuration also includes the function of common-mode feedback. Specifically, the current corresponding to the common-mode output voltage (CM current) is produced by adding each current corresponding to each output voltage. Then, the CM current is compared with the current corresponding to the output common-mode reference voltage V_{cm}, and the difference is fed to both the plus and minus outputs. The current-mode addition and subtraction are realized by current mirrors. The multi-inputs can be realized by connecting transistors in parallel to input transistors.

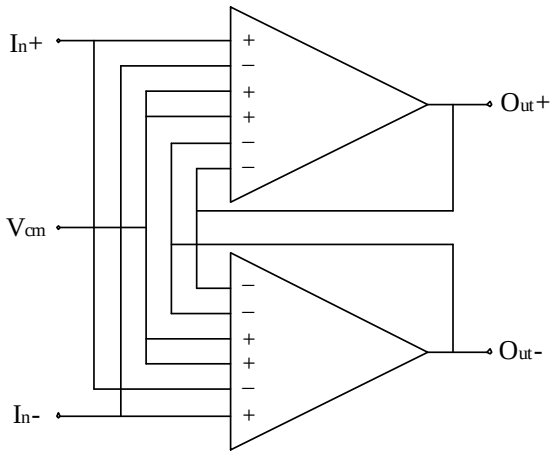

Figure II.4 Fully-balanced configuration using two multi-inputs single-ended transconductors

Although fully-balanced architectures include the functions of both CMFF and CMFB, they need good matching between the two single-ended transconductors, which is not easy to achieve, especially for high frequency systems.

2.3.3 Common-Mode Control Circuit Using Both CMFF and CMFB

As reported in [21], a common-mode control circuit based on CMFF scheme combines CMFF and CMFB. A simplified CMOS version is used here for explanation. The transconductor with the CM control is shown in Figure II.5. Transistors M1 and M2 compose the main transconductor. The right most part of the transconductor is the CMFF circuit, while the left most part of the main transconductor is the CMFB circuit. An assumption is made here that transistors M1 and M1' are working in triode region. Transistors M1' have the half dimensions as M1. The CMFF used here is very similar to the one shown in Figure II.2, except that a common-mode reference current I_{CM} is added. The left side CMFB is the same as the CMFF, with the exception that the gates of transistors M1' are connected to the outputs of the main transconductor.

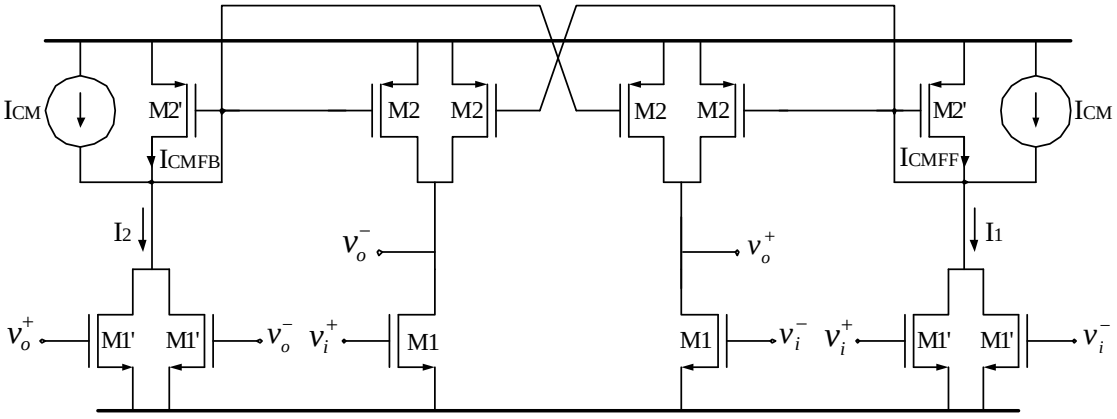

Figure II.5 Pseudo-differential transconductor with CMFF and CMFB

The common-mode reference current I_{CM} shown in Figure II.5 is defined as follows

$$I_{CM} = \frac{\beta}{2}\left[V_{CM} - V_T - \frac{1}{2}V_{DS}\right]V_{DS} \tag{8}$$

where V_{CM} is the reference common-mode voltage and it is generated by a bias circuit. The currents I_1 and I_2 generated by the CMFF and CMFB circuits can be expressed as

$$I_1 = I_{CMFF} + I_{CM} = \beta\left[V_{icm} - V_T - \frac{1}{2}V_{DS}\right]V_{DS} \tag{9}$$

$$I_2 = I_{CMFB} + I_{CM} = \beta\left[V_{ocm} - V_T - \frac{1}{2}V_{DS}\right]V_{DS} \tag{10}$$

Currents I_{CMFF} and I_{CMFB} generated respectively by the CMFF and CMFB are fed back into the main transconductor via two PMOS devices, resulting the following bias current

$$\begin{aligned} I_B &= I_{CMFF} + I_{CMFB} \\ &= \beta\left[V_{icm} - V_T - \frac{1}{2}V_{DS}\right]V_{DS} + \beta V_{DS}\left(V_{ocm} - V_{CM}\right) \end{aligned} \tag{11}$$

where the first term corresponds to the current required to reject the input CM signal and the second term corresponds to the current used to set the transconductor output CM voltage V_{ocm} to CM reference voltage V_{CM}.

The advantage of this CM control scheme is that it combines the CMFF and CMFB together. The disadvantages are that the CMFF and CMFB are correlated (both use I_{CM}, both use the same transistors as the input transistors, etc); It needs good match among many components (M1 and M1', M2 and M2', two I_{CM}), which is difficult to satisfy, especially for high frequency systems. The CMFB gain is fixed by the input transistors M1' and their transconductance is relatively small since they are working in triode region. Also, the CM reference current I_{CM} needs to be generated.

2.3.4 Adaptive Biasing for Tunable Transconductors

For tunable transconductors, it is desirable to control the output common-mode voltage to a fixed value over the whole tuning range in order not to degrade the transconductor's dynamic range. This issue becomes more critical for low-voltage applications, since the voltage swings are inherently constrained to small headroom voltages.

Figure II.6 shows a typical tunable transconductor with CMFB. Assume that under nominal conditions, the tail current source M5 sinks $2I_B$, the PMOS active load M3(M4) sources I_B. Also assume that the output common-mode voltage V_{ocm} equals the output CM reference voltage $V_{o,ref}$, and the common-mode control voltage is V_{cmfb}. Suppose during tuning, the tail current source M5 needs to sink $2(I_B+\Delta I_B)$. Then the top active load M3(M4) needs to source $I_B+\Delta I_B$, and the CMFB control voltage can be denoted as

$V_{cmfb}+\Delta V_{cmfb}$. Since the amplifier's gain is finite, the output CM voltage V_{ocm} is no longer equal to $V_{o,ref}$, i.e., the tuning forces the output CM voltage V_{ocm} to deviate from the CM reference voltage $V_{o,ref}$.

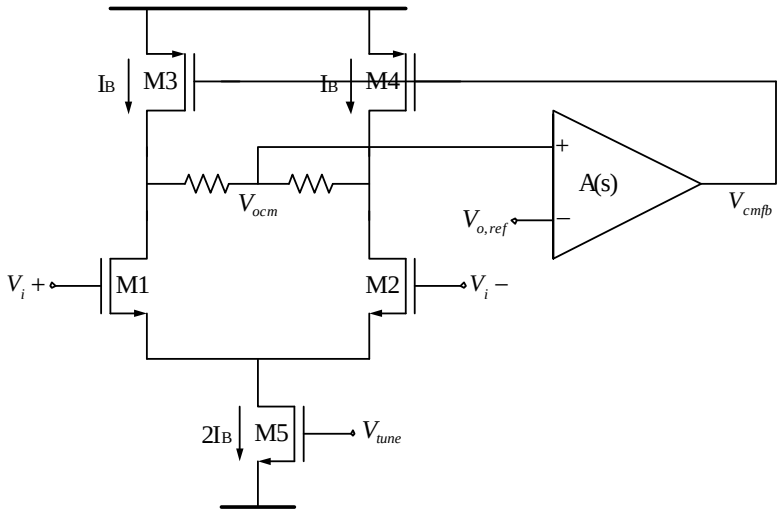

Figure II.6 Tunable transconductor with CMFB

An adaptive CMFB is proposed in [22]. This adaptive CMFB eliminates meaningful deviations of the CM voltage over transconductance tuning by delivering to the transconductor load an adaptive current. The adaptive current is produced by a tuning voltage dependent bias generator and it is mirrored to the tail current of the CMFB. The CMFB adjusts the transconductor active load current so that the output common-mode voltage remains the same over the tuning range. The pseudo-differential transconductor adopted in that paper uses only CMFB to control its CM behavior. So the CM control efficiency dependent on the CMFB only.

2.4. Pseudo-Differential Transconductor

From section 2.1, it can be seen that the most challenging specification of the filter is the very large linear signal swing. It is well known that a transistor working in triode region has a linear transconductance if its drain-source voltage is constant. Using the simple MOS transistor model, the drain current of a NMOS transistor working in triode region can be expressed as

$$i_D = \beta[(v_{GS} - V_{TN})v_{DS} - \frac{1}{2}v_{DS}^2] \quad (12)$$

where $\beta=\mu_n C_{ox}(W/L)$ and V_{TN} are the transconductance parameter and the threshold voltage, respectively. Assuming the drain-source voltage v_{DS} is constant, then the transistor has a linear transconductance and it is given by βv_{DS}. Also as discussed in section 1.3, a pseudo-differential OTA achieves larger signal swings than a fully-differential OTA by removing the tail current source. So a pseudo-differential OTA based on transistors operating in triode region is used for the filter design and it is shown in Figure II.7 [24]. Transistors M1 operate in triode region and they convert the voltage into current in a linear fashion. Transistors M2 and amplifier amp form a regulated-gain-control (RGC) loop and they are used to fix the drain voltage of M1. M3 and M4 are the cascoded active load of the OTA. M2, M3, and M4 are working in saturation region. The tuning voltage V_{TUNE} is used to adjust the OTA's transconductance. Assuming the amplifier amp is ideal and its gain is infinite, then we have both a constant drain-source voltage $v_{DS1}=V_{TUNE}$ independent of the input voltage level, and a linear transconductance given by βV_{TUNE}.

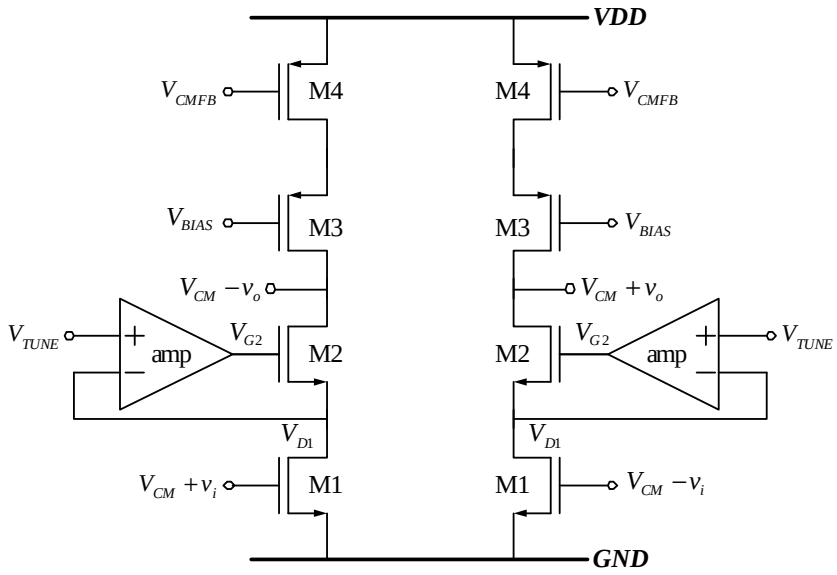

Figure II.7 Pseudo-differential OTA

In order to get the best OTA linearity performance, there are several design issues need to be addressed properly. First, we need to determine the common-mode voltage properly to maximize the linear range. Second, we need to optimize the design of the RGC amplifier amp so that M1's drain voltage is fixed well and its transconductance is linear, even at high frequencies. Also we need investigate the short channel effects of the input transistors M1 to have a good trade off between linearity performance and frequency response.

2.4.1 Optimizing the Linear Range

Let's consider a single branch and determine the CM voltage V_{CM} that maximizes the OTA linear input range. Assume that the power supply is V_{DD}. Let us denote the gate

voltage of M2 by V_{G2}, the gate voltage of M1 by V_{CM}-ν_i, and the output voltage by V_{CM}+ν_o, where V_{CM} is the CM reference voltage, where ν_i and ν_o are the input and output AC signals, respectively.

Since transistor M1 must operate in triode region for better linearity, then

$$V_{CM} - \nu_{i,\max} - V_{TN} > V_{TUNE} \tag{13}$$

where $\nu_{i,max}$ is the maximum amplitude of the input signal.

Also, transistor M3 must operate in saturation region, then

$$V_{CM} + \nu_{o,\max} < V_{BIAS} + |V_{TP}| \tag{14}$$

where $\nu_{o,max}$ is the maximum amplitude of the output signal.

In order to maximize the signal swing, we need to select the bias voltage V_{BIAS} such that the source-drain voltage of M4 is a bit larger than $|V_{DSAT4}|$. Assume we also have to support V_{DSAT3}(=V_{DSAT4}) for the source-drain voltage of M3, then equation (14) yields:

$$V_{CM} + \nu_{o,\max} < V_{DD} - 2|V_{DSAT4}| \tag{15}$$

From the filter transfer function (which will be discussed in section 2.6.), it can be seen that the signal swing at all of the filter's nodes are always equal or less than the input signal swing. So we can assume that the OTA's maximum input signal equals the maximum output signal; i.e. $\nu_{i,max}$=$\nu_{o,max}$. According to (13) and (15), the maximum input signal can be obtained as:

$$\nu_{i,\max} = \frac{1}{2}(V_{DD} - V_{TN} - V_{TUNE}) - |V_{DSAT4}| \tag{16}$$

where V_{TUNE} is obtained from the required filter bandwidth and the transconductance of the OTA.

As a result of this, the common-mode voltage that maximizes the linear signal range is given by:

$$V_{CM} = V_{DD} - v_{i,\max} - 2\left|V_{DSAT\,4}\right| \tag{17}$$

For a supply voltage of 2.3V, a threshold voltage V_{TN} of 0.6V, an overdriving voltage V_{DSAT} of 0.2V, and a tuning voltage V_{TUNE} of 0.2V, the maximum input voltage $v_{i,max}$ is 0.55V and the common-mode voltage V_{CM} which maximizes the linear signal swing is 1.35V.

2.4.2 Regulated Gain Control (RGC) Loop

The design of the RGC loop is critical for the OTA's linearity performance. One of the main sources of OTA's non-linearity is the low gain of the RGC loop at high frequencies, since smaller RGC loop gain leads to larger v_{DS1} variations, leading to larger harmonic distortion components. Figure II.8 is a simplified configuration used to evaluate the OTA performance. Capacitor C_L has a large capacitance, and it grounds the output for AC signals.

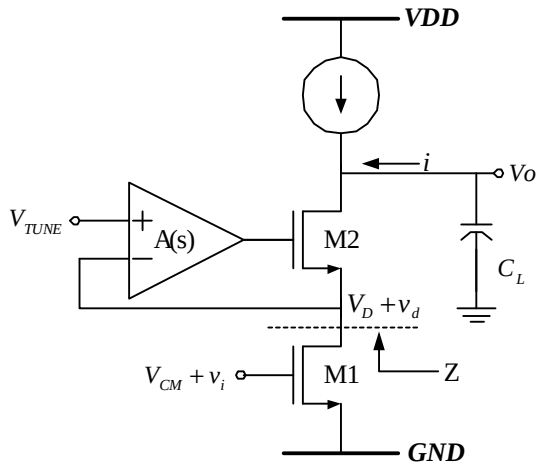

Figure II.8 Configuration for evaluating OTA transconductance

According to equation (12), and neglecting the second-order term $v_d^2/2$, it can be shown that the AC current across the capacitor C_L can be expressed as:

$$i \cong \beta[V_D v_i + v_d v_i + (V_{CM} - V_{TN})v_d - V_D v_d] \tag{18}$$

Using typical small signal analysis, the impedance looking into the RGC from the drain of M1 is approximated by an impedance $Z \cong 1/((A(s)+1)g_{m2})$, where A(s) is the gain of the RGC amplifier. Using $v_d \cong -iZ$, equation (18) leads to:

$$i = \frac{V_D v_i}{1/\beta + Z[(V_{CM} - V_{TN}) - V_D] + Z v_i} \tag{19}$$

And using Taylor series expansion with respect to v_i, then we have:

$$i = \alpha_1 v_i + \alpha_2 v_i^2 + \alpha_3 v_i^3 + \cdots \tag{20}$$

where $\alpha_1 = \dfrac{\beta V_D}{1 + \beta Z(V_{CM} - V_{TN} - V_D)}$,

$$\alpha_2 = \frac{\beta^2 Z V_D}{[1+\beta Z(V_{CM} - V_{TN} - V_D)]^2},$$
$$\alpha_3 = \frac{\beta^3 Z^2 V_D}{[1+\beta Z(V_{CM} - V_{TN} - V_D)]^3}, \ldots$$

Neglecting the higher order terms, the third-order harmonic distortion can be expressed as:

$$HD3 \cong \frac{V_i^2}{4} \cdot \frac{\beta^2 Z^2}{[1+\beta Z(V_{CM} - V_{TN} - V_D)]^2}$$
$$= \frac{V_i^2}{4} \cdot \frac{\beta^2}{[(A(s)+1)g_{m2} + \beta(V_{CM} - V_{TN} - V_D)]^2} \quad (21)$$

where V_i is the magnitude of the input signal, and A(s) is the RGC amplifier gain. The above expression shows the relationship between $(A(s)+1)g_{m2}$ and the third-order harmonic distortion. Figure II.9 shows the OTA's THD simulation results and the theoretical HD3 predicted by (21). When the amplifier's gain is small (e.g., A(s)<6), the OTA's THD is dominated by $(A(s)+1)g_{m2}$ and the theoretical values are close to the simulated ones; but with large amplifier's gain, the OTA's THD is limited by the short-channel effects (which will be discussed in the next section). It can be seen that in order to achieve THD figures around –50dB, the RGC amplifier's gain should be greater than 10V/V over the whole passband of the filter. Note that the non-zero impedance Z causes OTA transconductance reduction, which is clear from the expression of α_1.

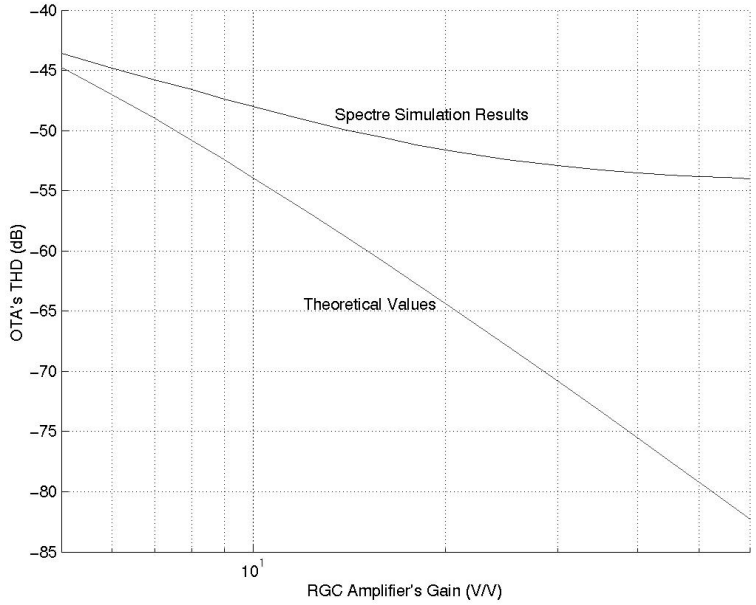

Figure II.9 OTA's THD vs. RGC amplifier's gain (L_{M1}=0.6μm)

Another important issue is the RGC loop stability, which has been already discussed in [25]. The implementation of the RGC amplifier is shown in Figure II.10. It is composed of a single-ended amplifier and two source followers. The source follower M2 shifts up M1's drain voltage ν_{DS1}, giving more room to the OTA's input stage and increasing the transconductance tuning range. The reason that we use two source followers is that we can have a clear idea about M1's drain voltage during the testing. The designed amplifier amp has a low-frequency gain of 31dB, a unity-gain frequency of 1.25GHz with a phase margin of 68^o, and a current consumption is 540μA.

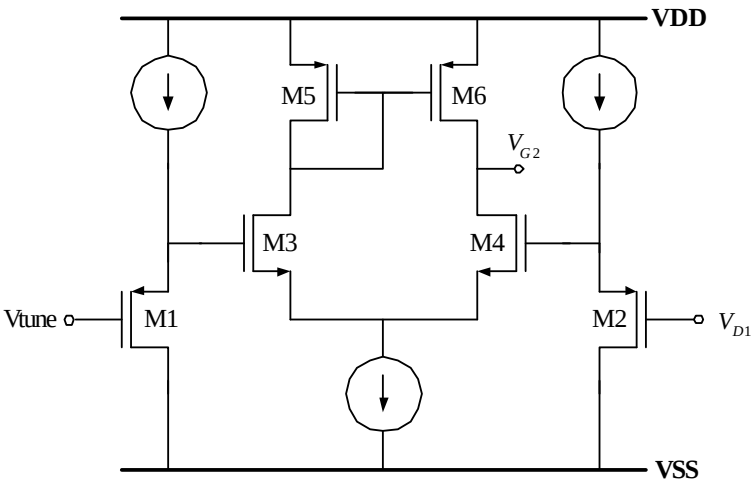

Figure II.10 RGC amplifier

2.4.3 Short-Channel Effects

Short-channel effects affect the OTA's linearity as well. For short channel devices, the effective carrier mobility (μ_{eff}) is a function of both lateral and vertical electric fields [26], and it can be expressed as:

$$\mu_{eff} = \mu_0 \cdot \frac{1}{1+\theta\left(V_{GS}+v_{gs}-V_T\right)} \cdot \frac{1}{1+\frac{1}{LE_c}\left(V_{DS}+v_{ds}\right)} \tag{22}$$

where μ_0 is the low electric field mobility, E_c is the critical electric field, and θ is a fitting parameter which is inversely proportional to the oxide thickness.

From equations (12) and (22), if the lateral electric field effect is fixed by the RGC loop, which fixes the drain-source voltage v_{DS}, the effective carrier mobility μ_{eff} should be independent of transistor length L, and so the OTA's linearity should be independent of the transistor length L.

In fact, according to higher order models [27], the above expression is only a simplified approximation for the drain-source current equation used by the Spice model. It can not predict the OTA's linearity versus the transistor length.

In [27], a more complex drain-source current model is used, and it is expressed as

$$I_{DS} = \frac{I_{DS,0}}{1+\frac{R_{DS} I_{DS,0}}{V_{DS,eff}}}\left(1+\frac{V_{DS}-V_{DS,eff}}{V_A}\right)\cdot\left(1+\frac{V_{DS}-V_{DS,eff}}{V_{A,SCBE}}\right) \tag{23}$$

where

$$I_{DS,0} = \frac{W_{eff} u_{eff} C_{ox}^{'} V_{GST,eff}}{L_{eff}\left[1+V_{DS,eff}/\left(\varepsilon_{sat} L_{eff}\right)\right]}\left[1-\frac{A_{bulk} V_{DS,eff}}{2\left(V_{GST,eff}+2kT/q\right)}\right]V_{DS,eff} \tag{24}$$

$$V_{GST,eff} = \frac{2nkT/q \ln\left[1+\exp\left(\frac{V_{GS,eff}-V_T}{2nkT/q}\right)\right]}{1+2n\frac{C_{ox}^{'}}{C_{dep,0}^{'}}\exp\left(-\frac{V_{GS,eff}-V_T-2\cdot VOFF}{2nkT/q}\right)} \tag{25}$$

$$V_{GS,eff} = V_{GS} - V_{poly,eff} \tag{26}$$

$$V_{poly,eff} = 1.12 - \frac{1}{2}\left(1.12 - V_{poly} - \delta + \sqrt{\left(1.12 - V_{poly} - \delta\right)^2 + 4\cdot\delta\cdot 1.12}\right) \tag{27}$$

$$V_{poly} = \frac{q\in_s NGATEC_{ox}^{'\,2}\cdot 10^6}{2}\left[\sqrt{1+\frac{2\left(V_{GS}-V_{FB}-2\phi_f\right)}{q\in_s NGATEC_{ox}^{'\,2}\cdot 10^6}}-1\right]^2 \tag{28}$$

$$\begin{aligned} V_T = {} & V_{TH0} + \delta_{NP}\left(\Delta V_{T,body\_effect} - \Delta V_{T,charge\_sharing} - \Delta V_{T,DIBL}\right. \\ & \left. + \Delta V_{T,reverse\_short\_channel} + \Delta V_{T,narrow\_width} + \Delta V_{T,small\_size}\right) \end{aligned} \tag{29}$$

$$\Delta V_{T,charge\_sharing} = DVTO\cdot$$

$$\left[\exp\left(-DVT1\frac{L_{eff}}{2L_t}\right)+2\exp\left(-DVT1\frac{L_{eff}}{L_t}\right)\right]\left(V_{bi}-2\phi_f\right) \tag{30}$$

$$\Delta V_{T,small\_size} = DVT0W \cdot$$

$$\left[\exp\left(-DVT1W\frac{W_{eff}L_{eff}}{2L_{tw}}\right)+2\exp\left(-DVT1W\frac{W_{eff}L_{eff}}{L_{tw}}\right)\right]\left(V_{bi}-2\phi_f\right) \tag{31}$$

It can be seen that $V_{GST,eff}$ is a function of $V_{GS,eff}$ and V_T; where V_T is a nonlinear function of L_{eff}. Also, $V_{DS,eff}$, R_{DS}, A_{bulk}, V_A, etc., all depend on $V_{GST,eff}$.

So it is too complicated to get a simple expression for the OTA linearity as function of the transistor length. So it is realistic here to refer to the simulation results.

In order to see the transistor length's effect on the OTA's linearity, we assume that the RGC amplifier has an infinite gain and we keep W/L constant for the input transistors M1. The simulation results for the OTA's THD versus the input transistor's length L are shown in Figure II.11 and they are summarized in Table II.1.

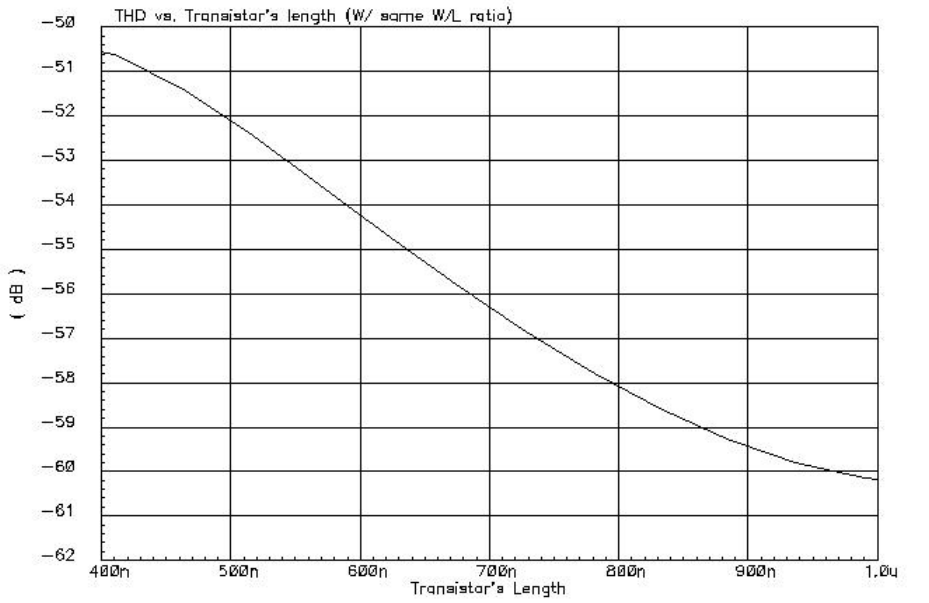

Figure II.11 OTA's THD vs. input transistor M1's length L

Table II.1 OTA's THD vs. input transistor length L ($V_{in} = 2V_{ppd}$)

Transistor Length L (μm)	0.4	0.6	0.8	1.0
OTA's THD (dB)	-50.6	-54.3	-58.2	-60.2

So we choose a transistor length of 0.6μm so that the OTA's THD is about –50dB with the actual RGC amplifier, in order to meet the filter's linearity specifications.

All of the issues discussed above have been considered in the OTA's design. The OTA has a low frequency gain of 31dB and an excess phase of -4.6^{o} at a unity-gain frequency of 150MHz. The OTA transistor dimensions and bias currents are summarized in Table II.2.

Table II.2 OTA transistor dimensions and bias conditions

Transistor	M1	M2	M3	M4	M5	M6	M7
W/L($\mu m/\mu m$)	40/0.6	48/0.4	240/0.4	320/0.4	36/0.4	36/0.6	24/0.6
$I_{bias}(mA)$	1.08	1.08	1.08	1.08	0.18	0.18	0.18

2.5. Common-Mode Control Circuits

The OTA shown in Figure II.7 requires a proper common-mode control system. It should not only stabilize the OTA output CM voltage, but also reject the input CM signals and supply noise. So the combination of a CMFB and a CMFF for the CM control is essential for high performance systems with pseudo-differential architectures. Due to the benefits of the CMFF, the loop gain and bandwidth requirements of the CMFB can be relaxed. Conventional CM control circuits for pseudo-differential structures with CMFB and/or CMFF are shown in Figure II.12a. In order to simplify the design of pseudo-differential architectures, it is more efficient to have a CM control circuit that combines CMFB and CMFF together as shown in Figure II.12b. A CM control system with this feature is used here.

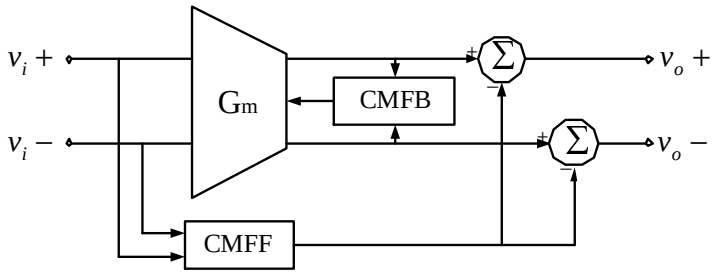

Figure II.12a Conventional CM control using separate CMFB and CMFF

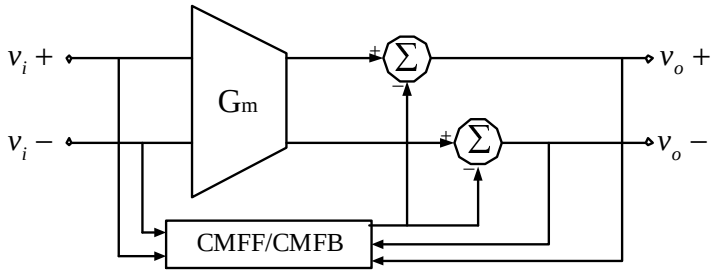

Figure II.12b Proposed CM control that combines CMFB and CMFF

2.5.1 Common-Mode Control Principle

The basic idea of the proposed CM control circuit is that the circuit senses the input CM information as well as the output CM information, then it combines both signals together to control the OTA's CM behavior. The implementation of the CM control is shown in Figure II.13.

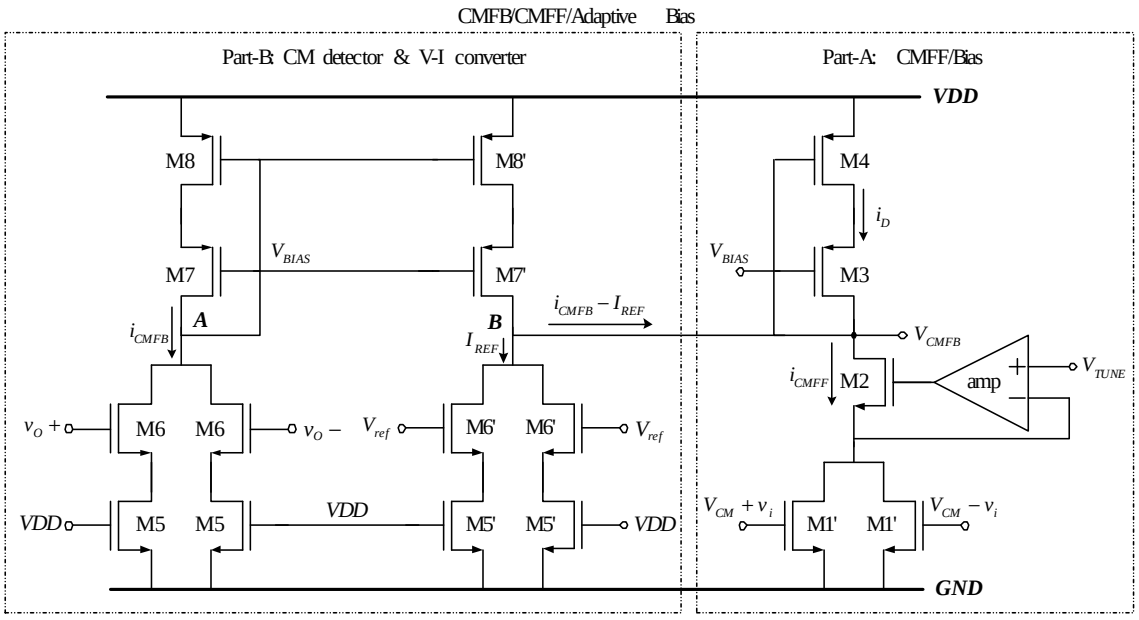

Figure II.13 Common-mode control circuit

The CM control circuit contains two parts. *Part-A* is a CMFF and an adaptive bias circuit. *Part-B* is a CM detector and V-I converter. The combination of the two parts functions as a CMFB, a CMFF, and an adaptive-bias scheme. In *Part-A*, the CMFF/Bias is a replica of a single branch of the OTA except that the dimensions of M1' are one half of the main OTA's input transistor (M1 in Figure II.7). Transistors M1' are connected to the inputs of the OTA and they are used to cancel the CM input signal. The CMFF current is:

$$i_{CMFF} = I_{CMFF} + 2g_{m1}^{'} v_{icm} = I_{CMFF} + g_{m1} v_{icm} \tag{32}$$

where I_{CMFF} is the ideal DC bias current with zero input CM signal, and v_{icm} is the CM input signal. In *Part-B*, transistors M6 and M6' are driven by OTA outputs and the CM reference voltage, respectively. Transistors M5 and M5' are working in deep triode region, their gates are connected to V_{DD}, and they operate in a source degeneration configuration in order to improve the linearity of the CMFB. These circuits compare the output CM voltage with the reference CM voltage and convert the voltage difference into the CMFB correcting current.

$$i_{cmfb} \equiv i_{CMFB} - I_{REF} \cong \frac{2g_{m6} v_{ocm}}{1 + g_{m6} R_5} \tag{33}$$

where R_5 is the effective drain-source resistance of M_5, see Figure II.14. It is assumed that M5=M5' and M6=M6'. Both of the CMFB correcting current i_{cmfb} and CMFF curent i_{CMFF} are then fed into transistors M3 and M4 to control the OTA outputs. The overall current mirrored to the OTA output is:

$$i_D = I_{CMFF} + 2g_{m1}^{'} v_{icm} - \frac{2g_{m6} v_{ocm}}{1 + g_{m6} R_5} \tag{34}$$

where I_{CMFF} provides the adaptive DC current, $2g'_{m1}v_{icm}$ provides the CMFF correcting current, and $2g_{m6}v_{ocm}/(1+g_{m6}R_5)$ provides the current for the action of CMFB. Equation (34) clearly shows why the transistors M1' have to be one half of the main OTA's input transistors. The CM control fixes the common-mode issues but it is transparent to differential signals, and so it does not affect the integrator's differential signal operation.

2.5.2 Common-Mode Control Frequency Response

In order to get some insight in the CMFB loop frequency response, a simplified integrator with the CMFB is shown in Figure II.14.

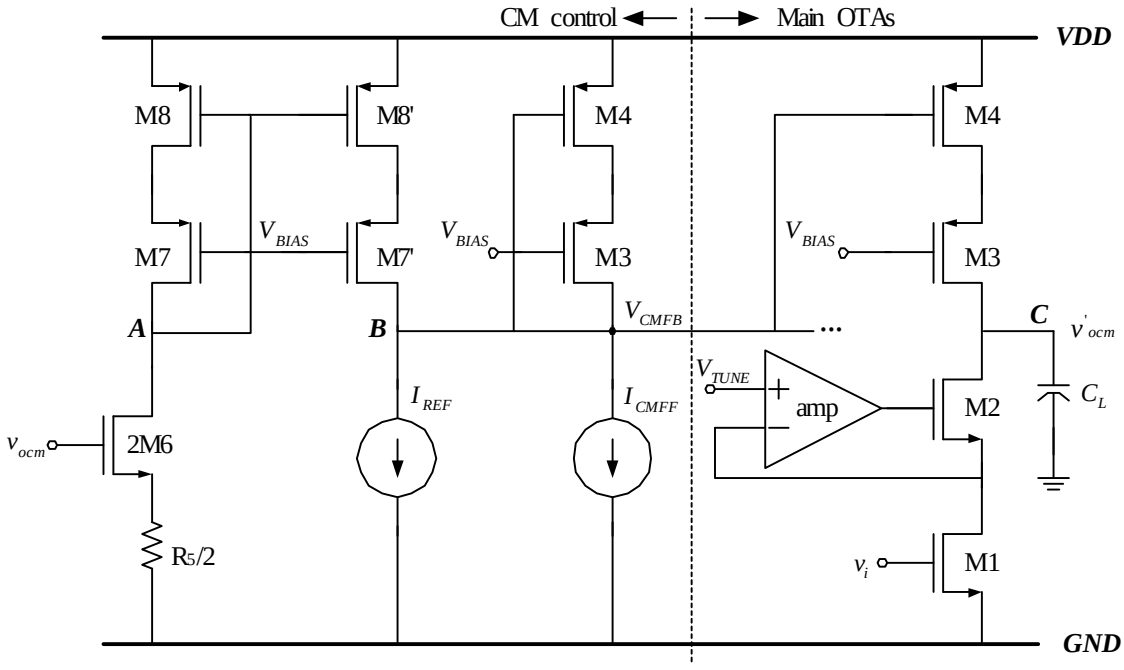

Figure II.14 Simplified CMFB loop equivalent circuit

If we neglect the pole-zero pair produced by the source degeneration composed by $2M_6$ and $R_5/2$, and we also neglect the parasitic poles produced by the cascode transistors, then there are three main poles in the CMFB loop at nodes *A*, *B*, and *C*. For M8=M8' and M4=M4', the CM loop gain $A_{CMFB}(s)$ is approximated by:

$$A_{CMFB}(s) = \frac{v'_{ocm}}{v_{ocm}} \cong \frac{2g_{m6}}{(1+g_{m6}R_5)(g_{m8}+sC_A)} \cdot \frac{g_{m8}}{g_{m4}+sC_B} \cdot \frac{g_{m4}}{g_{oc}+sC_C}$$

$$= \left(\frac{2g_{m6}}{(1+g_{m6}R_5)g_{oc}} \right) \left[\frac{1}{\left(1+s\frac{C_A}{g_{m8}}\right)\left(1+s\frac{C_B}{g_{m4}}\right)\left(1+s\frac{C_C}{g_{oc}}\right)} \right] \tag{35}$$

where $g_{oc} \cong 2(g_{o3}g_{o4}/g_{m3}+g_{o1}g_{o2}/(Ag_{m2}))$ is the output conductance at node *C*; C_A, C_B, C_c are the total capacitance at the nodes *A*, *B*, and *C*, respectively. The factor "2" comes from the fact that the OTA has two identical branches. The CMFB open loop DC gain is $A_{DC}=2g_{m6}/((1+g_{m6}R_5)g_{oc})$, the dominant pole is at $\omega_d=g_{oc}/C_c$, and the non-dominant poles are located at $\omega_{nd1}=g_{m4}/C_B$ and $\omega_{nd2}=g_{m8}/C_A$. To insure enough phase margin in the CMFB loop, the frequencies of the non-dominant poles must be greater than two times that of the gain-bandwidth product ($=4g_{m6}/((1+g_{m6}R_5)C_c)$). The load capacitor C_L is chosen to be 0.9pF. Under this conditions, the unity-gain frequency of the integrator equals the filter's second biquad resonant frequency, which represents the filter's integrator largest unity-gain frequency and it represents the worst case for the common-mode loop stability. The simulated CMFB open loop phase margin is 68 degrees at the unity-gain frequency of 160MHz. Applying a CM current step of 50μA at the OTA outputs, the CM voltage settles properly within 4 nsecs. An overshot of 10mV without

ringing was observed for all simulations. The DC offset produced by the 50μA common-mode current is less than 50mV. This CMFB closed loop CM step response is shown in Figure II.15.

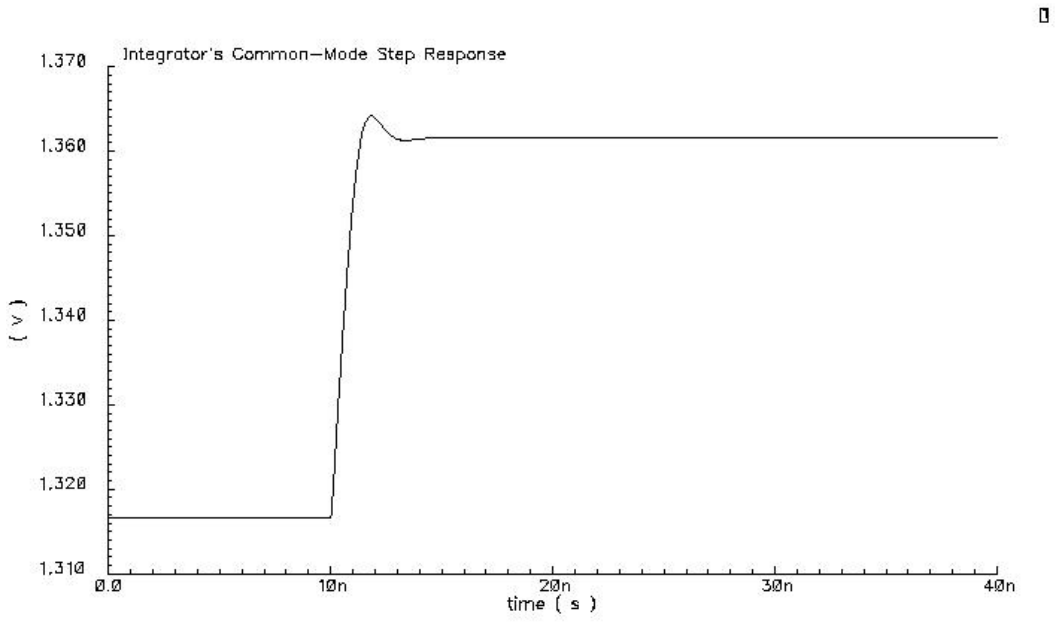

Figure II.15 CMFB closed loop CM step response with a CM current step of 50μA

2.5.3 A Fast Common-Mode Control Circuit

As shown in Figure II.14, the output CM correcting current is combined with the input CM correcting current at node *B*. Then the combination of these two correcting currents is mirrored to the main OTA. Although this CM control circuit (with CMFF, CMFB, and adaptive-biasing) works well for this filter design, there are two non-

dominant poles at node *A* and node *B* in the CMFB loop, which may cause stability problems for faster systems. So it is good to reduce the number of non-dominant poles in the CM loop.

A potential solution to reduce the number of non-dominant pole is to inject the CMFB correcting current directly into the main OTA, eliminating the non-dominant pole at node *B* which is produced by the combination. The conceptual schematic of this solution with one branch of the main OTA is shown in Figure II.16. This schematic contains two parts: the right part is one branch of the main OTA, while the left part is the CM control circuit. The CM control circuit contains a CMFF branch and two CMFB branches, but only one of the two branches is shown in the figure. The output CM reference current I_{REF} is generated outside of the CM control circuit once and it can be mirrored to multiple CMFB branches. Transistor M_{CM} and source-degeneration resistor R_{CM} are used to detect the output CM voltage and convert it into CM current i_{CMFB}. The difference of the output CM reference current I_{REF} and the output CM current i_{CMFB} is then injected into one of the two main OTA branches and it is used to control the output CM voltage. The branch composed by M3, M4 and input CM current i_{CMFF} is the CMFF part of the CM control circuit. It is the same as the one shown in Figure II.13. It can be seen that there is one dominant pole in the CMFB loop (at node *B*) and one non-dominant pole (at node *A*). Notice that R_{CM} operates as a source degeneration resistor that linearizes the CMFB. On top of that, it introduces a high frequency zero that improves even further CMFB loop phase margin. This CM control circuit can be used for faster systems.

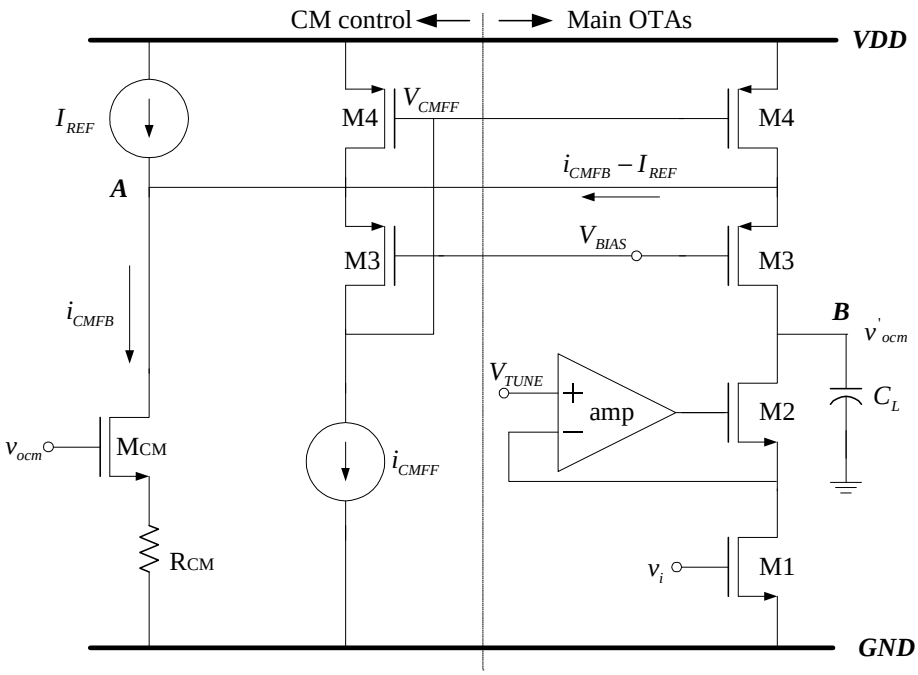

Figure II.16 Conceptual schematic of a faster common-mode control circuit

The implementation of the CM control is shown in Figure II.17. This CM control circuit contains two parts: *Part-A* is the CMFF and adaptive bias part; *Part-B* is the output CM detector and V-I converter. Reference voltage V_{REF} is generated outside of the CM control circuit once and it is used by multiple CMFB branches so that the output CM reference current I_{REF} can be mirrored to the top PMOS current sources in the CMFB branches. The CM correcting currents i_{CMFB}-I_{REF} are injected into the sources of the cascode PMOS transistors M3 in the main OTA two branches, respectively, as shown in the right part of Figure II.16. The CMFF current i_{CMFF} is converted into voltage V_{CMFF} and it is connected to the gates of the PMOS current sources in the main OTA so that the CMFF correcting current can be. mirrored to the main OTA branches.

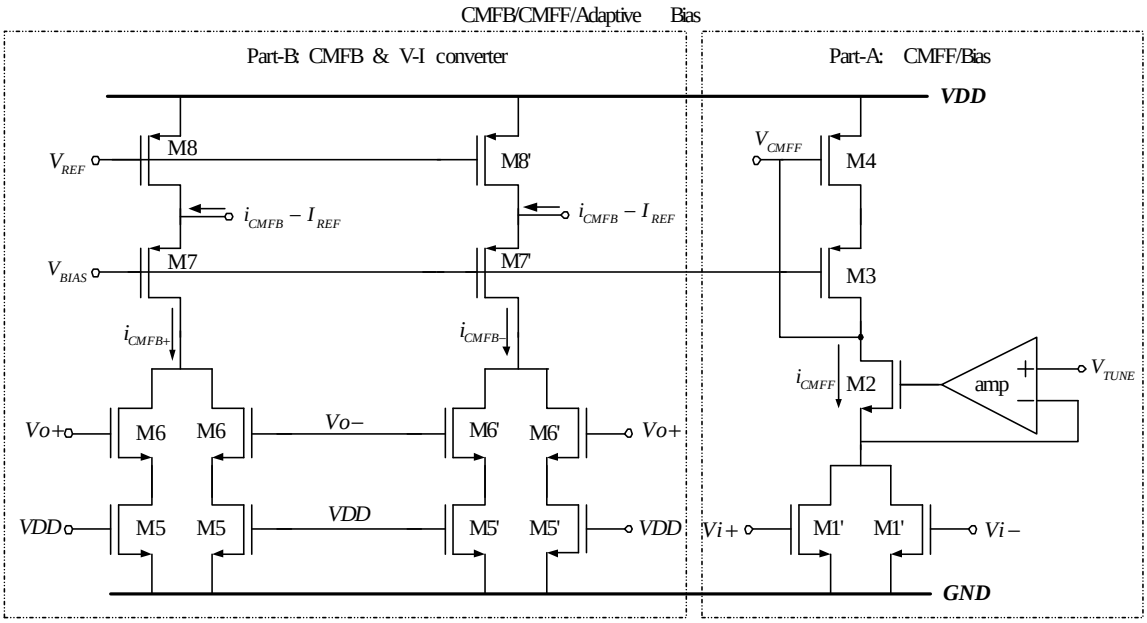

Figure II.17 A fast common-mode control circuit

This CM control circuit is used to control an integrator's output CM voltage and the simulated CM step response is shown in Figure II.18. The simulation conditions are the same as those that produces Figure II.15. With a unity-gain frequency of 156MHz, the phase margin of the CMFB loop is 80.3 degrees. It can be seen that no overshot is observed in the CM step response, which means this CMFB is more stable than the previous discussed CM control circuit. Compared to the CM control circuit discussed in sections 2.5.1 and 2.5.2, this CM control circuit has less poles in the CMFB loop, faster response, similar power consumption, but increased parasitics (two branches for the CM detection and V-I converting).

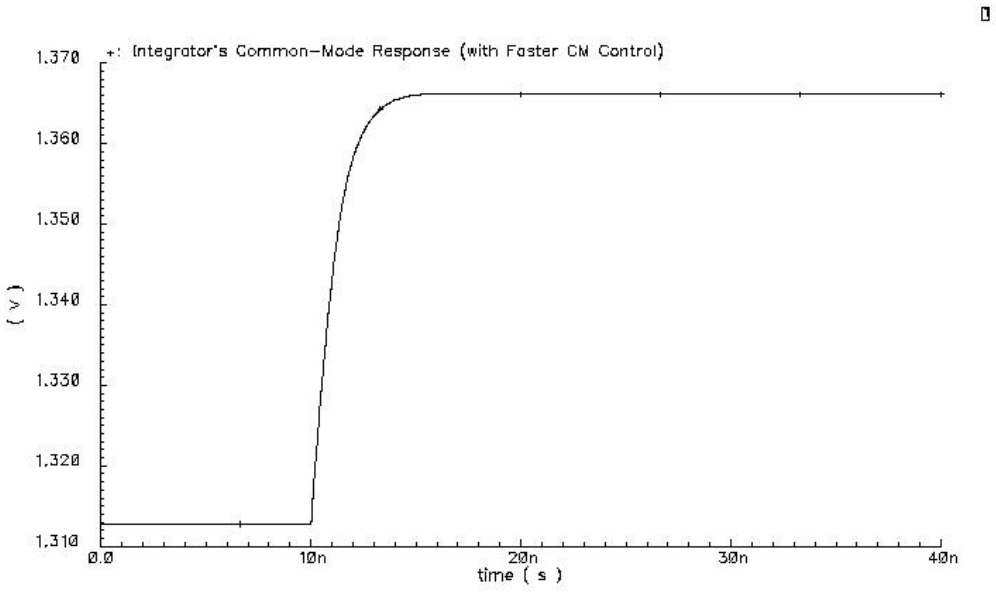

Figure II.18 CMFB closed loop CM step response with a CM current step of 50μA

2.6. Filter Architecture

Usually Bessel-Thomson approximation (maximally flat delay) and equiripple delay approximation are the two filter approximations used for the design of filters with approximately constant group delay. Since for a given delay error the useful bandwidth of the equiripple delay approximation is expected to be wider than that of a maximally flat delay approximation of the same order, a fourth-order equiripple linear phase filter was chosen. The normalized filter transfer function is given by:

$$H(s) = \frac{1.0151}{s^2 + 1.7571s + 1.0151} \cdot \frac{2.5558}{s^2 + 1.3925s + 2.5558} \tag{36}$$

where ω_{o1}=1.0075, Q_1=0.5734, ω_{o2}=1.5987, Q_2=1.1481.

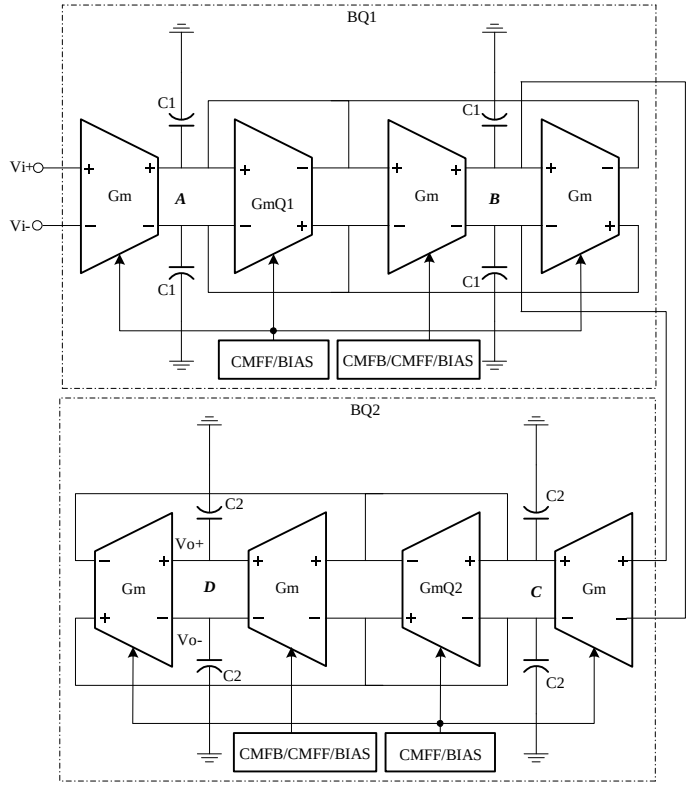

Figure II.19 4th-order equiripple linear phase filter

The filter architecture is shown in Figure II.19. Same transconductance is used for all of the six G_m cells. Similar but scaled transconductance is used for G_{mQ1} and G_{mQ2} in order to adjust the Q's of the biquads. C_1 and C_2 represent the total capacitance at nodes *A, B* and nodes *C, D,* respectively. C_1 and C_2 include the load capacitance as well as the parasitic capacitance. Two common-mode control circuits have been used to control the two nodes *B* and *D*. As a result of the pseudo-differential structure used, *A* and *C* are low-impedance nodes for both differential signals and common-mode signals; hence, we

only use *Part-A* of the CM control circuit to provide CMFF and adaptive-bias for these nodes. The transconductance of G_m, G_{mQ1}, and G_{mQ2} are tuned by an automatic tuning system (which will be explained in the next section). For each biquad of the filter, we can match the total capacitance at the biquad's nodes. In this way, we can scale the OTA according to the desired Qs directly and get the proper transconductance for G_{mQ1} and G_{mQ2}. The capacitance at the filter's nodes (*A*, *B*, *C*, and *D*) are summarized in Table II.3. There is a trade-off between the frequency response and the noise performance. While smaller capacitance provides higher achievable bandwidth, the noise performance is degraded. Also with smaller capacitance, the parasitics becomes more significant and this limits the circuit accuracy.

Table II.3 Capacitances at the filter's nodes

Filter's node	Parasitic capacitance (*pF*)	Poly capacitance (*pF*)	Target capacitance (*pF*)
A	0.52	1.18	1.70
B	0.34	1.36	1.70
C	0.48	0.58	1.06
D	0.34	0.72	1.06

2.7. Automatic Tuning System

Low quality factor filters are low sensitive to component tolerances and temperature variations, hence, Q-tuning schemes are not required for those applications. For this design, a simple automatic frequency-tuning system is used to compensate the variations

of the pole locations. The topology is based on the architecture reported in [28]; the principle of the automatic tuning system is shown in Figure II.20.

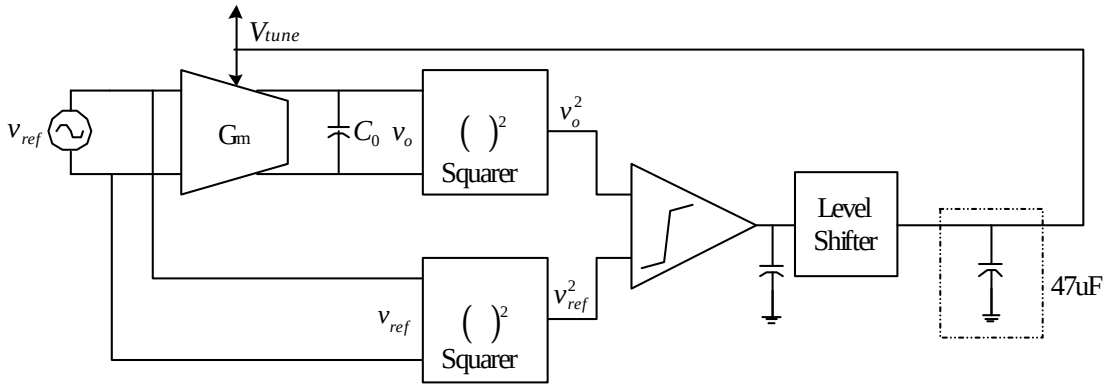

Figure II.20 Block diagram of the automatic tuning system

The OTA G_m is a replica of the transconductor used in the filter. Connected as an integrator, its transfer function is given by

$$H(s) = \frac{G_m}{G_o + s \cdot C_o} \tag{37}$$

where G_o and C_o are the output conductance and the total capacitance at the integrator's output, respectively. Around the unity-gain frequency of the integrator, $H(s) \cong G_m/(sC_o)$ and the unity-gain frequency is $f_u = G_m/(2\pi C_o)$. By using a reference input-signal $v_{ref} = A\sin(2\pi f_r t)$, the integrator output voltage becomes

$$v_o = \left(\frac{f_u}{f_r}\right) A\cos(2\pi f_r t) \tag{38}$$

i.e. the integrator output signal magnitude is proportional to the ratio of the integrator unity-gain frequency to the reference frequency. Hence, by comparing the magnitude of the reference input signal with the integrator output signal, the integrator unity-gain frequency can be tuned to the reference frequency. The voltage comparator can be realized using two peak detectors and a low-pass filter; low dc-offset circuitry is required for this approach.

The approach used here is based on comparing the mean squared values. Squaring ν_{ref} and ν_o and applying the trigonometrical identities the following expressions can be obtained:

$$v_{ref}^2 = \frac{A^2}{2} - \frac{A^2}{2}\cos(4\pi f_r t) \tag{39}$$

$$v_o^2 = \frac{A^2}{2}\left(\frac{f_u}{f_r}\right)^2 - \frac{A^2}{2}\left(\frac{f_u}{f_r}\right)^2 \cos(4\pi f_r t) \tag{40}$$

After filtering the high frequency components, the dc levels are compared to obtain the correction error. This error is shifted down and further low-pass filtered by an external capacitor (4.7μF), then it is used to adjust the OTA's transconductance. If the control loop dc gain is large enough, under steady-state conditions, the error is close to zero and G_m/C_o is tuned to the reference frequency.

The squarer is similar to the one used in [29] and it is shown in Figure II.21. The squarer is based on the simple model that the drain current of a transistor working in saturation region is proportional to the gate-source voltage, that is, the difference of two inputs. Transistors M1 – M5 are working in saturation region. M3 and M4 act as source

followers, where M1 and M2 are squaring transistors. An assumption is made here that the aspect ratio $(W/L)_3$ of the source follower is much larger than $(W/L)_1$ of the squaring transistor, and the drain current of the squaring transistor is much less than the bias current I_S. Then the gate-to-source voltage drop of the source follower may be regarded as a constant since the drain current variation of the source follower is very small with respect to the bias current I_S. It can be shown that the current flowing through the diode-connected transistor M5 can be expressed as

$$i_{M5} = \frac{1}{4}\beta\left(\frac{W}{L}\right)\left(V_i^+ - V_i^-\right)^2 + I_{M5} \tag{41}$$

where $\beta=\mu C_{ox}$, and I_{M5} represents the dc biasing current of the two squaring transistors. Notice that the current i_{M5} is not affected by the dc common voltage of the two inputs V_i^+ and V_i^- as long as the dc common voltages at the two inputs are the same, which is the case in this tuning scheme.

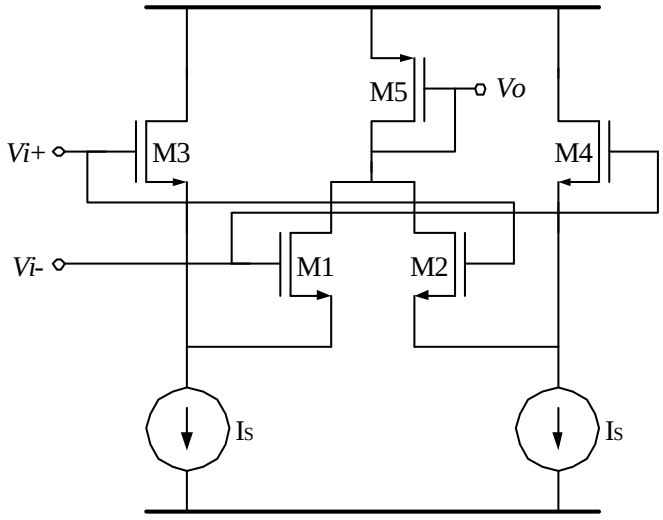

Figure II.21 Squarer

The comparator and the level-shifter are shown in Figure II.22a and Figure II.22b. The comparator is a single stage OTA. The level shifter is used to maximize the linear range of the automatic tuning system. The loop gain is stabilized by an external capacitor. This structure is compact and allows us to control the filter cutoff frequency within an error below 5%. The accuracy of the system is limited by the OTA differential offsets, offset current due to the voltage squarers and comparator, finite gain of the control loop, and mismatches between the master and slave circuits.

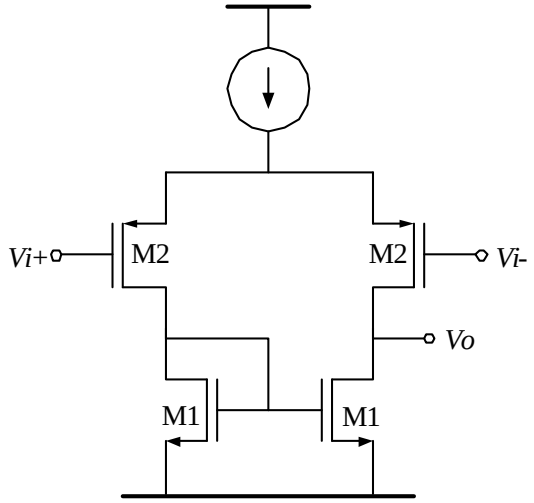

Figure II.22a Comparator

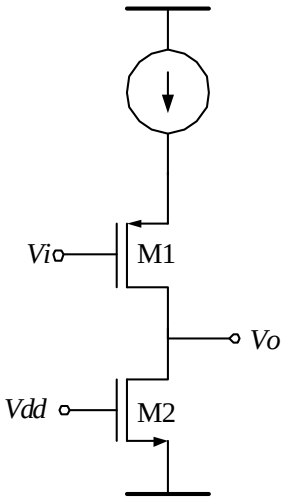

Figure II.22b Level-Shifter

The experimental results show a cutoff frequency tuning error of less than *5%* over a frequency range of 80-200MHz. The tuning accuracy is also limited by the mismatches between the integrator's capacitance and the filter's capacitance.

2.8. Experimental Results

The proposed OTA and the filter have been fabricated in a 0.35μm CMOS process through the MOSIS service. The chip micrograph is shown in Figure II.23.

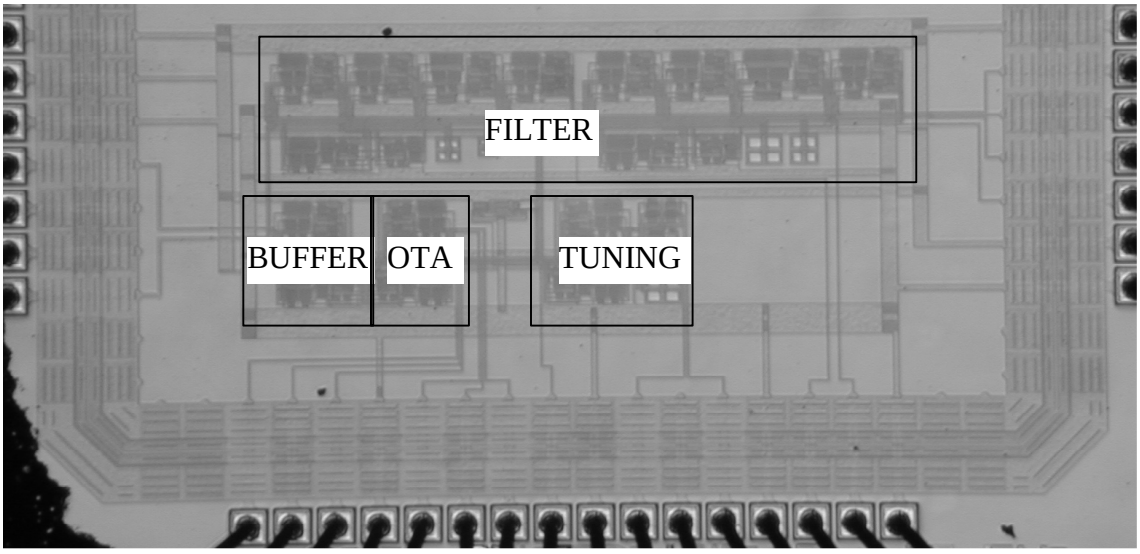

Figure II.23 Chip micrograph

With a single 2.3V power supply, the OTA's power consumption is 7.4mW. The OTA was terminated with a 50Ω matching impedance network. Experimental results for the standalone OTA show that the THD is –48dB for a $2V_{pp}$ differential input at frequency of 20MHz, while the simulated THD is –49.4dB; the experimental output spectrum under these conditions is shown in Figure II.24.

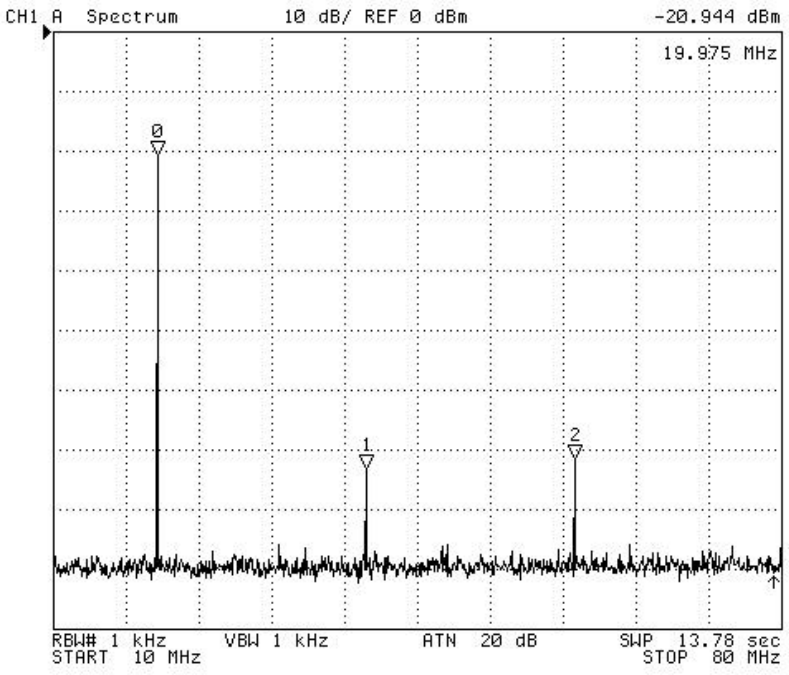

Figure II.24 OTA's output spectrum ($V_{in}=2V_{pp}$)

All the previously discussed circuits and techniques are used for the design of a 4^{th}-order 0.05^{o} equiripple linear phase filter. For the filter's experimental setup, a similar OTA is used as a buffer to converts the filter outputs into current. The buffer is terminated with 50Ω resistors and a high frequency transformer. The experimental results show that the filter has a large signal swing; THD figures of less than –44dB for input signals up to $2V_{pp}$ at frequency of 20MHz are achieved, as shown in Figure II.25 (the simulated THD is –47.8dB). The third-order inter-modulation (IM3) of the filter for a two-tone input of $1V_{pp}$ (at 60MHz and 70MHz) is –40dB, as shown in Figure II.26. The measured inband IM3 is shown in Figure II.27; notice that the IM3 is less than –38dB over the whole filter bandwidth.

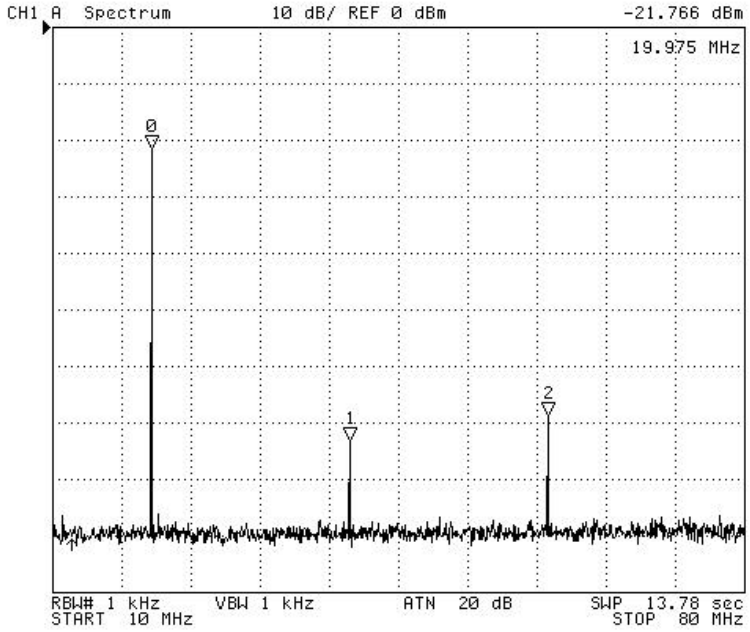

Figure II.25 Filter's output spectrum ($V_{in}=2V_{pp}$)

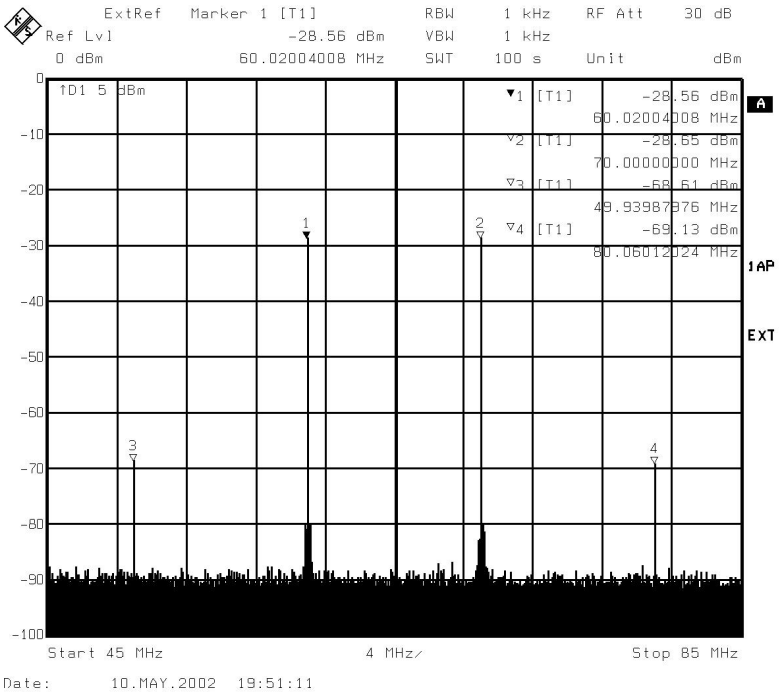

Figure II.26 Filter's IM3 for a two-tone input (@60MHz and 70MHz) of $1V_{pp}$ each

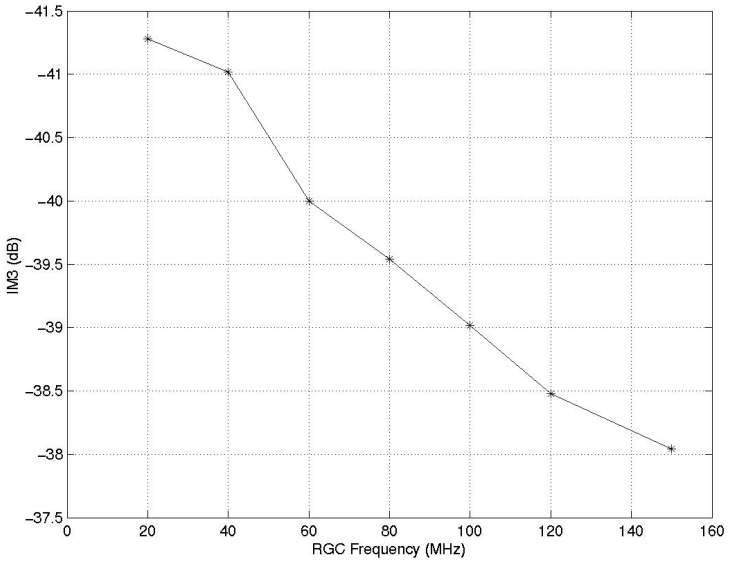

Figure II.27 Filter's IM3 vs. frequency (V_1=1V_{pp}, V_2=1V_{pp})

For the filter tuned at 150MHz, the filter's magnitude response, phase response, and group delay response are shown in Figure II.28, Figure II.29, and Figure II.30, respectively. The filter's –3dB frequency is around 150MHz. The filter's phase response is linear and the group delay ripple is less than ±100ps up to 1.5f_c.

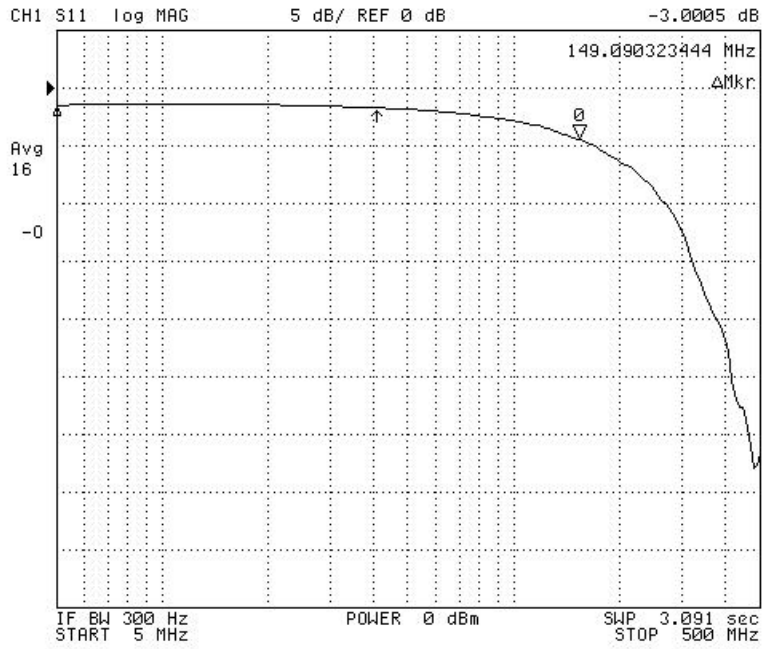

Figure II.28 Filter magnitude response with a bandwidth of 150MHz

Figure II.29 Filter's phase response with a bandwidth of 150MHz

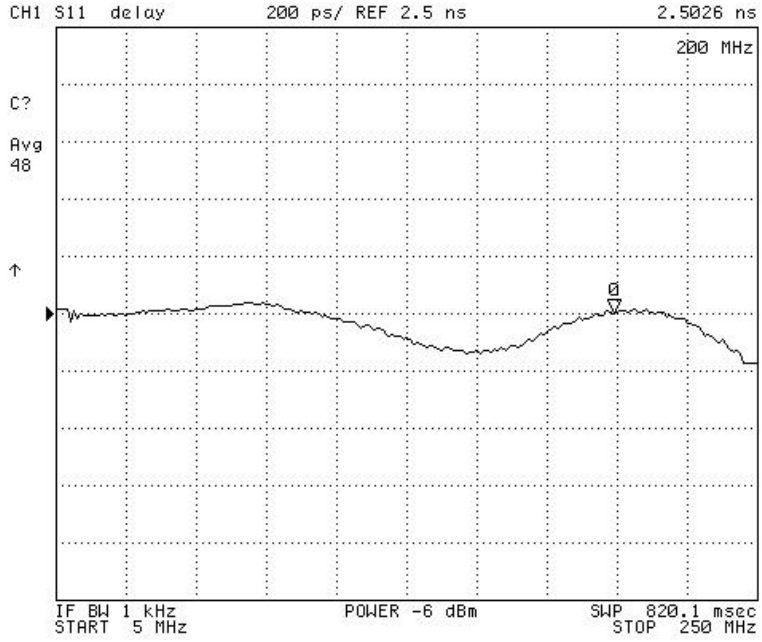

Figure II.30 Filter's group delay response with a bandwidth of 150MHz

The magnitude response of the filter, driven by the automatic tuning system, is shown in Figure II.31. The differences in the low-frequency gain are due to the different transconductance of the buffer connected after the filter over the tuning, which was also controlled by the automatic tuning circuit. The cutoff frequency tuning error is less than 5% for all frequencies.

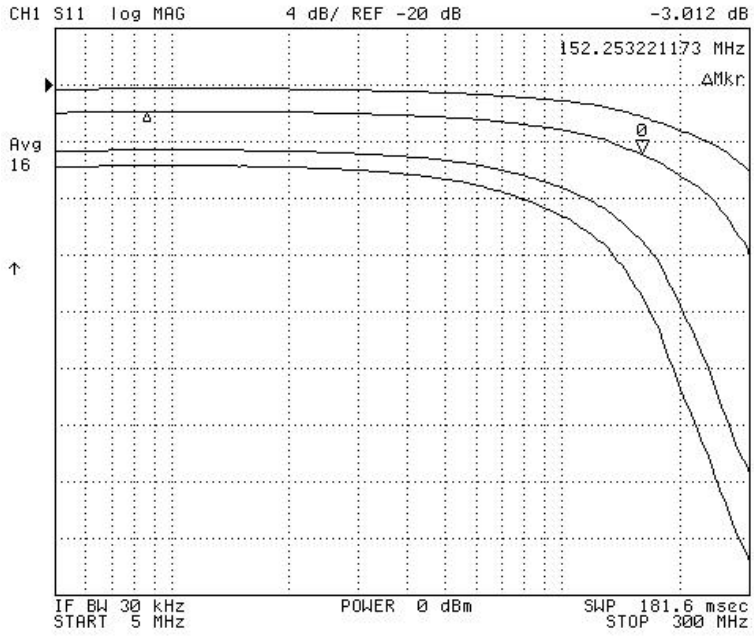

Figure II.31 Zoomed filter's magnitude response with automatic frequency tuning system (reference frequency = 80MHz, 100MHz, 150MHz, and 200MHz)

The common-mode rejection ratio (CMRR) of the filter is 40dB at 60MHz and is greater than 32dB at 150MHz. The positive and negative power supply rejection ratios ($PSRR^+$ and $PSRR^-$) are 38dB and 31dB at low frequencies and they are greater than 21dB and 22dB within the whole passband, respectively. The dynamic range of the filter is 52dB @THD<-44dB, and the power consumption of the whole system is 90mW. The measured performances of the filter are summarized in Table II.4.

Table II.4 Performance summary of the standalone filter prototype fabricated in 0.35 CMOS process

Process	*0.35um CMOS*
Filter type	4^{th}-order equiripple
Power supply	*2.3V*
Power consumption	*72mW*
Cutoff frequency	*80-200MHz*
Group delay ripple	*<4%* up to $1.5f_c$
Noise level (*BW=150MHz*)	$1.69mV_{rms}$
Differential input for *THD<-44dB @20MHz*	*2Vpp*
Dynamic range *@THD=-44dB*	*52dB*
Worst case CMRR *@f=150MHz*	*32dB*
Worst case $PSRR^+$ *@f=150MHz*	*21dB*
Worst case $PSRR^-$ *@f=150MHz*	*22dB*

The experimental results of the proposed design are also compared with previous realizations in Table II.5. For the proposed filter, the automatic tuning system is included in the power budget. With the cheapest technology and the lowest power supply voltage, the proposed filter has the largest linear signal swing. It is a result of the well designed pseudo-differential OTA with transistors operating in triode region and the well controlled common-mode level due to the proposed common-mode control circuit.

Table II.5 Comparison of several linear phase filters

Parameters	[30]*	[31]*	[32]*	[33]*	This work
$f_c(MHz)$	10-100	30-100	30-120	80-200	80-200
Technology	0.29um BiCMOS	0.25um CMOS	0.25um CMOS	0.25um CMOS	0.35um CMOS
$V_{in,max}\,(mV_{pp})$	100	200	200	800	2000
THD@ $V_{in,max}\,(dB)$	-46	-46	-50	-42	-44
Dynamic Range (dB)	40	--	45	--	52
Power/Pole (mW)	17	30	15	30	22
Supply Voltage(V)	3	2.5	2.5	3	2.3

* These filters provide gain boosting, hence they are more complex, but the automatic tuning systems are not included for the power consumption.

2.9. Conclusions

A low voltage and highly linear full CMOS transconductor using transistors operating in triode region has been presented. A common-mode control circuit that combines CMFB, CMFF, and adaptive-bias has been discussed. A large linear signal swing has been achieved due to the well controlled CM behavior. The principle of the CM control circuit can be easily applied to the design of differential structures, and it is well suited for low voltage pseudo-differential architectures.

Experimental results of the OTA with the CM control and the 80-200MHz 4^{th}-order linear phase filter are in good agreement with the theoretical results. The proposed circuit is attractive for low-voltage applications and it presents good power efficiency. The ratio of the RMS (root-mean-square) value of the AC signal to the power supply voltage is around 31%, which is much better than previous realizations.

CHAPTER III

LOW-VOLTAGE, LOW-POWER LVDS DRIVERS

3.1. Background and Motivation

The demand for more processing power continues to increase, and apparently has no limit. The ever-increasing processing speed of microprocessor motherboards, optical transmission links, chip-to-chip communications, etc., is pushing the off-chip data rate into the gigabits-per-second range. While scaled CMOS technologies continue to enhance the on-chip operating speeds, off-chip data rates have gained little benefit from the increased silicon integration. This is primarily due to the excessive power consumption necessary for driving impedance-controlled electrical interconnects, which leads to an increase in the costs related to packaging and thermal management [15].

In the past, off-chip high data rates were achieved by massive parallelism, with the disadvantages of increased complexity and cost for the IC package and the printed circuit board (PCB). So it is beneficial to move the off-chip data rate to the range of Gb/s-per-pin or above. In fact, the SIA Silicon Roadmap [34] forecasts an off-chip frequency of 1GHz for peripheral buses with the 100-nm generation in 2006. Also reducing the power consumption is critical for battery-powered portable systems as well as some other systems in order to extend the battery life and reduce the cost related to packaging and additional cooling systems.

Scalable Coherent Interface (SCI) is a high-speed packet transmission protocol that efficiently provides the functionality of bus-like transactions (read, write, lock, etc.), but it uses a collection of fast point-to-point links instead of physical buses to reach higher speeds. The initial physical implementations are based on emitter coupled logic (ECL) signal levels [16], which consume more power than is practical in the low-cost workstation environment and are inconvenient for some applications. Low-voltage differential signaling (LVDS) is a technology developed to provide a low-power and low-voltage alternative [17] to ECL and other high-speed I/O interfaces for point-to-point transmissions. LVDS achieves higher speed and significant power savings by means of a differential scheme for transmission and termination, in conjunction with low voltage swing.

The following are some of the basic design strategies selected by the LVDS standard [17]:

—Low-voltage swing. To minimize power dissipation and enable operation at very high-speed, small swing (400 mV maximum) signals are specified.

—Differential signals. Small signal swings require differential signaling for adequate noise margin in practical systems.

—Self-terminated. To minimize board area and cost, and to maximize clock rates, each receiver is assumed to provide its own termination resistors.

Differential signaling at first appears to double the number of signal lines, but the pin-count overhead is actually much less than this, since reliable single-ended schemes require many more ground signals (many high-speed chips and/or backplanes provide

one ground for every two signal pins) and run at significantly lower speeds. Other design benefits associated with differential signals include Constant Driver Current (which simplifies the design of power-distribution wiring), Low Power (differential signals allow low signal current to be used), Simple Board Design (differential signals are usually less sensitive to imperfections in the transmission line environment), Low Electromagnetic Interference (EMI) (equal and opposite currents create canceling electromagnetic fields, which dramatically reduces the electromagnetic emissions), and Low Susceptibility to Externally Generated Noise (that can be considered as common-mode noise and is rejected by the differential nature of the architecture).

The purpose of the LVDS standard is to provide a protocol for high speed, low-power, and low cost point-to-point communications, and so the standard demands for low-voltage, low-power transmitter and drivers to increase the data rate and reduce the cost. The target of this work is to design high speed (data rate of 1Gb/s and above), ultra low-voltage (single supply voltage as low as 1.6V) and low-power LVDS drivers fully compatible with IEEE Std 1596.3-1996 [17] for general purpose links and IEEE Draft P802.3ae/D5.0 [35] for XSBI interface. With low voltage supplies, the driver's power consumption is further reduced. The EMI and the cost related to the packaging and cooling systems are reduced as well. Also, low-voltage supply drivers make it possible to use single supply for both the I/O and the core circuits and simplify the board design.

3.2. LVDS Interfaces

A LVDS interface, as shown in Figure III.1a, has a low-voltage swing (250 mV – 400 mV); it is connected point-to-point and achieves very high data rates (up to 500 Mb/s per signal pair) and reduced power dissipation [36]. LVDS uses differential data transmission and the transmitter is configured as a switched-polarity current generator. A differential load resistor at the receiver end provides current-to-voltage conversion and optimum line matching at the same time.

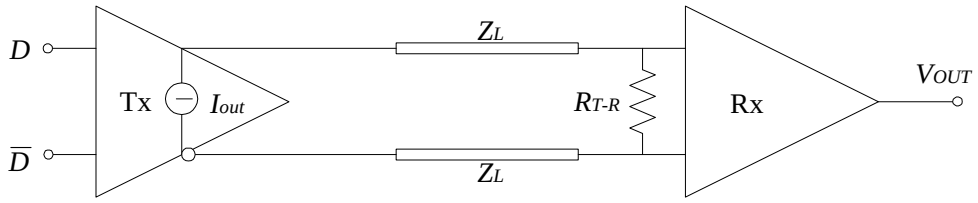

Figure III.1a LVDS interface with line termination at the receiver end

The power dissipation is low because signal swings are small: a minimum of 2.5mA is sent to the 100Ω termination resistor. This sharply reduced power dissipation presents an important advantage: integrating the line termination resistors, interface drivers and receivers, and the processing circuits in the same integrated circuit.

The switching speed is high because the driver load is an uncomplicated point-to-point 100Ω transmission line environment. Switching speed is also high because interface devices are all on the same piece of semiconductor material, reducing the skew due to process, temperature, and supply variations between signal pairs.

Due to the imperfect termination, package parasitics, and component tolerance, or crosstalk [37], there are reflected waveforms returning to the driver. The reflected waveforms see current sources (which has a very high output impedance) with reflection coefficient of +1. Therefore, the driver provides no termination and fully reflects both the differential and common-mode reflected signals [38]. The 100Ω termination resistor at the receiver end terminates the differential mode. In summary, the differential-mode is terminated only at the load, while the common-mode is not terminated at all.

The termination provided by the LVDS is adequate since the receiver rejects common-mode noise, and the differential signal is terminated at the load. As data rates push significantly above 600 Mb/s and as connectors are added, this LVDS termination scheme fails to provide adequate signal integrity. Under these circumstances, an additional termination resistor is usually placed at the source end to suppress reflected waves, as shown in Figure III.1b, and the LVDS signaling can be substantially enhanced.

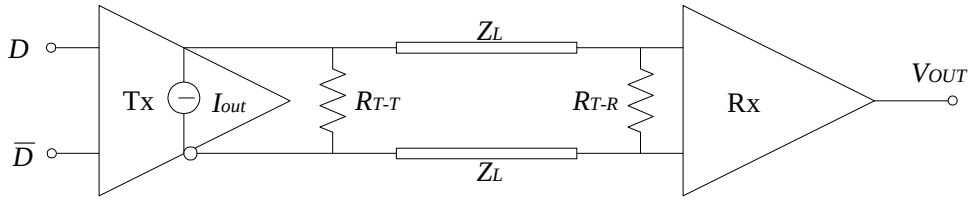

Figure III.1b LVDS interface with termination at the receiver and source ends for gigabits-per-second operation

With the both ends termination, the common-mode signals are still not terminated, so the receiver's common-mode rejection is still used to avoid common-mode noise. For

both the driver and receiver, building the termination resistors into the circuits can simplify the PCB design and optimize the signal integrity.

3.3. LVDS Driver Structures

3.3.1 Typical Bridged-Switches LVDS Driver

A typical bridged-switches LVDS driver behaves as a current source with switched polarity [17] as shown in Figure III.2a. The bias current I_b is switched through the termination resistors in one direction according to the data input, and thus produces the correct differential output signal swing. A possible implementation of the typical LVDS driver is shown in Figure III.2b. It uses a configuration with four MOS switches (M1 – M4) in a bridge configuration. If switches M1 and M3 are on (D=HIGH), the polarity of the output current is positive together with the differential output voltage. On the contrary, if switches M1 and M3 are off (switches M2 and M4 are on), the polarity of the output current and voltage is reversed.

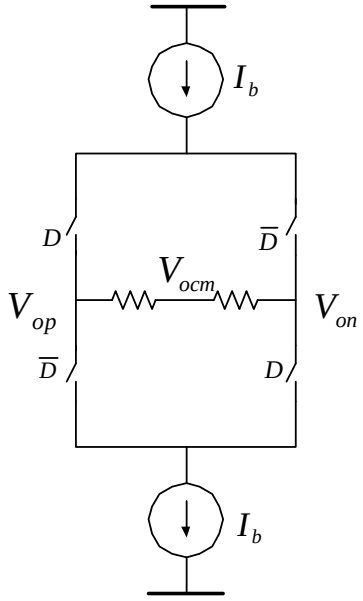

Figure III.2a Typical LVDS driver model

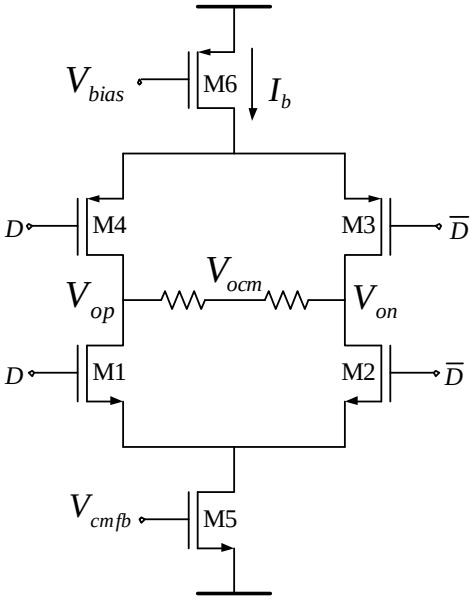

Figure III.2b A possible implementation

The typical LVDS driver works well if the supply voltage (V_{DD}) is 2.5V or greater. It is simple and it only needs minimum static current consumption to produce the required output signal swing. The drawback of the typical LVDS driver is that it is not suitable for low-voltage supplies (eg. V_{DD} less than 2V). This is mainly due to the finite on-resistance of the PMOS transistor switches and the large amount of current (nominally 6.4mA for a signal swing of 320mV and a 50Ω termination resistance) flowing through the switches. The voltage drop across the resistance consumes headroom and it requires relatively high voltage supplies for the LVDS driver to operate properly.

3.3.2 All NMOS Switches LVDS Driver with CMFB

One implementation similar to the typical LVDS driver was proposed in [39] and it is shown in Figure III.3a. Notice that the top two switches M3 and M4 are NMOS

transistors instead of PMOS transistors. This configuration reduces the effects of the charge injection at the output nodes V_{op} and V_{on}. As shown in Figure III.3c, we assume the gate-drain capacitance of M1 and the gate-source capacitance of M4 are C_{p1} and C_{p4}, respectively. Also we assume the parasitic capacitance from node V_{op} to ground is C_p. As the input data D charges (discharges) C_p through C_{p1}, the out-of-phase input data D' discharges (charges) C_p through C_{p4} and it partially cancels the charge injection caused by D. Similar charge injection cancellation occurs at node V_{on}.

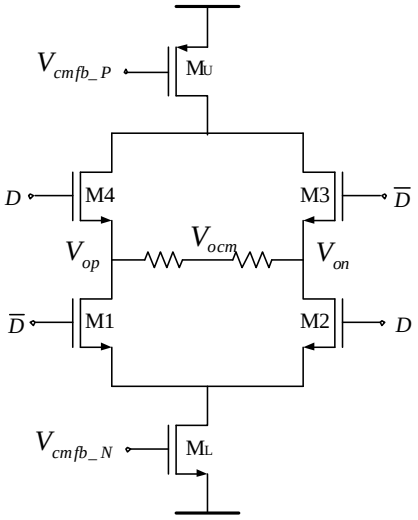

Figure III.3a LVDS driver core

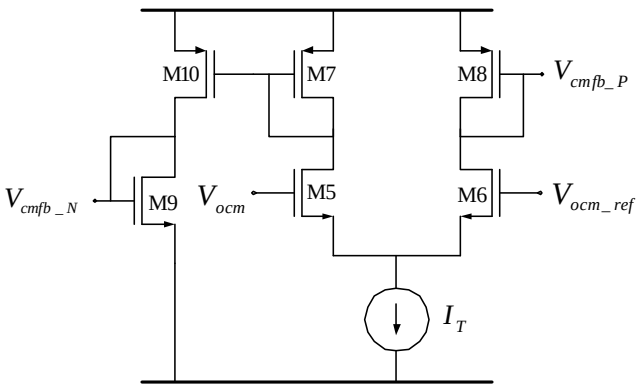

Figure III.3b LVDS driver CMFB

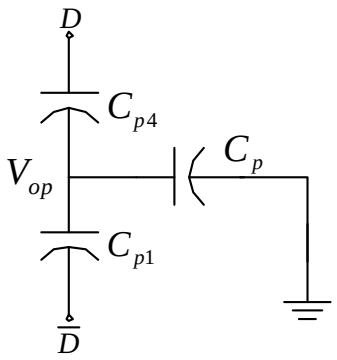

Figure III.3c Parasitic capacitors associated with the charge injection

In order to achieve higher precision and lower circuit complexity, a simple low-power common-mode feedback control was used in the driver; the topology is shown in Figure III.3b. The output common-mode voltage is sensed by means of a termination resistive divider and compared with a 1.25V reference by the differential amplifier M5 – M8. The fractions of the tail current I_T flowing across M7 and M8 are mirrored to M_U and M_L, respectively, thus forcing $V_{ocm} \approx 1.25V$. The tail current I_T is chosen to develop the correct voltage swing on the termination resistors. The mirroring gain K of M_U/M_7 and M_L/M_8 is large in order to reduce the power consumption of the common-mode feedback circuit. The bias current I_T is obtained from a reference voltage provided by an internal bandgap and an integrated resistor.

This all NMOS switches LVDS driver has the similar advantages as the typical LVDS driver. It is simple and its static current consumption is kept to minimum if we neglect the current consumption of the CMFB. The simple CMFB maintains the output common-mode level within the specifications over the process, supply voltage, and temperature (PVT) variations, without external components nor trimming procedures.

Similarly, due to the on-resistance of the top switches, the drawback of this all NMOS switches LVDS driver is that it is not suitable for low-voltage supplies neither.

This LVDS driver can operate up to 1.2Gb/s with 8-bit random data pattern. Its static power consumption is 43mW from a 3.3V supply (corresponds to a static current consumption of 13mA) and it occupies 0.175mm^2.

3.3.3 Two Switches LVDS Drivers

Instead of using four switches in a bridge configuration, a LVDS driver using two switches in an open drain configuration for current steering was proposed in [40]. A simplified schematic revealing the basic idea of this LVDS driver is shown in Figure III.4. A reference voltage V_{CM} and current i_1+i_2 are provided by an unity gain buffer. M1 and M2 are two NMOS switches controlled by the input data. Suppose switch M1 is off, and the current flowing through R1 and R_T is i_1 and the current flowing through R2 is i_2, then $i_2=3i_1$. Assume $i_1+i_2=8$mA, then $i_1=2$mA and the signal swing across R_T is 200mV. The output common-mode voltage is 1.2V.

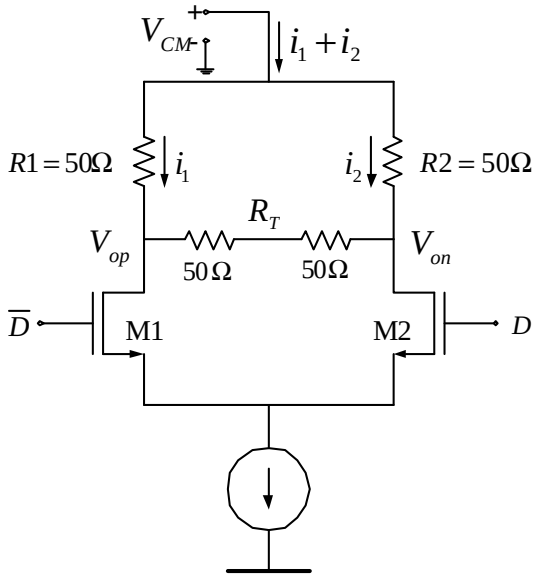

Figure III.4 Two switches LVDS driver

Since R1 and R2 consume voltage headroom, this two switches LVDS driver is not suitable for low-power supplies neither. The buffer that provides the reference voltage needs to provide 8mA current; its output impedance should be much less than 50Ω; it is a very strong buffer and its design is not trivial. This LVDS driver is compatible with IEEE LVDS standard [17] for reduced range links. Its static power consumption is 23mW from a 1.8V supply and it occupies 0.022mm^2.

3.4. Roadmap to the Low-Voltage, Low-Power LVDS Drivers

Low voltage differential signaling (LVDS) is a standardized data transmission format that is widely used for serial data transmissions [17]. Such LVDS formatting with different supply voltages is illustrated in Figure III.5. As shown in Table III.5, a

differential signal is centered about a common mode voltage of 1.25V. The maximum magnitude of the differential signal is 400mV. Typically, the LVDS signal varies in magnitude from 1.05V to 1.45V.

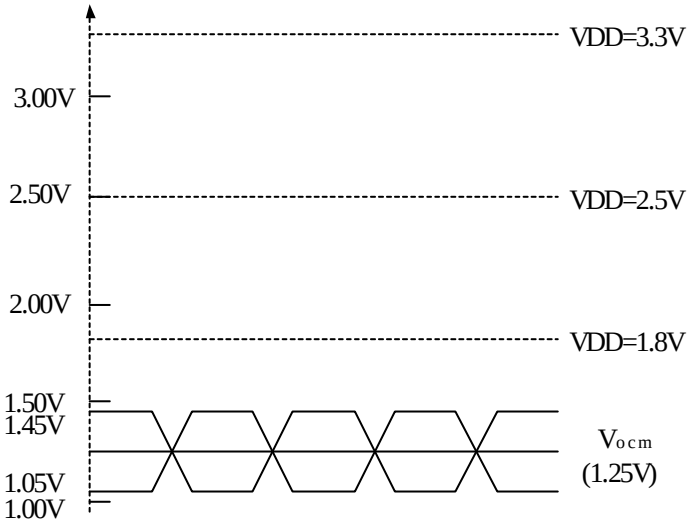

Figure III.5 LVDS signal formatting

3.4.1 LVDS Driver Specifications

The LVDS specifications for some of the driver parameters are summarized in Table III.1.

Table III.1 Specification for LVDS driver

Symbol	Parameter	Conditions	Min	Max	Units
$\|V_{OD}\|$	Output differential voltage	Differential load, R_{load}=100Ω±1%	250	400	mV
V_{OS}	Output offset voltage	Differential load, R_{load}=100Ω±1%	1125	1375	mV
R_O	Output impedance, single ended		40	140	Ω
ΔR_O	R_O mismatch			10	%
$\|\Delta V_{OD}\|$	Change in V_{OD} between “0” and “1”	Differential load, R_{load}=100Ω±1%		50	mV
$\|\Delta V_{OS}\|$	Change in V_{OS} between “0” and “1”	Differential load, R_{load}=100Ω±1%		50	mV
t_{fall}	V_{od} fall time, 20-80%	Z_{load}=100Ω±1%	300	500	ps
t_{rise}	V_{od} rise time, 20-80%	Z_{load}=100Ω±1%	300	500	ps

As shown in Table III.1, LVDS standards pose relatively stringent requirements on the output common-mode voltage as well as the differential signal swing, raising interesting design issues if low-cost solutions with neither external components nor trimming procedures are required. Specifically, the output differential voltages are within 250mV and 400mV, and the output common-mode voltages (or output offset

voltage) are within 1.125V and 1.375V, with a nominal common-mode voltage of 1.25V.

3.4.2 Headroom Issues Associated with the Previous LVDS Drivers

The typical bridged-switches LVDS driver is shown in Figure III.2b. This LVDS driver works well when the supply voltage (V_{DD}) is 2.5V or greater, which is common for 0.25μm and 0.35μm CMOS technologies. But when the supply voltage drops below 2V (e.g., 1.8V for 0.18μm CMOS technology), the typical LVDS driver does not have enough headroom in the V_{DD} direction. With a differential output signal swing of 400mV, as shown in Figure III.5, the signal swing is bounded from 1.05V to 1.45V, centered at a common-mode voltage of 1.25V. If, as allowed by the LVDS standard, the common-mode voltage drifts by 10% (e.g. 1.375V), then the output signal ranges from 1.175V to 1.575V. With a 1.8V supply, there is only 225mV of headroom for the PMOS current source and the PMOS transistor switches. For an on-resistance of 12Ω (corresponds to a TSMC 0.35μm CMOS process PMOS transistor with a dimension of 700μm/0.4μm) and a drain current of 8mA, the voltage drop across the switch is around 96mV, leaving only 129mV drain-source voltage for the PMOS current source, which is apparently insufficient. This problem is further accentuated when the supply voltage is less than 1.8V.

Similarly, the other architectures discussed in section 3.3. have the same headroom issue in the V_{DD} direction. For instance, for the two switches LVDS driver shown in

Figure III.4, R1 (R2) needs a voltage drop of 200mV for an output signal swing of 400mV, which tightens the headroom issue.

3.4.3 Double Current Sources (DCS) LVDS Driver

A solution to the headroom issue is to remove the top two PMOS switches and replace the PMOS current source by two PMOS current sources, as shown in Figure III.6a and Figure III.6b. We call this LVDS driver Double Current Sources (DCS) LVDS driver. In order to produce the same signal swing, the bottom NMOS current source is required to sink 2Ib, which doubles the current consumption as required by the output signal swing. Accordingly, the embodiment of Figure III.6b consumes more power than the embodiment of Figure III.2b. In addition, the NMOS transistor switches and the bottom NMOS current source are required to be larger than the corresponding transistors in the embodiment of Figure III.2b. If an integrated circuit includes a plurality of LVDS drivers, the increased power consumption and transistor dimensions may be unacceptable.

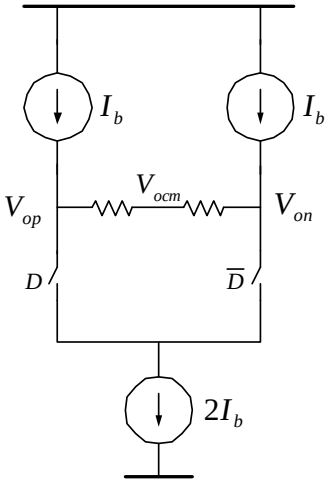

Figure III.6a DCS LVDS driver model

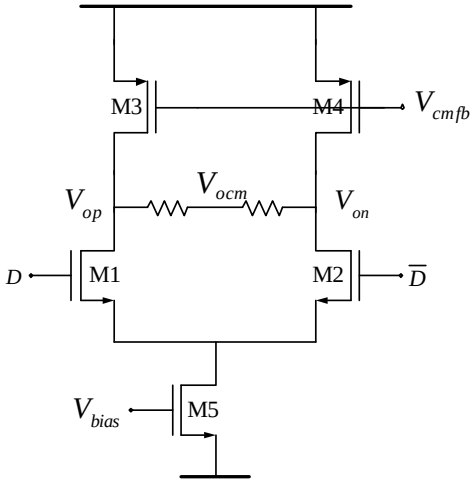

Figure III.6b Possible implementation

Therefore, a need exists for a low-power LVDS driver that operates at very low supply voltages.

3.4.4 Switchable Current Sources (SCS) LVDS Driver

Another solution to the headroom issue is shown in Figure III.7. In stead of using two constant current sources at the top, two switchable current sources are used here, and we call this new driver Switchable Current Sources (SCS) LVDS driver. Depending on the data input, one of the two switchable current sources conducts current. This current flows through the termination resistors and produces the output voltage swing. Notice that the bottom NMOS current source only needs to sink I_b, leading to minimum static current consumption.

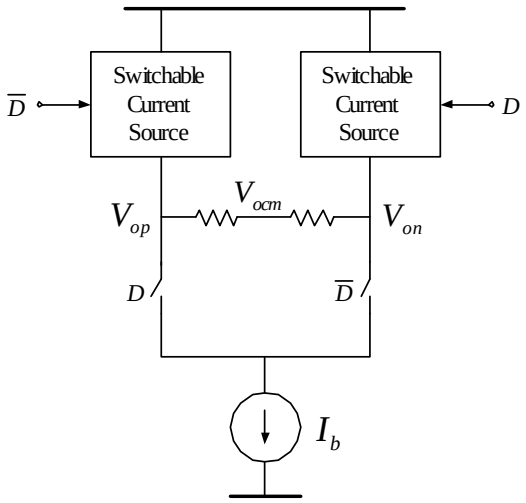

Figure III.7 SCS LVDS driver model

Figure III.8 shows the main principle of the SCS LVDS driver. Suppose we can generate a proper voltage V_{ON} and when this voltage is applied to the gate of M1(M2), it conducts certain current I_D, regardless of the PVT variations. Here transistors M1 and M2, and switches S1 and S2 act as switchable current sources. For instance, when D is HIGH, M2 is ON and it conducts current I_D. This current I_D is then used to produce the output voltage swing.

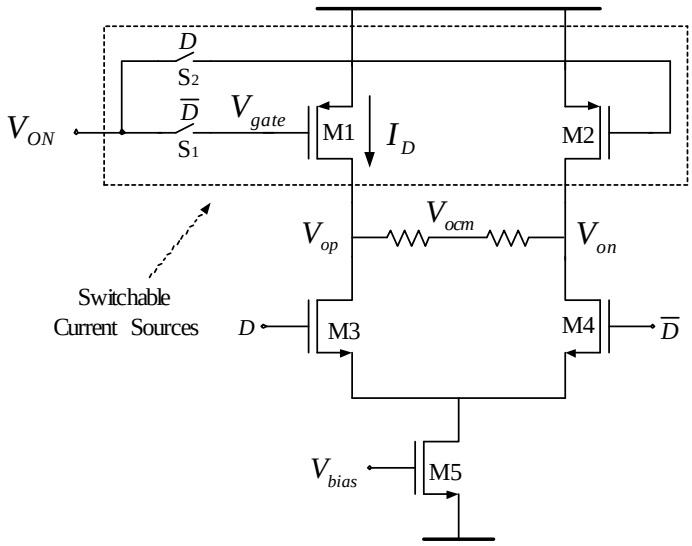

Figure III.8 Main principle of the SCS LVDS driver

In order for the SCS LVDS driver shown in Figure III.8 to be practical, two issues need to be addressed. First, how to generate the corner-dependent reference voltage V_{ON} such that I_D keeps at the proper value, regardless of the PVT variations? Second, since the PMOS switchable current sources need to conduct large currents (e.g., a drain current of 6.4mA is needed for an impedance of 50Ω looking at the two output nodes and a norminal output voltage swing of 320mV), their transistor dimensions are large as well as the parasitic capacitances. So another question is how to change the gate voltages of M1 and M2, or how to charge and discharge the parasitic capacitors at the gate of M1 and M2 quickly?

The above mentioned two issues are addressed in the following SCS LVDS driver shown in Figure III.9. This LVDS driver contains two parts: the switchable current source control module and the core of the LVDS driver.

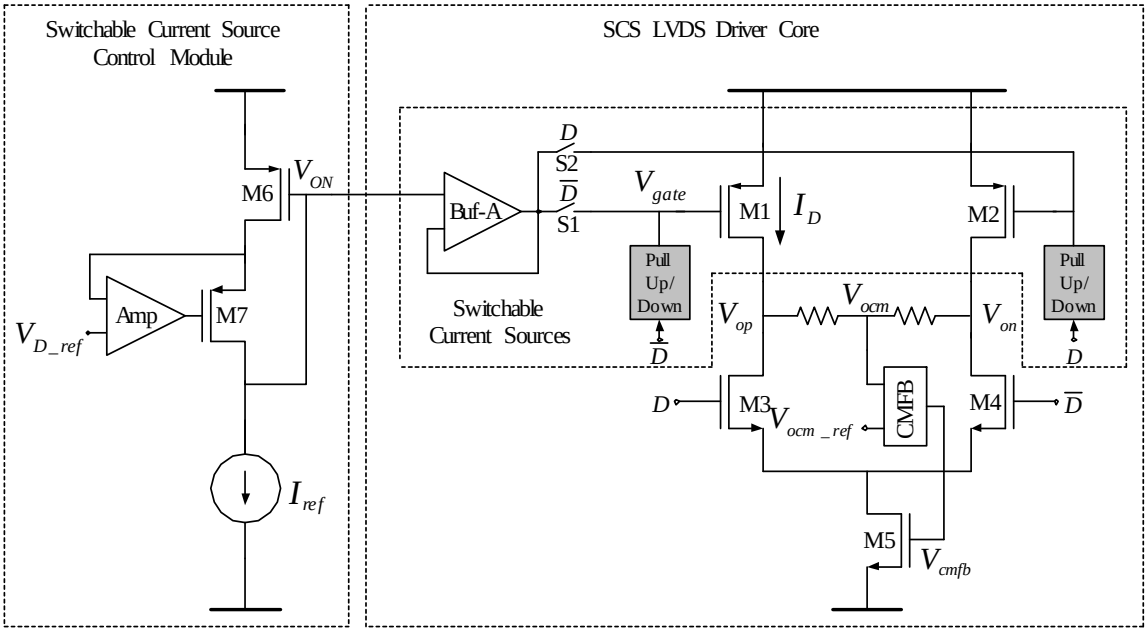

Figure III.9 Schematic of the SCS LVDS driver with active pull up/down

The left part of Figure III.9 is the switchable current source control module. It is used to generate a reference current (I_{ref}) dependent voltage V_{ON} such that when V_{ON} is applied to the gate of M1(M2), it conducts a drain current I_D proportional to I_{ref}. Cascode transistor M7 and amplifier Amp forms a regulated-gain control (RGC) loop. This RGC loop is used to set M6's drain voltage to V_{D_ref}. An important observation is that the output common-mode voltage and signal swing must be maintained; hence the higher voltage of V_{op}(V_{on}) is fixed, and it is defined by V_{D_ref}(=V_{ocm_ref}+$V_{o,swing}$/2), regardless of the PVT variations. V_{ocm} is the output common-mode reference voltage, and $V_{o,swing}$ is the required signal swing. For instance, for a output common-mode voltage of 1.25V and an output signal swing of 320mV, ideally the higher voltage of V_{op}(V_{on}) should be

1.41V. By setting the drain voltage of M6 to V_{D_ref}, we have a good matching for the current mirror composed of M6 and M1(M2). It is worth to mention that the switchable current source control module can be shared by several LVDS drivers, but independent buffers are used for each driver in order to minimize the signal feedthrough.

The right part of Figure III.9 is the core of the SCS LVDS driver. The switchable current sources are used to generate current I_D and they are composed of transistors M1 and M2, buffer-connected amplifier Buf-A, switches S1 and S2, and the pull up/down circuits. The pull up/down circuits are used to quickly change the gate voltages of M1 and M2, i.e. to quickly charge or discharge the parasitic capacitors associated with the node V_{gate}.

The buffer-connected amplifier Buf-A is used to isolate the DC voltage V_{ON} from the data controlled switches. It also provides “fine adjustment” to the gate voltage of M1(M2) when the switch S1(S2) is closed, while the pull up/down circuit driven by the input data provides coarse control. The CMFB is used to set the output common-mode voltage to the desired reference voltage V_{ocm_ref}.

The operation of the switchable current sources is explained as follows. If data D is LOW, then switch S1 is ON and switch S2 is OFF. The M1’s gate voltage is pulled down to V_{ON} through the pull up/down circuit during the data transition while M2’s gate voltage is pulled up to V_{OFF}. M1 conducts current I_D and M2 is OFF. The current I_D flows through the termination resistors and produces the signal swing.

3.4.5 Pull Up/Down Circuits

A potential implementation of the pull up/down circuit is shown in Figure III.10 [41]. It includes a pull up and a pull down circuit. Both of the pull up and pull down circuits are used to produce short period of current pulses at the data's transition edges. These current pulses are used to charge/discharge the parasitic capacitors and so to pull up/down the switchable current source gate voltages.

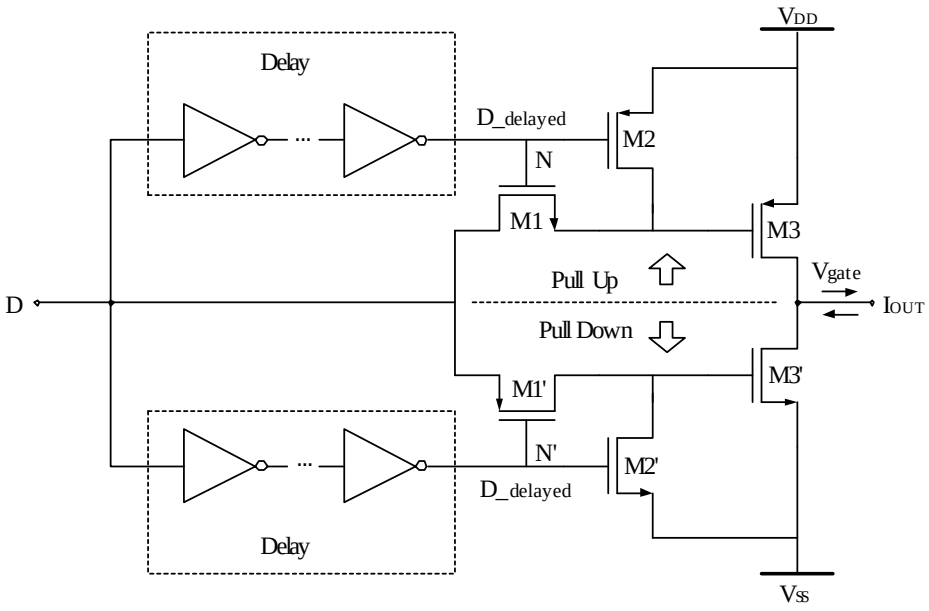

Figure III.10 Active pull up/down circuit

Figure III.11a and Figure III.11b show the waveforms for the data, delayed data and the current pulses for the pull-up and pull-down circuits.

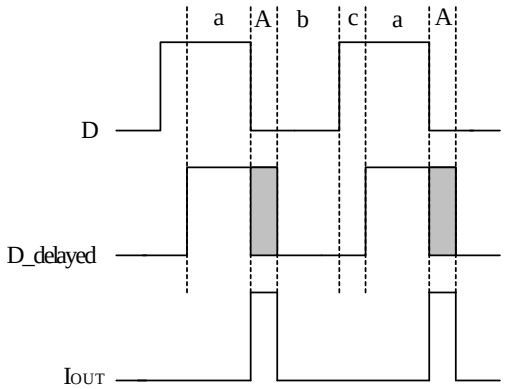

Figure III.11a Pull-up circuit waveforms

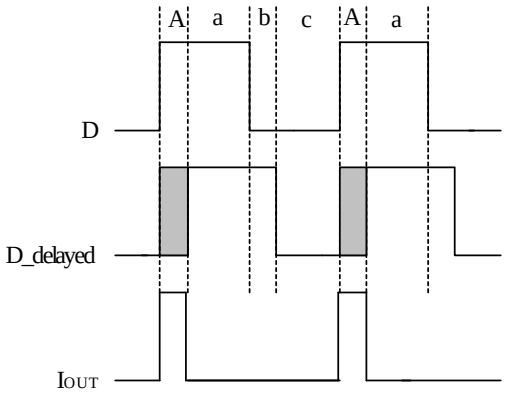

Figure III.11b Pull-down circuit waveforms

Let us analyze the pull up circuit and the corresponding waveforms first. By dividing the waveforms into four time periods A, a, b, and c, the operation of the pull up circuit can be explained as follows.

(1) Period a: Both D and D_delayed are HIGH. M2 is OFF, and M1 is also OFF. Then node N is HIGH, M3 is OFF and the output current I_{OUT} is zero;

(2) Period A: D is LOW and D_delayed is HIGH. M2 is ON and M1 is OFF. Then Node N is LOW, M3 is ON and the output current I_{OUT} is non-zero;

(3) Period b: Both D and D_delayed are LOW. M1 is OFF and M2 is ON. Then node N is HIGH, M3 is OFF and the output current I_{OUT} is zero;

(4) Period c: D is HIGH and D_delayed is LOW. M1 is OFF and M2 is ON. Then node N is HIGH, M3 is OFF and the output current IOUT is zero.

Notice that a current pulse is produced only at the falling edge of the data and the current pulse is used to charge the paracitic capacitors and pull the switchable current source gate voltage up.

Similarly, the operation of the pull-down circuit can be explained as follows.

(1) Period A: D is HIGH and D_delayed is LOW. M1' is ON and M2' is OFF. Then node N' is HIGH, M3' is ON and the ouput current I_{OUT} is non-zero;

(2) Period a: Both D and D_delayed are HIGH. M1' is OFF and M2' is ON. Then node N' is LOW, M3' is OFF and the output current I_{OUT} is zero;

(3) Period b: D is LOW and D_delayed is HIGH. M1' is OFF and M2' is ON. Then node N' is LOW, M3' is OFF and the output current I_{OUT} is zero;

(4) Period c: Both D and D_delayed are LOW. M1' and M2' are OFF. Then Node N' is LOW, M3' is OFF and the output current I_{OUT} is zero.

A current pulse is produced only at the rising edge of the data and it is used to discharge the parasitic capacitors and pull the switchable current source gate voltage down.

There are some design issues for the above disscussed pull-up/pull-down circuit. First the circuit itself consumes dynamic power. Second, the current produced by M3 and M3' is finite and the speed of the charging/discharging is a concern. Third, since the charging and discharging currents are produced by PMOS and NMOS transistors, respectively, the charge injected onto the capacitors can not be guarranted to be equal to the charge extracted from the capacitors, and the gate voltage change is not symmetrical. This difference should be supplied by the "Buffer" as shown in Figure III.9; and this requires a fast buffer and also more power consumption.

3.4.6 Proposed SCS LVDS Driver with Passive Pull Up/Down Circuit

In stead of using active pull-up/pull-down circuits, we propose to use passive capacitors C_{PP} driven by the input data for the SCS LVDS driver. The schematic of the complete SCS LVDS driver is shown in Figure III.12. The passive pull up/down circuit solves all of the above mentioned issues faced by the active pull up/down circuits. The capacitors C_{PP} driven by the input data are used to pull up/down M1(M2) gate voltage with drastically reduced transition time and to provide coarse control over the gate voltage V_{gate}. As shown in Figure III.12, parasitic capacitor C_{gs}, and capacitor C_{PP} form a capacitive divider. C_{PP} is driven by the input data, therefore M1(M2) gate voltage varies accordingly. The waveforms of the data and the gate voltage V_{gate} are also shown in Figure III.12. It is easy to show that the M1(M2) gate voltage variation ΔV_{gate} can be expressed as:

$$\Delta V_{gate} = \frac{C_{pp}}{C_{pp} + C_{gs}} \cdot V_{DD} \tag{42}$$

where ΔV_{gate} is defined as $\Delta V_{gate} = V_{OFF} - V_{ON}$.

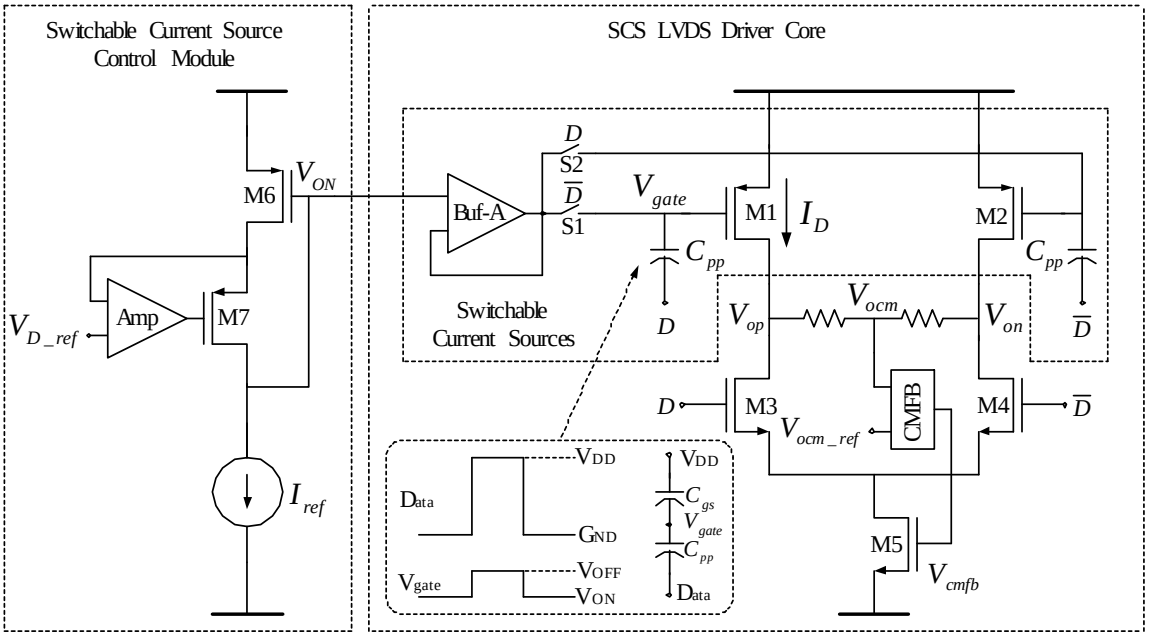

Figure III.12 Schematic of the proposed LVDS driver

It is worth to mention that when the transistor M1(M2) is turned off, its gate voltage V_{OFF} needs not to be V_{DD}; for fast circuits, it is better for V_{OFF} to be lower than V_{DD} such that the transistor operates in subthreshold region. In this way, we can turn on/off the switchable current sources more quickly and also we can minimize the dynamic power consumption needed to charge/discharge C_{pp} and C_{gs}, as long as the current flowing through the "OFF" switchable current source I_{OFF} is negligible (e.g., I_{OFF} is less than 320μA).

By choosing a proper limit for I_{OFF}, we can find the gate voltage variation ΔV_{gate} such that I_{OFF} does not exceed this limit over the PVT variations. Then the value of the capacitor C_{pp} can be determined as:

$$C_{pp} = \frac{C_{gs} \cdot \Delta V_{gate}}{V_{DD} - \Delta V_{gate}} \tag{43}$$

For this design, C_{gs} is 6.4pF and C_{pp} is chosen to be 0.8pF. The current flowing through the "OFF" switchable current source I_{OFF} is around 240μA and ΔV_{gate} is around 200mV under typical corner.

Compared to active pull-up/pull-down circuit [42], this passive pull up/down circuit is faster as a result of the capacitors used, it consumes less power, and the up/down voltage changes are symmetrical. With symmetrical voltage changes, the switches S1 and S2 can be small and the speed of the Buf-A is relaxed. Also the driver's architecture is simpler and so more robust.

3.5. DCS LVDS Driver Circuit Design

3.5.1 DCS LVDS Driver Core and CMFB

The core of the DCS LVDS driver with the source termination resistors is shown in Figure III.13. Since there is enough headroom in the V_{SS} direction, a low voltage, wide swing cascode current mirror is used to generate the tail current such that we can have a good control over the output voltage swing. The nominal tail current $2I_b$ is chosen to be 12.8mA. With a 100Ω source termination and 100Ω receiver termination, the nominal voltage swing is 320mV.

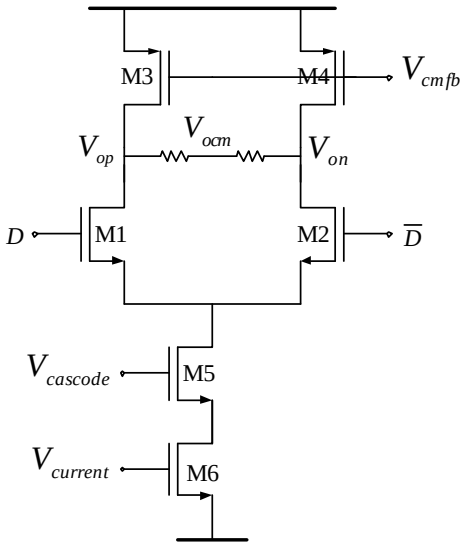

Figure III.13 DCS LVDS driver core

The transistor dimensions of the LVDS driver core are summarized in Table III.2. The transistor's gate-source parasitic capacitances are also included in the table. Because of the large bias current needed, the transistor dimensions are very large, especially for the PMOS current sources.

Table III.2 Transistor dimensions and parasitic capacitances of the DCS LVDS core

Transistor	M1	M2	M3	M4	M5	M6
W/L (μm/μm)	600/.4	600/.4	4000/.4	4000/.4	2000/.4	2000/.4
C_{gs} (pF)	0.96	0.96	6.4	6.4	3.2	3.2

The common-mode feedback of the driver is shown in Figure III.14. It is a simple single-ended differential amplifier. The CMFB tail current is 100μA and its power consumption is quite small.

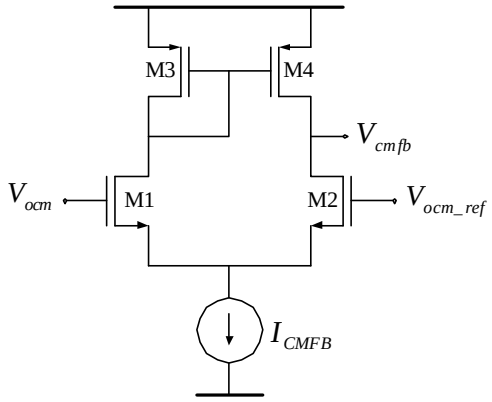

Figure III.14 DCS LVDS driver CMFB

3.5.2 Adaptive Current Generator

Let's consider the double-end terminated LVDS interface as shown in Figure III.1b. R_{T-T} and R_{T-R} are the source end termination and receiver end termination resistors, respectively. While the receiver end termination resistor R_{T-R} is fixed to be 100Ω±1%, as specified in the LVDS standard, the source termination resistor R_{T-T} maybe different from 100Ω if it is realized as an integrated POLY resistor.

In order to have a constant voltage swing regardless of the R_{T-T} variations, it is desired for I_{out} to have two current components: a fixed current I_{fixed} used to produce the desired voltage swing through R_{T-R}, and an adaptive current $I_{adaptive}$ used to produce the

same voltage swing through R_{T-T}. The adaptive current $I_{adaptive}$ can be generated by applying a reference voltage V_{REF} to a reference resistor R_{REF}, which is the same type integrated POLY resistor. The adaptive current $I_{adaptive}$ can be expressed as:

$$I_{adaptive} = \frac{V_{REF}}{R_{REF}} \tag{44}$$

Since R_{REF} varies in the same way as R_{T-T} does under PVT variations, by properly choosing V_{REF} and R_{REF}, the adaptive current $I_{adaptive}$ can produce the same desired voltage swing through R_{T-T}, regardless of the PVT variations.

An adaptive biasing current generator which generates both the fixed and the adaptive currents is shown in Figure III.15. It is used to generate the above described adaptive current I_{out} such that the LVDS driver output voltage swing remains at the same desired level, regardless the PVT variations. The adaptive biasing current generator consists of three parts: an adaptive current source, a fixed current source, and a current summer. The adaptive current $I_{adaptive}$ is generated by applying a reference voltage V_{REF} to a reference integrated POLY resistor R_{REF}. The fixed current I_{fixed} is mirrored from some reference current $I_{reference}$. The two currents are summed together and the sum is then mirrored to the LVDS driver core tail current source.

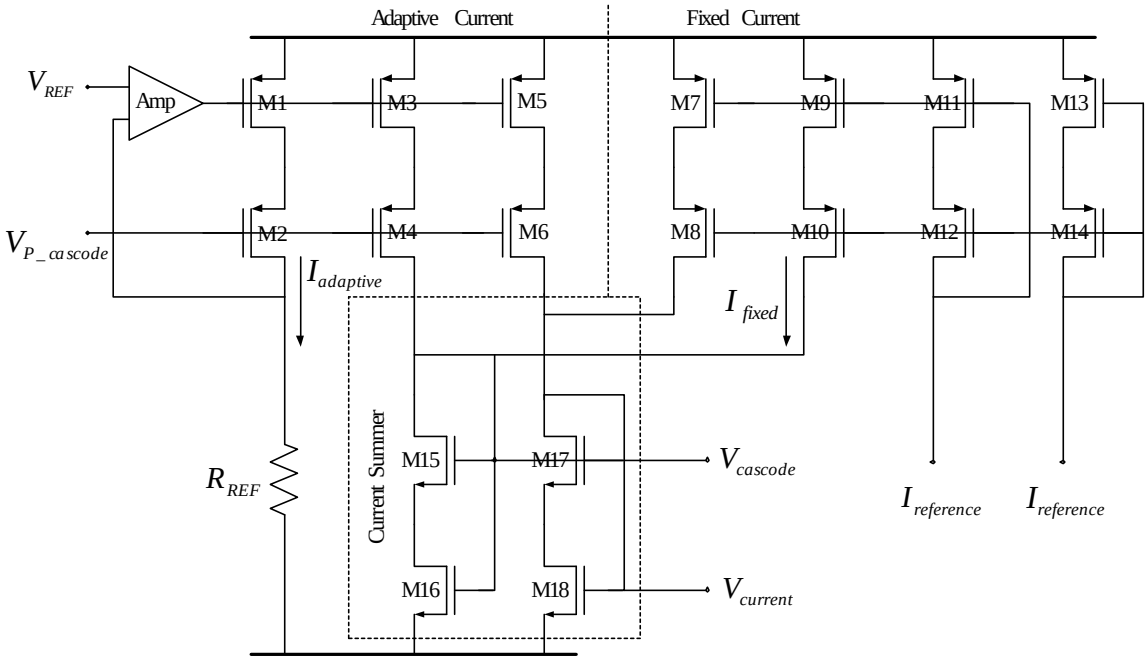

Figure III.15 Adaptive biasing current source

3.6. SCS LVDS Driver Circuit Design

3.6.1 SCS LVDS Driver Core

The schematic of the Switchable Current Sources LVDS driver is shown in Figure III.12. The transistor dimensions and the gate-source parasitic capacitances of the driver's core are summarized in Table III.3.

Table III.3 Transistor dimensions and parasitic capacitances of the SCS LVDS core

Transistor	M1	M2	M3	M4	M5
W/L (μm/μm)	4000/.4	4000/.4	200/.4	200/.4	1000/.4
C_{gs} (pF)	6.4	6.4	0.32	0.32	1.6

The pull-up/pull-down capacitors C_{PP} is chosen to be 800fF. The parasitic capacitance associated with the gate of the switchable current source is around 6.4pF. For a supply voltage of 1.8V, the gate voltage variation ΔV_{gate} is around 200mV and the current I_{OFF} flowing through the "OFF" switchable current source is 240μA under nominal conditions (while I_{OFF} is less than 320μA under all corners). The current I_D flowing through the "ON" switchable current source is mirrored from the reference current I_{ref} and it is 6.4mA. The common-mode feedback is the same as the one used in the DCS LVDS driver.

The buffer-connected amplifier Buf-A isolates the DC voltage V_{ON} from the switches and provides fine adjustment to the switchable current source gate voltage V_{gate}. This amplifier is implemented as a telescopic amplifier as shown in Figure III.16. Telescopic amplifiers have the advantages of high speed and small power consumption compared to typical two-stage amplifiers and folded-cascode amplifiers. Also telescope amplifiers provide high gain. Although telescopic amplifiers connected as unity-gain buffer have limited voltage swing, it is not a problem here, since the positive input of the

amplifier is a DC voltage and the voltage variation at the negative input is relatively small.

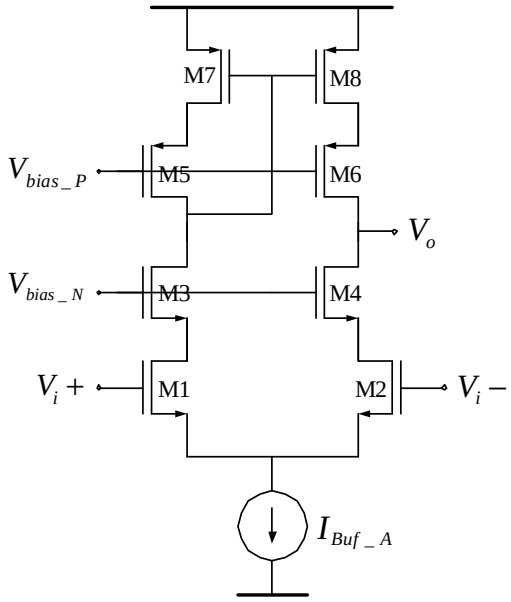

Figure III.16 Telescope amplifier

In order to have a good matching between the reference current I_{ref} and the current I_D flowing through the "ON" switchable current source, it is desired for the amplifier Buf-A to have a high DC gain. Also its offset voltage should be minimized. In this design, the amplifier's DC gain is 52dB. The transistor dimensions of the input transistors M1 and M2 are chosen to be large (1000μm/0.4μm) in order to reduce the offset voltage.

As mention in section 3.4.6, the amplifier Buf-A needs not to be very fast because of the passive capacitors used, but enough transconductance and dc gain are required. The current consumption of the amplifier is 480μA.

3.6.2 SCS LVDS Driver Switchable Current Source Control Module

The switchable current source control module is used to generate a reference current (I_{ref}) dependent voltage V_{ON}. The RGC loop composed of amplifier Amp and transistor M7 is used to set M6's drain voltage to V_{D_ref}. The schematic of the RGC amplifier Amp is shown in Figure III.17. It is composed of two level shifters and a simple differential amplifier. The dc input voltage of the amplifier is high (around 1.41V), and the level shifters are used to shift the voltage down. Since the switchable current source control module is providing a DC voltage V_{ON} and the RGC loop is only used to set M6's drain voltage, its DC gain and unity-gain frequency requirements are quite relaxed. The current drawn by the RGC amplifier is only 30μA. The reference current I_{ref} is generated by an adaptive current generator as discussed in section 3.5.2.

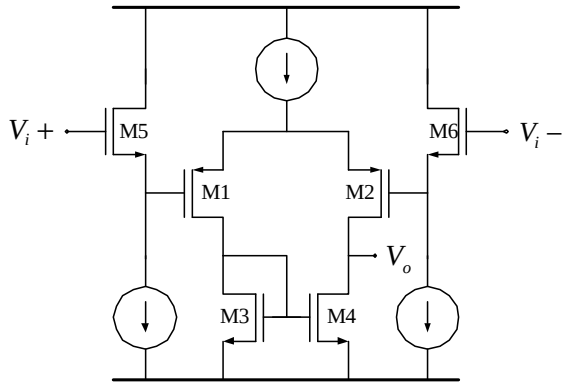

Figure III.17 RGC amplifier

3.7. Simulation Results

The simulation configuration for the DCS and SCS LVDS drivers is shown in Figure III.18. R_{T-T} is the on-chip integrated source termination resistor and R_{T-R} is the termination resistor at the receiver end. The model of the load is shown in Figure III.19. It includes lumped models for the ESD devices, bonding wires, and packages.

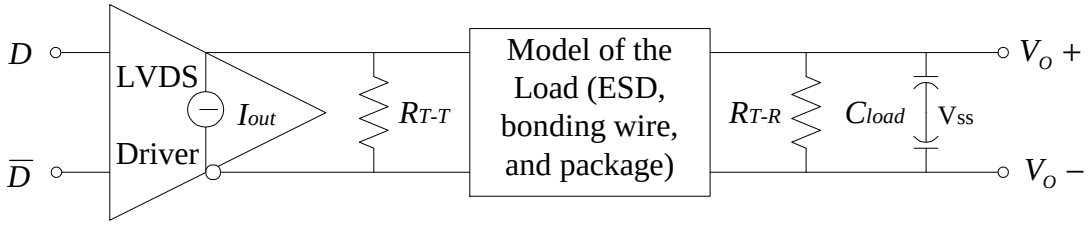

Figure III.18 Simulation configuration for the LVDS drivers

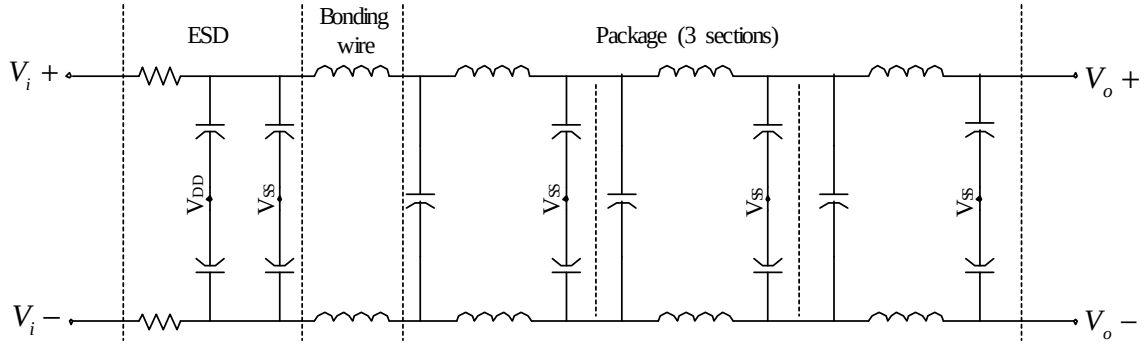

Figure III.19 Model of the load used for simulations

3.7.1 DCS LVDS Simulation Results

Figures III.20 - III.23 show some of the simulation results of the DSC LVDS driver for a data rate of 1.25Gb/s, but with different data patterns. Specifically, Figure III.20 and Figure III.21 show the output differential and common-mode voltages for a data pattern of 101010, with and without the load model, respectively. Without the load model, the output common-mode level presents variations of around 100mV, which is within the specifications (1.125V - 1.375V). The output differential signal swing is around 312mV, which is close to the design value (320mV) and it is also within the specifications (250mV - 400mV). With the load model, the output common-mode level presents variations of around 200mV and it is still within the specifications. While without the load model, the output differential voltage shows no ringing, it shows some ringing with the load model. This is due to the LC tanks in the load model.

Figure III.22 and Figure III.23 show the output differential and common-mode voltages for data patterns of 1111100000 and 100000, respectively, both with the load model. It can be seen that the output differential voltage swings and the common-mode voltage variations are within the specifications for both data patterns.

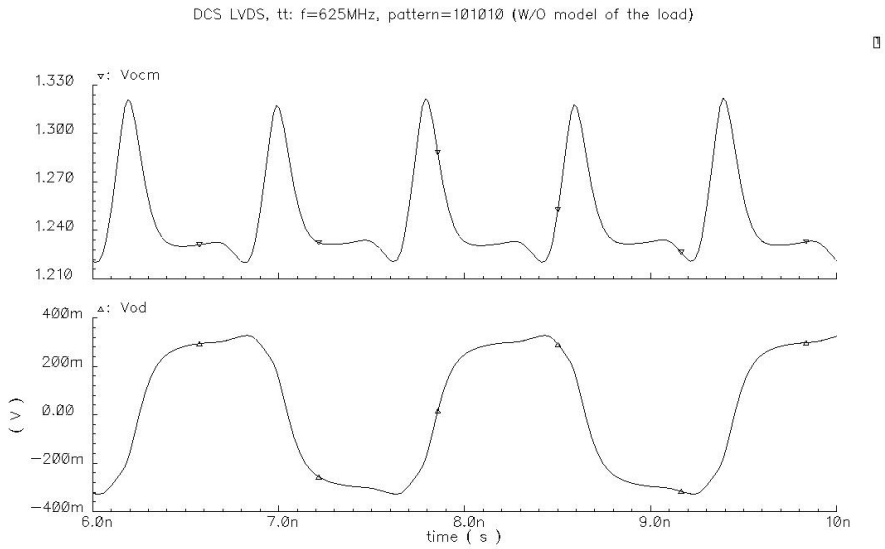

Figure III.20 DCS LVDS driver output waveforms without the load model (101010)

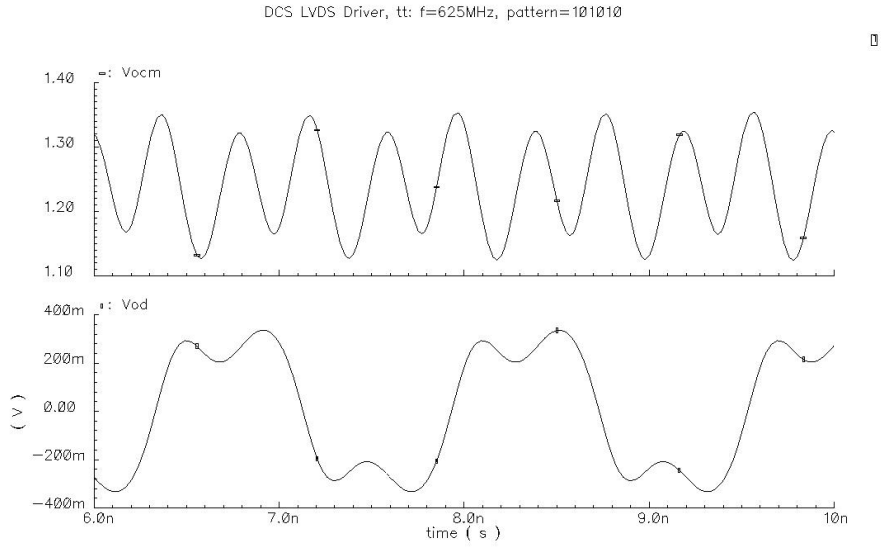

Figure III.21 DCS LVDS driver output waveforms with the load model (101010)

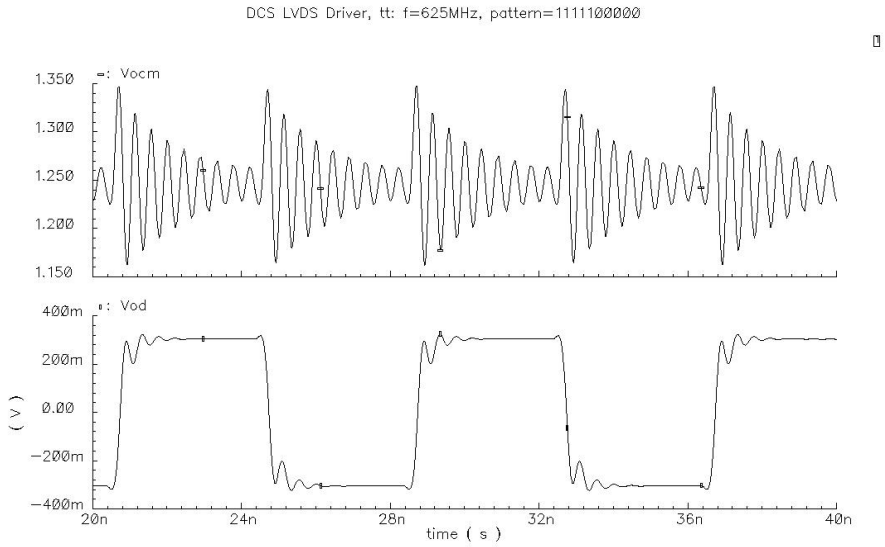

Figure III.22 DCS LVDS driver output waveforms with the load model (1111100000)

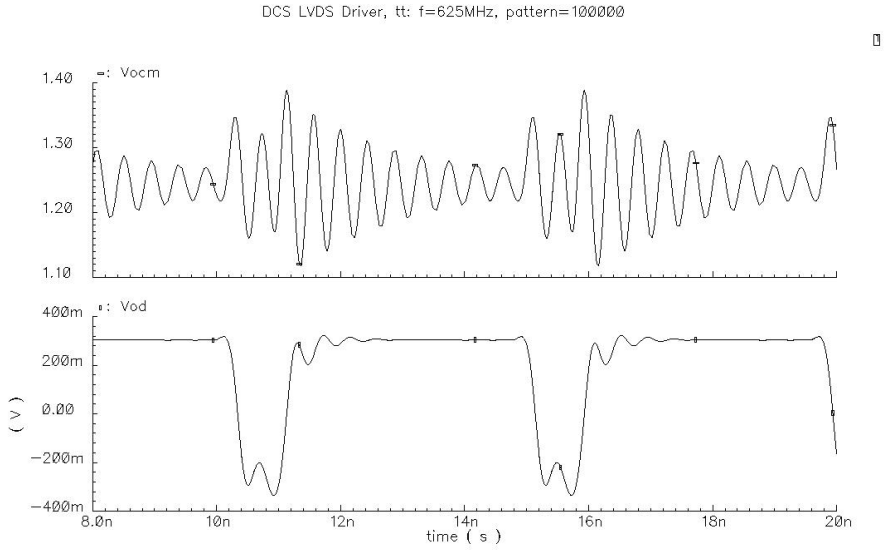

Figure III.23 DCS LVDS driver output waveforms with the load model (100000)

3.7.2 SCS LVDS Driver Simulation Results

From the discussions in section 3.4.4, 3.4.6, and 3.6.1, we know that the key design issue of the SCS LVDS driver is to control the switchable current source gate voltage V_{gate} and so the corresponding drain current properly. Figure III.24 shows the simulation results for the switchable current source gate voltage V_{gate}, transistor drain current $I_D(I_{OFF})$, and the corresponding output differential voltage without the load model. The input data rate is 625Mb/s and the data pattern is 101010. It can be seen that the gate voltage V_{gate} and the corresponding drain current $I_D(I_{OFF})$ changes properly. The transition time is only around 240ps and it can be seen that the rising time and falling time of the output signal are within the specifications (300ps – 500ps). The small transition time is mainly due to the passive capacitors we used for the pull up/down circuit, and operating the switchable current sources in subthreshold region when they are turned "OFF". The gate voltage variation ΔV_{gate} is around 200mV, and the drain current I_D and I_{OFF} are around 6.4mA and 240μA, respectively. Notice that the gate voltage V_{gate} and the drain current I_D present small variations. They are due to the transients of charging/discharging the parasitic capacitances. The output differential voltage changes properly as well, and its voltage swing is around 320mV.

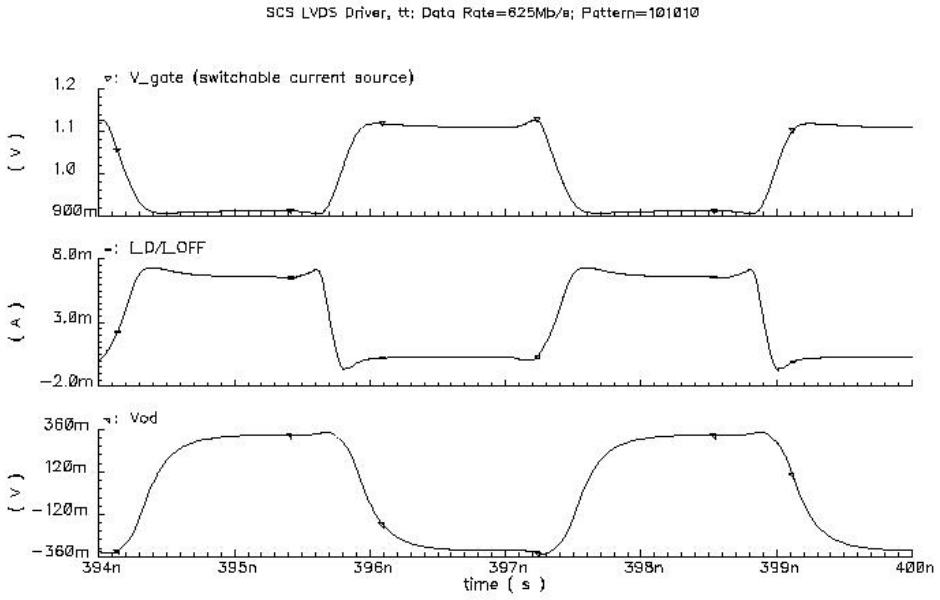

Figure III.24 Switchable current source gate voltage, drain current, and the output differential voltage (101010)

Figures III.25 - III.28 show some of the simulation results of the SCS LVDS driver for a data rate of 1.25Gb/s, with different data patterns. Figure III.25 and Figure III.26 show the output differential and common-mode voltages for a data pattern of 101010, with and without the load model, respectively. It can be seen that both the output differential signal swings and the common-mode levels are within the specifications for both simulations. Similar to the DCS LVDS driver, the SCS LVDS driver output differential voltage shows no ringing without the load model and it shows some ringing with the load model, which is also caused by the LC tanks in the load model. Compared to the simulation results of the DCS LVDS driver, the SCS LVDS driver output signal

presents larger rising time and falling time. This is due to the finite transition time of the gate voltage and drain current of the switchable current sources.

Figure III.27 and Figure III.28 show the output differential and common-mode voltages for data patterns of 1111100000 and 100000, respectively, both with the load model. It can be seen that the output differential voltage swings and the common-mode voltage variations are also within the specifications for both data patterns.

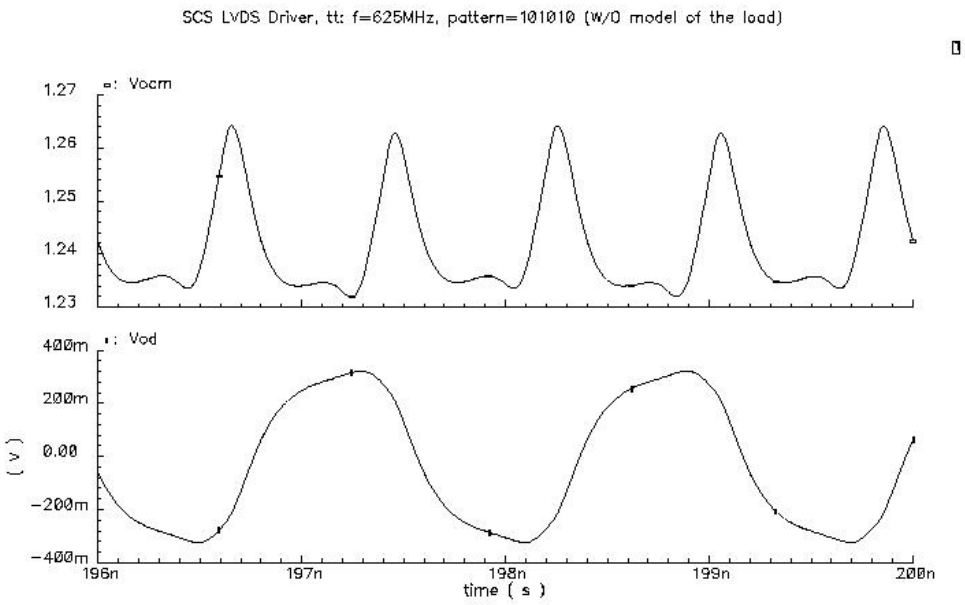

Figure III.25 SCS LVDS driver output waveforms without the load model (101010)

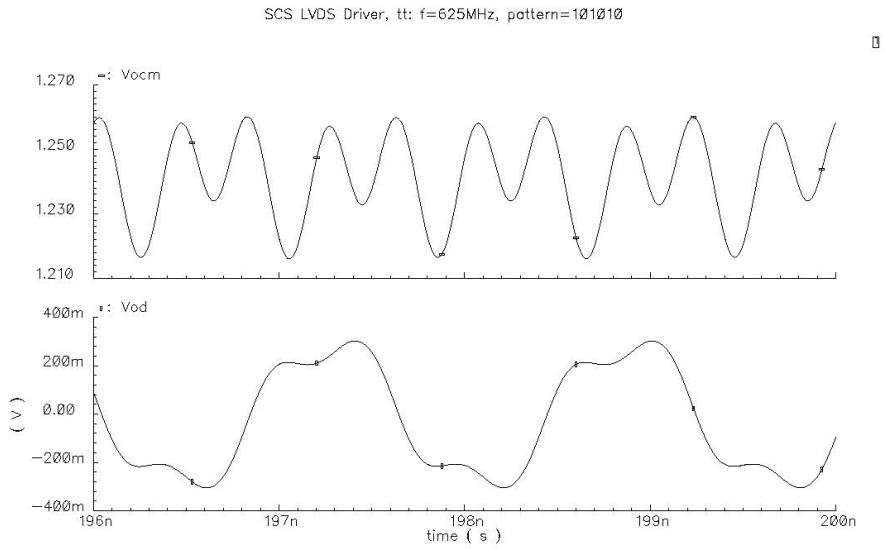

Figure III.26 SCS LVDS driver output waveforms with the load model (101010)

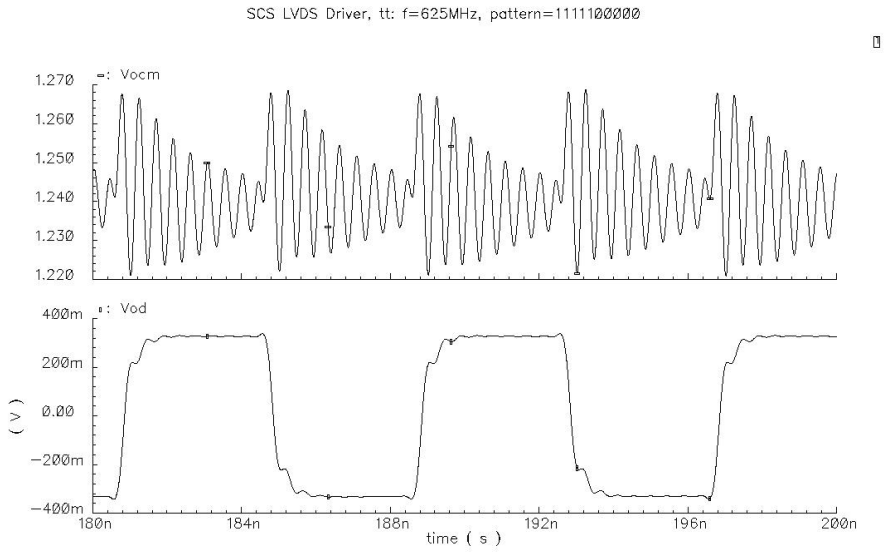

Figure III.27 SCS LVDS driver output waveforms with the load model (1111100000)

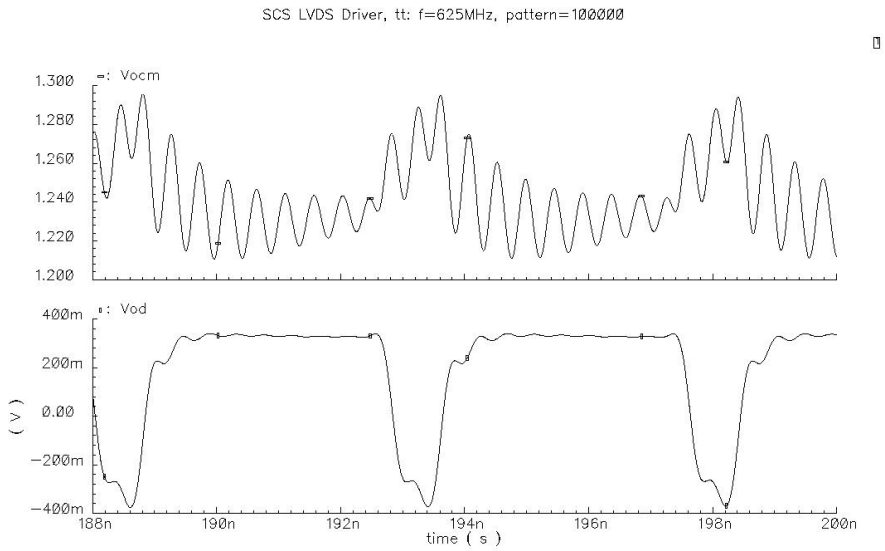

Figure III.28 SCS LVDS driver output waveforms with the load model (100000)

3.8. Experimental Results

Both the DCS and SCS LVDS drivers have been fabricated in a 0.35μm CMOS process through MOSIS service, and the die areas are $0.11mm^2$ and $0.14mm^2$, respectively. The chip micrograph is shown in Figure III.29. The experimental results of the output differential and common-mode voltages as well as the eye-diagrams are shown in the following figures. A Pseudo Random Bit Sequence (PRBS) of 2^{31}-1 was chosen for the eye-diagram testing. According to the experimental results, the DCS LVDS driver can operate properly for a data rate up to 1.4Gb/s and the SCS LVDS drive can operate properly for a data rate up to 1.2Gb/s.

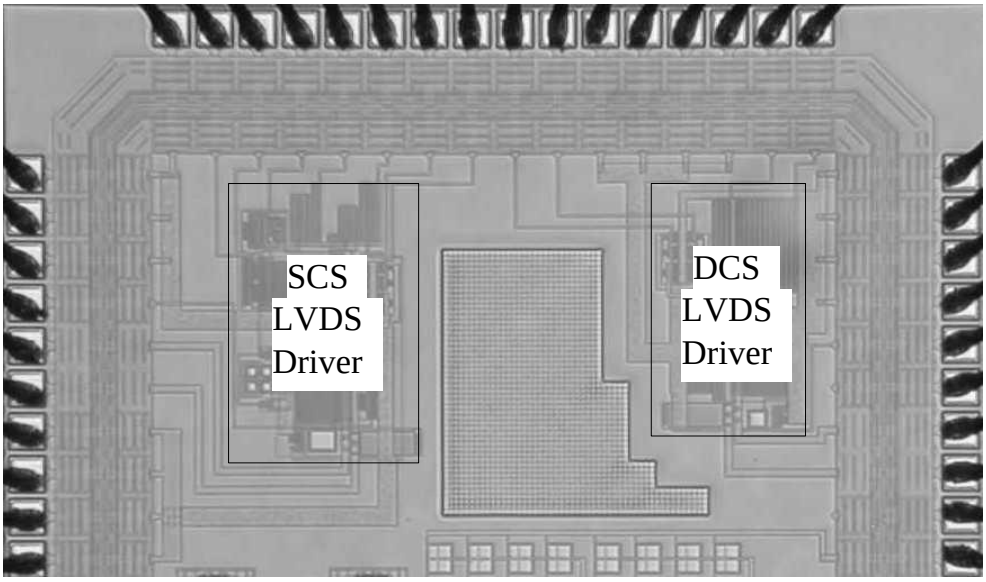

Figure III.29 DCS and SCS LVDS drivers chip micrograph

3.8.1 DCS LVDS Driver Experimental Results

Figure III.30 shows the DCS LVDS driver differential output eye diagram with a 2^{31}-1 PRBS pattern and a data rate of 680Mb/s. The differential output signal swing is around 340mV and the root-mean-square (RMS) jitter is 15ps. It can be seen that the eyes are wide open and the driver works well.

Figure III.31 shows the eye diagram with a data rate of 1.0Gb/s. The differential signal swing is also around 340mV and the RMS jitter is 36ps. Although it presents double traces, which is due to the asymmetry between the two single-ended outputs, the eyes are still wide open and the driver works well.

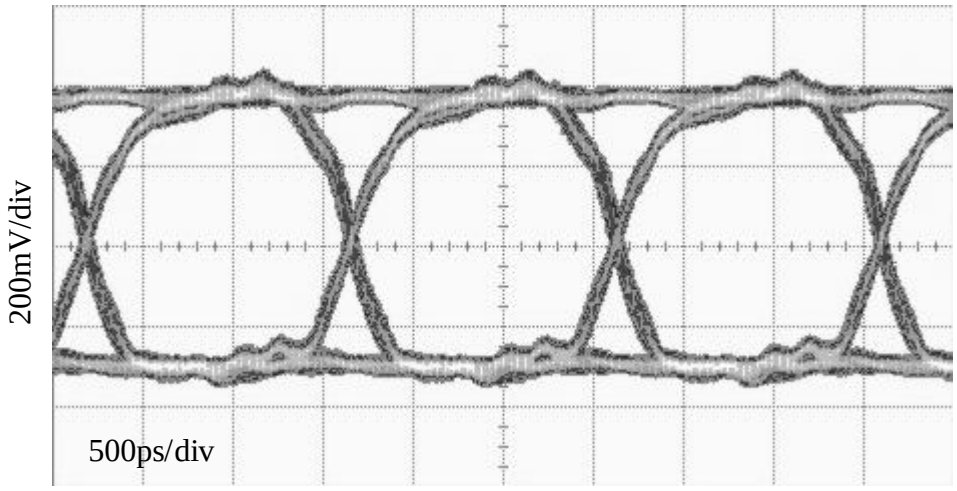

Figure III.30 DCS LVDS driver eye diagram (data rate = 680Mb/s)

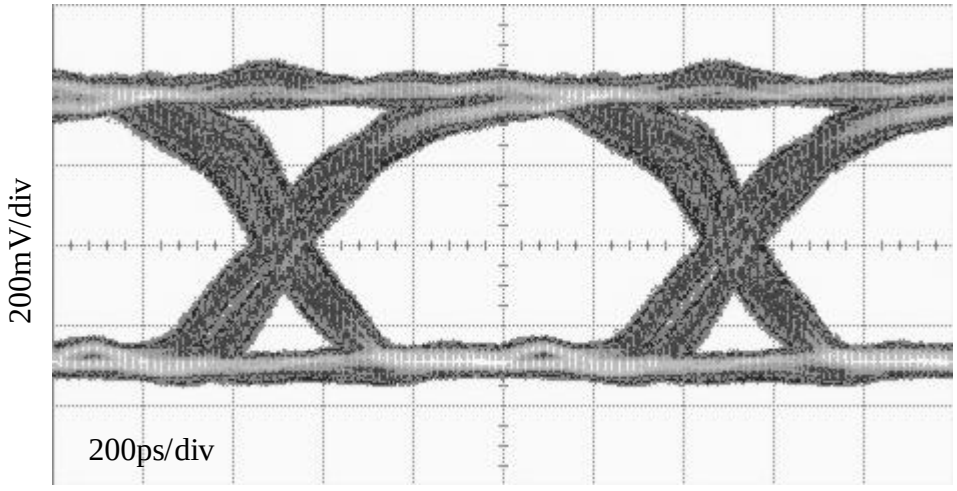

Figure III.31 DCS LVDS driver eye diagram (data rate = 1.0Gb/s)

3.8.2 SCS LVDS Driver Experimental Results

Figure III.32 and Figure III.33 show the SCS LVDS driver eye diagram with a 2^{31}-1 PRBS at data rates of 680Mb/s and 1.0Gb/s, respectively. Their differential output signal swings are 340mV and the RMS jitters are 28ps and 50ps, respectively.

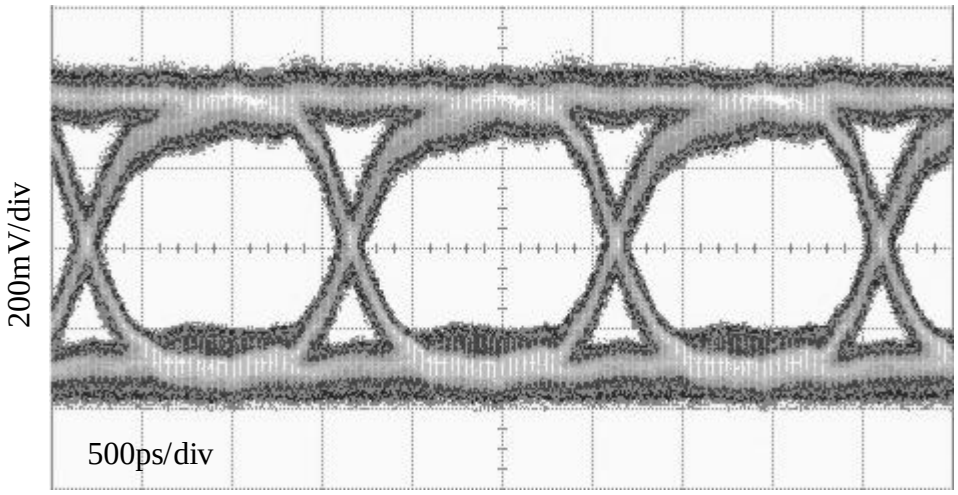

Figure III.32 SCS LVDS driver eye diagram (data rate = 680Mb/s)

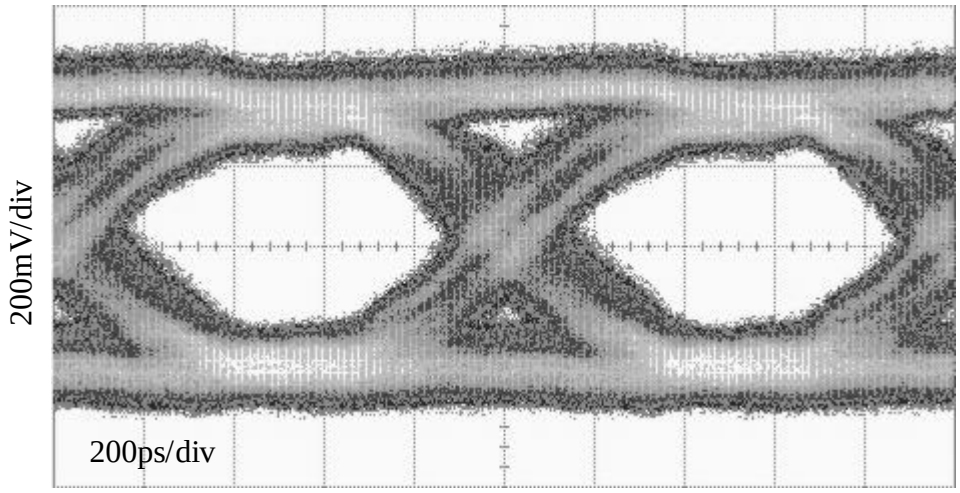

Figure III.33 SCS LVDS driver eye diagram (data rate = 1.0Gb/s)

Compared to the DCS LVDS driver eye diagrams at the same data rates, the SCS LVDS driver eye diagrams present larger jitter and narrower open eyes. Several factors contribute to the performance degradation. First, the rising and falling times of the SCS LVDS driver output signal are larger than those of the DCS LVDS driver output signal, which is discussed in section 3.7.2; larger rising time and falling time cause larger jitter. Second, while the drain current of the PMOS current sources in the DCS LVDS driver keeps constant, the drain current of the switchable current sources in the SCS LVDS driver presents some variations, which was discussed in section 3.7.2, and increases the jitter. Also, the effect of the charge injection on the driver's output nodes is more pronounced for the SCS LVDS driver than for the DCS LVDS driver. While for the DCS LVDS driver only the NMOS switches inject charge onto the output nodes, the PMOS switchable current sources also inject charge onto the output nodes for the SCS LVDS driver. The charge injection affects the differential output signal and it contributes

to the jitter. Taking into count all of the above effects, the SCS LVDS driver still works well for data rates up to 1.2Gb/s.

Figure III.34 shows both differential and common-mode signals for a data rate of 300Mb/s. It can be seen that both differential and common-mode signals are within the specifications. Figure III.35 shows the eye diagram of the SCS LVDS driver with a supply voltage of only 1.6V and a data rate of 800Mb/s. We can see that the driver works pretty well with the very low supply voltage and at a very high data rate.

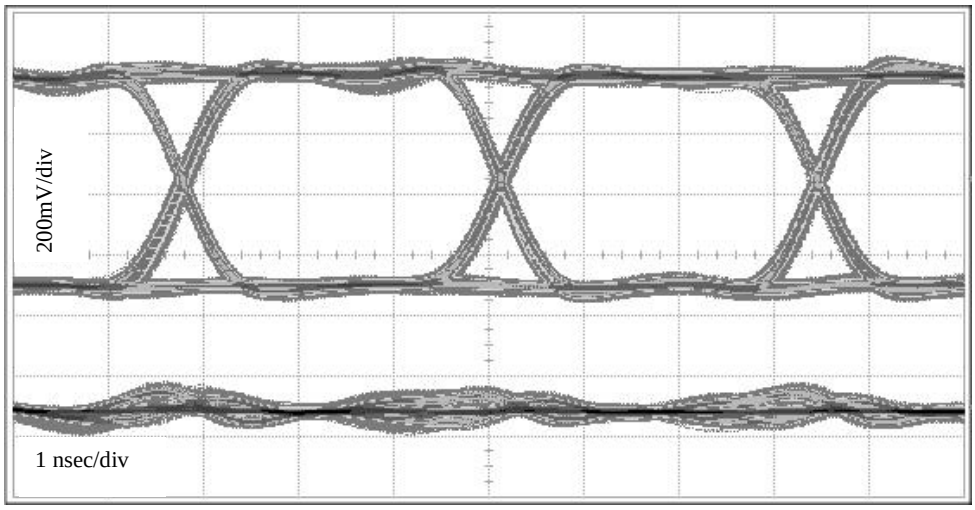

Figure III.34 SCS LVDS driver output signals (data rate = 300Mb/s)
Top curve: Differential signal; Bottom curve: Common-mode signal.

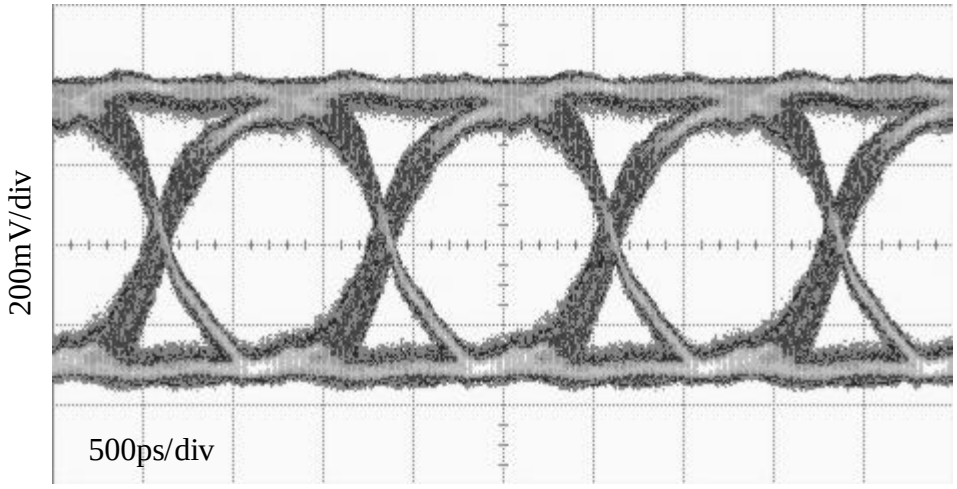

Figure III.35 SCS LVDS driver eye diagram (V_{DD}=1.6V; data rate = 800Mb/s)

3.9. Comparison and Conclusions

Two LVDS driver structures suitable for very low-voltage supplies are discussed. The DCS LVDS driver is simple and fast. If we neglect the dynamic power consumed by the parasitic capacitance of NMOS switches, the DCS LVDS driver power consumption is constant, regardless of the data patterns. A major drawback of the DCS LVDS driver is that its static current consumption is twice the minimum required by the output voltage swing. Another drawback of the DCS LVDS driver is that the transistor dimensions of the NMOS switches and the bottom NMOS current sources are large because of the larger amount of current used, so the die area and the parasitic capacitance are large. If an integrated circuit includes a plurality of LVDS drivers, the increased current consumption and the increased die area maybe unacceptable.

The design of the SCS LVDS driver is more complex compared to the DCS LVDS driver, but its biggest advantage is that the static current consumption is kept to the minimum as required by the voltage swing. Since it is needed to charge/discharge the parasitic capacitance associated with the switchable current sources, the SCS LVDS driver power consumption depends on the data pattern, even if we neglect the dynamic power consumed by the parasitic capacitance of NMOS switches. The higher the data rate, the larger the dynamic power consumption is.

The total current consumption (both static and dynamic) of the two LVDS structures for different data rates is shown in Table III.4. Notice that the dynamic power consumed by the parasitic capacitance of the NMOS switches has been neglected for both structures. While in this table the current consumption of the DCS LVDS driver only

consists the static tail current, that of the SCS LVDS driver includes the current drawn by the buffer-connected amplifier Buf-A, the dynamic current consumed by the parasitic capacitance of the switchable current sources, and the static tail current. It can be seen that for data rates up to 1.2Gb/s, the SCS LVDS driver draws much less current than the DCS LVDS driver.

Table III.4 Current consumption for DCS and SCS LVDS drivers

Data Rate (Mb/s)	625	1200	2000
DCS $I_{average}$ (mA)	12.8	12.8	12.8
SCS $I_{average}$ (mA)	8.4	9.2	10.2

A comparison among these two structures and the previously reported LVDS drivers is shown in Table III.5. It can be seen that both the DCS and SCS LVDS drivers consumes less power than the previous realizations. Especially for the SCS LVDS driver, by dynamically switching the current sources, it reduces the power consumption by 60% compared to the previous implementations if the same signal swing is maintained. In addition, while the previously reported LVDS drivers can not operate properly with low-voltage supplies, both the DCS and SCS LVDS drivers are suitable for low-voltage supply applications, and they are still compliant to the LVDS standards and operate properly at very high data rates.

Table III.5 Comparison with the previous realizations

	[9]	[10]	DCS	SCS
Technology	0.35µm CMOS	0.18µm CMOS	0.35µm CMOS	0.35µm CMOS
Output Voltage Swing (mV)	412	200	320	320
Static Power Consumption (mW)	43	23	23	12.8
Maximum Data Rate (Mb/s)	1200	622	1400	1200
Supply Voltage (V)	3.3	1.8	1.8	1.8

In addition to the low-power consumption, the other benefits of the low-voltage supply drivers are reduced EMI and reduced cost related to the packaging and cooling systems. Being able to operate with low-voltage supplies makes it possible to use the same supply for both the core circuits and the I/O drivers, which can simplify the circuit design as well as the PCB design.

CHAPTER IV

CONCLUSIONS

In this dissertation, two low-voltage, low-power integrated circuits used for data communication systems have been examined. For the low-voltage, low-power continuous-time linear phase filter, the most challenging requirement is the large linear signal swing. A pseudo-differential OTA based on transistors operating in triode region is used to achieve a large linear signal swing. A common-mode control circuit that combines CMFB, CMFF, and adaptive-bias has been proposed to control the OTA's common-mode voltage. Due to the well controlled common-mode behavior, the filter's total harmonic distortion is less than –44dB for a $2V_{PP}$ differential input with a single 2.3V power supply. The ratio of the root mean square value of the ac signal to the power supply voltage is around 31%, which is much better than previous realizations. The principle of the common-mode control circuit can be easily applied to the design of fully differential structures, and it is well suitable for low-voltage pseudo-differential architectures.

Two low-voltage, low-power LVDS drivers used for high-speed point-to-point links have been also examined. While the previously reported LVDS drivers can not operate with low-voltage supplies, the proposed DCS LVDS driver and the SCS LVDS driver are suitable for ultra low-voltage supply applications. While the static current consumption is as twice as the minimum required by the signal swing, the DCS LVDS

driver is simple and fast. The SCS LVDS driver, by dynamically switching the current sources, draws minimum static current and reduces the power consumption by 60% compared to previous realizations. Being able to operate with low supply voltages and reduced power consumption, the EMI can be reduced as well as the cost related to the package and thermal management. Also the circuit and PCB designs can be simplified. The two LVDS drivers are compliant to the standards and can operate at data rates up to gigabits-per-second.

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