MICROWAVE AND MILLIMETER-WAVE MULTI-BAND POWER AMPLIFIERS, POWER COMBINING NETWORKS, AND TRANSMITTER FRONT-END IN SILICON GERMANIUM BICMOS TECHNOLOGY

A Dissertation

by

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ABSTRACT

This dissertation presents new circuit architectures and techniques for designing high performance microwave and millimeter-wave circuits using 0.18-μm SiGe BiCMOS process for advanced wireless communication and sensing systems.

The high performance single- and multi-band power amplifiers working in microwave and millimeter-wave frequency ranges are proposed. A 10-19, 23-39, and 33-40 GHz concurrent tri-band power amplifier in the respective Ku-, K-, and Ka-band using the distributed amplifier structure is presented first. Instead of utilizing multi-band matching networks, this amplifier is realized based on distributed amplifier structure and two active notch filters employed at each gain cell to form tri-band response. In addition, a power amplifier operating across the entire K-band is proposed. By employing lumped-element Wilkinson power divider and combiner, it produces high output power, high gain, and power added efficiency characteristics over broadband due to its inherent low-pass filtering response. Moreover, a highly integrated V-band power amplifier is presented. This power amplifier consists of four medium unit power cells combined with a four-way parallel power combining network.

Secondly, microwave and millimeter-wave power combining and dividing networks are proposed. A wideband power divider and combiner operating up to 67 GHz is developed by adopting capacitive loading slow-wave transmission line to reduce size as well as insertion loss. Also, two-way and 16-way 24/60 GHz dual-band power divider networks in the K/V-band are proposed. The two-way dual-band power divider is realized with a slow-wave transmission line and two shunt connected LC resonators in order to minimize the chip size as well as insertion loss. Furthermore,

a 16-way dual-band power dividing and combining network is developed for a dual-band 24/60 GHz 4×4 array system. This network incorporates a two-way dual-band power divider, lumped-element based Wilkinson power dividers, and multi-section transmission line based Wilkinson structures.

Finally, a K-/V-band dual-band transmitter front-end is proposed. To realize the transmitter, a diplexer with good diplexing performance and K- and V-band variable gain amplifiers having low phase variation with gain tuning are designed. The transmitter is integrated with two diplexers, K- and V-band variable gain amplifiers, and two power amplifiers resulting in high gain, high output power, and low-phase variation with all gain control stages.

DEDICATION

To my beloved wife Mikyung Lee and daughter Minseung Kim and son Ryan Jewoo Kim for all their love and unwavering support

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CHAPTER I

INTRODUCTION

1.1 Background

In the past couple of decades, the wireless communication industry has grown up remarkably in order to satisfy the needs of people. Innumerable applications such as mobile phone, global positioning system (GPS), wireless local area network (Wi-Fi), and Bluetooth devices have become the important part of people's lives. Most of these applications happen in the industrial, scientific and medical frequency band (ISM-band). Due to the explosive number of applications, developing communication systems suffer from overlapping and shortage of available frequencies. The microwave and millimeter-wave frequencies were typically used for military applications. Recently, some of the microwave and millimeter-wave frequencies, especially those in K-band (18-26.5 GHz), V-band (50-75 GHz), and W-band (75-110 GHz) have been utilized for commercial usage. Use of proper microwave and millimeter-wave frequencies can overcome the frequency shortage and overlapping a dilemmas for next generation wireless communication systems.

In the past, microwave and millimeter-wave systems were developed in the realm of compound semiconductors, especially III-V based technologies, due to the superior performance of such devices compared to thoses on silicon technology. During past couple of decades, silicon processes have been evolving considerably and it has led to enhancement of devices and offered the possibility for designing high speed integrated circuits and systems. Using the silicon technologies provides highly integration capability combined digital circuitry with great yields and it makes possible development of a whole system on single-chip. As the reflection of the evolution on the

frequency properties of silicon technologies, many researches have been carrying out to develop microwave and millimeter-wave components and front-end subsystems on silicon. Even though silicon technologies offer their advantages as mentioned above, many challenges need to be confronted to overcome their weaknesses such as lossy substrates and low breakdown voltages. In this context, new design techniques need to be devised to deal with the disadvantages of silicon circuits for better realization.

1.2 Research Contributions

This research aims to investigate the possibility and find new techniques to overcome the challenges encountered the design and implementation of microwave and millimeter-wave circuits and systems in silicon technology. Specifically, single- and multi-band power amplifiers, power combining/dividing structure, and a transmitter front-end in commercial 0.18-μm SiGe BiCMOS process. The design and layout optimization of both passive structures such as transmission lines, capacitors, RF pads, as well as active devices are investigated. Two designed power amplifiers are operating at K- and V-band and one power amplifier are operating at Ku/K/Ka-band concurrently. The power combiners and splitters are also designed for K- and V-band for single as well as dual-band operation. Finally, a dual-band transmitter front-end is presented, which consists of two variable gain amplifiers, two power amplifiers, and two diplexers for concurrent K- and V-band operation.

1.3 Dissertation Organization

This dissertation presents several new circuit architectures and techniques to develop high performance microwave and millimeter-wave circuits using a SiGe BiCMOS process. There are three major parts in this dissertation involving power amplifiers, power combining and dividing networks, and dual-band transmitter front-end. In this context, the dissertation is organized in 10 chapters.

This chapter, Chapter I, begins with an introduction and background information.

Chapters II, III, and IV, the first main parts of the dissertation, present the design of single- and multi-band power amplifiers working in microwave and millimeter-wave frequency ranges. Chapter II begins with designing multi-band amplifier, and then presents complete designs and measurement of Ku-/K-/Ka-band concurrent tri-band power amplifier using the distributed amplifier structure. Design procedure, simulation, and measurement results are discussed. Chapter III covers the design of a power amplifier operating across entire K-band. By employing lumped-element Wilkinson power divider and combiner, it produces high output power, high gain, and PAE characteristics over broadband due to its low-pass filtering response. Chapter IV presents a V-band power amplifier design and measurement. This power amplifier is highly integrated with four medium unit power cells combined by four-way parallel power combining network.

Chapter V and VI, the second major part of this dissertation, cover the design of microwave and millimeter-wave power combining and dividing network. Chapter V presents a wideband power divider and combiner operating up to 67 GHz. The developed power divider adopted capacitive loading slow-wave transmission line to reduce size as well as insertion loss. Simulation and measurement results are also discussed in detail. Chapter VI shows the design procedure and validated measurement results for two-way and 16-way K/V dual-band power divider networks. Firstly, two-way dual-band power divider is explained with design technique, simulated and measured results. After that, 16-way dual-band power dividing and combining network is designed for a 44 array system. This network incorporates two-way dual-band power divider, lumped-element based Wilkinson power divider, and multi-section transmission line based Wilkinson structures. All the measured results for the fabricated

circuit are included.

Chapters VII, VIII, and IX cover the design of the components and integration of a K-/V-band dual-band transmitter front-end. Specifically, Chapter VII describes the design of the constituent microwave filters and K/V-band diplexer along with the simulated and measured data of the diplexer. To realize the diplexer, two different types of bandpass filters are designed and integrated with a T-junction matching network. Specifically, a capacitive coupled 2nd-order Chebyshev bandpass filter and an inductive coupled 2nd-order Chebyshev bandpass filter are designed for K- and V-band operations, respectively. Chapter VIII covers the design topology and techniques as well as the simulated results of variable gain amplifiers working at K- and V-band frequencies. By employing current steering technique with phase compensation capacitor at the gain-control device, the designed variable gain amplifiers provide decent gain tuning range with good return losses and low phase variation while their gain states are varied. Lastly, the integration of the K/V dual-band transmitter front-end is presented in Chapter IX. It consists of the input and output diplexers presented in Chapter VII, K- and V-band variable gain amplifiers described in Chapter VIII, and two power amplifiers described in Chapters III and IV. Finally, a summary of this dissertation is given in Chapter X.

CHAPTER II

A CONCURRENT Ku/K/Ka TRI-BAND DISTRIBUTED POWER AMPLIFIER WITH NEGATIVE-RESISTANCE ACTIVE NOTCH*

In this chapter, a new tri-band power amplifier (PA) on a 0.18-μm SiGe BiCMOS process, operating concurrently in Ku-, K-, and Ka-band, is presented. The concurrent tri-band PA design is based on the distributed amplifier structure with capacitive coupling to enable large device size, while maintaining wide bandwidth, gain cells with the enhanced-gain peaking inductor, and negative-resistance active notch filters for improved tri-band gain response. The concurrent tri-band PA exhibits measured small-signal gain around 15.4, 14.7, and 12.3 dB in the low band (10-19 GHz), midband (23-29 GHz), and high band (33-40 GHz), respectively. In the single-band mode, the PA has maximum output powers of 15, 13.3, and 13.8 dBm at 15, 25, and 35 GHz, respectively. When the PA is operated in dual-band mode, it has maximum output powers of 11.4/8.2 dBm at 15/25 GHz, 13.3/3 dBm at 15/35 GHz, and 8.7/6.7 dBm at 25/35 GHz. In the tri-band mode, it exhibits 8.8/5.4/3.8-dBm maximum output power at 15/25/35 GHz. The concurrent tri-band PA exhibits relatively flat responses in gain and output power across its three frequency bands and good matching up to 40 GHz.

2.1 Introduction

Multiband RF systems provide numerous advantages as compared to their single-band counterparts for communications and sensing. Multiband operation is doubly attractive when all of the multiband functions can be realized within a single system

hardware using concurrent design principle for all constituent components, thus making the entire system not much more complicated than a single-band counterpart. Achieving concurrent functions over multiband enables one single system to be used in multiple bands simultaneously avoiding the need of physically combining separate systems, each working in an individual band together. A multiband system that incorporates several different systems increases the size and complexity, and is difficult and expensive to realize in practiceparticularly when more bands are involved and many systems, such as those in large networks, are needed. The concurrency approach integrates multiband together electrically besides physically. Consequently, the total RF components in a concurrent system employing truly concurrently components remain essentially the same as those for a single-band counterpart, leading to optimum size, cost, power consumption, and ease in realization for the system. Concurrent functions also eliminate some usual components in multiband systems, such as those needed for combining and splitting signals in different bands as used in conventional system architectures, thus enhancing the performance and further reducing the system size, cost, and complexity.

Concurrent multiband power amplifiers (PAs) are the most important component in concurrent multiband transmitters. Concurrent multiband PAs are designed to support multimode (or concurrent modes) in which multiband signals occur simultaneously; yet they can also support single mode in which only the signal in one band occurs at each time. Various approaches for multiband PAs have been reported [1–6]. In [1] and [2], individual PAs were designed for different frequency bands and combined in parallel to achieve multiband operation for the composite PA. This type of multiband PA achieves better performance than other multiband PAs since each individual PA is optimized for each frequency band. However, these PAs have large size, are not cost efficient, and have more complex circuitry due to

the employed combining structures, matching networks, and biasing and switching circuits. Moreover, these PAs cannot support concurrent modes because they operate using bias switching for selected frequency mode. In [3] and [4], reconfigurable matching networks were implemented to realize multiband PAs. These PAs can reduce the number of active devices and have smaller chip size as compared to those in [1] and [2]. The approach in [3] and [4], however, also has the same drawbacks of [1] and [2], in which different control voltages are needed to adjust reconfigurable elements, and hence cannot be operated simultaneously for different signal bands, thereby not supporting concurrent modes.

Concurrent multiband PAs were proposed using multiband input and output matching networks [5, 6]. Using multiband matching reduces the circuit complexity and chip size as compared to the approaches in [1–4]. Multiband matching networks consist of passive elements, such as inductors, capacitors, and resistors, which lead to increased insertion loss, especially for inductors in silicon substrates, and large size when many of them are used. Concurrent multiband PAs with less passive elements in the matching networks are preferred for optimum performance.

In this chapter, a new tri-band PA operating concurrently in three different bands of 10-19, 23-29, and 33-40 GHz is reported. The concurrent tri-band PA is based on the distributed amplifier (DA) structure and realized using a 0.18-μm SiGe BiCMOS process. Specifically, the concurrent tri-band PA implements the active notch filters having negative-resistance property, instead of tri-band matching networks, to achieve the concurrent tri-band operation with a better tri-band gain response resulted from increased quality factor (Q). The simulated and measured small- and large-signal results demonstrate the concurrent tri-band PA's workability not only in tri-band, but also in dual- and single-band.

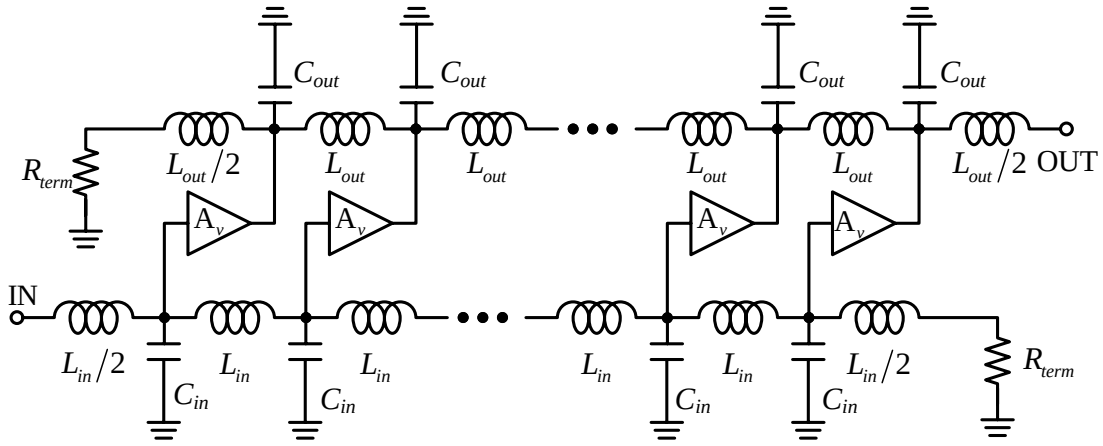


Figure 2.1. Schematic of a conventional DA.

2.2 General Distributed PA Design

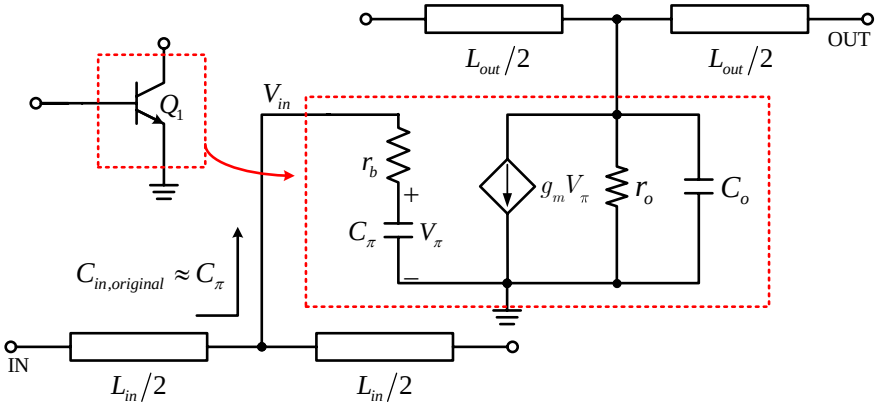
The proposed concurrent tri-band PA is based on the DA structure. Therefore, the design of distributed PAs is briefly discussed first in this section.

2.2.1 Capacitively Coupled DA for Enhanced Power Handling Capability

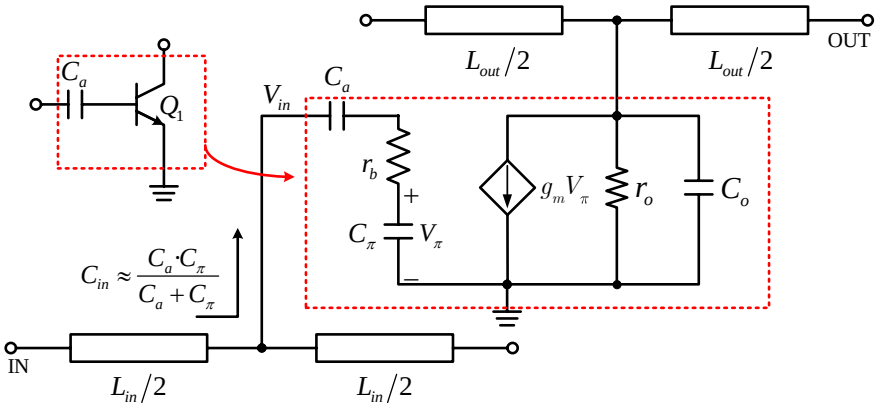
Figure 2.1 shows a basic topology of the DAs, which consists of an input synthetic transmission line represented by inductors (L_{in}, $L_{in}/2$) and capacitors (C_{in}), output synthetic transmission line represented by inductors (L_{out}, $L_{out}/2$) and capacitors (C_{out}), terminating resistors (R_{term}), and gain cells ($Av's$). The cut-off frequency of the input and output synthetic transmission lines can be written as

$$f_c = \frac{1}{\pi\sqrt{L_{in}C_{in}}} = \frac{1}{\pi\sqrt{L_{out}C_{out}}} \tag{2.1}$$

accounting for the required phase matching between these transmission lines. The bandwidth of the DA is proportional to this cut-off frequency, which is, in turn, reversely proportional to the capacitance of the synthetic transmission lines. Since the



(a)



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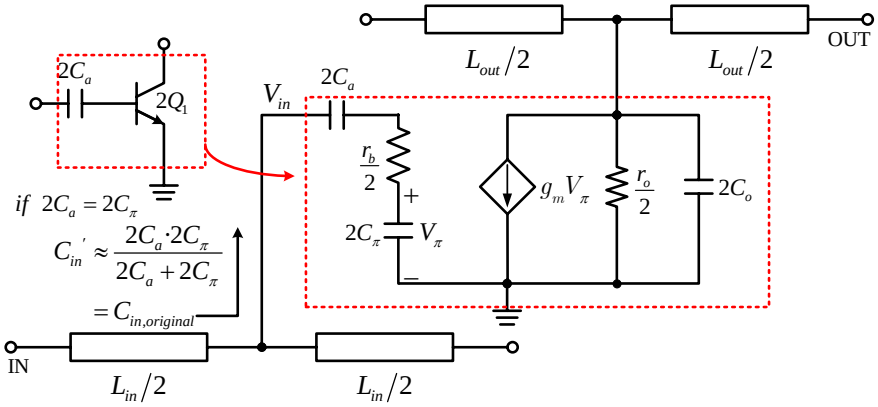


(c)

Figure 2.2. Equivalent circuits of a single-cell DA (a) and capacitively coupled DA: (b) without and (c) with the transistor size and series capacitance doubled.

power handling capability of the DA is proportional to the size of the employed active devices, large devices are needed for high power. Large devices, however, produce large parasitic capacitances, hence inadvertently limiting the DA's bandwidth. The design of a PA based on the distributed topology thus requires a trade-off between the output power and bandwidth. One possible solution for improving the power handling capability without compromising the bandwidth of the distributed PA is implementing a capacitively coupled structure by adding a series capacitor at the input of the gain stage as proposed in [7].

Figure 2.2 shows the equivalent circuits of a single-cell DA and capacitively coupled DA employing a capacitor in series with a common-emitter BJT for two different BJT sizes (Q_1, $2Q_1$) and capacitance values (C_a, $2C_a$). r_b, C_π, r_o, C_o, g_m, represent the series base resistance, emitter-base capacitance, output resistance, output capacitance, and transconductance of the BJT, respectively, that constitute a simplified small-signal equivalent-circuit model for the BJT. For good BJTs, rb is negligibly small, and hence the input capacitance of the BJT's equivalent circuit [Figure 2.2(b)] can be approximately obtained as

$$C_{in} \approx \frac{C_\pi C_a}{C_a + C_\pi} \tag{2.2}$$

The added capacitance (C_a) is in series with the parasitic capacitance (C_π) of the BJT, causing a reduction in the total input capacitance (C_{in}) of the device as can be seen in equation (2.2). The added capacitance also causes a voltage drop across the base terminal as

$$V_\pi = \frac{C_a}{C_a + C_\pi} V_{in} \tag{2.3}$$

When the transistor size is doubled as shown in Figure 2.2(c), its parasitic capac-

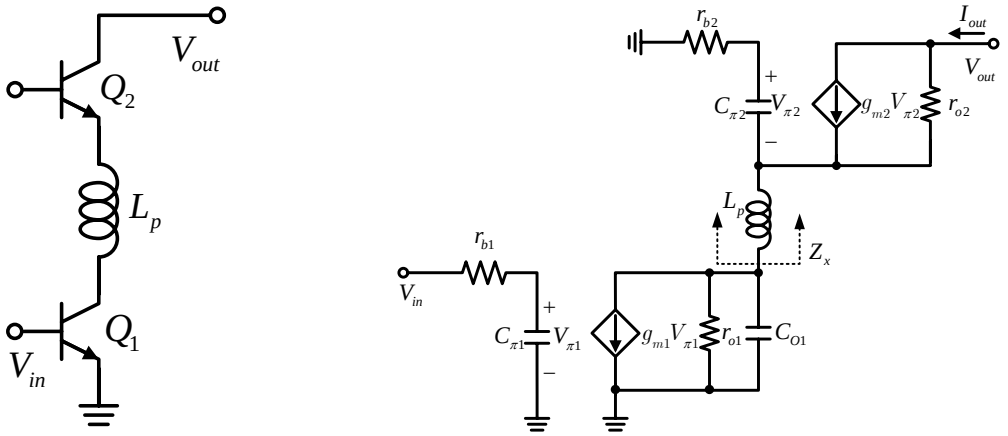
itance also increases approximately twice as much ($2C_\pi$). If an external capacitor having a capacitance of $2C_a = 2C_\pi$ is added to the transistor's input, then the total input capacitance (C'_{in}) would remain the same as the original input capacitance ($C_{in,original}$) of the original device as seen in

$$C'_{in} = \frac{2C_\pi \cdot 2C_a}{2C_a + 2C_\pi} = C_{in,original} \tag{2.4}$$

Equation (2.4) shows that the transistor's size can be increased along with a properly adjusted series capacitor to maintain the overall input capacitance. In other words, increasing the device periphery for high power along with a proper series capacitor does not affect the loading capacitance of the DA's input synthetic transmission line and hence its bandwidth. Each gain cell of the capacitively coupled DA with its transistor size doubled can handle higher input power and produce more output power, while does not affect the DA's operating bandwidth. As seen in equation (2.3), the series capacitor (C_a) acts as a voltage divider and reduces the amplitude of the RF signal at the base terminal, consequently increasing the input power handling capability. For typical BJTs, the output parasitic capacitance is smaller than the input parasitic capacitance, resulting in different phase velocities for the two synthetic transmission lines and hence unmatched phases. A larger device, as desired here, would generate larger output parasitic capacitance, thereby enabling better phase matching between the input and output synthetic transmission lines [7].

2.2.2 Inductive Peaking in Gain Cell for Bandwidth Enhancement

Practical DAs employ a finite number of gain cells to minimize the loss of the passive elements and the parasitics of the active devices, which lead to the optimal number of gain cells for DAs [8]. Four or five gain cells are typically used in recent DAs designed in silicon technology [9]. Several types of gain cells can be used for



(a) (b)

Figure 2.3. (a) Peaking cascode gain-cell with peaking inductor Lp and (b) its equivalent small-signal model.

DAs [10]. The cascode structure has better reverse isolation than the common-emitter and common-source structures, and is chosen as the core for the gain cell in the proposed distributed concurrent tri-band PA.

The cascode structure, however, has a drawback in which the parasitic capacitance at the internal node of the cascode structure creates a pole affecting the bandwidth of the gain cell. To resolve this problem, we utilize the inductive peaking technique [11], [12] to form a peaking cascode gain cell consisting of the basic cascode structure with a series peaking inductor between the common-emitter and common-base transistors. Figure 2.3(a) shows this peaking cascode gain cell and Figure 2.3(b) shows its small-signal equivalent circuit. The transfer function can be written as

$$G_m(s) = \frac{I_{out}}{V_{in}}(s) \quad = \quad -g_{m1} \cdot \left(\frac{1}{sC_{o1}} \parallel Z_x \right) \cdot \left(\frac{g_{m2}}{s^2 L_p C_{\pi 2} + sL_p g_{m2} + 1} \right)$$

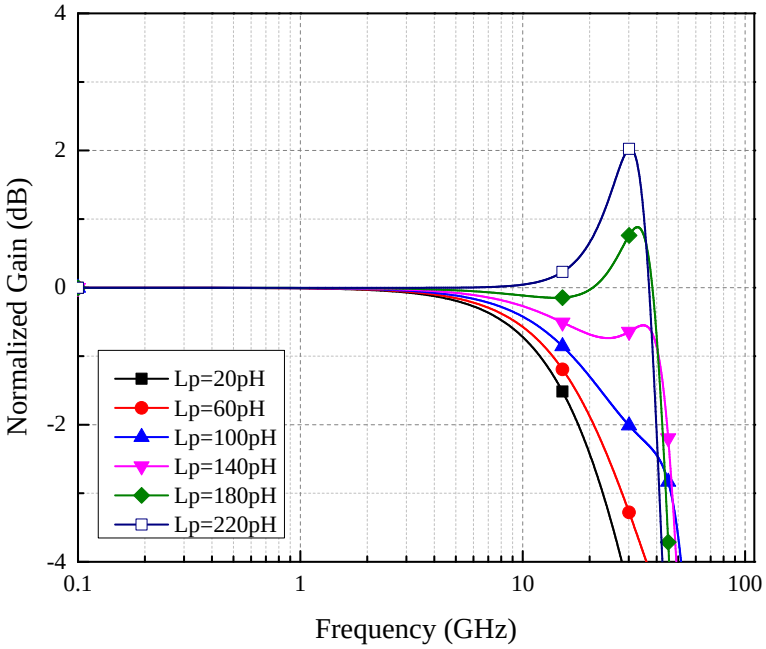


Figure 2.4. Normalized gain versus frequency for various series peaking inductor values.

$$= \quad -g_{m1} \cdot \frac{1}{1 + sC_{o1}Z_x} \cdot \frac{1}{1 + s\frac{C_{\pi 2}}{g_{m2}}} \tag{2.5}$$

where

$$Z_x(s) = sL_p + \frac{\frac{1}{g_{m2}}}{1 + s\frac{C_{\pi 2}}{g_{m2}}} \tag{2.6}$$

This transfer function is based on BJT; a similar expression using MOSFET is presented in [12]. According to equation (2.5), the transfer function of the peaking cascode gain cell has a pole at $\omega_0 = g_{m2}/C_{\pi 2}$ and depends on the impedance Z_x. Due to the existence of L_p, Z_x can cause a resonance with C_{O1}, the output capacitance of Q_1, and produces gain peaking at the resonant frequency ω_p of Z_x and C_{O1} [12]. Figure 2.4 shows the simulated performance of the peaking cascode gain cell with various inductance values for L_p. As can be seen, using large peaking inductor increases the bandwidth and gain peaking. These simulation results show that

the cascode gain cell with inductive peaking technique enables flatter gain response and compensates for the gain drop due to the parasitic elements at high frequencies for the DAs.

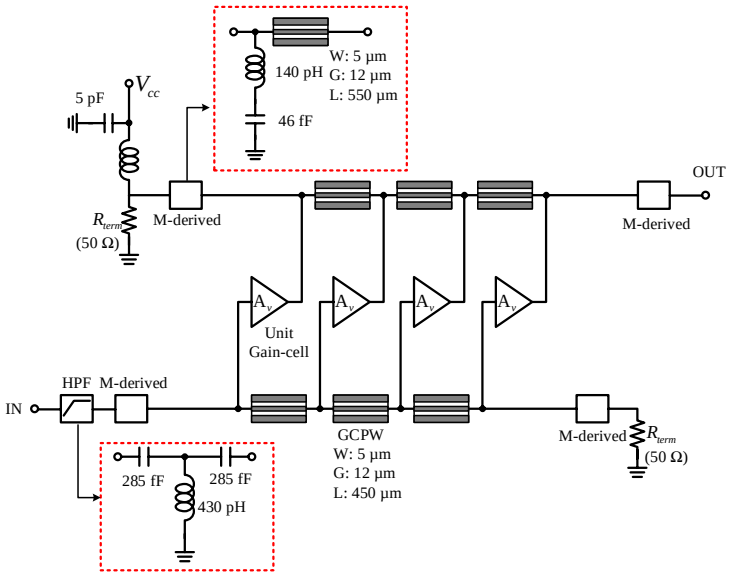
2.3 Design of the Concurrent Tri-Band Power Amplifier

A tri-band PA operating concurrently in three separate bands of 10-19 GHz, 23-29 GHz and 33-40 GHz [13] is designed based on the DA approach discussed in section 2.2 and fabricated using Jazz 0.18-μm SiGe BiCMOS process [14]. Figure 2.5 shows the schematic of the concurrent tri-band PA and one of its gain cells. The concurrent tri-band PA consists of a high-pass filter (HPF) at the input and multiple gain cells, each consisting of a peaking cascode gain cell and two active notch filters at 20 and 30 GHz, and grounded conductor-backed coplanar waveguide (GCPW) simulating inductive transmission lines.

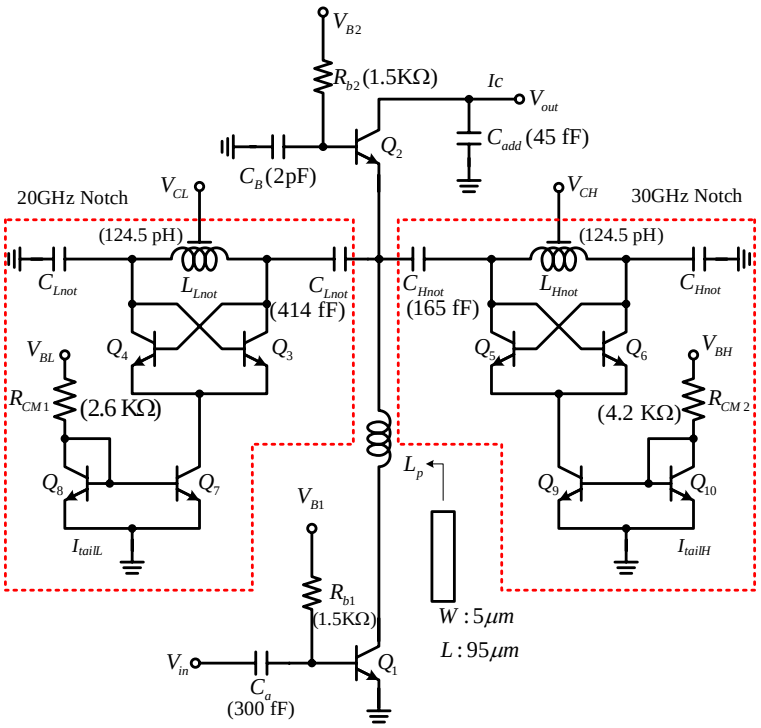
2.3.1 Grounded-Conductor-Backed Coplanar Waveguide

Figure 2.6 shows the GCPW used to realize the inductive transmission lines in the concurrent tri-band PA. The lowest metal layer (M1) is used as the back conductor and substrate shielding. The top metal layer (M6) is used for the signal line and two sided ground planes. The sided ground planes are tied together with the back conductor through vias connecting all the metal layers (M1-M6).

As compared to microstrip line, the GCPW lends itself more freedom in optimizing the transmission-line parameters, such as characteristic impedance and loss, using the width of the signal line and the gaps between the signal and coplanar ground lines, as well as provides more isolation between adjacent lines due to the existence of the coplanar ground lines. The GCPW is also more preferred than the conventional CPW as it can shield the transmission line from the high-conductivity silicon substrate, hence leading to lower dielectric loss which could be substantial

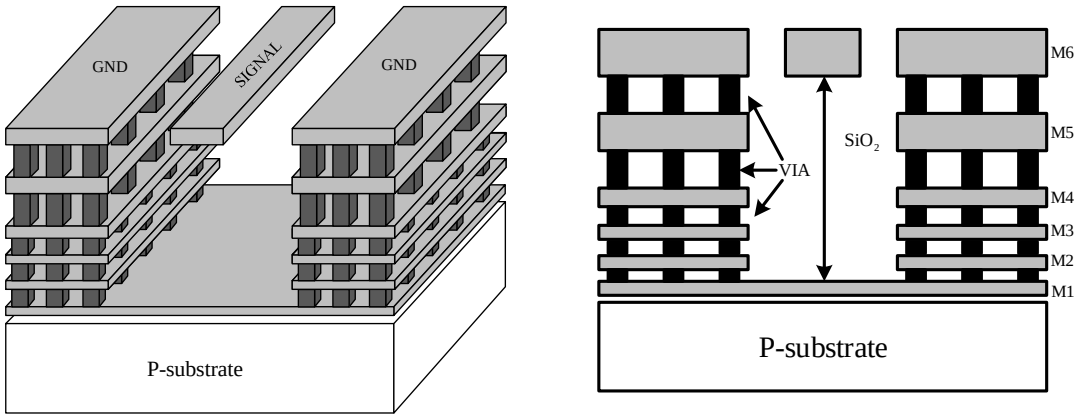


(a)



(b)

Figure 2.5. (a) Schematic of the concurrent tri-band PA and (b) its gain-cell unit.



(a) (b)

Figure 2.6. GCPW: (a) side view and (b) cross section view.

at millimeter-wave frequencies. As compared to the conventional CPW, the GCPW has lower loss, yet also lower characteristic impedance. Moreover, the GCPW implemented on CMOS/BiCMOS process should have a larger gap between the signal and ground lines to maintain the same signal-line width for a given characteristic impedance, and hence the same conductor loss, thereby resulting in a slightly increased size.

Figure 2.7 compares the attenuation constant and characteristic impedance, simulated using IE3D [15], for the CPW and GCPW having the same physical dimensions of 5 μm width, 12 μm gap, and 500 μm length, showing the expected results of less loss and lower characteristic impedance for the GCPW. Such GCPW is used as the inductive transmission lines in the concurrent tri-band PA.

2.3.2 High-Pass Filter

A simple HPF is used in front of the input synthetic transmission line as shown in Figure 2.5(a) to suppress undesired gain at low frequencies below 10 GHz. The HPF has a cut-off frequency of 10 GHz and consists of 3 elements: a 430-pH inductor

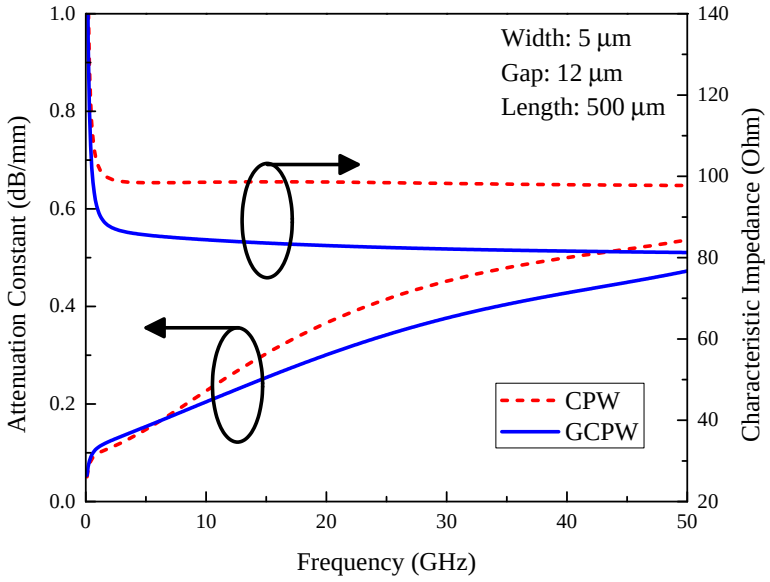
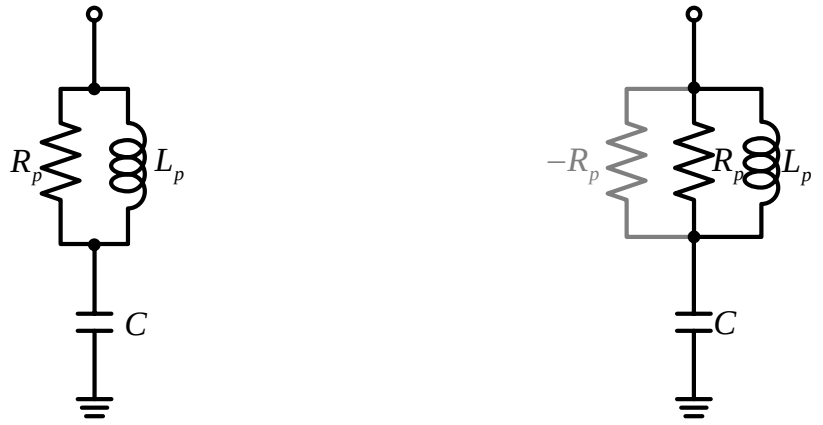


Figure 2.7. Attenuation constant and characteristic impedance of GCPW and CPW.

and two 285-fF capacitors.

2.3.3 Active Notch Filter with Negative Resistance

The tri-band response can be realized by incorporating notch filters at the desired stop-bands. Passive notch filters with high orders can produce large rejection ratios, yet also leading to high insertion loss and large size on silicon. Moreover, as passive notch filters typically consists of inductors and capacitors, the Q of the inductors primarily affect the attenuation characteristics of the notch filters at the notch frequency. Design of high-Q integrated inductors in current CMOS and BiCMOS technologies, however, is challenging, which hinders the design of high-rejection passive notch filters. One possible solution to enhance the Q of integrated inductors is incorporating a negative-resistance circuit whose negative resistance compensates for the loss and hence improves the Q of the inductors. Figure 2.8(a) shows a simple LC notch filter model with a lossy inductor represented by inductance L_p and resis-



(a) (b)

Figure 2.8. (a) LC notch filter model with lossy inductor and (b) active notch filter with lossy inductor and negative resistance.

tance R_p accounting for the inductor's loss. The Q of the inductor, and hence the notch filter, is proportional to R_p and can thus be enhanced significantly by adding a negative resistance close to $-R_p$ in parallel with R_p to form an active notch filter as shown in Figure 2.8(b).

To generate a negative resistance needed to enhance the inductor's Q, a cross-coupled pair of two BJTs is used as shown in Figure 2.5(b). The real part of the input impedance between the two collectors' nodes of the cross-coupled circuit can be derived as [16]

$$R_{in} = -\frac{2}{g_m} \tag{2.7}$$

which shows that a negative resistance can be produced with a cross-coupled transistor pair. Two active notch filters with negative-resistance cross-coupled BJT circuits were designed to have resonance frequencies of 20 and 30 GHz as shown in Figure 2.5(b). To facilitate the formation of a symmetrical structure with the cross-coupled pair, an identical capacitor (C_{Lnot} or C_{Hnot}) is used at each side of a differential

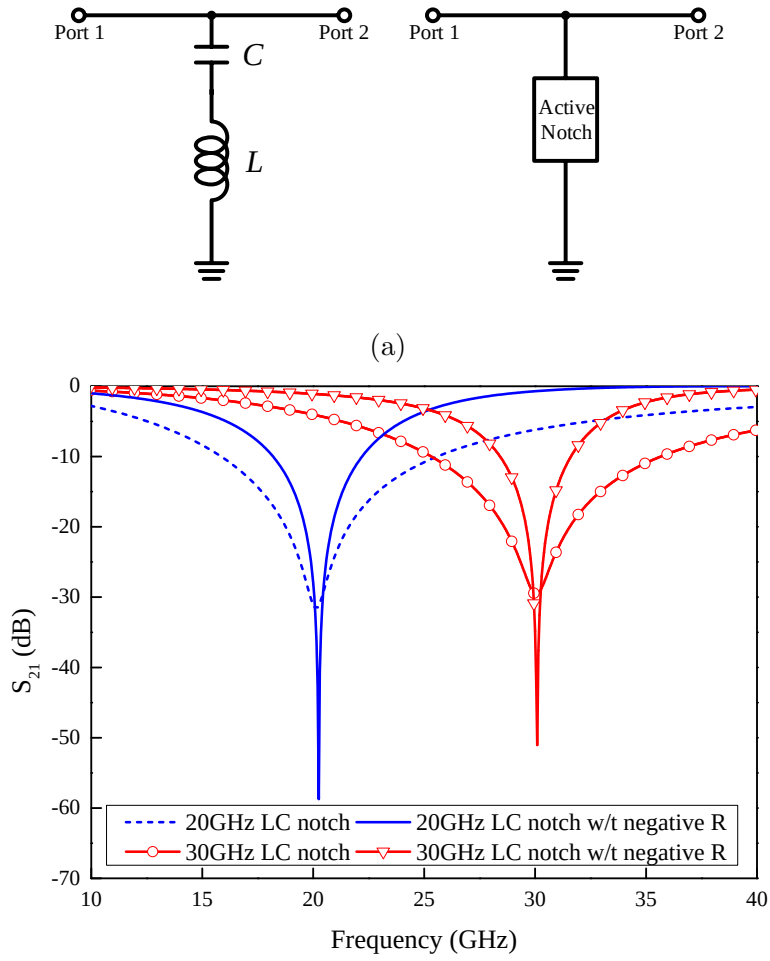


Figure 2.9. 20- and 30-GHz LC passive and active notch filters. (a) Test ports and (b) simulated insertion losses.

inductor (L_{Lnot} or L_{Hnot}) for each negative g_m cell. 414 fF and 165 fF are used for C_{Lnot} and C_{Hnot} of the 20 and 30 GHz notch filters, respectively. Proper device size and tail current of the cross-coupled pairs need to be determined to produce desired g_m. To that end, devices having 0.15 μm emitter width and 2.54 μm emitter length are chosen for both notch filters. The tail current is set by using a current mirror so that the reference current can be duplicated at the common node of cross-coupled

cell using the same device size ($Q_7 = Q_8$, $Q_9 = Q_{10}$). The tail currents for the cross-coupled pairs in the 20 and 30 GHz notch filters are 587 and 388 μA, respectively. With these devices and tail currents, 10.5 mS and 7 mS of transconductance are generated for the 20 and 30 GHz notch filters, respectively.

The design center frequencies of the tri-band PA are about 15, 25, and 35 GHz per our system's specifications. The notch frequencies are around 20 and 30 GHz which are not chosen arbitrarily. This choice is made to produce a symmetrical stop-band at 20 GHz between the first (15 GHz) and second (25 GHz) pass-bands and at 30 GHz between the second (25 GHz) and third (35 GHz) pass-bands, to reject the first pass-band's second harmonic at 30 GHz, and to achieve approximately the same pass-band bandwidth for the three pass-bands (11-19 GHz, 21-29 GHz, and 31-40 GHz).

Figure 2.9 shows the simulation ports and results for the designed passive and active notch filters at 20.3 GHz and 30.1 GHz. It is apparent that the active notch filters having negative-resistance improves the depth as well as the sharpness of the notches as compared to the conventional LC notch filters. The negative resistance generated in the active notch filter by the negative-resistance cell reduces substantially the effect of the inductor loss and consequently enhances the Q of the notch filters.

2.3.4 Concurrent Tri-band Power Amplifier

Figure 2.5(a) shows the schematic of the concurrent tri-band PA. Four identical gain-cells, A_v, are employed along with the GCPW to form the required input and output synthetic transmission lines.

To provide better matching for the synthetic transmission lines, m-derived half section is used at each side of the transmission lines. The series inductors of the

Table 2.1. Transistor sizes and configurations and bias conditions.

Transistor	Emitter width × length - E, B, C finger	Multiplier
Q_1, Q_2	0.15 μm × 4.52 μm - 2, 3, 2	4
$Q_3 - Q_{10}$	0.15 μm × 2.54 μm - 1, 2, 1	1

V_{B1}	V_{B2}	V_{BL}	V_{BH}	V_{CC}	V_{CL}	V_{CH}
1.2 V	2.4 V	2.4 V	2.5 V	3 V	2.4 V	2.4 V

I_C	I_{tailL}	I_{tailH}
21.5 mA	587 μA	388 μA

m-derived half sections are also designed using GCPW for better integration with the GCPW of the synthetic transmission lines. The shunt inductors, however, are realized using spiral inductors to reduce the overall chip size. Figure 2.5(b) shows the schematic of each designed gain cell. The gain cell is based on a cascode structure with gain-peaking series inductor incorporating two active notch filters at 20 and 30 GHz. The employed SiGe HBT transistors have breakdown voltages of $BV_{CEO} = 1.9$ V and $BV_{CBO} = 5.8$ V with peak f_t of 200 GHz and f_{max} of 180 GHz. Table 2.1 shows the sizes, configurations, and bias voltages and currents of the employed transistors. The transistors (Q_1, Q_2) of the cascode cell have an emitter area of $0.15 \times 9.04\ \mu m^2$ and the current density of the device is $4mA/\mu m^2$. The active notch filters provide the necessary tri-band function with good response for the concurrent tri-band PA. The gain-peaking inductor is implemented using microstrip line. The input series capacitor (C_a) helps reduce the total input capacitance of the gain-cell unit and enables large device periphery to be used, hence resulting in improved power handling capability. The value of C_a is 300 fF and almost the same as the overall input capacitance of Q_1. Four transistors, each having $0.15\mu m$ emitter width

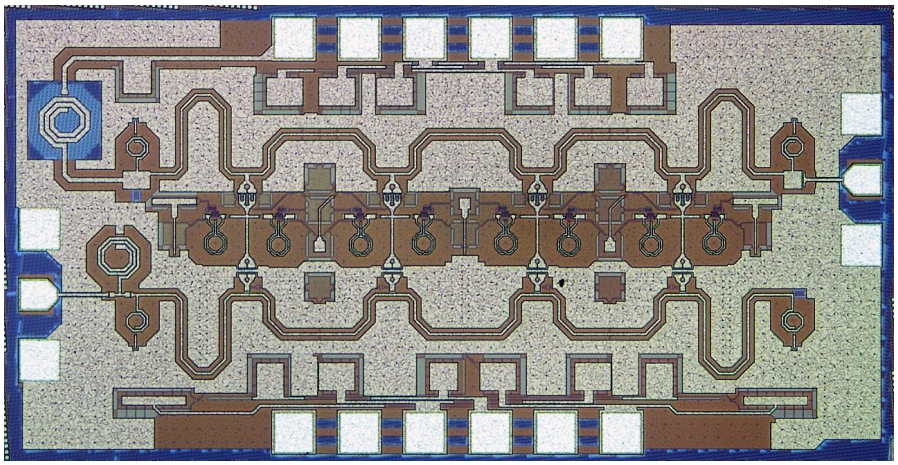


Figure 2.10. Photograph of the fabricated concurrent tri-band PA.

and $4.52\mu m$ emitter length, are combined to generate each device (Q_1 or Q_2) in the cascode cell. The additional shunt capacitor (C_{add}) is used at the output node to achieve phase matching between the input and output synthetic transmission lines. This is necessary since the output parasitic capacitance of BJTs is typically smaller than the input parasitic capacitance. C_{add} is absorbed into the parasitic of the output synthetic transmission line.

All of the passive elements were simulated and optimized using the EM simulator IE3D [15]. Figure 2.10 shows a photograph of the concurrent tri-band PA, which occupies a die size of $2mm \times 1mm$ including the RF and DC pads. The RF pad has $90\mu m \times 75\mu m$ for the signal pad and $100\mu m \times 100\mu m$ for each of the ground pads with $150\mu m$ pitch. The ground pad is implemented with six metal stacks (M1-M6) while the signal pad uses only the two topmost metals (M5-M6). The size of the DC pads is $100\mu m \times 100\mu m$ for each pad with $150\mu m$ pitch.

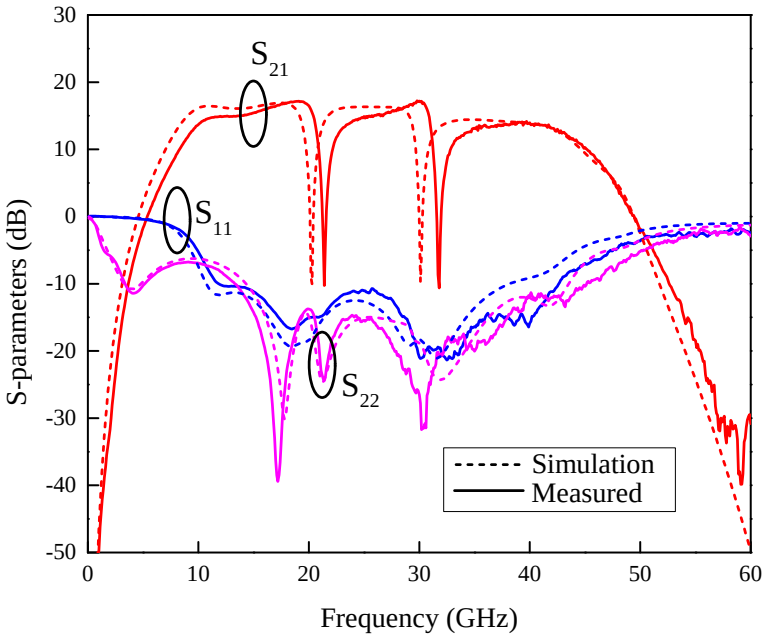


Figure 2.11. Measured and simulated S-parameters.

2.4 Simulation and Measurement Results

Small-signal performance based on S-parameters and large-signal responses were simulated and measured on-wafer. The large-signal characterizations include single-, dual-, and triple-band mode in which signals in one, two, and three bands were used as the input, respectively.

2.4.1 Small-Signal Performance

Figure 2.11 shows the simulated and measured S-parameters of the concurrent tri-band PA, which are well matched to each other. Table 2.2 summarizes the results. The gain differences between the simulation and measured results are due to the change of the notch frequencies. The simulated notch frequencies are 20.3 and 30.1 GHz, whereas those measured are 21.4 and 31.8 GHz. Since the resonance frequencies of the two notch filters shift up, the gain responses for the mid-band and high-band

Table 2.2. Summary of measured and simulated S-parameters.

	Gain (S21)		
	Low-Band (10-19 GHz)	Mid-Band (23-29 GHz)	High-Band (33-40 GHz)
Simulation (dB)	15.5-16.1	15.3-16.1	13.9-14.2
Measured (dB)	13.7-17.1	13-16.4	10.6-13.9
Gain Variation	< 1.8 dB 0.9dB at 15GHz	< 2.3 dB 1.4dB at 25GHz	< 3.3 dB 1.2dB at 35GHz

	Measured Input and Output Matching
S_{11}	> 10 dB between 11.8 GHz and 42.6 GHz
S_{22}	> 10 dB between 13 GHz and 46 GHz

	Notch Frequency	
	Low-Band	High-Band
Simulation	20.3 GHz	30.1 GHz
Measured	21.4 GHz	31.8 GHz

also move to slightly higher frequencies. Decent gains and input and output matching are obtained in the whole three frequency bands. It is noted that, in general, DAs normally have good input and output matching from DC up to a high frequency. The designed concurrent tri-band PA, however, has a different matching behavior due to the HPF located at the input of the input synthetic transmission line and the on-chip choke inductor that supplies bias at the collector of the upper BJT of each cascode gain-cell. At low frequencies, the input matching follows that of the HPF, whereas the output matching is affected by the choke inductor. Figure 2.12 shows the simulated and measured stability factor (K) of the concurrent tri-band

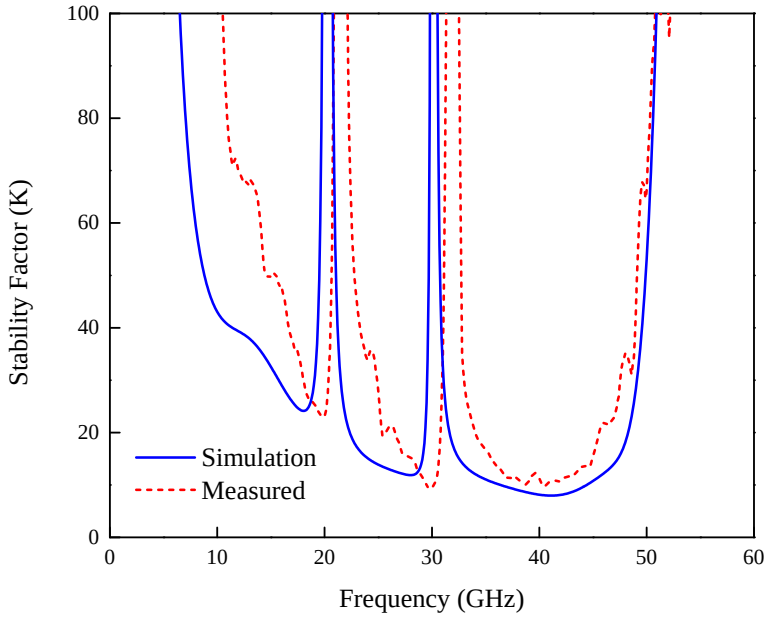


Figure 2.12. Measured and simulated K-factor.

PA, demonstrating its unconditional stability up to 60 GHz. The measured and calculated K's also behave similarly.

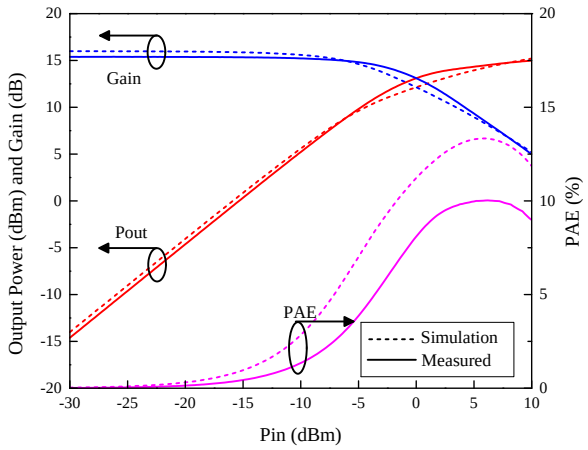
2.4.2 Large Signal Characteristics for Single-band Mode

The large-signal performance of the concurrent tri-band PA under the single-band mode was characterized by using input signal in one of the three frequency bands at a time. Figures 2.13(a), 2.13(b), and 2.13(c) show the simulated and measured output power (P_{out}), power gain, and power added efficiency (PAE) as a function of input power level at 15, 25, and 35 GHz, respectively. As shown in Figure 2.13(a), at 15 GHz, the concurrent tri-band PA exhibits measured maximum output power ($P_{out,max}$) of 15 dBm, 11.4-dBm output power at 1-dB compression point (P_{1dB}), and maximum PAE of 10% at around 5-dBm input power level. The measured power gain and output power are almost the same as the simulation results, but the measured PAE is lower than the simulated one. For the case of 25 GHz as shown in

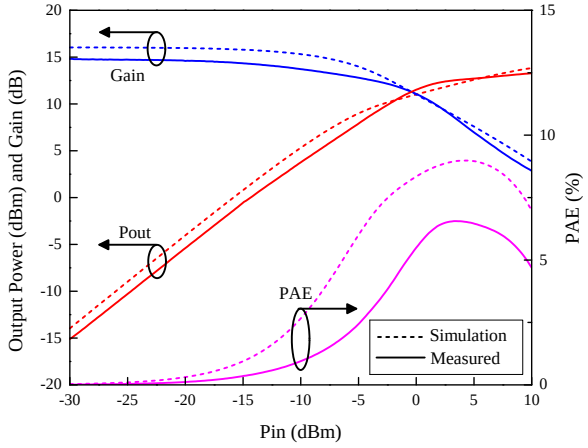
Figure 2.13(b), 13.3-dBm $P_{out,max}$, 3.3-dBm P_{1dB}, and maximum PAE of 6.5 % at around 4-dBm input power were measured. At 35 GHz, the measured results show 13.8-dBm $P_{out,max}$, 0-dBm P_{1dB}, and 7.5% PAE at 6.5-dBm input power. As can be seen at 25 and 35 GHz, the measured and simulated power gain and output power match reasonably well, while the measured PAE decreases from the simulated one. Figures 2.14(a), 2.14(b), and 2.14(c) show the simulation and measurement results for $P_{out,max}$ and P_{1dB} versus frequency in three separate bands.

In the low-band (10-19 GHz), the measured $P_{out,max}$ and P_{1dB} are between 14.4 and 15.4 dBm and 8.2 to 13.1 dBm, respectively. In the mid-band (23-29 GHz), the measured $P_{out,max}$ is between 14 and 14.7 dBm from 25 to 29 GHz, and 9.2 and 11.8 dBm at 23 and 24 GHz, respectively. It is also observed that the P_{1dB} at 23 and 24 GHz are smaller than those at other frequencies. This power-drop phenomenon occurs when the input signal gets closer to the stop-band of the notch. The active notch circuit can degrade the linearity of the amplifier due to the non-linear characteristics of the active devices and, therefore, the Pout and P_{1dB} can be reduced within the active notch circuit's operating region. The P_{1dB} of the PA actually follows the responses of the constituent active notch filters. This phenomenon is also observed at the high-band frequencies as shown in Figure 2.14(c). If the input signal moves closer to 31.8 GHz, which is the designed notch frequency, P_{1dB} decreases. The measured $P_{out,max}$ across the high-band (33-40 GHz) is 13-14 dBm. As can be seen, the measured and simulated $P_{out,max}$ are in good agreement for all bands, except in the mid-band below 25 GHz.

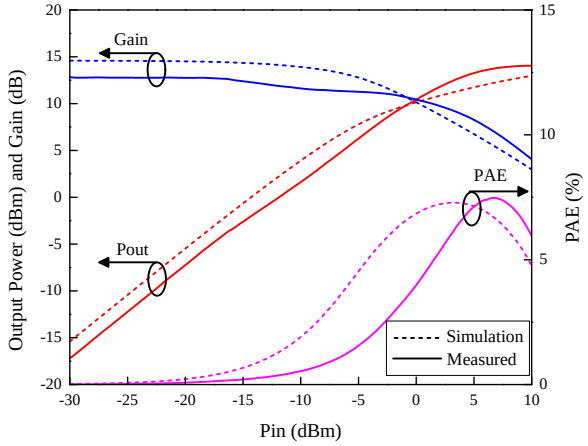
The measured results particularly show that the variation of the $P_{out,max}$ of the designed concurrent tri-band PA over the three different bands is relatively small. It is noted that the measurements of the concurrent tri-band PA in single bands are only for references; this PA is not designed for single-band operation.



(a)

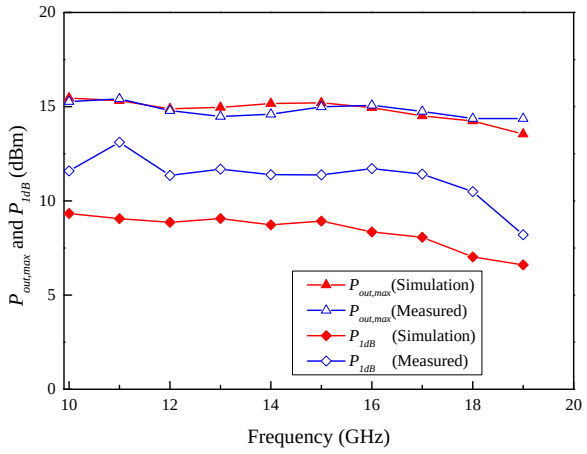


(b)

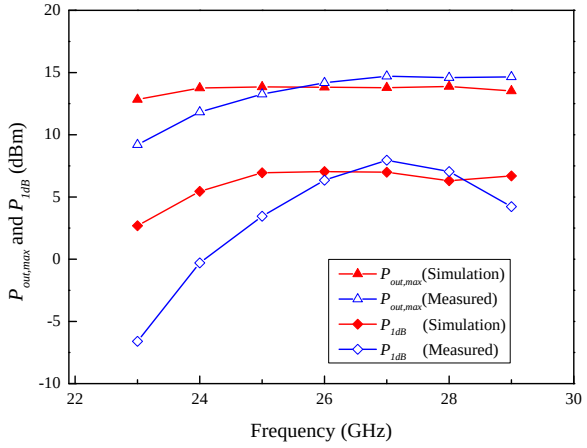


(c)

Figure 2.13. Simulation and measurement results for the single-band mode: P_{out}, gain and PAE at 15 GHz (a), 25 GHz (b) and 35 GHz (c).



(a)



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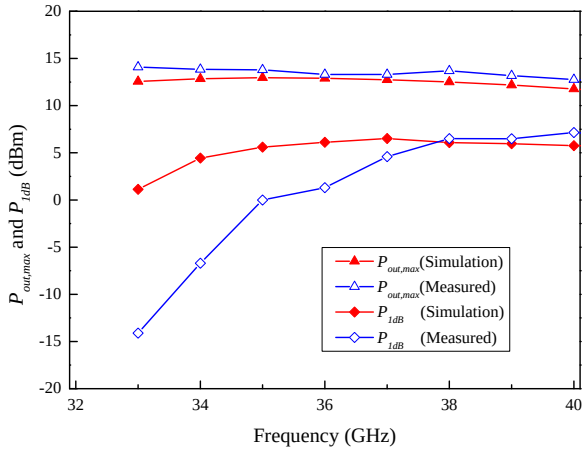


(c)

Figure 2.14. Simulation and measurement results for the single-band mode: P_{out}, gain and PAE for low-band (a), mid-band (b) and high-band (c).

2.4.3 Large Signal Characteristic for Dual-band Mode

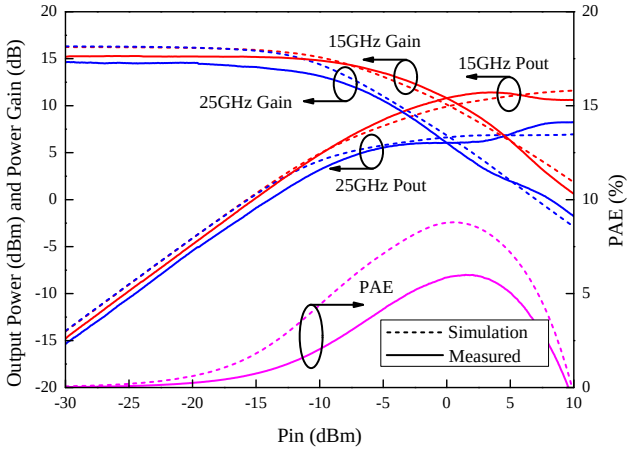
In the dual-band mode, two signals in two different bands are combined internally in the vector network analyzer (VNA) and injected into the input of the concurrent tri-band PA simultaneously. The composite signals used in the measurements are at 15/25 GHz, 15/35 GHz, and 25/35 GHz. Figure 2.15 shows the performance for three cases.

Figure 2.15(a) shows the results for the P_{out}, power gain, and PAE for the first case of the dual-band mode at 15/25 GHz. It is noted that P_{in} in the abscissa is the (equal) input power at each frequency. At 15 and 25 GHz, the measured $P_{out,max}$ are 11.4 and 8.2 dBm, and the P1dB are 7.1 and 1.7 dBm, respectively. As can be seen, the measured and simulated results agree reasonably well. At 1.5-dBm input power, the measured PAE for the 15/25GHz dual-band mode reaches a maximum value of 6%. The PAE for multi-band mode is calculated, taking into account the multiple concurrent signals, as

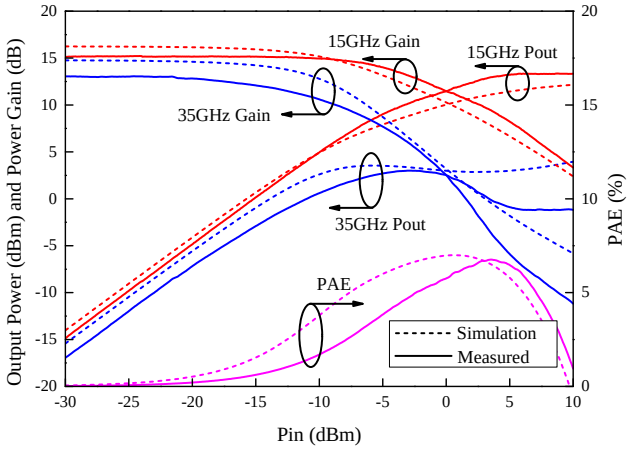
$$PAE(\%) = 100 \times \frac{\sum_{n=1}^{N} (P_{out,n} - P_{in,n})}{P_{DC}} \tag{2.8}$$

where N is the number of the concurrent input signals, $P_{out,n}$ and $P_{in,n}$ are the output and input powers for signal n, respectively, and P_{DC} is the DC power. Figure 2.16(a) displays the output frequency spectrum under the 15/25 GHz dual-band operation when the power for each input signal is -20 dBm. It is observed that undesired signals are suppressed by at least 43 dB from the 15/25 GHz signal.

In the second case, the input signal is formed by two concurrent signals at 15 and 35 GHz. Figure 2.15(b) shows the simulation and measured results. The concurrent tri-band PA achieves measured $P_{out,max}$ of 13.3 and 3 dBm and P_{1dB} of 8.7 and -2.6



(a)



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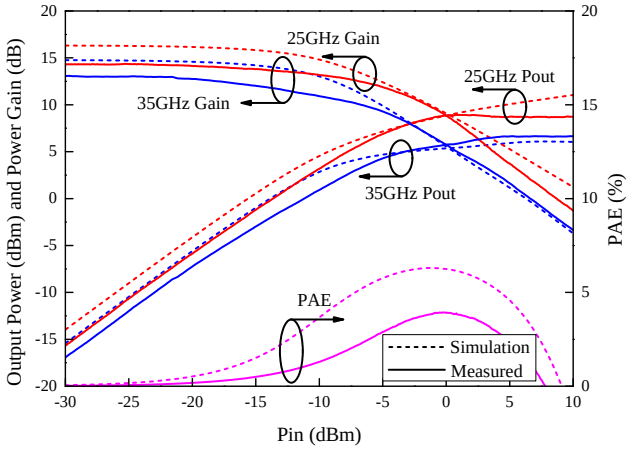
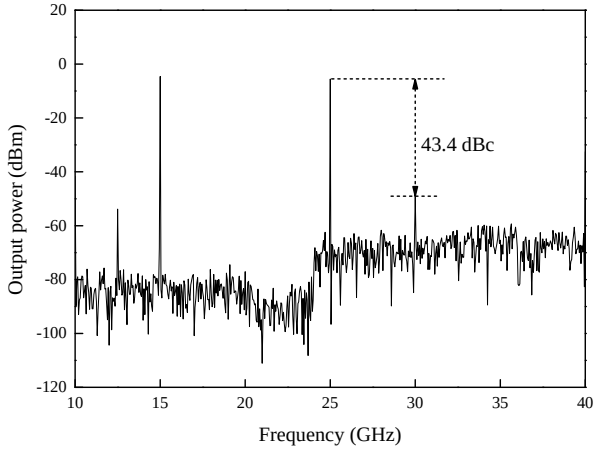
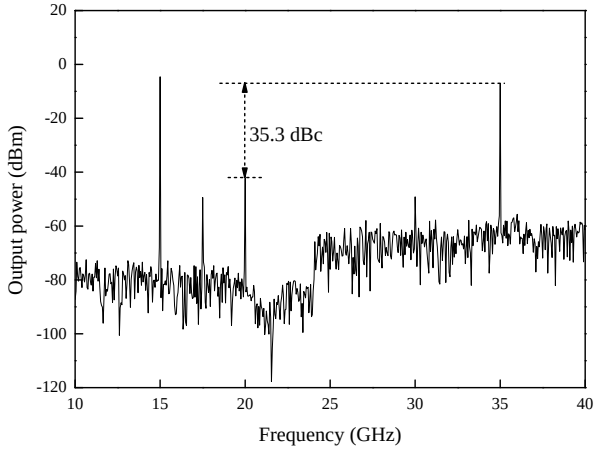


(c)

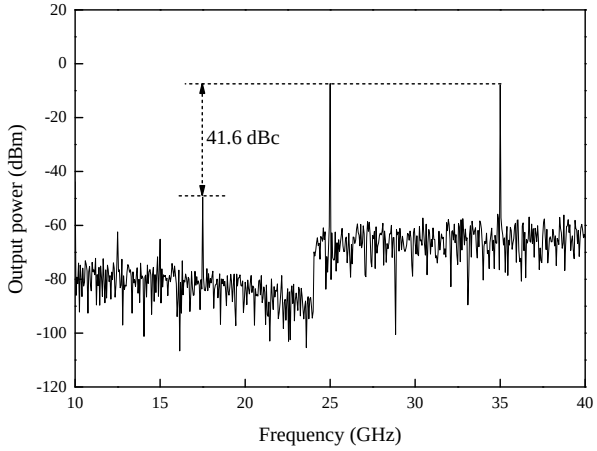
Figure 2.15. Results for dual-band operations: simulated and measured P_{out}, gain, and PAE for 15/25 GHz (a), 15/35 GHz (b) and 25/35 GHz (c).



(a)



(b)



(c)

Figure 2.16. Results for dual-band operations: measured output spectrum at -20 dBm input power for 15/25 GHz (a), 15/35 GHz (b) and 25/35 GHz (c).

Table 2.3. Summary of dual-band performance.

		15/25 GHz	15/35 GHz	25/35 GHz
$P_{out,max}$ (dBm)	Simulation	11.6 / 6.7	12.2 / 3.5	11 / 6.1
	Measured	11.4 / 8.2	13.3 / 3	8.7 / 6.7
P_{1dB} (dBm)	Simulation	4.9 / 3	4.9 / 1.1	3.5 / 1.1
	Measured	7.1 / 1.7	8.7 / -2.6	2.6 / -2.9
Max. PAE (%)	Simulation	8.8	7	6.3
	Measured	6	6.8	3.9

dBm at 15 and 35 GHz, respectively, and maximum PAE of 6.8% at 3.5-dBm input power. The measured output frequency spectrum is shown in Figure 2.16(b) with -20-dBm for each input signal. The suppression of unwanted signals is more than 35 dB.

The third case has 25- and 35-GHz signals combined for the input signal. Figure 2.15(c) shows the simulation and measured results. The measured $P_{out,max}$ and P_{1dB} are 8.7 dBm and 2.6 dBm at 25 GHz, while those at 35 GHz are 6.7 dBm and -2.9 dBm, respectively. The maximum PAE is 3.9 % at -0.2-dBm input power. The output frequency spectrum is shown in Figure 2.16(c) at an input power of -20 dBm, indicating at least 41 dB suppression for undesired signals. Table 2.3 summarizes the simulation and measurement results.

Figure 2.17 shows the frequency spectrums for the three dual-band operation modes at 15/25 GHz, 15/35 GHz and 25/35 GHz for 0- and 10-dBm input power. As can be seen, the amplitudes of the intermodulation tones increase as the input power is increased. Also, the 20- and 30-GHz intermodulation signals are larger than others. This is due to the fact that the measured notch frequencies actually occur at 21.4 and 31.8 GHz, hence causing less rejection at 20 and 30 GHz.

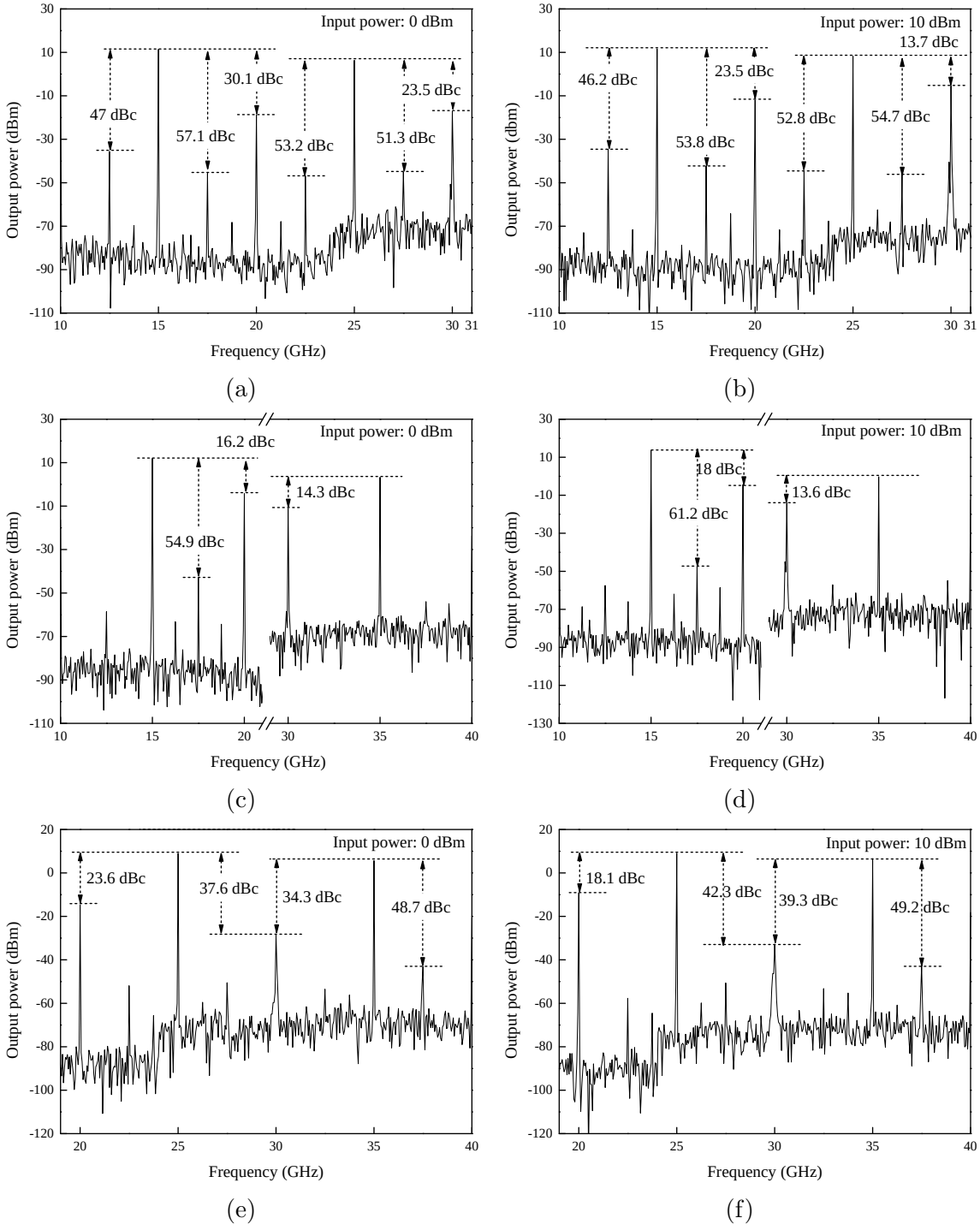
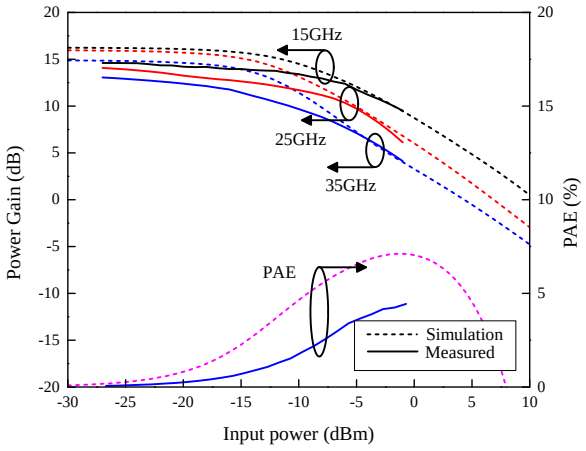


Figure 2.17. Frequency spectrums for dual-band operation modes with 0- and 10-dBm input power at 15/25 GHz (a, b), 15/35 GHz (c, d), and 25/35 GHz (e, f).

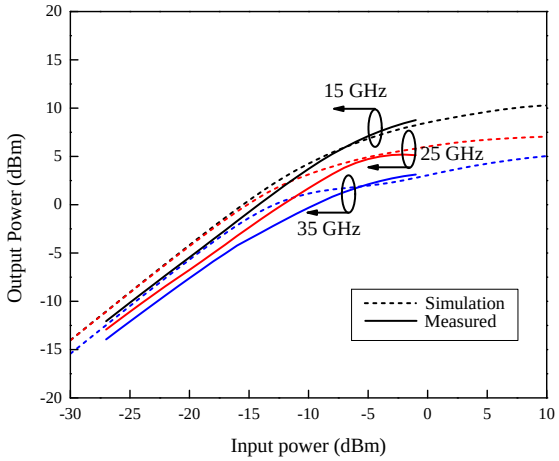
2.4.4 Large Signal Characteristic for Tri-band Mode

Finally, the tri-band mode for the concurrent tri-band PA was measured using the concurrently combined 15/25/35 GHz as the input signal. The 25- and 35-GHz signals provided by the VNA are combined with the 15-GHz signal from an external synthesizer through a 2-50 GHz 13-dB directional coupler. The simulation and experimental results are shown in Figure 2.18. The measured results show $P_{out,max}$ of 8.8, 5.4, and 3.8 dBm, P_{1dB} of 2.9, -5, and -4.9 dBm at 15, 25, and 35 GHz, and maximum PAE of 4.4% at -1-dBm input power, respectively. Figure 2.18(c) shows the measured frequency spectrum of the output signal, showing more than 21 dB suppression of unwanted signals. It is noted that the maximum available input power is limited at -1 dBm due to the limited output power from available sources and use of the 13-dB coupler for signals combination, hence resulting in less output power and PAE. Table 2.4 summarizes the performance under the tri-band operation. Figure 2.19 shows the frequency spectrums for the tri-band operation at 15/25/35 GHz for -9 and -1 dBm input power. Similar to the dual-band operations mentioned earlier, we can see that many unwanted signals are generated and the amplitudes of the 20- and 30-GHz intermodulation tones are larger than others. Table 2.5 compares the measured performance of the designed concurrent tri-band PA for different operating modes.

The designed concurrent tri-band PA does not achieve high PAE performance as compared to single-band PAs operating in the same frequency ranges, mainly due to the fact that it is not optimized for single-band operations. Moreover, the design of multi-band PAs having high output power over the entire multiple bands with decent PAE is very challenging. The PAE of the proposed tri-bane PA, however, could be improved by modifying its topology and design - for instance, using different appro-



(a)



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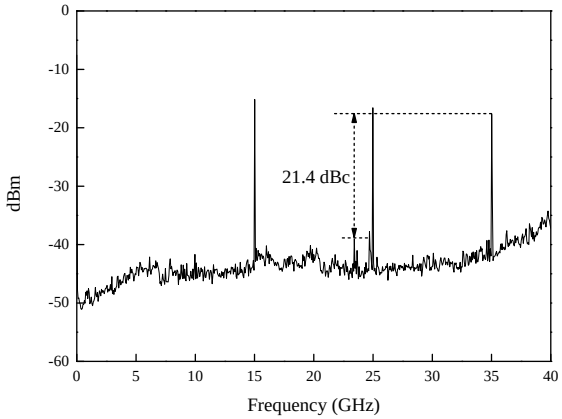
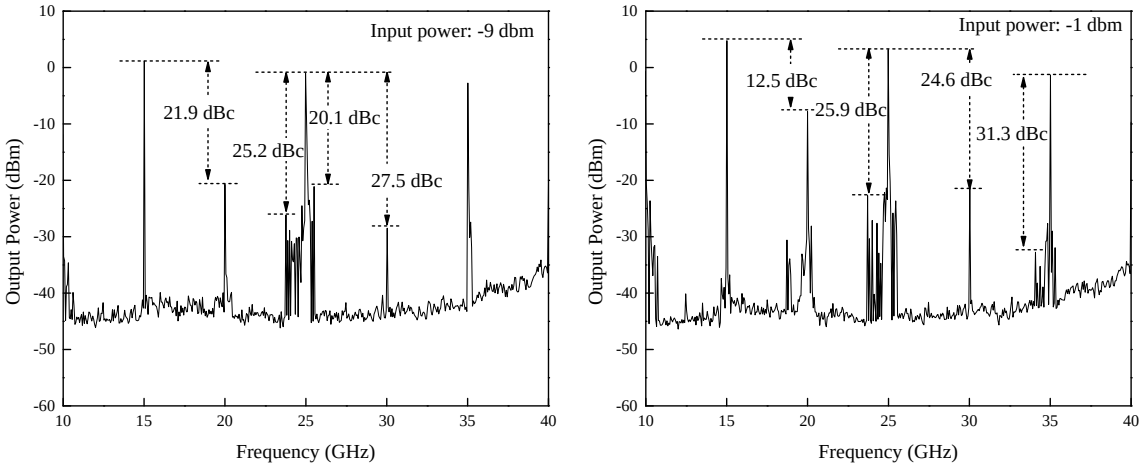


(c)

Figure 2.18. Performance for the 15/25/35GHz tri-band mode: measured and simulated power gain and PAE (a) and output power (b), and measured frequency spectrum at -27-dBm input power (c).



(a) (b)

Figure 2.19. Frequency spectrum for tri-band operations with respect to input power (a) with -9 dBm input power, and (b) with -1 dBm input.

Table 2.4. Summary of tri-band performance.

		15GHz	25GHz	35GHz
$P_{out,max}$ (dBm)	Simulation	10.3	7.1	5
	Measured	8.8	5.4	3.8
P_{1dB} (dBm)	Simulation	2.5	0.9	-1
	Measured	2.9	-5	-4.9
Max. PAE (%)	Simulation	7.1 at -1 dBm input		
	Measured	4.4 at -1 dBm input		

priate values for the series capacitor (C_a) for different gain cells [17], which result in equal input signal at each gain cell, leading to more constructive addition of the powers from the outputs of the gain cells and hence improved PAE; using transistors with different periphery with tapered transmission line [18]; and implementation of a mechanism to suppress the intermodulation products. Suppression of the intermodulation products in multi-band PAs, however, is very challenging due to many

Table 2.5. Comparison of measured performance for different operating modes.

Parameters	Single-band mode			Dual-band mode			Tri-band mode
Frequency (GHz)	15	25	35	15/25	15/35	25/35	15/25/35
Gain (dB)	15.4	14.8	12.8	15.4/14.8	15.4/12.8	14.8/12.8	15.4/14.8/12.8
$P_{out,max}$ (dBm)	15	13.3	13.8	11.4 / 8.2	13.3 / 3	8.7 / 6.7	8.8/5.4/3.8
P_{1dB} (dBm)	11.4	3.3	0	7.1 / 1.7	8.7 / -2.6	2.6 / -2.9	2.9/-5/-4.9
Max. PAE (%)	10	6.5	7.5	6	6.8	3.9	4.4

unwanted signals resulting from multi-band operations - many of which could fall within the desired pass-bands.

Table 2.6 compares the performances of the designed concurrent tri-band PA to some recently reported silicon-based single-band PAs at similar operating frequencies. It is noted that our PA is designed for multi-band operation, not for single-band operations as those it is compared to. Therefore, this comparison should not be taken strictly.

2.5 Conclusion

The development of the concurrent 10-19 GHz, 23-29 GHz and 33-40 GHz tri-band PA on 0.18-μm SiGe BiCMOS process has been presented. The concurrent tri-band PA utilizes the distributed amplifier topology with capacitive coupling to increase the power handling capability. It also implements gain cells with series peaking inductor for enhanced gain peaking. Particularly, the concurrent tri-band PA incorporates two active notch filters having negative resistance in each gain cell

to enhance the Q of the notch filters to produce better tri-band gain response. The GCPW is used to form the needed synthetic transmission lines to minimize the loss from the Si substrate. The concurrent tri-band PA exhibits fairly flat responses in gain and output power across the designed three bands and good input and output matching up to 40 GHz. It can operate in tri-band as well as dual-band and single-band modes. The concurrent tri-band PA should be attractive for tri-band communication and sensing systems operating in Ku, K and Ka-bands. The concurrent tri-band design technique is extendable for other multiband distributed PAs and circuits involving more than three bands.

Table 2.6. Comparison of proposed tri-band PA and single-band PAs.

Ref	Technology	Operation Mode	Freq. (GHz)	Gain (dB)	P_{sat} (dBm)	PAE (%)	Structure
[17]	0.25-μm BiCMOS	Single-mode	1-12	12	16.2-19.5	10.3-22.1	Distributed Amplifier
[19]	0.18-μm CMOS	Single-mode	DC-35	20.5	7-12.4 11@ 15G 10@ 25G 7@ 35G	N/A	Distributed Amplifier
[20]	0.18-μm CMOS	Single-mode	27	14.5	14	13.2	Narrow-band Amplifier
[21]	65 nm CMOS	Single-mode	27-34	> 22.8	9.7-10.8	19.1-23.5	Medium-band Amplifier
[22]	0.18-μm CMOS	Single-mode	31	6.1	12.3	N/A	Narrow-band Amplifier
This Work	**0.18-μm BiCMOS**	**Single-mode**	**10-19 23-29 33-40**	**13.7-17.1 13-16.4 10.6-13.9**	**14.4-15.4 9.5-14.7 12.8-14.1**	**10@ 15 GHz 6.5@ 25 GHz 7.5@ 35 GHz**	**Distributed-based**
		Dual-band mode	**15/25 15/35 25/35**	**15.4/14.8 15.4/12.8 14.8/12.8**	**11.4 / 8.2 13.3 / 3 8.7 / 6.7**	**6 6.8 3.9**	**Concurrent Amplifier**
		Tri-band mode	**15/25/35**	**15.4/14.8/12.8**	**8.8/5.4/3.8**	**4.4**	

CHAPTER III

A HIGH PERFORMANCE K-BAND POWER AMPLIFIER*

In this chapter, a high performance K-band power amplifier is presented, which is a broadband fully integrated power amplifier (PA) with 3-dB bandwidth from 16.5 to 28 GHz designed using a 0.18-μm SiGe BiCMOS process [23]. The PA consists of a drive amplifier and two parallel main amplifiers. Lumped-element Wilkinson power divider and combiner are especially used to combine the main amplifiers as well as to provide suppression for the harmonics through their inherent low-pass filtering characteristic. The PA exhibits measured gain of more than 34.5 dB and very flat output power of 19.4±1.2 dBm across 16.5-28 GHz, and power added efficiency (PAE) higher than 20 % and 17 % between 16-24.5 GHz and up to 28 GHz, respectively. Specifically at 24 GHz, it achieves 19.4 dBm output power, 22.3 % PAE, and 37.6-dB gain.

3.1 Introduction

The design of RF power amplifiers (PAs) on silicon substrates is still one of the most challenging works. Devices on silicon have low breakdown voltages which constrain the voltage swings and lead to reduced power gain. Furthermore, silicon substrates are highly conductive and hence very lossy at high frequencies, leading to reduced gain and output power. In order to resolve the low breakdown voltage problem and have more headroom for the voltage swings, cascode structure, that has higher breakdown voltage than single common emitter (CE) or base (CB), has been used for PAs designed with silicon technologies [24–29]. Nevertheless, it is still

difficult to achieve high gain and output power with decent PAE simultaneously across wide frequency ranges for silicon-based PAs. Such PAs are always in demand, particularly at commonly used frequencies such as the ISM frequency of 24 GHz.

In this chapter, the development of a broadband PA covering more than K-band (18-26.5 GHz) with high gain, flat and high output power, and high PAE on a 0.18-μm BiCMOS process is reported. The PA employs two identical amplifiers in parallel, each with a cascode gain stage, and achieves good performance with output power of 19.4 $\pm$ 1.2 dBm, gain of more than 34.5 dB across 16.5 to 28 GHz, and PAE of higher than 20 % from 16-24.5 GHz and 17 % up to 28 GHz. Specifically, at the popular ISM frequency of 24 GHz, the PA achieves 19.4-dBm output power, 22.3 % PAE, and 37.6-dB gain. The lumped-element Wilkinson power divider/combiner is implemented especially designed to exhibit the low-pass filtering characteristic that helps suppress the harmonics as well as enhance the bandwidth, primarily resulting in good PA performance over a wide frequency range. To the best of my knowledge, there has been no silicon-based PA reported that implements the lumped-element Wilkinson device and exploits its wideband low-pass filtering behavior.

3.2 Circuit Design

Figure 3.1 shows the schematic of the PA, which includes a driver amplifier, Wilkinson power divider and combiner, and two identical main amplifiers. Power combining is employed to attain 3-dBm increase in output power. The main and driver amplifiers employ cascode structure, which has more gain than the CE or CB structure, for all the gain cells to achieve high gain. This leads to large device size ratio between the transistors of the main and drive amplifiers, hence resulting in desirably less burden for the drive amplifier. Furthermore, the cascode configuration also provides better reverse isolation, making it function more unilateral, hence

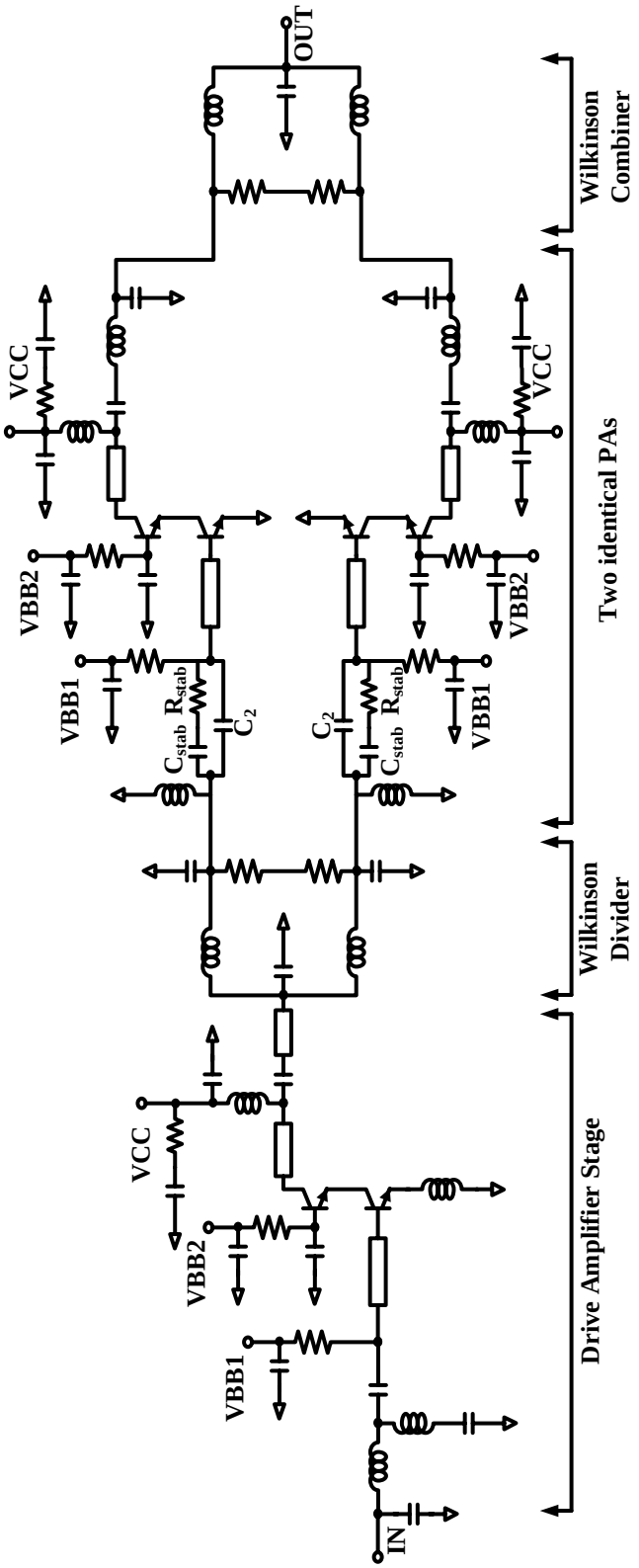


Figure 3.1. Schematic of the designed PA.

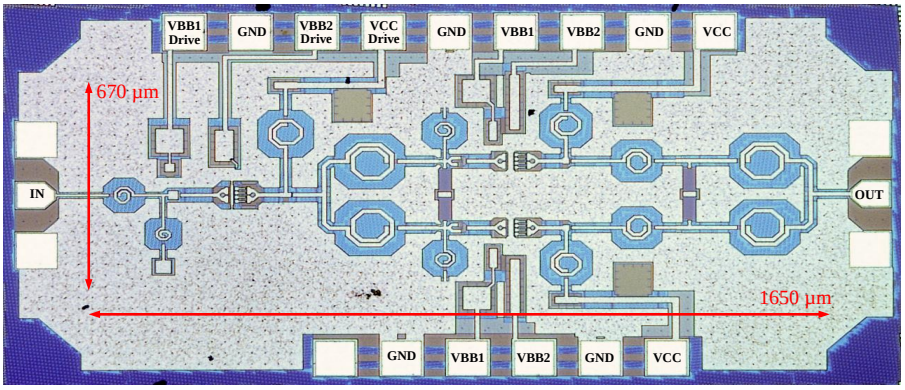


Figure 3.2. Photograph of the fabricated PA.

facilitating the design.

Figure 3.2 shows a photograph of the designed PA fabricated using Jazz 0.18-μm SiGe BiCMOS process [14]. The chip area is $2 \times 1\ mm^2$ or $1.65 \times 0.67\ mm^2$ with or without the RF and DC pads, respectively. As can be seen, all of the spiral inductors and transmission lines for the input and output feeding as well as interconnections are implemented using coplanar waveguide (CPW) on the topmost metal layer for the lowest possible loss. The common ground plane for the CPW is also extended around all the inductors to isolate the inductors from nearby elements, hence minimizing the coupling, as well as to provide a continuous ground plane as large as possible for the entire PA chip. For RFIC operating at high frequencies, a ground should be considered as a distributed structure, and maintaining a possible large continuous ground plane is crucial for the performance of RFICs, especially at high frequencies and/or for large chips. These components were designed and simulated using the EM simulator IE3D [15]. Furthermore, the RCX simulation in Cadence [30] was also conducted for the whole PA to extract the parasitic elements produced by the layout.

3.2.1 Main Amplifier Design

Each transistor in the main amplifiers consists of four transistor constituents, each having 0.15 μm emitter width and 10.16 μm emitter length selected based on load-pull simulations for high output power under the class AB bias point. In general, PAs typically employ large transistors, thereby making them more prone to instability. To improve the PA stability and attain unconditional stability at lower frequencies, series RC circuit with shunt capacitor (C_2) [24] is connected to the input of the main amplifier as shown in Figure 3.1. This RC network is designed to produce resistive loss at low frequencies so that the excessive gain of the active devices at lower frequencies can be reduced, thereby resulting in an improvement for the stability. To further improve the low-frequency stability, a 4.2 pF bypass capacitor connected in parallel with a series combination of a small 5 Ω resistor and a larger 13.2 pF bypass capacitor are used at the collector's DC supply node (V_{CC}). The simulated stability factor (K) of the amplifier is greater than 30 for all frequencies between DC and 60 GHz.

3.2.2 Lumped-Element Wilkinson Power Divider and Combiner Design

Traditionally, Wilkinson power divider/combiner is designed using two quarter-wavelength transmission lines. Using such transmission lines, however, is not desirable at 16.5-28 GHz for CMOS/BiCMOS RFICs due to their rather long length. To minimize the chip size, lumped-element Wilkinson power divider/combiner [31], [32] is implemented. The traditional quarter-wavelength transmission line is replaced with a pi-network as shown in Figure 3.1. The inductance and capacitance of the pi-network can be derived as $L = Z_0/2\pi f_0$ and $C = 1/2\pi f_0 Z_0$, respectively, where Z_0 is the transmission line's characteristic impedance and f_0 is the design frequency. Figure 3.3(a) shows the simulated S-parameters of the designed lumped-element

Wilkinson power divider/combiner. At 24 GHz, the insertion loss is 3.66 dB and its second harmonic is rejected by more than 16 dB. As can be seen, the designed lumped-element power divider/combiner exhibits a low-pass filtering response over a wide bandwidth. This is due to the fact that each of its two arms resembles a synthetic transmission line which operates as a wideband low-pass filter up to a cut-off frequency. This wideband low-pass filtering behavior is exploited to suppress the undesired harmonics, which cannot be otherwise achieved on PAs employing transmission-line Wilkinson devices, as well as to enhance the bandwidth of the PA. In order to verify the harmonic suppression and improved PAE on PAs due to the use of the lumped-element Wilkinson devices with low-pass filtering, we simulated two PAs designed with lumped-element and transmission-line Wilkinson power dividers/combiners. Figure 3.3(b) and 3.3(c) show the simulated output powers of the 24-GHz fundamental and 48-GHz second-harmonic signals and the PAE. As can be seen, the PA with the lumped-element Wilkinson power divider/combiner provides more suppression of the second harmonic, while producing slightly higher fundamental output power, and higher PAE.

3.2.3 Driver Amplifier Design

The driver amplifier is designed to provide the required input power for the main amplifiers. Each device of the driver amplifier combines four transistors each having 0.15 μm emitter width and 4.52 μm emitter length. With respect to the main and driver amplifiers' device sizes, the device size ratio of the input and output for the PA is larger than 4:1. A degeneration inductor, implemented by a short transmission line, is used at the emitter of the CE constituent. Inductive emitter degeneration introduces negative series feedback and enables broadband input matching. An input matching network is also included for the driver amplifier.

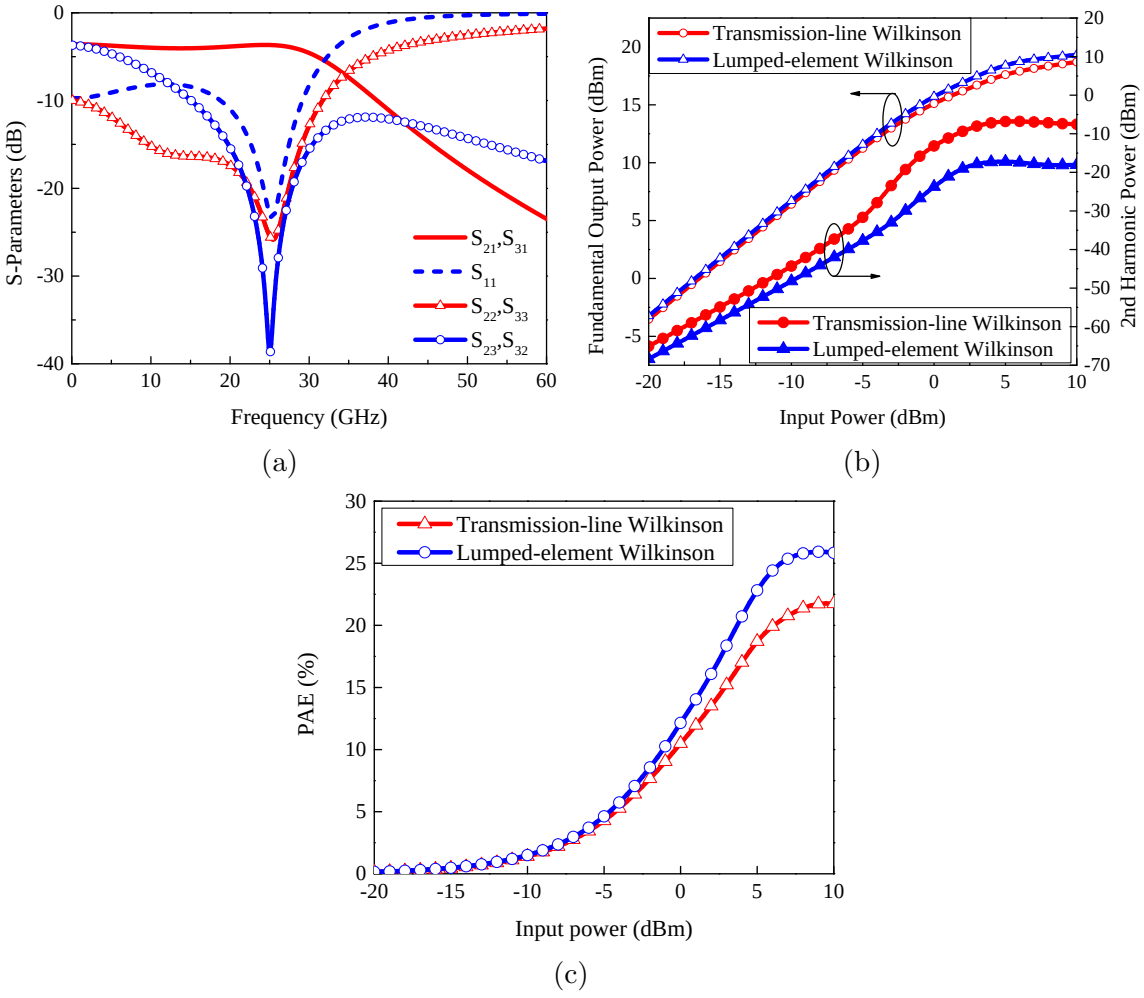


Figure 3.3. (a) Performance of the lumped-element Wilkinson divider/combiner. 1 and 2, 3 are the input and two output ports, respectively. Simulated fundamental and 2nd harmonic power (b) and PAE (c) of PAs with lumped-element and transmission-line Wilkinson power.

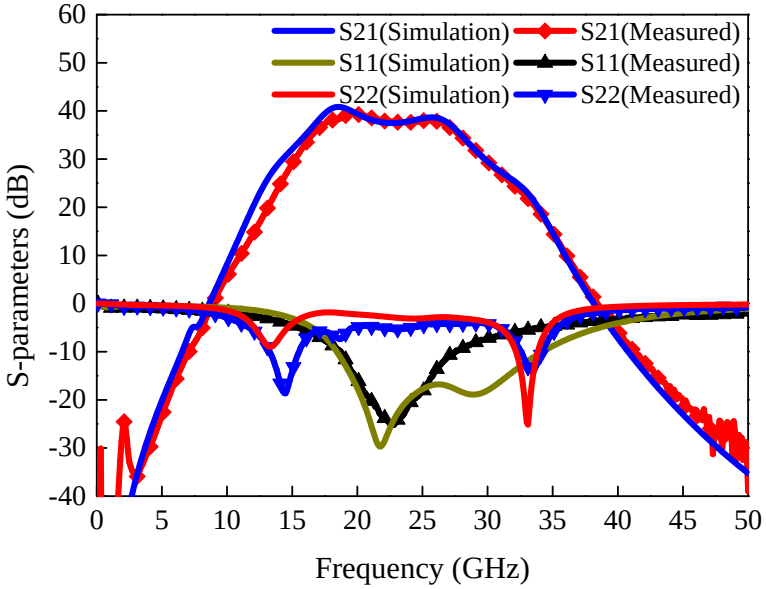


Figure 3.4. Measured and simulated S-parameters.

3.3 Performance

The PA was measured on-wafer. The collector voltage of the cascode device (V_{CC}) was set to 2.4 V and the DC current of drive and main amplifiers were 30 mA and 65 mA, respectively. Figure 3.4 shows the measured and simulated small-signal S-parameters of the designed PA. The measured small-signal gain across the 3-dB gain bandwidth of 16.5 to 28 GHz is larger than 34.5 dB and matches very well with that simulated. Specifically at 24 GHz, the gain was measured as 37.6 dB which is very close to the simulation result of 37.8 dB. The measured and simulated input and output return losses also agree reasonably well. The measured input return loss is below 10 dB from 18.7 to 28 GHz. Figure 3.5 shows the measurement and simulation results of power gain, output power, and PAE with respect to the input power at 24 GHz. At 24 GHz, the saturated output power is 19.4 dBm corresponding to the peak PAE of 22.3 %, and the output power at 1-dB compression point (OP1dB) is 13.8

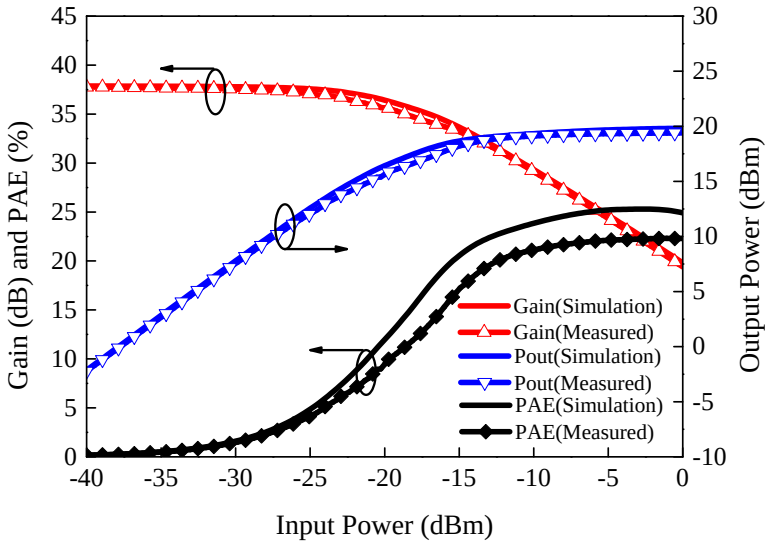


Figure 3.5. Measured and simulated power gain, output power, and PAE at 24 GHz.

dBm. Figure 3.6 shows the measured and simulated saturated output power, 1-dB compressed output power, and PAE from 15-30 GHz. As can be seen, the measured saturated output power is highest at 20.6 dBm at 19 GHz. Between 17-22 GHz, 16-25 GHz, and 25.5-28 GHz, the measured saturated output power reaches more than 20, 19, and 18.3 dBm, respectively. It is also observed that the measured saturated output power from 16.5-28 GHz is very flat within ±1.2 dBm. The measured PAE is more than 20 % between 16 and 24.5 GHz and greater than 17 % up to 28 GHz. The discrepancy between the simulated and measured PAE is mainly due to the differences in the simulated and measured bias condition for the PA, which are primarily due to the unavoidable, yet expected, process variation.

Table 3.1 compares the performance of the designed PA with other reported silicon-based PAs in K-band [25–29]. The designed PA has the highest gain (37.6 dB at 24 GHz, higher than 34.5 dB across 16.5-28 GHz), widest 3-dB-gain bandwidth (51.7 %), and very flat power response across the 3-dB bandwidth (±1.2 dBm). It

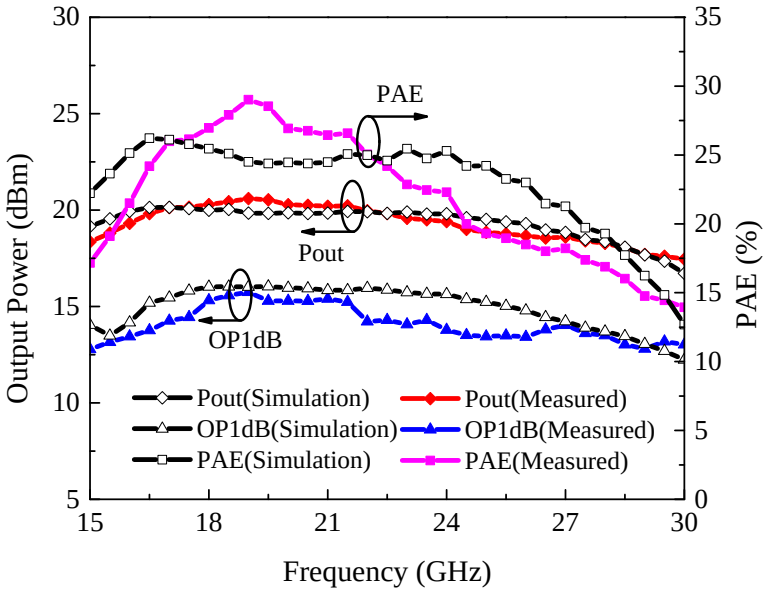


Figure 3.6. Measured and simulated saturated output power, OP1dB, and PAE.

also has the highest output power among the reported PA at 24 GHz, except that in [27]. However, it has better overall output power and PAE performance of 18.3-20.6 dBm and 17-29% across 16.5-28 GHz as compared to around 17.5-23.8 dBm and 5-25.1 % from 16.5-27 GHz in [27], respectively. Moreover, the PA in [27] was realized on 65-nm CMOS process, its 3-dB bandwidth is only 18-22 GHz, and the power variation is larger than that of the designed PA. Although the PAE of the designed PA is lower than that of the PA reported in [26] at 24 GHz, it is higher than those in [25] and [27–29]. Moreover, it has high PAE across a wide bandwidth of 16.5-28 GHz, which has not been reported in other PAs [25–29].

3.4 Conclusion

A broadband PA working across a bandwidth wider than K-band was designed using a 0.18-μm SiGe BiCMOS process. The PA achieves more than 34.5-dB gain and very flat out power of 19.4 ± 1.2 dBm across 16.5-28 GHz with PAE higher than

20 % and 17 % between 16-24.5 GHz and up to 28 GHz, respectively. At 24 GHz, the measured output power is 19.4 dBm with peak PAE of 22.3 %. These results, predominantly made possible with the incorporation of a lumped-element Wilkinson power divider/combiner having a wideband low-pass filtering characteristics, demonstrate possibility of designing high-performance PAs covering wide bandwidths with high, flat output power, and good efficiency using silicon processes, which are desired for Si-based fully integrated broadband systems.

Table 3.1. Performance summary and comparison with reported PAs.

Parameter	**This Work**	[25]	[26]	[27]	[28]	[29]
Process	**0.18μm BiCMOS**	0.13μm CMOS	0.18μm CMOS	65 nm CMOS	0.18μm CMOS	0.13μm CMOS
3-dB-Gain Freq. Range (GHz)	**16.5-28**	24*	24*	18-22	18-23	21*
Gain (dB)	**37.6 @ 24 GHz >34.5 (16.5-28 GHz)**	15.6	19	22 @ 19 GHz 26 @ 21 GHz	22.5 @ 20.5 GHz*	19.5 @ 21 GHz*
Pout (dBm)	**19.4 @ 24 GHz 18.3-20.6 (16.5-28 GHz)**	16	19	23.8 @ 19 GHz 21 @ 24 GHz 17.5-23.8 (16.5-27 GHz)	20.1 @ 20 GHz 18.1-20.1 (19-22 GHz)	20 @ 21 GHz 15.4-20**
PAE (%)	**22.3 @ 24 GHz 17-29 (16.5-28 GHz)**	17.7	24.7	25.1 @ 19 GHz 18 @ 24 GHz	9.3 @ 20 GHz 7.3-9.3 (19-22 GHz)	12.4 @ 21 GHz 4.3-12.7**
Topology	**2 stages, Cascode**	2 stages, Transformer Coupled	2 stages, Cascode	2 stages, Transformer Coupled	3 stages, Cascode	2 stages, Cascode

* Only single frequency provided ** Measured from 20-25 GHz

CHAPTER IV

A V-BAND POWER AMPLIFIER UTILIZING PARALLEL POWER COMBINING TECHNIQUE BASED ON INTEGRATED WILKINSON POWER COMBINER AND TRANSFORMERS

In this chapter, a high output power fully integrated V-band power amplifier (PA) using a four-way parallel power combining structure developed using a 0.18-μm SiGe BiCMOS technology is presented [33]. The developed PA makes use of four-way parallel power dividing and combining structures to feed and combine powers from four identical unit-PA cells, respectively. Especially, the parallel power combiner and divider are developed by integrating a low-loss wideband Wilkinson structure and two transformers connected in parallel, which achieve broad bandwidth and minimum phase and amplitude mismatches between ports. The unit-PA is designed as a pseudo-differential two-stage cascode amplifier, which employ transformers for both matching and impedance transformation. At 60 GHz, it has 27.3-dB measured small-signal gain and 13.3-dBm of maximum output power with 7.3 % of PAE. The complete PA achieves measured broadband small-signal gain of 19 dB and 3-dB bandwidth of 56.8-67.5 GHz, which encompasses the overall unlicensed V-band spectrum (57-64 GHz). In addition, it delivers 18.8 dBm of saturated output power and 15.3 dBm of output 1-dB compressed power with 4.2-% of PAE at 60 GHz. Across 55 to 65 GHz, the complete PA achieves a very flat power performance with maximum output power between 17-19.1 dBm.

4.1 Introduction

Increased demands of high data-rate wireless communications make millimeter-wave (mm-wave) communication systems become more attractive for reduced con-

gestions in the lower frequency bands. Especially, the unlicensed V-band frequency spectrum around 60 GHz (57-64 GHz) has drawn attention for short-range high data-rate communication systems with important applications such as high-definition (HD) video, audio, and IEEE 802.11ad [34] and 802.15.3c [35]. Low-cost highly integrated mm-wave circuit designs with decent performance are possible with available advanced silicon processes that provide scaling down of active devices. In this context, many researches have been carrying out to develop V-band (50-75 GHz) front-end circuits, subsystems, and systems on silicon instead of compound semiconductors such as GaAs and InP. At 60 GHz, propagating signals suffer high attenuation due to the oxygen absorption characteristic, yet making it suitable for short-range communications with good spatial isolation [36]. High output powers at mm-wave including 60 GHz, and hence power amplifiers (PAs) are crucial for mm-wave communications. Even though the development of mm-wave PAs has advanced significantly, it is still challenging to design high-performance mm-wave PAs on silicon due to the inherent limitations of silicon active devices such as low-breakdown voltages resulting in low voltage swing and degradation of power gain. To mitigate these issues, power combining networks are essential, and some works along this line were already reported [37–41]. Recent discussions show that three power combining techniques are generally adopted in mm-wave silicon-based PAs: Wilkinson power combining [37,38], transformer-based voltage combining, and transformer-based current combining [39–41]. The main challenge of designing power combining networks is to obtain low insertion loss, while maintaining compactness and small amplitude and phase imbalances between ports, since it is directly related to the power combining efficiency. Low insertion loss, however, is not easy to achieve on silicon substrates.

In this chapter, a 0.18-μm SiGe BiCMOS V-band PA with high output power and decent gain and linearity is reported. The PA consists of four identical PA units and

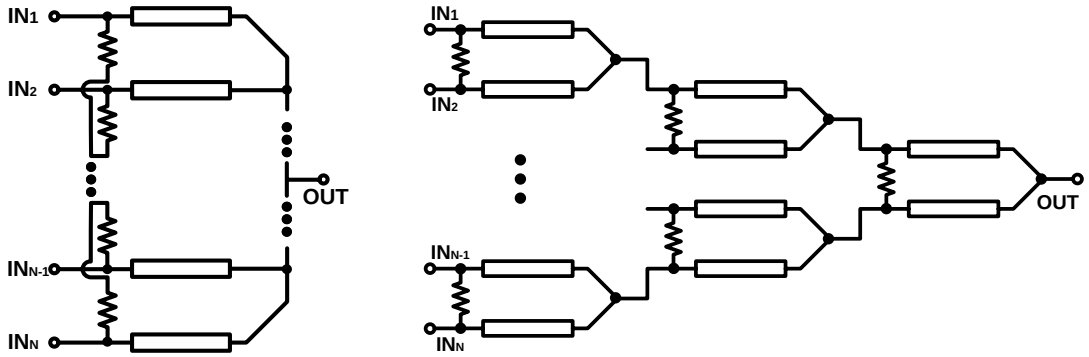
four-way parallel power dividing and combining networks. The unit-PA is designed as a pseudo-differential two stage cascode amplifier structure. The input and output transformers of the unit-PA play role in conversion of differential signal to single-ended input and output signals, as well as being parts of the matching networks. The employed power combiner, which is identical to the power divider, is a four-way parallel power combining structure designed by integrating low-loss broadband slow-wave Wilkinson power combiner and two transformers. The fully integrated PA has features of high and flat output power over a broad frequency range including the entire unlicensed V-band.

4.2 Four-way Parallel Power Combiner/Divider Design

Three well-known power combining techniques are utilized in many mm-wave silicon based PAs including Wilkinson power combining [37,38], transformer (TXF)-based voltage combining, and TXF-based current combining [39–41], each having its own advantages and disadvantages. In the following subsections, these topologies will be described followed by the proposed four-way parallel power combining/dividing network.

4.2.1 N-way Wilkinson Power Combiner

Figure 4.1(a) shows an N-way Wilkinson power combiner, which consists of quarter-wavelength transmission lines having characteristic impedances of $\sqrt{N}Z_0$, where Z_0 is the system or terminating impedance. The characteristic impedance increases as N is increased, making it hard to implement in most silicon process, even for a moderate value of $N = 4$. For instance, for $N = 4$ and $Z_0 = 50\Omega$, Z_{TL} is 100Ω and it is hard to realize a TL with characteristic impedance higher than 100Ω in most silicon processes. To alleviate the transmission-line realization problems, a binary combining structure employing multiple two-way Wilkinson structures as



(a) (b)

Figure 4.1. N-way Wilkinson power combiner (a) and N-way binary combining structure implementing multiple two-way Wilkinson power combiners (b).

shown in Figure 4.1(b) can be adopted. This combiner, however, has large footprint and high insertion loss, thereby increasing the cost and degrading the power combining efficiency, respectively, and hence is not very suitable for silicon radio-frequency integrated circuits (RFICs).

4.2.2 Transformer-Based Voltage and Current Combiner

The TXF-based voltage combining technique, also called series combining, piles up the voltage swings of the PA-cells, each designed as two amplifiers differentially as shown in Figure 4.2(a). When each PA-cell is identically connected at N-combining paths, the voltage (V) and current swing (I) are also same at each primary inductor of the TXF having $1 : X$ turn-ratio, and the output voltage (V_{out}) and current (I_{out}) across the secondary winding is $N \cdot XV$ and I/X, respectively. Furthermore, the transferred impedance Z_{TXF} at the TXF's primary inductor from the load impedance (R_L) is $R_L/(NX^2)$. Under this situation, power matching can be obtained between Z_{TXF} and the optimum output impedance of each single-ended amplifier (Z_{opt}) at PA_N, and hence $Z_{opt} = R_L/(2NX^2)$.

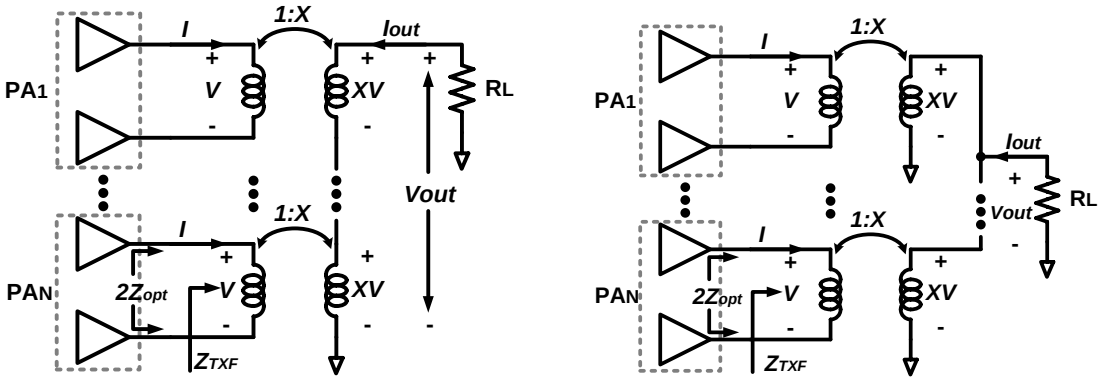


Figure 4.2. N-way transformer power combiners implementing voltage combining (a) and current combining schemes (b).

Figure 4.2(b) shows the TXF-based current (or parallel) combining topology employing N transformers with $1:X$ turn-ratio. Unlike the voltage combining structure, all TXFs are parallel-connected, thereby accumulating the currents of the secondary windings instead of the voltages. Consequently, the output current (I_{out}) of $(N \cdot I)/X$ flows into the load impedance. Also, the input impedance of each transformer (Z_{TXF}) is $(NR_L)/X^2$ and the value of Z_{opt} should be $(NR_L)/2X^2$ for power matching.

Employing TXFs for power combining makes possible design on more compact footprint compared to those utilizing Wilkinson power combiners, which is attractive, especially for RFICs. Furthermore, impedance transformation can be inherently made through the TXFs, thereby avoiding use of separate matching networks and further reducing the size. The TXF-based power combiners, however, also have some weaknesses. For the voltage combining method, the amplitude and phase mismatch issues are significant due to the combiner's physical structure, thereby degrading the power combining efficiency. Furthermore, Z_{TXF} is inversely proportional to the number of combining paths (N), hence Z_{opt} for large N becomes small for power

matching. Thus, each PA is designed with large devices, thus making them sensitive to parasitics [41]. For instance, for $N = 4$, $X = 1$, and $R_L = 50$, $Z_{opt} = 6.25\ \Omega$, which is very small. In contrast to the voltage combining topology, the current combining structure is more symmetrical, resulting in mitigation of the phase and amplitude imbalance problems. A comparison of the phase and amplitude mismatches between the two techniques is given in [41]. From the viewpoint of impedance, each PA-cell in the current combining topology can be designed with higher Z_{opt} than the voltage combining structure; yet this causes decreased output power of the PA-cell. For this reason, TXFs with X larger than 1, are normally adopted for the current combining structure. For example, $N = 4$, $X = 2$, and $R_L = 50\ \Omega$, which result in $Z_{opt} = 25\ \Omega$. Although the current combining technique seems much better than the voltage combining method, there are several design issues for multi-turn TXFs. One of them is the low quality factor and high insertion loss suffered by TXFs with large turn ratios, thereby lowering the power transfer efficiency [42]. Another problem is that the turn-ratio of TXFs may not be an integer number for certain situations, hence making it difficult to implement TXFs [43].

4.2.3 Proposed Four-way Parallel Power Combiner/Divider

There are two fundamental key points in the design of power combiners and dividers: minimizing the insertion loss and amplitude and phase mismatches between ports. To reduce the port imbalances, which directly affect the inter-port amplitude and phase balances, the parallel power combining architecture is chosen to implement the proposed four-way power combiner. Figure 4.3 shows the schematic of the proposed combiner, which consists of a Wilkinson power combiner and two 1:1 turn-ratio TXFs parallel-connected to its amrs. This combiner possesses the advantages of both Wilkinson and TXF parallel combining techniques.

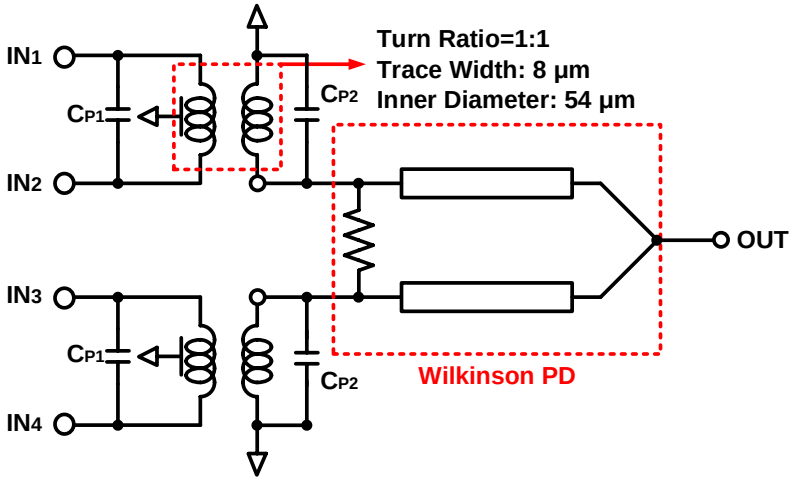


Figure 4.3. The schematic of the proposed four-way power combiner structure.

4.2.3.1 Design of Low-loss Wilkinson Power Combiner with Slow-wave Capacitive Loading

For the Wilkinson power combiner constituent, minimum insertion loss and compact size are two important design criteria. In this context, the low-loss Wilkinson power divider with capacitive loading slow-wave structure reported in [44] is employed. For the capacitive loading, a TL of electrical length θ_1 shorter than a quarter-wavelength TL loaded with two shunt capacitors (C_W) is employed and the values of θ_1 and C_W can be calculated as

$$Z_{01} = \frac{Z_0}{\sin(\theta_1)} \tag{4.1}$$

$$C_W = \frac{\cos(\theta_1)}{\omega \cdot Z_0} \tag{4.2}$$

where Z_0 and Z_{01} are the characteristic impedances of the original quarter-wavelength and modified shorter TLs, respectively. According to the above equations, the length

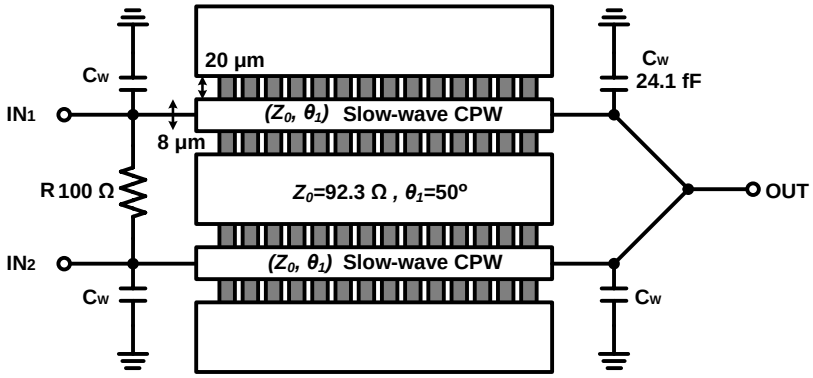


Figure 4.4. The schematic of designed Wilkinson power combiner employing capacitive loading slow-wave structure.

of modified TL ($\theta 1$) is inversely proportional to the required characteristic impedance (Z_{01}) and the capacitance values (C_W). Figure 4.4 shows the Wilkinson power combiner with loading capacitors of 24.1-fF and 92.3 Ω slow-wave CPW having 50° length at 60 GHz, following the design described in [44]. The slow-wave CPW is employed for further length reduction besides minimization of the insertion loss since it leads to increased effective dielectric constant and causes reduced physical length of a TL. The slow-wave effect, however, causes decrease in the characteristic impedance of the TL because of the confinement of the electric field. In this context, the metal layer for the floating metal strips should be chosen with consideration of the required TL's characteristic impedance. Hence, the slow-wave CPW is implemented by placing periodical floating metal strips on metal layer 4 (M4) orthogonally to the signal line on the topmost metal layer 6 (M6). The 24.1-fF shunt capacitors are designed based on interdigitated capacitors, in which the top three metal layers (M4, M5, and M6) are stacked and formed each finger of the capacitors, thereby achieving higher capacitance density compared to the general interdigitated capacitors.

4.2.3.2 Transformer Design

Two TXFs are designed and they act as baluns to convert single-ended to differential signals. The turn-ratio of the TXFs is set to 1:1 ($X = 1$) to avoid a low self-resonant frequency problem and have a low insertion loss as mentioned early. There are two types of TXFs used in common: the planar type and the vertical structure. The TXFs are realized utilizing the two topmost metal layers (M5 and M6) for the primary and secondary inductors, respectively, hence forming a vertical structure that achieves more coupling between the two windings than a planar counterpart [45]. Each inductor is designed as octagonal shape with 8-μm trace width and inner radius of 54-μm. Furthermore, a capacitor is connected in parallel at each winding (C_{P1}, and C_{P2}), as shown in Figure 4.3, to tune the transformer for better matching and loss reduction [46].

4.2.3.3 Design of Four-way Power Combiner/Divider

Figure 4.5 shows the physical layout of the designed four-way power combiner, which integrates the capacitive loading slow-wave Wilkinson power combiner with the two TXFs. The differential input RF signals are combined through the TXFs to appear as in-phase at the input ports of the Wilkinson combiner and are, ultimately, added together at the output port of the Wilkinson combiner. Figure 4.6(a) shows the simulated S-parameters of the designed power combiner. At 60 GHz, $S_{51} = S_{54} = -7.3$ dB and $S_{52} = S_{53} = -7.43$ dB can be achieved. The power combiner can also be used as a power divider and hence the insertion loss of the designed power combiner can be calculated from

$$IL(dB) = |P_{out} - P_{in}| = \left| 10log\left(\sum_{i=1}^{4} 10^{S_{5i}/10}\right) - P_{in} \right| \tag{4.3}$$

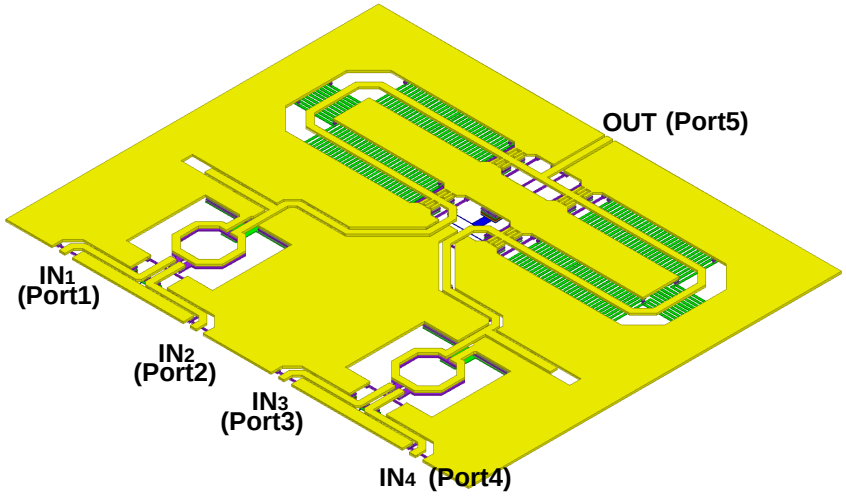
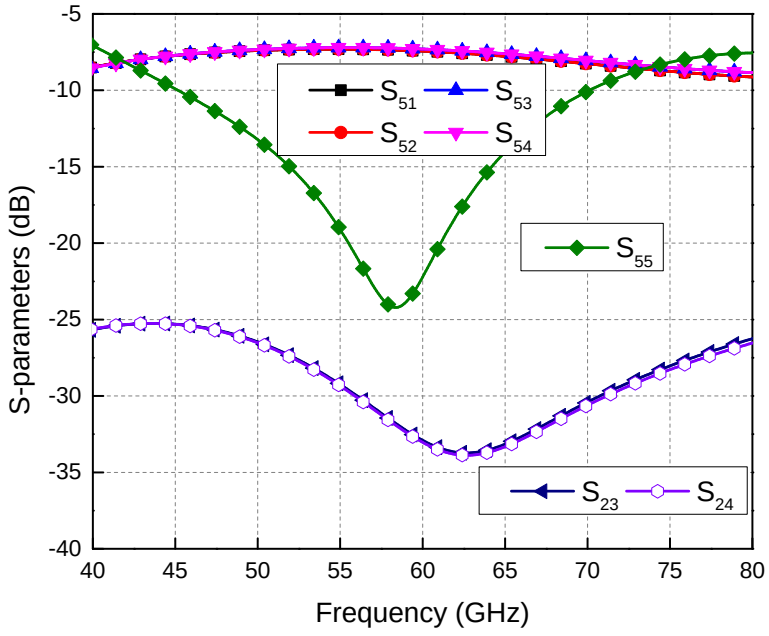


Figure 4.5. Physical layout of the designed four-way power combiner.

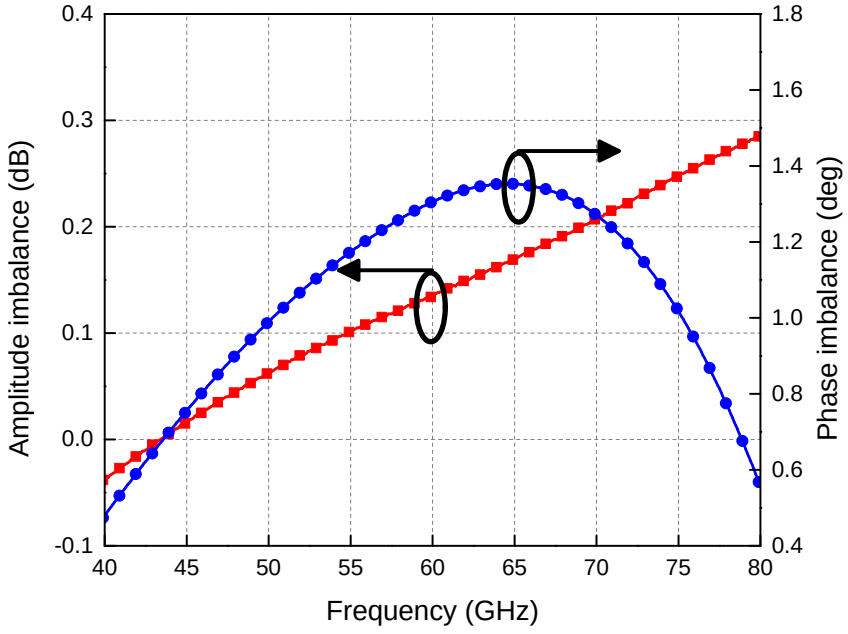
where P_{in} is the input power at port 5 and Pout is the total output powers at ports 1 to 4. At 60 GHz, an insertion loss of 1.35 dB is obtained. Furthermore, the power efficiency of the designed power combiner (η_{PD}), measured by its insertion loss, can be represented as

$$\eta_{PD}(\%) = \frac{P_{out}(Watt)}{P_{in}(Watt)} \times 100 \tag{4.4}$$

which shows that 73.4% of power efficiency can be achieved at 60 GHz. Due to symmetry, the isolation S_{23} between IN_2 and IN_3 is equal to the isolation S_{14} between IN_1 and IN_4, and the isolation between IN_2 and IN_4 (S_{24}) is the same as that between IN_1 and IN_3 (S_{13}). All the isolations are higher than 25 dB across the V-band. The output return loss (S_{55}) is higher than 10 dB from 45 to 73 GHz. The inter-port amplitude and phase imbalances are plotted in Figure 4.6(b). As can be seen, amplitude and phase mismatch of less than 0.2 dB and 1.4°, respectively, are achieved between 55 and 70 GHz.



(a)



(b)

Figure 4.6. Performance of the designed four-way power combiner: (a) simulated S-parameters and (b) amplitude and phase mismatches between input ports.

4.3 V-Band Power Amplifier Design

The designed V-band PA consists of the four-way power combiner and divider described in Section 4.2.3 and four identical unit PAs. This section describes details of the unit PA and the complete PA designed and fabricated using TowerJazz 0.18-μm SiGe BiCMOS process [14].

4.3.1 Design of the Unit-PA

Figure 4.7 shows the schematic of the designed unit-PA, which is a pseudo-differential two-stage transformer based PA. Table 4.1 shows the values of all components. The unit-PA is composed of the drive and power stages with matching networks and three transformers (TXF_1, TXF_2 and TXF_3). TXF_1 and TXF_3 converts single-ended to differential signals and vice versa, hence providing differential power division and combination, respectively, and are parts of the corresponding matching networks. TXF_2 is part of the inter-stage matching network and used to convert the input impedance of the main amplifier to the drive stages optimum impedance. Using TXFs as matching elements makes possible to design more compact matching networks than those based on transmission lines [47]. MIM capacitors and coplanar waveguide (CPW) interconnects are also used.

Unlike the fully differential structure, the pseudo-differential configuration does not have the tail current source and hence mitigating voltage headroom problem, making it attractive for low power supply applications. Moreover, the pseudo-differential structure has a common ground, which is an important feature in the design of mm-wave circuits and systems. A well-defined common ground plane is important and at mm-wave frequencies, it should be considered as a distributed structure and retained as a continuous ground plane for design of high-performance mm-wave RFICs [23], [48]. Moreover, the cascode topology is employed to obtain

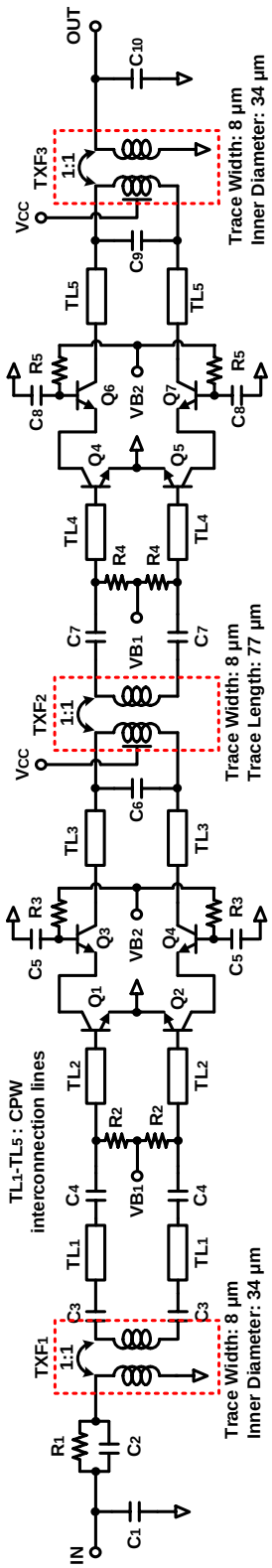


Figure 4.7. The schematic of the designed unit-PA cell.

Table 4.1. Component values of unit-PA.

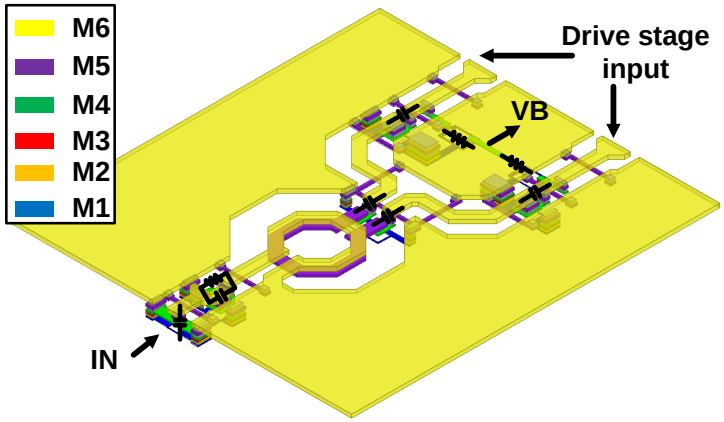
Components	Values	Components	Values
R_1	260 Ω	Q_1, Q_2, Q_3, Q_4	$5\mu m \times 2$
R_2, R_3	4.5 $K\Omega$	($E_W \times M$)	
R_4, R_5	3.4 $K\Omega$	Q_5, Q_6, Q_7, Q_8	$10\mu m \times 2$
		($E_W \times M$)	
C_1	82.8 fF	C_6	41.4 fF
C_2	198 fF	C_7	134 fF
C_3	125 fF	C_9	125 fF
C_4	222 fF	C_{10}	98 fF
C_5, C_8	1.6 pF		

E_W: Emitter width, M: Multiplier

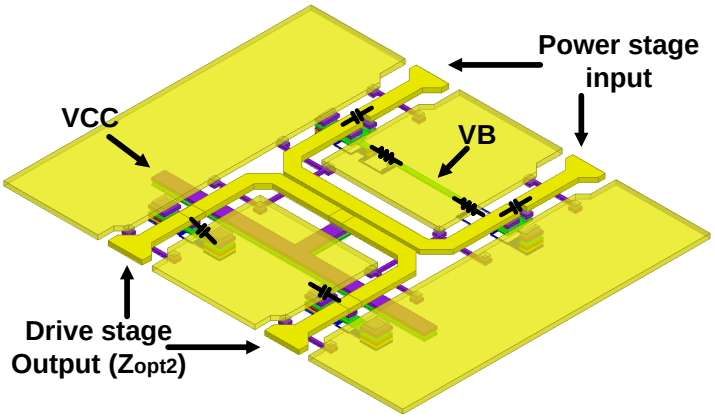
high power gain and isolation between input and output. The optimum device sizes are determined by using the load-pull simulations, and the device size ratio between the drive and the power stages is 1 : 2. The DC currents of the drive and power stages on each branch are 24 and 36 mA under 2V of V_{CC}, respectively.

Figure 4.8(a), (b), and (c) show the physical structures of the input, inter-stage, and output matching networks, respectively. All of the TXFs as well as CPW's in the matching networks are simulated and their performances are verified by the EM simulator Momentum (Keysight Technology, Advanced Design System 2013 [49]). The dimensions of all the TXFs are chosen for proper impedance transformations.

In the output matching network, TXF_3 is realized as a vertical structure utilizing the two top metal layers (M6 and M5) for the primary and secondary windings, respectively. The output matching network is designed between the load and the optimum impedance (Z_{opt1}) of the device for the power stage, which is $10+j10\Omega$ obtained from load-pull simulation for maximum output power. In this design, the output matching network is implemented with TXF_3 and two MIM capacitors and inter-



(a)



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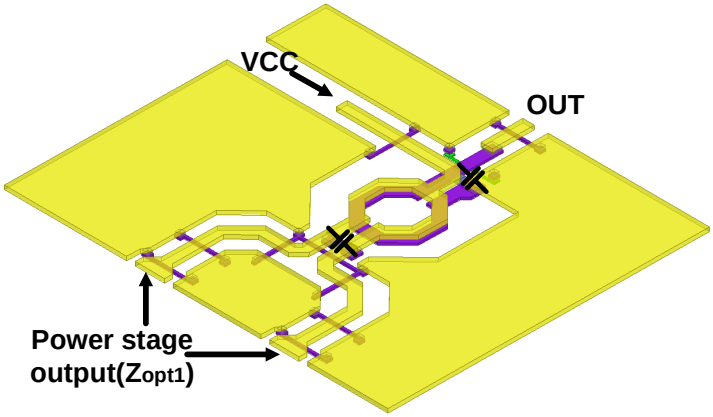


(c)

Figure 4.8. The physical structures of (a) input matching, (b) inter-stage matching, and (c) output matching network.

connection CPW lines as shown in Figure 4.8(c), so that the output load impedance is transformed to Z_{opt1}. Besides being part of the output impedance matching, TXF_3 also acts as a circuit that enables DC bias injection through the center tap, thereby allowing a single biasing circuit to provide biasing to both differential paths symmetrically. In the inter-stage matching network shown in Figure 4.8(b) is composed of the TL-based TXF, MIM capacitors, and CPW inter-connection lines. TXF_2 is implemented as a coupled-transmission-line based transformer instead of a vertical transformer. This structure was reported in [50]. The coupled transmission line is realized with the thickest M6 metal for low loss and the gap between the two TLs is set to 2-μm. Similar to TXF_3 of the output matching network, the center tap of TXF_2 is used to supply the collector DC bias for the drive stage. The DC feed line is implemented with the combined M5 and M4 metals through vias for low loss and improved current handling capability. Shunt capacitor C6 is realized with two capacitors connected to the common ground plane. Therefore, the designed inter-stage matching network provides the impedance matching between the input impedance of the power stage and optimum impedance (Z_{opt2}) of the drive stage, which is $20 + j17.5\Omega$. Lastly, in the input matching network shown in Figure 4.8(a), TXF_1 is designed as a vertical structure similar to TXF_3. Besides contributing to the input matching, TXF_1 also acts as a balun converting a single-ended input signal into differential signals.

In general, large-size transistors are employed for PA design; yet this causes designed PA's prone to instability. Utilizing TXFs as parts of the matching networks in amplifiers can improve the amplifiers' stability factors, hence helping overcome the instability caused by using large devices. This is due to the fact that the series resistances of the primary and secondary inductors as well as the lossy shunt mutual inductor of the TXFs help improve the stability [47]. To enhance the stability factor

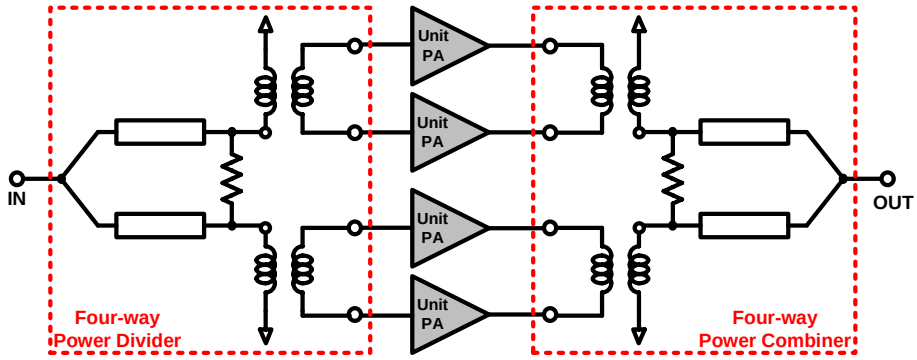


Figure 4.9. Block diagram of the designed PA.

at low-frequency region, a parallel RC network is used in front of TXF_1. This RC network produces a resistive loss at low frequencies, hence resulting in improved stability.

4.3.2 Design of the Complete PA

Figure 4.9 shows the complete V-band PA integrating the four-way parallel power divider and combiner and four unit-PA cells. To maintain symmetry, the V-band PA is laid out symmetrically with respect to each arm of the Wilkinson power combiner/divider, which is part of the designed four-way power combining/dividing network. The total DC currents for the driver and main power stages are 208 and 284 mA under 2 V of V_{CC} voltage, respectively.

4.4 Simulation and Measurement Results

Small-signal performance based on S-parameters and large signal responses of the designed unit-PA and complete PA were simulated and measured. All simulation results include EM-simulated data for passive elements and parasitic effects of layout extracted from the RCX simulations in Cadence (Cadence Design System, Assura). The measurements were done on-wafer with 150-μm pitch GSG probes and multi-

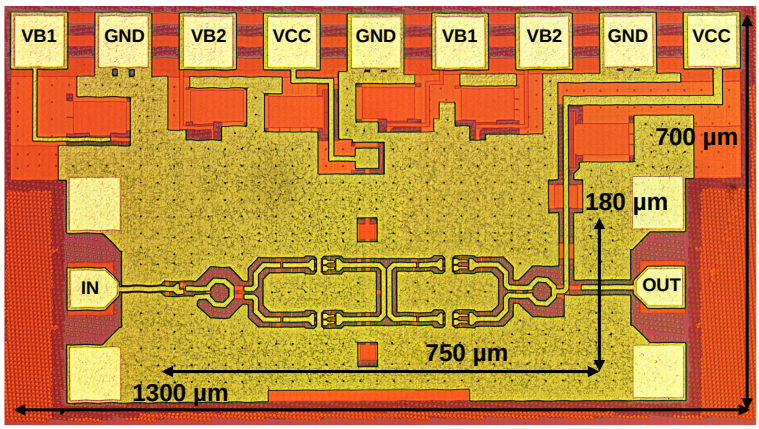


Figure 4.10. Photograph of the fabricated unit-PA.

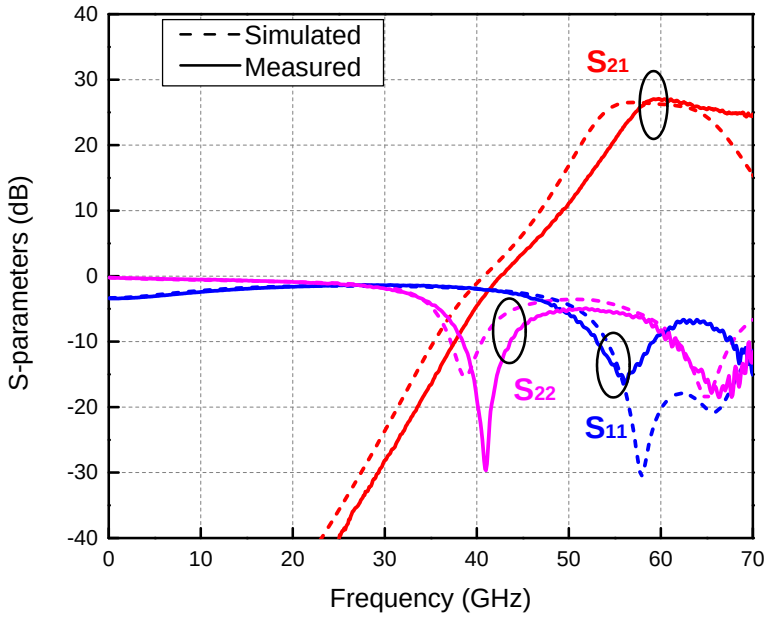


Figure 4.11. Measured and Simulated S-parameters of the unit-PA.

contact DC probes.

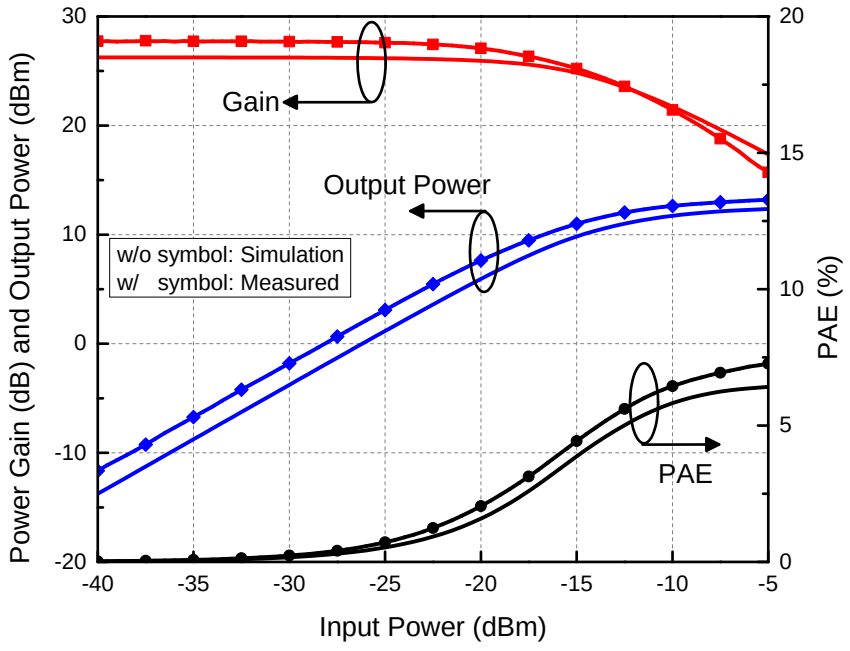
4.4.1 Performances of the Unit-PA

Figure 4.10 shows a photograph of the fabricated unit-PA. The total chip area including RF and DC probe pads and the core size are 1.3×0.7 mm^2 and 750×180 μm^2, respectively. The measured and simulated S-parameter results are plotted in Figure 4.11. As can be seen, all the measured results are well matched to the simulated ones. The measured gain (S_{21}) shifts to higher frequencies due to the difference between the estimated parasitics of the active devices used in the simulation and those of the actual devices. Due to the limitation of the equipment, measured data were only obtained up to 70 GHz. Specifically at 60 GHz, the measured and simulated gains are 27.3 and 26.2 dB, respectively, showing only 1-dB gain difference.

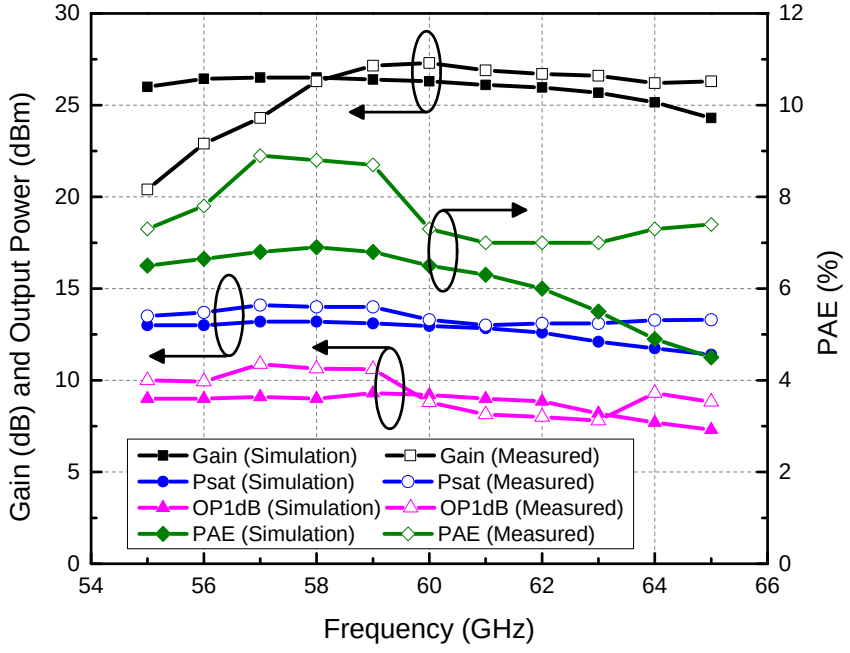
Figure 4.12(a) shows the simulated and measured power gain, output power, and power added efficiency (PAE) with respect to the input power at 60 GHz. At 60 GHz, the saturated output power (P_{sat}) is 13.3 dBm corresponding to the peak PAE of 7.3 %, and the output power at 1-dB compression point (OP1dB) is 9 dBm. Figure 4.12(b) shows the measured and simulated power gain, P_{sat}, OP1dB, and PAE between 55 and 65 GHz. The measured P_{sat} in this frequency range is over 13 dBm and the highest level is 14 dBm attained at 58 GHz. PAE of 7.3-9 % was measured in this frequency range.

4.4.2 Performances of the Complete PA

Figure 4.13 shows a microphotograph of the complete PA. The size of the actual core area is 1.65×0.85 mm^2 including bias networks while that of the chip including two RF and two DC pads is 2×1.3 mm^2. Figure 4.14 shows the simulated and measured S-parameters showing a good agreement between them. The overall measured small signal gain is lower than that simulated. Specifically, the measured gain



(a)



(b)

Figure 4.12. Large signal characteristics of the unit-PA: (a) power gain, output power and PAE at 60 GHz, and (b) power gain, maximum output power, output P1dB and PAE from 55 to 65 GHz.

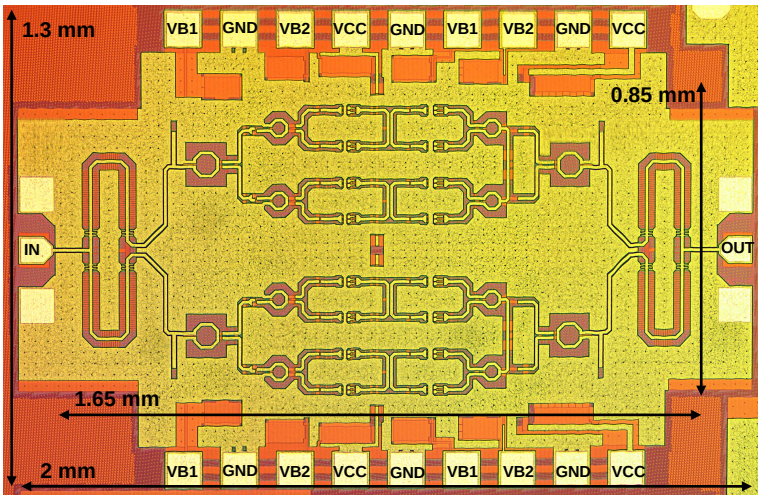


Figure 4.13. Photograph of the fabricated complete PA.

reaches a maximum of 19 dB at 60 GHz, which is 2.9 dB lower than the simulated gain. This discrepancy between the simulated and measured gains is mainly due to the unavoidable process variation. The measured 3-dB gain bandwidth also shifts to higher frequencies similar to that of the constituent unit-PA. The measured 3-dB gain bandwidth is 10.7 GHz from 56.8 to 67.5 GHz, which covers the entire unlicensed V-band spectrum. The simulated peak gain of the complete PA is 22 dB at 60 GHz, which is 4.2 dB lower than that of the unit-PA. This is due to the 1.35-dB loss of each of the four-way power combiner and divider used in the complete PA and additional losses caused by the interconnections between the power combiner/divider and four unit-PAs.

Figure 4.15(a) shows the measured and simulated power gain, output power, and corresponding PAE at 60 GHz. As can be seen, the P_{sat} is 18.8 dBm with peak PAE of 4.2 % and the OP1dB is 15.3 dBm. The measured saturated output power is slightly higher than that of the simulated result. The gain discrepancy between the simulation and measurement is already observed in the small-signal measurement

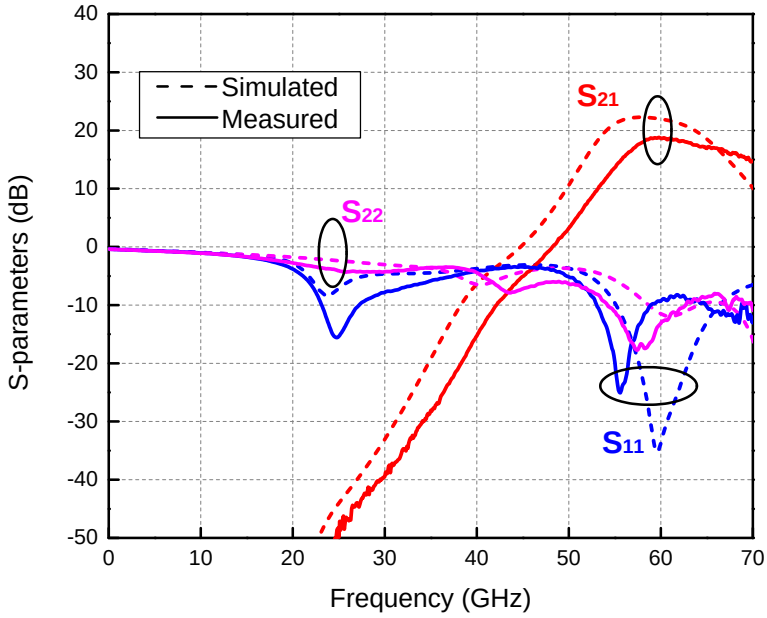
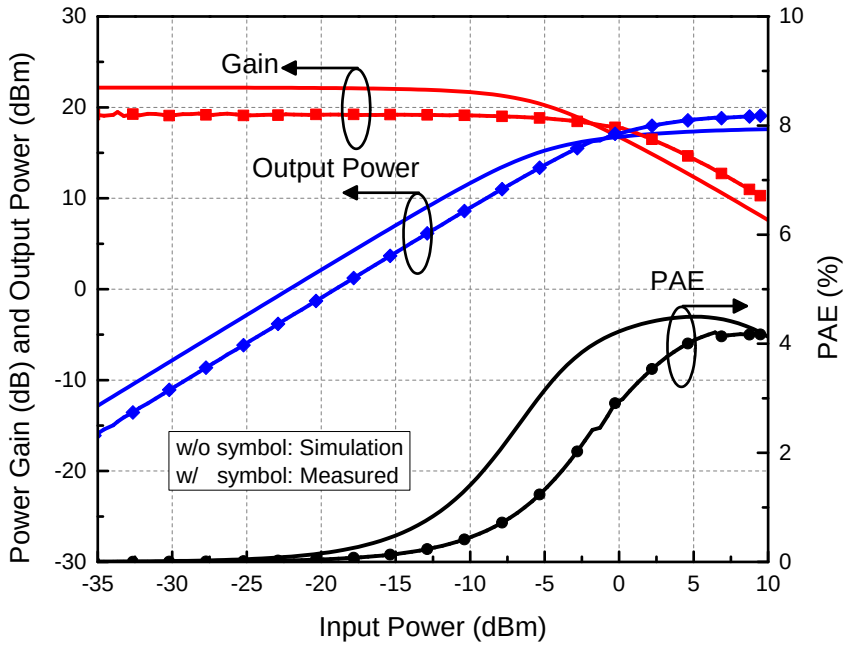


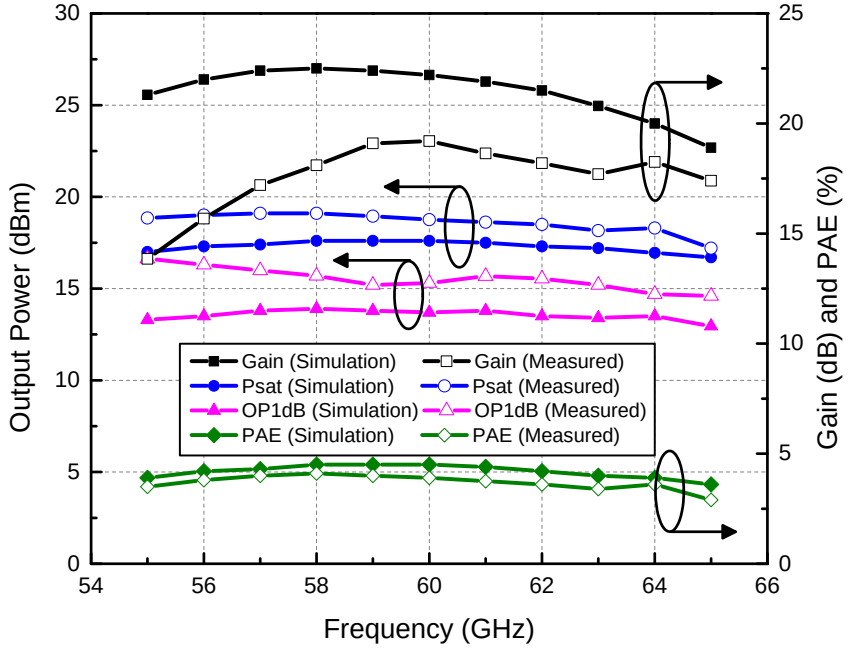
Figure 4.14. Measured and simulated S-parameters of the complete PA.

and, due to decreased measured power gain, the measured OP1dB is higher than the simulated one. The measured PAE is lower than the simulated result due to changes in biasing voltages used in the measurement. The power gain, P_{sat}, OP1dB, and PAE between 55 and 65 GHz are shown in Figure 4.15(b). Over this frequency range, the measured maximum output power is between 17 and 19.1 dBm and the measured PAE is 3-4.2 %. The highest output power, 19.1 dBm, is obtained at 58 GHz. Moreover, the measured OP1dB level is between 14.6 and 16.6 dBm. According to the results, the complete PA has very flat power performance over the 10-GHz bandwidth, which is attributed to the broadband characteristic of the implemented 4-way parallel power combiner/divider.

Table 4.2 summarizes and compares the performance of the developed V-band PA on 0.18-μm SiGe BiCMOS with other PAs recently reported in the literature at 60 GHz [43], [51–54], which use 40 to 90-nm CMOS technologies. The developed V-band



(a)



(b)

Figure 4.15. Large signal characteristics of the complete PA: (a) power gain, output power and PAE at 60 GHz, and (b) power gain, maximum output power, output P1dB, and PAE between 55 and 65 GHz.

PA produces the highest output power. In addition, higher 1-dB compressed output power is also observed among other works. The power gain of this PA is comparable to that of [52–54]. The 3-dB bandwidth is 10.7 GHz, which is much larger than other PA's except that of [51]. Although the PAs in [43], [52] and [54] have higher PAE than that of the developed PA, the P_{sat}, OP1dB, and 3-dB bandwidth performances of the developed PA are better. In general, as can be seen, the overall performance of the developed PA is good and comparable to those PAs designed with more advanced technologies.

4.5 Conclusion

This chapter presents the development of a V-band high output power PA on 0.18-μm SiGe BiCMOS process. The designed PA is formed by integrating four identical unit-PA cells and four-way parallel power combining and splitting networks. Each unit-PA cell is designed as two-stage pseudo-differential cascode amplifier. The proposed four-way parallel power combiner/splitter is comprised of a wideband low-loss capacitive loading slow-wave Wilkinson structure and two transformers connected in parallel at each branch of the Wilkinson device. It shows broadband performance with minimized phase and amplitude imbalances between ports. The developed PA achieves an output power of 18.8 dBm and power gain of 19 dB at 60 GHz. It also has very flat output power characteristic between 55 and 65 GHz. Moreover, its 3-dB bandwidth 10.7 GHz from 56.8-67.5 GHz covers the whole unlicensed V-band spectrum. The achieved good performance of the developed V-band PA demonstrates not only its usefulness for Si-based V-band wireless communication and radar systems, but also potential of developing high-performance Si PA's at higher mm-wave frequencies.

Table 4.2. Comparison of 60 GHz PA performance.

Reference	**This work**	[43]	[51]	[52]	[53]	[54]
Technology	**0.18 μm BiCMOS**	90 nm CMOS	65 nm CMOS	65nm CMOS	65 nm CMOS	40 nm CMOS
Frequency (GHz)	**60**	60	60.5	60	61	60
Gain (dB)	**19**	15.7	15.5	19.2	20	21.2
P_{sat} (dBm)	**18.8**	18.5	18.1	17.7	15.6	17.4
OP1dB (dBm)	**15.3**	14.7	11.5	15.1	13.5	14
PAE (%)	**4.2**	10.2	3.6	11.1	6.6	28.5
3 dB BW (GHz)	**10.7**	5.8	15	N/A	N/A	5.5
Topology	**2-stage CC + 4-Way Wilkinson and TXF combiner**	3-stage CS + 4-Way TXF Combiner	2-stage CC + 8-Way TL Combiner	3-stage CS + 4-Way TXF Combiner	2-stage CS + 4-Way TXF Combiner	3-stage CG+CS + 2-Way TXF Combiner

CS: Common Source structure, CC: Cascode structure
CG: Common Gate structure, TXF: Transformer
TL: Transmission Line

CHAPTER V

AN ULTRA-WIDEBAND LOW-LOSS MILLIMETER-WAVE SLOW-WAVE WILKINSON POWER DIVIDER*

In this chapter, an ultra-wideband low-loss millimeter-wave Wilkinson power divider, which has been developed on a 0.18-μm SiGe BiCMOS process, is described [44]. The miniaturization and low loss of the power divider are achieved by utilizing capacitive loading and a slow-wave CPW structure configured with floating metal strips periodically placed orthogonal to the CPW. The developed power divider has extremely wideband performance from DC to 67 GHz with less than 1-dB insertion loss from DC to 61 GHz, amplitude and phase imbalances less than 0.5 dB and 2 degrees from DC to 67 GHz, respectively, and isolation greater than 15 dB across 37-67 GHz. At 60 GHz, the designed power divider has only 0.9 dB of insertion loss and better than 25 dB of isolation. The core chip size is 150 $\mu m \times 525$ μm.

5.1 Introduction

Ultra-wideband passive and active microwave components operating within a certain band or across multiple bands are desirable in the quest for systems with bandwidths as wide as possible operating in either single-band or across multi-band. Wilkinson device first proposed in 1960 [55] is still widely used for power combining and dividing. Conventional Wilkinson power dividers, however, are relatively large

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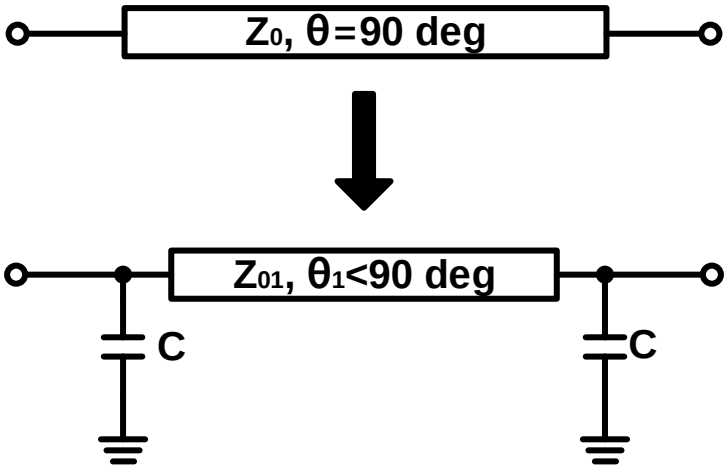


Figure 5.1. Capacitive loading technique.

due to the use of two quarter-wave transmission lines, making them not very suitable for silicon-based RFICs. Many researches have been carried out to reduce the size of the quarter-wavelength transmission lines and hence Wilkinson power dividers such as implementing lumped elements [32], capacitive and inductive loading [56], slow-wave [57, 58], elevated CPW [59], meander line with defected ground [60], and meander line with asymmetrical shunt-stub [61] for the transmission lines.

This chapter reports a compact and low-loss millimeter-wave Wilkinson power divider with an extremely wide bandwidth attainable by implementing capacitive loading together with a slow-wave CPW structure backed periodically with parallel metal strips orthogonal to the CPW. The developed Wilkinson power divider realized on a 0.18-μm SiGe BiCMOS process achieves an unprecedented ultra-wide bandwidth to 67 GHz with low insertion loss, decent isolation, and good amplitude and phase balances.

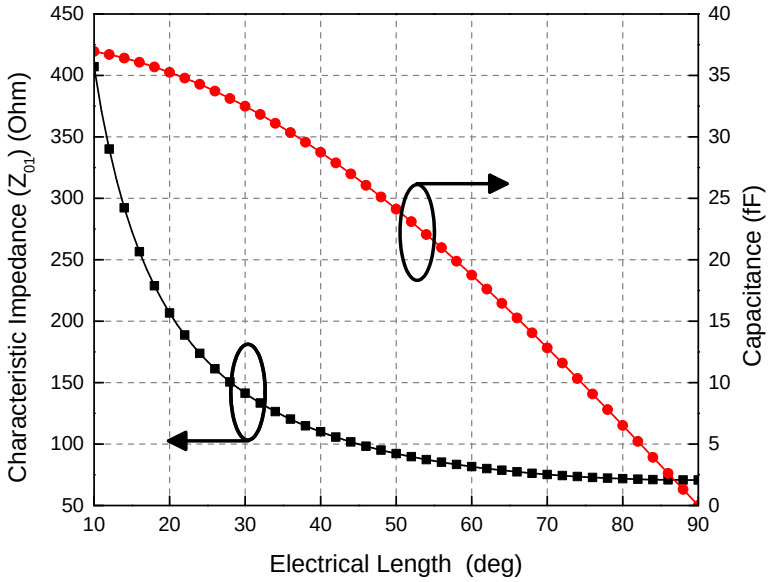


Figure 5.2. Characteristic impedance and loading capacitance versus electrical length of the modified transmission line at 60 GHz.

5.2 Design of Proposed Power Divider

The proposed Wilkinson power divider designed and fabricated using TowerJazz 0.18-μm SiGe BiCMOS process [14]. The design of the power divider including its constituent elements is described in the following subsections.

5.2.1 Capacitively Loading Transmission Line

Capacitive and inductive loading techniques have been used to reduce the length of the transmission lines in branch-line couplers and Wilkinson power dividers [56]. As shown in Figure 5.1, for the capacitive loading, a quarter-wavelength transmission line is replaced with a shorter transmission line of electrical length θ_1 loaded with shunt capacitors of capacitance C, where θ_1 and C are related as [56]

$$Z_{01} = \frac{Z_0}{sin(\theta_1)} \tag{5.1}$$

$$C = \frac{cos(\theta_1)}{\omega \cdot Z_0} \tag{5.2}$$

with Z_0 and Z_{01} being the characteristic impedances of the original $\lambda/4$ wavelength and modified shorter transmission lines, respectively. Figure 5.2 shows the characteristic impedance of the modified transmission line and the loading shunt capacitance with respect to the transmission line's length. As can be seen, a shorter transmission line requires a higher characteristic impedance and shunt capacitance. In most silicon IC processes, however, it is hard to implement transmission lines having characteristic-impedance higher than 100 Ω, thereby limiting possible reduction of the transmission-line length. Accordingly, for the employed 0.18-μm SiGe BiCMOS process, a transmission line having electrical length of 50° at 60 GHz and characteristic impedance of 92.3 Ω, loaded with shunt capacitors of 24.1 fF, is chosen for the power divider.

5.2.2 Metal-strip Backed Slow-wave CPW

While a transmission line shorter than a quarter-wavelength loaded with capacitors could be used to reduce the size of Wilkinson power dividers, as discussed in the foregoing section, the physical length is still relatively long for silicon technology. To further reduce the length, as well as to minimize the insertion loss of the transmission line, slow-wave CPW is employed for the selected capacitively loaded 50° transmission line. The slow-wave CPW is particularly designed to have floating parallel metal strips periodically placed orthogonal to the CPW on a metal layer under the signal line, which result in increased effective dielectric constant leading to reduced transmission line's physical length [62]. This slow-wave effect, however, adversely lowers the characteristic impedance of the transmission line because of the confinement of electric fields between the signal and ground lines, facilitated by the floating metal strips underneath. Therefore, a metal layer under the signal line needs to be properly

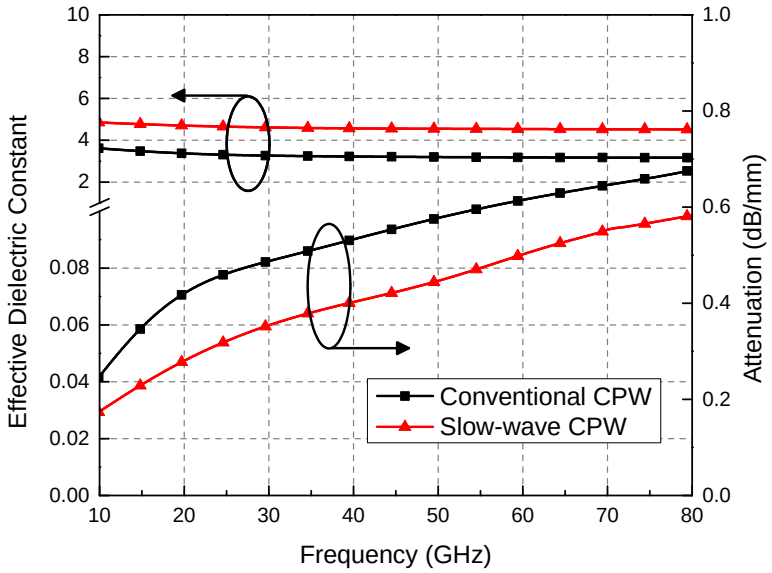


Figure 5.3. Effective dielectric constants and attenuation constants of the 92.3 Ω conventional and designed metal-strip backed slow-wave CPW's.

chosen for the floating metal strips to compensate between the desired increase in effective dielectric constant and the unwanted decrease in characteristic impedance. The signal line of the CPW is located on the topmost metal layer 6 (M6), which has the thickest metallization for low conductor loss. Placing the floating metal strips on the closest metal layer 5 (M5) would then maximize the slow-wave effect, yet making the designed 92.3- characteristic impedance unrealizable. Consequently, metal layer 4 (M4) is selected for the floating strips.

Figure 5.3 compares the effective dielectric constants and attenuation constants between the conventional and designed metal-strip backed slow-wave CPW's. As can be seen, the slow-wave effect realized with the periodic floating metal strips on M4 pushes the effective dielectric constant of the CPW from 3.1 to 4.5 at 60 GHz. Furthermore, the metal-strip backed slow-wave CPW has lower attenuation per unit length than the conventional CPW, which subsequently leads to further reduction in

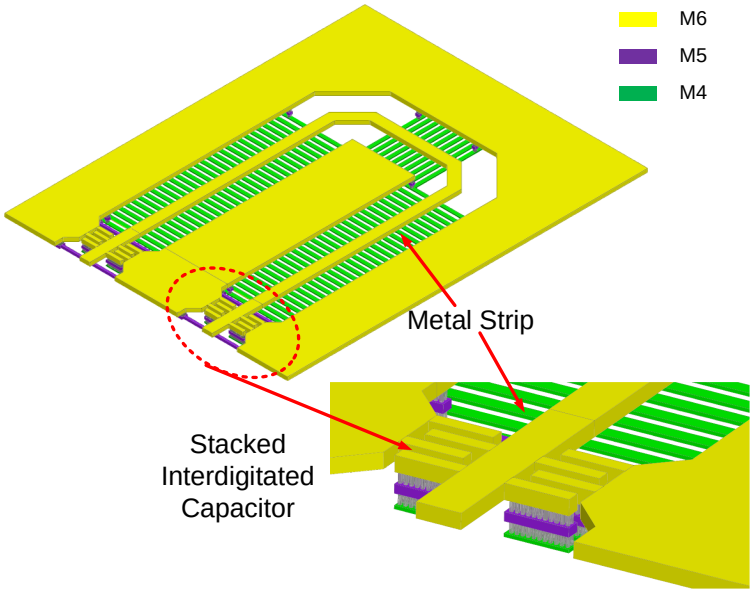


Figure 5.4. Capacitive loading metal-strip backed slow-wave CPW.

the overall insertion loss due to the resulting shorter transmission line.

5.2.3 Loading Capacitor

The metal-strip backed slow-wave CPW is terminated with 24.1-fF shunt capacitors, which are realized using interdigitated capacitors instead of metal-insulator-metal (MIM) capacitors available in the process design kit (PDK) to avoid possible problems with such small-sized MIM capacitors due to process variation. Using interdigitated capacitors, however, has a drawback of low capacitance density, which requires increased physical dimensions for capacitors. To overcome the low capacitance density of interdigitated capacitors, stacked multiple metal layers for each finger are utilized, which effectively increase the area between adjacent fingers, resulting in more capacitance as compared to that of conventional interdigitated capacitors having the same physical dimensions. In this context, the top three metal layers (M4, M5, and M6) are utilized for the stacked fingers of interdigitated capacitors.

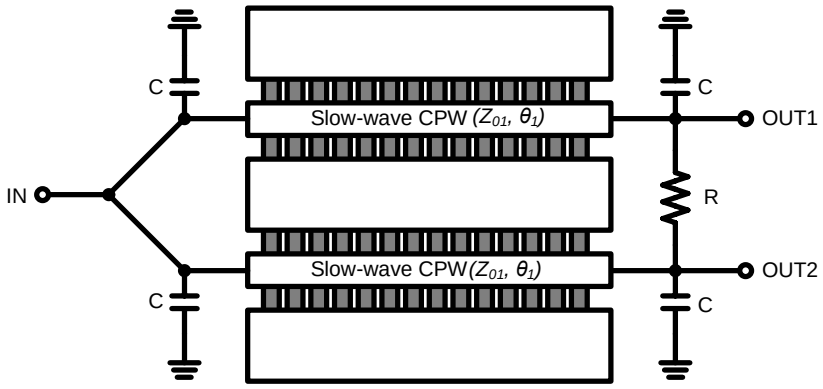


Figure 5.5. Schematic of the designed power divider.

5.2.4 Design of the Proposed Power Divider

Figure 5.4 shows the designed capacitive loading metal-strip backed slow-wave CPW. The signal line and two coplanar ground planes are implemented with M6 and the parallel metal strips for the slow-wave structure are formed on M4. The two interdigitated capacitors are placed at the ends of the slow-wave CPW. The fingers of these capacitors are placed symmetrically between the signal and two ground planes to maintain symmetry. All components except the resistor between the two arms are designed using the EM-simulator IE3D [15]. The width of the signal line and the gap between it and the ground planes are 8 and 20 m, respectively. Each finger of the interdigitated capacitor has 2.5-μm width, 2-μm gap, and 11.5-μm length on stacked metals M4-M5-M6. Figure 5.5 shows the schematic of the designed power divider.

5.3 Simulation and Measurement Results

Figure 5.6 shows a photograph of the fabricated power divider, which occupies a die size of 150 $\mu m \times 525$ μm without three RF pads. The power divider was measured on-wafer up to 67 GHz. Figure 5.7 shows the simulated and measured S-parameters.

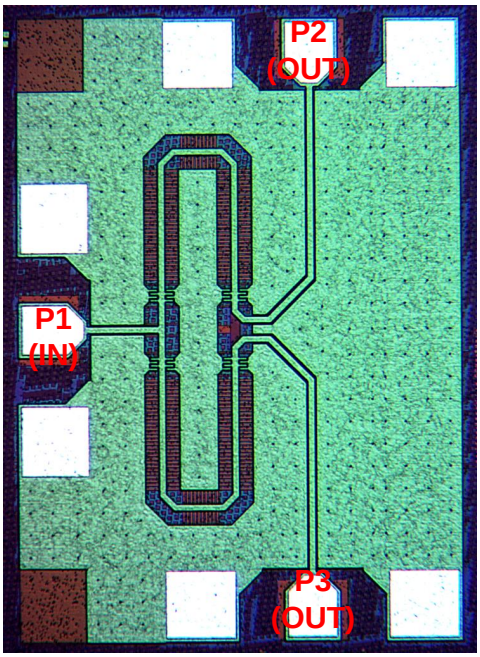


Figure 5.6. Photograph of the fabricated power divider.

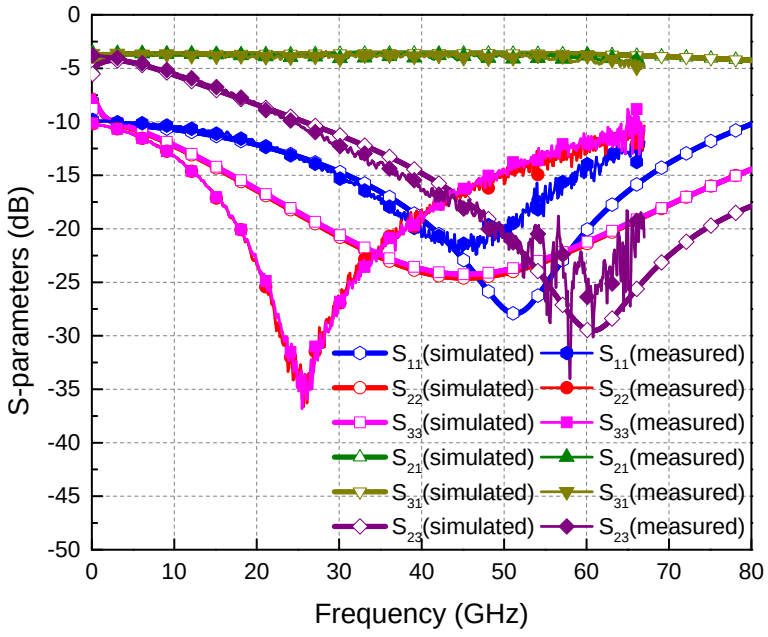


Figure 5.7. Simulated and measured S-parameters.

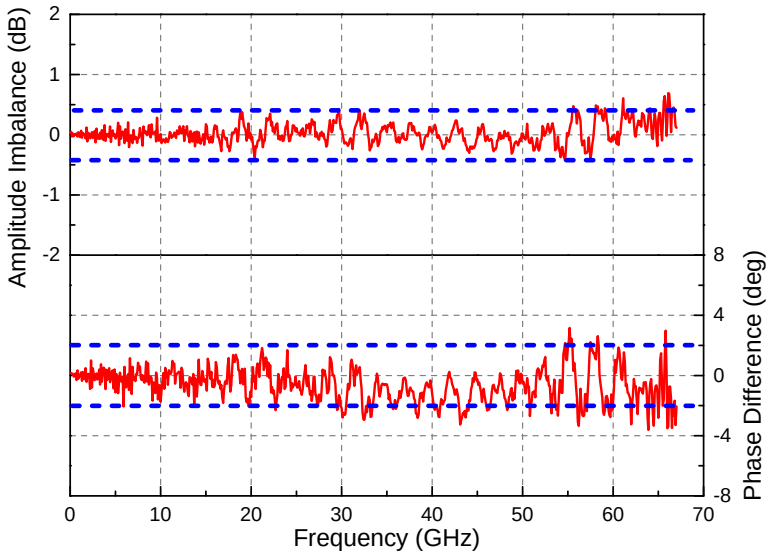


Figure 5.8. Measured amplitude and phase imbalance between two output ports.

The measured insertion losses (S21 and S31) are below 1 dB across DC to 61 GHz and well matched to those simulated in the measured frequency range of DC-67 GHz. At 60 GHz, these values are 0.7 and 0.9 dB, respectively. It is noted that the physical length of the slow-wave CPW is 310 μm, which is equivalent to around $\lambda/8$ at 60 GHz. This short length (in term or wavelength) coupled with a high characteristic impedance (92.3 Ω) make the slow-wave CPW behave approximately as an inductor. Each arm of the power divider, consisting of the slow-wave CPW and two shunt capacitors, hence behaves like a (semi) lumped low-pass network, leading to a very wideband performance for the power divider. The measured isolation between the two output ports (S23) is larger than 20 dB above 50 GHz. The measured input (S_{11}) and output (S_{22} and S_{33}) return losses are better than 10 dB up to 67 GHz. Figure 5.8 shows the measured amplitude and phase mismatches between the two output ports. Amplitude imbalance of less than 0.5 dB and phase mismatch smaller than 2 degrees are obtained from DC to 67 GHz. Table 5.1 compares the performance of the

designed power divider with other reported silicon-based Wilkinson power dividers at similar millimeter-wave frequencies. The proposed divider has the widest operating frequency range from DC-67 GHz, defined based on 10 dB return loss, with very low insertion loss (DC-67 GHz) and high isolation (37-67 GHz).

5.4 Conclusion

A millimeter-wave Wilkinson power divider on 0.18-μm SiGe BiCMOS process, implementing capacitive loading and slow-wave CPW configured with parallel metal strips periodically placed perpendicular to the CPW, has been developed with good performance over an extremely wide bandwidth. To the authors' best knowledge, this is the first silicon-based power divider with widest bandwidth having very low insertion loss from DC to 67 GHz and high isolation across 37-67 GHz. The designed slow-wave CPW configured with periodic metal strips orthogonal to the CPW could prove to be a viable transmission line for low-loss and miniature silicon-based RFICs.

Table 5.1. Comparison performances between designed power divider and reported power dividers in mm-wave region.

Ref.	Tech.	Topology	BW (GHz)	IL (dB)	Isolation (dB)	Amp. diff. (dB)	Phase diff. (°)	Area**
[59]	90 nm CMOS	Stub-loaded Elevated CPW	40-67*	2.3 @ 60G	13 @ 60G	0.07 @ 60G	0.22 @ 60G	0.051
[60]	180 μm Bi-CMOS	Defected grounding structure	40-70	1.5 @ 60G < 2 (40-70G)	>17 (57-66G) >15 (40-70G)	< 0.1 (DC-67G)	< 2 (DC-67 G)	0.09
[61]	90 nm CMOS	Asymmetrical shunt-stub	40-50	0.6-1.2	> 18	< 0.5	N/A	0.06
This work	**180 μm Bi-CMOS**	**Capacitive loading Slow-wave CPW**	**DC-67**	**< 1 (DC-61G)**	**> 20 (50-67G) > 15 (37-67G)**	**< 0.5 (DC-67G)**	**< 2 (DC-67G)**	**0.078**

*Based on meas. S_{21} and S_{11}, ** Area dimension: mm^2

CHAPTER VI

A SiGe BiCMOS CONCURRENT K/V DUAL-BAND 16-WAY POWER DIVIDER AND COMBINER

In this chapter, a new dual-band 16-way power divider and combiner on a 0.18-μm SiGe BiCMOS process that works concurrently over 18-26 GHz (K-band) and 57-64 GHz (V-band) is presented [63]. The 16-way K/V dual-band power divider integrates a two-way K/V dual-band Wilkinson-based power divider with a high-pass filter and multiple broad-band two-way lumped-element and transmission-line Wilkinson power dividers. The two-way dual-band power divider is designed by employing a slow-wave transmission line and two shunt-connected series LC resonators in each arm, leading to miniaturization and low loss with dual-band transmission in K- and V-band, decent return losses, and good isolation of larger than 20 dB over the dual-band. The developed 16-way K/V dual-band power divider possesses good performance over the dual-band. Specifically, it achieves measured insertion losses of 18.4 and 21 dB at 24 and 60 GHz, respectively, with good return losses. Furthermore, it also exhibits measured isolation larger than 20.1 and 17.7 dB between any two output ports at 24 and 60 GHz, respectively.

6.1 Introduction

Power combiners and dividers, either stand-alone components or parts of microwave and millimeter-wave (mm-wave) circuits, are essential for microwave and mm-wave systems. In some circuits such as power amplifiers or antenna-array feeding networks, they are necessary for optimum performance and/or circuit functionality.

As wireless communications and sensing advance to meet increased demands, a single system capable of multi-band performance becomes indispensable for reduced

cost and size as well as enhanced performance and capability. The issues of cost and size are even more pronounced for silicon-based systems. Recently, vigorous research activities in multi-band communication and sensing systems have driven the development of various multi-band components including power combiners and dividers with low loss and compact size. Power combiners and dividers are typically realized with passive elements, which occupy a relatively large area, making it undesirable to create a multi-band power combiner or divider by combining individual single-band counterparts, especially for silicon-based radio-frequency integrated circuits (RFIC). To minimize the area and hence cost, a multi-band power combiner or divider should be designed as a single component having multi-band function instead of combining separate power combiners or dividers, each optimized in a single band.

Several kinds of dual-band power dividers based on Wilkinson power divider [55] have been proposed using open-/short-circuited transmission lines [64–67], transmission lines with lumped elements [68–71], and coupled transmission lines [72, 73]. All reported dual-band Wilkinson-based power dividers are two-way, implemented as hybrid circuits, and do not operate at mm-wave frequencies. Furthermore, implementing these power dividers on RFIC could introduce large losses and dimensions due to employed cascaded transmission lines and long lengths of open-/short-circuited stubs and coupled lines, especially for power dividers with more than two dividing ways. Moreover, the reported power dividers, except [66], do not provide zero-transmission property between two bands, implying that the transmission characteristic is actually not distinctive dual-band. To support the development of microwave and mm-wave dual-band RFIC systems, especially those involving multiple channels such as phased arrays, compact, low-lost power combiners or dividers having more than two ways and distinctive dual-band characteristics need to be developed.

In this chapter, a new dual-band 16-way Wilkinson-based power divider on 0.18-

μm SiGe BiCMOS process, which works simultaneously over 18-26 GHz and 57-64 GHz in the K- and V-band, respectively, is presented. The dual-band 16-way power divider consists of a new dual-band two-way power divider and multiple wide-band two-way power dividers. The dual-band two-way power divider utilizes a dual-band slow-wave transmission line between two LC resonators in each arm and achieves good return losses for all ports, good isolation between outputs at two distinctive bands, and transmission zero for out-of-band signal suppression. The wide-band two-way power dividers implement either lumped elements or transmission lines. To the best of the my knowledge, this is the first developed concurrent 16-way dual-band power divider and combiner for microwave and mm-wave operations on RFIC.

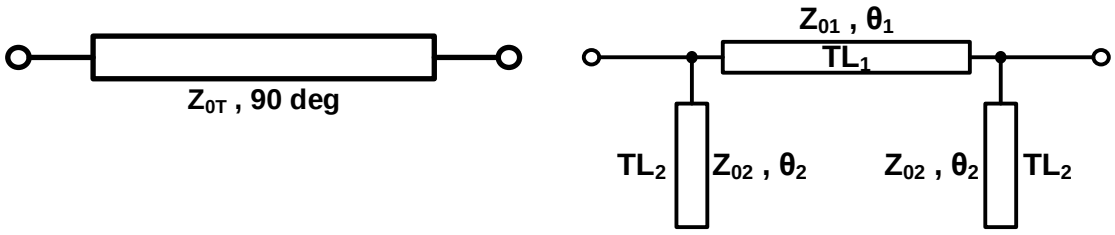
6.2 Two-way K/V Dual-band Power Divider

The two-way dual-band power divider is based on the Wilkinson power divider and consists of two dual-band slow-wave transmission-line networks and four shunt-connected LC resonators. In this section, the design methodology and analysis of the two-way K/V dual-band power divider are explained in details.

6.2.1 Dual-band Transmission-Line Network

Figure 6.1 shows a $\lambda/4$ transmission line of characteristic impedance Z_{0T} and its equivalence consisting of a transmission line (TL_1) and two identical open-circuited stubs (TL_2). The characteristic impedances and electrical lengths of these transmission lines are Z_{01}, Z_{02} and θ_1 and θ_2 , respectively. The ABCD matrix of the quarter-wavelength transmission line, assuming lossless, is given by

$$M_T = \begin{bmatrix} 0 & jZ_{0T} \\ jY_{0T} & 0 \end{bmatrix} \tag{6.1}$$



(a) (b)

Figure 6.1. (a) A $\lambda/4$ transmission line and (b) its dual-band equivalent network.

where $Y_{0T} = 1/Z_{0T}$. Also, the ABCD matrices for open stubs (M_{OC}) and cascaded TL (M_S) of the equivalent transmission line network shown in Figure 6.1(b) can be obtained as

$$M_S = \begin{bmatrix} cos\theta_1 & jZ_{01}sin\theta_1 \\ jY_{01}sin\theta_1 & cos\theta_1 \end{bmatrix} \tag{6.2}$$

$$M_{OC} = \begin{bmatrix} 1 & 0 \\ jY_{02}tan\theta_2 & 1 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ jY_{0C} & 1 \end{bmatrix} \tag{6.3}$$

The ABCD matrix of the equivalent lossless networks can then be derived as

$$\begin{aligned} M_{\Pi} &= M_{OC}M_SM_{OC} \\ &= \begin{bmatrix} \cos\theta_1 - Z_{01}Y_{oc}\sin\theta_1 & jZ_{01}\sin\theta_1 \\ jY_{01}\sin\theta_1(1 - Z_{01}{Y_{oc}}^2 + 2Z_{01}Y_{oc}\cot\theta_1) & \cos\theta_1 - Z_{01}Y_{oc}\sin\theta_1 \end{bmatrix} \end{aligned} \tag{6.4}$$

where $Y_{OC} = Y_{02}tan\theta_2$, $Y_{01} = 1/Z_{01}$ and $Y_{02} = 1/Z_{02}$. Equating (6.1) and (6.4) gives

$$Y_{oc} = Y_{02}\tan\theta_2 = Y_{01}\cot\theta_1 \quad \text{and} \quad Z_{0T} = Z_{01}\sin\theta_1 \tag{6.5}$$

In order for the equivalent network to have a dual-band operation, it should be electrically equal to the quarter-wavelength transmission line having an electrical length of $\pm 90^\circ$ as well as satisfy the following conditions [74]:

$$Z_{01} \sin \theta_{1(f_1)} = Z_{01} \sin \theta_{1(f_2)} = \pm Z_{0T} \tag{6.6}$$

where $\theta_{1(f_1)}$ and $\theta_{1(f_2)}$ are the electrical lengths of the transmission line TL_1 at frequencies f_1 and f_2 of the first and second pass-band, respectively. From (6.6), we obtain

$$\theta_{1(f_2)} = n\pi - \theta_{1(f_1)}, \quad n = 1, 2, 3, \ldots \tag{6.7}$$

Similarly, the electrical lengths $\theta_{2(f_1)}$ and $\theta_{2(f_2)}$ of the transmission line TL_2 follow

$$\tan \theta_{2(f_1)} = \frac{Z_{02}}{Z_{01}} \cot \theta_{1(f_1)} \quad \text{and} \quad \tan \theta_{2(f_2)} = \frac{Z_{02}}{Z_{01}} \cot \theta_{1(f_2)} \tag{6.8}$$

from which,

$$\theta_{2(f_2)} = m\pi - \theta_{2(f_1)}, \quad m = 1, 2, 3, \ldots \tag{6.9}$$

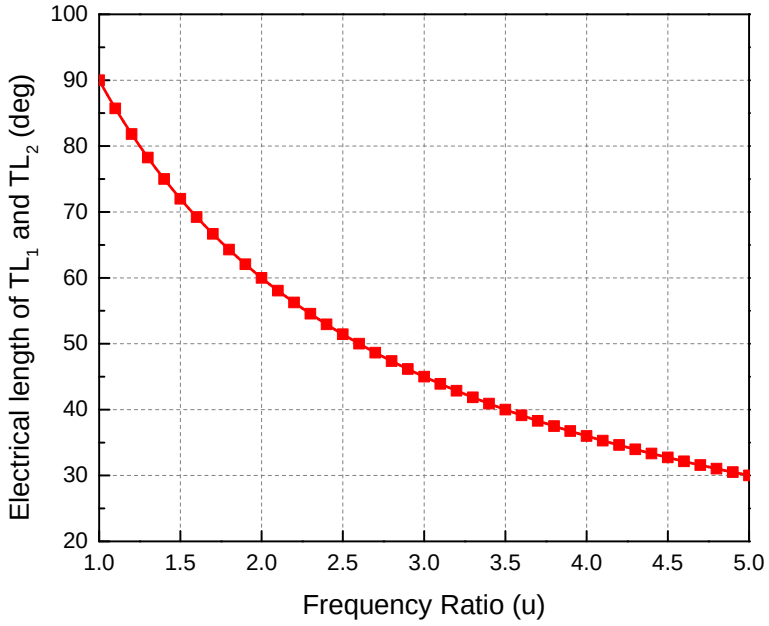
The frequency ratio between the two operating frequencies can be written as

$$u = \frac{f_2}{f_1} = \frac{\theta_{1(f_2)}}{\theta_{1(f_1)}} = \frac{\theta_{2(f_2)}}{\theta_{2(f_1)}} \tag{6.10}$$

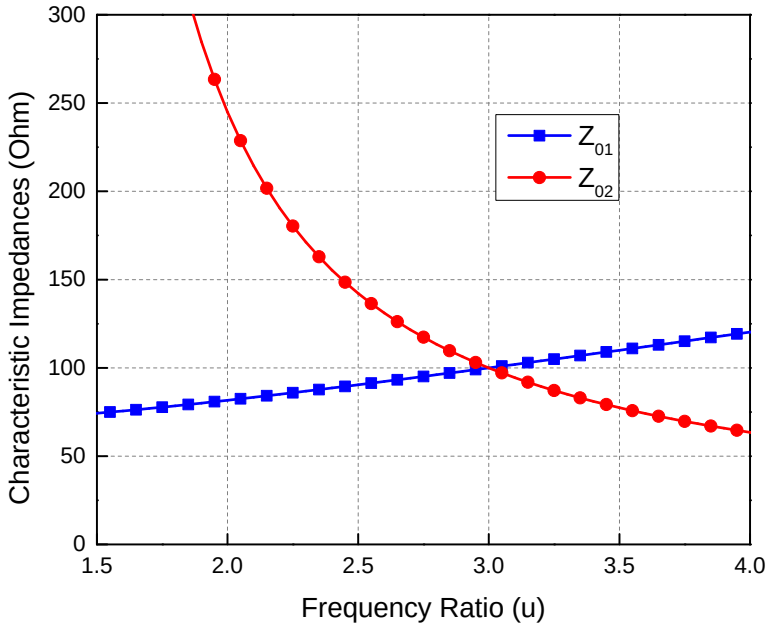
which, upon substituting into (6.7) and (6.9), yields

$$\theta_{1(f_1)} = \frac{n\pi}{u+1} \quad \text{and} \quad \theta_{1(f_2)} = \frac{n\pi u}{u+1} \tag{6.11}$$

$$\theta_{2(f_1)} = \frac{m\pi}{u+1} \quad \text{and} \quad \theta_{2(f_2)} = \frac{m\pi u}{u+1} \tag{6.12}$$



(a)



(b)

Figure 6.2. Parameters of the equivalent dual-band network: (a) electrical length of the cascaded transmission line (θ_1) and (b) characteristic impedance of the cascaded and shunt transmission lines versus frequency ratio (u).

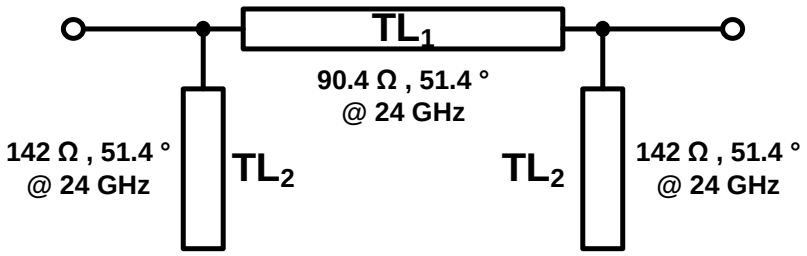


Figure 6.3. Equivalent dual-band transmission-line network.

For compact design, $n = m = 1$ is chosen, which leads to $\theta_{1(f_1)} = \theta_{2(f_1)}$ and $\theta_{1(f_2)} = \theta_{2(f_2)}$. Finally, the characteristic impedances of the transmission lines can be derived from (6.6) and (6.8) as

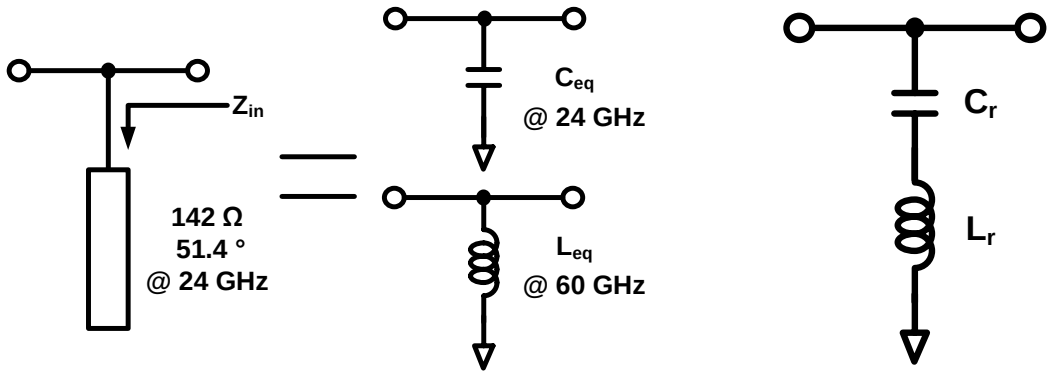
$$Z_{01} = Z_{0T}/sin\theta_{1(f_1)} \tag{6.13}$$

$$Z_{02} = Z_{01}tan\theta_{1(f_1)}tan\theta_{2(f_1)} \tag{6.14}$$

Figure 6.2 shows the electrical lengths and characteristic impedances of TL_1 and TL_2 with respect to the frequency ratio. For the design dual-band frequencies of 24 and 60 GHz, $\theta_1 = \theta_2 = 51.4^\circ$ at 24 GHz and $Z_{01} = 90.4\Omega$ and $Z_{02} = 142\Omega$. It is noted that the electrical lengths of TL_1 and TL_2 are the same due to the setting of $n = m = 1$. Figure 6.2(b) shows that, a higher characteristic impedance for TL_2 is required for a lower frequency ratio, which may not be realizable, hence possibly limiting the use of the dual-band equivalent network.

6.2.2 Series LC resonator for Shunt Open Stub

Figure 6.3 shows the equivalent dual-band transmission-line network including all design values for the K/V dual-band power divider obtained from the analysis in Section 6.2.1. The 142 Ω characteristic impedance of the two open stubs (TL_2), however, is not suitable for implementing on silicon substrate. To resolve this problem, a



(a) (b)

Figure 6.4. Open stub and its separate equivalence at 24 and 60 GHz (a), and equivalent LC network at both 24 and 60 GHz. (b)

technique to realize these open stubs is proposed as follows. The method is conceived by first investigating the input impedance of the open stub. The input impedance of an open stub (assumed to be lossless) is $Z_{OC} = -jZ_0 \cot\theta$, where Z_0 and θ are the characteristic impedance and electrical length at the operating frequency, respectively. At 24 and 60 GHz, the open stub has negative and positive input impedances, respectively, thereby acting as a capacitor (C_{eq}) and inductor (L_{eq}), respectively, as shown in Figure 6.4(a). This behavior is similar to that of a resonator, which has negative and positive reactances below and above its resonance frequency, respectively. Therefore, the shunt open stub can be replaced with a series LC resonator as illustrated at Figure 6.4(b), and the capacitance (C_r) and inductance (L_r) of the resonator can be determined by following conditions:

$$\omega_1 L_r - \frac{1}{\omega_1 C_r} = -\frac{1}{\omega_1 C_{eq}} \quad \text{and} \quad \omega_2 L_r - \frac{1}{\omega_2 C_r} = \omega_2 L_{eq} \tag{6.15}$$

which give

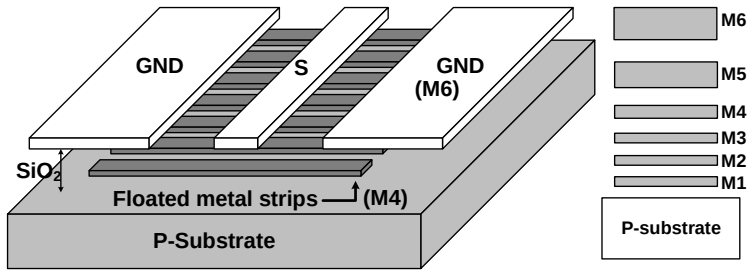
$$C_r = \frac{{\omega_2}^2 - {\omega_1}^2}{(\omega_1\omega_2)^2 L_{eq} + {\omega_2}^2 {C_{eq}}^{-1}} \tag{6.16}$$

$$L_r = \frac{{C_{eq}}^{-1} + {\omega_2}^2 L_{eq}}{{\omega_2}^2 - {\omega_1}^2} \tag{6.17}$$

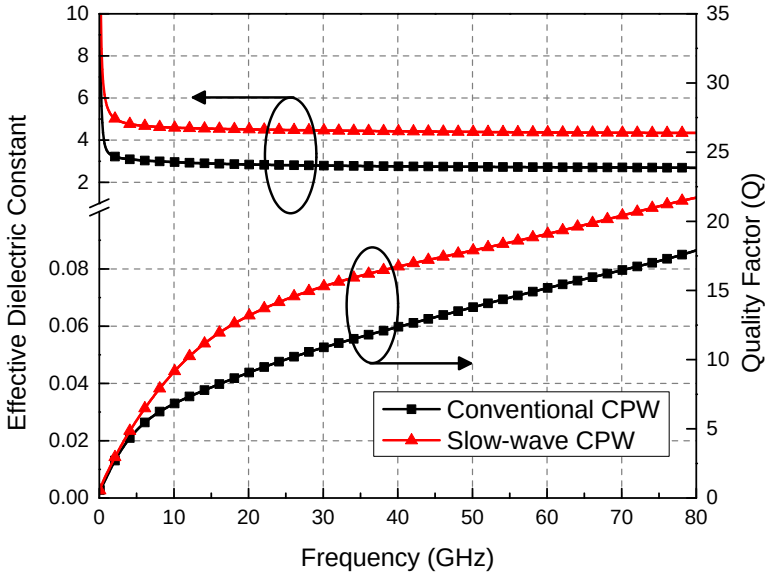
where ω_1 and ω_2 are two (radian) frequencies for dual-band operation. From equations (6.15)-(6.17), C_r =35 fF and L_r =501 pH can be obtained.

6.2.3 Slow-wave CPW for the Cascaded Transmission Line

The cascaded transmission line (TL_1) has 90.4 Ω characteristic impedance and 51.4° length at 24 GHz, as seen in Fig. 3. This transmission line length, even though is only slightly longer than $\lambda/8$, it is still considered long for implementation on silicon substrate. To further reduce the length and lower the loss of this transmission line, a slow-wave CPW is used. The slow-wave CPW consists of a signal line, two sided ground planes, and metal strips placed underneath and perpendicularly to the signal and ground planes as shown in Figure 6.5(a). These floating metal strips play a role in increasing the effective dielectric constant and hence reducing the physical length of the CPW. Furthermore, the floating metal strips reduce the electrical field penetration into the lossy silicon substrate, thereby reducing the loss. Proper choice for the floating strips' metal layer with respect to the signal's metal layer should be considered for the slow-wave CPW due to the trade-off between the slow-wave effect and characteristic impedance [44]. More slow-wave effect corresponding to more electrical field confinement leads to reduced length and lower characteristic impedance for the TL. To that end, the 90.4 Ω slow-wave CPW is realized with the signal and ground planes on the topmost metal layer (M6) and the floating metal strips on M4 layer. Figure 6.5(b) shows the comparison of the simulation results for the effective dielectric constants and quality factors between the conventional CPW



(a)



(b)

Figure 6.5. (a) Designed slow-wave CPW and (b) effective dielectric constant and quality factor of the conventional and designed slow-wave CPW.

and the designed slow-wave CPW. As expected, the effective dielectric constant of the slow-wave CPW is higher than that of the conventional CPW and particularly, those at 24 GHz are 4.5 and 2.8, respectively. Furthermore, the quality factor of the slow-wave CPW is improved as compared to that of the conventional CPW. The quality factor of a TL is defined as [75]

$$Q = \frac{\beta}{2\alpha} \tag{6.18}$$

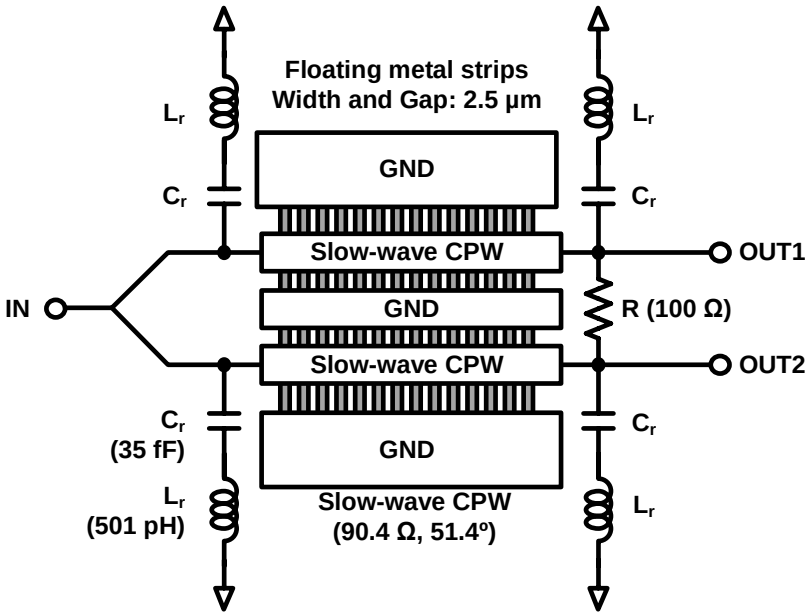


Figure 6.6. Schematic of the designed K/V dual-band Wilkinson power divider.

where α and β are attenuation and phase constants for the TL.

6.2.4 Design of the Two-way K/V-Band Power Divider

Figure 6.6 shows the schematic of the designed K/V dual-band Wilkinson power divider. It consists of a slow-wave CPW in each arm between two LC series resonators described earlier. The designed SWCPW has 5-μm width for signal line and 25-μm gap between it and the ground planes. The capacitors for the LC resonators are designed as interdigitated capacitors, each having 2.5-μm width, 2-μm gap, and 32-μm length on stacked metals M4-M5-M6. All components except the 100-Ω resistor between the two output arms are designed using ADS Momentum (Keysight Technology, Advanced Design System 2013 [49]).

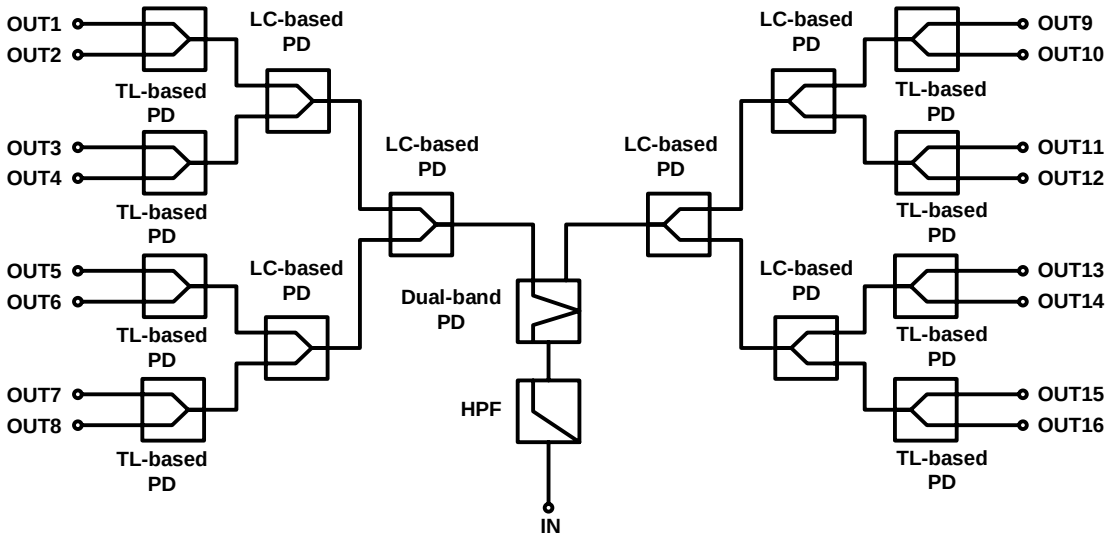


Figure 6.7. Block diagram of the 16-way K/V dual-band power divider consisting of a dual-band power divider (PD) and 14 broadband (TL- and LC-based) PD's.

6.3 Design of 16-way Dual-band Power Divider

In this section, the designs of the 16-way K/V dual-band power divider and its constituents, except the 2-way K/V dual-band power divider described in Section 6.2, are explained in details.

6.3.1 N-way Power Divider Topology

A simple way to design a dual-band N-way power divider is to utilize a dual-band N-way Wilkinson-based power divider. However, it is not easy to implement this structure in a planar configuration due to the connection of multiple resistors at the common node for $N \geq 3$ as can be inferred from the (singe-band) N-way Wilkinson power divider [75]. To overcome this difficulty, multiple two-way dual-band power dividers discussed in Section 6.2 can be cascaded together to realize a N-way dual-band power divider. This, however, would lead to a large chip size and increased loss, which are undesirable, especially for silicon implementation. To

alleviate this issue, we propose to use the dual-band two-way power divider only in the first stage while employing smaller-size broadband two-way power dividers in the subsequent stages to realize a compact 16-way power divider as shown in Figure 6.7. Both LC and transmission-line based broadband two-way power dividers are used for trade-off between size and isolation.

6.3.2 Two-way LC-Based Wilkinson Power Divider

Broadband lumped-element (LC) based two-way Wilkinson power divider is chosen for miniaturization. The LC-based power divider can be synthesized by converting the $\lambda/4$ length transmission line in each arm into an equivalent Π-network consisting of two shunt capacitors (C) and a series inductor (L) in between given by

$$L = \frac{Z_0}{2\pi f_0} \quad \text{and} \quad C = \frac{1}{2\pi f_0 Z_0} \tag{6.19}$$

where Z_0 is the transmission line's characteristic impedance and f_0 is the design frequency. The LC-based power divider exhibits broadband characteristic due to the inherent low-pass filter property of the equivalent Π-network. However, a single section of the LC-based WPD does not provide good broadband matching. Thus, multi-section LC-based WPD design needs to be considered for broadband matching at the expense of increased circuit size. In consideration of circuit size and matching bandwidth, two-section WPD design is chosen. Two sections are employed for the LC-based power divider to provide a wide passband up to around 70 GHz while still maintaining a relatively small size.

The two-section LC-based power divider is designed for Butterworth response. A two-section transmission-line power divider is initially designed using a single transmission line for the first section to reduce the number of elements for reduced loss and compact size, following [76], as shown in Figure 6.8. All the transmission

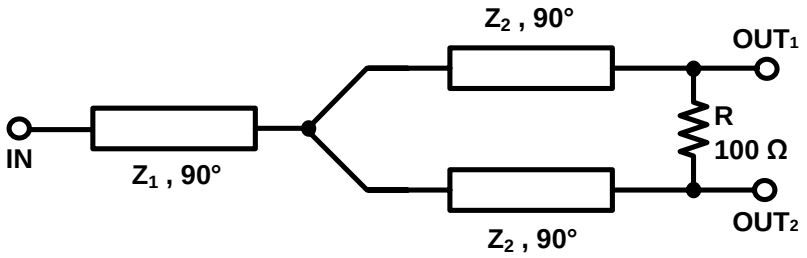
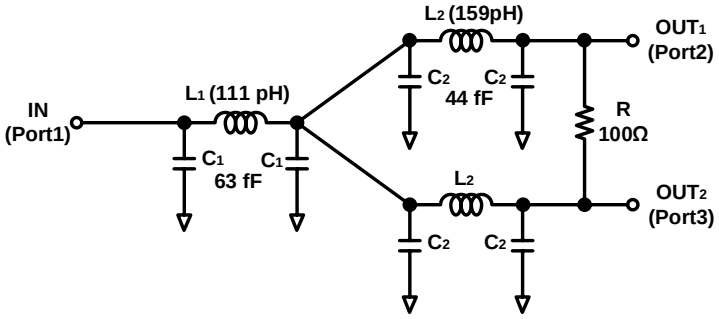


Figure 6.8. The schematic of two-sections Wilkinson power divider with TLs.

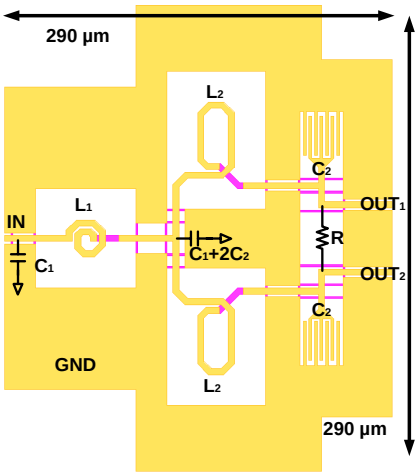
lines have 90° electrical length at 60 GHz, and their characteristic impedances Z_1 and Z_2 can be determined from the following binomial transformer equation [75]:

$$Z_{n+1} = Z_n \exp\left[2^{-N} C_n^N ln\left(\frac{Z_{out}}{Z_{in}}\right)\right] \tag{6.20}$$

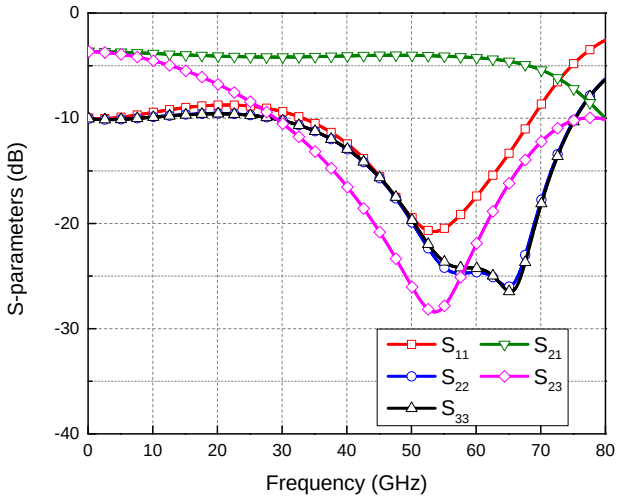
where $n = 1, 2$; N is the number of sections; C_n^N is the binomial coefficient; and Z_{in} and Z_{out} represent the input and output impedance of the binomial transformer, respectively. Substituting $N = 2$, $Z_{in} = 2Z_0$ and $Z_{out} = Z_0$ gives $Z_1 = 42\text{-}\Omega$ and $Z_2 = 60\text{-}\Omega$. The two-section LC-based power divider is then synthesized by converting the transmission lines of the power divider in Figure 6.8 to corresponding lumped elements Π-networks as shown in Figure 6.9(a). Figure 6.9(b) shows the physical layout of the two-section LC-based power divider with overall dimensions of 290 μm × 290 μm. The capacitor of the second section (C_2) is designed as a metal-stacked interdigitated capacitor instead of MIM capacitor due to its small 44-fF capacitance, which results in tiny dimensions for a MIM capacitor. All components except the MIM capacitor C_1 and resistor R are verified by the EM simulator Momentum (Keysight Technology, Advanced Design System 2013). Figure 6.9(c) shows the simulated S-parameters of the designed LC-based power divider, which



(a)



(b)



(c)

Figure 6.9. Schematic (a), layout (b), and simulated S-parameters of the designed two-section LC-based Wilkinson power divider (c).

indicate very flat S_{21} of around 4 dB up to 60 GHz and good return loss at all ports up to around 70 GHz. The isolation between the two output ports (S_{23}) in K-band, however, is not good, implying that this power divider should not be used at the last stage of the 16-way power divider.

6.3.3 Two-way Transmission-line Based Wilkinson Power Divider

To resolve the poor isolation problem in the K-band region of the LC-based power divider, a transmission-line based two-way Wilkinson power divider is chosen for the last stages of the 16-way power divider to enhance its overall isolation. In order to cover a broad band up to around 70 GHz, the transmission-line power divider is designed with two sections with Chebyshev response. Figure 6.10(a) shows the schematic of the designed two-section transmission-line power divider. Z_1 and Z_2 are the characteristic impedances of the $\lambda/4$ TL's at f_0, the mean value of the two operating frequencies, and R_1 and R_2 are the resistors needed for isolation purpose. Firstly, Z_1 and Z_2 can be obtained by using tabularized values in [75] and setting $\Gamma_m = 0.05$ with $N = 2$, maximum allowable reflection coefficient magnitude in passband, and given N, the total number of sections. Hence, 82Ω and 61Ω of Z_1 and Z_2 are achieved, respectively. Next, the value of the isolation resistors, R_1 and R_2, can be calculated by the following equations [77]:

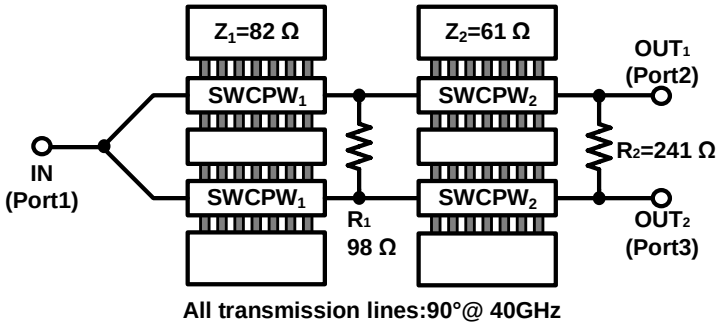
$$R_1 = \frac{2z_1z_2}{\sqrt{(z_1+z_2)\cdot(z_1-z_2\cot^2\theta_3)}} \tag{6.21}$$

$$R_2 = \frac{2R_1(z_1+z_2)}{R_1(z_1+z_2)-2z_1} \tag{6.22}$$

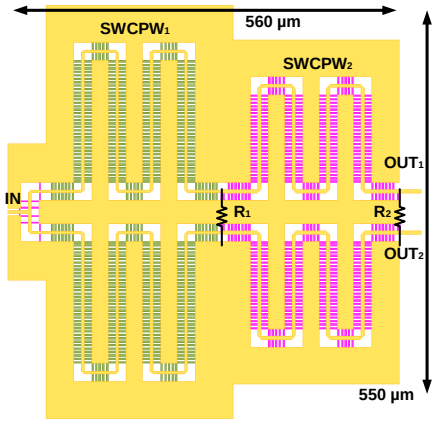
where

$$\theta_3 = 90^\circ\left[1-\frac{1}{\sqrt{2}}\left(\frac{f_H/f_L-1}{f_H/f_L+1}\right)\right] \tag{6.23}$$

$$z_1 = Z_1/Z_0 \quad \text{and} z_2 = Z_2/Z_0 \tag{6.24}$$



(a)



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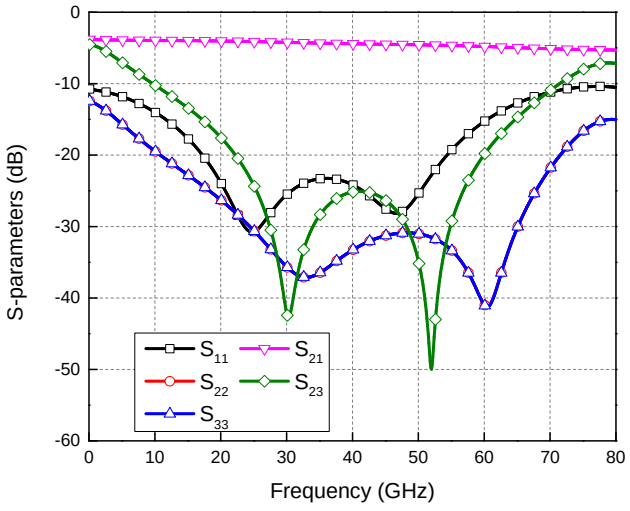


(c)

Figure 6.10. Schematic (a), layout (b), and simulated S-parameters of the designed two-section transmission-line Wilkinson power divider (c).

From Eqs. (6.21)-(6.24) and f_H/f_L, the ratio between the equal-ripple band-edge frequencies, the values of these two resistors are $R_1 = 98\Omega$ and $R_2 = 241\Omega$. It is noted that the electrical length of all TLs is 90° at 40 GHz, which is too long to be implemented on silicon substrate. Thus, the last procedure is to adopt a slow-wave structure for all TLs to achieve reduced physical structure.

Figure 6.10(b) shows the physical layout of the designed transmission-line power divider. Slow-wave CPW (SWCPW) is employed to reduce the lengths of the transmission lines. Considering the trade-off between the slow-wave effect and characteristic impedance mentioned in Section 6.2.3, the floating metal strips of $SWCPW_1$ and $SWCPW_2$ are realized on M4 and M5 metal layer, respectively. It is noted that the physical length of $SWCPW_2$ is shorter than that of $SWCPW_1$ due to larger slow-wave factor. Figure 6.10(c) shows the simulated S-parameters demonstrating broadband insertion loss, return loss, and isolation characteristics up to around 70 GHz. Particularly, at 24 and 60 GHz, the insertion losses are 4.1 and 4.8 dB, respectively, with good return losses and isolation higher than 20 dB in the interested frequency ranges.

6.3.4 16-way K/V Dual-band Power Divider

Figure 6.11 shows the total schematic of the designed 16-way K/V dual-band power divider. The two-way K/V-band dual-band power divider described in Section 6.2 is employed at the first stage to make the dual-band function in the K- and V-band. A simple high-pass filter (HPF) having 15-GHz cutoff frequency is located in front of the dual-band power divider to suppress signals lower than K-band frequencies. For miniaturization, the second and third stages of the network are composed of six designed two-section LC-based power dividers described in Section 6.3.2. Eight two-section transmission-line power dividers described in Section 6.3.3

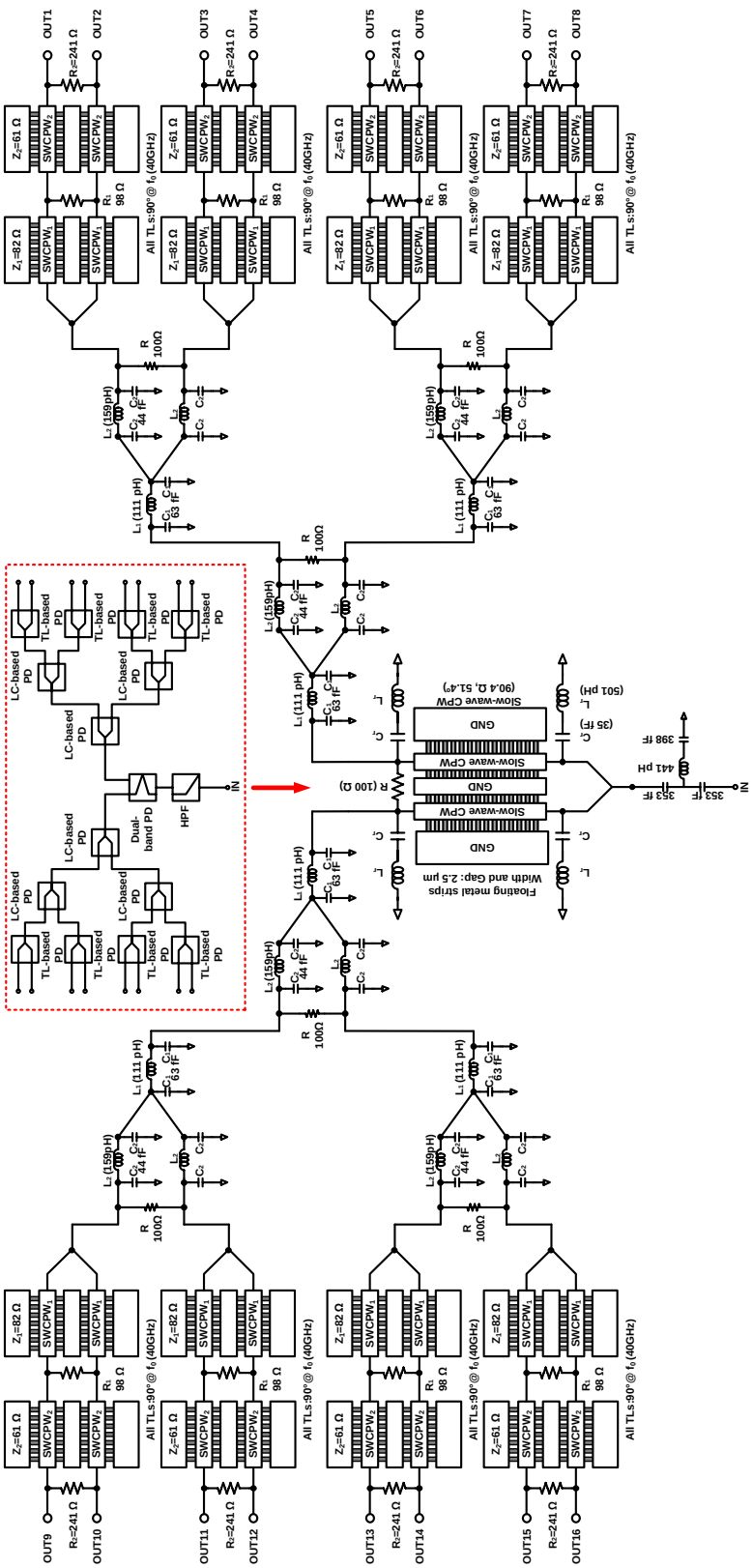


Figure 6.11. Block diagram of the 16-way K/V dual-band power dividing network.

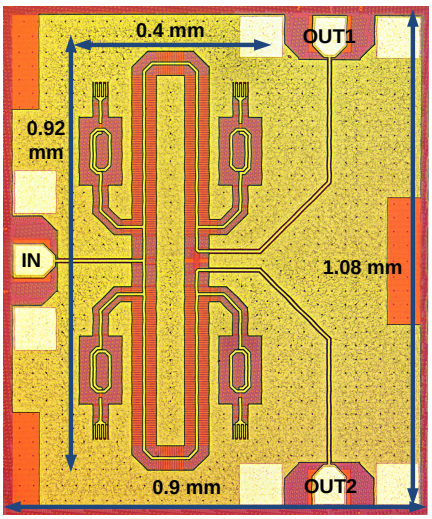


Figure 6.12. Photograph of the fabricated two-way dual-band power divider.

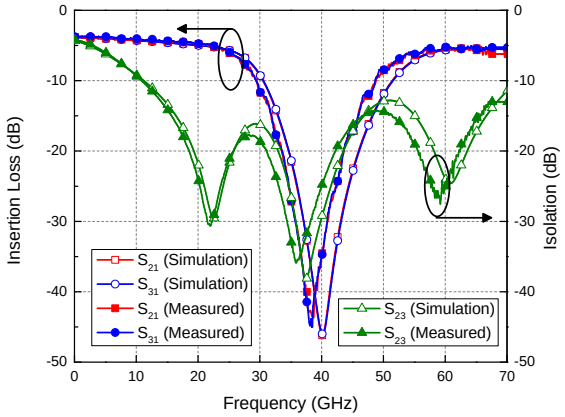
are employed for the last stages of the 16-way power divider to enhance its overall isolation.

6.4 Simulation and Measurement Results

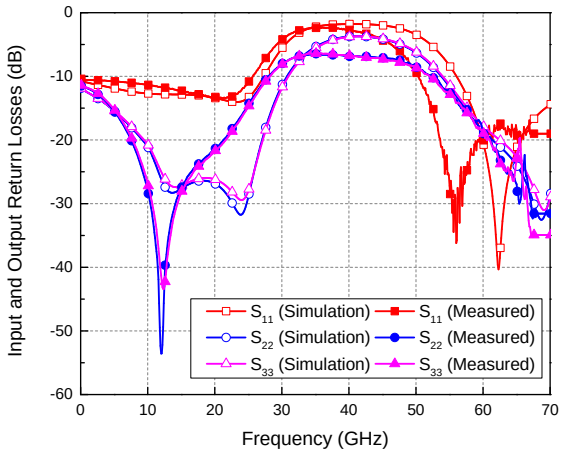
In this section, the simulated and measured data of the designed K/V dual-band two-way and 16-way power dividers are presented. All the simulation results include the EM-simulated data for passive elements as well as parasitic effects of their layouts extracted from the RCX simulation in Cadence (Cadence Design System, Assura). All circuits were fabricated with TowerJazz 0.18-m SiGe BiCMOS process [14]. Three-port S-parameter measurements were conducted on-wafer by using a vector network analyzer up to 67 GHz.

6.4.1 Two-way K/V Dual-band Power Divider

Figure 6.12 shows a photograph of the fabricated two-way K/V dual-band power divider. The chip size is 0.9 $\times$ 1.08 mm^2 with three RF probing pads and the



(a)



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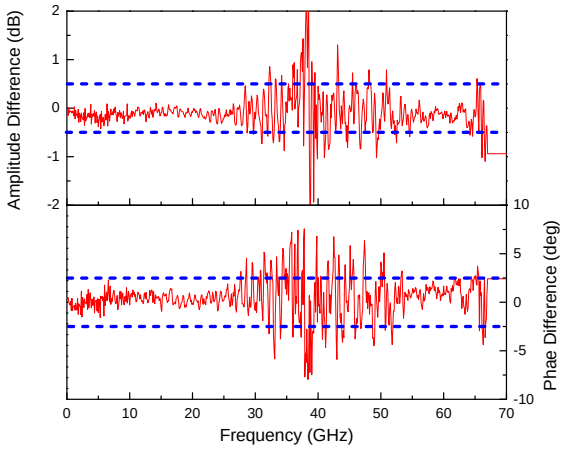


(c)

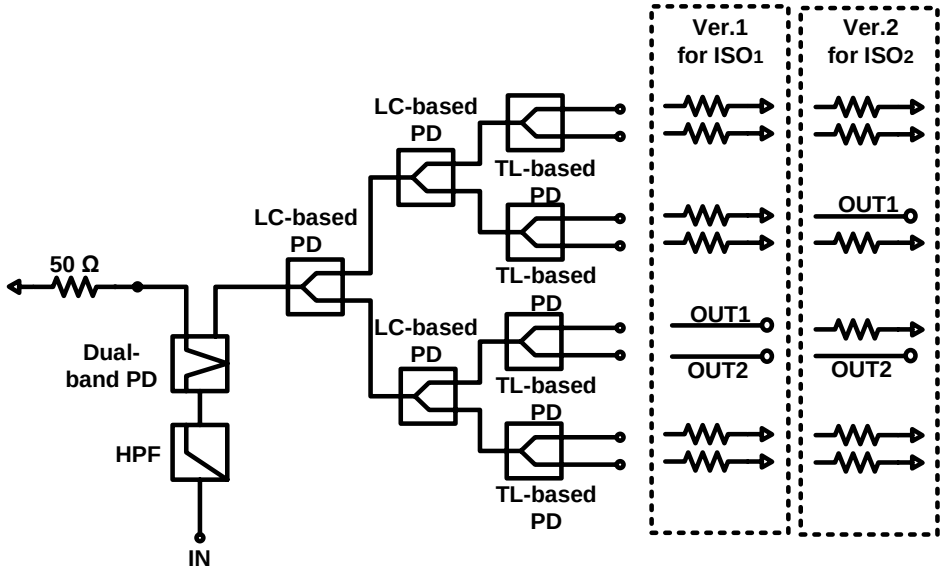
Figure 6.13. Simulated and measured S-parameters of the designed two-way dual-band power divider: (a) insertion loss and isolation, (b) return losses, and (c) amplitude and phase imbalances between two outputs.

core size is 0.4 × 0.94 mm^2. Figure 6.13(a) and 6.13(b) show the simulated and measured S-parameters and Figure 6.13(c) displays the measured amplitude and phase mismatches between the two outputs. As can be seen, all the measurement results are very well matched to the simulation ones. The measured insertion losses (S_{21} and S_{31}) at 24 and 60 GHz, as seen in Figure 6.13(a), are 5.5/5.3 and 5.4/5.3 dB, respectively while all ports are very well matched to the system impedance. Moreover, the measured isolation between the two outputs (S_{23}), as shown in Figure 6.13(a), is larger than 20 dB between 18.6-25.7 GHz and 55.6-62.4 GHz. Particularly at 24 and 60 GHz, 24 dB and 26.5 dB of isolation are achieved, respectively. The measured amplitude and phase mismatches are less than ±0.5 dB and ±2.5° across the interested frequencies in the K- and V-band, respectively.

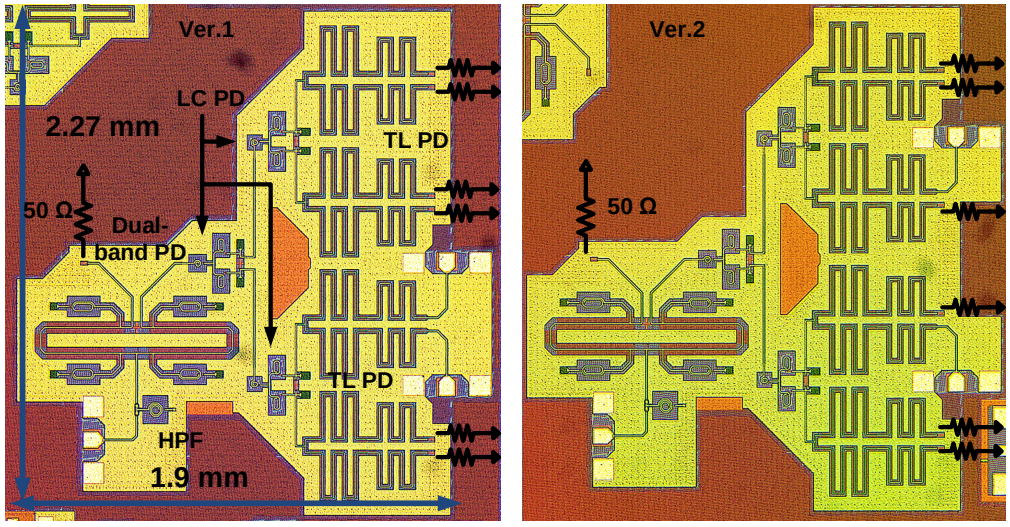
6.4.2 16-way K/V Dual-band Power Divider

To verify the K/V dual-band 16-way power distribution network with a limited die area, two halves of the 16-way power divider, each representing an 8-way power divider with 50-Ω terminations at un-used ports, as shown in Figure 6.14 were fabricated. Version 1 is used for measuring the isolation between OUT_1 and OUT_2 (the two adjacent output ports), while Version 2 is used for characterizing the isolation between OUT_1 and OUT_2 (the two outputs placed through the LC and transmission-line power dividers).

Figure 6.15 shows the simulated and measured S-parameters of the fabricated power dividing networks. As can be seen, the measured results are in very good agreement with those simulated. The two halves (versions 1 and 2) show similar insertion losses and return losses. The transmission characteristics shown in Figure 6.15(a) clearly show a dual-band shape due to the presence of the high-pass filter for suppressing low-frequency signals, two-way dual-band power divider with trans-



(a)



(b)

Figure 6.14. Two half section versions of the 16-way dual-band power divider with different output ports and terminations: (a) block diagrams and (b) photographs.

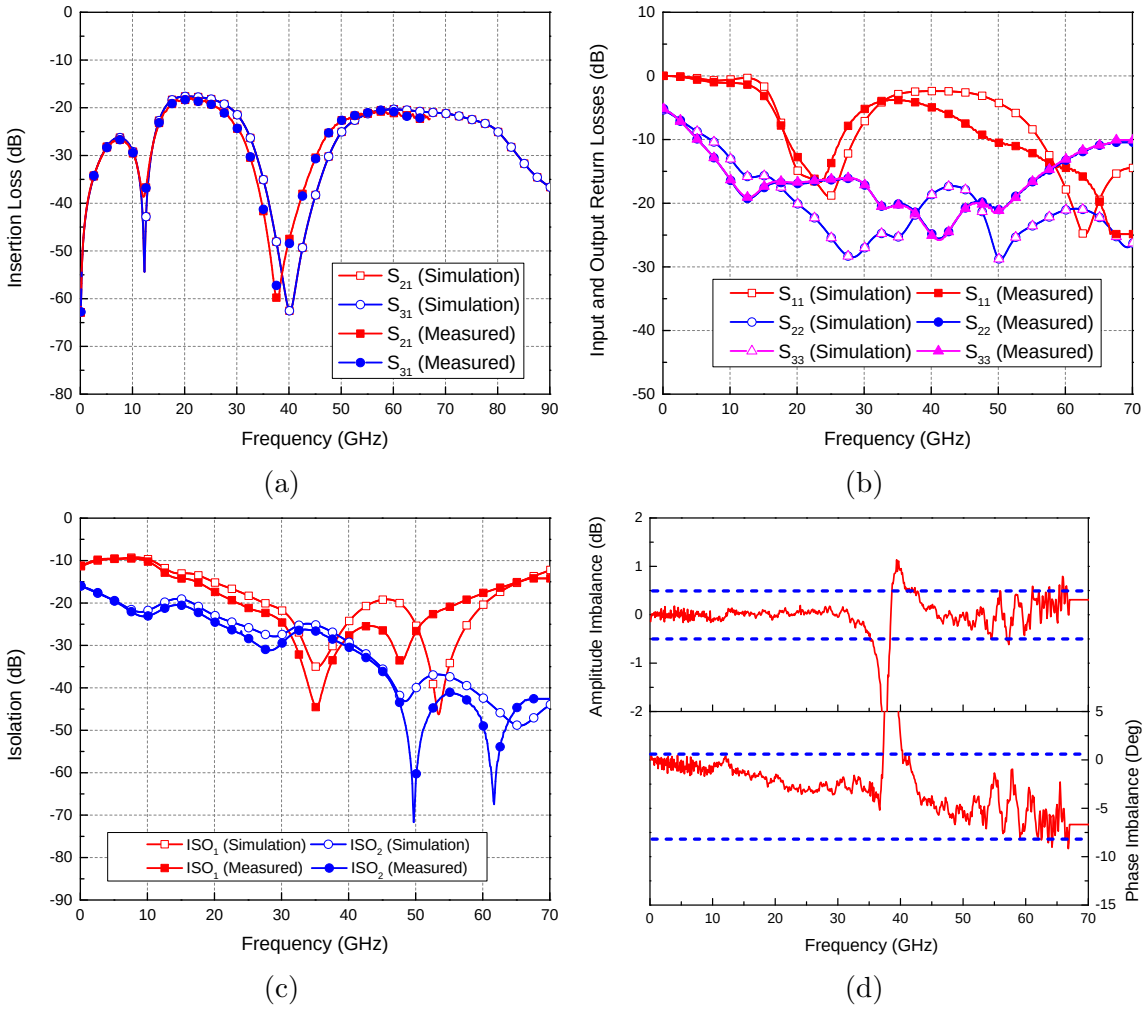


Figure 6.15. Simulated and measured S-parameters of half-sections of the 16-way dual-band power divider: (a) insertion loss, (b) input and output return losses, (c) isolation between two output ports, and (d) amplitude and phase mismatches between two outputs.

Table 6.1. Projected measured performance for the 16-way dual-band power divider.

Parameters		18-26 GHz (K-band)	57-64 GHz (V-band)
Insertion Loss (dB)		18.8-19.8 18.4 @ 24 GHz	21-22 21 @ 60 GHz
Return Loss (dB)	Input	> 12 16.2 @ 24 GHz	> 13 14.5 @ 60 GHz
	Output	> 16 16.2 @ 24 GHz	> 11.5 13.6 @ 60 GHz
Amplitude Imbalance (dB)		<0.19 0.19 @ 24 GHz	<0.5 0.2 @ 60 GHz
Phase Imbalance (°)		< 3.2 2.5 @ 24 GHz	< 7.8 6.3 @ 60 GHz
Isolation (dB)	Between 2 closest ports	> 15 20.1 @ 24 GHz	>15.7 17.7 @ 60 GHz
	Between other 2 ports	>22.6 26.6 @ 24 GHz	>41 48.4 @ 60 GHz

mission zeros, and inherent low-pass filter response of the LC-based power dividers. Specifically, the measured insertion losses (S_{21} and S_{31}) are 18.4 and 21 dB at 24 and 60 GHz, respectively, with good input and output return losses. The isolation attributes between two output ports are shown in Figure 6.15(c). The measured isolation between two nearest ports shown in Version 1 (ISO_1) is 20.1 and 17.7 dB at 24 and 60 GHz, respectively, while that between non-adjacent ports shown in Version 2 (ISO_2) is 26.6 and 48.4 dB at 24 and 60 GHz, respectively. As expected, ISO_2 is higher than ISO_1 since the two output ports corresponding to ISO_2 are located farther at two different last-stage power dividers that are connected by the second- and third-stage power dividers. Finally, Figure 6.15(c) shows that the measured amplitude and phase mismatches are less than ± 0.5 dB and 7.8° across the interested

dual-band frequencies of 18-26 and 57-64 GHz. The measured performance of the entire 16-way power divider can be deduced from that measured for its half-sections as shown in Table 6.1.

6.5 Conclusion

A new dual-band 16-way power divider and combiner that works concurrently across 18-26 GHz and 57-64 GHz of the respective K- and V-band has been developed on a 0.18-μm SiGe BiCMOS process. The 16-way power divider integrates a new K/V dual-band two-way power divider, realized using slow-wave transmission lines and LC series resonators, and multiple broad-band two-way lumped-element and transmission-line power dividers. Good measured performance has been obtained for both the K/V dual-band 16-way and 2-way power dividers. To the authors' best knowledge, these are the first silicon-based mm-wave dual-band 16-way and 2-way power dividers reported. Good measured performances obtained for both the K/V dual-band 16-way and 2-way power dividers demonstrate not only their usefulness for power distribution in Si-based K/V dual-band circuits and systems, but also possibilities of developing larger silicon on-chip power distribution networks for microwave and millimeter-wave circuits and systems that operate over multiple bands simultaneously.

CHAPTER VII

A K/V-BAND DIPLEXER

In this chapter, the K/V-band diplexer designed using 0.18-μm SiGe BiCMOS technology is presented [78]. The proposed diplexer consists of two types of bandpass filters for K- and V-band and a T-junction matching section. For the K-band bandpass filter, an L-coupled resonator topology is utilized and a C-coupled resonator topology is chosen for the V-band bandpass filter. All of the filters are realized based on 2nd order Chebyshev response. To combine the two filters, a T-junction matching section, employing a high-impedance slow-wave CPW, is inserted at the common input node. The measurement results show very well agreement to the simulation results. Particularly, 4.1 and 4.8 dB of the insertion losses at 24 and 60 GHz are obtained, respectively, while return losses of all ports are larger than 10 dB. In addition, the isolation between the two bands is higher than 40 dB. The chip area of the proposed diplexer is 900 μm $\times$ 800 μm including three RF probe pads.

7.1 Introduction

Filters and diplexers are some of the crucial passive components in RF wireless communication and sensing systems. A typical duplex wireless communication system utilizes diplexers to transmit and receive signals through a single antenna. Diplexers can be also used to separate a common input signal to two individual outputs in dual-band systems. Diplexers are typically employed to connect two individual filters operating at different frequencies. For the design of diplexers, footprint size, insertion loss, and matching as well as isolation should be considered. Employing a T-junction matching network at the common port is most popular one to achieve good return loss. Since the two filters should not affect each other, the

proper T-junction matching network has to be designed. Some techniques for designing T-junction network have been reported in the literature [79, 80]. From the viewpoint of size, the simplest ways of reducing the diplexer size is to miniaturize the two constituent filters.

7.2 Design of K- and V-band Bandpass Filters

To realize a diplexer, two filters such as low-pass, high-pass, and bandpass filters are necessary. For simplicity, low-pass and high-pass filters can be utilized for a diplexer design, but these do not provide rejection of unwanted signals for each band. To resolve this issue, two bandpass filters (BPFs) are often employed to form a diplexer at the expense of increasing chip area and loss since BPFs normally have more elements compared to low-pass filters (LPFs) or high-pass filter (HPFs), assuming the same order is used for all filters. Due to this reason, the insertion loss of BPFs is worse than that of LPFs or HPFs at microwave and mm-wave ranges, and hence BPF design with low loss becomes important. In this section, two kinds of BPFs design are presented in details in K- and V-band.

7.2.1 Microwave Bandpass Filters

Filters are two-port networks used to control the frequency response in microwave systems by providing good transmission of desired signals while attenuating unwanted signals. In this context, the design goal is to minimize transmission loss within passband while rejecting unwanted signals in stopband. Typically, there are four types of filters: low-pass, high-pass, bandpass, band-stop (also called band reject or notch).

Microwave filter design typically starts from low-pass filter (LPF) synthesis and this method consists of the following steps [75, 81]:

1) Design of a prototype low-pass filter with the desired passband characteristics.

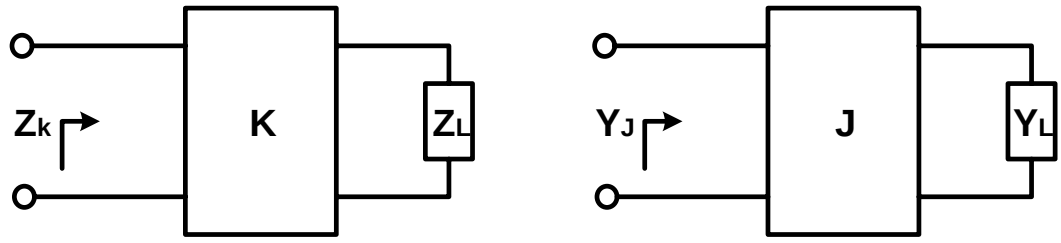
2) Transformation of the initial designed low-pass prototype to the wanted type (low-pass, high-pass, bandpass, or band-stop) filter with the center and/or band-edge frequencies specifications.

3) Realization of the network with lumped and/or distributed elements.

For a low-pass filter design, the insertion loss method has been utilizing extensively. In this method, the design of the filter stars with the specifying the insertion loss or the return loss for a lossless network over the desired frequency band. After that, the network with determined insertion loss can be synthesized [82]. Two possible solutions are commonly used for synthesizing low pass filter network with insertion loss method: Butterworth and Chebyshev responses. Butterworth, also called maximally flat, response provides the flat passband response as much as possible so that the transmission property is smooth. The drawback of it, however, is that attenuation characteristic is also gentle. On the contrary, Chebyshev response produces sharp cut-off and attenuation property at the expense of presence of equi-ripple in the passband. In this sense, one of them can be chosen as an insertion loss method depending on the specific application requirements for designing a low pass filter network.

When a BPF is synthesized by converting from LPF with certain specification, very small values of lumped elements could be produced, which are not realizable with the available process technology and this gives rise to the need of other types of BPF for practical design. Furthermore, larger numbers of lumped elements are introduced by converting from LPF, thereby leading to increased complexity and insertion loss. In this context, K- (impedance) or J- (admittance) inverters, shown in Figure 7.1(a) and 7.1(b), are utilized to modify the complicated network.

The impedance inverter or admittance inverter is a circuit, which provides input



(a) (b)

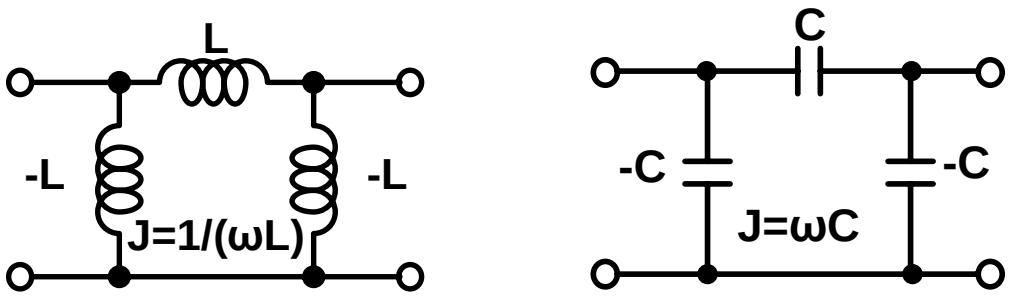
Figure 7.1. K-(impedance) inverter (a) and J-(admittance) inverter (b).

impedance or input admittance inversely proportional to the load impedance or admittance, respectively [81]. The impedance and admittance seen from the input can be expressed by following equation:

$$Z_K = \frac{K^2}{Z_L} \quad \text{and} \quad Y_J = \frac{J^2}{Y_L} \tag{7.1}$$

From equation (7.1), it is obvious that the load impedance or admittance can be converted into an arbitrary impedance or admittance by choosing an appropriate K or J value. Also, these inverters operate like a quarter wave transformer with a characteristic impedance or admittance of K or J at all frequencies [81]. Besides a quarter wave transformer, there are some other lumped-element networks that can act as inverters such as two admittance inverters shown in Figure 7.2. It is noticed that some component values are negative. Although it is not practical to realize such capacitors and inductors, they will be absorbed by adjacent lumped components.

There are two types of BPF that are widely used and simplified by J-inverters: C- (capacitive) and L- (inductive) coupled BPFs. The C-coupled BPF consists of shunt parallel LC resonators coupled via series capacitors. On the other hand, the shunt resonators coupled via series inductors makes the L-coupled BPF. These two



(a) (b)

Figure 7.2. Admittance inverters using lumped elements (a) inductors, and (b) capacitors.

topologies use more reasonable values of components as well as allow for easier control of the passband response by tuning their own resonators. The remarkable difference between them is the attenuation characteristic in their stop-band due to the fact that stop-band and skirts of these topologies are asymmetric. In case of the C-coupled BPF, the stop-band and skirt above the passband are worse than those below the passband. On the contrary, for L-coupled BPF, the stopband and skirt below the passband are worse than above the passband. The two BPFs for the K/V-band diplexer are designed by employing these two topologies with the 2^{nd} order Chebyshev equi-ripple response and are explained in details in the following sections.

7.2.2 C-coupled Bandpass Filter: V-band BPF Design

For designing the V-band BPF, the first step is to synthesize a LPF prototype with Chebyshev response. Table 7.1 shows the parameter setting to achieve LPF prototype and the elements values can be calculated by the equations in [82]. By using MATLAB [83] with the equations, the element values with respect to various

Table 7.1. Parameters for LPF synthesis.

Parameters	Values
Input Resistance	50 Ω
Output Resistance	50 Ω
Passband Ripple	0.25 dB

Table 7.2. Element values for equi-ripple LPF prototypes.

0.25 dB ripple						
Order (N)	g_1	g_2	g_3	g_4	g_5	g_6
1	1	0.486	1			
2	1	1.113	0.687	1.619		
3	1	1.303	1.146	1.303	1	
4	1	1.378	1.269	2.055	0.850	1.619

number of filter's order are obtained and shown in Table 7.2. Although a higher order filter provides better filter response, more number of elements are required resulting in increased complexity and insertion loss. In this sense, 2^{nd} order prototype has been chosen for LPF synthesis to compromise the filter's response and loss. After completion of the LPF synthesis, it is converted to BPF and employed J-inverter to reduce the number of components further.

Figure 7.3 shows the transformed BPF with two identical shunt resonators and three J-inverters that come from the 2^{nd} order LPF. The targeted two edge frequencies of the passband (ω_1 and ω_2) are set to 52 and 67 GHz and the element values from Table 7.2 for $N = 2$, the values of the elements for shunt resonators and J-inverters can be found. The fractional bandwidth (FBW) can be calculated as

$$FBW = \frac{\omega_2 - \omega_1}{\omega_0} \tag{7.2}$$

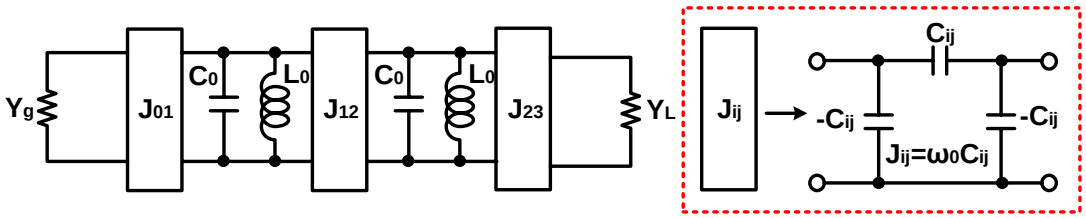


Figure 7.3. A transformed BPF using two identical resonators and capacitive J-inverters.

where $\omega_0 = \sqrt{\omega_1 \omega_2}$ is the center frequency of passband. Next, the inductor of the shunt resonators (L_0) is set to a reasonable value for realization as 50 pH to reduce the inductor's physical size as well as loss. Since the resonance frequency of the resonator is the same as ω_0, the capacitor of the resonators (C_0) can be obtained as

$$C_0 = \frac{1}{\omega_0^2 L_0} \tag{7.3}$$

and 145.5 fF is attained. Now, J-inverters' coefficients are given by following equations

$$J_{12} = \omega_0 C_0 FBW \sqrt{\frac{1}{g_1 g_2}} \tag{7.4}$$

$$J_{01} = J_{23} = \sqrt{\frac{\omega_0 C_0 FBW}{g_0 g_1 Z_0}} \tag{7.5}$$

where $FBW = 0.2542$, g_1 and g_2 are the elements values of LPF for $N = 2$, and hence the values of $J_{12} = 0.01568$ and $J_{01} = J_{23} = 0.01570$ are attained. If the J-inverter is replaced to the equivalent Π- network consisting of three capacitors as shown in Figure 7.3, then $C_{12} = 42.3$ fF is achieved from J_{12}. In case of C_{01} and C_{23}, the absorption of the negative capacitance does not work between the end resonators and the generator and load pure resistance, and another equivalent circuit is required.

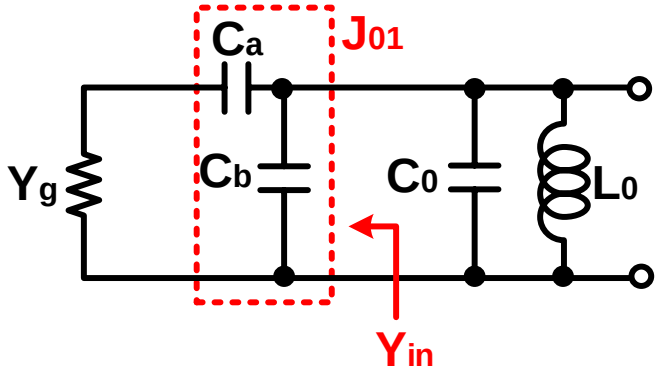


Figure 7.4. Equivalent inverter between the end of resonator and the termination.

Thus, an inverter can be realized by using only two capacitors as shown in Figure 7.4. If the termination impedance is Z_0, the admittance Y_{in} is given by

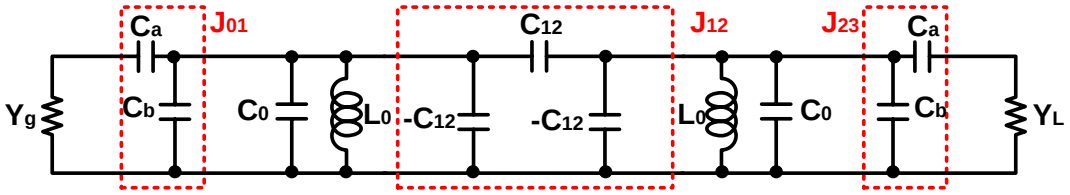
$$Y_{in} = \frac{J_{01}^2}{Y_g} = J_{01}^2 Z_0 = j\omega_0 C_b + \frac{1}{\frac{1}{j\omega_0 C_a} + Z_0} \tag{7.6}$$

From above equation (7.6), the values of two capacitor can be obtained as following:

$$C_a = \frac{J_{01}}{\omega_0 \sqrt{1 - (J_{01} Z_0)^2}} = 68.3 \text{ fF} \tag{7.7}$$

$$C_b = -\frac{C_a}{1 + (Z_0 \omega_0 C_a)^2} = -26.2 \text{ fF} \tag{7.8}$$

Figure 7.5(a) shows the schematic of the C-coupled BPF with two shunt resonators and three J-inverters realized by $\Pi-$equivalent network, and the final version of schematic is depicted in Figure 7.5(b). Table 7.3 shows the parameters' values on the final schematic. The capacitor of the resonators (C_0) absorbs shunt and negative



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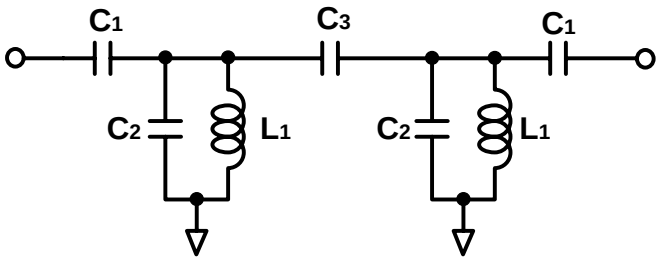

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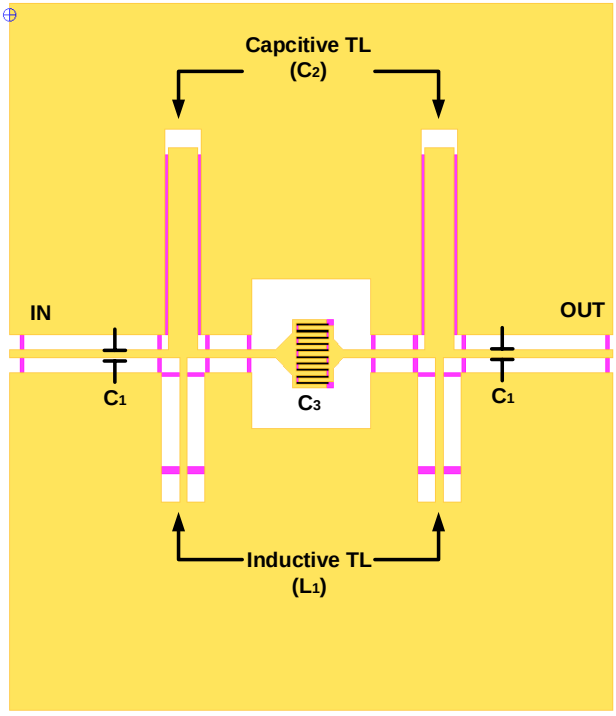


(c)

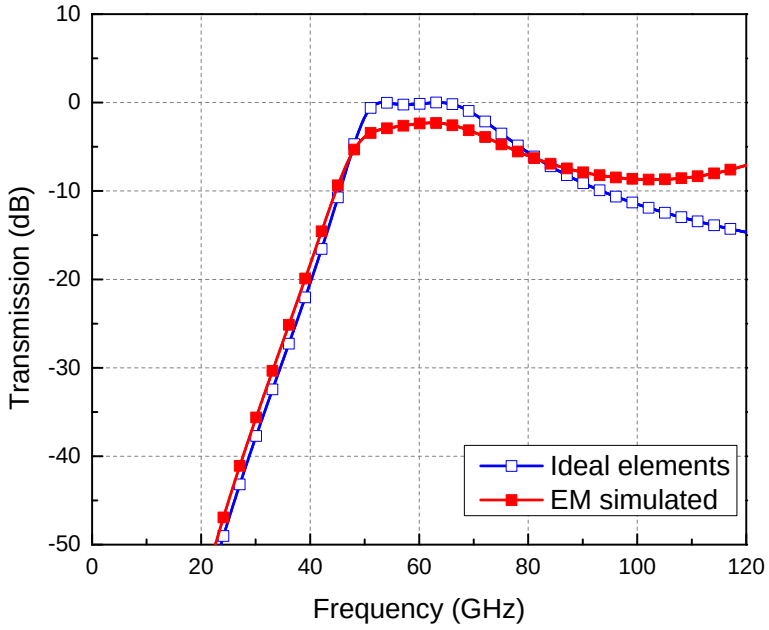
Figure 7.5. Designed C-coupled BPF:(a) schematic with J-inverters and two shunt resonators, (b) the final schematic, and (c) physical layout.

Table 7.3. Parameters of designed C-coupled BPF.

Parameters	Values
$C_1 = C_a$	68.3 fF
$C_2 = (C_b \parallel C_0 \parallel -C_{12})$	77 fF
$C_3 = C_{12}$	42.3 fF
$L_1 = L_0$	50 pH

capacitors of J-inverters (C_b and C_{12}). Figure 7.5(c) exhibits the layout of the designed V-band BPF. The capacitor of C_1 is realized with MIM capacitor. Also, the inductor and capacitor on the resonators, L_1 and C_2, are implemented by using the short-circuited inductive transmission line and capacitive open stub, respectively. In case of C_3, the value is too small to be realized as an MIM capacitor due to very tiny physical dimension of such MIM capacitor leading to vulnerable process variation, hence a metal interdigitated capacitor, mentioned in the previous Chapter V, is utilized for implementing C_3. All transmission lines, interconnection, and interdigitated capacitor except C_1, MIM capacitor, are verified by using the EM simulator, ADS Momentum [49].

The S-parameters' simulation results with ideal elements and EM-verified elements are shown in Figure 7.6. As expected, the results of the final design with EM-simulated elements are close to the one with ideal elements. In the final design, no passband ripple can be found and it has 2.4 dB of insertion loss, since loss is taken into account in all components thereby leading to increased insertion loss performance as compared to that with ideal elements. Also, it is noted that the attenuation characteristic at out of bands is asymmetric, which is sharper at the frequency range below passband than upper passband as depicted in Figure 7.6(a).



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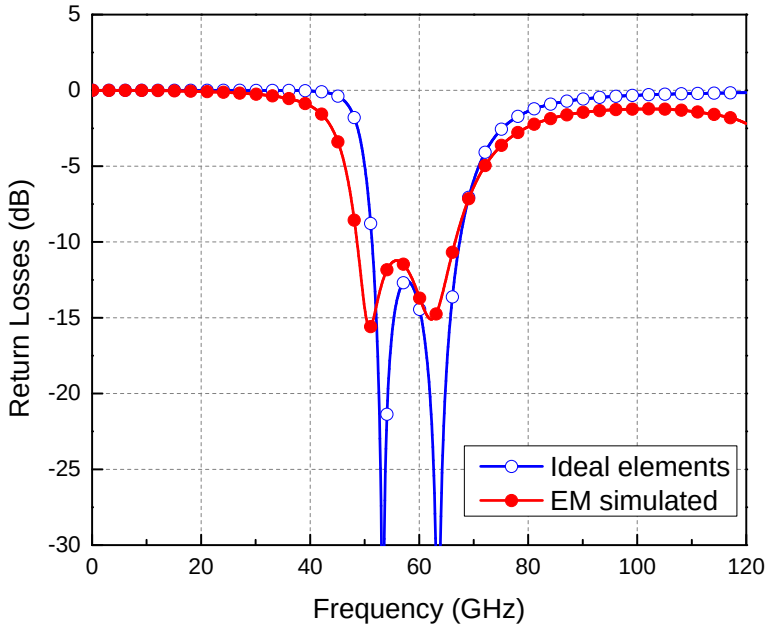


(b)

Figure 7.6. Simulation results of the designed V-band C-coupled BPF (a) transmission and, (b) return losses.

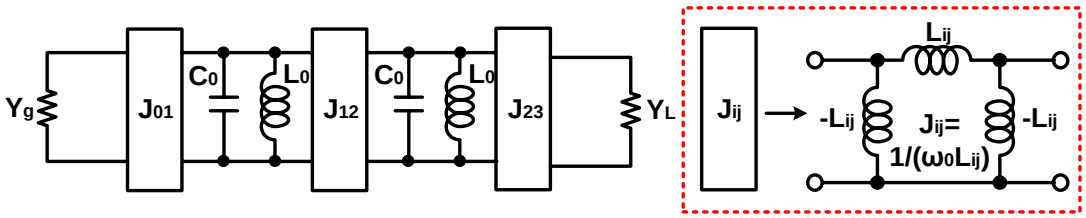


Figure 7.7. A transformed BPF using two identical resonators and inductive J-inverter.

7.2.3 L-coupled Bandpass Filter: K-band BPF Design

The K-band BPF design also starts from the synthesis of LPF like the previous V-band BPF. In the same manner of the V-band BPF, the initial LPF is synthesized based on Chebyshev 2^{nd} order 0.25-dB equi-ripple response. After completion of the synthesis of LPF, then it can be transformed to BPF with two identical resonators and J-inverters. In this case, the targeted two edge-frequencies (ω_1 and ω_2) are set to 21 and 28 GHz, respectively. Through the element values from Table 7.2 for $N = 2$ and desired bandwidth (ω_1, ω_2, and FBW=0.2887), the elements for shunt resonators and J-inverters can be obtained. Figure 7.7 exhibits the transformed BPF with two same resonators and inductive J-inverters. The capacitor of the resonators (C_0) is set to 0.5 pF for reasonable realization, the initial inductance values of the resonators can be given by

$$L_0 = \frac{1}{\omega_0^2 C_0}, \quad \omega_0 = \sqrt{\omega_1 \omega_2} \tag{7.9}$$

then 86.2 pH of inductance achieved. Next, the coefficients of J-inverters can be found with Equations (7.4) and (7.5) as well as the values of FBW, g_1 and g_2, thereby obtaining the values of $J_{12} = 0.02515$ and $J_{01} = J_{23} = 0.0199$, respectively.

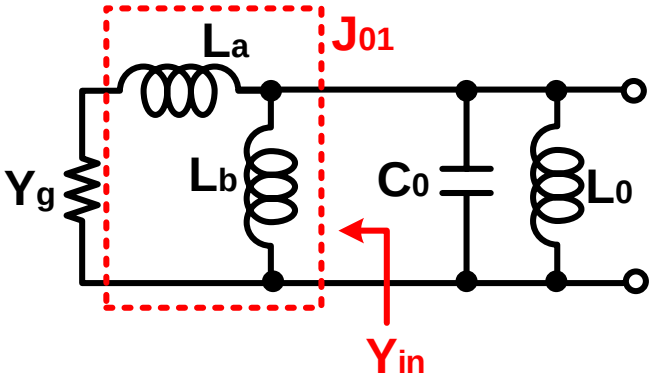


Figure 7.8. Equivalent inverter for J_{01} and J_{23}.

Thus, L_{12} is derived from J_{12} and the value of it is 261 pH. Similar to the case of using capacitive J-inverters in previously designed V-band BPF, J-inverters at the generator and load side can be designed with two inductors as illustrated at Figure 7.8. According to Figure 7.8, the admittance Y_{in} is given by

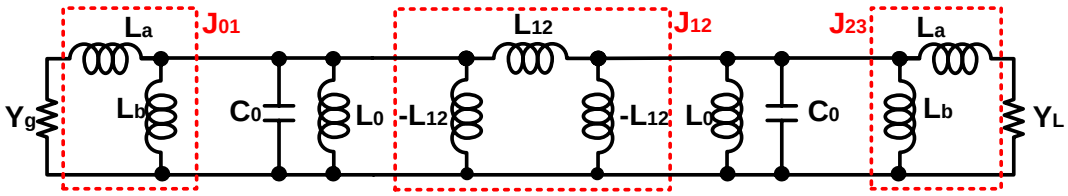
$$Y_{in} = \frac{J_{01}^2}{Y_g} = J_{01}^2 Z_0 = \frac{1}{j\omega_0 L_b} + \frac{1}{j\omega_0 L_a + Z_0} \tag{7.10}$$

and from Equation (7.10), the two inductors' value can be calculated as

$$L_a = \frac{1}{\omega_0}\sqrt{\frac{1}{J_{01}^2} - Z_0^2} \tag{7.11}$$

$$L_b = -\left(L_a + \frac{Z_0^2}{\omega_0^2 L_a}\right) \tag{7.12}$$

then $L_a = 36.1$ pH and $L_b = -3$ nH are attained. Figure 7.9(a) shows the schematic of the designed L-coupled BPF, which consists of two identical resonators and three inductive J-inverters and the final version of design is illustrated at Figure 7.9(b).



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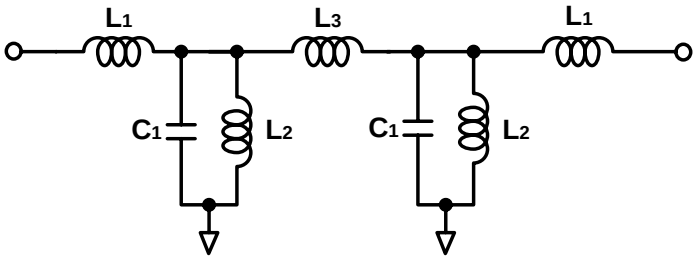

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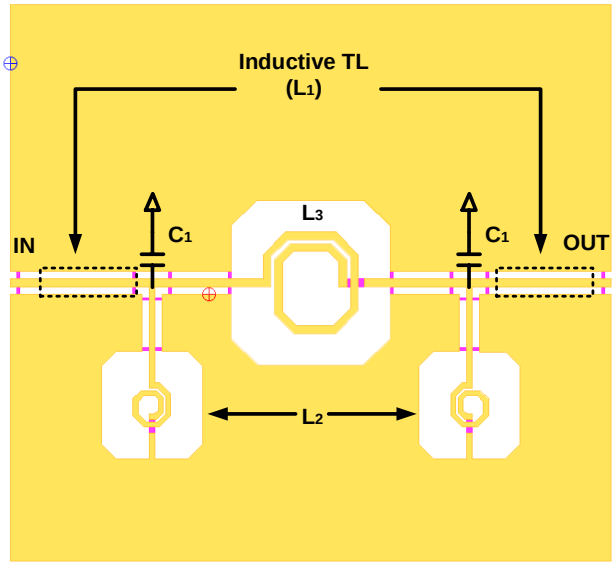


(c)

Figure 7.9. Designed L-coupled BPF: (a) schematic with J-inverters and two shunt resonators, (b) the final schematic, and (c) physical layout.

Table 7.4. Parameters of designed L-coupled BPF.

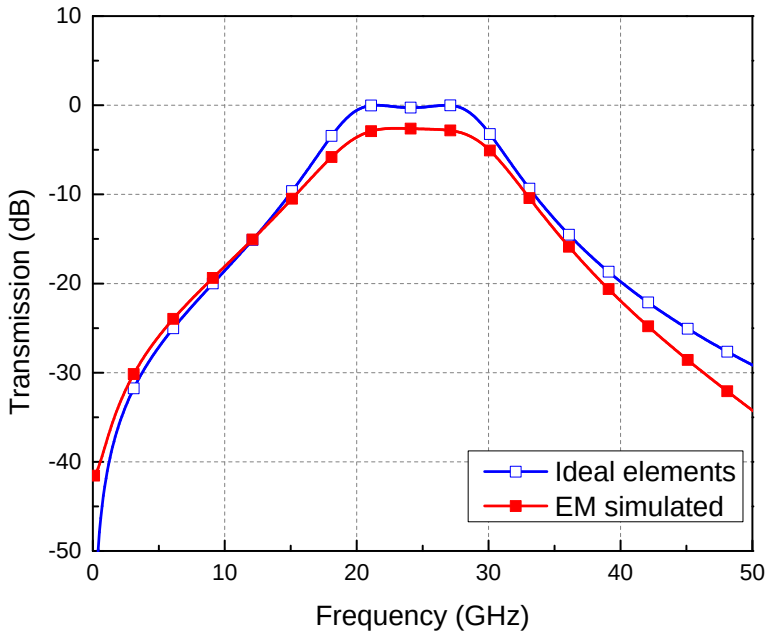
Parameters	Values
$L_1 = L_a$	36.1 pH
$L_2 = (L_b \parallel L_0 \parallel -L_{12})$	128.6 pH
$L_3 = L_{12}$	261 pH
$C_1 = C_0$	0.5 pF

Table 7.4 presents the parameters and their values of the final schematic. The inductor of the resonators (L_0) absorbs shunt and negative inductance of J-inverters (L_b and L_{12}). Figure 7.9(c) shows the physical layout of the designed K-band BPF. A MIM capacitor is employed for C_1 and spiral inductors are utilized for L_2 and L_3 realization. The inductor of L_1, however, is too small to be realized as a spiral type, thus an inductive transmission line is utilized. All spiral inductors and transmission lines for interconnection are also verified by using the EM simulator ADS Momentum [49].

The S-parameters' simulation results with ideal and EM-simulated elements are shown in Figure 7.10. As can be seen, very close results can be achieved compared to those with ideal elements except the insertion loss level between them. 2.6 dB of insertion loss is obtained for the final design due to the realistic passive components. Unlike the C-coupled BPF, the rejection property at the high frequency ranges over passband is sharper than the other side.

7.3 Design and Measurement of the proposed K/V-band Diplexer

Figure 7.11(a) exhibits the schematic of the designed diplexer consisting of two K- and V-band BPFs as well as slow-wave CPW transmission line. The slow-wave CPW transmission line plays a role in the T-matching section and it allows combination of the two independent BPFs without interference between them. This employed slow-



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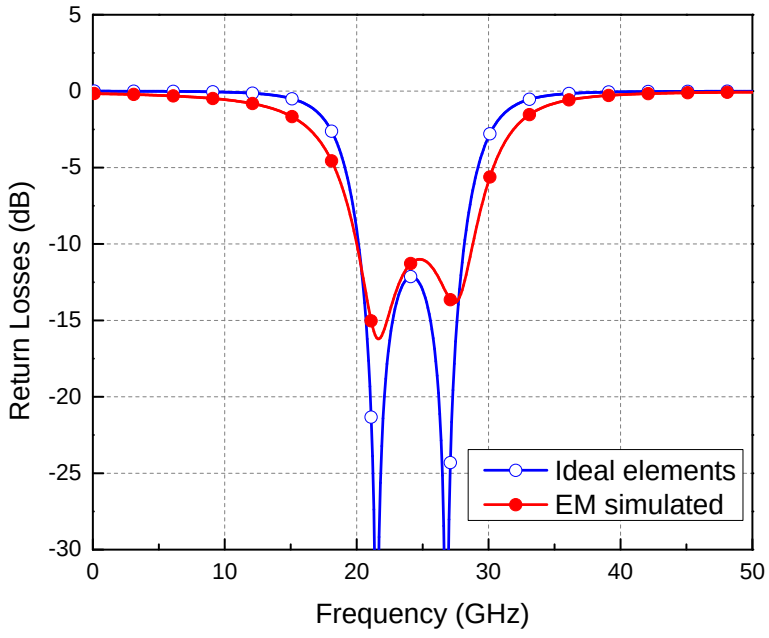
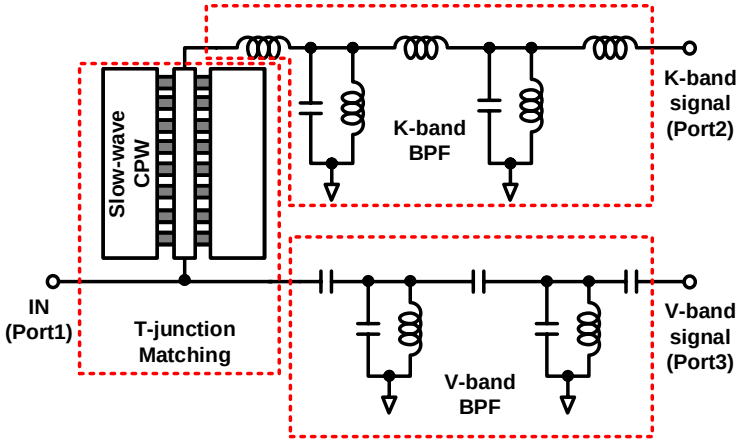


(b)

Figure 7.10. Simulation results of the designed K-band L-coupled BPF (a) transmission and, (b) return losses.



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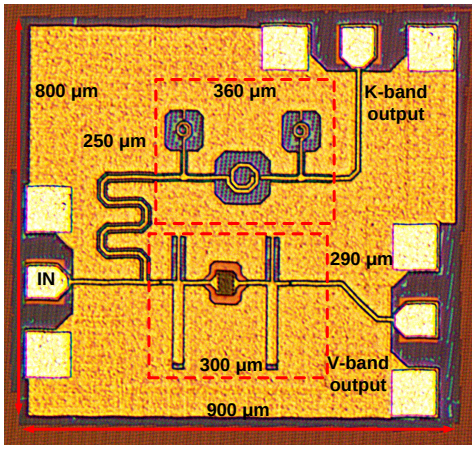


(b)

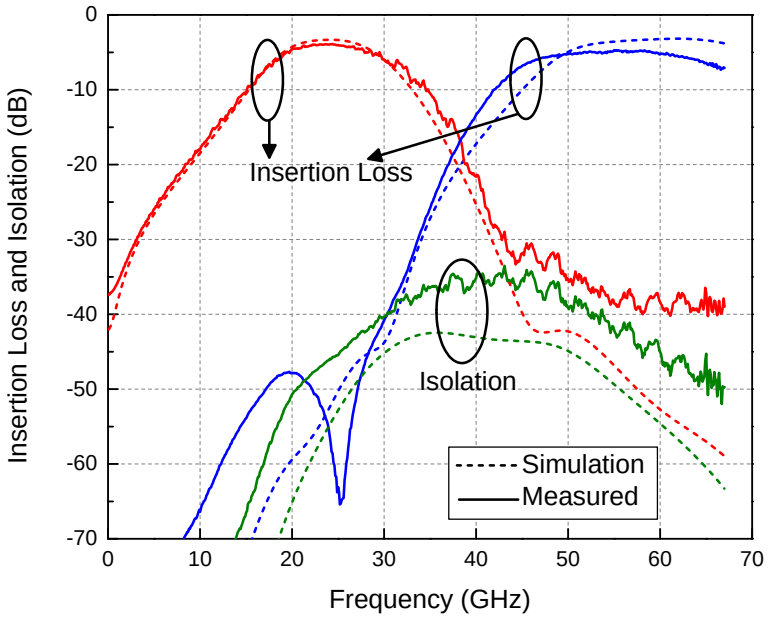
Figure 7.11. Designed K/V-band diplexer: (a) schematic, and (b) photograph of fabricated chip.

wave CPW structure introduces very high impedance for V-band signals, especially 60 GHz, thereby enabling common port matching for the two frequency bands simultaneously as well as enhancing the isolation between them. Figure 7.11(b) shows a photograph of the fabricated diplexer, which occupies 900 μm × 800 μm including three RF-probe pads. The core dimensions of the two BPFs, K- and V-band BPFs, are 360 μm × 250 μm and 300 μm × 290 μm, respectively.

Figure 7.12 shows the simulated and measured S-parameters for the diplexer. As can be seen, all measured results are very well matched to the simulation ones. Port 1 means the common port and Port 2 and Port 3 represent the K-band and V-band signal output, respectively. The measured insertion losses at 24 and 60 GHz, as shown in Figure 7.12(a), are 4.1 and 4.8 dB, respectively. Moreover, the isolation between the two frequency bands is higher than 40 dB in each band. The matching condition is also good at all three ports as shown in Figure 7.12(b).

7.4 Conclusion

In this chapter, miniaturized K/V-band diplexer designed by integrating two different BPFs with T-junction matching section has been decribed. The two BPFs are realized as capacitive and inductive coupled resonators with 2^{nd} order Chebyshev response for V- and K-band, respectively. In addition, good isolation between the two output ports can be obtained due to the asymmetric out of band rejection property of the two BPFs. The two designed BPFs are combined with the T-junction matching section, which is realized with high impedance slow-wave CPW. Good agreement between the simulated and measured results validates the design of the diplexer.



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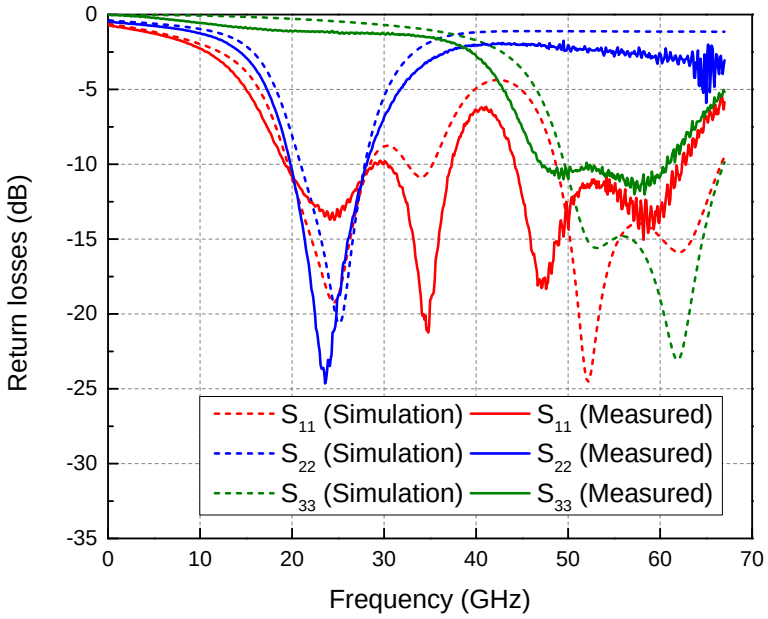


(b)

Figure 7.12. Simulated and measured results of the diplexer (a) insertion loss and isolation, and (b) return losses.

CHAPTER VIII

K- AND V-BAND VARIABLE GAIN AMPLIFIERS

In this chapter, the K- and V-band variable gain amplifiers (VGAs) designed using 0.18-μm SiGe BiCMOS technology are presented [78]. The proposed variable gain amplifiers adopt a current steering technique for gain tuning as well as employ a phase compensation capacitor at the base node of the control device for low phase variation, which is important for some applications such as phased arrays. The K-band VGA offers a maximum gain of 19 dB with 11-mA power consumption on a 2 V of V_{CC} and has a 12.6 dB gain control range. The designed V-band VGA provides 19 dB of maximum gain at 60 GHz with 13 mA on 2 V of V_{CC} and has 29.5 dB gain tuning range. Due to the current steering technique, the two amplifiers can maintain good input and output return losses with respect to all the gain states. To minimize the transmission phase variation, a phase compensation capacitor is employed at the base node of control device. As a result, the phase variations of the K- and V-band VGAs are less than 4.3° and 9° for the overall varied gain states, respectively. The core chip size of the K-band amplifier is 730 μm × 300 μm and that of V-band amplifier is 950 μm × 250 μm.

8.1 Introduction

A VGA has a wide range of applications in wireless systems such as audio level compression, synthesizers, amplitude modulation, automatic gain control loops, and attenuation/gain control [84]. For instance, it plays an indispensable role in receivers by controlling the incoming signal's power level and normalizing the average amplitude of the signal to a reference value. This allows the receiver to increase the data range without adding extra burden of linearity to the front-end systems

since adjusting the gain of the VGA can manage low power leveled input signal without additional amplifier, and this makes each component of the receiver to have more relaxed linearity specifications. Moreover, by using VGAs effectively, it can increase the system gain range. VGAs can also be employed in transmitters leading to possible gain and transmitting power level control. In this sense, VGA is one of the essential components in front-end systems and thus, various researches for designing microwave and mm-wave VGAs have been carrying out and reported in literature [84–95]. The reported VGAs adopted various gain control mechanisms such as current splitting technique [91], reflection-type attenuator [92], ladder-type attenuator [93], and current steering technique [94–96].

Using an attenuator in VGA as reported in [92] and [93] leads to high losses. Also, the current splitting technique in [91] introduces a small gain control range, poor return losses, high power consumption. On the contrary, the current steering technique provides a large gain control range with low power consumption and low complexity, thereby more suitable for designing VGAs operated in microwave and mm-wave regions. Many functions such as linearity, power consumption, matching, and gain control capability should be taken into account for VGA design. Additionally, the phase variation though a VGA should be also considered since the output signal's phase is different with respect to adjusted gain control of VGA. This is due to the fact that VGAs are one kind of amplifiers and inherent active devices characteristics produce phase variation for different gains. In a system, which has a phase shifter, the phase variations generated by the VGA can be corrected but the phase shifter does not provide constant gain or insertion loss versus phase. Therefore, it is important that phase variations for all controlled gain states should be minimized for a VGA design. Several techniques for low phase variation in VGAs are reported at [84–86, 95].

In this chapter, two VGAs, operating at K- and V-band, are presented with decent gain control range and low phase variation. These VGAs adopt the current steering technique for gain tuning function and employ a capacitor at the gain control device for phase compensation. The design of these VGAs is explained in details.

8.2 Analysis of Current Steering Technique and Phase Compensation Capacitor

The purpose of this section is to calculate the transfer function and associated phase variation in the current steering circuit realized with bipolar devices. Firstly, it addresses the gain tuning mechanism of the current steering circuit. In a second step, the phase compensation capacitor of the current steering topology is analyzed.

8.2.1 Current Steering Technique

Figure 8.1 exhibits the current steering gain cell for the VGA, which consists of three BJTs. The transistors, Q_1 and Q_2 are connected as a cascode device and Q_3 is used for gain control. The base's bias voltages for Q_1 and Q_2 are fixed as V_{BE1} and V_{B2}, respectively. The analysis of this circuit realized by CMOS is given in [96]. To explain the variable gain operation, the relationship between two collector currents of Q_1 and Q_2 (i_1 and i_2) should be obtained first. The collector current of Q_1 (i_1) is a summation of the emitter currents of the upper two devices (Q_2 and Q_3) and can be represented as

$$i_1 = i_2 + i_3 \tag{8.1}$$

i_1 is also the collector current of Q_1 and hence can be expressed as

$$i_1 = I_{S1} \cdot \exp\left(\frac{V_{BE1}}{V_T}\right) = I_{S1} \cdot \exp\left(\frac{V_{B1} + v_{in}}{V_T}\right) = I_1 \cdot \exp\left(\frac{v_{in}}{V_T}\right) \tag{8.2}$$

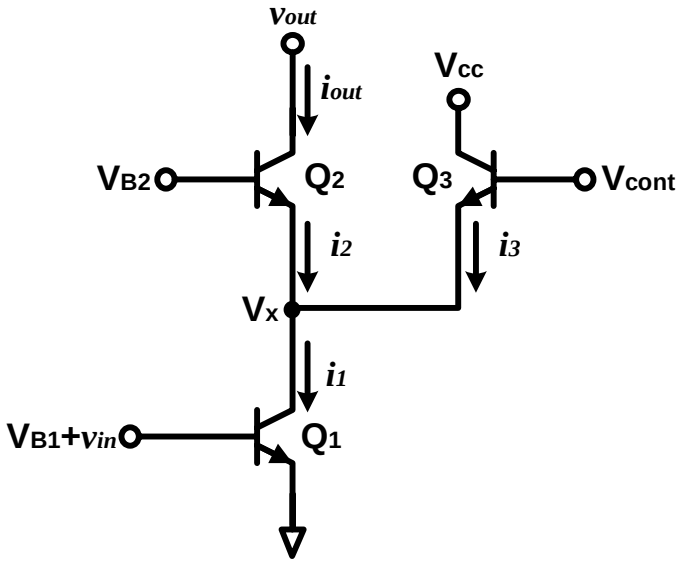


Figure 8.1. Current steering gain cell of the variable gain amplifier.

$$I_1 = I_{S1} \cdot \exp\left(\frac{V_{B1}}{V_T}\right) \tag{8.3}$$

where I_{S1}, I_1, and V_T are the saturation current of Q_1, DC bias current, and thermal voltage, respectively. Also, the emitter currents of Q_2 and Q_3, i_2 and i_3, are given by

$$\begin{aligned} i_2 &= \frac{I_{S2}}{\alpha_2} \cdot \exp\left(\frac{V_{B2} - V_x}{V_T}\right) \\ i_3 &= \frac{I_{S3}}{\alpha_3} \cdot \exp\left(\frac{V_{cont} - V_x}{V_T}\right) \end{aligned} \tag{8.4}$$

where I_{S2} and I_{S3}, α_2 and α_3 are the saturation currents and common base current gains of the devices, respectively. The voltage at the common node, V_x, is the combination of the DC and ac voltage, hence can be represented as $V_x = V_{C1} + v_{C1}$.

Therefore, i_2 and i_3 can be expressed as following equation.

$$\begin{aligned} i_2 &= \frac{I_{S2}}{\alpha_2} \cdot \exp\left(\frac{V_{B2} - V_{C1}}{V_T}\right) \cdot \exp\left(\frac{-v_{C1}}{V_T}\right) \\ i_3 &= \frac{I_{S3}}{\alpha_3} \cdot \exp\left(\frac{V_{cont} - V_{C1}}{V_T}\right) \cdot \exp\left(\frac{-v_{C1}}{V_T}\right) \end{aligned} \tag{8.5}$$

Assuming the voltage difference between the base bias of Q_2 and control voltage of Q_3 is $V_D = V_{B2} - V_{cont}$, then i_2 is simplified as

$$\begin{aligned} i_2 &= \frac{I_{S2}}{\alpha_2} \cdot \exp\left(\frac{V_D}{V_T}\right) \cdot \exp\left(\frac{V_{cont} - V_{C1}}{V_T}\right) \cdot \exp\left(\frac{-v_{C1}}{V_T}\right) \\ &= \frac{I_{S2}}{I_{S3}}\frac{\alpha_3}{\alpha_2} \cdot i_3 \cdot \exp\left(\frac{V_D}{V_T}\right) = K \cdot i_3 \cdot \exp\left(\frac{V_D}{V_T}\right) \end{aligned} \tag{8.6}$$

where $K = (I_{S2}\alpha_3)/(I_{S3}\alpha_2)$ and it is a constant value. By using Equations (8.1) and (8.6), the current of i_2 with respect to i_1 can be obtained as

$$\begin{aligned} i_2 &= \frac{K \cdot \exp\left(\frac{V_D}{V_T}\right)}{1 + K \cdot \exp\left(\frac{V_D}{V_T}\right)} \cdot i_1 \\ &= \frac{K \cdot \exp\left(\frac{V_D}{V_T}\right)}{1 + K \cdot \exp\left(\frac{V_D}{V_T}\right)} \cdot I_1 \cdot \exp\left(\frac{v_{in}}{V_T}\right) \end{aligned} \tag{8.7}$$

The overall transconductance (G_m) can now be computed with the above current equations. The overall transconductance is defined as

$$G_m = \frac{\partial i_{out}}{\partial v_{in}} \tag{8.8}$$

where v_{in} and i_{out} are the input ac voltage and output ac current of the current steering gain cell. If the common emitter current gain (β) is large enough, then $\alpha \simeq 1$ and it allows the output current, $i_{out} = \alpha_2 i_2 \simeq i_2$. In this sense, the overall

transconductance can be expressed by

$$G_m = \frac{\partial i_{out}}{\partial v_{in}} \simeq \frac{\partial i_2}{\partial v_{in}} = \frac{K \cdot \exp\left(\frac{V_D}{V_T}\right)}{1 + K \cdot \exp\left(\frac{V_D}{V_T}\right)} \cdot I_1 \cdot \exp\left(\frac{v_{in}}{V_T}\right) \frac{1}{V_T} \tag{8.9}$$

where

$$\frac{\partial i_1}{\partial v_{in}} = I_1 \cdot \exp\left(\frac{v_{in}}{V_T}\right) \frac{1}{V_T} = g_{m1} \tag{8.10}$$

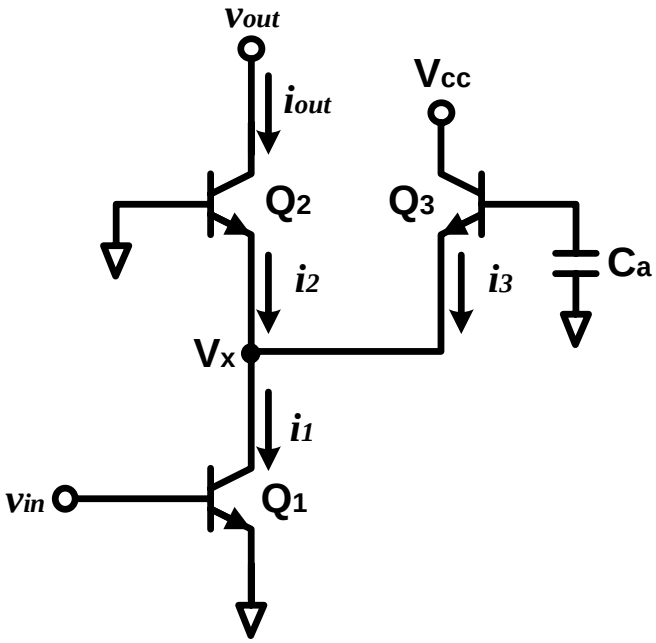
and g_{m1} is the transconductance of the common emitter device (Q_1). Therefore, G_m can be determined as

$$G_m = \frac{K \cdot \exp\left(\frac{V_D}{V_T}\right)}{1 + K \cdot \exp\left(\frac{V_D}{V_T}\right)} \cdot g_{m1} \tag{8.11}$$

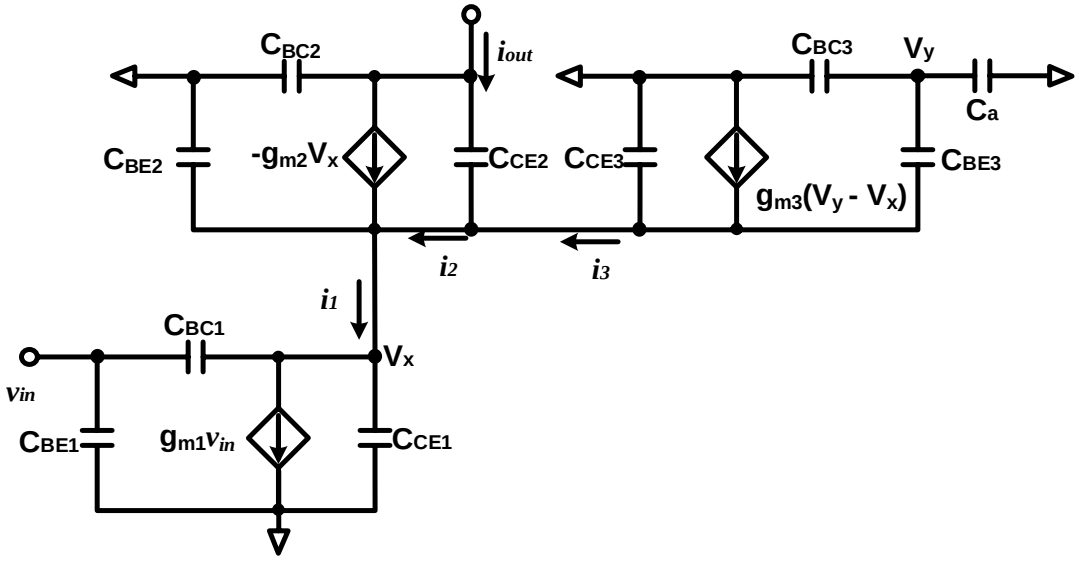
According to Equations (8.7) and (8.11), the gain control mechanism can be explained. Firstly, the output current (i_{out}) is controlled by the base control voltage of Q_3 (V_{cont}) as shown in equation (8.7). Secondly, the overall transconductance (G_m) is varied by adjusting i_{out}. For maximum gain, the control voltage of V_{cont} is set low enough to fully turn off transistor Q_3, and the total current of Q_1 flows through Q_2 ($i_1 = i_2$). If V_{cont} is increased then V_D is reduced, and it makes the current flowing through Q_2 decreases accordingly and thus overall G_m reduces ultimately. It is noted that the common emitter device (Q_1) does not affect the bias condition and its own transconductance with respect to gain control. In this sense, the input impedance does not change much while the gain is varied, thereby achieving very good return losses.

8.2.2 Phase Compensation Capacitor

As mentioned earlier, the output phase of the VGA can be changed with controlled gain status and this can cause a significant error for phase sensitive systems such as phased-arrays. Several techniques for minimizing phase variation with var-



(a)



(b)

Figure 8.2. The current steering gain cell with phase compensation capacitor (C_a) (a) schematic, and (b) simplified small-signal model.

ious gain status have been reported in the literature [84–86, 95]. One of them is to utilize a small phase compensation capacitor placed at the gate of a NMOS control device of the current steering topology and its phase analysis is reported in [95]. Figure 8.2(a) shows the schematic of this technique adopted on a BJT-based current steering gain cell and the capacitor (C_a) is connected at the base of gain control device (Q_3). In order to evaluate the phase variation property of this circuit, the simplified small-signal model is utilized as shown in Figure 8.2(b). Firstly, the relationship between V_y and V_x can be obtained at Q_3 and it can be expressed as following.

$$V_y = \frac{C_{BE3}}{C_a + C_{BE3} + C_{BC3}} V_x \tag{8.12}$$

Then, the total current of Q_3 (i_3) can be derived as

$$\begin{aligned} i_3 &= -sC_{CE3}V_x + g_{m3}(V_y - V_x) + sC_{BE3}(V_y - V_x) \\ &= -\left[\left(1 - \frac{C_{BE3}}{\alpha}\right) g_{m3} + s\left(C_{BE3} + C_{CE3} - \frac{C_{BE3}^2}{\alpha}\right)\right] V_x \end{aligned} \tag{8.13}$$

where $\alpha = C_a + C_{BE3} + C_{BC3}$. Moreover, the current i_1 of Q_1 and i_2 of Q_2 as well as i_{out} can be expressed in the following equations:

$$i_1 = -s[C_{BC1} + C_{CE1}]V_x + [g_{m1} - sC_{BC1}]v_{in} \tag{8.14}$$

$$i_2 = -\left(g_{m2} + s\left(C_{CE2} + C_{BE2}\right)\right) V_x \tag{8.15}$$

$$i_{out} = -(g_{m2} + sC_{CE2})V_x \tag{8.16}$$

Using Equations (8.12)-(8.16), the overall transconductance of the current steering gain cell can be derived as

$$\frac{i_{out}}{v_{in}} = \frac{(g_{m1} - sC_{BC1})(g_{m2} + sC_{CE2})}{(g_{m2} + \beta g_{m3}) + s(C_{BC1} + C_{CE1} + C_{BE2} + C_{CE2} + C_{CE3} + \beta C_{BE3})} \tag{8.17}$$

where

$$\beta = \frac{C_a + C_{BC3}}{C_a + C_{BE3} + C_{BC3}} \tag{8.18}$$

The phase of this transfer function is given by

$$\angle \left(\frac{i_{out}}{v_{in}} \right) = \phi_1 + \phi_2 + \phi_3 \tag{8.19}$$

where

$$\phi_1 = -tan^{-1}(\omega C_{BC1}/g_{m1}) \tag{8.20}$$

$$\phi_2 = tan^{-1}(\omega C_{CE2}/g_{m2}) \tag{8.21}$$

$$\phi_3 = tan^{-1}\left(\omega \frac{C_{BC1} + C_{CE1} + C_{BE2} + C_{CE2} + C_{CE3} + \beta C_{BE3}}{g_{m2} + \beta g_{m3}} \right) \tag{8.22}$$

Since the current steering technique provides the common emitter device (Q_1) with constant bias condition while the gain function is varied, ϕ_1 is also constant, which is comprised of C_{BC1} and g_{m1}. As a result, the phase variation is dependent on the combination of ϕ_2 and ϕ_3. By adding a phase compensation capacitor (C_a) at the base terminal of control device (Q_3), it helps decrease ϕ_3 leading to reduce the phase of combination of ϕ_2 and ϕ_3 ultimately. A proper value of C_a can be chosen by sweeping the control voltages of Q_3, then the total phase variation of the current steering variable gain cell can be minimized.

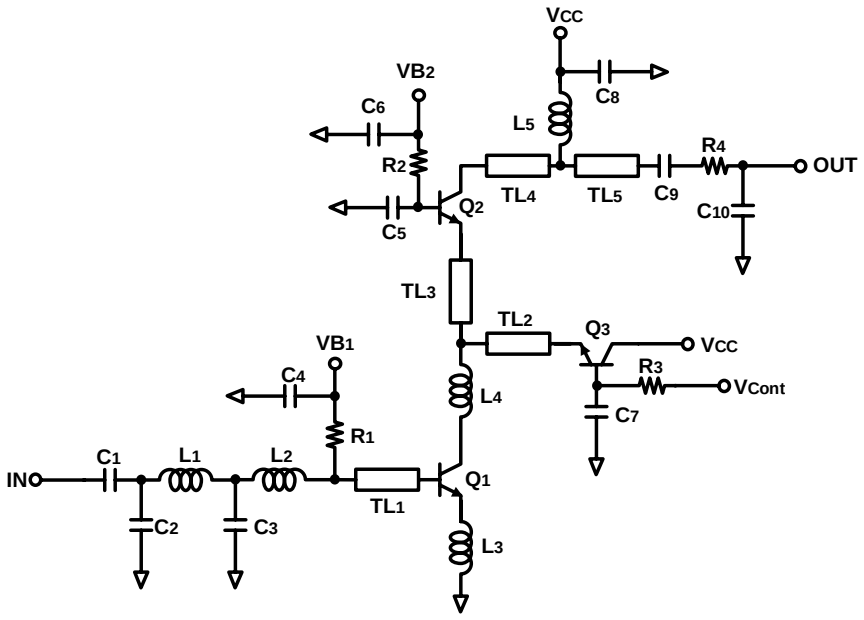


Figure 8.3. Schematic of the designed K-band VGA.

8.3 Design of K- and V-band VGAs

8.3.1 One-stage K-band VGA

Figure 8.3 shows the schematic of the designed one-stage K-band VGA and the values of all constituents are shown in Table 8.1. The cascode topology is adopted for high gain and isolation between input and output. For the gain control, the current steering technique is adopted to achieve good input and output return losses while gain is controlled by different control voltages. In this sense, the bias condition of the common emitter and common base devices are constant. This VGA produces high gain with low DC power consumption, which is 11 mA of collector current under 2 V of collector voltage of the common base part of the cascode (V_{CC}). The device size is determined based on the trade-off between maximum gain, gain control range, and power consumption. To enhance the linearity as well as to facilitate broadband

Table 8.1. Values of the elements used for the K-band VGA.

Components	Values	Components	Values	Components	Values
Q_1, Q_2, Q_3 ($E_W \times M$)	$5\mu m \times 1$	R_1-R_3	1.26 KΩ	C_7	30 fF
		R_4	15 Ω	C_9	220 fF
TL_1	30 μm	C_1	700 fF	C_{10}	134 fF
TL_2	60 μm	C_2	274.3 fF	L_1	186 pH
TL_3	45 μm	C_3	659 fF	L_2	257 pH
TL_4	55 μm	C_4, C_5	2 pF	L_3	20 pH
TL_5	55 μm	C_6, C_8	6 pF	L_4	50 pH
				L_5	280 pH

E_W: Emitter width, M: multiplier, TL width: 5 μm, gap: 10 μm

input matching, a degeneration inductor (L_3), implemented with inductive transmission line (TL), is connected at the emitter of common emitter device (Q_1). Due to gain decreasing with degeneration, an inductor (L_4) and inductive TL (TL_3) are inserted between the common emitter (Q_1) and common base (Q_2) devices of the cascode device. Regarding the input matching, two sections of LC ladder structure are employed resulting in broadband matching. In addition, CPW structure is utilized for realizing all the transmission lines for feeding and interconnection. For transmission phase compensation, the capacitor (C_7) is connected to the base node of the control device (Q_3) of the current steering cell and its value is chosen as 30 fF. This capacitor is realized by using a metal capacitor since its value is too small to be realized with a MIM capacitor provided by the process technology. Figure 8.4 shows the layout of the K-band VGA and it occupies 950 μm × 800 μm with two RF-probes and a six-pins DC-probe pads while the circuit core has 730 μm × 300 μm of die size.

Figure 8.5 exhibits the simulated S-parameters of designed K-band VGA. The maximum small-signal gain is 19.5 dB at 26 GHz and the 3-dB bandwidth is from

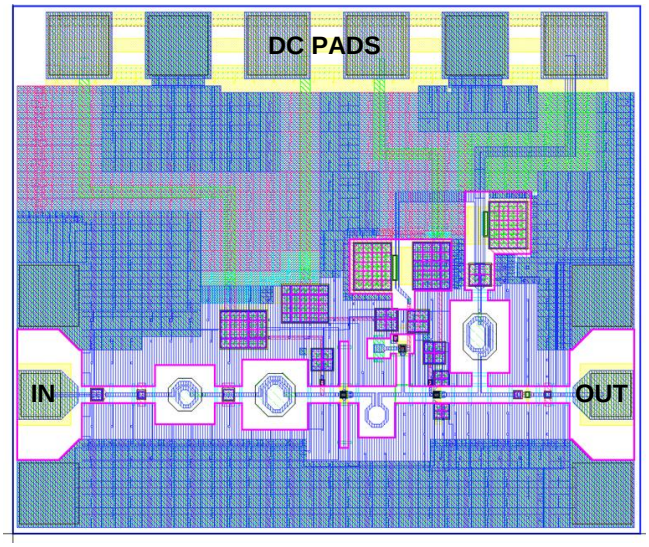


Figure 8.4. Layout of the designed K-band VGA.

21.4 to 31.2 GHz as depicted in Figure 8.5(a). In this case, the designed VGA is set as maximum gain status and it consumes 22 mW of DC power. Especially at 24 GHz, 19 dB of the maximum gain is achieved. The simulated small-signal gain of the VGA with different gain stage is shown in Figure 8.5(b). As can be seen, the VGA has a gain control between 6.9 and 19.5 dB by adjusting the control voltage (V_{cont}), thereby achieving a 12.6 dB gain control range. Figures 8.5(c) and 8.5(d) show the input and output return losses with respect to different gain states. As expected, the input and output return losses are larger than 10 dB for all gain states in the interested frequency band. In addition, the output return losses at each gain stage are almost constant because output load impedance rarely changes due to the constant bias points at the common base transistor of cascode structure (Q_2). Figure 8.6 shows the insertion phase variation of the VGA relative to the maximum gain state, which corresponds to 0° in the figure. The maximum phase variation for all gain states is less than 8° between 20 and 30 GHz. Specifically at 24 GHz, the

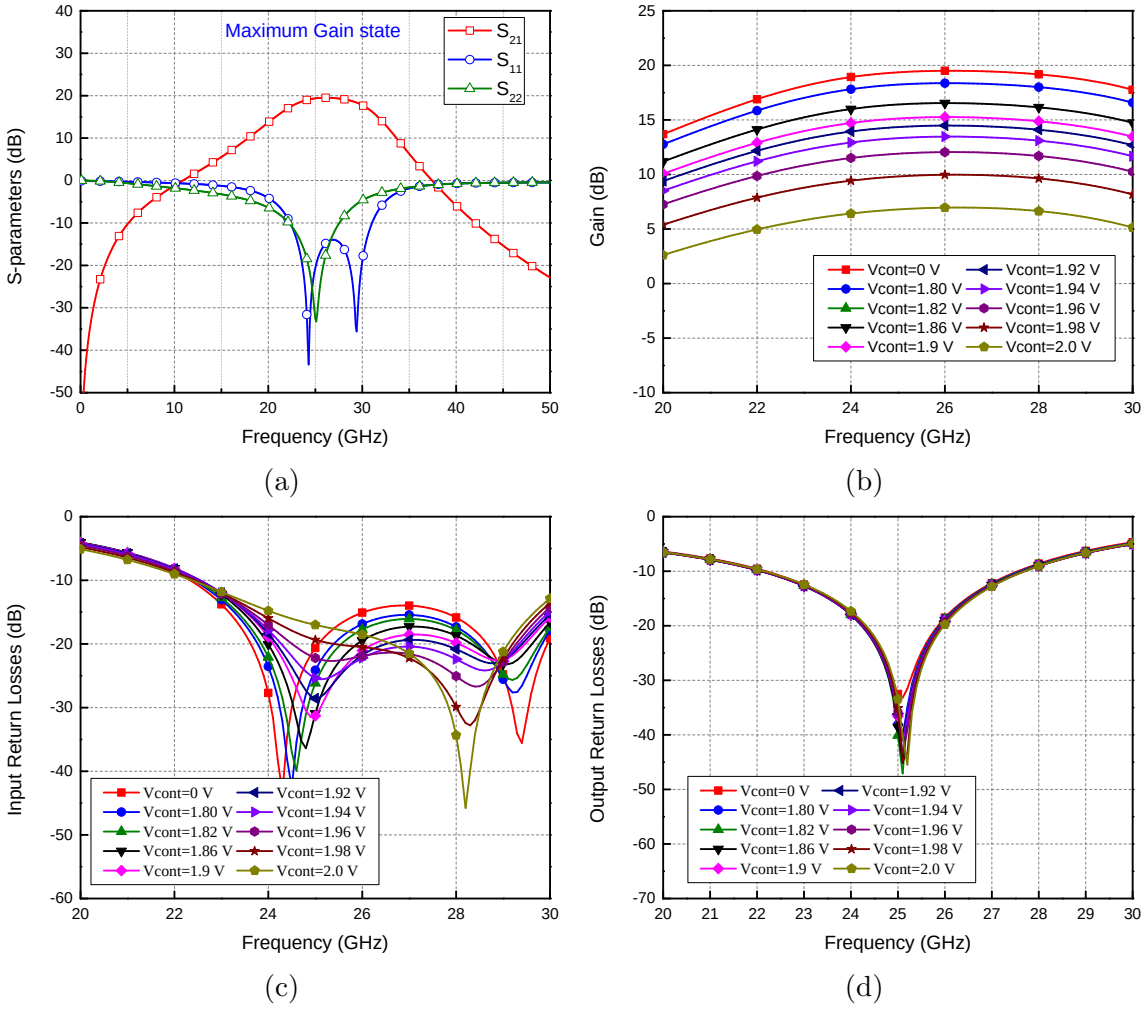


Figure 8.5. Simulation results of the designed K-band VGA: (a) S-parameters for maximum gain, (b) gain control, (c) input return losses, and (d) output return losses.

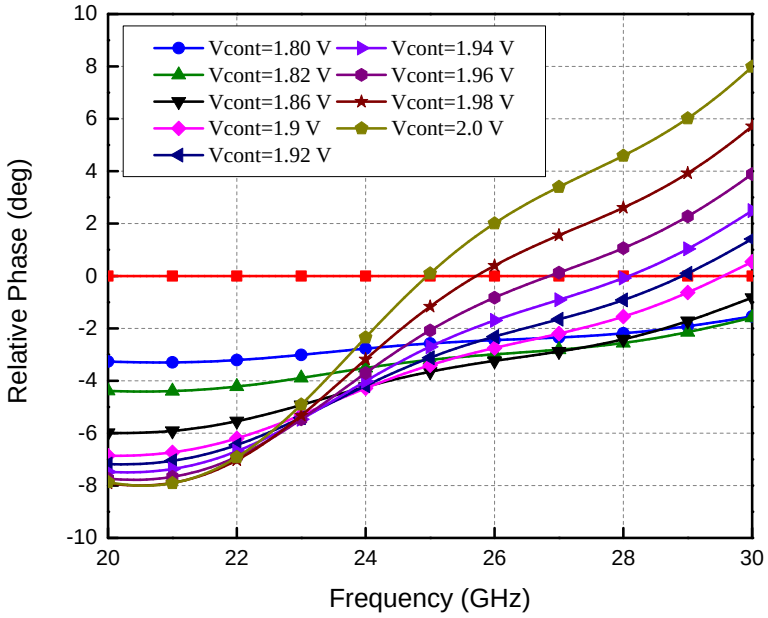


Figure 8.6. Relative phase variation of the design VGA between 20 and 30 GHz.

achieved phase variation is less than 4.3° for all different gains.

8.3.2 V-band Two-stage VGA

In this section, a another designed VGA working in V-band is explained. Figure 8.7 illustrates the schematic of the designed V-band VGA. The topology and employed techniques, except the number of stages are the same as the previous design methodology for the K-band VGA and the values of the components are shown in Table 8.2. Due to degradation of the gain performance of the devices at higher frequencies, two-stage amplifier structure has been chosen to produce high gain. All transmission lines (TLs) shown in the schematic are designed by CPW structure, which is realized on the top thickest metal layer. For the input matching network, a π-network is utilized, which is comprised of capacitors and inductive TLs. In addition, the degeneration inductors, L_1 and L_4, provides the negative feedback leading to increased real impedance at the base node of common emitter devices (Q_1 and

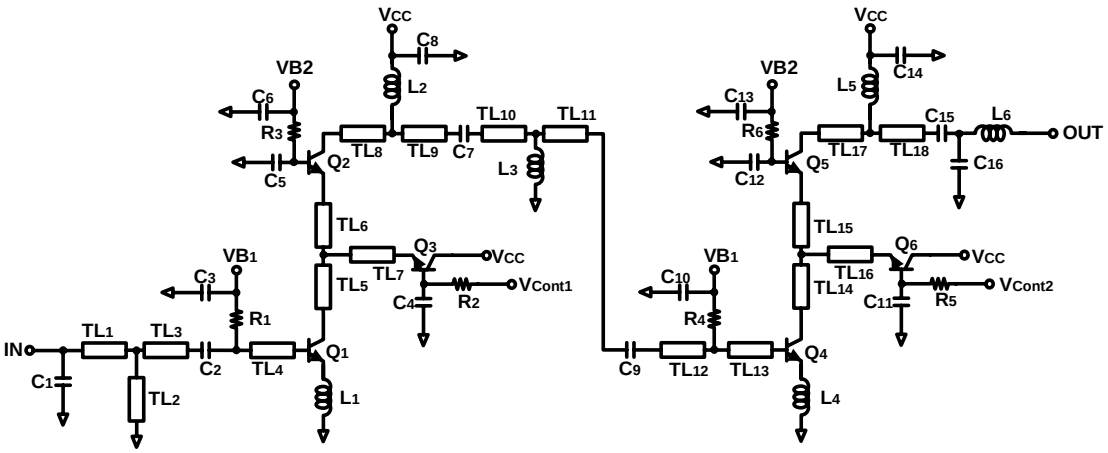


Figure 8.7. Schematic of the designed two-stage V-band VGA.

Table 8.2. The values of the elements of the V-band VGA.

Devices and lumped elements' values

Q_1-Q_6 ($E_W \times$ M)	5 $\mu m \times 1$	C_4, C_{11}	30 fF	R_1-R_6	1.26 KΩ
		C_5, C_{12}	1 pF	L_1, L_4	15 pH
C_1	75 fF	C_7	83 fF	L_2	80 pH
C_2	209 fF	C_9	55 fF	L_3	50 pH
C_3, C_6, C_8	2 pF	C15	40 fF	L_5	80 pH
C_{10}, C_{13}, C_{14}		C_{16}	30 fF	L_6	150 pH

E_W: Emitter width, M: multiplier

Lengths of the transmission lines

TL_1	TL_2	TL_3	TL_4	TL_5	TL_6	TL_7*	TL_8	TL_9
75 μm	90 μm	45 μm	55 μm	45 μm	45 μm	60 μm	55 μm	45 μm
TL_{10}	TL_{11}	TL_{12}	TL_{13}	TL_{14}	TL_{15}	TL_{16}*	TL_{17}	TL_{18}
25 μm	25 μm	23 μm	23 μm	45 μm	45 μm	60 μm	55 μm	28 μm

width: 5 μm, gap: 10 μm (For TL_7* and TL_{16}*, width: 7.5 μm)

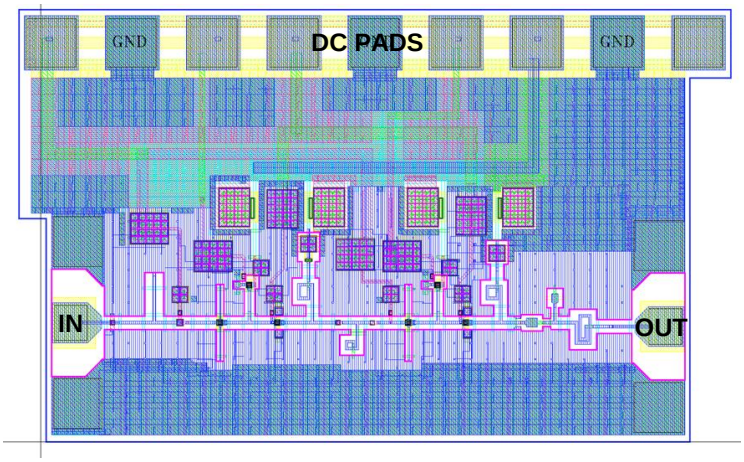
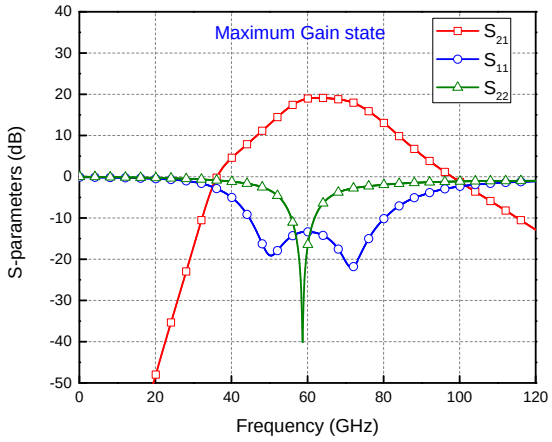


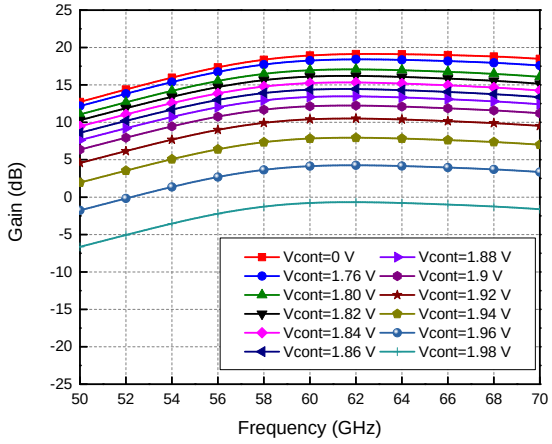
Figure 8.8. Layout of the designed V-band VGA.

Q_4), which helps making wideband input matching possible. To enhance the degraded gain due to L_1 and L_4, inductive TLs are employed at the internal of the cascode devices as inductive peaking method. The input/output matching circuit is designed as conjugate matching circuit for high gain as well as for minimum return loss larger than 10 dB while gain is varied with different control voltage (V_{cont}). Inter-stage matching network is also implemented as conjugating matching between the two stages.

For the gain control, the current steering technique is also adopted for the 1^{st}- and 2^{nd}-stage of the VGA. Thus, the bias condition of the cascode devices of both amplifier stages are fixed, and the DC power consumption is low, which is total 13 mA of current under 2 V of collector voltage (V_{CC}). Since each stage has gain control device, there is more degree of freedom to tune the gain. For instance, various gains can be introduced by using only one of the control devices or both devices. The latter technique can provide more fine tuning as well as large gain control range. To minimize the phase variation for all gain states, phase compensation capacitors (C_4



(a)



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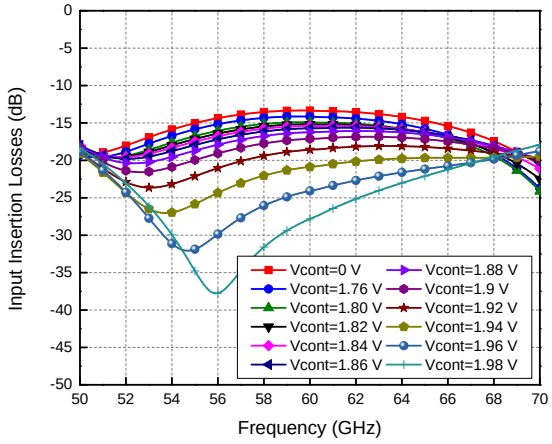
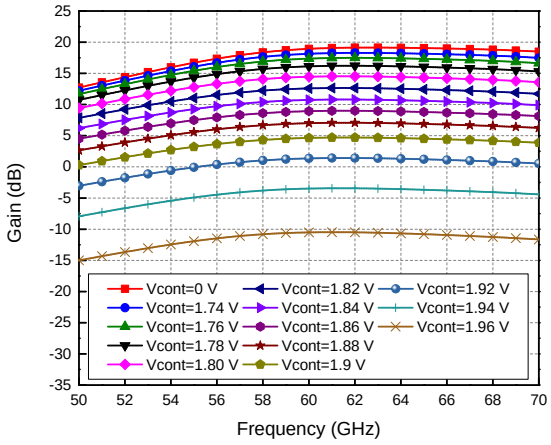
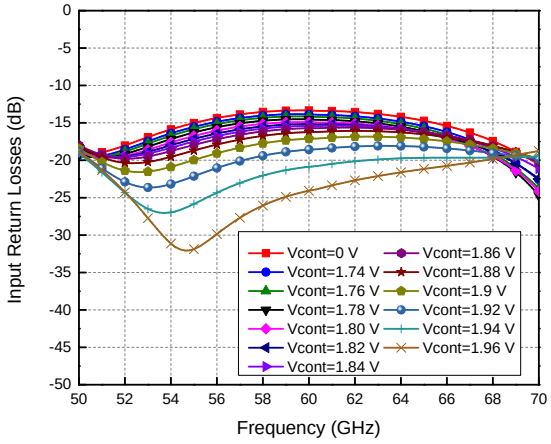


(c)

Figure 8.9. Simulation results of the designed V-band VGA for 1-stage gain tuning: (a) S-parameters for maximum gain, (b) gain control, (c) input return losses, and (d) output return losses.



(a)



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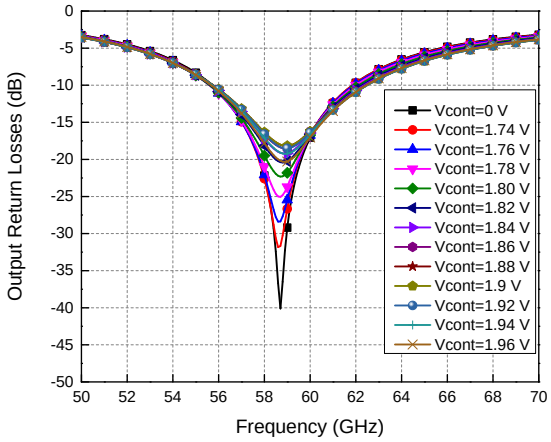
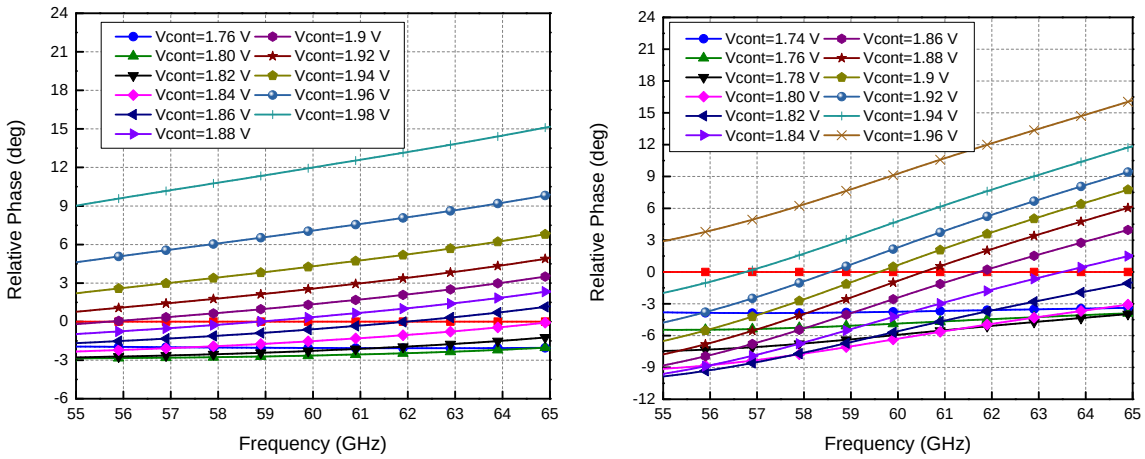


(c)

Figure 8.10. Simulation results of designed V-band VGA for 2-stage gain tuning: (a) S-parameters for maximum gain, (b) gain control, (c) input return losses, and (d) output return losses.



(a) (b)

Figure 8.11. Relative phase variation of the designed VGA between 55 and 65 GHz.

and C_{11}) are shunt connected at the base of control devices (Q_3 and Q_6) as explained in the previous section 8.2.2. Figure 8.8 shows the layout of V-band 2-stage VGA and it occupies 1300 μm × 800 μm with two RF-probes and one 8-pins DC-probe pads while the circuit core has 950 μm × 250 μm of die size.

Figure 8.9(a) shows the simulated S-parameters of the designed V-band VGA with 19 dB maximum gain at 60 GHz and 54.1-75.9 GHz of 3-dB bandwidth. Figure 8.9(b) exhibits the gain control with different control voltage at the 1^{st} stage only. As can be seen, the VGA has a gain control between -1 and 19 dB by adjusting the control voltage (V_{cont}) thereby achieving 20 dB gain control range. The input return losses corresponding to the various gain states are shown in Figure 8.9(c) and still remain larger than 10 dB for overall gain states as expected. The output return losses in this case do not change since the second stage amplifier is fixed without control. Figure 8.10 illustrates the gain tuning characteristic and input/output return losses with respect to different gain control voltages for both stages. It is noted that the control voltage for both stages are the same that is $V_{cont1} = V_{cont2} = V_{cont}$. As can

be seen in Figure 8.10(a), the gain control range is larger than the previous one, which is 29.5 dB from -10.5 to 19 dB. Furthermore, in this situation, the input and output return losses change depending on the changed gain states as depicted in Figures 8.10(b) and 8.10(c), and they are larger than 10 dB under all gain states. Figures 8.11(a) and 8.11(b) show the insertion phase variation of the VGA relative to the maximum gain state for gain control of the 1^{st} stage only and both stages, respectively. The insertion phase at the maximum gain state is set to 0° in the figures. As can be seen, the maximum phase variation for all gain states is less than 12° at 60 GHz when only the 1^{st} stage is tuned whereas, the maximum phase variation is less than 9° at 60 GHz when the control voltages are injected to both stages.

8.4 Conclusion

In this chapter, K- and V-band VGAs designed using 0.18-μm SiGe BiCMOS technology are presented. The proposed VGAs adopt the current steering technique as the gain control mechanism as well as employ a phase compensation capacitor at the base node of the control device for low phase variation with varied gain states. By utilizing the current steering technique, the designed VGAs provide wide gain tuning range with good input and output return losses for all gain states. As a result, variable gain amplifiers with low phase variation as well as decent tuning range and power consumption working on K- and V-band are achieved.

CHAPTER IX

A K/V DUAL-BAND TRANSMITTER FRONT-END DESIGN

Integration of a millimeter-wave multi-mode multi-band transmitter on a single chip enables a low-cost millimeter-wave system for next-generation communication and sensing systems. This chapter presents a K/V dual-band transmitter front-end designed using 0.18-μm SiGe BiCMOS technology [78]. The designed transmitter includes two diplexers located at the input and output, a K-band variable gain amplifier (VGA), a V-band VGA, a K-band power amplifier (PA) and a V-band PA. The transmitter achieves 52.3 and 36.8 dB of maximum gain at 24 and 60 GHz, respectively. Also, the gain control range at 24 and 60 GHz are 12.4 and 29.6 dB between 39.9-52.3 and 7.2-36.8 dB, respectively. The chip size is 3.5 $\times$ 2.5 mm^2 including two GSG RF probes and two multi-contact DC probe pads.

9.1 Transmitter Architecture and Operation

The block diagram of the proposed K/V dual-band transmitter front-end module is shown in Figure 9.1, which consists of two diplexers, K-band VGA, V-band VGA, K-band PA, and V-band PA. These constituents have been described in Chapters III, IV, VII, and VIII. The diplexer reported in Chapter VII has 4.1 and 4.8 dB measured insertion losses at 24 and 60 GHz, respectively, with good input/output return losses and isolation higher than 40 dB between two output ports. The two VGAs, 1-stage K-band VGA and 2-stage V-band VGA are presented in Chapter VIII. They are based on the current steering topology with phase compensation capacitor for low transmission phase variation and provide 19 dB of maximum gain at 24 and 60 GHz as well as 12.6 and 29.5 dB gain tuning range at 24 and 60 GHz, respectively. The K-band PA, however, needs to be re-designed for the proposed transmitter

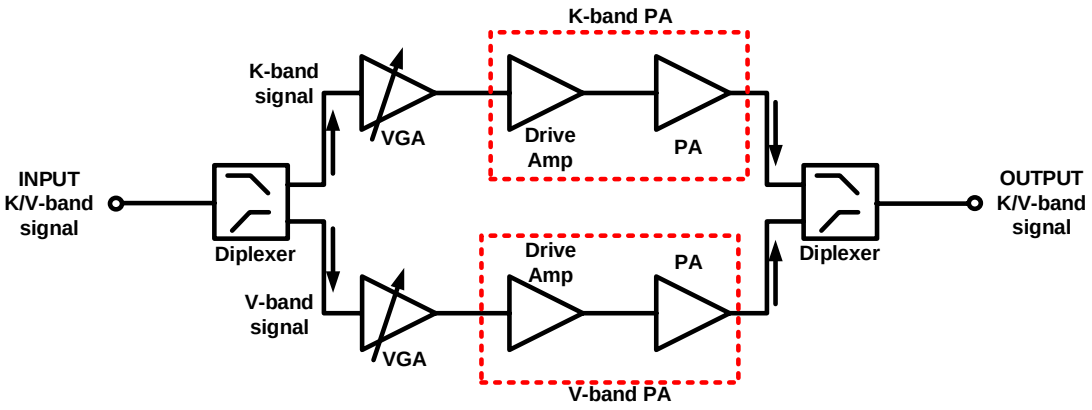


Figure 9.1. Block diagram of the K/V dual-band transmitter front-end.

since the K-band PA described in Chapter III was designed and fabricated with a different process technology. Although the process for fabrication is different, the topology of the re-designed PA is exactly same as the PA in Chapter III, which implements two identical main power amplifiers combined in parallel using lumped-element based Wilkinson power divider and combiner with and one driver amplifier connected in front of them. It has 36.2 dB of measured gain and 17 dBm of the measured maximum output power with 18.7 % PAE at 24 GHz. Lastly, the V-band PA described in Chapter IV produces 19 dB of the measured gain and 18.8 dBm of measured maximum output power.

The designed transmitter supports dual-band and dual-mode operation, which is either individual single-band mode or concurrent dual-band mode. For the single-band mode, an input signal can be either K-band signal or V-band signal. The input signal can go through the input diplexer and is amplified by the VGA and PA working on its band, and the output signal of the PA is delivered to the output diplexer while the VGA and PA on another path are set in off-state. For the concurrent dual-band mode, both K- and V-band signals are injected into the transmitter as concurrent

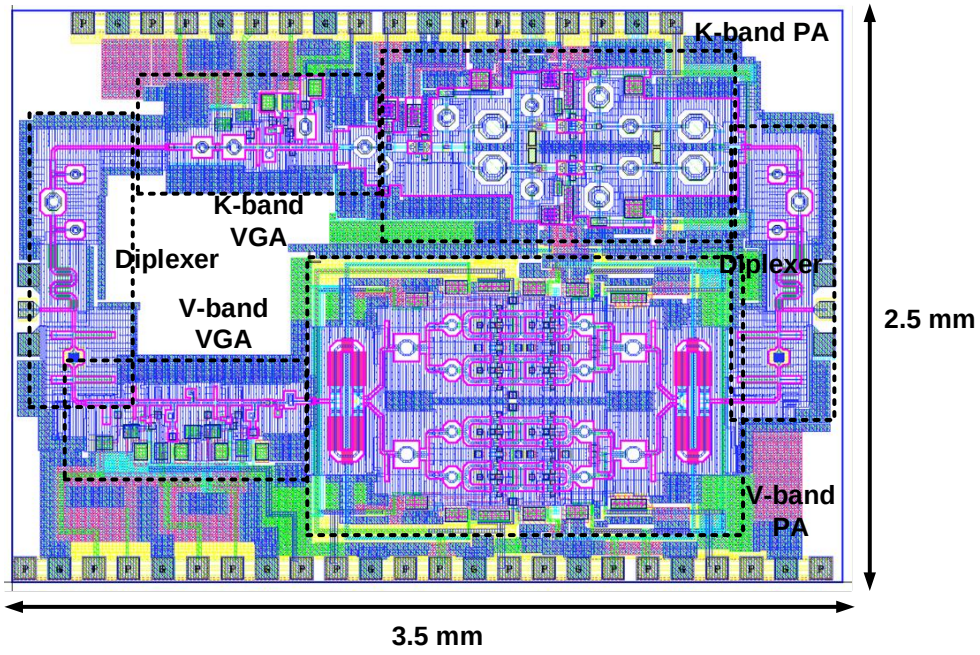


Figure 9.2. Layout of the proposed dual-band transmitter front-end.

input signals. The input signal is split by the input diplexer and the two divided signals are delivered to each path. The VGA and PA on each path amplify the signals and finally deliver them to the output diplexer, which transmits these signals to the common output port. In addition, the VGA at each path amplifies the signals as well as provides gain control leading to various output powers for the signals.

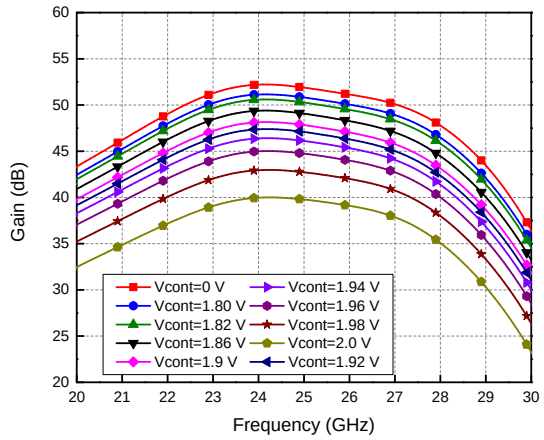
9.2 Dual-band Transmitter Integration

The designed transmitter front-end is a concatenation of individual constituents as shown in Figure 9.2. The overall chip size is 3.5× 2.5 mm^2 including two GSG RF probes and two multi-contact DC probe pads used for on-wafer measurement. All interconnection and feeding transmission lines at the input and output are designed as CPW on the top thickest metal layer. To reduce the overall size, the interconnections are minimized among the components. Also, the layout of the diplexers has been

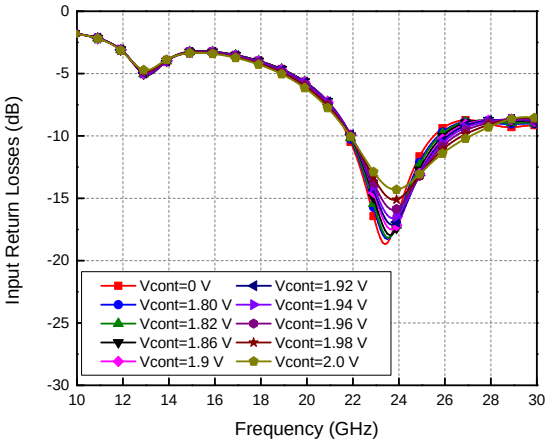
modified from that presented in Chapter VII to place the two output ports vertically, which results in reduced horizontal dimension. The metal stacked ground plane, from the bottom metal (M1) to the top metal (M6), is utilized as the common ground plane so that it can keep firm ground potential as well as satisfy the required metal density of all metal layers as imposed by the process design kit. Two DC probe pads, 18-pins and 24-pins, are inserted at the upper and bottom side of the chip, and the bias networks for K-band VGA and PA are distributed to connect to the upper 18-pins pads. Likewise, the whole bias circuits for the V-band VGA and PA are distributed for the bottom 24-pins DC pads connection. With all the design considerations, the integrated dual-band transmitter has been optimized to have high gain, high output power, high isolation as well as decent gain control ranges for K- and V-band.

9.3 Simulation Results

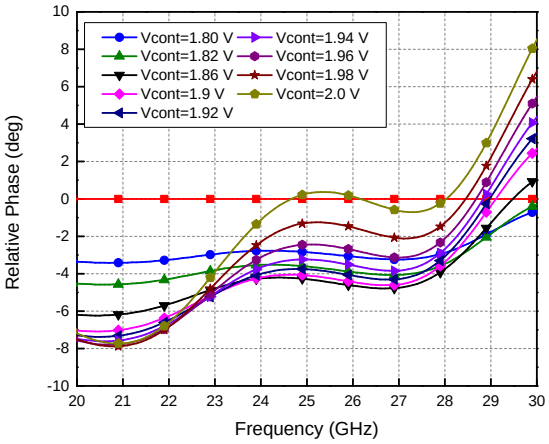
Figure 9.3 presents the simulated gains, input return losses, and phase variations with various control voltages of the K-band VGA between 20 and 30 GHz. It is seen that the transmitter operation for K-band results in excellent performance. The maximum gain at 24 GHz, shown in Figure 9.3(a), is 52.3 dB and the gain tuning range is 12.4 dB between 39.9 and 52.3 dB. The input insertion losses for various gain states are exhibited in Figure 9.3(b) and they are larger than 14.3 dB at 24 GHz. The output return losses for the different gain states remain as constant since the output return losses of the VGA change quite small with different gain states as explained in Chapter VIII, and it does not alter the following K-band PA's and output diplexer's performances significantly. The transmission phase variation for the various gain states relative to the maximum gain state is plotted at Figure 9.3(c). From the simulation, the achieved phase variations for different gain states are less than 4.3° at 24 GHz. These small phase variations are expected because the phase



(a)

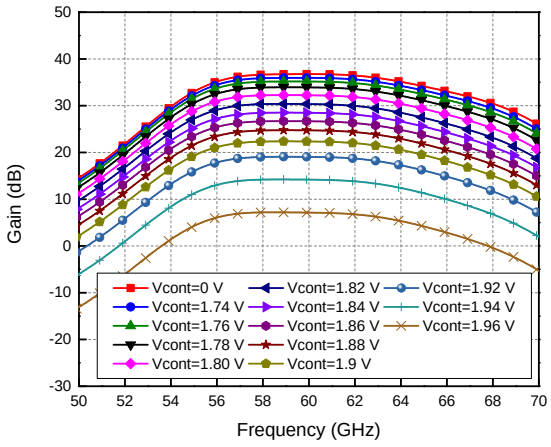


(b)

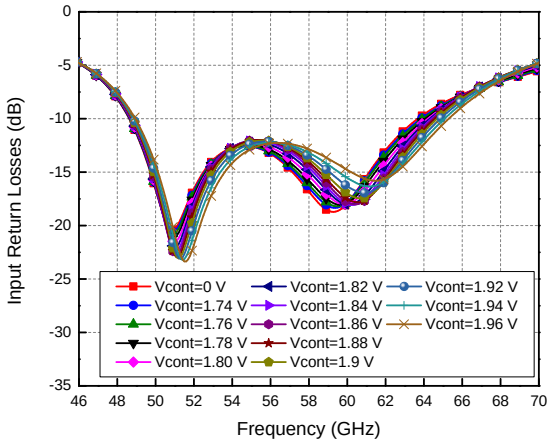


(c)

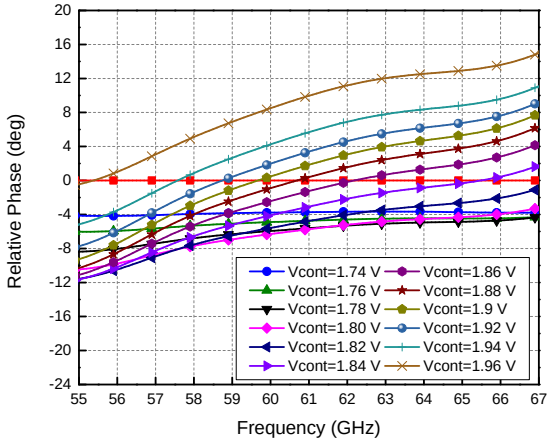
Figure 9.3. Simulation results of designed transmitter for K-band signal with respect to different control voltage (a) gain control, (b) input return losses, and (c) relative phase variation to maximum gain state.



(a)



(b)



(c)

Figure 9.4. Simulation results of designed transmitter for V-band signal with respect to different control voltage (a) gain control, (b) input return losses, and (c) relative phase variation to maximum gain state.

Table 9.1. Summary of the performances for the designed dual-band transmitter front-end.

	24 GHz	60 GHz
Maximum Gain	52.3 dB	36.8 dB
Gain Control Range	39.9-52.3 dB	7.2-36.8 dB
Input Return Losses	$>$ 14.3 dB	$>$ 14.7 dB
DC Power Consumption	478 mW	1.01 W

variations are produced by the VGA, not from the other components, thereby they follow the tendency of the VGA.

Figure 9.4 shows the simulated results of the controlled small-signal gains and input return losses between 50 and 70 GHz and the phase variation between 55 and 67 GHz with respect to different gain control voltages of the V-band VGA. It is noted that the control voltage for the 1^{st}- and 2^{nd}-stage of the V-band VGA is the same ($V_{cont1} = V_{cont2} = V_{cont}$). Firstly, the gain control performance in this case is illustrated in Figure 9.4(a), and the maximum gain at 60 GHz of 36.8 dB is achieved, and gain tuning range is 29.6 dB, which is from 7.2 to 36.8 dB. The input return loss characteristics still remain as excellent while varying the gain performances as shown in Figure 9.4(b). Specifically at 60 GHz, the input return losses are larger than 14.7 dB for all different gain states. The performances of the output return losses are rarely affected with the gain variations due to the same reason for the previous situation. For the phase variation for different gain states, it is less than 8.5° achieved at 60 GHz, which is almost same as the variation rate for the V-band VGA only as mentioned in Chapter VIII. Table 9.1 shows the summarized performances of the designed dual-band transmitter front-end.

9.4 Conclusion

In this chapter, a highly integrated K/V dual-band transmitter front-end designed and implemented on 0.18-μm SiGe BiCMOS technology is presented. This transmitter is comprised of two diplexers, K-band VGA, V-band VGA, K-band PA, and V-band PA. The transmitter exhibits a peak gain of 52.2 dB and 36.7 dB and gain tuning range of 39.9-52.3 dB and 7.2-36.8 dB at 24 and 60 GHz, respectively with low phase variation. By employing diplexers at the input and output, the signal path can be separated and each input signal can transmit and be amplified by their variable gain amplifier and power amplifier and delivered to the common output port. In this sense, each signal path can be optimized for the best possible performance. This work demonstrates the possibility for implementing high performance mm-wave dual-band transmitters using silicon technologies on single chips.

CHAPTER X

SUMMARY AND CONCLUSION

High demands for numerous wireless applications in our lives push engineers and scientists to develop advanced technologies more and more for people's smart life-styles. It gives rise to new applications in microwave and mm-wave ranges, resulting in drawing high attention for developing new wireless communication systems. The great merits of silicon technologies drives aggressively to develop microwave and mm-wave components and systems, but some challenges still remain.

In this dissertation, several promising techniques and circuit architectures manifesting unprecedented performance have been proposed and validated for developing microwave and mm-wave circuits and systems using a commercial SiGe BiCMOS process.

Firstly in Chapter II, the concurrent tri-band PA, which covers 10-19 GHz, 23-29 GHz and 33-40 GHz on 0.18-μm SiGe BiCMOS process has been developed. The concurrent tri-band PA utilizes the distributed amplifier topology with capacitive coupling to increase the power handling capability and series peaking inductor at each gain cell provides gain and bandwidth enhancement. Especially, two active notch filters having negative resistance in each gain cell are incorporated to the concurrent tri-band PA to make tri-band gain response. The GCPW is employed to input and output synthetic transmission lines for loss minimization. The concurrent tri-band PA exhibits fairly flat responses in gain and output power across the designed three bands and good input and output matching up to 40 GHz. It can operate in tri-band as well as dual-band and single-band modes. The concurrent tri-band PA should be attractive for tri-band communication and sensing systems operating in

Ku, K and Ka-bands.

In Chapter III, a broadband PA operating across a bandwidth wider than K-band has been designed and validated. The designed PA incorporates the lumped-element Wilkinson power divider and combiner exhibiting wideband low-pass filtering characteristics, harmonic suppression as well as size reduction and it gives rise to design high performance PA possible using silicon process. The designed PA achieves more than 34.5-dB gain and very flat out power of 19.4 ± 1.2 dBm across 16.5-28 GHz with PAE higher than 20 % and 17 % between 16-24.5 GHz and up to 28 GHz, respectively. At 24 GHz, the measured output power is 19.4 dBm with peak PAE of 22.3 %.

In Chapter IV, a high performance V-band PA has been presented. The designed V-band PA is synthesized by integrating four identical unit-PA cells and the new four-way parallel power combining and splitting networks. Each unit-PA cell is designed as two stage pseudo-differential cascode amplifier. The proposed four-way parallel power combiner/splitter is consisted of the wideband low-loss capacitive loading slow-wave Wilkinson structure and two transformers connected in parallel at each branch of Wilkinson structure. The developed PA can achieve an output power of 18.8 dBm as well as power gain of 19 dB at 60 GHz. The four-way parallel power combiner/splitter has also broadband performance and it makes very flat output power characteristic between 55 and 65 GHz. Moreover, the 3-dB bandwidth of designed PA is 10.7 GHz that can cover whole unlicensed V-band spectrum.

In Chapter V, a millimeter-wave Wilkinson power divider which has two arms implementing capacitive loading and slow-wave CPW has been designed and presented. The designed power divider structure exhibits good performance over an extremely wide bandwidth. It achieves very low insertion loss from DC to 67 GHz and high isolation across 37-67 GHz. The designed slow-wave CPW configured with periodic

metal strips orthogonal to the CPW could prove to be a viable transmission line for low-loss and miniature silicon-based RFICs.

In Chapter VI, the two-way and 16-way K/V dual-band power combining and splitting networks based on the Wilkinson structure have been proposed, designed and characterized. Firstly, the two-way dual-band power divider and combiner have been developed. For miniaturization as well as forming the dual-band function, the slow-wave CPW transmission line and two series LC resonator have been employed. The insertion losses at 24 and 60 GHz are 5.3 and 5.4 dB, respectively, while all ports are very well matched. Moreover, 24 dB and 26.5 dB of isolation are obtained at 24 and 60 GHz, respectively, along with very low amplitude and phase imbalances at the two output ports. This is the first developed dual-band power divider/combiner on chip for mm-wave applications and it is a suitable candidate for a future mm-wave dual-band wireless communication and sensing systems. Based on the developed two-way dual-band power divider, the 16-way dual-band power combining and dividing network has been developed, presented, and validated. The developed 16-way power combing/splitting network integrates two-way dual-band power divider, *LC* based two-section Wilkinson power divider, and two section TL-based Wilkinson structures. Its performances have been verified with good agreement between measured and theoretical results.

In Chapter VII, the K/V-band diplexer designed by integrating two different BPFs with a T-junction matching section has been proposed. For the V- and K-band operation, the capacitive and inductive coupled resonators with 2nd-order Chebyshev response bandpass filters are designed, respectively. Moreover, due to the asymmetric out of band rejection property of the two BPFs, good isolation between two output ports is achieved. The T-junction matching section realized with high impedance of slow-wave CPW is inserted at the common port of the diplexer to combine the two

BPFs. From the measurement results, which are very well matched to the simulated ones, the performance of the proposed diplexer has been validated.

In Chapter VIII, the K- and V-band VGAs realized by employing the current steering technique and a phase compensation capacitor at the gain control device have been proposed. By utilizing the current steering technique, the designed VGAs provide wide gain tuning range with good input and output return losses while the gain is varied. In addition, the phase compensation capacitor at the gain control device introduces low phase variation for all different gain states. As a result, variable gain amplifiers with low phase variation as well as decent tuning range and power consumption working on K- and V-band can be designed.

In Chapter IX, a highly integrated transmitter prototype chip has been designed and implemented by incorporating the two diplexers, K-band VGA, V-band VGA, K-band PA, and V-band PA. The transmitter exhibits a peak gain of 52.2 dB and 36.7 dB and gain tuning range of 39.9-52.3 dB and 7.2-36.8 dB at 24 and 60 GHz, respectively, with low phase variation. By employing the diplexers at the input and output, the signal path can be separated and each signal can be transmitted and amplified by their respective variable gain amplifier and power amplifier, and each signal can finally go through the common output port of the transmitter. In this design scheme, each signal path can be optimized for the best performance. This work demonstrates the possibility for implementing high performance mm-wave dual-band transmitter using silicon technologies.

Successful development of the single-chip dual-band K/V-band transmitter along with its constituent components demonstrate not only the developments of the transmitter and and the diplexers, VGA, and PA that are capable of operating in dual-band in K and V bands for possible use in dual-band K/V-band wireless communications and sensing systems, but also the design of these on silicon technologies.

Furthermore, these successful developments also show the possibility of developing transmitters, receivers, and components for multi-band wireless communications and sensing systems operating at millimeter-wave frequencies.

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