TOPOLOGY AND CONTROL FOR PHOTOVOLTAIC MICROINVERTERS

A Dissertation

by

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ABSTRACT

Motivated by the continuously increasing world energy demands and greenhouse-gas (GHG) emissions from conventional fossil fuels, renewable energy, especially solar energy is ready to become a significant part of global energy portfolio.The microinverters, as the interface between the photovoltaic (PV) modules and the ac electrical power grid, have become popular due to the potentials to achieve high reliability, improved system flexibility and enhanced electrical safety compared with the string or central inverters. Thanks to the decreasing costs and disruptive enabling technologies, they have rapidly emerged in the global residential and even commercial PV market.

This dissertation proposes a two stage isolated PV microinverter comprised of dc-dc converter followed by dc-ac inverter. For the front-end dc-dc converter, the with enhancement gallium nitride filed-effect transistors (eGaN FETs) is used to achieve high voltage gain, soft switching and high frequency operation. To further explore the electrical and thermal characteristics of eGaN FETs, the driving signals of eGaN FETs with appropriate overlap are proposed and implemented to not only optimize the reverse conduction performance of eGaN FETs, but also avoid shoot-through current during dead time in single phase leg structure. To evaluate the cooling requirements in advance to ensure effective heat dissipation with minimized heat sink, a simplified thermal resistor model of eGaN FETs is proposed and verified thorugh both finite element analysis (FEA) and LabVIEW/ Multisim co-simulation.

Single phase inverters are inherently subject to the double line frequency ripple power at both ac and dc sides The general solutions that unify all existing power decoupling techniques is obtained. The component counts, energy utilization and voltage/current ripple of energy storage components, dc voltage utilizations of both main circuit and power decoupling circuit, and the current stresses of power devices in main circuit are derived and investigated. The evaluations on all existing power decoupling techniques for the two stage PV microinverters, are summarized to provide helpful guidance during design. A digitally implemented proportional resonant (PR) and hybrid hysteresis current control with soft switching in the dc-ac inverter of the two stage PV microinverters is proposed to reduced switching losses, optimize zero-crossing distortions and mitigate low frequency harmonics.

DEDICATION

My mother; Zhimin Wang, My wife; Shuang Chen and My son; Elliot Zhang

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NOMENCLATURE

GHG	Greenhouse-gas
PV	Photovoltaic
eGaN FETs	Enhancement gallium nitride field-effect transistors
MOSFETs	Metal-oxide-semiconductor field-effect transistors
PCB	Printed circuit board
FEA	Finite element analysis
PR	Proportional resonant
CO_2	Carbon dioxide
MPPT	Maximum power point tracking
CEC	California Efficiency Commission
DCM	Discontinuous current mode
BCM	Boundary current mode
SR	Synchronous rectification
GaN	Gallium nitride
ZVS	Zero voltage switching
ZCS	Zero current switching
ZVT	Zero voltage transition
EPC	Efficient Power Conversion Co.
RMS	Root mean square
FR-4	Flame retardant-4

SPWM	Sinusoidal pulse width modulation
SVPWM	Space vector pulse width modulation
CM	Common-mode
EMI	Electromagnetic interference
HEMT	High-electron mobility transistor

TABLE OF CONTENTS

Page

LIST OF FIGURES

Page

LIST OF TABLES

Page

1. INTRODUCTION

1.1 Renewable energy outlook

Motivated by the continuously increasing world energy demands and GHG emissions from conventional fossil fuels, renewable energy such as solar, wind, fuel cell and geothermal heat etc. are ready to become a significant part of global energy portfolio [1, 2]. In the New Policies Scenario, as shown in Figure 1.1, the share of renewable energy in three main energy utilizations towards electricity, heat and transportation will rise by 18% in 2035 [2]. Power continues to be the world's dominant fossil fuel consumer and source of energy-related carbon dioxide (CO_2) emissions [1]. To keep the increase in global average temperature to well below 2°C above pre-industrial levels [3], renewable energy must contribute significantly to transform the world's energy system as pledged from Figure 1.2, where it is revealed that before 2016, the increase of world electricity generation always keeps the same pace with that of the CO_2 emissions. With the higher penetrations of renewable energy, the CO_2 emissions and world electricity generation will start decoupling after 2016 [1]. According to the statistics, electricity generated from renewable energy sources is growing rapidly and increases by over 7,000 TWh from 2011 to 2035, making up almost half of the increase in total generation all over the world [2]. Solar energy, as one of significant renewable energy in power generation, increased by 43% (29.4GW) in 2013, accounted for 15% of the total growth in global power generation capacity [2]. From Figure 1.3, in 2035, electricity produced from solar PV can rise to 950

TWh and reach up to 690GW [2]. Solar PV continues to receive the largest portion of subsidies just before 2040 worldwide to make competitiveness a moving target [4].

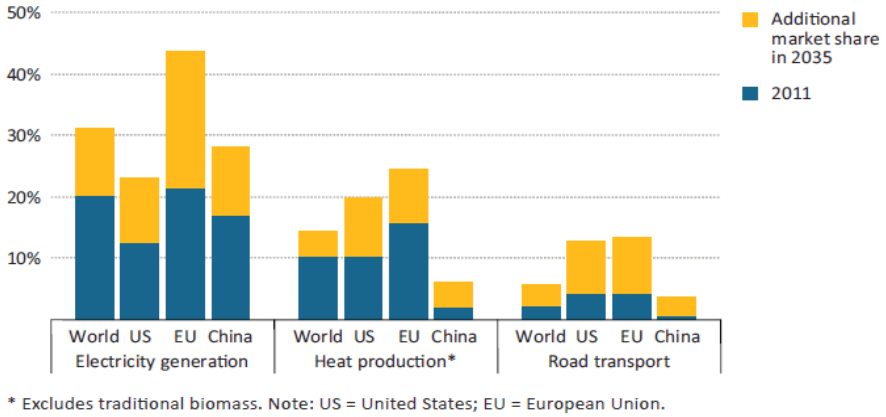


Figure 1.1: Renewable energy share in total primary energy demand by category and region in New Policies Scenario of 2011 and 2035 [2].

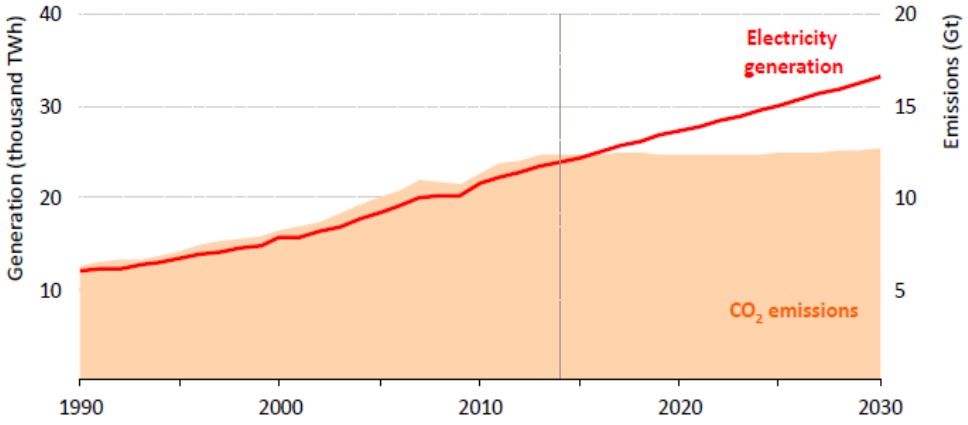


Figure 1.2: Trendency between world electricity generation and related CO_2 emissions [1].

In U.S., electricity from solar PV is more affordable than ever. The average price of a completed commercial PV project in Q2 2014 has dropped by 14% year over year and by more than 45% since 2012. There are over 22,700MW of cumulative solar electric

capacity operating now, enough to power more than 4.6 million American homes as shown in Figure 1.4 [5].

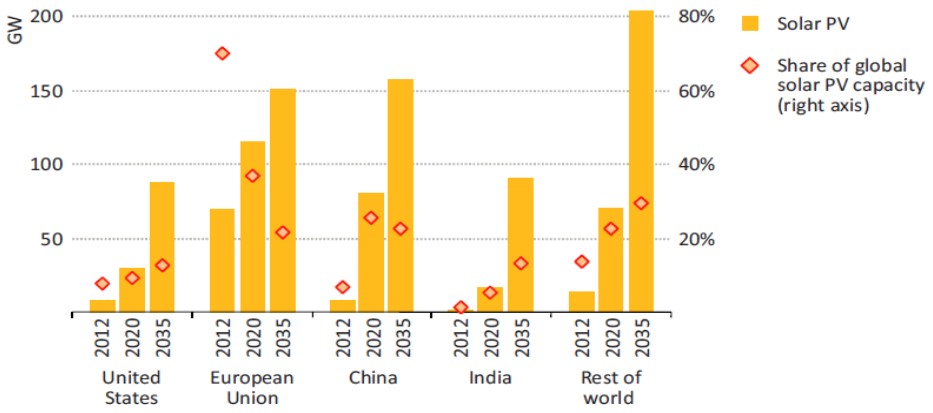


Figure 1.3: Installed solar PV capacity by region in New Policies Scenario of 2012, 2020 and 2035 [2].

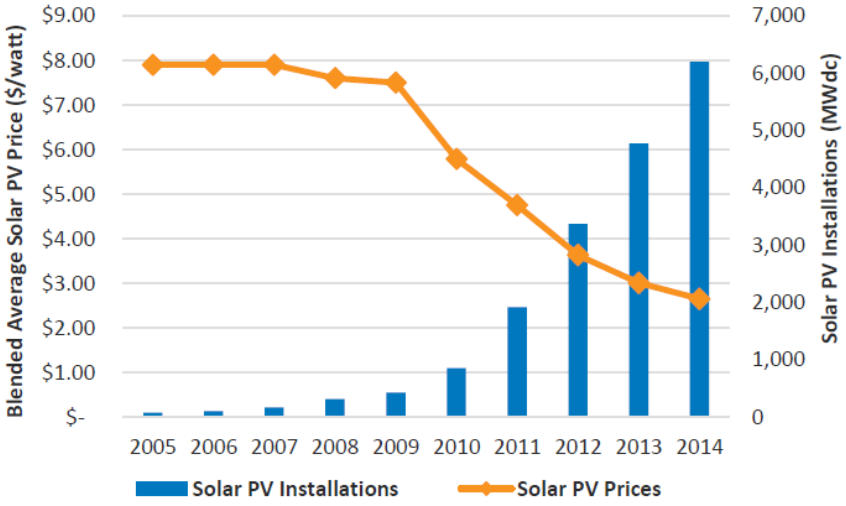


Figure 1.4: Solar PV installation and solar PV price from 2005 to 2014 in U.S. [3].

1.2 Opportunities and challenges for the photovoltaic microinverter

As the interface between PV modules and the ac power grid, PV inverters play a critical role in efficient and reliable PV generation systems. Generally, there are three different types of PV inverters in terms of system configurations, power ratings and applications: central inverters, string inverters and microinverters [6-8]. Figure 1.5 illustrates the typical configuration of microinverter PV system in which it is observed that every PV module is attached by a PV microinverter and the numerous microinverters are connected to the power grid through ac connection. Compared with the central and string inverters, PV microinverters is becoming more popular, in part, because of the potential to achieve high reliability, improved system flexibility and enhanced electrical safety [7, 9, 10]. Thanks to the decreasing costs [11-13] and disruptive enabling technologies [14-16], they have rapidly emerged in the global residential and even commercial PV market [17-19] and with module level maximum power point tracking (MPPT), are an effective method to maximize energy harvest from solar [20-27]. In 2013, PV microinverters accounted for over 30% of the inverter shipments to PV systems of

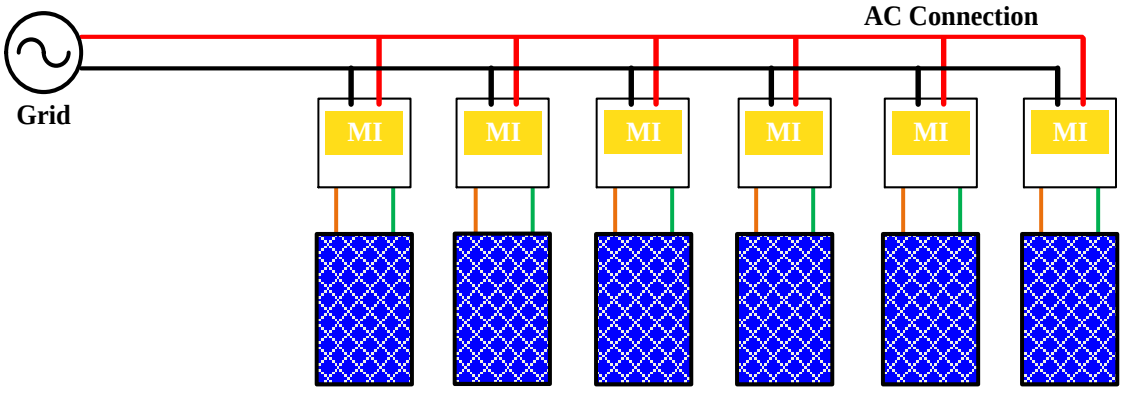


Figure 1.5: Configuration of microinverter PV system.

Table 1-1: Transformer isolated commercial products from main PV microinverter manufacturers until 2015 [22-30].

Type Designation	Manufacturer	Max. Input Voltage	Input Voltage Range	Rated Power	Nominal AC Voltage/Range	Max. Efficiency/CEC Efficiency	Dimensions	Weights	Year in the Market
SB 240-US-10	SMA	45V	23~39V	240W	2*120V/211~264V	95.9%/96%	188.4/218.4/43.7mm	1.3kg	2014
S230-60-LL-2-US	Enphase	48V	16~48V	220W	208V/183~229V (208VAC)	96.7%/96.5% (208VAC)	172/175/35mm	1.8kg	2015
					240V/211~264V (240VAC)	97.2%/97% (240VAC)			
S280-60-LL-2-US	Enphase	48V	16~48V	270W	208V/183~229V (208VAC)	96.8%/96.5% (208VAC)	172/175/35mm	1.8kg	2015
					240V/211~264V (240VAC)	97.3%/97% (240VAC)			
P250LV	SolarBridge (SunPower)	48V	18~37V	238W	208V/183~229V (208VAC)	95.7%/95%	272.3/101.3/35.3mm	1.6kg	2012
P250HV		64V	25~50V		240V/211~264V (240VAC)				
MICRO-0.25-I-OUTD	ABB	65V	12~60V	250W	208V/183~228V (208VAC)	96.5%/96%	266/246/35mm	1.65kg	2011
					240V/211~264V (240VAC)				
MICRO-0.3-I-OUTD		65V	12~60V	300W	208V/183~228V (208VAC)				
					240V/211~264V (240VAC)				
MICRO-0.3-HV-I-OUTD		79V	19~75V	300W	208V/183~228V (208VAC)				2014
					240V/211~264V (240VAC)				
YC250A	Apsystems	55V	22~45V	250W	240V/211~264V	95.5%/94%	160/15029mm	1.5kg	
YC500A				500W	208V/183~228V (208VAC)	95.5%/95%	221/167/29mm	2.5kg	2014
					240V/211~264V (240VAC)				
MIG240UL00	Darfon	60V	24~40V	220W	240V/211~264V (240VAC)	95.7%/95%	220/130/37mm	2.5kg	2013
MIG300				250W	240V/211~264V (240VAC)	95.8%/95%			2014
MIG320			Specifications are still unavailable						2015
Replus-250A	ReneSola	55V	22~45V	225W	240V/211~264V (240VAC)	96.3%/95%	230/138/35mm	2kg	2012
Replus-250B					208V/186~228V (240VAC)				2012
Replus-250					230V/200~270V (240VAC)				

under 100kW in the USA. The global shipments of microinverters are forecast to increase by over 40% a year on average through 2017 compared to just 13% for the total PV inverter market. By 2017 global cumulative PV microinverter shipments are forecast to reach over 7GW [28]. To satisfy the high demands of PV microinverters, more and more companies all over the world are coming into this market. Table 1-1 shows several transformer isolated commercial products from main PV microinverter manufactures until 2015 [29-37]. From that, it is observed that 1) since every microinverter is connected to single PV module as shown in Figure 1.5, the input voltage is low (in the range of 12V~60V), which means that a high voltage gain is needed to satisfy the requirement of grid-connection; 2) the power rating is almost around 200W~300W; 3) the California Efficiency Commission (CEC) efficiency is about 96%, which is lower than that in string or central inverter (about 98%); 3) the volumn and weight are always minimized to improve the power density.

In terms of galvanic isolation, PV microinverters can be divided into transformer-less and transformer isolated configuration [6, 8, 14, 38]. For the former, by eliminating the high frequency transformer, lower cost, smaller volume and higher efficiency can be achieved at the cost of increased ground leakage current and limited voltage gain [39, 40]. For the latter, they can be classified into single stage and two stage topology [8, 14]. In single stage topology, flyback or isolated buck-boost inverter are the most popular ones. Even though less power devices can be used, the voltage boost, isolation and output current shaping are all implemented through flyback or isolated buck-boost circuit which inevitably complicates the design of high frequency transformer [41-47]. To further

improve the efficiency and simplify the control loop, discontinuous current mode (DCM), boundary current mode (BCM) [48], hybrid switching strategy (DCM and BCM) [49], synchronous rectification (SR) [50] and active clamping of main power devices [51, 52] have been investigated. In the two stage topology, the front-end dc-dc converter is used to achieve voltage boost and isolation, and usually H-bridge inverter, as the second stage, is used to regulate the current flowing into the grid. For the front-end converter, the design towards high step-up, low cost and high efficiency is always the main challenge [53, 54]. Due to the simple structure, the optimizations of the dc-ac inverter are focused on control strategies to reduce switching losses of power devices, and improve power quality and transient performance [55-58]. What's more, since single phase inverters are inherently subject to the double line frequency ripple power at both ac and dc sides, which could lead to adverse system performance [59], active power decoupling techniques are desirable to replace bulky and short lifetime electrolytic capacitor with reliable film capacitor [60-62]. Thus, different active power decoupling topologies, control and modulation strategies have been developed [63] which show different characteristics on components counts, energy utilization and voltage/current ripple of energy storage components, dc voltage utilizations, and current stresses. Given the requirements of low cost, high reliability, high efficiency, high power density and easy-to-implement in the two stage PV microinverters, it is always necessary to evaluate the existing power decoupling techniques and find out appropriate solutions.

1.3 Research motivations and objectives

In the two stage transformer isolated PV microinverters topology, the front-end dc-dc converter must achieve high voltage gain with a simple topology, low power devices counts and easy-to-implement control strategy. To boost the voltage gain and avoid extreme duty ratio, high frequency transformer, coupled inductor, voltage doubler or switched capacitor can be combined with the typical step-up dc-dc converters. The resonant tank is advantageous to achieve soft switching and allow high switching frequency. The advent of gallium nitride (GaN) power devices, regarded as promising next generation semiconductor technology, enables PV microinverters with higher efficiency and higher power density to become possible. Compared with conventional silicon based ones, since GaN power devices show their own electrical and thermal characteristics, it is necessary to be evaluated and optimized to maximize their performance.

For single phase inverter, it is always necessary to balance the instantaneous power of input and output sides through energy storage components. The general solutions on the voltage or current of energy storage components are critical to understand the principle of power decoupling, investigate exisiting power decoupling techniques and innovate new topologies, control or modulation strategies. Since the conventional passive power decoupling approaches using bulky electrolytic capacitors and inductors, confront the issues like limited lifetime, high masses and volumes, numerous active power decoupling techniques including series and parallel power decouplings have been developed for different applications. To ensure low cost, high reliability, high efficiency, high power

density and easy implementation, different power decoupling techqniues should be evaluated comprehensively to provide guidances in the two stage PV microinverters.

The switching power losses due to hard switching operation are always the main issue that limits the increase of switching frequency in the conventional H-bridge dc-ac inverter. Thus soft switching techniques are always preferred. Bipolar hysteresis current control with soft switching can reduce the switching losses greatly and also provide inherent fast dynamic response and robust current regulation. To further reduce the switching frequency, unipolar modulation, enabling halved switching frequency of power devices, can be applied without increasing the output inductance. However, the zero-crossing distortions and low frequency harmonics of the grid current resulted from wide hysteresis bands, dead time, driving circuit delays and sampling intervals can worsen the power quality flowing into the grid. Thus, the control strategy to compensate zero-crossing distortions and mitigate low frequency harmonics must be developed.

With the research motivations mentioned above, the research objectives in my thesis can be summarized as follows.

- In order to avoid extreme duty ratio or turns ratio, the front-end dc-dc converter with high voltage gain is proposed and build up. At the same time, the soft switching techniques are explored to allow higher switching frequency.
- In order to make full use of the superior features of GaN power devices, it is necessary to explore the electrical and thermal characteristics of GaN power devices for this application.

- In order to decouple the double line frequency ripple power, the general solutions on power decoupling are derived and compared. By considering the ripple power paths, all existing power decoupling techniques are investigated and evaluated to provide guidances on the design of two stage PV microinverters.
- In order to minimize the switching losses and allow higher switching frequency, the unipolar hysteresis current control strategy with soft switching in dc-ac inverter of the two stage PV microinverters is proposed and analyzed.
- In order to improve the power quality flowing into the grid, the control strategy, compensating zero-crossing distortions and mitigating low frequency harmonics of the grid current, will be discussed and verified through both simulation and experimental results.

1.4 Dissertation outline

Section 2 presents the proposed front-end resonant dc-dc converter in the two stage transformer isolated PV microinverters. With a simple topology, reduced power devices counts and easy-to-implement duty ratio control strategy, high voltage gain is achieved through boost operation, high frequency transformer and voltage-doubler rectifier together. Resonant operation enables zero voltage switching (ZVS) of high-side power devices, conditional ZVS of low-side power devices and inherent zero current switching (ZCS) of rectifier diodes. The resonant inductor is integrated into high frequency transformer as the leakage inductor. The principle of the proposed topology, parameters designs and losses analysis are investigated in detail. The proposed resonant dc-dc converter can be configured as interleaved topology to extend the ZVS of low-side power devices, reduce the input current ripple and operate in higher power applications. Since eGaN FETs have no intrinsic anti-parallel body diodes, unlike conventional silicon-based metal-oxide-semiconductor field-effect transistors (MOSFETs), and exhibit poor reverse conduction characteristics, the overlapped driving signals are proposed and implemented to not only optimize the reverse conduction performance of eGaN FETs, but also avoid shoot-through current during dead time in single phase leg structure. In addition, due to the relatively low thermal conductivity of gallium nitride materials, a simplified thermal resistor model is used to evaluate the cooling requirements and ensure effective heat dissipation with minimized printed circuit board (PCB) area through FEA and LabVIEW/ Multisim co-simulation. Finally the simulation and experimental results verify the feasibility of the proposed topology and overlapped driving signals.

Section 3 presents the general solutions to achieve power decoupling, and investigations on existing power decoupling techniques. Based on the principle of power decoupling, the voltage or current of energy storage components to decouple double line frequency ripple power are derived. By taking ripple power paths and waveforms of energy storage components into consideration. all existing power decoupling topologies and modulations can be derived through the proposed solutions. The component counts, energy utilization and voltage/current ripple of energy storage components, dc voltage utilizations of both main circuit and power decoupling circuit, and current stresses of power devices in the main circuit are investigated in detail. The evaluations on different power decoupling technqiues are summarized to provide guidance on the design of two stage PV microinverters.

Section 4 presents digitally implemented PR and hybrid hysteresis current control strategy with soft switching for dc-ac inverter of two stage transformer isolated PV microinverters. The principle of unipolar hysteresis current control with soft switching is introduced first. It allows ZVS commutation around zero-crossing points and ZCS commutation in other moments of line frequency period through controlling output inductor current within the designed hysteresis bands cycle by cycle. Thus fast dynamic response, robust current regulation and soft switching can be achieved. The frequency analysis of output inductor current in terms of different parameters are investigated then. Due to wide hysteresis bands, reduced output inductance and delays from dead time, driving circuit and sampling intervals, zero-crossing distortions exist in original unipolar hysteresis current control. Therefore, hybrid hysteresis current control is proposed to

enable bipolar modulation, around zero-crossing points, to minimize the zero-crossing distortion of grid current and unipolar modulation, in other moments of the line frequency period, to halve the switching frequency of power devices without increasing the output inductance. The combined digital PR controller is implemented to further mitigate the low frequency harmonics and improve the quality of grid current flowing into the grid by minimizing the steady state error at low frequency without complicated predictive calculations. Finally, the simulation and experimental results verify the validity of the theoretical analysis mentioned above.

Section 5 presents research conclusions discussed in this dissertation and the future works will also be included.

2. FRONT-END RESONANT DC-DC CONVERTER*

2.1 Introduction

Considering the front-end dc-dc converter in two stage transformer isolated PV microinverters, it is necessary to satisfy the requirements of high voltage gain, and high efficiency across wide input and load ranges due to low and variable output of PV module. To do that, numerous techniques with high boost ratio and soft switching, as summarized in Figure 2.1, have been developed based on typical dc-dc converters with voltage boost characteristics such as boost converter, sepic converter and forward converter, etc [64-67].

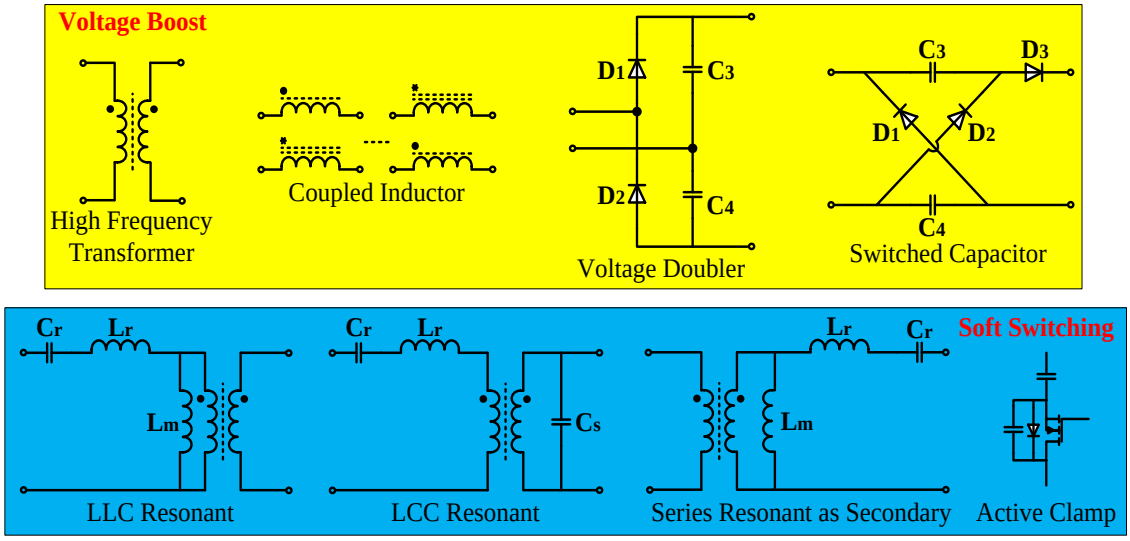


Figure 2.1: Techniques to achieve high boost ratio and soft switching for front-end dc-dc converter in the two stage transformer isolated PV microinverters.

*© 2015 IEEE. Reprinted, with permission, from H. Zhang and R. S. Balog, "Loss Analysis During Dead Time and Thermal Study of Gallium Nitride Devices," IEEE 30th Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, Mar. 2015

By combining those typical dc-dc converters with different techniques on voltage boost, isolated boost converter in [68, 69], isolated two-inductor boost converter in [70, 71], zero voltage transition (ZVT) boost converter in [66], flyback-forward converter in [53], and isolated sepic (or zeta, cuk) converter in [64, 72] can always achieve high voltage gain with appropriate duty ratio of power devices and turn ratio of high frequency transformer. However, to ensure soft switching and minimize the voltage stresses of power devices, additional active clamping circuits have to be added. At the same time, some of them need optimized design of magnetic components to achieve isolation and extra boost ratio, which can result in additional power losses of magnetic components and limit their applications in PV microinverters. The full-bridge LLC or LCC resonant converters in [73-75] can be employed to provide high set-up and inherent soft switching. However the high current through the resonant tank can increase the conduction losses. It is also hard to regulate and maintain high efficiency across wide input voltages. What's more, the variable frequency operation complicates the design of control loop and MPPT. To solve those problems, a fixed frequency hybrid series resonant converter with boost converter as secondary [67] was proposed. The boost half-bridge dc-dc converter in [76] allowed high boost ratio and ZVS of primary power devices with simple topology and quasi-square waveform of leakage inductor current.

This section proposes a high step-up front-end resonant dc-dc converter with simple topology, less power devices counts and easy-to-implement duty ratio control strategy. Combined with boost operation, high frequency transformer and voltage-doubler rectifier together, high voltage gain can be achieved. Resonant operation enables ZVS of

high-side eGaN FET, conditional ZVS of low-side eGaN FET and inherent ZCS of rectifier diodes. The resonant inductor is integrated into high frequency transformer as the leakage inductor. As promising next generation power devices [77, 78], eGaN FETs from Efficient Power Conversion (EPC) are used to replace the conventional silicon MOSFETs to eliminate the reverse recovery losses in the proposed converter. Since eGaN FETs have no intrinsic anti-parallel body diodes, unlike conventional silicon-based MOSFETs, and exhibit poor reverse conduction characteristics, the high source to drain voltage drop during dead time in single phase leg structure, can result in increased reverse conduction power losses. One of the methods to reduce that power losses is to have a schottky diode with low parasitic inductance in parallel with eGaN FET. In this way, the reverse current will flow through schottky diode rather than eGaN FET and then the forward voltage drop can be reduced greatly. Another method is the proposed driving signals with appropriate overlap. By ensuring the crossing voltages of the gate to source voltage ($v_{gs}(t)$) between high-side and low-side eGaN FETs are always below the gate to source threshold voltage ($v_{gs(th)}(t)$), the source to drain voltage can be reduced and the shoot-through current can be avoided without extra anti-paralleled schottky diodes. Another characteristic of eGaN FETs is the relatively low thermal conductivity due to silicon substrate. Since eGaN FETs from EPC are only available in die form, only multilayered PCB is mounted beneath the them to achieve heat dissipation. To evaluate the cooling requirements and ensure effective heat dissipation, a matrix resistors network, in which the thermal resistors and current sources indicate most possible heat dissipation paths and the power losses of eGaN FETs respectively, can be built up. However, it is complicated and highly dependent on

the PCB design, components placement and airflow, etc. Therefore, a simplified approach based on equivalent thermal resistor model is proposed. By calculating the equivalent thermal resistance at a prescribed maximum temperature rise and the minimum board size under worst case scenario, the cooling requirements of eGaN FETs on PCB can be estimated at different power losses.

In this section, the principle of the proposed topology, parameters designs and extended interleaved topology are explored first. Second the reverse conduction power losses optimization and loss analysis are investigated. The validity of the proposed overlapped driving signals is verified by experimental results. Then, the thermal study of eGaN FETs based on the simplified thermal resistor model is discussed and examined through both Solidwork FEA and LabVIEW/ Multisim co-simulation. Finally the simulation and experimental results verify the feasibility of the proposed topology.

2.2 Topology and operation principle

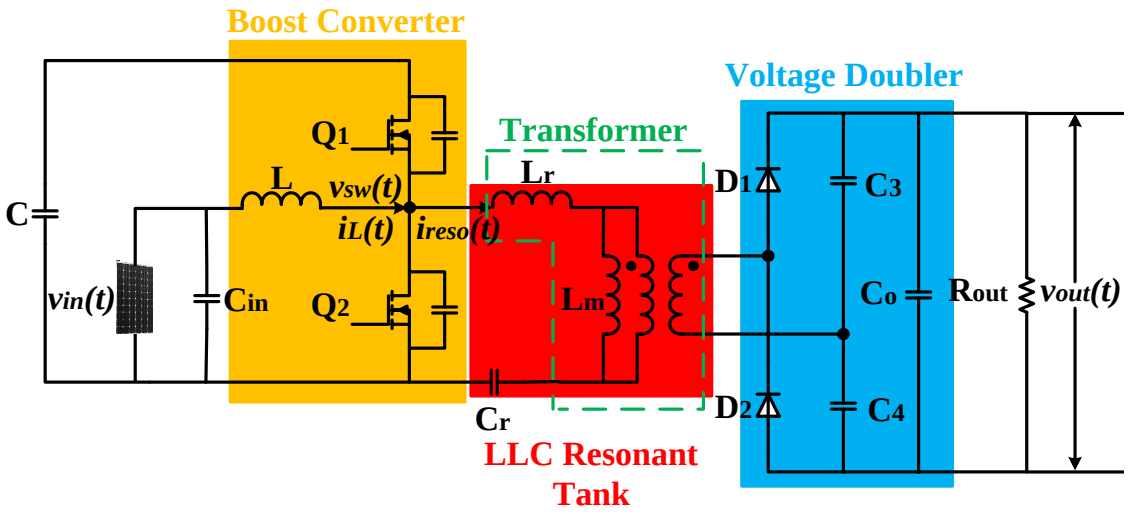


Figure 2.2: Front-end resonant dc-dc converter.

A eGaN FETs based front-end resonant dc-dc converter is proposed as the first stage of two stage transformer isolated PV microinverters as shown in Figure 2.2 where boost converter, high frequency transformer and voltage doubler are combined together to obtain high voltage gain, and LLC resonant tank is used to achieve soft switching. $v_{in}(t)$ is the input voltage from PV module. C_{in} and L are the input capacitor and boost inductor respectively. Q_1 and Q_2 are eGaN FETs, and controlled in complementary manner with fixed switching frequency. C_r represents resonant capacitor. Due to small inductance in this proposed topology, resonant inductor L_r can be integrated into high frequency transformer. L_m is the magnetizing inductor of the high frequency transformer. L_r, C_r, and L_m comprise resonant tank to achieve ZVS of Q_1, conditional ZVS of Q_2 and inherent ZCS of rectifier diodes D_1 and D_2 which comprise voltage doubler rectifier with C_3 and C_4. C_o is the output capacitor of front-end dc-dc converter which is also dc bus capacitor in two

stage PV microinverter. $v_{out}(t)$ is the output voltage which is assumed to be constant during the analysis of fron-end dc-dc converter. Figure 2.3 illustrates the typical operation waveforms of the proposed topology. Through this, the different operation modes within one switching cycle are discussed in detail.

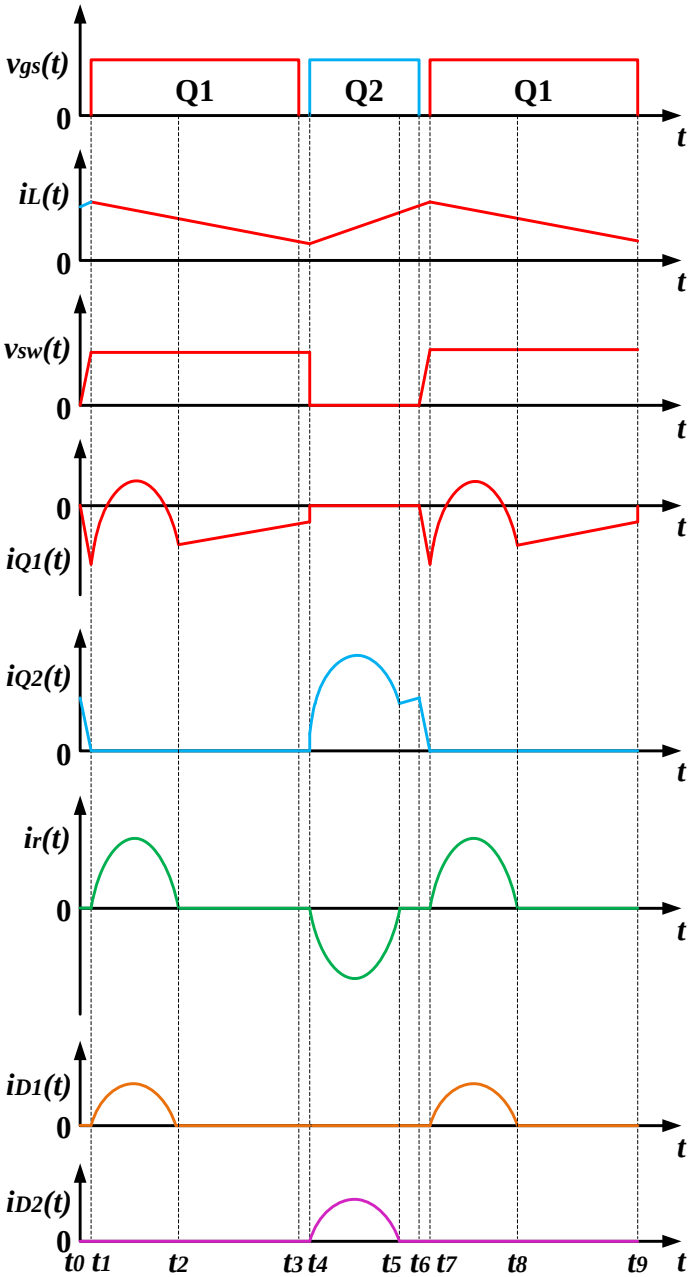


Figure 2.3: Typical operation waveforms of the proposed front-end dc-dc converter.

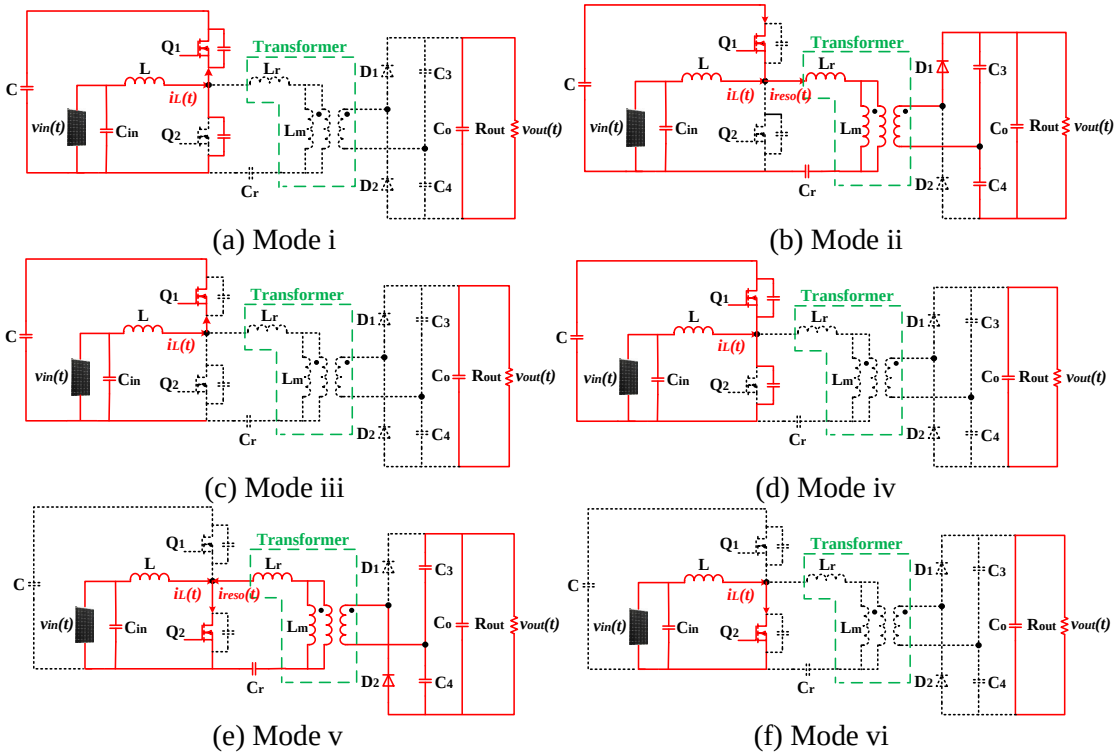


Figure 2.4: Operation modes of the proposed front-end dc-dc converter.

Mode i [$t_0<t<t_1$]: as shown in Figure 2.4(a). Q_2 turns off at t_0. The current through boost inductor L will charge the drain to source capacitor (C_{ds}) of Q_2 and discharge C_{ds} of Q_1. When the gate to drain voltage ($v_{gd}(t)$) is larger than the threshold value of gate to source voltage ($v_{gs(th)}(t)$), Q_1 will operate in the third quadrant which allows Q_1 to be turned on with ZVS at t_1.

Mode ii [$t_1<t<t_2$]: as shown in Figure 2.4(b). Q_1 turns on with ZVS. The capacitor C will resonant with L_r, C_r, secondary capacitors C_3 and C_4 through D_1. The resonant period can be given in (2.1). The current flowing through Q_1 can be expressed as shown in (2.2). Since the voltage across boost inductor is the difference between the input voltage and the voltage across C, the inductor current will decrease and is given by (2.3).

$$T_{r\_Q1} = \pi\sqrt{\frac{L_r \cdot n^2 \cdot (C_3 + C_4) \cdot \frac{C_R \cdot C}{C_r + C}}{C_r + [n^2 \cdot (C_3 + C_4)]}} \tag{2.1}$$

$$i_{Q1}(t) = i_{reso}(t) - i_L(t) \tag{2.2}$$

$$\frac{di_L(t)}{dt} = \frac{v_{in}(t) - v_C(t)}{L} \tag{2.3}$$

Mode iii [t_2<t<t_3]: as shown in Figure 2.4(c). The current through the resonant tank and rectifier diode D_1 goes to zero. The current through the boost inductor is equal to that through Q_1. There is no circulating current in the resonant tank.

Mode iv [t_3<t<t_4]: as shown in Figure 2.4(d). At t_3, Q_1 turns off. Since $v_{gd}(t)$> $v_{gs(th)}(t)$ is still satisfied, Q_1 operates in the third quadrant again. During this moment, C_{ds} of Q_2 can be discharged only if the current through boost inductor reverses its direction. Thus, the turn-on of Q_2 is conditionally ZVS.

Mode v [t_4<t<t_5]: as shown in Figure 2.4(e). Prior to the turn-on of Q_2, there is current through Q_1. When Q_2 turns on at t_4, there will be reverse recovery losses if conventional silicon MOSFETs are used. For eGaN FETs in this proposed topology, there is no reverse recovery charge. Therefore, optimized efficiency performance can be achieved even at high switching frequency. The resonant path is consisted of L_r, C_r, secondary capacitors C_3 and C_4 through D_2. The resonant period can be given by (2.4). The current through Q_2 is the sum of that through boost inductor and reosnan tank as expressed in (2.5). Since the voltage across boost inductor is the input voltage, the inductor current will increase and can be expressed in (2.6).

$$T_{r\_Q2} = \pi\sqrt{\frac{L_r \cdot n^2 \cdot (C_3 + C_4) \cdot C_r}{C_r + [n^2 \cdot (C_3 + C_4)]}} \tag{2.4}$$

$$i_{Q2}(t) = i_{reso}(t) + i_L(t) \tag{2.5}$$

$$\frac{di_L(t)}{dt} = \frac{v_{in}(t)}{L} \tag{2.6}$$

Mode vi [t_5<t<t_6]: as shown in Figure 2.4(f). The current through resonant tank and rectifier diode D_1 goes to zero. The current through boost inductor is equal to that through Q_1. There is no circulating current in the resonant tank as well.

From the analysis mentioned above and the principle of voltage-second balance, the voltage gain in this proposed front-end dc-dc converter can be obtained as:

$$\frac{v_{out}(t)}{v_{in}(t)} = \frac{n}{1-D} \tag{2.7}$$

where n is the turn ratio of high frequency transformer and D is the duty ratio of Q_2. Thus compared with conventional boost converter, n times higher voltage gain can be achieved, and there is no extreme duty ratio of eGaN FETs and turn ratio of high frequency transformer. At the same time, to achieve ZCS of voltage doubler rectifier diodes D_1 and D_2, the resonant periods in (2.1) and (2.4) should be smaller than the conduction moments of Q_1 and Q_2 respectively as shown in the equations below.

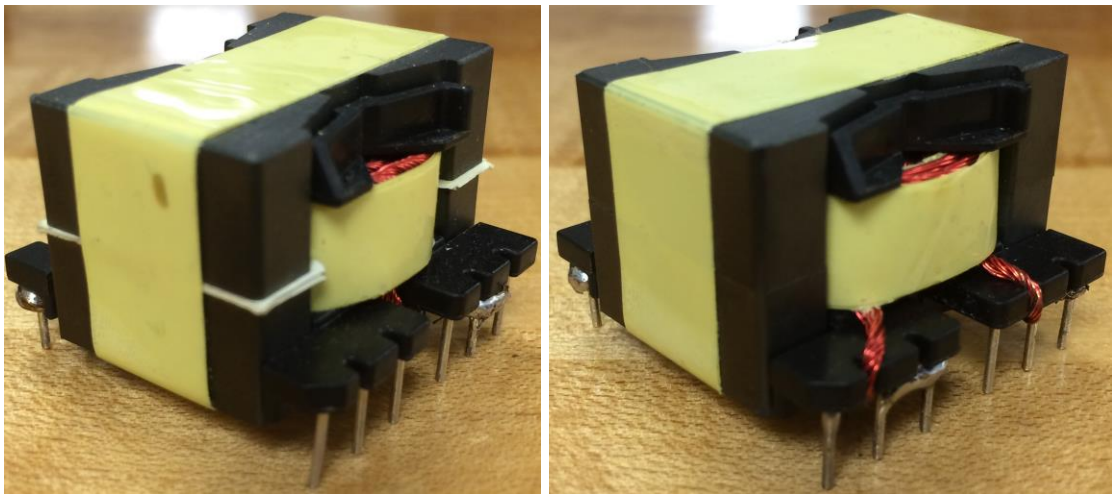
$$T_{r\_Q1} = \pi\sqrt{\frac{L_r \cdot n^2 \cdot (\mathrm{C}_3 + \mathrm{C}_4) \cdot \dfrac{C_r \cdot C}{C_r + C}}{C_r + [n^2 \cdot (C_3 + C_4)]}} \le \frac{v_{in\_\min}(t)}{f_s v_C(t)} \tag{2.8}$$

$$T_{r\_Q2} = \pi\sqrt{\frac{L_r \cdot n^2 \cdot (\mathrm{C}_3 + \mathrm{C}_4) \cdot C_r}{C_r + [n^2 \cdot (C_3 + C_4)]}} \le \frac{v_C(t) - v_{in\_\min}(t)}{f_s v_C(t)} \tag{2.9}$$

where $v_{in\_min}(t)$ is the minimum allowed input voltage from PV module. To reduce the peak value of the resonant current, the resonant periods should be as close as the minimum conduction moments of Q_1 and Q_2. The required boost inductance with certain current

ripple requirement can be given by (2.10) and Figure 2.5 shows the designed boost inductor and high frequency transformer in which resonant inductor L_r has been integrated as mentioned previously [79].

$$L \geq \frac{v_C(t)(1-D)D}{\Delta i_L(t) f_s} \tag{2.10}$$



(a) Boost inductor (b) High frequency transformer

Figure 2.5: Boost inductor and high frequency transformer in the proposed front-end dc-dc converter.

The proposed eGaN FETs based front-end resonant dc-dc converter can be configured to be interleaved topology as shown in Figure 2.6 to reduce the input current ripple, double the voltage gain further and potentially extend the ZVS turn-on of low-side eGaN FETs for high power applications [80]. The operation principle of each phase is the same with what discussed in Figure 2.3 and 2.4. Since the input current is the sum of current through boost inductors L_1 and L_2, larger ripple current through each boost inductor can be achieved while ensuring the same input current ripple. Based on the analysis on Mode iv mentioned previously, the larger ripple current potentially allows

reversed current through each boost inductor and to achieve conditional ZVS turn-on of low-side eGaN FETs. The simulation wavefroms of LTspice based on eGaN FETs EPC2001 SPICE model is illustrated in Figure 2.7 where it is observed that with ZVS of both Q_1 and Q_2, and ZCS of both D_1 and D_2, input current can still have small ripple due to interleaved operation.

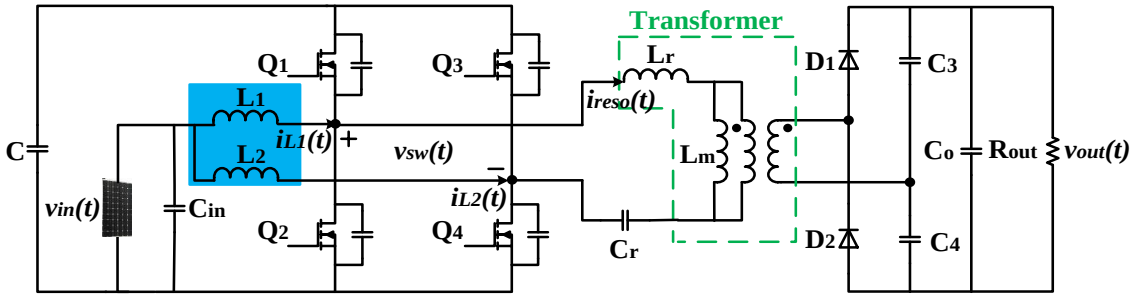


Figure 2.6: Extended interleaved topology of the proposed front-end dc-dc converter.

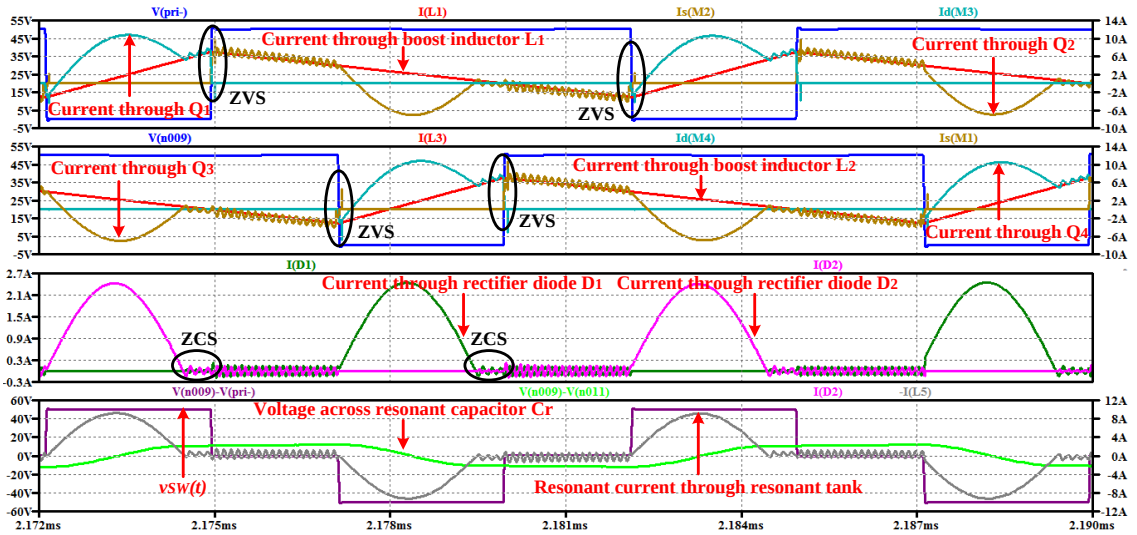


Figure 2.7: Simulation verification of the interleaved front-end resonant dc-dc converter.

2.3 Reverse conduction power losses optimization

Compared with conventional silicon MOSFETs, eGaN FETs have a purely lateral structure without parasitic bipolar junction which means that they have no built-in anti-parallel body diodes [81, 82]. This characteristic ensures that there are no minority carriers involved in conduction and no reverse recovery losses. The behaviors of eGaN FETs operating in the third quadrant from SPICE model simulation is shown in Figure 2.8 where it is revealed that while operating in the third quadrant, eGaN FETs have higher source to drain voltage ($v_{sd}(t)$) than the forward voltage drop of body diodes in silicon MOSFETs, especially when $v_{gs}(t)$ is lower than 2V. Consider the silicon MOSFET IPA180N10N3 from Infineon. As shown in Table 2.1, the forward voltage drop of built-in anti-parallel body diode (25°C) is only about 0.7V at no load and about 0.875V at 20A load condition [83]. The SPICE model simulation result in Figure 2.9 shows that $v_{sd}(t)$ of eGaN FETs also increase with drain current and temperature. Thus when eGan FETs are configured in

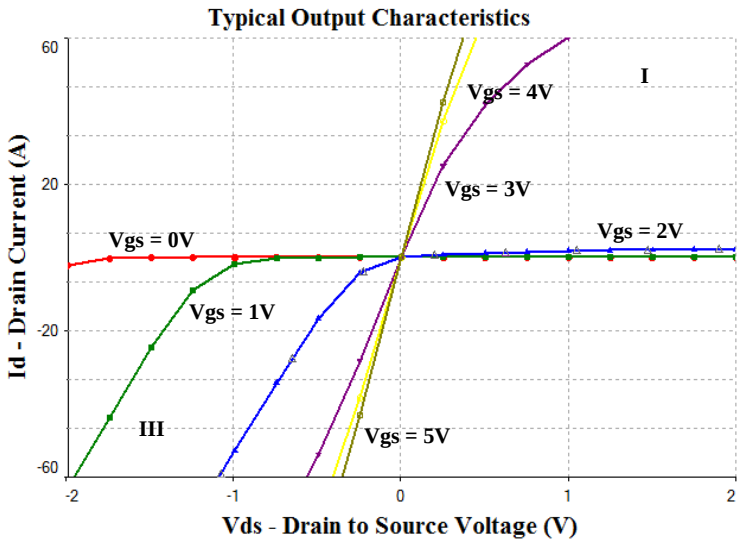


Figure 2.8: Typical output characteristic of eGaN FET EPC2001 (25°C).

Table 2-1: Comparison of $v_{sd}(t)$ between eGaN FETs and silicon MOSFETs.

eGaN FET EPC2001	Si MOSFET IPA180N10N3
$v_{sd}(t)$=2V ($v_{gs}(t)$=0V, 25°C, *no load*)	$v_{sd}(t)$=0.7V ($v_{gs}(t)$=0V, 25°C, *no load*)
$v_{sd}(t)$>2V ($v_{gs}(t)$=0V, 25°C, I_d=20A)	$v_{sd}(t)$=0.875V ($v_{gs}(t)$=0V, 25°C, I_d=20A)

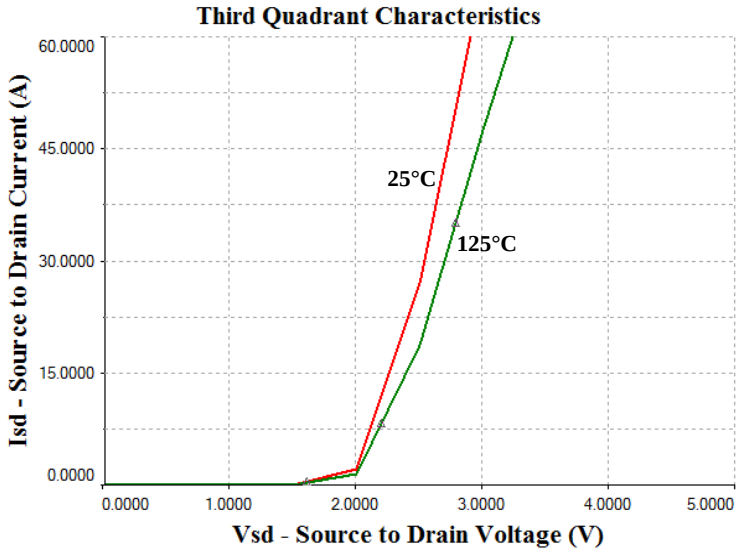


Figure 2.9: The third quadrant characteristic of eGaN FET EPC2001 (25°C).

the single phase leg structure, the large $v_{sd}(t)$ will result in substantial power losses during dead time.

One of the methods to reduce reverse conduction power losses is to have a schottky diode with low parasitic inductance in parallel with eGaN FET [84]. In this way, the reverse current will flow through the schottky diode rather than eGaN FET and then $v_{sd}(t)$ can be reduced greatly. Another method is to design the driving signals with appropriate overlap as shown in Figure 2.10(a). Take the single phase leg in this proposed front-end dc-dc converter for example (Figure 2.10(b)). When Q_2 starts turning off at t_4, the resonant

current $i_{reso}(t)$ has been decreased to zero after half resonant period. The boost inductor current $i_L(t)$ will charge C_{ds} of Q_2 and discharge C_{ds} of Q_1 to achieve ZVS for Q_1 at t_6. The time period to discharge of Q_1 completely can be approximated by (2.11).

$$t_{discharge} = \frac{C_{DS} v_C(t)}{i_L(t)} \tag{2.11}$$

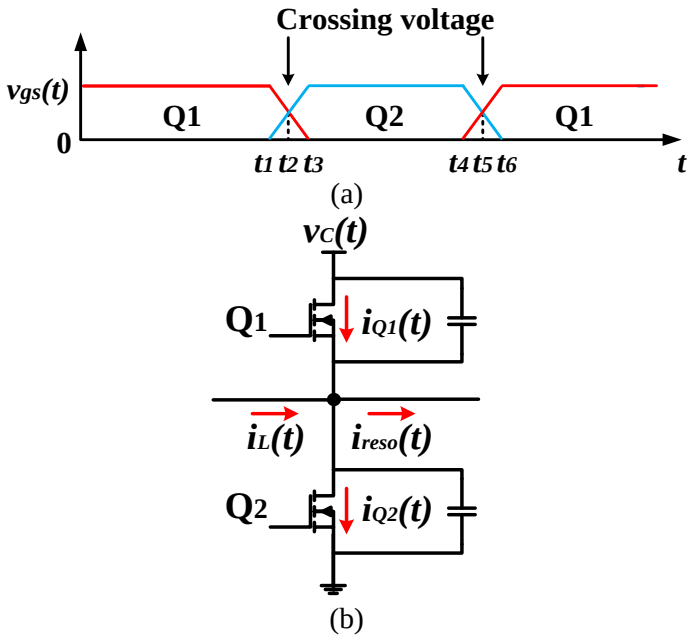


Figure 2.10: (a) The driving signals of eGaN FETs with overlap; (b) the single phase leg structure in proposed front-end dc-dc converter.

At the same time, to avoid shoot-through current, the driving signal $v_{gs}(t)$ should be smaller than the threshold voltage of eGaN FETs at t_5 [85]. When Q_2 turns off completely, $v_{gd}(t) > v_{gs(th)}(t)$ can be satisfied and Q_1 starts operating in the third quadrant. With the proposed overlapped driving signals, while Q_1 is reverse conducting, its driving signal is above 0V which means $v_{sd}(t)$ can be reduced. So the associated power losses (2.12) during reverse conduction can be reduced as well.

$$p_{rc}(t) = v_{sd}(t) i_L(t) t_{rc} f_s \tag{2.12}$$

where t_{rc} is the reverse conduction period during dead time. When Q_1 starts turning off at t_1, the current through boost inductor flows in reverse through Q_1 with small $v_{sd}(t)$. Similarly, the driving signal $v_{gs}(t)$ should be smaller than the threshold voltage of eGaN FETs at t_2. After that, when $v_{gs}(t)$ of Q_2 are higher than its threshold voltage, it starts turning on without shoot-through current. In Figure 2.11, the reverse conduction power losses comparisons with different dead times using conventional silicon MOSFETs, eGaN FETs without overlapped driving signals, eGaN FETs with schottky diodes and proposed eGaN FETs with overlapped driving signals are revealed. As shown, the reverse conduction power losses of the proposed eGaN FETs with overlapped driving signals can be reduced down to 10% of that towards eGaN FETs without overlapped driving signals and 30% of that towards eGaN FETs with schottky diodes in parallel.

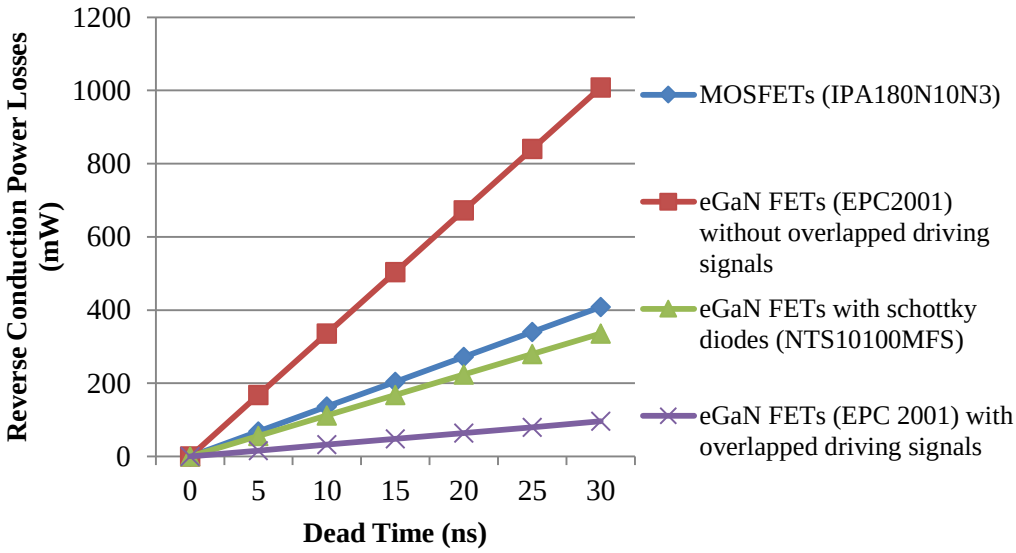


Figure 2.11: Comparisons on the reverse conduction power losses towards different methods (25°C).

The calculated power losses breakdown at 200W output power, different input voltages (25V and 50V) and different optimization methods on reverse conduction power losses are shown in Figure 2.12 where it is known that the reverse conduction power losses of eGaN FETs (EPC2001) without overlapped driving signals has higher proportion in switching losses of eGaN FETs at both 25V (8.68%) and 50V (5.6%) input voltage operating conditions. By contrast, the method of eGaN FETs with overlapped driving signals has lower reverse conduction power losses and total power losses without additional components.

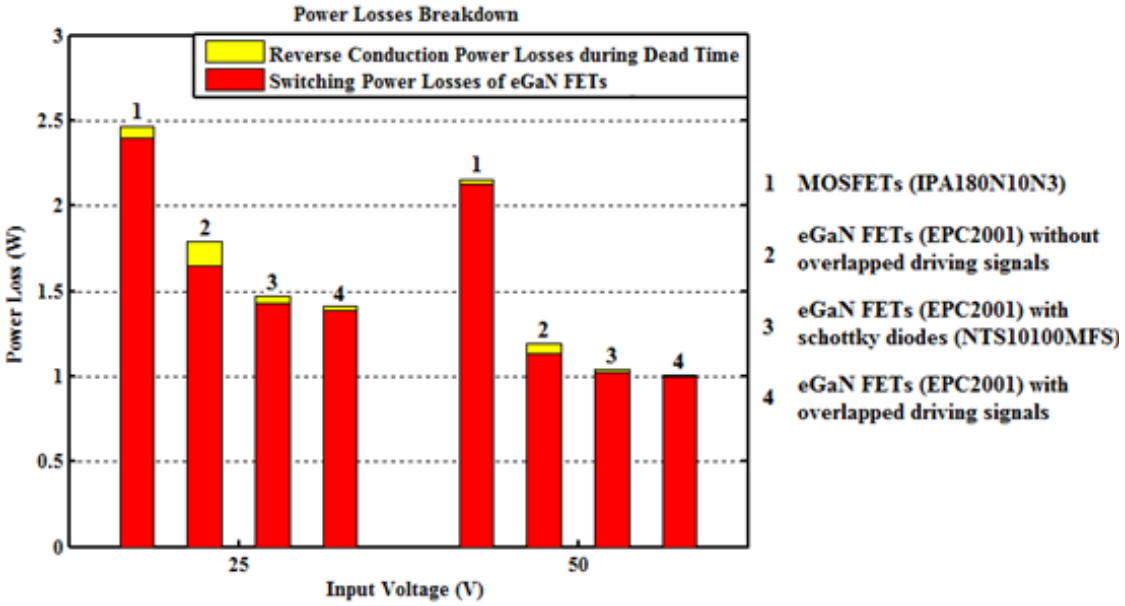


Figure 2.12: Calculated power losses breakdown of the proposed topology towards different reverse conduction optimization methods.

2.4 Loss analysis

According to the principle of the proposed eGaN FETs based front-end resonant dc-dc converter discussed above, it is known that the ZVS turn-on of Q_1, conditional ZVS turn-on of Q_2 and ZCS turn-off of voltage double rectifier diodes D_1 and D_2 can be achieved. The power transferred from the primary side to the secondary side through the high frequency transformer can be expressed as:

$$p_{trans}(t) = f_s[\int_0^{T_{r\_Q2}} v_{tr\_pri}(t) I_{reso\_p} \sin(\omega_r t)dt + \int_{DT_s}^{DT_s+T_{r\_Q1}} v_{tr\_pri}(t) I_{reso\_p} \sin(\omega_r t)dt] \quad (2.13)$$

where, ω_r is the resonant angular frequency which is related to T_{r_Q1} and T_{r_Q2}. $v_{tr\_pri}(t)$ is the primary voltage of the high frequency transformer during resonant periods and I_{reso_p} is the peak value of the resonant current. Thus the resonant current and the copper losses of high frequency transformer can be obtained below.

$$P_{trans\_loss} = {I_{reso\_RMS}}^2 R_{tr\_pri} + (\frac{I_{reso\_RMS}}{n})^2 R_{tr\_sec} \quad (2.14)$$

where, I_{reso_RMS} is the root mean square (RMS) value of the resonant current. R_{tr_pri} and R_{tr_sec} are the equivalent resistance of primary and secondary sides in high frequency transformer. Based on (2.2), (2.3), (2.5) and (2.6), the RMS current through Q_1 and Q_2 can be derived as:

$$I_{Q1\_RMS} = \sqrt{\frac{{I_{reso\_p}}^2 f_s T_{r\_Q1}}{2} + \frac{(V_{in}-V_C)^2 D^3}{3{L^2 f_s}^2} - \frac{2(V_{in}-V_C) I_{reso\_p} f_s T_{r\_Q1}}{\omega_r L} - \frac{4 I_{reso\_p} f_s}{\omega_r} \atop (I_L + \frac{V_C D}{L f_s} - \frac{V_{in} D}{2 L f_s}) + (I_L + \frac{V_C D f_s}{L} - \frac{V_{in} D f_s}{2L}) D [\frac{(V_{in}-V_C) D}{L f_s} + (I_L + \frac{V_C D}{L f_s} - \frac{V_{in} D}{2 L f_s})]} \quad (2.15)$$

$$I_{Q2\_RMS} = \sqrt{\frac{{I_{reso\_p}}^2 f_s T_{r\_Q2}}{2} + \frac{4 I_{in} I_{reso\_p} f_s}{\omega_r} - \frac{2 V_{in} D I_{reso\_p}}{\omega_r L} + \frac{2 V_{in} I_{reso\_p} T_{r\_Q2} f_s}{\omega_r L} + \frac{{V_{in}}^2 D^3 {f_s}^2}{3L^2} + (I_L - \frac{V_{in} D f_s}{2L}) D [\frac{V_{in} D}{L f_s} + (I_L - \frac{V_{in} D}{2 L f_s})]} \quad (2.16)$$

where, V_{in} and I_L are the average value of input voltage and boost inductor current. V_C is the average voltage across C. Then the total conduction power losses of both eGaN FETs can be calculated by:

$$P_{cond\_Q1Q2} = ({I_{Q1\_RMS}}^2 + {I_{Q2\_RMS}}^2) R_{ds\_oni} \quad (2.17)$$

where, R_{ds_oni} represents the conduction resistance of eGaN FETs (Q1 or Q2). Similarly, the conduction power losses of voltage double rectifier diodes D_1 and D_2 can be obtained by:

$$P_{cond\_D1D2} = 2(V_{f\_diodes} I_{avg\_diodes} + R_{diodes} {I_{diodes\_RMS}}^2) = 2(V_{f\_diodes} \frac{2 I_{reso\_p} f_s}{n \omega_r} + R_{diodes} {I_{reso\_p}}^2 \frac{T_r f_s}{2n}) \quad (2.18)$$

where, V_{f_diodes} and R_{diodes} are the forward voltage drop and equivalent resistance of D_1 and D_2. I_{diodes_avg} and I_{diodes_RMS} are average and RMS current through them respectively. From those equations above, the calculated power losses of the proposed eGaN FETs based front-end resonant dc-dc converter with different power ratings at both 25V and 50V input voltage are shown in Figure 2.13. Given the high switching frequency, hard switching turn-off of both eGaN FETs and condition ZVS turn-on of Q_2, the switching losses are the main components in total power losses especially at light load. At the same time, due to larger current through Q_2 and conditional ZVS turn-on of Q_2, both the conduction and switching losses of Q_2 are higher than that of Q_1.

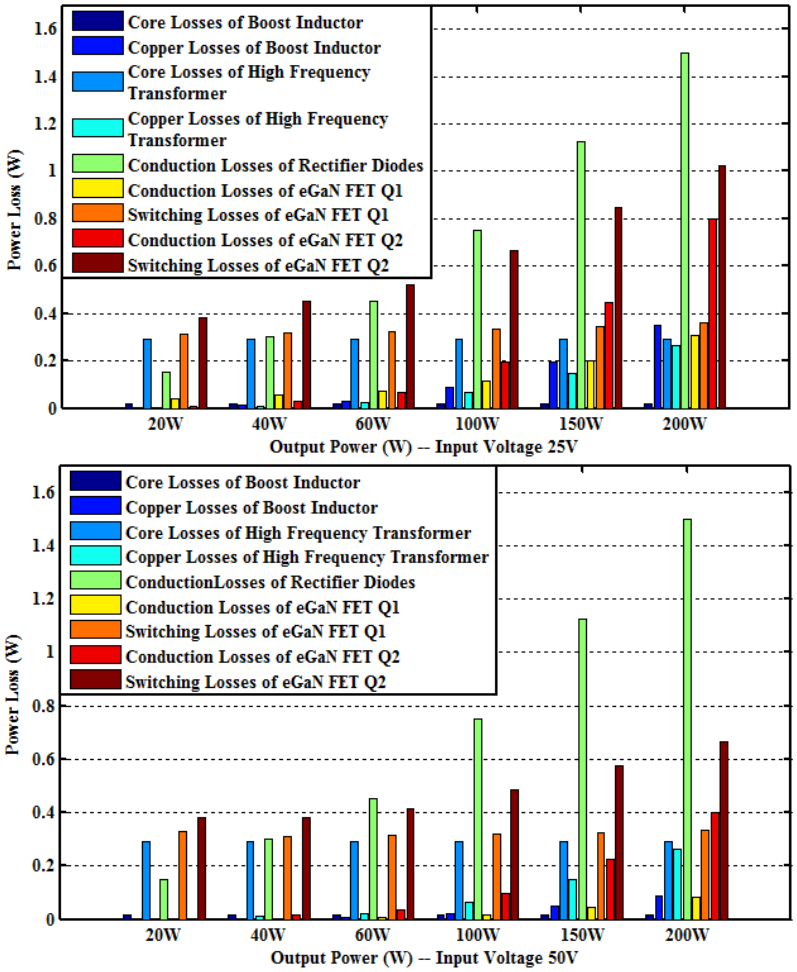


Figure 2.13: Calculated power losses breakdown of the proposed eGaN FETs based front-end resonant dc-dc converter with different power ratings.

2.5 Thermal study

Due to low cost of GaN power devices using silicon substrates and the unavailability of single crystal GaN substrate [86], all commercial GaN power devices including eGaN FETs from EPC are typically grown on silicon substrate. However, the relatively low thermal conductivity of silicon materials inevitably results in concerns for thermal design which is important to evaluate the reliability and power density of eGaN FETs based power converters. Generally, there are three different paths for heat dissipation including conduction, convection and radiation [87, 88]. Since eGaN FETs EPC2001 in this proposed topology are available in a die form, only a multilayered PCB with 2 oz. copper is mounted beneath them to achieve heat dissipation. To analyze thermal performance and cooling requirements of eGaN FETs, an equivalent thermal resistor model of heat transfer is used. The thermal resistor model of flame retardant-4 (FR-4) PCB is shown in Figure 2.14 approximately. In this figure, θ_{JB} is the thermal resistance

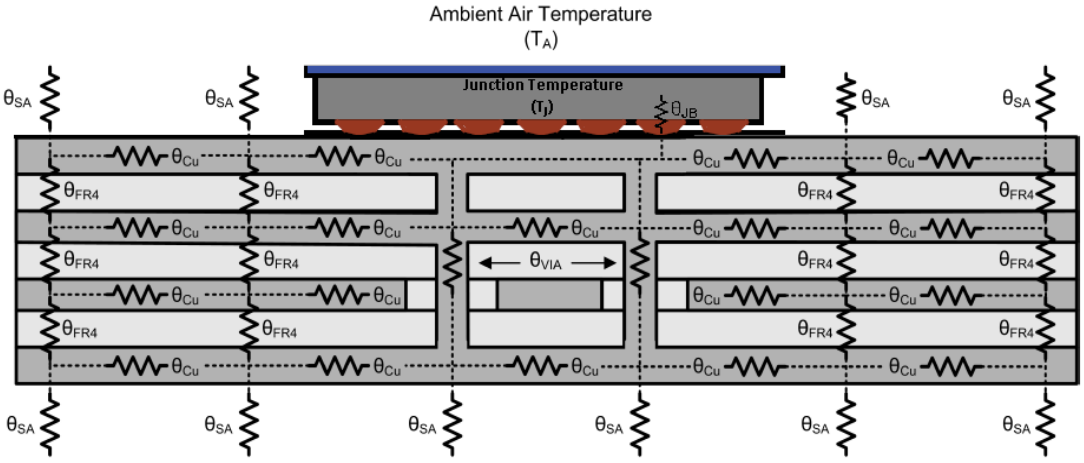


Figure 2.14: Thermal resistor model of FR-4 PCB.

from the device junction to the bottom of the solder bumps in °C/W. For eGaN FETs EPC2001, the value is 15°C/W. θ_{cu} and θ_{FR4} are the lateral thermal resistance of copper plane and the vertical thermal resistance of FR-4 substrate in °C/W respectively. θ_{VIA} is the thermal resistance of a via passing through the board transversely in °C/W. Usually, many thermal vias are placed together to form an array. θ_{SA} is the thermal resistance from the surface of PCB to the ambient air due to natural convection in °C/W. With these parameters, a matrix, including both resistors network indicating most possible heat dissipation paths and current source indicating power losses of eGaN FETs, can be built up [89]. Then the temperature rise above ambient temperature can be obtained. Acutally, the analysis mentioned above is complicated and highly dependent on the layout of PCB, components placement and airflow, etc. To further simplify the process, it is alternative to get the equivalent thermal resistance first by assuming a prescribed maximum temperature rise, and then, based on the calculated power losses of eGaN FETs, estimate the minimum size of the PCB or heat sink. When the whole thermal resistors network is replaced by an equivalent thermal resistor model, it can be expressed by (2.19).

$$\theta_{JA} = \frac{T_J - T_A}{P_{eGaN\_loss}} \tag{2.19}$$

where, θ_{JA} given in °C/W is a lumped parameter defining the equivalent thermal resistors network. T_J and T_A are device junction temperature and ambient temperature in °C. P_{eGaN_loss} is the total power losses of eGaN FETs. Then, through the relationship between the normalized thermal resistance and board area in [90], the minimum board size S_{b_min} for heat dissipation can be given by (2.20).

$$S_{b\_\min} = \frac{80.28 - \theta_{JA}}{3.7637 \frac{^{\circ}C}{W \cdot cm^2}} \tag{2.20}$$

According to the losses analysis previously, to keep the junction temperature of eGaN FETs in this proposed front-end resonant dc-dc converter from exceeding 125°C while operating with 0.4722W power losses of Q_1 and 1.0476W power losses of Q_2, the board size requirement based on the single sided, 2 oz. copper FR-4 PCB without additional heat sink are summarized in Table 2.2 below. If the thickness of PCB is increased, more thermal vias are added, or forced cooling is used, the minimum board size can be reduced. Thus the cooling requirement in Table 2.2 can be regarded as the one under worst case scenario.

To further investigate the heat dissipation of eGaN FETs on a calculated minimum size of PCB at certain ambient temperature and power rating, FEA method, which provide a fast and efficient thermal structural analysis to determine the steady state or transient thermal performance on a given design, is used and the 3D model of eGaN FETs with PCB mounted is built up in SolidWorks. From the FEA results in Figure 2.15, it is revealed

Table 2-2: Summary of the required minimized board size without heat sink.

Ambient Temperature T_A (°C)	Thermal Resistance (°C/W)	Minimized board size S_{b_min} (cm^2)
-20	95.4073	No min-limit on board area
25	65.798	3.8478
50	49.3486	8.2183
75	32.899	12.5889
100	16.4495	16.9595
110	9.8697	18.7077

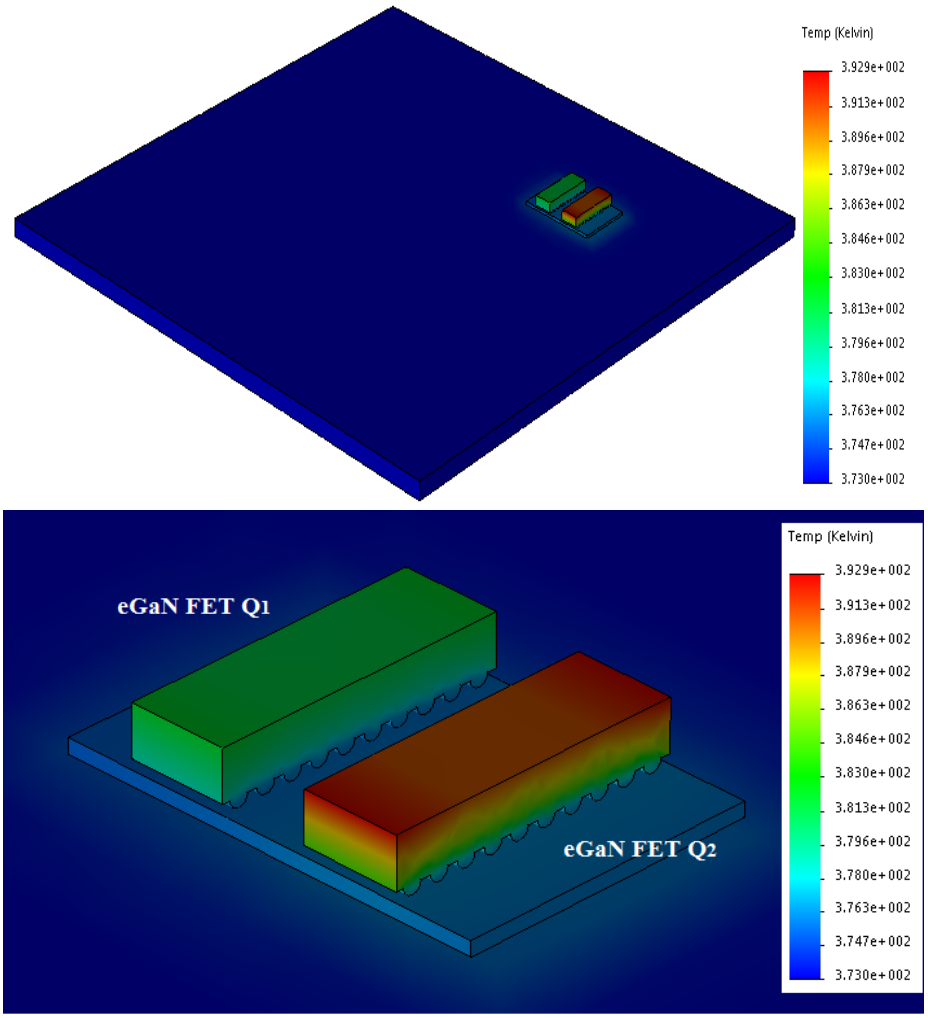
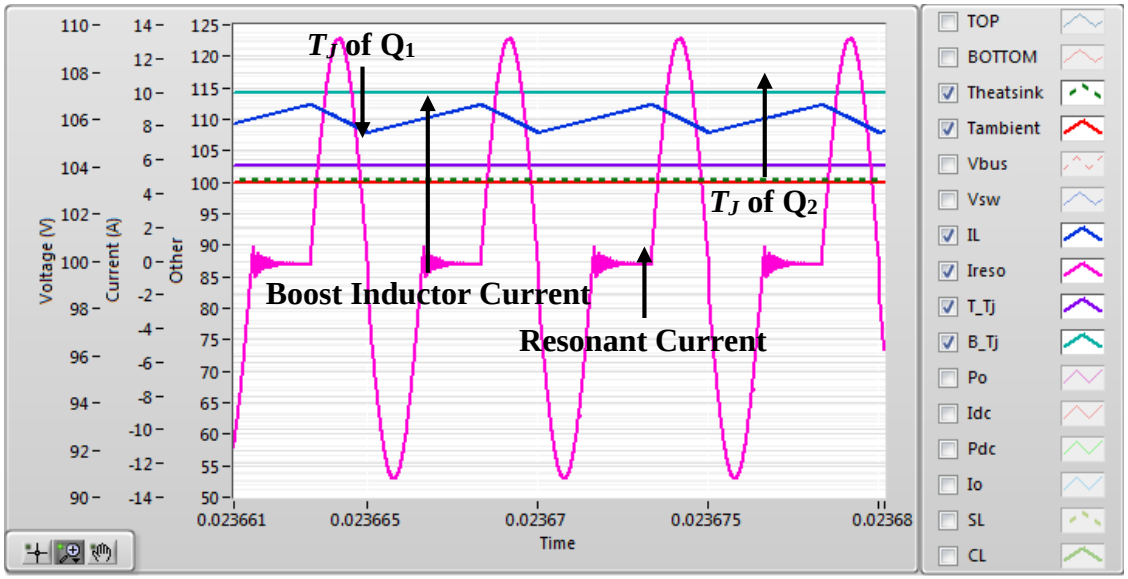
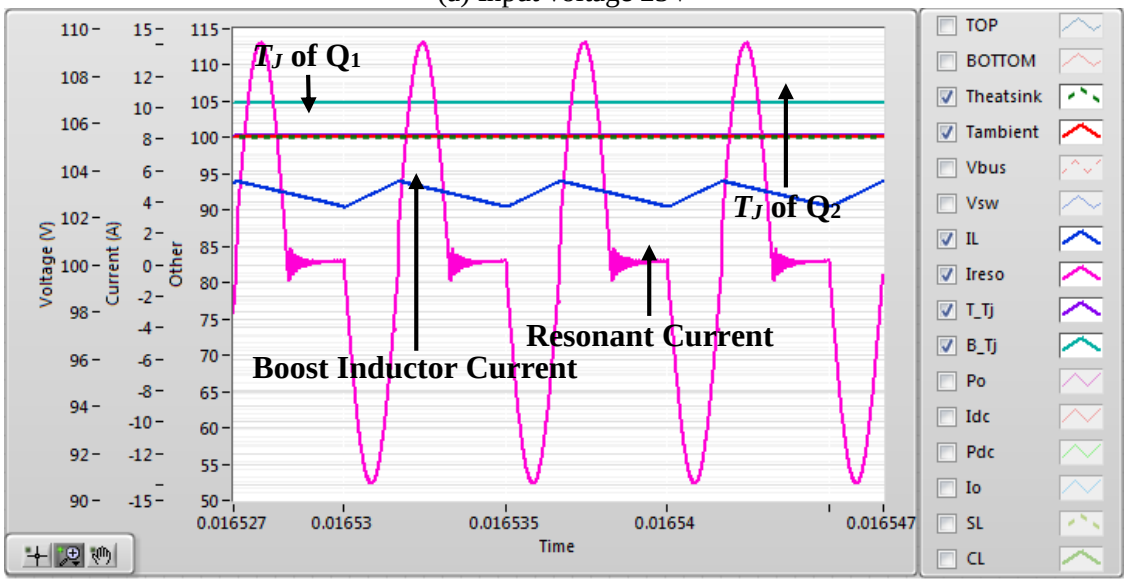


Figure 2.15: FEA thermal analysis of eGaN FETs on 16.9595cm^2 PCB at 100°C ambient temperature in the proposed front-end resonant dc-dc converter.

that when the ambient temperature is 100°C (373.15K) and the board size is 16.4495cm^2, the temperature rise of both eGaN FETs can be limited to no more than 125°C. Q_2, due to higher power losses as discussed previously, has higher temperature rise. The top sides of both eGaN FETs die show higher temperature which are 109.85°C (383K) and 119.75°C (392.9K). Thus the doube-side cooling of eGaN FETs can be used for high power applications [90].



(a) Input voltage 25V

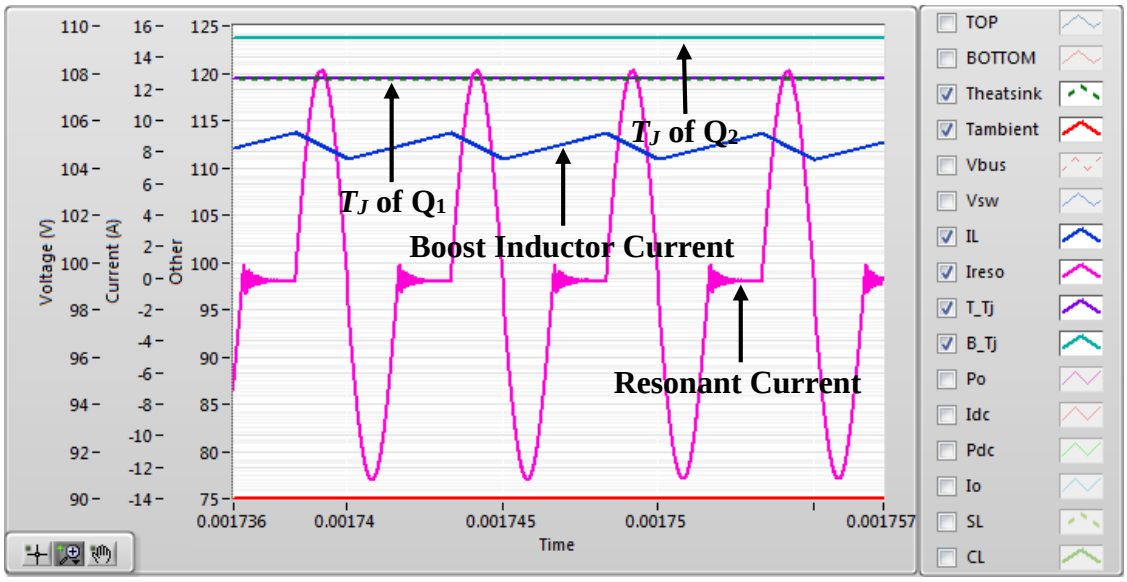


(b) Input voltage 50V

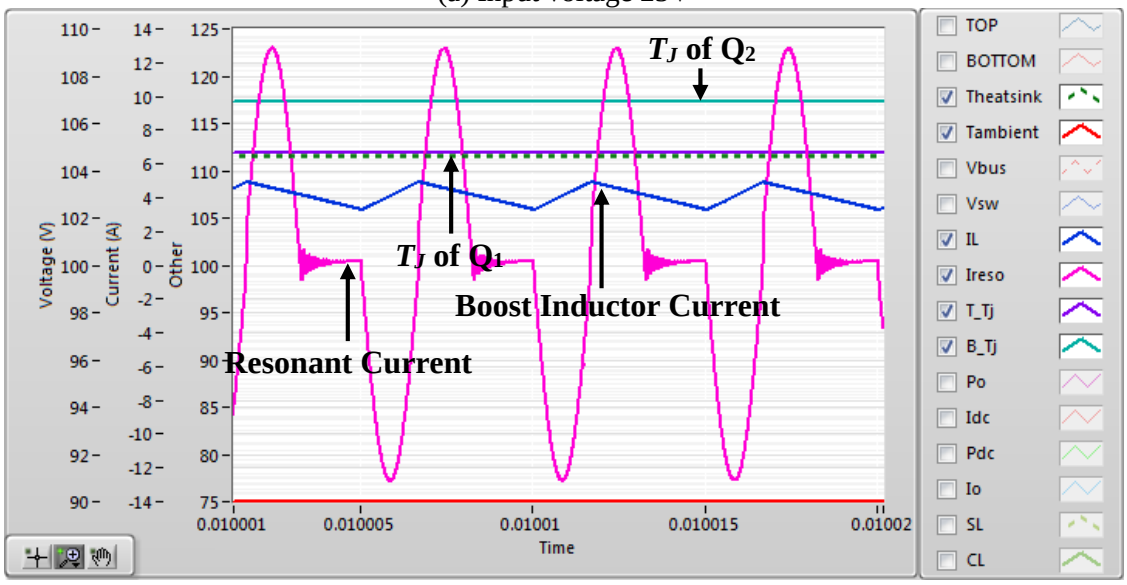
Figure 2.16: Simulation results of the thermal model in Multisim and LabVIEW co-simulation (ambient temperature 100°C and thermal resistance 16.4495°C/W).

The thermal model of power devices in Multisim provides an efficient method to accurately decide the thermal behaviors and explore the thermal effect of power electronic circuits. With the electrical specifications, thermal SPICE model [91] and calculated

power losses, the detailed thermal model of eGaN FETs EPC2001 in Multisim can be obtained [92]. In terms of that, a thermal model simulation of eGaN FETs based front-end resonant dc-dc converter was built up with Multisim and LabVIEW co-simulation to evaluate the temperature rise of eGaN FETs at different thermal resistances, ambient temperatures and output powers. From Figure 2.16(a), it is indicated that when eGaN FETs in the proposed topology operate at 25V input voltage, 100°C ambient temperature and 16.4495°C/W thermal resistance, the steady state junction temperatures of Q_1 and Q_2 are 102.54°C and 114.07°C respectively, which limits the junction temperature to below 125°C. In Figure 2.16(b), while increasing the input voltage to 50V, the steady state junction temperatures of Q_1 and Q_2 reduce to 100.21°C and 104.75°C. At the same time, it is also observed that the temperature of PCB (identified as Theatsink) in Figure 2.16(a) is a little bit higher than that in Figure 2.16(b), but both of them are close to the ambient temperature which is in accordance with FEA result in Figure 2.15. Likewise, Figure 2.17(a) shows the steady state junction temperature of Q_1 (119.36°C) and Q_2 (123.68°C) while operating at 25V input voltage, 75°C ambient temperature and 32.899°C/W thermal resistance. With 50V input voltage, the steady state junction temperature of Q_1 and Q_2 are 111.83°C and 117.25°C as shown in Figure 2.17(b). In addition, the temperature of PCB is higher than the ambient temperature and close to that of Q_1.



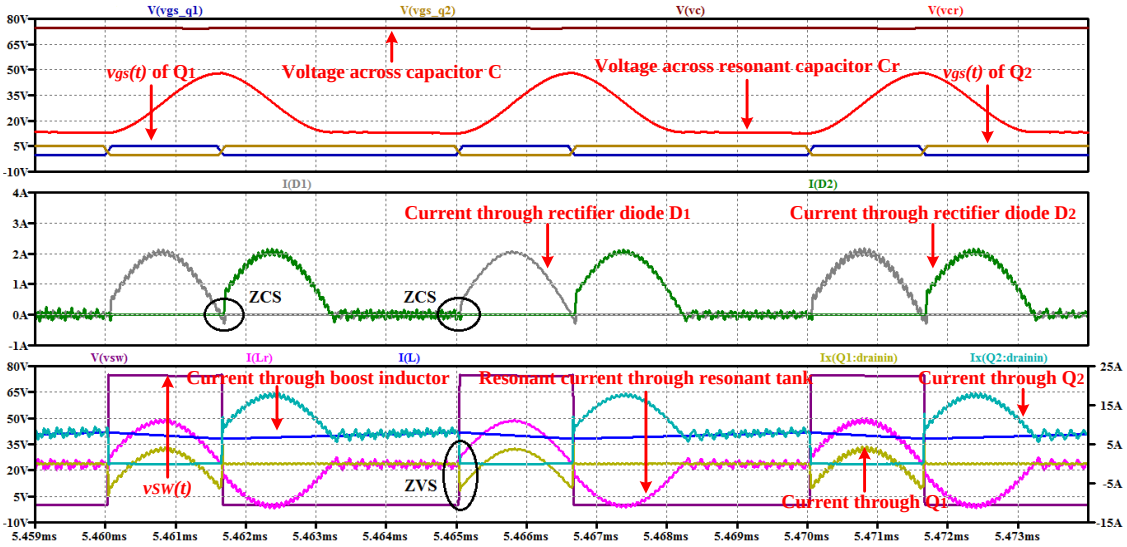
(a) Input voltage 25V



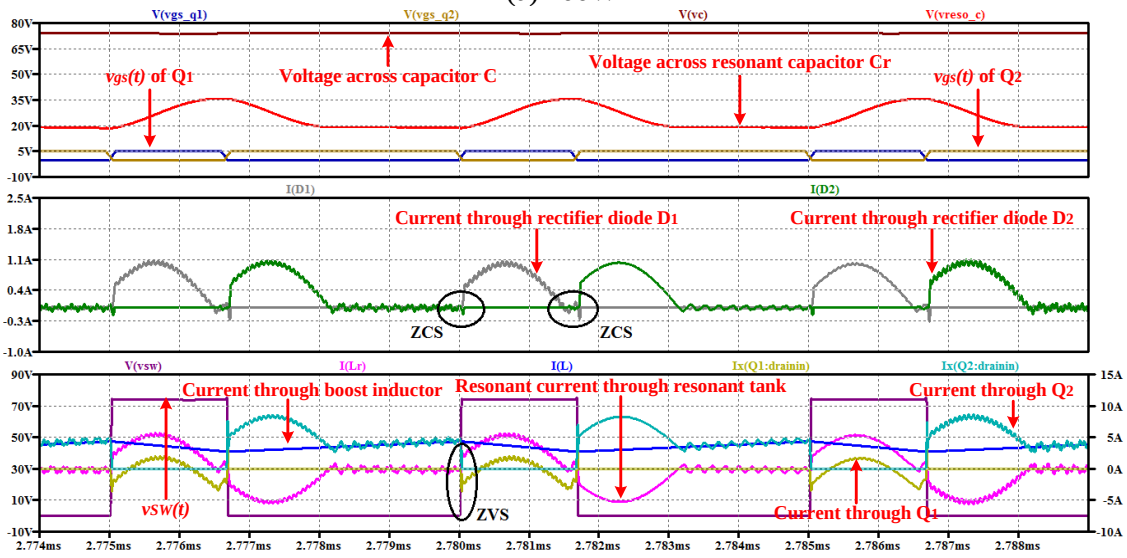
(b) Input voltage 50V

Figure 2.17: Simulation results of the thermal model in Multisim and LabVIEW co-simulation (ambient temperature 75°C and thermal resistance 32.899°C/W).

2.6 Simulation and experimental results



(a) 200W

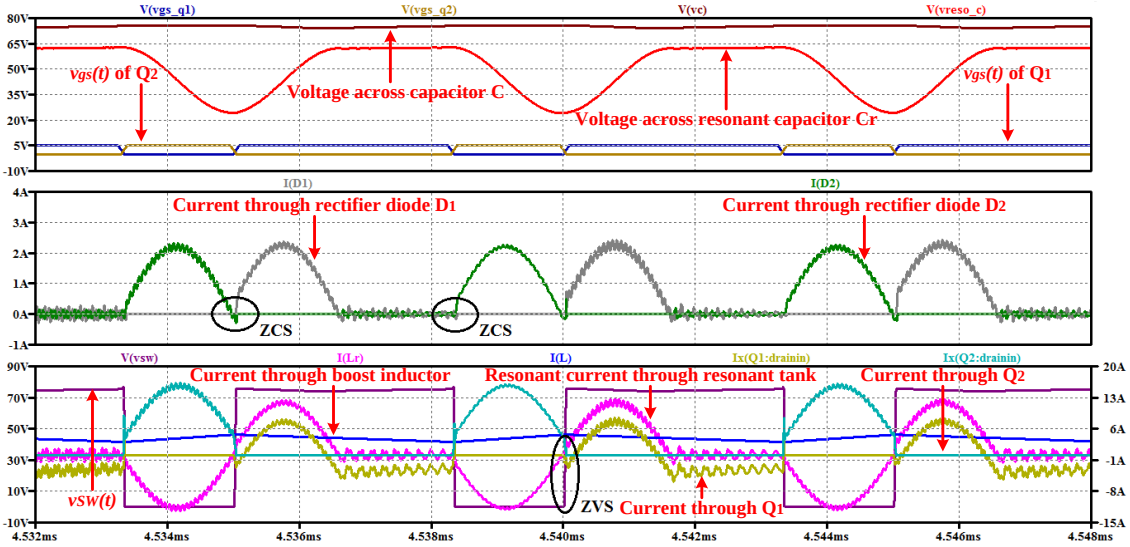


(b) 100W

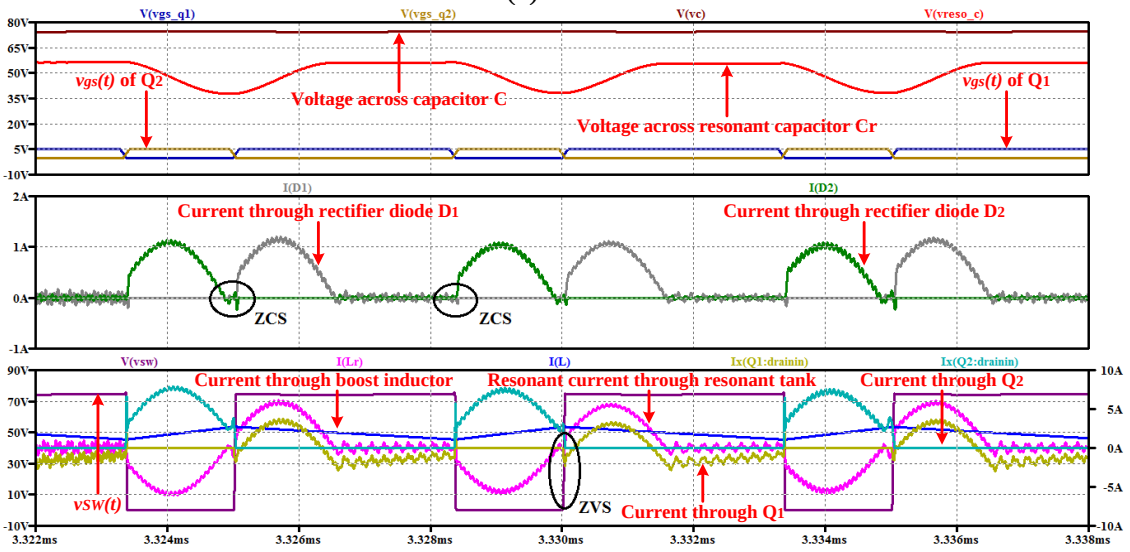
Figure 2.18: Simulation results of proposed front-end resonant dc-dc converter operating at 25V input voltage.

To verify the effectiveness of the proposed front-end resonant dc-dc converter, first a simulation model based on EPC2001 SPICE model is built up in LTspice. Figure

2.18 shows the simulation results while operating at 25V input voltage where it is observed that ZVS of Q_1 and ZCS of D_1 and D_2 can be always achieved as expected. The resonant periods are very close to the conduction moments of Q_1 to minimize the peak value of resonant current. The simulation results at 50V input voltage are shown in Figure 2.19 where it is observed that the voltage across capacitor C is almost constant and there is no



(a) 200W



(b) 100W

Figure 2.19: Simulation results of proposed eGaN FETs based front-end resonant dc-dc converter operating at 50V input voltage.

Table 2-3: Electrical specifications of proposed eGaN FETs based front-end resonant dc-dc converter.

Switching Frequency (kHz)	200	Turn Ratio	6:32
Input Voltage (V)	25~50	Resonant Inductor (nH)	450
Output Voltage (V)	400	Resonant Capacitor (nF)	470
Duty Ratio	1/3~2/3	Capacitor C (uF)	4.7
eGaN FETs	EPC2001	Rectifier Diodes	HFA04SD60S
Boost Inductor	50uH	PQ32/20 ferrite core PC 98	
High Frequency Transformer		PQ32/20 ferrite core PC 95	

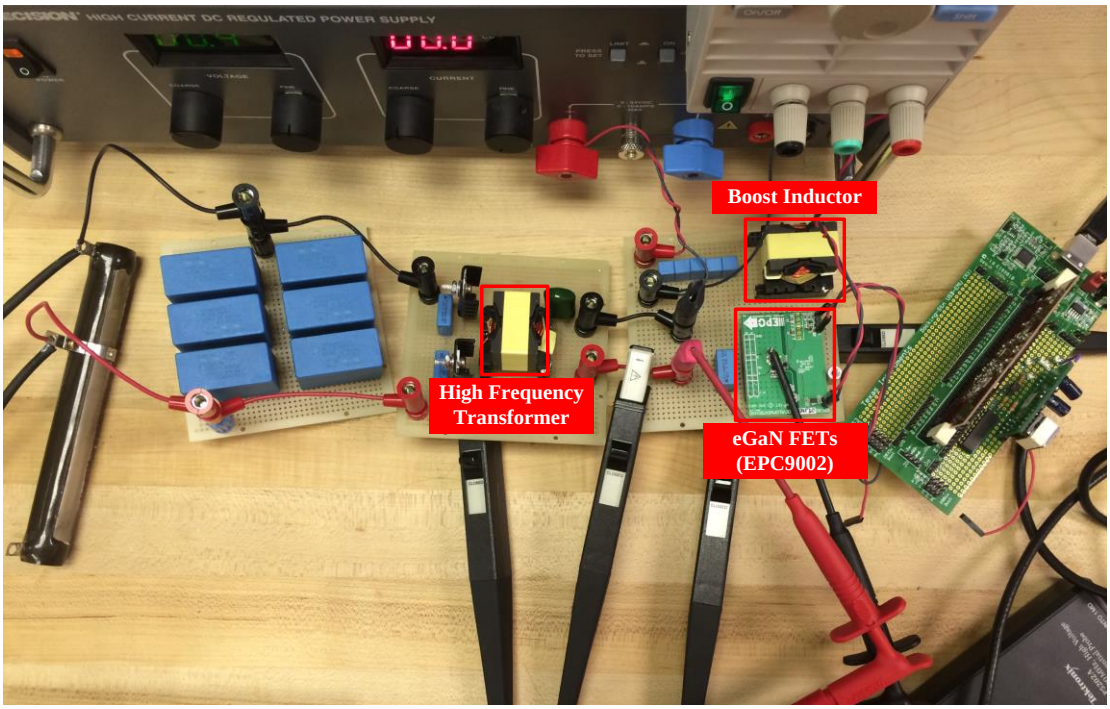
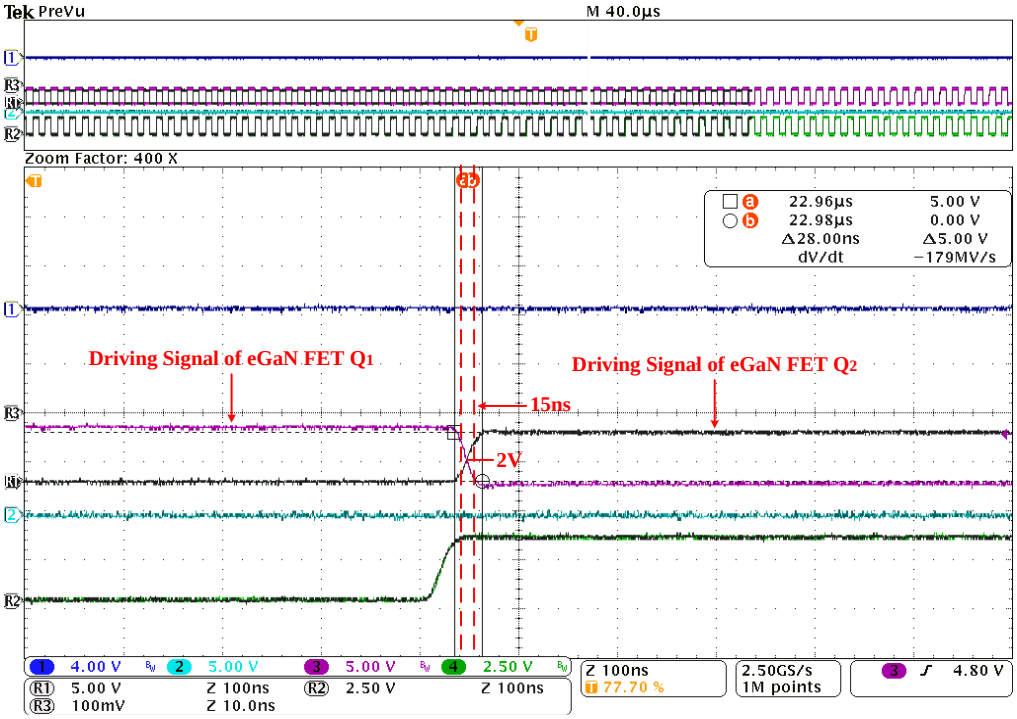
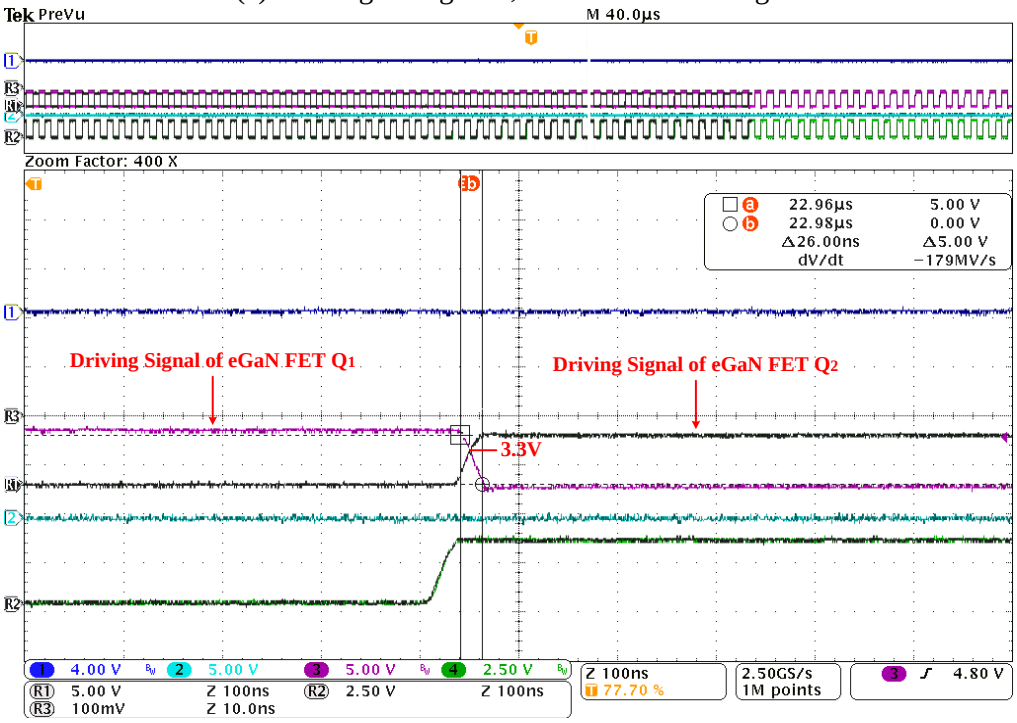


Figure 2.20: Experimental setup of proposed eGaN FETs based front-end resonant dc-dc converter.

circulating current in the resonant tank beyond resonant periods. Likewise, the resonant periods are close to the conduction moments of Q_1 to minimize the peak resonant current.

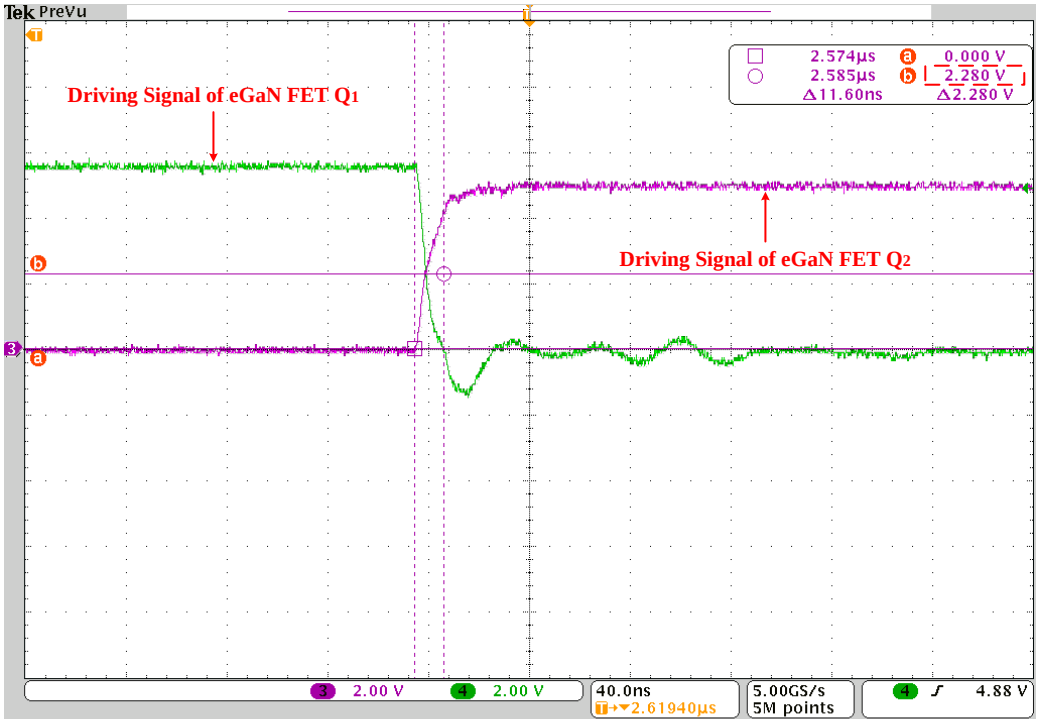


(a) crossing voltage 2V, without shoot through

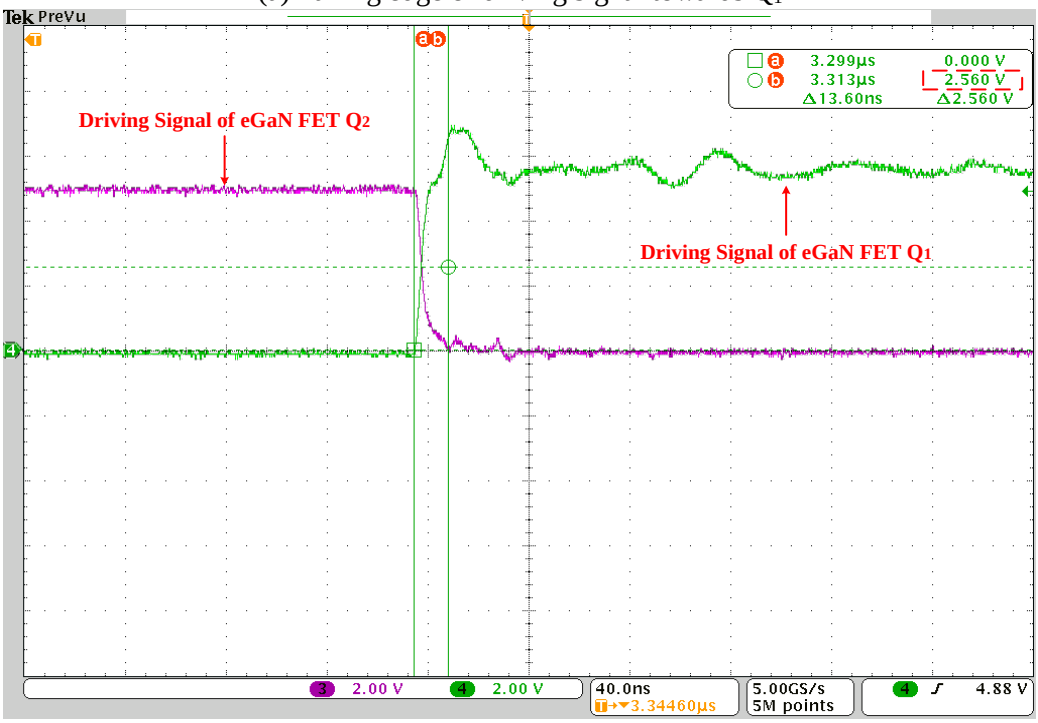


(b) crossing voltage 3.3V, shoot-through

Figure 2.21: Experimental waveforms of proposed overlapped driving signals at 200kHz switching frequency.



(a) Falling edge of driving signal towards Q_1

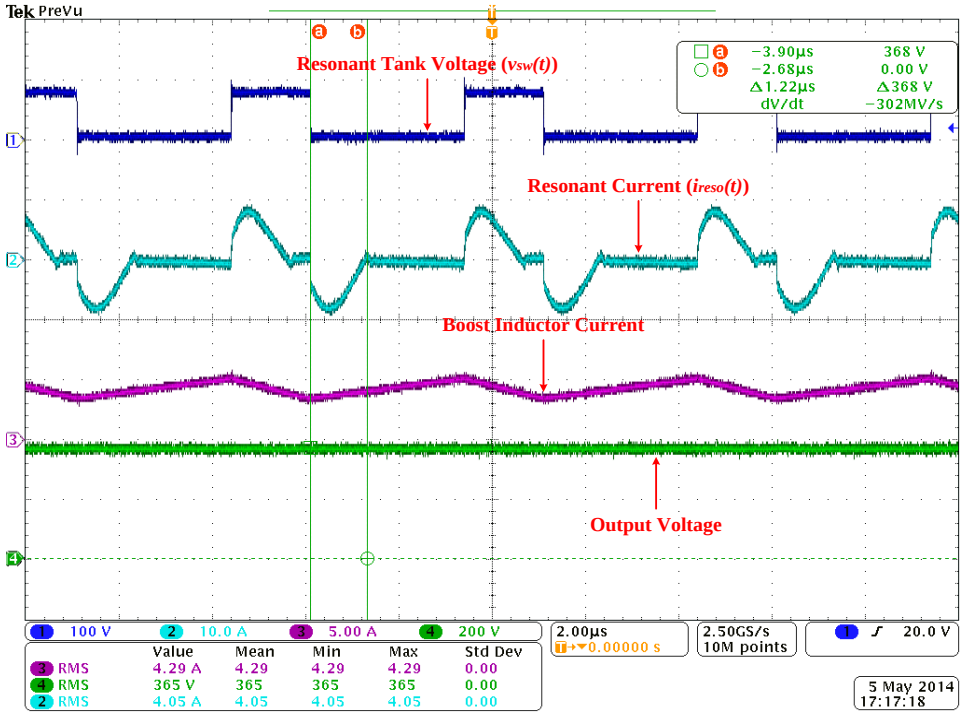


(b) Rising edge of driving signal towards Q_1

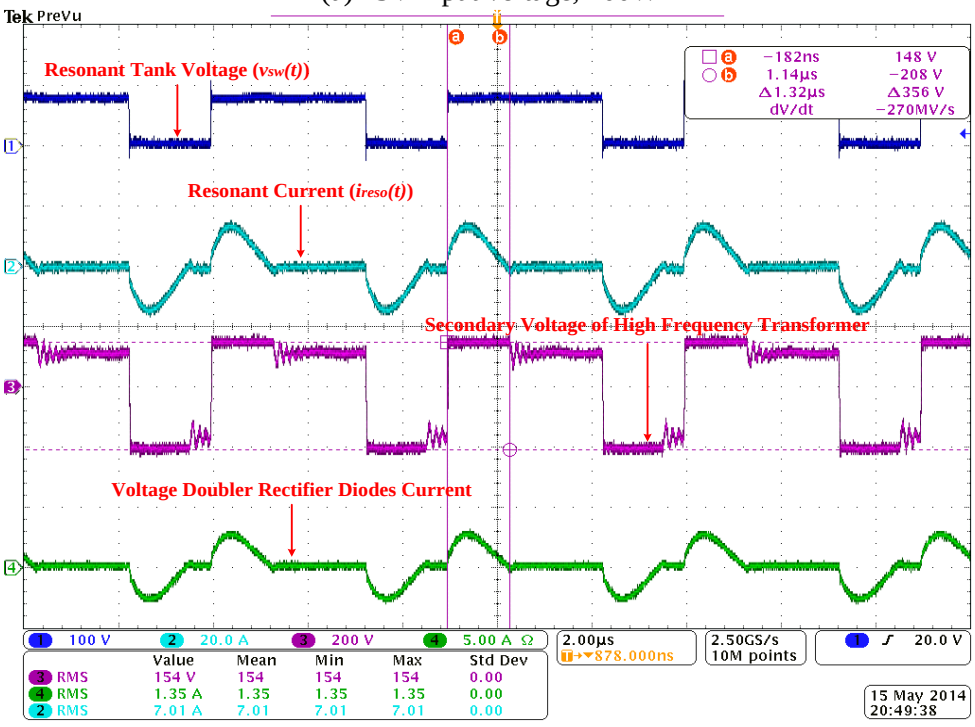
Figure 2.22: Experimental waveforms of proposed overlapped driving signals at 500kHz switching frequency.

Table 2.3 indicates the electrical specifications of the eGaN FETs based front-end resonant dc-dc converter and a 200W experimental setup is built up as shown in Figure 2.20 where EPC9002 evaluation board is used to configure the main power devices with driving circuits integrated and TI TMS320F28335 is applied to achieve duty ratio control digitally. The experimental waveforms of the proposed overlapped drving signals at 200kHz switching frequency are shown in Figure 2.21. From Figure 2.21(a), it is observed that the crossing voltage of the overlapped drving signals in single phase leg is about 2V and the effective dead time is about 15ns. Thus, compared with conventional driving signals, $v_{sd}(t)$ can be reduced greatly without shoot-through current during dead time. However, in Fugure 2.21(b), the crossing voltage is about 3.3V ($V_{gs(th)max}$=2.5V, 25°C) and there is shoot-through current in the single phase leg. Therefore, for the proposed overlapped driving signals, it is important to choose appropriate crossing voltage to minimize the reverse conduction losses and avoid shoot-through current. In Figure 2.22, the switching frequency of the overlapped driving signals is increased to 500kHz and it is known that the crossing voltage of overlapped driving signals towards both rising and falling edges almost keep the same and there is only a little bit increase which are 2.28V and 2.56V respectively without shoot-through. Thus the switching frequency has limited influence on the crossing voltage of proposed overlapped driving signals, which, to some extent, verifies the feasibility of this method again.

Figure 2.23 shows the experimental waveforms of the proposed front-end resonant dc-dc converter where it is observed that voltage doubler rectifier diodes D_1 and D_2 operate with ZCS and there is no circulating current beyond resonant periods in the resonant tank.



(a) 25V input voltage, 100W



(b) 50V input voltage, 200W

Figure 2.23: Experimental waveforms of proposed eGaN FETs based front-end resonant dc-dc converter.

Due to the compact footprint of eGaN FETs EPC2001, it is impossible to measure the current through Q_1 directly and verify its ZVS turn-on. Thus an equivalent single phase leg using MOSFETs (FB59N10D) is built up to prove the ZVS turn-on of Q_1 as shown in Figure 2.24 where the negative current through Q_1 (marked by the red cycle) will discharge its C_{ds} first and allow Q_1 turn on with ZVS at the following moment.

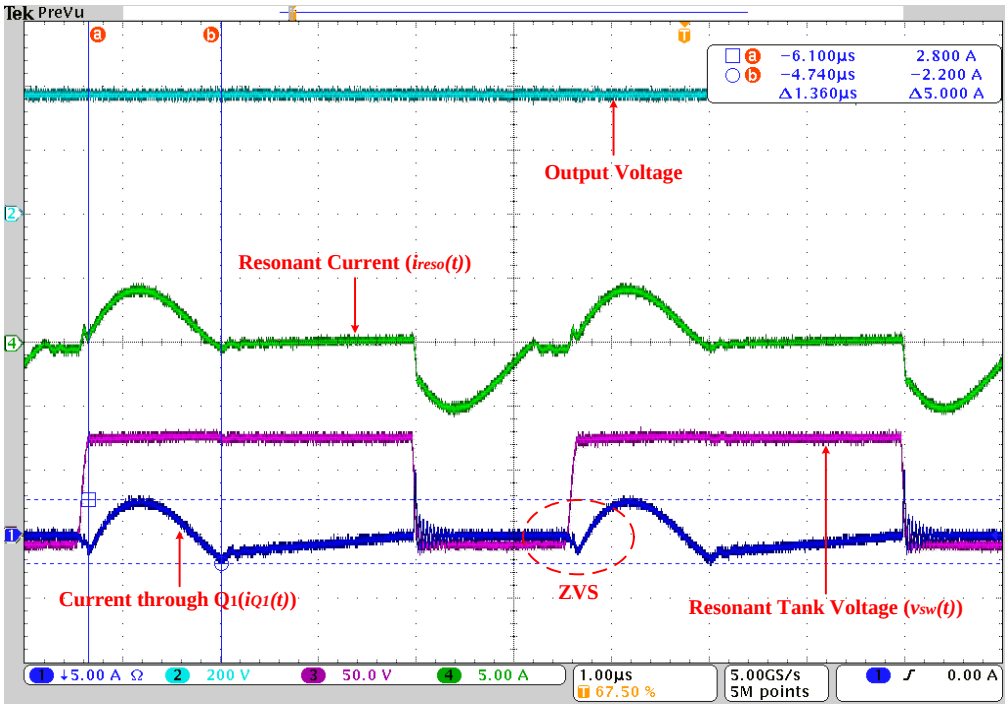


Figure 2.24: ZVS turn-on of Q_1 in proposed front-end dc-dc converter.

To further verify the validity of the efficiency improvement with the proposed overlapped driving signals, the measured efficiencies among eGaN FETs without overlapped driving signals, eGaN FETs with schottky diodes in parallel and eGaN FETs with overlapped driving signals are illustrated in Figure 2.25. From the efficiency curves, it is concluded that at both 25V and 50V input voltage, the method with the proposed

overlapped driving signals shows higher efficiency (about up to 0.7 percentage points efficiency increase) than that without overlapped driving signals from 50W to 200W. Finally, the experimental waveforms of MPPT algorithm in this proposed topology using solar simulator Magna-Power XR200 are illustrated in Figure 2.26. The maximum power points (MPP) in X-Y display during MPPT are shown in Figure 2.26(a). The dynamic performance of input current and input voltage during MPPT are shown in Figure 2.26(b). The *p-v* curve and remote sensed MPP from the instrument are shown in Figure 2.26(c). From those, it is observed that the MPPT algorithm can track the MPP of solar emulator effectively.

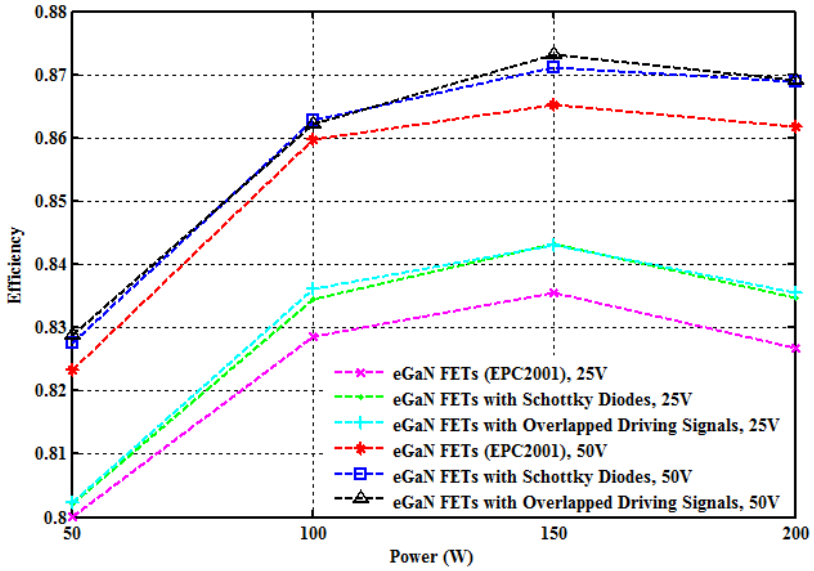
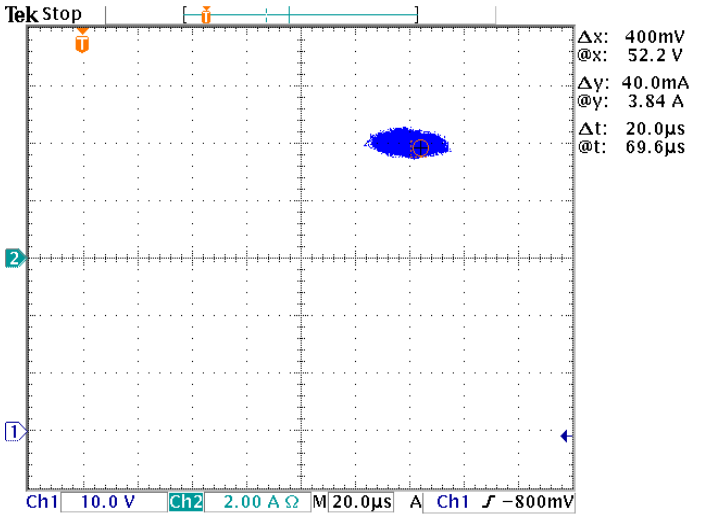
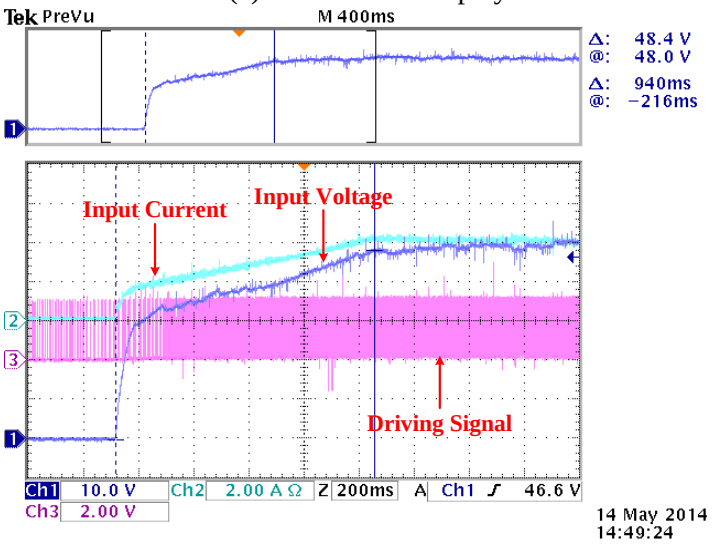


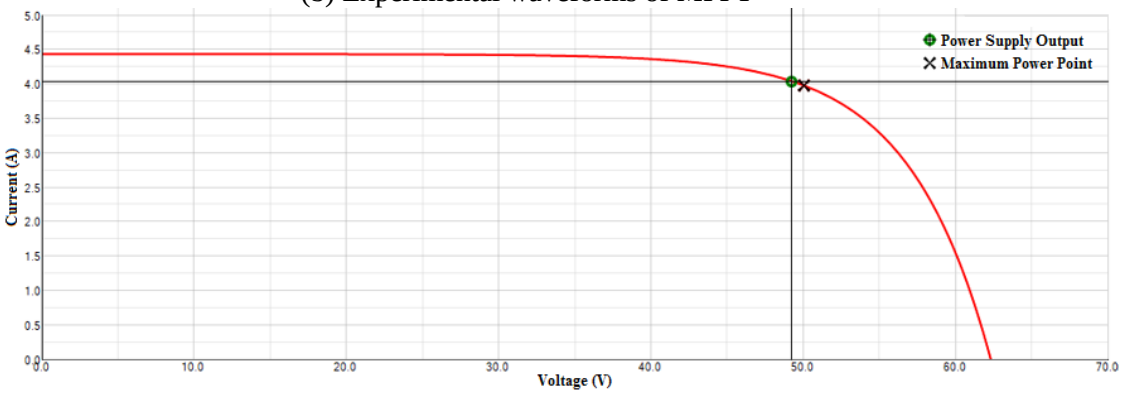
Figure 2.25: Measured efficiency comparison among eGaN FETs without overlapped driving signals, eGaN FETs with schottky diodes in parallel and eGaN FETs with overlapped driving signals.



(a) MPP in X-Y display



(b) Experimental waveforms of MPPT



(c) *v-i* curve of MPPT algorithm

Figure 2.26: Experimental waveforms of MPPT in the proposed eGaN FETs based front-end resonant dc-dc converter.

2.7 Summary

This section presents eGaN FETs based high step-up front-end resonant dc-dc converter with simple topology, less power devices counts, easy-to-implement duty ratio control strategy. ZVS of Q_1, conditional ZVS of Q_2 and ZCS of voltage doubler rectifier diodes D_1 and D_2 are verified by theoretical analysis, simulation and experimental results. To satisfy the requirements of extended ZVS of Q_2, reduced input current ripple and high power applications, the interleaved topology is suggested and the validity is demonstrated by simulation results.

The reverse conduction characteristics and thermal performance of eGaN FETs are investigated in detail. The overlapped driving signals are proposed to reduce $v_{sd}(t)$ and reverse conduction power losses during dead time in single phase leg structure. Compared with the method with schottly diodes in parallel, no additional components are needed. Through efficiency measurement, the method with the proposed overlapped driving signals shows higher efficiency (about up to 0.7 percentage points efficiency increase) than that without overlapped driving signals from 50W to 200W. To optimize reverse conduction performance and avoid shoot-through current, the crossing voltage of the overlapped driving signals should be chosen appropriately. Combined with FEA thermal analysis and thermal model simulation, the equivalent thermal resistor model provides a simplified process to evaluate the cooling requirements and ensure effective heat dissipation for eGaN FETs.

3. DOUBLE LINE FREQUENCY POWER DECOUPLING TECHNIQUES

3.1 Introduction

Single phase inverters are inherently subject to the double line frequency ripple power which not only results in three-order harmonics in ac side, but also can potentially influence the MPPT efficiency of PV module [93] or thermal performance of fuel cell [94, 95]. To solve this problem, it is necessary to have energy storage components to decouple the double line frequency ripple power, which act as a buffer to balance the difference of the instantaneous power. Thus the passive approach using bulky electrolytic capacitors or inductors can be an effective solution. But both of them will lead to low efficiency and low power density [96]. Even the electrolytic capacitors have the drawback of short lifetime and low reliability especially at high temperatures. An alternative approach on mitigating the ripple power is to use active power decoupling technqiues [63, 97]. In that case, the double line frequency ripple power will be transferred to other energy storage components that have low inductance and capacitance, by introducing active/passive circuits and advanced control or modulation strategies.

For the two stage PV microinverters, since the dc bus voltage is high, the film capacitors with low capacitance can be used to buffer the double line frequency ripple power without the additional power decoupling circuits. The degradation of MPPT efficiency and the distortion of grid current, resulting from high dc bus voltage ripple, can be compensated through advanced control strategies that are capable of high double line frequency ripple rejection [98]. Another type of active power decoupling techniques can

be generally divided into parallel and series active power decoupling in terms of the ripple power paths as shown in Figure 3.1, where the additional ripple ports are needed to buffer the ripple power. [99] and [100] proposed series active power decoupling for voltage source and current source topologies respectively. By connecting an independently controlled voltage compensator in series with the dc and ripple source, the ripple voltage can be compensated by power devices and capacitors with low voltage ratings, and the capacitance of dc bus capacitor can be reduced. However, the increased component counts limit their applications in PV microinverters. [101-103] introduced parallel active power decoupling with capacitor as energy storage component. Even though no extra power devices is needed, the coupling between the main and power decoupling circuit reduces the dc voltage utilization and potentially means higher voltage gain for the front-end dc-dc converter to satisfy the requirements of grid connection. [104-107] presented parallel active power decoupling with one or two single phase legs added, where both capacitor and inductor can be the energy storage component, and the additional power devices can be modulated independently or dependently to buffer the double line frequency ripple power. Some other active power decoupling techniques like six-switch power decoupling [108, 109], ac-link power decoupling [110], decoupling using the center tap of isolated transformer [111], and power decoupling using active buffer [112], etc. are included in the literatures for different applications [113-116]. Furthermore, by replacing the current-bidirectional two-quadrant switches with the voltage-bidirectional two-quadrant ones, similar power decoupling technqiues can be applied in current source inverter [117, 118]. Figure 3.1 summarizes all existing active power decoupling techniques until 2015. From

that, it is known that even though there are different topologies, control or modulation strategies, waveforms of energy storage components and ripple power paths, etc., the general solutions based on power decoupling principle should be satisfied. At the same time, for the two stage PV microinverters, some of them show better performance than others. Thus, in this section, the general solutions to achieve power decoupling will be derived and discussed in detail first. Based on that, the investigations on existing power decoupling techniques will be included. Finally the evaluations on component counts, energy utilization and voltage/current ripple of energy storage components, dc voltage utilizations of both the main and power decoupling circuit, and current stresses of power devices in the main circuit, will provide helpful guidance on the design of power decoupling in the two stage PV microinverters.

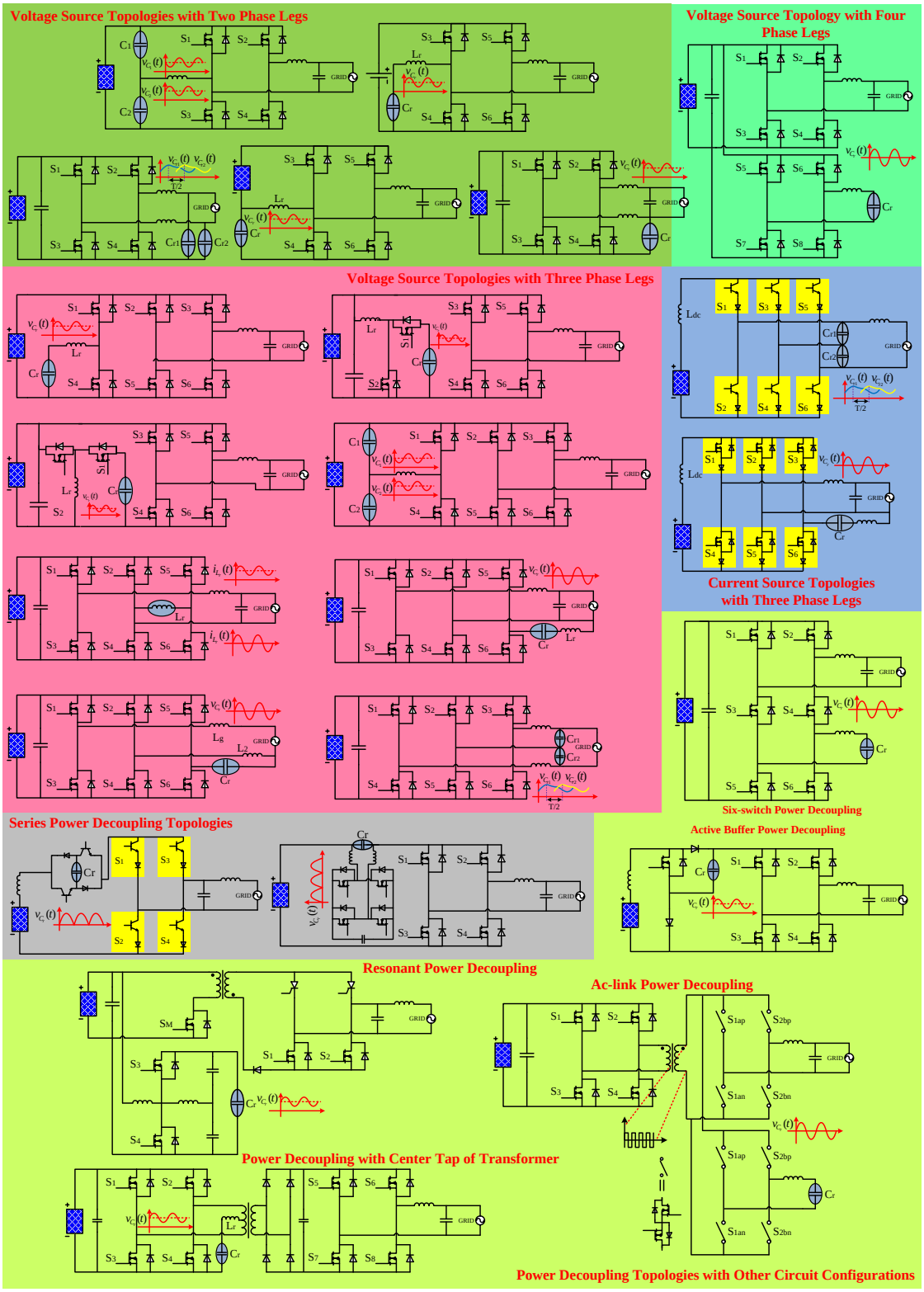


Figure 3.1: Summary of active power decoupling techniques.

3.2 General solutions on power decoupling

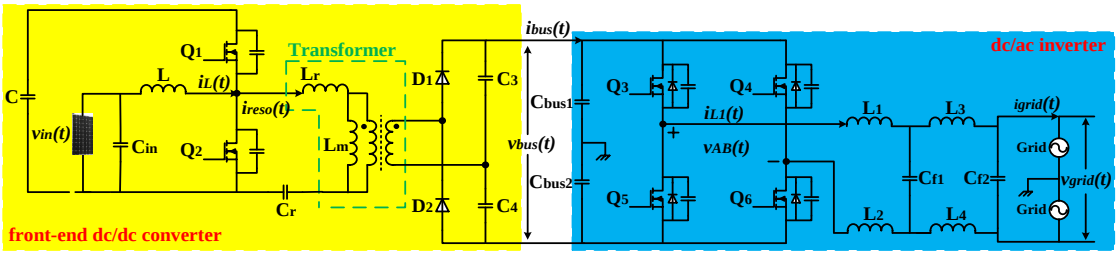


Figure 3.2: Configuration of the proposed two stage PV microinverter.

The configuration of proposed two stage PV microinverter is shown in Figure 3.2 where the first stage is eGaN FETs based resonant dc-dc converter discussed in previous section and the second stage is H-bridge dc-ac inverter that will be explored in the following section. $v_{bus}(t)$ is the dc bus voltage and generally, there are large electrolytic capacitor (C_{bus1} and C_{bus2} in this figure) across dc bus to buffer the double line frequency ripple power as shown in (3.1) below.

$$C_{bus} = \frac{P_{grid}}{\omega \cdot V_{bus} \cdot \Delta V_{bus}} \tag{3.1}$$

where ΔV_{bus} is the allowed voltage ripple across dc bus. It is assumed that the grid side voltage and current can be expressed as the following equations:

$$v_{grid}(t) = \sqrt{2} V_{grid} \sin(\omega t) \tag{3.2}$$

$$i_{grid}(t) = \sqrt{2} I_{grid} \sin(\omega t + \varphi) \tag{3.3}$$

where, V_{grid} and I_{grid} are the RMS value of grid voltage and current respectively. φ is the phase difference between voltage and current at ac side. Thus the instantaneous power at grid side can be calculated below.

$$p_{grid}(t) = v_{grid}(t) \cdot i_{grid}(t) = V_{grid} I_{grid} \cos\varphi - V_{grid} I_{grid} \cos(2\omega t + \varphi) \tag{3.4}$$

In the two stage PV microinverters, sicne the instant power of output filter is normally less than 1/10 of that from the grid side, it can be neglected to simplify the analysis. Thus the instant power at dc bus, without considering the power losses, can be expressed as:

$$p_{bus}(t) = p_{grid}(t) = P_{cons} + p_r(t) \tag{3.5}$$

From (3.5), it is observed that the instantaneous power at dc bus consists of two terms: a constant power P_{cons} which feeds the dc power, and a double line frequency ripple power $p_r(t)$ which must be decoupled by energy storage components, as shown in Figure 3.3.

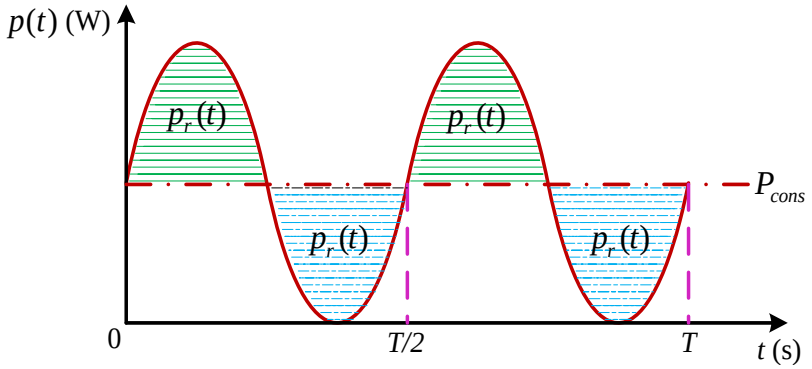


Figure 3.3: Instantaneous power between dc bus and grid side in single phase inverters.

Given the high power density and light weight of PV microinverters, capacitors are usually used as energy storage component rather than inductors. Thus the following equation should be satisfied to achieve power decoupling.

$$p_{Cr}(t) = v_{Cr}(t) \cdot i_{Cr}(t) = \frac{1}{2} C_r \frac{d(v_{Cr}(t)^2 + A)}{dt} = p_r(t) \tag{3.6}$$

where A is a time-constant value. $v_{Cr}(t)$ and $i_{Cr}(t)$ are the voltage and current of energy storage capacitors. By solving the differential equation above and doing Fourier analysis on $v_{Cr}(t)$, it is found that the complete solution on the voltage across C_r can contain different orders frequency components as shown below.

$$|v_{Cr}(t)| = A_0 + \sum_{k=1}^{n} A_k \sin(k\omega t + \theta_k) \tag{3.7}$$

where n =1, 2, 3, etc.. To decouple the double line frequency ripple power in (3.4) and (3.5) completely and minimize the involved other frequency ripple powers, there are three general solutions on the voltage across energy storage capacitors as shown in Figure 3.4: i) A_k=0 and k≠1, then $v_{Cr}(t) = A_1 \sin(\omega t + \theta_1)$; ii) A_k=0, k≠0, k≠2 and A_2<<A_1, then $v_{Cr}(t) = A_0 + A_2 \sin(2\omega t + \theta_2)$; iii) A_k=0 and k≠1, then $v_{Cr}(t) = |A_1 \sin(\omega t + \theta_1)|$.

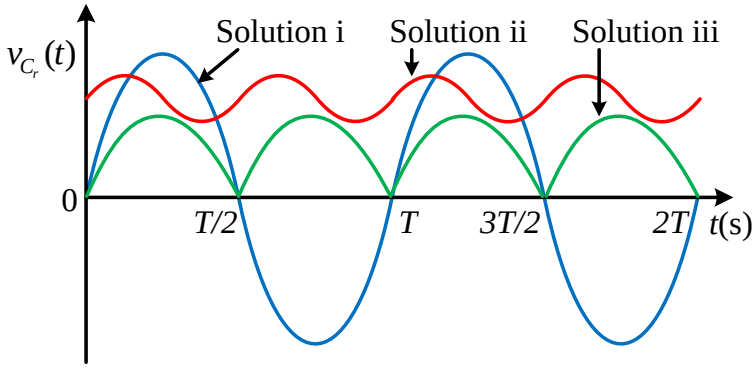


Figure 3.4: Three solutions on the voltage across energy storage capacitors.

For Solution i, it is observed that the voltage across energy storage capacitors is line frequency sinusoidal waveform without dc offset. If the energy utilization efficiency η_E is defined to be the ratio of double line frequency ripple energy to the maximum energy stored in energy storage capacitors, it will be 1 which represents complete utilization of

energy storage capacitors. Similarly, if the voltage ripple factor η_r is defined to be the ratio of voltage ripple to the peak value of voltage across energy storage capacitors, it is also 1 which means the energy storage capacitors are fully charged and discharged. For Solution ii, it is observed that the voltage across energy storage capacitors is double line frequency sinusoidal waveform with dc offset. Through (3.6) and (3.7), it is known that there will be undesired fourth-order line frequency power from energy storage capacitors which, to some extent, violates the theoretical derived power decoupling requirement. To minimize the fourth-order line frequency component, A_2 should be small enough and A_0 should be large enough to satisfy the requirement of power decoupling. Thus, compared with that in Solution i, larger voltage ratings of energy storage capacitors are needed. At the same time, according to the definition of η_E and η_r above, the following equations should be satisfied.

$$\eta_E = \eta_r (1 - \eta_r) \tag{3.8}$$

$$\eta_r = \frac{2A_2}{A_0 + A_2} \leq 1 \tag{3.9}$$

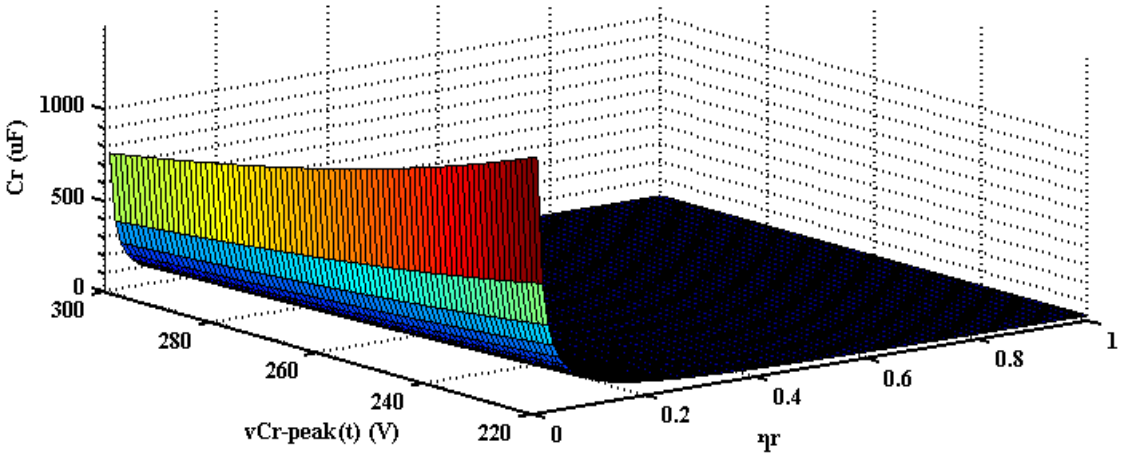
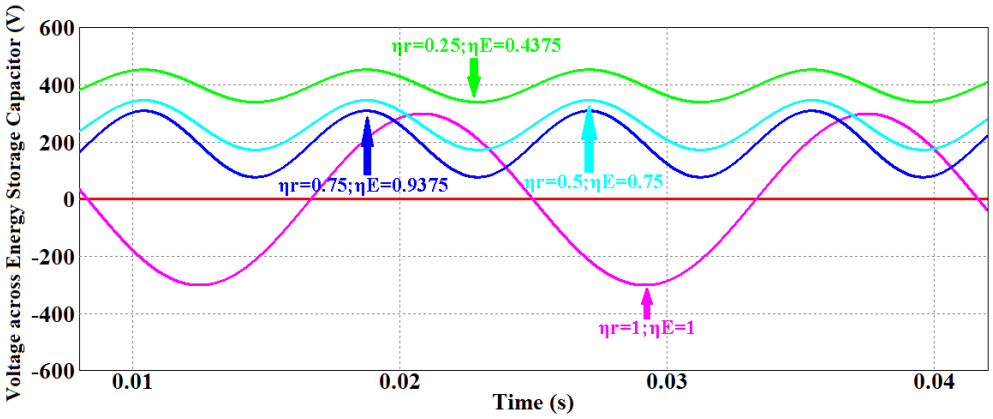
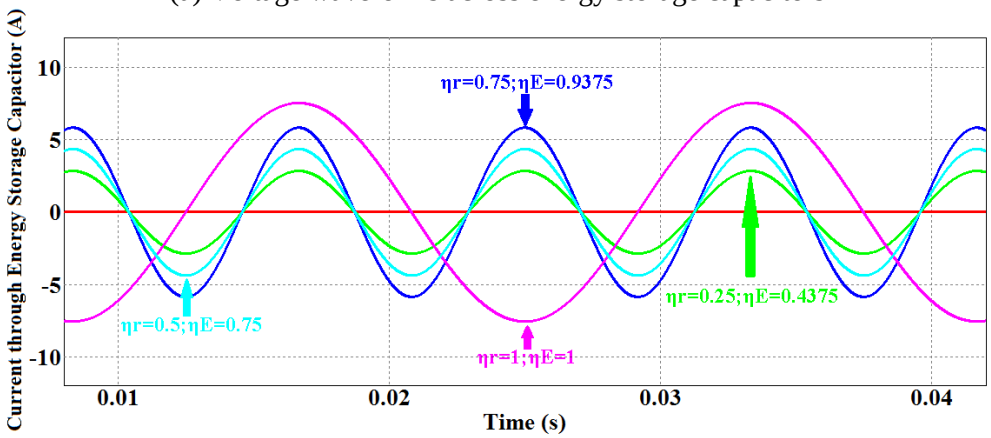


Figure 3.5: Relationships among energy storage capacitance, peak voltage across energy storage capacitor and voltage ripple factor.



(a) Voltage waveforms across energy storage capacitors



(b) Current waveforms through energy storage capacitors

Figure 3.6: Voltage and current wavefroms of energy storage capacitors with different different energy utilization efficiency η_E and voltage ripple factor η_r.

$$A_0 + A_2 = \sqrt{\frac{P_r(2-\eta_r)}{2\omega C_r \eta_r}} + \sqrt{\frac{P_r \eta_r}{2\omega C_r (2-\eta_r)}} = \sqrt{\frac{2P_r}{\omega C_r \eta_r (2-\eta_r)}} \tag{3.10}$$

where P_r is the peak value of the double line frequency ripple power. Combined with the condition of Solution ii mentioned previously, it is revealed that η_r should be much less than 1 to minimize the fourth-order frequency ripple power, which, to some extent, limits the minimum value of energy storage capacitance as illustrated in Figure 3.5. At the same time, from (3.8) and (3.10) smaller η_r also represents low energy utilization efficiency η_E and there is always tradeoff between the energy storage capacitance and the peak

voltage across C_r. For Solution iii, the voltage across energy storage capacitors behaves like full-wave rectified line frequency sinusoidal waveform. Similar to Solution i, since the energy storage capacitors are fully charged and discharged, and completely utilized, both η_r and η_E can be regarded as 1.

Figure 3.6 provides the voltage and current waveforms of energy storage capacitor with different energy utilization efficiency η_E and voltage ripple factor η_r where it is assumed that the double line frequency ripple power and the energy storage capacitance keep constant. Through them, it is concluded that 1) smaller η_r means larger peak voltage across energy storage capacitors and lower current through energy storage capacitors; 2) with the increase of η_E, the voltage ripple increases and the dc offset decreases as expected. High η_E leads to higher current through energy storage capacitors.

3.3 Investigations on power decoupling techniques

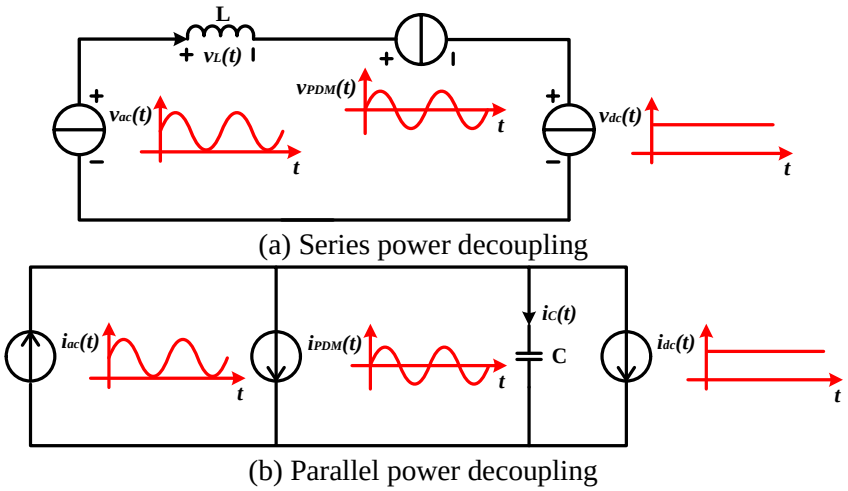


Figure 3.7: Power decoupling with different ripple power paths.

Based on the principle of power decoupling, there is always a ripple power path to transfer the double line frequency ripple power to other energy storage components with lower inductance or capacitance. By considering the ripple power paths, the active power decoupling techniques can be divided into series and parallel one respectively. In theory, to eliminate the double line frequency ripple voltage, a voltage source can be in series with the ripple source and the desired dc source to compensate the instantaneous voltage imbalance as illustrated in Figure 3.7(a). Likewise, a current source can be in parallel with the ripple source and the desired dc source to compensate the instantaneous current imbalance and then eliminate the ripple current as shown in Figure 3.7(b). In terms of the series active power decoupling in the two stage PV microinverters, an active ripple port, consisting of power devices and film capacitors, can be connected between the front-end dc-dc converter and the dc-ac inverter to achieve power decoupling with independent

modulation and control schemes. For the parallel active power decoupling, since the conventional half-bridge structure is still the basic unit in dc-ac inverter, the ripple power can be always decoupled through the general configuration in Figure 3.8 below.

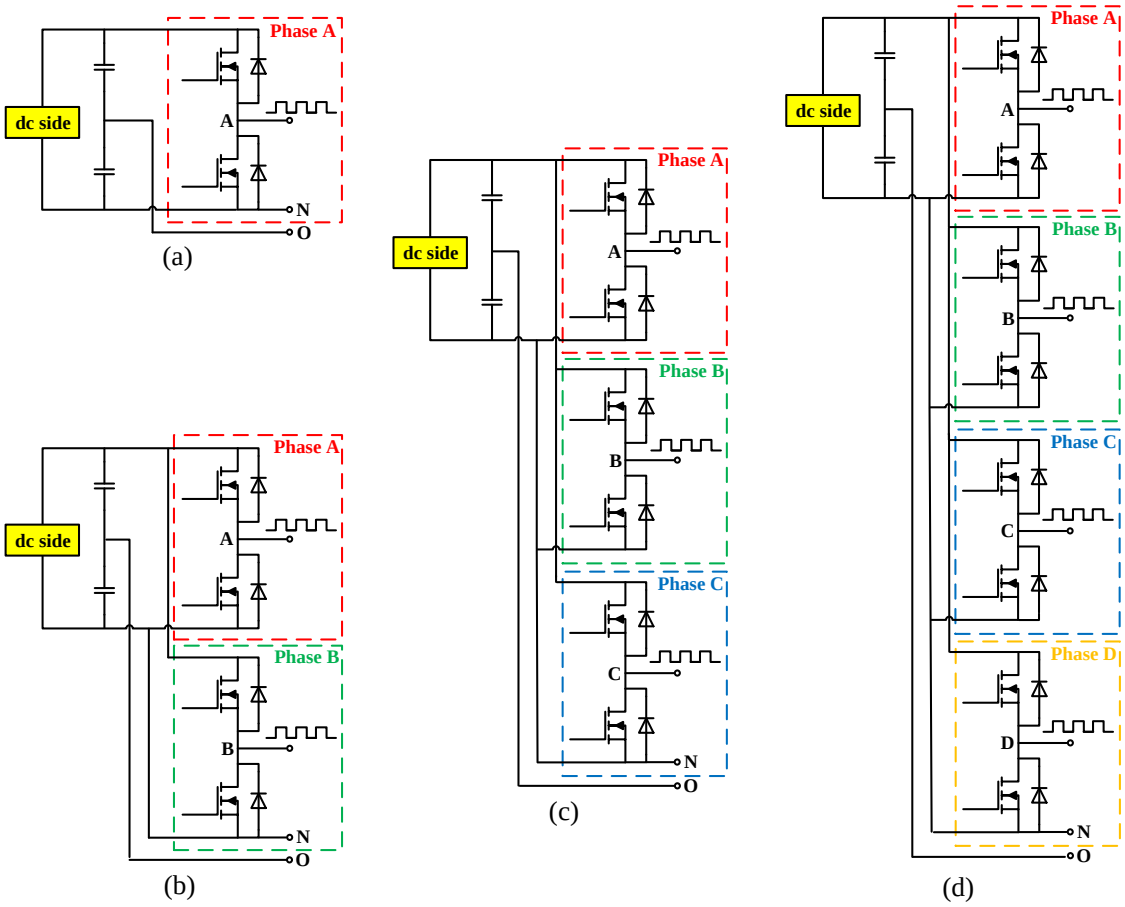


Figure 3.8: General configuration of parallel power decoupling in the two stage PV microinverters.

From Figure 3.8(a), it is observed that there is only one control objective can be achieved through the switch function of the single phase leg. Thus, to satisfy the requirements of both dc-ac inversion and power decoupling, at least two single phase legs are needed as shown in Figure 3.8(b). According to the general solutions on the voltage

across energy storage capacitors derived previously, both line frequency sinusoidal waveform with/without dc offset and double line frequency sinusoidal waveform with dc offset can be implemented through different connections of four possible ports A, B, O and N. However, since one single phase leg (phase B for example) is modulated to decouple the double line frequency ripple power, the dc voltage utilization for the main circuit (dc-ac inverter) is just 0.5 and behaves like half-bridge circuit, which potentially means doubled voltage gain for the front-end dc-dc converter to obtain desired dc bus voltage, and limits their applications in the two stage PV microinverters. By introducing another control objective, the power decoupling with three single phase legs in Figure 3.8(c) can achieve full dc voltage utilization of the main circuit and complete ripple power decoupling with either independent or dependent modulation strategies. For independent modulation, the single phase leg used for power decoupling is completely decoupled with the main circuit. Thus the dc voltage utilization for power decoupling circuit is just 0.5 and the current stresses of power devices in main circuit will keep the same. For dependent modulation, since at least one single phase leg will be shared by both the main and power decoupling circuit, the current stresses of power devices in the shared single phase legs will be definitely changed. At the same time, the dc voltage utilization of both the main and power decoupling circuit will be related to the modulation strategies. The detailed evaluations will be included in the following parts. Of course, it is totally possible to add another single phase leg to configure H-bridge topology for both main circuit and power decoupling circuit with independent modulation as shown in Figure 3.8(d). But the

increased component counts only double the dc voltage utilization of power decoupling circuit and are not preferred in the two stage PV microinverters.

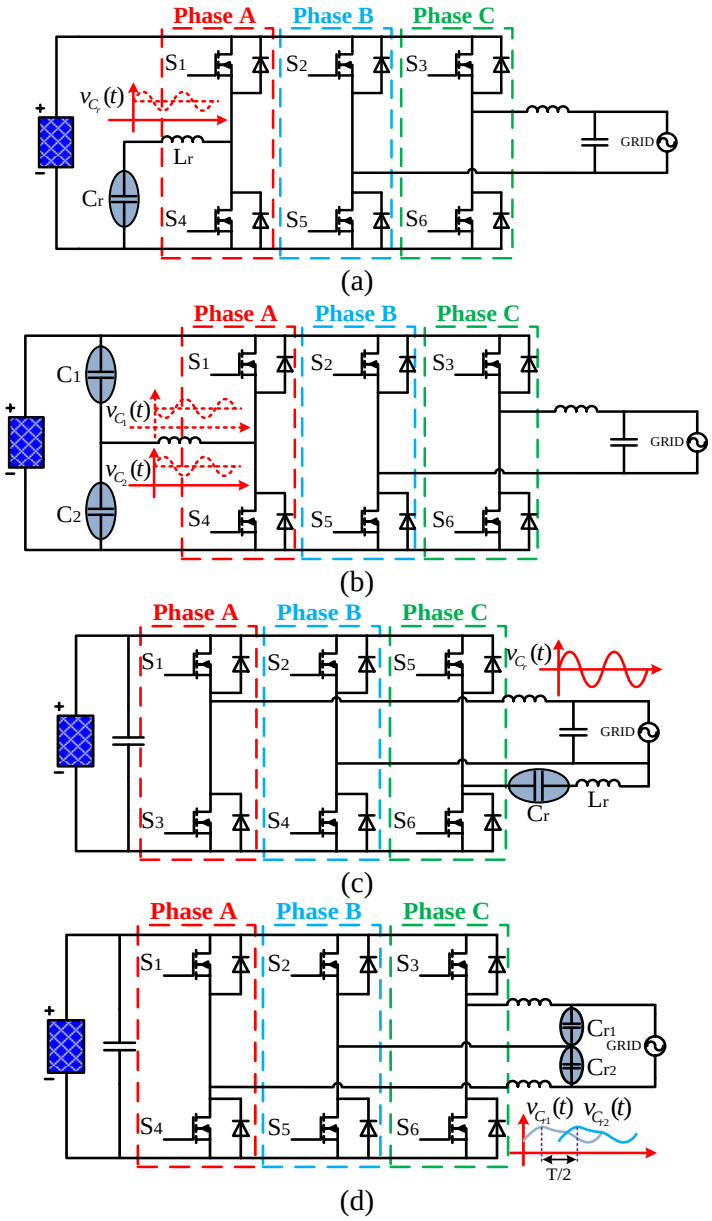


Figure 3.9: Main parallel power decoupling techniques for the two stage PV microinverters.

Generally, there are lots of active power decoupling technqiues for different applications as summarized in the introduction of this section. But for the two stage PV microinverters, given the requirements of high reliability, high efficiency, high power density, low component counts, small volumes and high voltage gain of the front-end dc-dc converter, only the techniques using film capacitor and advanced control strategies with high double line frequency ripple rejection capability in [98], and parallel power decoupling with three single phase legs can be better options [107, 119-121]. Figure 3.9 above shows the main parallel power decoupling techniques for the two stage PV microinverters.

For parallel active power decoupling with three single phase legs, at most three control objectives can be achieved through different connections among A, B, C, N and O. To maximize the dc voltage utilization of the main circuit and minimize the voltage gain of the front-end dc-dc converter, it is always desired to use two phases (phase A and B for example) to modulate the main circuit and obtain the full dc voltage utilization. Thus the modulation signals (m_A and m_B) of phase A and B can be expressed as $M\sin(\omega t+\varphi_{AB})$ and $-M\sin(\omega t+\varphi_{AB})$ respectively, where φ_{AB} represents the phase angle between the two phases. For the independent modulation, since phase C is decoupled with the main circuit completely, the modulation signal is decided by the voltage waveforms across energy storage capacitors from the general solutions as given by (3.11) and (3.12).

$$m(t)=\sqrt{\frac{2V_{grid}I_{grid}\cos\varphi}{\omega C_r\cos\theta_2}}\frac{\sqrt{\frac{2-\eta_r}{\eta_r}}+\sqrt{\frac{2-\eta_r}{\eta_r}}\sin(2\omega t+\theta_2)}{2V_{bus}}\quad\text{Solution ii}\qquad(3.11)$$

$$m(t) = \frac{0.5V_{bus} + A_1 \sin(\omega t + \theta_1)}{V_{bus}} \text{ Solution i} \tag{3.12}$$

For the dependent modulation, phase C is combined with either phase A or B to decouple the ripple power. Assuming that the voltage and current of energy storage capacitors can be expressed as:

$$v_{Cr}(t) = V_{Cr} \sin(\omega t + \theta_1) \tag{3.13}$$

$$i_{Cr}(t) = I_{Cr} \cos(\omega t + \theta_1) = \omega C_r V_{Cr} \cos(\omega t + \theta_1) \tag{3.14}$$

Then the peak values of $v_{Cr}(t)$ and $i_{Cr}(t)$ can be obtained below to meet the power decoupling requirements.

$$V_{Cr} = \sqrt{\frac{2V_{grid} I_{grid} \cos\varphi}{\omega C_r (1 - \omega^2 L_r C_r) \sin(2\theta_1)}} \tag{3.15}$$

$$I_{Cr} = \sqrt{\frac{2\omega C_r V_{grid} I_{grid} \cos\varphi}{(1 - \omega^2 L_r C_r) \sin(2\theta_1)}} \tag{3.16}$$

where $\theta_1 = \frac{1}{2}\arctan(\frac{\cos\varphi}{\sin\varphi})$ and L_r is the inductance of the smoothing inductor. Thus the phase angle between θ_1 and φ should satisfy the following relationship.

$$\theta_1 = \frac{\varphi}{2} + \frac{\pi}{4} \quad \text{or} \quad \theta_1 = \frac{\varphi}{2} - \frac{3\pi}{4} \tag{3.17}$$

Combined with the modulation signals of phase A and B, (3.13) and (3.14), the following equations can be derived.

$$v_{AB}(t) = v_{AO}(t) - v_{BO}(t) = V_{bus} M \sin(\omega t + \varphi_{AB}) = \sqrt{2} V_{grid} \sin\omega t \tag{3.18}$$

$$v_{CB}(t) = v_{CO}(t) - v_{BO}(t) = \frac{1}{2} V_{bus} M_C \sin(\omega t + \varepsilon) + \frac{1}{2} V_{bus} M \sin(\omega t + \varphi_{AB}) = V_{Cr}(1 - \omega^2 L_r C_r) \sin(\omega t + \theta_1) \tag{3.19}$$

where ε is the phase angle of modulation signal on phase C. Then the modulation index of phase C can be obtained by:

$$M_C = \frac{2V_{Cr}(1-\omega^2 L_r C_r)\cos\theta_1}{V_{bus}\cos\varepsilon} - M\frac{\cos\varphi_{AB}}{\cos\varepsilon} \tag{3.20}$$

where $\varepsilon = \arctan[\frac{V_{Cr}(1-\omega^2 L_r C_r)\sin\theta_1 - V_{bus}M\sin\varphi_{AB}}{V_{Cr}(1-\omega^2 L_r C_r)\cos\theta_1 - V_{bus}M\cos\varphi_{AB}}]$. The aforementioned modulation strategies for parallel active power decoupling with three single phase legs are all based on sinusoidal pulse width modulation (SPWM). In fact, since there are three single phase legs, they can also be treated as three phase unbalanced circuits. Therefore, the concept of space vector pulse width modulation (SVPWM) is applicable where there is tradeoff towards the dc voltage utilizations between the main and power decoupling circuit [108, 120, 122].

Due to the coupling between the main and power decoupling circuit, it is necessary to investigate the current stresses of the shared single phase leg to ensure that there is no obvious increased current through power devices of the main circuit. It is assumed that

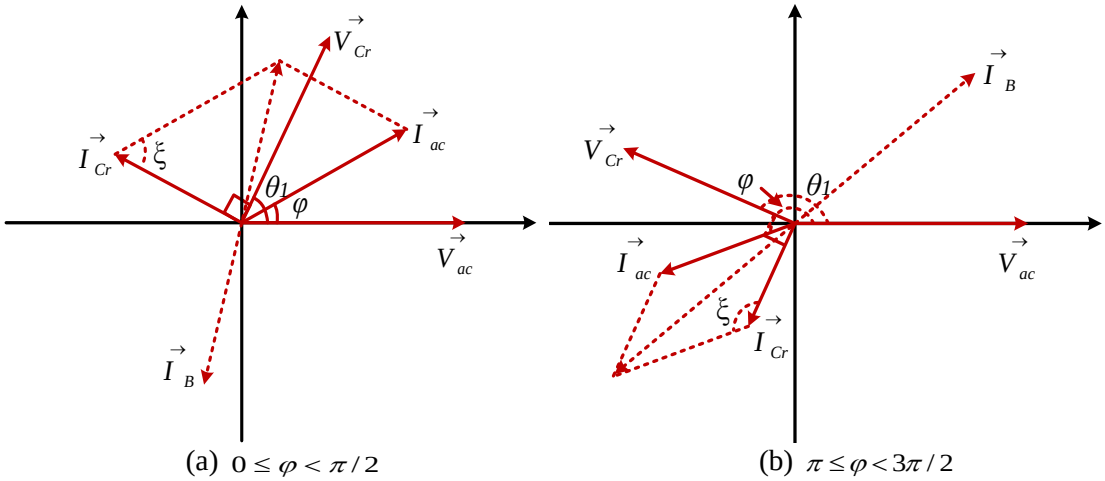


Figure 3.10: Phasor diagram of parallel active power decoupling with three single phase legs.

phase B is shared by both the main and power decoupling circuit. From (3.17), if $0 \le \varphi < \pi/2$, $\theta_1 \ge \varphi$ can be obtained and the phasor diagram is shown in Figure 3.10(a) in which $\xi = \pi/2 - \theta_1 + \varphi \le \pi/2$. Therefore according to (3.21), the current stresses of power devices in phase B can increase when $V_{grid} > \sqrt{2} V_{Cr} \cos\xi$.

$$I_{Cr}{}^2 + 2I_{grid}{}^2 - 2\sqrt{2} I_{Cr} I_{grid} \cos\xi = I_B{}^2 \tag{3.21}$$

When $\pi \le \varphi < 3\pi/2$, the phasor diagram is shown in Figure 3.10(b) where $\xi = \pi/2 - \theta_1 + \varphi > \pi/2$. Therefore, the current stresses of phase B will definitely increase.

To provide helpful guidance on the design of active power decoupling for the two stage PV microinverters, Table 3.1 summarizes the evaluations on component counts, energy utilization and voltage/current ripple of energy storage components, dc voltage utilizations of both the main and power decoupling circuit, and current stresses of power devices in the main circuit respectively.

Table 3-1: Summarized evaluation of active power decoupling techniques for the two stage PV microinverters.

Active Power Decoupling Technqiues	Components	Energy Utilization Efficiency	Voltage Ripple Factor	Dc Voltage Utilization		Current Stresses (shared single phase leg)	Modulation Index		Capacitors Selection	Features
				Main Circuit	Power Decouping Circuit		Main Circuit	Power Decoupling Circuit		
[98]		1	equation (3.9)	1		Keep the same with main circuit with power decoupling	$in(\omega t+\varphi_{AB})$ and $-in(\omega t+\varphi_{AB})$		Solution ii equation (3.1)	1. No additional components; 2. Advanced control strategies with high double line frequency ripple rejection capability.
Figure 3.9(a)	2 power devices, 1 smooth inductor and 1 energy storage capacitor	equation (3.8)	equation (3.9)	1	0.5	Keep the same with main circuit with power decoupling	$in(\omega t+\varphi_{AB})$ and $-in(\omega t+\varphi_{AB})$	equation (3.11)	Solution ii $C_r=\frac{V_{grid}I_{grid}}{2\omega A_0 A_2}$	1. Independent SPWM modulation; 2. Bi-directional Buck.
Figure 3.9(b)	2 power devices, 1 smooth inductor	1	1	1	0.5	Keep the same with main circuit with power decoupling	$in(\omega t+\varphi_{AB})$ and $-in(\omega t+\varphi_{AB})$	equation (3.12)	Solution i $C_r=\frac{V_{grid}I_{grid}}{\omega {A_1}^2}$	1. Independent SPWM modulation; 2. Dc bus capacitors are used as energy storage capacitors; 3. Two energy storage capacitors at dc side.
Figure 3.9(c)	2 power devices, 1 smooth inductor and 1 energy storage capacitor	1	1	1	0.5	Figure 3.10	$in(\omega t+\varphi_{AB})$ and $-in(\omega t+\varphi_{AB})$	equation (3.20)	Solution i $C_r=\frac{2V_{grid}I_{grid}}{\omega {A_1}^2}$	1. Dependent SPWM modualtion; 2. Smoothing inductor can be combined with output inductor.
Figure 3.9(d)	2 power devices, 2 energy storage capacitor	1	1	1	0.5		$in(\omega t+\varphi_{AB})$ and $-in(\omega t+\varphi_{AB})$		Solution i	1. Dependent SPWM modualtion; 2. Two energy storage capacitors at ac side; 3. The voltage across each energy storage capacitor contains lots of harmonics components; 4. Both grid current and power decoupling current flow through output inductor.

3.4 Summary

This section presents the double line frequency power decoupling technqiues for the two stage PV microinverters. Based on the principle of power decoupling, the general solutions on the voltage across energy storage capacitors are derived and discussed. To decouple the ripple power completely and minimize the involved other frequency ripple powers, Solution i, in which the voltage across energy storage capacitors is line frequency sinusoidal waveform without dc offset, Solution ii, in which the voltage across energy storage capacitors is double line frequency sinusoidal waveform with dc offset, and Solution iii, in which the voltage across energy storage capacitors is full-wave rectified line frequency sinusoidal waveform, are obtained. The energy utilization efficiency η_E and voltage ripple factor η_r are introduced to evaluate the three solutions. By considering the ripple power paths, existing active power decoupling techniques can be divided into series and parallel ones. For parallel active power decoupling, the general configuration based on half-bridge structure can be obtained. Benefiting from the full dc voltage utilization of main circuit and full energy utilization of energy storage capacitors, parallel active power decoupling with three single phase legs and Solution i can be a good option for the two stage PV microinverters. In this case, the modulation of power decoupling circuit can be either dependent or independent on that of the main circuit. Furthermore, parallel active power decoupling with three single phase legs and Solution ii can be alternative for the two stage PV microinverters. In this case, the modulation of power decoupling circuit is independent on that of the main circuit. Even though the peak voltage of energy storage capacitors is higher, it allows lower capacitance and lower current through energy storage

capacitors. The dc voltage utilizations and the current stresses of power devices in the main circuit towards both independent and dependent modulation strategies are investigated in detail. Finally, the evaluations on the component counts, the energy utilization and voltage/current ripple of energy storage components, the dc voltage utilizations of both the main and power decoupling circuit, and the current stresses of power devices in the main circuit are summarized to provide guidance on the design of power decoupling in the two stage PV microinverters.

4. PR AND HYBRID HYSTERESIS CURRENT CONTROL STRATEGY

4.1 Introduction

Among various dc-ac inverters, the H-bridge, multilevel, Z-source and dual-buck topologies are broadly available in different applications [123-128]. Even though low *dv/dt*, smaller common-mode (CM) voltage, and low distortions of input current and output voltage can be achieved, multilevel topologies are mainly applied in the area of high-power medium-voltage power conditioning. For Z-source and quasi-Z-source topologies [129, 130], the voltage boost and inverter functions are combined into one power conversion stage. But the limitation between duty ratio and modulation index makes it hard to achieve high voltage gain and satisfy the grid-connected requirement simultaneously in PV microinverters. Furthermore, the non-isolation structure, and large volumes and power losses of passive components also limit the applications in PV microinverters. Even though the dual-buck topology in [126] can overcome shoot-through problem without dead times, extra power devices are needed. Given the low costs and low power devices counts, conventional H-bridge dc-ac inverter is always the most popular option in the two stage transformer isolated PV microinverters. However, the hard switching operation will inevitably result in high switching losses and severe electromagnetic interference (EMI), which, to some extent, limit the increase of switching frequency and the decrease of volumes towards passive components like output filter. Thus soft switching techniques such as passive losses soft switching snubber circuit in [131], auxiliary resonant commutation cell in [132], dc-link resonant circuit in [133, 134]

and ac-link auxiliary resonant circuit in [135], etc. are developed. But all of them need additional components which makes them complicated-to-implement, low efficient at light load or even only preferred in medium and high power applications. So hysteresis current control [136] and predictive control [137] were introduced to achieve soft switching without extra components. By intentionally controlling the output inductor current within hysteresis bands, fixed reverse current control, variable reverse current control, constant bandwidth current control and dual mode ZVS ZCS current control in [58, 138], etc can be implemented. Even though the wide hysteresis bands definitely increase the core losses of the output inductor and the variable frequency operation complicates the design of output filter, the switching losses can be reduced greatly which means increased efficiency.

This section first proposed unipolar hysteresis current control with soft switching to halve the switching frequency of power devices without increasing the output inductance. However, it suffers from zero-crossing distortions and low frequency harmonics in the grid current. The zero-crossing distortions can result from either the delays or the smaller slope of output inductor current than that of reference current. [139] explained the reason of zero-crossing distortions caused by delays in terms of average current analysis method and compared that with bipolar modulation. By establishing the mathematical model of grid-connected inverter around zero-crossing points, [140] proposed on-line leading phase angle compensation to suppress the distortions due to smaller slope. Based on those, the hybrid hysteresis current control with soft switching is proposed which enables bipolar modulation around zero-crossing points to eliminate zero-

crossing distortions and unipolar modulation in other moments of the line period to achieve halved switching frequency of power devices. The wide hysteresis bands and low output inductance in this proposed control strategy can cause errors between the reference current and the average current through output inductor, which increases with sampling intervals and can introduce lots of low frequency harmonics. To solve this problem, [141] proposed a switching time prediction by linearizing the tolerance band limit to reduce the deviation substantially. In [142], another switching time prediction, which was based on calculated time quantities and rough estimation of output inductance, was presented to compensate the bad effect of delays from dead time, driving circuits and sampling intervals. [143, 144] also introduced a predictive control to calculate the duty cycle for each switching period and limit the output inductor current within the hysteresis bands. Even though the predictive algorithms mentioned above can minimize the low frequency harmonics by controlling the switching states accurately, the increased signal processing requirements and control complexity definitely burden the digital controller. Thus, the combined PR controller is used to minimizing the steady state error at low frequency and mitigate the low frequency harmonics without complicated predictive calculations.

In this section, the principle of the proposed unipolar hysteresis current control with soft switching, parameters designs and frequency distributions are investigated first. Then the analysis and solutions on zero-crossing distortions and low frequency harmonics are discussed in detail. Finally, the simulation and experimental results verify the feasibility of the proposed control strategy.

4.2 Operation principle

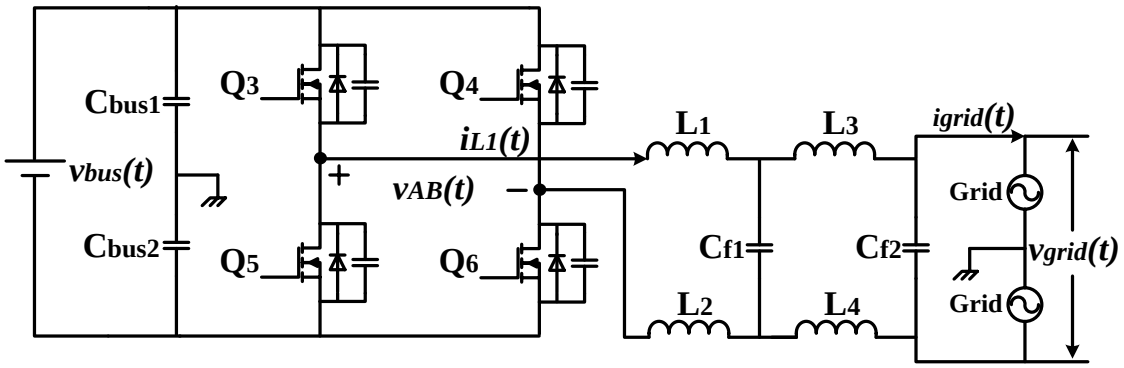


Figure 4.1: Topology of dc-ac inverter in the two stage PV microinverters.

The topology of dc-ac inverter in the two stage PV microinverters is shown in Figure 4.1 where $v_{bus}(t)$ is the input voltage (dc bus voltage) and is also the output voltage of the front-end dc–dc converter. $v_{AB}(t)$ is the H-bridge output voltage and $i_{L1}(t)$ is the current through output inductor L_1 and L_2. The split phase grid voltage for the residential and commercial applications is $v_{grid}(t)$. The current flowing into the grid is $i_{grid}(t)$. Collectively, L_1, L_2, L_3, L_4, C_{f1} and C_{f2} comprise the output filter. The scheme of the unipolar hysteresis current control with soft switching is illustrated in Figure 4.2 where $i_{L1\_upper}(t)$ and $i_{L1\_lower}(t)$ are the hysteresis bands. I_{hb} and I represent the reverse current and the boundary current respectively. $i_{ref}(t)$ represents the reference of the grid current. From this, it is known that there are two commutation modes in one line cycle. When the reference current is close to zero-crossing points and the magnitude is less than I, $i_{L1}(t)$ is intentionally controlled to flow in both positive and negative directions to achieve ZVS commutation. When the magnitude of the reference current is larger than I, $i_{L1}(t)$ is regulated using boundary current mode to achieve ZCS commutation. The typical

waveforms in both positive and negative half line cycle are shown in Figure 4.3. From that, the unipolar modulation allows halved switching frequency of power devices without increasing the output inductance as expected. The different operation modes within one switching period of positive half cycle can be discussed in detail as follows.

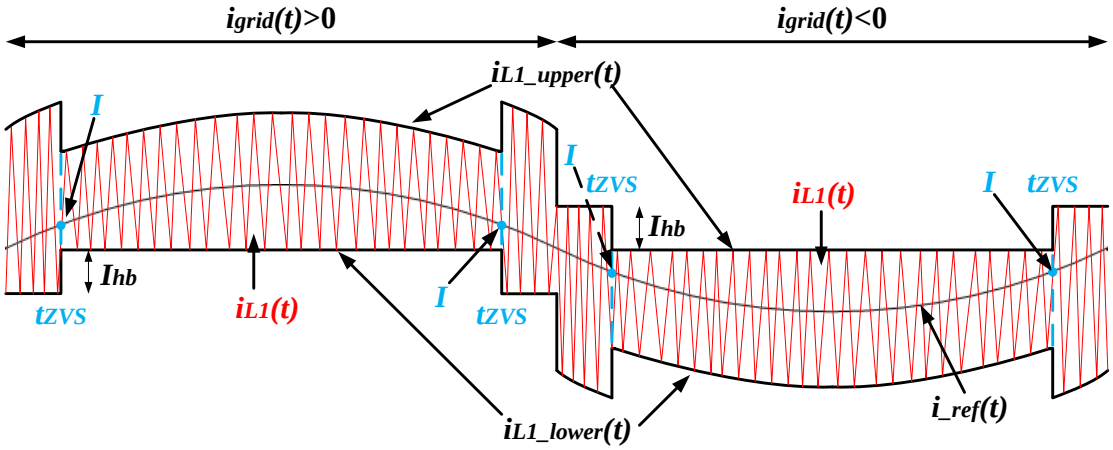
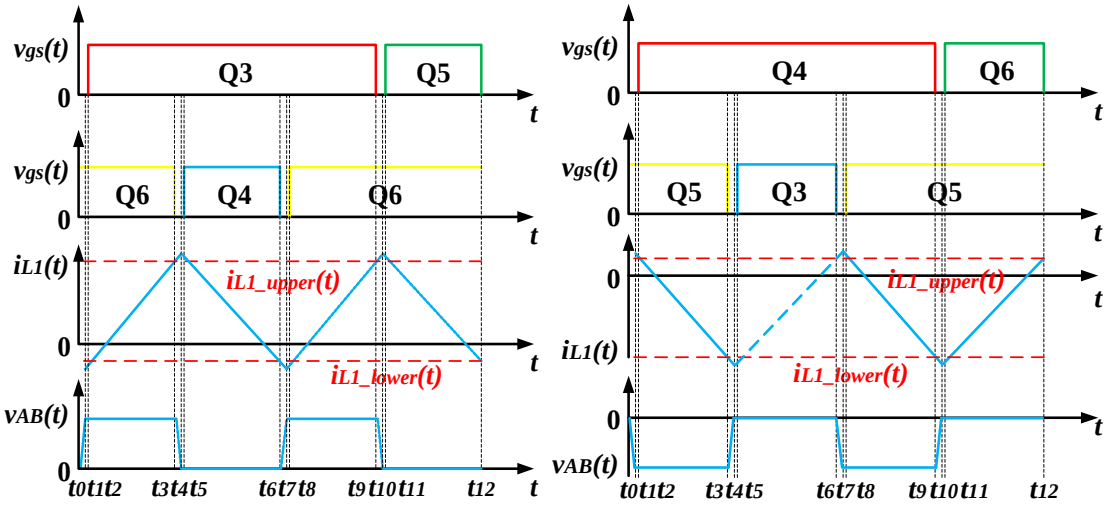


Figure 4.2: Scheme of the unipolar hysteresis current control.



(a) $i_{grid}(t)>0$ (b) $i_{grid}(t)<0$

Figure 4.3: Typical waveforms of the unipolar hysteresis current control.

Mode i [t_0<t<t_1]: as shown in Figure 4.4(a). Q_5 turns off at t_0. If the reference current is around zero-crossing points which means ZVS commutation, the output inductor current $i_{L1}(t)$ charges C_{ds} of Q_5 and discharges C_{ds} of Q_3 respectively. If the magnitude of the reference current is larger than I, $i_{L1}(t)$ is zero and will allow Q_5 to turn off with ZCS. The hysteresis band $i_{L1\_lower}(t)$ can be expressed as:

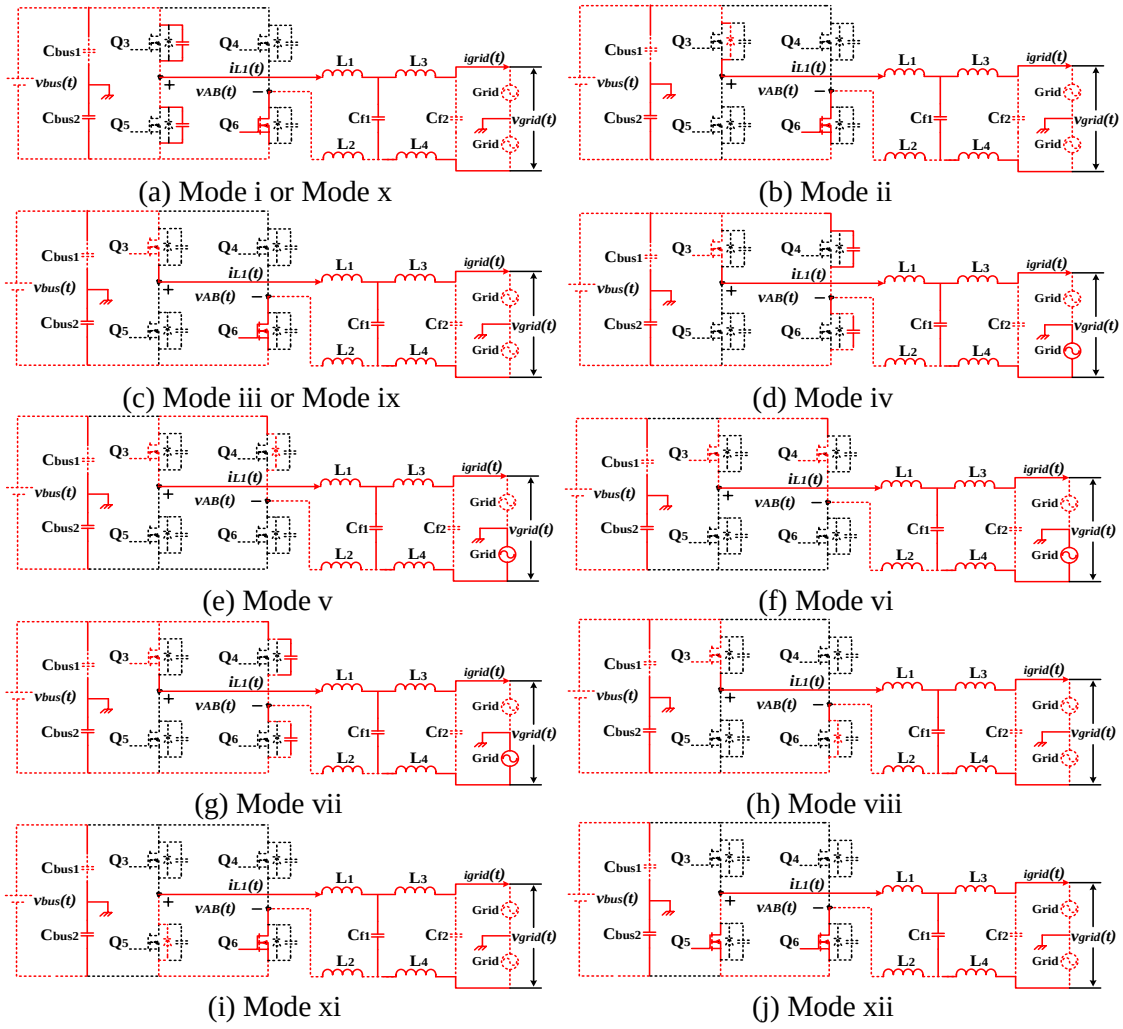


Figure 4.4: Operation modes of unipolar hysteresis current control with soft switching ($i_{grid}(t)$>0).

$$i_{L1\_lower}(t)=\begin{cases}-I_{hb} & \text{if } \sqrt{2}I_{grid}\sin(\omega t)\geq 0 \text{ and } \sqrt{2}I_{grid}\sin(\omega t)\leq I\\ 0 & \text{if } \sqrt{2}I_{grid}\sin(\omega t)\geq 0 \text{ and } \sqrt{2}I_{grid}\sin(\omega t)> I\\ 2\cdot\sqrt{2}I_{ref}\sin(\omega t)-I_{hb} & \text{if } \sqrt{2}I_{grid}\sin(\omega t)< 0 \text{ and } \sqrt{2}I_{grid}\sin(\omega t)\geq -I\\ 2\cdot\sqrt{2}I_{ref}\sin(\omega t) & \text{if } \sqrt{2}I_{grid}\sin(\omega t)< 0 \text{ and } \sqrt{2}I_{grid}\sin(\omega t)< -I\end{cases} \quad (4.1)$$

Mode ii [$t_1<t<t_2$]: as shown in Figure 4.4(b). While C_{ds} of Q_3 is fully discharge, its body diode turns on and this allows Q_3 to turn on with ZVS at t_2.

Mode iii [$t_2<t<t_3$]: as shown in Figure 4.4(c). At t_2, Q_3 turns on with ZVS or ZCS. During this period, the voltage across output inductor L_1 and L_2 can be expressed as:

$$(L_1+L_2)\frac{di_{L1}(t)}{dt}=v_{bus}(t)-v_{grid}(t) \quad (4.2)$$

Mode iv [$t_3<t<t_4$]: as shown in Figure 4.4(d). Once Q_6 turns off with hard switching, the output inductor current $i_{L1}(t)$ will charge C_{ds} of Q_6 and discharge C_{ds} of Q_4. The hysteresis band $i_{L1\_upper}(t)$ can be expressed as:

$$i_{L1\_upper}(t)=\begin{cases}2\cdot\sqrt{2}I_{ref}\sin(\omega t)+I_{hb} & \text{if } \sqrt{2}I_{grid}\sin(\omega t)\geq 0 \text{ and } \sqrt{2}I_{grid}\sin(\omega t)\leq I\\ 2\cdot\sqrt{2}I_{ref}\sin(\omega t) & \text{if } \sqrt{2}I_{grid}\sin(\omega t)\geq 0 \text{ and } \sqrt{2}I_{grid}\sin(\omega t)> I\\ I_{hb} & \text{if } \sqrt{2}I_{grid}\sin(\omega t)< 0 \text{ and } \sqrt{2}I_{grid}\sin(\omega t)\geq -I\\ 0 & \text{if } \sqrt{2}I_{grid}\sin(\omega t)< 0 \text{ and } \sqrt{2}I_{grid}\sin(\omega t)< -I\end{cases} \quad (4.3)$$

Mode v [$t_4<t<t_5$]: as shown in Figure 4.4(e). When C_{ds} of Q_4 is fully discharged, its body diode turns on and this allows Q_4 to turn on with ZVS at t_5.

Mode vi [$t_5<t<t_6$]: as shown in Figure 4.4(f). Q_4 turns on with ZVS. During this period, the voltage across output inductor L_1 and L_2 can be given by:

$$(L_1+L_2)\frac{di_{L1}(t)}{dt}=-v_{grid}(t) \quad (4.4)$$

Mode vii [$t_6<t<t_7$]: as shown in Figure 4.4(g) which is similar to Mode i. When $i_{L1}(t)$ reaches the hysteresis band $i_{L1\_lower}(t)$, Q_4 turns off. If the reference current is around

zero-crossing points which means ZVS commutation, the output inductor current $i_{L1}(t)$ charges C_{ds} of Q_4 and discharges C_{ds} of Q_6 respectively. If the magnitude of the reference current is larger than I, $i_{L1}(t)$ is zero and will allow Q_4 to turn off with ZCS.

Mode viii [$t_7<t<t_8$]: as shown in Figure 4.4(h). While C_{ds} of Q_6 is fully discharged, its body diode turns on and this allows Q_6 to turn on with ZVS.

Mode ix [$t_8<t<t_9$]: as shown in Figure 4.4(c). At t_8, Q_6 turns on with ZVS or ZCS which is similar to that in Mode iii.

Mode x [$t_9<t<t_{10}$]: as shown in Figure 4.4(a). When Q_3 turns off at t_9 with hard switching, the output inductor current $i_{L1}(t)$ will charge C_{ds} of Q_3 and discharge C_{ds} of Q_5.

Mode xi [$t_{10}<t<t_{11}$]: as shown in Figure 4.4(i). When C_{ds} of Q_5 is fully discharged, its body diode turns on and this allows Q_5 to turn on with ZVS. The H-bridge output voltage $v_{AB}(t)$ is equal to zeo and $i_{L1}(t)$ starts decreasing.

Mode xii [$t_{11}<t<t_{12}$]: as shown in Figure 4.4(j). At t_{11}, Q_5 turns on with ZVS which is similar to that in Mode vi. Then a new switching period will be followed. In negative half cycle, the switching sequence of power devices is shown in Figure 3.3(b) where the operation modes are similar to those discussed above.

4.3 Frequency analysis

Based on the investigations on the unipolar hysteresis current control strategy, (4.2) and (4.4), the frequency of H-bridge output voltage $v_{AB}(t)$ can be derived from (4.5) below.

$$f_{H-b}(t) = \frac{v_{Cf}(t)[v_{bus}(t) - v_{Cf}(t)]}{(L_1 + L_2)[i_{L1\_upper}(t) - i_{L1\_lower}(t)]v_{bus}(t)} \tag{4.5}$$

where, $v_{Cf}(t)$ is the voltage across output capacitor C_{f1} and can be expressed as:

$$v_{Cf}(t) = (L_3 + L_4)\frac{di_{L3}(t)}{dt} + v_{grid}(t) = \sqrt{2}\omega(L_3 + L_4)[I_{grid}\cos(\omega t) - C_{f2}V_{grid}\omega\sin(\omega t)] + \sqrt{2}V_{grid}\sin(\omega t) \tag{4.6}$$

In PV microinverters, since $\omega C_{f2}V_{grid} < I_{grid}$ and $\omega(L_3 + L_4)I_{grid} << V_{grid}$, $v_{Cf}(t)$ can be simplified as $v_{Cf}(t) \approx \sqrt{2}V_{grid}\sin(\omega t)$. Then substituting (4.1) and (4.3) into (4.5), the frequency of H-bridge output voltage becomes:

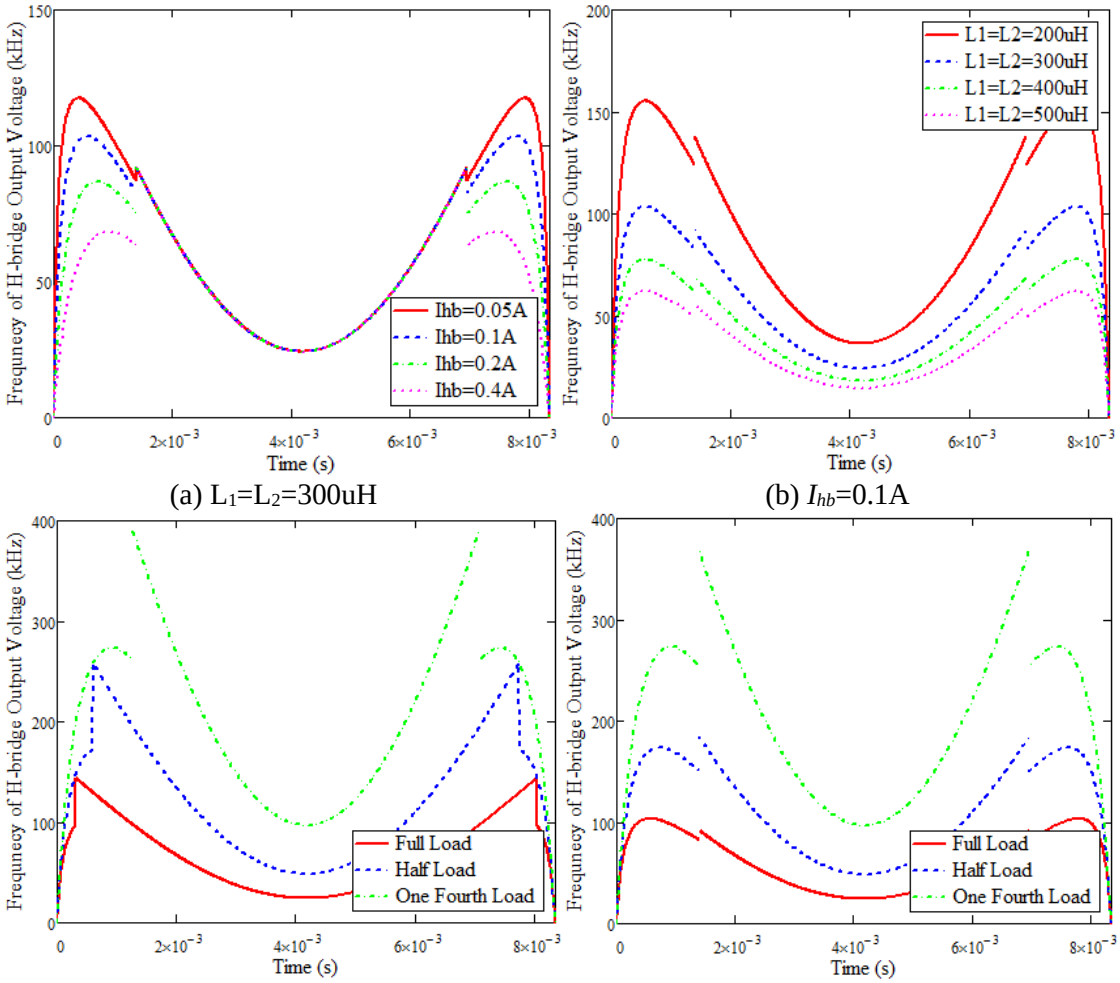
$$f_{H-b}(t) = \begin{cases} \dfrac{\sqrt{2}V_{grid}\sin(\omega t)[V_{bus} - \sqrt{2}V_{grid}\sin(\omega t)]}{(L_1 + L_2)[2\sqrt{2}I_{grid}\sin(\omega t) + 2I_{hb}]V_{bus}} & \text{if } \left|\sqrt{2}I_{grid}\sin(\omega t)\right| \le I \\ \dfrac{\sqrt{2}V_{grid}\sin(\omega t)[V_{bus} - \sqrt{2}V_{grid}\sin(\omega t)]}{(L_1 + L_2)[2\sqrt{2}I_{grid}\sin(\omega t)]V_{bus}} & \text{if } \left|\sqrt{2}I_{grid}\sin(\omega t)\right| > I \end{cases} \tag{4.7}$$

where, V_{bus} represents the average voltage of dc bus. While defining M as the amplitude modulation index of the proposed control strategy, the ratio of the rising time towards output inductor current $i_{L1}(t)$ to the instantaneous switching period, in terms of the peak split phase grid voltage and the dc bus voltage, can be obtained by (4.8).

$$d(t) = M\sin(\omega t) = \frac{\sqrt{2}V_{grid}}{V_{bus}}\sin(\omega t) \tag{4.8}$$

From those equations, it is revealed that the switching frequency of power devices isn't constant and the frequency distributions are dependent on several different varaibles.

Figure 4.5 shows the frequency distributions of H-bridge output voltage $v_{AB}(t)$ on output inductance of L_1 and L_2, reverse current I_{hb}, boundary current I and boundary point t_{ZVS}, which can be concluded that with full load, larger output inductance results in smaller frequency variations and smaller frequency changes at boundary points. At the same time, larger reverse current I_{hb} contributes to smaller frequency variations, but represents larger



(a) L_1=L_2=300uH (b) I_{hb}=0.1A

(c) L_1=L_2=300uH; I_{hb}=0.1A; I=0.2A (d) L_1=L_2=300uH; I_{hb}=0.1A; t_{zvs}=1/720s

Figure 4.5: Frequency distributions of H-bridge output voltage in half line cycle.

frequency changes at boundary points. The minimum reverse current I_{hb} should fully discharge C_{ds} of Q_5 or Q_6 to allow ZVS commutation. While comparing Figure 4.5(c) with (d), it can be observed that with the fixed boundary point t_{ZVS}, there will be reduced frequency variations and frequency changes except for at light load. Furthermore, while the boundary current I is equal to 0.2A, the respective boundary points t_{ZVS} are always less than 1/720s. In terms of (4.9) below, the RMS of output inductor current $i_{L1}(t)$ only has limited increase with that of t_{ZVS} as show in Figure 4.6(a) and (c). So combined with Figure 4.5(c) and (d), the fixed boundary points can be chosen to optimize the frequency distributions of output inductor current $i_{L1}(t)$.

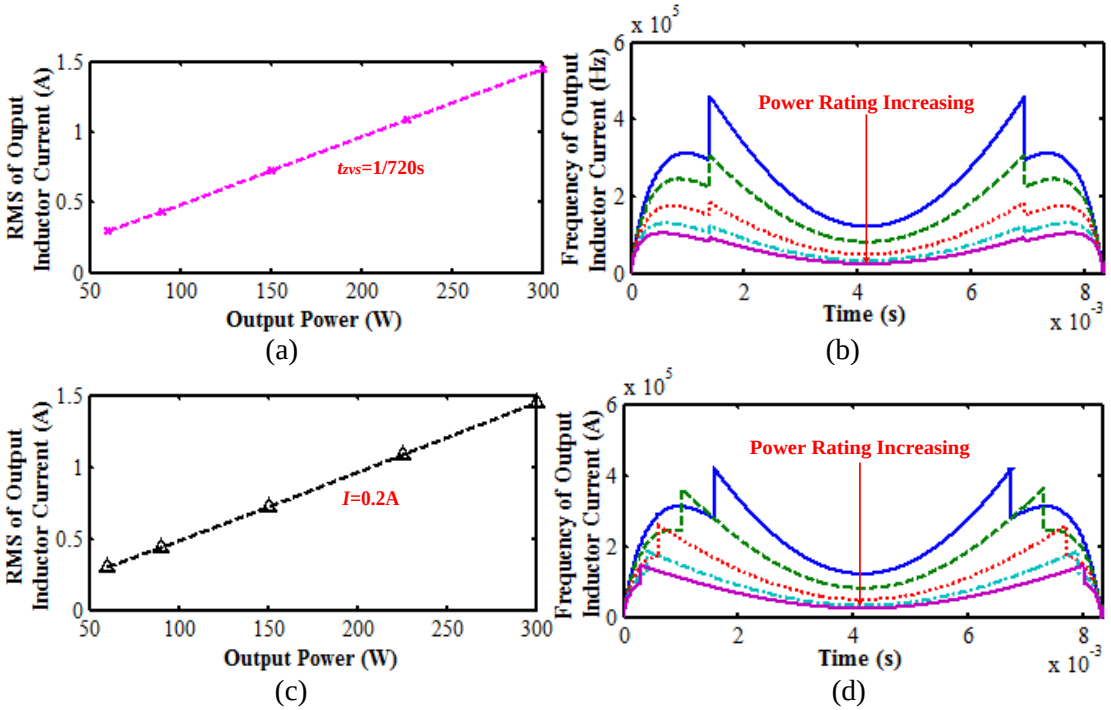


Figure 4.6: (a) RMS of output inductor current $i_{L1}(t)$ with fixed boundary point t_{ZVS}; (b) Frequency distributions with fixed boundary points t_{ZVS} at different loads; (c) RMS of output inductor current with fixed boundary current I; (d) Frequency distributions with fixed boundary current I at different loads.

$$i_{L1\_RMS}(t) = \sqrt{\frac{4}{3} I_{grid}{}^{2} + \frac{4}{3} I_{hb}{}^{2} t_{ZVS} f_s} \tag{4.9}$$

At the same time, to avoid sudden frequency changes at boundary points and limit the maximum switching frequency, the following two equations should be satisfied while designing the parameters in this proposed control strategy.

$$\frac{\sqrt{2}V_{grid}\sin(\omega t_{ZVS})[V_{bus} - \sqrt{2}V_{grid}\sin(\omega t_{ZVS})]}{(L_1 + L_2)[2\sqrt{2}I_{grid}\sin(\omega t_{ZVS}) + 2I_{hb}]V_{bus}} \cong \frac{\sqrt{2}V_{grid}\sin(\omega t_{ZVS})[V_{bus} - \sqrt{2}V_{grid}\sin(\omega t_{ZVS})]}{(L_1 + L_2)[2\sqrt{2}I_{grid}\sin(\omega t_{ZVS})]V_{bus}} \tag{4.10}$$

$$f_{H-b\_\max}(t) = \frac{2V_{grid}I_{hb}{}^{2} + V_{grid}I_{grid}V_{bus} - 2V_{grid}\sqrt{V_{grid}{}^{2}I_{hb}{}^{2} + V_{grid}I_{grid}V_{bus}I_{hb}}}{2(L_1 + L_2)V_{bus}I_{grid}{}^{2}} \tag{4.11}$$

In the light of the discussions about above, the parameters of output inductance L_1 and L_2, reverse current I_{hb}, and boundary point t_{ZVS} in the proposed unipolar hysteresis current control strategy can be calculated approximately and the respective frequency distributions can be obtained.

4.4 Loss analysis

According to the operation principle of proposed unipolar hysteresis current control strategy in dc-ac inverter discussed above, when the dc-ac inverter operates under ZVS commutation, the RMS of output inductor current $i_{L1}(t)$ within one switching period can be obtained by:

$$i_{L1\_RMS\_ZVS}(t) = \sqrt{\frac{1}{3}}[2\sqrt{2}I_{grid}\sin(\omega t) + 2I_{hb}] \tag{4.12}$$

When it operates under ZCS commutation, the RMS of $i_{L1}(t)$ within one switching period can be expressed as:

$$i_{L1\_RMS\_ZCS}(t) = \sqrt{\frac{1}{3}}[2\sqrt{2}I_{grid}\sin(\omega t)] \tag{4.13}$$

Thus combined with (4.14) and (4.9), the conduction power losses of power devices can be given by:

$$i_{L1\_RMS} = \sqrt{\frac{1}{T}\left(\begin{array}{l}\int_0^{t_{ZVS}} {i_{L1\_RMS\_ZVS}}^2 dt + \int_{T/2-t_{ZVS}}^{T/2+t_{ZVS}} {i_{L1\_RMS\_ZVS}}^2 dt + \int_{T-t_{ZVS}}^{T} {i_{L1\_RMS\_ZVS}}^2 dt + \\ \int_{t_{ZVS}}^{T/2-t_{ZVS}} {i_{L1\_RMS\_ZCS}}^2 dt + \int_{T/2+t_{ZVS}}^{T-t_{ZVS}} {i_{L1\_RMS\_ZCS}}^2 dt\end{array}\right)} \tag{4.14}$$

$$P_{con\_Q} = 4{i_{L1\_RMS}}^2 R_{ds\_on\_inv} \tag{4.15}$$

where, T is the line period (16.67ms). $R_{ds\_on\_inv}$ represents the conduction resistance of power devices in dc-ac inverter. Within ZVS commutation region, the turn-off of all power devices are hard switching. However, since the reverse current I_{hb} is small, the turn-off switching losses of Q_2 and Q_3 in positive half cycle (Q_1 and Q_4 in negative half cycle) are small as well. Within ZCS commutation region, while commutating in positive half cycle, both turn-on and turn-off of Q_1 and Q_4 are hard switching; while commutating in negative

half cycle, both turn-on and turn-off of Q_2 and Q_3 are hard switching. Therefore, the switching losses can be calculated from (4.16) approximately.

$$P_{sw\_Q}(t) = \frac{V_{bus}\left(\frac{24 t_{ZVS} I_{hb} f_{sw}(t)}{T} + 4 I_{equiva} f_{sw}(t)\right)\left(\frac{Q_{gd} R_{goff}}{V_{plateau}} + \frac{Q_{gs} R_{goff}}{V_{plateau} + V_{gs(th)}}\right)}{2} \tag{4.16}$$

where, $f_{sw}(t)$ is switching frequency of power devices which is half of that towards H-bridge output voltage. Q_{gd} and Q_{gs} are the gate-to-drain and gate-to-source charge respectively. R_{goff} is the gate resistance. $V_{plateau}$ and $V_{gs(th)}$ represent the plateau voltage and threshold voltage of power devices. Since the hysteresis bands are changing within one line cycle, the equivalent current I_{equiva}, which is equal to $4\sqrt{2} I_{grid} / \pi$, is used to emulate the turn-off current.

Given the soft switching operation in the proposed unipolar hysteresis current control strategy, the switching losses and reverse recovery losses of power devices, which are the main components of total power losses in conventional hard switching strategies, can be reduced greatly. At the same time, due to the wide hysteresis bands, the copper and core losses for the output inductor L_1 and L_2 will definitely increase, especially while there is large ac flux swing in the magnetic core. In the two stage PV microinverters, since the power rating is about 200W~300W and the split phase grid voltage is 240V, the grid current is aound 1A. Therefore, by choosing appropriate magnetic cores with low core losses (such as ferrite core or Kool Mμ powder core) and optimizing the magnetic design, it is totally possible to ensure that the increased power losses from the output inductor L_1 and L_2 are much lower than the reduced power losses because of soft switching operation. Recently, benefiting from the superior conduction and swiching characteristics, the high

voltage (600V~650V) GaN power devices (shown in Table 4-1) are also becoming more and more popular [145-148]. By replacing the MOSFETs with GaN HEMTs, the power losses of power devices in dc-ac inverter with the proposed unipolar hysteresis current control strategy can decrease by 15%-20%. At the same time, the possible higher switching frequency can boost the power density of the dc-ac inverter in the two stage PV microinverters.

Table 4-1: Commercially available GaN power devices from the main manufacturers until 2015 [145-148].

Manufacturers	Voltage Ratings	Current Ratings	Conduction Resistance	Configuration
EPC	30 V~300 V	1 A~60 A	1.3 mohm~2800 mohm	enhancement mode
Transphorm (Fujitsu)	600 V	9 A~34 A	52 mohm~290 mohm	cascaded
RFMD	650 V		45 mohm	cascaded
MicroGaN	600 V	30 A	170 mohm	cascaded (normally-on)
			320 mohm	cascaded (normally-off)
Infineon (IR)	600 V			cascode (cascaded)
Panasonic (Infineon)	600 V	10 A, 15 A	54 mohm, 71 mohm	enhancement mode
GaN Systems	100 V	45 A, 80 A, 90 A	7.4 mohm, 15 mohm	enhancement mode
	600 V	7 A~60 A	27 mohm~220 mohm	

4.5 Zero-crossing distortions

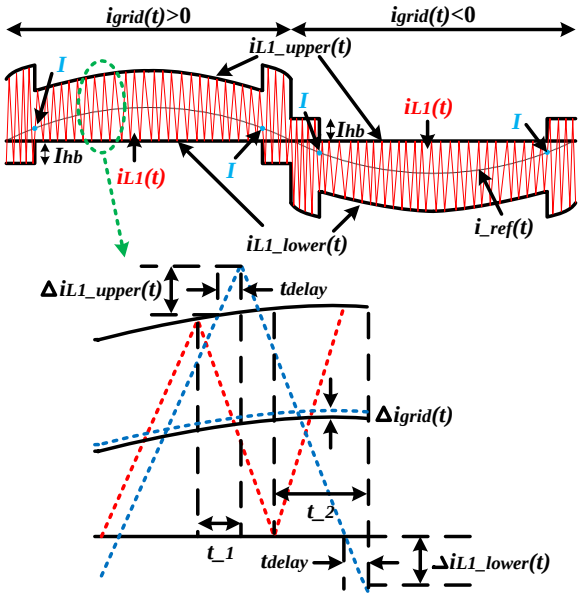


Figure 4.7: Detailed current waveform through output inductor L_1 and L_2 in one switching period.

The detailed output inductor current $i_{L1}(t)$ within one switching period is illustrated in Figure 4.7 where the red solid line and the blue dot line represent the ideal and actual current through L_1 and L_2 respectively. It is observed that due to the delay (t_{delay}) from dead times, driving circuits and sampling intervals, the actual output inductor current $i_{L1}(t)$ can be beyond the hysteresis bands. Since, for each switching period, both the rising and falling slopes of $i_{L1}(t)$ are dependent on the input voltage and grid voltage, the overshoot currents $\Delta i_{L1\_upper}(t)$ and $\Delta i_{L1\_upper}(t)$ can be different which inetivably results in different switching delays ($t_{\_1}$ and $t_{\_2}$) and deviations ($\Delta i_{grid}(t)$) between the reference current and average output inductor current through L_1 and L_2. Thus the reference current and actual average output inductor current can behave as shown in (4.17) and Figure 4.8 where it is

known that, around zero-crossing points, there is dc offset which results in the zero-crossing distortions.

$$i_{L1\_ave}(t) = [i_{\_ref}(t) - \frac{t_{delay} v_{grid}(t)}{L_1 + L_2}]\sin(\omega t) \pm \frac{t_{delay} v_{bus}(t)}{2(L_1 + L_2)} \tag{4.17}$$

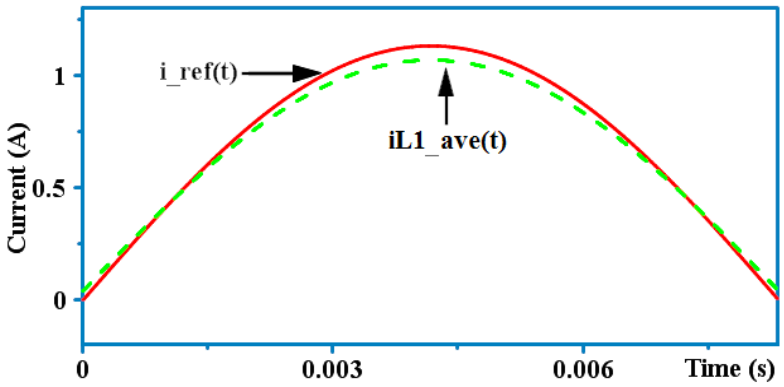
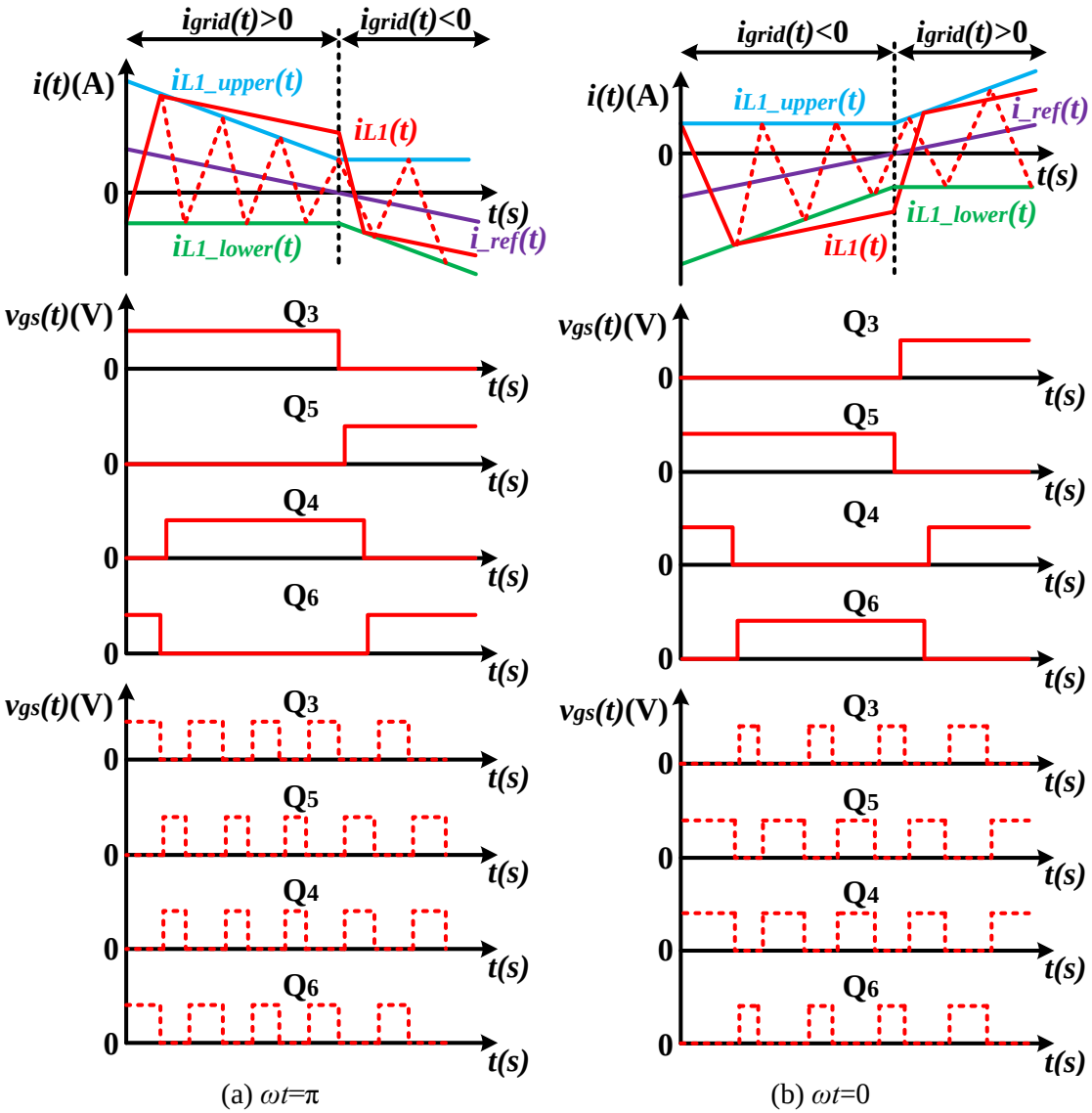


Figure 4.8: Difference between reference current and average output inductor current through L_1 and L_2 in unipolar modulation with delays.

Another reason on zero-crossing distortions is the smaller slope of the output inductor current $i_{L1}(t)$ than that of reference current as shown in Figure 4.9 where the solid red line and dot red line of $v_{gs}(t)$ represent the original and optimized driving signals respectively. Through Figure 4.9(a), it is shown that when the falling slope of $i_{L1}(t)$ is smaller than that of the reference current in positive half cycle, the output inductor current $i_{L1}(t)$ will not fall to the lower hysteresis band until the reference current go to the negative half cycle. At the same time, due to the smaller slope at the first several switching periods of negative half cycle, it takes longer time for $i_{L1}(t)$ to rise to the upper hysteresis band which means slower regulation on the output inductor current through L_1 and L_2. Thus there are always zero-crossing distortions. Similarly, when the falling slope of $i_{L1}(t)$ is smaller than that of the reference current in negative half cycle of Figure 4.9(b), the output

inductor current $i_{L1}(t)$ will not rise to the upper hysteresis band until the reference current go to the positive half cycle. Likewise, due to smaller slope at the first several switching periods of positive half cycle, it takes longer time for $i_{L1}(t)$ to fall to the lower hysteresis band. So the zero-crossing distortions exist around both ωt=0 and ωt=π.



(a) ωt=π (b) ωt=0

Figure 4.9: Analysis and solution on zero-crossing distortions due to smaller slope of output inductor current $i_{L1}(t)$ than that of reference current around zero-crossing points.

According to the analysis mentioned above, it is revealed that both delays and smaller slope of output inductor current $i_{L1}(t)$ result in the zero-crossing distortions. For the former reason of the distortions, combined with (4.17), it can be optimized by minimizing the delays or increasing the output inductance or using bipolar modulation. However, first the increased output inductance will decrease the power density of dc-ac inverter. Second, since the main component in those delays is from the sampling intervals, the minimized delays will definitely require fast digital controllers. Finally, the bipolar modulation will double the switching frequency and the switching losses of power devices. For the latter reason, it is inherently related to the unipolar modulation and the increased output inductance can even worsen the zero-corssing distortion due to much smaller slope of the output inductor current $i_{L1}(t)$. Therefore, the hybrid hysteresis current control, which enables bipolar modulation around the zero-crossing points to minimize the zero-crossing distortions and unipolar modulation in other moments of the line cycle to achieve halved switching frequency of power devices, is proposed as shown in Figure 4.9. The boundary condition should satisfy the following equation.

$$\frac{di_{\_ref}(t)}{dt} = \sqrt{2} I_{REF} \omega \cos(\omega t) = \frac{\sqrt{2} V_{grid} \sin(\omega t)}{L_1 + L_2} = \frac{di_{L1}(t)}{dt} \tag{4.18}$$

where, it is observed that once the output inductance L_1 and L_2, and the grid voltage are fixed, the boundary condition is only dependent on the grid current (power rating). Combined with the boundary points between ZVS and ZCS commutation in the original unipolar hysteresis current control, it is necessary to find out the larger one to simplify the control logic and eliminate the possible current spikes during multiple transitions.

4.6 Low frequency harmonics mitigation

In fact, the hybrid hysteresis current control proposed above to optimize the zero-crossing distortions can mitigate some of the low frequency harmonics. But due to wide hysteresis bands for soft switching, low output inductance L_1 and L_2, and non-negligible sampling intervals from the digital controller, the errors between reference current and average output inductor current still result in lots of low frequency harmonics. Thus the grid current needs to be sensed and fed back to compare with the reference current. At the same time, the reference current can be fed forward. Then the steady state error at low frequency can be mitigated by the PR control [149] and the power quality flowing into the grid can be further improved. The proposed control diagram is shown in Figure 4.10 below.

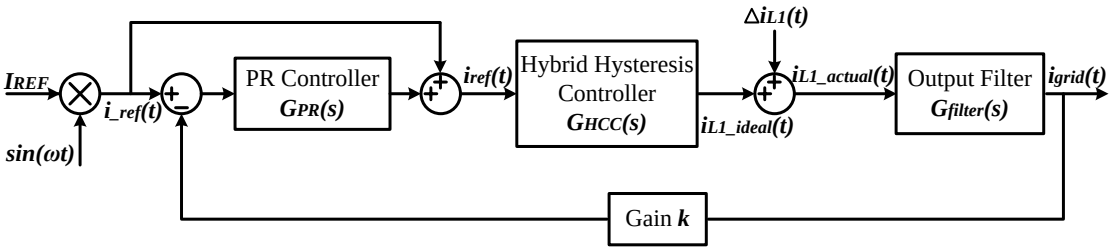


Figure 4.10: Control diagram of proposed PR and hybrid hysteresis current control.

The transfer function of PR controller in this proposed control diagram can be expressed as:

$$G_{PR}(s) = k_p + \frac{2k_c\omega_c s}{s^2 + 2\omega_c s + \omega_0{}^2} \tag{4.19}$$

For the transfer function of hybrid hysteresis current control, since it is non-linear controller, the small signal and the averaging assumption in conventional linear controller

are no long valid. Thus an equivalent transfer function based on extended state averaging method using perturbed on-time and switching period is given by [150]:

$$G_{HCC}(s) = k_{HCC} \tag{4.20}$$

where it is concluded that the equivalent model can be regarded as a proportional component and k_{HCC} is a constant related to the sensing gain. This approximation above is valid for two main reasons: 1) the switching frequency is much higher than the line frequency; 2) the discussion is focued on low frequency harmonics in the grid current. The disturbance $\Delta i_{L1}(t)$ in this control diagram results from the proposed hysteresis current controller, and the delays mentioned previously in which the sampling interval is the main component. The open loop transfer function $G(s)$ is given by (4.21) and the bode plots are illustrated in Figure 4.11.

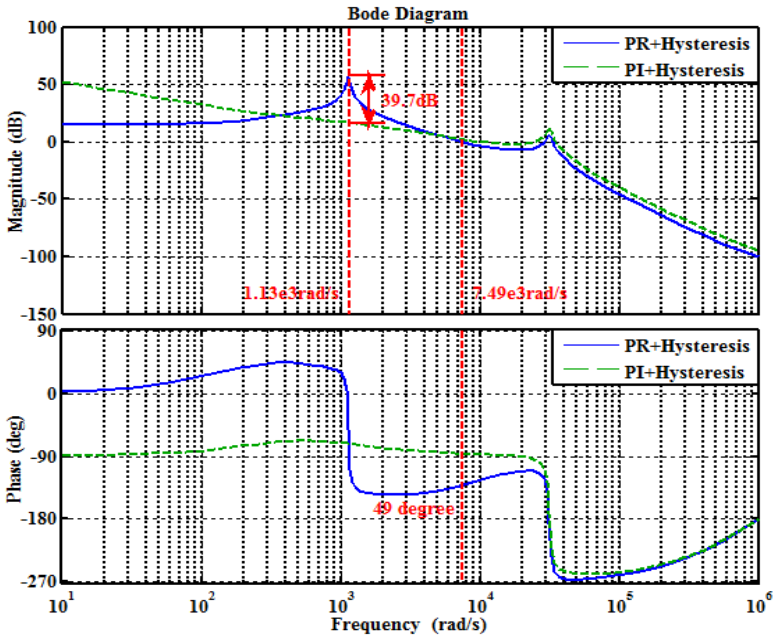


Figure 4.11: Bode plots of open loop transfer function with PR control.

$$G(s) = \frac{ki_{grid}(s)}{i_{\_ref}(s)} = kG_{HCC}(s)G_{filter}(s)[G_{PR}(s)+1] \tag{4.21}$$

Through them, it is known that the PR control provides high gain at the specific resonant frequency while tuning 3rd low frequency harmonic. Compared with PI control, there is gain boost at the resonant frequency.

The transfer function $G_{dis}(s)$ between the disturbance $\Delta i_{L1}(t)$ and grid current $i_{grid}(t)$ can be expressed below and the bode plots is shown in Figure 4.12 where there is the same gain reduction at the specific resonant frequency.

$$G_{dis}(s) = \frac{i_{grid}(s)}{\Delta i_{L1}(s)} = \frac{G_{filter}(s)}{1+kG_{HCC}(s)G_{filter}(s)G_{PR}(s)} \tag{4.22}$$

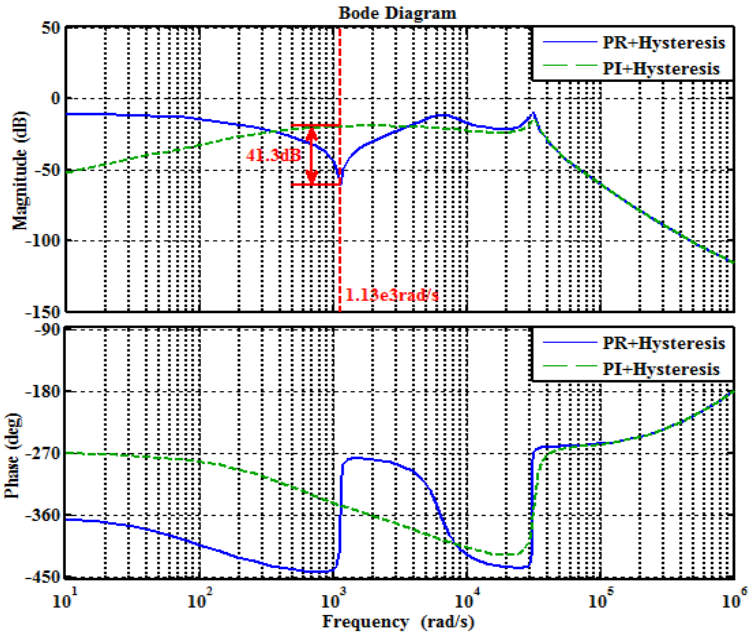


Figure 4.12: Bode plots of transfer function $G_{dis}(s)$ with PR control.

In the original unipolar hysteresis current control, since there are several different low frequency harmonics in the grid current, the PR controller designed for different

resonant frequency can be in parallel to mitigate the respective harmonic components. The open loop transfer function and bode plots can behave like (4.23) and Figure 4.13 where it is observed that both the bandwidth and phase margin are increased by introducing multi-PR control in parallel.

$$G_{PR\_multi}(s) = \sum_{k=3,5,7,9,11\ldots} k_{pk} + \frac{2k_{ck}\omega_{ck}s}{s^2 + 2\omega_{ck}s + \omega_{0k}{}^2} \tag{4.23}$$

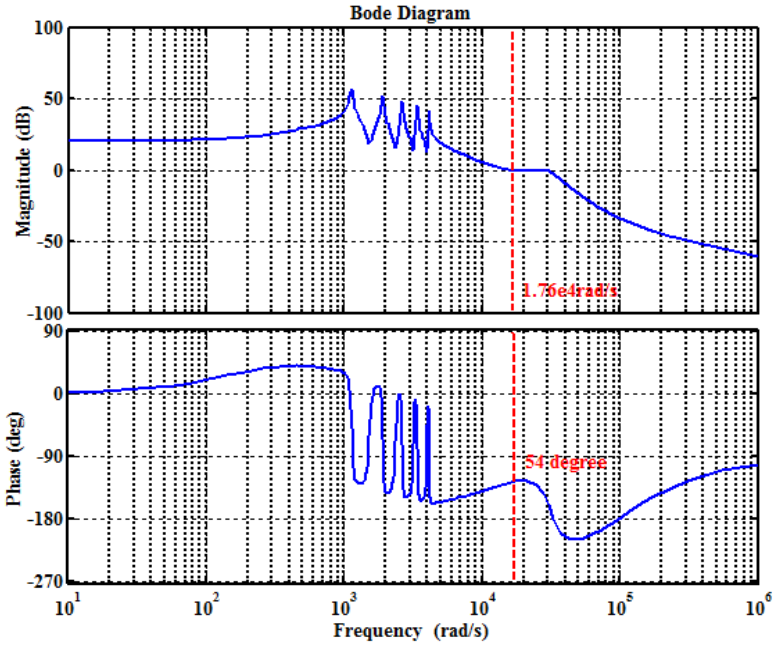


Figure 4.13: Bode plots of open loop transfer function with multi-PR control in parallel.

In practical design, given the disturbance $\Delta i_{L1}(t)$ is related to the behaviors of hysteresis current controller and delays as mentioned previously, the multi-PR control can change $\Delta i_{L1}(t)$ except mitigating the harminics at resonant frequencies. Then other unexpected harmonics can be introduced into the actual output inductor current $i_{L1\_actual}(t)$ and deteriorate the grid current. Therefore, the multi-PR control doesn't definitely mean better low frequency harmonics mitigation and the performance should be evaluated

through experiments as well. The similar problem also exists while replacing the PR control with the repetitive control [151]. It is totally possible that the quality of grid current can have limited improvement or even be worsened. What's more, while minimizing the influence of delays from the digital controller, the sampling frequency should be maximized which means a lot of memories occupied by the repetitive control algorithm. That is also one of the reasons that repetitive control isn't an appropriate option in this application.

4.7 Simulation and experimental results

A simulation model is built up with Multisim and LabVIEW co-simulation to verify effectiveness on the proposed PR and hybrid hysteresis current control with soft switching in dc-ac inverter of the two stage PV microinverters. Figure 4.14 shows the simulation waveforms of the output inductor current $i_{L1}(t)$ and the generated driving signals in unipolar hysteresis current control without zero-crossing optimization and low frequency harmonics mitigation. The halved switching frequency and soft switching operation of power devices are evident as is the smooth transition between ZVS and ZCS commutations as shown in the inset at the top right corner.

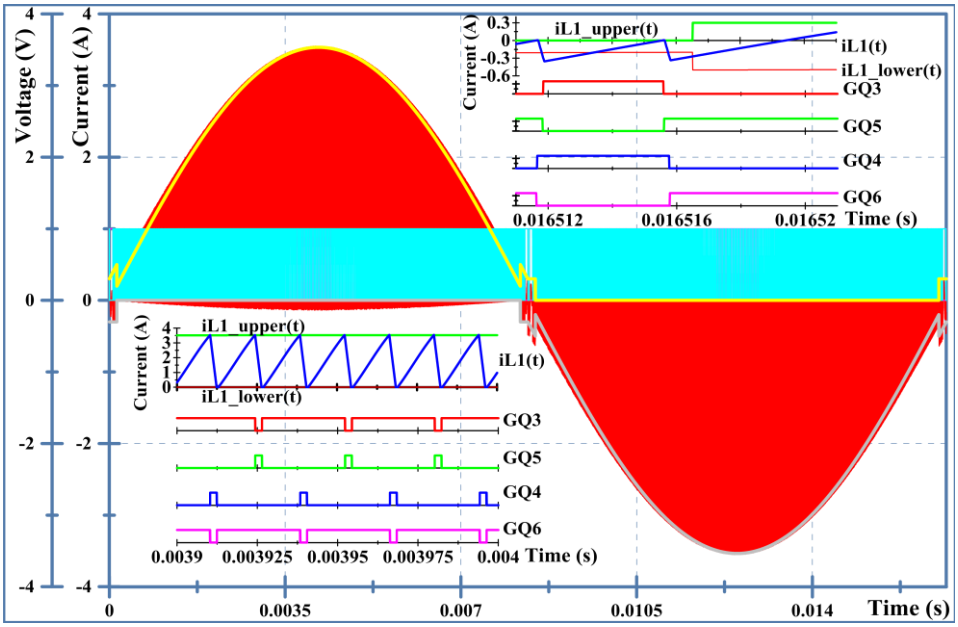


Figure 4.14: Simulation results of output inductor current $i_{L1}(t)$ and drving signals in unipolar hysteresis current control without zero-crossing optimization and low frequency harmonics mitigation.

The zero-crossing distortions due to 1us delays (10ns step size) is illustrated in Figure 4.15 where it is revealed that there is deviation between the grid current and the reference current as expected from (4.17). Thus, at the zero-crossing point, the grid current is still larger than zero and then there is sudden transition to negative value which inevitably generates current spikes and certain low frequency harmonics during the process.

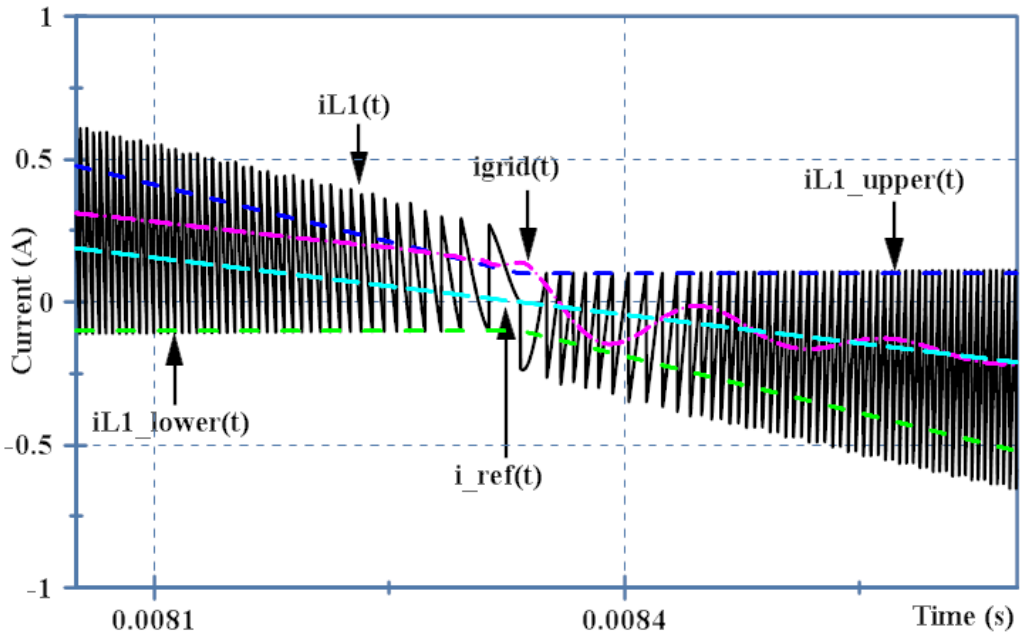


Figure 4.15: Zero-crossing distortions resulted from 1us delay.

In Figure 4.16, the zero-crossing distortions due to smaller slope of output inductor current $i_{L1}(t)$ than that of the reference current is shown. Take the condition $\omega t=\pi$ for example. It is observed that in the last switching period of the zero-crossing point, the falling down of $i_{L1}(t)$ behaves like oscillation. Likewise, at the first few switching periods after the zero-crossing point, the rising up of $i_{L1}(t)$ also has oscillation. Compared with the

theoretical analysis in Figure 4.9 mentioning that the output inductor current $i_{L1}(t)$ will fall down or rise up with calculated slopes in terms of the grid voltage and inductance of L_1 and L_2, the oscillations in $i_{L1}(t)$ from the simulation results worsen the quality of the grid current, and even result in current spikes and instability of the dc-ac inverter. Actually, the oscillations exists during the whole periods when the slope of the output inductor current $i_{L1}(t)$ is less than that of the reference current (the region marked with red arrow). The similar simulation results can be obtained at ωt=0 of Figure 4.16.

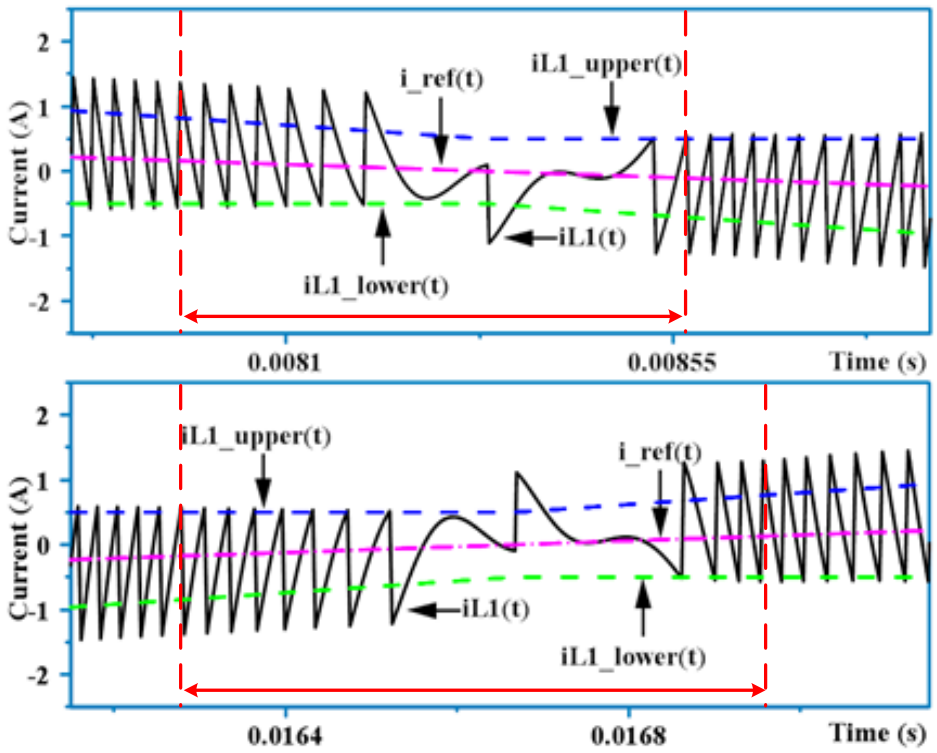


Figure 4.16: Zero-crossing distortions resulted from both delays and smaller slope of output inductor current through L_1 and L_2.

Figure 4.17 shows the simulation results of optimized zero-crossing distortions with hybrid hysteresis current control. Even though there is about 2us delay (10ns step

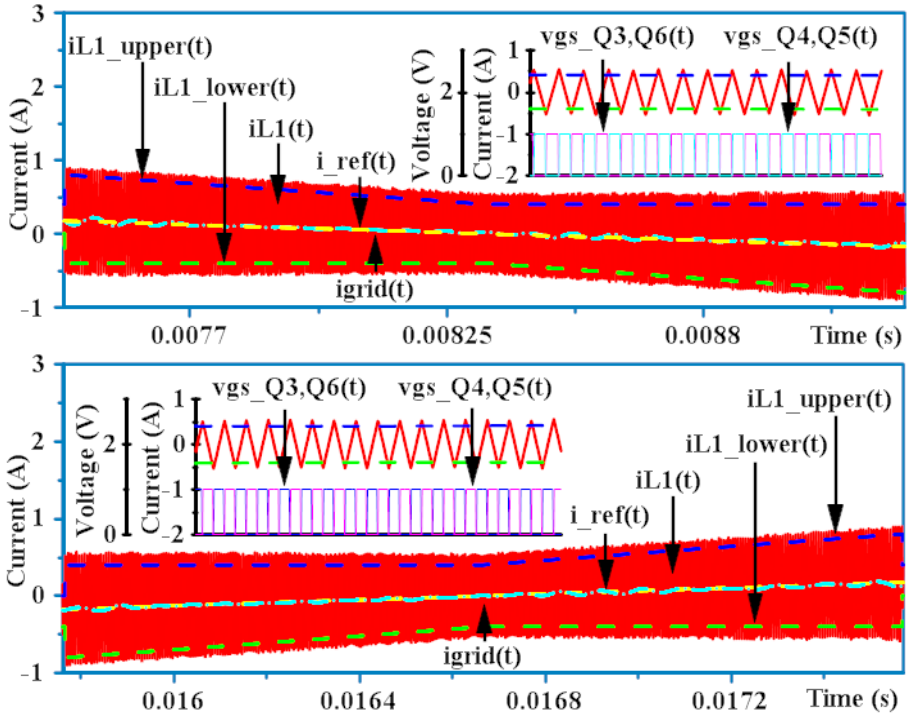


Figure 4.17: Simulation results using hybrid hysteresis current control to optimize zero-crossing distortions.

size), the grid current almosts follows the reference current by using bipolar modulation around zero-crossing points. The transitions around zero-crossing points are smooth, and the current spikes and oscillations can be eliminated. The simulation results of combined PR and hybrid hysteresis current control with soft switching in dc-ac inverter towards the two stage PV microinverters are shown in Figure 4.18 where it is observed that the grid current tracks the reference current well and is in phase with the grid voltage. The transitions of zero-crossing points and ZCS-ZVS commutations (or unipolar and bipolar modulation) are smooth and robust. The harmonic spectrums of the output inductor current $i_{L1}(t)$ are given in Figure 4.19 where it is revealed that by using combined PR and hybrid hysteresis current control, the low frequency harmonics (180Hz, 300Hz, etc) have been

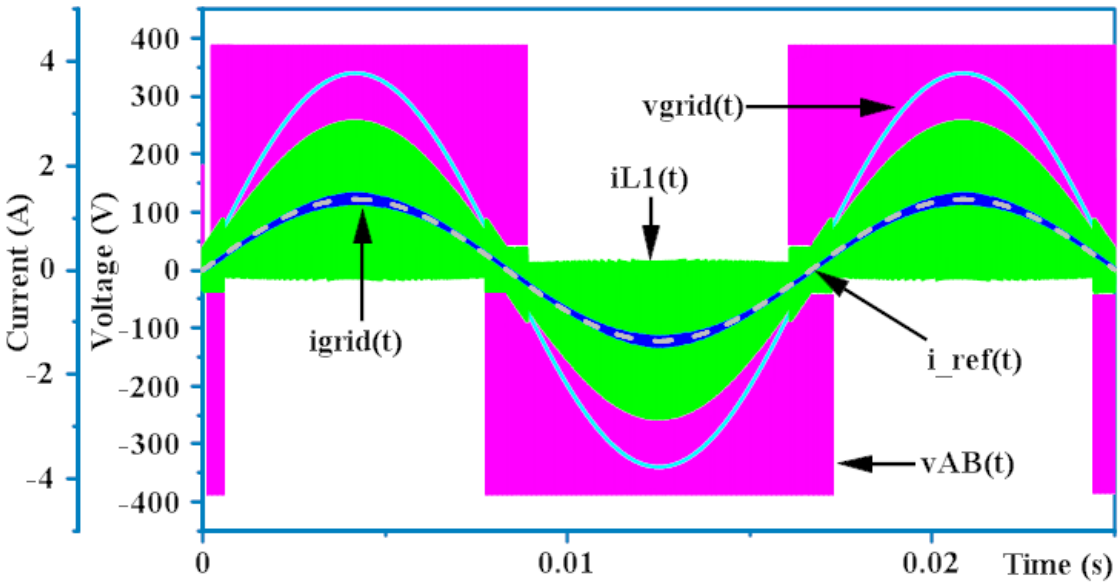


Figure 4.18: Simulation results of combined PR and hysteresis current control with soft switching in dc-ac inverter.

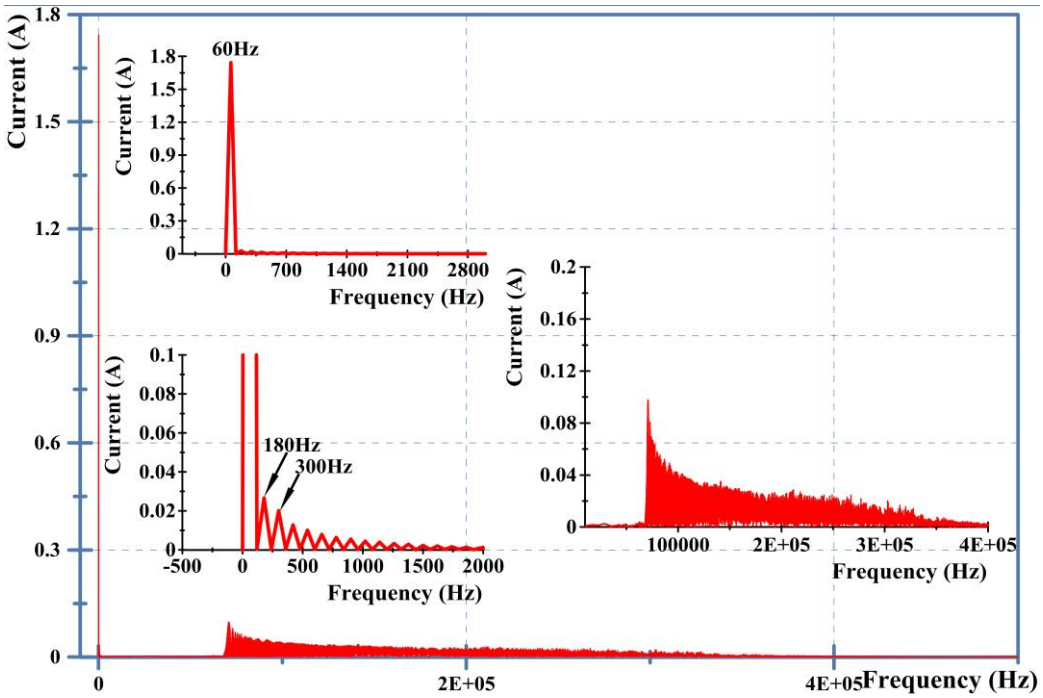


Figure 4.19: Harmonic spectrum of output inductor current $i_{L1}(t)$.

mitigated greatly. Due to the hysteresis operation, the harmonic spectrums are distributed over a range of frequencies as expected in (4.11) which results in the challenges while designing the output filter. But at the same time, it has potential advantages to meet conducted emissions limits.

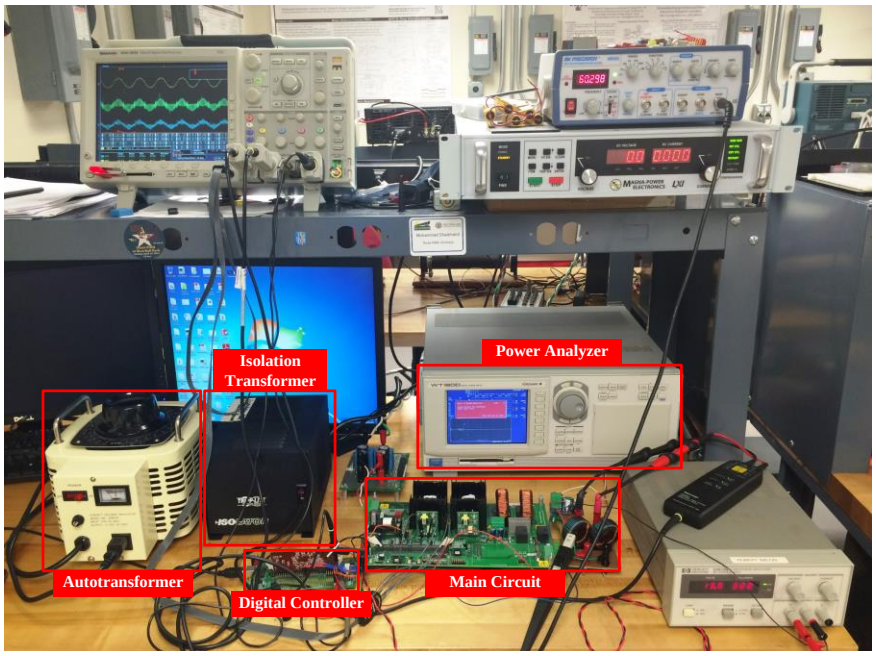


Figure 4.20: Experimental setup of laboratory-scale dc-ac grid-connected inverter.

The experimental setup of laboratory-scale dc-ac grid-connected inverter in the two stage PV microinverters are built up as shown in Figure 4.20 where, the combined PR and hybrid hysteresis current control with soft switching is implemented by TI TMS320F28335 microcontroller. The isolation transformer and autotransformer are used to achieve galvanic isolation between the main circuit and the grid, and adjust the grid voltage during experiments respectively. The electrical specifications of this prototype are

Table 4-2: Electrical Specifications of dc-ac grid-connected inverter in the two stage PV microinverters.

Input Voltage (V)	400	Output Inductor L_1, L_2 (uH)	300
Gird Voltage (split phase, RMS, V)	120	Output Capacitor C_{f1} (uF)	1u
Power (W)	200	Output Inductor L_3, L_4 (uH)	500
Sampling Frequency (kHz)	150	Output Capacitor C_{f2} (uF)	1u
Dead Time (us)	0.7	MOSFETs	IRFP460
k_p	1	k_c	400
ω_c (rad)	20	ω_0 (rad)	2π*180
t_{ZVS} (s)	1/720	I (A)	0.1~0.25

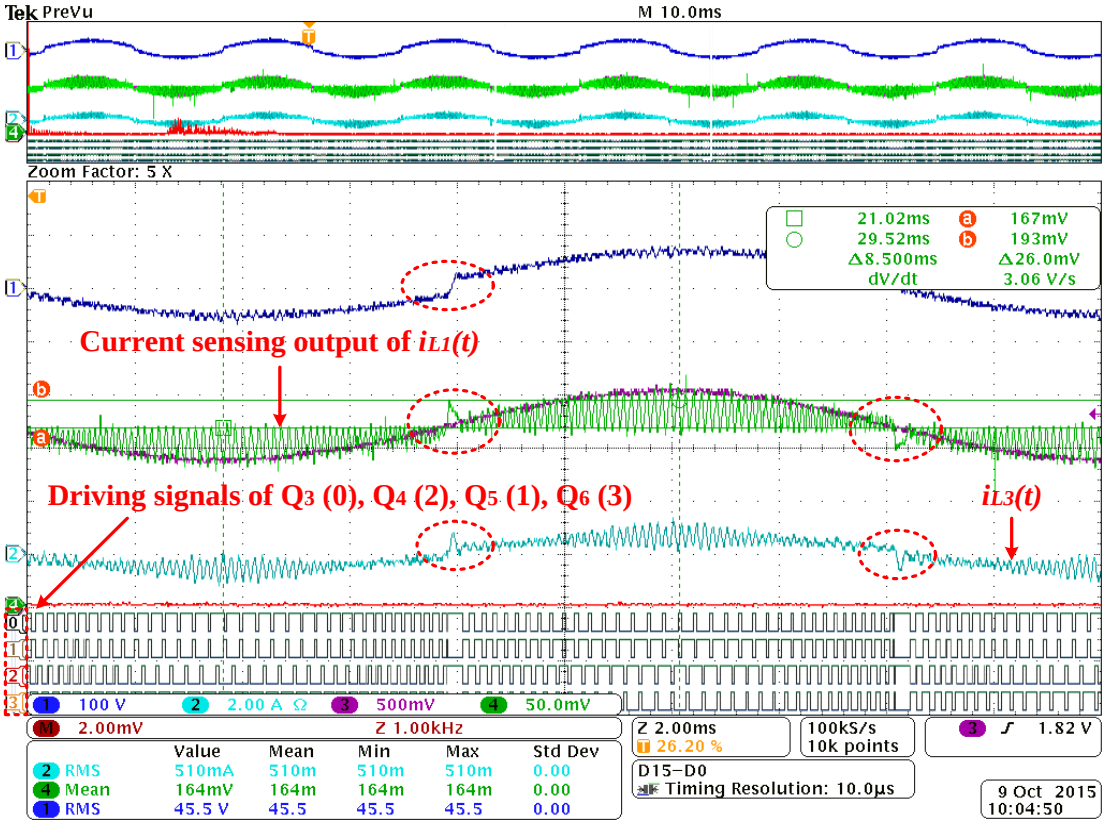


Figure 4.21: Experimental waveforms of unipolar hysteresis current control without zero-crossing optimization.

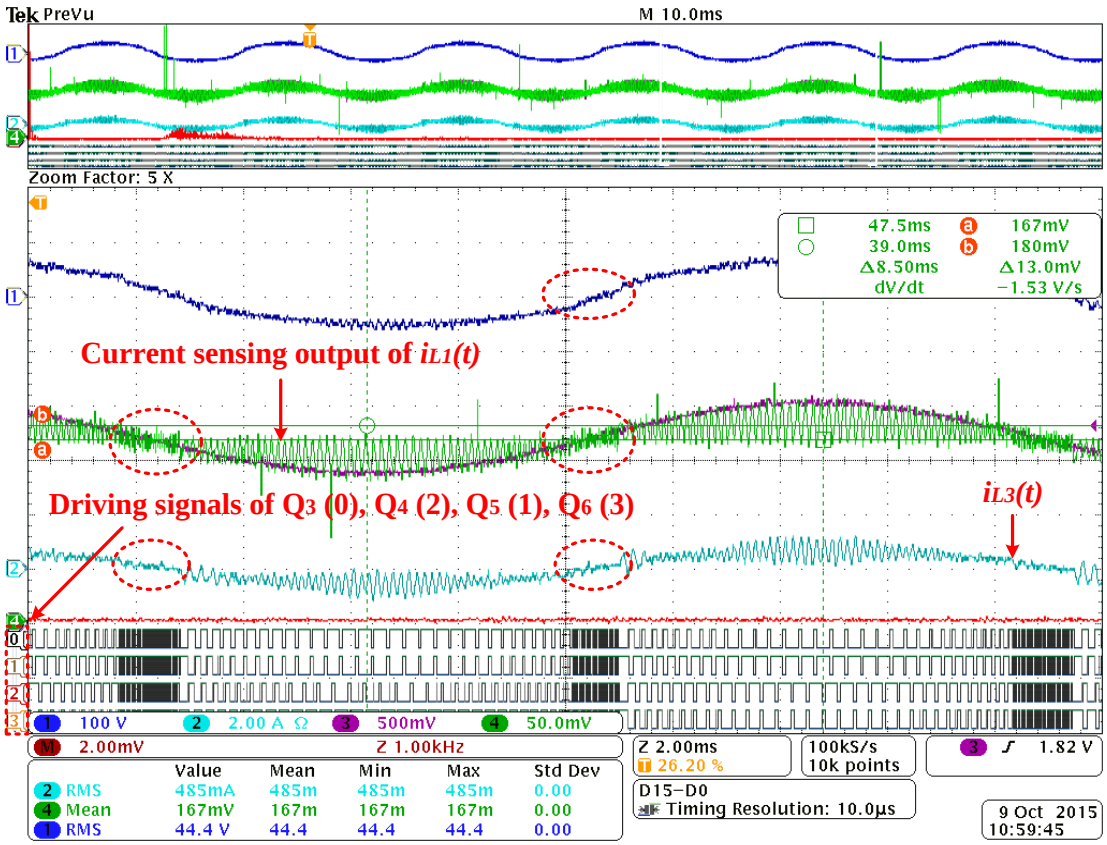


Figure 4.22: Experimental waveforms of zero-crossing optimization through hybrid hysteresis current control.

shown in Table 4.1. Since the 3rd harmonic is the main component in the grid current, there is only one PR control with 180Hz resonant frequency is applied. With the appropriate designs of k_p, k_c, ω_c and ω_0, both 3rd and other low frequency harmonics (mainly 5th, 7th, 9th) can be mitigated as well.

Figure 4.21 and 4.22 show the experimental waveforms without and with zero-crossing optimization respectively. Through comparison, it is concluded that the bybrid hysteresis current control can eliminate the current spikes at zero-crossing points

effectively which verifies the validity of the theoretical analysis and simulation results mentioned previously.

The ZVS turn-on around zero-crossing points is illustrated in Figure 4.23. The grid current harmonic analysis on low frequency harmonics mitigation through YOKOGAWA WT1600 Power Analyzer are given by Figure 4.24. From that, it is observed that even though the zero-crossing optimization can smooth the transition at zero-crossing points and reduce certain low frequency harmonics, there are still lots of 3^{rd}, 5^{th}, 7^{th}, and 9^{th} harmonics in the grid current. By combining with the PR control (180Hz resonant frequency), the low frequency harmonics, especially the 3^{rd} one, can be mitigated greatly to reduce total harmonic distortion (THD) of the grid current.

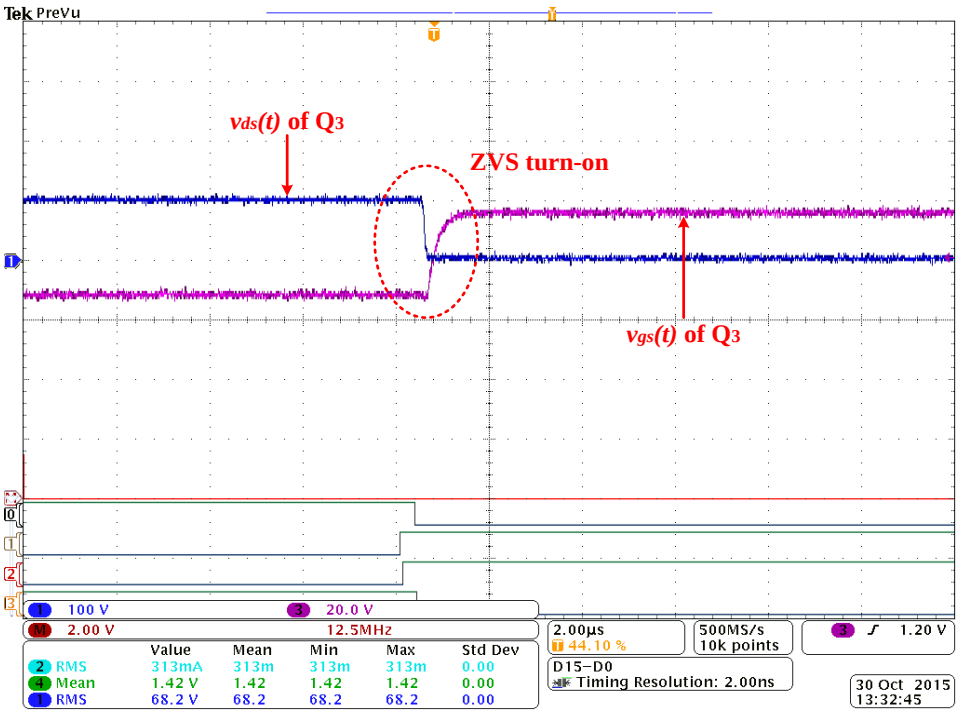
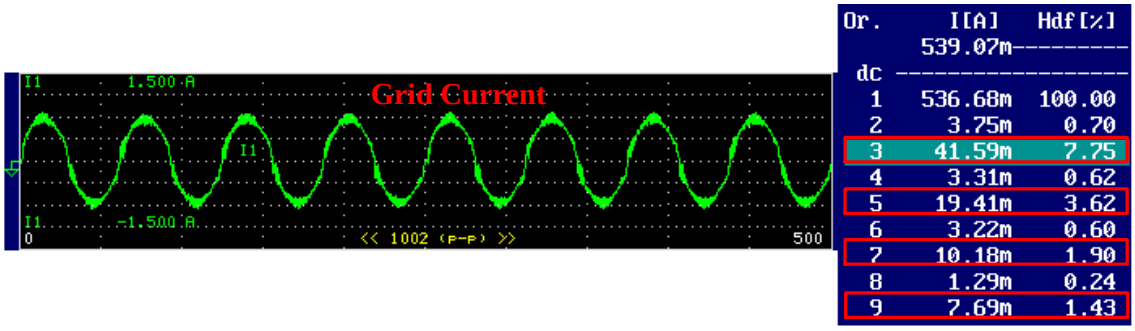
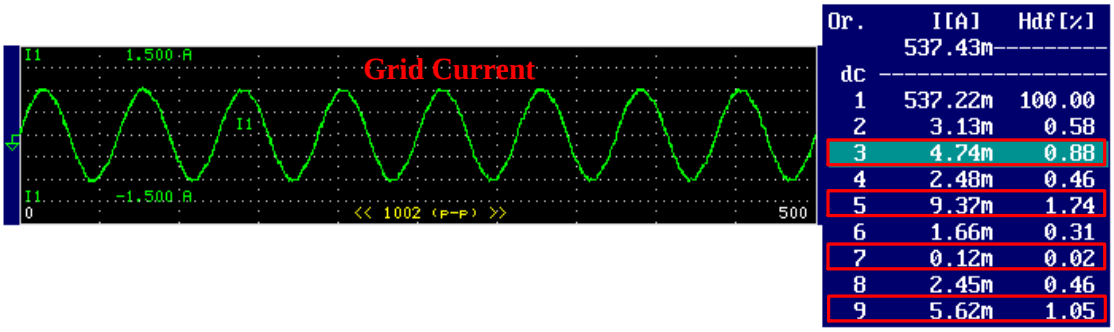


Figure 4.23: Experimental waveforms of ZVS turn-on of Q_3.



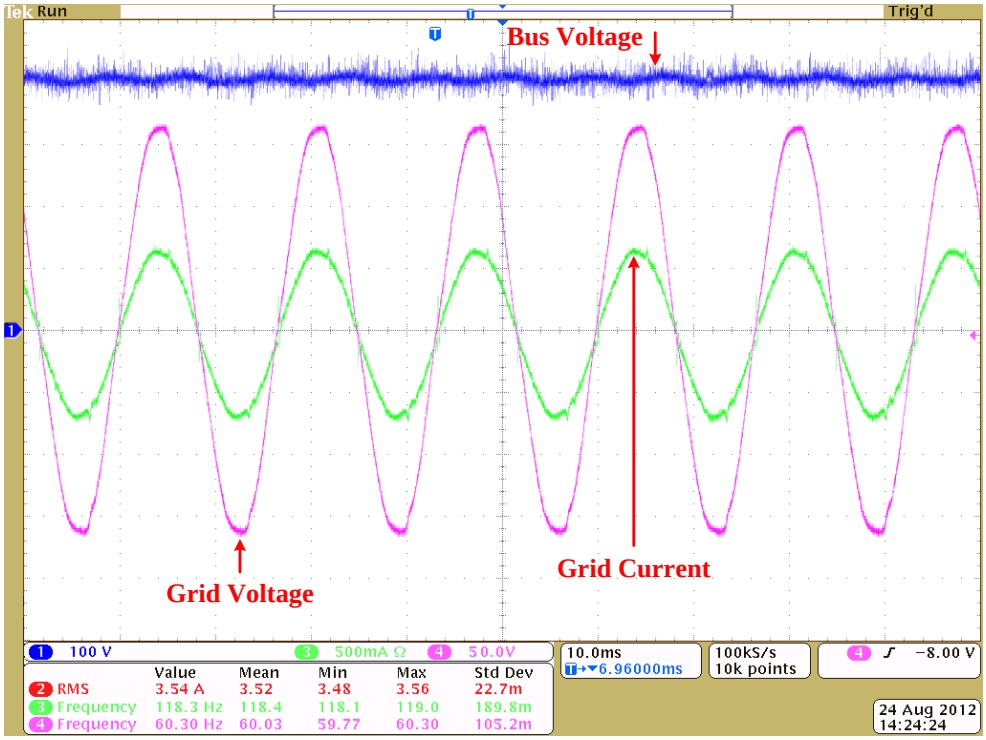
(a) Grid current harmonic analysis without the PR control



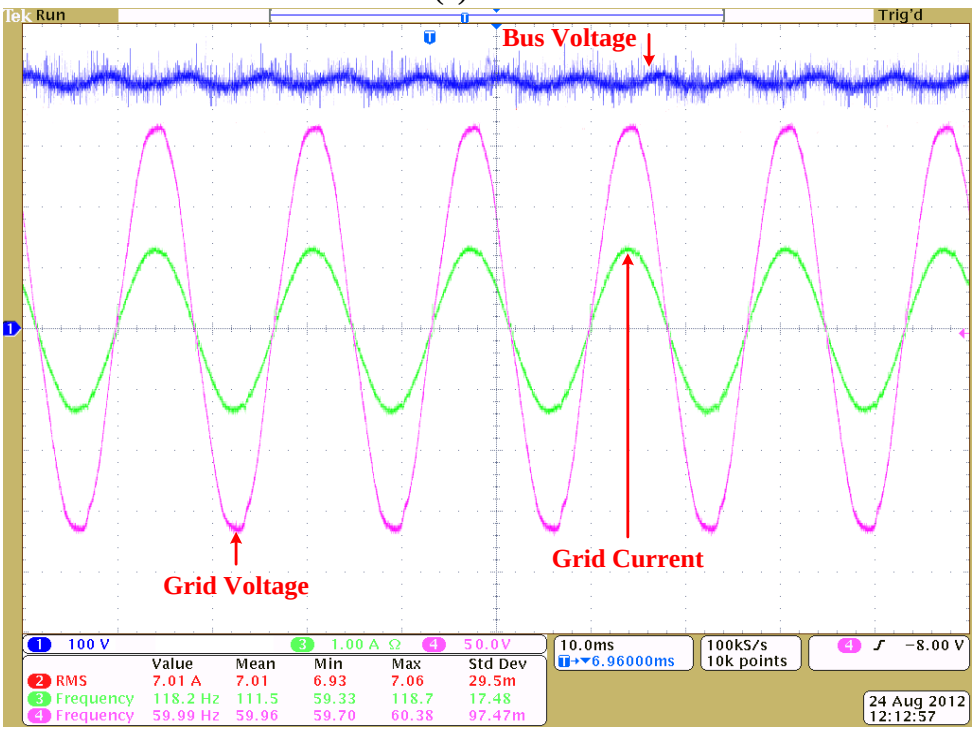
(b) Grid current harmonic analysis with the PR control (180Hz resonant frequency)

Figure 4.24: Experimental waveforms of zero-crossing optimization through hybrid hysteresis current control.

The experimental waveforms of proposed PR and hybrid hysteresis current control with soft switching in dc-ac inverter towards the two stage PV microinverters at about 55W and 110W output power are shown in Figure 4.25. Through that, it is revealed that the grid current is always in phase with the grid voltage and has smooth transition at zero-crossing points. Due to the inherent instantaneous power imbalance in single phase inverter, there are double line frequency ripple on the bus voltage. The THDs at different output power ratings are plotted in Figure 4.26 where it is concluded that through zero-crossing optimization and low frequency mitigation, the THD of grid current in the dc-ac grid-connected inverter can be limited to be less than 5%. The efficiency comparisons shown in Figure 4.27 between the bipolar hysteresis current control with soft switching



(a) 55W



(b) 110W

Figure 4.25: Experimental waveforms of dc-ac grid-connected inverter with proposed PR and hysteresis current control strategy.

and the proposed PR and hybrid hysteresis current control with soft switching, verifies the increased efficiency (maximum 1.3%) due to halved switching frequency of power devices while operating at unipolar modulation. In this prototype, since the conduction losses of power devices, power losses from gate drivers and output inductors (both core losses and copper losses) aren't optimized, the proportion of switching losses of power devices in total power losses is small. If the overall power losses can be reduced further, the efficiency improvement of the proposed PR and hybrid hysteresis current control with soft switching can perform much better than that of bipolar hysteresis current control with soft switching.

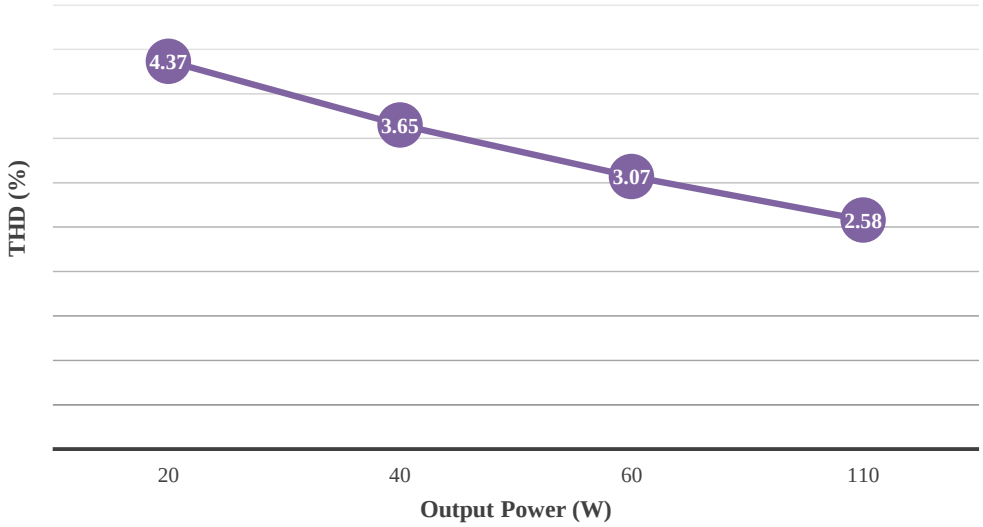


Figure 4.26: THDs at different output power ratings of dc-ac grid-connected inverter with proposed PR and hybrid hysteresis current control strategy.

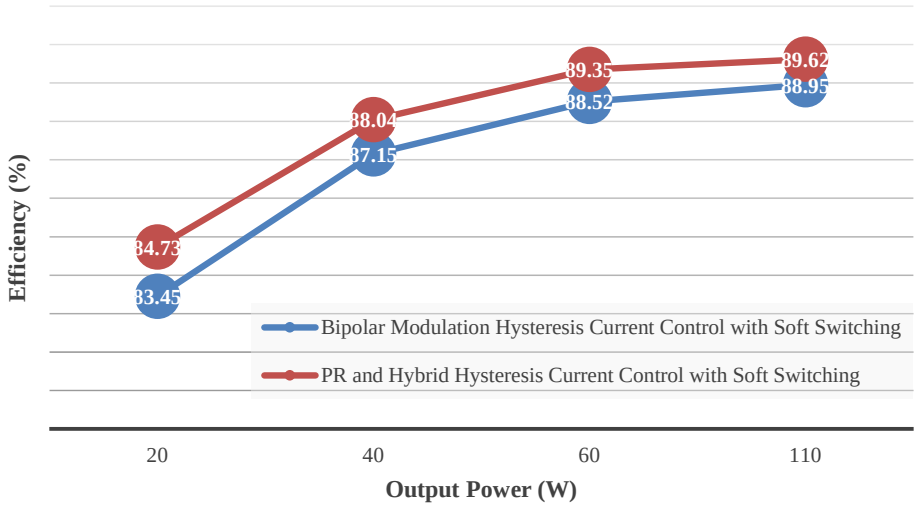


Figure 4.27: Dc-ac grid-connected inverter efficiency comparison between bipolar hysteresis current control with soft switching and combined PR and hybrid hysteresis current control with soft switching.

4.8 Summary

This section presents combined PR and hysteresis current control strategy with soft switching in dc-ac inverter of the two stage PV microinverters. By controlling output inductor current $i_{L1}(t)$ within the designed hysteresis bands cycle by cycle, within ZVS commutation reigon, ZVS turn-on of all power devices can be achieved; within ZCS commutation reigon, ZVS turn-on and ZCS turn-off of Q_4 and Q_5 in positive half cycle (Q_3 and Q_6 in negative half cycle) can be satisfied. Thus the switching losses of power devices can be reduced greatly compared with conventional hard switching operation. At the same time, given the current ratings in PV micorinverters, the core and copper losses of output inductor L_1 and L_2 only have limited increase through appropriate magnetic design. Thus the toal power losses can be reduced. Compared with bipolar hysteresis current control, the proposed control strategy has increased efficiency (maximum 1.3%).

To optimize the zero-crossing distortions resulted from the delays and smaller slope of output inductor current $i_{L1}(t)$ than that of reference current around zero-crossing points, the hybrid hysteresis current control, which enables bipolar modulation around the zero-crossing points to minimize the zero-crossing distortion and unipolar modulation in other moments of the line cycle to achieve halved switching frequency of power devices, is proposed. To further mitigate the low frequency harmonics of grid current, PR control is applied to minimize the steady state error at low frequency. Finally, the THD of grid current can be limited to be less than 5%.

5. CONCLUSIONS AND FUTURE WORKS

5.1 Summary and conclusion

This dissertation presents the eGaN FETs based topology for the front-end dc-dc converter, and combined PR and hybrid hysteresis current control with soft switching for dc-ac inverter in the two stage PV microinverters. At the same time, the double line frequency power decoupling techniques for single phase inverters have been investigated. Major contributions of this dissertation can be summarized as follows:

1. A high step-up front-end resonant dc-dc converter with simple topology, less power devices counts, easy-to-implement control strategy is firstly proposed in this dissertation. The high voltage gain is achieved by boost operation, high frequency transformer and voltage doubler rectifier together to avoid extreme duty ratio of power devices and turn ratio of high frequency transformer. The resonant tank allows ZCS of rectifier diodes (D_1 and D_2), ZVS of Q_1 and conditional ZVS of Q_2. Due to small inductance, the resonant inductor can be integrated into the high frequency transformer.

2. eGaN FETs from EPC are applied to replace the conventional silicon based MOSFETs due to low conduction resistance, low capacitance, high power density, etc. Since there is no intrinsic anti-parallel body diodes like conventional silicon-based MOSFETs, the reverse conduction characteristics of eGaN FETs are explored. To optimize the reverse conduction power losses and avoid shoot-through current in single phase leg structure, overlapped driving signals for eGaN FETs are proposed. The choose

of crossing voltage towards the overlapped driving signals are illustrated and the efficiency improvement is verified.

3. Combined with FEA and Labview/Multisim thermal model simulation, the simplified thermal resistor model can be used to evaluate the cooling requirements and estimate the minimum board size for heat dissipation of eGaN FETs under worst case scenario.

4. The general solutions (Solution i, ii and iii), unifies all possible waveforms of energy storage components to achieve double line frequency power decoupling, are derived and discussed. The energy utilization efficiency η_E and voltage ripple factor η_r are introduced to evaluate the three solutions. Both parallel and series power decoupling techniques are investigated by considering the ripple power paths.

5. The general configuration of parallel power decoupling in the two stage PV microinverters is explored. The evaluations on the component counts, the energy utilization and voltage/current ripple of energy storage components, the dc voltage utilizations of both the main and power decoupling circuit, and the current stresses of power devices in the main circuit are summarized to provide guidance on the design of power decoupling in the two stage PV microinverters.

6. Benefiting from fast dynamic response and robust current regulation, the proposed unipolar hysteresis current control is used to achieve halved switching frequency of power devices and soft switching operation of H-bridge dc-ac inverter without additional components. Compared with hard switching operation, the switching losses are reduced greatly at the cost of limited increase of power losses towards output inductor L_1 and L_2.

The frequency distributions on different parameters of the control strategy are investigated.

7. The analysis and solutions on zero-crossing distortions in original unipolar hysteresis current control are discussed. The hybrid hysteresis current control, which enables bipolar modulation around the zero-crossing points to minimize the zero-crossing distortions, and unipolar modulation in other moments of the line cycle to achieve halved switching frequency of power devices, is proposed.

8. The digital PR control is introduced to be combined with hybrid hysteresis current control to mitigate the low frequency harmonics of the grid current without complicated predictive calculations.

5.2 Future works

1. Explore the operation of GaN high-electron mobility transistors (HEMTs) in the dc-ac inverter with higher switching frequency and power density.

2. Implement and test the two stage PV microinverters with both eGaN FETs based front-end resonant dc-dc converter and GaN HEMTs based dc-ac inverter using proposed PR and hybrid hysteresis current control strategy.

3. Work on the power decoupling of double line frequency ripple power in the single phase two stage PV microinverters.

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