

A NEW HIGH POWER DENSITY MODULAR MULTILEVEL DC-DC  
CONVERTER WITH LOCALIZED VOLTAGE BALANCING CONTROL FOR  
ARBITRARY NUMBER OF LEVELS

A Thesis

by

YONG ZHOU

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Chair of Committee,	Prasad Enjeti
Committee Members,	Robert S. Balog
	Shanker P. Bhattacharya
	Duncan Henry M. Walker
Head of Department,	Miroslav M. Begovic

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## ABSTRACT

A new modular multilevel DC-DC converter (MMC) with high power density and simplified localized voltage balancing control is proposed. Converter building block and controller module are built separately considering level propagation for each row. In the proposed configuration, the converter building blocks with the same power handling capability are connected in parallel in each row. This leads to a triangular structure from top to bottom. Converter building block consists of integrated H-bridge and mutually coupled inductors whose total current is nearly ripple free. These features are shown to reduce the voltage ripple of DC-link capacitors significantly, leading to a smaller capacitance and size. An optimized control algorithm with voltage feedback PI loop is proposed, resulting in the elimination of current sensors. Thus, the overall system complexity is reduced and the cost-effectiveness is increased. Significant ripple reduction of the inductor current and capacitor voltages is observed based on the simulation and prototype of a 5-level system. With a fully modular power stage module and localized control module, a system which has arbitrary number of level can be built by stacking the modules, thereby contributing to enhanced system redundancy.

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## TABLE OF CONTENTS

ABSTRACT .....	ii
ACKNOWLEDGEMENTS .....	iii
TABLE OF CONTENTS .....	iv
LIST OF FIGURES.....	vi
LIST OF TABLES .....	ix
1. INTRODUCTION AND LITERATURE REVIEW .....	1
1.1 Introduction .....	1
1.1.1 Application of Higher Power Rating Conversion .....	2
1.1.2 Power Density of Converters .....	3
1.2 Literature Review .....	4
1.2.1 Modular Multilevel Converter (MMC) Topologies .....	4
1.2.2 Modulation, Control Algorithm and Operation Characteristic .....	8
1.2.3 Research Objective.....	12
2. MODELLING OF PROPOSED CONFIGURATIONS.....	14
2.1 Introduction .....	14
2.2 Modelling Building Block of Half-bridge with Single Inductor.....	15
2.3 Modelling Building Block of H-bridge with Mutually Coupled Inductor .....	20
2.3.1 State Space Equation Derivation.....	21
2.3.2 Self-inductance of Mutually Coupled Coils.....	25
2.3.3 Energy Stored in Mutually Coupled Coils .....	26
2.4 Advantages and Disadvantages of New Configuration.....	28
3. OPEN LOOP SIMULATION VERIFICATION .....	30
3.1 Introduction .....	30
3.2 Design Example .....	30
3.3 Open Loop Simulation .....	31
4. CLOSED LOOP CONTROL ALGORITHM DESIGN .....	36
4.1 Design Consideration .....	36
4.2 Compensation Network Design .....	37

4.3 Closed Loop Simulation.....	40
5. HARDWARE IMPLEMENTATION .....	45
5.1 Power Stage Building Block Implementation/PCB Design .....	45
5.1.1 Component Selection .....	45
5.1.2 Printed Circuit Board (PCB) Design .....	47
5.2 Controller Module Implementation/PCB Design.....	48
5.3 Prototype System and Experimental Result .....	50
6. CONCLUSION AND FUTURE WORK.....	56
6.1 Conclusion.....	56
6.2 Future Work .....	56
REFERENCES .....	58

## LIST OF FIGURES

	Page
Figure 1-1 Conventional 3-level voltage source neutral point clamp (NPC) converter [4] (©2015 IEEE) .....	3
Figure 1-2 Schematic diagram of a typical three-phase MMC [7] (©2015 IEEE) .....	5
Figure 1-3 Popular SM/cell structures: (a) half bridge, (b) full bridge, (c) clamp double, (d) three phase FC - flying capacitor, (e) three phase NPC – neutral point clamp, (f) five level cross-connected SM (©2015 IEEE) .....	6
Figure 1-4 Proposed bidirectional TMMC and its SM in [8] (©2015 IEEE) .....	8
Figure 1-5 Multilevel carrier waveforms (a) PD, (b) POD, (c) APOD, (d) Saw-tooth rotation, (e) Phase shifted carriers [15] (©2009 IEEE) .....	10
Figure 2-1 Conventional buck converter circuit.....	14
Figure 2-2 Two building blocks for MMC power stage module: (a) Half-bridge with single inductor, (b) H-bridge with mutually coupled inductors .....	15
Figure 2-3 Five level step down (5:1) MMC DC-DC converter. (a) Detailed Circuit Diagram. (b) Building block of half-bridge with single inductor. (c) Circuit block diagram .....	16
Figure 2-4 Waveforms of state variables from Matlab state-space toolbox based on a 5-level example .....	19
Figure 2-5 Five level step down (5:1) MMC DC-DC converter. (a) Building block of H-bridge with mutually coupled inductor. (c) Circuit block diagram.....	20
Figure 2-6 Waveforms of state variables from Matlab state-space toolbox based on a 5-level example for the new configuration.....	24
Figure 3-1 PSIM open loop simulation circuit of the five-level new configuration design example .....	32
Figure 3-2 Capacitor voltage waveform.....	32
Figure 3-3 Total inductor current for all building blocks of each row.....	33
Figure 3-4 Separate coil current of the mutually coupled inductors .....	33

Figure 3-5 (a) Total current; (b) Current difference waveforms of certain mutually coupled inductors.....	34
Figure 3-6 Input current waveform from power supply .....	34
Figure 4-1 Block diagram of the whole system with converter building blocks and localized controller modules.....	36
Figure 4-2 TMMC (a) Outer voltage loop; (b) Internal current loop [8] (©2015 IEEE) .	38
Figure 4-3 Close-loop control algorithm for each row.....	40
Figure 4-4 PSIM close loop simulation circuit of the five-level design example.....	41
Figure 4-5 Capacitor voltage waveform.....	42
Figure 4-6 Total inductor current for all building blocks of each row .....	42
Figure 4-7 Separate coil current of the mutually coupled inductors .....	43
Figure 4-8 (a) Total current; (b) Current difference waveforms of certain mutually coupled inductors.....	43
Figure 4-9 Input current waveform from power supply.....	44
Figure 5-1 PCB of power stage building block. 1) Mutually coupled inductors/ common mode choke; 2) Integrated H-bridge IRSM505-084; 3) Film Capacitor; 4) Voltage regulator; 5) Voltage sensor and divider.....	47
Figure 5-2 PCB of controller module. 1) Microchip dsPIC33FJ06GS102A MCU; 2) ADC input; 3) 4-channel PWM outputs for H-bridge; 4) Voltage regulator from 15V to 3.3V; 5) PICKit 3 debugger connection .....	50
Figure 5-3 The 4-level prototype system .....	51
Figure 5-4 Capacitor voltage waveform $V_{c1}$ and $V_{c2}$ .....	52
Figure 5-5 Capacitor voltage waveform $V_{c3}$ and $V_{c4}$ .....	52
Figure 5-6 Total current of single coupled inductors for each row.....	53
Figure 5-7 Current waveform of single winding for coupled inductors at each row .....	53
Figure 5-8 Current waveforms of each winding for coupled inductors at 1st row .....	54
Figure 5-9 Current difference of coupled inductors at each row .....	54

Figure 5-10 Output current of DC power supply .....55

## LIST OF TABLES

	Page
Table 1-1 Comparison of various SM/cell circuits [7] (©2015 IEEE) .....	7
Table 2-1 Stored energy comparison between the three configurations .....	27
Table 3-1 A detailed design example of the new configuration.....	31
Table 5-1 Major component selection for the power stage building blocks .....	46

# 1. INTRODUCTION AND LITERATURE REVIEW

## 1.1 Introduction

The growth of electricity demand has been increasing from 1950 even the annual rate of growth has dropped from peak 9.8% (from 1949 to 1959) to only 0.7% in the first decade of the 21st century based on the U.S. Annual Energy Outlook [1]. It shows this trend in a 3-year moving average. Among this huge electricity demand, the majority is generated from fossil fuels, like coal and natural gas. However, the usage of renewables, such as photovoltaic, wind turbine, biomass, is rising consistently. The United States' Department of Energy (DoE) predicts that as a proportion of total electricity supply, renewable energy sources will contribute almost 20% in the year 2050 compared to 12% in 2010 (NREL report [2]).

In order to maximize the power that can be utilized, two aspects are taken into consideration: electricity transmission, power conversion. From the power transmission perspective, conventional AC transmission system has lower efficiency because of skin effect and the existence of unwanted capacitance and inductance. Siemens describes the power grid of the future as “must be secure and enable economic power transmission as well as environmental friendly power transmission” [3]. HVDC is a realistic technical and economic alternative to AC transmission, especially preferred if power delivery is over long distance via cables. Coincidentally, most of the renewable resources (offshore wind farms, large scale PV farms) are located far away from living area. Additionally, the DC characteristics of HVDC transmission makes it a perfect candidate for the grid interface

of renewable energies. In this case, bulky and pricy transformers in conventional AC transmission are not required. From the power conversion perspective, especially in some high voltage/current situations, the objective is to process maximum power with the highest efficiency and reliability, at the smallest footprint and cost. Take the conventional buck DC-DC topology as an example, when the input voltage or power processing is increasing, the size of passive components will be very significant and series or parallel of switch devices will be required because of the unavailability of single device with such high voltage/current ratings. This would weaken the reliability and power density of the whole system. With this background, a lot of research has been done on modular multilevel converters (MMCs). Its standardized and optimized design makes it popular in high-power and medium-power communities.

### *1.1.1 Application of Higher Power Rating Conversion*

In some applications, like large battery storage system, PV farm or data center, large amount of power is processed. Figure 1-1 shows a conventional 3-level voltage source neutral point clamp (NPC) converter, the classical nominal voltages for power transistors in high voltage level application could be several thousand volts [4]. In practice, a large number of transistors have to be placed in series. However, in order to avoid excessive stressed on one individual component, this large stack of series switches need to have nearly identical parameters and synchronized ignition. This weakens the reliability of the whole system. This restriction brings a new idea to our sight: using many identical

units with same power ratings to process partial of the whole system power. This technological breakthrough is called the modular multilevel converter (MMC).

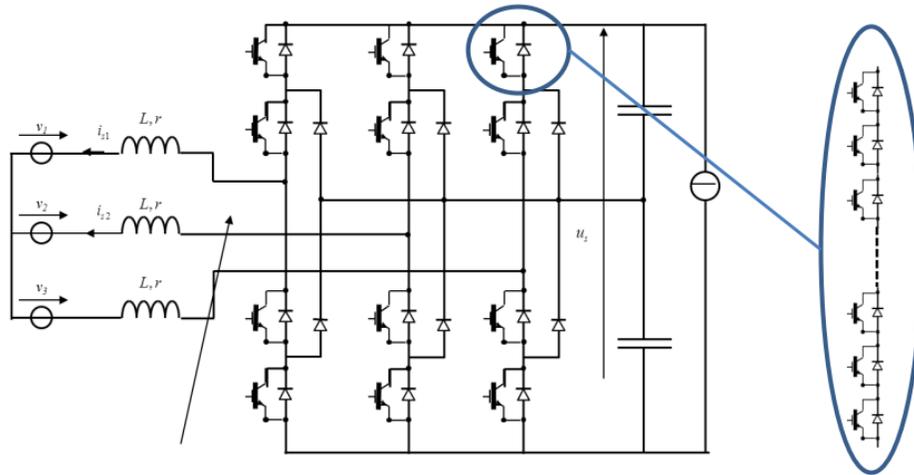


Figure 1-1 Conventional 3-level voltage source neutral point clamp (NPC) converter [4]

(©2015 IEEE)

### 1.1.2 Power Density of Converters

Power density of a converter can be defined as (1.1) [5]:

$$\text{Power Density} \left( \frac{W}{m^3} \right) = \frac{\text{Total Power Processed (W)}}{\text{Total Volume (m}^3\text{)}} \quad (1.1)$$

Alternately, some density is defined as power-to-mass or power-to-weight ratio. This definition is used often in cases with fossil fuels. For power electronics systems, equation (1.1) can be applied in most cases when talking about power density. Advantages of achieving higher power density are: reduced volume/weight, simpler transportation and installation, lower cost, etc. One conclusion from Emerson data center power supply report is “Higher Density = Lower Cost” [6].

A typical power conversion scheme contains the following major components: power switch devices (MOSFETs, IGBTs, etc.), passive components (inductors, capacitors, etc.), heat sinks and power transformers (galvanic isolation case). Generally, power transformer can occupy large space if it is used. Otherwise, passive components will be the major factor determining the power density of the whole system.

## **1.2 Literature Review**

Over the past few years, a lot of research has been done to address the technical challenges associated with the operation and control of modular multilevel converters (MMCs) [7], especially in high voltage (HV) and medium voltage (MV) applications. Fully modular converters are suitable for industrial applications whose power rating varies in a wide range. Generally, several advantages of modular multilevel converters are: 1) “one time for all design” which is convenient for propagation; 2) predictive voltage and current stressed for components by incorporation of identical modules in series or parallel; 3) higher power density and better thermal management due to optimized design of each module and optimal combination of different modules; 4) reduced design, manufacturing, installation and maintenance costs due to the design standardization, etc. This review part will cover the following concerns: topology, modelling, control, operation characteristic and application.

### *1.2.1 Modular Multilevel Converter (MMC) Topologies*

The schematic diagram of a typical three-phase MMC is shown in Figure 1- 2.

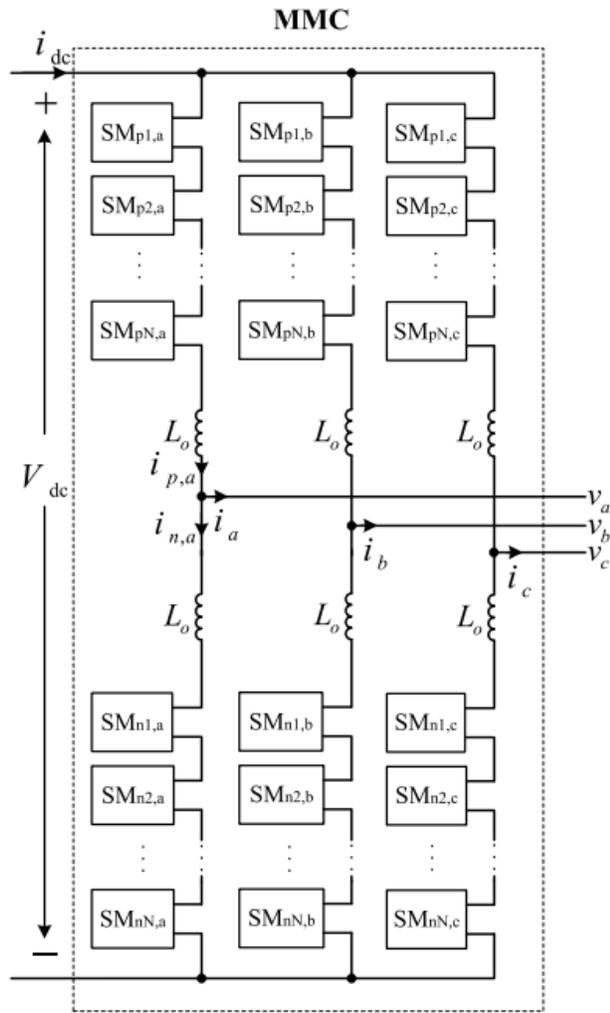


Figure 1-2 Schematic diagram of a typical three-phase MMC [7] (©2015 IEEE)

This structure consists of two arms per phase leg where each arm comprises  $N$  series-connected, nominally identical submodules (SMs), and a series inductor  $L_o$ . While the SMs in each arm are controlled to generate the required ac phase voltage, the arm inductor suppresses the high-frequency components in the arm current. The upper (lower) arm of three phase-legs are represented by subscript “p” (“n”). Each submodule is identical to each other. The desired output voltage waveform is obtained by setting the operation

sequence of each leg. For each submodule/cell, six popular structures are shown in Figure 1-3, (a) to (f), separately. The detailed output voltage levels cases are discussed in detailed in [7]. A comparison of various SM circuits, in terms of voltage levels, dc-side short-circuit fault handling capability, and power losses, is provided in Table 1-1.

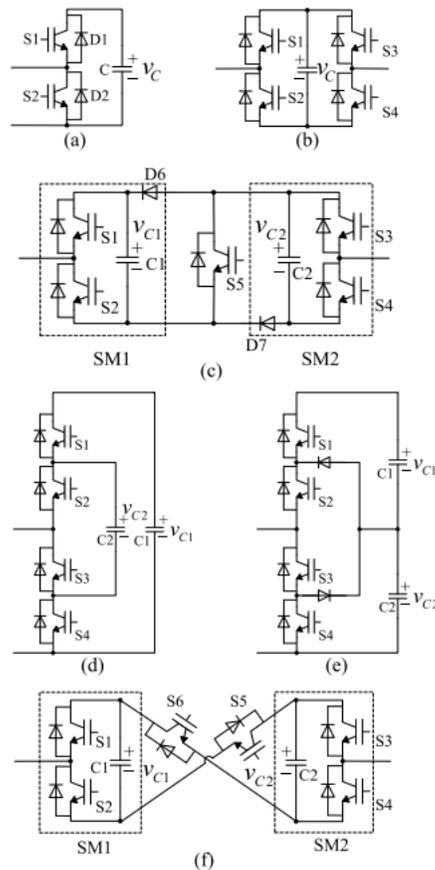


Figure 1-3 Popular SM/cell structures: (a) half bridge, (b) full bridge, (c) clamp double, (d) three phase FC - flying capacitor, (e) three phase NPC – neutral point clamp, (f) five level cross-connected SM (©2015 IEEE)

Table 1-1 Comparison of various SM/cell circuits [7] (©2015 IEEE)

SM/cell Circuit	Voltage Levels	DC-fault Handling	Losses
Half-bridge	$0, v_C$	No	Low
Full-bridge	$0, +v_C$	Yes	High
Clamp-double	$0, v_{C1}, v_{C2}, (v_{C1} + v_{C2})$	Yes	Moderate
Three-level FC	$0, v_{C1}, v_{C2}, (v_{C1} - v_{C2})$	No	Low
Three-level NPC	$0, v_{C1}, (v_{C1} + v_{C2})$	No	Moderate
Five-level cross-connected	$0, v_{C1}, v_{C2}, +(v_{C1} + v_{C2})$	Yes	Moderate

Among all of the SM circuit configurations, the half-bridge SM has been the most popular because of the less complexity and higher efficiency. Similarly, a half-bridge submodule is used in a proposed bidirectional triangular modular multilevel DC-DC converter (TMMC) in [8]. The overall system and its SM are shown in figure 1-4. The submodule on the right corner of Figure 1-8 is derived from a buck-boost converter. This topology is bidirectional such that high side voltage ( $V_{HV}$ ) and low side voltage ( $V_{LV}$ ) could be exchanged either as input or output. In this paper, a two-level prototype system with three submodules is analyzed regarding current flow with different switching states.

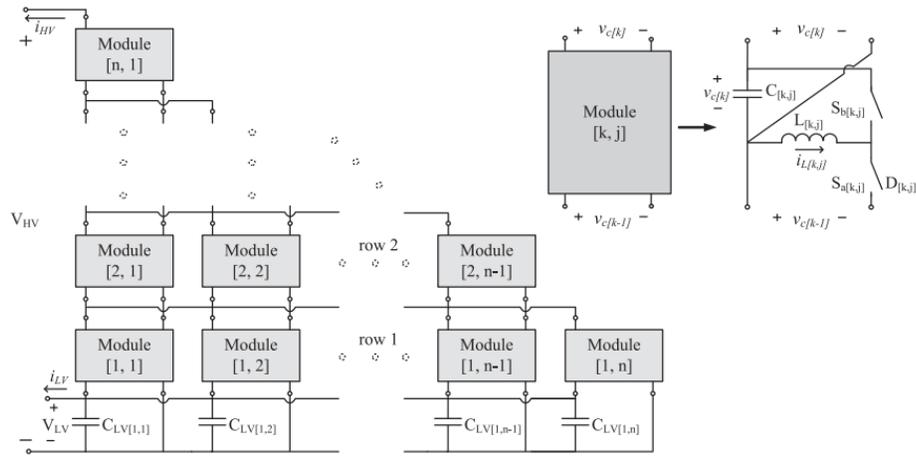


Figure 1-4 Proposed bidirectional TMMC and its SM in [8] (©2015 IEEE)

Additionally, several other effective modular multilevel DC-DC converter have been proposed. In [9], a novel completely modular multilevel capacitor-clamped DC-DC converter is proposed with the comparison to the conventional flying capacitor topology. In [10], [11], the inductor-free design has high efficiency and flexible conversion ratio which is suitable for power management of fuel cell or automotive applications. Some merits in [12] are multilevel loads/sources support and fault tolerant capability. Furthermore, soft switching technology is researched focusing on efficiency increase and current/voltage spike reduction during switching transition. In [13] and [14], zero current switching and zero voltage switching are employed, respectively.

### 1.2.2 Modulation, Control Algorithm and Operation Characteristic

In this literature, various pulse-width modulation (PWM) techniques have been proposed, mainly based on using a single reference waveform. In [15], it offers a

performance comparison of various multicarrier sinusoidal pulse width modulation (PWM) techniques for the control of the modular multilevel converter (MMC) based on the half-bridge capacitor cell.  $N$  identical carrier waveforms are displaced symmetrically with respect to the zero axis. Based on the phase shift among the carrier waveforms, these techniques are further classified into: a) phase disposition (PD), b) phase opposition disposition (POD), and c) alternate phase opposition disposition (APOD), shown in Figure 1-5 (a)–(c), respectively. These techniques are easy to implement, especially for digital control methods. However, potential disadvantages could be unequal distribution of voltage ripple across the SM capacitors. [16] proposed a modified PD PWM with an SM capacitor voltage balancing technique. Alternately, subharmonic techniques are used, with  $2N$  identical carrier per phase-leg. Sawtooth or triangular carriers with a phase shift of  $360^\circ/2N$  are used as shown in Figure 1-5 (d) and (e). Assuming the same number of switching transitions for both the PD PWM and subharmonic techniques, the PD PWM technique produces better line-to-line voltage THD. Additionally, modulation techniques based on multiple references could be summarized as: 1) Direct modulation, 2) indirect modulation, etc.

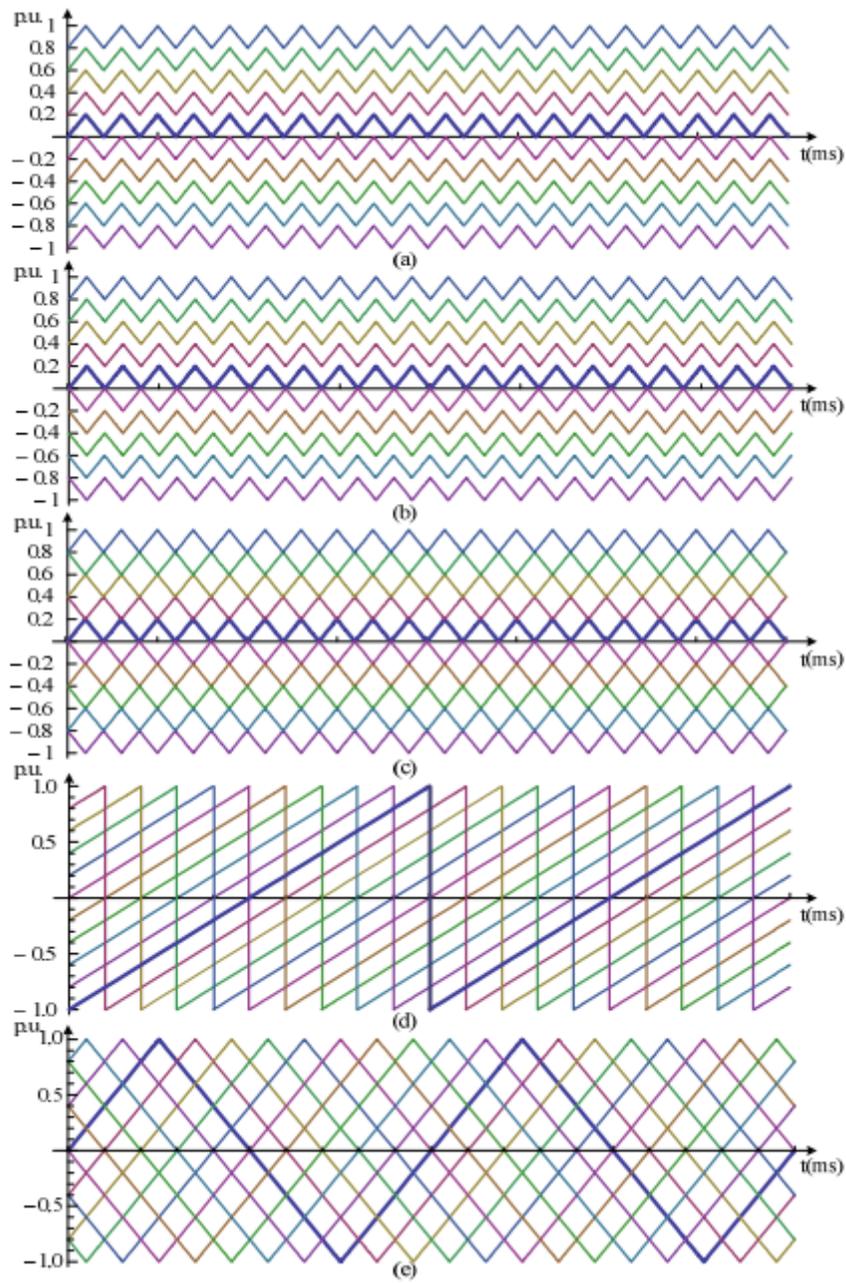


Figure 1-5 Multilevel carrier waveforms (a) PD, (b) POD, (c) APOD, (d) Saw-tooth rotation, (e)

Phase shifted carriers [15] (©2009 IEEE)

Some of the design and control issues regarding MMC are: SM capacitor voltage balancing, capacitor voltage/inductor current ripple reduction, localized control, etc.

Similar to any other multilevel converter topology, the MMC needs an active voltage balancing strategy to balance and maintain the SM capacitor voltages at  $V_{dc}/N$ . In [8], an effective dual close-loop is proposed which can achieve not only capacitor voltage balancing, but equal inductor current sharing. The current reference of the internal current controller is provided by the outer voltage controller. This complicates the overall control algorithm. In [17], a voltage balancing strategy is achieved by assigning appropriate PWM pulses to the SMs of each arm. This does not require the measurement of arm currents and it simplifies the control loop and reduces the number of sensors. In [18], a modular controller concept is proposed which uses a closed-loop controller for each SM. Some other novel capacitor voltage balancing control strategies are also proposed, like predictive control and sorting method based control.

The SM capacitor voltage ripple has been studied in [19], [20]. Most of the harmonic components are low-order which impacts the size and value of the SM capacitor in order to maintain the SM capacitor voltage ripple within reasonable limits. In some cases, the ripple can be reduced by injecting appropriate harmonic components. However, the disadvantage of most capacitor voltage ripple reduction techniques is increasing the power losses and current rating of the components. In [8], an interleaved operation technique is proposed which will achieve significant reduction in the input current and output voltage ripples of a two-level prototype system. This is done by phase-shifting the corresponding gating signals 180 degree. Comparing with non-interleaved case, the

experimental result shows a reduction of 38% and 45% for output voltage and input current ripples, respectively. Additionally, the efficiency is increased from 95.9% to 96.2%.

For the localized control, [8] proposed an effective PI control principle based on outer voltage loop and internal current loop by using TI DSP28335 for a two-level system. However, for systems with larger number of level, this principle needs to be re-evaluated and a higher controller cost may occur.

From the operation perspective, the capacitors in [9] are exposed to different steady-state voltage stresses, this makes the topology non-modular. In [8], the two-level MMC prototype system is verified by centralized DSP 28335 microcontroller. However, with the increased number of level, one single DSP is not enough to drive all the modules and gate driver isolation could be a potential problem. In this case, localized control and modular control concept can be done further research.

### *1.2.3 Research Objective*

The goal of this study is to propose and analyze a new modular multilevel DC-DC converter which has higher power density and level propagation characteristic for high power applications such as HVDC and battery storage system. In order to realize “fully modular design” concept, both the power stage building blocks and controller modules are designed separately considering level propagation and localized control for each row. Correspondingly, their print circuit boards are built separately. In the proposed configuration, the converter building blocks with the same power handling capability are

connected in parallel in each row. This leads to a triangular structure from top to bottom. Any system with arbitrary number of levels can be constructed by simply stacking these two kinds of modules together. In this case, any voltage conversion ratio can be achieved.

Converter building block consists of integrated H-bridge and mutually coupled inductors whose total current of two windings is nearly ripple free. These features are shown to reduce the voltage ripple of DC-link capacitors significantly, leading to a smaller capacitance and size. Additionally, the ripple cancellation of the total current for coupled inductors let the phase shift between building blocks not necessary, which simplifies the control and operation of the whole system.

An optimized control algorithm with voltage feedback PI loop is proposed resulting in the elimination of current sensors. Thus, the overall system complexity is reduced and the cost-effectiveness is increased. Significant ripple reduction of the inductor currents and capacitor voltages is observed based on the simulation and prototype of a 5-level system.

With a fully modular power stage module and localized control module, the system of arbitrary number of level can be built by stacking the modules thereby contributing to enhanced system redundancy.

## 2. MODELLING OF PROPOSED CONFIGURATIONS

### 2.1 Introduction

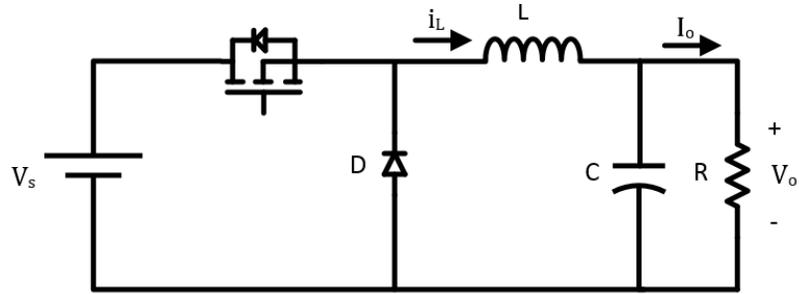


Figure 2-1 Conventional buck converter circuit

Figure 2-1 is the conventional buck converter, the ideal output voltage is defined by  $V_o = D * V_s$ .  $D$  is the duty cycle of the switch. From the voltage ratio perspective, it's a step-down conversion. My power stages modules are derived from this topology.

Two kinds of power stage modules (building blocks) are proposed: two switches (half-bridge) with single inductor; H-bridge with mutually coupled inductors. The first one is initially proposed which is similar to the conventional synchronous buck converter. Then this module is improved and a new configuration with H-bridge and mutually coupled inductor is proposed. They are shown in Figure 2-2 (a) and (b), respectively.

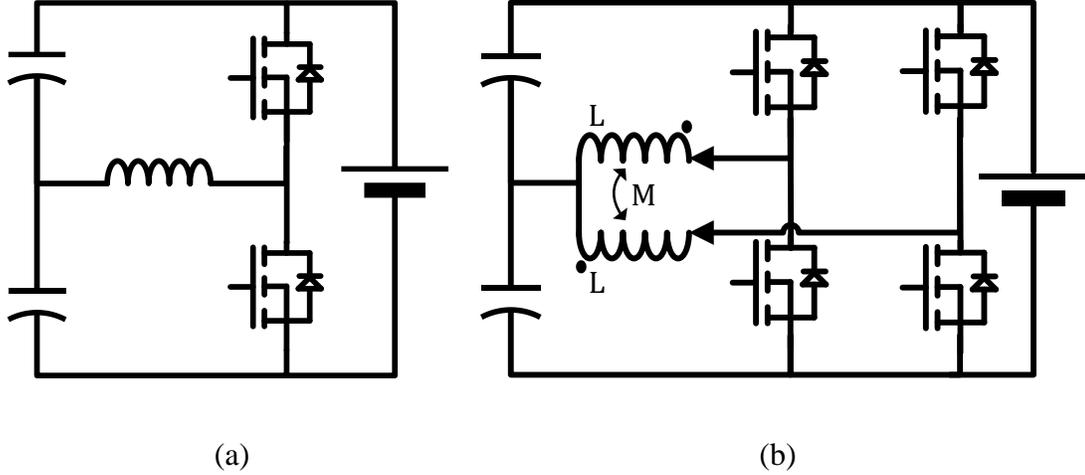
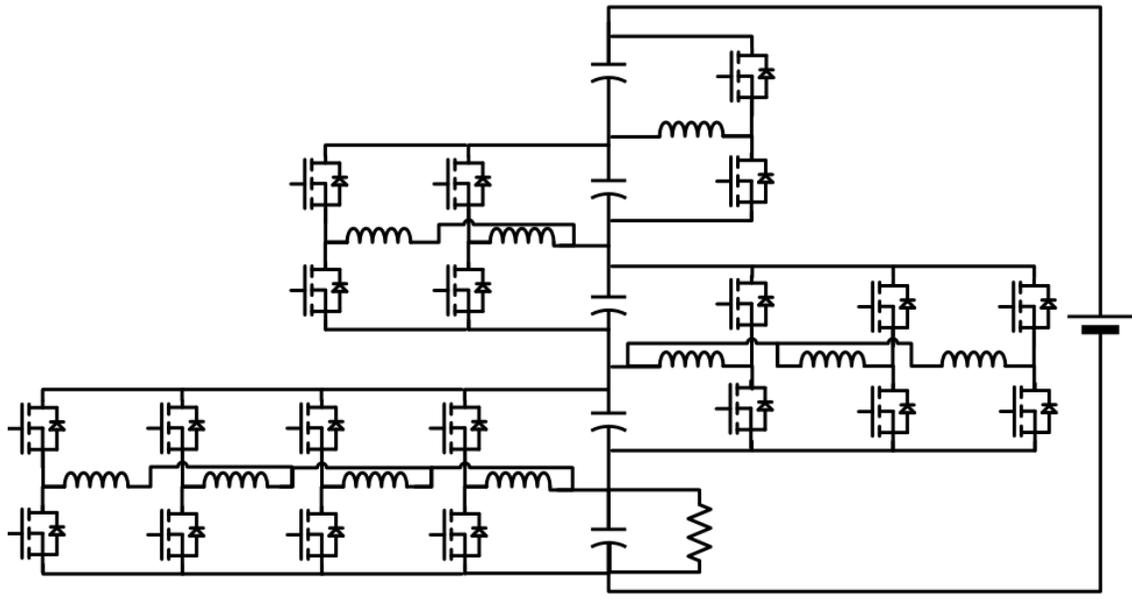


Figure 2-2 Two building blocks for MMC power stage module: (a) Half-bridge with single inductor, (b) H-bridge with mutually coupled inductors

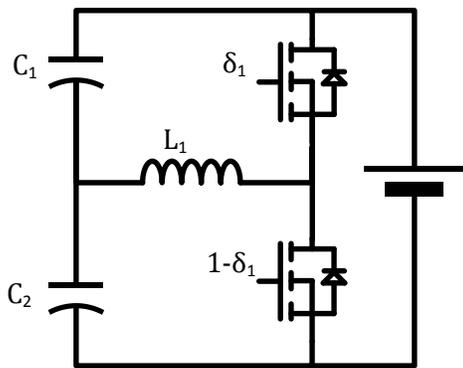
In this thesis, the five-level step down DC-DC converter is set as example for discussion. However, this configuration can be generalized to any number of levels because of the modular design concept. The input can be constant voltage or current power sources. The load can be tapped to any voltage level, and multiple loads can be interfaced at different points. Also, the source side and load side are interchangeable which enables stepping-up operation as well. Due to the bi-directional conduction characteristic of MOSFETs/IGBTs, the power flow in this configuration is also bi-directional.

## 2.2 Modelling Building Block of Half-Bridge with Single Inductor

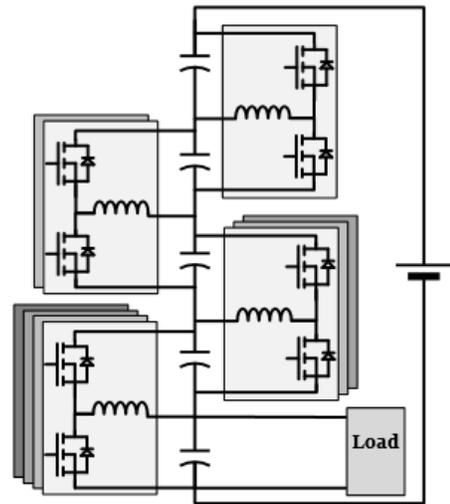
The details configuration of five level step down (5:1) MMC DC-DC converter by using building block of half-bridge with single inductor is shown in Figure 2-3.



(a)



(b)



(c)

Figure 2-3 Five level step down (5:1) MMC DC-DC converter. (a) Detailed Circuit Diagram.

(b) Building block of half-bridge with single inductor. (c) Circuit block diagram

To analyze and design the proposed configuration, a state-space analysis is provided for an arbitrary n-level converter in step-down mode. State-space equations are derived based on the current and voltage equations, which are the derivative of capacitor voltages and inductor currents, respectively.

To simplify the analysis, the following assumptions are applied:

- 1) All the inductor values are L
- 2) All the DC-link capacitor values are C
- 3) Input source current is considered constant, with the value  $I_s$
- 4) No phase shift between paralleled building blocks of the same row
- 5) From top to bottom, the sequence is 1st, 2nd, 3rd, etc
- 6)  $L_k = L/k$ , this is equivalent to the parallel connection of all the inductor
- 7)  $i_{Lk} = ki_L$ ,  $i_L$  is the current flowing through each single inductor
- 8)  $r_k$  is the LSR of kth row inductors.

Writing current equations 2.1-2.4:

$$C \dot{v}_{c1} = I_s - \delta_1 i_{L1} \quad (2.1)$$

$$C \dot{v}_{c2} = I_s + (1 - \delta_1) i_{L1} - \delta_2 i_{L2} \quad (2.2)$$

$$C \dot{v}_{c3} = I_s + (1 - \delta_2) i_{L2} - \delta_3 i_{L3} \quad (2.3)$$

⋮

$$C \dot{v}_{cn} = I_s + (1 - \delta_{n-1}) i_{L(n-1)} - \frac{v_{cn}}{R} \quad (2.4)$$

Similarly, writing voltage equations 2.5-2.7:

$$L_1 \dot{i}_{L1} = \delta_1 v_{c1} - (1 - \delta_1) v_{c2} - r_1 i_{L1} \quad (2.5)$$

$$L_2 \dot{i}_{L2} = \delta_2 v_{c2} - (1 - \delta_2) v_{c3} - r_2 i_{L2} \quad (2.6)$$

...

$$L_{(n-1)} \dot{i}_{L(n-1)} = \delta_{(n-1)} v_{C(n-1)} - (1 - \delta_{(n-1)}) v_{Cn} - r_{(n-1)} i_{L(n-1)} \quad (2.7)$$

Rewriting 2.1-2.7 in a state space form (2.8).

$$\begin{bmatrix} v_{c1} \\ v_{c2} \\ v_{c3} \\ \vdots \\ v_{cn} \\ i_{L1} \\ i_{L2} \\ i_{L3} \\ \vdots \\ i_{L(n-1)} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \vdots & 0 & 0 & 0 & 0 & 0 & \vdots & 0 \\ \dots & \dots & \dots & \cdot & \dots & \dots & \dots & \dots & \dots & \cdot & \dots \\ 0 & 0 & -\frac{\delta_3}{C} & \vdots & 0 & 0 & 0 & 0 & 0 & \vdots & 0 \\ 0 & -\frac{\delta_2}{C} & \frac{1-\delta_2}{C} & \vdots & 0 & 0 & 0 & -\frac{r_2}{L_2} & 0 & \vdots & 0 \\ -\frac{\delta_1}{C} & \frac{1-\delta_1}{C} & 0 & \vdots & 0 & 0 & -\frac{r_1}{L_1} & 0 & 0 & \vdots & 0 \\ 0 & 0 & 0 & \vdots & -\frac{1}{RC} & 0 & 0 & 0 & 0 & \vdots & \frac{\delta_{n-1}-1}{L_{n-1}} \\ \dots & \dots & \dots & \cdot & \dots & \dots & \dots & \dots & \dots & \cdot & \dots \\ 0 & 0 & 0 & \vdots & 0 & 0 & 0 & \frac{\delta_2-1}{L_2} & \frac{\delta_3}{L_3} & \vdots & 0 \\ 0 & 0 & 0 & \vdots & 0 & 0 & \frac{\delta_1-1}{L_1} & 0 & 0 & \vdots & 0 \\ 0 & 0 & 0 & \vdots & 0 & 0 & 0 & 0 & 0 & \vdots & 0 \\ 0 & 0 & 0 & \vdots & 0 & 0 & 0 & 0 & 0 & \vdots & 0 \end{bmatrix} \begin{bmatrix} i_{L(n-1)} \\ \vdots \\ i_{L3} \\ i_{L2} \\ i_{L1} \\ v_{cn} \\ \vdots \\ v_{c3} \\ v_{c2} \\ v_{c1} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \\ \vdots \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad (2.8)$$

Using Matlab state-space toolbox, the waveforms of state variables based on a random 5-level example is shown in Figure 2-4. All of the capacitor voltages are the same (balanced). The total inductor current of each row is increasing following the relationship  $i_{Lk} = ki_L$ . Additionally, the transient response for each waveform is very smooth which verifies the effectiveness of the state space derivation.

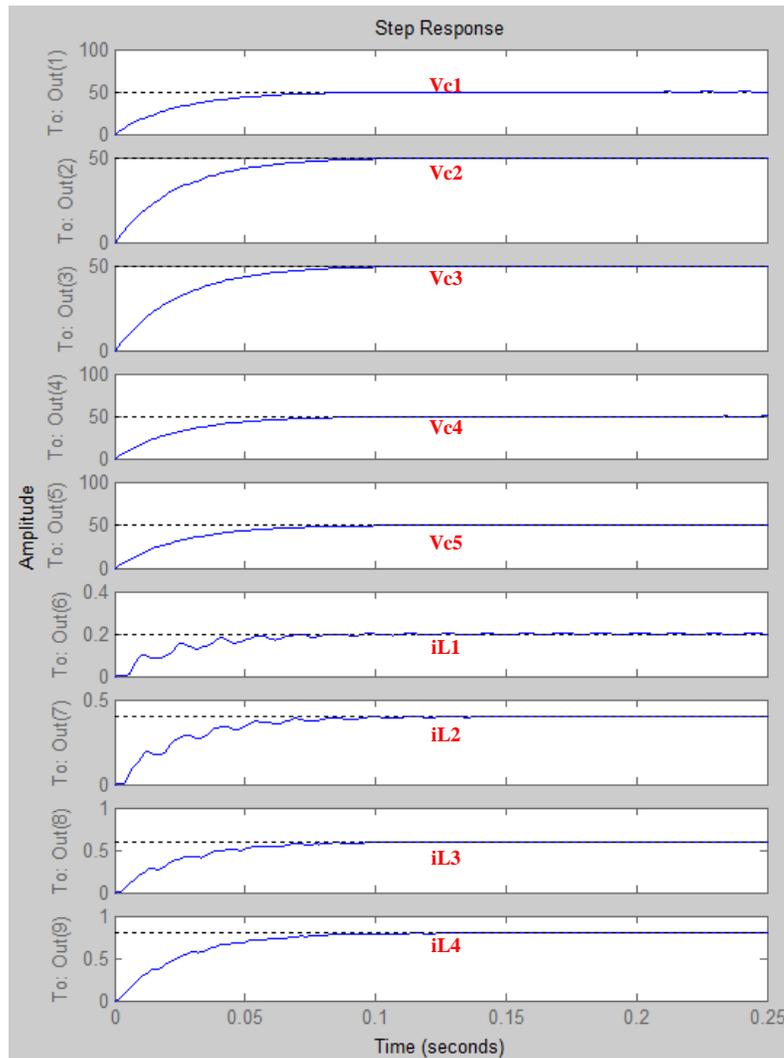


Figure 2-4 Waveforms of state variables from Matlab state-space toolbox based on a 5-level example

### 2.3 Modelling Building Block of H-bridge with Mutually Coupled Inductor

Similarly, the details configuration of a five-level step down (5:1) MMC DC-DC converter by using building block of H-bridge with mutually coupled inductor is shown in Figure 2-5.

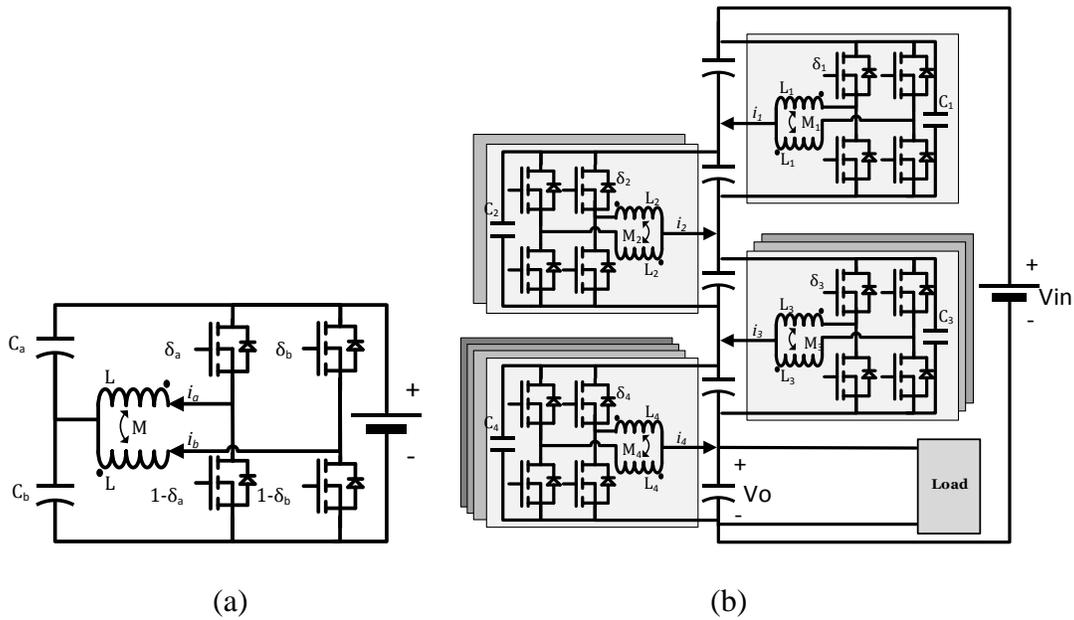


Figure 2-5 Five level step down (5:1) MMC DC-DC converter. (a) Building block of H-bridge with mutually coupled inductor. (c) Circuit block diagram

To simplify the analysis, the following assumptions are applied to the building block:

- 1) For the coupled inductors, the self-inductance is  $L$ , mutual inductance is  $M$  and the leakage inductance is  $L_l$ . Coupling coefficient is  $k_M$
- 2) All the DC-link capacitor values are  $C$
- 3) Input source current is considered constant, with the value  $I_s$

- 4) No phase shift between paralleled building blocks of the same row
- 5) From top to bottom, the sequence is 1<sup>st</sup>, 2<sup>nd</sup>, 3<sup>rd</sup>, etc.

### 2.3.1 State Space Equation Derivation

Writing voltage equations 2.9-2.10 for each building block:

$$L \dot{i}_a - M \dot{i}_b = \delta_a v_{C a} - (1 - \delta_a) v_{C b} - r i_a \quad (2.9)$$

$$L \dot{i}_b - M \dot{i}_a = \delta_b v_{C a} - (1 - \delta_b) v_{C b} - r i_b \quad (2.10)$$

Adding Equations 2.9 and 2.10, the result is shown in Equation (2.11)

$$L (\dot{i}_a^\circ + \dot{i}_b^\circ) - M (\dot{i}_a^\circ + \dot{i}_b^\circ) = (\delta_a + \delta_b) v_{C a} - (2 - \delta_a - \delta_b) v_{C b} - r (i_a + i_b) \quad (2.11)$$

Subtracting Equations 2.9 by 2.10, the result is shown in Equation (2.12)

$$L (\dot{i}_a^\circ - \dot{i}_b^\circ) - M (-\dot{i}_a^\circ + \dot{i}_b^\circ) = (\delta_a - \delta_b) v_{C a} - (-\delta_a + \delta_b) v_{C b} - r (i_a - i_b) \quad (2.12)$$

The self-inductance is the sum of the leakage inductance and the mutual inductance, as shown in Equation 2.13.

$$L = M + L_l \quad (2.13)$$

Renaming variables  $i_t = i_a + i_b$  and  $\Delta i = i_a - i_b$ , then substituting by 2.13 in 2.11 and 2.12, Equations 2.14 and 2.15 are shown below.

$$L_l \dot{i}_t^\circ = (\delta_a + \delta_b) v_{C a} + (\delta_a + \delta_b - 2) v_{C b} - r i_t \quad (2.14)$$

$$(2L - L_l) \Delta \dot{i}^\circ = (\delta_a - \delta_b) v_{C a} + (\delta_a - \delta_b) v_{C b} - r \Delta i \quad (2.15)$$

Rewriting Equations 2.14 and 2.15 in a matrix form 2.16.

$$\begin{bmatrix} \dot{i}_t^\circ \\ \Delta \dot{i}^\circ \end{bmatrix} = \begin{bmatrix} \frac{\delta_a + \delta_b}{L_l} & \frac{\delta_a + \delta_b - 2}{L_l} \\ \frac{\delta_a - \delta_b}{2L - L_l} & \frac{\delta_a - \delta_b}{2L - L_l} \end{bmatrix} \begin{bmatrix} v_{C a} \\ v_{C b} \end{bmatrix} + \begin{bmatrix} \frac{-r}{L_l} & 0 \\ 0 & \frac{-r}{2L - L_l} \end{bmatrix} \begin{bmatrix} i_t \\ \Delta i \end{bmatrix} \quad (2.16)$$

During normal operation,  $\delta_a$  &  $\delta_b$  are 50% duty and 180° phase shifted from each other, thus  $\delta_a + \delta_b = 1$ .

Hence, Equation 2.16 can be rewritten as:

$$\begin{bmatrix} i_t^\circ \\ \Delta i^\circ \end{bmatrix} = \begin{bmatrix} \frac{1}{L_l} & \frac{-1}{L_l} \\ \frac{2\delta_a-1}{2L-L_l} & \frac{2\delta_a-1}{2L-L_l} \end{bmatrix} \begin{bmatrix} v_{C a} \\ v_{C b} \end{bmatrix} + \begin{bmatrix} \frac{-r}{L_l} & 0 \\ 0 & \frac{-r}{2L-L_l} \end{bmatrix} \begin{bmatrix} i_t \\ \Delta i \end{bmatrix} \quad (2.17)$$

Or separately,

$$i_t^\circ = \frac{v_{C a} - v_{C b}}{L_l} - \frac{r}{L_l} i_t \quad (2.18)$$

$$\Delta i^\circ = \frac{(2\delta_a-1)(v_{C a} + v_{C b})}{2L-L_l} - \frac{r}{2L-L_l} \Delta i \quad (2.19)$$

From Equations (2.18) and (2.19), we can conclude:

The total current is driven by the voltage difference of the upper and lower capacitors ( $v_{C a}$  and  $v_{C b}$ ) and the leakage inductance determines its dynamics. The current difference is driven by the duty cycle error compared to 50% for each leg, and the self-inductance (leakage inductance is small compared to self-inductance) determines its dynamics. In most cases, leakage inductance is very small, this requires the upper and lower capacitor voltages are well balanced in order to keep the total current variation within an acceptable range. On the contrary, even if there is some duty cycle error, the current difference variation could be maintained within an acceptable level because of the relatively high self-inductance. This reveals one critical point for control algorithm: achieving as accurate voltage balancing control as possible.

Similarly, the state space matrix of a n-level system can be expressed in equation 2.20.



Similarly, using Matlab state-space toolbox, the waveforms of state variables based on a random 5-level example is shown in Figure 2-6. All of the capacitor voltages are the same (balanced). The total current is almost ripple free. The current difference is close to zero. Additionally, the transient response for each waveform is very smooth which verifies the effectiveness of the state space derivation.

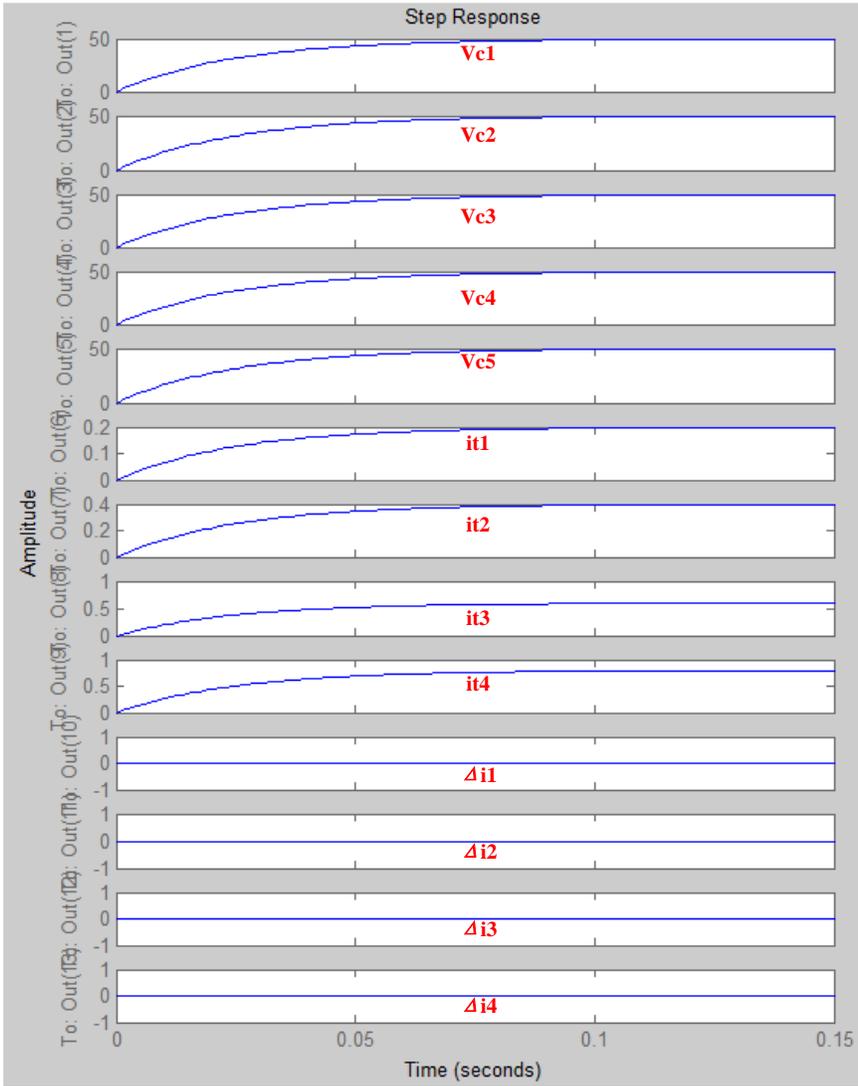


Figure 2-6 Waveforms of state variables from Matlab state-space toolbox based on a 5-level example for the new configuration

### 2.3.2 Self-inductance of Mutually Coupled Coils

Assume coupling coefficient is  $k_M$  ( $0 < k_M < 1$ ), we can get equation (2.21) and (2.22).

$$M = k_M L \quad (2.21)$$

$$L_l = L(1 - k_M) L \quad (2.22)$$

The self-inductance can be derived from equation (2.16) (neglecting winding resistance) and then expressed in (2.23).

$$L(1 + k_M) \frac{\Delta i}{T_s/2} = (\delta_a - \delta_b)(v_{C a} + v_{C b}) \quad (2.23)$$

Approximately,

$$i_a \approx i_b \approx I_s \quad (2.24)$$

Based on switching function, we have:

$$(\delta_a - \delta_b) = \pm 1 \quad (2.25)$$

Assume  $k_i I_s$  is the current ripple of single coil, the current difference can be expressed in (2.26),

$$\Delta i = i_a - i_b = (2k_i)I_s \quad (2.26)$$

Therefore, the self-inductance is calculated by (2.27):

$$L = \frac{1}{(1+k_M)} \frac{T_s/2}{\Delta i} \frac{2V_{DC}}{n} = \frac{1}{(1+k_M)} \frac{V_{DC}}{n} T_s \frac{1}{k_i 2 I_s} \approx \frac{V_{DC}}{n} \frac{T_s}{2} \frac{1}{k_i 2 I_s} \quad (2.27)$$

Where,

$V_{DC}$  Input voltage;

$n$  Number of levels;

$T_s$  Switching period ( $T_s = \frac{1}{f_s}$ ).

The self-inductance is proportional to SM capacitor voltage, and reversely proportional to switching frequency and current ripple percentage.

### 2.3.3 Energy Stored in Mutually Coupled Coils

First, keep the assumptions from (2.24) and (2.26), the total energy that is stored in mutually coupled coils can be expressed as following:

$$\begin{aligned}
E_{mut} &= \frac{1}{2} L i_a^2 + \frac{1}{2} L i_b^2 - M i_1 i_2 \\
&= \frac{1}{2} L i_a^2 + \frac{1}{2} L i_b^2 - (L - L_l) i_a i_b \\
&= \frac{1}{2} L (i_a^2 + i_b^2 - 2 i_1 i_2) + L_l i_a i_b \\
&= \frac{1}{2} L (i_a - i_b)^2 + L_l i_a i_b \\
&= \frac{1}{2} L \Delta i^2 + L(1 - k_M) i_a i_b
\end{aligned} \tag{2.27}$$

Substituting (2.24), (2.26) and (2.27), hence,

$$\begin{aligned}
E_{mut} &= \frac{1}{2} L (\Delta i^2 + 2(1 - k_M) i_a i_b) \\
&\approx \frac{1}{2} \frac{1}{(1+k_M)} \frac{V_{DC}}{n} T_s \frac{1}{k_i 2 I_s} ((k_i 2 I_s)^2 + 2(1 - k_M) I_s^2) \\
&= \frac{1}{2} \frac{1}{(1+k_M)} \frac{V_{DC}}{n} T_s \frac{1}{k_i 2 I_s} ((k_i 2)^2 + 2(1 - k_M)) I_s^2 \\
&= \frac{1}{2} \frac{1}{(1+k_M)} \frac{V_{DC}}{n} T_s \frac{1}{k_i 2 I_s} ((k_i 2)^2 + 2(1 - k_M)) I_s^2 \\
&= \frac{V_{DC} T_s I_s}{2 n k_i} \left( 2 \frac{k_i^2 + \frac{1-k_M}{2}}{(1+k_M)} \right)
\end{aligned} \tag{2.28}$$

Regarding the energy part corresponding to  $\frac{1-k_M}{2}$ , it represents the stored energy of leakage inductance, while not the energy stored in the magnetic core.

Assume  $k_M=0.99$ ,  $k_i=0.05$ ,  $n=100$ , the stored energy is calculated by:

$$E_{mut} = \frac{V_{DC} T_s I_s}{2 n k_i} \left( 2 \frac{k_i^2 + \frac{1-k_M}{2}}{(1+k_M)} \right) = \frac{V_{DC} T_s I_s}{2 n k_i} (0.00754)$$

For the same power rating, the comparison of total energy stored among the three configurations can be conclude in Table 2-1.

Table 2-1 Stored energy comparison between the three configurations

Topology	New Configuration (coupled inductors)	Old Configuration (single inductor)	Conventional Buck
Stored Energy	$\frac{V_{DC} T_s I_s}{2 n k_i} \left( 2 \frac{k_i^2 + \frac{1-k_M}{2}}{(1+k_M)} \right)$	$\frac{V_{DC} I_s T_s}{2 k_i} (n-1) \frac{1}{2}$	$\frac{V_{DC} I_s T_s}{2 k_i} (n-1) \left( \frac{1}{n} \right)$
Ratio (with $L_l$ )	0.337	50	1
Ratio (without $L_l$ )	0.130	50	1

Based on the result in Table 2-1, the total store energy for a n-level system (in case of mutually coupled coils) is much less than the other two cases, especially compared with proposed topology with separate coil. Less energy storage will lead to the significant reduction of size, weight and magnetic materials needed. For this reason, the final design example and prototyping would be based on the proposed topology with mutually coupled coils.

However, the above estimation of total energy storage is proportional to the total volume of the used inductors if same core material is considered. It is clearly shown that the proposed topology (with mutually coupled coils) will have smaller volume compared

to conventional buck case. Nevertheless, large inductors (as the one used for conventional buck case) are usually air cored, on the other side the small inductors used in the proposed topology can be wound on ferrite cores of high relative permeability resulting in further size reduction.

## **2.4 Advantages and Disadvantages of New Configuration**

A list of advantages for the new configuration can be concluded as following:

- 1) Modularity and redundancy
- 2) No series connection of semiconductor switches, i.e. lower losses and increased operation stability.
- 3) Better utilization of semiconductor switches
- 4) The current ripple of the bus bars feeding parallel modules is minimum, so low EMI
- 5) During partial loading, some of the parallel modules can be turned off to enable other modules to operate at full load, thus the overall efficiency can be higher.
- 6) Regarding fault tolerance, the failure of one of the modules will create a short circuit on a portion of the bus, and the remaining modules (attached to the rest of capacitors) will carry some extra voltage to keep the DC bus voltage constant.
- 7) Higher power density.

Regardless of these advantages, potential disadvantages are listed below:

- 1) Higher number of switches, however, the total VA rating of all semiconductor switches is the same as in conventional buck converter case.
- 2) Higher number of inductors
- 3) The introduction of leakage inductance, which may cause high-frequency resonance between the leakage inductance and DC-link capacitor.

### 3. OPEN LOOP SIMULATION VERIFICATION

#### 3.1 Introduction

Before heading to the close-loop algorithm design and analysis, a design example is given and its simulation implemented by open loop control for ideal case will be presented. Based on the modelling part in Chapter 2, during optimal operation,  $\delta_a$  &  $\delta_b$  are 50% duty and 180° phase shifted from each other. From (2.18) and (2.19), we know that capacitor voltages unbalancing and leakage inductance will affect the shape of total current and current difference waveforms of mutually coupled inductors. Additionally, high frequency resonance might be caused by the small leakage inductance and DC-link capacitors. All of the problems above can be analyzed by open loop simulation and it will be a helpful guide to design the close-loop algorithm from the perspectives of steady state and dynamic response.

#### 3.2 Design Example

In order to verify the effectiveness of the proposed new configuration, a design example with all the detailed system specifications is given in Table 3-1.

Table 3-1 A detailed design example of the new configuration

System Power Rating	$P_o = 1.125KW$
Source Voltage (constant)	$V_{in} = V_{DC} = 375V$
Source Current (average)	$I_s = 3A$
Load	$R = 5\Omega, V_o = 75V, I_o = 15A$
Switch Frequency (Max)	$f_s = 20Khz (T_s = 1/f_s)$
Number of level	$n = 5$
Average current of each coil	$i_a \approx i_b \approx I_s = 3A$
Current ripple ratio for each coil	$k_i \leq 0.05$
Peak-peak current for each coil	0.15A
Current difference between two coils	$\Delta i = i_a - i_b = (2k_i)I_s = 0.3A$
Self-inductance of each coil	$L = 6.375mH$ (Equation (2.27))
Leakage inductance of each coil	$L_l = 10nH$
Capacitor value	25uF

### 3.3 Open Loop Simulation

For optimal operation, all the switches gating signal are 50% duty cycle. The top switch and bottom switch of each leg are operating in a complementary manner. All the building blocks of the same role are operating synchronously, with no phase shift. This open loop simulation is done by PSIM, the circuit screenshot is shown in Figure 3-1.

The simulation results are shown below. Figure 3-2 is capacitor voltage waveform. Figure 3-3 is total inductor current for all building blocks of each row. Figure 3-4 is the separate coil current waveform of the mutually coupled inductors. Figure 3-5 are total current and current difference waveforms of certain mutually coupled inductors. Figure 3-6 is the input current waveform from the power supply.

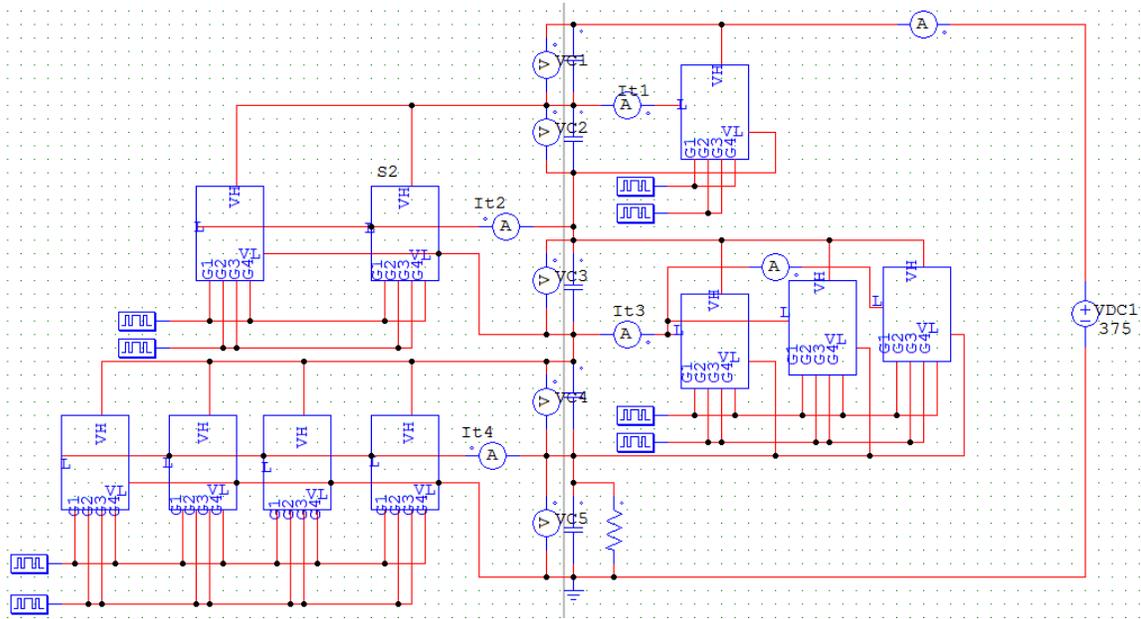


Figure 3-1 PSIM open loop simulation circuit of the five-level new configuration design example

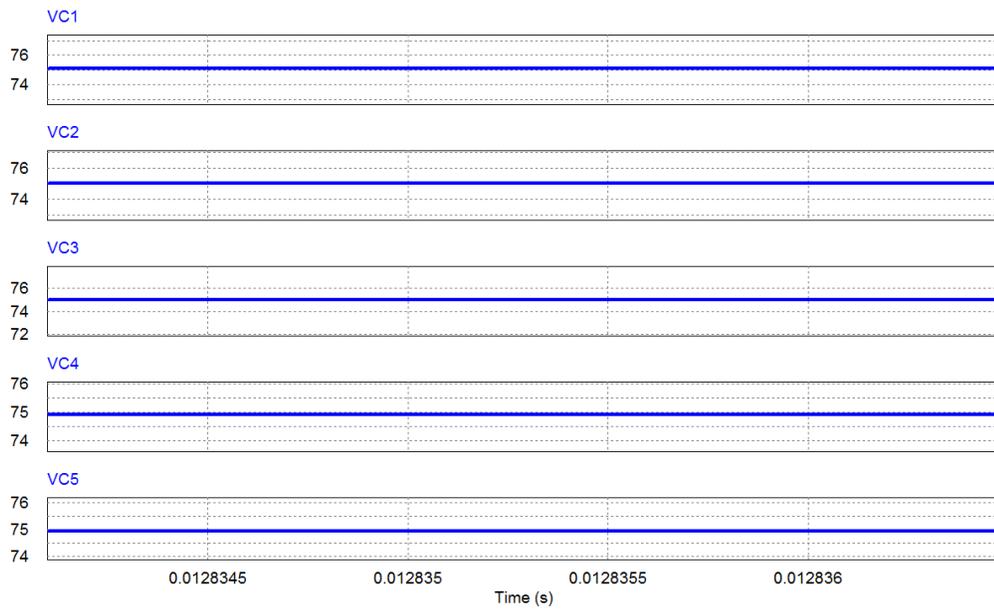


Figure 3-2 Capacitor voltage waveform

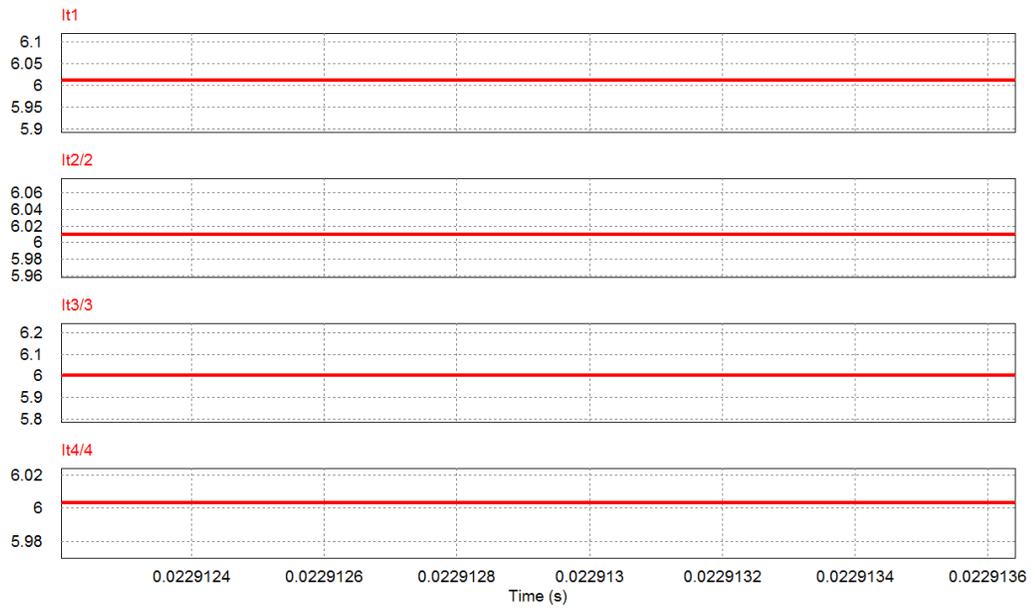


Figure 3-3 Total inductor current for all building blocks of each row

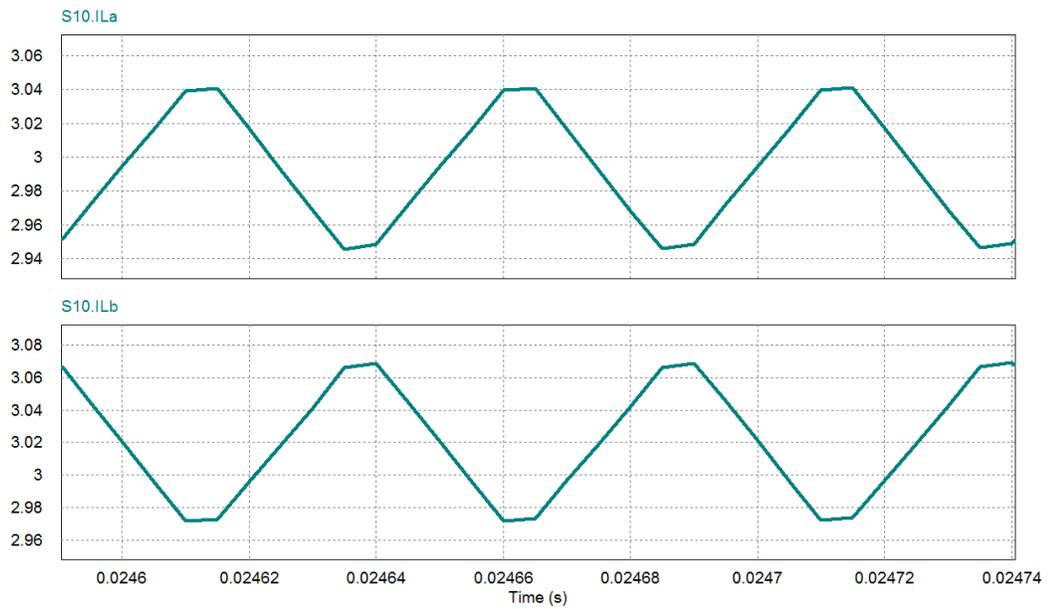


Figure 3-4 Separate coil current of the mutually coupled inductor

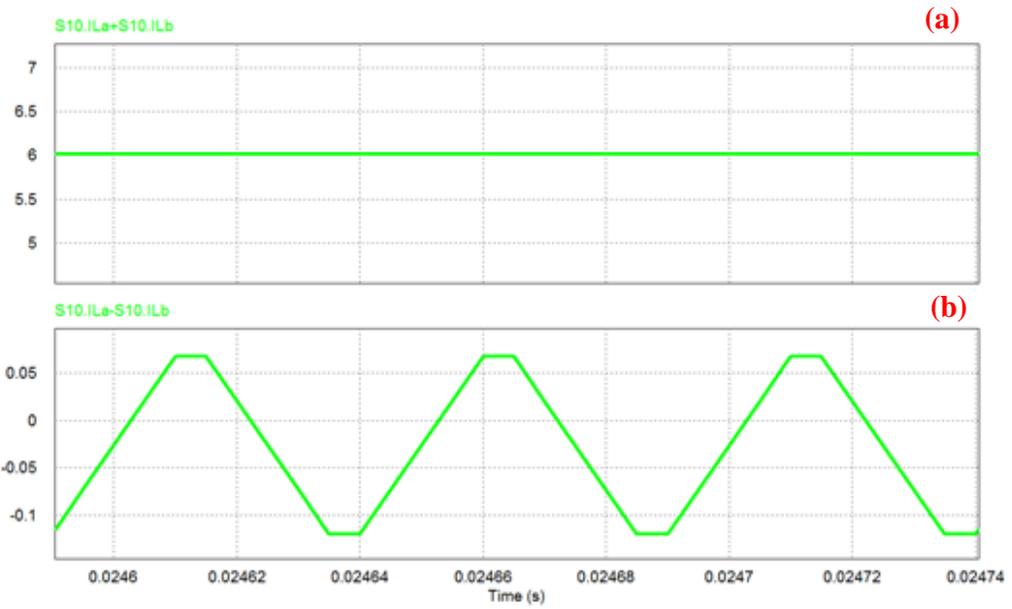


Figure 3-5 (a) Total current; (b) Current difference waveforms of certain mutually coupled inductors

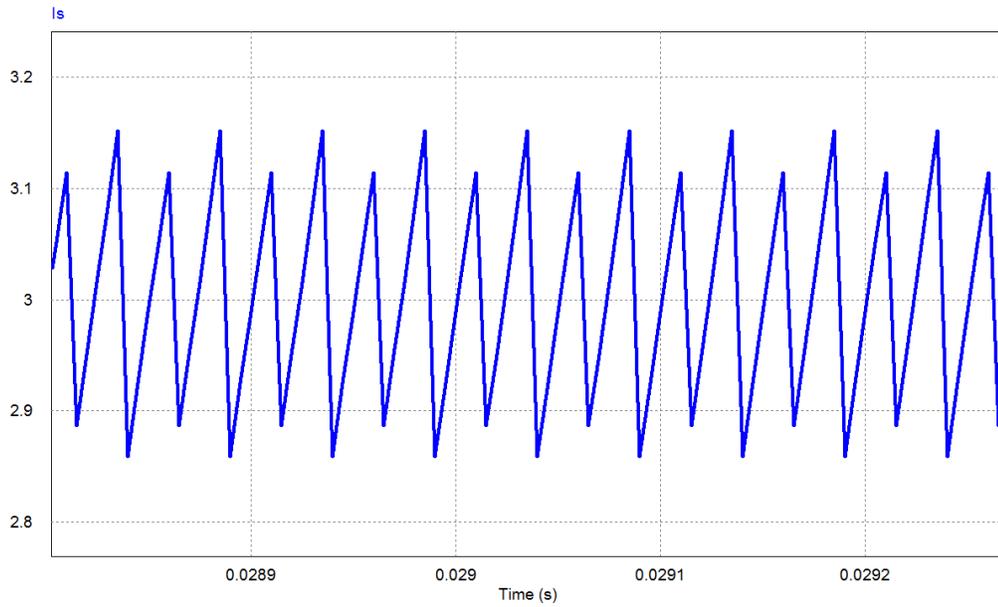


Figure 3-6 Input current waveform from power supply

Based on the simulation results, the five DC-link capacitor voltages are balancing which is exactly one fifth of the source voltage. The total current for the each mutually coupled inductors is 6A with negligible ripples. From top to bottom, the total current injected to the DC-link capacitor is proportionally to the number of paralleled building blocks of each row. As for the source current, it will ramp up and down periodically because of the switching operation of the H-bridge in the first row. The currents that are flowing through the two coupled coils are changing in a reverse manner, however, the peak-peak current ripples are the same as 0.15A. Therefore, the current difference peak-peak value will be doubled, as shown in the last waveform with the value of 0.3A. The input current of this configuration contains a DC value of 3A with small ripple components.

## 4. CLOSED LOOP CONTROL ALGORITHM DESIGN

### 4.1 Design Consideration

The control algorithm is aiming at simplifying sensor circuit and also providing localized modular control of all converter building blocks. It's also focusing on hardware installation and future extension flexibility. Each controller module is only responsible for the converter building blocks of the same role. In this case, both the power stage building block and the controller module are really modular which is just as the name “modular multilevel DC-DC converter” shows. A brief block diagram of the whole system with controller modules is shown in Figure 4-1.

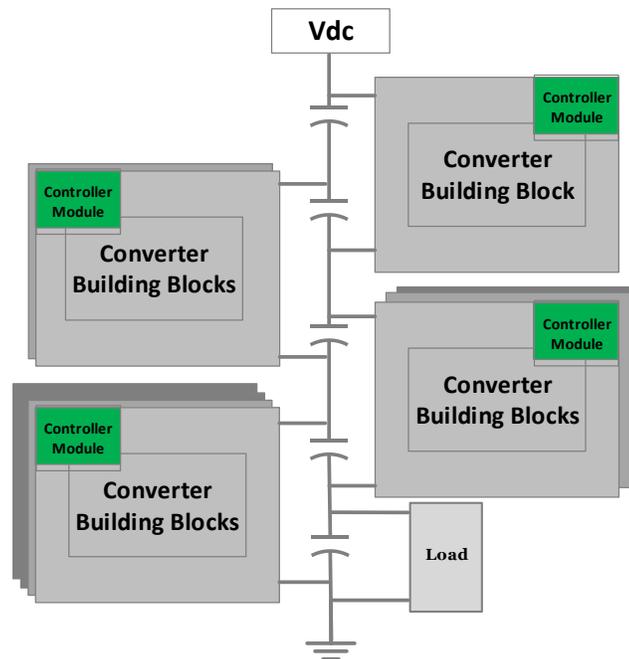


Figure 4-1 Block diagram of the whole system with converter building blocks and localized

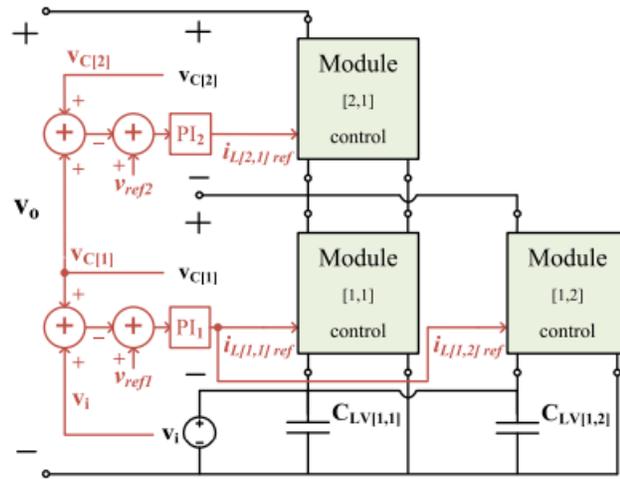
controller modules

Equation (2.18) indicates the total current is driven by the voltage difference of the upper and lower capacitors ( $v_{c_a} - v_{c_b}$ ). From (2.16), the current difference is determined by the duty cycle difference of the two upper switches, as ( $\delta_a - \delta_b$ ). For the mutually coupled inductors, current difference will increase the total magnetic flux within the magnetic core, even saturate the choke. Hence, dynamic capacitor voltage balancing and duty cycle matching are the basis of proposed control algorithm. With this prerequisite, the equal current sharing between converter building blocks will be achieved automatically, equal power sharing as well.

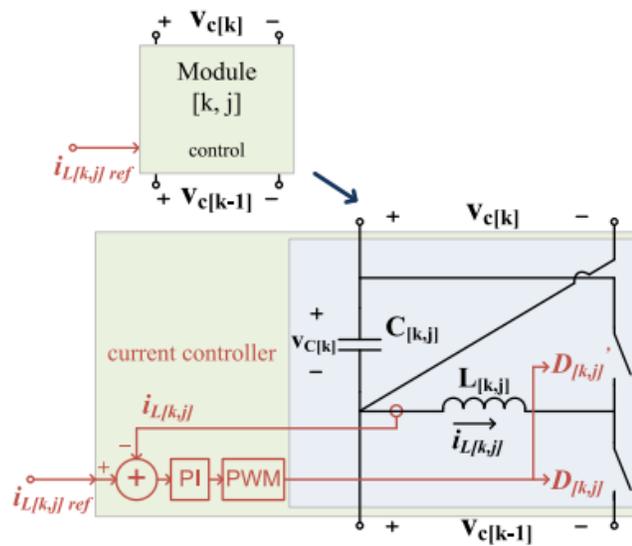
For two capacitors connected in series, if single capacitor voltage is one half of the voltage across the two, the capacitor voltage balancing is achieved. The negative polarity of the lower capacitor could be regarded as the floating ground of this row. From top to bottom, the floating ground of each row will be created in this manner. Likewise, the controller module drives converter building blocks of the same row referring to the corresponding floating ground.

## **4.2 Compensation Network Design**

In [8], a proportional-integral (PI) compensation network is proposed. It creates a dual-loop feedback system: outer voltage loop and internal current loop. They are shown in Figure 4-2 (a) and (b).



(a)



(b)

Figure 4-2 TMMC (a) Outer voltage loop; (b) Internal current loop [8] (©2015 IEEE)

It is effective in achieving capacitor voltage balancing and equal current/power sharing of each module. However, the requirement of both voltage and current sensor circuits complicate the system design. Consider the total current and current difference

characteristics which are discussed before, compensation network which is targeting at achieving capacitor voltage balancing and 50% duty will be able to achieve current sharing automatically.

Regarding the compensation type, proportional-integral (PI) or proportional-integral-derivative (PID) controller could be possible candidates. For the PID controller, the derivative part will amplify the system noise which is mostly from the switching operation. Hence, derivative loop is not preferable for the proposed new configuration which has large number of switches. In this case, proportional-integral controller is a good candidate to achieve the dynamic capacitor voltage balancing between the upper and lower switches.

As for the configuration of feedback control loop, it accepts the voltage difference as input from the upper and lower capacitors, and the output of the PI compensation network is compared with triangular signal to generate the PWM signals which are sent to the gates of H-bridge. The control algorithm for each row is shown in Figure 4-3.

In this proposed control algorithm, current sensor circuit and voltage reference are eliminated. This greatly simplifies the control loop and improves the system robustness. The dynamic capacitor voltage balancing will always be achieved no matter how source voltage and load change. Additionally, by creating a floating ground for each row, this control algorithm can be applied to a system with any number of levels.

As clarified before, in each row, power stage modules are connected in parallel. There is no phase shift between each pair of gating signals for paralleled modules thanks to the current ripple cancellation strategy for the mutually coupled inductors. This leads

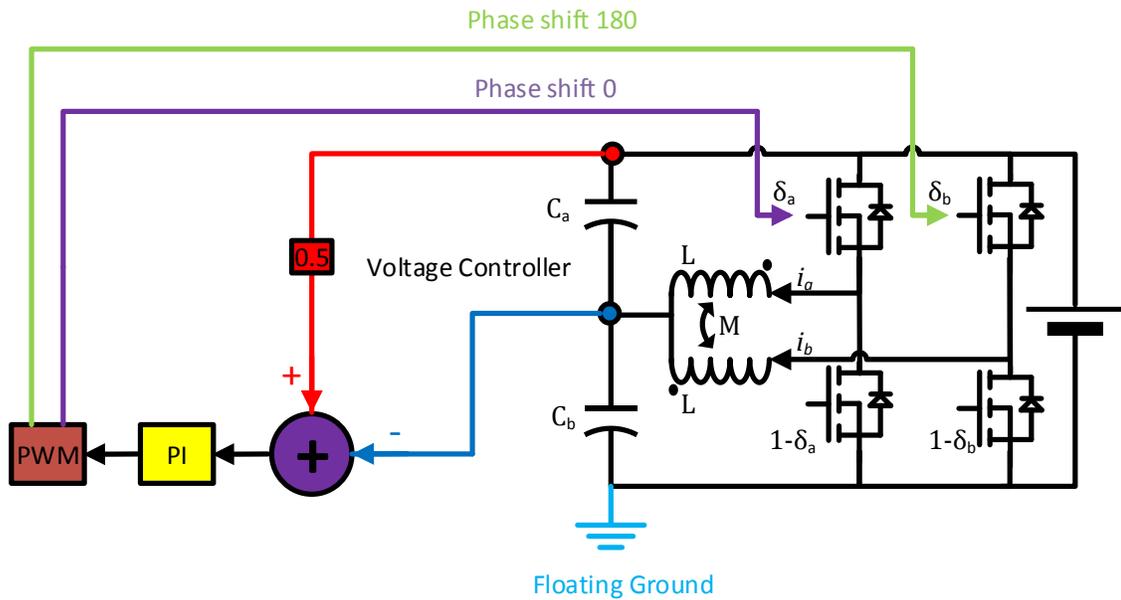


Figure 4-3 Close-loop control algorithm for each row

to simpler control algorithm design and makes modular controller into reality. The generation of “floating ground” for each row will be discussed in detail in the hardware implementation chapter.

### 4.3 Closed Loop Simulation

The PSIM simulation screenshot of the design example by implementing the proposed control algorithm is shown in Figure 4-4.

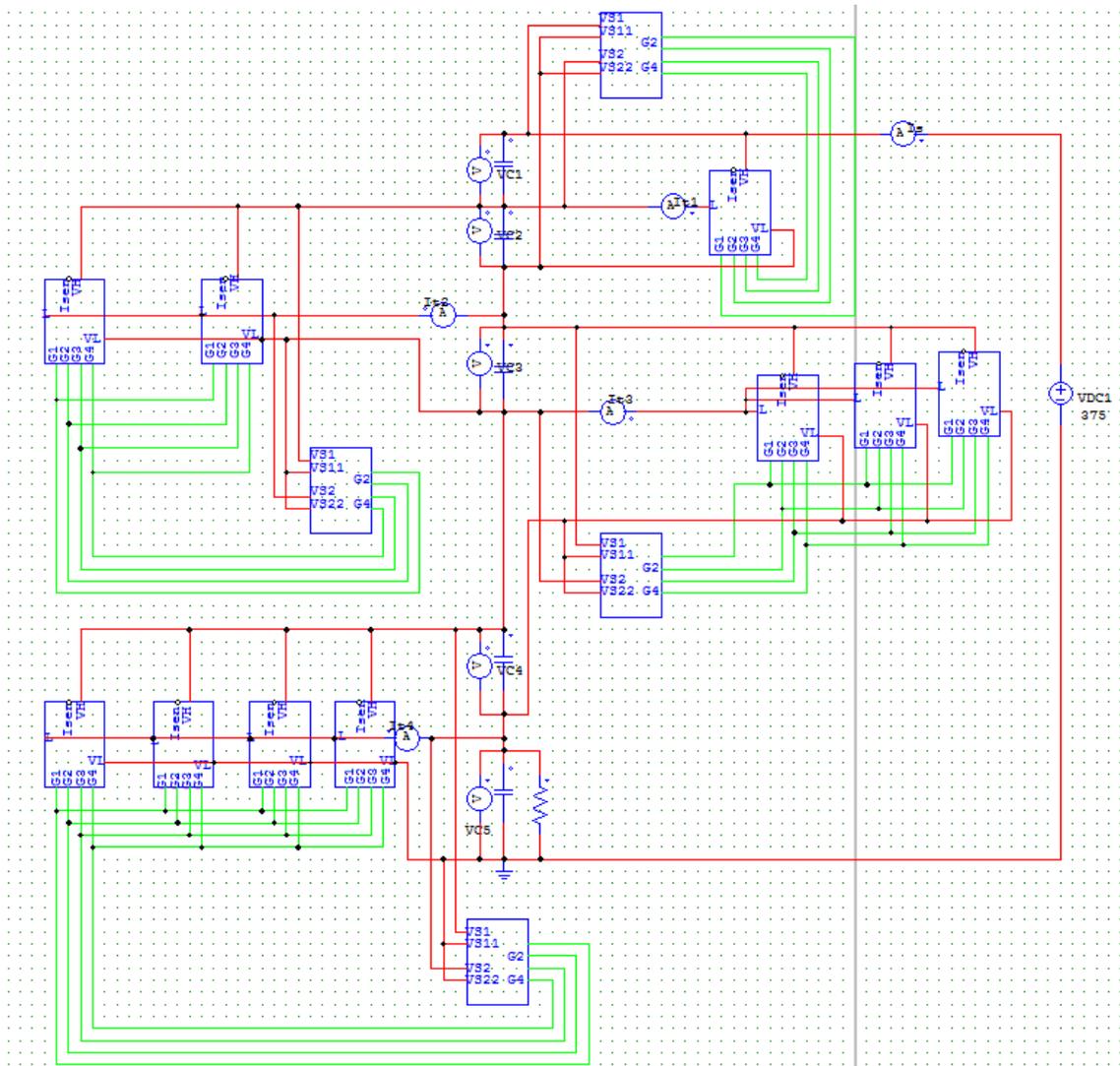


Figure 4-4 PSIM close loop simulation circuit of the five-level design example

The simulation results are shown below. Figure 4-5 is capacitor voltage waveform. Figure 4-6 is total inductor current for all building blocks of each row. Figure 4-7 is the separate coil current waveform of the mutually coupled inductors. Figure 4-8 are total current and current difference waveforms of certain mutually coupled inductors. Figure 4-9 is the input current waveform from the power supply.

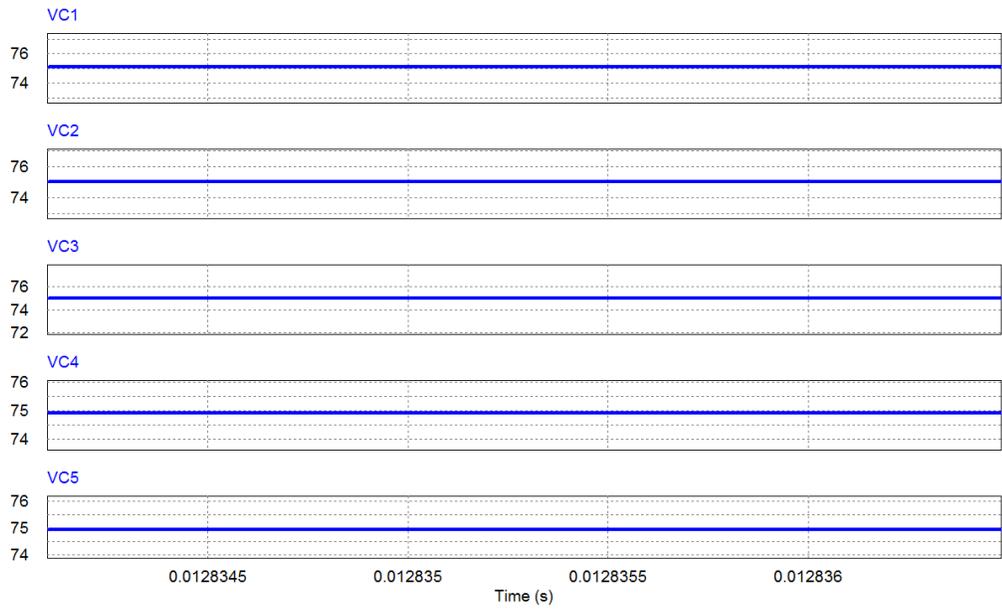


Figure 4-5 Capacitor voltage waveform

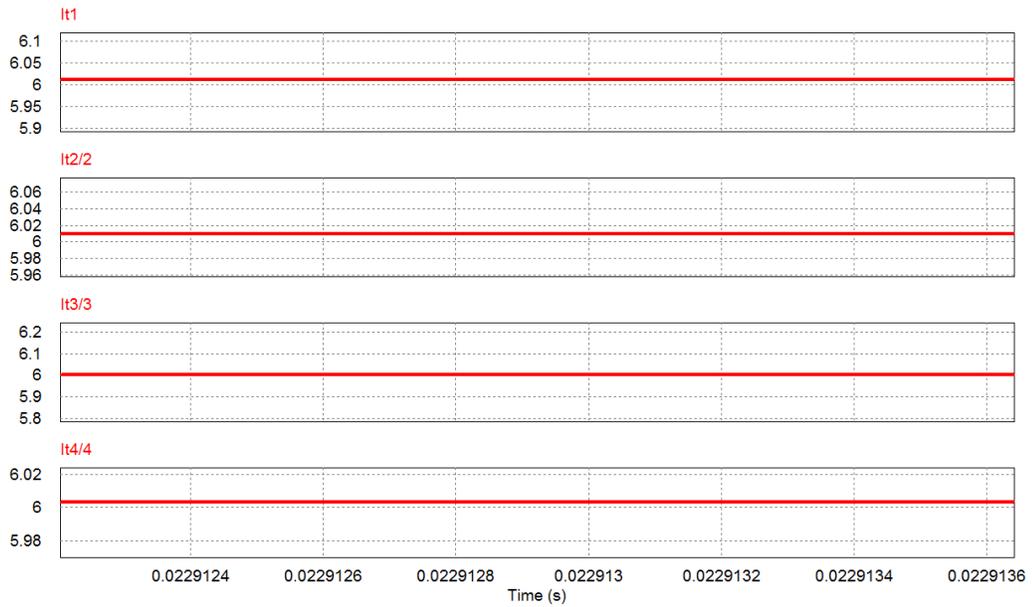


Figure 4-6 Total inductor current for all building blocks of each row

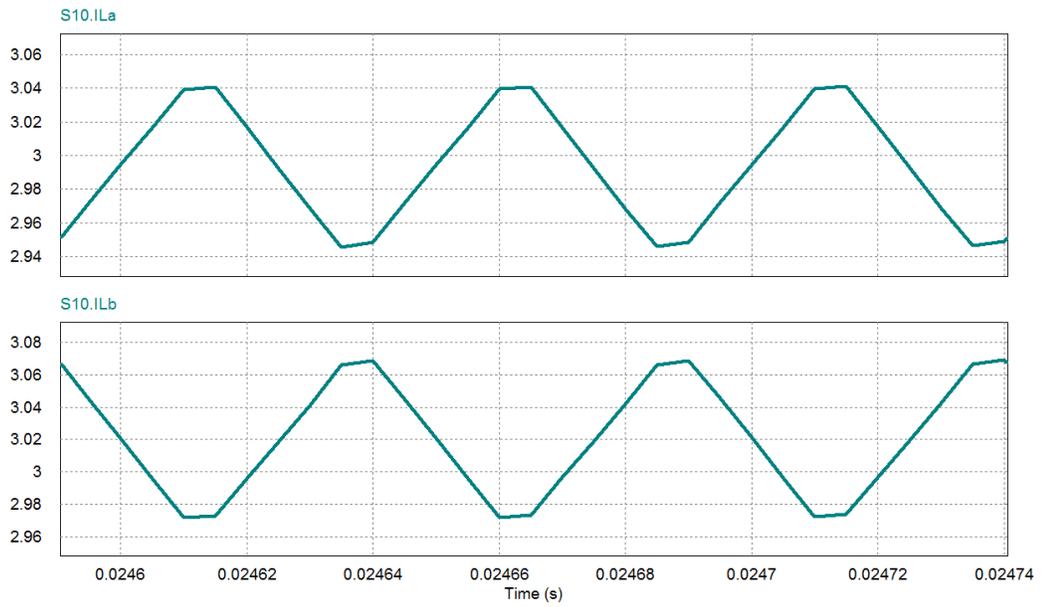


Figure 4-7 Separate coil current of the mutually coupled inductors

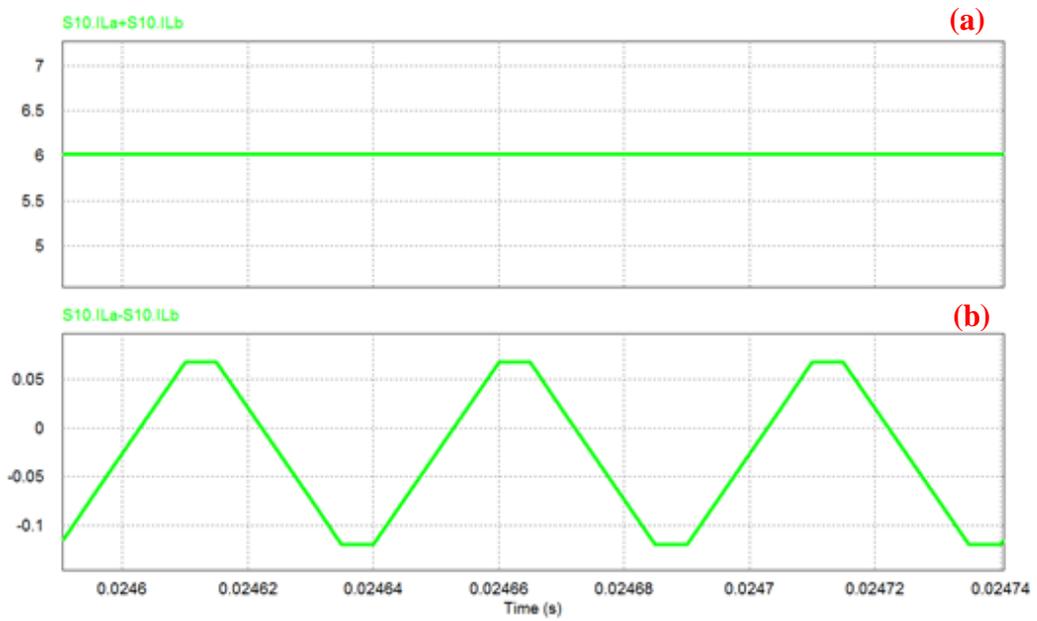


Figure 4-8 (a) Total current; (b) Current difference waveforms of certain mutually coupled

inductors

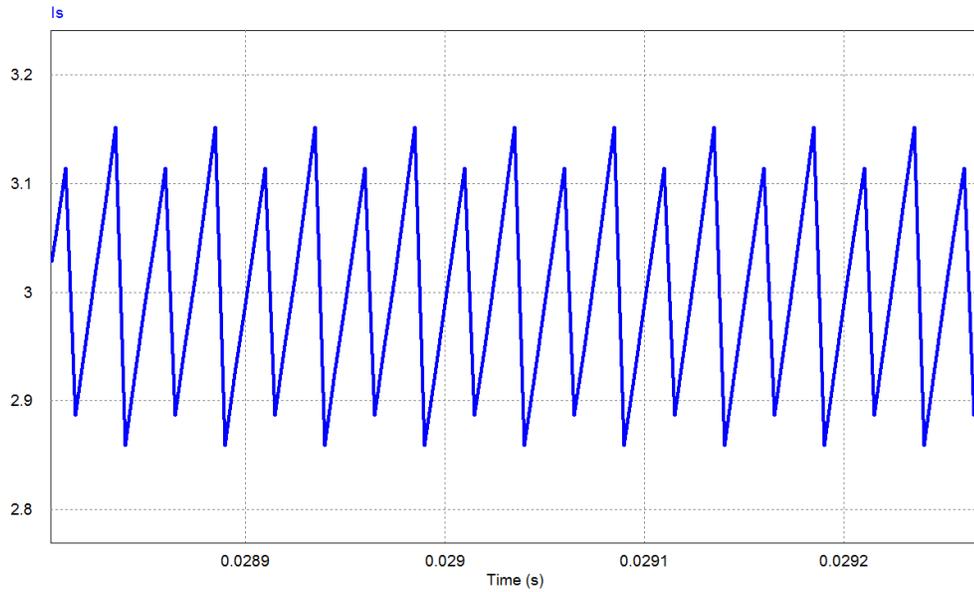


Figure 4-9 Input current waveform from power supply

Comparing close loop simulation results with open loop simulation results, the effectiveness of the proposed control algorithm is verified. Similar conclusions could be drawn as discussed in Chapter 3.3.

## 5. HARDWARE IMPLEMENTATION

### 5.1 Power Stage Building Block Implementation/PCB Design

#### 5.1.1 Component Selection

First of all, H-bridge (4 switches, two legs) needs to be selected/designed very carefully. Based on the design example shown in Chapter 3.2, the blocking voltage for each switch is  $75 * 2 = 150V$ , the average current flowing through drain-source is 3A. In this case, considering safety margin for the voltage and current rating. The maximum blocking voltage for each switch should be around 250~300V, the maximum drain-source current should be rated at 4.5A~6A. Additionally, considering the efficiency and power density, the drain-source on resistance should be as small as possible.

The first option is using separate switches and driver circuits to build the H-bridge. This can be much more flexible and avoid over design. However, this may complicate the design process and decrease the overall power density because of the separate design (non-compact). Considering the aim of increasing power density, integrated H-bridge with its driver circuit can be an option. The compact size of the integrated component makes it a good candidate. After searching all the possible options online, the integrated power module IRSM505 by International Rectifier is the final choice. It has 3 phase in a tiny package which is targeted for the small applicant motor drive applications such as energy efficient fans and pumps. In our case, we can use 2 of all the 3 phases for our design.

As for the coupled inductor selection, it has self-inductance as  $L = 6.375mH$  and average current as 3A from the previous design example. Final selection is Triad

Magnetics: CMT-8112. It's rated at 8 mH, 5.6A for each winding. The dimension is very small 1.45" x 1.35" x 0.8" which makes it fit for the higher power density requirement. This compact size characteristics is especially valuable when it's compared with separate inductance of 8 mH rated at 5.6A.

15V is needed for the IRSM505 to operate. The H-bridge is connected across two consecutive DC-link capacitors. For the gate drivers, they are referred to the negative side of the lower capacitor. Similarly, PWM signals from the digital controller are also referred to the negative side of the lower capacitor as above. Considering the integrity of the whole system, external power supply for ICs are not recommended. In this case, non-isolated voltage regular whose input is from the DC-link capacitor clamp voltage is considered. Using this strategy for each row, they can be operating independently by creating the "floating ground" for each level. This enables modular multilevel converter topology to be applied to arbitrary number of levels.

Table 5-1 shows the major component selection for the power stage building blocks.

Table 5-1 Major component selection for the power stage building blocks

Component	Value	Dimension	Description
Common Mode Choke	8 mH	1.45" x 1.35" x 0.8"	Triad Magnetics: CMT-8112
Capacitor	10uF	1.240" x 0.591"	EPCOS (TDK) B32774D4106K
H-bridge	250V, 4.6A	1.14" x 0.67"	International Rectifier IRSM505-084 (SMD)
Voltage Regulator	110V~450V to 15V	1.30" x 1.22" x 0.81"	Tamura: EPM1510SJ

### 5.1.2 Printed Circuit Board (PCB) Design

Some considerations for designing the printed circuit board (PCB) are: a) capacitor should be placed as close to H-bridge as possible in order to absorb the switching noise; b) avoiding recirculating between power circuit and signal/control circuit; c) let the path from power flow to ground as short as possible; d) try to deliver as much compact PCB design as possible.

Figure 5-1 shows the PCB of power stage building block with dimension designed by Altium Designer.

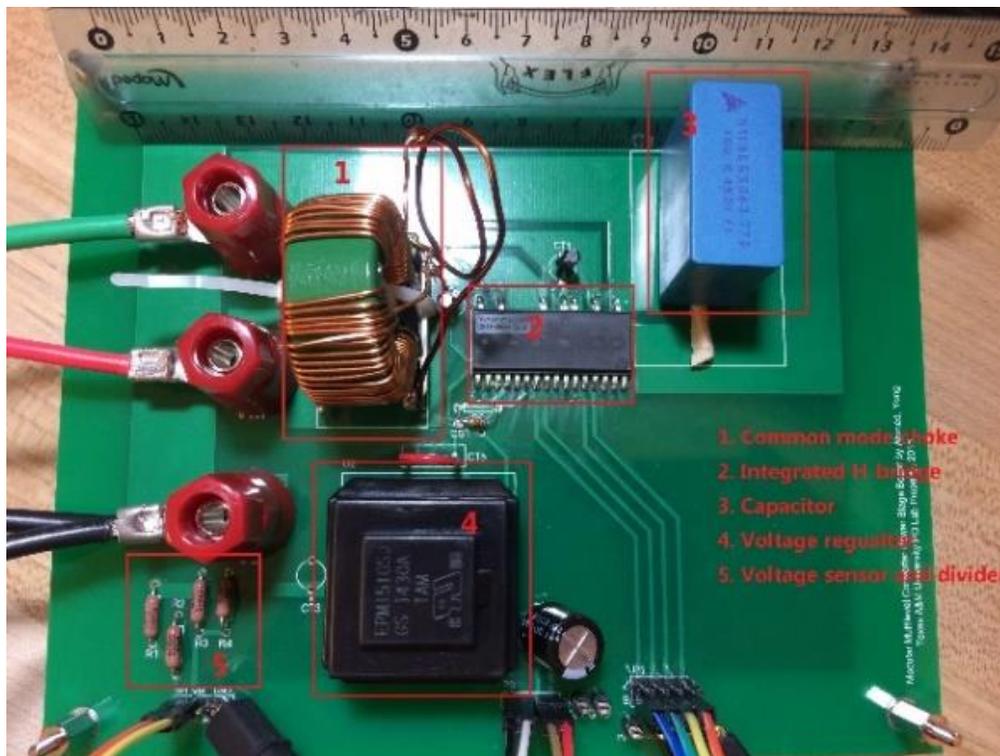


Figure 5-1 PCB of power stage building block. 1) Mutually coupled inductors/common mode choke; 2) Integrated H-bridge IRSM505-084; 3) Film Capacitor;

4) Voltage regulator; 5) Voltage sensor and divider

From the figure above, all of the passive components are very small and placement is compact which increase the overall power density. Considering the power loss and heat dissipation issues of the integrated H-bridge, heat sink is needed for safety operation. The power loss consists of two major parts: conduction loss and switching loss. Conduction loss can be calculated by using  $I_{DS}^2 * R_{on}$ . The on resistance  $R_{on}$  is a function of temperature, however, it would be a reasonable approximation based on the typical value given in the data sheet. In this case, the conduction loss can be assumed to be proportionally to only  $I_{DS}^2$ . The switching loss is somehow difficult to estimate because of the parasitic parameters of MOSFET. From the perspectives of capacitor charging and discharging, switching loss is proportionally to  $V^2$ , where  $V$  is the blocking voltage across the MOSFET. Hence, the higher blocking voltage, the more switching loss. However, increased drain-source current can also contribute to the increased switching loss, it's just not that significant compared to the increased blocking voltage. The thermal resistance of the heat sink could be designed based on these concepts.

## **5.2 Controller Module Implementation/PCB Design**

As discussed in Chapter 4, 2 ADC inputs and 4 PWM outputs are required for the digital microcontrollers. The ADC inputs are DC which means the ADC sampling frequency can be relatively low. Maximum switching frequency is 20KHz in this design. The resolution of PWM module should be high in order to achieve a perfect capacitor voltage balancing which is the basis of current balancing of coupled inductors. The clock frequency should be fast enough for the sake of reducing the delay of digital feedback

control loop. The upper switch and lower switch are operating in complementary mode. This means that PWM module which has complementary output mode is a preference in this design.

A very popular digital microcontroller option is TI DSP 28335. It's able to fulfil all the performance discussed above. However, the price is expensive and it's over designed considering the performance required in my topology. In order to improve the cost effectiveness of this design, MCUs from microchip and Atmel are alternatives. These two companies have equivalent MCUs product for a wide range of price and performance. Additionally, most of the programming is user friendly C/Assembly based. After searching and comparing, dsPIC33FJ06GS102A from Microchip is finalized. The architecture is 16-bit and it's designed for SMPS & digital power conversion applications. The high-speed PWM module has two pairs of PWM outputs. Supported PWM modes are standard edge-aligned, true independent output, complementary, center-aligned, push-pull, multi-phase, variable phase, fixed off-time, current reset, and current-limit. ADC is 10-bit resolution with maximum 2 Msps conversion rate. The controller module PCB is shown in Figure 5-2.

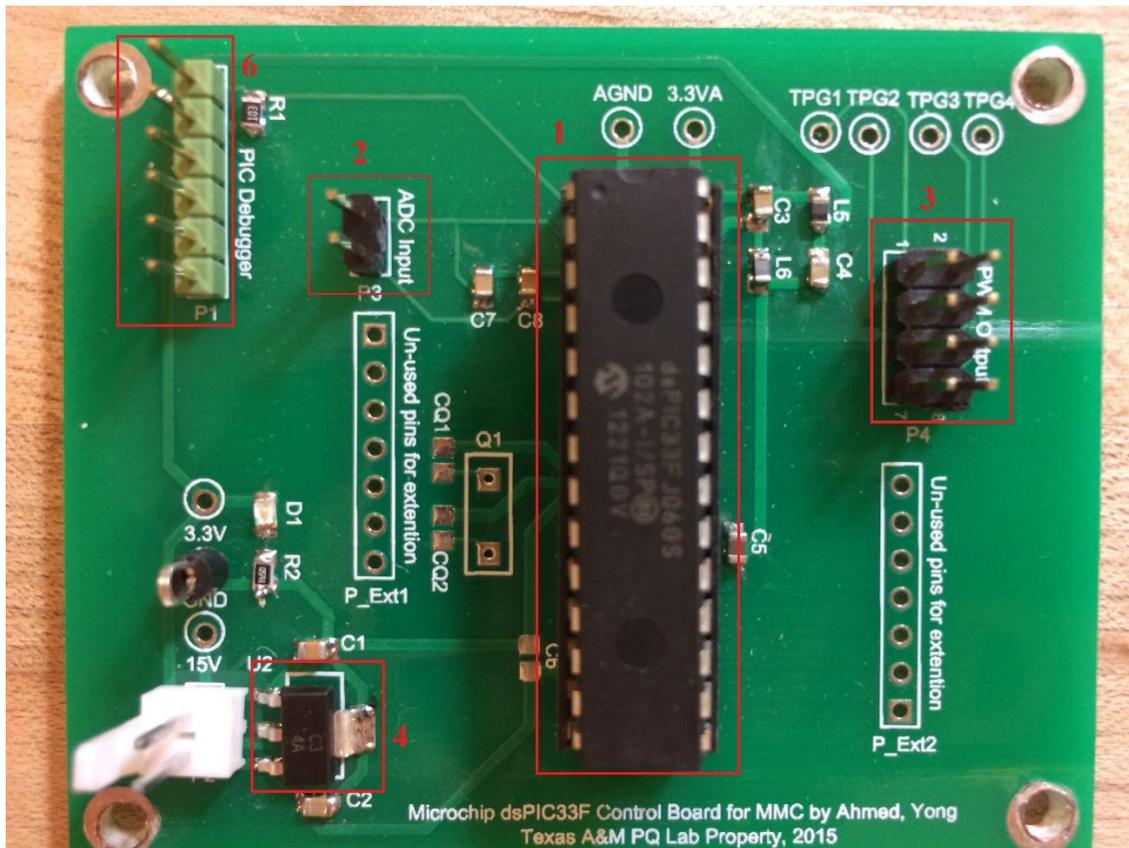


Figure 5-2 PCB of controller module. 1) Microchip dsPIC33FJ06GS102A MCU; 2) ADC input; 3) 4-channel PWM outputs for H-bridge; 4) Voltage regulator from 15V to 3.3V; 5) PICkit 3 debugger connection

### 5.3 Prototype System and Experimental Result

The 4-level prototype system is shown in Figure 5-3.

This system has three rows which consists of six power stage modules and three controller modules. Looking from right to left, it's like a triangular structure. We can predict that this configuration can be easily propagated to a high number of level when the input voltage increases.

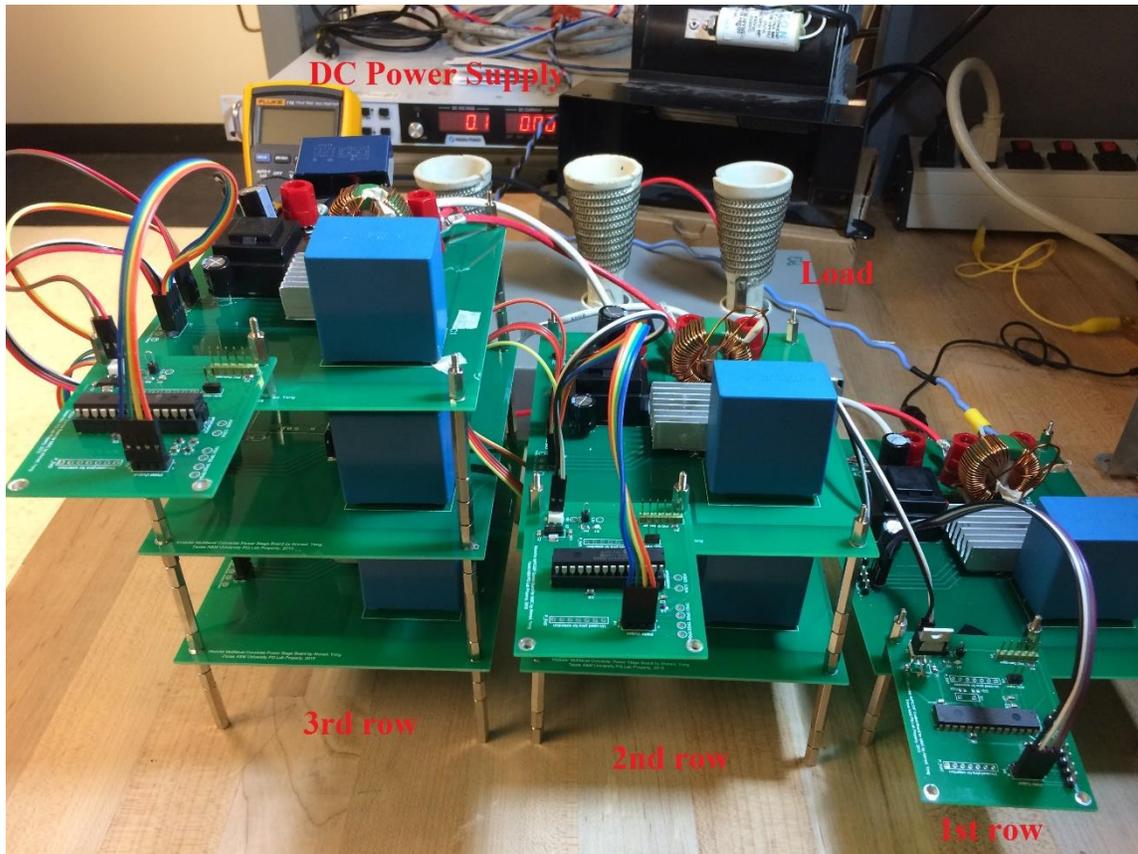


Figure 5-3 The 4-level prototype system

The experimental voltage and current waveforms are shown as in the following. Figure 5-4 and 5-5 show the capacitor voltages which are balanced. Figure 5-6 shows the total current of single coupled inductors for each row. Figure 5-7 shows the current waveform of single winding for coupled inductors at each row. Figure 5-8 shows current waveforms of each winding for coupled inductors at 1st row. Figure 5-9 is current difference of coupled inductors at each row. Figure 5-10 is the output current of DC power supply.

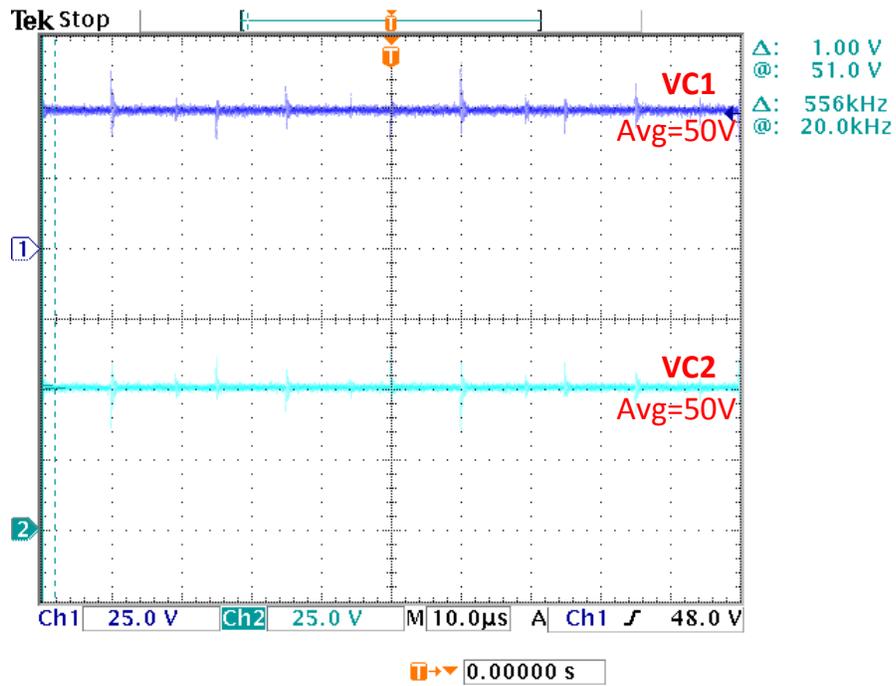


Figure 5-4 Capacitor voltage waveform  $V_{C1}$  and  $V_{C2}$

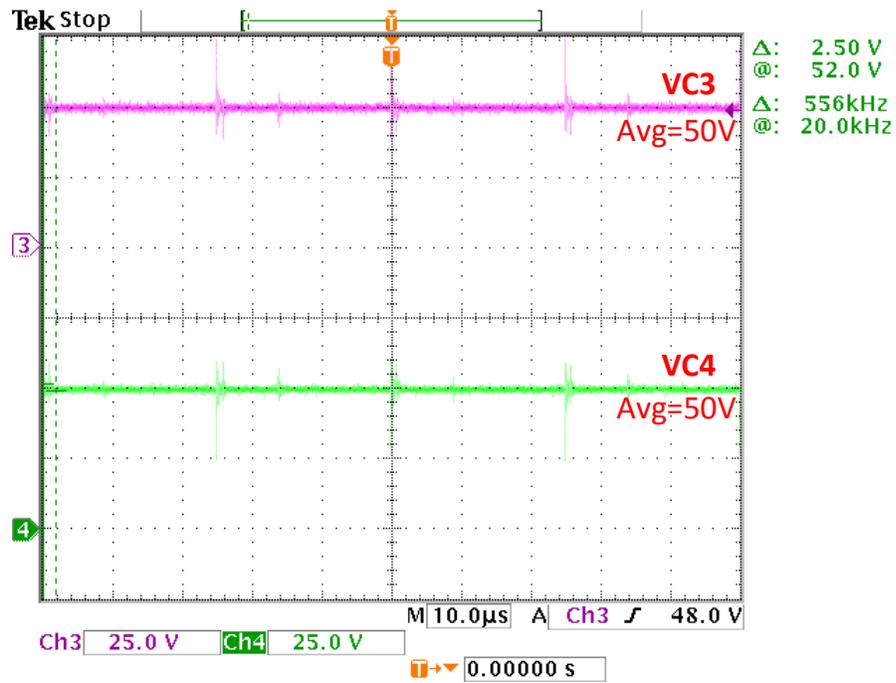


Figure 5-5 Capacitor voltage waveform  $V_{C3}$  and  $V_{C4}$

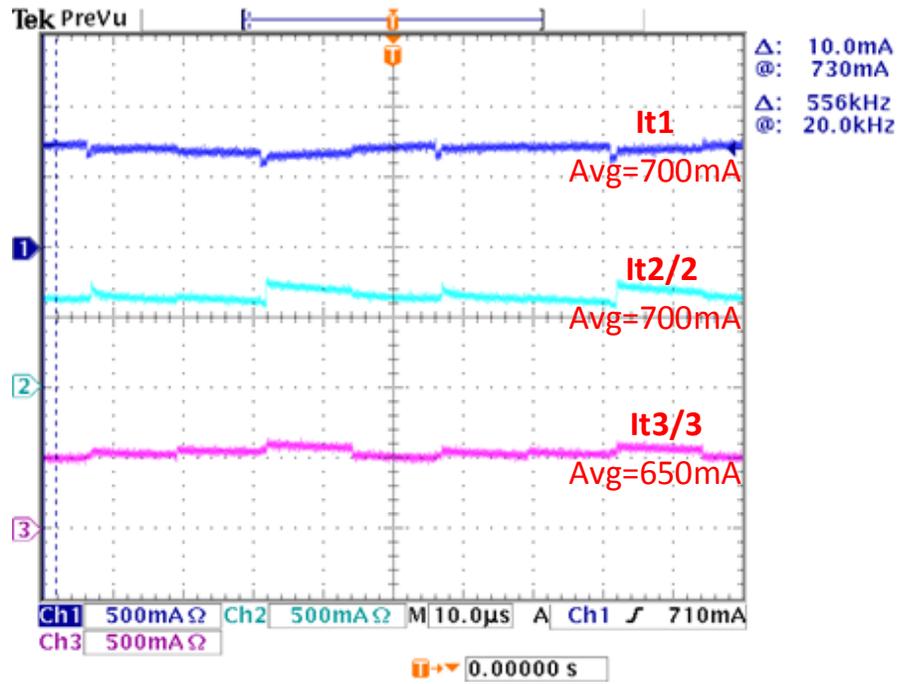


Figure 5-6 Total current of single coupled inductors for each row

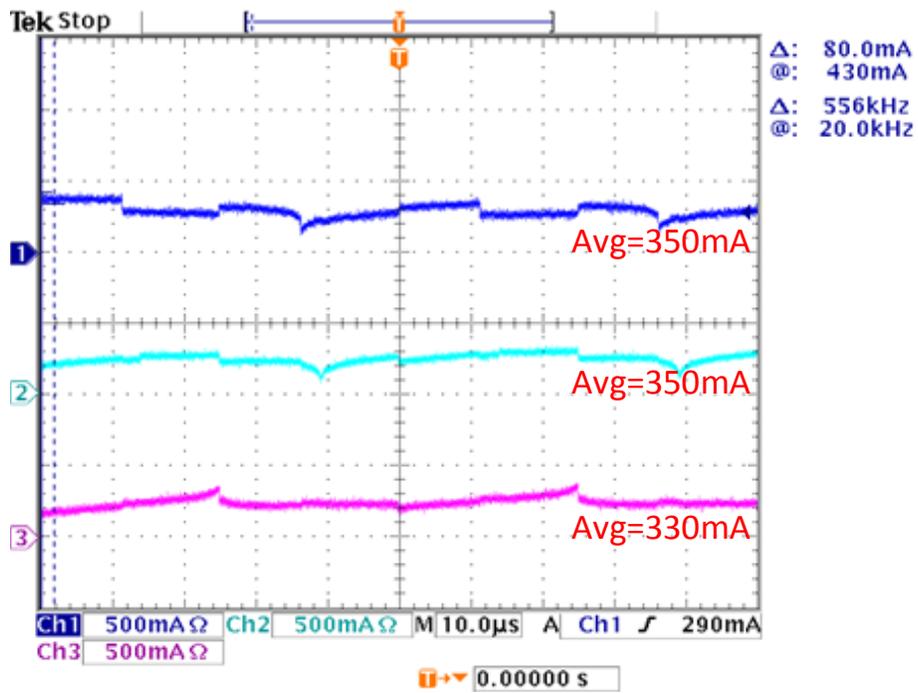


Figure 5-7 Current waveform of single winding for coupled inductors at each row

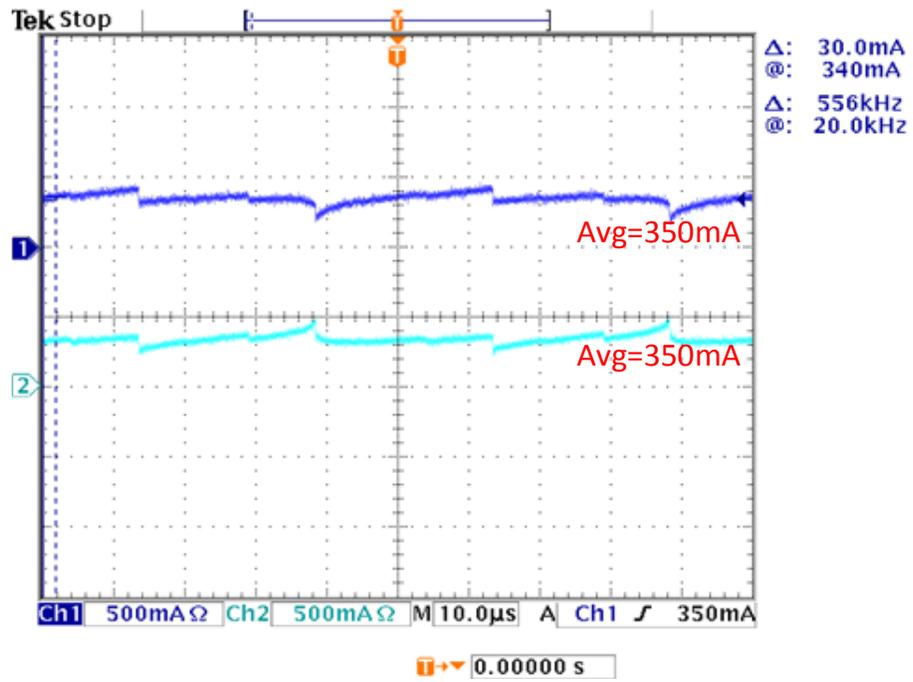


Figure 5-8 Current waveforms of each winding for coupled inductors at 1<sup>st</sup> row

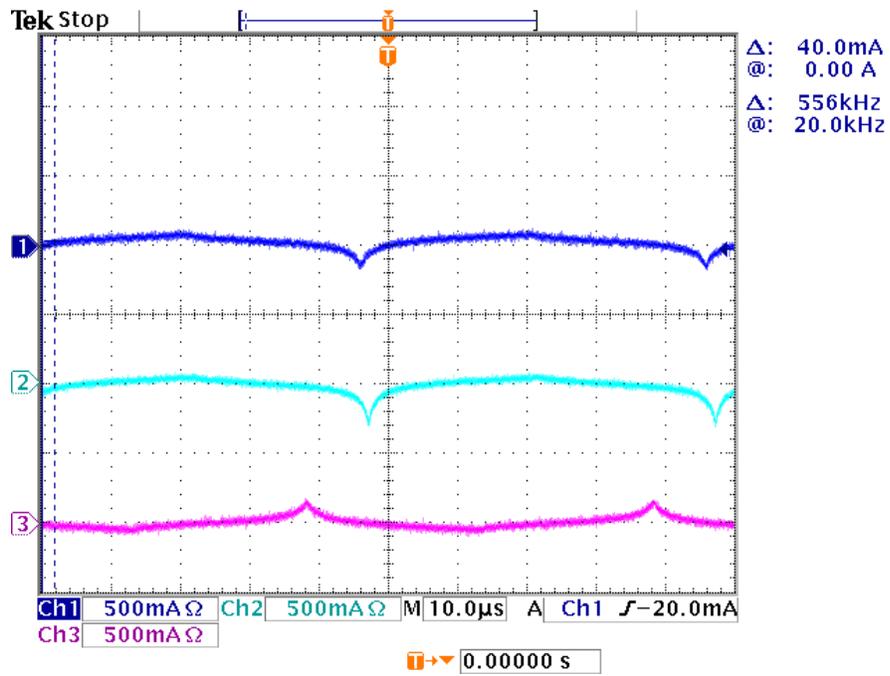


Figure 5-9 Current difference of coupled inductors at each row

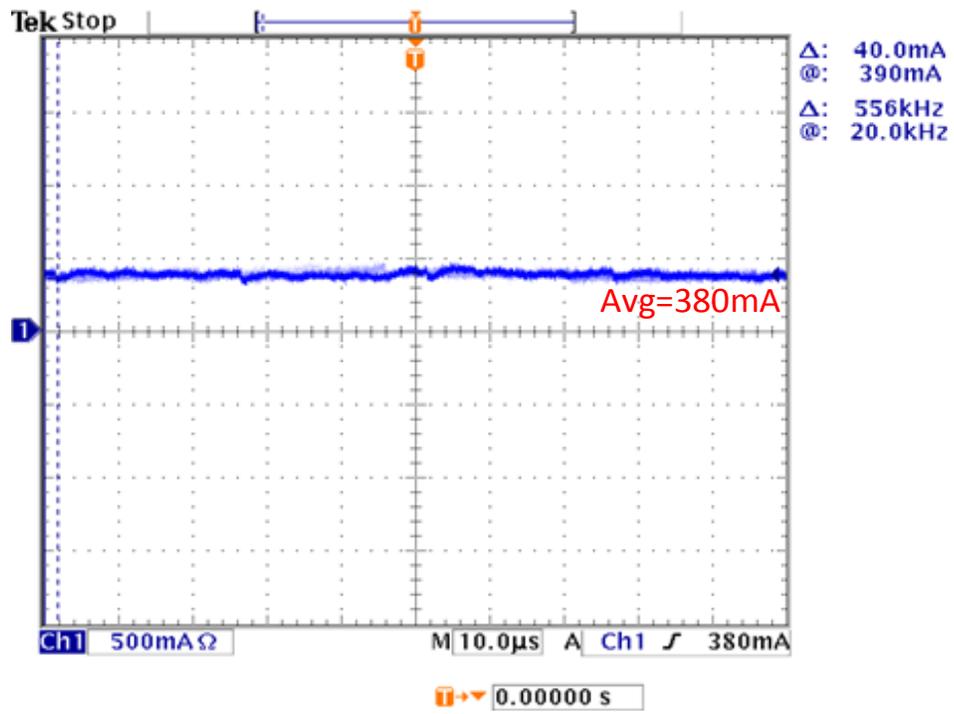


Figure 5-10 Output current of DC power supply

## 6. CONCLUSION AND FUTURE WORK

### 6.1 Conclusion

A new modular multilevel DC-DC converter with high power density and simplified localized voltage balancing control is proposed. In the proposed configuration, converter building blocks with the same power handling capability are connected in parallel in each row. Converter building block consists of an H-bridge and mutually coupled inductors whose total current is nearly ripple free. These features are shown to reduce the voltage ripple of DC-link capacitors significantly, leading to a smaller capacitance and size. An optimized control algorithm with voltage feedback PI loop is proposed resulting in the elimination of current sensors. This, reduces overall system complexity and increases cost-effectiveness. Significant ripple reduction of the inductor current and capacitor voltages is observed based on the simulation and prototype of multi-level systems. With a fully modular power stage module and localized control module, a system of arbitrary number of level can be built by stacking modules thereby contributing to enhanced system redundancy.

A 4-level prototype system is built. The experiment results show the voltage and current abilities of the proposed configuration. Additionally, the effectiveness of the proposed localized control strategy is verified.

### 6.2 Future Work

- Increase the power rating of the prototype system

- Use separate MOSFETs and their corresponding driver circuit to replace the current integrated H-bridge
- Focus on increasing the efficiency of this configuration compared to convention topologies
- Check a larger system with more number of levels
- Investigate the load transient response

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