EQUALIZATION ARCHITECTURES FOR HIGH SPEED ADC-BASED SERIAL I/O RECEIVERS

A Dissertation

by

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ABSTRACT

The growth in worldwide network traffic due to the rise of cloud computing and wireless video consumption has required servers and routers to support increased serial I/O data rates over legacy channels with significant frequency-dependent attenuation. For these high-loss channel applications, ADC-based high-speed links are being considered due to their ability to enable powerful digital signal processing (DSP) algorithms for equalization and symbol detection. Relative to mixed-signal equalizers, digital implementations offer robustness to process, voltage and temperature (PVT) variations, are easier to re-configure, and can leverage CMOS technology scaling in a straight-forward manner. Despite these advantages, ADC-based receivers are generally more complex and have higher power consumption relative to mixed-signal receivers. The ensuing digital equalization can also consume a significant amount of power which is comparable to the ADC contribution. Novel techniques to reduce complexity and improve power efficiency, both for the ADC and the subsequent digital equalization, are necessary.

This dissertation presents efficient modeling and implementation approaches for ADC-based serial I/O receivers. A statistical modeling framework is developed, which is able to capture ADC related errors, including quantization noise, INL/DNL errors and time interleaving mismatch errors. A novel 10GS/s hybrid ADC-based receiver, which combines both embedded and digital equalization, is then presented. Leveraging a time-interleaved asynchronous successive approximation ADC architecture, a new structure for 3-tap embedded FFE inside the ADC with low power/area overhead is used. In addition, a dynamically-enabled digital 4-tap FFE + 3-tap DFE equalizer architecture is introduced, which uses reliable symbol detection to

achieve remarkable savings in the digital equalization power. Measurement results over several FR4 channels verify the accuracy of the modeling approach and the effectiveness of the proposed receiver. The comparison of the fabricated prototype against state-of-the-art ADC-based receivers shows the ability of the proposed architecture to compensate for the highest loss channel, while achieving the best power efficiency among other works.

To My Mom and Dad,

who taught me most of what I know,

and showed me the way to learn the rest.

To My wife Basma,

the joy of my life,

and my two little angels, Omar and Malik.

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1. INTRODUCTION

The rapid increase in the number of internet users, as well as the advances in network-enabled devices and connections, led to a continued growth in the global IP traffic over the past few years. Faster broadband speeds are allowing more users to access emerging services such as cloud computing and video on demand (VON) streaming services. Fig. 1.1 shows the projected growth of global internet traffic, in PetaBytes (10^{15} Bytes) per month, where the total IP traffic is expected to nearly triple from 2014 to 2019 [1]. This increase in internet traffic requires an equivalent improvement in data centers, in terms of the number of servers and their data rates, which translates to more power dissipation. This is one of the main drivers of the high speed serial link communications market.

As the data rates of wire-line communication links increases, channel impairments such as skin effect, dielectric loss, fiber dispersion, reflections and cross-talk become more pronounced. This warrants more interest in analog-to-digital converter (ADC)-based serial link receivers (Fig. 1.2), as they allow for more complex and flexible back-end digital signal processing (DSP) relative to binary or mixed-signal receivers [2–5]. Utilizing this back-end DSP allows for complex digital equalization and more bandwidth-efficient modulation schemes, while also displaying reduced process/voltage/temperature (PVT) sensitivity. Furthermore, these architectures offer straightforward design translation and can directly leverage the area and power scaling offered by new CMOS technology nodes.

Despite these advantages, ADC-based receivers are generally more complex and have higher power consumption relative to mixed-signal receivers [6]. While significant improvements in multi-GS/s ADC figure-of-merit (FOM) have been recently

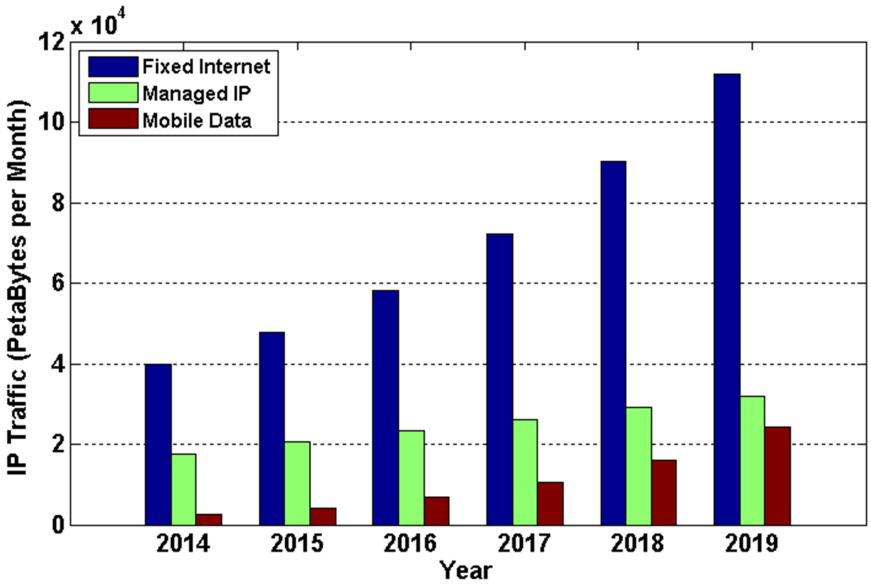


Figure 1.1: Expected growth in global internet traffic.

achieved [7–9], the ensuing digital equalization can also consume a significant amount of power which is comparable to the ADC contribution [2]. Thus, in order to reduce the power of these ADC-based receiver systems, techniques to improve equalization efficiency and relax ADC resolution requirements have been developed. Non-uniform ADC quantization has been proposed to enable efficient implementations of digital decision feedback equalizers (DFEs) with either a minimal number of comparators [10], a BER-optimal threshold settings [11] or a thermometer-code selection-based architecture [5]. However, these designs do not allow for any digital feed-forward equalization (FFE), which is useful for canceling pre-cursor and long-tail ISI. Other promising approaches included embedding partial analog equalization inside the ADC [12–14] which allows for both reduced ADC resolution and also relaxes the requirements of the following digital equalization [15]. On the digital equalization front, techniques such as parallelized distributed arithmetic [16] and multiple supply and frequency domains [17] have been utilized to improve the digital equalizer power

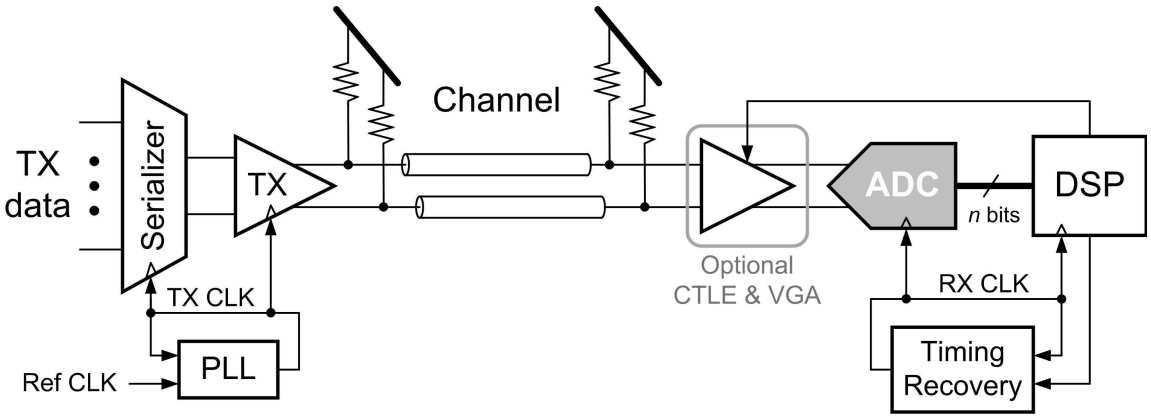


Figure 1.2: Block diagram of ADC-based serial link receiver.

efficiency.

This research targets the design of efficient ADC-based receiver implementation with 10Gb/s data rate in 65nm CMOS. The ideas proposed in this work, however, can be extended to higher data rates, and can efficiently leverage CMOS scaling to more advanced technology nodes.

1.1 Dissertation Organization

Section 2 presents a background overview on the topic of ADC-based receiver design. An introduction on sampling and quantization in ADCs is first presented. Challenges in the design of multi-Gbps time interleaved ADCs are then discussed. Details on the design of one of the critical blocks, the clock generation and timing calibration circuitry, is reviewed. Brief discussion of high-speed link architectures and different receiver equalization techniques, namely feed-forward equalization (FFE), infinite impulse response equalizer (IIR) and decision feedback equalization (DFE), are given.

The remainder of this work focuses on the modeling, design and implementation of power efficient ADC-based receiver architectures. In section 3, a statistical modeling

framework is presented, which can predict the system performance both efficiently and accurately, down to the target bit error rate (BER) of 10^{-12} or lower. The framework builds on state of the art statistical binary links receiver simulation tools [18, 19], by extending it to the ADC-based receiver case. ADC-related non-idealities such as quantization noise, linearity errors and time interleaving errors are included in the statistical model. The model is then used to evaluate different techniques to efficiently embed partial analog equalization inside the front-end high-speed ADC, potentially improving the efficiency of the full ADC-based receiver [15]. Two case studies of high speed ADCs with embedded equalization are considered [13,14], where good matching between the model and measurement results verifies the the accuracy of the model.

Next, a novel hybrid ADC-based receiver architecture that combines embedded and digital equalization is discussed in section 4. By dynamically enabling the digital equalizer on a per-symbol basis, considerable amount of power of the digital equalization may be saved, where the concept of reliable symbol detection is used to ensure the digital equalizer is only enabled when the received symbol is unreliable, and disabled otherwise. A receiver prototype is fabricated in 65nm CMOS, with an asynchronous SAR ADC architecture used for the front-end ADC. Three taps of partial analog FFE are efficiently embedded inside the capacitive DAC of the ADC, and 4 taps of digital FFE plus 3 taps of digital DFE are fully synthesized as the back-end equalizer. Measurement results over different FR4 channels prove the effectiveness of the proposed architecture, where comparison with state of the art ADC-based receivers shows that the architecture can equalize for the highest loss channel, while achieving the best power efficiency [20].

Finally, section 5 concludes the research presented, and suggests some interesting ideas to extend the work in the future.

2. BACKGROUND ON HIGH-SPEED ADC-BASED RECEIVERS

This section explains briefly some concepts that are closely related to the design of ADC-based serial link receivers. First, basic concepts of ADC operation, the sampling and the quantization, are revised. Next, the idea of time interleaving, which enables multi-Gbps operation of ADCs, is discussed. Implications that arise due to mismatches in time interleaving architecture are analyzed, showing how those non-idealities can affect the performance of the ADC. Following this, the design of the clock generation and timing calibration circuitry, which is curial to the operation of the time interleaved structure, is reviewed. Different equalization and signaling architectures used in high speed link systems are then presented.

2.1 Basic ADC Concepts, Sampling and Quantization

The basic operation of any ADC includes two main quantization functions, sampling of the input, which may be viewed as quantization in the time domain, followed by amplitude quantization into discrete digital levels. In order to ensure proper reconstruction of the signal, the Nyquist criteria must be fulfilled during the sampling, where the input bandwidth must be kept below one half of the sampling frequency to prevent aliasing [21]. In ADC-based high speed link applications, the channel loss limits the bandwidth of the input signal, eliminating the need for explicit ant-aliasing filter.

While it is theoretically possible to fully recover the signal after sampling, the jitter on the sampling clock is going to add an error to the output signal, since the ideal sampling instants are modulated by the sampling clock jitter. The error due to jitter may be written as [22]:

$$\Delta X[nT] = \epsilon[nT] \left. \frac{dX(t)}{dt} \right|_{(t=nT)} \tag{2.1}$$

Where $\epsilon[nT]$ is the jitter at sampling instant. Assuming an input sine wave:

$$X(t) = Asin(\omega_{in}t) \tag{2.2}$$

The error may be given as:

$$\Delta X[nT] = \epsilon[nT]A\omega_{in}cos(\omega_{in}nT) \tag{2.3}$$

This introduces a limit on the maximum SNR an ADC could achieve under certain jitter conditions. With the sine wave input assumption, this maximum SNR may be given as [22]:

$$\begin{aligned} SNR &= \frac{P_{signal}}{P_{error}} = \frac{A^2/2}{A^2\omega_{in}^2\epsilon_J^2/2} = \frac{1}{\epsilon_J^2\omega_{in}^2} \\ SNR_{dB} &= -20 \cdot log(\epsilon_J\omega_{in}) \end{aligned} \tag{2.4}$$

Where ϵ_J is the rms value of the jitter.

To show the effect of jitter on the SNR degradation, a MATLAB model is used, where a sine wave is sampled with the presence of random jitter, and the resulting SNR is extracted from the output spectrum. The results are shown in Fig. 2.1 for different input frequencies, and equation 2.4 is also plotted for comparison. As expected, the simulation results and the calculated values match each other closely.

In reality, however, the input signal may not always be sinusoidal. It can be proven [23] that for the case of a random input signal which has a rectangular spectrum with maximum frequency of ω_{in}, the SNR is given as:

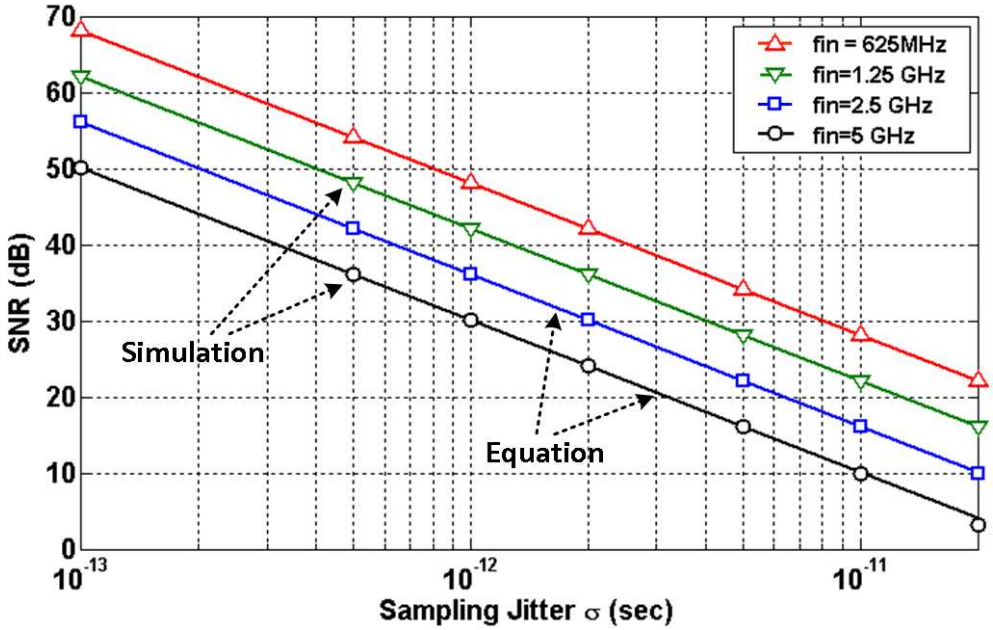


Figure 2.1: Effect of sampling jitter on SNR of signal.

$$SNR = \frac{3}{\epsilon_J^2 \omega_{in}^2}$$
$$SNR_{dB} = -20 \cdot log(\epsilon_J \omega_{in}) + 4.77 \tag{2.5}$$

Next, the error due to quantization of the input signal is considered. While sampling may be viewed as quantization of the input signal in the time domain, amplitude quantization, on the other hand, may be viewed as "area sampling" of the input probability density function (PDF) [24]. The quantization process works to concentrate the PDF of the input signal over each quantization interval into a single quantized output level, converting the continuous input PDF into a discrete output probability mass function (PMF), as shown in Fig. 2.2. Assuming uniform quantization, this is mathematically equivalent to performing a convolution operation between the in-

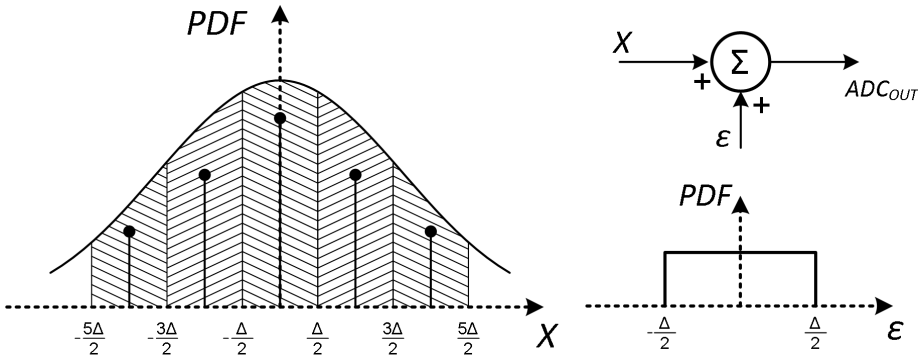


Figure 2.2: Area sampling of input PDF and equivalent quantization noise model.

put PDF and a uniform PDF, with width equal to the quantization interval, and then multiplying the resulting PDF with an impulse train to obtain the final PMF. This model has been presented by Widrow as the pesudo-quantization noise (PQN) model [25], where under certain conditions, the quantization noise may be assumed to be uniform over the the quantization interval, and the effect of quantization may be approximated as an additive noise term.

Now, assuming an ADC with N-bit resolution, and full scale equal to V_{FS}, the width of the quantization interval is given by:

$$\Delta = \frac{V_{FS}}{2^N} \tag{2.6}$$

The quantization noise power, assuming a uniform error PDF over one quantization interval, may then be calculated as:

$$\begin{aligned} E(\epsilon_q^2) &= \frac{1}{\Delta}\int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} \epsilon^2 d\epsilon \\ &= \frac{\Delta^2}{12} \end{aligned} \tag{2.7}$$

Assuming a sinusoidal input with full scale amplitude leads to the well-known SNR formula:

$$\begin{aligned} SNR &= 1.5 \times 2^{2N} \\ SNR_{dB} &= 6.02N + 1.76 \end{aligned} \tag{2.8}$$

The formula suggests that the SNR of the ADC improves by 4X for every additional bit of resolution. Now, if the input signal is assumed to be uniform rather than sinusoidal, the SNR changes slightly to:

$$\begin{aligned} SNR &= 2^{2N} \\ SNR_{dB} &= 6.02N \end{aligned} \tag{2.9}$$

Alternatively, assuming the input signal has a Gaussian random PDF, with the full scale set to $\pm 3\sigma$ of the random distribution, and assuming no quantizer overload [26], the SNR becomes:

$$\begin{aligned} SNR &= \frac{1}{3} \times 2^{2N} \\ SNR_{dB} &= 6.02N - 4.77 \end{aligned} \tag{2.10}$$

Comparing equations 2.8 and 2.10, a difference in SNR equivalent to more than one bit of resolution can be observed. Noting that equation 2.8 is usually used to extract the effective number of bits (ENOB) specification of an ADC, it's important to keep in mind that this number is calculated assuming a sinusoidal input signal, which may not be always be accurate when a different input, e.g. with Gaussian PDF,

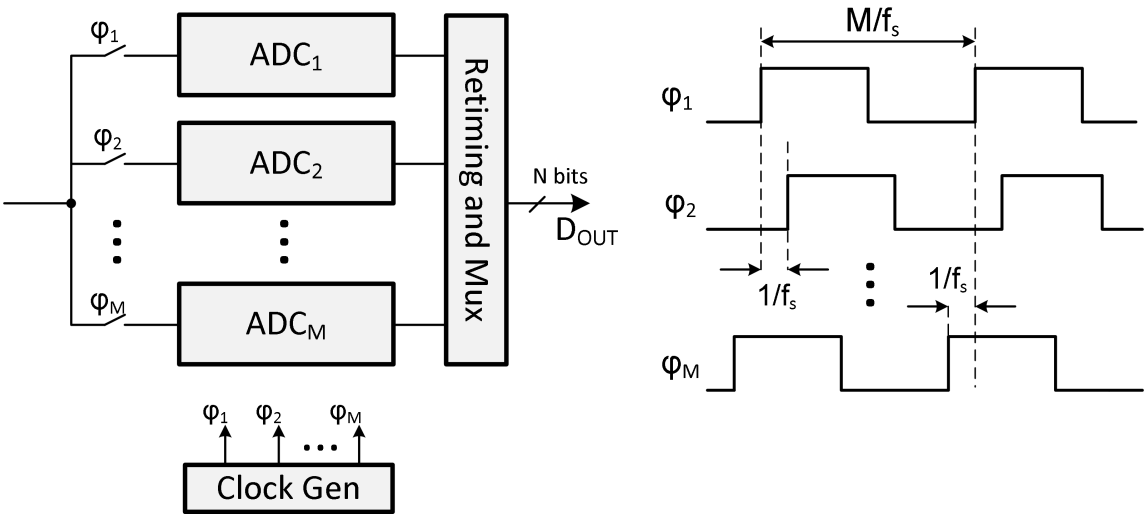


Figure 2.3: Block diagram of an N-way time-interleaved ADC.

is used. In general, when it comes to random input signals, the highest possible SNR that may be obtained from a uniform quantizer is obtained when the input PDF is uniform [26].

2.2 Time-Interleaving of ADCs

In order to enable multi-Gbps operation, time interleaving is usually incorporated in ADC design, as shown in Fig. 2.3. A time interleaved ADC consists of M sub-ADCs operating in parallel. Each sub-ADC operates at $1/M$ of the sampling frequency of the full ADC [27], enabling sampling rates higher than the technology limit. In reality, mismatches between the interleaved channels degrades the ADC performance, and must to be calibrated. These mismatches are usually due to three main types of errors: offset errors, gain errors and time skew errors [28, 29].

The output signal of an M-channel time interleaved ADC may be given as:

$$\begin{aligned} y(t) =& x(t) \sum_{k=-\infty}^{\infty} \delta(t - MkT) + x(t) \sum_{k=-\infty}^{\infty} \delta(t - (Mk+1)T) \\ &+ x(t) \sum_{k=-\infty}^{\infty} \delta(t - (Mk+2)T) + \dots \\ &+ x(t) \sum_{k=-\infty}^{\infty} \delta(t - (Mk+M-1)T) \end{aligned} \tag{2.11}$$

Where $\delta(.)$ denotes the delta Dirac function. The spectrum of this signal may be written as:

$$\begin{aligned} Y(f) =& X(f) \otimes \sum_{k=-\infty}^{\infty} \delta(f - \frac{kf_s}{M}) + X(f) \otimes \sum_{k=-\infty}^{\infty} \delta(f - \frac{kf_s}{M}) e^{-j2\pi \frac{f}{f_s}} \\ &+ X(f) \otimes \sum_{k=-\infty}^{\infty} \delta(f - \frac{kf_s}{M}) e^{-j2\pi \frac{2f}{f_s}} + \dots \\ &+ X(f) \otimes \sum_{k=-\infty}^{\infty} \delta(f - \frac{kf_s}{M}) e^{-j2\pi \frac{(M-1)f}{f_s}} \end{aligned} \tag{2.12}$$

Since each channel is sampled at f_s/M, this means that the spectrum at each channel output will contain images every kf_s/M, $k = 0, 1, 2, ...M-1$. Under ideal conditions, the phase difference between the interleaved channels results in canceling of all the images except for those at kf_s. In reality, however, mismatches between the interleaved channels will cause incomplete cancellation of the signal images, resulting in aliasing of the uncancelled images which produces errors at the output signal. In the following subsection, the three mismatch error sources are discussed, and there impact on the sampled signal is analyzed.

2.2.1 Offset Mismatch Error

The offset error arises in the ADC due to process variations in the comparator, leading to the threshold being slightly shifted from its nominal value. Mismatches in the offset voltage between the time interleaved channels result in degradation in the ADC performance. To quantify this degradation, a worst case scenario is assumed, where the offset voltage between interleaved channels toggles between $\pm V_{OF}$. This creates a tone at half the sampling frequency, which is added to the input signal, resulting in a spur in the output spectrum at $f_s/2$. The SNDR due to this error may be written as, assuming an input sine wave with full scale swing:

$$\begin{aligned} SNDR &= \frac{(V_{FS}/2)^2/2}{V_{OF}^2} = \frac{V_{FS}^2}{8 \cdot V_{OF}^2} \\ SNDR_{dB} &= 20 \cdot log\left(\frac{V_{FS}}{V_{OF}}\right) - 9.03 \end{aligned} \tag{2.13}$$

Where due to sampling at $f_s/2$, the offset signal power is V_{OF}^2 rather than $V_{OF}^2/2$.

Alternatively, if a random normal distribution of the offset voltage with standard deviation σ_{OF} is assumed, the resulting SNDR is:

$$\begin{aligned} SNDR &= \frac{(V_{FS}/2)^2/2}{\sigma_{OF}^2} = \frac{V_{FS}^2}{8 \cdot \sigma_{OF}^2} \\ SNDR_{dB} &= 20 \cdot log\left(\frac{V_{FS}}{\sigma_{OF}}\right) - 9.03 \end{aligned} \tag{2.14}$$

Comparing equations 2.13 and 2.14, it is obvious that from an SNDR perspective, the effect of a worst case offset mismatch with offset voltage $\pm V_{OF}$, is equivalent to the effect of a random Gaussian distributed offset mismatch , when the standard deviation is equal to V_{OF}.

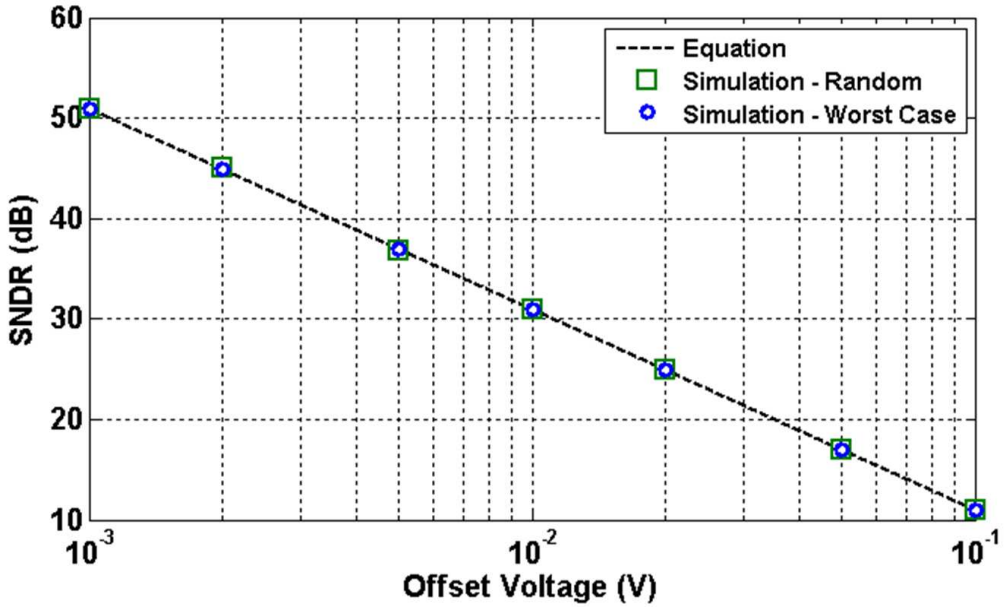


Figure 2.4: Effect of offset mismatch on SNDR of signal.

To demonstrate the effect of offset mismatch on ADC performance, a MATLAB model is used to calculate the SNDR of an ideally sampled signal, when both a worst case offset error and randomly distributed offset errors are added. The results are shown in Fig. 2.4, where an 8-channel time interleaved system is assumed with full scale voltage of 1V. For the Gaussian offset errors case, 10^3 transient simulations are performed, with a set of randomly generated offset voltages per simulation used as the offsets of the interleaving channel. The SNDR is then calculated based on the expected value (average) of the distortion across all simulations, excluding the dc offset error [30]. The results show perfect matching between the two simulation cases, and with the result obtained using equation 2.13 or 2.14, also plotted for comparison.

It's worth noting that since the offset error is added to the input, the error is independent of the input signal frequency. In addition, the SNDR degradation due

to offset error is independent on the time interleaving factor. In general, the offset error results in tones at kf_s/M, where $k = 0, 1, 2, ...M/2$ [28].

The gain mismatch error may be decomposed into two types, dc gain error and ac gain error, where the latter represents the bandwidth mismatch between the time interleaved channels. Each of the two errors will be considered separately, starting with the dc gain error, simply referred to as the gain error. To prevent confusion, the ac gain error will be referred to as the bandwidth error.

2.2.2 Gain Mismatch Error

Following a similar approach to the offset error , the effect of the gain mismatch may be quantified assuming worst case gain error variations, for which the dc gain will change between $(1+\epsilon_g)$ and $(1-\epsilon_g)$, meaning that the input signal will be multiplied by a sine wave at $f_s/2$ with amplitude equal to ϵ_g. Due to the multiplication, the resulting tones will appear at $fs/2 \pm f_{in}$, resulting in an SNDR given by:

$$\begin{aligned} SNDR &= \frac{(V_{FS}/2).^2/2}{(V_{FS}.\epsilon_g/2)^2/2} = \frac{1}{\epsilon_g^2} \\ SNDR_{dB} &= -20 \cdot log(\epsilon_g) \end{aligned} \tag{2.15}$$

The effect of the gain error may also be considered statistically. It may be proven that, assuming the gain error has a random distribution with Gaussian PDF, the SNDR is given by [31, 32] :

$$\begin{aligned} SNDR &\approx \frac{M}{M-1} \cdot \frac{1}{\sigma_g^2} \\ SNDR_{dB} &\approx -10 \cdot log\left(\frac{M-1}{M} \cdot \sigma_g^2\right) \end{aligned} \tag{2.16}$$

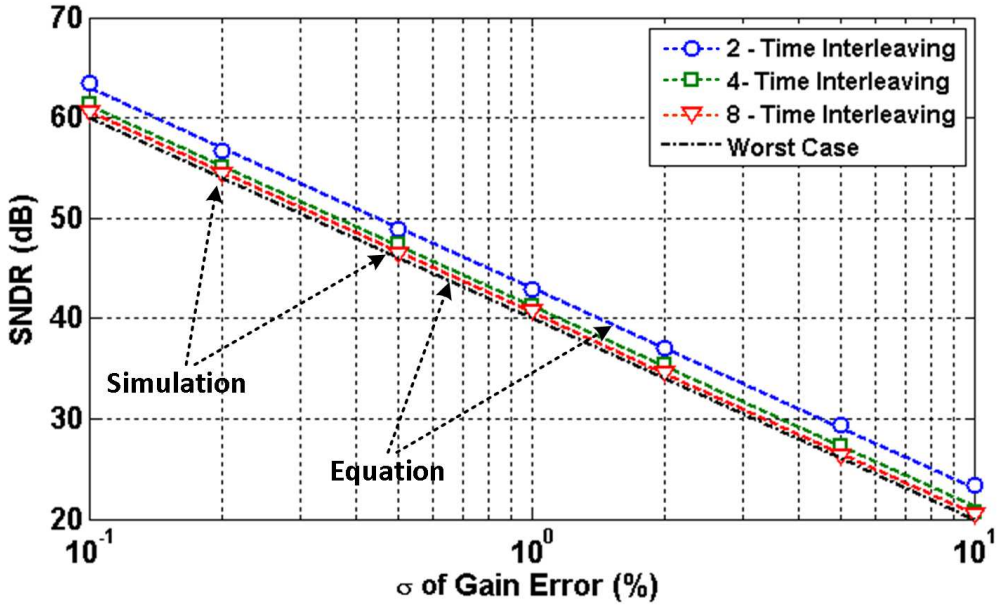


Figure 2.5: Effect of gain mismatch on SNDR of signal.

Where σ_g is the standard deviation of the gain error.

The effect of gain mismatch is simulated similar to the offset error case, and the results are shown in Fig. 2.5. As equation 2.16 suggests, the SNDR will have some dependence on the time interleaving factor. However, as the interleaving factor increases, the gain error effect becomes less dependent on the interleaving factor, and the SNDR approaches that of the worst case, showing a behavior similar to the offset error. The time interleaving dependence results in an SNDR difference of 3dB between $M = 2$ and $M = \infty$. Compared to the theoretical SNDR calculated by equations 2.15 and 2.16, the transient results match perfectly. The gain error is neither dependent on the input full-scale voltage nor the input frequency. In general, the gain error results in tones at $(i/M)f_s \pm fin$, where $i = 0, 1, 2, ...M/2$ [28].

2.2.3 Bandwidth Mismatch Error

Unlike dc gain error, bandwidth error will affect both the magnitude and the phase of the input signal. In order to find the effect of bandwidth error on SNDR, a single-pole system is assumed, where the nominal gain and phase are given by [33]

$$\begin{aligned} A(\omega) &= \frac{1}{\sqrt{1+(\omega/\omega_B)^2}} \\ \Phi(\omega) &= -tan^{-1}(\frac{\omega}{\omega_B}) \end{aligned} \tag{2.17}$$

Where ω_B is the bandwidth. Now, in order to find error due to bandwidth mismatch, the gain and phase errors are calculated as follows:

$$\frac{\Delta A}{\Delta \omega_B} = \frac{A}{\omega_B} \cdot \frac{(\omega/\omega_B)^2}{1+(\omega/\omega_B)^2} \tag{2.18}$$

$$\frac{\Delta t}{\Delta \omega_B} = \frac{1}{\omega_B}\frac{\Delta \Phi}{\Delta \omega_B} = \frac{1}{\omega_B^2} \cdot \frac{1}{1+(\omega/\omega_B)^2} \tag{2.19}$$

The error due to bandwidth mismatch may be expressed as [33]:

$$e(t) = (A+\Delta A)\cdot V_{in}(t+\Delta t) - A\cdot V_{in}(t) \approx \Delta A V_{in}(t) + A\frac{\partial V_{in}}{\partial t}\Delta t \tag{2.20}$$

For a sinusoidal input this reduces to:

$$e(t) \approx V_{in}(t)\cdot(\Delta A + j\omega A \Delta t) \tag{2.21}$$

The SNDR may be written as:

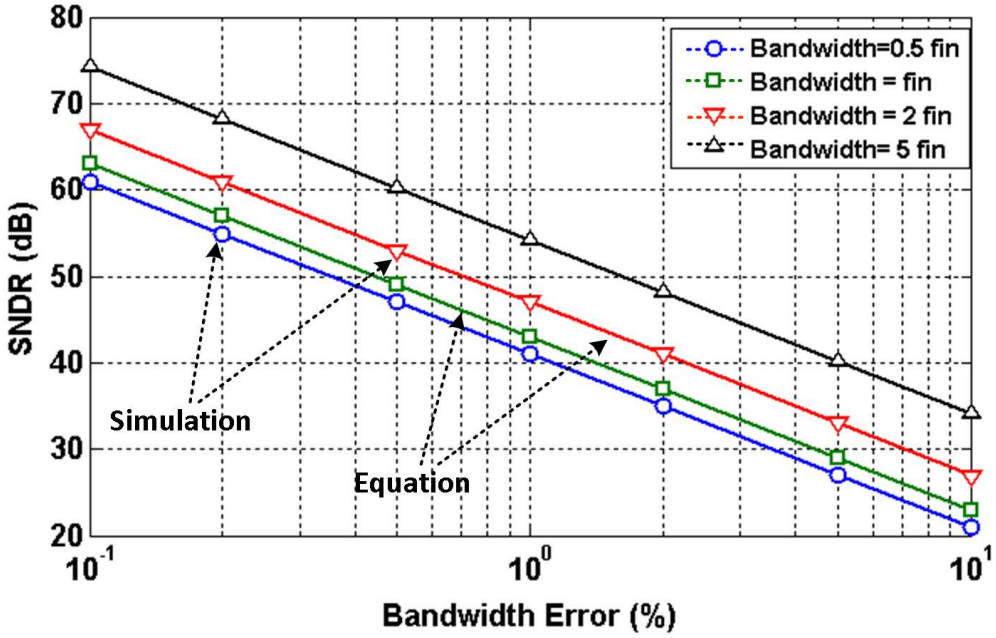


Figure 2.6: Effect of bandwidth mismatch on SNDR of signal.

$$SNDR = \frac{A^2}{\Delta A^2 + (\omega A \Delta t)^2} \tag{2.22}$$

Substituting from 2.18 and 2.19 and simplification finally gives:

$$\begin{aligned} SNDR &= \left(\frac{\omega_B}{\Delta\omega_B}\right)^2 \cdot \frac{1 + (\omega/\omega_B)^2}{(\omega/\omega_B)^2} \\ SNDR_{dB} &= -20 \cdot log\left(\frac{\omega \cdot \Delta\omega_B/\omega_B^2}{\sqrt{1 + (\omega/\omega_B)^2}}\right) \end{aligned} \tag{2.23}$$

As with the previous two errors, the effect of bandwidth mismatch on SNDR is simulated in MATLAB using transient simulations to verify the theoretical equation. Assuming the error condition where the bandwidth toggles between $\omega_B \cdot (1 \pm \Delta\omega_B)$,

the SNDR is plotted against the bandwidth error, and the results are shown in Fig. 2.6 for different bandwidth to input frequency (ω_B/ω) ratios. As this ratio increases, suggesting higher system bandwidth, the effect of bandwidth mismatch errors is reduced, resulting in better SNDR. Results from equation 2.23 are also plotted, showing perfect matching with the simulation results. As the equation suggests, no dependence on the time interleaving factor is observed. Note that this error scenario does not cause worst case condition here, where for the bandwidth error, worst case is expected when the bandwidth mismatch results in the minimum bandwidth for all the channels.

Now, if a Gaussian random distribution of the mismatch error is assumed, the SNDR is expected to depend on the time interleaving factor similar to the gain error case. By modifying equation 2.23 to include the time interleaving factor similar to equation 2.16, the SNDR becomes:

$$\begin{aligned} SNDR &= \frac{M}{M-1} \cdot \left(\frac{\omega_B}{\sigma_{\omega_B}}\right)^2 \cdot \frac{1+(\omega/\omega_B)^2}{(\omega/\omega_B)^2} \\ SNDR_{dB} &= -20 \cdot log\left(\sqrt{\frac{M-1}{M}} \cdot \frac{\omega \cdot \sigma_{\omega_B}/\omega_B^2}{\sqrt{1+(\omega/\omega_B)^2}}\right) \end{aligned} \tag{2.24}$$

Where σ_{ω_B} is the standard deviation of the random mismatch error. Transient simulation are performed with the random mismatch, and the results are plotted in Fig. 2.7, assuming $\omega = \omega_B$. The results show very good matching between the simulations and equation 2.24. Similar to the gain error case, as the number of interleaving channels increases, the SNDR becomes less dependent on the interleaving factor, and approaches that of equation 2.23. In general, the bandwidth mismatch depends on the input frequency, but is independent on the input amplitude. Similar to the gain mismatch case, bandwidth mismatch results in tones at $(i/M)f_s \pm fin$,

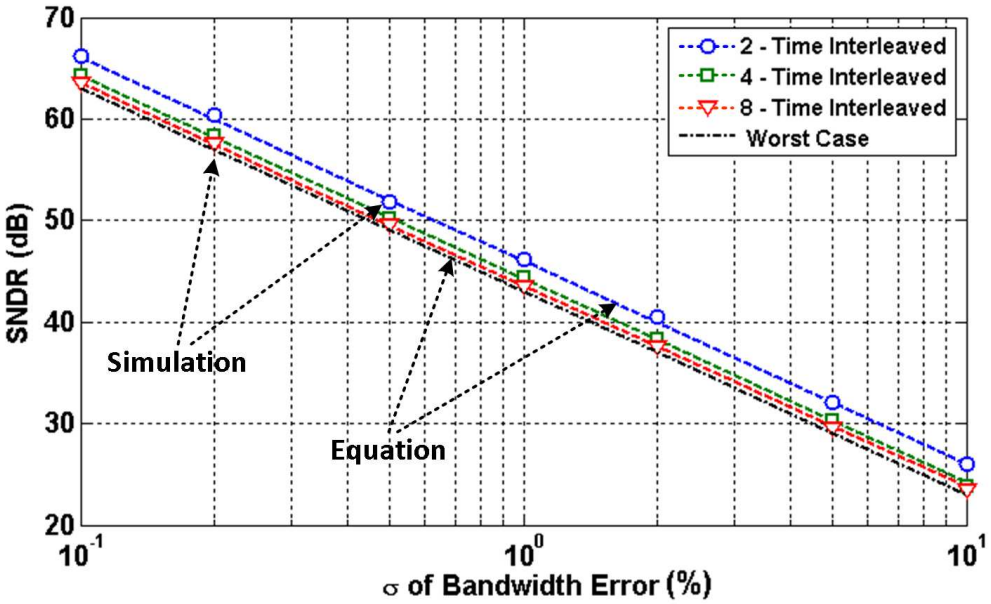


Figure 2.7: Effect of statistical bandwidth mismatch on SNDR of signal.

where $i = 0, 1, 2, ...M/2$.

2.2.4 Timing Mismatch Error

The effect of timing mismatch is very similar to that of sampling jitter, where the sampling instants are modulated by the skew errors. Unlike the error due to jitter, the timing mismatch error is deterministic. Assuming a worst case scenario, where the timing skew of each channel toggles between $\pm\Delta\tau$, this is equivalent to full rate sampling with a clock that has a period toggling between $T - \Delta\tau$ and $T + \Delta\tau$. Following a similar approach to the one used for equation 2.3, the SNDR can be written as:

$$\begin{aligned} SNDR &= \frac{A^2/2}{A^2\omega_{in}^2\Delta\tau^2/2} = \frac{1}{\Delta\tau^2\omega_{in}^2} \\ SNDR_{dB} &= -20 \cdot log(\Delta\tau\omega_{in}) \end{aligned} \tag{2.25}$$

Comparing this result to that of equation 2.4 for the case of random jitter, the two equations are very similar to each other.

The effect of timing mismatch may also be treated statistically. It can be proven [34] that the SNDR with random timing mismatch effect may be written as:

$$SNDR \approx \frac{M}{M-1} \cdot \frac{1}{R_x''(0) \cdot \sigma_\tau^2} \tag{2.26}$$

Where $R_x(.)$ is the autocorrelation function of the input and σ_τ is the standard deviation of the timing error. For a sinusoidal input, $R_x''(0) = \omega_{in}^2$, and the SNDR may be written as:

$$\begin{aligned} SNDR &\approx \frac{M}{M-1} \cdot \frac{1}{\omega_{in}^2\sigma_\tau^2} \\ SNDR_{dB} &\approx -10 \cdot log\left(\frac{M-1}{M} \cdot \omega_{in}^2\sigma_\tau^2\right) \end{aligned} \tag{2.27}$$

From equation 2.26, it may be concluded that the timing mismatch error follows similar dependence on interleaving factor to that of gain or bandwidth errors, and as the interleaving factor increases, the expression in equation 2.27 approaches that of equations 2.25.

The MATLAB model is used to validate the results obtained in equation 2.27, and the waveforms are shown in Fig 2.8, showing perfect matching between simulations and theoretical equations. In general, similar to gain and bandwidth errors, the

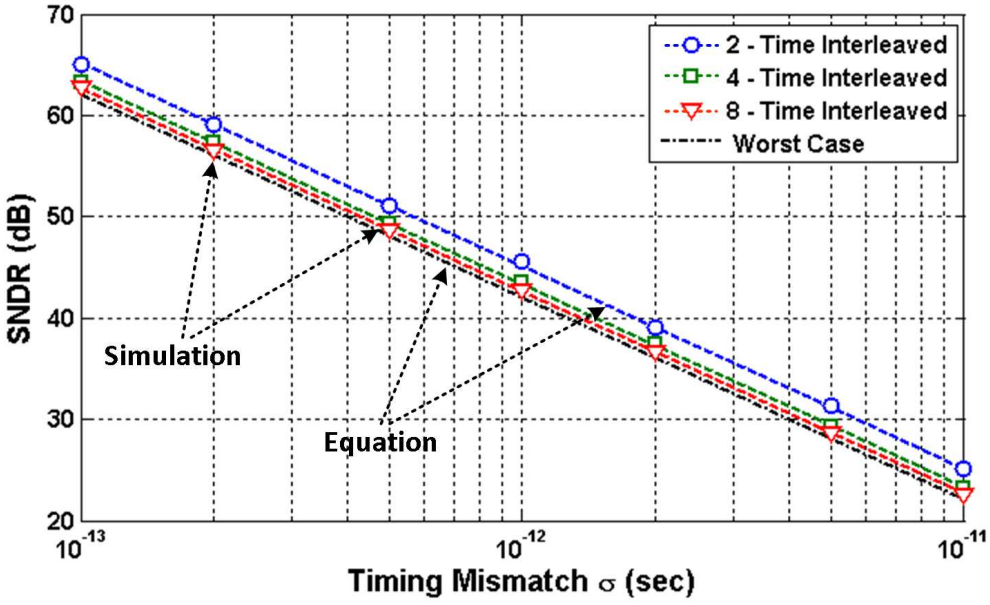


Figure 2.8: Effect of timing skew mismatch on SNDR of signal.

timing mismatch errors depend on the input frequency and is independent on its amplitude. The error results in tones at $(i/M)f_s \pm fin$, where $i = 0, 1, 2, ...M/2$ [28].

2.3 Multi-Phase Generation and Timing Skew Calibration

One of the critical blocks in the design of time interleaving ADCs is the clock generation circuit. An M-channel time interleaved architecture requires M evenly spaced phases each running at f_s/M. Due to process variations and other systematic errors, the clock phases are skewed and require calibration. As discussed in the previous section, unlike offset and gain mismatches which are static errors, meaning that they are independent on the input frequency, the timing skew error is dynamic, making it harder to calibrate. In this section, different architecture for multi-phase clock generation and clock skew detection and correction methods are discussed.

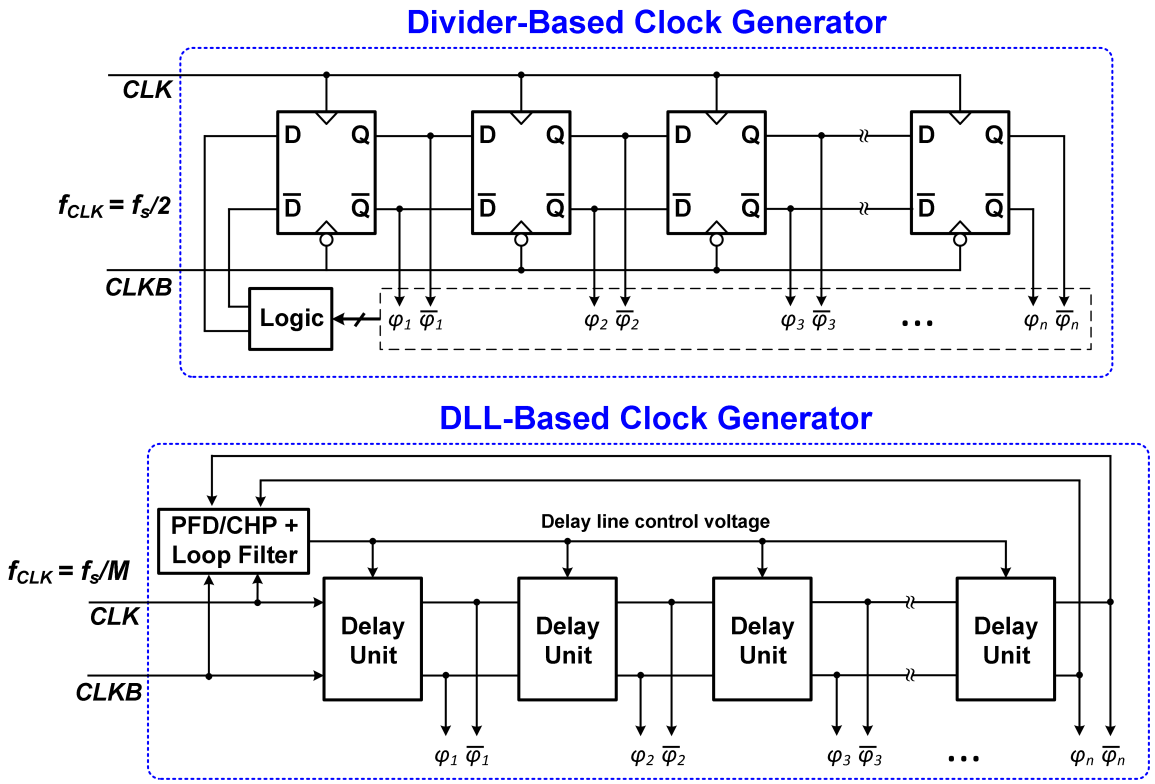


Figure 2.9: Block diagrams of divider-based and DLL-based clock generators

2.3.1 Multi-Phase Clock Generation

Different methods exist for multi-phase generation [35]. Two of the famous methods are DLL-based and divider-based phase generators. Simplified block diagrams of the two architectures are shown in Fig. 2.9. For the divider-based generator, an input clock at full sampling rate f_s is synchronously divided by M to generate the time interleaving phases. For the case of fully differential implementation, like the one shown in the figure, two phase of clock at half the sampling rate $f_s/2$ can be used instead, as long as 50% duty cycle is guaranteed. The DLL-based phase generator, on the other hand, does not require a full rate clock, where the delay of a voltage controlled delay line is locked to generate the required phases. It was proven, however,

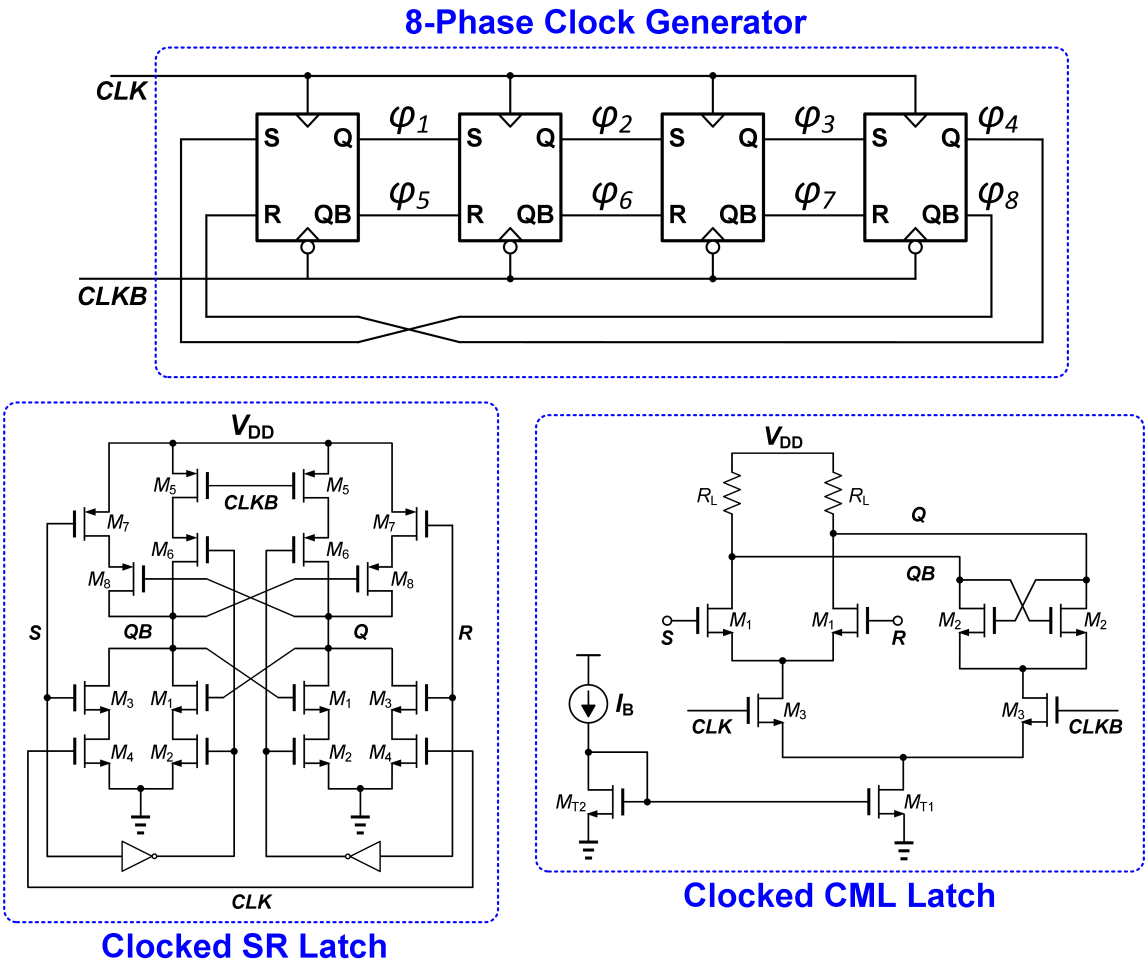


Figure 2.10: An example of divider-based 8-phase clock generator, showing two different realizations of clocked SR latch

that the divider-based architecture out-performs the DLL-based in many cases [36]. One reason is that the DLL architecture suffers from jitter accumulation through the delay line, which is not a problem in the divider-based architecture, since the phase is reset every clock edge. Another advantage of the divider-based generator is that it usually has a wider operating range, since no delay-tuned elements are required which usually have limited delay range.

An example of an 8-phase clock phase generator using the divider-based architec-

ture is shown in Fig. 2.10, using SR latches. Depending on the operating frequency, two different implementations of the SR latch is shown. In the first realization, the SR latch is a modified version of the balanced SR latch presented in [37] is used, where clocking controls are added to the latch. By utilizing the balanced latch architecture, a fully differential implementation of the divider is possible. This clock phase generator is used for two 6 bit 10GS/s time interleaved SAR ADCs [14,20]. In the second realization, a CML architecture is used to enable higher speed operation, where the phase generator is used for a 6 bit 25GS/s binary-search ADC [9].

2.3.2 Clock Skew Detection and Correction

Many techniques exist in the literature for detection and correction of the timing skew error. Those techniques may be divided into three categories [38]: all analog methods [39], in which both the detection and correction are realized in the analog domain, all-digital methods [40] in which the process is fully realized in the digital domain and mixed mode techniques that usually combine digital detection and analog correction. The third method is the most common one, since analog detection of timing skew is susceptible to PVT variations, making it very hard to detect skew errors in the order of sub-picoseconds. All-digital detection performs the skew detection in the digital domain, allowing it to detect skew errors at much higher accuracies. The correction, however, is also implemented in the digital domain, requiring complex fractional filters to interpolate between already sampled data points. The mixed-mode method performs the digital detection, and corrects the phases by adjusting the delay of digitally-controlled variable delay elements, which corrects the clock phases before the input is sampled.

Different methods have been proposed to perform the digital skew detection. Since the skew error results in tones in the output spectrum, one method is to use the

output spectrum with a known sinusoidal input to extract the timing information [41, 42]. A main drawback of this method is that it can only be performed as a foreground calibration, since a well-defined sinusoidal input signal is required. Another drawback is that the implementation of the FFT to extract the spectrum of the output is not straight forward. A simpler detection method is to use code density test (CDT) to measure the phase spacing between every two adjacent phases [43]. Here, an asynchronous input signal is applied, and a histogram counter is used to count the input signal edge transitions between every two adjacent sampling clocks [44]. Since the input is asynchronous with respect to the sampling clocks, the number of counted transitions is proportional to the spacing between the two phases. Although this implementation is simpler, it still needs an asynchronous input, making it suitable for foreground calibration only.

To enable background calibration, a correlation-based detection method was proposed in [45], where an extra reference sub-ADC channel is used, and the cross-correlation between the output of every interleaved channel and the reference channel is maximized through a calibration loop, which is equivalent to the two sampling phases being aligned. Another method, also based on correlation, was later proposed, which requires no extra reference channel [46]. Instead of calculating the cross-correlation with a reference signal, the auto-correlation functions of the input at two consequent sampling instants are calculated. The difference between those two auto-correlation functions is finally used to extract the skew information [46].

2.4 Equalization in High Speed Links Applications

The bandwidth of electrical interconnects is generally limited by high frequency loss of electrical traces, reflections due to impedance mismatches and cross-talk of adjacent signal traces [47], as shown in Fig. 2.11, for an example of a backplane

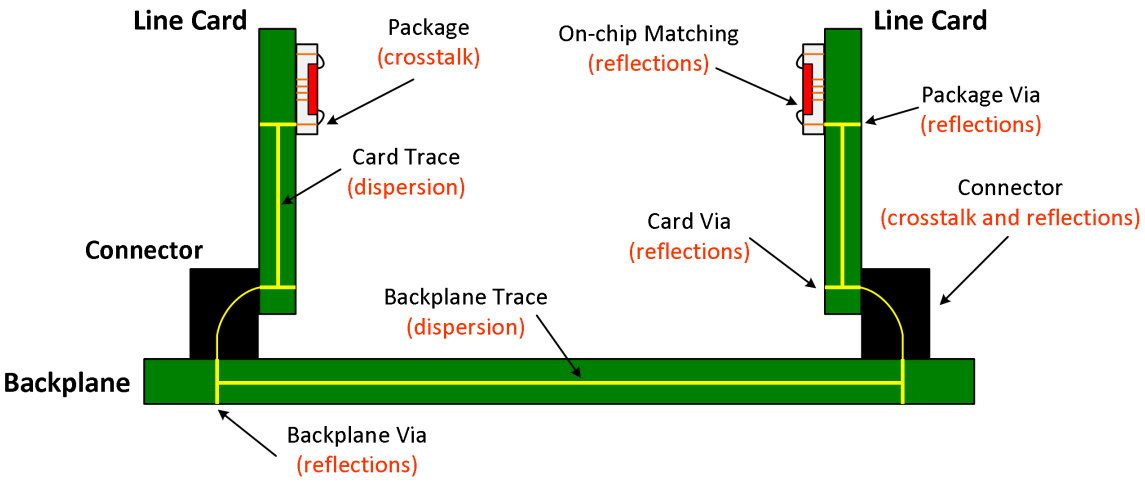


Figure 2.11: Cross-section of backplane system.

channel system. Skin effect and dielectric losses of the PCB traces cause frequency dependent attenuation or dispersion, resulting in signal attenuation at high frequencies. The skin effect describes the current crowding near the conductor surface, which results in a resistive loss proportional to the square root of the frequency [48]. The loss factor due to the skin effect may be written as [49]:

$$\alpha_R = \frac{\sqrt{\pi\mu\rho}}{4Z_0 w}\sqrt{f} \tag{2.28}$$

Where μ is the magnetic permeability, ρ is the conductor resistivity and w is the width of the wire, assuming rectangular strip wire.

Dielectric loss describes the loss due to dissipation of energy in the dielectric material, mathematically expresses as an imaginary part to the dielectric permittivity. This results in a loss term proportional to the frequency of the signal [49]. The loss factor may be given as:

$$\alpha_D = \frac{\pi\sqrt{\epsilon_r}tan\delta_D}{c} f \tag{2.29}$$

Where ϵ_r is the relative dielectric permittivity, c is the speed of light and $tan\delta_D$ is the loss tangent of the dielectric material.

Impedance discontinuities due to PCB trace vias or other non-ideal matching conditions result in signal reflections. If the source termination is not perfectly matched, the reflection may bounce back and fourth between the source and the discontinuity giving rise to multiple reflections, which appear at the receiver end as attenuated replicas of the transmitted signal, causing interference errors. Capacitive and inductive coupling of adjacent traces generate cross-talk errors, which may be caused by near-end (NEXT) aggressors or far-end (FEXT) aggressors [50], also giving rise to interference errors. In practice, cross-talk can be a major limit to high speed link scaling [47], where the cross-talk energy may exceed the through channel signal energy, requiring the use of cross-talk cancellation techniques [51].

Fig. 2.12(a) shows the frequency dependence of channel loss for three different backplane channels, two with smooth responses and one with a frequency notch. The 10GS/s pulse responses of the channels are also shown. It may be concluded from the figure that the channel with the longer trace has higher attenuation, which translates into a wider or "more dispersed" shape of the pulse response. In addition, the channel with the frequency null, which usually appears due to signal reflections, has worse pulse response. Instead of a single pulse, the dispersed pulse response has pre-cursor and post-cursor components in addition to its main cursor. Those components interfere with the previous and following data symbols, causing the so called inter-symbol interference (ISI). This is demonstrated in Fig 2.12(b) , where the pattern "101" is transmitted through the 20-inch smooth channel, and the output is shown in the figure. The ISI error may cause the middle 0 symbol to be mis-interpreted as a 1 symbol, resulting in a potential bit error.

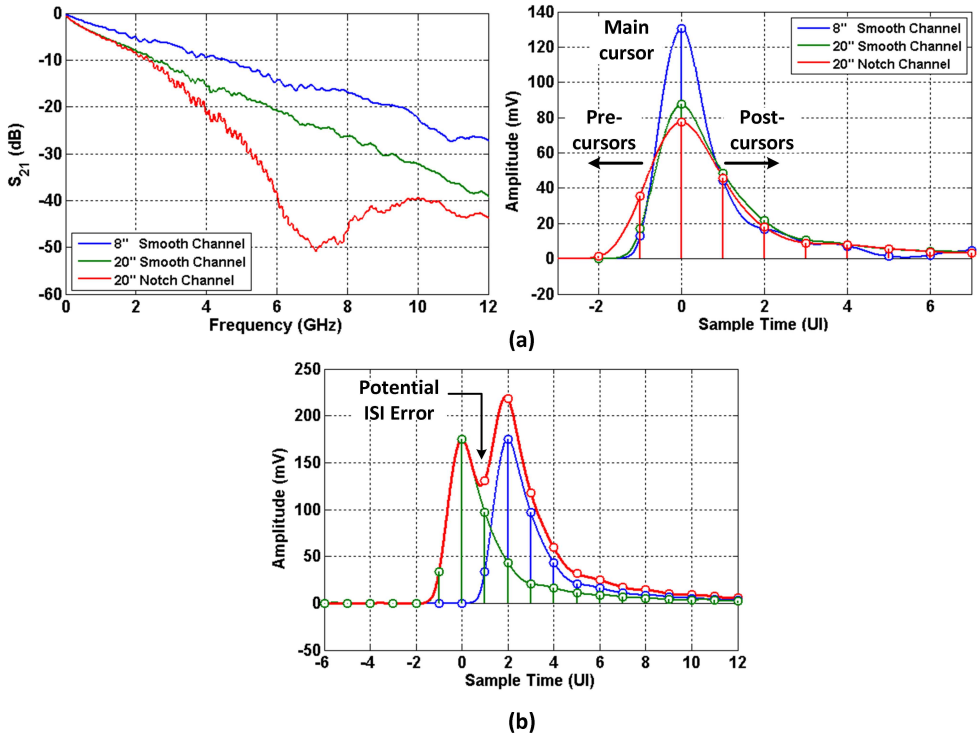


Figure 2.12: (a) Channel and pulse responses for three backplance channels, and (b) Error due to inter-symbol interference (ISI) effect

2.4.1 Equalization Techniques

In order to extend the bandwidth of electrical channels to enable high speed operation, signal equalization is usually employed to cancel the effect of ISI. Equalizers can be implemented as linear or non-linear filters, can have continuous time or discrete time implementations and may be placed at the transmitter side or at the receiver side. In the following discussion, Two main types of equalizers, the feed-forward equalizer (FFE) and decision feedback equalizer (DFE) are considered. Another type of linear equalizer, the continuous-time linear equalizer (CTLE), is also common at the receiver side, where an active or passive filter implements a high-pass function to equalize the signal. The equalization achieved by CTLE is usually limited

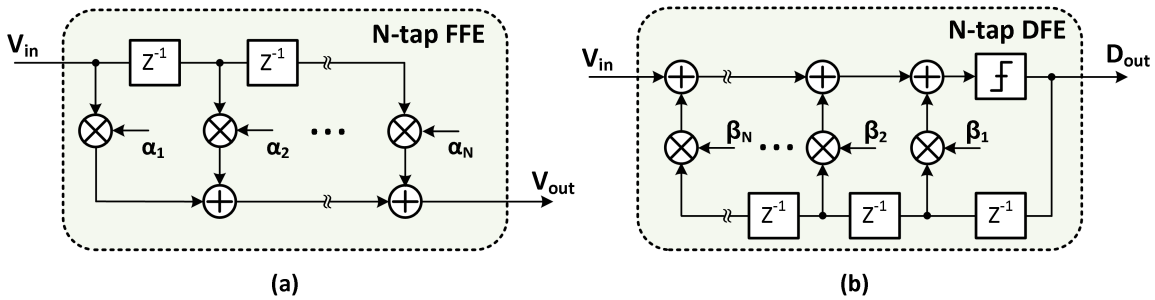


Figure 2.13: Block diagram of (a) N-tap FFE and (b) N-tap DFE equalization.

to first order compensation. In addition, the operating speed is limited by the gain-bandwidth product of the amplifier, which may result in increased power dissipation to achieve high speed operation. As a continuous time system, the CTLE may also be very sensitive to process, voltage and temperature (PVT) variations, requiring some form of tuning for proper operation [52].

2.4.1.1 Feed-Forward Equalization (FFE)

In the feed-forward type of equalization, time delayed and scaled versions of the signal are used to implement a finite impulse response (FIR) filter to equalize the channel, as shown in Fig. 2.13(a). The FFE may be implemented at the transmitter side, usually called TX-FIR, which provides pre-emphasis to the signal before the channel. One limitation of the TX-FIR is the peak power constraint of the transmitter swing [53], which means that in order to achieve high frequency boosting, the low frequency components of the signal are attenuated. Another disadvantage is that the equalization occurs before the channel, which means that adaptive equalization can not be used to optimize for the TX-FIR taps, unless a back-channel is provided which is not generally available.

At the receiver side, the FFE equalization can either use an analog or a digital implementation. With an analog FFE implementation, the received analog signal is

delayed using delay cells and scaled by the equalizer coefficient. This architecture is usually used to implement fractionally spaced filters [54, 55]. With enough dynamic range, this filter may boost the high frequency content of the signal rather than attenuate the low frequency components. The filter taps may also be adaptively tuned without the need of a back-channel, since the signal equalization is implemented after the channel. The realization of the analog delay cells and tap coefficients may be an issue, since they would be susceptible to PVT variations. A digital FFE implementation, on the other hand, provides robustness to PVT variations, but requires an analog-to-digital converter (ADC) at the receiver front-end.

In general, due to its linear implementation, the FFE equalizer suffers from the issue of noise amplification, where the noise and cross-talk is amplified along with the signal. Even in the case of digital FFE implementation, the FFE equalizer will amplify the quantization noise added to the signal due to the ADC quantization.

2.4.1.2 Decision Feedback Equalization (DFE)

Unlike FFE, the DFE is a nonlinear equalizer which works to directly subtract the post-cursor ISI components of the signal, as shown in Fig. 2.13 (b). The DFE therefore does not suffer from the noise amplification problem, since symbol decisions are made before subtraction of the ISI. The DFE, however, suffers from critical feedback timing limitations, where the feedback loop elements need to be fast enough to close the loop timing before the next symbol arrives. Speculation may be used to relax the timing constraints, where the DFE taps are loop-unrolled to implement all possible coefficient cases, and the proper case is selected based on the previous symbols through a multiplexer [56]. The complexity of the system grows exponentially with the number of unrolled taps, limiting the number of DFE taps that may be speculated.

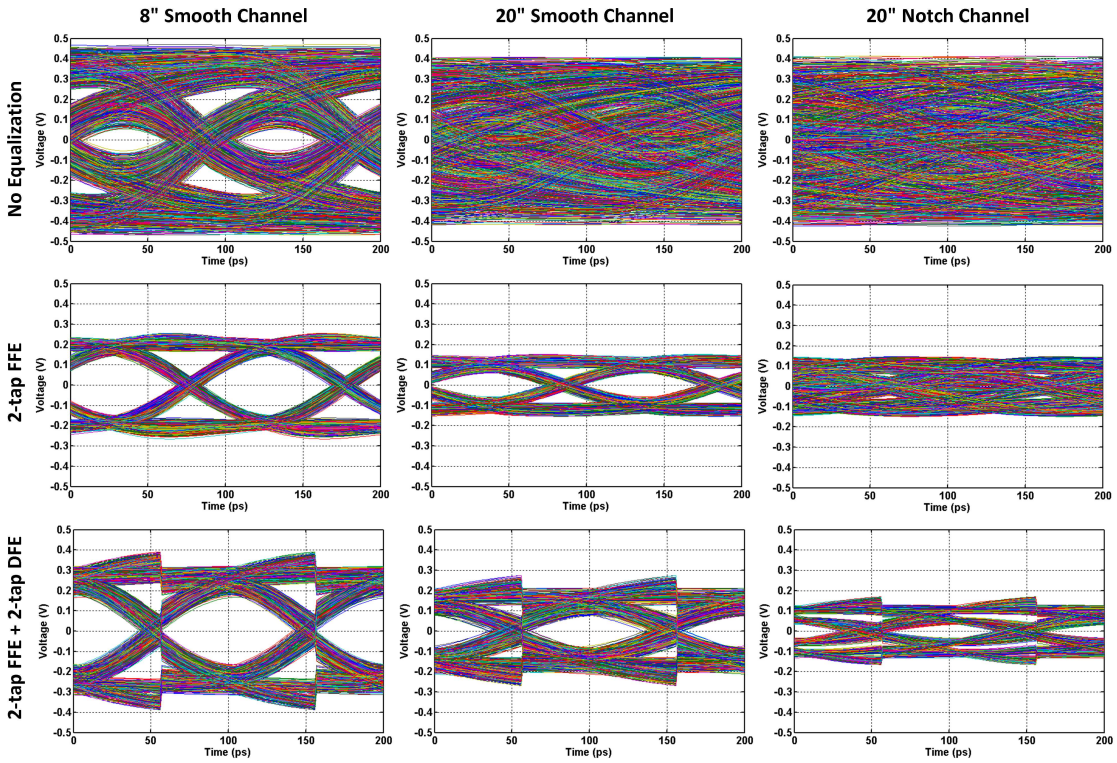


Figure 2.14: Eye diagram for the three backplance channels of fig 2.12 (a) under different equalization condition.

To demonstrate the effect of equalization on the received signal, the three channels of Fig. 2.12 are simulated with random data input, and the output eye-diagrams are shown in Fig. 2.14 for different equalization scenarios. First, with no equalization, only the lowest-loss 8-inch channel shows an open eye, while the eye is closed for the other two 20-inch channels. Adding 2 taps of FFE equalization, the voltage margin for the first channel improves significantly, and an open eye may be obtained for the smooth 20-inch channel. However, for the 20-inch notch channel, the eye is still closed. Combining 2 taps of FFE with 2 taps of DFE finally results in an eye opening for the highest loss channel, while further improving the eye opening for the other two channels.

3. STATISTICAL MODELING OF ADC-BASED RECEIVERS*

As data rates for serial I/O links increase, operation over standard legacy channels becomes more challenging due to excessive frequency-dependent channel attenuation, which causes large amounts of inter-symbol interference (ISI). In order to operate reliably over such channels at high data rates, equalizer circuits in the form of continuous time linear (CTLE), feed-forward (FFE) or decision-feedback (DFE) equalizers are usually employed [6]. While analog equalization can allow for increased system data rate, there has been on-going interest in ADC-based high-speed links (Fig. 3.1), where CMOS technology scaling allows for the efficient implementation of powerful on-chip digital signal processing (DSP) algorithms for equalization and symbol detection [2, 57]. This digital equalization offers robustness to PVT variations and is easier to re-configure than mixed-signal equalization circuitry. Moreover, ADC-based receivers also enable more spectrally-efficient modulation schemes such as duo-binary and PAM4, and more complicated equalization strategies such as sequence estimation.

Despite these advantages, ADC-based receivers are generally more complex and consume higher power than binary receivers [58]. Even with state of the art multi-GS/s ADC implementations, power is often prohibitive for many systems where link power efficiency is the key metric. The digital equalization that follows the ADC can also consume significant power, comparable to the power of the ADC [2]. To enable

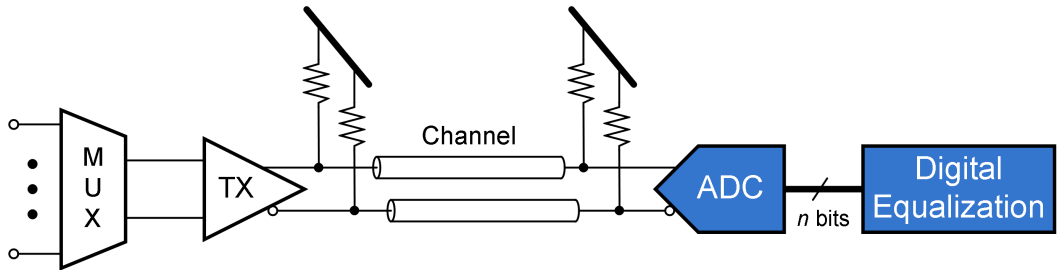


Figure 3.1: Block diagram of a high speed link with ADC-based receiver.

ADC-based receivers for these systems, a fast and reliable analysis tool is required to rapidly investigate trade-offs in system complexity and performance, in order to arrive at optimal ADC resolution and digital equalizer complexity requirements. The tool may also be useful in studying the effectiveness of system and circuit techniques used to save power in ADC-based receivers such as partial analog pre-equalization [14].

The growing complexity of high speed links systems made it impractical to use time domain Monte Carlo (transient) simulations alone to predict the system performance, where the number of bits required to validate typical bit error rate (BER) requirements ($< 10^{-12}$) becomes prohibitive. On the other hand, worst case analysis methodologies such as peak distortion analysis are often pessimistic and result in over design. For these reasons, most of today's high speed link simulation tools use statistical models to predict performance metrics such as BER without the need for lengthy bit-by-bit simulations [18, 19].

While these statistical tools are growing mature for binary links, conventional modeling approaches for ADC-based receivers and digital equalization use ADC performance metrics based on mean-square error (MSE), such as signal-to-noise and distortion ratio (SNDR) or effective number of bits (ENOB) [59, 60]. Currently, high-speed link analysis tools are unable to model ADC-related non-idealities such

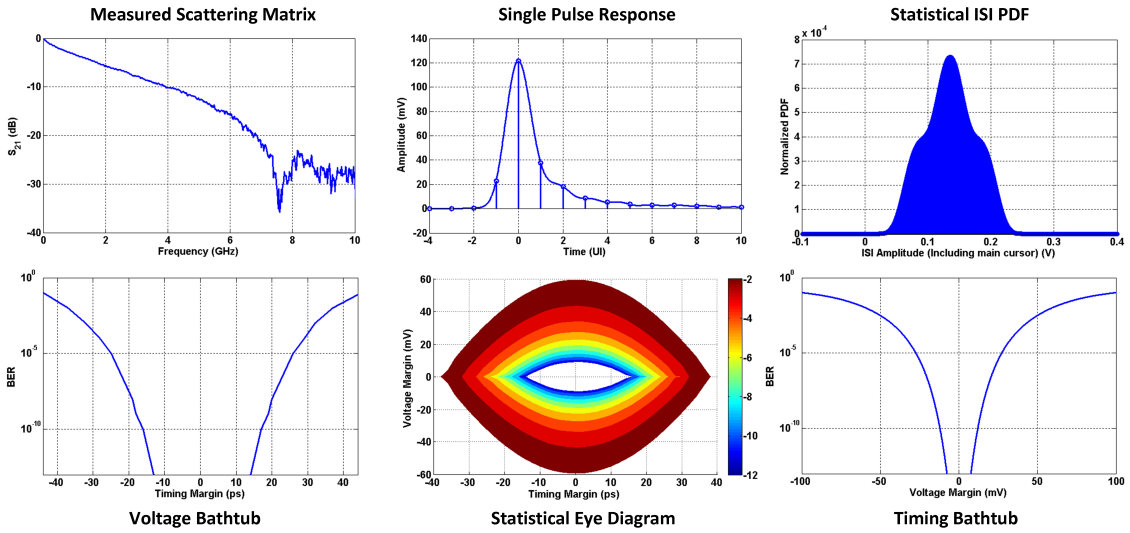


Figure 3.2: Statistical simulation framework.

as the effect of quantization noise, non-linearities and time interleaving mismatches in an efficient way, which can lead to over design of ADC and digital equalization. Provided these challenges are addressed, there exists an opportunity for ADC-based high-speed links to efficiently meet the I/O bandwidth demands of future computing systems.

In this section, a modeling framework for efficient design of high performance ADC-based serial link receivers is introduced. Section 3.1 discusses the statistical simulation assumptions used to model and analyze the ADC-based receiver performance. In section 3.2, Modeling of ADC-related errors such as quantization noise, integral and differential non-linearities (INL/DNL), and other time interleaving-related errors are then presented. Based on this model, performance analysis of ADC based links is investigated in section 3.3, disclosing ADC and digital equalization trade-offs, and providing proof for the potential advantages of partial embedding of analog equalization inside the ADC. Measurement results of a 10GS/s ADC prototype with both embedded and digital equalization are used to validate our statistical modeling

approach in section 3.4, and section 3.5 concludes the section.

3.1 Statistical BER Modeling

First, consider a statistical framework similar to state of the art statistical simulation engines. Assuming no jitter, the signal at channel output can be given as:

$$y(t) = \sum_{k} b_k p(t - kT) \tag{3.1}$$

where b_k is the transmitter output symbol, k is symbol index and $P(t)$ is the channel single pulse response, which can be extracted from the channel measured scattering matrix. After sampling, t is replaced with nT,and the sampled channel output $y[n]$ can be written as:

$$y[n] = \sum_{k} b_k p[n - k] \tag{3.2}$$

The first step in the statistical analysis is to find the probability density function (PDF) of the channel inter-symbol interference (ISI). In order to calculate this, the individual channel ISI components are convolved together, given by:

$$pdf_{ISI,m}(v) = \frac{1}{2}(\delta(v - p[m]) + \delta(v + p[m])) \tag{3.3}$$

$$\begin{aligned} pdf_{ISI} = pdf_{ISI,-i} \otimes pdf_{ISI,-i+1} \otimes \dots \\ pdf_{ISI,j-1} \otimes pdf_{ISI,j} \end{aligned} \tag{3.4}$$

where $\delta(.)$ is the delta Dirac impulse function, $m \in [-i, j]$ and $m \neq 0$. Here, we assume the channel has i pre-cursor and j post-cursor ISI taps. The resulting PDF contains the probability of ISI voltage error added by the channel. An example of

a statistical ISI PDF is shown in Fig. 3.2. Once this PDF is obtained, additional voltage noise components such as random Gaussian noise and uniform power supply noise can be included into the system by convolving the noise PDF with the ISI PDF. The final step is to shift the total PDF to the main cursor position, at $\pm p[0]$, and by performing integration, a cumulative density function (CDF) results, which representing the BER versus the voltage margin, or the voltage bathtub curve, at the channel output.

In order to find the timing bathtub curve, which represents the BER versus the timing margin of the system, the sampling instant of the pulse response is modified by a small timing perturbation, resulting in a family of pulse responses with different ISI components:

$$y(t) = \sum_k b_k p(t - kT - \epsilon) \tag{3.5}$$

where $\epsilon \in [-T/2, T/2]$ is the small perturbation. Those pulse responses are used to generate a family of ISI PDFs corresponding to the time shifts caused by the perturbation. Given these ISI PDFs, the voltage bathtub curve at each time shift can be calculated. Combining these curves and plotting them versus time shift, a timing bathtub curve, as well as a statistical eye diagram, can be constructed as show in Fig. 3.2.

In the presence of receiver jitter, the eye opening is expected to become worse, since the sampling instant is modulated by the jitter, resulting in sampling the pulse at sub-optimal positions. To include the effect of receiver jitter in the model, the pulse response is modified to:

$$y(t) = \sum_k b_k p(t - kT - \epsilon_k^{RX}) \tag{3.6}$$

where ϵ^{RX} is the receiver jitter. Comparing equations 3.5 and 3.6, it is clear that the effect of the receiver jitter is to shift the pulse sampling point. Unlike equation 3.5 which introduces a fixed shift in sampling instant, the shift due to jitter will be function of k, since receiver jitter is a random process. Now, to include the effect of receiver jitter, the ISI PDF's at each sampling instants may be considered a conditional PDF at this instant, and the ISI PDF including the jitter effect is the sum of all conditional PDF's weighted by the value of the jitter PDF at the corresponding sampling instant:

$$pdf_{ISI,\epsilon^{RX}} = \sum_{\tau} f_{\epsilon^{RX}}(\tau) pdf_{ISI,\tau} \tag{3.7}$$

where $f_{\epsilon^{RX}}(\tau)$ is the PDF of the receiver jitter. A family of ISI PDF's including the jitter effect can also be constructed at different sampling instants, by shifting the jitter PDF in equation 3.7 by a small $\epsilon \in [-T/2, T/2]$, and voltage and timing margin plots similar to the ones shown in Fig. 3.2 may be obtained.

The forgoing statistical simulation procedure is very similar to the ones implemented in many statistical simulator engines such as SimLab and LinkLab [61], used to model binary receivers. In order to extend the capability of these statistical simulators for ADC-based links, it is essential to capture the effect ADC-related errors on the system performance. An ADC consists of a sampling stage, followed by a quantization stage. While the sampling in the ADC-based links is usually similar to that in the binary links, quantization on the other hand is a non-linear effect that needs to be properly modeled. The error that results from the quantization process, referred to as quantization noise, will pass through the digital equalizer that follows the ADC, usually in the form of a digital FFE+DFE, where the FFE is expected to amplify this noise. Simplified analysis sometimes approximates the ADC quantiza-

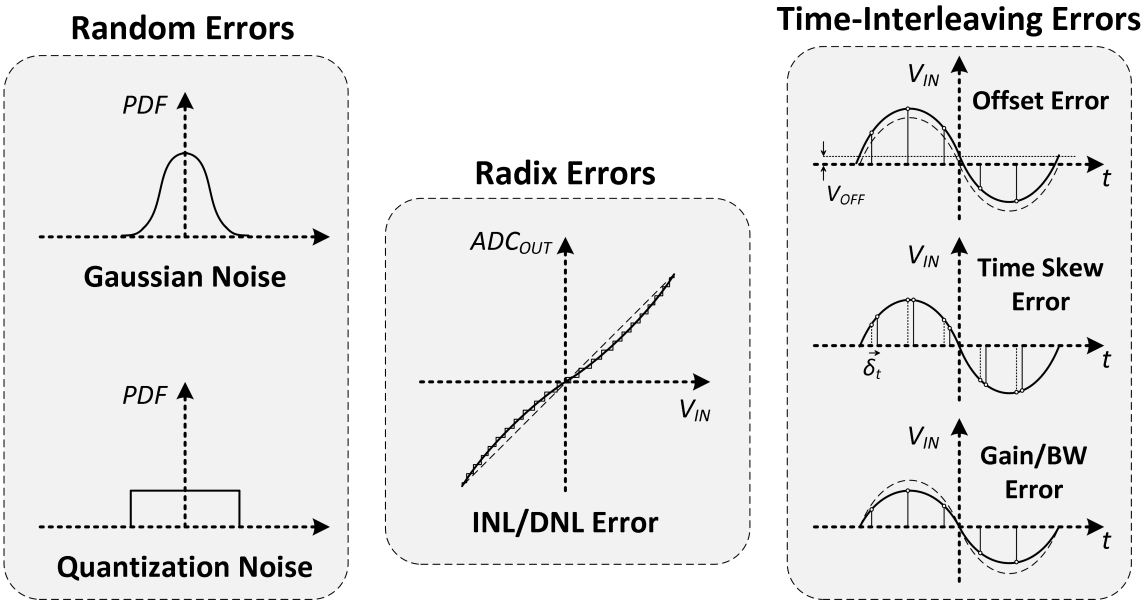


Figure 3.3: Types of ADC-related errors.

tion distortion to a Gaussian normal distribution [59,60], and the total error variance is assumed to be the sum of the random thermal noise and quantization distortion variances. While this may be valid when random noise dominates over quantization distortion [59], this is not the case for ISI-limited systems with low-resolution ADCs, typically 4-6 bits, usually used in high-speed link systems. In the following section, ADC-related errors are analyzed and statistically modeled, and transient simulations are used to verify the accuracy of each model.

3.2 Modeling of ADC-Related Errors

In this section, errors due to the presence of the ADC in the receiver front-end are considered. These errors can generally be classified into three categories, as shown in Fig. 3.3: Random errors, radix errors and time-interleaving errors. Each of those errors is analyzed in the following subsections.

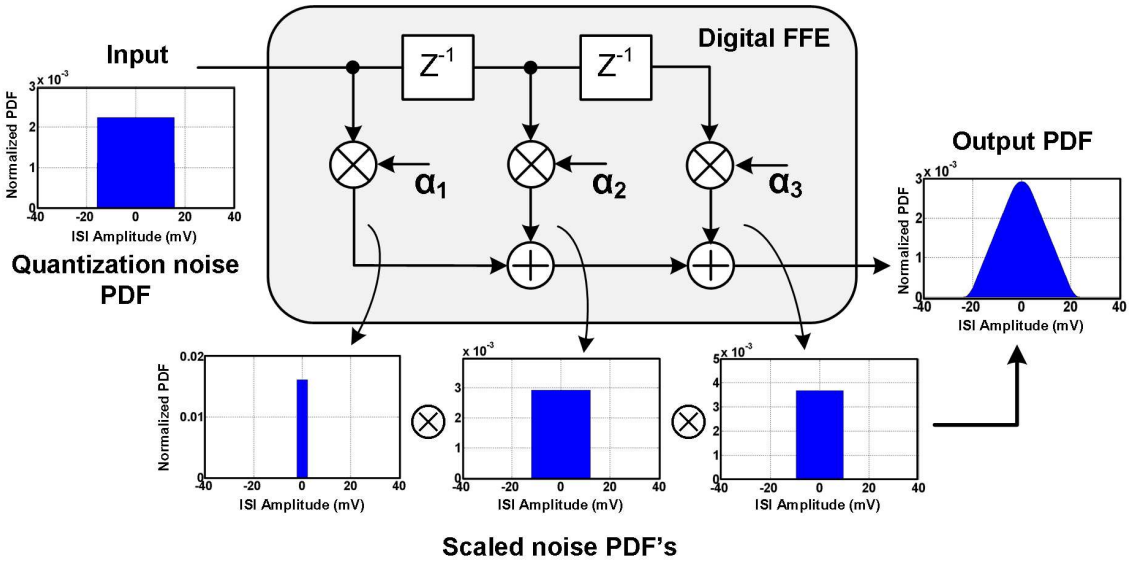


Figure 3.4: Modeling of quantization noise amplification through digital FFE.

3.2.1 Random Errors

Random errors are errors that are uncorrelated with the input signal. They include random and quantization noises. While random noise is stochastic in-nature, and thus can easily be incorporated into the statistical model, quantization noise may in fact depend on the input signal, since it is the result of passing the input through the quantizer. Under certain conditions, however, the quantization noise may be considered as an independent random variable. It was proven by Widrow [25] that the quantization process is mathematically equivalent to convolution of the input PDF with a uniform PDF, and thus under certain conditions, referred to as the quantization theorems, the quantization distortion may be modeled as uniformly distributed random noise component. In ADC-based high speed link receivers, the quantized input signal is usually equalized through digital FFE, which results in amplification of this quantization noise. To include this effect, the quantization PDF is scaled by the FFE coefficients and resulting PDFs are convolved together to arrive

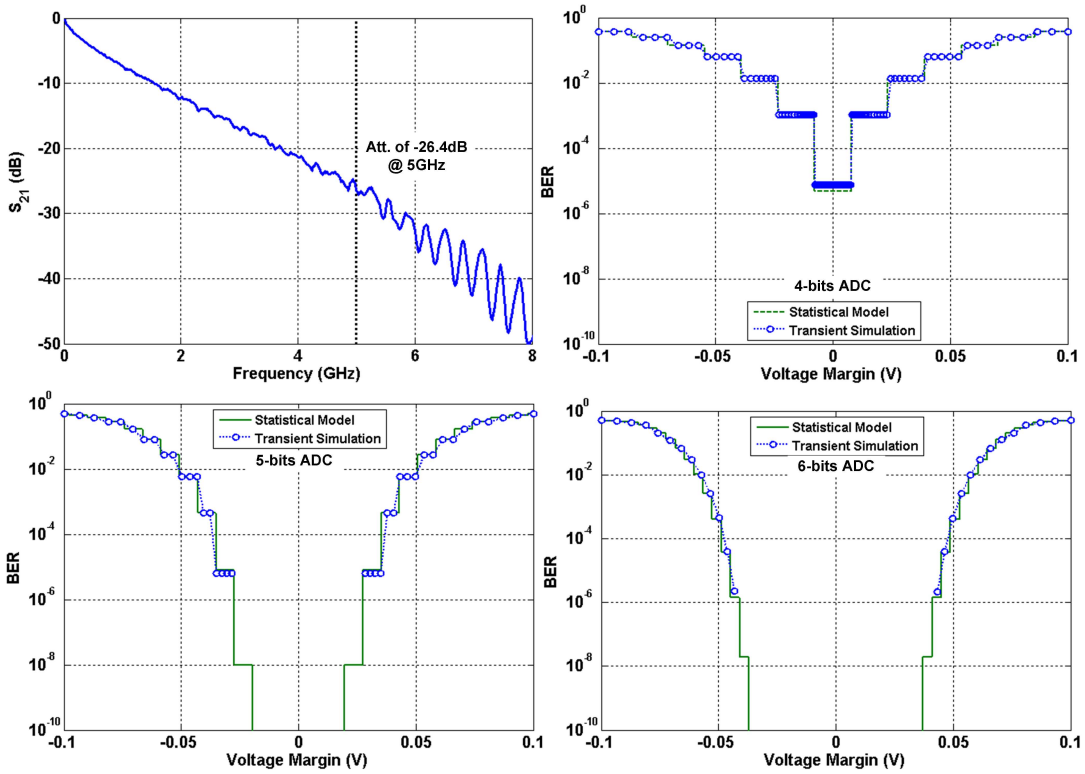


Figure 3.5: Comparison between the quantization noise model and transient simulations.

at the final quantization noise PDF, as shown in Fig. 3.4. While FFE results in noise amplification, DFE, which mitigates residual ISI by eliminating corresponding post cursor ISI taps, does not affect quantization distortion.

In order to verify the quantization noise model, transient simulations are performed and the results are compared to the statistical simulations. The results are shown in Fig. 3.5 for the case of five taps of digital FFE equalization and different ADC resolutions, assuming 10GS/s operation over a backplance channel with 26.4dB of loss at Nyquest frequency, as shown in the figure. The resolution of the digital equalizer coefficients is assumed to be 2 bits more than the ADC resolution, and its assumed that the adders and multipliers of the digital equalizer have enough

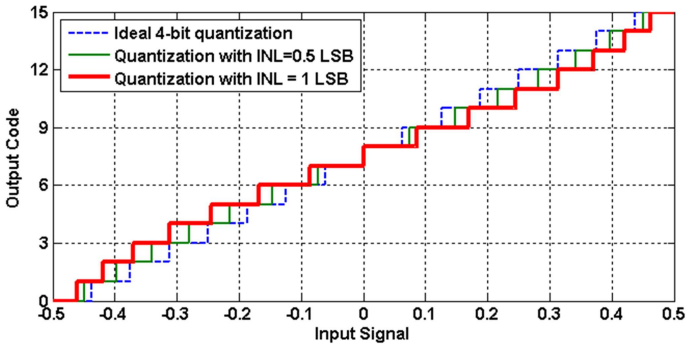


Figure 3.6: ADC quantizer characteristics with sinusoidal INL (note the missing code when INL=1LSB)

resolution to prevent overflow. The quantization noise model shows very good agreement with transient simulations. For the channel under test, at least 5 bits of ADC resolution are necessary to obtain an open eye with BER levels less that 10^{-12}.

3.2.2 Radex Errors

With an ideal quantizer, the input of the ADC is mapped to a number of discrete output levels, where the number of these levels and their positions depends on the type of the quantizer. The most commonly used quantizers are the uniform radix-2 type, in which the input is mapped to one of 2^n equally spaced levels, where n is the ADC number of the bits. In reality, however, quantizers exhibit non-idealities due to process variations and other circuit mismatches, which result in modifying the positions of the quantizer output levels. These non-idealities are usually quantified in the form of differential non-linearity (DNL) and integral non-linearity (INL). A common design strategy is to keep the values of INL below one half of the ADC least significant bit (LSB), which guarantees no missing codes [62].

The effect of INL/DNL on the system performance has been studied in more details in terms of degradation in signal to quantization noise ratio (SQNR) [63–65].

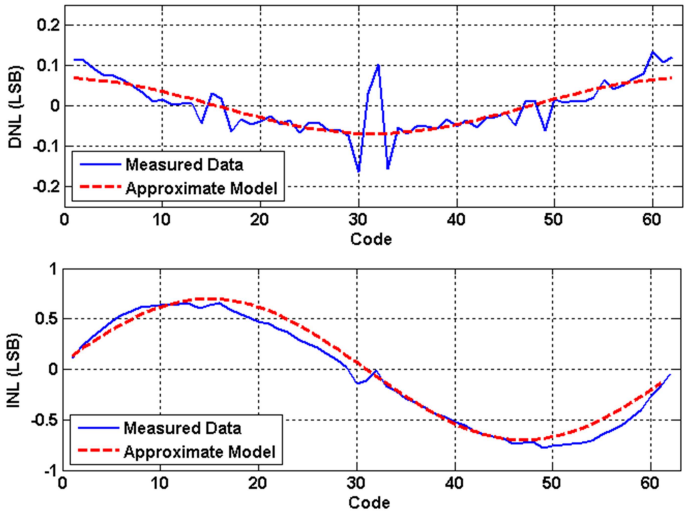


Figure 3.7: Comparison between sinusoidal INL model and measured data.

Assuming the quantizer thresholds are given as:

$$s_i = s_{0i} + u_i \tag{3.8}$$

where s_{0i} is the ideal i_th threshold position and u_i is the error due to INL. It can be proven [64,65] that the effect of INL on the quantization noise power may be approximated as:

$$V_{noise}^2 \cong \frac{\Delta^2}{12} + \Delta \sum_i f_x(s_{0i}) u_i^2 \tag{3.9}$$

where Δ is the LSB of the ADC, $f_x(.)$ is the PDF of the input and it is assumed that the input PDF is almost constant over the interval $[s_{0i}, s_{0i} + u_i]$. A similar result was obtained in [63] which relates the value of the DNL error to the SQNR.

In order to model the effect of INL/DNL, a sinusoidal profile is considered, as shown in Fig. 3.6 for the case of a 4-bit quantizer. The modified quantization thresholds may be written as:

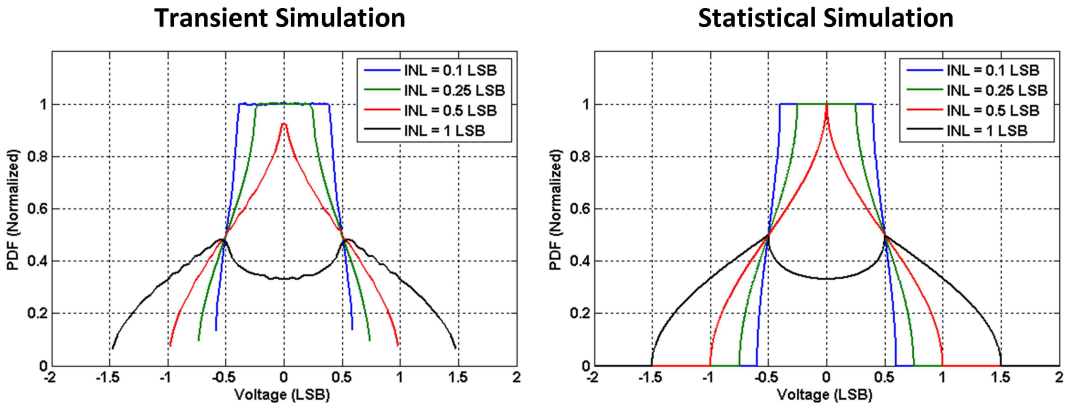


Figure 3.8: Comparison between quantization noise PDF extracted from transient simulations with uniform input and the statistical convolution model.

$$s_i = s_{0i} + \epsilon_{INL} sin(\frac{2\pi}{2^N} i) \tag{3.10}$$

Where ϵ_{INL} is the maximum INL error in LSB, and the index $i \in [0 : 2^N]$ is the threshold level number. This profile assumes a third order non-linearity, which is expected for fully differential implementations. The model is compared to measurement results from 6bit 10GS/s SAR ADC in [14] as shown in Fig. 3.7. The model gives reasonable approximation to real measured INL/DNL profile.

Now, in order to include the effect of INL/DNL inside the statistical model, it is necessary to determine the shape of the quantization noise PDF with INL/DNL. One simple way would be to convolve the ideal uniform quantization noise PDF with the INL PDF, as was suggested in [66]. This calculation, however, does not account for the shape of the input PDF. Transient simulations show that this simple convolution model can actually predict the quantization noise PDF in the presence of INL/DNL correctly, but only when a uniform input PDF is assumed, as shown in Fig. 3.8, where histogram data are extracted from the transient simulations and compared to

the statistical results. If the transient simulations assume any other input PDF e.g. Gaussian, the model fails.

Alternatively, following a procedure similar to [26], the effect of input PDF may be taken into account in the model. The quantization noise PDF may be given by:

$$\begin{aligned} f_q(q) &= \sum_i f_x(y_i - q | X \in s_i) \\ &= \sum_i f_x(y_i - q) w_i \\ w_i &= \begin{cases} 1, & x \in s_i \\ 0, & x \notin s_i \end{cases} \qquad x = y_i - q \end{aligned} \tag{3.11}$$

Where w_i is a window function with width equal to the i_{th} quantization step. Equation 3.11 implies that in order to obtain the quantization noise PDF for any arbitrary quantizer, the input PDF is shifted to the position of each quantization interval, multiplied by the window function w_i and the results are summed up over all the quantization intervals. In order to verify the model, histogram data are extracted from transient simulations with different input PDF shapes, and the results are compared to the PDF calculated using equation 3.11. The results are shown in Fig.3.9, where sinusoidal INL profile is assumed. The model successfully captures the effect of input PDF on the shape of the quantization noise, whether the input PDF is uniform, Gaussian or a real ISI PDF.

The next step is to find the effect of digital FFE equalization on quantization noise. Following a procedure similar to the one explained in Fig. 3.4, where scaled versions of the quantization noise PDF are convolved together to capture the quantization noise amplification through the FFE, the resulting quantization noise PDF

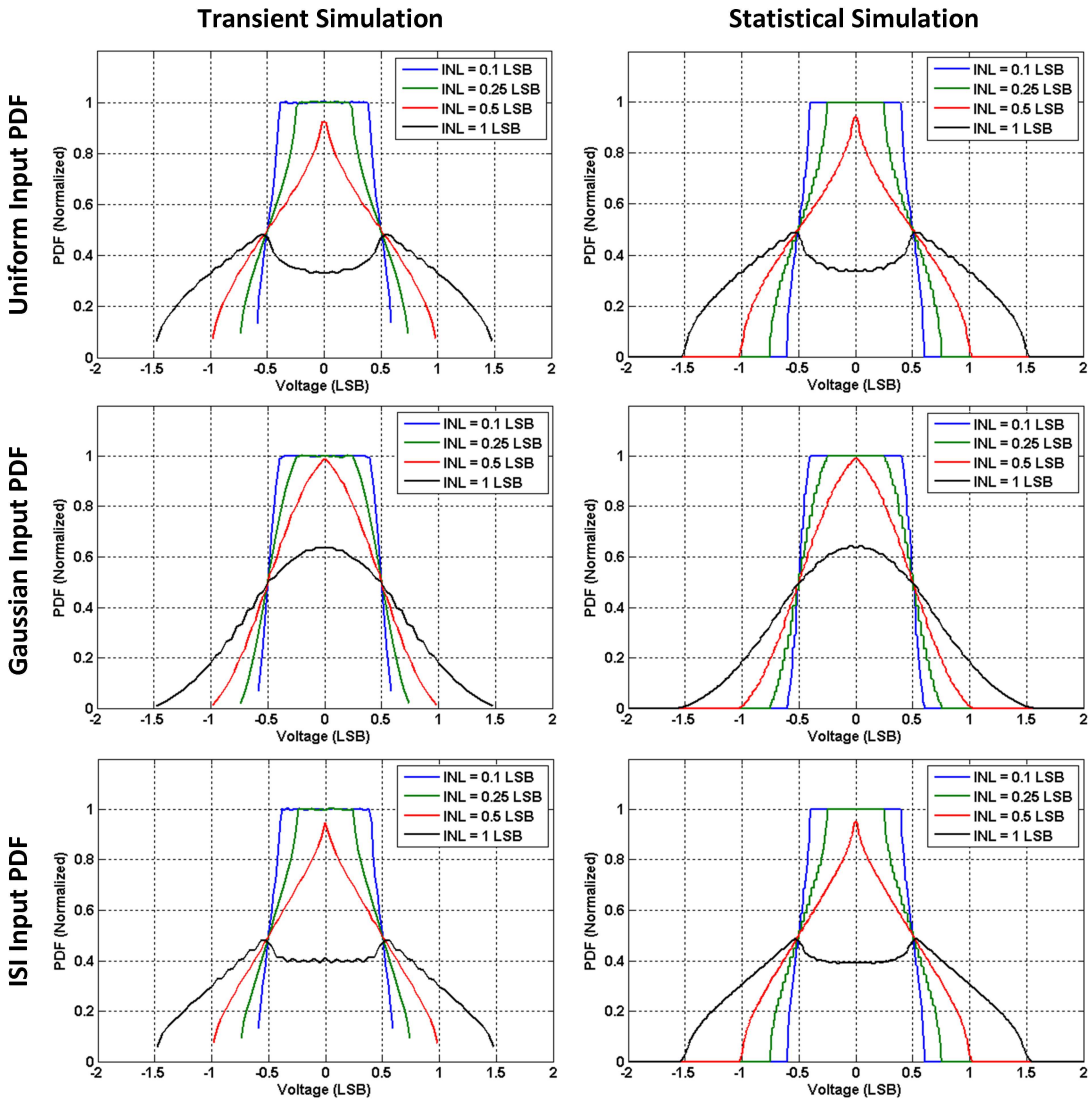


Figure 3.9: Comparison between quantization noise PDF extracted from transient simulations and the statistical models based on equation 3.11 for three different cases of input PDFs.

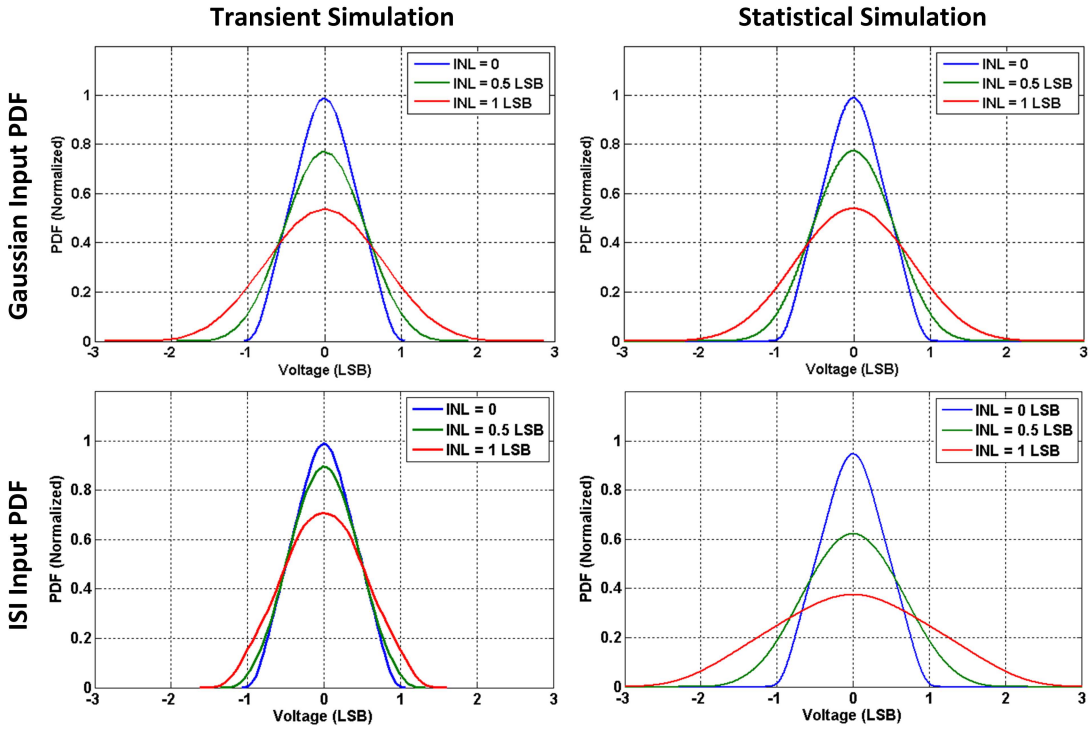


Figure 3.10: Comparison between quantization noise PDF after the digital FFE extracted from transient simulations and the one calculated using the statistical model, for two different cases of input PDF.

is shown in Fig. 3.10 for two cases of input PDF: with Gaussian input and with real channel input. The results are compared to histograms extracted from transient simulations. As can be seen in the figure, when a random Gaussian input PDF is assumed, the quantization noise amplification is captured properly. However, when the actual ISI channel is considered, the model very pessimistic. The reason for this discrepancy is due to the quantizer non-linearity, where the quantization error for the case of the real channel becomes dependent on the input signal, resulting in the error terms becoming correlated when passed through the FFE equalizer. In other words, the signal component of the quantization error gets "equalized" when passed through the FFE equalizer, which is not captured by the statistical model. For the

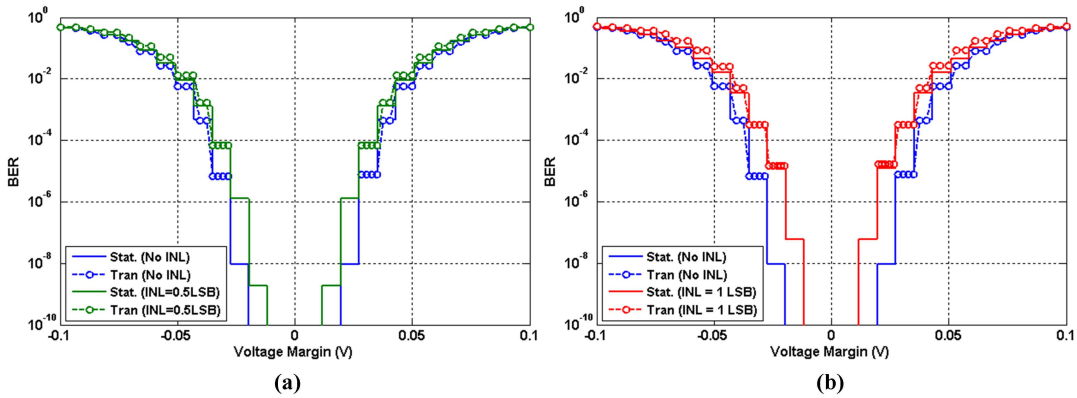


Figure 3.11: Comparison between the quantization noise model using histogram data and transient simulations for (a) INL=0.5 LSB and (b) INL=1 LSB.

case of the Gaussian random input, the error terms are uncorrelated even after they are passed through the FFE equalizer, resulting in a correct convolution model.

Now, since it's not straight forward to analytically find the effect of FFE equalization on the quantization noise with linearity error, the quantization noise PDF after the FFE may be extracted from transient simulations using histogram method, and then used inside the statistical model. Following this procedure, it's possible to correctly predict the BER including INL/DNL effect, as shown in Fig. 3.11, where a sinusoidal INL profile is assumed for a 5 bit ADC, and operation conditions similar to the ones used in Fig. 3.5. The simulations show good matching between the transient and statistical models.

3.2.3 Time-Interleaving Errors

The effect of time interleaving errors on ADC performance has been studied in terms of degradation in SNDR [28–33], as was discussed in section 2. In order to include the time interleaving errors in the statistical model, the procedure shown in Fig 3.12 is followed. For an M-channel time interleaved system, M different pulse

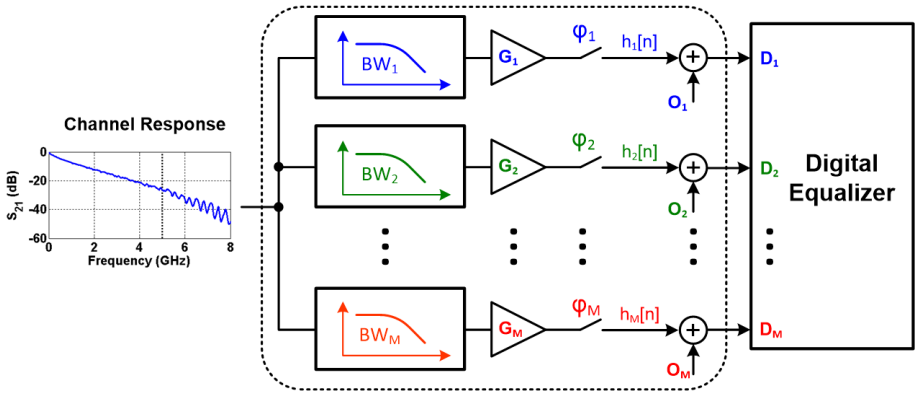


Figure 3.12: Block diagram of time-interleaved system showing the mismatch errors

responses are extracted from the measured channel s-parameter data at the target bit rate, where each response exhibits the gain and bandwidth of its corresponding channel. The pulse responses are then sampled, taking into account the timing skew errors, and the samples from different channels are combined according to the number of digital FFE taps, starting with the main cursor at one channel and interleaving the other ISI cursors between different channels. This is repeated for each time interleaved channel, arriving at a new set of pulse responses, which include the effects of bandwidth, gain and timing skew errors. The new pulse responses are finally equalized through the digital FFE equalizer, and used to generate the ISI PDFs required to calculate the BER.

The mathematical formulation of this procedure may be arranged as follows: Assuming an ideal channel pulse response $h[n]$ with N taps, and a digital FFE equalizer $\alpha[k]$ with K coefficients, $N \geq K$, with no channel mismatches present, the equalized pulse response $g[n]$ may be represented using the convolution equation as:

$$g[n] = \sum_{k=0}^{K-1} \alpha[k]h[n-k] \tag{3.12}$$

Equation 3.12 can be rewritten using a Toeplitz matrix representation [67] as:

$$\begin{bmatrix} g[0] \\ g[1] \\ g[2] \\ \vdots \\ g[N-1] \end{bmatrix}^{\mathrm{T}} = \begin{bmatrix} \alpha[0] \\ \alpha[1] \\ \alpha[2] \\ \vdots \\ \alpha[K-1] \end{bmatrix}^{\mathrm{T}} \begin{bmatrix} h[0] & h[1] & h[2] & \cdots & h[N-1] \\ 0 & h[0] & h[1] & \cdots & h[N-2] \\ 0 & 0 & h[0] & \cdots & h[N-3] \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & h[N-K] \end{bmatrix} \tag{3.13}$$

With time interleaving mismatches present, each FFE tap coefficient will see a different channel response, as shown in Fig. 3.12. To include the effect of those mismatches, assuming M time-interleaved channels, the Toeplitz matrix in equation 3.13 is modified as:

$$\begin{bmatrix} g[0] \\ g[1] \\ g[2] \\ \vdots \\ g[N-1] \end{bmatrix}^{\mathrm{T}} = \begin{bmatrix} \alpha[0] \\ \alpha[1] \\ \alpha[2] \\ \vdots \\ \alpha[K-1] \end{bmatrix}^{\mathrm{T}} \begin{bmatrix} h_1[0] & h_1[1] & h_1[2] & \cdots & h_1[N-1] \\ 0 & h_2[0] & h_2[1] & \cdots & h_2[N-2] \\ 0 & 0 & h[0] & \cdots & h_3[N-3] \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & h_L[N-K] \end{bmatrix} \tag{3.14}$$

Where the first row of the matrix represents the first channel pulse response $h_1[n]$, the second raw is the second channel pulse response $h_2[n]$ and so on. If the number of interleaved channels M is larger than or equal to the number of FFE taps K, then $L = K$. Otherwise, the interleaved channels are repeated in the rows of the matrix, and $L = rem(K, M)$, where $rem(.)$ is the reminder after division function. The resulting pulse response $g[n]$ is one possible outcome, where the first

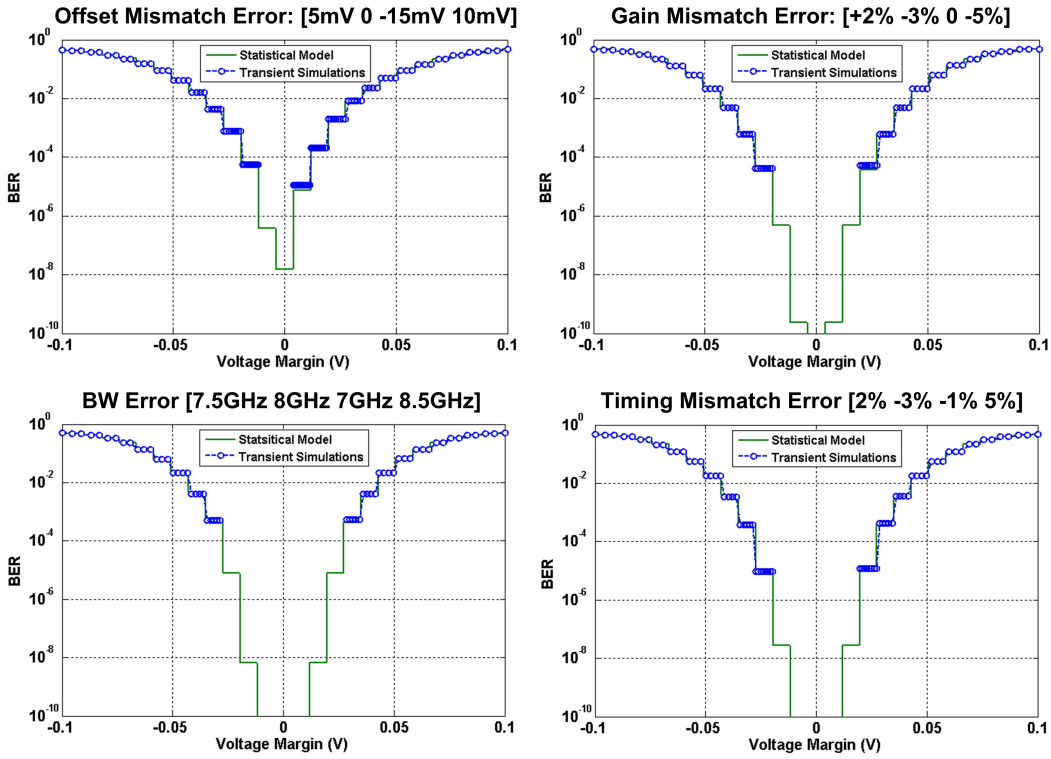


Figure 3.13: Comparison between time interleaving statistical model and transient simulations

interleaved channel is the input to the first FFE tap. Total of M pulse responses can be constructed, starting with channel m applied to the first FFE tap and circularly rotating through the other time-interleaved channels, with $m = 1, 2, \cdots M$. Each of the resulting pulse responses is used to construct an ISI PDF, and the total PDF is the average of all the M possible PDFs.

So far, the effect of gain, bandwidth and timing skew mismatch errors have been considered. The offset mismatch error is a static error, which is added to the signal before the digital FFE. In order to include the effect of offset error, the offset voltages at the input of the digital FFE are referred to the output by performing convolution with the FFE response, which may be written as:

$$O_{out}[m] = \sum_{k=0}^{K-1} \alpha[k] O[m-k] \tag{3.15}$$

Once the offset voltage is referred to the output of the FFE, a simple error PDF may be constructed according to the values of the offset voltages, and this error PDF may be included in the model by convolution with the final ISI PDF.

In order to verify the statistical time interleaving model, transient simulations are carried for different cases, where each error is considered separately and the results are compared to the transient model. A 5 bit 4-time interleaving ADC architecture is assumed with 10GS/s operation, and the results are shown in Fig 3.13. The results show very good matching between the model and the transient simulations, verifying the modeling approach used.

3.3 Exploration of Design Specifications for ADC-Based Receiver Architectures

As previously discussed, one main challenge that ADC-based receivers need to overcome is the high power dissipation of the core ADC and the digital equalization. Novel techniques, both on the architecture level and on the circuit level, are needed to reduce the power consumption of the receiver. In this section, exploration of different specifications of the receiver are considered using our developed statistical model. The effect of embedded partial analog equalization inside the ADC is studied, resulting in potential power and complexity savings of the receiver. The requirements on ADC resolution, digital resolution, digital feed-forward equalization (FFE) and digital decision feedback equalization (DFE) are obtained.

3.3.1 Embedded Partial Analog Equalization

One technique that can be used to improve the power efficiency of ADC-based receivers is to embed partial analog equalization inside the ADC. With embedded

equalization, ISI subtraction is implemented before ADC quantization. Unlike digital equalization, where the resolution is set by the ADC, embedded equalization applies the equalization taps to the un-quantized analog input, providing potential savings in overall ADC resolution and the following digital equalization.

The statistical BER model is used to evaluate the impact of embedded equalization on receiver performance. The presented results constrain DSP resolution to one bit higher than the ADC resolution and assume $1mV_{rms}$ receiver input thermal noise and receiver sampling jitter with a 20 mUI deterministic component (DJ) in the form of duty cycle distortion and a 20 mUI rms random component (RJ). Ten backplane channels [68] are analyzed for 10Gbps operation, with channel loss ranging from 11 to 37dB at the 5GHz Nyquist frequency. The ADC resolution requirements to achieve a BER better than 10^{-12} for different conditions of digital equalization complexity and embedded equalization is shown in Fig 3.14 [15]. As channel loss increases, a larger amount of digital equalization taps and higher ADC resolution are required. Moreover, with embedded equalization added to the ADC, savings of at least 2 bits of the ADC resolution can be achieved for the four highest attenuation channels.

Based on these results, two case studies for implementations of ADC front ends with embedded equalization are considered, the first with one tap of embedded DFE [13], and the second with two taps of embedded FFE plus one tap of embedded DFE [14]. For each case, the statistical simulations are first used to study the system performance. Those simulations are then compared to experimental results, where good agreement between the measurement and the model is observed.

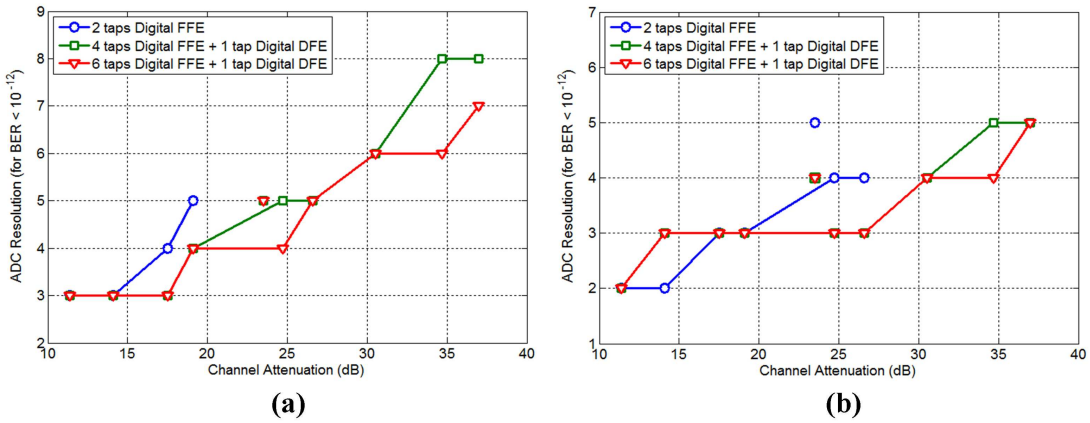


Figure 3.14: ADC resolution requirements for ADC-based 10Gbps receiver with (a) all-digital equalization and (b) 2 taps embedded FFE.

3.3.1.1 Case Study 1: 6-bit 1.6-GS/s ADC with Embedded Redundant Cycle DFE

Here, the performance impact of embedding two types of feedback equalization, DFE and IIR, inside the ADC is analyzed. Utilizing the statistical simulation model, the embedded equalization approaches are compared for different operating conditions such as channel profile, transmitter equalization, and ADC resolution.

Fig. 3.15(a) and (b) shows a block diagram comparing an ADC with an embedded DFE tap and post-ADC digital DFE. In both cases, the output MSB, which is considered the decision in a conventional 1-tap DFE with binary signaling is fed back, weighted by the DFE coefficient, and subtracted. The advantage of ADC embedded equalization is that unlike digital equalization, where the resolution is limited by the ADC, embedded equalization applies the equalization taps to the un-quantized analog input, allowing for both a lower ADC resolution and reduced digital equalization complexity at a target bit-error rate [15].

Similarly, Fig. 3.15(c) and (d) compares between embedded and digital IIR equalization realizations. In either case, the full ADC output word is scaled by

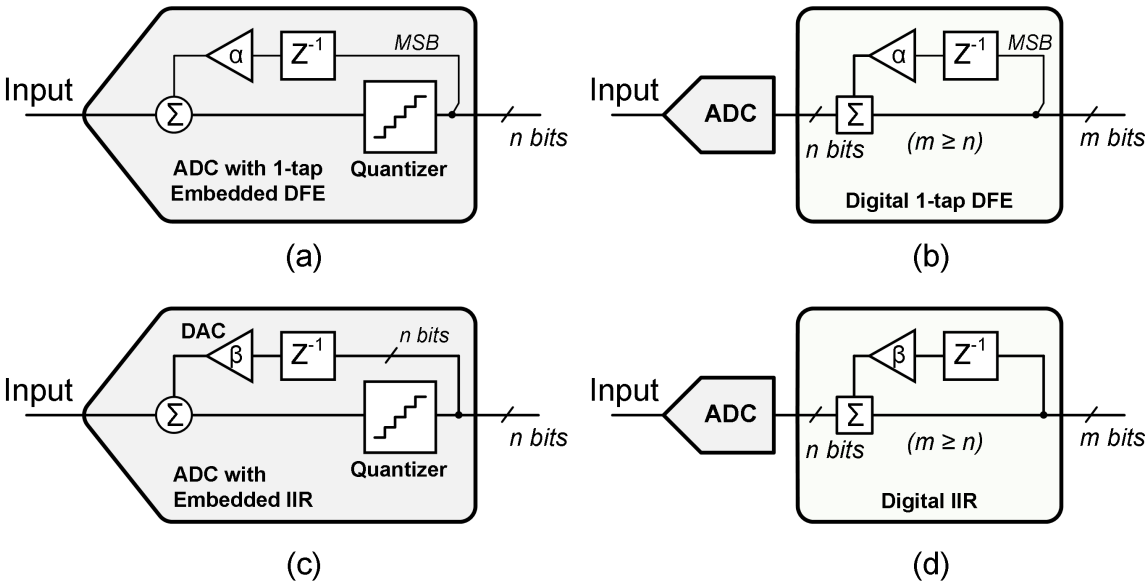


Figure 3.15: Block diagrams of (a),(b) embedded vs. digital DFE, and (c) and (d) embedded vs. digital IIR.

the equalization coefficient and subtracted from the input, where the subtraction is performed with the analog input for the case of embedded equalization and with the quantized input in the case of digital IIR. The embedded IIR offers a potential advantage over embedded DFE, in that the IIR can be optimized to cancel multiple ISI terms, rather than a single post-cursor for the DFE case. However, while an analog value can still be used for the full-scale β value, the embedded IIR suffers from the ADC quantization in the feedback, which implies a minimum ADC resolution is necessary to avoid the quantization noise propagating in the feedback system.

The statistical framework is used to model the effect of embedded equalization on system performance, with 1.6Gb/s operation assumed over the three FR4 channels shown in Fig. 3.16(a). While the first two channels display a similar 11dB channel loss at the 0.8GHz Nyquist frequency, the first channel has a smooth attenuation profile, in contrast to the second channel, which has a frequency notch near 2GHz.

In the time domain 1.6Gb/s pulse response, shown in Fig. 3.16(b), this translates to a reduced main cursor to first post-cursor ratio for the second channel and also some noticeable reflections near the fifth and sixth post-cursors. The third channel has a higher attenuation of about 14dB at Nyquist frequency. This again is reflected in the time domain pulse response, where the main cursor for the third channel is almost half that for the other two channels. The presented results assume 1Vppd transmit swing, 2.5mVrms receiver input-referred thermal noise and 10mV uniform supply noise, and receiver sampling jitter with a 0.02 unit interval (UI) deterministic component (DJ) in the form of duty cycle distortion and a 0.02 UI_{rms} random component (RJ).

The impact of including one tap of embedded DFE for each of the channels is shown in Fig. 3.16(c), quantified in terms of receiver voltage margin at 1.6Gb/s and a BER¡10-12 for a given number of TX-FIR equalization taps. Without any TX equalization (1 tap), the embedded DFE offers significant performance improvements in all three channels, with the voltage margin in channel 1 and 2 improving by 100mV and 115mV, respectively, and the higher-loss channel 3 displaying a 50mV margin from a previously closed eye. While the loss of channel 1 and 2 are similar, a higher percentage improvement with embedded DFE for the notch-shaped channel 2 is observed due to the cancellation of the first-post cursor that is a higher percentage of the main cursor value. The embedded DFE allows the optimization of the TX FIR taps to ignore the first post-cursor ISI term, which translates into more flexibility in FIR tap weighting to match a specific channel profile with additional taps. In order to have a fair comparison, the values of the TX-FIR taps are optimized separately with and without embedded DFE. Continued margin improvement is observed when TX equalization is introduced, with the embedded DFE offering a relatively constant additional 45 to 50mV for channel 1 and 2 from 2 to 4 TX FIR taps, while for channel 3 this margin increases from 20 to 30mV. Note that for these channels the voltage

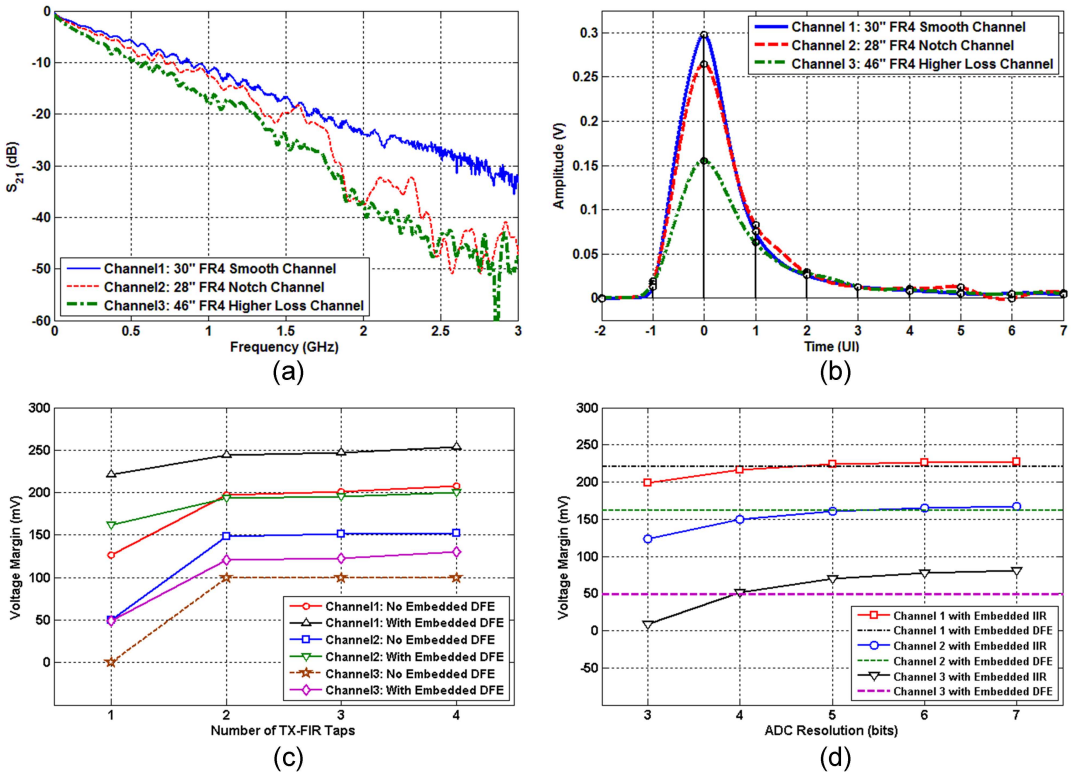


Figure 3.16: (a) Magnitude and (b) 1.6Gb/s pulse responses of three FR4 channels. (c) Impact of including one tap of embedded DFE equalization for different levels of TX-FIR equalization, and (d) impact of ADC resolution with embedded DFE and embedded IIR equalization with no TX FIR equalization over three FR4 channels.

margin roughly plateaus when TX equalization is introduced due to the majority of the residual ISI being cancelled and the 1Vpp TX peak swing constraint.

These three channels are also utilized to compare the performance of embedded IIR with embedded DFE. Fig. 3.16(d) shows the achievable 1.6Gb/s voltage margin as the ADC resolution is varied, assuming no transmit equalization. While the performance of the embedded DFE is independent of the ADC resolution, the embedded IIR equalization requires at least 4 to 5 bits of resolution to approach the performance of the embedded DFE equalization for all three channels. As the

hardware overhead of embedded IIR increases with ADC resolution, due to all the output bits being used for ISI cancellation, these results suggest that for the typical high-speed link ADC resolutions embedded DFE offers potential performance and efficiency advantages.

The statistical model is used to generate timing bathtub curves for operation under each channel, and the modeling results are compared to the measured data of the 1.6GS/s prototype with embedded DFE [13]. These simulations assume 1Vppd transmit swing, 2.5mVrms receiver input-referred thermal noise, 10mV uniform supply noise and receiver sampling jitter with a 0.032 UI deterministic component and 0.032 UI_{rms} random component. As shown in Fig. 3.17, good matching between the model and the experimental results may be observed.

3.3.1.2 Case Study 2: 6-bit 10-GS/s ADC with Embedded 2-tap FFE/1-tap DFE

A conventional architecture, consisting of an ADC and subsequent digital equalization, and a system with an ADC with embedded DFE and FFE are shown in Fig. 3.18. In order to implement a 1-tap DFE with NRZ signaling (Fig. 3.18(a),(b)), the MSB of either the ADC with embedded DFE or the digital equalizer output is fed back, weighted by the DFE coefficient, and subtracted. Quantization noise is reduced in the system with an ADC with embedded DFE, as the equalization tap is subtracted from the un-quantized analog input. In order to implement a 2-tap FFE (Fig. 3.18(c),(d)), the input signal is delayed, weighted by the FFE coefficient, and then summed. Again, quantization noise is reduced in the system with an ADC with embedded FFE, as the full analog resolution is preserved for the input, delayed signal, and the final summation value. Our previous statistical modeling studies [15], [13] have shown that the quantization noise reduction offered by both the embedded DFE and FFE equalization allows for both a lower ADC resolution and reduced digital

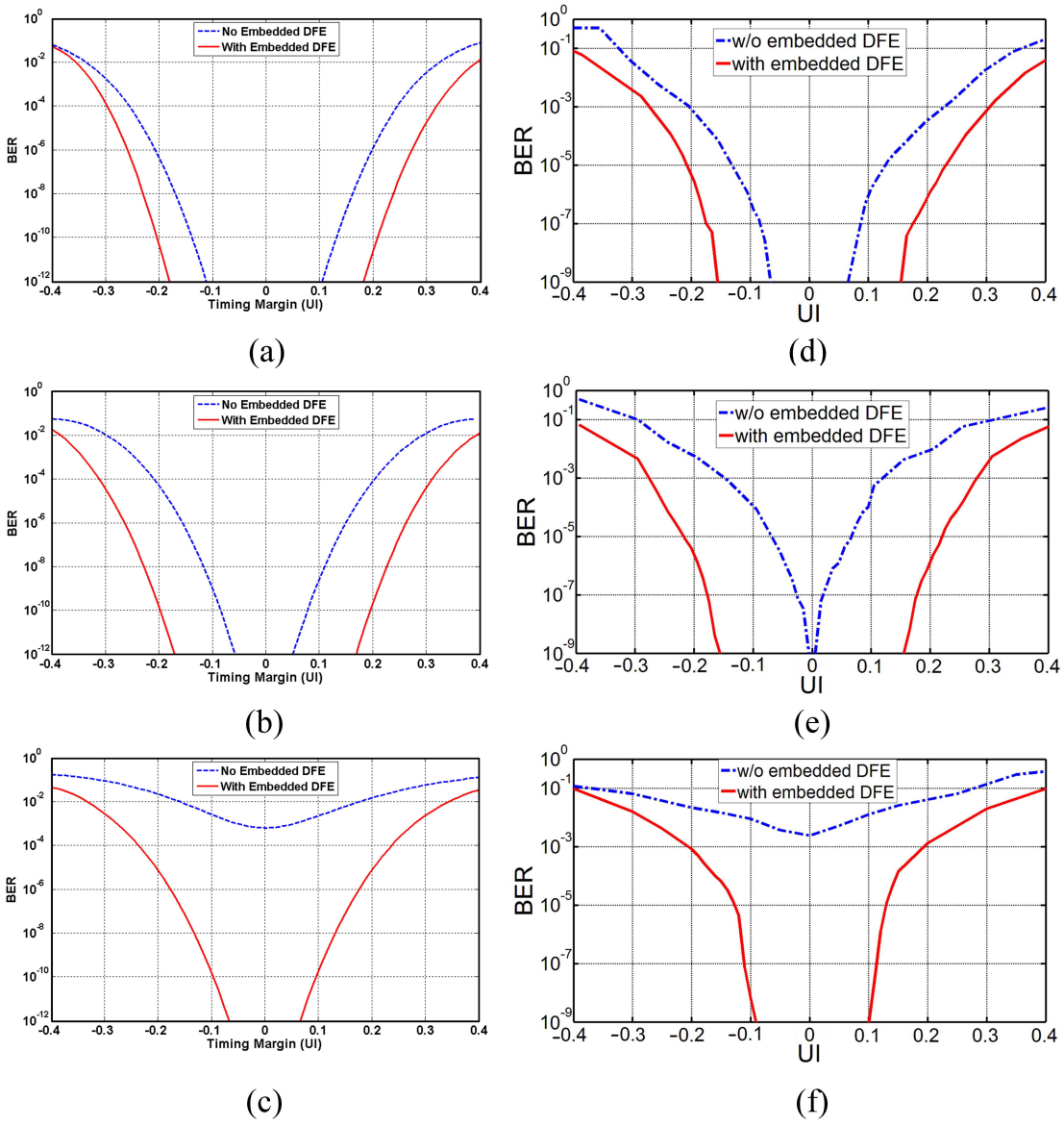


Figure 3.17: Comparison between modeling (a)-(c) and measurement (d)-(f) results for 1.6GS/s prototype with embedded DFE.

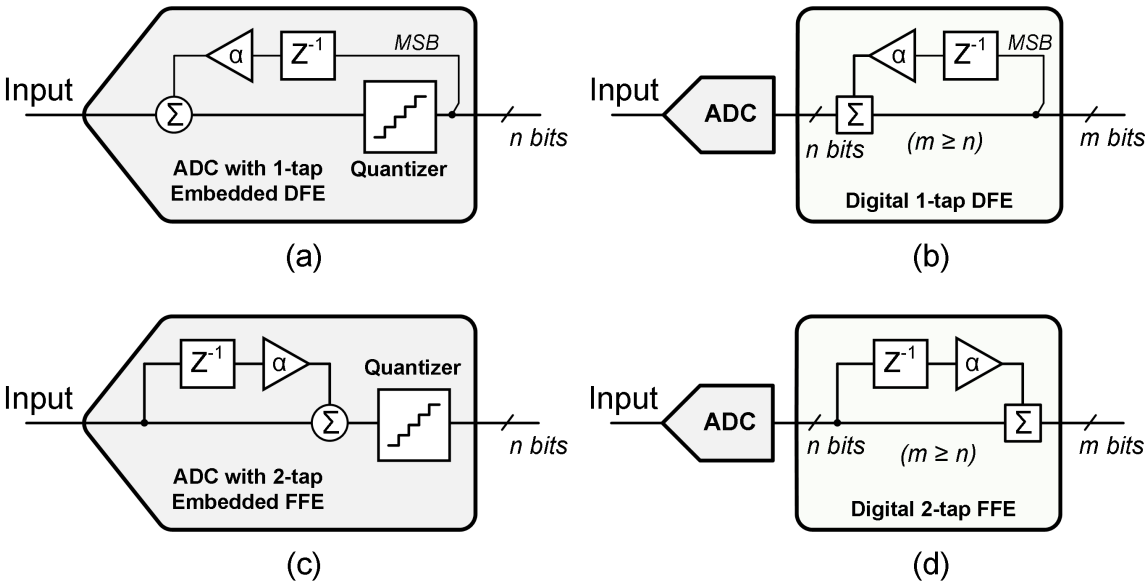


Figure 3.18: Block diagrams of (a) embedded vs. digital DFE, and (b) embedded vs. digital FFE.

equalization complexity at a target BER.

In order to quantify the relative performance impact of embedded DFE and FFE equalization, the four FR4 channels of Fig. 3.19 are utilized. As shown in Fig. 3.19(a), the loss at the 5-GHz Nyquist frequency increases with channel length, with the longest 30" channel having 23.8 dB attenuation. This is reflected in the time domain 10-Gb/s pulse responses (Fig. 3.19(b)), where the ratio of the main cursor to the ISI cursor values degrades with channel length. 10-Gb/s operation is modeled with the statistical link tool, assuming a $500mV_{ppd}$ transmit swing, 1mVrms receiver input-referred thermal noise, 5mV uniform supply noise, and receiver sampling jitter with a 0.02 unit interval (UI) deterministic component (DJ) in the form of duty cycle distortion and a 0.02 UI_{rms} random component (RJ).

Fig. 3.20 shows the advantage of embedded equalization over its digital counterpart for channels 1–3, with the receiver voltage margin (BER=10^{-12}) obtained

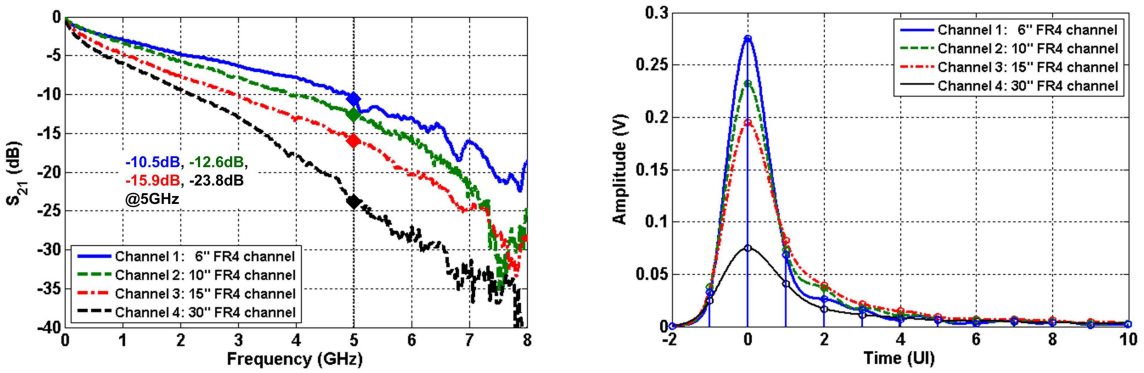


Figure 3.19: (a) Magnitude and (b) 10Gb/s pulse responses of four FR4 channels.

versus front-end ADC resolution for both digital and embedded implementations of a 2-tap FFE plus 1-tap DFE equalization structure. Similar to the prototype discussed later, here the embedded 2-tap FFE consists of an un-attenuated main cursor and an adjustable second FFE tap with $V_{LSB}/4$ maximum coefficient resolution, while the embedded DFE has an un-quantized analog resolution. Due to the quantization error, the digital equalization implementation requires more than 6-bits effective ADC resolution to achieve a similar performance as the embedded equalization architecture. The impact of the various embedded equalization schemes is shown in the 10-Gb/s voltage and timing margins of Fig. 3.21(a) and (b), respectively. For the case when no equalization is embedded in the ADC, only the relatively low-loss 6" channel displays an open eye. Including a 1-tap DFE allows cancellation of the first post-cursor ISI term, which improves the 6" channel margins and opens the previously-closed eye for the 10" channel. However, operation is still not possible for the 15" channel due to excessive residual ISI. As a 2-tap FFE can cancel significant long-tail ISI, better margins are obtained relative to the DFE-only scenario, with all three channels displaying open eyes. Combining both the 2-tap

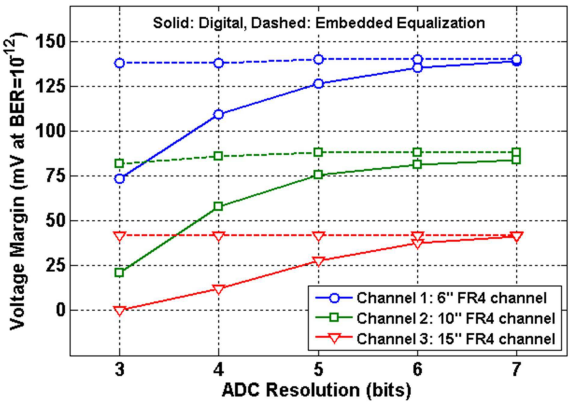


Figure 3.20: Simulated voltage margin versus ADC resolution with both digital and embedded implementations of a 2-tap FFE + 1-tap DFE equalization structure for channels 1-3 in Fig. 3.19.

FFE and 1-tap DFE yields the best margins, with the 15" channel having the largest 6× increase in voltage margin relative to the FFE-only case. Finally, it is interesting to consider the potential impact adding a front-end continuous-time linear equalizer (CTLE) can have, particularly with the highest-loss 30" channel. As shown in the Fig. 5(c) voltage and timing margins, combining embedded equalization with a front-end CTLE allows for opening a previously closed eye, with the embedded DFE providing a higher relative improvement versus embedded FFE.

These modeling results show that embedded equalization can be useful for both reducing the required ADC resolution and providing a better input signal for subsequent digital equalization, translating into a simpler digital back-end. Although it is beyond the scope of the presented work, the embedded DFE can also be used to enable a hybrid receiver mode [4]. For low ISI channels, only the embedded equalization is used with a reduced re-configurable ADC resolution, while for high ISI channels where the embedded equalization alone does not provide the target BER, the embedded DFE can be disabled to avoid potential error propagation and the front-end

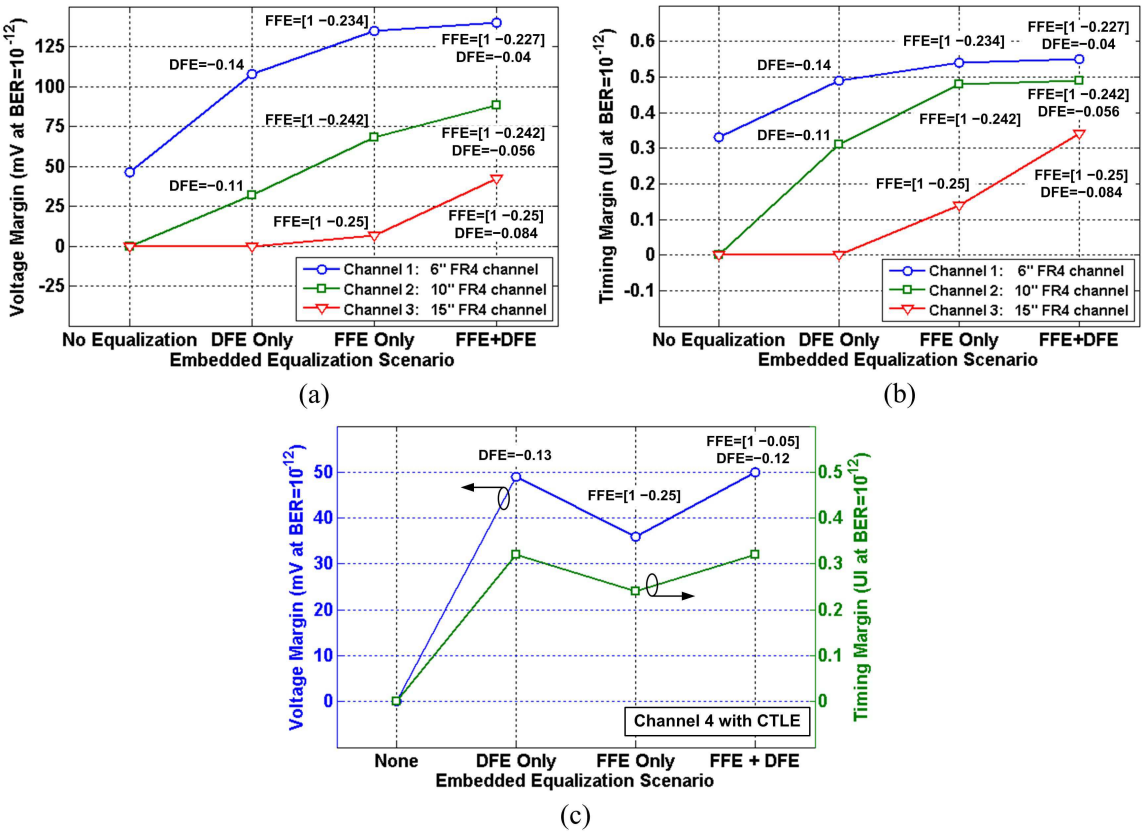


Figure 3.21: Impact of including embedded DFE and FFE equalization on (a) voltage margin and (b) timing margin for channels 1-3 in Fig. 3.19, with tap coefficients shown for the embedded equalization. (c) Impact of including embedded DFE and FFE equalization on voltage margin and timing margin in the presence of a front-end CTLE for channel 4 in Fig. 3.19.

ADC with embedded FFE allows for a reduced complexity digital equalizer relative to a separate dual-path front-end implementation [4].

The statistical model is used to generate timing bathtub curves for operation under each channel with different equalization scenarios, and the modeling results are compared to the measured data of the 10GS/s prototype with embedded FFE+DFE [14]. These simulations assume 0.5Vppd transmit swing, 1mVrms receiver input-referred thermal noise, 5mV uniform supply noise and receiver sampling jitter with

a 0.02 UI deterministic component and 0.02 UI_{rms} random component. As shown in Fig. 3.22, good matching between the model and the experimental results may be observed.

3.3.2 Requirements on Digital Feed-Forward Equalizer (FFE)

Fig. 3.23 shows the obtained voltage margin (vertical eye opening) for different ADC resolutions and different digital equalization complexities (in terms of number of taps and resolution of the DSP calculation), for 10Gbps operation over the backplane channel of Fig. 3.5. As can be seen from the results, with increased number of digital equalization taps, a lower ADC resolution is required to obtain an eye opening. In addition, increasing the resolution of the DSP to one or two bits more than the ADC resolution results in savings in the ADC resolution and the number of taps of the digital equalizer required to obtain an eye opening. It's worth noting that increasing the digital resolution beyond two bits more than the ADC resolution has negligible effect on the system performance.

3.3.3 Requirements on Digital Decision Feed-Back Equalizer (DFE)

Unlike digital FFE, which equalizes the signal by weighted feed-forward summation, digital DFE incorporates a decision made over the incoming data, which is fed back and subtracted from the previous data input samples. This makes the DFE better from noise prospective, since no noise propagates through the equalizer. However, the presence of feedback puts critical timing limitation on the implementation of the equalizer, which can be leveraged by speculation or loop-unrolling [69].

Modeling of DFE equalization is usually straight forward; the target DFE tap is ideally set to zero, assuming full cancellation of the DFE tap. In reality, a small ISI residue will always exist due to quantization of the input and the feedback coefficient, In addition, DFE exhibits error propagation, which may affect the performance of

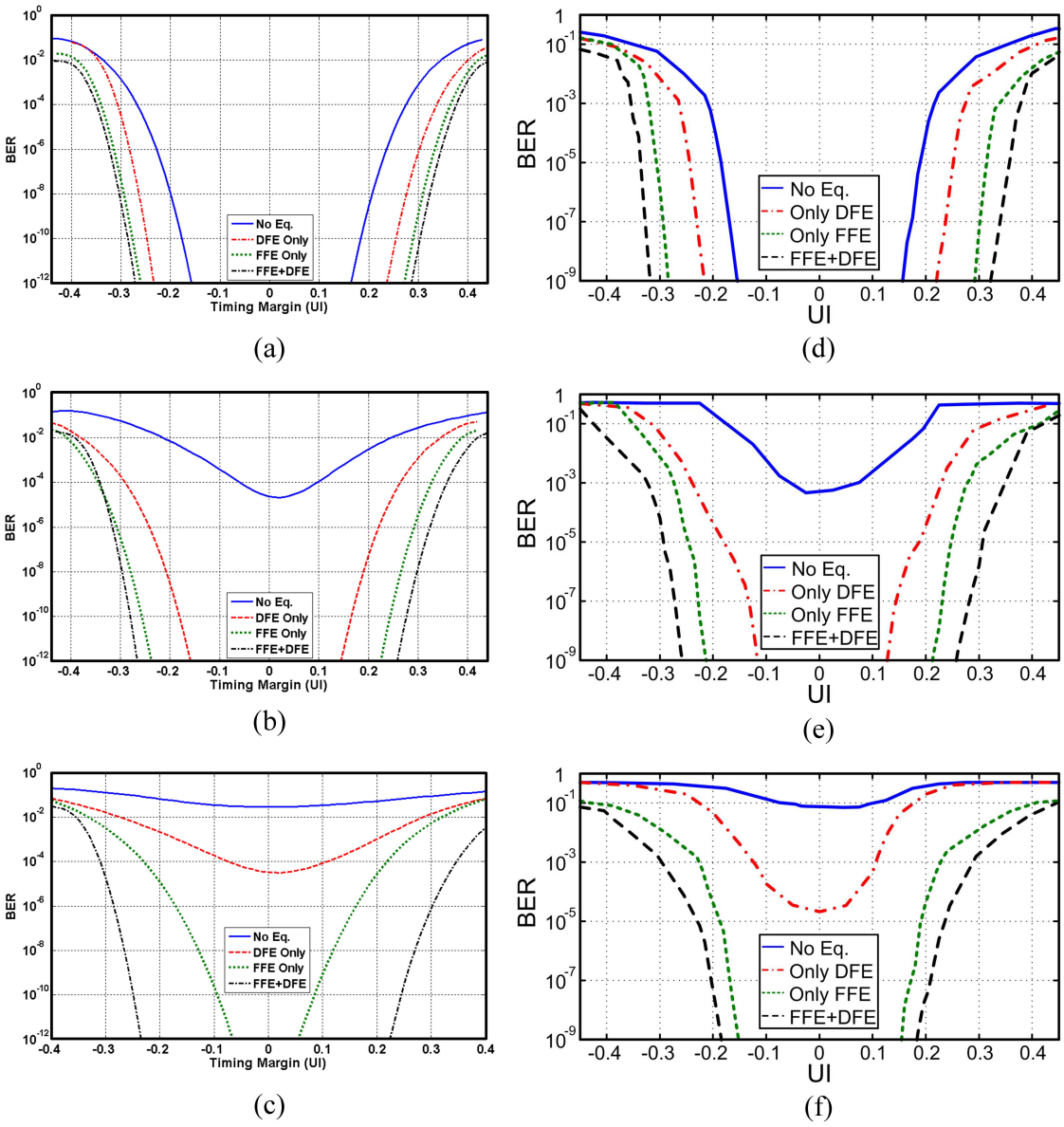


Figure 3.22: Comparison between modeling (a)-(c) and measurement (d)-(f) results for 10GS/s prototype with embedded FFE+DFE

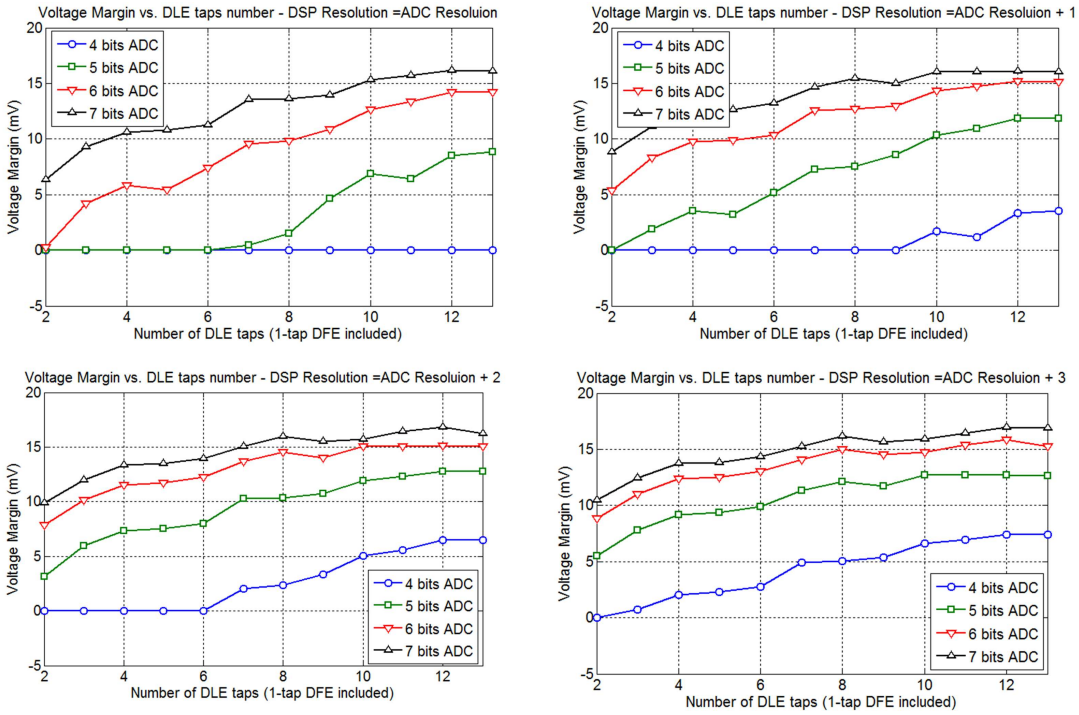
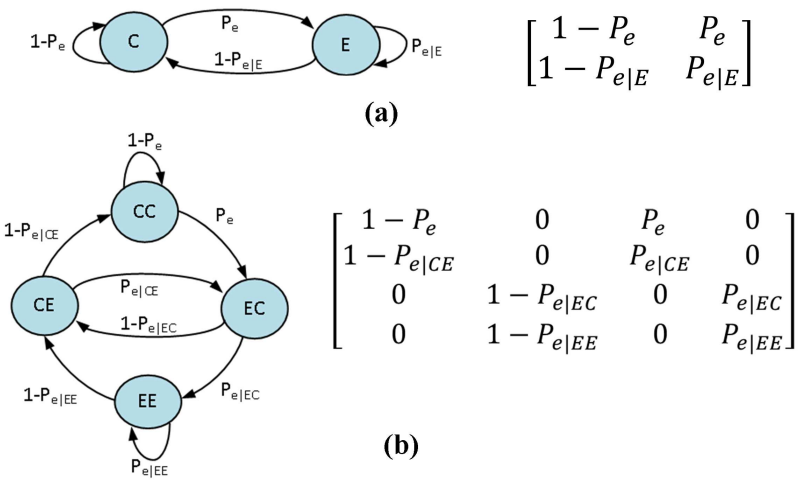


Figure 3.23: Voltage margins for 10Gbps operation under different conditions of ADC resolution and digital equalization.

the equalizer. In this subsection, the effect of error propagation on DFE equalization is evaluated. In order to model the effect error propagation effect, a Markov chain model is developed [70] to find the degradation in BER due to error propagation. Fig. 3.24 shows the transition probability state diagram and probability matrix for the simple cases of 1-tap and 2-taps of DFE equalization. For the case of 1-tap DFE, there exists only two possibilities for the current DFE tap: the previous decision can be either correct (denoted as C) or erroneous (denoted as E). The final error probability, assuming an initial wrong decision, can be given by:



$$\begin{bmatrix} 1-P_e & P_e \\ 1-P_{e|E} & P_{e|E} \end{bmatrix}$$

$$\begin{bmatrix} 1-P_e & 0 & P_e & 0 \\ 1-P_{e|CE} & 0 & P_{e|CE} & 0 \\ 0 & 1-P_{e|EC} & 0 & P_{e|EC} \\ 0 & 1-P_{e|EE} & 0 & P_{e|EE} \end{bmatrix}$$

Figure 3.24: Markov chain model showing the transition probability graph and matrix for (a) 1 tap of DFE and (b) 2 taps of DFE.

$$\begin{aligned} BER_{DFE} &= \frac{P_e}{1+P_e-P_{e|E}} \approx \frac{P_e}{1-P_{e|E}} \\ BER_{DFE} &\leq 2P_e \end{aligned} \tag{3.16}$$

Meaning that, for 1-tap of DFE, the BER degradation due to error propagation is always less than or equal to 2x.

Similarly, for the 2-tap DFE case, the final BER after an initial double error (EE) event can be put as:

$$\begin{aligned} BER_{DFE} &= \frac{2+\frac{P_{e|EC}}{1-P_{e|EE}}}{2+\frac{P_{e|EC}}{1-P_{e|EE}}+\frac{1-P_{e|CE}}{P_e}} \\ BER_{DFE} &\leq 6P_e \end{aligned} \tag{3.17}$$

Which sets the upper limit on degradation due to error propagation to no more

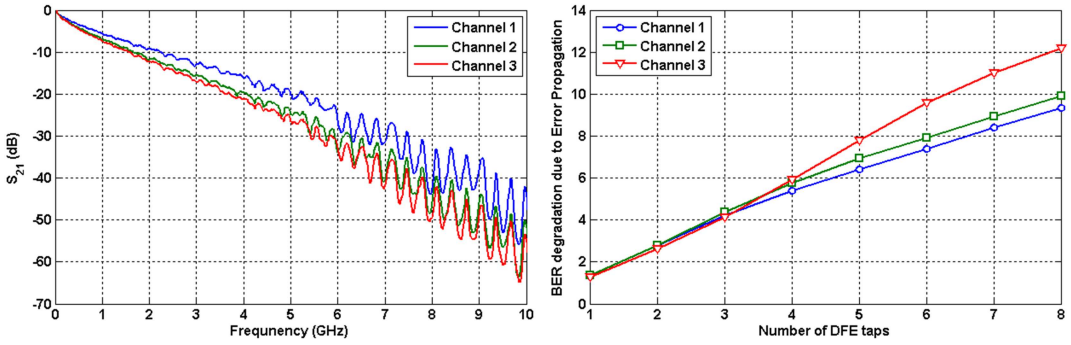


Figure 3.25: BER degradation due to error propagation vs. number of DFE taps for 3 backplane channels.

than 6x.

Following a similar approach, the magnitude of BER degradation due to error propagation can be calculated for a given channel for different number of DFE taps. The result is shown in Fig. 3.25. The figure suggests that for more than 5 DFE taps, the error propagation starts to significantly affect the BER, resulting in almost one order of magnitude degradation.

4. A 10GS/S HYBRID ADC-BASED RECEIVER*

The growth in worldwide network traffic due to the rise of cloud computing and wireless video consumption has required servers and routers to support increased serial I/O data rates over legacy channels with significant frequency-dependent attenuation. For these high-loss channel applications, ADC-based high-speed links are being considered due to their ability to enable powerful digital signal processing (DSP) algorithms for equalization and symbol detection [2, 57, 58]. Relative to mixed-signal equalizers [6], digital implementations offer robustness to process, voltage and temperature (PVT) variations, are easier to re-configure, and can leverage CMOS technology scaling in a straight-forward manner.

Despite these advantages, ADC-based receivers are generally more complex and have higher power consumption relative to mixed-signal receivers [2]. While significant improvements in multi-GS/s ADC figure-of-merit (FOM) have been recently achieved [7–9], the ensuing digital equalization can also consume a significant amount of power which is comparable to the ADC contribution [2]. Thus, in order to reduce the power of these ADC-based receiver systems, techniques to improve equalization efficiency and relax ADC resolution requirements have been developed. Non-uniform ADC quantization has been proposed to enable efficient implementations of digital decision feedback equalizers (DFEs) with either a minimal number of comparators [10] or a thermometer-code selection-based architecture [5]. However, these designs do not allow for any digital feed-forward equalization (FFE), which is useful for canceling pre-cursor and long-tail ISI. Other promising approaches included

embedding partial analog equalization inside the ADC [12–14] which allows for both reduced ADC resolution and also relaxes the requirements of the following digital equalization [15]. On the digital equalization front, techniques such as parallelized distributed arithmetic [16] and multiple supply and frequency domains [17] have been utilized to improve the digital equalizer power efficiency.

While these techniques are effective, a key issue is their efficiency in supporting operation over a wide range of channels with varying amounts of inter-symbol interference (ISI). A potential solution to this is a dual-path receiver which employs two operation modes [58], either an ADC-based receiver with digital equalization or a parallel slicer-based receiver with a continuous-time linear equalizer (CTLE). However, this parallel slicer-based path can only provide 10dB peaking to support low-loss channels, while for high-loss channels the ADC and digital equalizer are constantly in operation.

This work presents a hybrid ADC-based serial link receiver architecture which employs both a 3-tap analog FFE embedded inside a 6-bit asynchronous SAR ADC and a per-symbol dynamically-enabled digital equalizer to reduce digital equalization complexity and power consumption over a wide range of channels [20]. Section 4.1 provides an overview of the proposed hybrid receiver architecture which leverages a reliable symbol technique to dynamically-enable the digital equalizer and presents statistical simulation results which quantify the potential power savings. Key design details of the 6-bit asynchronous SAR ADC with embedded 3-tap analog FFE are discussed in section 4.2. Section 4.3 details how the digital equalizer, consisting of a 4-tap FFE and 3-tap DFE, is modified to allow for per-symbol dynamic-enabling. Experimental results from a general purpose (GP) 65 nm CMOS prototype are presented in section 4.4. Finally, section 4.5 concludes this section.

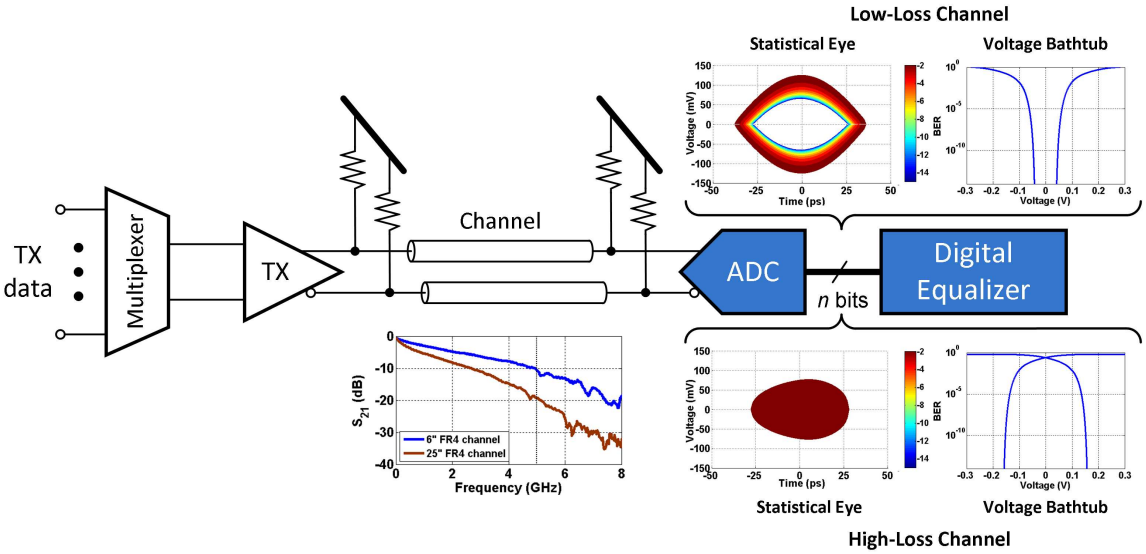


Figure 4.1: A 10Gb/s high-speed electrical link system with a front-end ADC and digital equalizer.

4.1 Hybrid ADC-Based Receiver Architecture

In order to understand the reliable symbol detection concept that the proposed hybrid ADC-based receiver utilizes to dynamically enable the digital equalizer on a per-symbol basis, consider the wireline transceiver block diagram of Fig. 4.1. Here the incoming symbols at the channel output are digitized by the front-end ADC and then equalized with the digital equalizer. As shown by the pre-equalizer 10Gb/s statistical bit error rate (BER) eye diagrams and voltage-margin bathtub curves, which assume a 1Vppd transmitter swing, the receiver margins are a strong function of the channel loss. For the lower-loss 6 FR4 channel the eye is open, implying that no subsequent digital equalization is necessary to correctly detect the received symbols. However the higher-loss 25 channel displays more ISI, resulting in a closed eye and the necessity for additional equalization to enable reliable operation.

4.2 gives a closer look at the BER voltage bathtub curves for the two channels,

where each curve represents the probability of erroneously detecting either an unreliable 0 or 1 symbol as a function of the slicer threshold voltage. For the lower-loss channel (Fig. 4.2(a)), a voltage region centered about the nominally-optimal zero threshold for a conventional binary two-level slicer allows for reliable detection of both 0 and 1 symbols at the target BER. Unfortunately, for the higher-loss channel (Fig. 4.2(b)), the same nominal zero threshold would result in unacceptable BER performance due to the excessive channel ISI. For this case, typical receivers employ equalization on all the received symbols to cancel this ISI and open the eye to achieve the target BER. However, even when the eye is closed at the target BER, certain received symbols have a very low probability of generating an error. Symbols received with voltages in the reliable 0 and 1 regions do not necessarily require any additional equalization to achieve the target BER. In order to distinguish between these reliable symbols and the unreliable symbols in the ambiguous region which do require subsequent equalization, a three-level decision can be used utilizing thresholds set at the border between the reliable and ambiguous regions. This provides suitable information to enable the digital equalizer on an as-needed basis when an unreliable symbol is detected. Whereas, when a reliable symbol is detected, no additional equalization is necessary and the digital equalizer can be bypassed to potentially save significant power.

Employing analog pre-equalization, where the input signal is partially equalized before the ADC quantization, can shrink the ambiguous voltage region for a given channel and reduce the number of received symbols which require further digital equalization. As shown in the high-loss channel bathtub curves of Fig. 4.3, embedding FFE in the ADC shrinks the ambiguous voltage region from 154mV to 24mV and reduces the rate of unreliable symbols from 49% to less than 5%. Furthermore, quantization noise is reduced in a system with an ADC with embedded equalization,

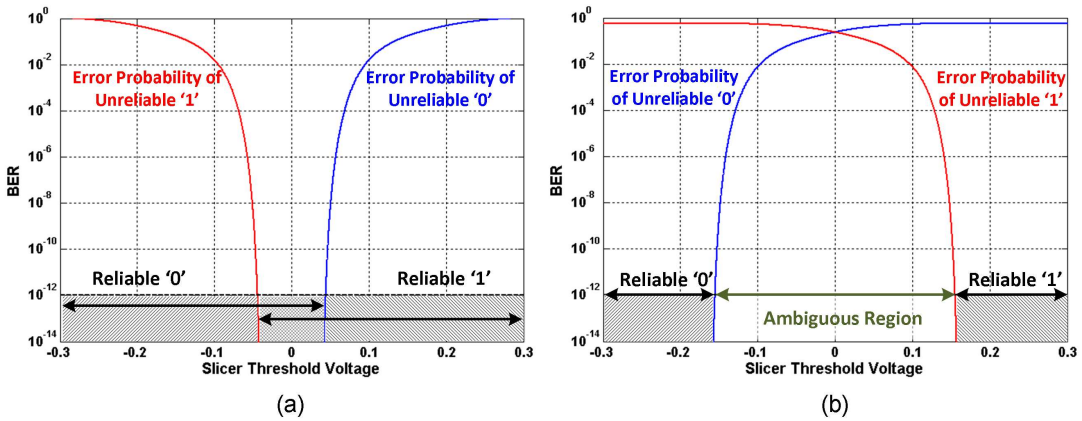


Figure 4.2: 10Gb/s BER voltage bathtub curves for the 4.1 lower-loss channel and (b) higher-loss channel.

as the ISI subtraction is performed on the un-quantized analog input. This allows for both reductions in the ADC resolution requirements and the subsequent digital equalizer complexity [15].

Combining the concept of reliable symbol detection with partial analog equalization, Fig. 4.4 shows the proposed hybrid ADC-based receiver architecture which includes both a 3-tap FFE embedded in a 6-bit ADC and per-symbol dynamically-enabled digital equalization Fig. [20]. A digital threshold detector, whose levels are programmable based on the channel loss and target BER, monitors the ADC output to decide whether the incoming symbol are reliable. If the quantized signal lies in the reliable range, the digital equalizer is bypassed and a symbol decision is made based on the ADC output MSB. For signals in the ambiguous region, the digital equalizer is enabled on a per-symbol basis to achieve the target BER.

A statistical modeling tool [15] is utilized to estimate the performance of the hybrid ADC-based receiver. This modeling tool calculates the ISI probability density function (PDF) at the channel output and combines it with PDFs of other noise

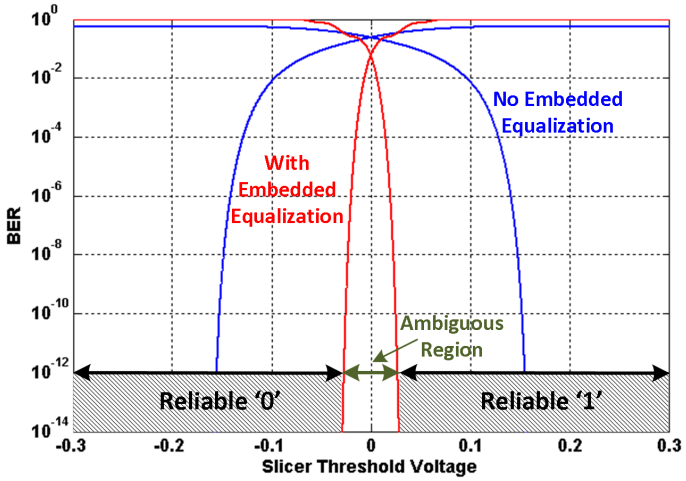


Figure 4.3: 10Gb/s BER voltage bathtub curves for the Fig. 1 higher-loss channel when an embedded 3-tap FFE is included in the front-end ADC.

sources, including ADC and digital equalizer quantization noise, using convolution in order to predict voltage and timing margins at the receiver. Simulations are carried out for the four FR4 channels shown in Fig. 4.5, which display channel attenuations at the 5GHz Nyquist rate that range from 21dB to 36.4dB when the additional 1.5dB loss due to the chip package and short PCB test-board traces are considered. These channel responses provide inherent bandwidth limiting at the ADC input, allowing for no explicit anti-aliasing filter in the receiver. As shown in the 10Gb/s pulse responses, the amount of ISI is a strong function of the channel loss. Assuming a 1Vppd transmit swing, 1mVrms receiver input-referred thermal noise, 5mV uniform power supply noise, and receiver sampling jitter with a 0.02 unit interval (UI) deterministic component (DJ) in the form of duty cycle distortion and a 0.02UIrms random component (RJ), Fig. 4.6 shows the obtained voltage and timing bathtub curves when only the embedded equalization in the ADC is utilized and when the digital equalizer is enabled. As in the prototype detailed later, the embedded

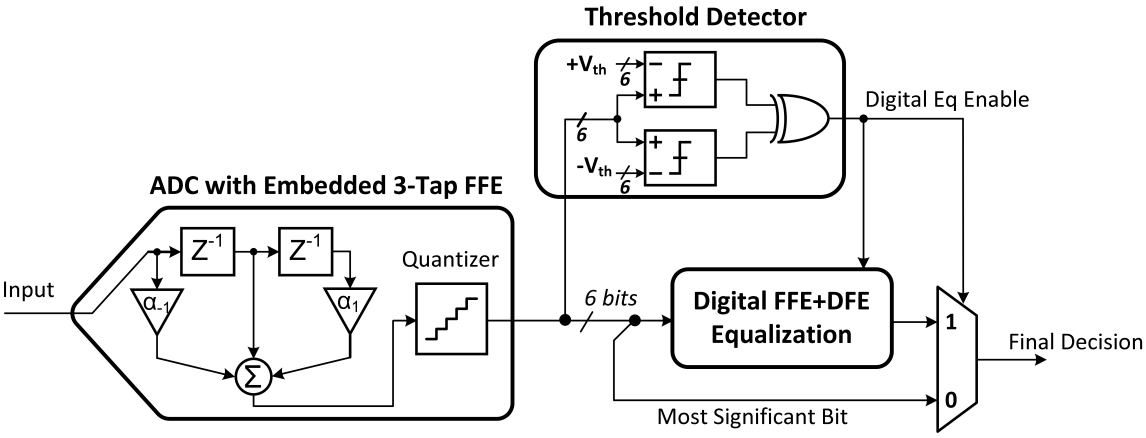


Figure 4.4: Proposed hybrid ADC-based receiver architecture.

3-tap FFE consists of an un-attenuated main cursor and a pre-cursor and post-cursor tap with 1.1VLSB resolution, while the digital equalization implements a 4-tap FFE and a 3-tap DFE. Open eyes are achieved over the two lowest attenuation channels with only the 3-tap embedded FFE enabled, with no further digital equalization necessary (Fig. 4.6(a)). However, exclusive use of the 3-tap embedded FFE is not sufficient to achieve reliable operation for the two higher attenuation channels. As shown in Fig. 4.6(b), including the digital equalizer allows opening of the previously closed eyes with the higher attenuation channels.

In order to estimate the power savings with the proposed hybrid ADC-based receiver architecture, seven FR4 channels are considered with attenuations ranging from 11.5dB to 36.4dB. The probability density function of the received signal amplitude is constructed for each channel and the operational percentage of the digital equalizer is calculated based on the probability of the quantized signal falling within the ambiguous regions threshold levels. As a digital threshold detector is employed, these threshold levels are also quantized with the 6-bit ADC resolution. The modeling results of Fig. 4.7 show that utilizing the reliable symbol detection technique

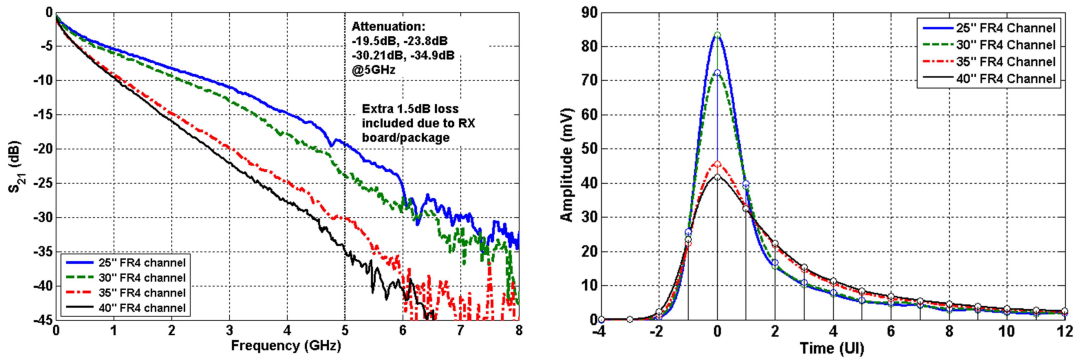


Figure 4.5: (a) Magnitude and (b) 10Gb/s pulse responses of four FR4 channels.

in combination with ADC embedded equalization allows for the digital equalizer to be disabled at near 100% for channel attenuations close to 25dB, while up to 85% of the digital equalizer power can ideally be saved with a 36.4dB channel. Realistically though, in disable mode power will still be dissipated due to the switching of the threshold detector and the digital equalizer leakage power. A power overhead near 20% is estimated from the gate level implementation of the equalizer using realistic simulation-generated switching activity vectors, resulting in a total power savings near 70% for up to 36.4dB of channel attenuation.

It is also interesting to consider the impact the proposed hybrid ADC-based receiver has on clock-and-data recovery (CDR) functionality. While not implemented in the presented prototype, two schemes are envisioned where a baud-rate CDR phase detector either utilizes 6-bit data from the output of the ADC with embedded FFE, bypassing the dynamically-enabled digital equalization, or utilizes 6-bit data from the final output of the hybrid-ADC receiver which also includes the digital equalization. There are trade-offs with both schemes, as shown in the Fig. 4.8 CDR simulation results with the 35 channel. For the case where the final output

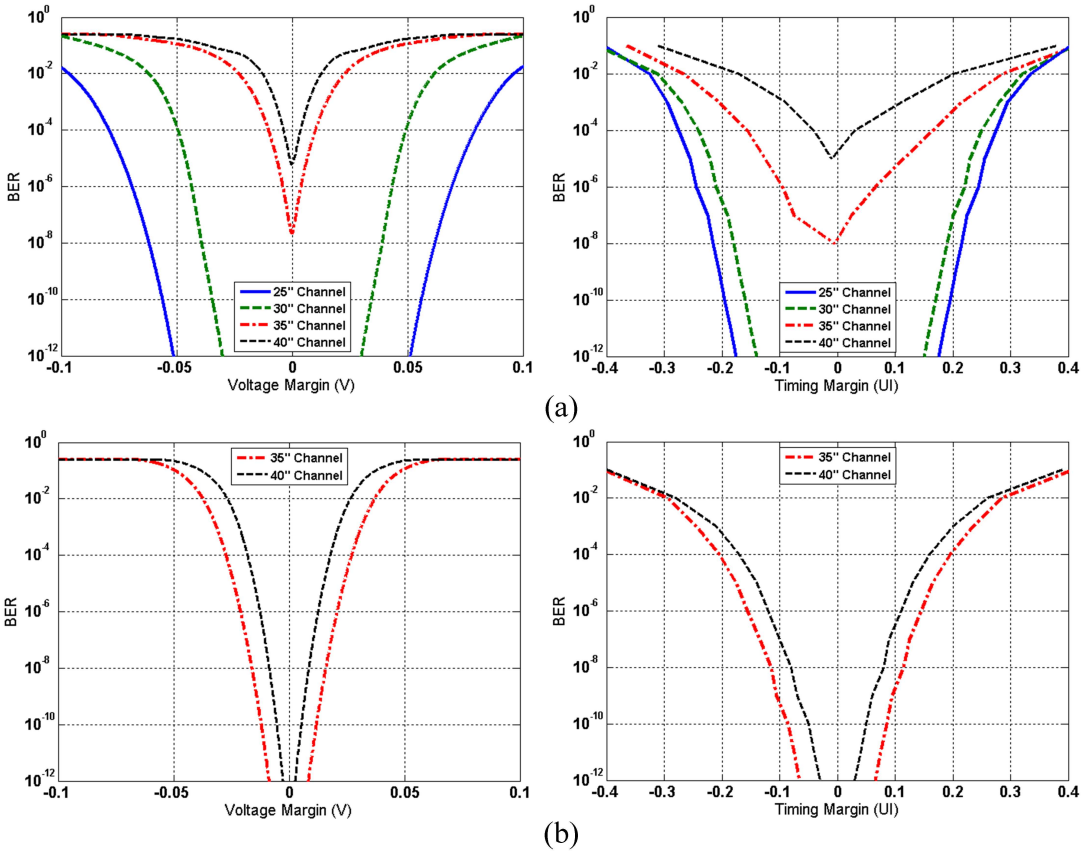


Figure 4.6: Simulated voltage and timing margins for (a) the four Fig. 4.5 channels with 3-tap embedded FFE only and (b) the two higher attenuation channels with both 3-tap embedded FFE and digital equalization.

with both embedded and dynamically-enabled digital equalization is utilized, the Mueller-Muller phase detector transfer characteristic displays near zero phase offset due to the improved ISI cancellation, while utilizing only the embedded equalization does result in a 0.02UI offset. This results in somewhat improved high-frequency jitter tolerance for the design which utilizes the phase detector at the final output. However, this comes at the cost of additional CDR latency, which translates into a lower 0.4 MHz loop-bandwidth relative to 0.63 MHz achieved with the design which places the phase detector directly at the ADC output. Note that for operation over

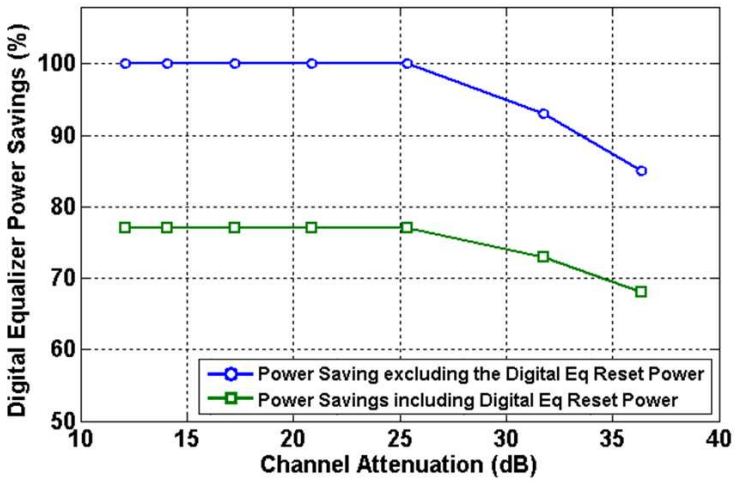


Figure 4.7: Simulated digital equalizer power savings versus channel attenuation with the proposed hybrid ADC-based receiver architecture.

a channel with low loss, which would ideally result in the digital equalization being always disabled, the final-output CDR is still receiving data from the ADC-output which includes embedded FFE with some additional latency. In this scenario, the final-output CDR performance should converge to the same high-frequency jitter tolerance as the ADC-output CDR, but with reduced loop bandwidth.

4.2 Asynchronous SAR ADC Implementation

While the previous modeling results have shown that embedded equalization in the ADC allows for reliable operation over 25dB loss channels with no/little digital equalization, an efficient implementation is necessary in order not to degrade ADC-based receiver power efficiency. This section details the design of a 6-bit 10GS/s asynchronous SAR ADC with a 3-tap FFE embedded in the capacitive DAC of the time-interleaved unit ADCs in a low-overhead approach.

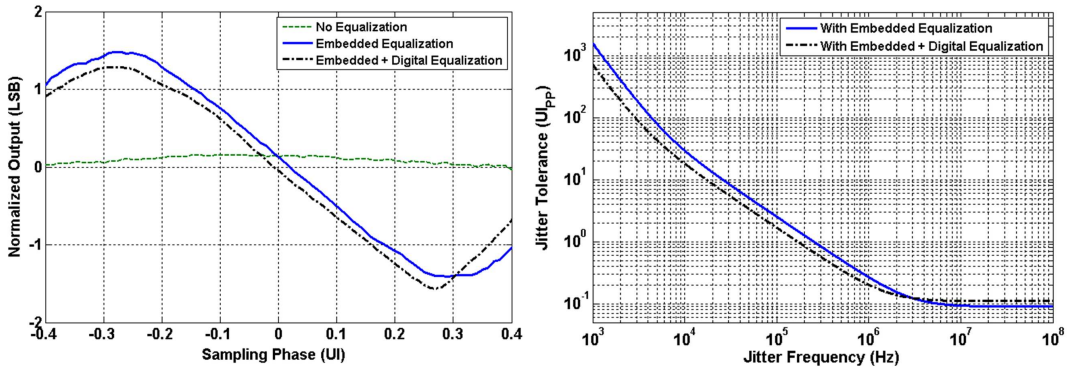


Figure 4.8: Simulated hybrid-ADC receiver baud-rate CDR performance for operation over the 35 channel: (a) Mueller-Muller phase detector characteristics, (b) jitter tolerance for BER=10-12.

4.2.1 SAR ADC with Embedded 3-Tap FFE

A sampled FFE can be efficiently embedded in the front-end ADC by incorporating the FFE multiplication and addition in the switched-capacitor structure of the SARs feedback DAC [14]. Fig. 4.9(a) shows a simplified single-ended unit ADC schematic to illustrate the switched- capacitor implementation of the 3-tap FFE during the first two phases of the SAR conversion, the sampling phase and the MSB computation. Here the un-attenuated main cursor tap is realized with the sampled input on CS. The pre- and post-cursor FFE taps are embedded inside the capacitive DAC structure with the $A_{1,-1}$ to $A_{5,-1}$ switches and the $A_{1,1}$ to $A_{5,1}$ switches that select between the pre/post-cursor input samples or ground to provide the α_{-1} pre-cursor and α_1 post-cursor coefficients without impacting the main cursor value. Since the pre and post-cursors share the connections to the same capacitors, each capacitor may be configured to implement either the pre-cursor or the post-cursor coefficient, but not both. This does impose limitations on the possible values that

can be assigned to each tap. However, this was not a major issue for the wide range of channels utilized in the experimental results of Section V. While it is possible to add more than three embedded taps, this must be balanced with the overhead due to additional routing capacitance. In addition, adding more taps would further limit the possible values each tap may take.

Bottom-plate sampling is used during the sampling cycle to apply Vin,n onto the CS capacitor and $V_{in,n-1}$ and $V_{in,n+1}$ onto a portion of the DAC capacitors. In the Fig. 4.9(b) example, the FFE coefficients α_{-1} and α_1 are defined by 5-bit words $A_{1,-1}A_{2,-1}A_{3,-1}A_{4,-1}A_{5,-1} = 00010$ and $A_{1,1}A_{2,1}A_{3,1}A_{4,1}A_{5,1} = 01001$ to charge the corresponding capacitors with $V_{in,n+1}$ and $V_{in,n-1}$, respectively, and discharge the remaining DAC capacitors. During the MSB computation cycle (Fig. 4.9(c)), the ϕ_S switches are OFF and the bottom-plate of all the DAC capacitors are connected to ground. The resultant charge sharing induces a voltage equal to $\alpha_{-1}V_{in,n+1}\alpha_1 V_{in,n-1}$ at the comparator positive input. By having the main cursor value $V_{in,n}$ at the comparator negative input, the effective voltage $V_{in,n} - \alpha_{-1}V_{in,n+1} - \alpha_1 V_{in,n-1}$ appears at the comparator differential input to emulate a 3-tap FFE. The adjustable pre- and the post-taps are hard-wired for subtraction, allowing for a high-pass filter function which is generally desired in wireline applications. Designing CS to be equivalent to the total DAC capacitance allows the main and pre/post-cursor taps to all experience the same capacitive-division attenuation at the comparator inputs. Hence, the 3-tap FFE normalized pre-cursor tap α_{-1} and post-cursor tap α_1 coefficients are insensitive to parasitic capacitances, and can be calculated as:

$$\alpha_{-1} = \frac{(A_{1,-1}A_{2,-1}A_{3,-1}A_{4,-1}A_{5,-1})_2}{32}, \alpha_1 = \frac{(A_{1,1}A_{2,1}A_{3,1}A_{4,1}A_{5,1})_2}{32} \tag{4.1}$$

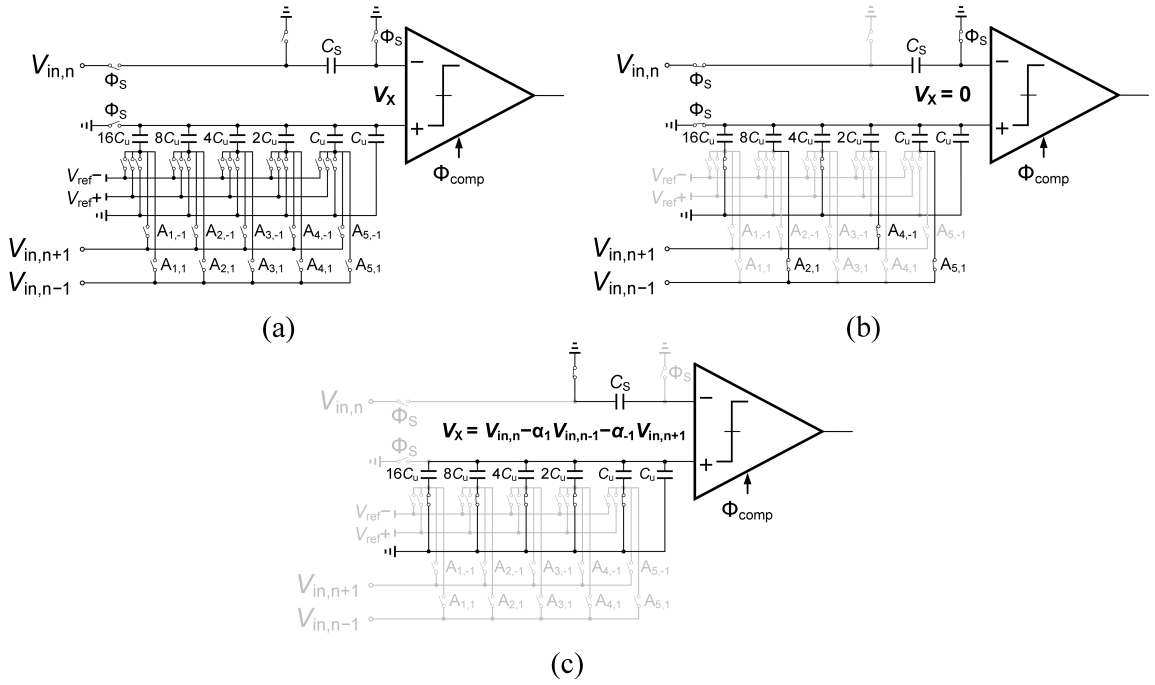


Figure 4.9: Simplified unit SAR ADC with embedded 3-tap FFE: (a) single-ended schematic, and operation during the (b) sampling phase, and (c) first MSB evaluation assuming $A_{1,-1}A_{2,-1}A_{3,-1}A_{4,-1}A_{5,-1} = 00010$ and $A_{1,1}A_{2,1}A_{3,1}A_{4,1}A_{5,1} = 01001$ for the post-cursor tap.

where (.)2 represents the binary-to-decimal conversion operator.

4.2.2 10GS/s Time-Interleaved ADC Architecture

Fig. 4.10 shows the block diagram of the complete 10-GS/s 6-bit converter with the 3-tap FFE embedded in the 32 time-interleaved unit ADCs. Eight parallel sub-ADCs are employed that operate at fs/8 = 1.25 GS/s and are individually made up of four parallel unit asynchronous SAR ADCs working at fs,unit = fs/32 = 312.5 MS/s. Each unit ADC has seven operation cycles: one for input and pre/post-cursor FFE sampling, and six for asynchronous bit conversions. Eight front-end track-and-holds (T/Hs), one per sub-ADC, are employed to limit the number of critical sampling phases to eight at 1.25GHz each. With three embedded FFE taps, the output of each

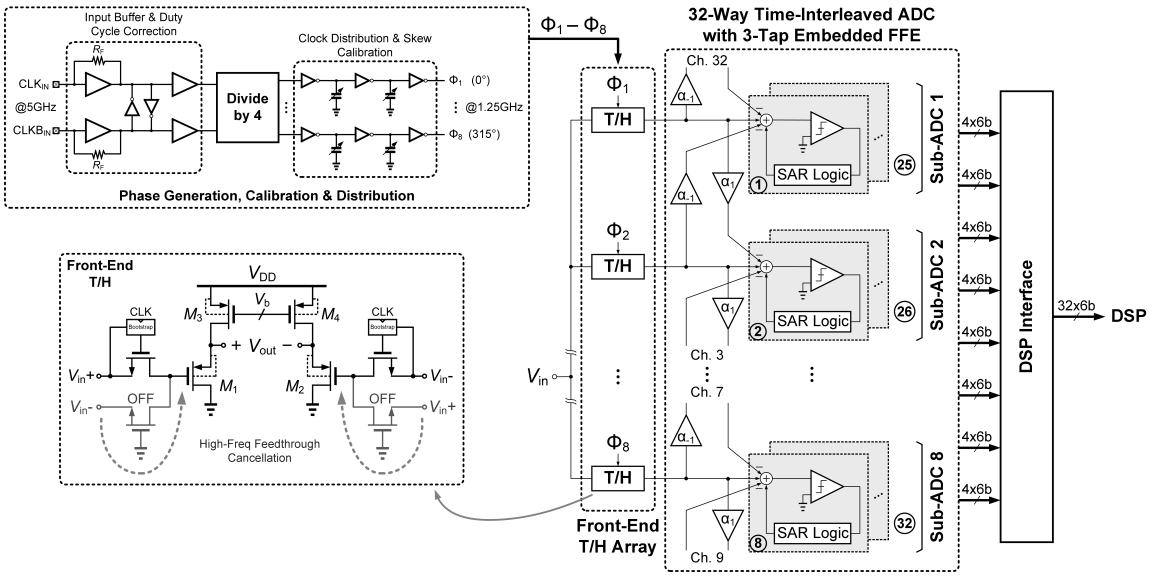


Figure 4.10: Block diagram of the 32-way time-interleaved asynchronous SAR ADC with 3-tap embedded FFE.

T/H needs to be routed to three sub-ADCs. Post-layout simulations show that this additional routing, relative to a non-embedded FFE design, results in about 2.25X increase in the loading capacitance. These 100ps-spaced eight phases are generated with a differential divide-by-four circuit that is clocked with a 5GHz differential input clock. Digitally-controlled capacitor banks, with ¡ 0.4ps resolution and 30ps range, are employed to calibrate timing mismatches in the clock distribution to the T/H blocks. Calibration DACs are also included for independent comparator offset correction and linear gain calibration in the 32 unit SAR ADCs.

4.2.3 Unit Asynchronous SAR ADC

The fully-differential schematic of the 6-bit unit asynchronous SAR ADC with embedded 3-tap sampled FFE is shown in Fig. 4.11. A modified StrongArm comparator with two differential input pairs is used [14]. One input pair is connected to the sampling capacitor which samples the main cursor, while the other input pair is

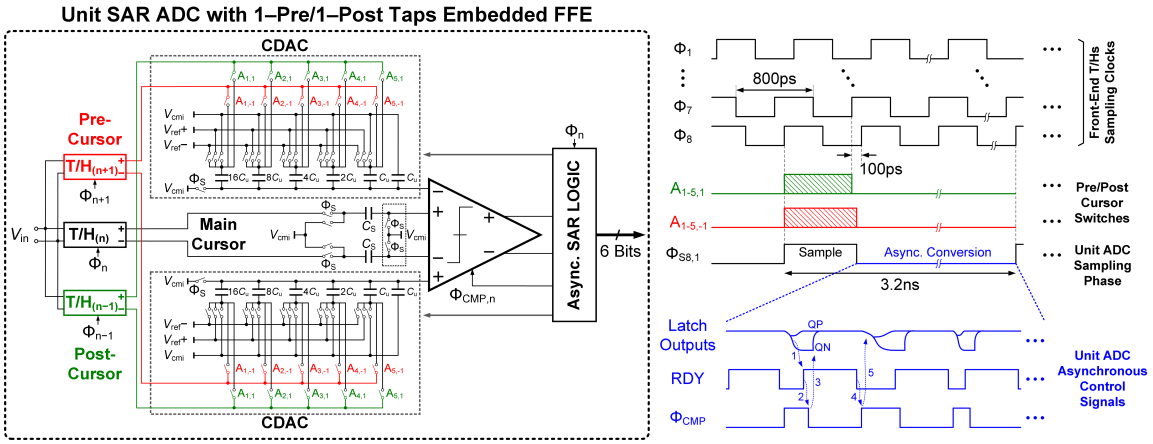


Figure 4.11: Fully-differential schematic of the unit asynchronous SAR ADC with sampled 3-tap embedded FFE.

connected to the DAC output which also implements the FFE pre-cursor and post-cursor taps. In order to ensure sampling of the correct pre-cursor and post-cursor samples, the DAC switches ($A_{1,-1}$ to $A_{5,-1}$ and $A_{1,1}$ to $A_{5,1}$) are only connected during the hold period of their corresponding T/H inputs. The asynchronous operation is explained as follows: (1) as soon as the comparators complementary outputs resolve, the asynchronous logic sets the ready signal RDY to 1 and passes it to the SAR logic [71] to start the DAC operation. (2) This RDY signal resets the comparator clock CMP to 0. (3) A low ϕ_{CMP} resets the latch outputs to VDD. (4) After a specific time assigned for the DAC settling, which is set by a tunable delay element, the RDY signal goes down to 0, which signals ϕ_{CMP} to transition to 1. (5) A high ϕ_{CMP} starts the next comparator decision cycle.

A merged capacitor switching (MCS) scheme [72], which allows for very low switching energy and reduced area through removal of the MSB capacitor, is employed in the DAC of each 6-bit unit SAR ADC. To further reduce DAC area, a custom layout with a 1fF metal-oxide-metal (MOM) unit capacitor Cunit is em-

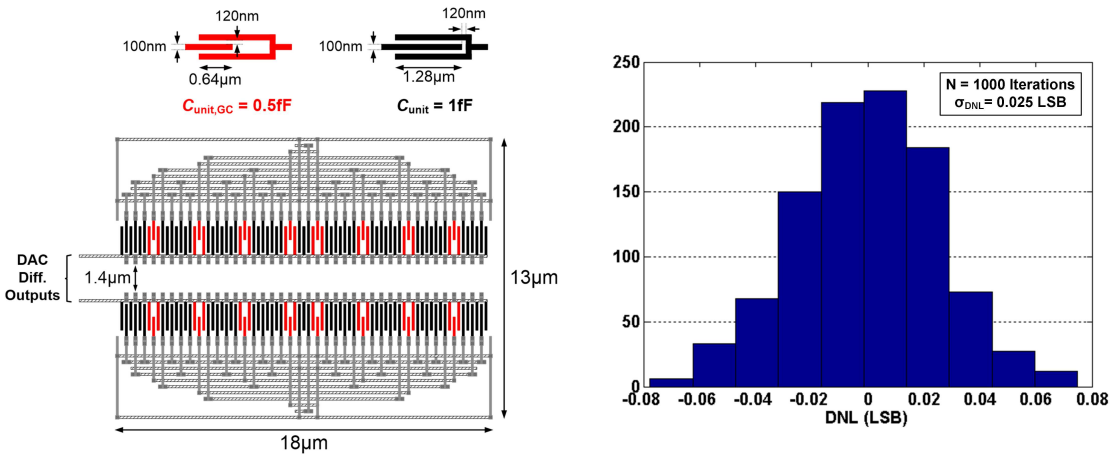


Figure 4.12: Custom layout of the differential capacitive DAC with 1fF MOM unit capacitors and embedded gain calibration, and (b) CDAC worst-case 01111 to 10000 transition DNL simulation results using 1000 Monte Carlo iterations.

ployed, as shown in Fig. 4.12(a). Four stacked minimum-width metal layers, metal 4 (M4) to metal 7 (M7), with minimum spacing are used, resulting in the optimum desired capacitance value with respect to the bottom-plate parasitic capacitance to substrate. While the loading capacitance of the T/H stages is dominated by the routing capacitance, which is 89% of the total, the use of a small unit capacitor minimizes the DAC switching and reference buffers power dissipation. The small area of the capacitive DAC also reduces the overall ADC area, resulting in less wiring capacitance. In order to ensure mismatches inside the DAC wont limit the performance, Monte Carlo simulations of the worst-case DNL error due to DAC capacitive mismatch, which happens in the transition from 01111 to 10000, are performed (Fig. 4.12(b)). The Monte Carlo parameters are extrapolated beyond the 6fF minimum MOM capacitor offered by the design kit, where the unit capacitor mismatch is approximately scaled by the square root of the capacitor area. The 1fF unit capacitor value results in maximum DNL error well below 0.5 LSB at 6 bit resolution. In order

to provide extra gain calibration capability, half-size dummy capacitors $C_{unit,GC}$ = 0.5fF are added between the DAC's main capacitor fingers. The top plates of all these dummy capacitors are connected to the DAC's output node, while the bottom plates are controlled in a binary-weighted fashion by switches which float the terminal when OFF and connect it to the comparator common-mode voltage when ON.

4.3 Dynamically-Enabled Digital Equalizer

Following the ADC is the dynamically-enabled digital equalizer shown in Fig. 4.13, which consists of a 4-tap FFE followed by a 3-tap loop-unrolled DFE and a preceding digital threshold detector block which determines the reliability of the incoming symbols. In order to achieve per-symbol dynamic enabling of the digital equalizer, this threshold detector controls latches inserted in the equalizer computation path that enables the dynamic switching of the FFE and DFE adders and multipliers. These latches are made transparent when an unreliable symbol is detected within the ambiguous region (Fig. 4.13(a)), allowing the signal to propagate through the digital equalizer and undergo the necessary extra equalization. For symbols which fall within the reliable regions (Fig. 4.13(b)), the quantized input to the equalizer is latched to prevent switching of the adders and multipliers. In order to select either the un-equalized reliable symbol MSB from the ADC output or the fully digitally-equalized bits as the symbol decision, a multiplexer bank controlled by the threshold detector is placed after the loop-unrolled DFE digital slicers.

Fig. 4.14 shows the full realization of the time interleaved digital equalizer. In order to accommodate various channels, reconfiguration of the 4-tap FFE is made possible with a main-cursor select control that allows all combinations ranging from all pre-cursor to all post-cursor equalization taps. Resolutions of 8-bit and 15-bit

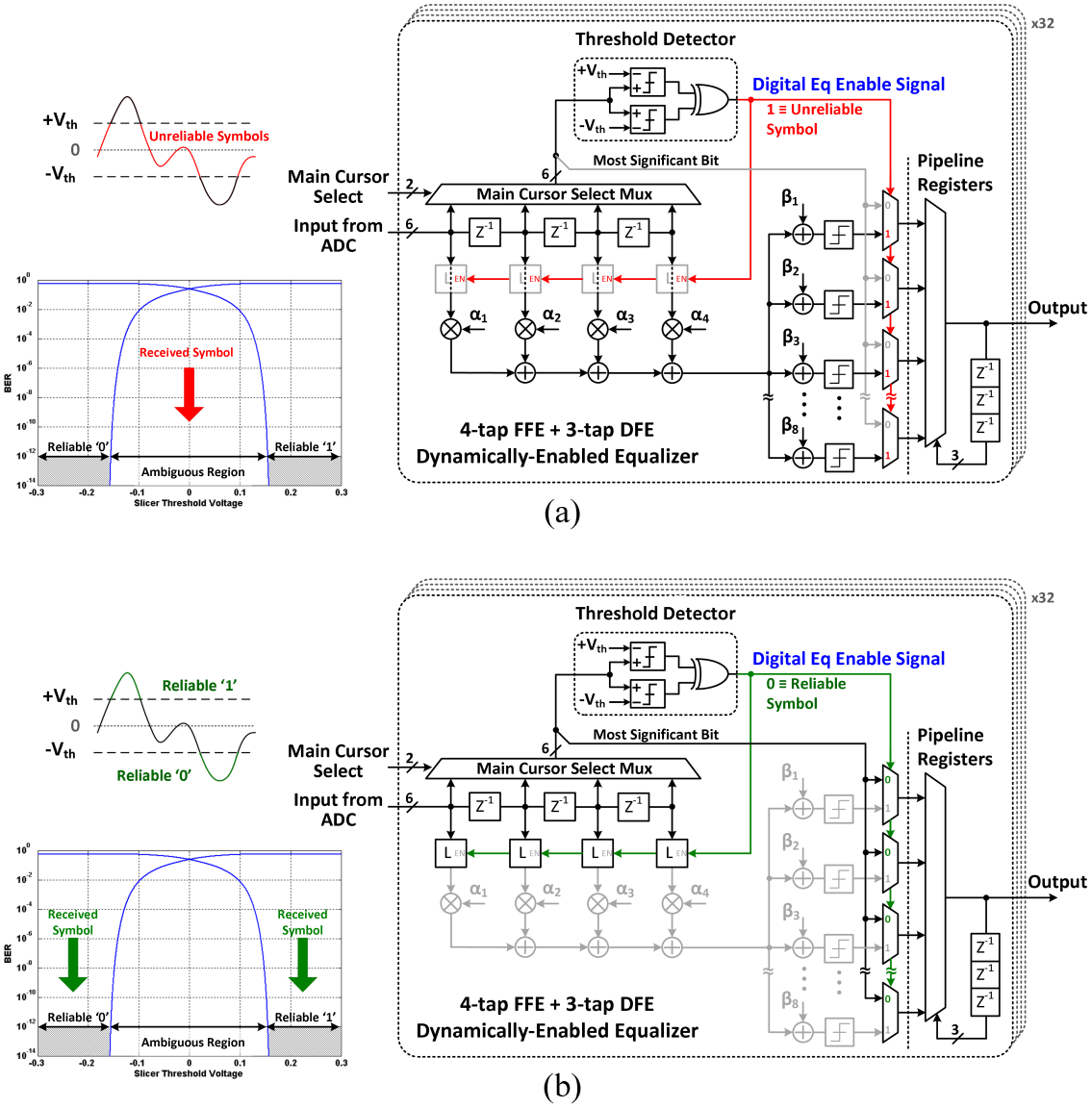


Figure 4.13: Block diagram of the per-symbol dynamically-enabled digital equalizer with 4-tap reconfigurable FFE and 3-tap loop-unrolled DFE: (a) operation under reception of an unreliable symbol and (b) operation under reception of a reliable symbol.

are utilized for the α FFE and β DFE tap coefficients, respectively. For the FFE taps, 8 bit resolution is selected to ensure the rounding errors of the tap values are negligible compared to the ADC quantization. Statistical modeling results predict that 12-bit resolution is required for the DFE taps. However, 15-bits were utilized to match the resolution of the digital signal after passing through the FFE multipliers and adders. Note that the additional three bits of DFE tap resolution were kept for convenience, and may have been truncated. A multiplexer-tree loop-unrolled architecture is utilized to meet the critical feedback timing paths of the digital 3-tap DFE [56, 69], with place-and-route timing analysis showing that loop-unrolling was required for all the DFE taps. A pipeline register bank is inserted to improve the timing slack before the DFE selection multiplexers. Placing the reliable symbol select multiplexer bank before the loop-unrolled DFE selection minimizes the multiplexer count in the DFE feedback loop, which is the most critical timing path of the digital equalizer. Note that when a reliable symbol is detected by the threshold detector, all the DFE multiplexers will have the same reliable MSB decision input and the output will be equal to this input regardless of the previous symbol decisions.

The digital equalizer was fully synthesized using a digital standard cell library and automatically placed-and-routed. 10Gb/s operation is achieved with a 32-way time-interleaved parallel implementation where each slice is clocked at 312.5MHz. An interface block re-times the digital output of the time-interleaved ADC to allow parallel computations inside the digital equalizer. As shown in Fig. 4.14, by matching the interleaving factor between the ADC and the digital equalizer, the design is simplified with the delay elements required to realize the FFE pre- and post-cursor taps in Fig. 4.13 inherently realized.

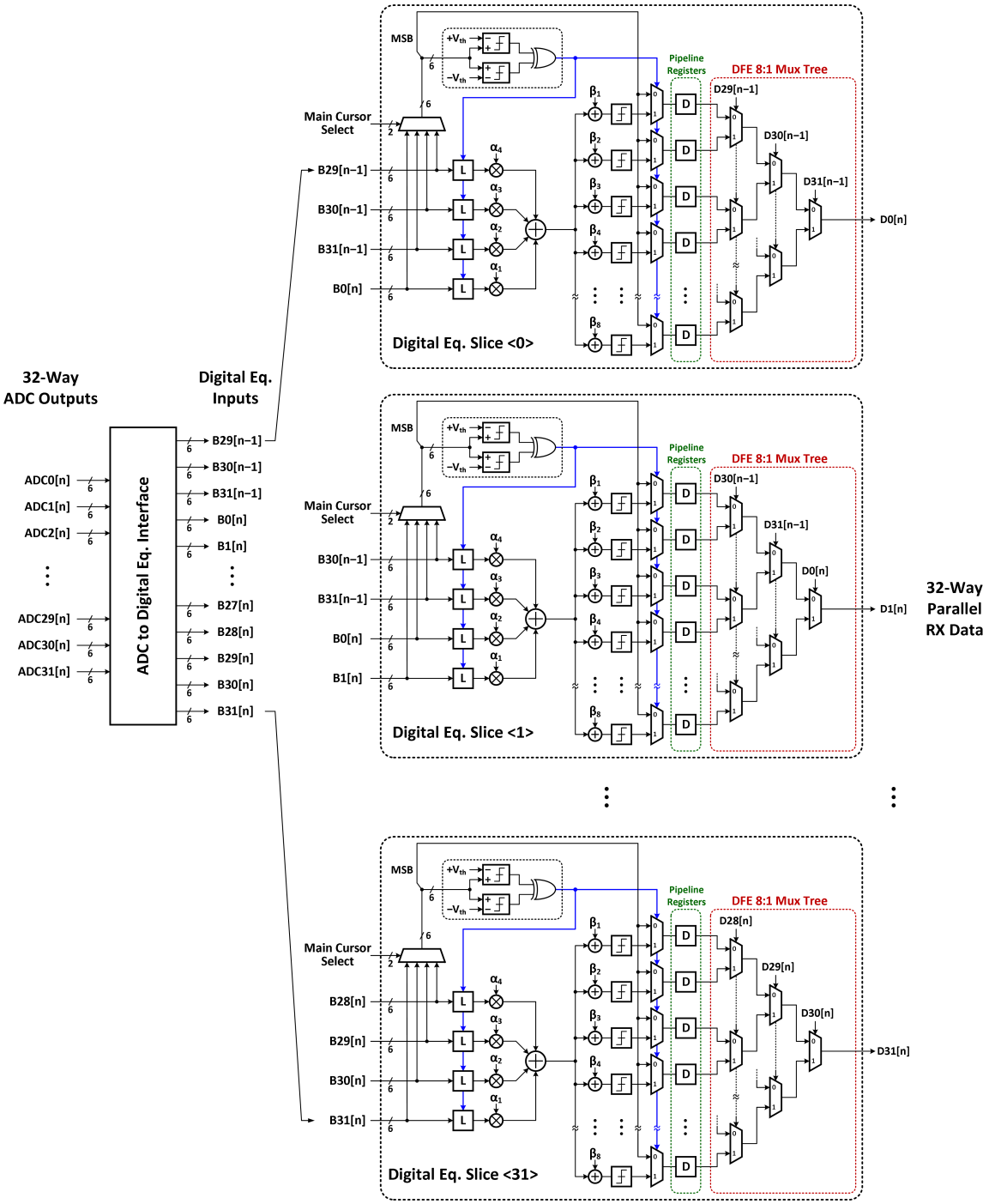


Figure 4.14: Detailed implementation of the dynamically-enabled 32-way parallel 4-tap FFE and 3-tap loop-unrolled DFE digital equalizer.

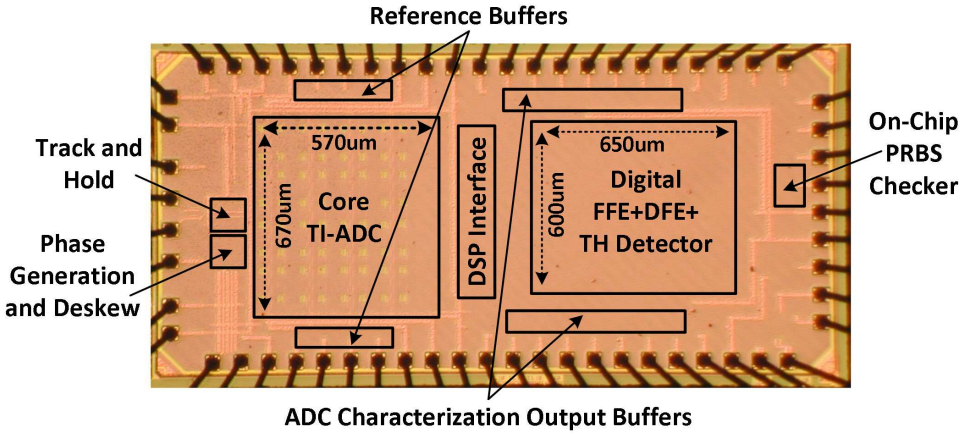


Figure 4.15: Prototype ADC-based receiver chip microphotograph.

4.4 Experimental Results

Fig. 4.15 shows the chip micrograph of the proposed hybrid ADC-based receiver prototype, which was fabricated in a GP 65nm CMOS process. The core 6-bit time-interleaved asynchronous SAR ADC occupies 0.38mm2. In order to minimize parasitic capacitance and routing of the critical sampling phases, the eight front-end T/Hs are placed close to both the input pads and the clock phase generator. An on-die transmission line structure is utilized to route the 5GHz differential clock from its input pads to the phase generator. In order to improve the symmetry among the unit ADCs, the on-die global reference buffers are split equally on the top and bottom of the core ADC layout. High-speed output buffers are also included that tap off the signals before the digital equalizer in order to allow for ADC characterization. The digital equalizer occupies 0.39 mm2, with other circuitry, such as the T/Hs, clock phase generation, reference buffers, and interface re-timing blocks bringing the total area to 0.81mm2.

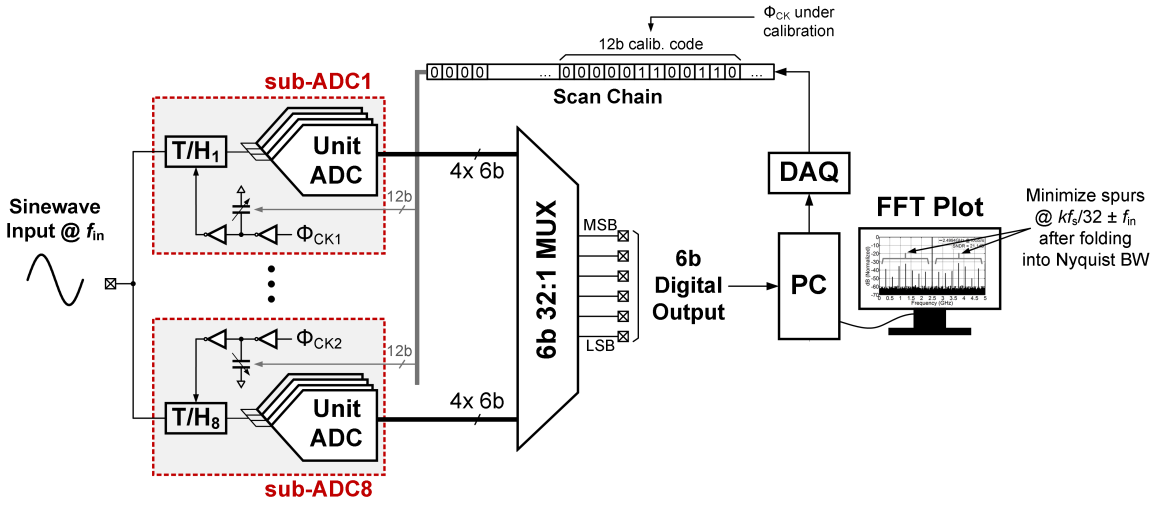


Figure 4.16: Simplified diagram of foreground clock skew calibration setup.

4.4.1 ADC Characterization

In order to calibrate the phase mismatches between the eight critical T/H sampling phases, an FFT-based foreground calibration method is used, as shown in Fig. 4.16. The FFT of the measured ADC output is calculated using a sine wave input with known frequency fin. Spurs that occur at kfs/8 fin, which correspond to the phase mismatches between the eight T/H stages, are minimized by tuning the digitally controlled MOS capacitors of the clock distribution delay lines using a successive approximation algorithm. The optimal calibration codes result in the best ADC output signal to noise and distortion ratio (SNDR).

The dynamic performance of the 10GS/s time-interleaved ADC is shown in Fig. 4.17. A low frequency SNDR of 30.3dB is achieved, which translates to an effective number of bits (ENOB) of 4.74 bits. The effective resolution bandwidth (ERBW) of the ADC is 4.13GHz, at which the ENOB drops to 4.2 bits. At high frequency, the ENOB is limited by the sampling clock jitter. A low frequency sine wave histogram method [73] is used for calculation of the ADC DNL/INL. Applying a 9.46MHz input

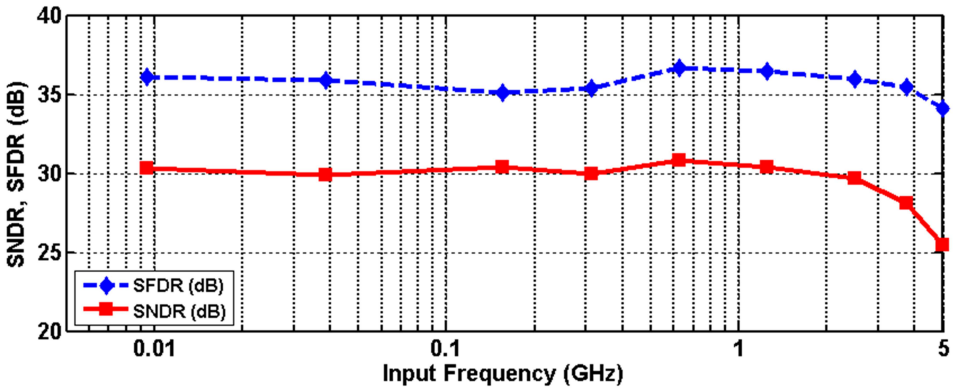


Figure 4.17: ADC SNDR and SFDR vs. input frequency at fs = 10 GHz.

with fs=10GS/s, Fig. 4.18 shows that the maximum DNL/INL values for the ADC are +0.17/-0.17 LSB and +0.51/-0.61 LSB, respectively.

Characterization of the embedded FFE tap range and resolution is performed with a maximum DC input voltage of 0.5V. As an individual FFE tap coefficient is varied, the ADC output is averaged and plotted as a function of the FFE code. Fig. 4.19 shows that since the taps are hard-wired to achieve subtraction, increasing the FFE code causes the ADC output to decrease. Both the FFE pre- and post-cursor taps are able to cover the full range of the ADC input, with a 35 LSB range and a resolution of 1.1LSB.

4.4.2 ADC-Based Receiver Characterization

Fig. 4.20 shows the test setup used to characterize the performance of the hybrid ADC-based receiver. 10Gb/s PRBS data with 1Vppd swing is passed through the four FR4 channels of Fig. 5 using a Centellax PCB12500 transmit module and the receivers digital equalizer output is fed back to the BERT. No transmit equalization is used in this test setup, with the embedded FFE in the ADC and the dynamically-enabled digital equalizer making up all the equalization in the system. The statistical

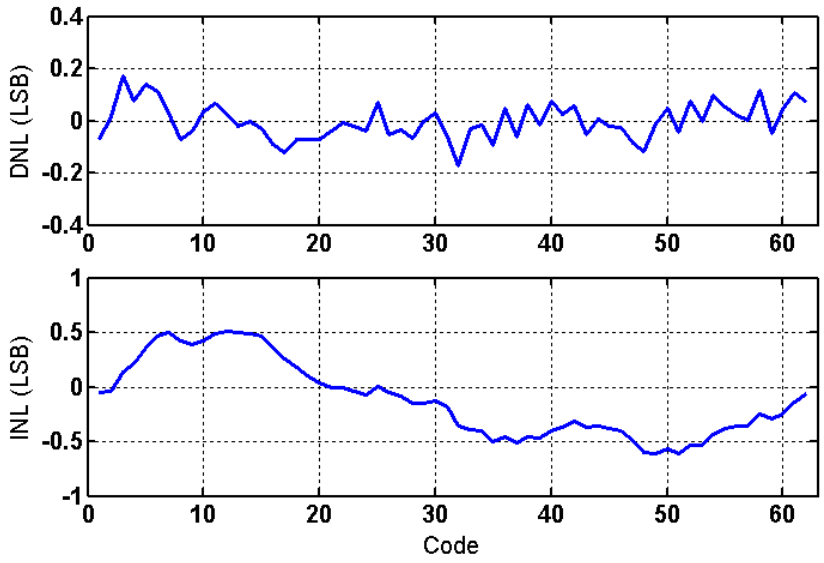


Figure 4.18: DNL/INL plots with fin = 9.46 MHz at fs = 10 GHz.

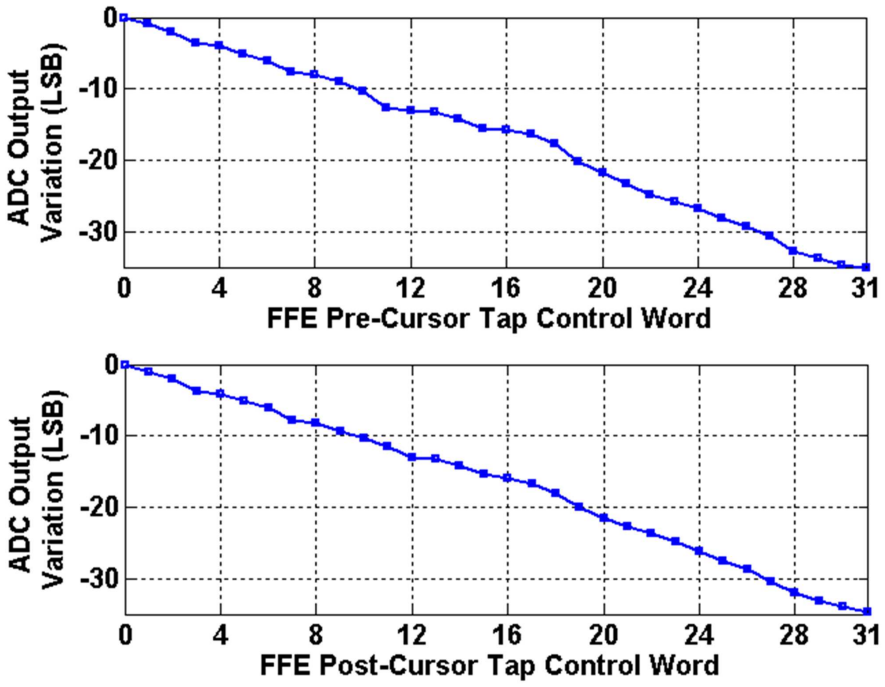


Figure 4.19: Measured tap coefficient range and resolution using DC input voltages for embedded FFE pre- and post- taps.

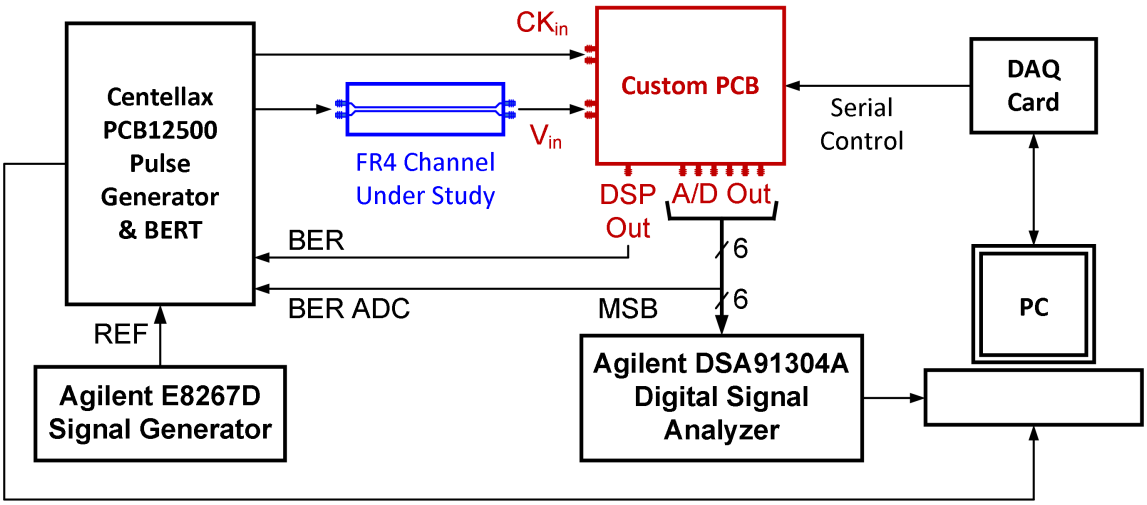


Figure 4.20: ADC-based receiver characterization test setup.

modeling discussed in Section II is used to obtain initial tap coefficients and positions, whose values are subsequently manually adjusted with the digital equalizer always in operation to achieve the lowest BER. By jointly optimizing the embedded and digital taps, the performance impact due to the limited values that can be assigned to the embedded taps is minimized. The optimal threshold for the dynamic enabling of the digital equalization is set manually by first utilizing the maximum threshold with the digital equalizer always in operation. Assuming the target BER is met in this condition, the threshold is reduced to the minimum value that can still achieve the target BER with negligible timing margin impact. While not implemented in this prototype, this procedure could be implemented on-chip as part of a BER-based adaptive equalization algorithm.

Fig. 4.21 shows timing margin bathtub curves for the four FR4 channels with attenuations ranging from 21.0 to 36.4dB at the 5GHz Nyquist frequency, when an additional 1.5dB loss from the receiver board and package is included. First considered is the performance with only embedded ADC equalization activated. For

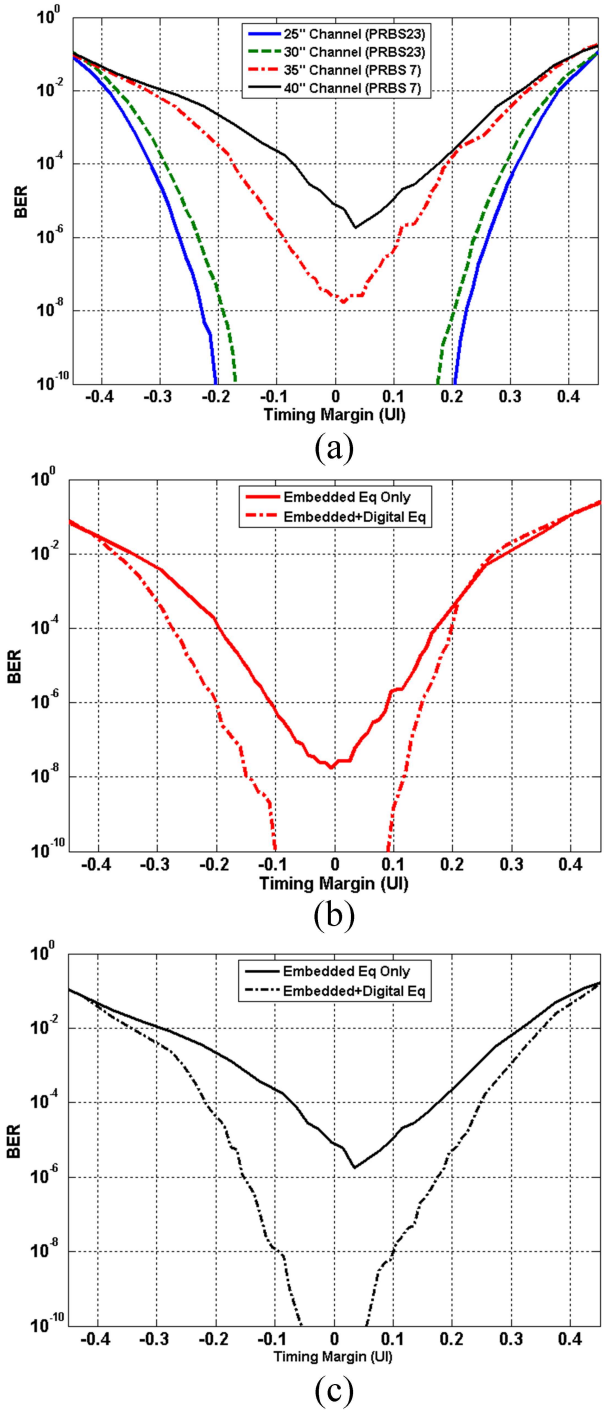


Figure 4.21: Measured bathtub curves for operation over the four Fig. 4.5 FR4 channels with (a) embedded equalization only, and collaborative use of the embedded and digital equalizers for (b) the 35 channel and (c) the 40 channel.

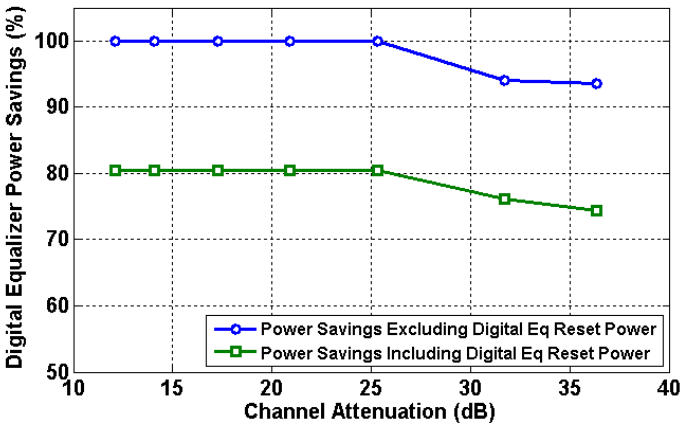


Figure 4.22: Measured digital equalization power savings versus channel attenuation.

this case, open eyes with timing margins exceeding 0.3UI are observed for the two lowest-loss channels with a PRBS23 data pattern. However, the two highest-loss channels require collaborative use of both the embedded and digital equalizers in order to obtain an open eye. When the digital equalizer is dynamically enabled on a per-symbol basis, timing margins of 0.2UI and 0.1UI are obtained for the 31.7dB and 36.4dB channels, respectively, at a $BER < 10^{-10}$ with a PRBS7 data pattern. For these high-loss channels, system performance is primarily limited by ADC quantization noise and non-linearity. As test equipment limitations limit efficient measurements at a lower BER, a Gaussian tail extrapolation is utilized to estimate the $BER = 10^{-12}$ timing margin at 0.37UI, 0.29UI, 0.1UI, and 0.025UI for the 25, 30, 35, and 40 channels, respectively.

Fig. 4.22 shows how digital equalizer power is saved with the hybrid-ADC receiver architecture for seven FR4 channels with attenuation ranging from 11.5dB to 36.4dB. The embedded equalizer alone opens the eye for channels with up to 25dB attenuation, translating into the digital equalizer being disabled 100% of the time and ideally all the digital equalizer power saved. Considering the disabled power

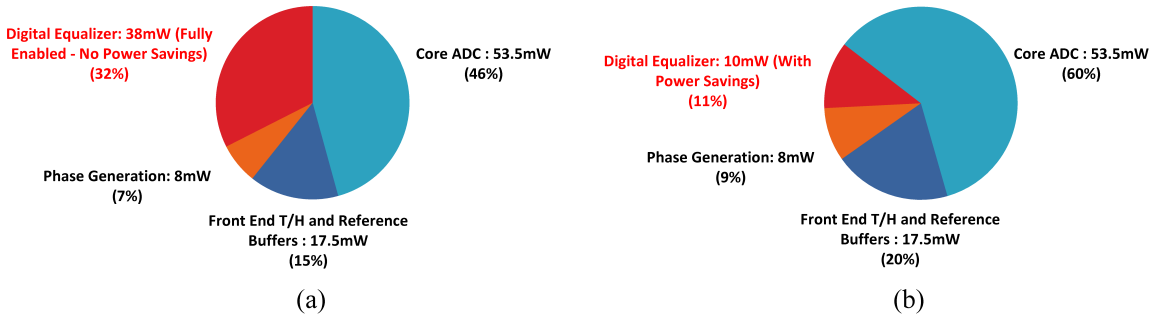


Figure 4.23: ADC-based receiver power breakdown for operation over the 36.4dB channel: (a) without per-symbol dynamic enabling and (b) with per-symbol dynamic enabling of the digital equalizer.

overhead due to the enable latches (0.5%), threshold detector (87.5%), and leakage currents (12%), this maps to a measured 80% digital equalizer power savings. For higher attenuation channels when the digital equalizer is being enabled on a per-symbol basis, the hybrid architecture achieves digital equalizer power savings of around 75% for up to 36.4dB channel attenuation.

Fig. 4.23 shows the power breakdown of the proposed receiver operating with the highest 36.4dB loss channel, both with and without dynamic enabling of the digital equalizer. The core ADC, T/Hs, and clock phase generation dissipate 79mW of power, while the digital equalizer consumes 38mW, out of which 28mW can be saved by the per-symbol dynamic-enabling. This power savings grows to more than 30mW for the lower loss channels. Considering the T/H power overhead due to the additional embedded FFE routing capacitance, which translates to around 10mW, an overall power savings of more than 20mW is achieved. Table 4.1 compares this work with other ADC-based receivers near 10Gb/s [2, 5, 58]. The presented receiver is able to support operation over the highest loss channel among these designs, while also providing significant power savings in the digital equalizer.

Table 4.1: Proposed 10Gb/s ADC-Based Receiver Performance Comparison

Specification	Harwood'07 [2]	Chen'12 [5]	Zhang'13 [4]	This Work [20]	
CMOS Technology	65-nm	65-nm	40-nm	65-nm	
Supply Voltage (V)	N/A	1.1	N/A	1.0	
ADC Structure	Flash	Variable VREF Flash	Rectifier Flash	TI Async. SAR	
Pre–Equalization	4-Tap FIR @ TX	HPF + 2-Tap FFE	N/A	Embedded 3-Tap FFE	
Post–Equalization	2-Tap FFE + 5-Tap DFE	5-Tap DFE	Adaptive FFE + DFE	4-Tap FFE + 3-Tap DFE	
Input Range (V_{pp})	N/A	0.6	N/A	1.0	
Resolution (bit)	4.5	4	6	6	
Sampling Rate (GS/s)	12.5	10	8.5–11.5	10	
Max ENOB (bit)	N/A	N/A	4.86	4.75	
Area (mm^2)	0.45	0.29	0.82	0.81	
Compensated Channel Loss	-24dB @ 12.5Gb/s	-29dB @ 10Gb/s	-34dB @ 10.3Gb/s	-25.3dB @ 10Gb/s	-36.4dB @ 10Gb/s
ADC Power (mW)	150	93	195	79	
DSP Power (mW)	85	37	N/A	8	10
Energy Efficiency (pJ/bit)	30.7	13	19	8.7	8.9

5. CONCLUSION AND FUTURE WORK

5.1 Conclusion

ADC-based receivers are increasingly being considered for high performance wire-line receivers, due to their ability to implement complex and flexible digital equalization relative to mixed-signal receivers. One key issue with ADC-based receivers, however, is the significant power consumption of both the front-end ADC and the subsequent digital equalization and symbol detection at high data rates. Embedding analog equalization in the ADC is a promising approach to both reduce ADC resolution and digital equalization complexity, allowing for improvements in overall receiver power consumption with low-overhead implementations of the common feed-forward equalizer (FFE) and decision-feedback equalizer (DFE) topologies used in wire-line receivers.

This research has presented a modeling framework that enables accurate and efficient simulation of ADC-based receiver architectures. A new 10Gb/s hybrid ADC-based receiver architecture have been proposed. Utilizing a simple digital threshold detector that monitors the ADC output allows for the detection of reliable symbols and the ability to dynamically enable the digital equalizer on a per-symbol basis. For a given channel loss, the probability of reliable symbols is dramatically enhanced by employing a low-overhead 3-tap FFE in the asynchronous SAR ADC. Measurements results of a 65nm receiver prototype verify that for channels with near 25dB the embedded FFE allows for close to 100% deactivation of the digital equalizer, while for higher-loss channels the per-symbol dynamic enabling technique offers close to 75% digital equalizer power savings. Overall, this proposed hybrid ADC-based architecture provides a single receiver design which has the flexibility to efficiently support

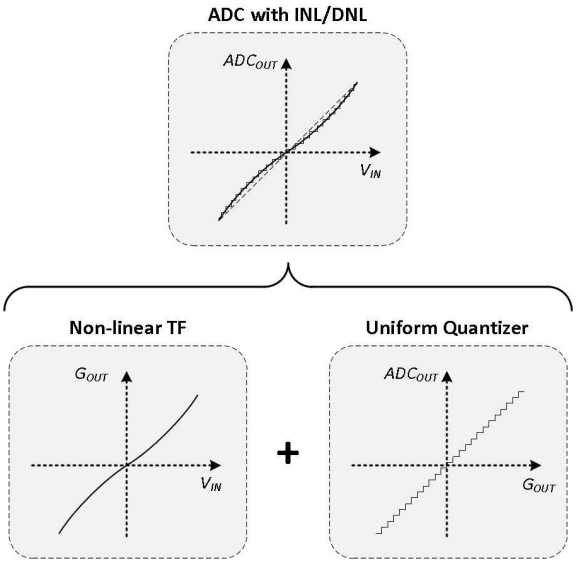


Figure 5.1: Decomposition of INL error into linearity + quantization errors

a wide range of channels with varying amounts of ISI.

5.2 Recommendations for Future Work

While the model presented in this research is able to capture the effect of INL with the help of transient-extracted quantization error PDF, it would be more efficient to estimate the quantization noise PDF without the need for any time-consuming transient simulations. One idea to consider is to separate the INL effect on quantization into a linearity error plus quantization error, as shown in Fig. 5.1.

By decomposing the quantizer with INL into a non-linear transfer function followed by an ideal quantizer, the quantization error may be written as:

$$\nu_{INL} = \nu_Q + \Delta(V_{in}) \tag{5.1}$$

Where ν_{INL} is the quantization error including INL effect, ν_Q is the quantization noise of the ideal quantizer and $\Delta(V_{in})$ is the error added to the input due to the

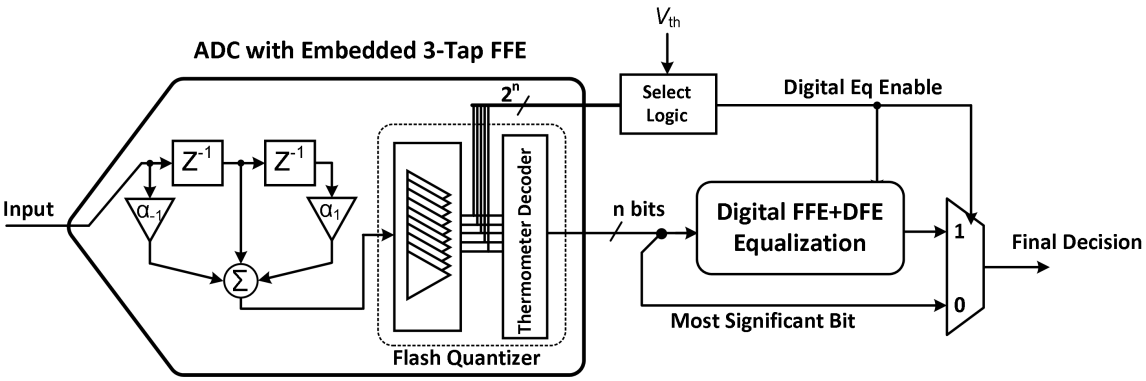


Figure 5.2: Block diagram of hybrid-ADC based receiver with inherent threshold detection using Flash ADC

non-linear function. Using approaches similar to [74, 75], it is possible to find the error due to the non-linear transfer function, and the questions remains whether or not the effect of the digital FFE on this error may be efficiently calculated.

5.2.1 Hybrid ADC-based Receiver with Flash ADC Implementation

In regards to the hybrid ADC-based receiver architecture, one interesting implementation that is worth investigation is to take benefit of the thermometer levels at the Flash ADC output to implement the threshold detection functionality. By leveraging the already available threshold levels, simple logic may be used to realize a threshold detector, which may be used to dynamically enable the following digital equalization, similar to the work presented. A block diagram of this implementation is shown in Fig 5.2.

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