A LOW JITTER WIDEBAND FRACTIONAL-N SUBSAMPLING PHASE LOCKED LOOP (SSPLL)

A Thesis

by

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ABSTRACT

Frequency synthesizers have become a crucial building block in the evolution of modern communication systems and consumer electronics. The spectral purity performance of frequency synthesizers limits the achievable data-rate and presents a noise-power tradeoff. For communication standards such as LTE where the channel spacing is a few kHz, the synthesizers must provide high frequencies with sufficiently wide frequency tuning range and fine frequency resolutions. Such stringent performance must be met with a limited power and small chip area.

In this thesis a wideband fractional-N frequency synthesizer based on a subsampling phase locked loop (SSPLL) is presented. The proposed synthesizer which has a frequency resolution less than 100Hz employs a digital fractional controller (DFC) and a 10-bit digital-to-time converter (DTC) to delay the rising edges of the reference clock to achieve fractional phase lock. For fast convergence of the delay calibration, a novel two-step delay correlation loop (DCL) is employed. Furthermore, to provide optimum settling and jitter performance, the loop transfer characteristics during frequency acquisition and phase-lock are decoupled using a dual input loop filter (DILF).

The fractional-N sub-sampling PLL (FNSSPLL) is implemented in a TSMC 40nm CMOS technology and occupies a total active area of 0.41mm^2. The PLL operates over frequency range of 2.8 GHz to 4.3 GHz (42% tuning range) while consuming 9.18mW from a 1.1V supply. The integrated jitter performance is better than 390 fs across all fractional frequency channel. The worst case fractional spur of -48.3 dBc occurs at a 650

kHz offset for a 3.75GHz fractional channel. The in-band phase noise measured at a 200 kHz offset is -112.5 dBc/Hz.

DEDICATION

To my mother and sister…….

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TABLE OF CONTENTS

Page

LIST OF FIGURES

LIST OF TABLES

Page

1. INTRODUCTION

Recent advancements in modern electronics and communication systems have pushed the demand for higher data rates and stringent signal-to-noise ratio (SNR) specifications. Whether for multi-standard radio frequency transceivers or high throughput digital signal processors (DSPs), the integrated circuits (ICs) that make up such systems must meet stringent performance requirements with limited power and small chip area.

Frequency synthesizers serve as crucial building blocks in integrated circuits by providing periodic clock signals required to perform various functions including: defining the sampling instance of analog-to-digital converters (ADC) or digital-to-analog data converters (DAC); translating wanted signals (up conversion and down conversion) in wireless transceivers; synchronizing data flow in wireline and optical serial data communication lines as well as coordinating the operation of digital circuitry in digital ICs. Figure 1.1 shows the block diagram for a generic transceiver where a frequency synthesizer is used as local oscillator (LO) to provide the needed frequency translation when receiving (down conversion) or transmitting (up conversion). In order to achieve increased processing power and data bandwidth most modern communication systems are operated in the multi-gigahertz range. Furthermore, the portable electronics industry has pushed the need for multi-standard transceivers and as such the synthesized frequencies must have a sufficiently wide tuning range to cover the various frequency bands and also compensate for process variation.

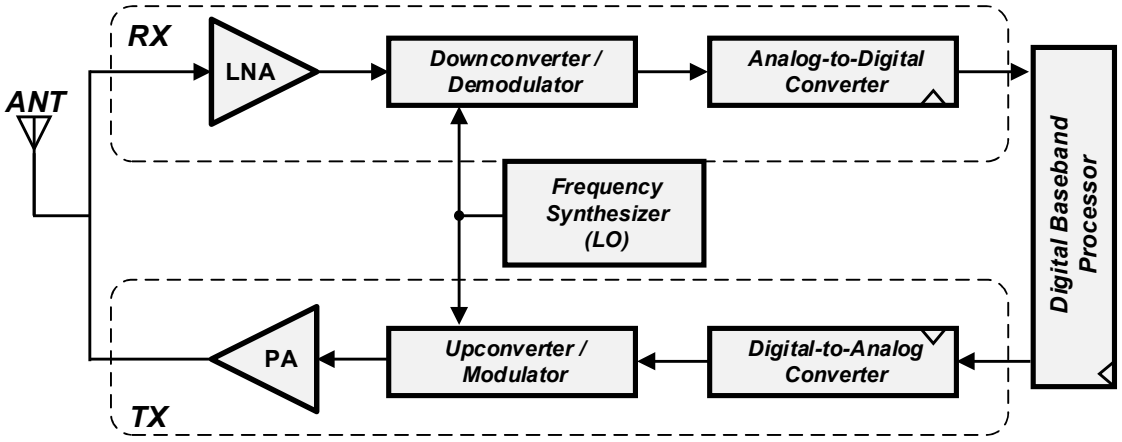


Figure 1.1 A generic RF transceiver block diagram

The narrow channel spacing in modern communication standards means that the LO frequency synthesizer must have fine frequency resolution.

Over the years various frequency synthesizer based on direct analog synthesis (DAS), direct digital synthesis (DDS) and indirect or phase locked loop (PLL) based synthesis have been proposed [1, 2]. Due to their low power consumption and smaller chip area, PLL based frequency synthesizers have achieved much prominence and have been shown to be well suited to RF application.

1.1 Spectral Purity of Clock Signals

Ideally the LO signal in the transceiver chain must be stable and clean exhibiting an ideal tone in its frequency spectrum. However in practical frequency synthesizers, intrinsic noise from devices and noise from the surrounding environment generates

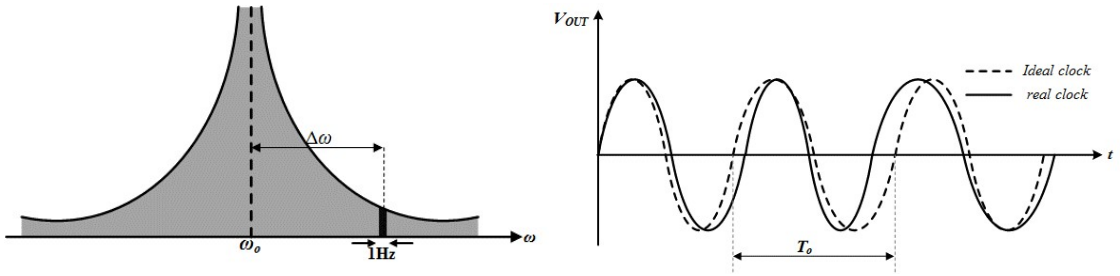


Figure 1.2 Representation of phase noise in an oscillator in (a) frequency and (b) time (jitter)

fluctuations on the phase and amplitude of the clock signal. This results in spectral components at frequencies other than the desired frequency. Typically the effect of the amplitude noise is trivial since it is relatively constant over time and can be easily removed with a limiter circuit [1] . Considering only the deviations in the phase, the output signal of an oscillator is:

$$V_{out}(t) = A\cos\big(\omega_0 t + \phi(t)\big) \tag{1.1}$$

where $\phi(t)$ represents the small random deviations in the phase of the of the signal and is commonly termed as "phase noise". Usually $|\phi(t)| \ll 1\ rad$ and hence

$$V_{out}(t) \approx A\cos\omega_0 t - A\phi(t)\sin\omega_0 t \tag{1.2}$$

Equation (1.2) reveals that the spectrum of $\phi(t)$ is translated to $\pm\omega_0$. Figure 1.2 shows the effect of phase noise on the clock signal in the frequency and time domain.

1.1.1 Phase noise

To quantify the phase noise, the notation $\mathcal{L}\{\Delta\omega\}$ is used to represent the single side band phase noise (within a 1-Hz unit bandwidth at a certain offset $\Delta\omega$ away from the carrier frequency) to carrier ratio (SSCR) expressed in dBc/Hz as :

$$\mathcal{L}\{\Delta\omega\} = 10\log\left(\frac{P_{sideband}(\,\omega_0 + \Delta\omega, 1Hz\ bandwidth)}{P_{carrier}}\right)\ [dBc/Hz] \qquad (1.3)$$

Phase noise calculation often require the phase noise power spectral density (PSD) S_ϕ (and its rms value) to be known. In [3] it is shown that the power spectral density of the phase noise spectrum is related to $\mathcal{L}\{\Delta\omega\}$ as follows:

$$S_\phi(\Delta\omega) = 2 \times 10^{\mathcal{L}\{\Delta\omega\}/10}\ [rad^2/Hz] \qquad (1.4)$$

and hence

$$\mathcal{L}\{\Delta\omega\} = 10\log\left(\frac{S_\phi(\Delta\omega)}{2}\right)\ [dBc/Hz] \qquad (1.5)$$

In wireless applications the phase noise corrupts the desired signal and thus limits both the achievable SNR and data rate. To achieve a required SNR (for a given bit error rate (BER)) in any transceiver design, the phase noise of the LO must satisfy the following condition [2]:

$$\mathcal{L}(\Delta\omega) < S_{RF} - S_{blocker} - 10\log(BW) - SNR \qquad (1.6)$$

where

S_{RF} is the desired RF signal power;

$S_{blocker}$ is the blocking signal power;

BW is the channel bandwidth of the desired RF signal

SNR is the SNR needed to meet the required BER of the communication standard

Apart from the noise sidebands, the output spectrum may also exhibit discrete spurious tones ("spurs"). Generally, these spurs are due to perturbations (due to substrate or supply coupling or signal pick-up) at a fixed frequency or by modulation of the oscillator by deterministic baseband signals [3]. These spurs act as "pirate" LO signals if present in a transceiver and may translate unwanted signals onto the desired signal. The tolerable amplitude of the spurious tones is usually defined by a pre-specified power mask for the particular communication standard.

1.1.2 Timing jitter

In the time domain, the noise related phase/frequency deviations causes uncertainty in the zero-crossing of the clock signal which is characterized as "jitter "or "timing jitter". This uncertainty in the zero crossing of clock signals is a statistically measured metric which exhibits a zero-mean Gaussian distribution. In [4] various time-domain measures of clock jitter are defined. The long-term or absolute jitter $\sigma_{\Delta T}$ of an oscillator is characterized by the sequence:

$$\sigma_{\Delta T} = \sum_{n=1}^{N} (t_n - T_o) \ [s] \tag{1.7}$$

where t_n is the period of the oscillator output at the nth cycle and T_o is the nominal oscillator period. Absolute jitter is the most suited to measure the jitter performance of oscillators and has been shown to limit the resolution of ADCs even if the quantizer is

perfect [4]. Figure 1.3 shows the achievable ADC SNR and the corresponding effective number of bits for different input signal frequency limited by a certain amount of sampling clock jitter.

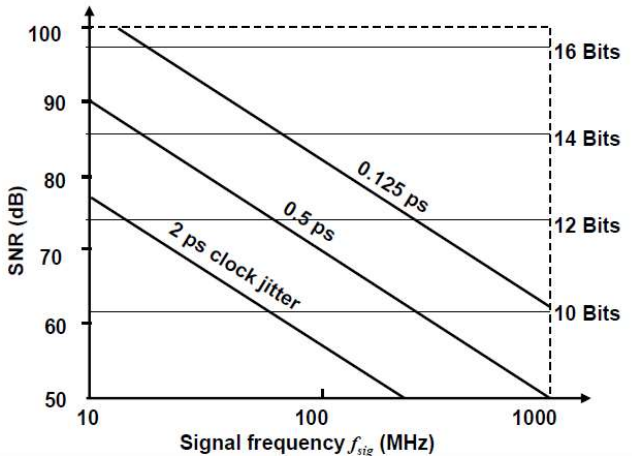


Figure 1.3 Achievable ADC SNR with signal frequency and sampling clock jitter [5]

High-frequency synchronous systems also require minimum clock fluctuations to prevent race conditions, shorten setup and hold time requirements and to maximize possible operating speed of clocked systems.

Phase noise and jitter are closely related and mathematical expressions linking the two quantities is analyzed in [4].

$$\sigma_{\Delta T}^2 = \frac{1}{(2\pi f_{out})^2} \int_0^\infty S_\phi(f)\, df \;\; [s^2] \tag{1.8}$$

The focus of this research is to develop a fully integrated low phase noise (less than -100dBc within the bandwidth of the PLL) low jitter PLL (in order of 100fs') covering a wideband and consuming low power. The research focuses on clock generation for high throughput applications like LTE-Advanced communication system and high performance ADCs and DACS which are perfect candidates for low jitter fractional-N frequency synthesizers.

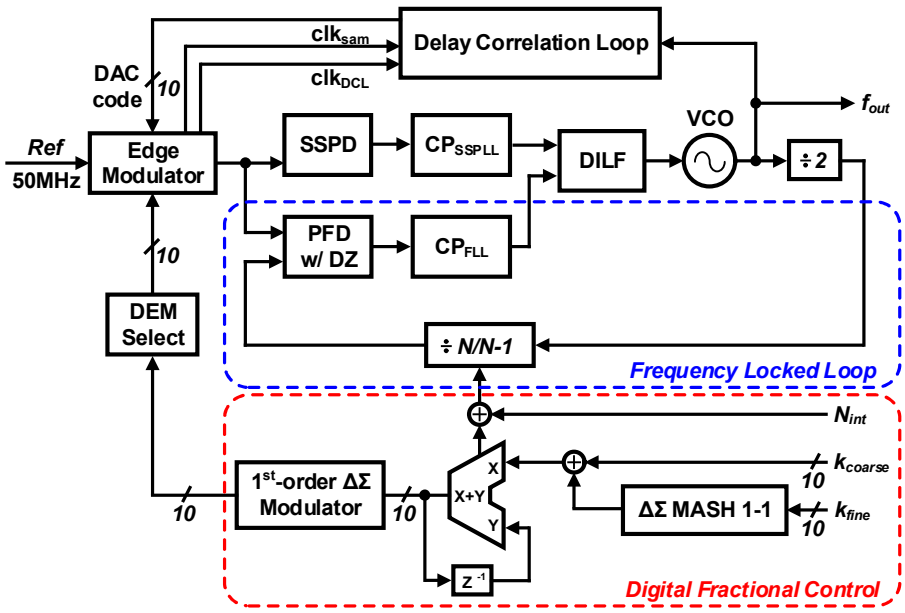


Figure 1.4 Proposed architecture for the fractional-N subsampling PLL

The presented low noise prototype PLL synthesizer is based on a subsampling PLL architecture [6] which has recently received much attention. The proposed architecture for

the PLL is shown in Figure 1.4. The PLL consists of the main subsampling loop which is assisted by an edge modulator block to help achieve fractional frequency phase lock. The fractional value of the synthesizer is provided using a simple digital fractional controller (DFC). A delay correlation loop is also employed to compensate for the non-ideal characteristics of the edge modulator block. A frequency locked loop (FLL) is used to prevent the false locking of the subsampling PLL.

1.2 Thesis Organization

The thesis is organized as follows:

Section 2 presents an overview of PLL concepts. The section describes the classical charge pump PLL and its phase domain model. The different PLL noise sources and their impact on the output phase noise is presented. The concept of fractional frequency synthesis is introduced and the limitations of the basic fractional topology is examined. A discussion is also presented on the popular fractional-N PLL which employs an oversampling modulator.

In Section 3 the concept of subsampling PLL (SSPLL) is discussed. The phase noise model of the SSPLL and a comparison of the phase noise of the classical PLL and SSPL is presented to show the low noise advantage of the latter architecture. The proposed fractional control of the SSPLL is then discussed. The practical limitations and techniques to mitigate these are also discussed. The section is concluded with a model and noise analysis of the proposed system.

Section 4 details the circuit design and implementation of various sections of the proposed architecture. Measurement results for a test chip designed in 40nm CMOS process are included in this section. A comparison of the fabricated prototype with the state-of-the-art fractional-N PLL is also made

In Section 5, conclusions are made and the nature and scope of future work in this thesis is discussed.

2. PLL OVERVIEW

2.1 Introduction

A Phase Locked Loop (PLL) is a feedback system which synchronizes an output and input signal in frequency as well as in phase. The system is said to be synchronized or in the *locked* state when the phase error between the input and output signal is zero. If the phase error builds up, the control loop regulates the output signal in a direction that reduces the phase error. The PLL was first introduced in the area of coherent communication by de Bellescize in 1932 [7]. Since then the PLL has proven to be a very essential component in modern ICs due to its versatility it has found application in frequency multiplication and clock generation, frequency modulation and demodulation, clock and data recovery, synchronization, skew compensation and spread spectrum signal generation. The PLL has therefore become an essential building block in modern system-on-chip (SoCs) which contain microprocessors, I/O interfaces, memories, power management, and communication systems. The next sub-section introduces some basic concepts of the classical charge pump PLL. This is followed by an analysis of the phase noise performance based on the phase domain model of the PLL. A brief discussion on Fractional-N PLL techniques and a review of the spectral purity performance of Fractional-N PLLs based on ΣΔ MASH modulator is then presented. The total output jitter and jitter optimization methods are discussed

2.2 PLL Basics

While there exists many architectures for PLL-based frequency synthesizers [3, 8-11] , the most widely used is the charge pump PLL (CP-PLL) [12] shown in Figure 2.1. The loop consists of a voltage controlled oscillator (VCO) of gain K_{VCO}[Hz/V], a programmable divider with divider ratio N, a phase/frequency detector (PFD) and a single ended charge pump (CP) with a combined gain of K_{pd} and a low pass filter (LPF) with a trans-impedance $Z_{LF}(s)$.

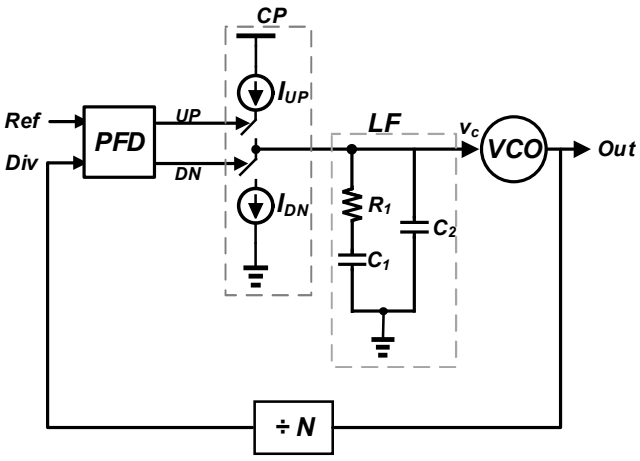


Figure 2.1 Charge pump PLL

The output of the charge pump is proportional to the phase difference between the reference signal and the fed back signal from the divider. Figure 2.2 shows the current-to-

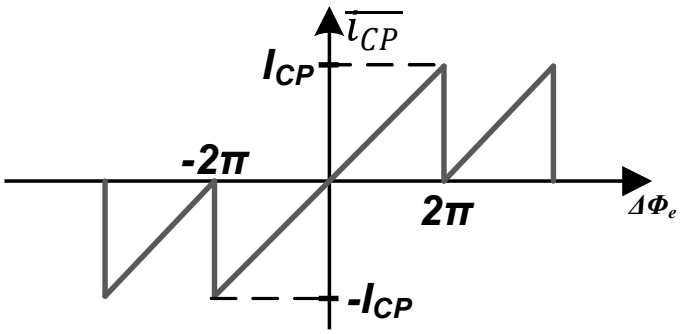


Figure 2.2 PFD/CP characteristics

phase relationship of the PFD and CP. The combined PFD and CP gain is given by the slope of the characteristic between a -2π to 2π:

$$\frac{\overline{i_{CP}}}{\Delta\phi} = \frac{I_{CP}}{2\pi} \tag{2.1}$$

The current from the charge pump consists of the corrective DC signal and an AC component superimposed on it due to the non-ideal characteristics and noise of the various loop components. The loop filter accumulates the DC components and filters out some of the AC components and generates a DC signal with a small superimposed AC signal, v_c which controls the VCO. When the PLL is in lock, the output frequency is related to the reference frequency by $f_{out} = N \cdot f_{Ref}$.

Due to the non-linear nature of the PFD, the PLL is inherently a non-linear feedback system. However, in the locked state, assuming the PFD transfer characteristic is linear about this operating point, the PLL can be modeled as a linear time-invariant (LTI) system [10] as shown in Figure 2.3. The LTI model makes it possible to analyze the

behavior of the PLL using well-defined tools in control system theory. Since LTI system model is for a phase locked loop, the variables of interest are the phases of the signals in the loop.

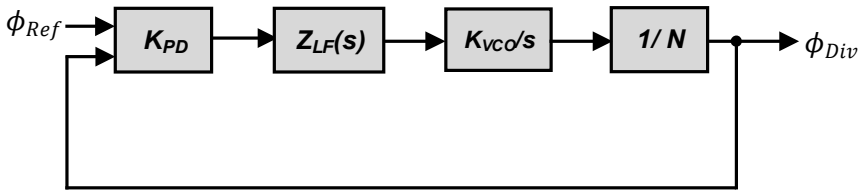


Figure 2.3 Linear model of the charge pump PLL

The open loop transfer function of the system can be expressed as

$$A(s) = K_{pd}\, Z_{LF}(s)\, \frac{K_{VCO}}{s}\, \frac{1}{N} \tag{2.2}$$

The closed loop transfer $G(s) = \phi_{div}/\phi_{Ref}$ is evaluated as

$$G(s) = \frac{A(s)}{1 + A(s)} \tag{2.3}$$

The open loop transfer function determines the static (static phase error, spurious suppression) and dynamic performance (tracking and settling time) of the PLL [10]. In most applications, the PLL is a third-order or higher system as the loop filter contains additional poles necessary to adequately suppress the reference spurious signals [3]. It is thus useful to define an open-loop bandwidth (f_c) and phase margin ϕ_m in order to account for the influence of the higher order poles when analyzing the loop.

The open-loop bandwidth is defined as the frequency at which the magnitude of the open loop response is unity, $|A(j2\pi f_c)| = 1$ and is also referred to as the 0dB crossover frequency. The phase margin is defined as

$$\phi_m = \arg\big(A(j2\pi f_c)\big) + \pi \tag{2.4}$$

In order to suppress the unwanted AC signals on the control voltage, the loop bandwidth must be as narrow as possible. However, a narrow bandwidth affects the dynamic performance such as settling time adversely. The time taken by the loop to settle to the output frequency for a given accuracy ε is related to the open bandwidth as [10]:

$$T_\varepsilon \approx -\frac{\ln \varepsilon}{2\pi f_c} \tag{2.5}$$

Most modern applications require the PLL to acquire lock (settle) in 100's of microseconds or less. Therefore, careful consideration must be given to the loop bandwidth trade-off in practical designs.

2.3 Phase Noise in a Charge Pump PLL

Figure 2.4 shows the linear phase domain model with the noise from the various building blocks modelled as additive (phase) noise sources [13]. The phase noise of the reference, PFD and free-running VCO are represented by $\phi_{n,Ref}$, $\phi_{n,PFD}$ and $\phi_{n,VCO}$ respectively and have units of $[rad/\sqrt{Hz}]$. The noise of the charge pump is modelled as a noise current source $i_{n,CP}$ $[A/\sqrt{Hz}]$, while the equivalent noise of the loop filter is modeled with a noise voltage source $v_{n,LF}$ $[V/\sqrt{Hz}]$. Similarly, the loop divider rms phase noise power density is accounted for by $\phi_{n,DIV}$ $[rad/\sqrt{Hz}]$.

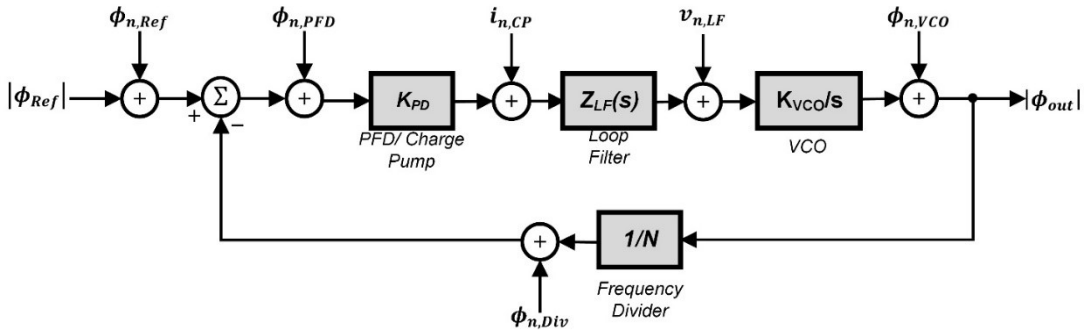


Figure 2.4 Phase domain model of the charge pump PLL with noise sources

The total output phase noise power spectral density (PSD) is a function of two components:

$$S_{\phi,out}(\Delta f) = S_{\phi,in-band}(\Delta f) + S_{\phi,out-band}(\Delta f) \tag{2.6}$$

where the subscripts in-band and out-band have been chosen to reflect the impact of the noise component with respect to the PLL open loop bandwidth f_c.

2.3.1 Phase noise due to loop filter and VCO phase noise

VCO

The phase noise mechanism in VCOs and various noise reduction techniques have received a lot of attention in literature [14-17] . The Leeson–Cutler phase noise model [18] presents a "basic" model and predicts the phase noise behavior of the free running oscillator; the single sideband to carrier ratio (SSCR or $\mathcal{L}$) is

$$\mathcal{L}_{VCO}(\Delta f) = 10\log\left\{\frac{2FkT}{P_{sig}}\left[\left(1+\left(\frac{1}{2Q}\frac{f_o}{\Delta f}\right)^2\right)\left(1+\frac{\Delta f_{1/f^3}}{\Delta f}\right)\right]\right\}[dBc/Hz] \tag{2.7}$$

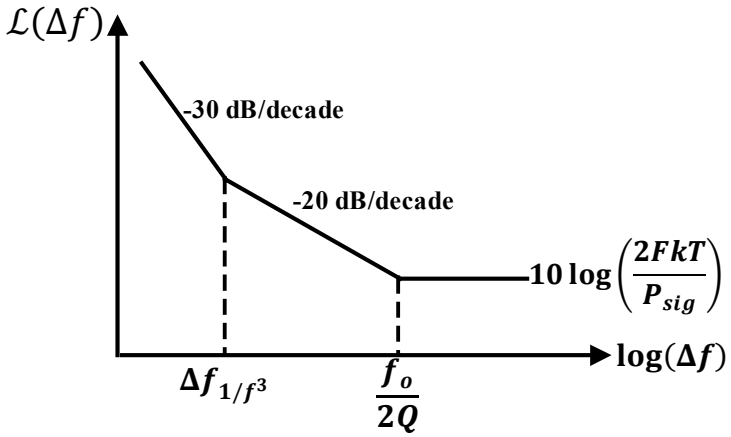


Figure 2.5 Typical phase noise plot of a free running oscillator (Leeson–Cutler model)

where F is an empirical fitting noise factor, k is the Boltzmann constant, T is the absolute temperature, P_{sig} is the power of the oscillator signal, f_o is the oscillation frequency, Q is the loaded quality factor of the tank, Δf is the offset from the carrier and $\Delta f_{1/f^3}$ is the frequency of the corner between the -30dB/decade and -20dB/decade regions in Figure 2.5. A method for calculating $\Delta f_{1/f^3}$ is presented in [15] . It can be deduced from (2.7) that in order to decrease the phase noise power at a given oscillation frequency f_o and offset frequency Δf , the signal power P_{sig} and the quality factor of the tank Q must be maximized while minimizing the noise factor F [3].

Loop filter

The noise power spectral density $S_{\phi,LF}(\Delta f)$ due to $v_{n,LF}$ is [3] :

$$S_{\phi,LF}(\Delta f) = v_{n,LF}^2(\Delta f)\frac{K_{vco}^2}{\Delta f^2}\ [rad^2/Hz] \tag{2.8}$$

The equivalent thermal noise of the loop filter modulates the VCO control voltage.

Effect of the loop

The effect of the feedback loop on the free running VCO phase noise power density $S_{\phi,VCO}(\Delta f)$ and open loop phase noise power density of the loop filter, $S_{\phi,LF}(\Delta f)$ is expressed by the transfer function $H(s) = \phi_{out}/\phi_{n,VCO}$,

$$H(s) = \frac{1}{1 + K_{pd}\, Z_{LF}(s)\, \frac{K_{VCO}}{s}\, \frac{1}{N}} = \frac{1}{1 + A(s)} = 1 - G(s) \tag{2.9}$$

$H(s)$ has a high-pass characteristic whose -3dB cut-off frequency corresponds to the open-loop bandwidth of the PLL, f_c.

$$S_{\phi,out-band}(\Delta f) = |1 - G(j2\pi\Delta f)|^2 \left(S_{\phi,LF}(\Delta f) + S_{\phi,vco}(\Delta f)\right) \tag{2.10}$$

The high-passed noise (out-of-band) noise is typically dominated by the VCO phase as the loop filter noise can be made considerably smaller by minimizing the VCO gain and careful selection of the loop filter components [19].

2.3.2 Phase noise due to reference path, divider, PFD and CP

Reference path, divider and PFD jitter

The circuits of the reference path, divider and PFD are digital in nature and operate at the reference frequency f_{ref}. The switching action of these circuits leads to sampling of the phase of the output signal at a rate of f_{ref}. Due to this sampling process, the noise components at frequencies higher than $f_{ref}/2$ are folded back and thus the phase noise spectrum is defined in the Nyquist band $\left[0 \;\; f_{ref}/2\right]$. Assuming a white noise spectrum, the single-sided phase noise is related to the rms output jitter σ_t as [20, 21]

$$\mathcal{L} = \frac{S_{\phi,n}}{2} = (2\pi\sigma_t)^2 \cdot f_{ref} \ [rad^2/Hz\,] \tag{2.11}$$

Charge pump current source noise

Assuming the current sources of the charge pump are identical ($I_{UP} = I_{DN} = I_{CP}$), the PSD of the thermal noise current of the current sources is

$$S_{n,i} = 2 \times 4kT\gamma \cdot g_{m,CP} = 8kT\gamma \cdot \left(\frac{\alpha I_{cp}}{V_{eff,CP}}\right) [A^2/Hz\,] \tag{2.12}$$

where I_{cp} is the CP current, α is a transistor model parameter , $V_{eff,CP}$ is the effective gate voltage of the transistors in the current source, $g_{m,CP} = \alpha I_{cp}/V_{eff,CP}$ is the equivalent transconductance of the CP current sources, and γ is the noise factor.

When the PLL is locked, the CP is switched on only for a fraction of time τ_{PFD} of the reference period T_{Ref} in order to avoid the dead zone. This leads to under-sampling of the CP current noise resulting in the reduction of the noise contributed by the CP current sources [21]. The output PSD of the sampled CP thermal noise is calculated as [21]

$$S_{i,CP} = S_{n,i} \cdot \frac{\tau_{PFD}}{T_{ref}} \ [A^2/Hz\,] \tag{2.13}$$

Effect of the loop

The phase noise power spectral density of the divider, PD/CP and reference (and its associated buffer noise) referred to the input of the PFD can be expressed as the *detector* noise

$$S_{\phi,detector} = \left(S_{\phi,Ref} + S_{\phi,Div} + S_{\phi,PD} + \frac{S_{i,CP}}{K_{PD}^2}\right) [rad^2/Hz] \tag{2.14}$$

The noise transfer function of the (referred) detector noise to the output of the PLL and the noise PSD due to the detector noise at the output of the PLL can be expressed as ;

$$T_{lp}(s) = N\frac{A(s)}{1+A(s)} = N \cdot [G(s)] \tag{2.15}$$

$$S_{\phi,in-band}(\Delta f) = N^2|G(j2\pi\Delta f)|^2\left(S_{\phi,detector}(\Delta f)\right)[rad^2/Hz] \tag{2.16}$$

From (2.15) and (2.16) the detector noise is low pass filtered (with a corner frequency determined by the PLL bandwidth f_c) to the output of the PLL but is amplified by N^2 due to the loop divider in the feedback. Generally, the phase noise contribution from the reference clock depends on the quality of the crystal available. Thus for the charge pump PLL, the charge pump (CP) and phase detector (PD) can be considered as the dominant source of detector noise.

2.3.3 Total PLL phase noise

The total phase noise power spectral density at the output of the Charge Pump PLL can be found by substituting (2.10) and (2.16) into (2.6) :

$$\begin{aligned} S_{\phi,out}(\Delta f) = {} & N^2 \cdot S_{\phi,detector}(\Delta f)\,|G(j2\pi\Delta f)|^2 \\ & + |1-G(j2\pi\Delta f)|^2\left(S_{\phi,LF}(\Delta f) + S_{\phi,vco}(\Delta f)\right) \end{aligned} \tag{2.17}$$

Figure 2.6 shows the simulated closed loop SSCR, $\mathcal{L}$ of a third order type 2 charge pump PLL. The PLL has open-loop bandwidth $f_c \approx 1\,MHz$. For frequencies $f \ll f_c$ the PLL output spectrum and hence *in-band* phase noise is dominated by the detector noise $S_{\phi,detector}$. For frequencies $f \gg f_c$ the VCO noise dominates as shown in Figure 2.6

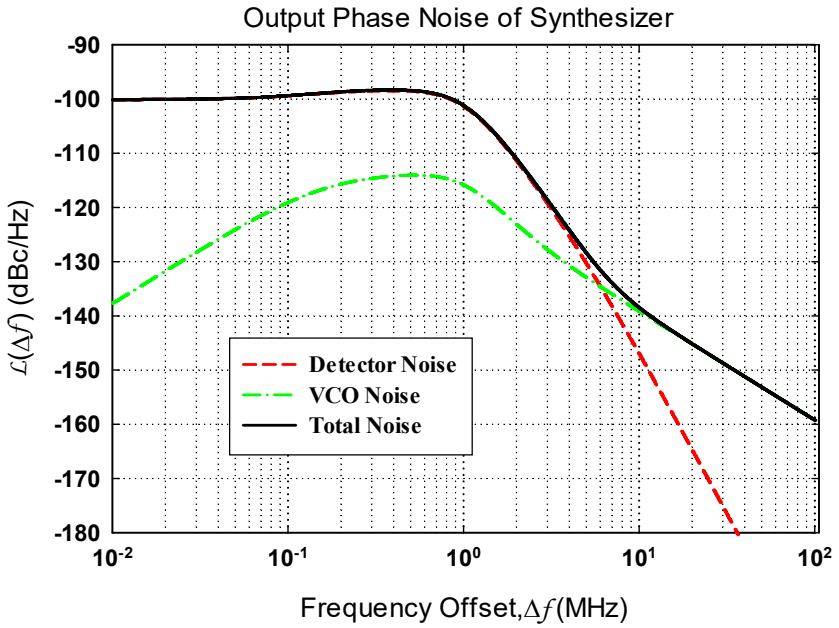


Figure 2.6 Phase noise power density for a classical PLL (1/f noise neglected)

2.4 Reference Spurs

When the PLL is *locked*, the charge pump output current is ideally zero; the VCO control voltage would be a DC signal (the tuned voltage stored in the loop filter capacitor). Practically, the charge pump output current under locked conditions is non zero and contains components at the reference frequency and its harmonics [3]. This error current is fed into the loop filter and consequently causes ripples on the VCO control line which translate to spurious tones at the output of the PLL. These tones occur at the reference frequency and its harmonics away from the output frequency: $f_{out} \pm n.f_{Ref}$. The phenomenon has been studied extensively [3, 11, 22]. Figure 2.7 shows the simulated output spectrum of a CP-PLL; the spectrum shows the reference spurious tones.

While these "reference spurs" are caused by various artefacts in the PLL [22], the two main mechanisms that generate these reference spurious tones are: 1) leakage currents through the charge pump, VCO and loop filter capacitors and 2) mismatch and unequal turn on times of the charge pump up and down current sources [3].

The ripple voltage due to the leakage current is expressed as [3] :

$$V_{ripple,leak}(n.f_{Ref}) = 2I_{leak}\left|Z_{LF}(j2\pi n f_{Ref})\right| \tag{2.18}$$

where I_{leak} is the average leakage current in the loop filter. In modern PLLs the leakage currents are typically small, 1nA or less and thus exhibit a lesser effect, except at low reference frequencies [11]. Similarly the ripple voltage due to the mismatches in the charge pump current sources are [3]:

$$V_{ripple,mismatch}(n.f_{Ref}) = \Delta I_{CP}(n.f_{Ref})\left|Z_{LF}(j2\pi n f_{Ref})\right| \tag{2.19}$$

where ΔI_{CP} is the mismatch current between the up and down current sources. The magnitude of the spurious signal with respect to the carrier is [3]:

$$SP_{fref} = \left[\frac{A_{sp}}{A_{out}}\right]_{dBc} = 20\log\left(\frac{V_{ripple}(n\cdot f_{Ref})\cdot K_{VCO}/2\pi}{2\cdot n\cdot f_{Ref}}\right)\ [dBc] \tag{2.20}$$

where V_{ripple} is the total ripple due to all non-ideal effects.

From (2.18)-(2.19) the relative amplitude of the reference spurs depends on the trans-impedance of the loop filter, the VCO gain and the reference frequency.
Considering the popular second order RC filter shown in Figure 2.1; the trans-impedance of the filter is given as:

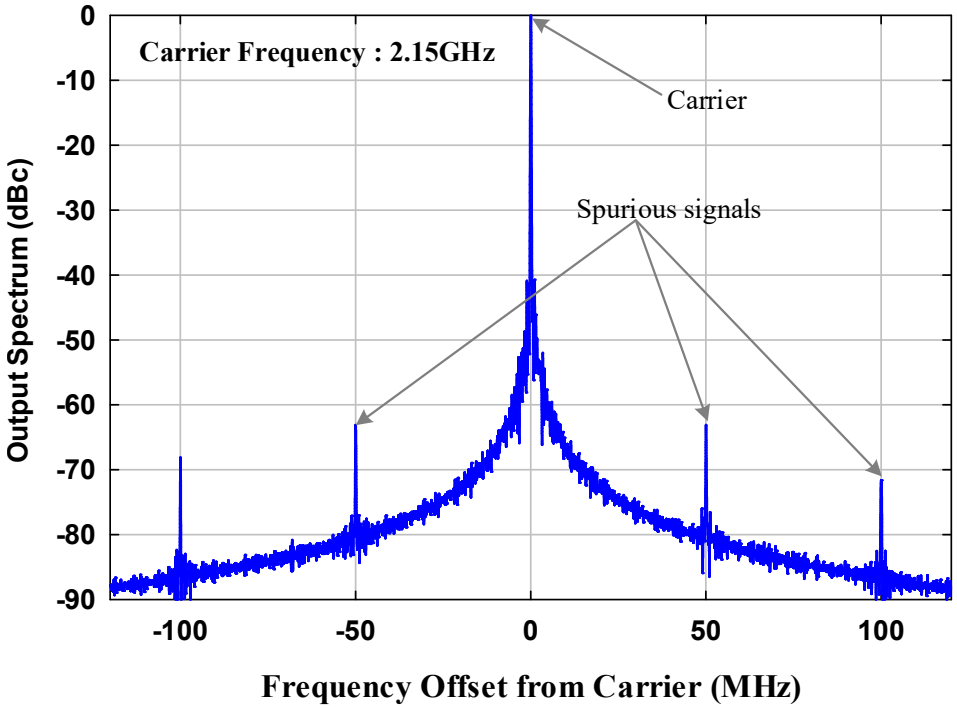


Figure 2.7 Simulated CP-PLL output spectrum (f_{Ref}=50 MHz, N=43)

$$Z_{LF}(s) = \frac{1}{(C_1 + C_2)s} \cdot \frac{1 + R_1 C_1 s}{1 + R_1 \cdot \frac{C_1 C_2}{C_1 + C_2} \cdot s} = \frac{1}{(C_1 + C_2)s} \cdot \frac{1 + s/2\pi f_z}{1 + s/2\pi f_p} \qquad (2.21)$$

where $f_z = 1/2\pi R_1 C_1$ and $f_p = 1/[R_1 \cdot C_1 C_2/(C_1 + C_2)]$ are the FL zero and pole frequency respectively. For most PLL designs $f_z < f_p \ll f_{ref}$ and $C_1 \gg C_2$ and hence

$$SP_{f_{ref}} \propto 20 \log \left[\frac{i_{ripple} \cdot R_1 \cdot K_{VCO}}{4\pi f_{ref}} \right] + 20 \log \frac{f_p}{f_{ref}} \qquad (2.22)$$

The open loop bandwidth of a third order PLL employing the second order RC filter described above is approximately [10] :

$$f_c \approx \frac{\beta \cdot R_1 \cdot K_{VCO}}{2\pi} \tag{2.23}$$

where $\beta = K_{PD}/N$ is the gain from the VCO output to the CP output. From (2.26) and (2.27) the reference spur magnitude

$$SP_{f_{ref}} \propto 20\log\frac{i_{ripple}}{2 \cdot \beta} + 20\log\frac{f_p}{f_c} + 40\log\frac{f_c/f_{ref}}{n} \tag{2.24}$$

Equation (2.28) provides very useful insights to the trade-off that exists for lower reference spur performance. To reduce the spur magnitude the PLL designer can: 1) use a larger β which means a smaller $R_1 \cdot K_{VCO}$ for a desired f_c , however this leads to a reduced VCO tuning range or larger loop filter capacitance; 2)use a smaller f_p/f_c ratio, however this ratio is limited by the phase noise and settling requirements; 3) use a smaller bandwidth to reference frequency ratio f_c/f_{ref} ; 4) use a higher order loop filter however, narrow bandwidths are required in higher order PLLs to ensure stability [10]. Clearly a stringent trade-off exists between low reference spur performance and larger f_c.

2.5 Fractional-N PLLs

In the charge pump PLL synthesizers studied so far, the output frequencies synthesized are limited to integer multiples of the reference frequency f_{Ref} (integer-N PLL) requiring smaller f_{Ref} for finer resolutions. To ensure stability, the loop bandwidth must be at least an order of magnitude less than the reference frequency (leading to large total capacitance in the loop filter) [10, 12]. Furthermore, a smaller loop bandwidth is required to sufficiently suppress spurious signals at the reference frequency. The choice of a smaller reference frequency degrades the PLL dynamic behavior. Also, for smaller

f_{Ref} larger divider values, N are required, which lead to larger in-band phase noise (as evident in (2.16)). Consequently, the design of an integer-N PLL presents a stringent trade-off between frequency resolution, spectral purity and PLL dynamic behavior.

Synthesizers based on Fractional-N techniques [1, 23, 24] enable the PLL to generate frequencies that are fractional multiplies of the reference frequency. This allows for a higher reference frequency to be used for any given frequency resolution allowing the use of larger loop bandwidth without sacrificing the spectral purity perfomance. Further, better PLL dynamic behavior can be achieved and the total capacitance required in the loop filter can be decreased allowing full integration of the PLL. Fractional-N synthesizers have the same basic architecture as that of the classical PLL with the addition of digital circuitry to control the divider value. The achievable frequency resolution is limited by the complexity of the digital circuitry.

2.5.1 The fractional-N principle

The basic fractional-N PLL is shown in Figure 2.8, the division modulus of the loop divider is controlled by the overflow of a digital accumulator of *k*-bit width; the division modulus is set to $N + 1$ whenever the overflow goes high. In order to realize a fractional division ratio $N + n$, with $0 \leq n \leq 1$ the input of the accumulator is set to $K = n \cdot 2^k$. The accumulator produces an overflow K times in every 2^k cycles of f_{Ref}. The divide ratio therefore has an average value:

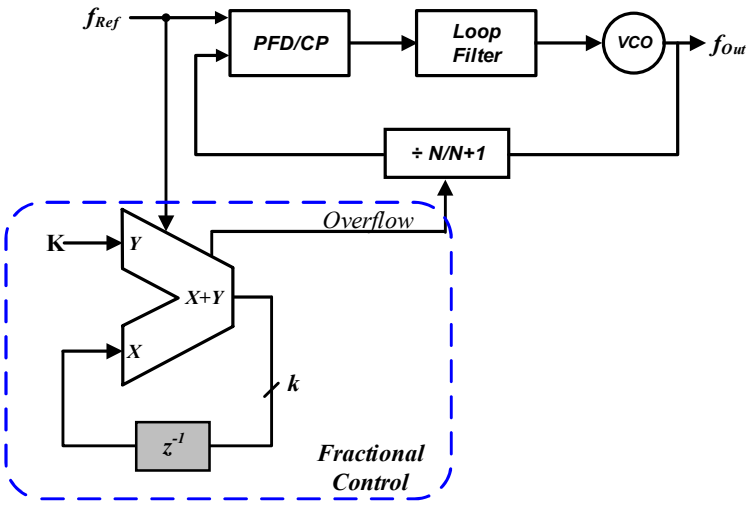


Figure 2.8 Basic fractional-N PLL

$$N_{avg} = \frac{(2^k - K) \cdot N + K \cdot (N+1)}{2^k} = N + \frac{K}{2^k} = N + n \tag{2.25}$$

Figure 2.9 shows the timing sequence of the PD/CP output (and phase error) with the VCO signal and f_{ref} for N=6 and n =3/8. The accumulator value increments to [3, 6, 1(overflow goes high), 4, 7, 2(overflow goes high), 5, 0(overflow goes high)] repeatedly. The overflow goes high 3 times for every 8 cycles of the reference. When dividing by N, the phase error accumulates since the period of the reference signal is larger than the period of the signal at the output of the divider.

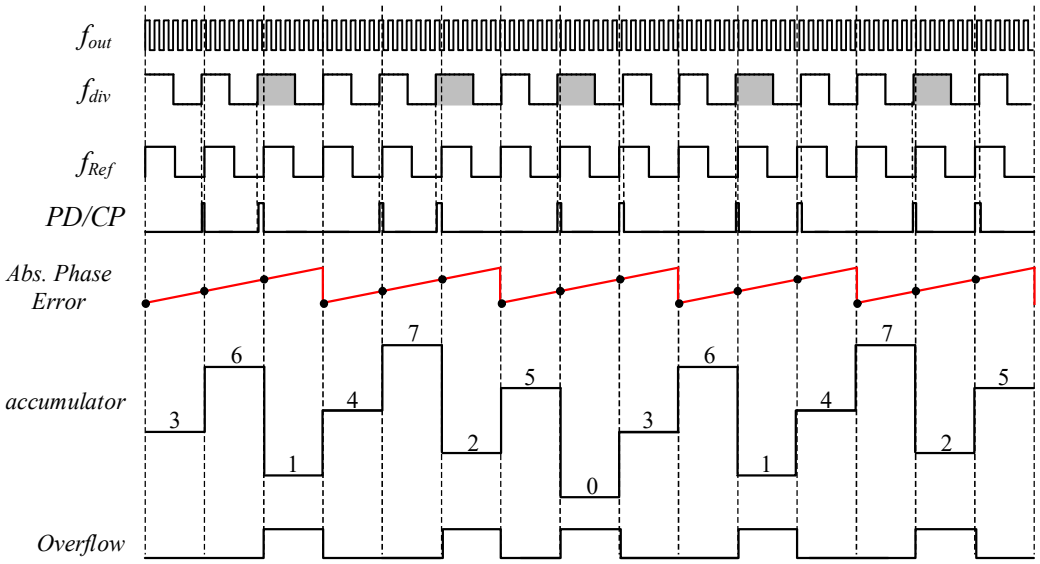


Figure 2.9 Timing sequence for the operation of the basic fractional-N PLL; N=6 and n=3/8=0.375

When the overflow is asserted, the divider divides by $N + 1$ and a VCO cycle is "swallowed". This swallowing of a VCO cycle corresponds to a removal of 2π from the phase error [25]. This results in a periodic absolute phase error, exhibiting a saw-tooth waveform whose fundamental frequency is given by $f_{spur} = n * f_{ref}$.

Figure 2.10 shows the simulated output frequency spectrum for a 10-bit accumulator; the spectrum shows the fractional spurs due to the switch. The periodic error modulates the VCO control voltage and results in undesirable spurious tones in the output of the synthesizer at offsets of f_{spur} and its harmonics degrading the phase noise performance of the PLL as shown in Figure 2.11.

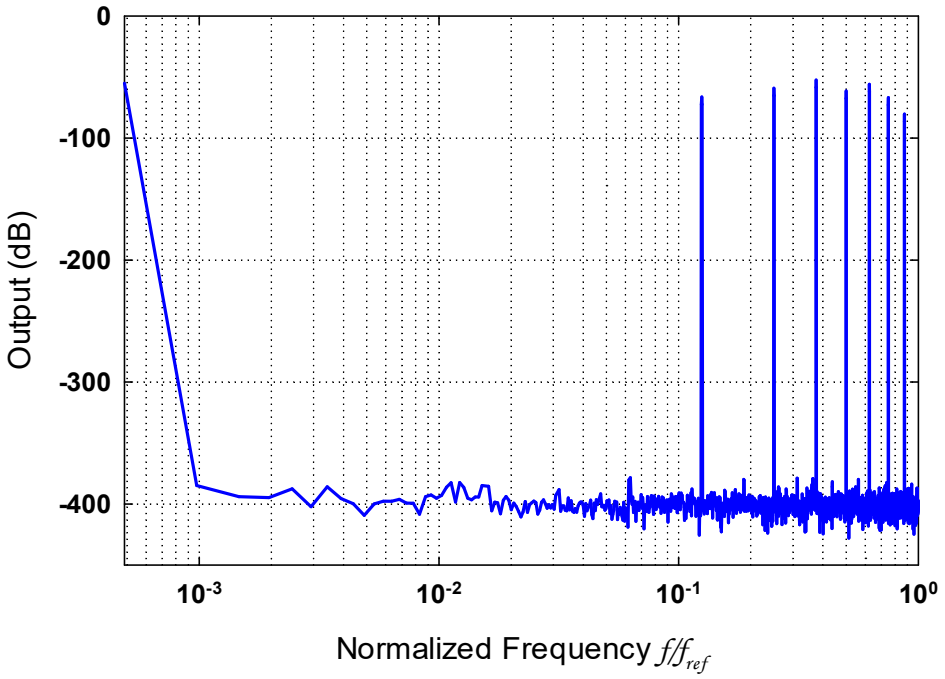
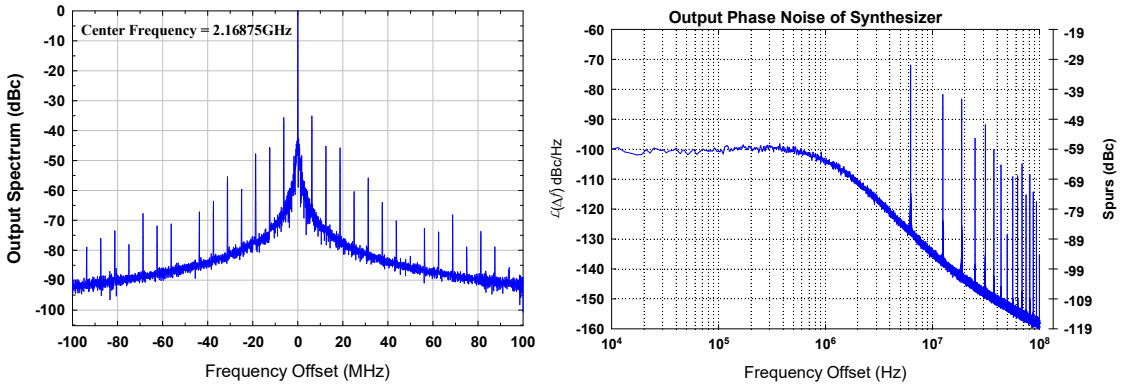


Figure 2.10 Simulated output spectrum of a 10-bit accumulator; f_{Ref} = 50 MHz, N=6 n=3/8 = 0.375

Due to the switching action of the PFD the spurious components at frequencies higher than $f_{ref}/2$ are aliased (folded back) into the Nyquist band$[0\ f_{ref}/2]$. The spur performance of the basic fractional-N PLL worsens for smaller values of n as the spurs may fall within the loop bandwidth and hence will not be attenuated by the loop. Various techniques have been proposed to reduce the problem of fractional spurs and are summarized in Table 2.1.



(a) (b)

Figure 2.11 Effect of fractional spurs on the PLL (a) output spectrum (b) phase noise for $N = 43, n = 3/8 = 0.375$ and f_{Ref} = 50 MHz

Table 2.1 Fractional N spur reduction techniques (reprinted with permission from [26])

Technique	**Feature**	**Problem**
DAC Phase Estimation	Cancels spur by DAC	Analog Mismatch
Wheatley Random Jittering	Randomizes divider	Frequency Jitter
ΣΔ modulation	Modulates divider ratio	Quantization Noise
Phase interpolation	Inherent fractional divider	Interpolation jitter
Pulse generation	Inserts pulses	Interpolation jitter

2.5.2 ΣΔ modulation in fractional-N synthesis

The use of sigma-delta, ΣΔ modulators for spurious suppression in Fractional-N synthesizers has proven to be very attractive due to its oversampling and noise shaping properties. Oversampling and noise shaping techniques have been used extensively in ADCs to shape the spectrum of the quantization noise such that the SNR within the band of interest is improved. Equivalently ΣΔ modulation techniques employed in fractional-N synthesizers (Figure 2.12) are used to shape the phase error spectrum such that the quantization noise is pushed further away from the carrier frequency [25]. Figure 2.12 shows the adaptation of ΣΔ modulators in Fractional-N PLLs.

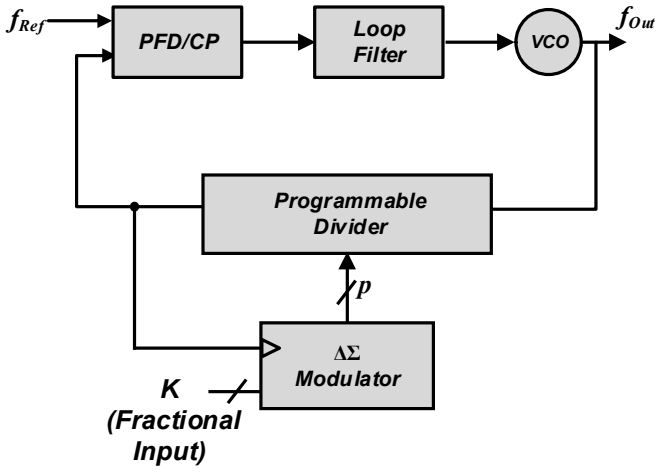


Figure 2.12 ΣΔ Fractional-N Synthesizer

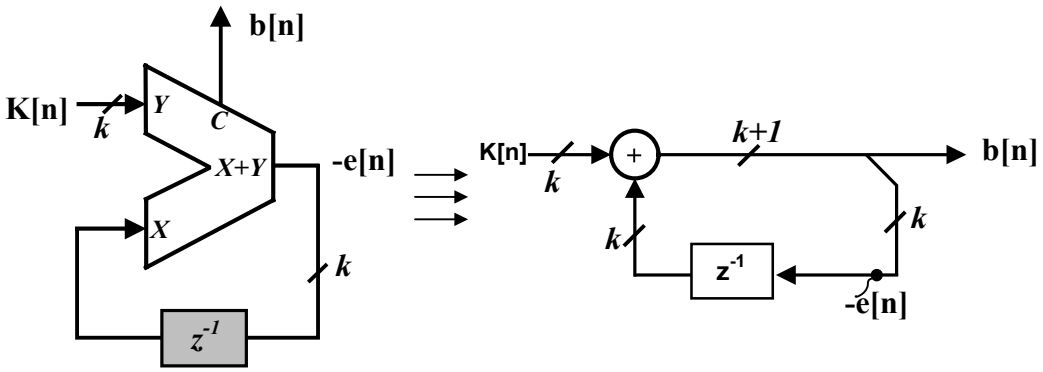


Figure 2.13 Digital implementation of first order modulator and signal-flow graph

The divider value is controlled by a p^{th} order ΣΔ modulator which acts as a coarse quantizer since only integer division values can be realized. The fractional value is achieved by toggling the divider value between two (or more) integer values such that the average value corresponds to the required division ratio.

The accumulator discussed previously is an equivalent digital implementation of a first-order modulator [23, 24]. Figure 2.13 shows the signal flow diagram of the digital accumulator. For each reference cycle the accumulated value is added to the k-bit input signal $K[n]$ producing a value between 0 and 2^{k+1}. The carry output of the accumulator, the MSB of the (k+1)-bit word output, represents a coarse, discrete-time prediction of the accumulator input; the carry output is therefore a single bit quantized version of the accumulator input. This coarse prediction introduces a quantization error which corresponds to the phase error waveform in Figure 2.9. The residual k-bits which is stored

in a *k*-bit register (to be summed with the input at the next clock cycle) represents the negative of the quantization error signal.

The accumulator implementation of the first-order ΣΔ modulator can be modeled by the error-feedback topology [25] shown in Figure 2.14. The accumulator transfer function of is derived as:

$$Y(z) = X(z) + (1 - z^{-1}) \cdot E(z) \tag{2.26}$$

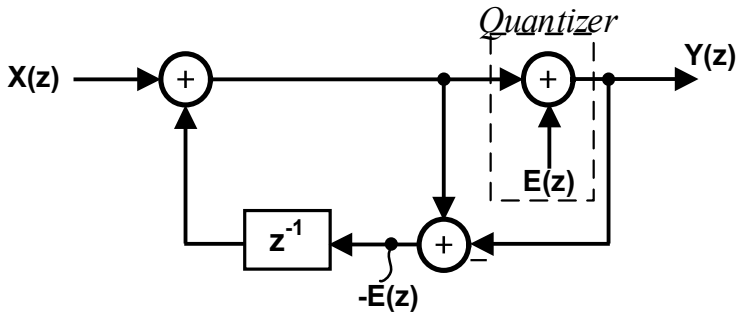


Figure 2.14 Equivalent block diagram of accumulator

From (2.26), the carry output consists of the input in addition to a high-pass "shaped" version of the quantization error, which is the ΣΔ technique [25] . It is well known that first order modulators generate unwanted spurious tones in their output spectrum in response to constant input signals [25] which aligns with the observation made in 2.5.1 (see Figure 2.10 and Figure 2.11). In [23] and [24] it was shown that second order or higher ΣΔ modulators (ideally) do not generate spurious tones when used to randomize

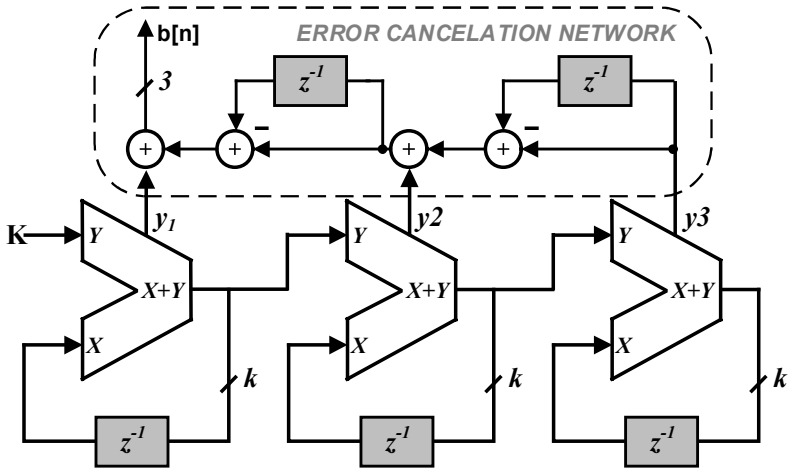


Figure 2.15 3rd Order all-digital ΣΔ MASH Modulator (MASH 1-1-1)

the divider modulus; they effectively shape the quantization noise without causing any spurs. However, this shaped quantization noise presents an extra source of phase noise that must be accounted for in the spectral performance of the PLL. In order to investigate the effect of ΣΔ modulators on the output phase noise of fractional synthesizers, the discussion is based on multi-stage noise shaping (MASH) architectures as such architectures represent an extreme end of the ΣΔ modulator topology spectrum [1].

MASH modulators

MASH modulators have the advantage of being simple to implement with minimum hardware. Figure 2.15 shows the structure of a 3rd order MASH or MASH 1-1-1 modulator which consists of a cascade of digital accumulators and an error cancellation network [25]. The first order accumulator re-quantizes the quantization error from the

previous stage. The error cancellation network sums the filtered versions of the first order accumulator outputs, y_i in such a way that the quantization error from the first two modulators are cancelled. This cancellation is perfect in an all-digital implementation. The output of the modulator in Figure 2.15 is a 3-bit word whose mean value is n. Therefore the divider must switch between 2^3 division ratios centered around the nominal division ratio N. Figure 2.16 shows the division ratio switching due to the MASH 1-1-1; the output is from a simulated system with $f_{Ref} = 50MHz$, *N*=43 *n*=3/8

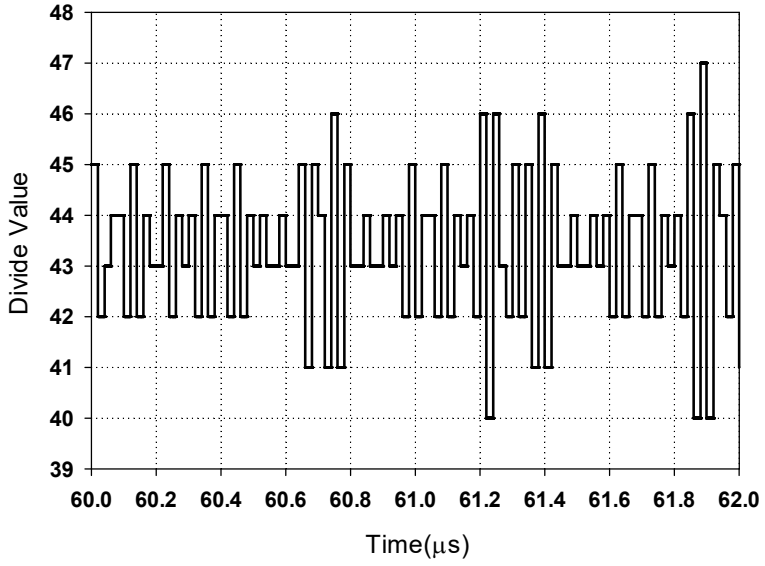


Figure 2.16 3rd Order ΣΔ MASH (MASH 1-1-1) divider value switching (f_{Ref} = 50 MHz $N = 43\ n = 3/8$)

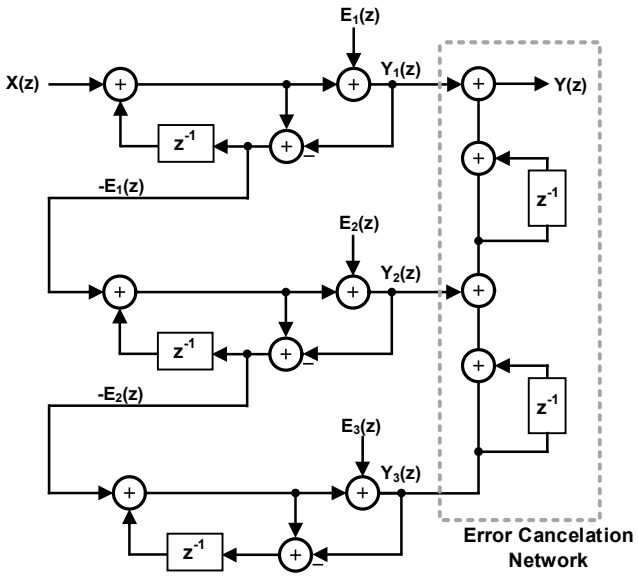


Figure 2.17 Block diagram of the 3rd Order all digital MASH Modulator

The output-input transfer characteristics of the modulator can be derived from its error feedback model which is shown in Figure 2.17. The output of the modulator is:

$$\begin{aligned} Y &= Y_1 + (1 - z)^{-1} \cdot Y_2 + (1 - z^{-1})^2 . Y_3 \\ &= K + (1 - z^{-1})^3 \cdot E_3(z) \end{aligned} \tag{2.27}$$

From (2.27) it is evident that MASH modulator exhibits a first-order nature (the system has no poles) making it unconditionally stable. The intensive switching of divider values at the output of the modulator translates to high frequency ΣΔ quantization noise in the frequency domain. This is evident in the Noise Transfer Function (NTF) of the modulator which can be derived from (2.27). The NTF of the 3rd order MASH modulator is

$$H_{qn}(z) = (1 - z^{-1})^3 \tag{2.28}$$

Similarly the modulator signal transfer function (STF) $H_s(z) = 1$

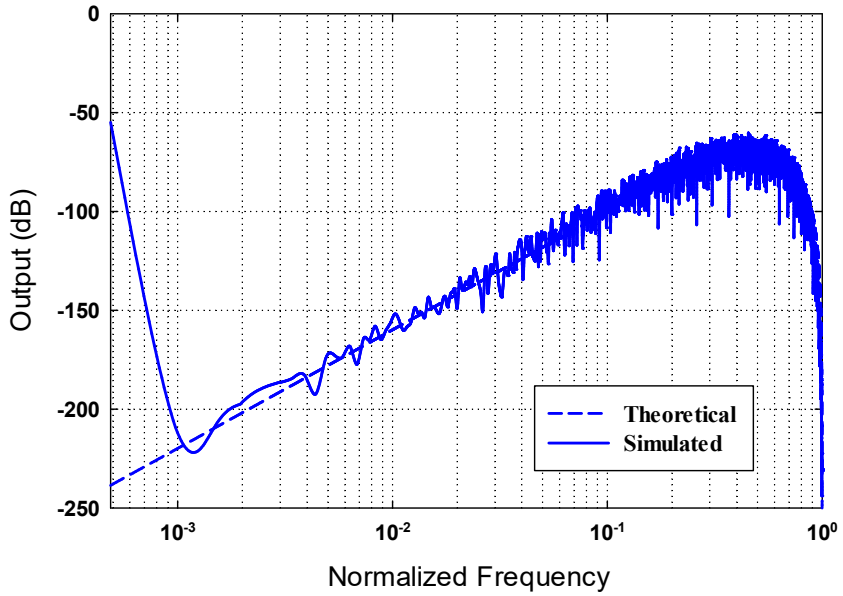


Figure 2.18 PSD of 3rd order MASH modulator output (f_{Ref} = 50 MHz n=3/8)

Figure 2.18 shows the theoretical PSD and the simulated PSD for a 3rd order MASH modulator; the quantization noise is shaped by the high pass NTF. By substituting $z = e^{j2\pi f/f_{ref}}$ and assuming the quantization noise spectra is white, the PSD is calculated from the NTF as

$$S_f(\Delta f) = \frac{\Delta^2}{12 \cdot f_{ref}} \left[2 \sin\left(\frac{\pi f}{f_{ref}}\right) \right]^{2n} \tag{2.29}$$

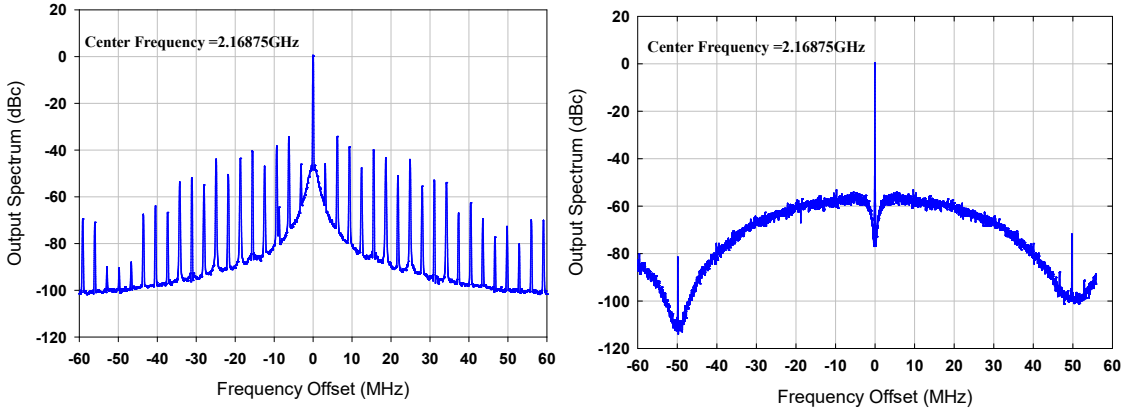
where n is the order of the modulator and the quantization step $\Delta = 1$ (since the minimum change in divider value can only be 1).

2.6 Fractional Spurs

A major disadvantage of MASH modulators is their tendency to produce periodic limit cycles in response to DC inputs [25]. These limit cycles lead to spurs at the output of the PLL and are most severe when the desired fractional offset is a rational fraction of the reference frequency [23]. Despite the digital nature of the ΣΔ approach the spur locations are hard to predict [11]. Furthermore, the magnitude of the spurs are not correlated with the fractional value as such various fractional ratios must be simulated to determine the worst case spur. In [25] it is asserted that in order to prevent limit cycles, the LSB of the input bit stream can be preset to "1" to set an irrational number condition. Presetting the LSB however introduces an error in the synthesized frequency. Thus, in order to minimize the frequency error, the size of the accumulator needs to be made large enough.

Figure 2.19 shows the simulated spectrum of a Fractional-N PLL for $f_{out} = 2.16875$ GHz with a 24-bit ΣΔ modulator. In Figure 2.19 (a) the input of the ΣΔ modulator was set to K= $(011000000000000000000000)_2$, which is the 24-bit representation of 0.375 (the choice of a 24-bit accumulators leads to a negligible frequency error for the preset condition). In Figure 2.19 (b) the LSB of the first accumulator in the MASH modulator was preset to '1'. The irrational initial condition is effective in eliminating the fractional spurs. The only visible spur is a reference spur. From Figure 2.19 (b) it can be observed that the phase noise is shaped by the high pass characteristic NTF of the MASH modulator and the PLL closed loop transfer function. Thus the phase noise increases to a point and

then decreases when the attenuation provided by the PLL closed loop transfer function begins to dominate the modulator NTF.



(a) (b)

Figure 2.19 Output spectrum of fractional-N PLL (f_{Ref} = 50 MHz $N = 43, n = 0.375$ $f_{out} = 2.16875$GHz): (a) zero initial condition (b) preset LSB '1' condition

2.7 Phase Noise Analysis of Fractional-N PLL with MASH ΣΔ Modulator

Due to the non-linear nature of ΣΔ PLLs [27], the LTI model for the PLL becomes more complicated and its behavior is no more well predicted by the model presented previously. Various modeling and analysis approaches for ΣΔ PLLs have been presented [1, 21-23, 27, 28]. The model in [27] is a simple frequency model which is parameterized by the characteristic closed loop transfer function $G(f)$ of the PLL (Figure 2.20). The model presents several insights into the ΣΔ PLLs.

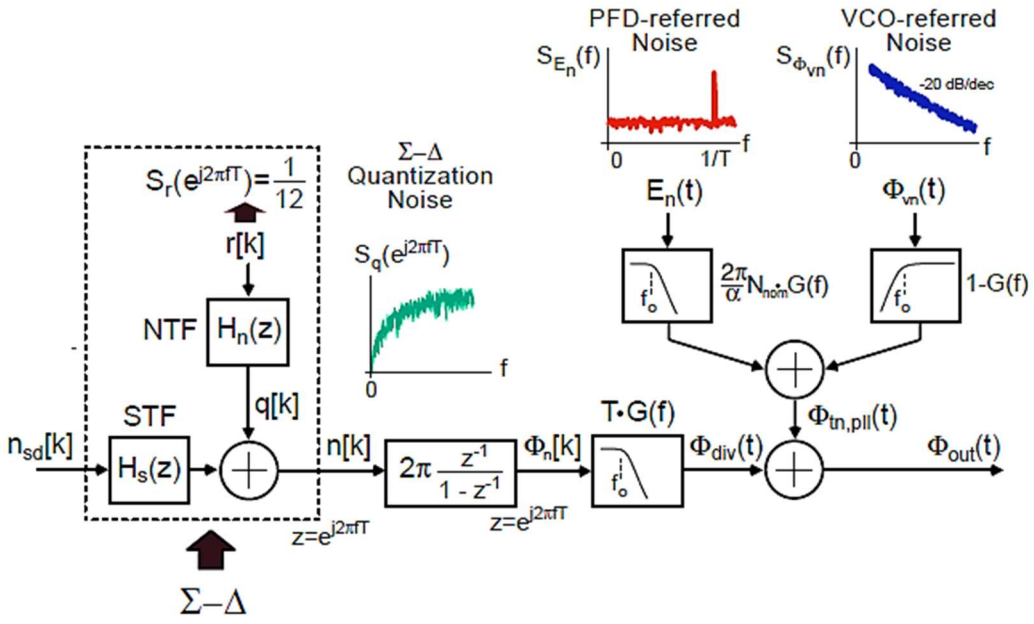


Figure 2.20 Parameterized model of ΣΔ synthesizer (reprinted with permission from [27])

In the ΣΔ PLL the output of the loop divider is influenced by the integration of the deviations in the divider value due to the modulator, as such a digital accumulator is used to model the integrating effect of the loop divider. The order of the shaped quantization noise in the ΣΔ modulator is reduced by one due to the action of the digital accumulator. The low pass closed loop transfer function $G(f)$ then acts on the shaped quantization removing the high frequency components. The resulting ΣΔ quantization noise presents as an additional noise source to the existing phase noise contributors.

Using the above model the impact of the ΣΔ quantization noise on the PLLs noise performance is easily derived. Employing Figure 2.20 and a discrete-input to continuous

time output, DT-to-CT, transformation [27] the impact of the quantization noise at the output of the PLL is calculated as :

$$S_{\phi,\Sigma\Delta}(f) = \frac{1}{T}|T \cdot G(f)|^2 \left|2\pi \frac{e^{-j2\pi fT}}{1-e^{-j2\pi f}}\right|^2 \times \left|\left(1-e^{-j2\pi fT}\right)^p\right|^2 S_r(f) \qquad (2.30)$$

where $T = 1/f_{ref}$ is the PFD input frequency ,$S_r(f) = 1/12$ is the quantization noise spectrum (assumed to be white) and p is the order of the modulator.

The SSB phase noise PSD for a MASH modulator at the output of the PLL is then re-written as ;

$$S_{\phi,\Sigma\Delta}(\Delta f) = \left[\frac{(2\pi)^2}{12 f_{ref}}\left[2\sin\left(\frac{\pi\Delta f}{f_{ref}}\right)\right]^{2(p-1)}\right] \cdot |G(j2\pi\Delta f)|^2 \left[\frac{rad^2}{Hz}\right] \qquad (2.31)$$

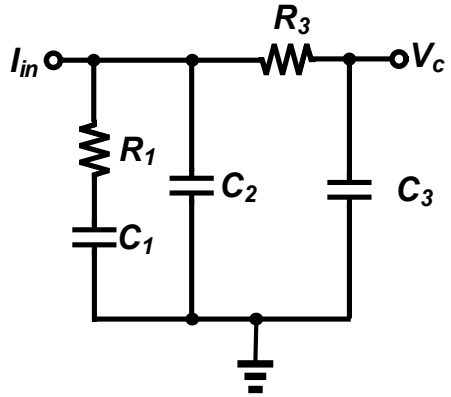
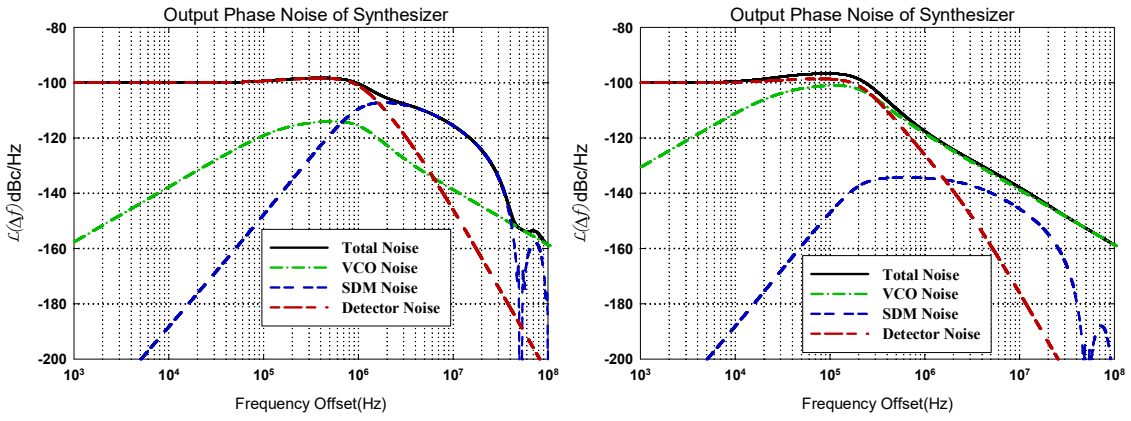


Figure 2.21 Third order passive low pass filter

For second and higher order modulators, the modulator quantization noise increases rapidly at higher frequencies around $f_{ref}/2$. To effectively suppress the high frequency noise of a pth order modulator a PLL of at least (p +1)th order is required([1, 10]) Figure 2.21 shows a third order passive low pass filter [29] that is usually employed in fractional N PLLs with 3rd order MASH modulators [1] (an implementation of this loop filter results in a fourth order PLL).



(a) (b)

Figure 2.22 Effect of the PLL filtering on the ΣΔ noise (a)with a large loop bandwidth (b) with a reduced loop bandwidth set by the ΣΔ characteristics

In Figure 2.22 the ΣΔ quantization noise of the MASH modulator at the output of the PLL is plotted with the output phase noise. Figure 2.22 reveals the equivalence of the loop bandwidth on the phase noise contributed by the ΣΔ modulator. Figure 2.22 (a) shows

the output phase noise plot of a fractional-N PLL with $f_c \approx 1MHz$. The fourth order PLL incorporates a third order loop filter (Figure 2.21) and a 3rd order MASH modulator. The out-of-band phase noise is dominated by the quantization noise over a broad frequency range. In Figure 2.22(b), f_c is reduced to 200 kHz and the effect of the quantization noise is reduced.

From Figure 2.22 it is obvious that there exists a tradeoff between the loop bandwidth and the phase noise contribution of the ΣΔ modulator to the out-of-band phase noise. The maximum bandwidth requirement to meet a given out-of-band phase noise specification at a given offset can be approximated for a p^{th} order MASH modulator as [1]:

$$f_{c,max} \approx \left[S_{\phi,\Sigma\Delta}(\Delta f) \cdot \frac{12}{(2\pi)^{2p}} . f_{Ref}^{2p-1} \cdot \Delta f^2 \right]^{\frac{1}{2p}} \tag{2.32}$$

The constraints posed on the ΣΔ modulator due to in-band noise contributions are less severe than the constraints due to the out-of-band phase noise when the loop bandwidth is chosen appropriately [1]. For the purposes of this thesis it is assumed that the loop parameters in a ΣΔ fractional-N PLL are chosen so that the VCO still dominates the out-of-band noise, as in Figure 2.22 (b).

The narrow bandwidth constraint posed on the design of the fractional-N PLL ((2.32)) contradicts the initial goal of implementing fractional techniques for higher loop bandwidth. Although the bandwidth advantage of the ΣΔ fractional-N PLL is limited (as evident in (2.32)), it still provides a better design advantage compared to integer PLL when fine frequency resolutions are required. For the same bandwidth, fractional N synthesizers

can employ higher reference frequencies, reducing the loop divider value and thus provide better *in-band* noise performance. Further, advantage of using higher reference frequency in the fractional-N PLL makes its reference spurs less sensitive to leakage currents.

2.8 PLL Output Jitter

Absolute jitter is the widely used jitter metric in PLL design literature. The definition of the absolute jitter and its relation to other jitter metrics is presented in [4]. The variance of the long-term PLL absolute jitter is related to the PLL phase noise PSD as [4] :

$$\sigma_{t,PLL}^2 = \frac{1}{(2\pi f_{out})^2} \int_0^\infty S_{\phi,PLL}(f)\, df \ \ [\, s^2] \tag{2.33}$$

The total output phase noise of the PLL can be approximated as

$$S_{\phi,PLL}(\Delta f) = S_{\phi,in-band}(\Delta f) + S_{\phi,out-band}(\Delta f) + + S_{\phi,\Sigma\Delta}(\Delta f) \tag{2.34}$$

As discussed earlier, if the order and bandwidth f_c of the PLL is chosen appropriately the noise performance of the PLL will be limited by $S_{\phi,in-band}(\Delta f) + S_{\phi,out-band}(\Delta f)$ which are due to the detector noise and the VCO noise respectively.

The PLL output jitter is minimized when f_c equals the frequency at which the detector noise and VCO phase noise spectrum cross over [3, 30]. When f_c is equal to this optimum frequency $f_{c,opt}$ the in-band and out-of-band noise components contribute equally to the output phase noise. The optimal PLL design (from the jitter and phase noise perspective) therefore has the 1) the detector and VCO consuming equal power and 2) the PLL open loop bandwidth set at $f_{c,opt}$. When these conditions are satisfied, the output jitter is independent of the reference frequency f_{ref} and the output frequency f_{out} [30].

2.9 Motivation and Problem Statement

The achievable data rates in high throughput applications such as LTE-Advanced is limited by the phase noise performance of the RF synthesizers used in the transceiver chain. Jitter associated with clock signals limits the SNR performance of data converters (ADCs and DACs) and results in degraded performance of clocked digital circuits. From the discussions presented in this section, it is obvious that the in-band phase noise performance of the traditional PLL is degraded by the feedback divider and is constrained to $\mathcal{L}_{detector} + 20\log_{10} N$. Furthermore, a larger loop bandwidth is required to suppress the VCO noise. A larger loop bandwidth also improves the dynamic performance of the PLL. However, the loop bandwidth of the classical PLL is limited to at least an order of magnitude less than the reference frequency. The narrow bandwidth issue is further worsened by the effect of reference spurs. To minimize the jitter in the synthesized clock, both the in-band and out-band noise must be reduced and the loop bandwidth must be optimally chosen such that both noise components contribute equally to the total output phase noise.

Fractional techniques are required in PLLs to achieve finer frequency resolution to support applications which require very accurate frequencies (such as NMR spectroscopy) or in communication standards where the channel spacing is small. Fractional techniques in the classical PLL achieve better frequency resolution by decoupling the reference frequency from the required resolution. However, the quantization noise resulting from the fractional operation degrades the spectral purity of the synthesized frequency. This

leads to a stringent trade-off between the bandwidth of the PLL and the degrading effect of the fractional modulator quantization noise on the PLL output spectrum.

The analog nature of the PLL makes it susceptible to effects such as mismatches and leakage current which lead to spurious signals at the output of the PLL. As CMOS technology keeps scaling down, the performance of analog circuits in logic centric nanometer processes has worsened and will continue to degrade as the process channel length is scaled down. To this end, all-digital PLLs (ADPLL) have received much prominence in recent publications [31-34]. ADPLLs employing high performance time-to-digital converters (TDC) can be used to synthesis fractional multiples of the reference clock. However, the phase noise and jitter performance of such systems is strongly reliant on the effective resolution and linearity of the TDC [34, 35]. The TDC is still generally an analog block and thus it is quite challenging to design it for high resolution and linearity especially in modern nanometer technologies.

The aim of this work is to design a Fractional-N PLL frequency synthesizer based on a divider-less architecture. By eliminating the divider (and its accompanying noise), the PLL in-band noise can be reduced. Also by employing a high detection gain in the PLL the remaining in-band noise components can be greatly reduced. A desired feature in the architecture is to reduce the reliance on high performance analog circuity by incorporating techniques that are insensitive to mismatches and precise timing. This will invariably lead to achieving lower phase noise with larger loop bandwidths.

As in the classical PLL, the fractional control of the design must be digital in nature for ease of implementation. The effect of the quantization noise on output of the

PLL and any tradeoff between the phase noise resulting from the fractional operation and the loop bandwidth must be minimized.

3. FRACTIONAL-N SUBSAMPLING PHASE LOCKED LOOP

3.1 Introduction

In the previous chapter it was shown that PLL output phase noise contributed by the detection circuitry (reference, PFD/CP and divider) is multiplied byN^2. As such the in-band phase noise of the conventional PLL is constrained to $\mathcal{L}_{PD/CP} + 20\log_{10} N$ and hence can be quite large for PLL with large divide ratios.

To mitigate the effect of the noise amplification caused by the loop divider, divider-less PLL architectures based on different phase detectors have been explored. PLLs based on aperture phase detectors, [36] and [37], directly compare the phases between the reference signal and the VCO signal in a small time window eliminating the need for frequency dividers. Even though the gain seen by the PD/CP noise to the output of the PLL is reduced, the effective multiplication factor is still a function of N^2 in practical implementation [37] . In the case of injection-locked PLLs [31, 38-40] it has been shown that the phase noise within the lock range f_l , is suppressed to that of the injection signal [39]. Provided $f_l > f_c$ the in-band phase noise is constrained to $N^2.S_{\phi,inj}$; $S_{\phi,inj}$ being the PSD of the injection signal. While the phase noise of the injection signal $S_{\phi,inj}$ is typically less than $S_{\phi,detector}$ of the CP-PLL, there is still a strong dependency of the in-band phase noise performance on N. The subsampling PLL (SSPLL) proposed in [6] achieved a very competitive low integrated phase noise (rms jitter) as well as figure-of-merit by removing the frequency divider and the conventional CP and incorporating a sampling based phase detector.

However, due to its innate integer-N operation, the SSPLL presented in [6] did not receive much attention. Recently the challenge of fractional operation in the SSPLL was addressed in [41] and [42] by modulating the phase of the reference frequency with a digital to time converter (DTC). In this work a fractional N SSPLL (FNSSPLL) based on a similar principle as that presented in [41] and [42] is designed and implemented.

The proposed FNSSPLL has the following similarities and differences compared to the previously reported works in [41] and [42] :

(1) The DTC modulator used in [41] is based on a MASH 1-1-1 modulator. While higher order modulators are preferred from the noise shaping and spur performance perspective, the use of such modulators increases the required DTC range. The design of a DTC with a wide dynamic range and fine resolution can prove to be challenging and present a power-jitter trade-off which will limit the FOM of the design. Thus in the proposed architecture, the modulator is built around a second order MASH modulator (MASH 1-1) to limit the required DTC specification; (2) the design incorporates a novel fast 2-step automatic background gain error correction mechanism which effectively reduces the noise folding and spurious tones due to non-idealities in the DTC; (3) unlike the previous FNSSPLLs in [41] and [42], the design presented in this work achieves higher frequency resolution without much hardware overhead by leveraging on the dithering provided by the MASH modulator as will be shown later; (4) in the presented design the traditional SSPLL is modified by incorporating a divide-by-2 in the feedback path to serve as a buffer between the VCO and the phase detector. As

will be discussed, this proves crucial in reducing the spurs at the reference frequency and its harmonics. The additional noise introduced by the divide-by-2 proves to be minimal, and thus the design still achieves comparable in-band phase noise performance while achieving a much better reference spur performance compared to the previous FNSSPLLs.

In the following sub sections an overview of the sub-sampling PLL operation is presented. This is followed by an analysis of the phase noise based on a linear phase model of the PLL. A comparison between the phase noise of the classical PLL and the SSPLL is then made. Following this the proposed digital fractional control is discussed. An analysis of the various implementation limitations and their mitigation is then discussed. The section is then concluded with a complete phase domain model and phase noise analysis of the proposed design

3.2 Sub-sampling PLL (SSPLL)

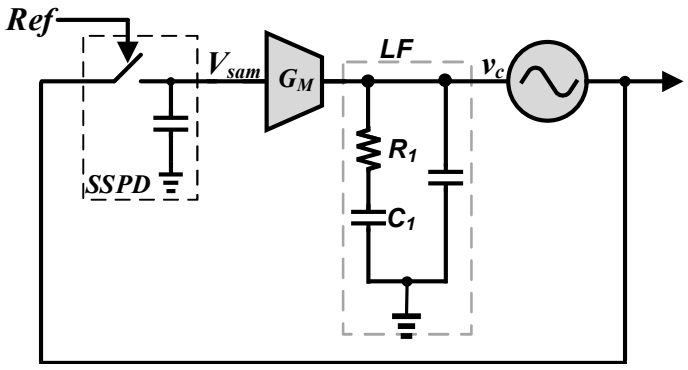


Figure 3.1 Basic architecture of the Sub-sampling PLL

The basic architecture for the SSPLL proposed in [6] (shown in Figure 3.1) consist of a sampler controlled by the reference clock which acts as the phase detector, a transconductor G_M which is analogous to CP in the classical CP-PLL, a loop filter and a VCO. The high frequency VCO signal is "sub-sampled" by a lower frequency (reference frequency) with the subsampling phase detector ($SSPD$). The output voltage of the sampler is proportional to the timing error (and thus the phase error) between the VCO frequency f_{vco} and the reference frequency f_{ref}. The sampled voltage V_{sam} is then converted to an error current by the transconductor G_M which is fed to the low pass filter LF. Under locked conditions, the phase error is ideally zero and consequently $V_{sam}$is the DC voltage of the VCO waveform and no current is fed to the LF .

3.2.1 Sampling based PD

Sample-and-hold phase detectors have been employed in PLL design for quite some time [9],[8, 43, 44]. Sampling PDs have been applied in frequency synthesizers to lock to harmonics of the sampling rate, suppress ripple or in applications where the signal appears in short burst [10]. It has been shown that PLLs based on such phase detectors offer optimal transient response and are theoretically capable of achieving lock in as little as one reference period [9]. However, sampling PDs require large filter capacitors due to their inherent high detection gain and have limited acquisition range, limiting their use in integrated PLLs [9]. In [6] a modified sample-and-hold PD was presented which alleviates these drawbacks.

Figure 3.2 and Figure 3.3 shows the conceptual and timing diagram of a sample-and-hold PD [6]. Given that the ratio and f_{vco}/f_{ref} is an integer, the sampled voltage V_{sam} is equal to the DC voltage V_{DC} of the VCO signal when the VCO and Ref phases are aligned. If a phase error exists the difference between V_{sam} and V_{DC} is proportional to the phase error between the VCO and Ref signals as shown in Figure 3.3. The sampling based PD can work without a divider when f_{vco}/f_{ref} is an integer, resulting in potentially lower in-band phase noise [6].

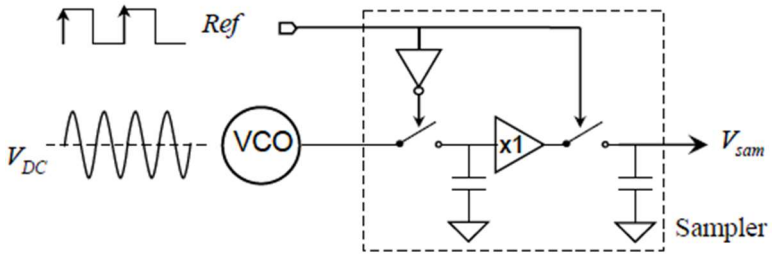


Figure 3.2 Conceptual diagram of sampling based PD [6]

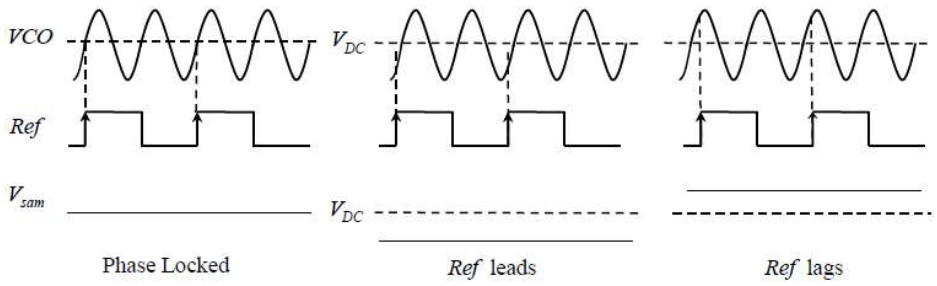


Figure 3.3 Timing diagram for the sampling based PD (reprinted with permision [6])

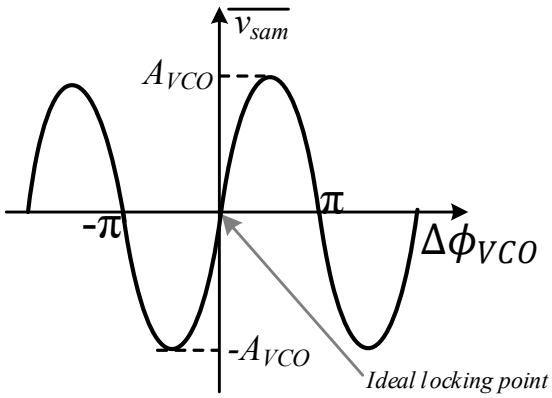


Figure 3.4 Characteristic of sampling based PD

The characteristic of sampling based PDs is the same shape as the VCO waveform in that if the VCO waveform is sinusoidal the PD characteristic is also sinusoidal with a maximum output equal to the VCO peak signal amplitude A_{VCO} [10]. Figure 3.4 shows the characteristic of a sampling based PD. The ideal lock point corresponds to the VCO crossing point that leads to zero phase error, however the PD will also lock at integer multiples of π; the PD cannot differentiate between integer multiples of the reference. Unlike the mixer based PD which also exhibits a sinusoidal characteristic, the SSPD is insensitive to the duty cycle or shape of the reference clock since in each reference period only a single sample of the VCO phase information is processed [6].

Around the locking point, the phase error is small and the SSPD gain is independent of the reference and VCO frequency and can be calculated as [6]:

$$K_{SSPD} = \frac{\Delta v_{sam}}{\Delta\phi_{VCO}} = \frac{A_{VCO}\sin(\Delta\phi_{VCO})}{\Delta\phi_{VCO}} \approx A_{VCO} \tag{3.1}$$

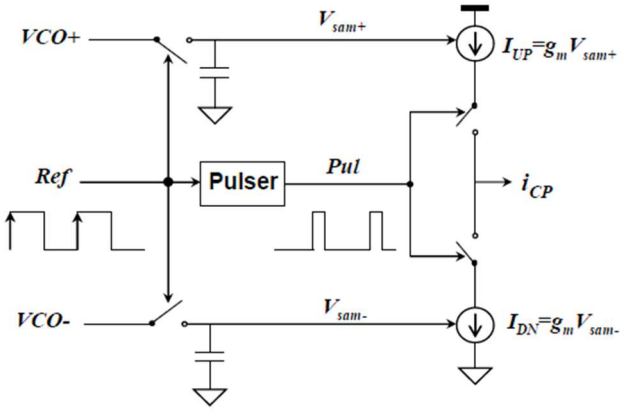


Figure 3.5 SSPD/CP with pulse width gain reduction (reprinted with permission from [6])

The combined gain of the sampling based PD and the transconductor CP is expressed as

$$K_{PD} = \frac{\Delta \overline{i_{CP}}}{\Delta \phi_{VCO}} = A_{VCO} \cdot g_m \tag{3.2}$$

3.2.2 SSPD/CP with pulsed gain reduction

The value of the loop capacitance required to have a stable loop is directly proportional to the PD/CP gain K_{PD} [12].The K_{PD} in equation (3.2) is large and thus would require a large filter capacitance making full integration difficult . One way to reduce the gain is to reduce the charge pump bias current effectively reducing g_m. However the effects of process, voltage and temperature (PVT) variations will be more pronounced for smaller current sources. In [6] a pulse reduction technique is used; a pulse generator (pulser) generates a pulse of width τ_{pul} in each reference period T_{Ref} which simultaneously turns on the UP and DN current sources as shown in Figure 3.5 and Figure

3.6. The average CP output current is thus reduced by τ_{pul}/T_{Ref} and the combined SSPD/CP gain is:

$$K_{PD} = \frac{\Delta\overline{i_{CP}}}{\Delta\phi_{VCO}} = 2 \cdot A_{VCO} \cdot g_m \cdot \frac{\tau_{pul}}{T_{Ref}} \tag{3.3}$$

Since the pulser output and *Ref* are non-overlapping there is no need for a second track and hold which is usually required to make the sampled voltage a constant DC value. Also the use of anti-phase VCO and differential sampling mitigates charge injection and charge sharing issues associated with sample-and-hold circuits and helps reject supply noise [6].

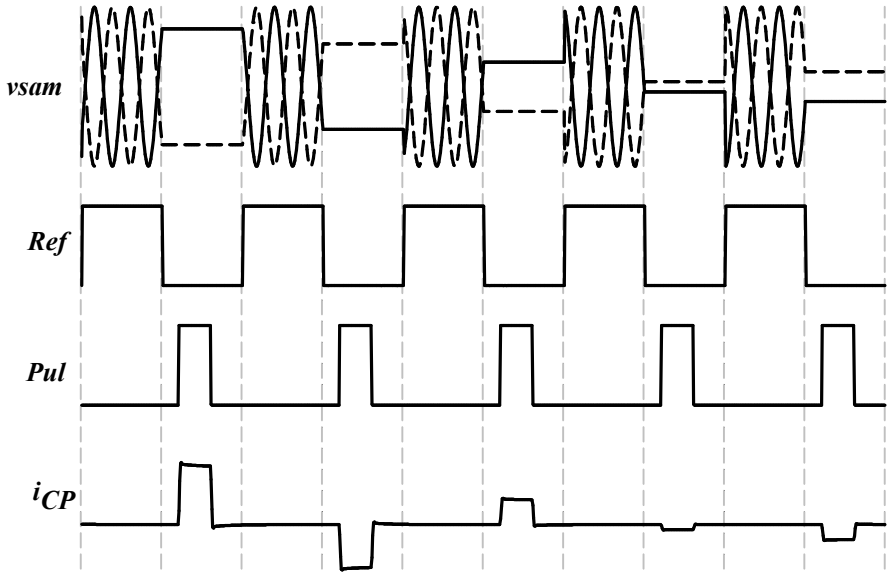


Figure 3.6 Simulated operation of SSPD/CP with gain reduction

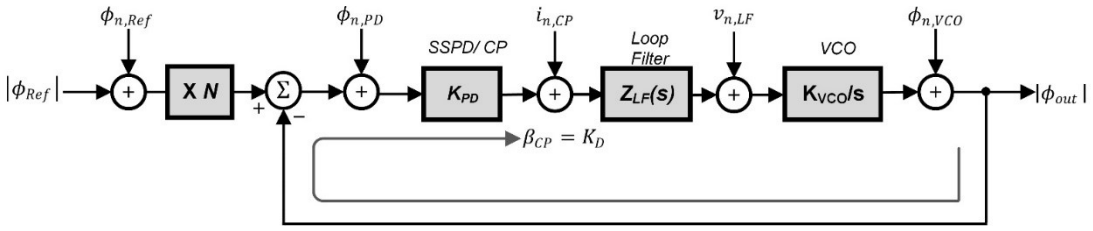


Figure 3.7 Phase domain model of SSPLL with noise sources

3.2.3 Linear continuous time model of SSPLL

Although sampling based PLLs are discrete time processes in nature, if the sampling period is constant and the open loop bandwidth is constrained to a tenth or less of the sampling rate, the loop behavior can be modeled by using continuous time system approximations[9]. If the system bandwidth constraint is not met, a complete z-domain analysis of the system is required to incorporate the effects of sampling; such analysis is presented in [9] and [43, 44] .

Due to the sub-sampling operation, the output of the sampler is an aliased signal of the VCO with a frequency given by:

$$f_{alias} = f_{VCO} - f_{ref} \times round\left(\frac{fvco}{fref}\right) = fvco - N \cdot fref \qquad (3.4)$$

where $round(x)$ rounds to the nearest integer N. From equation (3.4) there is a "virtual" multiplication $\times N$ of the reference frequency /phase of Ref at the phase comparison node. While this multiplication does not physically exist, it must be incorporated in the model to capture its effects on the system. As stated already, the sampling based PD can work without the feedback divider, hence there is no divider in the feedback path. Figure 3.7

shows the linear phase domain model of the basic SSPLL with noise sources. The open loop transfer function $A_{SS}(s)$ of the SSPLL is derived from Figure 3.7 as:

$$A_{ss}(s) = K_{PD}\, Z_{LF}(s)\, \frac{K_{VCO}}{s} \tag{3.5}$$

Similarly the closed loop transfer function from the input of the SSPD to the output of the PLL is expressed as:

$$G_{ss}(s) = \frac{A_{ss}(s)}{1 + A_{ss}(s)} \tag{3.6}$$

3.3 In-band Phase Noise

From the phase domain model in Figure 3.7, the equivalent noise referred to the input of the SSPD can be expressed as:

$$S_{\phi,SSdetector} = \left(N^2 \cdot S_{\phi,Ref} + S_{\phi,SSPD} + \frac{S_{i,SSCP}}{K_D^2} \right) \tag{3.7}$$

The transfer function of the (input referred) detector noise to the output of the PLL is the closed loop transfer function $G_{ss}(s)$. The total in-band phase noise at the output of the SSPLL is given as:

$$S_{\phi,in-band}\,(\Delta f) = |G_{ss}(j2\pi\Delta f)|^2 \left(N^2 \cdot S_{\phi,Ref} + S_{\phi,SSPD} + \frac{S_{i,CP}}{K_D^2} \right) \tag{3.8}$$

From equation (3.8) there is no divider noise, and SSPD and CP noise are not multiplied by N^2 when transferred to the PLL output. However, the noise due to the reference crystal and its buffers is still multiplied by N^2 . The SSPLL potentially achieves less in-band noise.

3.3.1 SSPD noise

The SSPD noise contribution is found by relating the equivalent voltage noise its output $\overline{v_{n,SSPD}^2}$ and the corresponding VCO phase error in the steady state [6]

$$\overline{v_{n,SSPD}^2} = \frac{kT}{C_{samp}} \approx \left(A_{VCO} \cdot \Delta\phi_{VCO,SSPD}\right)^2 \tag{3.9}$$

where C_{samp} is the value of the sampling capacitor. Due to aliasing the noise of the SSPD is band limited to $[0\ f_{ref}/2]$. If white noise spectrum is assumed, the steady state phase error due to the SSB PLL in-band noise contributed by the SSPD is:

$$\left(\Delta\phi_{VCO,SSPD}\right)^2 = \int_0^{f_{ref}/2} S_{\phi,SSPD}(f)\, df = S_{\phi,SSPD}(f) \times \frac{f_{ref}}{2} \tag{3.10}$$

Combining equations (3.9) and (3.10) the SSB noise of the SSPD is:

$$S_{\phi,SSPD}(f) = \frac{2kT}{C_{sam} \cdot A_{VCO}^2 \cdot f_{ref}} \tag{3.11}$$

Since the noise of the SSPD not multiplied by N^2 , a large C_{sam} is not required to keep the noise contribution of the SSPD inconsequential.

3.3.2 Charge pump noise

Since the output current of the SSCP is duty-cycled by the action of the pulser, the current sources are switched on for a fraction of time reducing the CP noise as in the CP-PLL. The equivalent thermal noise current due to the current sources is thus:

$$S_{i,CP} = 2 \times 4kT\gamma \cdot g_{m,CP} \cdot \frac{\tau_{pul}}{T_{Ref}} \tag{3.12}$$

3.3.3 Noise comparison

In the CP-PLL the CP noise often dominates the in-band noise [6] and thus the in-band noise performance can be approximated by the influence of the charge pump noise. The closed loop CP noise transfer function is calculated as:

$$H_{CP}(s) = \frac{1}{\beta_{CP}} \cdot \frac{A(s)}{1 + A(s)} = \frac{1}{\beta_{CP}} G(s) \tag{3.13}$$

where β_{CP} is defined as the feedback gain from the output of the PLL to the charge pump output. For frequencies well below the loop bandwidth $f \ll f_c$, $G(s) \approx 1$ and the in-band phase noise due to the CP is approximately:

$$S_{\phi,in-band,CP}\,(\Delta f) = \left|H_{cp}(\Delta f)\right|^2 S_{i,CP}(\Delta f) \approx \frac{S_{i,CP}}{\beta_{CP}^2} \tag{3.14}$$

From equation (3.14) a larger β_{CP} is required in order to suppress the CP noise. For the classical PLL which makes use of the 3-state PFD/CP the β_{CP} is reduced by the divide ratio N as indicated by equation (3.15) . This aligns with the observation of the charge pump noise power being multiplied by N^2.

$$\beta_{CP,PFD} = \frac{\Delta\overline{\iota_{cp}}}{\Delta\phi_{VCO}} = \frac{K_{PD}}{N} = \frac{I_{CP}}{2\pi} \cdot \frac{1}{N} \tag{3.15}$$

In the SSPLL, since there is no divider in the feedback path $\beta_{CP,SS}$ is independent of N and is given by:

$$\begin{aligned} \beta_{CP,SS} = \frac{\Delta\overline{\iota_{cp}}}{\Delta\phi_{VCO}} = K_D &= 2 \cdot A_{VCO} \cdot g_m \cdot \frac{\tau_{pul}}{T_{Ref}} \\ &= 2 \cdot A_{VCO} \cdot \frac{2I_{CP}}{V_{gs,eff}} \cdot \frac{\tau_{pul}}{T_{Ref}} \end{aligned} \tag{3.16}$$

A larger β_{CP} leads to a lower in-band noise if the CP noise dominates the detector noise; beyond a certain β_{CP} the noise of the CP is negligible, the in-band phase noise is dominated by the other detector noise components and increasing β_{CP} further will have no advantage. Therefore the reduction factor τ_{pul}/T_{Ref} must be chosen such that $\beta_{CP,ss}$ is not "unnecessarily high" but sufficient enough to make the CP noise contribution to the output in-band phase noise negligible [6]. A good choice of $\beta_{CP,ss}$ improves the phase noise performance without requiring an unnecessarily large loop filter capacitor to stabilize the loop [6].

Comparing the CP feedback gains of the CP-PLL and SSPLL using (3.15) and (3.16)

$$\frac{\beta_{CP,SS}}{\beta_{CP,PFD}} = 8\pi \cdot N \cdot \frac{A_{VCO}}{V_{gs,eff}} \cdot \frac{\tau_{pul}}{T_{Ref}} \tag{3.17}$$

Typically, $N \gg 1$, $A_{VCO} > V_{gs,eff}$ and $0.1T_{Ref} < \tau_{pul} < 0.5T_{Ref}$ and thus equation (3.17) is much larger than 1. Assuming the same current sources are used in both architectures, the theoretical CP noise improvement achievable by using the SSPLL over the classical CP-PLL is expressed by equation (3.18). The in-band phase noise contributed by the CP in the SSPLL is orders of magnitude lower compared to the CP-PLL and this advantage becomes more prominent for higher f_{vco} or lower f_{Ref} [6] .

$$\begin{aligned} \frac{S_{\phi,in-band,CP,PFD}}{S_{\phi,in-ba\quad,CP,SSPD}} &= \left(8\pi \cdot N \cdot \frac{A_{VCO}}{V_{gs,eff}}\right)^2 \left(\frac{\tau_{PFD}}{T_{Ref}}\right) \\ &= \left(8\pi \cdot \frac{A_{VCO}}{V_{gs,eff}} \sqrt{\tau_{PFD}}\right)^2 \times \left(\frac{f_{VCO}^2}{f_{Ref}}\right) \end{aligned} \tag{3.18}$$

3.4 Frequency Acquisition

The sinusoidal characteristics of the SSPD limits its frequency acquisition range [6] . Since the output of the SSPD is incapable of distinguishing between integer multiples of the reference, the SSPLL may *false lock* to an arbitrary harmonic of the reference frequency [10], as such an auxiliary frequency locked loop (FLL) is needed to lock the frequency to the desired value . The FLL can be a simple conventional PLL consisting of a divide-by-N and a 3-state PFD/CP with a dead zone (DZ) inserted between the PFD and CP [6]. The FLL CP current is set such that the FLL loop gain is larger than that of the SSPLL outside the DZ. When the frequency/phase error is large and exceeds the FLL DZ, the FLL dominates and drives the VCO control voltage to reduce the error.

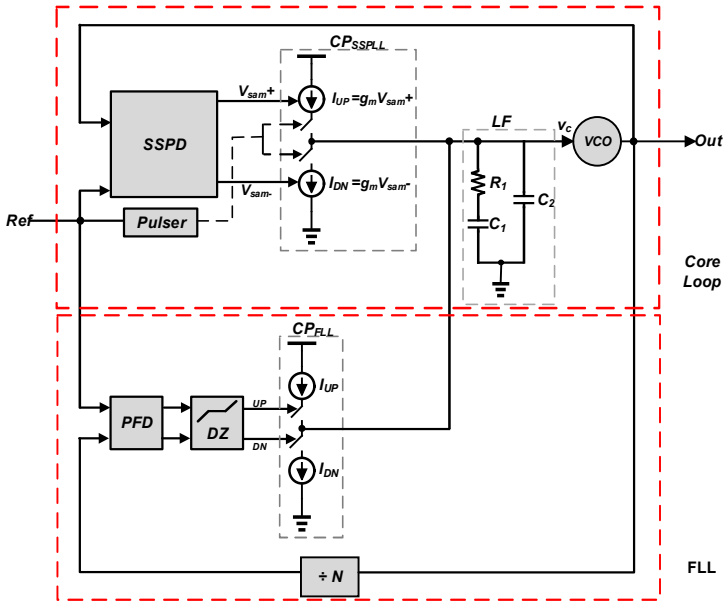


Figure 3.8 Block diagram of SSPLL (reprinted with permission from [6])

As the frequency error reduces and falls within the FLL DZ (frequency lock is acquired), the FLL CP current falls to zero and the core SSPLL takes over the loop control and locks the phase of the Ref and VCO (phase acquisition). When the SSPLL is in lock, the FLL does not influence the core loop performance and thus the low phase noise advantage of the sub-sampling technique is preserved. The complete block diagram of the SSPLL presented in [6] is shown in Figure 3.8.

3.5 Reference Spur Performance of SSPLL

In the SSPD/CP described in 0 , the amplitude of the output current depends on the sampled voltage but has a constant on-time τ_{pul} set by the pulser. Under locked condition, the net CP current is zero which implies that up and down current amplitudes must be equal. The loop tunes the VCO sampled point until the amplitudes of the current sources are matched by shifting the ideal locking point away from the VCO DC voltage. Since the action of the SSPLL drives the charge pump current to be equal, mismatches in the current sources lead to a steady state phase error as in the conventional PLL. However, the mismatch mechanism in the subsampling loop does not lead to ripples on the VCO control [45]. As such, the SSPLL has very low ripples on the VCO control. However, the periodic sampling of the VCO leads to charge injection, charge sharing and frequency modulation mechanisms that limit the spur performance of SSPLLs.

While buffers may be placed between the SSPD and VCO in practical design, the isolation provided by these buffers is limited by its parasitics especially at high frequencies

where parasitic effects are prominent; the sampling action still disturbs the VCO operation via parasitic paths in the buffers [46].

During the tracking phase of the sampler the VCO is loaded by C_{sam} (if a buffer is placed between the SSPD and the VCO, C_{sam} in this context is the effective capacitance seen by the VCO due to the sampler switching). The frequency during the tracking phase therefore varies from the VCO frequency during the hold phase of the sampler when the VCO is no longer loaded by C_{sam}. In [46] it is shown that the modulation in the VCO frequency by the periodic sampling action at f_{Ref} mimics binary frequency shift keying (BFSK) modulation. The VCO reference spur due to the BFSK effect is derived in [46] and is given as

$$SP_{f_{ref},BFSK} = 20\log\left[\sin(\pi\, D_{ref}) \cdot \frac{N}{2\pi} \cdot \frac{C_{sam}}{C_{tank}}\right] dBc \tag{3.19}$$

where D_{ref} is the duty cycle of the reference frequency and C_{tank} is the tank capacitance of the VCO. While a choice of a smaller C_{sam} will lead to a low spur level, the kT/C_{sam} noise of the sampler must also be kept low in order to achieve a good in-band phase noise performance.

Charge injection from the sampling switches also disturbs the VCO operation and results in spurs [45]. A dummy sampler can be used to cancel out the charge injection and reduce the BFSK effect since VCO is always connected to C_{sam}. The BFSK spur is then limited by the capacitor mismatch between the sampler and its dummy ΔC_{sam} and its amplitude is given as [46] :

$$SP_{f_{ref,BFSK}} = 20\log\left[\sin(\pi\, D_{ref}) \cdot \frac{N}{2\pi} \cdot \frac{\Delta C_{sam}}{C_{tank}}\right] \tag{3.20}$$

Charge sharing occurs between the VCO and C_{sam} since the sampling capacitor voltage and the tank capacitor voltage may be different when they are connected at the switch-on moment. While the sampling capacitor voltage is well-defined and equal to the VCO DC voltage, the tank capacitor voltage depends on the position of the reference tracking edge. Maximum charge sharing occurs if the reference tracking edge occurs at the peak of the VCO waveform[46]. . In [45] a duty cycle controlled reference buffer with a delay locked tuning is used to control the reference tracking edge to further reduce the spur level.

The spurs induced by the effects of the periodic sampling of the VCO are not associated with the loop filter and hence there is no trade-off between the loop bandwidth (and filter order) and the reference spur performance of the SSPLL. Therefore it is theoretically possible to achieve good spur performance with a large bandwidth in the SSPLL.

3.6 SSPLL in Fractional-N Mode

The SSPLL discussed so far is only capable of synthesizing integer multiples of the reference frequency. Figure 3.9 presents the issues in generating fractionally related frequencies to help understand the underlying principle of fractional operation. Figure 3.9 (a) shows two frequency waveforms whose frequency have a fractional relation, in this case $f_{Ref}/f_{VCO} = 1.75$. The timing difference between the edges $\Delta\tau$ (and hence phase

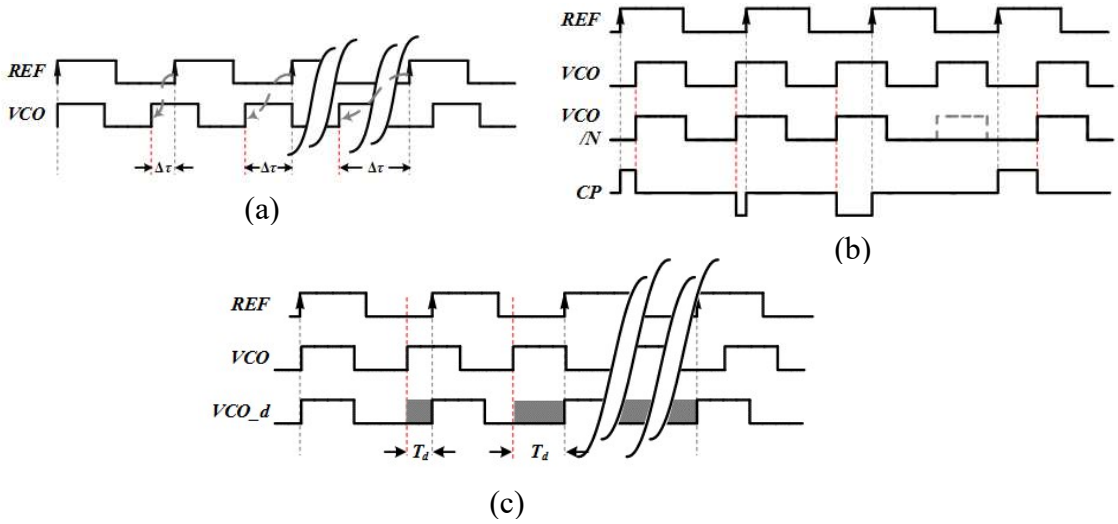


Figure 3.9 (a) Fractional frequency $f_{VCO} = 1.75 * f_{Ref}$. (b) programmable delay (c) programmable infinite delay

difference) becomes infinite with time. In order to achieve a zero average phase error (which is required for any PLL to lock), some phase modulation mechanism must exist in the PLL.

In the CP-PLL fractional operation is achieved by modulating the divide value such that some of the VCO pulses are "swallowed" and thus the average current of the CP is zero as shown in Figure 3.9 (b). A major advantage of the SSPLL is its ability to work without a divider leading to superior phase noise performance. It is therefore counter intuitive to introduce a divider to achieve fractional functionality. A residue DAC could be introduced to compensate the CP current due to the phase error, such that the average charge pump current when the PLL is locked is zero ([47] and [48]). However the DAC

resolution would need to be well matched to the loop gain leading to large DAC elements and the solution becomes cumbersome [41] .

Fractional operation can be achieved by modulating the VCO frequency; in Figure 3.9 (C) the VCO signal is delayed by T_d, to align the VCO edge with the reference edge. However a programmable infinite delay would be required to remove the timing skew over time making this impractical. Furthermore any operation on the VCO results in large power consumption (the VCO frequency is usually an RF signal and would require power hungry buffers) and poor phase noise performance.

In [41] it is observed that the phase of the reference can be modulated to match the phase of the VCO output to achieve a similar operation as the divider modulation in the CP-PLL. This technique is well suited to the sampling based PLL since the sampled phase error is controlled by the reference signal.

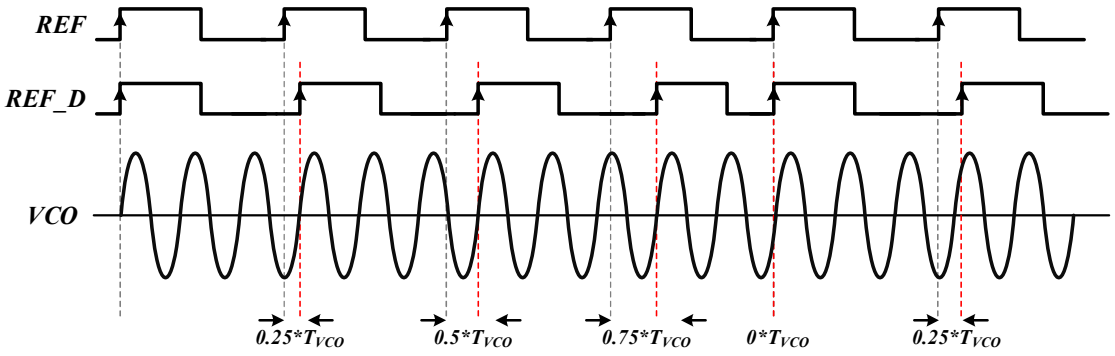


Figure 3.10 Fractional principle in the SSPLL: $f_{VCO} = 2.75 * f_{Ref}$

The basic fractional N operation in the SSPLL is illustrated in Figure 3.10. Assuming it is desired to generate a fractional ratio which differs from the integer ratio N_{int} by α where $0 \leq \alpha < 1$; in this example $\alpha = 0.25, N_{int} = 3$ and the desired division ratio $N = 3 - 0.25 = 2.75$. In the first reference cycle the sample point aligns with the positive zero-crossing point of the VCO as desired. However a timing error of $0.25 * T_{VCO}$ exists in the second cycle and the sampling edge must be delayed by this timing error in order to sample the positive zero crossing point of the VCO. The timing error in the 3rd cycle increases to $0.5 * T_{VCO}$ and the sampling edge must be delayed by this amount. Similarly, in the fourth cycle the sampling edge must be delayed by $0.75 * T_{VCO}$. By consequence the fifth sampling edge should be delayed by $1 * T_{VCO}$. However it can be observed that by skipping a VCO cycle, the sampling edge coincides with the VCO zero crossing and hence no delay is required ($0 * T_{VCO}$). In this example the SSPD samples the N_{int} VCO crossing point 3 times and $(N_{int} - 1)$ VCO crossing point once in every four reference cycles; the reference period and T_{VCO} are related as $4 \cdot T_{REF} = 3 \cdot N_{int} \cdot T_{VCO} + (N_{int} - 1) \cdot T_{VCO}$, and we note that

$$T_{REF} = \left(N_{int} - \frac{1}{4}\right) T_{VCO} = (N_{int} - \alpha) \cdot T_{VCO} \tag{3.21}$$

The desired divide ratio $f_{Ref}/f_{VCO} = N_{int} - \alpha$ is achieved by the "swallowing" of a VCO cycle similar to the action of the divider in the fractional-N CP-PLL. Since the SSPD exhibits a sinusoidal gain characteristic which repeats every VCO cycle this swallowing action does not generate any phase error and no modulation of the VCO control line occurs. Furthermore, the delay required in each reference period can be calculated

precisely, since both the desired fractional frequency and the reference frequency are well defined. Barring the ability to implement an ideal delay generator, the fractional-N SSPLL can produce a spur-less output frequency unlike the ΣΔ Fractional PLL in section 2.5. Since the delay wraps around, the delay range required is just a VCO period making this a more practical approach.

3.6.1 Fractional control of SSPLL

As previously stated the delay required in each reference cycle can be calculated precisely as it depends on the divide ratio N and the reference periodT_{Ref}. Therefore in order to control SSPLL for fractional operation, a DTC is employed to delay the reference signal. A digital controller is used to determine the required delay and controls the DTC as shown in Figure 3.11.

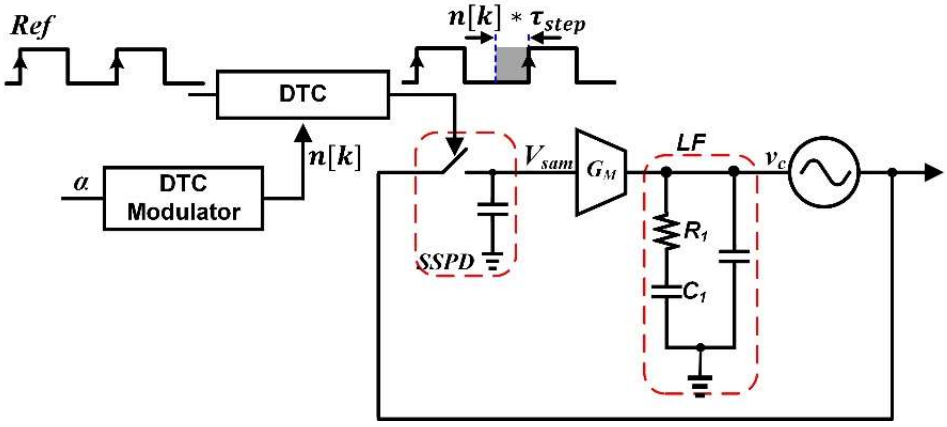


Figure 3.11 Basic implementation of a fractional-N SSPLL

Since the SSPD works with only integer related frequencies, α represents the frequency error in the phase detection. By accumulating this error we can determine the necessary phase adjustment (and thus delay) needed in the next clock cycle. By employing a digital accumulator, we achieve both the required accumulation and "phase wrapping" operations. The accumulator output then provides the precise delay (scaled by the VCO period) required in the subsequent cycle.

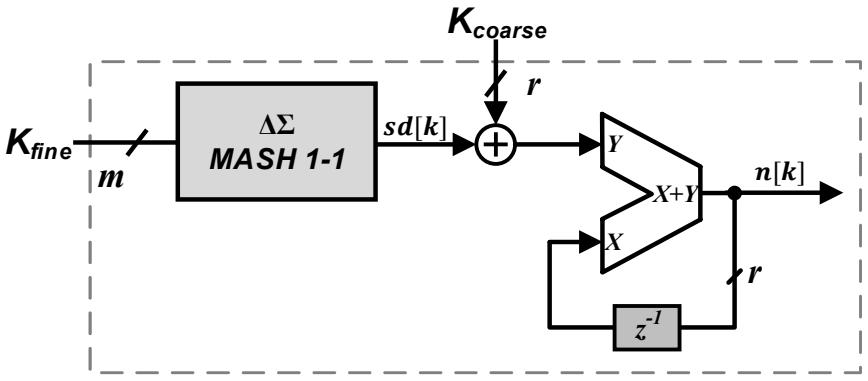


Figure 3.12 Proposed digital fractional control (DFC)

Figure 3.12 shows the proposed digital fractional control (DFC). For simplicity we initially assume sd[k] is 0. If we set $K_{coarse} = \alpha_1 * 2^r$, then the output of the r-bit accumulator, n[k] increments by K_{coarse} at each reference cycle. Provided the accumulator has no overflow the period of the DTC output is $N \cdot T_{VCO} = T_{ref} + n[k] *$

T_{VCO}. When the accumulator overflows the SSPD samples the (N-1)th VCO crossing point. The fractional value achieved is $N_{int} - K_{coarse}/2^r$.

In order to achieve higher frequency resolution K_{coarse} is dithered by the output of a MASH 1-1 ΔΣ modulator [49] . The output of the ΔΣ modulator sd[k] has a mean value $\alpha_2 = K_{fine}/2^m$ and thus the average input to the accumulator is $(K_{coarse} + \alpha_2)$. The resulting fractional part at the input of the accumulator becomes $\alpha = \alpha_1 + \alpha_2$ and hence

$$\alpha = \frac{K_{coarse}}{2^r} + \frac{K_{fine}}{2^{r+m}} \tag{3.22}$$

The achievable fraction division ratio is thus $N = N_{int} - \frac{K_{coarse}}{2^r} - \frac{K_{fine}}{2^{r+m}}$

3.7 DTC Non-Idealities

3.7.1 Finite quantization

The DTC delays the input reference in order to align the sampling edge and the VCO zero crossing point. Provided the least delay required is within the DTC resolution, no error exists in the sampling moment. The achievable accuracy in the delay generated and hence the sampling moment is limited by the resolution (LSB) of the DTC even for a noiseless system. A finite DTC resolution leads to error currents which are fed into the LPF leading to ripples on the VCO control line.

To reduce the effect of the limited DTC resolution on the PLL output spectrum, the quantization noise resulting from the finite DTC steps must be made negligible in comparison to the other noise sources [41]. MASH modulator at the input randomizes the

generated code which helps to reduce the spurious content. The second order modulator used has an output range of 3 .However the DTC range required becomes two VCO periods since codes generated have a larger range due to the action of the MASH 1-1 modulator.

3.7.2 Offset and gain error

Any offset in the DTC delay appears at the output of the PLL without degrading the spectral purity performance of the PLL since this delay is fixed and occurs in the reference path. Furthermore by careful design of the DTC the offset can be minimized. Due to the analog nature of the DTC, the DTC gain (delay per LSB) varies with PVT variations. The variations in the absolute gain cannot be predicted and differ under different operating condition.

Gain error in delay steps leads to spurs in the output spectrum of the PLL. Some form of automatic background calibration is required to keep track of the gain variations and adjust them either in the analog or digital domain. The required calibration can be implemented using sign least-mean-square (LMS) algorithms which have been extensively used in digital PLLs.

In [41] and [42] the LMS algorithm is achieved by extracting the sign of the sampled voltage and correlating it with a change in the direction of the digital control word. If γ is the DTC gain coefficient, then the LMS algorithm updates γ as follows:

$$\gamma[k+1] = \gamma[k] - \mu \cdot sgn\left[\sum_{j=1}^{k} p[j] \cdot SIGN\right] \tag{3.23}$$

where $p[j]$ is the digital control word from the DTC modulator , μ is the step size and SIGN is the sign of the sampled voltage. Intuitively the algorithm checks to see if the SSPD samples early or late with respect to a given word from the DTC modulator. For instance if SSPD samples earlier than delay determined by the DTC modulator, then the DTC gain is too low and γ is increased to compensate for this. The delay correction loop (DCL) does not contribute any noise to the circuit after it converges.

3.7.3 DTC nonlinearity

Integral non-linearity (INL) and differential non-linearity (DNL) in the DTC transfer function lead to an increased code-dependent quantization error and to potential noise folding and spurs [50]. Various techniques used to improve the linearity of DAC can be applied for the DTC as well. The main source of non-linearity is the mismatch between the delay tuning elements of the DTC. In this work careful consideration is given to the layout of the DTC elements; the layout is done in such a way to reduce the spread of the tuning elements and the routing parasitic. Matching improves with technology for the same area of capacitance [41] and as such the use of advanced nanometer-scale technology offers an added advantage in this regard. A dynamic element matching (DEM) technique based on data weighted averaging (DWA) [51] is employed to further improve the linearity of the tuning element array.

3.7.4 DTC phase noise

The device noise of the DTC appears in the reference path and adds to the reference noise. As previously mention the reference noise power is virtually multiplied by the frequency ratioN^2. Therefore the in-band phase noise performance of the SSPLL is limited by the phase noise of the DTC and reference. Careful design consideration must be to minimize the DTC noise to maintain the low phase noise advantage of the SSPLL.

4. DESIGN AND IMPLEMENTATION

This section presents the design of the various blocks in the proposed FNSSPLL. Design issues and techniques to circumvent these challenges are also presented.

4.1 Proposed System Architecture

Figure 4.1 shows the complete block diagram of the proposed FNSSPLL. The output frequency of the proposed FNSSPLL is given as:

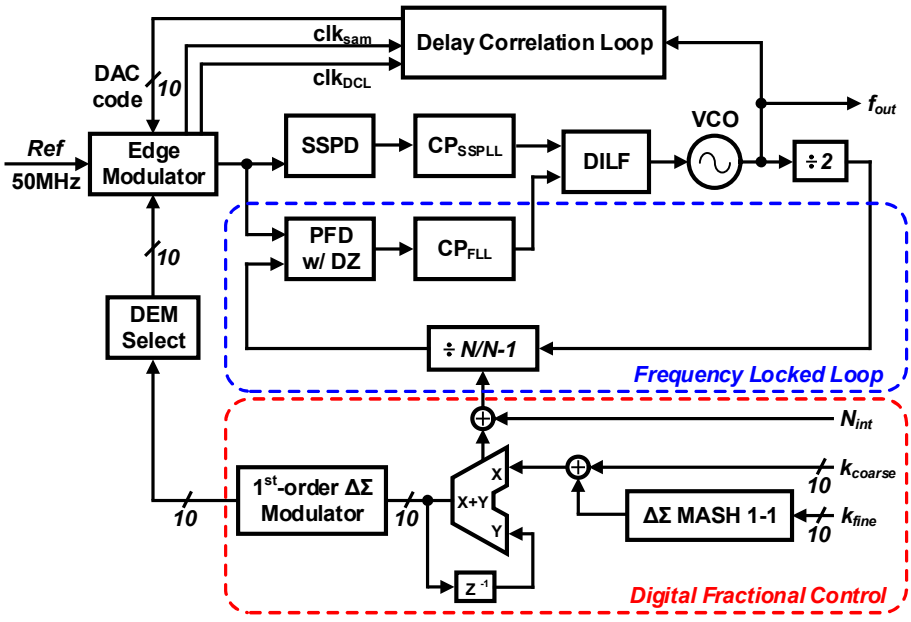


Figure 4.1 Block diagram of the proposed FNSSPLL

$$f_{out} = 2 * f_{ref}\left(N_{int} - \frac{k_{coarse}}{2^{10}} - \frac{k_{fine}}{2^{20}}\right) \quad (4.1)$$

where N_{int} is the integer division ratio and k_{coarse} and k_{fine} are the coarse and fine fractional control words. For a reference frequency of 50MHz the frequency resolution of the proposed FNSSPLL is 95.4 Hz.

In the following sections the implementation of the various blocks in the FNSSPLL are discussed.

4.2 Voltage Controlled Oscillator and Divide-By-2

4.2.1 Implementation of VCO

The implemented LC-VCO is based on a complementary cross-coupled negative resistances which has been shown to achieve lower power consumption for the same phase noise performance compared to NMOS/PMOS-only structures. The improved phase noise performance is achieved due to the modified impulse sensitivity function (ISF) and lower phase noise conversion gain of the architecture [14]. Figure 4.2 shows the schematic of the VCO

In this implementation the tail current source has been removed to reduce the flicker noise up conversion. Since the tail current has been removed the oscillation amplitude can be maximized to almost full swing. The VCO operates in the voltage-limited regime with almost constant amplitude along the entire tuning range [52]. By removing the tail current source, the VCO becomes sensitive to voltage variations on the supply line. To mitigate noise coupling from other circuits through the supply line the

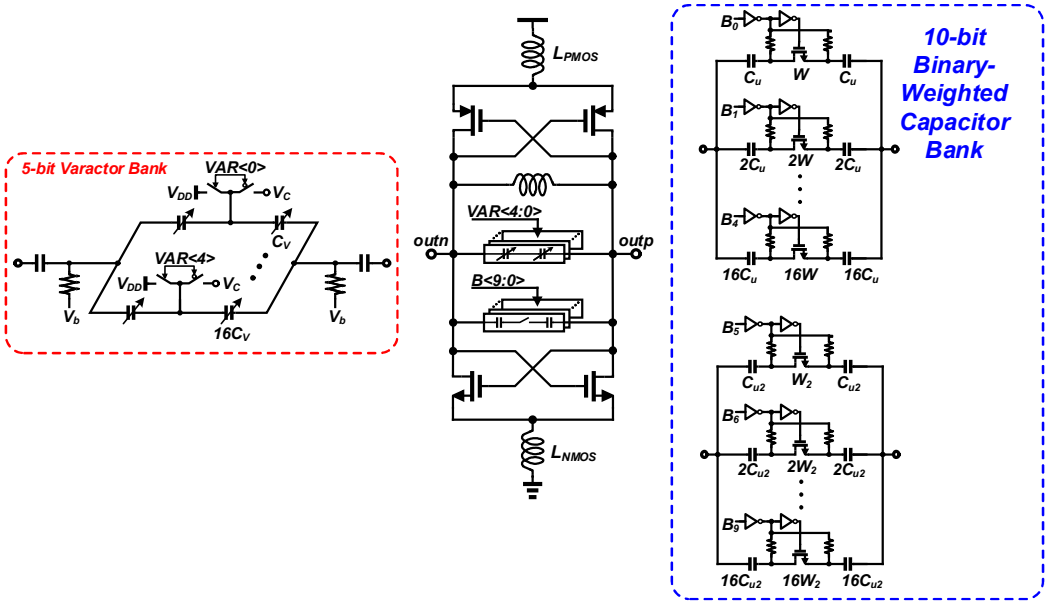


Figure 4.2 Schematic of complementary VCO circuit with capacitor banks

VCO core has a separate supply voltage line and thus a voltage regulator is used to supply the VCO supply voltage.

When the transistors enter deep triode during oscillation, the on-resistance of each transistor degrades the quality factor, Q, of the tank and the noise ISF from each transistor to the output phase is substantially larger [22]. Furthermore since the tail current has been removed the bias current of the circuit will vary largely across process and temperature. By decoupling the gate and drain of the PMOS transistors it is possible to bias the VCO core to minimize and control the current and avoid the PMOS transistors from entering deep triode. Since the gates of the PMOS do not see the full swing their sizes can be optimally chosen to reduce their parasitic capacitance.

Tail inductors are used to resonate the parasitic capacitance (at $2f_0$) at the PMOS and NMOS source nodes. The resulting source degeneration (at $2f_0$) reduces the flicker noise up conversion and tank Q degradation when one of the transistors enters the triode region [53].

A 10-bit capacitor array is connected to the tank to provide coarse frequency tuning of the VCO. The effect of a capacitance change on the frequency is less at lower frequencies as such the 10-bit bank is sub-divided into two 5-bit binary weighted capacitor banks and a larger unit capacitor is used for the lower frequencies.

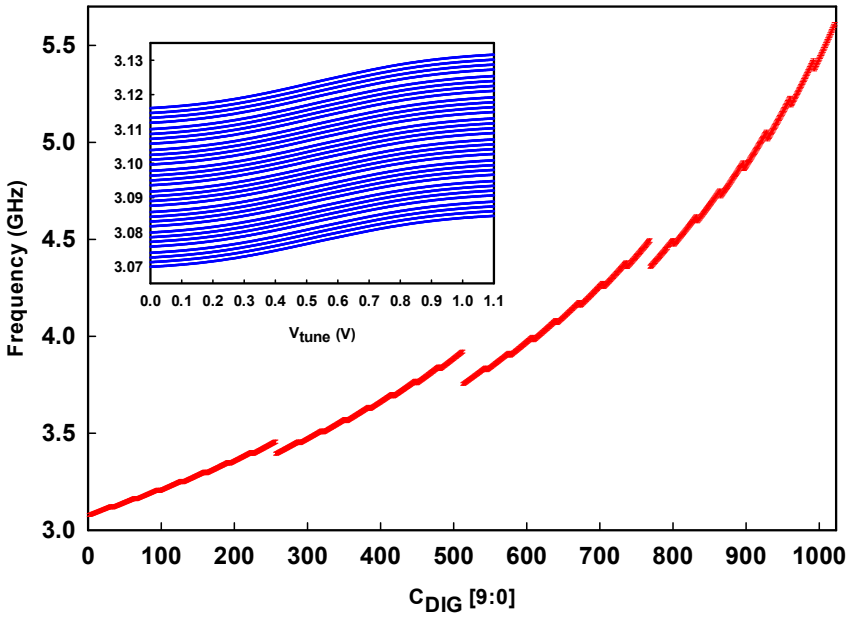
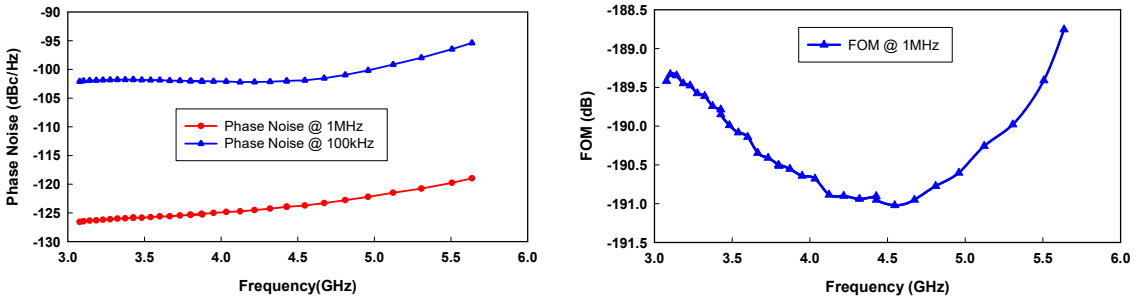


Figure 4.3 Simulated tuning range of the VCO across the coarse capacitor bank and fine tuning for $C_{DIG} = 0 - 31$ (insert)



(a) (b)

Figure 4.4 Simulated VCO performance across the VCO tuning range (a) Phase Noise at 100 KHz and 1MHz and (b) Figure-of-Merit (FOM)

Fine frequency tuning is achieved by using NMOS in N-well moscap varactors. Ac coupling between the varactors and VCO core is employed to avoid varactor modulation due to common mode variations. The varactors are biased to allow positive and negative voltages across them. This helps to provide a wide continuous tuning range. The coupling capacitors are chosen such that their effect on the capacitance provided by the varactors is minimum. Again since a wide tuning range is required a 5-bit binary weighted array of varactors is used to maintain the KVCO fairly constant across the entire frequency range. Figure 4.3 shows the simulated tuning characteristic of the VCO.

Figure 4.4(a) shows the simulated phase noise performance of the VCO across the tuning range at 100 kHz and I MHz offsets. The widely used figure-of-merit (FoM) for comparing the performance of VCOs is given as

$$FoM = Phase\ Noise - 10log\left[\left(\frac{\omega_0}{\Delta\omega}\right)^2 . \frac{1}{Power(mW)}\right] \qquad (4.2)$$

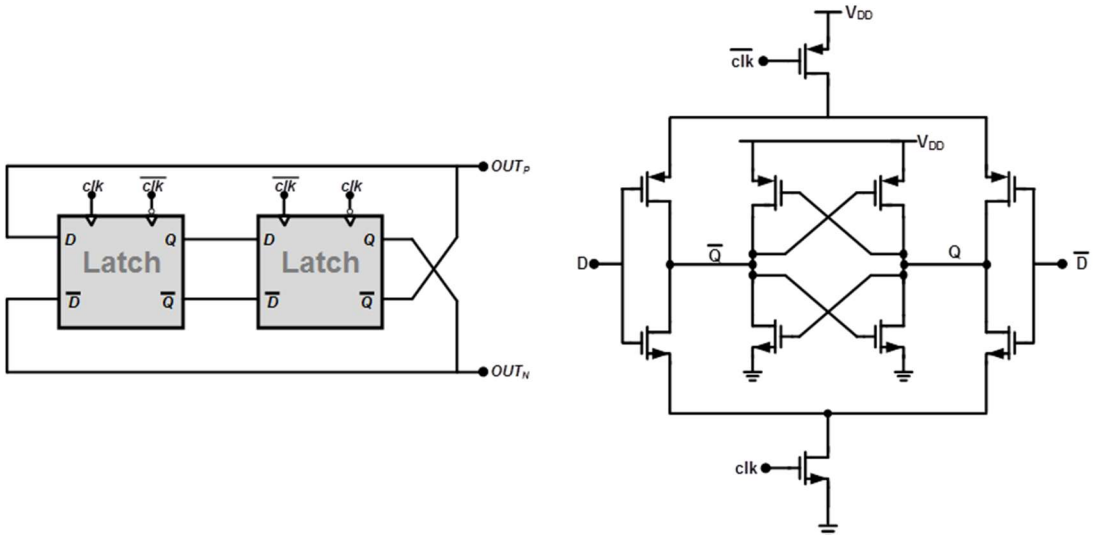
Table 4.1 Summary of simulated VCO performance

Parameter	Simulated
Frequency Range (GHz)	3.07~5.64
Power (mW)	3.28-4.98
Phase noise at 1MHz offset (dBc/Hz)	-123.95
FOM	-189.37

where ω_0 is the carrier frequency of the VCO and $\Delta\omega$ the offset from the carrier. In Figure 4.4(b) the simulated FoM at a 1MHz offset is plotted; the VCO achieves a FoM better than -189 dBc/Hz. The summary of the simulated VCO performance is presented in Table 4.1.

4.2.2 Divide-by-2

As discussed in the previous chapter, the periodic sampling of the VCO by the SSPD leads to BFSK phenomenon which introduces spurs in the output of the VCO. To reduce this effect, a divide-by-2 is inserted between the VCO and the SSPD to serve as a buffer. Furthermore the use of the divide-by-2 reduces the operating frequency of the SSPD and the programmable divider in the FLL. The divide-by-2 is shown in Figure 4.5 (a) consists of two dynamic differential cascode voltage switch logic (DCVSL) latches (Figure 4.5(b)) [54] connected in negative feedback loop. The DCVSL latches are used in this implementation since they provide low load capacitance on the input and provide automatic complementary function while consuming no static power. The simulated action of the divide-by-2 is shown in Figure 4.6.



(a) (b)

Figure 4.5 Divide-by-2 (a) circuit implementation (b) schematic for latch

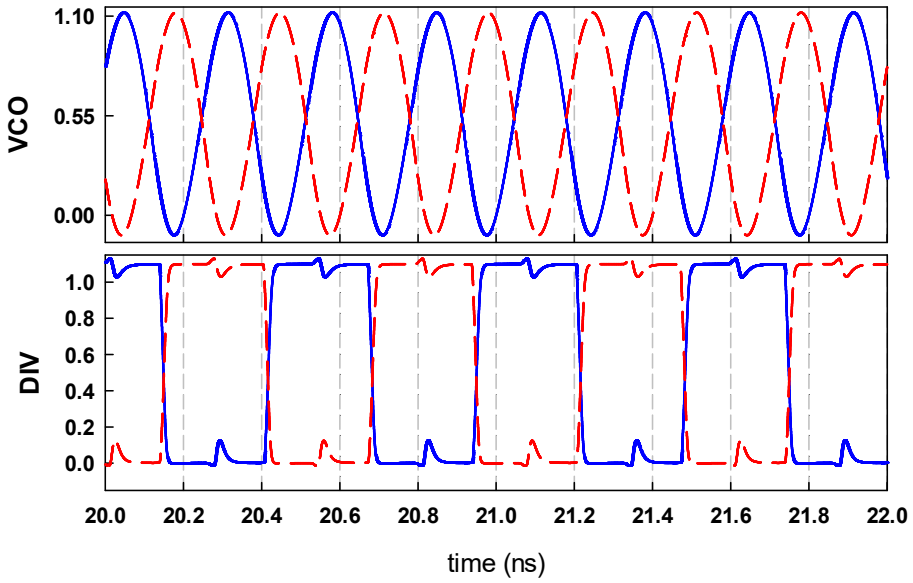
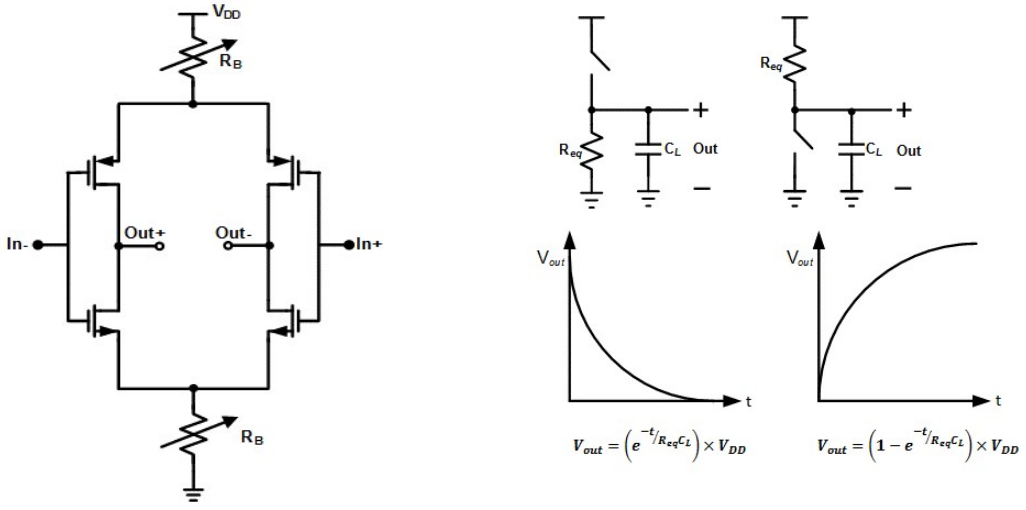


Figure 4.6 Simulated operation of the divide-by-2

4.3 Sampling Buffer and SSPD

4.3.1 Sampling buffer

The divide-by-2 output is a square wave, exhibiting a high slew rate. The gain of the SSPD will be unnecessarily high due to the high slew rate of such a signal. A sampling buffer is placed before the sampler to reduce the slew rate of the signal, by limiting the rise and fall time of the signal. Figure 4.7(a) shows the schematic of the sampler buffer which is based on an inverter loaded with resistors. The rise and fall time of the output is determined by the equivalent RC time constant during switching of the inverter (Figure 4.7 (b)). Figure 4.8 shows the RC- waveform at the output of the SSPD buffer.



(a) (b)

Figure 4.7 Implementation of sampling buffer (a) schematic (b) operation

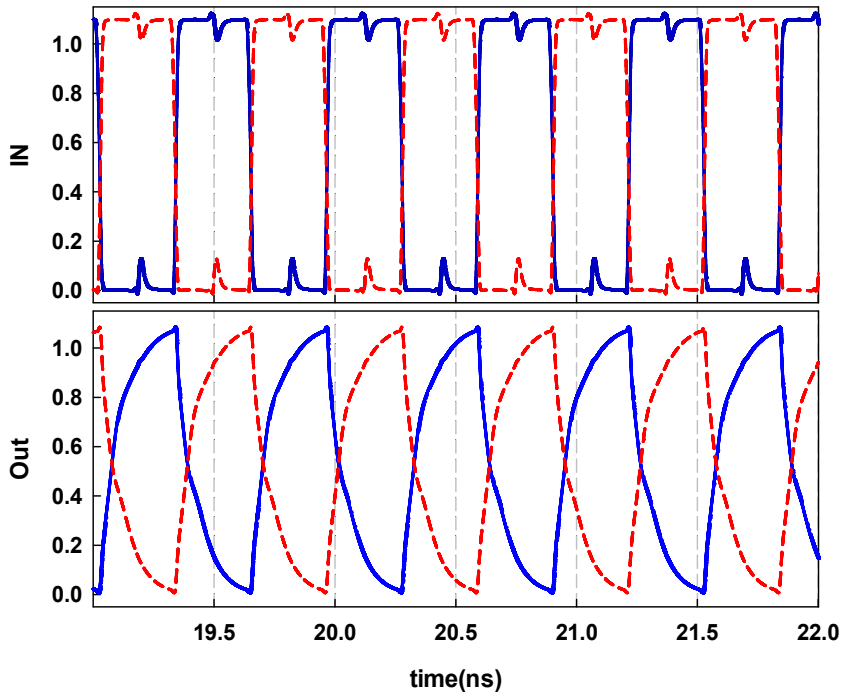


Figure 4.8 Simulation of the sampler buffer

4.3.2 SSPD

The sampler for the SSPLL is built with complementary CMOS switches and Metal-on-Metal (MOM) capacitors. Complementary switches provides a more linear switch resistance which reduces the non-linearity in the SSPD due to the switches. The total sampling capacitance value including the capacitance at the CP input is 100fF. The schematic implementation for the SSPD is shown in Figure 4.9.

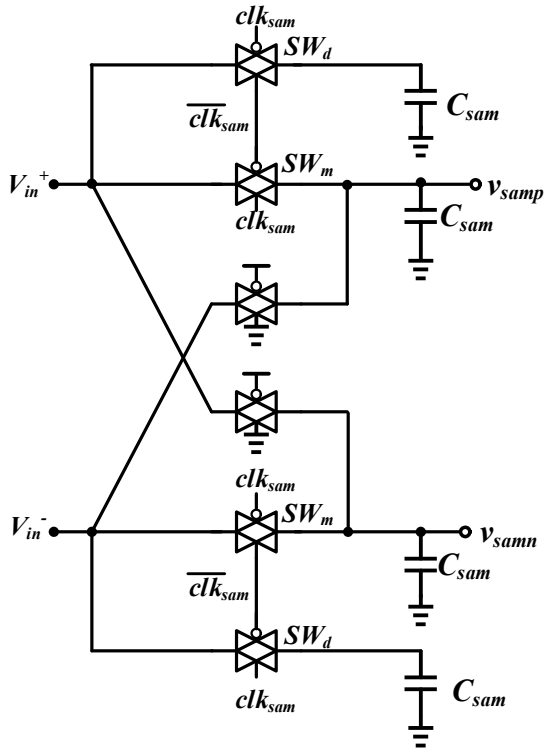


Figure 4.9 Implementation of SSPD

The phase noise contribution of the SSPD due to the sampler thermal noise is given as:

$$\mathcal{L}_{\phi,SSPD}(f) = 10\log\frac{kT}{C_{sam}\cdot A_{VCO}^2\cdot f_{ref}} \approx -142\ dBc/Hz \qquad (4.3)$$

For the targeted in band phase noise of -115dBc/Hz, the thermal noise contribution of the sampler is negligible and is further reduced by the large detection gain of the SSPLL. The SSPD incorporates an auxiliary sampler (which operates complementary to the main switches) and dummy switches to reduce the charge injection and sharing effect.

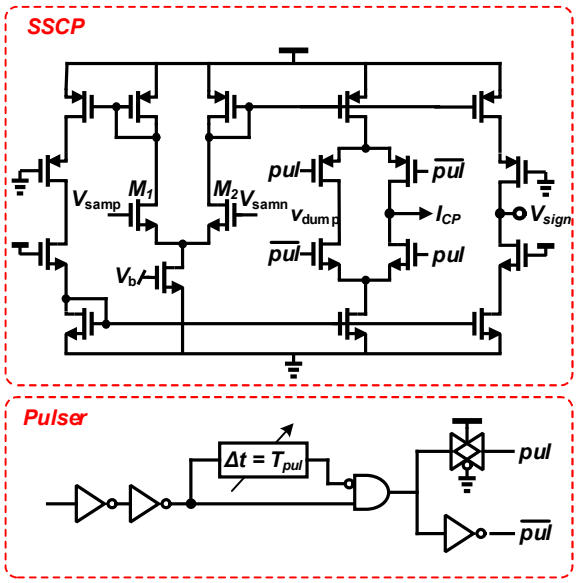


Figure 4.10 Schematic of SSCP and Pulser

4.4 SSCP and Pulser

Figure 4.10 shows the schematic of the implemented SSCP and pulser. The transconductance based SSCP consists of an input stage differential pair (M_1-M_2) followed by current mirrors to divert the current into the LPF. Similar to [6] the charge pump action is achieved with switches controlled by the pulser output signal *Pul*.

Charge sharing between the LPF and CP is mitigated by steering the current sources away to a voltage V_{dump} when Pul goes low. Unlike in traditional charge pumps a unity gain buffer is not required to keep this voltage equal to the loop filter input node voltage [46]. Both current sources have equal turn on times as such under locked conditions, their amplitudes must also be equal so that the net charge into the LPF is zero. This condition exists for both when the current sources are connected to the LPF and when

they are connected to V_{dump}. Since the current sources amplitudes are equal and their output impedances are finite, when the drain terminals of the PMOS and NMOS current sources are connected the two node voltages must be equal to ensure $I_{up} = I_{dn}$.

Figure 4.11 shows the simulated output current of the SSCP which is duty-cycled by the pulser action. In the ideal scenario, the direction of the PLL phase error can be derived from the sign of the sampled voltage. However any mismatches in the sampling loop circuitry (VCO, divide-by-2, buffers, SSPD and the SSCP) will cause SSPLL to

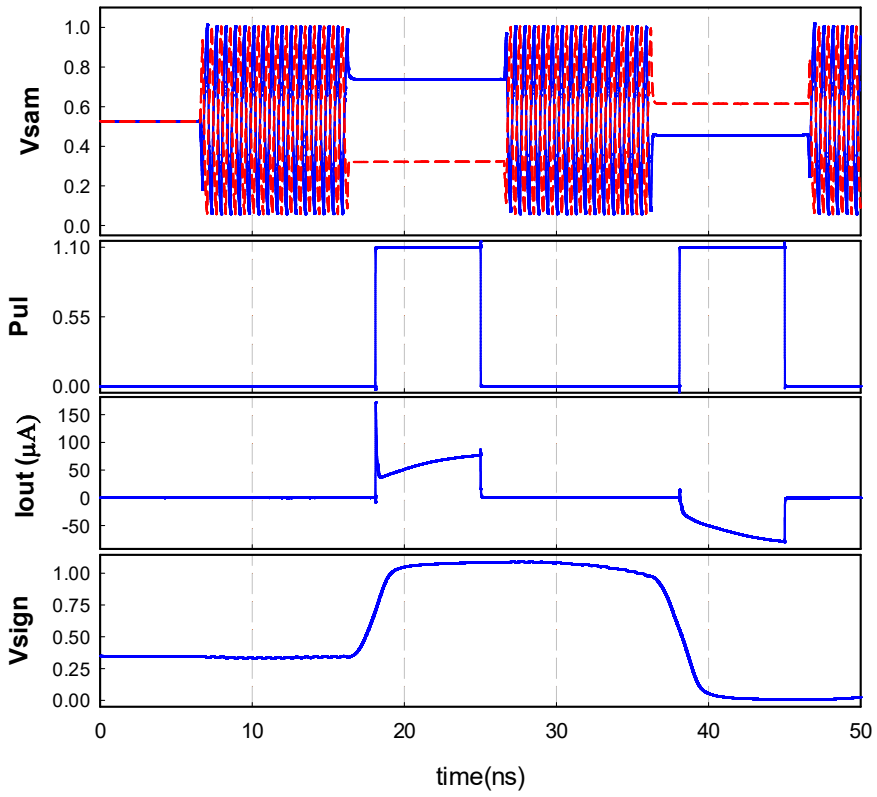


Figure 4.11 Transient simulation of the SSPD/CP action

adjust the locking phase so that the output current of the SSCP is zero. Therefore, the phase error sign needed in the delay correction loop can be derived from the sign of the SSCP current. Any slight imbalance in the current of the output branch results in a large voltage swing at the node V_{sign}.

The PLL loop gain is proportional to the width of the pulser signal which is determined by the delay in the pulser τ_{pul}. The pulser delay element is implemented with a programmable delay such that the PLL loop bandwidth can be tuned for optimal performance. Figure 4.12 shows the programmable delay line used in the pulser.

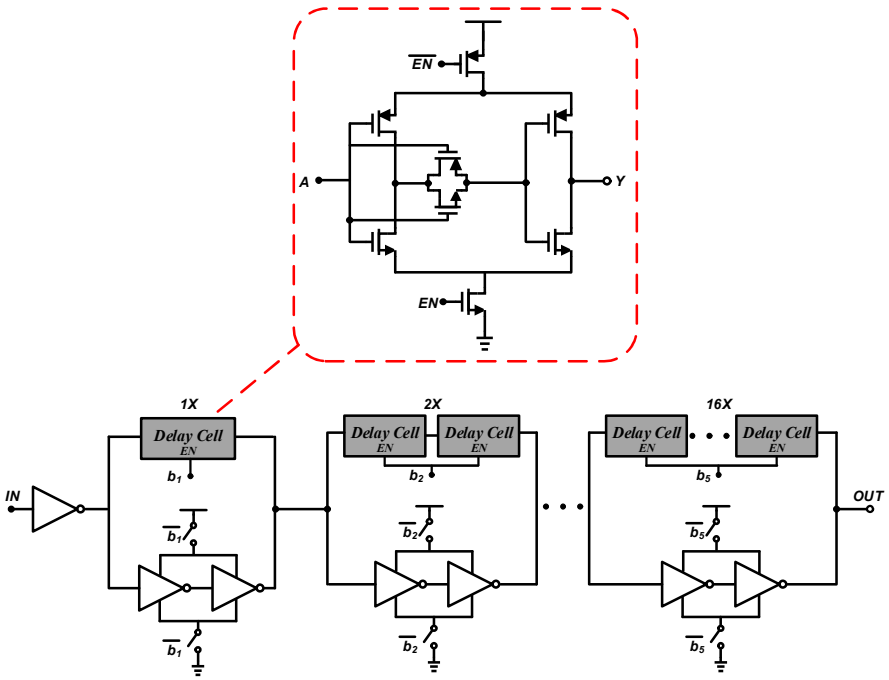


Figure 4.12 Programmable delay used in pulser

4.5 Frequency Locked Loop

A frequency locked loop (FLL) is used to prevent false locking of the SSPLL. The FLL is implemented with a modified three state PFD to incorporate a large dead zone which controls a simple charge pump and a multi-modulus programmable divider

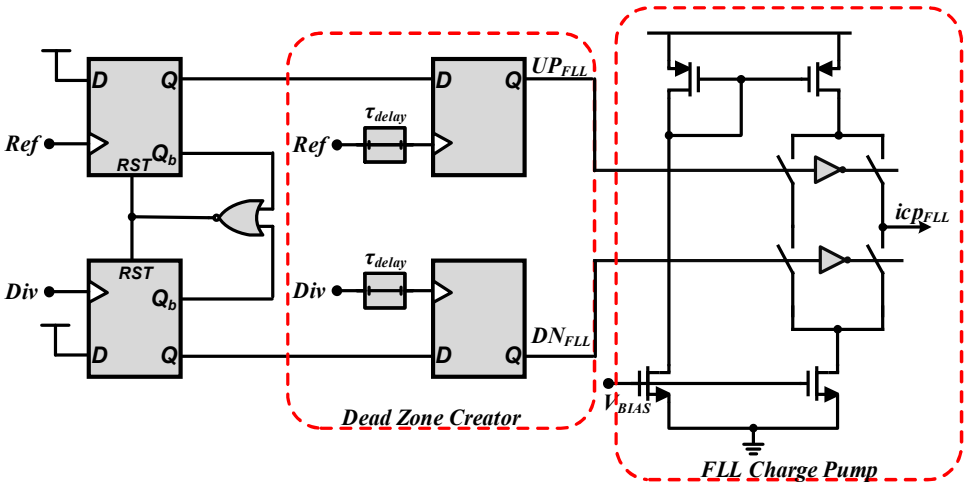


Figure 4.13 PFD with dead zone and charge pump for FLL

4.5.1 Three state PFD with dead zone and charge pump

Figure 4.13 shows the implementation of the PFD with dead zone and charge pump for the FLL. In the modified PFD the UP and DN pulses of the traditional 3-state PFD are resampled with D flip-flops triggered by delayed versions of the Ref and Div. The resampling occurs τ_{delay} after the rising edge as a consequence the UP and DN pulses with widths less than τ_{delay} are filtered out creating a dead zone of $\pm\tau_{delay}$. In Figure

4.14 the simulated timing of the modified PFD when Ref leads (Figure 4.14(a)) and when Ref lags (Figure 4.14 (b)) is shown. Within the dead-zone the gain of the PFD (and hence the FLL) is zero as shown in the characteristics plot in Figure 4.15.

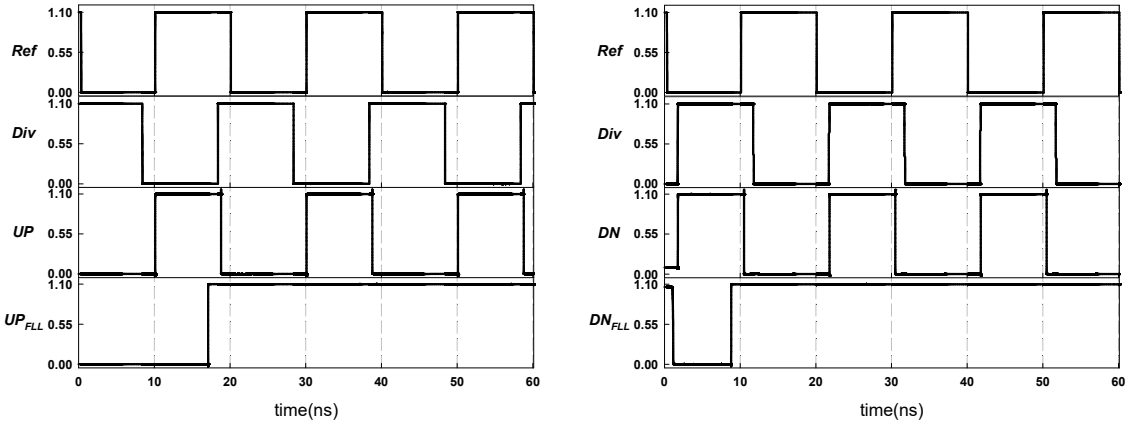


Figure 4.14 Timing diagram for PFD with deadzone (a) Ref leads Div (b) Ref lags Div

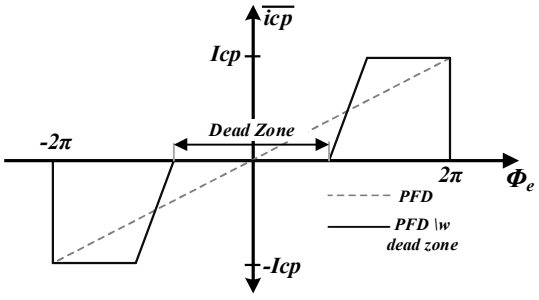


Figure 4.15 Characteristics of PFD with dead zone

4.5.2 Programmable divider

The multi-modulus divider for the FLL is based on the pulse swallow architecture. It consists of a divide by $N/(N+1)$ prescaler (where $N = 3$ in this case), a program counter (P-Counter) and a swallow counter (S-Counter). The S-Counter provides the modulus control (MC) of the prescaler which determines whether the prescaler divides by N or by N+1. The S-Counter sets the prescaler to divide by (N+1) for S counts. For the remaining (P-S) counts the prescaler is set to divide by N. Thus the overall divide ratio, $N_{int} = (N+1)S + (P-S)N = NP + S$.

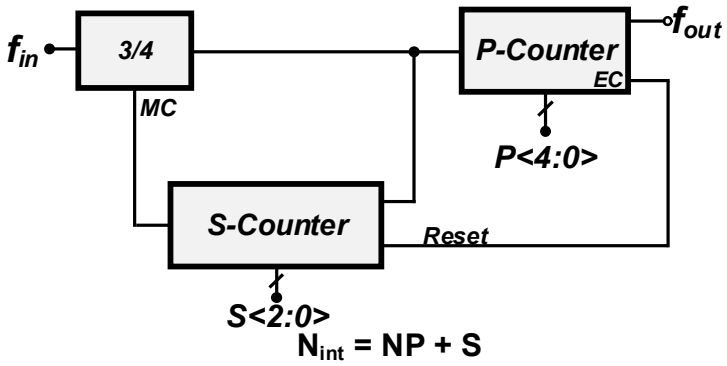


Figure 4.16 Pulse-swallow divider

Dual modulus prescaler

Figure 4.17 shows the schematic for a divide-by-3/4 prescaler. The instantaneous division ratio is set by the MC input. The output of the OR gate is always '1' when MC=1, allowing the AND gate to pass the output of the DFF_A to the input of DFF_B. Since each

DFF consists of 2 latches, the circuit then consist of 4 latches in a loop and performs a divide by 4 function. When MC=0, the circuit is reduced to perform a divide by 3 function. Figure 4.18 shows the simulated operation of the prescaler.

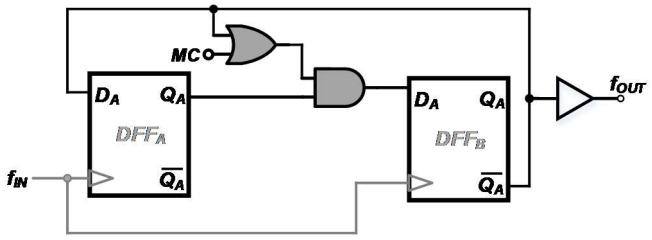


Figure 4.17 Divide-by-3/4 dual modulus prescaler

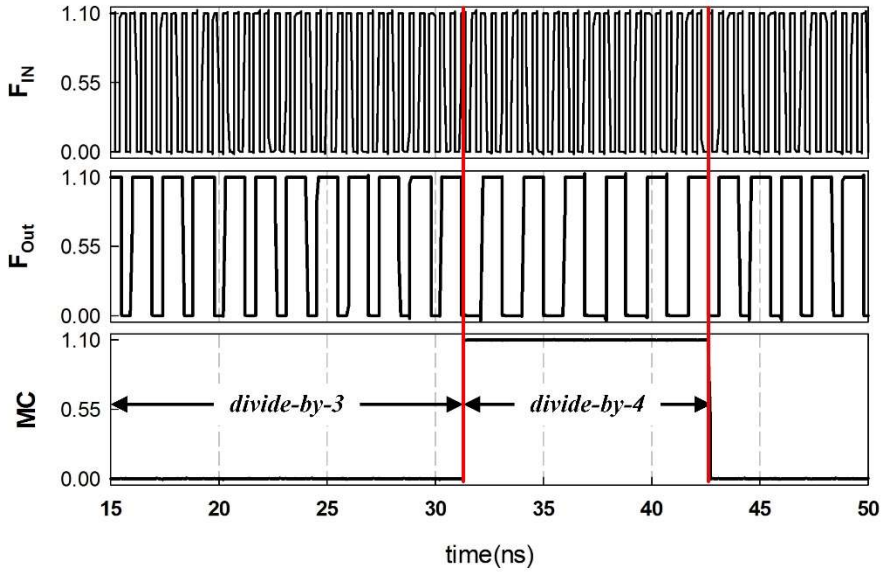


Figure 4.18 Prescaler operation: prescaler divides by 3 when MC=0 and divides by 4 when MC=1

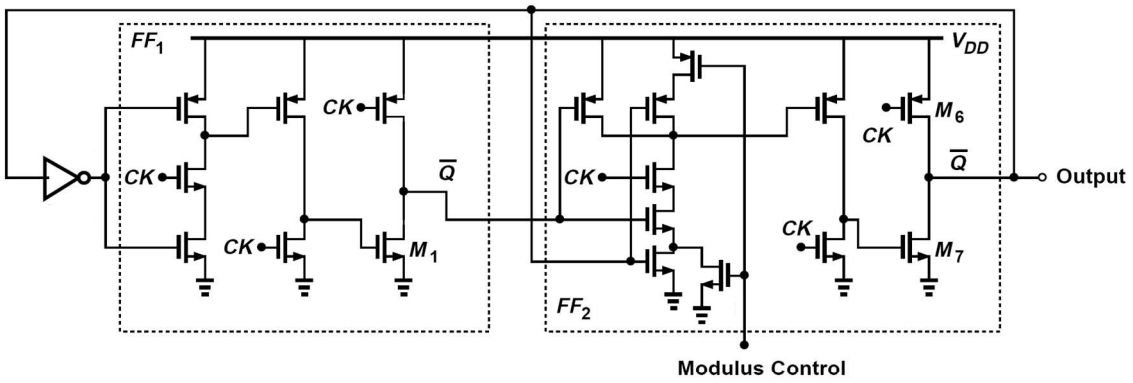


Figure 4.19 Transistor implementation of divide-by 3/4 prescaler

To maximize the operating speed of the prescaler, it is implemented with a TSPC [55] based architecture as shown in Figure 4.19. TSPC architectures are compact in size and consume no static power and thus are capable of operating at relatively high speeds with minimum power dissipation. However dividers based on such dynamic logic topologies can fail at low clock frequencies due to leakages of the transistors; in such topologies various nodes are floating during different clock and output phases [22].
To further improve the speed of the divider, the AND and OR functions are merged with the FFs.

Program counter

The program counter is designed as a 5-bit asynchronous counter for simplicity and low power as shown in Figure 4.20. The cascade of divide-by-2 stages count the clock pulses (CLK) up to the value set at the input of the P-Counter. Once the count is complete, the end-of-count node EC goes low and the stages are reset on the next clock cycle.

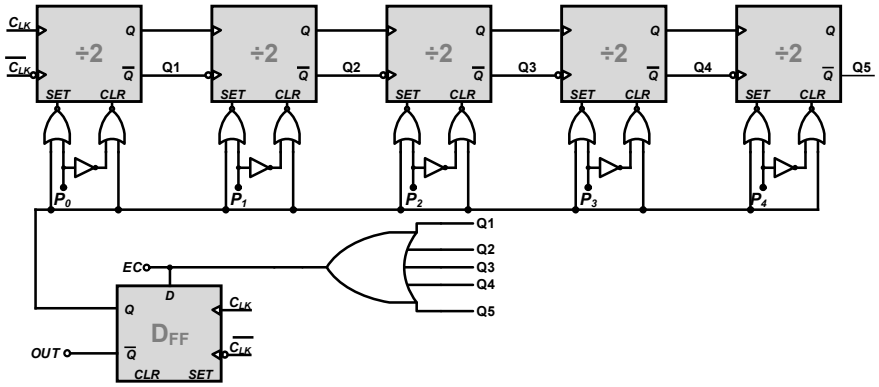
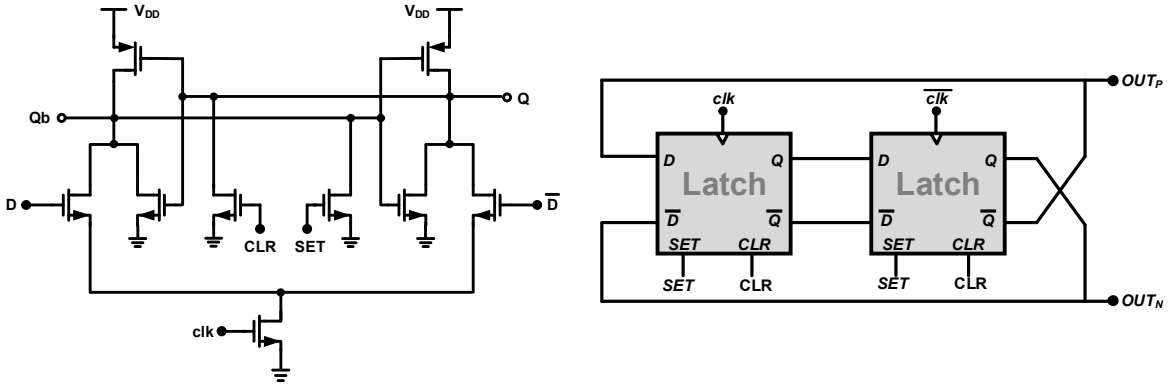


Figure 4.20 Schematic of the program counter

For instance if the counter input is set to 22, (10110_2) then the counter counts form 22→0, a total of 23 input pulses. Each divide-by-2 stage consist of 2 dynamic differential cascode voltage switch logic (DCVSL) latches [54] connected in negative feedback. Figure 4.21 shows the implementation of the dynamic DCVSL latches and the divide-by-2 circuit.



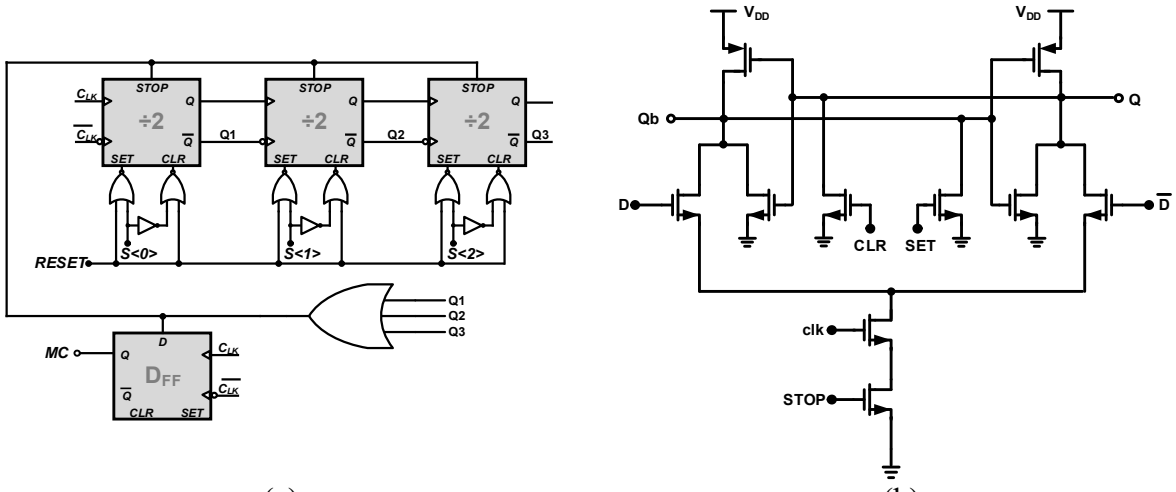
(a) (b)

Figure 4.21 Implementation of (a) dynamic differential cascode voltage switch logic (DCVSL) latch and (b) divide-by-2 circuit for Program counter

Swallow counter

The swallow counter is implemented as a 3-bit asynchronous counter similar to the P-Counter (Figure 4.22 (a)). The counter counts down from its initial value (determined by the inputs to S<2:0>) to zero, during which MC=1. After the initial count, the S-Counter changes MC=0 and stops counting. The S-Counter is reset when the Program counter fills up. The differential DCVSL latch used in the S-Counter divide-by-2 stages is shown in Figure 4.22(b). The circuit is modified from the DCVSL latch in Figure 4.21 (a) to implement the stop function required in the S-Counter.

A simulation of the programmable divider for a divide-by-51 operation is shown in Figure 4.23.



(a) (b)

Figure 4.22 (a) Swallow counter schematic (b) Differential DCVSL latch used in the S-Counter

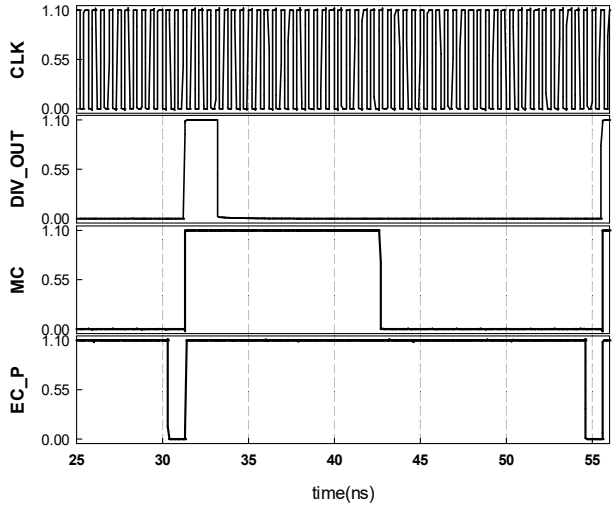


Figure 4.23 Divide-by-51 operation of the Frequency Divider

4.6 Dual Input Loop Filter

The SSPLL and FLL charge pump currents are applied to different nodes of the loop filter. This allows the location of the zeros of the two loops to be set independently resulting in additional freedom for bandwidth and phase margin optimization of both loops[3]. Figure 4.24 shows the schematic of the dual input loop filter (DILF).

The main filter consists of the resistors R_1 and R_2 and capacitors C_1 and C_2. R_3 and C_3 are included to provide further spur reduction in the FLL and are by passed when the SSPLL is operating. The trans-impedance of the loop filter from the FLL charge pump to the tuning voltage node $Z_{LF,FLL}\ (s) = V_{tune} / I_{cp,FLL}$ and form the SSPLL charge pump output to the tuning voltage node $Z_{Icp,SSPLL}\ (s) = V_{tune} / I_{cp,SSPLL}$ are given as:

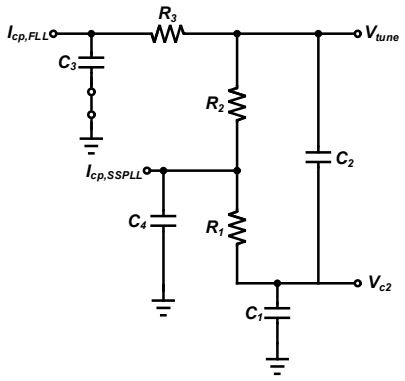


Figure 4.24 Schematic of the dual input loop filter

$$Z_{LF,FLL}\ (s) = \frac{1 + \mathrm{s}(R_1 + R_2)(C_1 + C_2)}{s(C_1 + C_3) \cdot p_2(s\ )} \tag{4.4}$$

$$Z_{LF,SSPLL}\ (s) = \frac{1 + s\big(R_1C_1 + C_2(R_1 + R_2)\big)}{(s(R_1 + R_2)C_2 + 1\ )sC_1} \tag{4.5}$$

where

$$p_2(s\ ) = 1 + \frac{sC_1}{C_1 + C_3}\left((R_1 + R_2 + R_3)C_3 + \left(1 + \frac{C_3}{C_1}\right)\big((R_1 + R_2)C_2\big)\right) + s^2\,\frac{(R_1 + R_2)R_3C_1C_2C_3}{C_1 + C_2} \tag{4.6}$$

Assuming $C_1 \gg C_2, C_1 \gg C_3$ and $R_3 \gg (R_1 + R_2)$

$$Z_{Icp,FLL}\ (s) \approx \frac{1 + \mathrm{s}(R_1 + R_2)(C_1 + C_2)}{sC_1(1 + s(C_3R_3 + C_2(R_1 + R_2)) + s^2\ (R_1 + R_2)R_3C_2C_3)} \tag{4.7}$$

During frequency acquisition the loop filter zero is approximately $1/2\pi\ ((R_1 + R_2)(C_1 + C_2))$ and is set to a lower frequency is set to a lower frequency (due to the relatively smaller detection gain) to ensure stability and fast tuning the phase margin. The

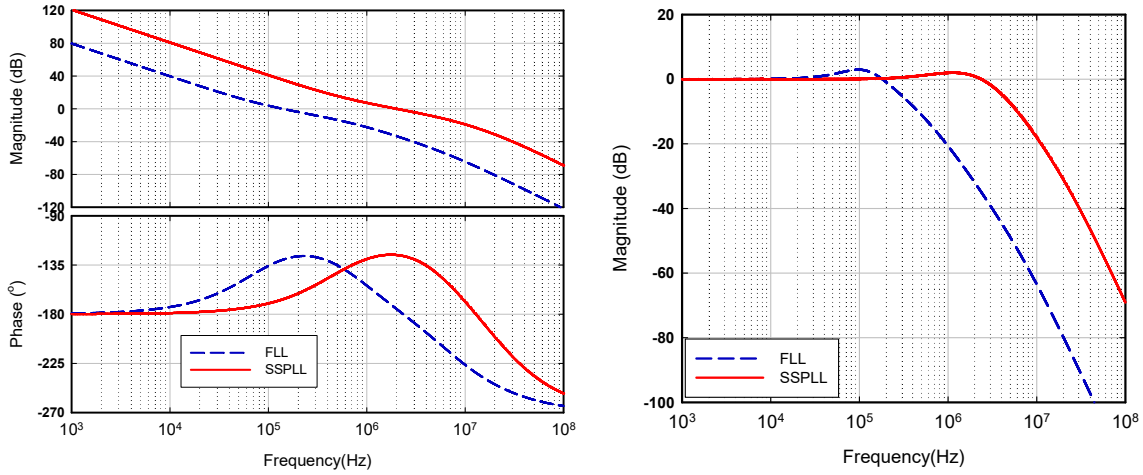
zero for the subsampling loop is set to a higher frequency to allow for optimum bandwidth-jitter trade-off to be achieved after locking. To allow for further optimization after fabrication the loop filter resistors are made programmable.

The open loop transfer functions of the two loop as given as

$$A_{FLL}(s) = K_{PFD}\, Z_{LF.FLL}(s)\, \frac{K_{VCO}}{s}\, \frac{1}{2 * N} \tag{4.8}$$

$$A_{SSPLL}(s) = \frac{1}{2} K_{SSPD}\, Z_{LF,SSPLL}(s)\, \frac{K_{VCO}}{s} \tag{4.9}$$

The open loop and closed loop frequency response for both loops are shown in Figure 4.25 (a) and Figure 4.25(b) respectively. Both loops achieve a phase margin better than 51°.



(a) (b)

Figure 4.25 Frequency response of the FNSSPLL (a) open loop response (b) closed loop response

Table 4.2 Loop parameters for the PLL

Loop Parameters			**Passive Elements**	
Reference frequency	50MHz		R_1	940Ω
KVCO	20MHz/V		R_2	5 kΩ
N	32-50		R_3	35 kΩ
K	600μA/2π	2*50uA/V	C_1	335pF
Loop Bandwidth (f_c)	154kHz	2MHz	C_2	3.8pF
Phase Margin	51	54	C_3	5pF
			C_4	9.5pF
			C_{TOTAL}	353.3pF

The loop parameters and filter components are given in Table 4.2. The total integrated capacitance for the DILF is 353.3 pF. The SSPLL nominal loop bandwidth is 2 MHz but is programmable by changing the bit settings of the loop filter resistors and the SSCP pulser.

4.7 Digital Fractional Control (DFC)

Figure 4.26 shows the block diagram of the DFC. The overflow of the phase accumulator is used to control the PS divider in the FLL to aid frequency locking; the divider value is set to (-1) when there is an overflow and N_{int} otherwise. Similar to the basic fractional N technique described in section 2.5.1, the average divider value is given as:

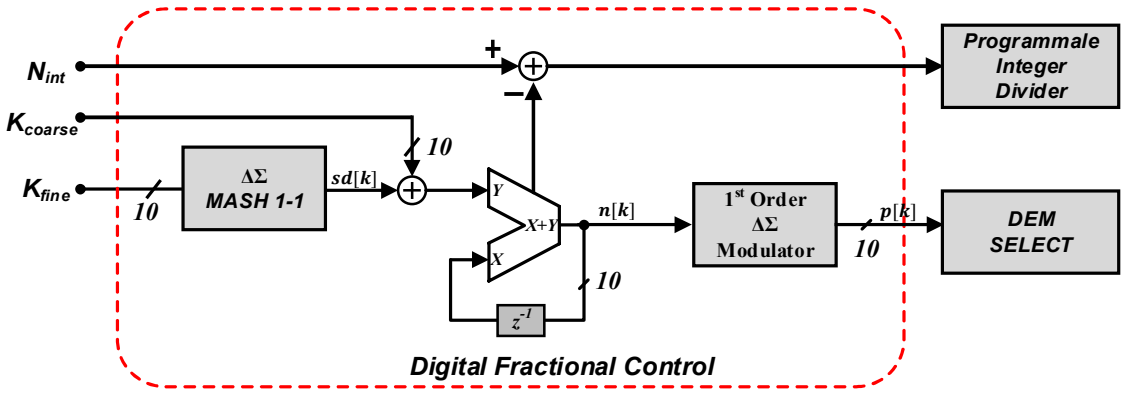


Figure 4.26 Block diagram of the digital fractional control

$$N_{avg} = \frac{(2^{10} - K) \cdot N + K \cdot (N - 1)}{2^{10}} = N + \frac{K}{2^{10}} = N - \alpha \tag{4.10}$$

where $K = k_{coarse} + \frac{k_{fine}}{2^{10}}$

Thus the FLL will aide frequency locking to the required fractional value.

4.7.1 MASH 1-1 SDM

The architecture of the MASH 1-1 SDM is shown in Figure 4.27. The system consists of a cascade of two digital accumulator. Each of the accumulators is made up of a 10 bit carry look ahead (CLA) adder.

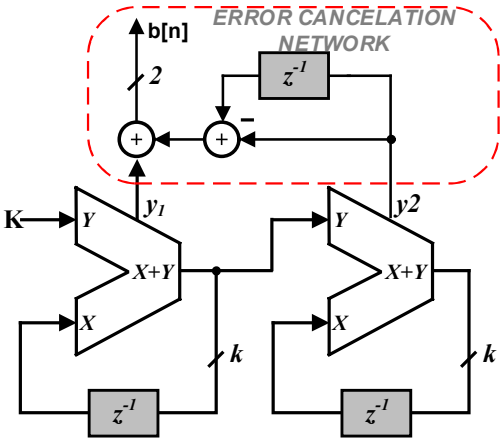


Figure 4.27 MASH 1-1 architecture for SDM

Table 4.3 Output coding for MASH 1-1

Output Level	b_3	b_2	b_1
-1	1	1	1
0	0	0	0
1	0	0	1
2	0	1	0

Compared to conventional ripple adders, CLA are faster since they make use of propagate and generate signals to determine the carry out signal[56].The output of the SDM is a signed 2-bit number based on two's complement [25] for its ease of implementation. The SDM therefore has 4 output levels from -1 to +2. The output coding for the MASH modulator is shown in Table 4.3. To avoid an overflow in at the summing node at the input of the accumulator the minimum value of K_{coarse} is constrained to 1. A sample simulated response of the DFC is shown in Figure 4.28

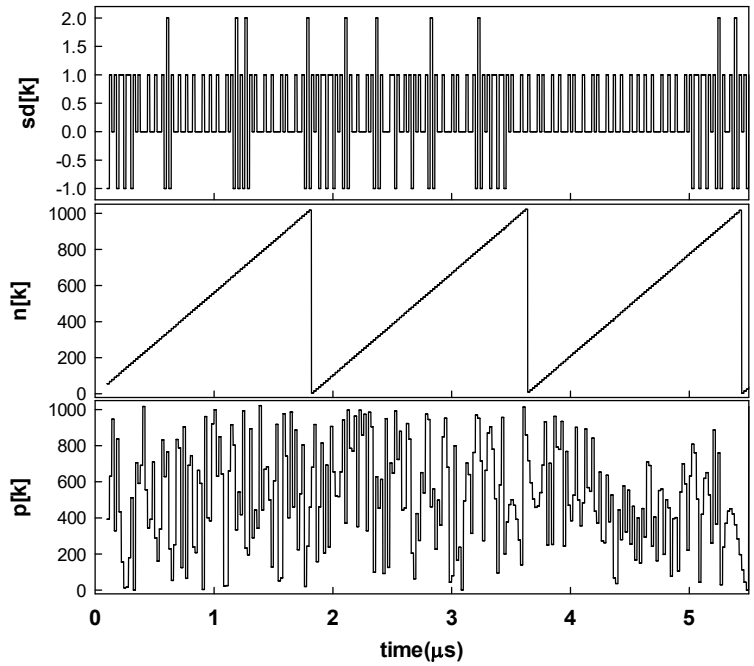


Figure 4.28 Simulation results of the DFC $k_{fine} = 313$, $k_{coarse} = 1$

4.7.2 Digital design flow

The entire digital fractional control and DEM select circuit were implemented using the digital design flow in Figure 4.29. The high level system simulations are done using MATLAB and Cppsim [57]. Cppsim is based on the C++ language and employs techniques that enable fast and accurate simulations of fractional-N synthesizers at a detailed behavioral level [57] and works well with the MATLAB framework. The Cppsim/MATLAB framework provides a good estimation of both the dynamic and spectral purity performance of PLL based systems.

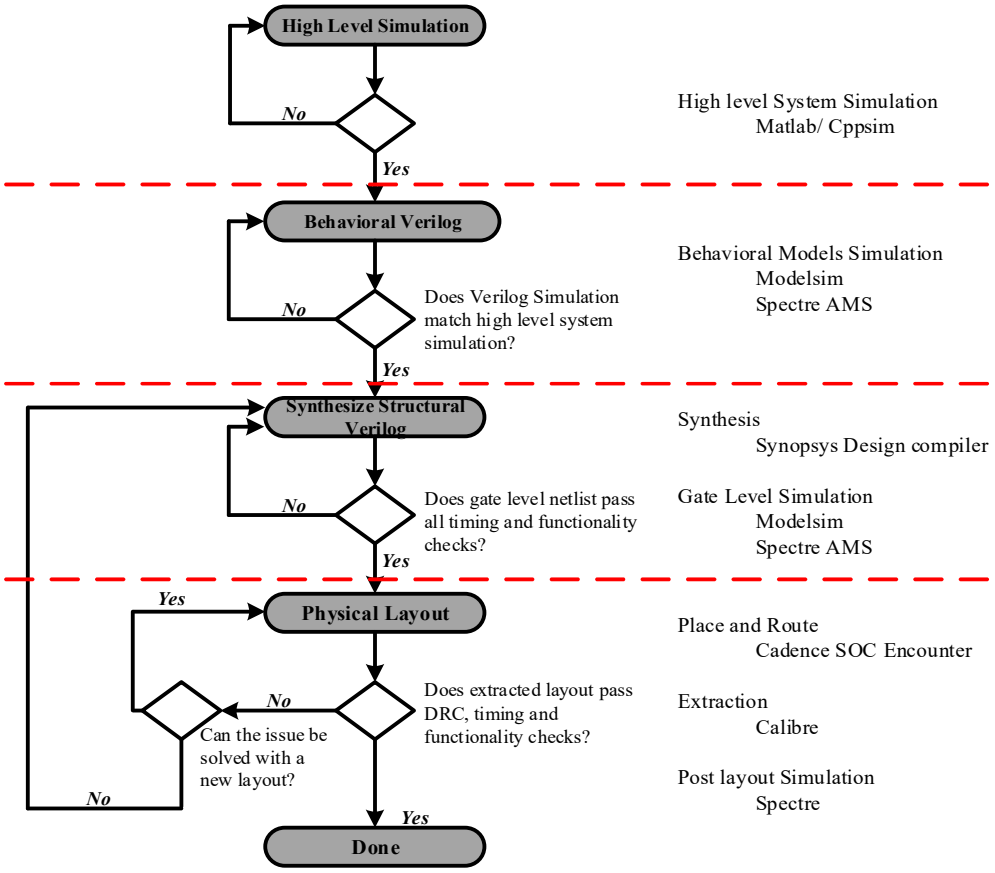


Figure 4.29 Digital design flow

Based on the insight from the high level simulations, we then develop behavioral Verilog models that achieve the required system performance. During this stage practical non-idealities such as gate delays and finite precision calculations are added to the model to investigate their impact on the system.

The functionally verified Verilog behavioral descriptions are then translated into a physical layout. In order to reduce the wiring between the various analog and digital sections, the digital control layout was split into the DFC and the DEM select circuit.

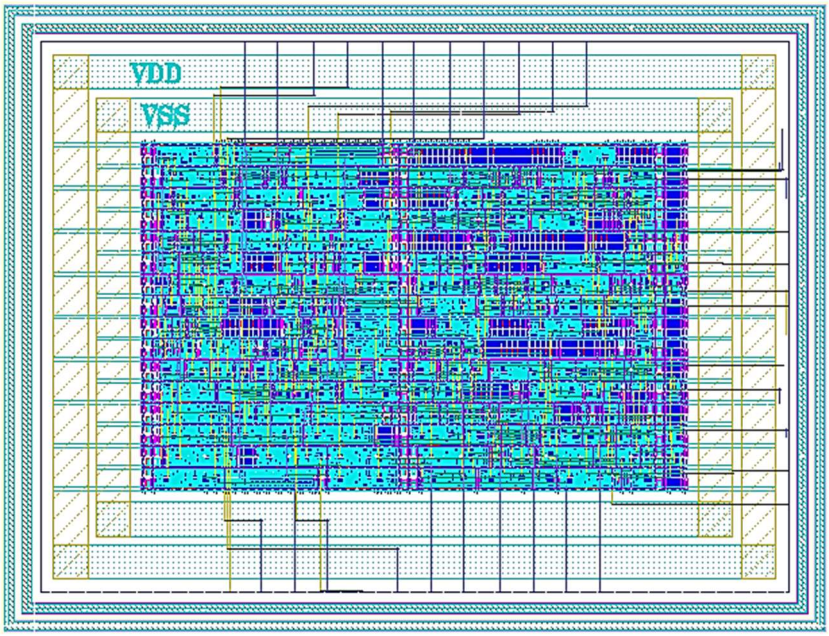


Figure 4.30 Generated layout of the DFC

Both subsystems were fully synthesized with the digital design flow. After the digital parts have been synthesized mixed signal simulations are performed to ensure that the digital and analog sections are correctly interfaced before we generate the physical description of the circuits

An automatic place and route tool, Cadence SOC Encounter, is used to generate the physical layout of the digital blocks. The tool generates a required floor plan and places the gates in a manner optimized for area, routing and delay. Figure 4.30 shows the final layout of the DFC generated from the Place and route tool.

The final step in the digital design flow is to generate a netlist based on the extracted values form the physical layout for simulation. However such simulation require a lot of

processing resources and time. For instance while simulation of the digital modulator at the structural Verilog level takes a few minutes to complete, the extracted netlist of the same block requires over 32 hours to complete. However such simulation are required since a large percentage of signal delays occur in the routing network.

4.8 Edge Modulator

4.8.1 DTC

A 10-bit DTC with a resolution of 0.2ps is implemented to cover the needed VCO periods and to reduce the output spurs due to the finite delay resolution. Due to the large number of bits, the DTC is implemented as a single digitally controlled delay cell as shown in Figure 4.31.

A chain of inverters at the input of the DTC serve as the reference buffer to convert the sine wave of the reference crystal oscillator to a steep square wave. The buffered reference serves as the input to the delay circuit which is loaded with a 10-bit MOM capacitor array. The capacitor array is controlled by the DFC output which selects the needed number of capacitor to achieve a required delay.

Similar to the reference noise, the device noise of the DTC appears at the input of the PLL and as such is multiplied by N^2. The phase noise due to the inverter based delay cell is given by [20]:

$$\mathcal{L} = \frac{S_\phi}{2} = 10\log\left[4\pi f_{ref} \cdot \frac{2kTC}{I_B^2}\right] dBc/Hz \tag{4.11}$$

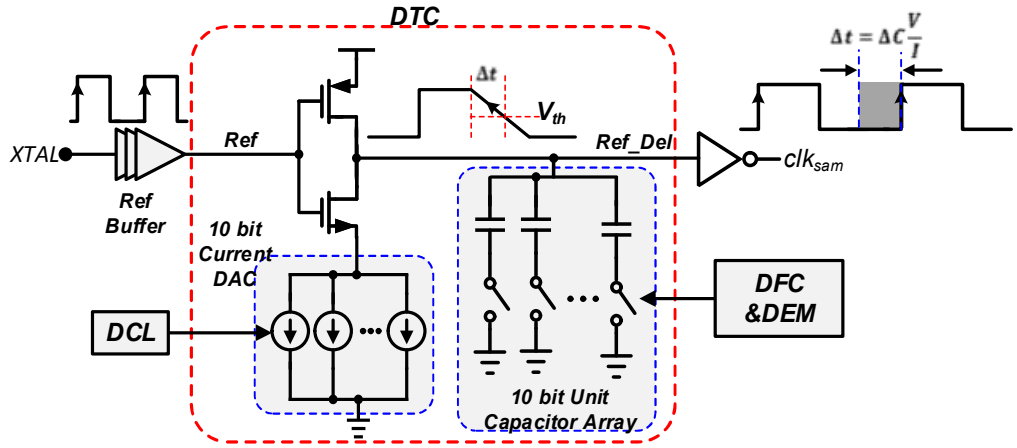
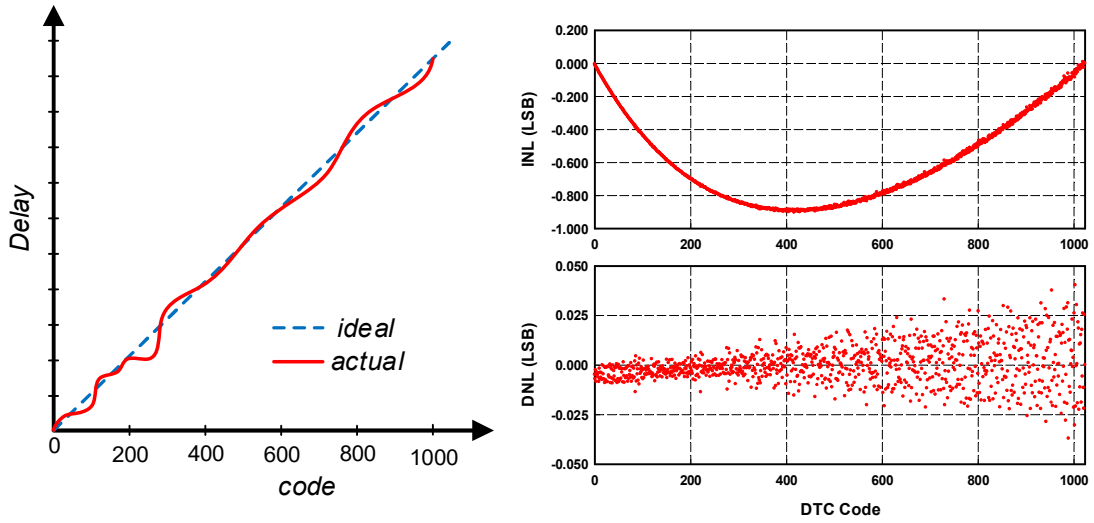


Figure 4.31 Schematic of the DTC

Unlike conventional DLL schemes the delay range of a single delay cell varies considerably over PVT variations deviating from the needed delay range of $2T_{VCO}$. Further, since the VCO covers a wide tuning range the DTC range must track the desired VCO frequency. As such a 10-bit current DAC controlled by a delay correlation loop (DCL) is used to regulate the DTC delay range. The delay generated is given by:

$$\Delta t = \Delta C \frac{V}{I_{DAC}} \tag{4.12}$$

where Δt is the delay associated with DTC and I_{DAC} is the current from the current DAC. Based on simulations, the size of the unit capacitor is chosen as 9fF and the full scale DAC current 850µA. The DTC phase noise for a 50-MHz reference signal is below -160 dBc/Hz at a 200 kHz offset. For a 3.5 GHz output the DTC noise contribution at the PLL output is better than -125dBc/Hz which is low enough not to affect the targeted noise performance.



(a) (b)

Figure 4.32 (a) cumulative non-linearity in the DTC and (b) post layout Monte-Carlo simulation for DTC nonlinearity ($LSB = 0.25ps$)

The single-cell DTC shown in Figure 4.31 suffers from two main sources of nonlinearity: (a) the random mismatch in the capacitance values of the capacitor array and (b)the nonlinearity of the *delay-vs-capacitive-load* characteristics; the delay of a simple CMOS inverter does not vary linearly as a function of the output capacitance [58]. The cumulative effect of these non-linear effects on the DTC characteristics is shown in Figure 4.32(a)

To cancel out the mismatch errors due to process gradient variations the capacitor array is laid out in a common-centroid scheme and the capacitor array selection is done through a dynamic element matching (DEM) algorithm to reduce the effect of the mismatch based error. Figure 4.32 (b) shows the post layout INL and DNL simulations

for the DTC with an LSB of 0.25ps. The absolute value of INL is better than 1 LSB and the DNL is better than 0.05 LSB.

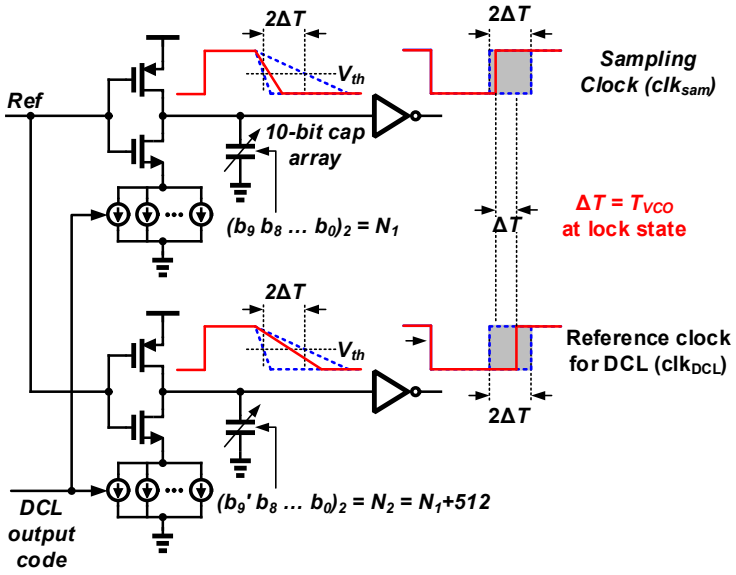


Figure 4.33 Schematic of edge modulator (DTC and replica DTC for DCL)

A replica DTC is used to generate a delayed version of the sampling clock. By inverting the MSB of the DFC code and applying this to the capacitor array of the replica, the delay between the sampling clock clk_{sam} and the replica clock clk_{DCL} ΔT represents half the delay range of the modulator (Figure 4.33). The delay ΔT is used in the DCL to regulate the delay range of the main DTC.

4.9 Dynamic Element Matching

Due to PVT variations and the fabrication process the values of the unit capacitor in the DTC capacitor array slightly differ from their nominal values. The deviation in capacitor value is not uniform especially for such a wide capacitor array.

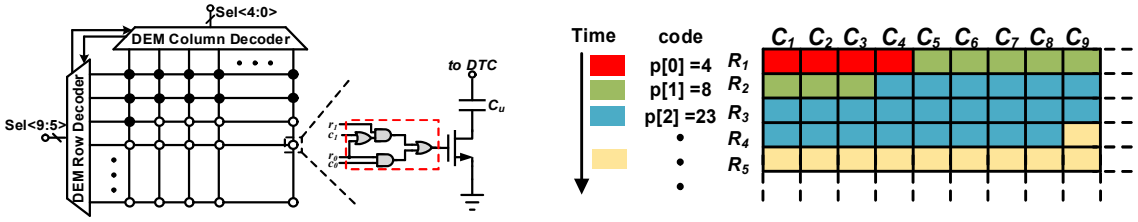
Dynamic element matching techniques [51] have been widely employed in DAC to improve their mismatch performance. The aim of DEM techniques is to select the nominally matched elements such that errors due to mismatches are modulated away from the desired signal frequencies. DEM techniques are widely preferred due to their simplicity and cost-effective implementation. It has been shown that cyclic cell selection also referred to as Data weighted averaging (DWA) DEM can shape mismatch error with a first-order noise shaping [51]. The DWA technique is achieved by selecting the array elements in such a way that all the elements are used equally. The DWA algorithm is chosen for this work due to its ease of implementation.

The algorithm requires a digital register pointer whose current value $ptr[k], 0 \leq ptr[k] < N$ is the address of the last cell selected in the array. At each clock cycle the pointer value is incremented modulo N by the input code.

$$ptr[k] = (ptr[k-1] + p[k])_{mod\ N} \tag{4.13}$$

At a given time k the cells between $ptr[k-1]$ to $ptr[k]$ are selected; the cells selected are $\begin{cases} ptr[k-1], ptr[k-1]+1, \dots ptr[k]-1, & ptr[k-1] \leq ptr[k] \\ ptr[k-1], ptr[k-1]+1, \dots N-1, 0, 1 \dots ptr[k]-1, & ptr[k-1] > ptr[k] \end{cases}$

The schematic for the DEM select block and an example of the selection of the capacitance array is shown in Figure 4.34(a) and (b). The capacitor selection starts from the preceding unselected one.



(a) (b)

Figure 4.34 (a) Schematic of DEM and (b) example selection sequence of the DEM

4.10 Delay Control Loop

Gain errors in the modulator lead to erroneous currents from the SSCP which periodically modulate V_{ctrl}, leading to large spurious contents. A 10-bit current DAC controlled by the DCL output is used in the modulator to regulate the delay range and compensate for gain errors. Figure 4.35 shows the schematic of the DCL with 2 step delay calibration.

In the first step, ΔT is compared with Tvco and a successive approximation register (SAR) control logic is used to find the best setting for the DAC to ensure ΔT is tuned to Tvco. To this end, two pulses are first generated with width of ΔT and T_{VCO} employing two PDs and two DFFs (Figure 4.35). Theses pulses are then applied to two CPs to generate a current proportional to the applied pulse width into the integrating capacitors. Finally, a comparator detects the voltage difference on CP's outputs after N reference cycles and the result is applied to a SAR control logic block which sets the DAC code accordingly. After the comparison is done, the capacitors are discharged for the next comparison cycle.

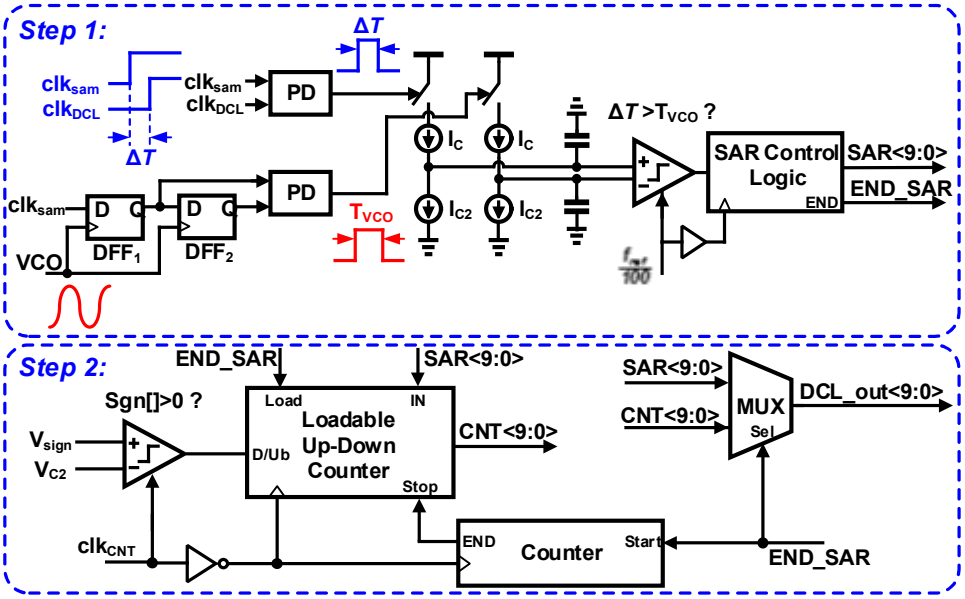


Figure 4.35 Schematic of the two-step DCL

In this design, Ic2 is chosen to be much smaller than Ic and is used to reduce the common-mode voltage on charge pump's outputs at each reference cycle. This makes it possible to increase the number of cycles (N) over which the charge is accumulated in the capacitors, leading to higher sensitivity. The voltage difference on comparator's inputs (ΔV) after N reference cycles can be easily found as

$$\Delta V = (\Delta T - T_{VCO}) \frac{I_c V_{DD}}{2(I_c T_{VCO} - I_{c2} T_{ref})} \tag{4.14}$$

By properly choosing Ic2, the system sensitivity can be increased.

Any mismatches between the two edge modulators and also between the two CPs can degrade the sensitivity of the above calibration loop. To overcome this problem, the SAR code serves as a starting point for a second correction step which uses the phase error

sign (V_{sign}) from the SSCP and V_{c2} from the DILF to find the final optimum code for the DAC.

4.11 Settling Behavior

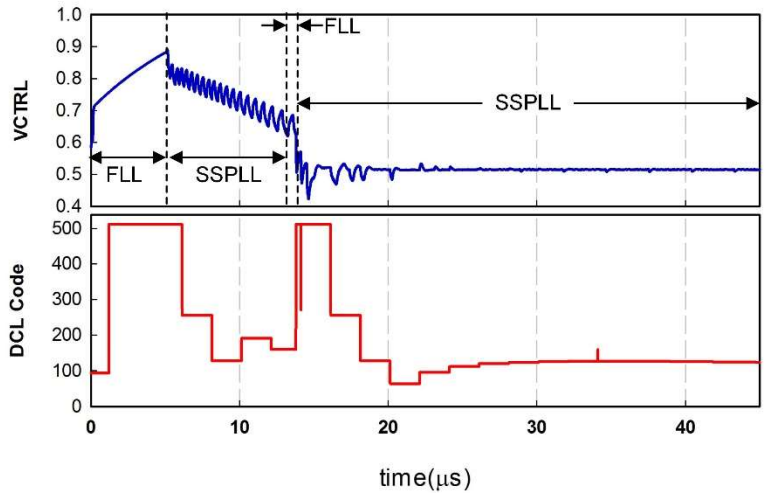


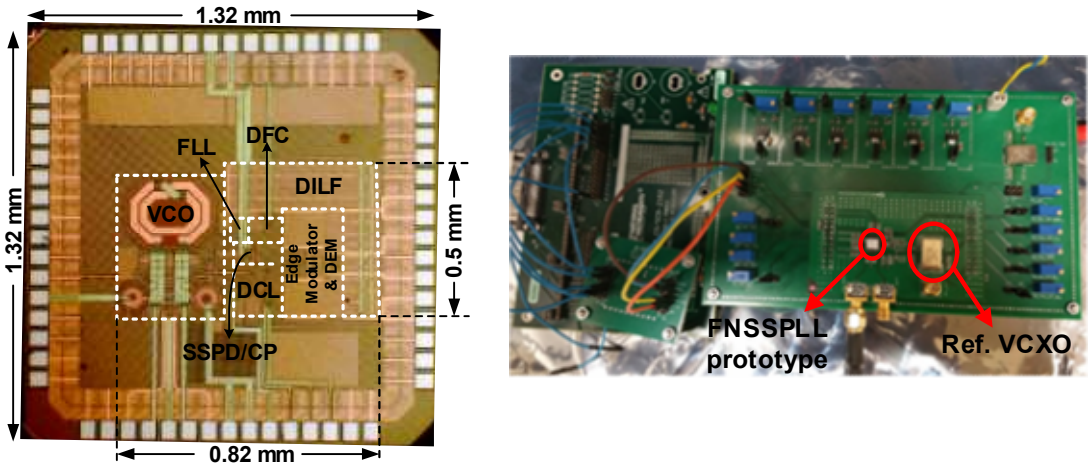
Figure 4.36 Settling characteristics of the PLL

The overall proposed architecture consists of multiple loops: the SSPLL core loop, the FLL and the DCL. The DCL loop does not affect the loop dynamics since its only function is calibrate out the errors in the unit delay of the DTC. Both the DCL and FLL are shutdown to conserve power after locking. Figure 4.36 shows the transient simulation for the entire system. During frequency acquisition, the phase error is large and the FLL dominates the loop dynamics. When the phase error is smaller than the deadzone, the FLL CP injects no current into the DILF and the SSPLL works to reduce the phase error.

From the system simulation the proposed architecture is capable of achieving lock within 25µs and the DCL loop converges within 30µs in the worst case.

4.12 Measurement Results

The proposed FNSSPLL was fabricated in a 40nm CMOS technology and packaged in a 36-pin QFN package. The chip occupies a total area of 1.32x1.32mm^2 including pads while the active area is 0.5 x 0.82mm^2 as shown in Figure 4.37(a). The chip is powered by a 1.1V supply. Excluding the VCO measurement buffer and powering down the FLL, the PLL consumes 9.18mW. The reference frequency is generated from a 50MHz ultra low noise sine wave crystal oscillator from Crystek. The VCXO has a noise profile of -170dBc/Hz at 100 kHz.



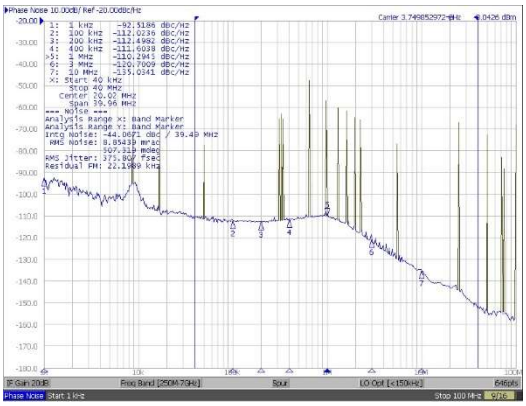
(a) (b)

Figure 4.37 (a) Chip micrograph (b) Fabricated PCBs and measurement setup

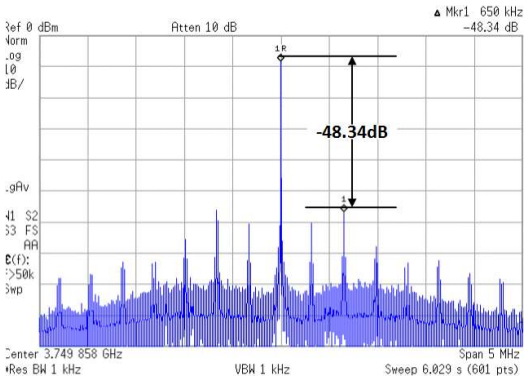
The different control bits of the prototype are set through a National Instruments PCI Data acquisition card. Figure 4.37(b) shows the fabricated PCBs and test setup for the chip measurements

4.12.1 Measured phase noise performance

Phase noise measurements were done using an Agilent E5052B signal source analyzer. The phase noise spectrum for a carrier frequency of 3.75 GHz showing the fractional-N spectrum with the worst case spur of -48.3 dBc at 650 kHz offset is shown in Figure 4.38(a) and (b).



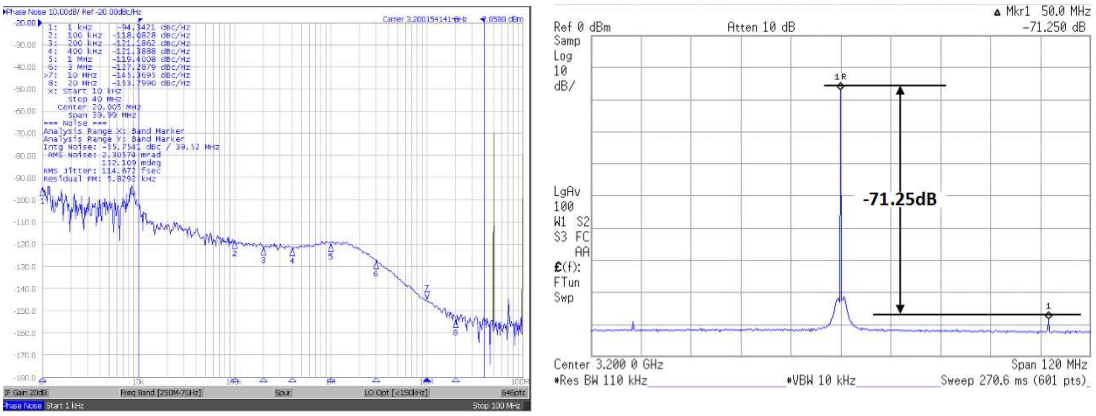
(a)



(b)

Figure 4.38 Measured (a) phase noise and (b) output spectrum of the PLL showing the worst case fractional spur

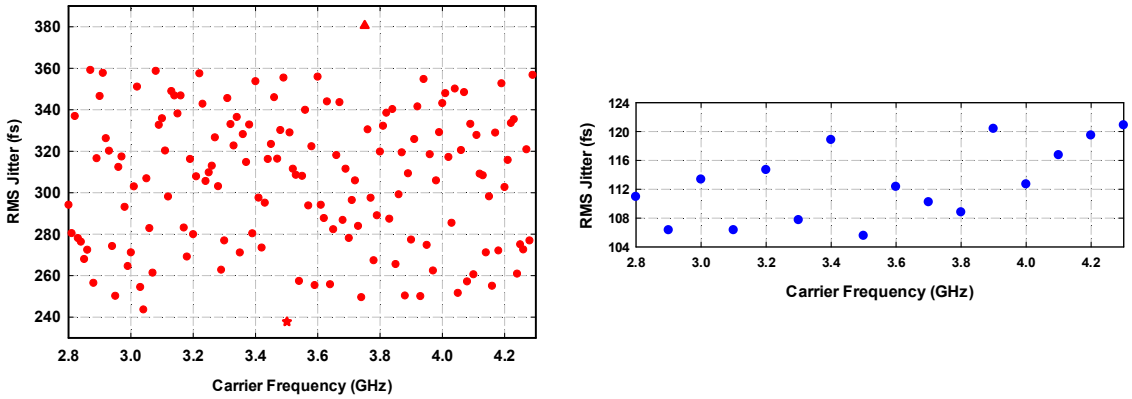
The in-band phase noise measured at 200 kHz offset is -112.5 dBc/Hz. In the integer mode, the synthesizer achieves an in-band phase noise of -121 dBc/Hz with a reference spur of -71.2 dBc as shown in Figure 4.39.



(a) (b)

Figure 4.39 Measured (a) Output spectrum and (b) phase noise measurement for the integer mode (3.2GHz)

Figure 4.40(a) shows the measured rms jitter across the fractional channels of the PLL. The rms jitter is between 238 fs and 390 fs. In the integer mode the rms jitter is better than 125 fs across the synthesizer tuning range. In both cases the integration for the rms jitter was done from 10 kHz to 40 MHz. In Figure 4.41 the spur performance and rms jitter are plotted against offset frequencies for the worst case fractional channel of 3.75GHz. The summary of measured results is presented in Table 4.4.



(a) (b)

Figure 4.40 Measured RMS jitter across (a) fractional-N channels and (b) as a function of the output frequency in the integer mode.

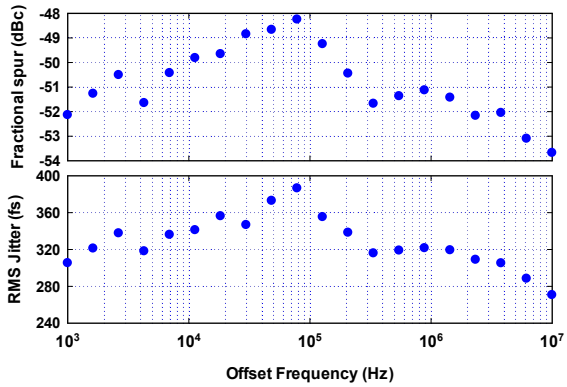


Figure 4.41 Measured fractional spur and integrated jitter across different frequency offset for the worst case fractional channel-3.75 GHz

Table 4.4 Summary of measured results

Tuning Range		2.8-4.3GH.z
Bandwidth		1.5MHz
In-band Phase Noise (@ 200KHz)	Integer Mode	-121dBc/Hz
	Fractional Mode	-112.5dBc/Hz
Out-band Phase Noise	Integer Mode @ 20MHz	-143dBc/Hz
	Fractional Mode @ 20MHz	-143dBc/Hz
Worst Case Fractional Spur		-48.3dBc
Reference Spur		-71dBc
Power		9.1mW

4.12.2 Performance summary and comparison to other works

Table 4.5 shows performance summary and comparison with other state-of-the-art low noise fractional-N synthesizers. A normalized in-band phase noise is employed for a comparison of the noise performance and is defined as:

$$\mathcal{L}_{norm} = \mathcal{L}_{in-band} - 20\log N - 10logf_{ref} \qquad (4.15)$$

The proposed FNSSPLL covers a wider tuning range as compared to the other presented works. Compared with [41] and [42] which are also DTC-enhanced SSPLLs, the proposed architecture achieves comparable in-band phase noise and spur performance with lower power consumption. A benchmarking figure-of-merit proposed in [30] is applied to account for the jitter-power tradeoff and make a fair comparison.

Table 4.5 Table of comparison

	This Work	[41]	[42]	[59]	[60]
Architecture	**Analog**	Analog	Analog	Digital	Digital
Method	**Sub-sampling**	Sub-sampling	Sub-sampling	Bang-Bang PD	Sub-sampling
Technology	**40nm**	28nm	180nm	65nm	65nm
Reference Freq. (MHz)	**50**	40	48	40	49.15
Tuning Range (GHz)	**2.8-4.3 (42%)**	9.2-12.7 (32%)	2.2-2.4 (8.7%)	2.9-4 (31.9%)	2.6-3.9 (40%)
Bandwidth	**1.5**	1.8	0.5	0.312	0.7
In-band Phase Noise (dBc/Hz)	**-112.5 (3.75GHz)**	-104 (10GHz)	-112 (2.3GHz)	-102 (3.35 GHz)	-110.6 (2.68GHz)
Normalized In-band Phase Noise	**-227**	-228	-214	-216.5	-222
Out-band Phase Noise (dBc/Hz)	**-143@20MHz**	-138@20MHz	-134.8@10MHz	-139	N/A
Worst Fractional Spur (dBc)	**-48.3**	-43	-48	-42	-62.3
Reference Spur (dBc)	**-71**	-60	-55	-72	-60
RMS jitter (fs)	**238-390**	230-280	266-400	400-560	226-240
Power (mW)	**9.18**	13	17.3	4.5	11.5
FOM	**-242.8 — -238.6**	-241.5 — -240	-239.1— -235.6	-238.3	-241.8
Area (mm^2)	**0.41**	N/A	0.75	0.22	0.23

The FoM is defined as:

$$FoM = 20 \cdot \log\left(\frac{\sigma_{t,PLL}}{1s}\right) + 10\log\left(\frac{P}{1mW}\right) \tag{4.16}$$

The FoM of the proposed FNSSPLL is -238.6 with the worst case in-band fractional spur and -242.8 when the fractional spur is out-of-band.

5. CONCLUSION AND FUTURE WORK

This work focused on the design considerations and implementation of a fully integrated fractional N subsampling PLL with a reduced in-band phase noise. The design was implemented in a standard 40nm CMOS process. Fractional frequency lock was achieved by placing a DTC assisted by a digital controller in the reference clock path to modulate the pulse width of the reference clock and thus change the sampling time. To alleviate the the non-idealities of the DTC, including gain error an effective 2-step background calibration mechanism is employed. A data weighted averaging DEM algorithm is also used to improve the performance of the system limited by mismatches in the DTC capacitor array.

From the measurement the FNSSPLL prototype achieves 390 fs RMS jitter with the worst case fractional spur and 120fs in the integer mode while consuming 9.18mW. The synthesizer has a 42% tuning range form 2.8-4.3GHz. From Table 4.5 , the measured in-band phase noise of -112.5dBc/Hz over the tuning range challenges the state-of-the-art fractional N synthesizers.

The current prototype depended on a manual tuning of the VCO capacitor bank control bit which is not desirable in a real world application. In future an automatic frequency control (AFC) similar to what is used in [61] would be employed to make the entire operation of the PLL automatic.

The low noise performance of the proposed system required the design of a DTC with fine resolution and a large dynamic range of 2 VCO cycles. This leads to a power-

jitter trade of the limits the FoM of the design. In future work we propose the use of a phase-interpolator (PI) in the feedback path to assist the DTC. An r-bit PI in the feedback will relax the DTC dynamic range requirements by a factor of $1/2^r$. Further, a pipelined implementation of the PI will relax the design constraints of designing a low power and low jitter PI to maintain the low phase noise advantage of the FNSSPLL.

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