# NOVEL CONTINUOUS-TIME LOW-PASS FILTER

A Thesis

by

FEIFEI LIU

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MASTER OF SCIENCE

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|---|---|
| Chair of Committee, | Jose Silva-Martinez |
| Co-Chair of Committee, | Aydin Karsilayan |
| Committee Members, | Jiang Hu |
| | Duncan M. (Hank) Walker |
| Head of Department, | Miroslav M. Begovic |

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# ABSTRACT

Continuous-time analog filters are important blocks for analog-to-digital converter (ADC) and IF filtering in receivers. Nowadays, cost and power consumption are major concerns for portable devices, so a low-power high performance solution is a great need.

The thesis proposes a novel continuous-time filter topology and implements a 10MHz low-pass filter achieving a signal-to-noise-and-distortion ratio (SNDR) of 70dB with only 1.3mW power consumption. This novel filter topology has an inherent low-noise property which alleviates the trade-off between noise and power consumption. The design considerations including frequency response, stability, noise, and distortion are presented. Since the performance of filters mainly depends on the amplifier, an AC-coupled class-AB OTA is proposed for the novel filter to improve the power efficiency and out-of-band linearity. The filter is implemented in IBM 130nm process and highly linear voltage-to-current converter and output buffer are also designed for testing. Compared with Tow-Thomas Biquad counterpart, the proposed filter saves about 40% power consumption for the same filter transfer function. Therefore, this proposed novel filter is a competitive filter topology for low-noise and low-power applications.

DEDICATION

To my parents and Fanglei

# ACKNOWLEDGEMENTS

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TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

Page

Page

LIST OF TABLES

Page

# 1. INTRODUCTION

## 1.1 Overview of analog filters

Analog filters have played an important role in telecommunications. Even though filtering is often preferred in digital domain due to the ease of implementation and immunity of manufacturing variations, analog filters have unique properties and must be used in some applications such as anti-aliasing filter for ADC in the receiver frontend [1].

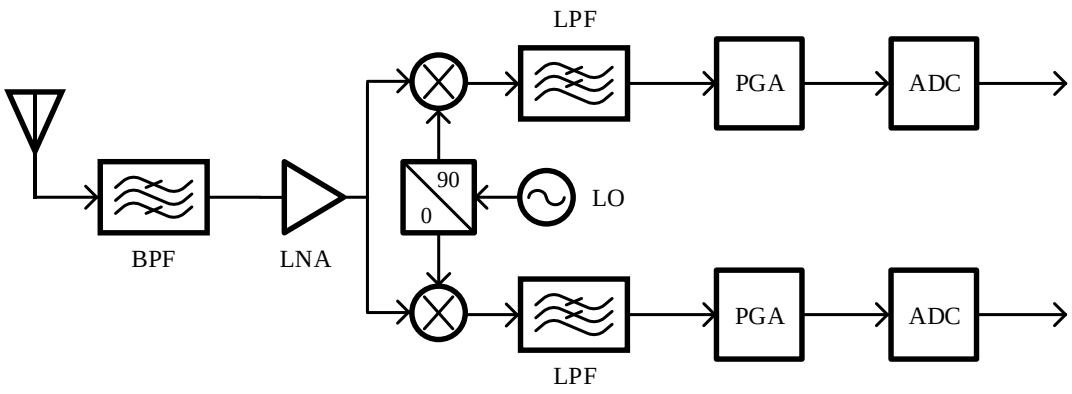



Figure 1 Direct-conversion receiver architecture

Figure 1 shows the architecture of Direct-conversion receiver which is very popular for fully integrated multi-standard receiver. And the low-pass analog filters are usually placed after the mixer to reject the blockers and adjacent channels to provide anti-aliasing for the Analog-to-Digital Converter (ADC).

There are three basic categories in analog filters: active-RC filters, OTA-C filters and switched-capacitor filter. The active-RC filters are featured as the amplifier in negative feedback configuration and an example is shown in Figure 2.

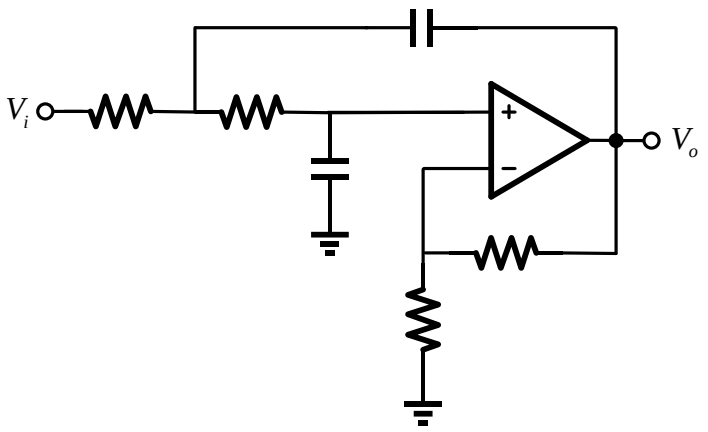



Figure 2 Example of Active-RC filter

This type of filter has the best linearity due to the feedback but the high performance relies on a high loop gain which is limited by stability. So the active-RC filters have limited cutoff frequency which is typically in the order of $10^7$Hz. And the cutoff frequency and quality factor usually depends on RC product and resistor ratio, which are quite sensitive to the process variation. And the accuracy can be as worse as 20% [2]. So the some tuning techniques are used to solve this issue.

OTA-C filters are using amplifier (OTA) in open-loop configuration so that it can provide cutoff frequency more than several $10^8$ Hz. Besides, the time constant depends on the capacitor and the transconductance of the OTA which is proportional to bias current, so the tuning is easy to do. One disadvantage is the distortion. Since the OTA has very small linear range, some linearization techniques must be used to reduce distortion. Moreover, the parasitic capacitance must be negligible compared with the load capacitance, which sets the upper limit of the operation frequency [2]. And an example of OTA-C filters is shown in Figure 3.

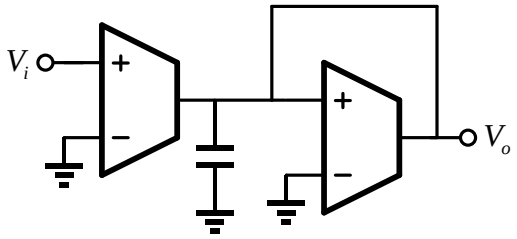



Figure 3 Example of OTA-C filter

Switched-capacitor filter belong to discrete-time filters. As shown in Figure 4, two non-overlapping clocks are used to charge and discharge the capacitor $C_1$so that it behaves like a resistor with the value of $1/f_{clk}C_1$, where $f_{clk}$ is the clock frequency. And many switched-capacitor filters can be obtained by substituting the resistors in active-RC filters with this emulated one. Such emulated resistor has two great advantages. The first one is the value of resistor can be very large. For example, if $C_1$is 1pF and $f_{clk}$ is 100kHz, the emulated resistor will be 10MΩ. Thus, some low frequency filters requiring a large time constant can be easily integrated by using switched-capacitor filters. The other one is the accuracy. The time constant in switched-capacitor filters depends on the ratio of capacitors and the absolute value of clock frequency. The accuracy of capacitor ratio is around 0.2% [2] and the clock is usually from the phase-locked-loop (PLL), which is also very accurate indeed. The drawback is the signal frequency must be much lower than the clock frequency for proper operation.

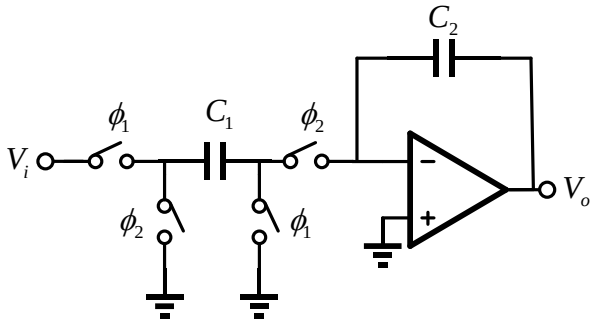



Figure 4 Example of switched-capacitor filters

**1.2 Thesis organization**

The thesis is organized with six sections. Section 1 briefly introduces the background of analog filter.

In section 2, the idea of the proposed novel filter is proposed. Some system level design considerations such as effect of real amplifier, stability, noise and distortion are explained.

In section 3, the transistor level design details of main building blocks are presented. Related design issues are also discussed.

In section 4, the chip layout, test setup and simulation results are presented.

In section 5, the analysis and simulation results of Tow-Thmoas Biquad are presented. And a fair comparison is made between the Tow-Thmoas Biquad and this novel filter.

In section 6, the conclusion of the thesis is drawn.

# 2. DESIGN OF THE NOVEL FILTER

## 2.1 The idea

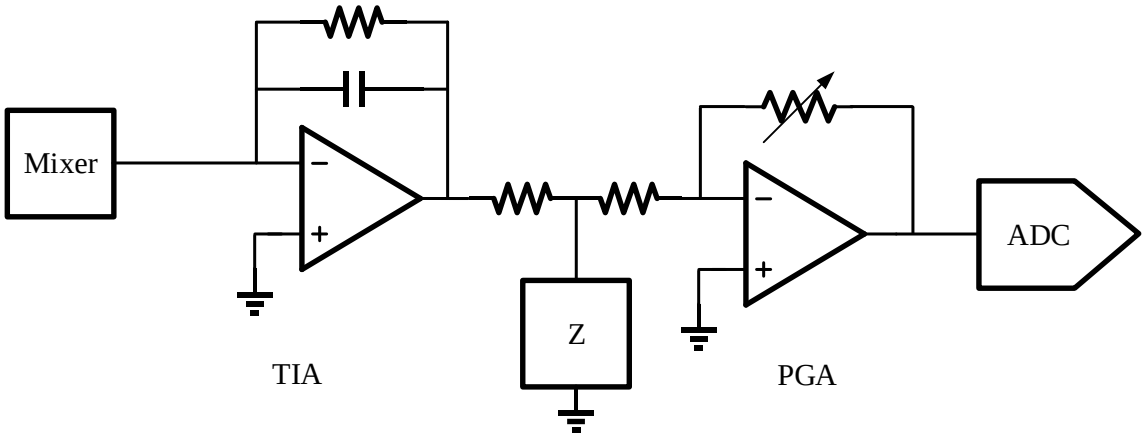



Figure 5 Proposed filter idea in receiver frontend

Part of a typical Direct-Conversion Receiver is shown in Figure 5. The Intimidate-Frequency (IF) current is converted into voltage by the Trans-Impedance Amplifier (TIA) and then is amplified by a Programmable Gain Amplifier (PGA) for the baseband ADC. The purpose of this research is to find a low cost solution for filtering in the receiver frontend. And we want to synthesize a block connected to the middle point of the input resistor, which is intentionally divided into two pieces in the PGA. The target block should have very large impedance at low frequency and starts to decrease in a second order roll-off after the cutoff frequency. Since the amplifier in the PGA provides a virtual ground at the negative input terminal. The part of target block is redrawn in the Figure 6.

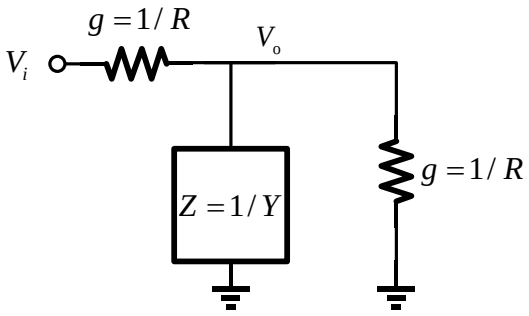



Figure 6 Concept of proposed filter

The transfer function of this part is $V_o/V_i$ which can be easily obtained by using the admittance of components as the following.

$$\frac{V_o}{V_i} = \frac{g}{2g + Y} \tag{2.1}$$

Since the DC gain of this network is one half and our target is to achieve a second order low pass transfer function, the target transfer function can be written as

$$\frac{V_o}{V_i} = \frac{1}{2} \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{2.2}$$

After combining equation (2.1) and equation (2.2), we obtain

$$Y = \frac{2g}{\omega_0 Q} s + \frac{2g}{\omega_0^2 Q} s^2 \tag{2.3}$$

Now the question is how to synthesize a network that has the admittance in equation (2.3). Obviously, this admittance Y can be seen as a capacitor in parallel with a 'super' capacitor [3], which can be realized by a General Impedance Converter (GIC) shown in Figure 7.

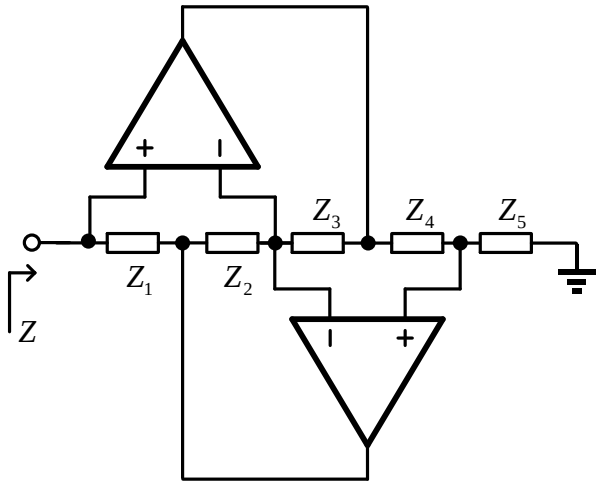



Figure 7 Schematic of GIC

The input impedance of GIC is given by

$$Z = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4} \tag{2.4}$$

Evidently we can set the $Z_1$ and $Z_5$ as capacitors and let the other impedance as resistors as shown in Figure 8.

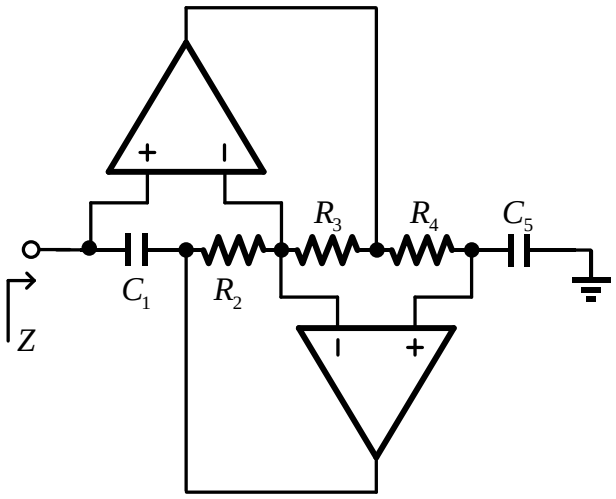



Figure 8 Impedance choice in GIC

In this case, the input impedance will be given by

$$Z = \frac{R_3}{s^2 C_1 C_5 R_2 R_4} \tag{2.5}$$

And that helps to synthesize the 'super' capacitor which is the second order term in equation (2.3). And the target admittance can be realized by adding a normal capacitor in parallel with it. However, neither the input of amplifier is connected to ground, which means all the inputs of amplifiers have the same signal swing as the input of the network. If the signal swing is large, the Op-amps have to accommodate large common mode input range, which complicates the design. Besides, there are two amplifiers in the network and five passive components, which is not a simple solution.

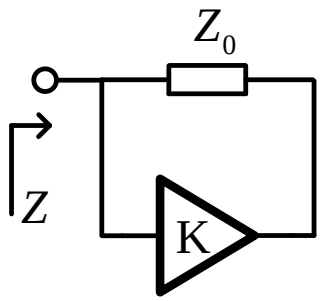



Figure 9 Concept of impedance scaler

In order to find a low-cost solution, the property of impedance scaler was examined. As shown in Figure 9, the input impedance of the impedance scaler is

$$Z = \frac{Z_0}{1 - K} \tag{2.6}$$

It has the potential to get a second order denominator if K is implemented by an inverting amplifier, shown in Figure 10.

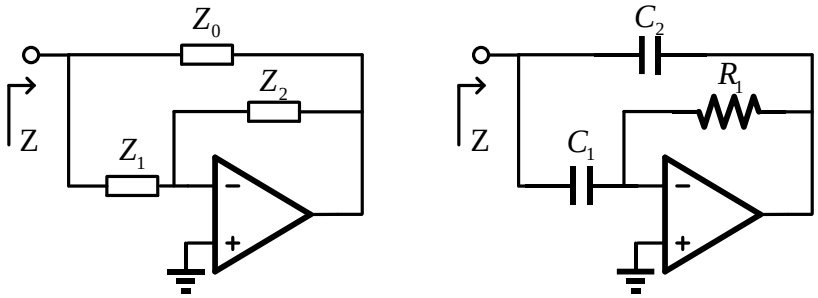



Figure 10 Implementation of impedance scaler

Now the input impedance is

$$Z = \frac{Z_0}{1+\frac{Z_2}{Z_1}} \| Z_1 \tag{2.7}$$

By setting $Z_0$ and $Z_1$ as capacitor, $Z_2$ as resistor, we have the input impedance

$$Z = \frac{1}{s(C_1+C_2)+s^2 C_1 C_2 R_1} \tag{2.8}$$

Thus the input admittance is

$$Y = \frac{1}{Z} = s(C_1+C_2)+s^2 C_1 C_2 R_1 \tag{2.9}$$

The equation (2.9) has exactly the same form as equation (2.3). Thus, it turns out to be a simple and efficient solution because it has only one amplifier and three passive components. Besides, the negative input terminal of the amplifier is a virtual ground and there is little signal swing. Thus this approach does not have the stringent common mode input range requirement for the amplifier.

## 2.2 Filter topology

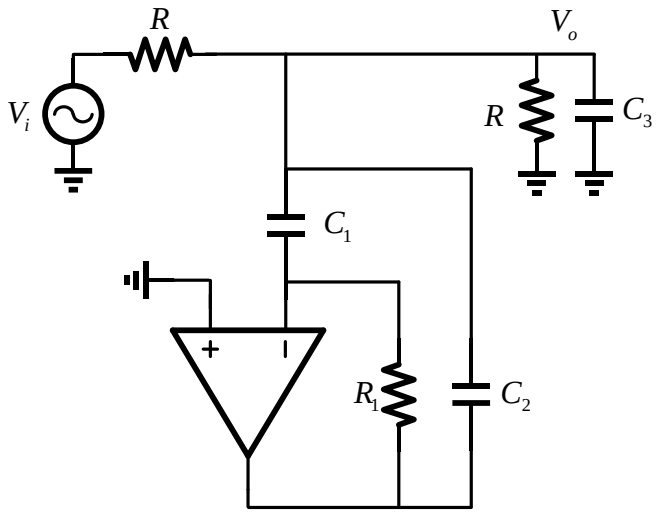



Figure 11 Filter topology

The filter topology is shown in Figure 11 and we note that there is an additional capacitor $C_3$ is added in parallel with the load resistor. At high frequency, the loop gain of the filter is not high enough to support normal operation of the synthesized impedance. And the capacitor $C_3$ will continue the job of synthesized impedance to provide high frequency filtering. The filter transfer function in Figure 11 is given by

$$\frac{V_o}{V_i} = \frac{1/R}{2/R + sC_3 + Y} = \frac{\frac{1}{2}\frac{2}{C_1C_2R_1R}}{s^2 + \frac{C_1+C_2+C_3}{C_1C_2R_1}s + \frac{2}{C_1C_2R_1R}} \qquad (2.10)$$

Where $Y = s(C_1+C_2) + s^2 C_1C_2R_1$

The second order low pass transfer function is

$$H(s) = \frac{1}{2} \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \tag{2.11}$$

Then the Q and $\omega_0$ are obtained as follow:

$$\omega_0 = \sqrt{\frac{2}{C_1 C_2 R_1 R}} \tag{2.12}$$

$$Q = \frac{1}{C_1 + C_2 + C_3} \sqrt{\frac{2C_1 C_2 R_1}{R}} \tag{2.13}$$

From equation (2.13), the Q has different form and unique parameter $C_3$ compared with $\omega_0$. Hence, the Q of the filter can be tuned by changing $C_3$ when $\omega_0$ is fixed.

The DC gain is one half due to the resistive divider and thus half of input signal is wasted on the resistor in series with the voltage source. However, it will be more efficient to realize the filter driven by a current source. As shown in Figure 12, all the input current signal is injected to the load without wasting the input signal. In another words, the gain is not limited by one half if the filter is driven by a current source. In this design, we maintain an equivalence of the two cases for testing. According to Thevenin-Norton Equivalencies, the following relationships guarantee the same transfer function of two cases.

$$I_i = \frac{V_i}{R} \tag{2.14}$$

$$R_2 = R / 2 \tag{2.15}$$

And the details of the current source implementation are discussed in section 3.2.

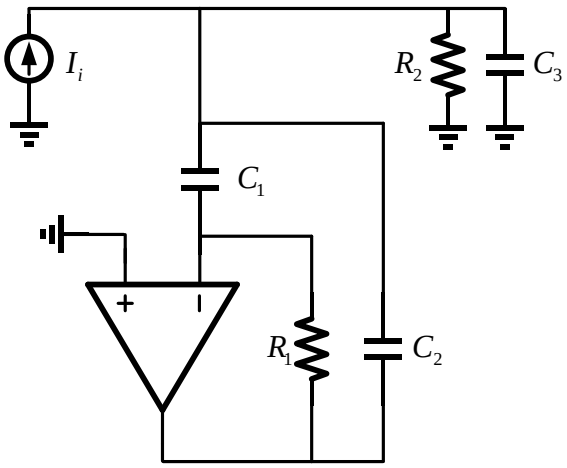



Figure 12 Filter driven by current source

## 2.3 General design considerations

### 2.3.1 Components value

The proposed filter is designed for a digital TV application and the target filter specs are given in Table 1.

Table 1 Target spec of proposed filter

| **Specs** | **Value** |
|---|---|
| Cutoff frequency | 10MHz |
| Q | 0.5~1 |
| Order | 2 |
| DC Gain | 0.5 |
| Pass band ripple | <0.5dB |

For a second order system,

$$H(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{2.16}$$

the magnitude at natural frequency $\omega_0$ is given by

$$\left|H(j\omega)\right|_{\omega=\omega_0} = \left|\frac{\omega_0^2}{-\omega_0^2 + \frac{\omega_0}{Q}j\omega_0 + \omega_0^2}\right| = Q \tag{2.17}$$

So Q is the magnitude of the transfer function at $\omega_0$ shown in Figure 13.

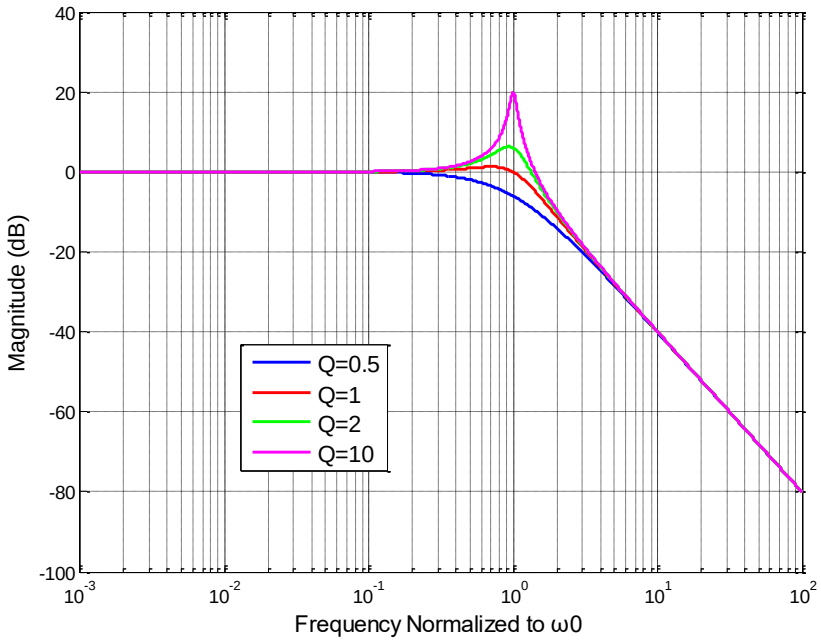



Figure 13 Frequency response of second order system with different Q

The cutoff frequency is defined as the maximum frequency where the DC gain does not attenuate. For Q equal to unity, the natural frequency $\omega_0$ is just the cutoff frequency according to the above definition.

According to equation (2.12) and (2.13), the component values have the following relationship assuming Q is unity.

$$C_1 C_2 R_1 = \frac{2}{R\omega_0^2} \tag{2.18}$$

$$C_1 + C_2 + C_3 = \frac{2}{R\omega_0} \tag{2.19}$$

The value of resistor R is critical. Large value of R can relax the specs of OTA but introduce more noise to the output node. Limited by the noise requirement, R is set to 2kΩ in this design. So the $R_2$ in Figure 12 is 1kΩ according to equation (2.15). Since $\omega_0$ is equal to the cutoff frequency $2\pi\times10$M rad/s, the sum of $C_1$, $C_2$ and $C_3$ can be calculated as 16pF. The value of $C_1$and $C_2$ are both chosen as 2pF as an initial point. And thus $C_3$ and $R_1$ can be obtained as 12pF and 64kΩ respectively.

Table 2 Final choice of component value

| **Component** | **Value** |
|---|---|
| $C_1$, $C_2$ | 2pF |
| $C_3$ | 8pF |
| $R_1$ | 18kΩ |
| R | 2kΩ |

However, the total capacitance of 16pF is still quite large so that the OTA has to consume large power to provide enough AC current. In order to relax the power consumption requirement of OTA, the values of components are modified according to simulation. And the values are given in the Table 2.

The $R_1$ and $C_3$ are reduced so does the quality factor Q which is reduced to about 0.7 in this design. Hence, the natural frequency $\omega_0$ increases beyond 10MHz to meet the cutoff frequency definition.

### 2.3.2 Effect of real OTA and Op-amp

Operational Transconductance Amplifier (OTA) is a basic cell in analog circuits. The difference between the OTA and Operational Amplifier (Op-amp) is illustrated in Figure 14.

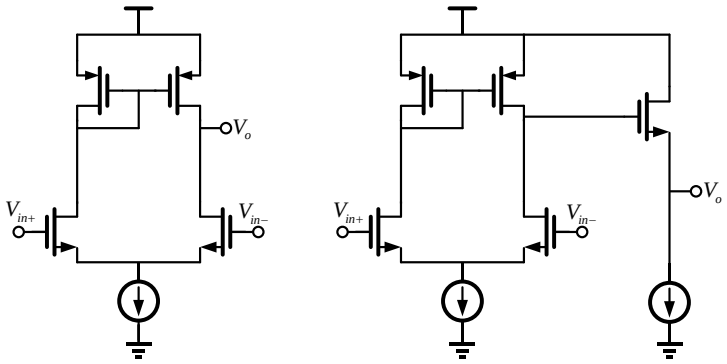



Figure 14 Example of OTA and Op-amp

Compared with OTA, the Op-amp circuit has an additional source follower stage as an output buffer. It can be seen that the Op-amp includes an OTA as well as an output buffer, so the OTA is only one part of the Op-amp. The output buffer provides a low

output impedance and makes Op-amp able to drive low impedance load. However, the output buffer usually consumes a great amount of power and complicates the circuit design. In the on-chip environment, the loads of the amplifier are usually capacitors or high-value resistance rather than low impedance. Hence, the OTA is typically an efficient solution and the OTA is used in the implementation of the filter. The ideal models of the OTA and Op-amp are also different and are shown in Figure 15. The OTA can be modeled as a voltage controlled current source with a transconductane $G_m$, while the Op-amp is a voltage-controlled voltage source with a voltage gain of A.

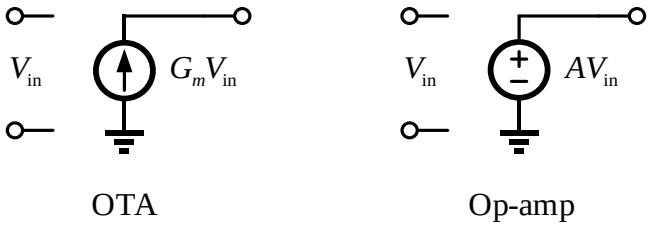



Figure 15 Ideal small signal model of OTA and Op-amp

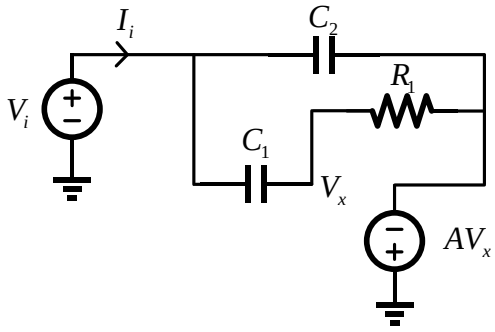



Figure 16 Input impedance derivation using ideal model of Op-amp

The derivation of the driving point impedance in section 2.1 is based on ideal Op-amp. As shown in Figure 16, we first consider the Op-amp has a finite gain and use the model of Op-amp in Figure 15 to derive the input impedance. The node equation at the negative terminal of the Op-amp can be written as

$$(V_i - V_x)sC_1 = \frac{V_x + AV_x}{R_1} \tag{2.20}$$

And the input current is given by

$$I_i = (V_i + A\,V_x)sC_2 + (V_i - V_x)sC_1 \tag{2.21}$$

By solving equation (2.20) and (2.21), the input impedance can be obtained as

$$Z_{in} = \frac{V_i}{I_i} = \frac{\frac{sC_1R_1}{1+A} + 1}{s(C_1 + C_2) + s^2 C_1C_2R_1} \tag{2.22}$$

From equation (2.22), the finite gain of Op-amp introduces a zero at $-(1+A)/C_1R_1$ to the input impedance. As long as the gain of the Op-amp is high enough, the zero should be at high frequency and have negligible effect to the overall transfer function of the filter.

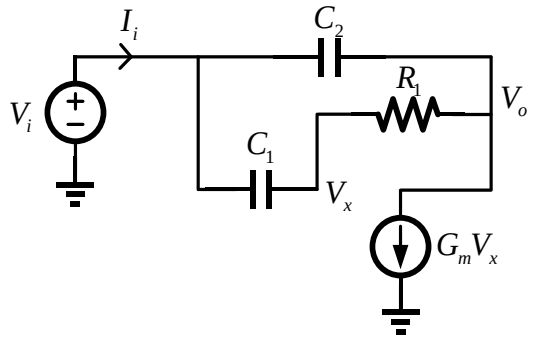



Figure 17 Input impedance derivation using ideal model of OTA

Now we replace the Op-amp with an OTA model and derive the input impedance again as shown in Figure 17. The node equations can be written as

$$I_i = (V_i - V_o)sC_2 + (V_i - V_x)sC_1 = G_m V_x \tag{2.23}$$

$$(V_i - V_x)sC_1 = \frac{V_x - V_o}{R_1} \tag{2.24}$$

By solving the equation (2.22) and (2.23), the input impedance can be obtained as

$$Z_{in} = \frac{V_i}{I_i} = \frac{\frac{s^2 C_1 C_2 R_1}{G_m} + \frac{s(C_1 + C_2)}{G_m} + 1}{s(C_1 + C_2) + s^2 C_1 C_2 R_1} \tag{2.25}$$

The equation (2.24) will be reduced to the same form as equation (2.8), if $G_m$ is infinity. However, the OTA always has a finite transconductance $G_m$ so that the input impedance will have a complex conjugate zero which directly appears in the closed-loop transfer function of the filter.

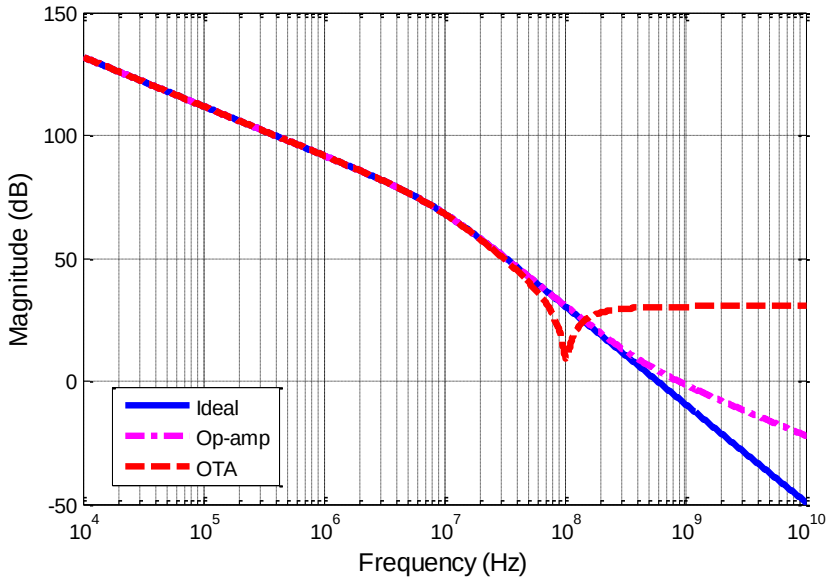



Figure 18 Input impedance by using different amplifier model

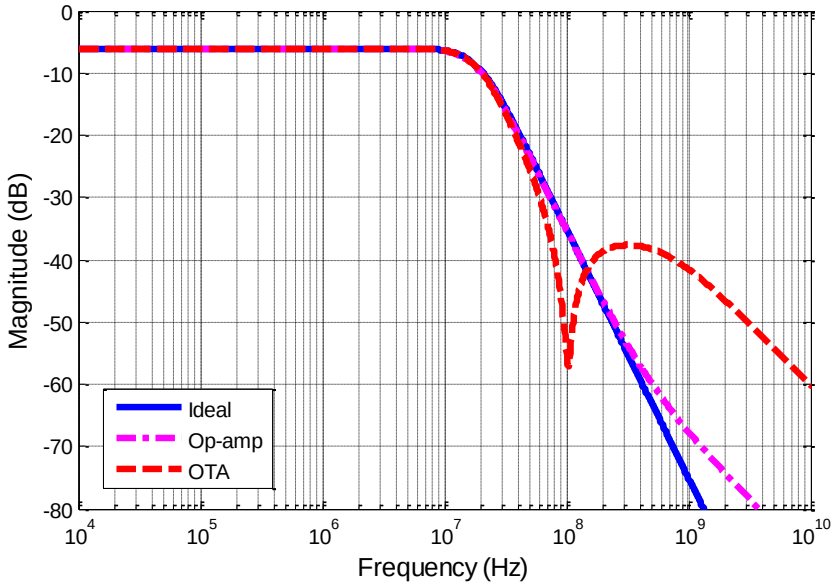



Figure 19 Filter response by using different amplifier model

And the simulated input impedance of using different macro-models of amplifiers are shown in Figure 18. Op-amp gain A is chosen as 100 and $G_m$ of OTA is set as 30mS in the simulation. The corresponding filter transfer function is shown in Figure 19.

Compared with equation (2.22), the finite $G_m$ of OTA introduces higher order of zero than the Op-amp, which is a penalty of removing the output stage to save power. But the complex conjugate zero helps to get a steeper roll-off compared with using Op-amp. Generally, the OTA should have a large overall $G_m$ as well as a high bandwidth to provide enough stopband attenuation.

From the numerator in equation (2.25), the Q and $\omega_0$ of the second order zero can be obtained similarly as the following.

$$\omega_0 = \sqrt{\frac{G_m}{C_1 C_2 R_1}} \tag{2.26}$$

$$Q = \frac{\sqrt{G_m C_1 C_2 R_1}}{C_1 + C_2} \tag{2.27}$$

Since the Q of zero is typically larger than 1 which means a complex conjugate zero, the filter response will have a big notch and the roll-off is actually large than 40dB/dec. In general, assuming the filter roll-off is 50dB/dec, in order to get at least K dB attenuation the $\omega_0$ of zero and the $\omega_0$ of pole should have the following relationship.

$$50 \log \frac{\omega_{0\_zero}}{\omega_{0\_pole}} > K \tag{2.28}$$

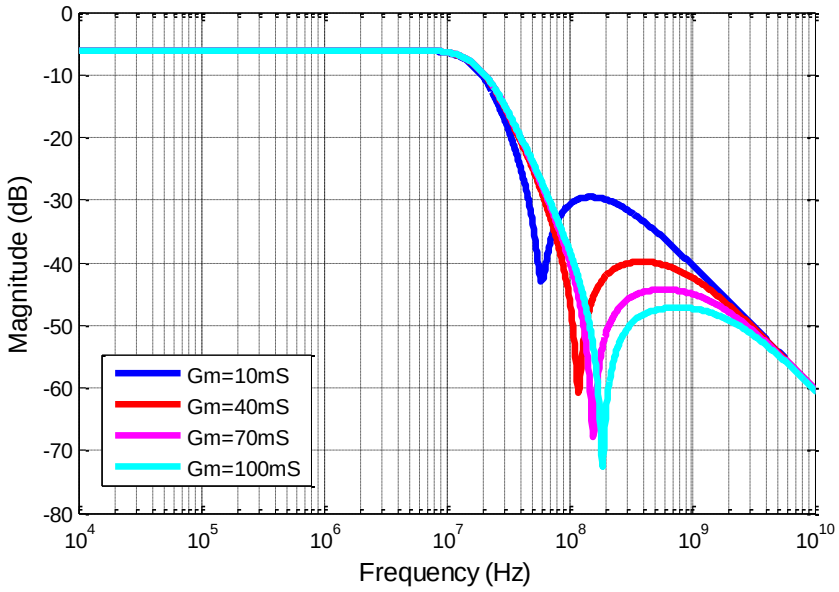



Figure 20 Filter response by using different $G_m$ of OTA

By substituting equation (2.26) and (2.12) into $\omega_{0\_zero}$ and $\omega_{0\_pole}$ respectively, we have

$$G_m > \frac{2}{R} 10^{\frac{K}{25}} \tag{2.29}$$

Given that the R is chosen as 2kΩ and K is 40dB in this design, the required $G_m$ is about 40mS. By changing the $G_m$ only, the filter response is shown in Figure 20.

We can see that increasing $G_m$ too much the attenuation is improved slowly because increasing $G_m$ will also increase the Q of the complex conjugate zero at the same time. So in this design, the optimum $G_m$ is from 30mS to 40mS to get a 40dB attenuation and that $G_m$is hard to achieve in a single-stage OTA with reasonable power consumption. Considering three-stage OTA has more poles and zeros, which complicates the design, typical class-A two-stage OTA is chosen first for the following analysis.

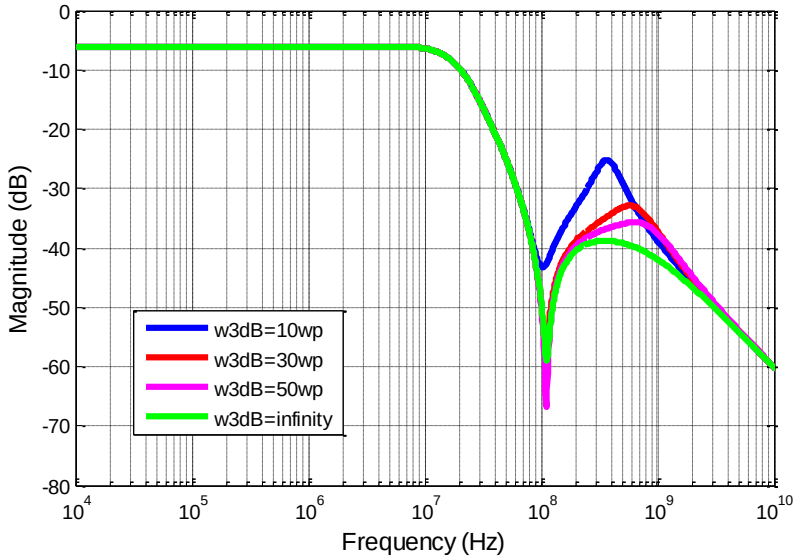



Figure 21 Filter response with different OTA bandwidth

Regarding the bandwidth of the OTA, we assume the $G_m$ has a finite 3dB bandwidth $\omega_{bw}$. Intuitively, $\omega_{bw}$ should be larger than the high frequency pole $\omega_p$ introduced by additional capacitor $C_3$ in Figure11. Without considering synthesized impedance, this pole is at $2/(RC_3)$. The simulation with different bandwidth of $G_m$ is shown in Figure 21.

It seems that the 3dB bandwidth of $G_m$ should be above 30 times the $\omega_p$ to reduce the high frequency peaking. And that demands a 600MHz 3dB bandwidth for the OTA in this design. OTA with 600MHz 3dB bandwidth seems hard to realize if considering the stability. But section 2.3.6 and 3.1 show that the OTA is possible to realize in this design. The above analysis is pessimistic in reality. The OTA usually has more than one pole and other circuitries in the receiver also has additional high frequency pole, heling reducing such peaking.

**2.3.3 Loop stability**

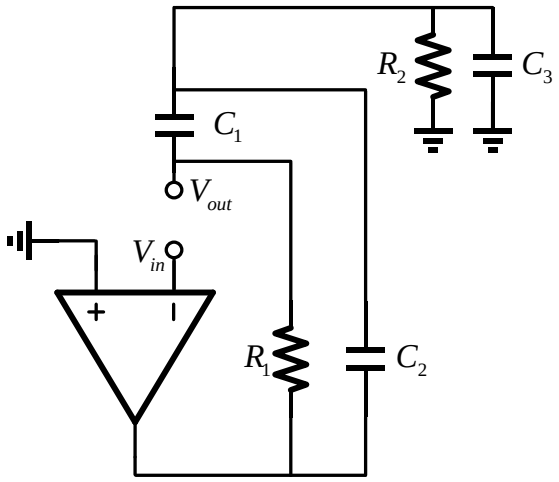



Figure 22 Filter circuits in Figure12 with loop broken

For any feedback system, the stability is always an issue. In order to make a stable loop, the location of poles and zeros of open-loop transfer function or loop gain should be clearly analyzed. Typically, the open-loop transfer function is found by breaking at the input terminal of the amplifier shown in Figure 22 and defined as $V_{out}/V_{in}$. Note that the input current source is set to zero by being seen as open circuit.

From the analysis of section 2.2.2, a two-stage OTA should be used and thus the corresponding macro-model is used in the open-loop circuit shown in Figure 23.

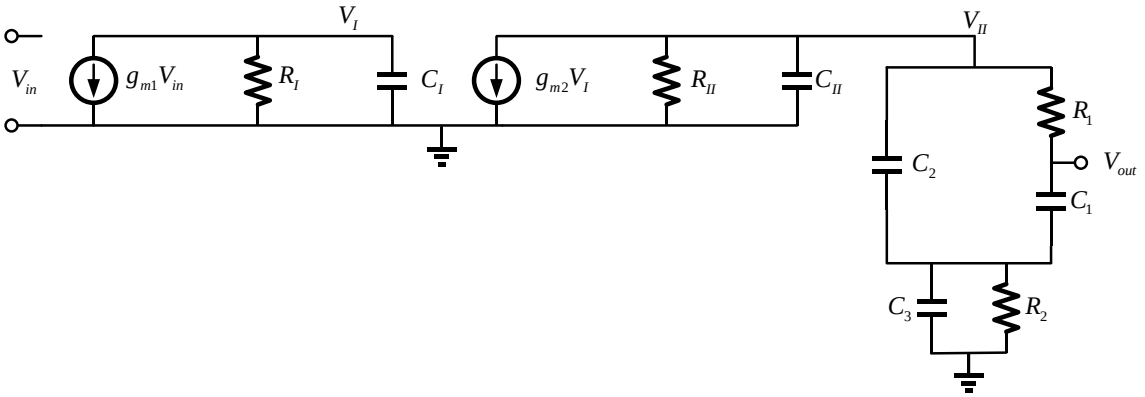



Figure 23 Open-loop circuits with macro-model of two-stage OTA

The open-loop transfer function can be divided into two parts as follow.

$$\frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_{II}} \frac{V_{II}}{V_{in}} \tag{2.30}$$

And the decomposition of the $V_{out}/V_{in}$ from simulation is illustrated in Figure 24. And each part will be discussed separately.

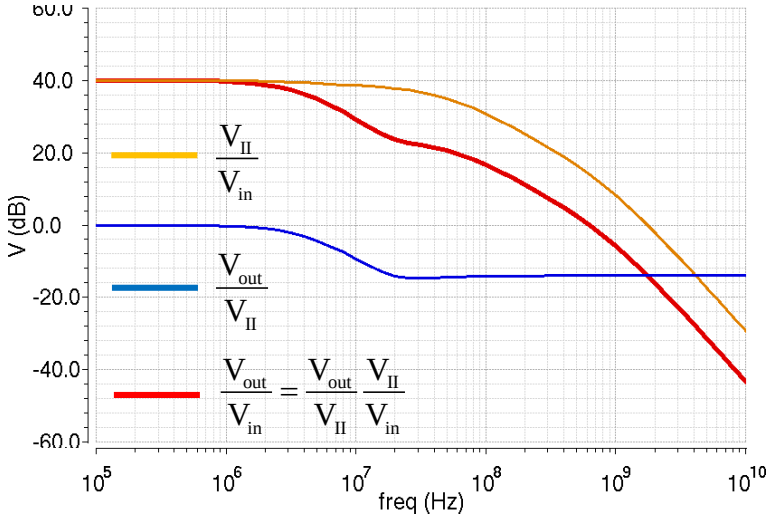



Figure 24 Decomposition of filter loop gain in simulation

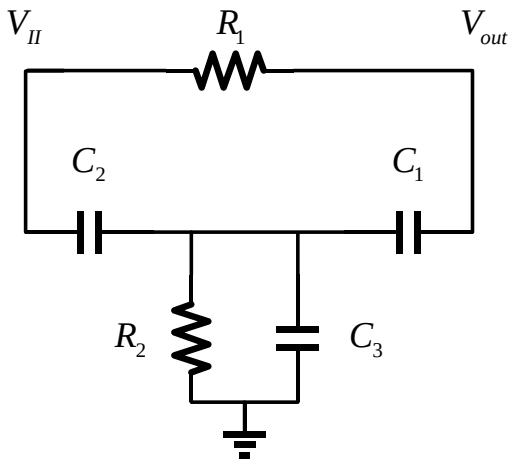



Figure 25 Circuit of first part

The circuit of the first part is illustrated in Figure 25. And the transfer function of $V_{out}/V_{II}$ can be obtained below by writing node equations.

$$\frac{V_{out}}{V_{II}} = \frac{s^2 C_1 C_2 R_1 R_2 + s(C_1 + C_2 + C_3) R_2 + 1}{s^2 C_1 (C_2 + C_3) R_1 R_2 + s[C_1 R_1 + (C_1 + C_2 + C_3) R_2] + 1} \tag{2.31}$$

If we assume the two poles are far away from each other [4], we can get

$$\omega_{p1} = -\frac{1}{C_1 R_1 + (C_1 + C_2 + C_3) R_2} \tag{2.32}$$

$$\omega_{p2} = -\frac{C_1 R_1 + (C_1 + C_2 + C_3) R_2}{C_1 (C_2 + C_3) R_1 R_2} \tag{2.33}$$

Since the two zeros are very close to the second pole, the magnitude drops a little after the first pole and then is flatten out around the second pole. The approximation of the first part is shown in Figure 26.

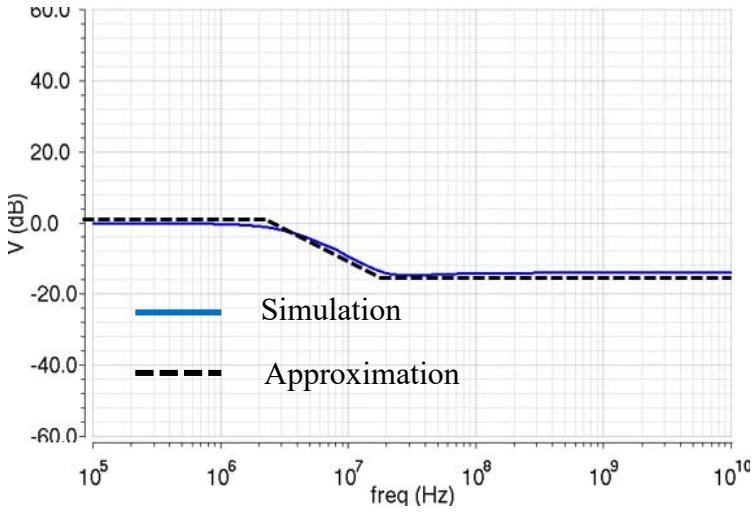



Figure 26 Approximation of first part

The second part in Figure 23 is simply the OTA driving a large load. In order to obtain the second part, the input impedance of the load needs to be analyzed first shown in in Figure 27.

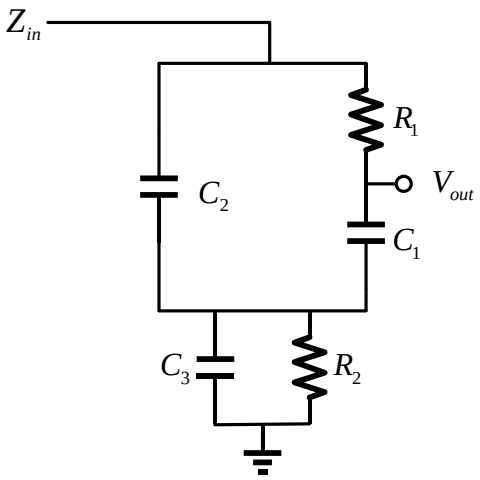



Figure 27 Load driven by OTA

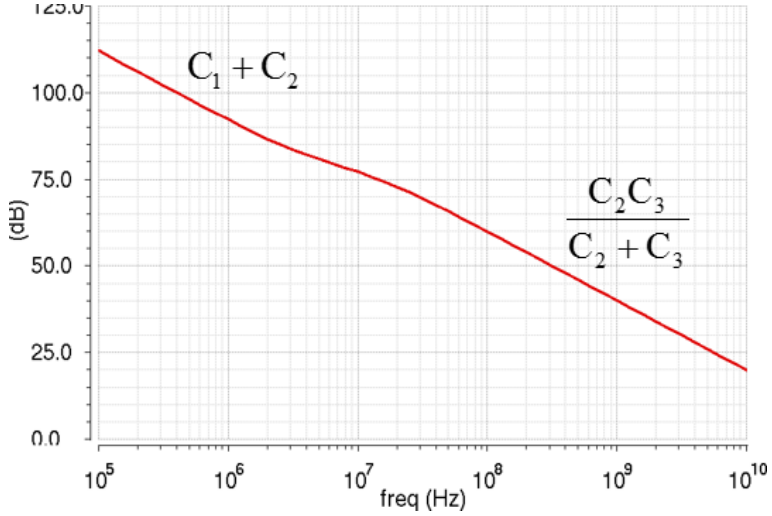



Figure 28 Simulation of input impedance of the load

At low frequency, $R_1$is very small compared with $C_2$and so do $R_2$ and $C_3$, which means the input impedance can be seen as $C_1$ in parallel with $C_2$ and then in series with $R_2$. Since the impedance of $C_1$ and $C_2$ are much larger than $R_2$ at low frequency, the input impedance can be simply estimated as $C_1$+$C_2$. Similarly, at high frequency, the

impedance of all the capacitors are much smaller than resistors. Thus, the input impedance is simply $C_2$ in series with $C_3$. As expected, the simulator shows the input impedance of the network in Figure 28. Since frequency beyond 10MHz is of more interest to find the phase margin in the open-loop analysis, this input impedance is simplified as $C_{eq}=C_1C_2/(C_1+C_2)$ to obtain the second part $V_{II}/V_{in}$ illustrated in Figure 29.

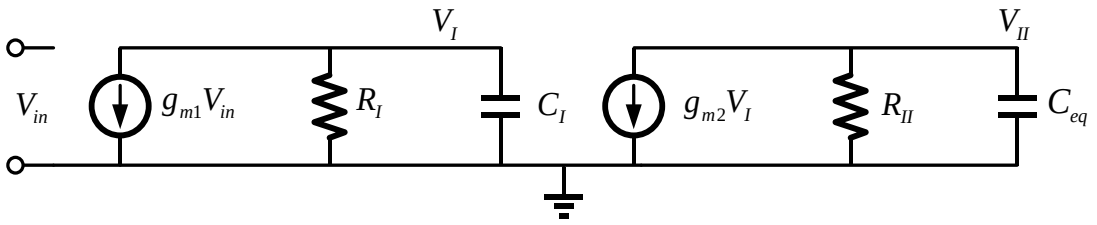



Figure 29 Open-loop circuits of the second part with equivalent capacitor

The parasitic capacitance $C_{II}$ is much smaller than $C_{eq}$ and thus neglected here. Now the transfer function of second part is obviously given by

$$\frac{V_{II}}{V_{in}} = \frac{g_{m1}g_{m2}R_IR_{II}}{(s+\omega_{p3})(s+\omega_{p4})} \tag{2.34}$$

Where

$$\omega_{p3} = -\frac{1}{\frac{C_2C_3}{C_2+C_3}R_{II}} \tag{2.35}$$

$$\omega_{p4} = -\frac{1}{C_IR_I} \tag{2.36}$$

The comparison between the above approximation of $V_{II}/V_{in}$ and its simulation is illustrated in Figure 30. It shows that even though there is a little difference around the

first pole due to the approximation of $C_{eq}$, the approximation yields a simple mathematical equation for analysis.

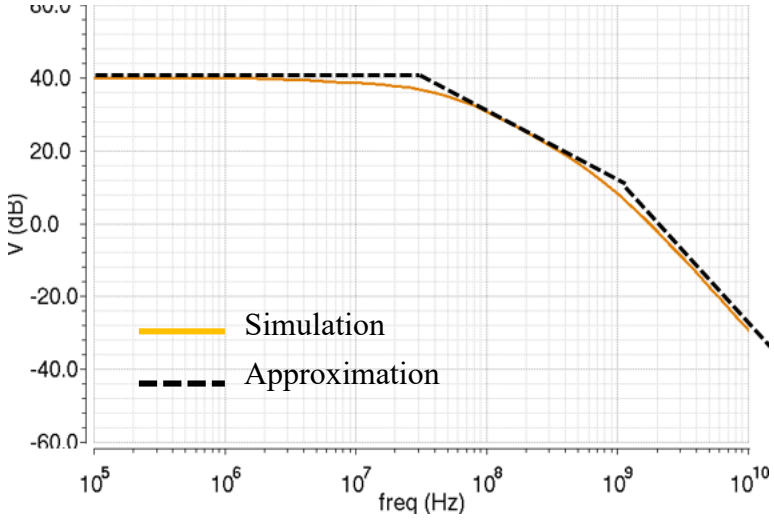



Figure 30 Approximation of second part

After obtaining the two parts, the open-loop transfer function can be found as the following.

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}g_{m2}R_I R_{II}[s^2 C_1 C_2 R_1 R_2 + s(C_1 + C_2 + C_3)R_2 + 1]}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})(s+\omega_{p4})} \tag{2.37}$$

Where the $\omega_{p1}$, $\omega_{p2}$, $\omega_{p3}$ and $\omega_{p4}$ are given by equation (2.32), (2.33), (2.35) and (2.36) respectively. However, it is still not easy to get the phase margin from equation (2.37). Thus, the open-loop transfer function can be further simplified as a two-pole system shown in Figure31.

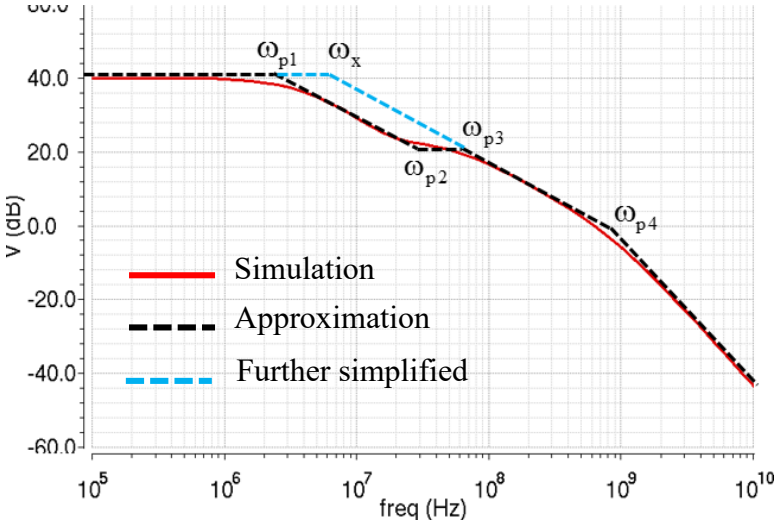



Figure 31 Further simplified approximation of loop gain

Assuming the open-loop transfer function has a dominant pole at $\omega_x$. We notice that the region between $\omega_x$ and $\omega_{p3}$ and the region between $\omega_{p1}$ and $\omega_{p2}$ are both -20dB/dec and thus we have

$$\frac{\omega_{p2}}{\omega_{p1}} \approx \frac{\omega_{p3}}{\omega_x} \tag{2.38}$$

By using equation (2.27), (2.28) and (2.30), $\omega_x$ is given by

$$\omega_x = \frac{\omega_{p1}\omega_{p3}}{\omega_{p2}} = -\frac{R_1 R_2 C_1 (C_2 + C_3)^2}{C_1 C_3 R_{II}[C_1 R_1 + (C_1 + C_2 + C_3) R_2]^2} \tag{2.39}$$

For a two-pole system, the second pole must be set beyond the unity gain frequency to ensure stability, so the unity gain frequency is equal to the gain bandwidth product (GBW) which is given by

$$\omega_u = g_{m1} g_{m2} R_I R_{II} \omega_x = -\frac{g_{m1} g_{m2} R_1 R_2 R_I C_1 (C_2 + C_3)^2}{C_2 C_3 [C_1 R_1 + (C_1 + C_2 + C_3) R_2]^2} \tag{2.40}$$

The phase margin of a two-pole system is equal to the following

$$PM = 90 - \tan^{-1}\frac{\omega_u}{\omega_{p4}} \tag{2.41}$$

Therefore, the stability of the loop gain is mainly depends on the $\omega_{p4}$, which should be put around $2\omega_u$ for a phase margin of 60 degree. Interestingly, $\omega_{p4}$ is the pole at the output of the OTA's first stage so that typical Miller compensation would degrade the phase margin. The above analysis indicates that the two-stage OTA should be implemented without Miller compensation and try to make the parasitic capacitance as small as possible at the output of the first stage. Without Miller compensation the 3dB bandwidth of the OTA will be improved remarkably so as to meet the bandwidth requirement in section 2.3.2.

**2.3.4 Noise analysis**

One of the big advantages of this filter is it introduces little in-band noise to the output. As illustrated in Figure 32, the capacitor $C_1$ and $C_2$has very high impedance at low frequency so that the noise of the OTA and resistor $R_1$is blocked by these two capacitors. The only dominant noise source is $R_2$, which can be controlled by limiting its value. Since the OTA noise is a great concern for many circuits and low noise usually requires high power consumption, the nice property of this filter alleviate the trade-off between noise and power to yield a low-noise power efficient filter.

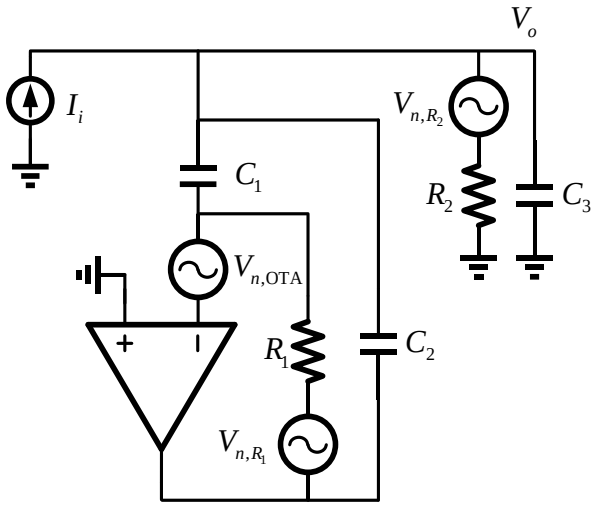



Figure 32 Noise sources in the proposed filter

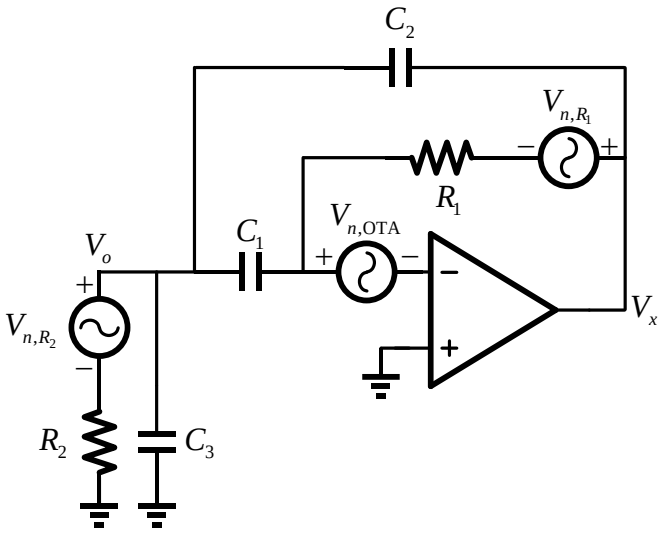



Figure 33 Circuits for noise analysis

To perform noise analysis, the input current source is set to zero by seeing it as an open circuit and then Figure 12 is redrawn in Figure 33. Assume the noise voltage

sources have the polarities in Figure 33, the node equations on the two terminals of $C_1$ can be written as the following.

$$\frac{V_o - V_{n,R_2}}{R_2} + V_o sC_3 + (V_o - V_{n,OTA})sC_1 + (V_o - V_x)sC_2 = 0 \tag{2.42}$$

$$(V_o - V_{n,OTA})sC_1 + \frac{V_x - V_{n,R_1} - V_{n,OTA}}{R_1} = 0 \tag{2.43}$$

By solving equation (2.42) and (2.43), the output noise voltage due to the three noise sources is obtained as

$$V_o = H_1(s)V_{n,R_2} + H_2(s)V_{n,OTA} + H_3(s)V_{n,R_1} \tag{2.44}$$

Where

$$H_1(s) = \frac{1}{s^2C_1C_2R_1R_2 + s(C_1 + C_2 + C_3)R_2 + 1} \tag{2.45}$$

$$H_2(s) = \frac{s^2C_1C_2R_1R_2 + s(C_1 + C_2)R_2}{s^2C_1C_2R_1R_2 + s(C_1 + C_2 + C_3)R_2 + 1} \tag{2.46}$$

$$H_3(s) = \frac{sC_2R_2}{s^2C_1C_2R_1R_2 + s(C_1 + C_2 + C_3)R_2 + 1} \tag{2.47}$$

It can be seen that the contributions of three noise voltage sources to the output are shaped by the transfer function $H_1(s)$, $H_2(s)$ and $H_3(s)$ respectively. Using the components value given in Table 2, their frequency responses are plotted in Figure 34. $H_1(s)$ is a second order low pass response. At low frequency, the gain of $H_1(s)$ is about unity so that the noise from $R_2$ is directly showing up at the output, which is intuitively true. Besides of two poles, $H_2(s)$ has one zero at origin and another zero at $(C_1+C_2)/C_1C_2R_1$ which is the same frequency as the dominant pole of the filter. So

$H_2(s)$ has a gain less than unity until the cutoff frequency of the filter, meaning the noise of the OTA is filtered out for the in-band signal. Similarly, $H_3(s)$ is a band-pass response compared with the high-pass $H_2(s)$. Hence, the noise of resistor $R_1$ is also filtered out for the in-band signal. The above mathematical derivation validates our intuitive explanation that the capacitors $C_1$ and $C_2$ block the noise of the OTA and $R_1$ at low frequency. The derivation even specifies the so called low frequency which in fact ranges from DC to the cutoff frequency of the filter.

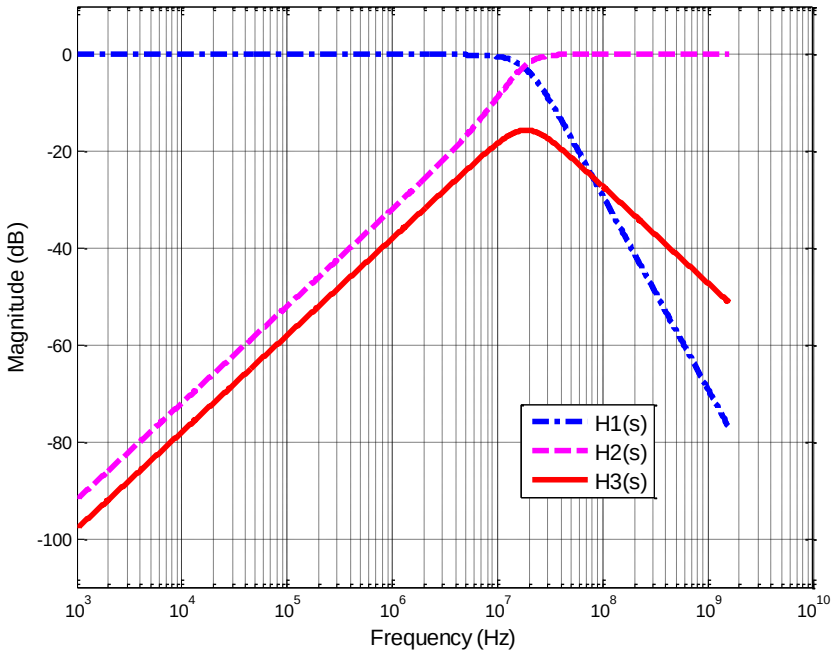
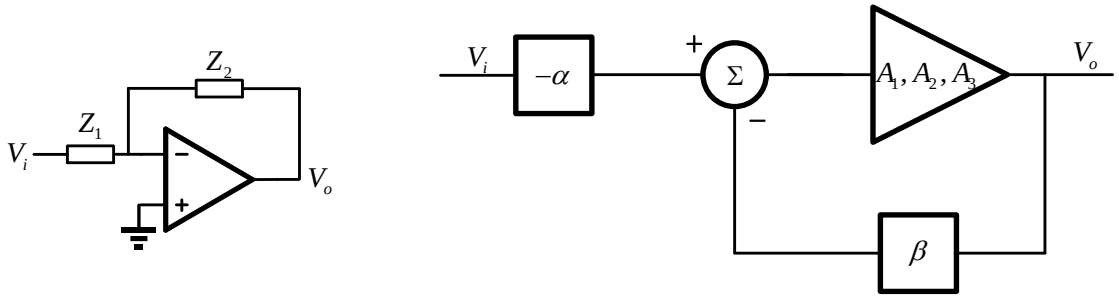



Figure 34 Plots of noise transfer functions

### 2.3.5 Distortion analysis




(a) (b)

Figure 35 (a) Inverting amplifier (b) Model of non-linearity

Since the passive components are very linear, the distortion is mainly from the amplifier. For inverting amplifier, the gain can be modeled in Figure 35 (b). The gain of OTA is $A_1$ and the second and third order coefficients are $A_2$ and $A_3$ respectively. The feedback factors are given by

$$\alpha = \frac{Z_2}{Z_1 + Z_2} \tag{2.48}$$

$$\beta = \frac{Z_1}{Z_1 + Z_2} \tag{2.49}$$

From Figure 35 (b), the output can be easily obtained by

$$V_o = A_1(-\alpha V_i - \beta V_o) + A_2(-\alpha V_i - \beta V_o)^2 + A_3(-\alpha V_i - \beta V_o)^3 \tag{2.50}$$

And the non-linear relationship between the $V_o$ and $V_i$ is modeled by a new set of coefficients $B_1$, $B_2$ and $B_3$ as given by the following.

$$V_o = B_1 V_i + B_2 V_i^2 + B_3 V_i^3 \tag{2.51}$$

Substituting equation (2.51) into equation (2.50) and ignoring the higher order terms,

$$B_1 = \frac{-A_1\alpha}{1+A_1\beta} \tag{2.52}$$

$$B_2 = \frac{-A_2\alpha^2}{(1+A_1\beta)^3} \tag{2.53}$$

$$B_2 = \frac{2\beta A_2{}^2\alpha^3 - (1+A_1\beta)A_3\alpha^3}{(1+A_1\beta)^5} \approx \frac{-A_3\alpha^3}{(1+A_1\beta)^4} \tag{2.54}$$

Then this non-linear model of inverting amplifier is substituted in the filter shown in Figure 36. And node equation at the output can be written as

$$I_i - V_o(\frac{1}{R_2} + sC_3 + sC_1) = [V_o - (B_1V_o + B_2V_o{}^2 + B_3V_o{}^3)]sC_2 \tag{2.55}$$

Also the non-linear relationship between the $V_o$ and $I_i$ is modeled by the following

$$V_o = Z_1I_i + Z_2I_i^2 + Z_3I_i^3 \tag{2.56}$$

Where $Z_1$, $Z_2$ and $Z_3$ are the total impedance, second order coefficient and third order coefficient of impedance respectively.

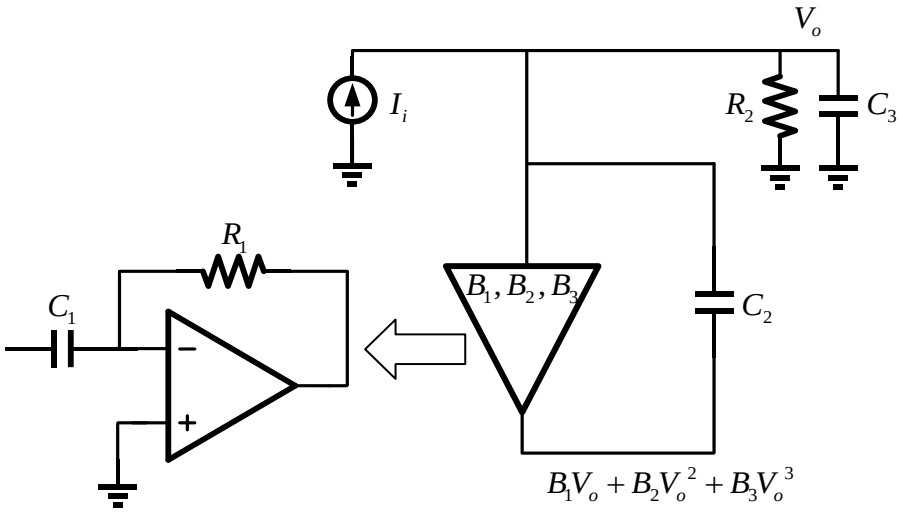



Figure 36 Non-linear model of proposed filter

Similarly, by substituting equation (2.56) into equation (2.55) and ignoring the higher order terms, we obtain the following.

$$Z_1 = \frac{R_2}{1+s(C_1+C_3)R_2+sC_2R_2(1-B_1)} \tag{2.57}$$

$$Z_2 = \frac{sC_2{R_2}^3B_2}{[1+s(C_1+C_3)R_2+sC_2R_2(1-B_1)]^3} \tag{2.58}$$

$$Z_3 \approx \frac{sC_2{R_2}^4B_3}{[1+s(C_1+C_3)R_2+sC_2R_2(1-B_1)]^4} \tag{2.59}$$

By using the equation (2.14) and (2.15), equation (2.56) can be rewritten as the voltage source equivalent form

$$V_o = H_1V_i + H_2V_i^2 + H_3V_i^3 \tag{2.60}$$

And the coefficient $H_1$, $H_2$ and $H_3$ can be found easily from $Z_1$, $Z_2$ and $Z_3$ respectively by the following

$$H_1 = \frac{Z_1}{2R_2} = \frac{1/2}{1+s(C_1+C_2+C_3)R_2+s^2C_1C_2R_1R_2} \tag{2.61}$$

$$H_2 = \frac{Z_2}{2{R_2}^2} = \frac{sC_2R_2B_2}{4[1+s(C_1+C_2+C_3)R_2+s^2C_1C_2R_1R_2]^3} \tag{2.62}$$

$$H_3 = \frac{Z_3}{8{R_2}^3} \approx \frac{sC_2R_2B_3}{8[1+s(C_1+C_2+C_3)R_2+s^2C_1C_2R_1R_2]^4} \tag{2.63}$$

The $IM_3$ of the filter is given by

$$IM_3 = \frac{3}{4}\left|\frac{H_3}{H_1}\right|V_i^2 \tag{2.64}$$

Where $H_1$ is transfer function of the filter because it is exactly the same as equation (2.10). By substituting equation (2.61) and (2.63) into equation (2.64), the $IM_3$ is reduced to

$$IM_3 = \frac{12sC_2R_2A_3\alpha^3H_1^3}{(1+A_1\beta)^4}V_i^2 \tag{2.65}$$

Since the passive components are determined by filter transfer function, the $IM_3$ is mainly depends on the OTA gain $A_1$ and third order distortion coefficient $A_3$. Hence, increasing the gain of OTA and using large $V_{dsat}$ for the input transistor of the second stage to reduce the distortion coefficient $A_3$ are the two effective ways to improve the linearity.

# 3. CIRCUITS IMPLEMENTATION

In section 2, some system level design considerations are presented. In this section, the circuit level design details are explained.

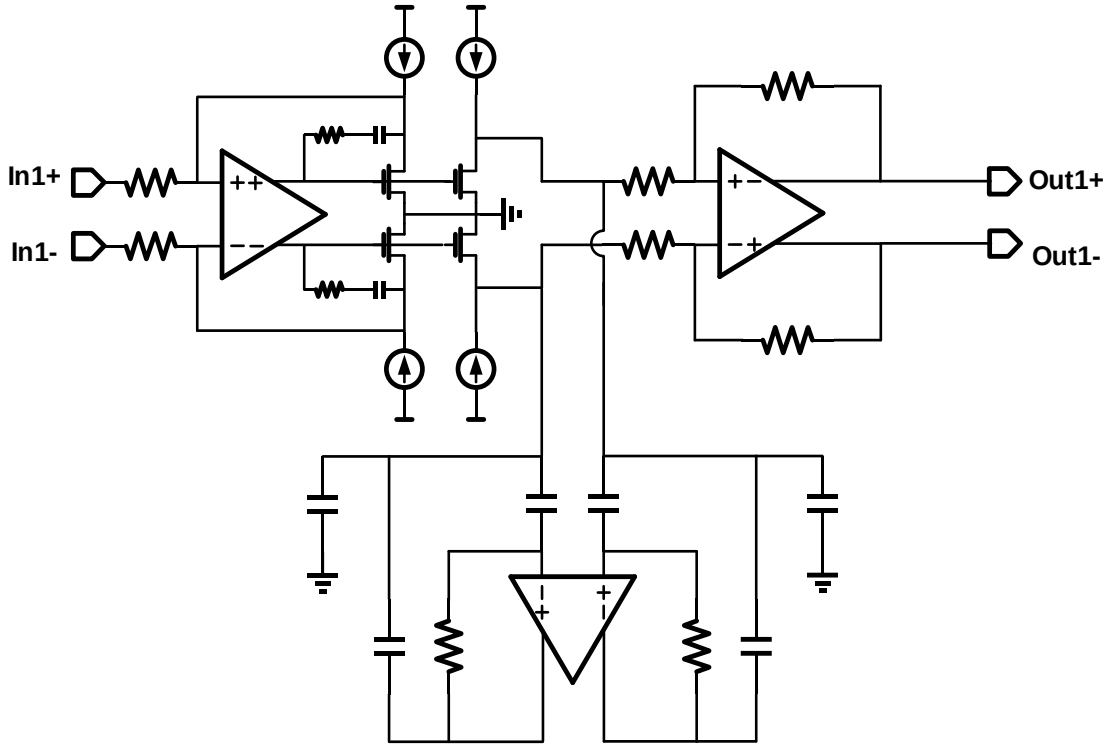



Figure 37 Top level on-chip schematic

Figure 37 illustrates the top level building blocks on-chip and all the circuits are fully differential. The first block is a voltage-to-current converter which pumps ac current to the filter because the filter is designed driven by a current source. Then followed by the proposed low-pass filter. The output node of the filter is very sensitive

because any large load such as pad frame, pin or probe of oscillators would affect the filter transfer function. Therefore, an output buffer is needed to drive the large loads mentioned above for measurement. The design detail of each building blocks are discussed in the rest of this section.

### 3.1 Class-AB OTA

The OTA for the filter is the most critical block. According to the conclusions drawn in section 2, the total transconductance should be large to provide enough attenuation of the filter transfer function. Also, the parasitic capacitance at the output of the first stage should be minimized for stability so that most of the transistors are designed with minimum channel length and no Miller compensation is used. Figure 38 shows the schematic of the proposed class-AB OTA and the dimensions and values of devices are listed in table 3. The input transistors M1 are designed with low value of $V_{dsat}$ (96mV) to increase the gain of the first stage and better matching. For the transistor M3 and M4 in the second stage, they are designed with relatively high $V_{dsat}$ (120mV) for better linearity as well as a good current efficiency. Since M2 and M3 are 1-to-1 ratio current mirror, the total current in the second stage is about the same as the first stage whose current is 500uA. So the total current of the OTA is 1.1mA including the current of the error amplifier. With the power supply of 1.2V, the total power consumption is only 1.3mW.

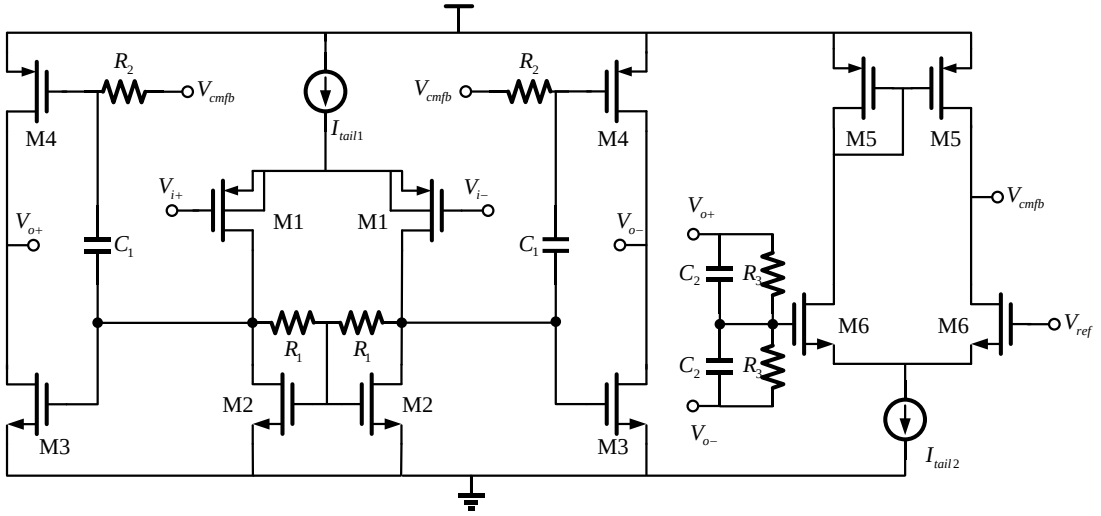



Figure 38 Class-AB OTA schematic

Table 3 Details of components for OTA in Figure 38

| Device | Dimensions/Value | Device | Dimensions/Value |
|---|---|---|---|
| M1 | (24) 4.2um/120nm | M4 | (10) 2.2um/120nm |
| M2 | (8) 1um/120nm | M5 | (2) 2.2um/120nm |
| M3 | (8) 1um/120nm | M6 | (6) 1um/120nm |
| $I_{tail1}$ | 500uA | $R_2$ | 100kΩ |
| $I_{tail2}$ | 100uA | $R_3 \parallel C_2$ | 32kΩ ‖ 60fF |
| $R_1$ | 32kΩ | $C_1$ | 1.5pF |

### 3.1.1 Input stage

The input stage is PMOS differential pair with local common-mode feedback. Compared with NMOS differential pair, the PMOS one has some advantages. First is the lower flicker noise. There are two main theories that have been developing in the past regarding the flicker noise. The one is called the number fluctuation theory stating that there are some traps in the $SiO_2$ – Si interface, randomly trapping and releasing charge carriers of the channel and thus fluctuating their number. The other one attributes the flicker noise to the random mobility fluctuations caused by lattice scattering. Today, these two theories combines together by correlating the traps' capture and release of carriers to the mobility fluctuation due to Coulomb scattering [5]. The unified theory gives the input referred noise density of

$$V_n(f) = \frac{K}{C_{ox}{}^2 WL}\frac{1}{f} \tag{3.1}$$

Where K is not only a process-dependent constant, but also bias point dependent. The typical K for PMOS is around $10^{-32}$ $C^2/cm^2$ and $4*10^{-31}$ $C^2/cm^2$ for NMOS. The lower K factor of PMOS is because oftentimes the NMOS channel is right under the $SiO_2$ – Si interface, while the PMOS channel is farther below the surface, less affected by the traps. In addition, PMOS transistors have smaller larger area for a given gm and current because of the lower channel mobility. From equation (3.1), it is obvious that the larger the device area, the smaller the flicker noise.

Second, it helps to achieve a better matching and Common-mode rejection. In the process of fabrication, there are always variations among transistors that you want to be

the same. One of the sources is dopant fluctuation, which means the number of dopant ions implanted inside each channel of devices is different. This phenomenon is pretty substantial for modern sub-micron technology. Another one is called line-edge roughness, meaning that we cannot get a perfect straight line for the edges of device but a rough line. Because these sources of variation are random, we can see from a statistic viewpoint the mismatch as a Gaussian distribution with zero mean. Threshold voltage mismatch is one of the major concern, which can be mathematically described by the following equation [4].

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}} \tag{3.2}$$

Where $A_{VTH}$ is proportionality factor.

So the mismatch is inversely proportional to the square root of the transistor area. For example, 1.8nm variation of channel length is 1% of the 180nm device, while it could be 10% of the 18nm device. Thus the size of the device provides a sort of averaging for the process variation and thus yield better matching. For providing the same transconductance, PMOS transistors have bigger size than the NMOS and thus better matching.

Another benefit of PMOS is that the bulk terminal can be connected to the source terminal in N-well process. Recall that the threshold voltage is given by

$$V_{TH} = V_{TH0} + \gamma(\sqrt{V_{SB} + 2|\phi_F|} - \sqrt{2|\phi_F|}) \tag{3.3}$$

$V_{SB}$ is not zero in the NMOS differential pair. There is also probably certain mismatch in the body effect coefficient $\gamma$ of two input NMOS transistors, further degrading the

mismatch of threshold voltage. Conversely, by shorting the bulk and source, $V_{SB}$ in the PMOS differential pair is equal to zero, eliminating the body effect. So the $V_{TH}$ mismatch in PMOS differential pair is better than NMOS.

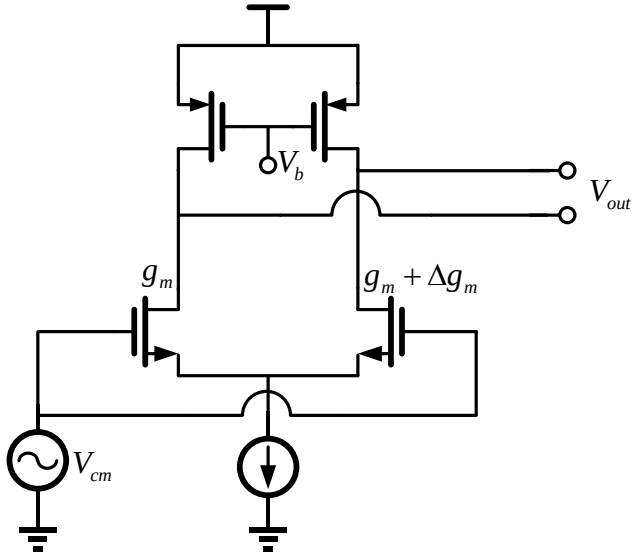



Figure 39 Input differential pair with mismatch

If a differential pair is perfectly symmetrical, the common mode input voltage will create the same output voltage at two branches and the differential output is zero. However, as shown in Figure 39, if the input transistors experience mismatch in $g_m$, the output voltages at two branches are different, creating a certain differential output voltage. Thus, mismatch results in common- mode to differential-mode conversion. The definition of common-mode rejection ratio (CMRR) is given by [4]

$$\mathrm{CMRR} = \left| \frac{A_{DM}}{A_{CM-DM}} \right| \tag{3.4}$$

So we can say that the PMOS differential pair has larger CMRR than NMOS because it has better matching and thus less common- mode to differential-mode conversion

Last but not least, since the common-mode voltage at the output of the PMOS differential pair is usually lower than half of $V_{dd}$ (PMOS tail current source eats some voltage headroom), the input device of the second stage should be NMOS to achieve a reasonable overdrive voltage. Thus, there is smaller parasitic capacitance at the first stage's outputs, which is critical for the stability of the filter.

### 3.1.2 Class-AB operation

The output of the first stage is also ac-coupled to the PMOS transistors of the second stage. The resistor $R_2$ and capacitor $C_1$ forms a high pass filter with corner frequency of $1/R_2C_1$. Below this frequency, the signal is attenuated by the high pass RC filter and thus the OTA just behaves like a class-A stage. Above the corner frequency, the path is active and PMOS transistors amplify the signal, meaning that the $g_m$ of the PMOS transistors is directly added to the total $g_m$ of the second stage. Compared with class-A OTA where the PMOS transistors in the second stage are only serve as current source, this class-AB operation reuses the wasted current on that PMOS loads for processing signal.

### 3.1.3 Common mode feedback

In fully differential circuits, the common-mode feedback (CMFB) is needed to define the common-mode level. There are unavoidable mismatches between the PMOS and NMOS current sources which are independently biased in fully differential circuits. As shown in Figure 40, the difference of the NMOS and PMOS current source flows

into the output resistor of the amplifier, creating the an voltage change of $(I_P\text{-}I_N)(R_P\|R_N)$. Because $R_P\|R_N$ is usually quite large, the error voltage may be substantial, deviating the CM level from desired value a lot. In the worst case, the transistors may go to the triode region and the circuit would not work properly.

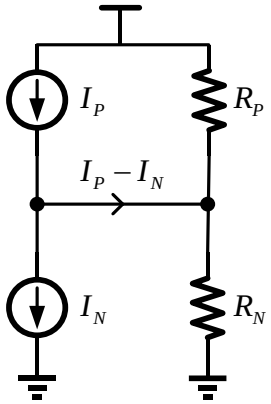



Figure 40 Simplified model of amplifier

The CMFB is a negative feedback loop whose block diagram is illustrated in Figure 41. The loop senses the output CM level first and then compared with a reference voltage. The difference between the two is then amplified by an error amplifier, whose output is connected to one of the independent current source. The negative feedback will force the sensed CM level to be equal to the reference voltage by adjusting the tail current source in this example.

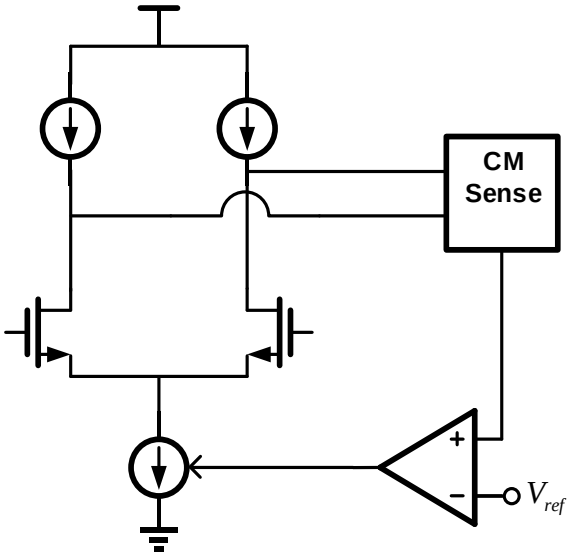



Figure 41 Block diagram of CMFB

Typically for two stage OTA, the common-mode voltage of both stages should be stabilized. One way of doing this is to feed the common mode control signal to the first stage, then the common mode voltage of the second stage is automatically controlled. However, there are three stages in the CMFB loop including the error amplifier, which complicates the compensation and limits the loop bandwidth. The other way is to apply the common mode feedback loop to the second stage only while using a local common mode feedback in the first stage. The proposed class-AB OTA utilizes the CMFB approach in Figure 38. The local common-mode feedback in the first stage is realized by two resistor $R_1$ which forms a common-mode detector to sense the common-mode voltage at the drain of M2 and then feed to its gate. Since the differential signal is cancelled out at the gate of M2, this point is an AC ground. And thus the differential gain of the first stage is

$$A_{v1} = g_{m1}(R_P \parallel R_N \parallel R_1) \tag{3.5}$$

As long as the $R_1$ is much greater than the intrinsic output impedance of the amplifier, it will not degrade the gain of the first stage. Since the current in the first stage is relatively high and the $R_P$ and $R_N$ are around 5kΩ, the $R_1$ is chosen as 32kΩ. So the first stage is self-biasing due to the local common-mode feedback and the second stage is applied with an external CMFB circuit. This approach makes the CMFB loop easy to compensate and the detailed reason will be discussed in section 3.3.

The CMFB is usually verified in two ways. One way is to simulate frequency response of the CMFB loop to see the loop gain, bandwidth and phase margin. The other way is transient response as illustrated in Figure 42. The amplifier is kept in a closed-loop form and the input is connected to the same common-mode level, which means the differential input signal is muted. Then a pair of identical current pulse is connected to the output. And the peak value of the current pulse is set as 10% of the DC current of the output stage. The CMFB will adjust the bias and identical step response will appear at both output nodes.

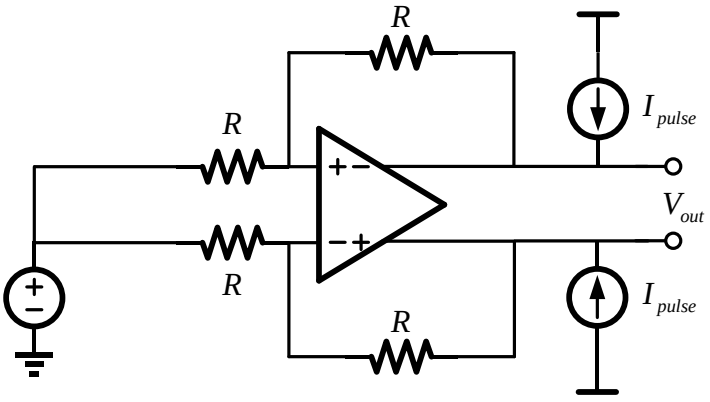



Figure 42 Transient response test setup for CMFB

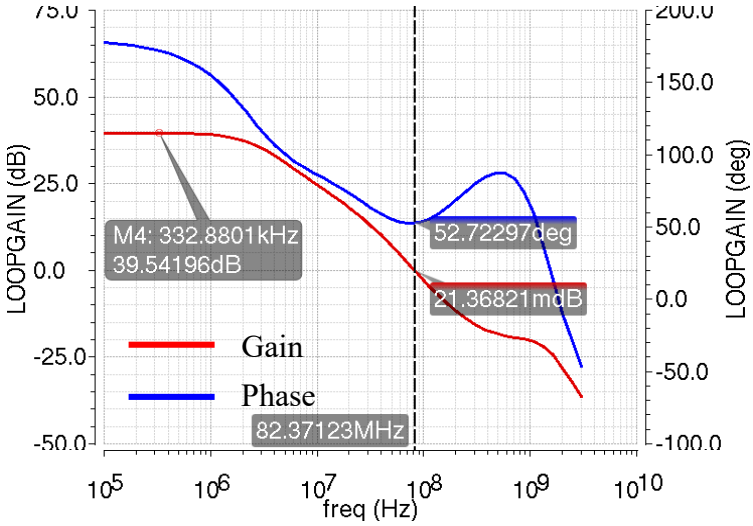



Figure 43 AC response of CMFB for class-AB OTA

The frequency response of the CMFB in the class-AB OTA at nominal point is shown in Figure 43. In order to improve the loop gain, the error amplifier in Figure 38 is using a single-ended OTA instead of OTA with diode connected load. The loop gain is around 40dB with a unity gain frequency of 82MHz. The phase margin is 52 degree in this case and it is greater than 45 degree for all the different corners and temperature.

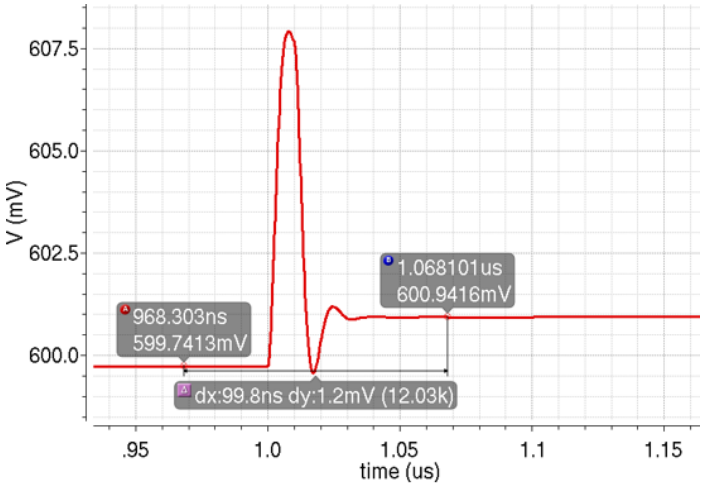



Figure 44 Transient response of CMFB for class-AB OTA

Figure 44 shows the transient response of the common mode feedback loop. The CMFB settles the final output voltage with an offset about 1mV.

### 3.1.4 Performance summary

The AC response of the class-AB OTA without loading is shown in Figure 45. The gain of OTA at DC is 36dB and begins to increase around 300kHz due to the class-AB operation. The gain achieves the peak value of 41dB at 10MHz. Since the open-loop transfer function of filter determines the stability, the phase margin of the OTA alone is meaningless.

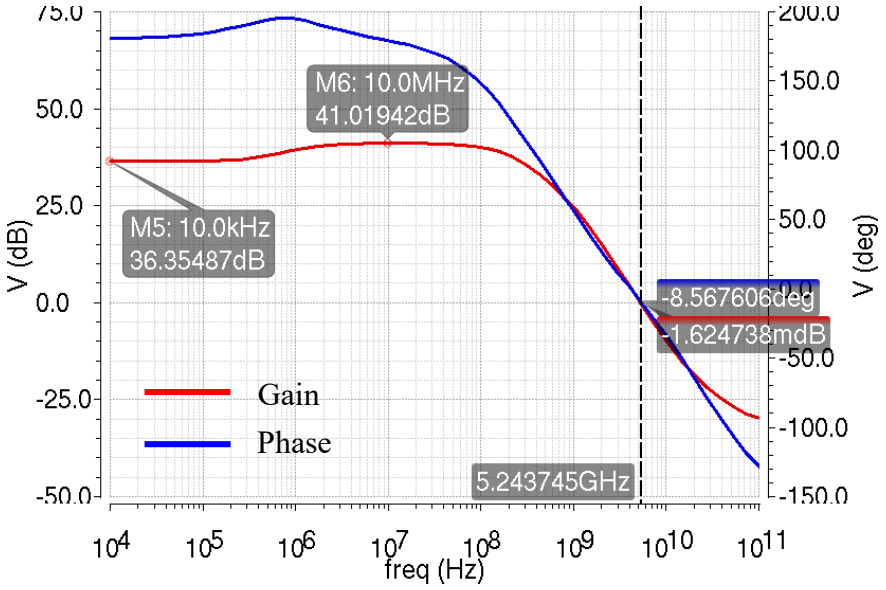



Figure 45 AC response of the class-AB OTA without loading

Figure 46 shows the spectrum and transient at the class-AB OTA differential output, when the full-scale input of the filter is used for two-tone test.

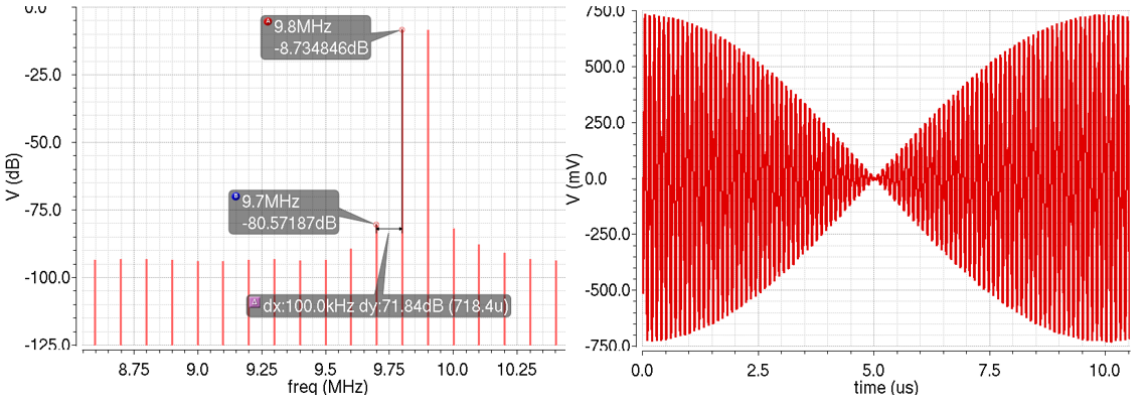



Figure 46 Differential output spectrum and transient of class-AB OTA

And the performance is summarized in Table 4. The in-band integrated noise is relatively large in the OTA because of the considerable flicker noise caused by using minimum channel length in the transistors. From the analysis in section 2.3.5, the noise of OTA has little effect on the output noise of the filter and thus it is more important to guarantee the stability by using small transistors.

Table 4 Class-AB OTA performance summary

| **Performance parameter** | **Value** |
|---|---|
| DC gain | 36dB |
| Peak gain | 41dB |
| Unity gain frequency | 5.2GHz |
| Input referred integrated noise (1Hz- 10 MHz) | 80uV |
| IM3 ($1.46V_{ppd}$) | -71.8dBc |
| Power consumption | 1.3mW |

### 3.2 Voltage-to-current converter

Since the filter is designed driven by a current source, an on-chip voltage-to-current converter is needed to perform this task and also serves as a good interface with external test circuits. The main design challenge is the linearity because the filter has an in-band $IM_3$ above 70dBc. Thus, the voltage-to-current converter (V-I converter) must be very linear without limiting the linearity performance of the filter. For such a high linearity requirement, the negative feedback is necessary to be used and a common solution is illustrated in Figure 47. The input voltage is copied at the negative terminal of the amplifier and then converted to linear current by the resistor R. Nevertheless, the difference between the input and output of the amplifier has to be the $V_{GS}$ of the NMOS transistor, which is difficult to realize in 1.2V power supply.

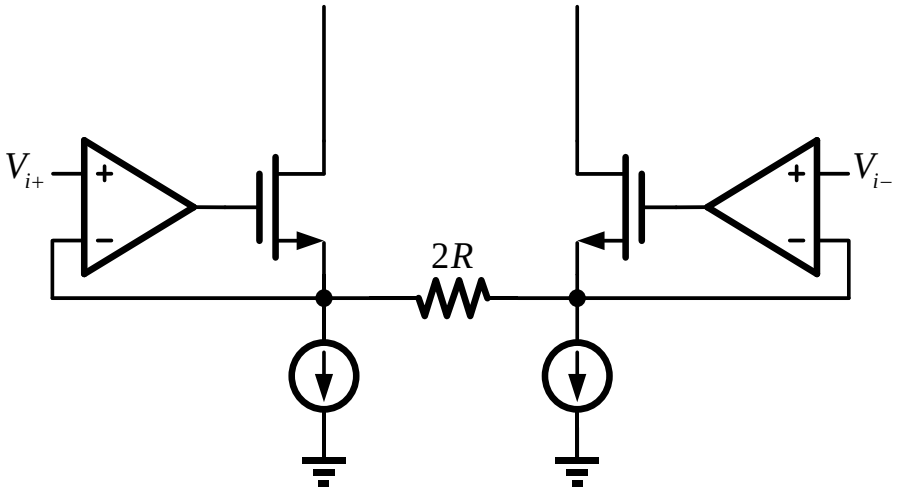



Figure 47 Typical linear voltage-to-current converter

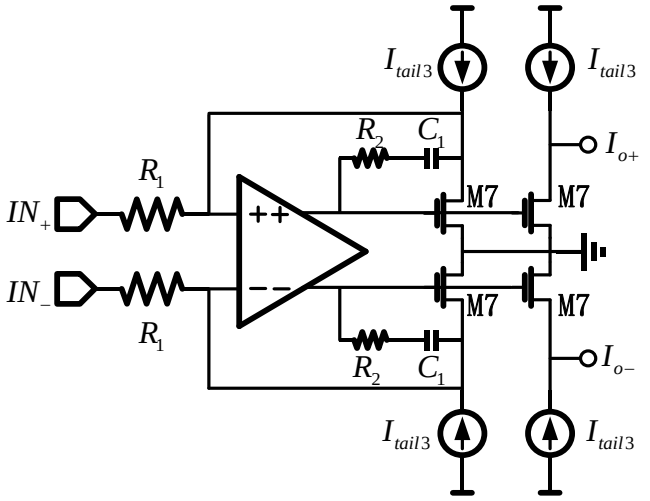



Figure 48 Proposed voltage-to-current converter

The proposed topology of voltage-to-current converter is shown in Figure 48. The amplifier makes the input terminal a virtual ground and the input voltage is converted to current by the resistor $R_1$ and flow into M7. The replica of M7 stage is made to copy the linear current and feed it to the filter. The $R_2$ and $C_1$ are the typical Miller compensation for the loop stability.

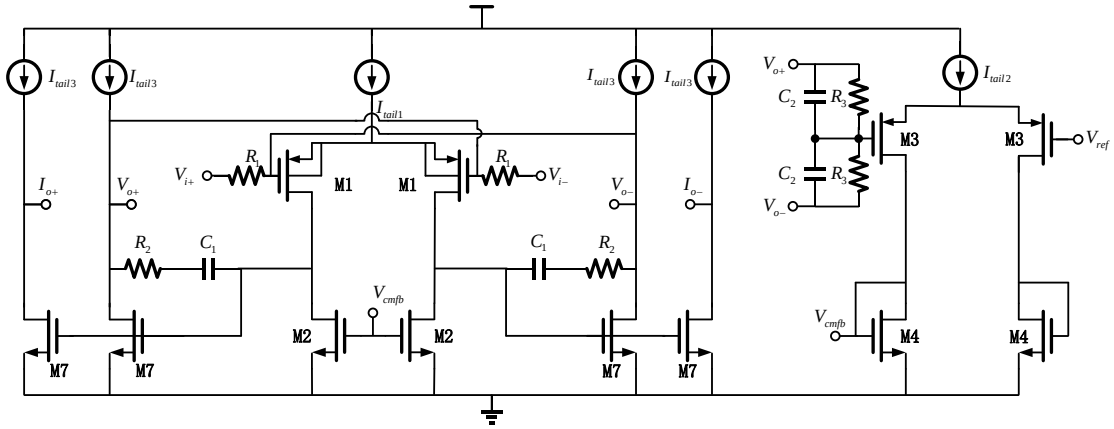



Figure 49 Complete circuits of V-I converter with single stage OTA

For simplicity, the amplifier can be a single-stage differential pair with common-mode feedback circuit. The complete circuits of voltage-to-current converter with this simple OTA is shown in Figure 49. However, this simple OTA causes a CMFB issue that actually exists in many closed-loop application of the amplifiers.

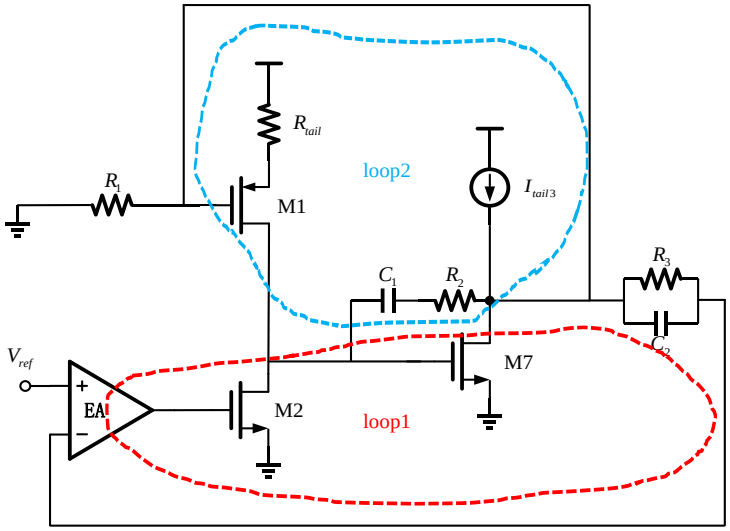



Figure 50 Common-mode half circuits of Figure 49

The common-mode half circuits are shown in Figure 50, where the error amplifier (EA) is illustrated as a symbol. Besides of the typical CMFB loop (loop1), there is also another positive feedback loop (loop2) which is formed by the negative feedback configuration of amplifier. Ideally, the gain of loop2 is below unity because the source degeneration of the first stage. However, when the bias current is high in submicron technology, the output resistor of the tail current source $R_{tail}$ is no more than 10kΩ. By using the small signal parameters given by DC simulation, it is found that the gain of loop2 is actually greater than unity and even comparable with loop2. Then the

frequency response shown in Figure 51 somehow becomes a positive feedback because the phase starts at zero. And there is even oscillation in the transient response, which will fail the normal operation of circuits.

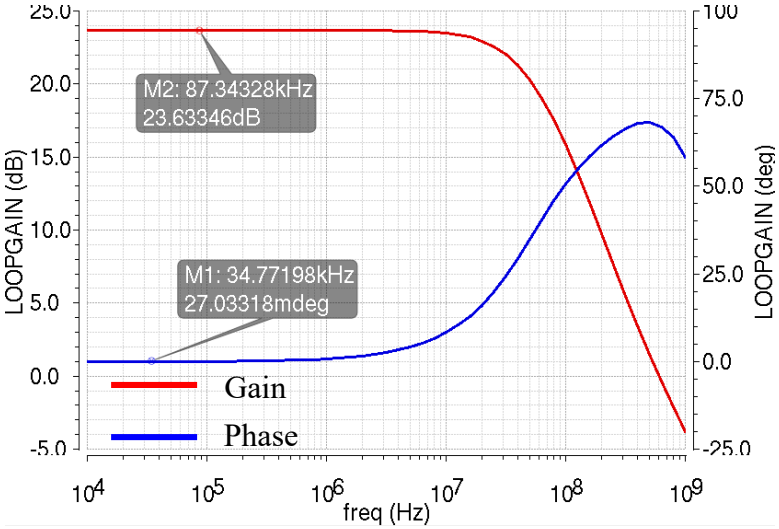



Figure 51 AC response of CMFB in Figure 49

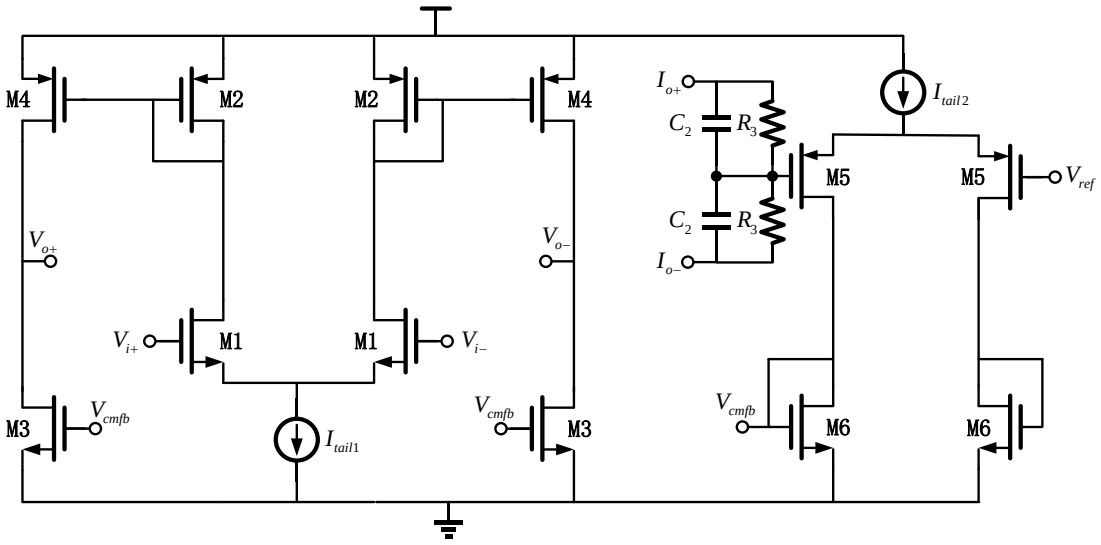



Figure 52 Current mirror OTA for proposed V-I converter

In order to solve this issue, a current mirror OTA is proposed as shown in Figure 52. And its device dimensions and components values are listed in Table 5.

Table 5 Details of components for OTA in Figure 52

| Device | Dimensions/Value | Device | Dimensions/Value |
|---|---|---|---|
| M1 | (4) 3um/200nm | M5 | (12) 4um/200nm |
| M2 | (4) 4um/200nm | M6 | (4) 3um/200nm |
| M3 | (4) 3um/200nm | M7 | (4) 4um/300nm |
| M4 | (4) 4um/200nm | $R_1$ | 1.5kΩ |
| $I_{tail1}$ | 240uA | $R_2$ | 1.1kΩ |
| $I_{tail2}$ | 270uA | $R_3$ ‖$C_2$ | 32kΩ ‖ 60fF |
| $I_{tail3}$ | 260uA | $C_1$ | 200fF |

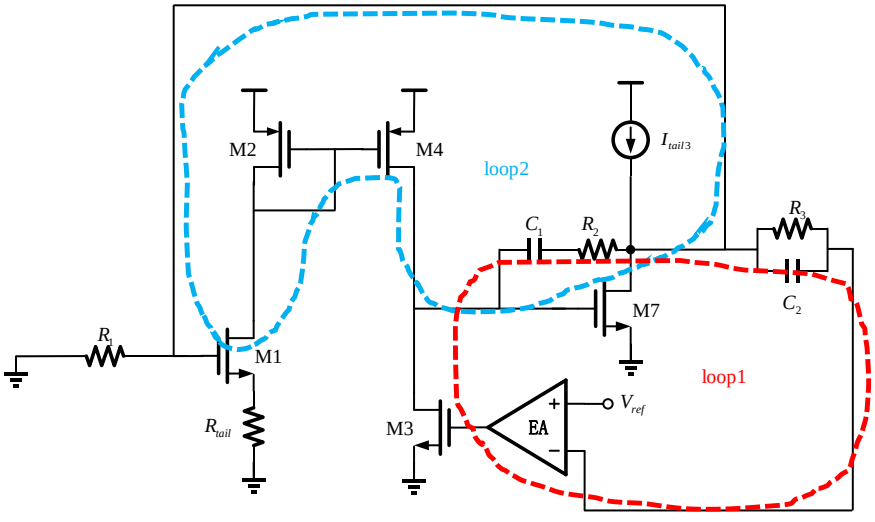



Figure 53 Common-mode half circuits of V-I converter with current mirror OTA

The common-mode half circuits of the voltage-to-current converter with proposed current mirror OTA are drawn in Figure 53. The reason why using current mirror OTA is that it provides an additional stage in the common-mode circuit analysis compared with single-stage OTA. So the loop2 becomes a negative feedback one, eliminating the positive feedback problem.

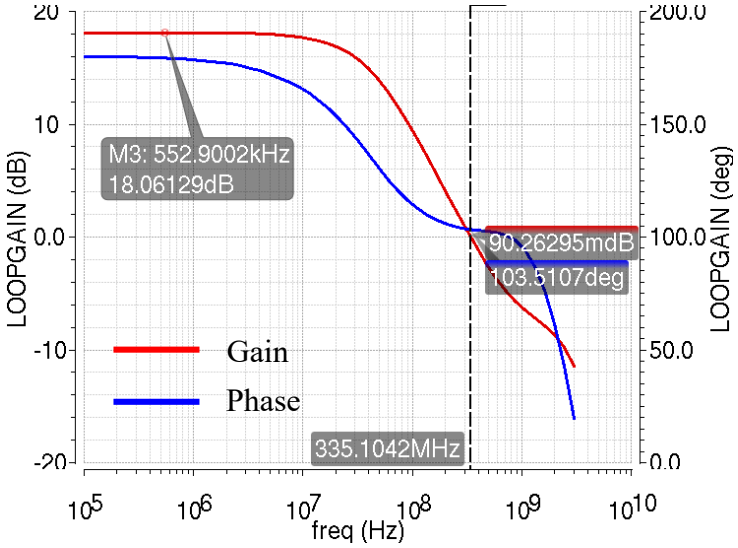



Figure 54 AC response of CMFB in V-I converter with current mirror OTA

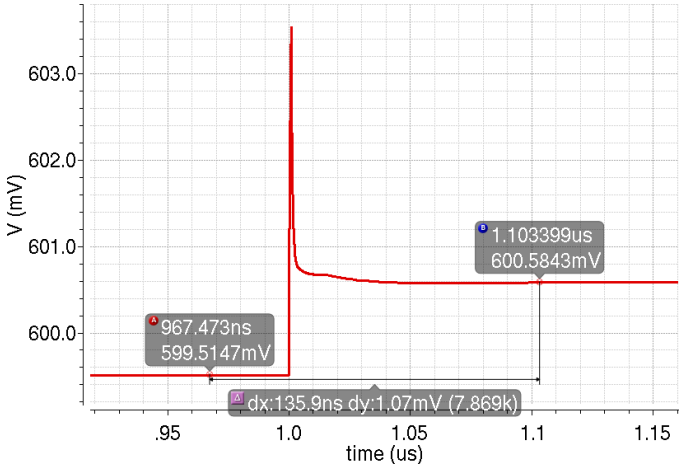



Figure 55 Transient response of CMFB in V-I converter with current mirror OTA

Figure 54 shows the frequency response of the CMFB loop. It has a gain of 18dB, unity gain frequency of 335MHz and a 103 degree of phase margin. When injecting the common-mode current pulses to the output, the transient response is shown in Figure 55. The output voltage settles with an offset of 1mV.

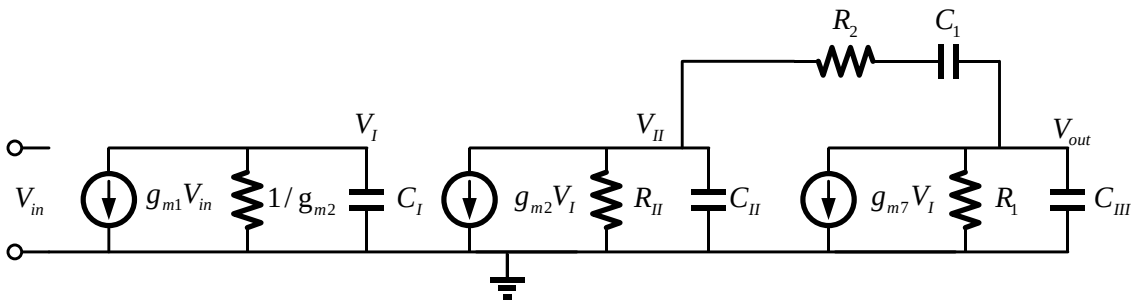



Figure 56 Small signal model of loop gain in proposed V-I converter

Figure 56 shows the small signal model of the open-loop transfer function, where $C_I$, $C_{II}$ and $C_{III}$ are the parasitic capacitance at the mirror node, output of the OTA and drain of M7 respectively. And $R_{II}$ is the output resistor of the OTA. The open-loop has three poles and one zero at the following locations.

$$\omega_{p1} = -\frac{1}{R_{II}C_I g_{m7} R_1} \tag{3.6}$$

$$\omega_{p2} = -\frac{g_{m2}}{C_I} \tag{3.7}$$

$$\omega_{p3} = -\frac{g_{m7}}{C_{II}} \tag{3.8}$$

$$\omega_z = \frac{1}{(R_2 - 1/g_{m7})C_1} \tag{3.9}$$

The Miller capacitor $C_1$ makes $\omega_{p1}$ the dominant pole and $\omega_{p2}$ is lower than $\omega_{p3}$ because $C_1$ contains two $C_{gs}$ at the mirror node. The right-half plane zero $\omega_z$ is compensated by resistor $R_2$ which is chosen to be equal to $1/g_{m7}$ to push the zero to infinite frequency in this design. For obtaining a phase margin of 60 degree, the two non-dominant pole $\omega_{p2}$ and $\omega_{p3}$ should be beyond twice the unity gain frequency. Thus the transistor M2, M4 and M7 are designed with high $V_{dsat}$ (200mV), which is also benefit for low distortion.

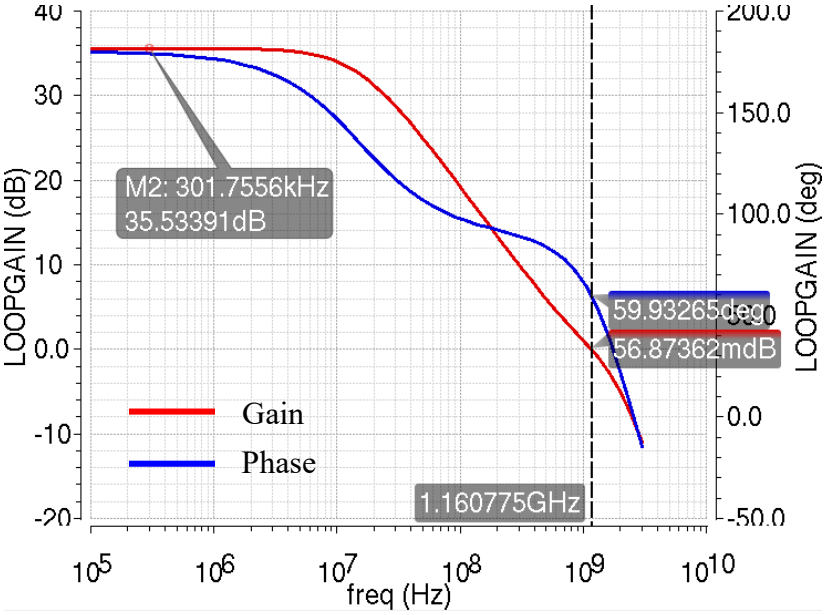



Figure 57 Open-loop response of V-I converter

Figure 57 shows the open-loop frequency response of the voltage-to-current converter. The open-loop gain is 35.5dB and 3-dB bandwidth is around 10MHz. Also, the phase margin is about 60 degree.

### 3.3 Output buffer

The output buffer is an inverting amplifier with the gain of unity shown in Figure 58. A typical class-A two-stage OTA shown in Figure 59 is used for the amplifier, whose design details are summarized in Table 6. Since the buffer has to drive the pad frame, bond wire and off-chip components, large bias current must be used for stability and linearity.

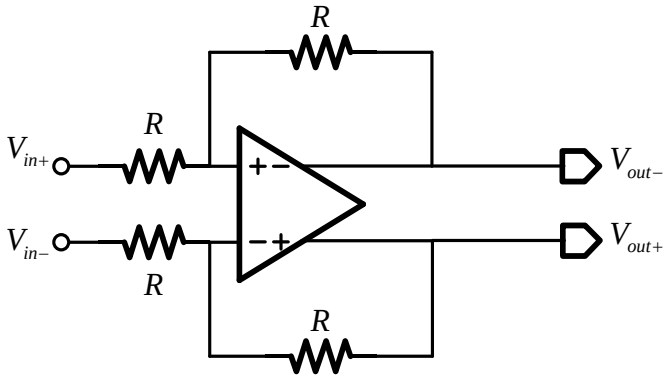



Figure 58 Output buffer schematic

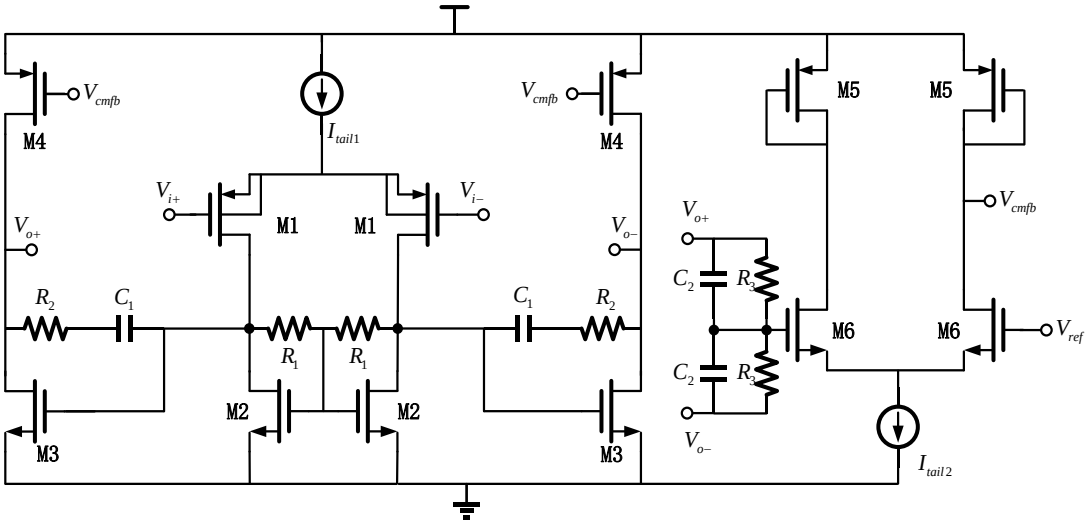



Figure 59 Schematic of OTA used in output buffer

Table 6 Details of components for OTA in Figure 59

| Device | Dimensions/Value | Device | Dimensions/Value |
|---|---|---|---|
| M1 | (24) 4.6um/150nm | M4 | (34) 4um/150nm |
| M2 | (12) 1.4um/150nm | M5 | (2) 4um/150nm |
| M3 | (24) 1.4um/150nm | M6 | (4) 1.4um/150nm |
| $I_{tail1}$ | 800uA | $R_1$ | 32 kΩ |
| $I_{tail2}$ | 100uA | $R_2$ | 1kΩ |
| $C_1$ | 940fF | $R_3 \parallel C_2$ | 32kΩ \|\| 60fF |

The OTA uses a local CMFB in the first stage and a typical CMFB for the second stage, similar to the class-AB OTA used in the filter. It also has the same CMFB issue discussed in section 3.2, but this local CMFB alleviates the problem. Again, the common-mode half circuits are drawn in Figure 60.

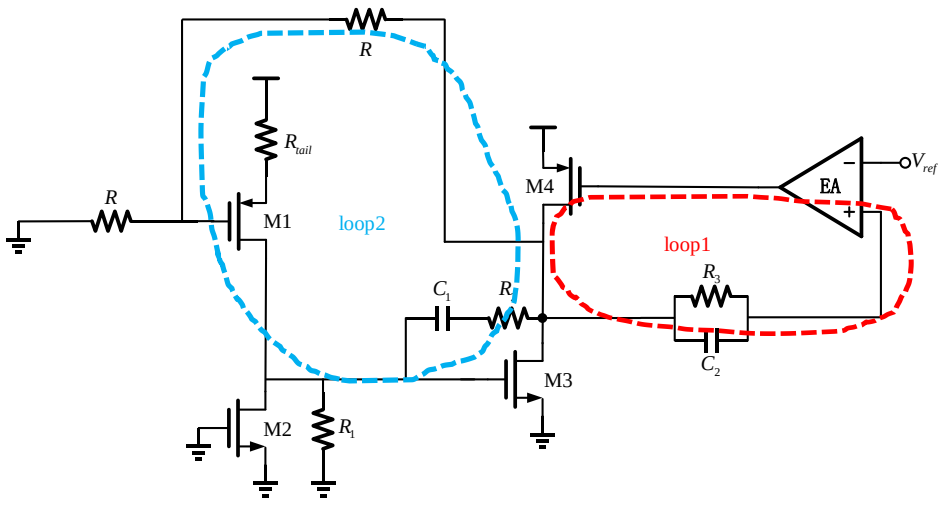



Figure 60 Common-mode half circuits of output buffer

Even though the loop2 is still a positive feedback, loop1 is less coupled with loop2 so that the open-loop frequency response is less affected and is shown in Figure 61. Also the transient response is shown in Figure 62.

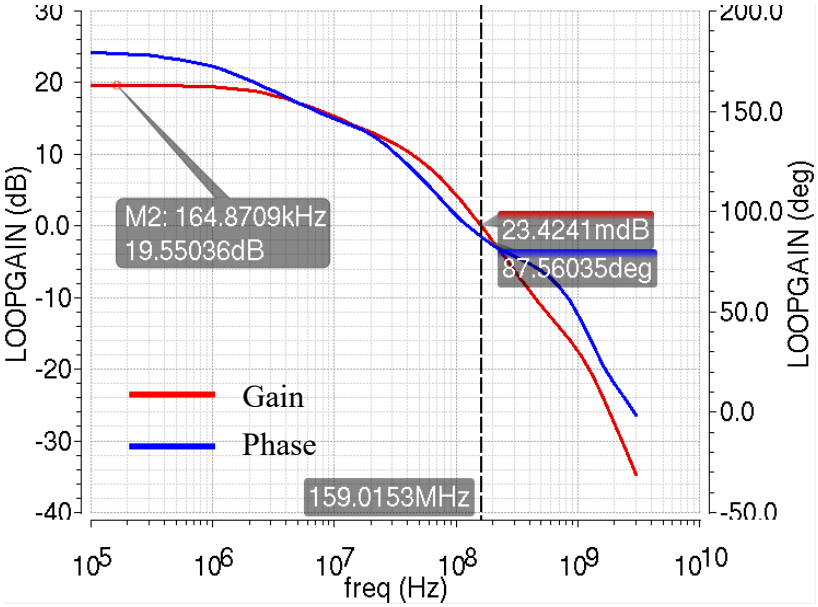



Figure 61 AC response of CMFB in output buffer

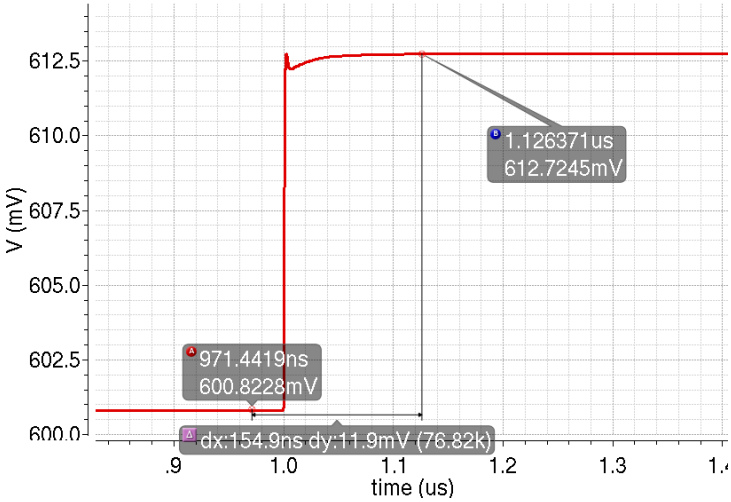



Figure 62 Transient response of CMFB in output buffer

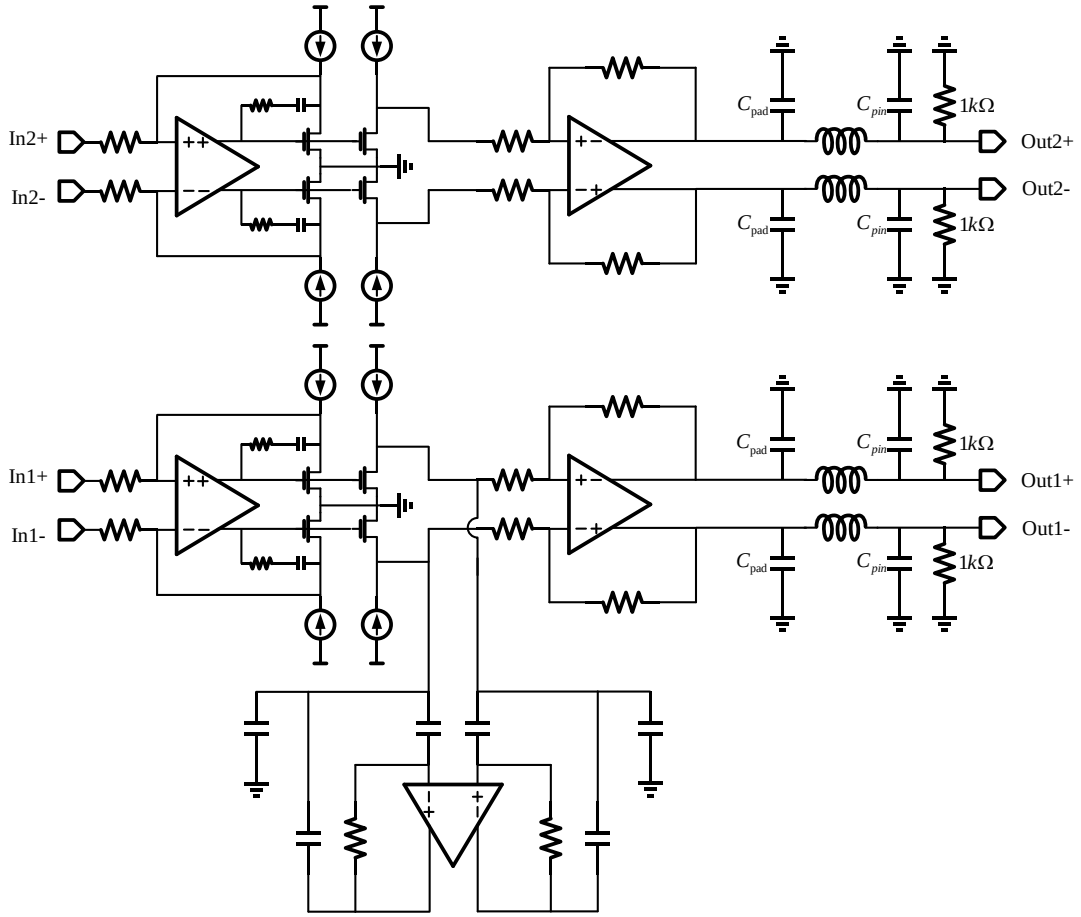



Figure 63 Top-level test circuits

Figure 63 shows the overall top-level test circuits. A replica of the voltage-to-current converter and output buffer is also placed on chip for noise characterization. The rms value of the noise from voltage-to-current converter, output buffer and filter can be measured at the output1. And at the output2, the rms noise from the voltage-to-current converter and output buffer can be measured. Then the rms value of noise from the filter itself can be obtained by subtracting the previous two noise measurement results. After

the output buffer, an inductor of 1nH is added to model the bond wire. Besides, the parasitic capacitance of the pin is modeled as 500fF and a resistor of 1kΩ will be added off-chip to avoid high-frequency oscillation.

### 4.1 Layout implementation

The chip layout with area of 1.1mm x 1.1mm is shown in Figure 64. And the layout was implemented in IBM 130nm technology (cmrf8sf). All the signal pads are connected to ESD diode and the connection of pins are listed in Table 7. The empty space of the chip is fully covered with decoupling capacitors for supply noise reduction.

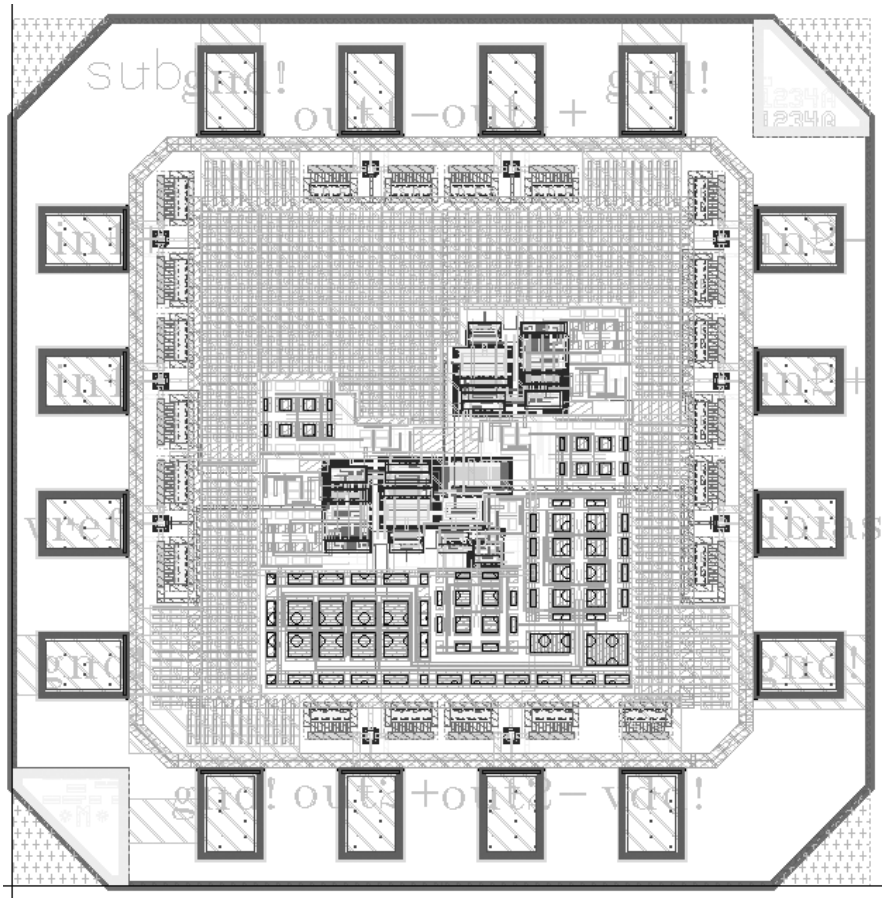


Figure 64 Chip layout

Table 7 Pin connections of chip layout

| Pin | Connection | Device | Dimensions/Value |
|---|---|---|---|
| In1+ | Input stimulus | Out1+ | 1kΩ resistor |
| In1- | Input stimulus | Out1- | 1kΩ resistor |
| In2+ | Input stimulus | Out2+ | 1kΩ resistor |
| In2- | Input stimulus | Out2- | 1kΩ resistor |
| Vdd | 1.2V | Vref | 0.6V |
| Gnd | 0V | ibias | 100uA |

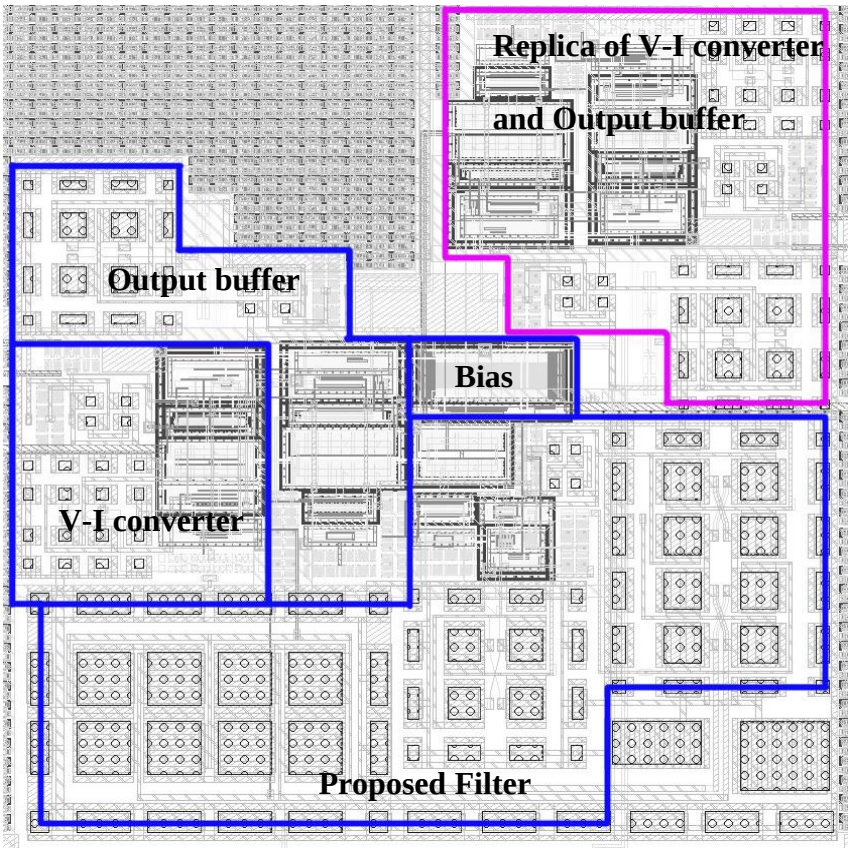



Figure 65 Building blocks on the layout

Figure65 shows the zoom-in version of every building blocks. And the area of the filter itself is about 0.08mm$^2$.

### 4.2 Post-layout simulation results

#### 4.2.1 Closed-loop frequency response

The comparison of closed-loop frequency response in schematic and post-layout simulation is shown in Figure 66 and Figure 67. The transfer function is $\frac{\text{Out1}}{\text{In1}}$ in Figure 63, so it includes voltage-to-current converter, filter, output buffer and passive components for modeling bond wire, pins and etc.

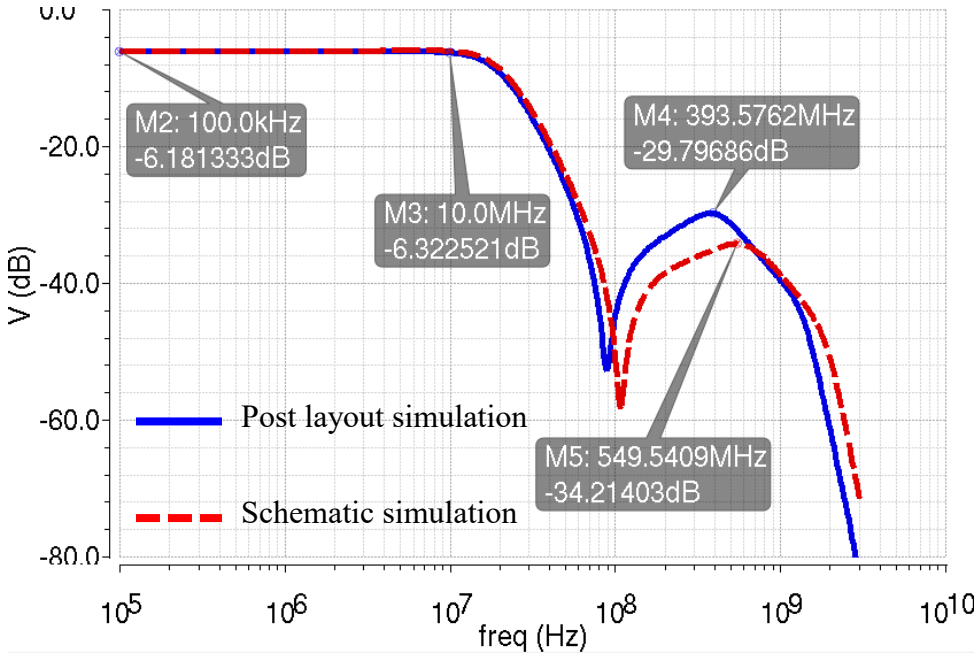



Figure 66 Closed-loop AC response comparison (Magnitude)

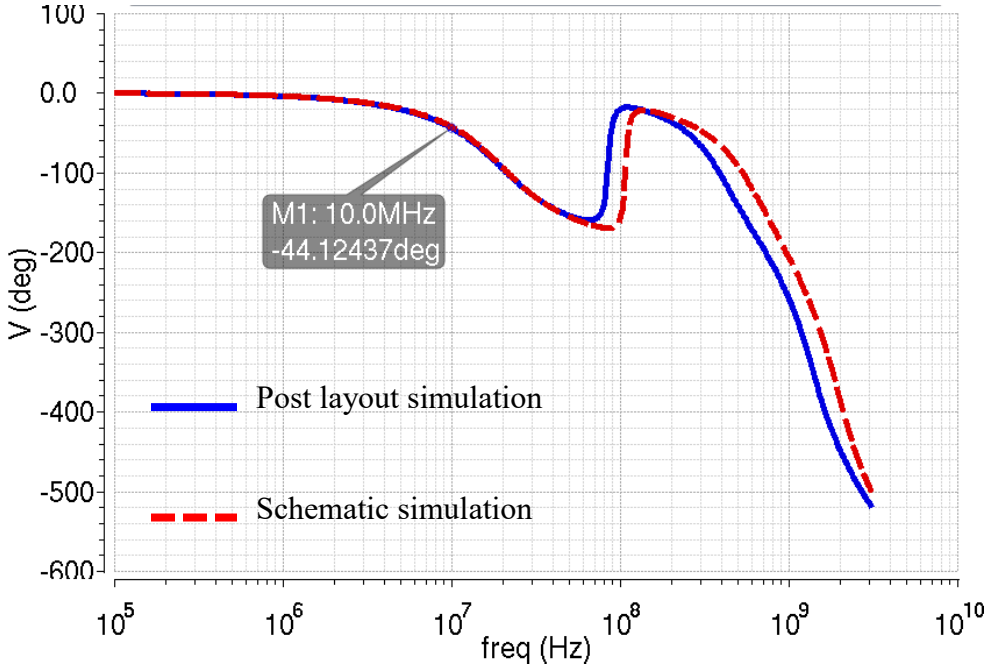



Figure 67 Closed-loop AC response comparison (Phase)

### 4.2.2 Open-loop frequency response

As derived in section 2.3.3, the open-loop phase margin depends on the parasitic capacitance at the first stage output of OTA. It is important to connect the top plate of the capacitor $C_1$to the output of the first stage in Figure 38, because the bottom plate has more parasitic capacitance to the ground, degrading the phase margin. The Figure 68 shows the open-loop frequency response of the filter. It shows that the open-loop gain at DC is 35.8dB and maintains a 28.6dB gain at the cutoff frequency 10MHz, which guarantees the linearity. Besides, at the unity gain frequency of 450MHz, the phase margin is 55 degree. The open-loop simulation is also run at different corners and temperature and the phase margin is always above 45 degree, which means the filter is stable.

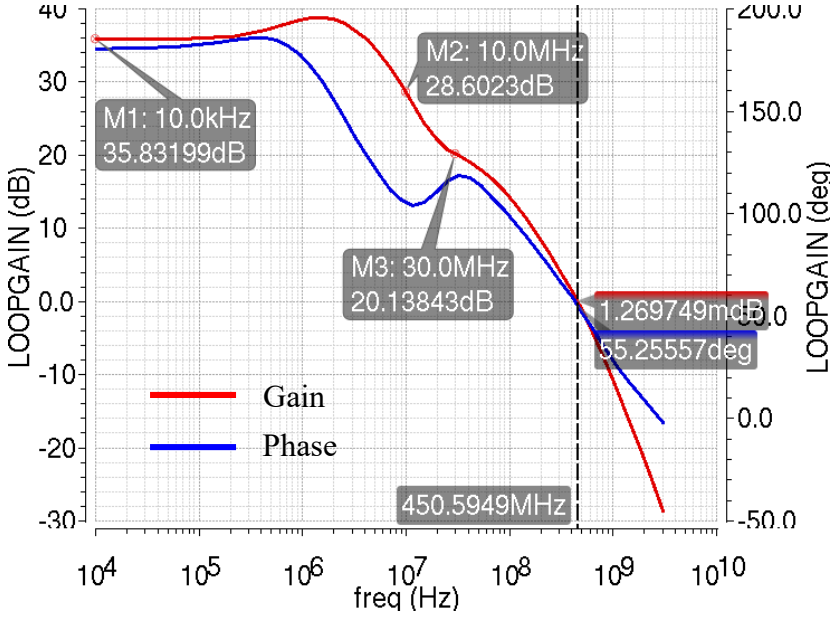



Figure 68 Open-loop AC response of filter

### 4.2.2 In-band linearity

It is often useful to measure the linearity with input signals close to the cutoff frequency [6]. Since the harmonic components of such signal fall out of the passband and are attenuated by the filter, the Total Harmonic Distortion (THD) is not able to report the performance of the filter. Thus, the two-tone third-order intermodulation ($IM_3$) test is used to report the linearity performance.

The full-scale input of the filter is two differential sinusoidal tones with the same amplitude of $600mV_{pp}$, which is applied at the input of the voltage-to-current converter. Due to the DC gain of one half, the output signal is $300mV_{pp}$ for each differential tone. The differential transient waveform of the input and output tones is shown in Figure 69.

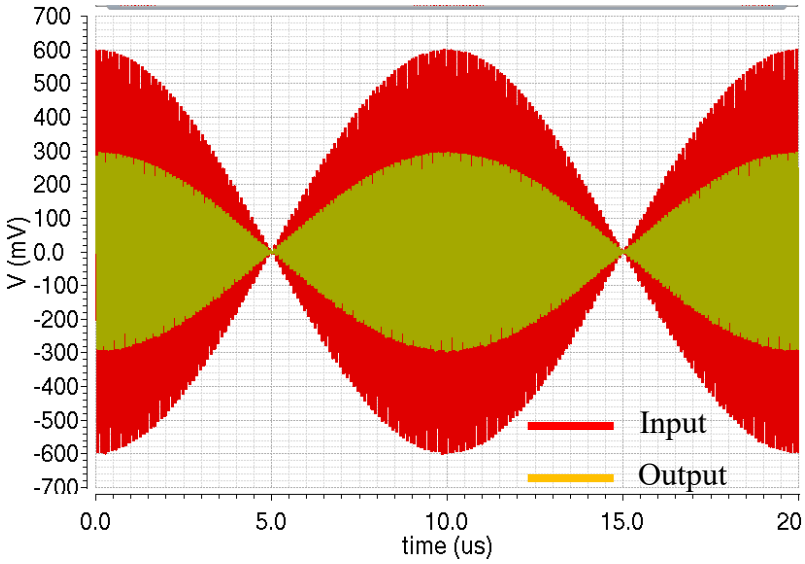



Figure 69 Transient waveform of two-tone test for in-band linearity

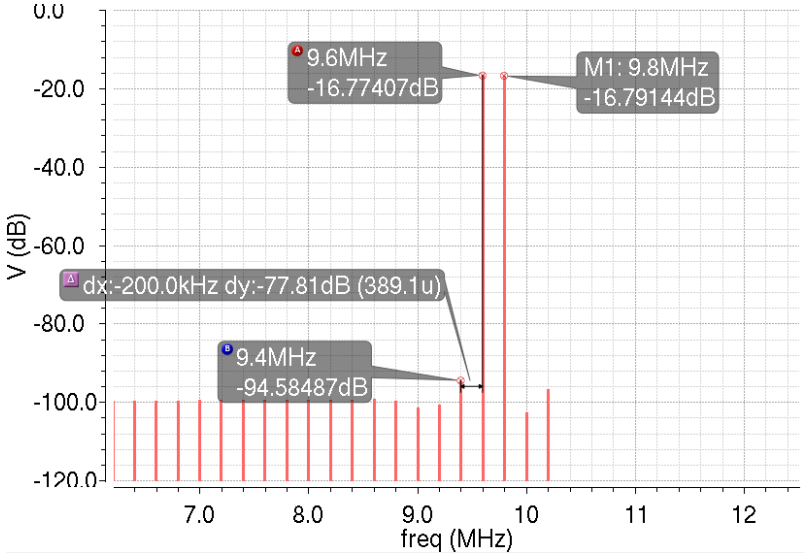



Figure 70 Output spectrum of two-tone test (9.6MHz and 9.8MHz)

The differential output spectrum is shown in Figure 70 and the $IM_3$ can be easily found as 77.8dBc.

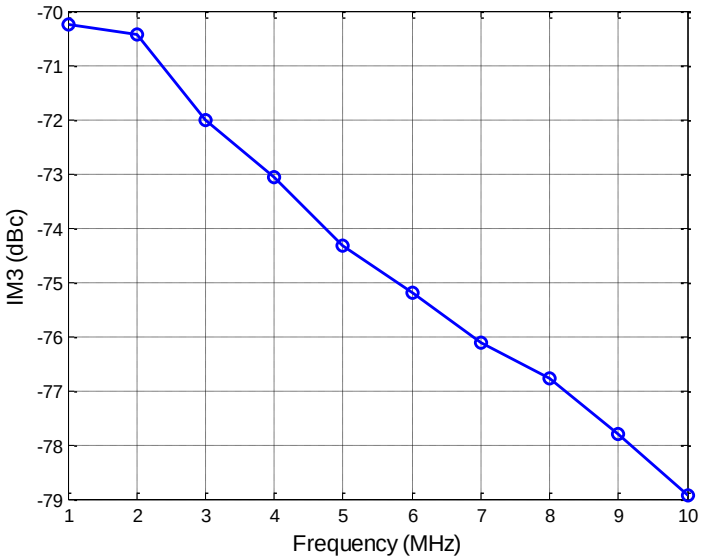



Figure 71 $IM_3$ performance versus frequency

Figure 71 shows the $IM_3$ performance at in-band frequency ranging from 1MHz to 10MHz. It can be seen that the $IM_3$ is better as the frequency approaching the cutoff frequency 10MHz. The reason is the class-AB operation gradually becomes more active so as to improve the linearity.

### 4.2.4 Out-of-band linearity

In digital television application, the signal at adjacent channels will become out-of-band blockers for the filter [7]. Around such frequency, the loop gain of filter is attenuated and not high enough to maintain a small error signal at the OTA input. Thus, the OTA has worse linearity at the frequency of blockers and the non-linear component falling in the passband will affect the wanted signal, degrading the SNDR.

In order to test the out-of-band linearity, two tones at 20MHz and 30MHz with full-scale amplitude ($600\text{mV}_{ppd}$) are applied to the input. The non-linear component in-

band will fall in 10MHz. And the differential output spectrum of the test is shown in Figure 72.

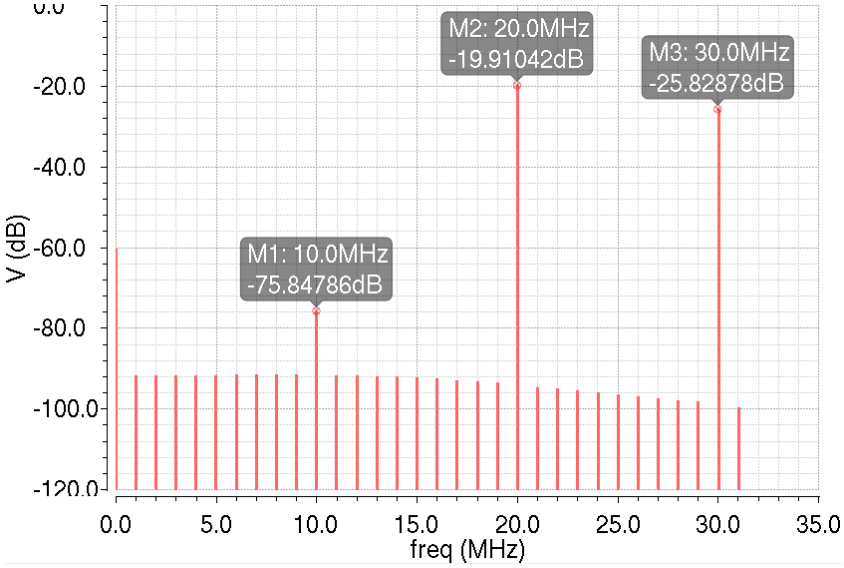



Figure 72 Output spectrum of two-tone test (20MHz and 30MHz)

Since the input tones are attenuated by the filter, the non-linear components should be compared with full-scale in-band output signal, which is 150m$V_{pkd}$, namely -16.47dBc. So the out-of-band $IM_3$ is -59.38dBc in Figure 72.

As shown in Figure 73, out-of-band $IM_3$ for two tones at 30MHz and 50MHz with full-scale amplitude is similarly obtained as -65.37dBc.

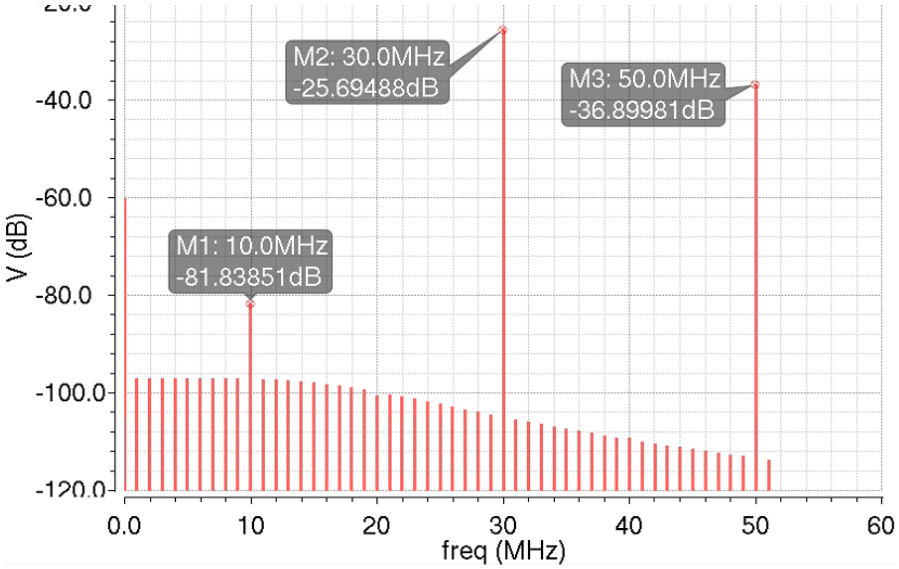



Figure 73 Output spectrum of two-tone test (30MHz and 50MHz)

### 4.2.5 In-band integrated noise

The noise of the filter itself is tested by using ideal current source and removing the output buffer. The total integrated noise at the differential output from 1Hz to 10MHz is shown in Figure 74, which is 20uV.

| Device | Param | Noise Contribution | % Of Total |
|---|---|---|---|
| OPpc3.rmb | rn | 7.95851e-06 | 15.05 |
| OPpc4.rmb | rn | 7.95851e-06 | 15.05 |
| OPpc3.rma | rn | 7.95851e-06 | 15.05 |
| OPpc4.rma | rn | 7.95851e-06 | 15.05 |
| /I8/T74 | fn | 4.85189e-06 | 5.59 |
| /I8/T73 | fn | 4.85189e-06 | 5.59 |
| OPpc3.reb | rn | 4.47961e-06 | 4.77 |
| OPpc4.reb | rn | 4.47961e-06 | 4.77 |
| OPpc3.rea | rn | 4.47961e-06 | 4.77 |
| OPpc4.rea | rn | 4.47961e-06 | 4.77 |

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 2.05165e-05
No input referred noise available
The above noise summary info is for noise data

Figure 74 Integrated noise of filter only from 1Hz to 10MHz

Since the full-scale output is two tones with differential amplitude of $150mV_{pkd}$, the rms value will be 150mV. Therefore, the signal to noise ratio (SNR) is given by

$$20\log(\frac{150mV}{20uV}) = 77.5dB \tag{4.1}$$

Recall that the in-band $IM_3$ is above 70dBc and the signal to noise and distortion ratio (SNDR) is still 70dB, which is limited by linearity. And the dynamic range is analyzed at the filter output, which is illustrated in Figure 75.

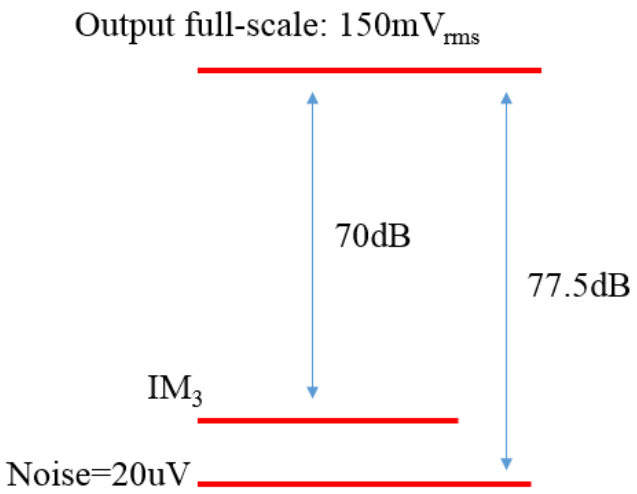



Figure 75 Output dynamic range of the proposed filter

# 5. COMPARISON WITH TOW-THOMAS BIQUAD

## 5.1 Tow-Thomas Biquad

Figure 76 shows the original single-ended Tow-Thomas Biquad proposed by Tow [8] and extended by Thomas [9]. This circuit has one biquadratic band-pass output and one low-pass output whose first-order transfer functions are given by the following.

$$\frac{V_{BP}}{V_i} = \frac{sC_2R_4(R_4/R_1)}{s^2C_1C_2R_2R_4 + \frac{sC_2R_2R_4}{R_3} + 1} \tag{5.1}$$

$$\frac{V_{LP}}{V_i} = \frac{R_4/R_1}{s^2C_1C_2R_2R_4 + \frac{sC_2R_2R_4}{R_3} + 1} \tag{5.2}$$

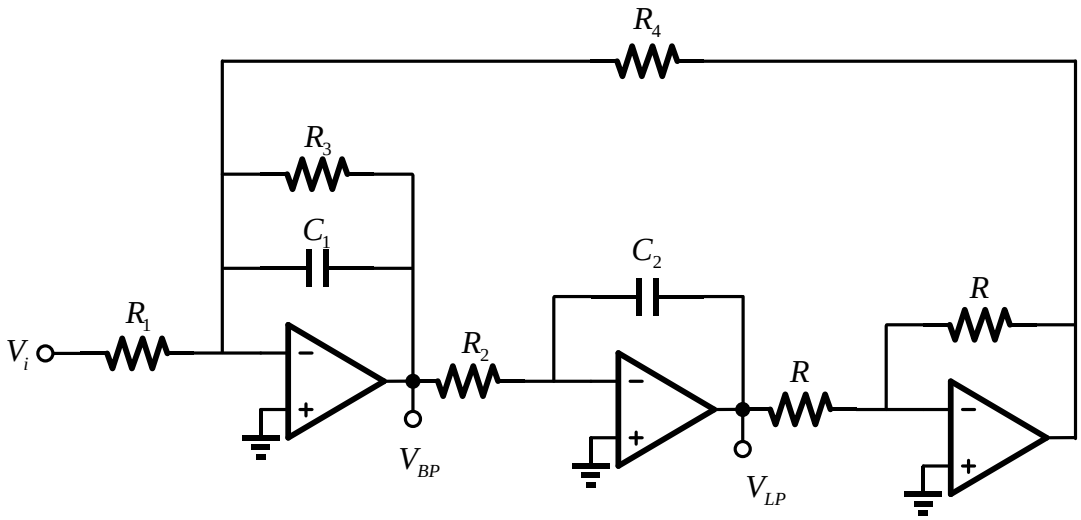



Figure 76 Tow-Thomas Biquad

Since the last stage only provides the gain of -1, the resistor R is not shown in the transfer functions. In addition, we can assume that $C_1$=$C_2$ and $R_2$=$R_4$ for simplicity. Therefore, the natural frequency $\omega_0$, quality factor Q and DC gain $A_0$ are given by

$$\omega_0 = \frac{1}{R_2 C_1} \tag{5.3}$$

$$Q = \frac{R_3}{R_2} \tag{5.4}$$

$$A_0 = \frac{R_4}{R_1} \tag{5.5}$$

Thus, the natural frequency $\omega_0$ and quality factor Q can be independently controlled by $C_1$ and $R_3$ respectively. One of the advantage of Tow-Thomas Biquad is that it can provide certain gain which is determined by the ratio of $R_4$ and $R_1$.

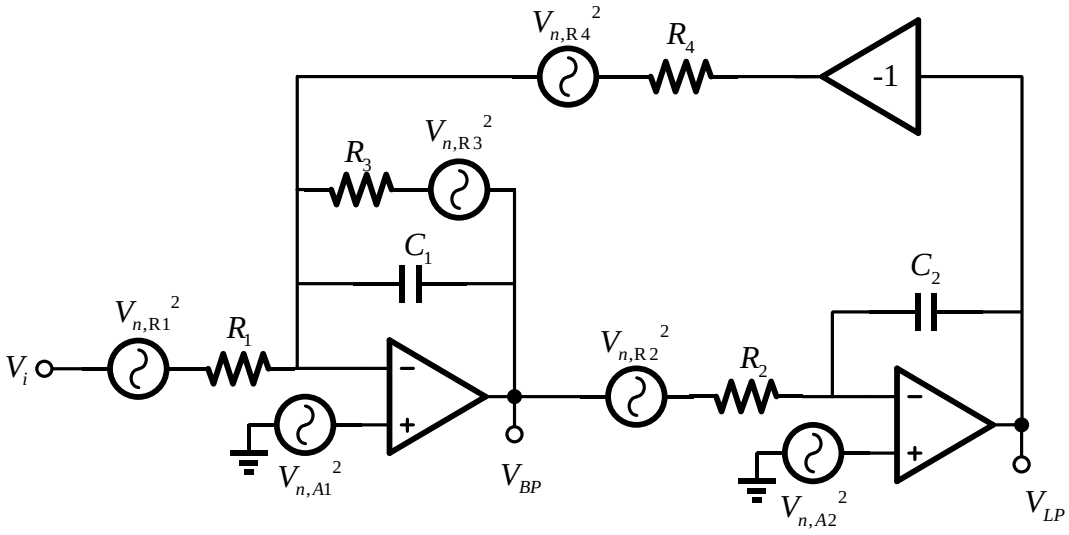



Figure 77 Noise analysis in Tow-Thomas Biquad

Figure 77 shows the noise sources in the Tow-Thomas Biquad. And the input referred noise of the filter is given below [10].

$$V_{in,n}^2 = 4kT\gamma R_1 \left(1 + \frac{R_1}{R_3} + \frac{R_1}{R_4}\right) + 4kT\gamma R_2 |sC_2R_2|^2$$

$$+ (V_{n,A1}^2 + V_{n,A2}^2 |sC_2R_2|^2) \left|\frac{R_1}{R_3} + sC_1R_1\right|^2 \tag{5.6}$$

As shown in equation (5.6), the noise of $R_2$ and $V_{n,A2}$ is negligible at low frequency because of the $|sC_2R_2|^2$ term. On the other hand, the noise of $R_1$ is directly added to the input referred noise of the filter and the noise of $R_3$ and $R_4$ is inversely proportional to their value.

**5.2 Circuits implementation**

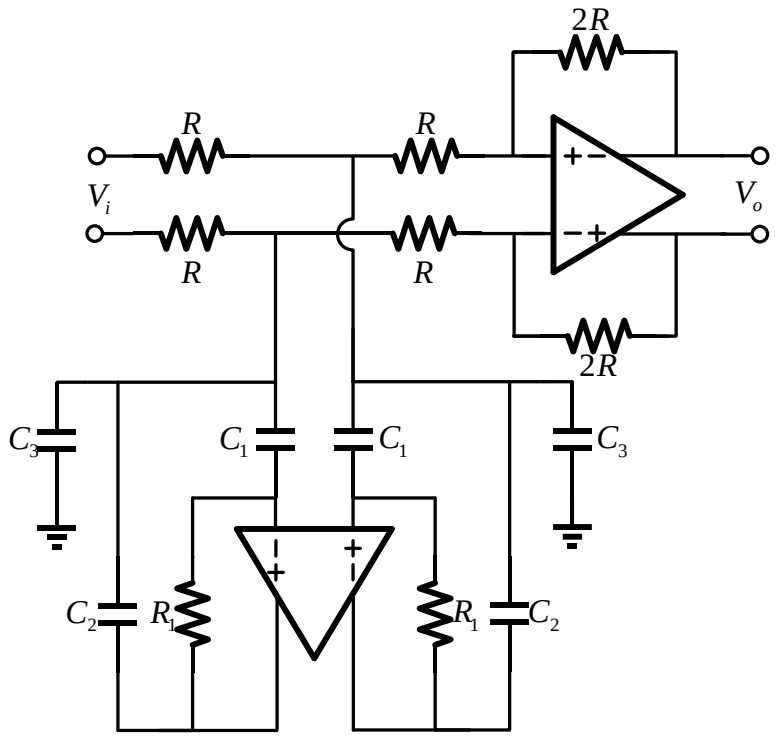



Figure 78 Proposed filter used along with PGA for comparison

In order to make a fair comparison, the proposed filter is used along with the PGA as shown in Figure 78. Since the PGA is already in the receiver frontend, the power consumption that should be considered for comparison is only the part of proposed filter. For the Tow-Thomas Biquad, the last stage in Figure 76 can be eliminated in fully differential implementation shown in Figure 79.

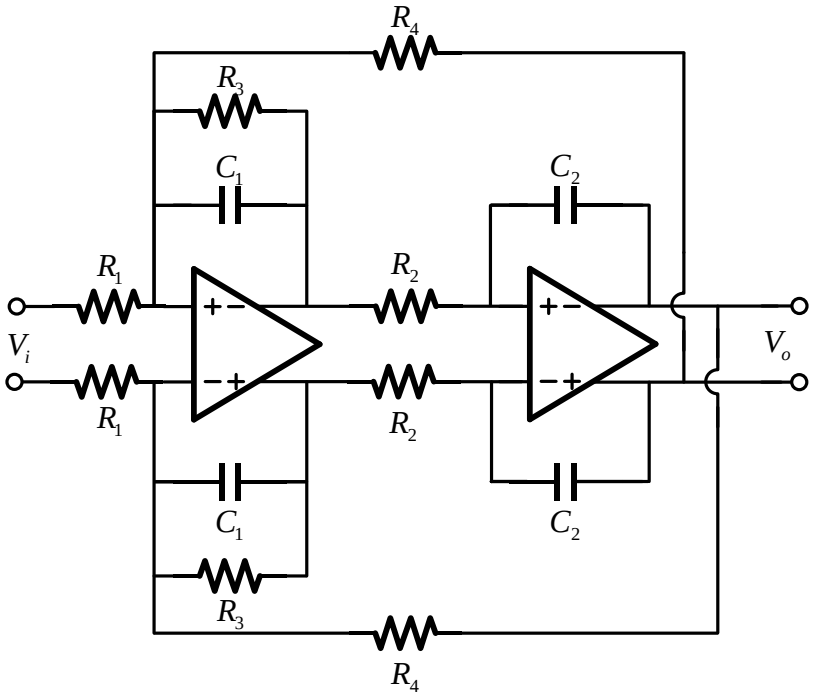



Figure 79 Tow-Thomas Biquad for comparison

Table 8 Target specifications for both cases

| **Specs** | **Value** |
|---|---|
| Cutoff frequency | 10MHz |
| Q | 0.7 |
| Order | 2 |
| DC Gain | 0dB |
| Pass band ripple | <0.5dB |

The transfer function for the two cases are the same for both cases and the filter specs are shown in Table 8. They both have a DC gain of unity and cutoff frequency of

10MHz with Q of 0.7. And the passive component values for Figure 78 and Figure 79 are shown in Table 9 and Table 10 respectively.

Table 9 Component values in Figure 78

| **Component** | **Value** |
|---|---|
| R | 2kΩ |
| $R_1$ | 18kΩ |
| $C_1$,$C_2$ | 2pF |
| $C_3$ | 8pF |

Table 10 Component values in Figure 79

| **Component** | **Value** |
|---|---|
| $R_3$ | 2.8kΩ |
| $R_1$,$R_2$,$R_4$ | 4kΩ |
| $C_1$,$C_2$ | 2pF |

Since the comparison is based on schematic simulation and there is less parasitic capacitance considered, the class-AB OTA in proposed filter is redesigned to reduce the current in the first stage so as to maintain enough phase margin. The detail of the class-AB OTA whose schematic is the same as Figure 38 is listed in Table 11. And we find that the power consumption is reduced to 1mW.

Table 11 Component details of OTA for proposed filter in Figure 78

| Device | Dimensions/Value | Device | Dimensions/Value |
|---|---|---|---|
| M1 | (24) 4.2um/120nm | M4 | (10) 2.2um/120nm |
| M2 | (8) 1um/120nm | M5 | (2) 2.2um/120nm |
| M3 | (8) 1um/120nm | M6 | (6) 1um/120nm |
| $I_{tail1}$ | 500uA | $R_2$ | 100kΩ |
| $I_{tail2}$ | 100uA | $R_3 \| C_2$ | 32kΩ \|\| 60fF |
| $R_1$ | 32kΩ | $C_1$ | 1.5pF |

Table 12 Component details of OTA for PGA in Figure 78

| Device | Dimensions/Value | Device | Dimensions/Value |
|---|---|---|---|
| M1 | (24) 5 um/300nm | M4 | (22) 8um/400nm |
| M2 | (4) 6um/800nm | M5 | (4) 8um/400nm |
| M3 | (8) 6um/800nm | M6 | (4) 1.4um/150nm |
| $I_{tail1}$ | 250uA | $R_1$ | 32 kΩ |
| $I_{tail2}$ | 100uA | $R_2$ | 500Ω |
| $C_1$ | 850fF | $R_3 \| C_2$ | 32kΩ \|\| 60fF |

The OTA used for the PGA in Figure 78 is a typical class-A type and the schematic is the same as Figure 59. The corresponding component detail is shown in Table 12. The total power consumption is also 1mW.

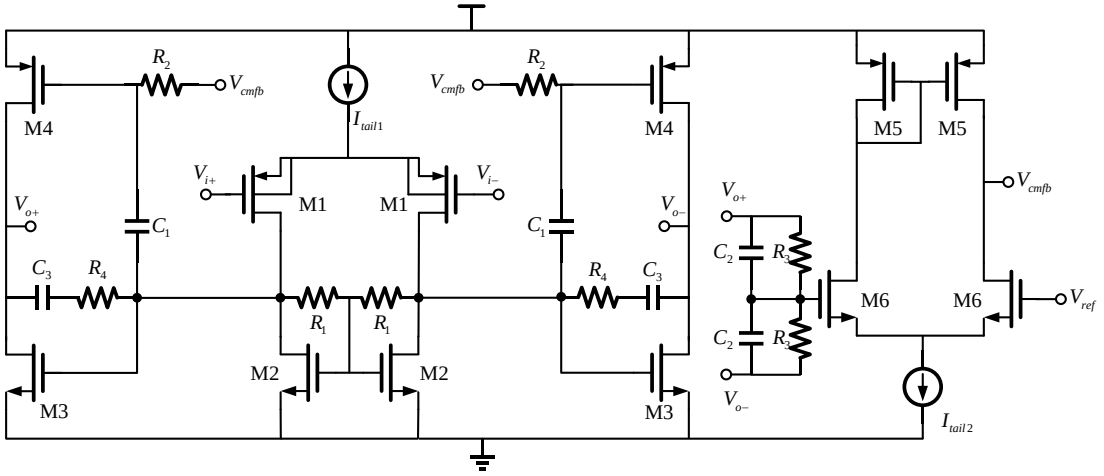



Figure 80 Class-AB OTA with Miller compensation

Table 13 Component details for OTA in Figure 80

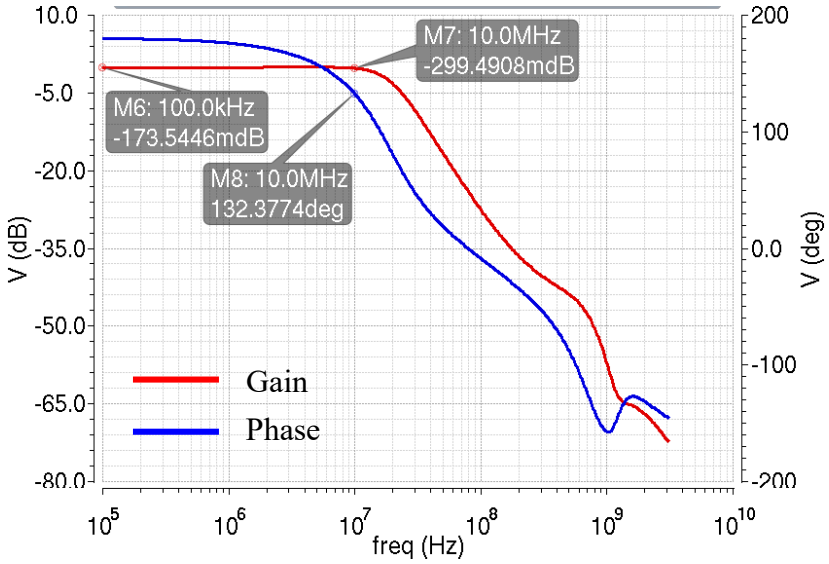
| Device | Dimensions/Value | Device | Dimensions/Value |
|---|---|---|---|
| M1 | (24) 4um/200nm | M4 | (5) 2.2um/120nm |
| M2 | (4) 4um/800nm | M5 | (2) 2.2um/120nm |
| M3 | (6) 4um/800nm | M6 | (6) 1um/120nm |
| $I_{tail1}$ | 190uA | $R_4$ | 400Ω |
| $I_{tail2}$ | 100uA | $R_3 \parallel C_2$ | 32kΩ ‖ 60fF |
| $R_1$ | 32kΩ | $C_1$ | 1.5pF |
| $R_2$ | 100kΩ | $C_3$ | 300fF |

The OTAs used in Tow-Thomas Biquad are identical and have the same topology as the class-AB OTA in the proposed filter. Since the OTAs of Tow-Thomas Biquad are in typical negative feedback configuration, Miller capacitor and nulling

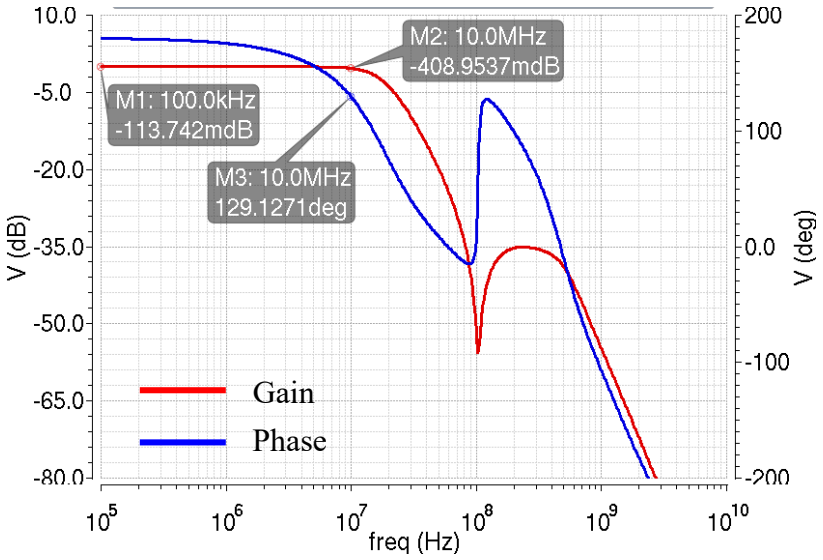
resistor are added for compensation. The schematic of the class-AB OTA in Tow-Thomas Biquad is shown in Figure 80 and the dimensions and values of devices are listed in Table 13. The flicker noise of transistor M1 and M2 in the first OTA contributes a large part of the in-band integrated noise. In order to lower the flicker noise, large channel length is used for these transistors. Each OTAs consumes power of 0.7mW and thus the total power consumption of the Tow-Thomas Biquad is 1.4mW.

**5.3 Simulation results and comparison**

The closed-loop response plots of Tow-Thomas Biquad and proposed filter are shown in Figure 81. Both have a DC gain of 0dB with cutoff frequency of 10MHz. It can be seen that the proposed filter has a notch in the closed-loop response while the Tow-Thomas does not. The notch actually helps to sharpen the roll-off in some extent as long as the frequency of the notch is high enough so as not to degrade the attenuation of filter reponse.

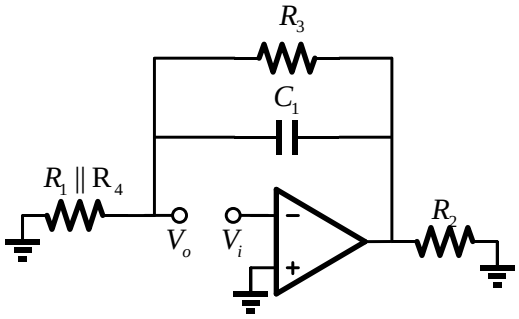


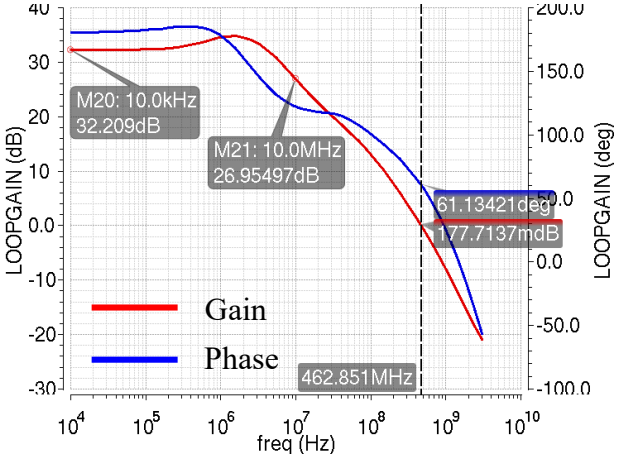

(a)




(b)

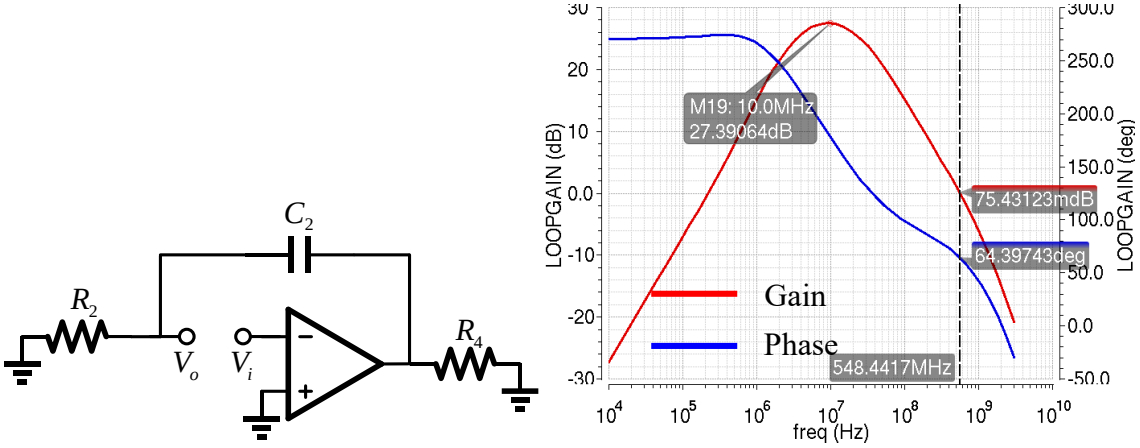
Figure 81 Closed-loop response comparison (a) Tow-Thomas Biquad (b) proposed filter



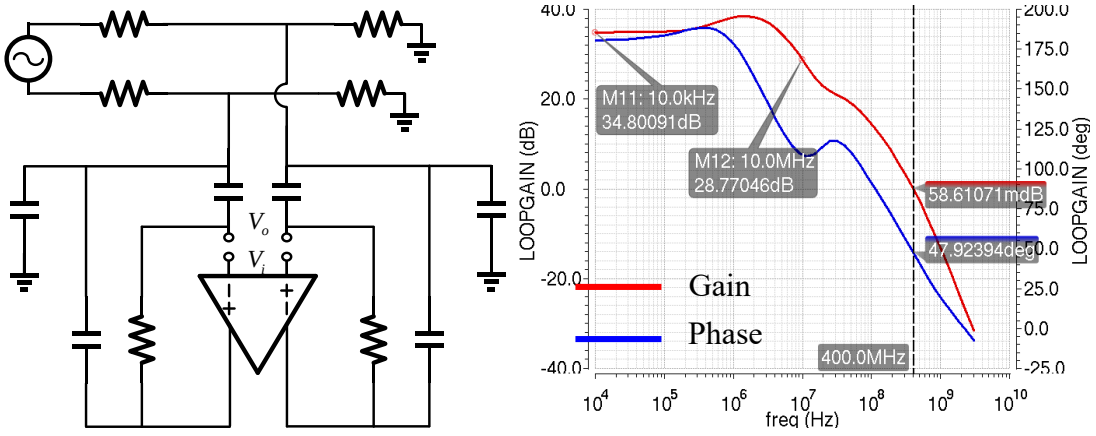

(a) (b)

Figure 82 (a) Open-loop circuit (b) Open-loop AC response of the first amplifier




(a) (b)

Figure 83 (a) Open-loop circuit (b) Open-loop AC response of the second amplifier

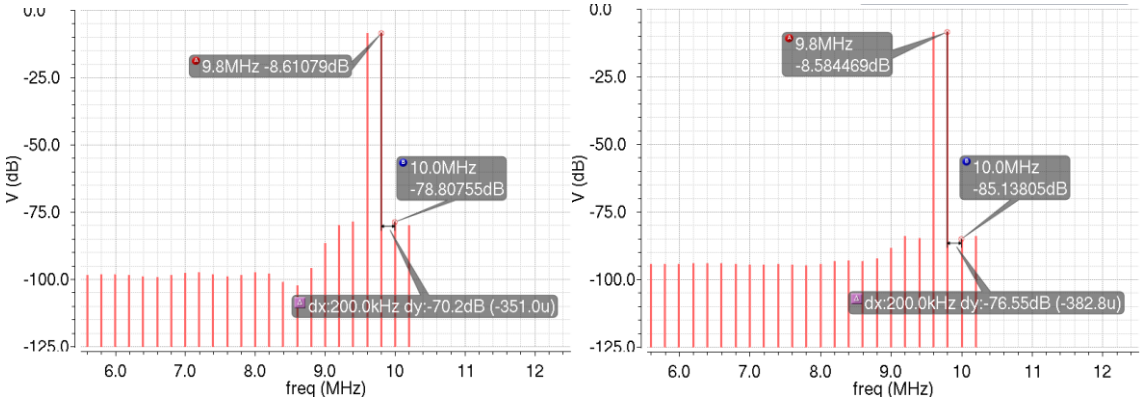



(a) (b)

Figure 84 (a) Open-loop circuit (b) Open-loop AC response of proposed filter

The stability of Tow-Thomas Biquad depends on each local feedback of the two amplifiers. The singled-ended open-loop circuits and simulation results of the open-loop frequency response are shown in Figure 82 and Figure 83 for the first and second amplifier respectively. As mentioned in section 4.2.2, the loop gain of the proposed filter

is shown in Figure 84. All of the loop gain maintains above 26dB before the cutoff frequency 10MHz and have a phase margin greater than 45 degree to guarantee stability.




(a) (b)

Figure 85 Output spectrum comparison (a) Tow-Thomas Biquad (b) proposed filter

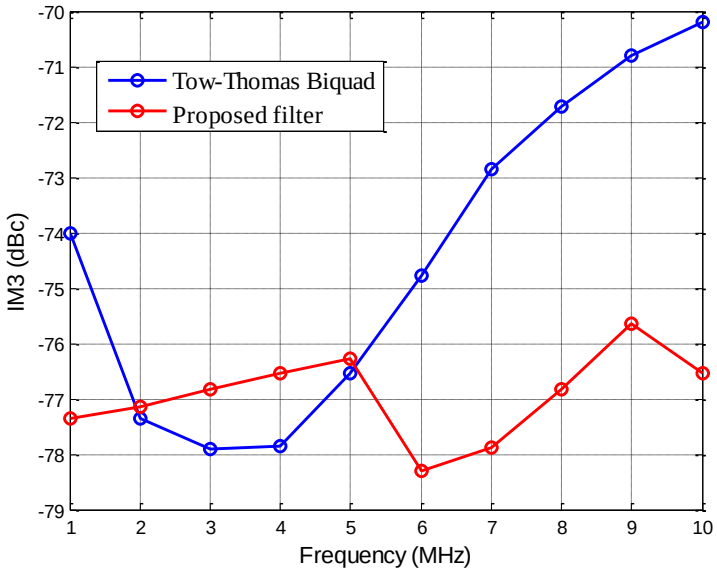
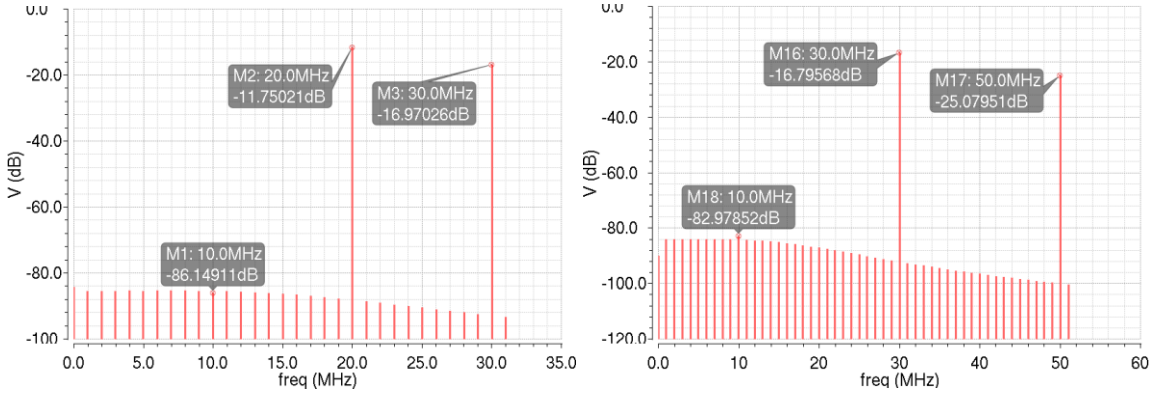



Figure 86 $IM_3$ performance versus frequency comparison

The in-band linearity is examined by two-tone test to find $IM_3$. The full-scale input of the Tow-Thomas Biquad is two differential sinusoidal tones with the same

differential amplitude of 768m$V_{pp}$ at 9.6MHz and 9.8MHz. The differential output spectrum is shown in Figure 58(a), which indicates an $IM_3$ of -70dBc at the edge of filter cutoff frequency 10MHz. The full-scale input of proposed filter is 780 m$V_{pp}$ for both differential tones at 9.6MHz and 9.8MHz and the output spectrum is shown in Figure 58(b). It shows that the $IM_3$ is -76dBc around 10MHz. Figure 86 shows the in-band $IM_3$ performance ranging from 1MHz to 10MHz for the two types of filters. It can be seen that the proposed filter maintains the $IM_3$ below -75dBc compared with -70dBc for the Tow-Thomas Biquad.

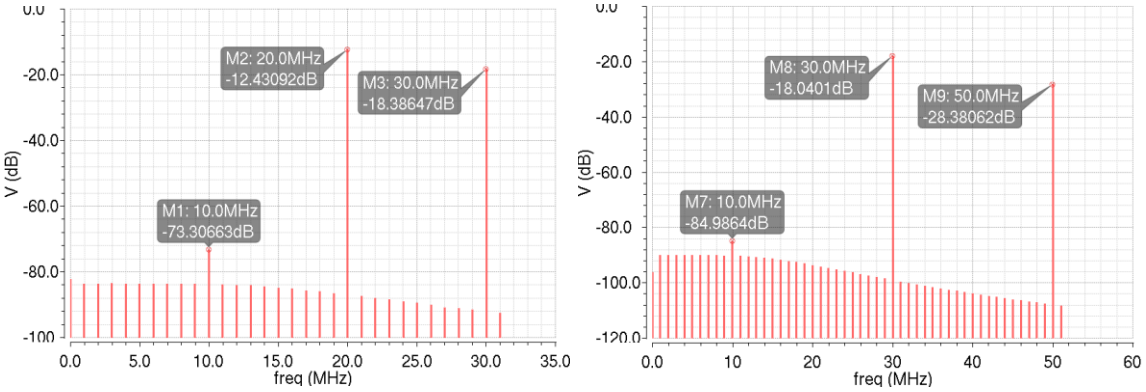



(a) (b)

Figure 87 Output spectrum of Tow-Thomas Biquad. Input tones at (a)20MHz and 30MHz (b)30MHz and 50MHz

Similar to section 4.2.4, the $IM_3$ test for out-of-band linearity also performed with the same full-scale input as the in-band $IM_3$ test and the differential output spectrum for Tow-Thomas Biquad and proposed filter are shown in Figure 87 and Figure 88 respectively. The out-of-band $IM_3$ of Tow-Thomas Biquad is -77.5dBc compared with -64.7dBc of proposed filter when input tones are at 20MHz and 30MHz. For input

tones at 30MHz and 50MHz, the out-of-band $IM_3$ of proposed filter is -76.4dBc and -74.4dBc for Tow-Thomas Biquad.




(a) (b)

Figure 88 Output spectrum of proposed filter. Input tones at (a)20MHz and 30MHz (b)30MHz and 50MHz

| | | | |
|---|---|---|---|
| /R8 | rn | 3.79788e-05 | 10.50 |
| /R2 | rn | 3.79788e-05 | 10.50 |
| /R0 | rn | 3.07912e-05 | 6.90 |
| /R7 | rn | 3.07912e-05 | 6.90 |
| /I8/T87 | fn | 3.07239e-05 | 6.87 |
| /I8/T86 | fn | 3.07239e-05 | 6.87 |
| /I8/T51 | id | 2.72654e-05 | 5.41 |
| /I8/T58 | id | 2.72654e-05 | 5.41 |
| /R9 | rn | 2.54649e-05 | 4.72 |
| /R5 | rn | 2.54649e-05 | 4.72 |

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000117206
Total Input Referred Noise = 0.000119359
The above noise summary info is for noise data

| | | | |
|---|---|---|---|
| /R0 | rn | 2.57639e-05 | 13.28 |
| /R7 | rn | 2.57639e-05 | 13.28 |
| /R4 | rn | 2.16284e-05 | 9.36 |
| /R3 | rn | 2.16284e-05 | 9.36 |
| /R1 | rn | 1.78569e-05 | 6.38 |
| /R6 | rn | 1.78569e-05 | 6.38 |
| /I125/T87 | fn | 1.6356e-05 | 5.35 |
| /I125/T86 | fn | 1.63559e-05 | 5.35 |
| /I125/T3 | id | 1.57516e-05 | 4.96 |
| /I125/T2 | id | 1.57516e-05 | 4.96 |

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 7.06916e-05
Total Input Referred Noise = 7.21938e-05
The above noise summary info is for noise data

(a) (b)

Figure 89 In-band noise comparison (a) Tow-Thomas Biquad (b) proposed filter

As shown in Figure 89, the integrated output referred noise (1Hz to 10MHz) of Tow-Thomas Biquad and proposed filter is 117uV and 71uV respectively. The full-scale differential output of Tow-Thomas Biquad is $370mV_{pkd}$ for each differential tone, which

means there is a 370 $V_{rms}$ signal at output. Similarly, the rms value at the output of proposed filter is 374 $V_{rms}$. Therefore, SNR of Tow-Thmoas biquad is given by

$$20\log(\frac{370\text{mV}}{117\text{uV}}) = 70\,\text{dB} \tag{5.7}$$

And the SNR of proposed filter is

$$20\log(\frac{374\text{mV}}{71\text{uV}}) = 74\,\text{dB} \tag{5.8}$$

Table 14 Comparison between the proposed filter and Tow-Thomas Biquad

| **Specs** | **Proposed Filter** | **Tow-Thomas Biquad** |
|---|---|---|
| DC gain | 0dB | 0dB |
| SNR | 74dB | 70dB |
| In-band $IM_3$ | -75dBc | -70dBc |
| Out-of-band $IM_3$(20MHz,30MHz) | -64.7dBc | -77.5dBc |
| Out-of-band $IM_3$(30MHz,50MHz) | -76.4dBc | -74.4dBc |
| Power consumption | 1.0mW | 1.4mW |
| Estimated area | $0.08mm^2$ | $0.08mm^2$ |

Table 14 shows the comparison summary of proposed filter and Tow-Thomas Biquad. The proposed filter provides a better SNR and in-band linearity. More importantly, we have to pay additional 40% power consumption if using Tow-Thomas Biquad to realize the same transfer function compared with proposed filter. The Tow-Thomas Biquad has better out-of-band linearity close to the cutoff frequency but has

similar performance when the frequency goes high. The total capacitance including the capacitor for the class-AB operation in OTA of the proposed filter and Tow-Thomas Biquad is 27pF and 14pF respectively. Since there are two OTAs with relatively large device size in the Tow-Thomas Biquad, the area should be similar for both cases.

# 6. CONCLUSION

In this work, a novel second order 10MHz low-pass filter topology has been proposed. And the main design considerations such as stability, noise and distortion were analyzed. This novel low-pass filter has an inherent low-noise property and alleviates the direct trade-off between noise and power. Besides, a class-AB OTA was proposed for the novel filter to further improve the power efficiency so that the proposed filter achieves a SNDR of 70dB with only 1.3mW power consumption. In order to test the filter, a highly linear voltage-to-current converter and output buffer were also implemented on chip. The Tow-Thomas Biquad, a common counterpart, has been also designed in same specs to make a fair comparison. It turned out that the proposed novel filter saves 40% power and provides 4dB more SNDR with similar die area compared with Tow-Thomas Biquad. The proposed novel filter is suitable for anti-aliasing filter in receiver frontend and loop filter in continuous-time sigma-delta ADC. The filter implementation was carried out in IBM 130nm process.

# REFERENCES


[1] J. Silva-Mart ínez and E. S ánchez-Sinencio, “Tutorial 1: Design of Continuous-Time Filters From 0.1 Hz to 2.0 GHz,” IEEE ISCAS Vancouver, May 2004

[2] W. Sansen, *Analog design essentials*. New York: Springer, 2006.

[3] R. Schaumann, M. Van Valkenburg and M. Van Valkenburg, *Design of analog filters*. New York: Oxford University Press, 2001.

[4] B. Razavi, *Design of analog CMOS integrated circuits*. New York: McGraw-Hill, 2001.

[5] Y. Tsividis and C. McAndrew, *The MOS transistor*. New York: Oxford University Press, 2012.

[6] T. Carusone, D. Johns, K. Martin and D. Johns, *Analog integrated circuit design*. Hoboken, NJ: John Wiley & Sons, 2012.

[7] L. Krishnan, “High Performance Class-AB Output Stage Operational Amplifier for Continuous-Time Sigma-Delta ADC,” M.S. thesis, Dept. Electr. Comput. Eng., Texas A&M Univ., College Station, TX, 2011.

[8] J. Tow, 'Active RC—A state-space realization', *Proceedings of the IEEE*, vol. 56, no. 6, pp. 1137-1139, 1968.

[9] L. Thomas, 'The Biquad: Part I-Some practical design considerations', *IEEE Trans. Circuit Theory*, vol. 18, no. 3, pp. 350-357, 1971.

[10] V. Gadde, “Filter Design Considerations for High Performance Continuous-Time Low-Pass Sigma-Delta ADC,” M.S. thesis, Dept. Electr. Comput. Eng., Texas A&M Univ., College Station, TX, 2009.