A SINGLE-PHASE RECTIFIER WITH RIPPLE-POWER DECOUPLING AND APPLICATION TO LED LIGHTING

A Thesis

by

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ABSTRACT

In recent years, Light-Emitting-Diode (LED) is widely used in lighting applications for its high efficacy and high reliability. However, the rectifier, which is required by the LEDs to convert the AC power from the grid into DC power, suffers from low-reliability caused by the filtering capacitor. In order to fully utilize the long operational hours of the LEDs, this thesis proposes a rectifier that has improved reliability by adding a ripple-port to eliminate the non-reliable electrolytic capacitor. The ripple-port is capable of decoupling the ripple-power inherited in a single-phase rectifier, which enables using the reliable film capacitor to replace the electrolytic capacitor. To guarantee that the ripple-port can effectively decouple the ripple-power, a closed-loop control scheme is designed and implemented in a digital controller. Simulation and experimental results show that the proposed rectifier can reduce the required capacitance by 70%, which results in a 60% increase in lifetime. The proposed ripple-port circuit can be considered as an add-on module to be integrated into the rectifiers used in applications that require long lifetime. A detailed analysis of the efficiency, cost and reliability of applying the ripple-port in LED lighting applications supports the feasibility of the proposed circuit.

ACKNOWLEDGEMENTS

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CHAPTER I

INTRODUCTION

1.1 Introduction: Need of rectifier in AC/DC power conversion and LED lighting

AC/DC power conversion is required by many industrial applications, home appliances and consumer electronics to take the pulsating power from ac system, e.g. grid, and to supply constant DC power to the load. An AC/DC converter, also referred as a rectifier, is the electrical device to perform AC/DC conversion or rectification, shown as Figure 1. Since the full amount of power is processed by the rectifier, the efficiency and reliability of the rectifier is of great importance.

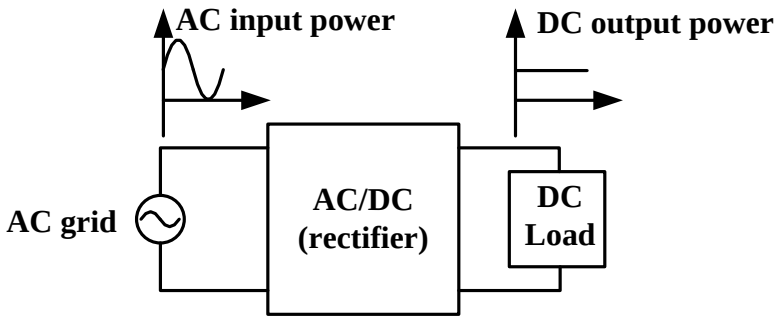
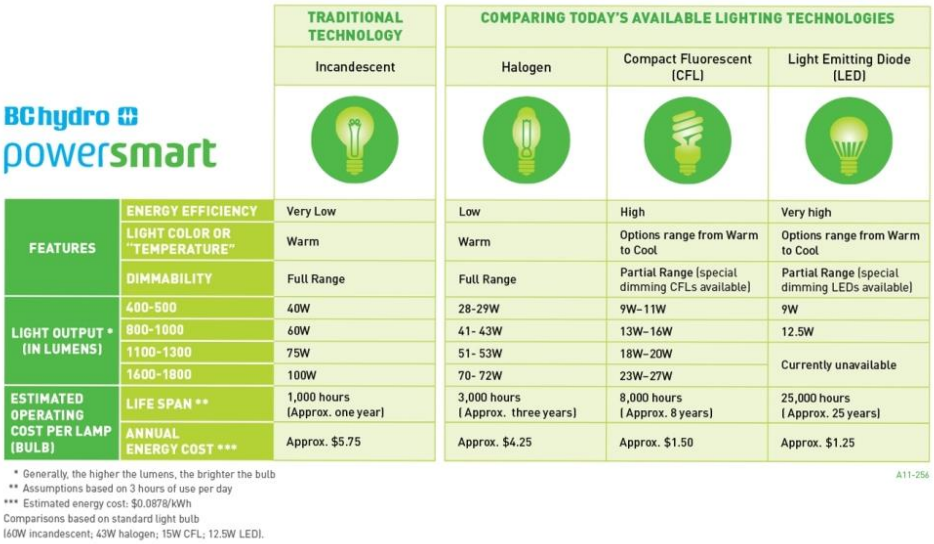


Figure 1 Block diagram of a rectifier

One of the important applications of rectifier is providing power conversion for lighting. In 2012, electricity used for lighting accounts for 17% of the total U.S. electricity consumption [1]. Among the various lighting technologies, the solid-state lighting, i.e. LED, is proven to have superior efficiency and reliability as well as more environmental-

friendly [2]. Figure 2 shows the comparison between the common lighting technologies in terms of energy efficiency and lifetime.



BC hydro powersmart

		TRADITIONAL TECHNOLOGY	COMPARING TODAY'S AVAILABLE LIGHTING TECHNOLOGIES		
		Incandescent	Halogen	Compact Fluorescent (CFL)	Light Emitting Diode (LED)
FEATURES	ENERGY EFFICIENCY	Very Low	Low	High	Very high
	LIGHT COLOR OR "TEMPERATURE"	Warm	Warm	Options range from Warm to Cool	Options range from Warm to Cool
	DIMMABILITY	Full Range	Full Range	Partial Range (special dimming CFLs available)	Partial Range (special dimming LEDs available)
LIGHT OUTPUT * (IN LUMENS)	400-500	40W	28-29W	9W-11W	9W
	800-1000	60W	41-43W	13W-16W	12.5W
	1100-1300	75W	51-53W	18W-20W	Currently unavailable
	1600-1800	100W	70-72W	23W-27W	
ESTIMATED OPERATING COST PER LAMP (BULB)	LIFE SPAN **	1,000 hours (Approx. one year)	3,000 hours (Approx. three years)	8,000 hours (Approx. 8 years)	25,000 hours (Approx. 25 years)
	ANNUAL ENERGY COST ***	Approx. $5.75	Approx. $4.25	Approx. $1.50	Approx. $1.25

* Generally, the higher the lumens, the brighter the bulb
** Assumptions based on 3 hours of use per day
*** Estimated energy cost: $0.0878/kWh
Comparisons based on standard light bulb (60W incandescent; 43W halogen; 15W CFL; 12.5W LED).

A11-256

Figure 2 Comparison between various lighting technologies taken from [3]

With the advance of semiconductor technology in recent years, the amount of LED installed in general lighting applications has been rapidly increased [4, 5]. The revenue growth of the LED market is shown in Figure 3.

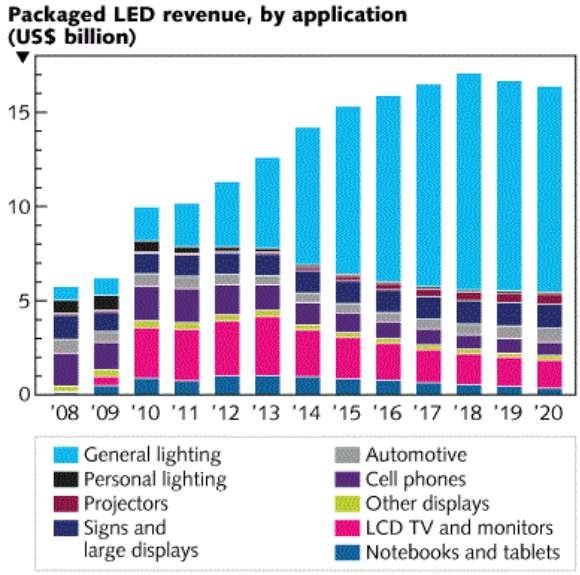


Figure 3 Growth of LED revenue

Source: Status of the LED industry report, August 2012, Yole Development

Unlike conventional incandescent light bulbs, which can be directly connected to AC line, LED requires an AC/DC converter to be driven by the AC main power since it is a DC device. Usually a switching converter is designed as the driver and assembled in the lighting fixture together with LEDs to achieve high efficiency, high power density and high control accuracy [6]. To justify the high manufacturing cost of the LED, the driver circuit, which is a rectifier with some auxiliary circuits, is required to have high efficiency and high reliability to achieve superior performance [7].

1.2 Fundamental challenges

1.2.1. Double-line frequency ripple in single-phase systems

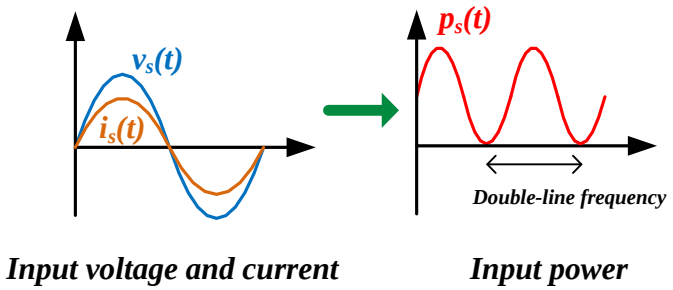


Figure 4 Waveform of input voltage, current and power of a single-phase rectifier

For general lighting applications, LED driver is an ac/dc converter, which is connected to the AC mains. Therefore, high power factor and low total harmonic distortion (THD) of input current are mandatory design requirements [8]. The single-phase PFC (Power Factor Correction) regulator is the most commonly used topology for offline power supplies to meet these requirements [9]. However, the single-phase AC/DC PFC regulator suffers from the inherent double-line frequency power ripple, demonstrated by Figure 4. Since the input voltage $v_s(t)$ and input current $i_s(t)$ are sinusoidal and in phase with each other, the input power $p_s(t)$ is pulsating in a frequency twice as the line frequency, which is referred as the double-line frequency.

Eq.(1) shows that the input power has a constant term, which represents the average power, and a sinusoidal term, which represents the ripple power. Ideally, only the

average power should be delivered to the load while the ripple power should be decoupled by the rectifier.

$$p_s(t) = v_s(t)i_s(t) = V_s \sin(\omega_0 t) I_s \sin(\omega_0 t) = \frac{V_s I_s}{2} - \frac{V_s I_s}{2} \cos(2\omega_0 t) \quad (1)$$

In practical, the rectifier must have an energy storage to make it possible that the output power can remain constant while the input power pulsates. Therefore, the rectifier shown in Figure 1 must be modified to the circuit shown in Figure 5.

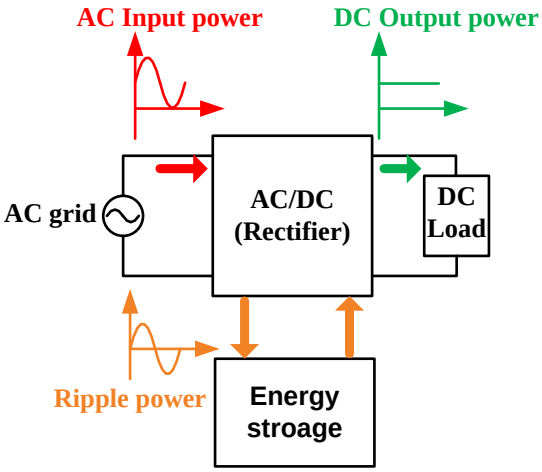


Figure 5 Block diagram of a practical single-phase rectifier

1.2.2. Need of ripple-free current by LED

LED is a current-driven device and thus the luminous of the LED is determined by current following through it. In addition, the LED has a non-resistive characteristic that the current is not a linear function of the voltage. The typical luminous v.s. current curve and V/I characteristic of a LED are shown in Figure 6.

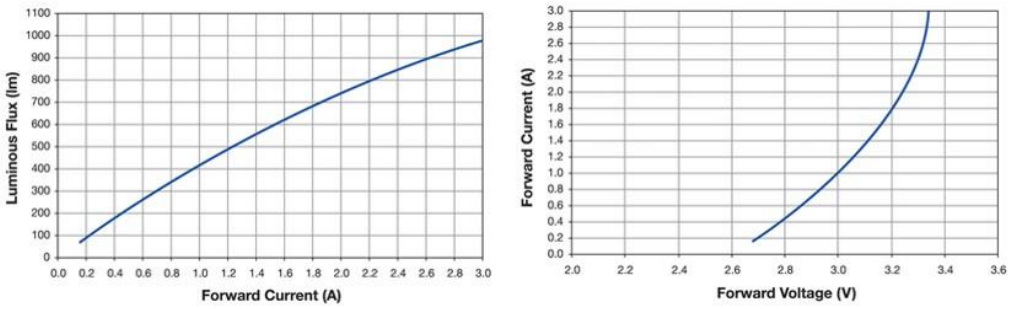


Figure 6 (a) Luminous v.s. Current (b) Voltage v.s. Current characteristic of LED

When using the single-phase rectifier to drive a LED load, the ripple power introduces a certain amount of ripple on both the voltage and current of the LED, which causes the luminous varying. In other words, the LED flickers in the double-line frequency, which can be harmful for human eyes [10, 11].

The most common practice to reduce the flicker is to connect a capacitor in parallel with the LED string to filter the ripple power, shown as Figure 7. The filtering capacitor is referred as the dc-bus connected capacitor as it is connected to the dc output directly.

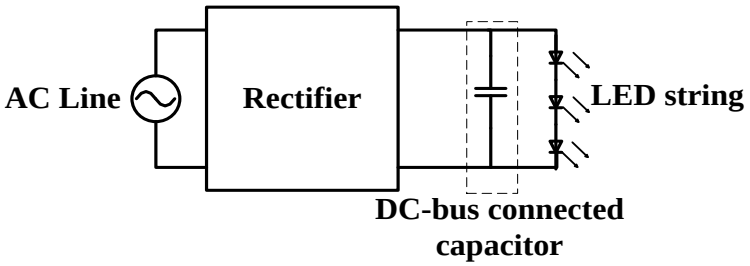


Figure 7 Using dc-bus connected capacitor in LED driver

The characteristic of a capacitor, shown in Eq.(2), shows that the amount of ripple power filtered by the capacitor P_c is related the capacitance C, the average voltage V_{dc}, the line frequency ω_0 and the amplitude of voltage ripple V_{ripple}.

$$C = \frac{P_C}{\omega_0 V_{dc} V_{ripple}} \tag{2}$$

The characteristic of the capacitor indicates that for a finite value of *C*, there will be a certain amount of V_{ripple} across the LED. Unfortunately the V-I characteristic of the LED show in Figure 6 suggests that the voltage ripple leads to a larger amount of current ripple. To avoid visible flickers, LED drivers usually require a very large dc-bus connected capacitor to suppress the voltage ripple.

1.2.3. Reliability of rectifier to match the lifetime expectancy of LED

In practical, the selection of the filtering capacitor needs to include the consideration of size and cost. The comparison between different types of capacitors in [12] suggests that electrolytic capacitor enjoys the advantage of high power density (power/volume) and low cost-per-joule, which makes it very popular for LED drivers in the industry. However, the electrolytic capacitor has very short lifetime compared to the LEDs and other components in the driver, which is a severe reliability problem that limits the lifetime of the LED light bulb. Even worse, as the lifetime of the electrolytic capacitor degrades as the temperature rises, the limitation is exacerbated when the capacitor operates under the high-temperature environment in the lighting fixture because the LED itself dissipates a significant amount of heat.

1.3 Research objective

The objective of this research is to propose a high reliability rectifier design by using an alternative approach to filter the ripple-power. Apparently it is difficult to achieve high reliability with the conventional bus-connected capacitor. Instead of using a dc-bus connected capacitor to directly filter the double-line frequency at the dc-link, a ripple-port circuit can be added to the rectifier to decouple the ripple-power from the input-to-output power path. This approach enables the capacitor having arbitrary voltage swing since it is detached from the load. Consequently the required capacitance can be significantly reduced and high-reliability film capacitor can replace the electrolytic capacitor.

Although the ripple-port concept had been proposed in [13], the control strategy has not been investigated and hardware experimental results are needed to verify the feasibility of this concept. This research is to design a control scheme that the ripple-port can always effectively decouple the ripple-power even when the load has changed. A current-mode control of the ripple-port together with a feed-forward control between the rectifier and ripple-port is proposed and proven to improve the load dynamic response. Also, a 60W hardware prototype of a ripple-port integrated rectifier is built to verify the control scheme and the ripple-port topology. Loss model of the ripple-port is also built to analyze the efficiency and study the tradeoff between efficiency and reliability of the ripple-port configuration.

1.4 Thesis outline

Chapter I gives an overview of the AC/DC converters and the inherent ripple-power problem in the single-phase rectifier. It is stated that the fast growth of solid-state

lighting in recent years introduces the necessity to improve the reliability of the rectifier used in LED drivers. The objective of the research is hence focused on designing a high-reliability rectifier.

Chapter II reviews the previous works on eliminating the electrolytic capacitor in the rectifier design. The ripple-port is introduced and a comparison is drawn against the previous solutions. The design challenges of the ripple-port is also introduced in this section.

Chapter III gives in-depth description of the control objectives of the ripple-port and the control scheme to achieve ripple-power decoupling. Small-signal model is built to study the stability of the proposed control scheme. The controller design is also discretized to enable the implementation in digital controller.

Chapter IV introduces the design example of a ripple-port integrated rectifier. The chapter introduces how to design component values and how to implement the proposed control scheme in a TMS320F28035 digital-signal-processor (DSP). Loss modelling is included to study the efficiency. Simulation and experimental results are included to verify the efficiency analysis and the effectiveness of the ripple-port.

Chapter V investigates the application of the ripple-port to LED lighting.

Chapter VI gives a general conclusion of the work and discusses the future work.

CHAPTER II

REVIEW OF RIPPLE POWER IN AC/DC CONVERTER

2.1 Introduction

All single-phase power systems, including the single-phase rectifier, are characterized by power that flows at twice the fundamental frequency of the voltage and current. Often called double-frequency power ripple, it is inherent and must be filtered within the rectifier system to prevent it from appearing on the rectifier DC output where it would deteriorate the voltage ripple performance of the system. Conventional approaches use large electrolytic capacitors (often referred to as E-caps) at the DC output to filter this 120Hz (100Hz) power ripple. This is such a common practice that datasheets for rectifier-grade E-caps specifically include performance characteristics at 120Hz. The energy-density and cost-per-joule make aluminum electrolytic capacitors very popular. While this technique may be acceptable for some low-cost applications, for applications that require long service life, such as photovoltaic (PV) inverters or LED lighting drivers, it represents a severe reliability problem that limits the lifetime of the power electronics converter [14-19]. This limitation is exacerbated when considering that the capacitors are exposed to uncontrolled and harsh thermal environments when co-located with the PV module in a micro-inverter or the LED chip in a lighting fixture. While derating techniques are well known, this ultimately adds costs as it results in an over-designed system. An alternative is to consider topologies and controls that enable inherently more reliable capacitors, proven to work under harsh and uncontrolled operating conditions, can be used instead of E-caps.

Film capacitors are known to have a long operating lifetime and high reliability due to self-healing properties and no aqueous electrolyte to dry out over time. As such, they are currently the best replacement option available in the market as a high reliability energy storage device [20]. However, they are more expensive compared to electrolytic capacitors on a microfarad basis, thus preventing a cost-effective simple component substitution approach to reliability improvement. A more elegant and fundamental solution is needed.

There are various ways to filter the double-line frequency ripple, the existing solutions can be categorized into three types, which will be introduced in this chapter.

2.2 Review of existing solutions

2.2.1 Passive ripple-power filter

Magnetic energy storage, e.g. an inductor, can be connected in series with the load to filter the double-line frequency ripple. However, the large volume and weight makes this solution unattractive in practical design [21]. DC-bus connected capacitor, shown as Figure 7, is the most popular way to filter the double-line frequency ripple. The required capacitance, however, is much higher than the minimum required capacitance because only a small voltage ripple is allowed due to the direct connection of the capacitor and the DC load [22].

2.2.2 Two-stage cascading architecture

In order to achieve good input current regulation and output voltage regulation at the same time, there are numerous attempts to combine a Power Factor Correction stage and a conventional dc/dc switching converter to form a two-stage architecture [23-30].

The two-stage PFC can achieve very good input current quality, low output ripple and fast dynamic response. Yet the tradeoffs are increased components count and decreased efficiency.

2.2.3 Bus-connected ripple-power filter

Numerous ripple-power filtering techniques using active circuits to decouple the energy-storage component from the dc-link had been proposed to improve the reliability of the single-phase rectifier [31-35]. The energy-storage component can be either a capacitor or an inductor and the former is favored in most proposed circuits because of its higher power density. Figure 8 shows the circuit diagram of an example of dc-bus connected filter.

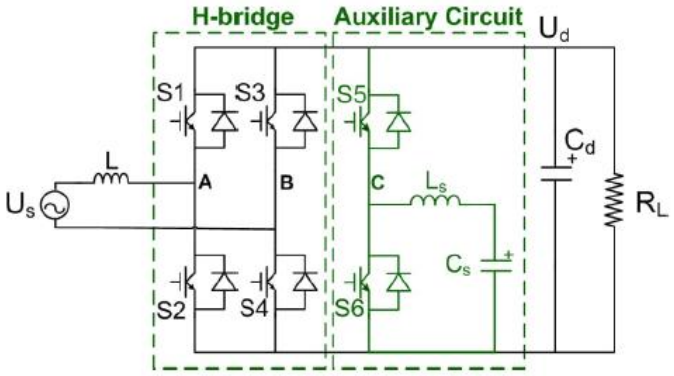


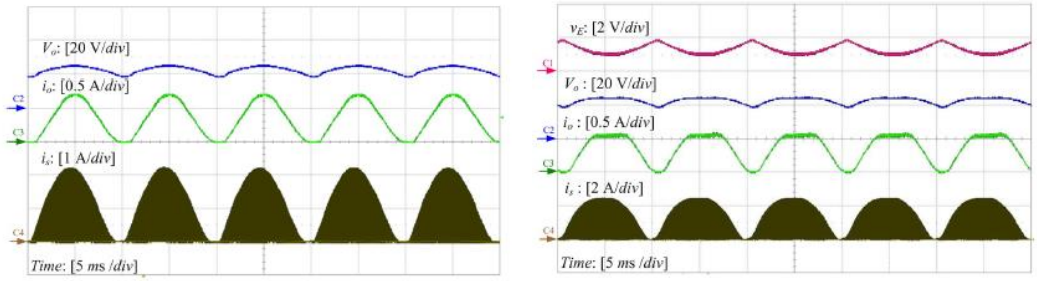
Figure 8 Example of dc-bus connected ripple-power filter taken from [32]

The limitation of dc-bus connected ripple-power filter is the limited voltage swing on the decoupling capacitor and a certain amount of capacitance is still required across the dc-bus. Furthermore, the dc-bus connected ripple-power filter in [32] operates in open-

loop with pre-programed duty ratio, which may enable the ripple-power in the filter drifting from the desired value when the inductor and capacitor has thermal variation. Therefore, a closed-loop control of the ripple-power filter is of great importance.

2.2.4 Input current harmonics injection

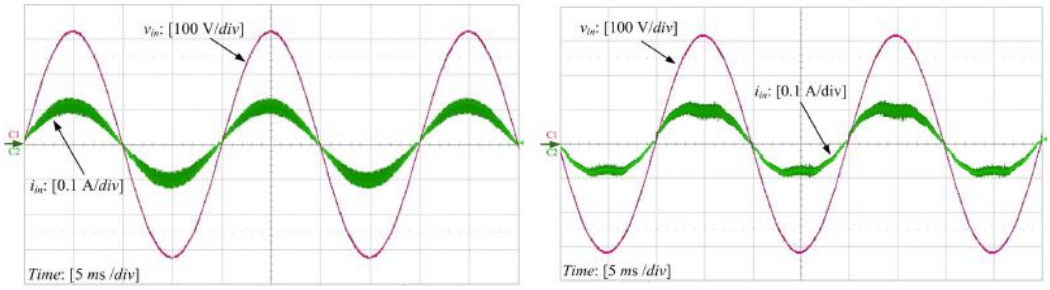
An alternative to circuit-topology modifications is to modify the control scheme of the single-phase rectifier to reduce the amplitude of the double-line frequency ripple. The ripple power is reduced by intentionally distorting the input current and sacrifice the power factor [23, 36, 37]. In [38], the input current harmonics injection had been proposed to reduce the ripple-power at the input of the single-phase rectifier. Figure 9 and Figure 10 the comparison of typical waveforms between a conventional single-phase PWM rectifier and a single-phase PWM rectifier using input current harmonics injection. The harmonics injection reduces the peak-to-average value of the output current without the need for extra circuitries. However, this method leads to direct tradeoffs between input current THD and output current ripple. Therefore, it is difficult to be adopted in applications required both low input current THD and tight output regulation.



(a) **(b)**

Figure 9 Waveforms of output voltage, output current and input current taken from [38]

(a)without harmonics injection (b)with harmonic injection



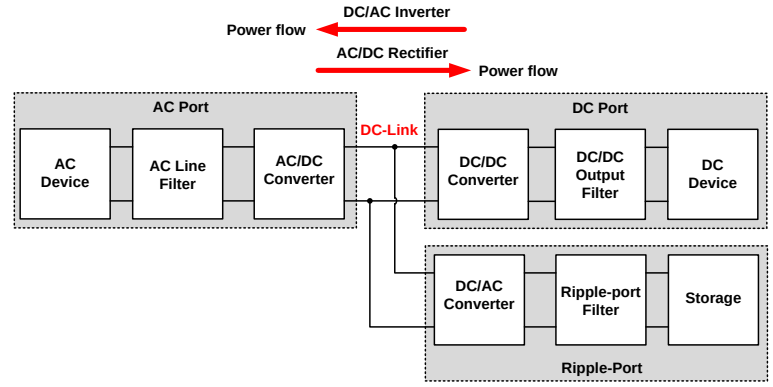
(a) **(b)**

Figure 10 Waveforms of input voltage and averaged input current taken from [38]

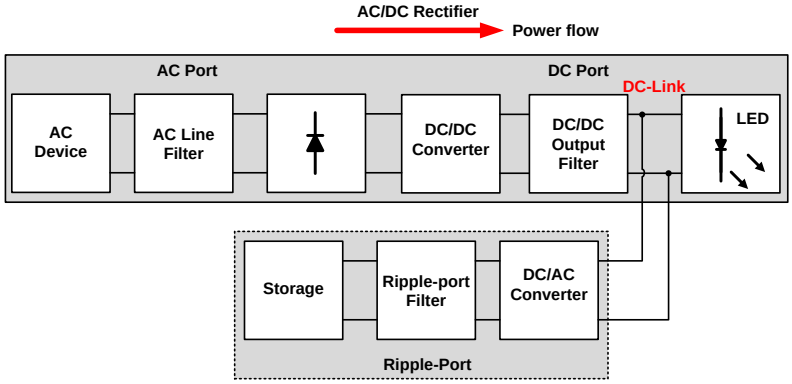
(a)without harmonics injection (b)with harmonic injection

2.3 Ripple-port configuration

In order to achieve minimum required capacitance while preserving unity power factor and low input current THD, ripple-port configuration is proposed in [13]. Without loss of generality, the proposed converter topology is based on the commonly used two-stage converter with a third port added to perform the ripple cancellation. One appreciates, however, that any topology can be used as long as a DC-link exists. Figure 11(a) illustrates the generalized block diagram of the ripple-port concept that can be applied for both DC/AC and AC/DC single-phase power conversion. In the DC/AC inverter applications, a DC power source, for example a PV panel, is used to supply power to a passive AC load or the AC grid. On the other hand, for the AC/DC rectifier applications, an AC power source is used to supply a DC load, for example a battery or an LED lighting system, and the system can be redrawn as in Figure 11 (b).



(a)



(b)

Figure 11 Block diagram of (a) A generalized converter with ripple-port power decoupling (b)LED driver with ripple-port

A generalized block diagram of an AC/DC rectifier system with the ripple-port is shown in Figure 12. It shows that the proposed ripple-port decoupling technique does not depend on the used AC/DC topology as long as the DC-link voltage can be regulated. The AC/DC converter for offline application is often referred as PFC regulator since it provides Power Factor Correction. The commonly used Boost PFC converter will be considered in this paper due to its numerous advantages including, simplicity, low

components count and low conducted electromagnetic interference (EMI) [39, 40], and is well suited for LED lighting applications.

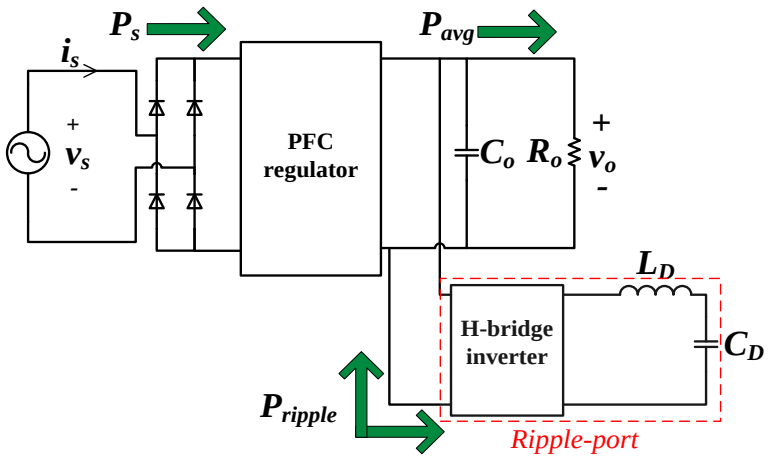


Figure 12 A generalized block diagram of an AC/DC system with the ripple-port

The waveforms of power shown in Figure 13 demonstrates the concepts of ripple-power decoupling. The AC component of the input power, $p_{ripple}(t)$, is processed by the ripple-port and only the average component of the input power is passed to the load. Since the ripple-port utilizes a capacitor, which is decoupled from the dc-link, to store energy, the capacitor allows arbitrary voltage swing and reduce the required capacitance, according to Eq.(2).

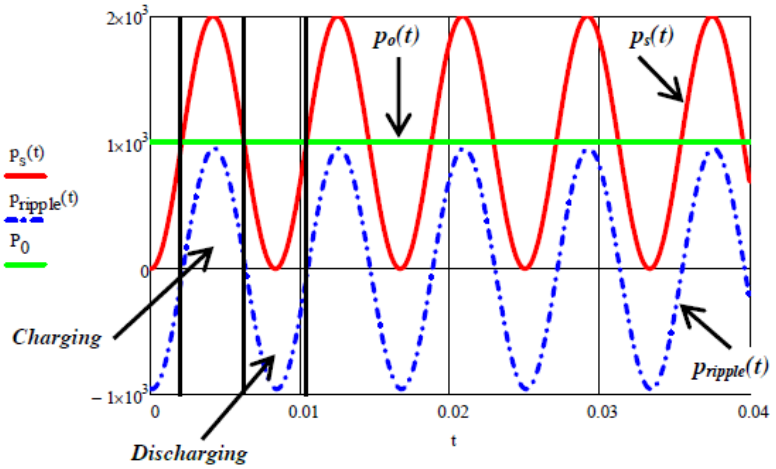


Figure 13 Waveforms of input power, ripple-power and output power of ripple-port integrated rectifier taken from [13].

2.4 Conclusion

The most common solutions for filtering the double-line frequency ripple in single-phase PWM rectifier had been reviewed. While the previous works demonstrate the effectiveness of ripple-power reduction, they bring certain tradeoffs in efficiency, input current THD or reliability. Ripple-port configuration is presented to provide an effective way to filter the double-line frequency ripple using the minimum required capacitance, which enables the replacement of the low-reliability electrolytic capacitor by film capacitor. The analysis and control theory will be presented in the proceeding chapter to understand the ripple-port configuration in depth.

CHAPTER III

ANALYSIS AND CONTROL THEORY OF RIPPLE-PORT

3.1 Introduction

At steady state, in order to have the ripple-port cancelling the double-line frequency ripple in the single-phase PWM rectifier, the power in the ripple-port must be equal to the ripple-component in the input power of the rectifier. The conditions when the ripple-port is able to cancel the double-line frequency ripple has been discussed in [13] and will be re-visited in section 3.2.

The conditions for ripple-power cancellation introduce the need of a closed-loop control scheme for the ripple-port to regulate the current or voltage, in both amplitude and phase, to avoid the power in the ripple-port drifting with the component imperfections, e.g. parasitic resistance, thermal variation.

This chapter proposes a modified Proportional Resonant (PR) controller to control the power in the ripple-port. Comparison between the PR controller and the conventional PI controller will be covered and demonstrates the advantages of the PR controller.

When being integrated into a single-phase PWM rectifier, the ripple-port needs to adjust the phase and amplitude of the reference signal in real-time to compensate the load and line variation in the rectifier. Therefore, a feed-forward control path from the rectifier to the ripple-port with phase-locked-loop is proposed and the improvement of dynamic response will be discussed.

3.2 Conditions for ripple-power cancellation

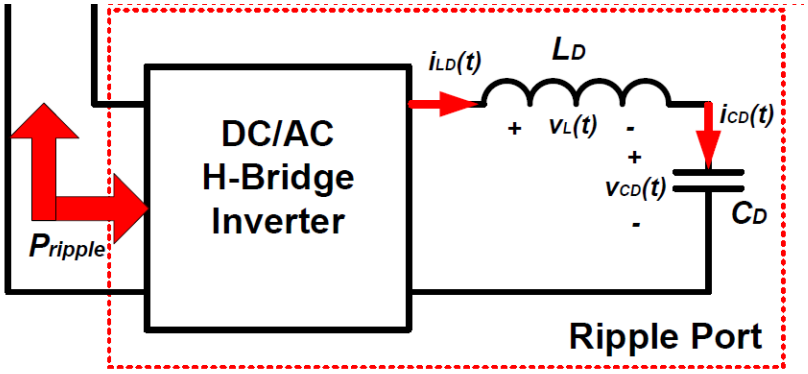


Figure 14 Circuit diagram of the ripple-port taken from [41]

The instantaneous power in the ripple-port can be expressed as the sum of the power in the inductor L_d and the capacitor C_d.

$$p_{rpp}(t) = i_{LD}(t)v_L(t) + i_{CD}(t)v_{CD}(t) \tag{3}$$

According to [41], the instantaneous power in the ripple-port can be re-written in terms of L_d, C_d, the line frequency ω_0 and the amplitude of the voltage across the capacitor V_{CD}.

$$p_{rpp}(t) = \frac{V_{CD}^2 C_d \omega_0 (1 - \omega_0^2 L_d C_d)}{2} \sin(2(\omega_0 t + \phi)) \tag{4}$$

According to Eq. (1), the ripple-power can be written as:

$$p_{ripple}(t) = \frac{V_s I_s}{2}\cos(2\omega_0 t) = P_{o\_avg}\cos(2\omega_0 t) \tag{5}$$

where P_{o_avg} represents the value of average output power.

In order achieve ripple-power cancellation $p_{rpp}(t)$ must be equal to $p_{ripple}(t)$, by equating Eq.(4) with Eq.(5), the following conditions can be obtained:

$$v_{Cd}(t) = \sqrt{\frac{V_s I_s}{\omega_0 C_d (1-\omega_0^2 L_d C_d)}}\sin(\omega_0 t - \phi - \frac{\pi}{2}) \tag{6}$$

$$i_{Ld}(t) = \sqrt{\frac{V_s I_s \omega_0 C_d}{1-\omega_0^2 L_d C_d}}\sin(\omega_0 t - \phi) \tag{7}$$

$$\phi = -\frac{\pi}{4}, or, \phi = \frac{3\pi}{4} \tag{8}$$

3.3 Control objectives

Since the capacitor C_d and inductor L_d are connected in series, the current flowing through the inductor is the same as the current flowing through the capacitor. Therefore, either Eq.(6) or Eq.(7) should be satisfied to meet the conditions for ripple-power cancellation.

Current mode control is inherently more stable than voltage mode control because the dc zero provides sufficient phase margin at the resonant frequency of LC. Therefore, the current mode control is adopted in this research that the inductor current $i_{Ld}(t)$ is regulated according Eq.(7).

Eq.(7) suggests that the regulated inductor current should be sinusoidal with a specific amplitude and phase. The amplitude of the regulated current should be a function of the amplitude of the rectifier input current I_s since C_d, L_d, ω_0 are all fixed variables and the amplitude of line voltage V_s is also assumed to be fixed in steady state. The phase of the regulated current should have a phase shift of ϕ relative to the line voltage. In conclusion, the amplitude and the phase of the inductor current are the two control objectives for the ripple-port.

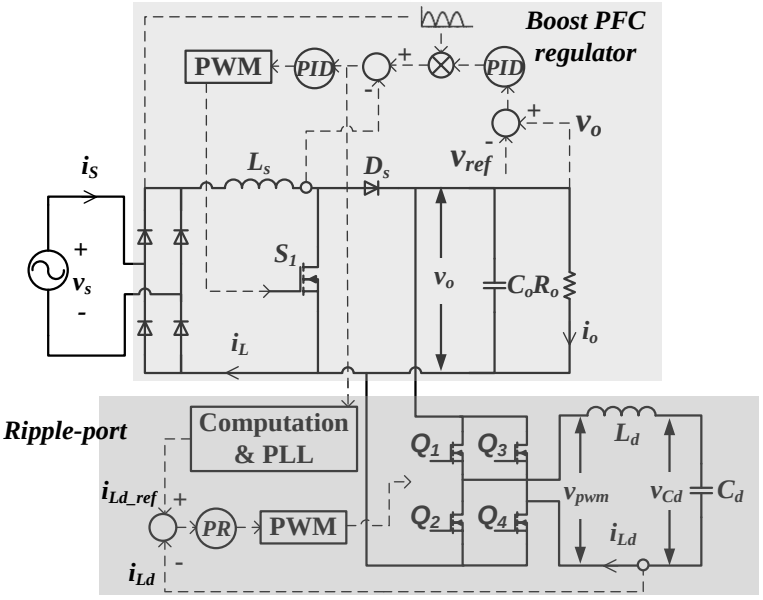


Figure 15 Diagram of the proposed control scheme

Figure 15 shows the control scheme proposed for the ripple-port. The ripple-port has a current feedback control loop that regulates the inductor current $i_{Ld}(t)$ against a reference signal generated from the rectifier stage. Although the diagram includes a boost

PFC regulator, which is a very common circuit topology for single-phase PWM rectifier, for illustration purpose, the proposed control scheme of the ripple-port is independent from the circuit topology of the rectifier. The reference signal for the current loop is generated by the computation & PLL block shown in Figure 15, which takes phase and amplitude information from the rectifier. The error between the reference signal i_{Ld_ref} and the feedback signal i_{Ld} is fed into a PR compensator. The output of the PR compensator is modulated by the PWM module and becomes the gate-drive signals for the H-bridge.

3.4 Ripple-port current loop design and stability analysis

3.4.1 Small-signal modelling

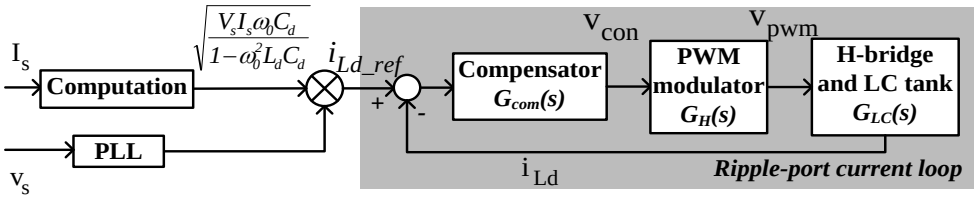


Figure 16 Small-signal model for ripple-port current loop

Figure 16 is the small-signal model of the current control loop introduced in the previous section. The bandwidth of the current loop should be much lower than the switching frequency since the control objective is to regulate the averaged inductor current. With the frequency band of interest being much lower than the switching frequency, i.e. by a decade, the PWM modulator does not contribute dynamic to the current loop and can

be considered to have a constant gain of V_o (dc-link voltage). Therefore, the control-to-output transfer function can be written as:

$$G_{ic}(s) = \frac{i_{Ld}(s)}{v_{con}(s)} = \frac{sC_dV_o}{1+s^2L_dC_d} \tag{9}$$

Figure 17 shows the bode plot of the control-to-output characteristic of the current-loop in the ripple-port. The peak represents the resonance introduced by the LC tank. The phase plot shows that a 90 degree phase shift is formed from dc and a -90 degree phase shift is formed after the resonance.

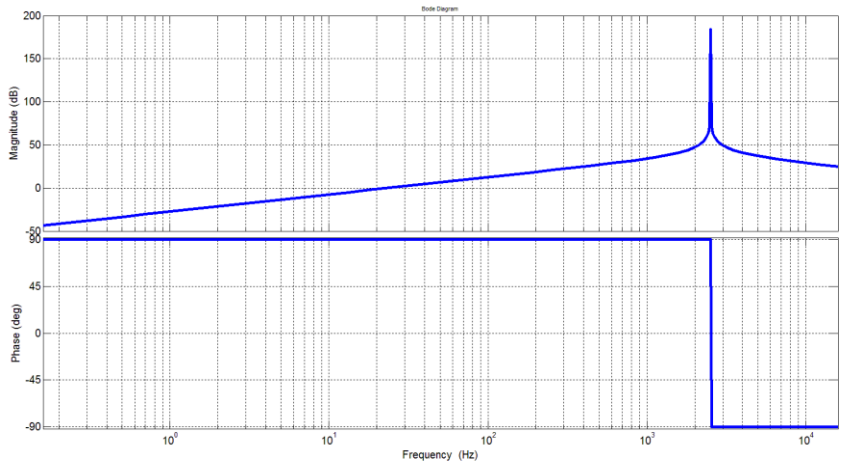


Figure 17 Bode plot of the control-to-output transfer function of Ripple-port

3.4.2 Comparison between PR controller and PI controller

In dc/dc converter design where the reference signal for voltage/current regulation has a constant value, Proportional Integral (PI) compensator is commonly used to achieve

maximum loop gain at dc and hence force the feedback signal to track the constant reference signal tightly [42, 43]. Eq.(10) shows that a PI compensator is a 1st order controller and the dc-pole reflects the its integrating characteristic in the time domain.

$$G_{PI}(s) = K_p + \frac{K_I}{s} \tag{10}$$

For dc/ac converter design, however, PI compensator does not provide the maximum gain at the frequency of the reference signal, which is an AC signal with frequency depends on the applications [44-46]. In alternative, Proportional Resonant (PR) controller gives the freedom of designing the maximum-gain-frequency, which makes it a more attractive candidate for the ripple-port since the reference signal of the current loop is a sinusoidal signal in the line frequency [47-50]. The transfer function of a PR controller can be written as [48]:

$$G_{PR}(s) = K_p + \frac{2K_I\omega_{cut}s}{s^2 + 2\omega_{cut}s + \omega_r^2} \tag{11}$$

It can be shown in Figure 18 that the peak gain frequency of the PR controller occurs at ω_r. ω_{cut} defines the Q factor of the PR controller and determines the bandwidth of the resonance. The phase plot of the PR controller shows that the phase-shift approaches 90 degree as the frequency approaches the resonance and a 180 degree phase-shift is presented at the resonant frequency.

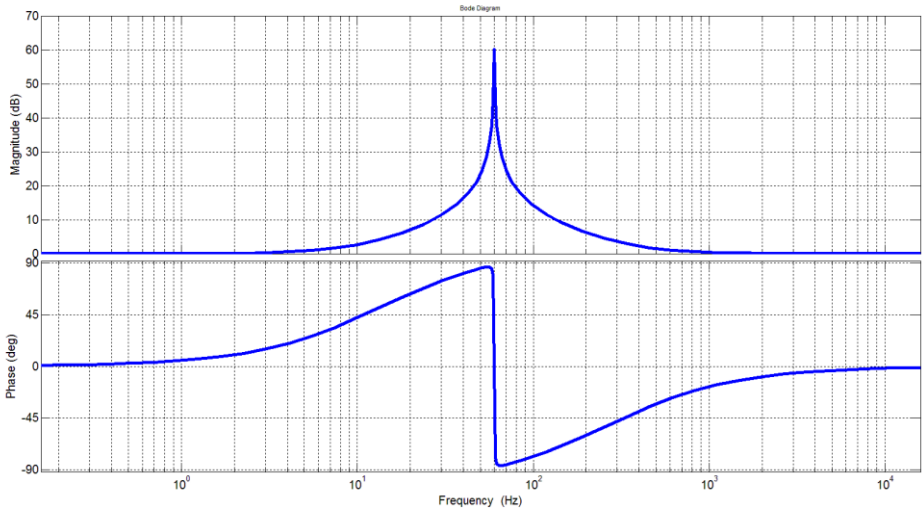


Figure 18 Bode plot of a PR controller

K_p=1, K_i=1000, ω_{cut}=1, ω_r=377;

Recall that in the control-to-output transfer function, a dc zero introduces 90 degree phase shift under resonance of the LC tank, shown as Figure 17, which can cause a 180 degree phase shift near the resonant frequency of the PR controller. This leads to positive feedback and the current-loop is not stable. This problem can be solved by adding a phase-compensating parameter in the PR controller, shown as Eq. (12):

$$G_{PR}(s) = K_p + K_I \frac{2\omega_{cut} s\cos\beta - 2\omega_{cut}\omega_r \sin\beta}{s^2 + 2\omega_{cut} s + \omega_r^2} \tag{12}$$

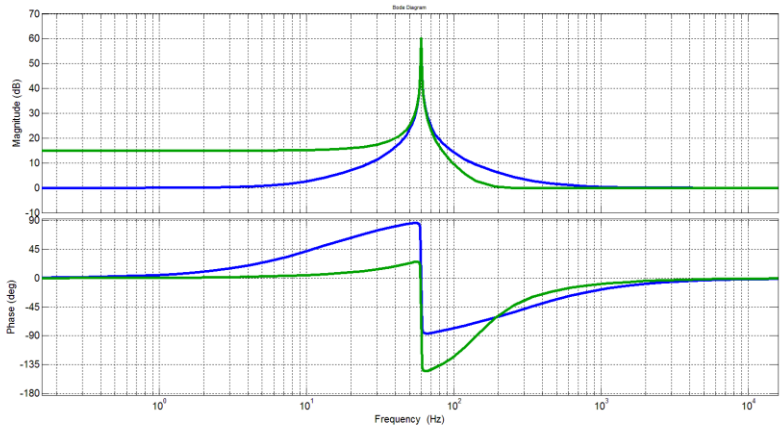


Figure 19 Bode plot of a PR controller with phase compensation

K_P=1, K_I=1000,ω_{cut}=1, ω_r=377, β=0(Blue); β=-π/3(Green)

Figure 19 shows the bode plot of a PR controller with a compensation angle of -60 °. At frequency slightly lower than the resonant frequency, the phase shift is 30 ° and followed by a 180 ° phase shift caused by the resonance.

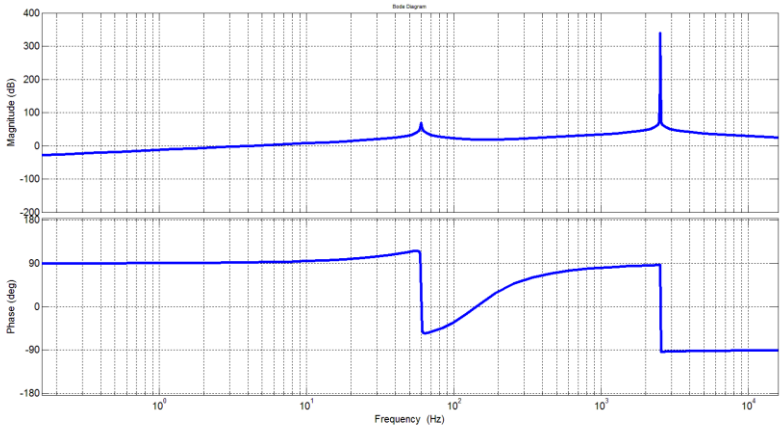


Figure 20 Bode plot of the loop gain of the ripple-port current loop

Figure 20 shows the open loop gain of the ripple-port current loop, ignoring the dynamics of the current-sensing circuit. It is shown that the phase margin is sufficient. The peak gain at high frequency is introduced by the LC tank, which has not included the consideration of parasitic resistance in the inductor and capacitor. In practical, the gain resulted from the LC tank resonance is much smaller due to the damping of the parasitic resistance.

3.5 Integrating the ripple-port to a single-phase rectifier

3.5.1 Feedforward control

Recall that in section 3.2 where the conditions of ripple cancellation was introduced, it had been stated that the inductor current must follow the function shown in Eq.(7), and repeated as following:

$$i_{Ld}(t) = \sqrt{\frac{V_s I_s \omega_0 C_d}{1-\omega_0^2 L_d C_d}} \sin(\omega_0 t - \phi) \tag{13}$$

Is in Eq.(13) represents the amplitude of the input current to the rectifier, which changes under different load power. To ensure the ripple-port drawing the correct amount of power, the amplitude of the reference signal in the ripple-port current loop must be calculated according to I_s. To simplify the illustration, it is assumed that I_s is the only changing variable, while V_s, ω_0, C_d and L_d are all fixed parameters.

The rectifier, which is also a PFC regulator, regulates the dc level of output voltage and shapes the input current waveform. For most PFC regulators, the voltage loop, which is an outer loop adjusts the amplitude of the input current to maintain the output voltage level. Therefore, I_s is in fact the output of the PFC voltage controller.

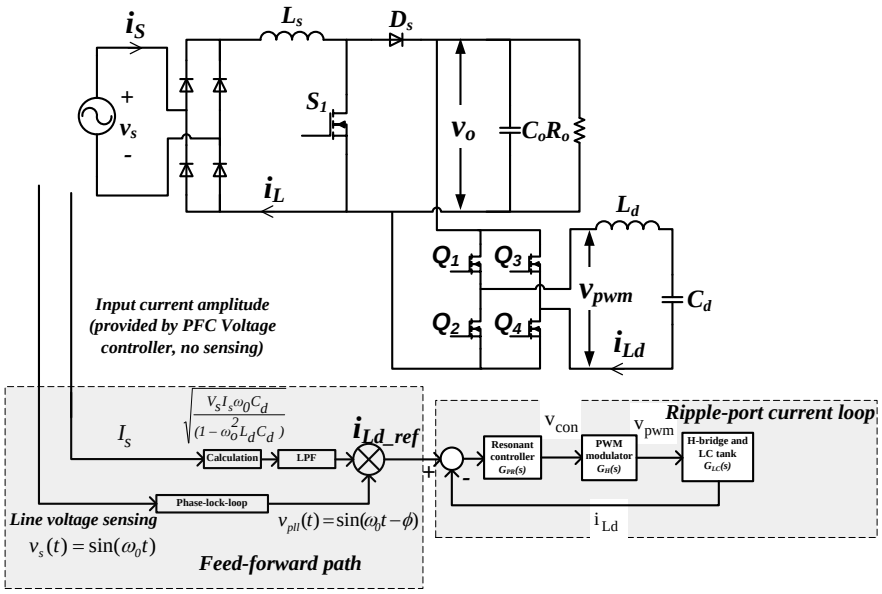


Figure 21 Block diagram of the feedforward control

The feedforward path is highlighted as red in Figure 21. A low-pass-filter is included in the feedforward path to limit the bandwidth in order avoid the high frequency components in I_s distorting the reference signal for the ripple-port. Furthermore, the feedforward path also includes a phase-locked-loop to ensure the angle ϕ is regulated as the value shown in Eq. (8).

3.5.2 Phase-locked-loop

A phase-locked-loop, or PLL, is used to produce a sinusoidal signal which has its phase locked with an input signal. Shown as Figure 21, the PLL produces a sinusoidal output voltage $v_{pll}(t)$ with ϕ phase-shift relative to the line voltage. Then $v_{pll}(t)$ is scaled by the amplitude information derived from the calculation block to generate the reference signal $i_{Ld\_ref}(t)$.

The PLL used for locking the line voltage can be realized according to the block diagram in Figure 22.

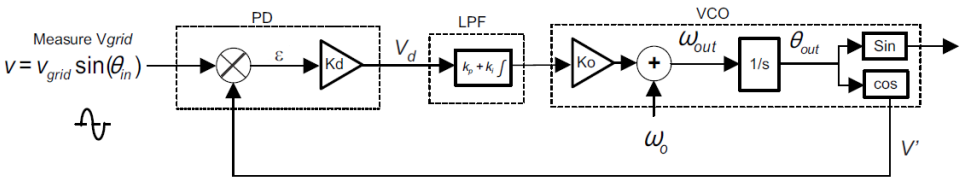


Figure 22 Phase lock loop basic structure, taken from [51]

A PLL consists of a phase detector, a loop filter, and a voltage controlled oscillator (VCO). The phase detector is used to obtain the phase difference between the feedback signal and input signal. Then loop filter provides infinite gain near dc and is realized by a PI controller. The output of the loop filter controls the frequency of the VCO. When analyzing the small-signal model, the VCO can be modeled as an integrator.

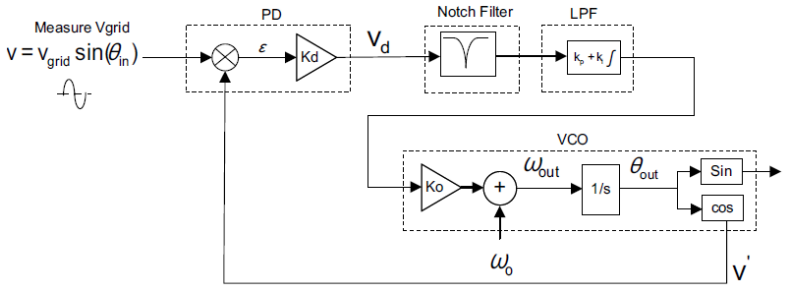


Figure 23 Phase lock loop with notch filter, taken from [51]

There are various ways to implement the phase detector. For grid-connected applications with digital controller, the phase detector can be implemented by a mixer followed by a notch filter [51].

Eq. (13) shows that the multiplication of the sensed grid voltage and the output voltage results in a high-frequency term representing the phase sum and a low-frequency term representing the phase difference. The high-frequency needs to be filtered out in order to extract the phase difference.

$$v_d(t) = \frac{K_d v_{grid}}{2}[\sin((\omega_{grid} - \omega_{pll})t + (\theta_{grid} - \theta_{pll})) + \sin((\omega_{grid} + \omega_{pll})t + (\theta_{grid} + \theta_{pll}))] \quad (14)$$

Since the grid voltage is 60Hz, the frequency separation between the two frequency components in Eq. (13) is as low as 120Hz. Using notch filter other than low-pass filter can provide a sharper attenuation at specific frequency.

$$G_{nf}(s) = \frac{s^2 + 2\xi_2\omega_n s + \omega_n^2}{s^2 + 2\xi_1\omega_n s + \omega_n^2} \quad (15)$$

Eq. (15) shows the transfer function of a notch filter.

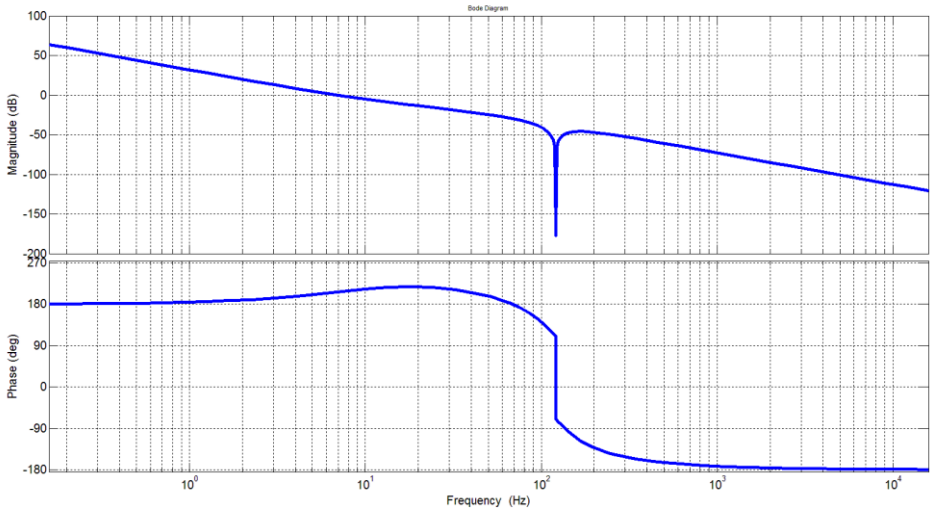


Figure 24 Phase lock loop open-loop gain

The loop gain of the PLL can be written as:

$$G_{lp}(s) = K_{PD} G_{nf}(s) G_{PI}(s) G_{vco}(s) = K_{PD} \frac{s^2 + 2\xi_2 \omega_n s + \omega_n^2}{s^2 + 2\xi_1 \omega_n s + \omega_n^2} \left(K_P + \frac{K_I}{s} \right) \left(\frac{K_{vco}}{s} \right) \tag{16}$$

It is shown in Figure 24 that the phase starts from 180 ° due to the two dc poles resulted from the PI controller and the VCO. The zero in the PI controller leads to the phase increasing to gain certain phase margin. The cross over frequency is determined by the DC gain and the location of the zero in the PI controller. To ensure stability, the crossover frequency must be much lower than the notch because the phase will cross 180 ° at the notch frequency.

3.5.3 Dynamic response analysis

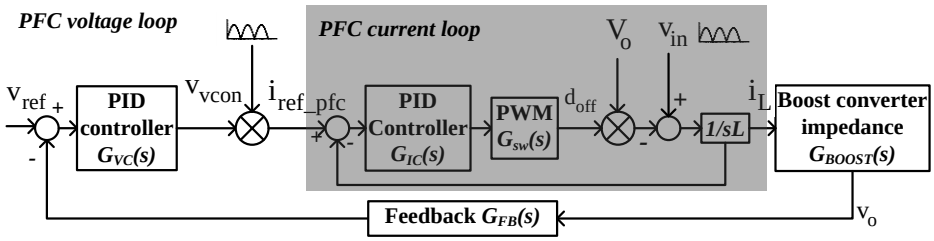


Figure 25 Small-signal model of a Boost PFC regulator

Figure 25 shows that the PFC is controlled by a voltage loop and a current loop. The control signal of the voltage loop v_{vcon} is used to determine the peak of i_{ref_pfc} which is the reference signal for the current loop. The loop gain of the current loop is sufficiently high near the line frequency so that the inductor current i_L is regulated to follow i_{ref_pfc}. Since i_L and i_s have same amplitude, the amplitude of i_s will be the same as the amplitude of i_{ref_pfc}, which is v_{vcon}. Therefore, the input of the calculation block, I_s, in Figure 21 is connected to v_{vcon} in Figure 25.

From the small-signal model, the loop gain of the voltage loop (open loop) can be written as:

$$G_{PFC}(s) = G_{FB}(s)G_{VC}(s)G_{BOOST}(s) = K_{FB}\left(\frac{K_d s^2 + K_p s + K_i}{s}\right)\left(\frac{R_o}{1 + R_o C_o s} K_c\right) \quad (17)$$

K_{FB} is the ratio of the voltage divider used in sensing the output voltage. K_d, K_p, K_i are the parameters of the PID controller of the voltage loop. And K_c is the gain from the v_{vcon} to i_o, which is a constant designed according to the voltage swing of the PID

controller against the maximum operating power. The dynamic of current loop can be neglected in the voltage loop transfer function because the current loop is much faster than the voltage loop [52]. The bode plot of the voltage loop is shown in Figure 26.

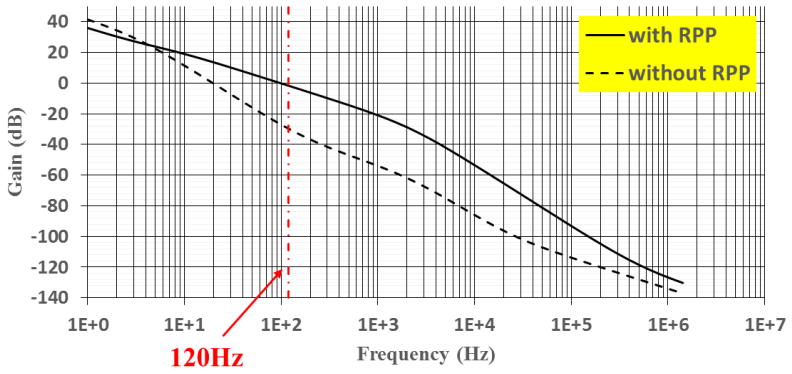


Figure 26 Open-loop gain of the voltage loop: K_{FB}=0.01; K_c=0.42;

Dashed curve: K_d=0; K_i=500; K_p=20; R_o=250; C_o=200 μF;

Solid curve: K_d=0; K_i=100; K_p=0.9; R_o=250; C_o=100 μF;

For conventional PFC regulator, due to the presence of double-line frequency ripple in the output voltage, the gain of the feedback circuit and the controller, i.e. $G_{FB}(s)G_{VC}(S)$, must have sufficient attenuation at the double-line frequency [53-56], i.e. 120Hz, shown as the dashed curve in Figure 26.

According to [57], the the 3rd harmonic in the input current is related to the 120Hz component in vvcon, shown as Eq. (18)

$$\frac{i_{s\_3}}{i_{s\_fundamental}} = \frac{v_{vcon\_120Hz}}{v_{vcon\_dc}} = \frac{V_{ripple} K_{FB} G_{VC}(120Hz)}{V_o /(R_o K_c)} \tag{18}$$

If V_{ripple} is reduced, voltage controller`s gain at 120Hz (G_{vc}(120Hz)) can be proportionally increased. For the proposed PFC rectifier, since V_{ripple} is significantly reduced by ripple decoupling, G_{vc}(120Hz) can have higher gain, shown as the solid curve in Figure 26. The comparison of dynamic response between the two voltage loop designs in Figure 26 is shown in the simulation results in the proceeding chapter.

3.6 Conclusion

The control theory of ripple-port is discussed in this chapter. Current-mode control is adopted to regulate the inductor current. In order to optimize the error-tracking ability of the current loop against a sinusoidal reference signal. The small-signal model of the current control loop has been derived, and it was found that the PR controller needs to have a phase compensation parameter to ensure sufficient phase margin.

To integrate the ripple-port to a single-phase rectifier, a feedforward path and phase-locked-loop needed to be included because the reference signal for the ripple-port must dynamically adjust its amplitude and phase to ensure the ripple-port achieving ripple cancellation.

CHAPTER IV

DESIGN OF A RIPPLE-PORT INTEGRATED RECTIFIER

4.1 Introduction

The chapter introduces the design of a ripple-port integrated rectifier. Since the design of the single-phase rectifier has been presented in many existing literature, this chapter will focus on the controller design, choosing the decoupling capacitor and efficiency analysis.

In recent years, digital control had been widely adapted in controlling power converters for its robustness to PVT variation and high re-configurability [58]. Although in some applications, the digital controller is less preferred than analog controller due to its limited bandwidth, single-phase PWM rectifiers generally do not require aggressive controller speed, which makes digital-signal-processor a very suitable candidate for the controller in the ripple-port. Therefore, while the control theory is discussed in the continuous-time domain in the previous chapter, the implementation of the controller will be discussed in the discontinuous-time domain.

4.2 Selection of the decoupling capacitor

According to [41], the required capacitance for decoupling the double-line frequency ripple can be written as:

$$C_D = \frac{2P_o}{V_{C_D}^2 \omega_o (1 - \omega_o^2 L_D C_D)} \tag{19}$$

Since it is desired that the double-line frequency ripple power being stored in the decoupling capacitor, a small inductor should be used only to limit the current ripple.

Furthermore, the resonant frequency of the LC tank should be much higher than the line frequency to ensure stability, shown as Eq. (20). Consequently, the expression of required capacitance can be written as Eq. (21)

$$\omega_o << \frac{1}{\sqrt{L_D C_D}} \tag{20}$$

$$C_D = \frac{2P_o}{V_{C_D}^2 \omega_o} \tag{21}$$

It can be inferred from Eq. (21) that the required capacitance is inversely proportional to the voltage across the decoupling capacitor C_D. With the output power P_o at 60W, the correlation between required capacitance and capacitor voltage can be plotted.

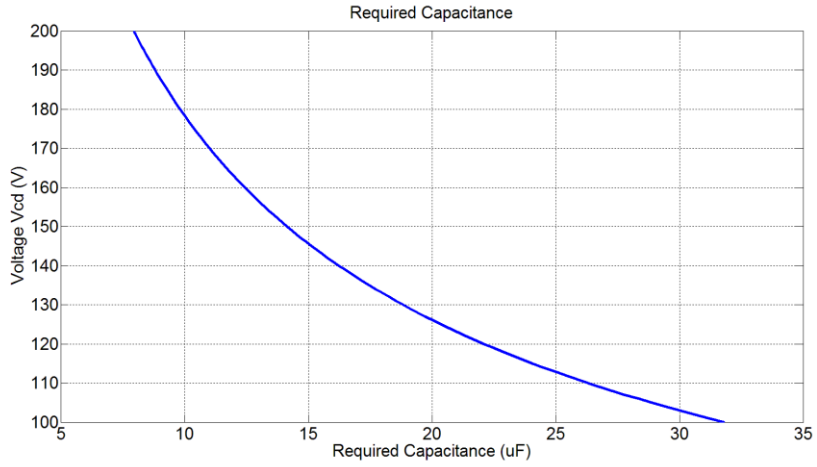


Figure 27 Capacitor voltage v.s. required capacitance

Figure 27 shows that required capacitance increased if the allowed voltage swing is reduced. For the circuit topology proposed in this thesis, the peak voltage across the

decoupling capacitor must be lower than the dc-link voltage because the ripple-port is a voltage source inverter.

Another consideration of choosing the decoupling capacitor is the rms current, which determined the amount of conduction loss on the capacitor. The rms current discussed here is in the line frequency. The magnitude of high-frequency component in the capacitor current is mainly determined by the switching frequency and the inductance L_d, which will be discussed in the section 4.4.

$$I_{C_D\_rms} = \frac{V_{C_D}}{\sqrt{2}C_D\omega_o} \tag{22}$$

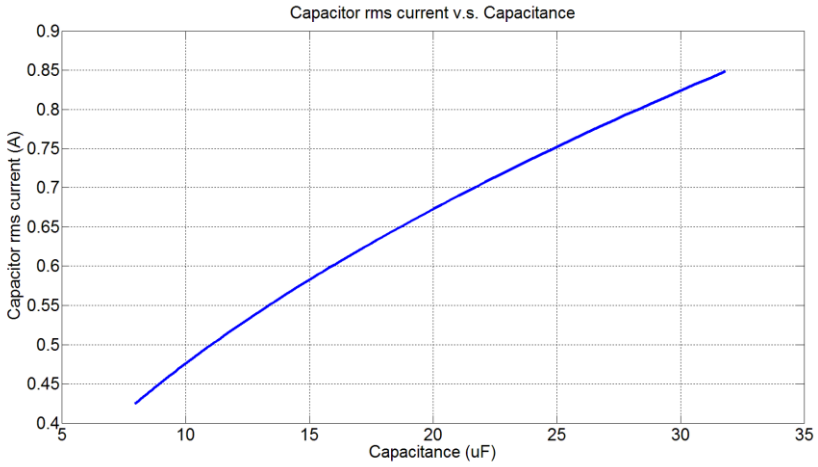


Figure 28 Capacitor RMS current v.s. capacitance

Figure 28 suggests that the RMS current increases with the capacitance. Therefore, designing the capacitor to have voltage swing as large as possible can not only reduce the

capacitor size, but also reduce the RMS current in the line frequency, which is beneficial to the efficiency.

4.3 Digital controller implementation

The controller is implemented in TMS320F28035 microcontroller from Texas Instruments. The specifications of the microcontroller can be found in [59]. The most important function of the microcontroller used in this project is the 2p2z controller which has two poles and two zeros in its transfer function. The discrete transfer function and the difference equation is shown in Eq. (23) and Eq. (24), respectively. Figure 29 shows the block diagram of 2p2z controller, which shows that the 2p2z controller is in fact an Infinite Impulse Response (IIR) filter, since it has its output feedback.

$$\frac{U(z)}{E(z)} = \frac{b_2 z^{-2} + b_1 z^{-1} + b_0}{1 - a_2 z^{-1} - a_2 z^{-2}} \tag{23}$$

$$u(n) = a_1 u(n-1) + a_2 u(n-2) + b_0 e(n) + b_1 e(n-1) + b_2 e(n-2) \tag{24}$$

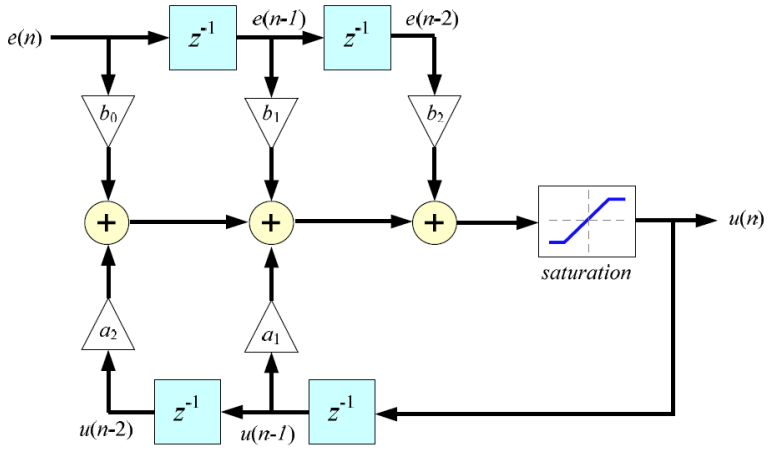


Figure 29 Block diagram of 2p2z controller

Since all the controllers mentioned in the previous sections, including the notch filter, PI controller and PR controller are 2nd order systems. In previous chapters the transfer functions are all in continuous-time domain. Using bilinear transform (also known as Tustin`s method), the continuous-time transfer function can be which can be written in the form of Eq. (23).

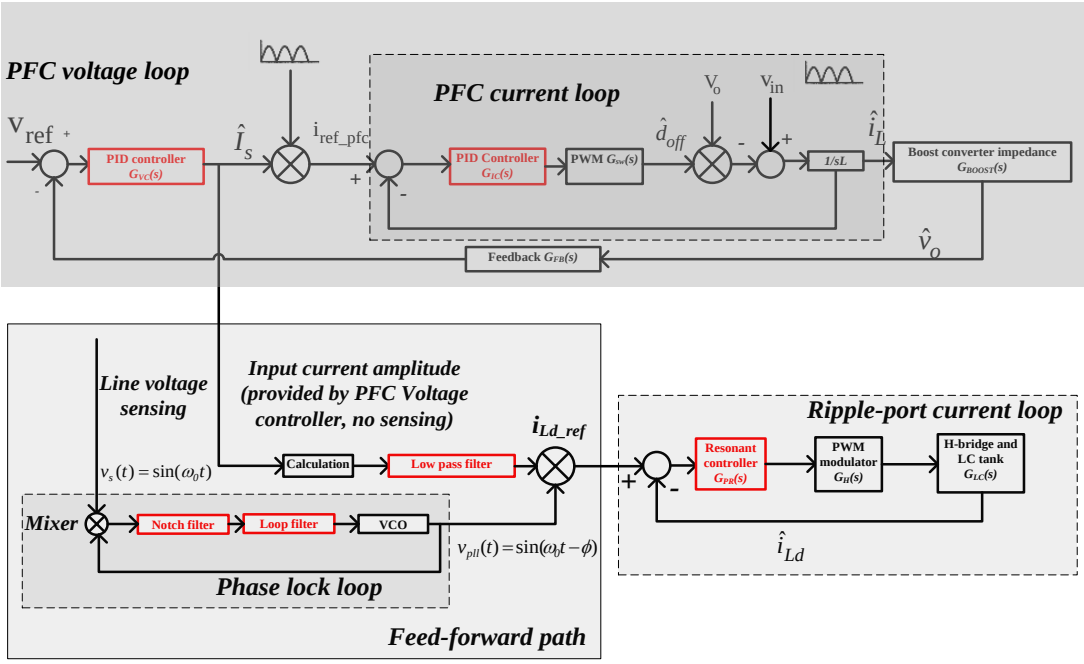


Figure 30 Block diagram of the control loops in a ripple-port integrated rectifier

Discrete-time controller has a sampling frequency which determines how frequency it updates its variables. Selecting high sampling frequency can avoid aliasing, but also implies occupying more cycles of the CPU. Therefore, the sampling frequency should be selected according to the bandwidth requirement. For example, the bandwidth

of the voltage loop in the PFC stage is around a few hundred hertz, hence a sampling frequency of a few kHz will be sufficient for the voltage controller.

Figure 30 shows the block diagram of the control loops with the 2nd order controllers highlighted as red. The following sections will discuss the discretization of these 2nd order controllers.

4.3.1 Voltage and current controllers: 2nd order PR and PID controller

The PFC stage has a dual-loop control: a fast current loop as the inner loop and a slow voltage loop as the outer loop. PID controllers are used for both loops. Averaged current mode control is adopted in this design, which had been discussed in many literatures [60, 61] and hence will not be repeated here. Using bilinear transform, the continuous time transfer function discussed in the previous sections can be implemented by digital controller [62-64].

Table 1 PFC controllers in continuous and discrete form

	Voltage controller	Current controller
Continuous	$H_{s\_PFC\_V}(s)=\frac{3s+1950}{s}$	$H_{s\_PFC\_I}(s)=\frac{0.25s+1.38\times10^4}{s}$
Discrete	$H_{z\_PFC\_V}(z)=\frac{-2.981z^{-1}+3.019}{1-z^{-1}}$	$H_{z\_PFC\_I}(z)=\frac{-0.1812z^{-1}+0.3187}{1-z^{-1}}$
Sampling frequency	50kHz	100kHz

Table 1 shows the controller design of the PFC stage. At nominal operating point, the current loop has the zero-crossing frequency at around 50kHz, which is around a

quarter of the switching frequency, with a phase margin of 90°. The voltage loop has the zero-crossing frequency around 100Hz, with a phase margin of 70°.

4.3.2 Type-2 2nd order PLL

Table 2 PLL controllers in continuous and discrete form

	Notch Filter	Loop filter
Continuous	$H_{s\_Notch}(s)=\frac{s^2+5.11\times10^{-13}s+5.77\times10^5}{s^2+547.6s+5.77\times10^5}$	$H_{s\_LP}(s)=\frac{1.739\times10^{-6}s^2+90s+5441}{s^2+350.7s-668.8}$
Discrete	$H_{z\_Notch}(z)=\frac{-0.9033-1.725z^{-1}+0.9033z^{-2}}{1-1.725z^{-1}+0.8066z^{-2}}$	$H_{z\_LP}(z)=\frac{0.01703+4\times10^{-4}z^{-1}-0.017z^{-2}}{1-1.869z^{-1}+0.8689z^{-2}}$
Sampling frequency	2.5kHz	2.5kHz

The notch filter shown in Table 2 has the notch at 120Hz in order to extract the low frequency component of the mixer output, which is the phase error between the reference signal and feedback signal.

4.3.3 PR controller

Table 3 PR controllers in continuous and discrete form

	PR Controller
Continuous	$H_{s\_PR}(s)=\frac{s^2+1002s+7.951\times10^5}{s^2+2s+142129}$ K_P=1, K_I=1000,ω_{cut}=1, ω_r=377, β=-π/3
Discrete	$H_{z\_PR}(z)=\frac{5.594+11.19z^{-1}+5.594z^{-2}}{1+2z^{-1}+z^{-2}}$
Sampling frequency	100kHz

Table 3 shows the discrete time implementation of the PR controller and the design parameters referred in Eq. (12) are shown in the table.

4.4 Efficiency analysis of the ripple-port

The ripple-port is implemented by an H-bridge followed by an LC tank, which is used to store power when the instantaneous input power is lower than the average input power and supply power when then instantaneous input power is higher than the average input power.

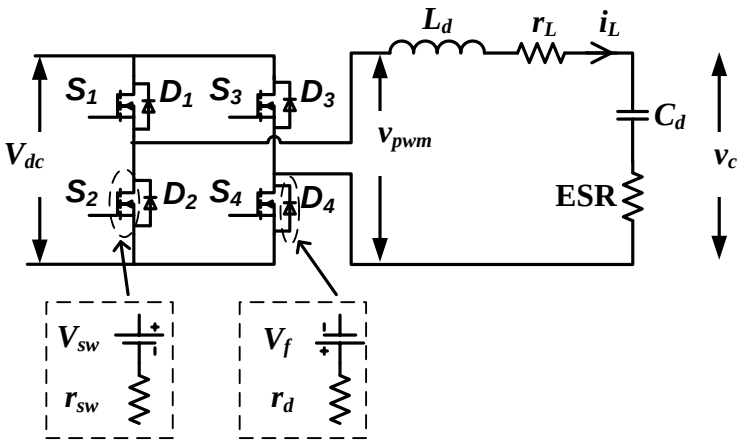


Figure 31 Circuit model of the Ripple-port for loss analysis

Figure 31 shows the circuit model used for loss analysis. Without loss of generosity the switch is modeled as a voltage source in series with a resistor. For MOSFET switch, V_{sw} is very small while the r_{sw} dominates the voltage drop across the switch; for IGBT switch, r_{sw} is small and V_{sw} dominates the voltage drop across switch.

The inductor is modeled as an ideal inductor in series with a resistor which represents the winding resistance. The capacitor is modeled as an ideal capacitor in series with a resistor which represents the capacitor ESR.

Since capacitors has higher power density than inductor, the ripple-port utilize the capacitor to store ripple energy while the inductor is solely to filter the switching current. Therefore, small inductor should be chosen to reduce the volume of the ripple-port, which results in large inductor current ripple caused by the switching.

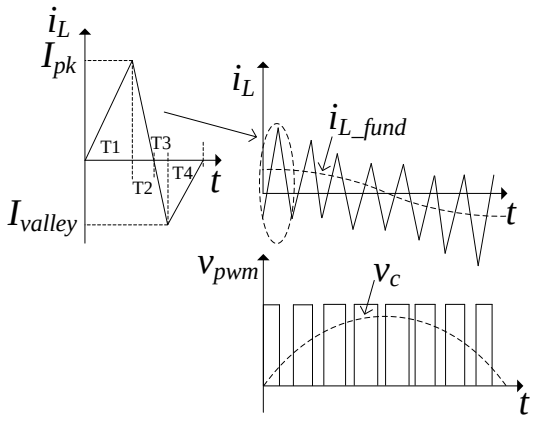


Figure 32 Current and voltage waveform of the ripple-port

Figure 32 shows the typical inductor current waveform in the ripple-port, which utilizes unipolar SPWM control. The waveform shows half of the period in line frequency because the other half is exactly in terms of power loss. In each switching period, the inductor current increases to its peak value and then decreases to negative values. The average value of the inductor current, denoted by i_{L_fund}, is regulated by the current loop and is sinusoidal in the line frequency. Allowing the large inductor current ripple implies high RMS current, which increases conduction loss. Yet it also bring the advantage of zero-voltage turn-ON.

Table 4 Conducting devices in different periods within a switching cycle

Period	Conducting devices
T1	S1, S4
T2	D2, S4
T3	S2, D4
T4	D1, D4

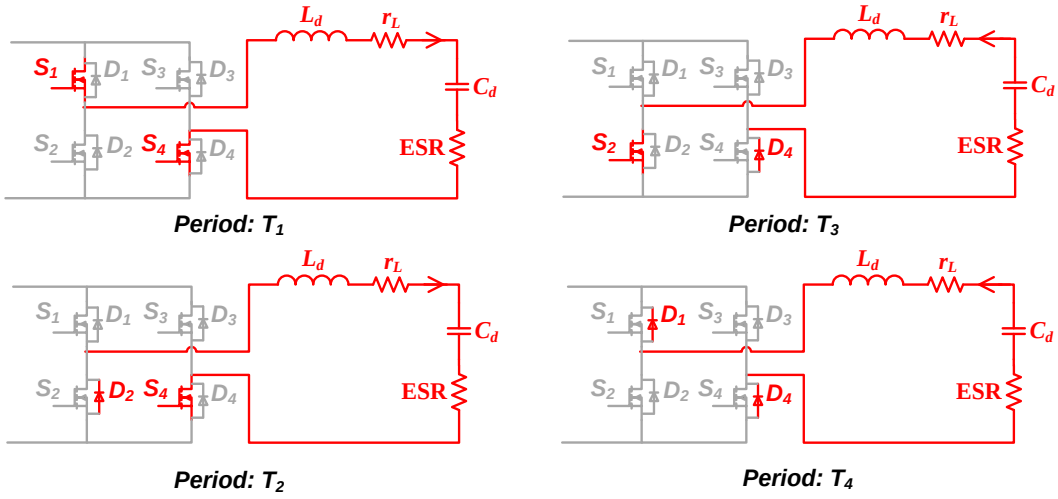


Figure 33 circuit diagram of conducting devices

Switching loss calculation

Table 4 shows the conducting devices in different period within a switching cycle and Figure 33 graphically shows the conducting devices and current flow. At the transition from T4 to T1 and from T2 to T3, the body diode conducts prior to the commutation of the switch, which enables the switches to turn ON at zero drain-to-source voltage. At the transition from T1 to T2, S1 turns off at hard-switching; at the transition from T3 to T4, S2 turns off at hard-switching. Assuming the turn-ON loss can be negligible due to zero-voltage switching, the switching loss in a switching period can be calculated as the sum of turn-off loss of S1 and S2. The turn-off loss of the IGBT can be calculated according to the V_{ce} and I_{ce} by the following equation, assuming the IGBT is operating in room temperature:

$$E_{off} = E_{offref}(\frac{V_{ce}}{V_{ceref}})(\frac{I_{ce}}{I_{ceref}}) \tag{25}$$

E_{offref}, V_{ceref} and I_{ceref} are parameters provided by the datasheet of the device, and V_{ce} is the dc-link voltage. Therefore, at a given dc-link voltage, the turn-off loss of a switch is proportional to the turn-off current:

$$E_{off} = k_{sw} i_{off} \tag{26}$$

The turn-off current of S1 and S2 are i_{pk} and i_{valley}. Let Δi_L represent the inductor current ripple, the turn-off currents at the transition T1-T2 and T3-T4 can be written as:

$$i_{pk} = i_{L\_fund} + \frac{1}{2}\Delta i_L \tag{27}$$

$$i_{valley} = \left| i_{L\_fund} - \frac{1}{2}\Delta i_L \right| = \frac{1}{2}\Delta i_L - i_{L\_fund} \tag{28}$$

Therefore the switching loss in a switching cycle can be written as:

$$E_{sw} = k_{sw} i_{pk} + k_{sw} i_{valley} = k_{sw} \Delta i_L \tag{29}$$

The inductor current ripple can be calculated as:

$$\Delta i_L = |d| \frac{V_{dc} - |v_c|}{f_{sw} L} \tag{30}$$

where d is the duty ratio of the SPWM signal and m_a is the modulation index:

$$d = m_a \sin(\omega_0 t) \tag{31}$$

Since a small inductor is chosen, the impedance of the LC tank at the fundamental frequency is dominated by the impedance of the capacitor. Hence v_c equals to average value of the output voltage from the H-bridge with a small phase shift ϕ caused by the inductor impedance:

$$v_c = V_{dc} m_a \sin(\omega_0 t + \phi) \tag{32}$$

Substituting Eq. (31) and Eq. (32) into Eq. (30), the inductor current ripple at switching frequency can be written as:

$$\Delta i_L = |d| \frac{V_{dc} - |v_c|}{f_{sw} L} = \frac{V_{dc}[1 - |m_a \sin(\omega_0 t + \phi)|]|m_a \sin(\omega_0 t)|}{f_{sw} L} \tag{33}$$

From Eq. (33), it can be inferred that the inductor current ripple varies from each switching cycle. To represent the inductor ripple in a switching cycle, the discrete form of the inductor current ripple can be written as:

$$\Delta i_L(nT_{sw}) = \frac{V_{dc}[1 - |m_a \sin(\omega_0 nT_{sw} + \phi)|]|m_a \sin(\omega_0 nT_{sw})|}{f_{sw} L} \tag{34}$$

The value of n is from 1 to N. And N can be expressed as the ratio between the line frequency and the switching frequency:

$$N = \frac{f_{sw}}{f_0} \tag{35}$$

The switching loss power can be written as the product of the switching energy loss in a line-frequency period and the line frequency. Since the diodes turn off at zero current, the reverse recovery of the diode does not contribute significantly to the switching loss. Hence the switching loss energy in each switching period is given in Eq. (29). And the switching loss of the ripple-port can be written as:

$$P_{switching} = f_0 \sum_{n=1}^{N} E_{sw}(nT_{sw}) = f_0 \sum_{n=1}^{N} k_{sw} \Delta i_L(nT_{sw}) = f_0 k_{sw} \sum_{n=1}^{N} \Delta i_L(nT_{sw}) \tag{36}$$

As shown in Eq. (36) the switching loss can be calculated by summing the inductor current ripple over a line period. Combining Eq. (34) and Eq. (35) into Eq. (36) leads to:

$$P_{switching} = \frac{V_{dc} m_a k_{sw}}{L} \sum_{n=1}^{N} \frac{[1 - \left| m_a \sin(\frac{\omega_0 n}{N f_0} + \phi) \right|] \left| \sin(\frac{\omega_0 n}{N f_0}) \right|}{N} \tag{37}$$

Eq. (37) indicates that the switching loss is not correlated to the switching frequency. Therefore, it is preferable to operate the ripple-port in higher switching frequency to achieve smaller current ripple and reduce conduction loss, which will be discussed in the following analysis.

However, Eq. (37) is only valid when the ripple-port operates in discontinuous conduction mode shown in Figure 32. When the switching frequency exceeds certain

values and the inductor current ripple is small enough, the ripple-port goes into continuous conduction mode and the above analysis is not applicable.

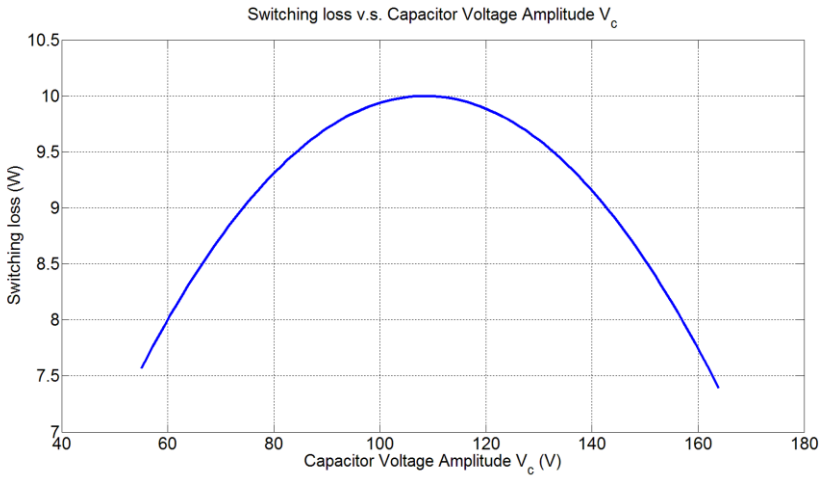


Figure 34 Switching loss v.s. Capacitor voltage amplitude

V_{dc} = 170V; L = 100μH; C = 40μF; $k_{sw} = 2.9\times10^{-5}$; f_{sw} =25kHz

Figure 34 shows the relationship between the switching loss and the capacitor voltage amplitude. The switch used as the example is IRG4PC30FD from International Rectifier. According to the datasheet, k_{sw} can be calculated as 2.9×10^{-5}. The curve shows that the switching loss is maximized when the modulation index is around 0.65 and starts to decrease when the modulation index is larger than 0.65. Since the modulation index is directly related to the voltage across the decoupling capacitor, shown in Eq. (32), the peak capacitor voltage should be designed as close to the dc-link voltage as possible.

Conduction loss calculation

As shown in Figure 32, the inductor current consists of a fundamental frequency component, which represents the average value, and a high frequency component, which represents the current ripple introduced by switching. Therefore the instantaneous value of inductor current is:

$$i_L(t) = i_{L\_fund}(t) + i_{L\_sw}(t) \tag{38}$$

The fundamental component i_{L_fund} is a sinusoidal wave. Since the switching frequency is much higher than the fundamental frequency, i_{L_fund} can be assumed to have a constant value within a switching cycle, denoted as $i_{L\_fund}(nT_{sw})$

$$i_{L\_fund}(nT_{sw}) = I_{L\_fund}\sin(\omega_0 nT_{sw} + \phi + \frac{\pi}{2}) \tag{39}$$

The high frequency component, i_{L_sw}, is a triangular wave with a peak-to-peak value of Δi_L. Therefore, over each switching cycle, the RMS value of the inductor current can be written as:

$$i_{L\_rms}(nT_{sw}) = \sqrt{i^2_{L\_fund}(nT_{sw}) + (\frac{1}{\sqrt{3}}\frac{\Delta i_L(nT_{sw})}{2})^2} \tag{40}$$

Over a line period, the rms value of the inductor current can be calculated by summing up the rms inductor current in each switching cycle and then divided by the number of switching cycles:

$$I_{L\_rms} = \sqrt{\frac{1}{N}\sum_{n=1}^{N} i^2_{L\_rms}(nT_{sw})} = \sqrt{\frac{1}{N}\sum_{n=1}^{N}[i^2_{L\_fund}(nT_{sw}) + (\frac{1}{\sqrt{3}}\frac{\Delta i_L(nT_{sw})}{2})^2]} \tag{41}$$

The result in Eq. (41) can be used to calculate the conduction loss in the resistance associated with the inductor and capacitor.

$$P_{inductor} = I_{L\_rms}^2 r_L \tag{42}$$

$$P_{ESR} = I_{L\_rms}^2 ESR \tag{43}$$

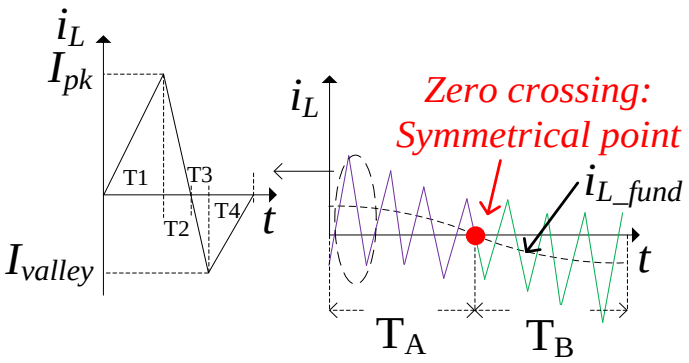


Figure 35 Inductor current waveform of the ripple-port

Figure 35 shows the inductor current waveform for a half of the line period. Since the average inductor current, indicated as i_{L_fund} is symmetrical against the zero crossing point, the instantaneous inductor current in T_A is also symmetrical to the instantaneous inductor current in T_B, against the zero-crossing point of i_{L_fund}.

If integrating the inductor current over the period of T_A+T_B, the total charge in all the T1 periods equals to the total charge in all the T4 periods, because of the symmetric. Similarly, the total charge in all the T2 periods equals to the total charge in all the T3 periods. With this conclusion and referring to Table 4, two conclusions can be drawn. First, the total charge flowing through the switches has the same amount as the total charge flowing through the diodes. Second, at any time instance the inductor current always flows through two devices: a diode and a switch, or, two diodes, or two switches. Therefore to

calculate the conduction loss of the diodes and switches, the H-bridge can be transformed to an equivalent circuit of a diode connected in series with a switch, shown as Figure 36.

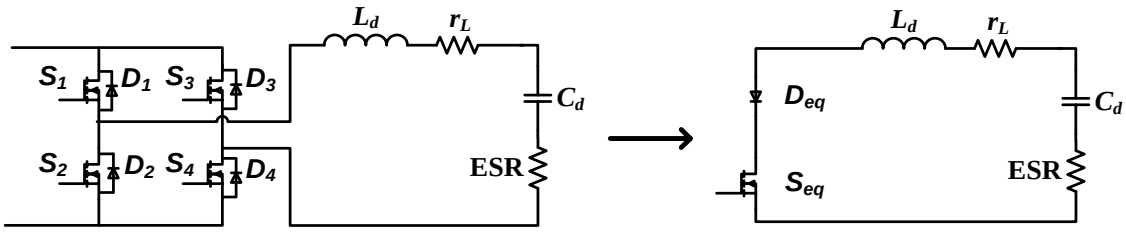
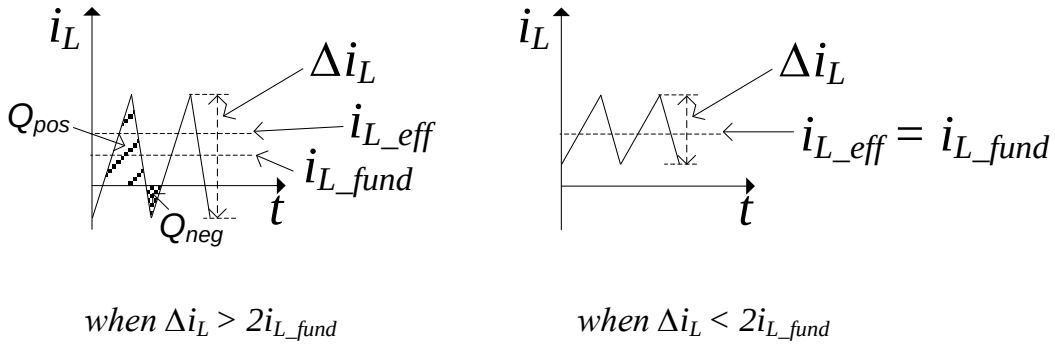


Figure 36 Equivalent circuit for calculating conduction loss of the H-bridge

In order to calculate the conduction loss on the switches and diodes, the average value of current flowing through the device is needed because there is a voltage source in both the models of the switch and diode. However, since the current always flows into the positive terminal of the voltage source, the effective current needed for calculating the conduction loss on the voltage source should be the absolute value of the inductor current.



when $\Delta i_L > 2i_{L\_fund}$ *when* $\Delta i_L < 2i_{L\_fund}$

Figure 37 Effective current for voltage sources loss calculation

As shown in Figure 37, when the inductor current ripple Δi_L is larger than twice of the average inductor current i_{L_fund} and the inductor current goes to negative for a certain period of time. The effective current is the sum of Q_{pos} and Q_{neg} divided by the switching period, while i_{L_fund} is the difference between the charge amount Q_{pos} and Q_{neg} divided by the switching period:

$$\begin{aligned} i_{L\_fund} &= f_{sw}(Q_{pos} - Q_{neg}) \\ i_{L\_eff} &= f_{sw}(Q_{pos} + Q_{neg}) \end{aligned} \tag{44}$$

The ratio of the two triangles` area representing Q_{pos} and Q_{neg} can be found by geometric analysis of the waveform shown in Figure 37:

$$\frac{Q_{pos}}{Q_{neg}} = \left(\frac{i_{L\_fund} + \frac{1}{2}\Delta i_L}{i_{L\_fund} - \frac{1}{2}\Delta i_L}\right)^2 \tag{45}$$

By combining Eq. (44) and Eq. (45), the effective current can be found as:

$$i_{L\_eff}(nT_{sw}) = \frac{2i_{L\_fund}^2(nT_{sw}) + \frac{1}{2}\Delta i_L^2(nT_{sw})}{2\Delta i_L(nT_{sw})} \tag{46}$$

When the inductor current ripple Δi_L is smaller than twice of the average inductor current i_{L_fund}, the effective current equals to the average inductor current. Therefore:

$$i_{L\_eff}(nT_{sw}) = \frac{2i_{L\_fund}^2(nT_{sw}) + \frac{1}{2}\Delta i_L^2(nT_{sw})}{2\Delta i_L(nT_{sw})} \; when \Delta i_L(nT_{sw}) > 2i_{L\_fund}(nT_{sw}) \tag{47}$$

$$i_{L\_eff}(nT_{sw}) = i_{L\_fund}(nT_{sw}) when \Delta i_L(nT_{sw}) < 2i_{L\_fund}(nT_{sw})$$

The average value can be calculated by summing over a line cycle:

$$I_{L\_eff} = \frac{1}{N}\sum_{n=1}^{N} i_{L\_eff}(nT_{sw}) \tag{48}$$

$$P_{switch} = I_{L\_eff} V_{sw} + I_{L\_rms}^2 r_{sw}$$
$$P_{diode} = I_{L\_eff} V_f + I_{L\_rms}^2 r_d \quad (49)$$

To verify the derivation of I_{L_rms} and I_{L_eff}, a Simulink model of the ripple-port is built. The simulation data of the inductor current is logged. The measured inductor RMS current is compared with the predicted inductor RMS current using Eq. (41), shown in Figure 38.

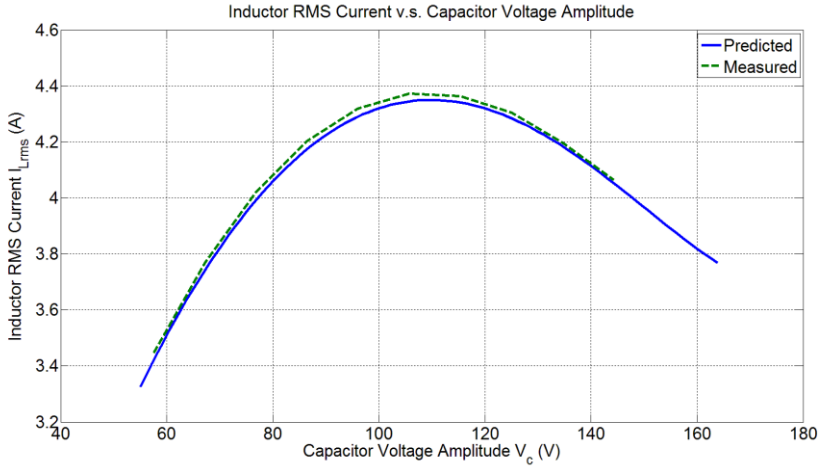


Figure 38 Comparison between the measured I_{L_rms} and calculated I_{L_rms}

The measured effective inductor current is obtained by taking the absolute value of the instantaneous inductor current and then taking the average value. The result is compared with the predicted result in Eq. (48), shown as Figure 39.

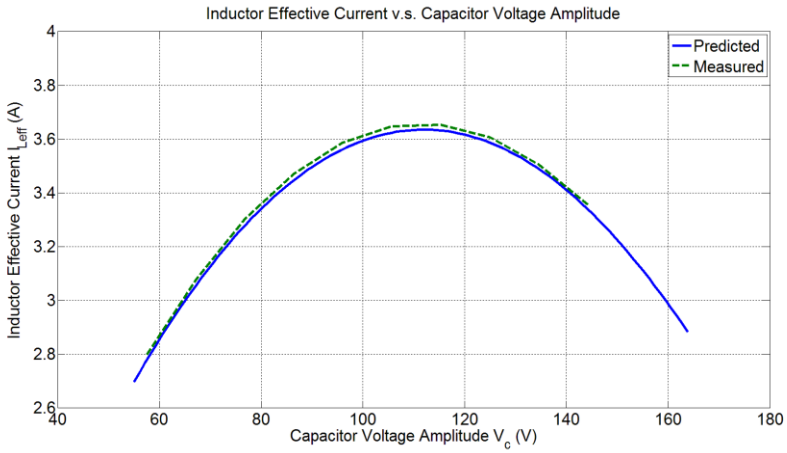


Figure 39 Comparison between the measured I_{L_eff} and calculated I_{L_eff}

Figure 38 and Figure 39 show that the calculation for I_{L_rms} and I_{L_eff} are valid and also reveals the peaking characteristic of curve for the inductor current versus the capacitor voltage amplitude. Once again this result suggests the ripple-port should avoid operating near the peak of the inductor current. To achieve that, the amplitude of the capacitor voltage should be designed close to the dc-link voltage to reduce conduction loss.

Table 5 Specifications of the ripple-port for loss analysis shows an example of using the above loss model to analyze the loss of a ripple-port.

Table 5 Specifications of the ripple-port for loss analysis

Operating conditions	
V_{dc} = 170V; f_{sw} =25kHz; V_c=140V; P_o = 60W	
Component variables	
k_{sw}=2.9×10^{-5}; r_L=0.3Ω; ESR=0.2Ω; V_{sw}=1.07V; R_{sw}=31mΩ; V_f=1.16V;R_d=44mΩ; L = 100μH; C = 40μF;	
Loss contribution	
Switching loss $P_{switching}$	9.2W
Switch Conduction Loss P_{switch}	4.2W
Diode Conduction Loss P_{diode}	4.7W
Inductor winding loss $P_{inductor}$	5.1W
Capacitor ESR loss P_{ESR}	3.4W
Total	26.5W

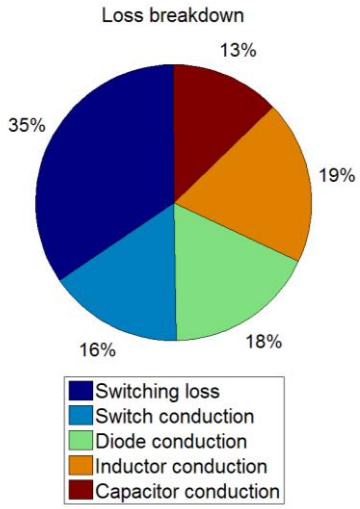


Figure 40 Loss breakdown

Figure 40 shows the sources of power loss. It can be shown that the loss induced by the H-bridge has significant portion, including switching loss and conduction loss of switches and diodes.

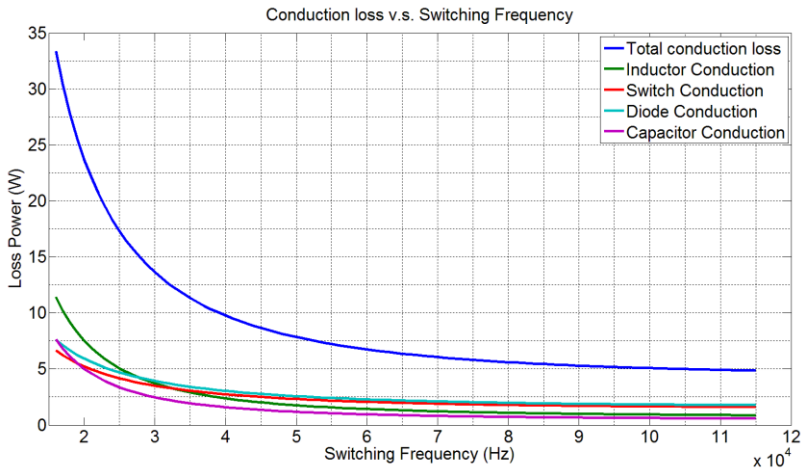


Figure 41 Correlation between conduction loss and switching frequency

Figure 41 shows that the conduction loss reduces significantly when switching frequency is increased to 50kHz. The reduction of conduction loss above 50kHz becomes marginal. In addition, setting the switching frequency too high the inductor current will be in CCM and switching loss will be increased because of hard switching.

4.5 Simulation results

A 60W single-phase rectifier, which rectifies an $110V_{rms}$ sinusoidal input voltage from the utility into a regulated 170V DC voltage on the output, was simulated in Simulink.

Table 6 lists the parameters used in the simulation. In a conventional circuit, 1,330 μF is required at the DC-link. However, using the ripple port requires only 20 μF for the dc bus and 40 μF for the ripple-port decoupling capacitor.

Table 6 AC/DC rectifier with ripple-port simulation parameters

Power Stage design		**Ripple-port control design**	
$\mathbf{V_s}$	110 Vrms	$\mathbf{f_{sw}}$	25kHz
$\mathbf{I_{dc}}$	350mA	$\boldsymbol{\omega_0}$	377 rad/s
$\mathbf{V_{dc}}$	170V	$\mathbf{K_p}$	0.1
$\mathbf{C_{dc}}$	20μF	$\mathbf{K_i}$	1000
$\mathbf{C_D}$	40μF	**B**	$\pi/3$
$\mathbf{L_D}$	100μH	$\boldsymbol{\omega_{cut}}$	0.2

Figure 42 shows the input $p_s(t)$, output $p_o(t)$, and ripple-port $p_{rip}(t)$ power waveforms, which matches with the theoretical waveforms in Figure 13. Figure 43 shows the double-frequency power ripple that has been suppressed to a very small level with around 2% peak-to-peak ripple. This is achieved by the regulating the voltage across the decoupling capacitor to have 45 degree lagging behind the input voltage. To achieve a similar output voltage ripple using dc-link capacitor, a 200μF capacitor is needed, which is 10 times as the dc-link capacitor used in the ripple-port configuration.

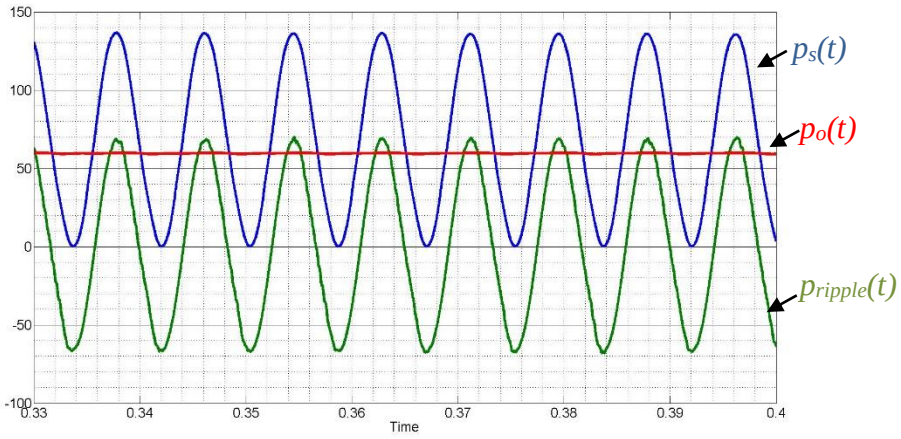


Figure 42 Simulation results - input, output, and ripple power waveforms

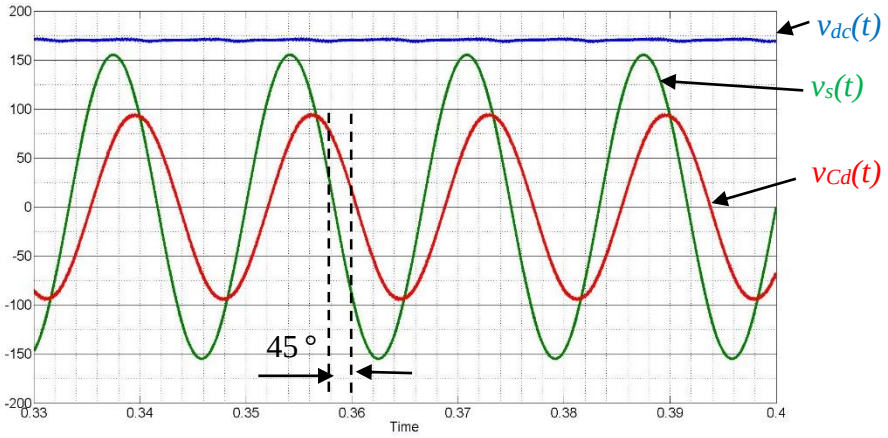


Figure 43 Input, output voltages, and the voltage across the decoupling capacitor

Figure 44 shows the calculated FFT for the input current $i_s(t)$, which indicates a very low THD. The calculated THD is 4.65%. Figure 45 shows the dynamic response when the load steps from 50% to 100%. The output voltage is quickly regulated to 170V without experiencing a long settling time and large voltage sag. This is benefited from the increased voltage loop bandwidth by removing the bulky capacitor at dc-link.

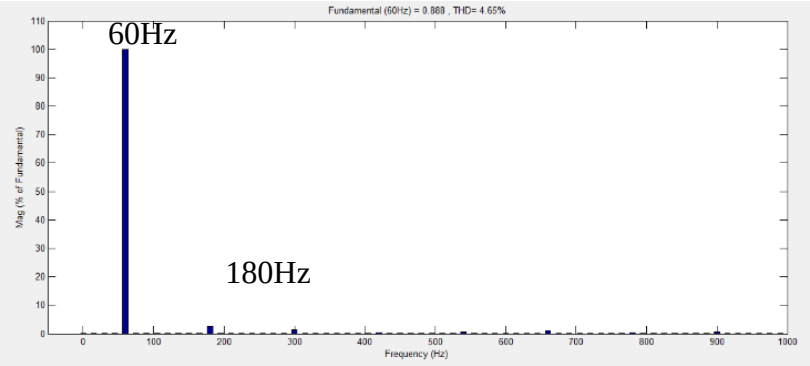


Figure 44 Calculated FFT of the Input Current (in dB)

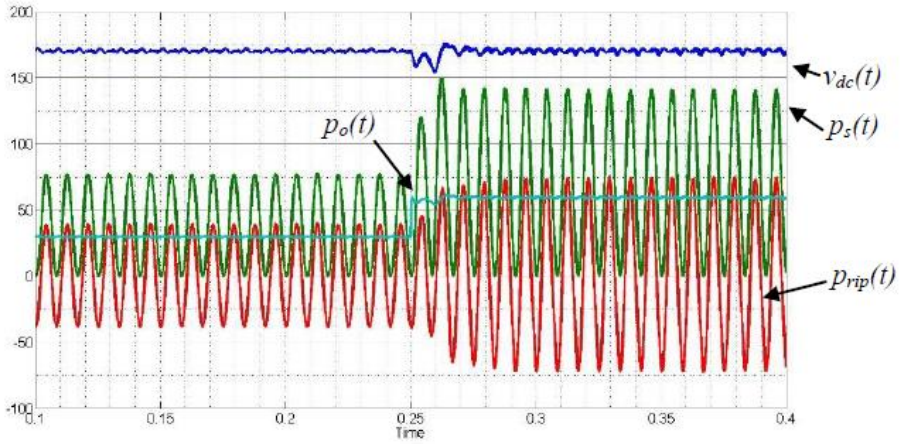


Figure 45 Load dynamic response, from half load to full load

4.6 Experimental results

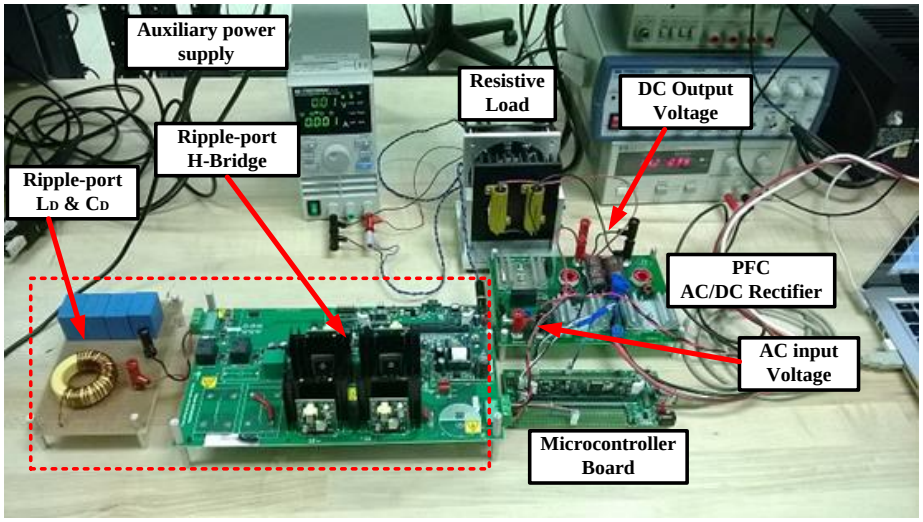


Figure 46 Hardware prototype of a 60W single-phase rectifier with ripple-port

To verify the proposed control scheme and efficiency analysis, a hardware prototype utilizing evaluation boards from Texas Instruments and the Picollo TMS320F28035 MCU is built and tested. Figure 46 shows the setup of the hardware prototype with different stage of the converter being labeled. The microcontroller board controls both the rectifier and ripple-port.

Table 7 Component values and operating conditions for the hardware prototype

Component	Value	Component	Value
Input voltage	$110V_{rms}$ AC @ 60Hz	Decoupling capacitor (C_D)	40 µF
DC-link voltage	$170V_{dc}$	Decoupling inductor (L_D)	100 µH
DC-link capacitance (C_0)	20 µF	Output power (P_0)	60W
PFC f_{sw}	200kHz	Ripple-port f_{sw}	25kHz

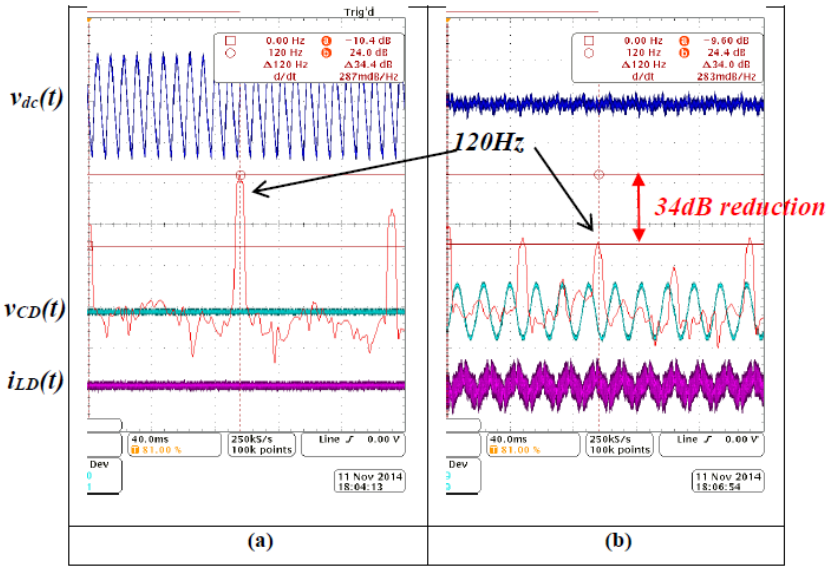


Figure 47 Experimental results: (a) Ripple-port disabled (b) Ripple-port enabled

Figure 47 shows the DC-link output voltage $v_{dc}(t)$, decoupling LC filter's current $i_{LD}(t)$, and decoupling capacitor voltage $v_{CD}(t)$ waveforms. To illustrate the effectiveness of the ripple-port, the waveforms of the proposed circuit operates with the ripple-port disabled are shown in Figure 47(a), the peak-to-peak ripple of $v_{dc}(t)$ is around 52V, since only 20uF capacitor is used. When the ripple-port is enabled, as shown in Figure 47 (b),

the peak-to-peak voltage ripple on $v_{dc}(t)$ is reduced to around 5V. The calculated FFT shows that the double-line-frequency component (120Hz) is suppressed by 34dB.

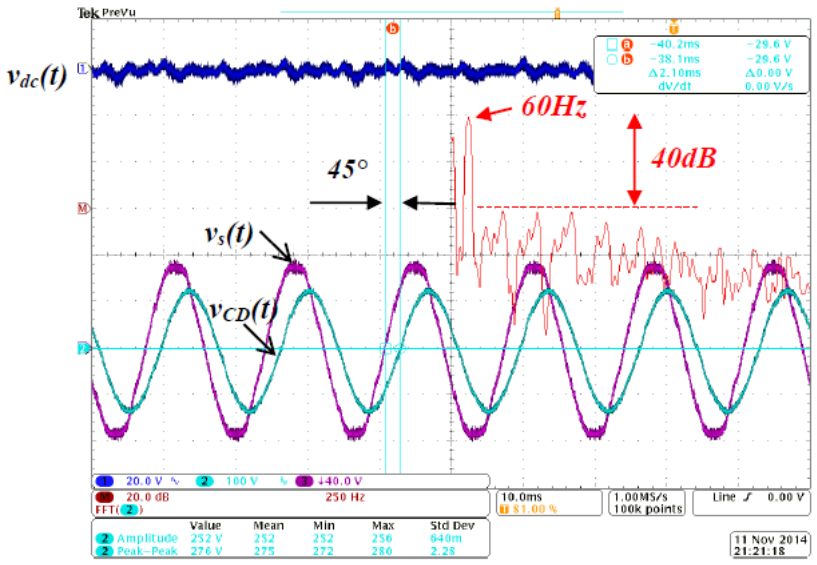


Figure 48 Phase-shift between input voltage and capacitor voltage to achieve ripple-cancellation

Figure 48 shows the efficacy of the current loop control in the ripple-port. With the proposed PR controller, the inductor current $i_{LD}(t)$ is tightly regulated against a sinusoidal reference signal generated by the PLL, which locks the phase of the reference signal with the line voltage with a 45 degree leading offset. The amplitude of the reference signal is calculated in the DSP. As a result, the voltage across the decoupling capacitor $v_{CD}(t)$ lags behind the line voltage by around 45 degree, which makes the power in the ripple-port in phase with the ripple power. FFT of $v_{CD}(t)$ shows that the most significant

harmonic (3^{rd}) is lower than the fundamental by 40dB, which leads to a low THD in the ripple-port power.

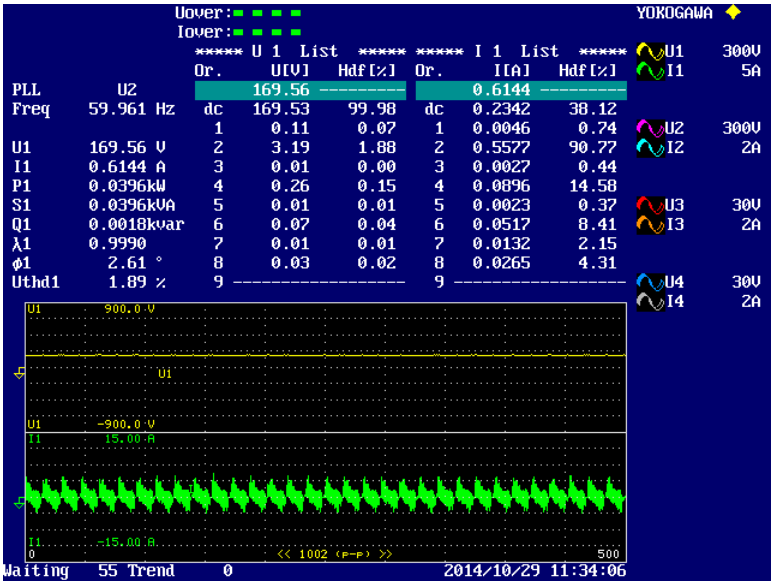


Figure 49 Harmonic content of the input voltage and input current to the ripple-port

Figure 49 shows the measurements from a power analyzer, connecting between a dc power source and the ripple-port, which is operating at the nominal point. The fundamental frequency is the line frequency, i.e. 60Hz. The results shows that the dominant frequency component of the current drawn by the ripple-port is at 120Hz. Besides, the current carries some harmonics in 240Hz and 360Hz, which is caused by the zero-crossing distortion of the capacitor voltage V_{CD}. Another important reading from Figure 49 is the dc component of the current, which indicates the real power drawn by the ripple-port. Since the ripple-port draws reactive power ideally, and Figure 48 shows that

there is no dc offset of the capacitor voltage, the real power indicates the power loss of the ripple-port. The power loss can be calculated as the product of the dc value of the current and the dc-link voltage.

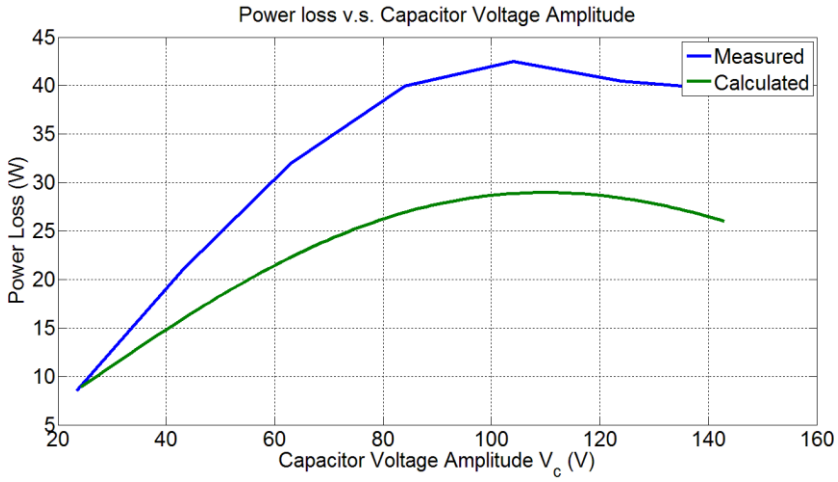


Figure 50 Comparison of power loss between measured value and calculated value

Figure 50 shows the comparison between the measured power loss and calculated power loss according to the loss analysis in the previous section. The measured power loss verifies the conclusion that the power loss is maximized when the capacitor voltage amplitude is around 110V. However, there is about 10W difference between the measured power loss and the calculated power loss. There are several reasons: First, the skin effect of the inductor winding has not been included in the loss analysis. Since the inductor current in the switching frequency is very significant and generates loss on the winding due to the resistance, which is higher than the dc resistance, the extra loss caused by skin effect should not be neglected. Second, the core loss of the inductor is not included in the

loss analysis. But with the large inductor current ripple caused by switching, the core loss caused by the hysteresis of the B-H loop and eddy current cannot be ignored.

In fact, the hardware prototype is operating at a non-optimized condition that the high frequency component in the inductor current is too large compared to the fundamental component, which is not practical for real applications. Provided that the inductor current switching ripple is reduced by increasing the switching frequency or the inductance, the power loss induced by skin effect and inductor core loss will be insignificant so that the loss model derived in the previous section will give a more accurate prediction of the power loss.

4.7 Conclusion

A design example of the ripple-port has been presented in this chapter. The value of the decoupling capacitance is correlated to the allowable voltage swing across the decoupling capacitor, which should be maximized to reduce required capacitance. Additionally, the loss analysis also suggests that operating the ripple-port at the high capacitor voltage swing can reduce rms inductor current, which reduces power loss. Also, the discretization of the controllers using bilinear transform has been discussed. Simulation and experimental results verify the proposed control scheme is capable of the ensuring ripple-cancellation.

CHAPTER V

APPLYING RIPPLE-PORT TO LED APPLICATIONS

5.1 Introduction

The most significant advantage of ripple-port configuration is the high reliability because of the elimination of electrolytic capacitor. For solid-state-lighting, the life-time of LED driver is limited by the bulk capacitor, which often utilize electrolytic capacitor for its high power density. Therefore, applying the ripple-port configuration to LED applications can extend the lifetime of the existing solutions. This chapter provides an overview of how ripple-port configuration can improve the reliability to LED applications as well as the tradeoffs in volume and efficiency.

5.2 Common-used circuit topologies for offline LED driver

For LED drivers connected to the line, must follow the International Electrotechnical Commisson IEC61000-3-2 standard, which specifies the harmonics content in the current drawn from the line. Therefore, a single-stage PFC regulator or a two-stage converter with the first stage as PFC regulator are commonly used in offline LED driver design [65-71], shown as Figure 51.

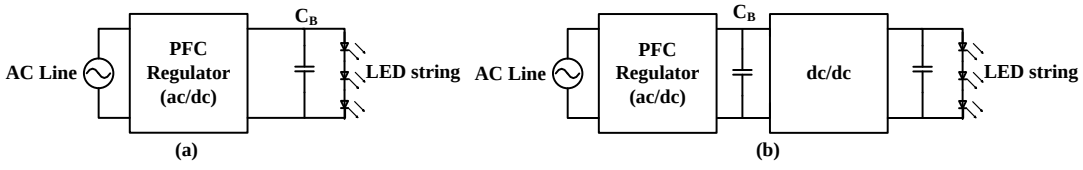


Figure 51 (a) Single- and (b) Two-stage architecture used for LED drivers

For a majority of low-power lighting fixtures in the United States are designed for LED strings below 42V for safety regulations [72]. However, for high-power lighting applications, low-voltage LED needs multiple parallel-connected strings to achieve high brightness, which requires extra current balancing circuit to guarantee every LED string is driven by the same amount of current. On the other hand, high-voltage LEDs can achieve high brightness without extra circuit.

The choice of circuit topology for the PFC regulator depends on the specifications for output voltage and isolation requirement. Fly-back converter is a very popular topology because the voltage conversion ratio can be modulated by the designing the turns ratio of the transformer. Plus, the transformer provides galvanic isolation, which meets the safety requirements for certain applications. Boost converter is commonly used as PFC pre-regulator, where a high dc-link voltage, typically around 450V, is generated from the line. Therefore, boost converter is also adopted in single-stage non-isolated LED drivers for high-voltage LED or used as the first-stage PFC in a two-stage architecture. Compared to isolated converter, the Boost converter has a more straight-forward output voltage sensing.

5.3 Double-line frequency flickers in offline LED lighting application

Similar to the single-phase rectifier, the offline LED has the design challenge of handling the double-line frequency ripple. The problem is exaggerated in lighting application because the resulted flicker, although invisible, can lead to health effects such as headaches and eye-strain.

Since the luminous of the LED is determined by the driving current, the figure of merit for flicker performance of LED drivers is the output current ripple. Since LED is non-resistive device, the correlation between current ripple and voltage ripple depends on the dc operating point, shown as Figure 52.

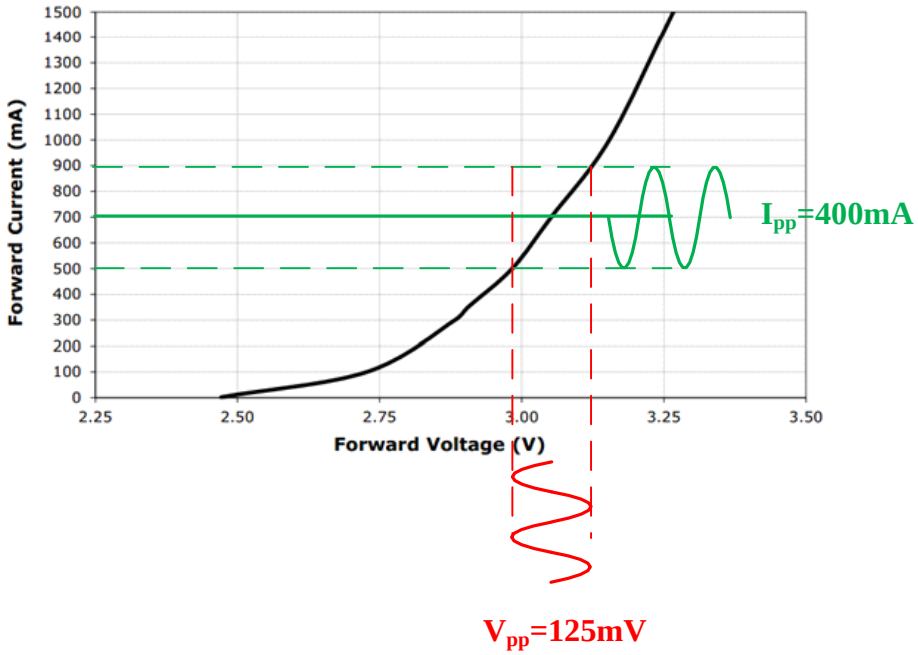


Figure 52 Correlation between current ripple and voltage ripple of Cree XLamp XP-G LEDs

Figure 52 illustrates the correlation between current ripple and voltage ripple of a LED, using Cree XLamp XP-G LEDs as an example. When the LED is driven by current source with 700mA average current and 400mA peak-to-peak ripple, according to the V-I characteristic the voltage ripple will be 125mV.

Most LEDs are rated below 1A and hence multiple LEDs are connected in series as a string to achieve certain output power. Therefore, the voltage ripple seen by the LED driver is given by Eq. (50)

$$V_{o\_ripple} = n \times V_{pp}\Big|_{I_{pp}} \tag{50}$$

The output voltage ripple of the LED driver is specified as the product of the number of LEDs in the string, n, and the voltage ripple V_{pp} of a LED under certain current ripple specification Ipp. As shown in Eq. (50), for a fixed current ripple specification, the more LEDs are connected in series, the larger output voltage ripple can be allowed for the LED driver, which implies the advantage of high-voltage LED string that a smaller filtering capacitor can be used in the driver.

5.4 Reliability issue of conventional offline LED lighting application

The most straight forward approach to achieve low current ripple in LED driver is to connect a bulk filtering capacitor in parallel with the LED. Three types of capacitors are generally available for dc-link applications, which are the Aluminum Electrolytic Capacitors(Al-Caps), Metallized Polypropylene Film Capacitors (MPPF Caps) and high capacitance Multi-Layer Ceramic Capacitors (MLC-Caps) [16]. Considering the cost and size requirements of the LED driver design, Al-Cap is generally employed for its high capacitance/(volume*cost). Yet it has been widely acknowledged that Al-Cap has the lowest operational lifetime among the three options. While the LEDs has extremely long lifetime which can reach 100000 hours under proper thermal design and good electrical protection, the lifetime of Al-Cap can hardly reach 10000 hours under the high operating temperature inside the lighting fixture [73].

5.5 Comparison between ripple-port configuration and conventional solutions

There are various design constraints to be considered in order to compare the ripple-port configuration to the conventional dc-link capacitor solution. For offline LED drivers, the most important figure of merits are efficiency, reliability, size and cost.

The analysis of ripple-port integrated rectifier in the previous chapters assume a 100% efficiency for the ripple-port, which is obviously impossible in practical design. As shown in the Chapter IV, the power loss of the ripple-port leads to a dc current drawn by the ripple-port from the dc-link, which suggests that the power of the ripple-port has a dc component, which represents the power loss, and a ripple component, which is the reactive power used to cancel the double-line frequency ripple power. The instantaneous power of the ripple-port is written in Eq. (51).

$$p_{rpp}(t) = P_{rpp\_loss} + P_{rpp\_ripple}\cos(2\omega_0 t) \tag{51}$$

The efficiency of the ripple-port is defined as:

$$\eta_{rpp} = \frac{P_{rpp\_ripple}}{P_{rpp\_loss} + P_{rpp\_ripple}} \tag{52}$$

Since PFC regulator can achieve power factor close to unity and low input current THD, it is valid to assume that the instantaneous input power consists of a dc component, which represents the average power, and a double-line frequency component, which represents the ripple power. Furthermore, the amount of double-line frequency ripple is determined by the average input power drawn. Considering that the power must be balanced between input and output, the average input power is the sum of the power goes

into the LED and the loss power of the ripple-port, divided by the efficiency of the PFC regulator. Therefore, the instantaneous input power of the LED driver can be written as:

$$p_s(t) = P_{avg} + P_{avg}\cos(2\omega_0 t) = \frac{P_{LED} + P_{rpp\_loss}}{\eta_{PFC}} + \frac{P_{LED} + P_{rpp\_loss}}{\eta_{PFC}}\cos(2\omega_0 t) \quad (53)$$

And the instantaneous power at the dc-link can be written as:

$$p_{dc\_link}(t) = \eta_{PFC}\, p_s(t) = (P_{LED} + P_{rpp\_loss}) + (P_{LED} + P_{rpp\_loss})\cos(2\omega_0 t) \quad (54)$$

5.5.1 Capacitor size and cost

In the previous discussion, it is assumed that the ripple-port decouples all the double-line frequency ripple in the input power to eliminate the double-line frequency ripple at the output voltage. However, the ripple-port can also decouple only part of double-line frequency ripple, depends on how small the output voltage ripple needs to achieve. Let K represents the ratio of ripple-port power divided by the total double-line frequency ripple power:

$$K = \frac{P_{rpp\_ripple}}{P_{LED} + P_{rpp\_loss}} \quad (55)$$

The value of K is designed between any values 0 to 1, indicating how much power is decoupled by the ripple-port. When K=0, the ripple-port is not activated and all the double-line frequency ripple is filtered by the dc-link capacitor, which represents the conventional LED driver. When K=1, the ripple-port decouples all the double-line frequency ripple.

When K is less than 1, there is a difference between the input double-line frequency ripple and the ripple-port ripple power, a dc-link capacitor is required to filter the ripple power presented at the dc-link and the required capacitance is:

$$C_o = \frac{(P_{LED} + P_{rpp\_loss}) - P_{rpp\_ripple}}{\omega_0 V_{dc} V_{o\_pp}} \tag{56}$$

where V_{o_pp} is the peak-to-peak output voltage ripple needs to be achieved, V_{dc} is the average value of the output voltage.

The required capacitance for the decoupling capacitor in the ripple-port can be written as:

$$C_D = \frac{2P_{rpp\_ripple}}{V_{C_D}^2 \omega_o} \tag{57}$$

As discussed in Chapter IV, the amplitude of the voltage across the decoupling capacitor, V_{CD} should be chosen as close to the V_{dc} as possible to minimize required capacitance and to reduce RMS current in the ripple-port. It is reasonable to set V_{CD} as 90% of V_{dc} with 10% margin to avoid over modulation of ripple-port. Substituting Eq. (52) and Eq. (55) into Eq. (56) and Eq. (57), the CD and Co can be expressed as:

$$C_o = \frac{P_{LED}(1-K)\eta_{rpp}}{\omega_0 V_{dc} V_{o\_pp}(\eta_{rpp} - K + K\eta_{rpp})} \tag{58}$$

$$C_D = \frac{2P_{LED} K \eta_{rpp}}{(0.9V_{dc})^2 \omega_o (\eta_{rpp} - K + K\eta_{rpp})} \tag{59}$$

$$C_{total} = C_o + C_D \tag{60}$$

Since K=0 represents the conventional solution, and K=1 represents the ripple-port with maximum capacitance reduction. The maximum reduction ratio of required capacitance can be written as:

$$\frac{C_{total}\big|_{K=0}}{C_{total}\big|_{K=1}} = \frac{0.81(2\eta_{rpp}-1)V_{dc}}{V_{o\_pp}} = \frac{0.81(2\eta_{rpp}-1)}{d_{ripple}} \tag{61}$$

where d_{ripple} represents the percentage of peak-to-peak voltage ripple divided by the dc-link voltage. Eq. (61) shows that the maximum reduction ratio depends on two variables: the ripple-port efficiency and the percentage of voltage ripple.

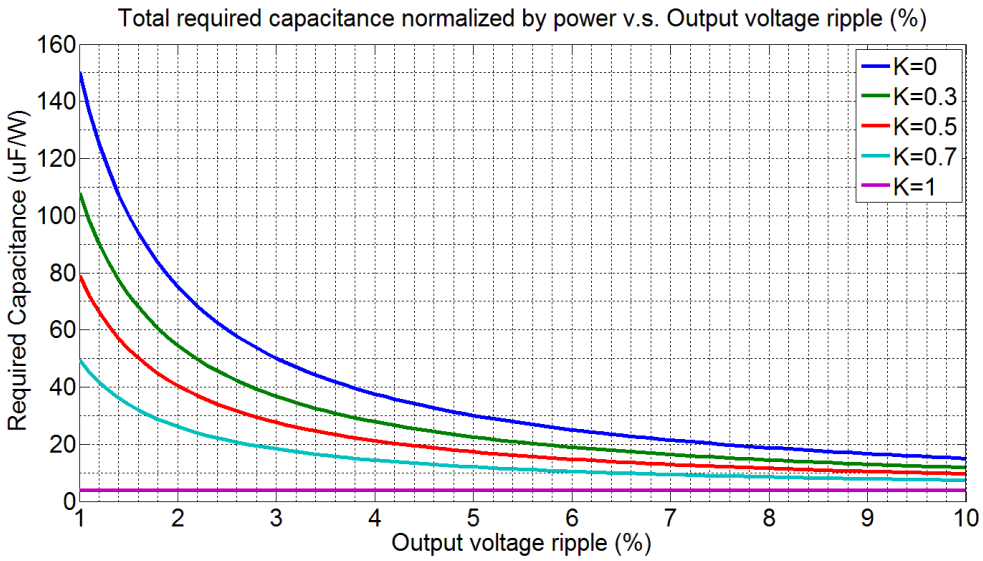


Figure 53 Normalized required capacitance v.s output voltage ripple

η_{rpp}=95%, η_{PFC}=90%, V_{dc}=42V

Figure 53 shows an example of the required capacitance for an LED driver with 170V dc-link voltage. In this example, it is assumed that the ripple-port achieves 95%

efficiency and the PFC regulator achieves 90% efficiency, which are the typical specifications in the industry for single-phase inverter and rectifier [74-78]. The required capacitance is normalized against the LED power to show the μFarad/watt in different K value. It is found that when very small output voltage ripple is required, the ripple-port configuration reduces the required capacitance significantly, for example, 20x at 1% V_{o_pp} and K=1. Also, it is shown that when K is chosen close to 1, the required capacitance is reduced more significantly.

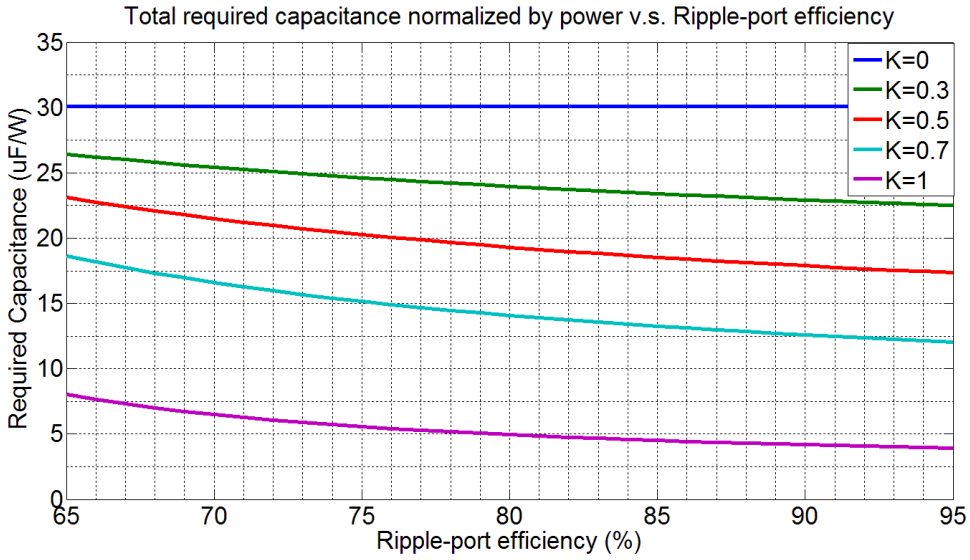


Figure 54 Normalized required capacitance v.s Ripple-port efficiency

η_{PFC}=90%, V_{o_pp}=5%V_{dc}, V_{dc}=42V

Figure 54 shows that the ripple-port efficiency affects the required capacitance significantly. For K=1, the required capacitance is doubled, from 4μF/W to 8 μF/W, when the ripple-port efficiency decreases from 95% to 65%. Therefore, it is of great importance

to optimize the ripple-port design to achieve high efficiency in order to reduce required capacitance.

5.5.2 Efficiency

According to Eq. (55), the reactive power drawn by the ripple-port equals to the ripple-component in Eq. (54), scaled by K.

$$P_{rpp\_ripple} = K(P_{LED} + P_{rpp\_loss}) \tag{62}$$

The overall efficiency of the LED driver with ripple-port configuration can be written as the ratio between LED power and the average input power:

$$\eta_0 = \frac{P_{LED}}{(P_{LED} + P_{rpp\_loss})/\eta_{PFC}} \tag{63}$$

Substituting Eq. (52) and Eq. (62) into Eq. (63):

$$\eta_0 = \frac{\eta_{rpp} - K + K\eta_{rpp}}{\eta_{rpp}} \eta_{PFC} \tag{64}$$

Typical efficiency of a PFC regulator, utilized as offline LED driver, is between 85% to 95%.

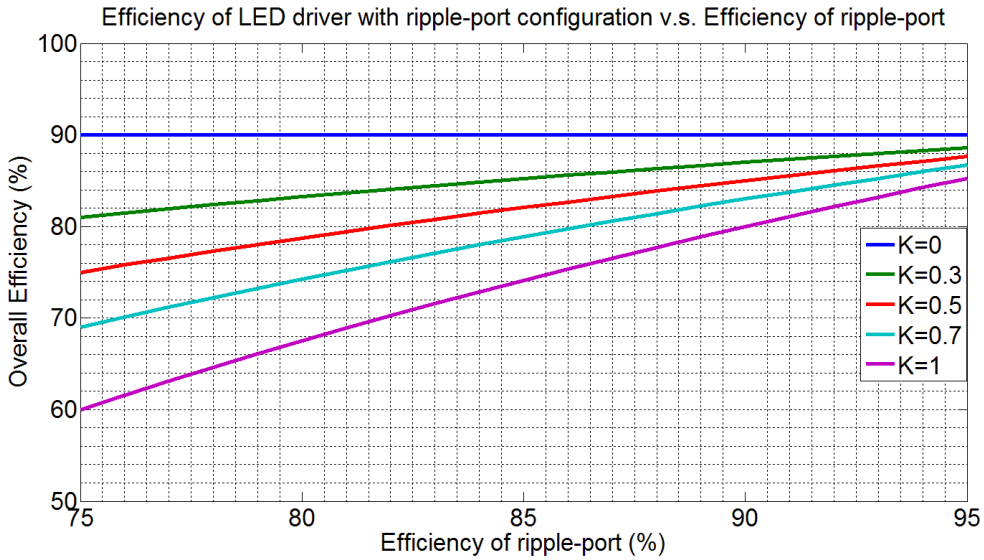


Figure 55 Overall Efficiency v.s. Ripple-port Efficiency

η_{PFC}=90%

Figure 55 shows the efficiency of the LED driver with ripple-port configuration when PFC regulator achieves 90% efficiency. The x-axis the efficiency of the ripple-port, varying from 75% to 95%. When K=0, corresponding to the conventional solution, the overall efficiency is the efficiency of the PFC regulator since all the power is processed by the PFC regulator only. It is shown that the overall efficiency degrades when K increases, since more power loss is generated by the ripple-port. It can be inferred from Figure 55 that the overall efficiency can be controlled by modulating the coefficient K, this is an advantage of ripple-port configuration over the cascading two-stage architecture, where the overall efficiency is always the product of the efficiency of the two stages. However, reducing K to achieve higher overall efficiency will increase total required

capacitance, as shown in Figure 53. Therefore, an important design tradeoff for the ripple-port configuration is the efficiency against the total required capacitance.

5.6 Conclusion

This chapter reviews the reliability challenges in offline LED lighting applications caused by the filtering capacitor. Three common types of filtering capacitors are reviewed and it is concluded that Metalized Polypropylene Film capacitor is the most suitable alternative for the Aluminum Electrolytic capacitor to improve the reliability of the driver circuits. However, the total required capacitance must be reduced to enable the replacement. Applying ripple-port configuration to LED lighting applications involves the tradeoffs between efficiency and capacitor size. A design variable K, indicating the amount of ripple-power decoupled by the ripple-port, is introduced to give a quantified evaluation of the tradeoffs and comparison between ripple-port configuration and the conventional solutions.

CHAPTER VI

CONCLUSION AND FUTURE WORK

AC/DC converters is widely needed to rectify the AC power from grid to power the dc devices. Single-phase rectifier inherently suffers from the double-line frequency ripple problem, which requires energy storage components to decouple it from the dc load. The energy storage can either be a passive component, such as an inductor or a capacitor, or an active filtering circuit. For conventional single-phase rectifiers, a bulky capacitor is employed at the dc-link because of its high capacitance/(volume*cost). However, its low reliability makes it unsuitable for applications requiring long operational life, such as solid state lighting.

Previous existing approaches to eliminate the electrolytic capacitor have been reviewed, including cascading two-stage converter, input current harmonics injection and dc-bus-connected filter, which have the same goal: to reduce the required capacitance so that film capacitor can replace the electrolytic capacitor. Ripple-port configuration had been proposed in previous literature and it is suggested as the most effective solution in achieving the minimum required capacitance. The objective of this thesis is to design a control scheme for the ripple-port configuration and evaluate the effectiveness of applying this technology to offline LED drivers.

The control objectives had been analyzed and it is concluded that the control loop must provide accurate phase and amplitude regulation of the power in the ripple-port. Thus a current control loop with PR controller is proposed for the ripple-port. In addition, a

feed-forward control, including amplitude calculation and phase-locked-loop, is added between the AC/DC converter and the ripple-port.

A circuit topology with Boost PFC regulator as the AC/DC stage and an H-bridge inverter as the ripple-port is chosen as an example to illustrate the design of a ripple-port integrated rectifier. The discussion was focused on the ripple-port design and the interaction between the ripple-port and the PFC regulator. In the design example, it is illustrated how to design the decoupling capacitor in the ripple-port to achieve minimum capacitance and to optimize efficiency. A loss model is derived to show how to choose the operating point of the ripple-port, including switching frequency, voltage swing and inductor sizing. A Texas Instrument microcontroller is used to implement the digital controller, which involves discretizing the controller design and selecting the proper sampling frequency for the feedback signals. Simulation and experimental results is presented to verify the design example.

When applying the ripple-port configuration to practical offline LED driver design, more realistic variables needs to be considered, such as the efficiency of the ripple-port and the output voltage ripple. These variables affect the overall efficiency and required capacitance significantly. The K coefficient, which controls how the double-line frequency ripple power is distributed between the dc-link and the ripple-port, is introduced. By properly choosing K, the design can achieve the optimized tradeoff between overall efficiency and required capacitance according to the design specifications.

The extension of this work might focus on the following aspects:

- Feedback control of the dc-link voltage ripple. The response of the dc-link voltage ripple is not monotonic to the control signal, therefore the feedback control requires comparison between the present state and the previous state to decide whether to increase or decrease the control signal, similar to the MPPT algorithm.
- Optimize the hardware design to achieve high efficiency. Compare the efficiency between continuous conduction mode (CCM), discontinuous conduction mode (DCM) and critical conduction mode (CRM) operation of the ripple-port. Then choose the optimal operating mode.

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