A MULTIBAND LOW NOISE AMPLIFIER FOR SOFTWARE DEFINED RADIO USING SWITCHABLE ACTIVE SHUNT FEEDBACK INPUT MATCHING

A Thesis

by

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ABSTRACT

Radio frequency (RF) receivers are the key front-end blocks in wireless devices such as smartphones, pagers, PDAs etc. An important block of the RF receiver is the Low-noise amplifier. It's function is to amplify with little noise addition, the RF signal received at the atenna. Modern wireless devices for example the smartphone, incorporates multiple functionalities supported by various RF standards- GPS, Bluetooth, Wifi, GSM etc. Thus, the current trend in the wireless technology is to integrate radio receivers for each RF standard into a single system-on-chip (SoC) in order to reduce cost and area of the devices. In view of this, multiband RF receivers have been developed which feature multiband LNAs.

This thesis presents the design and implementation of a multiband LNA for Software Defined Radio Applications. In this thesis, basic radio-frequency concepts are discussed which is followed by a discussion of pros and cons of various multistandard low-noise amplifier topologies. This is then followed by the design of the proposed reconfigurable LNA. The LNA is designed and fabricated in IBM 0.18um CMOS technology. It is made up of dual LC resonant tanks, one to switch between 5.2GHz and 3.5GHz frequency bands and the other, to switch between 2.4GHz and 1.8GHz bands. The input matching of the LNA is achieved using a switchable shunt active feedback network. The LNA achieves S21 of between 10.1dB and 13.43dB. It achieves an input matching (S11) between -13.44 dB and -11.97 dB. The noise figure measured ranges from 2.8 dB to 4.3 dB. The LNA also achieves an IIP3 from -7.12 dBm to -3.45 dBm at 50 MHz offset. The power consumption ranges from 7 mW to 7.2 mW.

DEDICATION

I dedicate this work to my Lord and Savior Jesus Christ

ACKNOWLEDGEMENTS

My utmost thanks is to the Most High God, who has been my guide through my master's program.

Secondly, I would like to express many thanks to my advisor, Dr. Kamran Entesari, for providing me with the necessary guidance through my master's program. I would also like to thank Dr. Jose Silva-Martinez, Dr. I-Hong Hou and Dr. Jaakko Jarvi for serving on my thesis committee.

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1. INTRODUCTION

1.1 Motivation

This era is marked by increasing development in communication technology due to the spiraling growth in wireless applications and the ever increasing demand for high speed data communication. The wireless industry is the major contributor to the rapid growth in communication technology. Today, various portable wireless communication devices can be found on the electronic market -from smartphones, notebook computers,pagers, PDAs to handheld portable games such as the Playstation Portable (PSP). Tremendous effort has been invested to develop wireless terminals that integrate multiple functionalities. For example, one can use today's smartphone to make phone calls, for navigation/exploration, for internet connectivity, for short range connectivity and data transfer between the two smartphones. Several wireless communication standards exist for each of these functionalities.

The RF standards which have emerged as a result include but not limited to GSM900, DCS1800, PCS1900 and WCDMA standards for cellular communication; WLAN a/b/g/n, UWB and Bluetooth standards for wireless data connectivity and communication; GPS for navigation; and FM radio standards for entertainment [1]. Table 1-1 illustrates the various RF standards with respect to their applications and frequency bands.

Table 1-1 : Wireless standards [2]

Standard	Application	Carrier Frequency
GSM	Voice	925-960 MHz 1.710-1.785 GHz
DCS 1800	Voice	1.805-1.88 GHz 1.85-1.91 GHz
PCS 1900	Voice	1.93-1.99 GHz
GPS	Location	1.57542 GHz
Bluetooth	Data	2.4-2.4835 GHz
UWB	Data	3.1-10.6 GHz
IEEE 802.11a	Data	5.15-5.85 GHz
IEEE 802.11b	Data	2.4-2.48GHz
Zigbee 802.15.3	Data	868-868.6 MHz 2.412-2.472 GHz
WiMax 802.16a	Data	2-11 GHz

These wireless communication standards continue to grow in number. As a result, recent research in wireless communications has moved towards achieving multiband RF receivers which are the core of mobile terminals [3]. For example, Chang *et al.* [4] reported a dual-band heterodyne receiver for 2.4/5.2-GHZ wireless local area network applications. Wu *et al.* [5] demonstrated a 900-MHz-1.8-GHz dual-band heterodyne receiver employing

weaver architecture. Dongpo *et al.* [6] showcased a dual-band concurrent receiver for 1.2/1.57 GHz next generation of global navigation satellite systems (GNSSs). The main goal in the design of these multiband receiver architectures is to share as many as possible, building blocks for various standards to reduce the cost and area of mobile devices [3]. A key block of any RF receiver is the Low Noise Amplifier (LNA). It is the first amplification block in the RF receiving path as shown in Figure 1-1. In fact, the performance of the RF receiver is significantly influenced by the LNA. The LNA plays an important role in amplifying the received signal while adding little noise to it. As shown in Figure 1-1, the received signal is filtered, amplified by the LNA and translated to base-band by mixing with a local-oscillator (LO)[7]. The signal is then filtered after which it is applied to an analog-to-digital converter (ADC) which digitizes the analog signal. The digital signal is then processed in a digital signal processing unit (DSP).

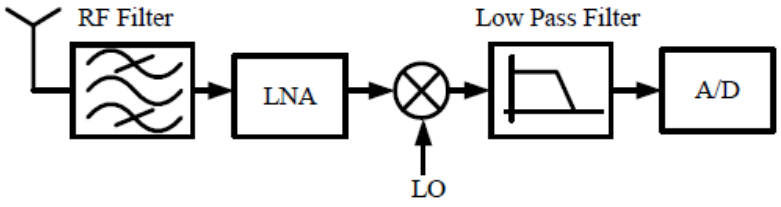


Figure 1-1: A typical receiver block diagram showing LNA[7]

A classical multiband system that makes use of the LNA is the Software Defined Radio (SDR). SDR is a radio communication system where components that have been

typically implemented in hardware (e.g mixers, filters, modulatos/demodulators, etc) are instead implemented by means of a software on a personal computer or embedded system. The ideal software defined radio receiver[8] consists of an antenna, an LNA, an analog-to-digital converter (ADC) and a digital signal processing chip as shown in Figure 1-2. The SDR converts the modulated RF analog signal received by the atenna into digital signal which is achieved by the ADC. The DSP and general purpose processor then handle the processing of the signal.

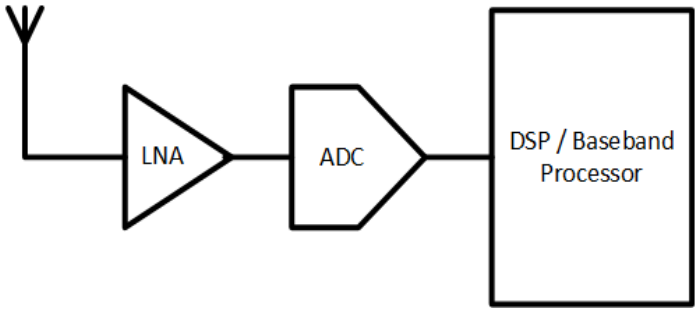


Figure 1-2: Basic architecture of SDR[8]

The basic concept behind the software defined radio is to configure the receiver settings using software so as to select and process signal(s) belonging to a particular frequency band at a particular time. This implies there is the need for a reconfigurable LNA which would select a specific frequency band at a time. Different standards have different specifications of signal level and noise required at the input of the ADC.

Therefore, such LNAs should provide specific gains in addition to selecting a specific frequency band and as add as small as possible noise to the received RF signal. This work presents a reconfigurable Low Noise Amplifier for Software defined radio applications at target frequencies of 1.8/2.4/3.5/5 GHz using IBM CMOS technology.

1.2 Thesis Objectives

The objective of this thesis is to present a reconfigurable LNA for software defined radios using switchable gm active shunt feedback input matching. The LNA is designed to switch these standards; GSM (1.8GHz), Bluetooth (2.4 GHz) , WiMax (3.5GHz) and IEEE 802.11a. The LNA was developed using the IBM 0.18um CMOS7RF process and was fabricated by MOSIS.

1.3 Thesis Outline

This thesis is organized as follows: Section 2 reviews basic RF concepts such as impedance matching, noise figure, linearity, stability, scattering parameters and passives. It also elaborates on LNA topologies, a brief literature review and the proposed LNA architecture. Section 3 covers the design process and the simulated and measured results of the proposed LNA. Section 4 highlights the conclusions and future works.

2. REVIEW OF RF CONCEPTS AND MULTIBAND RECONFIGURABLE LNA ARCHITECTURES

This section highlights the required basic RF concepts in the design of the proposed LNA. It also talks about some performance trade-offs involved in the design of LNAs. The section concludes with literature review of state-of-the-art reconfigurable LNAs.

2.1 Basic RF Concepts

The LNA is a key block in any receiver chain. It is typically the first active-signal processing block after the antenna. The received RF signal is normally accompanied by interferers with significant amplitudes. The LNA should hence be able to amplify all these signals without causing much distortion in the receiver chain. Moreover, the level of received RF signal is typically small and as the sensitivity of the LNA determines the sensitivity of the entire receiver, the LNA should add very little noise to the signal chain. The LNA as the first active block in the receiver chain should be able to provide significant gain in order to suppress the noise of subsequent blocks. These factors among others are very vital in the design of the LNA and need a careful study. This chapter highlights the review of RF concepts such as noise, linearity, gain , matching and other concepts relating to passives such as quality factor, noise etc.

2.1.1 Noise Figure

Noise is a major limiting factor in most RF circuits and is any signal other than the desired RF signal. Without noise, an RF receiver would be able to detect very small

input signals, allowing communication across very long distances [7]. Noise comes in many forms with different mechanisms of generation. In RF systems, the noise of any device is characterized by the parameter known as Noise Factor (F).The noise factor of a device is a measure of the signal-to-noise ratio degradation as the signal is processed through the circuit and is normally expressed in decibels in which case it is called Noise Figure(NF). The noise figure of a device is defined as:

$$NF = 10log_{10}F = 10log_{10}\frac{SNR_{in}}{SNR_{out}} \qquad 2-1$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratios at the input and at the output of the two-port circuit respectively. A receiver system is made up of many blocks(active and passive) cascaded in series. As the signal propagates from the antenna to the ADC, noise is introduced by different blocks to the signal. The effective *NF* of the system is dependent on the *NF* of each block as well as the gain of preceding stages.

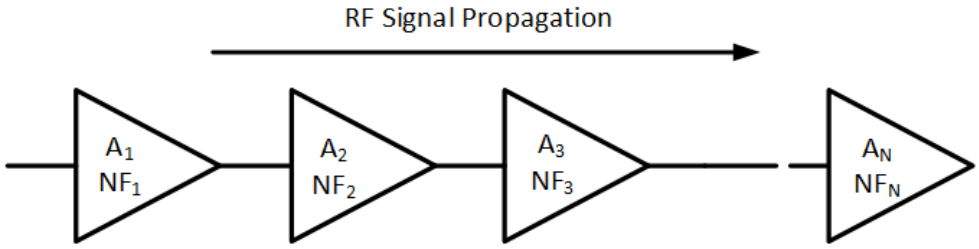


Figure 2-1: Cascade of noisy blocks[7]

The NF of a cascaded system as shown in Figure 2-1 according to Friis [7] is given by :

$$NF_{tot} = NF_1 + \frac{NF_2}{A_1} + \frac{NF_3}{A_1 A_2} + \cdots + \frac{NF_N}{A_1 A_2 \ldots A_{(N-1)}} \qquad 2-2$$

Where NF_m and A_m are the noise factor and the available power gain of the m[th] stage. According to this equation, the noise contributed by each stage decreases as the gain of the preceding stage increases. Thus, the first few stages in a cascade are the most critical stages. In practice, the LNA is the first active block in the receiving chain. Therefore, its NF directly adds to that of the system. An LNA should provide enough gain to overcome the noise contribution of the subsequent stages and add as little noise as possible. NF_{tot} determines the sensitivity of the overall receiver.

2.1.2 Sensitivity

Sensitivity is defined as the minimum signal level that a receiver can detect with appreciable quality [7]. The appreciable quality is defined as sufficient signal-to-noise ratio (SNR) in the presence of noise. The SNR itself depends on the type of modulation and the bit error rate (BER) that the system can tolerate. Sensitivity is analytically given by :

$$Sensitivity(dBm) = -\frac{174dBm}{Hz} + 10\ log\ (BW) + NF_{tot} + 10\log(SNR_{out})\ 2-3$$

where -174dBm/Hz is the available noise power from the antenna (noise floor) and *BW* is the bandwidth of the desired signal, and the last term is the minimum acceptable SNR at the receiver output.

2.1.3 Non-Linear Effects

The linearity of a system determines the maximum allowable input signal level. Active devices exhibit some form of non-linearity one way or the other. Non-linear

behavior of the devices in circuits leads to signal distortion. The common measures of linearity for RF circuits are the *1-dB compression point (P_{1dB})* and the *third-order intercept point (IIP3)* [7].

2.1.3.1 The 1-dB Compression Point

The input 1-dB compression point is normally defined as the amplitude of the input signal at which the power gain drops 1dB below its ideal curve as shown in Figure 2-2. Input signals beyond this point experience clipping at the output of the circuit.

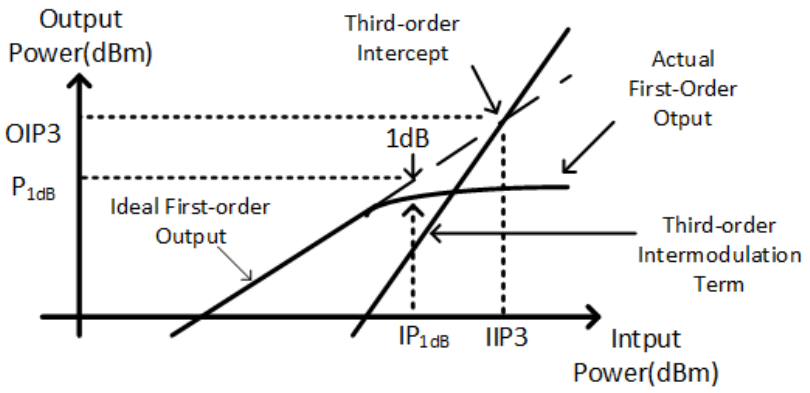


Figure 2-2: Illustration of P_{1dB} and *IP3* [7]

2.1.3.2 The 3rd Order Intercept Point

Another case that can cause signal distortion is the mixing(multiplication) of the input signal with it's harmonics, resulting from the nonlinear nature of the system. This mixing(multiplication) produces output terms known as *inter-modulation products* (IMP). Given a non-linear system as shown in Figure 2-3, when a transient signal $x(t)$

is applied at the input, there is a resultant output signal given by:

$$y(t) = \alpha_0 + \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \qquad 2-4$$

Where α_0 represents the DC component, α_1 represents the small signal gain of the sytem and α_2 and α_3 represent the co-efficients of the higher order terms.

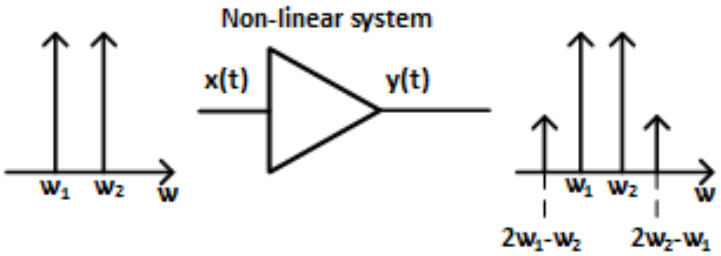


Figure 2-3: Intermodulation in a non-linear system[7]

Assuming that two signals with different frequencies are applied to the non-linear system (Fig. 2-3), the output exhibits some unwanted components that are not harmonics of the input frequencies. The frequencies of these unwanted components may be very close to that of the desired signals and hence cause signal distortion. Assume that the input signal is $x(t) = A_1 cos\omega_1 t + A_2 cos\omega_2 t$, then the output through the system will be :

$$y(t) = \propto_1 (A_1 cos\omega_1 t + A_2 cos\omega_2 t) + \propto_2 (A_1 cos\omega_1 t + A_2 cos\omega_2 t)^2 \qquad 2-5$$
$$+ \propto_3 (A_1 cos\omega_1 t + A_2 cos\omega_2 t)^3$$

Expanding the right side and discarding dc terms and harmonics, we obtain the following intermodulation products:

$$w = w_1 \pm w_2 : \propto_1 A_1 A_2 \cos(w_1 + w_2)\, t + \propto_2 A_1 A_2 \cos(w_1 - w_2)\, t \qquad 2-6$$

$$= 2w_1 \pm w_2 : \frac{3\propto_3 {A_1}^2 A_2}{4} \cos(2w_1 + w_2)\, t + \frac{3\propto_3 {A_1}^2 A_2}{4} \cos(2w_1 - w_2)\, t \qquad 2-7$$

$$= 2w_2 \pm w_1 : \frac{3 \propto_3 {A_2}^2 A_1}{4} \cos(2w_2 + w_1)\, t + \frac{3 \propto_3 {A_2}^2 A_1}{4} \cos(2w_2 - w_1)\, t \qquad 2-8$$

and these fundamental components:

$$w = w_1 w_2 : \left(\propto_1 A_1 + \frac{3}{4} \propto_3 {A_1}^2 A_2\right) cos w_1 t + \qquad 2-9$$

$$\left(\propto_1 A_2 + \frac{3}{4} \propto_3 {A_2}^3 + \frac{3}{2} \propto_3 {A_2}^2 A_1\right) \cos w_2 t$$

As illustrated in Figure 2-3, if the difference between w_1 and w_2 is small, the third-order IM products at $2w_1 \pm w_2$ and $2w_2 \pm w_1$ appear in the vicinity of w_1 and w_2, thus revealing nonlinearities.

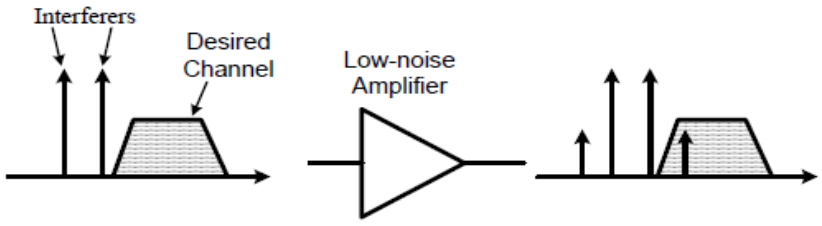


Figure 2-4: Corruption of a signal due to intermodulation between two interferers[7]

Intermodulation is a troublesome phenomenon in RF system. As shown in Figure 2-4 , if a small amplitude signal in the presence of two strong interferers experiences third-order non-linearity, then one of the IM products falls in the band of interest, corrupting the desired component. The "third intercept point" (*IP3)* is used to characterize the

corruption of signals due to third-order intermodulation of two nearby interferers. It is measured by a two-tone test where $A_1 = A_2 = A$. The input signal level, where the power of the third-order IM product equals to that of the fundamental is defined as "two-tone input-referred third-order intercept point" (IIP3). And the corresponding output level is called the "output third-order intercept point" (*OIP3*). *IIP3* [7] can be calculated as:

$$IIP3 = 20log_{10}\sqrt{\frac{4}{3}|\frac{\propto_1}{\propto_3}|} \qquad 2-10$$

IIP3 [7] can be given by

$$IIP3 > \frac{3P_{int} - P_{sig} + SNR_{min} + margins}{2} \qquad 2-11$$

where P_{int} is the power of two interferers and P_{sig} is the power of the desired signal.

For a cascade of N-stage network, the *IIP3* of the system, $IIP3_{tot}$, can be expressed as [7]:

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_1} + \frac{A_1}{IIP3_2} + \frac{A_1A_2}{IIP3_3} + \cdots + \frac{A_1A_2 \ldots A_{N-1}}{IIP3_N} \qquad 2-12$$

where $IIP3_i$ and A_i (i=1,2,…N) are the *IIP3* and the available power gain of the i^{th} stage network respectively. Equation 2-12 suggests that, for the $IIP3_3$ calculation, the last stage contributes the most to the distortion of the system. Thus it is important to end the system with a high linearity block.

2.1.4 Dynamic Range

Dynamic range (DR) generally describes the absolute minimum and absolute maximum input signal amplitude that can be tolerated by a system. The LNA should possess large dynamic range (*DR*) to ensure that it remains linear when receiving weak signals in the presence of strong interferers. The minimum detectable signal that can be

tolerated is referred to the sensitivity. The upper limit is the maximum input power that the circuit can handle without entering into saturation.

2.1.5 Impedance Matching

An essential concept in RF circuits is impedance matching. Input matching is required to deliver maximum power from the antenna to the LNA. The antenna characteristic impedance is normally 50 Ohms hence similar impedance is required at the input port of the LNA for maximum power transfer. It is necessary to introduce the concept of the voltage standing wave ratio(VSWR) in order to quantify the extent of impedance matching:

$$VSWR = \frac{1 + |\Gamma|}{1 - |\Gamma|} \qquad 2 - 13$$

where Γ is the reflection coefficient defined as :

$$\Gamma = \left|\frac{Z - Z_O}{Z + Z_O}\right| \qquad 2 - 14$$

Z is the actual input impedance whiles Z_O is the characteristic impedance of the source, usually given as 50Ω. Γ is usually in the range of $0 \leq \Gamma \leq 1$ from perfect matching condition($Z = Z_O$) to short circuit($Z_O = 0$) or open circuit($Z_O = infinity$) conditions.

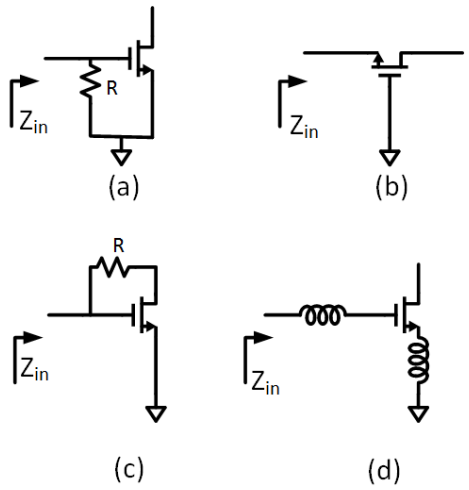


Figure 2-5: Different Input matching topologies (a) resistive termination (b)$1/g_m$ termination (c)shunt feedback (d) inductive degeneration [7]

Several input matching schemes required to generate 50Ω impedance at the input port of the LNA exist as shown in Figure 2-5. The simplest scheme to achieve matching over wide frequency range is the use of the resistive termination illustrated in Figure 2-5(a). This scheme however suffers from a relatively high NF due to the thermal noise of the resistive termination. Another approach to input matching the use of the source of a MOS transistor as the input termination, as illustrated in Figure 2-5 (b). This is used normally in common-gate LNA architectures. In this case, the impedance looking into the source terminal of active device is $1/g_m$. To ensure input matching, it is necessary to provide proper device baising and sizing to make sure $1/g_m = 50$. This scheme still suffers from the high NF issue. Shunt feedback[7] (Fig. 2-5 (c)) is another method for achieving input matching. This type employs negative feedback to generate the 50Ω impedance at the input port.

The thermal noise of the feedback resistor impacts on the NF of the amplifier. To annul the impact of real resistors on the NF of LNAs, a widely used approach known as inductively degenerated LNA(Fig. 2-5 (d)) scheme is employed. Considering the Figure 2-6 which shows the small signal model of an inductively degenerated LNA, the KVL at the input port is obtained as :

$$V_{in}(\omega) = i_{in}(\omega)\left(j(L_g + L_S)\omega - \frac{j}{C_{gs}\omega}\right) + g_m v_{gs}(jL_S\omega) \qquad 2-15$$

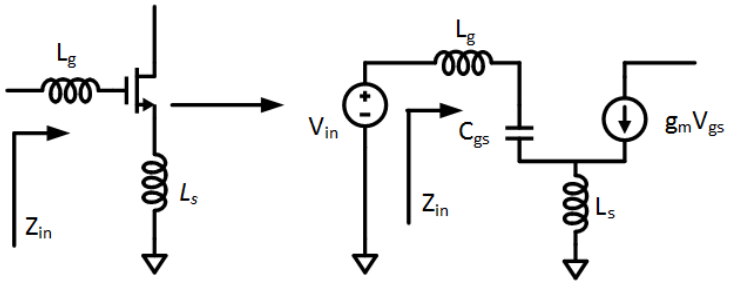


Figure 2-6: Small signal model of inductively degenerated LNA[7]

Which yields $$Z_{in}(\omega) = \frac{V_{in}(\omega)}{i_{in}(\omega)} = \frac{1}{jC_{gs}\omega} + j(L_S + L_g)\omega + \omega_t L_S \qquad 2-16$$

where $\omega_t = g_m/C_{gs}$ is the transit frequency of the input transistor. The last term is a real impedance with no explicit resistor. Thus the thermal noise due to a resistor is avoided. A very small value of source inductance is needed to satisfy the input matching, i.e. $\omega_t L_S = 50\Omega$ and this can be realized using bond-wires. It can be observed from equation 2-16 that,

the impedance matching is only obtainable at a single frequency, the resonant frequency of the series inductor and gate-source capacitance:

$$\omega_O = \frac{1}{\sqrt{(L_g + L_S)C_{gs}}} \qquad 2-17$$

This architecture finds many applications in the industry due to the superior performance in terms of noise .

2.1.6 S-Parameters

Scattering parameters (S-parameters) can be used to quantify the degree of input/output impedance matching. S-parameters is normally applied in radio frequency and microwave design to describe the behavior of a linear system in terms of the reflected and transmitted voltage with reference to an input voltage. Figure 2-7 shows a two-port network, where a_1 and a_2 are the incident waves; b_1 and b_2 are reflected waves[9]. Their relation is expressed as:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} = [S] \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \qquad 2-18$$

The matrix [S] is called scattering matrix, where S_{11} is the input reflection coefficient, S_{12} is the reverse transmission coefficient, S_{21} is the forward transmission coefficient, and S_{22} is the output reflection coefficient. They can be measured according to Figure 2-8 and equations (2-19a)-(2-19d):

$$S_{11} = \frac{b_1}{a_1}|_{a_2=0} = \text{input reflection coefficient with matched output port} \qquad 2-19a$$

$$S_{12} = \frac{b_1}{a_2}|_{a_1=0} = \text{reverse transmission coefficient with matched input port} \qquad 2-19b$$

$S_{21} = \frac{b_2}{a_1}|_{a_2=0}$ =forward transmission coefficient with matched output port 2 – 19 c

$S_{22} = \frac{b_2}{a_2}|_{a_1=0}$ = output reflection coefficient with matched input port 2 – 19 d

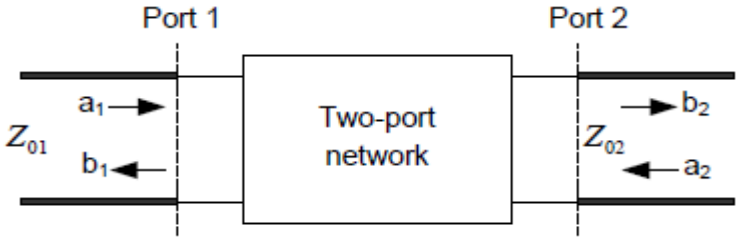


Figure 2-7: Two-port network [9]

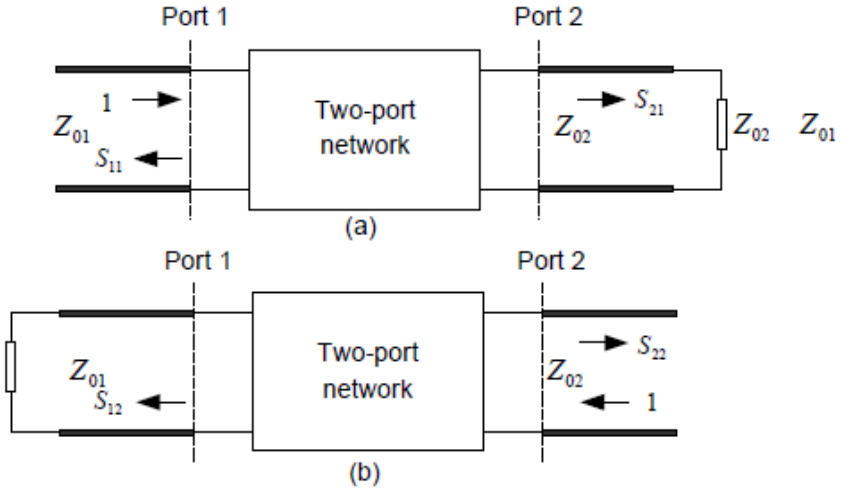


Figure 2-8: Measurement of s-parameters using (a) matched output port, (b) matched input port [9]

For the amplifier design, S_{11} and S_{22} denote how well the input and output impedances are matched to the reference impedance respectively. S_{21} measures the amplification gain of

the amplifier. S_{12} represents the isolation between output and input ports. S-parameters can be converted to Y or Z-parameters or other network representations. Detailed formula can be found in most microwave textbooks [9],[7],[10].

2.1.7 Stability

Stability is another key factor in LNA design. Stability of an LNA measures the tendency of the amplifier to oscillate. A properly designed LNA is the one which remains stable for all source and load impedances at all frequencies. If the LNA oscillates at any other frequency than the frequency of interest, it becomes highly nonlinear and it's gain is very heavily compressed [7]. A parameter used to characterize the stability of circuits is the "Stern stability factor" defined as

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{21}||S_{12}|} \qquad 2-20$$

where $= S_{11}S_{22} - S_{12}S_{21}$. If $K > 1$ and Δ<1, then the circuit is unconditionally stable, i.e., it does not oscillate with any combination of source and load impedances.

LNAs may become unstable due to ground and supply parasitic inductances resulting from the packaging. For example, if the gate terminal of a common-gate transitor sees a large series inductance, the circuit may suffer from substantial feedback from the output to the input and become unstable at some frequency[7].

2.2 LNA Design and Architecture

This section highlights basic LNA design schemes and factors to be considered in LNA design. LNA topologies with their pros and cons will also be covered in this section.

The section concludes with literature review on various reconfigurable LNA architectures and then introducing the proposed reconfigurable LNA.

2.2.1 LNA Design Factors

The front-end of a typical RF transceiver consists of a receiver and a transmitter. For the transmitter path, the only existent signal is the desired RF signal. This makes the design of the transmit path simpler compared to the receive path because issues such as noise, interference rejection and selectivity can be relaxed. However, for the receiver, the desired RF signal is weak and surrounded by noise and interferers. Hence, the design of the receiving path involves many issues and trade-offs. LNA is the first active block in the receiving chain and it's NF and gain play an important role in the overall performance of the receiver. In reality, the incoming RF signals are considerably small, which leads to a small SNR. Any additional noise will further degrade the overall SNR and hence the receiver performance. Because LNA is the first gain stage along the receiver chain, its NF needs to be very small enough to keep the overall system's NF low. Low NF of the LNA can be achieved with noise matching techniques, proper transistor sizing and biasing and selection of a proper LNA topology [7]. In addition, the gain of the LNA needs to be high enough to mask the noise contribution from the subsequent mixer and other stages, but not too high to degrade the overall system's linearity. This elaborates on the trade-off between LNAs gain and linearity.Impedance matching is another factor to be considered in designing LNAs. It is required to enhance maximum power transfer to the LNA from the preceding block(i.e. antenna or filter) . The LNA must be impedance matched to the output impdenace of the preceding filter and should be able to drive the input of the block

at it's output(i.e normally the mixer). In the case of the SDR, the LNA would be required to have sufficient output power to drive the input of the ADC. Matching is generally not required at the output of the LNA for integrated receivers as the blocks following the LNA are integrated together with the LNA on the same chip. Hence the distance between the devices relative to the wavelength of the RF signal on the chip is insignificant. Another factor to be considered is the chip size. The LNA is required to provide input matching with minimum discrete componenets. A fully-integrated LNA is the best option. Finally, power consumption is a concern, especially for portable devices. In summary, the important features in the design of an LNA in recent receiver architecture are: NF, gain, input impedance matching, power consumption, reverse isolation, chip size and linearity[7].

2.2.2 Performance Trade-offs in LNA design

Different applications require different requirement for LNA performance. Hence, it is important to understand the trade-offs involved in LNA design. The three important trade-offs are gain vs. power efficiency, linearity vs. drain-source dc current and LNA's gain vs. receiver's dynamic range.

2.2.2.1 Gain vs Power Efficiency

An amplifier's gain is proportional to the transconductance, g_m, of its input transistor. High g_m is desirable for high gain. Using the standard saturation region dc current equations for long channel devices, we can approximate:

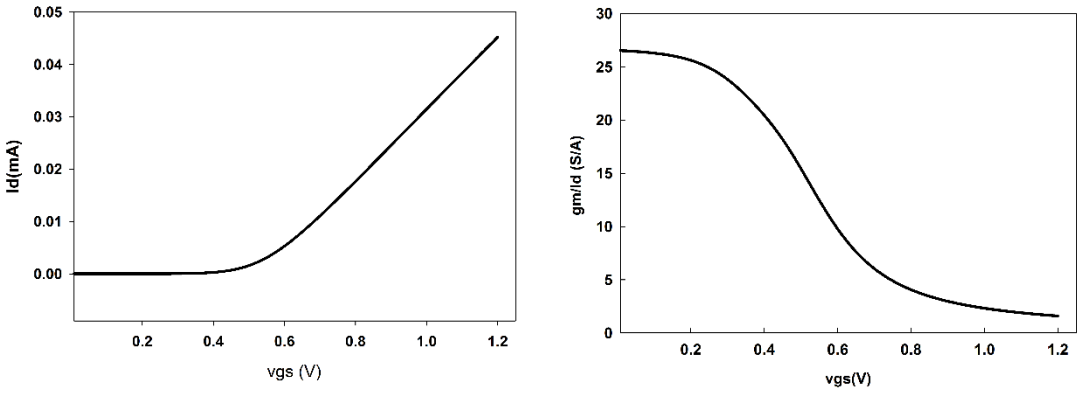
$$I_{DS} = \frac{1}{2} K \frac{W}{L} (V_{GS} - V_t)^2 \qquad 2-21$$

$$g_m = \sqrt{K\frac{W}{L}I_{DS}} \qquad 2-22$$

$$\frac{g_m}{I_{DS}} = \frac{2}{(V_{GS}-V_t)} \qquad 2-23$$

Where K is a technology dependent constant, W and L are the width and length of the transistor, I_{DS} is the drain-source dc current, V_{GS} is the gate-source voltage and V_t is the threshold voltage. From equations (2-21) and (2-23), we notice that I_{DS} is directly proportional to $(V_{GS}-V_t)^2$, while g_m/I_{DS} is inversely proportional to $(V_{GS}-V_t)$.

Figure 2-9 shows the I_{DS} and g_m/I_{DS} ratio vs. V_{GS} for IBM 0.18um CMOS technology.



(a) (b)

Figure 2-9: (a) Variation of Id with vgs in IBM 0.18um CMOS (b) variation of gm/Id with vgs in IBM 0.18um CMOS technology

The analysis and simulation results (Fig. 2-9) clearly demonstatre the trade-off between gain and power efficiency. High gain but low power efficiency is achieved at high V_{GS} while high power efficiency but low gain is achieved at low V_{GS} .

2.2.2.2 Linearity vs Current

Assume the main nonlinearity of a MOS transistor arises from transconductance nonlinearity [7].The *IIP3* of an LNA can be calculated as:

$$IIP3 = 20\ log_{10}\sqrt{\frac{4}{3}\left|\frac{g_1}{g_3}\right|} \qquad 2-24$$

where g_1 and g_3 are the 1st and 3rd order coefficient of the input transistor obtained by taking the derivative of the drain-source dc current I_{DS} with respect to the gate-to-source voltage V_{GS} at the dc bias point:

$$g_1 = \frac{\partial I_{DS}}{\partial V_{GS}}, \qquad g_3 = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial^3 {V_{GS}}^3} \qquad 2-25$$

W fixed the input transistor's drain source voltage V_{DS} and swept the gate source voltage V_{GS}. The first three derivatives of the drain source current I_{DS} with respect to V_{GS} are plotted in Figure 2-10. For high *IIP3,* it is desired to bias the transistor near the spot where g_3 = 0. Outside the high linear region, the linearity improves as Vgs or Ids increases. This highlights the trade-off between linearity and current . High linearity means high current consumption and vice versa. It is hence the task of the circuit designer to choose a bias point such that high IIP3 is achieved while using as little power as possible.

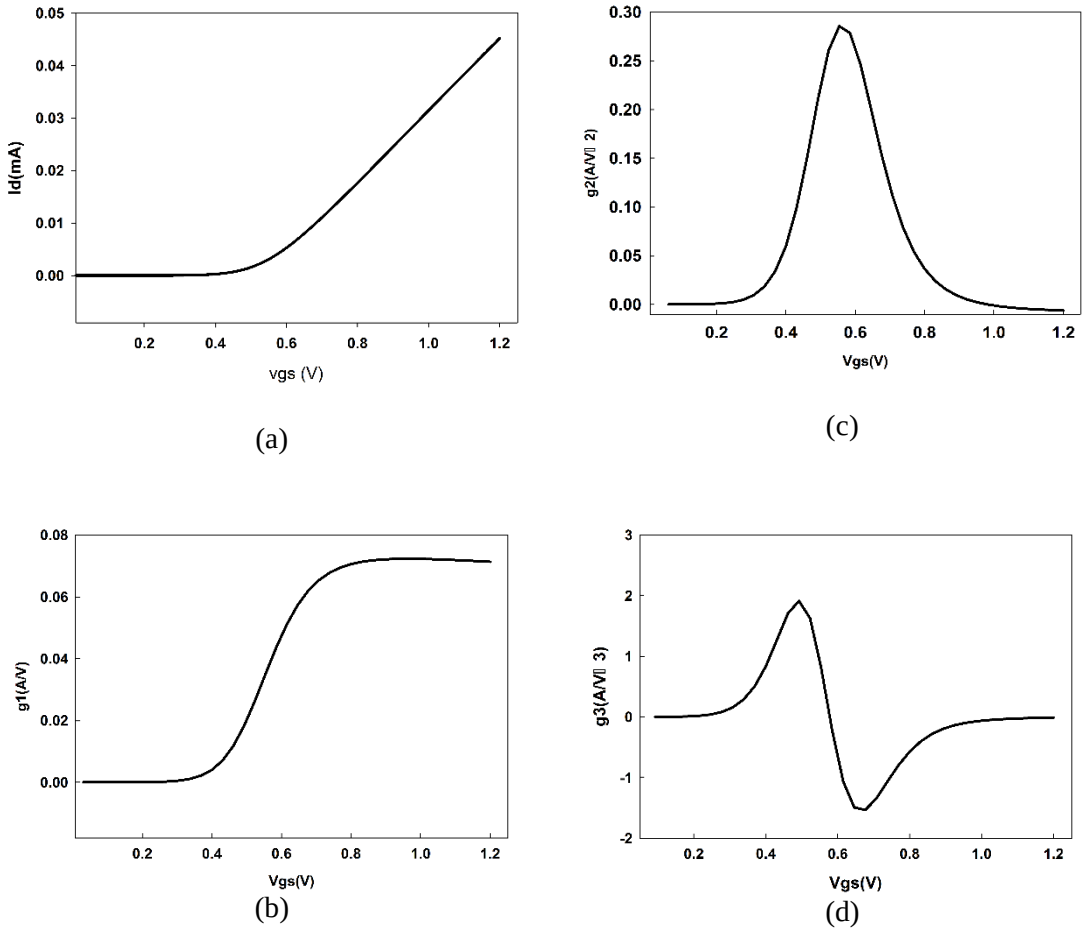


Figure 2-10: (a) Id versus vgs for IBM 0.18um NFET (b) g1 versus vgs for IBM 0.18um NFET (c) g2 versus vgs for IBM 0.18um NFET (d) g3 versus vgs for IBM 0.18um NFET

2.2.2.3 LNA's Gain vs Receiver's Dynamic Range

The trade-off between LNA gain and receiver dynamic range can be explained using these two equations:

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_{p1}} + \frac{F_3 - 1}{A_{p1}A_{p2}} + \cdots + \frac{F_N - 1}{A_{p1}A_{p2} \ldots A_{p(N-1)}} \qquad 2-26$$

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \cdots + \frac{G_1 G_2 \ldots G_{N-1}}{IIP3_N} \qquad 2-27$$

As shown in equation (2-26), high LNA gain is required so that the noise added by elements in the receiver lineup following the LNA are minimized. However, equation (2-27) shows that the receiver's linearity decreases as LNA's gain increases.

2.3 LNA Topologies

From the previous section, it is known that input impedance matching to 50 Ω is one of the common goals in LNA design. Input matching architectures in LNAs can be classified into four types: CS with resistive termination, CG, CS with shunt feedback and CS with inductive source degeneration. Each of these architectures can be implemented in single-ended or differential form.

2.3.1 Common-Source Stage with Source Inductive Degeneration LNA

Figure 2-11 shows the architecture which employs source inductive degeneration to generate a real term in the input impedance. The input impedance [7] is :

$$Z_{in} \approx j\left(\omega L_g + \omega L_S - \frac{1}{\omega C_{gs}}\right) + \frac{g_m L_S}{C_{gs}} \qquad 2-28$$

The input impedance has a resistive term $g_m L_S / C_{gs}$, which is directly proportional to the inductance value. Whatever value this resistive term is, it does not generate thermal noise like an ordinary resistor does, because a pure reactance is noiseless [7].

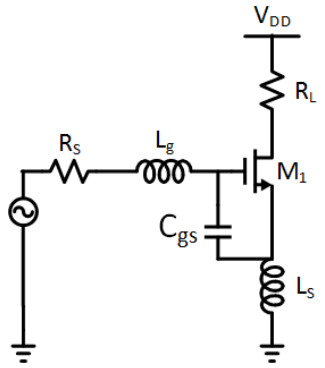


Figure 2-11: Common-source input stage with source inductive degeneration[7]

Therefore, this structure can be exploited to provide the specified input impedance without degrading the noise performance of the amplifier. To get the 50 Ω input impedance, let the real part $g_m L_S/C_{gs}$, of equation (2-28) equal to 50 Ω and the imaginary part [$[\omega L_g + \omega L_S - 1/(\omega C_{gs})]$ be zero at the frequency of interest. The resonance frequency is therefore :

$$\omega_O = \frac{1}{\sqrt{(L_g + L_S)C_{gs}}} \qquad 2-29$$

The noise factor can be simplified as [7] :

$$F = 1 + 2.4\frac{\gamma}{\alpha}\frac{\omega_O}{\omega_T} \qquad 2-30$$

Where $\omega_T = g_m/C_{gs}$ is the unity current gain frequency.

2.3.1 Common-Source Stage with Resistive Termination LNA

This technique uses resistive termination in the input port to provide 50 Ω input impedance. As indicated in Figure 2-12, a 50 Ω resistor, R_1, is placed in parallel with the

input, to realize input matching for the LNA. However, this termination generates noise.

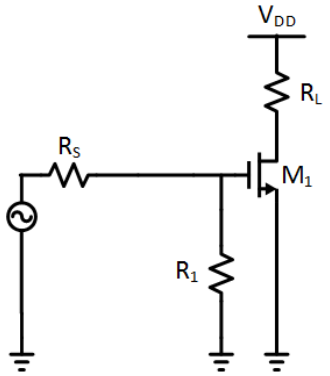


Figure 2-12: Common-source with resistive termination[7]

The noise factor[7] of the circuit can be found as:

$$F = \frac{4(R_s//R_1)}{R_s} + \frac{4\gamma}{\alpha g_m R_s} = 2 + 4\frac{\gamma}{\alpha}\frac{1}{g_m R_s} \qquad 2-31$$

Where g_m is the transconductance of the input device, and α is the ratio of g_m to the zero V_{DS} channel conductance. The NF ($10log_{10}F$) of this structure is very high. The NF degradation is due to two reasons. First, the added resistor R_1 contributes as much noise as the source resistor R_s does. It results in a factor of 2 in the first term of equation (2-31). Secondly, the input is attenuated, leading to a factor of 4 in the second term of equation (2-31) [7]. The poor NF makes this architecture unattractive for applications where a low noise as well as good input matching is desired.

2.3.2 Common-Gate LNA

Figure 2-13 shows the simplified CGLNA. The CGLNA is noted for wideband

appplications [7] . The input impedance and voltage gain of a CGLNA are :

$$Z_{in} = \frac{1}{g_m} \qquad 2-32$$

$$A = g_m R_L \qquad 2-33$$

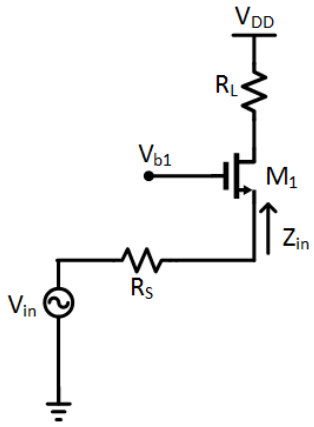


Figure 2-13: Common gate LNA[7]

To realize the input matching, its g_m value is fixed at $1/R_S$. As a result, only the load impedance R_L remains as a design variable. Moreover, due to the input matching constraint, the transconductance of the input transistor cannot be arbitrarily high, thus imposing a lower bound on the noise factot. Through derivation, the total noise factor [7] of the CGLNA can be simplified as :

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_S} \qquad 2-34$$

When the input is matched, noise factor simply becomes $1 + \gamma/\alpha$. This noise factor is quite reasonable and acceptable. However, it is important to note that other noise sources

such as gate induced noise and substrate noise can degrade the performance substantially. Furthermore, the load as well as the biasing circuits can generate additional noise.

2.3.3 Common-Source Stage with Shunt Feedback LNA

Figure 2-14 illustrates another topology, which uses the resistive shunt feedback to set the 50 Ω input impedance of the LNA.

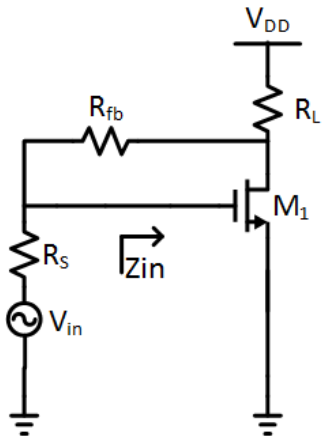


Figure 2-14: Common-source input stage with shunt feedback[7]

The input impedance [7] can be expressed as:

$$Z_{in} = R_{fb}/(1 + |A_V|) \qquad 2-35$$

Where R_{fb} is the feedback resistor and A_V is the corresponding voltage gain which equals to $[1 - g_m(R_L//R_{fb})]$. The noise factor[7] for this configuration can be expressed as follows:

$$F = 1 + \left(\frac{G_S + G_{fb}}{g_m - G_{fb}}\right)^2 R_S(G_L + \gamma g_{d0}) + \left(\frac{G_S + g_m}{g_m - G_{fb}}\right)^2 R_S G_{fb} \qquad 2-36$$

Where g_{d0} is the zero V_{DS} channel conductance, G_S , G_{fb} and G_L is the conductance of the resistors R_s, R_{fb} and R_L respectively. This topology is commonly used for wideband applications. Compared to the conventional CGLNA, it normally can achieve lower NF. However, it still has several disadvantages. First, the input impedance Z_{in} depends on R_{fb} and A_V. Therefore, it is sensitive to process variation. Second, the feedback signal may contain susbstantial noise, thus raising the NF to an unacceptable level. Finally, the total phase shift around the loop may create instability for certain source and load impedances.

2.3.4 Tuning Techniques of LNA's Load

The tuning techniques applied to the load at the device output also affects the performance of the LNA besides the input matching network. Three types of tuning loads commonly used are : resistive load, passive LC load and active inductor and passive capacitor load. As shown in Figure 2-15, an ordinary resistor R_L is used as the LNA output load. Sometimes, a resistor R_L is replaced by a MOS transistor operating in linear region. This method produces wideband frequency response and can implemented easily. However, it is not suitable for low noise applications, because the resistor generates thermal noise. Morever, the use of resistive load will reduce the voltage headroom across the transistor significantly. This will result in poor linearity performance if low supply voltage is required.

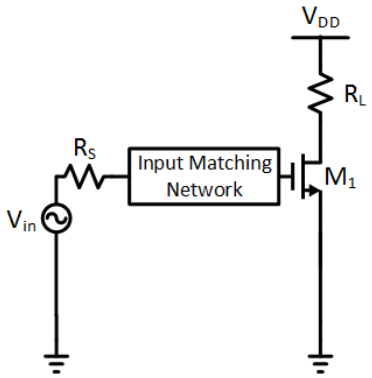


Figure 2-15: LNA with resistive load[7]

Figure 2-16 shows another type of load. It is the most widely used type in LNA design . It is used extensively in communication circuits to provide selective amplification of wanted signals and to filter out unwanted signals to some extent. The RLC network has an admittance of:

$$Y = j\left(\omega C_L - \frac{1}{\omega L_L}\right) + \frac{1}{R_p} \qquad 2-37$$

where C_L equals to the total parasitic capacitances at the drain terminal of M_1 plus the capacitance of next stage, R_p is the equivalent parallel resistance of L_L. When the inductor L_L and capacitor C_L are designed to resonate at a selected frequency, the impedance is purely real and at its maximum. The higher the quality factor of L_L is, the larger R_p is, and the higher the voltage gain is. This type of tuning load is very suitable for narrow-band applications. It allows LNAs to achieve substantial gain at relatively high frequencies with low power consumption.

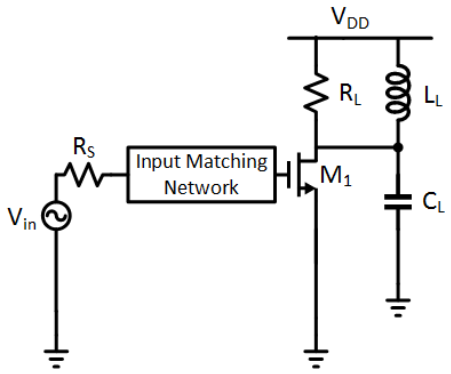


Figure 2-16: LNA with passive LC tuning range[7]

In practice, the silicon-based on-chip spiral inductor does not have a large quality factor Q. Hence, R_p is not very high. R_p is normally less than 1 kΩ for most of the cases. There are several ways to increase R_p. One way is to use high-Q off-chip inductors by sacrificing the market demands for highly-integrated products. Another way is through process modification to obtain a higher inductor Q. For example, a higher Q can be achieved by removing the inductor's underlying silicon substrate or by using a thick top metal [7]. The third way is to use the Q-enhanced technique [7], as illustrated in Figure 2-17.

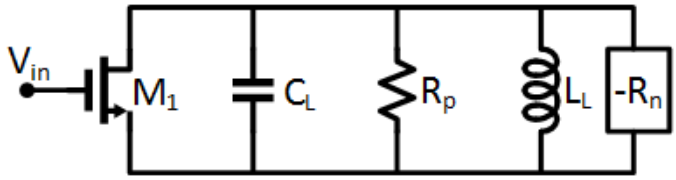


Figure 2-17: Q-enhancement technique

The basic principle of the Q-enhancement technique is to add a negative conductance to the LC resonator so that the resistive loss of the inductor can be compensated. Without the negative resistance $-R_n$, Q can be expressed as $Q = (\sqrt{C_L/L_L})R_p$ [11] . The above equation indicates that Q is drastically reduced because of the ohmic loss in the inductor. To reduce the effect of R_p on the Q, a negative resistance $-R_n$ is employed to compensate the loss in the inductor. Thus the Q of the tuned circuit increases to $Q = (\sqrt{C_L/L})\, R_P R_n/(R_n - R_p)$. With this method, the achieved Q can be 20 or even higher.

Due to the limitation of spiral inductors, for example, large chip area or parasitic capacitance and resistance loss, active inductors that can be implemented with a reasonable physical size offer a good alternative compared to its passive equivalent [12]. Traditional active inductors are typically implemented by using high gain operational amplifiers with negative feedback, and are unsuitable for operating frequencies up to gigahertz. Another type of active inductor is implemented by exploiting the parasitic capacitance of the transistors to generate the required poles and zeros[13] as shown in Figure 2-18.

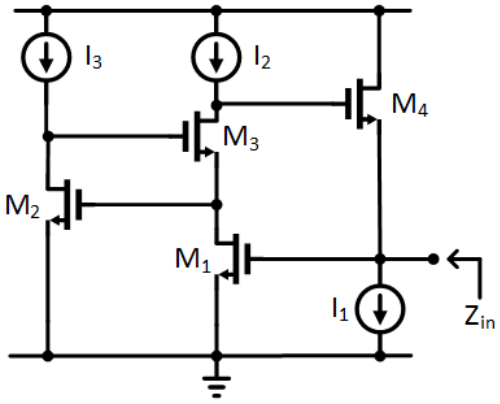


Figure 2-18: Active inductor

2.4 Multiband LNA Architecture Review

The basic LNA topologies have been discussed in the previous sections. This section highlights the generic schemes of implementing multiband LNAs. There are basically four major approaches regarding multistandard LNAs. These are parallel narrow-band LNAs, wideband LNAs, concurrent LNAs and narrow-band frequency reconfigurable LNAs [3].

2.4.1 Parallel LNAs

To implement multistandard LNA, the simplest approach would be having a specific signal path for each frequency band of interest. The most straightforward way to implement the LNA for a multi-band receiver would be to have a dedicated signal path for each frequency band of interest. This is a common scheme in single-chip dual-band radios [14],[15]. One of the paths is selected based on the band of interest. This approach requires a large chip area to accommodate multiple standards.

2.4.2 Wideband LNAs

Another approach to multistandard LNAs is the use of a wideband LNA [16],[17],[18]. The wideband LNAs have continuous multiple pass band allowing signals at broad range of frequencies. These LNAs normally have resistive loads to provide wideband response. This approach has the disadvantage of amplifying blockers at different frequencies together with the desired RF signal. These amplified interferers can desensitize the receiver.

2.4.3 Concurrent LNAs

Multistandard LNAs can be achieved by using concurrent multi-band LNAs [19], [20],[21]. These LNAs have multiple pass bands separated by notches. Thus, only signals from select bands are allowed to pass through rather than a wide and continuous range of frequencies as in wideband LNAs. Still, a spur in one pass-band can corrupt signals in another band. In order to eliminate the effects of such spurs, radio architectures typically require that the LNA has high linearity [22]. However, the major drawback of concurrent LNAs can be understood by looking at the reported implementations. These LNAs have concurrent multi-band filters at the input and the output. The complexity of these filters increases with the number of the pass-bands. It means that the number of passives and thus the LNAs size increases with the number of pass-bands thus increasing the chip size. Additionally, in order to get an admissible quality-factor(Q) for the filters, sometimes high Q off-chip passives have to be used which further increases the cost and eliminates the possibility of monolithic integration. Moreover, concurrent LNAs might not be suitable for use in SDRs, where the radio should be capable of operating at any frequency over a

wide continuous spectrum. Hence, a narrow-band LNA whose center frequency can be dynamically changed without increasing the number of area expensive passives, would be even better than a concurrent multi-band LNA. This way, there won't be the problem of out-of-band spurs desensitizing the receiver while retaining the capability to cover a wide and continuous frequency range.

2.4.4 Narrow-band Reconfigurable LNAs

A frequency reconfigurable narrow-band LNA has characteristics of tuned amplifier but its frequency of operation can be dynamically changed by altering the characteristics of one of its components. The narrow-band reconfigurable LNA can be realized with the tunable multitap inductor [23] or switched inductors [24] or switched capacitors [25] or using feedback [26].

2.5 Reconfigurable LNA Literature Review

The previous section highlighted the various LNA topologies for multistandard systems. This section discusses some previous works on reconfigurable LNA topologies using shunt-feedback method and other approaches to achieve reconfigurability. The various works have been grouped into two depending on whether the results presented are based on simulation or measurement; (a) to (f) have results based on simulation, (g) to (k) have been fabricated and have measurement results.

a) Low power and high linear reconfigurable CMOS LNA for multi-standard wireless applications [27]

This work describes an LNA with inductively degenerated common source gain stage (Fig. 2-19). The frequency reconfigurability is achieved by adding a series of MOS-

varactors and capacitors to both input and output of the LNA.. Continuosly tuning the voltage applied to the varactors adjusts the capacitance values at the input and output in order to shift from one frequency to another. This work also employs a post-linearization technique to improve linearity. This design is implemented in 0.18um CMOS technology and achieves a power gain of 21-23.5dB, a noise figure of 2.45-2.7dB, an IIP3 of -3 to1.45dBm and an S11 less than -12dB for frequency variation 1.9-2.4 GHz. The total power consumption is 10.9mW at a supply of 1.8V. The drawback of this topology comes from the poor quality factor associated with MOS varactors[7] which brings about tradeoff between power consumption and gain. This is because, to compensate for loss of gain due to lower quality factor of the LC tank, the current has to be increased. The other drawback is that it covers a narrow tuning range.

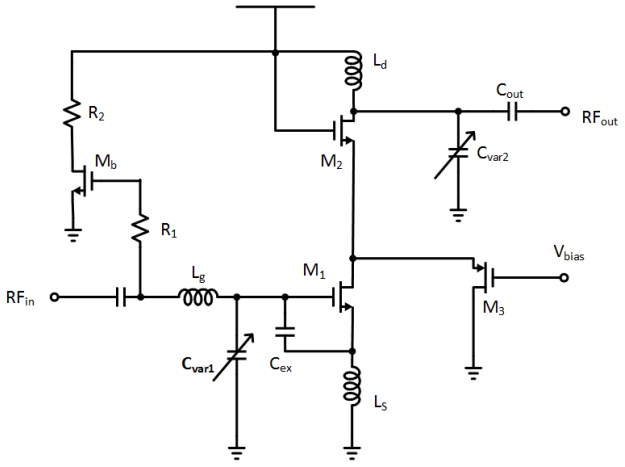


Figure 2-19: Schematic of reconfigurable LNA[27]

b) A compact dualband LNA using self-matched capacitor [28]

This work describes an LNA with self-matched capacitor for simultaneous input and noise matching (Fig. 2-20). The self-matched capacitor is obtained by changing the position of conventional extra capacitor such that the capacitor and the gate inductor are now in parallel [28]. Switched inductor and switched capacitor are used for frequency selection. High frequency mode is selected by turning on the matching transistor(M_S) and vice versa. The LNA is designed in 0.18 um CMOS process for 2.4 GHz and 5 GHz bands. The LNA achieves a gain of 15dB/15dB, a noise figure of 2.3dB/2.4dB, an IIP3 of -3dBm/-6.7dBm, an S11 of -30dB/-20dB and power consumption of 9mW/5.04mW for frequencies 2.4GHz/5GHz. This work used a supply of 1.2V and covers an area of 0.49mm^2.

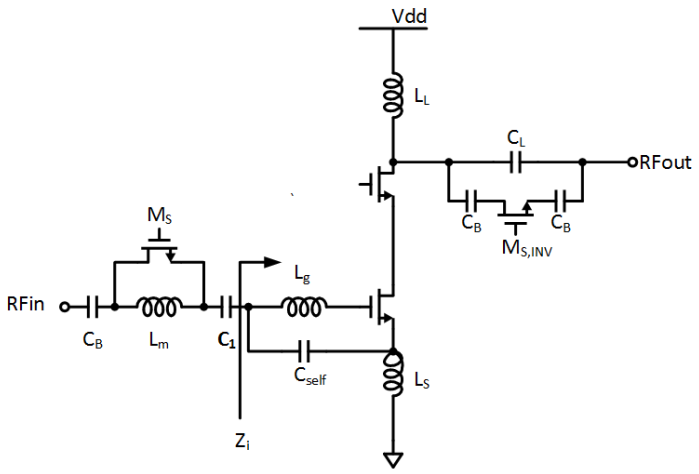


Figure 2-20: Self-matched capacitor LNA[28]

c) A triple-mode LNA enhanced by dual feedback loops for multistandard receivers [29]

This work describes a reconfigurable LNA area-optimized for DCS1800, UMTS and IEEE 802.11 b/g standards (Fig. 2-21). Single-stage common gate LNA architecture is used in this design. This work employs two feedback loops; one loop makes use of the gain-boosted gm technique[30] to improve the NF by increasing the gm without increasing the LNA bias current and the other loop employs a voltage-voltage capacitive feedback technique to achieve input impedance matching by adjusting the capacitance, C_2. This work was designed in 0.18um CMOS technology achieves a gain of 9.8-10dB, NF of 2.0-2.25dB, S11 of -18db to -17dB and an IIP3 of 15dBm for frequency range 1.8-2.45GHz. The total power consumption of this LNA is 15mW at a supply of 1.5V. The drawback of this LNA comes from the complexity in the use of the on-chip transformer.

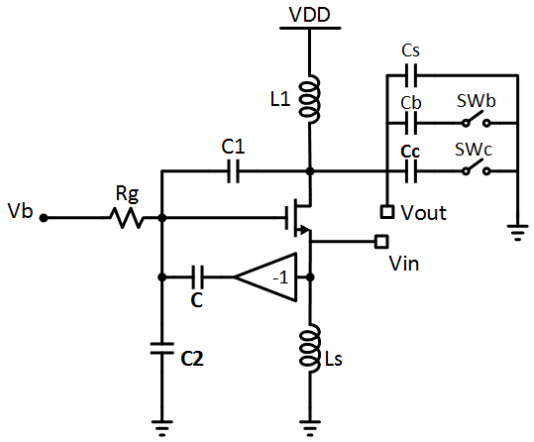


Figure 2-21: Common gate reconfigurable LNA[29]

d) A 0.18um CMOS reconfigurable multi-band multi-gain LNA [31]

This work describes an LNA made up of two stages. The first stage is a common gate amplifier. The second stage is a programmable frequency and gain selective amplifier (Fig. 2-22). The frequency selection is achieved by a multi-tapped inductor and a varactor at the load of the LNA. The gain selection is done by adding in parallel, transistors M2B and M2C by switching on or off, S5 and S6 respectively. The LNA operates at 900MHz, 1.5GHz and 2.4GHz. It exhibits a voltage gain of 15-20dB, NF of 1.9-4.5dB and approximately 30 mW power consumption with a 1.8 V power supply.

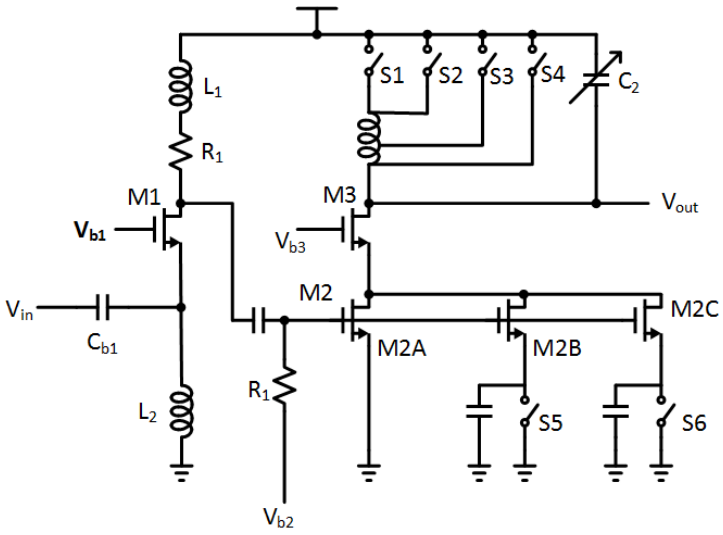


Figure 2-22: Multi-band LNA[31]

e) Reconfigurable multiband multimode LNA for LTE/GSM, Wimax, and IEEE 802.11 a/b/g/n [32].

This work describes an LNA with an inductively-degenerated common source gain stage consisting of four parallel CS FETs for adjustable gain and multiple selectable loads for various resonant frequencies. Input matching is achieved with three switchable series gate-inductors, which are in addition to the RF input bondwire (Fig. 2-23). This approach selects the inductance value by bypassing or not bypassing the three on-chip series gate inductors. This work is designed in 0.18um CMOS process and operates at 1.9GHz, 2.4GHz, 3.5GHz and 5.2GHz bands. The LNA achieves gain of 13-17dB, NF of 1.5-3.1dB, IIP3 of -17.5dBm and S11 of -14dB for the frequency range 1.9-5.2GHz. It consumes total power of 3-5.3mW at 1.5V supply for the same frequency range. It provides excellent input matching and good noise figure, however, the main disadvantage of this design is imposing large area requirements because of the number of inductors.

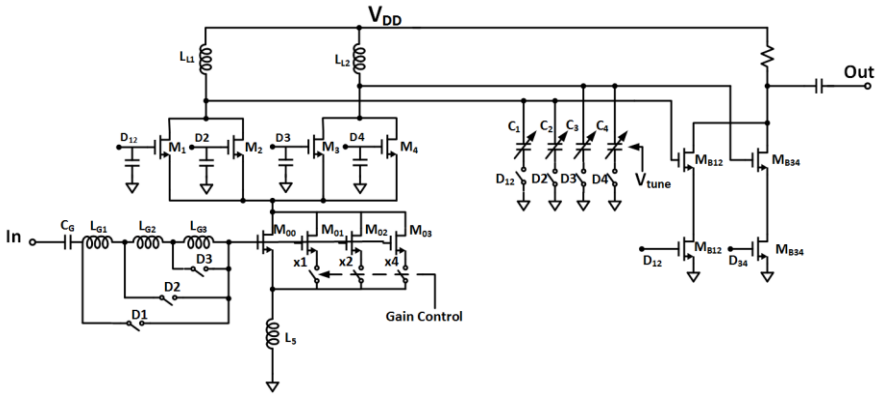


Figure 2-23: Reconfigurable multiband multimode LNA[32]

f) A highly reconfigurable signle-ended LNA for software defined radio applications [33]

This work describes a reconfigurable LNA with variable gain, bandwidth and center frequency. This amplifier employs a variable-bias active shunt feedback input matching, a switchable capacitive load, Q-enhancement circuit and a noise cancelling output stage(Fig. 2-24). The active shunt feedback circuit provides input matching with very low noise and high linearity. The switchable capacitive load is used to provide frequency tuning by switching on or off capacitors in a capacitor bank. The Q-enhancement circuit is a tunable negative resistance circuit that helps to boost the quality factor of the capacitor bank. The noise cancelling output stage consists of common-source transistor M_{13} and source follower M_{14}. Noise current generated in M_1's channel generates a noise voltage at the output of M_2, and a lesser noise voltage at the input due to the feedback action of Z_{fb}. Transistor M_{13} amplifies and inverts the input signal along with

this input noise voltage. The source of M_{14} follows the signal at the output of M_2 along with the output noise voltage. Signal amplified by M_{13} and M_{14} is in phase at their outputs, whereas the noise is out-of-phase. These inverse noise voltages sum at the V out node and subtract one another, while the signal sums in phase. Therefore, the noise cancelling stage helps to improve gain and reduce the noise figure. The active shunt feedback input matching concept is also employed in this thesis work. This work was implemented in 0.13um CMOS technology and operates from 2GHz to 5.7GHz. It achieves a gain of 13-14.7dB, NF of 2.9-7dB, IIP3 of -21.5dBm – -16.9dBm, S11 of -16dB – -10dB and a power consumption of 7.2-12.6mW at a supply of 1.2V for the frequency range 2-5.7GHz.

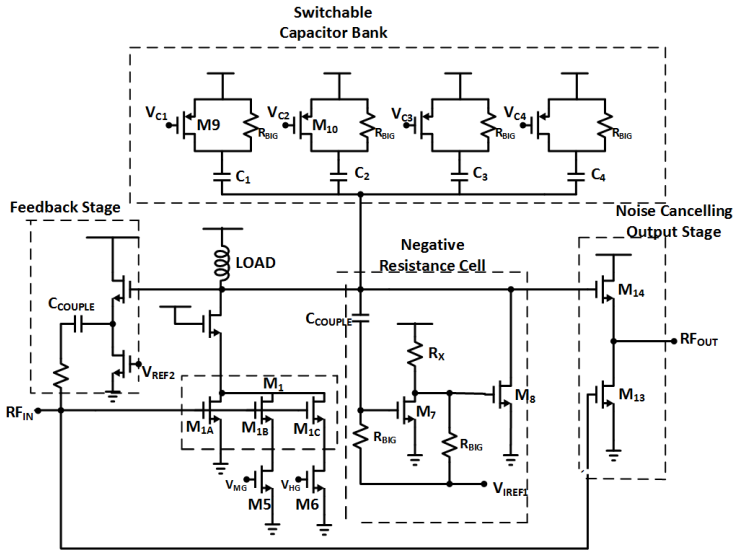


Figure 2-24: Single ended reconfigurable LNA[33]

g) A Dual-Band 2.45/6 GHz CMOS LNA utilizing a dual-resonant transformer-based matching network [34]

This work describes an LNA that uses a transformer-based matching network capable of simultaneously matching two different frequencies at the LNA input (Fig. 2-25). The band switching is achieved by switching a capacitor at the load. The LNA is fabricated in 0.13um CMOS process and is capable of operating at 2.45 GHz and 6 GHz. It achieves a gain of 9.4dB/18.9dB, noise figure of 2.8dB/3.8dB, an IIP3 of -4.3dBm/-5.6dBm, and S11 of -12.62dB/-21dB at frequencies 2.45GHz/6GHz. The total power consumption is 2.79mW at a supply of 1.2V. The total area of the chip is 0.61mm^2. The drawback of this work comes from the large area coverage and complexity of chip due to the use of the on-chip transformer at the input.

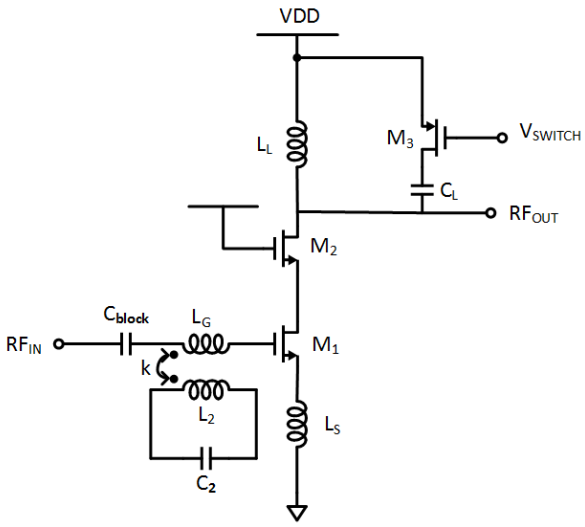


Figure 2-25: LNA with transformer based input matching[34]

h) Analysis and design of a reconfigurable multimode LNA utilizing a multitap transformer [35]

This work explains a reconfigurable multimode LNA incorporating a switched multitap transformer into the input matching network of an inductively degenerated common source amplifier (Fig. 2-26). The input impedance is tuned by changing the coupling coefficient of the transformer by selectively short-circuiting different taps. The LNA operates at 2.8, 3.3 and 4.6 GHz frequencies. The LNA achieved a gain of 14.2-16.1dB, an NF of 2.4-3.7dB, an IIP3 of -4dBm to -2dBm, S11 of -35.4dB to -18.6dB for the frequency range 2.8-4.6GHz. The LNA was fabricated in 0.13um CMOS technology and has a power dissipation of 6.4 mW from a 1.2-V supply. The chip occupies an area of 0.73mm^2. The drawback of this work comes from the complexity in the use of the on-chip transformer.

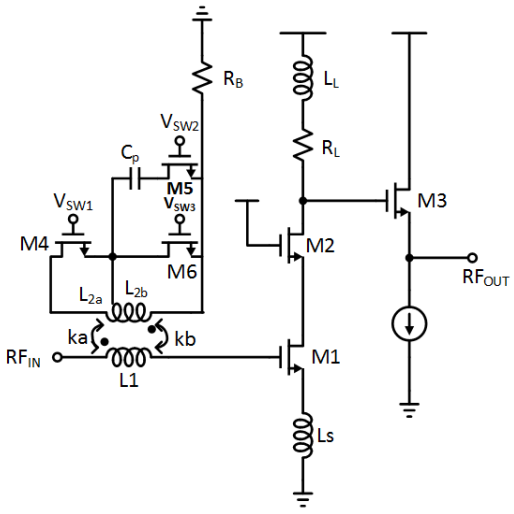


Figure 2-26: Multi-tap LNA[35]

i) Compact inductorless CMOS low-noise amplifier for reconfigurable radio [36]

This work explains an LNA that features a current reuse shunt feedback amplifier for input matching, low-noise figure and small area (Fig. 2-27). It also makes use of a tunable active LC resonator for high gain and continuous tuning of bands. The LNA is designed and fabricated in 0.13um CMOS process and operates from 1.8GHz to 2.4GHz. This work achieved gain of 20.6-22.1dB, NF of 3.2-3.5dB, IIP3 of -16dBm to -11.8dBm, S11 of -14dB for the frequency range 1.8-2.4GHz. It consumes 9.6 mW from a 1.2V supply voltage. The chip occupies an area of 0.052mm^2.

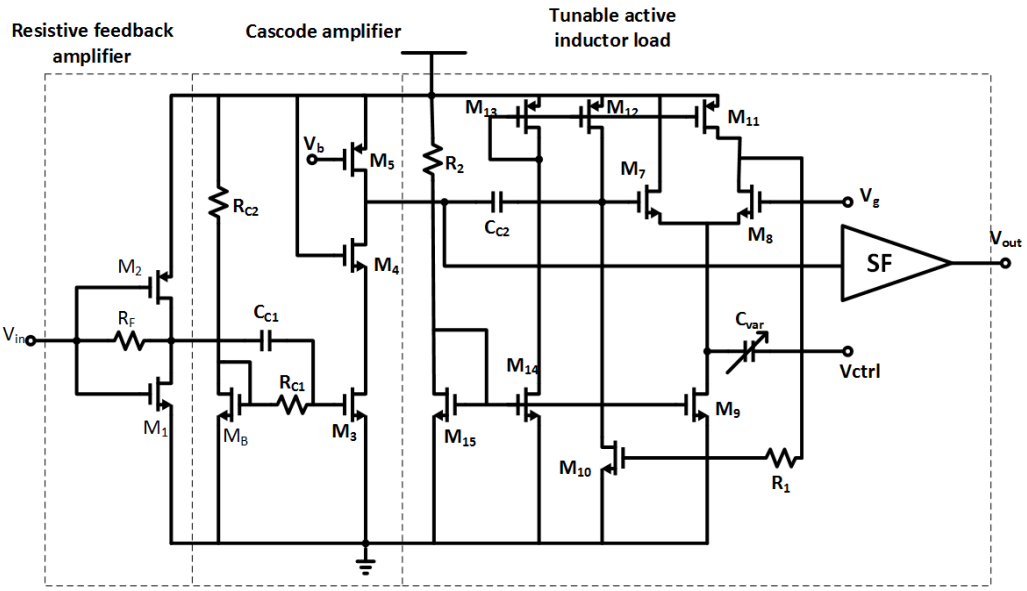


Figure 2-27: Active inductor LNA[36]

j) A CMOS LNA with reconfigurable input matching network [3]

This work describes an LNA with a tunable input matching network (Fig. 2-28). The tunable input matching network consists of an inductor with a gain-modulated inductance. The value of inductance is tuned by tuning the control voltage Vc, which in turn tunes the gain of the active common drain circuit. This LNA was implemented in 0.13um CMOS technology and achieves tunable input matching from 1.9GHz to 2.4GHz. It achieved a gain of 10-14dB, NF of 3.2-3.7dB and an IIP3 of -6.7dBm for the frequency range 1.9GHz-2.4GHz. The total power consumption was 17mW at a supply of 1.2V. The chip occupies an area of 0.083mm^2.

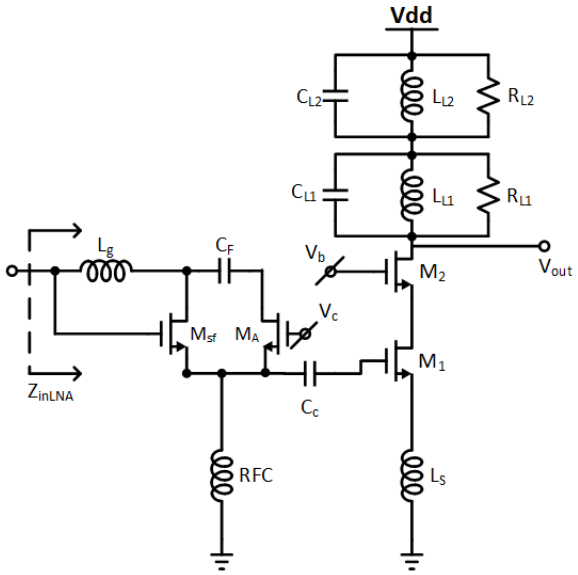


Figure 2-28: LNA with reconfigurable input matching network[3]

k) A 2.4-5.4GHz wide tuning-range CMOS reconfigurable LNA[37]

This work explains an LNA that consists of two stages: a broadband input stage for a steady input matching and noise performance, and a reconfigurable band-selective stage which provides a wide range frequency tuning (Fig. 2-29). The broadband inout matching is achieved with a dual-reactive feedback technique and frequency tuning is conducted by a multitapped switching inductor and varactors. This design is implemented in 0.13um CMOS technology and achieves frequency tuning from 2.4GHz to 5.4GHz. It achieves a gain of 22-24dB, an NF of 2.2-3.1dB, IIP3 of -16– -21dBm and S11 of -30 – -14dB for the frequency range, 2.4-5.4GHz. The total power consumption is 4.6mW at a supply of 1V. The drawback of this work is that it requires the use of an on-chip transformer, which consumes a lot of space.

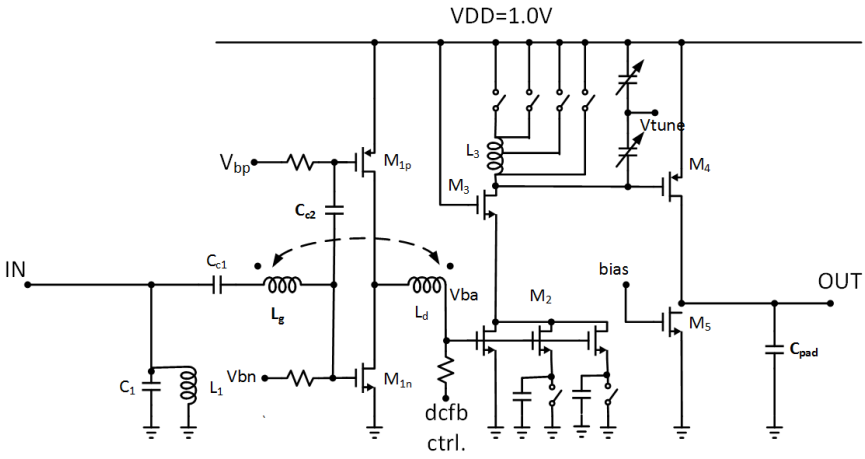


Figure 2-29: Wide tuning-range CMOS reconfigurable LNA[37]

Table 2-1 summarizes the performances of the above designs stating which results are based on simulation and which results are based on actual measurement.

Table 2-1: Performance comparison

	Technology	Frequency Coverage (GHz)	Tuning Method	Gain (dB)	NF (dB)	IIP3 (dBm)	Power (mW)	Results Type
[27]	CMOS 0.18um	1.9/2.1/2.4	discrete	21-23.5	2.45-2.7	-3 –1.45	10.9	simulation
[28]	CMOS 0.18um	2.4/5.2	discrete	15	2.3-2.4	-6.7 – -3	5.04-9	simulation
[29]	CMOS 0.18um	1.8/2.1/2.4	discrete	10	2.0-2.2	15	15	simulation
[31]	CMOS 0.18um	0.9/1.5/2.4	discrete	15-20	1.9-4.5	N/A	30	simulation
[32]	CMOS 0.18um	1.9/2.4/3.5/5	discrete	13-17	1.5-3.1	-17.5	3-5.3	simulation
[33]	CMOS 0.13um	2-5.7	discrete	13-14.7	2.9-7	-21– -17	7.2-12.6	simulation
[34]	CMOS 0.13um	2.45/6	discrete	9.4-18.9	2.8-3.8	-4 – -5.6	2.79	measurement
[35]	CMOS 0.13um	2.8/3.3/4.6	discrete	14.2-16.1	2.4-3.7	-4– -2	6.4	measurement
[36]	CMOS 0.18um	1.8-2.4	continuous	20.6-22.1	3.2-3.5	-16–12	9.6	measurement
[37]	CMOS 0.13um	2.4/3.43/3.96/4.49/5.4	discrete	22-24	2.2-3.1	-16– -21	4.6	measurement
[3]	CMOS 0.13um	1.9-2.4	continuous	10-14	3.2-3.7	-6.7	17	measurement

3. MULTI-BAND RECONFIGURABLE LNA DESIGN

This section covers the design process of the proposed LNA and also the simulation and measurement results.

3.1 LNA Design Overview

In the previous section, a reconfigurable LNA that uses active shunt feedback topology for input matching and LC tank with switchable capacitor bank was discussed[33]. The drawback of this work is that switching several bands with the same capacitor bank reduces the quality factor of the tank each time a capacitor is switched on. This reduction in quality factor is compensated for by using the negative resistance circuit to boost the quality factor of the capacitor bank. However, ths negative resistance circuit is an active circuit that consumes extra current and also introduces noise at the output of the LNA in practice. To overcome these issues, an LNA with dual tanks along with active shunt feedback topology is designed in this work. As shown in Figure 3-1 , the LNA uses active shunt feedback topology for input matching. For band-switching, the LNA has dual LC tanks thus the upper frequency tank and the lower frequency tank. This LNA is designed for operation at 1.8 GHz, 2.4 GHz, 3.5 GHz and 5.2 GHz bands. The upper frequency tank is a parallel combination of inductor and capacitor bank to switch between 5.2 GHz and 3.5 GHz bands while the lower frequency tank switches between 2.4 GHz and 1.8 GHz bands.

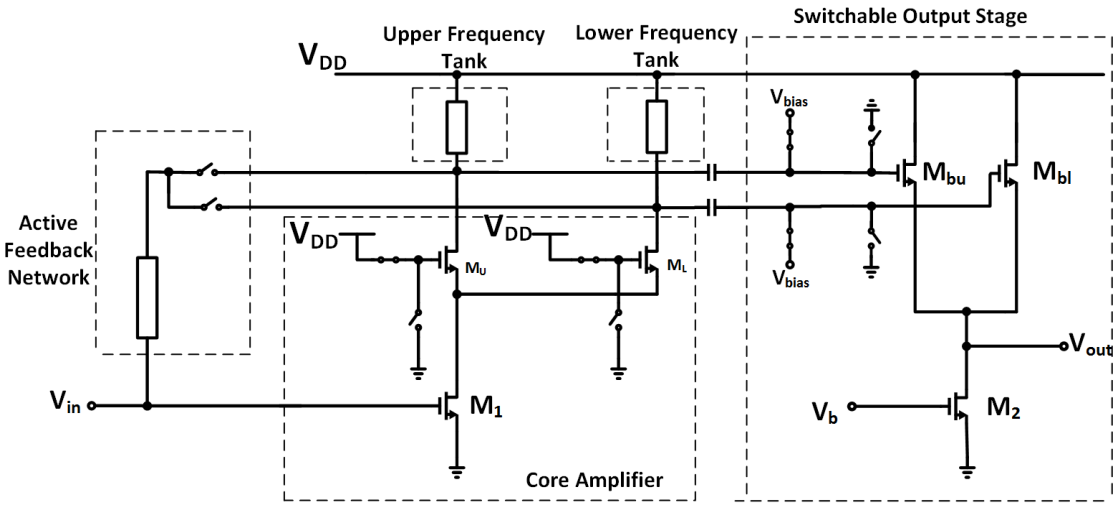


Figure 3-1: Architecture of proposed LNA

3.2 LNA Design

3.2.1 Core Amplifier and Switchable Gm Active Shunt Feedback

The core amplifier(Fig. 3-2) consists of the input transconductor M_1 and the switchable cascode transistors M_U and M_L. The transistor M_U, serves the upper frequency tank while M_L, serves the lower frequency tank. The cascode transistors are turned on and off depending on the band of operation. For example, M_U is turned on when either 5.2 GHz or 3.5 GHz band is desired. This is achieved by connecting it's gate through the switch S_9 to *Vdd* in which case, the complementary switch S_{10} is turned off. The gate controls are V_U and $\overline{V_U}$ respectively. Concurrently, the transistor M_L is turned off by connecting it's gate through the NFET switch S_{12} to ground and opening the complementary PFET switch S_{11}. The gate control signals in this case are $\overline{V_L}$ and V_L respectively.

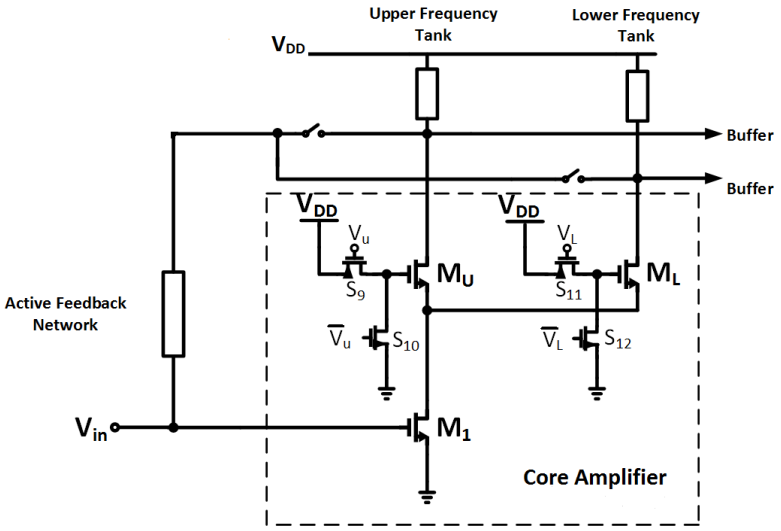


Figure 3-2: LNA core amplifier

The active shunt feedback matching technique is proven to be effective for reconfigurable LNAs[33]. In this design, a switchable gm active shunt feedback matching was employed. This circuit consists of an externally biased source follower, M_{FB} as shown in Figure 3-3.

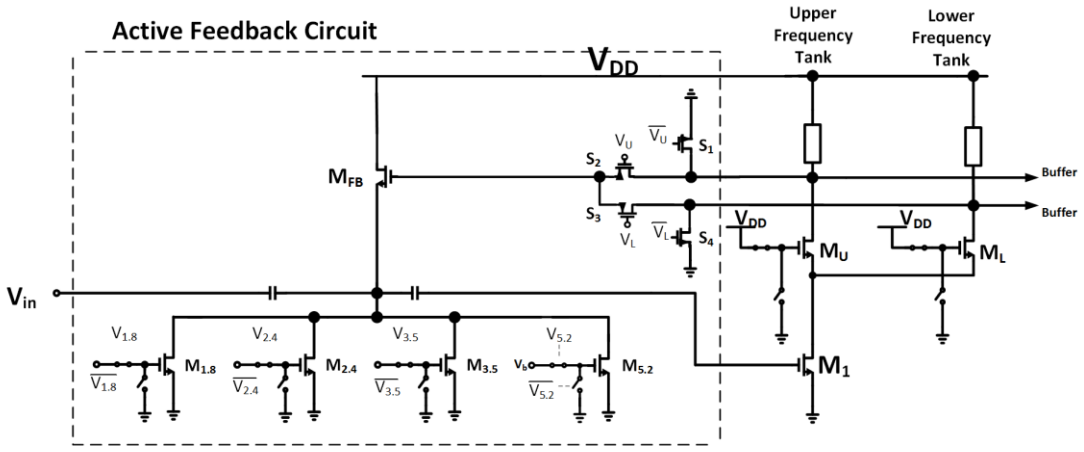


Figure 3-3: Active feedback circuit of LNA

The design equations of the LNA include the input impedance (Z_{in}), the voltage gain (A_V) and the noise factor (F)[38]. Z_{in} is defined as

$$Z_{in} = \frac{1}{gm_{M_{FB}}(1 + gm_{M_1}R_L)} = 50\Omega \qquad 3-1$$

Where $gm_{M_{FB}}$ is the transconductance of the feedback transistor, M_{FB}, gm_{M_1} is the transconductance of the input common source transistor, M_1 and R_L is the equivalent parallel resistance of the selected resonant load. A_V is given by

$$A_V = gm_{M1}R_L\left[\frac{1/gm_{MFB}}{1/gm_{MFB} + R_S(1 + gm_{M1}R_L)}\right] \qquad 3-2$$

Where R_S is the source impedance. F is derived as:

$$F = 1 + (1 + \frac{1}{1 + A_{VO}})^2.\frac{\gamma_1}{4gm_{M1}R_S} + \frac{\gamma_{MFB}}{4(1 + A_{VO})} \qquad 3-3$$

$$+ \frac{gm_{MF}R_S\gamma_F}{4} + \frac{R_L}{4R_S(1 + A_{VO})^2}$$

Where γ_1 , γ_{MFB} and γ_F are the noise factors of M_1, M_{FB} and M_F ($M_{1.8}$ or $M_{2.4}$ or $M_{3.5}$ or $M_{5.2}$) in Fig. 3-3, respectively. A_{VO} is the open loop gain given as:

$$A_{VO} = gm_{M1}R_L \qquad 3-4$$

The second term of equation 3-3 represents the noise contribution from M_1. The third term represents the noise contribution from M_{FB}. The last two terms represent noise from the switchable current source M_F ($M_{1.8}$ or $M_{2.4}$ or $M_{3.5}$ or $M_{5.2}$) and R_L respectively. R_L is frequency dependent as will be discussed later. From equation 3-3, it is noticed that the noise contributions from M_{FB} and R_L are insignificant for a large open loop gain.

The noise factor equation also features contribution from the switchable current

transistor M_F ($M_{1.8}$ or $M_{2.4}$ or $M_{3.5}$ or $M_{5.2}$). This contribution is minimized for smaller gm_{MF}. Therefore, a smaller aspect ratio is used for M_F. The most important term in the equation 3-3 is the noise contribution from M_1. Larger gm_{M1} provides lower noise contribution and vice versa. It can also be noted from equation 3-1 that the input impedance depends on gm_{M1}. Therefore, the major design issue comes from the sizing of the input transistor M_1 so as to ensure input impedance matching and minimum noise. The first step is to determine the size and bias condition (current density) of M_1 that satisfies both impedance matching and minimum noise.

There is an optimum current density for the minimum noise figure (NF_{min}). To determine the current density for NF_{min}, a simulation test bench is set up to sweep the bias current of M_1 through a 30um transistor with 5um fingers while M_{FB} is set to 50um/180nm. An ideal current source is used to provide current through M_{FB} in this case. A plot of NF_{min} versus current density for various frequency bands for M_1 are obtained. The optimum current density (J_{OPT}) is approximately 0.27mA/um and is independent of frequency (Fig. 3-3).

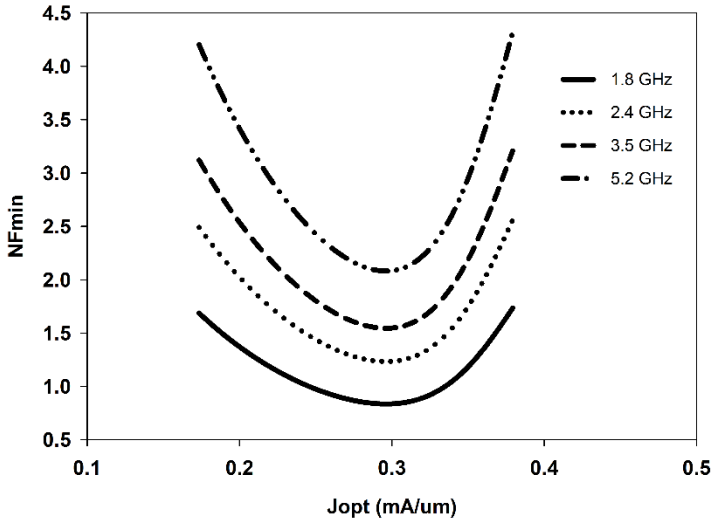


Figure 3-4: NFmin versus J(mA/um) for various frequency bands

To find the width of M_1 for input matching and minimum noise, the width was swept while maintaining a constant current density of 0.27mA/um until the source impedance for minimum NF_{min} reached 50 Ω. On the Z-smith chart, this occurs when Γ_{opt} intersects the $\Gamma=1$ circle on the smith chart(Fig. 3-5). The width was found to be approximately 300um.

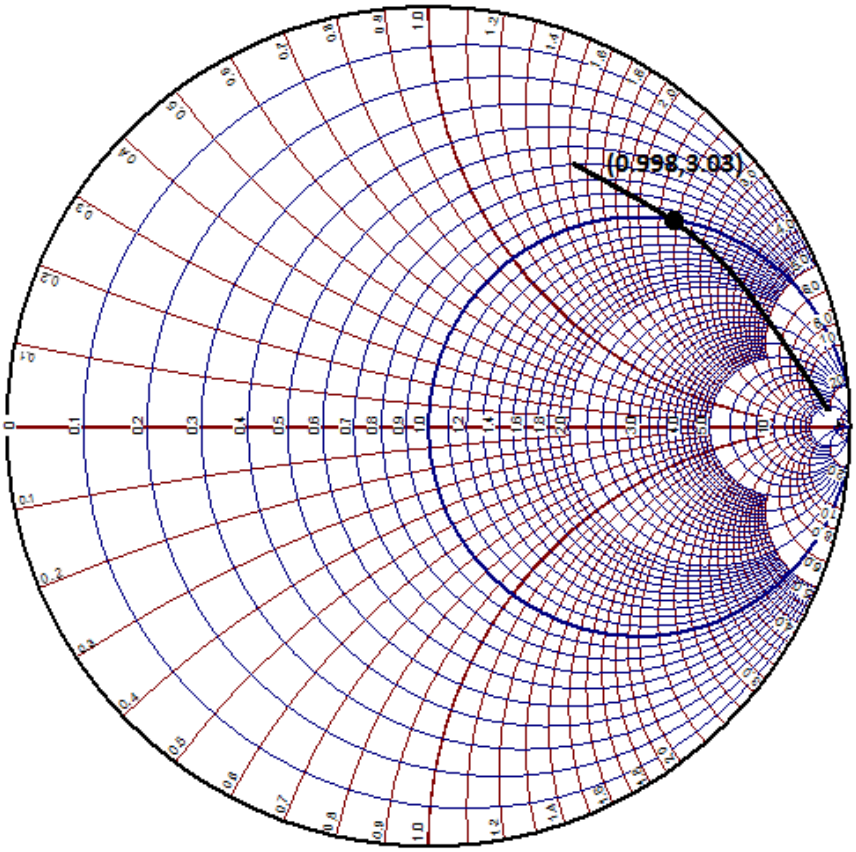


Figure 3-5: Γ_{opt} versus input stage transistor width

To achieve 50Ω input matching using equation 3-1, gm_{MFB} is adjusted accordingly using M_F. The variation of gm_{MFB} doesn't affect NF_{min} according to equation 3-3.

The size of the cascode transistor is chosen as small as possible to minimize the parasitic capacitance. Higher drain parasitic capacitance limits the maximum operating frequency. The cascode transistor doesn't have significant effect on the overall noise figure.

The active shunt feedback technique is used in this work to provide input matching

according to equation 3-1. This circuit consists of a source follower, M_{FB} with switchable current sources as shown in Figure 3-3. Z_{in} depends on the effective load impedance at the operating frequency, R_L which, can be expressed as:

$$R_L = \omega LQ || R_{p,cap} \qquad 3-5$$

Where Q represents the quality factor of the inductive load and $R_{p,cap}$ is the effective parallel resistance of the tuned capacitor bank at resonance. Depending on the frequency of operation a particular tank is selected as input to the gate of the feedback transistor. gm_{MFB} can be appropriately adjusted using M_F to achieve 50Ω at the input for each desired frequency.

The inductors selected for the two tanks have their peak Q's at the respective lower bands that is, at 1.8GHz band and 3.5GHz band for the LFS and UFS tanks, respectively. As frequency decreases, the R_L decreases accordingly. Thus, in order to maintain an input matching impedance of 50Ω, $gm_{M_{FB}}$ must increase and vice versa according to equation 3-1. $gm_{M_{FB}}$ at each frequency band of operation is set by enabling the appropriate current transistor and disabling the rest. The current source bank M_F of the feedback transistor consists of $M_{1.8}$, for 1.8GHz band, $M_{2.4}$ for 2.4 GHz band, $M_{3.5}$ for 3.5GHz and $M_{5.2}$ for 5.2GHz operation. These transistors have widths determined by the amount of current necessary to provide an input matching (S_{11}) of better than -10 dB at the band of operation. The sizes of the current source transistors and currents are depicted in Table 3-1.

Table 3-1: Sizes and currents of switchable current source transistors for active shunt feedback input matching circuit

Transistor	Size (W/L)	Current (uA)
$M_{1.8}$	42u/240nm	530
$M_{2.4}$	35u/240nm	440
$M_{3.5}$	38u/240nm	480
$M_{5.2}$	40u/240nm	500

3.2.2 LNA Band Switching

As described in the previous sections, the band switching is achieved by switching two tanks known as upper section and lower section tanks. This is illustrated in Figure 3-6 [39]. Each tank also incorporates two bands. The upper section tank comprises the 5.2GHz and 3.5 GHz frequency bands whiles the lower section tank comprises the 2.4 GHz and the 1.8 GHz frequency bands. To select a tank, the corresponding cascode transistor is turned on while the other remains off.

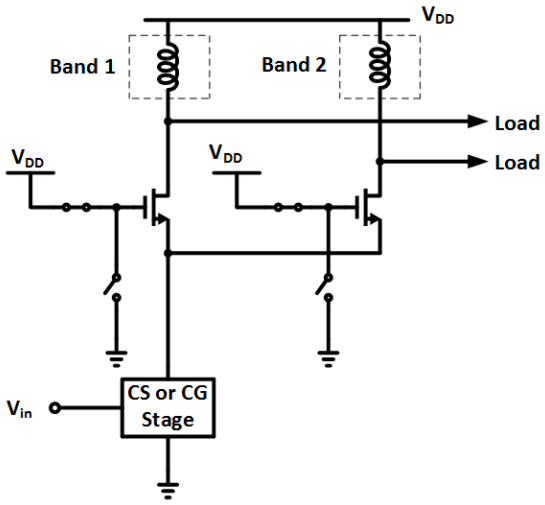


Figure 3-6: Band switching by programmable cascode branches[7]

3.2.2.1 Upper Section Tank

The upper secton tank is an inductive-capacitive resonant tank to switch 5.2 GHz and 3.5 GHz frequencies. As shown in Figure 3-7, the load consists of an inductor L_u, two capacitors $C_{5.2}$ and $C_{3.5}$ and a PMOS switch $S_{3.5}$. When the switch is off, the resonance of the tank occurs at 5 GHz band thus selecting the upper band by default. To select the 3.5 GHz band, the capacitance $C_{3.5}$ has to be added in parallel to $C_{5.2}$ by putting on the switch $S_{3.5}$.

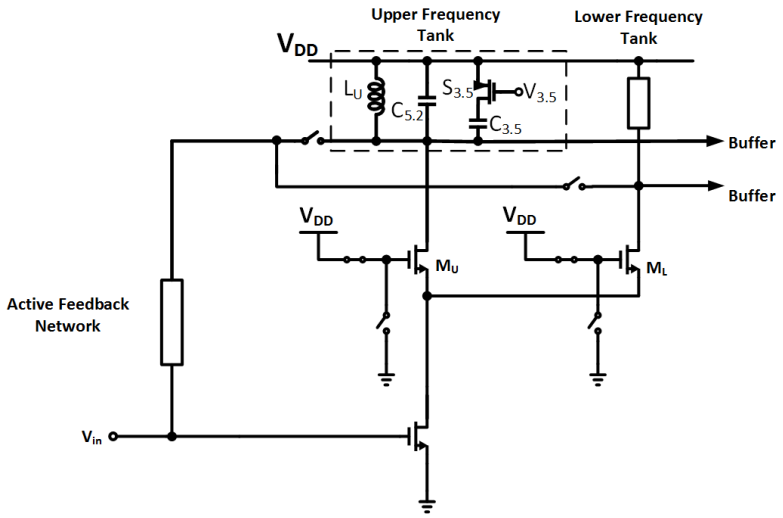


Figure 3-7: Upper frequency section load

The sizing of the inductance, capacitance and switch is very critical in the design. The inductance used in the design is the spiral inductor in the IBM technology. It's value and dimensions is chosen such that the self resonant frequency is above the maximum resonant frequency which in this case is 5.2 GHz. Larger inductor metal widths gives lower loss hence higher Q, but at reduced inductances and lower self resonant frequency (SRF), due to increased self-capacitance and coupling to the substrate. Larger outer dimension yields higher inductance, but lower self-resonant frequency due to increased inductance and self-capacitance. Larger number of turns increases the inductance, but also increases self capacitance, and thus a lower SRF than an equivalent inductor with less turns and larger area. The outer dimension of the inductor is 270um with and metal width of 25 um (Fig. 3-8).

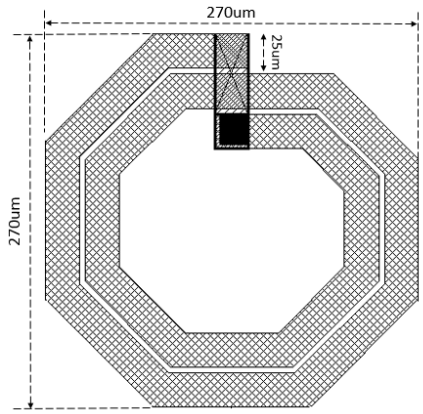


Figure 3-8: Layout of inductor L_U

The value of inductance used for the upper band was 1.10 nH. This value resonates with the capacitor $C_{5.2}$ and the parasitics of $C_{3.5}$ and switch $S_{3.5}$ when the switch is off to produce desired resonance at 5.2 GHz band. The parasitics also include the parasitic of the cascode transistor. The design was made in order to minimize this parasitic as much as possible. This is done by reducing the size of the transistor. When the switch $S_{3.5}$ is on, the inductance 1.10nH resonates with the capacitances $C_{5.2}$ and $C_{3.5}$ and the parasitics of the switch and the cascode transistor to produce frequency peaking at 3.5 GHz.The Q of the inductor L_U was set with a peak close to 3.5 GHz to nullify the frequency effect on the quality factor of the capacitive load which is higher at 5.2GHz. This is done in order to maintain a fairly constant gain across bands as will be discussed later. The frequency variation of the Q factor is illustrated in Figure 3-9. Figure 3-9 shows the inductance variation versus frequency with a self resonant frequency around 9 GHz . The inductance varies from 1.10 nH at 5.2 GHz to around 0.96 nH at 3.5 GHz which represents

a variation of 12.7% across the two bands.

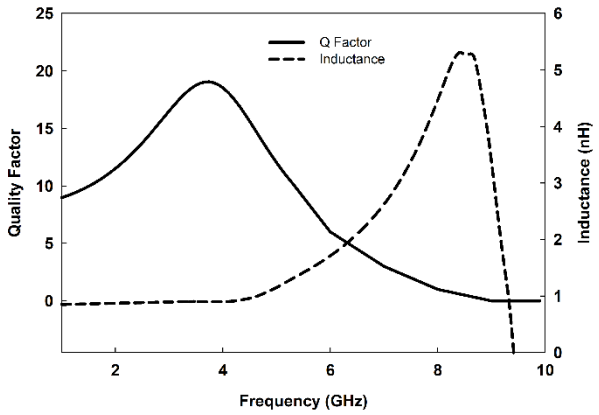
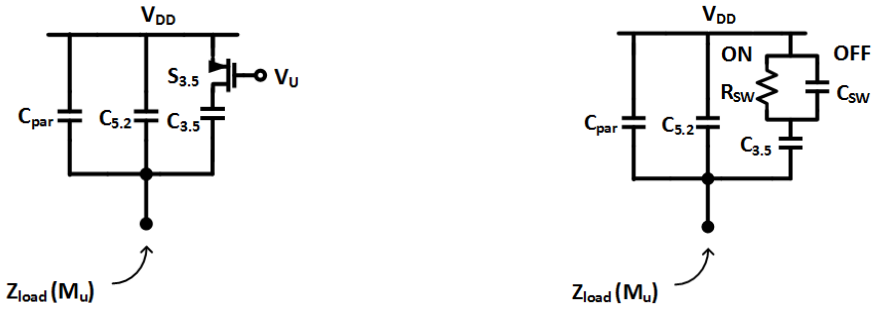


Figure 3-9: Quality factor and inductance versus frequency of L_U

The capacitive load of the tank comprises the parallel combination of $C_{5.2}$, the parasitics of the cascode transistor and the series combination of $C_{3.5}$ and the PMOS switch $S_{3.5}$ as shown in Figure 3-10. The capacitors $C_{5.2}$ and $C_{3.5}$ are Metal Insulator Metal (MIM) capacitors. These MIM capacitors are chosen due to their relatively higher linearity and quality factor compared to MOS capacitors. The capacitors are formed using the sixth metal as the top plate and the fourth metal as the bottom plate with silicon dioxide as the dielectric.



(a) (b)

Figure 3-10: (a) Capacitive load of upper frequency section tank, (b) equivalent load showing the on resistance and total parasitic capacitance of switch $S_{3.5}$

The FET switch is controlled by the voltage V_U. The capacitor, $C_{3.5,}$ is enabled by pulling the gate of the PMOS switch to ground and disabled by pulling it to V_{DD}. The PMOS switch can be represented by the parallel combination of resistance ,$R_{SW,}$ and the total parasistic capacitance of the switch ,C_{SW}. The sizing of the transistor $S_{3.5}$ proves critical. For narrow transistor, the on-resistance remains so high that the tank does not notice the effect of the capacitance, $C_{3.5}$, in casse the 3.5 GHz needs to be selected. For a moderate width, the on-resistance limits the Q of $C_{3.5,}$ thus lowering the Q of the overall tank and hence the voltage gain at 3.5 GHz band. This can be demonstrated by transforming the series combination of $C_{3.5}$ and R_{SW} to a parallel network comprising $C_{5.2}$ and

$$R_p \approx Q^2 R_{SW} \qquad 3-6$$

$$Q = (C_{3.5} \omega R_{SW})^{-1} \qquad 3-7$$

This implies that R_{SW} should be minimized such that R_P is significantly larger than the

equivalent parallel resistance of inductor L_U. However, increasing the width of $S_{3.5}$ increases the capacitance that it introduces in the off state that is, when the 5.2 GHz band is selected. The equivalent capacitance seen by the tank when $S_{3.5}$ is off is equal to the series combination of $C_{3.5}$ and C_{SW}. This means, $C_{5.2}$ must be less than it's original value by this amount. Thus the width of $S_{3.5}$ poses a trade-off between the tolerable value of $C_{5.2}$ when $S_{3.5}$ is off and the gain reduction when $S_{3.5}$ is on. The variation of resistance R_{SW} and total parasitic capacitance C_{SW} is illustrated in Figure 3-11.

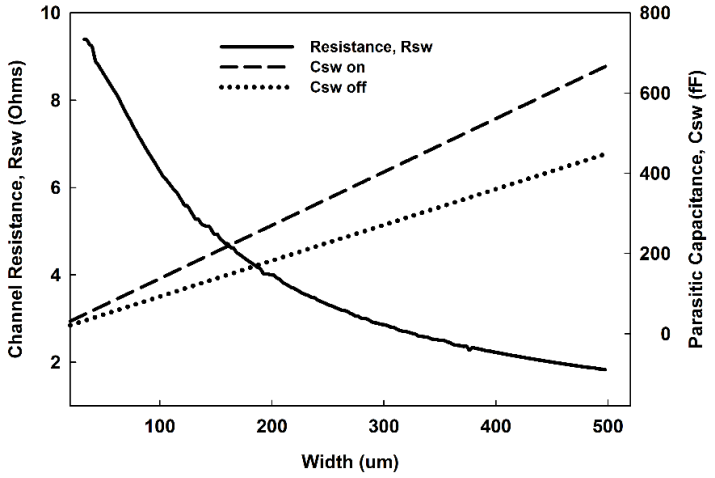


Figure 3-11: Channel resistance and parasitic capacitance versus width of PFET switch

The switch was sized at 200um with 5um fingers at minimum length to achieve a channel resistance of 4 Ω. This dimension of switch transistor gives a parasitic capacitance of 210 fF when the switch is on and 166 fF when off. This size was chosen to

ensure that there is very little variation in parasitic capacitance as the switch is turned on and off. The quality factor of the capacitive load was simulated at 3.5 GHz and 5.2 GHz bands and found to be around 13.95 and 20.1, respectively. It can be observed that the Q of the capacitive load increases with resonant frequency. This is due to the decrease in the parallel impedance of the capacive load with capacitance and the inverse relation between the capacitance and the resonant frequency. Thus to maintain a fairly constant gain across the two bands, it is imperative to choose an inductor with the peak Q as close to the 3.5 GHz band as possible as shown in Figure 3-9. The quality factor of the inductor changes from 18.8 at 3.5 GHz to 11 at 5.2 GHz. This represents a percentage decrease of 43 % approximately. For the capacitive load, the Q factor changes from 13.95 at 3.5 GHz to 20.1 at 5.2 GHz , a percentage increase of 44 % approximately. Therefore, a fairly constant gain can be ensured. The sizes of the passives and the switch transistor is shown in Table 3-2.

Table 3-2: Size/Value of upper frequency tank devices

Device	**Size/Value**
Inductor (L_U)	1.10 nH
Capacitor ($C_{5.2}$)	720 fF
Capacitor ($C_{3.5}$)	990 fF
Parasitic Capacitance (C_{par1})	110 fF
PFET switch ($S_{3.5}$)	200 um/180 nm

3.2.2.2 Lower Frequency Section Tank

The lower frequency section tank is also an inductive-capacitive resonant tank to switch 2.4 GHz and 1.8 GHz frequencies. The load consists of inductor L_L, the capacitors $C_{2.4}$ and $C_{1.8}$ and the PMOS switch $S_{1.8}$. as shown in Figure 3-12. The signal $V_{1.8}$ is the switch control voltage. It pulls the gate to 1.8 V to switch the transistor off and pulls it to ground to turn it on. When the switch is off, the inductor L_L resonates with $C_{2.4}$ and the parasitic capacitance of the cascode transistor M_L to produce frequency peaking at 2.4 GHz. The capacitor $C_{1.8}$ is added in parallel to $C_{2.4}$ when the switch $S_{1.8}$ is turned on in which case the resonance occurs at 1.8 GHz band.

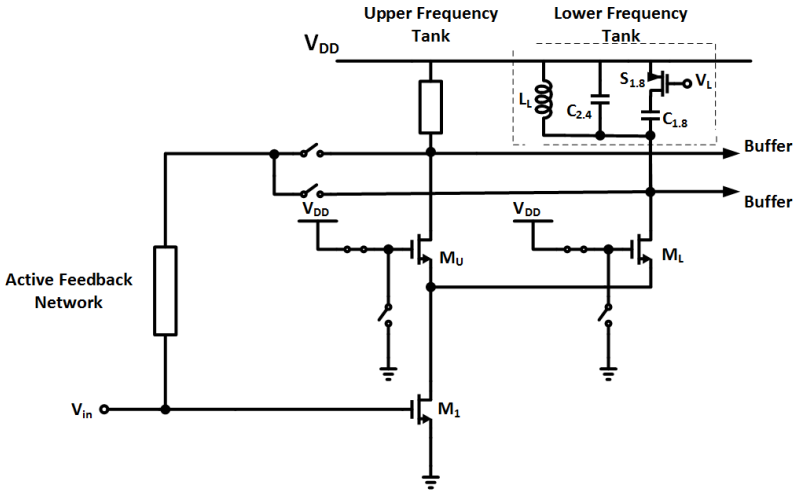


Figure 3-12: Lower frequency section tank

Similar to $L_{U,}$ the inductor used in the lower frequency section tank, L_L is a spiral inductor(Fig. 3-13). The outer dimension of the inductor is 300um and the metal width is 25um.

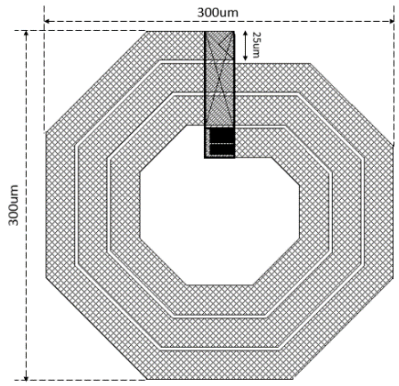


Figure 3-13: Layout of inductor L_L

The inductor , L_L is designed to have a peak Q as close to the lower band that is ,1.8 GHz as possible and the self resonant frequency beyond the higher frequency band that is 2.4 GHz band similar to the higher band inductor, L_U. The Q of the inductor decreases from 18.2 at 1.8 GHz to 13 at 2.4 GHz a percentage decrease of 29 % approximately across the two bands. The inductor varies from 1.84 nH at 2.4 GHz to 1.68 nH at 1.8 GHz, a variation of 8.7 % across the two bands. The frequency variation of the Q and the inductance of L_L is shown in Figure 3-14. The capacitive load of the tank consists of the parallel combination of $C_{2.4}$, the parasitics of the cascode transistor, $M_{L,}$

and the series combination of $C_{1.8}$ and the PMOS switch $S_{1.8}$ as shown in Figure 3-15.

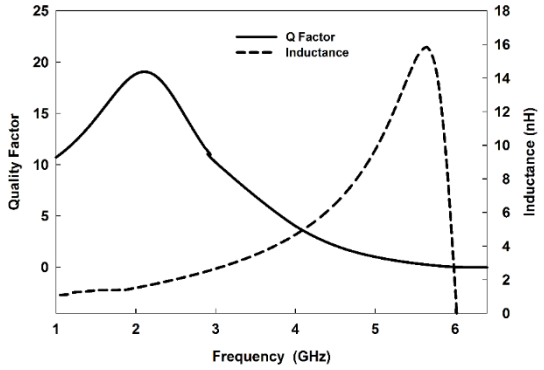


Figure 3-14: Frequency variation of Quality factor and inductance of L_L

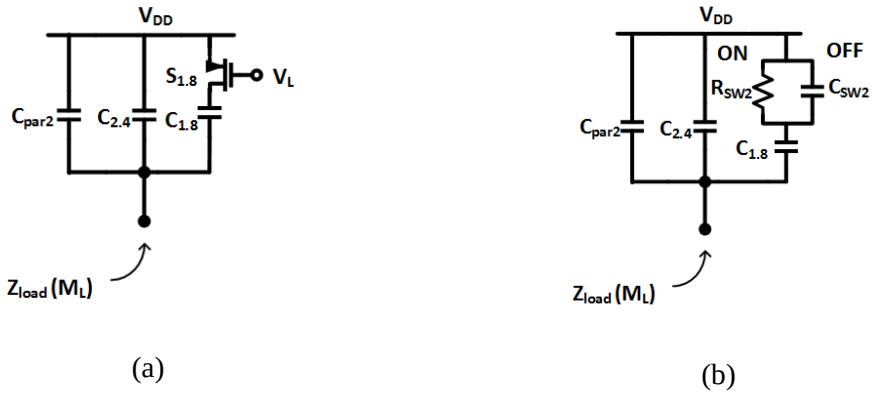


Figure 3-15: (a) Capacitive load of lower frequency section tank, (b) equivalent load showing the resistance and total parasitic capacitance of switch $S_{1.8}$

Similar to the previous section, the capacitors $C_{2.4}$ and $C_{1.8}$ are MIM capacitors and C_{par2} represent the parasitic capacitance of the cascode transitor, M_L. R_{SW2} and C_{SW2} represent the channel resistance and total parasitic capacitance of the PMOS switch, $S_{1.8}$. The switch transistor was sized at a width of 200um at minimum length and has the same characteristics as in Figure 3-11. The quality factor of the capacitive load was simulated. It increases from 15.6 at 1.8 GHz to 20.34 at 2.4 GHz, a percentage increase of 30.3 % which almost nullifies the percentage decrease in inductor quality factor of 29 %. Thus a fairly constant gain can be maintained across the two lower bands. The sizes of the passives and PFET switch are shown in Table 3-3.

Table 3-3: Size/Value of devices of lower frequency tank

Device	**Size**
Inductor (L_L)	1.84 nH
Capacitor ($C_{2.4}$)	2.25 pF
Capacitor ($C_{1.8}$)	1.81 pF
Parasitic Capacitance	110 fF
PFET Switch ($S_{1.8}$)	200 um/ 180 nm

3.2.3 Switchable Output Stage

The output stage of the LNA is based on a source follower topology as shown in Figure 3-16. It consists of source follower transistors, M_{bu} and M_{bl}, a current source, M_2

and complementary switch pairs S_5/S_6 and S_7/S_8. The gates of M_{bu} and M_{bl} are AC coupled to the upper frequency section tank and lower frequency section tank, respectively. The source followers M_{bu} and M_{bl} are enabled by connecting their gates through the PFET switches S_6 and S_8 to the bias voltage, V_{bias} . They are disabled by connecting their gates to ground through the switches, S_5 and S_7. The control voltages to the switches are; $V_U/\bar{V}_U$ for S_6/S_5 and $V_L/\bar{V}_L$ for S_8/S_7. The switch control voltages are such that one source follower (that is M_{bu} or M_{bl}) is enabled at a time. The main purpose of using this output stage is to accomplish an output impedance of 50 Ω. The transconductances of M_{bu} or M_{bl} , gm_{bu} and gm_{bl} are chosen such that $1/gm_{bu} \,||g_{ds2}$ or $1/gm_{bl} \,||g_{ds2}$ is equal to 50 Ω. g_{ds2} represents the conductance of M_2.

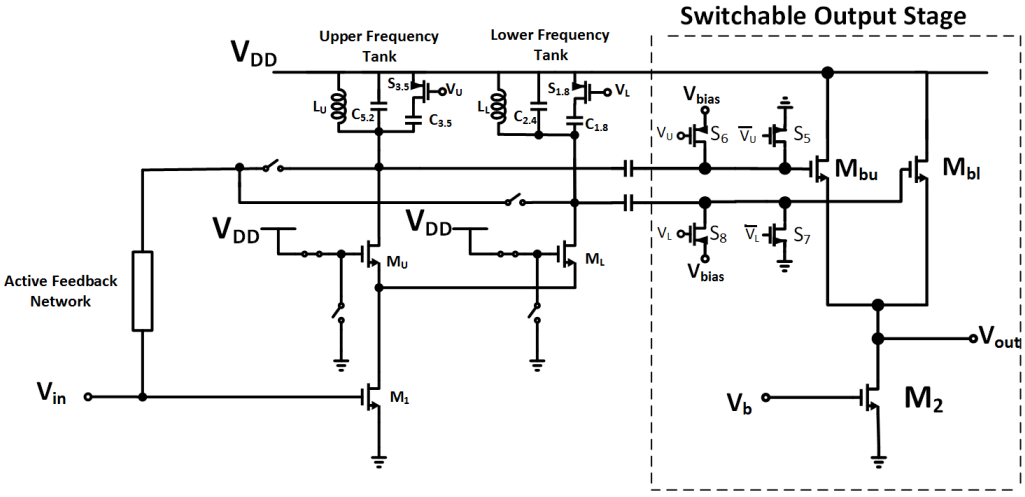


Figure 3-16: Switchable output stage of LNA

3.2.4 Digital Control Circuit

The control voltages to the switches used in the LNA design are generated by a combination of digital gates as shown in Figure 3-17. The digital control block has four inputs; $I_{1.8}$ for 1.8 GHz band, $I_{2.4}$ for 2.4 GHz band, $I_{3.5}$ for 3.5 GHz band, $I_{5.2}$ for 5.2 GHz band. These inputs are pulled to 1.8 V or 0 V depending on the band of interest. The digital bock has six pairs of complementary output voltages $(V_L, \overline{V_L})$, $(V_U, \overline{V_U})$, $(V_{1.8}, \overline{V_{1.8}})$, $(V_{2.4}, \overline{V_{2.4}})$, $(V_{3.5}, \overline{V_{3.5}})$, $(V_{5.2}, \overline{V_{5.2}})$. The logic used for the output voltage is an active low logic in which case a 0 (0 V) to the gate input of a PFET transistor is required to enable a current source transistor, a source follower or an LC load. The truth table for the control block is shown in Table 3-4.

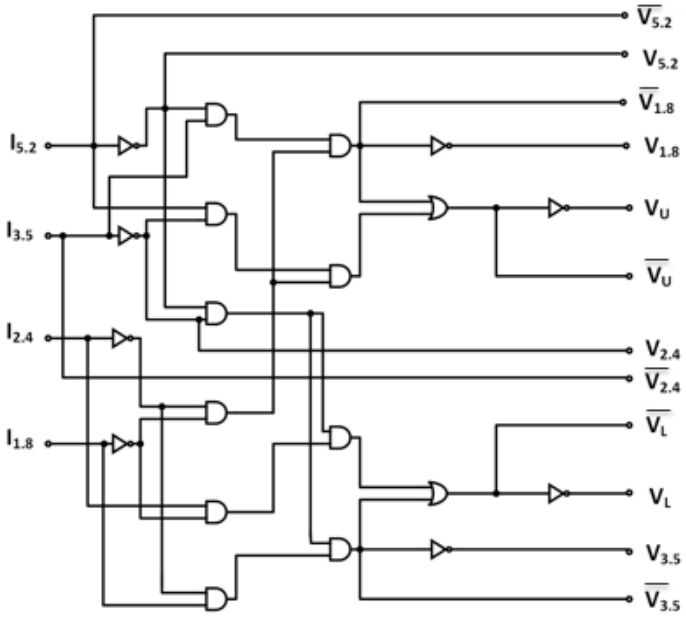


Figure 3-17: Digital control circuit of LNA

Table 3-4: Truth table of digital control circuit

$I_{1.8}$	$I_{2.4}$	$I_{3.5}$	$I_{5.2}$	V_U	V_U^1	V_L	V_L^1	$V_{1.8}$	$V_{1.8}^1$	$V_{2.4}$	$V_{2.4}^1$	$V_{3.5}$	$V_{3.5}^1$	$V_{5.2}$	$V_{5.2}^1$
0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	0	1	0	1	1	0	1	0	1	0	1	0	0	1
0	0	1	0	0	1	1	0	1	0	1	0	0	1	1	0
0	0	1	1	1	0	1	0	1	0	1	0	0	1	0	1
0	1	0	0	1	0	0	1	1	0	0	1	1	0	1	0
0	1	0	1	1	0	1	0	1	0	0	1	1	0	0	1
0	1	1	0	1	0	1	0	1	0	1	0	0	1	1	0
0	1	1	1	1	0	1	0	1	0	0	1	0	1	0	1
1	0	0	0	1	0	0	1	0	1	1	0	1	0	1	0
1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1
1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0
1	0	1	1	1	0	1	0	0	1	1	0	0	1	0	1
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1	1	0	1	1	0	1	0	0	1	0	1	1	0	0	1
1	1	1	0	1	0	1	0	0	1	0	1	0	1	1	0
1	1	1	1	1	0	1	0	0	1	0	0	1	0	1	

3.3 Complete LNA Schematic

The complete schematic of the proposed LNA is shown in Figure 3-18. Current mirrors, DC blocking resistors and digital control block are missing in this diagram.

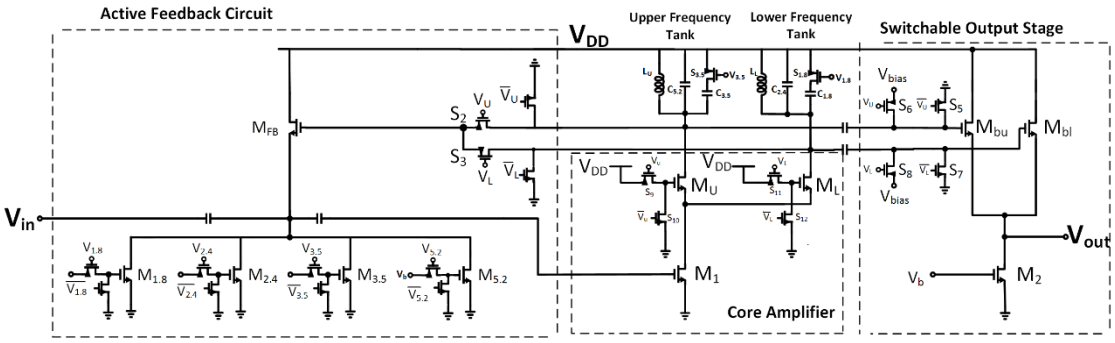


Figure 3-18: Complete schematic of LNA

3.4 LNA IC Layout and Post-Layout Simulations

The layout of the LNA was designed with the goal of minimizing parasitic elements on signal lines by keeping them as short as possible, and reasonably balancing the width to length ratios of the lines, in order to optimize the balance between parasitic capacitance and series resistance. Upper layer metals are used for longer signal routing distances, as these have generally lower sheet-resistances compared to lower metal layers. Power and ground lines are made wide enough to reduce voltage drops along power traces and to increase coupling to the substrate so as to minimize noise on these lines. MIMCAPs are used as decoupling caps between the power and ground lines in order to provide a path

for noise currents to ground. ESD protection is applied at all dc and signal pads to protect the circuit from ESD spikes. A microphotograph of the fabricated LNA is shown in Figure 3-19. The simulations after extraction of the layout are shown in Figure 3-20 through Figure 3-22.

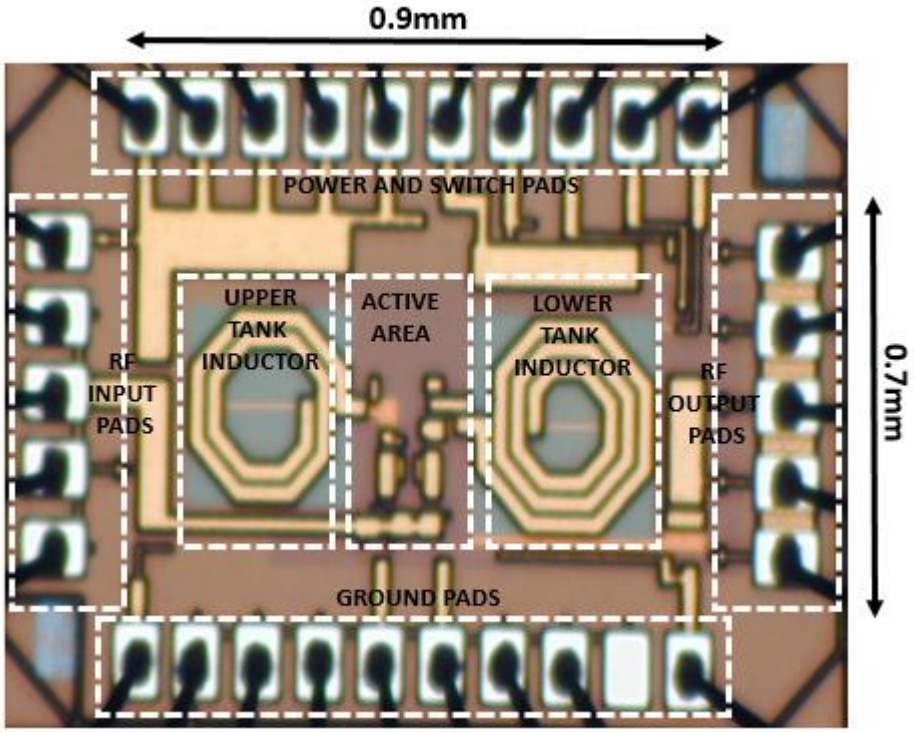
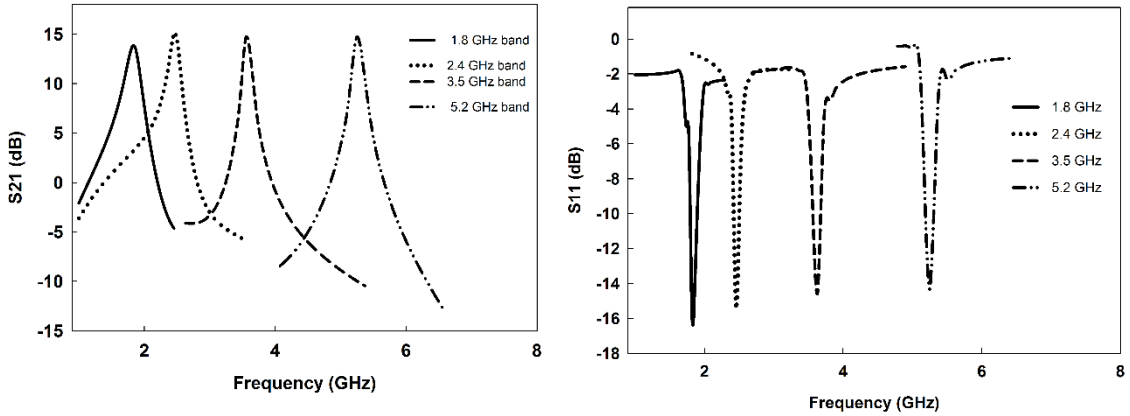


Figure 3-19: Chip micrograph



(a) (b)

Figure 3-20: (a)Simulated S21 of LNA (b)simulated S11 of LNA

As shown in Figure 3-20(a), the S21 for all bands remain fairly constant as predicted. The gain has a minimum of 14dB at 1.8GHz and a maximum of 15dB at 2.4GHz. The S11 varies from -16 dB to -14.8 dB from 1.8 GHz band to 5.2 GHz band.

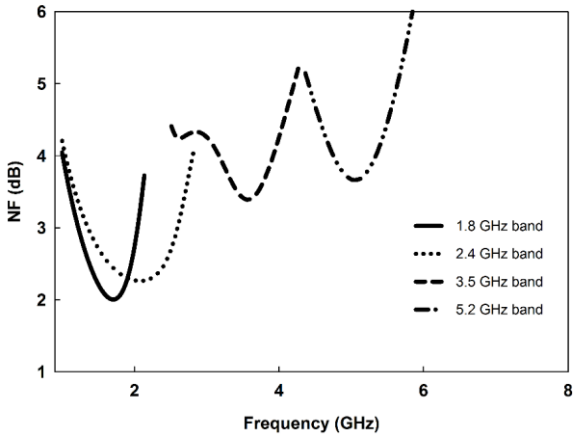


Figure 3-21: Simulated noise figure of the LNA for four different bands

The simulated noise figure for all bands is shown in Figure 3-21. As can be seen, the NF varies from 2 dB to 3.8 dB from 1.8 GHz band to 5.2 GHz band.

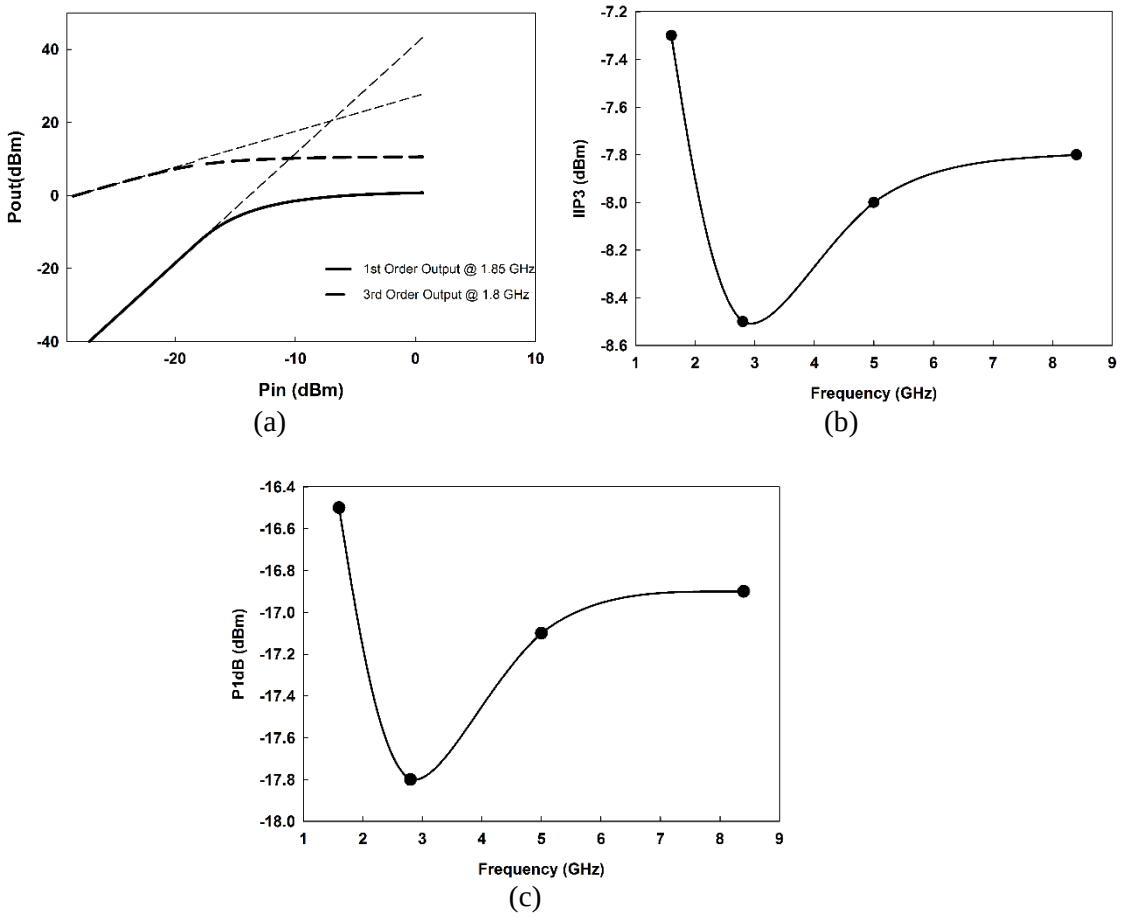


Figure 3-22: (a) IIP3 simulation for 1.8 GHz band (b) IIP3 versus frequency
(c) P1dB versus frequency

Figure 3-22 shows the linearity simulations. Two tones at 50MHz apart from each other were used as input signals to the LNA. The transfer characteristics for the first order output and third order output were plotted from which the IIP3 can be determined (Fig. 3-22(a)). The IIP3 has a minimum of -8.5dBm at 2.4GHz and a maximum of -7.3dBm at 1.8GHz. This is evident from the fact that the minimum and the maximum gains occur at 1.8GHz and 2.4GHz respectively. The P1dB also has a minimum of -17.8dBm at 2.4GHz and a maximum of -16.5dBm at 1.8GHz. The S-parameter, NF and linearity simulations for all the four bands are summarized in Table 3-5.

Table 3-5: S-parameter,NF,IIP3 and P1dB values at various bands

Frequency(GHz)	S21(dB)	S11(dB)	NF(dB)	IIP3(dBm)	P1dB(dBm)
1.8	13.9	-16.3	2.1	-7.3	-16.5
2.4	15.1	-15.4	2.5	-8.5	-17.8
3.5	14.9	-14.6	3.4	-8.0	-17.1
5.2	14.7	-14.3	3.8	-7.8	-16.9

3.5 Measurement Setup and Results

In this section, test setup and measurement results of the fabricated LNA will be discussed. The populated PCB board which (Device Under Test (DUT)) is shown in Figure 3-23. The LNA tests includes DC test, S-parameter test, noise figure test and

linearity test. The basic RF equipment used include network analyzer(NA), spectrum analyzer, signal generator etc.

Figure 3-23: PCB board

3.5.1 S-parameter Testing and Results

The S-parameters of the LNA (S11,S22,S12 and S21) are measured by connecting the DUT to the network analyzer, shown in Figure 3-24. An Agilent N4467 series network analyzer was used to take the measurement. The input and output were connectd to a 50 ohms standard cable. The network analyser, cable and probes were calibrated prior to each measurement.

The calibration was done by connecting calibration terminations for open, short and matched load conditions to the input and output ports of the network analyzer through

the cables which were used for the testing and then enabling the appropriate calibration functions of the network analyzer. The S-parameters(S21 and S11) were then measured and are shown in Figure 3-25.

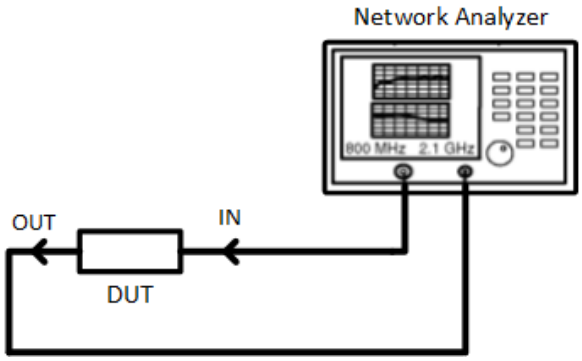
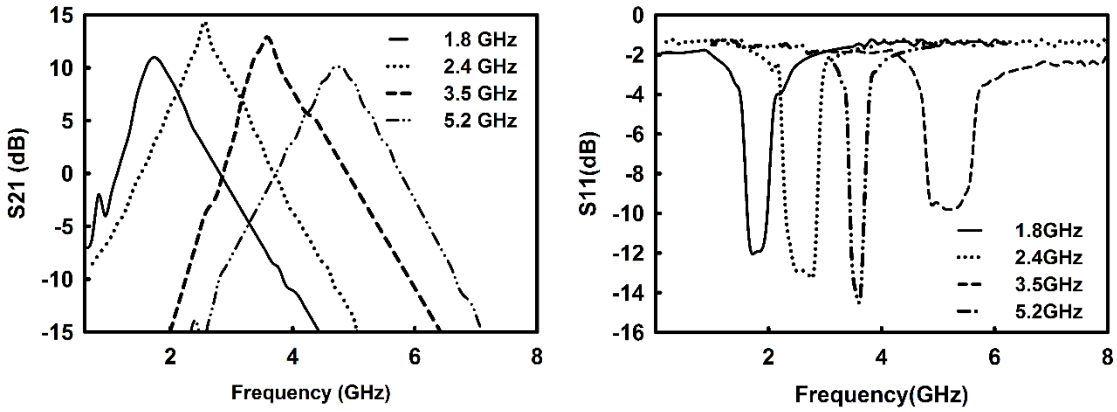


Figure 3-24: S parameter measurement setup



(a) (b)

Figure 3-25: Measured S21 parameters for the four bands b) measured S11 parameters for the four bands

The minimum gain measured is 10.1dB at the 1.8GHz band and the maximum gain is 13.6dB at the 2.4GHz band. The measured S21 values for all the four bands are generally lower compared to the simulated results (minimum of 13.9dB at 1.8GHz and a maximum of 15dB at 2.4GHz). Also the measured frequency responses show slight frequency offsets (approximately 100MHz) from the simulation response. These effects (i.e. reduction in gain and frequency offsets) can be attributed to the parasitic effects associated with the fabricated chip and measurement setup. The measured S11 is better than -10dB input return loss for all frequency bands. A minimum value of -13.5dB at the 3.5GHz band and a maximum of -12dB at the 1.8GHz band were recorded. The measured S11 compared to the simulated values (a minimum value of -16.3dB at the 1.8GHz band and a maximum of -14.3dB at the 5.2GHz band) are lower and have slight frequency offsets due to effects mentioned earlier.

3.5.2 Noise Figure Testing and Results

The noise figure measurement was done using the Y Factor method[40]. The setup for the NF measurement is shown in Figure 3-26. An excess noise ratio (ENR) source is needed. The ENR head usually requires a high DC voltage supply. The ENR (HP346C) has a standard noise figure parameter of it's own at specified frequencies. An example table is given in Table 3-6.

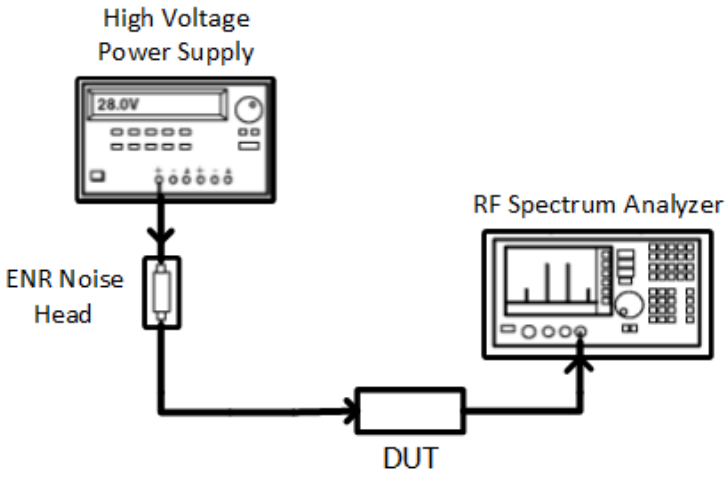


Figure 3-26: Noise figure measurement setup

Table 3-6 : ENR of HP346C noise head[40]

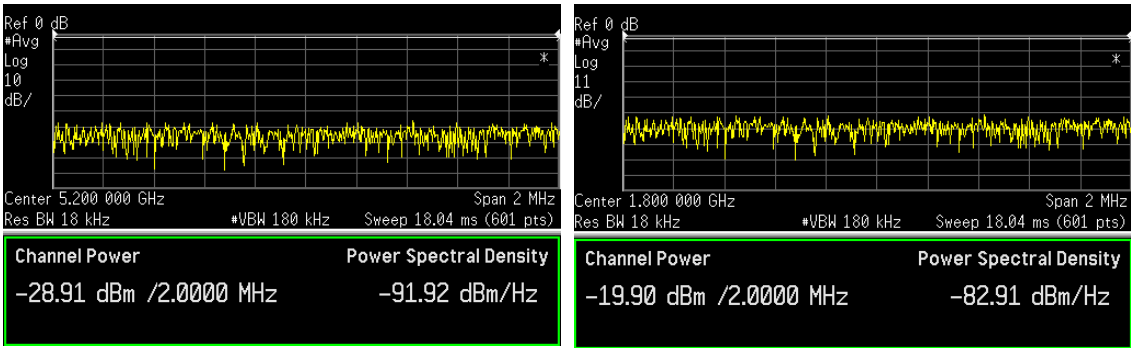
Frequency(GHz)	ENR (dB)
1	12.92
2	12.88
3	12.81
4	12.79
5	12.95

The NF is determined by measuring the output noise power spectral density corresponding to the noise source ON(Fig. 3-27(a)) and the noise source OFF(Fig. 3-27(b)) using the

spectrum analyzer. The change in the noise power density is the Y factor. The noise figure is calculated as[40] :

$$Noise\ Figure\ (NF) = 10 * log_{10}\left(\frac{10^{(ENR/10)}}{10^{(Y/10)}-1}\right) \qquad 3-8$$

Using the above formula, the NF at frequencies within the bandwidths of the four frequency bands(1.8GHz, 2.4GHz, 3.5GHz and 5.2GHz) are calculated from the noise source ON output noise power spectral densities shown in Table 3-7.



(a) (b)

Figure 3-27: (a) noise power spectral density for noise source OFF case, (b)noise power spectral desnity for noise source ON case at 1.8GHz

The measured NF at the four bands are shown in Figure 3-28. The minimum NF measured is 2.8dB at 1.8GHz and the maximum is 4.3dB at 5.2GHz. The measured NF for all bands are worse compared to the simulation results (minimum of 2.1dB at 1.8GHz and maximum

of 3.8dB at 5.2GHz. This can be attributed to parasitic effects of the fabricated chip and measurement setup.

Table 3-7: On-case noise power spectral density for four center frequencies

Frequency(GHz)	Noise power spectral density(dBm/Hz)
1.8	-82.91
2.4	-83.93
3.5	-84.93
5.2	-85.34

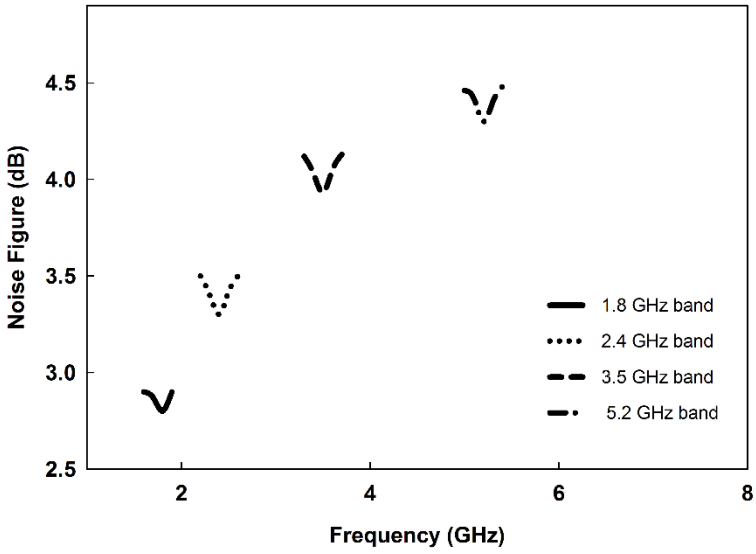


Figure 3-28: Measured noise figure for various bands

3.5.3 Linearity Testing

To measure the linearity of the LNA, two RF signal generators, an RF power combiner and a spectrum analyzer are required, as illustrated in Figure 3-29. The measures of linearity include both P1dB and IIP3 measurements. The P1dB is measured by turning off one signal generator and sweeping the other generator power level from -50dBm to 0dBm at the desired frequency. The output power level is measured by the spectrum analyzer.

When measuring the IIP3, two tones generated by two RF generators are used. The output signal spectrum measured for various bands are shown in Figure 3-30. In this test, two RF tones, 50MHz apart were generated and used as the input signals to the LNA. The output spectrums shown in Figure 3-30 illustrate the output effects at the various bands of operation. For example, Figure 3-30(a) shows the output spectrum when two tones at 1.85GHz and 1.9GHz are passed through the LNA. It shows the output tones at the said frequencies and in addition, the IM3 signal at 1.8GHz. Similar tests are done for the frequencies, 2.4GHz, 3.5GHz and 5.2GHz (Fig. 3-30(b) through (d)).

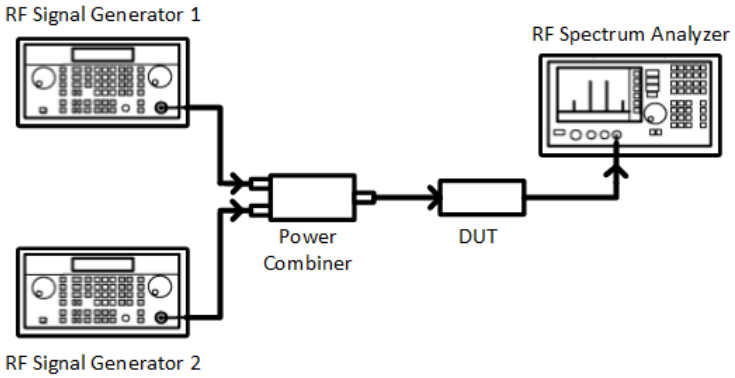
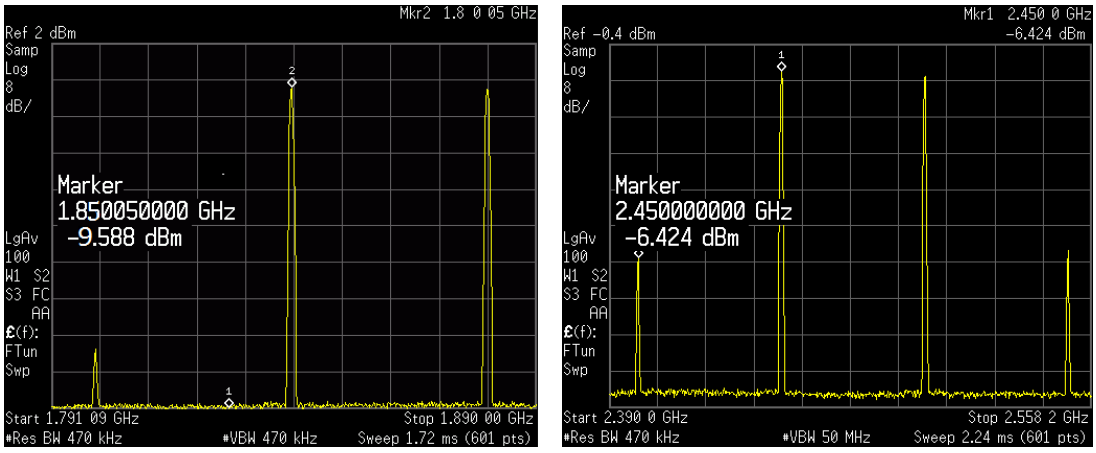
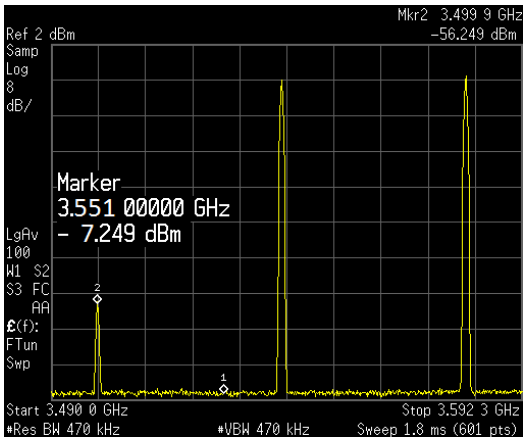


Figure 3-29: Linearity measurement Setup

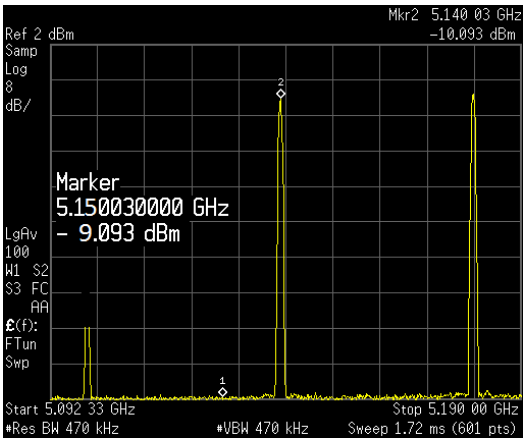


(a) (b)

Figure 3-30: (a) Output spectrum of DUT at 1.85 GHz (b) output spectrum of DUT at 2.45 GHz (c) output spectrum of DUT at 3.55 GHz (d) output spectrum of DUT at 5.15 GHz



(c)



(d)

Figure 3-30: continued.

The IIP3 and P1dB for the four bands are determined from the output spectrums shown in Figure 3-30. The results of the linearity measurements for the various bands are summarized in Table 3-8. The minimum IIP3 measured is -7.1dBm at the 2.4GHz band where the highest gain of 13.43dB occurs and the maximum is -3.5dBm at the 1.8GHz band where the lowest gain of 10.1dB occurs. The IIP3 at the 3.5GHz band which has a gain of 12dB, is -6.2dBm and that at the 5.2GHz band which has a gain of 10.43dB, is -4.34dBm. This IIP3 variation with frequency illustrates the relation between gain and linearity; the higher the gain, the better the linearity and vice versa. The measured IIP3 results are better than the simulated IIP3 results(maximum of -7.3dBm at 1.8GHz and minimum of -8.5dBm at 2.4GHz) due to the general decrease in the gains at the four bands

of the fabricated LNA. The minimum P1dB -16.9dBm at the 2.4GHz band and the maximum is -13.5dBm at the 1.8GHz bands. The measured P1dB are also better compared to simulated results (minimum of -17.8dBm at 2.4GHz and maximum of -16.5dBm at 1.8GHz) for similar reasons.

Table 3-8 : Linearity results

Frequency Band	IIP3 @ 50 MHz offset (dBm)	P1dB (dBm)
1.8 GHz	-3.45	-13.51
2.4 GHz	-7.12	-16.91
3.5 GHz	-6.2	-16.5
5.2 GHz	-4.34	-14.21

3.6 Discussion of Results

From the results above, the proposed LNA achieves S21 of between 10.1dB and 13.43dB. It achieves an input matching (S11) between -13.44 dB and -11.97 dB. The noise figure measured ranges from 2.8 dB to 4.3 dB for the four bands of interest. The LNA also achieves an IIP3 from -7.12 dBm to -3.45 dBm at 50 MHz offset. It also achieves a minimum P1dB of -16.9dBm and a maximum P1dB of -13.4dBm. The total power consumption ranges from 7mW to 7.2mW at a supply of 1.8V.

Table 3-9 summarizes the performance of the fabricated LNA.

Table 3-9 : Performance summary of LNA

Frequency (GHz)	1.8	2.4	3.5	5.2
S21(dB)	10.1	13.5	12	10.43
S11(dB)	-12	-12.6	-13.5	-12.5
NF (dB)	2.8	3.3	3.9	4.3
IIP3 (dBm)	-3.45	-7.1	-6.2	-4.33
P1dB(dBm)	-13.4	-16.9	-16.4	-14.2
Power(mW)	7.2	7.04	7.11	7.15
Supply(V)	1.8V			
Technology	CMOS 0.18um			

4. CONCLUSIONS AND FUTURE WORKS

This thesis focussed on the design and fabrication of a narrow band reconfigurable LNA for SDR applications. The design was done using IBM CMOS 0.18um technology. The proposed LNA is able to cover a wide frequency range from 1.8 GHz to 5.2 GHz for four bands.

In section 2, a conscise discussion of some basic RF fundamentals was presented. LNA topologies ranging from common source to common gate architectures were discussed. The section was ended with a comprehensive literature review of some works on reconfigurable LNA.

In section 3, the proposed LNA was presented. The stages of the LNA from the input stage to the output stage and the digital control circuit were discussed. The sizing of the transistors and the design of the passives were fully covered in the same section. The post-layout simulations/results of the LNA were discussed. The section concluded with discussion of measurement results. The RF testings included gain test, noise figure test and linearity tests. The LNA achieved S21 of between 10.1dB and 13.43dB. It achieved an input matching (S11) between -13.44 dB and -11.97 dB. The noise figure measured ranged from 2.8 dB to 4.3 dB. The LNA also achieved an IIP3 from -7.12 dBm to -3.45 dBm at 50 MHz offset. The power consumption ranged from 7 mW to 7.2 mW. The LNA is compared with some previous works in Table 4-1.

Table 4-1: Comparison table

	[3]	[34]	[35]	[36]	[37]	This Work
Freq(GHz)	1.9-2.4	2.45/6	2.8/3.3/4.6	1.8-2.4	2.4/3.43/3.9 6/4.49/5.4	1.8/2.4/3.5/5.2
Tuning Method	continuous	discrete	discrete	continuous	discrete	discrete
Gain(dB)	10-14	9.4-18.9	14.2-16.1	20.6-22.1	22-24	10.1-13.4
NF(dB)	3.2-3.7	2.8-3.8	2.4-3.7	3.2 - 3.5	2.2-3.1	2.8-4.3
IIP3(dBm)	-6.7	-4– -5.6	-4– -2	-16 –11.8	-16– -21	-7 to -3.4
Power (mW)	17	2.79	6.4	9.6	4.6	7-7.2
Technology	CMOS 0..13um	CMOS 0.13um	CMOS 0.13um	CMOS 0.18um	CMOS 0.13um	CMOS 0.18um

The major advantage of this work is it's ability to cover a wide range of discretely tuned frequency bands (i.e 1.8GHz, 2.4GHz, 3.5GHz and 5.2GHz) as opposed to the relatively small frequency ranges covered by [3] (1.9GHz to 2.4GHz), [34] (2.45GHz and 6GHz), [35] (2.8GHz, 3.3GHz and 4.6GHz) and [36] (1.8GHz-2.4GHz). Although [37] covers a similarly wide frequency range (2.4GHz, 3.43GHz, 3.9GHz, 4.49GHz and 5.4GHz), the proposed LNA in this thesis has and additional advantage of discretely tuning the input matching.

In terms of gain, this work compares well with [3] (10dB-14dB), however, the works [34] (S21 of 9.8dB and 18.9dB), [35] (S21 of 14.2dB-16.1dB), [36] (S21 of 20.6dB-22.1dB) and [37] (S21 of 22dB-24dB) have better performance. The NF of this work

(2.8-4.3dB) compares greatly with the previous works. Also, the IIP3 of this work(-7dBm to -3.45dBm) is better compared to [35] (-16dBm to -11.8dBm) and [37] (-21dBm to -16dBm). Above all, it is noted that [34], [35] and [37] achieve better gain and NF performances while having pretty low power consumptions (2.79mW, 6.4mW and 4.6mW) due to the better technology (CMOS 0.13um) that these works use. The only exception is [3] which even though uses CMOS 0.13um, has a power consumption of 17mW. It can be concluded that, if this work is in the future redesigned and fabricated in CMOS 01.3um, it can achieve a much better performance.

The LNA currently achieves discrete tuning of the input matching and output frequency response. As a result, variations due to process and temperature can affect the S11 and S21 value and can also cause frequency shifts. To account for these, a complementary continuous tuning scheme will be added. This will be implemented by adding a fifth current source whose bias can be continuously tuned thus, continuously varying the current through the source follower, M_{FB} to compensate for the shifts in the S11. Also, a continuous tuning scheme in the form of voltage controlled varactor will be added in parallel to the two output tanks to compensate for the variations due to process and temperature. In addition, a switchable bank of transistors will be added in parallel to the input transistor to allow gain tuning. These are highlighted in Figure 4-1.

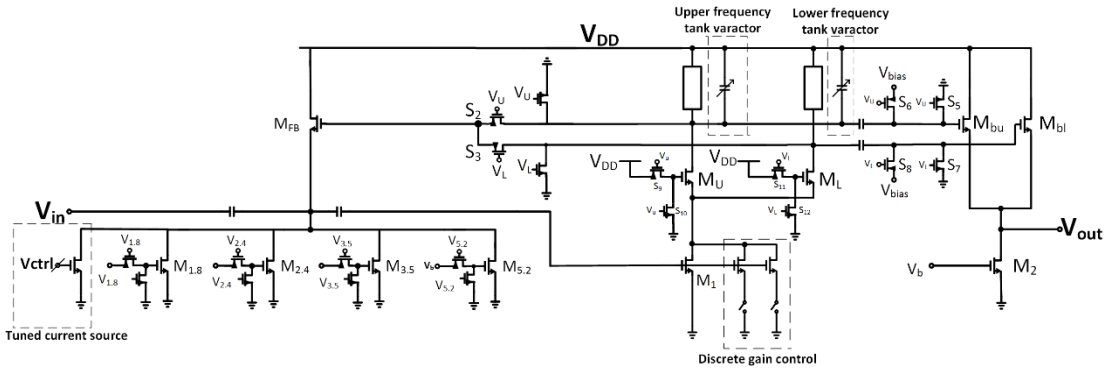


Figure 4-1: Complete schematic of LNA showing future works

REFERENCES

[1] J. H. C. Zhan, B. R. Carlton, and S. S. Taylor, "A broadband low-cost direct-conversion receiver front-end in 90 nm CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 43, pp. 1132-1137, 2008.

[2] M. Brandolini, P. Rossi, D. Manstretta, and F. Svelto, "Toward multistandard mobile terminals - fully integrated receivers requirements and architectures," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 53, pp. 1026-1038, 2005.

[3] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A CMOS low-noise amplifier with reconfigurable input matching network," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 57, pp. 1054-1062, 2009.

[4] S. F. R. Chang, C. Wen-Lin, C. Shuen-Chien, T. Chi-Kang, W. Chang-Lin, C. Chih-Hung, *et al.*, "A dual-band RF transceiver for multistandard WLAN applications," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 53, pp. 1048-1055, 2005.

[5] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *Solid-State Circuits, IEEE Journal of,* vol. 33, pp. 2178-2185, 1998.

[6] C. Dongpo, P. Wenjie, J. Peichen, J. Jing, M. Tingting, and Z. Jianjun, "Reconfigurable dual-channel multiband RF receiver for GPS/Galileo/BD-2 systems," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 60, pp. 3491-3501, 2012.

[7] B. Razavi. (2011). *RF microelectronics (2nd ed.)*,Prentice Hall; New Jersey.

[8] M. Dillinger, K. Madani, and N. Alonistioti, *Software defined radio : architectures, systems and functions*, Wiley, 2003; Hoboken, NJ.

[9] A. Grebennikov, *RF and microwave transmitter design*, 2011,Wiley;New Jersey.

[10] E. Da Silva, *High frequency and microwave engineering*, 2001,Newnes;Oxford.

[11] T. H. Lee, *The design of CMOS radio-frequency integrated circuits*, 2nd ed. Cambridge .

[12] W. Zhuo, J. P. de Gyvez, and E. Sanchez-Sinencio, "Programmable low noise amplifier with active-inductor load," in *Circuits and Systems, 1998. ISCAS '98. Proceedings of the 1998 IEEE International Symposium on*, 1998, pp. 365-368 vol.4.

[13] R. Akbari-Dilmaghani and A. Payne, "An RF CMOS differential bandpass amplifier using an active inductor," in *Systems on a Chip (Ref. No. 1998/439), IEE Colloquium on*, 1998, pp. 16/1-16/6.

[14] B. Tenbroek, J. Strange, D. Nalbantis, C. Jones, P. Fowers, S. Brett, *et al.*, "Single-chip tri-band WCDMA/HSDPA transceiver without external SAW filters and with integrated TX power control," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 202-607.

[15] S. Mehta, M. Zargari, S. Jen, B. Kaczynski, M. Lee, M. Mack, *et al.*, "A CMOS dual-band tri-mode chipset for IEEE 802.11a/b/g wireless LAN," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2003 IEEE*, 2003, pp. 427-430.

[16] S. Arshad, F. Zafar, and Q. Wahab, "Design of a 4-6GHz wideband LNA in 0.13um CMOS technology," in *Electronics Design, Systems and Applications (ICEDSA), 2012 IEEE International Conference on*, 2012, pp. 125-129.

[17] Z. Heng, F. Xiaohua, and E. S. Sinencio, "A low-power, linearized, ultra-wideband LNA design technique," *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 320-330, 2009.

[18] Y. Jehyung, P. Changjoon, S. Heesong, C. Inyoung, and B. Kim, "A wideband LNA with dual-feedback for TV tuner," in *Microwaves, Communications, Antennas and Electronics Systems, 2009. COMCAS 2009. IEEE International Conference on*, 2009, pp. 1-4.

[19] T. Torikka, D. Xinzhong, Z. Li-Rong, E. Tjukanoff, and H. Tenhunen, "Chip-package co-design of a concurrent LNA in system-on-package for multi-band radio applications," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 1687-1692 Vol.2.

[20] E. Kargaran and B. Madadi, "Design of a novel dual-band concurrent CMOS LNA with current reuse topology," in *Networking and Information Technology (ICNIT), 2010 International Conference on*, 2010, pp. 386-388.

[21] C. P. Moreira, E. Kerheve, P. Jarry, and D. Belot, "A concurrent fully-integrated LNA for W-LAN IEEE 802.11b/g/a applications," in *Microwave Conference, 2006. 36th European*, 2006, pp. 1552-1555.

[22] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 50, pp. 288-301, 2002.

[23] F. Chang-tsung, K. Chun-Lin, K. Chien-Nan, and Y. Z. Juang, "A 2.4-5.4-GHz wide tuning-range CMOS reconfigurable low-noise amplifier," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 56, pp. 2754-2763, 2008.

[24] D. Vu Kien, B. Quang-Diep, and P. Chul-Soon, "A multi-band 900MHz/1.8GHz/5.2GHz LNA for reconfigurable radio," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE*, 2007, pp. 69-72.

[25] C. L. Kok, M. T. Mustaffa, N. M. Noh, A. A. Manaf, and O. Sidek, "A switchable CMOS LNA using capacitor switching," in *Computer Applications and Industrial Electronics (ICCAIE), 2011 IEEE International Conference on*, 2011, pp. 117-120.

[26] P. Jaewoo, K. Shin-Nyoung, S. Ji-Hwan, R. Yong-Seong, Y. Changsik, L. Kyoohyun, *et al.*, "A direct-conversion CMOS RF receiver reconfigurable from 2GHz to 6GHz," in *VLSI Circuits, 2008 IEEE Symposium on*, 2008, pp. 38-39.

[27] A. Taibi, A. Slimane, M. T. Belaroussi, S. A. Tedjini, and M. Trabelsi, "Low power and high linear reconfigurable CMOS LNA for multi-standard wireless applications," in *Microelectronics (ICM), 2013 25th International Conference on*, 2013, pp. 1-4.

[28] S.-S. Yoo and Y. Hyung-Joun, "A compact dualband LNA using self-matched capacitor," in *Radio-Frequency Integration Technology, 2007. RFIT 007. IEEE International Workshop on*, 2007, pp. 227-230.

[29] M. B. Vahidfar and O. Shoaei, "A triple mode LNA enhanced by dual feedback loops for multi standard receivers," in *Circuits and Systems, 2006. MWSCAS '06. 49th IEEE International Midwest Symposium on*, 2006, pp. 159-162.

[30] L. Xiaoyong, S. Shekhar, and D. J. Allstot, "Low-power gm-boosted LNA and VCO circuits in 0.18 um CMOS," in *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, 2005, pp. 534-615 Vol. 1.

[31] L. Zhangfa and W. Jing, "A 0.18um CMOS reconfigurable multi-band multi-gain low noise amplifier," in *Electric Information and Control Engineering (ICEICE), 2011 International Conference on*, 2011, pp. 961-964.

[32] P. Anh-Tuan and R. Farrell, "Reconfigurable multiband multimode LNA for LTE/GSM, WiMAX, and IEEE 802.11.a/b/g/n," in *Electronics, Circuits, and Systems (ICECS), 2010 17th IEEE International Conference on*, 2010, pp. 78-81.

[33] R. Beare, C. Plett, and J. Rogers, "Highly reconfigurable single-ended low noise amplifier for software defined radio applications," in *New Circuits and Systems Conference (NEWCAS), 2012 IEEE 10th International*, 2012, pp. 549-552.

[34] N. M. Neihart, J. Brown, and Y. Xiaohua, "A dual-band 2.45/6 GHz CMOS LNA utilizing a dual-resonant transformer-based matching network," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 59, pp. 1743-1751, 2012.

[35] Y. Xiaohua and N. M. Neihart, "Analysis and design of a reconfigurable multimode low-noise amplifier utilizing a multitap transformer," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 61, pp. 1236-1246, 2013.

[36] A. Slimane, F. Haddad, S. Bourdel, B. Tedjini, x, S. A. liche, *et al.*, "Compact inductorless CMOS low-noise amplifier for reconfigurable radio," *Electronics Letters*, vol. 50, pp. 892-893, 2014.

[37] F. Chang-tsung, K. Chun-Lin, and K. Chien-Nan, "A 2.4 to 5.4 GHz Low power CMOS reconfigurable LNA for multistandard wireless receiver," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2007 IEEE*, 2007, pp. 65-68.

[38] S. Andersson, C. Svenson, and O. Drugge, "Wideband LNA for a multistandard wireless receiver in 0.18um CMOS," in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, 2003, pp. 655-658.

[39] B. Razavi, T. Aytur, C. Lam, Y. Fei-Ran, L. Kuang-Yu, Y. Ran-Hong, *et al.*, "A UWB CMOS transceiver," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 2555-2562, 2005.

[40] Agilent.com, "Noise figure measurement accuracy –The Y-Factor method," p. 45, February 26th, 2014 .