HIGH-K BASED NON-VOLATILE MEMORY DEVICES WITH THE LIGHT EMITTING APPLICATION

A Dissertation

by

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ABSTRACT

The zirconium-doped hafnium oxide (ZrHfO) high-k gate dielectric films with and without the embedded nanocrystals have been studied for the applications of the nonvolatile memory and light emitting devices. By replacing the polycrystalline Si with the novel discrete nanocrystal embedded high-k ZrHfO structure, the promising memory functions can be expected. On the other hand, by using the same metal oxide semiconductor (MOS) capacitor structure with ZrHfO gate dielectric layer but different operating gate voltage (V_g) ranges, e.g., when V_g is larger than the breakdown voltage (V_{BD}), the device starts emitting the white light. This new solid state incandescent light emitting device (SSI-LED) unveils a new concept for the future LED evolution.

The nanocrystals cadmium selenide (nc-CdSe) and molybdenum oxide (nc-MoO_3) embedded ZrHfO on the p-type silicon wafer have been fabricated by self-assembly process and studied for their charge trapping, detrapping, and retention characteristics. Moreover, the temperature effect on the memory function has been investigated on the nc-MoO_3 embedded device. More than half of the originally trapped holes can be retained in the CdSe nanocrystals for more than 10 years. For the temperature test, with the increase of temperature, the memory window was enlarged and the Coulomb blockade effect was suppressed in the nc-MoO_3 embedded ZrHfO memory device. At the same time, the interface quality was deteriorated, the leakage current was increased, and the lifetime was shortened.

The light emission characteristics of the new SSI-LED composed of the ZrHfO or WO_3 thin film have been investigated. The light emitting principle is based on the thermal excitation of the conductive paths formed after the dielectric breakdown, which is different from the electron-hole or exciton radiative recombination mechanism in conventional LEDs. The emission spectrum covers the visible to the near IR wavelength range with the color rendering index of 98.4. The light intensity can be enhanced by embedding CdSe nanocrystals into the ZrHfO dielectric layer due to the increase of the defect density which causes the enhancement of the leakage current. The SSI-LED has a very long lifetime of > 5,664 hours in the atmosphere.

Lastly, the additive gas effect of a plasma-based process for etching the copper film over a near-vertical step has been investigated. A new process that minimizes the excessive attacks of the cusp region was developed.

DEDICATION

This dissertation is gratefully dedicated to my beloved father Chan-Yie Lin, mother Ming-Yie Hsiao, and brother Chi-Yu Lin

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CHAPTER I

INTRODUCTION

1.1 High-K Gate Dielectrics

1.1.1 Why High-K Gate Dielectrics?

Due to the rapid growth of the complementary metal oxide semiconductor (CMOS) integrated circuit (IC) technology since the late 1980's, the downsizing of the silicon-based metal oxide semiconductor field effect transistor (MOSFET) has drawn much wider attention.[1] For achieving the greater device performance and lower cost in the IC fabrication, the higher density of transistors on a single wafer is required. Figure 1 shows the illustration of the typical nMOSFET.[2] The rapid shrinking on the feature size of the transistors has forced the channel length (L) to decrease rapidly, which increases the switching speed and results in a larger drive current (I). The drive current of the nMOSFET can be expressed as the following equation:[3]

$$I = \frac{W}{L} \mu C_{ox} (V_{GS} - V_T) V_{DS} \qquad [1]$$

where W is the width of the transistor channel, μ is the channel carrier mobility, C_{ox} is the capacitance density associated with the gate dielectric when the underlying channel is in the accumulated state, V_{GS} and V_{DS} are the gate to source and drain to source voltages, respectively, and the threshold voltage is given by V_T.

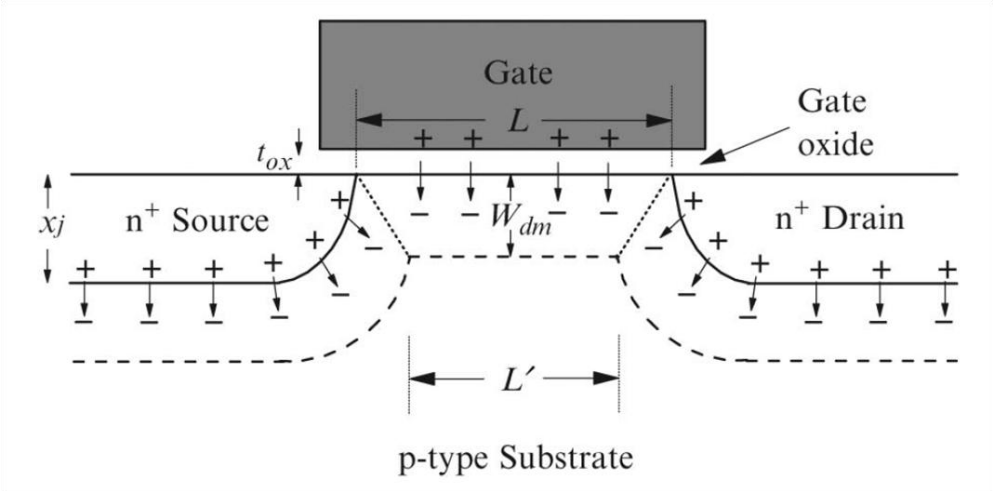


Figure 1. Schematic diagram of nMOSFET.[2]

According to equation 1, the drive current can be increased by shrinking the L or increasing the C_{ox}. However, when the L is decreased, the gate area is decreased simultaneously, which reduces the gate capacitance C_{ox} calculated from the following equation:[1]

$$C_{ox} = \frac{k\varepsilon_0 A}{d} \qquad [2]$$

where ε_0 is the vacuum permittivity (8.85×10^{-14} F/cm), and k is the dielectric constant. Therefore, in order to maintain the good control over the channel, the thickness (d) of the gate dielectric needs to be reduced.

The current CMOS gate dielectric, thermally grown silicon dioxide (SiO_2), has been used for decades because it offers several advantages such as the high energy band gap (E_g ~9 eV), high dielectric breakdown strength (~15 MV/cm), high amorphous-to-

polycrystalline temperature (> 1100 ^{o}C), low interface state density ($D_{it} < 10^{11}$ $eV^{-1}cm^{-2}$), and high conduction (3.5 eV) and valance band (4.4 eV) offsets with respect to Si.[1, 4-5] The current CMOS gate dielectric SiO_2 thickness can be scaled down to at least 1.3 nm,[1] however, the gate leakage current becomes very large due to the direct tunneling effect and at the same time, the power consumption and device reliability will be the concerns. Therefore, some device parameters must be adjusted during this scaling process. According to Figure 2,[6] the direct tunneling occurs when the d is smaller than 3 nm and the gate leakage current increases by two orders as lowering SiO_2 film thickness by each 0.5 nm. The high-k material is needed when the d is shrunk to below 1.3 nm.

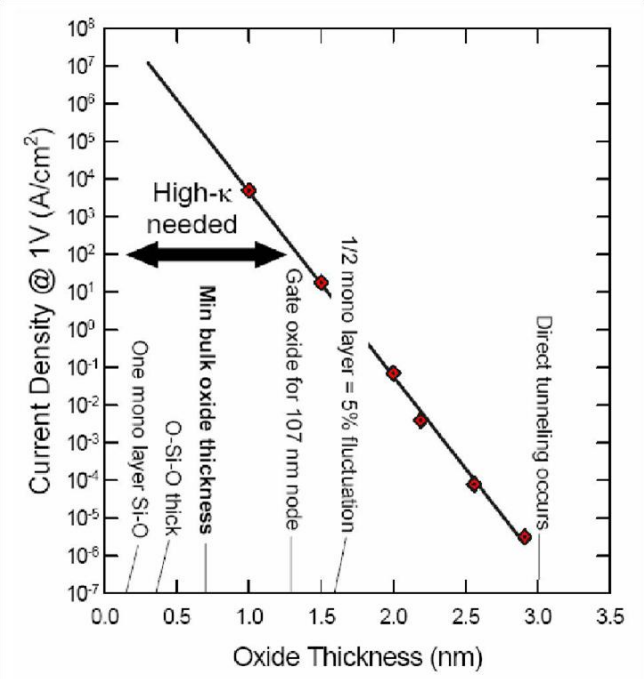


Figure 2. Direct tunneling current in thin SiO_2.[6]

The gate leakage current must be reduced without compromising the drive current. Therefore, the high-k metal oxide, such as HfO_2, ZrO_2, Ta_2O_5, La_2O_3, etc. has been proposed to replace the thermally grown SiO_2 for obtaining the high C_{ox} with the thicker physical thickness, maintaining the good gate control, low gate leakage current and sufficiently large drive current.

1.1.2 HfO_2 High-K Gate Dielectric

Although the high-k gate dielectric is a trend for replacing the thermally grown SiO_2, there are some requirements for choosing the high-k materials such as: compatible with CMOS manufacturing process, thermodynamically stable in contact with Si, reasonable range of the k value, $E_g > 5$ eV, etc. The k value has the following relationship with the E_g:[7]

$$E_g \sim k^{-} \cdot \quad [3]$$

If the k value is small, the equivalent oxide thickness (EOT) cannot be effectively reduced, which is not favorable for the device scaling process. The EOT can be estimated by the following equation:[1]

$$EOT \quad \frac{k_{ox}}{k_{high\text{-}k}} d_{high\text{-}k} \quad [4]$$

where k_{ox} is the dielectric constant of the SiO_2, i.e., 3.9, $k_{high\text{-}k}$ and $d_{high\text{-}k}$ are the dielectric constant and physical thickness of the high-k film, respectively. On the other hand, if the k value is too large, it will result in excessive direct tunneling currents due to the small E_g. Most work showing promising EOT-leakage current characteristics have been achieved with k value ranging from 20 to 30.[7] Figure 3 shows the relationship

between the k value and E_g of several gate dielectric candidates.[8] Judged from the requirements of high-k materials and Fig. 3, the hafnium oxide (HfO_2), zirconium oxide (ZrO_2) and lanthanum oxide (La_2O_3) films are likely the best high-k candidates because they have relatively high E_g's (> 5 eV) and suitable k values (~20-30).

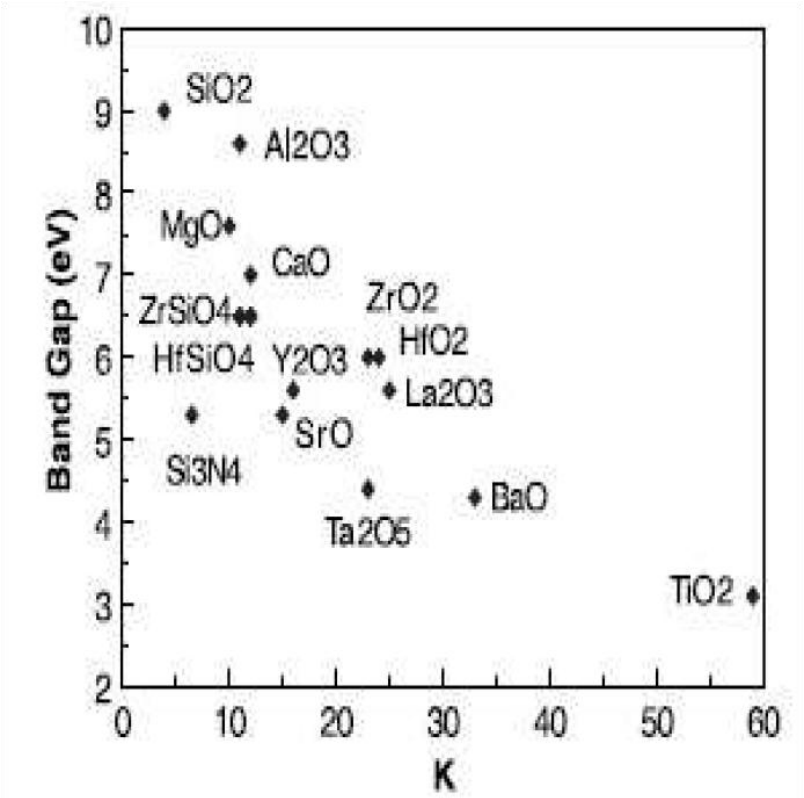


Figure 3. Dielectric constant versus band gap for candidate high-k gate oxides.[8]

The thermal stability is important because a high temperature post deposition annealing (PDA) process is required in the fabrication of the MOSFET.[9] If the high-k film is not thermally stable, the amorphous-to-polycrystalline phase transition may occur

and the diffusion paths through the grain boundaries can be created.[10] In this case, the gate leakage current is greatly increased.[11-12] Since the high-k film needs to be deposited on top of the Si substrate instead of thermally grown from the Si directly, the interface layer quality between the high-k film and the Si substrate is substantial to the MOSFET. The interface layer can be formed from the reaction of the diffused metal atoms with Si and O or the high-k film may directly react with the Si substrate to form the metal silicide during the deposition or PDA process.[13] The interface layer formed between the high-k film and Si wafer has a relatively low k value. Therefore, how to inhibit the interface layer formation or obtain the minimized interface state density (D_{it}) has been an important research topic.[14-16] Figure 4 shows the D_{it} of the HfO_2 and La_2O_3 films deposited on the Si substrate.[17] Under the same PDA condition, i.e., 500°C, the D_{it} with the La_2O_3 film is much higher than that with the HfO_2 film. Therefore, the La_2O_3 is not considered to be used as the gate dielectric in this study.

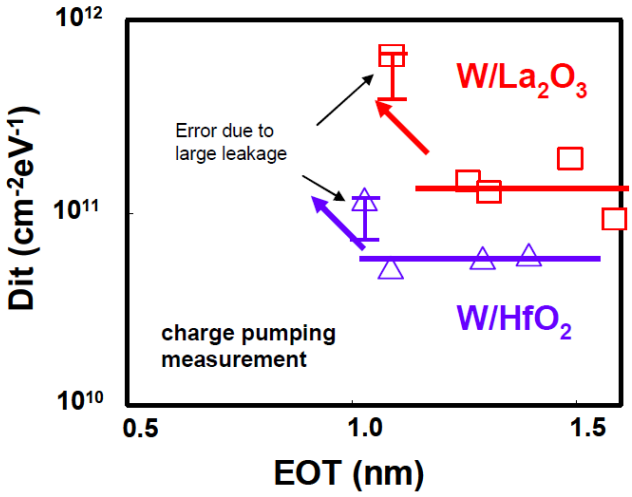


Figure 4. D_{it} of La_2O_3 and HfO_2.[17]

As mentioned in the previous paragraph, the high-k gate dielectric directly contacts with the Si substrate and therefore, its band alignments, i.e., the conduction band and valance band offsets with respect to Si, are strongly related to the carrier transport phenomenon. Usually, a large band offset favors a low gate leakage current.[18] The reported band alignments of the important high-k gate dielectric candidates are shown in Figure 5.[19] HfO_2 and ZrO_2 have the conduction and valance band offsets of 1.5 eV and 3.4 eV and 1.4 eV and 3.3 eV, with respect to Si, respectively. This number is relatively larger than that of the other high-k candidates which have comparable k values such as tantalum oxide (Ta_2O_5).

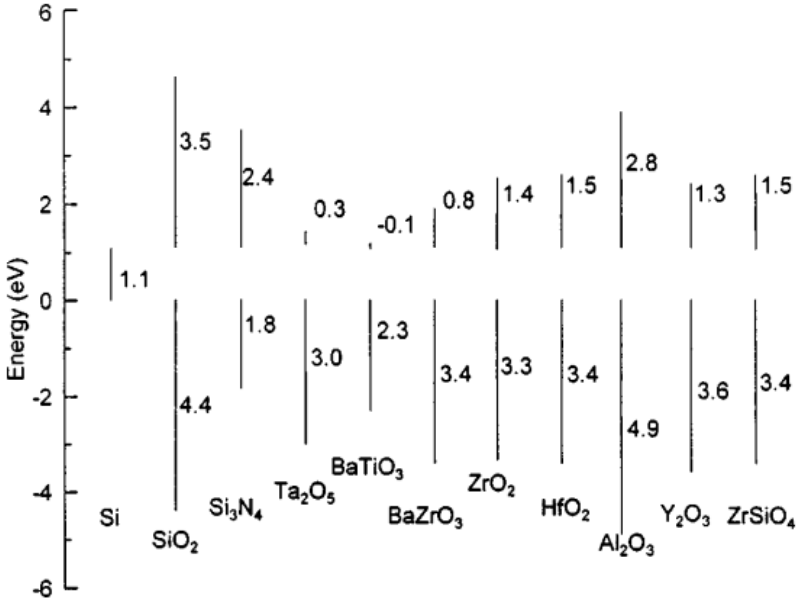


Figure 5. Calculated conduction band and valence band offsets of various oxides on Si.[19]

The chemistries of HfO_2 and ZrO_2 are nearly identical and both of them have been investigated extensively as the potential replacement of the SiO_2.[20] However, it has been reported that the ZrO_2 has larger propensity to form the silicide, i.e., ZrSi, than the HfO_2 does, since the formation of the silicide of the former is an exothermic reaction with the enthalpy change (ΔH) of 2 kJ/mol and of the latter is an endothermic reaction with the ΔH of 92 kJ/mol.[21] The formation of the metal silicide in between the high-k film and Si substrate will degrade the effective k value of increase the gate leakage current.[22] Moreover, the thermal expansion coefficient and self diffusion coefficient of the HfO_2 are both smaller than that of the ZrO_2 as shown in Table 1. Therefore, HfO_2 has more potential for the MOSFET application than ZrO_2 does.

Table 1. Thermal stability properties of HfO_2 and ZrO_2.[20-22]

	HfO_2	**ZrO_2**
Silicide formation ΔH (kJ/mol)	**92**	**-2**
Thermal expansion coefficient (10^{-6} K^{-1})	**5.3**	**7**
Self diffusion coefficient at 900 K	**$2.8x10^{-17}$**	**$6x10^{-10}$**

1.1.3 Zr-Doped HfO_2 (ZrHfO) High-K Gate Dielectric

As mentioned in the previous section, the HfO_2 has been studied extensively as the high-k gate dielectric because of its high k value, large electron and hole band offset respect to the Si compared to other high-k materials, and good thermal stability in contact with Si. However, there has a main drawback of the HfO_2 that the amorphous-to-crystalline transition happens at a relatively low temperature, i.e., 700^{o}C, which is a potential reliability problem.[23] Previously, it has been demonstrated that by adding a small amount of zirconium (Zr) into the Ta_2O_5 high-k gate dielectric can effectively increase the amorphous-to-crystalline temperature since the inclusion of the dopant in the film interferes the alignment of Ta_2O_5 molecules.[24] The amount of dopant is critical to the amorphous-to-crystalline temperature and crystalline structure. Since HfO_2 and ZrO_2 have similar gate dielectric properties, e.g., high k value, band gap, thermal stability, large band offsets, and other physical and chemical properties, they are totally miscible and hard to be separated in the solid solution as shown in Figure 6.[25] The crystallization temperature of the ZrHfO film is also expected to be higher than that of the un-doped HfO_2 film based on the similar theory as that in the Zr-doped Ta_2O_5. By adding small amount of Zr, i.e., 12 wt%, into the Hf target, i.e., 88 wt%, the ZrHfO high-k gate dielectric has been prepared by the sputtering machine under Ar/O_2 (1:1) atmosphere.[23] The ZrHfO gate dielectric showed much higher amorphous-to-crystalline temperature, i.e., > 900^{o}C, low EOT and D_{it} than the un-doped HfO_2. The 1.7 nm EOT has been obtained from the MOS capacitor with the ZrHfO gate dielectric film and TiN gate electrode.[26] Moreover, the sub-nanometer EOT, e.g., 0.97 nm, and low gate leakage

current, e.g., 10^{-1} A/cm^2 at V_g = -1 V, has been obtained from the sputter-deposited ZrHfO after 800°C pure N_2 PDA process as shown in Figure 7.[23] Therefore, the ZrHfO is a good high-k gate dielectric material and will be utilized in the study of this disseration for both nonvolatile memory and light emitting devices.

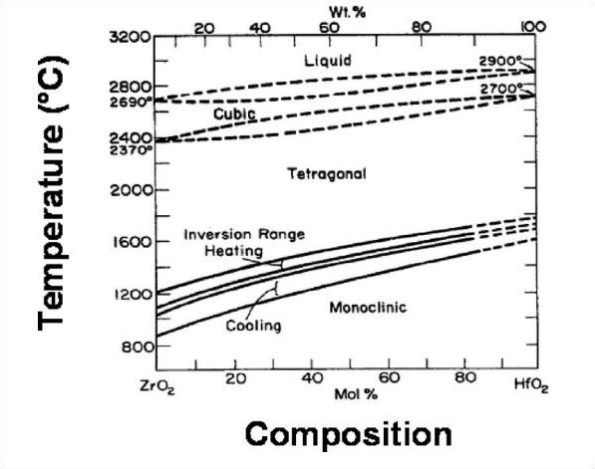


Figure 6. Temperature-composition phase of HfO_2-ZrO_2.[25]

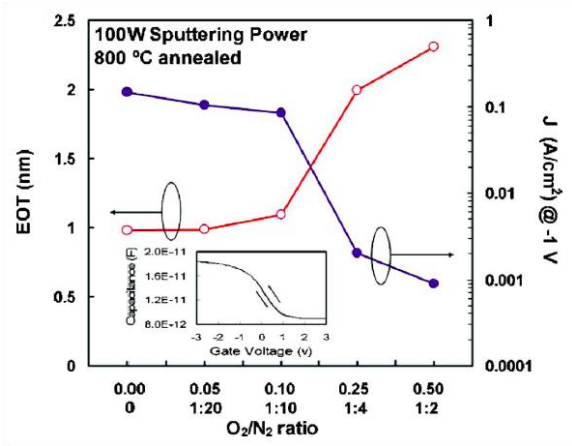


Figure 7. EOT and gate leakage current of ZrHfO films.[23]

1.2 Nanocrystal Nonvolatile Memory Device

1.2.1 Introduction of the Flash Nonvolatile Memory (NVM)

The flash NVM was firstly developed by Masuoka in 1984 when he was working in Toshiba and has been extensively studied for the past 30 years. The dominating NVM technologies in the industry today is the NAND flash because of the larger capacities, faster write and erase capabilities, and smaller erase units are required compared to the NOR flash. The definition of the NVM is that they are able to retain information even if the power supply is switched off. The memories are characterized by the two states, i.e., the written cell (logic " ") and the erased cell (logic "1"), based on the different threshold voltages (V_T) as shown in Figure 8 and the two states can be distinguished at least for 10 years.[27]

The flash NVM stores information in an array of memory cells, each cell resembles a standard MOSFET and the transistor is consisted of two gates, floating gate (FG) and control gate (CG). The FG structure was invented by Sze and Kahng at Bell Labs in 1967.[28] The FG is surrounded by the gate insulator as shown in Figure 9, which is electrically isolated.[29] Both writing and erasing operations will result in tunnel currents through the insulator 1. Therefore, the insulator 1 is named "tunnel oxide". The insulator 2 is usually thicker than the insulator 1 to prevent from the interactions between the FG and CG; thus, the insulator 2 is named "control oxide". The conventional FG is made of a continuous poly-Si layer, which acts as a potential well to trap charges when the CG is at the positive bias. As long as charges are trapped in this potential well, the cell is at the written state "0" and they will not escape without an

external electric field. When a negative bias is applied to the CG, the charges can be pulled off from the FG and the cell is at the erased state "1".[29]

Figure 10 shows a typical band energy diagram for a conventional FG device composed of poly-Si CG/control SiO_2/poly-Si FG/tunnel SiO_2/Si.[29] The FG is isolated from the exit or entry of charges by the high energy barrier between the conduction band of the poly-Si FG and the conduction bands of the control and tunnel SiO_2 layers. These barriers are much greater than the thermal energy, which can provide the nonvolatile retention of the charge. In order to program the charges into the FG, the potential of the FG relative to the potential on the opposite side of either SiO_2 layer needs to be changed until some conduction mechanisms are invoked to overcome the barrier. Two common conduction mechanisms, i.e., channel hot electron (CHE) injection and Fowler-Nordheim (FN) tunneling are involved. FN tunneling is a phenomenon through which electrons can easily tunnel through a triangular barrier induced by a high gate field. The CHE injection is the process through which an electron gains energy from an electric field and then collides with the lattice to redirect it into the charge storage layer.[30] The NOR devices typically use CHE injection to program the FG and FN tunneling to erase the FG. NAND devices employ the FN tunneling for both program and erase.[29]

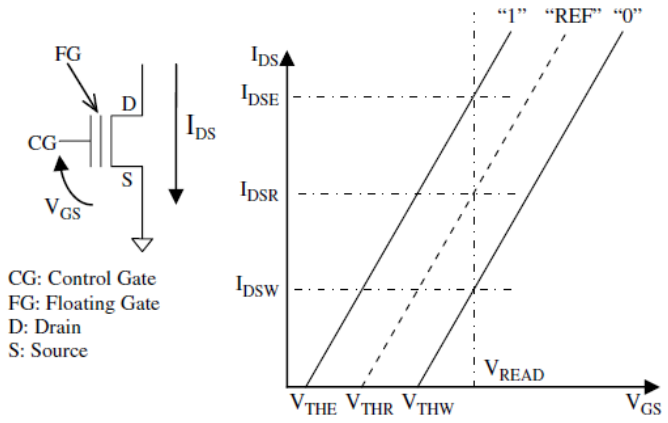


Figure 8. Current/voltage characteristics as a function of the threshold voltage of a flash cell.[27]

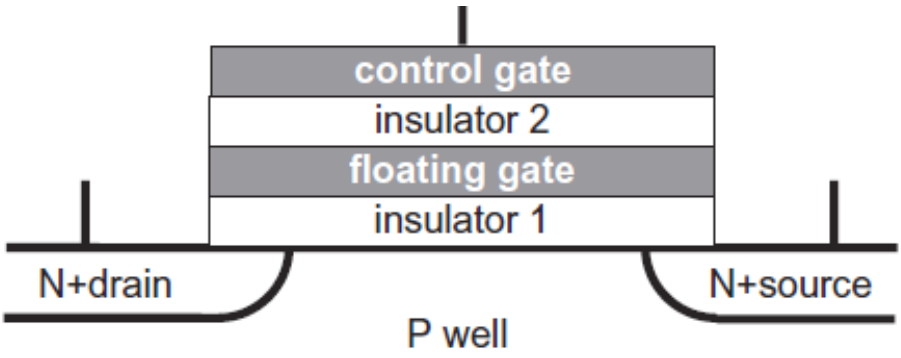


Figure 9. Schematic cross-sectional structure of flash memory core cell.[29]

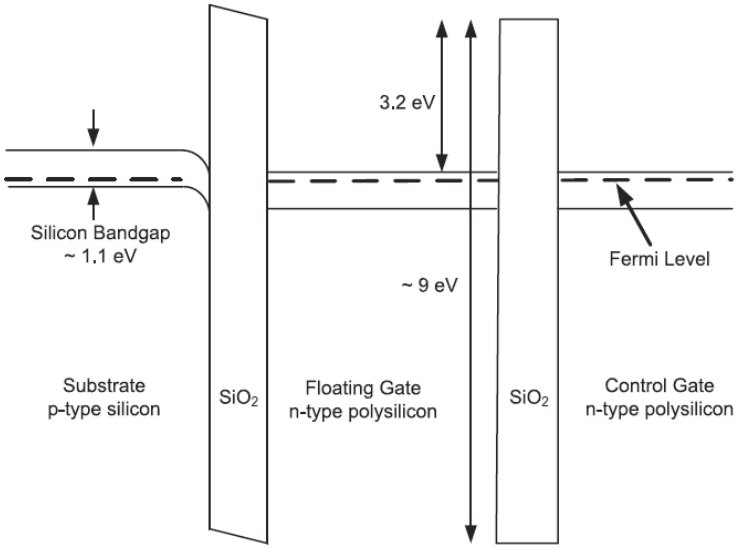


Figure 10. Energy band diagram for a typical FG structure.[29]

1.2.2 Nanocrystals Embedded FG Structure

In order to meet the Moor's law that the number of transistors in a dense IC doubles every two years,[31] the shrinking of transistors has been evolved as a method to not only pack more devices into a given area, but also improve the switching speed. In this situation, conventional poly-Si FG suffers from some limitations, such as an insufficient tunneling oxide thickness from the continual scaling down of the device structures.[30] Because the poly-Si FG is conductive, all charge will be lost if there forms a single leakage path in the tunnel oxide, resulting in a serious reliability issue for memory applications as shown in Figure 11.[32] Based on this intrinsic problem, the oxide layer thickness needs to be remained thick to prevent the charge loss. Discrete nanocrystal Si (nc-Si) NVM was first proposed by Tiwari in 1996 when he was working in IBM Watson Research Center.[33] If there forms a leakage path, only the charges stored in the

nanocrystal located at the leakage path will be drained as shown in Fig. 11. Therefore, the discrete nanocrystal NVM has been considered as a promising candidate for the solution of the scaling problem since 2000s. In addition, nanocrystal memory has a two bit per cell storage capability due to its discrete electron storing center. This means that more data can be stored in one memory cell, which readily increases the memory density.[30] The density of the stored charges (Q) can be estimated by measuring the threshold voltage shift (ΔV_T) of the memory device, then calculated from the below equation:[34]

$$\Delta V_T \quad \frac{npq}{\varepsilon_{tun}} \left(t_{control} \quad \frac{\varepsilon_{tun} t_{nc}}{2\varepsilon_{Si}}\right) \qquad [5]$$

where n is the nanocrystal number density, p is the average number of electrons stored per nanocrystal, q is the electronic charge, ε_{tun} represents the tunnel oxide dielectric constant, t_{nc} is the nanocrystal diameter, and $t_{control}$ represents the control oxide thickness. For storing a given number density of electrons, np, the defects in the tunnel oxide is mitigated by having a higher density (n) of nanocrystals and smaller number of electrons stored per nanocrystal (p). For nanocrystals to be sufficiently electrically isolated with respect to tunneling transport, their typical separation must be greater than about 4 nm from one another. Having the minimal area fraction of nanocrystals mitigates the probability of defects underlying any nanocrystal.[34] In nanocrystal memory, information is stored and removed on the same theory as the FG based NVM, i.e., FN tunneling and CHE injection. Nanocrystal flash memory has been demonstrated commercially, such as in Freescales's 9 nm node embedded nanocrystal flash memory and 128 KB NOR split gate nanocrystal memory.[35-36]

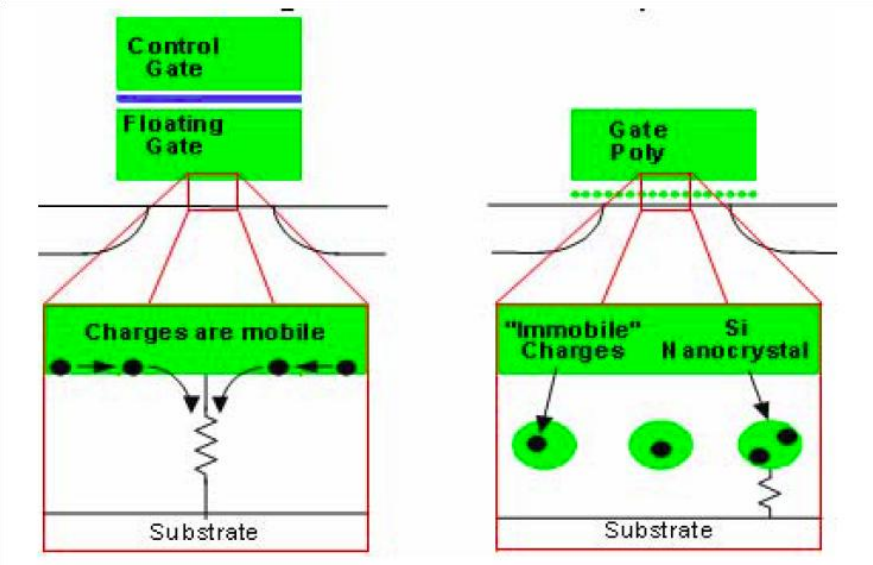


Figure 11. Schematic diagram illustrates how a defect chain affects the charge loss in conventional FG structure and nanocrystal FG structure.[32]

1.2.3 Fabrication of Nanocrystals Embedded FG NVM

In general, a nanocrystal FG NVM is fabricated as follows. First, a silicon (100) wafer is cleaned by the Radio Corporation of America (RCA) standard cleaning process to remove the native SiO_2, organic contaminants, and ionic contamination from the wafer surface.[37] A high quality oxide layer of 2-5 nm thickness is then grown as a tunnel oxide. Afterwards, a nanocrystal FG is deposited as the charge trapping layer (CTL), and then, a thick oxide layer is deposited to serve as a control oxide. Then, depending on the material, a thermal treatment may be necessary to produce nanocrystals. Finally, the gate electrodes are deposited and patterned. There are numerous methods that can be used to

form nanocrystal as storage center for NVM applications. The most commonly used are self-assembly and precipitation, as described below:[38-40]

Self-Assembly

The basic procedures of self-assembly for nanocrystal formation are shown in Figure 12 (a) to (c). A charge trapping layer (CTL) of 1-5 nm is deposited and then the film is annealed at a temperature close to its eutectic temperature in an inert ambient gas, usually N_2, to transform the CTL into a nanocrystal structure. Literature reports showed that the diameter of the nanocrystal is greatly influenced by the thickness of the CTL, as well as the temperature and duration of the thermal treatment.[38,41-43] Figure 12 (d) illustrates the major driving forces that contribute to this process. Dispersion forces and the electrical double layers affect the nanocrystal size and location distributions.[43-45] This process is accomplished through the relaxation of film stress and is limited by the surface mobility. During the thermal treatment, these atoms gain enough surface mobility, allowing the film to self-assemble into the more thermodynamically and energetically stable state.[43] The self-assembly is very popular due to its easy operation and many kinds of materials such as Si, cobalt (Co), gold (Au), tungsten (W), silver (Ag) and platinum (Pt) have been fabricated by the self-assembly method in the nanocrystal embedded FG NVM devices.[41-43, 46]

Precipitation

A trapping layer is prepared by high injection energy (~30-150 keV) ion implantation into a deposited gate insulator or co-deposit system to form nanocrystals accompanied with the annealing process (~950-1050 °C) for 30-60 min in N_2 atmosphere. as shown in Figure 13.[30,47,48] During the thermal annealing process, the reactants can gain enough energy to leave their initial sites and diffuse through the film. Collisions happens during the diffusion of the reactant and results in the nuclei formation.[49] With the increase in annealing temperature, more reactants tend to bond to the nuclei and form the nanocrystal structure in the trapping layer, forming a high density distribution of nanocrystal structures. However, employing traditional high-energy ion implantation for nanocrystal memory applications has revealed some obvious shortcomings.[50-51] The high injection energy may cause damage to the tunneling oxide, resulting in degradation of the device performance. In addition, this method lacks of the controllability of the size and spatial distribution of the nanocrystals in the gate dielectric. In this dissertation, the nc-CdSe and nc-MoO_3 embedded ZrHfO gate dielectric stack are fabricated based on the concept of the thin film self-assembly process. The thin nanocrystal layer will be deposited by the sputtering technique and subjected to a PDA process.

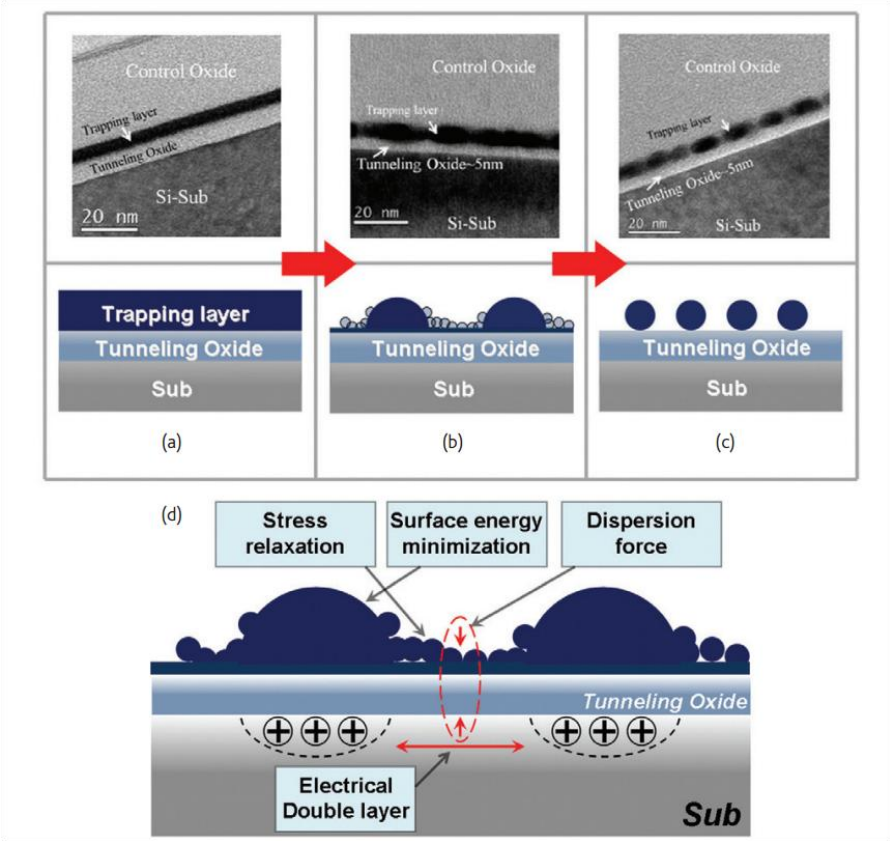


Figure 12. TEM image and schematic drawing of nanocrystal formation by self-assembly with increased duration of thermal treatment from (a) to (c); (d) Major driving forces in nanocrystal formation by self-assembly.[30]

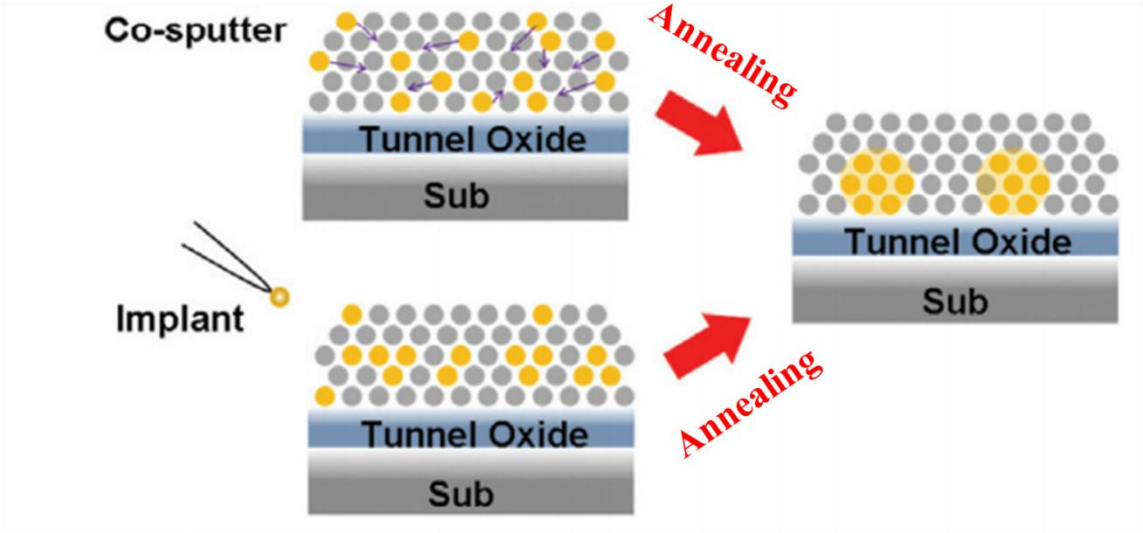


Figure 13. Schematic drawing of nanocrystal formation by precipitation.[30]

1.2.4 Nanocrystal Engineering

The nc-Si is firstly used in the nanocrystal FG NVM by Tiwari in 1996 because it provides a compatible process with the standard MOSFET technology. However, the nc-Si embedded FG NVM will have two main problems, i.e., the Coulomb blockade and quantum confinement effects,[52-53] which limit the electron trapping capability and retention performance.

Coulomb Blockade Effect

Coulomb blockade effect describes the increase of the energy levels when multiple electrons are stored and this effect becomes more pronounced when the nanocrystal size is below 3 nm.[54] The raising of energy levels can be approximately

calculated from the reversible work needed to charge the nanocrystal with the additional electron from the self capacitance C of the nanocrystal:[34]

$$C \quad 2\,\pi\,\varepsilon_{ox}\,d \qquad [6]$$

where ε is the dielectric constant of the tunnel oxide, and d is the nanocrystal size in diameter. The increase in energy for a nanocrystal on addition of the n_{th} electron is given by: [34]

$$\Delta E_{n,n-1} \quad \frac{e}{C}\,[\,n(n-1) - (n-1)(n- \,)\,] = \frac{(n-1)e}{C} \qquad [7]$$

This implies that the electrochemical potential change Δμ due to the addition of each electron is given by: [34]

$$\Delta\mu \quad \Delta E_{n,n-1} - \Delta E_{n-1,n-} \quad \frac{}{C} \qquad [8]$$

where q is the electron charge. The increase of the electrochemical potential is illustrated in Figure 14. Since the C of nanocrystals in the size range of interest is in atto farads (10^{-18} F) or smaller, this change in energy level is significant. For example, for a 5 nm Si nanocrystal, the self capacitance is approximately 0.7 atto farads and the above energy level increase is about 0.074 eV.[33] Therefore, the increase of the energy level decreases the energy barrier of the nc-Si/tunnel oxide. This will result in the degraded retention performance. Also, with some electrons stored in the nanocrystal, the energy level becomes higher and the electric field across the tunneling dielectric layer will be reduced. Therefore, electrons will be prevented to tunnel across the tunneling dielectric layer, which limits the electron trapping capability.[55]

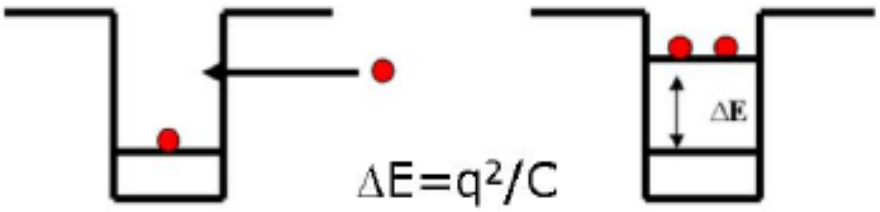


Figure 14. Illustrations of Coulomb blockade effects.

Quantum Confinement Effect

The quantum confinement effect can cause the nc-Si energy band edge shift to higher energy compared with bulk Si. As a result, the energy band offset between the nc-Si and the tunnel oxide is reduced. The following equation can be used to estimate the shift of the conduction band edge due to the quantum confinement effect:[56]

$$E_c(d_{si}) - E_c(d_\infty) \quad \frac{1.9}{d_{si}+1. \quad d_{si}+.} \quad \text{(eV)} \qquad [9]$$

where $E_c(d_{si})$ is the conduction band edge of the nc-Si, $E_c(d_\infty)$ is the conduction band edge of the bulk Si, and d_{si} is the nc-Si size in diameter. The increase of the conduction band edge is illustrated in Figure 15. From equation 9, the conduction band edge of a 5 nm nc-Si is higher than that of a bulk-Si by 0.04 V, i.e., about 3.57 % increase.

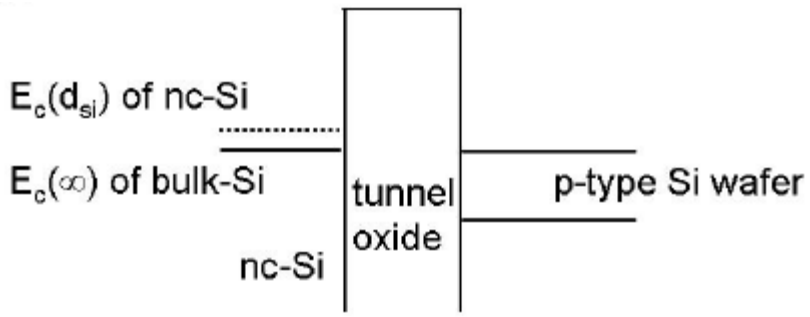


Figure 15. Illustrations of quantum confinement effect.[56]

Due to the Coulomb blockade and quantum confinement effects, the stored charge in the nc-Si will be easily tunneled back to Si substrate because of the reduced band offset between nc-Si and tunnel oxide. Researchers have demonstrated the nanocrystal Ge (nc-Ge) instead of nc-Si embedded FG because of the large memory window under low program/erase voltages and good retention capability due to their higher dielectric constant (~16.0, i.e. stronger coupling with the conduction channel) and smaller band gap energy (~0.6 eV).[57-58] In this dissertation, another semiconductor material, i.e., nanocrystal cadmium selenide (nc-CdSe), has been used to be the charge trapping medium. Recently, nc-CdSe has attracted enormous attention because of both their light emitting and charge storage abilities.[59] CdSe is a n-type semiconductor with a large work function, i.e., between 4.8 eV and 5 eV,[60] it can be embedded in the gate dielectric layer to trap and retain charges for a long period of time. In addition, the CdSe's energy band gap of 2.3 eV is favorable for the charge trapping and retention capability of the trapped holes.[61]

Moreover, to optimize the NVM devices, the program/erase speeds and long retention times need to be achieved simultaneously.[62] Recently, the metal nanocrystals have been proposed to meet this requirement. The major advantages of metal nanocrystals over semiconductor nanocrystals include higher density of states around the Fermi level, scalability of the nanocrystal size, a wide range of available work functions, and smaller energy perturbations due to carrier confinement.[43] Many metal nanocrystals, e.g., Ag, Pt, Au, Co, Ni, W, Mo, Ru, etc.,[42,63-69] have been demonstrated that can be embedded into the gate dielectric for memory applications. Moreover, instead of the metal nanocrystals, the metal oxide nanocrystals, is selected for serving as charge trapping medium. Researchers have demonstrated many kinds of the metal oxide embedded FG structure in the NVM device such as ZnO, ITO, and RuO_x.[70-72] These metal oxide nanocrystals own the advantages for both metal and semiconductor nanocrystals, i.e., a large density of states around the Fermi level (similar to metal)[43] and allow mid-gap trap states for a high capacity and deep charge trapping (similar to semiconductor).[72] In this dissertation, the nanocrystal molybdenum oxide (nc-MoO_3) has been used to be the charge trapping medium due to their high work functions (~5.8 eV) and large band gaps (~3.3 eV), which is favorable for both charge trapping and retention capabilities.[73-74]

1.2.5 Tunnel Oxide Engineering

In nanocrystal embedded FG NVM device, the programming speed and data retention is a tradeoff because they both rely on the tunneling current between

nanocrystals and substrate through a very thin tunneling dielectric layer.[75] In order to increase the programming speed but not lose the retention capability, several efforts have been made. For example, the NVM researchers used a crested and/or a multilayer tunneling barrier to increase the data retention capability.[76] However, the process is not straightforward. Recently, a high-k material, for example HfO_2, is used to replace the thermally-grown SiO_2 as the control and tunnel oxide in the NVM devices to overcome the problems mentioned above. Being physically much thicker than SiO_2, the leakage current of HfO_2 is several orders of magnitude smaller than SiO_2 for the same electrical oxide thickness (EOT),[77] resulting in great data retention behavior. In addition, HfO_2 provides much faster programming speed than SiO_2 because the energy barrier of the Si/HfO_2 is much smaller than that of the Si/SiO_2, i.e., 1.5 eV vs. 3.5 eV, as shown in Figure 16.[75] The low energy barrier favors the electron injection and therefore, improves the programming efficiency and power consumption. In this dissertation, the ZrHfO film is exploited as the tunnel and control oxide layers due to its excellent gate dielectric properties as mentioned in previous sections.

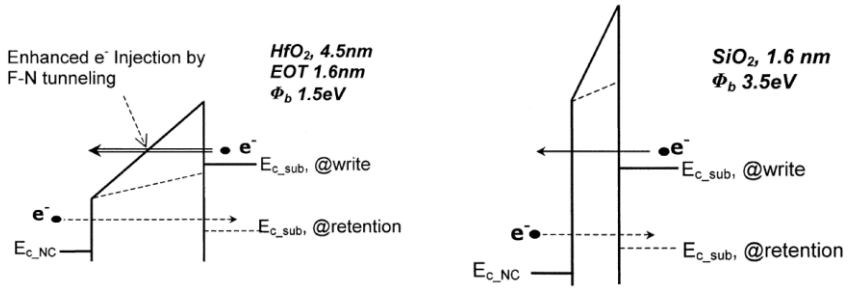


Figure 16. Energy band diagram of Si/HfO_2 (left) and Si/SiO_2 (right) during programming and retention conditions. Both HfO_2 and SiO_2 tunnel oxides have the same EOT of 1.6 nm.[75]

1.3 Light Emitting Device

1.3.1 General Background of the Light Emitting Device (LED)

The incandescent light bulb was invented in the late 1879,[78] it produces light with a W filament heated to a high temperature by a electric current passing through it. The incandescent light bulb is inefficient that converts the electrical energy into the visible light for less than 5% with the remaining energy converts into heat. Since incandescent light bulb provides color temperature close to that of sunlight and extremely high color rendering index (CRI, usually very close to 100),[79] it still occupies a large share of the entire lighting market in the United States. In particular, 90% of the residential sector in the United States is still lighted up by incandescent bulbs. On January 1, 2014, in keeping with a law passed by Congress in 2007, the old tungsten-filament 40- and 60-watt incandescent light bulbs can no longer be manufactured in the United States because they don't meet federal energy efficiency standards. The

fluorescent lamp, which was invented approximately at the same time as incandescent bulbs, provides a more efficient lighting alternative of ~50-60 lm/W compared to the < 20 lm/W of the incandescent light bulb. Fluorescent light bulbs rely on inelastic collisions of electrons with mercury atoms that lead to the emission of ultra violet (UV) photons that are subsequently absorbed by the lamp's fluorescent coating and converted into visible light. Commercial fluorescent lamps can be as efficient as 100 lm/W but their penetration into the residential market is inhibited by their poor CRI and color temperature. Moreover, it contains mercury vapor, which is an environmental pollutant.[80-81] The LED has a high conversion efficiency, e.g., 80%, with a long lifetime, e.g., 50,000 hours. Report shows that the high quality white LED has the potential to reduce ~38% total lighting energy usage in the United States.[82] Therefore, LEDs are replacing incandescent and fluorescent light bulbs in many lighting applications. The first visible-spectrum red LED was developed in 1962 by Nick Holonyak, Jr. while working at General Electric.[83] This first red LED emitted light from a III-V compound semiconductor material, i.e., $Ga(As_{1-x} P_x)$, under forward-biased condition. The theory of the LED is as following: It is essentially a p-n junction diode. When carriers, i.e., electrons and holes are injected across a forward-biased junction, it emits incoherent light. The emitted photon energy is approximately equal to the band gap energy as following equation:[84]

$$h\nu \quad \frac{hc}{\lambda} \quad E_g \qquad [10]$$

where h is Planck's constant of 6.626×10^{-34} J/s, ν is fre ue ncy of light, c is the speed of light of 3×10^8 m/s, λ is wavelength of light, and E_g is bandgap energy. Figure 17 shows

the unbiased p-n junction with the highly doped n side (n^+),[84] the initial built-in voltage V_0, can prevent the excess charges on the n^+ side from diffusing into the p side. When a forward bias is applied across the junction, the built-in potential is reduced from V_0 to V_0 - V. In this case, the electrons will be injected from the n^+ side the p side. Since the p side is not heavily doped, the hole injection from the p side to n^+ side is much less and the current is primarily due to the flow of electrons from n^+ side into the p side. The injected electrons recombine with the holes will induce the spontaneous emission of photons. The currently commercialized LEDs are still made from III–V compound semiconductor mateirals and different band gap energies will result in different wavelengths of the emission such as GaAlAs (red), AlInGaP (yellow-orange), InGaN (blue, green), AlInGaN (ultra violet).[85]

The recombination process can be classified into two kinds: radiative and non-radiative recombination.

Radiative Recombination

Radiative recombination is also referred to band-to-band recombination and it plays a major role in direct bandgap semiconductors. In direct bandgap semiconductors, the minimum energy of the conduction band lies directly above the maximum energy of the valence band in momentum space energy as shown in Figure 18.[86] In this material, free electrons at the bottom of the conduction band can recombine directly with free holes at the top of the valence band, as the momentum of the two particles is the same.

This transition from conduction band to valence band involves photon emission. Direct recombination occurs spontaneously. GaAs is an example of a direct bandgap material.[86]

Non-Radiative Recombination

In general, the non-radiative recombination includes Auger recombination, surface recombination, or recombination at defects.[87] In the indirect band gap materials, the minimum energy in the conduction band is shifted by a k-vector relative to the valence band as shown in Figure 19. The k-vector difference represents a difference in momentum. Due to this difference in momentum, the probability of direct electron-hole recombination is less. In these materials, additional dopants (impurities) are added which form very shallow donor states. These donor states capture the free electrons locally; provides the necessary momentum shift for recombination. These donor states serve as the recombination centers. This is called non-radiative recombination. The indirect recombination should satisfy both conservation energy, and momentum. Thus besides a photon emission, phonon emission or absorption has to take place. GaP is an example of an indirect band-gap material.[86]

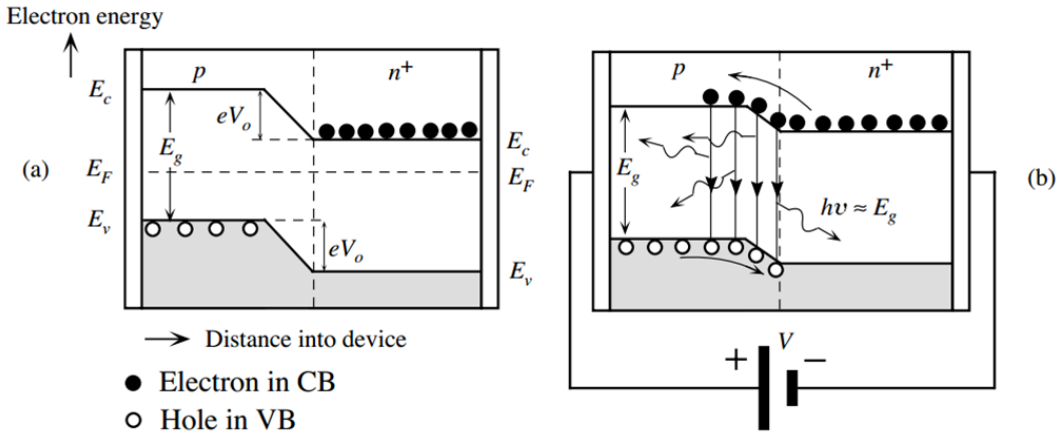


Figure 17. The energy band diagram of a p-n^+ junction (a) without bias and (b) with applied bias V.

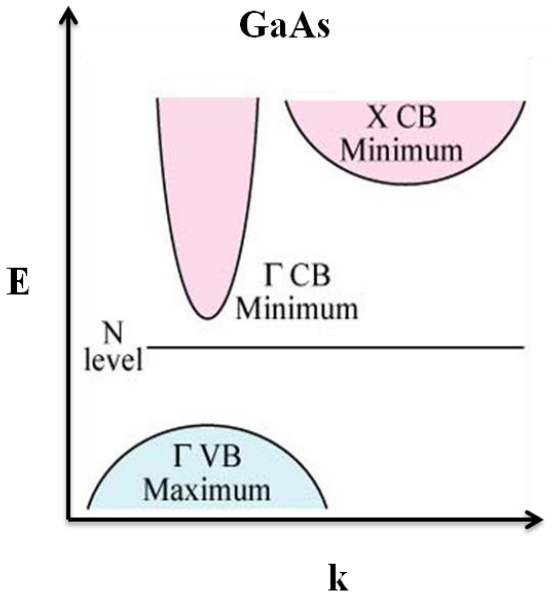


Figure 18. Schematic band structure of GaAs.[86]

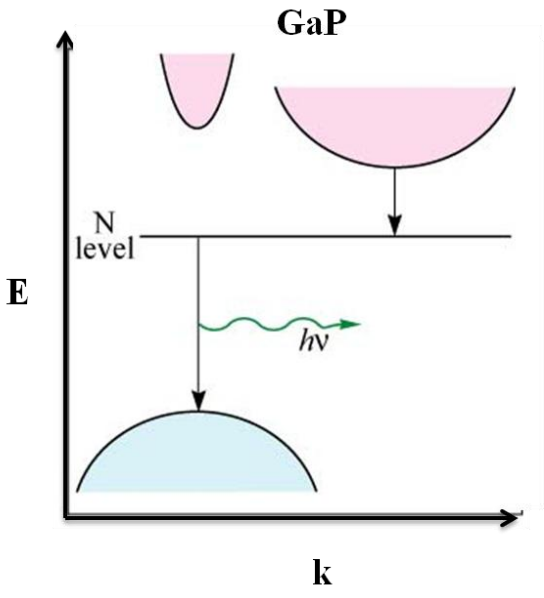


Figure 19. Schematic band structure of GaP.[86]

1.3.2 The Background and Application of the White Light LED

White LED is rapidly evolving for use in the general illumination applications. Switching to high quality white LED can reduce ~38% total lighting energy usage in the United States.[82] As previously mentioned, for a p-n junction LED, the emitted light wavelength is decided by the band gap energy of the semiconductor material. Therefore, the narrow band instead of the broad band light is generated from a single chip p-n junction LED. There are currently two major systems to create white light as shown in Figure 20.[78,85] First, combine three different LEDs that emit red, green, and blue lights as shown in Fig. 20 (a).[85,88] However, a special driving scheme is necessary to generate the color-balanced light.[89] Second, a blue or UV LED in combination with a yellow phosphor material, e.g., the Ce^{3+} doped $Y_3Al_5O_{12}$ (YAG:Ce) or a triphosphor blend, is required as shown in Fig. 20 (b).[78,90] However, it has the Stokes energy loss problem during the conversion of the short wavelength to the long wavelength emission.[78] This energy loss can reduce by 10-30% the overall efficiency of the phosphor-excited LEDs.

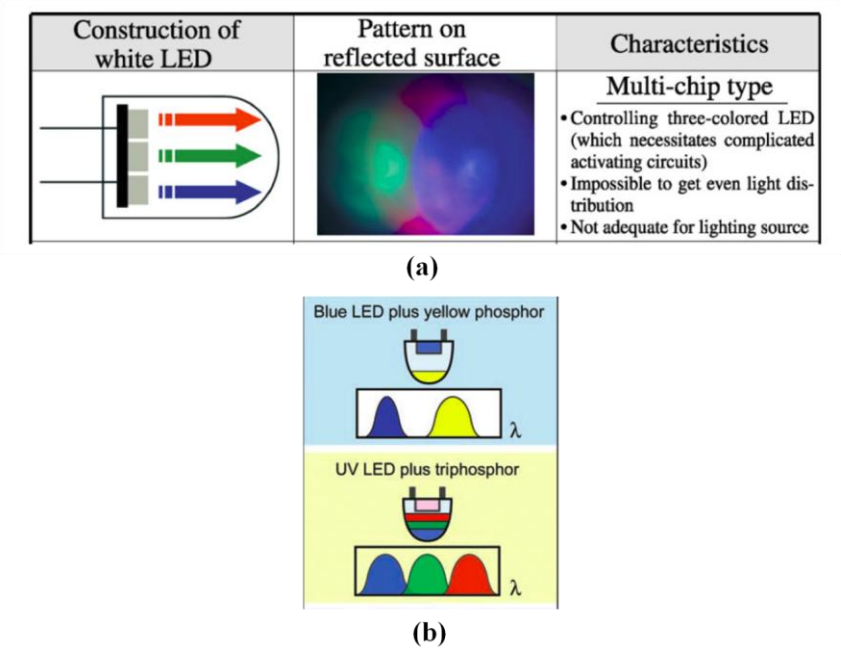


Figure 20. Construction and characteristics of white LED: (a) through colored RGB LEDs and (b) through blue/UV LED in combination with phosphors.[78,85]

White light can also be emitted from nanocrystalline quantum dots (QDs) of ZnSe, CdSe, CdSe/ZnS, etc., under the exposure of the UV light.[91-93] Figure 21 shows the spectra of the integration of blue 440 nm InGaN/GaN LED with CdSe/ZnS core shell nanocrystals along with a International Commission on Illumination (CIE) chart and the picture of the generated white light.[94] The wavelength of the light emission can be tuned by the changing the size of the nanocrystals. For example, Table 2 shows the dependence of the emission wavelength with the size of the CdSe/ZnS nanocrsytals.[94] Therefore, combining a variety sizes of CdSe/ZnS core-shell nanocrystals into a single device has been proposed as a possible route for creating white LEDs.[95-97] The quantum

efficiency of the QD-based white LED can be high enough for the flat-panel display application.[98] However, they are subject to environment contamination and the CRI's are not as good as that of the incandescent light due to the narrow-band emission used, similar to the fluorescent lighting.[82] The maximum CRI of 71 was obtained by applying different sizes of CdSe/ZnS nanocrystals.[94] Another disadvantage for the QD-based LED is the self-absorption due to the small Stokes shift. The emitted energy is absorbed by either the nanocrystals themselves or the neighboring nanocrystals, which reduces the overall quantum efficiency. The organic/inorganic hybrid nanocrystal LED can also emit the white light but it requires a complicated fabrication procedure.[99] Therefore, a convenient single-chip white-light LED is eagerly anticipated.

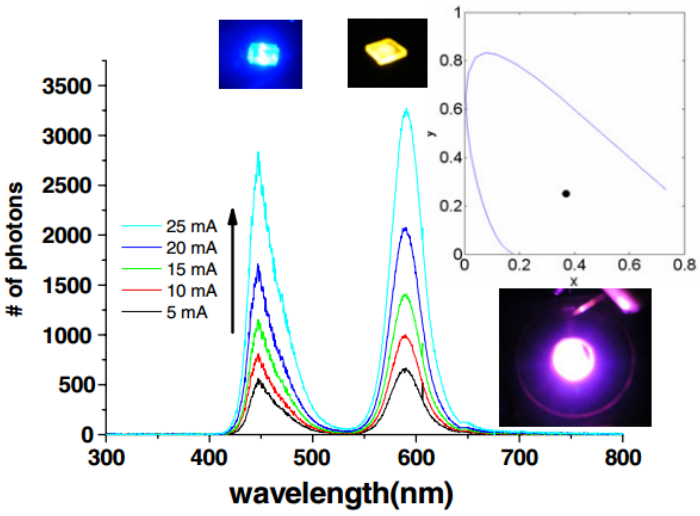


Figure 21. Electroluminescence spectra of blue LED in combination with CdSe/ZnS nanocrystal along with the CIR chart and white LED photo.[94]

Table 2. Dependence of the emission wavelength with the size of the CdSe/ZnS nanocrsytals.[94]

Nanocrystal photoluminescence colour	Crystal diameter (nm)	Peak emission wavelength (λ_{PL}) (nm)
Cyan	1.9	500
Green	2.4	540
Yellow	3.2	580
Red	5.2	620

1.3.3 New Solid State Incandescent LED

In order to overcome those shortcomings of the white LED, a new type of solid state incandescent light emitting device (SSI-LED), which can emit the broad band white light from a single device, has been reported by the Kuo and Lin, recently.[100-103] The idea of the new SSI-LED comes from the report in 1969 that the light emission from the dielectric thin film, e.g., 60 nm to 200 nm thick SiO_2 or Al_2O_3, impinged with an electron beam of 50 keV was observed consistently.[104] Experiments were carried out to determine the physics behind the light emission phenomenon using the classic electromagnetic theory. However, no nanoscale material or device studies were done probably because of the lack of advanced analytical instruments at that time. If the electron beam in the above study is replaced by charges injected from contacts adjacent to the dielectric film, the similar light emission phenomenon can be expected. Furthermore, if the dielectric layer is prepared into a very thin film, the energy required

to transfer the charge through it can be low. Metal oxide high-k dielectrics are good materials for this purpose because their electron and hole offsets to Si are smaller than those of SiO_2, which is favorable for the injection of the charges.[19] Recall the section 1.1.3, the ZrHfO have several advantages among other high-k materials. In addition, the tungsten oxide (WO_x) has been used as the gate dielectric layer in the thin film transistor and WO_3 has also been proved as the good gate dielectric for MOS devices. The W filament is common in the incandescent light bulb. Therefore, in this dissertation, the possibility of the light emission was investigated from an ultra thin ZrHfO and WO_3 high-k dielectric film sandwiched in between the Si substrate and ITO gate electrode. Furthermore, for the high-k dielectric, the PDA condition is critical to both the bulk- and the interface-layer properties.[105-108] The light emission mechanism and the spectrum characteristics may be dependent on the fabrication process. Therefore, the PDA process effects on the emission spectrum of this kind of SSI-LED were also investigated with respect to changes of the material and electrical properties.

1.4 Plasma-Based Copper Dry Etching

1.4.1 Plasma-Based Copper (Cu) Etching Process

In this dissertation, a novel etching technique was used to fabricate a new invented LED driving matrix, which will be addressed in Chapter V. Therefore, a brief introduction of the etching process will be reviewed in this section.

Cu is a popular interconnect material in ultra large scale integrated circuits (ULSICs) due to its lower electrical resistivity, i.e., 1.77 μΩ-cm, and large

electromigration resistance.[109] The use of Cu interconnect also improves the circuit performance by lowering the resistive-capacitive (RC) time delay.[110] However, the Cu thin film is difficult to prepare into fine patterns using a conventional plasma etching process due to the low volatility of the reaction product.[111-113] Figure 22 shows the vapor pressures of copper halides at various temperatures.[114] The conventional plasma etch process is based on the principle of forming volatile plasma reaction product which can be pumped away by the vacuum system. Due to the low volatility of the copper halide, the Cu substrate must be heated to above 200ºC, which makes the process less attractive for industry application. Currently, Cu interconnect lines are prepared with the damascene or dual damascene methods with the chemical mechanical polishing (CMP) process.[115-117] However, these processes are complicated and require various chemicals and wastewater treatment steps.[117]

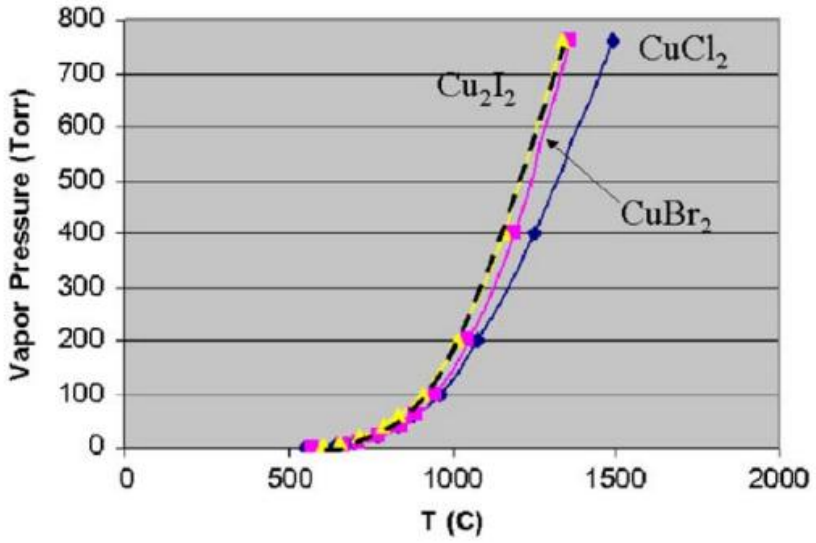


Figure 22. Vapor pressure of copper halides vs. temperature.[11]

In 2001, Kuo and Lee reported a new plasma-based Cu etch method.[118-119] Instead of vaporizing the plasma reaction product, the Cu film was converted into the chlorine or bromine compound, which was subsequently dissolved in a dilute hydrochloric acid (HCl). The Cu to $CuCl_x$ or $CuBr_x$ conversion rate is high, e.g., 300 to 400 nm/min at room temperature. Therefore, a Cu film with a thickness of several hundred nanometers can be totally converted into the $CuCl_x$ or $CuBr_x$ compound within one minute.[114,120] Submicrometer wide Cu lines were successfully prepared with this method.[114] Figure 23 shows the process flow chart of the plasma-based Cu etching process. First, the Cu film is patterned with a conventional photolithography process. Second, the patterned Cu film is exposed to the Cl- or Br-based plasma. The Cu at unprotected area will be converted into $CuCl_x$ or $CuBr_x$, which is considered as a nonvolatile product but is very soluble in an acid solution. Then, the plasma exposed Cu film is dipped into a dilute hydrogen chloride (HCl) solution (35% HCl:H_2O = 6:94) to remove the $CuCl_x$ or $CuBr_x$. Finally, the photoresist pattern is stripped off by acetone in an ultrasonic bath.

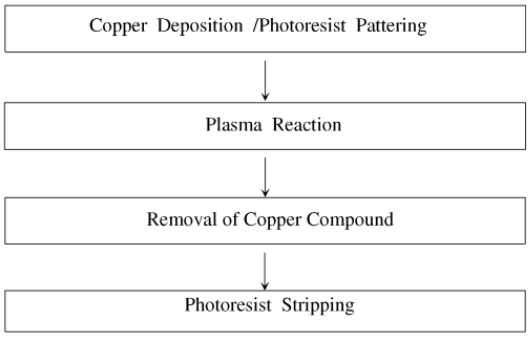


Figure 23. Flow chart of the plasma-based Cu etch process.[114]

This process has also been used to prepare source, drain, and gate electrodes of thin-film transistors.[121] This process was successfully demonstrated on BiCMOS chips and 15-inch thin film transistor liquid crystal displays (TFT-LCDs).[122] Recently, Wu et al. reported a plasma etching process using the H_2 plasma and a two-step plasma etching process using Cl_2 and H_2 gases below room temperature.[123-124] An etch rate of 20 nm/ min was obtained and the Cu line with the > 80^o sidewall slope has been achieved.

1.4.2 Step Effect for the Plasma-Based Cu Etch Process

For actual circuit applications, the interconnect film is often deposited on a topographic surface, e.g., over a vertical or a near-vertical step. Problems, such as cusp formation at the bottom of the step,[125] microcracks,[126-127] and conductive residue,[128] as shown in Figure 24 (a), (b), and (c), respectively, often occur during deposition or after etching. Figure 25 (a) shows the cusp structure of a metal film deposited on a dielectric step. Figure 25 (b) shows a metal line prepared from an ideal etching process. In reality, many electrical failures can be observed at the cusp area, i.e., the circled part in Fig. 25 (b), because of the metal thinning and the high local stress.[129] On the other hand, the directional etch process, such as RIE, often leaves stringers at the bottom corner of the step, which can cause line-to-line shortage.[130] An overetch step is required to remove the stringer.[130] However, the overetch step can cause the "notch" structure, which is the failure spot during the electromigration test.[131] Although there are studies on plasma etching of aluminum (Al) and molybdenum (Mo) over steps,[132] there is no report on the

step effect for the plasma-based Cu etch process. Therefore, in this dissertation, the step effect for the plasma-based Cu etch process will be investigated.

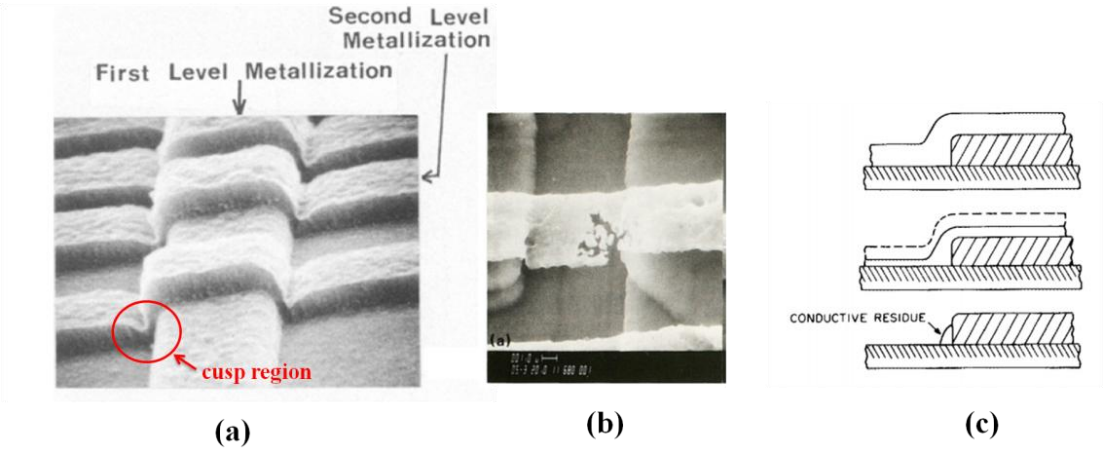


Figure 24. Illustration of the (a) cusp formation at the bottom of the step, (b) microcracks, and (c) conductive residue.[125-128]

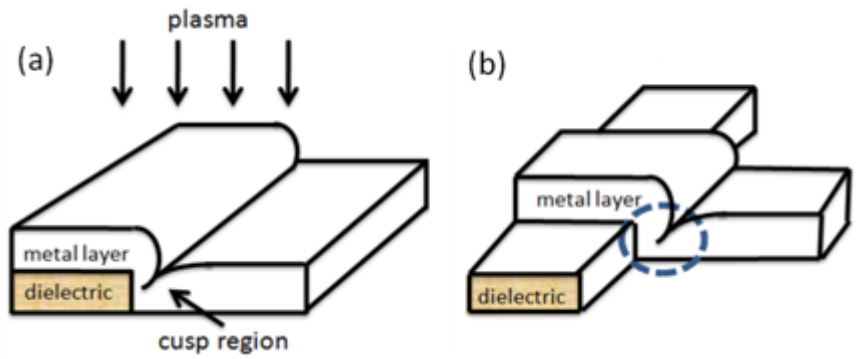


Figure 25. (a) Illustration of the cusp structure of the metal film deposited on a dielectric step and (b) the metal line prepared by an ideal etching process.

1.5 Outline of the Dissertation

Chapter II focuses on the experimental methods. Their corresponding background knowledge and the equipment operations will be described. At first, the process flow of fabricating the high-k based NVM and LED will be described in detail. Then, the fundamental background of the thin film deposition and etch equipments will be reviewed. The instruments and the background knowledge of the material characterizations, e.g., profilometer, X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), scanning electron microscope (SEM), and high-resolution electron transmission microscopy (HRTEM) will be introduced as well. The electrical and optical characterizations of the high-k ZrHfO NVM and LED such as the system setup, capacitance-voltage (C-V), current density-voltage (J-V), and spectrum measurement of the light emission, will be also discussed in this chapter.

Chapter III focuses on the nc-CdSe embedded ZrHfO high-k gate dielectric stack for the NVM applications. The detailed material and electrical investigations of this kind of memory device will be presented. The discrete nc-CdSe shows good charge trapping and retention capabilities. Charges can be deeply trapped at the bulk nc-CdSe sites or loosely trapped at the nc-CdSe/ZrHfO interface. The device can sustain the long-term data storage capability, i.e., retention time > 10 years. The nc-CdSe embedded ZrHfO MOS capacitor is a promising memory device for the future NVN applications.

Chapter IV describes the temperature effects on the charge transfer mechanism and the storage capacity of the nc-MoO_3 embedded high-k dielectric NVM. The high temperature suppressed the Coulomb blockade effect and caused the higher leakage

current due to the larger thermal energy of the trapped holes and the higher conductivity of the high-k film. The amount of trapped electrons was little influenced by the temperature because of the preference of hole trapping of the nc-MoO_3 site. About 43% of the trapped charges were retained after 10 years at 25^{o}C. However, the charge retention capability decreased with the increase of temperature.

Chapter V shows the light emission characteristics from the amorphous ZrHfO high-k stack with different physical thicknesses on the p-type Si wafer under the gate bias condition. The broad band white light was emitted from many small conductive paths formed after the dielectric breakdown. Light generation is due to the thermal excitation mechanism which is different from the electron-hole or exciton recombination mechanism in conventional p-n junction LEDs. The enhancement of the light emission intensity and the improvement of the light quality and efficiency have been observed by including the nc-CdSe layer in the amorphous ZrHfO film since the larger leakage current can be induced. This new single-chip, long lifetime SSI-LED is easy to fabricate using the IC compatible process and can be applied to a wide range of products. Moreover, a new LED driving matrix has been proposed for a better control of the LED operation.

Chapter VI discusses the annealing effect on the light emission from the ZrHfO based SSI-LED. The PDA temperature affects both the material and electrical characteristics of both the bulk and the interface layers and therefore, the emission light characteristics. The high temperature annealed sample has a larger leakage current than the low temperature annealed sample, which causes the brighter light emission in the

former. For the same reason, the light intensity increases with the increase of the magnitude of the applied voltage. The light emission process occurs almost instantaneously after the dielectric breakdown because the nano size conductive path can be quickly excited.

Chapter VII discusses the white light emission from the WO_3 thin film based SSI-LED. The warm white light characteristics have been confirmed from the CIE color coordinates. The light intensity increases with the increase of the magnitude of the applied voltage or the duty cycle in the pulsed driving condition. This new SSI-LED has a long lifetime due to the unique structure of embedding the conductive paths in the high quality dielectric film. This kind of device is easily fabricated with the low thermal budget process. It can be used in many commercial and industrial products.

Chapter VIII discusses the additive gas effect on the etch of the Cu film over a dielectric step using a new plasma-based process. Excessive attack of the cusp region and the edge roughness were observed after the pure Cl_2 plasma exposure process. By adding the additive gases such as Ar, N_2, and CF_4, the attack of the cusp region and the edge roughness were improved due to the change of the ion bombardment energy, Cl radical concentration, and the possible formation of a polymeric protection layer. A two-step RIE process, which has minimum attack of the cusp region with negligible residue left, has been developed. In summary, the Cu film on a topographic surface can be etched into fine lines with good configuration, such as “neck-free” in the cusp region, smooth edge, and no residue, using the new plasma-based etch process.

Chapter IX summarizes all studies in this dissertation and draws conclusions.

CHAPTER II

EXPERIMENTAL

2.1 Introduction

This chapter focuses on the experimental methods used in this dissertation. At first, the process flow of fabricating the nanocrsytal embedded high-k based NVM and high-k based SSI-LED will be described in detail. Then, the fundamental background of the RF magnetron sputtering, plasma enhanced chemically vapor deposited (PECVD) and reactive ion etching (RIE) will be introduced. After that, the material characterization instruments such as profilometer, XRD, XPS, SEM, and HRTEM will be discussed. In the end, the electrical and optical characterizations of the devices discussed in this dissertation such as the system setup, C-V, G-V, J-V, and spectrum measurement of the light emission, will be addressed.

2.2 Process Flow of Nonvolatile Memory Device

Figure 26 shows the process flow chart of fabricating a nanocrystal embedded high-k based NVM. In this dissertation, all the memory devices will be fabricated on the (100) p-type Si substrate (resistivity 11- Ω·cm, doping concentration at 1 ^{15} cm^{-3}, supplied from MEMC). The sample size is about 1 inch×1 inch.

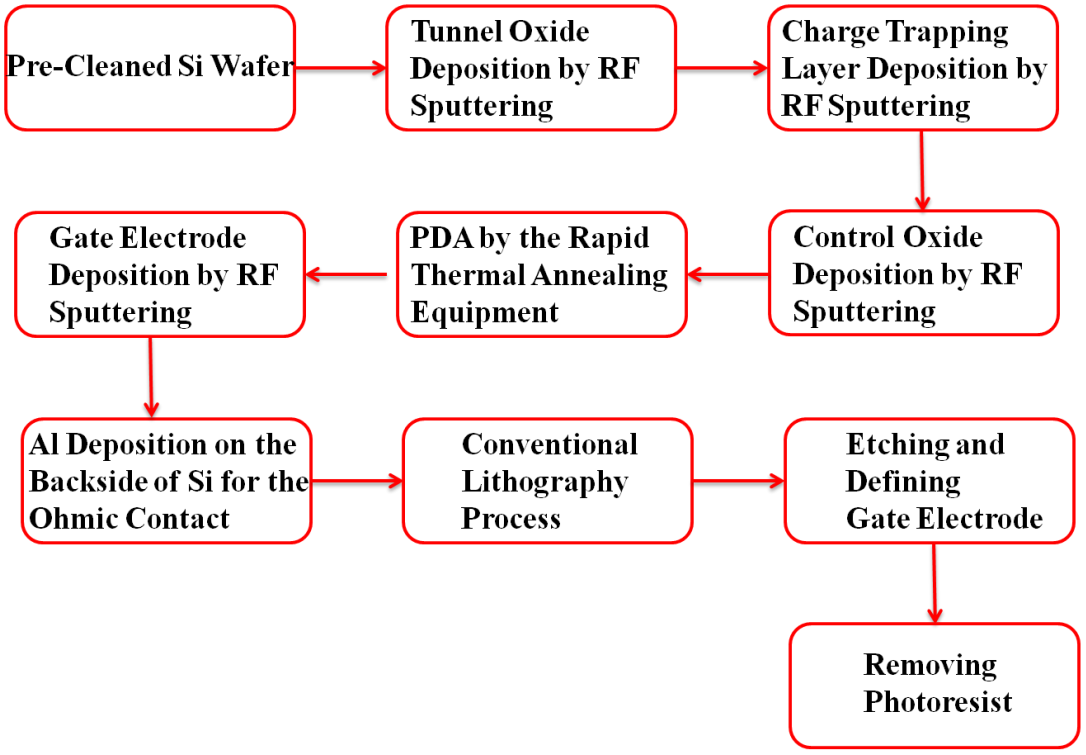


Figure 26. Process flow of the nanocrystal embedded high-k based NVM.

2.2.1 Si Wafer Clean and Load-Lock Sample Transferring System

The Si substrate will be oxidized while it contacts the air. The bare Si was cleaned by a dilute hydrofluoric acid (DHF, 2 %) solution for 5 min to remove the native oxide formed at the Si surface. The Si surface will transfer from hydrophilic to hydrophobic after removing the native oxide. Then, the sample was flushed by the deionized water (DI, resistivity > 1 MΩ·cm) for min. After drying with the N_2 gun, the sample was immediately put into the load-lock system connected to the main chamber of the sputtering system. The chamber was subsequently pumped down to about 10^{-5} Torr by the combination of the mechanical pump (Edwards, E2M8) and turbo

pump (Pfeiffer, TPU 170). This pumping process takes 20 min due to the small chamber volume (15 L). Then, the sample was transferred into the main sputtering chamber that was already in the high vacuum environment, i.e., $< 10^{-6}$ Torr. After the thin film deposition process, the sample was transferred back to the load-lock chamber without breaking the vacuum in the main chamber. Transferring the sample by using the load-lock system can effectively increase the production yield due to the long pumpdown time for the main chamber, i.e., > 4 hours, due to the large chamber size (65L). In addition, the contamination from the air can be eliminated by using the load-lock system due to less exposure of the sputtering chamber to the air.

2.2.2 Thin Film Deposition by RF Sputtering

For the tunnel/control oxide layers, nanocrystal CTL, gate electrode, and Al ohmic contact were all deposited by the RF sputtering in this dissertation. The sputtering power was set to 60-100 W depends on the thin film material. This is because the high power process may cause the strong ion bombardment damage to the sample surface,[133] and the low power process may decrease the deposition rate and degrade the film quality due to the low energized sputtered atoms. The too high process pressure will decrease the mean free path between sputtered atoms and atoms will get scattered before reaching the target, which results in low deposition rate. On the other hand, the plasma cannot be sustained in a too low process pressure environment. Therefore, the choose of the process pressure is critical to the thin film quality. The working pressure during the sputtering process was 5 mTorr for all processes in this dissertation. Figure 27 describes

the process parameters of the thin films used in this dissertation. Plus, a pre-sputtering step was required to clean the target surface before the deposition. This step can be done with the pure Ar plasma for 15 min. More details about the sputtering system will be reviewed in the section 2.4.

	Target	Pressure	power	Atmosphere
Tunnel/Control ZrHfO layer	Zr/Hf (12:88 wt%) composite target (99.8%)	5mTorr	60W	Ar/O_2 (1:1) 40 sccm
WO_3 Gate Dielectric	W (99.99%)	5mTorr	60W	Ar/O_2 (1:1) 40 sccm
Nanocrystal CdSe CTL	CdSe(99.99%)	5mTorr	60W	Pure Ar (50 sccm)
Nanocrystal MoO_x CTL	Mo(99.99%)	5mTorr	100W	Ar/O_2 (1:1) 40 sccm
Gate Electrode ITO layer	ITO (99.99 %)	5mTorr	80W	Pure Ar (50 sccm)
Al Ohmic Contact	Al (99.999 %)	5mTorr	100W	Pure Ar (50 sccm)

Figure 27. Thin film deposition parameters.

2.2.3 Post Deposition Annealing (PDA) by Rapid Thermal Annealing Process

After depositing the gate dielectric film and the CTL on the Si wafer, a PDA process was carried out with the rapid thermal annealing (RTA) method to densify the as-deposited film, remove the defects, and transform the continuous CTL into

nanocrystal structure. The sample was placed on the 4 inch Si wafer holder and heated in the quartz tube. The tungsten-halogen lamps combined with the closed-loop temperature control system and the water cooled assembly can provide a rapid heating and cooling function. The temperature profile can be precisely controlled in this RTA system with suitable parameter setting. The RTA process can greatly lower down the thermal budget compared to the conventional tube annealing process. The RTA chamber was not vacuumed during the annealing process, however, a large gas flow, i.e., > 5 SLPM, and a strong gas exhaust design can maintain the purity of the annealing ambient. Three kinds of gases were used in the RTA system, i.e., N_2 (99.999 %), O_2 (99.993 %), and forming gas (H_2/N_2 : 1/9). The flow rates of all gases are controlled by the mass flow control (MFC) system. In this dissertation, the as-deposited high-k films and CTL were annealed at 800 ^oC for 1-3 min in the pure N_2 depending on the process.

2.2.4 Depositions of Gate Electrode and Backside Ohmic Contact

After the PDA process, the gate electrode layer was deposited on the high-k gate dielectric stack. For the study of the nc-MoO_x embedded ZrHfO NVM, the 120 nm thick aluminum (Al) was used as the gate electrode due to its well-developed deposition and lithography processes. For the study of the nc-CdSe embedded ZrHfO NVM, the indium tin oxide (ITO) was employed as the gate electrode due to its good conductivity and excellent transparency since the same device will be utilized in the LED experiment. After the deposition of the gate electrode, a 150 nm thick Al layer was deposited on the backside of the Si wafer for ohmic contact. The backside of the Si wafer was lightly

scratched by the diamond pen for removing the native oxide prior to the Al deposition. After the Al deposition, the final devices were annealed at 400 ^{o}C in the forming gas (H_2/N_2 = 1:9) atmosphere for 5 min for passivating the oxygen deficiencies and dangling bonds in the NVM devices induced during the sputter deposition.

2.2.5 Patterning Gate Electrode by Lithography Process

In order to fabricate numbers of NVM devices on the same Si wafer, a lithography process was carried out to pattern the gate electrode layer. At first, the positive photoresist (AZ Electronics, AZ 5214-E) was spin coated on the top of the gate electrode and backside of the Al contact. The spin speed of the spin coater (Chemat Technology, KW-4A) was set to 4000 RPM and around 1.4-1.5 μm thick photoresist can be deposited on top of the surface. The sample was then soft-baking on the 90 ^{o}C hot plate for minimizing the concentration of the solvent and enhancing the adhesion. After the soft-bake process, the sample was covered with a patterned quartz mask and exposed to the UV light in the contact aligner (Quintel, Q4000) equipment in the contact mode. The exposure process took 60 s under the UV power density of 7 mW/cm^2. Then, the exposed pattern was developed in the solution that contains 3 parts of the developer (AZ Electronics, MIF 300) and 1 part of the DI. The MIF 300 developer was composed of tetramethylammonium hydroxide, which dissolved the UV-exposed photoresist. The develop process takes ~1 min to prevent the distortion of the pattern. After the developer process, the sample was put into a 125 °C oven for 5 min to solidify the photoresist, i.e., hard-baking process. After solidifying the photoresist, the non-protected area was wet

etched into the final pattern. For the Al gate, the etching solution consisted of H_3PO_4 : HNO_3 : CH_3COOH : H_2O (16 : 1 : 1 : 2). For the ITO gate, the etching solution is aqua regia, which is consisted of HNO_3 : HCl (1:3). The etching time depends on the layer thickness. The averaged etching rate of the Al gate and ITO gate was about 200 nm/min and 1,000 nm/min, respectively. After wet etching, the photoresist is removed by the acetone in an ultrasonic bath for 1 min. Finally, the device was rinsed by the DI water thoroughly for 3 min. Figure 28 illustrats the pattern transferring process. For simplicity, the figure is not drawn in scale.

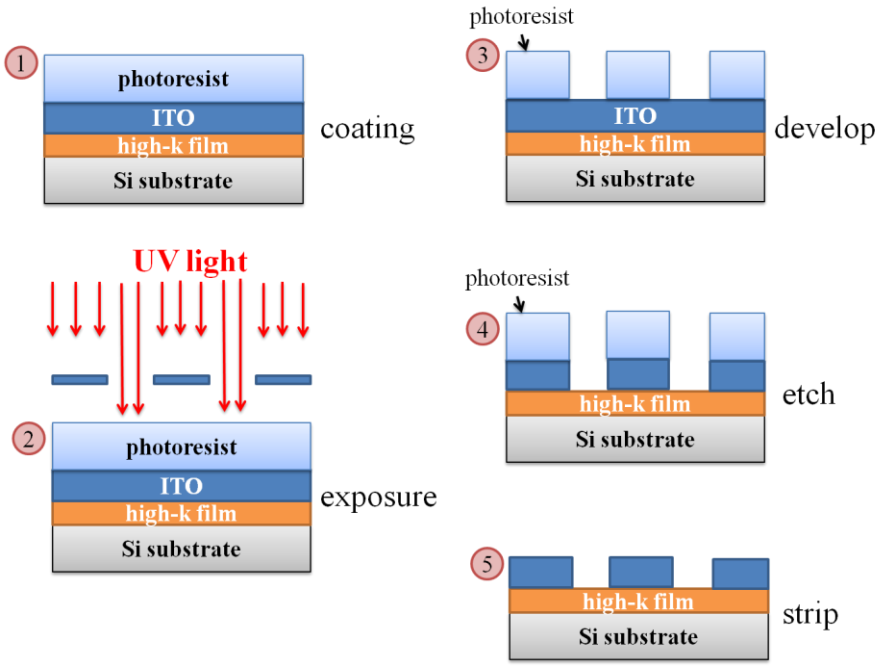


Figure 28. Illustration of the pattern transferring process.

2.3 Process Flow of Solid State Incandescent Light Emitting Device

In this dissertation, there are two kinds of light emitting layer for the SSI-LED, i.e., the high-k gate dielectric layer with and without the embedded nanocrystals. Figure 29 shows the process flow chart of fabricating a SSI-LED without the nanocrystal. The process flow of the structure with nanocrystals will be as same as that in Fig. 26. The sample size for the SSI-LED is about 2 inch×2 inch. The thin films are all deposited by the RF magnetron sputtering as same as that in the NVM device but the deposition time of the ZrHfO and WO_3 gate dielectric layers varies from 2 min to 12 min and the PDA temperatures varies from 800 ^{o}C to 1,000 ^{o}C for 3 min in the pure N_2. The ITO was utilized as the gate electrode due to its good conductivity and excellent transparency, which has been used in many LED applications.[134-135] Same forming gas (H_2/N_2 = 1:9) annealing process was applied to the SSI-LED after thin film deposition.

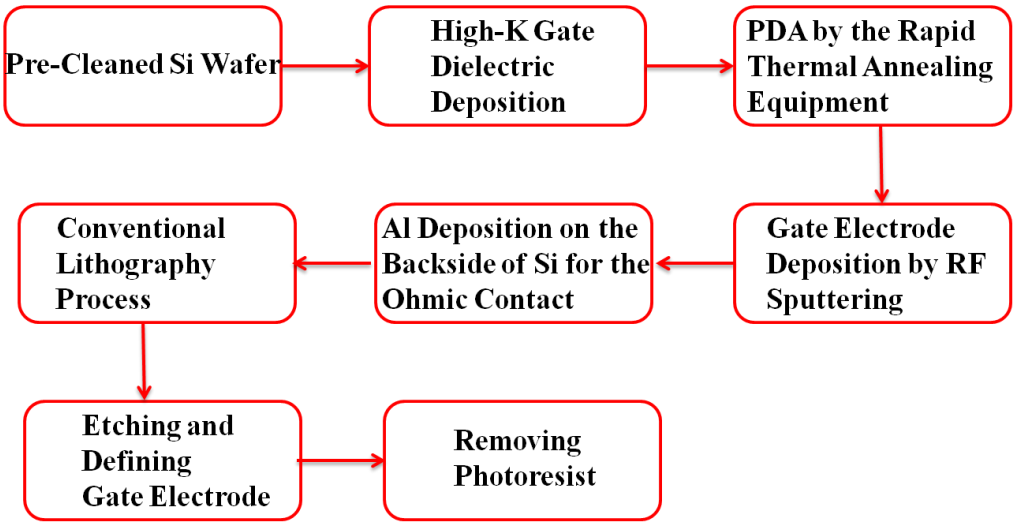


Figure 29. Process flow of the SSI-LED.

2.4 Plasma Deposition and Etching of the Thin Films

The plasma deposition and etching equipments utilized in this dissertation are RF magnetron sputtering, PECVD, and RIE. These equipments will be reviewed one by one in the following:

2.4.1 RF Magnetron Sputtering

In this dissertation, many of the thin film deposition processes, including the high-k gate dielectric, nanocrystal CTL layer, gate electrode, and bottom contact for both NVM and LED devices were carried out by the RF (13.56MHz) magnetron sputtering machine. Figure 30 shows its schematic diagram. The sputtering system is consisted of two chambers, i.e., load-lock and main chambers. Both chambers are made of the stainless steel, and vacuum sealed with the fluoroelastomers (Viton) o-rings and Cu gaskets. The load-lock system has been introduced in section 2.2.1. The main function of the load-lock system is to minimize the contact of the sputtering chamber to the air. Before the deposition process, the main chamber was pumped down to the high vacuum condition, i.e., background pressure ~2×10^{-6} Torr, by the combination of the mechanical pump (Alcatel, 2063 CP1) and turbo pump (Leybold, Turbovac 360). The switch of the mechanical pump is wired to the switch of the turbo pump and therefore, they will be turned on together when the "pump" button is clicked. After ~2 min, the chamber can be pumped down to ~10^{-3} Torr and the turbo pump simultaneously reaches the maximum speed of 72,000 rpm. The large size (65L) main chamber requires ~4 hours to be pumped down to the target background pressure of ~2×10^{-6} Torr. The sputtering system has three guns as shown in Fig. 30. The target size in each gun is ” in diameter and . ”

thick. Therefore, this sputtering system is available for the co-sputtering deposition process. Each gun is equipped with a permanent NdFeB magnet to magnetron control the plasma, and with a shutter to mechanically start/shut off the deposition process. In addition, both the turbo pump and sputtering gun are water cooled by the cycling chiller system (Neslab, CFT-33). The sample holder can be rotated at the speed of 10 rpm for improving the deposition uniformity. The distance between the sputtering gun and sample holder is 15 cm. The gases supplied to this sputtering system are argon (Ar, 99.999 %, research grade), oxygen (O_2, 99.993 %), and nitrogen (N_2, 99.999 %). Ar has its own MFC, while O_2 and N_2 share the same MFC. Therefore, the deposition can be done in three kinds of atmospheres, i.e., pure Ar, mixed Ar/O_2, and mixed Ar/N_2.

The RF sputtering technique is more widely utilized to deposit various kinds of materials compared to the DC sputtering technique because the former can be utilized even when the target material is insulating. If the material is insulating, the sputtering glow discharge cannot be sustained in the DC sputtering system because of the immediate charge build-up of a surface charge on the target. However, in the RF sputtering system, the charge build-up phenomenon would be minimized.[136] In addition, since the RF electrical field increases the collision probability between the secondary electrons and gas molecules, the operating pressure can be as low as 1 mTorr, which improves the sputtering efficiency because the sputtered target atoms can reach to the sample surface without being scattered.[136] The RF sputtering system requires an impedance-matching network between the RF generator and the gun as shown in Fig. 30. The matching box is consisted of two adjustable capacitors, i.e., load capacitor (Cap. 1,

1000 pf in maximum) and tune capacitor (Cap. 2, 500 pf in maximum), and one fixed inductor. By adjusting the load/tune capacitance, the impedance of the whole system can be matched to a certain value, e.g., 50 Ω, for most RF generators. By adjusting the impedance mismatch among the RF generator, sputtering gun, and chamber, the minimized reflected power can be reached, i.e., < 3 W.

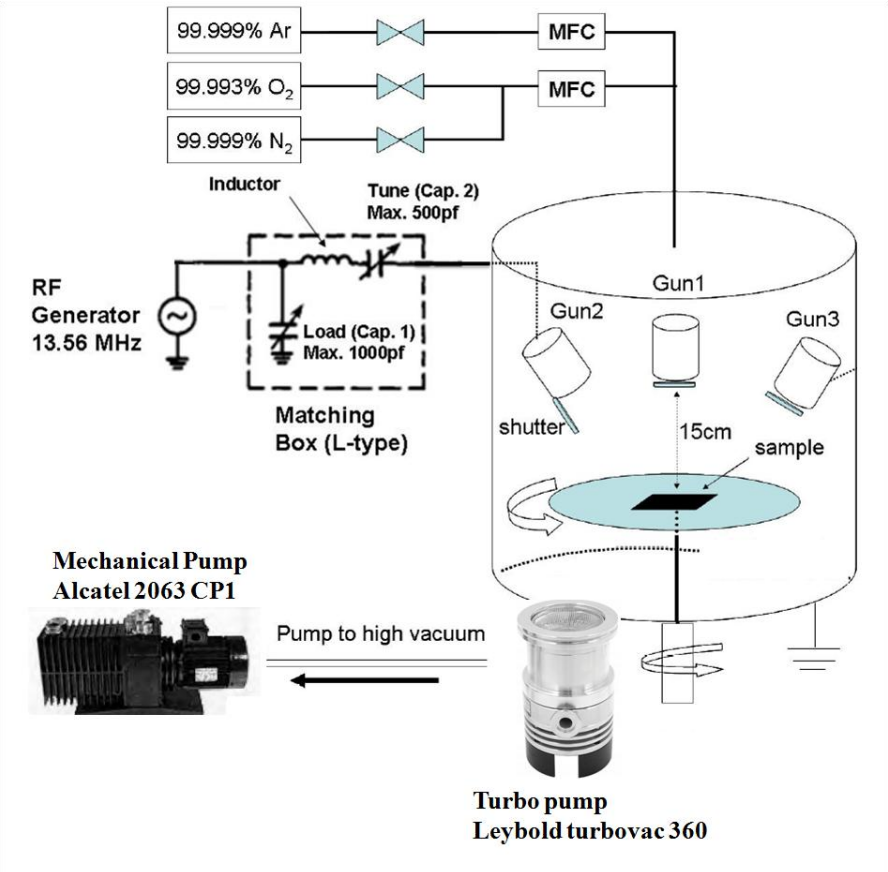


Figure 30. The illustration of the RF magnetron sputtering system.

With the aid of the magnetic field, the ionization of the sputtered gas can be increased significantly, which results in much higher deposition rate.[137] The concept of the magnetron enhanced sputtering is shown in Figure 31.[138] The RF sputtering system utilized in this dissertation is also featured with the circularly-arranged magnetron control ability. A magnetic field (B) is provided around the cathode (target) area, which is perpendicular to the electric filed (E). In this configuration, the electron movement would be confined into the E×B direction, and its movement path changes from a linear to a spiral style. Therefore, the magnetron control confines the plasma above the target in annular rings, which enhances the ionization of the sputtered gas such as Ar atoms and in consequence, increases the sputtering efficiency.

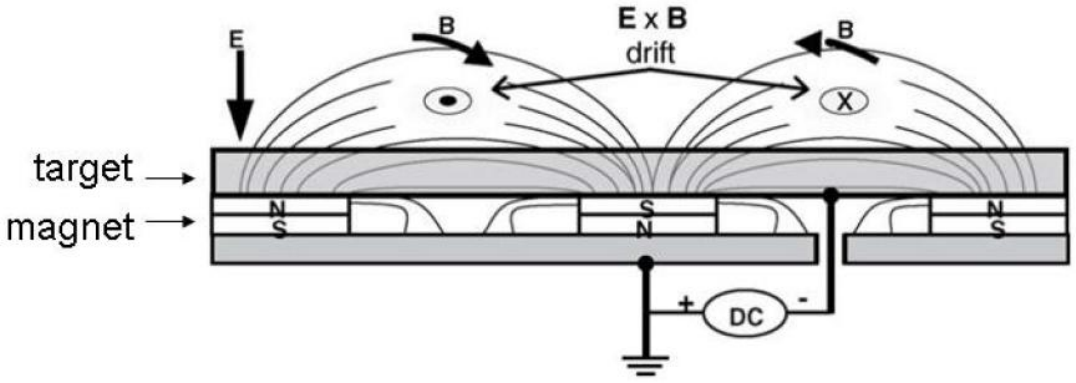


Figure 31. Schematic configuration of magnetron control.[138]

2.4.2 Plasma Enhanced Chemical Vapor Deposition (PECVD)

The PECVD used in this dissertation is AMP Plasma I made by Applied Materials. The SiN_x near-vertical step used in the plasma-based Cu dry etch study is

prepared by the PECVD. The PECVD system has a parallel-plate-electrode configuration with the electrode size of 65 cm in diameter and the electrodes distance of 6.25 cm. The feed gases of SiH_4 (semiconductor, 99.999% Air Liquide), NH_3 (semiconductor, 99.999% purity, Matheson Tri-Gas), and N_2 (semiconductor, 99.9999% purity, Praxair) are introduced into the PECVD and the gas flow rate is controlled by the independent MFCs. The primary reaction on the substrate surface during the deposition is:

i i x [11]

N_2 is used as a dilute to prevent the gas phase reaction. The SiN_x is usually nonstoichiometric. A certain amount of hydrogen may exist in the film in the form of Si-H or N-H.[139] Both the stoichiometry and the hydrogen content of film affect its mechanical and electrical properties. The N/Si ratio depends on the deposition conditions such as process pressure, feed gas flow rate, substrate temperature, and RF power. The pressure control system in PECVD includes an angle valve, a booster pump, mechanical pump, and capacitor manometer. The temperature system is made of three-zone heater and controllers. The substrate temperature can be controlled between 20ºC to 300 ℃ and the SiN_x is deposited under 250 ^{o}C in this dissertation. The plasma system consists of the 13.56 MHz RF generator (OEM-12A, ENI), a pi-type matching network (MW-10, ENI), and a plasma controller. The top electrode of the PECVD chamber is powered with the RF generator and the bottom electrode and the wall are grounded. The whole system is controlled by PC with LabWindow/CVI interface (National Instrument).

2.4.3 Reactive Ion Etching (RIE)

The plasma-based Cu dry etch study was done by a conventional diode-type RIE chamber (700D, Plasma-Therm, St. Petersburg, FL). Figure 32 shows a schematic diagram of the plasma reactor. A mechanical pump (Leybold D90) and a turbo pump (Alcatel 5402 CP) are attached to the system. The bottom electrode is powered with a 13.56 MHz RF generator connected to a matching network for the plasma generation. The upper electrode and the reactor wall are grounded. Both the top and bottom electrodes are made of anodized aluminum and were of the same size, i.e., a diameter of 9 inch, with a 2.8 inch gap in between. A heat exchanger is attached to the lower electrode to maintain the constant temperature during the plasma exposure. Multiple independent MFCs are used to connect various high purity feed gases such as hydrogen chloride (HCl) (ULSI purity, 99.999%, Matheson Tri-Gas), chlorine (Cl_2) (semiconductor purity, 99.99%, Matheson Tri-Gas), Ar (semiconductor purity, 99.999%, Matheson Tri-Gas), N_2 (semiconductor purity, 99.999%, Matheson Tri-Gas), and tetrafluoromethane (CF_4) (semiconductor purity, 99.95%, Matheson Tri-Gas).

After a sample is loaded into the RIE chamber, the chamber is pumped down by the mechanical pump and the turbo pump until it reaches the target background pressure, i.e., 10^{-5} Torr. The process parameters such as process pressure, feed gas, gas flow rate, RF power, and the plasma exposure time are all controlled through a software interface programmed by Lookout. During the plasma etching process, the RF source is connected to the lower electrode, resulting in a substantial potential drop and the cathode bias voltage ($-V_{dc}$) can be considered as a reference to the ion bombardment. Moreover, the

plasma phase was monitored with an optical emission spectroscope (OES, model PCM 100 SC technology). During the plasma generation process, the atoms or molecules are activated to an excitation state by the electron hit, then immediately relax to ground state and emit photon, which can be detected and analyzed by OES. It is a powerful technique that uses the intensity of light emitted from plasma at a particular wavelength to analyze the intensity of atoms or molecules of a certain element.

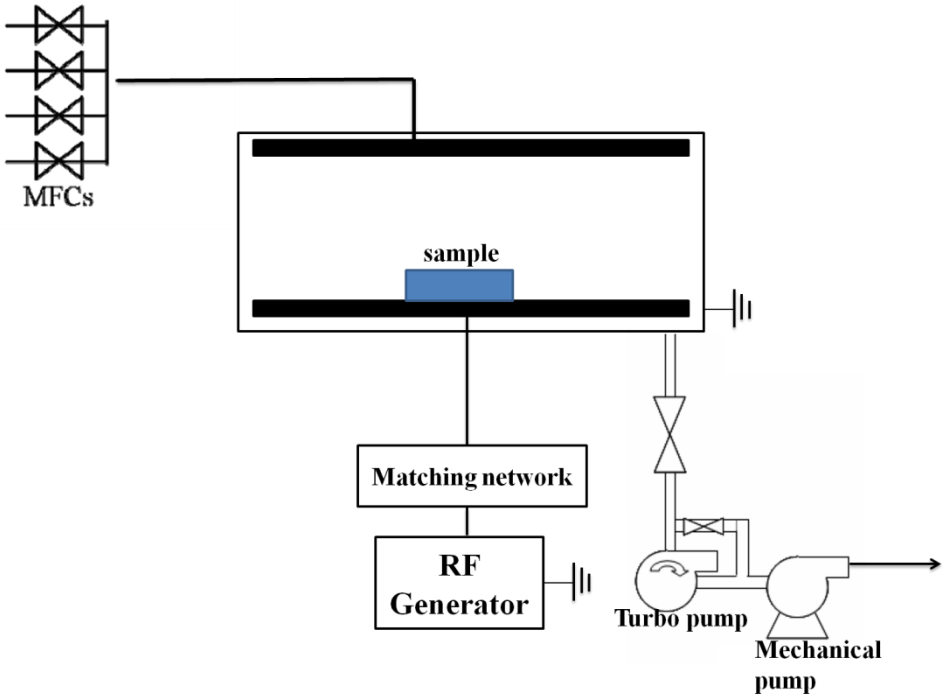


Figure 32. Illustration of the RIE system.

2.5 Material Properties Characterization

Material properties of the bulk high-k films and interface layers between Si substrate and high-k films were investigated in this dissertation. The background knowledge of each material characterization equipment will be introduced in this section. The profilometer (Veeco, Dektak^3 stylus) technique, which was used to measure the thickness of the thin film in order to define the deposition/etch rate, will be introduced in this section. XPS **(**Kratos Axis Ultra Imaging XPS**)** was used to analyze the chemical bonding states of the essential elements in the bulk and interface layers. XRD (Bruker, D8-Focus) was utilized to detect the crystalline structure of the bulk high-k films and nanocrystal layers. SEM (JEOL JSM-7500) provides high resolution images of a sample surface including top view or cross-sectional view. HRTEM (JEOL, JEM-2010) was utilized to investigate the material properties in the thin film, e.g., physical thickness of the bulk and interface layers and discrete nanocrystals identification.

2.5.1 Profilometer

The vertical profile of the thin film was measured by a Dektak^3 profilometer, which can accurately measure step heights from below 100 Å to over 50 μm. The profilometer has a stylus radius of 5 μm. During the horizontal scan, the stylus was kept distant to the sample surface by a contact force. This force is in the micron newton (mN) range and can be maintained as constant due to the cantilever system operating on the spring mechanic principle. The resolution in the horizontal direction is governed by the

scan speed and stylus radius, while that in the vertical direction is governed by the stylus radius and cantilever system.

2.5.2 X-ray Photoelectron Spectroscopy (XPS)

XPS, also known as electron spectroscopy for chemical analysis (ESCA), can both identify the element and its chemical binding states. In this dissertation, the chemical bonding states of the bulk high-k films, nanocrystal layers, and high-k/Si interface layers were all investigated by the XPS analysis. During XPS analysis, an monochromatic Al X-ray (Kα, 1 . eV) strikes the sample surface. The core level electrons absorb the energy and may be ejected out of the sample, which is known as photoelectron effect as shown in Figure 33.[140] The kinetic energy (KE) of the photoelectron can be correlated to the binding energy (BE) in the following equation:

$$BE \quad h\nu - KE - \Phi \qquad [12]$$

where hν is the X-ray energy (Al Kα, 1486.6 eV), and Φ is the work function of the spectrometer, which is usually in the range of 3-4 eV. KE of the emitted photoelectron can be detected by the analyzer. The chemical bonding states of an element can be determined by comparing the binding energy shift. Therefore, the element either in the neutral molecular state or in the charged compound state can be distinguished. However, there are some limitations of the XPS technique. For example, the hydrogen (H) and helium (He) cannot be detected by the XPS because their 1s orbital has a very small cross-section for photoemission which results in an almost zero catch probability. In addition, the detection limit of the normal XPS instrument is in the parts per thousand

range and due to the short mean free path of the emitted electron, XPS technique only can provide the chemical information at near surface region, i.e., about 10 nm depth. Besides those limitations, the charge accumulation effect will induce a incorrect BE information. Therefore, the detected XPS spectrum needs to be calibrated with the carbon (C) 1*s* peak at 284. 8 eV. The XPS Peak 4.1 software has been used to fit the data in this dissertation including the background fitting, peak deconvolution, and identification. The smallest mean s u ared error, i.e., $\Sigma \chi^2$, is achieved, for the peak fitting.

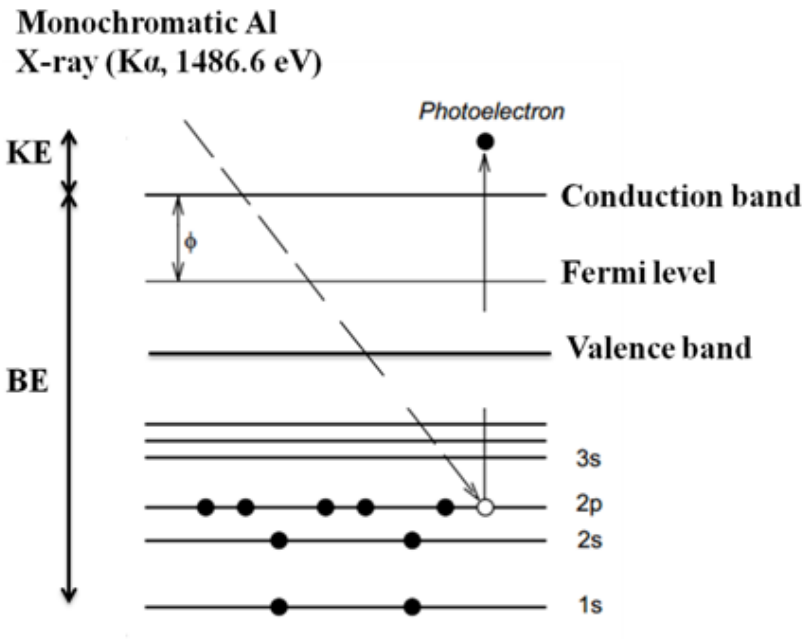


Figure 33. Illustration of the photoelectron effect.[140]

2.5.3 X-Ray Diffraction (XRD)

The crystalline structure information of the high-k films and nanocrystal layers such as grain size, preferred orientation, crystalline structure, can be obtained by using XRD analysis. The monochromatic Cu Kα X-ray (λ 1. 1 Å) was used in the XRD instrument. After the Cu Kα X-ray strikes the sample with an incident angle (θ), the X-ray can be reflected by the crystalline planes as shown in Figure 34.[141] The reflected X-rays from the two consecutively parallel crystalline planes can form the constructive or destructive interference. Only the former can be detected by the scintillation detector, which reflects a XRD peak in the XRD pattern. Judged from the XRD pattern and referred XRD peaks to the Joint Committee on Powder Diffraction Standards (JCPDS) database, the sample's crystalline structure, phase, and orientation can be determined. The condition to form the constructive interference must meet the Bragg's law:[141]

$$d \sin\theta \quad n\lambda \qquad [13]$$

where d is the spacing between the two consecutively parallel crystalline planes, n is an integer, and λ is the wavelength of the Cu Kα X-ray (1.5418 Å). In addition, the averaged grain size of each orientated grain in the polycrystalline sample can be also calculated from the XRD peak's location and full width at half maximum (FWHM) by the Scherrer equation,[142] i.e.,

$$t \quad \frac{.9\,\lambda}{B\cos\theta} \qquad [14]$$

where t is the averaged grain size, λ=1.5418 Å, θ corresponds to the half of the peak location (2θ), and B is the peak's FW M in ra diant unit.

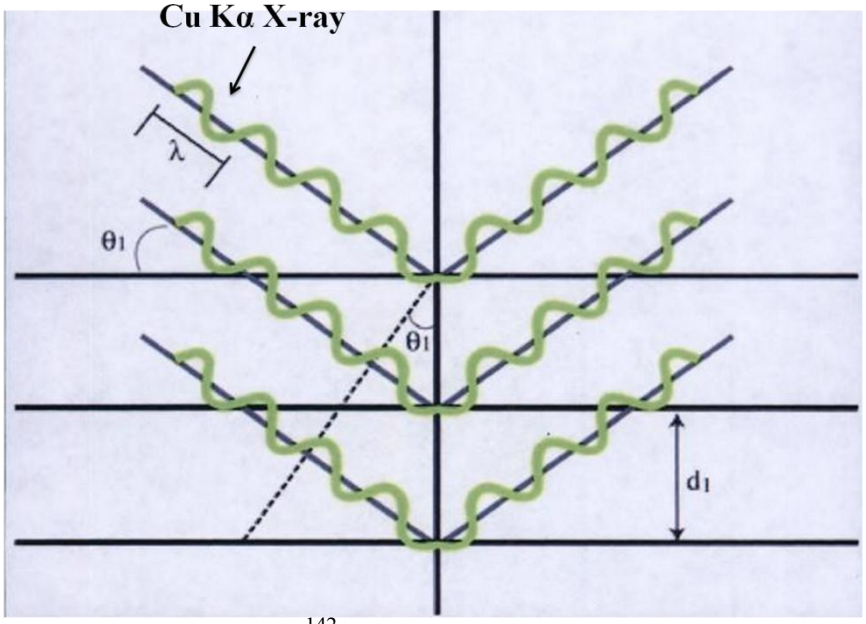


Figure 34. Illustration of the XRD.[142]

2.5.4 Scanning Electron Microscope (SEM)

SEM can provide high resolution images of a sample surface. The SEM used in this dissertation is a cold cathode analytical Field Emission (FE) SEM (JEOL JSM-7500 SEM) system. High density electrons are emitted when a strong electric field is applied to a cathode (electron emission element) with a sharpened tip. Compared to the thermal emission filament based SEM, the FE based SEM has some advantages such as the smaller diameter emitted beam and longer filament life because the emission is cool. The former can effectively increase the resolution.[143] However, the FE gun requires much higher vacuum, i.e., 10^{-7} Torr.[143] The highly coherent electron beam strikes the sample surface and results in the emission of backscattered and secondary electrons. The former is the high energy electrons that are ejected by an elastic collision of an incident electron.

The latter is from the inelastic scattering of the lower energy electrons. Each of which can be detected by specialized detectors. The signal collected by the detector is amplified and converted into a digital image. Usually the secondary electron imaging mode provides high-resolution imaging of fine surface morphology and the backscatter electron imaging mode provides image contrast as a function of elemental composition and the surface topography. The SEM micrographs in this dissertation were all taken under the secondary electron imaging mode. Moreover, if the material of the sample is not highly conductive, the charges can be accumulated on the sample surface, which may lower down the resolution. Therefore, the samples used in this dissertation are all coated with a thin highly conductive platinum (Pt) film layer by a sputtering machine, which can effectively prevent the surface charging and avoid the image distortion. Figure 35 shows the illustration of the SEM equipment.

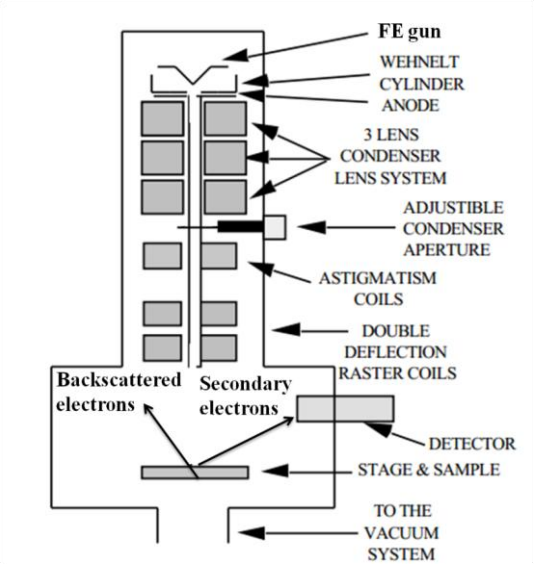


Figure 35. Illustration of the SEM.[143]

2.5.5 High-Resolution Transmission Electron Microscope (HRTEM)

In NVM and LED devices, the physical thickness of the bulk high-k film, high-k/Si interface layer, and the discrete nanocrystal structure, are critical to the device performance and need to be carefully examined by the HRTEM. Figure 36 shows the schematic diagram of the HRTEM system. Electrons are generated from the lanthanum hexaboride (LaB_6) filament by the thermo-ionic emission mechanism. Then, the electrons are accelerated by a 200 kV voltage, which produces a very short wavelength, i.e., ~ 0.006 nm. The specific ~ 0.23 nm point resolution can be achieved in the JEOL JEM 2010, which is the model utilized in this dissertation. The two condenser lens, C1 and C2, are used to make the electron beam more coherent and can also focus the beam on the sample. The beam is then restricted by the condenser aperture, which excludes the high angle electrons. After that, the beam strikes the specimen and part of it transmitted through the specimen depending on the thickness of the specimen. The transmitted beam is focused by the objective lens and transferred to the intermediate and projective lens and reaches the phosphor screen or charge coupled device (CCD) camera.[144] The objective aperture, which is located after the objective lens, can adjust the contrast by blocking part of the electron beam. By projecting the magnified TEM image on the image plane based on the transmission electrons is called the "bright-field imaging mode" due to the high energy nature of the transmitted electrons. On the other hand, the image formed based on the scattered electrons is called the "dark-field imaging mode" due to the relative low energy of the scattered electrons. In this dissertation, all TEM micrographs were taken under the bright-field imaging mode.

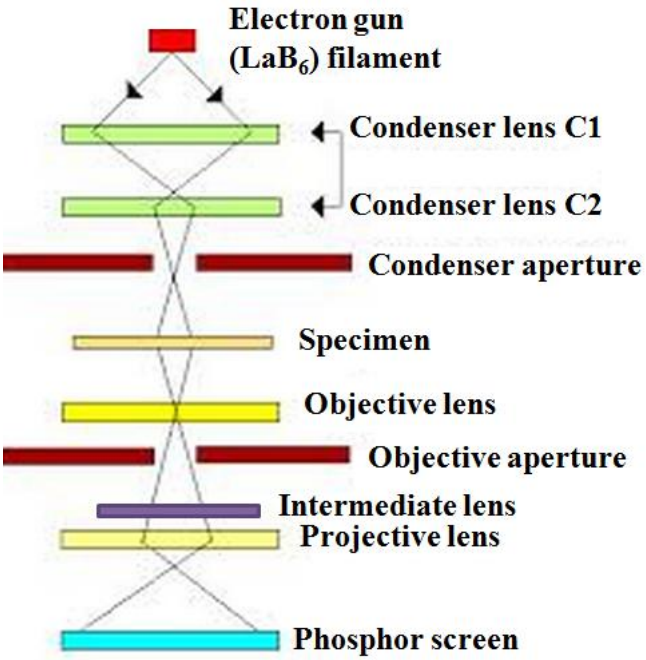


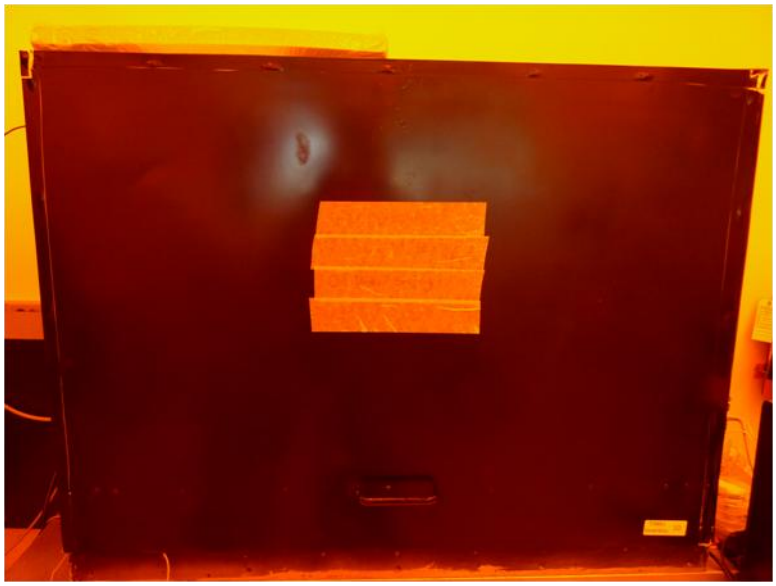
Figure 36. Illustration of the HRTEM.[144]

2.6 Electrical Properties Characterization

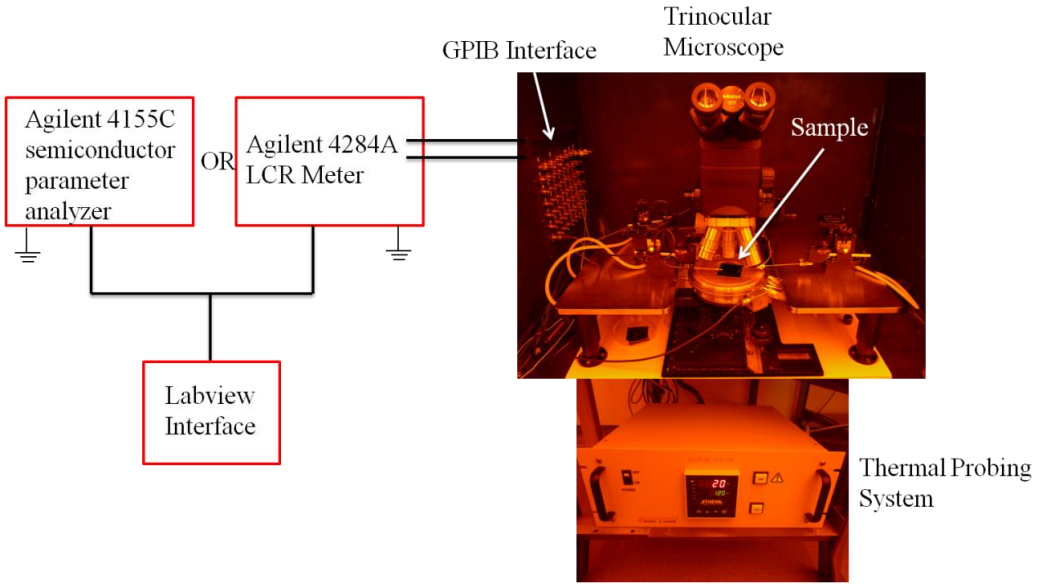
2.6.1 Electrical Characterization System Setup

In order to realize the performance of the nanocrystal embedded high-k NVM and SSI-LED, the electrical properties such as capacitance voltage (C-V), conductance-voltage (G-V), and current density-voltage (J-V) measurements were investigated in this dissertation. The entire measurement process was carried out in the customized flat Al black box, which is insulated from the outside environment disturbance, such as lights, noises, heats, and vibrations as shown in Figure 37 (a). The measurement was performed on the probe station (Signatone, S-1160) as shown in Figure 37 (b). The sample loading chunk of the probe station is made with the gold alloy with a vacuum for preventing

from the sample movement during the measurement. Also, a thermal probing system (Signatone S-1060R) is connected to the probe station and the chunk can be heated to maximum 600^{o}C for the temperature-dependent electrical test. In addition, the chunk was used to receive the measured signals from the backside of the Si substrate, therefore, it should be electrically floated to prevent from driving signals to the ground. The measurement probe tip is made of tungsten, and has a diameter of 1 μm. High frequency C-V, G-V curves were measured with the Agilent 4284A LCR meter and J-V curves were measured with the Agilent 4155C semiconductor parameter analyzer. The C-V and G-V measurements were conducted by triaxial cables and J-V measurement was tested by biaxial cables for a minimized electrical interference and signal loss. The National Instruments Labview 7 program was used to control the whole measurement process through the GPIB interface.



(a)



(b)

Figure 37. (a) Flat Al black box and (b) probe system for electrical characterization.

2.6.2 C-V Curve Measurement

The C-V curves of the nanocrytal embedded high-k NVM were characterized in this dissertation. Many critical electrical properties of the device, such as EOT, flat band voltage (V_{FB}), interface state density (D_{it}), and oxide trapped charges (Q_{ot}) can be extracted from the C-V curve.[145] V_{FB} decribes a voltage when the band turns to the flat-band condition.[146] The D_{it} describes the interface traps located at the interface between the dielectric film and the Si substrate.[146] The Q_{ot} decribes the traps inside the oxide layer and can be created by the X-ray radiation or carrier injection.[146] Also, the Si doping concentration can be extracted from the accumulation and inversion capacitance. The V_T can be extracted from the intersection point of inversion capacitance and extrapolation of C-V curve. Moreover, the frequency-dependent (100 kHz to 1 MHz) C-V measurements can be used to determine the charge trapping sites in the nanocrystal embedded high-k NVM devices. The principle of the C-V measurement is to use a linear DC bias swept in a range of the gate voltage. At the same time, a high frequency small sinusoidal AC voltage of 0.25 V is superimposed simultaneously to extract the capacitance (C) and conductance (G). C and G can be expressed as Equations 15 and 16:

$$C \quad \frac{dQ}{dV} \qquad [15]$$

$$G \quad \frac{dI}{dV} \qquad [16]$$

The Agilent 4284A assumes the device under testing has a parallel combination of C and G. By measuring the impedance (Z) of the parallel G-C circuit, i.e., ratio of the output AC current to the input AC voltage, the capacitor's G and C values can be obtained at the same time due to the following relationship:[145]

$$Z = \frac{G}{G + (\omega C)} - \frac{j\omega C}{G + (\omega C)} \quad [17]$$

where ω is the angular frequency of $2\pi f$, and f is the frequency of the superimposed AC voltage signal. The series resistance existed in the measurement system is unavoidable and needs to be minimized. A good electrical contacts is important to minimize the series resistance and moreover, the separate correction processes in the "open" mode (i.e., no contact between the probe tip and chunk) and in the "short" mode (i.e., the probe tip and chunk contact each other) were developed to further improve the accuracy of the measurement.[18]

On the other hand, the NCSU CVC program proposed by Hauser et al.[147] is used to extract the V_{FB} and Q_{ot} in this dissertation. This program appropriately correct the quantum confinement effect measurement errors when the high-k film is extremely thin, i.e., < 3 nm.

2.6.3 J-V Curve Measurement

The J-V measurements were performed on the nanocrystal embedded high-k NVM and SSI-LED in this dissertation. The current transport mechanism such as Schottky emission, Frenkel-Poole emission, and Fowler-Nordheim tunneling conduction mechanisms and charge trapping/detrapping phenomena can be characterized from the J-V curve.[146] Moreover, the breakdown phenomenon of high-k gate dielectric stack is critical to the light emission mechanism in the SSI-LED research, which can also be observed from the J-V curves. The basic principle of the J-V measurement is to apply a DC bias on the capacitor via the probe tip, and then receive the current signals from the

same probe tip. The voltage profile of the DC bias in this dissertation is in the ramp mode. However, in the ramp mode, the measured current may be contributed by the gate leakage current and the displacement current. In order to minimize the latter, the DC bias ramping with a very slow speed, i.e., 0.01 V/s, is usually used.

2.7 Optical Properties Characterization

The optical properties such as light emission spectrum, color coordinates on the International Commission on Illumination (CIE) chart, correlated color temperature (CCT), and CRI are critical to the performance of the SSI-LED. Moreover, the external quantum efficiency (EQE) can be characterized once the intensity of the light emission and current passing through the device are obtained.

2.7.1 The Measurement of the Light Emission Spectrum

For extracting of the light emission spectrum, the sample is set up on the same probe station as introduced in the section 2.6.1 with the same Al black box as shown in Figure 38. The ITO gate electrode was defined into round dots with different sizes and stressed with a DC gate voltage supplied by the Agilent E3645A power supply with the maximum voltage of 60 V. The 1 meter long optical fiber with 1,000 μm core diameter receptor in combination with the optical emission spectrometer (OES, StellarNet BLK-C-SR-TEC) was used to detect the light emission spectrum. The OES is equipped with a thermal electric cooling system for a better stability of the S/N ratio under long exposure time. The optical fiber was set on the top of the ITO pattern, i.e., the surface of the

receptor is parallel to the sample, with the distance of 0.2 cm as shown in Fig. 38. The OES needs to be calibrated, i.e., take the dark reference, in the black box before taking the light emission spectrum. The integration time is set at 30,000 ms and the average sampling is set at 1 for reaching the maximum count of photons, i.e., 65,000 count, in the "scope mode". After calibrating the OES under the "scope mode", the OES needs to be calibrated again under the "watts mode" by the same sequence and the light emission spectrum will be recorded under the "watts mode".

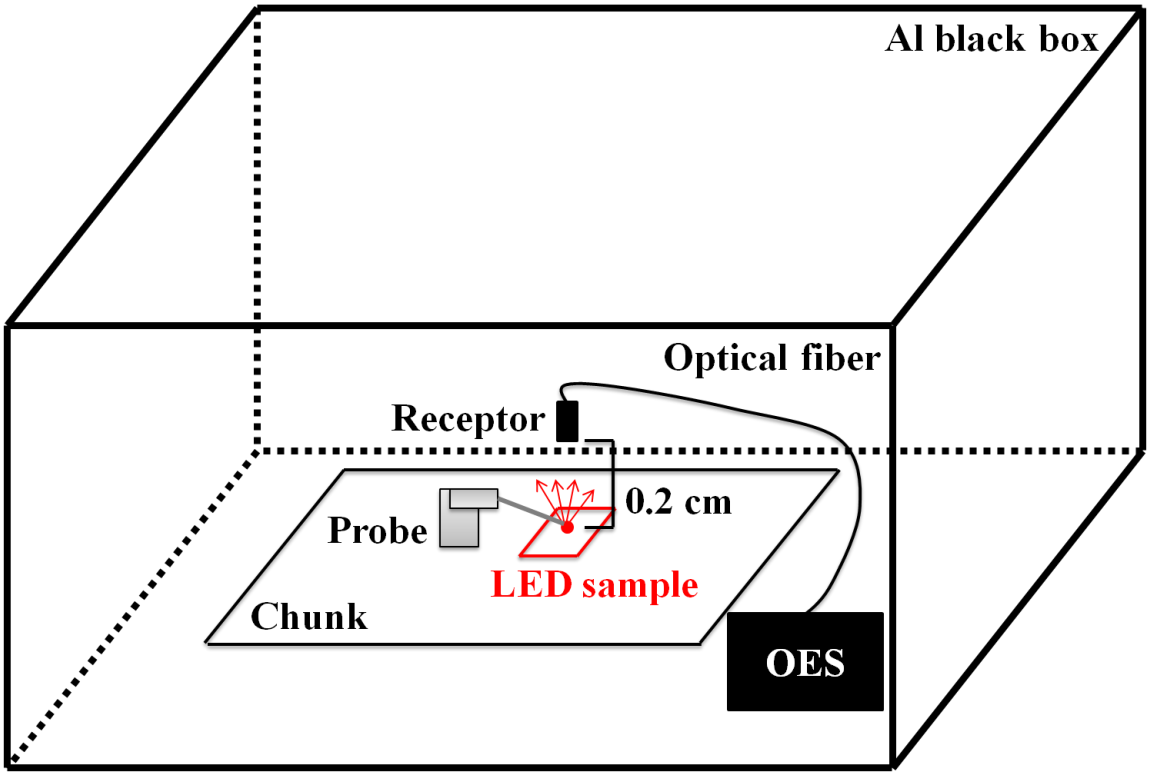


Figure 38. LED measurement set up.

2.7.2 Colorimetry

By using the light emission spectrum data acquired from the OES, other light characters such as the CIE chromaticity coordinates, correlated color temperature (CCT), and CRI can also be obtained for further describing the LED performance. The CIE 1931 color space was created by the International Commission on Illumination in 1931.[148] This color space can describe all visible colors to the human eye and can be shown as a three tristimulus values X, Y, and Z. The X, Y, and Z are expressed as following:

$$X \quad \int \quad I(\lambda)\bar{x}(\lambda)d\lambda \qquad [18]$$

$$\int \quad I(\lambda)\bar{y}(\lambda)d\lambda \qquad [19]$$

$$Z \quad \int \quad I(\lambda)\bar{z}(\lambda)d\lambda \qquad [20]$$

where $I(\lambda)$ is the spectral power distribution, $\bar{x}$, $\bar{y}$, and $\bar{z}$ are the color matching functions, which are similar to the spectral sensitivity of the cones in our eyes, and displayed in Figure 39.[149] Since it is hard to illustrate a three dimensional object and therefore, a two dimensional representation was launched:

$$x \quad \frac{X}{X \quad Z} \qquad [21]$$

$$y \quad \frac{}{X \quad Z} \qquad [22]$$

$$z \quad \frac{Z}{X \quad Z} \quad 1\text{-}x\text{-}y \qquad [23]$$

The new derived color space specified by x and y is widely used and can be plotted on the CIE 1931 chart as shown in Figure 40.[149] The ideal chromaticity coordinates for a white-light source are x=0.333, y=0.333, which is known as the equal energy point. The Planckian locus (also named black body locus) is also drawn in Fig. 40. The Planckian

locus is the locus that the color of an incandescent black body would take in the 1931 chromaticity space as the black body temperature changes.

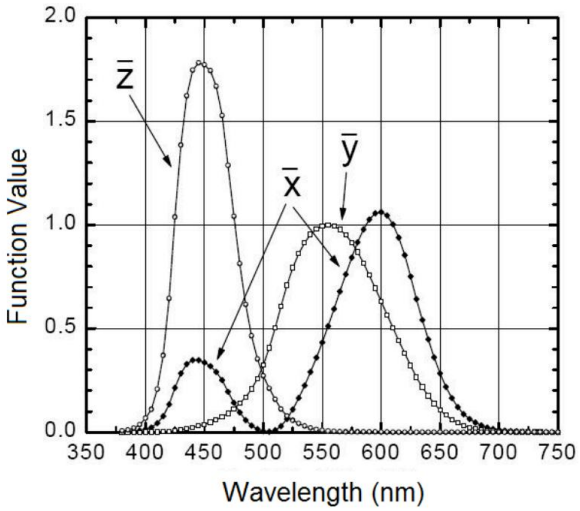


Figure 39. The 1931 CIE color-matching functions.[149]

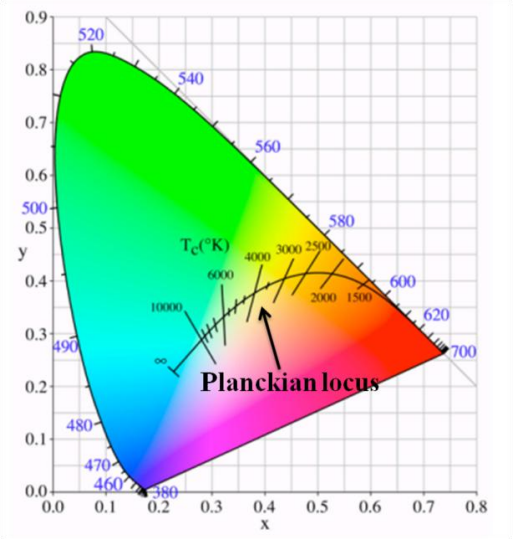


Figure 40. CIE 1931 chart.[149]

The CCT is a specification of the color appearance of the light emitted by a light source, relating its color to the color of light from a reference source (black body) when heated to a particular temperature, measured in degrees Kelvin (K). In general, for the purpose of calculating the CCT, the color coordinates of CIE 1931 need to be transformed into the color coordinates of CIE 1960. Then, the CCT of the LED is defined as the color temperature on the Planckian locus nearest to the color coordinates location on the CIE 1960 chart.[150] The light sources with the CCT rating below 3,200 K are considered as the "warm" sources, while those with the CCT above 4,000 K are considered as the "cool" sources. The conventional incandescent light has a CCT of 2,700 K. The CRI is a measure of the ability of a artificial light source to reproduce colors of an object illuminated by the light source. The scale of the color rendering index runs from 0 to 100. The larger value represents a more natural and vivid artificial light source. The distance between the color coordinates location on the CIE 1960 diagram and the Planckian locus, i.e., chromaticity distance, is used to calculate the CRI.[151] The literatures usually report two kinds of CRI, i.e., R_a and R_9. R_a is usually referred to the "general CRI" which is the average value of R_1 to R_8.[152] The R_a of a black body light source such as incandescent light bulb is 100. R_9 corresponds to the color rendering of the deep-red region, is usually referred to the "special CRI". The R_9 value is critical to the biomedical and painting applications.[153] In this dissertation, two kinds of CRIs were reported as the reference.

2.7.3 External Quantum Efficiency (EQE)

By definition, the EQE of the electroluminescence (EL), EQE_{EL}, is the number of photons emitted by the device (NP) divided by the total number of electrons injected as described in equation 24:[154,155]

$$EQE_{EL} \quad \frac{NP}{J/C} \qquad [24]$$

where is J is the current in amps (A) and C is the charge of an electron (1.602×10^{-19} C). The NP emitted by the device can be calculated using equation 25:[155]

$$\frac{\pi r}{A_{slit}} \int \frac{E(\lambda)\mathrm{d}\lambda}{\frac{hc}{\lambda}} \qquad [25]$$

where the $\pi r^2/A_{slit}$ is the factor of "Fraction of Light Collected", E(λ) is the irradiance of the light source, h is the Planck constant (6.626×10^{-34} J·S), λ is the wavelength, and c is the speed of light (3×10^8 m/s). There has a distance between the light source and the receptor of the optical fiber and therefore, the light intensity will be underestimated. In this case, the "Fraction of Light Collected" needs to be considered. The light is emitted isotropically from the device and the irradiance should be equal at all points along a hemispherical distance from the EL device. The reason why the hemisphere is used is because that there has no light emitted from the backside of the device. The πr^2 is the surface area of the hemisphere and the r is 0.2 cm in this dissertation.[155] The cross-sectional area of the optical fiber slit in this dissertation is 1,000 μm tall × 100 μm wide.

CHAPTER III

NANOCRYSTALLINE CADMIUM SELENIDE EMBEDDED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K NONVOLATILE MEMORIES*

3.1 Introduction and Motivation

The conventional FG NVM device contains a poly-Si layer embedded in the gate dielectric structure as the CTL, which has been reviewed in section 1.2. This poly-Si film can be replaced by a layer of nc-Si dots to prevent the total loss of the trapped charges from a single leakage path in the thin tunnel oxide layer. The nc-Si embedded SiO_2 gate dielectric has been used in commercial products.[30,156] However, for the nano size devices, SiO_2 is not an ideal dielectric material because 1) the electron and hole barrier heights between SiO_2 and Si wafer are large, i.e., 3.5 eV and 4.4 eV, respectively, and 2) it is easy to leak the stored charges through the ultra thin SiO_2 layer back to the Si wafer. These problems can be avoided when the SiO_2 is replaced with a high-k dielectric material, e.g., HfO_2 or ZrO_2.[75,157] Previously, it has been proved that the Zr-doped HfO_2 (ZrHfO) high-k dielectric has better electrical and material properties than the un-doped HfO_2 film, such as the lower EOT, Q_{ot}, D_{it}, and the higher amorphous-to-polycrystalline transition temperature.[158-159]

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* Part of data reported in this chapter is reproduced from "Memory Functions of Nanocrystalline Cadmium Selenide Embedded ZrHfO High-k Dielectric tack ", by Chi-Chou Lin and Yue Kuo, accepted for publication in the Journal of Applied Physics, 115, 084113 (2014), by permission of AIP-American Institute of Physics.

The electron barrier height between ZrHfO and Si is lower than that between SiO_2 and Si, i.e., 1.5 eV vs. 3.5 eV, which favors the high data writing speed. Based on the same EOT, a physically thicker ZrHfO film can be used to replace SiO_2 as the tunnel oxide in the NVM to extend the charge retention time.[160] The nc-Ge and nc-ZnO dots have been embedded in HfO_2 and ZrHfO high-k films, respectively, as the charge trapping media to achieve the better memory function.[161-162] Since CdSe is a n-type semiconductor with a large work function, i.e., between 4.8 eV and 5 eV,[60] it can be embedded in the gate dielectric layer to trap and retain charges for a long period of time. In addition, the energy band gap of CdSe is smaller than that of ZnO, i.e., 2.3 eV vs. 3.3 eV, which favors the former's charge retention capability.[61,162] Levichev et al., demonstrated that the nc-CdSe embedded SiO_2 memory device had a large memory window, e.g., a flat-band voltage (V_{FB}) shift of -2.5 V over the gate voltage (V_g) sweep range of -10 V to +10 V. However, it can only trap charges for a very short time, e.g., 35 min, and the charge trapping and detrapping mechanisms are not clear.[59] In this study, the nc-CdSe embedded ZrHfO high-k dielectric structure is used as the gate dielectric layer in the metal-oxide-semiconductor (MOS) capacitor to study the NVM characteristics.

3.2 Experimental

The MOS capacitor composed of nc-CdSe embedded ZrHfO high-k gate dielectric was fabricated on a HF cleaned p-type (10^{15} cm^{-3}) Si (100) wafer. The RF magnetron sputtering technique was used for the sample preparation. The (ZrHfO tunnel oxide/CdSe/ZrHfO control oxide) tri-layer was deposited in three steps sequentially in one pumpdown without breaking the vacuum. Both ZrHfO layers were deposited from

the Zr/Hf (12:88 wt%) target in the Ar/O_2 (1:1) mixture at 5 mTorr and 60 W, i.e., 2 minutes for the tunnel oxide layer and 10 minutes for the control oxide layer. The CdSe layer was deposited from the CdSe target with Ar at 5 mTorr and 60 W for 3 min and 5 min (named 3-min deposited and 5-min deposited, respectively). Then, the tri-layer was treated with a PDA step at 800°C and 900°C under the N_2 atmosphere for 3 min using a rapid thermal annealing machine (Modular Process Technology RTP-600S). The control sample, i.e., the MOS capacitor with the 12-minute sputter deposited ZrHfO gate dielectric layer, was prepared under the same PDA condition. The 80 nm ITO film with a conductivity of 3.2×10^{-3} Ω-cm, was sputter deposited on the tri-layer and wet etched into 100 μm diameter gate electrodes. The backside of the wafer was deposited with an Al layer to form the ohmic contact. The post metal annealing (PMA) step was done at 400°C under the H_2/N_2 (1:9) atmosphere for 5 min. Figure 41 shows the J-V curves of the four devices that separately contain 800°C and 900°C PDA conditions for 3-min and 5-min deposited samples. The V_g was swept from -6 V to +6 V. The 5-min deposited samples show much larger leakage current than that in the 3-min deposited samples in both negative and positive V_g ranges, which may be contributed by the larger defect density induced from the long CdSe deposition time. In addition, the C-V hysteresis curves swept from -6 V to +6 V and then back to -6 V were measured for the 3-min deposited samples fabricated under different PDA conditions, i.e., 800°C and 900°C, as shown in Figure 42. The fresh C-V curves, i.e., swept from -2 V to 1 V, are almost overlapped. However, the hysteresis phenomenon in the 800°C sample is much larger than that in the 900°C sample, which may be contributed to the size effect of the

nanocrystals. Therefore, the 3-min deposited sample with 800°C PDA condition was investigated in this study. Chemical bond structure of the dielectric stack was characterized with the X using the monochromatic Al Kα X-ray emission at 1486.6 eV. The background subtraction and peak fitting were performed using the software XPS Peak 4.1. The smallest mean squared error, i.e., $\Sigma \chi^2$ is achieved, for the peak fitting. The capacitor's C-V and G-V curves were measured with the Agilent 4284A LCR meter and J-V curves were measured with the Agilent 4155C semiconductor parameter analyzer, respectively. The V_{FB} was extracted from the C-V curve using the NCSU CVC program.[146]

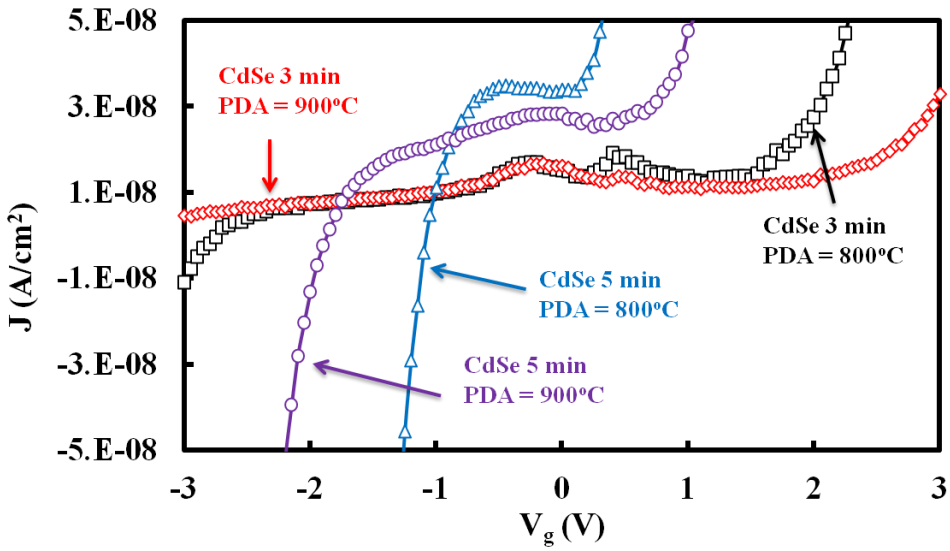


Figure 41. J-V curves for the 3-min and 5-min deposited nc-CdSe embedded samples.

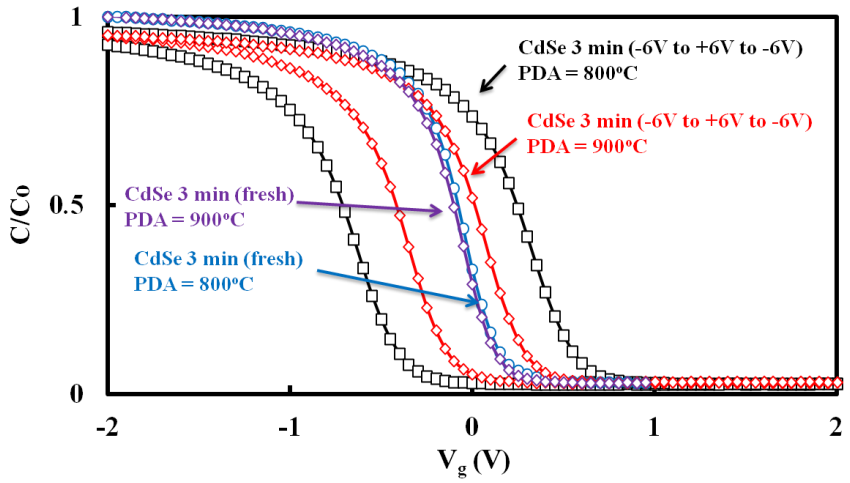
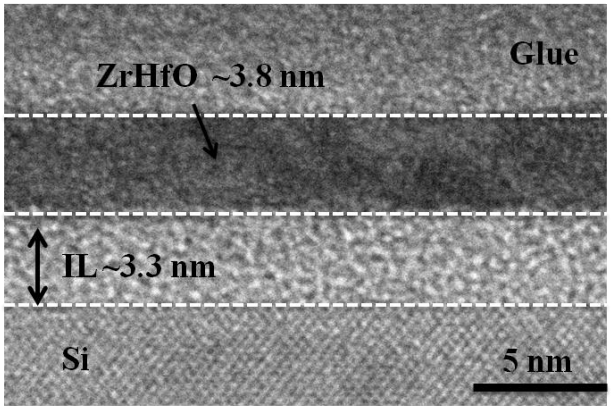


Figure 42. C-V hysteresis curves for the 3-min deposited nc-CdSe embedded samples with different PDA conditions. Fresh C-V curves are also included.

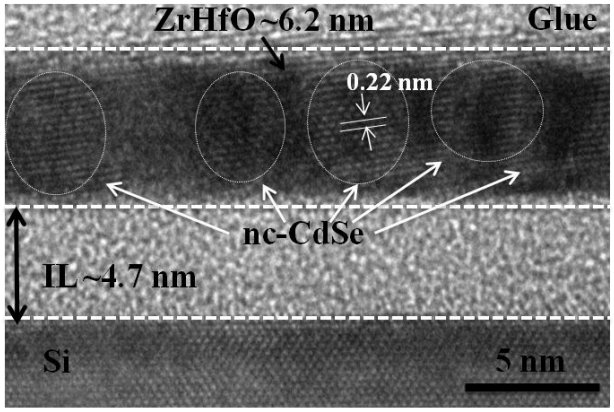
3.3 Material Properties of nc-CdSe Embedded ZrHfO High-K Gate Dielectric Stack

Figure 43 shows the cross-sectional HRTEM micrographs of (a) the control and (b) the nc-CdSe embedded samples. The control sample contains the amorphous ZrHfO film and an interface layer. The nc-CdSe embedded sample contains discrete nanodots in the amorphous ZrHfO film and a separate interface layer. The nanodot has the lattice fringe space of 0.22 nm corresponds to the CdSe (110) structure.[163] The thickness of the bulk ZrHfO film increases with the inclusion of the nc-CdSe layer, i.e., from 3.8 nm in the control sample to 6.2 nm in the nc-CdSe embedded sample. The interface layer between ZrHfO and Si is composed of Hf, Si, and O, i.e., a Hf-silicate ($HfSiO_x$) layer, which has been detected in other similar samples.[164] The IL thickness of the nc-CdSe sample is larger than that of the control sample, i.e., 4.7 nm vs. 3.3 nm. It was reported

that the oxygen diffusion through the amorphous film could be enhanced with the introduction of defects.[165] Since the CdSe bond length is different from those of the Hf-O and Zr-O, i.e., 2.61 Å vs. 1.80-1.83 Å and 1.80-1.82 Å,[166-167] respectively, the embedded dots can cause excessive stress and defects in the bulk ZrHfO film, which facilitates the growth of the interface layer.



(a)



(b)

Figure 43. Cross-sectional TEM micrograph of (a) the control sample and (b) the nc-CdSe embedded sample with 800°C PDA. IL represents the interface layer.

Figure 44 shows the XPS Hf 4*f* spectra of (a) the control and (b) the nc-CdSe embedded samples. Both samples contain the Hf $4f_{7/2}$ peak with the binding energy (BE) of 16.6 eV, which can be deconvoluted into two sub-peaks at 16.4 eV and 17.2 eV. The former is from HfO_2 in the bulk film[168-170] and the latter is from the $HfSiO_x$ interface layer adjacent to the Si substrate.[171] Compared with the control sample, the nc-CdSe embedded sample contains an additional Hf $4f_{7/2}$ peak at BE 17.4 eV, as shown in Fig. 44 (b), which may be from the HfO_x-like structure at the nc-CdSe/ZrHfO interface.[156] Figure 45 shows the XPS spectra of (a) Cd 3*d* and (b) Se 3*d* peaks in the nc-CdSe embedded sample, and (c) Si 2*p* and (d) Zr 3*d* peaks in both the control and the nc-CdSe embedded samples. The Cd and Se peaks in Fig. 45 (a) and (b) confirm the existence of the CdSe in the nc-CdSe embedded sample.[172-174] The Si 2*p* peak at BE of 99.8 eV in both samples is from the Si-Si bond of the Si substrate.[175] The Si 2*p* peak at BE 102.4 eV in the control sample is from the $HfSiO_x$ interface layer.[159,176] The nc-CdSe embedded sample has an additional Si peak at BE 103.1 eV, which is from the SiO_2-like $HfSiO_x$ group.[159] It was reported that the Hf dangling bond can be formed during the high temperature PDA process.[177] When the density of the dangling bonds in the film is large, Hf can diffuse toward the Si and react with oxygen at the substrate interface.[178-179] The embedded nc-CdSe probably forms an interface layer with ZrHfO, which contains the Cd-Hf or Se-Hf bond just like the Pt-Hf bond formation in the $TiN/Pt/HfO_2/Si$ structure.[180] There are less Hf dangling bonds in the bulk ZrHfO film to diffuse to the interface layer, which is the cause of the formation of the SiO_2-like $HfSiO_x$ group. The Zr $3d_{5/2}$ peak at BE 182.1 eV and Zr $3d_{3/2}$ peak at BE 184.5 eV in Fig. 45 (d) are from

the ZrO_2 compound in the bulk film.[181] There is almost no difference in the ZrO_2 BE's between the control and nc-CdSe embedded samples. Therefore, the inclusion of nc-CdSe in the ZrHfO film does not affect the chemical binding states of the small amount of Zr in the bulk ZrHfO film.

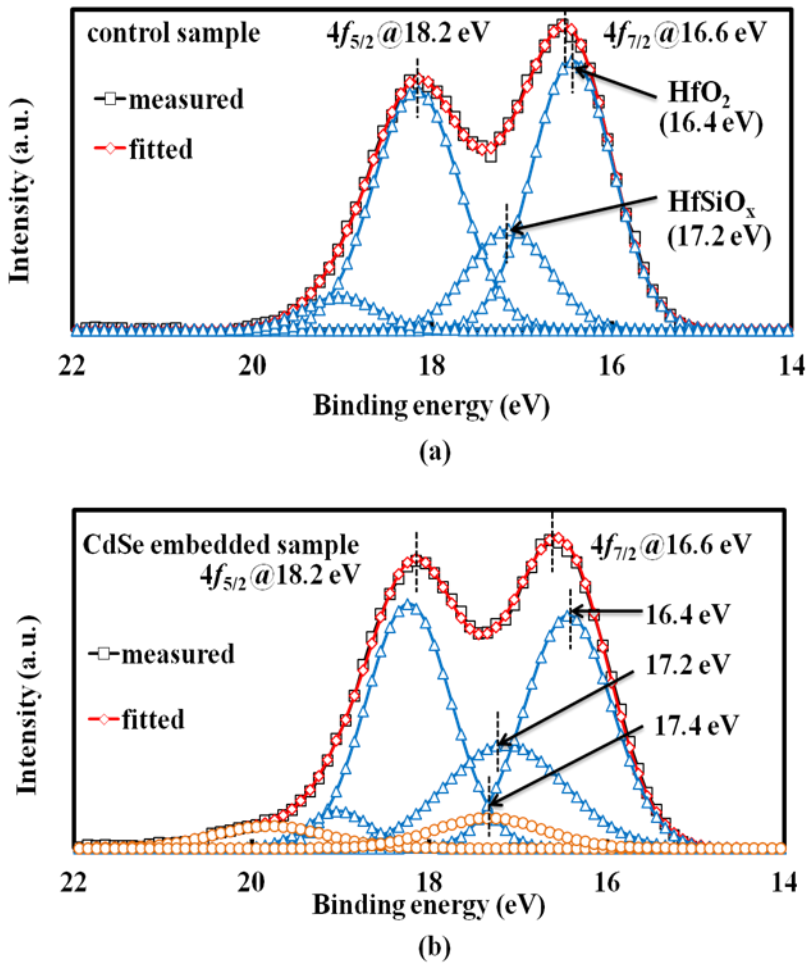


Figure 44. XPS Hf 4*f* spectra of (a) control and (b) nc-CdSe embedded samples. Peaks are deconvoluted.

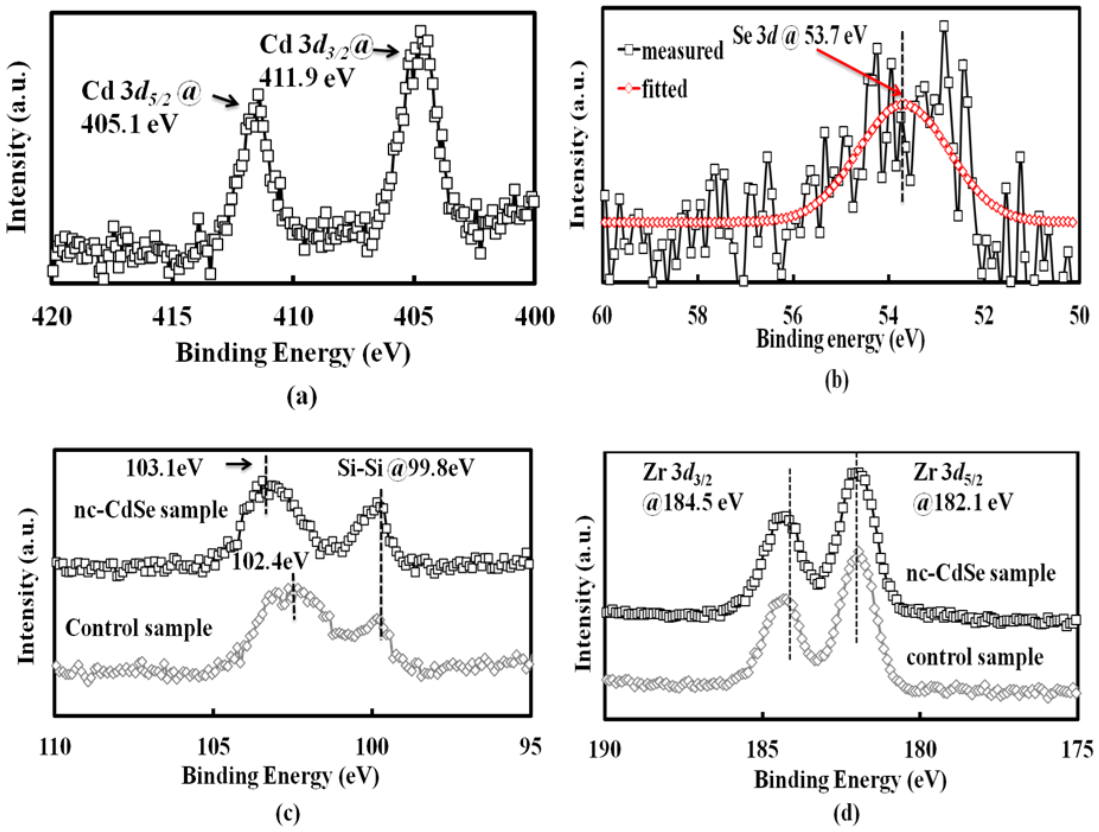


Figure 45. XPS spectra of (a) Cd 3*d* and (b) Se 3*d* of nc-CdSe embedded sample and (c) Si 2*p* and (d) Zr 3*d* of control and nc-CdSe embedded samples.

3.4 Electrical Properties of nc-CdSe Embedded ZrHfO High-K MOS Capacitor

3.4.1 Memory Functions Contributed by Hole and Electron Trapping

Figure 46 shows the C-V hysteresis curves of the control and nc-CdSe embedded samples measured at 1 MHz and room temperature with V_g swept from -7 V to +7 V, i.e., forward, and then back to -7 V, i.e., backward. The fresh C-V curve of the nc-CdSe embedded sample, which was measured from -2 V to +1 V to minimize charge trapping in the gate dielectric, is included in Fig. 46. The C-V curves are drawn in a small V_g

range of -2 V to +2 V for better exhibition of the hysteresis phenomenon. The control sample has a very small C-V hysteresis with the V_{FB} gap between the forward and the backward curves of 0.04 V due to the poor charge trapping capability of the bulk ZrHfO film and the $HfSiO_x$ interface. The nc-CdSe embedded sample has a much larger V_{FB} gap of 1.08 V. Compared with the V_{FB} of the fresh C-V curve ($V_{FB,fresh}$), the V_{FB} of the forward C-V curve ($V_{FB,forward}$) of the nc-CdSe embedded sample shifts toward the negative V_g direction by -0.64 V and the V_{FB} of the backward C-V curve ($V_{FB,backward}$) shifts toward the positive V_g direction by 0.44 V. Therefore, holes and electrons are trapped to the nc-CdSe site under the negative and positive V_g stress conditions, respectively.[162,164] The Q_{ot} of the control and nc-CdSe embedded samples are estimated to be 1.14×10^{11} cm^{-2} and 3.45×10^{12} cm^{-2}, respectively, based on the following equation:[164]

$$Q_{ot} \quad \frac{C\times\Delta V_{FB}}{q} \qquad [26]$$

where C is the capacitance in the saturated accumulation region, i.e., 4.81×10^{-11} F and 3.85×10^{11} F for the control sample and nc-Cd e embedded sample, respectively. ΔV_{FB} is $V_{FB,backward}$ - $V_{FB,forward}$, and q is the electron charge. The amount of charges trapped to the nc-CdSe embedded sample is about twenty times that of the control sample. Therefore, the embedded nc-CdSe is an effective charge trapping medium in the ZrHfO film. The inset in Fig. 46 shows the memory window, i.e., ΔV_{FB}, of the nc-CdSe embedded sample in various V_g sweeping ranges. The V_{FB}'s of the forward and backward C-V curves shift more toward the negative and positive V_g directions, respectively, with the increase of the V_g sweeping range. Therefore, the enlargement of

the memory window is due to increases of electrons and holes trappings in the large V_g sweep range.

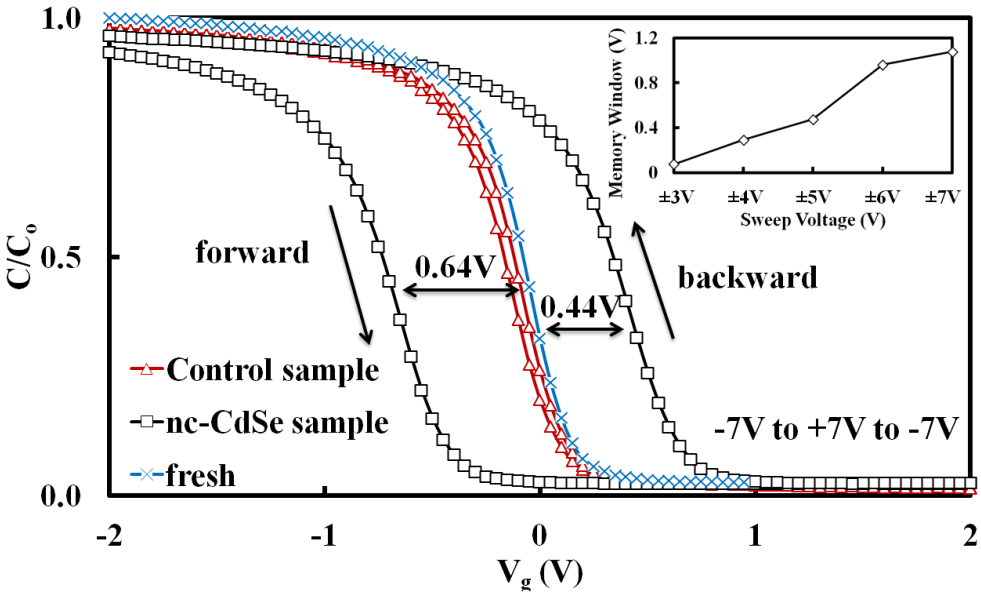


Figure 46. C-V hysteresis of control and nc-CdSe embedded samples in V_g range of ±7 V. Inset: memory windows of nc-CdSe embedded sample in V_g sweep ranges of ±3 V to ±7.

3.4.2 Differentiation of Hole and Electron Trapping

The charge-trapping mechanism of the nc-CdSe embedded sample was evaluated using the constant voltage stress (CVS) method. Before the stress test, the fresh C-V curve was measured over a small V_g range of -2 V to +1 V at 1 MHz. After the sample was stressed with a V_g for a period of time t, the C-V curve was measured in the same V_g range and the V_{FB} was calculated. Figure 47 shows curves of the V_{FB} shift, i.e., V_{FB}

after stress $-V_{FB}$ of the fresh sample, vs. stress time at V_g = -8 V and +8 V, respectively. The amount of charges stored in the device is proportional to the magnitude of the V_{FB} shift.[182] At V_g = -8 V, the V_{FB} moves to the negative V_g direction and with the increase of the stress time, the V_{FB} shift increases, e.g., -0.4 V after 1 ms and -1.01 V after 30 sec. After 30 sec, the hole trapping is saturated. The similar time-dependent electron trapping trend is observed. At V_g = +8 V, the shift of V_{FB} is +2 mV after 1 ms and 0.58 V after 30 sec. The saturation of electron trapping also occurs after 30 sec. When stress V_g's are of the same magnitude but different polarities, for the same period of time, more holes than electrons are trapped to the nc-CdSe site, e.g., V_{FB} shift of -0.4 V and +2 mV after V_g = -8 V and +8 V stress for 1 ms, respectively. There are several possible explanations for this phenomenon. First, the CdSe is a n-type semiconductor material, which can trap more holes than electrons.[164] Second, since the substrate is the p-type Si wafer, i.e., it is easier to form the hole-rich accumulation layer than the electron-rich inversion layer under the same magnitude of V_g.[183] Third, holes and electrons may be trapped at different sites of the embedded nanocrystals. Figure 48 shows the band diagram of the nc-CdSe embedded sample under the (a) unbiased, (b) $+V_g$, and (c) $-V_g$ stress conditions. Assuming that the work function and the band gap energy of the nc-CdSe are as the same as those of the bulk CdSe, the conduction and valence band offsets of the nc-CdSe to the Si substrate are different, as shown in Fig. 48 (a). Fig. 48 (b) and (c) show diagrams corresponding to the electrons and holes trapping conditions, respectively. Under the negative V_g stress condition, holes tunnel through both the interface and the tunnel oxide layers and therefore, can be trapped to the nc-CdSe/ZrHfO interface. The

similar trapping mechanism has been reported by Xu, et al.[184] on the Au-Al_2O_3 core shell nanocrystals embedded HfO_2 NVM.

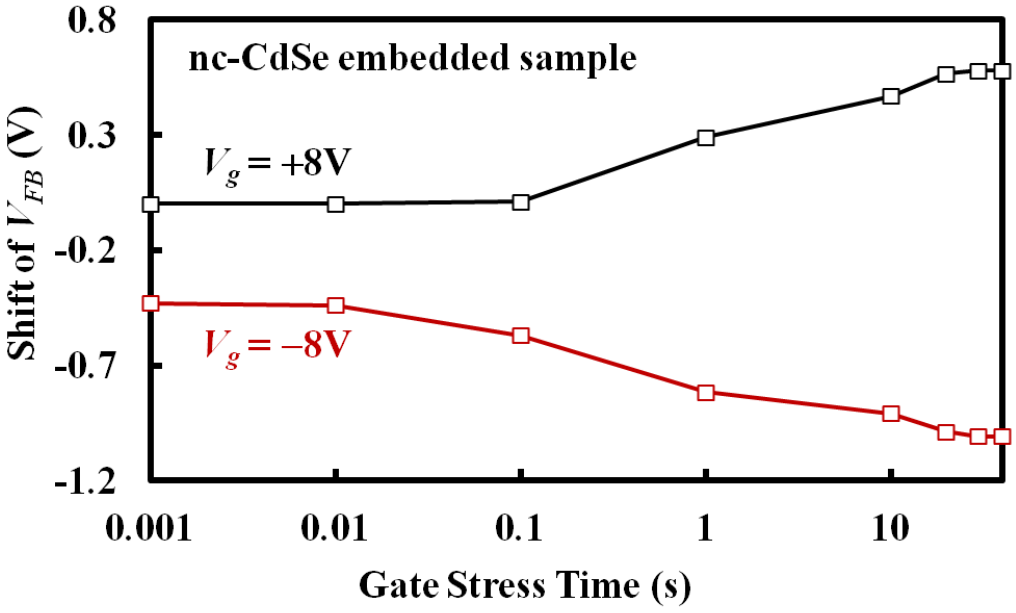


Figure 47. Shift of V_{FB} of nc-CdSe embedded sample at V_g -8 V and +8 V and different stress times.

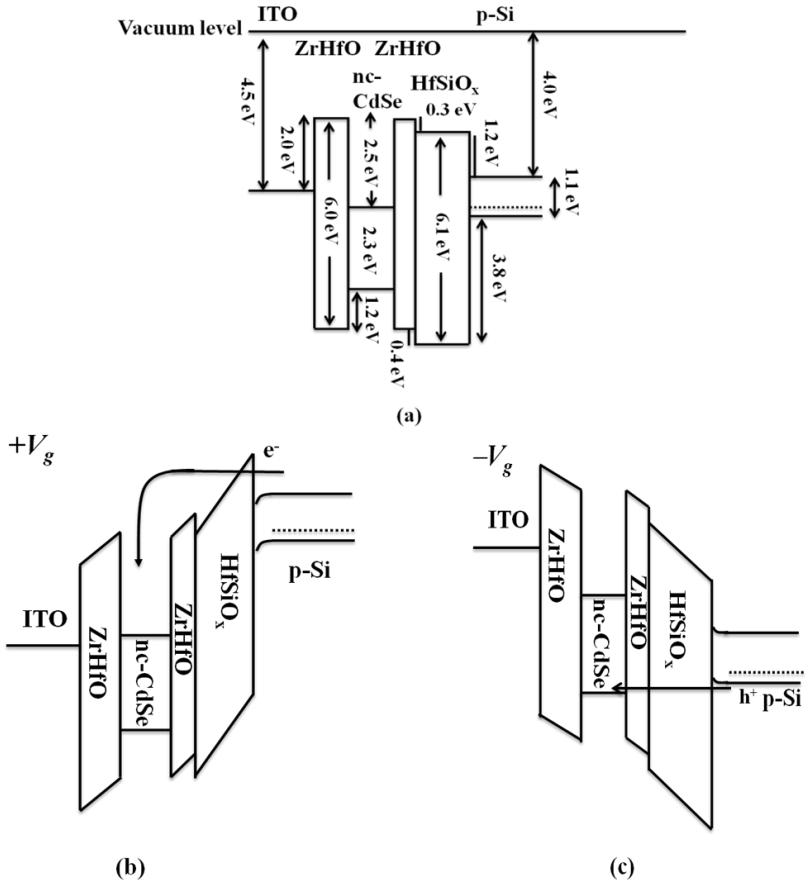


Figure 48. Energy band diagrams of nc-CdSe embedded sample under (a) unbiased, (b) $+V_g$, and (c) $-V_g$ conditions.

3.4.3 Differentiation of Charge Trapping Sites

In the nc-CdSe embedded sample, charges can be stored either in the bulk nc-CdSe dot or at the nc-CdSe/ZrHfO interface. The frequency dispersion method was used to identify the charge trapping site. Figure 49 and Figure 50 show the C-V curves of the control and nc-CdSe embedded samples at 100kHz, 500kHz, and 1MHz, respectively. The V_g was swept from -6 V to +6 V or +6 V to -6 V for the hole or electron trapping

condition. Curves in Fig. 49 and Fig. 50 are drawn in a small V_g range of -2 V to +2 V for better exhibition of the dispersion phenomena. For the control sample, as shown in the Fig. 49 (a) and (b), the C-V curves do not disperse with the change of the frequency in either the -6 V to +6 V or +6 V to -6 V sweep direction. Therefore, neither the bulk ZrHfO film nor the $HfSiO_x$ interface layer respond to the frequency change. For the nc-CdSe embedded sample, when the V_g is swept from -6 V to +6 V, with the decrease of the frequency, the C-V curve stretches and the V_{FB} shifts toward the positive V_g direction as shown in Fig. 50. It was reported that shallow-trapped holes, i.e., at the nanocrystals/surrounding oxide interface, responded to the low measurement frequency.[185] When the band structure moves to the flat-band condition, holes trapped at the nc-CdSe/ZrHfO interface may tunnel back to the Si substrate, and therefore, more positive V_g is needed to reach the flat-band condition, which shows the stretch of the C-V curve to the positive V_g direction. Therefore, some of the trapped holes are probably located at the ZrHfO/nc-CdSe interface. On the other hand, since the electron trapping curve, i.e., V_g swept from +6 V to -6 V in Fig. 50, almost does not respond to the frequency change, the electrons are probably deeply trapped in the bulk nc-CdSe site. The G-V curves of the nc-CdSe embedded sample swept from -6 V to +6 V and from +6 V to -6 V are drawn to provide further insights into the electrical properties of the device as shown in Figure 51. The magnitude of the conductance peak in both curves decreases with the reduction of the measurement frequency. At the low measurement frequency, interface traps could keep pace with the ac signal change, which reduces the energy loss of the capacitor.[18, 186-187] The smaller energy loss induces the lower conductance peak.

The decrease of the conductance peak height in the G-V curves from -6 V to +6 V is more pronounced than that in the G-V curves from +6 V to -6 V, e.g., by two times. The shallow-trapped holes at the nc-CdSe/ZrHfO interface can respond to the low measurement frequency, i.e., 100 kHz, and tunnel back to the Si wafer. The exchange of the holes between the nc-CdSe/ZrHfO interface and Si wafer reduces the energy loss, which causes the larger drop of the conductance peak.[187] The C-V and G-V responses to the frequency dispersion are consistent with the CVS result and the band diagrams.

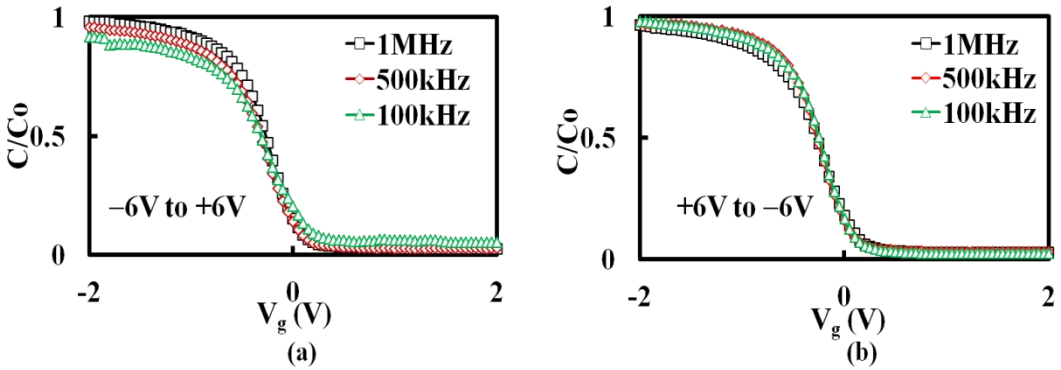


Figure 49. Frequency-dependent C-V curves of control sample with V_g swept from (a) -6 V to +6 V and (b) +6 V to -6 V.

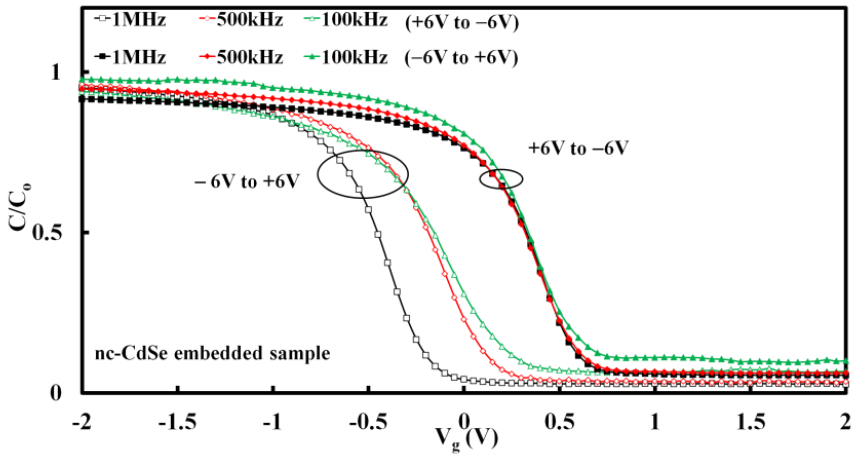


Figure 50. Frequency-dependent C-V curves of nc-CdSe embedded sample with V_g swept from -6 V to +6 V and +6 V to -6 V.

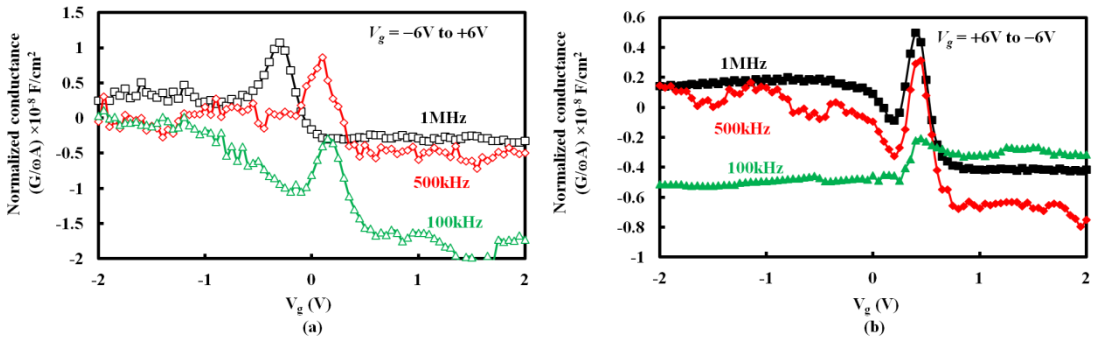


Figure 51. Frequency-dependent G-V curves of nc-CdSe embedded sample with V_g swept from -6 V to +6 V and +6 V to -6 V.

3.4.4 Current Transfer Characteristics

The charge trapping process is related to the leakage current pattern. Figure 52 shows the hysteresis curves of the leakage current density (J) vs. V_g of the control and

nc-CdSe embedded samples with the V_g swept from -6 V to +6 V (forward) and then back to -6 V (backward). The polarity of J is defined as negative when the current flows toward the gate and positive when the current flows toward the Si substrate. For both samples in the range of V_g = -6 V to 0 V, the polarity of the J changes from negative to positive in the middle of the V_g sweep. At V_g = -6 V, a large number of holes are injected from the p-type Si to the high-k stack. With the reduction of the magnitude of the V_g, some of the holes cannot be retained in the dielectric stack and therefore, tunnel back to the Si wafer. When the number of detrapped holes are larger than that of the injected holes, the positive J is observed. The transition of the current polarity for the control sample occurs at V_g = -4.1 V and that for the nc-CdSe embedded sample occurs at V_g = -2.8 V. The difference is due to the strong hole trapping capability of the embedded nc-CdSe sample. For both samples, a peak in the J-V curve at near V_g = 0 V, i.e., point A for the nc-CdSe embedded sample and point B for the control sample, is observed. This peak is due to the further release of the holes upon the change of the polarity of the applied V_g.[183] The J-V curve of the nc-CdSe embedded sample shows another peak, i.e., point C at V_g = +0.45 V. When the V_g is slightly larger than 0 V, the injected electrons create the repulsion force, i.e., Coulomb blockade effect, which prevents the further injection of the electrons. Therefore, a negative differential resistance peak is observed at point C. The Coulomb blockade effect is commonly observed in the nanocrystal-embedded SiO_2 or high-k sample.[188-195] With the increase of the $+V_g$, the inversion layer is fully established and more electrons are tunneled through the dielectric stack. Therefore, the Coulomb blockade effect is eliminated and the

leakage current increases with the increase of V_g. The control sample has very poor electron-trapping capability and therefore, does not show the Coulomb blockade effect. In the reverse J-V curves, i.e., from V_g = +6 V to 0 V, the polarity of J changes from positive to negative in the middle of the V_g sweep range with the transition occurs at V_g = +2.7 V and +2.15 V for the control and nc-CdSe embedded samples, respectively. Also, similar to the forward curve case, the leakage current curves show peaks at near V_g = 0 V, i.e., point D for the nc-CdSe embedded sample and point E for the control sample. The difference of the transition V_g's and the existence of these peaks are related to the charge retaining capabilities of these dielectric stacks.

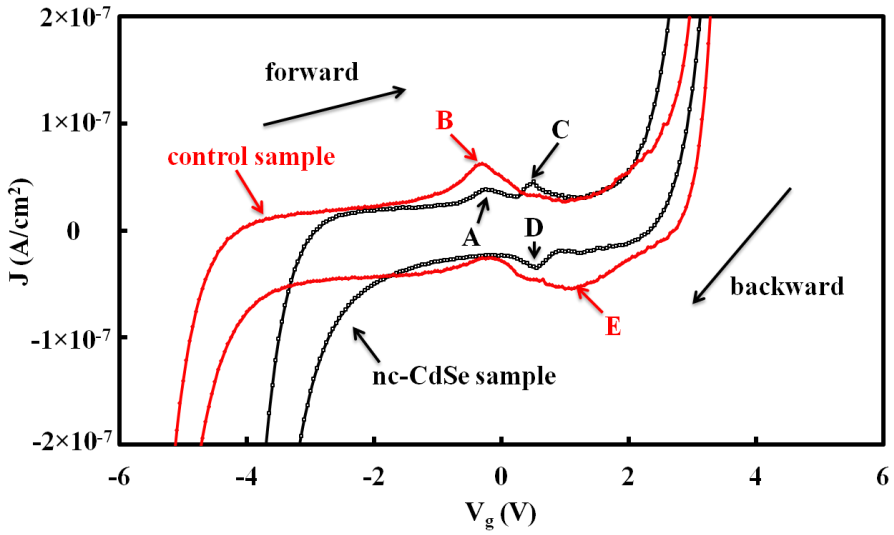


Figure 52. J-V hysteresis curves of control and nc-CdSe embedded samples. V_g range ±6 V.

3.4.4 Retention Characteristics of Holes and Electrons

The charge retention capability of the capacitor can be expressed as the percentage of the trapped charge remained in the device after releasing the stress voltage, as shown in the following equation:[189]

$$\text{charge remaining } (\quad) \quad \frac{V_{FB}(t)-V_{FB,fresh}}{V_{FB,stress}-V_{FB,fresh}} \qquad [27]$$

where $V_{FB,stress}$ is the V_{FB} immediately after the release of the stress voltage, $V_{FB,fresh}$ is the V_{FB} before the stress, and $V_{FB}(t)$ is the V_{FB} after releasing the stress voltage for a period of time t. The $V_{FB}(t)$ is determined from the C-V curve measured in a small range of -2 V to +1 V at time t. Figure 53 shows the charge retention curves of the nc-CdSe embedded sample after being stressed at V_g = -8 V and +8 V for 10 seconds, respectively. The V_{FB} was recorded every 1,800 s until 10 hours after the release of the stress voltage. In the first 1,800 s of the V_g = -8 V curve, about 16% of the originally trapped holes were probably loosely trapped at the nc-CdSe/ZrHfO interface, which could be released easily. The remaining holes were strongly retained by the nc-CdSe and slowly detrapped, e.g., only 9% was lost between t = 1,800 s and 36,000 s. On the other hand, only 6% of the originally trapped electrons were lost in the first 1,800 s, as shown in the V_g = +8 V curve, because most of them were deeply trapped in the bulk nc-CdSe. Between 1,800 s and 36,000 s, electrons were detrapped at a higher rate than holes were, i.e., 12% vs. 9%. This phenomenon can be contributed to the material property of the n-type nc-CdSe, which prefers to trap holes than electrons. The same two-stage charge detrapping phenomenon has been observed in other nanocrystalline embedded memory devices.[164,183] The inset of the Fig. 53 shows that when the curve is extrapolated to 10

years, more holes than electrons can be retained in the sample, i.e., 56% vs. 37%, which can also be explained by the preference of holes than electrons of the n-type CdSe nanodots.

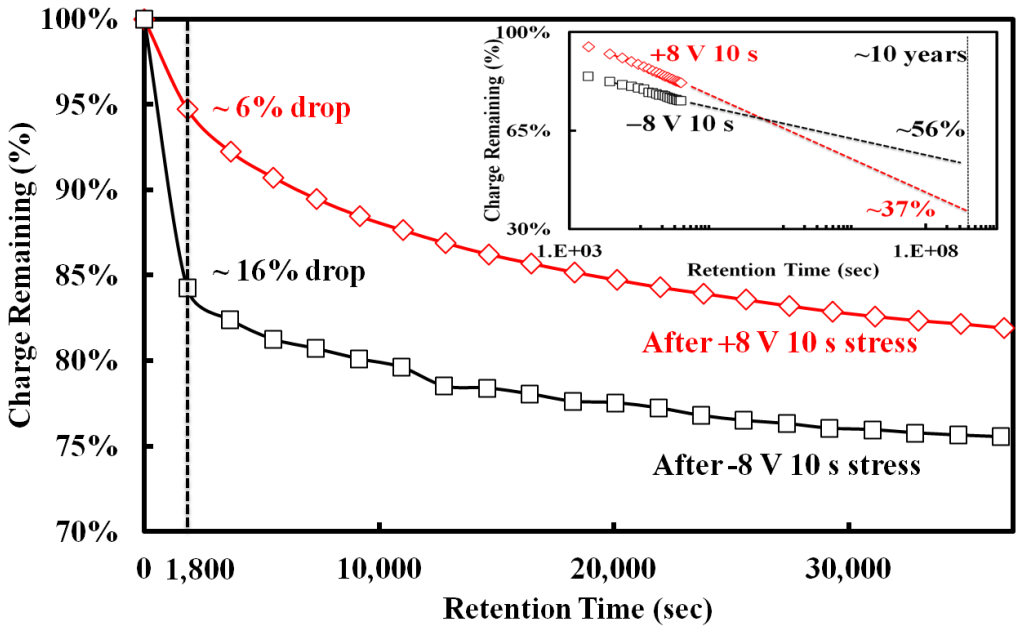


Figure 53. Charge retention characteristics of nc-CdSe embedded sample. Inset: 10-year extrapolation.

3.5 Summary

The nc-CdSe embedded ZrHfO high-k memory devices have been fabricated and investigated for the material properties and memory functions. The formation of the discrete nc-CdSe dots in the amorphous ZrHfO film on top of an interface layer is confirmed by the TEM photo. The nc-CdSe/ZrHfO interface structure is different from

that of the bulk CdSe or ZrHfO, which can be related to the charge trapping and retaining mechanisms. The nc-CdSe embedded sample can trap much more charges than the control sample, i.e., by 20 times. Both holes and electrons can be trapped to the nc-CdSe site depending on the polarity of the applied gate voltage. More holes than electrons can be trapped to the nc-CdSe embedded sample. From the frequency dispersion measurement, charges are stored to the nc-CdSe site in two states: loosely trapped at the nc-CdSe/ZrHfO interface or strongly trapped to the bulk nc-CdSe. Electrons trapped in the nc-CdSe embedded sample cause the Coulomb blockade effect. The embedding of nc-CdSe into the high-k film induces a larger leakage current because of the creation of excessive defects. Charges can be retained at the nc-CdSe site even after the breakdown of the high-k stack. More than 56% of the originally trapped holes remain in the device after 10 years. The nc-CdSe embedded ZrHfO high-k dielectric stack has good charge trapping and retaining properties, which is suitable for nonvolatile memory devices.

CHAPTER IV

TEMPERATURE EFFECTS ON NANOCRYSTALLINE MOLYBDENUM OXIDE EMBEDDED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K NONVOLATILE MEMORY FUNCTIONS*

4.1 Introduction and Motivation

In Chapter III, discrete nc-CdSe embedded ZrHfO high-k MOS capacitor has been fabricated and studied. This kind of device showed promising memory characteristics that can meet the nonvolatile memory operation requirements. However, the device performances were all measured under the room temperatures. Previously, the nc-MoO_3 embedded ZrHfO MOS capacitor has been fabricated and investigated.[188] Good charge trapping and retention capabilities have been presented due to the good thermal stability and large work function of MoO_3. The reliability of this nc-MoO_3 embedded ZrHfO memory device, especially at different temperatures, has never been studied. The temperature is an important factor for the memory device since the device degradation process can be accelerated at the high temperature,[189] it is imperative to understand the temperature effect on the charge trapping and retention mechanisms. In this study, the influence of temperature on the memory function of the nc-MoO_3 embedded ZrHfO MOS capacitor has been investigated.

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* Part of data reported in this chapter is reproduced from "Temperature Effects on Nanocrystalline Molybdenum Oxide Embedded ZrHfO High-k Nonvolatile Memory Functions", by Chi-Chou Lin and Yue Kuo, accepted for publication in the Journal of Solid State Science and Technology, 2, Q16-Q22 (2013) by permission of ECS-The Electrochemical Society.

4.2 Experimental

MOS capacitors with the ZrHfO (tunnel oxide)/MoO_3/ZrHfO (control oxide) gate dielectric stack were prepared by sputter deposition on the dilute HF cleaned p-type (10^{15} cm^{-3}) Si (100) wafer in a one pumpdown process. The ZrHfO films were deposited from the Zr/Hf (12:88 wt%) target in the Ar/O_2 (1:1) mixture at 5 mTorr and 60 W, i.e., 2 min for the tunnel oxide and 10 min for the control oxide. The MoO_3 film was deposited from the Mo target in the Ar/O_2 (1:1) mixture at 5 mTorr and 100 W for 15 s. The PDA step was done at 800°C for 1 min under the N_2 atmosphere by the same equipment as mentioned in Chapter III. After PDA, the as-deposited amorphous MoO_3 film was transformed into the nanocrystalline MoO_3, which was confirmed with the XPS and XRD, respectively, in the previous studies.[188,196] The Al gate electrode was prepared by sputtering and wet etching. The backside of the wafer was deposited with Al to form the ohmic contact. The PMA step was done at 300°C for 5 min under the H_2/N_2 (1:9) atmosphere. The control sample, i.e., ZrHfO gate dielectric layer without the embedded nc-MoO_x layer, was prepared under the same condition, i.e., sputtering from the Zr/Hf (12:88 wt%) target for 12 minutes. The wafer was loaded on the chuck of the probe station of which the temperature was controlled with a Signatone S-1060R thermal probing system. The capacitor's J-V, C-V, and G-V curves were measured by the same equipments used in Chapter III.

4.3 Material Properties of nc-MoO_3 Embedded ZrHfO High-K Gate Dielectric Stack

Figure 54 shows the XPS O 1*s* peak of the nc-MoO_3 embedded ZrHfO high-k stack prepare in this study. It has been deconvolued into 4 sub peaks. The peak with the binding energy (BE) of 530.3 eV is MoO_3. Peaks with BE 529.6 eV and 531.3 eV are related to HfO_2 and ZrO_2. The peak with BE 532.3 eV is probably contributed by the Al_2O_3 from the gate electrode. A small Mo $3d_{5/2}$ peak at 227.3 eV BE was detected, which is the Mo^{6+} element.[197] There is a crystalline MoO_3 peak detected by X-ray diffraction (XRD), i.e., θ .9 ^{o} as shown in Fig. 54 (b). The crystal size is about 28 nm, determined using the Scherrer equation.[198] The EOT's of the control sample and the nc-MoO_x embedded sample were 7.8 nm and 8.5 nm, respectively, calculated from the C-V curves.

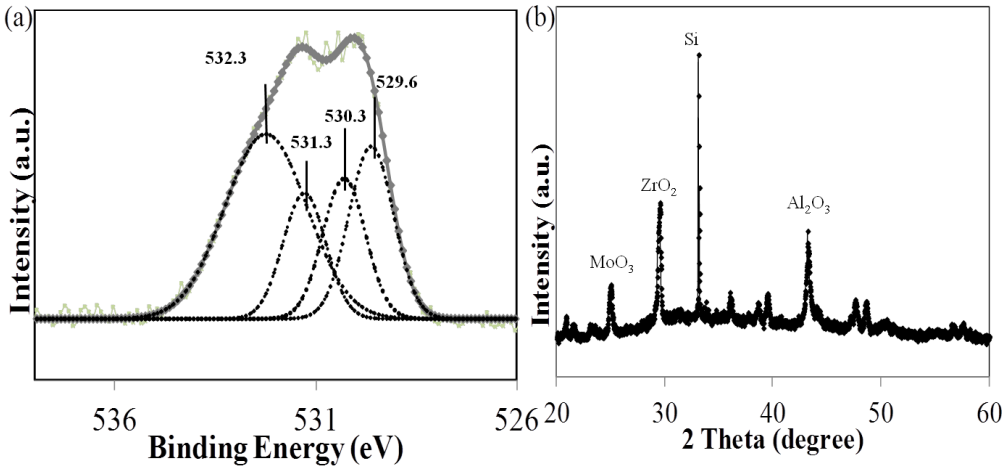


Figure 54. (a) XPS O 1s peak, and (b) XRD pattern of the nc-MoO_3 embedded ZrHfO sample.

4.4 Temperature Effects on Electrical Properties of nc-MoO_3 Embedded ZrHfO High-K MOS Capacitor

4.4.1 Temperature Effect on Charge Transfer Mechanism

Figure 55 shows J-V curves of the (a) control and (b) nc-MoO_3 embedded ZrHfO samples with V_g swept from -6 V to +6 V at 25°C, 75°C, and 125°C, respectively. Fig. 55 (a) shows that for the control sample, the leakage current increases with the increase of voltage in both $-V_g$ and $+V_g$ ranges at all temperatures with a jump A near $V_g = 0$ V. On the other hand, Fig. 55 (b) shows that for the nc-MoO_3 embedded sample at 25°C, there are two peaks in the $+V_g$ range. The jump at point B near $V_g = 0$ V is contributed by the same reason as the jump A that the quick release of the holes trapped in shallow traps from the high-k stack. The peak at point C near $V_g = +1$ V is known as the negative differential resistance due to the Coulomb blockade effect, which has been observed in many nanocrystals embedded SiO_2 or high-k memory devices under the room temperature.[186-194] When the V_g is increased further, the Coulomb blockade effect is suppressed and the tunneling current increases rapidly. At 75°C and 125°C, the current leakage peaks are not observed because the high temperature provides the high thermal energy to charges for easy transfer through the dielectric stack.[199-200]

At $V_g = -6$ V, holes were accumulated near the Si/high-k interface and transferred toward the gate direction. When the magnitude of the V_g was reduced, the amount of holes transferred in this direction was reduced. At the same time, those holes trapped in shallow traps, e.g., at the nc-MoO_3 site in the gate dielectric layer, tunneled back to the Si substrate.[183,188] Eventually, currents toward the gate and the Si directions become

equal at a V_g where the polarity of J changes. For the nc-MoO_3 embedded sample at 25^{o}C, the polarity of J changes at -2.6 V. However, the magnitude of V_g of the transition condition decreases with the increase of temperature, i.e., -2.1 V at 75^{o}C and -1.85 V at 125^{o}C, probably due to that more holes were trapped to the nc-MoO_3 site at the higher temperature. The high temperature provides holes with extra thermal energy to overcome the barrier height at the Si/high-k interface to reach the embedded nc-MoO_3 site.[201] The phenomenon of the polarity change also depicts that the hole injection from the Si substrate instead of the gate electron injection was the dominant conduction mechanism under the $-V_g$ condition. Moreover, Fig 55 (b) shows that in the $+V_g$ range, the J increases with the increase of temperature, i.e., at V_g = 2.5 V, J = 1.97×10^{-7} A/cm^2 at 25^{o}C vs. J = 1.05×10^{-6} A/cm^2 at 125^{o}C. In the $+V_g$ range, the transfer of the minority carriers through the high-k stack mainly contributes to the leakage current. Under the same $+V_g$ bias, the high temperature condition favors the inversion layer formation more than the low temperature condition. Also, the high-k film's electrical conductivity increases with the increase of the temperature. Both factors favor the high leakage current at the high temperature.[201] The same phenomenon has been observed in the $-V_g$ range and can be explained by the similar reason. In addition, although it is easier to form the hole-rich accumulation layer than the electron-rich inversion layer on the p-type Si wafer with V_g's of the same magnitude but different polarities, the absolute value of J at the $+V_g$ is larger than that at the $-V_g$. This can be contributed to that only part of the injected holes can be transported through the dielectric layer, i.e., a large percentage

of them were trapped in the nc-MoO_3 site or the nc-MoO_3/high-k interface or tunneled back to the Si substrate.

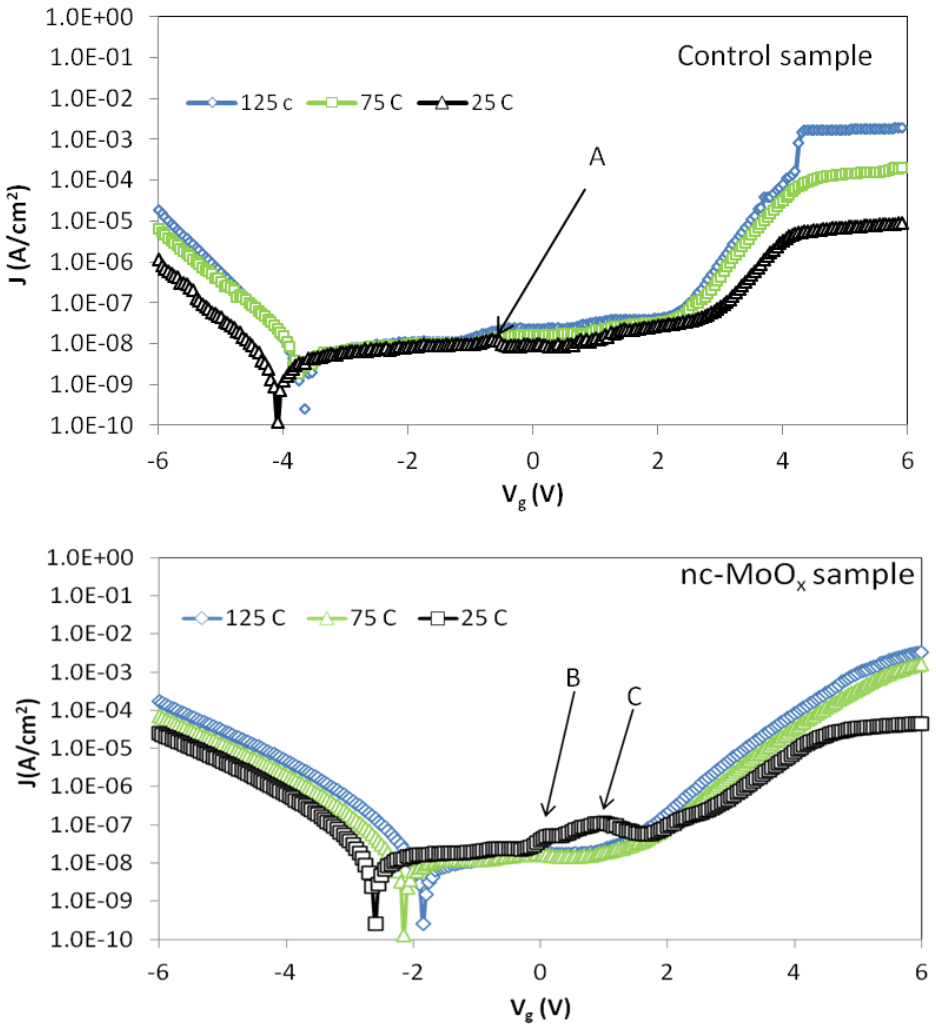
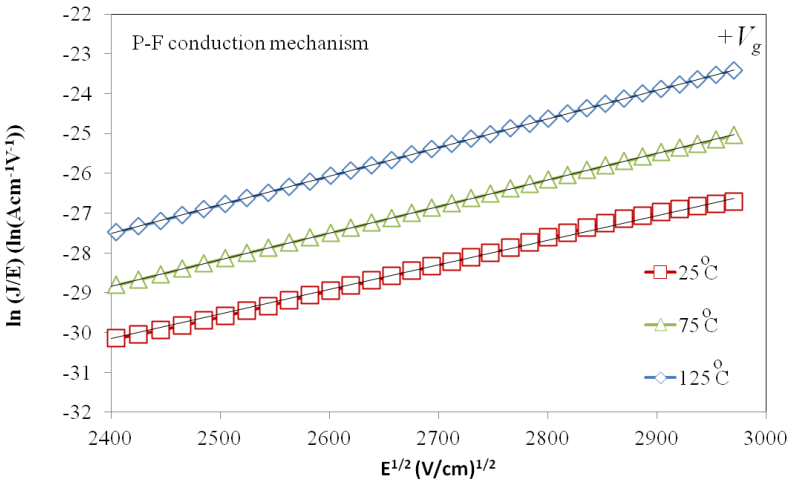


Figure 55. J-V curves of (a) control sample, and (b) nc-MoO_3 embedded ZrHfO sample at 25°C, 75°C, and 125°C, separately. V_g swept from -6 V to +6 V.

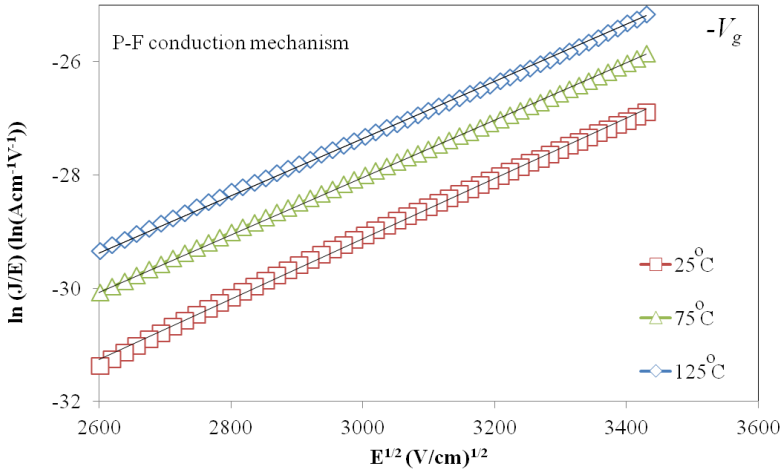
The strong temperature dependence of the leakage current of the nc-MoO_3 embedded sample indicates a possible Poole-Frenkel emission (P-F) or a Schottky emission (SE) conduction mechanism.[146,201] Previously, it was reported that the charge transported through the HfO_2 film following the P-F or the SE emission mechanisms.[202-203] However, in this nc-MoO_3 embedded ZrHfO film, the P-F emission mechanism, as shown in equation 28, appears to dominate the conduction mechanism.

$$J \quad E \quad \exp\left[\frac{-\left(\Phi_B - \sqrt{E/\pi\varepsilon_i}\right)}{kT}\right] \qquad [28]$$

where E is the electric field, q is the electron charge, Φ_B is the barrier height, ε_i is the insulator permittivity, k is the Boltzmann constant, and T is the temperature.[146] For example, Figure 56 (a) and (b) show that the P-F relationship fits the experimental data well in both the $+V_g$ and $-V_g$ ranges. The electron injection from the Si substrate under the $+V_g$ condition and the hole injection from Si substrate under the $-V_g$ condition are two dominant conduction processes. Since the electron- and hole-barrier heights at the Si/$HfSiO_x$ interface are much higher than the P-F trap energy, i.e., 1.2 eV and 3.8 eV vs. 0.59 eV, this is a further indication of a P-F conduction mechanism. In addition, intercepts to the y axis of the P-F fitting curves in Fig. 56 (b) decrease in magnitude while the temperature increases, i.e., -44.95 at 25^{o}C vs. -44.78 at 125^{o}C in the $+V_g$ range and -45.12 at 25^{o}C vs. -42.63 at 125^{o}C in the $-V_g$ range. This is consistent with the P-F relationship in Eq. 28, i.e., the intercept is inverse proportional to the temperature.[204] Figure 57 illustrates the schematic energy band diagrams of the nc-MoO_3 embedded sample at (a) $+V_g$ and (b) $-V_g$, separately. Electrons and holes were transferred by the P-F conduction mechanism under the $+V_g$ and $-V_g$ conditions, separately.



(a)



(b)

Figure 56. Fitting of P-F emission mechanism at 25°C, 75°C, and 125°C in the (a) $+V_g$ and (b) $-V_g$ ranges.

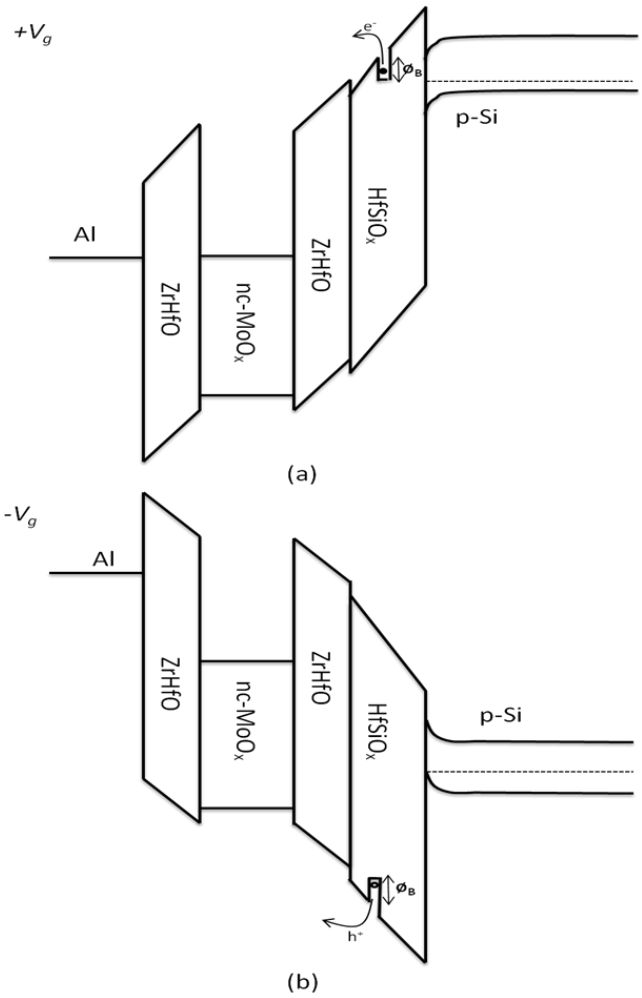


Figure 57. Energy band diagrams of the nc-MoO_3 embedded ZrHfO MOS capacitor under (a) $+V_g$ and (b) $-V_g$ conditions.

4.4.2 Temperature effect on charge trapping mechanism

Figure 58 shows the C-V hysteresis curves of (a) the control sample, and the nc-MoO_3 embedded ZrHfO sample at (b) 25^{o}C, (c) 75^{o}C, and (d) 125^{o}C, separately. All curves were measured at 1 MHz with V_g swept from -6 V to +6 V, i.e., forward, and then back to -6 V, i.e., backward. Fig. 58 curves are drawn in a small V_g range of -3 V to +1

V in order to better show the hysteresis phenomenon. For the control sample in Fig. 58 (a), the separation between the forward and backward curves are very small. The ΔV_{FB} between the backward and forward curves, i.e., $V_{FB,\ backward}$ - $V_{FB,\ forward}$, are almost independent of the temperature, e.g., 0.04 V at 25°C and 0.10 V at 125°C. Therefore, the ZrHfO film and its interface with Si trap negligible amount of charges. On the other hand, for the nc-MoO_3 embedded sample, the C-V hysteresis cannot be neglected. The C-V hysteresis of the nc-MoO_3 embedded sample under 25°C was mainly contributed by the negative V_g shift of the $V_{FB,\ forward}$, i.e., the holes were trapped in the nc-MoO_3 site. The initial negative charge was not considered to be responsible for the negative V_g shift of the $V_{FB,\ forward}$ since the device was annealed under the forming gas for 5 min prior to the measuring and it is well known that the H_2-annealing effect can passivate the initial negative charge.[205] In addition, it was reported that compared with the C-V curve of the fresh nc-MoO_3 embedded sample, i.e., without the -V_g stress, the C-V curve of the same sample after the -V_g stress was shifted to the negative V_g direction and the shift increase with the increase of the magnitude of the -V_g.[188] Table 3 summarizes parameters calculated from Fig. 58 (b)-(d), i.e., V_{FB}'s, charge trapping densities (Q_{ot}'s), and interface density of states (D_{it}'s) of the forward and backward C-V curves. The $V_{FB,\ fresh}$'s were determined from the fresh samples measured over a small V_g range, i.e., from -2.5 V to 1 V. In this small V_g range, the nc-MoO_3 embedded sample trapped negligible amount of charges. The $V_{FB,\ fresh}$ is independent of the temperature between 25°C and 125°C. However, when the V_g was swept from -6 V to +6 V, the $V_{FB,\ forward}$ shifted toward the negative V_g direction and the magnitude of shift increased with the increase

of temperature, e.g., from 25°C to 125°C. There are two possible explanations for the V_{FB} change. First, the high temperature makes it easier to form the hole-rich accumulation layer.[201] Second, the high temperature provides the accumulated holes with enough energy to overcome the barrier height at the Si/high-k interface.[201] Separately, the $V_{FB,\ backward}$ is little influenced by the temperature. Previously, it was observed that the nc-MoO_3 trapped negligible amount of electrons. Although the high temperature favors the formation of an electron-rich inversion layer and provided electrons with high energy, the nc-MoO_3 does not retain them. Therefore, the ΔV_{FB} increases with the increase of temperature, e.g., 0.16 V at 25°C to 0.81 V at 125°C. Table 3 also shows that the Q_{ot}'s increase with the increase of temperature. It is clear that the increase of Q_{ot} with temperature is due to the increase of the hole trapping capability. Separately, both $D_{it,\ forward}$ and $D_{it,\ backward}$ increase with the increase of temperature, which indicates the deterioration of the interface between Si and ZrHfO. In Fig. 55 (b), it was shown that the number of charges transferred across the high-k stack increased with the increase of temperature. The emission of the thermionic electrons at the high temperature could cause the damage to the interface.[206] Fig. 58 (d) shows an obvious shoulder between V_g = -0.8 V and -1.5 V at 125°C, which is absent from the control sample at the same temperature. This shoulder can be due to the existence of the near interface traps (NITs) located near the interface of the nc-MoO_3 and the surrounding ZrHfO.[189,207]

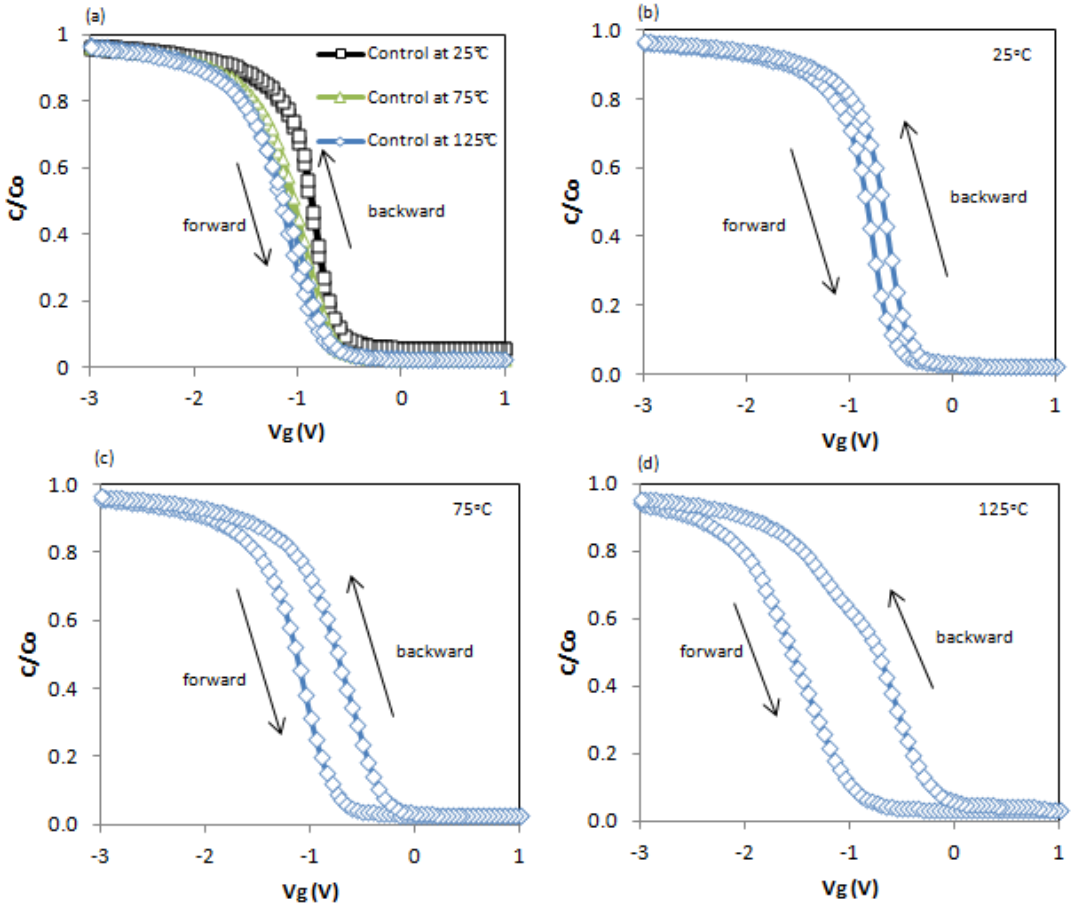


Figure 58. C-V hysteresis curves of (a) control sample at 25°C, 75°C, and 125°C, and nc-MoO_3 embedded ZrHfO sample at (b) 25°C, (c) 75°C, and (d) 125°C, separately.

Table 3. Parameters calculated from Fig. 58 (b)-(d).

Measurement Frequency: 1 MHz	25°C	75°C	125°C
$V_{FB,\ forward}$ (V)	−0.69	−0.97	−1.36
$V_{FB,\ backward}$ (V)	−0.53	−0.56	−0.56
$V_{FB,\ fresh}$ (V)	−0.46	−0.46	−0.47
Q (cm^{-2})	3.97×10^{11}	9.98×10^{11}	2.28×10^{12}
$D_{it,\ forward}$ ($cm^{-2}\ eV^{-1}$)	6.75×10^{11}	1.82×10^{12}	3.09×10^{12}
$D_{it,backward}$ ($cm^{-2}\ eV^{-1}$)	7.49×10^{11}	2.77×10^{12}	3.14×10^{12}

4.4.3 Temperature Effect on Charge Trapping Site

The trapped charges in the nc-MoO_3 embedded sample may be located within the bulk ZrHfO, at the Si/ZrHfO interface, within the nc-MoO_3, or at the nc-MoO_3/ZrHfO interface. In order to differentiate the charge trapping sites, the C-V curves were measured from V_g = -6 V to +6 V between 100 kHz and 1 MHz at 25^{o}C, 75^{o}C, and 125^{o}C. Figure 59 (a) shows the C-V curves of the control sample measured at different frequencies but the same 25^{o}C. They do not disperse with the frequency. The same result is observed at 75^{o}C and 125^{o}C of which the curves are not shown here. Therefore, neither the bulk ZrHfO nor the Si/ZrHfO interface responds to the measurement frequency in this temperature range. However, Figure 59 (b) shows that at 25^{o}C for the nc-MoO_3 embedded sample, the C-V curve is stretched and shifted to the positive V_g direction, i.e., from V_{FB} = -1.11 V to -1.02 V when the measurement frequency is decreased from 1 MHz to 100 kHz. The C-V stretch is due to the slow response of the holes trapped in shallow traps to the frequency, i.e., at the nc-MoO_3/ZrHfO interface.[183] The response of the interface trapped charge are more obvious with the increase of temperature, as shown in Figure 59 (c) and (d). At 125^{o}C, a hump is observed on the 100 kHz curve near the V_{FB}. Since more holes can be trapped at the starting V_g of -6 V, at the high temperature, the amount of holes trapped in shallow traps increases accordingly. They could tunnel back to the Si substrate when the band structure returned to the flat band condition. This is consistent with the data in Table 3 that $V_{FB,\ forward}$ shifts to the negative V_g direction when the temperature is increased from 25^{o}C to 125^{o}C.

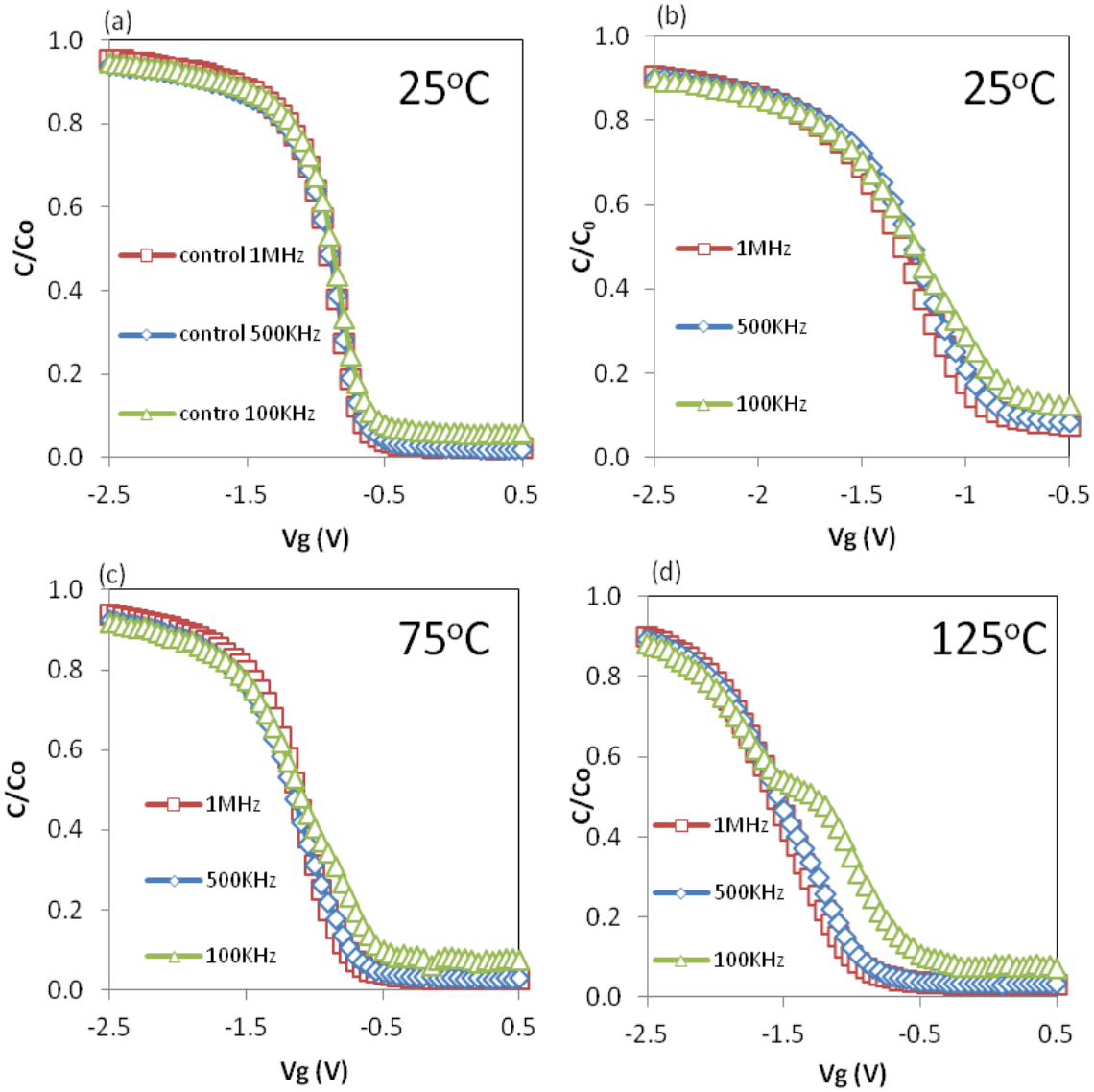


Figure 59. C-V curves of (a) control at 25°C, and nc-MoO_3 embedded ZrHfO sample at (b) 25°C, (c) 75°C, and (d) 125°C, separately, measured in the forward sweep direction at 1 MHz, 500 kHz, and 100 kHz.

Figure 60 shows the G-V curves of the (a) control (b) nc-MoO_3 embedded samples measured at 1 MHz with the V_g swept from -6 V to +6 V at 25°C, 75°C, and 125°C, separately. At the flat band condition, both the density of the majority carriers and their capture rate are low, which causes the energy loss.[185] Therefore, a conductance peak around the V_{FB} is observed. For both the control and the nc-MoO_3 embedded samples, the magnitude of the conductance peak increases with the increase of temperature. This is consistent with the ref. 186 which reports that the high temperature causes more energy loss. Previously, it was discussed that for the control sample, the charge trapping density is small and very slightly influenced by the change of temperature. However, for the nc-MoO_3 embedded sample, the charge trapping density is large and increases with the temperature. It takes longer time for the embedded nc-MoO_3 layer to capture and to emit them at the high temperature. Therefore, the high energy loss occurs on the nc-MoO_3 embedded sample at the high temperature. For the control sample, the magnitude of the peak in the G-V curve is one to two orders of magnitude smaller than that in the nc-MoO_3 embedded sample, i.e., 3×10^{-6} S vs. 2×10^{-5} S at 125°C. Because the hole trapping density of the former at V_g = -6 V is much smaller than that of the latter. In addition, for the control sample, the location of the G-V peak does not change with the temperature while for the nc-MoO_3 embedded sample, the peak shifted to the negative V_g direction with the increase of temperature. This is consistent with the previous result that at V_g = -6 V, the amount of holes trapped to the nc-MoO_3 site increased with the increase of temperature, which is absent for the control sample.

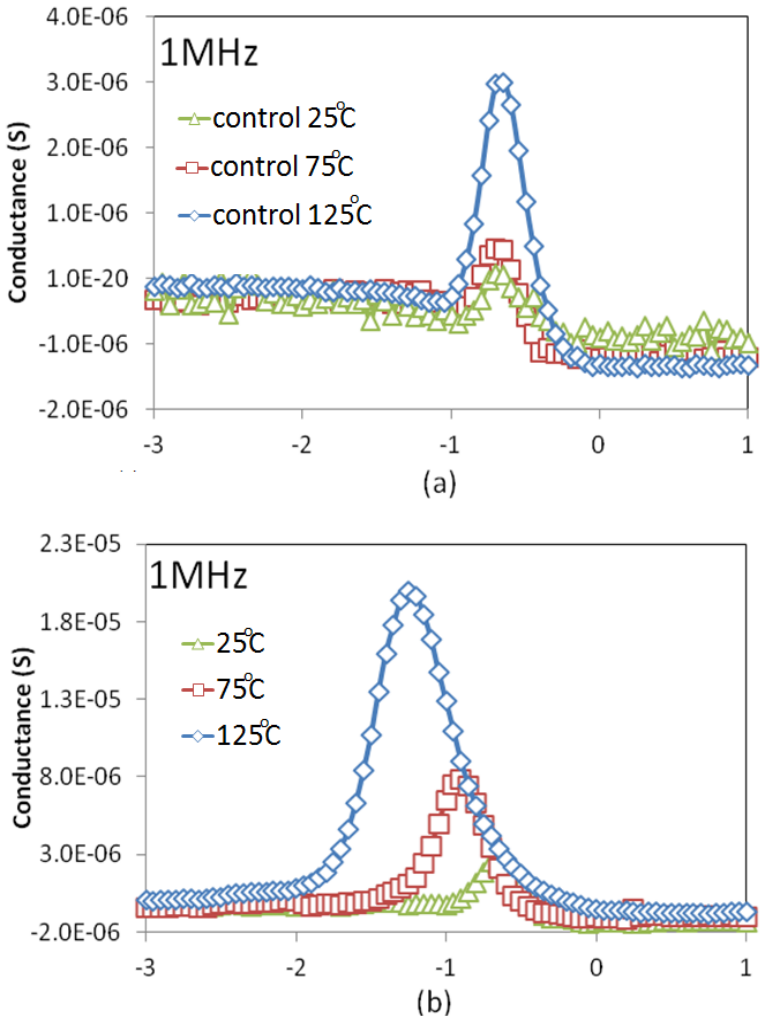


Figure 60. G-V curves of (a) control, and (b) nc-MoO_3 embedded ZrHfO sample at 1MHz at 25°C, 75°C, and 125°C, separately, measured in the forward sweep direction.

4.4.4 Temperature Effect on Charge Retention Characteristics

The temperature effect on the charge retention efficiency of the nc-MoO_3 embedded capacitor was investigated by stressing it with a V_g for a period of 1,800 s and then the charge trapping density was immediately measured. The procedure was

repeatedly until 10 hours.[199-200] Previously, it was reported that in the nc-ITO and nc-MoO_3 embedded ZrHfO samples, the holes trapped in shallow traps were located at the nanocrystal/ZrHfO interface site and the deeply trapped holes were within the bulk nanocrystal.[164,188] Figure 61 shows the percentage of remaining trapped charges vs. the time after releasing the stress V_g of -8 V for 10 s at 25°C, 75°C and 125°C, separately, on a x-log scale. The total measuring time was 10 hours and the data was recorded every 1,800 s. The remaining trapped charges were linearly extrapolated from 10 hours to 10 years. At 25°C, 43% of the originally trapped charges remained in the nc-MoO_3 embedded capacitor after 10 years. However, at the high temperatures, the trapped charges were lost quickly, e.g., all charges were lost after 772 days at 75°C and after 330 days at 125°C. The inset figure shows the original 10 hours measuring on a x-linear scale in order to show the detail. In the first 1,800 s, a portion of the holes trapped in shallow traps were quickly lost. After the first 1,800 s, the loss rate became small because the remaining holes were deeply trapped.[188] In the first 1,800 s, the charge loss percentages were 28%, 33%, and 58% at 25°C, 75°C, and 125°C, respectively. After 10 hours, the charge loss percentages were 38%, 52%, and 80% at 25°C, 75°C, and 125°C, respectively. Therefore, the temperature effect is applicable to charges trapped both in shallow and deep traps. There are two possible reasons for the higher charge loss rate at the high temperature. First, holes trapped at the high temperature have the higher thermal energy than those trapped at the low temperature. Second, the dielectric conductance of the ZrHfO film increases with the increase of temperature. Both factors could cause the quick release of a large portion of the trapped charges.[201]

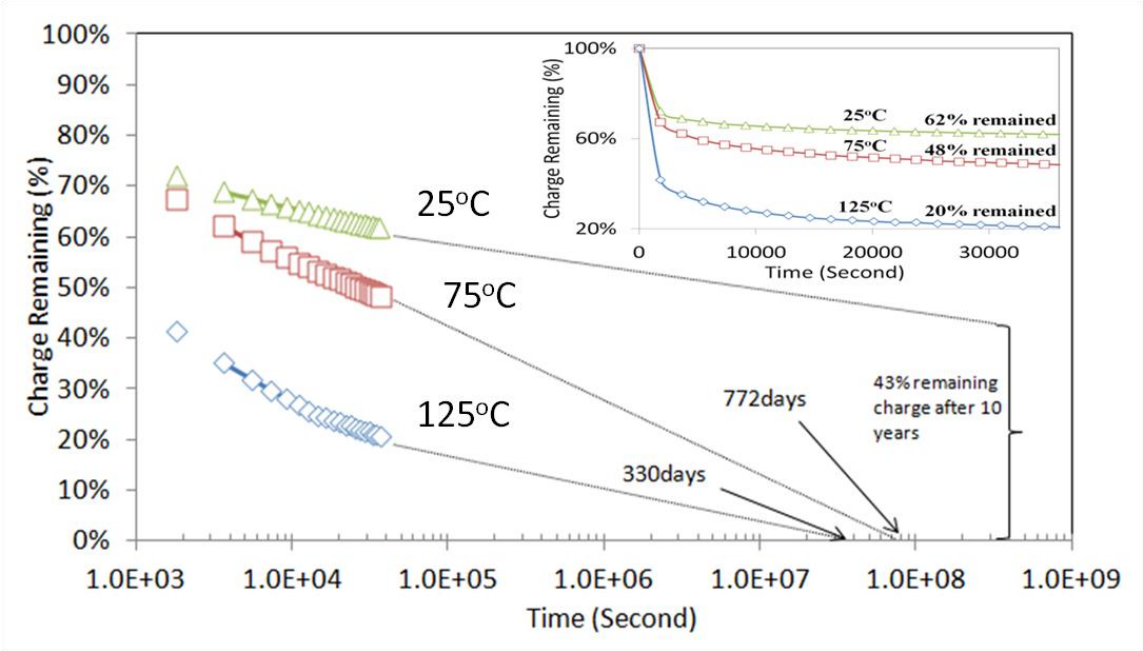


Figure 61. Charge retention characteristic of nc-MoO_3 embedded ZrHfO sample at different temperatures with the extrapolation to 10 years. The inset shows the original 10 hours data with the time expressed in the linear scale.

4.5 Summary

Temperature effects on the charge transfer mechanism and the storage capacity of the nc-MoO_3 embedded high-k dielectric capacitor have been investigated. The high temperature suppressed the Coulomb blockade effect and caused the higher leakage current due to the larger thermal energy of the trapped holes and the higher conductivity of the high-k film. The magnitude of V_g for the J to change its polarity decreased with the increase of temperature, which was contributed by the increase of the hole trapping density. The P-F emission mechanism dominates the conduction mechanism because the charge trapping energy is lower than the barrier heights at the Si/$HfSiO_x$ and Al/ZrHfO

interfaces. The amount of trapped electrons was little influenced by the temperature because of the preference of hole trapping of the nc-MoO_3 site. The deterioration of the Si/ZrHfO interface at the high temperature was caused by the high charge transfer rate. With the increase of temperature, the magnitude of the conductance peak in the G-V curve increased and the location shifted to the negative V_g direction because of the change of the energy loss rate of the trapped holes. About 43% of the trapped charges were retained after 10 years at 25^{o}C. However, the charge retention capability decreased with the increase of temperature. In summary, memory functions and the lifetime of the nc-MoO_3 embedded ZrHfO capacitor are dependent on the temperature because of the change of the hole trapping and detrapping mechanisms.

CHAPTER V

WHITE LIGHT EMISSION FROM ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K DIELECTRIC FILM WITH AND WITHOUT AN EMBEDDED NANOCRYSTAL LAYER*

5.1 Introduction and Motivation

The solid-state light emitting device (LED) has been used to replace the incandescent and fluorescent bulbs for the lighting purpose since it can significantly reduce the energy consumption. LEDs are typically made from semiconductors and alloys, e.g., GaSb, GaAs, GaAsP, InP, SiGe, AlGaP, InGaN, SiC, or ZnO, epitaxially grown on top of the single crystal wafers, e.g., Si, SiC, sapphire, or GaN.[208]

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* Part of data reported in this chapter is reproduced from "A light emitting device made from thin zirconium-doped hafnium oxide high-k dielectric film with or without an embedded nanocrystal layer", by u e Kuo and Chi-Chou Lin accepted for publication in the Applied Physics Letters, 102, 031117 (2013), by permission of AIP-American Institute of Physics.

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Conventionally, the semiconductor material is doped into the p-n junction structure. When it is forward biased, electrons and holes flow into the junction where they combine and release photons of a specific energy, i.e., equivalent to the band energy of the semiconductor layer. LEDs can also be made of the quantum well (QW) structure, e.g., an active region made of one or more very thin GaN-based epitaxy layers sandwiched between thicker layers of GaN. Depending on the composition, thickness, and material of the clad layer, lights of different wavelengths, e.g., from deep UV to IR, can be emitted.[209] The fabrication of the above two types of LEDs requires an expensive molecular beam epitaxy equipment or the highly toxic metal organic vapor deposition (MOCVD) process. The number of defects in the structure is a major yield concern. Also, it is difficult to emit the white light from a single LED. The white-light LED is needed for the general lighting and many other applications. It has to be generated by mixing red, green, and blue solid-state LEDs with different bandgap energies or using an UV/blue LED in combination with a yellow phosphor material, e.g., YAG:Ce.[78,88] The former requires the different operating voltages to adjust the color balance, which increases the cost.[89] The latter involves the rare-earth material and the unavoidable Stokes energy loss during the conversion of the wavelength.[78] In addition, the semiconductor nanocrystals have been used for the color conversion in the white-light LED because the semiconductor nanocrystals are known for the narrow band emission and high quantum yield.[210] For example, the CdSe/ZnS core-shell nanocrystals in combination of the blue InGaN/GaN LED has been proposed to generate the white light.[211,212] The white-light has also been generated from a monolayer composed of the blue (CdZnS alloy), green

(ZnSe/CdSe/ZnS core/shell/shell), and red (CdSe/ZnS core/shell) nanocrystals in a hybrid organic/inorganic structures.[99] However, it is difficult to maintain the particle size of each type of the nanocrystals and the emission color can be dramatically changed.[96] Another disadvantage for the nanocrystals-based LED is the self-absorption due to the small Stokes shift. The emitted energy is absorbed by either the nanocrystals themselves or the neighboring nanocrystals, which reduces the overall quantum efficiency.[210] Therefore, a convenient single-chip white-light LED is eagerly anticipated. It has been mentioned in the section 1.3.3 that the light emission from the dielectric thin film, e.g., 60 nm to 200 nm thick SiO_2 or Al_2O_3, impinged with an electron beam of 50 keV was observed. If the electron beam in the above study is replaced by charges injected from contacts adjacent to the dielectric film, the similar light emission phenomenon can be expected. Moreover, if the dielectric layer is thin, the required energy is low. Metal oxide high-k dielectrics are good materials for this purpose because their electron and hole offsets to Si are smaller than those of SiO_2. The ZrHfO high-k has been proved as the good gate dielectric for MOS devices as shown in Chapter III and IV. In this study, the possibility of the light emission was investigated from an ultra thin ZrHfO high-k dielectric film sandwiched between the Si wafer and a gate electrode stressed with an electric field. Moreover, the CdSe nanocrystals (nc-CdSe) were embedded into the ZrHfO gate dielectric layer for the possibility of enhancing the light emission intensity and improving other light characters such as the CRI value. More details regarding the nc-CdSe embedded SSI-LED will be addressed in section 5.4.

5.2 Experimental

The SSI-LED has a MOS capacitor structure with a thin ZrHfO gate dielectric layer on the dilute HF solution cleaned p-type (10^{15} cm^{-3}) Si (100) wafer. The ZrHfO film was sputter deposited from the Zr/Hf (12:88 wt%) target under the Ar/O_2 (1:1) atmosphere at 5 mTorr and 60 W for 2, 6, and 12 min (name 2-min, 6-min, and 12-min SSI-LED from now on). After deposition, the sample was treated with a PDA step at 800^oC for 3 min under the N_2 atmosphere. Then, a 80 nm thick ITO film was sputter deposited on top of the ZrHfO film and wet etched into gate electrodes. The backside of the wafer was deposited with an Al layer to form the ohmic contact. The complete sample was annealed at 400°C for 5 min under the H_2/N_2 (1:9) atmosphere. For the nanocrystal embedded sample, i.e., nc-CdSe embedded ZrHfO sample (name nc-CdSe SSI-LED from now on), the fabrication process is as same as that in Chapter III. The 12-min SSI-LED can also be used as the control sample for the nc-CdSe SSI-LED. Figure 62 shows the HRTEM figures of (a) 6-min and (b) 2-min SSI-LED. The 12-min SSI-LED and the nc-CdSe SSI-LED were as same as the control and nc-CdSe embedded samples in Chapter III and their HRTEM figures were shown in Fig. 43. A $HfSiO_x$ interface layer was formed between the ZrHfO film and the Si wafer in all three samples. The physical thickness of the bulk ZrHfO layer and the EOT are shown in Table 4. Both of them increase with the increase of the deposition time. The increase of the EOT is due to the decrease of the oxide capacitance caused by the larger physical thickness in the long deposition time condition. The capacitor's J-V and C-V curves were measured by the same method as discussed in Chapter III and IV. The D_{it} is

extracted from the C-V curve by using the Lehovec's method.[213] For the light emission experiment, the ITO electrode was stressed with a V_g and the emitted light was measured with an optical emission spectrometer (OES, StellarNet BLK-C-SR-TEC). The color coordinates of the light were calculated using the color matching functions of the 1931 CIE standard observer.[148] The CCT was defined as the color temperature on the Planckian locus nearest to the color coordinates point on the CIE 1960 diagram which was transformed from the CIE 1931 diagram.[150] Then, the distance between the color coordinates point on the CIE 1960 diagram and the Planckian locus, i.e., chromaticity distance, is used to calculate the CRI values.[151]

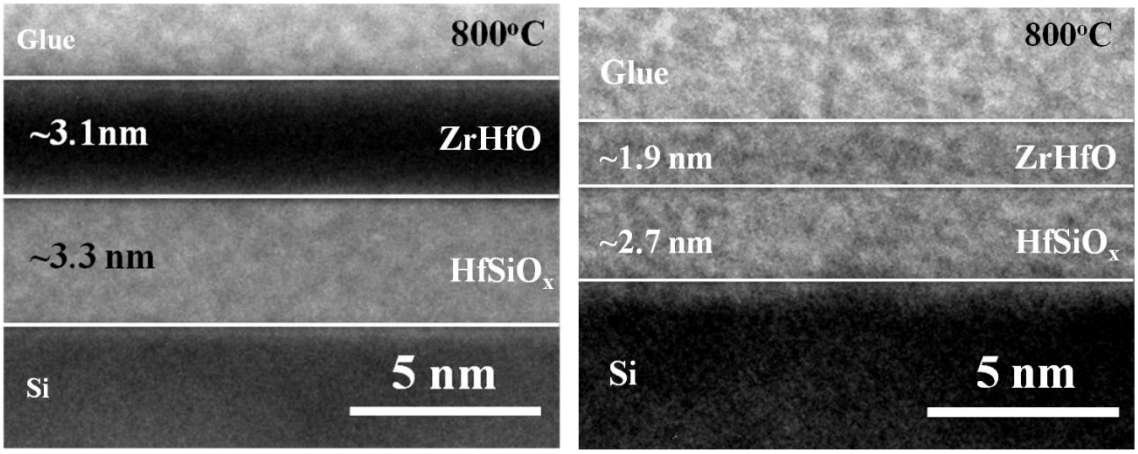


Figure 62. HRTEM figures for the 6-min and 2-min SSI-LED.

Table 4. Physical thickness and EOT of 2-min, 6-min, and 12-min SSI-LED.

	Physical thickness of the bulk ZrHfO	**EOT**
2-min SSI-LED	**1.9 nm**	**4.76 nm**
6-min SSI-LED	**3.1 nm**	**6.15 nm**
12-min SSI-LED	**3.8 nm**	**6.76 nm**

5.3 Electrical and Optical Properties of ZrHfO High-K Gate Dielectric Stack with Different Physical Thicknesses

Figure 63 (a) shows a low-magnification photo of light emission from a 300 μm diameter dot of the 6-min SSI-LED at V_g = -20 V. The dark region on the left side is the shadow of the probe needle. The light is emitted uniformly from the ITO electrode. However, the high-magnification photos, e.g., Fig. 63 (b), (c), and (d) for 2-min, 6-min, and 12-min SSI-LEDs, respectively, show that light is emitted from discrete small bright dots. For the p-n junction or QW LED, light is emitted uniformly from the electrode, i.e., not from discrete small bright dots. It is possible that the principle of light generation of the Fig. 63 devices is different from that of the conventional band-gap energy based LED. The light emission process of this new device is closely related to the polarity and magnitude of the applied V_g ($|V_g|$). In the positive V_g range, e.g., up to +50 V, the leakage current was very small and no light emission was observed from all three samples. This is because the number of electrons tunneled through the high-k stack are limited from the inversion layer of the p-type Si substrate. In the negative V_g range, the

J-V curve contains a breakdown voltage (V_{BD}), as shown in Figure 64, where the leakage current jumped abruptly. Light emission was observed when the $|V_g|$ is larger than the magnitude of the V_{BD} ($|V_{BD}|$). The J increases with the decrease of the physical thickness under the same $|V_g|$. This phenomenon can be contributed by the higher electric field of the thinner sample. At the same time, the $|V_{BD}|$ increases with the increase of the physical thickness of the high-k stack, e.g., -5.6 V, -9.7 V, and -11.8 V for the 2-min, 6-min, and 12-min SSI-LEDs, respectively. This is due to the lower leakage current of the thicker sample. Below the $|V_{BD}|$, the leakage current is very low and the conduction mechanism follows the Schottky emission (SE) and Poole-Frankel (P-F) mechanism.[159] Above the $|V_{BD}|$, the film is broken and the conductive paths are formed. Subsequently, the leakage current increases linearly with the increase of the $|V_g|$, i.e., following the Ohm's law. Therefore, the bright small dots in Fig. 63 (b), (c), and (d) are composed of conductive paths formed through the high-k stack after the dielectric breakdown. Since these dots only occupy a small portion of the gate electrode area, the current density in each of the conductive path is much larger than that of the corresponding J in Fig. 64. This is an indication that light is generated from thermal excitation of the conductive path, e.g., similar to the case of the incandescent light bulb.

Fig. 63 also shows that the dot brightness increases with the decrease of the physical thickness of the high-k stack. As discussed previously, the thinner film is prone to earlier breakdown than the thicker film due to the larger electric field. Therefore, the former is more favorable for the formation of the conductive path. In addition, the C-V hysteresis curves of three samples swept from -6 V to +6 V and then back to -6 V, were measured and the results are shown in a smaller V_g range, i.e., -3 V to +3 V to -3 V, in Figure 65 for a better exhibition. The D_{it} can be extracted from the C-V curves and the thinner sample has larger D_{it} than the thicker sample has, i.e., 1.60×10^{12} $cm^{-2}eV^{-1}$, 4.69×10^{11} $cm^{-2}eV^{-1}$,and 3.07×10^{11} $cm^{-2}eV^{-1}$, for the 2-min, 6-min, and 12-min SSI-LEDs, respectively. Moreover, the oxide trapped charges Q_{ot}, which is mainly related to the defect density in the bulk oxide layers,[214] also increased with the decrease of the deposition time, i.e., 2.83×10^{12} cm^{-2}, 1.53×10^{12} cm^{-2}, and 1.14×10^{11} cm^{-2} for the 2-min, 6-min, and 12-min SSI-LEDs, respectively. The thin high-k stack with the large interface and bulk defect densities favors the large leakage current.[215] Therefore, it is more prone to form conductive paths in the thin sample than the thick sample, which favors the light emission process.

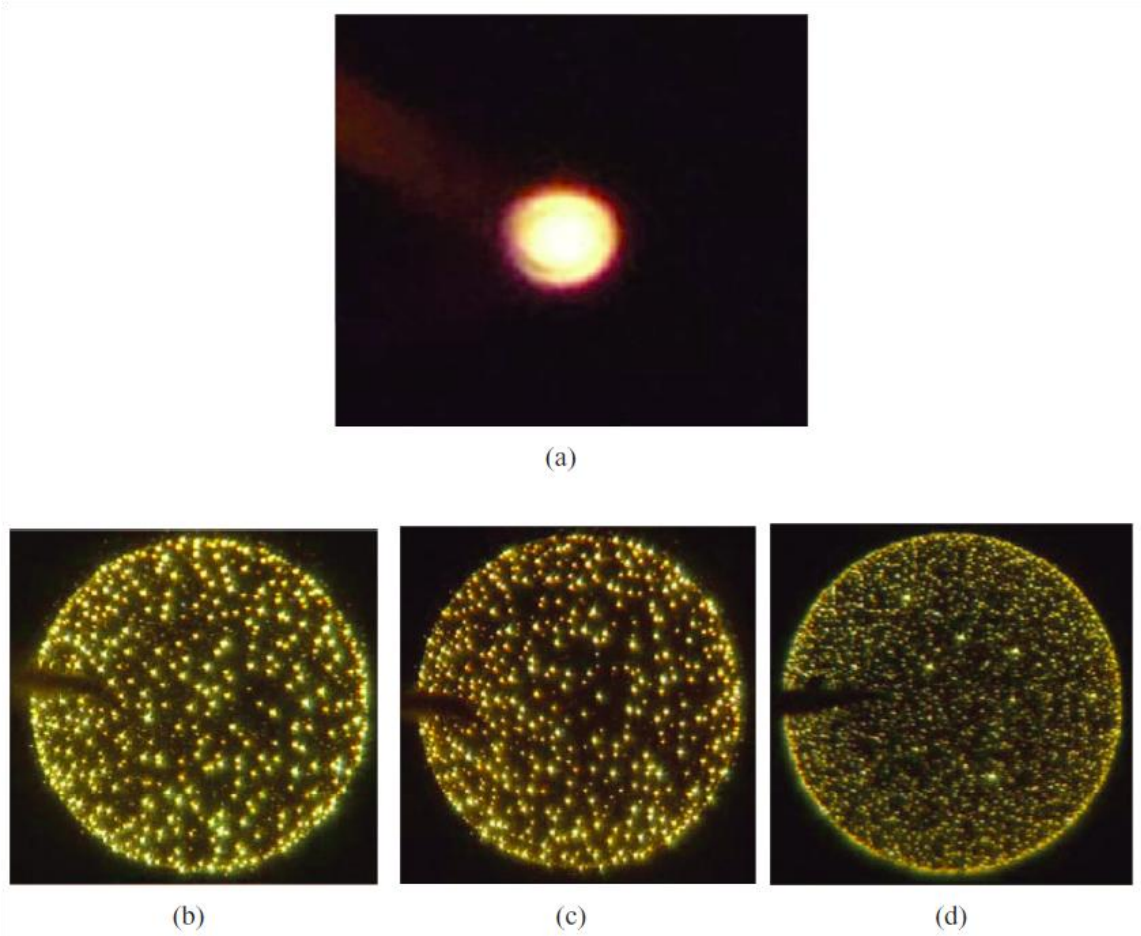


Figure 63. (a) A low resolution photo of the 6-min deposited sample, and high resolution photos (100X taken through an optical microscope) of (b) 2-min, (b) 6-min, and (d) 12-min SSI-LEDs. All samples: 300 μm diameter and at V_g = -20 V.

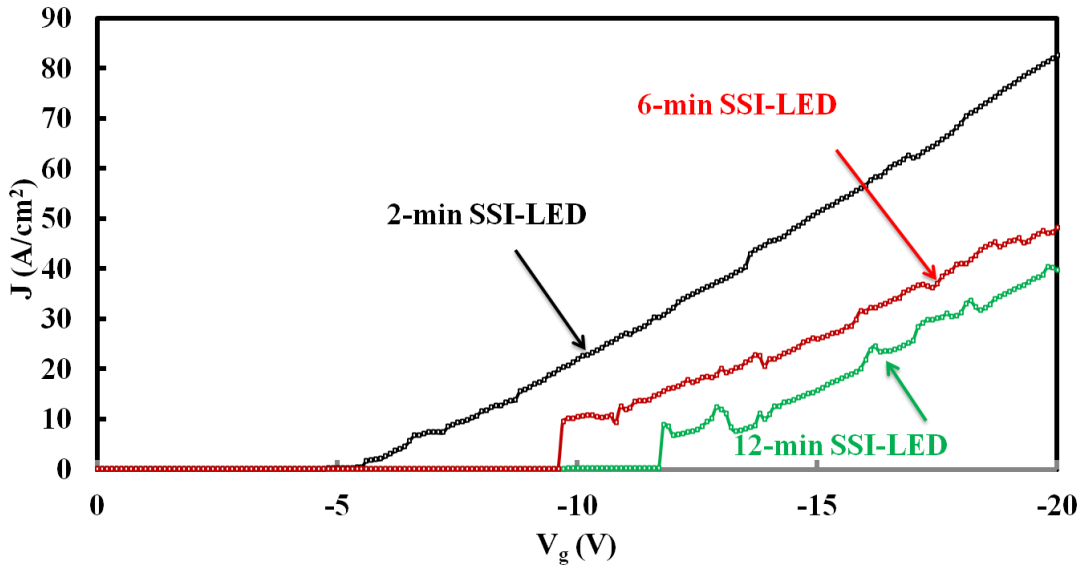


Figure 64. Current density vs. stress V_g of 2-min, 6-min, and 12-min SSI-LEDs. All samples: 300 μm diameter.

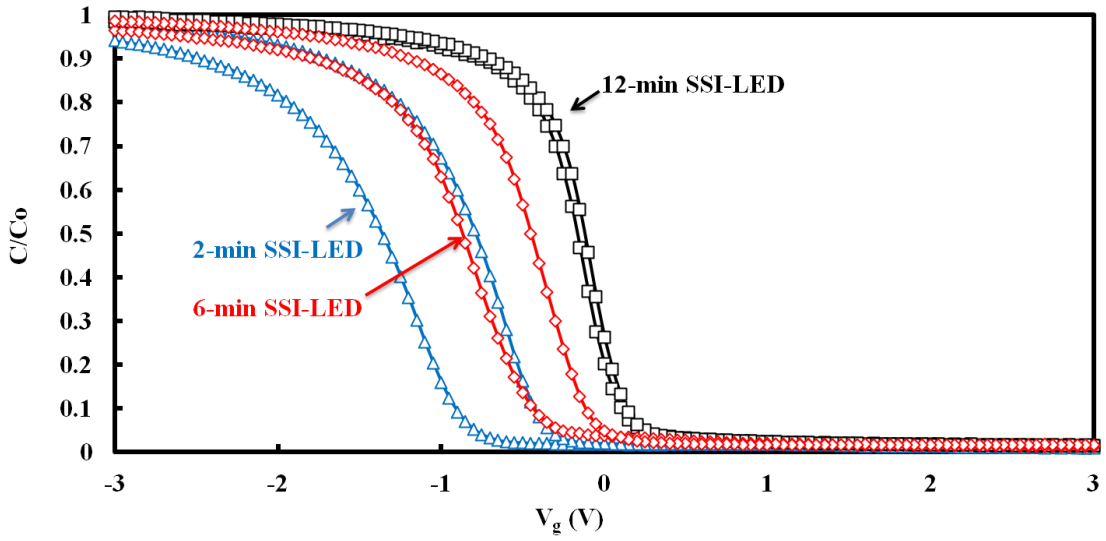


Figure 65. C-V hysteresis curves of 2-min, 6-min, and 12-min SSI-LEDs.

Figure 66 shows the emission spectra of samples with different ZrHfO deposition times stressed with the same V_g of -20 V. All samples emit similar broad band light from near UV to infrared wavelength. The intensity increases with the decrease of the ZrHfO stack thickness, i.e., the increase of the electric field strength. The larger electric field enhances the leakage current passing through the high-k stack and induces more heat to the conductive path. Therefore, stronger light emission intensity is observed. The change of the light intensity in Fig. 66 is consistent with the results in Fig. 63. Separately, the broad emission spectrum of Fig. 66 is different from the narrow emission spectrum of the conventional p-n junction or QW LED.[83,216] For this device, light is emitted from many individual dots across the electrode area, as shown in Fig. 63 (b), (c), and (d). However, for the conventional LED, light is emitted uniformly across the electrode. In addition, since there is no QD embedded in the amorphous ZrHfO stack in this new device, light cannot be emitted from the quantum confinement phenomenon. It is highly possible that the principle of light emission of this new device is different from that of the bandgap energy based LED. Based on Figs. 64 and 66 results, i.e., the broad spectrum light emitted from many small spots in the linear J-V region, the principle of light generation of this new device is similar to that of the incandescent lamp, i.e. thermal excitation of the conductive path. However, different from the conventional incandescent lamp that contains the conductive filament with the fixed cross-sectional area and length, conductive paths of this new device are formed in the dielectric breakdown process. The emission of visible light from the capacitor made of CdSe/ZnS core shell QD sandwiched between organic hole- and electron charge transfer layers is

due to quantum confinement in QDs and defects in the film.[217] However, no dielectric film was included in the above device structure. In another case, the bimodal light including the visible wavelength region was emitted from the nc-Si embedded SiN_x or SiO_2/Si_3N_4 stack.[154,218] This kind of device was operated at the low leakage current density range, i.e., before the dielectric breakdown. It was concluded that one peak in the spectrum was contributed by the electron-hole radial recombination in the nc-Si and the other peak was contributed by the defective Si bond.[154,218] On the other hand, Fig. 66 samples contain very thin amorphous ZrHfO high-k stacks without the embedded nanocrystals and light is only emitted while the leakage current is very large. Therefore, the principle of light emission of this new device is different from that of the QD embedded device. Separately, the shape of the curve in Fig. 66 is similar to that of the solar spectrum in the visible wavelength region except the λ_{peak} locations, i.e., 695.5 nm for the former and 475-504 nm for the latter.[219] Therefore, this is a single-chip, white-light solid state incandescent LED (SSI-LED).

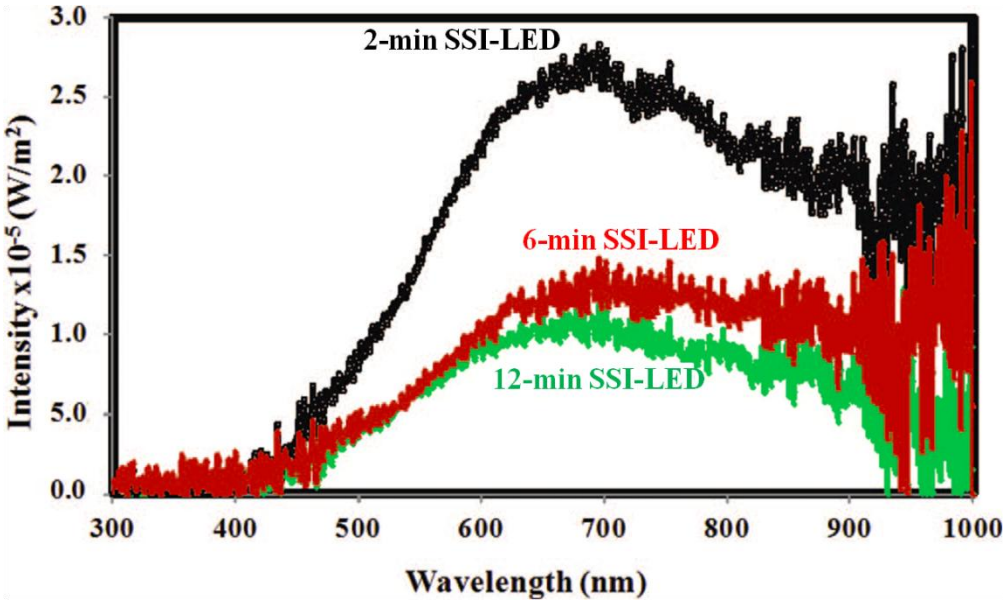


Figure 66. Emission spectra of 2-min, 6-min, and 12-min SSI-LEDs. All samples: 300 μm diameter and at V_g = -20 V.

The emitted light from these three samples stressed at V_g = -30 V were characterized for the chromaticity coordinates in the CIE 1931 chart, CCT, and CRI R_a values. The details are shown in Table 5. The CIE color coordinates for three SSI-LEDs with different ZrHfO thicknesses are very close to each other and the CCT increases with the increase of the ZrHfO physical thickness. The CRIs for all three samples are much higher than that in the commercial YAG:Ce white LED, i.e., 79, due to the broad band light emission of the former. In addition, all lights emitted from these new SSI-LEDs with different deposition times are located in the warm white light region of the CIE chart as shown in Figure 67. The tungsten incandescent light bulb and the YAG:Ce white LED are also marked in the same figure for comparison.[220,221] All lights emitted

from the SSI-LEDs are close to that of the incandescent light bulb. They are probably based on the similar light emission principle, i.e., thermal excitation of the conductive path.

The EQE quantifies the efficiency of converting the electrical energy into the emitted optical energy. The accurate value is usually obtained by measuring with an integrated sphere setup. A simple method of dividing the number of emitted photons per unit time with the total number of electrons injected to the device was used to make a rough estimation of the EQE of the new SSI-LEDs. The EQE increased as the increase of the physical thickness of the high-k stack while the device is stressed at -20 V, e.g., 0.025%, 0.042%, and 0.115% for 2-min, 6-min, and 12-min SSI-LEDs, respectively. This phenomenon can be contributed by the higher leakage current of the thinner sample. Higher leakage current increases the number of electrons passing through the device per unit time. If the light emission intensity does not increase linearly with the increase of the leakage current, the EQE drops accordingly.

Table 5. Color coordinates on CIE 1931 chart, CCT, and CRI R_a values for the 2-min, 6-min, and 12-min SSI-LEDs.

ZrHfO Deposition time	CIE x	CIE y	CCT [K]	CRI R_a
2 min	**0.466**	**0.418**	**2,666**	**95**
6 min	**0.460**	**0.414**	**2,725**	**97**
12 min	**0.461**	**0.429**	**2,821**	**94**

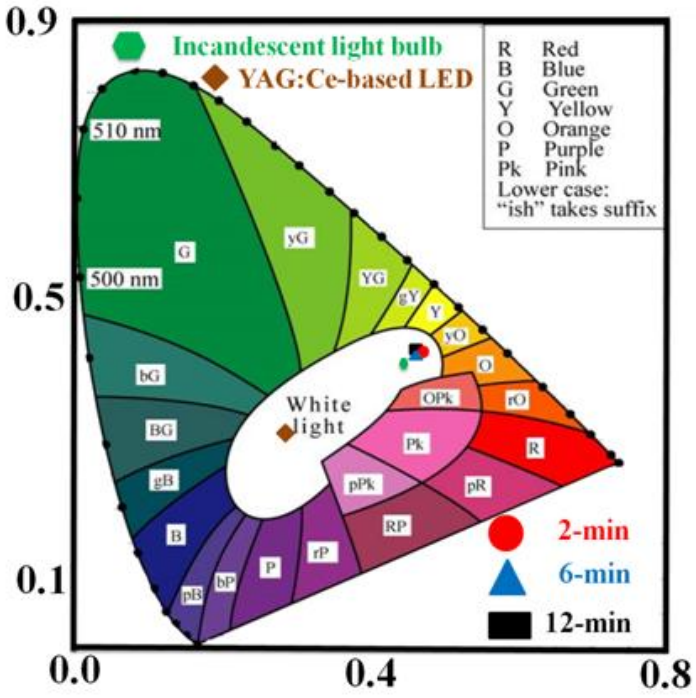


Figure 67. Location of the 2-min, 6-min, and 12-min SSI-LEDs on the CIE 1931 chart.

The lifetime of this new SSI-LED has been investigated. The light emission phenomenon, e.g., the small bright dots formation, and the J-V curves, e.g., the dielectric breakdown process, were repeatable. The device could be turned on and off for many times without deteriorating the light emission characteristics. In addition, the 12-min SSI-LED was stressed at V_g = -20 V in the atmosphere for 1,000 hours continuously with the current density and emission spectrum monitored every 10-20 hours. No obvious change of these characteristics was detected. The long lifetime of the device is contributed by the unique structure of surrounding the conductive paths with the high quality ZrHfO dielectric, which avoids the air contact.

5.4 White Light Emission Characteristics of ZrHfO High-K Gate Dielectric Stack with and without nc-CdSe Layer

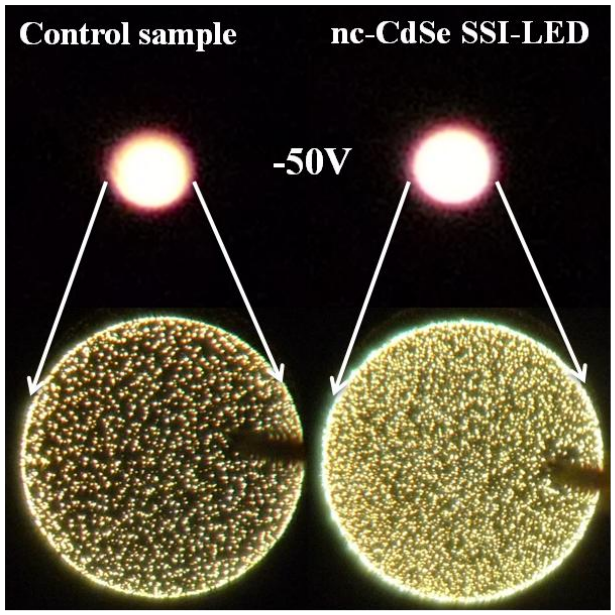
5.4.1 Motivation

In section 5.3, the single-chip, long lifetime, white light emission SSI-LEDs have been demonstrated. The light emission intensity increased with the decrease of the physical thickness of the ZrHfO stack due to the increase of the electric field and leakage current passing through the conductive path. Therefore, the enhancement of the current passing through the device is favorable for the formation of the conductive path and the intensity of the light emission. However, the EQE drops with the decrease of the physical thickness of the ZrHfO stack since the light emission intensity does not increase linearly with the increase of the leakage current. There exists a need to improve the EQE in this new SSI-LED. Recall the J-V curves results of the nc-CdSe embedded sample and its control sample in Figure 52, the leakage current of the former is larger than that of the latter because of the higher defect density from the stress mismatch between the nanocrystals and ZrHfO film. Instead of increasing the light emission intensity by shrinking the physical thickness of the ZrHfO stack, the nanocrystals embedded ZrHfO film can be a good light emission layer in the new SSI-LED. In this study, authors investigated the optical, electrical, and material characteristics of the nc-CdSe embedded ZrHfO sample.

5.4.2 Electrical and Optical Properties of ZrHfO High-K Gate Dielectric Stack with and without nc-CdSe Layer

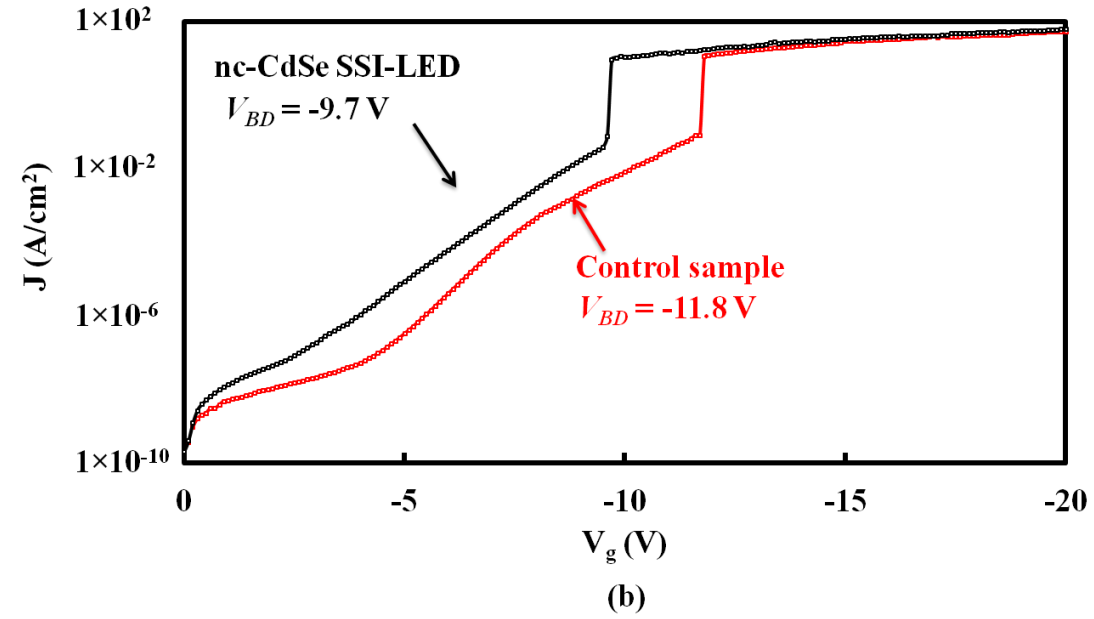
Figure 68 (a) shows the low- and high-magnification photos of the control (12-min SSI-LED) and nc-CdSe SSI-LED stressed at V_g = -50 V. The light emission pattern is composed of many small discrete bright dots, which is different from that of the conventional p-n junction or QW LEDs. As mentioned in section 5.3, this unique light pattern is from the thermal excitation of many tiny conductive paths formed from the dielectric breakdown process. Both the light intensity and the number of the bright dots in Fig. 68 (a) increase with the inclusion of the nc-CdSe layer in the ZrHfO film, which will be discussed later. Figure 68 (b) shows the J-V curves in the log scale of the same samples as Fig. 68 (a) from V_g = 0 V to -20 V. An obvious current jump can be observed at the V_{BD}'s of -11.8 V and -9.7 V for the control sample and nc-CdSe SSI-LED, respectively. The larger $|V_{BD}|$ of the former compared to that of the latter is due to the former's smaller J as shown in Fig. 68 (b). Defects were generated in the nc-CdSe SSI-LED because of the large stress mismatch between the CdSe nanodots and the bulk ZrHfO film, which causes the larger leakage current and favors the formation of conductive paths in the dielectric layer during the dielectric breakdown process. When the $|V_g|$ is smaller than the $|V_{BD}|$, the J-V curves for both samples in Fig. 68 (b) can be well fitted by the SE and P-F conduction mechanisms, which is consistent with the results in section 5.3.[146] The carriers transferred through the high-k stack by the SE mechanism at the low electric field (Ɛ) condition and -F mechanism at the high Ɛ regime as shown in Figure 68 (c) and (d), respectively. This is consistent as the literature

report that the SE mechanism occurs at the low Ɛ while the -F mechanism requires a high Ɛ.[222-223] When the $|V_g|$ is further increased to be higher than the $|V_{BD}|$, the small conductive paths are formed and function like resistors that are thermally excited to emit light upon the passing of the high current. This thermal excitation light emission principle is similar as the conventional incandescent light bulbs.[224]



(a)

Figure 68. (a) Low and high-magnification photos under -50V stress condition, (b) the J-V curve swept from 0V to -20V, and (c) the SE and (d) P-F fitting curves of the control sample and nc-CdSe SSI-LED.



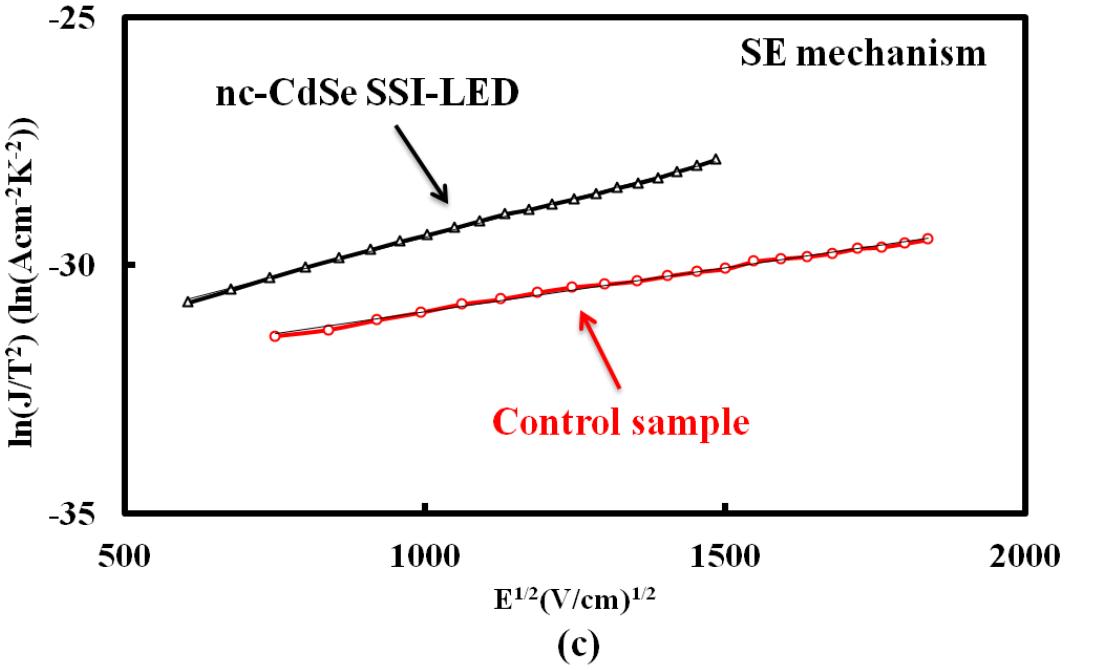


Figure 68 continued.

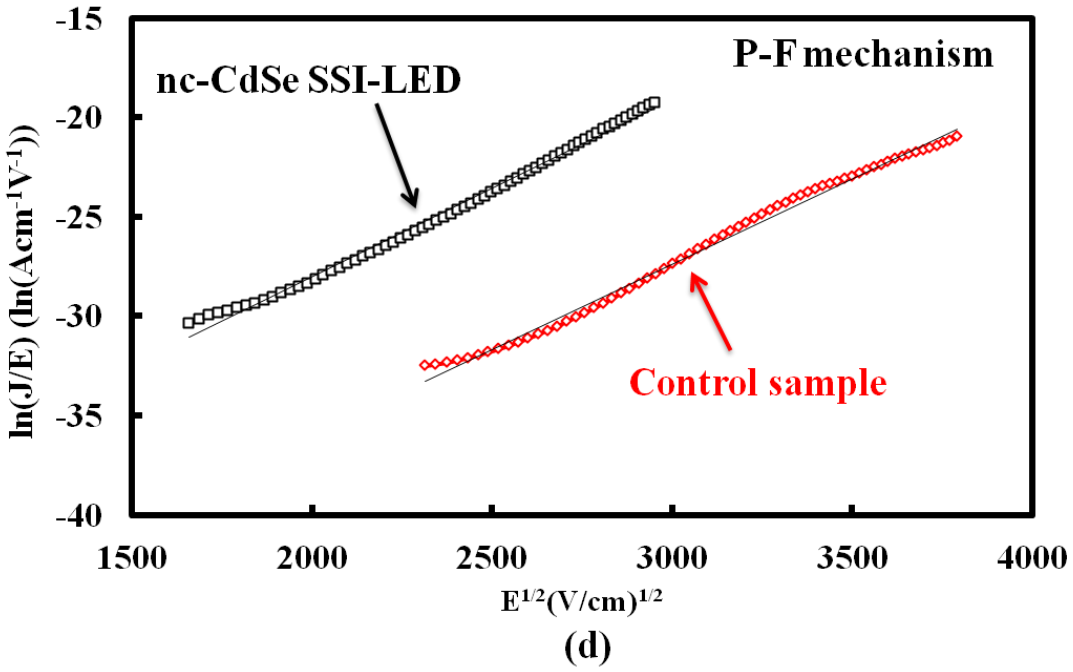


Figure 68 continued.

Figure 69 (a) shows the emission spectra of the control sample and nc-CdSe SSI-LED at V_g = -50V. Both samples emit the same broad band spectrum including the near UV to near IR wavelengths. The normalized emission spectra are overlapped, as shown in the inset, which represents that the inclusion of the nc-CdSe layer does not affect the light emitting principle. However, the light intensity increases with the inclusion of the nc-CdSe layer. This phenomenon is consistent with the results of Fig. 68 (a) and can be explained by the larger leakage current passing through the nc-CdSe SSI-LED compared to the control sample under the same V_g. The former's larger leakage current corresponds to the higher temperature or larger number of the conductive paths or both. Lights emitted from these two samples were investigated for their chromaticity coordinates in

the 1931 CIE chart, CCT, and CRI R_a. Both lights are in the warm white light region of the CIE chart as shown in Figure 69 (b) and is very close to the conventional incandescent light bulb of (0.447, 0.407). This is an indication of the similar light emission principle, i.e., thermal excitation. Other light characters are shown in the Table 6. The CCT increases with the inclusion of the nc-CdSe layer, i.e., 3,089 K vs. 3,141 K for the control sample and nc-CdSe SSI-LED, respectively. If the thermally excited light emission from these two samples follow the black body radiation as same as the incandescent light bulb, the CCTs can be taken as the actual temperatures of the conductive path.[225] Therefore, the higher CCT of the nc-CdSe SSI-LED confirms that the larger leakage current causes more thermal excitation of the path, which explains the higher intensity of each dot in the Fig. 68 (a)'s light pattern. Moreover, the large CRI R_a's of 97.9 and 98.4 for the control sample and nc-CdSe SSI-LED are much larger than the commercial YAG:Ce-based white LED, i.e., 79 and close to the black body emission of the conventional incandescent light bulb, i.e., 100.[79]

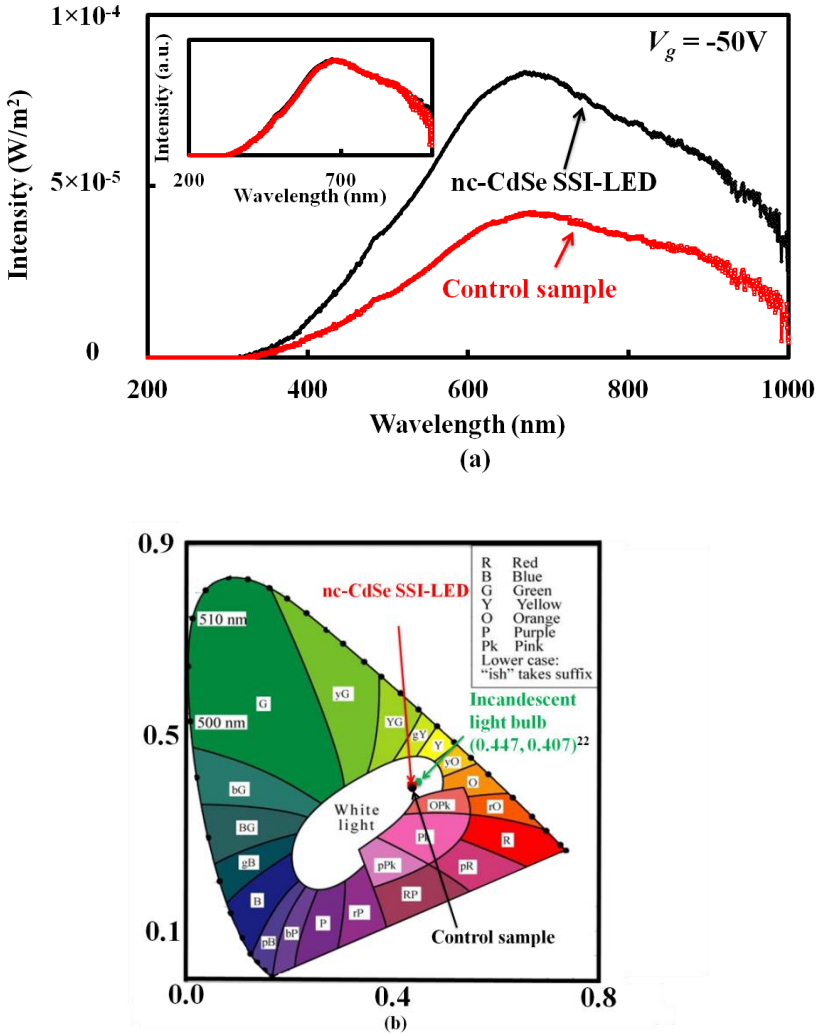


Figure 69. (a) Emission spectra of the control sample and nc-CdSe SSI-LED under -50V stress condition. (b) CIE color coordinates of the same samples as (a) and incandescent light bulb. Inset of (a) shows the normalized emission spectra.

Table 6. The CIE color coordinates, CCT, and CRI of the control sample and nc-CdSe SSI-LED at V_g = -50 V.

Sample	V_g	CIE x	CIE y	CCT [K]	R_a
Control sample	-50V	0.430	0.400	3,089	97.9
nc-CdSe SSI-LED	-50V	0.430	0.405	3,141	98.4

Figure 70 (a) shows the high-magnification photos of the control sample and nc-CdSe SSI-LED stressed at V_g = -10V, -30V, and -50V, respectively. With the increase of the $|V_g|$, the brightness and the number of the bright dots increase in both samples. Figure 70 (b) and (c) show the light emission spectra of the control sample and nc-CdSe SSI-LED, respectively, under different stress voltages from -10V to -50V with the increment of 10V. The light emission spectrum of -10V in the control sample was not able to be detected due to the limit resolution of the optical emission spectrometer. The light intensity increases with the increase of the $|V_g|$ for both samples, which is consistent with the result in Fig. 70 (a). This phenomenon can be explained by the thermal excitation mechanism. First, under the high $|V_g|$, a large current passes through the conductive path. The larger current causes more thermal excitation of the path, which induces higher intensity of the emitted light. Second, the higher $|V_g|$ increases the number of the emitted dots, which enhances the light intensity. On the other hand, the spectrum peak location (λ_{peak}) shifts toward the shorter wavelength direction (blue shift) with the increase of the $|V_g|$, i.e., from 695.5 nm at -20 V to 681.5 nm at -50 V and from

695.5 nm at -20 V to 676.5 nm at -50 V for control sample and nc-CdSe SSI-LED, respectively. The same blue shift has been observed in the incandescent light bulb when the bulb is operated under the high driving power condition.[226-227] This is an another indication of the same light emitting principle. Table 7 summarizes changes of both samples' CIE color coordinates, CCT, and the CRI values with the V_g. The CIE color coordinate numbers decrease and the CCT increases with the increase of the $|V_g|$ for both samples. The former matches the blue shift of the λ_{peak} in Fig. 70 (b) and (c) and the latter confirms that more heat was transferred to the conductive paths under the high $|V_g|$ condition. In addition, the R_a increases with the increase of the $|V_g|$ in both samples, which is contributed by the reduction of the chromaticity distance to the Planckian locus under high $|V_g|$. Therefore, both the light intensity and quality improve with the increase of the applied $|V_g|$ for the samples with or without the nc-CdSe layer.

The EQE increased with the inclusion of the nc-CdSe layer while the device is stressed at -20V, e.g., 0.160% and 0.115% for nc-CdSe SSI-LED and control sample, respectively. This phenomenon can be contributed by the much higher, i.e., ~2 times, light emission intensity with only ~1.4 times leakage current of the nc-CdSe SSI-LED compared to the control sample.

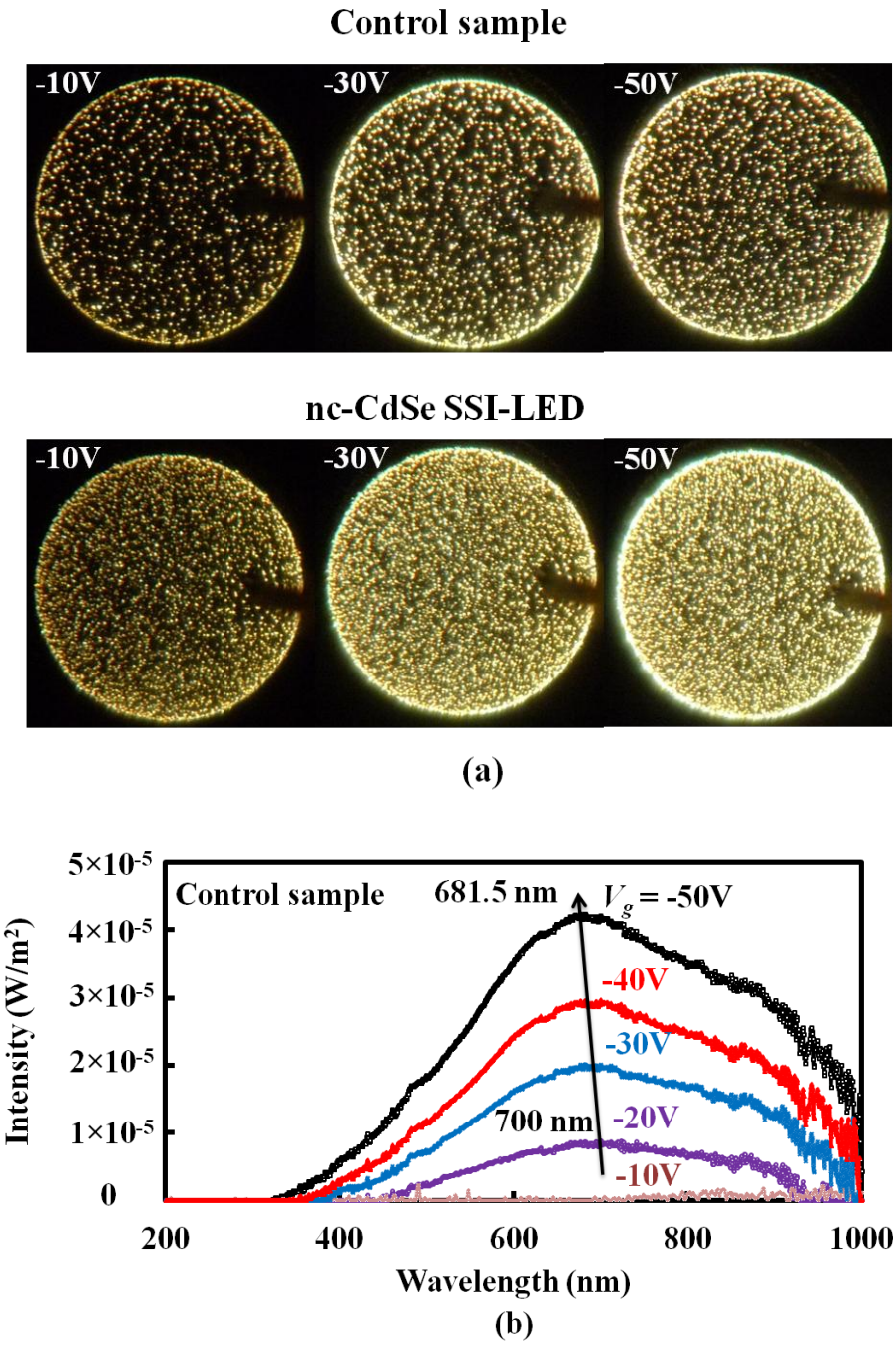


Figure 70. (a) Low- and high-magnification photos of control sample and nc-CdSe SSI-LED under -10V, -30V, and -50V stress conditions. Emission spectra under -10V to -50V stress conditions of (b) control sample and (c) nc-CdSe SSI-LED.

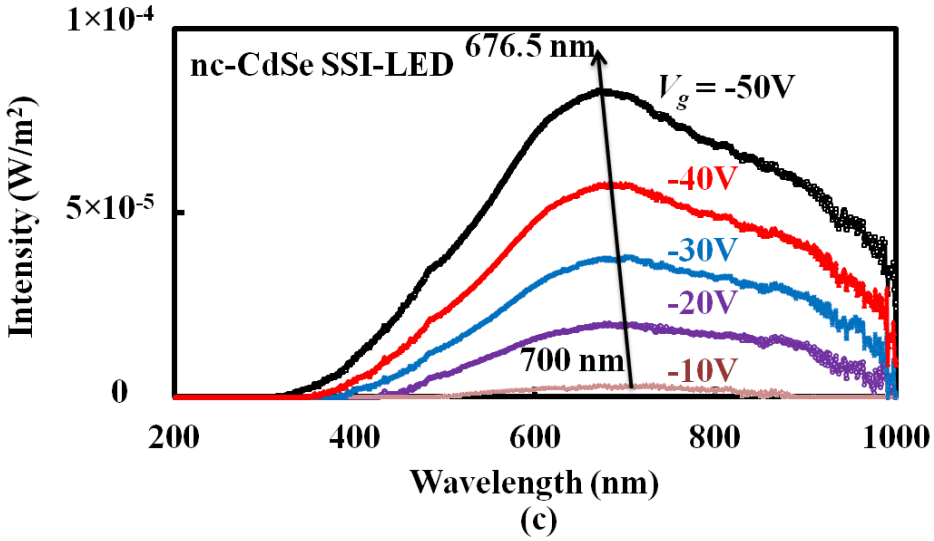


Figure 70 continued.

Table 7. The CIE color coordinates, CCT, and CRI of the control sample and nc-CdSe SSI-LED under different stress voltages.

Sample	V_g	CIE x	CIE y	CCT [K]	R_a
Control sample	-50V	0.430	0.400	3,089	97.9
	-40V	0.441	0.407	2,958	97.9
	-30V	0.451	0.417	2,893	96.7
	-20V	0.490	0.453	2,650	87.8
nc-CdSe SSI-LED	-50V	0.430	0.405	3,141	98.4
	-40V	0.432	0.406	3,107	97.9
	-30V	0.453	0.417	2,860	96.9
	-20V	0.486	0.447	2,657	90.9

Since the pulsed driving condition can lower down the power consumption and extend the lifetime of the LED,[228] the light emission characters of both samples driven

under different duty cycles (DCs) and frequencies were investigated. Figure 71 (a) and (b) show the light emission spectra for the control sample and nc-CdSe SSI-LED driven under different DCs but the same frequency and V_g, i.e., 1 kHz and -40 V, respectively. The spectrum range, shape, and λ_{peak} are all independent with the DC for both samples. Therefore, the change of DC does not change the light emission principle. The CIE color coordinates slightly move away from the Planckian locus and therefore, the CRI decreases with the drop of the DC. The light emission intensity decreases linearly with the drop of the DC, e.g., the λ_{peak} heights of the 75% and 50% DCs are ~3 and ~2 times that at the 25% DC for both samples. At the same time, the lower operation DC induces smaller CCT. These phenomena are due to the lower power consumption of the devices while the DC is reduced. Detailed light characters under different DCs were shown in Table 8. Moreover, the same samples were driven under different frequencies but same DC of 75% and same V_g of -40 V, as shown in Figure 71 (c). The light emission intensity, CIE color coordinates, CCT, and CRI have negligible change over a large range of the frequencies, i.e., 1 Hz to 100 kHz, for both samples. The stable light characters can be contributed by the fast response of the thermal excitation process since the ultra short conductive paths, i.e., 7.1 nm for the control sample and 10.9 nm for the nc-CdSe SSI-LED, are easily excited.

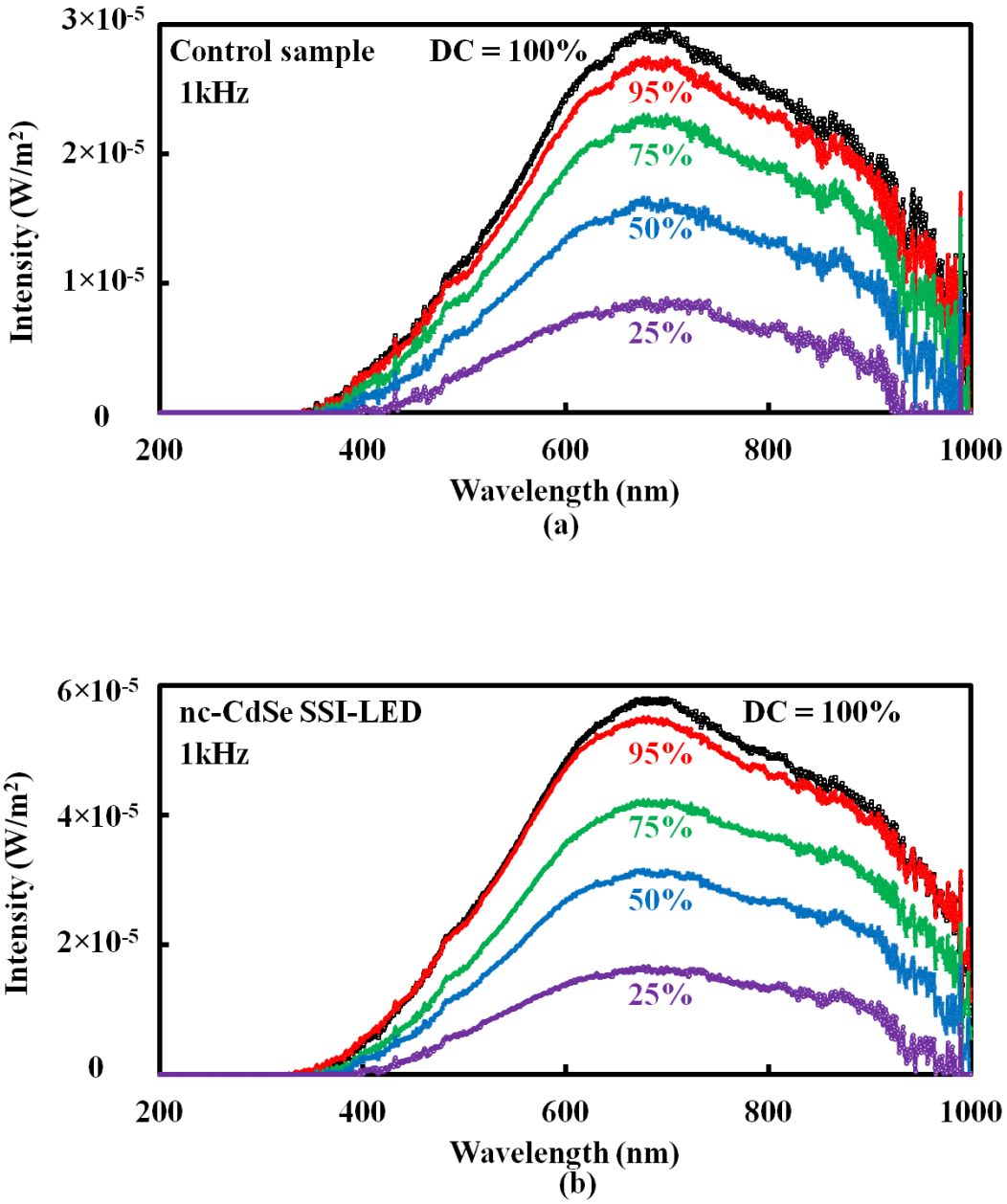


Figure 71. Emission spectra of the (a) control sample and (b) nc-CdSe SSI-LED under different duty cycles (c) Emission intensity of both samples stressed at Vg = -40 V and DC = 75% but different frequencies.

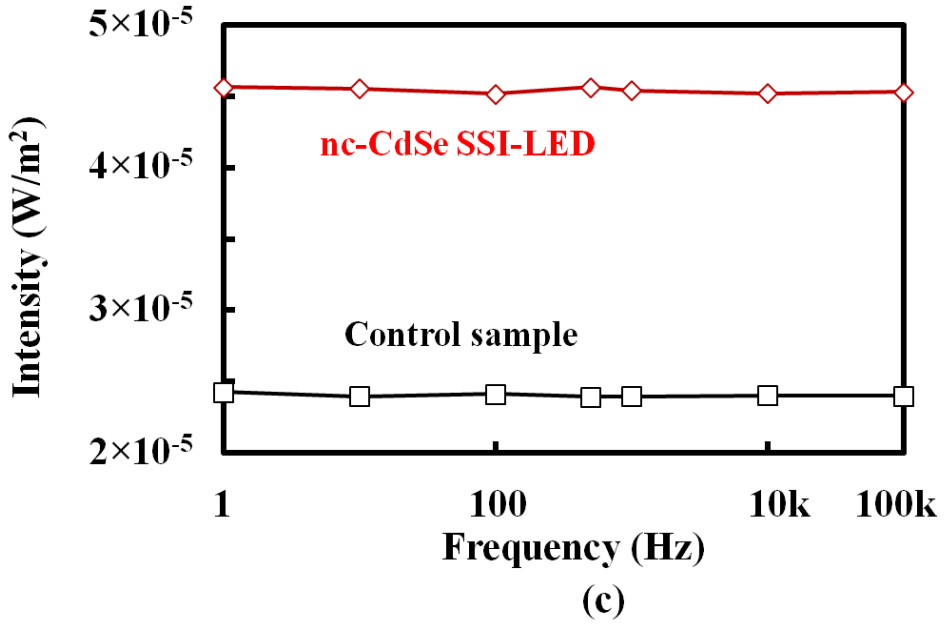


Figure 71 continued.

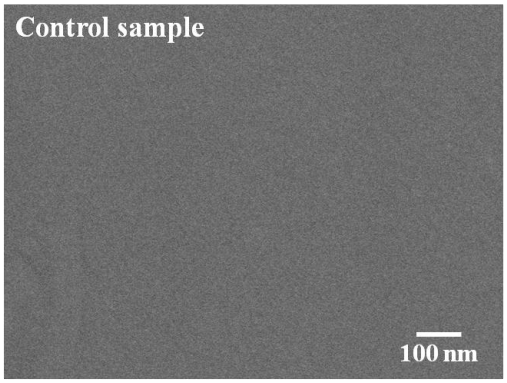
Table 8. The light intensity, CIE color coordinates, CCT, and CRI of the control sample and nc-CdSe SSI-LED at V_g = -40 V and different DCs.

Sample	V_g	DC	Intensity [W/m^2]	CIE x	CIE y	CCT [K]	R_a
Control sample	-40V	100%	2.9×10^{-5}	0.441	0.407	2,958	97.9
		95%	2.7×10^{-5}	0.442	0.409	2,958	97.9
		75%	2.3×10^{-5}	0.447	0.416	2,956	97.6
		50%	1.7×10^{-5}	0.451	0.417	2,893	96.4
		25%	8.8×10^{-6}	0.463	0.436	2,874	92.3
nc-CdSe SSI-LED	-40V	100%	5.8×10^{-5}	0.432	0.406	3,107	97.9
		95%	5.5×10^{-5}	0.437	0.407	3,025	97.4
		75%	4.2×10^{-5}	0.440	0.410	3,006	96.6
		50%	3.2×10^{-5}	0.443	0.413	2,996	96.2
		25%	1.7×10^{-5}	0.454	0.428	2,949	93.8

The extremely short conductive path is not only beneficial to the pulsed operation under wide range of the frequency, but also favorable to the efficiency of the LED. It was reported that the radiation intensity η of the conventional incandescent light is inversely proportional to the radius r and the length L of the filament.[225] Assuming that the new LED is operated under the same input power as that in the incandescent light bulb, e.g., 10 W, the light emission efficiency of the conductive path of 150 nm radius × ~10 nm length should be 1.3×10^{11} times that of the tungsten filament of 100 μm radius × 2 m length. Although the EQE is low at this stage, the ultra small conductive path indicates the possible high efficiency of this new LEDs.

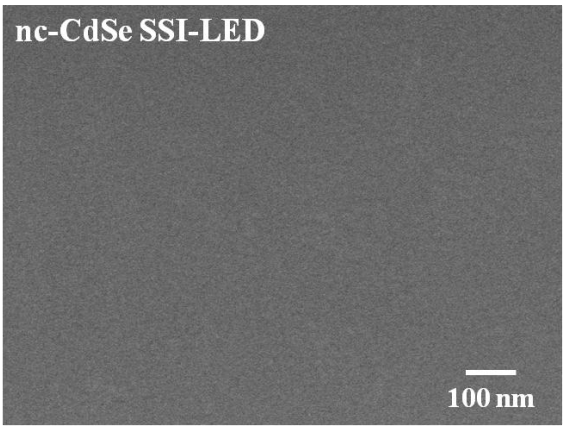
The thermally excited light emission may cause the surface change. The serious surface change may affect the lifetime of the LED. Therefore, it is essential to investigate the surface change for this new device after the light emission. Figure 72 shows the SEM micrographs of the (a) control sample, (b) nc-CdSe SSI-LED before stress, (c) control sample, and (d) nc-CdSe SSI-LED after -20 V, 20 min stress in low-magnification and 35^{o}-tilted high-magnification conditions. The SEM micrographs were all taken after the wet etching of the ITO electrode by the aqua regia solution. The high-k surface is smooth for both samples before the stress. After stress, the high-k surface becomes rough with the formation of bumps and holes as shown in Fig. 72 (c) and (d). These bumps and holes are not from the wet etching process because they are absent in Fig. 72 (a) and (b). The bump locations are consistent with the locations of the discrete bright dots in Fig. 68's microscope figures. Therefore, it is possible that the bumps were formed due to the high leakage current passing through the conductive path during the

light emission process. The holes were possibly formed from the melt of the bumps due to the local high temperature. In addition, the micrographs of the nc-CdSe SSI-LED shown in Fig. 72 (d) has the larger density of bumps and holes compared to that in the control sample shown in Fig. 72 (c). This result confirms that the higher light emission intensity of the nc-CdSe SSI-LED is not only contributed by the higher intensity of each dot but also larger number of the conductive path. Moreover, the 35^{o}-tilted high-magnification micrographs show that the bump grows higher from the nc-CdSe SSI-LED than the control sample does. The larger density and height of the bumps in the nc-CdSe SSI-LED can be explained by the higher leakage current passing through the device under the same V_g compared to the control sample, which is consistent with the J-V curves in Fig. 68 (b).

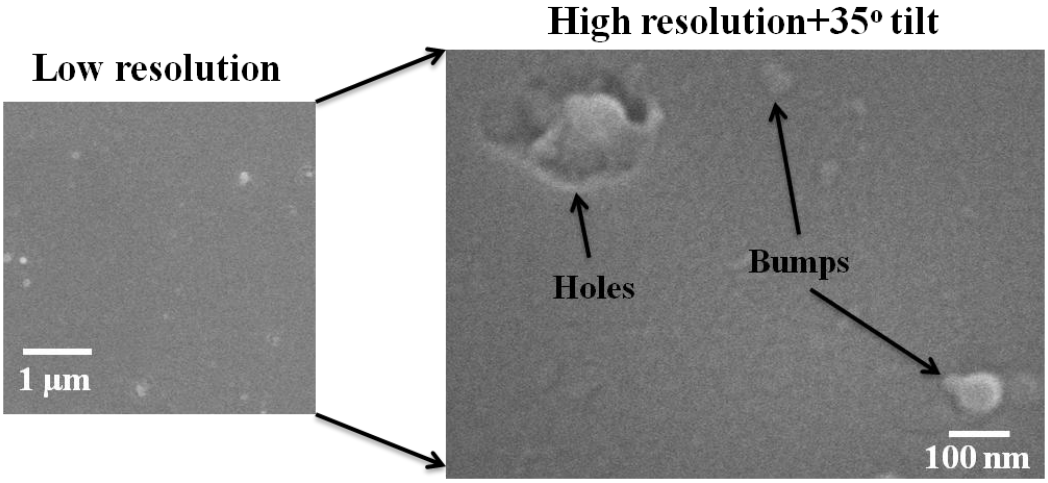


(a)

Figure 72. SEM micrographs of the (a) control sample, (b) nc-CdSe SSI-LED before stress, (c) control, and (d) nc-CdSe embedded sample after -20V, 20min stress in low-magnification and 35^{o}-tilted high-magnification conditions.



(b)



(c)

Figure 72 continued.

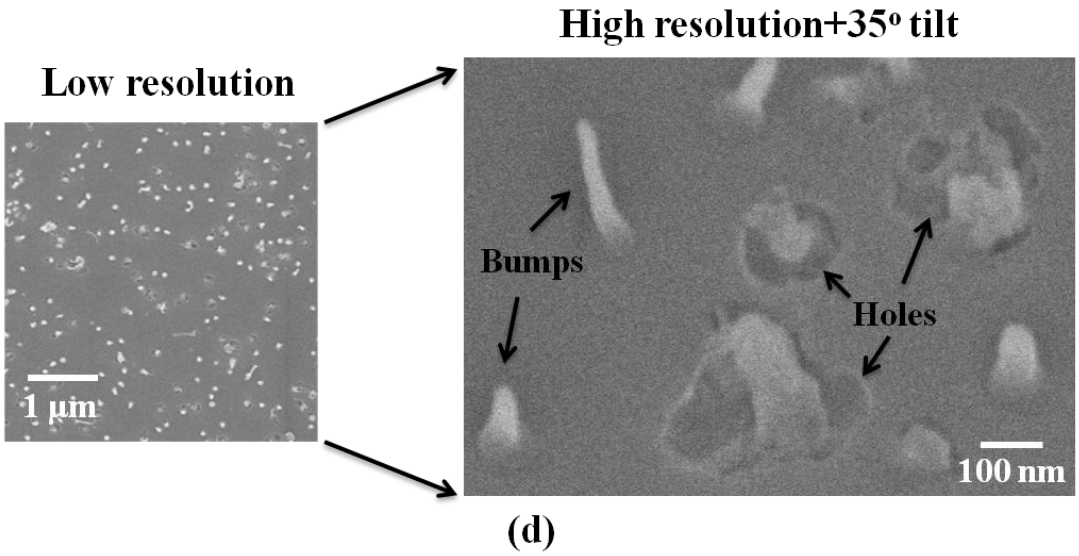


Figure 72 continued.

The lifetime of the LED is important to the practical application. The nc-CdSe SSI-LED was investigated for the electrical and optical characteristics over 5,664 hours at V_g = -20 V. Figure 73 shows the current vs. time curve in this period with the low-magnification photos recorded every 480 hours for comparison. The current dropped slightly, e.g. ~10%, after 2,400 hours and ~20% after 5,664 hours. However, the low-magnification photos show negligible difference on the light brightness after 5,664-hour operation. Figure 74 shows the emission spectra of the same sample before and after the 2,400- and 5,664-hour operation. The shape and the wavelength range of the spectrum remain the same with a observable drop on the light emission intensity. This phenomenon can be explained by the thermal excitation principle that the current passing through the conductive path decreases and so does the operation power after

5,664 hours. The smaller driving power induces less heat to the conductive path and therefore, weaker light intensity is observed. The long lifetime of the new LED is due to the unique structure of the device, i.e., surrounding the conductive paths with the high-quality dielectric film, which prevents the oxidation from the air.

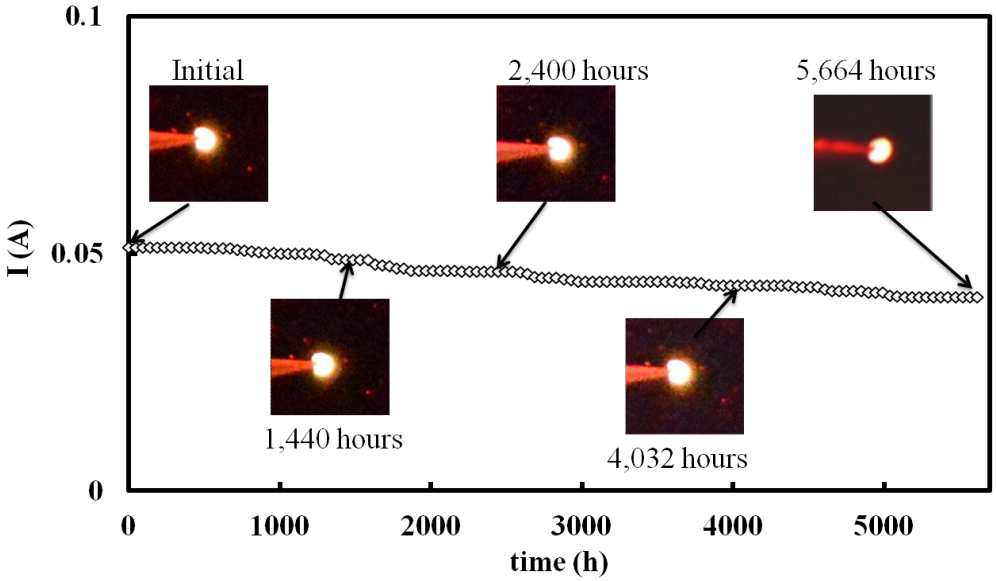


Figure 73. Current and low-magnification photos on the nc-CdSe SSI-LED within 5,664-hour operation.

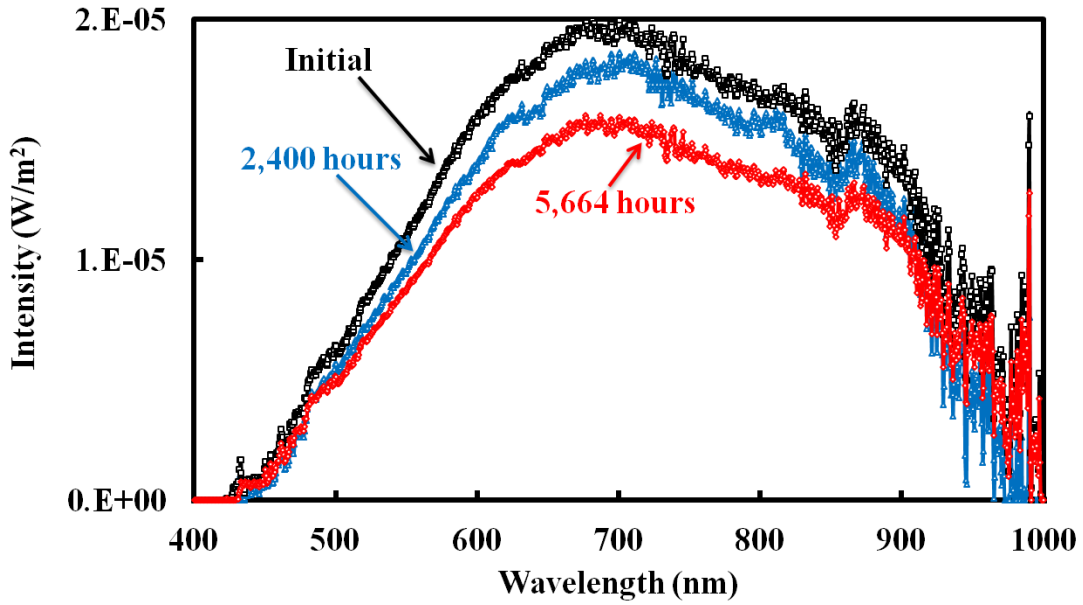


Figure 74. Emission spectra of the same sample as Fig. 73 between the initial and after 2,400- and 5,664-hour operation.

5.5 New Matrix Operation by Using Metal Interconnect

Recall the Fig. 68 and 70 in this chapter, part of the electrode will be blocked by the probe needle during the SSI-LED testing. By blocking the electrode, the EQE will be underestimated and moreover, only one SSI-LED can be driven at one time, which limits the application of the SSI-LED. Therefore, a new device driving matrix is proposed. By extending the metal interconnect to the edge of the wafer, the electrode will not be blocked during testing and multiple devices can be driven at the same time. Operating the SSI-LED with the new driving matrix, the light can be lit into many interesting patterns as shown in Figure 75, e.g., line, triangle, square pattern, etc.

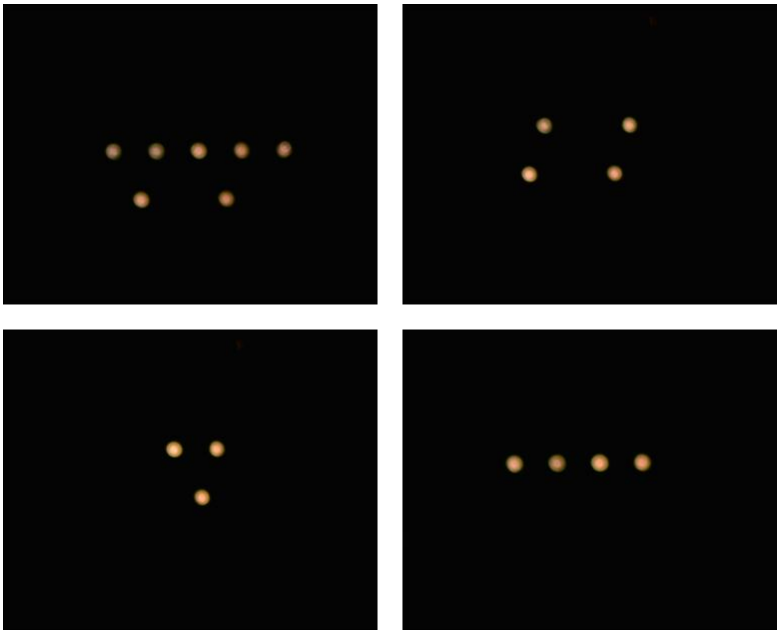


Figure 75. Patterns created by the new LED driving matrix.

5.6 Summary

Light emission from the amorphous ZrHfO high-k stack on the p-type Si wafer under the gate bias condition has been studied at room temperature. The broad band light including the visible and near IR wavelengths was emitted from many small conductive paths formed after the dielectric breakdown. The light intensity is affected by the thickness of the high-k stack as well as the polarity and $|V_g|$. Light generation is due to the thermal excitation mechanism which is different from the electron-hole or exciton recombination mechanism in conventional p-n junction or QW LEDs. The similar warm white light was emitted from the nc-CdSe embedded ZrHfO dielectric stack. The inclusion of the nc-CdSe layer in the ZrHfO film induces larger leakage current

compared to the 12-min deposited control sample, which causes the higher intensity of the emitted light and EQE. However, the light emitting principle does not change with the inclusion of the nc-CdSe layer. The light intensity of the nc-CdSe embedded ZrHfO LED increases with the increase of the $|V_g|$. Very high CRI, i.e., 98.4, can be obtained from this new SSI-LED. The surface of the high-k layer is smooth prior to the light emission for both nc-CdSe SSI-LED and its control sample. After the dielectric breakdown, the bumps and holes were formed on the surface of the ZrHfO layer in both samples due to the high leakage current passing through the conductive paths. The change of duty cycle does not change the light emission principle but the light emission intensity decreases linearly with the drop of the duty cycle. Moreover, for the nc-CdSe SSI-LED and its control sample, the light emission characters have negligible change under the same duty cycle of 75% but different driving frequencies due to the fast response of the ultra short conductive path. Overall, this new single-chip, long lifetime, high CRI SSI-LED is easy to fabricate using the IC compatible process and can be applied to a wide range of products.

CHAPTER VI

FACTORS AFFECTING LIGHT EMISSION FROM SOLID STATE INCANDESCENT LIGHT EMITTING DEVICES WITH SPUTTER DEPOSITED ZIRCONIUM-DOPED HAFNIUM OXIDE THIN FILMS*

6.1 Introduction and Motivation

As introduced in the Chapter V, the newly invented SSI-LED can emit the broad band white light from a single device with very long lifetime, i.e., > 5,664 hours. The light is emitted from many conductive paths formed in the thin metal oxide high-k layer based on the thermal excitation process similar to the blackbody emission. For the high-k dielectric, the PDA condition is critical to both the bulk- and the interface-layer properties.[106-108] Since the conductive path in the high-k film is formed from the breakdown process, the light emission mechanism and the spectrum characteristics are dependent on the fabrication process. Currently, there is no report on the PDA process effect on the performance of the SSI-LED. In this study, the PDA process effects on the emission spectrum of this new SSI-LED with respect to changes of the material and electrical properties will be investigated.

* Part of data reported in this chapter is reproduced from "Factors affecting light emission from solid state incandescent light emitting devices with sputter deposited Zr-doped HfO2 thin films", by Chi-Chou Lin and Yue Kuo accepted for publication in the Journal of Solid State Science and Technology, 3, Q182-Q189 (2014) by permission of ECS-The Electrochemical Society.

6.2 Experimental

The SSI-LED used in this study has the same fabrication process as that in the 6-min SSI-LED discussed in Chapter V. However, the sample was not only treated with a PDA step at 800°C, 3 min in the N_2 atmosphere, but also treaterd at 900°C, and 1,000°C. The complete sample was annealed at 400°C for 5 min under the H_2/N_2 (1:9) atmosphere. The HRTEM and XPS were used to examine the physical thickness and the chemical bonding states for the sample before and after V_g stress. The LED's J-V and C-V curves were measured with an Agilent 4155C semiconductor parameter analyzer and an Agilent 4284A LCR meter, separately. The D_{it} was calculated from the C-V curve using the Lehovec's method.[213] For the light emission experiment, the ITO electrode was stressed with a V_g and the emitted light was measured with an OES. The chromaticity coordinates on the 1931 CIE chart, CCT, and CRI were also investigated by the same way discussed in Chapter V.

6.3 Material Properties of the SSI-LED Annealed under Different Temperatures

Figure 76 shows the XRD patterns of samples with different PDA temperatures, i.e., 800°C, 900°C, and 1,000°C, respectively. The peak at θ .1° is from the Si substrate.[229] No peak of the crystalline HfO_2, i.e., at 28.4°, 31.7°, 34.4°, 35.6°, or ZrO_2, i.e., 28.2°, 30.0°, 31.5°, is detected.[230] The HfO_2 and ZrO_2 films crystallize at below 600°C.[231-232] However, the addition of a third element into the metal oxide could increase the crystalline temperature by a few hundred degrees.[159,164,183,233] Therefore, the ZrHfO film in the sample did not form crystalline HfO_2 or ZrO_2. Figure 77 also shows the cross-

sectional HRTEM micrographs of samples with the (a) 800°C, (b) 900°C, and (c) 1,000°C PDA temperatures, respectively. The total physical thickness of the high-k stack decreases with the increase of the annealing temperature, i.e., from 6.4 nm at 800°C to 6 nm at 1,000°C. However, the interface layer thickness increases with the increase of the annealing temperature, i.e., 3.3 nm, 3.4 nm, and 4 nm for 800°C, 900°C, and 1,000°C PDA samples, respectively. The bulk ZrHfO film thickness decreased accordingly. The high annealing temperature enhanced the oxygen diffusion through the metal oxide layer and the oxidation rate at the Si interface, both of which facilitated the growth of interface layer.[234-236] The formation of the interface layer consumed the bulk high-k film. The high annealing temperature could also densify the bulk high-k film to shrink its thickness.[237-238]

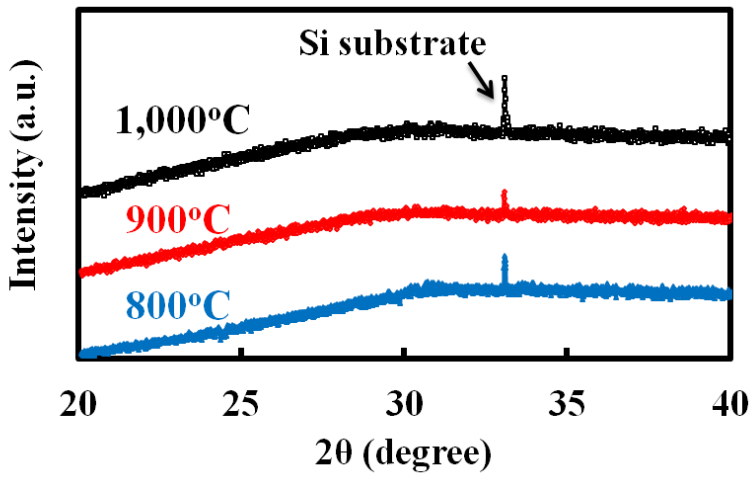


Figure 76. XRD analysis of the ZrHfO SSI-LEDs under 800°C, 900°C, and 1,000°C PDA temperatures.

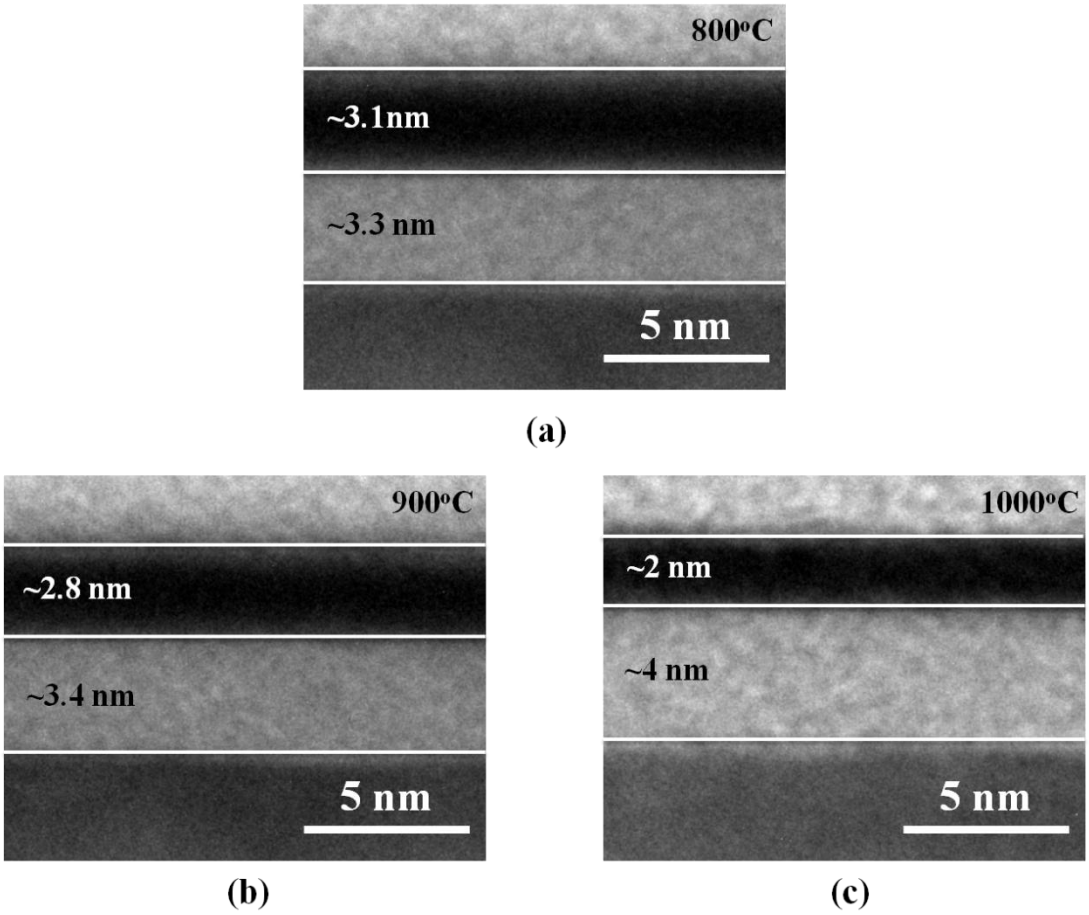


Figure 77. Cross-sectional TEM micrographs of (a) 800°C, (b) 900°C, and (c) 1,000°C PDA temperature.

6.4 Electrical and Optical Properties of the SSI-LED Annealed under Different Temperatures

Figure 78 shows the low- and high-magnification photos of lights emitted at V_g = -60 V from samples with the 800°C, 900°C, and 1,000°C PDA temperatures. The 4-cluster photos contain SSI-LEDs of different diameters, e.g., 250 μm, 300 μm, 350 μm, and 400 μm. The high-magnification photos are from the 350 μm diameter devices. The black line in each photo is due to the light blocking of the probe. Light is emitted from many tiny bright dots on the ITO electrode surface. For the conventional p-n junction or QW LED, light is uniformly emitted from the electrode area. The discrete bright dots are from the thermal excitation of the conductive paths formed from the dielectric breakdown of the ZrHfO high-k stack, which was discussed in Chapter V. Fig. 78 also shows that both the number density of the light dots and the brightness increase with the PDA temperature. As shown in Fig. 77, the total physical thickness of the high-k stack decreases with the increase of the PDA temperatures. Under the same applied V_g, the thinner film is prone to earlier breakdown than the thicker film, which is due to the former's larger electric field. In addition, the interface defect density D_{it} of the high PDA temperature sample is larger than that of the low PDA temperature sample, i.e., 4.69×10^{11} $cm^{-2}eV^{-1}$, 6.49×10^{11} $cm^{-2}eV^{-1}$, and 6.86×10^{11} $cm^{-2}eV^{-1}$ for the 800°C, 900°C, and 1,000°C PDA samples, respectively. Moreover, the oxide trapped charges Q_{ot}, which is mainly related to the defect density in the bulk oxide layers,[214] also increased with the increase of the PDA temperature, i.e., 1.53×10^{12} cm^{-2}, 1.82×10^{12} cm^{-2}, and 2.28×10^{12} cm^{-2} for the 800°C, 900°C, and 1,000°C PDA samples, respectively. The thin high-k

stack with the large interface and bulk defect densities favors the large leakage current.[215] Therefore, it is more prone to form conductive paths in the high PDA temperature sample than the low PDA temperature sample, which favors the light emission process.

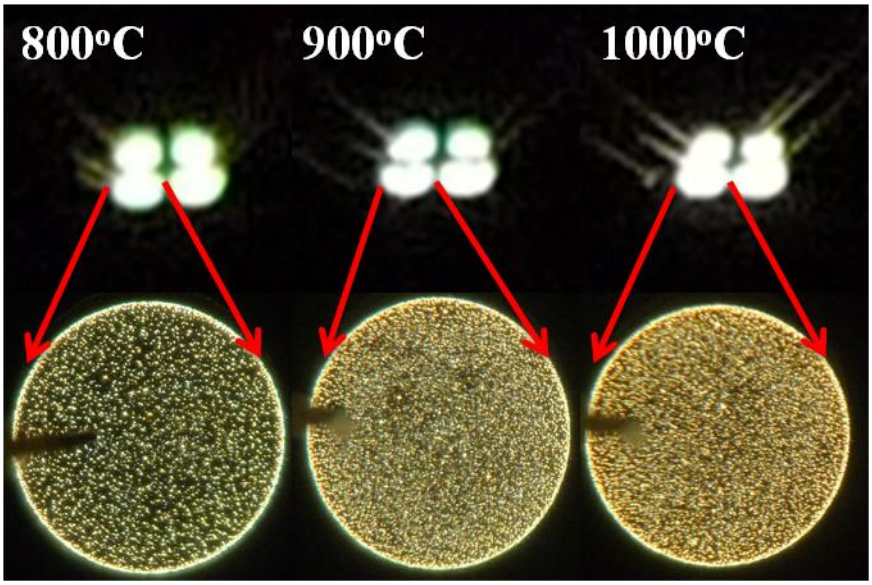


Figure 78. Low and high-magnification photos of samples with 800°C, 900°C, and 1,000°C PDA temperatures stressed at V_g = -60 V.

Figure 79 shows the energy band gap diagrams of the same device (a) before and (b) after the dielectric breakdown. When the $|V_g|$ is smaller than that of the $|V_{BD}|$, spotted defects are generated in the high-k stack. Holes are accumulated at the interface and transferred through the high-k stack following the P-F conduction mechanism.[146] With the increase of the $|V_g|$, the spotted defects are connected. Eventually when the $|V_g|$ is

larger than the $|V_{BD}|$, the dielectric stack is broken down to form the conductive paths. The conductive path functions like a resistor that is thermally excited to emit light under the high current density condition. This is similar to the light emission mechanism in the tungsten incandescent lamp.

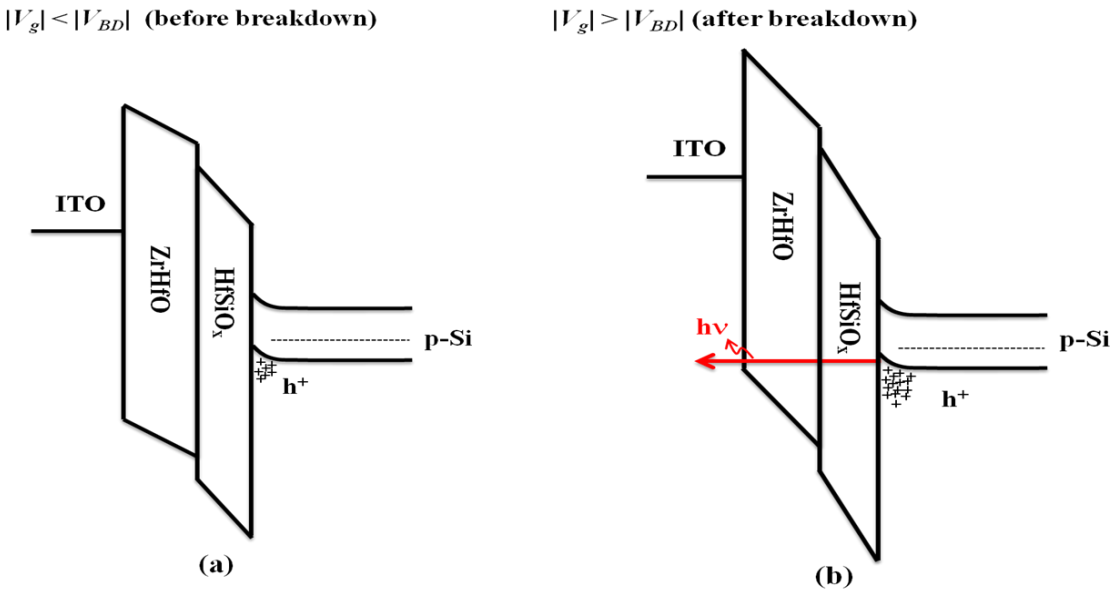


Figure 79. Band diagrams of the ZrHfO SSI-LED under (a) before breakdown, and (b) after breakdown conditions.

Figure 80 shows the emission spectra of the Fig. 78 samples, which covers the same broad range of wavelengths from near UV to 1,000 nm. The intensity increases with the increase of the PDA temperature. The inset in Fig. 80 shows that the normalized spectra of all samples almost overlap and are independent of the PDA temperature. Figure 81 shows the J-V curves of the Fig. 80 samples with V_g swept from 0 V to -30 V.

Each curve has an apparent breakdown point at V_{BD} where the current increases abruptly with the slight increase of the $|V_g|$. The $|V_{BD}|$ decreases with the increase of the PDA temperatures, e.g., -9.7 V, -9.1 V, and -8.6 V for the 800°C, 900°C, and 1,000°C PDA samples, separately. After the dielectric breakdown, the leakage current increases almost linearly with the increase of the $|V_g|$. At the same $|V_g|$, the leakage current increases with the increase of the PDA temperature. Since the sample with the high PDA temperature has a smaller high-k stack thickness than that of the low PDA temperature as discussed previously, it is easier for the former to form a hole-rich accumulation layer at the Si interface and to inject holes through the high-k stack.

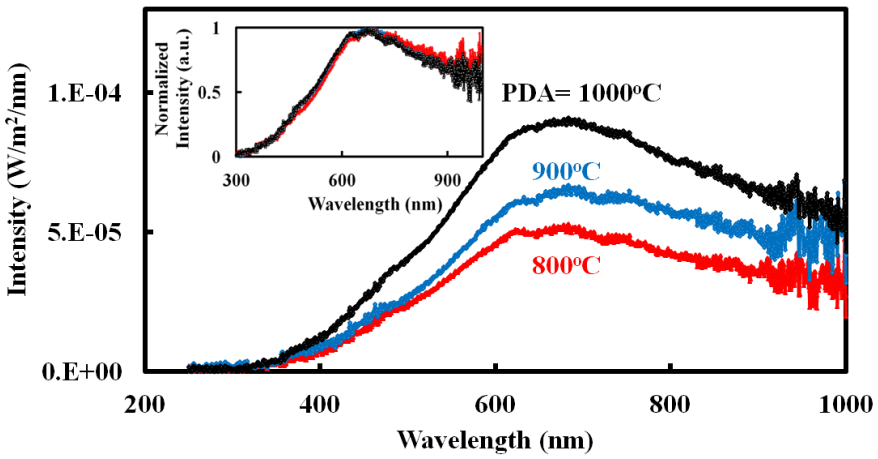


Figure 80. Spectra of the 800°C, 900°C, and 1,000°C annealed ZrHfO SSI-LEDs under -60 V stress. Inset: normalized spectra of the same SSI-LEDs.

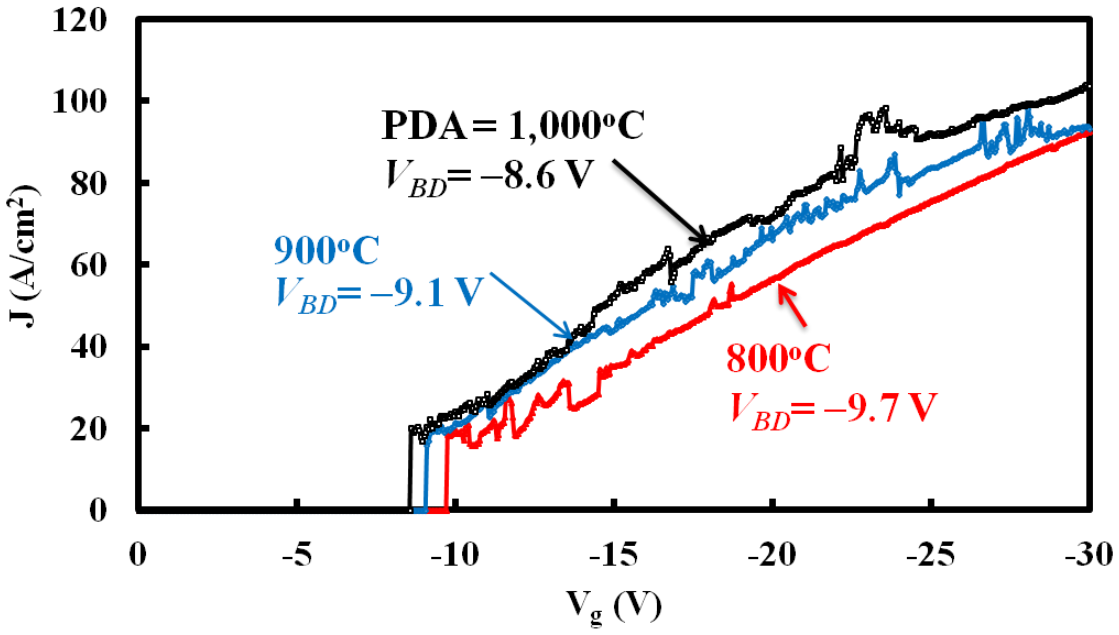


Figure 81. J-V curves swept from 0 V to -30 V of the ZrHfO SSI-LED under 800°C, 900°C, and 1,000°C PDA temperatures.

The possibility of the light emission under the electron injection condition was studied. Figure 82 shows the J-V curves of samples of different PDA temperatures with the V_g swept from 0 V to +60 V, which corresponds the electron-injection from the p-type Si wafer or hole-injection from the ITO electrode. No light emission was detected throughout the whole range. The leakage current in the $+V_g$ range is very different from that in the $-V_g$ range. From V_g of 0 V to around 4 V, the J increases slightly with the increase of V_g. The J jumps by 2 orders of magnitude with the further increase of the V_g. However, the $|V_g|$ where the J jumps in Fig. 82 is smaller than that in Fig. 81, i.e., 4 V vs. (-8.6 V to -9.7 V). Since the band offset between the Si substrate and the $HfSiO_x$

interface layer for the electron is smaller than that for the hole, i.e., 1.2 eV vs. 3.8 eV,[183] it is easier to transfer the former through the high-k stack than to transfer the latter. With the further increase of the $|V_g|$ up to +60 V, the J increases slowly and appears to approach the saturation value of 4.0×10^{-5} to 5.0×10^{-5} A/cm^2. On the other hand, the J in Fig. 81 jumps by more than 5 orders of magnitude near the V_{BD} point. The leakage current at V_g = -30 V is more than 6 orders of magnitude larger than that at V_g = 30 V in Fig. 82. In addition, the J increases linearly with the further increase of $|V_g|$ in Fig. 81. For the Fig. 82 case, it is possible that the number of electrons tunneled through the high-k stack increased with the increase of the V_g but the film was not physically broken down to form the conductive paths. The near saturation leakage current at the large $+V_g$ is due to the limited number of electrons transferring through the high-k stack, which were supplied from the inversion region of the p-type Si. For the Fig. 81 case, conductive paths were physically formed from the breakdown of the high-k stack. The conductive path functions as a resistor of which the current increases with the increase of the $|V_g|$.

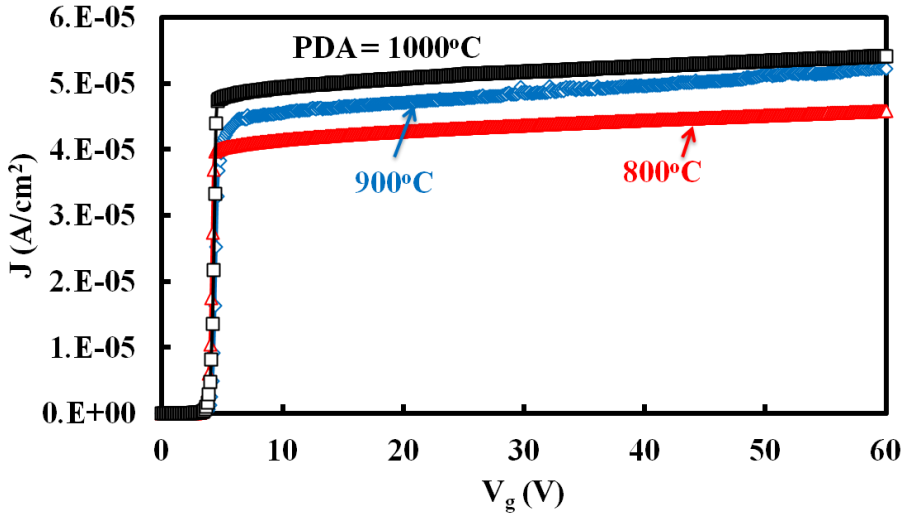


Figure 82. J-V curves from 0 V to +60 V of the ZrHfO SSI-LED under 800°C, 900°C, and 1,000°C PDA temperatures.

Separately, a control sample, i.e., the ITO electrode in direct contact with the Si wafer without the ZrHfO layer, was prepared under the same process condition as that of the Fig. 81 samples. No light emission was detected under either the negative or positive V_g stress condition. Therefore, the creation and thermal excitation of the conductive path in the high-k stack is the cause of light emission in the SSI-LED.

The emitted light was characterized for the chromaticity coordinates in the CIE 1931 chart, CCT, and CRI values including R_a and R_9. Figure 83 (a) shows that all lights emitted from SSI-LEDs of 800°C, 900°C, and 1,000°C PDA temperatures are located in the warm white light region of the CIE chart. The tungsten incandescent light bulb and the YAG:Ce-based white LED are also marked in the same figure for comparison.[220,221] All lights emitted from the SSI-LEDs are close to that of the incandescent light bulb.

They are probably based on the similar light emission principle, i.e., thermal excitation of the conductive filament. Figure 83 (b) is the enlarged view of the 3 samples of the Fig. 83 (a) with the Planckian locus.[239] Both the CCT and CRI R_a increase with the increase of the PDA temperature, i.e., 2,955 K and 97.8 for the 800^{o}C PDA sample, 3,038 K and 97.9 for the 900^{o}C PDA sample, and 3,224 K and 98.1 for the 1,000^{o}C PDA sample. These CRI R_a's are close to that of the black body emission of the incandescent light bulb, i.e., 100.[79] The increase of CCT with the increase of the PDA temperature in Fig. 83 (b) is due to the shift of the color coordinates toward the bluish white direction. The large CRI R_a of the high PDA temperature sample is contributed by the small chromaticity distance to the Planckian locus. Also, all samples have very large special CRI R_9's, e.g., 88.3, 89.7, and 91 for 800^{o}C, 900^{o}C, and 1,000^{o}C PDA samples, separately. The CRI R_9 is critical for deep-red rendering. The CRI R_9 of the fluorescent light lamp is 11 and that of the commercial YAG:Ce-based white LED is -2.5.[240-241] The combination of the large CRI R_a and R_9 numbers of the ZrHfO LEDs is important for the reproduction of the natural and vivid colors of different objects.[242] Moreover, the EQE increased as the increase of the PDA temperature while the device is stressed at -50 V, e.g., 0.079%, 0.100%, and 0.134% for 800^{o}C, 900^{o}C, and 1,000^{o}C PDA samples, respectively.

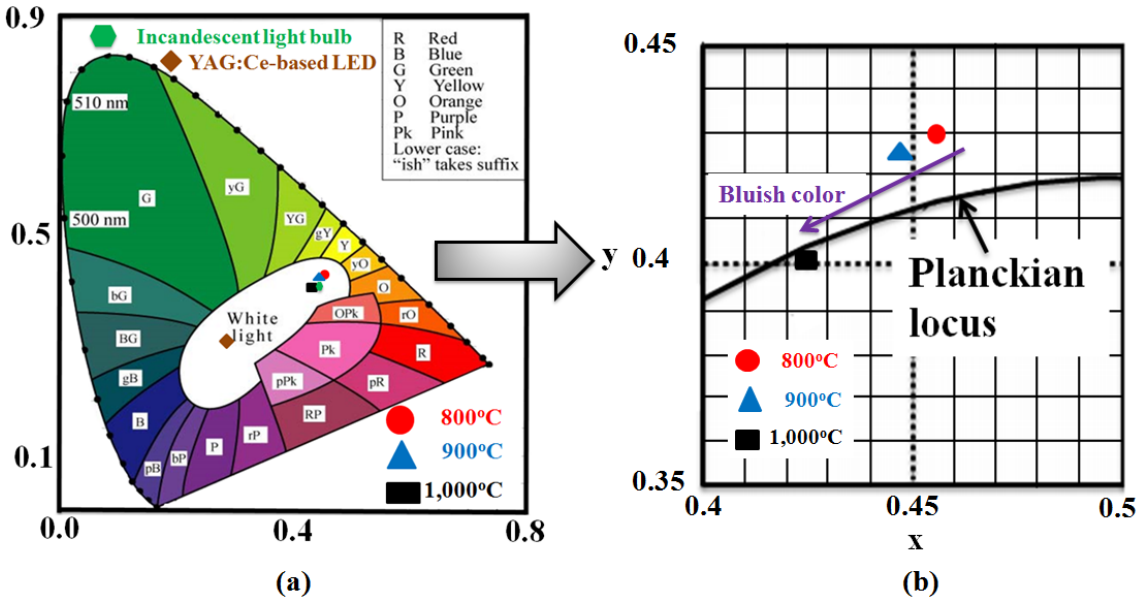
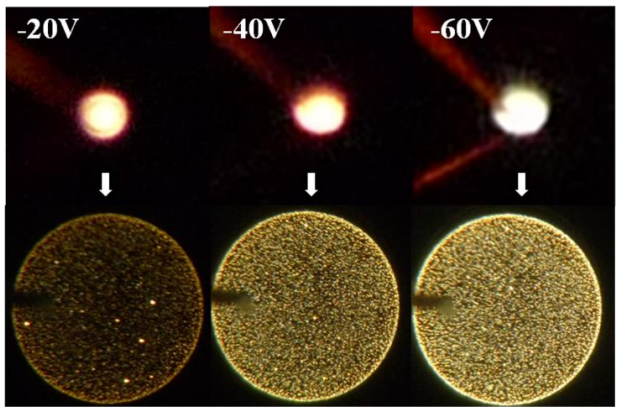


Figure 83. (a) The location of the CIE 1931 chromaticity coordinates of the 800°C, 900°C, 1,000°C PDA SSI-LEDs, W incandescent light, and YAG:Ce white LED, and (b) the enlargement of (a) with the Planckian locus of the 800°C, 900°C, 1,000°C PDA SSI-LEDs.

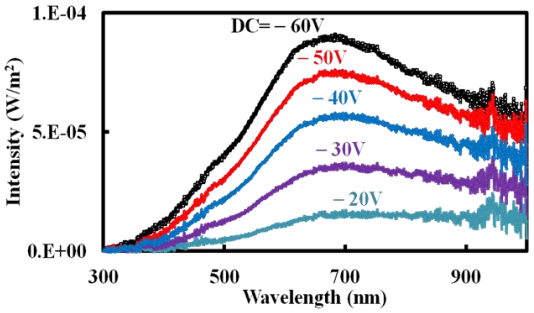
6.5 More Studies on the 1000°C PDA Annealed SSI-LED

Since the LED with the 1,000°C PDA shows the highest light intensity, EQE, and the largest CRI R_a and R_9 values among the three samples, its electrical and material properties were studied further. Figure 84 (a) shows the low- and high-magnification photos of the sample stressed at V_g = -20 V, -40 V, and -60 V, respectively. Both the visual light brightness and the number of the bright dots increase with the increase of the $|V_g|$. Figure 84 (b) shows that the wavelength range of the emission spectrum does not change but the intensity increases with the increase of the $|V_g|$. This result can be

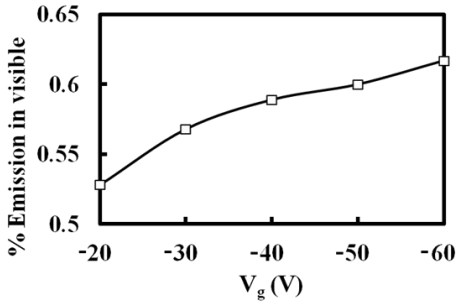
explained by the thermal excitation mechanism of the conductive path. The current passing through the device increases with the increase of the $|V_g|$. The large electrical energy induces more heat to the conductive path than the low electrical energy case, which causes the brighter light emission of the former. With the increase of the $|V_g|$, the peak wavelength (λ_{peak}) shifts to the blue direction, i.e., from 701 nm at -20 V to 683 nm at -60 V. Figure 84 (c) shows the increase of the % emission in visible, which was calculated by dividing the area from 380 nm to 780 nm with the area from 200 nm to 1,000 nm, with the increase of the $|V_g|$. Therefore, the efficiency of the visible light emission increases with the applied $|V_g|$. The similar increase on the % emission in visible has been observed in the tungsten incandescent light under the high voltage operation condition.[226-227] This is another indication of the similarity of light emission principle of the SSI-LED and the conventional incandescent light bulb. Table 9 summarizes changes of the sample's CIE color coordinates, CCT's, and the CRI's with the applied $|V_g|$. The CIE coordinate numbers decrease and the CCT increases with the increase of the applied $|V_g|$. This phenomenon can be contributed to the blue shift of the light, which is consistent with the change of the λ_{peak} number. In addition, the increase of the CRI with the increase of the $|V_g|$ is contributed by the reduction of the chromaticity distance to the Planckian locus. Therefore, the light emission characteristics of the SSI-LED move toward those of the black body emission when the $|V_g|$ is increased.



(a)



(b)



(c)

Figure 84. (a) Low and high-magnification photos, (b) spectra of the ZrHfO SSI-LED under -20 V to -60 V stress conditions, and (c) percentage of emission in visible range of the 1,000^{o}C PDA ZrHfO SSI-LED.

Table 9. CIE color coordinates, CCT, and CRI values for 1,000°C ZrHfO SSI-LED under different bias conditions.

V_g	CIE x	CIE y	CCT [K]	CRI R_a	R_9
–60V	0.423	0.400	3224	98.1	91
–50V	0.427	0.401	3152	98.2	90.9
–40V	0.430	0.401	3054	97.9	89.8
–30V	0.434	0.402	3031	97.8	90.8
–20V	0.439	0.406	2990	97.9	95.5

Since the light emission of the device is from the thermal excitation of the conductive path, the composition material of the device may change after the light emission process. Figure 85 shows the cross-sectional HRTEM view of a 1,000°C PDA sample after 1 min, V_g = -60 V stress. The total film thickness increased from original 6 nm to 6.8 nm, which is contributed by the increase of the interface layer from 4 nm to 5.4 nm and the decrease of the bulk ZrHfO layer from 2 nm to 1.4 nm. The thickness ratio of the (interface layer/whole high-*k* stack) increased from 0.67 to 0.79. There are two possible factors for the above ratio change. New Hf dangling bonds can be formed inside and around the conductive path due to the high local temperature.[177] The unpassivated Hf atoms can diffuse toward the Si substrate.[178-179] The high temperature can also enhance the diffusion of oxygen from the bulk ZrHfO film to the Si wafer.[107,235] At the same time, Si can diffuse quickly through the interface layer toward the bulk

high-*k* layer at the high temperature. The Hf, O, and Si react instantaneously to form the $HfSiO_x$ at the interface. Additionally, the bulk ZrHfO film can be densified to a physically thinner layer at the high temperature.[108,234,238]

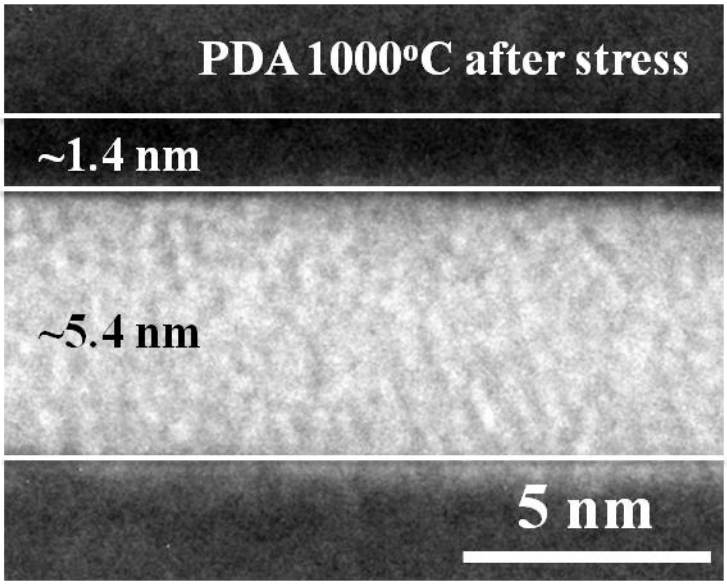


Figure 85. Cross-sectional TEM micrographs of 1,000°C PDA ZrHfO SSI-LED after 1 min, -60 V stress.

The chemical structure of the composing film also changes after the light emission process. Figure 86 shows the XPS Hf 4*f* spectra of a PDA 1,000°C sample (a) before and (b) after the 1 min, V_g = -60 V stress. In Fig. 86 (a), the two peaks at binding energies (BE's) 17.6 eV and 19.2 eV belong to the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peaks, separately. The BE of 17.6 eV peak is further deconvoluted into the HfO_2 ($4f_{7/2}$: ~17.2 eV) and $HfSiO_x$ ($4f_{7/2}$: ~18 eV) states. The former is contributed by the bulk ZrHfO film and the

latter is from the $HfSiO_x$ interface layer.[234,243] The similar $HfSiO_x$ interface layer was observed on the sample fabricated under the similar process condition.[159,164] The area ratio of the (HfO_2 peak/$HfSiO_x$ peak) in Fig. 86 (a) is 1.2. After the V_g stress, the Hf peak can also be deconvoluted into the same two peaks, as shown in Fig. 86 (b). However, the area ratio of the (HfO_2 peak/$HfSiO_x$ peak) decreases to 0.85. The decrease of the HfO_2 peak signal is consistent with the increase of the interface layer thickness and the decrease of the bulk ZrHfO film, e.g., as shown in Fig. 77 (c) and Fig. 85. The XPS spectra of Zr 3*d* of the same Fig. 86 (a) sample are shown in Figure 86 (c) before and (d) after the V_g = -60 V stress. The two Zr 3*d* peaks at BE 182.7 eV and 185.3 eV are contributed by ZrO_2 in the Zr $3d_{5/2}$ and Zr $3d_{3/2}$ states.[244-245] No peaks correspond to the Zr-silicate were detected because the interface is a $HfSiO_x$ film, as shown in Fig. 86 (a) and (b). The Zr binding energies change little after the V_g stress. This may be due to the low Zr concentration in the high-k stack compared with that of the Hf concentration, i.e., 12% vs. 88%. Therefore, the high temperature of the conductive path during the light emission process changed the bulk and interface material properties.

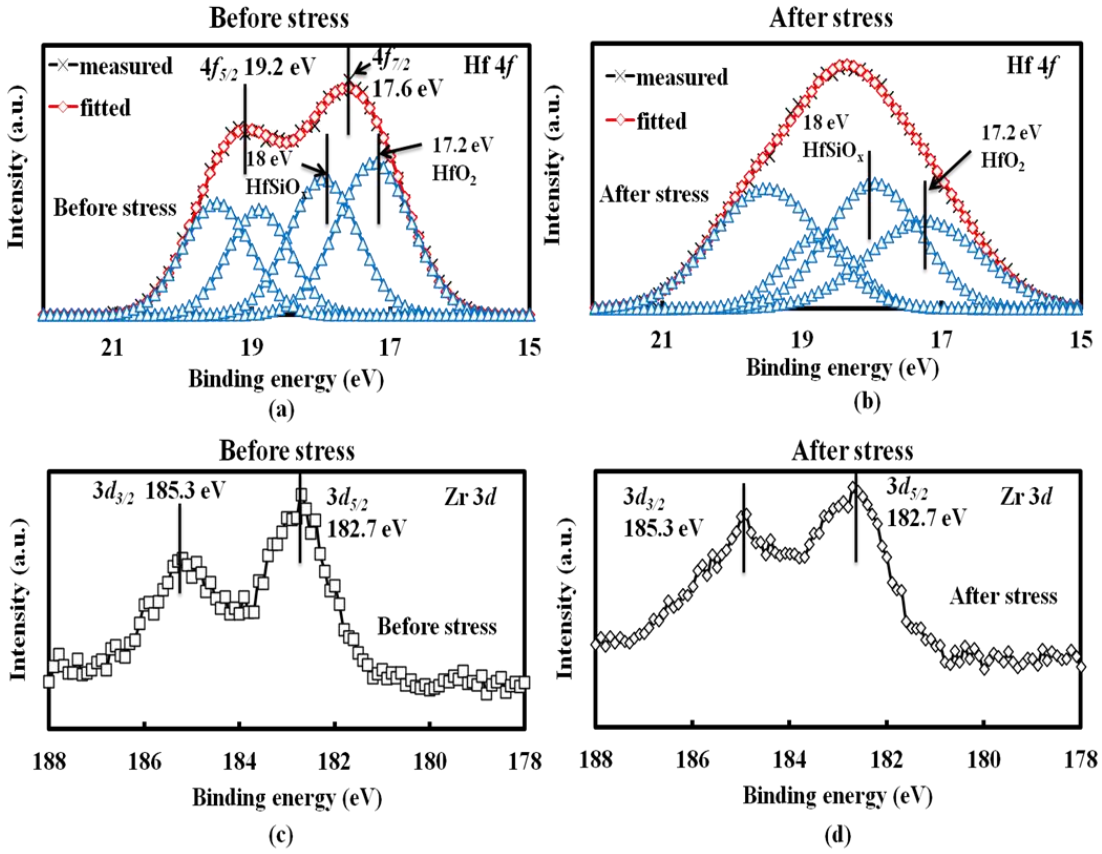


Figure 86. XPS analysis of Hf 4*f* spectra under (a) no stress and (b) 1 min and -60 V stress conditions and Zr 3*d* spectra under (c) no stress and (d) 1 min and -60 V stress conditions.

The light emission phenomenon was observed not only under the continuous DC stress condition but also the pulsed stress condition. Since the pulsed driving condition can lower down the power consumption and extend the device lifetime,[228] the light emission characteristics of the 1,000°C PDA sample under different stress conditions were investigated. Figure 87 shows the emission spectrum as a function of the duty cycle

(DC) at the 1 kHz, V_g = -50 V stress condition. The light wavelength range and the λ_{peak} location are not affected by the change of the DC. The light intensity decreases linearly with the reduction of the DC. For example, the λ_{peak} heights of the 50% and 75% DCs are 2 and 3 times that of the 25% DC. Table 10 lists the CIE chromaticity coordinates, CCT's, and CRI's, which change systematically with the reduction of the DC. If the light emission from the sample follows the black body radiation, the CCT can be taken as the real temperature of the conductive path.[225] Assuming that after the dielectric breakdown, all the input electric power (I×V) has been used to heat up the conductive paths with the neglect of heat losses from radiation and conduction to the environment. Then, the time needs for the conductive path to raise from room temperature, e.g., 298 K, to the CCT temperature, e.g., 3,152 K can be estimated by the following energy balance equation:[246]

$$Q = I \times V \times \Delta t = m \times C_p \times \Delta T \qquad [29]$$

where Q is the heat generated by the passage of the current I through a conductive path, V is the applied V_g, Δt is the time for the device to reach 3,152 K from 298 K, m is the mass of a conductive path, C_p is the heat capacity of the conductive path, and ΔT is the temperature difference between the CCT and room temperature. Assuming that all conductive paths are of the same cross-sectional area and length, the I can be calculated by dividing the measured current with the number of the conductive paths in the device, which can be estimated from the SEM micrograph. Assuming that 1) the diameter and the length of the conductive path are about 150 nm and 6 nm, separately, and 2) the

density and the C_p of the conductive path are the same as those of HfO_2, i.e., 9,680 kg/m^3 and 285.9 J/kg-K, separately,[247-248] the Δt is about 13 nanoseconds. Therefore, due to the ultra small size of the conductive path, the light emission process is much faster than the driving frequency of 1kHz. Therefore, the change of DC does not affect the light emission spectrum except the intensity.

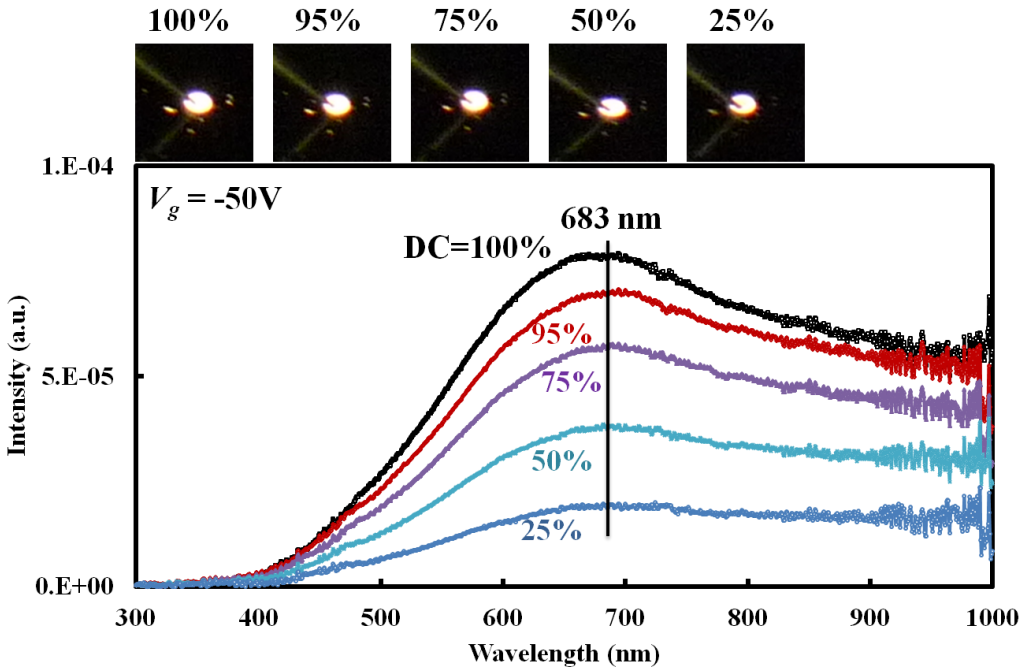


Figure 87. Emission spectra and low-magnification photos of the 1,000°C ZrHfO SSI-LED under different duty cycles. V_g = -50 V.

Table 10. CIE color coordinates, CCT, and CRI values for 1,000°C ZrHfO SSI-LED under 1kHz and different duty cycles.

Duty cycles	CIE x	CIE y	CCT [K]	CRI R_a	R_9
100%	0.427	0.401	3152	98.2	90.9
95%	0.429	0.403	3134	96.9	85.6
75%	0.430	0.404	3126	97.0	86.1
50%	0.432	0.406	3115	97.1	86.5
25%	0.442	0.420	3064	96.0	82.2

The nano size conductive path favors not only the pulsed stress condition but also the conversion efficiency of the SSI-LED. According to Forsythe et al., the radiation intensity η of the incandescent light is inversely proportional to the radius r and the length L of the filament:[225]

$$\eta \quad \frac{W}{2\pi rL} \qquad [30]$$

where W is the power. With the same 6 W input power, the light emission efficiency of the conductive path of 150 nm radius × 6 nm length should be 2.2×10^{11} times that of the tungsten filament of 100 μ radius × 2 m length. This high efficiency is not realistic probably because equation 2 is only applicable to the large size filament. However, the above simple estimation indicates the efficiency of the SSI-LED can be higher than that of the conventional incandescent light bulb.

The lifetime of the SSI-LED is crucial to the practical application. The sample with the 1,000^{o}C PDA temperature was tested for the electrical and optical characteristics over an extended period of time at the stress condition of V_g = -20 V under the atmosphere. Figure 88 (a) shows the current vs. time curve. The low-magnification photos are included to show the corresponding brightness change. The current dropped slightly, e.g. 9%, after continuous operation of 2,832 hours. However, the shape and brightness of the emitted light change little. Figure 88 (b) shows the emission spectra of the same sample before and after the 432- and 2,832-hour operations. The wavelength range of the spectrum remains the same. The location of the λ_{peak} is the same, i.e., at 701 nm. There is a slight decrease of the intensity in the short wavelength range of 450 nm to 700 nm. This phenomenon is consistent with the thermal excitation mechanism. The reduction of the current with time shown in Fig. 88 (a) indicates the decrease of the power transmitted through the conductive path. The decrease of the power causes the reduction of the light emission intensity. Moreover, the CRI value decreases slightly after the stress, e.g., 97.9 at the beginning and 97.0 after 2,832 hours, which means the move away of the CIE coordinates from the Plank locus, as shown in Fig. 88 (c). The long lifetime and slow deterioration rate of the new LED is contributed by the unique structure of the device, i.e., embedding the conductive paths in the high-quality ZrHfO dielectric film. The ZrHfO dielectric prevents the oxidation of the conductive path from the air.

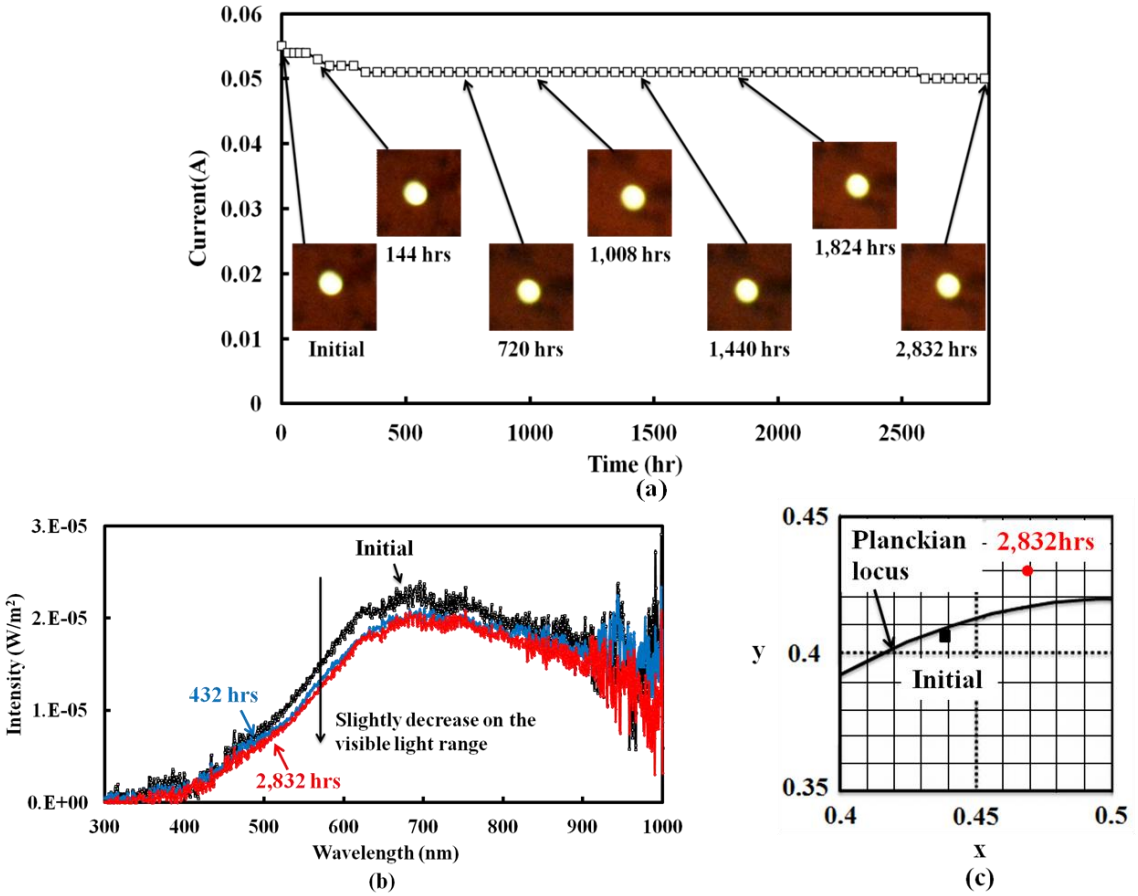


Figure 88. (a) The current and low-magnification photos of 1,000°C ZrHfO SSI-LED after 2,832-hour operation. (b) The spectra of the 1,000°C ZrHfO SSI-LED between the initial, after 432-hour, and after 2,832-hour operation. V_g = -20 V. (c) The location of the CIE 1931 chromaticity coordinates of the 1,000°C PDA SSI-LED before and after 2,832-hour operation.

6.6 Summary

The warm white light emission from the SSI-LED containing the amorphous ZrHfO dielectric stack on the p-type Si wafer has been studied. The light emission

occurred from the thermal excitation of many small conductive paths during the passage of the current. The PDA temperature affects both the material and electrical characteristics of both the bulk and the interface layers and therefore, the emission light characteristics. The CIE chromaticity coordinates, CRI's, and CCT's of the sample are close to those of the conventional tungsten incandescent light bulb. The high temperature annealed sample has a larger leakage current than the low temperature annealed sample, which causes the brighter light emission in the former. For the same reason, the light intensity increases with the increase of the magnitude of the applied voltage. The wavelength range of the emitted light is not affected by the duty cycle in the pulsed driving condition except the lowering of the intensity with the reduction of the actual driving time. The light emission process occurs almost instantaneously after the dielectric breakdown because the nano size conductive path can be quickly excited. The long lifetime and the IC compatible process make it easy to fabricate this kind of LED for various applications.

CHAPTER VII

WHITE LIGHT EMISSION FROM TUNGSTEN OXIDE DIELECTRIC FILM*

7.1 Introduction and Motivation

In Chapter V and VI, the new SSI-LED has been reported to emit the warm white light from ZrHfO and nc-CdSe embedded ZrHfO thin films. The light emission principle is the thermal excitation of conductive paths formed during the dielectric breakdown process. This kind of LED is easily fabricated using the IC compatible process without involving any environmental unfriendly chemicals. Since tungsten oxide (WO_x) has been used as the gate dielectric layer in the thin film transistor[249] and the W filament is common in the incandescent light bulb, this material can be used as a light emission layer in the new SSI-LED just like the ZrHfO film if conductive paths can be formed in it. In this study, the feasibility of light emission from the ultra thin WO_x film deposited on a Si wafer has been investigated.

***** Part of data reported in this chapter is reproduced from "White Light Emission from Ultra Thin Tungsten Metal Oxide Film", by Chi-Chou Lin and Yue Kuo, accepted for publication in the Journal of Vacuum Science and Technology B, 32,011208 (2014) by permission of American Vacuum Society.

7.2 Experimental

The MOS capacitor containing the WO_x gate dielectric was fabricated on the dilute HF cleaned p-type (10^{15} cm^{-3}) Si (100) wafer. The WO_x film was sputter deposited from the W target using the Ar/O_2 (1:1) mixture at 5 mTorr and 60 W for 2 min. After deposition, the sample was treated with a PDA step at 800℃, 900℃, and 1,000°C for 3 min under the N_2 atmosphere. Then, a layer of 80 nm ITO film was sputter deposited on top of the WO_x film and wet etched into the 300 μm diameter gate electrodes. The backside of the wafer was deposited with an Al layer to form the ohmic contact. The PMA step was done at 400°C for 5 min under the H_2/N_2 (1:9) atmosphere. The bulk- and interface-layer structures were examined with the HRTEM. The bond structure of the gate dielectric stack was characterized with the XPS. Figure 89 (a) shows the J-V curves and (b) emission spectra stressed at V_g = -20V for all three SSI-LEDs. Table 11 lists the chromaticity coordinates in the 1931 CIE chart, CCT's, and CRI's of the Figure 89 samples. They are all located in the white light region of the 1931 CIE chart. Under the same V_g condition, the SSI-LED prepared from the 1,000°C PDA has the highest light emission intensity and the lowest leakage current among the three samples, which represents the highest EQE of 0.127%. Also, it has the largest CRI R_a value of 95.1. Therefore, in this study, the material, electrical and optical properties of the WO_x sample annealed at 1,000°C has been studied.

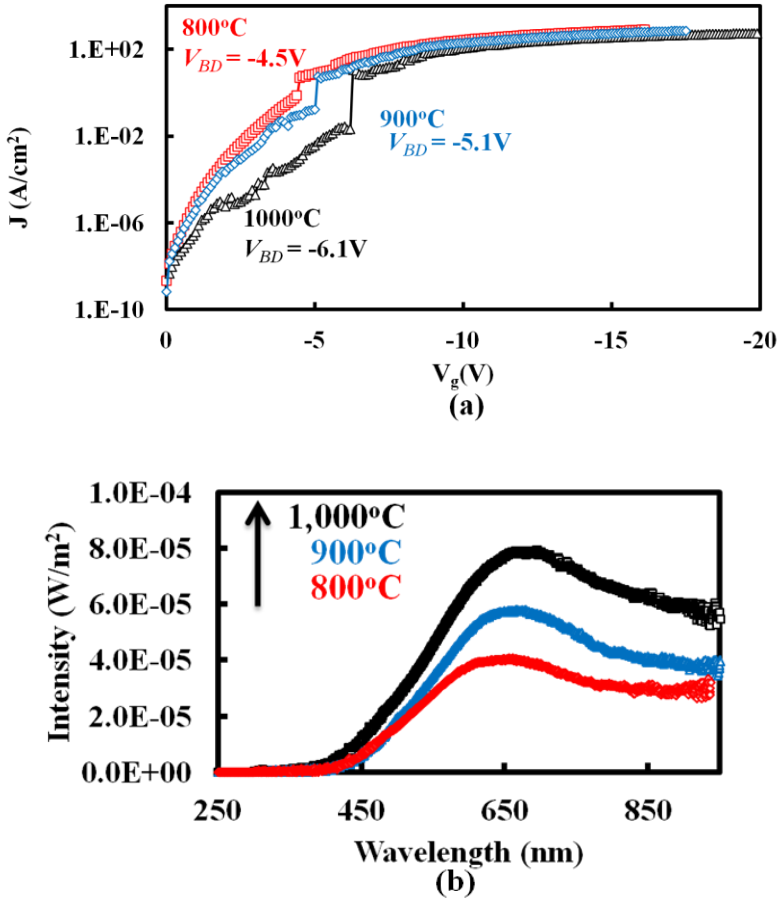


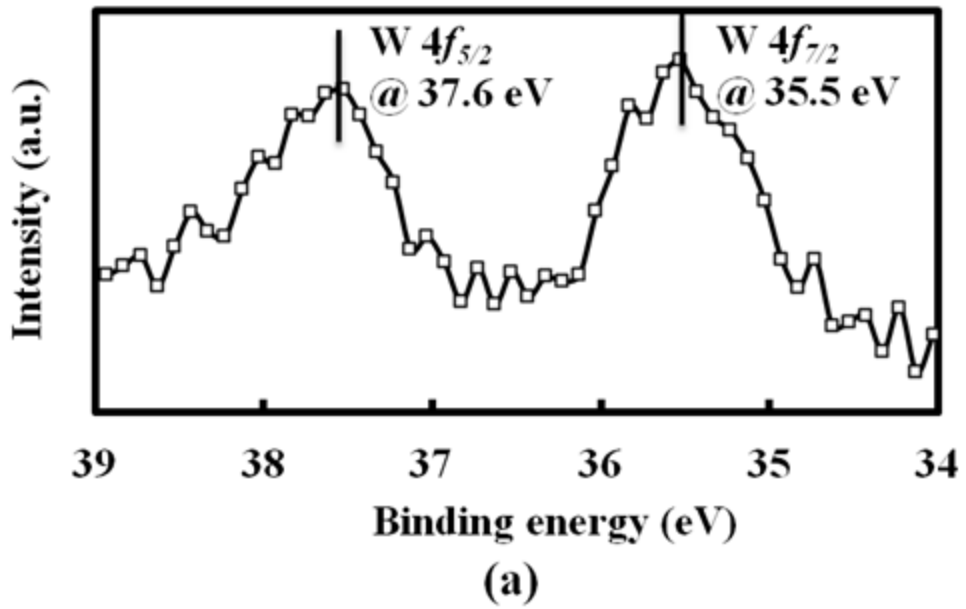
Figure 89. (a) J-V curves and (b) emission spectra stressed at V_g = -20V for WO_x SSI-LED stressed at V_g = -20V.

Table 11. CIE color coordinates, CCT's, and CRI's of WO_x SSI-LEDs with 800°C, 900°C, and 1,000°C PDA temperatures at V_g = -20 V.

PDA condition	V_g	CIE x	CIE y	CCT [K]	CRI R_a
800°C	-20V	0.455	0.428	2929	91.2
900°C	-20V	0.459	0.422	2817	92.2
1,000°C	-20V	0.460	0.422	2754	95.1

7.3 Material Properties of WO_3 SSI-LED

Figure 90 shows the XPS spectra of (a) W 4*f*, (b) O 1*s*, and (c) Si 2*p* of the WO_x dielectric stack annealed at 1,000°C. Fig. 90 (a) shows that the film contains two W peaks, i.e., at the binding energy (BE) of 37.6 eV for W $4f_{5/2}$ and BE of 35.5 eV for $4f_{7/2}$, respectively. These peaks correspond to the WO_3 compound.[250] Therefore, the WO_x film exists in the fully oxidized six-valent state, i.e., W^{6+}, after the 1,000°C PDA treatment. Fig. 90 (b) shows the O 1*s* spectrum that is deconvoluted into a major peak at BE 532.5 eV, i.e., corresponding to SiO_2, and a minor peak at BE 530.8 eV, i.e., corresponding to WO_3.[251-252] The SiO_2 component is from the interface layer formed between the WO_3 film and the Si substrate. The similar type of SiO_2 interface layer was formed between the sputter-deposited Ta_2O_5 and the Si substrate.[253] Fig. 90 (c) shows that the sample contains two Si 2*p* peaks at BE's 99. eV and 1 . eV, respectively. The former is the Si-Si bond from the Si substrate.[159] The latter is contributed by the SiO_2 interface layer,[254] which is consistent with the Fig. 90 (b) result. The HRTEM cross-sectional view of the same sample, as shown in Figure 90 (d), shows that the dielectric stack is composed of two amorphous layers, i.e., 1.6 nm thick WO_3 and 1.8 nm thick SiO_2 interface layer.



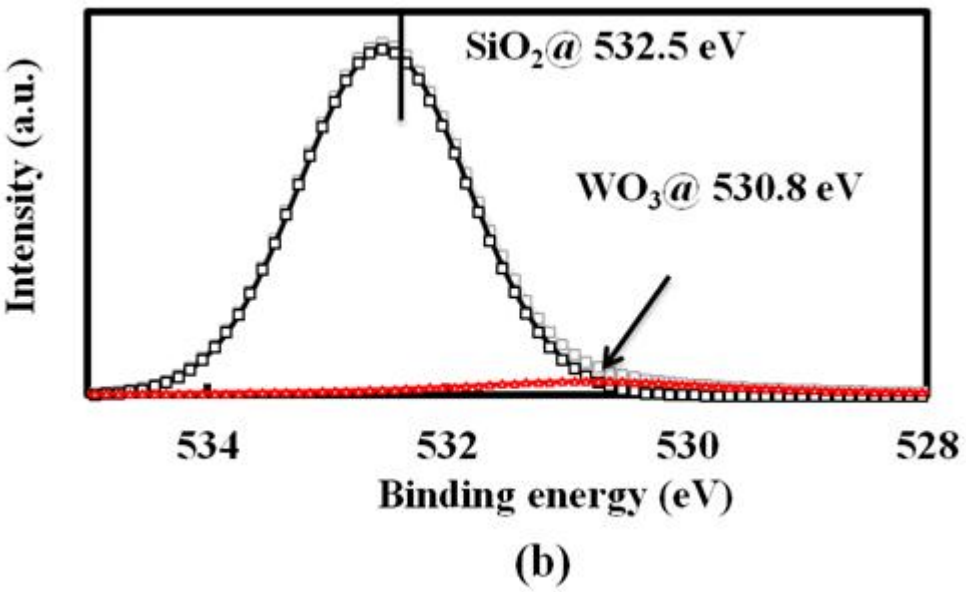
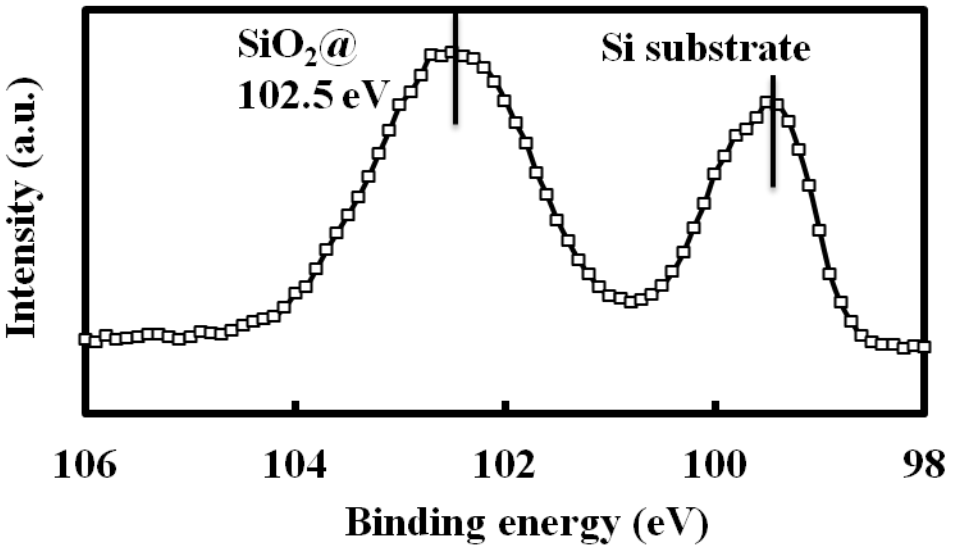
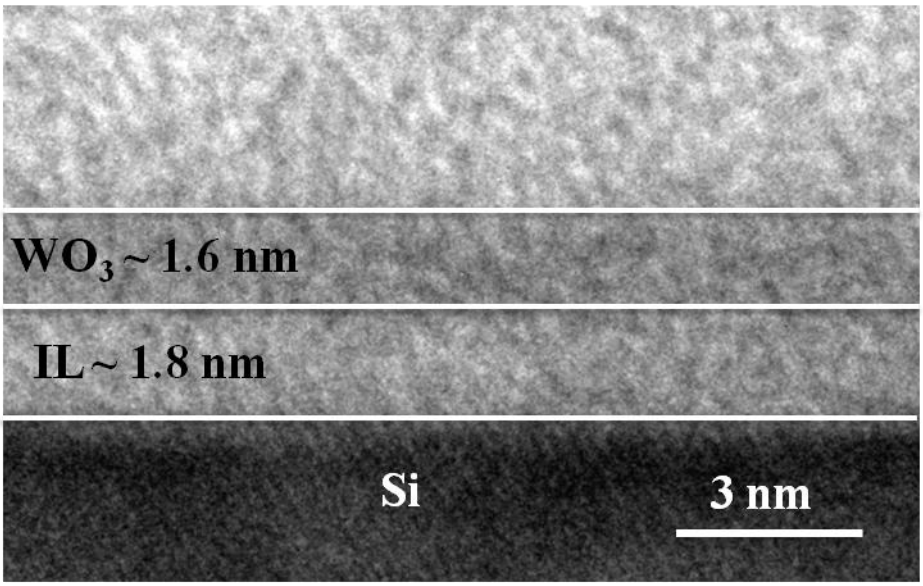


Figure 90. XPS spectra of (a) W 4*f*, (b) O 1*s*, (c) Si 2*p*, and (d) the cross-sectional view of the HRTEM of the WO_3 SSI-LED.



(c)



(d)

Figure 90 continued.

7.4 Electrical and Optical Properties of WO_3 SSI-LED

This device shows typical MOS capacitor behavior when $|V_g|$ is smaller than the $|V_{BD}|$. For example, Figure 91 (a) shows the J-V curve with V_g swept from -4 V to +4 V. In the positive V_g range, with the increase of V_g, the leakage current increases little first and then much faster until near the saturation value with an apparent transition region at around V_g = +2.5 V. In the negative V_g range, the leakage current increases slowly first and then drastically beyond -2.8 V. Since the device was fabricated on a p-type Si wafer, in the negative V_g region, the leakage current was supplied by the large number of holes formed in the accumulation region; in the positive V_g region, it was contributed by the limited number of electrons in the inversion region. The charge transfer mechanism in this dielectric stack is similar to that in the ZrHfO high-k gate dielectric stack, i.e., both follow the SE and P-F conduction mechanisms at low and high V_g, respectively. Separately, Figure 91 (b) shows C-V curves of the same sample swept in two V_g ranges. The "fresh" curve was measured from V_g = -2 V to +1 V, which trapped minimum amount of charges. The other curve was measured from V_g = -5 V to +5 V but is only shown in the -3 V to +2 V range here. The latter has a more negative V_{FB} than the former has, i.e., -0.65 V vs. -0.49 V, which represents more holes trapped in the WO_3 stack. Therefore, some defects remained in this dielectric structure even after the 1,000^{o}C PDA annealing step.

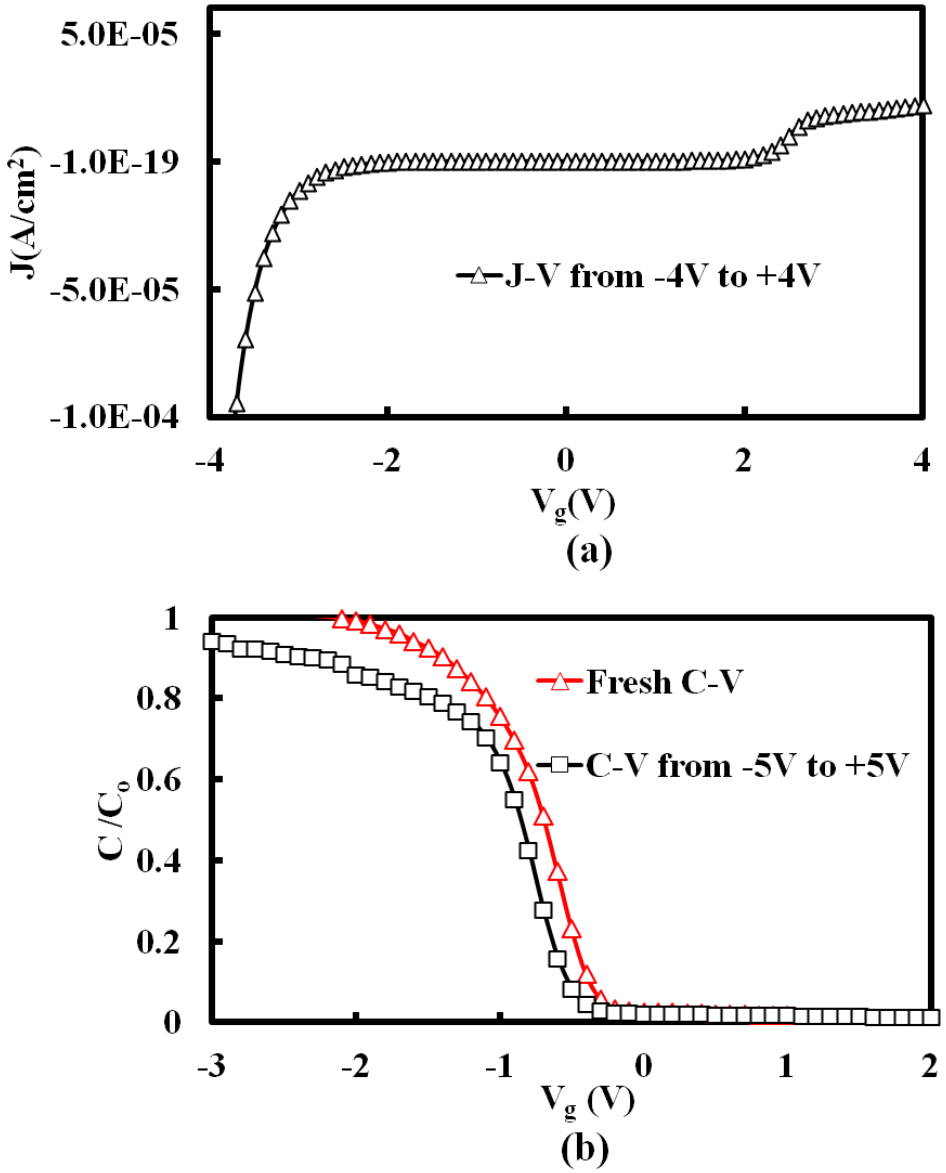


Figure 91. MOS capacitor characteristics of (a) J-V curve, and (b) C-V curves of the WO_3 SSI-LED.

Figure 92 (a) shows the low- and high-magnification photos of light emission from the WO_3 SSI-LED stressed at V_g = -20 V. The dark region in the high-

magnification photo is from the light blocking of the probe needle. Light is emitted from many separate dots evenly distributed on the ITO electrode, which is different from the uniform light emission from the conventional p-n junction or QW LED. Figure 92 (b) shows the J-V curve of the sample with V_g swept from 0 V to -30 V, which is in the hole-injection region. The leakage current jumps abruptly by three orders of magnitude at V_g = -6.1 V due to the breakdown of the WO_3 stack. No light emission was observed before the dielectric breakdown occurred, i.e., ($|V_g|$) < ($|V_{BD}|$). After dielectric breakdown, light emission was observed and the intensity of the light increased with the increase of the $|V_g|$. On the other hand, in the positive V_g range, e.g., 0 V to +60 V, no light emission was observed accompanied with the low leakage current and no dielectric breakdown. Separately, a control sample, i.e., with the ITO film directly deposited on the Si wafer without the WO_3 layer, was prepared. No light emission was observed under either the positive or negative V_g stress condition. Therefore, light emission is due to the existence of the WO_3 film and the phenomenon occurs only under the hole-injection condition. Instead of the radiative recombination of the electrons and holes occurred in the conventional LEDs, light emission from these bright dots is due to thermal excitation of conductive paths in the dielectric layer, which is similar to the principle of light emission in an incandescent light bulb. At $|V_g| < |V_{BD}|$, holes are accumulated near the Si/WO_3 interface. With the increase of the $|V_g|$, the leakage current increases and the defects are formed due to the injection of holes. At $|V_g| > |V_{BD}|$, defects are connected to form conductive paths within the WO_3 layer. Under the high leakage current condition, these conductive paths are thermally excited to emit light.

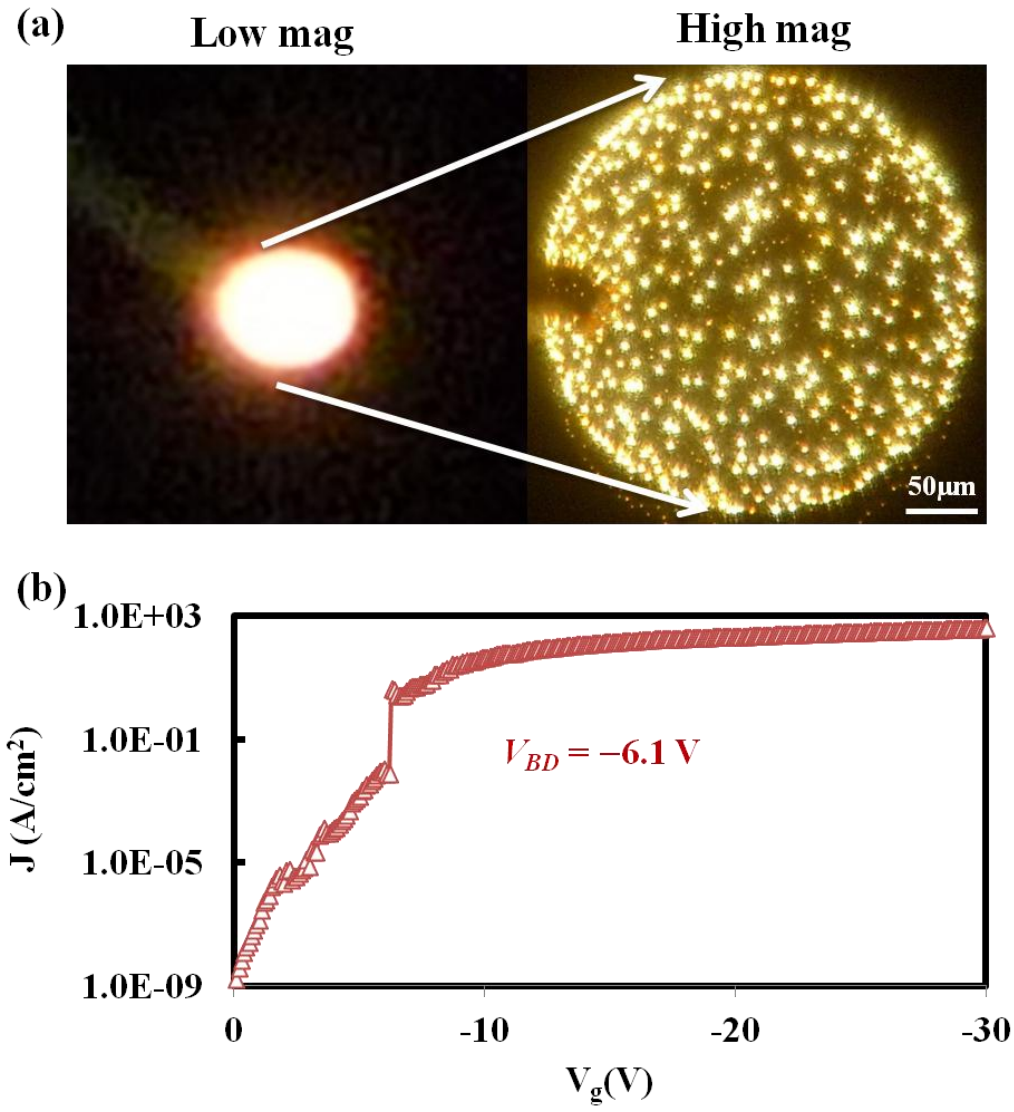


Figure 92. (a) Low and high-magnification photos under -20V stress condition and (b) the J-V curve swept from 0 V to -30 V of the WO_3 SSI-LED.

The light emission process depends not only on the polarity but also the $|V_g|$. Figure 93 (a) shows the low- and high-magnification photos of the WO_3 SSI-LED stressed at V_g = -10 V, -20 V, and -30 V, respectively. Figure 93 (b) shows that

independent of the $|V_g|$, the same broad band light, i.e., from 400 nm to 1,000 nm, is emitted. The intensity of the light increases with the increase of the $|V_g|$, which is consistent with the Fig. 93 (a) photos.

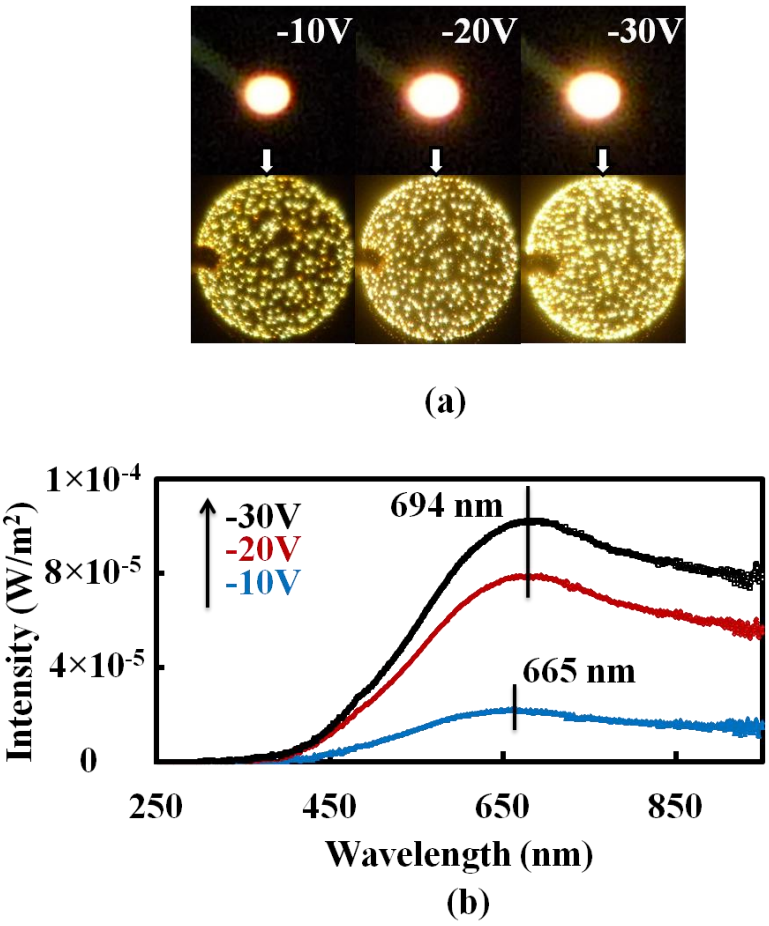


Figure 93. (a) Low- and high-magnification photos and (b) spectra of the WO_3 SSI-LED under -10 V, -20 V, and -30V stress conditions.

The EQE of the WO_3 SSI-LED at V_g = -20 V was estimated to be ~0.127%. The EQE can be increased by optimizing the device structure, the film properties, the layer thickness, PDA parameters, etc. In addition to lighting, this new device can be used in the signal generation in a spectrophotometer[255] or the optical interconnect in a semiconductor chip[256] to take advantages of the IC compatible material, structure, and fabrication process.

The emitted lights were analyzed by the CIE chart, CCT, and CRI R_a and R_9. For example, Figure 94 shows the CIE location of the light emitted from the WO_3 SSI-LED stressed at V_g = -30 V. It has the color coordinates of (0.466, 0.423) and CCT of 2,721 K. This warm white light is very close to the light emitted from an incandescent lamp with a color temperature of 2,700 K.[257] For this new LED, both the CIE color coordinates and CCT change little with the magnitude of $|V_g|$, as shown in Table 12. Therefore, this LED has good color stability over a large operation range. The CRI R_a of the WO_3 SSI-LED at V_g = -30V is much higher than that of the commercial YAG:Ce-based white LED, i.e., 95 vs. 79. The former light is from thermal excitation, which contains stronger red light emission while the latter light is from the blue LED excited yellow phosphor, which lacks the red light component. Also, the WO_3 SSI-LED has a special CRI R_9 of around 80 at V_g = -30V, which corresponds to the color rendering of the deep-red region. It is much larger than that of the tri-phosphor fluorescent lamp, i.e., CRI R_9 = 8, or the commercial YAG:Ce-based white LED, i.e., CRI R_9 = -2.5.[241] The large CRI R_9 value of the WO_3 SSI-LED makes it especially useful for the biomedical and painting applications.

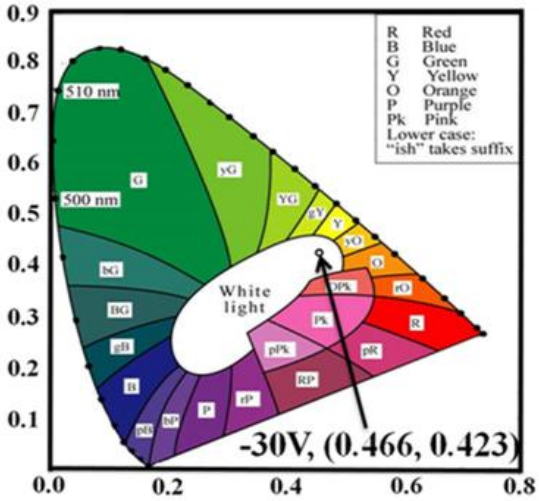


Figure 94. CIE color coordinates of WO_3 SSI-LED under -30V stress condition.

Table 12. The CIE color coordinates, CCT, and CRI of the WO_3 SSI-LED with 1,000°C PDA under various stress conditions.

Stress condition	CIE x	CIE y	CCT [K]	CRI R_a	R_9
-30V	0.466	0.423	2721	95	79
-20V	0.460	0.422	2754	95.1	79.5
-10V	0.456	0.421	2846	93.1	72.8

The power consumption of the LED can be reduced using the pulsed driving method. Figure 95 shows emission spectra of the same sample stressed at V_g = -20 V and 1 kHz with different DC's, i.e., from % to 100%. The wavelength range of the emitted light is not affected by the DC number. However, the intensity increases with the DC number. For example, the λ_{peak} heights of the 50% and 75% DC conditions are 2 and 3

times that of the 25% DC condition, respectively, which can be explained by the similar results reported in Chapter V and VI. The color coordinates, CCT, and CRI values of this new LED change slightly with the increase of the DC number, as shown in Table 13. When the DC number is lowered from 100% to 25%, the CRI increases from 95.1 to 96.9. At the same time, the CIE color coordinates move toward to the Planckian locus in the CIE 1931 chart. Therefore, except the minor change of the intensity of the emitted light, other spectrum characteristics of this new LED are stable over a large range of DC numbers at the 1 kHz and V_g = -20 V driving condition. These phenomena again can be contributed to the short length of the conductive path. The light is instantly emitted from this device upon the V_g stress and the response time is much quicker than the driving frequency.

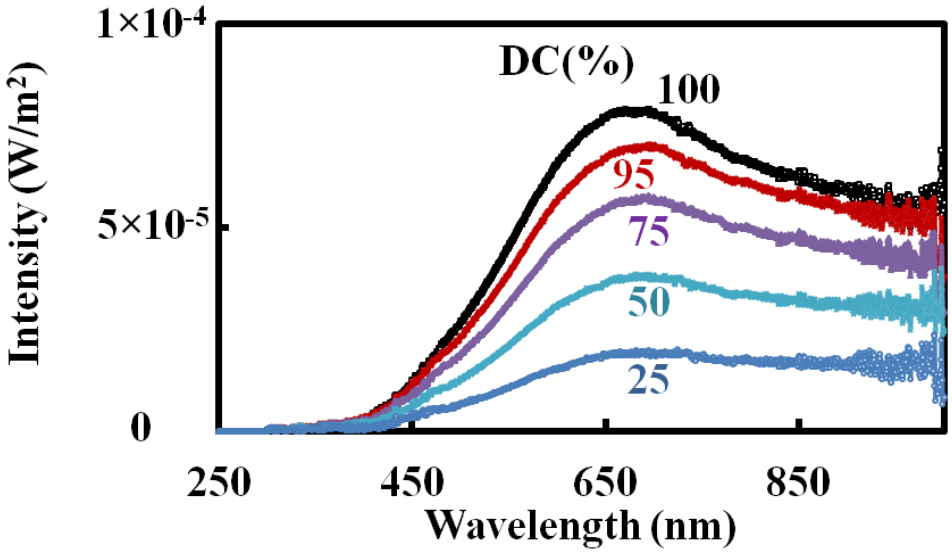


Figure 95. Emission spectra of the WO_3 SSI-LED under different duty cycles.

Table 13. The CIE color coordinates, CCT, and CRI of the WO_3 SSI-LED with 1,000°C PDA under various DCs at -20V, 1kHz.

Duty cycles	CIE x	CIE y	CCT [K]	CRI R_a	R_9
100%	0.460	0.422	2754	95.1	79.5
95%	0.457	0.422	2843	96.1	82.7
75%	0.456	0.421	2866	96.2	83.3
50%	0.455	0.417	2867	96.3	83.4
25%	0.455	0.416	2867	96.9	87.5

Although the light emission phenomenon of this WO_3 SSI-LED is repeatable, the long lifetime under the continuous operation is critical for the practical application. Figure 96 (a) shows the change of the leakage current with time at V_g = -20 V under the atmosphere condition. The low-magnification photos at different times are also included in the figure. Over the 1,300 hours operation period, this device continuously emitted light without visible deterioration of the brightness except the slight decrease of the leakage current. Figure 96 (b) shows the emission spectra of the Fig. 96 (a) LED before and after the 1,300-hour operation. There is no change of the wavelength range except the slight decrease of the intensity between 500 nm and 800 nm, e.g., the intensity of the λ_{peak} decreased by about 6%. Other light characteristics, e.g., CIE color coordinates, CCT, and CRI values, change slightly, as shown in Table 14. The long lifetime and low deterioration rate of the new LED is contributed by the unique structure of surrounding the conductive paths with the WO_3 dielectric film. Although the temperature of the

conductive path is high due to the thermal excitation mechanism, it is difficult for the air to diffuse through the dielectric layer to oxidize it.

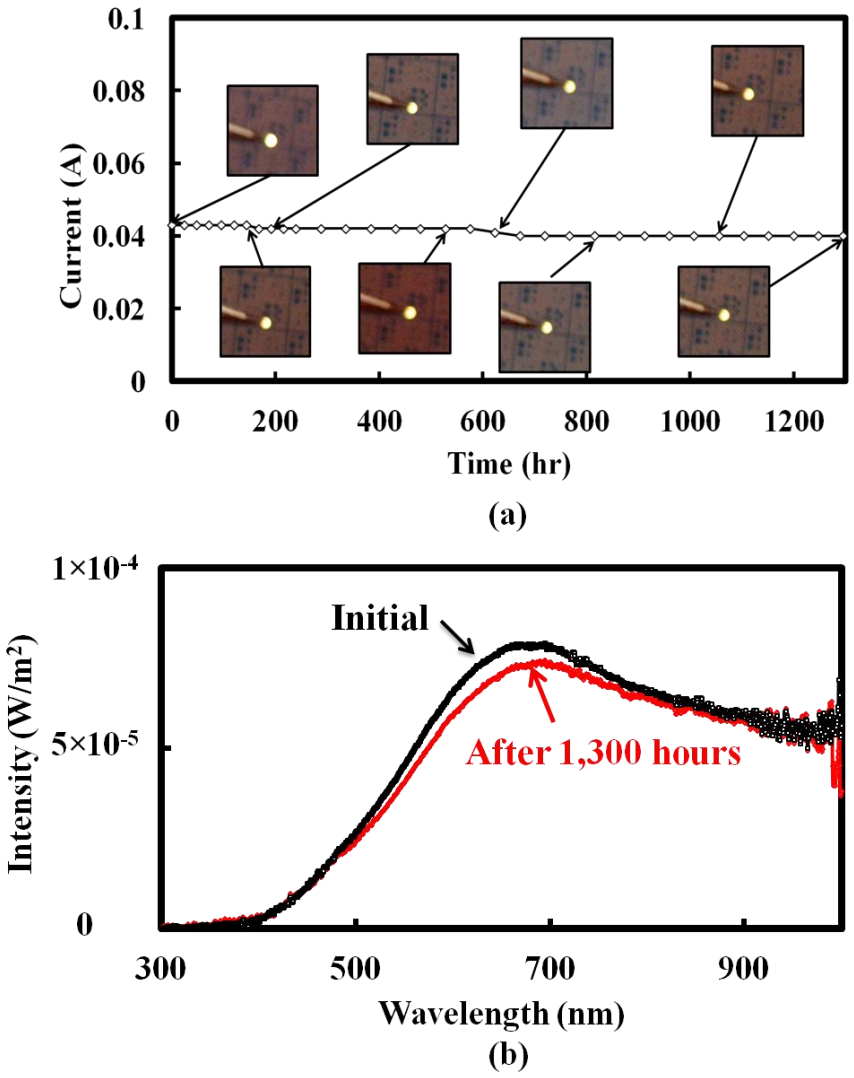


Figure 96. (a) the current and low-magnification photos on WO_3 SSI-LED within 1,300 hours. (b) the spectra of the WO_3 SSI-LED between the initial and after 1,300 hours operation.

Table 14. The CIE color coordinates, CCT, and CRI of the WO_3 SSI-LED before and after the 1,300-hour stress at V_g = -20V.

Time	CIE x	CIE y	CCT [K]	CRI R_a	R_9
Initial	0.460	0.422	2798	95.1	79.5
After 1,300 hours	0.457	0.417	2804	96.2	83.3

7.5 Summary

In summary, white light emission from a MOS capacitor with the WO_3 thin film dielectric stack on the p-type Si wafer has been observed and studied. Before the dielectric was broken, the device showed typical dielectric characteristics. After the dielectric breakdown, the broad band light in the visible wavelength range was emitted from many small bright dots due to the thermal excitation process. The warm white light characteristics have been confirmed from the CIE color coordinates and the large CRI number has been obtained. The light intensity increased with the increase of the magnitude of the applied voltage or the duty cycle in the pulsed driving condition. However, the light characteristics, such as the wavelength range and CRIs, are little affected by these factors. This new WO_3 SSI-LED has a long lifetime due to the unique structure of embedding the conductive paths in the high quality dielectric film. This kind of device is easily fabricated with the low thermal budget process. It can be used in many commercial and industrial products.

CHAPTER VIII

PROCESS EFFECTS OF COPPER FILM OVER A STEP ETCHED WITH A PLASMA-BASED PROCESS*

8.1 Introduction and Motivation

Cu is a popular interconnect material in ultra large scale integrated circuits (ULSICs) due to its lower electrical resistivity, i.e., 1.77 μΩ-cm, and large electromigration resistance.[109] The use of Cu interconnect also improves the circuit performance by lowering the RC time delay.[110] However, the Cu thin film is difficult to prepare into fine patterns using a conventional plasma etching process due to the low volatility of the reaction product.[111-113] Currently, Cu interconnect lines are prepared with the damascene or dual damascene and CMP processes.[115-117] Those processes require various complicated steps.[117] There were many studies on plasma etching of Cu, most of which were focused on increasing the evaporation rate of the plasma-Cu reaction product, e.g., by providing extra energy through direct heating or high energy infrared, ultraviolet, or laser beam exposure.[258-261]

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* Part of data reported in this chapter is reproduced from " Process effects of copper film over a step etched with a plasma-based process", by Chi-Chou Lin and Yue Kuo, accepted for publication in the Journal of Vacuum Science and Technology B, 30, 021204 (2012) by permission of American Vacuum Society.

As mentioned in the Chapter I, Kuo and Lee reported a new plasma-based Cu etch method in 2001.[118-119] Instead of vaporizing the plasma reaction product, the Cu film was converted into the chlorine or bromine compound, which was subsequently dissolved in a dilute HCl. Submicrometer Cu interconnect was successfully demonstrated by using this Cu dry etch technique.[114] For actual circuit applications, the interconnect film is often deposited on a topographic surface, e.g., over a vertical or a near-vertical step. Recall the new driving matrix proposed in Chapter V, the metal films were deposited over the ITO step. Problems, such as cusp formation at the bottom of the step,[125] microcracks,[126-127] and conductive residue,[128] often occur during deposition or after etching. In reality, many electrical failures can be observed at the cusp area because of the metal thinning and the high local stress.[129] By adding the additive gases such as Ar, N_2, or CF_4, the plasma chemistry and ion bombardment energy can be altered. In addition, the polymeric protection layer may be formed. Both of them can possibly minimize the excessive attack of the cusp area in order to prevent the electrical failure in the new LED driving matrix. In this final chapter, the effect of the additive gas in the Cl_2 plasma on the Cu line etch process has been studied. Changes of the Cu conversion rate, the attack of the cusp region, and the residue formation were investigated with respect to the plasma chemistry and ion bombardment as well as the slope of the underneath dielectric step. These issues are critical to the fabrication of the new LED driving matrix as well as the practical application of Cu interconnect lines in microelectronics products.

8.2 Experimental

The 150 nm thick PECVD SiN_x film was deposited on top of a 300 nm thick thermally grown SiO_2 on the Si (100) wafer. The SiN_x film was prepared into a line-and-space pattern defined with a photolithography step, followed by a plasma or wet etching step. The former was done with a RIE process at 100 mTorr, 500 W, and 20 sccm CF_4 for 1 min. The latter was done with a dilute buffered HF solution, i.e., 49% HF : H_2O = 0.5 : 99.5 by volume, for 2.5 min. Subsequently, the TiW/Cu (20 nm/250 nm thick) stack was sputter deposited on top of the sample. After being coated with a positive photoresist (AZ 5214) and patterned with a lithography step, the Cu film was etched with a plasma-based process as described in Refs. 118-119. The pattern size of the Cu line in this study was 30 μm wide. The plasma exposure step was carried out in a RIE reactor (Plasma Therm 700) at 40 mTorr, 500 W, and a total feed gas flow rate of 20 sccm. After plasma exposure, the sample was immersed in a dilute HCl solution (35% HCl:H_2O = 6:94) for 10 seconds to completely dissolve the $CuCl_x$ reaction product that was produced from the Cl_2 plasma-Cu reaction. The photoresist layer was then stripped with acetone in an ultrasonic bath at room temperature. The Cu conversion rate was defined as the average loss of Cu thickness on the flat SiO_2 surface over a plasma exposure period measured by the profilometer. The plasma-phase Cl radical concentration was monitored with the OES and estimated with the actinometry method.[262] The Cu line profile and residues were examined with the SEM.

8.3 Plasma Attack of Cusp Region and Pattern Edge

Figure 97 shows the SEM micrographs of the near-vertical (~80^o) 150 nm thick SiN_x step (a) without and (b) with a 250 nm thick Cu layer on top of it. In Fig. 97 (b), part of the Cu film was removed to show the cusp structure where the film at the bottom corner is thinner than that at the flat part. It was formed due to the shadow effects during sputter deposition.[263]

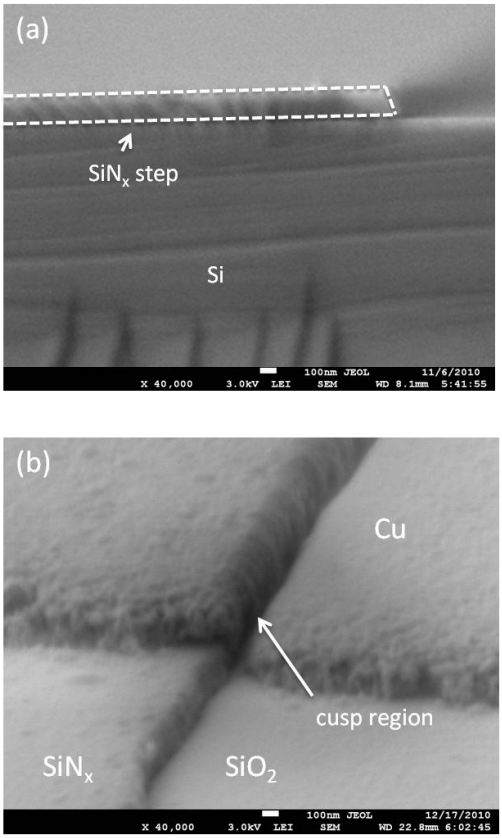

Figure 97. Cross-sectional SEM micrographs of (a) a 150 nm SiN_x step etched by RIE in the CF_4 plasma at 500 W, 100 mTorr, and 20 sccm, and (b) Cu film over the SiN_x step. The sample was tilted 70^o.

Assuming that the Cu conversion rate was constant, each film was overexposed to the plasma for 70% of the time that was required to completely convert Cu to $CuCl_x$. This overexposure time was used to be sure that no Cu stringer or residue was left after the etch process. Figure 98 (a) shows the top view of a Cu line over the SiN_x step, which was exposed to the Cl_2 plasma and subsequently dipped in the HCl solution. The total plasma exposure time was 8.5 min, which is equivalent to 70% over exposure time. Fig. 98 (b) shows the enlarged view of the "neck" structure formed at the cusp region. It was reported that the internal stress at the cusp region was higher than that at the flat area.[129] The high stress can facilitate the Cu-Cl bond formation.[264] In addition, when Cu was converted into $CuCl_x$ during exposure to the Cl_2 plasma, the volume was expanded by 7 times.[121] The expansion of the volume generated additional stress at the vertical and horizontal joint region, i.e., the cusp area, which further facilitated the Cu-Cl reaction rate.

The roughness of the Cu pattern edge in Fig. 98 (a) and (b) is contributed by the uneven local reactions. Since the Cu film is polycrystalline,[265] the Cu-Cl reaction rate at the grain boundary is different from that of the bulk region.[266-267] The difference in etch rates becomes more obvious when the Cl radical concentration is high.

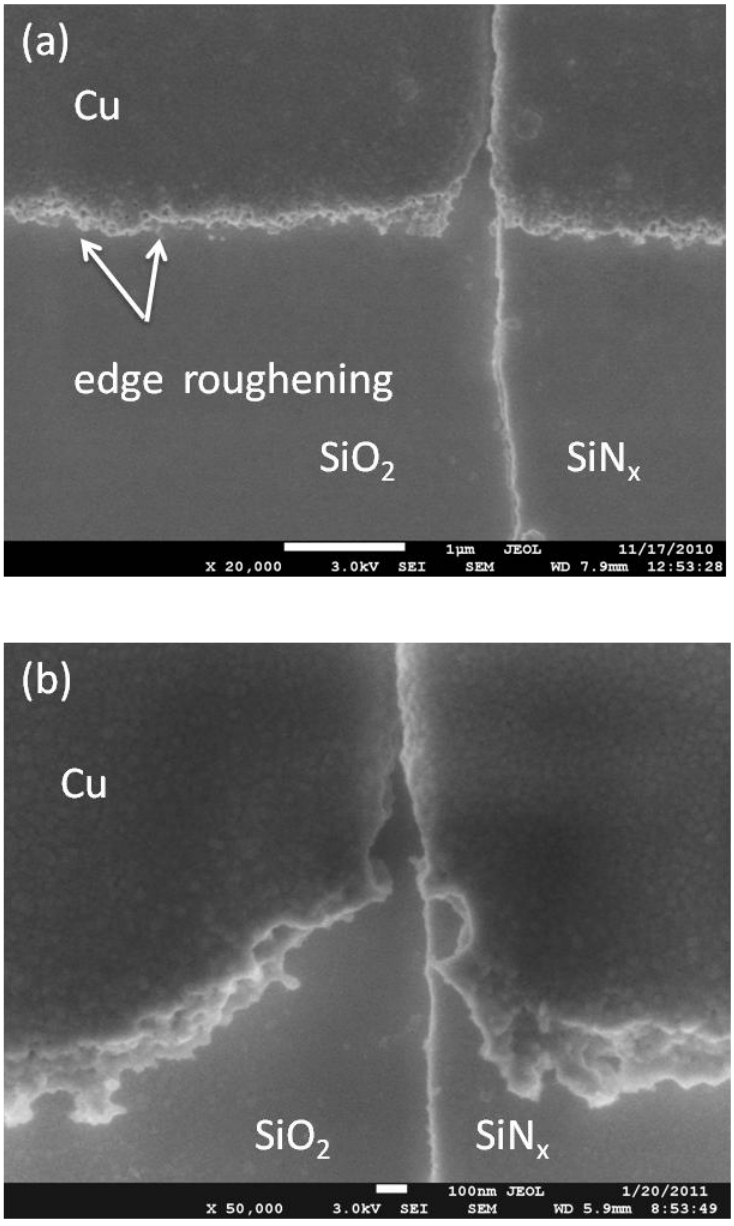

Figure 98. Top views of (a) Cu line (20k×magnification) over the 150 nm SiN_x step after Cl_2 plasma exposure with 70% over exposure time (8.5 min) followed by $CuCl_x$ removal, and (b) sample from the same process but with a higher magnification (50k×). Plasma condition: 500 W, 40 mTorr, 20 sccm.

8.4 Additive Gas Effect on Etched Cu Pattern

Several methods can be used to reduce the excessive attack of the cusp region and the edge roughness of the metal line in a plasma etching process. Since the excessive attack of the cusp region is due to the high lateral reaction rate, it can be reduced by lowering the Cl radical concentration or forming a surface hindrance layer. Gases, such as Ar, N_2 or CF_4, have been added to the Cl_2 plasma to change the Cl radical concentration.[264] In addition, when N_2 was included in the Cl_2 plasma, a CuN_x layer was formed on the Cu surface.[264] In another case, when CF_4 was added to the Cl_2 plasma, a film containing CuF_x and CF_x was formed.[268-269] If those surface layers are formed on the sidewall of Cu, the lateral direction attack of the cusp region can be reduced. The edge roughening in the metal line can be attributed to the nonuniform sidewall attack, i.e., reaction rates in the bulk grain and at the grain boundary are different. Therefore, the edge roughening of the metal line can be reduced by lowering the Cl concentration or forming a surface hindrance layer, both of which can be achieved with the addition of a proper gas component in the feed gas stream.

8.4.1 Ar Additive Effect

The Cl radical concentration and the ion bombardment energy are two major factors in the Cu conversion process. The Cl radical concentration in the Cl_2/Ar (50%/50%) plasma cannot be estimated using the actinometry method because the Ar concentration is higher than 5%.[262,264] However, the addition of Ar to the Cl_2 plasma can

increase both the Cl radical concentration and the ion bombardment energy.[270] The former is contributed by the following reaction[260,271]

$$Cl_2+Ar^* \rightarrow Cl+Cl+Ar \qquad [31]$$

while the latter can disrupt the Cu-Cu bond.[119] This is consistent with our observation that the Cu to $CuCl_x$ conversion rate in the Cl_2/Ar (50%/50%) plasma was about 1.7 times that in the Cl_2 plasma, e.g., 830 vs. 500 Å/min under the same plasma condition of 40 mTorr, 500 W, and total gas flow rate of 20 sccm.

Figure 99 (a) shows the top view of the edge of a Cu pattern over the SiN_x step after being exposed to the Cl_2/Ar (50%/50%) plasma at 40 mTorr, 500 W, for 3 min followed by HCl solution dipping. Figure 99 (b) shows the picture of the same Cu film prepared with the same plasma condition except with the 70% overexposure time (i.e., 5.1 min). Both photos show much smaller attack of the cusp region, compared with the Fig. 98 sample that was exposed to the Cl_2 plasma under the same pressure and power. The improvement can be attributed to the high ion bombardment energy and large Cu to $CuCl_x$ conversion rate in the direction perpendicular to the substrate surface. For example, the cathode self bias voltage ($-V_{dc}$) of the Cl_2 plasma was 173 V and that of the Cl_2/Ar (50%/50%) was 225 V. Since the ion bombardment direction is perpendicular to the substrate surface, the large $-V_{dc}$ favors the vertical reaction rate more than the lateral reaction rate.[272-273] The time required to completely convert the Cu film into $CuCl_x$ in the vertical direction is greatly shortened with the combination of the high ion bombardment

energy and the high Cl radical concentration. This leaves less time for the lateral reaction and therefore, the attack of the cusp region. However, since the Fig. 99 (b) sample was exposed to the plasma for a much longer time than that in the Fig. 99 (a) sample, the attack of the cusp region in the former is more serious than in the latter. Also, the edge of the Fig. 99 (b) pattern is rougher than that of Fig. 99 (a), which was due to the undercut of the photoresist pattern. The details will be discussed later in a separate section.

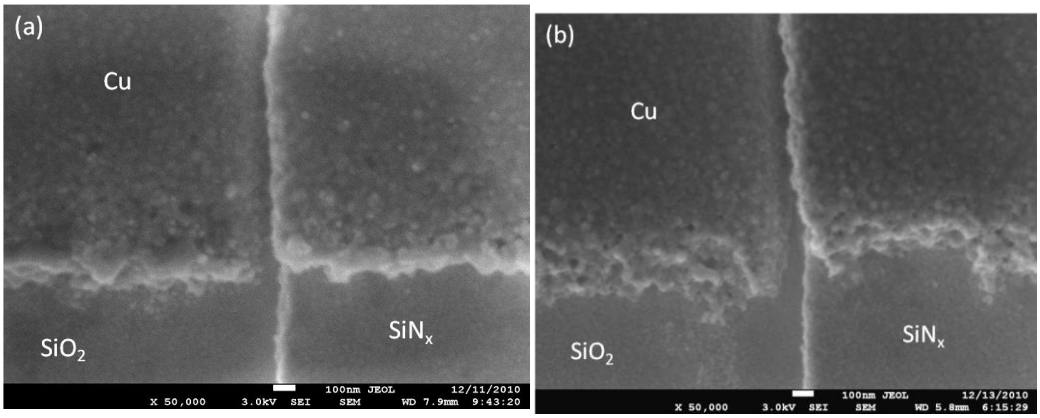

Figure 99. Top views of Cu line over the 150 nm SiN_x step after Cl_2/Ar (50%/50%) plasma exposure for (a) 3 min, and (b) 5.1 min (70% over exposure time) followed by $CuCl_x$ removal. Plasma condition: 500 W, 40 mTorr, 20 sccm.

8.4.2 N_2 Additive Effect

It was reported that in a plasma process the magnitude of the $-V_{dc}$ increased with the increase of the bond energy of the feed gas molecule.[274] Since the N≡N bond energy

is larger than that of the Cl-Cl bond, i.e., 9.8 vs. 2.5 eV,[275] the $-V_{dc}$ of the Cl_2 plasma increased with the addition of N_2.[264,275] In this study, authors observed that the $-V_{dc}$ of the Cl_2 plasma with the total gas flow rate of 20 sccm at 40 mTorr, 500 W was 173 V, which was increased to 223 V when the feed gas composition was changed to Cl_2/N_2 (50%/50%). Separately, N_2 can serve as a diluent in the Cl_2 plasma to reduce the Cl radical concentration.[276] For example, under the same total gas flow rate of 20 sccm, 40 mTorr, and 500 W, the Cl radical (at 837 nm wavelength) concentration in the Cl_2 plasma was 100 (A.U.), which was reduced to 38 (A.U.) in the Cl_2/N_2 (50%/50%) plasma. Since the Cu to $CuCl_x$ conversion rate in the Cl_2/N_2 (50%/50%) plasma was higher than that in the pure Cl_2 plasma, i.e., 830 vs. 500 Å/min, the Cu conversion rate is more influenced by the ion bombardment energy than the Cl concentration. Another factor that affected the Cu to $CuCl_x$ conversion rate was the porosity of the reaction product, which was formed on top of the unreacted Cu layer. Since $CuCl_x$ formed from the Cl_2/N_2 plasma is more porous than that formed from the Cl_2 plasma, it is easier to diffuse Cl through the former than the latter to reach and to react with the fresh Cu.[264]

Figure 100 (a) shows the top view of the edge of a Cu film over the SiN_x step after being exposed to the Cl_2/N_2 (50%/50%) plasma at 40 mTorr, 500 W, for 3 min followed with HCl solution dipping. Figure 100 (b) shows the photo of the same Cu film prepared with the same plasma condition, except with the 70% overexposure time (i.e., 5.1 min). Compared with the Cl_2 plasma exposed Cu film in Fig. 98, the Fig. 100 samples have much smaller attack of the cusp region and smoother Cu edge. The smaller attack of the cusp region in the Cl_2/N_2 (50%/50%) plasma can be attributed to the high

vertical-direction Cu conversion rate and the low Cl radical concentration. In addition, it was reported that a CuN_x layer was formed on the Cl_2/N_2 plasma exposed surface.[264] The same CuN_x layer was probably formed on the sidewall instead of the horizontal surface of Cu because high ion bombardment energy is unfavorable for the formation of Cu-N bonds.[277] This kind of sidewall layer could reduce the lateral chlorination rate and therefore, minimize the excessive attack of the cusp region. However, since the Fig. 100 (b) sample was exposed to the plasma for a much longer time than that of the Fig. 100 (a) sample, i.e., 5.1 min vs. 3 min, the rougher pattern edge of the former may be due to the time effect. However, a more detailed study is required to verify this.

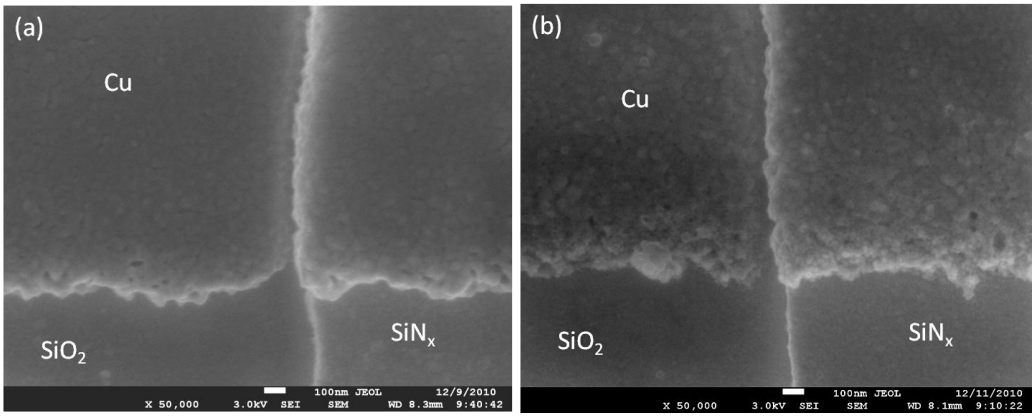

Figure 100. Top views of Cu film over the 150 nm SiN_x step after Cl_2/N_2 (50%/50%) plasma exposure for (a) 3 min and (b) 5.1 min (70% over exposure time) followed by $CuCl_x$ removal. Plasma condition: 500W, 40 mTorr, 20 sccm.

8.4.3 CF_4 Additive Effect

The addition of CF_4 into the Cl_2 plasma also increased the ion bombardment energy. For example, under the same 40 mTorr, 500 W and 20 sccm total gas flow rate condition, the $-V_{dc}$ of the Cl_2/CF_4 (50%/50%) plasma is larger than that of the Cl_2 plasma, i.e., 252 V vs. 173 V. Similar to the N_2 additive gas case, the increase of $-V_{dc}$ can be attributed to the larger C-F bond energy in CF_4 compared with that of the Cl-Cl bond in Cl_2, i.e., 5.7 vs. 2.5 eV.[264,276] The addition of CF_4 into the Cl_2 plasma also increased the Cl concentration in the plasma phase probably through the following reaction.[278]

$$Cl_2+CF_2 \rightarrow CClF_2+Cl \qquad [32]$$

The Cl radical (at 837 nm wavelength) concentration in the Cl_2/CF_4 (50%/50%) plasma is higher than that in the Cl_2 plasma, e.g., 157 (A.U.) vs. 100 (A.U.). The Cu to $CuCl_x$ conversion rate in the former was much higher than that in the latter, i.e., 1,250 vs. 500 Å/min. This result is similar to the Cl_2/Ar (50%/50%) plasma exposure case.

Figure 101 (a) shows the top view of the edge of a Cu film over the SiN_x step after being exposed to the Cl_2/CF_4 (50%/50%) plasma at 20 sccm, 40 mTorr, 500 W for 2 min followed by the HCl solution dipping. Figure 101 (b) is the picture of the same Cu film prepared from the same plasma exposure condition except with 70% overexposure time (i.e., 3.4 min). In both cases, the excessive attack of the cusp region is not observed. The ion bombardment energy of the Cl_2/CF_4 (50%/50%) plasma, i.e., $-V_{dc}$ = 252 V, was larger than those of the pure Cl_2, Cl_2/Ar (50%/50%), and Cl_2/N_2 (50%/50%) plasma, i.e.,

173 V, 225 V, 223 V, respectively. Therefore, the Cu film was totally consumed by the former plasma in a shorter time than those in the latter plasma. The shorter plasma exposure time reduced the attack of the cusp region. Separately, it was reported that the Cl_2/CF_4 plasma formed a CuF, CuF_2 or fluorocarbon containing layer on the Cu surface.[264,268,269] When this kind of film is formed on the sidewall, it could reduce the Cu to $CuCl_x$ conversion rate in the lateral direction.

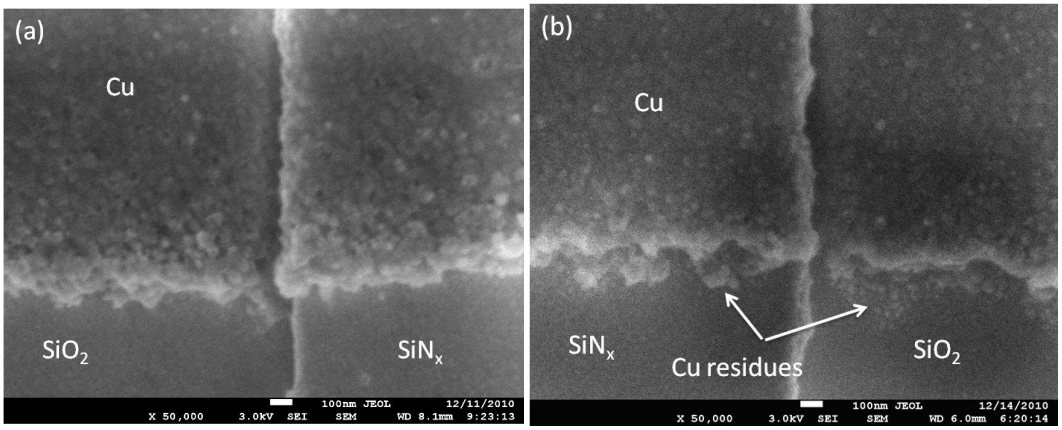

Figure 101. Top views of Cu line over the 150 nm SiN_x step after Cl_2/CF_4 (50%/ 50%) plasma exposure for (a) 2 min and (b) 3.4 min (70% over exposure time) followed by $CuCl_x$ removal. Plasma condition: 500 W, 40 mTorr, 20 sccm.

The lateral chlorination of Cu proceeds with the plasma exposure time. Therefore, if the lateral Cu to $CuCl_x$ conversion rate is large, the undercut of the photoresist pattern can be detected. The length of the undercut increases with the plasma exposure time.

Since there is lack of ion bombardment under the photoresist covered area, the Cu chlorination reaction in this region will be different from that of the uncovered region. In addition, the film at the interface with the underneath SiN_x layer will have a lower reaction rate than that in the bulk film because of the difference in the local material structures or compositions.[279] Therefore, without ion bombardment, Cu residues could be left in the photoresist covered area, i.e., along the edge of the pattern, as shown in Figure 102. The residue along the pattern edge of the Cl_2/CF_4 (50%/50%) plasma overexposed sample was Cu, which was confirmed with the EDS analysis. The residue left from the Cl_2/CF_4 plasma process was more serious than that from the Cl_2 and Cl_2/N_2 plasma processes. The former contains a higher Cl radical concentration than the latter, which causes the larger undercut of the photoresist pattern.

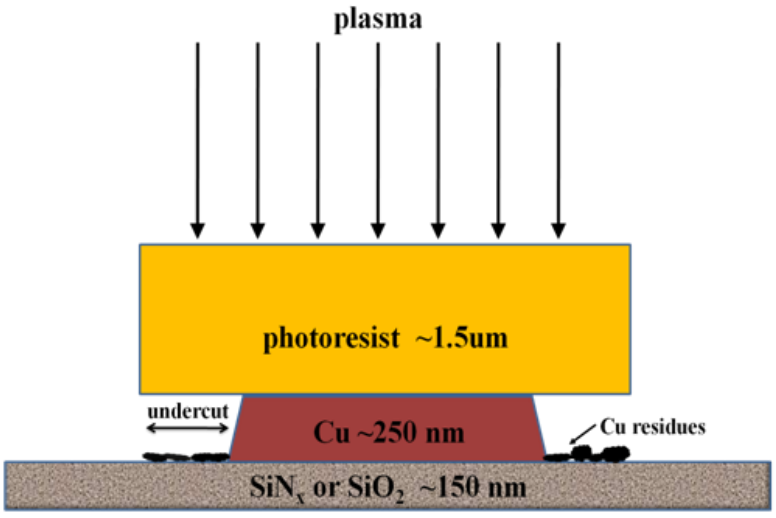

Figure 102. An illustration for the undercut of the photoresist pattern and the formation of the Cu residues.

8.5 Plasma Over Exposure Time Effect on Cusp Attack

Figure 103 (a), (b), and (c) show the top view of the Cu layer over the SiN_x step after being exposed to the pure Cl_2 plasma with over exposure time of 0%, 70%, and 100%, respectively. It is clear that the excessive attack of the cusp region is strongly related to the over exposure time. In addition, Cu at the bottom of the step, i.e., on the SiO_2 surface, was more excessively consumed than that at the top of the step, i.e., on the SiN_x surface. The uneven attack of Cu near the step can be explained by the local stress and the nonuniform original film thickness. For example, the Cu film on the sidewall of the step, i.e., the vertical direction (d_v), is larger than that in the horizontal direction (d_h), as shown in Figure 104 (a). For the non-photoresist covered area, during the Cl_2 plasma exposure, it takes longer time for the Cu film on the side of the SiN_x step to be totally converted to $CuCl_x$ than the bottom portion because the ion bombardment direction is perpendicular to the substrate surface. In addition, due to the high local stress, the Cu conversion rate at the cusp region is much faster than that of the flat surface away from the cusp region. Therefore, Cu in the cusp region can be totally converted to $CuCl_x$ and the reaction proceeds laterally along the bottom edge of the SiN_x step under the photoresist covered area. At the same time, part of the Cu film not covered by the photoresist and away from the cusp region remains unconverted, as shown in Fig. 104 (b). Fig. 104 (c) shows that the Cu film in the cusp region but covered by the photoresist pattern is excessively consumed by the lateral chlorination reaction process. The excessive consumption of Cu in the cusp and the non-cusp regions underneath the photoresist pattern, i.e., the undercut of the photoresist pattern, are shown as d_{u1} and d_{u2},

respectively in Fig. 104 (c). Fig. 104 (d) shows the final profile of the Cu film over the SiN_x step after the removal of photoresist. Since the Cu film on the bottom portion of the cusp region is more attacked by the lateral chlorination reaction than the Cu film on the top of the SiN_x step is, the width of the bottom Cu consumed area (w_b) is larger than that of the top area (w_s), as shown in Fig. 104 (d). Therefore, the area loss in the cusp region, which is expressed as a triangular shape in Fig. 103 (a), is more contributed by the loss of the Cu film on the bottom of the step than that on the top of the step.

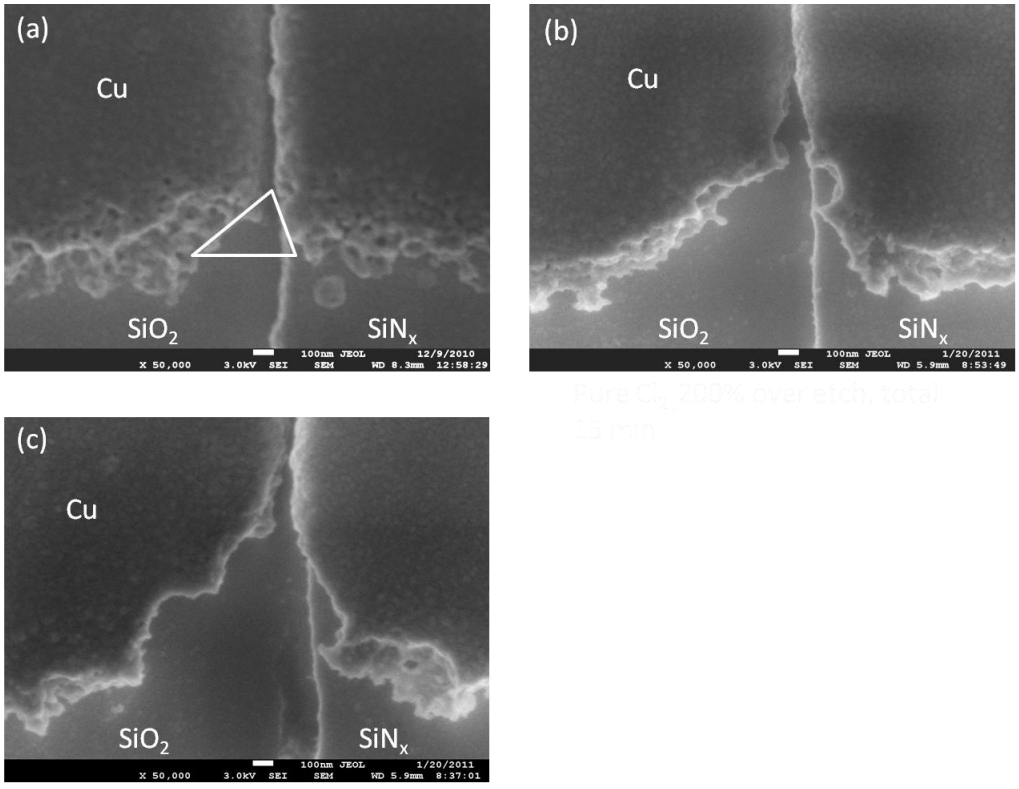

Figure 103. Top views of Cu layer over the 150 nm SiN_x step after Cl_2 plasma exposure for (a) 0%, (b) 70%, and (c) 100% over exposure times followed by $CuCl_x$ removal. Plasma condition: 500 W, 40 mTorr and 20 sccm.

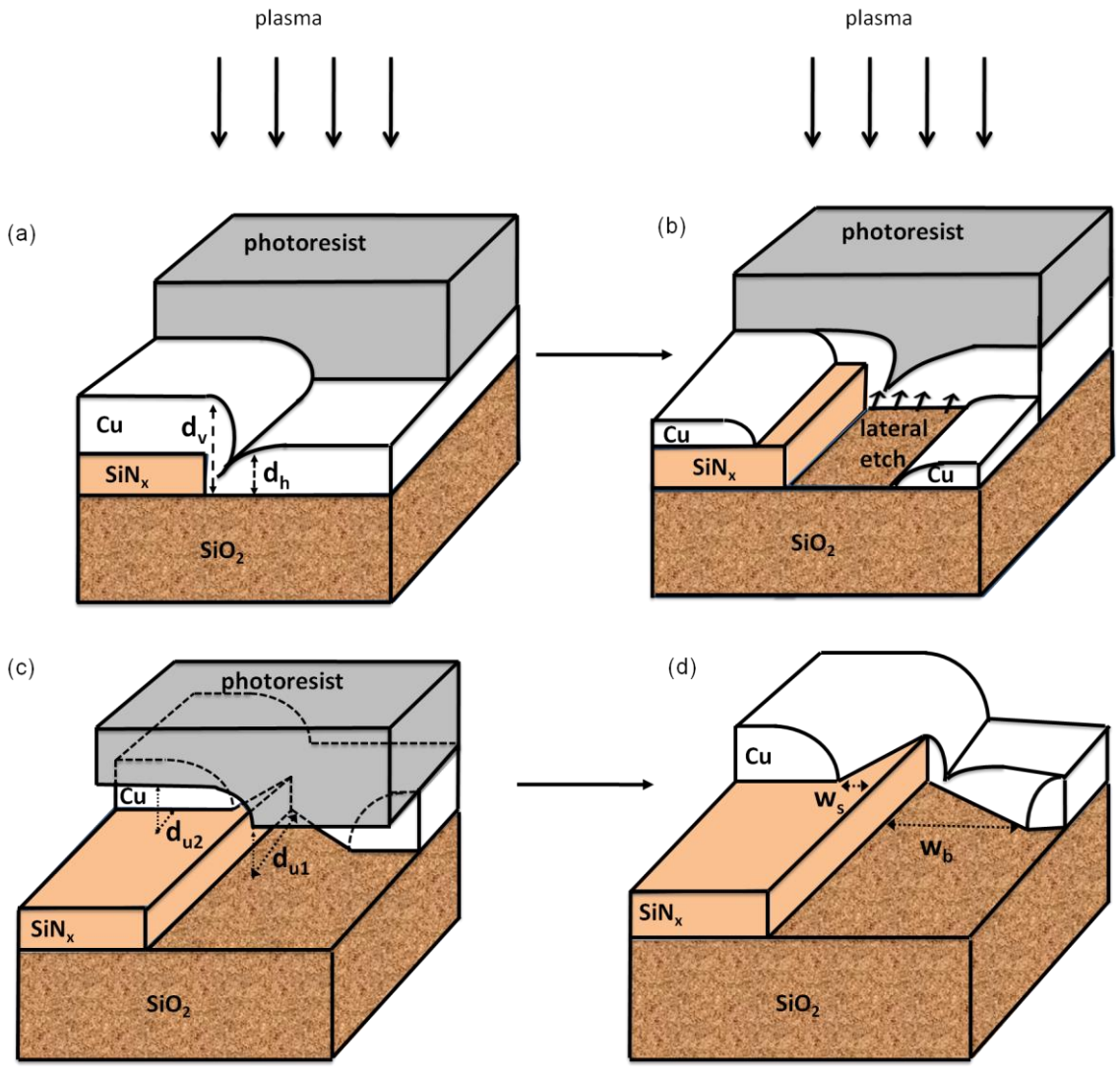

Figure 104. An illustration for the Cu pattern change at different plasma exposure times (with subsequent of the $CuCl_x$): (a) at beginning, (b) part of the convertion of Cu in the uncovered region, (c) totally complete conversion of Cu in the uncovered region, and (d) after removal of photoresist layer.

Both the lack of a sidewall protection layer formation in the Cl_2 plasma and the high Cl concentration cause the high lateral-direction Cu conversion reaction rate. Figure 105 shows d_{u1} and d_{u2} vs. the Cl_2 plasma over exposure time. Both d_{u1} and d_{u2} increased linearly with the plasma exposure time, i.e., at the rate of 0.21 μm/min and 0.12 μm/min, respectively. The d_{u1} value is larger than the d_{u2} value because the internal stress at the cusp region is larger than that at the flat area.[129] The high film stress facilitates the Cu to $CuCl_x$ conversion rate.[264] In addition, the linearity of the two curves in Fig. 105 indicates that there was plenty of Cl radical supply underneath the photoresist covered area, i.e., this is a reaction-controlled not the reactant supply-controlled process.

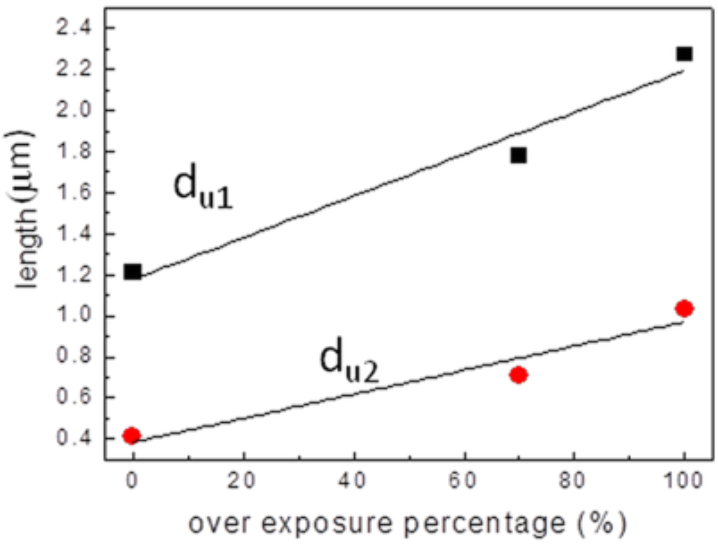

Figure 105. Lengths of the loss of the cusp region (d_{u1}) and the non-cusp region (d_{u2}) of the Cu pattern vs. the Cl_2 plasma over exposure time.

8.6 SiN_x Step Profile Effect on Cusp Attack

The size of the area loss of the cusp region, as shown in the triangular area of Fig. 103 (a), is related to the slope of the SiN_x step. Figure 106 (a) shows the cross-sectional view of a very slope SiN_x step, e.g., 20^o, prepared from a 0.5% HF/99.5% DI wet solution etch process. This kind of slope was formed because the solution attacked the SiN_x/photoresist interface while dissolving the SiN_x film. Figure 106 (b) shows the top view of the edge of an etched Cu line over the 20^o sloped SiN_x step. The plasma exposure condition was Cl_2 at 40 mTorr, 500 W, and 20 sccm flow rate with 70% overexposure time. The Cu film deposited on the small angle SiN_x step shows negligible cusp formation, i.e., uniform Cu film thickness and stress distribution. Therefore, no excessive attack was observed near the bottom of the step, which is very different from the Fig. 98 case.

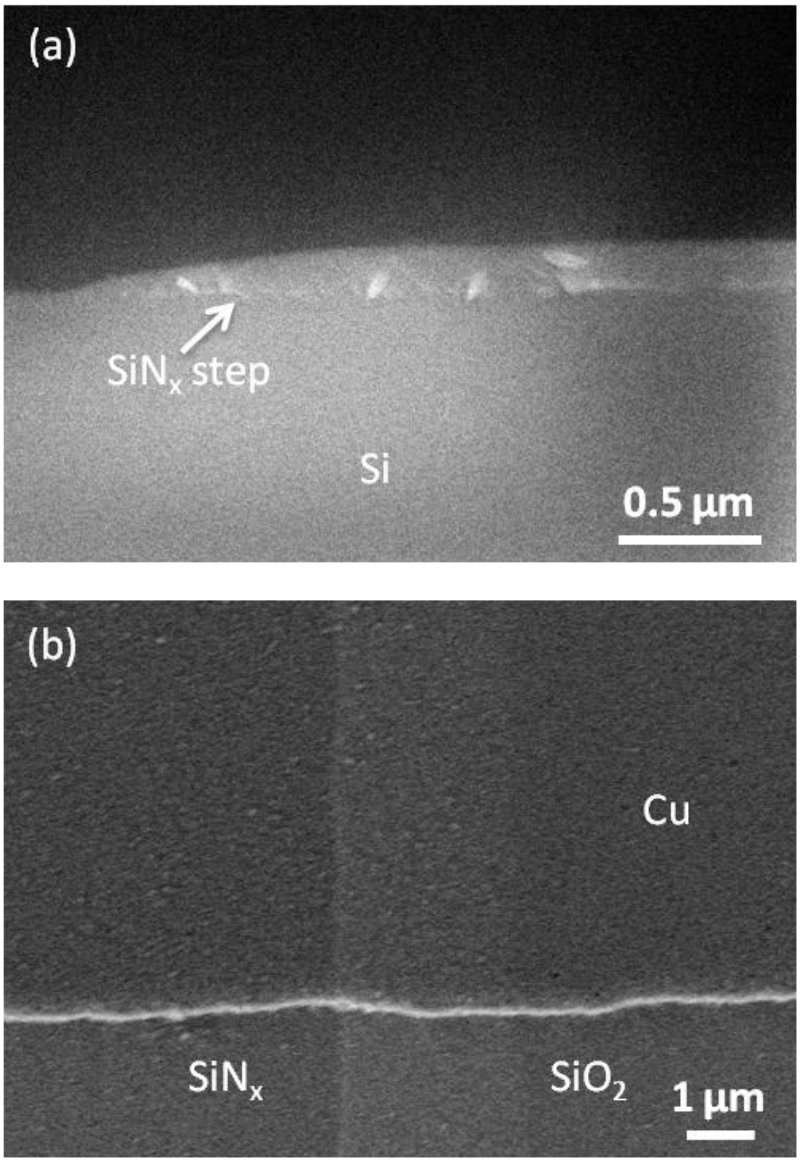

Figure 106. (a) Cross-sectional SEM micrograph of the small angle SiN_x step etched by 0.5% HF/99.5% DI wet solution etch process, and (b) top view of Cu layer over the SiN_x step after Cl_2 plasma exposure with 70% over exposure time (8.5 min) followed by $CuCl_x$ removal. Plasma condition: 500 W, 40 mTorr, and 20 sccm.

8.7 Two-Step RIE Process for Optimized Cu Line Etch

For practical applications, the Cu film is usually deposited over a near-vertical step. It is necessary to have an etch process that does not attack the film excessively near the cusp region and to have minimum undercut of the photoresist pattern. A two-step plasma exposure process has been developed to achieve this goal. For example, the first plasma exposure step that provides a large Cu conversion rate with minimum attack of the cusp region can be used to convert a large portion of the Cu film to $CuCl_x$. Then a second plasma exposure step that forms very little residue along the pattern edge can be applied to convert the rest of the Cu film into $CuCl_x$. Based on the result of the previous sections, the Cl_2/CF_4 (50%/50%) plasma at 40 mTorr, 500 W, 20 sccm, and 2 min was found to be proper for the first step. The Cl_2/N_2 (50%/50%) at 40 mTorr, 500 W, 20 sccm, and 1.4 min was adequate for the second step. Figure 107 shows the top view of a 250 nm thick Cu pattern over a 150 nm thick near-vertical SiN_x step prepared with this two-step process. No excessive cusp attack or residue was observed along the edge.

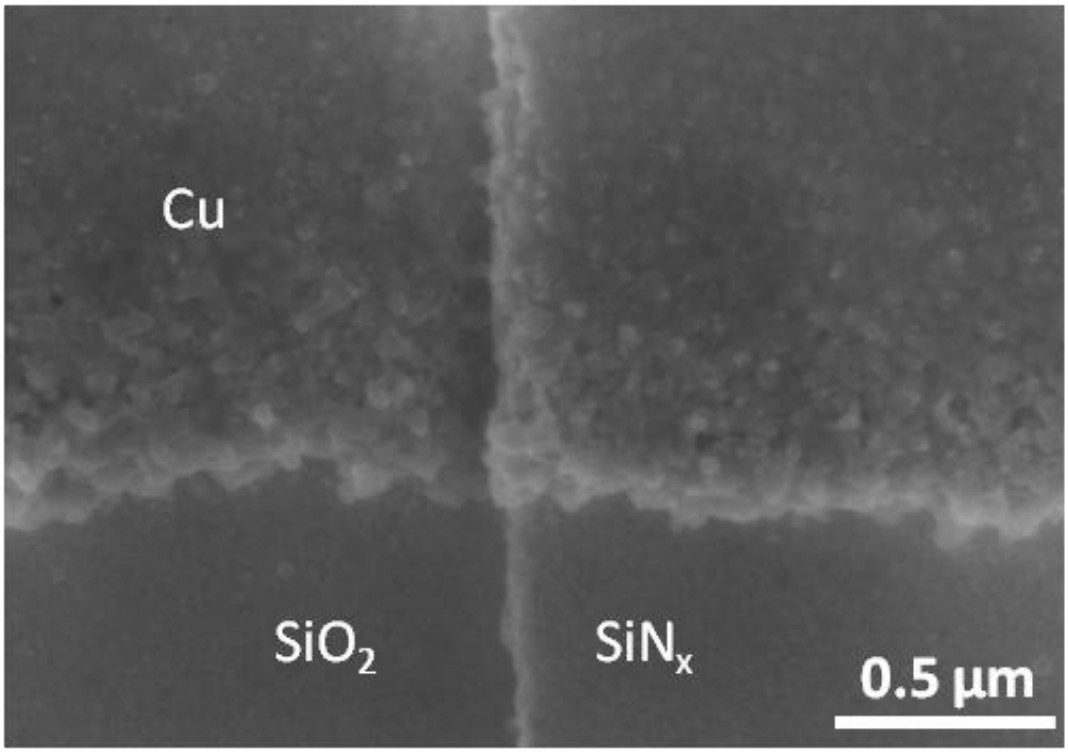

Figure 107. Top view of etched Cu over the 150 nm SiN_x step with the two-step plasma exposure process: first, Cl_2/CF_4 (50%/50%) plasma for 2 min, second Cl_2/N_2 (50%/50%) plasma for 1.4 min followed by $CuCl_x$ removal. Plasma condition: 500 W, 40 mTorr, 20 sccm.

8.8 Summary

The additive gas effect on the etch of the Cu film over a dielectric step using a new plasma-based process has been investigated. Excessive attack of the cusp region and the edge roughness were observed after the pure Cl_2 plasma exposure process. The attack of the cusp region was reduced in the Cl_2/Ar (50%/50%) plasma because the high ion bombardment energy facilitated the vertical-direction Cu conversion, which left little

time for the lateral Cu-Cl reaction underneath the photoresist covered area. In the Cl_2/N_2 (50%/50%) plasma exposure process, the attack of the cusp region and the edge roughness were also reduced due to high ion bombardment energy, low Cl radical concentration, and the possible formation of a CuN_x sidewall layer. In the Cl_2/CF_4 (50%/50%) plasma exposure process, no excessive attack of the cusp region was observed due to the high ion bombardment energy and the possible formation of a fluorine-containing sidewall protection layer. However, the Cu residue along the pattern edge was observed in the Cl_2/CF_4 (50%/50%) plasma with the 70% overexposure time condition due to the lack of ion bombardment underneath the photoresist covered area. For the Cl_2 plasma exposure case, the excessive attack of the cusp region is strongly dependent on the over exposure time. However, the cusp attack was negligible when the Cu film was deposited over a very slope SiN_x step. A two-step RIE process, which has minimum attack of the cusp region with negligible residue left, has been developed. In summary, the Cu film on a topographic surface can be etched into fine lines with good configuration, such as no "neck" in the cusp region, smooth edge, and no residue, using the new plasma-based etch process.

CHAPTER IX

SUMMARY AND CONCLUSION

This dissertation introduced the memory function of the nc-CdSe and nc-MoO_3 embedded ZrHfO nonvolatile memory devices. The thin films were all deposited by the RF magnetron sputtering in an one pumpdown process. Both NVM devices show great charge trapping and retention capabilities. Moreover, the temperature effect has been investigated on the nc-MoO_3 embedded ZrHfO memory device. Within the same structure but under different operating gate voltages, i.e., $|V_g| > |V_{BD}|$, the warm white light can be emitted from this kind of device after the dielectric breakdown. Therefore, this device can also be called the solid state incandescent light emitting device (SSI-LED). This new SSI-LED resolves the difficulties in the current LED market since the white light can be emitted from a single-chip device with the very good reliability and long lifetime feature. The light emission characteristics have been thoroughly studied with different fabrication parameters such as deposition time, annealing temperature, and high-k stack structure. In the end, the plasma-based Cu dry etch technique was reviewed and the step effect of the Cu film deposited over a near-verticle step was analyzed. The minimized cusp attack was achieved by using the two-step RIE proces. This two-step RIE process has been sucessfully utilized in the fabrication of the new LED driving matrix.

The nc-CdSe embedded ZrHfO high-k memory devices have been fabricated and investigated for the material properties and memory functions. The formation of the

discrete nc-CdSe dots in the amorphous ZrHfO film on top of an interface layer is confirmed by the TEM micrpgraph. The nc-CdSe/ZrHfO interface structure is different from that of the bulk CdSe or ZrHfO, which can be related to the charge trapping and retaining mechanisms. The nc-CdSe embedded sample can trap much more charges than the control sample, i.e., by 20 times. Both holes and electrons can be trapped to the nc-CdSe site depending on the polarity of the applied gate voltage. More holes than electrons can be trapped to the nc-CdSe embedded sample. Charges are stored to the nc-CdSe site in two states: loosely trapped at the nc-CdSe/ZrHfO interface or strongly trapped to the bulk nc-CdSe. Electrons trapped in the nc-CdSe embedded sample cause the Coulomb blockade effect. The embedding of nc-CdSe into the high-k film induces a larger leakage current because of the creation of excessive defects. Charges can be retained at the nc-CdSe site even after the breakdown of the high-k stack. More than 56% of the originally trapped holes remain in the device after 10 years.

Temperature effects on the charge transfer mechanism and the storage capacity of the nc-MoO_3 embedded high-k dielectric capacitor have been investigated. The high temperature suppressed the Coulomb blockade effect and caused the higher leakage current due to the larger thermal energy of the trapped holes and the higher conductivity of the high-k film. The P-F emission mechanism dominates the conduction mechanism because the charge trapping energy is lower than the barrier heights at the Si/$HfSiO_x$ and Al/ZrHfO interfaces. The deterioration of the Si/ZrHfO interface at the high temperature was caused by the high charge transfer rate. About 43% of the trapped charges were retained after 10 years at 25^{o}C. However, the charge retention capability decreased with

the increase of temperature. The memory functions and the lifetime of the nc-MoO_3 embedded ZrHfO capacitor are dependent on the temperature because of the change of the hole trapping and detrapping mechanisms.

Light emission from the amorphous ZrHfO high-k stack on the p-type Si wafer under the gate bias condition has been studied. The broad band light including the visible and near IR wavelengths was thermally excited from many small conductive paths formed after the dielectric breakdown. The light intensity is affected by the thickness of the high-k stack as well as the polarity and the magnitude of V_g. Light generation is due to the thermal excitation mechanism which is different from the electron-hole or exciton recombination mechanism in conventional p-n junction or QW LEDs. The similar warm white light was emitted from the nc-CdSe embedded ZrHfO dielectric stack. The inclusion of the nc-CdSe layer in the ZrHfO film induces larger leakage current compared to its control sample, which causes the higher intensity of the emitted light and EQE. The light intensity of the nc-CdSe SSI-LED also increases with the increase of the $|V_g|$. Very high CRI, i.e., 98.4, can be obtained from this new SSI-LED. The surface of the high-k layer is smooth prior to the light emission for both samples. After the dielectric breakdown, the bumps and holes were formed on the surface of the ZrHfO layer in both samples due to the high leakage current passing through the conductive paths. Moreover, the PDA temperature changes the material and electrical characteristics of both the bulk and the interface layers. Therefore, the light characters will be affected. The high temperature annealed sample has a larger leakage current than the low temperature annealed sample, which causes the brighter light emission in the former.

For the same reason, the light intensity increases with the increase of the $|V_g|$. A new driving matrix has been proposed to prevent the block of the light and improve the driving ability. Overall, this new single-chip, long lifetime SSI-LED is easy to fabricate using the IC compatible process and can be applied to a wide range of products.

Besides the ZrHfO thin film, the WO_3 thin film has been investigated as the light emission layer. After the dielectric breakdown, the broad band light in the visible wavelength range was also emitted from many small bright dots based on the same thermal excitation principle. The light intensity increased with the increase of the magnitude of the applied voltage or the duty cycle in the pulsed driving condition. However, the light characteristics, such as the wavelength range and CRIs, are little affected by these factors. This new LED has a long lifetime due to the unique structure of embedding the conductive paths in the high quality dielectric film.

The additive gas effect on the etch of the Cu film over a dielectric step using a plasma-based process has been investigated. Excessive attack of the cusp region and the was observed after the pure Cl_2 plasma exposure process. The attack of the cusp region was reduced in the Cl_2/Ar (50%/50%), Cl_2/N_2 (50%/50%) plasma exposure process due to the adjustment of the ion bombardment energy and Cl radical concentration. In the Cl_2/CF_4 (50%/50%) plasma exposure process, no excessive attack of the cusp region was observed. However, the Cu residue along the pattern edge was observed in the Cl_2/CF_4 (50%/50%) plasma with the 70% overexposure time condition due to the lack of ion bombardment underneath the photoresist covered area. A two-step RIE process, which has minimum attack of the cusp region with negligible residue left.

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