DYNAMIC MODELING FOR DESIGN AND ANALYSIS OF MEMRISTIVE AND STATIC RANDOM ACCESS MEMORIES

A Dissertation

by

YENPO HO

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Chair of Committee,	Garng M. Huang
Committee Members,	Peng Li
	Jose Silva-Martinez
	Guergana Petrova
Head of Department,	Chanan Singh

August 2014

Major Subject: Electrical Engineering

Copyright 2014 Yenpo Ho

ABSTRACT

Nowadays, the trend of modern memory technology is going towards the following directions: (1) look for new nonvolatile devices; (2) keep scaling down the existing volatile devices. Although nonvolatile devices enable to switch off its power supply to further suppress standby power, the down sides are the low switching speed and the complicated dynamic cell characteristics. On the other hand, researchers are looking to scale down SRAM since it is the most reliable and fast. However, the SRAM suffers read and write failure due to lack of good stability optimizing metric. To tackle the above mentioned problems, this work first introduces a promising nonvolatile device called Memristor, which is said to be possible to replace our memory devices now. By starting from basic memristor device equations, this work aims to develop a comprehensive set of properties and design equations for memristor based memory. The introduced schemes are specifically targeting key device properties relevant to memory operations. Using the discovered properties, a simple design of read/write circuits is investigated. In the second part of this work, SRAM stability analysis is focused. SRAM verification and stability analysis has become an essential task to investigate soft-errors. This work aims to extend the SNM to a new era. Based on the introduced Region-Analysis in this work, SRAM stability can be explained using bifurcation theory, and closed form expression can be derived. The derived expression provides physical characterization of SRAM noise tolerance property; thus has potential to provide needed design insights. Overall, dynamics of memristor and SRAM are strongly emphasized.

The derived memristor properties reveals that the memristor state change requires some time; it indicates that the memristor-based memory needs some “critical time” to flip the logic. Similarly to the SRAM, the SRAM write operation not only needs the injected current over a “critical current” but also need to maintain for some “critical time”. In short, both memristor-based memory and SRAM show the timely manner for read/write operation. Furthermore, the developed analytical formulae are able to reveal the dynamic aspect on memory read/write operations which address the key concern for modern memory technology.

DEDICATION

To my lovely father (Jii-Chung Ho) and mother (Li-Li Hu)

and in memory of my grandparents.

ACKNOWLEDGEMENTS

First of all, my appreciation goes to my advisor, Dr. Garng M. Huang, for his long-time support and guidance throughout my graduate study. Doctor Huang is always being a role model as a brilliant scientist with rigorous scientific attitude and wisdom, inspiring and encouraging to his students. He not only has taught me technical knowledge for my research work but also the vision to explore new areas for my future professional development. I am truly grateful to him for letting me involve in this interesting project.

I am greatly indebted to Dr. Peng Li. The work presented in this dissertation would not have been done without his support. His advice and guidance are vital to my PhD research. I am heartily thankful to him for sharing his thoughts and giving me helpful suggestions.

In addition, I would like to thank Dr. José Silva-Martínez and Dr. Guergana Petrova for serving on my committee. Thanks also go to my friends: Wenzong Wang, Hangtian Lei, Tian Lan, Li-Wei Tseng, Saeed Samadi, Ting-Xuan Chen and Hung-Yi Liao (Coze). Their friendship makes my time at Texas A&M University a joyful experience. Furthermore, I also want to thank Kai Jiang, Chenyan Guo, Kaigui Xie, Rui Ma and Jun An (Visiting professor) for being as my mentor provide advice toward the success of research path. They made my years at College Station a memorial one.

TABLE OF CONTENTS

Page

ABSTRACT ii

DEDICATION iv

ACKNOWLEDGEMENTS v

TABLE OF CONTENTS vi

LIST OF FIGURES viii

LIST OF TABLES xii

CHAPTER I INTRODUCTION 1

1.1. Literature Review 1
1.2. Research Contribution in This Work 3
1.3. Dissertation Organization 4

CHAPTER II REALIZATION OF MEMRISTOR DEVICES 7

2.1. The Memristor Theory Background 7
2.2. The Memristor Device Models 8

CHAPTER III DYNAMIC BEHAVIOR OF MEMRISTOR DEVICE AND ITS PROPERTIES FOR MEMORY USE 13

3.1. Characterize the Fundamental Memristor Device 14
3.2. Define Logic Regions 29
3.3. Memory Cell Read/Write Operations 30
3.4. Memristor Memory Array and Peripheral Circuitry 37

CHAPTER IV BACKGROUND ON THE STATIC RANDOM ACCESS MEMORY 41

4.1. How Does SRAM Work? 41
4.2. Traditional Static Noise Margin 45

Page

CHAPTER V THE DYNAMIC MODEL FOR SRAM CELL 48

5.1. The MOSFET Transistor Model 48
5.2. The Dynamic Model for SRAM 52

CHAPTER VI SRAM STABILITY AND ITS MATHEMATICAL EQUIVALENCE 56

6.1. Voltage Transfer Curves (VTCs) 57
6.2. The SRAM Equilibrium Points 58
6.3. Stability Boundary of an SRAM 58
6.4. Noise Induced Bifurcation and SRAM Instability Study 66

CHAPTER VII THE ANALYTICAL SOLUTION FOR STATIC NOISE MARGIN VIA THE CONCEPT OF CRITICAL CURRENT 76

7.1. The Point of Instability for an SRAM 77
7.2. The Region Analysis 78
7.3. The Analytical Solution for Critical Current 84
7.4. Static Noise Margin Metric in Current Representation 92
7.5. The Analytical Solution for Read/Write Margins in Current Representation 95

CHAPTER VIII THE ANALYTICAL SOLUTION FOR DYNAMIC NOISE MARGIN VIA THE CONCEPT OF CRITICAL TIME 97

8.1. The Definition of Dynamic Noise Margin (DNM) 98
8.2. The SRAM Cell Dynamics and Analytical Solution for Dynamic Noise Margin 100

CHAPTER IX SUMMARY 110

9.1. Summary and Contributions 110
9.2. Future Works 114
9.3. Acknowledgement 116

REFERENCES 117

APPENDIX A THE RELATION OF CRITICAL CURRENT AND CRITIAL VOLTAGE 128

LIST OF FIGURES

FIGURE		Page
2.1	Four fundamental circuit elements: Resistance ($dv=R{\cdot}di$), capacitance ($dq=C{\cdot}dv$), inductance ($d\varphi=L{\cdot}di$), and memristance ($d\varphi=M{\cdot}dq$) which is the missing link that Chua argued.	7
2.2	(a) Memristor device structure; (b) equivalent circuit model and (c) symbol for memristor.	9
3.1	A memristor biased using current source I_{in}.	15
3.2	A square-waveform current source I_{in} has amplitude I_A and $-I_A$ with equal width Δt (a) causes the memristor state (b) transition from w_0 to w_3.	19
3.3	A memristor biased using voltage source V_{in}.	19
3.4	A voltage divider consisting of a constant resistor R_x in series with a flux-controlled memristor $M(\varphi)$.	25
3.5	The window function vs. w/D plot.	29
3.6	Memristor output levels. (a) The output low margin is at 0.4 and output high margin is at 0.6 in linear drift model; (b) output levels in nonlinear drift model.	30
3.7	Write signals (bottom) and corresponding memristor states (top).	31
3.8	Write operation structure.	33
3.9	Write pulses (top) and corresponding memristor states (bottom).	33
3.10	(a) Operation stages; (b) read pattern.	36
3.11	Read operation (logic zero case).	39
3.12	Read operation (logic one case).	39
3.13	Proposed memristor-based memory array structure.	40

FIGURE Page

4.1 A 6-T SRAM cell. 41

4.2 A simplified graphical representation of 6-T SRAM cell. 42

4.3 (a) Noise injection during a read operation, and (b) its equivalent model. 42

4.4 (a) Noise injection during a write operation, and (b) its equivalent model. 43

4.5 An SRAM state flip caused by (a) a current going away; (b) a current injection in standby mode. 45

4.6 (a) characterization of the traditional SNMs, (b) SNM in standby, (c) SNM in write. 47

5.1 The plot of smooth version of S(x) with A=100 (Left) and A=50 (Right) 52

5.2 The SRAM cell with internal lumped capacitors drawn. 53

5.3 The SRAM cell with cross-coupled voltage sources inserted. 54

6.1 An example of voltage transfer curves on a 65nm technology SRAM 57

6.2 Example of phase portrait for an SRAM. 61

6.3 Separatrix of a 65nm SRAM cell 64

6.4 The plot of separatrix varying only V_{th} values when n is (a) 60; (b) 80 65

6.5 The plot of separatrix varying only K values when n is (a) 20; (b) 40; (c) 60; (d) 80. 66

6.6 The plot of separatrix varying V_{th} and K values at n=70. 67

6.7 The SRAM topology with voltage and current noise sources incorporated (simplified view). 69

FIGURE Page

6.8 Illustration of saddle node bifurcation. The voltage transfer curves when (a) V_N is zero; (b) V_N is 0.15 volt; (c) V_N=0.29 volt; (c) V_N=0.35 volt. 70

6.9 (a) Illustration of saddle node bifurcation as I_{n2} increases from zero to 200uA, (b) SRAM Butterfly curve when I_{n2}=150uA, (c) SRAM Butterfly curve when I_{n2}=192uA, (d) SRAM Butterfly curve when I_{n2}=200uA. 75

7.1 (a) Symbol for two cross-coupled inverters where functions f and g are for the top and bottom inverter; (b) Phase portrait plot showing two transfer curves tangent at bifurcation have the slope indicated.......... 78

7.2 The nullclines and region formation of an SRAM. The V_{1B-2D} is all the possible range for V_1 to have bifurcation in Region 2D. [C= Cutoff; L= Linear; S= Saturation.] 80

7.3 (a) An example of assigned regions for an SRAM; (b) the assigned regions when V_{dd} is reduced. 81

7.4 The phase portrait for (a) parameter set#1 and (b) parameter set#2. 82

7.5 (a) The plot of SRAM equilibrium points as I_{n2} changes. Increasing the magnitude of I_{n2} will make the saddle (in region 2 when $I_{n2}=0$) collapsed with the stable node (in region 3 when $I_{n2}=0$) and resulting saddle node bifurcation in region 7; (b) Illustration showing that the bifurcation point is approximately 2/3 of the height between $V_{2saddle}$ and V_{th2} on the same phase portrait. 87

7.6 The plot of (a) combinations of combinations of critical currents, and its (b) corresponding bifurcation point locations. 91

7.7 Illustration of read/write noise margin 93

7.8 The summary of static noise margin in voltage representation and in current representation. 95

8.1 The definition of dynamic noise margin: (a) dynamic read margin and (b) dynamic write margin. 98

8.2 (a) Phase portrait of SRAM when I_N is 500 µA; (b) the timing diagram of this cell. 102

FIGURE Page

8.3 (a) Phase portrait and (b) time diagram for a square pulse noise of 500µA amplitude and 0.43ns duration.. 102

8.4 (a) The simulated phase portrait of a 65nm SRAM based on the S-H model. It shows a cell state crosses separatrix (45° line through origin) and flips to the other side; (b) the timing diagram of the cell state. 103

9.1 An nvSRAM cell schemes of (a) 6T2R and (b) 8T2R 116

A.1 The circuit setup for (a) the critical voltage; (b) the critical current. 128

LIST OF TABLES

TABLE Page

5.1 Basic Transistor Drain Current Equations 48

5.2 Shichman-Hodges Representation 49

7.1 Summary of Region of Bifurcation.. 83

7.2 The BSIM4 Data on a 65nm Technology SRAM (unit is μA) 91

9.1 Summary on the Sensitivity of the System Parameters............................. 113

A.1 The Critical Voltage and Critical Time on Five Random Design Choices Using Numerical Method on L-1 Model...................................... 132

A.2 The Comparison on the Exact Values vs. 2st Order Expansion (V_{CX}=V_{CY})... 132

A.3 The Comparison on the Exact Values vs. 1st Order Expansion (V_{CX}=V_{CY})... 132

CHAPTER I

INTRODUCTION

1.1. Literature Review

1.1.1. The Existing Works on Memristor Cell

Very recently, a new device with pinched hysteresis was demonstrated [1-3], which was recognized as the first real-life realization of the so-called missing fourth circuit element, *memristor*. As a new nanometer device, memristor has drawn a significant interest from the research community [4-11]. Memristor was first theoretically predicted by L. Chua in 1971 [12]. The concept of memristor gained a broader scope in a series of works such as those of L. Chua and S. M. Kang [13-17]. In late 2008, S. Williams, *et al*. unveiled a two-terminal titanium dioxide nanoscale device that exhibited memristive characteristics, thus igniting renewed interest in memristors [18].

Recent research has showcased a number of promising applications of memristor devices. It has been shown by S. Williams and coworkers that solid-state memristors can be used to realize crossbar latches, which could replace transistors in future computers, while taking up a much smaller area [19-22]. There exists a great interest in searching for the next generation of universal memories, which are able to ubiquitously replace traditional DRAM, SRAM. The nonvolatile nature of memristors makes them an attractive candidate for the next-generation memory technology. Memristor memories may have greater data density than hard drives with access times potentially similar to

SRAMs. It has been shown that memristor devices can be scaled down to 10nm or below and memristor memories can achieve an integration density of 100Gbits/cm^2, a few times higher than today's advanced flash memory technologies [23-24]. More broadly, research has been done aiming at employing memristors in programmable logics [25-31], and analog circuit applications [32-38]. In the mean time, researchers have found that LC electronic networks with memristors can model adaptive behavior of unicellular organisms. Results have indicated that electronic circuits with memristors subjected to a train of periodic pulses behave like brain functions, which are able to learn and anticipate. Such a learning circuit may find its valuable applications in a variety of areas, e.g., neural networks and artificial intelligences [39-46].

1.1.2. Existing Works on Static Random Access Memory (SRAM)

SRAM provides indispensable on-chip data storage for an extremely wide variety of electronic applications including microprocessor, ASICs, FPGAs, and DSPs. In today's chip designs, the silicon area occupied by SRAM-based caches dominates over other logic devices, which may constitute more than 70% of chip area. In the past decades, aggressive scaling of transistor feature size has been a primary force driving higher SRAM integration density [47] [48]. On the other hand, the supply voltage is scaled down to meet device reliability constraints and to reduce power consumption. However, the stability margin of SRAM has been significantly degraded by such aggressive scaling. As a result, nanometer SRAM designs are getting increasingly susceptible to various noise problems and there is a growing concern on read-ability and

write-ability. Increasing process variation also has a dramatic impact on the stability of highly scaled SRAM designs.

The traditional static noise margin (SNM) analysis is widely used to characterize the robustness of an SRAM cell. It measure the largest differential voltage noise that can be tolerated at the two storage nodes [49] [50]. More specifically, the SNM is determined as the side of largest square that can be inscribed between the mirrored DC voltage transfer curves (VTCs) of the cross-coupled inverters. However, such a measure is intrinsically unable to characterize the dynamic process that leads to state flips, which is critical for understanding the complete stability picture.

In 2006, the work done by Zhang [51] investigates the SRAM dynamics stability noise margin in linear gate model. Compare to this work, the SRAM dynamic noise margin is derived in Shichman Hodges model (Level-1), which is more complicated model and thus provide more design insights.

1.2. Research Contribution in This Work

1.2.1. Contribution on the Memristor-Based Memory

In this work, by extending the preliminary work in [52], we systematically develop a rather complete set of properties and design equations for guiding the development of memristor based memories. We show important dynamical behaviors of memristor devices and how these characteristics will influence all aspects of analysis and design of memristor memories. Our analyses are much more general than what is presented in [52] and no longer assume a zero on-resistance value to simplify the derived

closed-form equations. We refine the derived equations in more details including, but not limited to, the above relaxed condition, and conclude them by useful properties. Utilizing these memristor properties as design guidance, we then investigate the design of memory read/write schemes and peripheral circuits. Important data integrity and parameter mismatch issues are discussed in depth. Finally, we use extensive simulations to verify the derived properties and demonstrate their usage in memory circuit design.

1.2.2. Contribution on the Static Random Access Memory

In this work, we extend the traditional static noise margin concept to a broader view. Stability will be defined by examining both the magnitude and duration of the injected current noise required to flip the SRAM state. As such, our new stability margin concepts fundamentally capture the temporal aspects of the state flip and provide immediate design insights for enhancing dynamic stability. The concepts of critical current and critical time, based on theoretically rigorous stability analysis of the dynamic behaviors of SRAM cells, provide physical characterizations of SRAM stability. Lastly, we explore an analytical approach to the evaluation of dynamic stability analysis for SRAMs.

1.3. Dissertation Organization

In this dissertation, beginning from Chapter II, the fundamental theory of memristor and the basic concept will be introduced. Most of the research works in the memristor area use the models proposed by HP research group. The proposed HP

memristor models can be categorized in linear and nonlinear drift model. Some of the commonly seen memristor models will be covered.

Chapter III introduces the dynamic behavior of memristor device will influence all aspect of design of memristor memories. The design flow has three basic steps: (1) Systematically develop a rather complete set of properties and design equations for guiding the development of memristor based memories, and show important dynamical behaviors of memristor devices and how these characteristics will influence all aspects of analysis and design of memristor memories. (2) Define logic one/zero region on a memristor cell. (3) Investigate the design of memory read/write schemes.

Beginning with Chapter IV, we first start with the background on SRAM operations and stability issues. Next in Chapter V, modified nodal analysis will be discussed, and we introduce the SRAM circuit and the corresponding nonlinear differential equations based on Shichman-Hodges model.

In Chapter VI, we discuss the bifurcation study to demonstrate the SRAM stability issues. We show that three equilibria are located in three different regions. Then we show the equilibria are two stable equilibria and a saddle (or meta-stable point). From there, we show that the saddle-node bifurcation will happen at a certain injected current magnitude called critical current or I_C. From the phase portrait analysis, when injected current amplitude reaches I_C, we observed that two equilibria collide and result in a saddle-node bifurcation. The collision location is called the bifurcation point. When this happens, the two colliding equilibria disappear, and only the other remaining stable

equilibrium point will survive. The cell state will traverse to that equilibrium point and causes state flip.

Next, in Chapter VII, we introduce region analysis to derive the stability margin analytically for an SRAM. We partition the state space into regions. The equilibrium point locations in terms of a noise injection and system parameters are derived. Furthermore, focus on the region of bifurcation; we derive the bifurcation point and I_C analytically. However, the outcome of analytical solution on bifurcation point and I_C is very complicate. For that, we observe on the numerical property and propose a new method to derive analytical solution for I_C and that can greatly simplifies the equation but keep the accuracy.

In Chapter VIII, we further derive the analytical formula for critical time (T_C). We show that a perturbed transient state trajectory will pass the stability boundary (called separatrix) resulting the state flip when the injected current has higher magnitude than I_C. For a perfectly symmetric SRAM, the stability boundary is a 45 degree line that passes through the origin. However, the injected current greater than I_C does not necessarily implies that the cell will flip its state [51] [53]. The current must be greater than I_c for a certain period of time (defined as critical time or T_C) to cross the separatrix. Once the state of the cell crosses the separatrix, the state will flip even the noise disappears. However, it is still not clear how the SRAM parameters physically influenced the phenomena observed from phase portrait analysis. Accordingly, we resort to analytical form solutions to find the relations. Lastly, in Chapter IX, we conclude the I_C and T_C dependency on technology parameters for design insights.

CHAPTER II

REALIZATION OF MEMRISTOR DEVICE

2.1 The Memristor Theory Background

The fundamental basic circuit elements are resistor, capacitor, and inductor. Resistor relates voltage and current ($dv=R.di$), capacitor relates charge and voltage ($dq=C.dv$), and inductor relates flux and current ($d\varphi=L.di$), respectively. The relation between flux and charge is evidently missing. As shown in Fig. 2.1, Chua argued that there is a missing link between flux and charge, which he called memristance M. [12]

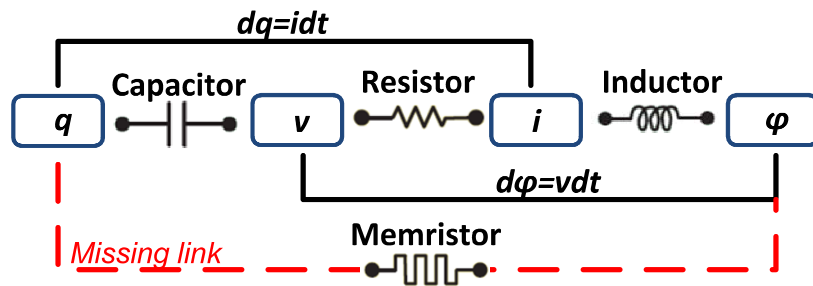


Fig. 2. 1 Four fundamental circuit elements: Resistance ($dv=R\cdot di$), capacitance ($dq=C\cdot dv$), inductance ($d\varphi=L\cdot di$), and memristance ($d\varphi=M\cdot dq$) which is the missing link that Chua argued.

By definition, a linear (constant) memristor acts like resistance. However, if φ-q relation is non-linear, the device behavior is more complex. The memristor characteristics, also referred to as memristance, can be described as:

$$M = d\varphi / dq \,. \tag{2. 1}$$

Similarly, the inverse of the q-φ relation is called memductance:

$$W = dq / d\varphi \,. \tag{2. 2}$$

From (2.1) and (2.2), it can be also seen:

$$v = M \cdot i, \tag{2. 3}$$

$$i = W \cdot v. \tag{2. 4}$$

The memristance M in (2.3) is equal to voltage over current which is also known as the resistance in the linear case. Therefore, memristance has the same unit (*Ohm*) as resistance. Similarly in (2.4), the memductance has the unit of conductance. The inverse of memductance would be memristance, so

$$M = 1/W. \tag{2. 5}$$

2.2 The Memristor Device Models

Hewlett Packard demonstrated the first fabricated physical structure of a memristor device in 2008 also known as *Titanium dioxide memristor*. The HP researcher, R.S. Williams, claims that the device is an electrically switchable semiconductor thin film sandwiched between two metal contacts [18]. The semiconductor thin film has a certain length D, and consists of a doped and un-doped region as shown in Fig. 2.2(a). The internal state variable w represents the length of the doped region. The doped region has low resistance while that of the un-doped region is much higher. As an external voltage bias $v(t)$ is applied across the device, the length w will change due to charged dopant drifting. Hence, the device's total resistivity changes. Fig. 2.2(b) shows its equivalent circuit model, and Fig. 2.2(c) shows the memristor symbol used in a circuit schematic. If the doped region extends to the full length D, that is $w/D=1.0$, the total resistivity of the device would be dominated by the low resistivity

region, with a value measured to be R_{on}. Likewise, when the un-doped region extends to the full length D, i.e. $w/D=0$, the total resistance is denoted as R_{off}. Thus, the mathematical model for memristive device resistance can be described as [18]:

$$R(w) = \left(R_{on} \cdot w/D + R_{off} \cdot (1 - w/D)\right), \quad (2.\ 6)$$

or it can be written as:

$$R(w) = R_{off} - \left(R_{off} - R_{on}\right) \cdot w/D\,. \quad (2.\ 7)$$

Because of physical constraint $0 \le w \le D$, *Property 1* is concluded.

> ***Property 1***: *R_{on} corresponds to memristor state $w=D$. R_{off} corresponds to memristor state $w=0$. The device resistance is bounded between:* $R_{on} \le R(w) \le R_{off}$

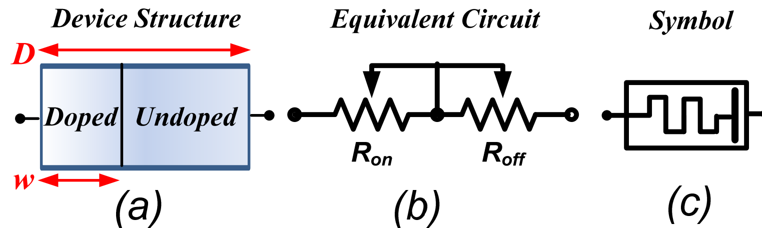


Fig. 2. 2 (a) Memristor device structure; (b) equivalent circuit model and (c) symbol for memristor.

Fig. 2.2(c) shows the memristor symbol used in a circuit schematic. The orientation of the symbol follows the equivalent circuit in Fig. 2.2(b), where R_{on} is at the left and R_{off} is at the right. The polarity matters in memristor circuits. If a bias condition excites the memristance to increase, the reverse connection of memristor would decrease the memristance, which is also equivalent to reverse the polarity of the biasing source. Using this resistive viewpoint, we have

$$v = R(w) \cdot i \ . \tag{2. 8}$$

Referring to Fig. 2.1, equation (2.8) presents the relation of voltage and current. According to the recent research results, there are two types of memristor models: linear drift model, and nonlinear drift model.

2.2.1 Linear Drift Model

The linear dopant drift model assumes a uniform electric field across the device. The net electric field induced a current flow through the memristor device is found to be linearly proportional to the drift-diffusion velocity. Since the drift-diffusion velocity corresponds to the speed of doped region (*dw/dt*), the following equation established [18]:

$$\frac{dw}{dt} = \mu_v \cdot {R_{on}}/{D} \cdot i \tag{2. 9}$$

where μ_v is the average ion mobility.

2.2.2 Nonlinear Drift Model

According to the actual memristor device manufactured in HP's lab, the small voltage can yield enormous electric field in nano-scale devices, which produce significant highly nonlinear ionic transport. These nonlinearities appear to slow down the drift velocity at the thin film edges, where the speed of the state transition around the boundary gradually decreases to zero. This nonlinear dopant-drifting phenomenon is so called the *boundary effect* [6] [54-56]. The nonlinear effect and its modeling are still not

fully understood and an ongoing research which has been pointed out by Kavehei [56]. Nevertheless, one approach to model the boundary effect is by applying *window function* *f(w)* to the drift velocity equation. That is

$$dw/dt = \mu_v \cdot R_{on}/D \cdot i \cdot f(w/D). \qquad (2.10)$$

A widely proposed window function introduced by [6] and [54] is the following:

$$f(x) = 1 - (2 \cdot x - 1)^{2 \cdot P} \qquad (2.11)$$

where P is the *control parameter* that needs to be matched to the manufactured memristor data. The control parameter can only be positive integers.

However, the theoretical models can go much deeper than just window functions. In late 2008, the research group at Hewlett-Packard further announces the memristive switch mechanism of a flux-controlled memristor can be described as follows [57]:

$$I = w^n \beta \cdot \sinh(\alpha \cdot V) + \chi \cdot (\exp(\gamma \cdot V)) - 1) \qquad (2.12)$$

where w is memristor state, V is the applied voltage to memristor, I is the current through memristor, and all others are fitting parameters. When the memristor is around R_{on}, Yang et al. (2008) referred to as ON state, the following approximation valid [57]:

$$I \approx \beta \cdot \sinh(\alpha \cdot V). \qquad (2.13)$$

A more detail descriptions on the dynamics of internal ionic transport involved quantum mechanics. Due to that reason, the suggested expression for the drift velocity becomes very non-linear at strong applied fields: [57]

$$\frac{dw}{dt} = f_{on} \sinh(\frac{i}{i_{on}}) \cdot \exp[-\exp\left((\frac{w - a_{on}}{w_c}) - \frac{|i|}{b} \right) - \frac{w}{w_c}] \qquad (2.14)$$

and

$$\frac{dw}{dt} = f_{off} \sinh(\frac{i}{i_{off}}) \cdot \exp[-\exp\left((\frac{w - a_{off}}{w_c}) - \frac{|i|}{b} \right) - \frac{w}{w_c}] \tag{2. 15}$$

where i_{on}, i_{off} are the minimum on and off magnitude, w_c, b and a_{off} are constants acquired by parameter fitting, and i is the applied current through memristor. Equation (2.14) is applicable when i<0, and (2.15) is applicable otherwise.

Based on the provided memristor model from HP, the minimum current for memristor state switching is not clear by the given simple linear drift formula. As we can see from the more completed memristor model, if the injected current i is less than the on or off magnitude (i_{on} or i_{off}), the value out of hyperbolic sine would be very small, thus the positive or negative drifting velocity would also be small. Therefore, the on and off currents work as a critical current for the memristor state to move, where the linear drift model does not indicate such on or off current phenomenon. However, the more completed model is more complicated than window function and difficult to work with. Nowadays scientists are still looking for other reasonable models.

CHAPTER III

DYNAMIC BEHAVIOR OF MEMRISTOR DEVICE AND ITS PROPERTIES FOR MEMORY USE *

In this Chapter, the characterization on the fundamental memristor device are heavily emphasized. From the basic memristor device model, systematically develop a rather complete set of properties and design equations for guiding the development of memristor based memories. Next, it's assigning memristor area into logic regions. A single memristor cell is to partition to disjointed regions: Logic one and logic zero regions. A safety margin is in between the regions to account for possible noise injection. Finally, a brief demonstration on memristor-based memory is provided. The derived memristor properties will be utilized to illustrate the memristor-based memory read/write operations. The derived designed formulae shown in (3.34) and (3.35) indicate the amount of minimum required time to switch the logic state. The write signal must be sustained longer than the minimum time for a successful write. Similar to devices like SRAM, the SRAM write operation also requires a minimum write time called "critical time". For the SRAM state to flip, the write signal must sustain long than the critical time for a successful write.

*©[2012] IEEE. Reprinted, with permission, from "Dynamical Properties and Design Analysis for Nonvolatile Memristor Memories," by Y. Ho, G. M. Huang, P. Li., *IEEE Trans. Circuits and Systems-I: Regular Paper*, vol. 58, no. 4, April 2011.

Moreover, the proposed read/write scheme used the derived properties as guidance. The design analysis is specifically targeting key electrical memristor device characteristics relevant to, but not limited to, memory operations.

3.1. Characterize The Fundamental Memristor Device

The purpose of characterize the memristor device is to transform the basic memristor device models and derive a set of closed-form design equations. The results succinctly capture the memristor behaviors in a way relevant to memory operations and provide clear design insights by re-derive the model equations.

3.1.1. Characteristics in Linear Drift Model

Memristors can be *charge-controlled* or *flux-controlled* depending on the biasing condition [12]. More specifically, when a memristor is connected to a current source, the current source will inject charges through the memristor cell. It is convenient to treat such a memristor as charge controlled because the state of the memristor changes according to the amount of charge injection, and the state causes memristance to change. On the other hand, when a voltage source is added across a memristor, it is natural to consider the memristor as flux controlled. In this case, the state of the memristor changes according to the amount of flux injection, and the state causes memristance to change.

3.1.1.1. Charge-Controlled Memristance

For a charge-controlled memristance, the memristor state controlled by the charge through the cell, and the state of memristor determines memristance. Figure 3.1 shows a memristor biased using a current source I_{in}, and I_{in} can be any waveform. Integrating (2.9) yields the instantaneous *w(t)*:

$$w(t) = w_0 + \mu_v \cdot {R_{on}}/{D} \cdot q \tag{3. 1}$$

where w_0 is the initial state for state variable *w*. The state of memristor moves from w_0 according to the charge going to the memristor cell. If there is a positive charge injection, the state will move to a higher position, $w>w_0$. If negative charge is injected, memristor state will move to lower position, $w<w_0$. However, memristor state has a physical constraint: the state is bounded in between zero and total length *D,* namely $0 \le w \le D$. Due to the physical constraint, we show that the internal memristor state corresponds to the following effective *q* range:

$$-w_0 D/(\mu_v R_{on}) \le q \le (D - w_0) D/(\mu_v R_{on}). \tag{3. 2}$$

Property 2 describes the actual behavior of memristor state.

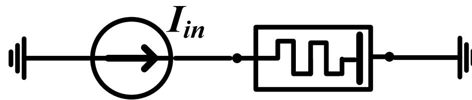


Fig. 3. 1 A memristor biased using current source I_{in}.

Property 2: *The state (length of the doped region) is charge-controlled and can be described as follows:*

$$\frac{w}{D} = \begin{cases} 1 & q > Q_{UP} \\ w_0 / D + \mu_v \cdot {R_{on}}/{D^2} \cdot q, & Q_{LOW} < q < Q_{UP} \\ 0 & q < Q_{LOW} \end{cases}, \qquad (3.\ 3)$$

$$Q_{UP} = (D - w_0)D/(\mu_v R_{on}) \qquad and \qquad Q_{LOW} = -w_0 D/(\mu_v R_{on})$$

where w_0 is the initial state, D is the memristor length, μ_v is the average ion mobility and q is injected charges. Q_{UP} is the upper limit of effective charge injection, and Q_{LOW} is the lower limit of effective charge injection.

Mathematically, when actual charge injection is more than the upper limit of effective charge injection, the state will not go further after it reaches *w=D*. Likewise, the lowest state is at zero even if charge injection is lower than the bottom limit of effective charge injection.

As (3.3) indicates, the memristance works as a charge driven resistance. Equation (3.3) together with (2.7), implies:

$$R(w) = M(q)\,. \qquad (3.\ 4)$$

The resistance becomes charge dependent; hence, the charge-controlled memristace is concluded in *Property 3*.

Property 3: *Charge-controlled memristance can be described as follows:*

$$M(q) = R_{off} - (R_{off} - R_{on}) \cdot \left(\frac{w_0}{D} + \frac{\mu_v R_{on}}{D^2} \cdot q \right). \qquad (3.\ 5)$$

The equation is valid in the range: $Q_{LOW} \leq q \leq Q_{UP}$.

As a special case where $w_0=0$ and R_{on} is small enough such that $(R_{off}-R_{on})\approx R_{off}$, charge-controlled memristance can be simplified to:

$$M(q) = R_{off} \cdot \left(1 - \frac{\mu_v R_{on}}{D^2} \cdot q(t)\right). \tag{3. 6}$$

Suppose a memristor M_a is biased using current sources I_a and a memristor M_b is biased using I_b, in which I_a and I_b have different waveform patterns. Source I_a is a sinusoidal waveform and I_b has a square-wave pattern. Based on (3.3) from *Property 2*, change of the state is controlled by the charges through the memristor. Since the charge is integral of the current with respect to time, the state change caused by I_a would be the same to that by I_b if both have the same integrated charges. This result is summarized in *Property 4*.

Property 4*: The state change of a memristor biased using a current source is only a function of the integrated bias charge regardless of the waveform shape of the bias current.*

One unique property of the memristor has been observed is that the internal state w always comes back to the initial place if the integral of current is zero over a time period. Figure 3.2 is a brief demonstration. The current source I_{in} has positive and negative pulse with equal amplitude and width. Starting from initial state w_0 at t_0, the state rises due to the positive pulse from t_0 to t_1, letting the state rest at w_1. Based on (3.3), the value for w_1 is:

$$w_1/D = w_0/D + \mu_v \cdot {}^{R_{on}}\!/_{D^2} \cdot (I_A \cdot \Delta t) \tag{3. 7}$$

where $(I_A \cdot \Delta t)$ is the charge injection by the positive pulse. From t_1 to t_2, the negative pulse follows, which moves the state from w_1 to w_2, and w_2 can be expressed in terms of w_1 as:

$$w_2 / D = w_1 / D + \mu_v \cdot {R_{on}}/{D^2} \cdot (-I_A \cdot \Delta t) \tag{3. 8}$$

where $(-I_A \cdot \Delta t)$ is the charge injected by the negative pulse. The state w_2 can be rewritten in terms of w_0 by substituting (3.7) to (3.8), which gives $w_2 = w_0$. This indicates that the final state w_2 will be the same as initial state w_0. This type of input waveforms in Fig. 3.2(a) are referred to as *zero net-charge injection* inputs because the integral of the current over the corresponding time period is zero. Zero net-charge injection waveforms do not have to be square waveform; it can be sinusoidal or any other waveforms as long as the integral over a period is zero. Zero net-charge inputs can bring the state back to original level regardless the initial state. However, the state comes back only when the charge exerts onto memristor is within the effective q range described in (3.2). Otherwise, the state will not come back to the original level. This concludes *Property 5*. As will be demonstrated in the following sections, this property plays an essential role in design of memristor memories.

Property 5*: If charge injection exerted onto a memristor is a zero net-charge injection, memristor state will move back to its original position if the exerted charge is within the effective q range:* $Q_{LOW} \leq q \leq Q_{UP}$.

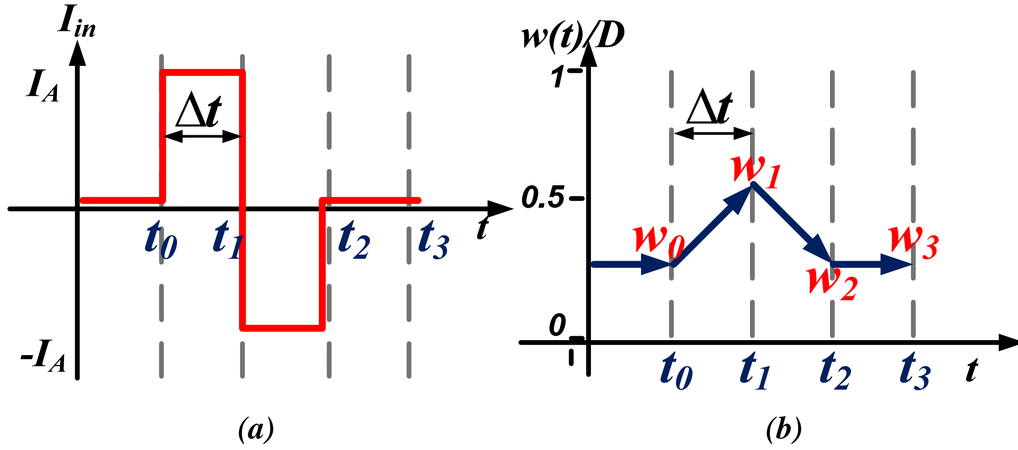


Fig. 3. 2 A square-waveform current source I_{in} has amplitude I_A and $-I_A$ with equal width Δt (a) causes the memristor state (b) transition from w_0 to w_3.

3.1.1.2. Voltage-Controlled Memristance

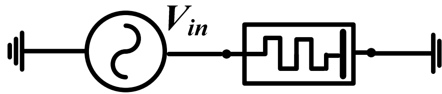


Fig. 3. 3 A memristor biased using voltage source V_{in}.

For a flux-controlled memristance, the memristor state is controlled by the flux across the cell, and the state of the memristor drives memristance. When a voltage source biases a memristor, the memristor can be considered as flux-controlled. Fig. 3.3 shows a memristor biased using a voltage source V_{in}, and V_{in} can be any waveform. Denote β the off/on ratio ($R_{off}=R_{on}\,\beta$). Equation (2.9) can be rewritten as:

$$\frac{dw}{dt}=\frac{\mu_v}{D\beta - w\cdot(\beta-1)}\cdot v\,. \tag{3. 9}$$

After certain manipulations using differential calculus, we get

$$w^2 - \frac{2 \cdot D\beta}{(\beta-1)} w + \frac{2}{(\beta-1)} \cdot (\mu_v \cdot \varphi + C) = 0 \tag{3. 10}$$

where

$$C = D\beta \cdot w_0 - (\beta-1)/2 \cdot w_0{}^2 . \tag{3. 11}$$

Since the integration of the voltage is the flux, denoted by φ, directly relates w with flux φ in a nonlinear fashion. Solving the quadratic equation of (3.10) and picking up the physically meaningful root leads to:

$$w(t) = \frac{D\beta}{(\beta-1)} \cdot \left[1 - \sqrt{\left(1 - \frac{\beta-1}{D\beta} w_0\right)^2 - \frac{2\mu_v(\beta-1)}{(D\beta)^2} \cdot \varphi(t)} \right] \tag{3. 12}$$

where $w(t=0)=w_0$ is the initial condition. Equation (3.12) shows an explicit dependency of the internal variable $w(t)$ on the applied flux. Note that this formula clearly indicates that $w(t)$ is a function of the *flux* applied; it is indirectly dependent on the voltage across the memristor. The input voltage waveform with the same flux leads to the same memristor state.

Due to the finite length D of the thin film, the internal memristor state is constrained as: $0 \le w(t)/D \le 1$, which corresponds to the following effective flux range:

$$-\frac{\Phi_D}{R_{off}{}^2}\left(R_{off}{}^2 - R(w_0)^2\right) \le \varphi(t) \le \frac{\Phi_D}{R_{off}{}^2}\left(R(w_0)^2 - R_{on}{}^2\right). \tag{3. 13}$$

As a result, the more complete set of the state equations are shown in *Property 6*.

Property 6: *The state (length of the doped region) is flux-controlled and can be described as follows:*

$$\frac{w}{D}=\begin{cases}1 & \varphi\geq\Phi_{UP}\\ \frac{\beta}{\beta-1}\left[1-\sqrt{\left(\frac{R(w_0)}{R_{off}}\right)^2-\frac{\varphi}{\Phi_D}}\right], & \Phi_{LOW}<\varphi<\Phi_{UP}\\ 0 & \varphi\leq\Phi_{LOW}\end{cases} \qquad (3.\ 14)$$

$$\Phi_{UP}=\frac{\Phi_D}{R_{off}^{\ 2}}\left(R(w_0)^2-R_{on}^{\ 2}\right) \quad \text{and} \quad \Phi_{LOW}=-\frac{\Phi_D}{R_{off}^{\ 2}}\left(R_{off}^{\ 2}-R(w_0)^2\right)$$

where β denoted the off/on ratio ($R_{off}=R_{on}\ \beta$), w_0 is the initial state, D is the memristor length, μ_v is the average ion mobility and φ is injected flux. Φ_{UP} is the upper limit of effective flux injection; Φ_{LOW} is the lower limit of effective flux injection, and

$$\Phi_D=\frac{(\beta D)^2}{2\mu_v(\beta-1)}$$

Because of the memristor physical constraint, $0\leq w(t)/D\leq 1$, memristor state w would not be more than D when the applied flux across memristor is over the upper bound, and it would not be lower than zero when the applied flux is smaller than the lower bound. Thus, the derived equation (3.14) works only when the applied flux is within the effective range. In other words, for a particular memristor, if the applied flux is larger than the upper limit of the effective range, φ would be the upper limit of effective injection. Likewise, φ would be the lower limit of effective injection if the applied flux is lower than the effective range.

As *Property 6* indicates, the memristance works as a flux driven resistance, thus it implies:

$$R(w)=M(\varphi)\,. \qquad (3.\ 15)$$

By substituting (3.14) into (2.7), the resistance becomes charge dependent, hence, the

charge-controlled memristace is concluded in *Property 7*. The corollary 7.1 also follows.

Property 7: *Flux-controlled memristance can be described as follows:*

$$M(\varphi) = R_{off}\sqrt{\left(\frac{R(w_0)}{R_{off}}\right)^2 - \frac{\varphi}{\Phi_D}} . \tag{3. 16}$$

The equation is valid in the flux range: $\Phi_{LOW} \leq \varphi \leq \Phi_{UP}$.

Corollary 7.1: $R_{on} \leq M(\varphi) \leq R_{off}$ *as seen from (3.16) and Property 1.*

When a single voltage source biases a memristor cell, it generates flux across the memristor and also pushes charges through the memristor. The state of the memristor supposes to move regards to the charge through memristor based on *Property 2*. The applied flux to the memristor cell would also change the state based on *Property 6*. Thus, the memristance change by charge or by flux should be identical, which implies:

$$M(q) = M(\varphi) . \tag{3. 17}$$

Therefore, the q-φ relationship can be expressed as:

$$q(\varphi) = \frac{2\Phi_D}{R_{off}}\left[\left(\frac{R(w_0)}{R_{off}}\right) - \sqrt{\left(\frac{R(w_0)}{R_{off}}\right)^2 - \frac{\varphi}{\Phi_D}}\right]. \tag{3. 18}$$

According to the definition of memductance, the memductance is derived to be:

$$W(\varphi) = 1 \bigg/ R_{off} \cdot \sqrt{\left(\frac{R(w_0)}{R_{off}}\right)^2 - \frac{\varphi}{\Phi_D}} . \tag{3. 19}$$

Based on (2.5), the inverse of memductance gives memristance. Since memductance has flux as the control variable, the inverse of that gives flux-controlled memristance, which is the same as (3.16).

Compared to the properties on charge-controlled case, similar properties can be developed. Suppose a memristor M_a is biased using voltage sources V_a and a memristor M_b is biased using V_b, in which V_a and V_b have different waveform patterns. The change to the memristor states would be the same regardless their waveform shapes as long as the flux injections (integration of their voltages) remain the same, as summarized in *Property 8*.

> ***Property 8***: *The state change of a memristor biased using a voltage source is only a function of the integrated bias voltage regardless of the waveform shape of the bias voltage.*

In addition, a *zero net-flux injection* input, one whose integrated voltage over the time is zero, pushes state of the memristor back to the initial level provided that the flux exerted onto the memristor is within the effective φ range described in *Property 7*. *Property 9* summarizes this phenomenon.

> ***Property 9***: *If the flux injection exerted onto a memristor is a zero net-flux injection, memristor state will move back to its original position if the exerted charge is within the effective* φ *range:* $\Phi_{LOW} \leq \varphi \leq \Phi_{UP}$.

> ***Property 10***: *The memristor state is initially at* w_0. *Suppose the state of memristor is desired to move to a feasible state* w *by a square-wave voltage pulse that has amplitude* V_A *and width* T_w*, the required width* T_w *is:*
>
> $$T_w = \frac{\Phi_D}{V_A R_{off}^{\ 2}} \left[\left(R(w_0)\right)^2 - \left(R(w)\right)^2 \right]. \quad (3.\ 20)$$

Property 10 addresses how much time is needed to move memristor state from an initial w_0 to any state w. Assume memristor state be initially at state w_0. Based on *Property 6*, suppose the state of memristor is desired to move to an arbitrary state w, the

applied flux needed across the memristor to do this job is:

$$\varphi(t)=\frac{\Phi_D}{R_{off}^{\ 2}}\left[\left(R(w_0)\right)^2-\left(R(w(t))\right)^2\right]. \tag{3. 21}$$

Let the applied voltage be a square-wave pulse with amplitude V_A and width T_w, the flux across the memristor is described as follows:

$$\varphi(t)=\int_0^t v(\tau)\partial\tau=\begin{cases}V_A\cdot t & if\ t\le T_w\\ V_A\cdot T_w & if\ t>T_w\end{cases}. \tag{3. 22}$$

When time is in between zero and T_w, the voltage magnitude is V_A and flux is accumulating in this time range. When time goes beyond T_w, the voltage magnitude is zero, so no more flux increment beyond time T_w. Hence, the total flux injection for a square-wave pulse is the amplitude times the width, which is $V_A \cdot T_w$ in this case. The total flux injection determines the change of memristor state. The required width needed to move memristor state from w_0 to w is concluded in *Property 10*. As a special case, the required time needed to move memristor state from $w=0$ to $w=D$ is the same as to move from $w=D$ to $w=0$. This leads to *Corollary 10.1*.

Corollary 10.1*: Suppose a voltage square-wave pulse has amplitude V_A and width T_w is applied to a memristor. The duration needed for memristor state to move from w=0 to w=D is the same as what is required to move the state from w=D to w=0, and the required duration T_w is:*

$$T_w=\left|\frac{\Phi_D}{V_A R_{off}^{\ 2}}\cdot\left(R_{off}^{\ 2}-R_{on}^{\ 2}\right)\right|. \tag{3. 23}$$

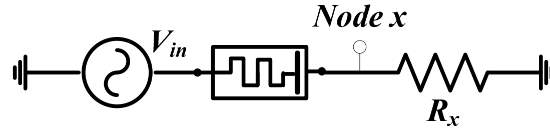


Fig. 3. 4 A voltage divider consisting of a constant resistor R_x in series with a flux-controlled memristor $M(\varphi)$.

Furthermore, consider a series connection of a constant resistor R_x and a memristor, biased using a voltage source, as shown in Fig. 3.4. Using the notion of voltage division, which will prove shortly, we show the voltage response at node *x* in *Property 11*.

> ***Property 11***: *In the voltage divider shown in Fig. 3.4, the node voltage response at node x is given by*
>
> $$V_x = V_{in} \frac{R_x}{R_x + M(\varphi_{in} - \varphi_x)} \tag{3. 24}$$
>
> *where V_x is the voltage at node x, φ_{in} is the input flux injection, φ_x is the flux accumulated at node x, and φ_{in}-φ_x is the flux across memristor M.*

To prove *Property 11*, we derive the input-output relationship of the divider circuit by solving φ_x in terms of φ_{in} analytically. Note that φ_{in} is the input flux injection, φ_x is the flux accumulated at node *x*, and φ_{in}-φ_x is the flux across memristor *M*. Based on Kirchhoff's Current Law, the KCL equation at node *x* implies that all the net charges into node *x* would be zero. Hence, the charges (integral of current) went through the memristor, q_x, should be the same charges went through the resistor, so $q_x=\varphi_x/R_x$. Accordingly, the flux across memristor is φ_{in}-φ_x, and replacing φ by φ_{in}-φ_x and q by q_x in (3.18) yields the charges went through the memristor:

$$\frac{2\Phi_D}{R_{off}}\left[\left(\frac{R(w_0)}{R_{off}}\right)-\sqrt{\left(\frac{R(w_0)}{R_{off}}\right)^2-\frac{\varphi_{in}-\varphi_x}{\Phi_D}}\right]=\frac{\varphi_x}{R_x} \tag{3. 25}$$

in which φ_x has an unique solution as shown below:

$$\varphi_x(t)=\frac{2\Phi_D R_x}{R_{off}}\cdot\left[\frac{R_x+R(w_0)}{R_{off}}-\sqrt{(\frac{R_x+R(w_0)}{R_{off}})^2-\frac{\varphi_{in}(t)}{\Phi_D}}\right]. \tag{3. 26}$$

Since voltage V_x is the total derivative of φ_x, V_x is derived to be:

$$V_x=V_{in}\cdot R_x\Big/\left[R_{off}\sqrt{(\frac{R_x+R(w_0)}{R_{off}})^2-\frac{\varphi_{in}}{\Phi_D}}\right] \tag{3. 27}$$

Therefore, the memristance $M(\varphi_{in}-\varphi_x)$ has become:

$$M(\varphi_{in}-\varphi_x)=R_{off}(\overline{\Phi}_X-R_x/R_{off}) \tag{3. 28}$$

where

$$\overline{\Phi}_X=\sqrt{(\frac{R_x+R(w_0)}{R_{off}})^2-\frac{\varphi_{in}}{\Phi_D}}. \tag{3. 29}$$

Finally, substituting (3.28) back to (3.24) shows that is exactly equal to (3.27). Therefore, that memristor series-connect resistor circuit in Fig. 3.4 indeed behaves as a voltage divider.

> ***Property 12****: For the circuit in Fig. 3.4, assume the voltage source V_{in} is a square-wave pulse with an amplitude V_A and a width T_w. To move the state of the memristor from w_0 to w, the required width T_w is:*
>
> $$T_w=\frac{\Phi_D}{V_A R_{off}^2}\cdot\left[(R(w_o)+R_x)^2-(R(w)+R_x)^2\right]. \tag{3. 30}$$

Property 12 specifies the time needed to move the memristor state from an initial w_0 to w for the divider circuit shown in Fig. 3.4. Note that the flux across memristor is

φ_{in}-φ_x, and φ_x is already derived in (3.26). Substituting $\varphi=\varphi_{in}-\varphi_x$ into (3.21) and yield the following analytical form:

$$\varphi_{in}(w) = \frac{\Phi_D}{R_{off}^{\;2}} \cdot \left[(R(w_o) + R_x)^2 - (R(w) + R_x)^2 \right]. \tag{3. 31}$$

Equation (3.31) reveals the amount of flux injection needed to move the memristor state from w_0 to w. For a supply voltage given in (3.22), as a special case, to move the state from $w_0=0$ to $w=D$ requires the same T_w as what is needed to move from state $w=0$ to $w=D$. This leads to *Corollary 12.1*.

Corollary 12.1*: For the circuit in Fig. 3.4, assume the voltage source V_{in} is a square-wave pulse with an amplitude V_A and a width T_w. The duration needed for the memristor state to move from w=0 to w=D is the same as what is needed to move the state from w=D to w=0, and the required duration T_w is:*

$$T_w = \left| \frac{\Phi_D}{V_A R_{off}^{\;2}} \cdot \left[(R_{off} + R_x)^2 - (R_{on} + R_x)^2 \right] \right|. \tag{3. 32}$$

A memristor has an effective flux restriction due to finite length D. *Property 6* demonstrates the effective φ range for a single memristor case. Thus, the total input flux-injection φ_{in} across memristor and a resistor should have a range as well. The upper bound of such effective range is the amount of flux that pulls initial state w_0 to D. Thus, substituting w=0 and $w=D$ into (3.31) gives the lower and upper bound. This result is summarized in *Property 13*.

Property 13*: When a memristor is connected in series with a resistor as shown in Fig. 3.4, the effective range for φ_{in} across both memristor and resistor is:*

$$\overline{\Phi}_{LOW} \leq \varphi_{in} \leq \overline{\Phi}_{UP} \tag{3. 33}$$

where φ_{in} is integral of V_{in} and,

$$\overline{\Phi}_{LOW} = -\frac{\Phi_D}{R_{off}^{\ 2}}\left((R_{off} + R_x)^2 - (R(w_o) + R_x)^2\right)$$

$$\overline{\Phi}_{UP} = \frac{\Phi_D}{R_{off}^{\ 2}}\left((R(w_o) + R_x)^2 - (R_{on} + R_x)^2\right)$$

Property 14*: Consider the circuit in Fig. 3.4 and assume the voltage source V_{in} has a zero-net-flux injection pattern. The memristor state will move back to the initial level provided that the applied input flux is within the effective range in (3.33).*

Finally, *Property 14* shows that a zero net-flux input voltage pattern will insure that the state of the memristor comes back to the initial position for the circuit shown in Fig. 3.4. It provides important design guidance for ensuring read stability as discussed in detail in later sections. To prove *Property 14,* simply set φ_{in} equal to zero in (3.31) and solve for possible solutions for *R(w);* two possible numerical solutions exist: one is $w=w_0$, and the other solution is outside of the memristor physical range. Therefore, the state will be back to the initial level as $w=w_0$. However, *Property 14* is true only when the effective flux range condition as in *Property 13* is satisfied.

3.1.2. Characteristics in Nonlinear Drift Model

In nonlinear drift model, the window function reflects the following fact: as the memristor state moves toward the boundary ($w=0$ or $w=D$), the dopant drift velocity drastically decreases. However, the state equation behaves close to the linear drift assumption in the region between, in which the properties in the linear drift model are

preserved. As shown in Fig. 3.5, the linear drift operation region is $0.1<w<0.9$. Accordingly, it is desirable to operate in a smaller linear range, say, $W^0 \leq w \leq W^1$, for faster switches and easier design. When approaching the boundaries, the constant average mobility used in the linear model, μ_v, is the upper bound of the nonlinear average mobility used in the nonlinear models.

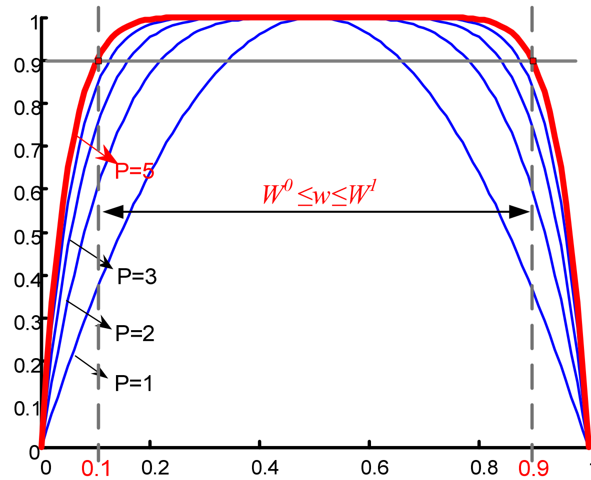


Fig. 3. 5 The window function vs. *w/D* plot.

3.2. Define Logic Regions

For simplicity, a memristor is at *logic zero* when $0<w/D<0.5$ and *logic one* when $0.5<w/D<1.0$. The corresponding ideal output low and high levels are $w/D=0$ and $w/D=1.0$, respectively. In reality, to account for possible noise injections, a safety margin is specified for each logic output: $0 \leq w/D \leq O_L$, ($O_L=W_L/D$ < 0.5) for logic zero, and $O_H \leq w/D \leq 1.0$ ($O_H=W_H/D$ > 0.5) for logic one. The region in between $O_L \leq w/D \leq O_H$ is an unsafe region that should be avoided for read/write data integrity. Fig. 3.6(a) illustrates the situation where $O_L=0.4$ and $O_H=0.6$.

On the other hand, the logic zero/one region needs to be defined before the memristor cell used as memory. With the consideration of the boundary effect, the memristor state is to keep off the boundary. For that, let W^0 be the lower limit and W^1 the upper limit, the ideal linear memristor state will only transition between $W^0 \leq w \leq W^1$. Moreover, W^0 and W^1 separate the nonlinear boundaries and the linear region, which are dependent on the fabrication. Fig. 3.6(b) shows an illustration of the defined output levels.

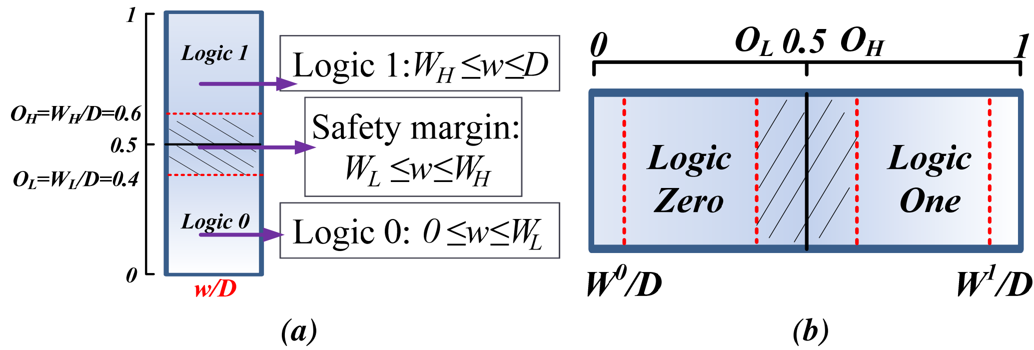


Fig. 3. 6 Memristor output levels. (a) The output low margin is at 0.4 and output high margin is at 0.6 in linear drift model; (b) output levels in nonlinear drift model.

3.3. Memory Cell Read/Write Operations

3.3.1. Write Operation Scheme

To write a logic value to a memristor cell, the proposed way is to have a structure in Fig. 3.7, where the memristor state will alter by the flux injection. Let the applied voltage be a square-wave pulse with amplitude V_A and width T_w.

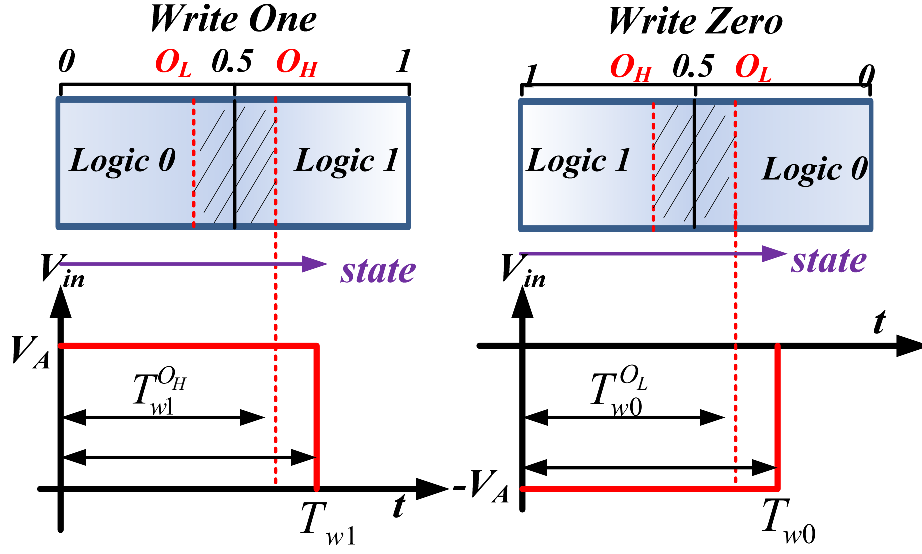


Fig. 3. 7 Write signals (bottom) and corresponding memristor states (top).

Assume initially the state w_0 is initial rest at ideal logic zero state, and it is desirable to write logic one to the cell. For the write process, input voltage V_{in} generates a square-wave pulse that has magnitude $+V_A$ and width T_{w1} as shown in Fig. 3.7. Pulse width T_{w1} must be longer than the minimum required time T_{w1}^{Ow} to insure the state rest inside the logic one region after write. The minimum required time T_{w1}^{Ow} is derived to be:

$$T_{w1}^{O_W} = \frac{\Phi_D}{|V_A| R_{off}^{\ 2}} \left[R_{w0}^{\ 2} - R(W_H)^2 \right], \tag{3. 34}$$

where R_{w0} is the resistance at logic zero state. If the initial state w_0 but somewhere inside the logic 0 region, a successful write can be guaranteed as long as $T_{w1} \geq T_{w1}^{Ow}$. Similarly to write a logic zero, the input voltage V_{in} is a negative square-wave pulse ($-V_A$) with duration T_{w0}. The minimum required time T_{w0}^{OL} would be:

$$T_{w0}^{O_L} = \frac{\Phi_D}{|V_A| R_{off}^2} \left[R(W_L)^2 - R_{w1}^2 \right]. \tag{3. 35}$$

where Rw1 is the resistance at ideal logic one state. The write zero process would be successful if pulse width T_{w0} is at least greater than T_{w0}^{OL}. Thus, a write signal that has duration equal or larger than the derived minimum required time can insure a successful write. Similar to devices like SRAM, the SRAM write operation also requires a minimum write time called "critical time". For the SRAM state to flip, the write signal must sustain long than the critical time for a successful write.

Moreover, the memristor state $w=0$ and $w=D$ are as ideal logic zero and one states in linear drift model. The equation from *Corollary 10.1* specifies the required pulse widths to move a state from $w_0=0$ *to* $w=D$ or move from $w_0=D$ *to* $w=0$. Therefore, the write pulse is highly recommended to have the width in *Corollary 10.1* so the state reaches the ideal logic zero/one state.

Suppose the memristor behavior follows nonlinear drift model. The state W^0 and W^1 are the ideal logic zero and one state. The goal of write operation is to precisely move the state to W^0 for logic zero and W^1 for logic one. They are done by write zero and one process. The proposed write scheme is briefly shown in Fig. 3.8, and Fig. 3.9 illustrates the corresponding pulses for write one/zero process.

Suppose the cell is desirable to write to ideal logic one state, the write one process is performed. Because positive flux injection raises the state, as shown in Fig. 3.9, the state increases due to constant magnitude pulse V_A. The reference voltage V^W_{ref} is set to:

$$V^W{}_{ref} = V_A \cdot R_x / \left(R_x + R(W^1)\right). \quad (3.36)$$

The reference voltage $V^W{}_{ref}$ would come to the same as V_x after some time. When that happens, the memristor state reached the desire state, and the comparator sends a feedback signal to switch off the write pulse.

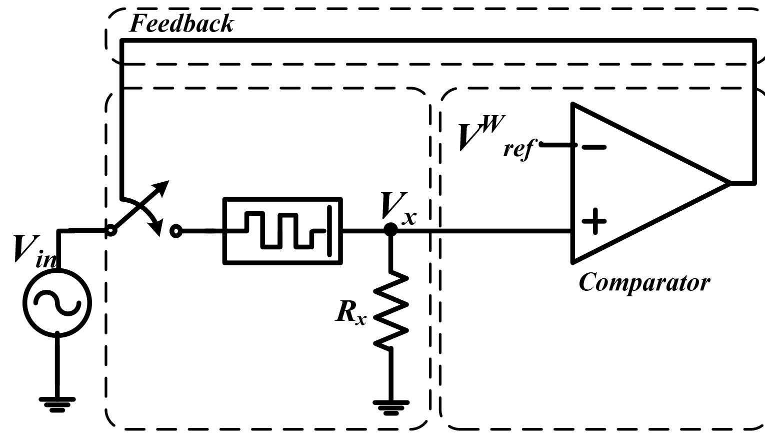


Fig. 3. 8 Write operation structure.

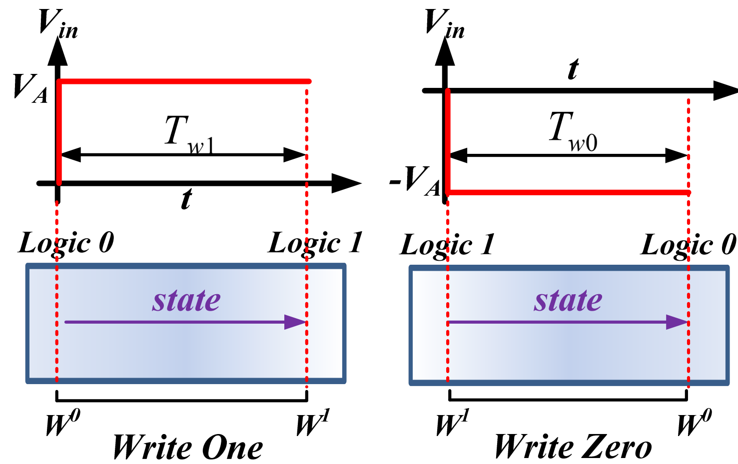


Fig. 3. 9 Write pulses (top) and corresponding memristor states (bottom).

The write zero operation is very similar. A constant magnitude $-V_A$ is applied to the memristor if the memristor does not initially stores a logic zero. The reference voltage is set according to the equation below for write zero process:

$$V^{W}{}_{ref} = -V_A \cdot R_x / \left(R_x + R(W^0)\right). \tag{3. 37}$$

In other words, the write process sets V_{in} to a constant V_A or $-V_A$ magnitude pulse depends on whether writing logic one or zero, and $V^{W}{}_{ref}$ is set accordingly.

3.3.2 Read Operation Scheme

The proposed memristor based memory cell structure is in Fig. 3.10; such read scheme works for both linear and nonlinear models. A read is performed in two stages: convert stage and amplifier stage. In convert stage, the memristor state information converts into a voltage signal, V_x, which reflects the memristor state information. The sense amplifier stage determines the logic based on V_x and output full-swing digital scale.

The designed read signal pattern has a negative pulse followed by a positive pulse with equal magnitude and duration as shown in Fig. 3.10(b). This read pattern will enforce zero net flux injection over one period to avoid altering memristor state after a read access.

In order to extract the information of the internal state, a voltage excitation is applied, which will perturb the memristor state. Due to the memristor property mentioned above, zero net flux injection read pattern avoids altering the memristor state after read cycles. The negative pulse cycle decreases the state and the positive cycle

brings the state back up. The read pulse T_r reflects the amount of perturbation to the memristor state. Large perturbation would lead to data integrity issues. If ideal one state (at W^1) is stored, the read pulse would be constrained by the W_H margin so the state would not travel to unsafe region. If ideal zero state (at W^0) is initially stored, the negative pulse drags the state to nonlinear region. The design on read process is motivated by the insights that nonlinear drift will slow down the drift process of the dopants, thus the designed read flux is a conservative bound based on the linear drift model that will not trap the dopants to the boundary. Accordingly, we constrain the read pulse based on our linear model, that is

$$T_r < \left| \frac{\Phi_D}{V_A R_{off}^2} \right| \cdot \min \left\{ \begin{array}{c} \left| \left(R(W^1) + R_x \right)^2 - \left(R(W_H) + R_x \right)^2 \right|, \\ \left| \left(R(W^L) + R_x \right)^2 - \left(R(W^0) + R_x \right)^2 \right| \end{array} \right\} \tag{3. 38}$$

which is taking the minimum flux injection to move the state from W^1 to W^H or W^0 to W^L.

The resistor in series with the memristor is to convert the memristor state into a voltage signal since the current through the memristor carries the memristor state information, thus the voltage at node x (V_x) would reflect the memristor state information. Use the simplified resistance model, V_x can be expressed as:

$$V_x = V_{in} \cdot R_x / \left(R_x + R(w) \right). \tag{3. 39}$$

Let the reference voltage set to:

$$V^R{}_{ref}(t) = V_A / 2 \tag{3. 40}$$

which V_A is the pulse magnitude shown in Fig. 3.10(b). The negative pulse comes at the first cycle makes V_x negative, and V_o would be zero out of the comparator. At the second

cycle of read pattern, V_x is compared with V^R_{ref} to determine the logic. If the state is below half of D, V_x would be below V^R_{ref}, and logic zero is read. Similarly, V_x higher than V^R_{ref} indicates the memristor state is in upper half of its length D, and logic one is read. For that, the corresponding R_x is the following:

$$R_x = (R_{on} + R_{off})/2\,. \tag{3. 41}$$

This way, we can distinguish logic zero and logic one.

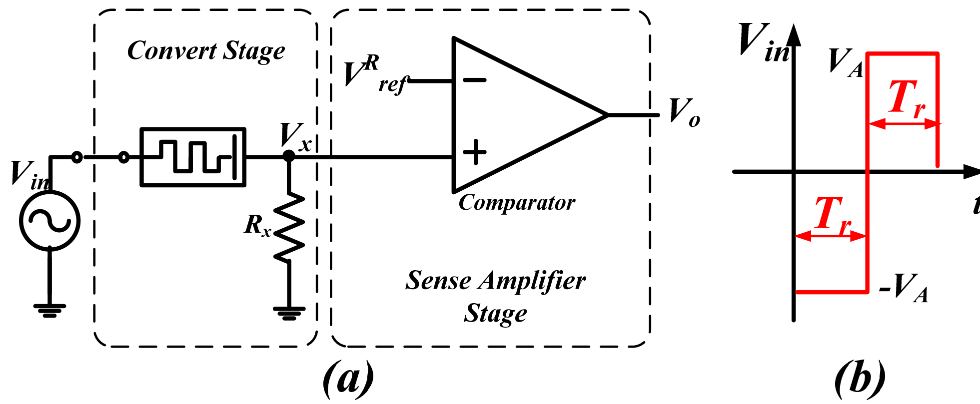


Fig. 3. 10 (a) Operation stages; (b) read pattern.

Figure 3.11 and Fig. 3.12 illustrate the read operation. When the memristor state is initially at logic zero, the input negative pulse (first-half cycle) would decrease the memristor state and the coming positive pulse (second-half cycle) increases the state. Since the read signal has a zero net flux injection pattern, the state is back to the initial level after read. Because the state remains under half of D for all the time, the memristor cell has a high resistance value. Due to the high resistance, the magnitude of V_x remains lower than V^R_{ref} throughout the read operation period, thus logic zero is successfully

read. Similarly to the logic one case illustrated in Fig. 3.11, the state travels within the logic one region as designed due to zero net-flux injection input pattern. Since the memristance is low in logic-one region, the magnitude of V_x is high. The output V_o rise high at the second-half of read cycle since V_x is higher than the reference voltage during that period. Therefore, the detector should read the second-half cycle since it reflects the correct logic state stored in the memristor.

3.4. Memristor Memory Array and Peripheral Circuitry

Figure 3.13 illustrates the overall block diagram view of the memristor-based memory array with peripheral circuits in a way similar to SRAMs. The proposed topology is aiming to fit both linear and nonlinear models. Typical memory arrays have far more words than bits in each word, which would lead to a very skinny shape that is hard to fit into the chip floor plan. Therefore, the array is often folded into fewer rows of more columns. Figure 3.13 is an example of folding design. Each row of the memory contains 2^k words, and the array is physically organized as 2^{n-k} *by* 2^{m+k}. The array has a row decoder, sense amplifiers and a column decoder. In addition, there is a pulse generator and selector units. The pulse generator generates read or write pattern signals. When a read operation is performed, read enable signal would go high and trigger the pulse generator to produce the read pattern signal. When the write operation is performed, the pulse generator will signal the write-one pulse or write-zero pulse depending on the incoming data stored in the input buffer (Data-in). On the other hand, the selector units switch the memristor cells to the ground for a write operation and R_x

for a read operation. R/W Enable (R/W) signal controls the selector to switch properly depending on whether it is a read or a write operation.

For write operations, the pulse generator produces write pulses to the memory array according to the data value sitting in the data-in buffer. In the meantime, the selectors will select the corresponding column lines to ground. The other unselected lines would be floating, so there will be no stage change for these unselected cells.

For read operations, the pulse generator is triggered to produce read pattern signals. Then the selectors switch each selected column to a resistor (R_x). The resulting voltage drop across R_x will be amplified by the sense amplifier to full voltage swing. Lastly, the data-out buffer will be triggered at the second half period of the read cycle to capture the readout data.

The procedure to access the memristor based memory is quite similar to the standard SRAM we have today. Data will be read or written to cells by the proposed read or write scheme. It is suggested to perform a write back (refresh) signal for better data retention since pulse mismatch and noise issues are often existed.

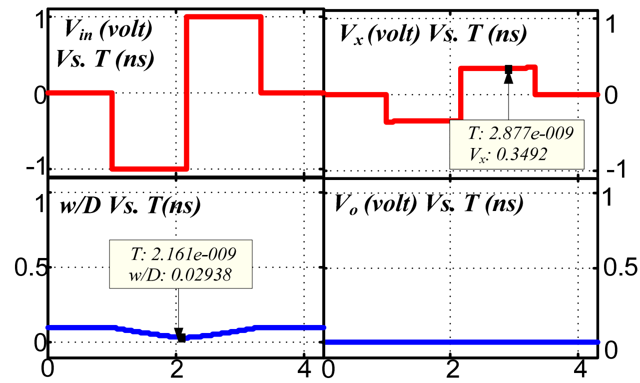


Fig. 3. 11 Read operation (logic zero case).

Image was adapted with permission [58].

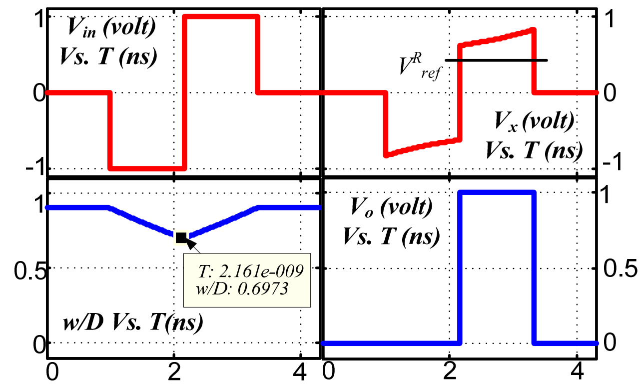


Fig. 3. 12 Read operation (logic one case).

Image was adapted with permission [58].

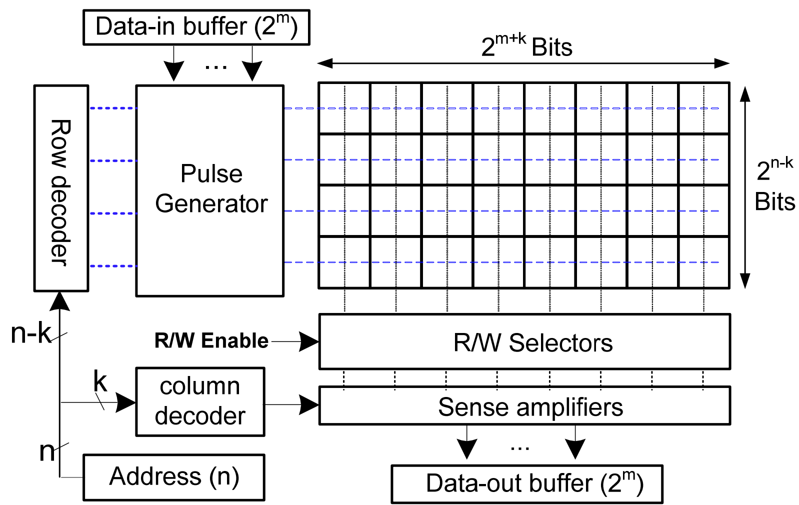


Fig. 3. 13 Proposed memristor-based memory array structure.

CHAPTER IV

BACKGROUND ON THE STATIC RANDOM ACCESS MEMORY

4.1. How Does SRAM Work?

The Static Random Access Memory cell (SRAM) is often constructed by two cross-coupled inverters (labeled *M1 M2 M3* and *M4*) and two access transistors, labeled *M5* and *M6* from Fig. 4-1 [59]. The access transistor acts as transmission gate allowing bidirectional current flow between the coupled inverters and bit-lines. The access transistors are turned on when the word line is selected. In particular, the SRAM can hold their stored data indefinitely as long as the power supply provided [60]. Figure 4-2 is another way to show a 6-T SRAM cell graphically, where the main SRAM cell (M_1 *to* M_4) is replaced by two cross-coupled inverter symbols.

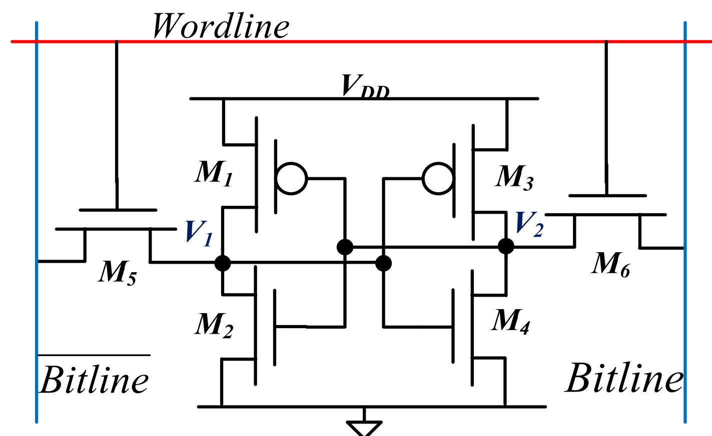


Fig. 4.1 A 6-T SRAM cell.

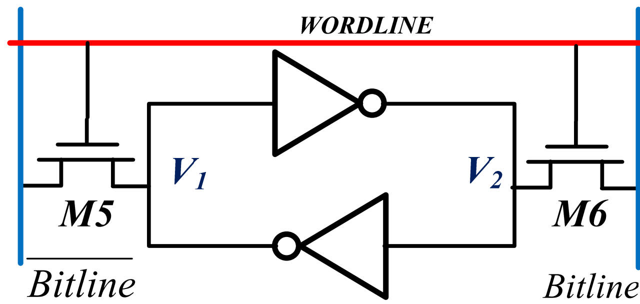


Fig. 4.2 A simplified graphical representation of 6-T SRAM cell.

4.1.1. The Read Operation

The goal of read operation is to retrieve the information stored in V_1 and V_2 node onto the two bit-lines. Assume the cell is initially stored a logic zero, meaning $V_1=V_{DD}$ and V_2=0. Before the read operation begins, the bit lines are pre-charged to V_{DD}, namely $V_{bitline}=V_{bitline\text{-}bar}=V_{DD}$. When the word line is high, *M5* and *M6* are turned-on. Because the bitline voltage ($V_{Bitline}=V_{DD}$) and the stored node V_2 form a potential difference, here will be current flow through M_6. The current direction is from the pre-charged bitline through *M6* and *M4* then onto ground. Thus, lower the pre-charged voltage at bitline. On the other side of circuit, no current will flow through M_5 since the pre-charged bitline-bar voltage $(V_{bitline\text{-}bar})$ and stored node V_1 are both V_{DD}. Fig. 4-3 summarized the read operation.

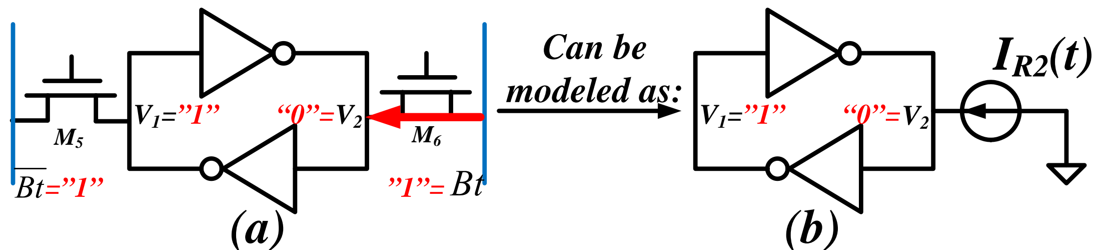


Fig. 4.3 (a) Noise injection during a read operation, and (b) its equivalent model.

Careful choice of transistor driving strength is necessary for correct operation. While the bitline is discharging through M6, it would raise V_2. If V_2 has accidently been raised high to certain threshold, it might flip the stored states. To avoid this, the pull down NMOS strength should design to be stronger than the access transistors, so it quickly drains out the rising voltage at V_2. This constraint will insure a stable read. In short, the read operation can be treated as a current source attached to the SRAM main cell as shown in Fig. 4-2(b). The read stability maintained if I_{R2} does not cause the state-flip.

4.1.2. The Write Operation

The goal of write operation is to send the information on bit line into the cross-coupled inverters' stored nodes. In another word, write operation is making node V_1 and V_2 to store the information on *bitline* and *bitline-bar*. Assume initially $V_1=V_{DD}$ and $V_2=0$, and the objective is to write $V_1=0$ and $V_2=V_{DD}$. To do that, the $V_{bitline\text{-}bar}$ will be discharged to zero, and the $V_{bitline}$ would be pre-charged to V_{DD}. Once the write line goes high, both M5 and M6 conduct drain currents, and the write operation can be treated as attaching two current sources onto SRAM main cell. Fig. 4-4 summarized the write operation.

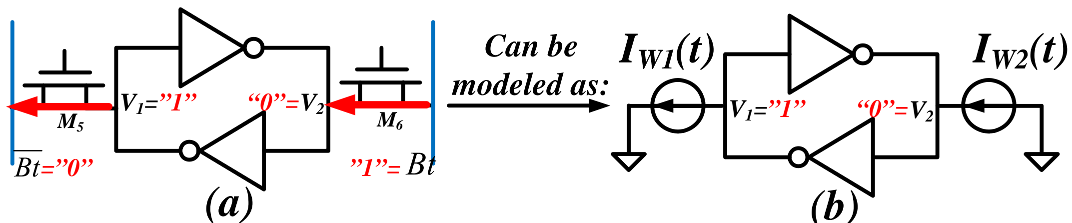


Fig. 4.4 (a) Noise injection during a write operation, and (b) its equivalent model.

Since M4 has strong pull down strength over M6 to satisfy stable read constraint, the access M6 transistor is unable to pull up V_2 because M4 has greater pull down strength. Hence, the cell must be written by forcing V_1 low. Originally V_1 stored V_{DD}, so the job of pulling V_1 down relies on the access transistor M5. Transistor M1 is opposing this operation because M1 is supplying current to node V_1. Thus, the strength of M1 must be weaker than M5, so M5 is able to pull V_1 down for successful write.

Therefore, for SRAM to have correct operation and maintain sufficient read-ability and write-ability, the strength of MOS should be designed in this order: NMOS>ACCESS>PMOS. The driving strength depends on transistor sizing. For greater driving strength, designers tend to size up a transistor, and size down a transistor for low driving strength. The K values we will introduce later contain the transistor sizing factor. Therefore, for correct operation, the SRAMs often design to have $K_n > K_p$. [61]

4.1.3. The Standby Mode

In the standby mode, the two access transistors are off, and the stored information contained in the SRAM cell. The SRAM state flips may occur if certain coupling noise, in the form of a noisy current, strikes one of the bit-lines. This noise injection process is illustrated in Fig. 4.5, where it is assumed that nodal voltages V_1 and V_2 correspond to logic "1" and "0", respectively. The same process has been analyzed to study the SRAM's immunity to single even upsets (SEU) [62-66]. During an SEU event, when

an ion particle strikes the diffusion region of a transistor, it deposits charge, which results in voltage spike on the affected node. The current pulse that results from such a particle strike is traditionally modeled as a double exponential function [53]. The expression for this pulse can be modeled as:

$$I_{noiseL,noiseR}(t) = \frac{Q}{T_\alpha - T_\beta}\left(e^{-t/T_\alpha} - e^{-t/T_\beta}\right) \qquad (4.\ 1)$$

where Q is the amount of charge deposited as a result of the ion strike, while T_α is the collection time constant for the junction and T_β is the ion track establishment constant. For the purpose of characterization, the following scenarios can cause the SRAM state flip: a noise current going away from the high voltage node (Fig. 4.5a), a noise current going into a low voltage node (Fig. 4.5b) or both.

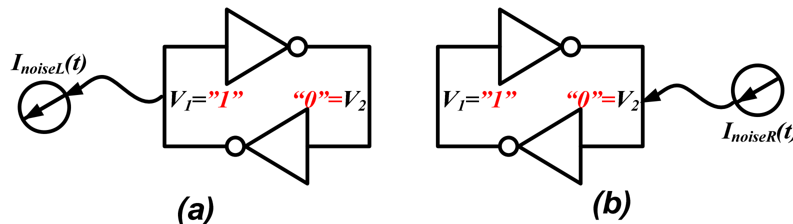


Fig. 4.5 An SRAM state flip caused by (a) a current going away; (b) a current injection in standby mode.

4.2. Traditional Static Noise Margin

The traditional static noise margin analysis characterizes the robustness of an SRAM cell by using two voltage sources as shown in Fig 2(a).Conventional SNMs measure the largest differential voltage noise that can be tolerated at the two storage nodes [67-68]. In standby, as shown in

Fig. 2(b), the SNM is determined as the side of largest square that can be inscribed between the mirrored DC voltage transfer curves (VTCs) of the cross-coupled inverters. The SNM in read can be defined similarly by including the two access transistors as part of the inverter pair VTCs. The SNM in read represents the largest DC voltage perturbation that can be tolerated without a state flip. During write, the SNM is found by inscribing the largest square in between the two VTCs as shown in Fig. 2(c).

An SNM metric describes the maximum voltage (or current) perturbation the SRAM circuit can tolerate without resulting a state flip. However, such a measure is intrinsically unable to characterize the dynamic process that leads to state flips, which is critical for understanding the complete stability picture. In the paper, stability will be defined by examining both the magnitude and duration of the injected current noise required to flip the SRAM state. As such, our new stability margin concepts fundamentally capture the temporal aspects of the state flip and provide immediate design insights for enhancing dynamic stability.

Clearly, as SNMs are characterized by finding the largest static voltage noise that can be tolerated in standby, read or write, they are not positioned in capturing the essential dynamic properties of these operations, as further discussed in the following chapter.

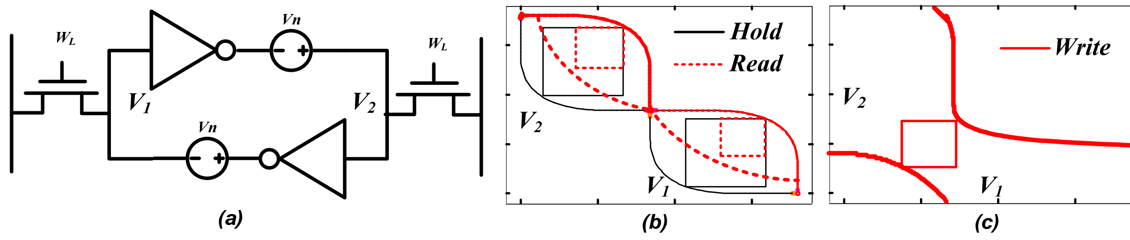


Fig. 4. 6 (a) characterization of the traditional SNMs, (b) SNM in standby, (c) SNM in write.

CHAPTER V

THE DYNAMIC MODEL FOR SRAM CELL

Before deriving the proposed models for dynamic stability, we first discuss the basic transistor-level models and how a cell can be modeled as a dynamic system.

5.1. The MOSFET Transistor model

5.1.1 Shichman-Hodges Representation (Level-1 Model)

The modeling method is based on the most commonly known model. The level-1 MOSFET spice model consists with three regions: cut-off, linear, and saturate region. Table 5.1 summarizes the conditions for each region, and drain current equations for NMOS and PMOS [60]. One thing to notice is that threshold voltage of PMOS from Table 5.1 is taken absolute value for simplicity later on.

Table 5.1. Basic Transistor Drain Current Equations

	NMOS	PMOS
Cut-off	$V_{GS} < V_{THN}$ $I_{DS} = 0$	$V_{SG} < \|V_{THP}\|$ $I_{SD} = 0$
Linear	$V_{GS} > V_{THN}$ $V_{DS} < V_{GS} - V_{THN}$ $I_{DS} = K_N (2(V_{GS} - V_{THN})V_{DS} - V_{DS}^2)$	$V_{SG} > \|V_{THP}\|$ $V_{SD} < V_{SG} - \|V_{THP}\|$ $I_{SD} = K_P (2(V_{SG} - \|V_{THP}\|)V_{SD} - V_{SD}^2)$
Saturate	$V_{GS} > V_{THN}$ $V_{DS} > V_{GS} - V_{THN}$ $I_{DS} = K_N (V_{GS} - V_{THN})^2$	$V_{SG} > \|V_{THP}\|$ $V_{SD} > V_{SG} - \|V_{THP}\|$ $I_{SD} = K_P (V_{SG} - \|V_{THP}\|)^2$

The term V_{DS} can be written as:

$$V_{DS} = V_D - V_S \tag{5. 1}$$

From KVL, V_D can be represented as:

$$V_D = V_{DG} + V_{GS} + V_S \quad (5.2)$$

After substitute (5.2) to (5.1), the other way to write V_{DS} in NMOS is below:

$$V_{DS} = V_{GS} - V_{GD} \quad (5.3)$$

Similarly, the V_{SD} in PMOS can be written in a similar manner as (2.4).

$$V_{SD} = V_{SG} - V_{DG} \quad (5.4)$$

By substituting (5.3) for the NMOS equations, and (5.4) for PMOS equations, the Level-1 current equations can be rewritten into the form shown in Table 5.2. [69] [70]

Table 5.2. Shichman-Hodges Representation

	NMOS	PMOS
Cutoff	$I_{DS} = 0$	$I_{SD} = 0$
Linear	$I_{DS} = K_N ((V_{GS}-V_{THN})^2 - (V_{GD}-V_{THN})^2)$	$I_{SD}=K_P ((V_{SG} -\|V_{THP}\|)^2 -(V_{DG} -\|V_{THP}\|))^2$
Saturate	$I_{DS} = K_N (V_{GS} - V_{THN})^2$	$I_{SD}=K_P (V_{SG}-\|V_{THP}\|)^2$

The advantage of writing in the form in Table 5.2 is keeping variable inside the square term. Using NMOS as example, notice that V_{GS} is less than V_{THN} when in cut-off mode, and V_{GS} is higher than V_{THN} if not in cut-off mode. In another word, V_{GS}-V_{THN} is less than zero for cut-off mode and has zero current. That's the same as treating saturation equation with V_{GS}-V_{THN} equal to zero. If not in cut-off mode, V_{GS}-V_{THN} is higher than zero and the term V_{GS}-V_{THN} survive as shown in linear and saturation mode.

One of the key difficulties in deriving analytical dynamic stability models lies in the fact that different equations for typically used for determining drain currents in the cut-off, linear and saturation regions. To resolve this problem, we adopt the equivalent

Shichman-Hodges representation of the drain currents shown in Table 5.2 [71] with the following S-function:

$$S(x) = \begin{cases} 0 & X \le 0 \\ X & X > 0 \end{cases} \tag{5. 5}$$

Using *S(x)* and Table 5.2, the drain currents for NMOS and PMOS transistors can be written as follows:

$$I_{DSN}(V_{GS}, V_{GD}) = K_N \cdot (S^2(V_{GS} - V_{THN}) - S^2(V_{GD} - V_{THN})), \tag{5. 6}$$

$$I_{SDP}(V_{SG}, V_{DG}) = K_P \cdot (S^2(V_{SG} - |V_{THP}|) - S^2(V_{DG} - |V_{THP}|)). \tag{5. 7}$$

The parameters K_1 to K_4 are the MOS device parameters of transistor M_1 to M_4:

$$K_{1,2,3,4} = \frac{1}{2}\mu_{n,p} \cdot C_{OX} \cdot W_{1,2,3,4} / L_{1,2,3,4} \tag{5. 8}$$

where $\mu_{n,p}$ is the carrier mobility (μ_n or μ_p), C_{OX} is the per unit area gate capacitance, $W_{1,2,3,4}$ and $L_{1,2,3,4}$ are the effective channel width and length of the transistor, respectively.

Note (5.7) and (5.7) are valid for all regions of operation. The function S(x) is used to combine the three drain current equations of NMOS and PMOS transistors into one equation. This constitutes an important step towards deriving the proposed analytical dynamic stability models. Furthermore, note that the threshold voltage of typical enhancement mode PMOS transistors is negative. For simplicity of presentation, with some abuse of notation, throughout the rest of the paper we use a variable such as V_{THP} to indicate the absolute value of the threshold voltage of a PMOS transistor, which is positive.

For continuously differentiable property, the following smooth version of *S(x)* function can be used:

$$S(x) = \log(1 + e^{A \cdot X}) / A \tag{5. 9}$$

where A is a constant. The suggested value for A is 100 for CMOS. The higher the A number is, the closer the log function approach to true *S(x)* function. Fig. 5.1 shows the plot of smooth version of *S(x)* function with A=100 and A=50. The transition is sharper for higher A. When use this smooth version of S(x) function, be aware of the digit of precision that machine need to handle to implement this type of function. When choosing a big A number like 100, assume V_{GS}-V_{THN} is 1, exponential of 100 is about ten to the power of 43. If V_{GS}-V_{THN} is zero, exponent of zero is one. That means this function deals numbers varying from one to ten to the power of 43, and not every compiler can deal this kind of precision. The modified sets of current equations with smooth version of *S(x)* functions are shown as follows:

$$I_{DSN} = \frac{K_N}{A^2} \cdot (\log^2(1 + e^{A \cdot (V_{GS} - V_{THN})}) - \log^2(1 + e^{A \cdot (V_{GD} - V_{THN})})) \tag{5. 10}$$

$$I_{SDP} = \frac{K_P}{A^2} \cdot (\log^2(1 + e^{A \cdot (V_{SG} - |V_{THP}|)}) - \log^2(1 + e^{A \cdot (V_{DG} - |V_{THP}|)})) \tag{5. 11}$$

5.1.2 The Berkeley Simulation IGFET Model (BSIM)

Accurate transistor models are needed for electronic circuit simulation, which in turn is needed for integrated circuit design. As the semiconductor devices gets into deep sub-micron process generations, a new model is needed to be developed to reflect the transistor's behavior for that technology node. Because the earlier models may become

inaccurate, the commercial and industrial analog simulators (such as CADENCE) have added many other device models as technology advanced. An industry working group so called the Compact Model Council was formed to standardize the models for industrial use, and BSIM (Berkeley Short-channel IGFET Model), developed by the Department of Electrical Engineering and Computer Sciences (EECS) at the University of California at Berkeley CA, is one of these standardized models [72]. The BSIM family includes BSIM3, BSIM4, BSIM6, BSIM-SOI and BSIM-CMG, BSIM-IMG.

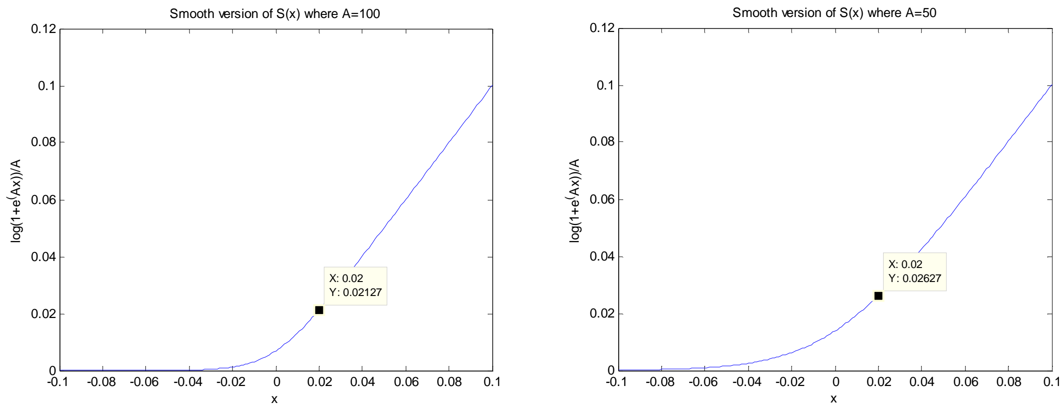


Fig. 5. 1 The plot of smooth version of S(x) with A=100 (Left) and A=50 (Right)

5.2. The Dynamic Model for SRAM

A circuit may be described using a modified nodal analysis formulation in the time domain:

$$\dot{Q}(v) = F(v) + I_N \tag{5. 12}$$

where $I_N \in R^N$ is the input, $v \in R^N$ is the state variables, F describes the resistive devices of the circuit, Q is the capacitive devices of the circuit, and I_N is an arbitrary current. For the SRAM cell in Fig. 5.2, for simplicity, we only consider two state

variables, voltage (V_1) and its complement (V_2). The circuit equations for the SRAM cell are:

$$\begin{cases} C_{11}(V_1,V_2)\cdot \dot{V}_1 + C_{12}(V_1,V_2)\cdot \dot{V}_2 = f_1(V_1,V_2) + I_{N1} \\ C_{21}(V_1,V_2)\cdot \dot{V}_1 + C_{22}(V_1,V_2)\cdot \dot{V}_2 = f_2(V_1,V_2) + I_{N2} \end{cases} \quad (5.\ 13)$$

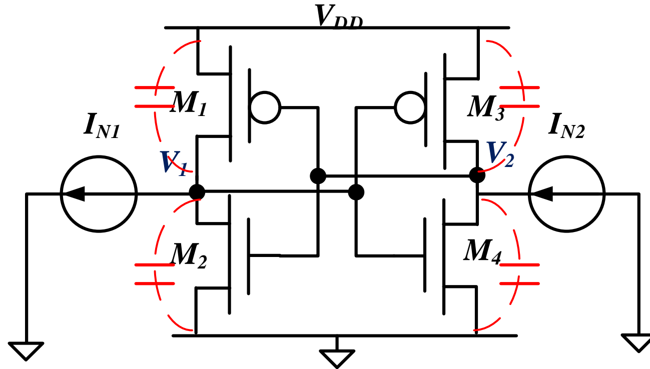


Fig. 5. 2 The SRAM cell with internal lumped capacitors drawn.

where the Cs are the capacitances associated with the two storage nodes, f_1 and f_2 represent the currents of the transistors in the two cross-coupled inverters, I_{N1} and I_{N2} represent additional currents injected to the two storage nodes. We assume the coupling effect between V_1 and V_2 is small, thus C_{12} and C_{21} are neglected. Note that physically C_{11} and C_{22} are mostly contributed by gate and drain parasitic capacitances at V_1 and V_2 nodes. For simplicity, we use circuit simulation to extract averaged small-signal capacitance values C_1 and C_2 by averaging C_{11} and C_{22} over a range of operating points, and finally arrive at:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_1,V_2) + I_{N1} \\ C_2 \cdot \dot{V}_2 = f_2(V_1,V_2) + I_{N2} \end{cases} \quad (5.\ 14)$$

where I_{N1} and I_{N2} represent as the injected DC currents. For instance, they can be used to describe the noise injected current in standby mode, or the read/write current through the access transistors.

In (5.14), f_1 and f_2 are determined by the drain currents of the transistors, which can be modeled using the Level-1 device equations in Table 5.2. As such, the following *f1* and *f2* complete the dynamic equations for SRAM:

$$\begin{cases} f_1(V_1,V_2) = I_1(V_1,V_2) - I_2(V_1,V_2) \\ f_2(V_1,V_2) = I_3(V_1,V_2) - I_4(V_1,V_2) \end{cases} \tag{5. 15}$$

where (I1, I2, I3, I4) are the drain current for transistor (M1, M2, M3, M4), and their expressions are as follows:

$$\begin{cases} I_1 = K_1[S^2(V_{DD} - V_2 - V_{TH1}) - S^2(V_1 - V_2 - V_{TH1})] \\ I_2 = K_2[S^2(V_2 - V_{TH2}) - S^2(V_2 - V_1 - V_{TH2})] \\ I_3 = K_3[S^2(V_{DD} - V_1 - V_{TH3}) - S^2(V_2 - V_1 - V_{TH3})] \\ I_4 = K_4[S^2(V_1 - V_{TH4}) - S^2(V_1 - V_2 - V_{TH4})] \end{cases} \tag{5. 16}$$

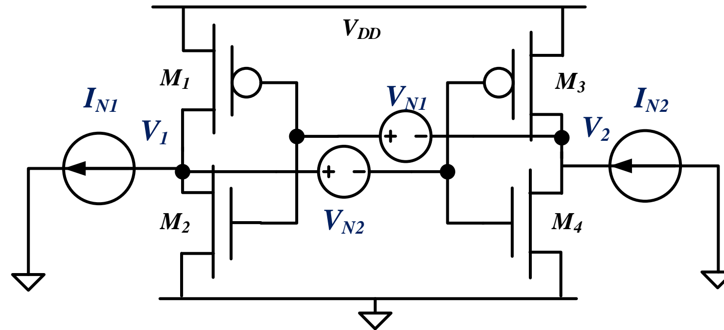


Fig. 5. 3 The SRAM cell with cross-coupled voltage sources inserted.

For traditional Static Noise Margin study, one can insert cross-coupled voltage sources in the SRAM main cell. The dynamic equations with cross-coupled voltage sources incorporated would be:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_1, V_2 + V_{N1}) + I_{N1} \\ C_2 \cdot \dot{V}_2 = f_2(V_1 - V_{N2}, V_2) + I_{N2} \end{cases} \tag{5. 17}$$

In addition, the cross-coupled voltage sources can also model the voltage loss on the metal lines.

CHAPTER VI

SRAM STABILITY AND ITS MATHEMATICAL EQUIVALENCE

This chapter will discuss SRAM instability and the bifurcation study. We will first introduce the concept of voltage transfer curves (or called nullclines), equilibrium point and separatrix mathematically for clarity. We show that SRAM has three equilibria. Two of the equilibrium points are stable and the other one is saddle (or meta-stable point).

SRAM state flip happens under perturbations. In general, one can model the perturbations using voltages and current sources. The noise injections are typically in current form. Noise pattern like SEU is a cosmic type current waveform striking the stored nodes. Thus, it can be modeled as a current sources attached to V_1 and V_2 nodes. On the other hand, traditional static noise margin studies SRAM instability by introducing voltage perturbations. It introduces cross-coupled voltage sources across two stored nodes. The cross-coupled voltage sources can also model the voltage drop on metal routings.

The dynamic modeling for both cases have been discussed in Chapter II. In this chapter, we will show how the voltage transfer curve and SRAM equilibrium points change with different injected voltage or current magnitude. With this, we can see that the SRAM instability happens when two voltage transfer curves tangent to each other at a point; this phenomenon is called *saddle-node bifurcation*, and the tangent point is

called the *bifurcation point*. The injected voltage or current magnitude causes the bifurcation to happen will be called the *critical voltage or current*, namely V_C or I_C.

When the injected noise magnitude goes higher than the critical magnitude, the SRAM state will start to traverse to stability boundary (or called Separatrix) and onto the other equilibrium point and cause state flip. Thus, the stat flip does not happen immediately. We name the time to the stability boundary the *critical time*, T_C. In summary, the injected noise magnitude (either in voltage or current) has to be higher than the critical magnitude (V_C or I_C) for a duration longer than critical time to result state-flip.

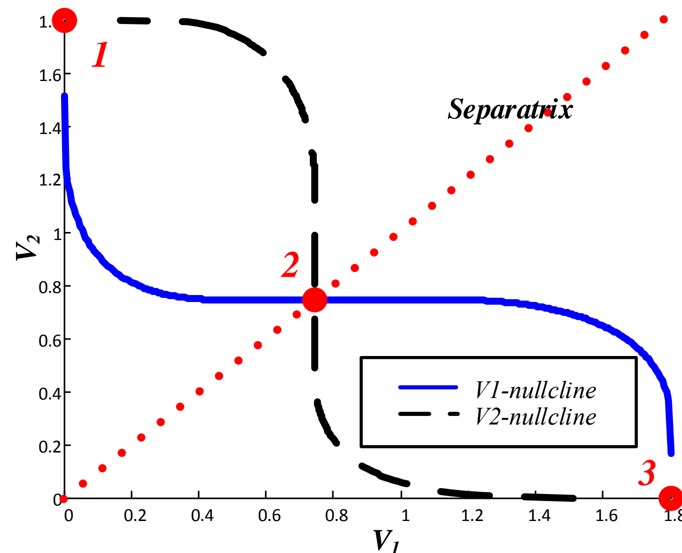


Fig. 6. 1. An example of voltage transfer curves on a 65nm technology SRAM.

6.1. Voltage Transfer Curves (VTCs)

In a general second order autonomous system, all the points satisfied $dV_1/dt=0$ is the V_1-nullcline and all the points satisfied $dV_2/dt=0$ is V_2-nullcline. The voltage transfer

curves are basically the concept of nullclines. Figure 6.1 shows the voltage transfer curves. The SRAM voltage transfer curves consist of V_1-nullcline and V_2-nullcline, where the nullcline of V_1 or V_1-nullcline is the set of points satisfied:

$$C_1 \cdot \dot{V}_1 = f_1(V_1, V_2) + I_{N1} = 0\,, \tag{6. 1}$$

and the nullcline of V_2 or V_2-nullcline is the set of points satisfied:

$$C_2 \cdot \dot{V}_2 = f_2(V_1, V_2) + I_{N2} = 0\,. \tag{6. 2}$$

The voltage transfer curves are also called the "butterfly curves" in some literatures. [70-74]

6.2. The SRAM Equilibrium Points

According to nonlinear theory, equilibrium points are found by solving function $dV_1/dt=0$ and $dV_2/dt=0$. In other words, the points of intersection onV_1-nullcline and V_2-nullcline are exactly the equilibrium points. As shown in Fig. 6.1, the point#1, point#2 and point#3 are the equilibrium points. The point#1 and point#3 are the stable equilibrium points, and point#2 is a saddle [75] [76].

6.3. Stability Boundary of an SRAM

The stability boundary, or called separatrix, separates the regions of attractions of the two stable equilibria as shown in the dot line in Fig. 6.1. Starting from any initial state above the separatrix, the SRAM state will eventually go to the stable equilibrium "1". Similarly, the state will be driven towards to the other stable equilibrium "3", if starting from a point below the separatrix.

In other words, an SRAM state starting anywhere within the stability region would converge to its equilibrium state. And, the stability boundary is a border that separate stable regions. For example, a point starts in the stable region of point#1 will gradually converge to equilibrium point #1.

During the SRAM operations, a state flipping would occur if the state is perturbed across the stability boundary. In a symmetrical case, the stability boundary is simply a 45 degree line passing through the origin on the phase portrait [51] [76]. The stability boundary for a given SRAM is also called *separatrix* because the stability boundary separates two stability regions [76]. In the case of SRAM cell, if the injected noise is higher than the stability margin, the state of the cell can deviate from the initial stable equilibrium and cross the separatrix after certain time period. If this happens, the cell state will fall into the stability region of the other stable equilibrium state and result in a state flip. The sections below discuss some of the concept in nonlinear theory point of view.

6.3.1. The Stability Boundary Theory

For a given dynamic equation $\dot{x} = f(x)$ with x in an N dimensional space, the equilibrium points are all the x_e's that satisfy $f(x_e)=0$. Its stable manifold and stability region can be described as below: [76]

6.3.1.1. General Theorems

The stable manifold of an equilibrium point x_e is defined as: [59][77-78]

$$W^s(x_e) = \{x \in R^N \mid \lim_{t \to \infty} \phi(t, x) = x_e\} \quad (6.3)$$

where $\phi(t, x)$ is the trajectory that starts from x and eventually converges to x_e. The stability region or region of attraction $A(x_e^s)$ of a stable equilibrium point x_e^s is the stable manifold of stable equilibrium point, x_e^s.

Definition of hyperbolic equilibria: [59]

An equilibrium is called hyperbolic if there are no eigenvalues on the imaginary axis.

Stable Manifold Theorem For a Fix Point: [76]

Suppose that $\dot{x} = f(x)$ has a hyperbolic fix point $\bar{x}$. Then there exist local stable and unstable manifold $W_{loc}^s(x)$ $W_{loc}^u(x)$ of the same dimension n_s, n_u as those of the eigenspace E^s, E^u of the linearized system and tangent to E^s, E^u at $\bar{x}$. $W_{loc}^s(x)$ $W_{loc}^u(x)$ are as smooth as the function f.

The stability boundary of the stability region is denoted by $\partial A(x_e^s)$. Based on some generic assumptions, we have the stability boundary theorem [79]:

Assumptions for Stability Boundary Theorem:

- All equilibria in $\overline{A(x_s^e)}$ are hyperbolic.
- Every trajectory in $\overline{A(x_s^e)}$ converges to an equilibrium point.
- The stable and unstable manifold of the equilibria in $\overline{A(x_s^e)}$ intersect

transversely.

Stability Boundary Theorem: [79]

The stability boundary $\partial A(x_e^s) = U_m W^s(x_m)$ *where* x_m*, m=1,2, …, are all equilibria of any order in* $\partial A(x_e^s)$.

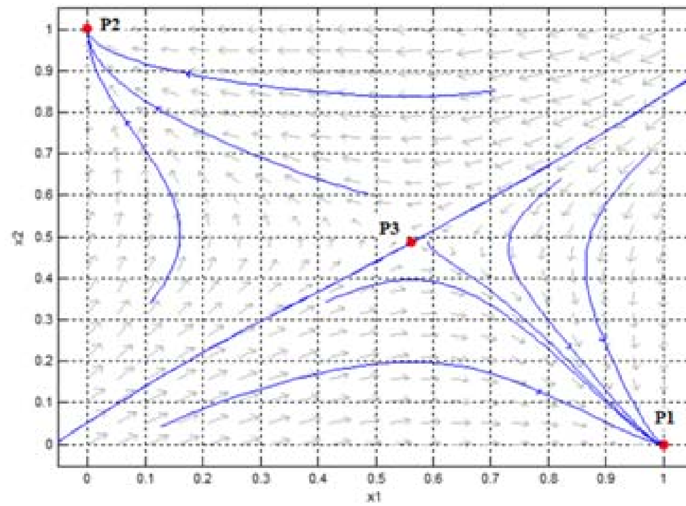


Fig. 6. 2 Example of phase portrait for an SRAM.

6.3.1.2. The Stable Manifold and Stability Boundary Theorem for SRAM

In particular case, from Fig. 6.2, P1 and P2 are two stable equilibrium points, x_e^s. The stability region of equilibrium point P1 is the region of all initial states whose trajectories will converge to P1. Accordingly, the stable region of P1 is the bottom right region in the phase portrait. Likewise, the stability region of P2 is the top left region of the phase portrait. The question remains on how to describe the stability region in a precise mathematical sense. From the same figure, we can see the stability boundary (the manifold passing through P3) naturally divides the state space into two stability regions. Accordingly, the stability boundary becomes one of the key components that decide the stability margin.

In SRAM case, stable equilibria are hyperbolic, every trajectory in $\overline{A(x_s^e)}$ converges to P3 and the stable and unstable manifold of P3 satisfies transversality. Thus, stability boundary theorem can be applied since SRAM satisfies the generic conditions. For the case of SRAM, saddle (P3) is the only one equilibrium on $\partial A(x_e^s)$, so the stability boundary is the stable manifold of saddle. Therefore, the stability boundary for SRAM can be described as:

$$\partial A(x_e^s) = W^s(x_e^u) \tag{6. 4}$$

where x_e^u is the unstable equilibrium point P3 on the boundary of A. Accordingly, to find the stability boundary, first is to identify the unstable equilibria on the stability boundary and find their stable manifolds. According to the Stable Manifold Theory [76], the stable eigenvectors of the linearized system around the equilibrium point will

be tangent to its corresponding stable manifold. Thus, we can start in a small neighborhood of x_e^u along the directions of stable eigenvector to integrate reverse in time to find the stable manifolds. We need to reverse in time to bypass the stability nature of the trajectories that will converge to x_e^u in a short distance.

As an example, Fig. 6.2 illustrates the above theorem. In Fig. 6.2, the trajectory pass through P3 is the separatrix that separate the state space into two stability regions. Points initially starts on the Separatrix will converge to P3, and the tangent vector on the Separatrix is the stable eigenvector with the stable Eigen-value of the linearized system around P3.

6.3.2. Algorithm on Finding the Two Dimentional Stability Boundary

Based on the stability boundary theorem and the stable manifold theorem, we can see for a two dimensional nonlinear systems such as SRAM, the stability boundary can be found by the following procedure:

1. Find all the x_e^u and x_e^s.
2. Focus on the interested x_e^s.
3. Check if x_e^u are on stability boundary.
4. Find the stable eigenvectors, V_s, of the equilibrium point x_e^u, where the stable eigenvector is the eigenvector corresponding to the stable eigenvalue.
5. Choose initial condition as $x_0 = x_e^u \pm \varepsilon \cdot V_s$, where ε is a small positive number.

6. Integrated backward by $\dot{x} = -f(x)$.

In practice, we can bypass procedures 4 and 5 as long as the initial conditions are nearby the unstable equilibria since the unstable components will dissipate fast as we integrate reverse in time. In 65nm technology SRAM as example, the unstable equilibrium point is (0.57, 0.57) and stable equilibrium points are (1,0) and (0,1). In order to find the stable and unstable eigenvectors of unstable equilibrium point, one way is finding out the Jacobian matrix addressed previously and evaluated at (0.57,0.57). This Jacobian matrix gives eigenvalues of ($1x10^{-11}$) and ($-1x10^{-11}$); the corresponding eigenvector are (0.707,-0.707) and (0.707,0.707). As mention before, the eigenvalue ($1x10^{-11}$) is positive, so it's unstable eigenvalue and the corresponding eigenvector (0.707,-0.707) is unstable eigenvalue; for the eigenvalue ($-1x10^{-11}$), its stable eigenvalue and the eigenvector (0707,0.707) would be stable eigenvector. This stable eigenvector would be the V_s described in step 4. By following the procedures, integrating backward from the unstable equilibrium point as described in step 6, the Separatrix can be traced out as shown in Fig. 6.3.

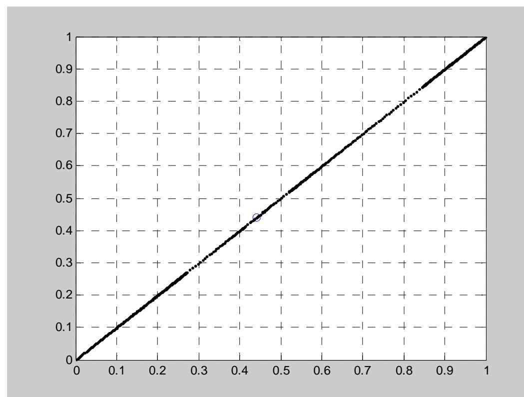
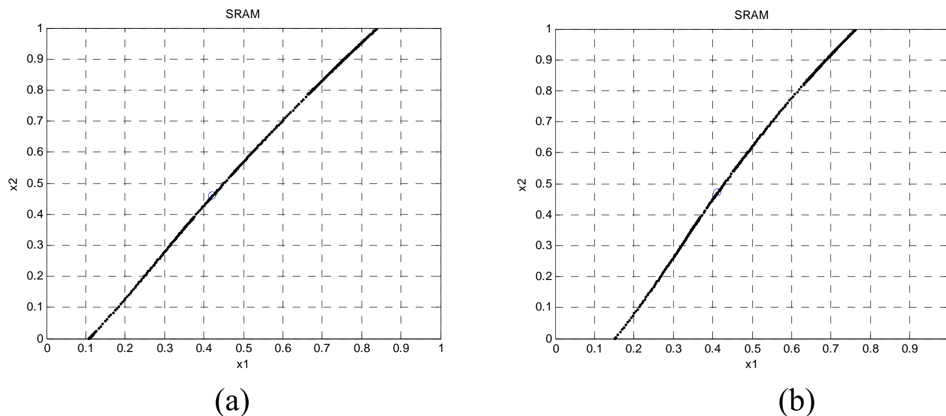


Fig. 6. 3 Separatrix of a 65nm SRAM cell

6.3.3. Higher Order Effect On the Curvature of Separatrix

The higher order effect regards to curvature of separatrix occurs often appears when the SRAM parameters are largely asymmetrically deviated. Using Level-1 model for demonstration, it appears to be that the separatrix would start to show nonlinearity if more than 50% deviation on a single threshold voltage or more than 15% on a *K* value. Since nonlinearity of separatrix is not showing so clear under varying a single parameter, we show a clear nonlinearity of separatrix in Fig. 6.4 by varying the thresholds in the manner of $V_{th1}=V_{th1nominal}*(1+n\%)$, $V_{th2}=V_{th2nominal}*(1+n\%)$, $V_{th3}=V_{th3nominal}*(1-n\%)$, $V_{th4}=V_{th4nominal}*(1-n\%)$, and Fig. 3-20 is varying *K* values in this manner, $K_1=K_{1nominal}*(1+n\%)$, $K_2=K_{2nominal}*(1+n\%)$, $V_{th3}=K_{3nominal}*(1-n\%)$, $K_4=K_{4nominal}*(1-n\%)$.



(a) (b)

Fig. 6. 4 The plot of separatrix varying only V_{th} values when n is (a) 60; (b) 80.

By comparing those figures, variation of thresholds larger seems to give the separatrix an "S" shape, and large variation of *K* values gives the separatrix in a "C" curve shape. Depends on the combination of thresholds and *K* values, the separatrix can be "S" or mirrored "S" shape and "C" or mirrored "C" shape. If put together with the

combinations from Fig. 6.4 and Fig. 6.5, the separatrix remains “C” shape for n=70 as shown in Fig. 6.6.

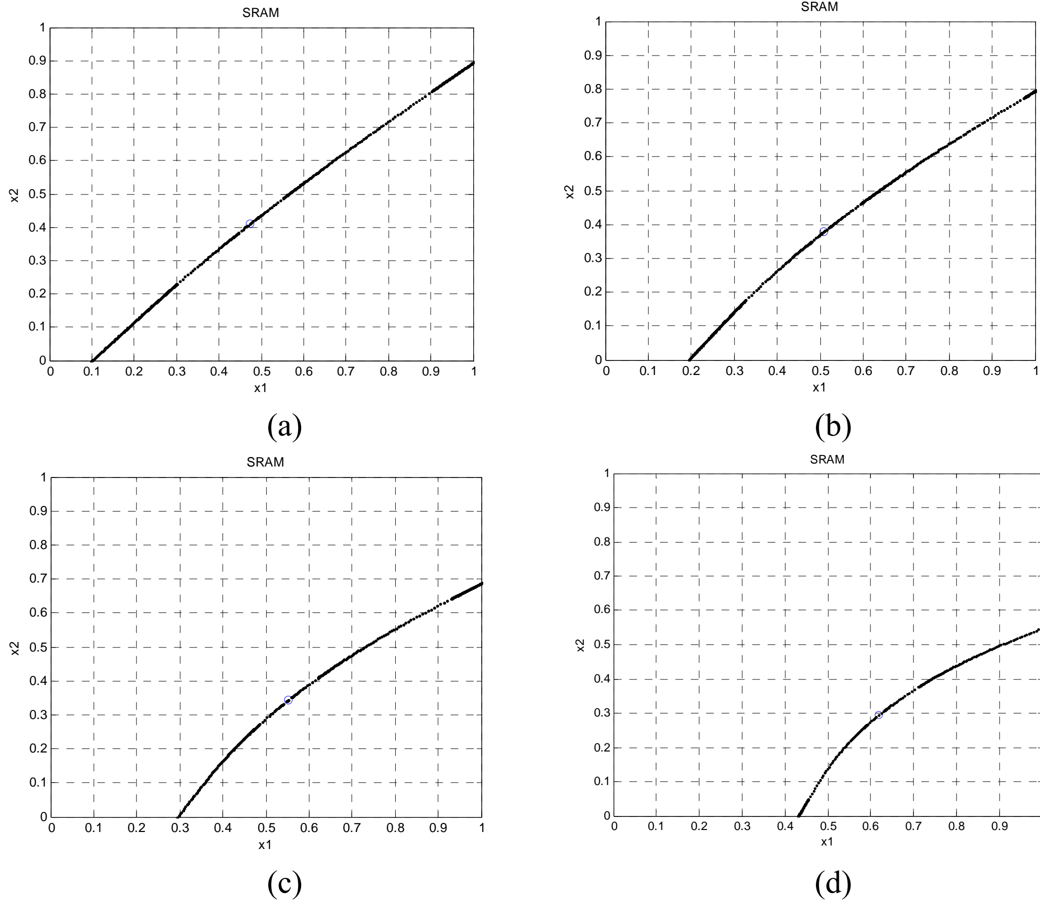


Fig. 6. 5 The plot of separatrix varying only K values when n is (a) 20; (b) 40; (c) 60; (d) 80.

6.3.4. The Mathematical Expression for The Separatrix

From the dynamic modeling equations of an SRAM, the slope of separatrix can be expressed by:

$$\frac{C_2 \cdot dV_2}{C_1 \cdot dV_1} = \frac{f_2(V_1, V_2)}{f_1(V_1, V_2)} \tag{6. 5}$$

or

$$\frac{dV_2}{dV_1} = \frac{C_1 \cdot f_2(V_1, V_2)}{C_2 \cdot f_1(V_1, V_2)} \tag{6. 6}$$

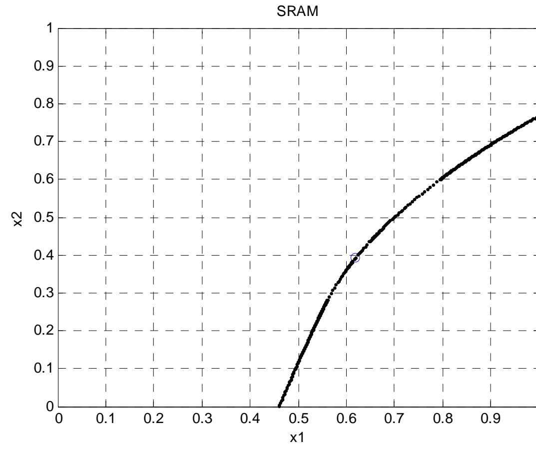


Fig. 6. 6 The plot of separatrix varying V_{th} and K Values at n=70.

where f_1 and f_2 are from (5.14). The mathematical expression of Separatrix can be acquired by solving (6.5). Assuming the points on Separatrix have all the four SRAM transistors in Saturation region, the Separatrix is solvable in Level-1 model [71]:

$$\begin{aligned}
&C_1 K_3 (V_{dd} - V_1 - Vth_3)^3 + C_1 K_4 (V_1 - Vth_4)^3 \\
&\quad - C_2 K_1 (V_{dd} - V_2 - Vth_1)^3 - C_2 K_2 (V_2 - Vth_2)^3 \\
&\qquad = C_1 (K_3 K_4^{3/2} + K_4 K_3^{3/2}) \cdot \left(\frac{(V_{dd} - Vth_3 - Vth_4)}{(\sqrt{K_3} + \sqrt{K_4})}\right)^3 \\
&\qquad\quad - C_2 (K_1 K_2^{3/2} + K_2 K_1^{3/2}) \cdot \left(\frac{(V_{dd} - Vth_1 - Vth_2)}{\sqrt{K_1} + \sqrt{K_2}}\right)^3
\end{aligned} \quad . \tag{6. 7}$$

For the special case, suppose the SRAM is symmetrical, meaning that $K_1=K_2=K_3=K_4$, $C_1=C_2$, $V_{thp}=V_{th1}=V_{th3}$ and $V_{thn}=V_{th2}=V_{th4}$, the separatrix becomes:

$$V_2 = V_1, \tag{6. 8}$$

which is 45° line passing through the origin on the phase portrait.

6.4. Noise Induced Bifurcation and SRAM Instability Study

As mentioned previously, SRAM state-flip can occur by introducing voltage or current perturbations. We use current sources and cross-coupled voltage sources to account all the different kind of noise perturbations, and SRAM instability can be observed by attaching them as shown in Fig. 6.7. It is also equivalent to Fig. 5.3.

The perturbation by either current or voltage sources can cause SRAM state-flip once the noise magnitude goes over the critical magnitude. When the injected noise amplitude changes, the equilibrium points will change accordingly. Stable equilibrium points remain in their relative positions while the saddle point moves closer to one of the equilibrium point, depending on the direction of the noise current. At certain critical magnitude, the saddle point will collide with a stable equilibrium point, resulting in a *saddle-node bifurcation*. The location that bifurcation occurs is called the bifurcation point. When this happens, the two colliding equilibrium points disappear, and only the other remaining stable equilibrium point will survive. The sections below discuss SRAM noise induced bifurcation by voltage and current perturbation separately.

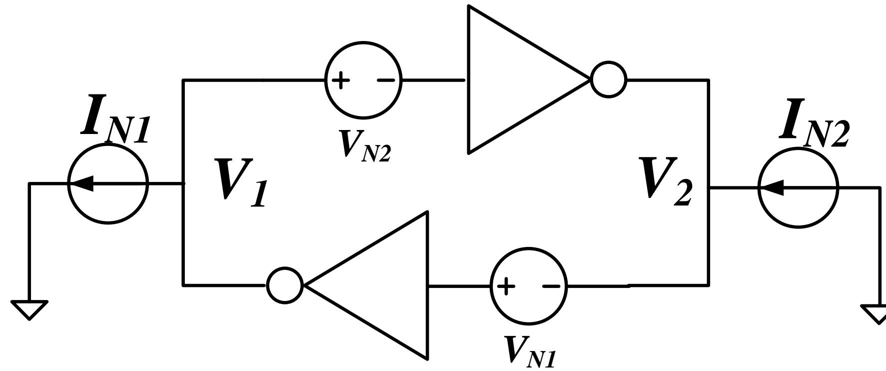


Fig. 6. 7 The SRAM topology with voltage and current noise sources incorporated (simplified view).

6.4.1. SRAM Instability Via Voltage Perturbation

The traditional static noise margin (SNM) introduces cross-coupled voltage sources and measures the maximum voltage magnitude an SRAM can handle at stored nodes. That is only considering the voltage sources V_{N1} and V_{N2} in Fig. 6.7. As discussed in Chapter V, the dynamic equations for SRAM with cross-coupled voltage sources are:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_1, V_2 + V_N) \\ C_2 \cdot \dot{V}_2 = f_2(V_1 - V_N, V_2) \end{cases} \tag{6. 9}$$

where $V_N = V_{N1} = V_{N2}$.

Figure 6.8 shows the voltage transfer curves and equilibrium points at different V_N. At V_N=0, the equilibria are labeled as “1”, “2” and “3”. Among these, “1” and “3” are stable equilibria and “2” the saddle. The dynamic property of the cell will change with injected voltages. As the magnitude of V_N increases to 0.14 volt, the three equilibra change their location as shown in Fig. 6.8(b). The saddle (marked as “2”) and the stable equilibrium point (marked as “3”) come closer to each other. In Fig. 6.8(c), the saddle

collapses with the stable equilibrium. The collapse results in saddle-node bifurcation [59]. The location where the bifurcation happens is called the *bifurcation point*, denoted by (V^V_{1B}, V^V_{2B}). In Fig. 6.8(d), the injected voltage magnitude increases to V_N=0.35 volt, yielding only one equilibrium point (marked as "1") in the entire state space. Starting from any point in the state space, the SRAM state will eventually go to this remaining stable equilibrium.

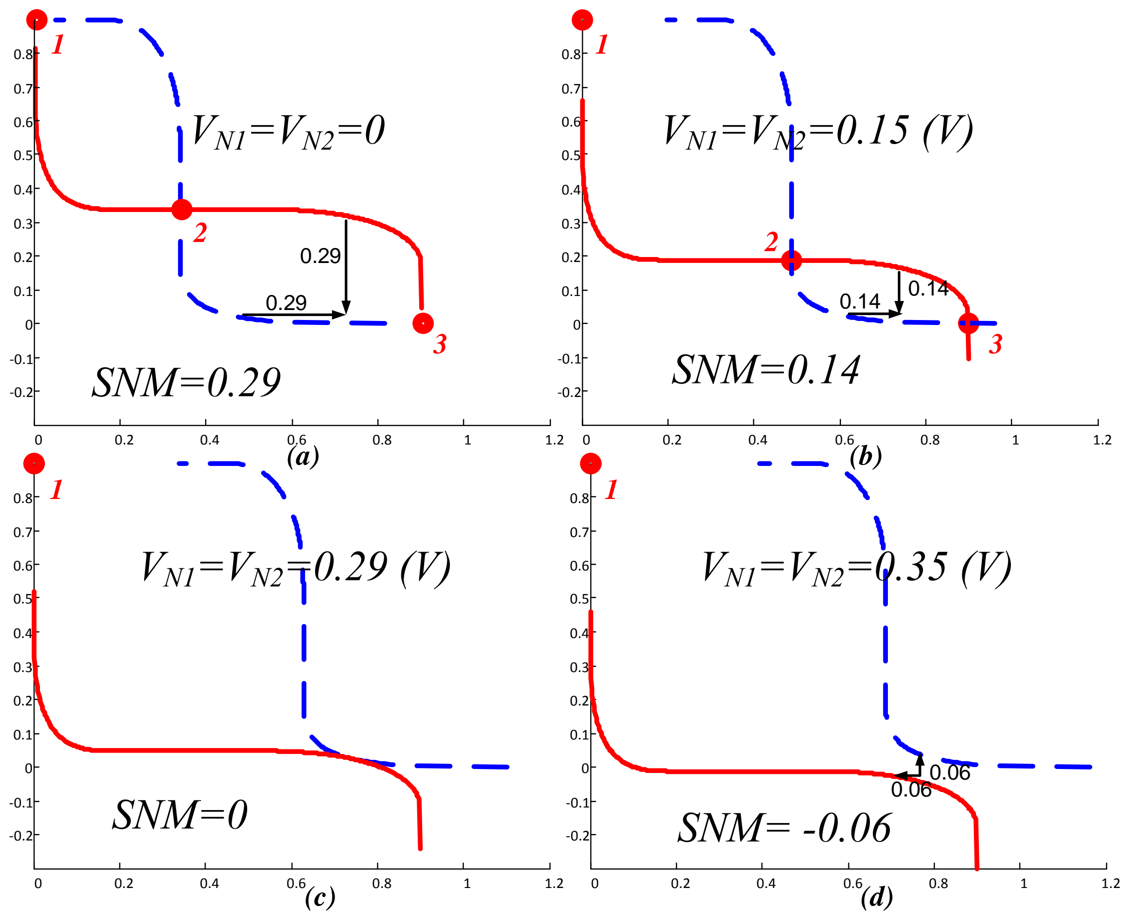


Fig. 6. 8 Illustration of saddle node bifurcation. The voltage transfer curves when (a) V_N is zero; (b) V_N is 0.15 volt; (c) V_N=0.29 volt; (c) V_N=0.35 volt.

As shown in Fig. 6.8(c), the occurrence of saddle-node bifurcation marks a critical structural change of the dynamic property of the SRAM cell. When the injected voltage V_N is above 0.29 volt, there is only one stable equilibrium. When the injected voltage V_N is less than 0.29 volt, there are still two stable equilibria. To flip the state, the injected DC (constant) voltage must be above 0.29 volt such that the starting stable equilibrium collapses with the saddle and hence disappears, and then the state anywhere on the phase portrait is attracted by the remaining stable equilibrium. We call SNM=0.29 volt the *critical voltage*.

The voltage transfer curves shit exactly by the amount of voltage injection. It can be seen from (6.9). Since the V_1-nullcine is all the points satisfied $f_1=0$, the new V_2 would be the old V_2 subtracts V_N and resulting the transfer curve shits down. Similarly, since the V_1-nullcine is all the points satisfied $f_2=0$, the new V_1 would be the old V_1 plus V_N and resulting the transfer curve shits to the right. There, that is why that SNM is determined as the side of largest square that can be inscribed between the mirrored DC voltage transfer curves (VTCs) of the cross-coupled inverters.

6.4.2. SRAM Instability Via Current Perturbation

Consider a constant noise input at the V_2 node, a representation of the system equations is given below:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_1, V_2) \\ C_2 \cdot \dot{V}_2 = f_2(V_1, V_2) + I_N \end{cases} . \quad (6.10)$$

Similar to the voltage case, saddle-note bifurcation will happen as the noise current, $I_{N,}$

increases. Figure 6.9 illustrates an example on the occurrence of noise induced bifurcation using current perturbation on V_2 node. As the injected current amplitude increased, the saddle node will gradually approach to the stable equilibrium state on the right side of the separatrix. When the noise amplitude reach the critical amplitude, the saddle point collides with the stable node, and the saddle node and the stable node along with separatrix disappear and result in a saddle-node bifurcation. In Fig. 6.9, the critical amplitude (I_C) is 192uA and equilibria colliding point (bifurcation point) is located at (1.7, 0.6). Once the noise magnitude goes larger than I_C, meaning $I_N>I_C$, the only equilibrium point left is the equilibrium point originally on the left side of separatrix.

Without losing the generality, the current perturbation can be classified into two categories: *Single-sided* and *double-sided*. The SRAM state flip by single-sided current injection has the following 4 scenarios:

- ***Four scenarios for single-sided current perturbation***

  Initial condition: (V_1='high', V_2='low')

  1. State-flip caused by current injection to the V_2 node, and its critical magnitude is denoted by I_{C2}^{IN}. It stands for critical current for going into V_2 node.
  2. State-flip caused by current leak out from the V_1 node, and its critical magnitude is denoted by I_{C1}^{OUT}. It stands for critical current for going out of V_1 node.

  Initial condition: (V_1='low', V_2='high')

3. State-flip caused by current injection into the V_1 node, and its critical magnitude is denoted by $\boldsymbol{I_{C1}^{IN}}$. It stands for critical current for going into the V_1 node.
4. State-flip caused by current extraction from the V_2 node, and its critical magnitude is denoted by $\boldsymbol{I_{C2}^{OUT}}$. It stands for critical current for going out of V_1 node.

The first scenario is already demonstrated in Fig. 6.9. For the other three scenarios, the transfer curves shift in different directions. On the other hand, the SRAM state flip by double-sided current injection has the following 4 scenarios:

- ***Four scenarios for double-sided current perturbation***

  Initial condition: (V_1='high', V_2='low')

5. SRAM state-flip occur caused by current injection to the V_2 node and leak out from the V_1 node.
6. SRAM state-flip occur caused by current injection to or leak out from to both V_1 and V_2 node.

Initial condition: (V_1='low', V_2='high')

7. SRAM state-flip occur caused by current injection to the V_1 node and leak out at V_2 node.
8. SRAM state-flip occur caused by current injection to or leak out from to both V_1 and V_2 node.

By the observation from the above eight scenarios, the SRAM state flip will NOT happen if current injected to a 'high' node or extract from a 'low' node.

In conclusion, this chapter studies the voltage and current perturbation induced bifurcation. In either case, voltage transfer curves of the two inverters in the cell become tangent to each other at bifurcation point. Evidently, two curves that are tangent to each other also have the same slope at that tangent point. It can be shown that the Jacobian matrix corresponding to the differential equation of the SRAM cell becomes singular at this point. This theoretical result is leveraged to develop analytical formulation.

Starting from Chapter VII, the process of analytical derivation for the critical current will be discussed. Critical current study has several benefits over critical voltage study: (1) the physical noise event is typically in current form (ex. SEU); (2) the SRAM operation is done by current biasing since transistors are voltage controlled current sources. Due to the above mentioned reasons, the noise margin metric in current representation has more advantage to work with in that sense.

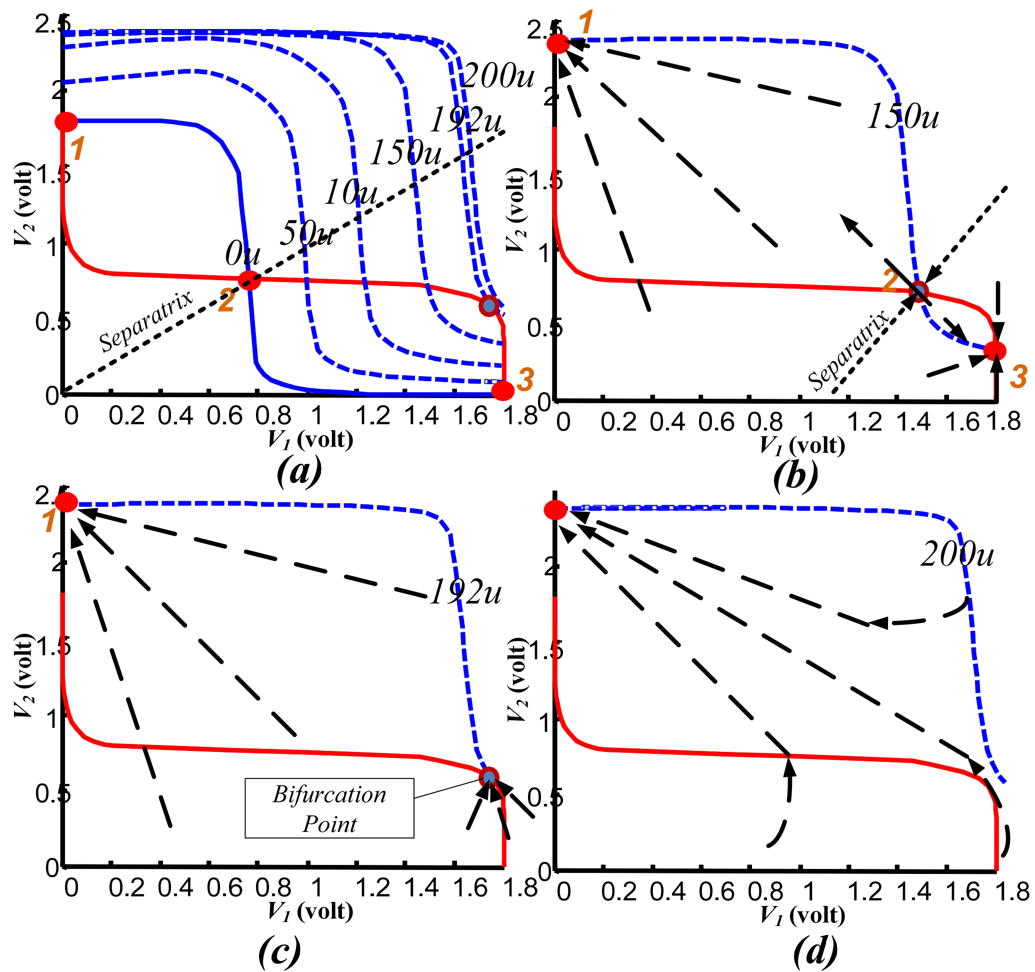


Fig. 6. 9 (a) Illustration of saddle node bifurcation as I_{n2} increases from zero to 200uA, (b) SRAM Butterfly curvewhen I_{n2}=150uA, (c) SRAM Butterfly curve when I_{n2}=192uA, (d) SRAM Butterfly curve when I_{n2}=200uA.

CHAPTER VII

THE ANALYTICAL SOLUTION FOR STATIC NOISE MARGIN VIA THE CONCEPT OF CRITICAL CURRENT *

To accurately account for transistor behaviors, sophisticated device models, e.g. BSIM3/4 models [80-84], are usually adopted. These device models, however, make it impossible to derive closed-form design models and prevent development of useful design insights. Instead, we adopt the popular simple Shichman-Hodges (Level-1) transistor models [69] [70] for developing the targeted dynamic stability models. This choice, nevertheless, allows us to rather accurately predict the trends of SRAM stability.

In order to derive analytical solution for critical current, the SRAM transistors' state at the point of instability must be known first. In this chapter, we newly introduce analysis by regions (also called region analysis) to know the region of bifurcation. Then, the transistors' state at the point of instability can also be known. Focus on the region of bifurcation; we derive the bifurcation point and I_C analytically. Furthermore, we extend the single-sided current injection to double-sided. Finally, we establish the static noise margin metric in current representation.

*©[2012] IEEE. Reprinted, with permission, from "Understanding SRAM Stability via Bifurcation Analysis," by Y. Ho, G. M. Huang, P. Li., A*CM Trans. Design Automation of Electronics and Systems*, accepted on May 19, 2014.

7.1. The Point of Instability for an SRAM

As mentioned in the previous chapter, voltage transfer curves shift by noise perturbation. The point of instability is when voltage transfer curves of the two inverters in the cell become tangent to each other at bifurcation point. Evidently, two curves that are tangent to each other have the same slope at that tangent point. It can be shown that the Jacobian matrix corresponding to the differential equation of the SRAM cell becomes singular at this point [85-86]. This theoretical result is leveraged to develop analytical formulation. Below summarizes this important theorem.

Theorem for the Point of SRAM Instability: [85-86]

For cross-coupled inverters like SRAM, the point of instability is when its Jacobian matrix becomes a singular matrix.

Proof:

Consider cross-coupled inverters with V_1 and V_2 variables as shown in Fig. 7.1(a). The static solutions for the cross-coupled inverters are the same as solving for nullclines as mentioned in (6.1) and (6.2). The following expressions established:

$$\begin{cases} V_2 = f(V_1) \\ V_1 = g(V_2) \end{cases} \tag{7. 1}$$

and

$$\begin{cases} C_1\dot{V}_1 = V_1 - g(V_2) = 0 \\ C_2\dot{V}_2 = V_2 - f(V_1) = 0 \end{cases}. \tag{7. 2}$$

The Jacobian matrix would be:

$$J = \begin{bmatrix} 1 & -\partial g/\partial V_2 \\ -\partial f/\partial V_1 & 1 \end{bmatrix}. \tag{7. 3}$$

If the Jacobian matrix is a singular matrix, its determinant would be zero as shown in the following:

$$\det(J) = 1 - \frac{\partial f}{\partial V_1}\frac{\partial g}{\partial V_2} = 0 \qquad (7.4)$$

Or

$$\frac{\partial f}{\partial V_1} = \frac{\partial V_2}{\partial g}. \qquad (7.5)$$

Equation (7.5) indicates the tangential point of two transfer curves have the same slope as shown in Fig. 7.1(b).

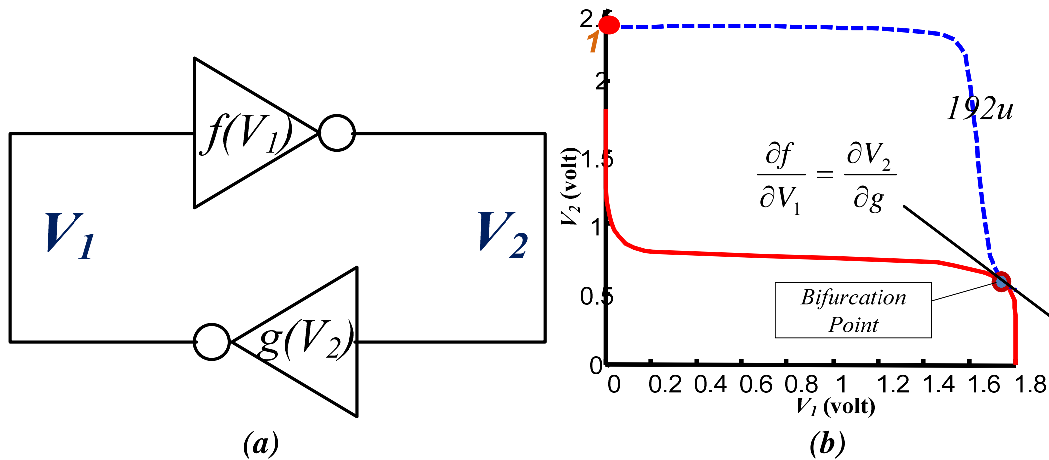


Fig. 7. 1 (a) Symbol for two cross-coupled inverters where functions *f* and *g* are for the top and bottom inverter; (b) Phase portrait plot showing two transfer curves tangent at bifurcation have the slope indicated.

7.2. The Region Analysis

The critical current is highly related to the bifurcation point since it causes equilibra to collapse. That is, the critical current can be found once the bifurcation point is known. In order to have analytical form expression for the bifurcation point and critical current, we introduce *region analysis* [71]. Each region in this analysis corresponds to one particular combination of transistor regions of operation (states) (e.g.

M1: Linear; M2: Cutoff; M3: Cutoff; M4: Linear). Through the region analysis, the transistor states at the bifurcation can be determined, and critical current can therefore be expressed in terms of system parameters.

7.2.1. The Defined Regions

The V_1 and V_2 voltages physically swing between zero to V_{dd}. This creates a state-space. The entire state space can partition into many small disjoint small areas. Figure shows the defined regions. In Fig. 7.2, each small area is a *region*. The lines separating the state space is based on the Shichman Hodges representation. In other words, every region has its corresponding dynamic equations, and certain $S(\cdot)$ terms are on or off in that particular region. Using Region 7 as an example, the transistor state combination [L,C;S,L] reads *M1=Linear, M2=Saturation, M3=Cutoff*, and *M4=Linear*. Every point in this region has such state combination, and the corresponding dynamic equations are:

$$\begin{cases} C_1\dot{V}_1 = f_1(V_1,V_2)\big|_{\mathrm{R7}} - I_{\mathrm{N1}} \\ C_2\dot{V}_2 = f_2(V_1,V_2)\big|_{\mathrm{R7}} + I_{\mathrm{N2}} \end{cases} \tag{7. 6}$$

where

$$\begin{cases} f_1(V_1,V_2)\big|_{R7} = I_{sdp1}{}^{LIN} - I_{dsn2}{}^{SAT} \\ f_1(V_1,V_2)\big|_{R7} = I_{sdp3}{}^{CUT} - I_{dsn4}{}^{LIN} \end{cases} \tag{7. 7}$$

and

$$\begin{aligned} I_{sdp1}{}^{LIN} &= K_1[(V_{DD} - V_2 - V_{TH1})^2 - (V_1 - V_2 - V_{TH1})^2]; \\ I_{dsn2}{}^{SAT} &= K_2(V_2 - V_{TH2})^2 \\ I_{sdp3}{}^{CUT} &= 0; \\ I_{dsn4}{}^{LIN} &= K_4[(V_1 - V_{TH4})^2 - (V_1 - V_2 - V_{TH4})^2] \end{aligned} \quad . \tag{7. 8}$$

Changing the threshold voltages or V_{dd} would shift the region lines and change the number of regions. As an example shown in Fig. 7.3, the state space would change from (a) to (b) by decreasing V_{dd}. As we can see that Regions 2A, 2B, 2C and 2D no longer exist. That means, the transistor combinations, which corresponds to those region, cannot happen under low V_{dd}. Further decrease of V_{dd} can make Region 2 disappear. When that happens, the output of one of the inverters will be floating.

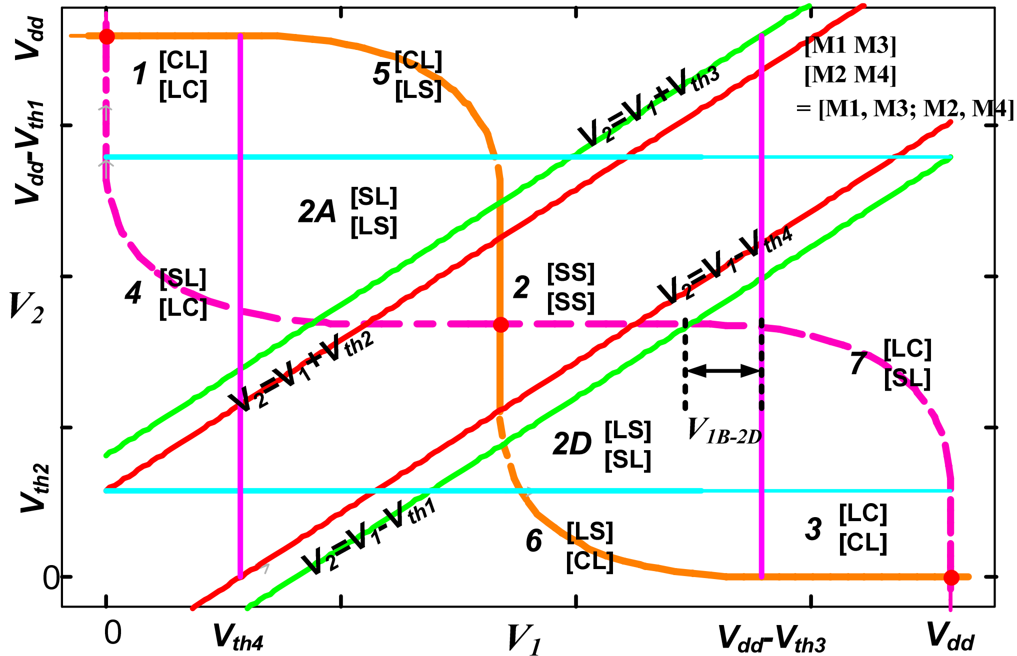


Fig. 7. 2 The nullclines and region formation of an SRAM. The $V_{1B\text{-}2D}$ is all the possible range for V_1 to have bifurcation in Region 2D. [C= Cutoff; L= Linear; S= Saturation.]

The equilibria of an SRAM cell, denoted as (V_{1e}, V_{2e}), are the solutions found by solving $dV_1/dt=0$ and $dV_2/dt=0$. When $I_{n1}=I_{n2}=0$, Region 1 and Region 3 each have a stable equilibrium strictly at (V_{dd}, 0) and (0, V_{dd}), and the saddle can fall onto one of the regions: 2A, 2B, 2, 2C, or 2D. For a symmetrical SRAM design, it can be shown that the

saddle is strictly located in Region 2. For convenience, we assume that the SRAM cell is symmetric, i.e. the two inverters in the cell are identical. The location of the saddle denoted by *($V_{1saddle}$, $V_{2saddle}$)* can be found to be:

$$\left(\frac{\sqrt{K_3}(V_{dd}-V_{th3})+\sqrt{K_4}V_{th4}}{\sqrt{K_3}+\sqrt{K_4}},\frac{\sqrt{K_1}(V_{dd}-V_{th1})+\sqrt{K_2}V_{th2}}{\sqrt{K_1}+\sqrt{K_2}}\right). \tag{7. 9}$$

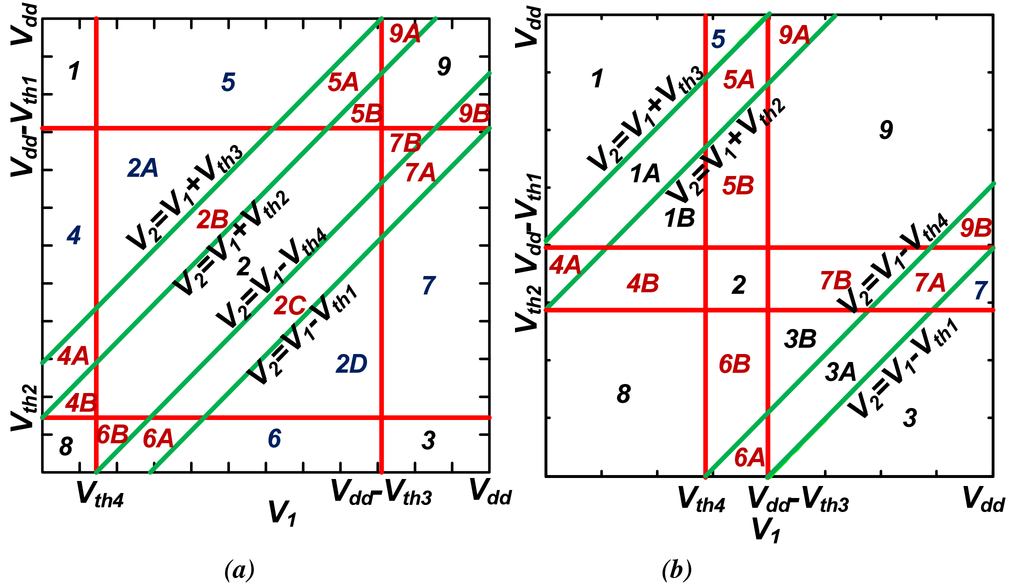
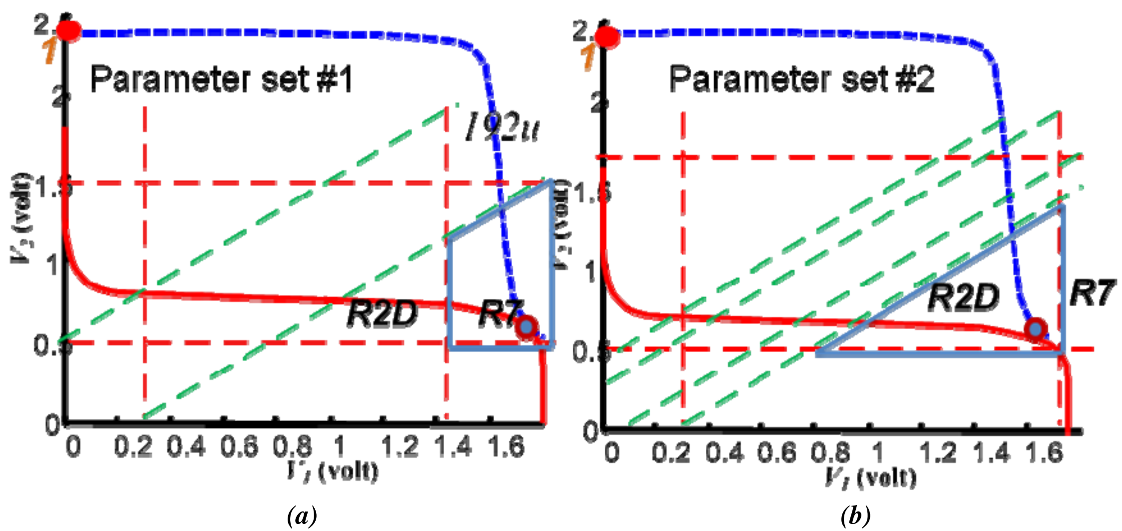


Fig. 7. 3 (a) An example of assigned regions for an SRAM; (b) the assigned regions when V_{dd} is reduced.

7.2.2. The Regions of Bifurcation

The region of bifurcation is the region where bifurcation happens, in other words, the region of bifurcation contains the bifurcation point. The bifurcation point may happen in different region for different parameter sets. Figure 7.4 shows an example of region of bifurcation for two different parameter sets. Parameter set #1 has the bifurcation point in Region 7, but the parameter set #2 has it in Region 2D.

Not all the regions in the phase portrait can happen to have bifurcation point. Majority of regions can never have bifurcation point for all possible parameter set. Exclude the regions cannot happen bifurcation are the regions able to find bifurcation for certain parameter sets. Those regions can have bifurcation are called *the candidate regions for bifurcation*, and only one region in the candidate regions is the region of bifurcation.



(a) *(b)*

Fig. 7. 4. The phase portrait for (a) parameter set#1 and (b) parameter set#2.

7.2.3. The Candidate Regions for Bifurcation

Every region can be classified of having 2, 1 or 0 equilibrium points (e.p.). For those regions can only have 0 e.p., the mathematical equations in that region cannot have any equilibrium solutions. For those regions can only have 1 e.p., the mathematical equations can be expressed in the first order form. The equilibrium solution can therefore be examined symbolically. Those regions can have more than one equilibrium point are the candidate regions of bifurcation; they are in the category of having 2

equilibrium points. The equation complexity reaches 4th order polynomial form for the candidate regions of bifurcation.

After examining all the regions for all possible parameter set, the candidate regions of bifurcation is summarized in Table 7.1. Based on the result, it shows that the region of bifurcation would not happen in the "*strap-regions*", meaning Regions 2, 2B, 2C, 4A, 4B, 5A, 5B, 6A, 6B, 7A, 7B, 8, 9, 9A and 9B combined in Fig. 7.2.

Table 7. 1 Summary of Region of Bifurcation

	INJECTION CONDITION	THE CANDIDATE REGIONS FOR BIFURCATION	THE REGION OF BIFURCATION BASED ON SYMMETRICAL DESIGN
Single-Side	$I_{N1}=0, I_{N2}>0$	*2D and 7*	*7*
	$I_{N1}=0, I_{N2}<0$	*2A and 4*	*4*
	$I_{N1}>0, I_{N2}=0$	*2D and 6*	*6*
	$I_{N1}<0, I_{N2}=0$	*2A and 5*	*5*
Double-Side	$I_{N1}>0, I_{N2}>0$	*2D, 3, 6, and 7*	*2D*
	$I_{N1}<0, I_{N2}<0$	*1, 2A, 4 and 5*	*2A*
	$I_{N1}<0, I_{N2}>0$	*2A, 2D, 5 and7*	$5(\|I_{N1}\|>\|I_{N2}\|)$, $7\ (\|I_{N1}\|<\|I_{N2}\|)$
	$I_{N1}>0, I_{N2}<0$	*2A, 2D, 4 and6*	$4(\|I_{N1}\|<\|I_{N2}\|)$, $6\ (\|I_{N1}\|>\|I_{N2}\|)$

7.2.4. Choose the Region of Bifurcation in the Candidate Regions

The region analysis eliminates all the impossible regions for bifurcation. However, it does not give the specific one region of bifurcation. Judgment based on transistor knowledge needs to be made to pick the region of bifurcation from the candidate regions. Using the first case as an example, we select Region 7 instead of Region 2D. Since transistor M3 is can only conduct negligible drain current in Region 2D, we assume it is in cutoff. By selecting Region 7 the region of bifurcation, we are taking the chances that M3 is in cutoff when bifurcation happens. In addition, this assumption is valid because bifurcation point is likely to be at the most curvy point of

the transfer curve and the curviest point is usually in Region 7. Here we complete the column for region of bifurcation assuming the SRAM is symmetrical designed.

7.3. The Analytical Solution for Critical Current

This section will show the complete derivation for analytical formula for critical currents. It has two main subsections: single-sided current injection and double-sided current injection cases.

The last chapter discussed total of eight scenarios, four on the initial condition of (V_1='high', V_2='low') and four on (V_1='low', V_2='high'), on current injection induced bifurcation. Once we get the analytical analysis for either one of the initial condition, we can flip the labels on the SRAM for the other initial condition without modified the analysis. In this work, we will work with the initial condition (V_1='high', V_2='low') only.

Assuming the initial condition ($V_{1o}=V_{DD}$, $V_{2o}=0$), SRAM state flip can happen if a noise current injects to V_2 node. The single-sided current injection has the dynamic equations in (6.10). We show the equations below for the readers:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_1, V_2) \\ C_2 \cdot \dot{V}_2 = f_2(V_1, V_2) + I_N \end{cases} \tag{7. 10}$$

where I_N is the injected noise current amplitude. The critical current for (7.10) is the magnitude of I_N at the point of instability. This critical current is labeled I_{C2}^{IN}, stands for current critical magnitude for injecting into V_2 node. In addition, the state flip can also

happen if there is a noise current going out of V_1 node, lowering the voltage V_1. Its dynamic equation is:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_1, V_2) - I_N \\ C_2 \cdot \dot{V}_2 = f_2(V_1, V_2) \end{cases} . \tag{7. 11}$$

Similarly, the critical current for (7.11) would be the magnitude of I_N in (7.11) at the point of instability; it is labeled I_{C1}^{OUT} for critical current magnitude going out of V_1 node.

On the other hand, the double-sided current injection has the dynamic equations in (5.14). We copy the equations here for readers:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_1, V_2) + I_{N1} \\ C_2 \cdot \dot{V}_2 = f_2(V_1, V_2) + I_{N2} \end{cases} . \tag{7. 12}$$

The critical current in double-sided case would be combinations of critical currents at V_1 and V_2 node, which are denoted by I_{C1} and I_{C2}. In this case, SRAM instability can be described by a line composed by combinations of I_{C1} and I_{C2}.

7.3.1. Single-Sided Current Injection

7.3.1.1. The Case When Current Injects to V_2 Node

The analytical expression of critical current involves solving for the bifurcation point in the region of bifurcation. Let the notation *f* and *g* be: $f=dV_1/dt$ and $g=dV_2/dt$. As illustrated previously, the system instability happens when the equilibria collapsed. It is proven that the Jacobian matrix becomes a singular matrix at bifurcation point. [85] Therefore, the following formulae can be established:

$$\begin{cases} f_{IN2} = f_1(V_1, V_2) = 0 \\ g_{IN2} = f_2(V_1, V_2) + I_N = 0 \end{cases} \quad (7.13)$$

where subscript "IN2" is added to the notation to indicate the case of current injected to V_2 node. The determinant of Jacobian matrix would be:

$$h_{IN2} = \left(\left(\partial f_{IN2} / \partial V_1\right) \cdot \left(\partial g_{IN2} / \partial V_2\right) - \left(\partial f_{IN2} / \partial V_2\right) \cdot \left(\partial g_{IN2} / \partial V_1\right) \right) = 0. \quad (7.14)$$

Let (V_{1B}^{IN2}, V_{2B}^{IN2}, I_{C2}^{IN}) be the solution of (V_1, V_2, I_N) satisfied the above f, g and h functions, where (V_{1B}^{IN2}, V_{2B}^{IN2}) is the bifurcation point for I_{C2}^{IN}. The problem becomes solving the three equations below for three variables (V_{1B}^{IN2}, V_{2B}^{IN2}, I_{C2}^{IN}):

$$\begin{cases} f_{IN2}(V_{1B}^{IN2}, V_{2B}^{IN2}, I_{C2}^{IN}) = f_1(V_{1B}^{IN2}, V_{2B}^{IN2}) = 0 \\ g_{IN2}(V_{1B}^{IN2}, V_{2B}^{IN2}, I_{C2}^{IN}) = f_2(V_{1B}^{IN2}, V_{2B}^{IN2}) + I_{C2}^{IN} = 0 \\ h_{IN2}(V_{1B}^{IN2}, V_{2B}^{IN2}, I_{C2}^{IN}) = \left(\left(\partial f / \partial V_1\right) \cdot \left(\partial g / \partial V_2\right) - \left(\partial f / \partial V_2\right) \cdot \left(\partial g / \partial V_1\right) \right)\Big|_{V_{1B}^{IN2}, V_{2B}^{IN2}} = 0 \end{cases} . \quad (7.15)$$

Below are the summarized steps to solve **(V_{1B}^{IN2},V_{2B}^{IN2},I_{C2}^{IN}):**
1. Determine the transistor states at bifurcation point.
2. Formulate continuous f_{IN2}, g_{IN2} and h_{IN2} function based on the transistor states from step 1, where f_{IN2} and g_{IN2} are the differential equations for the region of bifurcation and h_{IN2} as given by the singular Jacobian matrix.
3. Solve f_{IN2}=0 and h_{IN2}=0 for (V_{1B}^{IN2},V_{2B}^{IN2}) since f_{IN2} and h_{IN2} are independent of I_{C2}^{IN}.
4. Once the analytical form of (V_{1B}^{IN2},V_{2B}^{IN2}) is known, solve $g_{IN2}=0$ for I_{C2}^{IN}.

The above steps are applicable to any transistor models includes BSIM4 model. However, obtaining an analytical solution with complex transistor models is quite difficult. Hence, we use the simple Level-1 model to demonstrate.

Solving for (V_{1B}^{IN2}, V_{2B}^{IN2}) and I_C^{IN} symbolically in the Level-1 model is involved. The simplest analytical formula for I_{C2}^{IN} without any approximation is the following:

$$I_{C2}^{IN} = K_4[(V_{1B}^{IN2} - V_{TH4})^2 - (V_{1B}^{IN2} - V_{2B}^{IN2} - V_{TH4})^2] \quad (7.16)$$

where V_{1B} and V_{2B} are the bifurcation point can be expressed as follows:

$$V_{1B}^{IN2} = V_{2B}^{IN2} + V_{TH1} + \sqrt{(V_{DD} - V_{2B}^{IN2} - V_{TH1})^2 - \frac{K_2}{K_1}(V_{2B}^{IN2} - V_{TH2})^2} \qquad (7.\ 17)$$

$$V_{2B}^{IN2} = \frac{K_1(V_{DD} + V_{1B}^{IN2} - V_{TH1} - V_{TH4}) - K_2 \cdot V_{TH2}}{2(K_1 - K_2)} - \sqrt{\left(\frac{K_1(V_{DD} + V_{1B}^{IN2} - V_{TH1} - V_{TH4}) - K_2 \cdot V_{TH2}}{2(K_1 - K_2)}\right)^2 - \frac{K_1(V_{1B}^{IN2} - V_{TH1})(V_{1B}^{IN2} - V_{TH4})}{K_1 - K_2}}\ . \qquad (7.\ 18)$$

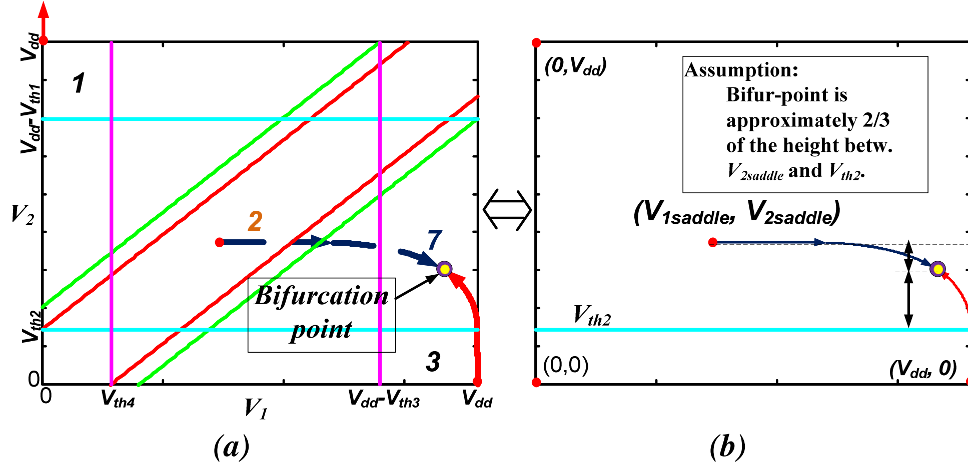


Fig. 7. 5 (a) The plot of SRAM equilibrium points as I_{n2} changes. Increasing the magnitude of I_{n2} will make the saddle (in region 2 when $I_{n2}=0$) collapsed with the stable node (in region 3 when $I_{n2}=0$) and resulting saddle node bifurcation in region 7; (b) Illustration showing that the bifurcation point is approximately 2/3 of the height between $V_{2saddle}$ and V_{th2} on the same phase portrait.

As can be seen, V_{1B}^{IN2} and V_{2B}^{IN2} are cross-coupled. Solving them would involve a 4th order polynomial, with polynomial roots having more than 10 symbolic terms.

Because the bifurcation point is always found in between $V_{2saddle}$ and V_{th2} as illustrated in Fig. 7.5(a), we simplified the expression for V_{2B}^{IN2} by approximating V_{2B}^{IN2} as a weighted sum of $V_{2saddle}$ and V_{th2} as: $w \cdot (V_{saddle} - V_{th2})$. The weighting factor w is chosen by averaging over more than 30 different parameter settings. It was observed that

the weight factor for the exact value of V_{2B} is within 8% of w=2/3 as illustrated in Fig. 7.5(b). With that, we have

$$V_{2B}^{IN2} = w\cdot(V_{2saddle} - V_{TH2}) + V_{TH2} \qquad w = 2/3 \tag{7. 19}$$

where $V_{2saddle}$ is

$$V_{2saddle} = \frac{\sqrt{K_1}(V_{DD} - V_{TH1}) + \sqrt{K_2}V_{TH2}}{\sqrt{K_1} + \sqrt{K_2}}. \tag{7. 20}$$

Therefore, the critical current, I_{C2}^{IN}, can be expressed in terms of system parameters by plugging the V_{1B}^{IN2} and V_{2B}^{IN2} expression given in (7.19) and (7.17) into (7.16).

7.3.1.2. The Case When Current Leaves at V_1 Node

This case deals with the dynamic equation in the form of (7.11). Increasing the magnitude of I_N would lower the stored voltage V_1, and SRAM state flip can happen if the magnitude of I_N is larger than the critical current, I_{C1}^{OUT}. Similar to the previous case, the bifurcation point and critical current can be acquired by solving:

$$\begin{cases} f_{OUT1}(V_{1B}^{OUT1}, V_{2B}^{OUT1}, I_{C1}^{OUT}) = f_1(V_{1B}^{OUT1}, V_{2B}^{OUT1}) - I_{C1}^{OUT} = 0 \\ g_{OUT1}(V_{1B}^{OUT1}, V_{2B}^{OUT1}, I_{C1}^{OUT}) = f_2(V_{1B}^{OUT1}, V_{2B}^{OUT1}) = 0 \\ h_{OUT1}(V_{1B}^{OUT1}, V_{2B}^{OUT1}, I_{C1}^{OUT}) = \left((\partial f/\partial V_1)\cdot(\partial g/\partial V_2) - (\partial f/\partial V_2)\cdot(\partial g/\partial V_1)\right)\Big|_{V_{1B}^{OUT1}, V_{2B}^{OUT1}} = 0 \end{cases} \tag{7. 21}$$

Below are the summarized steps to solve **($V_{1B}^{OUT1}, V_{2B}^{OUT1}, I_{C1}^{OUT}$):**

1. Determine the transistor states at bifurcation point.
2. Formulate continuous f_{OUT1}, g_{OUT1} and h_{OUT1} function based on the transistor states from step 1, where f_{OUT1} and g_{OUT1} are the differential equations for the region of bifurcation and h_{OUT1} as given by the singular Jacobian matrix.
3. Solve g_{OUT1}=0 and h_{OUT1}=0 for $(V_{1B}^{OUT1}, V_{2B}^{OUT1})$ since g_{OUT1} and h_{OUT1} are independent of I_{C1}^{OUT1}.
4. Once the analytical form of $(V_{1B}^{OUT1}, V_{2B}^{OUT1})$ is known, solve $f_{OUT1}=0$ for I_{C1}^{OUT1}.

Similar to the previous case, step 3 also runs into complicated expression and requires solving 4th order polynomial. We again use the idea of weighting factor $w=2/3$ to simplify the expression for V_{1B}^{OUT1} by approximating V_{1B}^{OUT1} as a weighted sum of $V_{1saddle}$ and $V_{DD} - V_{TH3}$. With that, we get:

$$V_{1B}^{OUT1} = \left(V_{DD} - V_{TH3}\right) - w \cdot \left(V_{DD} - V_{1saddle} - V_{TH3}\right), \; w = 2/3, \quad (7.22)$$

and the expression for the critical current would be:

$$I_{C1}^{OUT1} = K_1 \cdot \left[\left(V_{DD} - V_{2B}^{OUT1} - V_{TH1}\right)^2 - \left(V_{1B}^{OUT1} - V_{2B}^{OUT1} - V_{TH1}\right)^2\right] \quad (7.23)$$

where

$$V_{2B}^{OUT1} = V_{1B}^{OUT1} - V_{TH4} - \sqrt{\left(V_{1B}^{OUT1} - V_{TH4}\right)^2 - \frac{K_3}{K_4} \cdot \left(V_{DD} - V_{1B}^{OUT1} - V_{TH3}\right)^2}. \quad (7.24)$$

7.3.2. Double-Sided Current Injection

For the case of double-sided current injection, the following formulae can be established:

$$\begin{cases} f = f_1(V_1, V_2) - I_{N1} = 0 \\ g = f_2(V_1, V_2) + I_{N2} = 0 \\ h = \left(\partial f / \partial V_1\right) \cdot \left(\partial g / \partial V_2\right) - \left(\partial f / \partial V_2\right) \cdot \left(\partial g / \partial V_1\right) = 0 \end{cases}. \quad (7.25)$$

Let ($V_{1B}, V_{2B}, I_{C1}, I_{C2}$) be the solution of ($V_1, V_2, I_{N1}, I_{N2}$) satisfied the above *f, g* and *h* functions, where (V_{1B}, V_{2B}) is the bifurcation point and (I_{C1}, I_{C2}) are the critical currents. In the case, there can be many set of ($V_{1B}, V_{2B}, I_{C1}, I_{C2}$) for one system parameter, but one (I_{C1}, I_{C2}) set will only correspond to one bifurcation point (V_{1B}, V_{2B}) and vice-versa. The problem becomes solving the following three equations for four variables ($V_{1B}, V_{2B}, I_{C1}, I_{C2}$):

$$\begin{cases} f(V_{1B},V_{2B},I_{C1},I_{C2}) = f_1(V_{1B},V_{2B}) - I_{C1} = 0 \\ g(V_{1B},V_{2B},I_{C1},I_{C2}) = f_2(V_{1B},V_{2B}) + I_{C2} = 0 \\ h(V_{1B},V_{2B},I_{C1},I_{C2}) = \left((\partial f/\partial V_1)\cdot(\partial g/\partial V_2) - (\partial f/\partial V_2)\cdot(\partial g/\partial V_1)\right)\Big|_{V_{1B},V_{2B}} = 0 \end{cases} \quad . \qquad (7.\ 26)$$

Since there can be many sets of (I_{C1}, I_{C2}) satisfied the above three questions, we call the solutions the *combinations of critical currents*.

7.3.2.1. The Combinations of Critical Currents

Table 7.2 shows the combinations of critical currents in a 65nm technology process symmetrical designed SRAM, and Fig 7.6 shows their location graphically. The combinations of I_C is a continuous curve close to a straight line in a symmetrical SRAM. When the SRAM is asymmetrical, some nonlinearity can be observed on the line of combinations of IC.

Evidently, (0, I_{C2}^{IN}) and (I_{C1}^{OUT}, 0) from single-sided case are the cross point of the line of combinations of IC and y-axis and x-axis. Because $I_{C2}^{(7)}$=71uA is measured at zero I_{N1}, $I_{C2}^{(7)}$ in this example is the same as I_{C2}^{IN} and its analytical formula is already derived. Similarly, $I_{C1}^{(7)}$=18.2uA is the same as I_{C1}^{OUT}. We also have the analytical solution for that. However, the analytical formula for other points on the combinations of IC plot are unknown.

The combinations of IC also include negative I_{C1} and I_{C2} as long as *f*, *g* and *h* are satisfied, so the IC line in Fig. 7.6(a) can be extended to quadrant II and quadrant IV. If I_{C1} is negative, that means current is injecting into V_1 node and raise the stability at V_1 node. Thus, I_{C2} goes to a higher value than I_{C2}^{IN} when I_{C1} is negative.

Table 7.2. The BSIM4 Data on a 65nm Technology SRAM (unit is μA)

[$I_{C1}(0)$=	0	, $I_{C2}(7)$=	71	]	[$V_{1B}(0,7)$=	0.86	, $V_{2B}(0,7)$=	0.26	]
[$I_{C1}(1)$=	3.242	, $I_{C2}(6)$=	60	]	[$V_{1B}(1,6)$=	0.8	, $V_{2B}(0,7)$=	0.233	]
[$I_{C1}(2)$=	5.857	, $I_{C2}(5)$=	50	]	[$V_{1B}(2,5)$=	0.751	, $V_{2B}(0,7)$=	0.202	]
[$I_{C1}(3)$=	8.305	, $I_{C2}(4)$=	40	]	[$V_{1B}(0,7)$=	0.7	, $V_{2B}(0,7)$=	0.168	]
[$I_{C1}(4)$=	10.699	, $I_{C2}(3)$=	30	]	[$V_{1B}(0,7)$=	0.651	, $V_{2B}(0,7)$=	0.132	]
[$I_{C1}(5)$=	13.108	, $I_{C2}(2)$=	20	]	[$V_{1B}(0,7)$=	0.6	, $V_{2B}(0,7)$=	0.097	]
[$I_{C1}(6)$=	15.607	, $I_{C2}(1)$=	10	]	[$V_{1B}(0,7)$=	0.546	, $V_{2B}(0,7)$=	0.0627	]
[$I_{C1}(7)$=	18.22	, $I_{C2}(0)$=	0	]	[$V_{1B}(0,7)$=	0.48	, $V_{2B}(0,7)$=	0.0274	]

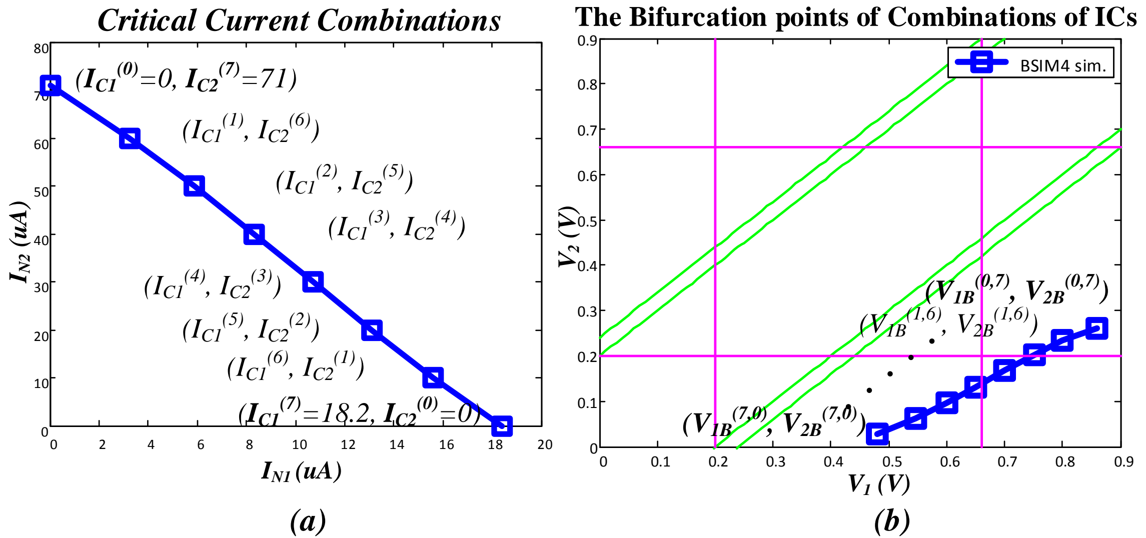


Fig. 7. 6 The plot of (a) combinations of combinations of critical currents, and its (b) corresponding bifurcation point locations.

7.3.2.2. The Analytical Solution to the Combinations of Critical Currents

The straight forward way is to write I_{C2} in terms of I_{C1} in (7.26), and I_{C2} can be traced by sweeping I_{C1}. Or, write I_{C1} in terms of I_{C2} and sweeping I_{C2} can also get the same result. However, the drawback is that f_1 and f_2 functions need to be updated to a different region equations as the bifurcation point get into another region. As shown in Fig. 7.6(b), the bifurcation points are not all in one region; the region equations need to be changed accordingly.

7.3.2.3. The Linear Approximation on the Combinations of Critical Currents

One simple way to acquire the analytical formula for the line of combinations of critical current is using the linear approximation. Although the line of IC combinations can have higher order effect, the line remains as a continuous curve close to a "straight line" in most of parameter sets as shown in Fig. 7.6(a).

We already know two points on the IC line; they are (0, I_{C2}^{IN}) and (I_{C1}^{OUT}, 0). Their analytical formula was derived previously. A linear line passes these two points can be described by the following equation:

$$I_{C2} = -\frac{I_{C2}^{IN}}{I_{C1}^{OUT}} I_{C1} + I_{C2}^{IN} \tag{7. 27}$$

where I_{C1}^{OUT} and I_{C2}^{IN} are expressed in (7.23) and (7.16).

7.4. Static Noise Margin Metric in Current Representation

Based on the results from single-sided and double-sided current injection case, one important phenomenon can be concluded, the combination of IC works as a stability boundary. SRAM state would flip if the injected noise combination, (I_{N1}^{0}, I_{N2}^{0}), is above the line of combination of ICs, and state flip cannot happen if the noise combination is below the line.

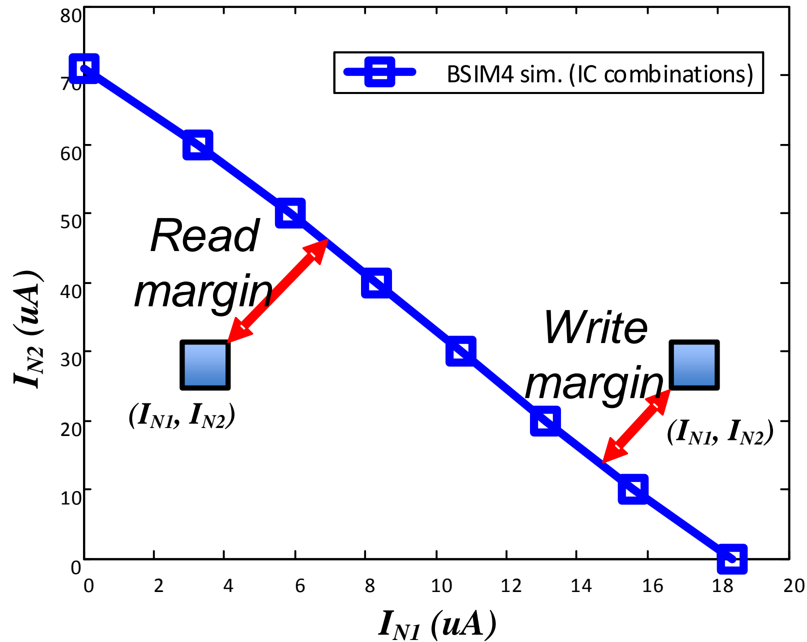


Fig. 7. 7 Illustration of read/write noise margin

The traditional static noise margin uses an inscribable largest square fitted inside the "eye" of transfer curves to describe the stability of an SRAM state. The better the stability means the larger the square is. On the other hand, the concept of critical current can also provide the same useful noise margin metric. The noise margin in current representation is defined as follows:

The Definition of SNM Read Margin in Current Representation:
- Suppose the injected noise combination (I_{N1}, I_{N2}) is below the critical current combination line. The shortest distance from (I_{N1}^{0}, I_{N2}^{0}) to the critical current combination is the read margin.

The Definition of SNM Write Margin in Current Representation:
- Suppose the noise combination (I_{N1}, I_{N2}) is above the critical current combination line. The shortest distance from (I_{N1}, I_{N2}) to the critical current combination is the write margin.

Figure 7.7 demonstrates the definition above graphically. The shortest distance away from the boundary gives designer an idea of how far away the perturbed SRAM state to the state of instability. The longer the distance is, the better the stability it has. Figure 7.8 summarized the SRAM read/write margin in voltage and current representation. This newly defined metric can work as a design guidance and provide physical insights. The noise margin in current presentation can have a few advantages over the voltage representation:

1. *The device noises are often described in current form.*

   In electronics, noise is a random fluctuation in an electrical signal. There are various type of noise in electronics circuits. The common one in memory devices is call Single-Event-Upset (SEU). A SEU noise changes the state by ions or electro-magnetic radiation striking a sensitive node in a microelectronics device. In other words, the state change is a result of the free charge created by ionization, and its mathematical model is a current waveform which has been discussed in (4.1).

2. *The SRAM access transistors are current driving sources*

   Transistors are voltage controlled current source. The SRAM operations rely on pass-gates driving currents. Therefore, the SNM in current representation is better associated with SRAM read/write stability.

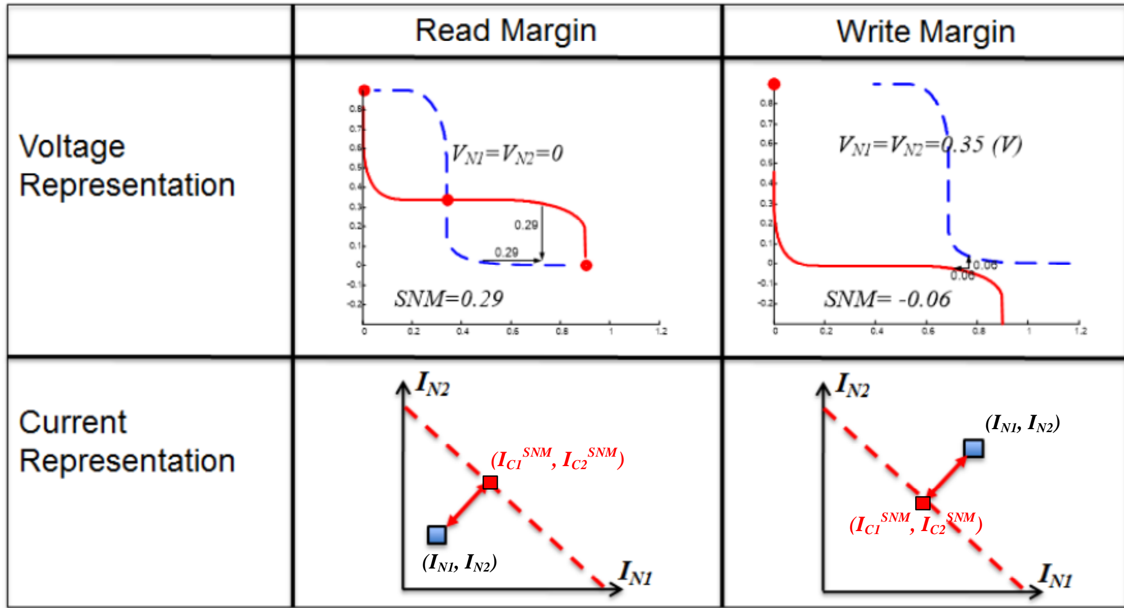


Fig. 7. 8 The summary of static noise margin in voltage representation and in current representation.

7.5. The Analytical Solution for Read/Write Noise Margin In Current Representation

The definition of noise margin in current representation is the shortest distance to the line of combination of critical current. The shortest distance would be in the direction perpendicular to the line of combination of IC in linear assumption. And, the analytical formula for the length of the shortest distance can be acquired. The mathematical expression for the linear approximated IC combination line is given in (7.27), and its perpendicular line equation passing through the injected noise current combination (I_{N1}^0, I_{N2}^0) would be:

$$I_{C2} = \frac{I_{C1}^{OUT}}{I_{C2}^{IN}}(I_{C1} - I_{N1}) + I_{N2}\,. \tag{7. 28}$$

The shortest distance point on the line of combination of IC is denoted as (I_{C1}^{SNM}, I_{C2}^{SNM}); its mathematical expression is derived to be:

$$\left(I_{C1}^{SNM}, I_{C2}^{SNM}\right) = \begin{pmatrix} \dfrac{\left(I_{C1}^{OUT}\right)^2 \cdot I_{N1} + I_{C1}^{OUT} I_{C2}^{IN} \cdot \left(I_{C2}^{IN} \cdot - I_{N2}\right)}{\left(I_{C1}^{OUT}\right)^2 + \left(I_{C2}^{IN}\right)^2}, \\ \dfrac{\left(I_{C2}^{IN}\right) \cdot \left(I_{C2}^{IN} \cdot I_{N2} - I_{C1}^{OUT} I_{N1} + \left(I_{C1}^{OUT}\right)^2\right)}{\left(I_{C1}^{OUT}\right)^2 + \left(I_{C2}^{IN}\right)^2} \end{pmatrix}. \quad (7.\ 29)$$

Finally, the analytical solution for the SNM in current representation is:

$$SNM = \sqrt{\left(I_{N1} - I_{C1}^{SNM}\right)^2 + \left(I_{N2} - I_{C2}^{SNM}\right)^2} \quad (7.\ 30)$$

or

$$SNM = \frac{\left| I_{N2} + \dfrac{I_{C2}^{IN}}{I_{C1}^{OUT}} \cdot I_{N1} - I_{C2}^{IN} \right|}{\sqrt{1 + \left(I_{C2}^{IN} / I_{C1}^{OUT}\right)^2}}. \quad (7.\ 31)$$

CHAPTER VIII

THE ANLAYTICAL SOLUTION FOR DYNAMIC NOISE MARGIN VIA THE CONCEPT OF CRITICAL TIME *

As discussed previously, if the injected noise (I_{N1}, I_{N2}) is below the line of combinations of I_C, the states will never cross the separatrix, so when the noise disappears, the states of the cell will always return to its stable equilibrium point. However, the static noise margin is not good enough to characterize the noise tolerance of this cell. The noise current above the line not necessarily implies that the cell will flip its state [59] [71] [76]. It must be above the line for a certain period of time (defined as critical time or T_C). Once the state of the cell crosses the separatrix, the cell will flip states even though the noise disappears. For state flip to occur, the state of SRAM must cross the separatrix. The critical time or $T_{critial}$ defined to be the time it takes from initial state to the separatrix. If the present of noise current with amplitude $I_{critial}$ has shorter duration than $T_{critial}$, the state has not yet crossed the separatrix, and it will come back when the noise disappear. On the other hand, the presence of noise has greater duration over $T_{critial}$, the state of SRAM would cross the separatrix, and state flip is inevitable even though disturbance is gone.

*©[2012] IEEE. Reprinted, with permission, from "Understanding SRAM Stability via Bifurcation Analysis," by Y. Ho, G. M. Huang, P. Li., A*CM Trans. Design Automation of Electronics and Systems*, accepted on May 19, 2014.

In this chapter, the definition of dynamic noise margin will be clearly stated. The analytical solution for the dynamic noise margin will be provided.

8.1. The Definition of Dynamic Noise Margin (DNM)

The definition of dynamic noise margin is clearly stated in [53]. Using the concept of stability boundary, the dynamic noise margin can be defined in read, write and hold.

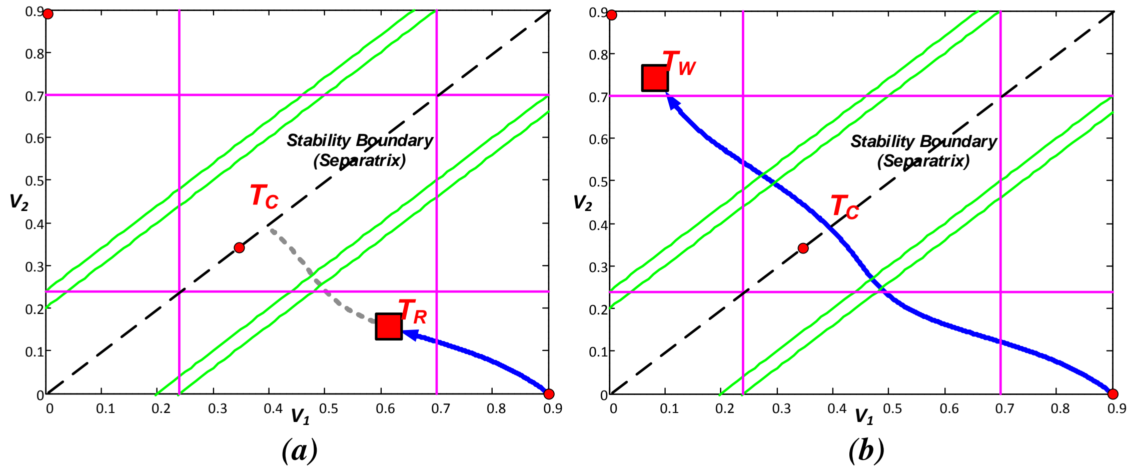


Fig. 8. 1 The definition of dynamic noise margin: (a) dynamic read margin and (b) dynamic write margin.

8.1.1. Dynamic Noise Margin in Read

When the read operation starts, the word-line goes high, the SRAM state would be pushed away from its initial state towards the separatrix of the cell. After the word-line goes off, the read operation ends and the cell returns to hold. If the trajectory does indeed go across the separatrix, a state flip will be generated after the access transistors are turned off in hold.

The read DNM is defined for a given wordline pulse width T_R. As shown in Fig. 8.1 (a), the read DNM is defined as

$$DNM_{READ} = T_C - T_R \tag{8. 1}$$

where T_C is the time it takes for the trajectory to reach the separatrix and T_R is a give word-line pulse width. The defined read DNM specifies the amount of read operation time margin before read instability takes place. That is, when $T_C > T_R$, there exists a positive margin; when $T_C = T_R$, the cell is on the verge of read instability; when $T_C < T_R$, state-flip happens and the cell loses read stability.

8.1.2. Dynamic Noise Margin in Write

The write DNM can be defined in a way analogous to that of the read DNM, but by noting that a successful write overwrites the SRAM state, hence producing a state flip. Similar to the previous case, as shown in Fig. 8.1 (b), T_C is the time when the state trajectory crosses the separatrix. For a given word-line pulse width, T_W, the write DNM is defined

$$DNM_{WRITE} = T_W - T_C\,. \tag{8. 2}$$

The static noise margin (SNM) may provide an optimistic estimate for dynamic write-ability. That is, even if the SNM predicts a successful write, in the reality, the write can actually fail. For the state-of-the-art SRAM designs with short access cycles and advanced read/write timing control circuitry, the distinctions between the SNMs and DNMs in read and write reveal the important role of cell nonlinear dynamics in determining dynamic SRAM stability.

8.1.3. Dynamic Noise Margin in Hold

The DNM in hold characterizes the data retention property of the cell under SEUs and noisy operating condition. DNM may be examined by injecting a current disturbance into the cell. Compared with the use of noise voltage disturbance in the SNM [84-85], modeling the disturbance as an injected current more physically reflects the nonlinear dynamic nature of the cell. The DNM shall be evaluated by considering both the amplitude and duration of the current disturbance. Depending on these two factors, the state trajectory in hold may cross the separatrix, leading to instability. It would be the same as the read scenario, with T_R replace by the disturbance duration.

8.2. The SRAM Cell Dynamics and Analytical Solution For Dynamic Noise Margin

Previous chapters discussed the SRAM cell in static point of view. The SRAM cell reaches its point of instability when the magnitude of external perturbation (such as noise currents and noise voltages) reaches the critical state. In this chapter, we will discuss the dynamic point of view. We will show how the stored state flip over. When under constant current (I_{N1}, I_{N2}) biasing, an initial state (V_{DD}, 0) will traverse across the stability boundary (separatrix) and reach another equilibrium state (0, V_{DD}).

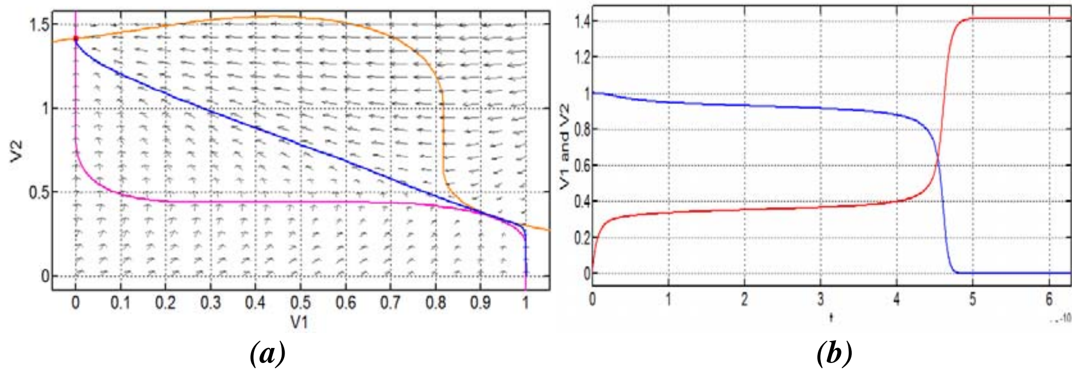
8.2.1. The SRAM Cell Trajectory on Phase Portrait

Figure 8.2(a) shows an example of stored state switching mechanism if consider only a current injection at V_2 node, its differential equations are described in (7.10). Assume this noise acts as a step input to V_2 node, which holds constant without

switching off. On the phase portrait, a trajectory starts from (1, 0) and gradually converge to the equilibrium point on (0, 1.4). From simulation result, the saddle-node bifurcation happens at approximately I_N of 496 μA, so I_C would be 496 μA. Because in this case I_N is 500 μA which is slightly larger than I_C, there is only one equilibrium point located at *(0, 1.4)* on the entire phase portrait. So, if the cell's states initially start at *(1, 0)*, the state of the cell will be converging to *(0, 1.4)*. When plotting V_1 and V_2 in time diagram as shown in Fig. 8.2(b), one can see that it takes approximately 0.48 ns for the cell to reach the equilibrium point *(0, 1.4)* which results a state flip. Since it is symmetrical designed, the separatrix is simply the linear line $V_1 = V_2$ [59] [71] [76] across the origin. It will take the cell about 0.45 ns to reach the separatrix. After the state of the cell crosses over the separatrix, the cell will not be able to come back to its original state. This means that a noise current pulse of constant amplitude 500 μA applied for less than 0.45 ns may not make the cell flip its state. However, when the noise duration is longer than 0.45 ns, the cell will flip its state. Therefore, 0.45ns is the T_C in this case. In addition, note that the transition time from the separatrix to the other equilibrium is only 0.03ns, which is only 1/15 fraction of the total transition time (.45ns), but the traveled distance is relatively long within such a short period of time.

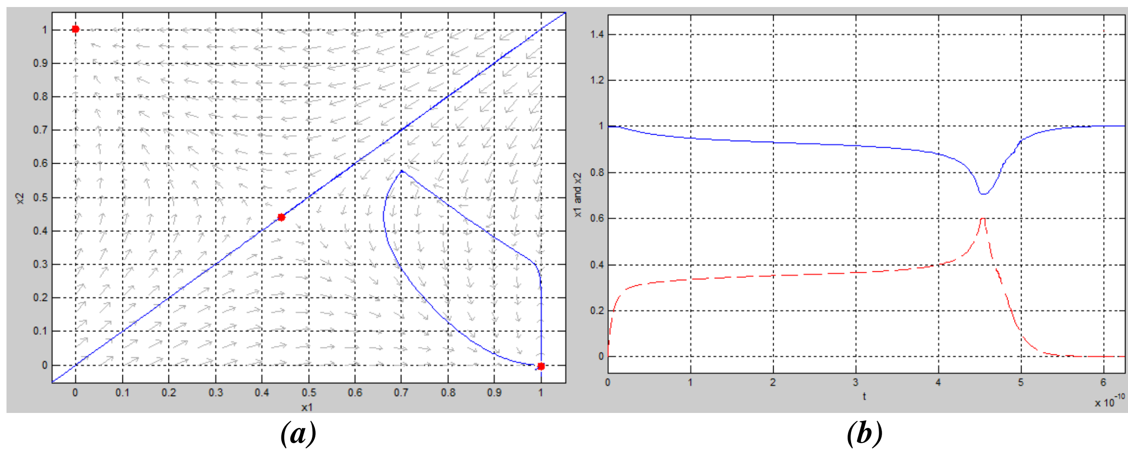
Consider a type of square pulse noise that has constant amplitude of 500 μA and its duration is only last 0.43ns. The cell state will not flip because the duration is less than T_C. From Fig. 3-11(b), the cell state is (0.7,0.582) at 0.43ns. Since the separatrix in this example is a straight line $V_1=V_2$ passing through the origin, after the noise is gone, the cell state (0.7, 0.582) is in the bottom right region of attraction of the equilibrium

point *(V_{dd},0)*. The cell state will go back to *(V_{dd},0)* gradually as shown in Fig. 8.3.



(a) ***(b)***

Fig. 8. 2 (a) Phase portrait of SRAM when I_N is 500 μA; (b) the timing diagram of this cell.



(a) ***(b)***

Fig. 8. 3 (a) Phase portrait and (b) time diagram for a square pulse noise of 500μA amplitude and 0.43ns duration.

If double-sided current injection (I_{N1}, I_{N2}) is considered, once the noise current (I_{N1}, I_{N2}) is at right hand side of combination of critical currents, the SRAM state will reach the separatrix. The time for the state to reach the separatrix is the critical time. As long as the injected noise magnitude keeps at right hand side of combination of critical currents, state-flip will occur. Next section will discuss the analytical formula of critical time (T_C) derivation.

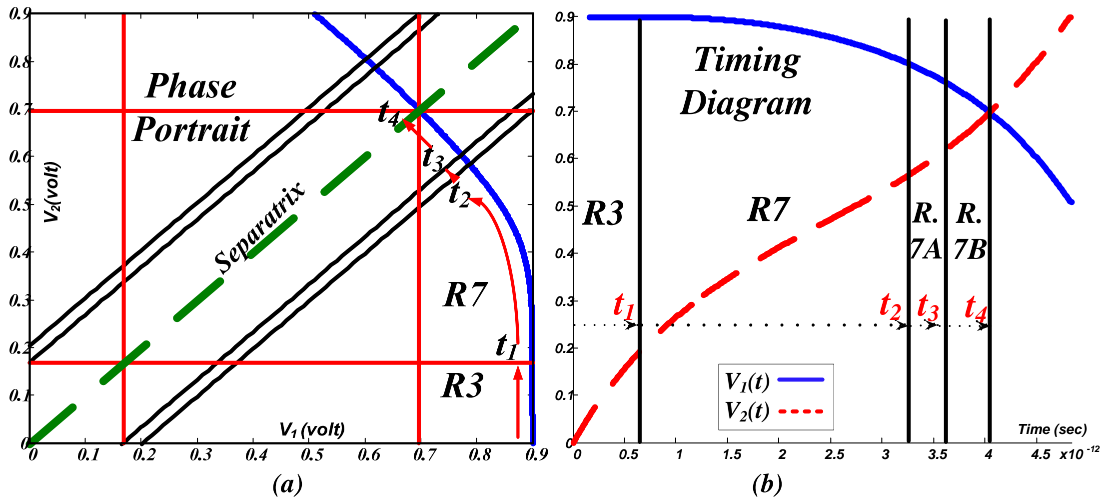


Fig. 8. 4 (a) The simulated phase portrait of a 65nm SRAM based on the S-H model. It shows a cell state crosses separatrix (45° line through origin) and flips to the other side; (b) the timing diagram of the cell state.

8.2.2. The Analytical Solution For Critical Time

The SRAM cell will flip if the cell state crosses the *stability boundary*. During the operation of the SRAM cell, if a stable state is perturbed across that boundary, a state flipping will be resulted. For a perfectly symmetric SRAM cell, the stability boundary can be simply defined by passing a 45 degree line through the origin on the phase portrait of the SRAM cell. The stability boundary of the SRAM is also called *separatrix* because the stability boundary separates two stability regions [59] [71] [87-89]. If the injected noise current is higher than the critical current, the state of the cell will drive from the initial stable and go across the separatrix eventually. The time it takes from the initial state to the separatrix is called *critical time* (T_C). After the trajectory across the separatrix, the cell state will fall into the stability region of the other stable equilibrium and result in a state flip.

An example is demonstrated in Fig. 8.4. Since it is symmetrical designed; the separatrix is the 45 degree line passing through the origin. In Fig. 8.4 (a), the cell state initially starts at (0.9, 0) in Region 3 (R3) at time 0. It enters Region 7 (R7) at time t_1 and enters Region 7A (R7A) at time t_2.The state will eventually reach the separatrix in Region 7B (R7B) at time t_4. Once the state passes the separatrix, the state can never be recovered even if the noise injections disappear. The total time taken for a state to reach the separatrix is the critical time, which is t_4 in this case.

Figure 8.4 (b) shows the timing diagram for that cell state. The state transits through many regions to flip the state. The rigorous way to find the critical time is to separately find the time spent in each region then sum each together. However, this results into symbolic expressions which is very cumbersome. The way we simplify the analytical formula is based on the observation that vector field strength around bifurcation point is weak so that the trajectory takes up more time in the region of bifurcation. In this regard, it is efficient to focus on the time spent in the region of bifurcation to arrive at a simple but physically meaningful expression for the critical time. In other words, we find the expression of the time spend in the region of bifurcation to be the critical time analytical formula. As demonstrated in Fig. 8.4(b), the trajectory spend most of the time in region of bifurcation, region 7 (R7), than any other regions. The analytical formula for T_C is to solve the nonlinear ODE corresponding to the transistor combination in Region 7 (R7), which mentioned in (5.14).

However, solving the cross-coupled nonlinear ODE in (5.14) is cumbersome. Mathematically, there is no good technique to directly solve this type of ODE. The way

we by-pass the nonlinearity is to linearize the ODE at the bifurcation point. In this regard, we preserve the characteristics of the cell state trajectory around bifurcation point and simplify the complexity of the equation at the same time. By doing that, the system can be modeled using two cross-coupled linear ODE as shown below:

$$\begin{cases} C_1 \cdot \dot{V}_1(t) = g_{11}(V_1 - V_{1B}) + g_{12}(V_2 - V_{2B}) - (I_{N1}(t) - f_1(V_{1B}, V_{2B})) \\ C_2 \cdot \dot{V}_2(t) = g_{21}(V_1 - V_{1B}) + g_{22}(V_2 - V_{2B}) + (I_{N2}(t) + f_2(V_{1B}, V_{2B})) \end{cases} \tag{8. 3}$$

or

$$\begin{cases} \dot{V}_1(t) = a_1 \cdot V_1(t) + b_1 \cdot V_2(t) + I_1(t) \\ \dot{V}_2(t) = a_2 \cdot V_1(t) + b_2 \cdot V_2(t) + I_2(t) \end{cases} \tag{8. 4}$$

where

$$\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} = \begin{bmatrix} \partial f_1 / \partial V_1 & \partial f_1 / \partial V_2 \\ \partial f_2 / \partial V_1 & \partial f_2 / \partial V_2 \end{bmatrix} \Bigg|_{\substack{V1=V1B \\ V2=V2B}}, \tag{8. 5}$$

$$\begin{bmatrix} a_1 & b_1 \\ a_2 & b_2 \end{bmatrix} = \begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix}^{-1} \cdot \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix}, \tag{8. 6}$$

$$\begin{bmatrix} I_1(t) \\ I_2(t) \end{bmatrix} = \begin{bmatrix} -(a_1 \cdot V_{1B} + b_1 \cdot V_{2B}) - (I_{n1}(t) - I_{C1})/C_1 \\ -(a_2 \cdot V_{1B} + b_2 \cdot V_{2B}) + (I_{n2}(t) - I_{C2})/C_2 \end{bmatrix} \tag{8. 7}$$

and

$$\begin{aligned} I_{C1} &= f_1(V_{1B}, V_{2B}) \\ I_{C2} &= -f_2(V_{1B}, V_{2B}) \end{aligned}. \tag{8. 8}$$

The coefficients (g_{11}, g_{12} …etc) are functions of system parameters. Since the Jacobian matrix (8.5) is singular at bifurcation point, the eigenvalues will be 0 and λ, and λ is a negative value. The singular Jacobian matrix means zero determine, namely:

$$a_1 b_2 - a_2 b_1 = 0\,. \tag{8. 9}$$

Solving (8.4) yields the following general solution using Laplace Transform:

$$\begin{cases} V_1(t) = \left(\frac{b_2}{\lambda} + \frac{a_1}{\lambda} e^{\lambda \cdot t}\right) \cdot V_1(0) + \left(-\frac{b_1}{\lambda} + \frac{b_1}{\lambda} e^{\lambda \cdot t}\right) \cdot V_2(0) \\ \quad + \left(\frac{b_2}{\lambda} + \frac{a_1}{\lambda} e^{\lambda \cdot t}\right) * I_1(t) + \left(-\frac{b_1}{\lambda} + \frac{b_1}{\lambda} e^{\lambda \cdot t}\right) * I_2(t) \\ V_2(t) = \left(-\frac{a_2}{\lambda} + \frac{a_2}{\lambda} e^{\lambda \cdot t}\right) \cdot V_1(0) + \left(\frac{a_1}{\lambda} + \frac{b_2}{\lambda} e^{\lambda \cdot t}\right) \cdot V_2(0) \\ \quad + \left(-\frac{a_2}{\lambda} + \frac{a_2}{\lambda} e^{\lambda \cdot t}\right) * I_1(t) + \left(\frac{a_1}{\lambda} + \frac{b_2}{\lambda} e^{\lambda \cdot t}\right) * I_2(t) \end{cases}, \tag{8. 10}$$

where

$$\lambda = a_1 + b_2 . \tag{8. 11}$$

The *$(V_1(0), V_2(0))$* is the initial condition and *(*)* is the convolution integral. In our case, we treat the injected current constant. Thus, the expression becomes:

$$\begin{cases} V_1(t) = A_{P1} + B_{P1} \cdot e^{\lambda t} + C_{P1} \cdot t \\ V_2(t) = A_{P2} + B_{P2} \cdot e^{\lambda t} + C_{P2} \cdot t \end{cases} \tag{8. 12}$$

where

$$C_{P1} = -\frac{1}{\lambda}\left(\frac{b_1(I_{N2} - I_{C2})}{C_2} + \frac{b_2(I_{N1} - I_{C1})}{C_1}\right),\ B_{P1} = \frac{\dot{V}_1(0) - C_{p1}}{\lambda},\ A_{P1} = V_1(0) - B_{P1}, \tag{8. 13}$$

$$C_{P2} = \frac{1}{\lambda}\left(\frac{a_1(I_{N2} - I_{C2})}{C_2} + \frac{a_2(I_{N1} - I_{C1})}{C_1}\right),\ B_{P2} = \frac{\dot{V}_2(0) - C_{p2}}{\lambda},\ A_{P2} = V_2(0) - B_{P2}, \tag{8. 14}$$

$(\dot{V}_1(0), \dot{V}_2(0))$ is acquired by evaluating (25) at *$t=0$*. The trajectory in (33) will cross the separatrix at

$$V_1(T_C) = V_2(T_C) \tag{8. 15}$$

since the separatrix is a 45º line through the origin.

We assume the exponential terms in (8.12) become negligible by the time the state trajectory reaches the separatrix due to the exponential decay, the formula for the critical time T_C is:

$$T_C = \frac{A_{P1} - A_{P2}}{C_{P2} - C_{P1}}. \tag{8. 16}$$

And, it leads to:

$$T_C = \frac{\left(-\lambda \cdot (V_1(0) - V_2(0)) + \left(\dot{V}_1(0) - \dot{V}_2(0)\right) - \left(C_{p1} - C_{p2}\right)\right)}{\lambda\left(C_{p1} - C_{p2}\right)}. \tag{8. 17}$$

We eliminate $(\dot{V}_1(0) - \dot{V}_2(0))$ and $(C_{P1}\text{-}C_{P2})$ on the numerator because together they are close to cancel each other and become insignificant. That simplifies the equation to:

$$T_C = \frac{\left(C_2 \cdot g_{11} + C_1 \cdot g_{22}\right) \cdot \left(V_1(0) - V_2(0)\right)}{\left(g_{11} + g_{12}\right) \cdot \left(I_{N2} - I_{C2}\right) + \left(g_{21} + g_{22}\right) \cdot \left(I_{N1} - I_{C1}\right)}. \tag{8. 18}$$

Equation (8.18) is the master equation for critical time for a given (I_{N1}, I_{N2}). The set of (V_{1B},V_{2B},I_{C1},I_{C2}) should be selected at (V_{1B}^{SNM}, V_{2B}^{SNM}, I_{C1}^{SNM}, I_{C2}^{SNM}), where (I_{C1}^{SNM}, I_{C2}^{SNM}) is the closest IC combination to (I_{N1}, I_{N2}) as discussed in (7.29).

Let us demonstrate a special case. Consider an injected noise combination (0, I_{N2}), which is a point on the right hand side of IC combination line as shown in Fig. 7.8. The critical currents ($I_{C1}^{SNM}, I_{C2}^{SNM}$) marked in Fig. 7.8, which is the closest critical currents to the noise combination (0, I_{N2}) and its formula is given in (7.29), will be the (I_{C1}, I_{C2}) used in (8.18). For that, the critical time formula is derived as follows after evaluated (8.18) at the initial condition ($V_1(0)=V_{dd}, V_2(0)=0$):

$$T_C = \frac{\left(C_2 \cdot g_{11} + C_1 \cdot g_{22}\right) \cdot V_{dd}}{\left(g_{11} + g_{12}\right) \cdot \left(I_{N2} - I_{C2}^{SNM}\right) + \left(g_{21} + g_{22}\right) \cdot \left(0 - I_{C1}^{SNM}\right)} \tag{8. 19}$$

where

$$\begin{cases} g_{11} = -2K_1 \cdot (V_{1B}^{SNM} - V_{2B}^{SNM} - V_{th1}) \\ g_{12} = -2K_1 \cdot (V_{dd} - V_{1B}^{SNM}) - 2K_2 (V_{2B}^{SNM} - V_{th2}) \\ g_{21} = -2K_4 \cdot V_{2B}^{SNM} \\ g_{22} = -2K_4 \cdot (V_{1B}^{SNM} - V_{2B}^{SNM} - V_{th4}) \end{cases} \tag{8. 20}$$

The coefficients (g_{11}, g_{12} …etc) are acquired from evaluating (8.5) in the region of bifurcation.

Furthermore, if take the exponential terms in (8.12) into account, the critical time equation can be simpler if substitute the exponential term ($e^{\lambda t}$) by its Taylor expansion $1+\lambda t$. The formula becomes nicely as follows:

$$T_C = \frac{(A_{P1} - A_{P2}) + (B_{P1} - B_{P2})}{(C_{P2} - C_{P1}) + \lambda \cdot (B_{P2} - B_{P1})} = \frac{V_1(0) - V_2(0)}{\dot{V}_1(0) - \dot{V}_2(0)} = \frac{V_1(0) - V_2(0)}{\frac{I_{N2} - I_{C2}}{C_2} + \frac{I_{N1} - I_{C1}}{C_1}}, \tag{8. 21}$$

and equivalently

$$T_C = C \cdot \frac{V_{dd}}{\left(I_{N2} - \left(I_{C2}^{SNM} + I_{C1}^{SNM}\right)\right)}. \tag{8. 22}$$

Equation (8.22) is a good approximation if the injected current magnitude (I_{N2}) is more than five times of its critical current (I_{C2}). If I_{N2} goes beyond eight times of I_{C2}, the formula can be shown as $T_C=C \cdot V_{dd}/I_{N2}$, which is the same formula shown in (Zhang, 2006) on p.320 [51].

Below are the summarized steps to solve critical time (***T_C***) for a given (I_{N1}, I_{N2})**:**

1. Have the line of IC combination known. The given (I_{N1}, I_{N2}) has to be on the right hand side of the line to have critical time. Otherwise, no critical time can be observed.
2. Find the closest IC combination (I_{C1}^{SNM}, I_{C2}^{SNM}) point on the line that is closest to (I_{N1},I_{N2}), and acquire the corresponding bifurcation point (V_{1B}^{SNM}, V_{2B}^{SNM}).
3. Formulate the linearized ODE at the bifurcation point.
4. Solve the general solution and particular solution for the linearized ODE.
5. Find the critical time, T_C, by solving $V_1(T_C)=V_2(T_C)$ for symmetrical designs.

In summary, the simplification was made to the dynamic system formulation at the bifurcation point (linearization) to obtain two linear ODEs, from which an analytic solution was found for the critical time (the time from initial state to the stability boundary).

CHAPTER IX

SUMMARY

9.1. Summary and Contributions

Overall, dynamics of memristor and SRAM are strongly emphasized. The derived memristor properties reveals that the memristor state change requires some time; it indicates that the memristor-based memory needs some "***critical time***" to flip the logic. Similarly to the SRAM, the SRAM write operation not only needs the injected current over a "***critical current***" but also need to maintain for some "***critical time***". In short, simulation shows that both memristor-based memory and SRAM show the timely manner for read/write operation. Furthermore, the developed analytical formulae are able to reveal the dynamic aspect on memory read/write operations which address the key concern for modern memory technology.

9.1.1. Memristor-based Memory

In this work, we systematically derive a comprehensive set of properties and analytical solutions for characterizing the fundamental electrical properties of memristor devices. Our compact closed-form expressions provide valuable design insights and allow an in-depth understanding of key design implications of memristor-based memories. Using our derived properties, we investigate the design of read/write circuits and analyze data integrity and noise-tolerance issues. In addition, we apply our valuable design insights from the fundamental electrical properties derived from the ideal linear

drift memristor model to design memristor-based memories that consist of more realistic nonlinear characteristics. Based on the provided memristor model from HP, the "critical current" for memristor state switching is not clear by the given simple linear drift formula. As we can see from the more completed memristor model, if the injected current i is less than the on or off magnitude (i_{on} or i_{off}), the value out of hyperbolic sine would be very small, thus the positive or negative drifting velocity would also be small. Therefore, the on and off currents work as a critical current for the memristor state to move, where the linear drift model is too simple that does not indicate such on or off current phenomenon. However, we demonstrate that linear drift model properties can be effectively used to resolve the boundary trapping issues faced by realistic nonlinear memristor models.

9.1.2. Static Random Access Memory

This dissertation has two main contributions on SRAM:

1. Newly established the concept of Static Noise Margin in current representation and further provided analytical formula for it.
2. Explored an analytical approach to the evaluation of dynamic stability analysis for SRAMs.

The concepts of critical current and critical time, based on theoretically rigorous stability analysis of the dynamic behaviors of SRAM cells, provide physical characterizations of SRAM stability. In summary, the dependencies of critical time and critical current on several key design and technology parameters are evaluated. We also

examine the effect of temperature and process variation effect to I_C and T_C. Furthermore, we studied the I_C and T_C dependencies on the system parameters shown in the equations in Appendix. The simplification is done by keeping the targeted parameter as a variable while plugging nominal values of the other parameters into the equation. This provides us an immediate understanding of the parametric dependency of the targeted parameter. A short summary and key observation on sensitivity of system parameters with_respect to global variation are as follows:

1. Both I_C and T_C have very high dependency on V_{dd}. They grow approximately quadratically with V_{dd}.
2. Both I_C and T_C also have high dependency on K_n. I_C tends to increase linearly with K_n, but T_C increases more rapidly with K_n.
3. Both I_C and T_C have low dependency on the rest of parameters.
4. Both I_C and T_C increase as K_n and K_p increase but decrease as V_{thn} and V_{thp} increase.
5. I_C does not depend on C, but T_C is highly depended on the capacitance at stored nodes.

The critical time is approximately proportional to $1/(I_n\text{-}I_C)$. Clearly, a current injection must be greater than I_C in order to flip the state. Intuitively, a larger injection would make the cell to flip its state faster and the time to flip the state is inversely proportional to the difference between the amplitude of the current noise and I_C.

Furthermore, we rank the sensitivity of the system parameters (V_{dd}, V_{thn}/V_{thp} and K_n/K_p) and summarized in Table 9.1 for the single-sided current injection case. T_C and I_C

both depend on the same sets of device parameters such as transistor threshold voltages, which create correlation between the two. We combine the collected data from previous sections.

Table 9.1. Summary on the Sensitivity of the System Parameters

	V_{dd}	V_{thn}	V_{thp}	K_N	K_P
I_C	*Very Strong*	*Weak*	*Very Weak*	*Strong*	*Weak*
T_C	*Very Strong*	*Weak*	*Very Weak*	*Strong*	*Weak*

Moreover, the analytic requires less computational power. Compare with the transistor-level simulation, the derived analytic provides a speedup of *6* order of magnitude. We use a transistor-level circuit simulator, in this case, Cadence Spectre to find both I_C and T_C as follows: I_C is found by incrementing the injected current until an SRAM state flip is resulted; T_C is acquired by doing a transient simulation. On average, it takes Cadence Spectre simulator 0.777 seconds to compute the critical current with a nano-amp precision. In addition, the average runtime for the critical time is 48 milliseconds. In comparison, for our C-based analytical models, the average runtime for I_C is 0.25 microseconds and 0.02 microseconds for T_C. As a result, the overall runtime speedup of our models over transistor-level circuit simulation is about 6 orders of magnitude. Lastly, the derived analytical models are also able to provide useful design insights and aid the designers to perform SRAM design optimization while considering the key dynamic stability property.

9.2. Future Works

9.2.1. Future Works on Memristor

Neuromorphic circuits get many attentions after the memristor device came out. Recently, there are two types of neuromorphic circuits: the learning circuits and neural networks [90]. More specifically, learning circuits are broadly the circuits that can demonstrate self-adaptation or smart operation, and neural network circuits are built based on biological structure and meant to mimic the learning functionalities in biological aspect. Neuromophic circuit is a very large area of research, in part because a large part of the analog science detail has to do with advances in cognitive psychology, artificial intelligence modeling, machine learning and recent neurology advances. In fact, scientists and engineers already started the work on neural field in the past decade. The earliest work traces back to 1960, which is the ADALINE neural network [91]. The research halted due to difficulties on implement the large size of complexity circuitry on chip. Due the advance of nanotechnology in the 20th century, such task becomes feasible to do. Moreover, scientist has shown that the memristor device follows the behavior of synapse [92]. Thus, the memristor have made the possibility to implement neural network on chip. In short, many scientists and researchers are exploring innovative approaches that enable revolutionary advances in devices for memristor-based learning circuitry and neural-synaptic mimicking.

9.2.2. Future Works on SRAM

Since the nonvolatile device has disadvantage on the switching speed, the nonvolatile device can combine with SRAM and benefit by the fast switching speed that SRAM has. And, SRAM can go off power in standby mode to save power consumption by storing the logic to nonvolatile memories. In fact, there already have some research works regards to such a hybrid device very recently. They called the nonvolatile SRAM or nvSRAM as shown in Fig. 9.1 [93-94]. In Fig. 9.1(a), the SRAM is not isolated from the nonvolatile device, so the nvSRAM 6T2R has some cell leakage during SRAM operations. The nvSRAM 8T2R in Fig.9.1 (b) is the newly proposed topology which it has extra transistors isolating the nonvolatile device and the SRAM to avoid cell leakage. Regardless Fig. 9.1(a) or (b), the nvSRAM has thses basic modes: (1) NORMAL; (2) STORE; (3) RESTORE. During NORMAL mode, SRAM is doing the read/write operation or what it supposed to do. The STORE operation is writing the stored logic into nonvolatile memory, and RESTORE is the other way around.

As it can be seen, as the SRAM communicates with the nonvolatile device such as memristor, there can be a lot of dynamics going on. The read/write stability issues have not been fully discovered yet at this stage. This material in this work is then able to provide much dynamic detail, and the developed SRAM stability metric would be a helpful tool to provide needed insights for a hybrid device like nvSRAM.

9.3. Acknowledgement

This material is based on work supported by the *National Science Foundation* under grant no. 0917204.

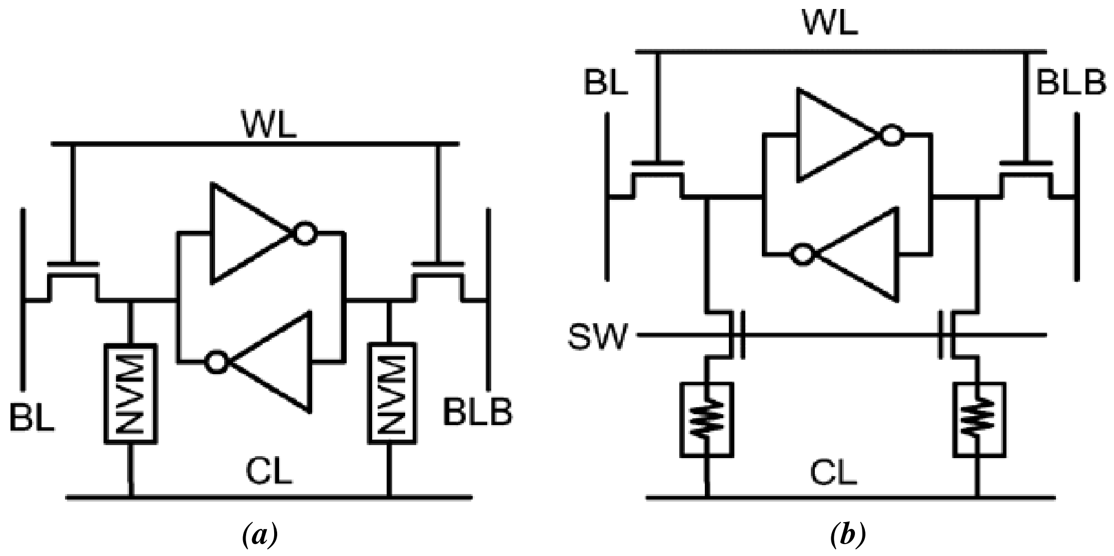


Fig. 9. 1. An nvSRAM cell schemes of (a) 6T2R and (b) 8T2R.

REFERENCES

[1] F. Wang, "Commentary: Memristor and memristive switch mechanism," Journal of Nanophotonics, vol. 2, p. 020304, 2008.

[2] J. M. Kumar, "Editorial: Memristor- Why do we have to know about it," IETE Technical Review, vol. 26, issue1, Jan 2009.

[3] G. Chen, "Leo Chua's memristor [Recognitions]", IEEE Circuits and Systems Magazine, vol. 8, p.p. 55, 2008.

[4] D.B. Strukov, J. L. Borghetti and R. S. Williams, "Coupled ionic and electronic transport model of thin-film semiconductor memristive behavior," Wiley Inter-Science, No 1-6, 2009.

[5] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: memristors, memcapacitors and meminductors," Proc. IEEE, vol. 97, pp. 1717–1724, 2009.

[6] Z. Biolek, D. Biolek, and V. Biolkova, "Spice model of memristor with nonlinear dopant drift," Radioengineering, vol. 18, no. 2, Part 2, pp. 210–214, June 2009.

[7] X. Wang, Y. Chen, H. Xi, H. Li, and D. Dimitrov, "Spintronic memristor through spin-torque-induced magnetization motion," IEEE Electron Device Lett., vol. 30, no. 3, pp. 294–297, 2009.

[8] Y. Chen, X. Wang, "Compact modeling and corner analysis of spintronic memristor", IEEE/ACM Nano-architecture, pp. 7-12, March 2009.

[9] Yu. V. Pershin and M. Di Ventra, “Spin memristive systems: Spin memory effects in semiconductor spintronics,” Phys. Rev. B, Condens. Matter, vol. 78, p. 113309/1-4, 2008.

[10] T. Driscoll, H. T. Kim, B. G. Chae, M. Di Ventra, and D. N. Basov, “Phase-transition driven memristive system,” Appl. Phys. Lett., vol. 95, no. 4, pp. 043 503/1–3, 2009.

[11] R. Riaza, “Nondegeneracy Conditions for Active Memristive Circuits”, IEEE Trans. Circuits and Systems II: Express Briefs, vol. 57, no. 3, pp. 223-227, March 2010.

[12] L. O. Chua, “Memristor—The missing circuit element,” IEEE Trans. Circuit Theory, vol. CT-18, pp. 507–519, Sept. 1971.

[13] L. O. Chua and S. M. Kang, “Memristive devices and systems,” Proc. IEEE, vol. 64, pp. 209-223, Feb 1976.

[14] L. O. Chua, “Device modeling via basic nonlinear circuit elements,” IEEE Trans. Circuits Syst., vol. CAS-27, pp. 1014–1044, Nov. 1980.

[15] L. Chua, ”Nonlinear Circuits”, IEEE Trans. Circuits and Systems, vol. CAS-31, No. 1, pp. 69-87, Jan. 1984.

[16] L. Chua, “Nonlinear circuit foundations for nanodevices, part I: The four-element torus,” Proc. IEEE, vol. 91, no. 11, pp. 1830–1859, Nov 2003.

[17] M. Itoh, L. Chua, ”Memristor oscillators”, Journal of Bifurcation and Chaos, Vol. 18, No. 11, 2008.

[18] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, “The missing memristor found,” Nature, vol. 453, pp. 80-83 (2008).

[19] G. Snider, “Computing with hysteretic resistor crossbars,” Applied Physics, vol. 80, pp. 1165-1172 (2005).

[20] A. C. Cabe, S. Das, “Performance simulation and analysis of a CMOS/Nano Hybrid Nanoprocessor System”, Nanotechnology, vol. 20, issue 16, pp. 1-8, April 2009.

[21] G. S. Snider, “Cortical computing with memristive nanodevices,” Sci- DAC Review, vol. 10, pp. 58–65, 2008.

[22] P. Vontobel, W. Robinett, P. J. Kuekes, D. R. Stewart, J. Straznicky, R. S. Williams, “Wrting to and reading from a nano-scale crossbar memory based on memristors”, Nanotechnology, issue. 42, October 2009.

[23] L. O. Chua, “Resistance switching memories are memristors,” Appl. Phys. A, Mater. Sci. Process., vol. 102, no. 4, pp. 765–783, March 2011.

[24] C. R. Johnson, “Missing Link memristor created: Rewrite the textbook?,” EETimes Magazine: Designlines Automotive, April 30 2008.

[25] J. Borghetti, Z. Li, J. Straznicky, X. Li, D. A. A. Ohlberg, W. Wu, D. R. Stewart, and R. S. Williams, “A hybrid nanomemristor/transistor logic circuit capable of self-programming,” Proc. Natl. Acad. Sci. U. S. A., vol. 106, no. 6, pp. 1699–1703, 2009.

[26] P. J. Kuekes, D. R. Stewart, and R. S. Williams, “The crossbar latch: Logic value storage, restoration, and inversion in crossbar circuits,” J. Appl. Phys., vol. 97, no. 3, pp. 034 301-1–034 301-5, Feb. 2005.

[27] T. Raja, S. Mourad, “Digital Logic Implementation in Memristor-based Crossbar”, IEEE ICCCAS 2009, pp. 939-943, 2009.

[28] G. Snider, P. Kuekes, R. S. Williams, “CMOS-like logic in defective, nanoscale crossbars,” Nature Nanotechnology, 2004.

[29] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, R. S. Williams,”Memristor-CMOS Hybrid integrated circuits for reconfigurable logic”., Nano letters, vol. 9, no. 10, pp. 3640-3645, 2009.

[30] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, R. S. Williams, “’Memristive’ switches enable ‘stateful’ logic operations via material implication”, Nature, vol. 464, April 2010.

[31] E. Lehtonen, M. Laiho, “Stateful implication logic with memristors”, International Symposium on Nanoscale Architectures, pp. 33-36, July 2009.

[32] Y. Pershin, M. Di Ventra, “Practical approach to programmable analog circuit with memristors”,IEEE Transactions on Circuits and Systems I: Regular Papers, pp. 99, 2009.

[33] S. Shin, K. Kim, S. Kang, “Memristor Applications For Programmable Analog ICs”, IEEE Trans. Nanotechnology, no. 99, 2010.

[34] S. Shin, K. Kim, and S. M. Kang, “Memristor-Based Fine Resolution Resistance and Its Applications,” ICCCAS, pp. 948-951, July 2009.

[35] H. Kim, M. Pd. Sah, C. Yang, L. O. Chua, “Memristor-based Multilevel Memory”, International Workshop on CNNA, pp. 89-94, 2010.

[36] M. Laiho, E. Lehtonen, “Arithmetic Operations within Memristor-Based Analog Memory”, International Workshop on Cellular Nanoscal Neworks and Theirs Applications (CNNA), pp. 1-4, 2010.

[37] Q. Yu, Z. Qin, J. Yu, Y. Mao, “Transmission Characteristics Study of Memristors Based Op-Amp Circuits”, IEEE ICCCAS 2009, pp. 974-977, 2009.

[38] D. Varghese, G. Gandhi, “Memristor based High Linear Range Differential Pair”, IEEE ICCCAS 2009, pp. 935-938, 2009.

[39] Y. V. Pershin and M. Di Ventra, “Experimental demonstration of associative memory with memristive neural networks,” arXiv:0905.2935, 2009.

[40] M. Itoh, L. O. Chua, “Memristor cellular automata and memristor discrete-time cellular neural networks”, International Journal of Bifurcation and Chaos, vol. 19, no. 11, pp. 3605-3656, 2009.

[41] Y. V. Pershin, S. La Fontaine, and M. Di Ventra, “Memristive model of amoeba’s learning,” Phys. Rev. E, vol. 80, p. 021926/1-6, 2009.

[42] G. S. Snider, “Spike-Timing-Dependent Learning in Memristive Nanodevices,” IEEE Int. Symp. Nano Architectures, pp. 85-92, June 2008.

[43] B. Linares-Barranco, T. Serrano-Gotarredona, “Memristance can explain spike-time dependent-plasticity in neural synapses”, Proc. Natural, Mar 2009.

[44] E. Lehtonen, M. Laiho, “CNN Using Memristors for Neighborhood Connections”, International Workshop on CNNA, pp. 1-6, 2010.

[45] J. Rajendran, H. Manem, G. S. Rose, “NDR Based Threshold Logic Fabric with Memristive Synapses”, IEEE-NANO 2009, pp. 727-728, 2009.

[46] M. J. Sharifi, Y. M. Banadaki, “General spice models for memristor and application to circuit simulation of memristor-based synapses and memory cells”, World Scientific Journal of Circuits Systems and Computers, vol. 19, no. 2, pp. 407-424, 2010.

[47] G. Angelov, M. Hristov, “SPICE modeling of MOSFETs in deep submicron.” In IEEE 27th International Spring Seminar on Electronics Technology: Meeting the Challenges of Electronics Technology Progress, vol. 2, pp. 257-262, May, 2004.

[48] D. Edenfeld, A. B. Kahng, M. Rodgers, Y. Zorian, “2003 technology roadmap for semiconductors.” Computer, vol. 37, no. 1, pp. 47-56, 2004.

[49] E. Seevinck, F. J. List, J. Lohstroh, “Static-noise margin analysis of MOS SRAM cells.” IEEE Journal of Solid-State Circuits, vol. 22, no. 5, pp.748-754, 1987.

[50] F. J. List, “The static noise margin of SRAM cells.” In IEEE 12th Solid-State Circuits Conference ESSCIRC, pp. 16-18, September 1986.

[51] B. Zhang, A. Arapostathis, S. Nassif, M. Orshansky, “Analytical modeling of SRAM dynamic stability.” In Proceedings of the 2006 IEEE/ACM international conference on Computer-aided design (ICCAD), pp. 315-322, 2006.

[52] Y. Ho, G. Huang, and P. Li, “Nonvolatile Memristor Memory: Device Characteristics and Design Implications,” IEEE/ACM International Conference on Computer Aid Design (ICCAD), Nov. 2009.

[53] W. Dong, P. Li, G. M. Huang, “SRAM Dynamic Stability: Theory, Variation and Analysis,” IEEE International Conference on Computer-Aided Design (ICCAD), pp. 378-335, Nov. 2008.

[54] Y. N. Joglekar, S. J Wolf, “The elusive memristor: properties of basic electrical circuits”, European Journal of Physics, vol. 30, pp. 661-675, 2008.

[55] Frank Y. Wang, “Memrister for introductory physics”, Proc. IEEE, Aug 2008.

[56] O. Kavehei, Y. Kim, A. Iqbal, K. Eshraghiam, S. F. Al-Sarawi, D. Abbott, "The Fourth Element: Characteristics, Modelling, and Electromagnetic Theory of the Memristor", Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences, vol. 466, no. 2120, pp. 2175-2202, 2010.

[57] J. J. Yang, M. D. Picket, X. M. Li, D. A. A. Ohlberg, D. R. Stewart and R. S. Williams, “Memristive switching mechanism for metal/oxide/metal nanodevices,” Nature Nanotechnology, vol. 3, pp.429-33, July 2008.

[58] G. M. Huang, Y. Ho, P. Li, “Memristor system properties and its design applications to circuits such as nonvolatile memristor memories,” IEEE Intl. Conf. on Communications, Circuits and Systems, pp. 805-810, July 2010.

[59] H. Khalil, *Nonlinear Systems*. 3rd ed. Upper Saddle River, NJ: Prentice-Hall., 2002.

[60] A. S. Sedra, K. C. Smith, *Microelectronic Circuits*, 5th ed., New York: Oxford University Press, 2004.

[61] H. Pilo, C. Barwin, G. Braceras C. Browning, S. Lamphier and F. Towler, “An SRAM design in 65-nm technology node featuring read and write-assist circuits to expand operating voltage”, IEEE Journal of Solid-State Circuits, vol. 42, no. 4, pp. 813-819, Apr. 2007.

[62] R. Garg, P. Li, S. P. Khatri, “Modeling dynamic stability of SRAMs in the presence of single event upsets (SEUs),” in Proc. of IEEE Int. Symp. on Circuits and Systems, pp. 1788-1791, May 2008.

[63] T. May and M. Woods, “Alpha-particle-induced soft errors in dynamic memories,” IEEE Trans. on Electron Devices, vol. ED-26, pp. 2–9, January 1979.

[64] J. Pickle and J. Blandford, “CMOS RAM cosmic-ray-induced error rate analysis,” IEEE Trans. on Nuclear Science, vol. NS-29, pp. 3962–3967, 1981.

[65] W. Massengill, M. Alles, and S. Kerns, “SEU error rates in advanced digital CMOS,” in Proc. Second European Conference on Radiation and its Effects on Components and Systems, pp. 546 – 553, Sept. 1993.

[66] R. Garg, N. Jayakumar, S. P. Khatri, and G. Choi, “A design approach for radiationhard digital electronics,” in Proceedings, IEEE/ACM Design Automation Conference (DAC), pp. 773–778, July 2006.

[67] E. Seevinck, F. List, and J. Lohstroh, “Static-noise margin analysis of MOS SRAM cells,” IEEE J. Solid-State Circuits, vol. SC-22, pp. 748–754, Oct. 1987.

[68] F. J. List, “The Static Noise Margin of SRAM cells,” IEEE Solid-State Circuits Conference (ESSCIRC), pp. 16-18, Sept. 1986.

[69] S. R. Nassif, “C-∞ Shichman Hodges Model,” A Report From IBM Research-Austin, 2006

[70] H. Shichman, D. A. Hodges, “Modeling and Simulation of Insulated-Gate Field-Effect Transistor Circuits,” IEEE J. of Solid-State Circuits, vol. SC-3, no.3, pp. 285-289, Sept. 1968.

[71] Y. Ho, “Dynamic stability margin analysis on SRAM,” M.S. thesis, Dept. of Electrical and Computer Engineering, Texas A&M Univ., College Station, TX, 2008.

[72] Sheu, Scharfetter, Ko, and Jeng, "BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors". IEEE Journal of Solid State Circuits, vol. SC-22, pp. 558–566, August 1987.

[73] N. Weste, D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 3rd Edition, Addison Wesley, 2005.

[74] F. Lai, Y. L. Chuang, “A New Design Methodology for Multiport SRAM Cell”, IEEE Trans. Circuits and System I: Fundamental Theory and Applications, vol. 41, no. 11, Nov 1994.

[75] A. Dayal, P. Li, and G. Huang, "Robust SRAM design via joint sizing and voltage optimization under dynamic stability constraints", Journal of Low Power Electronics, vol. 6, no.1, p. 66-79, 2010.

[76] G. Huang, W. Dong, Y. Ho, and P. Li, “Tracing SRAM separatrix for dynamic noise margin analysis under device mismatch,” Behavioral Modeling and Simulation Conf., pp. 6-10, Sept. 2007.

[77] J. Carr, Applications of Center Manifold Theory. New York: Springer Verlag, vol. 35, 1981.

[78] A. Kelley, "The stable, center stable, center, center unstable and unstable manifolds" J. Diff. Eq., vol. 3, pp. 546–570, 1967.

[79] J. Zaborszky, G. Huang, B. Zheng and T.C. Leung, “On the phase portrait of a

class of large nonlinear dynamic systems such as the power system," IEEE Transactions on Automatic Control, vol. 33, no. 1, pp. 4-15, January 1988.

[80] C. Hu, "Modern Semiconductor Devices for Integrated Circuits," Pearson/Prentice Hall, New Jersey, 2010.

[81] Y. Cheng et al., "BSIM3v3 Manual," Dept. of Electrical Engineering and Computer Sciences, Univ. California, Berkeley, 1995–1997.

[82] W. Liu and C. Hu,"BSIM4 and MOSFET Modeling for IC Simulation," World Scientific Publishing, Singapore, 2011.

[83] T. H. Morshed et al., "BSIM4v4.7 MOSFET Model User Manual," Dept. Elec. and Comp. Sciences, University of California, Berkeley, CA, 2011.

[84] Y. Cheng et al., "Modeling temperature effects of quarter micrometer MOSFETs in BSIM3v3 for circuit simulation," Semicond. Sci. Technology, vol. 12, no. 11, pp. 1349–1354, Nov. 1997.

[85] J. Lohstroh, E. Seevinck, and J. Groot, "Worst-case noise margin criteria for logic circuits and their mathematical equivalence," IEEE J. Solid State Circuits, vol. SC-18, pp. 803–806, Dec. 1983.

[86] E. Seevinck, "Deriving Stability Criteria for Nonlinear Circuits with Application to Worst-Case Noise Margin of I^2L," IEEE Electronic Letters, vol. 16, no. 23, Sept. 1980.

[87] Y. Song, H. Yu, S. M. Pudukotai-Dinakarrao, G. Shi, "SRAM dynamic stability verification by reachability analysis with consideration of threshold voltage variation." In Proceedings of the 2013 ACM international symposium on

International symposium on physical design, pp. 43-49, 2013.

[88] J. Wang, S. Nalam, and B. H. Calhoun, "Analyzing static and dynamic write margin for nanometer SRAMs," ISLPED, Jan. 2008.

[89] S. M. Jahinuzzaman, M. Sharifkhani, M. Sachdev, “An Analytical Model for Soft Error Critical Charge of Nanometric SRAM,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 17, no. 9, Sept. 2009.

[90] Y. V. Pershin, J. Martinez-Ricon, M. D. Ventra, "Memory circuit elements: from systems to applications", arXiv:1006.3598v1, 2010.

[91] B. Widrow, W. H. Pierce, J. B. Angell, "Birth, Life, and Death in Microelectronic Systems", Technical Report No. 1552-2/1851-1, 1961.

[92] S. H. Jo, T. Chang, W. Lu, "Nanoscale Memristor Device as Synapse in Neuromorphic Systems", America Chemical Society Nano Letters, vol. 10, pp. 1297-1301, 2010.

[93] P.-F. Chiu et al., “Low Store Energy, Low VDDmin, 8T2R Non-Volatile Latch and SRAM with Vertical-Stacked Resistive Memory (memristor) Devices for Low Power Mobile Applications,” IEEE J. Solid-State Circuits, vol. 47, pp. 1483-1496, Jun. 2012.

[94] Y. Shuto, S. Yamamoto, and S. Sugahara, “Static noise margin and powergating efficiency of a new nonvolatile SRAM cell based on pseudo-spintransistor architecture”, IEEE International Memory Workshop (IMW), vol. 16, pp.1-4, 2012.

APPENDIX A

THE RELATION OF CRITICAL CURRENTS AND CRITICAL VOLTAGE

The traditional static noise margin uses the concept of critical voltage to describe the SRAM stability, which is somewhat correlated to the critical currents. In order words, for two given set of system parameters, if the traditional SNM critical voltage for a particular set is higher than the other, the critical current for that set would also be higher than the other one.

From the model equation (5.17) in Chapter V, we display here in (A.1) as shown below:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_1, V_2 + V_{N1}) + I_{N1} \\ C_2 \cdot \dot{V}_2 = f_2(V_1 - V_{N2}, V_2) + I_{N2} \end{cases}, \tag{A.1}$$

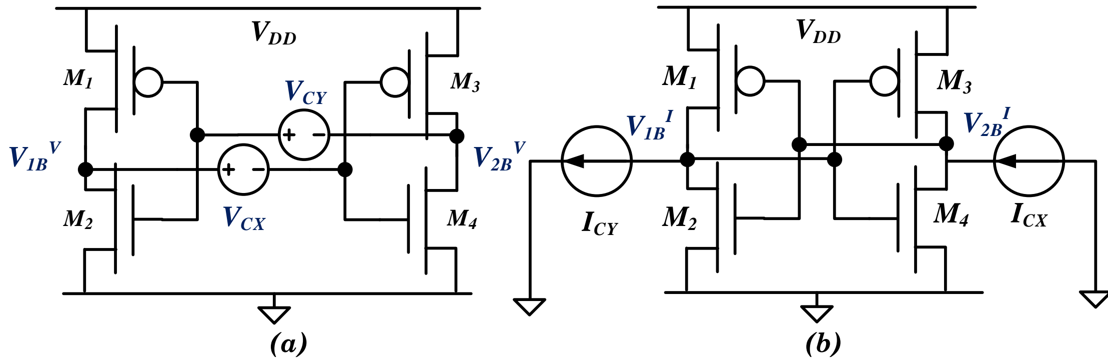


Fig. A.1 The circuit setup for (a) the critical voltage; (b) the critical current.

it can be seen that the V_{N1} and I_{N1} appear in dV_1/dt equation, and V_{N2} and I_{N2} appear in dV_2/dt equation. We will show that V_{N1} is highly correlated to I_{N1} and V_{N2} is highly correlated to I_{N2}. The idea is that, if somehow we can Taylor expand V_{N1} and V_{N2} out of

function f_1 and f_2, then the I_{N1} would be the sum of higher order terms of V_{N1}. Therefore, the higher V_{N1} gives higher I_{N1}.

Figure A.1 shows the circuit setup for critical voltage and critical current. The dynamic equations for critical voltage is as follows:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_{1B}^V, V_{2B}^V + V_{CX}) = 0 \\ C_2 \cdot \dot{V}_2 = f_2(V_{1B}^V - V_{CY}, V_{2B}^V) = 0 \end{cases} \tag{A.2}$$

where (V_{1B}^V, V_{2B}^V) is the bifurcation point for a chosen critical voltage ($V_{N1}=V_{CX}$, $V_{N2}=V_{CY}$) that makes the dynamic equations dV_1/dt and dV_2/dt equal to zero. Similarly, the dynamic equations for critical current is the following:

$$\begin{cases} C_1 \cdot \dot{V}_1 = f_1(V_{1B}^I, V_{2B}^I) - I_{CY} = 0 \\ C_2 \cdot \dot{V}_2 = f_2(V_{1B}^I, V_{2B}^I) + I_{CX} = 0 \end{cases} \tag{A.3}$$

where (V_{1B}^I, V_{2B}^I) is the bifurcation point for a chosen critical current ($I_{N1}=I_{CX}$, $I_{N2}=I_{CY}$) that makes the dynamic equations dV_1/dt and dV_2/dt equal to zero. Notice that the bifurcation points, (V_{1B}^V, V_{2B}^V) and (V_{1B}^I, V_{2B}^I), are not the same. In fact, they are different in most of cases.

The next procedure would be Taylor expand V_{CX} and V_{CY} out of f_1 and f_2 in (A.2) and then match with (A.3). Equation (A.2) can be rewritten to:

$$\begin{cases} f_1(V_{1B}^I + \Delta V_1, V_{2B}^I + \Delta V_Y) = 0 \\ f_2(V_{1B}^I + \Delta V_X, V_{2B}^I + \Delta V_2) = 0 \end{cases} \tag{A.4}$$

where those newly introduced variables are:

$$\begin{cases} \Delta V_1 = V_{1B}^V - V_{1B}^I \\ \Delta V_2 = V_{2B}^V - V_{2B}^I \\ \Delta V_X = \Delta V_1 - V_{CX} \\ \Delta V_Y = \Delta V_2 + V_{CY} \end{cases}. \tag{A.5}$$

The Taylor expansion on (A.4) would be:

$$\begin{cases} f_1(V_{1B}{}^I, V_{2B}{}^I) + \left.\dfrac{\partial f_1}{\partial V_1}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_1 + \left.\dfrac{\partial f_1}{\partial V_2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_Y + H.O.T. = 0 \\ f_2(V_{1B}{}^I, V_{2B}{}^I) + \left.\dfrac{\partial f_2}{\partial V_1}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_X + \left.\dfrac{\partial f_2}{\partial V_2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_2 + H.O.T. = 0 \end{cases} \tag{A.6}$$

After matching (A.3) and (A.6), it is evident to see that I_{CX} and I_{CY} are sum of all the higher order terms. The Taylor expansion to the 2nd order for I_{CX} and I_{CY} would be:

$$\begin{cases} I_{CX} = I_{CX}^{1st} + I_{CX}^{2nd} \\ I_{CY} = -(I_{CY}^{1st} + I_{CY}^{2nd}) \end{cases} \tag{A.7}$$

where 1st and 2nd denote the expansion to the 1st and 2nd order, and their expressions are :

$$\begin{cases} I_{CY}^{1st} = \left.\dfrac{\partial f_1}{\partial V_1}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_1 + \left.\dfrac{\partial f_1}{\partial V_2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_Y \\ I_{CX}^{1st} = \left.\dfrac{\partial f_2}{\partial V_1}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_X + \left.\dfrac{\partial f_2}{\partial V_2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_2 \end{cases} \tag{A.8}$$

and

$$\begin{cases} I_{CY}^{2nd} = \dfrac{1}{2}\left.\dfrac{\partial^2 f_1}{\partial V_1{}^2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_1{}^2 + \left.\dfrac{\partial^2 f_1}{\partial V_1 V_2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_1 \cdot \Delta V_Y + \dfrac{1}{2}\left.\dfrac{\partial^2 f_1}{\partial V_2{}^2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_Y{}^2 \\ I_{CX}^{2nd} = \dfrac{1}{2}\left.\dfrac{\partial^2 f_2}{\partial V_1{}^2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_X{}^2 + \left.\dfrac{\partial^2 f_2}{\partial V_1 V_2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_X \cdot \Delta V_2 + \dfrac{1}{2}\left.\dfrac{\partial^2 f_2}{\partial V_2{}^2}\right|_{\substack{V_{1B}{}^I \\ V_{2B}{}^I}} \cdot \Delta V_2{}^2 \end{cases} \tag{A.9}$$

According to the definition of traditional static noise margin, it treats $V_{CX}=V_{CY}=V_C$, and V_C would be the length of the square fits into the eye of voltage transfer curves. On the other hand, we set $I_{CX}=I_{CY}=I_C$ accordingly. The bifurcation points (V_{1B}^V, V_{2B}^V) and (V_{1B}^I, V_{2B}^I) can be acquired by solving the following expressions:

$$\begin{cases} f_I(V_{1B}^I, V_{2B}^I, I_C) = f_1(V_{1B}^I, V_{2B}^I) - I_C = 0 \\ g_I(V_{1B}^I, V_{2B}^I, I_C) = f_2(V_{1B}^I, V_{2B}^I) + I_C = 0 \\ h_I(V_{1B}^I, V_{2B}^I, I_C) = \left(\dfrac{\partial f_I}{\partial V_1} \dfrac{\partial g_I}{\partial V_2} - \dfrac{\partial f_I}{\partial V_2} \dfrac{\partial g_I}{\partial V_1} \right) \Bigg|_{\substack{V_{1B}^I \\ V_{2B}^I}} = 0 \end{cases} \quad \text{(A.10)}$$

and

$$\begin{cases} f_V(V_{1B}^V, V_{2B}^V, V_C) = f_1(V_{1B}^I, V_{2B}^I + V_C) = 0 \\ g_V(V_{1B}^V, V_{2B}^V, V_C) = f_2(V_{1B}^I - V_C, V_{2B}^I) = 0 \\ h_V(V_{1B}^V, V_{2B}^V, V_C) = \left(\dfrac{\partial f_I}{\partial V_1} \dfrac{\partial g_I}{\partial V_2} - \dfrac{\partial f_I}{\partial V_2} \dfrac{\partial g_I}{\partial V_1} \right) \Bigg|_{\substack{V_{1B}^I \\ V_{2B}^I}} = 0 \end{cases} . \quad \text{(A.11)}$$

The procedure to solve (A.10) and (A.11) is similar to the procedure discussed in Chapter VII. They are three equations solving for three unknowns. The analytical formula solution is not been developed due to the difficulty of solving 4th order polynomial. Once it is solved, bifurcation points (V_{1B}^V, V_{2B}^V) and (V_{1B}^I, V_{2B}^I) will only be in terms of system parameters. Then, V_C to I_C conversion can be done using only equations with system parameters.

Table A.1. The Critical Voltage and Critical Time on Five Random Design Choices Using Numerical Method on L-1 Model

Test Data	V_{1B}^{V}	V_{2B}^{V}	V_{1B}^{I}	V_{2B}^{I}	V_C *(V)*	I_C *(uA)*	ΔV_1	ΔV_2	ΔV_X	ΔV_Y
1	1.5046	0.0607	1.1762	0.2903	0.559	52.4	0.328	-0.229	-0.231	0.3298
2	2.1206	0.1768	1.7106	0.4835	0.705	64.1	0.409	-0.306	-0.295	0.3984
3	0.9040	0.0744	0.7374	0.1978	0.287	20.7	0.166	-0.12	-0.121	0.1639
4	1.2443	0.0762	1.0272	0.2768	0.421	26.7	0.216	-0.200	-0.204	0.2210
5	1.0219	0.0902	0.8454	0.2471	0.334	25.6	0.175	-0.156	-0.158	0.1773

Table A.2. The Comparison on the Exact Values vs. 2st Order Expansion ($V_{CX}=V_{CY}$)

Test data	The Exact $I_{CX} = I_{CY}$ (uA)	I_{CX} (uA) To the 2nd order	I_{CY} (uA) To the 2nd order	I_{CX} Error	I_{CY} Error
1	52.41	52.41	5.2.42	*0.000011%*	*0.021938%*
2	64.06	64.06	64.06	*0.000004%*	*0.000004%*
3	20.72	20.72	20.72	*0.000002%*	*0.000017%*
4	26.67	26.67	26.67	*0.000002%*	*0.000002%*
5	25.55	25.55	25.55	*0.000003%*	*0.000005%*

Table A.3. The Comparison on the Exact Values vs. 1st Order Expansion ($V_{CX}=V_{CY}$)

Test data	The Exact $I_{CX} = I_{CY}$ (uA)	I_{CX} (uA) To the 1st order	I_{CY} (uA) To the 2nd order	I_{CX} error	I_{CY} error
1	52.41	55.44	46.25	5.47%	11.76%
2	64.06	66.68	59.28	3.93%	7.46%
3	20.72	21.52	19.26	3.72%	7.07%
4	26.67	27.07	26.19	1.50%	1.79%
5	25.55	26.06	24.90	1.98%	2.53%

Furthermore, we use Newton-Raphson on five random design choices shown in Table A.1. The results in Table A.1 are the exact values. We then compare on the exact values to the values from 2nd order Taylor expansion formula in Table A.2 and 1st order expansion in Table A.3. As we can see, the 2nd order expansion match the exact value closely, and the 1st order expansion has error averagely around 6.1%.

In conclusion, the developed critical current concept aligns well with critical voltage which is used in traditional static noise margin. As it can be seen in Table A.1, that higher the V_C would give higher I_C. Therefore, the critical voltage and critical current is correlated.