ANALOG AND MIXED SIGNAL DESIGN TOWARDS A MINIATURIZED SLEEP APNEA MONITORING DEVICE

A Dissertation

by

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ABSTRACT

Sleep apnea is a sleep-induced breathing disorder with symptoms of momentary and often repetitive cessations in breathing rhythm or sustained reductions in breathing amplitude. The phenomenon is known to occur with varying degrees of severity in literally millions of people around the world and cause a range of chronicle health issues. In spite of its high prevalence and serious consequences, nearly 80% of people with sleep apnea condition remain undiagnosed. The current standard diagnosis technique, termed polysomnography or PSG, requires the patient to schedule and undergo a complex full-night sleep study in a specially-equipped sleep lab. Due to both high cost and substantial inconvenience, millions of apnea patients are still undiagnosed and thus untreated. This research work aims at a simple, reliable, and miniaturized solution for in-home sleep apnea diagnosis purposes. The proposed solution bears high-level integration and minimal interference with sleeping patients, allowing them to monitor their apnea conditions at the comfort of their homes.

Based on a MEMS sensor and an effective apnea detection algorithm, a low-cost single-channel apnea screening solution is proposed. A custom designed IC chip implements the apnea detection algorithm using time-domain signal processing techniques. The chip performs autonomous apnea detection and scoring based on the patient's airflow signals detected by the MEMS sensor. Variable sensitivity is enabled to accommodate different breathing signal amplitudes. The IC chip was fabricated in standard 0.5-μm CMOS

technology. A prototype device was designed and assembled including a MEMS sensor, the apnea detection IC chip, a PSoC platform, and wireless transceiver for data transmission. The prototype device demonstrates a valuable screening solution with great potential to reach the broader public with undiagnosed apnea conditions.

In a battery-operated miniaturized medical device, an energy-efficient analog-to-digital converter is an integral part linking the analog world of biomedical signals and the digital domain with powerful signal processing capabilities. This dissertation includes the detailed design of a successive approximation register (SAR) ADC for ultra-low power applications. The ADC adopts an asynchronous 2b/step scheme that halves both conversion time and DAC/digital circuit's switching activities to reduce static and dynamic energy consumption. A low-power sleep mode is engaged at the end of all conversion steps during each clock period. The technical contributions of this ADC design include an innovative 2b/step reference scheme based on a hybrid R-2R/C-3C DAC, an interpolation-assisted time-domain 2b comparison scheme, and a TDC with dual-edge-comparison mechanism. The prototype ADC was fabricated in 0.18μm CMOS process with an active area of 0.103 mm^2, and achieves an ENoB of 9.2 bits and an FoM of 6.7 fJ/conversion-step at 100-kS/s.

DEDICATION

To my Mother

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1. INTRODUCTION

"Be not ashamed of mistakes and thus make them crimes."

– Confucius

1.1 Building Miniaturized Medical Electronics

As predicted by the Moore's Law [3], the feature size of semiconductor devices has been rapidly decreasing over the years and has now developed into the nanometer scale regime. Therefore, the design of both analog and digital CMOS (Complementary Metal-Oxide Semiconductor) circuits have received tremendous benefits especially in terms of lower power consumption and smaller device area. Electronic circuits now can be designed and built with reduced fabrication cost, advanced processing power, and prolonged battery life. This technological trend has provided a huge boost in the development of modern portable consumer electronics such as mobile smartphones and tablet computers.

Although traditionally a much slower-moving industry compared to consumer electronics, the medical electronic device market has seen a rapid adoption of advanced semiconductor technology as well. As a result, a variety of medical equipment that conventionally operates in hospitals, clinics, or medical labs has become portable and suitable for home and point-of-care scenarios. Diabetes patients now can monitor their blood glucose levels anywhere they go with a portable glucose meter. Even insulin injection devices can be miniaturized into implantable pumps controllable by an external handheld remote. Portable medical electronics such as there, among many others, are now revolutionizing

the healthcare industry and benefiting patients of different pathological conditions in various ways.

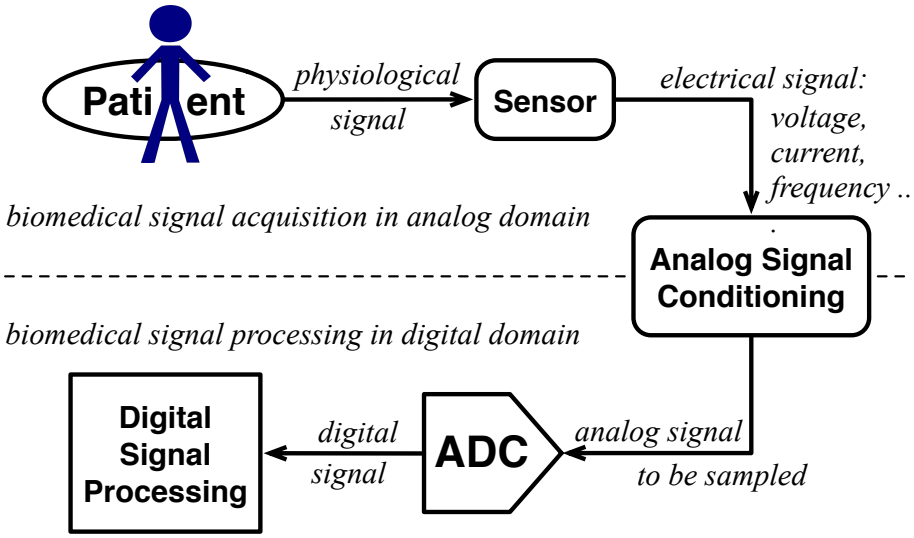

Figure 1.1: Top level view of a general medical electronic device based on digital signal processing.

Medical conditions are measured and analyzed in different ways according to their respective natures, however, the top level design of medical electronics can be described in a general way as illustrated in Fig. 1.1. The patient is connected with a certain type of sensor to capture physiological signals that contain biomedical information for a certain disease or condition. The sensor acts as a transducer to generate electrical representations, either in voltage, current, or frequency, of the acquired signal. Since all physiological signals are inherently in analog format and often accompanied with interfering signals including noise and artifacts, they need to be conditioned, usually amplified and filtered, using analog circuits. The conditioned analog signal is then sampled and digitized by the analog-to-digital

converter (ADC) so that the biomedical information can be extracted, analyzed, and evaluated in digital domain using digital signal processing (DSP) techniques. Softwares are normally required to utilize powerful and sophisticated DSP algorithms.

Alternatively, a medical device can also be approached by specialized circuits instead of general purpose functional blocks as demonstrated in Fig. 1.1. Depending on the level of signal processing needed, an Application-Specific Integrate Circuit (ASIC) may provide a more compact and energy-efficient solution for dealing with certain medical conditions. Instead of using general purpose ADC and DSP circuits, an ASIC solution allows optimized hardware based on specific needs or purposes during the process of analyzing and evaluating pathological conditions. As shown in Fig. 1.2, an ASIC may include signal conditioning circuits as well as special purpose circuits for realizing signal processing algorithms. The final results after data measurement and analysis are generated using hardware rather than software.

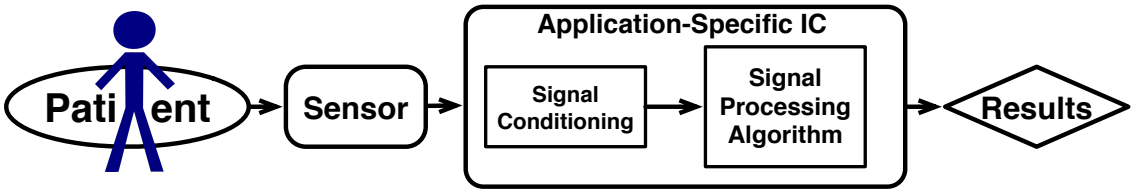

Figure 1.2: Top level view of a general medical electronic device based on application-specific ICs.

It is difficult to compare the pros and cons of the two aforementioned approaches without the context of a specific disease or condition. In cases where the requirement for signal processing is relatively simple and straightforward, the ASIC approach is favorable

in terms of small device footprint and low power consumption. When sophisticated signal processing algorithms are needed, it is beneficial to move to digital/software domain for more powerful computation capabilities. This chapter will continue on to discuss the background of sleep apnea and its current diagnosis method. The rest of this dissertation is organized as follows: Chapter 2 reviews the existing sleep apnea monitoring techniques suitable for portable diagnosis purposes and describes the system level overview of the proposed sleep apnea monitoring solution; Chapter 3 presents the proposed apnea monitoring IC chip design using the time-domain hardware-based detection algorithm; Chapter 4 demonstrates the design of a prototype apnea monitoring device based on the proposed apnea monitoring IC, and its clinical testing procedures and results; Chapter 5 describes the design of an ultra-low power ADC suitable for miniaturized battery-operated medical devices including the proposed apnea monitoring device; Chapter 6 concludes this research work.

1.2 The Field of Portable Medical Devices

With the assist of advanced semiconductor manufacturing technology, a myriad of sophisticated yet affordable personal medical devices proliferated during the past decade. The development of portable medical devices have become the center of various academic and commercial endeavors. Due to their different nature compared to traditional medical equipments, portable medical devices are transforming the entire healthcare industry in terms of interactions between patients and doctors, medical costs, and disease diagnosis and monitoring procedures. The rapid growth of the portable medical device market comes

from a host of factors including:

1. An aging population needing constant health care and monitoring
2. Skyrocketing costs of traditional physician-directed medical care
3. Increasingly stringent health insurance payout policies
4. Increasing consumer awareness of the benefits of personal medical products
5. The positive feedbacks of widespread consumer devices online and in retail stores

Nowadays, consumers are able to monitor vital signs, including electrocardiogram (ECG), blood oxygen level (SpO_2), blood glucose level, and etc, either at home or on the go without needing to pay costly and inconvenient visits to the hospital. Consumer medical devices, such as heart rate monitors, blood pressure monitors, blood glucose monitors, and insulin pumps, represent the fastest-growing segments in the medical equipment market. Besides meeting the requirements regulated by government entities such as the Food and Drug Administration (FDA), the consumer portable medical devices should meet other stringent requirements to be successful in the market, such as

1. Convenience of use for patient
2. Ease of result interpretation
3. High reliability and safety
4. Low-power operation and long battery life
5. High measurement accuracy
6. Small form factor
7. Affordable device cost

8. Other . . .

The category of consumer or portable medical electronic device development entails a vast research and industrial field with goals towards the diagnosis, treatment, and monitoring of various medical conditions and diseases. Building a device for a specific kind of illness may require entirely different knowledge, strategy, and physical hardware than that of another kind, but often requires collaborative efforts and expertise from multiple disciplines. Therefore, it is virtually impossible to apply a single design method in all medical design tasks and be successful. However, we can distill the essence of developing a successful piece of medical equipment by examining the evolution of blood glucose monitoring techniques for diabetes patients.

Although glucose meters are widely available today, monitoring and managing blood glucose level was once considered impossible. Invented by Ernie Adams in 1963, the first glucose indicator was a paper strip named *Dextrostix* that develops a blue color with an intensity proportional to blood glucose concentration which could be read by visual comparisons between the strip's color and an approximate color-concentration relation chart. In 1970, the first blood glucose meter and glucose self-monitoring system was developed by Anton H. Clemens. The system was named the Ames Reflectance Meter (ARM) and was designed to detect reflected light from a *Dextrostix*. Weighing 3 lb and costing 650 dollars, this ARM device was intended for physician office use only.

For a long time, the practice of blood glucose level testing have been done strictly inside clinics or hospitals. For severe diabetes who needs everyday monitoring, lab tests are

simply too expensive and inconvenient to perform at such high frequencies. The rapid development of silicon (Si) semiconductor technology has made modern electronics smaller and cheaper than ever, which paved way for the emerge of hand-held glucose meters. Modern blood glucose meters fit into the patient's palm, weight only a few ounces, and cost less than 20 dollars. Modern glucose meters are composed of two essential parts: an enzymatic reaction and a electronic detector [4]. The glucose meter's enzyme portion is generally packaged in a dehydrated state in the form of disposable strips that accept whole blood samples, and is incorporated into a biosensor that generates electrons to be detected by the detector portion.

The advancement of MicroElectroMechanical System (MEMS) technology allows the fabrication of mechanic systems in micrometer scale. MEMS-based devices are controllable electronically, which when coupled with integrated circuit (IC) technology allows the birth of many implantable medical devices. Nowadays, blood glucose level not only can be monitored but also managed via implantable real-time insulin pumps which are fabricated using MEMS technology. The insulin pump microchip can be inserted into tissues just under the skin [5] and transmits data wirelessly to a small receiver externally worn on the patient. With such a device implanted, the patient no longer needs to prick a finger every time to collect blood samples. The insulin pump automatically regulates the blood glucose level and thus avoids the need of manually injecting medicine every so often. As a result, the device greatly reduces pain and inconvenience for diabetes patients, allowing them to enjoy everyday life as much as healthy individuals.

The evolution of blood glucose level monitoring and managing techniques that has briefly described here sends an important message: a successful medical device should be built on patient needs and take advantage of appropriate technologies available. Although design approaches and physical components needed may be different for treating other diseases and conditions, the ultimate goal in building a medical device should be always guided by the patient's need to improve their quality of life. The designer should always attempt to survey available technologies applicable in their specific design tasks in order to allow patients to satisfy their needs at reduced costs, improved convenience, and enhance experience.

1.3 Sleep Apnea: A Brief Background

Sleep apnea is a sleep-induced breathing disorder with symptoms of momentary and often repetitive cessations in the breathing rhythm or sustained reductions in the breathing amplitude [6]. The disorder causes ventilatory inadequacies, sleep state fragmentation, and frequent arousals from sleep during the night. Long-term sleep apnea patients usually suffer from a range of health issues as medical sequelae of the condition. The sleep apnea phenomenon is known to affect millions of people around the world with various degrees of severity. Even though strong indications of its widespread existence dated back to as early as the 19th Century, people have only begun to study and understand this problem over the past 50 years [7].

In the mid 1960s, the association between sleep apnea and obesity in patients with Pickwickian syndrome was fully recognized by Gastaut [8]. The discovery provided as the

first comprehensive link relating obesity and daytime sleepiness to sleep-induced breathing irregularities. However, related research proceeded very slowly during the decade following these observations. Various findings during the time period of mid 1970s through early 1990s formed a major impetus to medical research in the field of sleep-induced breathing disorder. J. Orem *et al.* studied the effects of sleep on both brain stem respiratory neuronal activity and reflex control mechanism of breathing [9, 10]. J. E. Remmers *et al.* described the mechanism of human upper airway occlusion during sleep at the anatomical and neurophysiological level[11], providing the definition of obstructive sleep apnea (OSA) pathogenesis. Shortly thereafter, C. E. Sullivan and colleagues made the landmark introduction of continuous nasal pressure (CPAP) application as the noninvasive treatment for obstructive sleep apnea [12]. In 1993, the first population study, commonly referred to as the Wisconsin Sleep Cohort, conducted in-laboratory studies of to reveal the correlation of sleep and breathing in the public population. The study showed a significant prevalence of sleep-disordered breathing (including sleep apnea) in a middle-aged non-clinical population, giving evidence for the largely undiagnosed condition of sleep apnea and its potentially significant effect on public health [13].

From the mid 1990s onwards, the sleep apnea condition has been the focus of many researchers from various disciplines and clinical specialties. Tremendous research efforts have been made aiming toward the causes, consequences, and treatment of sleep-induced breathing disorders. Meanwhile, being a potentially serious and not well defined clinical problem, sleep apnea has fermented the growth of many commercial ventures focusing

on the diagnosis and treatment of the condition. Sleep clinics and other business entities were built in large quantities in the United States and other countries in the western world. Today, sleep medicine has grown into a clinical as well as research specialty due to the high prevalence of sleep apnea and its pathological and social consequences.

1.4 Prevalence and Sequelae of Sleep Apnea

The Wisconsin Sleep Cohort Study accomplished in 1994 collected data over a 4-year period based on samples of adults 30–60 years of age. The results of the study uncovered a high prevalence of sleep apnea with approximately 42 million or 20% of american adults being affected [13]. The findings were also confirmed by other later US population-based studies [6]. Since obesity is a strong causal factor for sleep apnea [14, 15], and due to the ongoing obesity epidemic in the United States [16], the prevalence of sleep apnea is still on the rising trend. The ongoing Wisconsin Sleep Cohort Study obtained more sleep data during the period of 2007–2010 based on a total of 1,520 participants who were 30–70 years of age. Calculating over different age and sex groups based on improved models, the newly estimated prevalence published in 2013 has increased to 26% [17], representing a substantial overall increase of 30% compared to the study results unveiled nearly two decades ago.

Besides its high prevalence in the general population, the sleep apnea condition also causes a range of harmful health consequences [7]. Immediate effects include intermittent arterial hypoxemia and hypercapnia, sleep state fragmentation, and exaggerated fluctuations in heart rhythm, blood pressure, and intra-thoracic pressure [18]. In turn, these acute

physiologic disruptions evolve into long-term sequelae, such as (1) cardiovascular diseases including hypertension [19, 20], stroke[21, 22], and cardiac dysrhythmias [23], (2) decrements in cognitive function including impaired memory and concentration [24], and (3) altered insulin sensitivity and homeostasis of glucose regulation causing or contributing to the development of diabetes [25]. Secondary sequelae of sleep apnea include brain and myocardial infarction induced by hypoxemia under ventilatory inadequacies [21, 26]. Sleep apnea causes premature death [27, 28] in infants and has also been associated with sudden infant death syndrome (SIDS) [29]. Sleep apnea in adults can also indirectly affects mood and cause psychiatric issues such as depression and anxiety [30, 31]. Daytime sleepiness due to reduce sleep quality also contributes to social problems such as traffic accidents [32] and work injuries [33]. Fig. 1.3 highlights the prevalence of apnea in several different comorbidities.

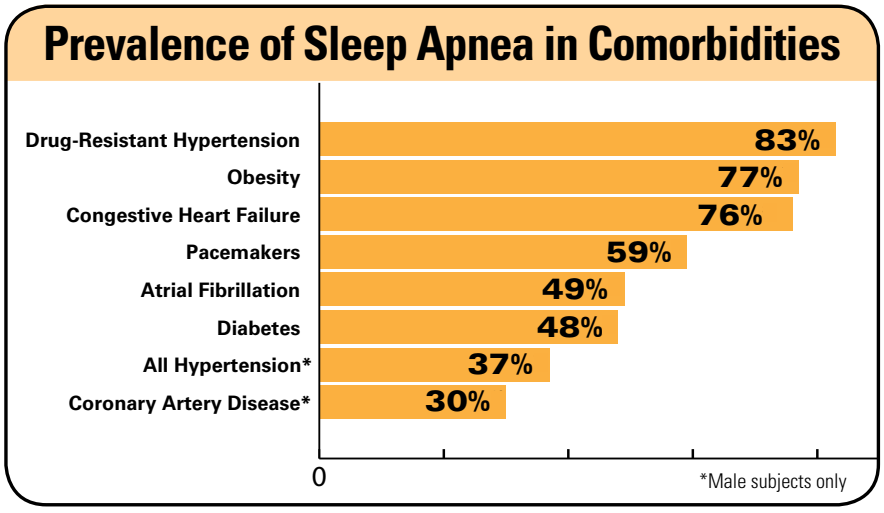

Figure 1.3: Prevalence of sleep apnea in comorbidities. Image courtesy of ResMed, Inc..

From the healthcare economics standpoint of view, the medical cost inflicted by the diagnosis and treatment of sleep apnea also represents a major sector for healthcare spending and consumes a significant amount of public healthcare resources. Fig. 1.4 illustrates the annual healthcare dollar spending for several different medical conditions. The obstructive sleep apnea, which is a dominant subset of sleep apnea, demands $165 billion in the US market each year, only second to spending in Cardiovascular diseases (CVD) and Stroke.

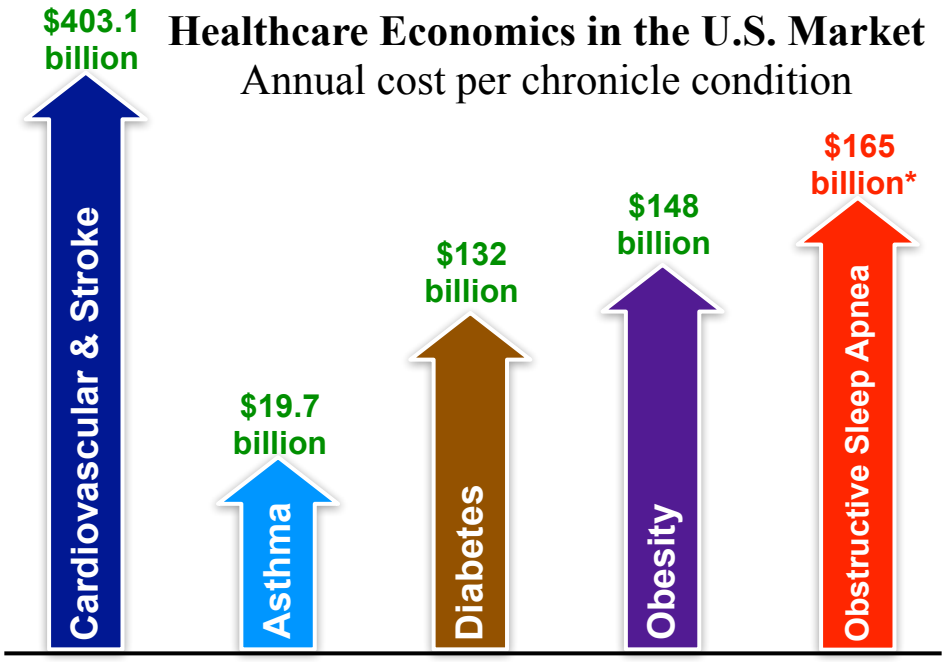

Figure 1.4: Top annual-spending chronicle conditions in the U.S. market. Data sources: Centers for Disease Control and Prevention (2012) and McKinsey/Harvard Medical School (2010).

1.5 Sleep Apnea Diagnosis

Sleep apnea conditions are diagnosed based on sleep studies, which are tests that measure how well the patient sleeps and how the patient's body behaves under abnormal sleep

conditions. These sleep tests require substantial hardware complexity to record related physiological parameters and extensive clinical expertise to score the sleep data in terms of severity. Therefore, it is of significant importance to understand such technical and clinical details so as to pave way for the development of at-home sleep apnea diagnosis devices.

1.5.1 Severity of Sleep Apnea – The Apnea-Hypopnea Index

The sleep apnea condition is a sleep-induced breathing disorder which refers to two main events: the *apnea* event and the *hypopnea* event. During an apnea event, the patient experiences momentary and often cyclical interruptions in the breathing rhythm. During a hypopnea event, the patient has momentary or sustained reductions in the breath amplitude, along with reduced blood oxygen level (SpO_2). Both apneas and hypopneas can be accompanied by 1) a compromised, often entirely closed, extrathoracic upper airway leading to airflow blockage, or an "obstructive" event; 2) a marked reduction or cessation of brain stem respiratory motor output leading to the complete absence of breathing effort, or a "central" event; and 3) a combination of central and obstructive events[34, 35]. Of the three different forms of apnea condition, the obstructive sleep apnea (OSA) type is much more clinically significant due to its higher prevalence indicated by several population-based studies. The mechanism of OSA is graphically illustrated in Fig. 1.5. Since obesity is a significant comorbidity to OSA, the current rising trend of the obesity epidemic is expected to contribute to a higher OSA prevalence in the future.

Both apnea and hypopnea events are characterized by their time durations under marked

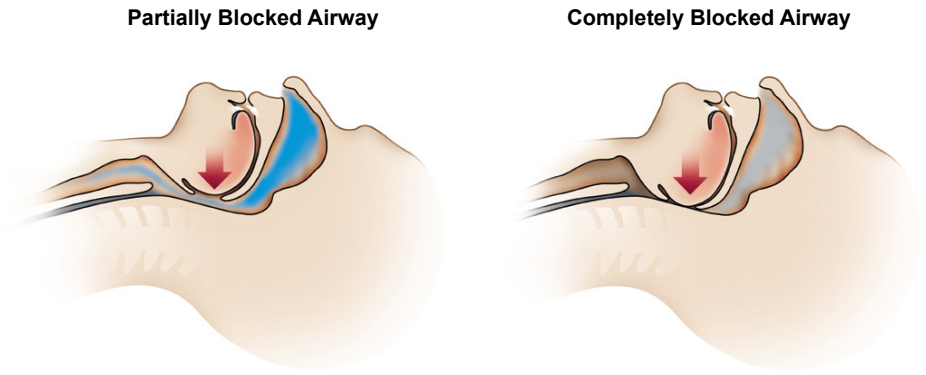

Figure 1.5: Causes of obstructive sleep apnea (OSA): partially (left) and completely (right) blocked upper airway. Image courtesy of ResMed, Inc.

thresholds, and are used for apnea severity assessment. According to the standards outlined by the American Association of Sleep Medicine (AASM), an apnea event is characterized when the respiratory amplitude decreases below 20% of normal level for a continuous time period of at least 10 seconds [36], while a hypopnea event is characterized when the respiratory amplitude drops below 70% of normal value along with the association of 3-4% drop in SpO_2 level and/or an electroencephalographic (EEG) -based arousal. The overall severity of sleep apnea is quantified or scored by the total number of apnea and hypopnea events observed per hour of sleep, i.e. the Apnea-Hypopnea Index or AHI value. Table 1.1 summarizes the severity of sleep apnea condition based on AHI scores. According to the Wisconsin Sleep Cohort Study [37], approximately 1 in 5 adults has at least mild (AHI $= 5-15$) obstructive sleep apnea and 1 in 15 adults has OSA of moderate or worse severity (AHI > 15).

Table 1.1: Severity of sleep apnea and AHI values

AHI	Severity
0-5	Normal range
5-15	Mild sleep apnea
15-30	moderate sleep apnea
>30	severe sleep apnea

1.5.2 Polysomnography – The Gold Standard Diagnosis Approach

Sleep apnea decrease quality of life and impose a series of medical risks to patients, therefore the proper diagnosis of sleep apnea is of paramount importance from both social and economic standpoints. As recommended by the American Association of Sleep Medicine (AAMS) [38, 39], the current gold standard for sleep apnea diagnosis is the Polysomnography (PSG) study. The diagnosis technique requires the patient to stay at a specially equipped sleep laboratory for a full-night study attended by sleep specialists [40]. This complex diagnosis method records multiple physiological parameters including electroencephalogram (EEG), electrooculogram (EOG), electrocardiogram (ECG), respiratory activity, blood oxygen levels (SpO_2), among other data channels [39]. Sticky patches with sensors and electrodes are placed on various locations of the patient's body such as scalp, face, chest, limbs, and one of their fingers. During the sleep study, these sensors detect signals including brain activity, eye movements, heart rate and rhythm, blood pressure, and the blood oxygen level. Elastic belts are placed around the patient's chest and belly, which measure respiratory efforts defined by the strength and duration of chest movements

during inhale and exhale breathing events.

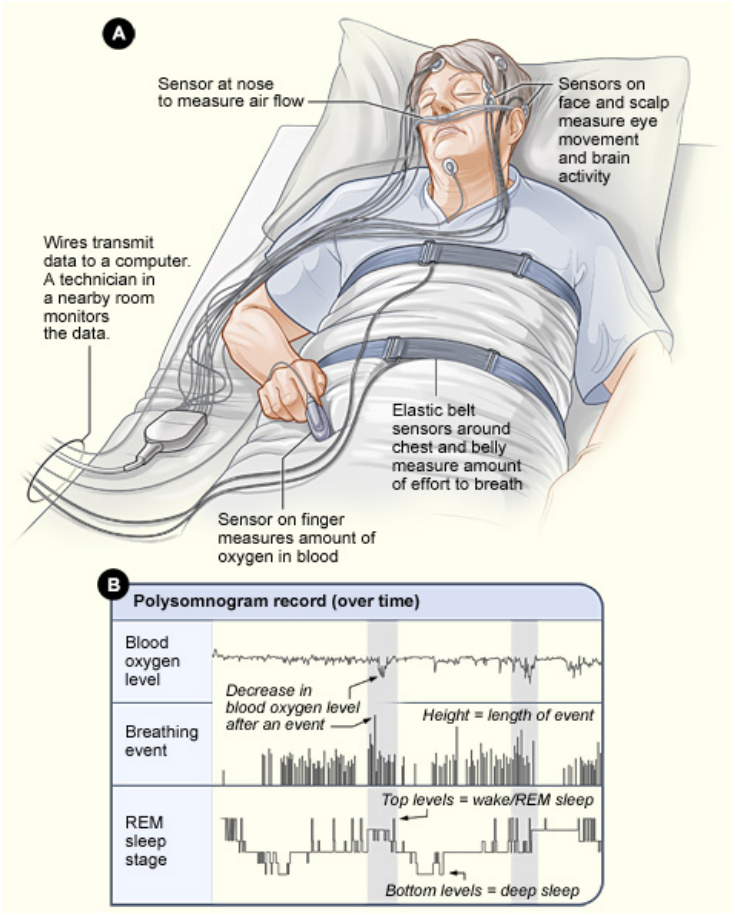

Figure 1.6: Typical setup of a standard polysomnography study. Image courtesy of National Heart, Lung, and Blood Institute (NHLBI).

Fig. 1.6 illustrates the typical setup of a standard polysomnography study in a sleep lab. In Fig. 1.6(A), the patient lies in bed with various sensors and electrodes attached to the body. Physiological data were collected and transmitted to a computer or workstation in a control room via wires attached to the sensors and electrodes. The wires are often bundled together to reduce their restriction to the patient's movement as much as possible so they don't cause discomfort or disrupt sleep. In Fig. 1.6(B), the polysomnogram recording

shows the blood oxygen level, breathing event, and rapid eye movement (REM) sleep stage over time, among other physiological data channels.

1.6 Research Focus

As the current gold standard for sleep apnea diagnosis, the polysomnography technique has been proven to be a reliable method for monitoring sleep apnea conditions and evaluate its severity. However, PSG requires substantial technical expertise, and is labor intensive and time consuming in terms of clinical practice. For the majority of apnea patients, inexpensive and timely access to PSG studies is a big problem, which makes them continue to have undiagnosed sleep apnea. In the Wisconsin sleep cohort study, 93% of women and 82% of men with moderate-to-severe sleep apnea did not receive diagnoses. Thus, there is a growing interest in alternative approaches to diagnosis, such as portable monitoring techniques that are suitable in the diagnostic assessment of patients with suspected sleep apnea in their own homes.

The main focus of this research is to build an inexpensive apnea monitoring solution and provide access to apnea diagnosis to the broader public. Current portable apnea monitoring devices involve fewer data channels [41] to allow unattended in-home testing. In practice, however, such devices are still somewhat too complex for the average patient to apply and often generate inconsistent results. Therefore, a simple and reliable single-channel device would be more appreciated for in-home apnea monitoring purposes. Such a device would help the doctors to determine further diagnosis method, as well as to suggest the proper therapy based on the patient's real-time progress.

2. SLEEP APNEA MONITORING

2.1 The Polysomnography Study

The gold standard approach to diagnosis sleep apnea is the in-laboratory technician-attended polysomnography study over a full-night sleep period. As recommended by the American Academy of Sleep Medicine in their 1997 and 2005 publications titled "*Practice Parameters for the Indication for Polysomnography and Related Procedures*", using polysomnography for the evaluation of sleep apnea requires the following signals as a minimum set of data channels: electroencephalography (EEG), electrooculography (EOG), chin electromyogram (EMG), breathing airflow, arterial oxygen saturation (SpO_2), respiratory effort, and electrocardiography (ECG) or heart rate [38, 39]. The breathing airflow amplitudes and blood oxygen levels directly determines the occurrence of apnea and hypopnea events, while the respiratory effort data help judge the specific type or nature of each apnea event, i.e. obstructive, central, or mixed. When EEG and EMG signals are simultaneously recorded, sleep staging tasks can be performed to provide a denominator for the AHI scoring. Other channels like anterior tibialis EMG is useful in detecting arousals based on patient body movement, thus providing added value of assessing periodic limb movements that may relate to breathing disorders during sleep.

Alternative diagnostic tools recommended by the same AASM documentation include (1) nocturnal oximetry: may be sufficient in assessing a sleep disorder where the severity of hypoxemia is the principal pathological issue and sleep stage or sleep apnea assessment

is not required; and (2) pulmonary function tests: may be useful to determine the level of respiratory dysfunction. Either technique is not as comprehensive as the PSG method in terms of recorded data channels necessary for apnea scoring, therefore they are much less frequently used for clinical diagnostic purposes.

2.2 Portable Sleep Apnea Monitor

Due to the associated expertise intensity and technical complexity, the polysomnography study is only performed in well-equipped sleep laboratories, making it a rather expensive and inconvenient diagnostic method for the majority of sleep apnea patients. For sleep apnea patients seeking more approachable diagnostic techniques in terms of cost and convenience, one question naturally arises: are there any portable solutions? can sleep apnea diagnosis be done at the comfort of the patient's home? In fact, portable or in-home sleep apnea monitoring devices have gained increased interest in both medical research and commercial development.

2.2.1 AASM Regulations

In the present day clinical practice, portable sleep apnea devices have been distributed to patients for screening purposes. The clinical guidelines published by the *Portable Monitoring Task Force of the American Academy of Sleep Medicine* in [1] made recommendations on the use of portable monitoring techniques in the diagnosis and management of patients with OSA. As a general principle suggested by AASM, portable monitoring "should be integrated into a comprehensive program of patient evaluation and treatment under the direction of a sleep specialist board certified in sleep medicine," and "be regu-

lated by policies and procedures that maximize the reliability and validity of the diagnostic process." Fig. 2.1 illustrates the decision tree for using portable sleep monitoring devices towards patients with suspected sleep apnea conditions. Although the current stringent requirements limit the range of apnea patients suitable for portable monitoring, the AASM expects that future studies and developments will expand the sleep apnea population appropriate for portable monitoring studies.

2.2.2 Different Types of Portable Monitoring Solutions

The term portable monitoring encompasses a wide range of devices that can record as many signals as does attended polysomnography or only one signal, such as with oximetry. The EEG and EMG signals are recorded when sleep staging is to be performed to provides a denominator for AHI scoring. More commonly, EEG and EMG signals are not recorded by portable monitors, in which case breathing events are usually quantified per hour of monitoring time as a respiratory disturbance index (RDI). Portable monitors were classified into the following four different types according to the 1994 review published by *American Sleep Disorders Association (ASDA)* [42] and as well as the 2003 practice parameter article published by the AASM [43].

Type I: Polysomnography. The in-lab technician-attended PSG technique is considered the reference standard to which the other monitor types were compared. The physiologic signals that were recorded and used to define a breathing event on a portable monitor varied among studies and across monitor types. As detailed below, the other types of monitors normally encompass less data channels or measuring requirements.

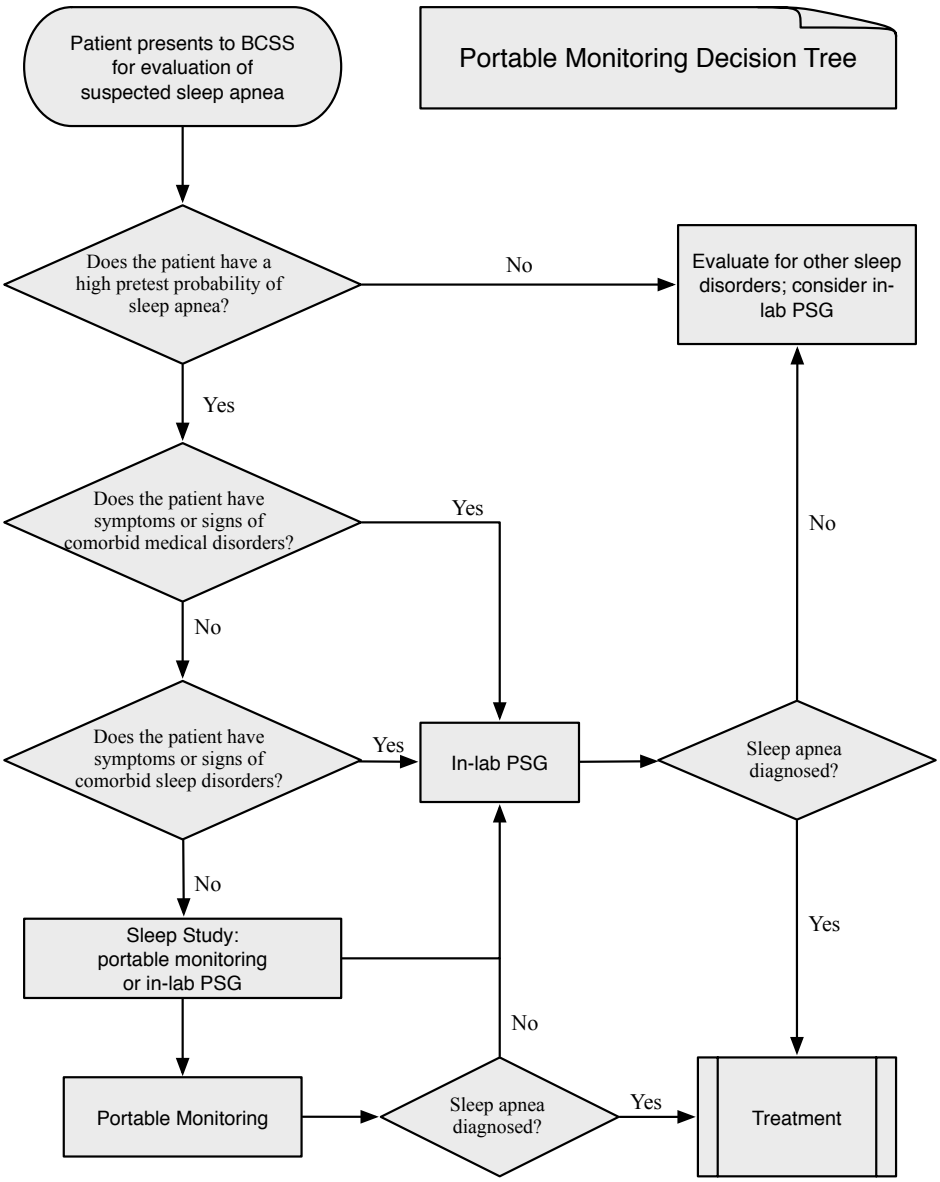

Figure 2.1: Portable monitoring decision tree recommended by the Portable Monitoring Task Force of the American Academy of Sleep Medicine [1].

Type II: Comprehensive portable polysomnography. These monitors incorporate a minimum of seven channels, including EEG, electrooculogram, chin EMG, ECG or heart rate, airflow, respiratory effort at thorax and abdomen, and oxygen saturation. This type of monitor allows for sleep staging and therefore for the calculation of an AHI, but do not need the attendance of sleep technologists.

Type III: Reduced-channel portable devices. This type of monitor incorporates a minimum of four monitored channels, including ventilation or airflow (at least two channels of respiratory movement at thorax and abdomen, or respiratory movement and airflow), heart rate or ECG, and oxygen saturation.

Type IV: Continuous single or dual bio-parameter devices. Most monitors of this type measure a single parameter or two parameters, for example, oxygen saturation or airflow. A monitor not meeting the criteria for type III, i.e. a monitor that measured one to three channels or did not include airflow despite having four channels, is classified as type IV.

Table 2.1 outlines the detailed requirements for the aforementioned different types of sleep apnea monitor devices for both in-lab and in-home uses. In spite of the high prevalence and seriousness of the condition, nearly 80% of people with sleep apnea remain undiagnosed and untreated [6]. Current screening procedures involve paper questionnaires without any physiological data collection and thus lead to a rather high false-negative rate [44]. Therefore portable monitoring devices with reduced channels may serve as a better screening method for the purpose of increasing diagnosis rate among sleep apnea patients. Proper treatment of sleep apnea allows people to feel physical and mentally

Table 2.1: Four types of sleep monitors and requirements on data recording channels

	Type I	Type II	Type III	Type IV
Other names	Polysomnography	Comprehensive portable devices	Reduced-channel portable devices	continuous single or dual bioparameter devices
Application place	Sleep laboratory	home	home	home
Attendance	attended	unattended	unattended	unattended
Requirement or Recommendations	full sleep staging	minimum of 7 channels	minimum of 4 channels	using 1–2 channels
Recorded Data channels	EEG EOG ECG/Heart rate Chin EMG Limb EMG Respiratory effort Air Flow Oxygen saturation Additional channels*	EEG EOG ECG/heart rate EMG Air Flow Respiratory effort Oxygen saturation	Air Flow Respiratory effort ECG/heart rate Oxygen saturation	Air Flow Oxygen saturation (or other channels that allow direct calculation of an AHI or RDI as the result of measuring data)
* Includes: CPAP/BiPap levels, CO2, pH, pressure, etc.				

better, suffering less from lacking of energy during daytime, depression, anxiety, etc.

2.3 Signals Used in Portable Monitoring

Portable sleep apnea monitoring usually involves a subset of the data channels comprising the polysomnography method. The following list includes the most common signals entities grouped into physiological conditions for portable sleep apnea detection and diagnosis:

1. Oximetry: measurement of blood oxygen level and sometimes heart rate.
2. Respiratory monitoring, including but not limited to:
   (a) Breathing effort
   (b) Breathing airflow
   (c) Snoring
   (d) End-tidal CO_2
   (e) Esophageal pressure
3. Cardiac monitoring, including but not limited to:
   (a) Heart rate or heart rate variability
   (b) Arterial tonometry
4. Measurements of sleep wake activity, including but not limited to:
   (a) Electroencephalography
   (b) Actigraphy
5. Body position monitoring
6. Other ...

As indicated by the above list, there can be vastly different ways in building portable monitors that record various signals to detect breathing events. There are also heterogeneity with respect to using different techniques to record specific physiological parameters that define an apnea or other abnormal breathing event using a portable sleep monitor. As will be explained in details below, the most commonly used parameters to detect breathing events are reduction in breathing airflow, drop in blood oxygen level, and under some circumstances both of these methods applied simultaneously.

1. Breathing airflow: Measuring reductions in breathing airflow is the standard method defined by AASM for detecting an apnea or hypopnea event. The recommended criterion for defining an apnea event is airflow reductions of $< 10\%$ from the measurement baseline, and $< 50\%$ for the hypopnea case. The traditional method to quantify breathing flow is the pneumotachograph. However, this technology is not friendly for portable monitors due to its large size.
   (a) Thermistor: Thermistors detect temperature differences in breathing airflow. Since thermistors do not possess a linear relationship with true airflow, they have not been recommended for clinical research purposes. However, they remain to be the most common technique for defining breathing events due to their capability of detecting nasal and oral airflows.
   (b) Nasal pressure: Nasal pressure provides a linear approximation of airflow through the nose. It may not accurately differentiate an apnea from a hypopnea; but in routine clinical use this drawback is not regarded to be significant. Ther-

mistors could provide a poor quality signal when the patient breaths through the mouth for long periods of time, making it difficult to be used in an unattended at-home sleep study where visual signals are not available for cross checking.

2. Respiratory Plethysmography: When properly calibrated, respiratory inductance plethysmography is capable of measuring breathing tidal volume. It is primarily used in conjunction with other channels during the polysomnography study. It is not a common channel in unattended portable studies due to the complexity and cumbersomeness to apply by the patient.
3. Oxygen saturation: Oxygen saturation levels are measured by oximeters. Most oximeters detect the drop in oxygen saturation when it comes to analyzing the oxygen saturation signal, while others detect oxygen re-saturation. In identifying sleep apnea events in patients, some studies measure the accumulative time during which the oxygen saturation drops by $< 90\%$, while other studies quantify the variability of oxygen saturation over an entire study.

Other apnea event defining methods include the recurring of snoring sound in combination with oxygen desaturation as an auxiliary criterion [45]. Snoring combined with heart rate variability has also been used for event detection [46]. Spectral analysis based on the heart rate signal was also explored to define sleep apnea events [47].

2.4 Methods for Scoring Apnea Events

As we have discussed previously, portable sleep apnea monitoring varies in the physiologic data used for analysis, the criteria used to define events, and the algorithm used to score events. In general, portable sleep studies based on monitors measuring airflow by thermistor perform manual scoring, while studies based on monitors measuring nasal pressure perform automated scoring [48]. Some studies allow for manual checking along with computer-based automated scoring algorithm.

Compared to manual scoring, automated scoring provides the advantage of eliminating errors or inconsistencies due to the difference in the scorer's recognition of events. In reality, the gold standard method of the polysomnography study utilize manually scoring to determine whether or not patients have sleep apnea. Therefore, it often appears to be difficult to perform parallel comparison between the portable method and the polysomnography method as a reference. When portable sleep apnea devices are used for screening purposes however, such results validation discrepancies are of much less concern since the portable devices do not replace the PSG method as a complete diagnosis method; rather, the portable study is used as a "pre-test" to determine whether further PSG study is required on particular patients.

2.5 Proposed Sleep Apnea Monitoring System

The goal of this research work is to design towards an in-home sleep apnea monitoring device that is minimum in footprint, easy to apply, cost effective, and reliable in apnea

measurement and scoring. For breathing signal detection, we propose to use a MEMS (micro-electro-mechanical systems) pressure sensor as a transducer to measure nasal (and oral) airflows, which is deemed as the most reliable parameter for apnea detection [49]. Fig. 2.2 conceptually illustrates a miniaturized facial-wearable apnea monitoring device that can be realized using high-level integration SoC (system-on-chip), which incorporates a MEMS sensor and customize designed integrated circuits (ICs) for apnea detection and scoring algorithm. The MEMS sensor is a piezo-resistive transducer that can be integrated with semiconductor IC technology, thus offers the maximum potential for device size reduction. Such a device would have minimum interference with the patient's sleep due to the fact that it is applied directly to the facial area and uses minimal length cannula to pick up the breathing airflow pressure signals. The battery-operated feature together with the wireless connectivity of the device eliminates the need of any electrical cords, therefore entirely avoiding the possible entanglement of cables during the patient's sleep in many other apnea monitoring devices.

In order to build towards the sleep apnea monitoring device demonstrated conceptually in Fig. 2.2, we propose the system level architecture for the apnea monitoring system as illustrated in Fig. 2.3. The system entails a MEMS pressure sensor to detect the breathing airflow signal, followed by an Analog Signal Conditioning block for signal amplification and filtering. Afterwards, two different signal paths function in parallel to enable (1) hardware based apnea detection and scoring capability using the Sleep Apnea Detection circuitry, and (2) original breathing signal recording using the Low Power A/D Converter

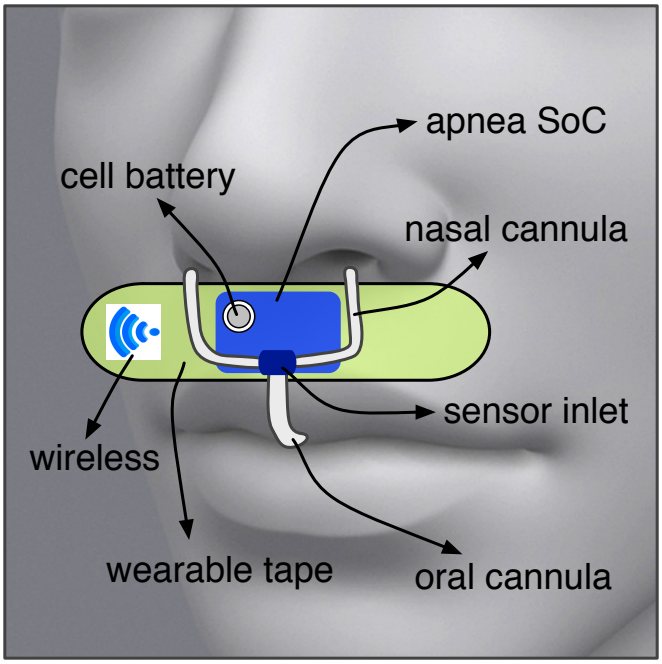

Figure 2.2: Wearable patch bearing a miniaturized sleep apnea detection device.

for post-study comprehensive analysis. The apnea scores (in digital format) from the first signal path, as well as the digital breathing waveforms from the second signal path, are processed, stored, and transmitted wirelessly to mobile devices or remote stations through the combination of the digital signal processing (DSP), memory and the wireless transceiver blocks.

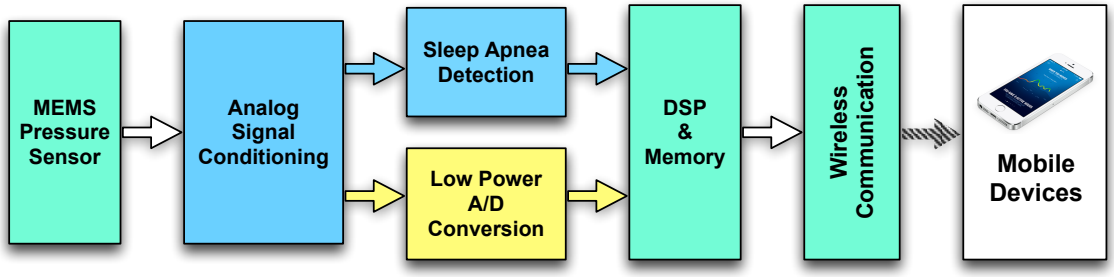

Figure 2.3: System level view of proposed apnea monitoring system.

As will be discussed in details in the forthcoming chapters, an apnea detection and scoring chip (blue blocks in Fig. 2.3) is designed and tested using 0.5μm CMOS technology. The proposed time-domain signal processing algorithm is implemented in a low-complexity integrated circuits to provide on-chip signal conditioning and apnea event detection. A prototype device is designed and tested based on the custom apnea detection chip and commercial circuit blocks (green blocks in Fig. 2.3) for design validation. An ultra-low power 10-bit A/D converter (yellow block in Fig. 2.3) is also proposed for biomedical applications in general with low power and low sampling rate characteristics. The A/D converter adopts a successive approximation register (SAR) architecture using a hybrid R-2R/C-3C DAC, and asynchronously converts 2 bits per step at a sampling rate of 100 kS/s or lower. The ADC is designed and fabricated in standard 180nm CMOS technology and achieves a 6.7 fJ/conversion-step when converting at 100 kS/s with a 600-mV supply.

3. A SLEEP APNEA DETECTION IC CHIP FOR IN-HOME SLEEP TEST*

3.1 Overview

Sleep apnea is a common [6] sleep-disordered breathing condition with symptoms of momentary and often repetitive cessations in respiratory rhythm or reductions in breathing amplitude [7]. Sleep apnea causes intermittent hypoxemia, which often leads to sleep state interruptions and transient arousals during sleep, hence severely undermines the patient's sleep quality. Constant deprivation of oxygen also contributes to the severity and secondary sequelae of brain and myocardial infarction [21, 26]. Clinical and academic research continue to show apnea-related evidence regarding risks of developing a constellation of diseases such as stroke[21, 22], hypertension [19, 20], depression [31], and cardiac dysrhythmias [23] in untreated sleep apnea patients. In North America, according to studies presented in [34], approximately 4% of males and 2% of females, which amounts to a total of 18 million people, suffer from sleep apnea.

In spite of the high prevalence of sleep apnea, nearly 80% of people with such conditions remain undiagnosed and therefore untreated. The main reason for this situation is that the current *gold standard* for sleep apnea diagnosis is both expensive and inconvenient to the patient. The diagnosis technique, termed polysomnography (PSG), requires the patient to undergo overnight sleep studies in a specially equipped sleep laboratory

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[40]. The complex study records multiple physiological parameters including electroencephalogram (EEG), electrooculogram (EOG), electrocardiogram (ECG), respiratory activity, blood oxygen levels (SpO_2) and more [39]. Current apnea screening devices involve fewer data channels [41] to allow in-home testing. In clinical practice, however, such devices are still somewhat complicated for the average patient to apply and often generate inconsistent results. Therefore, a simple and reliable single-channel device would be more appreciated for in-home screening purposes. Such a device would help the doctors to determine further diagnosis method, as well as to suggest the proper therapy based on the patient's real-time progress.

Multiple techniques have been developed to monitor human respiratory activities [51, 52, 53, 54, 55, 56] for the purpose of sleep apnea detection. Werthammer *et al.* [57] reported an acoustic-based method that monitors the patient's respiratory activity by recording the sound of breathing from nasal airflow. More recently, Corbishley *et al.* [58] also proposed an acoustic method using a neck-mounted microphone that records acoustic signals created by the turbulence in the respiratory airway. Both approaches depend on complex frequency analysis to extract breathing information from a variety of interfering signals, increasing design cost and device liability. Video technologies have also been exploited [59], but demand even higher cost due to rigorous signal processing. Nepal *et al.* [60] used an abdominal strain gauge as a transducer for measuring breathing rate via thoracic movements. However, the detection algorithm does not address obstructive apnea with existing thoracic movements but no airflow. SpO_2 level was also analyzed to indicate

respiration rate and apnea in [61], but it was not clear how to detect certain apnea events when oxygen level is unchanged. Beside their individual drawbacks, all of the aforementioned techniques require complicated signal processing algorithms to score apnea events. As a result, post-study analysis of recorded data is often required, adding extra medical cost to the patient.

The esophageal pressure (P_{es}) measurement gives an accurate indication of intra-thoracic pressure which becomes sub-atmospheric during inspiration and decreases further when the upper airway is partially or entirely closed. Therefore, P_{es} is considered as the gold standard measure of respiratory effort to discriminate sleep-disordered breathing especially obstructive sleep apnea. However, the technique is relatively invasive and interfere with sleep since the probe has to be placed inside the patient's esophagus. Alternatively, noninvasive P_{es} surrogates are preferred, such as nasal flow recorded by cannula and thoracic-abdominal movements.

The goal of this work is to develop a simple, cost-effective, yet reliable apnea screening device with auto-scoring capabilities for the home environment. We propose to use a MEMS (micro-electro-mechanical systems) pressure sensor as a transducer to measure nasal airflow, which is deemed as the most reliable parameter for apnea detection [49]. An elegant time-domain signal processing algorithm is implemented in a low-complexity integrated circuit (IC) chip to provide hardware-based autonomous detection. A prototype device is designed and assembled with a MEMS sensor, a custom signal processing IC, and a wireless transceiver for performance verification (in Chapter 4). To the best of our

knowledge, this is the first single-channel apnea screening device with hardware-based scoring capabilities. The rest of this chapter will outline the fundamentals of sleep apnea scoring, present the details of the proposed apnea detection algorithm and system level design considerations, describe the implementation of the proposed signal processing IC, and demonstrates the prototype chip and its test results.

3.2 Sleep Apnea Scoring

There are two main types of sleep apnea: 1) obstructive apnea: induced by partial or complete collapse of extra-thoracic upper airway [34], and 2) central apnea: caused by reduced or ceased output of the brain stem respiratory motor [35]. According to standards outlined by American Association of Sleep Medicine (AASM), apnea occurs when the respiratory amplitude decreases below 20% of normal level for a period of at least 10 seconds [36]. Another related event is hypopnea, where the respiratory amplitude drops below 70% of normal value with the association of 3-4% drop in SpO_2 level and/or an electroencephalographic (EEG) arousal. The overall severity of sleep apnea is measured by the apnea-hypopnea index (AHI), which is the total number of apnea and hypopnea events per sleep hour.

Although it is difficult to definitively classify both apnea and hypopnea events via a single-channel detection, nasal airflow measurement is nevertheless an adequate method to infer the apnea-hypopnea index with good success rate [49]. A simple nasal airflow based device with reduced cost is highly favorable for evaluating potential apnea conditions in a broader population, who would otherwise be undiagnosed and untreated due to the high

cost of standard techniques. Real-time autonomous scoring capability is also essential to a low-cost and in-home screening device. With current techniques, raw sleep data are often manually scored by special personnel, which increases not only medical cost and diagnosis time, but also potential inconsistencies due to different interpretations of rules or unequal experience among individual practitioners.

3.3 Sleep Apnea Detection

3.3.1 Breathing Detection via MEMS Sensor

In the past decade, interest in MEMS technology has grown rapidly for biomedical applications such as pacemakers and biosensors [62]. The MEMS pressure sensor offers features such as small size, low cost and high sensitivity, making it an attractive transducer for measuring nasal airflow pressure. In addition, MEMS sensors can be integrated with CMOS circuits on the same silicon substrate [63, 64], which opens a realistic possibility for an ultra-compact device for apnea detection. Such a device can be very user-friendly and bears minimal intrusion to the patient.

Previous breathing monitoring techniques often involves complicated algorithm for apnea detection. The acoustic method proposed in [58] involves placing a microphone on the neck to record tracheal sound. However, strong in-band interference and artifacts arise from internal sound (such as heartbeat) and external acoustic noise, thus requiring rigorous frequency domain analysis to extract the actual breathing signal. Abdominal strain gauge was used to monitor apnea by detecting the body movements due to respiration efforts [60], but required special algorithm such as second order autoregression to address motion

artifacts issue. Both of these methods demand complex computation for reliable detection, leading to increased analog and digital circuitry for signal processing.

Demonstrated in Fig. 3.1(a) is a breathing signal $V_{sig}(t)$ recorded by a piezoresistive MEMS sensor (connected via a medical nasal cannula) based on its linear pressure-to-voltage response. The signal swings up during exhale activity, i.e. increased air pressure, and swings down during inhale activity, i.e. decreased air pressure. Therefore, it is a direct time-domain representation of the breathing profile. The time instances of exhale/inhale activities are indicated by the crossovers of the signal curve at its DC baseline. Fig. 3.1(b) illustrates the recorded signal's Fourier transform (2048-point FFT) spectrum $|V_{sig}(f)|$, which shows no interference or artifacts within the frequency range of 0.1-1 Hz for respiration signals [65]. These important features of the MEMS pressure sensor give advantage for apnea detection. As will be shown later, signal processing algorithm can be implemented in a much more straightforward fashion compared to previously discussed methods, which makes the MEMS sensor an optimal transducer for a reliable yet cost-effective apnea detection solution.

3.3.2 Time-Domain Apnea Detection Algorithm

As illustrated in Fig. 3.2, breathing signals demonstrate different amplitudes depending on the apnea conditions. During a central apnea event when respiratory efforts are nonexistent, the signal appears as a flat level around DC baseline. For an obstructive apnea event when breathing airflow is obstructed, the detected signal shows a reduced amplitude compared to normal conditions. By applying a detection threshold window, apnea events

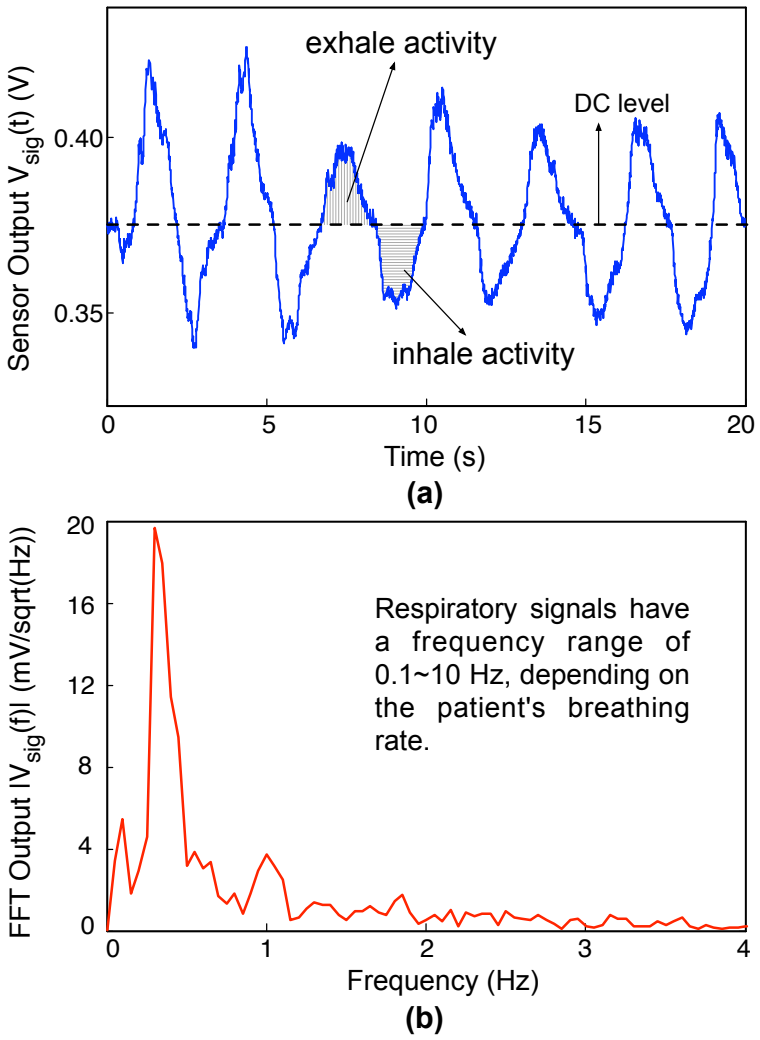


Figure 3.1: Breathing signal recorded by a MEMS pressure sensor: (a) time domain response, and (b) frequency domain content (2048-point FFT).

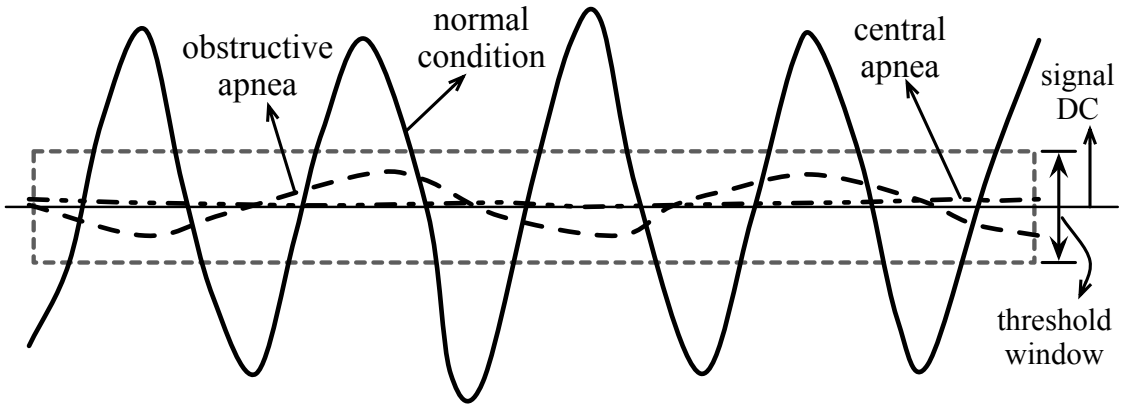


Figure 3.2: Detection threshold window and breathing signals under different apnea conditions: normal, obstructive, and central.

with signal amplitudes falling within the windowed range can be captured. Additionally, the window size should be adjustable for individual patients as their reference values (normal breathing amplitudes) usually vary. In general, the threshold window should be set between 20–70% of reference value, which ensures detection of all apnea events and a certain amount of "quasi" hypopnea events without the presence of SpO_2 or EEG data. By this method, a certain degree of AHI over-scoring is achieved, which is strategically favorable in a screening device to determine the need for further diagnosis. Although this method does not distinguish between central and obstructive apnea, it is sufficient for the purpose of screening since it counts both events into the total AHI value.

The apnea detection algorithm proposed for this work is illustrated in Fig. 3.3. The breathing signal detected by the MEMS transducer is compared to a pre-set threshold window. A timer is used to register the time duration of a potential apnea event. If the signal amplitude exceeds the detection level as in a non-apnea event, the system will reset

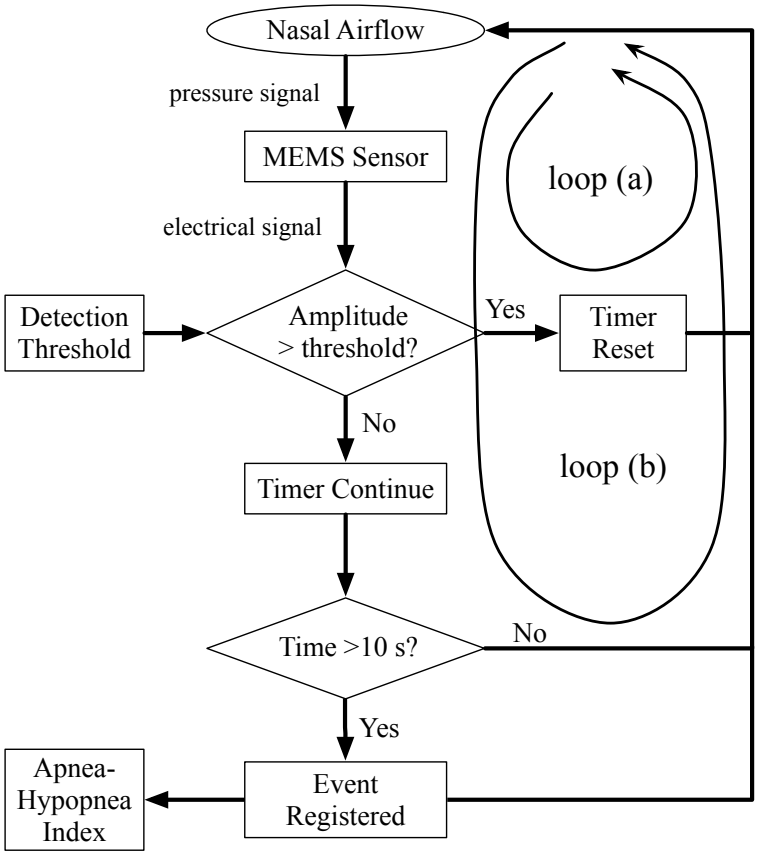


Figure 3.3: Signal flowchart that implements the proposed sleep apnea detection algorithm.

the timer and continue onto loop (a). If the breathing amplitude falls into the threshold window, the timer continues and the total time for the current condition is compared to a reference of 10 s: if total time has lasted for more than 10 s, an apnea event is detected and registered; if total time is less than 10 s, the system continues onto loop (b). The total number of apnea events will accumulate, and the apnea-hypopnea index will be calculated.

The proposed detection algorithm processes breathing data in a real-time fashion, capable of generating scoring results immediately after sleep sessions. In environments where

no dedicated scoring personnel is available, this is a favorable feature since it reduces medical cost and improves convenience. Therefore, compared to previous techniques that relies heavily on post-study data analysis, the proposed algorithm better suits the in-home apnea screening scheme.

3.3.3 System Level Design

Fig. 3.4 illustrates the system block diagram that implements the proposed detection algorithm. The MEMS sensor captures and converts nasal air pressure to an electrical signal. The breathing signal is then amplified by a front-end amplifier and converted into a "pseudo" pulse-position-modulated (PPM) signal by a hysteresis comparator. It's called pseudo-PPM since the modulation is not clocked at a set frequency but rather at the asynchronous breathing rhythm. The pseudo-PPM signal contains exhale and inhale timings at its rising and falling edges, respectively. The breathing rhythm detection (BRD) block indicates breathing cycles by the inhale/exhale timings, followed by the time-to-digital converter (TDC) that digitizes the time duration of each breathing period. A system clock of 25 Hz, provided by an on-chip relaxation oscillator, is used to synchronize all digital logic circuits.

The system represents an low-complexity implementation for apnea detection. The hysteresis window of the comparator offers two major benefits in signal processing: (1) voltage fluctuations at crossovers can be tolerated and false transition edges can be avoided, and (2) variable hysteresis windows serve as adaptive thresholds for patients with different breathing amplitudes. The TDC also compares event durations to the 10-s threshold for

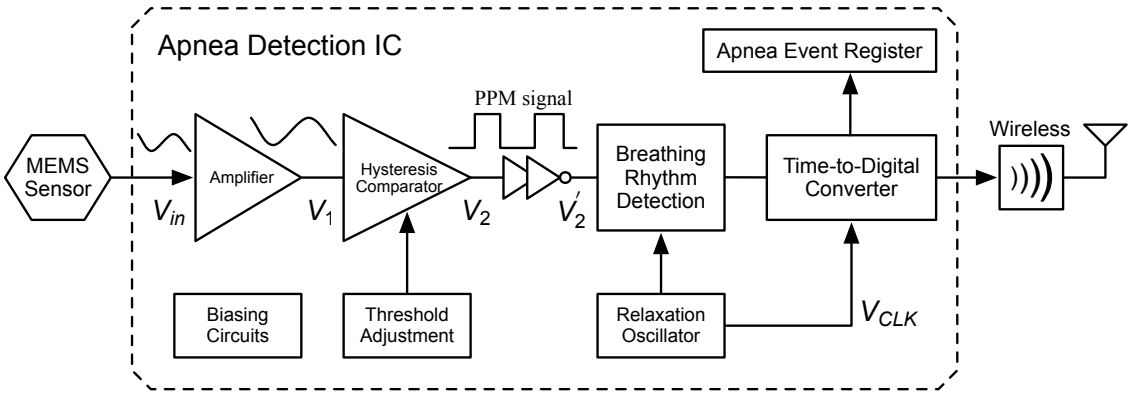


Figure 3.4: System block diagram including the sensor, the signal processing chip, and wireless module for data transmission.

apnea detection, while the total count of apnea events is stored in the Apnea Event Register. As a result, conventional building blocks such as filters, A/D converter (ADC) and digital signal processing (DSP) are not required, saving substantial power and hardware cost.

3.4 Signal Processing IC Design

3.4.1 Front-End Amplifier

The front-end amplifier (FEA) amplifies the breathing signal at the output of the pressure sensor. Fig. 3.5 shows the schematic of the proposed FEA. The operational transconductance amplifier (OTA) is implemented using a single-stage folded cascode structure [66] that provides high DC gain and accurate DC transfer in unity-gain configuration. Input AC-coupling blocks the DC level of the sensor output and restores it to mid-rail voltage V_{mid} for further comparison. The midband gain (A_o) and cut-off frequencies (ω_L and ω_H)

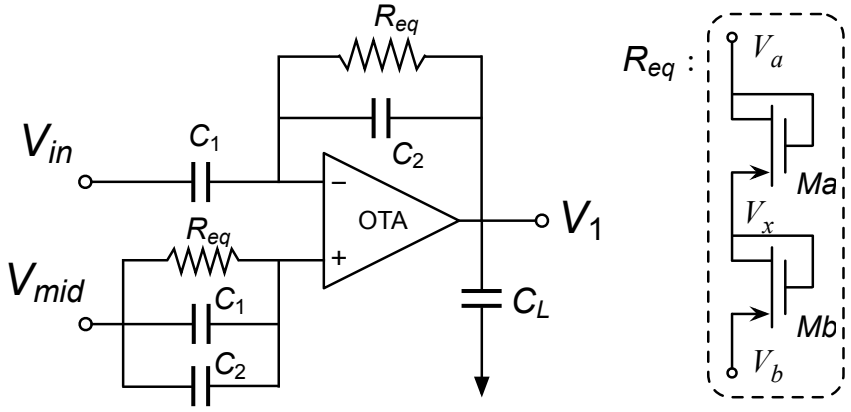


Figure 3.5: Implementation of the front-end amplifier (FEA).

can be expressed as

$$A_o = C_1/C_2 \tag{3.1}$$

$$\omega_L = 1/(R_{eq} \cdot C_2) \tag{3.2}$$

$$\omega_H = g_m/(A_o \cdot C_L) \tag{3.3}$$

where g_m is the transconductance of the OTA.

In order to create poles at ultra-low frequencies down to a few hertz without using off-chip components, diode-connected pMOS transistors *Ma* and *Mb* are used to emulate large resistances (R_{eq}) up to $10^{12}\ \Omega$. These two transistors or diodes operate with relatively small drain-to-source voltages [67, 68] such that the diodes are in off state, allowing minimal passage current and thus providing high resistance. To maintain the off-state for the diodes, it is critical to keep their voltage swings under threshold voltage, which is usually around 0.7 V for normal diodes. The two diodes are stacked in series with the purpose of further

reducing the effective voltage drop ($V_a - V_x$ and $V_x - V_b$) across each of them.

Based on previous discussions on breathing signals captured by the MEMS sensor, the higher corner frequency is not critical due to little interference at higher frequencies. Noise level in biomedical front-end circuits is often a critical design aspect [69], however, it is less of an issue in this particular design due to relatively large input signal levels and the presence of hysteresis window in the comparator.

3.4.2 Hysteresis Comparator with Adjustable Threshold

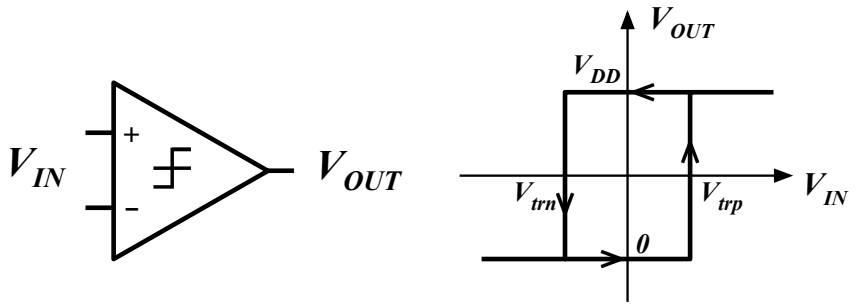


Figure 3.6: A hysteresis comparator and its hysteresis curve for the input and output voltage.

A hysteresis comparator generates a comparison result, "1" or "0", only when the input voltage exceed certain trip voltages. Fig. 3.6 shows the relationship of a hysteresis comparator's input voltage V_{IN} and its corresponding output voltage V_{OUT} as a hysteresis curve, where output voltage level V_{DD} is equivalent to a logic "1" and voltage level 0 is equivalent to a logic "0". In order to generate the result "1" from the state "0", the input voltage has to be increasing to pass the positive trip voltage V_{trp}; whereas in order to generate the result "0" from the state "1", the input voltage voltage needs to be decreasing

to pass the negative trip voltage V_{trn}. The voltage range between V_{trp} and V_{trn} is the hysteresis window, within which the comparator's output state remains unchanged.

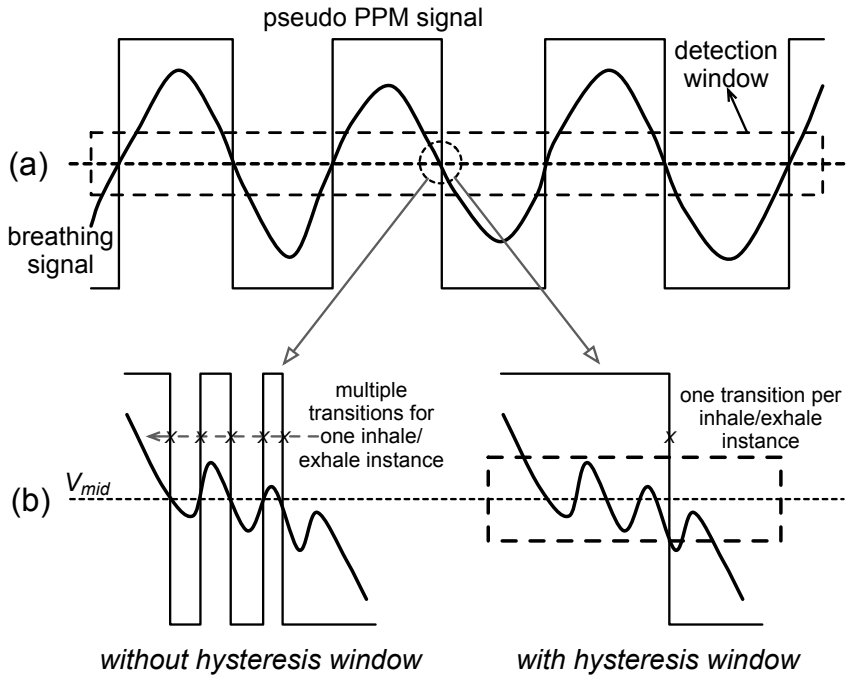


Figure 3.7: Modulation of breathing signal: (a) breathing signals converted into pseudo-PPM signals via comparison, and (b) hysteresis window effectively reduces false transitions due to signal fluctuations at crossovers.

The proposed hysteresis comparator modulates the breathing signal into a series of pulses, or a pseudo-PPM signal, as shown in Fig. 3.7(a). By comparing the input signal with a reference (V_{mid}), the time instances of exhale and inhale activities can be registered as rising and falling edges at the comparator output, respectively. However, voltage fluctuations at crossovers, due to either noise or artifacts, can cause multiple false transitions at a single exhale/inhale instance and create erroneous time information. Rigorous filtering can be employed to address this issue, but at a high cost of device area due to low-

frequency operations. This design overcomes such issue by applying a hysteresis window in the comparator. As illustrated in Fig. 3.7(b), with a hysteresis window size of proper size, only one transition edge is triggered for each breathing instance.

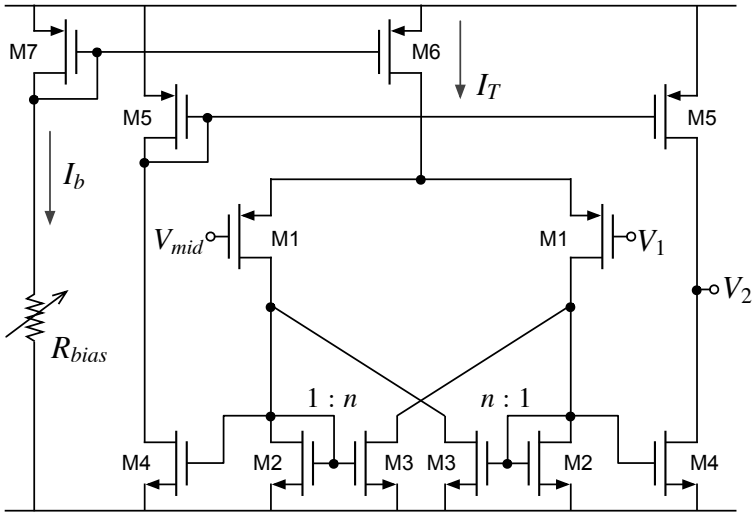


Figure 3.8: Implementation of hysteresis comparator with hysteresis window tunable via bias resistor R_{bias}.

In order to perform autonomous hardware scoring, an adjustable detection threshold is required for accommodating patients with different breathing amplitudes. The comparator's variable hysteresis window plays a vital role in such an adaptive detection mechanism. As shown in Fig. 3.8, the comparator is a high-gain, open-loop structure with both negative and positive feedback paths. Hysteresis effect exists in the voltage transfer curve when the dimension ratio $n = \frac{(W/L)_3}{(W/L)_2} > 1$ between M3 and M2, indicating positive feedback stronger than negative feedback. Assuming proper transistor matching, trip voltages

of the hysteresis curve can be derived as [70]:

$$V_{trp}^{+} = \left|V_{trp}^{-}\right| = \sqrt{\frac{2I_T}{\beta_1}}\left(\sqrt{\frac{n}{1+n}} - \sqrt{\frac{1}{1+n}}\right) \tag{3.4}$$

where I_T is the tail current through M6, and β_1 is the transconductance coefficient of M1. Thus, the hysteresis window can be tuned by the ratio n or the tail current I_T. Fig. 3.9 shows the variation of the comparator's hysteresis window width according to different current bias conditions. Considering the input signal amplitude and the gain of FEA stage, the hysteresis window is designed to be tunable in the range of $(\pm)\ 50 \sim 150$ mV via the external bias resistor R_{bias}.

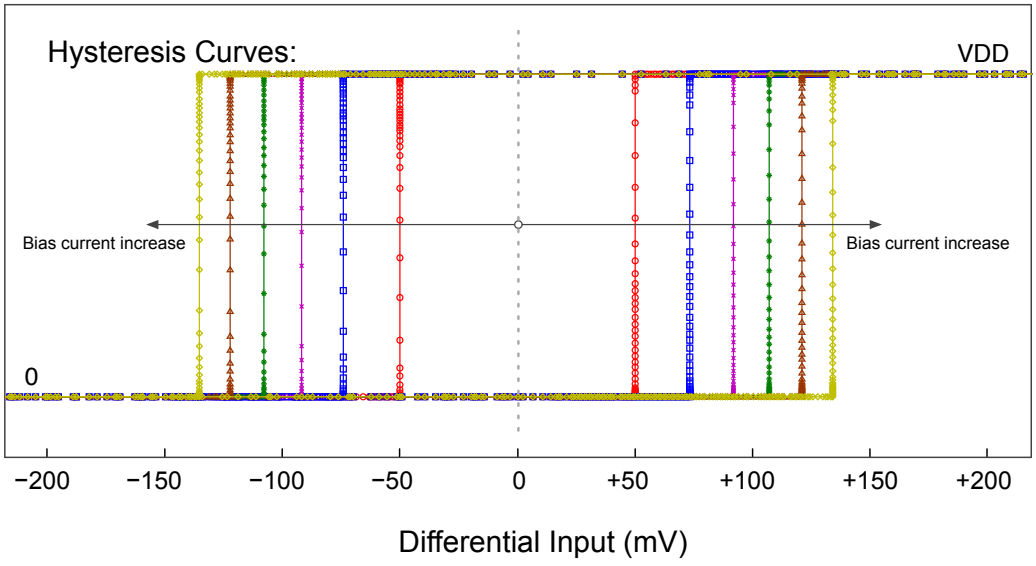


Figure 3.9: Adjusting hysteresis window via bias current.

3.4.3 Breathing Rhythm and Apnea Detection

The function of the BRD block is to detect the breathing rhythm, i.e. the time instances of inhale or exhale activities. The implementation of the BRD circuitry is illustrated in Fig. 3.10, which consists of digital logics that recognize breathing activities (exhale and inhale) via the pseudo-PPM signal's rising and falling edges. The breathing cycle can be defined using both rising edges and falling edges in the PPM signal. In this implementation, each breathing cycle and its time period is defined by consecutive rising edges or inhale instances.

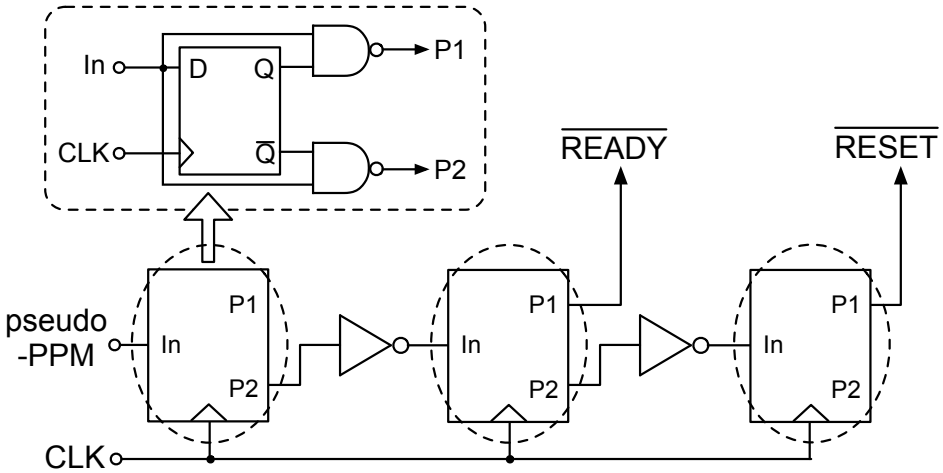


Figure 3.10: Implementation of the BRD logics.

The function of the TDC is to digitize the time duration of each breathing cycle detected by the BRD block. As shown in Fig. 3.11, the TDC consists of a synchronous 10-bit counter based on T flip-flops and generates a 10-b word representing the time period of each breathing cycle defined by the BRD. The combination of TDC and BRD

together detects sleep apnea events when the time elapse of breathing cycles exceed the time threshold of 10 s. As illustrated in the timing diagram in Fig. 3.12, the BRD logics generate an active-low *READY* signal when a complete breathing cycle between two consecutive inhale instances has been observed, which triggers TDC data transfer within one clock cycle. Afterwards, the *RESET* signal (active-low) is activated for one clock period to reset the TDC's output to '0', followed by a new time-to-digital conversion session for the next breathing cycle.

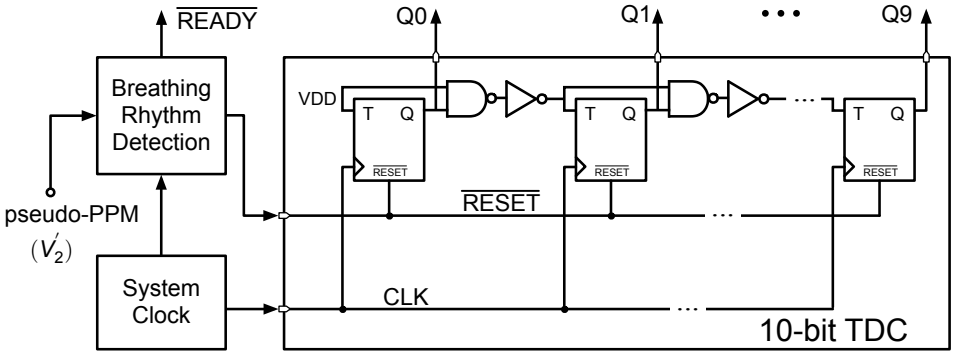


Figure 3.11: Breathing rhythm and apnea detection based on the BRD logic and the TDC.

Based on a system clock at 25 Hz, the 10-bit TDC operates with a time resolution of 40 ms and a maximum recordable time duration of 40 s. Since the *MSB-2* bit represents the 10-s threshold for apnea detection, it is utilized to trigger up-counts for total number of apnea events when *MSB-2* goes from '0' to '1'. Synchronized by the *READY* signal, the digital output of the TDC is interfaced with an off-chip transmitter and wirelessly transferred to a remote computer for scored results.

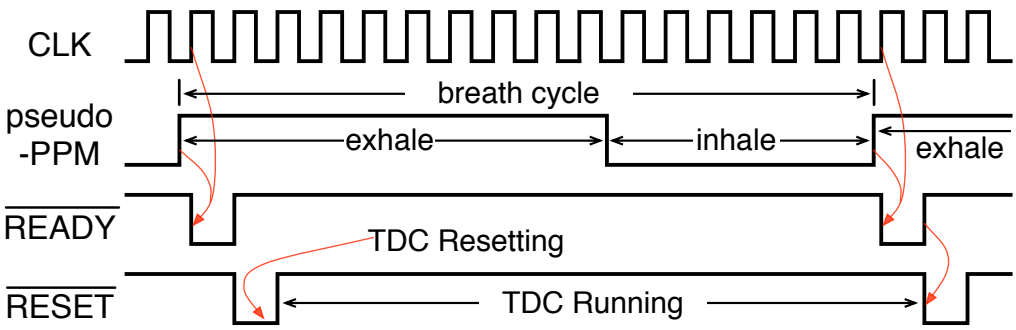


Figure 3.12: Timing diagram of the BRD signals.

3.4.4 Tunable Relaxation Oscillator

The on-chip system clock synchronizes the digital algorithm for breathing detection and time digitization. The design of the system clock entails trade-offs between speed, time resolution, and power consumption. Essentially, the clock period defines the time resolution of the TDC and thus the accuracy of the breathing rate and apnea event duration. A faster clock leads to a more accurate time resolution, but also to a high power consumption. For this particular application, a 1% accuracy for breathing period should be reasonable. Assuming the breathing rate to be 1 Hz, the system clock frequency should be 100 Hz in order to achieve such an accuracy.

On-chip oscillators are widely used in systems where device size, power, and cost are important aspects of the design task. There exist different oscillator options of which the ring oscillator and relaxation oscillator are the most popular ones. Based on cascaded combination of delay stages, the ring oscillator is an architecture very friendly in modern CMOS technologies. However, it would require many delay stages to arrive at very low

frequencies, making the ring oscillator inefficient in both area and power in this particular application. The relaxation oscillator is based on charging and discharging an energy storage element which provides the level or state for the excitation of a periodic output signal. The output signal frequency can be controlled by the charging/discharging speed and the size of the element, and is arguably the best option for a monolithic on-chip oscillators for low-frequency clock generation.

Fig. 3.13 shows the proposed relaxation oscillator for system clock generation. In order to achieve low frequency oscillation, current-limiting transistors MP2 and MN2 source a 2-nA current for ultra-slow charging and discharging of the 1-pF load capacitor C_L. The capacitor voltage turns around when it reaches the threshold of the comparator. As a result, a low-speed sawtooth signal forms across the load capacitor with a period T_o expressed as

$$T_o = V_{HW} \cdot C_L \cdot \left(\frac{1}{I_{bp}} + \frac{1}{I_{bn}} \right) \tag{3.5}$$

where V_{HW} is the hysteresis window of the comparator [70] inside the oscillator, and I_{bp} and I_{bn} are the bias currents of both MP2 and MN2, respectively. The output clock is buffered by a D flip-flop, which divides the clock frequency by a factor of 2. Compared to [71], the hysteresis window extends the threshold level for voltage trip-over, achieving even lower switching frequency at the output of the oscillator. Although crystal oscillator provides a more accurate clock, the relaxation oscillator is a preferred choice in this approach due to its simplicity and energy-efficiency. The output clock frequency can be conveniently calibrated and tuned via current bias.

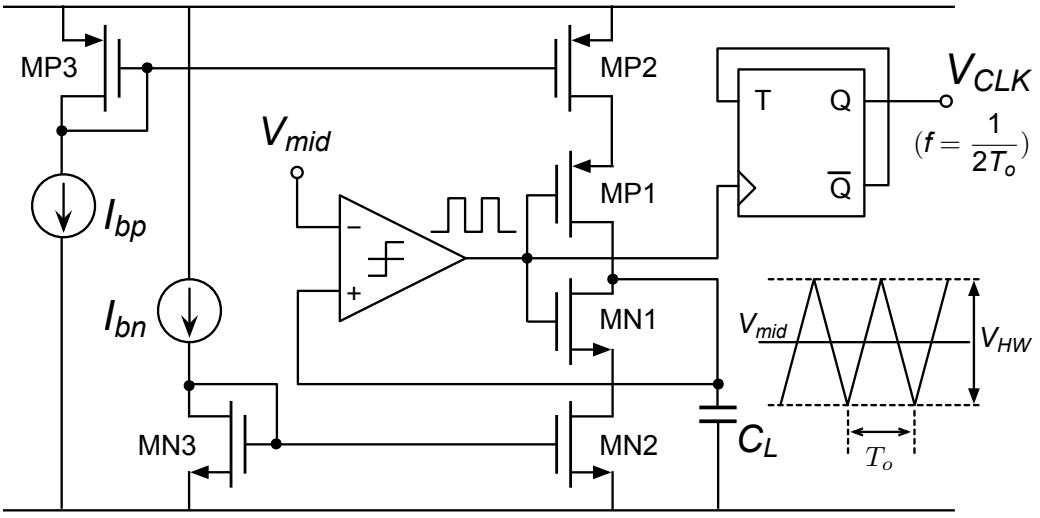


Figure 3.13: Implementation of the relaxation oscillator for on-chip system clock generation.

3.5 Apnea Detection Chip Measurement

The apnea detection IC chip was designed and fabricated in 0.5-μm standard CMOS technology and packaged in a DIP 40 casing. The designed chip occupies an active area of 0.163 mm^2. Fig. 3.14 shows the die micrograph of the fabricated chip.

With a test supply of 5 volt, the signal processing IC consumes 33 μW of power. Multiple internal nodes were probed for validation of functionality. Fig. 3.15(a) shows the outputs of the front-end amplifier and the hysteresis comparator, which demonstrate the modulation of the breathing waveform into a pseudo-PPM signal. Both time instances and time durations of inhale/exhale activities are correctly represented as pulse positions and pulse widths, respectively. Fig. 3.15(b) shows the TDC's digital output (LSB only) aligned with the received breathing waveform. The TDC's resetting action at the beginning

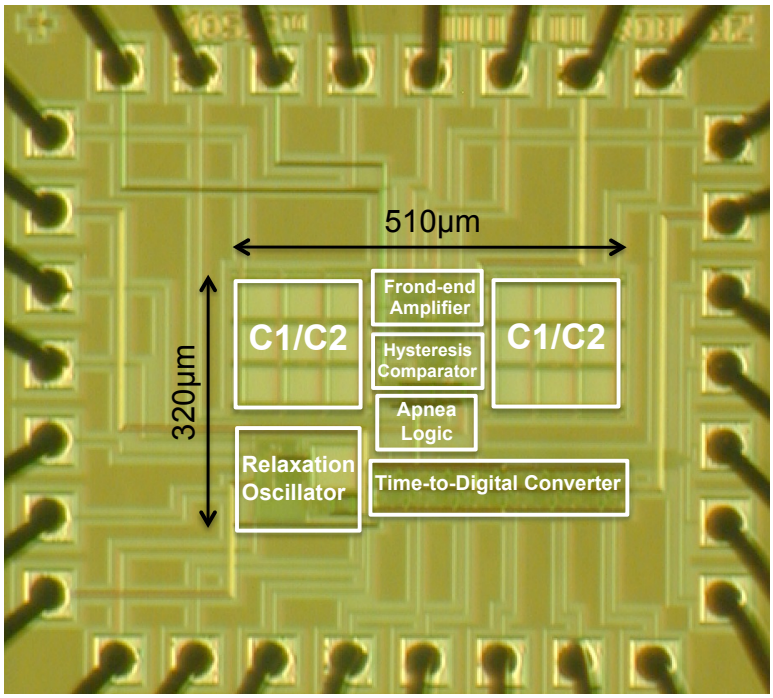
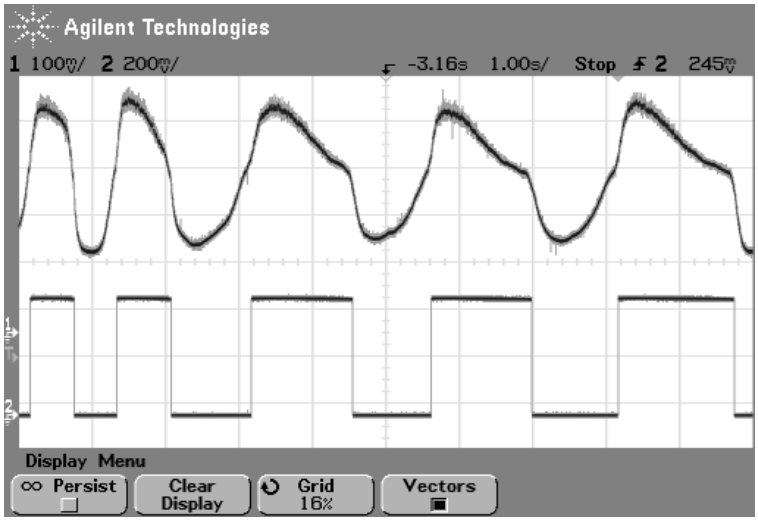


Figure 3.14: Chip micrograph.

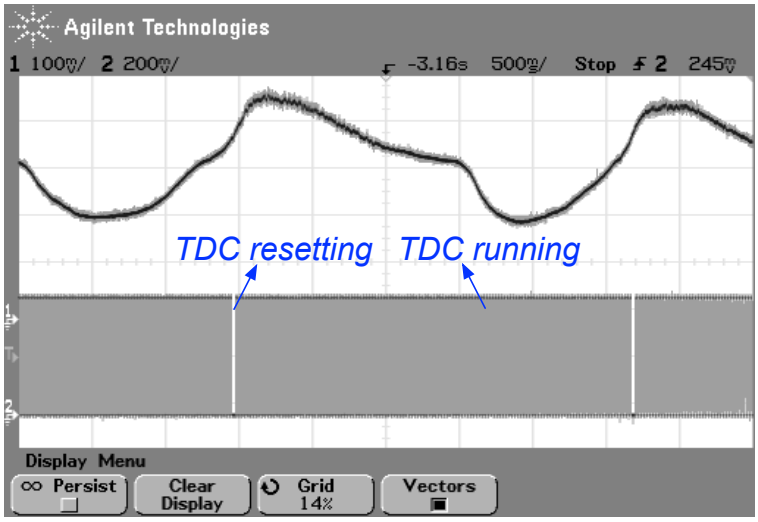
of each breathing cycle is indicated by a short period of "0" state, while the counting action is indicated by the switching "0" and "1" states until the next breathing cycle arrives.

3.6 Conclusions

This chapter proposed a hardware-based sleep apnea detection and scoring algorithm based on signals recorded by a MEMS pressure sensor. The design goal is to achieve a compact device suitable for low-cost in-home apnea testing, which provides a more viable diagnosis method for people with potential sleep apnea conditions. The use of a MEMS pressure sensor allows inhale and exhale events to be detected with much reduced interference and artifacts, which leads to a much simplified apnea detection algorithm. An adjustable detection threshold enables auto-scoring with minimal hardware complexity.



(a)



(b)

Figure 3.15: Measured signals on the tested chip: (a) outputs of the FEA and the hysteresis comparator; (b) outputs of the FEA and the TDC (only LSB is displayed).

The proposed algorithm is implemented using integrated circuits design and fabricated in standard 0.5 μm CMOS technology. A monolithic apnea detection SoC solution with integrated MEMS sensor and apnea detection circuits can potentially further reduce device size and cost, which makes this approach even more appealing to breathing-related medical applications with the benefits of improving patient's everyday life quality.

4. PROTOTYPE DEVICE DESIGN AND ASSEMBLY

A prototype apnea monitoring device was designed and assembled based on the apnea detection algorithm and breathing signal processing chip described in Chapter 3. The device also includes a *Freescale* MEMS pressure sensor for breathing signal detection, a *Cypress PSoC 5* platform for programmable testing, and an *Artaflex* wireless transceiver module for data transmission, all mounted on a custom-designed PCB and packaged in a casing produced by 3-D printing technology. The entire device is powered by a single USB battery pack with a 5-volt output voltage. The following sections will describe in details on the prototype device design and assembly.

4.1 Prototype Device

4.1.1 MEMS Pressure Sensor

The *MPXV4006* series MEMS pressure sensors from *Freescale* are selected for detecting breathing airflow signal. The sensor is a piezoresistive pressure transducer combining advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure [72]. Fig. 4.1 shows the detailed internal structure of the sensor chip. On top of the sensor package for model *MPVZ4006GW6U*, an axial port is used to accommodate industrial/medical grade tubing. To channel the patient's inhale/exhale air pressure to the sensor, a nasal cannula (from *Salter Labs*) is used in connection with the sensor's axial

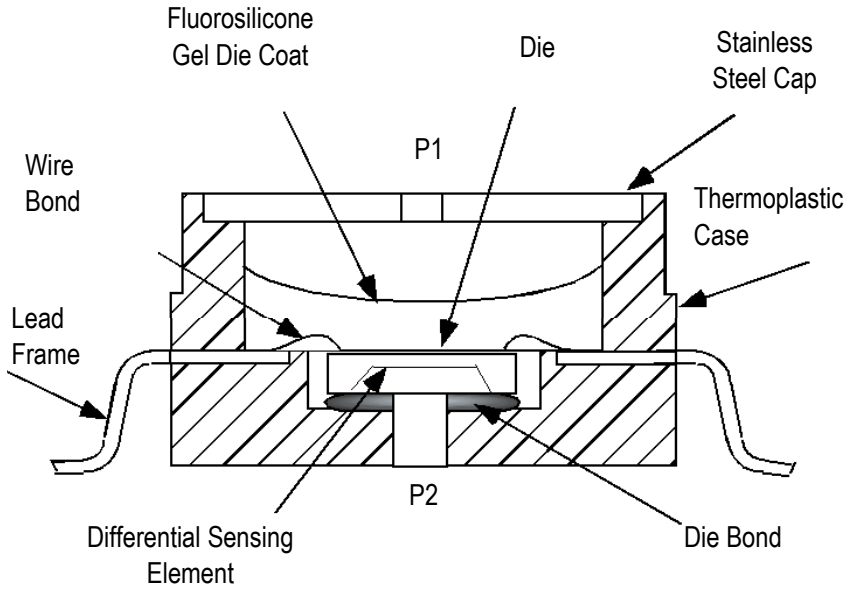


Figure 4.1: Cross-section diagram of the MEMS sensor's small outline package (not to scale). Image courtesy of Freescale.

port. The full-range response of the sensor is illustrated in Fig. 4.2.

4.1.2 PSoC Platform and Wireless Transceiver Module

The *Cypress Programmable System-on-Chip* (PSoC) platform is a family of integrated circuits made by *Cypress Semiconductor*. These PSoC platform features a CPU along with programmable analog peripherals (OpAmps and Comparators), programmable digital blocks, and programmable routing and flexible IO circuits. Incorporating the PSoC into the prototype device allows the digital sleep data from the custom designed signal processing IC to be stored on a remote host. The sleep data was relayed via the PSoC to a wireless transmitter which sends signals to a USB receiver connected to a PC. Fig. 4.3 shows the commercial *Cypress PSoC 5* board with a *Artaflex* wireless transceiver (model

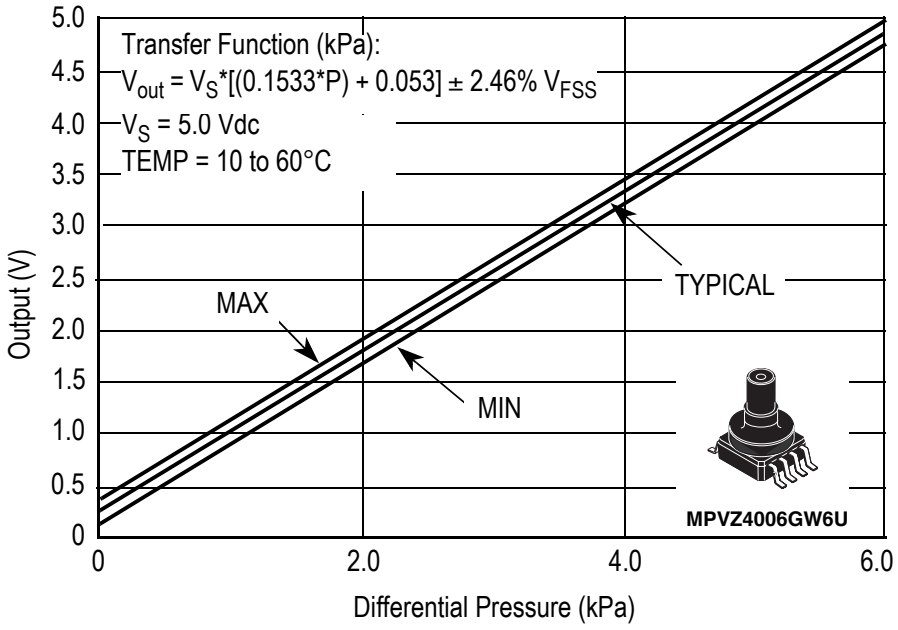


Figure 4.2: MEMS sensor output voltage versus input Differential Pressure. Figure courtesy of Freescale.

AW24MCHL-H2) mounted on its wireless socket. The on-board USB connector is used for PSoC programming interface as well as power supply port.

4.1.3 Prototype Device PCB Design

The prototype device incorporates the MEMS sensor, the apnea detection IC in a DIP (dual inline package) 40 package, and the *Cypress* PSoC platform with the *Artaflex* wireless transceiver. Fig. 4.4 shows the printed circuit board (PCB) design which accommodates the aforementioned components. The PSoC platform is designed to sit on top of the apnea IC such that the overall device size can be minimized. The PCB measures 1.875 inches wide and 3.875 inches deep. The designed PCB is manufactured using standard

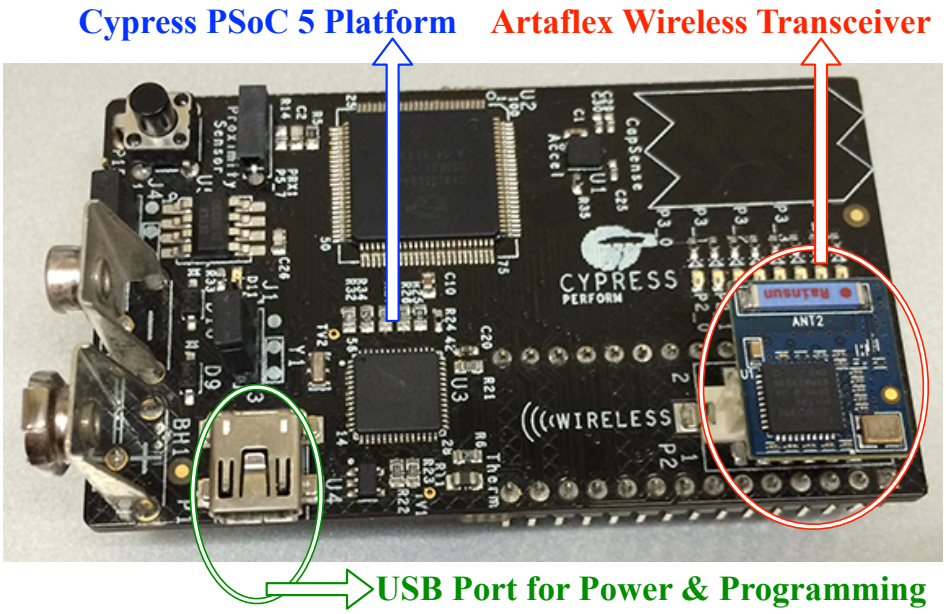


Figure 4.3: Cypress PSoC 5 platform with Artaflex wireless transceiver module mounted on top.

2-layer PCB technology.

4.1.4 Prototype Device Assembly

The assembled prototype device is shown in Fig. 4.5. The custom designed PCB (in green color) accommodates the PSoC board (black PCB), the MEMS breath sensor, and the apnea detection chip (underneath the PSoC board). The entire device is housed in a plastic casing produced by 3-D printing technology. The prototype assembly measures 10 cm deep, 5 cm wide, and 3.5 mm high. An external USB battery pack is used to power the entire device through the USB port of the PSoC platform. The device wirelessly transmits its data to a PC connected to An *Artaflex* USB receiver (*AWAC24U*).

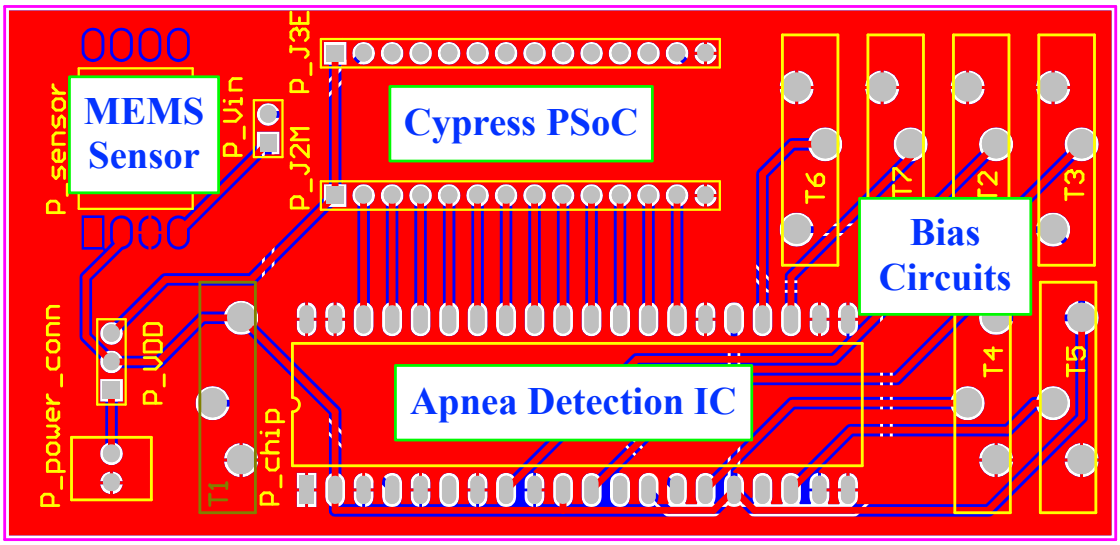


Figure 4.4: Prototype device PCB design.

4.2 Conclusion

This chapter demonstrated the design and assembly of a prototype sleep apnea monitoring device. The prototype device uses a MEMS pressure sensor to capture the patient's breathing activity with much reduced interference and artifacts which leads to a much simplified and robust apnea detection algorithm. Wireless connectivity allows the scored sleep data to be transmitted to mobile phones or remote stations immediately after each study session, which is a significant improvement comparing to existing devices that require the patient the return the device to the clinic for apnea scoring by manual inspection or software-based methods.

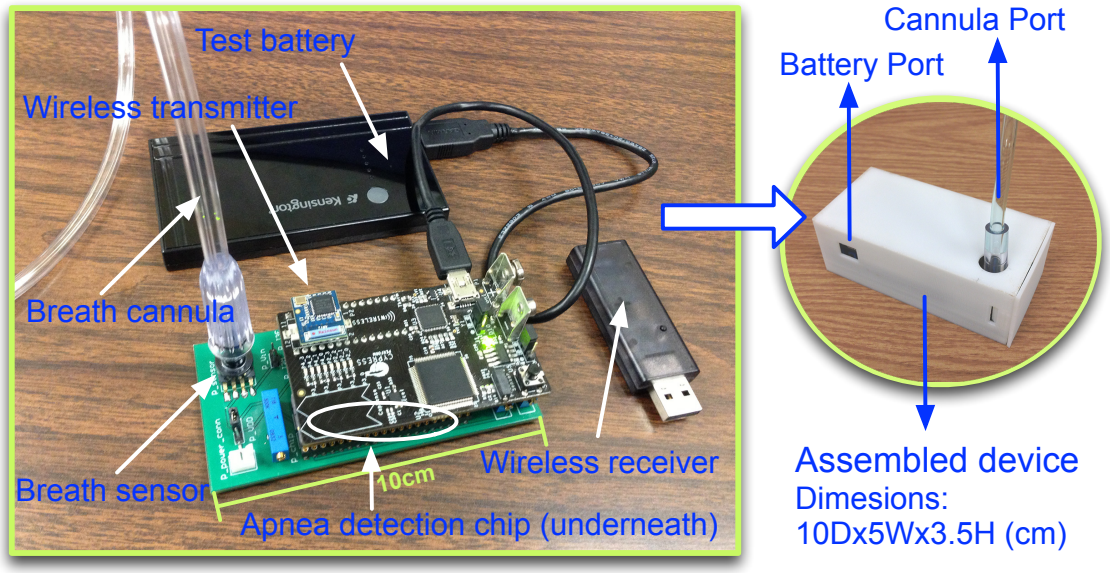


Figure 4.5: Proposed prototype device for apnea screening tests.

5. ULTRA-LOW POWER ANALOG-TO-DIGITAL CONVERTER*

5.1 ADC in Biomedical Applications

Practically all biomedical signals to be detected and recorded from a human subject are in analog forms. However, digital domain signal processing provides a powerful and sophisticated tool for biomedical information analysis, especially with the recent advances in semiconductor technology to reduce both power and cost of digital circuitry. Therefore, an Analog-to-Digital Converter becomes essential in a medical device in order to take advantage of both digital and analog worlds. This chapter presents design details for an ultra-low power ADC suitable for biomedical applications.

Figure 5.1: General view of a medical electronic system.

A modern medical electronic system consists of a sensor, a low-noise signal-conditioning front-end, an analog-to-digital converter (ADC), and a digital backend for signal processing. Fig. 5.1 shows a brief diagram of such a system. The sensor element captures the physiological signal from the patient and generates its representation as an analog electrical signal. This analog signal is conditioned and amplified by the low-noise front-end

*Part of this section is reprinted with permission from "An Energy-Efficient Time-Domain Asynchronous 2 b/Step SAR ADC With a Hybrid R-2R/C-3C DAC Structure" by Jiayi Jin, 2013, IEEE Journal of Solid-State Circuits, Volume: 49, Issue: 6, Page(s): 1383 - 1396 [73], Copyright 2013 by IEEE

circuits, followed by the ADC and digital backend that digitizes it and processes it in digital domain respectively. The addition of the digital backend is very beneficial, since today's VLSI technology has made digital signal processing more powerful in computing capability and yet more economic in power and area cost. Hence the ADC, which links analog physiological signals to the digital world, becomes essential for these devices to take such advantages.

Advances in deep sub-micron CMOS processes [74] have enabled various biomedical ICs with lower power, smaller footprints, and smarter signal processing [69, 75, 76]. Medical devices can now be easily built in portable and wearable format, capable of point-of-care applications such as measuring blood pressure level, blood glucose level, and blood oxygen level (oximetry), as well as recording electrocardiography (ECG) and electroencephalography (EEG). Implantable medical applications have also emerged to treat and monitor multiple diseases including epilepsy [77, 78], abnormal heart rhythms (pacemakers) [79, 80], and diabetes [81].

For most portable and battery-operated applications, high energy-efficiency is normally required due to very limited energy sources to power such devices. The limited footprints also limit the size of batteries to be use, and hence their power capacity as. For medical-implant devices, in particular, it is crucial to build ultra-low power devices to extended battery lives, or even make them self-sustainable on ambient power sources [82], which helps avoid frequent battery replacement and its associated invasive surgeries on patients. The ultimate goal for energy efficient devices is to improve the medical device's

level of convenience and reduce medical expenses to patients.

5.2 Existing Ultra-Low Power ADC Solutions

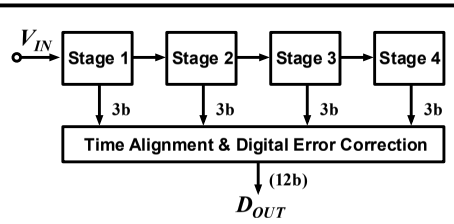
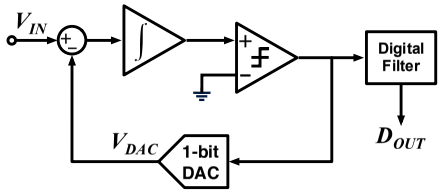
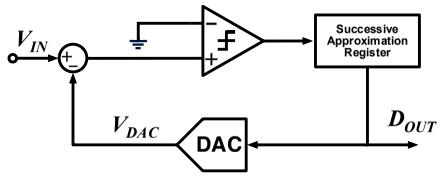
5.2.1 ADC Architectures

There exists many architectures for ADC implementations, of which the pipeline ADC, the Sigma-Delta ADC, and the Successive Approximation Register (SAR) ADC are the most widely used structures. Based on cascaded stages of sub-ADCs (usually flash ADCs), the pipeline ADC features simultaneous operation of individual stages to achieve high conversion speed and accuracy that covers a wide range of applications. Thus, pipeline ADC has become a very popular choice for scenarios such as CCD imaging, ultrasonic imaging, cable modems, etc. However, it is relatively power and area costly due to operations of multiple sub-ADC stages.

The Sigma-Delta ADC is an oversampling A/D converter topology based on the Sigma-Delta Modulation principle. The topology is capable of extremely high resolution (16-24 bits), especially in single-bit structures where its internal 1-bit DAC is inherently linear without any calibration or laser-trimming. Being digitally intensive, the ADC receives great benefits with technology scaling. Due to its over-sampling nature, the Sigma-Delta ADC is often limited to medium-to-low speed applications. Sigma-Delta ADCs have been the popular choice for video, audio, and precision industrial measurement applications.

The SAR ADC operates in a step-by-step fashion based on the binary search algorithm called the Successive Approximation method. The topology features minimal circuit blocks, which are reused in each conversion step. Due to the multi-step conversion

Table 5.1: Comparisons among the Pipeline, Sigma-Delta, and SAR ADC architectures.

	Pipeline ADC	**Sigma-Delta ADC**	**SAR ADC**
Topology			
Speed	medium-to-high speed	low speed	low-to-medium speed
Resolution	medium-to-high resolution (8-16 bits)	high resolution (16-24 bits)	medium resolution (8-12 bits)
Power	high power consumption	medium power consumption	low power consumption
Application	CCD imaging Ultrasonic imaging Cable modem	Video Audio Precision measurement	Portable electronics Medical devices Pen digitizers

mechanism, the SAR ADC requires a high-speed internal synchronization clock, limiting the overall conversion speed. The structural simplicity allows the ADC to operate with extremely high energy efficiency, earning its popularity in applications such as battery-operated medical devices, pen digitizers, and so on. Table 5.1 demonstrates the comparison of the three ADC architectures in terms of power, area, speed, resolution, and their respective applications. For the majority of biomedical applications, input signal frequencies are normally under 50 kHz and ADC resolutions fall into the medium-to-high category. Therefore, the SAR ADC architecture satisfies all requirements for digitizing biomedical signals and at the same time achieves the lowest power consumption.

5.2.2 Ultra-Low Power SAR ADCs

The SAR ADC has proved [83, 84] to be an excellent low-energy architecture for medium-speed applications. Illustrated in Fig. 5.2 are the block level implementation of a conventional N-bit SAR ADC (a) and the timing diagram of its step-by-step conversion procedure (b). The input signal is sampled at a rate of F_S, while the conversion steps are synchronized using the clock $F_c = (N+1)F_S$ controlling the comparator. The Successive Approximation (SA) register generates a N-bit word during each conversion step based on the comparison results. The N-bit Digital-to-Analog Converter (DAC) provides an analog reference level according to the SA register's digital output. As demonstrated in Fig. 5.2(b), during the first F_c clock cycle, the input signal is tracked, sample and held – normally on a Sample and Hold capacitor. Immediately after the track-and-hold period, the comparator starts to compare the input signal level and the DAC reference level, which

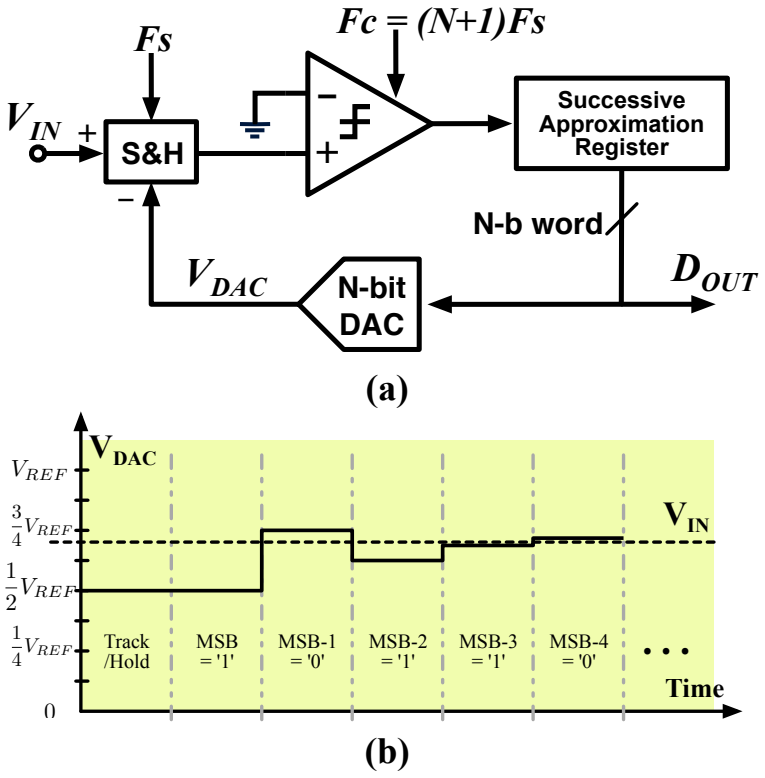


Figure 5.2: A conventional N-bit SAR ADC: (a) block level implementation and (b) timing diagram of conversion procedure.

is initially set to be half of V_{REF}. Here, V_{REF} is the full input range of the ADC. During the upcoming steps, the DAC adjusts its output level according to all previous comparison results in order to gradually approximate the input signal level.

Although the simple SAR ADC is already very low-power compared to other ADC implementations, there are still ongoing efforts to further optimize the energy efficiency of the SAR architecture. Literature in this specific area has reported various energy reduction strategies aiming at different aspects of the SAR ADC structure, including circuit blocks, system level, conversion algorithm, etc. A representative collection of such works can be

summarized as follows:

1. Reduced Supply Voltage

   Being digitally intensive, the SAR ADC would receive significant power reductions under reduced voltage. However, analog components such as the comparator and DAC suffer in terms of signal-to-noise ratio and speed as a result. Shikata et. al [84] proposed to use a tri-level comparator to relax the speed requirement of the comparator and decrease the resolution requirement of the DAC under extremely low supply voltages. Agnes et. al and others [85, 86] explored to perform time delay comparisons instead of voltage level comparisons in the Successive Approximation scheme. Time-domain comparators can take advantage of the fine time resolution of advanced CMOS technologies and avert the penalty of stringent voltage comparator performance requirement (including noise, resolution, and input-referred offset) under extremely low supply voltages.

2. Reduced DAC Size

   The capacitive binary-weighted DAC is often the common DAC choice in the SAR architecture, and normally commands the highest energy consumption compared to all other circuit blocks within a SAR ADC. In medium-to-high resolution applications, the size of the capacitive DAC and hence its power is often dictated by the ADC resolution and matching performance of the unit capacitors, which is usually much larger than what is required by the kT/C noise level. For a 10b case, the unit capacitors are normally in the range of 5-50 fF range depending on the process

characteristics.

Harpe et. al [83] implemented a segmented DAC in which the 4 MSBs are encoded in a thermometer fashion while the remaining 8 LSBs are encoded in a binary fashion. The thermometer encoding scheme effectively mitigates the probability of large DNL errors since the number of unit elements to be switch in each step is much reduced compared to the binary encoding scheme. As a result, the size of the unit capacitor is reduced to 250 aF, greatly reducing the DAC's power consumption.

Xu et. al [87] proposed a novel digital calibration method based on dithering techniques. With dithering, the weights of MSB capacitors can be measured very accurately so that the matching requirement for unit capacitors are much reduced and that very small capacitors can be used. As a result, a 20-fF unit metal-insulator-metal (MIM) capacitor (a total of 2.54 pF) with only 1% matching accuracy can be utilized to implement a 10-bit DAC. Physical manual trimming of unit capacitors is also an effective approach to reduce capacitor matching requirement and achieve lower power, albeit more costly to perform.

3. Improved Switch Schemes

   The binary searching scheme of the successive approximation algorithm can be implemented in multiple ways, which are mainly reflected on the switching scheme, and to that end the energy consumption of the SAR ADC's DAC operations. Mathematically, the DAC energy can be expressed as $E_{DAC} = \alpha_k C V_{REF}^2$, where α_k is a constant depending on a specific switching scheme, C is the unit capacitance,

and V_{REF} is the input reference voltage to the DAC. In a conventional switching scheme, where the DAC always outputs the middle voltage within the identified sub-voltage ranges in each step, the average switching energy is $1365.3CV_{REF}^2$. In a split-capacitor scheme where the DAC is segmented, the average switching energy is reduced to $847.1CV_{REF}^2$. In a monotonic switching method where the DAC output level approaches the input level in a uni-directional way, the DAC only consumes $255.5CV_{REF}^2$ of energy. In merged-capacitor and charge-average switching schemes, the DAC's energy consumptions are further reduced to $170CV_{REF}^2$ and $88.6CV_{REF}^2$, respectively. Table 5.2 summarizes the DAC energy consumptions under various switching schemes.

Table 5.2: Energy consumption of different DAC switching schemes

Switching Scheme	Conventional Switching	Split-Cap Switching	Monotonic Switching	Merged-Cap Switching	Charge-Average Switching
Refence	[88]	[89]	[90]	[91]	[92]
Energy(CV_{REF}^2)	1365.3	847.1	255.5	170	88.6

4. Reduced Idle and Leakage Power

   In low-speed scenarios, the ADC's idle and leakage power can be a significant compared to its total power consumption. Zhang et. al [93] made efforts to enforce maximum circuit simplicity using the SAR structure and reduced the leakage power. Sekimoto et. al [94] utilizes full asynchronous operation and boosted self-power gating to mitigate leakage power dissipation during ADC's non-active state after

all conversation steps are finished. As will be discussed later in this chapter, the asynchronous technique can be very effective in reducing idle power when the ADC consumes static current during conversion.

5. Other Applications Specific Techniques

   The power consumption of a SAR ADC can also be further optimized when the nature of the signal to be digitized is known. Signal-specific energy reduction strategies can be extremely useful when designing an ADC for biomedical applications. Huang et. al [95] proposed a bypass window mechanism in which the ADC skips several conversion steps when the signal amplitude is within a predefined small window, thus effectively saving power when the input medical signal amplitude is very small. For applications such as ECG recording where the input medical signals has a small and low-variation amplitude, the ADC's energy efficiency can be greatly improved when the bypass window is properly set.

   In high resolution scenarios, the comparator usually demands very high energy consumption in exchange for better SNR. Harpe et. al [83] devise a data-driven method to relax the SNR requirement of the comparator. The method monitors the comparison time to find the most critical comparison with an input amplitude less than 0.5 LSB and triggers 4 additional repeated comparisons. The final comparison result is taken using majority voting scheme to mitigate the random noise effect.

   Yaul et. al [96] also presented a signal-activity-based power-saving algorithm called LSB-first successive approximation. The algorithm starts with an initial guess of the

current input value and bit-cycles the LSBs first instead of the conventional MSB-first method. The ADC maintains a constant sample rate and resolution, scales logarithmically with signal activity, and does not inherently suffer from slope overload. The energy efficiency of the ADC can improve as much as 6 times depending on the range of the input signal amplitude.

For lower-sampling-rate portable medical applications, energy efficiency is often a critical matter [97, 92, 98]. However, it is not obvious how best to utilize smaller-feature-size technologies inherently faster devices so as to maximize energy efficiency. In a SAR ADC, the dynamic power from the capacitive DAC (CDAC) or digital circuits can be expressed [99] as $P_{dyn} = ACV^2f$, where V is the supply or reference voltage, f is the switching frequency, C is switched capacitance, and A is the activity factor for digital circuits or code-dependent coefficient for the CDAC. Although the CDAC's dynamic power does scale with speed, the dynamic *energy* spent for converting each bit stays the same. Reducing CDACs energy can be achieved by minimizing the capacitor size, but this method is eventually limited by the linearity and matching requirement. Hence, for a given resolution, the CDAC's energy efficiency is usually unchanged albeit at reduced speeds.

In comparison, the static energy dissipation of a resistive DAC (RDAC) is determined by its resistance value or available timing to settle, thereby has a greater potential to achieve better efficiency at lower conversion rates. When excess time budget is present due to longer clock periods, the RDAC can reduce its power by using larger unit resistances. Additionally, the asynchronous SAR scheme [100] helps the resistive DAC to

dynamically adjust its energy dissipation to the actual time needed for converting each bit, which also allows the RDAC to take advantage of faster circuits in advanced technologies for enhance efficiency.

The 2b/step conversion technique reduces both conversion time and the switching activity factor (A) of an asynchronous SAR ADC, thereby can be very beneficial in saving static and dynamic energy. However, such techniques are normally used in high-speed applications [101, 102], and involves either multiple capacitor-based DACs [103] or a resistive string DAC with complex switch networks [104] to obtain additional reference levels for 2b conversion. Therefore, to achieve highly efficiency operations, the 2b/step scheme needs to be optimized and refined to avoid excessive circuit and energy overhead.

The timing diagram in Fig. 5.2(b) manifests a synchronous conversion plan where each conversion steps are allocated with equal time period. In a synchronous 10-bit ADC with sampling rate of 100 kS/s, for instance, the ADC would need a F_c of 1.1 MHz equally divided into 11 time slots, each with a period of 1 μs. The first of the 11 time periods is used for signal sampling, and the remaining 10 periods are used for conversion of 10 digital bits, one bit per conversion step. Alternatively, the SA conversion procedure can adopt the asynchronous mechanism. Fig. 5.3 demonstrates the difference between the synchronous conversion and the asynchronous conversion. The main benefits of the asynchronous scheme include (1) the internal synchronization clock is no longer needed, and (2) idle times between conversion steps are eliminated. More detailed reasoning for choosing the asynchronous scheme will be discussed later in this chapter.

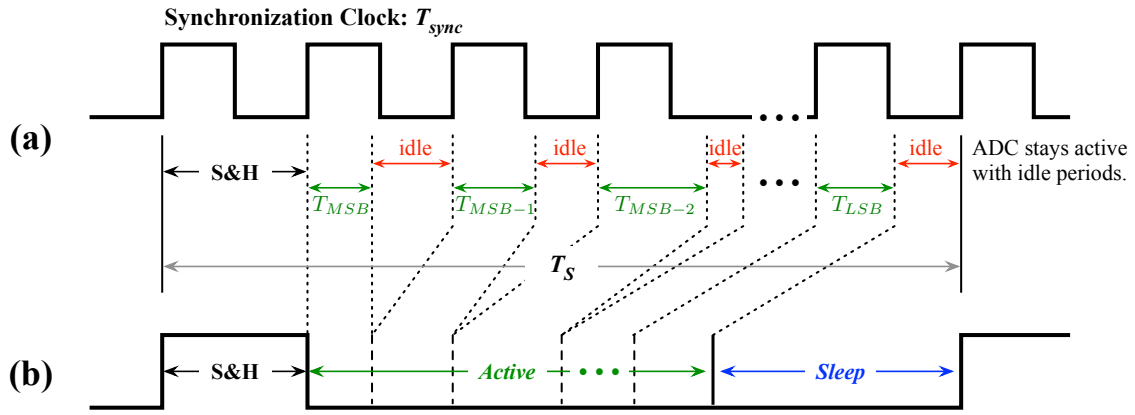


Figure 5.3: ADC conversion: (a) conventional scheme with synchronization clock T_{sync}, and (b) asynchronous scheme with sleep mode and minimal idle periods.

Fig. 5.4 shows the conceptual block diagram of a SAR ADC that incorporates the asynchronous and 2b/step conversion schemes. The innovative low-energy strategies will be demonstrated in this chapter based on a 10-bit asynchronous 2b/step SAR ADC using a resistive-based DAC. The asynchronous technique eliminates idle times between conversion steps, effectively reducing the ADC's active time and allowing sleep mode to be engaged at the end of each clock period. The 2b/step conversion scheme is executed using a R-2R/C-3C hybrid DAC with minimal energy overhead and saves 50% in both conversion time and switching activities. As a result, both static and dynamic energy are substantially reduced. The time-domain 2b comparison scheme involves absolute value comparison and sign interpolation, requiring only one additional comparator as opposed to two in conventional 2b schemes. This technique helps maintain the same comparator energy efficiency as in the 1b schemes due to halved switching events on each comparator circuit under 2b/step conversion. Furthermore, our time-domain comparator (TDC) com-

pares on both rising and falling clock edges and, thus, effectively reuses energy that would otherwise be wasted during TDC reset phases.

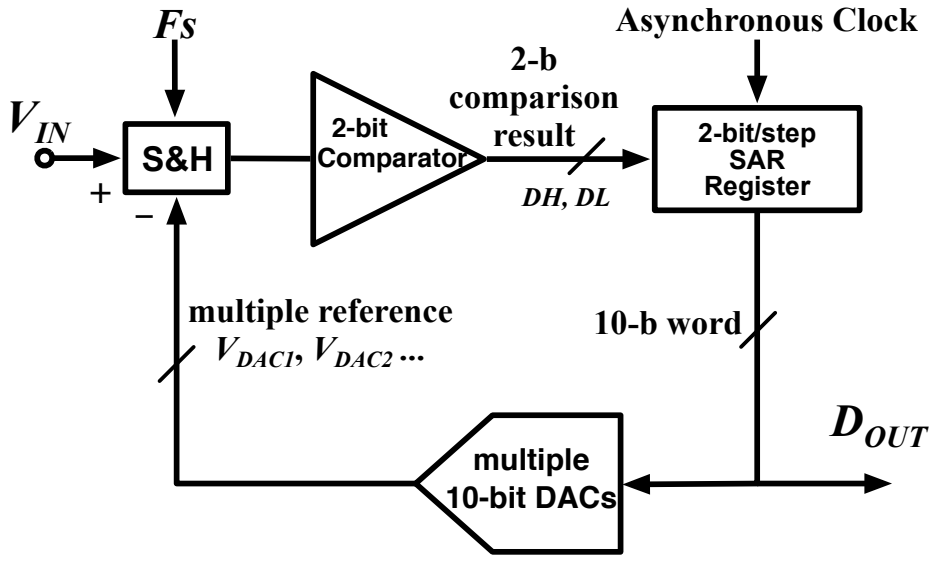


Figure 5.4: Conceptual block diagram of a 10-bit asynchronous 2b/step SAR ADC.

The rest of this chapter will provide in details the description of the proposed ADC architecture and its energy-reduction strategies, illustrations of the principles of the proposed 2b/step conversion scheme with reduced circuit complexity, discussions on circuit level implementations and design considerations, and measurement results of the fabricated prototype IC chip for design validation.

5.3 Proposed ADC Architecture and Low Energy Strategy

5.3.1 Proposed Architecture

Fig. 5.5 shows the proposed SAR ADC architecture. The ADC adopts the Asynchronous conversion scheme, where each conversion step is triggered immediately after

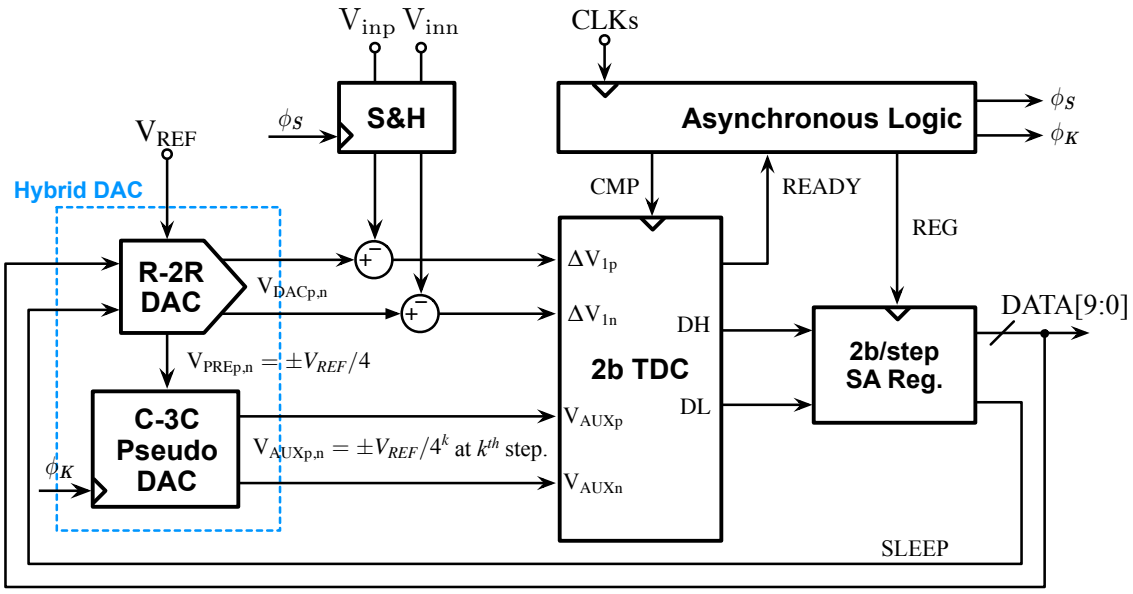


Figure 5.5: Architecture of the proposed asynchronous 2b/step SAR ADC.

the completion of the previous step without the need of an internal high-speed synchronization clock (F_c in Fig. 5.2). The ADC also converts two bits in each step, and adopts the combination of a resistive R-2R main DAC and a switched-capacitor C-3C pseudo DAC as a hybrid DAC to provide reference levels ($V_{DACp,n}$ and $V_{AUXp,n}$) for the 2b/step conversion scheme. The 2b comparison results (*DH* and *DL*) between the input signal ($V_{inp,n}$) and the reference levels are resolved in time domain using a 2b dual-edge time-domain comparator (TDC) instead of conventional voltage comparators. As we will show, the proposed hybrid R-2R/C-3C DAC and the TDC effectively reduce circuit complexity for 2b/step operation and, therefore, reduce design effort and overall power consumption. Meanwhile, the 2b/step technique halves overall conversion time and switching activities, which reduces the static and dynamic energy, respectively.

The conversion plan of the ADC is shown in Fig. 5.6. After input signal sampling and initial DAC settling, the falling edge of *CLKs* triggers the first rising edge of comparison clock *CMP* for the TDC. Beyond this point, the ADC operates in asynchronous mode: the *READY* signal indicates the completion of the TDC comparisons by its rising and falling edges, while the *REG* signal controls the 2b shift register to store the comparison results (*DH* and *DL*); a delayed version of *READY* allows the hybrid DAC to settle to proper reference voltages and triggers the next *CMP* edge; the *SLEEP* signal, generated by the last flip-flop of the shift register, shuts down the ADC after all 10 bits are resolved.

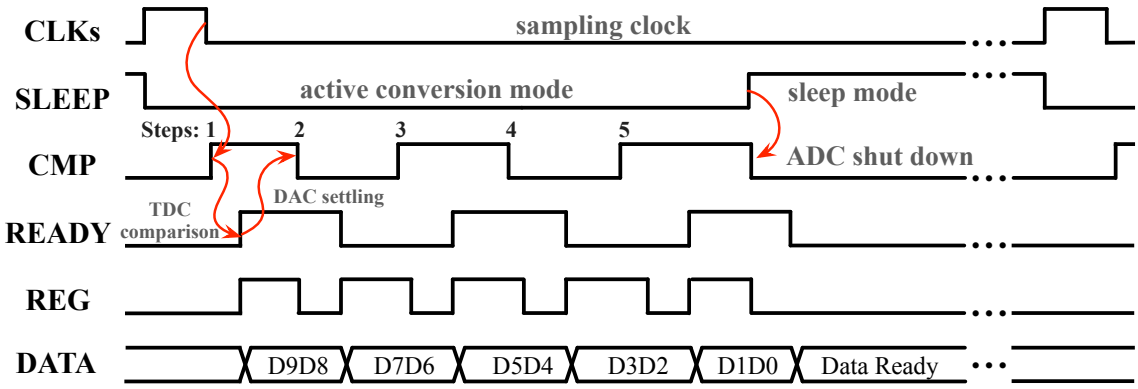


Figure 5.6: ADC conversion plan with asynchronous timing diagram.

The goal of this design is to achieve optimal power with targeted performance and speed, i.e., the lowest energy spent per-bit-operation during each sampling clock period (T_S), with an output of desired resolution. For the proposed asynchronous SAR ADC, the total energy consumption *during one* T_S can be qualitatively expressed as

$$E_{ADC} \approx \frac{1}{2} \cdot N \cdot V_{DD}^2 \cdot C_{eq} + \frac{V_{DD}^2}{R_{eq}} \cdot T_{active} + V_{DD} \cdot I_{leak} \cdot T_S \tag{5.1}$$

where N is the resolution, C_{eq} is the equivalent total capacitance (from digital circuits, S&H, C-3C, etc) charged to V_{DD} in one 2b conversion step, R_{eq} is the R-2R DAC's code-dependent resistance from $V_{REF}(= V_{DD})$ to ground during the active conversion time T_{active}, and I_{leak} is the total leakage current. Eq. (5.1) provides insights into strategies for overall energy reduction. The first term of the equation represents dynamic energy consumption originating from circuit switching, which can be reduced by minimizing total number of circuit switching activities. The 2b/step technique and dual-edge TDC reflect such strategy. The second term manifests static energy dissipation due to the DAC's quiescent current, which can be reduced by tightening the active time window of the ADC. Low supply voltage is another effective way to reduce overall energy consumption. While it is not our focus to tackle leakage, this asynchronous design offers the potential to reduce leakage power when proper circuit techniques [105] are applied during sleep mode.

5.3.2 Dynamic Energy Reduction

In common SAR ADCs, the capacitive DAC is often a major source of dynamic energy consumption. In practice, the size of the DAC capacitors is usually dictated by linearity/matching requirements rather than kT/C noise for low-to-moderate resolutions ($N \leq 10$). Therefore, its power optimization is eventually limited by the matching performance as well. Although calibration techniques have been developed [87, 106] to allow smaller DAC capacitors and thus lower power, they lead to increased design cost and circuit complexity. This work uses a R-2R resistive ladder DAC; thus, a significant amount of dynamic energy is transformed into the static type, and is now limited by the available

time budget for DAC settling under the asynchronous scheme. The R-2R DAC offers an additional degree of freedom in sizing its unit resistance (via L/W ratio) to achieve optimal power and still keeps the same area (WL) for matching accuracy. Moreover, with increased resolution, the decoupling of DAC power from matching performance allows the RDAC to keep its power constant, whereas the CDAC's power will increase exponentially.

The 2b/step technique cuts the converter's switching activities from the DAC drivers and digital circuits by half, giving the factor of '1/2' for the dynamic energy term in Eq. (5.1). As will be shown later, the proposed 2b reference scheme saves 66% in DAC hardware compared to the regular 2b conversion method. The custom-designed 2b TDC adopts a unique interpolation mechanism and requires only 2X comparator hardware instead of 3X for normal 2b comparison schemes. As a result, energy and circuitry overhead for implementing the 2b/step technique is rather minimal. Table 5.3.2 summarizes the switching energy savings compare to conventional 1b/step and 2b/step schemes.

Reducing VDD leads to a quadratic decrease in dynamic energy, and it favors digital circuits as long as timing requirements are met. For thermal-noise-limited analog circuits, energy dissipation will actually increase [107, 108], especially with the addition of preamplifiers to combat the reduced LSB voltage. In comparison, the TDC is much more amenable to low supplies since it functions similarly to a digital gate and, thus, needs only slightly more than a MOS threshold voltage to operate. For low-speed applications, an abundant timing budget is available for improving the TDC's performance [86]. Thanks to the proposed dual-edge-comparison design (details described in later sections), the to-

Table 5.3: Hardware and energy savings by the proposed 2b/step conversion scheme

	1b/step (conventional)	2b/step (conventional)	2b/step (proposed)
Comparator: (14% of total ADC power in this design.)			
# switching events	10	5	5
# comparators	1	3	2
Total Energy[1]	10	15	10
SAR Logic: (36% of total ADC power in this design.)			
# digital gates	X	—	X
# switching events	10	—	5
Total Energy[1]	10X	—	5X
DACs: (27% of total ADC power in this design.)			
# DACs	1	3	1
# switching events	10	5	5
Total Energy[1]	10	15	5
1: in units of energy per switching event per hardware.			

tal switching activities of the TDC is also reduced by half. In a conventional TDC, the *energy-per-comparison* can be expressed as

$$\begin{aligned} E_{TDC} &= E_{compare} + E_{reset} \\ &= (+V_{DD})^2 C_L + (-V_{DD})^2 C_L \\ &= 2V_{DD}^2 C_L \end{aligned} \tag{5.2}$$

where C_L represents the sum of gate capacitances for each delay stage within the TDC, and we have neglected crowbar current. The factor '2' comes from the fact that each gate capacitor is switched twice between V_{DD} and ground during one compare/reset cycle.

By utilizing the reset actions towards a new comparison, the proposed dual-edge scheme effectively cuts this dynamic energy consumption by half since no energy is wasted during the otherwise necessary reset phase as in [86, 85].

5.3.3 Static Energy Reduction

Although capacitive DACs have been popular for SAR converters, we use an R-2R DAC in this design for its energy scaling capability at low conversion rates. For an N-bit conversion, the CDAC's total energy consumption can be expressed as

$$E_{CDAC} = \sum_{i=0}^{N-1} \alpha_i V_{REF}^2 C_u = A_k V_{REF}^2 C_u \tag{5.3}$$

where α_i are code-dependent coefficients, V_{REF} is the reference voltage, C_u is the unit capacitance, and A_k is an energy factor based on the DAC's switching scheme [90, 92, 89, 91, 88]. As the value of C_u is determined by matching requirements at moderate resolutions and is not affected by the conversion rate, the CDAC's energy consumption stays constant when the ADC's speed decreases.

In the case of a resistive DAC, the ADC's active time has a strong impact on its energy efficiency. In Eq. (5.1), the term T_{active} includes DAC settling time t_{DAC}, TDC resolving time t_{TDC}, and digital gate delays t_{dd}, which leads to the RDAC's static energy expression

$$E_{RDAC} = \sum_{i=1}^{N/2} \frac{V_{REF}^2}{\beta_i R_u} \cdot (t_{DAC} + t_{TDC,i} + t_{dd,i}) \tag{5.4}$$

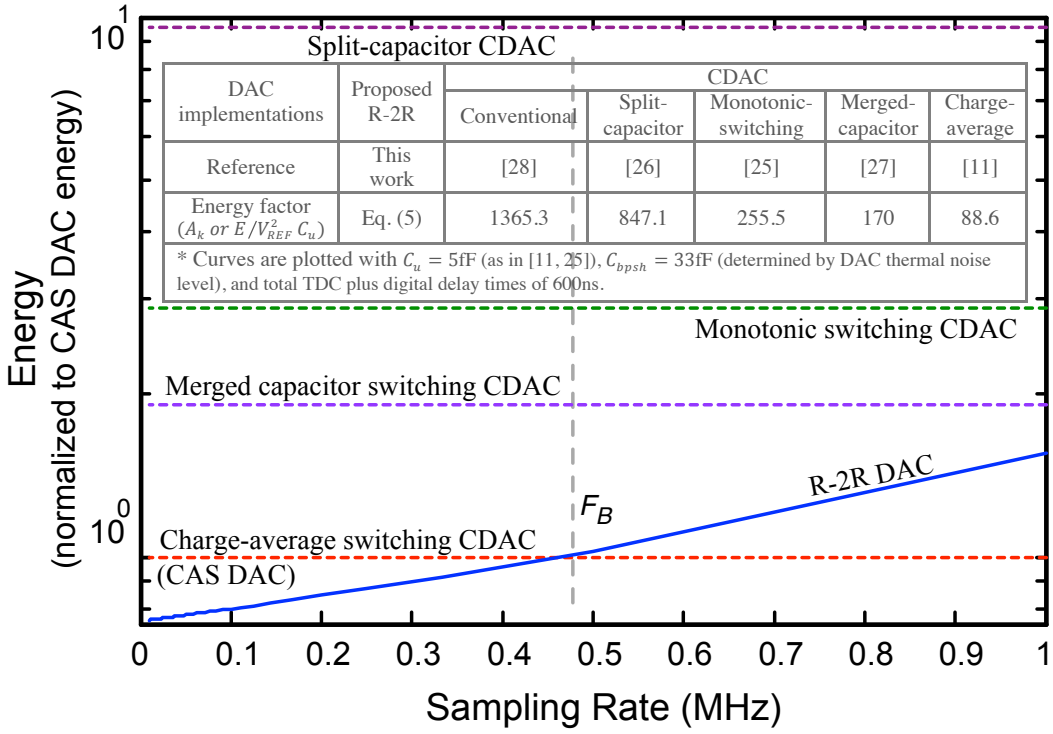
where β_i are code-dependent coefficients, R_u is the unit resistance, and $t_{TDC,i}$ varies due

to different input amplitudes. In an N-bit RC-limited DAC, a settling time of $t_{DAC} = N \cdot \ln(2) \cdot \tau_{DAC}$ is required in order to achieve $\frac{1}{2}V_{LSB}$ accuracy [109]. In this design, the R-2R DAC's time constant is $\tau_{DAC} = R_u C_{bpsh}$ (C_{bpsh} is C_{SH}'s bottom-plate capacitance, refer to Fig. 5.13), and the static energy during DAC settling $E_s = \sum_{i=0}^{N/2} N \ln(2) V_{REF}^2 C_{bpsh}/\beta_i$ is relatively independent of DAC's resistance. Thus, we can rewrite Eq. (5.4) as

$$E_{RDAC} = \sum_{i=1}^{N/2} \frac{N \ln(2) V_{REF}^2 C_{bpsh}}{\beta_i} \cdot (1 + \frac{t_{TDC,i} + t_{dd,i}}{t_{DAC}}) \tag{5.5}$$

For given t_{TDC} and t_{dd}, the RDAC's energy can be optimized by increasing the time constant τ_{DAC} when timing permits. In other words, the RDAC is capable of utilizing excess time budget at low conversion rates to achieve higher energy efficiency. Additionally, faster circuit speeds in advanced processes lead to smaller comparison times and digital delays, thereby reducing the RDAC's energy as well.

Ideally, the RDAC reaches its maximum efficiency when it uses all available time budget for settling: $T_{DAC} = \sum_{i=1}^{N/2} t_{DAC} = T_S - \sum_{i=1}^{N/2}(t_{TDC,i} + t_{dd,i})$. Using this criteria, Fig. 5.7 plots the R-2R DAC's energy (normalized to the charge-average switching DAC case) based on Eq. (5.5) with respect to sampling rate $F_s = 1/T_s$. Compared to the most recent CDACs included, the RDAC becomes the most efficient of all when F_s is below $F_B = 480$ kHz. In reality, F_B may shifts to lower frequencies due to design constraints such as ADC requiring certain time margin for worst-case comparator times or C_{bpsh} being limited by factors other than thermal noise level. Despite of these potential design challenges, we expect the RDAC to represent a preferred solution for the majority of use cases



DAC implementations	Proposed R-2R	CDAC				
		Conventional	Split-capacitor	Monotonic-switching	Merged-capacitor	Charge-average
Reference	This work	[28]	[26]	[25]	[27]	[11]
Energy factor (A_k or $E/V_{REF}^2\ C_u$)	Eq. (5)	1365.3	847.1	255.5	170	88.6

* Curves are plotted with C_u = 5fF (as in [11, 25]), C_{bpsh} = 33fF (determined by DAC thermal noise level), and total TDC plus digital delay times of 600ns.

Figure 5.7: Resistive DAC energy scaling with sampling rate.

with lower sampling rates.

The RDAC maintains its advantage in energy efficiency when the CDAC capacitors are matching limited rather than thermal-noise limited at moderate resolutions. As calculated and stated in Fig. 5.7, the C_{bpsh} value under thermal noise requirement for 10b is 33 fF, which is normally not a feasible value to implement a CDAC with sufficient matching, therefore allows relatively lower power. Once the CDAC is noise constrained at high resolutions, its dynamic power consumption becomes comparable to that of the RDAC since capacitors from both structures are dictated by the same kT/C requirement.

The 2b/step scheme improves the RDAC's energy efficiency in two ways. First, it

halves the total number of conversion steps and reduces the summation limit in Eq. (5.4) from "N" to "$N/2$". As a result, the DAC's total on-time (and energy dissipation) is significantly reduced. Second, the 2b/step scheme saves almost half of ADC's active time and provides a huge time margin for DAC settling, which allows larger unit resistances and lower DAC power. Although the CDAC likewise exhibits reduced dynamic energy under the 2b/step scheme, the RDAC potentially saves more energy. From Eq. (5.3) and (5.4), a 2b/step CDAC saves on average 50% the energy of a 1b/step CDAC, while a 2b/step RDAC saves anywhere from 50% (when E_s dominates DAC energy) to 75% (when E_s is negligible) the energy of the 1b/step RDAC (conservatively assuming R_u is doubled in the 2b/step case).

The conventional synchronous SAR algorithm, as shown in Fig. 5.3(a), could leave large idle periods between conversion steps during which static energy is wasted. As illustrated in Fig. 5.3(b), the asynchronous scheme takes only as much time as the circuit speed requires to convert each bit. Thus, we adopted the asynchronous processing technique [100, 110] to eliminate idle times during conversion. In this design, the asynchronous technique complements the RDAC by dynamically scaling its energy to actual conversion times, as well as avoiding static energy dissipation during sleep mode at the end of each clock period.

5.4 2b/Step Conversion With Reduced Hardware

The following sections detail the principle of the proposed 2b reference scheme and the time-domain 2b comparison process. Using the low-power hybrid DAC greatly reduces

additional DAC hardware for 2b/step conversion, leading to substantial static and dynamic energy savings from reduced conversion time and activities. The proposed 2b comparison scheme is based on a time-domain interpolation mechanism, which allows less comparator hardware compared to traditional approaches, thereby simplifying both circuitry and matching complexity. In this design, the 2b/step architecture helps to achieve low-energy operation instead of the more conventional application of higher-speed operation.

5.4.1 Pseudo DAC Assisted 2b Reference Scheme

In a SAR ADC, converting two consecutive bits (*DH* and *DL*) in one step requires multiple reference levels, as illustrated in Fig. 5.8. At the k^{th} conversion step, these references include the high-bit reference $V_{RH,k}$ to determine *DH* and the two low-bit references $V_{RLi,k}$ (i=1,2) to determine *DL*. Since $V_{RLi,k}$ takes on a wide range of voltage levels, multiple DACs [103] are normally required, leading to significant area and energy overhead, especially in fully differential implementations.

Table 5.4: An numeric example: reference values for 2b/step conversion with example input '1011010011'

Conv. Step (k)	Conv. Bits	$V_{RH,k}$	$V_{RL1,k}, V_{RL2,k}$	δ_1, δ_2 ($V_{AUX,k}$)	Result
1	D9, D8	1/2	1/4, 3/4	$\pm$1/4	10
2	D7, D6	5/8	9/16, 11/16	$\pm$1/16	11
3	D5, D4	23/32	45/64, 47/64	$\pm$1/64	01
4	D3, D2	91/128	181/256, 183/256	$\pm$1/256	00
5	D1, D0	361/512	721/1024, 723/1024	$\pm$1/1024	11

This design proposes a different scheme that bypasses full-range DACs for additional reference generation. According to the successive approximation algorithm, the differ-

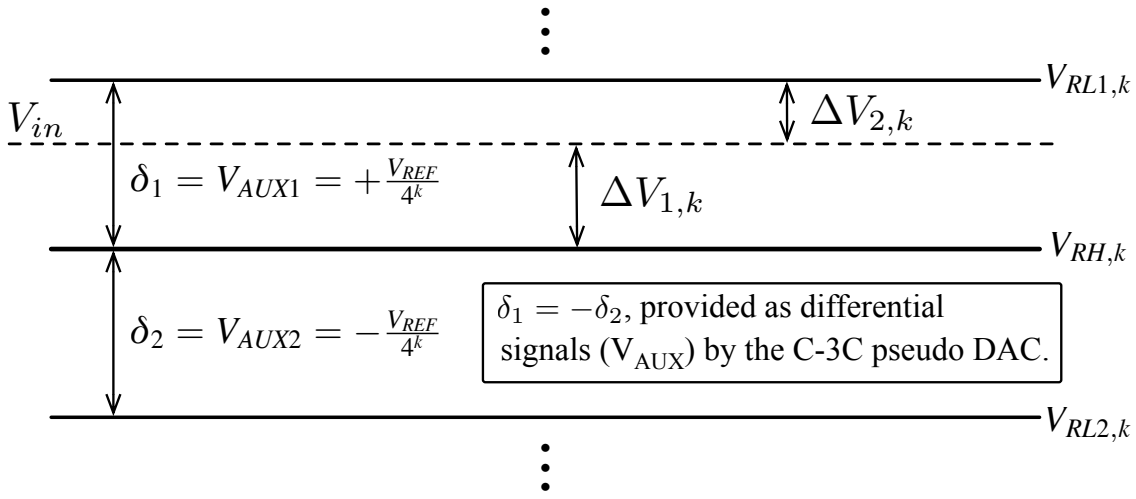


Figure 5.8: Reference levels needed for 2b/step conversion at k^{th} conversion step. Here $\Delta V_{2,k}$ is chosen as $\Delta V_{1,k} - (+V_{AUX})$ since $DH = 1$.

ences between $V_{RH,k}$ and $V_{RLi,k}$, namely δ_1 and δ_2 (in Fig. 5.8), take on differential values of $\pm V_{REF}/4^k$ at the k^{th} step during the 2b/step conversion process. Table 5.4 shows the required reference levels for 2b/step conversion with an example input corresponding to the digital output of 1011010011. Thus, instead of directly generating $V_{RLi,k}$, it suffices to provide auxiliary references $V_{AUXi,k}$ to represent the differential values of $V_{RLi,k}$:

$$V_{AUXi,k} = V_{RLi,k} - V_{RH,k} = \pm V_{REF}/4^k, i = 1, 2 \tag{5.6}$$

assuming $V_{RH,k}$ is available. During each conversion step, the high bit *DH* is determined by the residue voltage $\Delta V_{1,k}$, which is equal to the voltage difference between the input signal and $V_{RH,k}$:

$$\Delta V_{1,k} = V_{in} - V_{RH,k} \tag{5.7}$$

The low bit *DL* is determined by another residual voltage, $\Delta V_{2,k}$, which is equal to the difference between $\Delta V_{1,k}$ and the auxiliary references $V_{AUXi,k}$:

$$\Delta V_{2,k} = \Delta V_{1,k} - V_{AUXi,k} \tag{5.8}$$

Substituting corresponding terms using (5.6) and (5.7), we can rewrite Eq. (5.8) as:

$$\begin{aligned} \Delta V_{2,k} &= (V_{in} - V_{RH,k}) - (V_{RLi,k} - V_{RH,k}) \\ &= V_{in} - V_{RLi,k} \end{aligned} \tag{5.9}$$

Therefore, $\Delta V_{2,k}$ indeed represents the comparison between the input signal and low-bit references. Fig. 5.9 shows the signal flow representation of the proposed 2b conversion process.

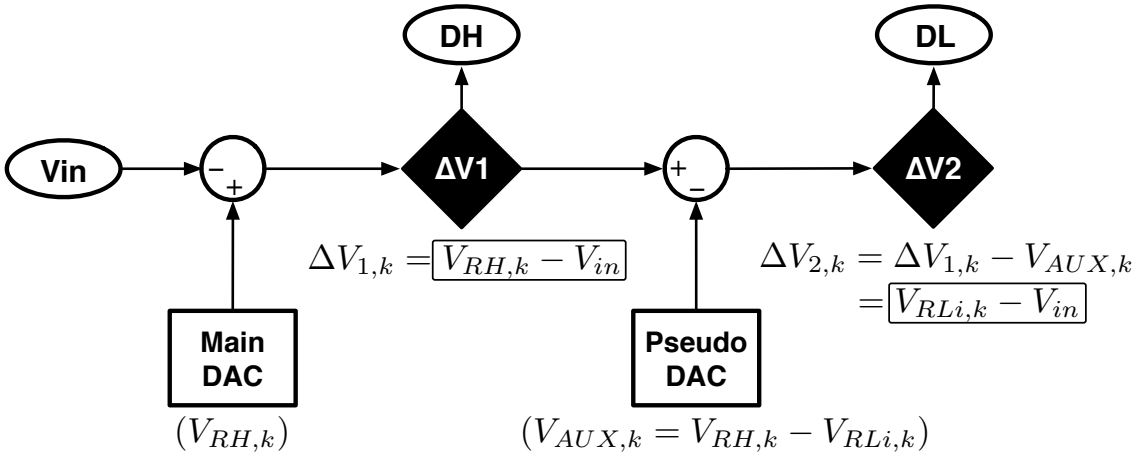


Figure 5.9: Signal flow chart to illustrate the proposed 2b/step reference scheme.

Compared to the conventional method, the proposed 2b reference scheme offers significant advantages. First of all, the auxiliary references $V_{AUXi,k}$ are differential signals,

which can be easily realized by one single reference instead of two ($V_{RLi,k}$) in a differential implementation. This results in area and power savings for one pair of differential DACs. Secondly, $V_{AUXi,k}$ represents a code/input-independent voltage sequence starting with $\pm V_{REF}/4$ and divided by 4 during each subsequent step. Therefore, the proposed scheme obviates another pair of full-range DACs. Fig. 5.10 illustrates the savings of DAC hardware along with S&H circuitry reductions. As will be shown later, a simple C-3C switched-capacitor charge-redistribution structure can implement this auxiliary reference. Furthermore, since the R-2R DAC starts to settle during the S&H period, the initial level of $\pm V_{REF}/4$ is already available from the R-2R DAC at the first comparison, requiring no extra reference sources.

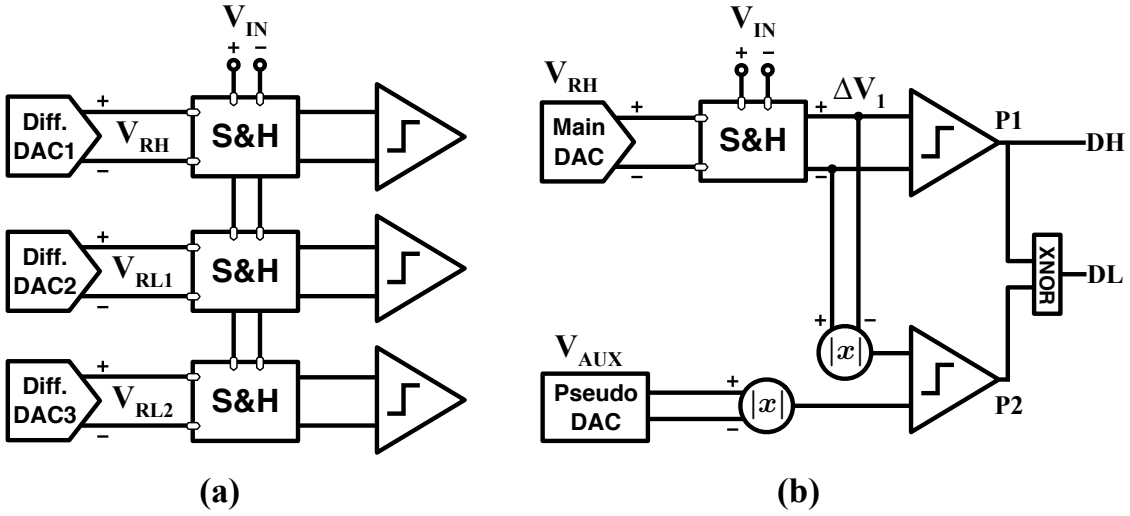


Figure 5.10: Top level diagrams of (a) conventional and (b) proposed 2b/step conversion architecture.

5.4.2 *Interpolation Assisted 2b Comparison*

In a conventional 2b comparison scheme, three comparators are normally required: one comparator for the input and the *DH* reference, and two comparators for the input and the two *DL* references, respectively. Fig. 5.10(a) shows such a comparison scheme that also includes three sampling front-ends and three pairs of differential DACs. In [104], the interpolated sampling method was proposed to reduce down to two pairs of differential references and two sampling front-ends based on a resistive string DAC with a switch network, but the scheme still needed three comparators to generate a 2b result.

In this design, the 2b comparison scheme is further simplified via absolute value comparison and sign interpolation. Depending on the higher-bit result *DH*, the lower-bit *DL* is generated by choosing the result from one of the two comparisons between (1) $\Delta V_{1,k}$ and $+V_{AUXi,k}$, and (2) $\Delta V_{1,k}$ and $-V_{AUXi,k}$ (Fig. 5.8 may help visualize this process). In other words, *DH* also contains the sign information of $V_{AUXi,k}$ for determining *DL*. Thus, it suffices to compare the absolute values of $\Delta V_{1,k}$ and $V_{AUXi,k}$ and obtain *DH* and *DL* via sign interpolation. Fig. 5.10(b) demonstrates the proposed comparison scheme, where *DH* $=$ *P1* and *DL* $= \overline{P1 \oplus P2}$. As will be shown later, interpolating *DL* only takes a simple *XNOR* gate applied to *P1* and *P2*, while absolute values of $\Delta V_{1,k}$ and $V_{AUXi,k}$ can be easily realized in time domain at a mere cost of four additional transistors within the 2b TDC.

Reducing comparator hardware from 3X to 2X saves area and power overhead. In this 2b scheme, the overall comparator energy efficiency is the same as in 1b schemes due to halved switching events. Reduced TDC hardware also lessens mismatch issues caused by

multiple comparators. In this time-based design, the TDC's input-referred offset can be reduced via larger voltage-to-time gains or LSB timings (T_{LSB}) [86]. With abundant time budget available at low conversion rates, it becomes affordable to use larger T_{LSB} to mitigate comparator offsets and potentially waive calibration effort for comparator mismatch, albeit at the cost of longer comparison time and increased DAC energy.

5.5 Circuit Description

The proposed ADC is implemented as a fully differential structure. This section describes circuit details and design considerations for main circuit blocks. For the convenience of future discussions, we define differential signals as: $V_{in} = V_{inp} - V_{inn}$, $V_{DAC} = V_{DACp} - V_{DACn}$, $\Delta V_1 = \Delta V_{1p} - \Delta V_{1n}$, and $V_{AUX} = V_{AUXp} - V_{AUXn}$. The auxiliary references $V_{AUX1,2}$ previously described are now $V_{AUXp,n}$, respectively.

5.5.1 R-2R Main DAC

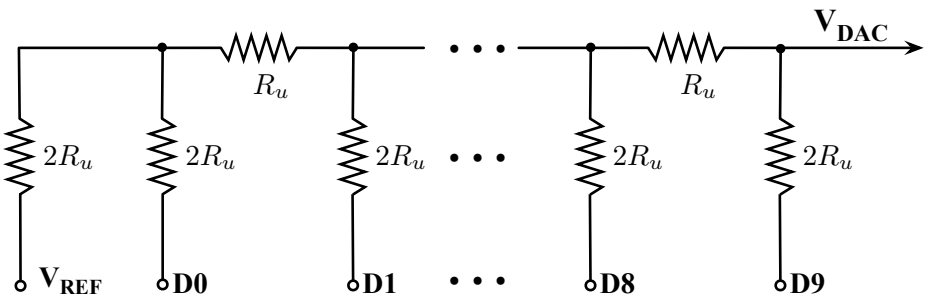


Figure 5.11: Implementation of a conventional 10-bit R-2R DAC.

The implementation of a conventional 10-bit R-2R DAC is shown in Fig. 5.10. The input signals include the reference voltage V_{REF} representing the full scale output of the

DAC, and the 10 digital input bits with $D9$ being the most significant bit (MSB) and $D0$ being the lease significant bit (LSB). The analog output voltage of the DAC is expressed as

$$V_{DAC} = \frac{V_{REF}}{2^{10}} \cdot \sum_{i=0}^{9} Di \cdot 2^i \tag{5.10}$$

where digital input bits Di take on values of "1" or "0". In general, an N-bit R-2R DAC uses $2N$ unique resistor elements in a ladder configurations. Each of the horizontal resistors are valued at R_u, while each of the vertical resistors are valued at $2R_u$. In a practical layout, the vertical resistors are usually realized as two R_u resistors in series in order to achieve optimal matching performance. Therefore, a total of $3N + 1$ unit resistors are utilized to realize an N-bit R-2R DAC.

The matching performance of the unit resistors determines the overall linearity of the DAC. The matching characteristics of resistors are expressed as [111]:

$$\sigma_R = \frac{\Delta R_u}{R_u} = \frac{\alpha_R}{\sqrt{WL}} \tag{5.11}$$

where σ_R is the resistor mismatch variance, α_R is a process-dependent matching coefficient, W is the width of the unit resistor, and L is the length of the unit resistor. Therefore the resistor DAC achieves better matching and thus better linearity using larger area for unit resistors. In essence, this is a trade-off between circuit area compactness and ADC linearity performance, which the capacitive DAC embraces as well. However, the size and hence the power of a capacitor DAC increase simultaneously with the effort of increasing

DAC linearity, while the power of a resistive DAC is dependent on its W/L ratio rather than area. Therefore, it is possible to maintain the same resistive DAC power consumption in the process of linearity optimization.

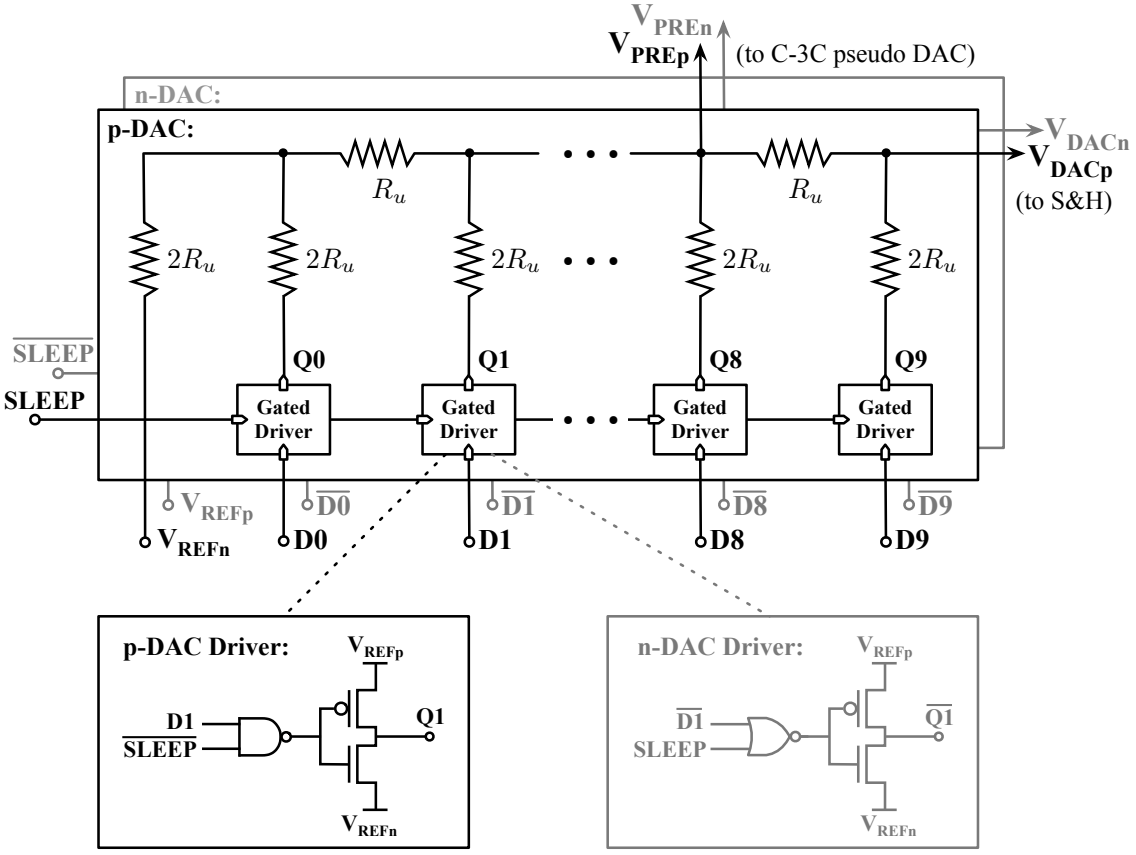


Figure 5.12: Implementation of R-2R DAC with power-gating technique using the *SLEEP* signal.

As shown in Fig. 5.12, the proposed R-2R DAC provides the main reference V_{DAC} (or V_{RH}) to determine *DH*, and auxiliary levels $\pm V_{REF}/4$ (via V_{PRE}) to initialize the pseudo DAC during S&H phase. Reference voltage V_{REFp} is the same as *VDD* at 0.6 V, while V_{REFn} is connected to ground. At 10-bit resolution, the R-2R DAC uses a total of 31 unit

resistors. The gated bit-drivers shut down the DAC circuit when the ADC enters sleep mode. For the p-DAC drivers, a NAND gate engages the *SLEEP* signal, which when asserted, forces 0 volt across the resistive ladder, eliminating static current. The n-DAC drivers involve NOR gates and operate in a similar fashion.

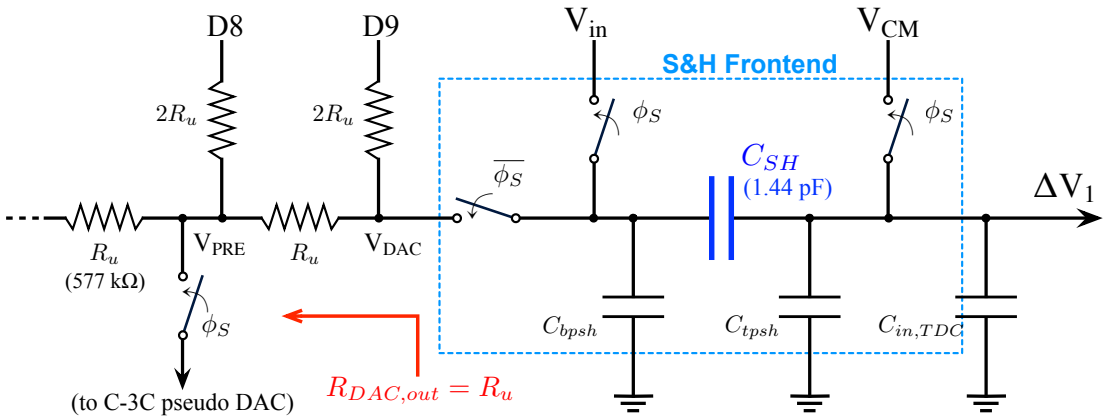


Figure 5.13: R-2R DAC output connected with the S&H frontend: $\tau_{DAC} \approx R_u C_{bpsh}$.

The R-2R DAC's settling time depends on its output resistance and the S&H capacitor. Fig. 5.13 illustrates the sampling front-end circuit composed of three bootstrapped switches [2] and a sampling capacitor C_{SH} and connected to the R-2R DAC's output. The output resistance of the R-2R DAC constantly equals R_u regardless of DAC codes. C_{bpsh} and C_{tpsh} are the bottom and top plate capacitance of C_{SH}, respectively, and $C_{in,TDC} \ll C_{bpsh}$ is the TDC's input capacitance. Ignoring switch resistance, the settling time constant is approximately $\tau_{DAC} = R_u C_{bpsh}$. As discussed previously, although the R-2R DAC's energy consumption within its settling time frame is independent of resistor values, larger resistance is still preferred for less static power beyond settling.

The transistor level implementation of the bootstrapped switch used in this ADC is shown in Fig. 5.14. The switch is controlled by complementary clock phases ϕ_S and $\overline{\phi}_S$: when ϕ_S is high ('1' or VDD) the switch is turned on; when ϕ_S is low ('0' or ground) the switch is turned off. The input signal is injected at the source node of transistors MN1 and MN2 and passed through to node V2 via MN2 and to the output via MN1. The capacitors C1, C2 and C3 are charged to VDD during steady states, allowing voltage stacking at the gate terminals of transistors to achieve nodal voltages higher than supply level VDD. In this implementation with rail-to-rail input range, the threshold voltages of NMOS transistors are around 400 mV and the supply VDD is only 600 mV; thus it is of pivotal importance to obtain large switch voltages in order to achieve required linearity performance.

As discussed in [2], the nodal voltage levels within the switch at the complementary phases of ϕ_S are listed in Table 5.5. When the switch is turned on or ϕ_S = VDD, the gate voltage of the sampling transistor MN1 is equal to VDD+Vin, leading to a gate-source voltage of $V_{GS,MN1}$ = VDD. Therefore, the gate-source bias voltage of MN1 is independent of input voltage level and is always constant at supply voltage VDD, which effectively eliminates switch harmonic distortion. The maximum internal voltage is 2VDD = 1.2 V, which is well below the upper voltage limit of this standard 0.18-μm CMOS process and will not raise device breakdown concerns.

Based on proper matching of DAC resistors and different signal paths as well as adequate TDC time allowance, we choose a unit resistance of 577 kΩ and S&H bottom-plate

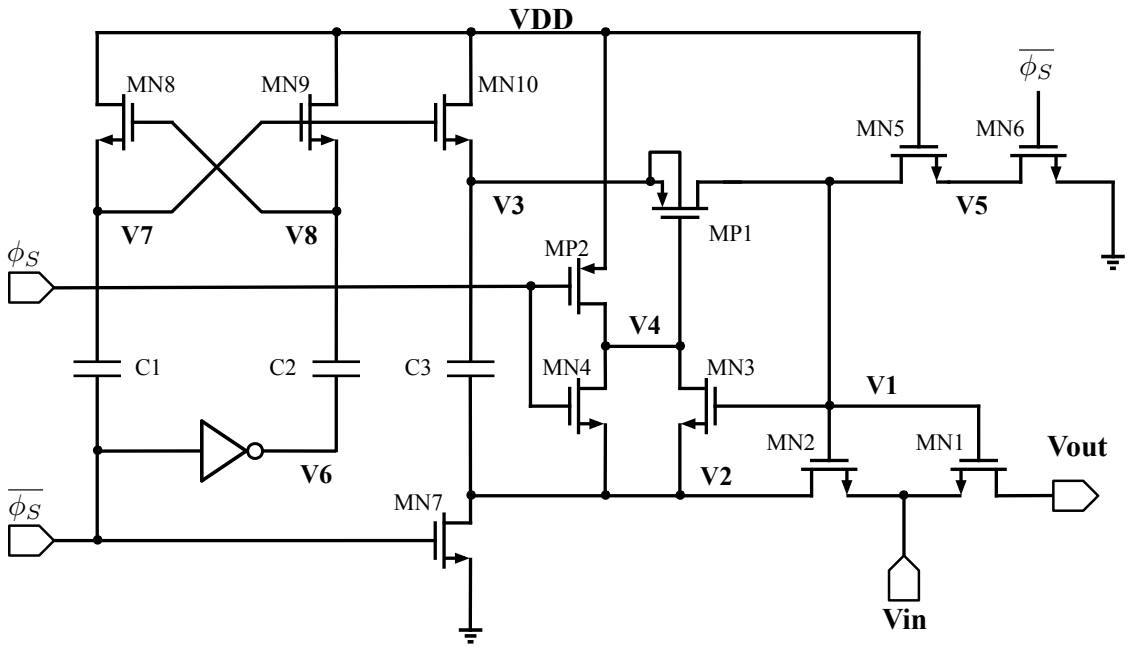


Figure 5.14: Transistor level implementation of bootstrapped switch [2].

capacitance of 84 fF to allow the DAC to settle within 400 ns. The R_u dimensions are W $= 360\ \mu m$ and L $= 1\ \mu m$, and are determined by varying the L/W ratio to increase its resistance while maintaining the same area for matching accuracy until the DAC's settling time reaches its time budget for this design. The unit resistor's $\pm 3\sigma$ matching accuracy is 0.58% according to the process data. The DAC's worse-case DNL and INL errors are calculated as $\sigma_{DNL,max} = 0.18$ LSB and $\sigma_{INL,max} = 0.092$ LSB, respectively. The simulated noise levels for the DAC and the S&H circuit are 202 μV_{rms} and 55.7 nV_{rms}, respectively.

5.5.2 C-3C Pseudo DAC

The auxiliary reference levels $V_{AUX,k}$ are generated by the pseudo DAC consisting of two parallel capacitors *C* and *3C* as illustrated in Fig. 5.15. Operations of the pseudo DAC

Table 5.5: Nodal voltages at different clock phases within the bootstrapped switch

Node	$\phi_S = 0$	$\phi_S = 1$
ϕ_S	0	VDD
N1	0	VDD+Vin
N2	VDD	Vin
N3	VDD	VDD+Vin
N4	2VDD	0
N5	2VDD	VDD
N6	VDD	2VDD
N7	Vin	0
N8	0	Vin

are controlled by three phases: the sampling phase ϕ_S, the charge redistribution phase ϕ_K, and the charge dislodge phase $\overline{\phi_K}$. Fig. 5.16 shows the pseudo DAC's output voltage levels along with a timing diagram of these control phases. During the phase of ϕ_S, the capacitor *C* is precharged to $\pm V_{REF}/4$ by the R-2R DAC, while the capacitor *3C* is connected to common mode level V_{CM} and depleted of any charge. After the first comparison, ϕ_K goes high and the voltage across capacitor *C* is divided by 4 via charge redistribution, resulting in a new reference voltage for the next comparison. Afterwards the charges on capacitor *3C* are depleted again for the next redistribution cycle. This process continues and provides the proper references for each conversion step. Since the capacitors switch under rapidly decreasing voltages, the pseudo DAC operates with an energy consumption of a mere 5% of the total energy budget.

The matching requirement for the pseudo DAC's capacitors is much relaxed due to

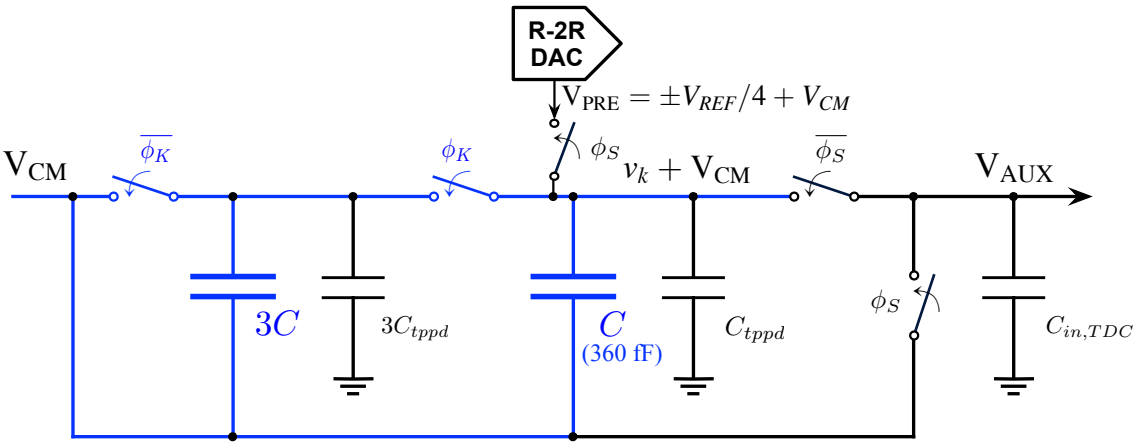


Figure 5.15: Implementation of C-3C pseudo DAC with top-plate parasitic capacitors C_{tppd}.

low-voltage operations. Since the maximum voltage to process is $\pm V_{REF}/4$ at $k = 1$, the maximum error voltage ($|\sigma_{AUX}|_{max}$) due to capacitor mismatch occurs with the 2^{nd} auxiliary reference ($\pm V_{REF}/16$) after the first voltage division. Forcing $|\sigma_{AUX}|_{max} < 0.5V_{LSB}$ reveals a matching requirement ($\delta C/C_u$) of only 1.04%, which is much reduced from the main DAC's 10b linearity.

Besides capacitor mismatch, parasitic capacitances also affects voltage division accuracy and thus generate voltage errors. These parasitics mainly concern the TDC's input parasitic capacitance $C_{in,TDC}$ and the pseudo DAC's top plate capacitance C_{tppd} (including capacitance from switches and metal wires). However, as will be demonstrated below, such division errors may only induce gain errors rather than linearity degradation, provided both signal paths of $V_{AUX,k}$ and $\Delta V_{1,k}$ are properly matched via design. Considering all the stray capacitances in Fig. 5.15, the pseudo DAC's output voltage after division can be

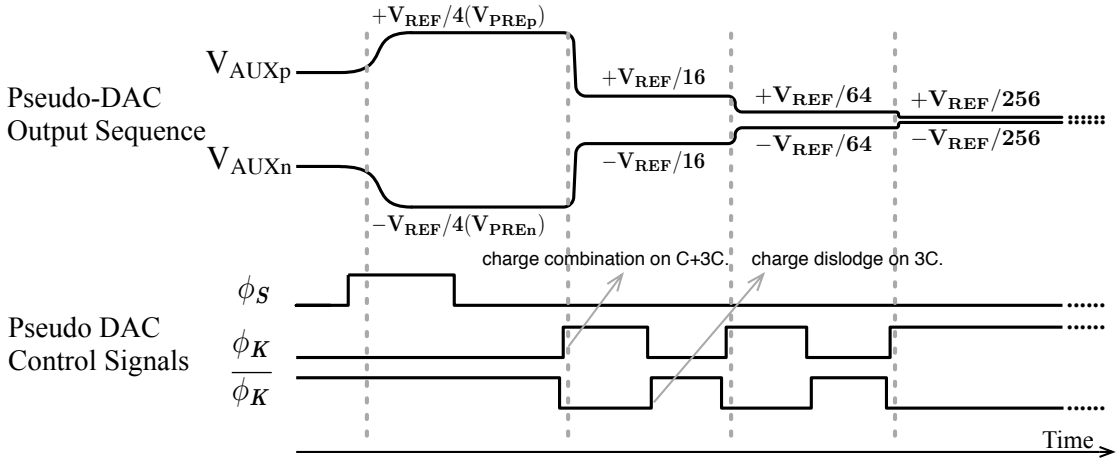


Figure 5.16: C-3C pseudo DAC output levels along with timing diagram of control phases.

calculated as

$$V_{AUX,k} = \frac{v_k}{4} \cdot \underbrace{\left(\frac{4C'}{4C' + C_{in,TDC}}\right)}_{\text{error factor: } E_A} + V_{CM} \tag{5.12}$$

where v_k is the voltage level before each division, and $C' = C + C_{tppd}$. Error factor *EA* is induced by the parasitics. Similarly, based on Fig. 5.13, the expression of $\Delta V_{1,k}$ at the input of the TDC can be derived as

$$\Delta V_{1,k} = (V_{in} - V_{DAC,k}) \cdot \underbrace{\left(\frac{C_{SH}}{C'_{SH} + C_{in,TDC}}\right)}_{\text{error factor: } E_B} + V_{CM} \tag{5.13}$$

where $C'_{SH} = C_{SH} + C_{tpsh}$. Based on Eq. (5.8), the value of C_{SH} should be set to 4X that of *C* in order to equalize the error factors E_A and E_B and avoid linearity degradations.

In the above analysis, we have assumed the values of C_{tpsh} and C_{tppd} are matched via proper layout and are sufficiently smaller compared to C_{SH} such that capacitances

$4C' = C_{SH}$ and error terms $E_A = E_B$. However, the two error terms differ by the value of C_tpsh even with the condition $C_{SH} = 4C$, thereby giving rise to linearity error which should be controlled under $0.5V_{LSB}$. To factor in the difference in the error terms, we express

$$E_B = E_A - \delta_c \tag{5.14}$$

where $\delta_c \approx \frac{C_{tpsh}}{C_{SH}} \approx \frac{C_{tppd}}{C}$. Therefore, Eq. 5.12 and Eq. 5.13 can be rewritten as

$$V_{AUX,k} = \frac{v_k}{4}E_A + V_{CM} \tag{5.15}$$

$$\Delta V_{1,k} = (V_{in} - V_{DAC,k})(E_A - \delta_c) + V_{CM} \tag{5.16}$$

The nonlinear error due to the inequality between E_A and E_B only affects the term $\Delta V_{2,k}$ which is derived by subtracting the above two equations

$$\Delta V_{2,k} = \underbrace{(V_{in} - V_{DAC,k} - \frac{v_k}{4})E_A}_{\text{linear term } \Delta V'_{2,k}} - \underbrace{(V_{in} - V_{DAC,k}) \cdot \delta_c}_{\text{nonlinear error}} \tag{5.17}$$

When the value of the linear term $\Delta V'_{2,k}$ is large, the normally small-valued nonlinear error $(V_{in} - V_{DAC,k})\delta_c$ is not significant enough to alter the comparison results based on $\Delta V'_{2,k}$, i.e. to change its value from positive (> 0) to negative (< 0) or vice versa. Therefore, we only need to consider cases when $\Delta V'_{2,k} \rightarrow 0$ or $V_{in} - V_{DAC,k} \approx \frac{v_k}{4}$, when the nonlinear term becomes most significant and can be expressed as $\frac{v_k}{4}\delta_c$. Since $\frac{v_k}{4}$ keeps decreasing during the conversion process, its maximum value is $\frac{V_{REF}}{16}$ after the first

division and its associated error happens. Thus, in order to avoid erroneous comparison results from $\Delta V_{2,k}$, it is necessary to have

$$|(V_{in} - V_{DAC,k}) \cdot \delta_c|_{max} = \frac{V_{REF}}{16} \cdot \delta_c < 0.5 V_{LSB} = \frac{V_{REF}}{2^{11}} \tag{5.18}$$

This condition leads to $\delta_{c,max} = \frac{1}{2^7}$ or $C_{tpsh} < \frac{1}{2^7} C_{SH}$, which is quite achievable via careful layout. In this design, metal-insulator-metal (MIM) capacitors with values $C = 360$ fF and $C_{SH} = 4C = 1.44$ pF are used in order to tolerate total top-plate parasitic capacitances up to 11.2 fF and minimize the effect of E_A/E_B mismatch.

5.5.3 2b Time-Domain Comparator

Conventional SAR ADC implementations use voltage domain comparators to compare the input signal level with the DAC output level. As modern CMOS technology advances into deep sub-micron regime, the supply voltage VDD shrinks as well. Therefore, the LSB voltage of the same resolution becomes smaller with reduced VDD, imposing more challenging noise and offset requirements for the comparator. To combat such difficulties, higher power consumption and larger device area are inevitable to improve the overall performance of the comparator, making the overall ADC less compact and energy efficient.

Alternatively, the comparison process can be accomplished in time domain rather than voltage domain. In this architecture, the major advantage of using the time-domain comparison scheme is that it utilizes the ample timing budget to improve performance under low-voltage supplies and consumes very little power. As Fig. 5.17(a) illustrates, voltage

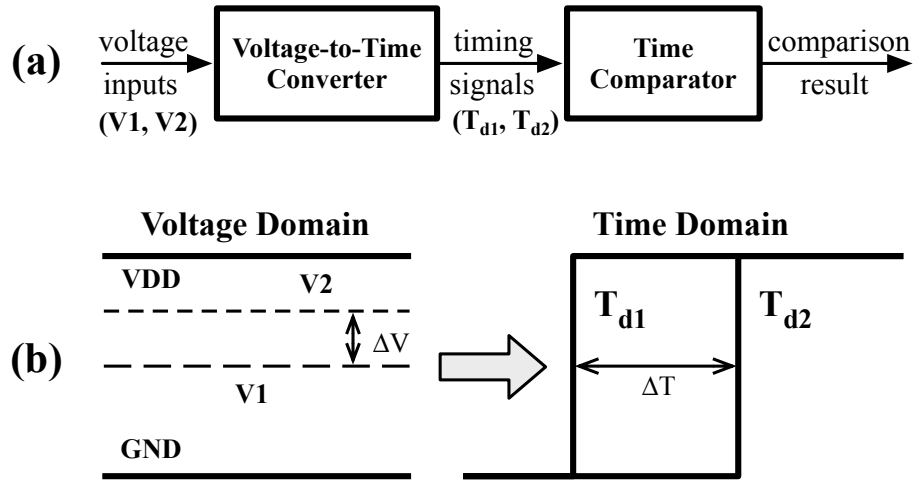


Figure 5.17: Signal comparison in time domain: (a) block level voltage-to-time conversion and comparison concept; (b) comparison signals in in voltage domain vs time domain.

signals can be translated to timing signals using voltage-to-time (V2T) converters, followed by timing comparison via time comparators (which are usually implemented as phase detectors). The demonstration of Fig. 5.17(a) basically manifests a block level implementation of a TDC. Fig. 5.17(b) shows the relative signal amplitudes in both voltage domain and time domain. Unlike the voltage domain case, time domain comparison compares the time delays of pulse signals, thus decoupling the supply voltage amplitude with the resolution requirement of the comparator. The TDC actually benefits from technology scaling in terms of more refined time resolutions in smaller-size technologies.

In general, an TDC can be implemented using the configuration illustrated in Fig. 5.18(a). Voltages V_{in1} and V_{in2} are input signals to the voltage-controlled delay lines (VCDLs) which delay the pulsed signal Φ_K. The voltage information are translated into time delays between the VCDL's output pulse and its input pulse Φ_K, thereby accomplishing

the voltage-to-time conversion. The time comparator, normally implemented as a phase detector, compares the arrival times of the input pulses, generating a comparison result based the delay times caused by the VCDLs. As shown in Fig. 5.18(b), the VCDL can be composed of a number of cascaded voltage-to-time (V2T) cells, with each cell contributing to the total delay time of T_n. The V2T cells are normally current controlled inverters as demonstrated in Fig. 5.18(c). The input pulse Φ'_K is delayed via the inverter with an output pulse Φ''_K. The time duration of t_d between the input and output pulse signals is determined by the input voltage V_{in} at the current source transistor MN0 and the size of the load capacitor C_L.

The previous discussion introduces the principles of a 1b TDC. In this particular ADC, an innovative 2b TDC is proposed to achieve minimal energy and circuit overhead for the 2b/step conversion scheme. Fig. 5.19 shows the top-level block diagram of the proposed 2b TDC. The four identical voltage-controlled delay lines (VCDLs) and two phase detectors (PDs) is equivalent to two 1b TDCs in hardware. A dummy PD is used to equalize different delay signal path parasitics.

The VCDLs convert input differential voltage signals ΔV_1 and V_{AUX} into time delays $T1 \sim T4$ embedded in delayed voltage signals $V_{T1} \sim V_{T4}$, respectively. By increasing delay stages, the voltage-to-time (V2T) conversion gain can be increased and input-referred noise and offset can be reduced [86], at the cost of increased VCDL power. In this design, the VCDL's simulated input-referred noise is 144 μV_{rms} with six V2T stages. As demonstrated in Fig. 5.20, the conventional VCDL in (a) compares on rising clock edge and

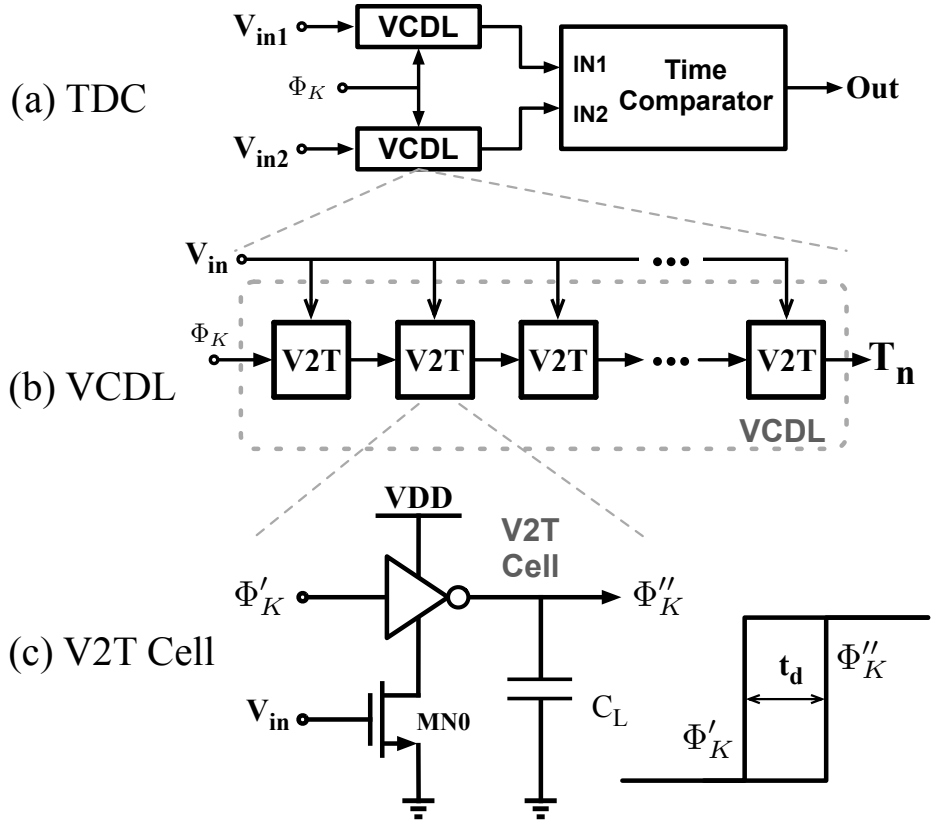


Figure 5.18: General TDC implementation: (a) top level block diagram based on VCDLs and a PD; (b) VCDL structure with cascaded V2T stages; (c) V2T cell based on a voltage controlled delay cell.

resets itself on the falling clock edge, while the proposed VCDL in (b) compares on both clock edges. With *complementary* input transistors in each V2T stage, both pull-down and pull-up actions are voltage-controlled, thus avoiding the need of reset phases.

As indicated by the red colorcode in Fig. 5.20, in a rising-edge comparison, delay stages are controlled by NMOS current sources with input V_{cn} and PMOS current sources with input V_{cp}. Thus, the amount of time delay is proportional to the input control voltage $(V_{cp} - V_{cn})$. As illustrated in Fig. 5.21, smaller (more negative) VCDL input voltages

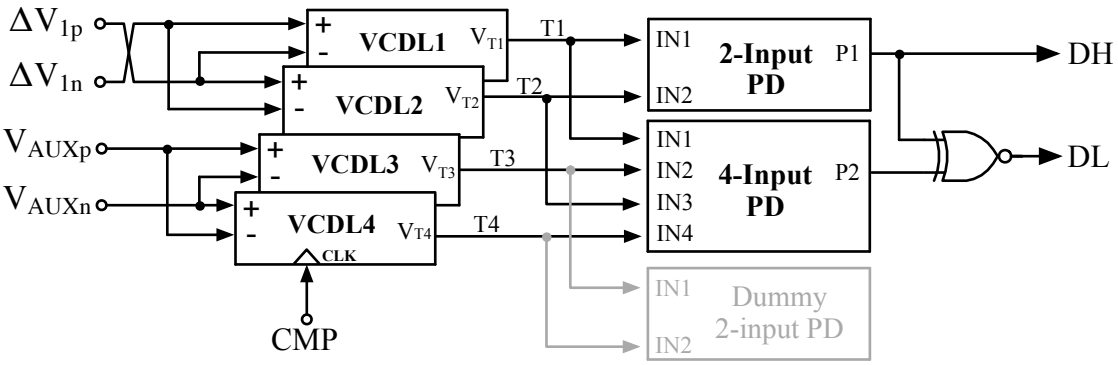


Figure 5.19: Implementation of 2b TDC. Inputs ΔV_{1p} and ΔV_{1n} are switched to account for the polarity inversion in the S&H circuit.

lead to smaller time delays and vice versa. Correspondingly, in a falling-edge comparison, the voltage-to-time-delay relationship is inverted since delay stages are controlled by V_{cn} on PMOS and V_{cp} on NMOS. Thus, smaller (more negative) VCDL inputs lead to larger delays and vice versa.

It's worth noting that memory effect could arise when extremely large or small inputs are applied leading to small delays on one VCDL but huge delays on the other. As a result, the states of the latter VCDL's internal nodes become stagnant and error timing can be generated in the next comparison. As shown in Fig. 5.22(a), we included extra acceleration transistors MPa and MNa to help the internal nodes proceed to the correct states once the current comparison is finished. The timing digram in Fig. 5.22(b) illustrates the acceleration process controlled by signal *RDYx*, which is a delayed version of the *READY* signal generated after the completion of the current comparison.

Implementations of the PDs are illustrated in Fig. 5.23. The 2-input latch-based PD

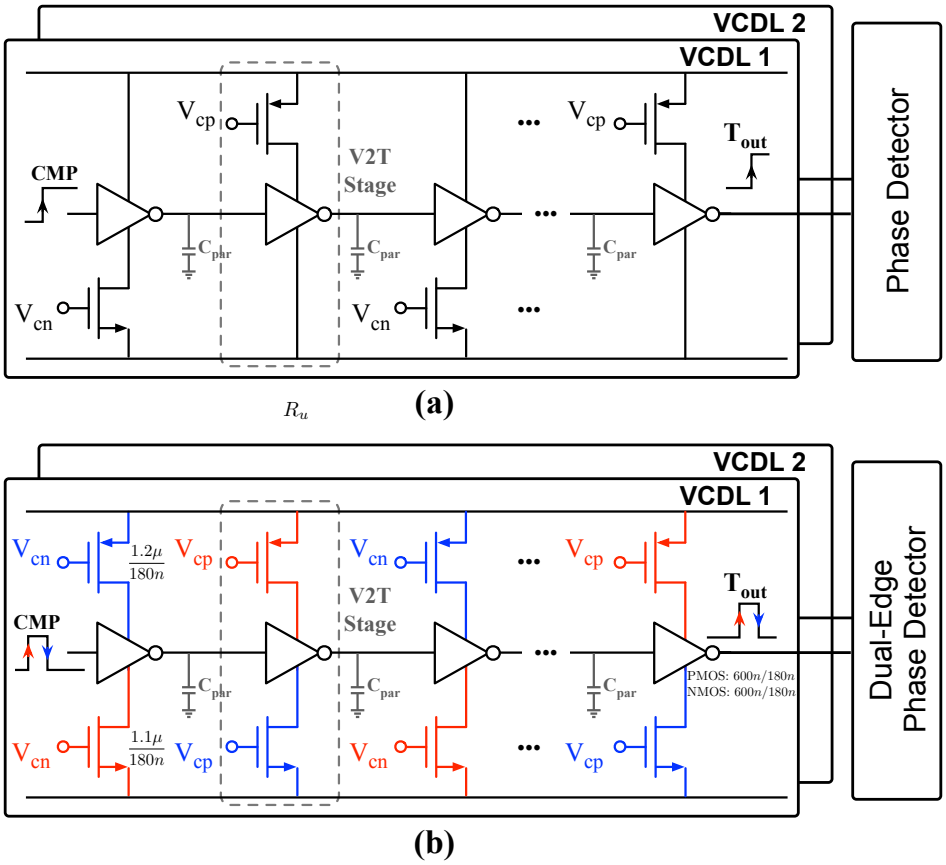


Figure 5.20: VCDL design comparison: (a) conventional single-edge operation; (b) proposed dual-edge operation with complementary input transistors in each stage.

makes a decision on its outputs (*P1* and *P1x*) upon the arrival of V_{T1} or V_{T2}. The control signals *SR* and *SF* preset the PD outputs to proper levels according to different comparison edges. During a rising-edge comparison, the PD outputs are preset to '1' by *SR*. The smaller delay (generated by the VCDL with a smaller input voltage) arrives first and pulls down the corresponding output arm to '0' while the other arm stays at '1'. In a falling-edge case, the PD outputs are initialized to '0' by *SF*. The smaller delay (generated by the larger VCDL input voltage) arrives first and pulls up its arm to '1'. The timing diagram of

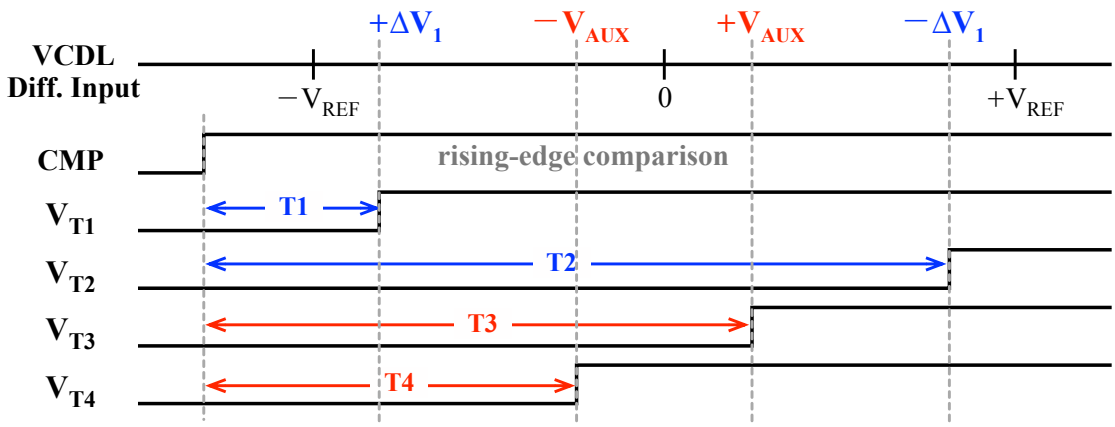


Figure 5.21: Timing diagram of VCDL signals during a rising edge comparison. Rising case: $T_{delay} \propto V_{cp} - V_{cn}$. Falling case: $T_{delay} \propto V_{cn} - V_{cp}$.

the 2-input PD and its operations are illustrated in Fig. 5.24.

The 4-input PD shares the same structure as the 2-input part except for 4 additional transistors M5∼M8 that implement the absolute-value function for time-domain signals V_{T3} and V_{T4}. By placing the input transistors of V_{T1} and V_{T2} in parallel on one arm and those of V_{T3} and V_{T4} on the other, e.g., M1‖M5 and M2‖M6, the PD will resolve when either polarity of the differential signal pairs arrives. Therefore, it is equivalent as to compare the absolute values of $|\Delta V_1|$ and $|V_{AUX}|$, the result of which is stored in *P2*. Table 5.6 outlines how the 2b results *DH* and *DL* are interpolated based on *P1* and *P2*, where included mathematical expressions are defined as: $\Delta V_1 = V_{in} - V_{DAC}$, $\Delta V_2' = |\Delta V_1| - |V_{AUX}|$, $DH = P1$, $DL = \overline{P1 \oplus P2}$.

In this TDC design, a systematic mismatch exists between the rising- and falling-edge comparisons since in each case different transistors govern the TDC's behavior. However, note that for any given bit decision process, all VCDLs receive the same edge, either rising

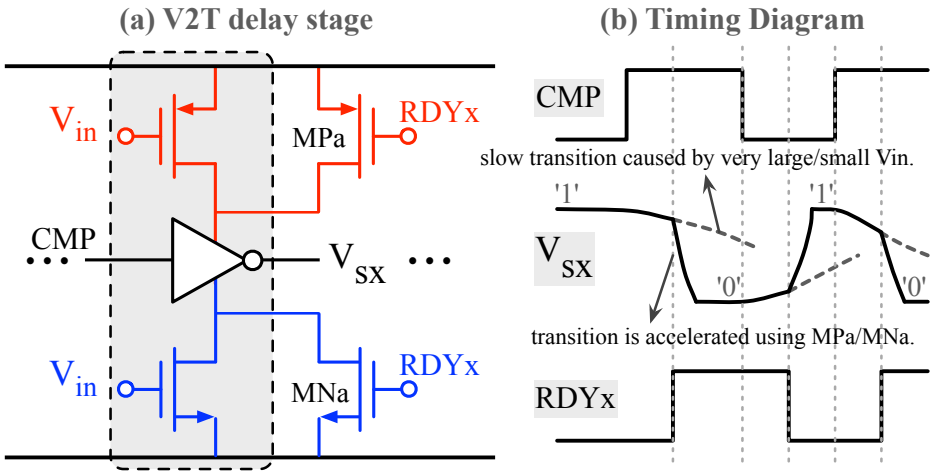


Figure 5.22: (a) VCDL delay stage with acceleration transistors MPa/MNa and (b) timing diagram of acceleration process when very large/small voltage inputs are causing memory effect.

or falling. As illustrated in Fig. 5.20, the rising and falling delays of VCDLs are governed by the following devices outline in Table 5.7, where $\Delta V_{in} \equiv \Delta V_{1p} - \Delta V_{1n}$ as shown in Fig. 5.19. Therefore, mismatch between transistors of the same color governs error in the differential delay at the rising and falling edge, which we denote as $\Delta t_{dr} \equiv \Delta t_{dr1} - \Delta t_{dr2}$ and $\Delta t_{df} \equiv \Delta t_{df1} - \Delta t_{df2}$, respectively.

The above quantities are conceptually illustrated in Fig. 5.25 along with the effect of random variations where μ and σ indicate the mean and standard deviation, respectively. As a good design approach, it is necessary to ensure that $\sigma[T_{LSB}] < \sigma[T_{LSB}]$, where $T_{LSB} = t_{dr,f}(V_{LSB}) - t_{dr,f}(-V_{LSB})$, to allow the TDC to tolerate input-referred offset without calibration. The mismatch from one edge to the other does not play a role in the comparators decision, only the mismatch in corresponding transistors (e.g. red transistors from *VCDL1* vs. red transistors from *VCDL2*). The monte-carlo simulations results

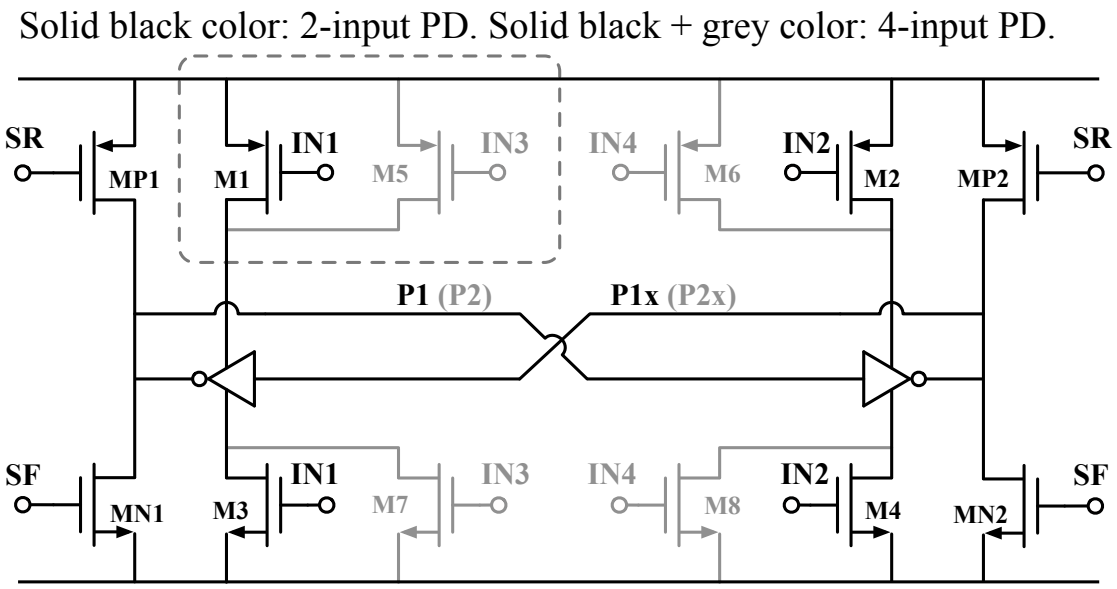


Figure 5.23: Implementation of PDs. Parallel inputs (of 4-input PD) M1‖M5 is equivalent as a single input of min{T1, T2} in time domain, or $|\Delta V_1|$ in voltage domain.

(process and mismatch) illustrated in Fig. 5.26 show the means and standard deviations of delay lines LSB timing T_{LSB} at the LSB input of V_{LSB}. The falling edge MC (left) shows a mean $\mu[T_{LSB,f}] = 7.85ns$, with a standard deviation $\sigma[T_{LSB,f}] = 1.59ns$, while the rising edge MC (right) shows a mean $\mu[T_{LSB,r}] = 8.72ns$, with a standard deviation $\sigma[T_{LSB,r}] = 1.65ns$. Therefore, the VCDL will tolerate input-referred offset within $\pm 3\sigma$ confidence.

5.5.4 Asynchronous Logic

Compared to the traditional synchronous scheme, the asynchronous conversion scheme eliminates idles times between conversion steps, effectively reducing conversion time in each step and saving overall static power consumption. The Asynchronous Logic replaces

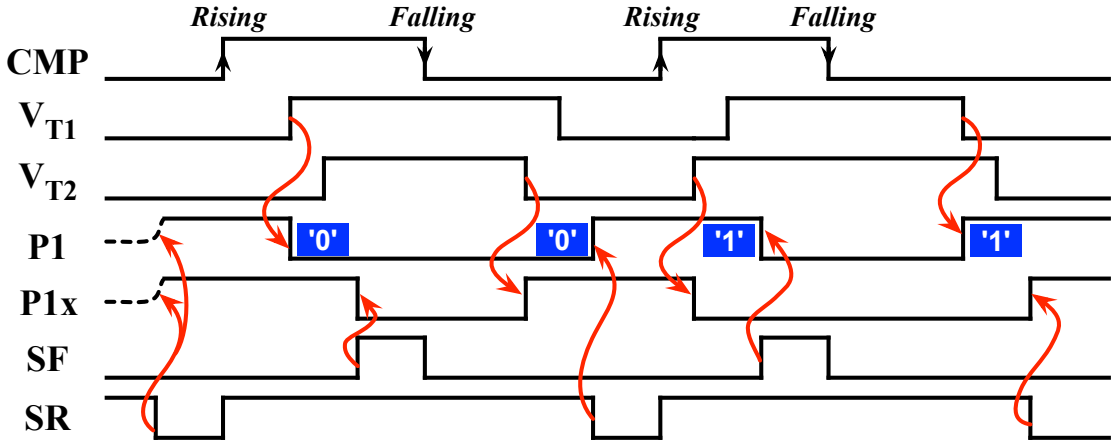


Figure 5.24: Timing diagram of 2-input PD signals with an output sequence of '0011'.

Table 5.6: Interpolation of 2b comparison results based on TDC input voltage amplitude and output delay signals

ΔV_1	$\Delta V_2'$	VCDL Rising-Edge Delays	P1	P2	**DH**	**DL**
> 0	> 0	$T1 > T3 > T4 > T2$	1	1	**1**	**1**
> 0	< 0	$T3 > T1 > T2 > T4$	1	0	**1**	**0**
< 0	< 0	$T3 > T2 > T1 > T4$	0	0	**0**	**1**
< 0	> 0	$T2 > T3 > T4 > T1$	0	1	**0**	**0**

the internal high frequency synchronization clock in a conventional SAR ADC implementation and oversees the ADC's operations. As have been indicated in Fig. 5.5 (repeated here as Fig. 5.27), the 2b/step conversion process is regulated by the asynchronous logic signals *READY*, *CMP*, *REG*, and *SLEEP*. Fig. 5.28 contains the digital logic circuits for control signal generation. In the *READY* signal circuit in (a), the header and footer transistors MP and MN control the output to rise or fall based on the current comparison edge

Table 5.7: VCDL delay and governing transistors in rising and falling comparisons

Quantity	Description	Transistors determining response
$t_{dr1}(\Delta V_{in})$	Rising-edge delay of VCDL1	Red transistors in VCDL1
$t_{df1}(\Delta V_{in})$	Falling-edge delay of VCDL1	Blue transistors in VCDL1
$t_{dr2}(-\Delta V_{in})$	Rising-edge delay of VCDL2	Red transistors in VCDL2
$t_{df2}(-\Delta V_{in})$	Falling-edge delay of VCDL2	Blue transistors in VCDL2

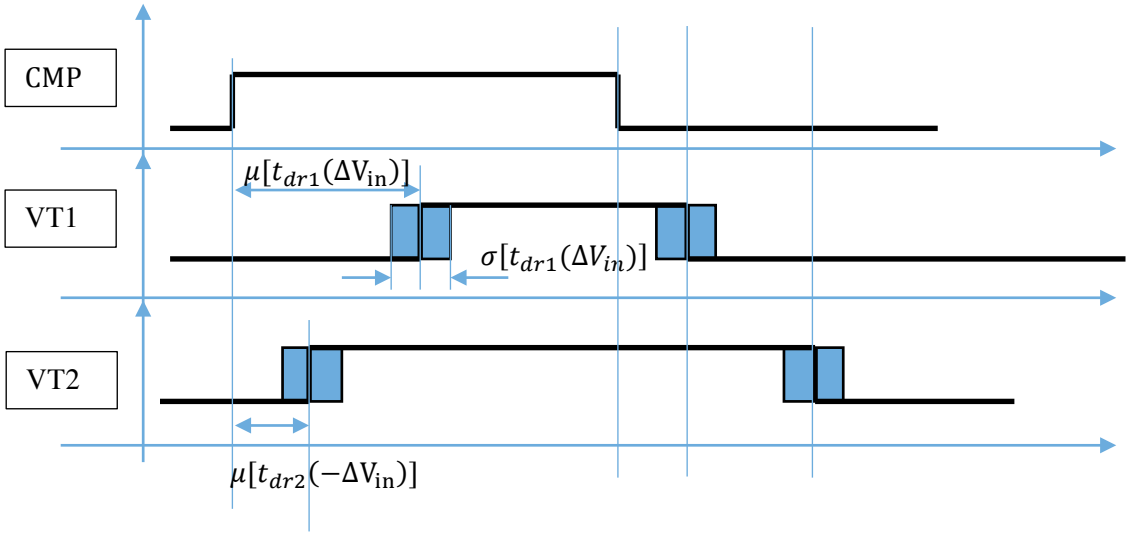


Figure 5.25: VCDL delay mismatches.

CMP. Parallel transistors M1A||M1B and M4A||M4B take the 2-input PD outputs *P1* and *P1x* such that when either signal makes a transition, a conduction path to the output will be created. Transistors M2A||M2B and M3A||M3B function in the same manner with signals *P2* and *P2x*. When the 2b comparison is finished, both PDs make a transition on their outputs, leading to a toggle action on the *READY* signal. In this way, completion of comparisons can be quickly and reliably captured.

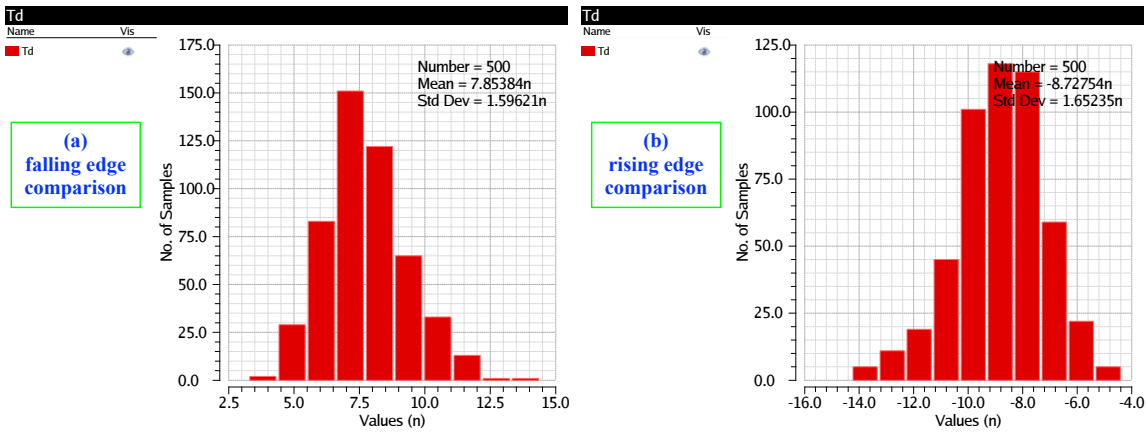


Figure 5.26: Monte Carlo simulation results on VCDL delay mismatches: (a) falling edge comparisons, (b) rising edge comparisons.

Delayed versions of *READY* (*RDY1* and *RDY2*) are utilized to generate *CMP*, *REG* and PD control signals *SR* and *SF*, as indicated in (b) and (c) of Fig. 5.28. To ensure proper DAC settling before the *CMP* signal edge occurs, we used R1, C1, R2, C2 to track the DAC's RC delay. In the layout, R1 and R2 are both 4X DAC unit resistance R_u; C1 and C2 track C_{bpsh}, and both are bottom-plate capacitances of 1.25X C_{SH} capacitors. Post-layout simulation shows a total tracking delay of $7\tau_{DAC}$ plus roughly 25% margin. Energy consumption of the delay track circuit can be reduced by using smaller C1/C2 and larger R1/R2, but area overhead may be inflicted depending on the compactness of R_u compared to that of C_{SH}.

Fig. 5.29 shows the 2b shift register circuit, which is a modification of the classic 1b register [112] with added 2b-per-shift capability. The signal *START* (complementary to the sampling clock *CLKs*) initializes the shift register. After each comparison, signal *REG* clocks the shift register to store the 2b result and generate the next digital code. When all

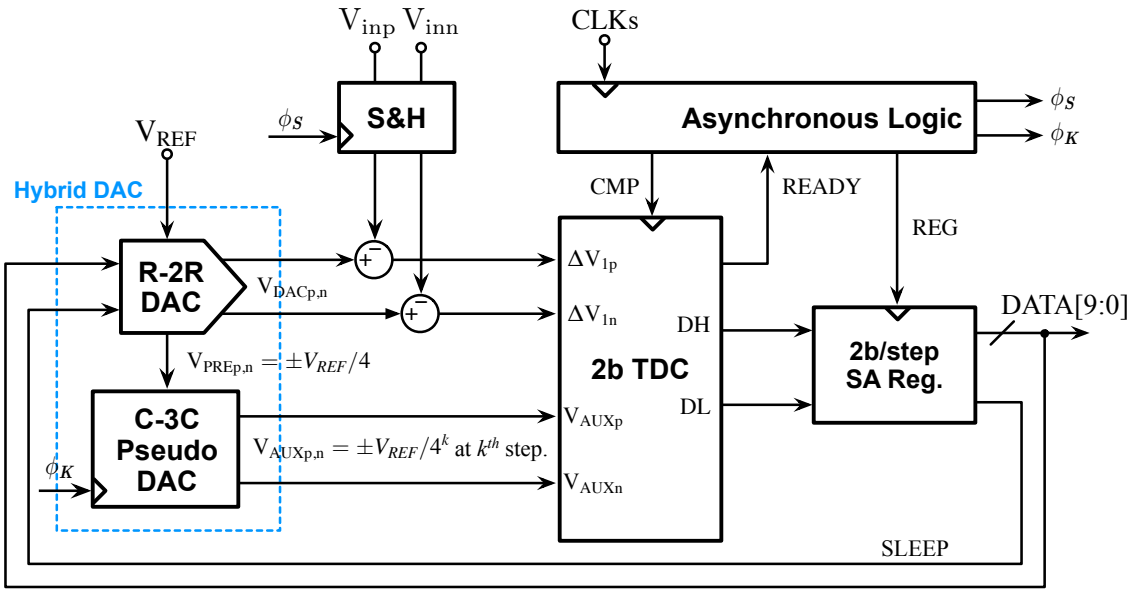


Figure 5.27: Architecture of the proposed asynchronous 2b/step SAR ADC.

5 steps or 10 bits have been resolved, the register shifts to its 6^{th} D flip-flop and activates the *SLEEP* signal to power down the entire ADC.

5.6 ADC Measurement

5.6.1 Measurement Setup

Fig. 5.30 shows the measurement setup for testing the fabricated ADC chip. The sampling clock *CLKs* is generated by the Agilent 81110A Pulse/Pattern Generator. The sinusoidal input signal is generated by the Stanford Research SRS DS360 Low-Distortion Function Generator. The digital output data of the ADC are read and stored by the Agilent 1670G Logic Analyzer. The performance of the ADC, e.g. SNDR, SFDR, INL, and DNL, are obtained via post-process using a PC. A dedicated testing PCB, shown in Fig. 5.31, is designed bearing the ADC chip together with power supply connections and bias circuits.

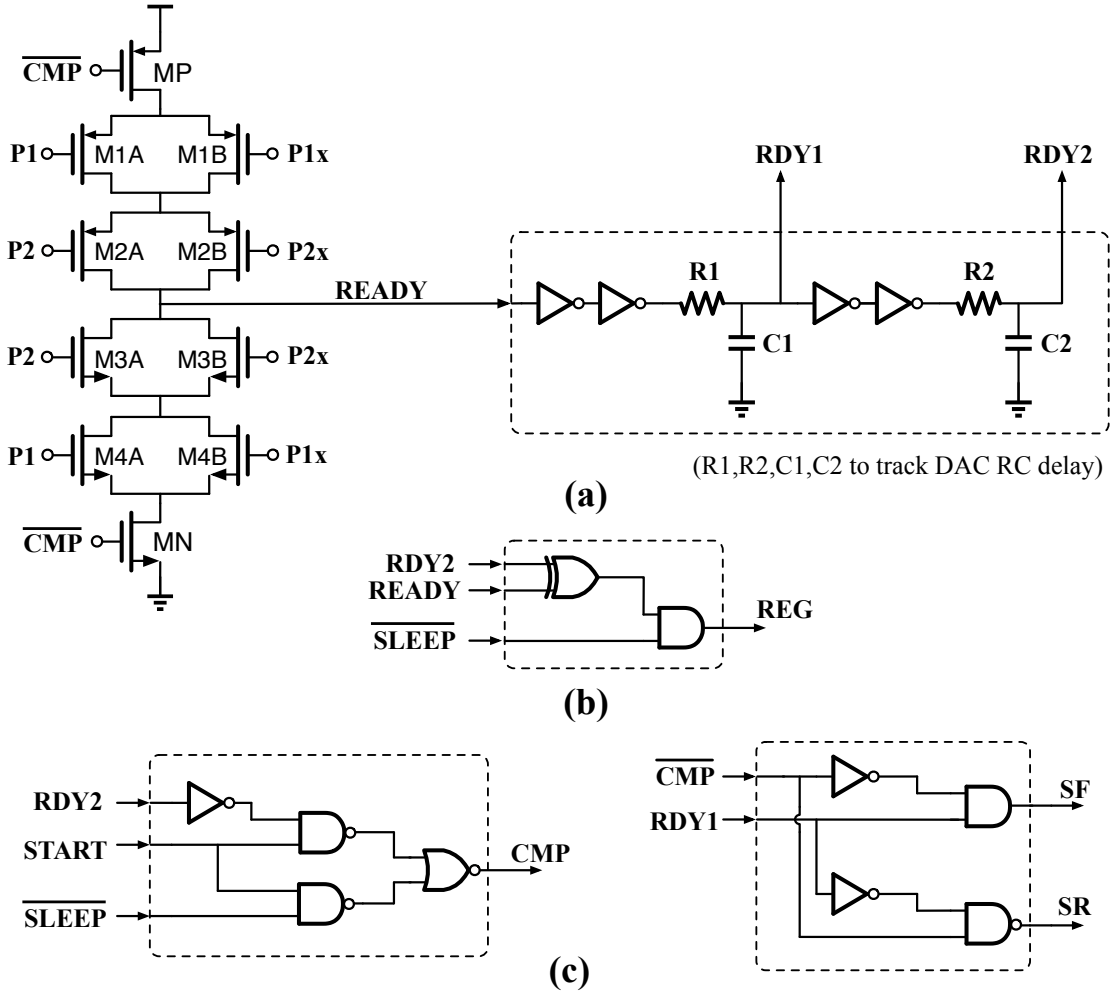


Figure 5.28: Asynchronous signal generations: (a) comparison *READY* signal, (b) shift register clock *REG*, and (c) TDC clock *CMP* and controls *SR* and *SF*.

The motherboard included biasing circuits and input signal ports, and the the daughter-board (to be mounted on the motherboard via a custom socket) accommodates the sample IC chips. This PCB configuration facilitates the multi-sample measurement process.

The prototype ADC with proposed ultra-low power design strategies are designed and fabricated in standard 0.18-μm CMOS technology. The chip micrograph is shown in

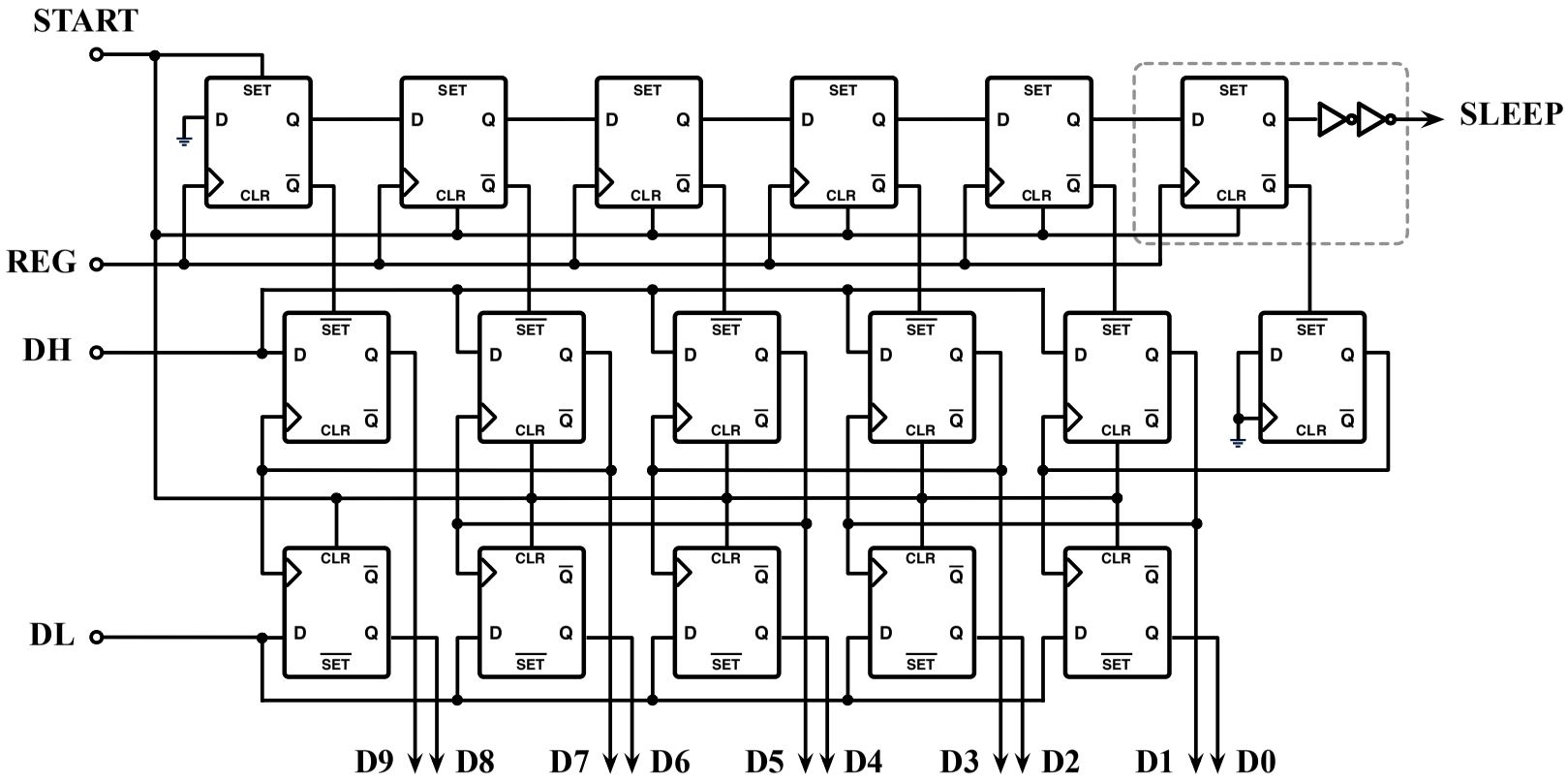


Figure 5.29: 2b shift register implementation and *SLEEP* signal generation.

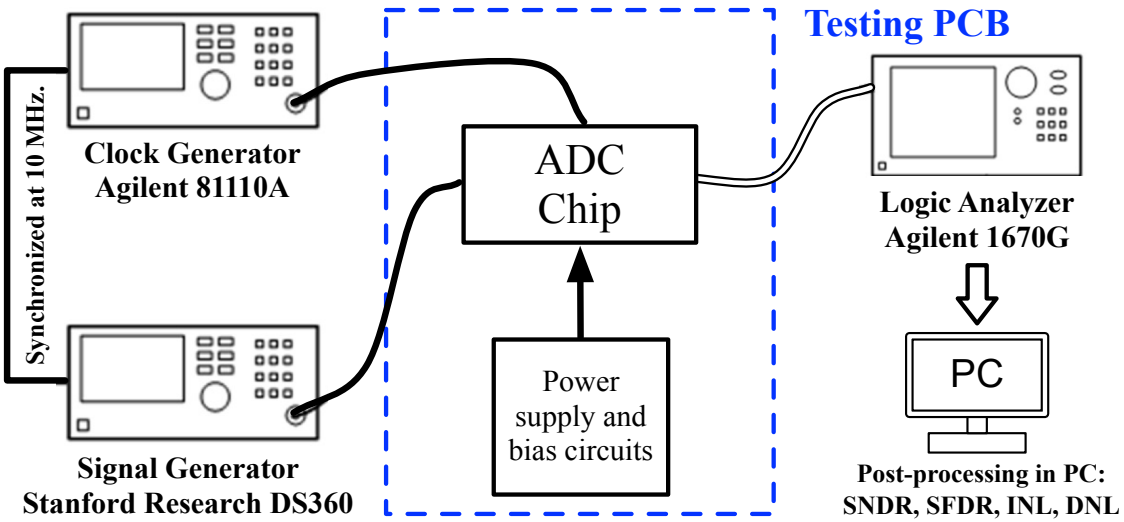


Figure 5.30: ADC measurement setup.

Fig. 5.32 with an active area of 0.077 mm^2. The 1.5 mm $\times$ 1.5 mm die is packaged in a 0.5-mm pitch QFN package. A total of 6 chips were measured. The chips were tested with a 0.6-V supply voltage for both digital and analog circuits. V_{REFp} and V_{REFn} are 0.6 V and ground, respectively, with V_{CM} at 0.3 V. The input differential signal swing is rail-to-rail at 1.2 Vpp, and is generated by Stanford Research DS 360 Signal Generator.

5.6.2 ADC Metrical Definitions

Differential Nonlinearity (DNL): DNL is a measure of code width uniformity within the ADC's input range. The width of ADC's output code k is calculated as the difference between the transition voltages for code k and $k+1$. For an ideal ADC, all output codes should have equal width of $V_{LSB} = V_{FSR}/2^N$, where V_{FSR} is the full-scale input range

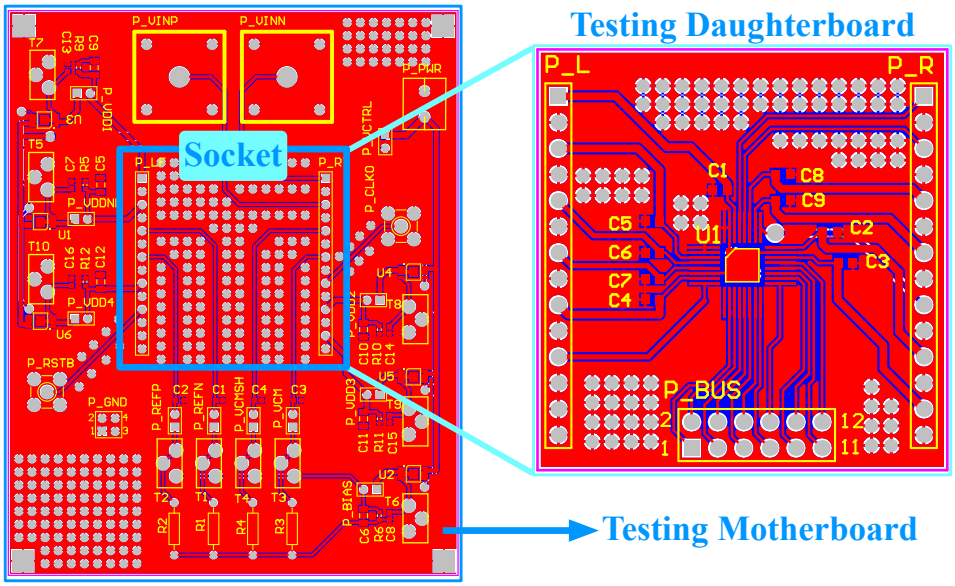


Figure 5.31: PCB design for testing the ADC prototype chips.

and N is the resolution of the ADC. The DNL error of output code k is defined as:

$$DNL(k) = \frac{V_{k+1} - V_k}{V_{LSB}} - 1, \text{ where } 1 < k < 2^N - 2. \tag{5.19}$$

which is the difference between its actual/measured width V_k and the ideal width V_{LSB}, in units of V_{LSB} or simply LSB. Fig. 5.33 shows an example of an input-output transfer curve of a 3-bit ADC. The offset and gain error are calibrated and removed so that the first and last code transitions are places in their ideal location. Apparently, the DNL of first and last code are not defined based on Eq. (5.19). In a monotonic ADC, the value of DNL $= 0$ indicates an ideal transition, while the value of DNL $= -1$ indicates missing code, as demonstrated by code 5 in Fig. 5.33.

DNL specifications are often spoken in terms of the minimum/maximum values across

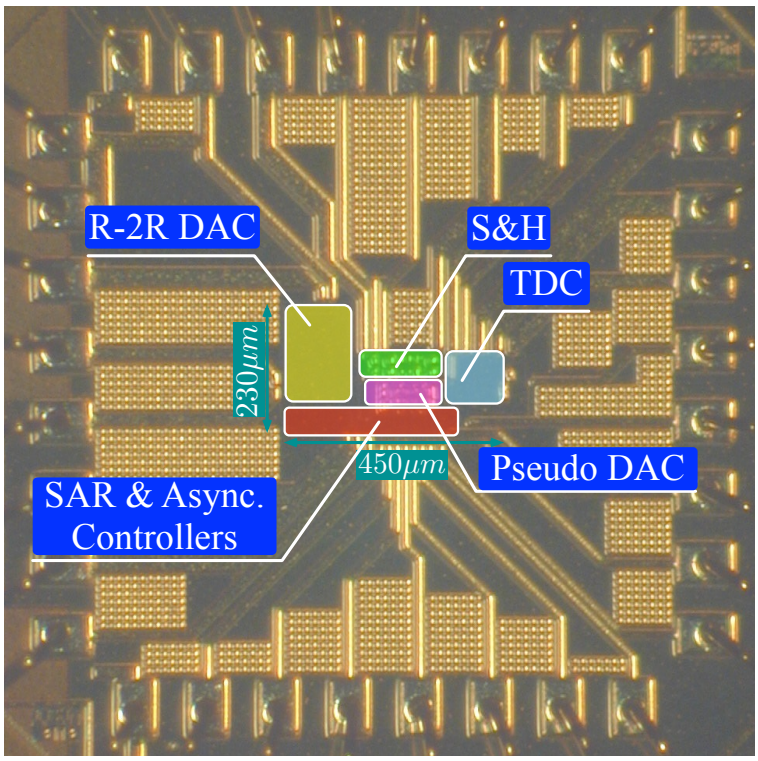


Figure 5.32: Die micrograph of the prototype ADC.

all codes, e.g. DNL $= +0.57/-0.89$ LSB means the ADC bears a minimum DNL error of $+0.57$ LSB and a maximum DNL error of -0.89 LSB. The presence of noise and spurious components along with quantization errors contributes to higher DNL values and limits the ADC's effective resolution.

Integral Nonlinearity (INL): INL error is described as the deviation, in LSB or percent of V_{FSR}, of an actual transfer curve from the ideal transfer function at certain code transitions. As indicated in Fig. 5.33, the magnitude of an INL(k) depends directly on the k^{th} code transition voltage, i.e. INL$(3) = V(3)_{ideal} - V(3)_{actual} = 0.5$ LSB. After gain error and offset calibration, it is obvious that both INL(0) and INL(7) are equal to 0. It can

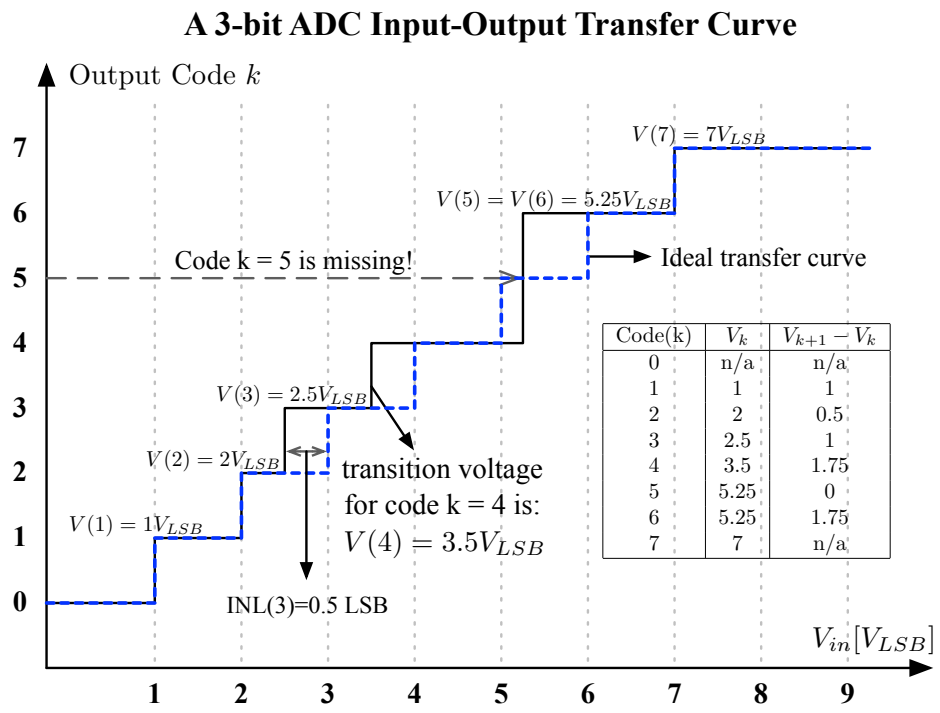


Figure 5.33: Illustrations of INL and DNL based on a 3-bit ADC's input-out transfer curve.

be shown that INL can be expressed as:

$$INL(k) = \sum_{i=1}^{k-1} DNL(i) \tag{5.20}$$

Therefore, once DNL values are computed, INL values can be easily found using a cumulative sum operation on the DNL vector. DNL indicates local linearity behavior of the ADC, while INL reveals overall linearity performance. The combination of DNL and INL often tells ADC architectural details such as major transitions due to specific operations or component mismatches, therefore are extremely useful ADC metrics.

SNDR: The SNDR, or Signal-to-Noise-Distortion Ratio, is the most important dynamic performance specification for an ADC defined as $SNDR = \frac{P_{signal}}{P_{signal}+P_{distortion}+P_{noise}}$. It depends on the overall resolution and entails specifications including linearity, distortion, clock glitches, noise, and settling time. It is normally calculated for a sine wave input with a maximum (or very close to maximum) amplitude, and is a function of signal frequency.

SFDR: The SFD, or Spurious Free Dynamic Range, is another important ADC dynamic specification. It is defined as the ratio between the maximum signal component and the largest distortion component. ADCs with low distortions or good integral linearity usually give an SFDR that is larger than the SNR performance.

ENoB: The ENoB, or Effective Number of Bits, is a specification that indicates the ADC's effective resolution. Due to the presence of noise, distortion, clock glitches, etc, the resolution of an ADC normally suffers and degrades from its nominal resolution. The ENoB is directly related to SNDR and can be calculated as:

$$ENoB = \frac{SNDR - 1.76 \text{ dB}}{6.02} \tag{5.21}$$

Therefore, the ADC's effective resolution drops 1 bit for every 6-dB degradation in its SNDR specification. For instance, for a nominal 10-bit ADC that achieves 58.3 dB SNDR performance, its actually achieved resolution is equal to 9.4 bits.

FoM: Energy efficiency is a very important specification of an ADC especially for ultra-low power applications. It is measured by the Figure-of-Merit, or FoM, which is

formulated according the following equation

$$FoM = \frac{P_{ADC}}{2^{ENoB} \times f_s} \tag{5.22}$$

where P_{ADC} is the total ADC power consumption, ENoB is the ADC's effective number of bits, and f_s is the sampling rate. In essence, the FoM is a power measure normalized to sampling rate and resolution, and is a manifest of energy consumption needed to effectively each bit of resolution. Therefore, it is possible to compare energy efficiency among ADC's with different architecture, resolution, and speed via this FoM specification.

5.6.3 Measurement Results

The static linearity performance was tested using the code density method. A sampling rate of 100 kS/s and an input sinusoid signal of 1.010 kHz were used. A total of one million samples were collected for each run. Fig. 5.34 shows the differential nonlinearity (DNL) and integral nonlinearity (INL) of the ADC output. The maximum DNL and INL measured are +0.50/-0.26 LSB and +0.89/-0.82 LSB, respectively.

The ADC's dynamic performance is measured using single tone testing. Fig. 5.35 shows the Fast Fourier Transform (FFT) spectra of the ADC output with both 1.010 kHz and 47.00 kHz full-scale sinusoidal inputs, each sampled at 100kS/s. The average SNDR and SFDR measured are 57.2 dB and 66.8 dB, respectively, for the 1.010 kHz signal. The ADC achieved an ENoB (effective number of bits) of 9.2 bits. In Fig. 5.36(a), the measured ENoB is plotted over a series of input signals with different frequencies, all

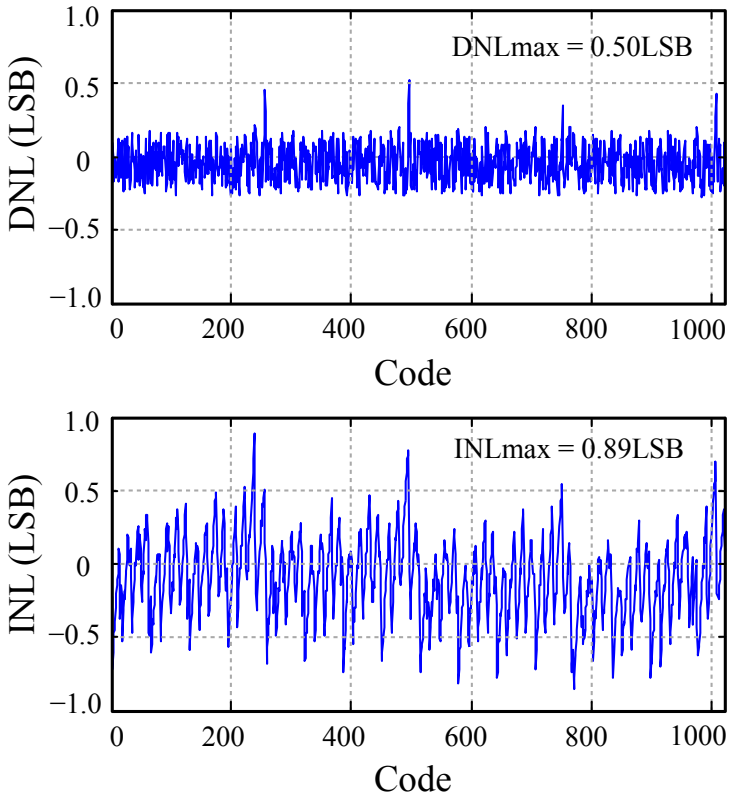


Figure 5.34: Measured DNL and INL errors.

sampled at 100 kS/s.

At a supply voltage of 0.6 V and sampling rate of 100 kS/s, the ADC consumes a total power of 390 nW, with 5.8 nW leakage power in sleep mode. As illustrated in Fig. 5.37, a detailed breakdown shows that 27% of total energy is consumed by the R-2R DAC, 13% by its drivers, 5% by the C-3C pseudo DAC, 14% by the TDC (11.7% in VCDL and 2.3% in PD), 36% by digital logic, and 5% by S&H. Our 2b/step technique reduced the digital-switching power by 110 nW (28% of total ADC power), while the dual-edge-comparison technique and the absolute-value comparison scheme saved 46 nW (11% of total ADC

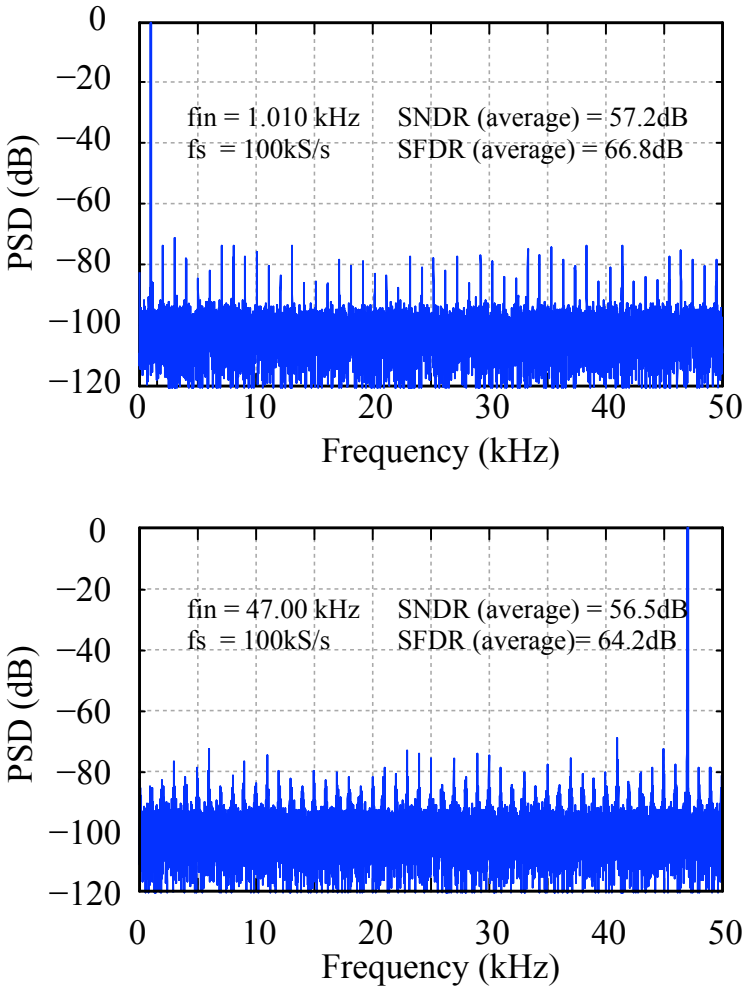


Figure 5.35: Measured 8,192-point FFT spectra of ADC output with (a) 1.010 kHz and (b) 47.00 kHz full-scale input signals.

power) and 27 nW (7% of total ADC power) in TDC power, respectively.

The FoM of the ADC is calculated based on its power consumption, effective resolution, and sampling rate. Fig. 5.36(b) shows the FoM and power at different sampling rates. The power consumption scales uniformly to sampling rates thanks to the asynchronous scheme. Performance and power variations among measured chips are shown in Fig. 5.38.

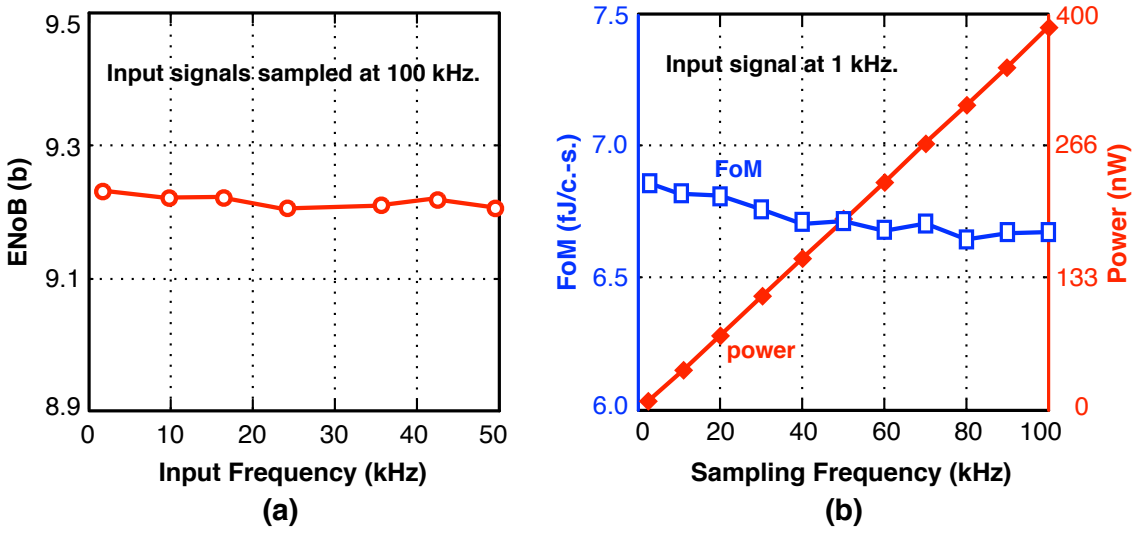


Figure 5.36: Measured results: (a) ENoB versus input frequencies and (b) power and FoM versus sampling frequencies. All input signals are at full-scale amplitude.

The ADC achieves an average FoM of 6.7 fJ/conversion-step, which proves the effectiveness of the low-energy design strategies.

It is expected that implementing the proposed approach in newer technologies would further improve ADC efficiency. To compare overall energy efficiency with ADCs designed in different technology nodes, it is necessary to consider the process scaling impact on energy consumptions. According to the discussions in [113], the power consumptions of matching limited and digital circuits scales at a rate of $1/S^2$, and that of noise-limited circuits scales at a rate of S. Here S is the technology scaling factor, e.g. scaling from 180nm to 90nm, S = 180nm/90nm = 2. For the proposed SAR ADC architecture in particular, we can make the following assumptions:

1. The $1/S^2$ factor applies to the digital asynchronous SAR logics, the DAC drivers

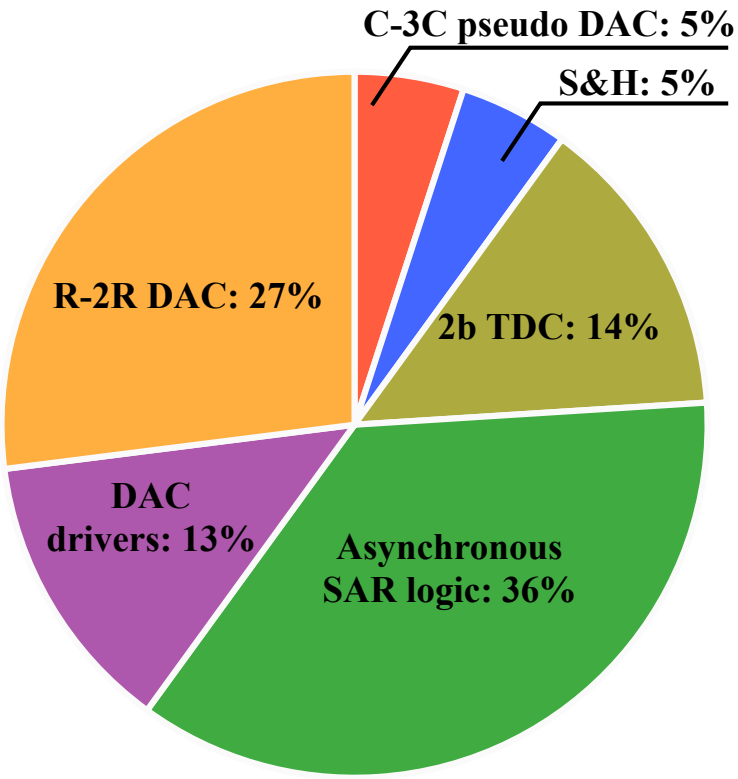


Figure 5.37: ADC energy consumption breakdown.

(large inverters), and the C-3C and S/H capacitors (limited by matching and gate parasitic caps).

2. For the TDC: its not straightforward to predict with a first order approach: reduced device size lead to lower power and faster comparison time, but input referred offset/noise demand the same device size/time delay to maintain the LSB timing for 10b. Thus it is fair to consider its power to be unchanged.
3. For the R-2R DAC: although it is matching limited in terms of linearity, its power and resistance value is limited by the amount of time budget available for settling in this time-based topology. Although faster digital circuits in advanced technologies

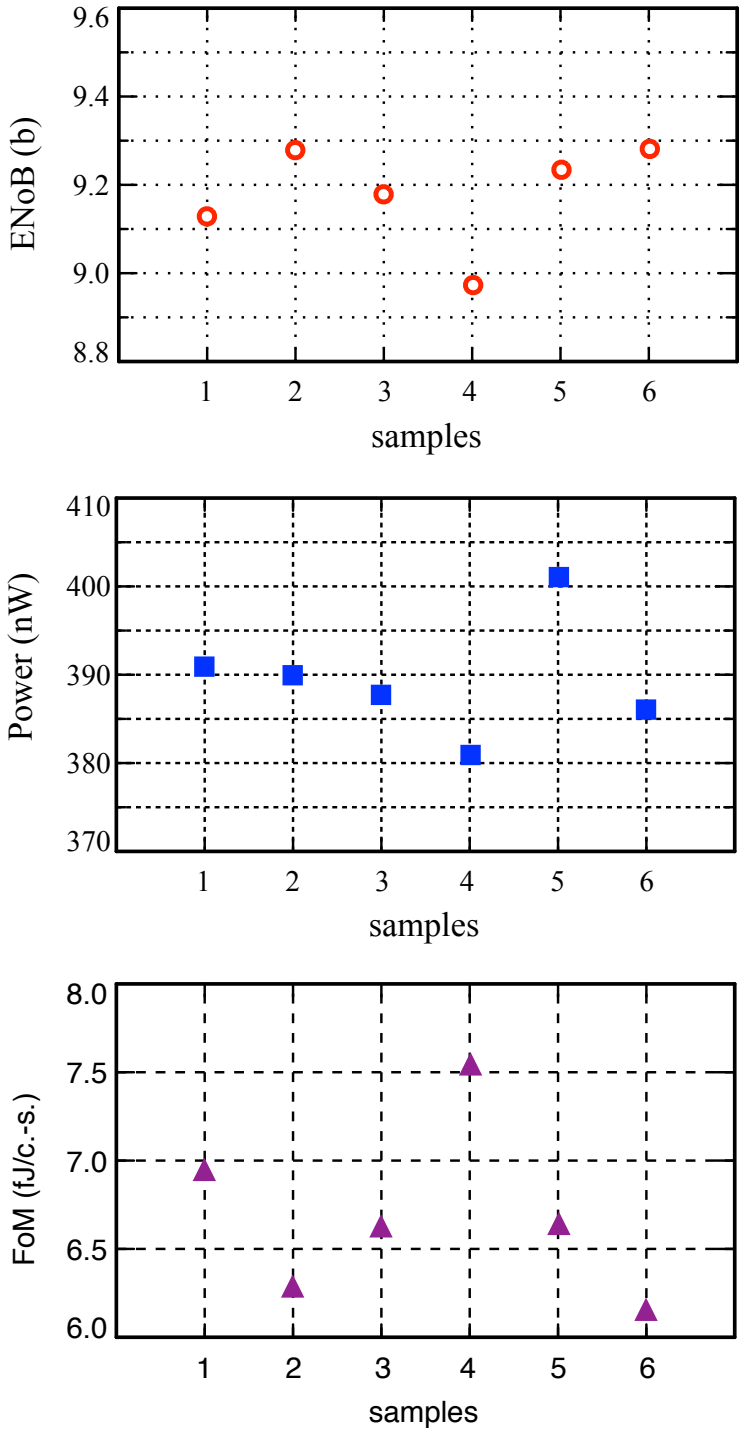


Figure 5.38: ENoB, power, and FoM variations among measured chips.

will provide extra timing that will lead to lower power, we conservatively predict the R-2R DAC power to stay constant at a given sampling rate.

With the above remarks, Table 5.6.3 summarizes the predictions of the ADCs energy efficiency at different technology nodes. As indicated in the table, we estimate the FoM to roughly halve from 6.7 fJ/conversion-step to 3.3 fJ/conversion-step when scaled to 65nm process from the current 180nm process. Thus, we feel that our approach provides energy-saving benefits on par with state-of-the-art SAR architectures when process scaling benefits are taken into account.

Table 5.8: ADC power consumption scaling and efficiency predictions in various technologies

Technology node	180nm	130nm	90nm	65nm
Scale factor S	1.00	1.38	2.00	2.77
Power factor $1/S^2$	1.00	0.52	0.25	0.13
C-3C, S/H power	39 nW	20 nW	9.8 nW	5.1 nW
SAR logic power	140 nW	72.8 nW	35.0 nW	18.2 nW
DAC driver power	50 nW	26 nW	12.5 nW	6.5 nW
Comparator power	55 nW	55 nW	55 nW	55 nW
R-2R DAC power	105 nW	105 nW	105 nW	105 nW
ADC total power	390 nW	279 nW	217 nW	190 nW
ADC FoM	6.7 fJ/c.-s.	4.8 fJ/c.-s.	3.7 fJ/c.-s.	3.3 fJ/c.-s.

Table 5.9 summarizes the performance of the tested ADC, along with previous works from literature for comparison purposes. The ADC achieves an overall energy efficiency (FoM) of the 6.7 fJ/conversion-step, consisting roughly 70% of dynamic energy and 30%

of static energy. In more advanced technologies, the proposed 2b/step time-based topology is expected to achieve even higher efficiencies for two main reasons. First, smaller device size will lead to reduced dynamic power, especially in the digital logic and DAC drivers. Secondly, faster circuit operation will reduce ADC active time and provide extra time budget for the resistive DAC to settle, allowing larger R_u and lower static power. In addition, this architecture is also capable of saving power on a system level, e.g., in a biomedical front-end, since the asynchronous processing technique eliminates the need of a clock generator for the fast internal synchronization clock. Fig. 5.39 illustrates the ADC's FoM-Speed plot based on survey data presented on Dr. Boris Murmman's website [114]. This plot clearly shows that the proposed architecture offers a leading energy efficiency performance among all other implementations.

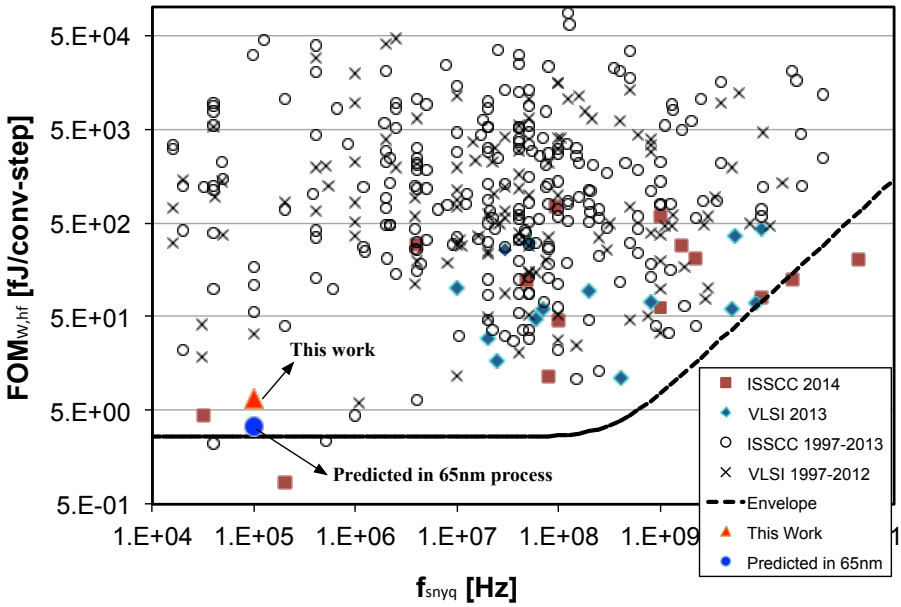


Figure 5.39: ADC survey data plot. Envelope is derived using the average of 5 best data points found in the survey pool.

5.7 Conclusion

This chapter presented an energy efficient asynchronous SAR ADC based on a R-2R/C-3C hybrid DAC. The ADC achieved 9.2-bit of resolution, and a FoM of 6.7 fJ/conversion-step at a sampling rate of 100 kS/s. The 2b/step technique reduces both active conversion time and total switching activities in the DAC and the SAR logic circuits by 50% thereby significantly saving both static and dynamic energy consumption. The hybrid DAC reference scheme and time-domain interpolation technique greatly reduce circuit and energy overhead for 2b/step conversion. The dual-edge-comparison technique provides additional savings in dynamic energy. The proposed architecture entails valuable strategies for trading excess circuit speed and timing for higher energy efficiency, e.g. it enables DAC energy scaling at reduced sampling rates. As supported by the power consumption analysis, with roughly 70% of digital switching power at the current technology node, it is expected that the proposed asynchronous 2b/step time-domain architecture will accrue even greater benefits in newer, faster, smaller-feature-sized technologies.

Table 5.9: ADC performance summary and comparisons

	[115] ISSCC'14	[94] JSSC'13	[84] JSSC'12	[83] ISSCC'13	[92] ISSCC'13	[98] VLSI'12	[93] ESSCIRC'12	[96] ISSCC'14	[86] JSSC'11	**This work**
Technology	40nm	40nm	40nm	65nm	90nm	90nm	65nm	180nm	180nm	180nm
Supply (V)	0.45	0.5	0.5	0.6	0.4	0.35	0.7	0.6	0.6	0.6
Fs (S/s)	200k	1k	1.1M	40k	500k	100k	1k	16k	100k	100k
Bit/step	1b	1b	1b	1b	1b	1b	1b	1b	1b	2b
DNL (LSB)	0.44	0.36	1.4	0.32	0.34	0.30	0.55	0.10	0.70	0.50
INL (LSB)	0.45	0.44	1.1	0.48	0.62	0.60	0.61	0.20	0.80	0.89
ENoB (bit)	8.9	8.2	7.5	9.4	8.7	9	9.1	9.7	9.3	9.2
Power (W)	84n	1.9n	1.2μ	72n	500n	170n	3n	170n	1.3μ	390n
Area (mm^2)	0.0065	0.013	0.011	0.076	0.042	0.032	0.037	0.120	0.125	0.103
FoM (fJ/c-s)	0.85	6.1	6.3	2.7	2.4	3.2	5.5	20	21	6.7

6. CONCLUSIONS

6.1 Research Summary

This research work proposed a miniaturized in-home sleep apnea monitoring device with the intention of providing a more viable diagnosis method for people with potential sleep apnea conditions. The system level architecture of the monitoring device is proposed based on extensive literature review on the pathology of sleep apnea, the medical definition of apnea events, and recommended diagnostic methods and standards by several organizations specialized in sleep medicine including AASM (American Academy of Sleep Medicine) and ASDA (American Sleep Disorders Association). The system contains one signal path for hardware-based automatic apnea detection using the proposed algorithm, and the other signal path for breathing waveform recording via an low-power analog-to-digital converter for post-study analysis.

The proposed device uses a MEMS pressure sensor to measure breathing airflow as the input signal and a time-domain signal processing algorithm for sleep apnea event detection and scoring. The use of a MEMS pressure sensor allows breathing events (inhale and exhale) to be detected with much reduced interference and artifacts, which leads to reduced complexity in circuitry design. The proposed apnea detection algorithm together with analog signal conditioning circuitry is implemented in standard $0.5\mu m$ CMOS technology for validation. Based on this apnea detection chip, a prototype apnea monitoring device is designed and assembled with a commercial MEMS sensor, a commercial programable

platform and a wireless transceiver.

An low-power analog-to-digital converter is essential in a biomedical device for recording analog physiological signals and accessing sophisticated digital signal processing. This dissertation presented an energy efficient ADC suitable for biomedical applications. The proposed ADC adopts an asynchronous successive approximation register (SAR) architecture and processes 2 digital bits per conversion step. The 2b/step conversion technique reduces both active conversion time and total switching activities in the DAC and the SAR logic circuits by 50% thereby significantly saving both static and dynamic energy consumption. The ADC relies on a R-2R/C-3C hybrid DAC for reference levels required 2b-per-step conversion. The hybrid DAC reference scheme, together with a novel time-domain interpolation technique greatly reduce circuit and energy overhead needed for 2b/step conversion in DAC and comparator design. The dual-edge-comparison technique in the time-domain comparator provides additional savings in dynamic energy. The proposed architecture entails valuable strategies for trading excess circuit speed and timing for higher energy efficiency, e.g. it enables DAC energy scaling at reduced sampling rates. The ADC achieved an energy efficiency (FoM) of 6.7 fJ/conversion-step when converting at a sampling rate of 100 kS/s.

6.2 Future Work

To make the conceptual in-home sleep apnea monitoring device proposed in this work a reality, two main design steps are yet to be accomplished. The first step is to perform a thorough System-on-Chip (SoC) integration to include the MEMS pressure sensor, the

custom apnea detection and scoring circuitry, digital control circuit (including memory), and the wireless transceiver. The second step is to design the PCB to accommodate the apnea SoC, the battery and biasing circuitry, and nasal/oral cannula with proper fixtures and complete assembly to arrive at the target device format and footprint. To elaborate particular challenges in these steps:

1. Apnea SoC Integration: A high-level integration apnea SoC will significantly reduce the footprint of the apnea monitoring device since the total number of IC chips needed for the system is reduced. To realize the apnea SoC, a special semiconductor design technology is required to fabricate the MEMS pressure sensor on the same die as the signal processing integrated circuitry. An alternative, and potentially cheaper, approach would be multi-chip packaging to have separate sensor die and signal processing IC die. In either cases, a challenge will arise as to how to design a proper air-tight cavity for the SoC packaging with air inlet port in order to have accurate breathing airflow pressure measurement. A more straightforward design would be using a small-sized commercial MEMS sensor chip together with the apnea detection chip, but this is obviously more bulky in terms of device size. To evaluate the aforementioned approaches for a best design decision, one would have to weigh the total design time and cost, achievable device size, and device performance to find a reasonable balance.
2. Apnea Device Assembly: To make an apnea device that can be comfortably affixed on the patient's facial area, it is necessary to mount all electronics and other compo-

nents on a flexible PCB design to accommodate the curvatures of the human face. Medical-grade adhesives should be used to guarantee no irritation will be caused when the device is applied on the facial skin. A nasal/oral cannula should also be properly designed to connect with the pressure sensor port and channel the patient's breathing airflow from both nose and mouth. The selection of battery as the device's power supply represents another design challenge. First of all, it's output voltage should be high enough to at least drive the low-dropout (LDO) voltage regulator. Secondly, the physical size of the battery should be large enough to have the capacity to last for at least one test session, and at the same time should be small enough to achieve a small overall device size. Of course, the actual battery capacity should depend on whether the device is design to work for one study session only (i.e. as a disposable design) or for multi-use purposes.

Developing a medical diagnostic device requires a great amount of knowledge from various disciplines and encounters a myriad of challenges from various aspects. Aside from the aforementioned design challenges in this dissertation, the medical device is also subject to government (especially the Food and Drug Administration or FDA) regulations, industry standards, clinical practices, etc. Despite of the vast and appalling difficulties often involved in medical device development, researchers and designers like myself take great passion in this particular endeavor with the hopes for a better life and a better future for our humanity.

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