SINGLE-PHASE INVERTER AND RECTIFIER FOR HIGH-RELIABILITY APPLICATIONS

A Dissertation

by

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ABSTRACT

With the depletion of fossil fuels and skyrocketed levels of CO_2 in our atmosphere, Renewable Energy Resources, generated from natural, sustained, clean, and domestic resources, have caught the eye in recent years of both the industries and governments worldwide. In addition to finding these energy resources, new technologies are being sought to improve the efficiency of consuming the generated energy. Power Electronics is the key technology for both generation and the efficient consumption of energy. The recent trend in power electronics is to integrate the electronics into the source (Photovoltaic (PV)) or the load (light). For PV and outdoor lighting applications, this imposes a harsh, wide-range operating environment on the power electronics. Thus, the reliability of power electronics converters becomes a very crucial issue. It is required that the power electronics, used in such environments, have reliability indices, such as lifetime, which match with the source or load one. This eliminates the reoccurring cost of power electronics replacement. Relatively high efficiencies have been reported in the literature, and standards have been developed to measure it. However, the reliability aspect has not received the same level of scrutiny. In this study, two main aspects have been investigated: (1) A new methodology to evaluate the integrated power electronics that becomes more involved task; and (2) new topology and control schemes, for the single-phase DC/AC and AC/DC converters, which will improve the reliability. The proposed methodology has been applied for different PV Module-Integrated-Inverter (MII) that employs different power decoupling techniques. The results showed that the decoupling capacitor is the

limiting lifetime component in all the studied topologies. Moreover, topologies use film capacitor instead of electrolytic capacitor showed an order of magnitude improvement in the lifetime. This clearly suggests that replacing the electrolytic capacitor by a high-reliability film capacitor will enhance the reliability of the PV MII. In the second part of this study, the ripple-port concept is applied for the single-phase DC/AC inverter and AC/DC rectifier, which allows for the usage of the minimum required decoupling capacitance. In conclusion, film capacitor can be used, which led to the improvement of the overall reliability and lifetime.

DEDICATION

To

My Father; Mohammad and My Late Mother; Mariam

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1 INTRODUCTION

1.1 National energy and technical challenges

The Department of Energy (DOE) has identified a number of energy challenges that are necessary to upgrade into the future smart grid [1]. Figure 1.1 summarizes these challenges and illustrates how the field of Power Electronics has a very important role in bridging the gap between the national energy and the technology challenges that will eventually facilitate the transition into the future smart grid.

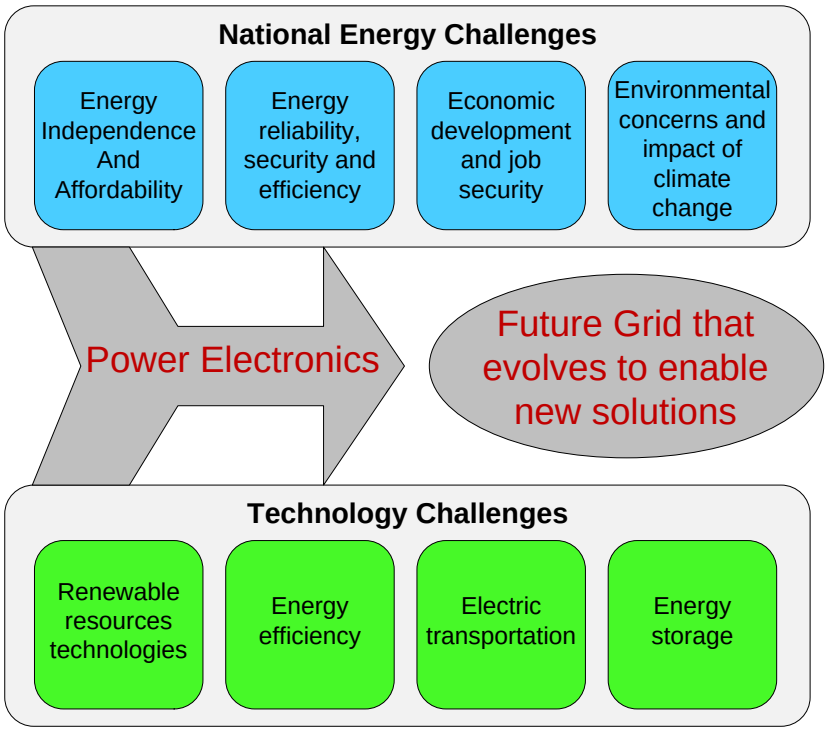
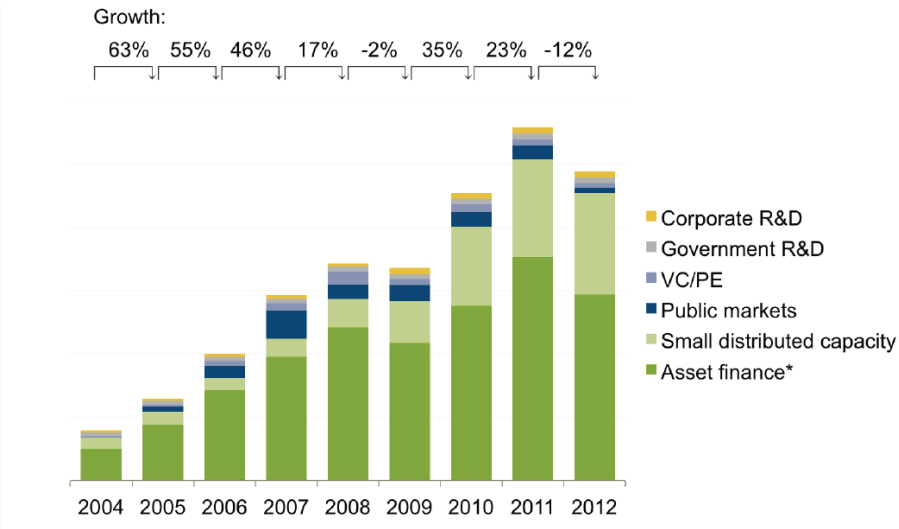


Figure 1.1: National energy and technology challenges

With the depletion of fossil fuels, renewable sources, generated from natural resources, have caught the eye in recent years from both the industries and governments worldwide due to their environmental friendliness, sustainability nature, economic benefits, and energy security. Figure 1.2 shows the investment growth in the Renewable Energy field during the last decade, which shows an exponential growth [2].



*Asset finance volume adjusts for re-invested equity. Total values include estimates for undisclosed deals
Source: UNEP, Bloomberg New Energy Finance

Figure 1.2: Global new investment in Renewable Energy by asset class, 2004-2012, [2]

In the United States, Renewable Energy counts for 11.2% of the total Energy production for 2012, as shown in Figure 1.3 [3]. Although Wind Energy and Solar Energy only count for 2% of the Renewable energy production, they are the two Renewable energy sources with the highest growing rate in the last decade, as show in Figure 1.4. Wind and

Photovoltaic (PV) Energy resources were the fastest growing technologies, as shown in Figure 1.4. In 2012, wind and PV energy have experienced 28% and 83% increment in cumulative installed capacity, respectively, in the US [3]. To meet the 2020 renewable energy targets of the European Union, the European Photovoltaic Industry Association (EPIA) recently estimated that the possible contribution of photovoltaic is up to 12% of the electricity supply by 2020.

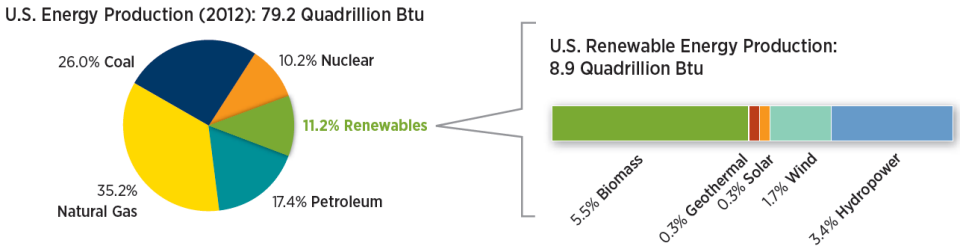


Figure 1.3: Energy production in US for the year of 2012, source: DOE [3]

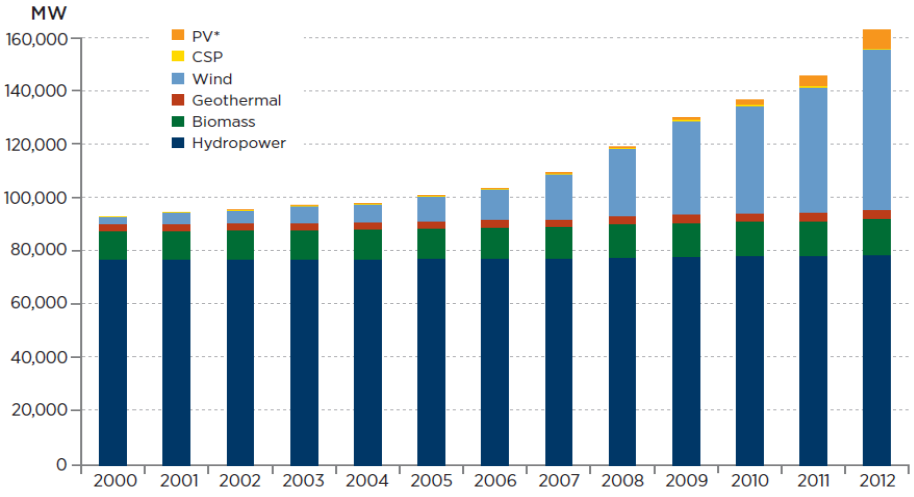


Figure 1.4: Renewable energy growth in US, source: DOE [3]

In 2012, more than 100 GW of PV are installed globally—an amount capable of producing at least 110 TWh of electricity every year [3]. Moreover, in Figure 1.5, new players have entered into the PV field. Figure 1.5 shows that United States and China have doubled and tripled, respectively, their PV installed capacity during the last three years [4].

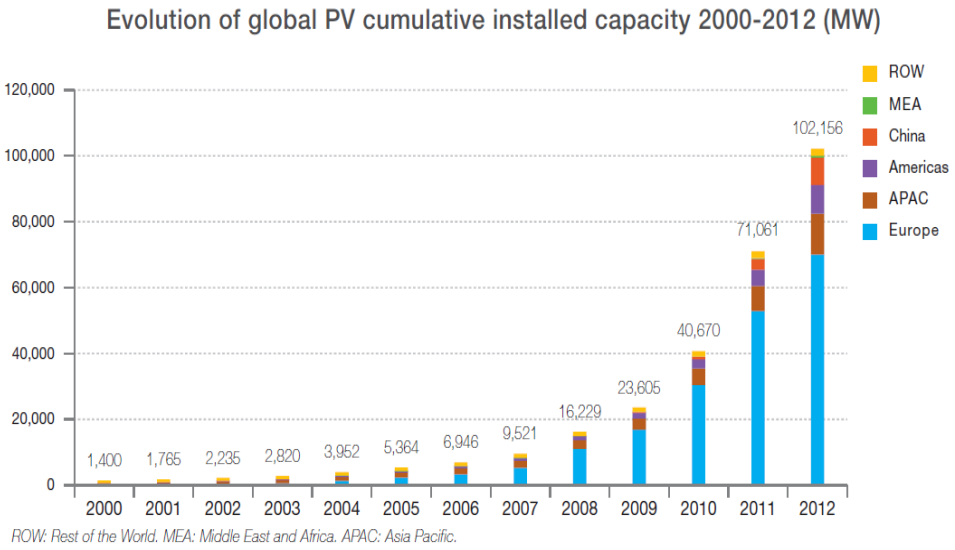


Figure 1.5: Evolution of global PV cumulative installed capacity, source: EPIA [4]

Figure 1.6 shows that grid-connected (AKA "grid-tie") PV systems represent the largest share of the market [5]. The Grid-connected PV system has become the trend in the past decade because no energy storage devices are needed. Energy storage devices have relatively low lifetime, and high cost.

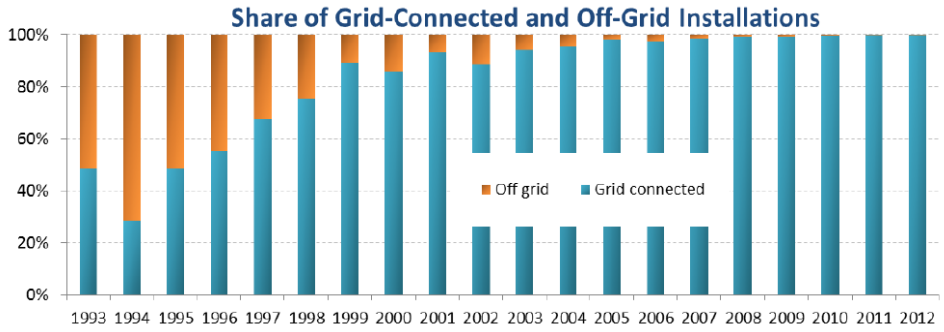


Figure 1.6: Share of grid-connected and off-grid PV installations, source: EPIA [5]

1.2 Photovoltaic system

1.2.1 Grid parity

In order for PV energy to become competitive with the conventional energy sources, its cost needs to decrease to what is called a "grid parity" point, where the cost of energy generated from PV equals the one generated from the conventional sources. Both governments and industry have been working on bringing the cost of the PV energy down rigorously. In the effort to address this crucial issue, the DOE has put a plan to bring the cost of the PV energy down. The "$1/Watt Electricity from Solar" plan aims to decrease the cost of energy from PV to $1/Watt in order for the PV energy to become a competitive energy source. PV technologies have experienced unprecedented developments and improvements since PV was first proposed in 1977. Figure 1.7 shows how the PV cell's price has been decreasing exponentially to $0.74/Watt in 2013 [6].

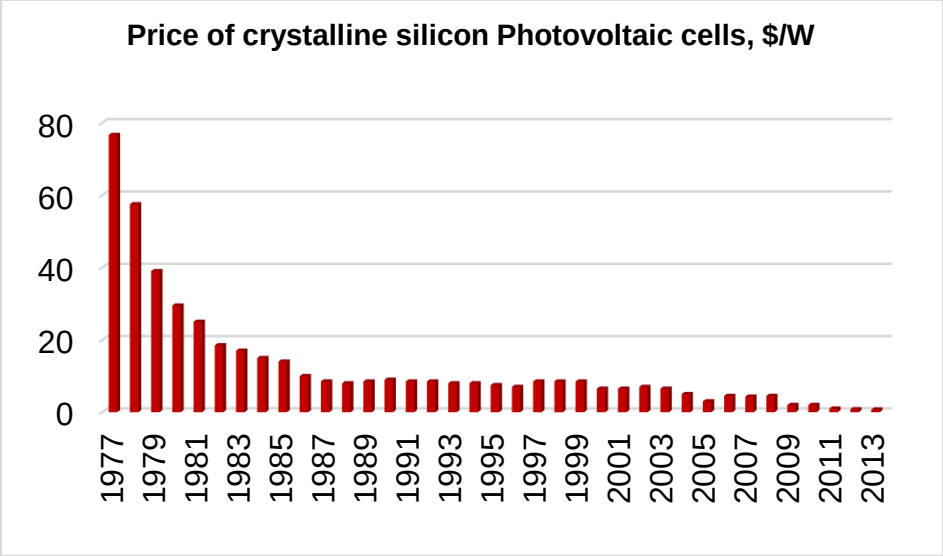


Figure 1.7: Price of Crystalline silicon photovoltaic cells, $/watt, source: Bloomberg New Energy Finance [6]

However, the PV module's cost approximately counts for about 50% of the total PV system's cost, as shown in Figure 1.8 [7]. The other 50% is due to the cost of the power electronics (DC/AC inverter) and the balance of system (BOS) components that are used to connect the PV source through the inverter into the AC load or the utility grid. Figure 1.8 shows that the cost of the BOS is almost 50%.

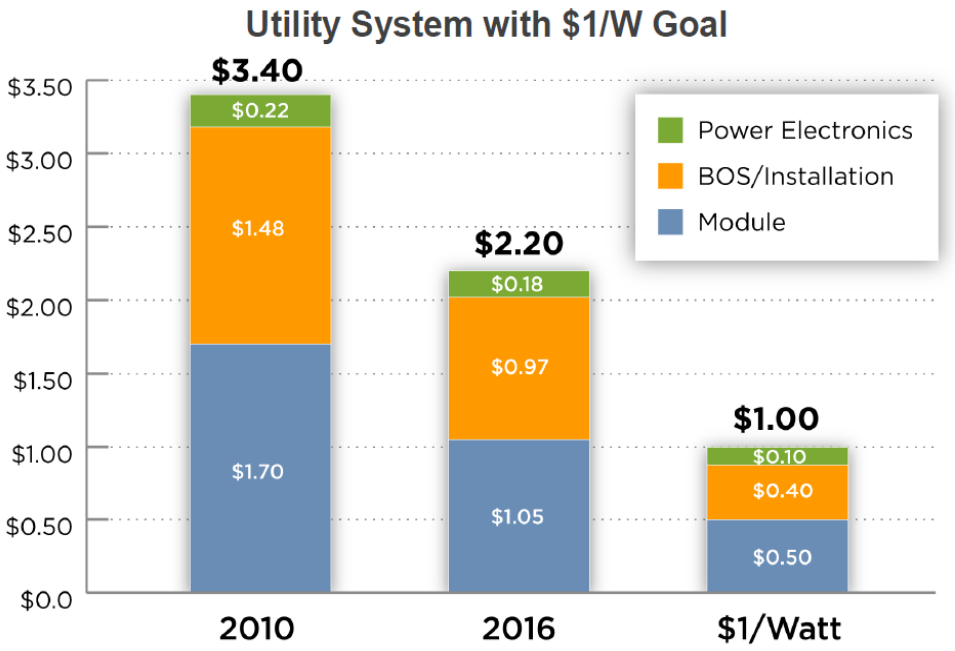


Figure 1.8: The Prospect for $1/Watt Electricity from Solar, source: DOE [7]

1.2.2 Photovoltaic system configurations

Grid-connected PV systems are categorized into three categories: centralized inverter, string inverter, and AC-Module "microinverter" [8-10]. Microinverter or Module-Integrated-Inverter (MII), with power levels ranging from 150W to 300W, has become the trend for grid-connected PV systems due to its numerous advantages including: improved energy harvest, improved system efficiency, lower installation costs, "Plug-N-Play" operation, and enhanced modularity and flexibility. However many challenges remain in the way of achieving low manufacturing costs, high conversion efficiencies, and long life span. Since MII is typically attached to the back of the PV module, and may be well integrated to the PV module back skin, it is desirable that the inverter has a lifetime that

matches the PV module one. It is well known that electrolytic capacitors are the limiting components that determine the lifetime of the microinverter [11]. The aforementioned advantages of the integration of the power electronics into the PV Module does not come for free, the reliability of the power electronics should match the PV module's one, namely 25 years [8, 9, 12].

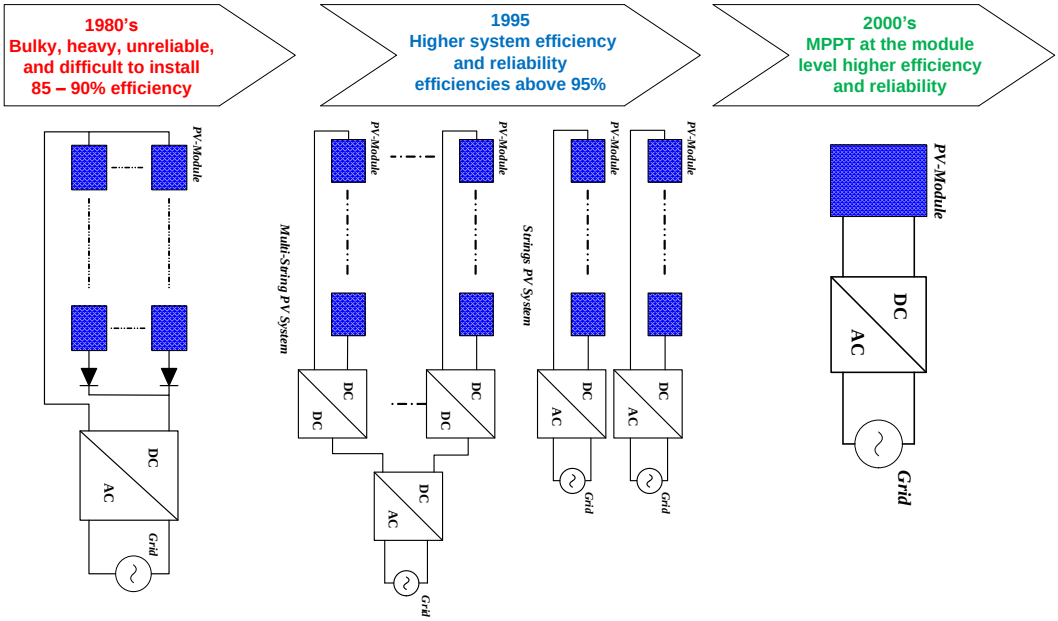


Figure 1.9: Photovoltaic (PV) system configurations

1.3 LED lighting – Energy efficiency

According to [13] it was found that one-fifth of the world-wide electricity is consumed in lighting applications. In the US, 17% of the total electricity is used for lighting [14].

The most commonly used lighting sources include incandescent bulbs and fluorescent lamps. However, these lighting sources have reported a relatively low efficiency. Recently, a new form of fluorescent lights, the compact fluorescent lamp (CFL), has becoming more popular in the lighting industry, which is known as "energy-saving light" because of its higher efficiency compared to the old technologies. However, CFL lights still suffer from a low lifetime. Thus, a new more efficient, high-reliable, and cost effective lighting source has been proposed using LED semiconductors. Figure 1.10 shows the three different lighting technologies and their advantages. LEDs have attracted the attention in last few years due its many advantages: high efficiency, small size (compactness), light weight, robustness, long lifetime (high reliability), and environmental friendliness [13, 15].

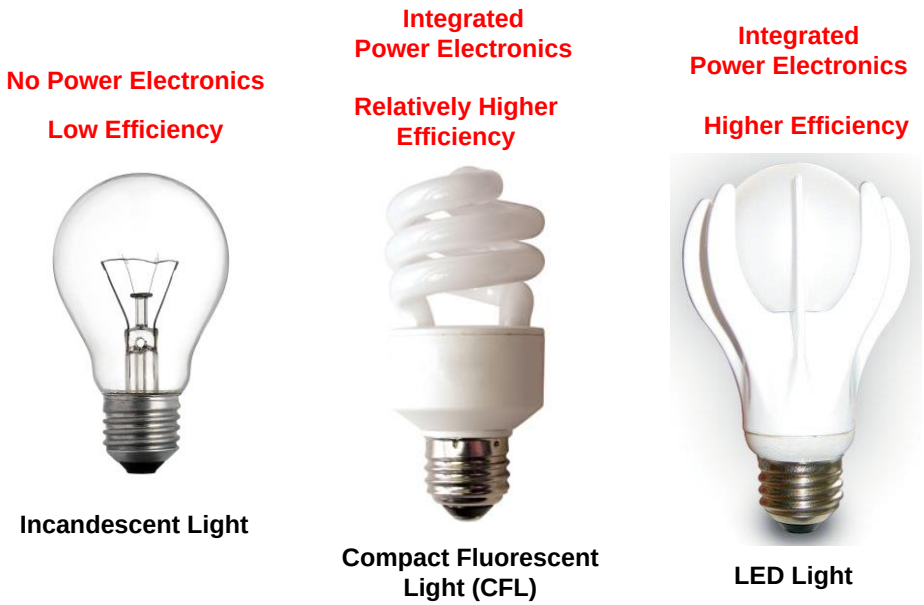


Figure 1.10: The evolution of the lighting technology

Figure 1.11 shows that by using LED lights, the energy consumption will be cut in half by 2030 [16].

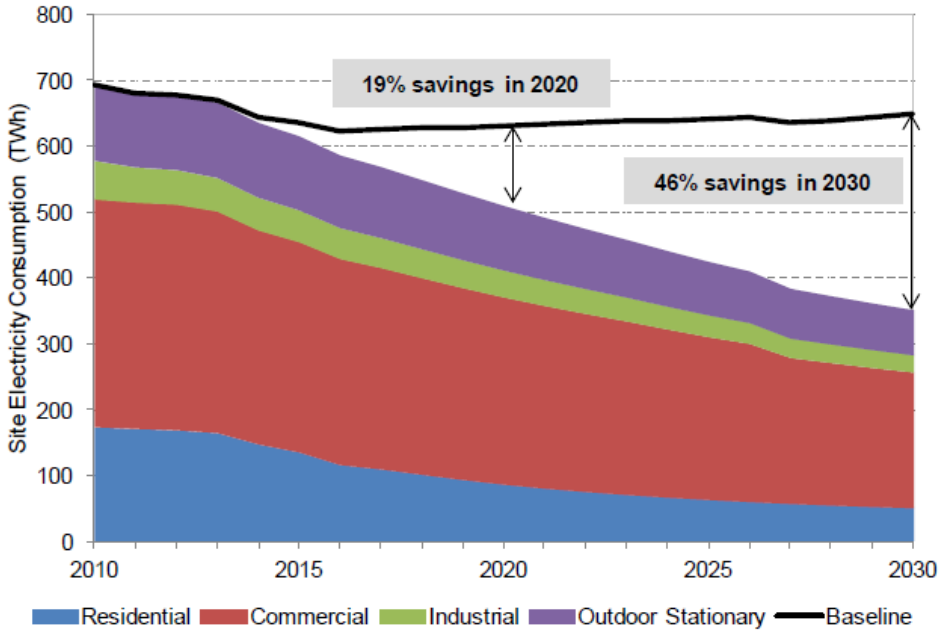


Figure 1.11: Forecasted U.S. lighting energy consumption and savings resulting from the increased use of LEDs, 2010 to 2030, source: DOE [16]

The CFL and LEDs lighting systems have the power electronics integrated into them. This necessitates that the power electronics have a lifetime that matches the light's lifetime. In the CFL case, this is not a serious issue, since the CFL's lifetime is relatively low. However, LED lights have a longer lifetime, more than 20 years [8]. LEDs lighting systems need a DC current to turn it on. Hence, if the source is an AC-line, then an AC-DC converter is needed to drive the LEDs. Many rectifier circuits have been proposed in

the literature [15, 17]. Based on the number of conversion stages and the number of phases, theses rectifier topologies can be categorized into four types: single-phase single-stage, single-phase multi-stage, three-phase single stage, and three-phase multi-stage [17]. The single-phase PWM rectifier has numerous advantages over classical passive rectifier topologies including: unity power factor, low THD, bidirectional power flow, and low components count [18, 19], and is well suited for applications with power ranging from data center servers to LED lighting.

1.4 Dissertation outline

This thesis deals with the reliability of the integrated power electronics that are used in uncontrolled operating environments, such as: renewable energy applications, LED lighting systems, etc. Operating in such an environment imposes very harsh, volatile, and wide-range conditions on the power electronic converters. And thus, evaluating the reliability of these converters becomes more involved task. The study is divided into two main aspects: (1) a new methodology for evaluating the integrated power electronics; and (2) a new power decoupling technique for the single-phase DC/AC and AC/DC converters, which will improve the reliability. The remainder of this dissertation is organized as follows.

In section 2, the reliability of integrated power electronics is thoroughly investigated taking into account the usage model. PV module-integrated-inverter (MII) is considered as a case study, and a comparative study of the reliability for different PV-MII topologies is performed.

In section 3, the PV-MII configuration is compared against the string PV system configuration. A typical 6 kW residential PV system is designed considering both PV configurations. Reliability, environmental factors, inverter failure, and electrical safety are the main factors that are investigated and evaluated.

In section 4, the double-line frequency ripple problem is presented alongside its negative effects. Different decoupling techniques are presented and categorized based on the decoupling capacitor place.

In section 5, the DC-link based ripple-port technique for double-line-frequency ripple cancellation is presented. The ripple-port concept is implemented and tested in DC/AC inverting mode and AC/DC rectifying mode. Analysis, simulation, and experimental results are presented.

In section 6, the AC-link ripple-port topology is presented. Similarly, analysis simulation results are presented. Practical experimental limitations for the proposed topology implementation and possible solutions are presented.

In Section 7, the DC-link ripple-port MII is compared to the conventional DC-link MII. Based on the assumption that both configuration offer the same lifetime, efficiency, power density, and cost of each configuration are studied and presented.

Finally, Section 8 is a summary and conclusion of the work presented in this dissertation. Also, possible future work on this subject is presented.

2 TAXONOMY, USAGE MODEL, AND RELIABILITY [*]

The trend in power electronics is to integrate the electronics into the source (PV) or the load (light). For PV and outdoor lighting applications, this imposes a harsh, wide-range operating environment on the power electronics. Thus, the reliability of power electronics converters becomes a very crucial issue. It is required that the power electronics, used in such harsh and uncontrolled environments, have reliability indices, namely: lifetime that matches the lifetime of the source or the load. For example, integrating the inverter with the PV module necessitates that the integrated-inverter has a lifetime that matches the PV module, 25 years or more [8, 20, 21]. This eliminates the reoccurring cost of inverter replacement that haunts current PV system return on investment (ROI). The reoccurring cost is further extended in a PV- Module-Integrated-Inverter (MII) since the electronics are exposed to a harsher environment than in the past when the inverter was mounted indoors [22, 23]. Similarly in LED applications, the power electronic circuit is integrated into the LED lighting; since the LED has a high lifetime—more than 20 years—the power electronics are desired to have a lifetime that matches that of the LED.

Relatively high-efficiency topologies have been reported in the literature [9], and

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standards have been developed to measure the efficiency [24]. However, the reliability aspect has not received the same level of scrutiny. The emergence of the ACPV module in which the power electronics are directly mounted to the PV module has led to the start of a rigorous study of the reliability of the PV inverter [25-29]. The recent surge of interest in cost-effective renewable energy has accordingly focused attention on the balance of system (BOS), including the power electronics needed to convert generated power into a useful form and facilitate the penetration of these resources to the utility grid [30]. Although not everyone agrees with the methodology or underlying data, MIL-HDBK-217 [31] has long been considered a standard for computing Mean Time Between Failure (MTBF) as an assessment of reliability, and thus serves as an excellent relative yardstick for comparison. MIL-HDBK-217 is based on probability distribution and it is not a demonstration of actual life of the specific device nor does it seek to identify failure modes. As such, testing a small sample of units to failure may not result in exactly identical results to the MTBF prediction. However, the MIL-HDBK-217 approach instead takes into account statistically large samples sizes of individual components and applies an acceleration factor based on the various component stresses—in the case in this study, for example, power dissipation and ambient temperature. Operation time and operating environment are important conditions that strongly affect the reliability of power electronics. Evaluating inverter's reliability at just one single operating condition, for example, the worst operating condition, leads in most cases to unrealistically low and pessimistic results, which require more expensive components to mitigate.

In this section, a new methodology to calculate the MTBF of a PV-MII is presented,

which takes into consideration the usage model of the inverter—the statistical distribution of expected operating temperature and power processed rather than a single (worst-case) operating point. Then, six different inverter topologies, suitable for a MII, will be studied in the scope of reliability [8, 9]. This section is organized as follows: the usage model for PV-MII is developed in the next section, and then different ways for calculating the MTBF is presented in 2.2. The proposed methodology is applied on different MII topologies in 2.3 followed by the reliability and lifetime results in 2.4 and 2.5, respectively.

2.1 Usage model for reliability evaluation

Operating conditions can be either experimentally measured data or predicted by a thermal model [22]. Although the actual measurements result in accurate reliability predictions, it is more complex because of the need for an experimental setup and long time to collect a meaningful set of data. On the other hand, using thermal analytical models eliminates the aforementioned disadvantages, but on the expense of the accuracy. A combination of both experimental measurement and thermal model prediction could potentially give accurate, fast, and less expensive measurements.

2.1.1 Developing a usage model

In this section, an electrical model is developed using expected operating points. Either from a thermal model [22] or experimentally measured data, it is possible to obtain the range of operating points for temperature and insolation level (T_m, G_m) in pairs as follows:

(Operating temperature (T_m), Insolation Level (W/m^2), G_m).

Given the system specifications (the output voltage of the inverter, v_0, and the inverter topology type), the electrical stresses on the inverter components can be calculated at each operating point. After calculating these stresses, the reliability calculation starts. Figure 2.1 shows the flowchart of the proposed methodology for calculating the reliability of integrated power electronics in outdoor applications.

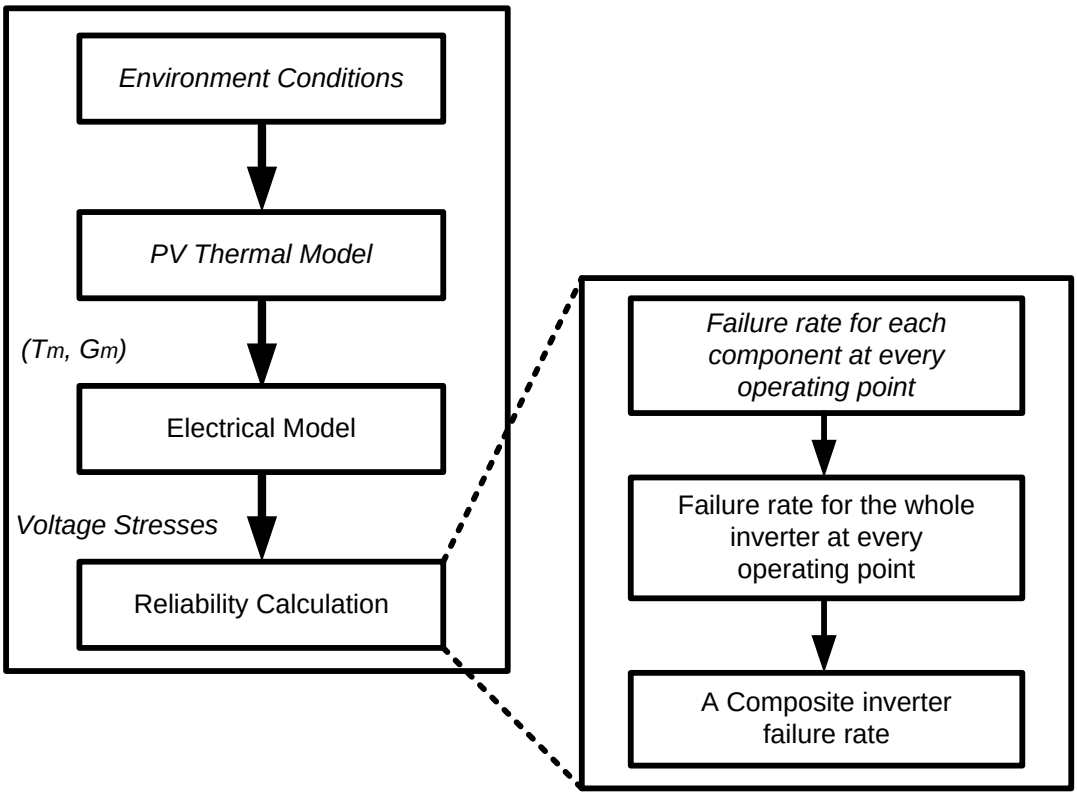

Figure 2.1: New methodology for calculating the reliability of integrated power electronics in outdoor applications

2.1.2 Experimental data

The experimental hourly measurements, used in this section, come from the PV system installed on the roof of the Zachry Engineering Building at Texas A&M University, College Station, Texas, USA. The data used is from the period between May 2010 and Oct. 2010 and represents a wide range of hourly operating conditions including the hottest season in Texas. Figure 2.2 and Figure 2.3 show the measured operating temperature (T_m) and insolation level (G_m), respectively.

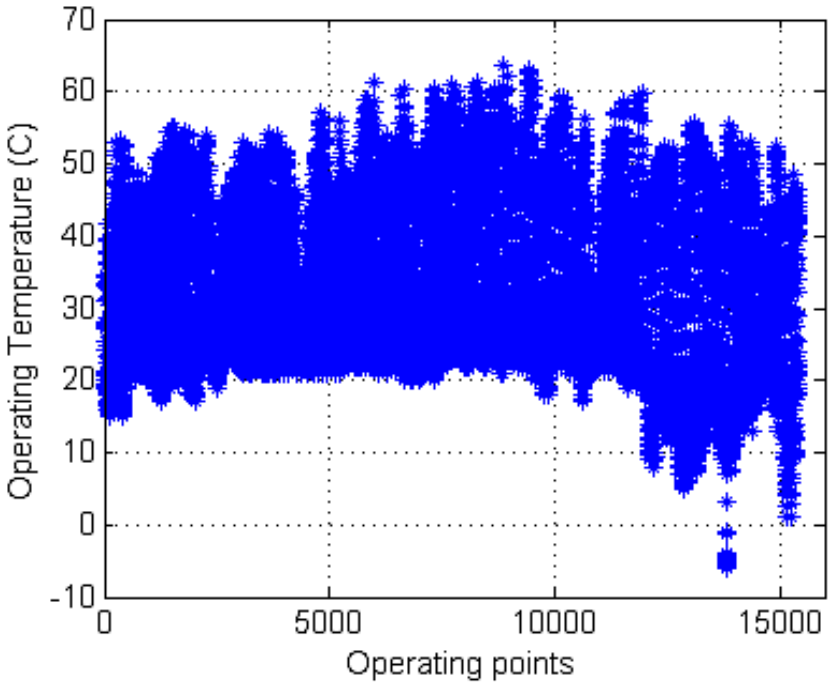

Figure 2.2: Hourly measured operating temperature (T_m)

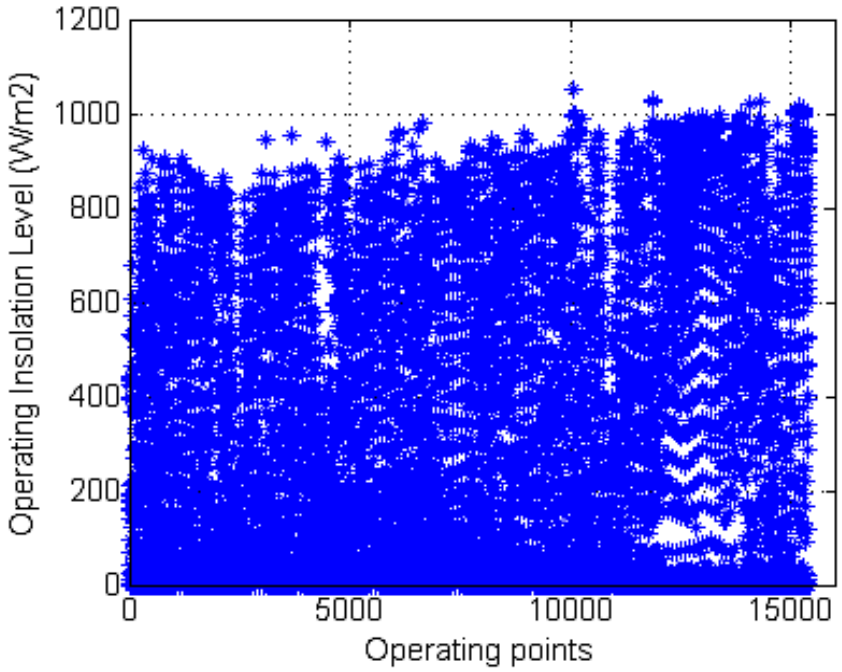

Figure 2.3: Hourly measured insolation level (*G*)

2.1.3 PV electrical model

The output voltage at the PV module terminals, V_{PV}, can be calculated for every operating point using the simplified PV cell model [32]. The output current of the PV module is found from the Shockley equation diode model of the cell as shown in (2.1)

$$I = I_L - I_0\left(\exp\left(\frac{V_{PV}}{N_S V_T}\right) - 1\right) \tag{2.1}$$

where the photocurrent (I_L) and the diode current (I_0) are given as follows:

$$I_L = I_L(T_r)\left(1 + K_0(T_m - T_r)\right) \tag{2.2}$$

$$I_0 = I_0(T_r)\left(\frac{T_m}{T_r}\right)^{3/n} \exp\left(\frac{-qV_g}{nk\left(\frac{1}{T_m} - \frac{1}{T_r}\right)}\right) \tag{2.3}$$

All parameters in (2.1) – (2.3) can be found in [32].

Since both the voltage and the current of the PV module are unknown, a third equation is needed. The output power provides this extra equation:

$$\begin{aligned} P_{PV} &= V_{PV} I \\ P_{PV} &= V_{PV}\left(I_L - I_0\left(\exp\left(\frac{V_{PV}}{N_S V_T}\right) - 1\right)\right) \end{aligned} \tag{2.4}$$

The PV-MII system is assumed to operate at the maximum power point (MPP), a realistic assumption given the desire to extract maximum energy from the PV system and the prevalent use of maximum power point tracking controls. Hence, the derivative of the power in (2.4) with respect to the PV module output voltage is zero, as shown in (2.5)

$$\frac{dP_{PV}}{dV_{PV}} = I_L + I_0\left(1-\exp\left(\frac{qV_{PV}}{N_S kT}\right)\left(1+\frac{qV_{PV}}{N_S kT}\right)\right) = 0 \tag{2.5}$$

Solving (2.5), for V_{PV}, results in the voltage across the PV module terminals for each operating point. Figure 2.4 shows V_{PV} as the operating conditions change. From the PV module voltage, the voltage stresses of components within the inverter can be calculated.

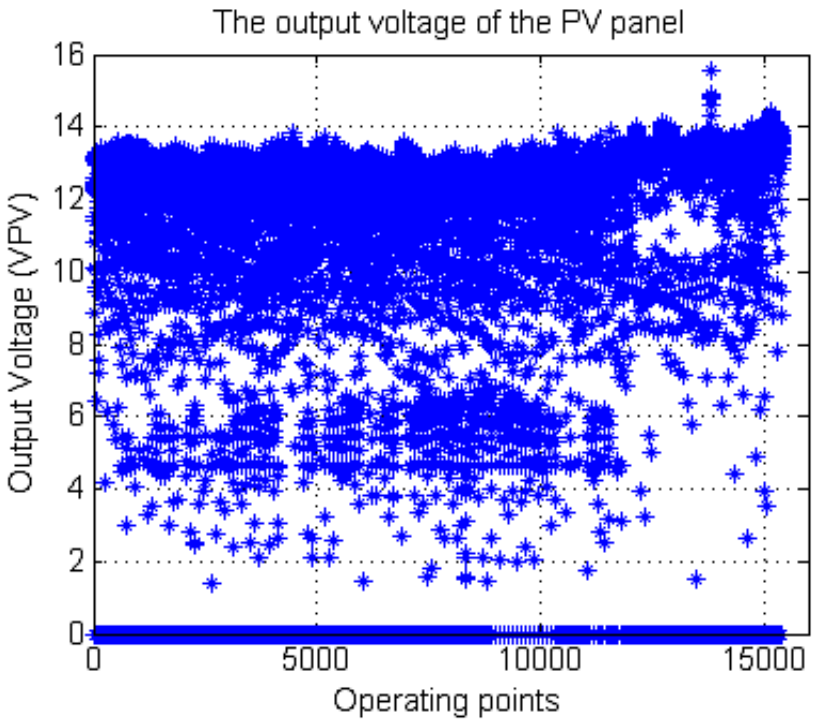

Figure 2.4: PV module output voltage (V_{PV}) variations as insolation conditions change

2.2 Reliability prediction calculation

Any reliability calculation standard can be used to calculate the failure rate. In this section, MIL-HDBK-217 [31] is used because it is freely available unlike other reliability tools—Telcordia. The failure rate for each component is calculated at every operating point (T_m, G_m) using MIL-HDBK-217. The failure rate formulas, shown in Table 2.1, clearly show that operating temperature affects all considered components. The Module Integrated Inverters are assumed to operate in a benign environment, and according to MIL-HDBK-217 the environment factor in this case is one ($\pi_E=1$).

It is worth mentioning that reliability is usually represented by the reciprocal of the failure rate. The term Mean Time Between Failure (MTBF) is often used interchangeably with MTTF, which is valid when a failure is not repairable. In most electronic devices, these values are similar if not identical because of the limited or total lack of reparability of a failure [33]. Hence, the more common expression MTBF is used in this section with the understanding that what is meant is really MTTF.

2.2.1 Different methods for calculating the MTBF

The failure rate for the PV-MII is calculated in five different ways:

I. At each operating point *(T_m, G_m)*

II. The worst case or the minimum MTBF

III. The corner MTBF, which occurs at the maximum temperature and maximum power (or insolation level)

IV. The composite (averaged) MTBF, found from the arithmetic mean as follows:

$$MTBF_{av} = \frac{1}{L}\left(\sum_{i=1}^{L} MTBF_i\right) \tag{2.6}$$

a) $MTBF_{av}$ is the averaged inverter MTBF

b) $MTBF_i$ is the inverter MTBF at the i^{th} operating point

c) L is the total number of operating points

V. Finally, since the operating temperature (T_m) affects the failure rate of all components, its distribution, shown in Figure 2.5, will be used to calculate a weighted MTBF.

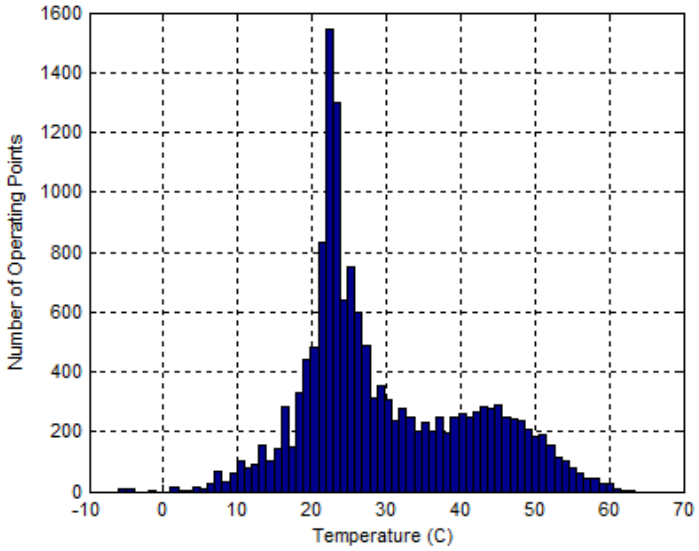

Figure 2.5: Operating temperature, Tm, distribution

The results in [22] strongly support the idea of considering all operating temperatures in calculating the MTBF. Also, the results in [22] show that the PV module temperature exceeded 80°C for only 2 hours out of the 59,740 total operating hours in the 15 year data set. Moreover, it shows that the PV module was operating at temperatures less than 60°C for 95% of the time.

2.2.2 Weighted MTBF

Analysis of the operational data reveals that some operating points occur more frequently than others, which means that the inverter will be operating at these conditions more frequently than at others. This can be taken into consideration by calculating a weighted MTBF. This section does not endorse the merits or suggest improvements to deficiencies of MIL-HDBK-217, but rather presents a way to use the tool to analyze the relative differences in reliability of candidate converter topologies. MIL-HDBK-217 does not include stress factors for every physical failure mode that we as designers must consider. Indeed there are other analysis tools, such as the Telcordia method that improves upon MIL-HDBK-217. That said, we feel that the concept of using a reliability index, in this case MIL-HDBK-217, has merit and deserves to be understood as another way in which candidate topologies can be compared analytically before committing to a design and investing time and money into building and testing a prototype. In the formulas shown in Table 2.1, the temperature is used as an input to the calculation for the failure rate of each component. Solar insolation also affects the failure rate by varying the input voltage at the PV module terminals, V_{PV}. According to MIL-HDBK-217 [31], the failure rate

formula for the MOSFET, shown in Table 2.1, does not have a voltage stress factor, and it depends on the following factors: base failure rate (λ_{b_S}), which is given in MIL-HDBK-217, the temperature factor (λ_T) that depends on the operating temperature as shown in Table 2.1, the power factor (λ_A), which is given in MIL-HDBK-217 for different power ratings, and finally the quality (λ_Q) and environment (λ_E) factors, which also are given in MIL-HDBK-217 and selected for a specific application. Hence, the failure rate of the MOSFET, according to MIL-HDBK-217, will not be directly affected by the changes in the applied voltage, since the power rating categories, given in MIL-HDBK-217, are relatively wide. Hence the input voltage affects just the diode failure rate. As a result, the temperature has a stronger impact on the MTBF values than the insolation. Therefore, weight factors based on the operating temperature will be used and a composite MTBF will be formed from the weighted average failure rates of the operating points.

First, the weight factors are given as follows:

$$C_i = \frac{N_i}{N_T} \tag{2.7}$$

where:

N_i is number of operating temperature points in the i^{th} temperature range,

N_T is the total number of operating temperature points,

i= 1, 2, ……N_n, and

N_n is number of intervals, given as:

$$N_n = Ceil\left(\frac{T_{\max} - T_{\min}}{S}\right),$$

Ceil is the rounds the number of temperature intervals into the nearest higher integer

S is step in temperature.

Then, the weighted MTBF is calculated as follows:

$$MTBFWg = \sum_{k=1}^{Nn} MTBF(T_k) * C_k \tag{2.8}$$

where:

$MTBFW_g$ is the weighted inverter MTBF,

$MTBF\ (T_k)$ is the MTBF at T_k , and

$T_k = \frac{T_i + T_{i+1}}{2}$, $k=1,2,....N_n$

Following this procedure leads to a large reduction in the number of total computational operations required to calculate the average inverter MTBF. Next, the proposed methodology is applied to evaluate the reliability of potential MII candidates.

Table 2.1: Failure rate formulas, MIL-HDBK-217 [31]

	Failure Rate (λ_p)	
MOSFET	$\lambda_{P\_S} = n * \lambda_{b\_S} \pi_T \pi_A \pi_Q \pi_E$	$\lambda_{b\_S} = 0.012$ $\pi_T = \exp\left(-1925\left(\frac{1}{T_m + 273} - \frac{1}{298}\right)\right)$ $\pi_A = 8 \left(50 \le P_r < 250W\right)$ $\pi_Q = 5.5$ (Lower)
Diode	$\lambda_{P\_D} = n * \lambda_{b\_D} \pi_T \pi_S \pi_C \pi_Q \pi_E$	$\lambda_{b\_D} = 0.025$ $\pi_T = \exp\left(-3091\left(\frac{1}{T_m + 273} - \frac{1}{298}\right)\right)$ $\pi_S = \begin{cases} 0.054 & V_S \le 0.3 \\ V_S^{2.43} & 0.3 < V_S \le 1 \end{cases}$ $\pi_Q = 5.5$ (Lower)
Capacitor	$\lambda_{P\_C} = n * \lambda_{b\_C} \pi_{CV} \pi_Q \pi_E$	$\lambda_{b\_C} = 0.00254\left(\left(\frac{S}{0.5}\right)^3 + 1\right)\exp\left(5.09\left(\frac{T_m + 273}{378}\right)^5\right)$ $\pi_{CV} = 0.34C^{0.18}$ $\pi_Q = 10$ (Lower)
Inductor & Transformer	$\lambda_{P\_I} = n * \lambda_{b\_I} \pi_T \pi_Q \pi_E$	$\lambda_{b\_I} = 0.00003,\ \lambda_{b\_Tr} = 0.019$ $\pi_T = \exp\left(\frac{-0.11}{8.617 * 10^{-5}}\left(\frac{1}{T_m + 273} - \frac{1}{298}\right)\right)$ $\pi_Q = 3$ (Lower)

2.3 Candidate inverter topologies for photovoltaic applications

There are many inverter topologies in the literature that have been proposed in the last decade for PV applications. Aside from the obvious differences in voltage, power, and number of phase, these topologies can further be classified according to the number of the power conversion stages, the power decoupling technique employed, and the presence of galvanic isolation. For single-phase grid-connected MII, the latter is desirable for safety purposes. Within a given topology, the capacitor technology used for power decoupling is a crucial issue [34] as it is widely known to have a significant impact on the reliability of the inverter, as will be demonstrated in this section.

In a single-phase inverter, a double-line frequency ripple is reflected at the input (DC) side. In a PV system, this ripple will deteriorate the MPPT performance and consequently reduce the system total energy harvest. Hence, a storage device is needed to filter out the double-line frequency ripple. Usually, a capacitor is used to accomplish this task [8, 9, 35-37]. The double-line-frequency ripple problem is presented in Section 4 in detail. Figure 2.6 shows the input current (blue) and the output voltage (green) of a single-phase inverter that uses an electrolytic capacitor on the input side ($4400\mu F$). The results in Figure 2.6 show an almost ripple-free input current. However, when the large, electrolytic capacitor, used in the previous test, is replace by a another smaller capacitor ($33\mu F$) the input current has a much higher double-line frequency ripple, as shown in Figure 2.7. Figure 2.6 and Figure 2.7 experimentally justify the necessity of using the capacitor in order to have a ripple-free input power. Having the double-line frequency ripple on the input side of the MII results in shifting the MPP operating point away from the optimum operation [8]. The

previous conventional technique is one of many decoupling techniques that will be presented later in section four [38].

In this section, a module-integrated inverter, rated for 235W, is considered for interface with the AC utility grid under high-line / low-line conditions (V0=[90 – 132]V_{rms} [39]). The specifications of the selected PV module (SHARP Solar electric 235W [12]) are as follows: open circuit voltage (V_{oc}) 37 V, maximum power voltage (V_{MPP}) 30.1 V, short circuit current (I_{sc}) 8.5 A, maximum power current (I_{MPP}) 7.81 A, and module efficiency (%) 14.4%.

The selected topologies for the purpose of this study are categorized into three groups based on the place and the type of the decoupling capacitor: 1) PV-side-electrolytic capacitor (Ia1); 2) dc-link-electrolytic capacitor (IIa1); and 3) PV-side-film capacitor (Ib2). All possible decoupling techniques for the single-phase inverter are listed in Table 2.2. The double-line ripple problem and decoupling techniques are investigated thoroughly in section four.

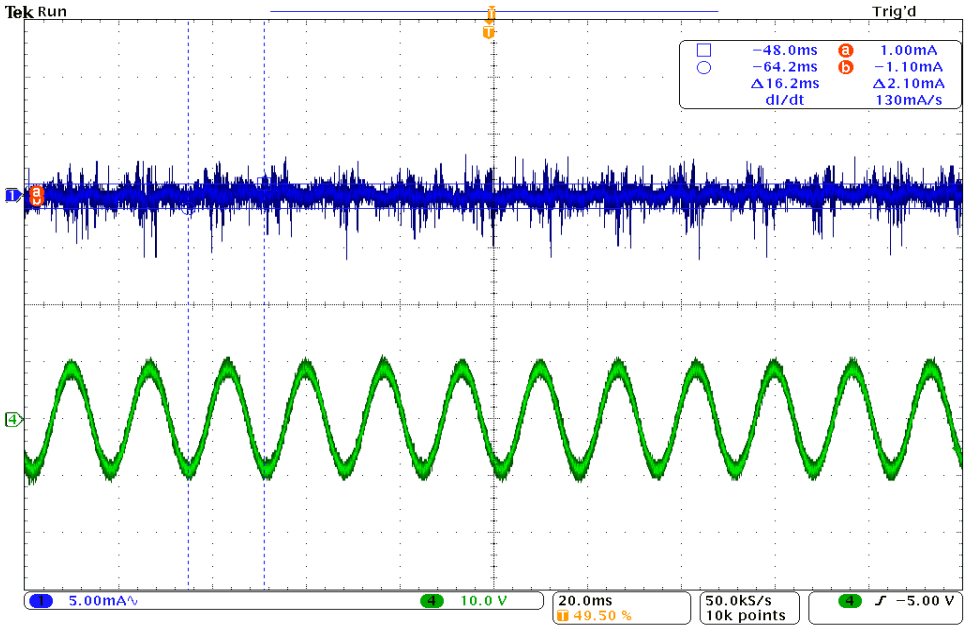

Figure 2.6: Input current (top trace), and the output voltage (bottom trace) of a single-phase inverter, with a large electrolytic capacitor (4.4 mF) at the input

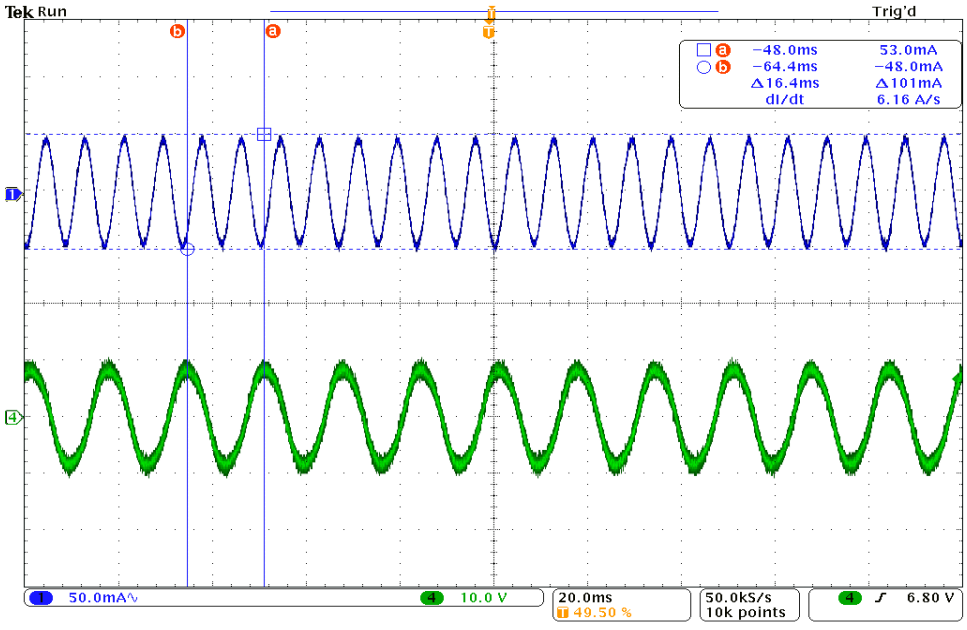

Figure 2.7: Input current (top trace), and the output voltage (bottom trace) of a single-phase inverter, with a small capacitor (33 µF) at the input

Table 2.2: Power decoupling techniques based on the place and the type of the capacitor

Type – Decoupling Technique		A- Electrolytic Capacitor	B- Film Capacitor
Type I – PV side	1- Passive circuit	Very Large capacitor Low lifetime	Not cost effective Very large capacitor
	2- Active circuit	Extra components – no valuable improvement	Extra components
Type II – DC-link	1- Passive circuit	large capacitor Low lifetime	Not cost effective large capacitor
	2- Active circuit	Extra components – no improvement	Extra components
Type III – AC side	1- Passive circuit	Not feasible	Not feasible
	2- Active circuit	Not feasible	Extra components Minimum required capacitance

2.3.1 Type I -PV-side-electrolytic capacitor (Ia1)

The topology in Figure 2.8 is a commercial inverter [8]. Although it consists of three power conversion stages, the decoupling capacitor is placed at the PV-side. According to [38], the required capacitance is given by (2.9)—the detailed analysis is presented in Section four. In order to meet the system specifications (235W, 30V, and 5% voltage ripple), an electrolytic capacitor of *13,760µF* is needed. In practice, numbers of paralleled smaller capacitors are used. The two options (one large capacitor and four smaller

capacitors) are explored to quantify the effect of number of components.

$$C_D = \frac{P_{PV}}{\omega_o V_{DC} \Delta V} \tag{2.9}$$

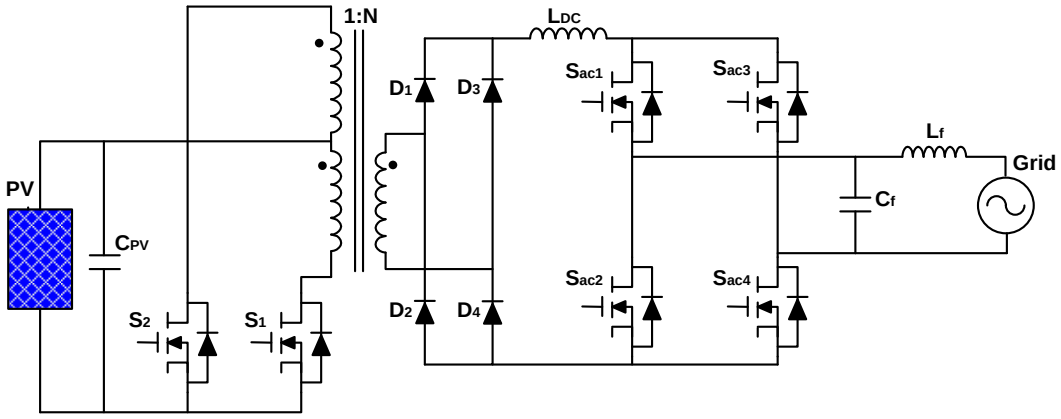

Figure 2.8: Commercial inverter topology, PV-side-electrolytic capacitor

The same power decoupling technique is employed by the topology in Figure 2.9 [40]. However, this inverter topology consists of single power conversion stage, hence, fewer components are used. The purpose is to explore the impact of the number of power components on inverter reliability. Only two diodes and three MOSFETs are needed compared to four diodes and six MOSFETs needed by the previous topology in Figure 2.8.

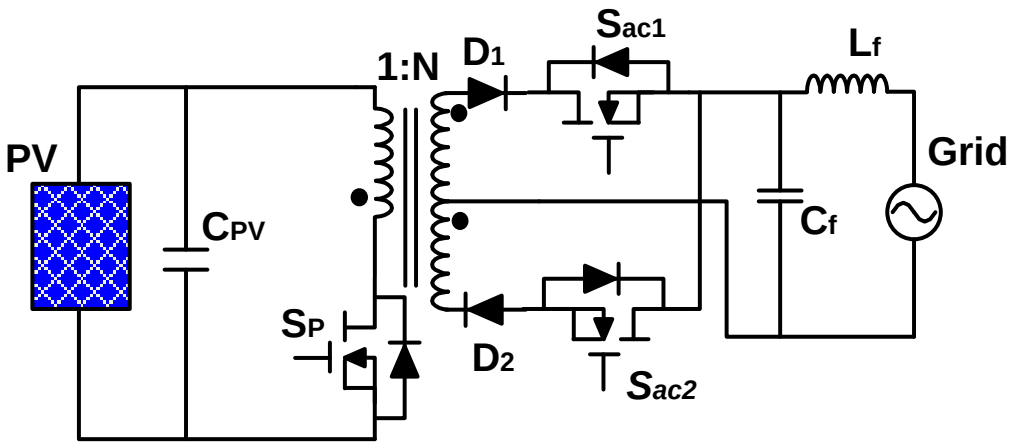

Figure 2.9: Flyback type topology, PV-side-electrolytic capacitor

2.3.2 Type II - DC-Link-electrolytic capacitor (IIa1)

The topology shown in Figure 2.10 is also a commercial inverter [9]. It consists of three power conversion stages; an inverter and a rectifier, at the front end, are used to provide a galvanic isolation using high-frequency transformer. The decoupling capacitor is placed at the DC-link with a relatively higher voltage level. This, in turn, allows for a smaller capacitance to be used for the same power rating. According to (2.9), a $330\mu F$ electrolytic capacitor is needed to meet the aforementioned specifications. Another topology, shown in Figure 2.11 [41, 42], also employs the DC-link power decoupling; however, it consists of two power conversion stages. As a result, fewer components are used. Similarly, this is meant to study the effect of components other than the decoupling capacitor on the reliability of the inverter.

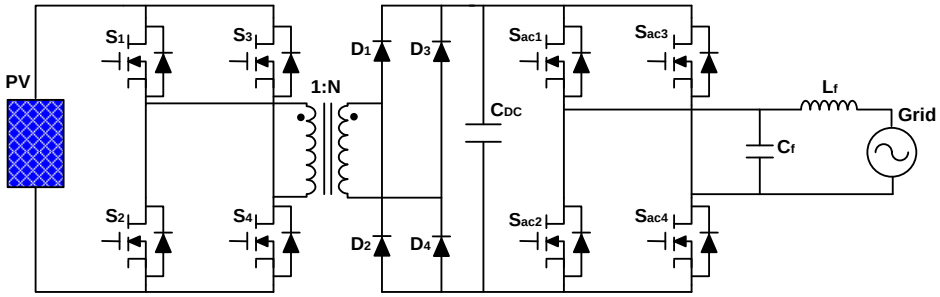

Figure 2.10: Commercial inverter topology with electrolytic dc link capacitor

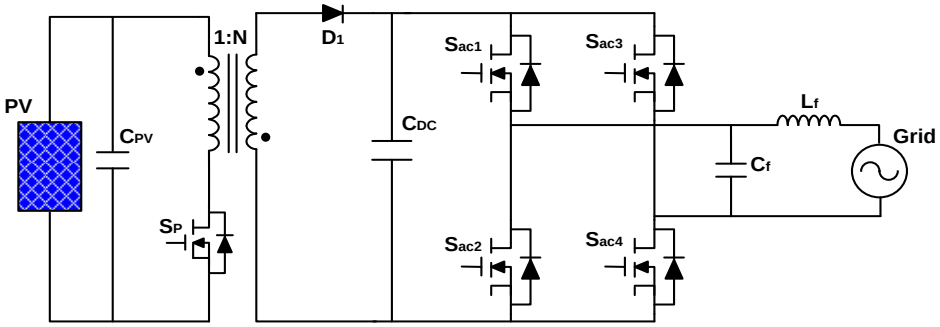

Figure 2.11: Flyback inverter topology with electrolytic dc link capacitor

2.3.3 Type I - PV-side-film capacitor (Ib2)

Recently, many researchers tend to replace the bulky electrolytic capacitors with film capacitors that are more reliable [43]. Accordingly, a number of inverter topologies have been proposed in the past few years [35]. In this section, and for comparison purpose, two inverter topologies are analyzed. Both topologies use film capacitor at PV-side as a decoupling capacitor.

The topology, shown in Figure 2.12, is based on the flyback inverter, where the

decoupling capacitor is detached from the PV terminals by using one extra MOSFET and diode [44]. Removing the decoupling capacitor from the PV module terminals allows for arbitrary high voltage across the capacitor's terminals. Consequently, only a small decoupling capacitance is needed f to meet the aforementioned system specifications of 235W, the required capacitance is $40\mu F$ [44].

The second topology, shown in Figure 2.13 [39], is a modified version of the previous topology. The main advantage of this topology is the ability to handle the transformer leakage energy without using an extra circuitry—snubber circuit—as in the previous topology [39]. Yet, the modified topology uses more power switches. Hence, the effect of higher components count on the reliability is evaluated. This topology also needs $40\mu F$ of decoupling capacitance for a 235W system.

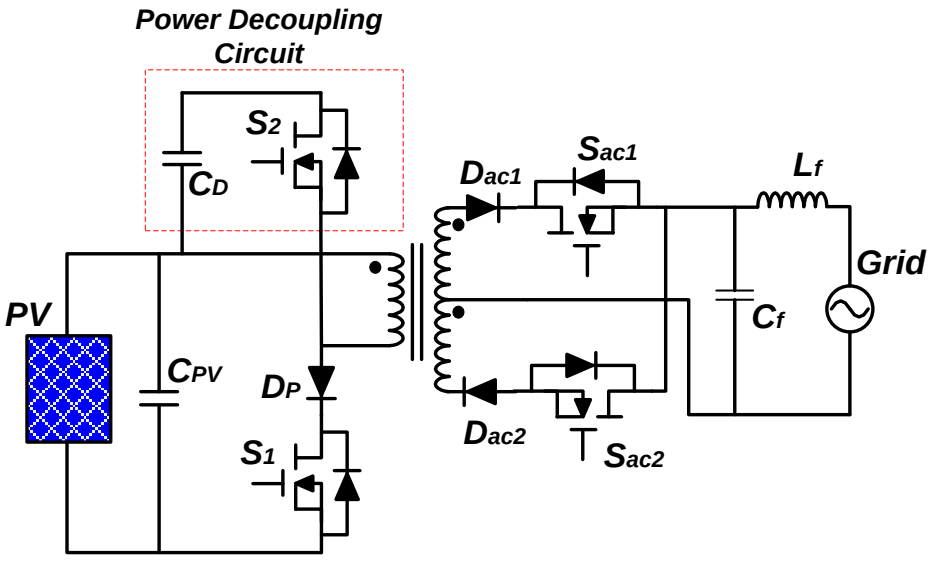

Figure 2.12: Flyback inverter with film capacitor as a decoupling capacitor

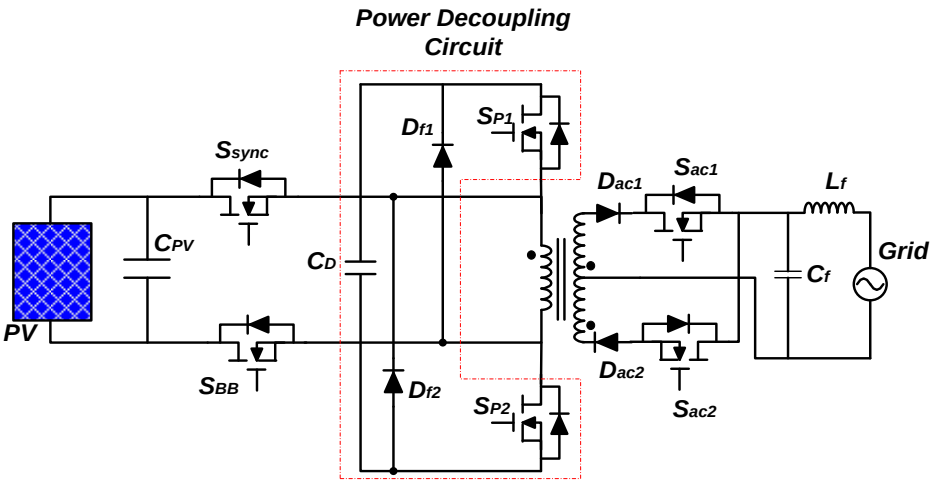

Figure 2.13: A modified version of the flyback inverter with film capacitor as a decoupling capacitor

2.3.4 Inverter electrical stresses

According to the MIL-HDBK-217 standard, only diodes and capacitors are affected by the voltage stress. However, the failure rate of MOSFETs is affected by the power rating of the inverter, which is considered the same for all the topologies in this section [31]. But, numbers of the MOSFETs vary from each topology that has an impact on the failure rate. Table 2.3 shows the voltage stresses on the diodes and capacitors used in each topology. The stresses are functions of the actual voltage across the PV module terminals, V_{PV} that depends on the operating point: actual operating temperature (T_m) and insolation level (G_m).

Table 2.3: Voltage stress as a function of the operating point (T_m, G_m)

	Diodes	Capacitor
Figure 2.8	$V_{D1} = V_{D2} = V_{D3} = V_{D4} = NV_{PV}$	$V_{Cdc} = V_{PV\_OC}$
Figure 2.9	$V_{D1} = V_{D2} = NV_{PV} + V_{grid\_P}$	$V_{Cdc} = V_{PV\_OC}$
Figure 2.10	$V_{D1} = V_{D2} = V_{D3} = V_{D4} = NV_{PV} + V_{DC}$	$V_{Cdc} = V_{DC}$
Figure 2.11	$V_{D1} = NV_{PV} + V_{DC}$	$V_{Cdc} = V_{DC}$
Figure 2.12	$V_{Dp} = V_{PV} + V_{Cdc}$ $V_{Dac} = NV_{PV} - V_{grid\_P}$	$V_{Cdc} = V_{dc\_o} + \tilde{V}_{dc}$
Figure 2.13	$V_{Df} = V_{Cdc} - V_{PV}$ $V_{Dac} = NV_{PV} + V_{grid\_P}$	$V_{Cdc} = V_{dc\_o} + \tilde{V}_{dc}$

2.4 Reliability results

As explained in section 2.2.1, the MTBF is calculated in different ways. The results of applying these different ways on the potential MII topologies, in section 2.3, are presented in this section. The measurements, from section 2.1, were used for both finding the electrical stresses and failure rate calculations. For each MII topology, the MTBF for the MOSFETs, Diodes, transformer, and the decoupling capacitor are calculated at each operating point. The failure rate formulas, given in Table 2.1, are used to calculate the failure rate for these aforementioned components at each operating point. Then, the MTBF for the whole inverter is calculated using (2.11). Table 2.4 shows the MTBF (*million hours*) at the maximum operating temperature for the MOSFETs, capacitor, diode, inductor, transformer, and the whole inverter. The averaged and the weighted MTBF of the whole inverter, calculated using (2.6) and (2.8) respectively, are listed in Table 2.4 as

well.

The failure rate for the whole inverter is the sum of the failure rates of all components as follows:

$$\lambda_{P\_inv} = \lambda_{P\_S} + \lambda_{P\_D} + \lambda_{P\_C} + \lambda_{P\_I} + \lambda_{P\_Tr} \tag{2.10}$$

and the MTBF is computed as

$$MTBF = \frac{1}{\lambda_{P\_Inv}} = \frac{1}{\lambda_{P\_S} + \lambda_{P\_D} + \lambda_{P\_C} + \lambda_{P\_I} + \lambda_{P\_Tr}} \tag{2.11}$$

The proposed methodology, for evaluating the reliability of the MII, does not depend on a specific reliability calculation tool. Although MIL-HDBK-217 [31] is used in this study to calculate the MTBFs, shown in Table 2.4, it is worth to mention that other reliability tools like Telcordia and RELEX will result in approximately similar results. The results show that the averaged and the weighted MTBFs—for each topology—are almost the same. This concludes that a huge reduction in number of calculations—needed to find the average inverter MTBF—is gained by using the temperature distribution, shown in Figure 2.5. Although measured operating temperature is used in this study, the PV module temperature can also be calculated using the thermal model proposed in [22]. The PV-

side-electrolytic (Ia1) shows the lowest MBTF. While a small improvement is achieved by the DC-link-electrolytic (IIa1) technique, the PV-side-film (Ib2) technique shows three to six times improvement. The results in Table 2.4 show that the averaged MTBF for almost all the topologies is three times higher than the worst (corner) MTBF.

Table 2.4: MTBF for different MII topologies (million hours)

	Individual component						Complete inverter		
Topology	MOSFETs	Capacitor	Diodes		Inductor	Transformer	min MTBF & Corner MTBF	Averaged MTBF	Weighted MTBF
Figure 2.8 *4 caps*	141.34	0.1958	14.86		8758.5	41.48	0.1921	0.4764	0.4758
1 cap		0.6223					0.5863	1.4637	1.4607
Figure 2.9 *4 caps*	282.69	0.1958	10.34		-	41.48	0.1912	0.477	0.475
1 cap		0.6223					0.5776	1.470	1.453
Figure 2.10	106.01	0.892	13.11		-	41.48	0.5220	1.718	1.572
Figure 2.11	169.60	0.892	19.41			41.48	0.8318	2.090	2.070
Figure 2.12	212.02	6.376	D_p	D_{ac}	-	41.48	3.1704	5.577	5.504
			9.676	37.85					
Figure 2.13	141.34	6.376	D_f	D_{ac}	-	41.48	1.3200	3.274	3.343
			3.515	3.519					

2.5 Lifetime of the module-integrated inverter (MII)

In the previous section, the reliability calculations show that the MTBF of the whole inverter is determined significantly by the decoupling capacitor. The topologies that use film capacitor technology show a higher MTBF, which means that the probability of the inverter to work and accomplish all the required tasks properly during its useful lifetime

is higher. The useful lifetime of the inverter is determined by the component that has the lowest lifetime, which is believed to be the capacitor based on the reliability calculations in the previous section. Inverters that use film capacitor, as a decoupling capacitor, are expected to have a longer lifetime than inverters use an electrolytic capacitor. In this section, the lifetime of electrolytic and film capacitors will be examined.

Table 2.5 lists the capacitances used in the three categories along with their lifetime at the rated voltage and reference temperature [43, 45]. The formula in (2.12) is used to calculate the projected lifetime (L) at different operating temperature [46]. Figure 2.14 shows the projected lifetime for the three cases presented in Table 2.5: lifetime of the electrolytic capacitor on the PV-side (L_{E_PV}), the lifetime of the electrolytic capacitor on the DC-link (L_{E_DC}), and the lifetime of the film capacitor on the PV-side (L_F). Placing the decoupling capacitor on the DC-link allows for smaller capacitance to be used that in turn improves the lifetime of the inverter, as shown in Figure 2.14. The film capacitors show an order of magnitude higher lifetime over the entire operating temperature range.

$$L = \frac{L_0\left(2^{\left(T_{ref}-T\right)/10}\right)}{\left(\frac{V_{op}}{V_r}\right)^{2.6087\left[\left(V_{op}/V_r\right)+0.5167\right]}} \tag{2.12}$$

where V_{op} is the operating voltage and T is the operating temperature.

Table 2.5: Rate values of the capacitors used in this study

	PV-side-electrolytic capacitor	DC-link-electrolytic capacitor	PV-side-film capacitor
Capacitance (C)	4X3900µF	330µF	40µF
Rated voltage (V_r)	50V	250V	300V
Reference Temperature (T_{ref})	105ºC	105ºC	85ºC
Base Lifetime (L_0)	3000 Hr	7000 Hr	200,000 Hr

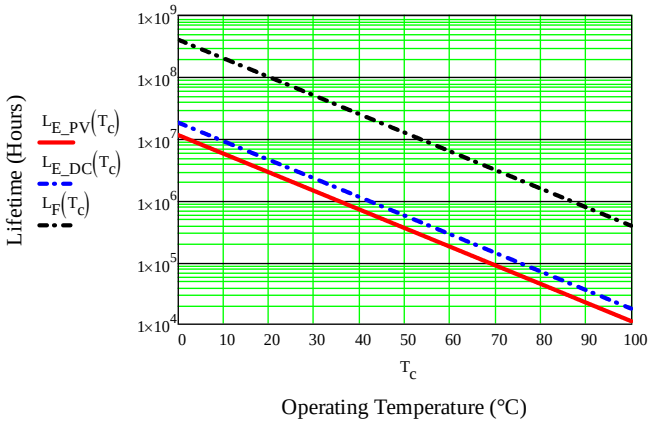

Figure 2.14: Capacitor lifetime as function of the operating temperature

2.6 Conclusion

The reliability of integrated power electronics converters is scrutinized in this section. A module-integrated inverter (MII) is considered as a case study. A new methodology for calculating the MTBF of the PV-MII based on a stress-factor approach is proposed. The proposed methodology takes into account the operating environment volatility of the PV-

MII. Hence, the results provide a quantified assessment of realistic MTBF under expected operating conditions. The MTBF for six different MII topologies was calculated based on the expected usage model for a PV module-integrated inverter and the MIL-HDBK-217. It was found that considering the usage model, rather than a singular worst-case operating point, yields a more optimistic MTBF. The results showed confirm the long-held belief that the double-line frequency decoupling capacitor is the dominant component, not the MOSFET, regardless of the numbers of power switches needed in the topology. Moreover, topologies that employ film capacitor for power decoupling instead of aluminum electrolytic capacitors have higher MTBF and longer lifetime. The reader is undoubtedly aware that the computation of MTBF can be easily influenced by good and bad design practices, such as component derating. Therefore, the objective of this study is not to judge the reliability merits of one topology over another. Rather, it is meant to present a method of applying a usage model of expected inverter operation as an evaluation tool when comparing different topologies on the basis of MTBF. The dataset we used in this section is, admittedly, limited, and therefore, it should not be taken to generally represent the expected MII reliability in general. Further work in this area will apply a larger dataset of operating points to represent a higher fidelity set of operating conditions.

3 MICROINVERTER AND STRING INVERTER GRID-CONNECTED PHOTOVOLTAIC SYSTEM – A SYSTEMATIC STUDY [*]

This section presents a systematic comparison between two different PV configurations: a string inverter based PV energy system and a microinverter based system. Reliability, environmental factors, inverter failure, and electrical safety of a test case 6kW residential PV system are thoroughly evaluated and compared considering the two configurations. The impact of all these features on the cost of the PV system is estimated. The results show that when the levelized cost of energy (LCOE) is considered, the break-even cost can be reached by the microinverter more quickly than with a string inverter operating in the same environment. Moreover, considering the replacement cost associated with the expected string inverter failure, the microinverter configuration is the more cost effective configuration.

3.1 Introduction

Is a microinverter more expensive than a string inverter? A microinverter connected to a single PV module has become a trend for residential grid-connected PV systems, replacing a single inverter connected to a string of series-connected PV modules. This is due microinverter advantages including: (1) improved energy harvest, (2) improved

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system efficiency, (3) lower installation costs, (4) plug-N-play operation, and (5) enhanced flexibility and modularity [8, 9, 47]. At first glance, the string inverter appears to have a lower per-watt capital cost when just the inverter is considered. However, the inverter represents only about 15% of the entire PV system cost whereas the installation labor and balance of system (BOS) cost account for 40%, depending on the system configuration and inverter technology [48]. These factors have made it difficult to perform a comparative cost study. Hence, in this section, we consider a 6kW PV system and compare the microinverter-based system with the string inverter-based system.

An alternating-current photovoltaic module (ACPV) is created when the microinverter is directly attached to a single PV module [49-52]. The result is a PV module that produces AC power without any extra electronic components. The implication, however, is that since the power electronic is indelibly integrated with the PV module, the microinverter must have a lifetime that matches the lifetime of the PV module—namely 25 years. Hence, most of the microinverter manufacturers provide a standard 25-year warranty [49, 50, 53, 54]. The high-reliability and long lifetime of the microinverter offer an added advantage over the string inverter that typically has a lifetime of only 10 years [55]. The impacts of the longer lifetime on the power generation, system failure, maintenance, and replacement cost have not been thoroughly investigated in the literature. This section identifies the effects of all the aforementioned factors on the total cost of the system over the expected 25-year lifetime of the PV module.

This section is organized as follows: the specifications of the system considered in this study are presented in the next section. Then, the reliability impacts of both configurations

are evaluated. After that, the impact of the operating environment is presented, and the levelized cost of energy (LCOE) of the system is evaluated. Finally, although it is not easy to quantify because of limited published data, the safety of the microinverter versus string inverter configurations is considered.

3.2 Case study system characteristics

In order to have an apple-to-apple comparison, a 6kW grid connected PV system is designed considering two approaches. The first approach uses a string inverter configuration, with 24 PV modules—250W each. Two strings are formed and connected in parallel; each string consists of 12 PV modules in series. Then, the DC output is connected to a 6kW string inverter, as shown in Figure 3.1(a). The other PV system is based on the microinverter concept in which each PV module is connected to one microinverter. The 24 microinverters are connected in parallel (AC connection), as shown in Figure 3.1(b). The safety of the high DC string voltage connection versus the AC connection will be examined later in this section.

The purpose of this study is not to evaluate the performance of the inverter itself, but rather the impact of different inverter-module configurations on the overall performance, lifetime and cost of the PV system. Therefore, the following features are assumed to be common for both string inverter and microinverter: (1) efficiency, (2) high quality voltage and current output, and (3) galvanic isolation. Also, both inverters are equipped with the maximum power point tracking (MPPT) feature [56] in order to harvest the maximum available energy. The string inverter performs MPPT at the string level while in the

microinverter configuration MPPT is performed at the module level. This leads to an increase in the amount of harvested energy and reduce the effect of shaded modules [8, 57, 58]. The impact of shaded module is quantitatively evaluated later in this study. Recently, the DC/DC optimizer has been proposed mainly to overcome the mismatch between the different PV modules and enhancing the energy harvesting function with a module-level MPPT [59, 60]. However, this configuration still suffers from the single point failure problem since only one DC/AC inverter is used for the whole system. Moreover, the DC/DC optimizers are connected in series to form high DC voltage that is fed into the string inverter. Hence, it is not considered in this study.

Monitoring the performance of the system is an essential feature for any PV system; it helps monitoring the power generation as well as detecting any failure the moment it happens that expedites the repair time. Consequently, it is assumed that both systems are equipped with a device that continuously monitors the system performance [55, 61].

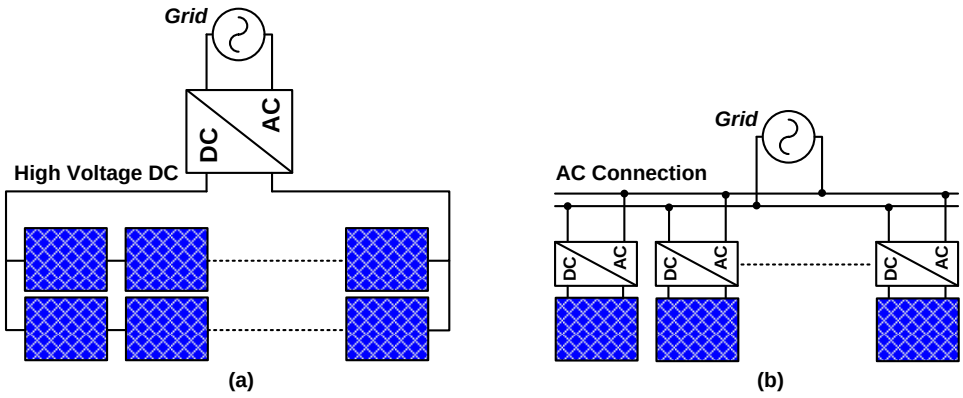

Figure 3.1: Comparison of electrical wiring for photovoltaic systems: (a) series dc connection for the string inverter (b) parallel ac connection for the microinverter

3.3 Reliability of the PV system

Currently, microinverter manufacturers are providing 25-year warranties [49, 50, 54]. On the other hand, manufacturers of string inverters typically provide 10 years warranties, and thus, the string invert is expected to need replacement at least once over the 25 years power-output guaranty of the PV modules [55, 62]. Thus the total system lifetime cost of the string inverter must include two inverters, the original and a replacement.

The inverter is generally considered to be the most failure prone component in the PV energy system [55, 63]. Recently, some PV operators have started publishing failure data from their installed PV systems. These results show that the string inverter is responsible for 43% of failures and 36% of energy loss [63]. The similar data for the microinverter is not available because it has not been in the field for long time yet. However, in addition to the 25-year warranty, its mean time to fail (MTTF) is very high, around 300 years [53]. This means that the probability of the microinverter to accomplish all the required tasks with no failure, during the useful lifetime, is 92% [33]. However, similar information is not available for the string inverter. Hence, the failure rate of the conventional string inverter is calculated in this study using MIL-217 handbook and the analysis in [47]. In single-phase inverters, energy storage, usually capacitors, is needed for double-frequency power decoupling. If the capacitor is located on the DC bus inside the inverter, the required capacitance is a function of the power ratings, DC voltage bus voltage, allowable bus voltage ripple, and the grid frequency [8, 64]:

$$C_D = \frac{P_{PV}}{\omega_0 V_{DC} \Delta V} \tag{3.1}$$

Equation (3.1) shows that the required capacitance is directly proportional to the system's power rating. Since the string inverter is rated for high power (6kW), it uses a large electrolytic capacitor as an energy balancing device [8, 9, 64]. It is known that electrolytic capacitors are the weakest component in the inverter [47]. Its failure rate, given in (3.2), is directly proportional to its capacitance and operating voltage and temperature [31]. This suggests that the failure rate of the string inverter is expected to be higher than the failure rate of the microinverter:

$$\lambda_{P\_C} = n * \lambda_{b\_C} \pi_{CV} \pi_Q \pi_E$$

$$\lambda_{b\_C} = 0.00254 \left(\left(\frac{S}{0.5} \right)^3 + 1 \right) \exp\left(5.09 \left(\frac{T_m + 273}{378} \right)^5 \right) \tag{3.2}$$

$$\pi_{CV} = 0.34 C^{0.18}$$

$$\pi_Q = 10$$

For the 6kW PV system at $400V_{DC}$ and 2% (8V) ripple, a 5,000µF is required as a decoupling capacitance according to (3.1). In practice, inverter manufacturers de-rate the

decoupling capacitance in order to ensure sure that the minimum capacitance requirement is met at the end of the inverter's lifetime. Assuming a stress factor (S) of 0.75, and 50°C operating temperature, the failure rate of a conventional string inverter is calculated using (3.2) to be *1.5 failures per million hours*. This can be interpreted, using (3.3), as 72% probability of operation and accomplishing all the required functions during its expected lifetime (25 years); whereas a commercial microinverter has a 92% probability.

$$p(\lambda) = e^{-\lambda t} \tag{3.3}$$

Unlike the conventional energy generating source, the loss (or cost) is related only to the cost of repair, since when the system is down no fuel is being consumed. But, in the case of alternative energy resource in general and PV system especially, the time that the system is not operating is considered as loss. This is because the energy source (or the fuel) is free, and just needs to be converted to the useful form. Hence, this potential energy loss is a key factor that should be precisely evaluated to help estimate the levelized cost of energy (LCOE) over the expected lifetime of the system. The impact of the failure rate manifests itself in the amount of loss in energy production when the inverter is not operating due to failure or repair time. However, a typical residential 6KW string inverter is non-repairable; rather it will be replaced with a new inverter once it fails. The cost of the inverter depends on whether the manufacturer warranty is limited to only one replacement during the inverter's lifetime. In this study we assume that the warranty is for

unlimited replacement during the inverter's lifetime and that the inverter will be replaced only one extra time during the PV system's lifetime (25 years) not covered by the warranty. The quantified cost will be presented later in the cost section.

3.4 Environmental impact

In this section, the impact of shaded PV modules is examined. It is expected that with different insolation level, the energy production, from PV modules of a fixed capacity also changes. The insolation dataset used is the average of the insolation level over the last 22 years for Austin, TX [65]. Consequently, the total expected energy production, over the PV modules' lifetime, is *1,660,324 kWh*. Next, the loss of energy production due to the shade of PV modules is investigated. In string inverter configuration, multiple PV modules are connected in series. Thus, even if only one PV module is shaded, the power output of the entire string is reduced. In the microinverter configuration, because MPPT is performed at the module level, the loss due to shading of only one module does not affect the output of the unaffected modules. In a case study of 6kWh PV system at Austin, TX, the effect of 50% and 100% shading of one module is shown in Figure 3.2 and Figure 3.3. Evaluating the exact cost of the loss of energy production due to shading effects is very complicated because the shading depends on many factors that vary by location, surrounding environment, time of day, and season of the year.

However, the probability of shading can be calculated for a specific location, and thus, the expected loss of energy production is calculated. In [57], a comparison study between a string inverter and microinverter PV systems was conducted that is intended to analyze

the impact of the shade on the amount of the generated power for residential PV system. The shading was quantified based on the site survey and categorized into three shade weighting factors; (1) light shade corresponds to 7% irradiance reduction, (2) moderate shade corresponds to 15% - 19%, and (3) heavy shade corresponds to 25%. In the same study, the advantage of the microinverter configuration has been shown by producing more power than the string inverter configuration. Under the light, moderate, and heavy shading, the microinverter generation was 3.7%, 7.8%, and 12.3%, respectively, higher than the string inverter.

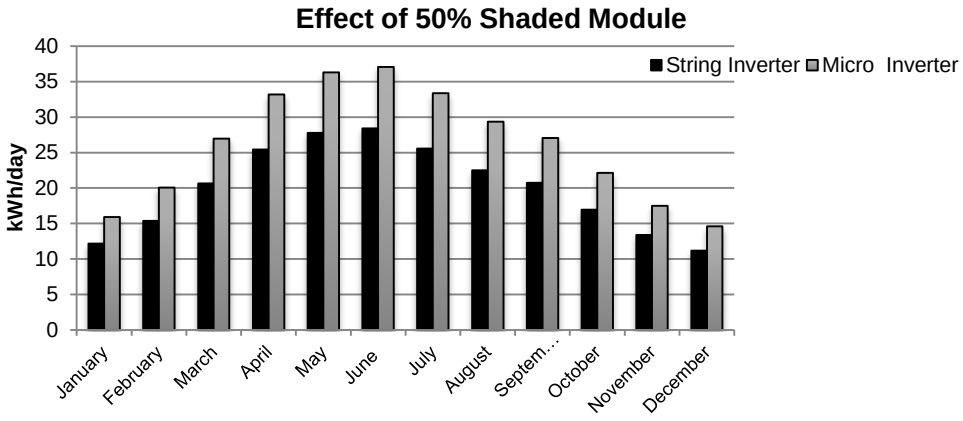

Figure 3.2: Example of partial module shading impact on the energy production for both locations (50% shading)

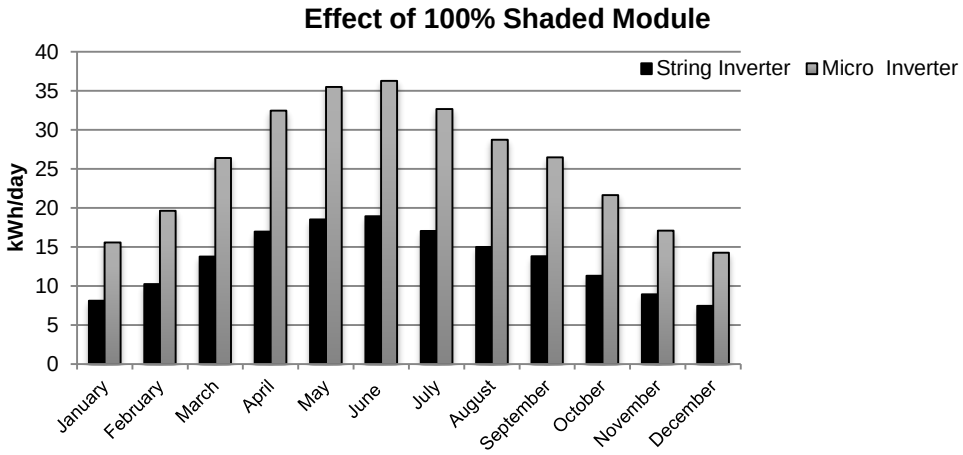

Figure 3.3: Example of complete module shading impact on the energy production for both locations (100% shading)

In this section, we present an approach to quantify the cost of the loss of energy production due to the shade effects. Similarly, shade site survey can be used to determine the shade weighting factors for a specific installation. However, the results from [57] will serve the purpose of the study in this paper, and thus, they are used to calculate the loss in energy production. First, the expected energy generated by the microinverter configuration will be calculated using the irradiance reduction percentage (r) [57]:

$$E_{micro\_SH} = (1-r)E_T \tag{3.4}$$

where: *r = 7%, 19%, and 25%*. This energy will be considered the reference value against which the energy produced by the string inverter is compared. The energy generated by

the string inverter will be less than from the microinverter by the gain factor *k* [57],

$$E_{string\_SH} = (1-k)E_{micro\_SH} \tag{3.5}$$

where *k = 3.7%, 7.8%,* and *12.3%*.

The gain in energy produced by the microinverter is calculated as

$$E_{gain} = E_{sh\_micro} - E_{sh\_string} = kE_{sh\_micro} \tag{3.6}$$

Table 3.1 summarizes the results for three shade weighting factors.

Table 3.1: The impact of the shade on the gnerated energy

Shade weighting factor	Microinverter energy (kWh)	String inverter energy (kWh)	Energy Gain of microinverter system (kWh)
Light	1,544,101	1,486,970	57,131
Moderate	1,344,862	1,239,963	104,899
Heavy	1,245,243	1,092,078	153,165

3.5 Cost

The cost of the PV system can be divided into the following categories: PV module, inverter, balance of system (BOS), installation, maintenance and repair, and lost production costs [55, 63]. Apart from the cost of the PV modules, the cost of other factors differs based on the configuration that is selected to configure the system. String inverter and microinverter configuration s are evaluated considering the aforementioned factors. The total cost of installed residential PV system, in US, is $4.36 /watt, with only $1.8/watt cost for PV module. The large difference in the cost is mainly due to the expensive labor in US [48]. The installation process for the string inverter needs a high level of electrical skills, because of the nature of the system that involves different subsystems that need to be connected together at high DC voltage, such as high voltage DC wiring, string combiner box, and DC protection circuit. On the other hand, in the microinverter configuration, the AC outputs of the inverters are connected in parallel, which is easy, safer, and needs shorter installation time. The study in [66] shows that the microinverter saves 24% of installation cost, and 11% of the system cost for 7kWH system. Moreover, the total cost of the maintenance, as a percentage of initial PV system costs, is 11% for string inverter, and only 2% for the microinverter [66]. Table 3.2 lists the BOS for each configuration along with the available retailer prices. It is worth to mention that these are the retailer prices, since it is hard to estimate the real cost.

Table 3.2: BOS retailer prices for both approaches

String Inverter		Microinverter	
Components	Cost ($/Unit)	Components	Cost ($/Unit)
Fuse PV-10A10F (DC)	$17.21	Cable (1986164-2 TYCO)	$1.01 (per foot)
Fuse PV-20A10F (DC)	$27.14	Transition Cable	$47.00
Fuse Holder (CHPV1U)	$19.64	End Caps	$2.50
Blocking Diode (SD 2510-B)	$15.00	Data Logger	$627.50
DC Disconnects (SBCD-4-40)	$260.16	Transition Box (2106916-1 TYCO)	$99.95
Cable (1986164-2 TYCO)	$1.01 (per foot)	AC Disconnects (H321DSEI)	$2,382.39
Cable Coupler (6-1394462-3-female; 6-1394461-5-male TYCO)	$2.32	Cable Coupler (6-1394462-3-female; 6-1394461-5-male TYCO)	$2.32
Sub-array Combiner Box (SPD)	$322.35		
AC Disconnects (H321DSEI)	$2,382.39		
Data Logger	$627.5		
Total	**$4,035.34**	**Total**	**$3,400.09**

To refine the cost estimate from the installer side, two quotations were obtained from Austin, TX based PV installers, for both configurations [67], as shown in Table 3.3. The microinverter configuration costs just $581.4 extra than the string inverter configuration. This extra cost can be easily compensated when the cost of loss of energy production is taken in consideration. Table 3.3 shows that the labor cost is the same for both approaches; nevertheless, few microinverter manufacturers have started producing what so called "ACPV" to reduce the installation cost to half [49, 50, 54]. In the ACPV, the microinverter is physically and electrically connected to the PV module in the factory.

Table 3.3: PV installer quotations

	Total cost	PV modules, inverter, and BOS	Labor
Microinverter approach	20,359.72	16,265.40	3,190.00
String inverter approach	19,747.18	15,684.00	3,190.00

3.5.1 Levelized cost of energy (LCOE)

The aforementioned quotations are the cost of the installed PV system, however, levelized cost of energy (LCOE) is not considered. These quotations do not include the cost of unharnessed energy due to system's failure and shading effects. In order to comprehensively evaluate the cost as well as calculate the break-even cost of the PV system, the LCOE needs to be calculated.

The calculation of the loss of energy production, due to system failure, can be divided into two main time factors: time to detect the failure and the time to repair. In the string inverter case, failures that are not related to the inverter can be easily missed, and the system continues to operate at lower power rating. In a system similar to the string system studied in this paper [68], a connector failure in one of the two strings resulted in a reduction of the harvested power to half of the expected value. This failure persisted for two months during the summer of 2012 until it was accidently discovered. Also, the repair time is very complicated to expect, it depends on the cause of failure, whether it is hardware or software failure [63]. Hence, the string inverter is considered to be replaced at least one time during the 25 years PV system's lifetime.

On the other hand, the cost of the loss of energy production due to shade effects can be calculated using the results presented in the previous section. Using the price of electricity in Austin, 0.109 $/kWh, the energy production gained by the microinverter is interpreted into cost for the three shade weighting factors, light, moderate, and heavy, as follows: $6,227, $11,434, and $16,695, respectively. If these gains are evenly distributed over the system's lifetime, then, it will be $249, $457, and $668. Since the difference between the two quotations is $581, this concludes that microinverter configuration PV system takes at most, considering light shade weighting factor, less than three years to reach the break-even cost with the string inverter configuration. It is worth to mention that the replacement cost of the string inverter has not included in the previous calculations. An average price for a 6kW string inverter is approximately $2,500. Adding this $2,500 as a replacement cost, results in making the microinverter configuration cost competitive with the string inverter at the time of installation. Another way to calculate the break-even cost is to compare the cost of the power electronics. 24 microinverters are needed to construct a 6kW PV system with $130/piece retailer price; the total is $3,120. Again, $620 will be the difference in favor of the string inverter, which will be compensated by the gain in energy harvest by the microinverter.

3.6 Safety

Safety of PV systems is becoming increasingly a concern [69, 70]. This paper compares the safety of both the string inverter and the microinverter configurations. The safety aspect of the PV system is very crucial not only because of the hazardous conditions that

could result, but also because of the potential for large financial losses. The latter can be interpreted into cost (LCOE); however, due to the lack of research in this particular topic, it is complicated to quantify the cost caused by hazardous conditions. The safety has been studied in two aspects; (1) shock hazard and (2) arc fault.

Shock hazard is related to the amount of the current flow, which depending on the voltage level, and can be lethal. In the string inverter configuration, the DC voltage can be as high as $600V_{DC}$, creating a hazardous system voltage [71]. On the other hand, the DC voltage level in the microinverter configuration is limited to the output of the PV module, which could be as high as $40V_{DC}$. Moreover, this DC voltage is connected to the microinverter either directly or by very short wires, and thus, the potential for a hazardous situation is much less. Arc faults are more likely to occur in high DC-voltage PV connection system, and can cause system fires [70]. Figure 3.4 [72] and Figure 3.5 [73] show examples of hazards and resulting damage from arcing in PV systems.

Figure 3.4: Glowing arc in the DC wiring near a combiner box [72]

Figure 3.5: Fire damage to a roof-mounted PV array [73]

Three aspects of system design contribute to the arc faults risk: high voltage, high current and large geographic distribution of AC or DC wiring. Arc faults can be divided into AC and DC arc faults based on the electrical connection. However, AC connections are less likely to sustain arcs since the current flows through zero twice per grid cycle [71]. In the string inverter configuration based PV system, 12 PV modules are connected in series to form 360VDC. Then, connecting multiple strings in parallel will increase the DC current. Besides, these PV modules with the DC distributed connection occupy a large geographic area. This combination of high voltage, high current and large DC distributed area results in increasing the probability of an arc fault to occur. Figure 3.6 illustrates possible locations for arc faults in a typical string inverter configuration PV system [70].

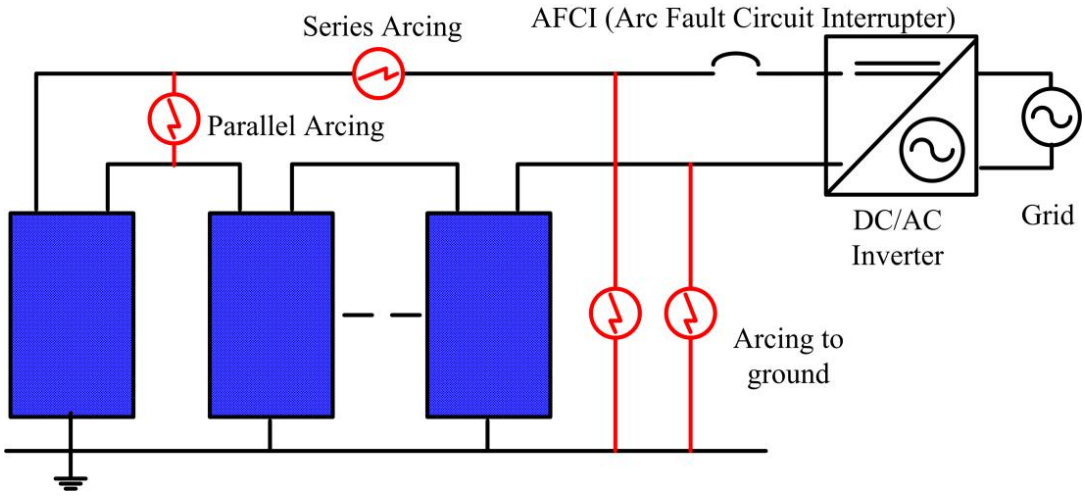

Figure 3.6: Possible arc faults locations in string inverter

Standards have been developed to address the safety issues in PV system, for example: UL1699B photovoltaic arc-fault circuit protection standard, which is a subset of the National Electrical Code (NEC 690). It defines requirements for systems with a DC bus voltage equal to or greater than 80 V_{DC} and less than 1,000 V_{DC} [70]. These standards necessitate installing necessary protection equipment to ensure the safety of the system. Hence, this leads to increase the total cost and the complexity of whole system.

In contrast, the microinverter configuration works at much lower DC voltages; the PV module output voltage of 18V to 36V for most silicon modules. With this lower DC voltage, it is harder to sustain an arc [74]. Moreover, the microinverter is physically attached to the back of the PV module, thus, the DC wiring is almost negligible. Microinverters are designed to stop operating once a fault or disconnection in the wiring is detected. However, quantifying the cost associated with the extra safety requirements is difficult due to two main reasons: (1) the safety of PV system is new topic, and has not been thoroughly studied yet; (2) the protection equipment technology is still immature and different technologies have been proposed recently.

3.7 Conclusion

Two different power electronics configurations for PV system, string inverter and microinverter, are examined and compared in this paper. Reliability, availability, safety, failure, and cost of both configurations were compared. The additional energy harvest of the microinverter was found to give it an economic advantage over the expected lifetime of the PV system, particularly when the cost of replacing the string inverter is taken into

account. The microinverter also offers safety advantages, which have not previously been monetized into the LCOE calculations.

4 DOUBLE-FREQUENCY POWER FLOW IN SINGLE-PHASE SYSTEMS *

In grid-connected PV applications, electrical isolation is necessary for safety issues [8]. In terms of the operating frequency of the isolation transformer, the microinverter configurations can be categorized into two basic groups: (1) isolation with a line frequency transformer; and (2) isolation with a high frequency transformer. Since the line transformer is bulky and costly, it is not recommended for microinverter applications. In this section, we focus on microinverter configurations that employ high frequency transformer. Microinverter configurations with high frequency transformer fall into three basic categories based on the dc link configurations[9]: DC link, pseudo DC link and high frequency AC, as shown in Figure 4.1.

As seen in Figure 4.1(a), in the DC link implementation, DC-DC converter is designed to implement the Maximum Power Point Tracking (MPPT) and amplify the PV DC voltage to a sufficient voltage level compatible with the grid. Any DC-DC topology that provides galvanic isolation can be the candidate for the DC-DC stage. Figure 4.1(b) shows the microinverter configuration with the pseudo DC link, where the voltage is expected to be rectified-sine waveform, and the unfolding inverter, operating at line frequency, converts the rectified sine waveform into the sine waveform. In this configuration, the power decoupling capacitor cannot be placed on the DC link. It is placed on the PV-side

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instead, and usually this results in a large capacitance due to the low DC level and the need for ripple-free voltage on the PV-side.

If we replace the rectifier circuit on the secondary side with the cyclone converter, a new configuration without the DC link is derived, as illustrated in Figure 4.1(c). In this case, the cyclone converter directly converts the high frequency AC into the desired line frequency AC output. As for the power decoupling capacitor, in this case usually it is placed on the PV-side, which is similar to the previous case, and a large capacitance is needed. However, the power decoupling capacitor can be placed on the AC side, and consequently, a very small capacitance is needed for the same power ratings.

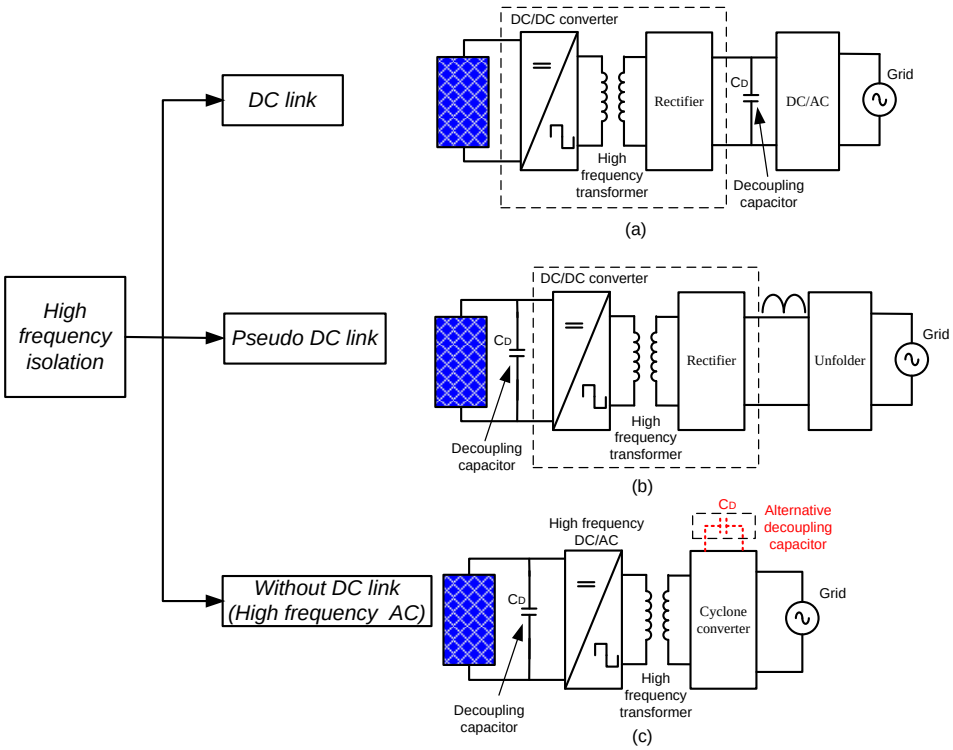


Figure 4.1: Basic microinverter's configurations

This section presents the double-line frequency issue that is inherent in the single-phase conversion systems. Also, it scrutinizes the various power decoupling techniques that have been proposed and compares their performance in terms of efficiency, cost, and control complexity. Although the following analysis is based on the single-phase, grid-connected PV system, shown in Figure 4.2, but the result or the effect is similar for a single-phase rectifier system.

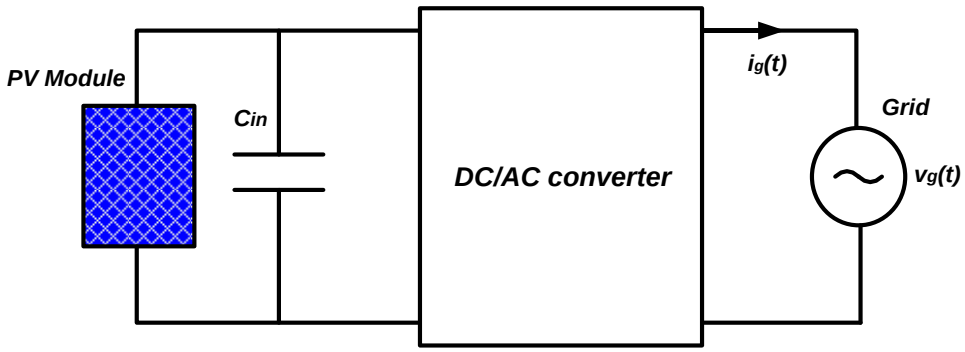


Figure 4.2: Single-phase grid-connected PV system

4.1 Double-line frequency ripple

In a single-phase, grid-connected system, the injected current to the grid is given in (4.1) and the grid voltage is given in (4.2).

$$i_g(t) = I_g \sin(\omega_0 t + \varphi) \tag{4.1}$$

$$v_g(t) = V_g \sin(\omega_0 t) \tag{4.2}$$

where ω_0 is the grid frequency and φ is the phase difference between the injected current and the grid voltage, which is desired to be zero for unity power factor operation. Then, the instantaneous output power, $p_0(t)$, is given as follows:

$$p_0(t) = v_g(t) * i_g(t) \tag{4.3}$$

$$p_0(t) = \frac{1}{2} V_g I_g \cos(\varphi) + \frac{1}{2} V_g I_g \cos(2\omega_0 t + \varphi) \tag{4.4}$$

when the phase shift (φ) is zero, then the expression for $p_0(t)$ in (4.4) is reduced to (4.5)

$$p_0(t) = \frac{1}{2} V_g I_g + \frac{1}{2} V_g I_g \cos(2\omega_0 t) \tag{4.5}$$

The output instantaneous power in (4.5) consists of two terms: the average output power $P_{0\_av}(t)=\frac{1}{2}V_g I$, which is constant, and the second time varying term (pulsating power) $p_{0\_ac}(t)=\frac{1}{2}V_g I\cos\left(2\omega_0 t\right)$, which oscillates at twice the line frequency. On the other hand, the power from the PV module is controlled by the maximum power point tracking (MPPT) system and kept constant, $P_{PV}=P_{dc}$. By neglecting the losses in the power stage, the power generated by the PV module will be equal to the average output power, P_{0_av}, as shown in Figure 4.3.

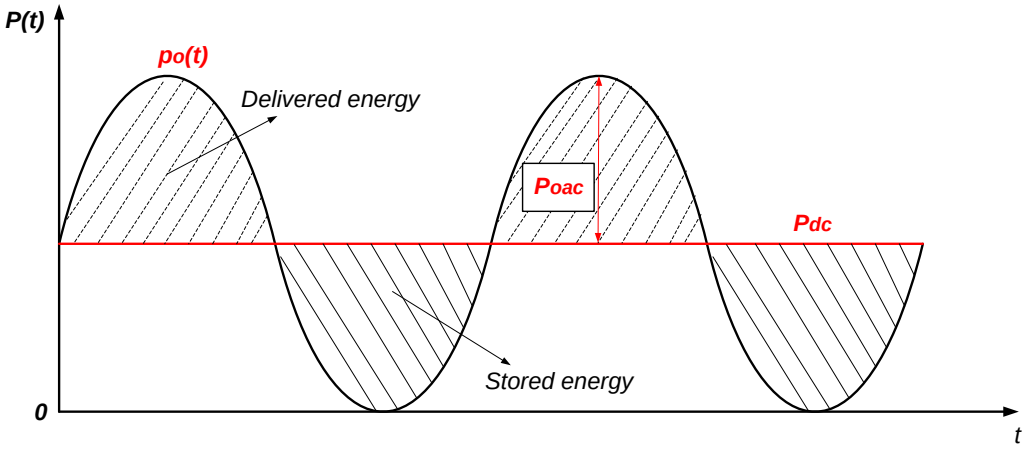


Figure 4.3: The total power processed by the decoupling capacitor

4.1.1 The effects of the double-line frequency ripple

The time varying term will degrade the PV system performance. This ripple has a strong negative impact on the MPPT performance, where MPPT is trying to track the voltage and

current that result in the maximum output power from the PV module, as shown in Figure 4.4. Having these time varying components (voltage and current) reflected on the terminals of the PV module will deteriorate the MPPT performance, and as a result, the overall energy conversion efficiency is decreased by 50% [8]. To maintain power-balance, the pulsating power, $P_{oac}=P_o-P_{dc}$, must be handled by an energy storage device. Usually, a capacitor "*Decoupling Capacitor*" is used to mitigate the power ripple effect at the PV-Module side [75]. This decoupling capacitor can be embedded within the inverter stage or just connected in parallel with the PV-Module.

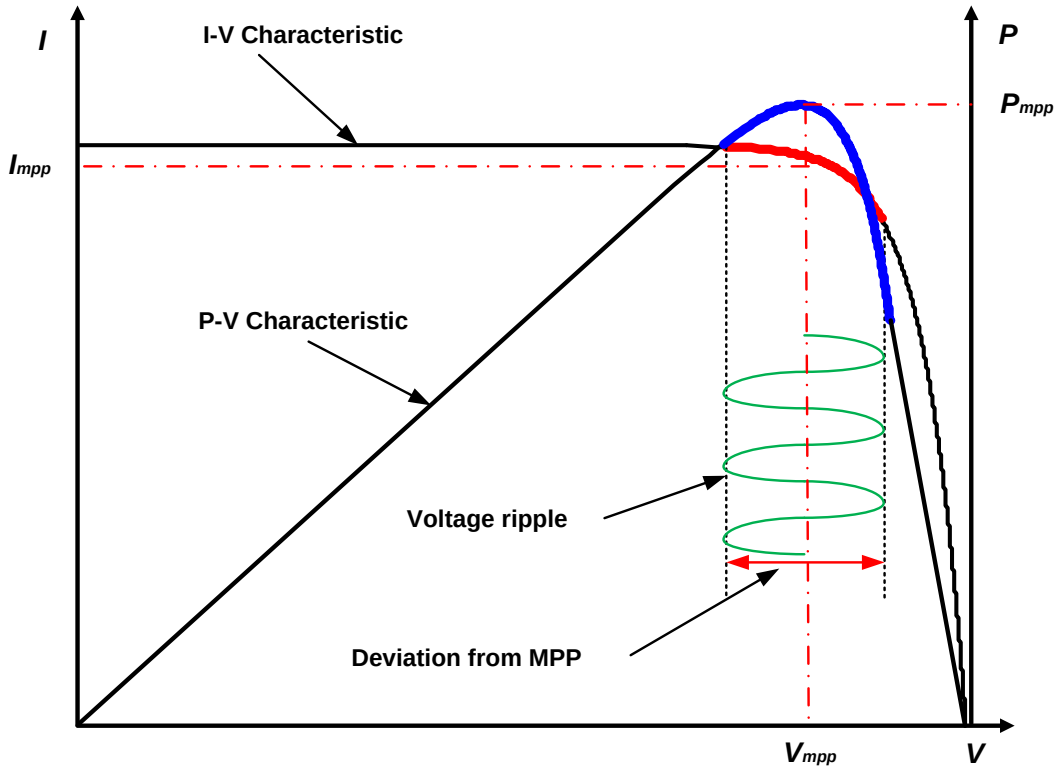


Figure 4.4: I-V and P-V characteristic of a PV module

The energy that is being charged to or discharged from the decoupling capacitor during a half line cycle can be calculated by integrating one of shadowed areas in Figure 4.3.

$$E_{CD} = 2(\int_0^{\frac{1}{8 f_{grid}}} (P_{dc} - P_o(t))dt) = \frac{1}{2} C_D (V_{dc\_\max}^2 - V_{dc\_\min}^2) \tag{4.6}$$

where f_0 is the line (grid) frequency, and V_{dc_max} and V_{dc_min} are maximum and minimum voltages across the decoupling capacitor.

Combining (4.5) and (4.6), the required decoupling capacitance is found to be as follows:

$$C = \frac{P_{dc}}{2\pi f_0 V_{dc} \Delta v} \tag{4.7}$$

where V_{dc} is the DC voltage level and Δv is the allowed voltage ripple across the capacitor's terminals. It is obvious that by increasing either V_{dc} or Δv or both, the needed decupling capacitance, to cancel the double-line frequency, decreases. However, this will impose a higher voltage stress on the semiconductors, and thus, a compromise design should be carried out.

Usually, a capacitor is used to serve as a power decoupling element. However, the lifetime of different types of capacitors varies greatly, e.g. electrolytic capacitors typically have a limited lifetime, namely 1000~7000 hours at 105˚C operating temperature [45]. Most of presently available commercial microinverter s use electrolytic capacitors as power decoupling storage element due to their large capacitance and ease of implementation, which tend to limit the lifetime of the microinverter [11, 53, 76, 77]. Some researchers have explored various ways to reduce the size of the required capacitance so as to allow for other longer lifetime capacitor technologies, such as film capacitors, to be used. In the next section, different power decoupling techniques are presented, categorized, and compared in terms of efficiency and performance.

4.2 Power decoupling techniques

Different topologies and techniques have been proposed in the last decade that tackle the double-line frequency issue, and enhance the reliability of the single-phase converters. These topologies and techniques are presented in this section, and they will be categorized into three different categories based on the place of the decoupling capacitor. Advantages and disadvantages of each of these topologies will be discussed as well.

Based on the micro inverter configuration that is being employed, different power decoupling techniques can be implemented. As it was shown in the previous section, microinverter topologies can be divided into three groups, according to the DC link configurations. Usually, the pseudo DC link configurations are referred to as single-stage inverters since the second stage is just unfold the rectified low-frequency DC signal; hence

it is called “unfolder”. And, the decoupling capacitor can only be placed on the DC side. Other configurations are considered multi-stage inverters. The single stage inverters, as shown in Figure 4.5, accomplish both tasks: boosting the input voltage, and sine or rectified sine waveform modulation. In this case, the only way to employ the power decoupling capacitor is to place it on the DC (PV) side.

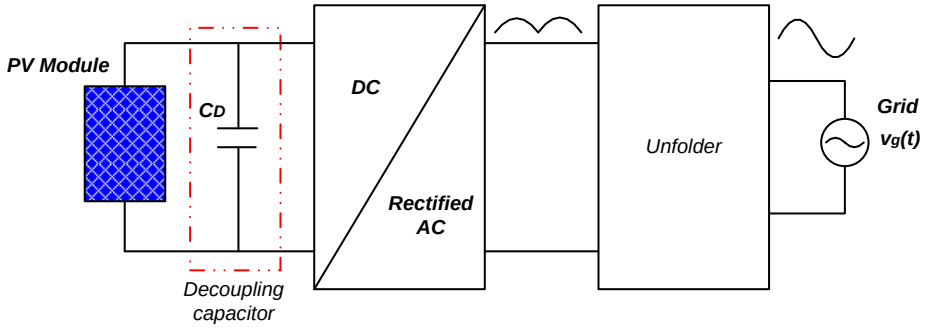
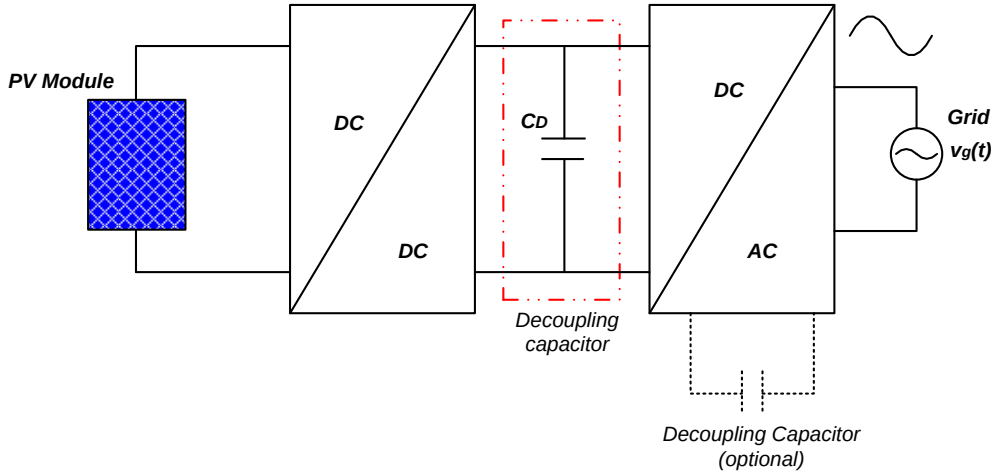
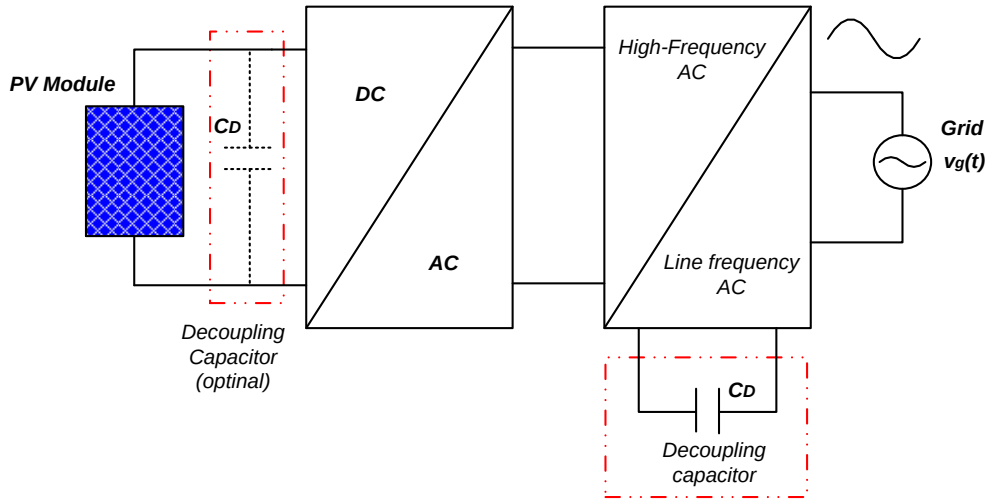


Figure 4.5: Single stage inverter



(a) DC-Link approach



(b) AC-Link approach

Figure 4.6: Multi-stage inverter

On the other hand, multi-stage inverters can be further classified into DC-AC-DC-AC and DC-AC-AC, as shown in Figure 4.6. For the topologies with DC-AC-DC-AC configurations, the first power stage usually is used to boost the low PV DC-voltage to a high DC voltage level compatible with the grid voltage, as well providing electrical isolation. In this case, it is recommended to place the decoupling capacitor at the high

voltage DC link, which will reduce the required decoupling capacitance, according to (4.7). By adding several active switches and reactive components, the decoupling capacitor can also be placed on the AC-side. Cycloconverters (or matrix) changing high frequency AC to line frequency AC, are used in topologies with DC-AC-AC implementation, in which the power decoupling capacitor can only be placed on the PV side or on the AC side. Detailed description and analysis are given in the following subsections. The inverter topologies can be categorized based on the location of the decoupling capacitor and associated circuitry, as shown in Table 4.1. However, in this study only the most three viable decoupling techniques options will be investigated, namely, (1) PV side decoupling (IA1 and IB2); (2) DC link decoupling (IIA1); and (3) AC side decoupling (IIIB2).

Table 4.1: Power decoupling techniques based on the place and the type of the capacitor (Decoupling taxonomy)

Type – Decoupling Technique		A- Electrolytic Capacitor	B- Film Capacitor
Type I – PV side	1- Passive circuit	Very Large capacitor Low lifetime	Not cost effective Very large capacitor
	2- Active circuit	Extra components – no valuable improvement	Extra components
Type II – DC-link	1- Passive circuit	large capacitor Low lifetime	Not cost effective large capacitor
	2- Active circuit	Extra components – no improvement	Extra components
Type III – AC side	1- Passive circuit	Not feasible	Not feasible
	2- Active circuit	Not feasible	Extra components Minimum required capacitance

4.2.1 DC side decoupling

In a single stage microinverter configuration as shown in Figure 4.5, having the power capacitor on the DC-side (across the PV module terminals) results in a very large capacitor since the allowable voltage ripple must be kept to very low values (<1%) in order to achieve high MPP efficiency [8, 75]. For example, for a 200W microinverter , the minimum decoupling capacitance required is 13.9mF in order to achieve a 98% PV utilization factor [8]. This represents a very large value, which increases the size of the microinverter. More importantly, the large electrolytic capacitor negatively impacts the lifetime of the microinverter. One potential solution is to add an auxiliary circuitry, between the PV module and the inverter, to decouple the AC pulsating power while maintaining the MPP voltage stable, as shown in Figure 4.7.

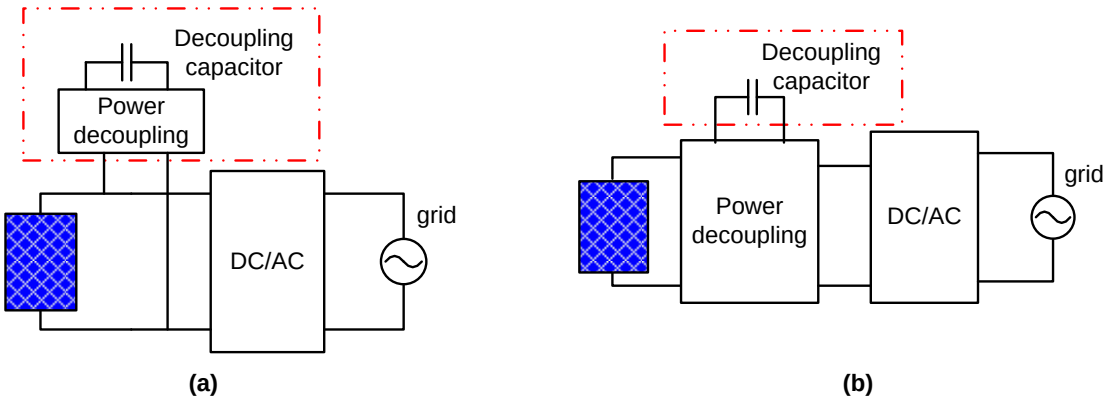


Figure 4.7: Employing power stage to realize power decoupling on the PV side

A bidirectional buck-boost converter was proposed in [78] to realize the power decoupling as shown in Figure 4.8. With this active filter technique, the decoupling capacitor C_d is reduced from 3000uF to 100uF by increasing the average voltage and ripple voltage across the decoupling capacitor to 62V and 35V, respectively. As shown in Figure 4.9 the average current i_2, injected to the grid, is a rectified sinusoidal waveform. To maintain the input current, I_{DC}, constant, the buck-boost current, i_3, should be complementary to the current i_2 with the offset I_{DC}. Based on the current direction, the buck-boost converter has two operation modes. In buck mode, the energy stored in the decoupling capacitor is released to the grid, while in the boost mode; the surplus power from the PV source is stored to the decoupling capacitor. Current hysteresis control is employed to control the current and make it follow a given reference. Although in [78] no specific number regarding the overall inverter efficiency is mentioned, the power losses associated with the decoupling circuit will reduce the overall efficiency. Moreover, using a smaller decoupling capacitor leads to higher stresses on the power devices, which may result in more losses and lower efficiency. Similar concept is also found in other applications [79, 80].

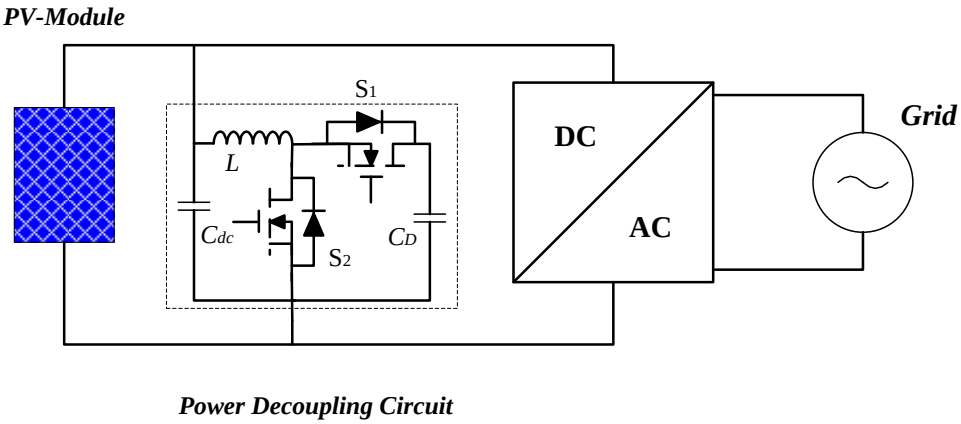


Figure 4.8: Topology proposed by Kyritsis, *et al* [78]

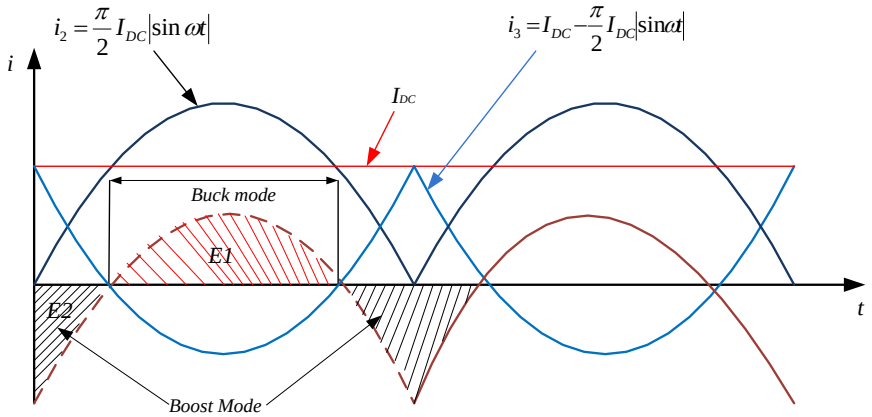


Figure 4.9: Power decoupling control strategy

The topology shown in Figure 4.10 is a flyback type single-stage microinverter with a decoupling power circuit, in which a 40uF film capacitor was used for a 100Watt system. In this topology, the constant power from PV is first transferred to the decoupling capacitor C_D, which is then modulated with a rectified sine waveform and injected into the grid. As shown in Figure 4.11, the power from PV first is charged to the flyback transformer and

then is released to the decoupling capacitor, C_D. After that, the energy stored in C_D will be injected to the grid in a sinusoidal form. Given the cascaded conversion process, the projected efficiency will be low, as indicated in [44], where 70% is achieved as the peak efficiency.

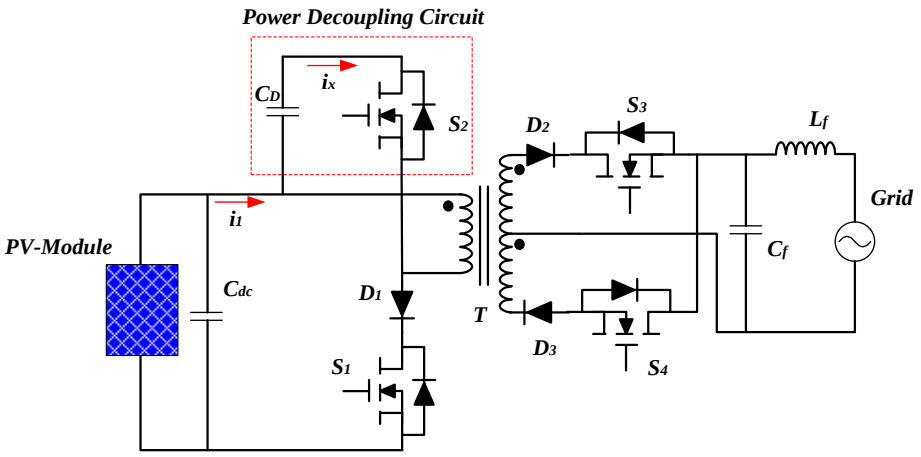


Figure 4.10: Topology proposed by Shimizu, *et al* [44]

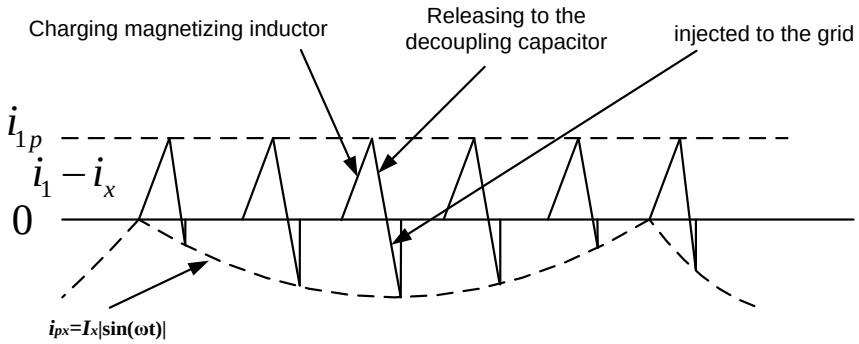


Figure 4.11: Magnetizing currents at primary side

Figure 4.12 shows a modified topology in [39], where the leakage inductance energy is recycled using a "dual-switch flyback converter". As shown in Figure 4.13, the energy from PV is stored in the magnetizing inductor by switching ON S_{sync} and S_{BB} simultaneously. Then the energy in the magnetizing inductor is discharged into the decoupling capacitor through D_1 and D_2 once the switches S_{sync} and S_{BB} turn OFF. When the switches S_1 and S_2 turn ON at the same time, the decoupling capacitor, C_D, discharges the required amount of energy back into the magnetizing inductor, which will be injected into the grid. Even with design optimization, the estimated peak efficiency is 86.7% according to [39].

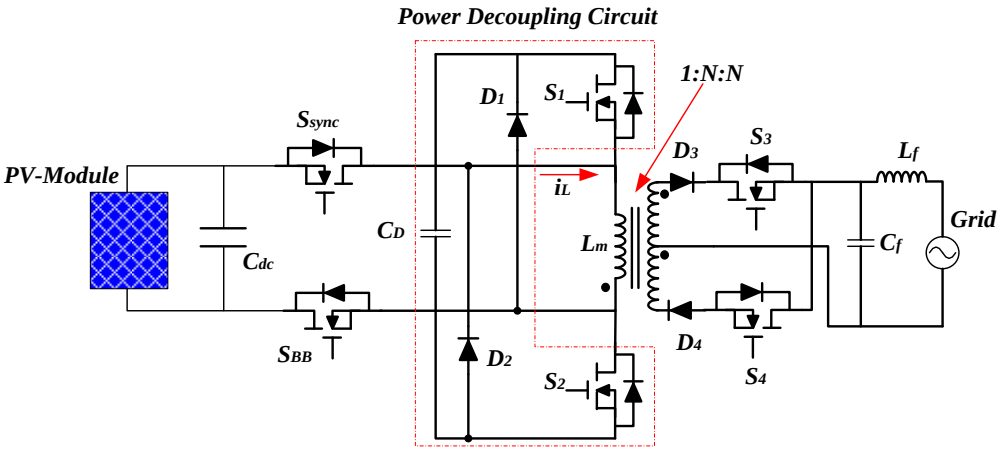


Figure 4.12: Modified topology proposed by Kjaer, *et al* [39]

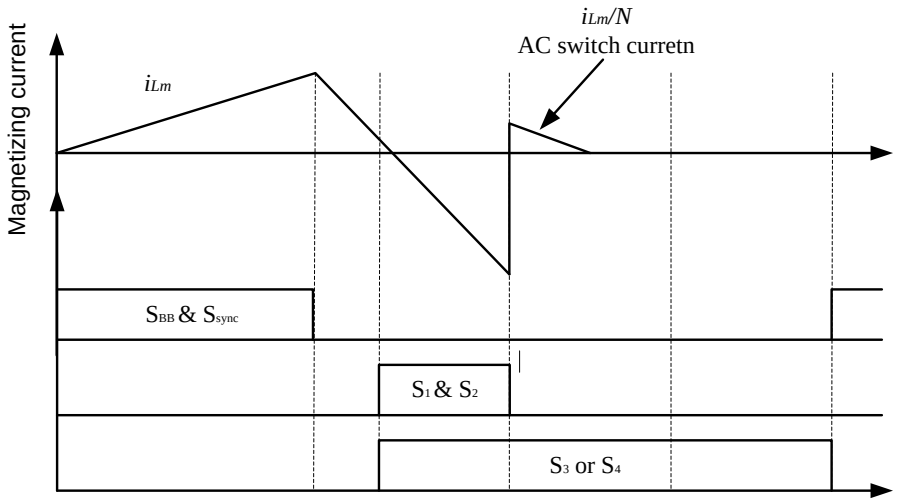


Figure 4.13: Key waveforms in one switching cycle

The authors in [37, 81] proposed three-port flyback topologies with one port dedicated for the power decoupling function, as shown in Figure 4.14 and Figure 4.15. The power decoupling capacitor (C_D) serves both as an energy storage element and as a snubber to recycle the leakage energy. For a 100W inverter, the decoupling capacitance can be as low as 46uF with an average voltage 150V and 40V ripple across the decoupling capacitor. The operation principle of these two topologies is quite the same, whose key waveforms is illustrated in Figure 4.16, except that the peak magnetizing current in Figure 4.14 is constant while in Figure 4.15, the peak value is constant in mode I and is variable in mode II. These two topologies have two operation modes: In mode I, the input power is larger than instantaneous output power, the surplus energy from PV is charged into C_D. In mode II, the input power is less than the instantaneous output power, the power from the C_D compensates the deficit power by switching ON the S_2. By operating the converter in DCM (Discontinuous Conduction Mode) mode, the peak efficiency can reach as high as

90.6%, including auxiliary power consumption [37].

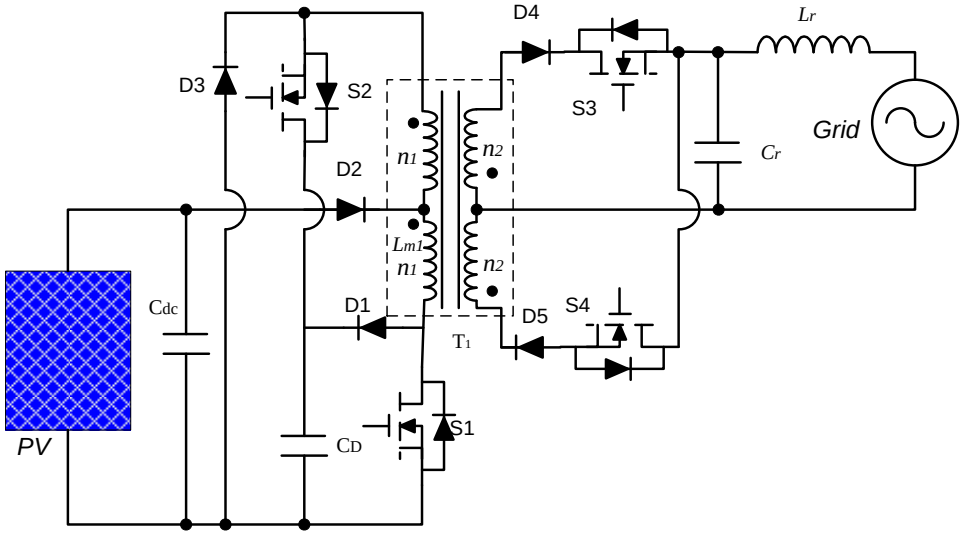


Figure 4.14: Topology proposed by Hu, *et. al* [82]

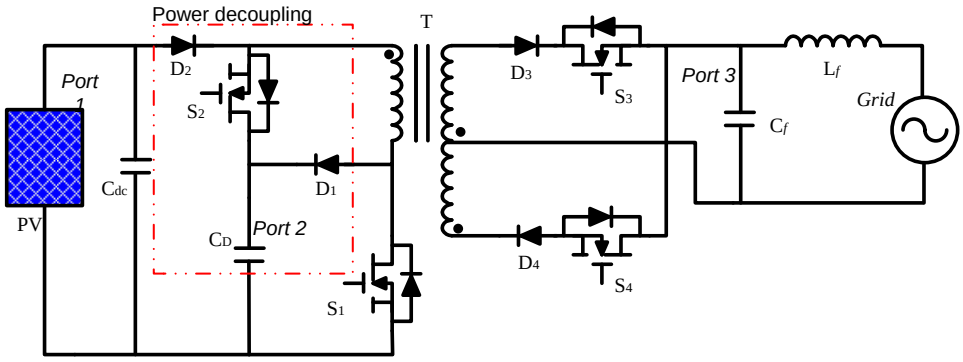


Figure 4.15: Topology proposed by Harb, *et. al* [83]

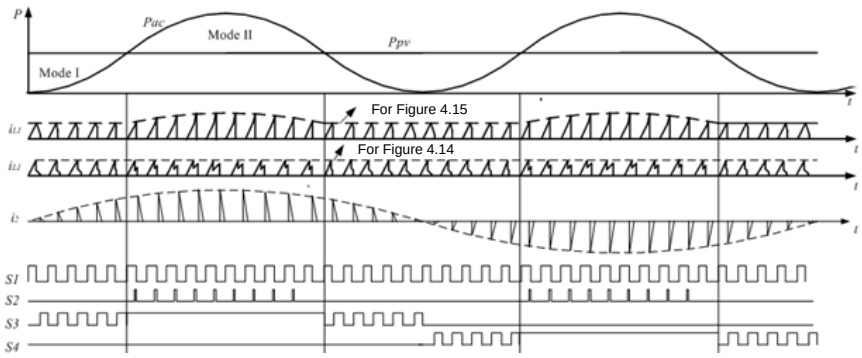


Figure 4.16: Key waveforms for topologies in Figure 4.14 and 4.15

Figure 4.17 shows a novel microinverter with power decoupling capability, which is composed of a push-pull type forward converter, an unfold inverter, and a decoupling circuit depicted in a dotted-line area [84].For a 500W microinverter , the decoupling capacitance (C_X) is as small as 50uF in simulation with a voltage ripple, across its terminals, around 100V. As shown in Figure 4.18, the topology has two operation modes. In mode I, the surplus power is charged to the decoupling capacitor by turning ON the S_{x0} and the switch S_{m1} or S_{m2} turns ON alternatively to inject the power into the grid. In mode II, besides the power transfers from the PV source directly to the grid by turning ON the S_{m1} or S_{m2}, the decoupling capacitor (C_X) also injects its energy, which was stored in mode I, into the grid by turning ON the S_{x1} or S_{x2}. The reported conversion efficiency is 95% [84].

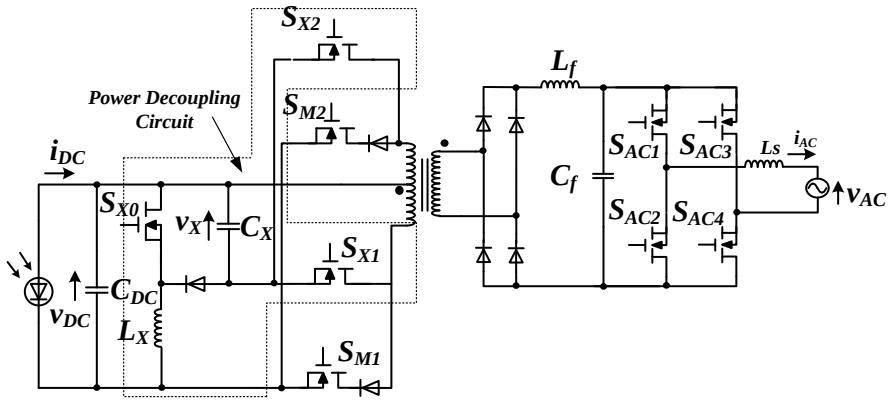


Figure 4.17: Topology proposed by Shinjo, *et. al* [84]

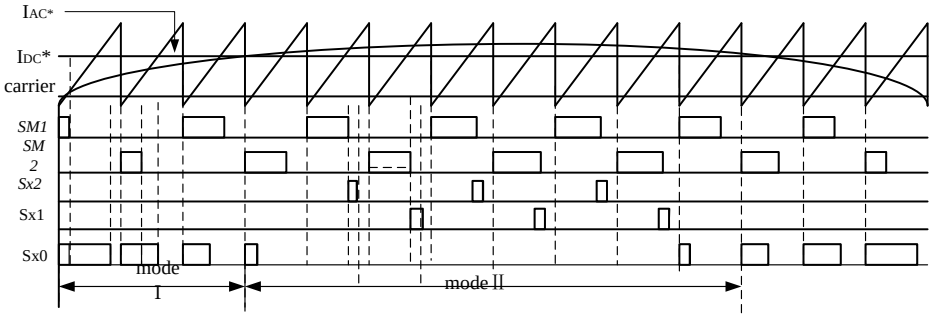


Figure 4.18: The driver signal for the topology in Figure 4.17

Another flyback-based microinverter is proposed in [85], as shown in Figure 4.19. A Time-shared Magnetizing Modulation (TMM) method is employed to avoid double power conversion, as illustrated in Figure 4.20. The operation principle is similar to the topologies shown in Figure 4.14 and 4.15. The decoupling capacitor only stores surplus power from the PV in mode I and releases the deficit power in Mode II, which results in higher conversion efficiency in comparison to those in [39, 44]. Although the proposed

topology and method can improve the conversion efficiency, the efficiency only increases from 65% to 73%, which is still too low from practical point view [85].

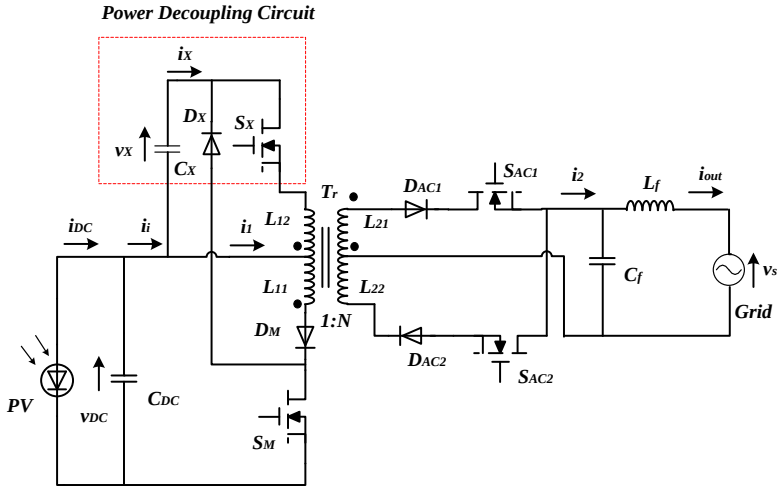


Figure 4.19: Topology proposed by Hirao, *et al* [85]

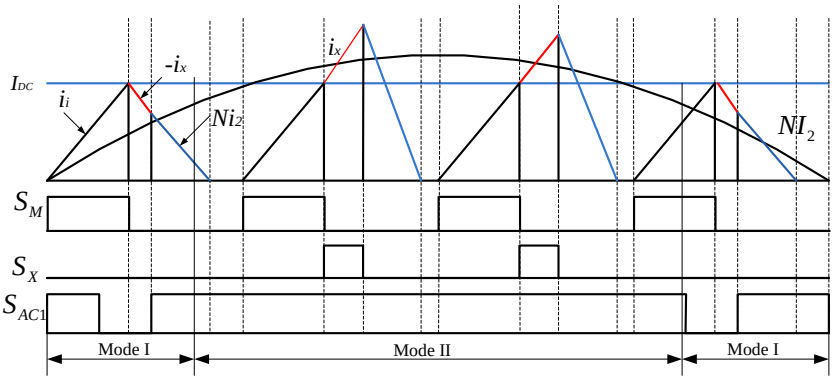


Figure 4.20: Magnetizing current and driver signals for the topology in Figure 4.19

In [86], an additional winding and an active power decoupling circuit was added to the conventional flyback converter, as shown in Figure 4.21. As shown in Figure 4.22, in mode I, the surplus power from PV source is charged to the decoupling capacitor (C_3) through the third winding and two switches S_{M4} and S_{M6}. In mode II, the energy stored in C_3 is delivered to the magnetizing inductor by turning ON S_{M5} and S_{M3}, which will provide the deficit power. Only 40µF decoupling capacitor is used for 200W microinverter system, and the voltage ripple across C_3 can reach as high as 100V [86]. In [87], a new flyback-based microinverter is proposed, as shown in Figure 4.23, that uses a boost converter to store the energy in the decoupling capacitor, (C_d) in one mode, and then release this energy to magnetizing inductor through S_2 during the other mode [87]. The operation modes are illustrated in Figure 4.24. In Mode I, the power delivered to the grid is controlled by turning ON S_3, while the surplus power is charged to the decoupling capacitor by turning ON S_1. In mode II, after the switch S_1 turns OFF, the magnetizing current continues to be charged by switching ON S_2 until the energy exactly equals the required energy by the AC side.

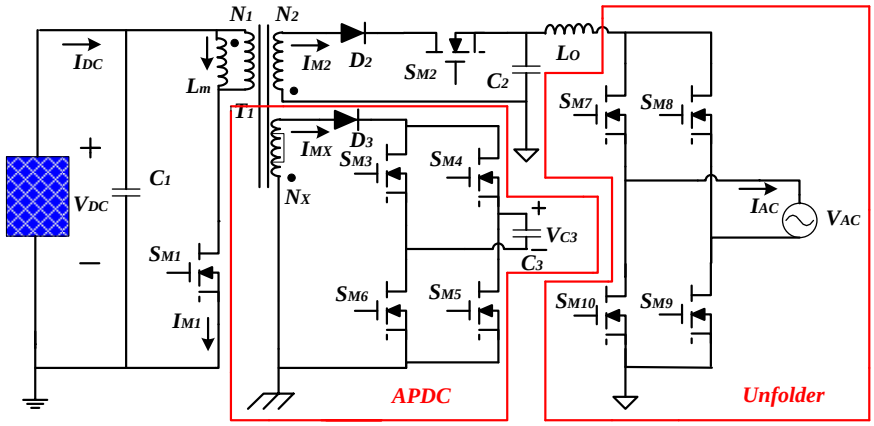


Figure 4.21: Topology proposed by Chen, *et. al* [86]

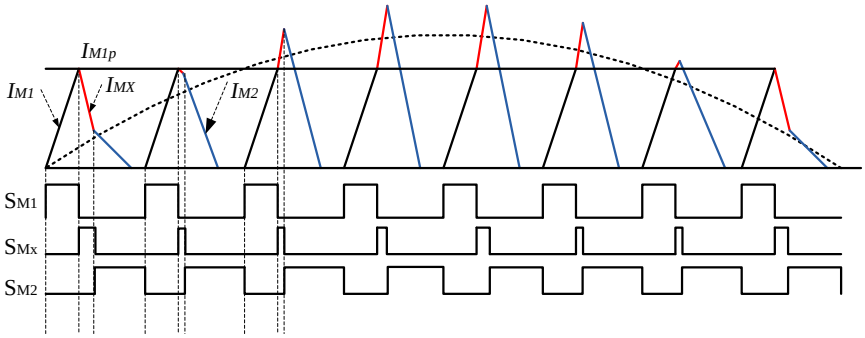


Figure 4.22: Key waveform for topology in Figure 4.21

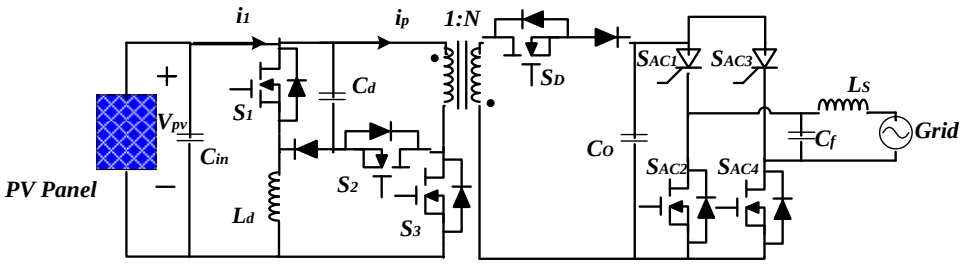


Figure 4.23: Topology proposed by Li, *et. al* [87]

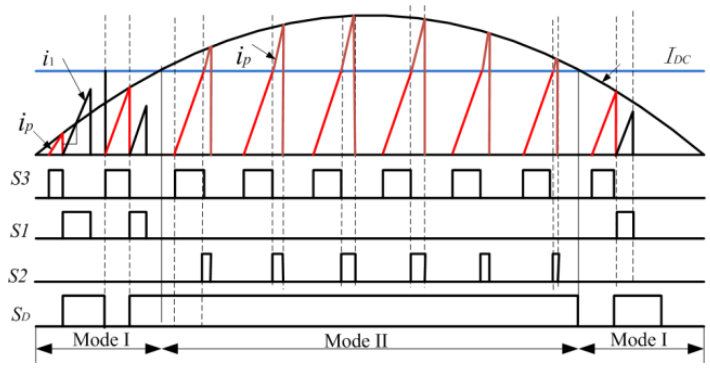


Figure 4.24: Operation modes and driving signals for the topology in Figure 4.23

In [88], the author combined the boost and flyback topologies and proposed a new topology that is capable of implementing power decoupling with smaller capacitance, as shown in Figure 4.25. The basic operation waveforms for the proposed topology are shown in Figure 4.26. The energy stored in the decoupling capacitor (C_d) is delivered to the grid through the forward converter when S_2 turns ON. When S_1 turns ON, the source (V_{PV}) charges the inductor (L_1) and when the S_1 turns OFF, this stored energy in L_1 is transferred to the decoupling capacitor. It can be viewed as a two-stage power conversion with first stage for processing the DC power from PV, and the second stage for implementing the AC power modulation. Using this technique, the size of the decoupling capacitor will be reduced due to the relatively high voltage level and voltage ripple allowed across its terminals.

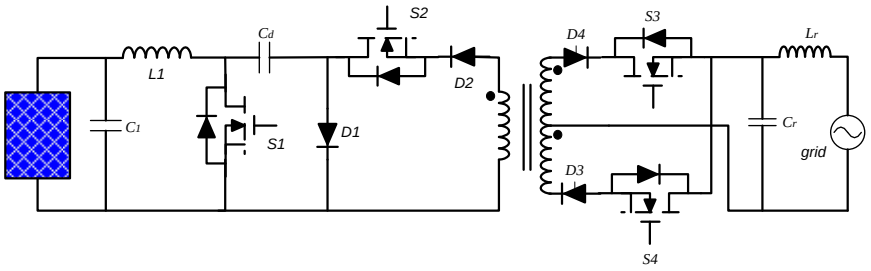


Figure 4.25: Topology proposed by Tan, *et. al* [88]

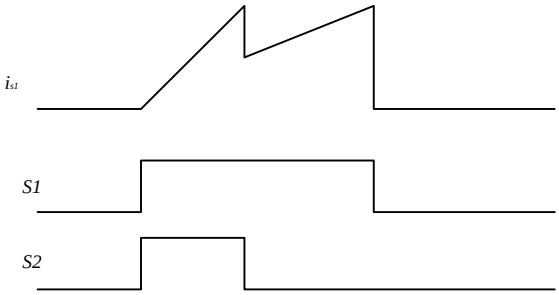


Figure 4.26: Key waveforms for the topology in Figure 4.25

4.2.2 DC-link decoupling

For multi-stage microinverter design, the main power decoupling capacitor is placed on the high voltage DC link, as shown in Figure 4.6(a). Unlike PV side decoupling, where the PV nominal voltage is relatively low and the voltage ripple should be limited to a very small range in order to maximize the energy harvest from the PV, DC link decoupling allows for a higher DC link voltage as well as a higher voltage ripple voltage. Thus, this leads to a smaller decoupling capacitance according to (4.7).

Although increasing the DC link level and voltage ripple leads to reduce the value of

decoupling capacitance, the minimum voltage across its terminals must be higher than the peak value of the output grid voltage, as shown in Figure 4.27 [89]. More specifically, the instantaneous DC link voltage must be greater than the instantaneous AC voltage as illustrated in Figure 4.28, otherwise the inverter would malfunction [90]. Detailed explanation and calculations on how to select the DC capacitance is given in [91]. The authors in [92] used this concept to minimize the DC link capacitance in AC/DC application, and also proposed a third-harmonic injection method to further reduce the size of the capacitance by compromising the power factor and capacitance [79, 93].

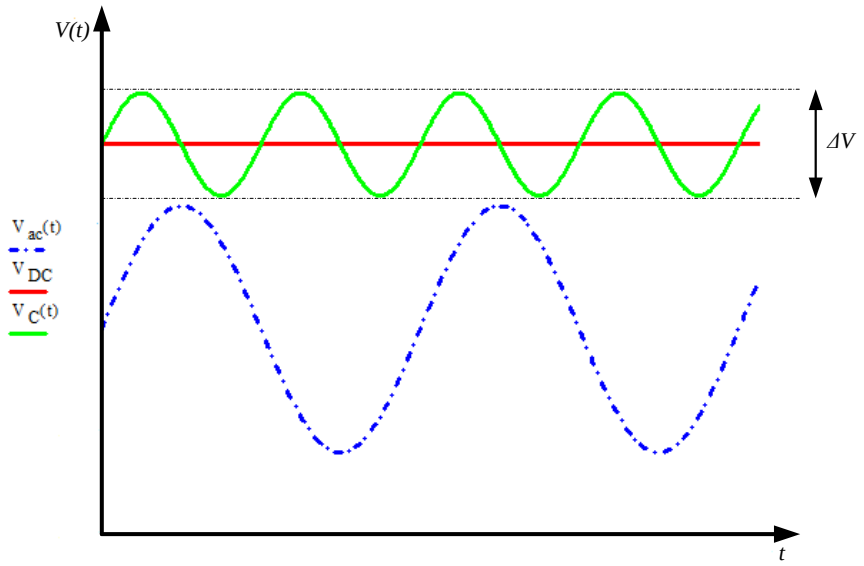


Figure 4.27: DC link voltage and the output AC voltage waveforms [89]

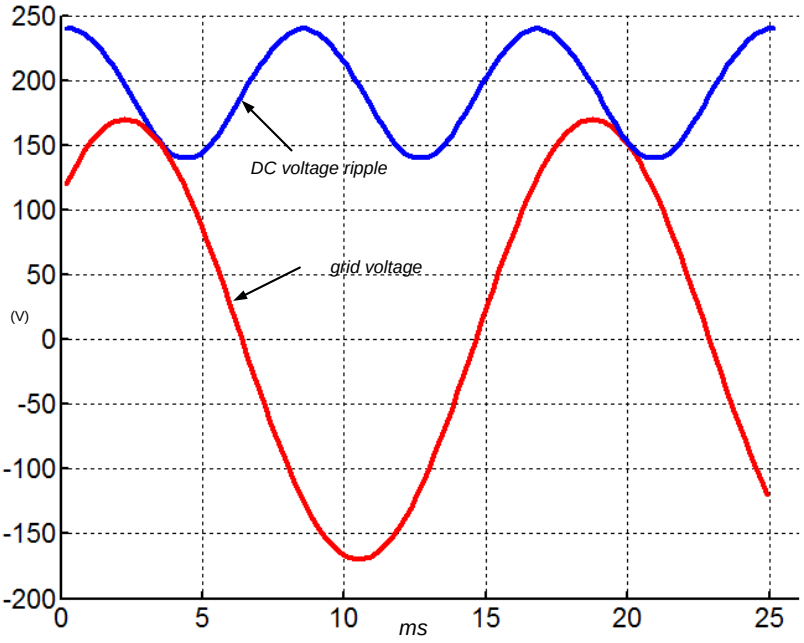


Figure 4.28: Allowed maximum DC voltage ripple [90]

Having a large voltage ripple across the DC link may result in deteriorating the output current waveform. To resolve this issue, several control techniques have been proposed. A simple method to mitigate the DC voltage ripple impact is to decouple the DC voltage, as proposed in [94], in which a modified modulation strategy to reject the DC-link voltage ripple in the control system is proposed. The proposed control scheme is illustrated in Figure 4.29. In [95], a control technique is proposed, shown in Figure 4.30, that allows for 25% ripple voltage without distorting the output current waveform. In this design, the voltage loop cutoff frequency was designed at 10Hz, greatly attenuating the double line frequency DC voltage ripple in the control loop. However, with such low cutoff frequency, the proposed control system degrades the system dynamic performance.

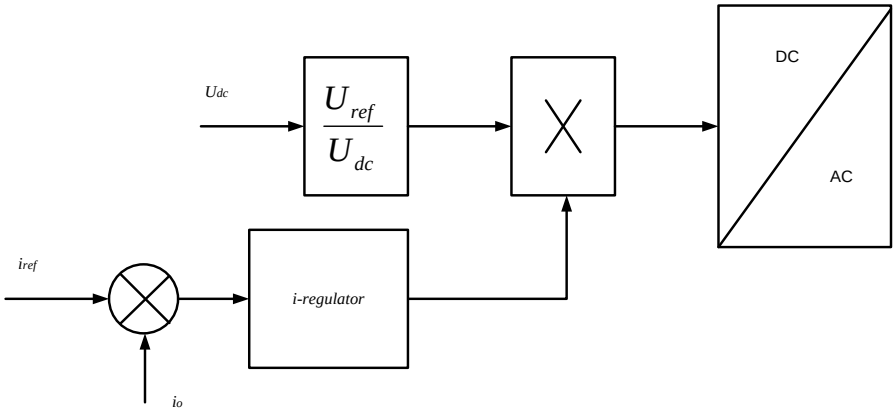


Figure 4.29: Modulation technique proposed by Enjeti, *et. al* [94]

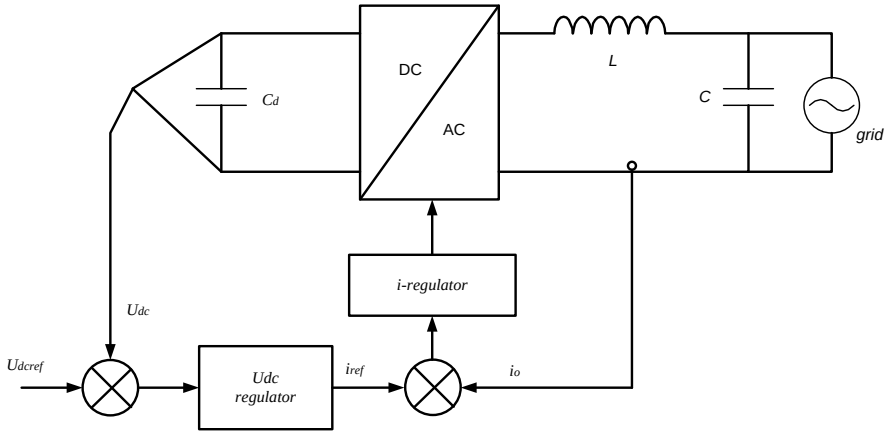


Figure 4.30: Control scheme proposed by Brekken, *et. al* [95]

To achieve a higher bandwidth for the voltage control loop, the authors is [96] proposed a DC voltage ripple estimation control strategy, as shown in Figure 4.31. In the proposed strategy, no DC voltage ripple is fed to the DC voltage regulator. This is done by subtracting DC voltage from the estimated voltage ripple. The authors in [97] proposed a predictive DC voltage regulator, based on the power balance and the relationship between

energy and DC capacitor voltage, to achieve low current distortion on the AC side and high voltage ripple on the DC link. The detailed design on how to maintain the constant current draw from PV source and inject power into the grid with unity power factor, while allowing the 25% DC voltage ripple of the rated DC link voltage is presented in [95]. In this way, the DC voltage regulator can achieve a faster transient response. The authors in [75, 98, 99] follow the same concept to allow the voltage ripple as large as possible, while make the injected current acceptable in terms of THD.

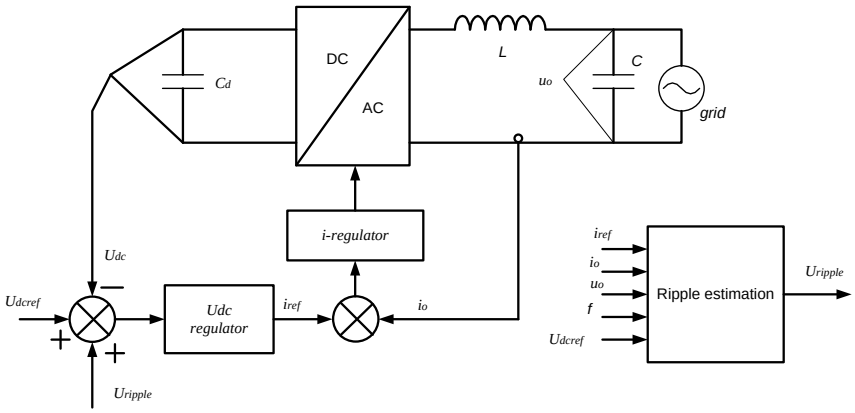


Figure 4.31: Voltage-ripple estimation strategy for large DC ripple proposed by Ninad*, et. al* [96]

4.2.3 AC side decoupling

In AC side decoupling techniques, the decoupling capacitor is usually embedded in the inverter stage itself. Because of the high voltage swing on the AC side, the capacitor value can be very small, and a non-polarized (film) capacitor can be used. In topologies that

employ this kind of power decoupling, bi-directional switches are required to provide a path for the positive and negative current polarity. The possible integration of the bi-directional switch and its driver circuitry could simplify these topologies, and enhance the overall system reliability. Two topologies that employ AC side decoupling are shown in Figure 4.32 and Figure 4.33 [100, 101]. The concept in both topologies is quite similar. An additional phase leg is added to the AC-side to accommodate the decoupling capacitor between the inverter and the grid. Both topologies are based on the current source inverter (CSI) implementation. Authors in [102, 103] proposed a voltage source inverter (VSI) with additional phase leg for compensating the pulsating power in single-phase AC/DC applications, as shown in Figure 4.34 and Figure 4.35. Although the topologies are different, the principle of power decoupling on the AC side is quite the same, and can be applied to DC/AC applications as well.

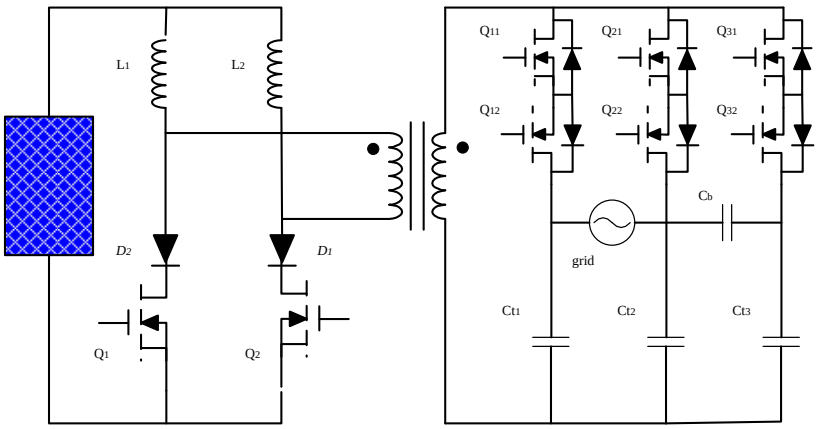


Figure 4.32: Topology proposed by Li, *et. al* [100]

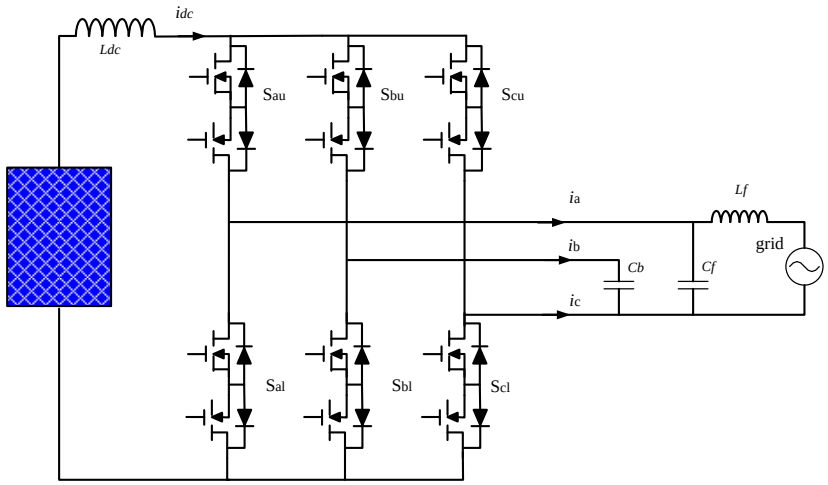


Figure 4.33: Topology proposed by Bush, *et. al* [101]

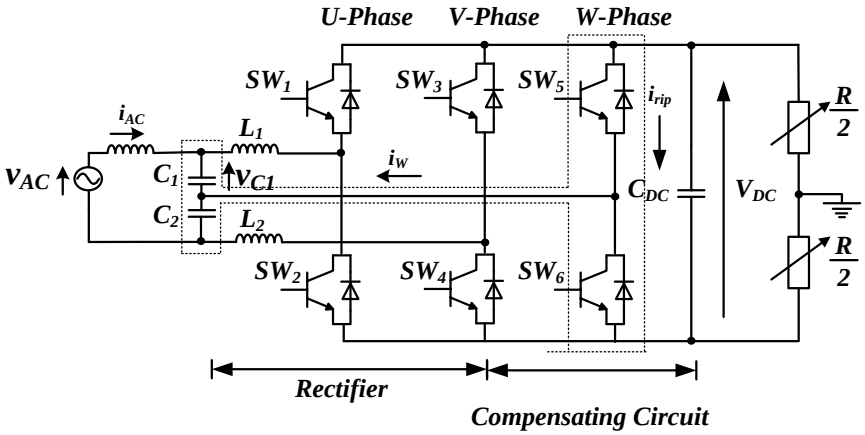


Figure 4.34: Topology proposed by Shimizu, *et al* [102]

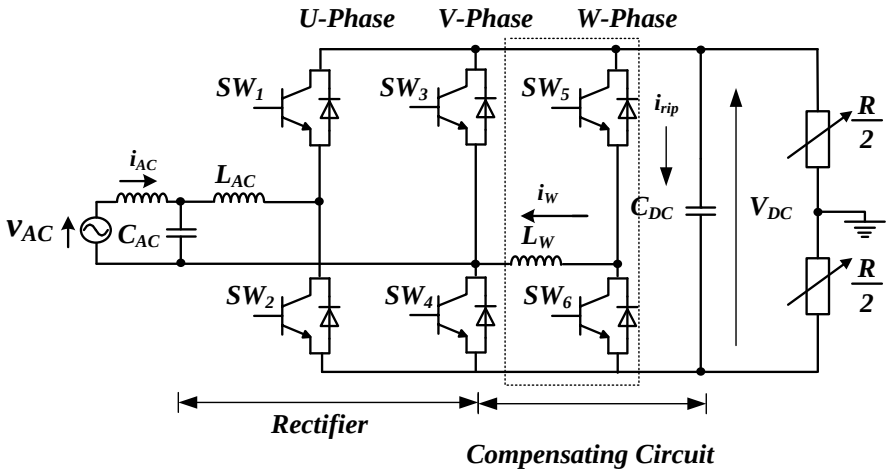


Figure 4.35: Topology proposed by Tsuno, *et al* [103]

The aforementioned topologies, which employ AC side decoupling technique, are a typical unbalanced three phase system with three phase voltages and currents described as follows:

$$\begin{cases} v_a = V_a \sin(\omega t) \\ v_b = V_b \sin(\omega t + \varphi_{ub}) \\ v_c = 0 \end{cases} \tag{4.8}$$

$$\begin{cases} i_a = I_a \sin(\omega t + \varphi_{ia}) \\ i_b = I_b \sin(\omega t + \varphi_{ib}) \\ i_c = -i_a - i_b \end{cases} \tag{4.9}$$

where ω is the angular frequency of the grid, V_a, V_b, I_a and I_b are the amplitudes of

voltages and currents in phase *a* and *b* respectively. φ_{vb} is the voltage phase angle of phase *b*, and φ_{ia} and φ_{ib} are the current phase angles of phase *a* and *b*.

The total instantaneous power can be calculated as:

$$\begin{aligned} P_{total} &= u_a i_a + u_b i_b + u_c i_c \\ &= \underbrace{\frac{U_a I_a \cos\varphi_{ia}}{2} + \frac{U_b I_b \cos(\varphi_{ub} - \varphi_{ib})}{2}}_{P_1} - \underbrace{\frac{U_a I_a}{2}\cos(2\omega t + \varphi_{ia}) - \frac{U_b I_b}{2}\cos(2\omega t + \varphi_{ub} + \varphi_{ib})}_{P_2} \end{aligned} \tag{4.10}$$

As indicated in (4.10), first two terms,P_1, are constant, while the last two terms, P_2, are time-varying. To maintain the power, P_{total}, constant, the only solution is to make the sum of the last two terms, P_2, equals zero. Therefore, the following two constraints have to be satisfied:

$$\begin{cases} U_a I_a = U_b I_b \\ \varphi_{ia} = \varphi_{ub} + \varphi_{ib} + \pi \end{cases} \tag{4.11}$$

Since only the capacitor is connected in phase *b*, the angle and amplitude of voltage and current in phase *b* have the following constraints:

$$\begin{cases} \varphi_{ib} = \varphi_{ub} + \dfrac{\pi}{2} \\ I_b = \omega C U_b \end{cases}, \tag{4.12}$$

where C is the power decoupling capacitance connecting to phase b.

Substituting the expression (4.12) into (4.11), we can draw the following constraints for power balance operation:

$$\begin{cases} I_b = \sqrt{\omega C U_a I_a} \\ \varphi_{ib} = \dfrac{1}{2}(\varphi_{ia} - \dfrac{\pi}{2}) \end{cases} \tag{4.13}$$

Based on the constraints in (4.13), the control scheme can be calculated by using the symmetrical component method to decompose both positive and negative components.

4.3 Performance comparison of the decoupling circuits

The power decoupling techniques presented above will impact the overall system's reliability, cost, and efficiency. For the efficiency comparisons, we use η_0 as the conversion efficiency without the power decoupling circuit while η_d is the efficiency of the added power decoupling circuit.

The power process in the grid-connected PV system with power decoupling circuit is shown in Figure 4.36. The main power stage will process the total power from the PV-

Module, while the power processed by the auxiliary decoupling circuit would be at least the shadowed area in Figure 4.3, whose power can be calculated as:

$$P_{decoupling} = 4 f_{grid} \int_0^{\frac{1}{4 f_{grid}}} \left| P_{dc} - P_o \right| = \frac{2}{\pi} P_{dc} \tag{4.14}$$

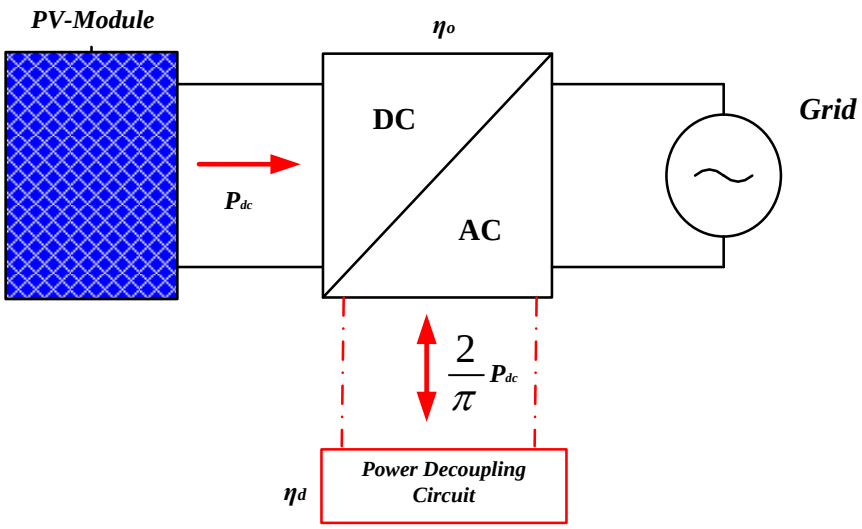


Figure 4.36: The power process in the PV system with power decoupling circuit

Based on the above assumptions on the efficiency, the overall efficiency with the decoupling circuit is expected to be $\eta_o - \frac{2}{\pi}(1-\eta_d)$. Table 4.2 shows the comparison results of the various decoupling techniques with respect to the size of decoupling capacitor, the added cost, the impact on the efficiency, and the decoupling control circuit complexity. For PV side decoupling techniques, from an efficiency aspect, having the decoupling

capacitor directly across the PV output terminals would be the best choice. However, the capacitance is quite large, which will increase the cost, reduce the power density, and shorten the lifetime. As for DC link decoupling techniques, the cost is low due to the fact that no additional circuitry or only control is needed, and the efficiency will be relatively high. However, these techniques can only apply to the multi-stage inverter configurations with DC link implementation. In the AC side decoupling techniques, the capacitance can be very small due to the high voltage swing. However, another phase leg is added, which will increase cost, especially in the aforementioned two current-source based topologies which need bidirectional switches. This would negatively affect the overall efficiency and control complexity.

Table 4.2: Performance comparison of the various power decoupling techniques

Decoupling techniques		Power rating(W)	decoupling capacitor	Additional Cost	Theoretical Efficiency	Experimental/ calculation efficiency	Control Complexity
PV side Decoupling	Fig.4.5	200	13.9mF	Capacitor	η_0	-	No control
	Fig.4.8	70	100uF	Capacitor+2 switches+1 inductor	η_0-2/π(1- η_d)	-	Active filter control
	Fig.4.10	100	40uF	Capacitor+1 switch	η_0-2(1- η_d)	70%	Peak current control
	Fig.4.12	156	314uF	Capacitor+2 switches	η_0-2(1- η_d)	86.7%	Peak current control
	Fig.4.14	100	46uF	Capacitor+1 Switch +3 Diodes	η_0-2/π(1- η_d)	90.6%	Discontinuous current control +Power balance control
	Fig.4.15	100	46uF	Capacitor+1 Switch +2 Diodes	η_0-2/π(1- η_d)	-	Power balance control
	Fig.4.17	500	50uF	3 switches+1capactitor+1 inductor +1 diode	η_0-2/π(1- η_d)	-	Discontinuous current control +Power balance control
	Fig.4.19	100	44uF	1 capacitor +1 switch+ 1 diode	η_0-2/π(1- η_d)	73%	Discontinuous current control +Power balance control
	Fig.4.21	200	40uF	4 switches+ 1 diode+1 capacitor +1 winding	η_0-2/π(1- η_d)	-	Power balance control
	Fig.4.23	100	40uF	2 switches +1 inductor+1diode+1capacitor	η_0-2/π(1- η_d)	-	Power balance control
	Fig.4.25	500	50uF	Capacitor+1 switch+1 inductor	$\eta_0 * \eta_d$	-	control for Boost +Flyback
DC side Decoupling	Fig.4.29	-	-	Capacitor	η_0	-	DC voltage Feed-forward control
	Fig.4.30	200	15uF	Capacitor	η_0	-	Low voltage loop bandwidth
	Fig.4.31	100	500uF	Capacitor	η_0	--	Voltage ripple estimation
AC side Decoupling	Fig.4.32	100	5.53uF	Capacitor+2 switches	η_0-2/π(1- η_d)	-	three-phase current modulation
	Fig.4.33	-	-	Capacitor+2 switches	η_0-2/π(1- η_d)	-	Modified three-phase current modulation
	Fig.4.34	100	165uF	2 switches+ capacitor	η_0-2/π(1- η_d)	-	Three-phase voltage modulation
	Fig.4.35	1000	-	2 switches+ 1 Inductor	η_0-2/π(1- η_d)	~94%	Three-phase voltage modulation

4.4 Discussion

In single-stage microinverter designs, power decoupling circuits can reduce the size of the required energy storage capacitor, thus improving the inverter lifetime, which is a desired feature for PV-MII system. However, the power decoupling circuit will result in additional power losses, due to the power flow through the decoupling circuit, consequently, reducing the overall efficiency. Although the power decoupling circuit may increase the total system's cost due to the additional circuitry required, the extended lifetime eliminates the reoccurring cost of inverter replacement that haunts current PV system return on investment (ROI). To reduce the decoupling circuit power loss, the power processed by the decoupling circuit should be minimal and limited to $2/\pi P_{dc}$.Furthermore, to reduce the cost of decoupling circuit and achieve high conversion efficiency, the three-port converter with features of low component count, high integration and high conversion efficiency is believed to be one of the best choices, with one port implementing MPPT and a second port is dedicated for power decoupling. Recently many three-port converters have been proposed to interface a renewable system. Two examples use a third port to realize the power decoupling are shown in Figure 4.37 and 4.39 [104, 105].

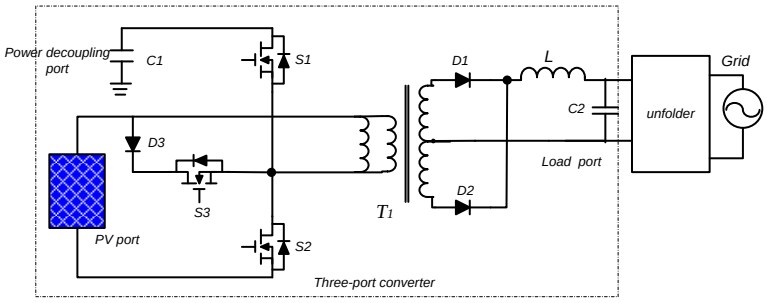


Figure 4.37: An integrated three-port inverter with power decoupling capability [104]

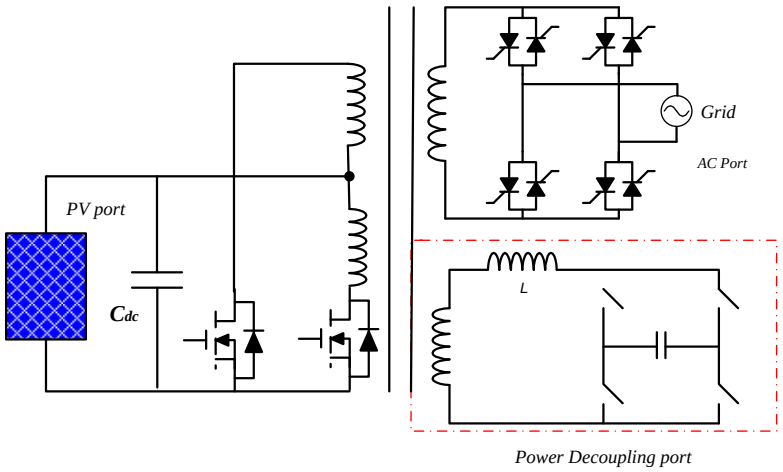


Figure 4.38: AC link implementation of three-port converter proposed in [105]

4.5 Conclusion

The double-line frequency ripple issue in a single-phase power DC/AC or AC/DC converter was presented and explained. An energy storage capacitor is used to decouple the difference between the DC and the AC power is needed, hence the name decoupling capacitor. Recently, many research works have been proposed to improve the

microinverter's reliability by using high-reliability decoupling capacitor technology. This section reviews various power decoupling techniques that have been employed in a single-phase microinverter to reduce the size of decoupling capacitor and improve the converter's lifetime expectancy. Conventionally, for single-stage inverters, the decoupling capacitor is placed across PV module's terminals resulting in a large size capacitor. PV-side power decoupling circuits can be employed to reduce the capacitor size. However, the overall inverter's efficiency is negatively affected. Three-port converters may offer better alternatives for single-stage inverters due to their lower cost and higher efficiency. For multistage microinverter topologies with DC link, the DC-link capacitor offers the best alternative for power decoupling. However, sophisticated control strategies should be employed to allow for higher voltage ripple and to maintain a low THD in the injected current into the grid, which will result in reducing the size of the decoupling capacitor. Finally, AC-side decoupling involves incorporating a third phase to implement the power decoupling, where a very small capacitance is required, but the control complexity is increased dramatically.

5 DC-LINK BASED RIPPLE-PORT [*]

In section four, different decoupling techniques are presented that aim to cancel the double-line frequency ripple on the DC side. However, most of the proposed techniques depend on modifying an existed topology, and hence, each technique is tailored for a specific topology, which makes it very difficult, if not impossible, to employ it for another topology or power flow. This section presents a general technique that can be used to suppress the double-line frequency ripple. Without loss of generality, the proposed converter topology is based on the commonly used two-stage converter with a third port is added for ripple cancellation purposes. One appreciates, however, that any topology can be used as long as a suitable DC-link exists. Figure 5.1 shows the general block diagram of the proposed ripple-port concept that can be applied for both DC/AC and AC/DC single-phase power conversion. For the purpose of this dissertation, the storage element of the ripple-port is sized for the double-line frequency component. However, in general, the ripple-port concept can be extended to other applications.

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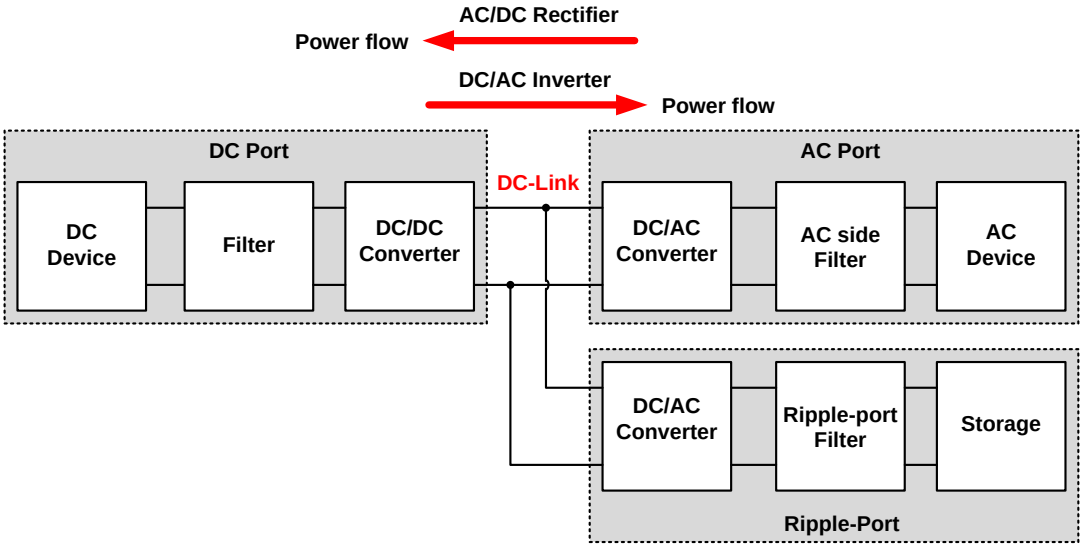


Figure 5.1: A general system block diagram of the ripple-port

In the DC/AC inverter applications, a DC power source, for example a PV panel, is used to supply power to a passive AC load or the AC grid. On the other hand, for the AC/DC rectifier applications, an AC power source is used to supply a DC load, for example a battery or an LED lighting system. Later in this section, analytical, simulation, and experimental results are presented to verify the concept of the proposed ripple-port concept for both PV energy and LED lighting applications.

Although the ripple-port concept is mainly applied for cancelling the double-line frequency ripple that is inherent in the single-phase power converter, in general, the AC port could be a three-phase. In a balanced three-phase system we would not expect a double-line or a triple-line frequency ripple. However, if the system is not completely balanced, these components could exist and the ripple-port could be used to filter them out.

This section is organized as follows, different implementation options of the ripple-port for DC-link PV module-integrated-inverter (PV-MII) are presented in section 5.1. Also, in section 5.1, the power process in the proposed ripple-port is explained; simulation and experimental results are presented as well. In section 5.2, the ripple-port concept is applied for a single-phase AC/DC rectifier application. Similarly, simulation and experimental results are presented as well, Followed by a conclusion in section 5.3.

5.1 DC-Link-Based PV Module-Integrated-Inverter (MII)

The proposed topology, suitable for use as a module-integrated inverter (MII), is based on the commonly used two-stage inverter with a third port is added, on the DC-link, for ripple cancellation purposes. Later in this section, it will be shown that the double-line frequency ripple can be filtered using a very small decoupling capacitance (C_D), and, as a result, high reliability film capacitor can be used instead of the bulky, low-reliability electrolytic ones [25, 28, 106]. Figure 5.2 shows the system block diagram of the ripple-port module-integrated inverter (RP-MII) in which double-frequency ripple cancellation is accomplished by adding a "ripple-port" on the DC-link of the multi-stage inverter. Comparing Figure 5.2 to the block diagram in Figure 5.1, the AC port consists of the DC/AC converter, L_fC_f low pass filter, and the grid as load. The DC port consists of the PV module as a power source and the DC/DC converter and filter. And finally, the ripple-port consists of a DC/AC converter, L_D low-pass filter, and the decoupling capacitor as a load. It will be presented in section 5.2 that the same ripple-port, shown in Figure 5.2, can be used for the AC/DC rectifier application.

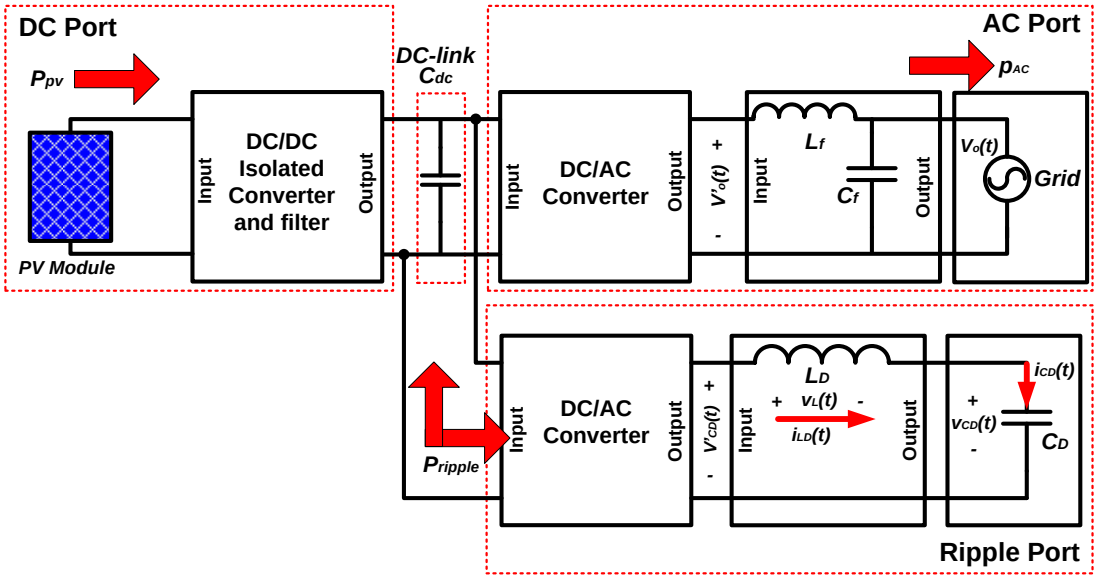


Figure 5.2: System block diagram of the ripple-port module-integrated inverter (RP-MII)

Another advantage is that this ripple port concept can be used with any isolated DC/DC converter topology capable of boosting the input voltage and providing galvanic isolation for grid-connected applications. In case that galvanic isolation is not required, boost converter can be used. However, since it has to operate at high duty ration in order to provide a DC voltage that is compatible with the grid voltage, its efficiency will be significantly deteriorated. Hence, a high-frequency transformer, with a suitable turn ratio, based topology is used instead.

Consider the ripple-port that consists of an H-bridge and decoupling capacitor (C_D), as shown in Figure 5.3. Kirchoff's Voltage Law (KVL) necessitated to have an inductor (L_D) added, as a filter block, between the two different voltage source. This is to prevent the sudden change in the decoupling capacitor's voltage due to the H-Bridge switching effect.

Decoupling the energy storage from the DC-link allows creation of any arbitrary voltages across the storage device. As a result, when the circuit takes advantage of a zero-to-peak sinusoidal energy cycle, only a very small capacitance is needed to store and deliver the double-line frequency pulsing power in the ac system.

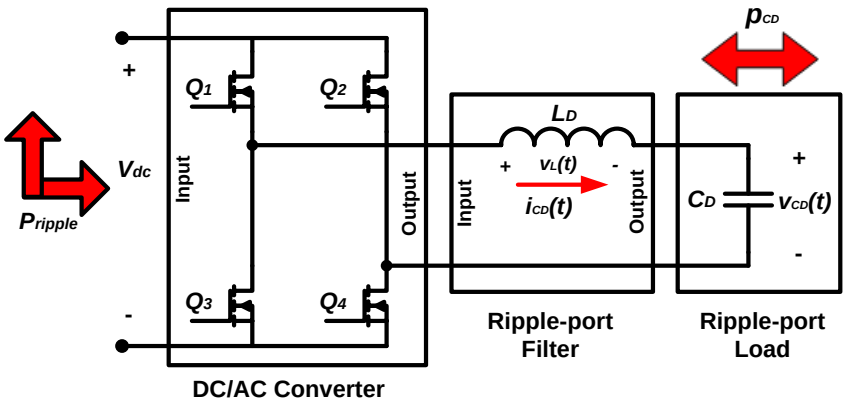


Figure 5.3: Ripple-port schematic

5.1.1 RP-MII implementation

The input DC/DC stage can be implemented using any DC/DC converter topology that is capable of boosting the voltage from the PV module and providing the needed galvanic isolation for safety purposes. In addition to the required galvanic isolation, the transformer's boosting capability improves the system's efficiency. To demonstrate the concept, the popular flyback converter is used in this section [8, 37, 39, 40, 44]. The proposed MII can be implemented in two ways: integrated and separated ripple-port

winding. Both implementations are explored in this section along with simulation results. However, the reliability analysis, which will be presented later in this section, shows that the separated ripple-port winding does not add a significant improvement to the system's reliability. Although the separated ripple-port winding can be implemented in a way that reduces the required decoupling capacitance, its impact on the reliability, compared to the integrated option, is very small. The detailed analysis is presented later in this section. Hence, only the integrated RP-MII is experimentally tested.

5.1.1.1 Integrated ripple-port (Single flyback output)

Figure 5.4 shows the implementation of the proposed RP-MII with single output flyback converter. The ripple-port is integrated with the output port on the secondary winding of the flyback coupled inductor. Hence, the peak voltage of the decoupling capacitor (V_{CD}) is constrained by the dc link. For a 235W inverter with a $200V_{dc}$ DC-link and depth of modulation (DoM) of 0.95 for the ripple-port DC/AC inverter, a 36µF is needed according to the equation (5.8), which is derived in section 5.1.2. However, due to imperfect coupling between the transformer's winding and power losses through the system, a slightly larger decoupling capacitance is needed in practice, since the calculation is based on the ideal lossless system.

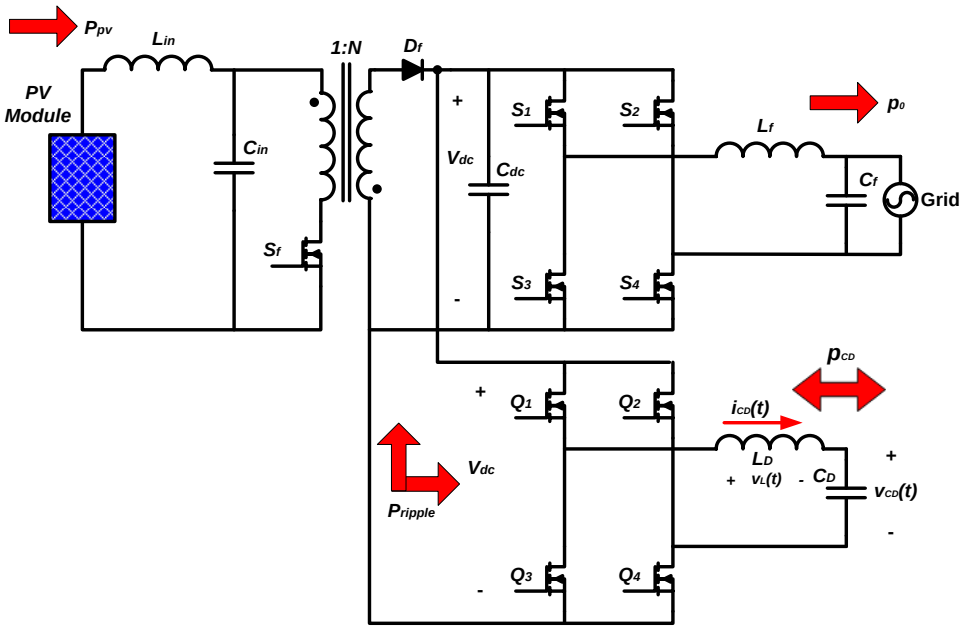


Figure 5.4: Ripple-port module-integrated inverter, single winding

5.1.1.2 Separated ripple-port (multiple flyback outputs)

Figure 5.5 illustrates the integration of the ripple-port into the flyback converter through a separated transformer's winding. In this case, the decoupling capacitor peak voltage (V_{CD}) is not constrained by the DC-link. Consequently, the capacitance can be minimized by using a higher voltage. For the same 235W RP-MII, but with a turns ration that provides a $550V_{dc}$ on the input of the ripple-port, only 4.6µF is needed (5µF is used in the simulation) according to the equation (5.8), which is derived in section 5.1.2. This extra degree of design freedom carries with it the tradeoffs of requiring extra components and the efficiency implications of power losses and transformer leakage energy. This idea of introducing a separate transformer's winding suggests a concept of an AC-link ripple-port,

which will be fully explored in section seven. Table 5. 1 compares the two implementation approaches.

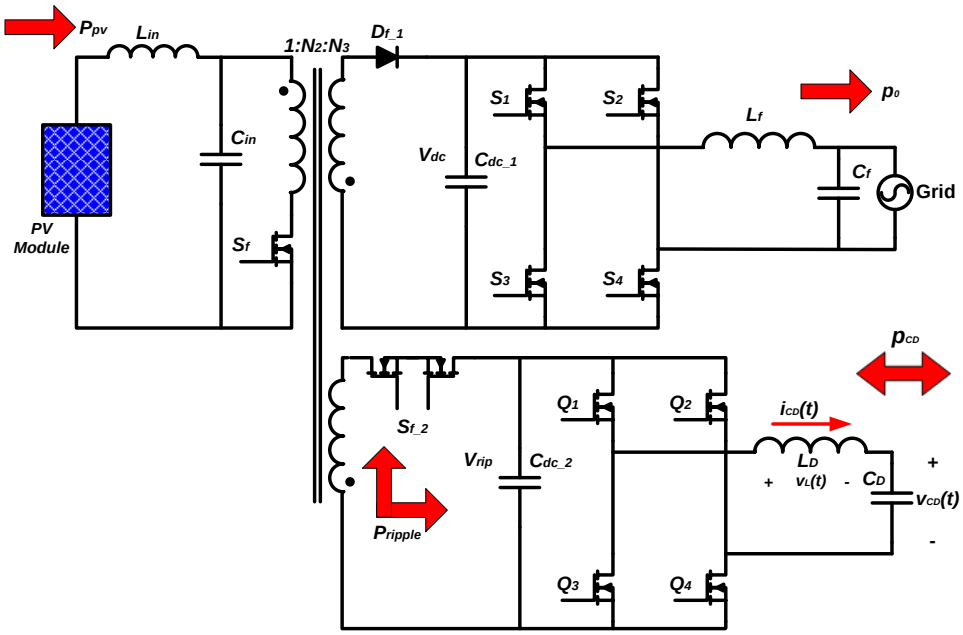


Figure 5.5: Ripple-port module-integrated inverter, multiple windings

Table 5.1: A comparison of ripple-port implementations

Implementation approach	Decoupling capacitance (C_D)	DC-link voltage	Complexity
Integrated winding	36µF	200 V	No additional components
Separated winding	4.6 µF	550 V	Extra transformer winding, DC-link capacitor, and bidirectional switch on the DC input side of the ripple-port

5.1.2 Ripple-port power processing

Figure 5.2 illustrates the voltage polarity and current direction in the ripple-port load/source (L_D and C_D). A small inductor is used to satisfy KVL and prevent sudden changes in the capacitor's voltage because of the switching effect. Assuming unity power factor, the output power given in (4.5) becomes as given in (5.1), which has a constant average value and a double-line frequency component.

$$p_0(t) = P_{PV} + P_{PV}\cos(2\omega_o t) \tag{5.1}$$

where $P_{PV} = \frac{1}{2} V_g I_g$

Since, the ripple-port is processing the power on the DC-link, this implies that the phase shit effect of the AC port low pass filter should be taken into consideration in order to achieve an accurate ripple cancellation on the DC side. This can be accomplished by considering the power on the input of the AC output port filter. Considering a *LC* low pass filter in Figure 5.6 with a transfer function of *G*, the voltage ($v_0'(t)$) on the input side of the AC port filter is given in (5.2), where only the fundamental component is considered.

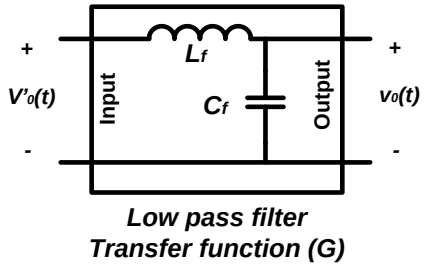


Figure 5.6: Low pass filter block diagrm

$$v_0^{'}(t) = \frac{v_0(t)}{G}, \tag{5.2}$$

where

$v_0^{'}(t) = V_0^{'} \sin\left(\omega_o t + \theta_{filter}\right),$

$\theta_{filter} = \frac{\angle v_0(t)}{\angle G}$ is the phase shift introduced by the filter,

G is the input-to-output voltage transfer function.

For the specific filter configuration shown in Figure 5.6, $v_0^{'}(t)$ is given in (5.3).

$$v_0^{'}(t) = \frac{Z_{C_f} + Z_{L_f}}{Z_{C_f}} v_0(t), \tag{5.3}$$

Where Z_{Cf} and Z_{Lf} are the capacitor and inductor impedances, respectively.

An ideal output *LC* filter will not alter the phase of the output voltage. However, in practice, both the inductor and the capacitor have series resistance, and thus, the amplitude and the phase of the output voltage will be affected by the L_fC_f filter. The impact of the *LC* filter on the amplitude is insignificant, and can be neglected. Consequently, the power that is processed by the AC port H-bridge should take the phase shift introduced by the filter as given in (5.4)

$$p_0(t) = P_{PV} + P_{PV}\cos\left(2\left(\omega_0 t + \theta_{filter}\right)\right) \tag{5.4}$$

On the other hand, the input power, extracted from the PV module, is controlled at a constant value, P_{PV}, based upon the available maximum power point. Then, the ripple-port will be processing the difference between the input and the output power as given in (5.5)

$$p_{rip}(t) = P_{PV} - p_0(t) \tag{5.5}$$

The power processed by the ripple-port is the total power processed by the decoupling capacitor, C_D, and the inductor, L_D, which is calculated as follows:

$$p_{rip}(t) = p_{L_D}(t) + p_{C_D}(t) = v_{L_D}(t) i_{L_D}(t) + v_{C_D}(t) i_{C_D}(t) \tag{5.6}$$

However, the same current flows in both L_D and C_D, which it is given in (5.7), assuming $v_{CD}(t)=sin(\omega_0 t+\phi)$. Then, $p_{rip}(t)$ as function of L_D, C_D, and the peak capacitor voltage is given in (5.8).

$$i_{C_D}(t) = C_D \frac{dv_{C_D}(t)}{dt} = V_{C_D} C_D \omega_o \cos(\omega_o t + \phi) \tag{5.7}$$

$$\begin{aligned} p_{rip}(t) &= i_{C_D}(t) * v_{C_D}(t) = \left(V_{C_D} C_D \omega_o \cos(\omega_o t + \phi)\right)\left(V_{C_D} \sin(\omega_o t + \phi)\right) \\ p_{rip}(t) &= \frac{V_{C_D}^2 C_D \omega_o \left(1 - \omega_o^2 L_D C_D\right)}{2} \sin(2(\omega_o t + \phi)) \end{aligned} \tag{5.8}$$

Substituting (5.4) and (5.8) in (5.5), the required decoupling capacitance, C_D, and the phase angle (ϕ) of the voltage across the decoupling capacitor is calculated as shown in (5.9) and (5.10) [36]

$$C_D = \frac{2P_{PV}}{V_{C_D}^2 \omega_o \left(1 - \omega_o^2 L_D C_D\right)}, \tag{5.9}$$

and

$$\cos\left(2\left(\omega_0 t + \theta_{filter}\right)\right) = \sin\left(2\left(\omega_0 t + \phi\right)\right)$$
$$\phi = \pm\frac{\pi}{4} + \theta_{filter} \tag{5.10}$$

The AC port's LC filter and the ripple-port's L filter introduce a small phase shift, as shown in Figure 5.6. This phase shit needs to be taken in consideration in the control design.

From (5.9), it is clear that a tradeoff exists between the value of the decoupling capacitance (C_D) and the peak capacitor voltage (V_{CD}). The latter will determine the stresses on the power switches, which, in turn, affects the efficiency and the cost of the inverter. Controlling voltage across the decoupling capacitor ($v_{CD}(t)$) according to (5.9) and (5.10) will result in a balance three-port system. Figure 5.6 shows the output voltage and the voltage across the decoupling capacitor with a clear 45 degree phase shift. Figure 5.7 shows power waveforms of the RP-MII, where the double-line frequency ripple, on the input side, is eliminated.

The aforementioned analysis shows that the key of the ripple cancellation process, using

the proposed ripple-port technique, is to control the voltage across the decoupling capacitor ($v_{CD}(t)$) considering both (5.9) and (5.10). By doing so, the decoupling capacitor (C_D), connected through the ripple-port, will store the excess power whenever the input constant power (P_{PV}) is higher than the instantaneous output power ($p_0(t)$), and deliver it back to the output when the input power is lower than the instantaneous output power. The controller scheme, based on SPWM, is presented in the next section 5.1.3.

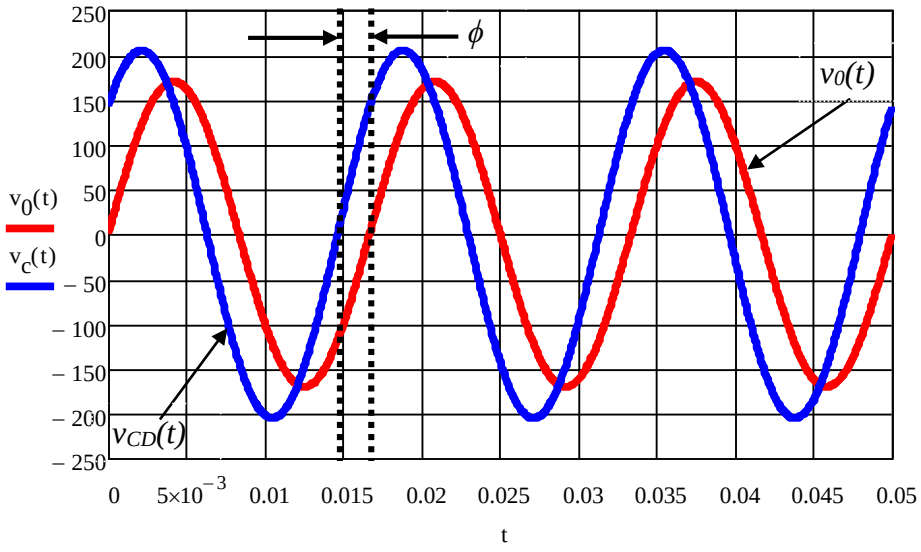


Figure 5.7: Theoretical voltage waveform of a single-phase grid-connected PV System

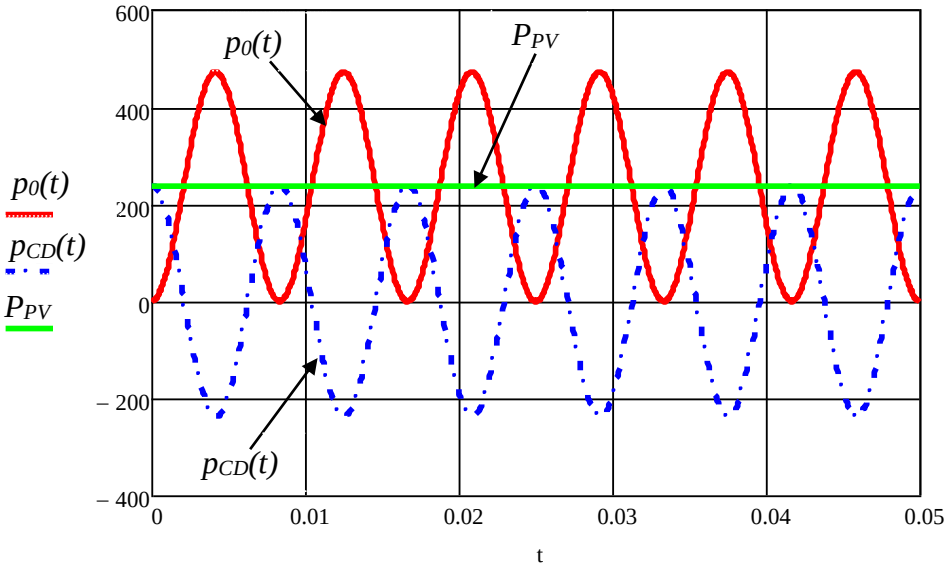


Figure 5.8: Theoretical power waveform of a single-phase grid-connected PV System

From (5.9), it is clear the relationship between the power level, decoupling capacitor's voltage (V_{CD}), and the decoupling capacitance. Since the latter is a design parameter that cannot be changed during the operation. Hence, the only parameter that can and needs to be modified in order to cancel the double-line frequency is V_{CD}. This can be accomplished by modifying the DoM_{RP} of the ripple-port DC/AC converter. Assuming C_D and L_D are very small, V_{CD} is calculated as given in (5.11) for different operating power, and then, the DoM_{RP} is calculated by (5.12). This value will be fed to the SPWM modulator.

$$V_{CD} = \sqrt{\frac{2P_{PV}}{\omega_o C_D}} \tag{5.11}$$

$$DoM_{RP} = \frac{V_{CD}}{V_{dc}} \tag{5.12}$$

For 235W and 200Vdc PV-MII system, figure 5.9 shows how the DoM_{RP} changes as the operating power changes. Also, it shows the relationship between the DoM_{RP} and the operating power at different decoupling capacitor (C_D) design values. Figure 5.9 shows the C_D*'s* values that guarantee the double-line frequency ripple cancellation without an overmodulation operation mode. It shows that as the C_D increases the DoM_{RP} range decreases for the expected operating power levels. This indicates a tradeoff problem between using smaller C_D, which results in a lower cost, and the narrow DoM_{RP}, which results in optimum conversion efficiency. However, there are many factors that play a role in the design process. For example, using smaller CD means high peak voltage across its terminals (according to (5.9)). The higher DC-link voltage can be achieved using higher number of transformer's turns. Having a high DC-link voltage has two negative impacts, higher voltage stress on semiconductor devices and higher conduction power loss in the transformer's turns. In [107-109], a multi-objective optimization methodology is presented and applied for different power electronic applications. It takes into account the usage model of the application in order to find the optimum design. A new high-frequency magnetic modeling technique, for power electronics converters, is presented in [110-112], where the finite element analysis is used to determine the parasitic components of high-frequency magnetics' windings and its impact on the overall system's performance.

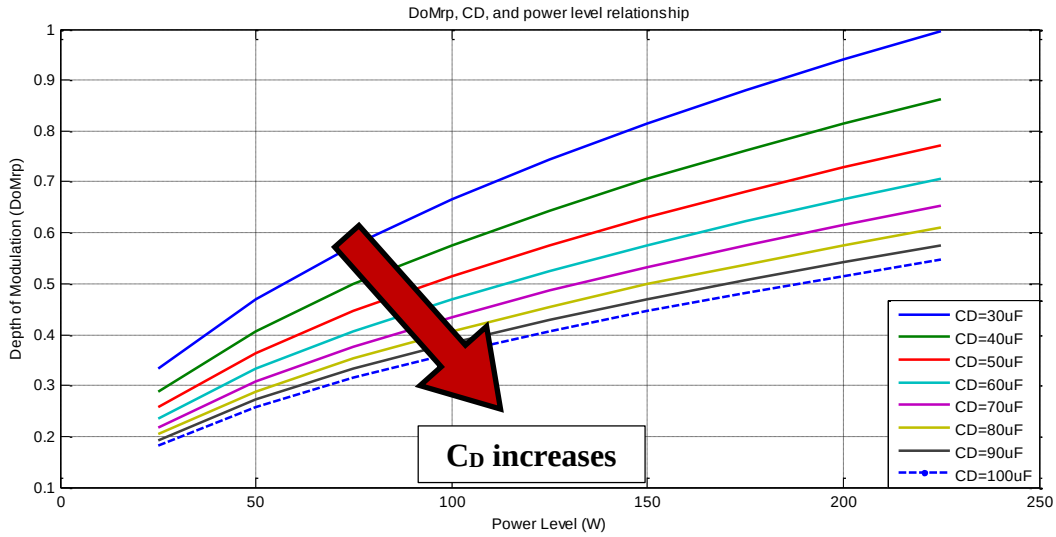


Figure 5.9: The relationship between the DoM_{RP} and the operating power at different decoupling capacitor (C_D) design values

As shown previously, the proposed ripple-port consists of an H-Bridge (four switches) followed by an *LC* filter. Selecting the switches depends on the voltage ratings, which is determined by the peak voltage across the decoupling capacitor (V_{CD}). The latter, also, determines the required decoupling capacitance giving the average input power (P_{PV}). However, in the integrated implementation option, the DC-link voltage is determined by the output (grid) voltage. Hence, V_{CD} is determined now, and then the decoupling capacitor is calculated using (5.9). Finally, the inductor is used to prevent any sudden change in the voltage across the decoupling capacitor as a result of the switching action for the H-Bridge. The inductance value (L_D) can be precisely calculated using (5.13); however, both the voltage across C_D and the time change of the current are changing as the SPWM duty ratio changes. However, for the purpose that this inductor is being used, a precise value is not really critical. And this difficulty in calculating L_D can be avoided. A very small

inductance, in the range of tens of micro Henrys will accomplish the task. In the simulation as well as the experiment, in this paper, a 200µH was used.

$$v_{LD}(t) = L_D \frac{di(t)}{dt} = V_{DC} - v_{CD}(t)$$
$$L_D = \frac{V_{DC} - v_{CD}(t)}{\Delta I} \tag{5.13}$$

5.1.3 Controlling the proposed RP-MII

One of the proposed RP-MII advantages is a simple control. The most commonly used SPWM control scheme is used to control both H-Bridge (output and Ripple-port) inverters. Figure 5.8 shows the block diagram of the control system. The upper SPWM process generates the gate signals that control the output H-Bridge inverter. While the gate signals of the ripple-port are generated by the lower one. The modulating signal of the ripple-port inverter is a shifted version of the one used for the output inverter, where the phase shift (ϕ) is calculated from (5.10), which takes into account any phase shift occurred due to the AC port's LC filter and the ripple-port's L filter. The *DoM* of the output inverter is determined by the output (grid) voltage, however, for the ripple-port, the DoM_{RP} determines the peak voltage across the decoupling capacitor (V_{CD}). On the other hand, V_{CD} determines the required decoupling capacitor (C_D) for a specific power rating, as shown in (5.9). The latter requires a compromise decision between the used decoupling capacitance on one hand, and the voltage stressed imposed on the power switches on the

other hand, which will affect the overall efficiency of the inverter.

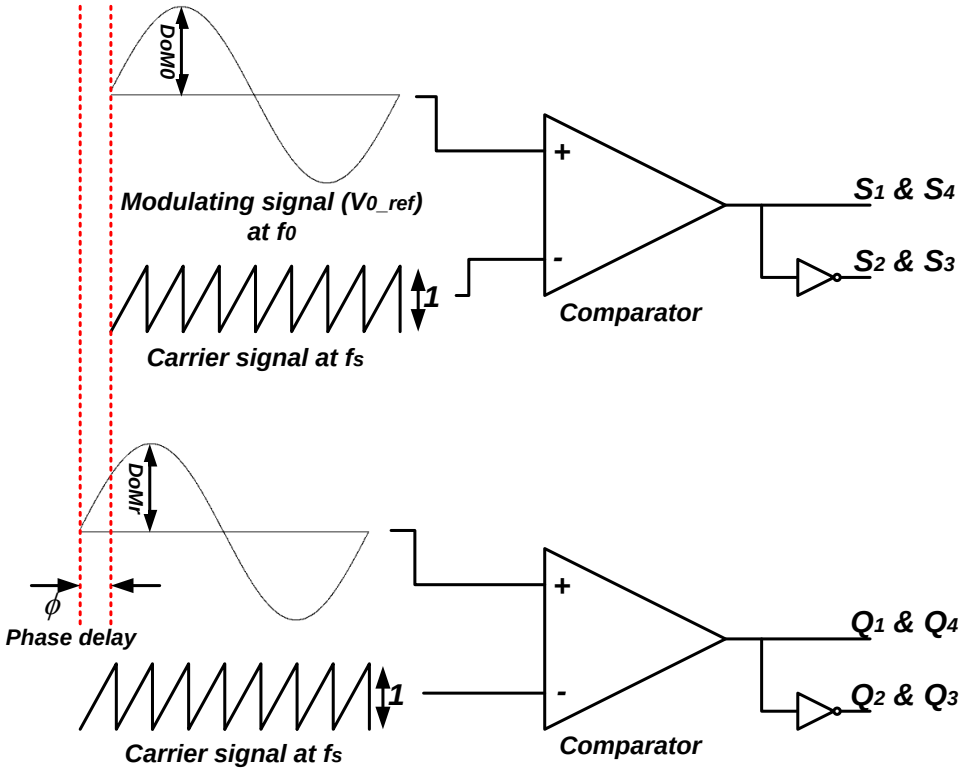


Figure 5.10: Block diagram of a candidate SPWM control scheme used to control both the output and the ripple-port inverters. In practice, a deadtime would need to be added to ensure no shoot-through condition

5.1.4 Reliability of the proposed RP-MII flyback topologies

The proposed topology aims to improve the reliability of the MII by using film capacitors instead of electrolytic ones. Hence, the reliability improvement for both topologies is examined. However, from [11], it was found that the decoupling capacitor is

the limiting component whether electrolytic or film is used. The failure rate of the film capacitor is found using (5.14) [31]:

$$\lambda_P = \lambda_b \pi_{CV} \pi_Q \pi_E \tag{5.14}$$

λ_b is given in (5.15), which is function of the operating temperature (*T (C)*) and voltage stress (*S*). These two factors are operating factors.

$$\lambda_b = 0.00099\left[\left(\frac{S}{0.4}\right)^5 + 1\right]\exp\left(2.5\left(\frac{T+273}{398}\right)^{18}\right) \tag{5.15}$$

Thus, λ_b, π_Q, and π_E all operating-related factors, and will be the same for both configurations (integrated and separated options). Hence, they can be factored out, and λ_P is function of just the capacitance factor, π_{CV}, which is for film capacitor is calculated by (5.16)

$$\pi_{CV} = 1.1C^{0.085} \tag{5.16}$$

Then, the failure rate of the decoupling capacitor is given (5.17)

$$\lambda_P = \pi_{CV}\mathrm{K} \tag{5.17}$$

where $\mathrm{K} = \lambda_b \pi_Q \pi_E$

Evaluating the failure rate for both configurations, with 36µF used in the first configuration in Figure 5.4, and two 5µF capacitors in the second configuration in Figure 5.5, the capacitance factors are calculated in (5.18).

$$\begin{aligned} \pi_{CV1} &= 1.1(36)^{0.085} = 1.492 \Rightarrow \lambda_{P1} = 1.492\mathrm{K} \\ \pi_{CV2} &= 1.1(5)^{0.085} = 1.261 \Rightarrow \lambda_{P2} = 2(1.261)\mathrm{K} = 2.522\mathrm{K} \end{aligned} \tag{5.18}$$

Then, the conclusion is that the number of capacitors used has a stronger effect on the failure rate than the value of the capacitance itself. Moreover, the lifetime projection formula in (5.19) [46] does not depend on the capacitance value, consequently, both decoupling will have the same expected lifetime, providing the same operating conditions

$$L = \frac{L_0 \left(2^{\left(T_{ref} - T \right) / 10} \right)}{\left(\frac{V_{op}}{V_r} \right)^{2.6087 \left[\left(V_{op} / V_r \right) + 0.5167 \right]}} \tag{5.19}$$

where L_0 is the basic (test) lifetime, V_{op} is the operating voltage, V_{ref} is the rated voltage, T is the operating temperature, and T_{ref} is the test temperature.

As a result, from reliability point view, using film capacitor, regardless of its value, will improve the overall reliability of the inverter for the specific PV-MII studied in this section.

5.1.5 Simulation results for the DC-link MII

Consider the 235W system, the component values of the RP-MII topology, shown in Figure 5.4, are listed in Table 5.2. PSIM was used to verify the validity of the proposed RP-MII shown in Figure 5.4. Figure 5.11 shows the schematic of the system. The flyback's transformer is assumed to have a perfect coupling. DC-link, output, and decoupling capacitor voltages are shown in Figure 5.12. Figure 5.13 shows that the input, output, and ripple power waveforms match the theoretical waveforms in Figure 5.7. Figure 5.14 reveals that processing 238W results in less than a 1W ripple (0.42% power ripple) on the input. It shows a 51 degree phase shift between $v_0(t)$ and $v_{CD}(t)$. Figure 5.15 shows the FFT waveform of the input power.

Table 5.2: Components list used in the simulation

Component	Value	Component	Value
V_{in}	30 V_{dc}	L_{in}	2mH
V_0	120 V_{rms}	L_m	200µH
f_{s1}	50KHz	L_f	1mH
f_{s2}	100KHz	L_D	100µH
n_2:n_1	9:1	C_{in}	50µF
n_3:n_1	27:1	C_f	10µF
R_0	60Ω	C_D	40µF
DoM_0	0.85	C_{dc}	20µF
DoM_{RP}	0.9	ϕ	51˚

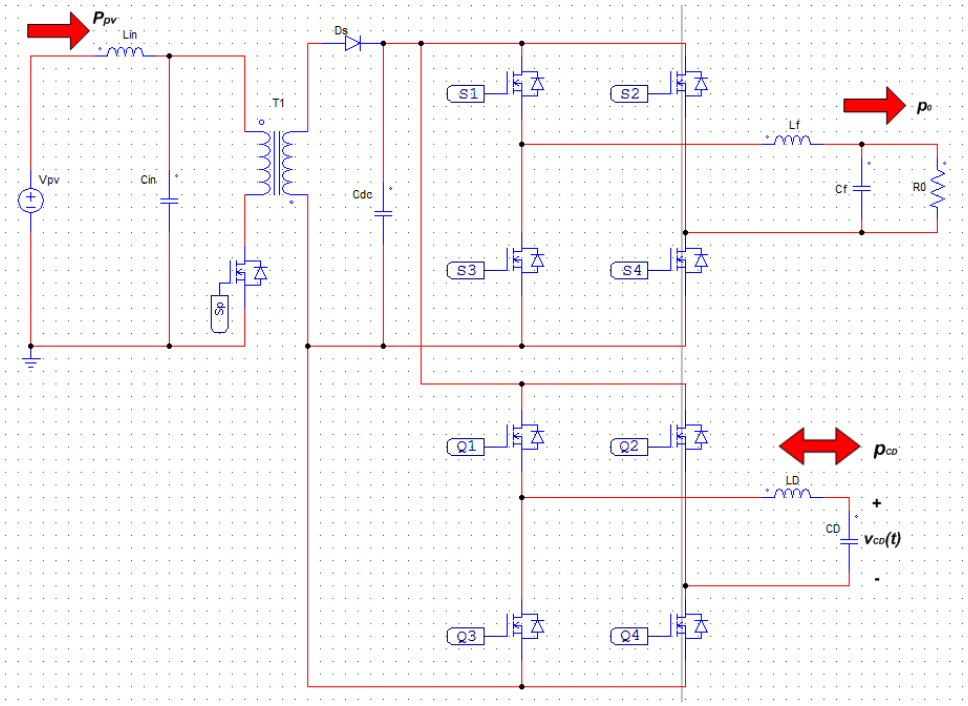


Figure 5.11: PSIM simulation schematic of the ripple-port module-integrated inverter, single winding

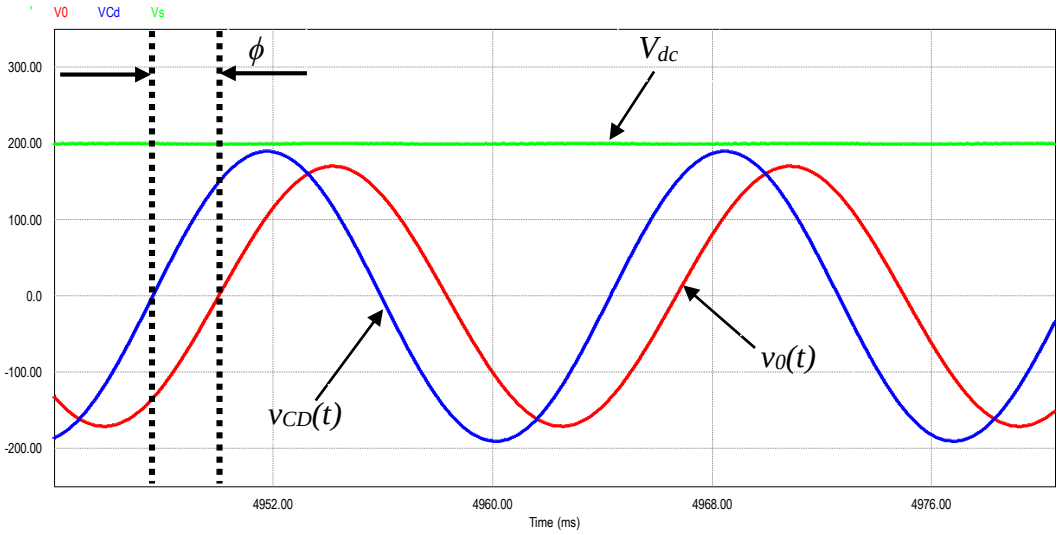


Figure 5.12: DC-Link, output, and decoupling capacitor voltage

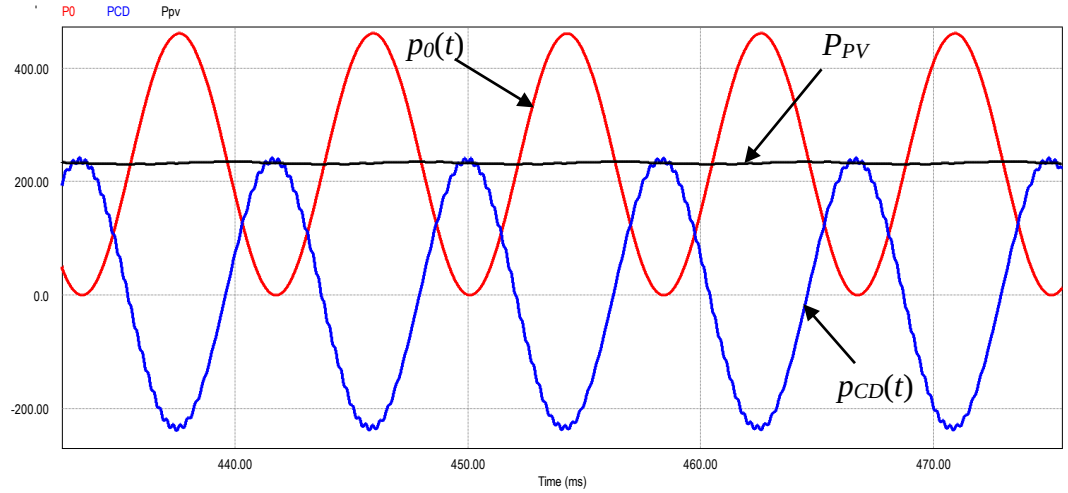


Figure 5.13: Simulation shows operation of cancels double-line frequency

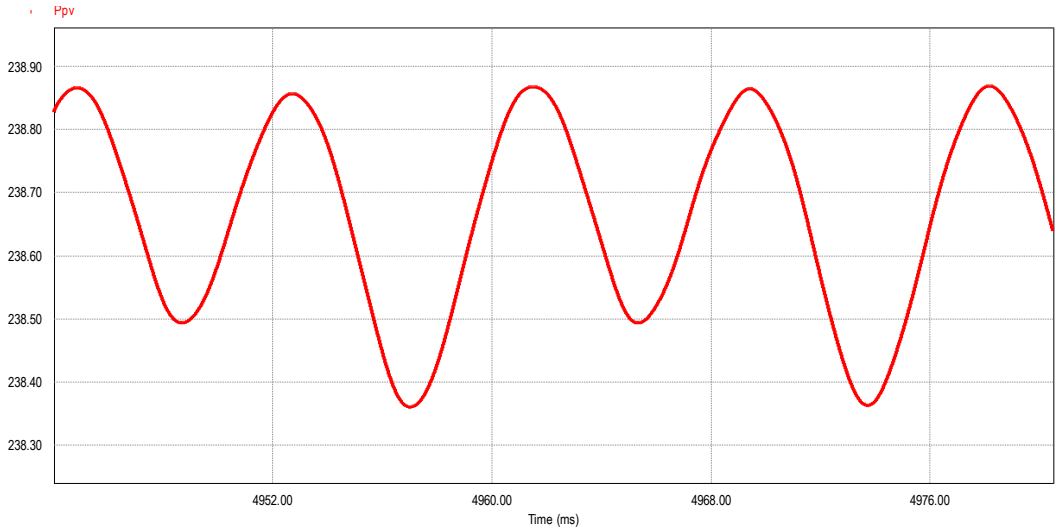


Figure 5.14: Zoom in of the input power waveform, from Figure 5.13, showing attenuation of the double-frequency ripple

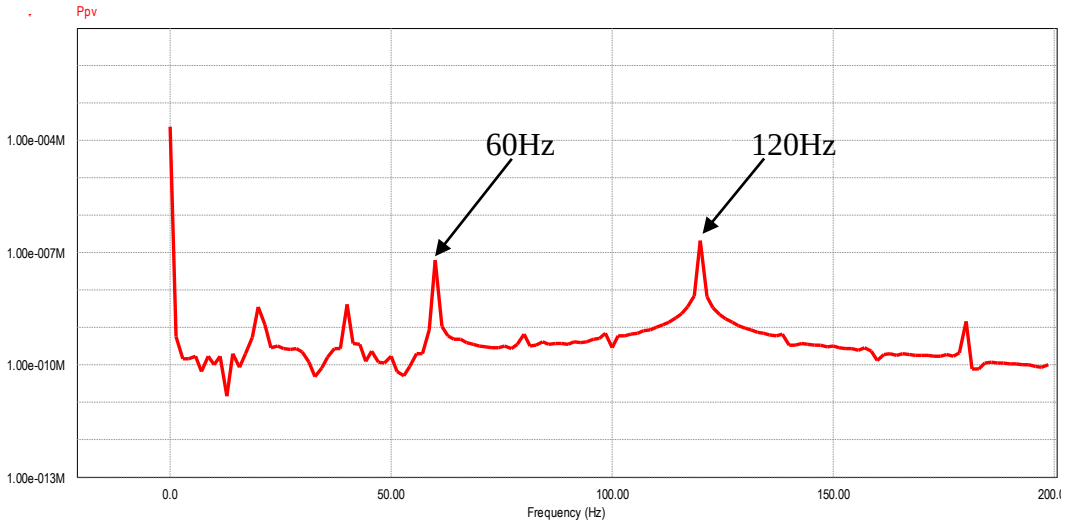


Figure 5.15: FFT of the input power waveform

The system was simulated at different combinations of DoM_{RP} and phase shift (ϕ), and the peak-to-peak input current ripple (Δi_{dc}) was recorded for each case as shown in Table

5.3. These results are shown in Figure 5. 16, which shows a unique operation point (DoM_{RP},ϕ) that results in the minimum double-line frequency ripple.

Table 5.3: Simulation results at different DoM_{RP} and phase shift (ϕ) combinations

ϕ	46 degree		48 degree		50 degree		52 degree		54 degree	
DoM_{RP}	Δi_{dc} (A)	%	Δi_{dc} (A)	%	Δi_{dc} (A)	%	Δi_{dc} (A)	%	Δi_{dc} (A)	%
0.87	1.68	21.54	1.32	16.92	1.1	14.1	1.19	15.26	1.45	18.59
0.90	1.42	18.2	0.9	11.54	0.62	7.95	0.73	9.36	1.17	15
0.93	1.28	16.4	0.77	9.87	0.22	2.82	0.49	6.28	0.96	12.3
0.96	1.4	17.95	0.89	11.4	0.55	7.05	0.69	8.85	1.12	14.36
0.99	1.7	21.8	1.45	18.6	1.19	15.26	1.28	16.4	1.58	20.26

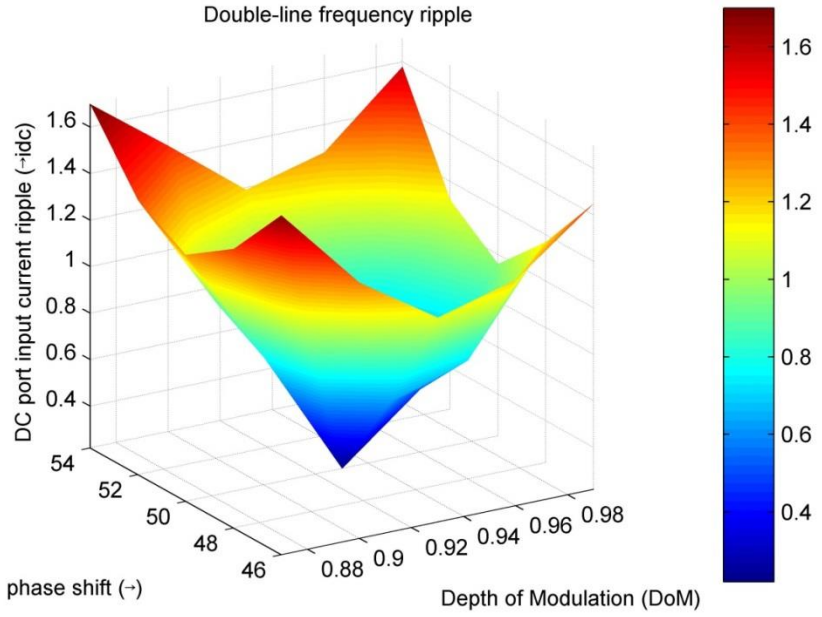


Figure 5.16: Double-line frequency ripple as a function of DoM_{RP} and phase shift (ϕ)

5.1.6 Experimental results

The ripple-port concept was experimentally tested using the new Solar_HV_DC_AC kit from Texas Instruments (*TMDSHV1PHINVKIT*) [113]. It is an IGBTs-based full bridge inverter followed by a low pass filter (LC-filter). Two identical boards were used to implement the AC port and the ripple-port DC/AC converters shown in Figure 5.2. Figure 5.17 show the experiment setup of the RP-MII. Table 5.4 lists the values of the components used in the experiment test. Both boards were controlled by the PWM signals generated using a single TI Delfino microcontroller (*TMS320F28335*). Figure 5.18 shows the output ($v_0(t)$) and decoupling capacitor ($v_{CD}(t)$) voltages and the resulting AC

component of the input current. The depth of modulation (*DoM*) for the output H-Bridge was kept constant at 0.85. The depth of modulation of the ripple-port H-Bridge (DoM_{RP}) and the phase angle (ϕ) were manually tuned to minimize the double-line frequency ripple on the input side. The waveform in Figure 5.18 shows that the input current ripple is suppressed to less than 10% peak-to-peak, and this at $DoM_{RP} = 0.848$ and $\phi = 51.5°$, which results in a peak $v_{CD}(t)$ voltage of 102V. Figure 5.19 shows the input current along with its experimentally measured FFT, which confirms that the 120Hz frequency has been suppressed to the same amplitude as the other low-order harmonics (-46.4dB).

Table 5.4: DC/AC inverter experimental components values

Component	Value	Component	Value
V_{in}	$120V_{dc}$	I_{in}	500mA
L_f	3.5mH	C_f	1µF
R_0	70Ω	L_D	100µH
C_D	40µF	C_{in}	40 µF

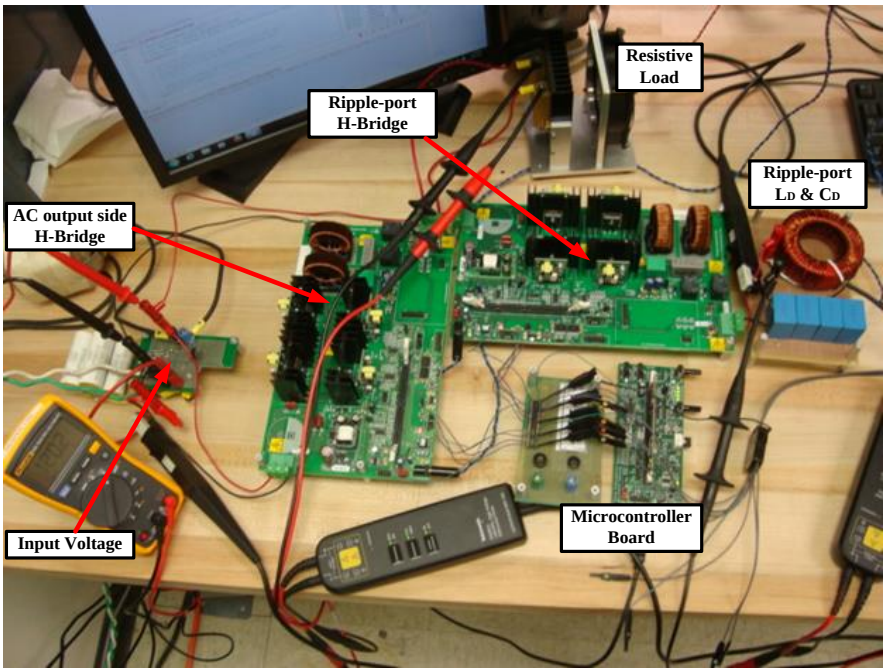


Figure 5.17: Ripple-port experiment set up

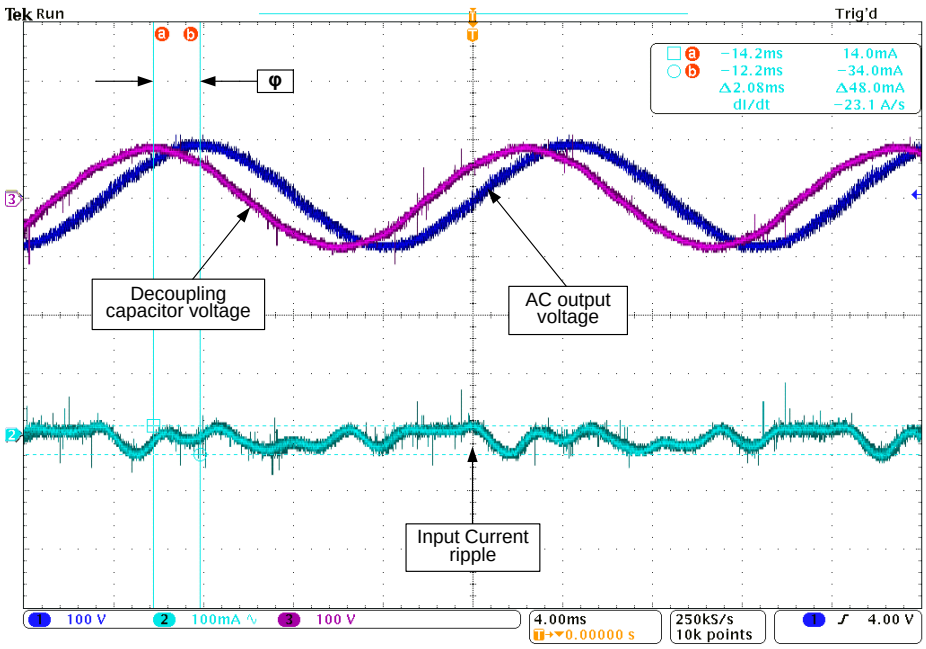


Figure 5.18: Experimental waveform - AC port output voltage, ripple-port decoupling capacitor voltage, and the DC port input current ripple

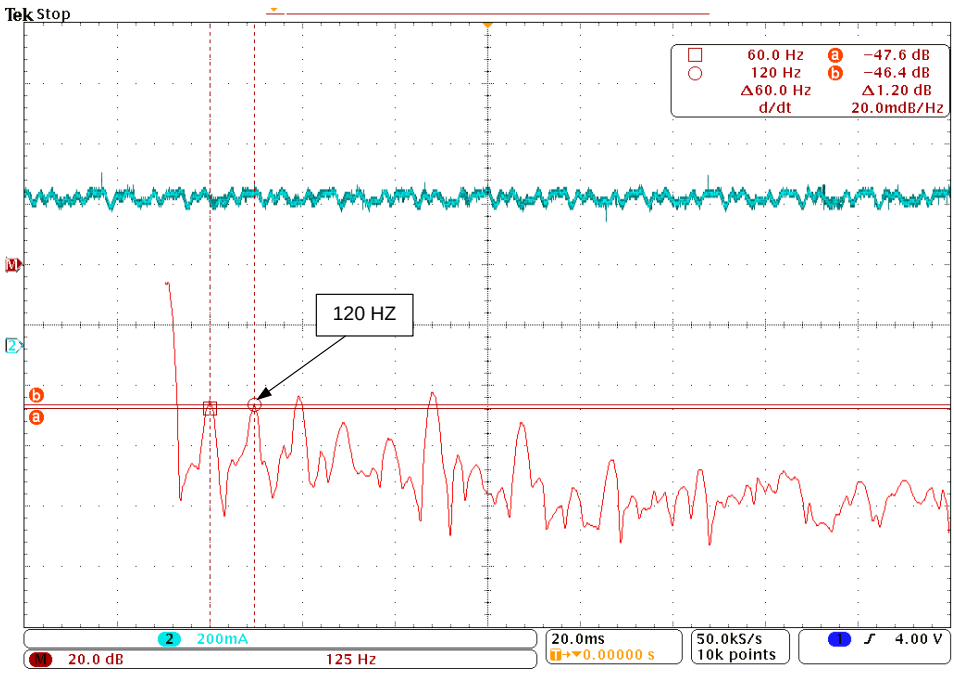


Figure 5.19: Input current (top trace), and the FFT experimental measurement (bottom trace)

To examine the efficacy of the ripple-port, the DoM_{RP} was reduced to 0.5, while the value of ϕ is kept the same as in the previous case. The results, shown in Figure 5.20, clearly show the double-line frequency ripple on the input side. In this case, the input current ripple is 476m peak-to-peak. Figure 5.21 shows the input current and its experimentally measured FFT, which is 30dB higher than what was achieved with manual tuning in Figure 5.19.

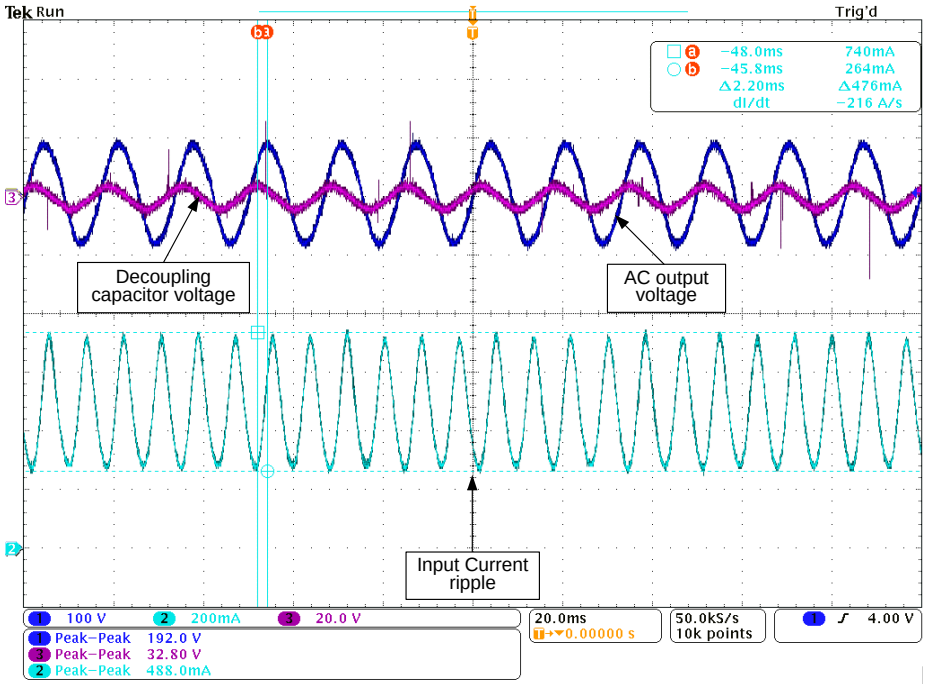


Figure 5.20: Experimental waveform - AC port output voltage, ripple-port decoupling capacitor voltage, and the DC port input current when ripple-port is purposely mis-adjusted

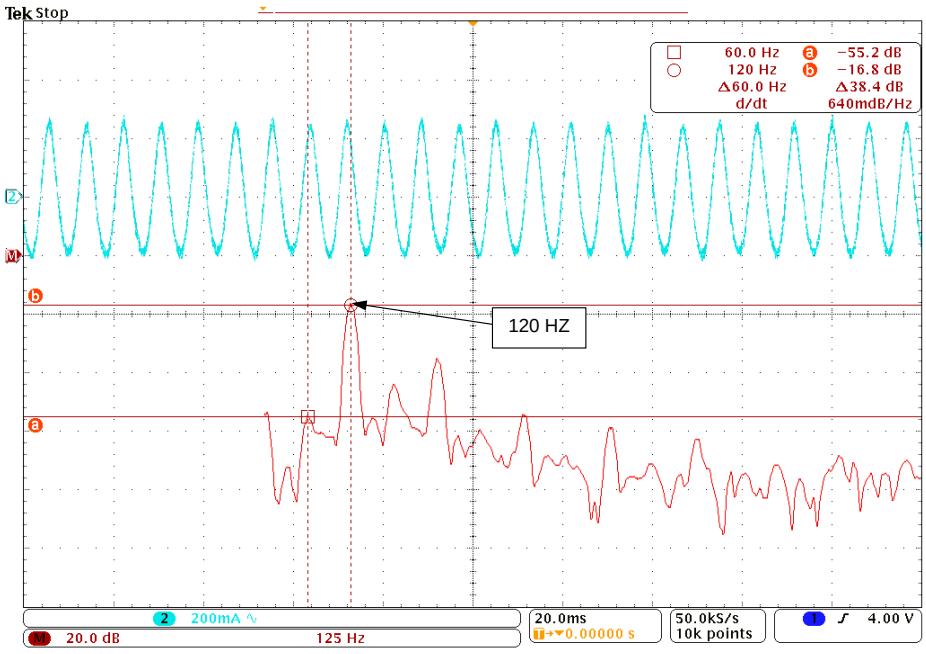


Figure 5.21: DC port input current (top trace), and the FFT for reduced DoM_{RP}

Table 5.5: Comparison of the operation with different DoM_{RP}

	DC port input current ripple (Δi_{dc})	120 Hz of the DC port input current	120 Hz relating to DC
Ripple-port activated	48m A	-46.4 dB	40 dB
Ripple-port deactivated	476m A	-16.8 dB	-38 dB
Ripple-port suppression		29.6 dB	

5.2 Single-phase rectifier with ripple-port

In this section, the ripple-port concept is applied to a single-phase PWM rectifier that eliminates the need for the electrolytic capacitor. Consequently, this improves the reliability of the system that is suitable for long-life applications such as LED lighting. A generic block diagram of an AC/DC rectifier system with the ripple-port is shown in Figure 5.22, which is derived from the block diagram in Figure 5.1. This evidently show the modularity feature of the proposed ripple-port techniques unlike other decoupling techniques presented in section four.

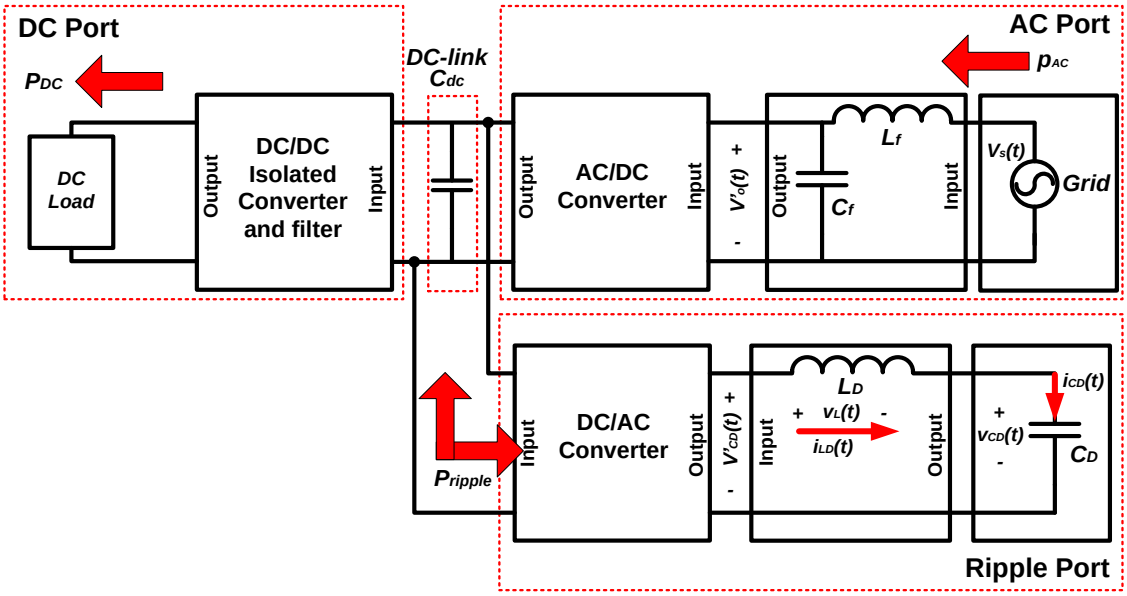


Figure 5.22: A generic block diagram of an AC/DC rectifier system with the ripple-port

The ripple-port is added in parallel with the output (DC-side) of the PWM rectifier to filter the double-line frequency ripple using the minimum capacitance necessary for power buffering. Hence, a very small, highly reliable film capacitor is used that will improve the reliability significantly compared to the bulky electrolytic capacitor option. The latter, in addition to limiting the reliability, increased the power density of the system. The proposed topology doubles the MTBF and increases the lifetime by one order of magnitude, as it will be presented later in this section. Moreover, the design of the ripple-port is independent from the PWM rectifier circuit, so it can be dropped in as an auxiliary circuit to an existing design.

5.2.1 Single-phase PWM rectifier

The single-phase PWM rectifier has numerous advantages over classical passive rectifier topologies including, unity power factor, low THD, bidirectional power flow, and low components count [18, 19], and is well suited for applications of power ranging from data center servers to LED lighting. Like all single-phase power systems, the single-phase PWM rectifier systems suffer from the inherent double-line frequency ripple problem. This ripple must be filtered, and prevented from being reflected to the DC output, where it would deteriorate the voltage ripple performance of the system. Conventionally, a large electrolytic capacitor is used, on the DC-link, for filtering purposes. However, in addition to reducing power density, it is well known that electrolytic capacitors are the most vulnerable components, which limit the lifetime of the power electronics converter [106, 114].

5.2.1.1 **Single-phase PWM rectifier with the ripple-port implementation**

Figure 5.23 shows the proposed single-phase PWM rectifier with the power decoupling ripple-port. The ripple-port is connected to the output DC-link and processes bidirectional power. When the input instantaneous power is greater than the output power, the ripple-port charges the difference in to the decoupling capacitor (C_D). Then, it discharges this energy into the DC load during the opposite situation. This is accomplished by controlling the H-bridge of the ripple-port to have a sinusoidal voltage across the decoupling capacitor (C_D) as explained in section 5.1.2.

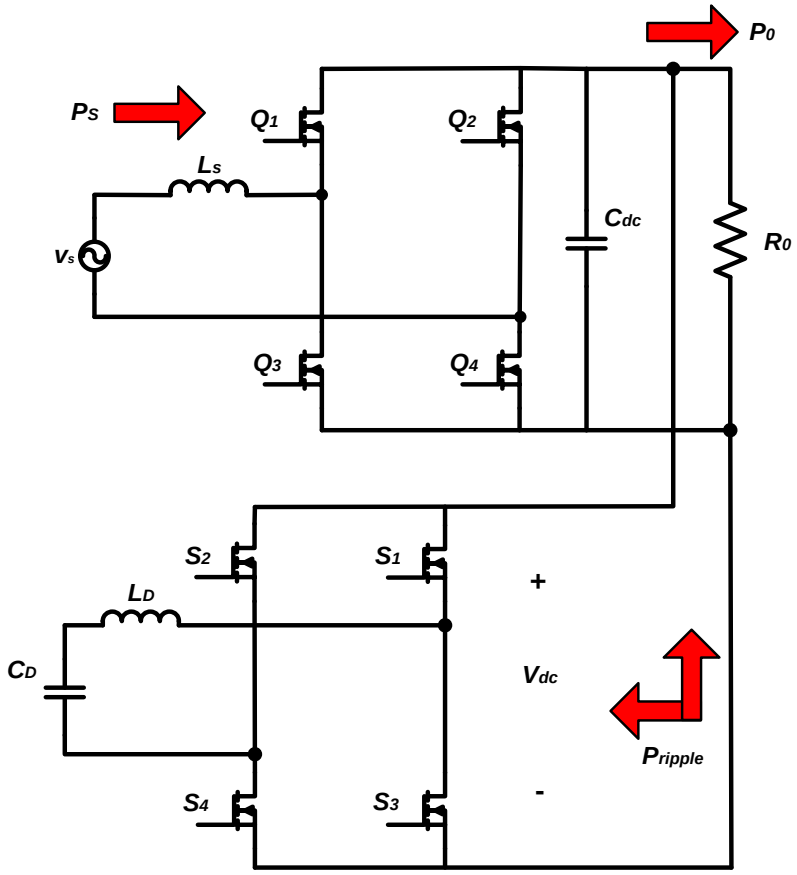


Figure 5.23: Single-phase PWM rectifier with power decoupling ripple-port

5.2.2 Double-line frequency ripple cancellation

The analysis in this subsection is very similar to the analysis in section 5.1.2. However, in order to have a complete and comprehensive explanation for the ripple-port, it will be presented here considering a rectifying mode. The ripple port is connected to the dc output of the PWM rectifier, as shown in Figure 5.23. Without loss of generality, assuming unity power factor the instantaneous AC input power $p_s(t)$ is given in (5.20), and assuming a lossless converter, the average power from the source P_{s_av} and the output dc power P_o are

equal. Then, the double-line frequency, time varying power $p_{df}(t)$ from the ac source must appears on the DC-link (the output side). This power ripple is manifested as voltage ripple on the output capacitor, and must be filtered by the ripple-port to improve the performance of the rectifier. In LED applications, this double-line frequency ripple will negatively affect the efficacy of the LED light, and thus, results in an unstable light output and the potential to shorten the LED operating lifetime. This implies that the ripple-port has to be capable of processing the power given (5.21).

$$p_S(t) = \frac{V_S I_S}{2} - \frac{V_S I_S}{2}\cos\left(2\omega_0 t\right) = P_{S\_av} - p_{df}(t) \tag{5.20}$$

$$p_{ripple}(t) = -p_{df}(t) \tag{5.21}$$

The amplitude (V_{CD}), and the phase angle (ϕ) of the ripple-port capacitor voltage required to cancel the double-line frequency ripple on the dc output port is given by (5.9) and (5.10); where θ is the phase shift in the output voltage caused by the filter components, including L_D and input L-C low pass filter, as well as the phase shift due to non-unity power factor. Complete analysis of the double-frequency ripple cancellation process can be found in [36, 115].

Imposing the conditions in (5.9) and (5.10) for controlling the ripple-port, the input, output, and the ripple-port power are balanced as shown in Figure 5.24 for a 1kW rectifier

system. Figure 5.24 illustrates the ripple-port storing energy by charging the decoupling capacitor (positive p_{ripple}) when the instantaneous input power is greater than the output power, and discharging the decoupling capacitor (negative p_{ripple}) when the input power is less than the output power.

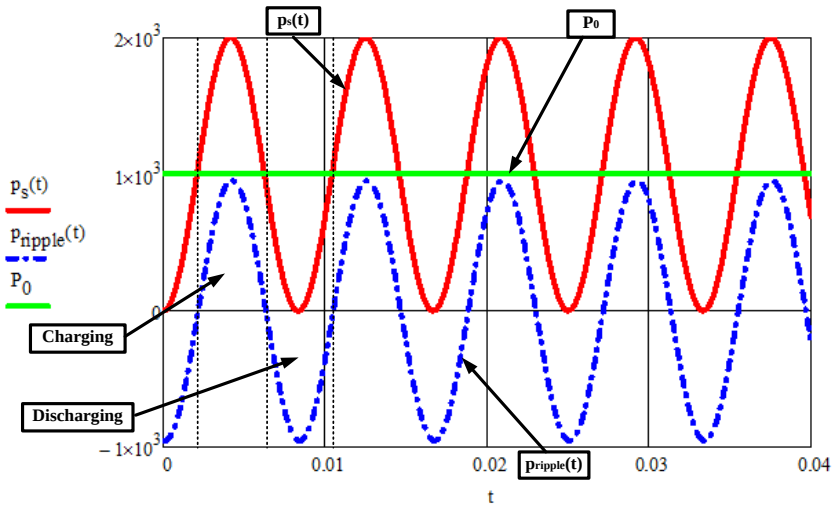


Figure 5.24: Input, output, and ripple power waveforms

5.2.3 Parameters design

The values of the input (L_s) and the decoupling (L_D) inductors are functions of the switching frequency and the power rating. The inductance varies inversely with the average input power ($P_{s\_av} = P_0$) [18] and the design must handle the required peak current and current ripple. For example, at 1kW, the required input inductance is 1.5mH, while

for 100W, 14mH is required. Similarly, for the decoupling circuit, 500µH is needed for 1KW, and 3.4mH for 100W. With the ripple port managing the 120Hz power, the DC-link capacitor (C_{dc}) is only needed to filter high frequency switching ripple. For a 1kW system, 80µF will suffice. On the ripple-port, the double-line frequency ripple is cancelled by the decoupling capacitor (C_D), which is calculated from (5.9). For a 1kW system switching at 100 kHz, only 140µF is needed.

5.2.4 Reliability of the proposed rectifier topology

The proposed single-phase PWM rectifier uses two film capacitors, 80µF across the DC-link and 140µF as a decoupling capacitor. The reliability analysis, for both the conventional electrolytic capacitor option (1,330µF) and the ripple-port capacitor showed that the proposed rectifier topology has improved the MTBF by a factor of more than two, and the lifetime by an order of magnitude, as it is shown in Figure 5.25. MIL-HDBK-217 [31] is used to calculate the MTBF for both options, and the results are shown in Table 5.5. It is worth mentioning that a temperature usage model approach can be used for evaluating the MTBF, such as the one developed for PV inverters [115], instead of a singular operating temperature to present a more realistic assessment of true expected MTBF. This is particularly relevant for outdoor applications of the circuit.

Table 5.6: Comparison of the calculated MTBF for a conventional design with electrolytic capacitor and the ripple-port with film capacitor

	Conventional design	Ripple-port
Capacitance	1,330µF	80µF+140µF
Number of MOSFETs	4	8
MTBF (million hours)	1.1758	2.3480

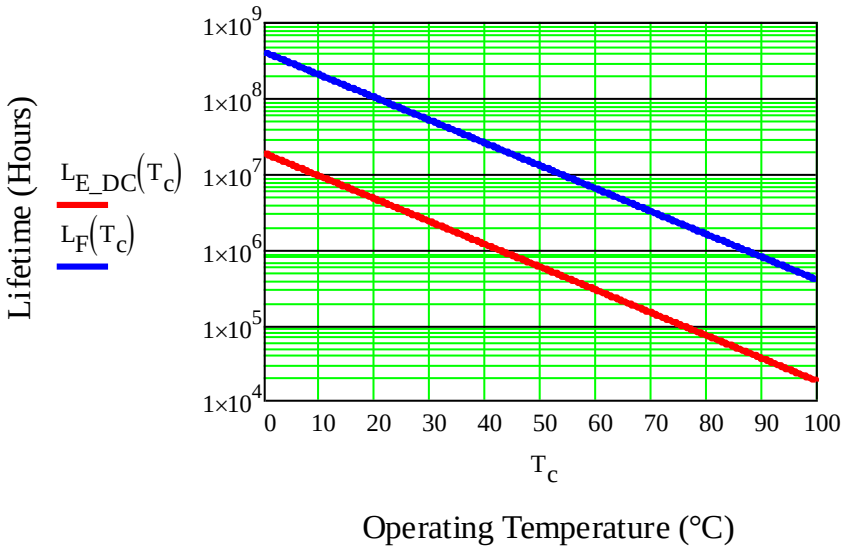


Figure 5.25: Lifetime projection for the conventional dc bus design with electrolytic capacitor (LE-DC) and the proposed ripple-port with film capacitor (LF). Over the entire temperature range the film capacitors exhibit superior longevity

5.2.5 Simulation results for the DC-link AC/DC

A 1kW single-phase PWM rectifier, which rectifies a 170Vp sinusoidal input voltage from the utility into a regulated 200V at the output, was simulated in PSIM. In Figure

5.26, the system's schematic is shown. Table 5.6 lists the parameters used in the simulation. In a conventional circuit, 1,330µF is required on the DC-link. However, using the ripple-port, only 80µF on the DC-link and 140µF for the ripple-port decoupling capacitor are required. Figure 5.27 shows the input $p_s(t)$, output P_0, and ripple-port $p_{rip}(t)$ power waveforms, which matches with the theoretical waveforms in Figure 5.24. Figure 5.27 also shows the double-line frequency power ripple that has been suppressed to a very small level with only 5% peak-to-peak ripple, which was arbitrarily chosen to prove the concept and can be further reduced in practice.

Table 5.7: AC/DC rectifier with ripple-port simulation parameters

Component	Value	Component	Value
V_s	120 Vrms	R_o	40
I_s	12.5Ap	f_s	100KHz
L_s	1.5mH	K_{pv}	0.01
C_{dc}	80uF	K_{iv}	100
C_D	140uF	K_{pi}	5
L_D	100uH	K_{ii}	500

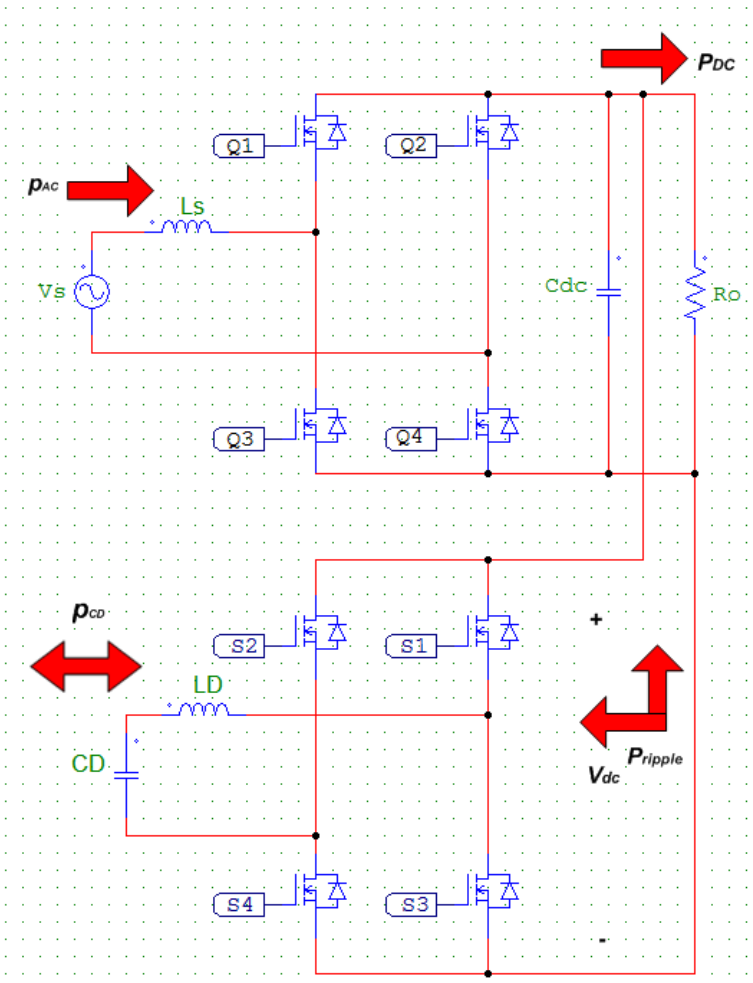


Figure 5.26: PSIM simulation schematic of a single-phase PWM rectifier with power decoupling ripple-port

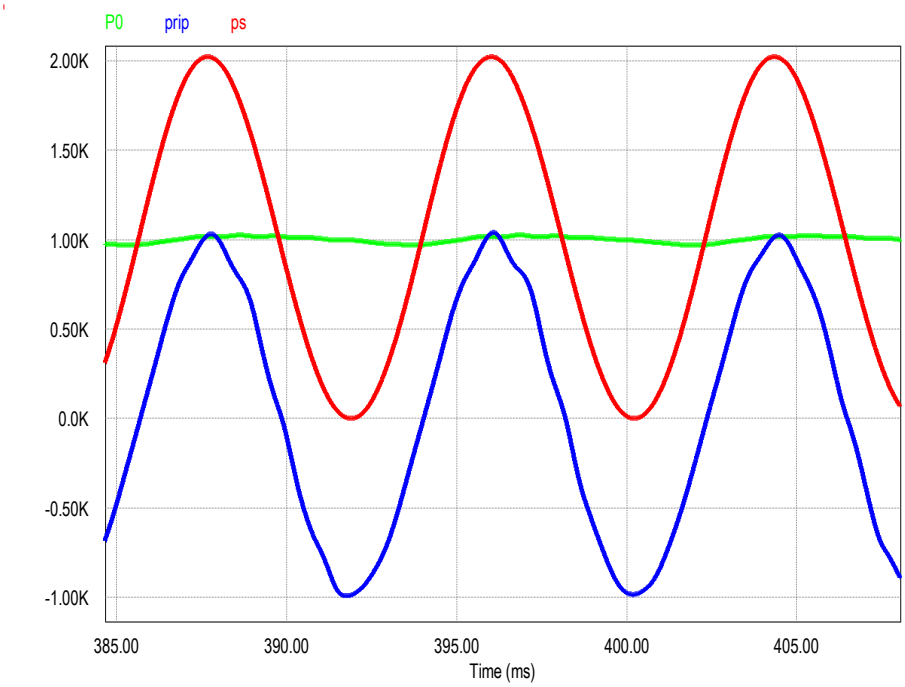


Figure 5.27: Simulation results - input, output, and ripple power waveforms

Figure 5.28 shows the output voltage, V_0, and current, I_0. Both show approximately 5% peak-to-peak ripple. In Figure 5.29, it is clearly observed that the input current $i_s(t)$ is in phase with the input voltage $v_s(t)$. This is verified by nearly unity power factor as shown in Figure 5.30. Figure 5.31 shows the calculated FFT for the input current $i_s(t)$, which indicates a very low THD. The calculated THD is 3.5%. On the DC-link side, Figure 5.32 shows the calculated FFT of the output power P_0, and it is clearly noticeable how the double-line frequency component is suppressed to a very low level (less than 5%). Figure 5.33 shows the regulated output voltage (V_0) on top of the input voltage ($v_s(t)$) and the voltage across the decoupling capacitor ($v_{CD}(t)$). It shows the 46 degree phase shift between $v_s(t)$ and $v_{CD}(t)$.

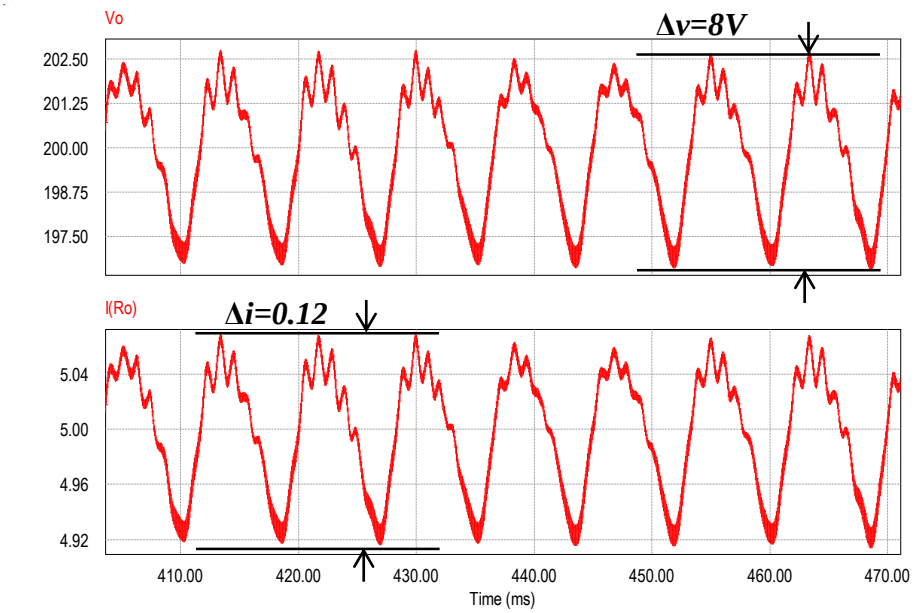


Figure 5.28: Output voltage (above), and output current (bottom)

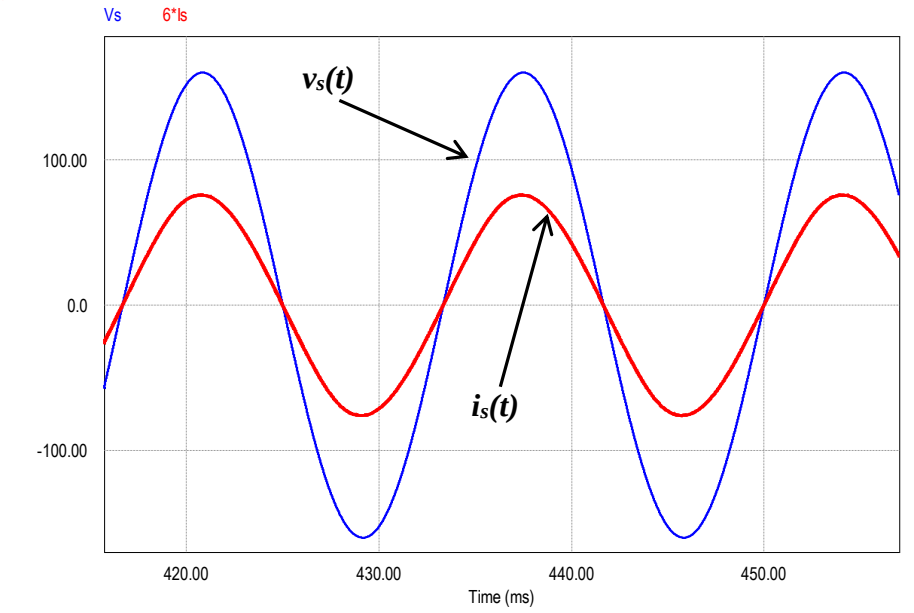


Figure 5.29: Input voltage and current (scaled for comparison)

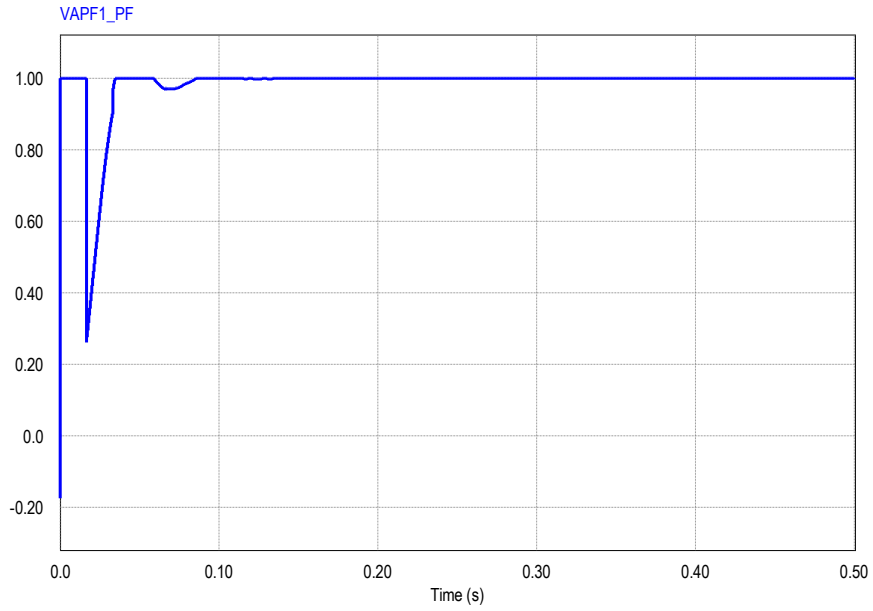


Figure 5.30: Power factor nearly unity (0.99)

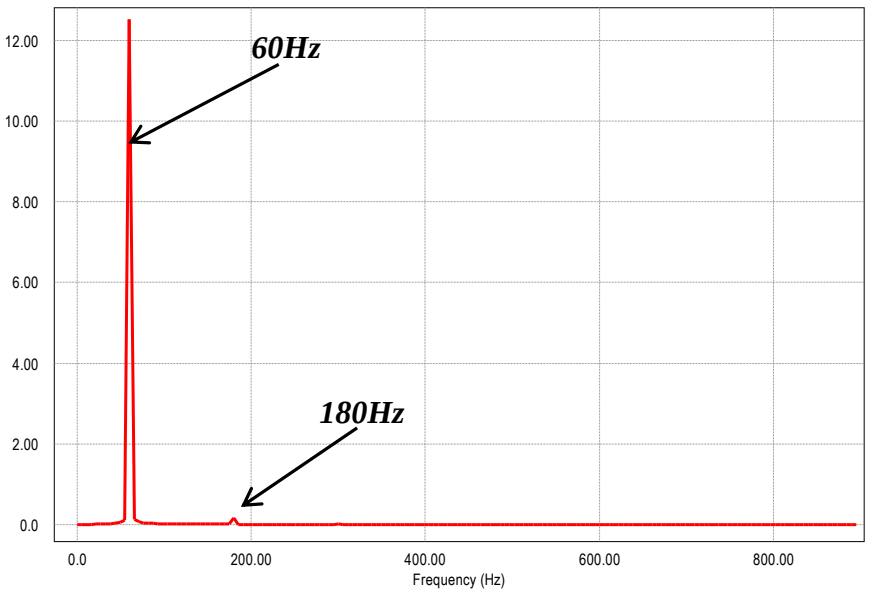


Figure 5.31: Calculated FFT of the input current ($i_s(t)$)

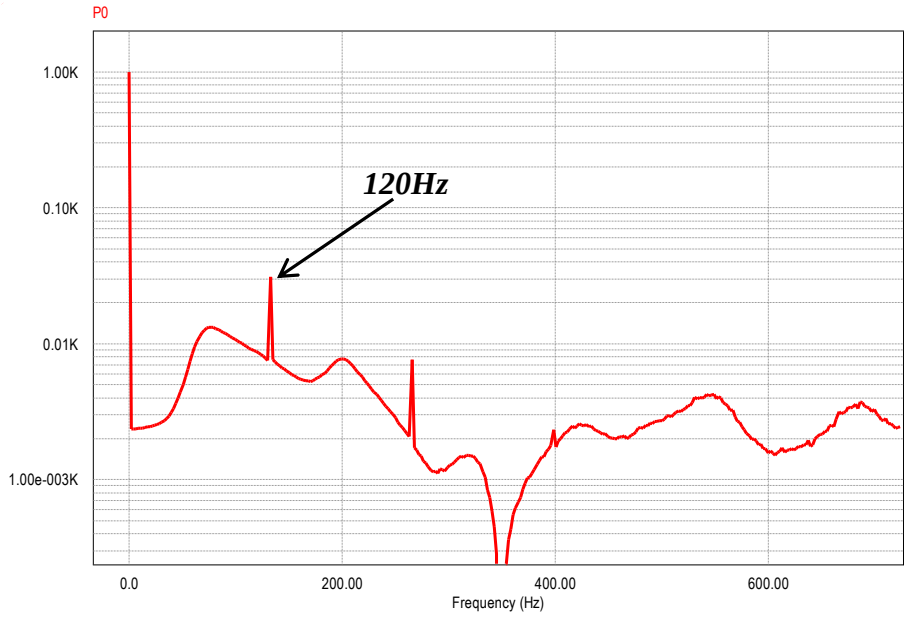


Figure 5.32: Calculated FFT of the output power (in dB)

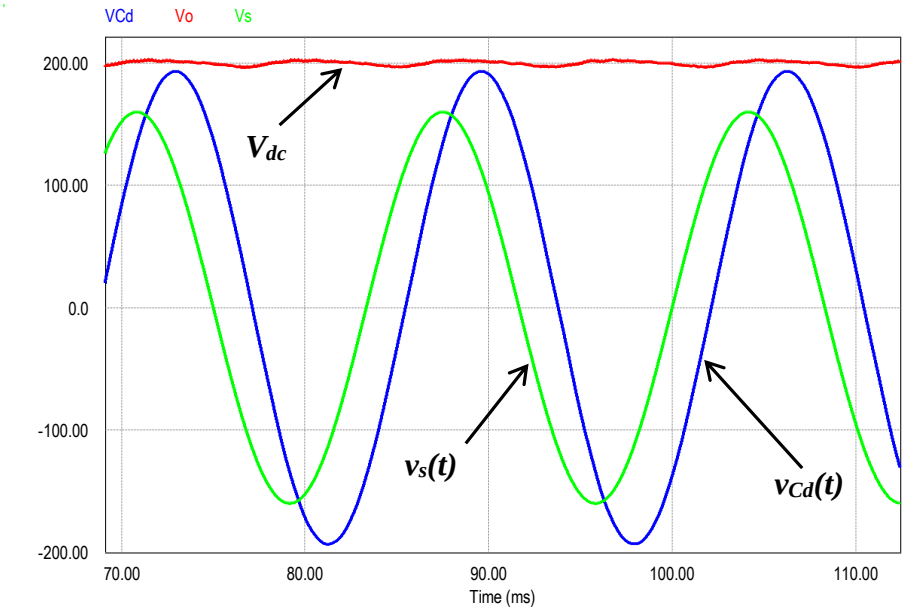


Figure 5.33: Input, output voltages, and the voltage across the decoupling capacitor

5.2.6 Experimental results – AC/DC rectifier with ripple-port

Figure 5.34 shows the experiment setup for the single-phase AC/DC rectifier with the proposed ripple-port. The AC/DC rectifier stage is implemented using the evaluation board from TI (UCC28070EVM). It consists of a diode bridge and two-phase interleaved PFC boost converter, as shown in Figure 5.35. Although the ripple-port concept was simulated using the PWM rectifier, the experimental results in this section show that its operation is completely independent of the type of the AC/DC topology. Table 5.7 lists the experiment operation parameters.

Table 5.8: AC/DC rectifier experimental components values

Component	Value	Component	Value
Input voltage	$20V_{rms}$ AC @ 60Hz	Decoupling capacitor (C_D)	40µF
DC-link voltage	$50V_{dc}$	Decoupling inductor (L_D)	100µH
DC-link capacitance (C_0)	100µF	Output power (P_0)	10W

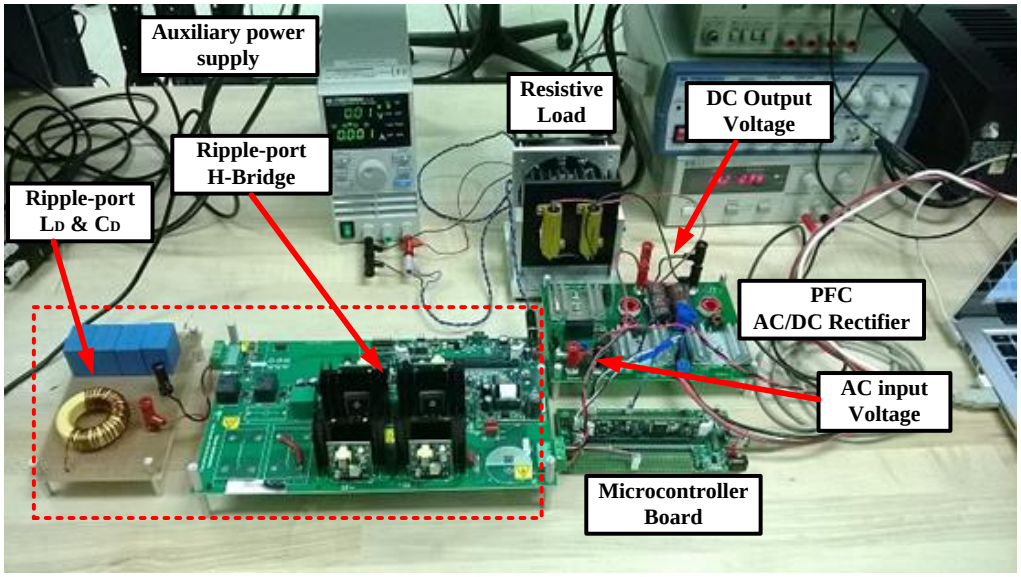


Figure 5.34: Single-phase AC/DC rectifier with ripple-port - experiment setup

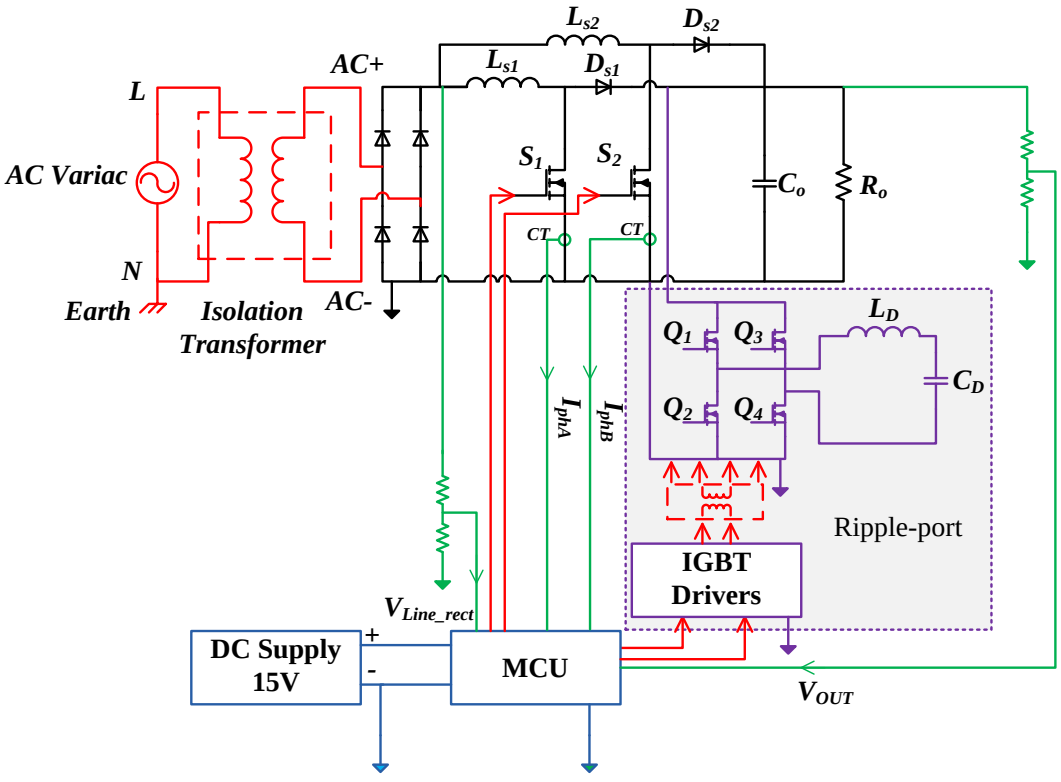


Figure 5.35: Single-phase AC/DC rectifier with ripple-port – experiment schematic

Figure 5.36 shows the DC-link output voltage (ch.3), decoupling LC filter's current (ch.2), and input (ch.1) and decoupling capacitor (ch.4) voltage waveforms. The depth of modulation of the ripple-port H-Bridge (DoM_{RP}) and the phase angle (ϕ) were manually tuned to minimize the double-line frequency ripple on the output DC side at DoM_{RP} = 0.848 and ϕ = 46°. It is clear that the double-line frequency ripple is significantly suppressed on the DC-link output voltage, which is almost ripple-free. In Figure 5.37, the experimentally measured FFT of the DC-link output voltage shows 47.2dB suppression of the double-line frequency (120Hz) ripple on the DC side.

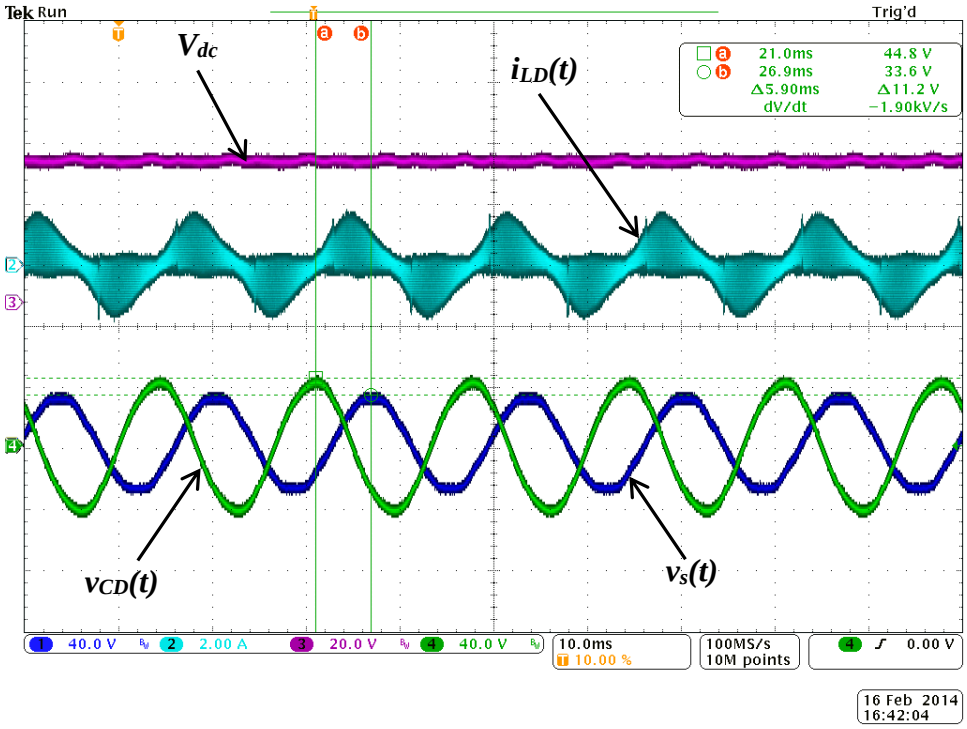


Figure 5.36: Experimental results: DC-link output voltage (ch.3), decoupling LC filter's current (ch.2), and input (ch.1) and decoupling capacitor (ch.4) voltage waveforms (with ripple-port)

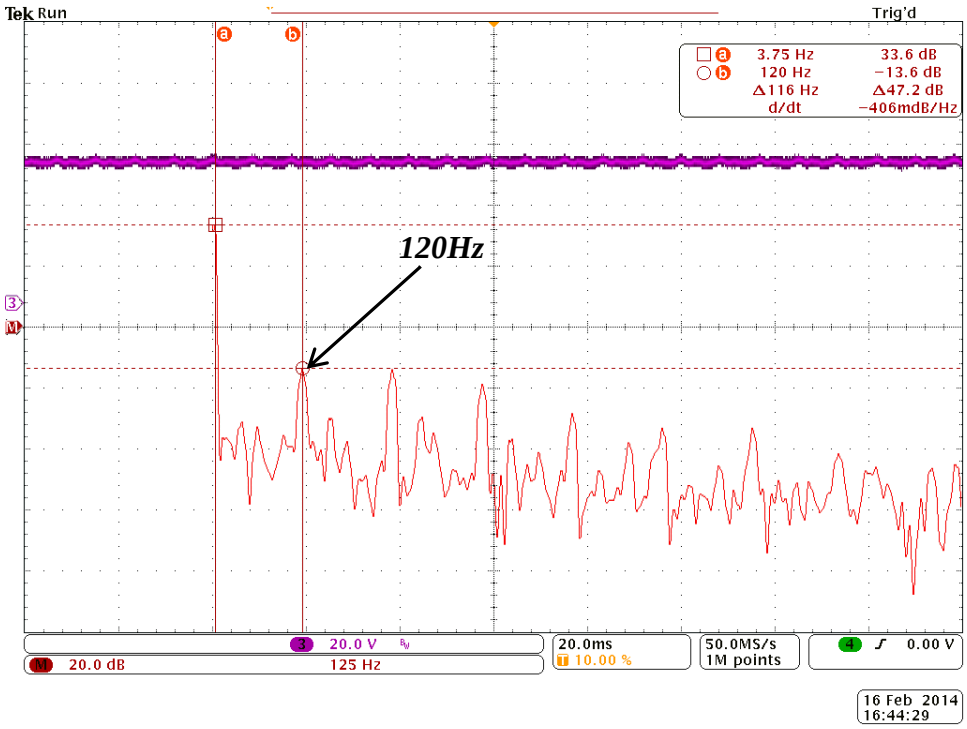


Figure 5.37: The experimentally measured FFT of the DC-link output voltage (with ripple-port)

To illustrate the efficacy of the ripple-port, the AC/DC rectifier stage was operated with the ripple-port disabled. In Figure 5.38, the increase in the 120Hz ripple on the DC output side can be easily noticed—8 V peak-to-peak voltage ripple. The measured FFT of the DC output voltage shows a 19.6dB increase in the 120Hz component compared to the previous case, as shown in Figure 5.39. Table 5.8 present a comparison of the system's performance in terms of double-line frequency ripple with and without the ripple-port.

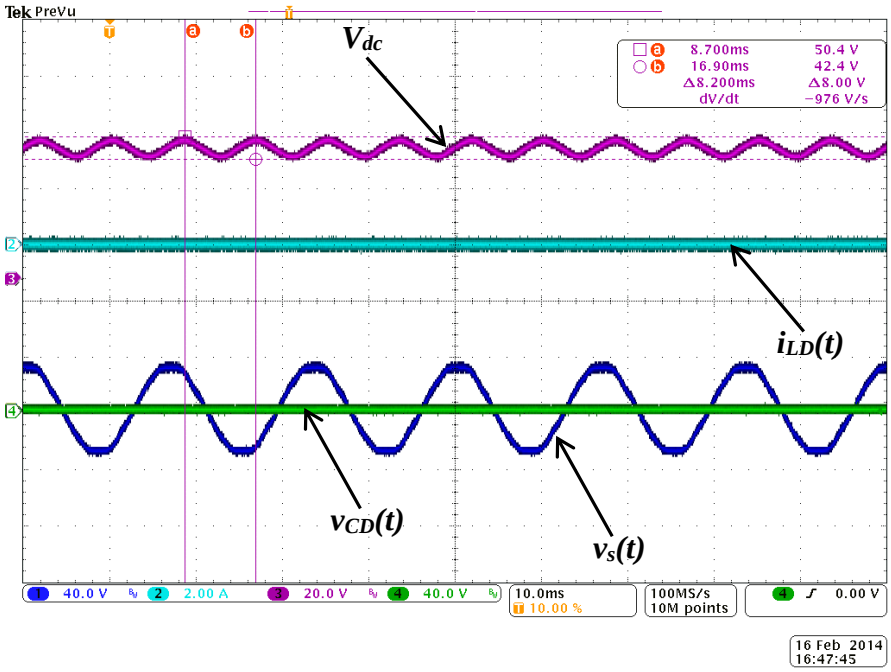


Figure 5.38: Experimental results: DC-link output voltage (ch.3), decoupling LC filter's current (ch.2), and input (ch.1) and decoupling capacitor (ch.4) voltage waveforms (without ripple-port)

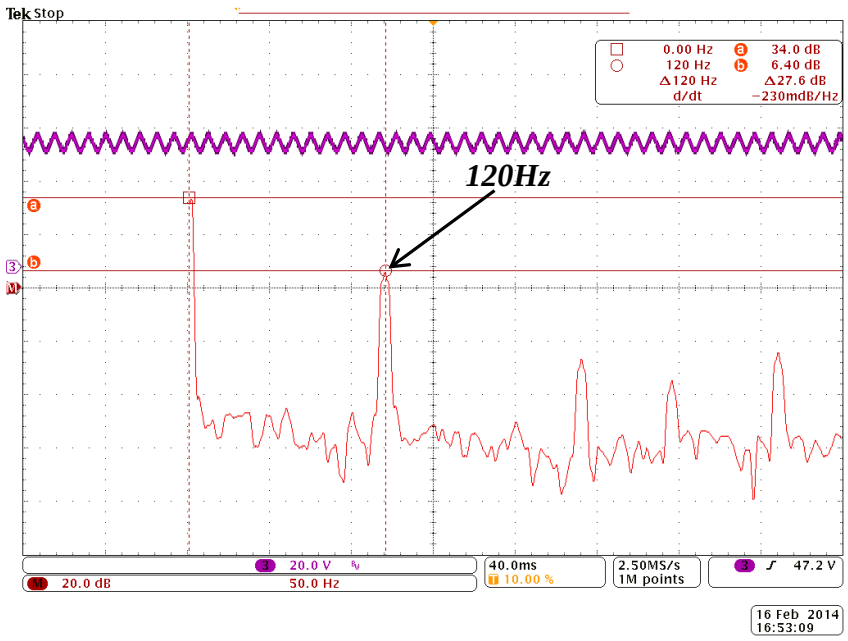


Figure 5.39: The experimentally measured FFT of the DC-link output voltage (without ripple-port)

Table 5.9: Comparison of operating the AC/DC system with and without the ripple-port

	DC voltage ripple (ΔV)	120 Hz of DC port current	120Hz relating to DC
Ripple-port activated	1.4V	-13.6 dB	47.2 dB
Ripple-port deactivated	8V	6.4 dB	27.6 dB
Ripple-port suppression		20 dB	

5.3 Conclusion

The ripple-port concept, for double-line frequency ripple cancellation, is presented in this section. It is implemented for both single-phase DC/AC inverter and AC/DC rectifier applications. First, the proposed module-integrated inverter (MII) is based on the commonly used two-stage inverter. A third port is added for ripple cancellation purposes; it simply attached to the DC-Link. This implies that the ripple-port could be added to many commercially available inverter topologies. Two configurations for implementing the proposed MII were examined by simulation, and the best was experimentally tested. Second, the ripple-port is connected to a single-phase AC/DC rectifier. Only 140μF is needed as decoupling capacitance. Simulation and experimental results were presented that proves the ripple cancellation concept without affecting the high performance of the PWM rectifier. The results show that the ripple-port is completely independent of the type of the AC/DC rectifier stage (PWM or diode bridge followed by boost PFC). For both applications, a very small capacitance is required, where a high reliability film capacitor

can be used instead of the bulky, low reliability electrolytic ones. Consequently, the system's reliability and power density are improved. The ripple-port can be completely designed and controlled independently of the main power stage design process.

6 DC-LINK BASED POWER DECOUPLING VERSUS THE RIPPLE-PORT POWER DECOUPLING TECHNIQUES

In this section, the proposed ripple-port MII, Figure 6.1, is compared against the conventional DC-link MII, Figure 6.2. In the conventional DC-link MII topology, the decoupling capacitor can be placed either on the low-voltage PV side or on the relatively high-voltage DC-link. In this study, the latter approach will be considered since less decoupling capacitance is needed for the same power rating. Thus, a smaller capacitor can be used. Yet, film capacitors are not a cost effective technology. More detail on the feasibility and the cost effectiveness of film capacitors are discussed later in the section. The aim of this comparative study is to thoroughly investigate the impact of the extra components, due to the ripple-port, on the efficiency and the cost of the MII—given that both topologies have the desired 25-year lifetime.

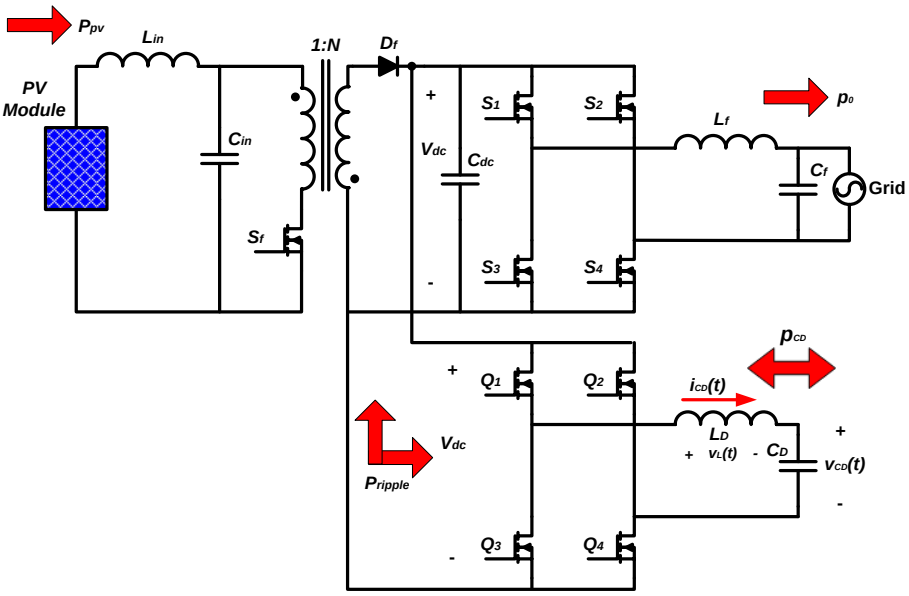


Figure 6.1: Ripple-port module-integrated inverter (RP-MII)

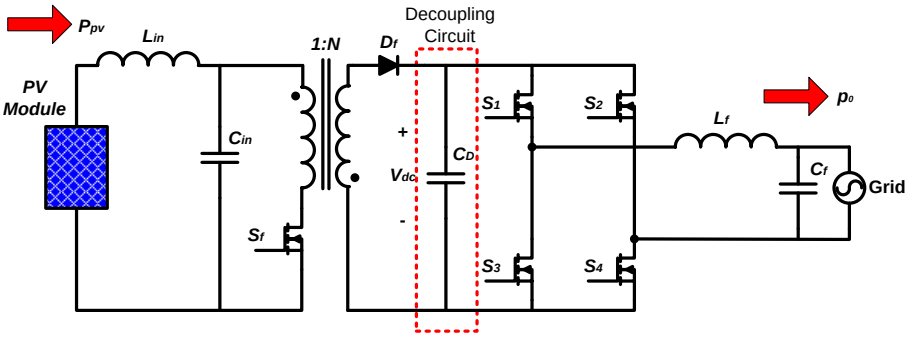


Figure 6.2: DC-link module-integrated inverter (DC-MII)

The same design specifications in 2.3 are considered for this study also, which are: P_{in}=235W, open circuit voltage (V_{oc}) 37 V, maximum power voltage (V_{MPP}) 30.1 V, short circuit current (I_{sc}) 8.5 A, maximum power current (I_{MPP}) 7.81 A, 200V DC-link voltage—for V_0=[90 – 132]V_{rms} [39] grid-connected applications.

The rest of this section is organized as follows: First, both topologies are designed for high-reliability in 6.1. Then, the efficiency calculations are presented in 6.2. In 6.3, the price comparison is presented, and finally, a conclusion is drawn in 6.4.

6.1 Design for high-reliability

In this section, the required decoupling capacitance is calculated for both topologies. Then, for the conventional DC-link MII topology, the decoupling capacitance is derated in order to have a 25-year lifetime.

6.1.1 Design the decoupling capacitor for the conventional DC-link MII

This decoupling technique belongs to type IIa1, as shown in section 4, and the required decoupling capacitance is calculated using (6.1). The capacitance value results from (6.1) can be implemented using either electrolytic or film capacitor technology. However, implementing this relatively large capacitance by film capacitor technology is not practically feasible due to its high cost and large size. Hence, this decoupling capacitance is implemented by electrolytic capacitor. The price and size of different capacitor options are presented later in this section.

$$C_D = \frac{P_{in}}{\omega V_{dc} \Delta \tilde{v}_{dc}} \qquad (6.1)$$

$$C_D = \frac{235}{377 * 200 * 10} \cong 312 \mu F$$

Usually, the base lifetime (L_0) is given by the manufacturer for specific test conditions, and it can be found in the datasheet of the selected capacitor. However, the capacitor's lifetime can be increased by running the capacitor at operating conditions below the manufacturer's ratings. Then, the projected lifetime is calculated using (6.2), which is a function of the base lifetime and the expected operating temperature (T) and voltage (V_{op}).

$$L = \frac{L_0\left(2^{\left(T_{ref}-T\right)/10}\right)}{\left(\frac{V_{op}}{V_r}\right)^{2.6087\left[\left(V_{op}/V_r\right)+0.5167\right]}} \tag{6.2}$$

where V_r and T_{ref} are the capacitor's rated voltage and temperature, respectively.

If the DC-link capacitor's voltage is rated at twice the expected operating voltage (V_{op}), then, according to (6.2), the projected lifetime (L) will be increased by a factor of six. Also, by design, the capacitor's operating temperature is well-controlled to remain at least 10˚C below its maximum rated temperature. This, in turn, guarantees a minimum lifetime of double the base lifetime. Notice that the rise in the capacitor's temperature is governed by its ESR (equivalent series resistor) and the amount of the current ripple flows through it. So, the larger the ESR, the more heat is generated, and thus, the shorter the capacitor's lifetime—electrolytic capacitor is known to have a large ESR. Although the results in

[116] show that the capacitor's temperature could reach as high as 100˚C, the measurements in section 2 show that the module's operating temperature was as high as 65˚C. Moreover, according to [22], the PV module was operating at temperatures less than 60˚C for 95% of the time. Hence, it is a fair assumption that the capacitor's maximum temperature is 10˚C less than its rated one. Following these assumptions, the expected lifetime is at least 12 times the base time, as shown in (6.3).

$$L = \frac{2L_0}{0.15907} = 12.57L_0 \tag{6.3}$$

However, using a capacitor with a rated voltage twice the maximum expected operating voltage is definitely going to increase the cost. Moreover, operating the capacitor at a temperature level with 10˚C lower than its rated temperature may need extra requirements. For example, using a larger inductance results in a reduced current ripple, consequently, lower temperature rise in the capacitor. However, this could increase the losses in the inductor and the cost of the MII. Quantifying these practical techniques is beyond the scope of this section.

Two electrolytic capacitors are considered as a case study, as shown in Table 6.1 [117, 118]. The purpose of this comparison is not to study the performance or the quality of different manufacturers' products rather than showing an actual lifetime calculations. Both capacitors' rated voltage is 450V. According to (6.3), option I and II, in Table 6.1, are

expected to last for 4.3 years and 7.17 years, respectively. Table 6.1 shows that option II has a lifetime 1.66 times the lifetime of the first option. But, its price is 2.47 times the price of option I. However, the lifetime is not the only thing that has improved in option II; its operating temperature is 20˚C higher and its ESR is almost half the ESR of option I.

Table 6.1: Two electrolytic capacitor options

Manufacturer	Capacitance	Base lifetime	ESR	Size	Price ($)
I - Panasonic Electronic - Electrolytic	330µF	3,000 Hrs @ 85°C	553 mΩ	30mm x 50mm (D x H)	5.89
II - Vishay - Electrolytic	330µF	5,000 Hrs @ 105°C	300 mΩ	35mm x 40mm (D x H)	14.56
EPCOS - Film	40µF	200,000 Hrs @ V_R, 85°C	1.9 mΩ	57.5mm x 30mm x 45mm (LxWxH)	10.487

6.1.1.1 Derating the decoupling capacitor at the DC-link

It is required for the microinverter, built using the convention DC-link approach, to keep performing and meet the design specifications, such as voltage ripple and THD. The voltage ripple on the DC-link is directly related to the capacitance value. However, it is well-known that the end of life for the aluminum electrolytic capacitor is determined by

one of the following factors: (1) capacitance decreases by at least 20%, (2) or the dissipation factor (or ESR) increases by at least 300%. In this study, the change in the electrolytic capacitor is considered as the main factor that determines its end of life, as shown in Figure 6.3. Thus, this decrement in the capacitance needs be taken into account and compensated for at the design stage by derating the required capacitance.

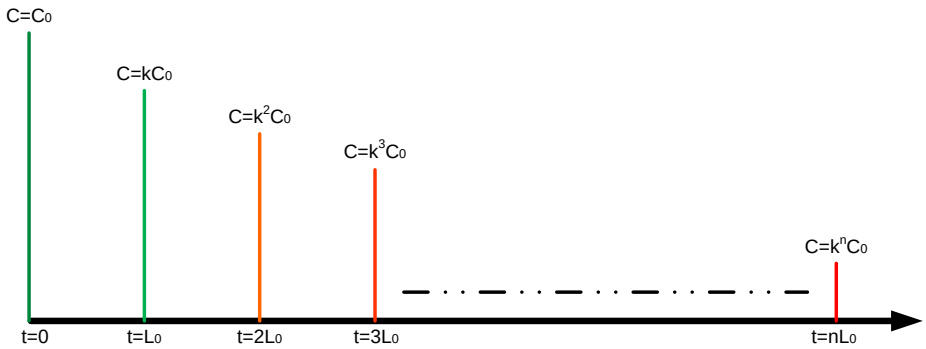


Figure 6.3: Pictorial illustration of the capacitance decrement with time

The desired capacitance (C_D) that the MII needs to have by the end of its expected lifetime is given in (6.4). In order to cancel the double-line frequency ripple, the designer must make sure that at the end of the MII's lifetime the decoupling capacitance matches with (6.1). Then, the required initial capacitance (C_0) can be calculated using (6.4), where (n) is the ratio of the desired lifetime to the base lifetime given in (6.3).

$$C_D = (k)^n C_o = (k)^{\frac{L_d}{L}} C_o \tag{6.4}$$

k=1-ΔC% is determined based on the allowed ripple on the DC-link that can be tolerated without significantly affecting the MPPT performance as well as the THD of the injected output current. However, the capacitor is considered to have a soft failure if its capacitance decreased by 20% of its initial value [119]. Considering option II that has a longer lifetime (62,850 hours), the initial capacitance (C_0) is 1.863 times C_D according to (6.4)—given a 20-year lifetime (175,200 hours). From (6.1), 312 µF is required for decoupling purposes. Thus, C_0=1.863*312µF=581.26µF. A 560µF capacitor from Nichicon (LGX2G561MELC40) is considered with a base lifetime of 5,000 hours and $10.36 unit price [120].

6.1.2 Design the decoupling capacitor for the DC-link based ripple-port MII

It was presented in section five that the decoupling capacitance for the DC-link ripple-port MII is calculated as given in (6.5); and for the system's specifications given in section 6.1, 40µF is needed, which can be implemented by film capacitor technology.

$$C_D = \frac{2P_{in}}{\omega V_{CDp}^2}$$

$$C_D = \frac{2*(235)}{377*(180)^2} \cong 40\mu F \tag{6.5}$$

Table 6.1 shows the main parameters for a film capacitor from EPCOS [121]. With 200,000 hours base lifetime, this capacitor is expected to last for more than 22 years if it operates at the rated 85˚C temperature, which is not the case as it was explained previously in this section. This suggests that a film capacitor can be designed to operate at the rated conditions (voltage and temperature), yet, it will last for longer time compared to the electrolytic capacitor. Moreover, the *ESR* of the electrolytic capacitor is at least 100 times larger than the film capacitor one.

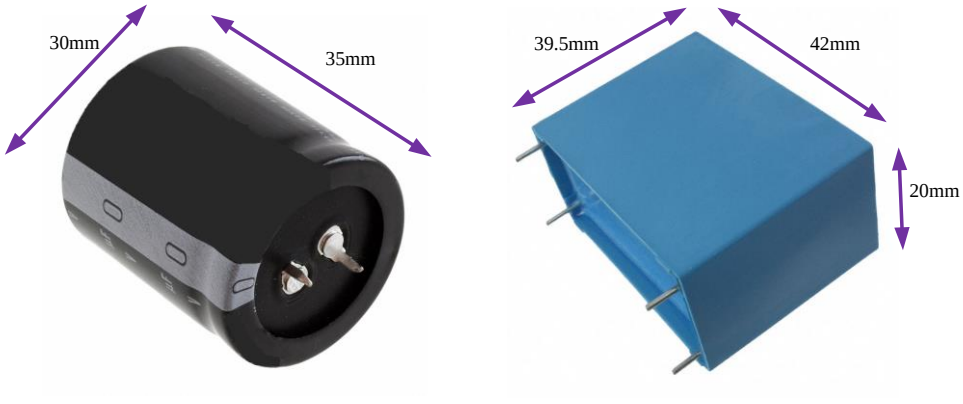
6.1.2.1 Multiple capacitor in parallel option

Paralleling number of capacitors with smaller capacitance is a very common engineering practice mainly to reduce the equivalent ESR, which will be divided by the number of capacitors. Hence, the calculated decoupling capacitor for both approaches (electrolytic and film approaches) will be implemented by four paralleled capacitors. Table 6.2 lists the main parameters of each selected capacitor. However, in aluminum electrolytic capacitor technology, the *ESR* is a function of the capacitance and the operating frequency, as given in (6.6). This means that when a small capacitance is used, its *ESR* is expected to be relatively larger. For example, if a 150 µF capacitor is considered, its *ESR* is 910m Ω, which is almost three times of the larger capacitor (560 µF).

$$\tan(\delta) = DF = 2\pi fCESR \Rightarrow ESR = \frac{DF}{2\pi fC} \tag{6.6}$$

Table 6.2: Parallel capacitors option

Manufacturer	Capacitance	Base lifetime	ESR	Size	Price ($)
EPCOS Inc (B43505A5157M)	150µF	5000 Hrs @ 105°C	910m Ω	30mm x 35mm (DxH)	5.55x4
EPCOS Inc (B32676E4106K)	10µF	200,000 Hrs at V_R, 85 °C	7.3m Ω	42mm x 20mm x 39.50mm (LxWxH)	3.88x4



Aluminum Electrolytic Capacitor
C=150µF, ESR=910m Ω

Metalized Polypropylene Film Capacitor
C=10µF, ESR=7.3m Ω

Figure 6.4: Aluminum electrolytic and metalized polypropylene film capacitors – comparison

6.1.3 Electrolytic versus film capacitor

Many studies have been published recently on the reliability of the DC-link capacitor and the technology used to enhance the inverter's performance as well as reliability [122, 123]. In [122], a detailed analysis on designing the DC-link capacitor for high-reliability is presented. Failure modes and mechanisms for three capacitors' technologies (aluminum electrolytic, metalized polypropylene film, and multi-layer ceramic capacitors) are

investigated in the study [122].

The aluminum electrolytic capacitor has high energy density at low cost, but at the expense of relatively high *ESR*, low current ripple capability, and relatively short lifetime due to evaporation of electrolyte. On the other hand, metalized polypropylene film (MPPF) capacitor shows superiority in terms of current ripple capability and low ESR. However, it suffers from a low energy density (large size) and moderate operating temperature [122]. Moreover, the self-healing capability of the MPPF capacitor makes it an attractive option when compared to aluminum electrolytic capacitor.

6.2 Efficiency calculation

In this section the power loss due to the added component in each MII topology is examined. For the conventional DC-link MII, the added power loss is due to the derated DC-link capacitor. And, for the proposed DC-link ripple-port, the power loss is due to the added H-Bridge (4 MOSFETs) and the decoupling LC filter.

6.2.1 DC-link current

$I_{C,rms}$ is the rms (root mean square) value of the current ripple flows in the DC-link capacitor. I_{Crms} is needed to calculate the power loss in the DC-link capacitor's *ESR*. The inverter's input current is needed to calculate the power loss in the H-Bridge's MOSFETs. The DC-link capacitor's current is a function of the output current of the input DC/DC stage (i_{dc0}) and the H-Bridge inverter's current (i_{inv}) as given in (6.7).

$$i_{C_{DC}}(t) = i_{dc0}(t) - i_{inv}(t)$$
$$I_{C_{DC},rms} = I_{dc0,rms} - I_{inv,rms} \tag{6.7}$$

i_{dc0} depends on the type of the DC/DC stage, however, for PV-MII applications, it should be a boost-type converter. Considering the most common flyback topology, the output current is given in (6.8).

$$I_{dc0,rms} = \left(1 - D_{DC/DC}\right) * \left(\frac{N_p}{N_s D_{DC/DC}} I_{mmp} \right)^2 \tag{6.8}$$

The inverter's input current can be calculated as shown in (6.9), using the H-Bridge's output voltage from [124].

$$i_0(t) = \frac{v_{B0}(t)}{Z_0} \Rightarrow i_0(t) = \frac{1 + R_0 C_f s}{R_0 L_f C_f s^2 + L_f s + R_0} v_{B0}(t)$$
$$v_{B0}(t) = 2V_{DC} M \cos\left(\omega_0 t\right) + \frac{8V_{DC}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{2m} j_{2n-1}\left(m\pi M\right) \cos\left(\left[m + n - 1\right]\pi\right) \cos\left(2m\omega_c t + \left[2n - 1\right]\omega_0 t\right) \tag{6.9}$$

Considering a lossless system, the rms value of the inverter's input current is calculated as follows:

$$P_{DC} = P_0$$

$$V_{DC} I_{inv,rms} = V_{B0,rms} I_{0,rms} \tag{6.10}$$

$$I_{inv,rms} = \frac{V_{B0,rms} I_{0,rms}}{V_{DC}}$$

6.2.2 DC-link MII

Because of the derated DC-link capacitor's ESR_{CD}, this approach will experience more power loss in the form of dissipated heat. It is very important to precisely calculate the power loss due to the ESR_{CD} not only to estimate the system's efficiency, but also to calculate the increment in the capacitor's operating temperature, as given in (6.11). This increase in the operating temperature will potentially decrease the capacitor's expected lifetime according to (6.2).

$$T_{CD} = T_A + P_{loss} * R_{th-C-A} = T_A + I_{C,rms}^2 * ESR_{CD} * R_{th-C-A} \tag{6.11}$$

This power loss is calculated using (6.12).

$$P_{loss} = I_{C,rms}^2 * ESR_{CD} \tag{6.12}$$

6.2.3 DC-link based ripple-port MII

The power loss due to the extra H-Bridge (four MOSFETs) and the decoupling LC filter is calculated. However, the dominant power loss is due to the MOSFETs since they are hard-switched. The power loss in MOSFETs can be estimated following the analysis in [125]. The main power loss equations, for a PWM controlled single-phase inverter, are presented next.

6.2.3.1 Conduction power loss

The power loss in the tipple-port's H-Bridge is divided into conduction and switching losses. The conduction losses in MOSFET and its body diode are given in (6.13) and (6.14), respectively.

$$P_{C\_MOS} = R_{DS-ON} * I_{D,rms}^2 = R_{DS-ON} * I_0^2 * \left(\frac{1}{8} + \frac{M}{3\pi}\cos(\phi)\right) \tag{6.13}$$

$$P_{C\_Diode} = v_{D0} * I_{Fav} + R_D * I_{F,rms}^2 = v_{D0} * I_0 * \left(\frac{1}{2\pi} - \frac{M}{8}\cos(\phi)\right) + R_D * I_0^2 * \left(\frac{1}{8} - \frac{M}{3\pi}\cos(\phi)\right) \tag{6.14}$$

6.2.3.2 Switching power loss

Table 6.3 shows how to calculate the energy loss due to turning ON and OFF the MOSFET. Because the drain-source voltage nonlinearly depends on the MOSFET's output capacitance, the two-point approximation is used to estimate the rise and falling

time of the drain-source voltage, as shown in Table 6.3 [125]. In the PWM AC power loss calculation, the $I_{D,ON}$ and $I_{D,OFF}$ can be considered to equal the average value of the output current over a half link cycle $I_{D,ON} = I_{D,OFF} = \frac{I_0}{\pi}$

Table 6.3: Switching power loss calculations

Device	Switching losses
MOSFET	$P_{SW\_MOS} = \left(E_{ON,MOS} + E_{OFF,MOS}\right) * f_{SW}$ where $E_{ON,MOS} = V_{DC} * I_{D,ON} * \frac{t_{ri} + t_{fv}}{2} + Q_{rr} * V_{DC}$ $E_{OFF,MOS} = V_{DC} * I_{D,OFF} * \frac{t_{rv} + t_{fi}}{2}$ $t_{fv} = \frac{t_{fv1} + t_{fv2}}{2}$ $t_{fv1} = \left(V_{DC} - R_{DS-ON} * I_{D,ON}\right) * R_G * \frac{C_{GD1}}{V_G - V_{plateau}}$ $t_{fv2} = \left(V_{DC} - R_{DS-ON} * I_{D,ON}\right) * R_G * \frac{C_{GD2}}{V_G - V_{plateau}}$ $t_{rv} = \frac{t_{rv1} + t_{rv2}}{2}$ $t_{rv1} = \left(V_{DC} - R_{DS-ON} * I_{D,ON}\right) * R_G * \frac{C_{GD1}}{V_{plateau}}$ $t_{rv2} = \left(V_{DC} - R_{DS-ON} * I_{D,ON}\right) * R_G * \frac{C_{GD2}}{V_{plateau}}$
Diode	$P_{SW\_Diode} = \left(E_{ON,Diode} + E_{OFF,Didoe}\right) * f_{SW} \approx E_{ON,Diode} * f_{SW}$ $E_{ON,Didoe} = \frac{1}{4} * Q_{rr} * V_{DC}$

6.3 Comparison

The price and power loss, due to the capacitor's ESR, of each approach are presented in this section. Table 6.4 shows the volume, power loss, and price of both the electrolytic and film capacitors. It shows that the film capacitor approach results in 26% increase in the volume. However, film capacitor approach turned out to be 30% less expensive.

Table 6.4: Paralleled capacitors implementation comparison

	Volume	Power loss	Price ($)
Electrolytic capacitors	$4x24.74cm^3=99cm^3$	278.8 mW	22.2
Film Capacitor	$4x33.18cm^3=134.4cm^3$	6.73 mW	15.52

Table 6.5 shows the distribution of the power losses in one MOSFET, which conclude that an H-Bridge (four MOSFETs) will have a total power loss (P_{total}) of 18.73 W. This translates into 7.97%. However, Table 6.5 shows that the dominant cause of the power losses in MOSFET occurs at the turn ON instant. It accounts for 68% of the total power loss, as shown in Figure 6.5. The root cause of this power loss is the reverse recovery in the boy diode. Hence, in order to improve the performance of the ripple-port, the losses due to the reverse recovery need to be suppressed. One simple and straightforward approach is to use new semiconductor MOSFET, such as SiC or Gan. Also employing

zero voltage switching (ZVS) technique can completely eliminate the turn ON losses.

Table 6.5: MOSFET power loss

	Conduction Loss	Switching Loss			Total loss by device
		Turn ON	Turn OFF	Total	
MOSFET	0.3384	3.1709	0.2978	3.4687	3.8071
Body Diode	0.1254	0.75			0.8754
Total power loss	0.4638	4.2187			4.6825

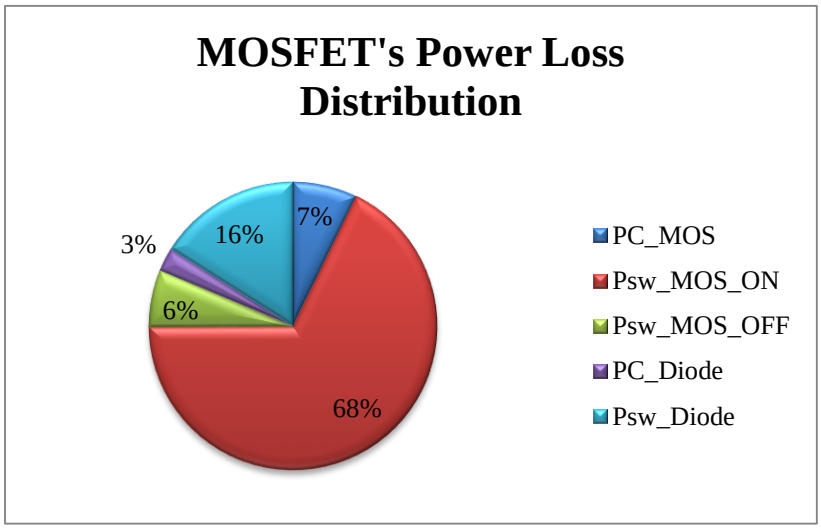


Figure 6.5: MOSFET's power losses distribution

6.4 Conclusion

The proposed DC-link based ripple-port PV-MII topology, which is presented in section five, was compared to the conventional DC-link based inverter in this section. For a 20 years lifetime, the efficiency, size, and price of both configurations were presented. It was found that the proposed ripple-port topology is competitive with the conventional topology in terms of size and price. Although the film capacitor approach results in 26% increase in the volume, it turned out to be 30% less expensive. Given the current semiconductor devices state, there is approximately 8% power loss due to the extra four switches introduced by the proposed ripple-port (H-Bridge). However, 68% of these power losses can be eliminated by either using a new semiconductor technology (GaN, SiC) or employing ZVS technique.

7 AC-LINK BASED RIPPLE-PORT [*]

7.1 High-frequency AC-link MII

In the section V, the impact of the number of capacitors on the reliability was presented. In addition to reducing the value of the decoupling capacitance, reducing the number of the capacitors will decrease the failure rate of the inverter. Another way to implement the ripple-port concept is by attaching it to a multi-stage inverter at a high-frequency AC link. Figure 7.1 shows a general block diagram of the proposed AC-link based ripple-port. As it was presented in section 5, the proposed technique can be applied for both DC/AC and AC/DC power conversion applications. In this section, it will be implemented for PV-MII application. The proposed MII can be implemented in two different topology configurations, based on the way that the ripple-port is added to the inverter: a separated ripple-port shown in Figure 7.2 or an integrated ripple-port shown in Figure 7.3. By controlling the power flow at the AC-link the double-frequency ripple from the grid-connection is prevented from propagating to the PV module on the dc port. This improves energy harvest as it was illustrated in section four. When the input power from the PV module is greater than the instantaneous output power to the utility the extra power is stored in the decoupling capacitor. This power will be transferred into the output side (grid utility) when the input PV power is lower than the output grid. Figure 7.3 shows how the

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ripple-port can be coupled to the ac-link in the main circuit topology by adding an additional transformer winding, which gives the designer the ability to control the input voltage of the ripple-port by adjusting the turn's ratio. This degree of freedom in the design of ripple-port, however, increases the complexity of the transformer design [126].

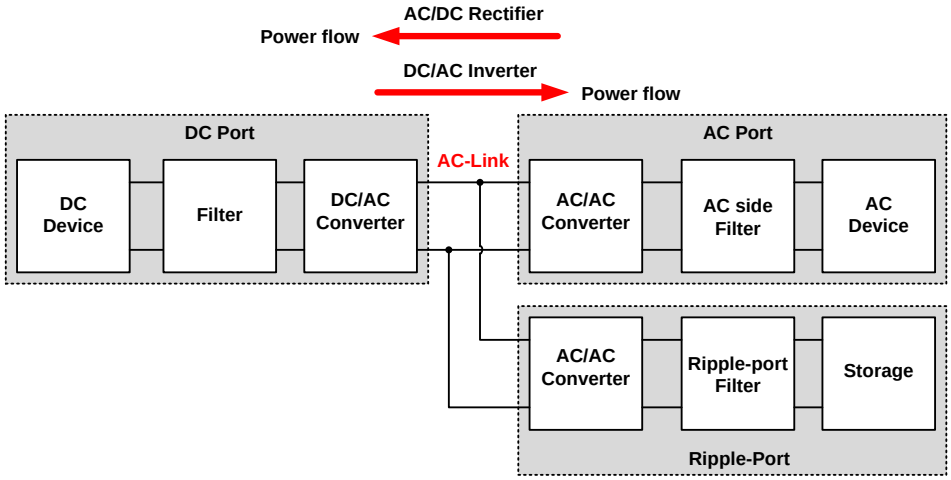

Figure 7.1: A general system block diagram of AC-link based ripple-port

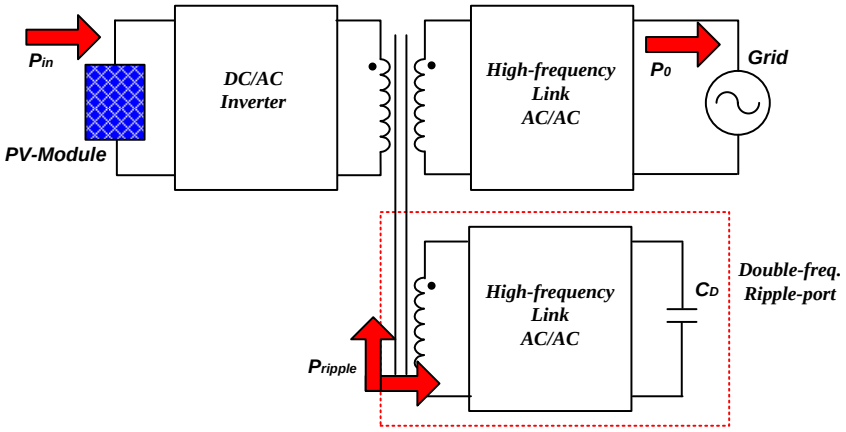

Figure 7.2: AC link ripple-port concept – separate winding configuration

Another approach for implementing the ripple-port is by integrating it to the secondary side of the transformer as shown in Figure 7.3. Although a simpler transformer design, integrating the ripple-port constrains the input voltage of the ripple port to be equal to the input voltage of the high frequency link output converter, which is governed by the grid voltage. In either case, the DC/AC stage on the PV-side generates a high frequency bipolar square wave for efficient use of the magnetic core and can be implemented with either a push-pull or a full-bridge based converter as shown in Figure 7.4.

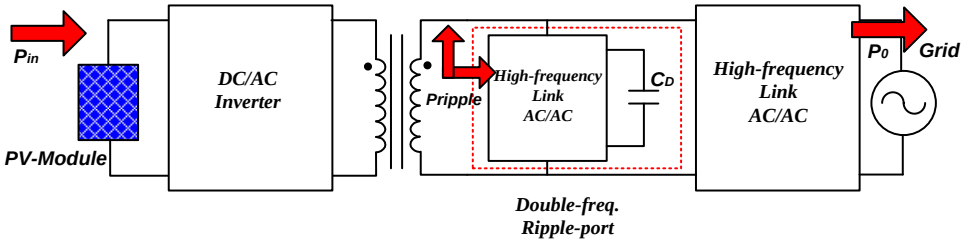

Figure 7.3: AC link ripple-port concept – integrated single winding

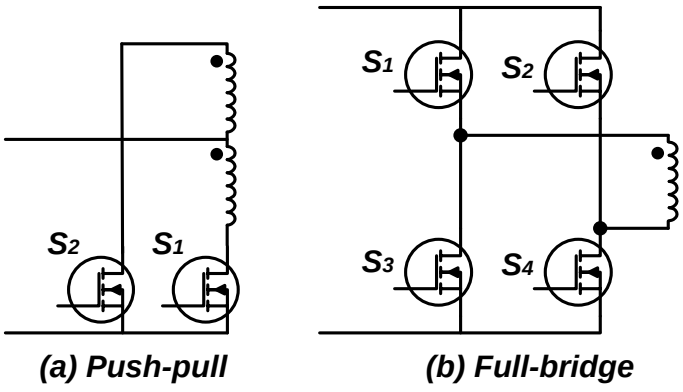

Figure 7.4: Two possible converters for DC/AC stage at the PV-side

7.1.1 Integrated ripple-port MII implementation (i-RP-MII)

Figure 7.5 shows the implementation of the integrated ripple-port configuration. The full-bridge is switching at f_{s1} with a duty ratio of half. Both high-frequency link AC/AC converters, on the secondary side, are switching at f_{s2}, which has to be faster than fs1 (multiple of f_{s1}). Bidirectional switches are used for both converters to provide a bidirectional current path. Two bidirectional switch configurations are shown in Figure 7.6. The common-source ac switch enables the same gate drive signal to be applied to both MOSFETs, which reduces the requirements for high-side isolated gate drives. However, applying the same gate signal for both MOSFTs implies a hard switching, which means that snubber circuits are needed to prevent damaging the MOSFETs. Hence, extra cost and higher power losses. In practice an external anti-parallel Schottky diode may be used to achieve lower losses. Another approach of switching the bidirectional switches, in high-frequency AC/AC converter, is "four-step switching" technique [127, 128], which guarantees to provide a path for the output current during the commutation period while eliminating the need for snubber circuit. It also provides partial soft switching. This switching technique is thoroughly presented later in this section.

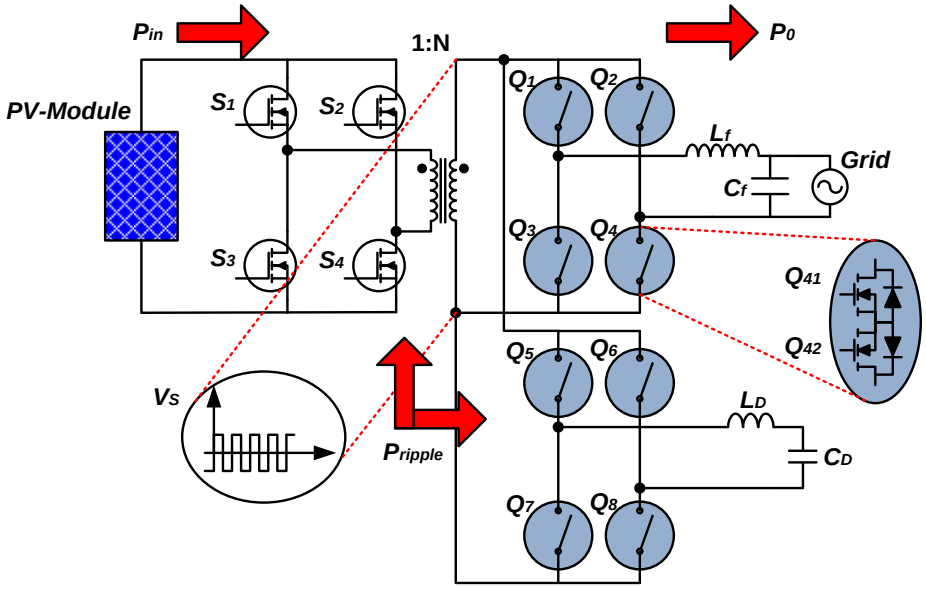

Figure 7.5: AC-link based inverter with an integrated ripple-port

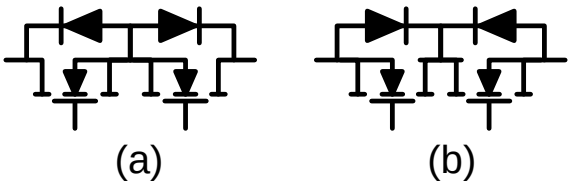

Figure 7.6: Bidirectional switch configuration: (a) common-source, (b) common-drain configurations

7.1.2 Controlling the HF link PWM inverters

The gate signals that control both high-frequency link AC/AC converters are generated as shown in Figure 7.7. V_{0ref} is the output voltage reference, and $V_{ripple\text{-}ref}$ is the voltage across the decoupling capacitor reference, which has the amplitude and phase angle as shown in (5.9) and (5.10).

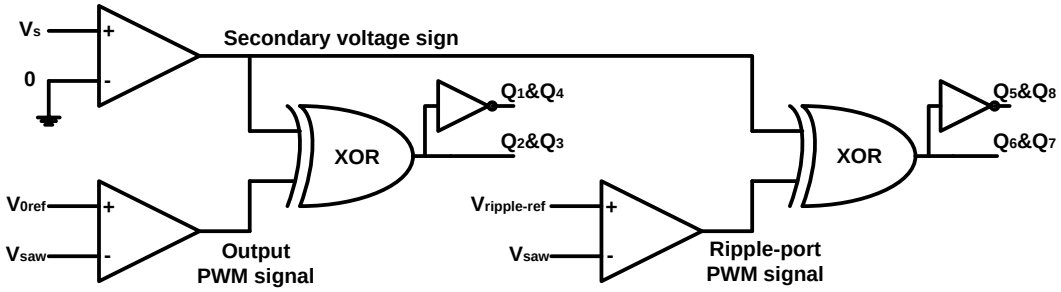

Figure 7.7: Control Circuit: high-frequency AC/AC converter driving signals generation

7.2 Controlling the bidirectional AC/AC H-Bridge

Table 7.1 shows all the possible static switch states for the high-frequency AC/AC converter shown in Figure 7.5. The polarity of the load current does not affect the static switch states, which are: State 1 when Q_1, Q_4 are ON and State 2 when Q_2, Q_3 are ON. For each state, there are two possible conditions that determine the static conduction state, as shown in Figure 7.8. The transitions between these conduction states are pictorially presented in Figure 7.9, which shows **when** the transitions happen.

Table 7.1: All possible static switch states

i_{Load}	V_{Link}	PWM	Switch ON
+	+	High	Q_1, Q_4
+	+	Low	Q_2, Q_3
+	-	High	Q_2, Q_3
+	-	Low	Q_1, Q_4
-	+	High	Q_1, Q_4
-	+	Low	Q_2, Q_3
-	-	High	Q_2, Q_3
-	-	Low	Q_1, Q_4

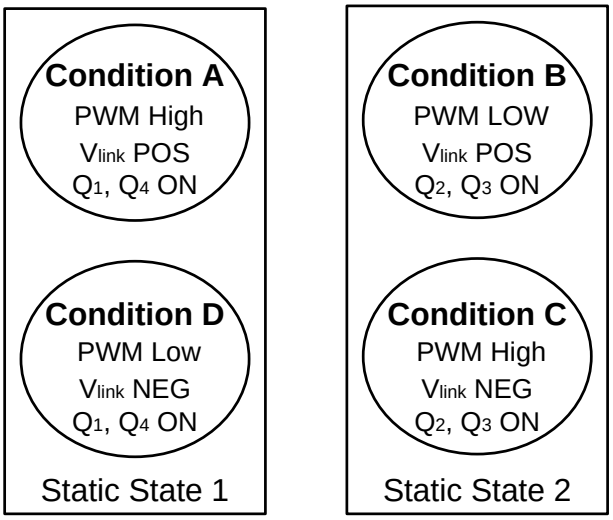

Figure 7.8: Possible conduction conditions

Figure 7.9 shows that the link voltage will change its polarity while the PWM signal remains the same (constant); however, this transition condition is eliminated if the following two assumptions are guaranteed:

1- The switching of the secondary stage is multiple integer of the switching frequency of the input stage,

2- Both switching frequencies are synchronized.

As a result, the 12 possible transitions will be reduced to 8 possible transitions. Similar 12 states are expected if the polarity of the load current is considered. The polarity of the load current does not have an impact on the static states. However, it affects the conduction states during the commutation process. It determines which diode to turn ON during the 4-step commutation process, which is presented later in this section.

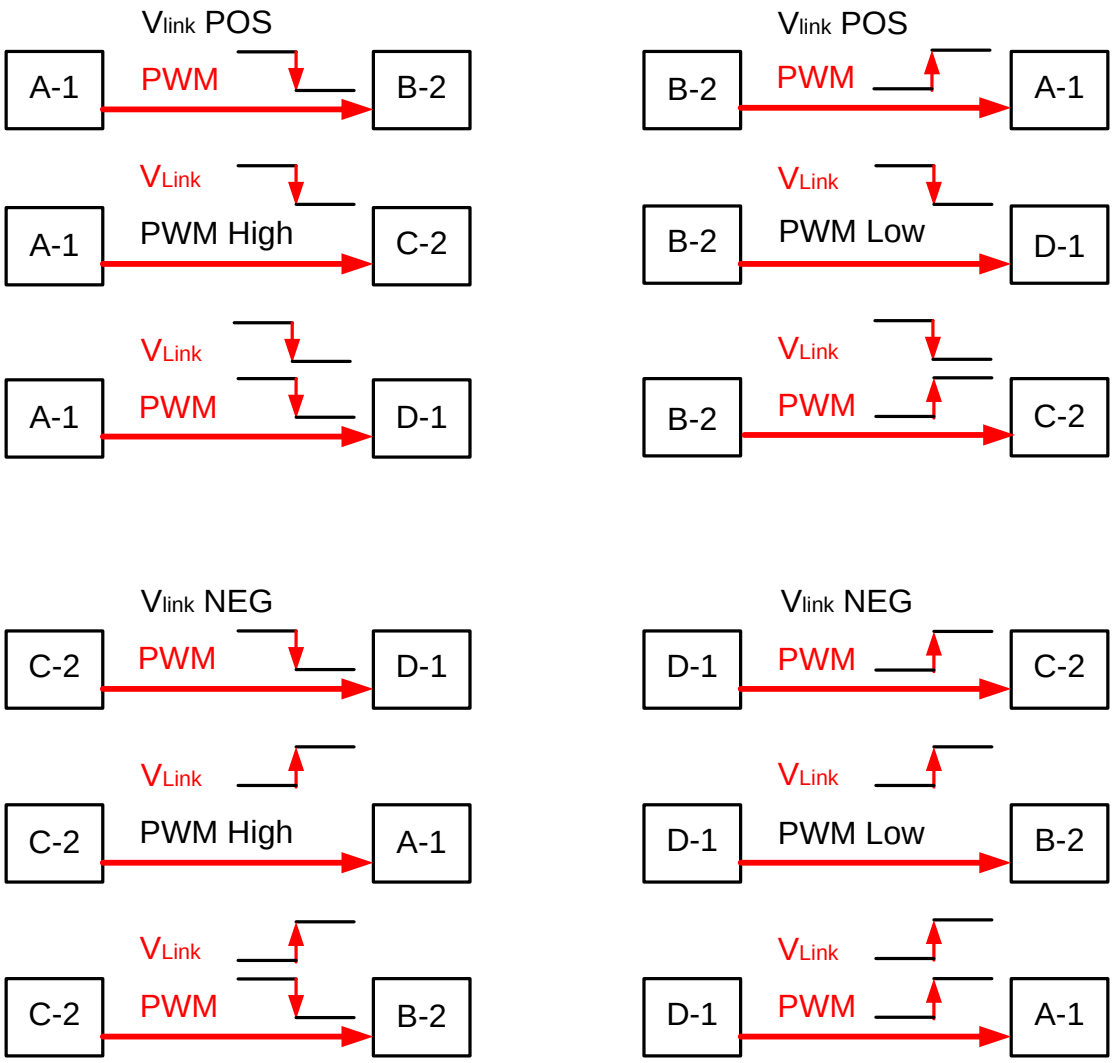

Figure 7.9: The transitions between the conduction states

7.2.1 Multi-step commutation

In the conventional H-Bridge, the body diodes provide a conduction path for current ro flow when the MOSFET is turning off. However, for the bidirectional H-Bridge, two MOSFETs are connected in series (common-source) in order to provide the bidirectional

current flow and voltage blocking capability. However, when the switches Q_1 and Q_4 in Figure 7.5 are turned OFF, there will be no path for the current to flow, since the body diodes of Q_2 and Q_3 will block it. Hence, this will result in a huge voltage spike across the MOSFETs, which can damage them if not snubbed or clamped. So, a path for this current must be provided during the switches commutation. Conventionally, dissipative snubber circuits are used across each switch. In addition of extra cost of this solution, it also increases the power losses, and, as a result, decreases the overall converter efficiency. Alternatively, the four-step switching control technique [127-129] is a make-before-break switching strategy that establishes an incoming path for the output current before breaking the outgoing path. No extra components are needed by the four-step switching technique. And soft-switching may be possible under the right conditions, as it will be shown later in this section. Hence, lower power loss and higher efficiency. Thus, it will be employed to control the commutation of the secondary stage of the AC-link MII proposed in this section.

Figure 7.10 is a moore state machine representation that shows all the possible transitions and the commutation processes. The turned ON switches, due to the corresponding action, are indicated in black color, while the conducting switches are indicated in light gray. It shows that the 8 possible state transitions, shown in Figure 7.9, are reduced to only 4 state transitions. For the remaining 4 state transitions, the PWM signal acts as triggering signal that starts the current commutation process as shown in Figure 7.10. The detailed circuit schematics for these 4 state transitions are shown in Figure 7.11 and 7.12.

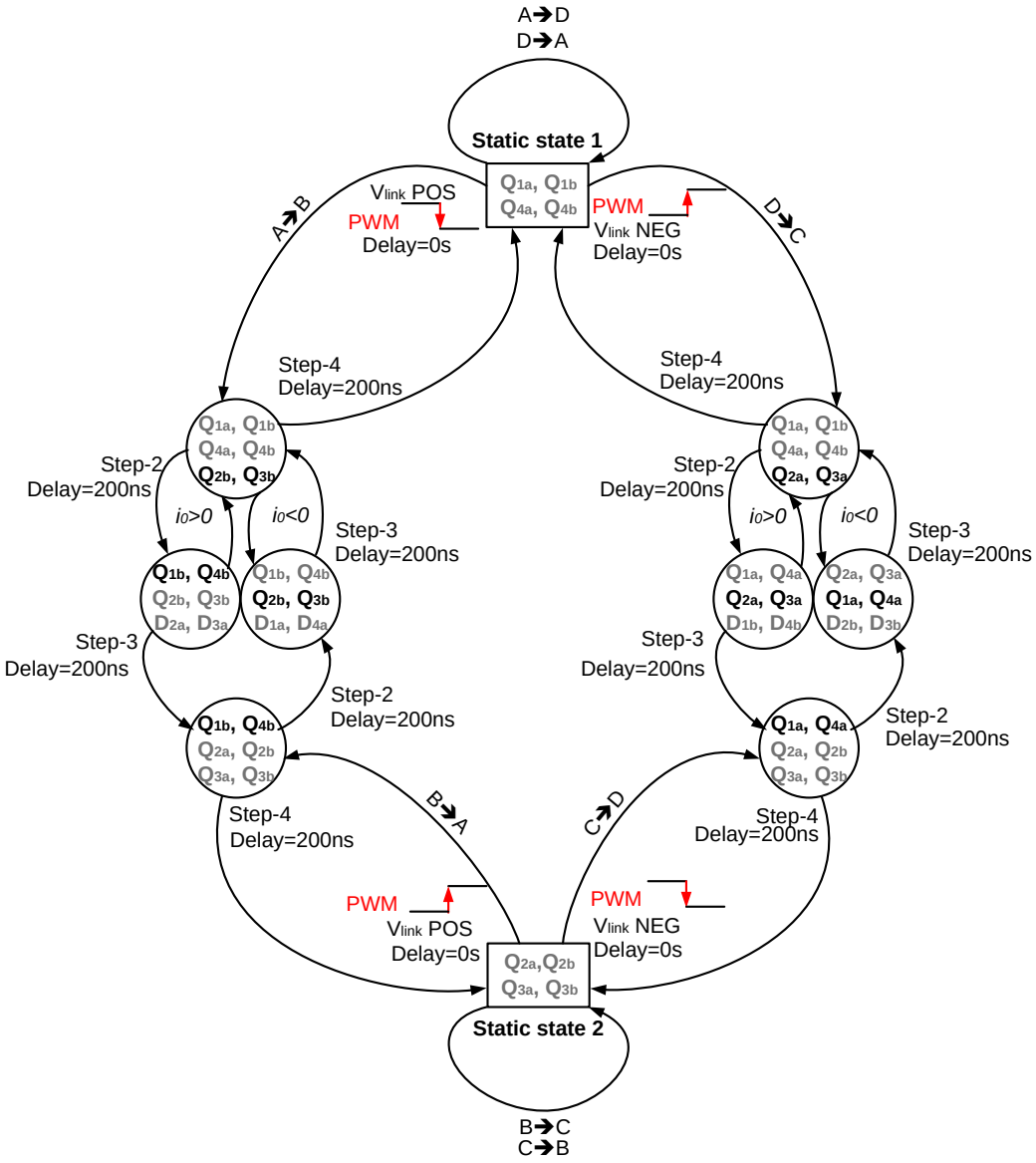

Figure 7.10: All possible transitions and the commutation process

Figure 7.11 shows the current commutation when switching from Q_1, Q_4 to Q_2, Q_3, in the case of positive link voltage. The four-step commutation process starts by turning ON Q_{2b} and Q_{3b} in step-1, and then, Q_{1a} and Q_{4a} are turned OFF in step-2. If the output current

($i_0(t)$) is positive, it will be transferred to Q_2, Q_3 during step-2, and thus, Q_{2a} and Q_{3a} are turned ON at ZVS in step-3. But, if $i_0(t)$ is negative, it will keep flowing through the body diode of Q_{1a} and Q_{4a} and the N-channel of Q_{1b} and Q_{4b} during step-2. In step-3, $i_0(t)$ will be transferred to Q_2, Q_3 once Q_{2a} and Q_{3a} are turned ON. We notice that, in this case, the ZVS is lost. Finally, Q_{1b} and Q_{4b} are turned OFF at ZCS in step-4. The backward commutation is followed to switch from Q_2, Q_3 to Q_1, Q_4 starting by turning ON Q_{1b} and Q_{4b} (step-3 in Figure 7.11).

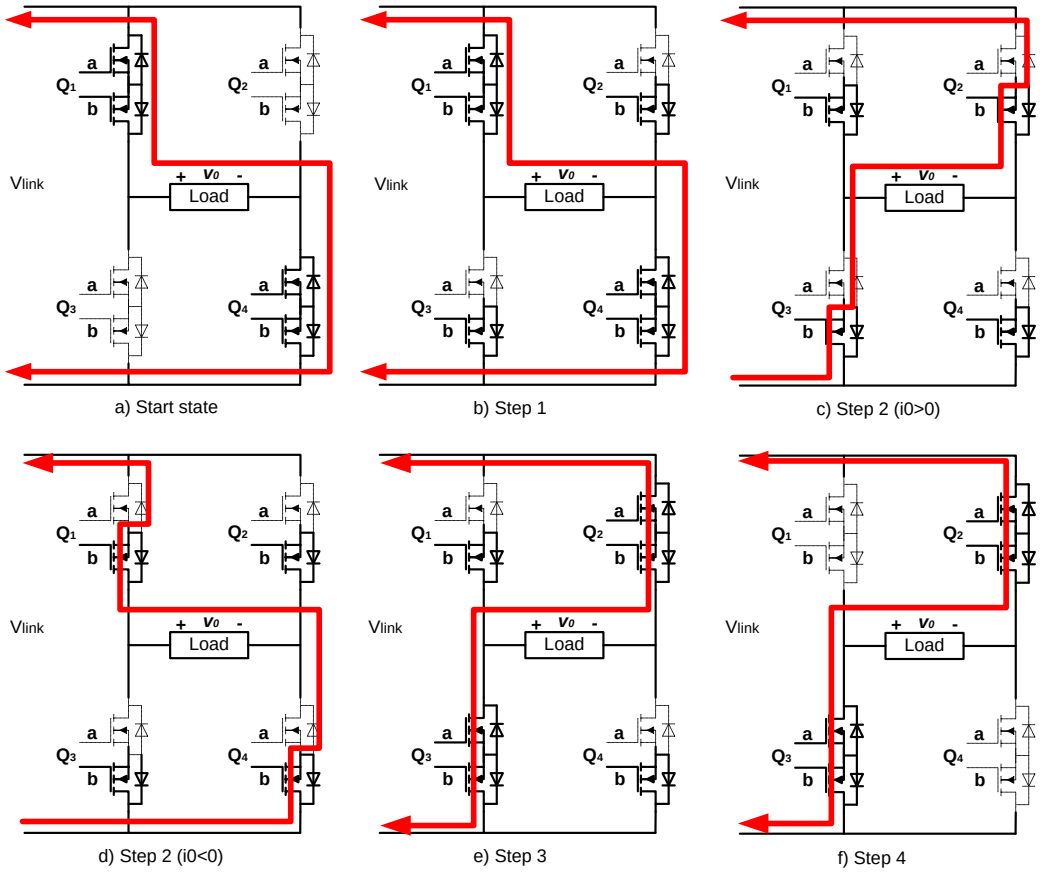

Figure 7.11: Four-step switching technique (V_{link} is positive)

Similarly, Figure 7.12 shows the switching from Q_1, Q_4 to Q_2, Q_3, but in the case of negative link voltage. The four-step commutation process starts by turning ON turning ON Q_{2a} and Q_{3a}, and then, Q_{1b} and Q_{4b} are turned OFF in step-2. If the output current ($i_0(t)$) is negative, it will be transferred to Q_2, Q_3 during step-2, and as a result, Q_{2b} and Q_{3b} are turned ON at ZVS. But, if $i_0(t)$ is positive, it will keep flowing through the N-channel of Q_{1a} and Q_{4a} and the body diode of Q_{1b} and Q_{4b} during step-2. In step-3, $i_0(t)$ will be transferred to Q_2, Q_3 once Q_{2b} and Q_{3b} are turned ON—the ZVS is lost. Finally, Q_{1a} and Q_{4a} are turned OFF at ZCS during step-4. The backward commutation is followed to switch from Q_2, Q_3 to Q_1, Q_4 starting by turning ON Q_{1a} and Q_{4a} (step-3 in Figure 7.12).

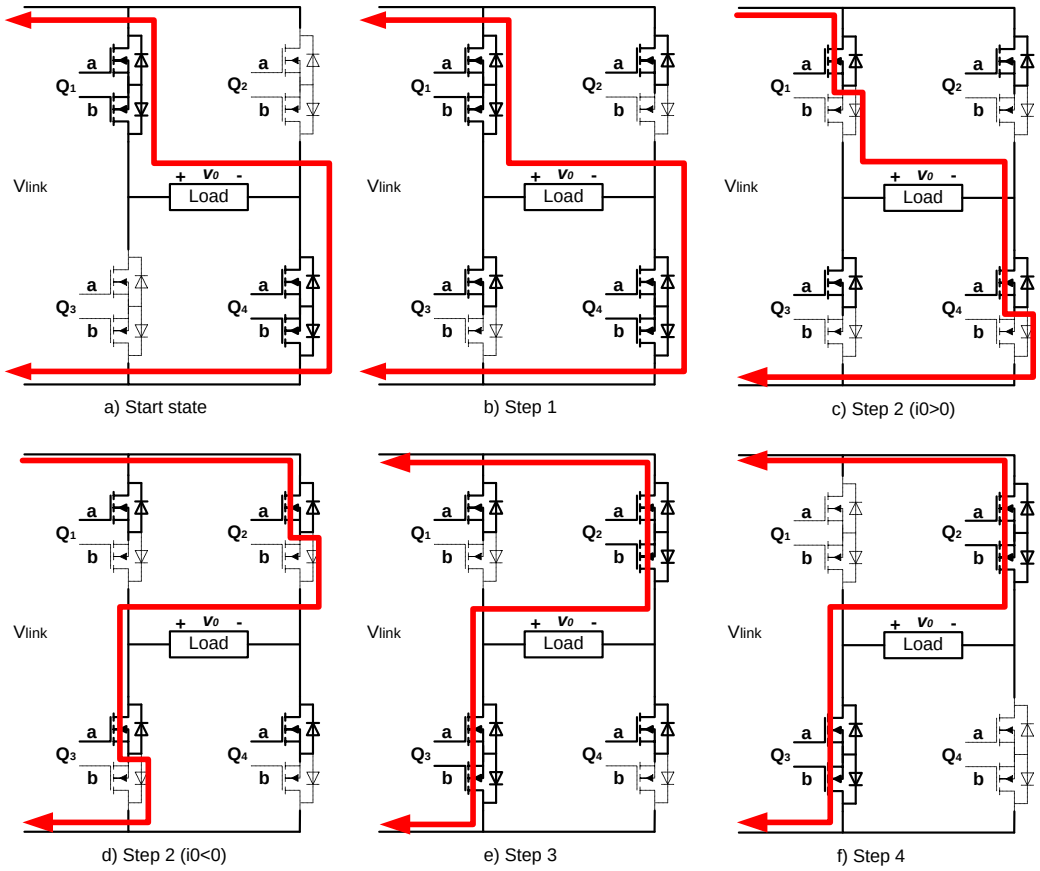

Figure 7.12: Four-step switching technique (V_{link} is negative)

7.3 Efficiency and reliability

Although the extra switches needed in the proposed topologies add power losses, holistically there are system benefits that outweigh these losses. Further, emerging, post-silicon power semiconductor technologies, such as: SiC and GaN are capable of reducing power losses by 70% to 80% [130]. Thus the issue of losses in the extra switches is minimized and must be weighed against the added advantages gained in the flexibility and capability of the circuit.

Although, a partially soft switching is provided by the aforementioned four-step switching technique, employing full soft switching techniques is another option that will further reduce the power losses associated with the MOSFET. On the other hand, the overall reliability of the MII is improved by using a highly reliable film capacitor. Moreover, it has to be stressed that the DC-link capacitor is completely eliminated. Consequently, the reliability is further improved as shown in [131].

7.4 Simulation results

PSIM was used to simulate the RP-MII. Table 7.2 shows the values of components that are used in the simulation. L_{in} and C_{in} are the input filter, which filters out the high frequency ripple.

Table 7.2: Simulation parameters

Component	Value	Component	Value
V_{in}	$30V_{dc}$	L_{in}	5mH
V_0	$120V_{rms}$	C_{in}	1000µF
f_{s1}	6KHz	L_f	10mH
f_{s2}	18KHz	C_f	10µF
N_1:N_2	1:12	L_d	200µH
R_0	60Ω	C_d	40µH

Figure 7.13 and Figure 7.14 show the gate signals of the output AC/AC converter during the four-step commutation process. Figure 7.13 shows the gate signals when V_{link} is

positive, while Figure 7.14 shows the case when V_{link} is negative.

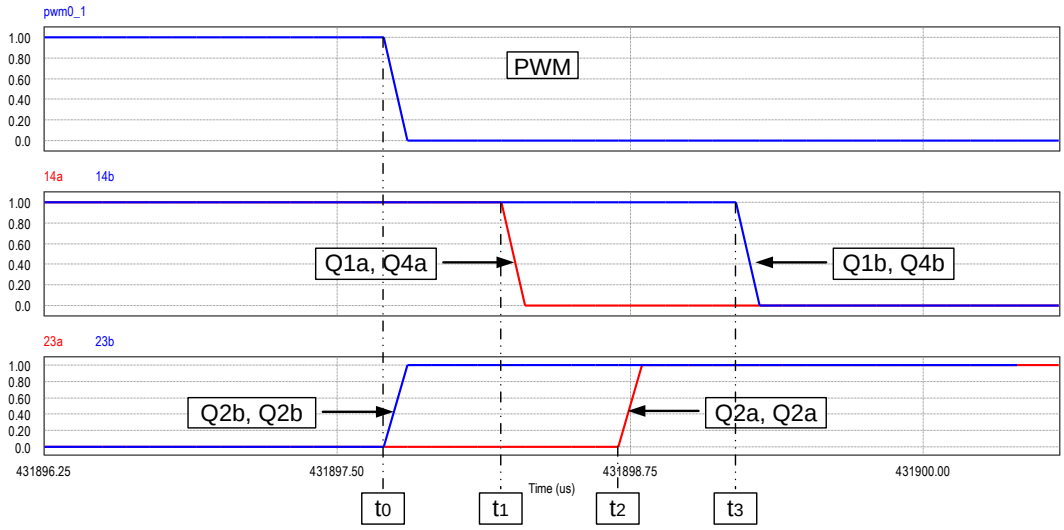

Figure 7.13: Current commutation when switching from Q_1, Q_4 to Q_2, Q_3 (V_{link} is positive)

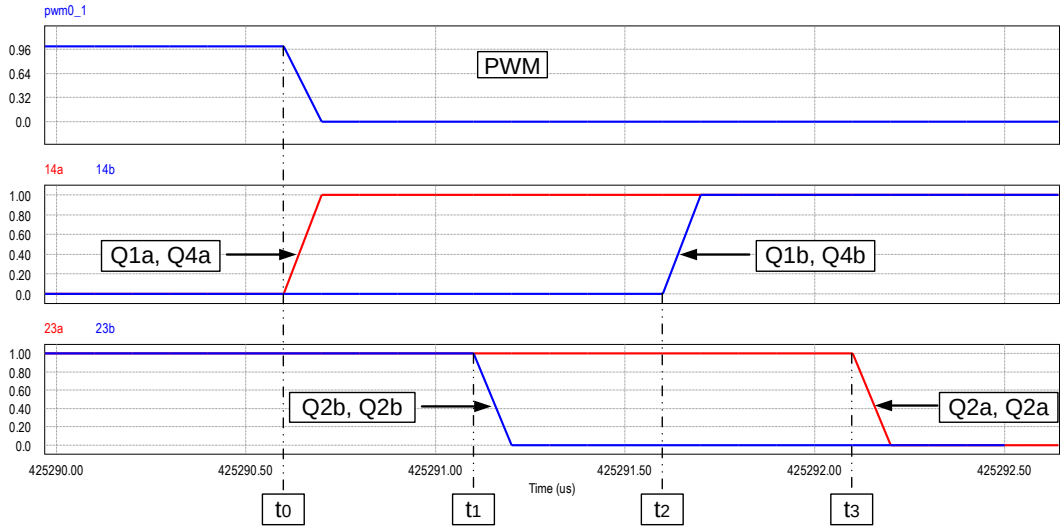

Figure 7.14: Current commutation when switching from Q_2, Q_3 to Q_1, Q_4 (V_{link} is negative)

The output (grid) voltage, v_0, and the decoupling capacitor voltage, v_{CD} are shown in Figure 7.15. The timing between the grid voltage and the decoupling capacitor, shown in Figure 7.15, is 2.27ms which corresponds to a phase difference is ϕ=49.032°. It is slightly higher than the 45° degree derived in [132] due to the presence of the phase shift of the grid-coupling LC filter and the inductor in the ripple-port. While this converter design has not been optimized for efficiency, this performance is favorable compared to other film-capacitor-based designs in the literature [39, 44]. Figure 7.16 shows the input, output, and ripple-port power waveforms. It is clear in Figure 7.16 that whenever the input power is greater than the instantaneous output power ($p_0(t)<P_{in}$), the difference will be charging the decoupling capacitor. And, the decoupling capacitor will discharge this power into the output during the opposite state ($p_0(t)>P_{in}$).

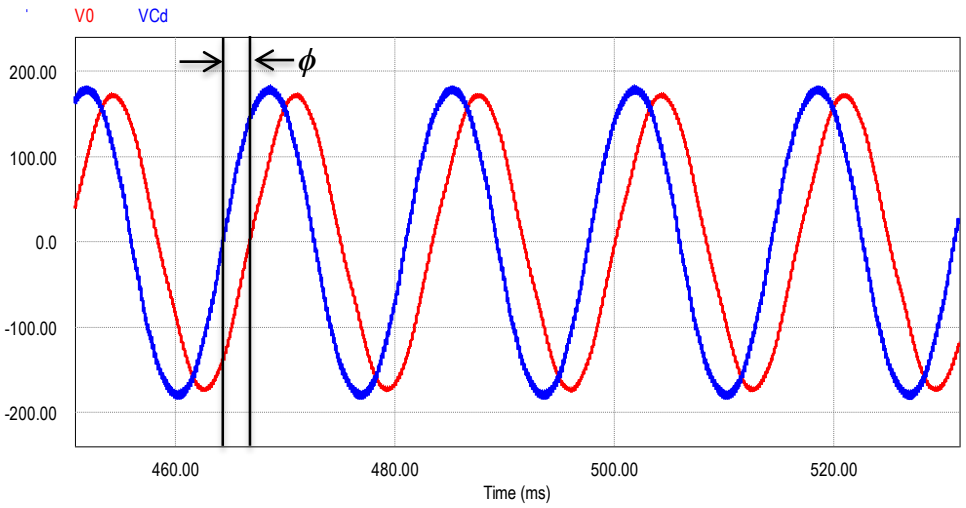

Figure 7.15: The output voltage, v_0, and the voltage across the decoupling capacitor, v_{CD}

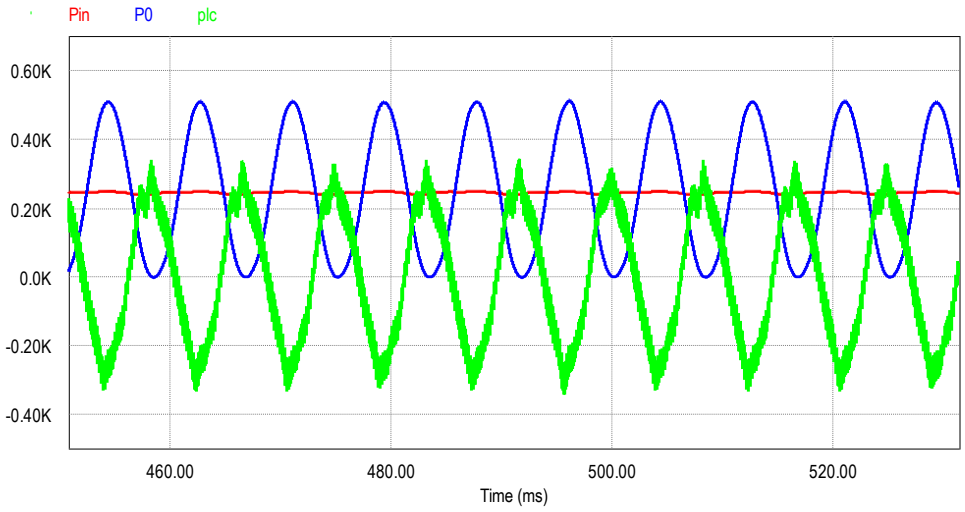

Figure 7.16: Input, output, and ripple-port power waveforms

Figure 7.17 shows the input current, i_{in}, it is clear that the input current is almost ripple-free a very small ripple ($\Delta i_{in}/i_{in}$=4%). The calculated FFT of the input current is shown is Figure 7.18. Similarly, Figure 7.19 and Figure 7.20 show the input power waveform and it calculated FFT. These figures clearly show the effectiveness of the ripple-port in filtering the input current ripple.

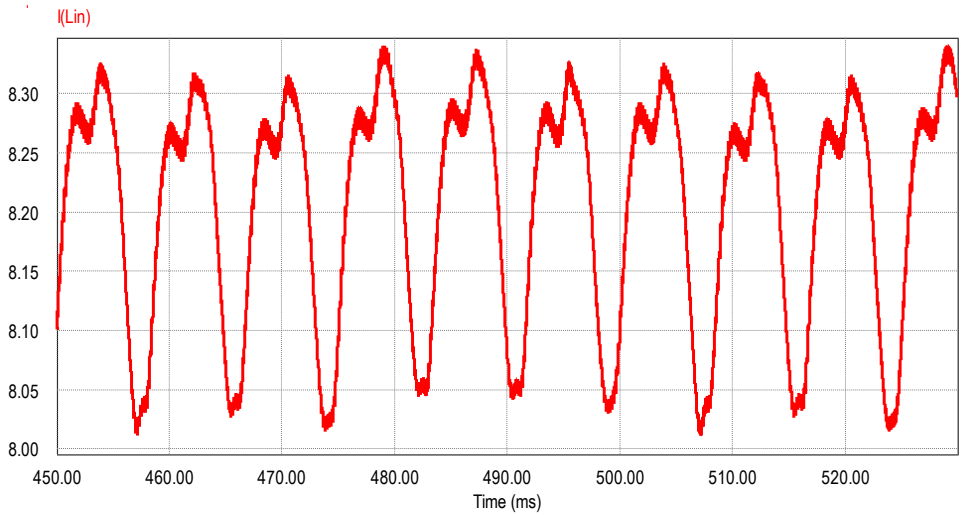

Figure 7.17: Input current waveform

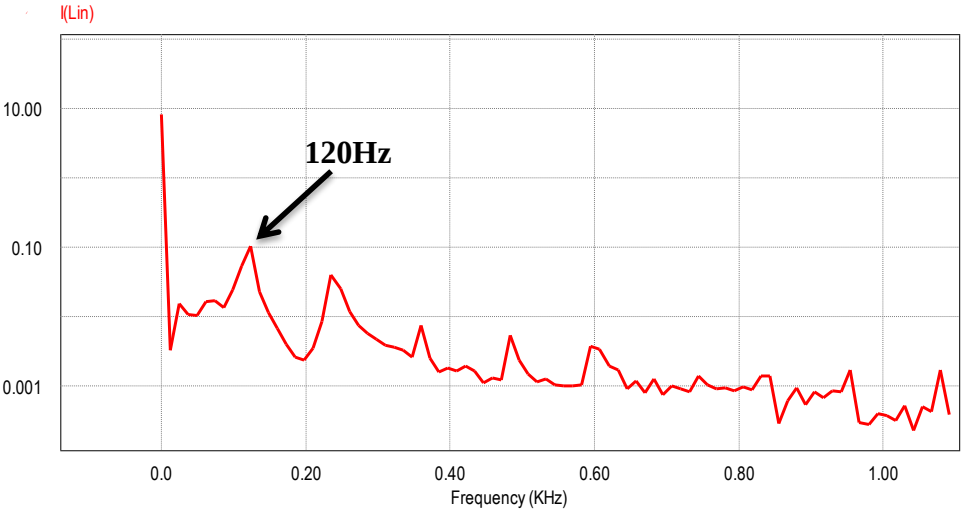

Figure 7.18: Calculated FFT of the input current

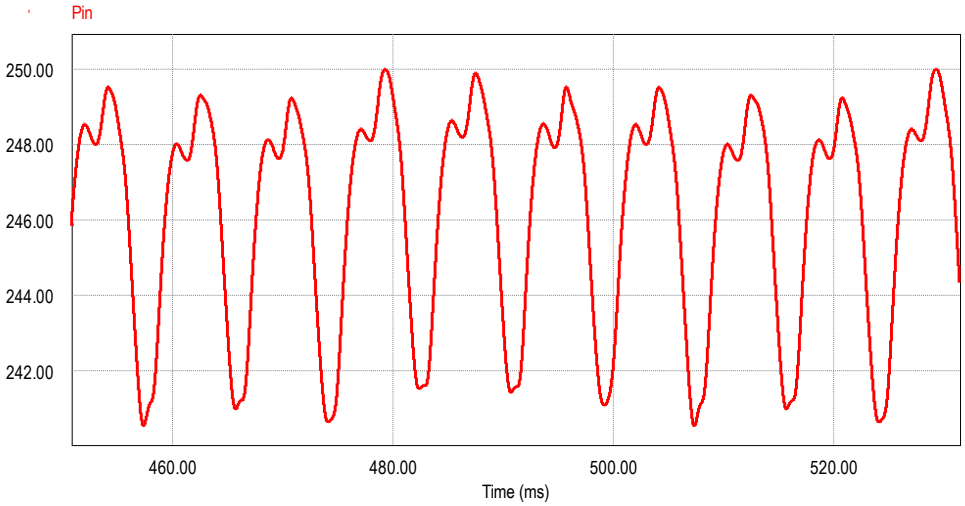

Figure 7.19: Input power waveform

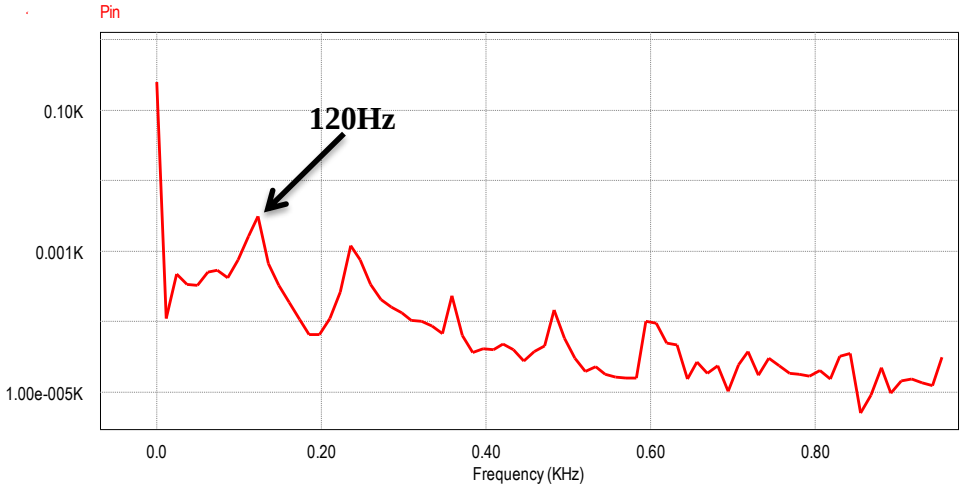

Figure 7.20: Calculated FFT of the input power

7.5 Experimental implementation and practical limitations

The proposed MII was prototyped for proof of operation concept, and the experimental setup is shown in Figure 7.21. A constant DC voltage is used to represent a PV module operating at MPPT. Figure 7.21 shows that both the AC-output and the ripple-port stages are implemented using the same board construction. This illustrates the modularity of implementing the proposed ripple-port concept.

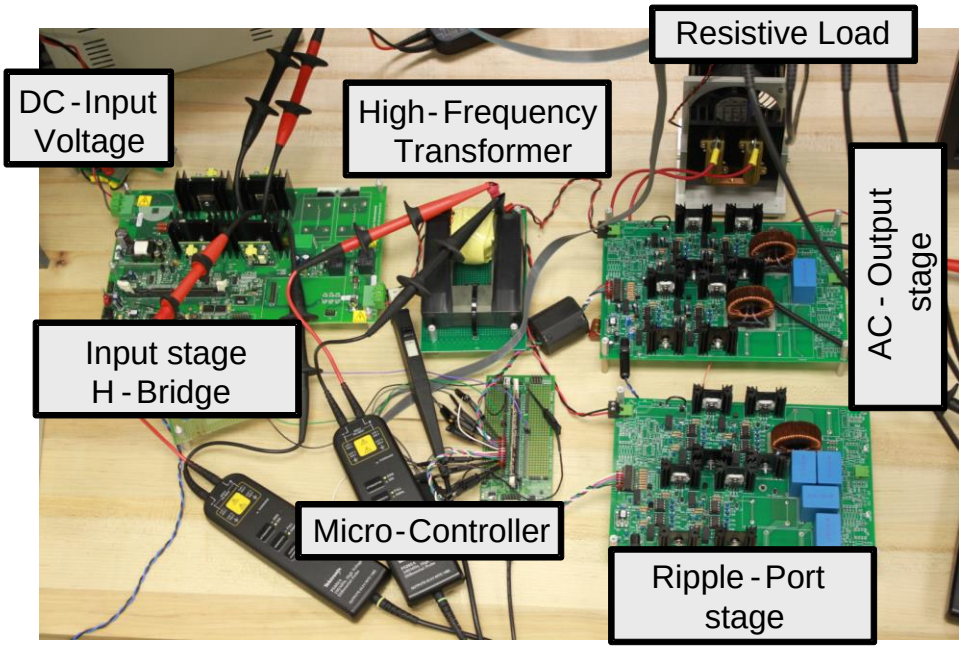

Figure 7.21: Experimental setup of the proposed topology - PV-mode operation

7.5.1 Preliminary experimental results

The proposed AC-link ripple-port MII, shown in Figure 7.21, was operated and tested at low power level (V_{in}=10V, I_{in}=3.5A, R_0=70Ω). The experimentally measured FFT for the input DC current without the ripple-port is shown in Figure 7.22 that clearly shows a high double-line frequency (120Hz) component. Then, the ripple-port was included, and the result (measured FFT) is shown in Figure 7.23. The ripple-port is capable of suppressing the 120Hz component. Figure 7.24 shows the output and the decoupling capacitor's voltage waveforms.

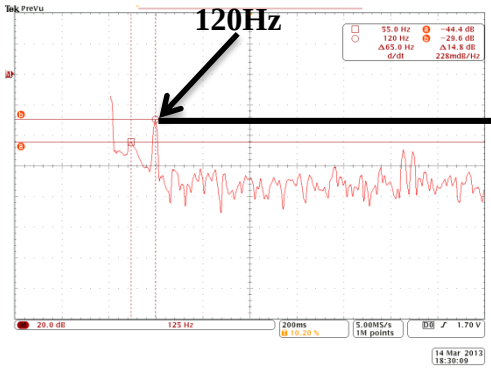

Figure 7.22: Measured FFT of the Input current without the ripple-port

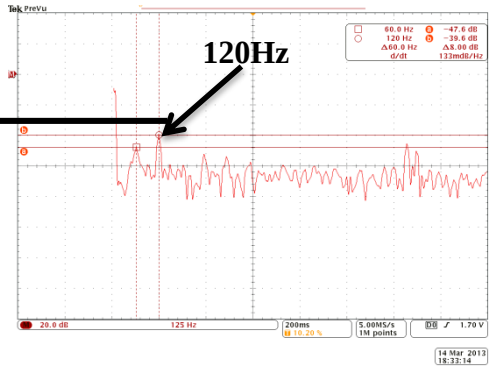

Figure 7.23: Measured FFT of the Input current with the ripple-port

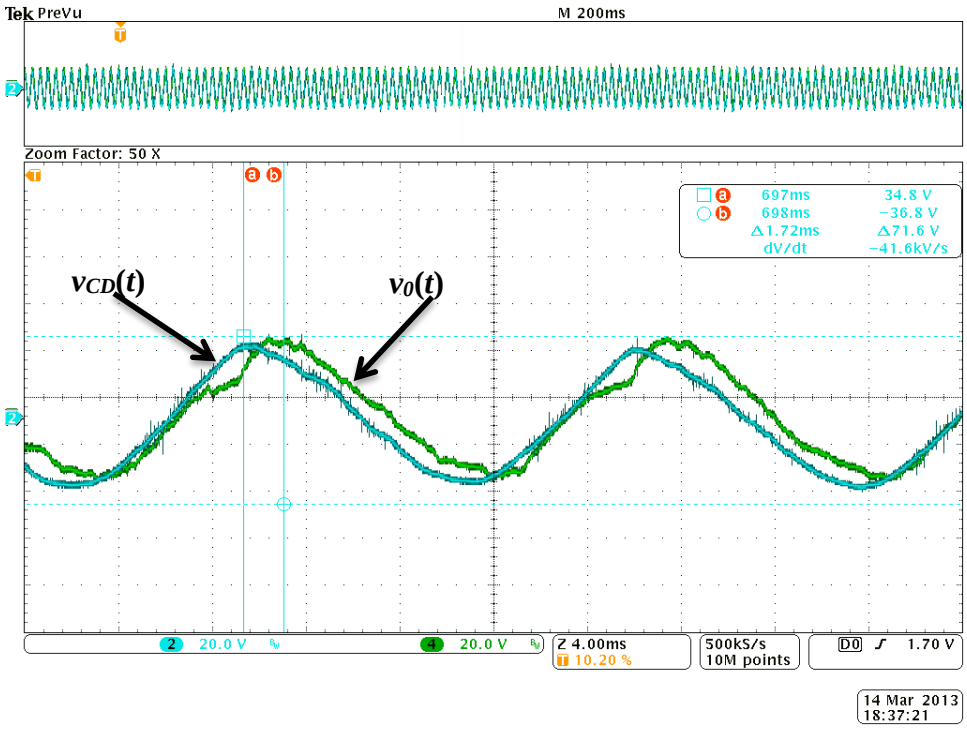

Figure 7.24: Output voltage and decoupling capacitor's voltage (V_{in}=10V, I_{in}=3.5A, R_0=70Ω)

The proposed topology was not operated at full load due to voltage spikes issue on the transformer's secondary side. The root cause of these voltage spikes is disconnecting the transformer's secondary current (inverter's input current) that flows through the transformer's leakage inductance. A passive RCD (resistor, capacitor, and diode) snubber circuit was connected on the transformer's secondary side to mitigate the voltage spikes issue. The system was able to operate and get the results shown in Figures 22, 23, and 24 with the help of the RCD snubber circuit.

7.5.2 Practical limitation

When operating the high-frequency AC/AC converter, voltage spikes across the link occurred at the link voltage polarity and AC/AC converter PWM transitions. Since the transformer has a relatively large turn ratio (1:10), which is needed for PV-MII applications, the reflected leakage inductance on the secondary side will be relatively large (100 times the primary leakage inductance) even though the transformer has a very good design with small primary leakage inductance.

7.5.2.1 **Passive snubber circuit**

A passive snubber circuit is used in order be able to operate the system. The simple capacitive snubber circuit, shown in Figure 7.25, is very common practice in the conventional DC-link inverter topology. However, for the AC/AC inverter topology, it will create another problem and will not help. Because the capacitor is connected directly across the AC-link that switches its voltage polarity, there will be a huge current spike through snubber capacitor. The RCD snubbing approach is shown in Figure 7.26. Including this snubber circuit on the transformer secondary side (AC-link) is able to reduce the voltage spikes to an acceptable level that is not the breakdown voltage of the MOSFETs neither the snubber diode. However, Snubber circuit are lossy solution and not advantageous. Figure 7.26 shows the transformer's practical model and the passive snubber circuit employed to help in suppressing the voltage spikes that occur when the transformer's secondary current is disconnected.

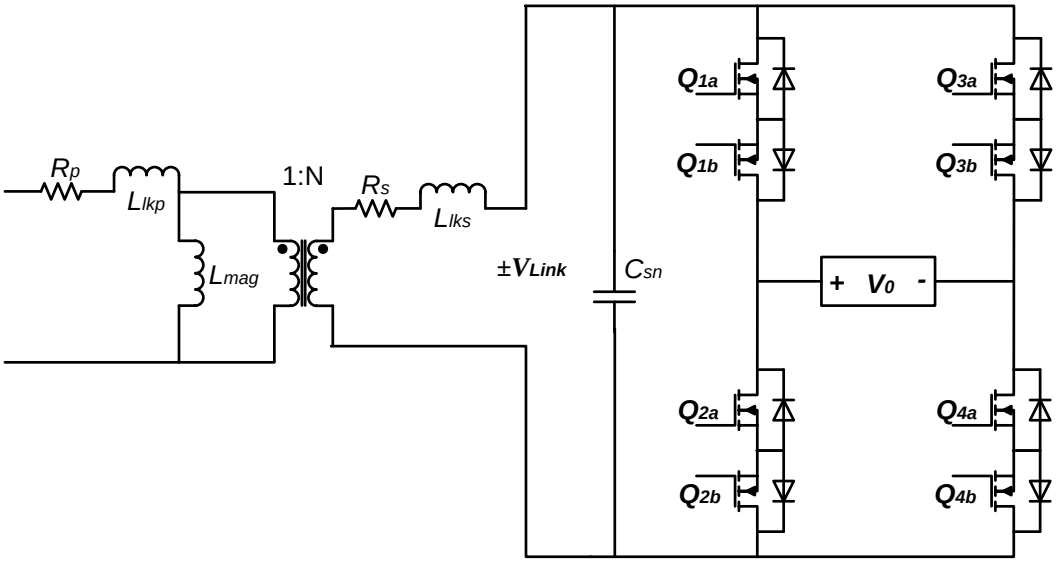

Figure 7.25: Simple capacitive snubber approach

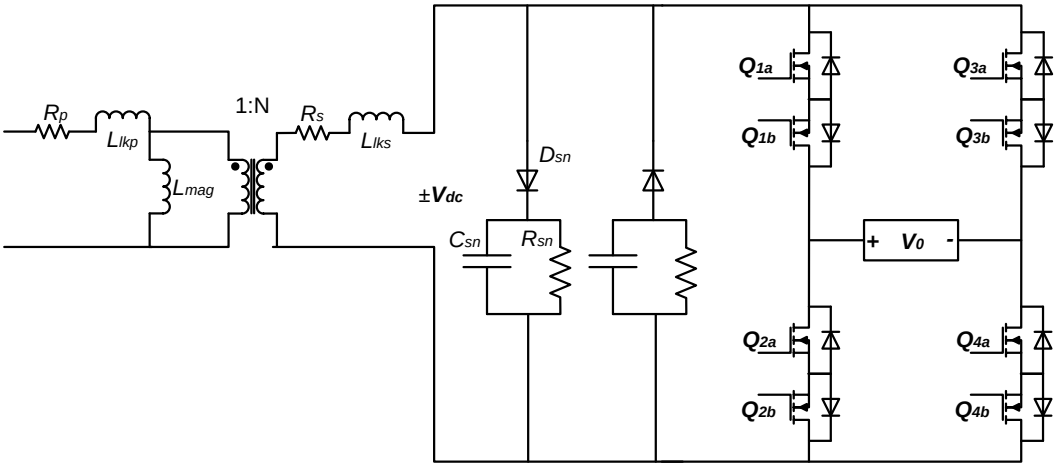

Figure 7.26: Passive snubber on the transformer's secondary side to suppress the voltage spikes

7.5.2.2 Active snubber circuit

Figure 7.27 shows an active snubber approach that is connected on the AC-link. The main idea is to provide a path for the transformer's secondary current during the secondary switches' transitions. So, similar approach can be employed in the H-Bridge AC-AC converter. However, using more switches does not sound an attractive approach since the main converter already uses extra switches (8 MOSFETs for each H-Bridge) compared to the conventional DC-link H-Bridge. Neither the passive nor the active snubber approach is a viable solution from efficiency and cost point view.

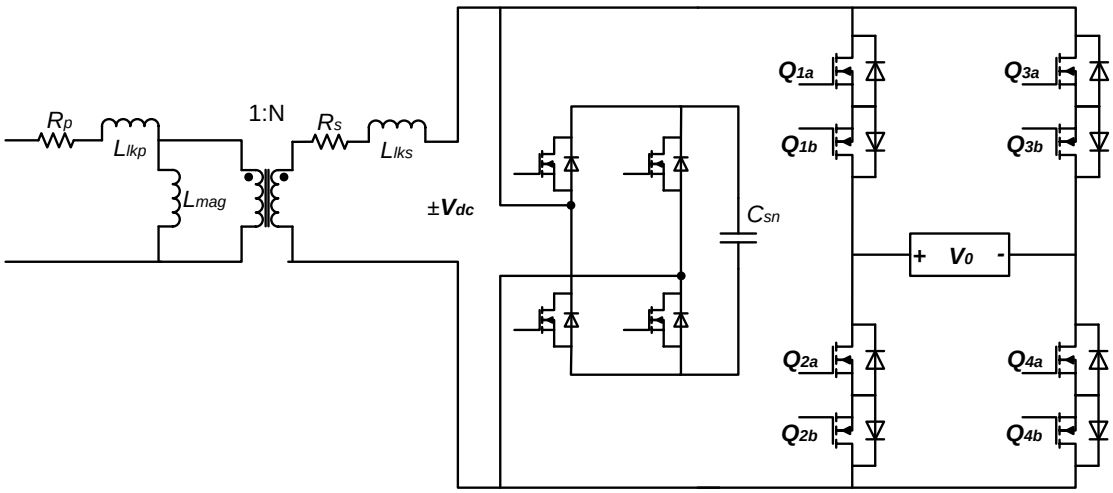

Figure 7.27: Active snubber approach for AC/AC converters

7.6 AC current source inverter

Figure 7.28 shows an AC Current Source Inverter. The existence of the transformer's leakage inductance suggests the CSI operation, which guarantees the continuity of the transformer's secondary side current. PWM control scheme is used to convert the high-frequency input current into the low (grid) frequency AC current. Given that the input current has a positive and negative polarity, an indirect PWM scheme is applied. The operation of the CSI shown below is divided into two main modes: transfer energy and short-circuit modes.

In the CSI based on the conventional PWM scheme, the switches switch at two different frequencies [133, 134].

- Q_1 and Q_3 are switching at low-frequency (output signal frequency)
- Q_2 and Q_4 are switching at high-frequency (PWM frequency)

(Note: the key point in the commutation process is to prevent short-circuiting the output capacitor (C_0))

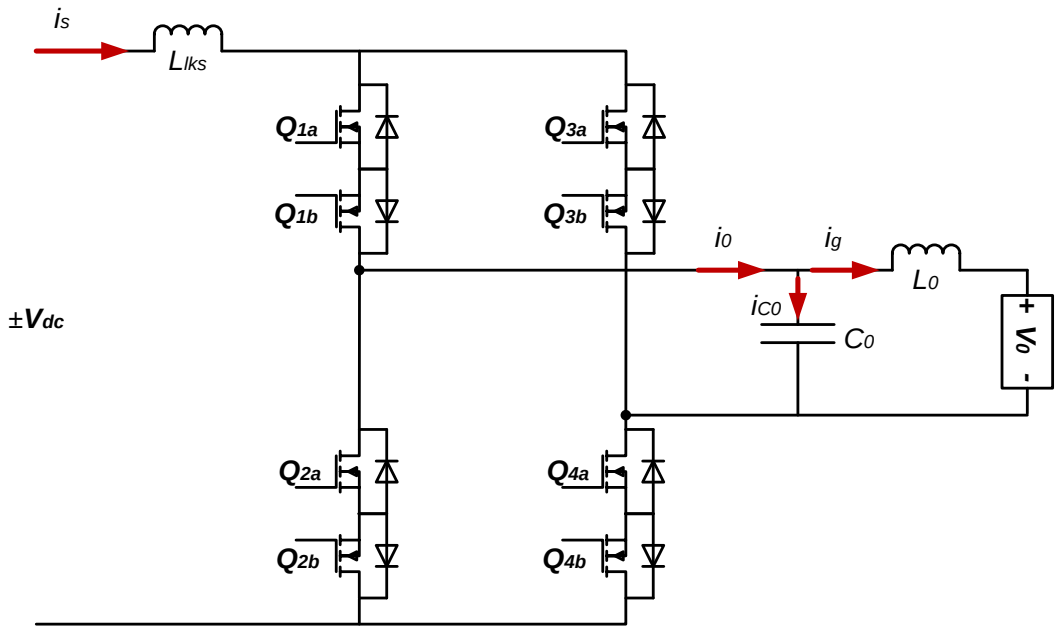

Figure 7.28: AC current source PWM inverter

7.6.1 Positive input current (I_{in}>0)

Figure 7.29 shows the conventional PWM control flowchart of the CSI when the input current is positive.

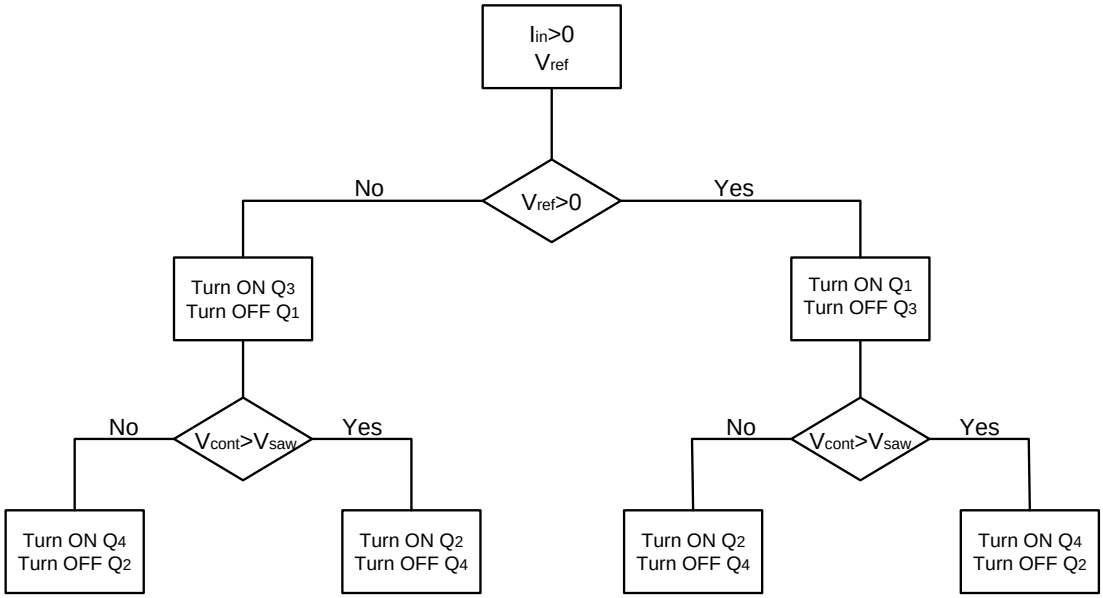

Figure 7.29: Control flowchart of a bidirectional CSI - Positive input current

It has been shown in simulation that when the input current is positive, only the diodes of the negative MOSFETs are needed for the circuit to operate. Hence, all negative MOSFETs can be either gated with a zero voltage (save the power loss due to the gate drive) or the same gate signal of the positive ones (save the power loss due to the body diode) during this mode.

7.6.1.1 Energy transfer mode

Q_1 and Q_4 are ON, the input current flows through Q_{1a}, Q_{1b} or D_{1b}, the output capacitor and the load, Q_{4a}, and Q_{4b} or D_{4b}, as shown in Figure 7.30. The energy stored in the input inductance transferred into the output as well as charging the output capacitor during this mode.

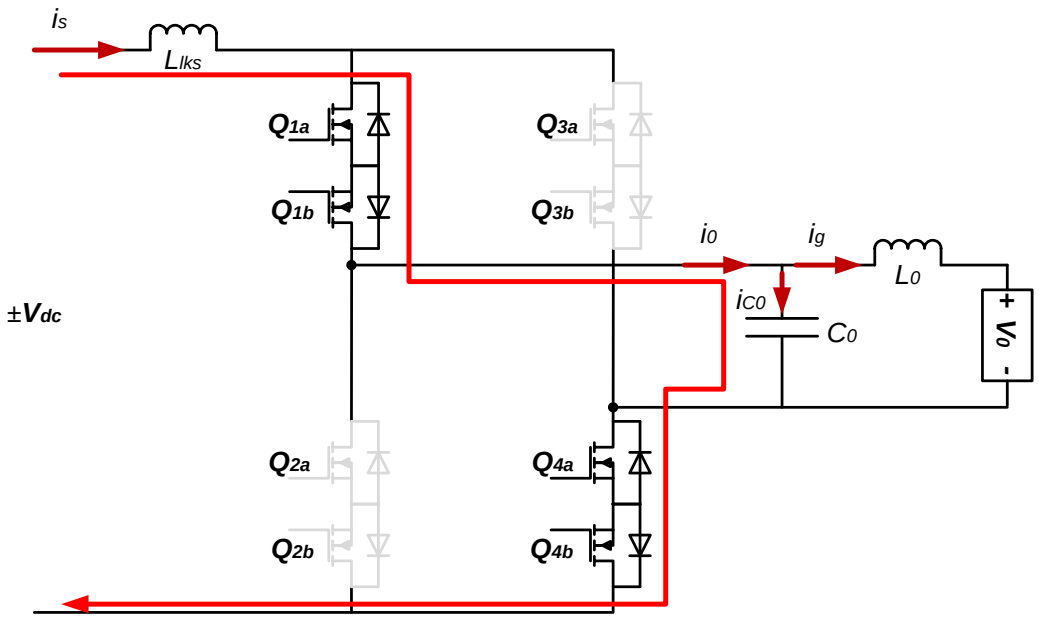

Figure 7.30: Energy transfer mode

7.6.1.2 Short-circuit mode

In this mode, a zero state is imposed across the input terminals of the CSI (Q1 and Q2 are ON), and the input current flows through Q1 and Q2, as shown in Figure 7.31.

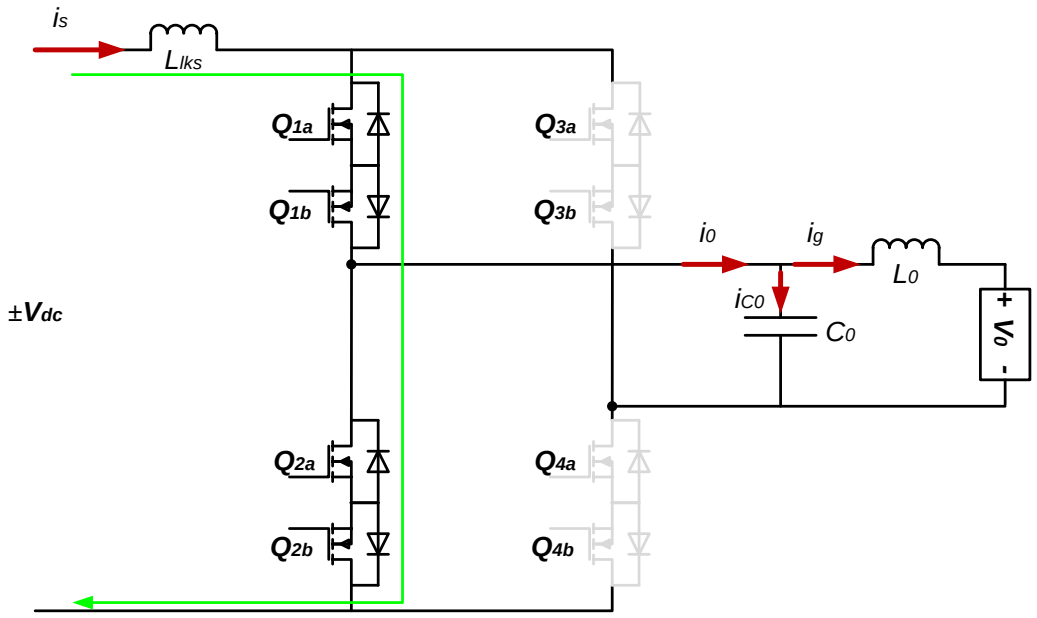

Figure 7.31: Short-circuit mode

7.6.2 Multi-step commutation

The switching between the aforementioned modes occurs at high-frequency (SPWM). to prevent short-circuiting the output capacitor , the input current needs to follow the multi-step commutation that ensure the existence of a path for the input current as well as preventing a short-circuit across the output capacitor.

7.6.2.1 Positive half-cycle - Q_1 is ON and Q_3 is OFF

Positive output (grid) voltage: the grid voltage is used as a reference (control) signal in the PWM control scheme. Q_2 and Q_4 are switched based on the PWM signal.

I. Q_4 is ON, then PWM geos low, then Q_2 needs to be turned ON and Q_4 OFF (commutating the current from Q_4 to Q_2). The system is in the transferring energy mode and will move into the short-circuit mode. Below are the four-step commutation process and Figure 7.32 shows the equivalent circuit during each step

   a) Turn ON Q_{2a} (the current remains flowing through Q_4 because the lower resistance, since Q_4n in ON. The MOSFET's channel resistance is lower than the body diode's resistance)

   b) Turn OFF Q_{4a} (the current commutates once Q_{4a} is turned OFF)

   c) Turn ON Q_{2b}

   d) Turn OFF Q_{4b}

For negative input current, the commutation process starts with the negative MOSFETs instead of the positive ones. It is completely a duality process, as explained below.

II. Q_2 is ON, and PWM geos High, then Q_4 needs to be turned ON (commutating the current from Q_2 to Q_4). The system is in the short-circuit mode and will move into the transferring energy mode

   a) Turn ON Q_{4a} (the current remains flowing through Q_2 because the lower resistance, since Q_{2b} is still ON. The MOSFET's channel resistance is lower that the body diode's resistance)

   b) Turn OFF Q_{2a} (the current commutates once Q_{4a} is turned OFF)

   c) Turn ON Q_{4b}

d) Turn OFF Q_{2b}

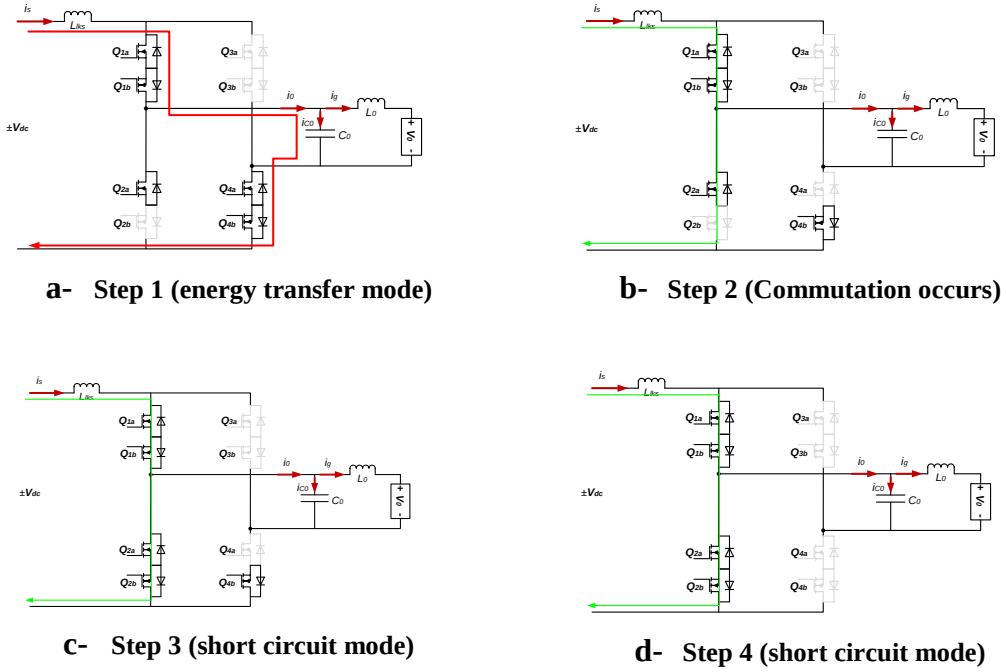

Figure 7.32: Multi-step commutation for CSI operation

For negative input current, the commutation process starts with the negative MOSFETs instead of the positive ones. It is completely a duality process.

III. Q_2 is ON, and PWM geos High, then Q_4 needs to be turned ON (commutating the current from Q_2 to Q_4). The system is in the short-circuit mode and will move into the transferring energy mode

a) Turn ON Q_{4a} (the current remains flowing through Q_2 because the lower resistance, since Q_{2b} is still ON. The MOSFET's channel resistance is lower that the body diode's resistance)

b) Turn OFF Q_{2a} (the current commutates once Q_{4a} is turned OFF)

c) Turn ON Q_{4b}

d) Turn OFF Q_{2b}

7.6.2.2 Negative half-cycle - Q_1 is OFF and Q_3 is ON

Negative output (grid) voltage. The PWM control is the opposite in this case, but the commutation process is the same.

I. Q_4 is ON, then PWM geos low, then Q_2 needs to be turned ON and Q_4 turned OFF (commutating the current from Q_4 to Q_2). The system is in the short-circuit mode and will move into the transferring energy mode

II. Q_2 is ON, then PWM geos High, then Q_4 needs to be turned ON and Q_2 turned OFF (commutating the current from Q_2 to Q_4). The system is in the transferring energy mode and will move into the short-circuit mode

7.7 Conclusion

A single-phase converter is proposed that is ideally suited for grid-connected PV (PV-Module Integrated Inverter (PV-MII)) and outdoor LED lighting applications. The proposed converter topology is based on bipolar, AC-link principle, so there are no electrolytic capacitors. The proposed converter incorporates a new ripple-port power

decoupling approach which implements the minimum energy condition, thus, allowing the minimum capacitance which can be realized using film capacitors. Hence, the reliability of the converter is increased dramatically. Also, it supports bidirectional power flow which offers flexibility to include other system requirements including storage. The proposed topology is analyzed and implemented for PV-mode of operation. Simulation and experimental results are presented to prove the operation of the proposed topology. Also, experimental limitations of the VSI implementation of the AC/AC converter were presented along with solutions—passive and active potential snubber circuits. CSI implementation was presented, which show a potential candidate for implementing the proposed AC-link PV-MII without adding extra lossy circuitry.

8 CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

Integrated power electronics are becoming the trend due to its improved efficiency and reduced cost. However, with these advantages, new challenges stem from the integration of the power electronics, such as: reliability, packaging, thermal modeling, etc. In outdoor applications, such as renewable energy applications, a harsh, wide-range operating environment will be imposed on the power electronics. Thus, the reliability of power electronics converters becomes a very crucial issue. It is required that the power electronics, used in such environments, have reliability indices, such as lifetime, which match with the source or load one. This eliminates the reoccurring cost of power electronics replacement. In this dissertation, the reliability of the integrated power electronic was thoroughly investigated, and a new methodology for evaluating the reliability of integrated power electronics was proposed and applied for different PV Module-Integrated-Inverter (MII) that employs different power decoupling techniques. The results showed that the decoupling capacitor is the limiting lifetime component in all the studied topologies. Moreover, topologies use film capacitor instead of electrolytic capacitor showed an order of magnitude improvement in the lifetime. This clearly suggests that replacing the electrolytic capacitor by a high-reliability film capacitor will enhance the reliability of the PV MII. In the second part of this dissertation, a new decoupling technique, for the single-phase DC/AC and AC/DC converters, was presented and

experimentally tested, which allows for the usage of the minimum required decoupling capacitance. In conclusion, film capacitor can be used, which led to the improvement of the overall reliability and lifetime.

In section 2, the reliability of integrated power electronics converters is scrutinized in this section. A module-integrated inverter (MII) is considered as a case study. A new methodology for calculating the MTBF of the PV-MII based on a stress-factor approach is proposed. The proposed methodology takes into account the operating environment volatility of the PV-MII. Hence, the results provide a quantified assessment of realistic MTBF under expected operating conditions. The MTBF for six different MII topologies was calculated based on the expected usage model for a PV module-integrated inverter and the MIL-HDBK-217. It was found that considering the usage model, rather than a singular worst-case operating point, yields a more optimistic MTBF. The results showed confirm the long-held belief that the double-line frequency decoupling capacitor is the dominant component, not the MOSFET, regardless of the numbers of power switches needed in the topology. Moreover, topologies that employ film capacitor for power decoupling instead of aluminum electrolytic capacitors have higher MTBF and longer lifetime. The reader is undoubtedly aware that the computation of MTBF can be easily influenced by good and bad design practices, such as component derating. Therefore, the objective of this study is not to judge the reliability merits of one topology over another. Rather, it is meant to present a method of applying a usage model of expected inverter operation as an evaluation tool when comparing different topologies on the basis of MTBF. The dataset we used in this section is, admittedly, limited, and therefore, it should

not be taken to generally represent the expected MII reliability in general. Further work in this area will apply a larger dataset of operating points to represent a higher fidelity set of operating conditions.

In section 3, two different power electronics configurations for PV system, string inverter and microinverter, are examined and compared in this paper. Reliability, availability, safety, failure, and cost of both configurations were compared. The additional energy harvest of the microinverter was found to give it an economic advantage over the expected lifetime of the PV system, particularly when the cost of replacing the string inverter is taken into account. The microinverter also offers safety advantages, which have not previously been monetized into the LCOE calculations.

In section 4, the double-line frequency ripple issue in a single-phase power DC/AC or AC/DC converter was presented and explained. An energy storage capacitor is used to decouple the difference between the DC and the AC power is needed, hence the name decoupling capacitor. Recently, many research works have been proposed to improve the microinverter's reliability by using high-reliability decoupling capacitor technology. This section reviews various power decoupling techniques that have been employed in a single-phase microinverter to reduce the size of decoupling capacitor and improve the converter's lifetime expectancy. Conventionally, for single-stage inverters, the decoupling capacitor is placed across PV module's terminals resulting in a large size capacitor. PV-side power decoupling circuits can be employed to reduce the capacitor size. However, the overall inverter's efficiency is negatively affected. Three-port converters may offer better alternatives for single-stage inverters due to their lower cost and higher efficiency. For

multistage microinverter topologies with DC link, the DC-link capacitor offers the best alternative for power decoupling. However, sophisticated control strategies should be employed to allow for higher voltage ripple and to maintain a low THD in the injected current into the grid, which will result in reducing the size of the decoupling capacitor. Finally, AC-side decoupling involves incorporating a third phase to implement the power decoupling, where a very small capacitance is required, but the control complexity is increased dramatically.

In section 5, the ripple-port concept, for double-line frequency ripple cancellation, is presented in this section. It is implemented for both single-phase DC/AC inverter and AC/DC rectifier applications. First, the proposed module-integrated inverter (MII) is based on the commonly used two-stage inverter. A third port is added for ripple cancellation purposes; it simply attached to the DC-Link. This implies that the ripple-port could be added to many commercially available inverter topologies. Two configurations for implementing the proposed MII were examined by simulation, and the best was experimentally tested. Second, the ripple-port is connected to a single-phase AC/DC rectifier. Only 140μF is needed as decoupling capacitance. Simulation and experimental results were presented that proves the ripple cancellation concept without affecting the high performance of the PWM rectifier. The results show that the ripple-port is completely independent of the type of the AC/DC rectifier stage (PWM or diode bridge followed by boost PFC). For both applications, a very small capacitance is required, where a high reliability film capacitor can be used instead of the bulky, low reliability electrolytic ones. Consequently, the system's reliability and power density are improved. The ripple-port

can be completely designed and controlled independently of the main power stage design process.

In section 6, the proposed DC-link based ripple-port PV-MII topology, which is presented in section five, was compared to the conventional DC-link based inverter in this section. For a 20 years lifetime, the efficiency, size, and price of both configurations were presented. It was found that the proposed ripple-port topology is competitive with the conventional topology in terms of size and price. Although the film capacitor approach results in 26% increase in the volume, it turned out to be 30% less expensive. Given the current semiconductor devices state, there is approximately 8% power loss due to the extra four switches introduced by the proposed ripple-port (H-Bridge). However, 68% of these power losses can be eliminated by either using a new semiconductor technology (GaN, SiC) or employing ZVS technique.

In section 7, a single-phase converter is proposed that is ideally suited for grid-connected PV (PV-Module Integrated Inverter (PV-MII)) and outdoor LED lighting applications. The proposed converter topology is based on bipolar, AC-link principle, so there are no electrolytic capacitors. The proposed converter incorporates a new ripple-port power decoupling approach which implements the minimum energy condition, thus, allowing the minimum capacitance which can be realized using film capacitors. Hence, the reliability of the converter is increased dramatically. Also, it supports bidirectional power flow which offers flexibility to include other system requirements including storage. The proposed topology is analyzed and implemented for PV-mode of operation. Simulation and experimental results are presented to prove the operation of the proposed topology.

8.2 Different power level operation

The PV-MII is expected to operate at different insolation level, which translates into different power ratings. However, the decoupling capacitor, in section 5.1, was designed for the rated power at full sun following the constraints in (5.9) and (5.10). This means that the DoM_{RP} needs to be modified according to the operation power level in order to follow the constraint in (5.9) and cancel the double-line frequency ripple. This can be accomplished automatically using a closed-loop controller, as it will be explained later in this section.

8.2.1 Step load simulation results

The system, in section 5.1, is simulated again in this section with half operating power rating (P_{pv}=120W). The DoM_{RP}=0.69 was calculated using (5.9), and used in the simulation. The results show that the ripple-port is capable in cancelling the double-line frequency ripple. Figure 8.1 shows the input power (P_{PV}), output power ($p_0(t)$), and decoupling capacitor's power ($p_{CD}(t)$) waveforms. The output voltage ($v_0(t)$), the decoupling capacitor's voltage ($v_{CD}(t)$), and the DC-link voltage (V_{DC}) waveforms are shown in Figure 8.1. The peak value of the $v_{CD}(t)$ indicates the modified *DoMRP*. Figure 8.2 shows zoom-in for the input power (P_{PV}) and the input current (i_{Lin}) with less than 7% double-line frequency ripple on both of them.

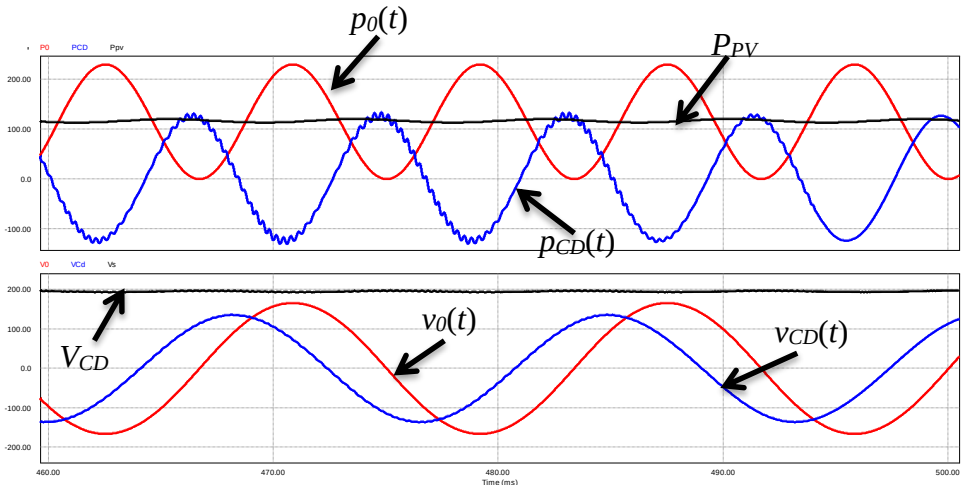

Figure 8.1: Simulation results at half power rating - P_{pv}, $p_0(t)$, and $p_{CD}(t)$ (top) and V_{dc}, $v_0(t)$, and $v_{CD}(t)$ (bottom)

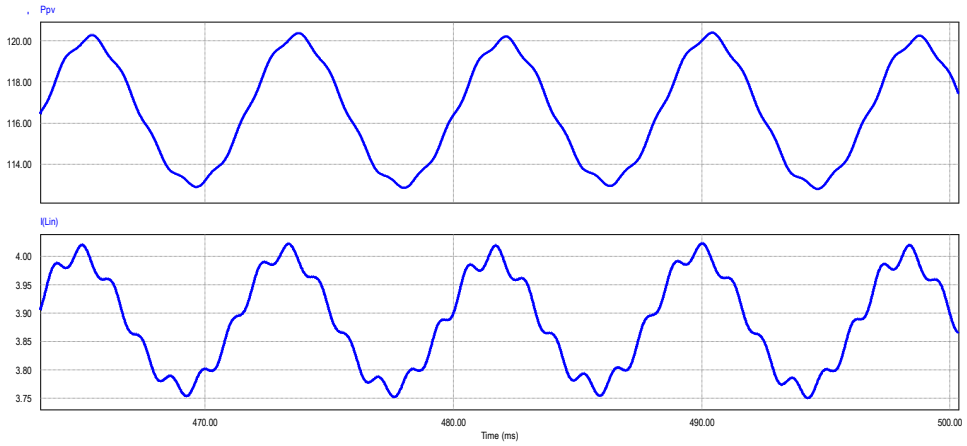

Figure 8.2: Simulation results – Zoom-in P_{pv} (top) and $i_{Lin}(t)$ (bottom) waveforms

8.3 Control design for the ripple-port

It was shown that as the operating power changes with different insolation levels, the DoM_{RP} needs to be modified accordingly to keep cancel the double-line frequency ripple

on the DC side. Figure 8.3 shows the block diagram of the proposed closed-loop control system. The operating input power (P_{PV}) can be calculated using the input voltage and current measurements that are already needed for the MPPT control block.

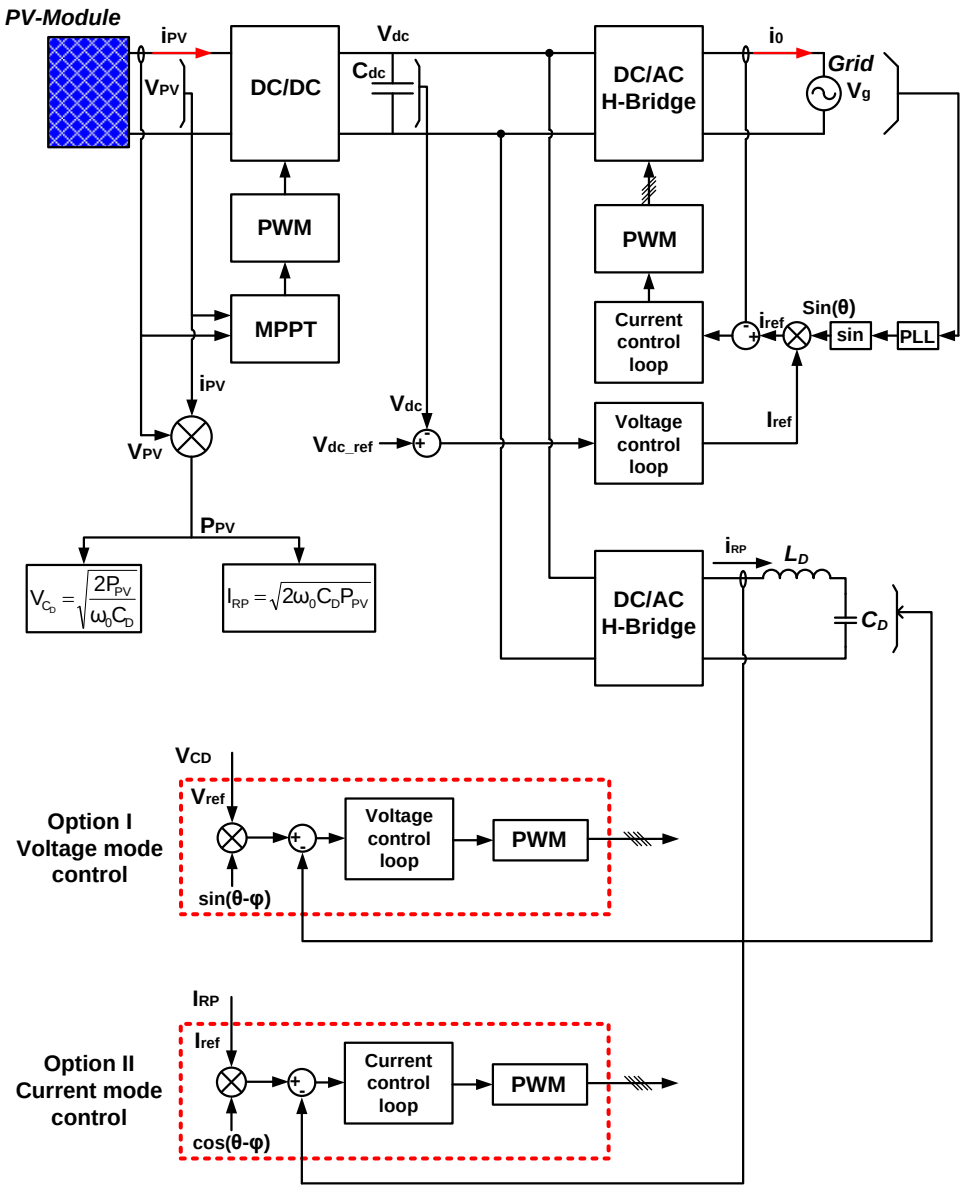

Figure 8.3: PV-MII system's block diagram with closed-loop control

Once P_{PV} is calculated, the designer has two options for controlling the ripple-port, namely voltage mode and current mode control, as shown in Figure 8.3. Advantages and disadvantages of each approach, the practical implementation, and the impact on the main power stage need further investigation.

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