HIGH-PERFORMANCE ORGANIC THIN-FILM TRANSISTOR

A Dissertation

by

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ABSTRACT

Organic compounds have been regarded as insulators for a long time. However, a semi-conductive organic material was discovered in the late 1940s. Since then, many organic semiconductors have been found and studied. However, the current carriers have quite lower mobility than those of inorganic counterparts so far. In spite of the low mobility, organic semiconductor devices have many interesting advantages such as low-cost fabrication, easy process, diverse substrate materials, and so on. Owing to the benefit of the low-cost fabrication, organic semiconductor can be applied to large-area electronic devices as well as ubiquitous devices. Although organic semiconductor has been widely utilized in electronics, its low performance has extremely restricted application in integrated circuits (ICs) that are essential for high-tech electronics. In order to be competitive in market, the performance improvement of organic thin film transistors (OTFTs) has become an indispensable prerequisite. Although the low performance of conventional OTFTs basically results from the inherent low carrier mobility, it is also attributed to low resolution fabrication processes and their inferior configuration with large parasitic capacitance.

With regard to solutions to improve the performance of OTFTs, three novel strategies are proposed in this work: submicron metal patterning, self-aligned structure, and metal semiconductor field-effect transistor (MESFET)-like structure. To realize the solutions, a new concept of lithography, dual-layer thermal nanoimprint, is devised and its potential for submicron organic semiconductor patterning is experimented. In

addition to the submicron resolution, two innovative patterning techniques, single-layer patterning and double-layer patterning, are successfully developed through the dual-layer thermal nanoimprint. Both patterning techniques can be utilized in fabricating self-aligned OTFTs and organic metal semiconductor field-effect transistors (OMESFETs). In the case of OMESFETs that require multiple-level metallization, the application of the dual-layer thermal nanoimprint lithography is extended from two-dimension to three-dimension to achieve self-aligned metallization that completely eliminates alignment errors. The 3D dual-layer thermal nanoimprint enables a sub-100 nm gap between metal patterns on an organic active layer. Because of the capability of nanoscale metal patterning on organic semiconductors with high overlay accuracy, this self-aligned metallization technique can be effectively utilized to fabricate high-performance top-contact OMESFETs.

DEDICATION

This dissertation is dedicated to my beloved wife, Yoojea, and my adorable sons,

Soomin and Woojin, for their endless encouragement, unconditional trust, and true love.

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NOMENCLATURE

Al	Aluminum
Au	Gold
BOE	Buffered Oxide Etch
BST	Barium Strontium Titanate
BZT	Barium Zirconate Titanate
CHF_3	Trifluoromethane
Cr	Chromium
E-beam	Electron-beam
FDTS	1H,1H,2H,2H-perfluorodecyltrichlorosilane
FET	Field-Effect Transistor
TES-ADT	5,11-bis(triethylsilylethynyl) anthradithiophene
FTS	(tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane
HMDS	Hexamethyldisilazane
HOMO	Highest Occupied Molecular Orbital
IC	Integrated Circuit
IP	Ionization Potential
LUMO	Lowest Unoccupied Molecular Orbital
MESFET	Metal Semiconductor Field-Effect Transistor
MTR	Multiple Trapping and Release
NIL	Nanoimprint Lithography

OMESFET	Organic Metal Semiconductor Field-Effect Transistor
OTFT	Organic Thin-Film Transistor
OTS	Octodecyltrichlorosilane
P3HT	Poly (3-hexylthiophene-2,5-diyl)
PECVD	Plasma-Enhanced Chemical Vapor Deposition
PGMEA	Propylene glycol methyl ether acetate
PMMA	Poly (methyl methacrylate)
PVA	Polyvinyl acetate
RFID	Radio Frequency Identification
RIE	Reactive Ion Etching
SAM	Self-Aligned Monolayer
SEM	Scanning Electron Microscope
Si_3N_4	Silicon nitride
SiO_2	Silicon dioxide
Tg	Glass Transition Temperature
TIPS-PEN	6,13-bis(triisopropylsilylethynyl) pentacene
UV	Ultra Violet

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CHAPTER I

INTRODUCTION AND PRINCIPLE OF ORGANIC THIN-FILM TRANSISTOR

Since the first OTFT was developed in 1986 [1], OTFTs have continuously been the keen interest of numerous researchers. The unceasing concerns are mostly attributed to their charming potentiality of very low-cost manufacturing that can be achieved from simple device structures and easy processing steps [2]. Owing to the high cost-effectiveness, OTFTs are preferred for large-area and low-cost applications such as active-matrix driving circuits for display, smart cards, low-cost radio frequency identification (RFID) tags, simple ICs, and memory devices. Furthermore, OTFTs can be fabricated at low-temperatures, even at room temperature, so that there are broad options for substrate materials; plastic or paper can be also used for the substrate. Consequently, flexible or transparent electronics are realized in such applications of display and electronic paper. The novel properties of flexibility and transparency enable the forming of a new paradigm of future electronics.

In spite of such unique advantages, OTFTs still have a long way to overtake their inorganic counterparts in a real commercial market. Although OTFTs have been gradually deployed for low-performance electronics on a commercial scale, their performance is extremely too low to satisfy market expectations that have become used to inorganic high-tech electronics. In order to extend the area of their commercial applications, it is indispensable to improve their poor performance. While there have been enormous efforts to improve the inferior electrical characteristics of materials,

studies on device structural and dimension-wise improvement have been in a stalemate for a long time because there has been no available lithography technique for the improvement. Therefore, it is difficult to expect a dramatic performance improvement of OTFTs without innovation of lithography techniques.

As the need of an innovative lithography technique comes to the forefront in realizing high-performance OTFTs, we have tried to assess the possibility of performance improvement from the nanoimprint lithography that is regarded as one of the next generation lithography techniques for sub-10 nm patterning. In order to make a breakthrough, however, the existing nanoimprint flow essentially needs to make up for its condition requiring a dry-etching that may seriously degrade the electrical characteristics of an organic semiconductor active layer. As a way to avoid the dry-etching, a new concept of nanoimprint, called dual-layer thermal nanoimprint, is devised. In addition, the concept is expanded from two-dimension to three-dimension to efficiently realize the structural improvement of OTFTs. For the first step towards high-performance OTFTs, appropriate solutions based on the dual-layer thermal nanoimprint are suggested after thoroughly explaining the principle of conventional OTFTs in this chapter. In the following chapters, the feasibility of the solutions is investigated through experimental results and then performance improvement is reported.

1.1 Overview of OTFTs

The three basic elements of OTFTs are a gate insulator, a thin organic active layer, and three electrodes – source, drain, and gate. According to their arrangement, conventional OTFTs are commonly classified into top-gate and bottom-gate types: the bottom-gate type of OTFTs is sorted into top-contact and bottom-contact types in more detail [3]. As shown in figure 1, the gate is separated from the organic active layer by the gate insulator whereas the other two electrodes, the drain and the source, are in contact with the organic semiconductor film. In the bottom-gate type, a heavily doped semiconductor substrate is often used for the gate so that a fabrication process is much simpler than that of the top-gate type because it does not need a metal patterning step for the gate.
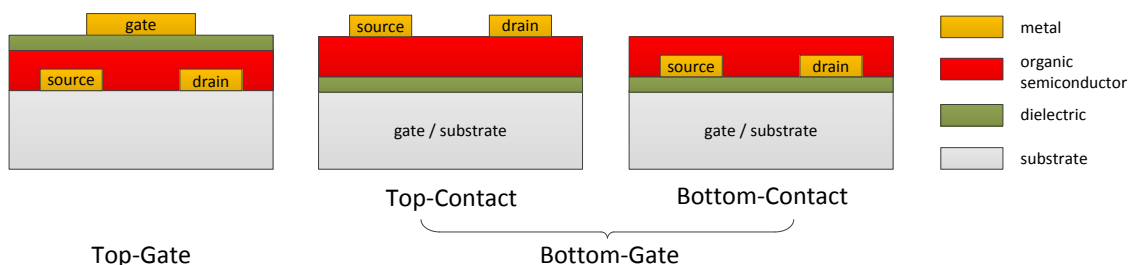
Figure 1. Schematic views of conventional OTFTs

As one of field-effect transistors, the carrier (hole or electron) distribution and mobility of OTFTs are also controlled by electric field change in an organic active layer. Because the organic active layer is morphologically in the form of a thin-film, it is difficult to gather carriers in inversion mode so that accumulation and depletion modes

are utilized to create and remove a conducting channel between source and drain, respectively [4]. In order to transport carriers from source to drain, extra carriers should be injected from source and then flow through a conducting channel. The type of carrier can be determined from the relative location between the Fermi level of a metal used for source electrode and the molecular energy level of an organic semiconductor. When the Fermi level of the metal is near to the highest occupied molecular orbital (HOMO) level of the organic semiconductor, holes are easily injected to the organic semiconductor while electron injection seems unlikely. In a case that the Fermi level of the metal is near to the lowest unoccupied molecular orbital (LUMO) level of the organic semiconductor, electrons are carriers injected from source electrode. Figure 2 illustrates the energy level of a p-type OTFT in which gold (Au) is used for electrodes and poly (3-hexylthiophene-2,5-diyl) (P3HT) is used for organic semiconductor. As seen in the energy level, the Fermi level of gold is near to the HOMO level of P3HT. Therefore, holes are injected and then transported to drain electrode when the drain electrode is negatively biased compared to the grounded source electrode.
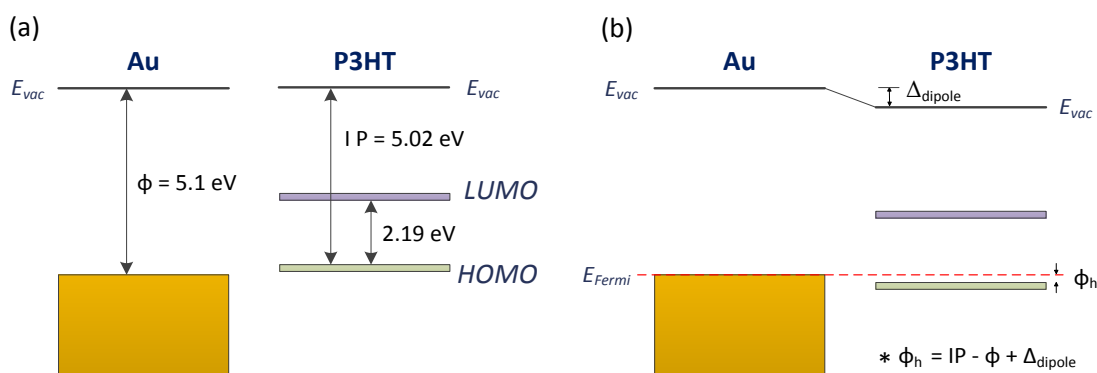
Figure 2. Schematic energy level diagram of gold and P3HT before (a) and after (b) contact. Hole-injection barrier (ϕ_h) is calculated from the ionization potential (IP) of P3HT, the work function (ϕ) of gold, and the interface dipole barrier (Δ_{dipole}).

Unlike completely delocalized charge carriers in a crystalline material, charge carriers in an amorphous organic semiconductor are highly localized due to irregular lattice and defect sites. Charge transport in delocalized states is interrupted by thermally-induced lattice deformations that lead to carrier scattering. Therefore, the carrier mobility in crystalline materials tends to drop with increasing temperature. On the other hand, the charge carriers in most organic semiconductors move faster at a higher temperature. The different tendency can be rationalized through several models of charge transport in amorphous semiconductors. As the first model, hopping mechanism was introduced in 1960 [5]. In the model, the charge is assumed to hop from an occupied state to a nearest unoccupied state with the assist of phonons. The initial model was further expanded to variable-range hopping instead of the limited hopping to the nearest unoccupied state [6]. The charge transport is also explained in the multiple trapping and release (MTR) model [7]. In the MTR model, charge carriers transit through a narrow

delocalized band while their motion is interrupted by carrier trapping into the high concentration of localized states (traps). The trapped carriers are released through thermal activation. In the MTR model, the drift mobility(μ_D) can be expressed by

$$\mu_D = \mu_0 \alpha \, \exp\left(-\frac{\Delta E_t}{kT}\right) \qquad \text{[Eq. 1]}$$

where μ_0 is the mobility in the delocalized band, α is the ratio of the density of states at the bottom of the delocalized band to the density of traps, and ΔE_t is energy difference between the edge of the delocalized band and the trap level in a single trap level.

According to the type of injected carriers, OTFTs are classified into two types, p-type and n-type. However, n-type OTFTs have been rarely utilized due to their drastic atmospheric decay and electron mobility that is substantially lower than the hole mobility of p-type OTFTs. It was found that the low electron mobility was attributed to electrons trapped by hydroxyl groups at the interface of dielectric and organic semiconductor [8]. By adopting hydroxyl-free gate dielectrics, the electron mobility of 1.46 cm^2/Vs was demonstrated from a n-type OTFT with a fullerene (C$_{60}$) channel [9]. In spite of the improved mobility, the practical application of n-type OTFTs is still far-off because of their instability in ambient air. Although there were several reports of air-stable n-type OTFTs whose semiconductor channels had high electron affinities so that the channel hardly reacts with moisture and oxygen, their mobility was too low to operate as a functional device [10, 11]. In addition, electrodes of n-type OTFTs need to have low work function for efficient electron injection. But, the electrodes with low

work function are easily hydroxylated and oxidized. As a result, the electrodes change

into insulating dielectrics and delaminate from the organic semiconductor so that their

conductivity seriously drops. Due to the main issue of the air-stability, p-type OTFTs

have been mostly used for commercial organic electronics whereas n-type OTFTs are

still in the level of laboratory research items.

1.2 Organic semiconductors

Organic semiconductors are required to induce carrier mobility and current

modulation (the ratio of I_{on}/I_{off}) high enough to function as a good active layer of OTFTs.

Unlike strong covalent bonds in inorganic semiconductors, organic molecules are

bonded by the weak Van der Waals force so that the weak inter-molecular coupling

results in high effective mass [12]. In addition, their carrier movements are interrupted

by scattering at crystalline grain boundaries and self-trapping. As a result, the best

carrier mobility of an organic semiconductor is still three orders of magnitude lower than

that of an inorganic semiconductor as shown in figure 3 [13, 14].
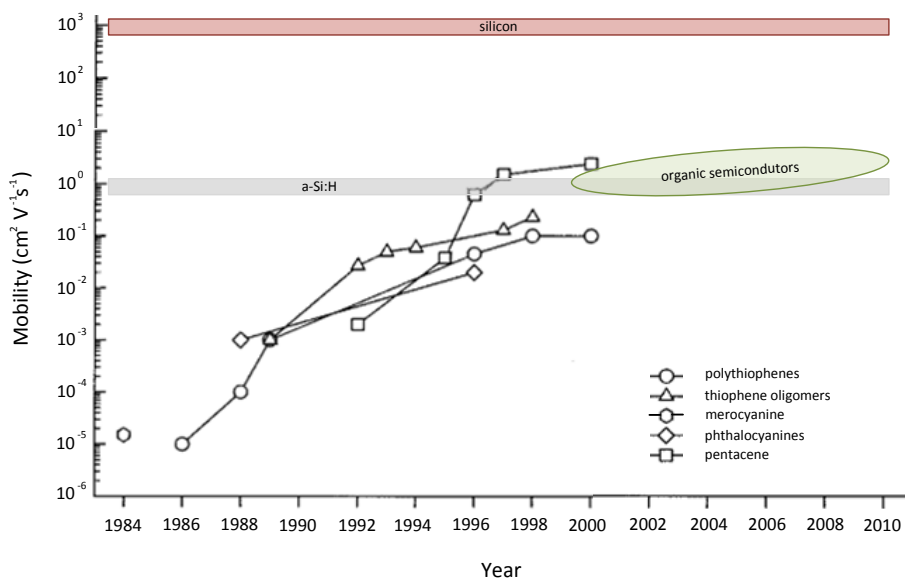
Figure 3. Carrier mobility of organic and inorganic semiconductors

Organic semiconductors are sorted into small molecules and conjugated polymers based on their sizes [15]. For example, pentacene belongs to the group of small molecules and P3HT is one of the conjugated polymers as shown in figure 4. According to the classified groups, they show different features that affect fabrication processes and electrical characteristics of OTFTs. As to thin-film preparation for an organic active layer, conjugated polymers can be deposited in a solution phase whereas small molecules are mostly processed in a gas phase. Unlike vapor deposition that requires high vacuum, solution-based processes such as printing and spin-coating techniques can be easily carried out at room temperature. In addition, the solution-based processes can be applied to large area at a very high speed. Consequently, polymer thin-films can be deposited at a low cost and with a high throughput compared to small molecule thin-films.
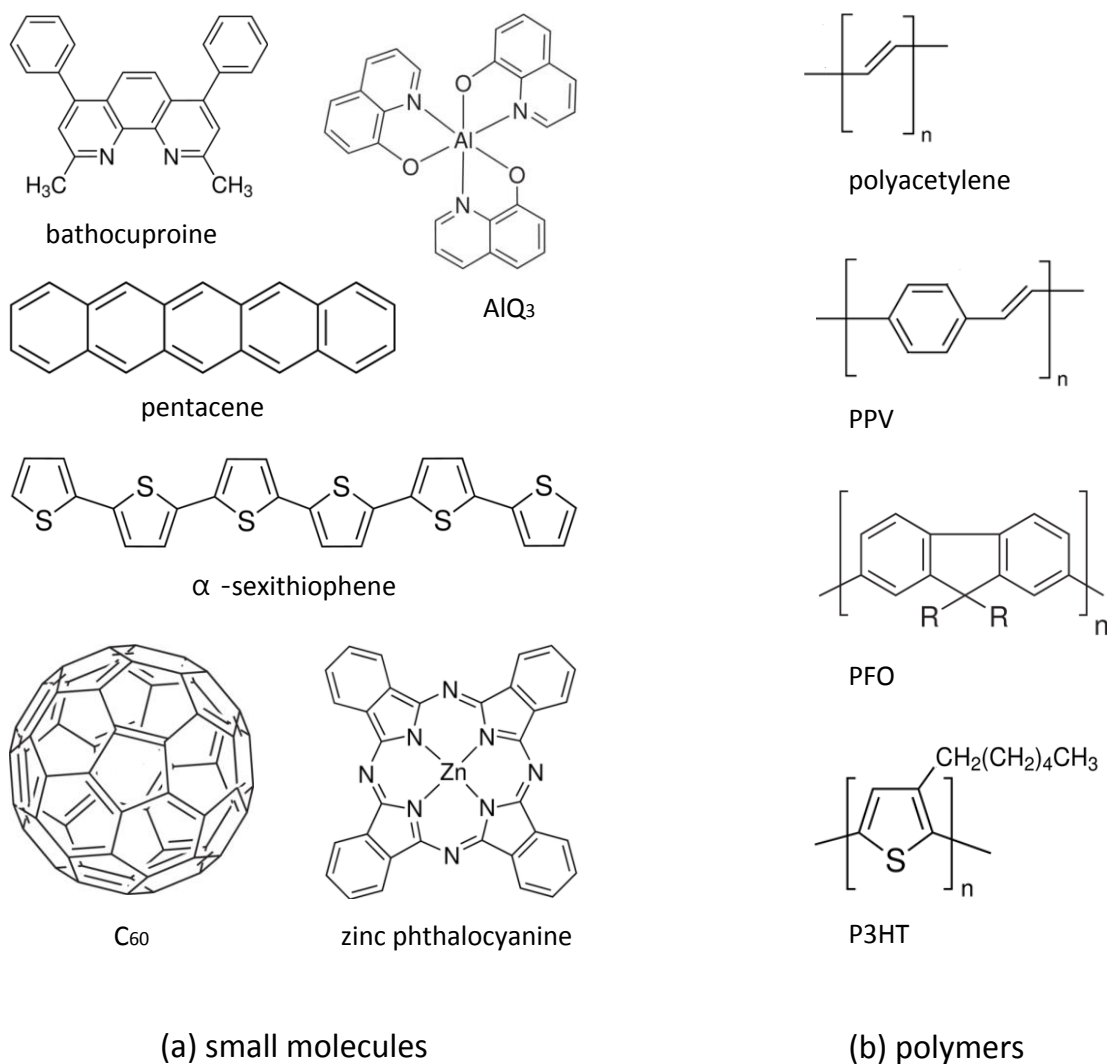
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Figure 4. Classification of organic semiconductors

In spite of such advantages in a fabrication process, conjugated polymers in solution tend to form a thin-film with poorer electrical property. The reason can be found from the degree of crystallization of organic semiconductor. Conjugated polymers are mostly semi-crystalline with amorphous regions after deposition while small molecules can form organic crystals. Because ordered structure through crystallization facilitates

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(a) small molecules   (b) polymers

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more rapid carrier movement in organic semiconductor, crystallized small molecules show much higher carrier mobility than conjugated polymer. For example, pentacene, one of commonly used small molecules, was already optimized to have the hole mobility of 5.5 cm^2/Vs that is higher than the carrier mobility of hydrogenated amorphous silicon (μ of a-Si:H: ~ 1 cm^2/Vs) [16]. On the other hand, the maximum carrier mobility of conjugated polymers still stays in the order of 0.1 cm^2/Vs [17].

Despite of the high carrier mobility, small molecules are not preferred for a large-area application due to the expensive cost of vacuum deposition. Therefore, the solubility of organic semiconductors is indispensable for price competitiveness. One way to make small molecules soluble is to substitute some ends of the small molecules with soluble precursors [18]. This approach efficiently increases the solubility of small molecules at a cost of electronic property degradation that results from non-conductible precursors. Representative soluble small molecules are 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-PEN) and 5,11-bis(triethylsilylethynyl) anthradithiophene (TES-ADT) that are synthesized from pentacene and anthradithiophene by combining soluble precursors (figure 5). It was reported that the carrier mobilities of 1.0 cm^2/Vs and 1.8 cm^2/Vs were achieved in OTFTs using TES-ADT and TIPS-PEN, respectively [19, 20]. Although it is hard to avoid some extent of performance degradation, the soluble precursor technique deserves in-depth researches because soluble small molecules not only show relatively high mobility compared to conjugated polymers, but also enable a low-cost fabrication.
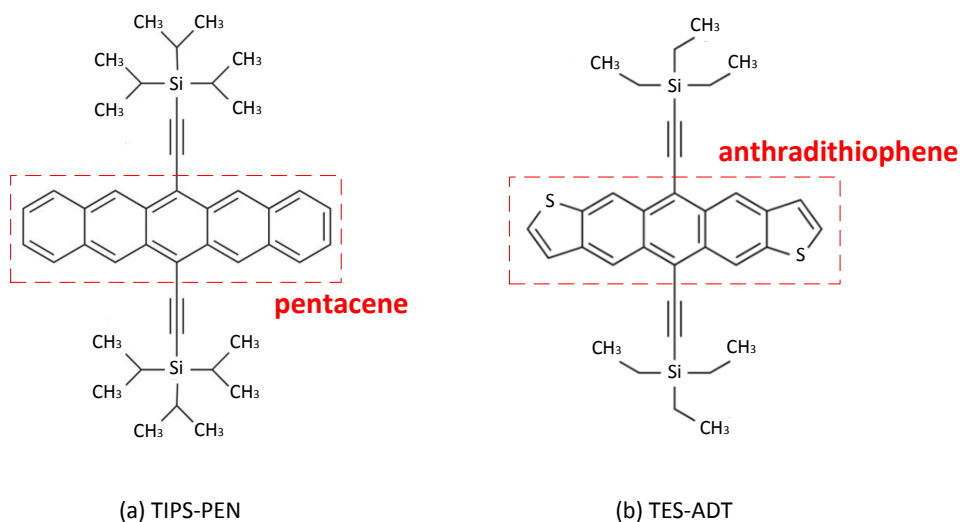
Figure 5. Molecular structures of soluble small molecules

In addition to developing efficient soluble small molecules, several notable

efforts have been made for the purpose of maximizing the carrier mobility through

single-crystals. Because single-crystals have highly ordered molecular structures and no

crystal defect, it has been expected that the highest carrier mobility can be realized from

single-crystalline OTFTs. However, many experiments in early stages did not achieve

satisfactory results so that mobility in single-crystalline OTFTs were even lower than the

highest mobility previously reported for the same materials [21-23]. Their poor

performance mainly resulted from the bad interface of single-crystals rather than the

single-crystal itself. Although it has been regarded as a hard task to make fragile and flat

single-crystals consistently contact both insulator and source/drain electrodes, there has

been continuous research to improve the interface condition. As a result, a carrier

mobility of 19 cm^2/Vs was realized from an OTFT with rubrene single-crystals [24].

1.3 Gate dielectrics

Gate dielectric in OTFTs is another crucial component whose effects on device performance are much broader than in inorganic transistors [3, 25]. The effects of the gate dielectric can be comprehensively analyzed in terms of insulator material, surface roughness, polarity at interface with an organic semiconductor, and employed device configuration (bottom-gate type or top-gate type). As an inorganic dielectric material, silicon dioxide (SiO_2) has been traditionally utilized. Given large numbers of defects and low carrier density in organic semiconductor active layers, however, the relative low dielectric constant of SiO_2 ($k = 3.9$) cannot induce a sufficient amount of accumulated charges at a low-voltage bias. Consequently, the need of high-k insulators arose to realize the low-voltage operation of OTFTs. The first low-voltage operation was demonstrated from pentacene-based TFTs which used high-k insulators such as barium strontium titanate (BST, $k = 16$), barium zirconate titanate (BZT, $k = 17.3$), and silicon nitride (Si_3N_4, $k = 6.2$) [26]. The OTFTs exhibited mobility of higher than 0.3 cm^2/Vs at the operation voltage of 5V. Although there were several controversial reports showing that carrier mobility decreased with increasing dielectric constant due to enhanced charge localization at higher polarity interface [27, 28], high-k insulators have been continuously researched as an effective way to reduce operating voltage [29, 30].

In addition to the dielectric constant, insulator surface state is another important parameter because it directly interacts with an organic semiconductor active layer. A rough surface leads to carrier traps at the insulator-semiconductor interface and it hinders the formation of a highly oriented organic semiconductor film. Consequently,

the interface roughness seriously degrades the available carrier mobility especially in bottom-gate type devices. The roughness can be effectively reduced by employing self-aligned monolayers (SAMs) such as hexamethyldisilazane (HMDS), octodecyltrichlorosilane (OTS), (tridecafluoro-1,1,2,2-tetrahydrooctyl) trichlorosilane (FTS) and phosphonic acid monolayers on the gate dielectric before depositing the organic semiconductor [31-33]. The SAMs can also chemically modify the dielectric surface so that it lowers surface-energy. As a result of the surface treatment, gate dielectric surface becomes smooth and passivated. The modified insulator surface enhances the molecular ordering of organic semiconductor and minimizes the carrier trap density at semiconductor-insulator interface. A polycrystalline pentacene TFT with a phosphonic acid-treated alumina dielectric even showed a mobility of ~ 3 cm^2/Vs which is close to that of a single-crystalline device [33].

Unlike in bottom-gate type OTFTs, only limited deposition processes can be harnessed to form dielectric films in top-contact type OTFTs in which the dielectric deposition processes may seriously affect the electrical characteristics of susceptible organic semiconductor active layers. Hence, OTFTs have been mostly fabricated in the configuration of bottom-gate devices. Although there were attempts to deposit inorganic materials such as Ta_2O_5 on organic semiconductor films through relatively safe electron-beam evaporation, it was also reported that high off-current occurred in the top-gate devices with the inorganic dielectrics [34]. The high off-current may be explained by oxygen doping during the evaporation process. In spite of the challenging gate dielectric deposition, top-gate configuration is still worth considering because mobility tends to be

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several times higher in a top-gate structure than in a bottom-gate structure [34]. To easily

and safely realize top-gate devices, solution-based processes such as printing or spin-

coating have been considered. Therefore, most top-gate OTFTs have been fabricated

with solution-processible organic materials as their gate dielectric instead of inorganics.

In addition to the solution-processibility, organic materials are compatible with flexible

devices. In spite of such advantages of organic insulators, OTFTs with organic gate

dielectrics were less attractive to practical applications due to their high operating

voltages that were required to compensate their quite low capacitors. However, their

operating voltages have been recently improved through ultrathin organic insulator films

that have been formed by self-aligned mono- or multiple-layers or 3D cross-linked

multilayers [35-37]. While thin inorganic insulators typically suffers large leakage

current, the ultrathin organic insulators show much better insulating property so that they

are compatible with low-voltage operation devices.

1.4 Fabrication and its limitations

Although there are several deep submicron lithography techniques such as

optical lithography, electron beam (E-beam) lithography, and nanoimprint lithography in

industry, those techniques have not been deployed on an organic semiconductor film due

to strict conditions of OTFT fabrication. Because organic semiconductors are susceptible

to ultra violet (UV) light and oxygen that critically degrade the performance of OTFT,

the high-resolution lithography techniques - that normally use intensive UV light or

oxygen plasma as their lithography resource - have not been applied to electrode

patterning on organic semiconductor. For instance, a device is exposed to intensive UV light during optical lithography. In case of E-beam lithography, it is a destructive lithography so that organic semiconductor film is destroyed during patterning. Organic semiconductor film is also damaged by an oxygen dry etching that is normally carried out after nanoimprint lithography.

In spite of the strict conditions of organic semiconductor fabrication, several research groups realized nanoscale OTFTs in the bottom-gate and bottom-contact structure. Because they deposited organic semiconductor active layer after forming all other elements of an OTFT that were patterned through high-resolution lithography techniques, organic semiconductor film was not damaged by UV or oxygen plasma. However, the nanoscale OTFTs did not show a significant performance improvement due to critical drawbacks of the bottom-contact structure such as high contact resistance and poor crystallization of organic semiconductor [38, 39]. Therefore, the bottom-contact type of OTFTs became less attractive to a commercial market. On the other hand, the top-contact type of OTFTs has been mostly fabricated through low-resolution lithography techniques that do not have a negative influence on the performance of OTFTs.

Direct evaporation through a shadow mask and various printings – inkjet printing, screen printing, stencil printing, gravure printing, micro-contact printing, and laser-transfer printing – have been commonly used to safely pattern electrodes on the organic active layer [40-42]. Because those techniques can be carried out at a low-temperature, even at room temperature, they can be freely applied to diverse substrates including

flexible or transparent materials. Besides, they show not only cost-effectiveness but also high throughputs owing to simple operations so that those techniques are suitable for large area applications. In spite of such attractive advantages, most of them have a resolution limitation that still stays at microscale as shown in figure 6. Although there is a possibility to form nanoscale metal patterns through a fine shadow masking [43], there are several insuperable obstacles in expending the possibility from a laboratory result to commercial mass products. For example, holes of the shadow mask are shrinking or disappear over multiple evaporations. Furthermore, the thin membrane of the shadow mask is easily bent so that it can cover only a restricted small area without the mask bending. Therefore, commercial OTFTs have been typically fabricated in microscale.
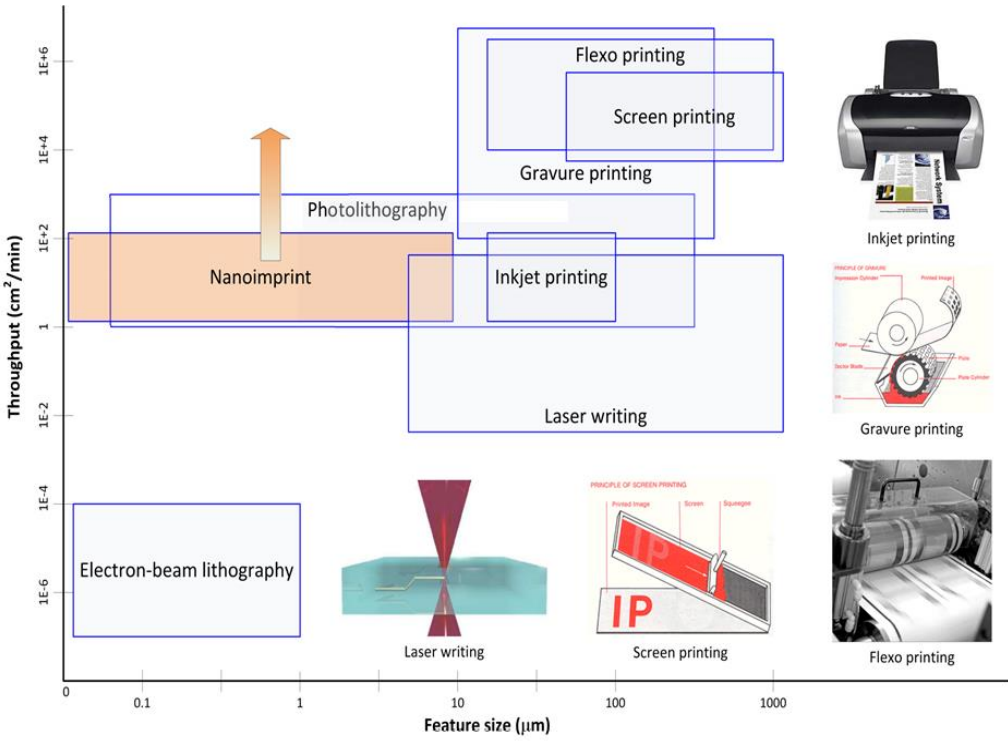
Figure 6. Throughputs and resolutions of commercial lithography techniques

1.5 Solutions towards a high performance OTFT

Low performance of OTFTs is mostly attributed to poor electrical characteristics of the organic semiconductor active layer, rough insulator, large overlap capacitance of conventional device structures, and low-resolution of available lithography techniques. There have been tremendous efforts to improve the electrical characteristic of organic semiconductor and insulator. As a result, the carrier mobility of amorphous silicon was already beaten by several organic semiconductors although average carrier mobility of crystalline inorganic semiconductors is still quite higher. On the other hand, there have been rare attempts to overcome the structural weakness and the resolution limitation although remarkable performance improvement was theoretically expected from the equation of cut-off frequency(f_T), which is one of the most important performance measures for OTFTs. The equation is written as:

$$f_T = \frac{g_m}{2\pi(C_G + C_{par})} \qquad \text{[Eq. 2]}$$

where $g_m \left(= \frac{W C_G}{L}\mu V_{DS}\right)$ is transconductance, C_G is gate capacitance, and C_{par} is overlap parasitic capacitance between source, drain, and gate. For example, the cut-off frequency of 800 MHz is expected when channel length is reduced to 0.1 μm although the cut-off frequency of today's OTFTs is still slower than 1 MHz.

Among deep submicron lithography techniques, the nanoimprint lithography (NIL) technique has room to avoid negative factors on subtle organic active layer.

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Nanoimprint is defined as a mechanical forming technique that physically molds a deformable material into a desired shape or pattern. There are two kinds of nanoimprint techniques. One is UV nanoimprint and the other is thermal nanoimprint. Like the optical lithography, UV nanoimprint involves intensive UV light. So it is not proper for OTFT patterning. However, thermal nanoimprint does not involve UV light. But, it is normally followed by oxygen dry etching to remove a residue layer. As shown in figure 7, the residue layer is formed as a by-product of nanoimprint process. Therefore, patterns can be complete only after removing the unwanted residue layer. If the residue layer is not formed during a thermal nanoimprint, the thermal nanoimprint is a possible solution to achieve deep submicron organic patterns. In addition to the high resolution, high throughput and low-cost process can be achieved by the thermal nanoimprint due to its quite simple operation mechanism.
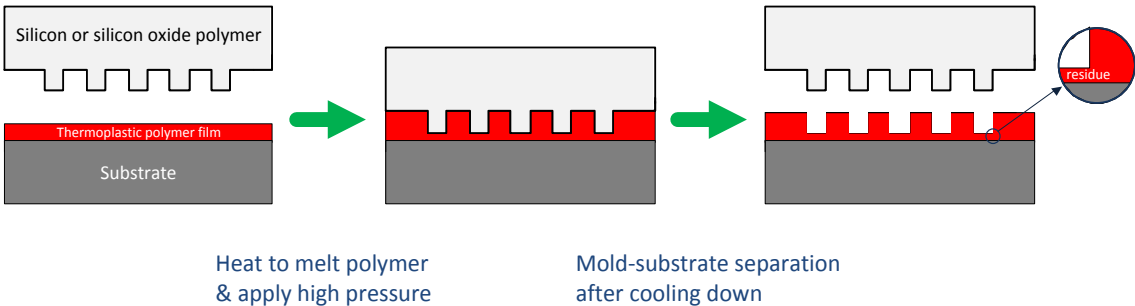
Figure 7. A schematic for thermal nanoimprint lithography process

There is more room to improve the performance of OTFTs. It is impossible to get a self-aligned structure from the conventional configurations. In order to enable a self-

aligned OTFT, a concept of double-layer patterning is considered as shown in figure 8. Because thermal nanoimprint resist can be used as a dielectric and nanoimprint can deform organic semiconductor film as well as the resist, thermal nanoimprint is a good candidate for the double-layer patterning. If two polymers that are used as the resist and the organic semiconductor are not mixed during thermal nanoimprint, the thermal nanoimprint on the dual-polymer layer may form the double-layer patterns that will be used to achieve the self-aligned OTFT.
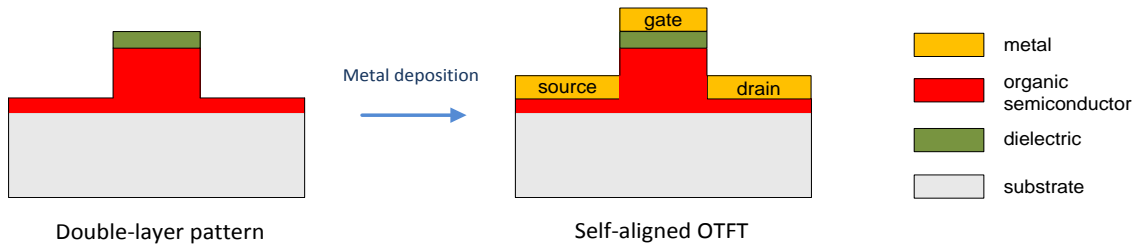
Figure 8. A self-aligned OTFT using double-layer pattern

In addition, the performance of OTFT can be improved through MESFET-like structure. The MESFET structure eliminates the overlap between source, drain, and gate as shown in figure 9. Furthermore, the structure tends to minimize the gap between source (or drain) and gate so that parasitic resistance existing between electrodes are reduced. Hence, the MESFET-like structure is an effective way to decrease parasitic resistance and capacitance. Based on the more complex equation of cut-off frequency [44],

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$$f_T = \frac{g_m}{2\pi \left[C_G \left(1 + \dfrac{R_D + R_S}{R_{DS}} \right) + C_{GD} g_m (R_D + R_S) + C_{par} \right]} \qquad \text{[Eq. 3]}$$

where source and drain resistances (R_S, R_D, R_{DS}) and gate-drain capacitance (C_{GD}) are additionally considered, higher cut-off frequency is expected from the reduced parasitic resistance and capacitance.
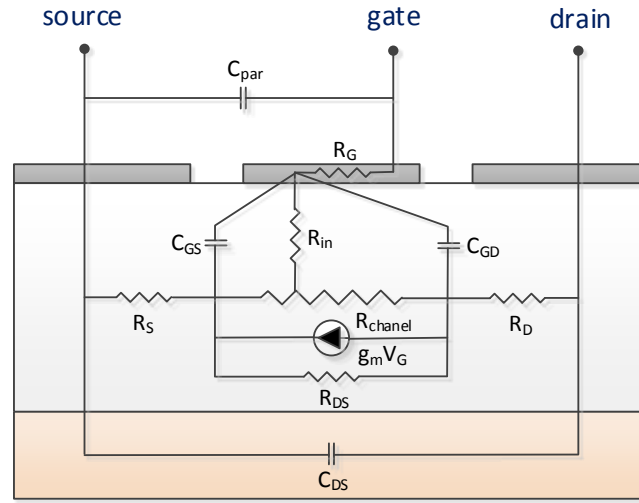
Figure 9. A small-signal equivalent circuit of a MESFET [44]

In addition, rectifying contact at gate efficiently replace a poor gate insulator that is considered as one of main performance degradation factors in OTFTs. In order to realize the MESFET-like structure without alignment errors, the application of the dual-layer thermal nanoimprint is expanded from two-dimension to three-dimension. As illustrated in figure 10, 3D resist pattern leads to 1st metal pattern with side-wing. The side-wing structure is utilized for self-aligned 2nd metal pattern.
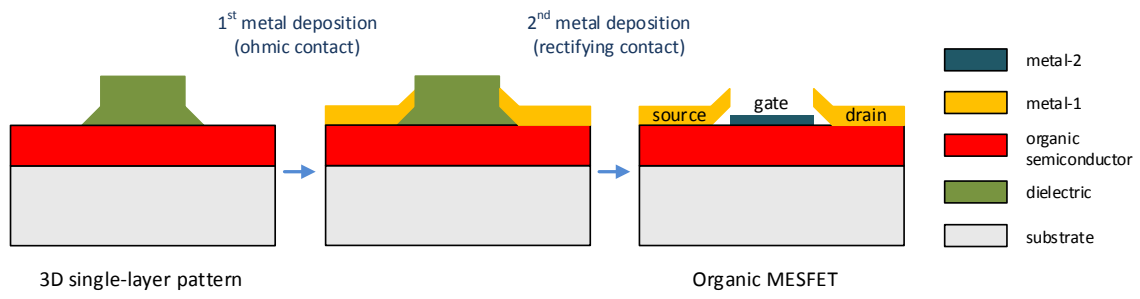
Figure 10. An OMESFET fabricated based on 3D single-layer patterns

CHAPTER II

DUAL-LAYER THERMAL NANOIMPRINT LITHOGRAPHY WITHOUT DRY

ETCHING[*]

2.1 Introduction

Nanoimprint lithography has been widely researched as one of the next

generation lithography techniques since it was first demonstrated that it has nanoscale

patterning capability [45, 46]. Nanoimprint is based on a direct mechanical molding of a

deformable resist layer [47-49]. Therefore, it not only simplifies the lithography process,

but also overcomes the resolution limitation that exists in photolithography due to light

scattering. In addition, the nanoimprint resist can be a specific functional material that

remains as an active component of a device instead of serving just as a mask layer for

pattern transfer [50]. The mechanical deformation of a nanoimprint resist can provide

sub-10 nm resolution at low cost [51, 52].

Despite its advantages, nanoimprint still needs development to satisfy strict

industrial requirements for mass production such as high throughput, high yield, and

process stability over multiple layers [50]. One of the challenges comes from the

residual layer, which should be removed to complete pattern definition [53]. Therefore,

an oxygen plasma dry etching after the thermal imprinting process is usually needed to

remove the unwanted residual layer. However, dry etching renders nanoimprint

incompatible with soft functional materials such as organic semiconductors because the oxygen dry etching will degrade or even destroy those materials. There have been several studies to realize residue-free or negligible residual layer nanoimprinting and satisfactory results were achieved in both curable resists and polymer resists through incomplete mold cavity filling [54-56].

In order to accomplish residue-free nanoimprint on an organic semiconductor, we demonstrate in this paper an efficient thermal nanoimprint onto dual non-compatible polymer layers, poly (methyl methacrylate) (PMMA) on P3HT. These two polymers are non-compatible with each other and they do not mix even above their glass-transition temperatures (T_g of PMMA: 105 $^\circ$C [57] of and T_g of P3HT: 45 $^\circ$C [58]). Depending on thermal nanoimprint parameters such as polymer thickness, mold depth, and nanoimprint temperature, two distinct and useful patterns can be formed as schematically shown in figures 11 and 12. In figure 11, pattern is only formed in the PMMA layer and this case is referred to as single-layer patterning. In figure 12, pattern is formed in both PMMA and P3HT layers and this scenario is referred to as double-layer patterning. The key concern of the single-layer pattern imprinting is to remove the PMMA residual layer on the P3HT without damaging the P3HT layer. It is successfully achieved through a delicate resist volume control. In the case of double-layer patterning, the flatness of the interfacial boundary between the PMMA and the P3HT layers is crucial for applications such as self-aligned OTFT. A smooth interfacial boundary can be achieved by controlling mold geometry and polymer film thickness. The patterning technique described in this work eliminates the oxygen dry etching step in thermal nanoimprint.

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This feature makes the patterning process highly compatible with organic functional materials such as conjugated semiconducting polymers. Both single- and double-layer patterns can find important applications in the fabrication of organic electronics.
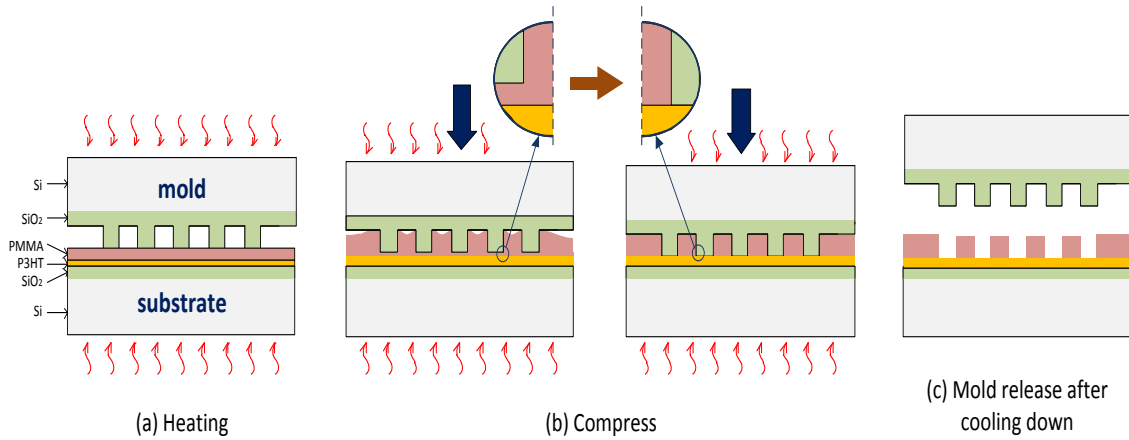
Figure 11. A schematic for the dual-layer thermal nanoimprint lithography process shows single-layer patterning. Only the top PMMA layer is patterned, while the bottom P3HT layer is intact.
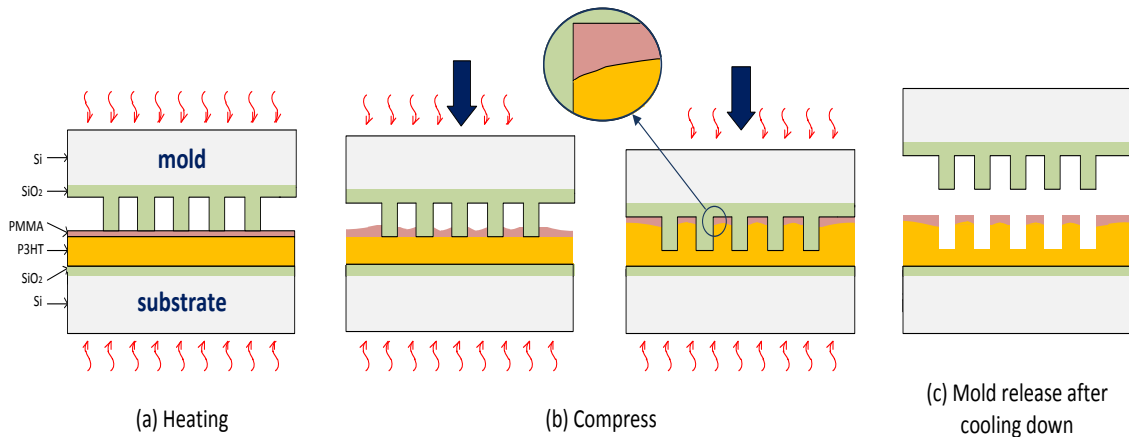
Figure 12. A schematic for the dual-layer thermal nanoimprint lithography process shows double-layer patterning. Both PMMA and P3HT layers are patterned.

2.2 Experimental methods

2.2.1 Adhesion improvement and dual polymer layer on SiO$_2$

Because P3HT thin film has poor adhesion on an oxide substrate, adhesion improvement is required for fabrication processes. In order to improve the adhesion of the P3HT thin film, amino-functionalized alkylsilane monolayer (bis[3-(trimthoxysilyl) propyl]-ethylenediamine, Gelest Inc.) was coated on the oxide surface before spin-coating the P3HT thin film [59]. The adhesion improvement was tested by visually observing the P3HT thin film in an ultrasound bath. While the P3HT thin film on a pure SiO$_2$ substrate started to peel off after 15 sec of sonication, the P3HT thin film on an aminosilane-coated substrate endured sonication for several minutes. The silane solution was prepared by adding 2 ml silane into methanol : distilled water (95ml : 5ml) that had been adjusted to pH = 5 with acetic acid. After 5 min for silanol formation, the wafer was dipped into the silane solution for 2 min and then it was rinsed in methanol. The wafer was cured at 110 ˚C for 10 min on a hotplate after drying methanol with nitrogen blowing. Afterwards, the adhesion-promoted oxidized silicon substrate was spin-coated with P3HT (highly regioregular, molecular weight: 20,000 ~ 40,000, Rieke Metals) and PMMA (molecular weight: 15,000, Sigma-Aldrich) consecutively. The P3HT solution and the PMMA solution were prepared by dissolving polymers in 1,2-dichlorobenzene and toluene, respectively. Various solution concentrations and spin-coating speeds were used for this study.

2.2.2 Non-compatibility testing for PMMA and P3HT

Non-compatible characteristic between PMMA and P3HT is a prerequisite for dual-layer thermal nanoimprint because it prevents the intermixing of PMMA and P3HT during nanoimprint and enables PMMA to dewet on P3HT. In order to verify the non-compatibility, thermal tests were carried out on SiO_2 samples that had been spin-coated with a dual PMMA (110 nm) and P3HT (85 nm) film. The thermal tests were performed in such a way that each sample was simply heated up to an intended temperature and then it was immediately cooled down. In order to investigate how temperature affects the dewetting process, the thermal tests were done at two different temperatures (180 and 220 ˚C). After cooling down the samples, the dewetting behavior of the PMMA layer was observed through an optical microscope.

2.2.3 Single-layer patterning

A silicon dioxide mold with 200 nm depth was prepared for imprinting. The mold was fabricated by photolithography and dry etching. The mold had 10 μm period grating with 45 % duty cycle (trench width: 5.5 μm and protrusion width: 4.5 μm). 1H,1H,2H,2H-perfluorodecyltrichlorosilane (FDTS, molecular weight: 581.56, Gelest Inc.) was coated over the mold for the purpose of anti-adhesion [60]. P3HT in 1,2-dichlorobenzene (10 mg/ml) was first spin-coated at 400 rpm for 5 min on the adhesion-promoted SiO_2 substrate to obtain 85 nm thick P3HT film. The P3HT-coated wafer was baked at 140 ˚C for 10 min in a vacuum oven. After the P3HT deposition, 3 wt. % PMMA in toluene was spin-coated on the P3HT layer at various spin-coating speeds

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(3000, 3300, 3500, 4000, 5000 and 7000 rpm) for 1 min and then the wafer was baked at

90 ˚C for 5 min. Toluene can dissolve P3HT very slowly, so quick spin-coating of

PMMA in toluene on P3HT surface had minimal observable effect on the P3HT layer.

Moreover, PMMA and P3HT will become phase segregated during nanoimprint due to

their non-compatibility and even some intermixing may occur at the layer interface

during spin-coating. Nanoimprint was performed in a commercial hydraulic hot press

(Specac) with heated aluminum (Al) plates. The mold was initially brought into contact

with the dual-polymer film. Then the mold and substrate were heated to 180 ˚C and a

pressure of 2500 psi was applied. While keeping the temperature and the pressure

constant, the sample was annealed for 20 min. After the annealing time, the sample was

cooled down to below their glass transition temperatures and then the mold was released

from the patterned substrate. PMMA patterns and the P3HT layer were observed through

both optical microscope and scanning electron microscope (SEM). In order to clearly

verify whether a PMMA residual layer existed on the P3HT layer, gold was deposited on

the patterned sample through a metal evaporator and then the sample was immersed in

propylene glycol methyl ether acetate (PGMEA, molecular weight: 132.16, Sigma-

Aldrich) to remove PMMA. PGMEA is a solvent that has no harmful impact on P3HT

[61]. In order to promote the gold lift-off, ultrasound was applied to the sample in

PGMEA for 30 sec. The lift-off result can be used to check if there exists a PMMA

residual layer on top of P3HT after nanoimprint.

2.2.4 Double-layer patterning

      In order to imprint both P3HT and PMMA in double-layer patterning, a thick

P3HT layer is preferred. Although a high P3HT concentration in 1,2-dichlorobenzene

(50 mg/ml) increases the thickness of the P3HT layer, it results in a rough P3HT surface

and a large film thickness non-uniformity. The rough P3HT surface is attributed to the

semi-crystalline nature of P3HT [62]. As a way to get a smooth P3HT surface, a multiple

spin-coating technique was adopted. Although the multiple spin-coating method reduced

film thickness, it was effective in achieving a smooth surface. After P3HT in 1,2-

dichlorobenzene (50 mg/ml) was spin-coated on an adhesion-promoted SiO_2 substrate at

400 rpm for 5 min, P3HT in 1,2-dichlorobenzene (30 mg/ml) was spin-coated thrice and

then P3HT in 1,2-dichlorobenzene (10 mg/ml) was spin-coated twice. Each additional

P3HT spin-coating was done at 1000 rpm for 5 min. After each P3HT spin-coating, the

sample was baked at 140 ˚C for 10 min in vacuum oven. After depositing the thick and

smooth P3HT layer, 2.5 wt. % PMMA in toluene was spin-coated on the P3HT layer at

6000 rpm for 1 min and then the sample was baked at 90 ˚C for 5 min. Two SiO_2 molds

were prepared to investigate the effect of mold geometry on the boundary interface

between the PMMA and the P3HT layers. One had 10 μm period grating with 45 % duty

cycle (trench width: 5.5 μm and protrusion width: 4.5 μm) and its depth was 400 nm.

The other had 750 nm period grating with 47 % duty cycle (trench width: 400 nm and

protrusion width: 350 nm) and the mold depth was 350 nm. Both molds were coated

with FDTS. Each mold was used for a dual-layer thermal nanoimprint as described in

figure 12. The imprint was also carried out at 180 ˚C and a pressure of 2500 psi with an

annealing time of 20 min. The dual-layer patterns and the boundary interface between P3HT and PMMA were investigated by SEM and optical microscope. To clearly visualize the P3HT structure under the PMMA patterns, each patterned sample was also observed after removing the top PMMA layer by dipping the samples in PGMEA.

2.2.5 Temperature range for dual-layer thermal nanoimprint

PMMA is non-compatible with P3HT and a smooth interface between the two layers can be maintained during nanoimprint. However at very high temperatures, both polymers melt and their viscosities become much lower. Consequently inter-penetration of liquid domains occurs during nanoimprint and it leads to irregular interface between the two layers. In order to find the upper limit of temperature, dual-layer thermal nanoimprints were performed on 60 nm PMMA on 730 nm P3HT at various temperatures (220, 230, and 250 ˚C). For these nanoimprints, a mold with 400 nm depth and 10 μm period grating was used. After each nanoimprint, patterns were investigated by optical microscope. In order to identify the inter-penetration of liquid domains of PMMA and P3HT, each sample was observed again through the optical microscope after dipping in PGMEA, which only dissolved the top PMMA layer.

2.3 Results and discussion

2.3.1 Non-compatibility of PMMA and P3HT

A thin PMMA film dewets on the P3HT layer at a high temperature because both polymers do not mix in a molten-state and the surface energy of the P3HT layer is low

[63]. As shown in figure 13, the dewetting starts with the ruptures of the PMMA film. As PMMA thin film dewets (figures 13(a) and (b)), bead- and worm-like PMMA ruptures (red color) occurs on P3HT surface (orange color). As the temperature increases, the dewetting quickly proceeds by expanding the ruptures and larger patches of PMMA are formed on P3HT surface (figure 13(c)). The fast dewetting progress is attributed to a lower viscosity of PMMA at a higher temperature. Since dewetting behavior is needed to achieve residual layer-free thermal nanoimprint [54], it is expected that PMMA melt can slip on P3HT surface and be squeezed into a mold cavity without leaving a residual layer on P3HT.
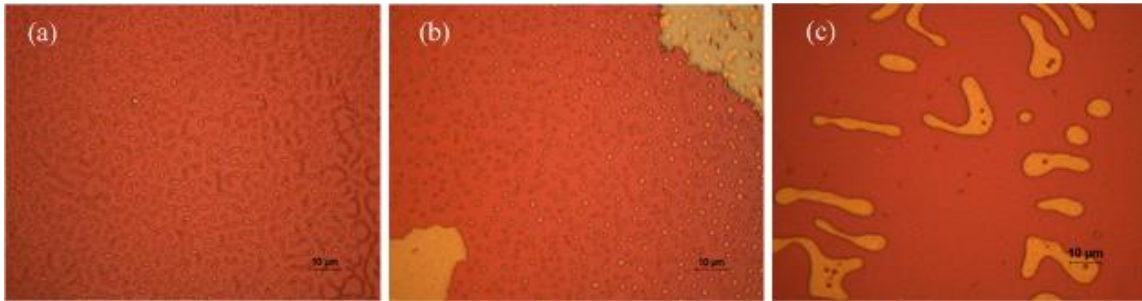
Figure 13. Optical microscope images of PMMA dewetting on P3HT at 180 ˚C ((a) and (b), including defects) and 220 ˚C (c). The orange-colored region is P3HT and the red-colored region is PMMA.

2.3.2 Single-layer patterning without residual layer

Single-layer PMMA patterns without a residual layer on the P3HT layer are successfully achieved through nanoimprint only where 3 wt. % PMMA in toluene is spin-coated between 3300 rpm and 4000 rpm. Given the mold geometry, trench width: 5.5 μm, protrusion width: 4.5 μm and depth: 200 nm, 110 nm PMMA film thickness is

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required to completely fill the mold cavity. Therefore, the result corresponds well with the measured PMMA film thickness (table 1). Although tiny dents that are resulted from incomplete filling exist on some PMMA patterns, they do not critically degrade the quality of the patterns as a lift-off mask. As shown in figure 14, no residual layer in the patterns is verified through a gold lift-off. Meanwhile, excessive or insufficient PMMA resist gives rise to a failure of gold patterning on top of P3HT. The residual layer due to excessive PMMA resist can be intuitively observed from the optical microscope image (figure 14(a)) that includes areas where some part of the residual layer peels off because of locally poor anti-adhesion of the mold. Furthermore, no gold pattern after the lift-off (figure 14(f)) proves the existence of the residual layer in PMMA patterns when PMMA is spin-coated at 3000 rpm. On the other hand, insufficient PMMA resist leads to incomplete filling of the mold cavity (figures 14(d) and (e)). In these cases, the lower P3HT layer is too thin to be deformed at the nanoimprint pressure, so the thin P3HT layer does not contribute to filling the mold cavity. Additionally, we found in our experiments that thin P3HT can only be imprinted at a temperature much higher than its glass transition temperature due to its high molecular weight and high viscosity. After gold lift-off, undesired gold patches between 5 μm gold lines are observed on the P3HT surface as seen in figures 14(i) and (j). In the cases when PMMA thickness is just enough to completely fill mold cavity, smooth PMMA patterns without residual layer are achieved in figures 14(b) and (c). Consequently, gold lift-off on those samples yields smooth and uniform gold lines on the P3HT surface (figures 14(g) and (h)). SEM micrographs verify these observations from optical microscope. In figure 15, well-

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formed PMMA patterns on top of the P3HT surface are shown under the optimal

processing parameters. When PMMA is too thin to fill the mold cavity, voids in PMMA

patterns are clearly seen in figure 16.
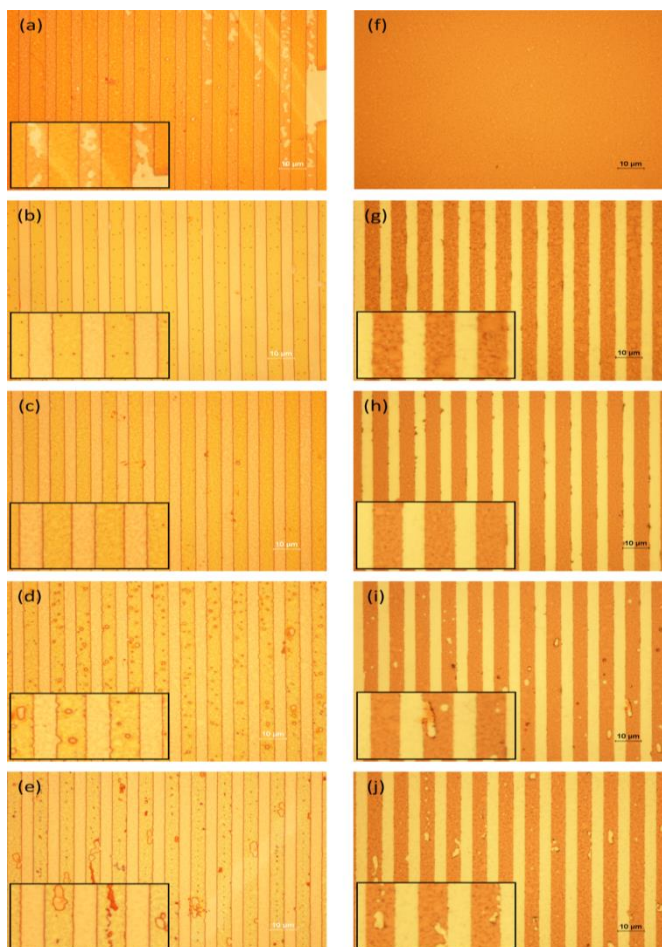
Figure 14. Optical microscope images of single-layer patterns (a, b, c, d, and e) and optical microscope images after their gold lift-off (f, g, h, i, and j) where 3 wt. % PMMA in toluene is spin-coated at 3000, 3300, 4000, 5000, and 7000 rpm, respectively. (a) The PMMA residual layer exists after nanoimprint, thus no gold pattern in (f). Notice that P3HT surface is not patterned by nanoimprint in (f); (b) and (c) have no PMMA residual layer after nanoimprint, and (g) and (h) show smooth 5 μm gold lines on top of P3HT after lift-off; in (d) and (e), PMMA is too thin to completely fill mold cavities, leading to defects in the form of voids in PMMA patterns. Gold lift-off in (i) and (j) shows gold patches in-between gold lines due to PMMA voids.
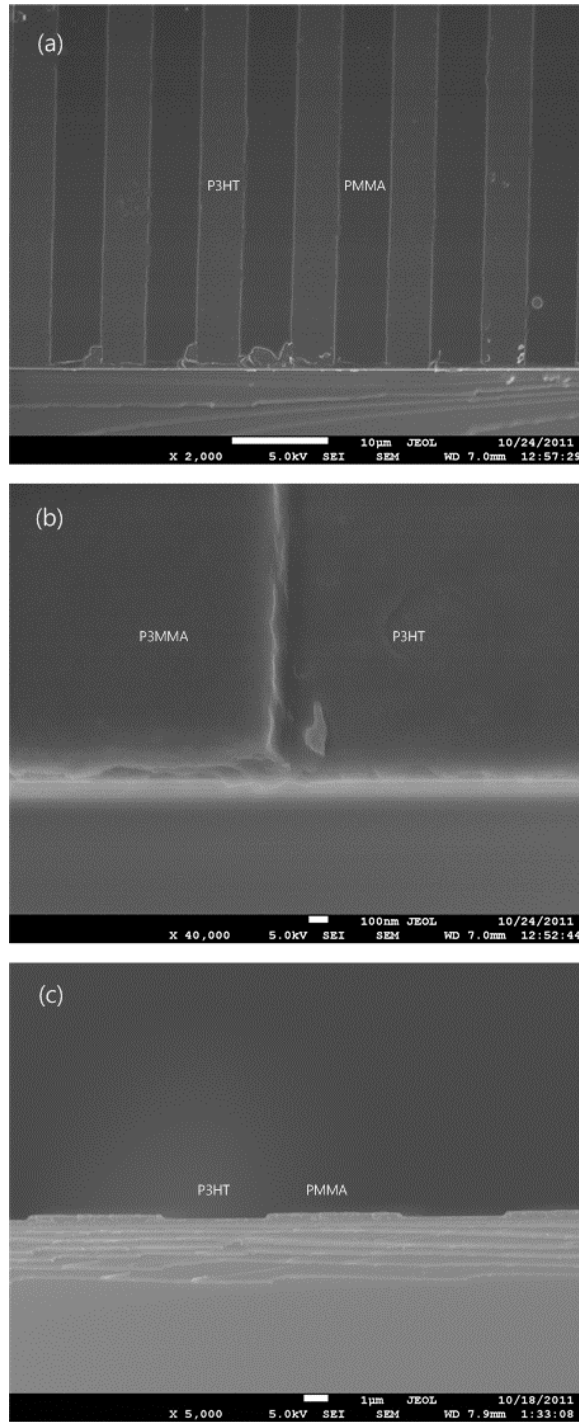
Figure 15. SEM images of the single PMMA layer patterns where 3 wt. % PMMA is spin-coated at 3500 rpm: (a) and (b) are the perspective views and (c) is the cross-sectional view.
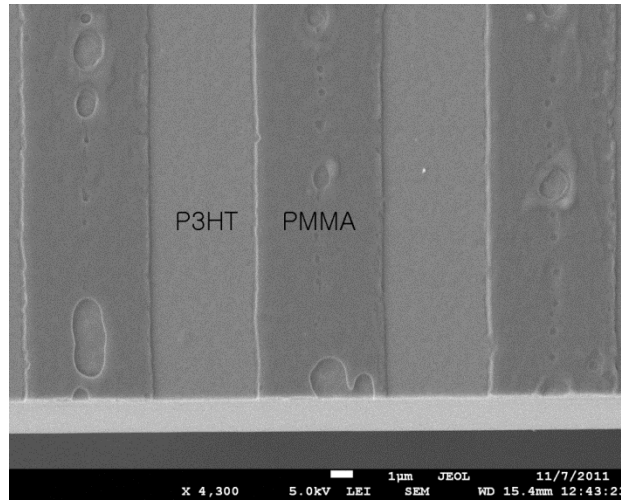
Figure 16. An SEM image of voids in PMMA patterns due to incomplete filling of mold cavity by PMMA melt where 3 wt. % PMMA is spin-coated at 7000 rpm.

Table 1. PMMA film thickness at different spin-coating speeds

spin-coating speed (rpm)	PMMA film thickness (nm)			
	measured data			average
1000	152	153	154	153
2000	127	129	134	130
3000	108	111	113	110.7
4000	97	101	102	100
5000	85	86	88	86.3
7000	72	73	75	73.3

The single-layer patterning can be utilized in organic semiconductor device fabrication. Due to material sensitivity, traditional photolithography and metal lift-off cannot be applied to conjugated polymers [64]. A direct metal deposition through a shadow mask has been commonly used to place metal pads on top of organic semiconductors. Recently, metal patterns in the nanoscale were realized through the approach [43]. However, the cost for such high-resolution shadow mask is high and this

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approach cannot be applied to a large area because of the distortion of the vulnerable

high-resolution shadow mask. Furthermore, the high-resolution apertures of the shadow

mask may shrink or be blocked over multiple metal depositions. Nanoimprint is

compatible to organic semiconductor because the patterning only requires heat and

pressure. However, nanoimprint has not been used for patterning metal structures on top

of organic semiconductors because it generally requires an oxygen dry-etching step to

remove the residual layer before metal lift-off, which will seriously damage organic

semiconductors. By eliminating the oxygen dry-etching step, the single-layer patterning

makes it possible to pattern high-resolution metal pads on top of organic semiconductors

for various types of organic electronic devices with improved performance.

2.3.3 Double-layer patterning

Unlike the single-layer patterning, a thick P3HT layer (thickness: 730 nm) is

prepared to facilitate the squeezing process of P3HT at the nanoimprint pressure for

dual-layer PMMA and P3HT patterning. In figure 17, the thick P3HT layer deposited

through multiple spin-coating shows a smooth P3HT surface while the thickness is

reduced by about 500 nm through the additional P3HT spin-coatings. Given the P3HT

thickness of 730 nm, two molds with different cavity widths produce morphologically

different P3HT structures under PMMA patterns. As shown in figure 18, a P3HT pattern

with a single peak is formed from a nanoimprint mold with a cavity width (400 nm) that

is narrower than the P3HT thickness (730 nm). From the cross-sectional image of the

P3HT patterns, it is identified that the P3HT peak looks like a gentle arc after PMMA

removal (figure 18(f)). P3HT patterns with dual peaks are formed when the mold cavity width (5.5 μm) is greater than the P3HT thickness (730 nm). As observed in figure 19, the dual peaks are highly localized near the mold sidewalls due to the viscous characteristic of P3HT. Consequently, the localized peaks cause PMMA thickness to be very thin near mold sidewalls. In the view of its application, the double-layer PMMA/P3HT patterns can facilitate a self-aligned metal deposition to fabricate a self-aligned OTFT device with very low parasitic capacitance for better ac performance. PMMA would be the gate dielectric in such OTFT and thin PMMA layer near pattern edges (figure 19) will cause inadvertent contact between gate and source/drain electrodes. Thus mold pattern size and film thickness need to be carefully selected to achieve relatively uniform PMMA thickness after dual-layer nanoimprint.

The two kinds of P3HT patterns after dual-layer nanoimprint are expected from the simulations of polymer flows that were reported in the literature [65, 66]. According to the simulations, polymer deforms differently during nanoimprint depending on three parameters: capillary number, polymer ratio, and cavity width to polymer thickness ratio. Among the parameters, the cavity width to polymer thickness ratio mainly affects the polymer flow profile. The profile becomes a single peak when the half width of the mold cavity is smaller than 1.2 times of the initial polymer film thickness. Otherwise, the polymer flow tends to give rise to a dual-peak pattern. Therefore, our observation from the dual-layer nanoimprint exactly corroborates these simulations.
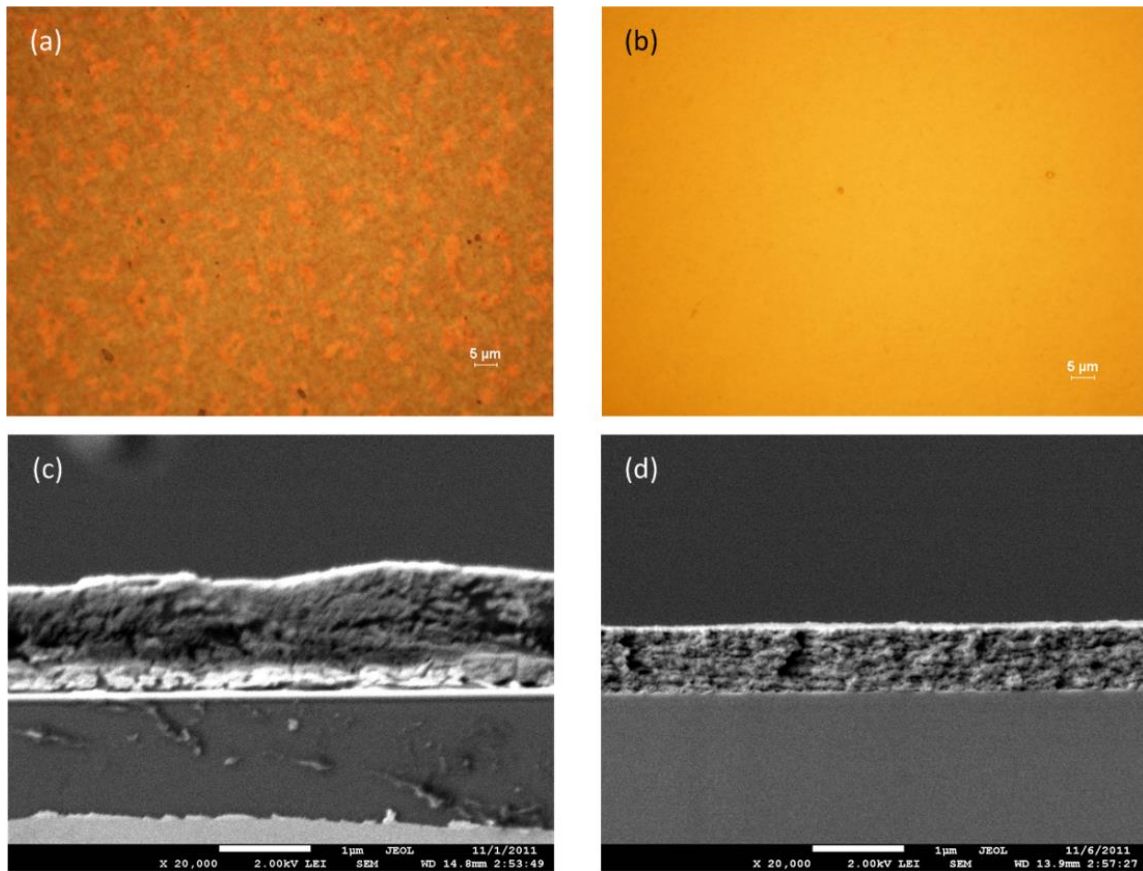
Figure 17. Optical microscope images of P3HT surface from single spin-coating (a) and multiple spin-coating (b), and their SEM cross-sectional images ((c) single spin-coating and (d) multiple spin-coating). The thickness of the P3HT layer from single spin-coating varies between 1.13 and 1.33 μm while the thickness from multiple spin-coating is uniform at 730nm.
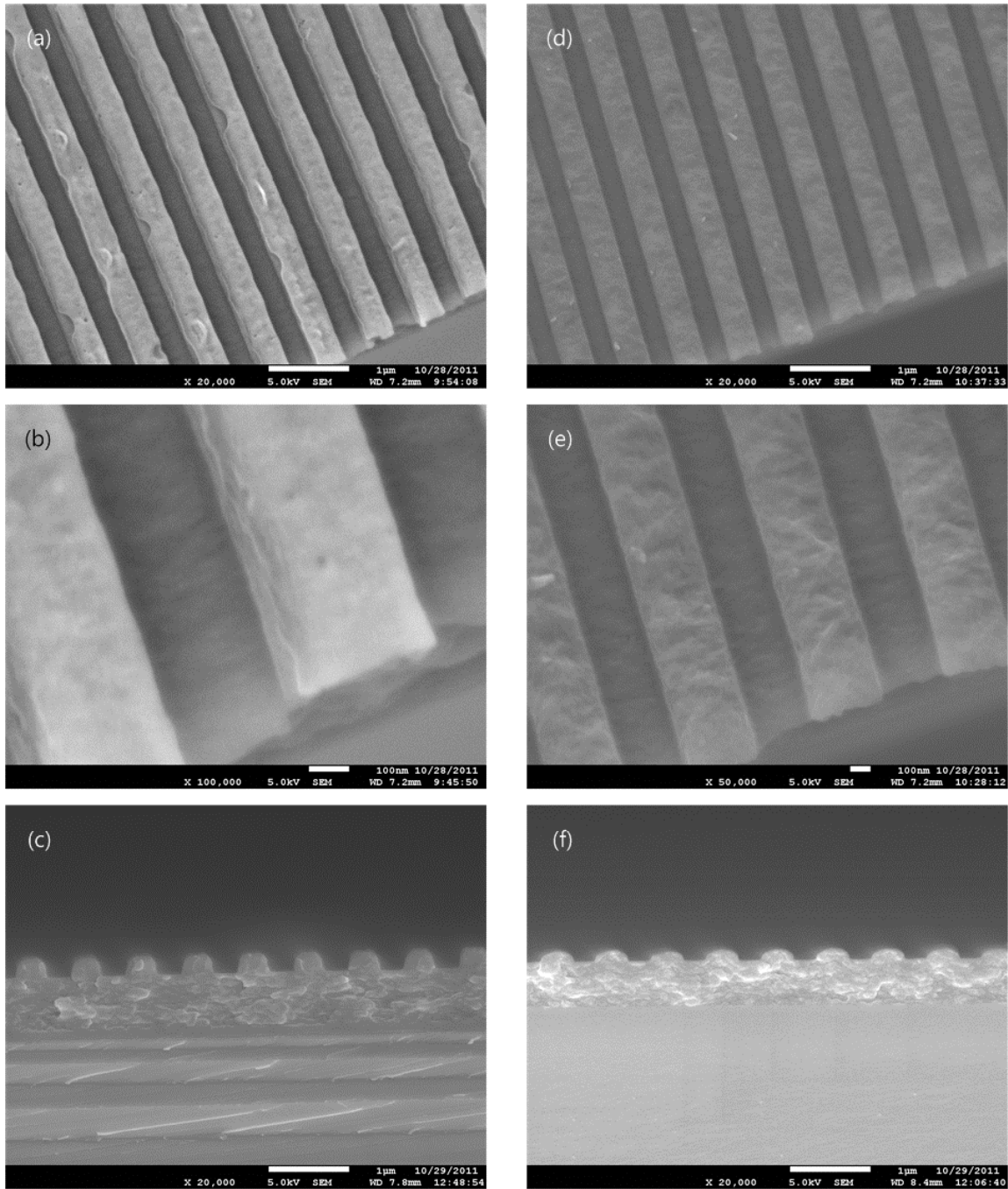
Figure 18. SEM images of double-layer PMMA and P3HT patterning ((a) and (b) are the perspective views and (c) is the cross-sectional view) and their SEM images after removing PMMA ((d) and (e) are the perspective views and (f) is the cross-sectional view). P3HT patterns with single peak are formed under the PMMA patterns. The mold used in this case has a cavity width of 400 nm.

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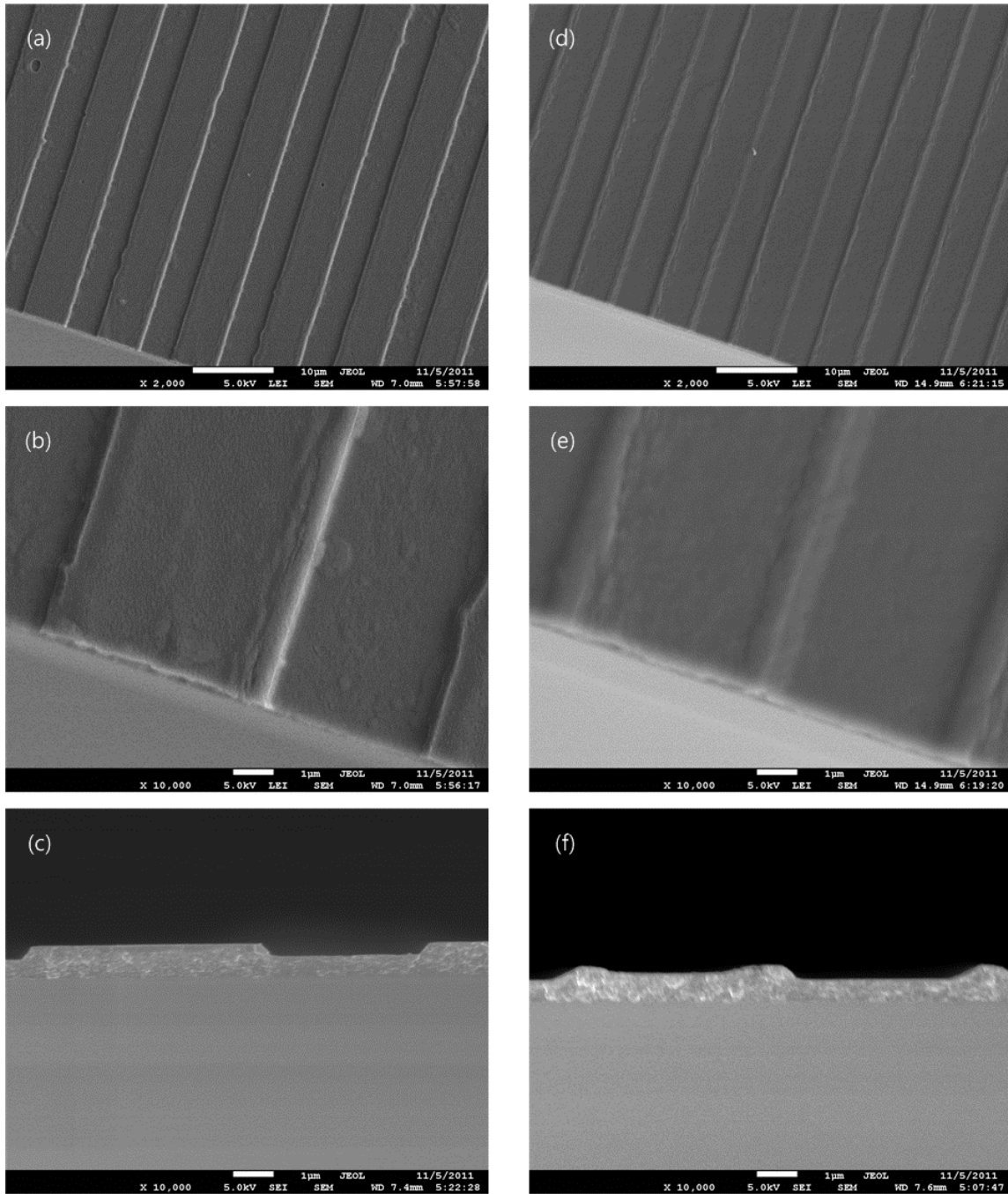
Figure 19. SEM images of double-layer PMMA and P3HT patterning ((a) and (b) are the perspective views and (c) is the cross-sectional view) and their SEM images after removing PMMA ((d) and (e) are the perspective views and (f) is the cross-sectional view). P3HT patterns with double peak are formed under the PMMA patterns. The mold used in this case has a cavity width of 5.5 μm.

2.3.4 Temperature range for dual-layer thermal nanoimprint

Unlike amorphous PMMA (T_g: 105 ˚C), semi-crystalline P3HT has both a glass transition temperature of 45 ˚C and a melting point of 233 ˚C [58]. Based on the glass transition temperatures, both polymers are in viscous state above 105 ˚C. Therefore, a dual-layer thermal nanoimprint can be theoretically performed on the PMMA-P3HT stack layer at a temperature above 105 ˚C. In addition to the lower temperature limit of 105 ˚C, there is an upper temperature limit below which the dual-layer nanoimprint can pattern as intended. The upper limit is identified through optical images of double-layer patterns that are imprinted at high temperatures. As shown in figure 20, the distinct dual peaks of P3HT patterns disappear and the admixture of both polymers due to very low melt viscosity comprises a large portion of patterns in samples imprinted at 230 and 250 ˚C. On the other hand, the sample imprinted at 220 ˚C has the proper double-layer pattern with the intended dual peaks in P3HT. These observations indicate that both polymers start to admixture at a temperature higher than or equal to 230 ˚C, which is close to the melting point of P3HT.
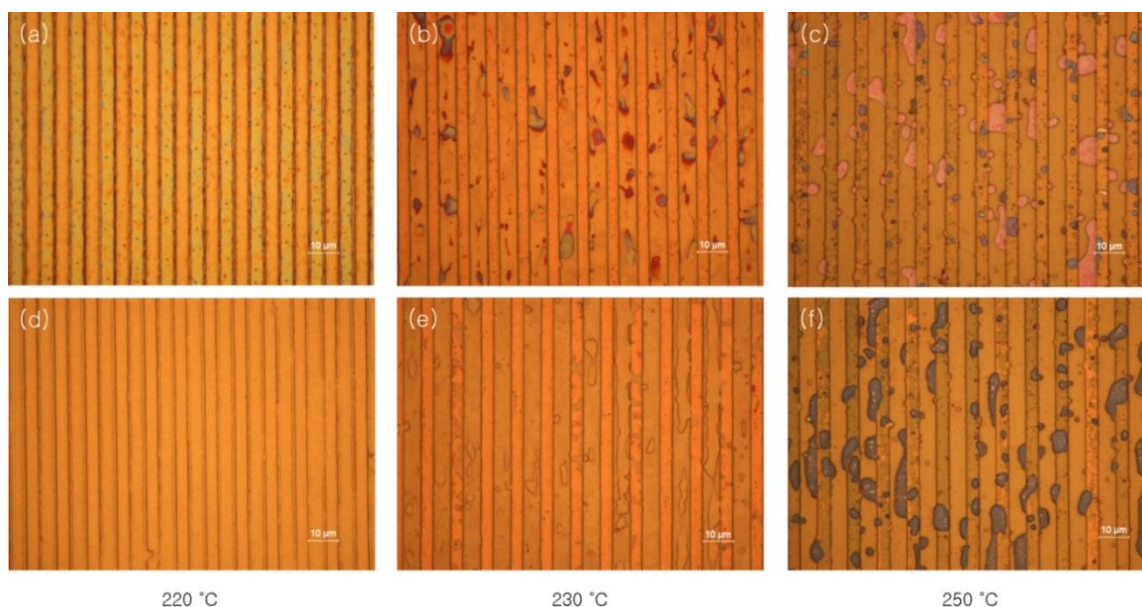
Figure 20. Optical microscope images of amixture of PMMA and P3HT melts in dual-layer nanoimprint at (a) 220, (b) 230, and (c) 250 ˚C. Their optical microscope images after removing PMMA are shown in (d), (e), and (f), respectively.

2.4 Summary

Dual-layer nanoimprint with non-compatible PMMA and P3HT layers are investigated in this work. In melt states, PMMA does not mix with P3HT and the surface energy of P3HT is low, so PMMA on P3HT easily slips and dewets without leaving a PMMA residual layer when a thermal nanoimprint is applied onto the stacked polymer layers. However, PMMA and P3HT polymer melts tend to mix with each other at temperatures above 220 ˚C. Based on the mixing temperature as well as the glass transition temperatures of both polymers, the optimal nanoimprint temperature range is determined for dual-layer nanoimprint. Within the optimal temperature range, the dual-layer thermal nanoimprint can yield two different patterning results, single-layer

patterning and double-layer patterning, depending on nanoimprint parameters. The single-layer patterning is successfully performed with a delicate PMMA volume control and a very thin P3HT layer. Unlike the single-layer patterning, a satisfactory double-layer patterning is achieved when a thick and smooth P3HT layer is formed under a thin PMMA layer. It is found that the required thick P3HT with a smooth surface is deposited through multiple P3HT spin-coatings that remarkably smoothen a rough P3HT surface. Furthermore, it is verified that the double-layer pattern profile is determined by the mold cavity width to polymer thickness ratio. The single-layer patterning can be used to deposit high-resolution metal patterns on top of P3HT for organic electronic applications. The double-layer patterning can be used to fabricate a self-aligned OTFT device that minimizes parasitic capacitance for improved ac performance. Those promising applications are enabled by the fact that no damaging dry-etching step is used in the dual-layer nanoimprinting process.

CHAPTER III

SELF-ALIGNED METALLIZATION ON ORGANIC SEMICONDUCTOR

THROUGH 3D DUAL-LAYER THERMAL NANOIMPRINT

3.1 Introduction

In order to avoid ultraviolet light and oxygen which seriously degrade the

performance of organic semiconductors [67, 68], organic semiconductor devices have

usually been patterned through low-resolution lithography techniques such as shadow

masking, inkjet printing, and screen printing [69]. Therefore, the fabrication of

submicron and nanoscale organic electronic devices for organic ICs has been regarded as

a challenging task. In order to realize nanoscale organic devices, high-resolution

lithography was indirectly applied to create a sacrificial template [70]. The approach led

to nanoscale organic semiconductor patterns but it was ineffective in patterning metal

layer on top of organic semiconductors, as required by the fabrication of many top-

contact devices. For an efficient metallization on an organic semiconductor, thermal

nanoimprint on dual non-compatible polymers was investigated [71]. The removal of a

destructive dry etching step through the dual-layer thermal nanoimprint enabled high-

resolution metal patterning on organic semiconductors without performance degradation.

In spite of the success in nanoscale metallization, the dual-layer thermal

nanoimprint technique still needs to overcome alignment difficulty for a multiple-level

metal patterning that is essential to implementing organic ICs. For example, the opacity

of a thermal imprint mold makes the alignment process very difficult in thermal

nanoimprint. In addition, thermal nanoimprint has inevitable and significant alignment errors that are resulted from multiple factors, including thermal expansion coefficient mismatch between the mold and the substrate, mold shift, wafer bending, and resist surface variation [72]. Consequently, the multiple-level metal patterning resolution is seriously restricted by the alignment errors. One effective way to eliminate the inherent alignment errors is a self-aligned metal patterning approach. Because the preceding metal patterns can be used as mask patterns for the succeeding metal patterns, this approach involves no misalignment so that it ultimately increases the resolution of multi-level metal patterning.

In order to realize self-aligned metal patterns on an organic semiconductor, we extend the dual-layer thermal nanoimprint technique through 3D imprint molds. The 3D molds can be fabricated through different methods: a combination of wet and dry etching and a selective dry etching [73]. The first technique leads to isotropic recesses on the sidewalls of mold trenches, and it is suitable for microscale dimensions; the second technique results in anisotropic recesses on the sidewalls of mold trenches, and it is good for nanoscale dimensions. Both 3D molds enable two different self-aligned metallization processes; one is based on isotropic side-wings and the other is based on anisotropic side-wings. The self-aligned metallization process based on isotropic side-wings is relatively simple; but it has a limitation in realizing a sub-100 nm gap between two metal patterns. On the other hand, a 60-nm gap is achieved through the self-aligned metallization process with anisotropic side-wings. In this experiment, gold and aluminum are used for the first and second metal patterns. Because the first metal pattern

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has ohmic contact to P3HT while a Schottky barrier exists between the second metal

pattern and P3HT, the fabrication schemes can be used to implement a top-contact

OMESFET, which can be used in high-performance organic ICs.

3.2 Experimental methods

3.2.1 Self-aligned metallization on P3HT based on isotropic side-wings
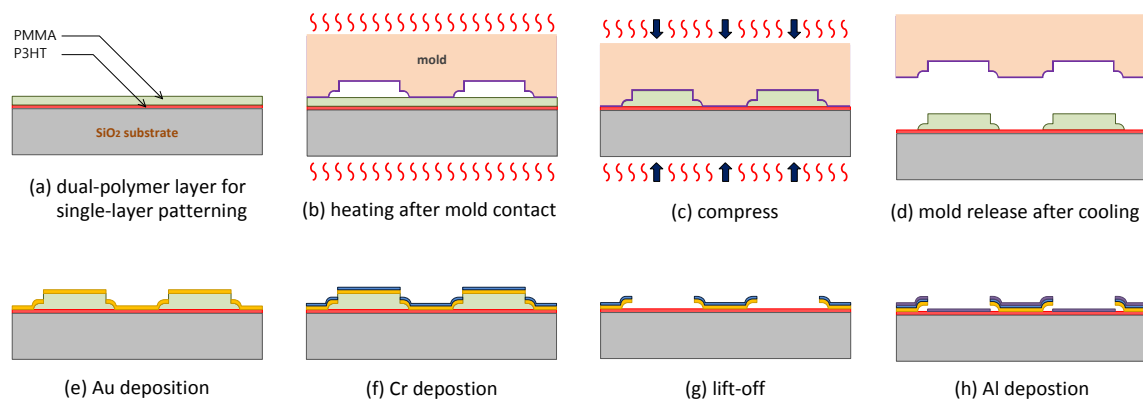
Figure 21. A schematic for the self-aligned metallization process based on istropic side-wings (scheme 1). The 3D nanoimprint mold can be fabricated by a combination of wet and dry etching. The nanoimprint process parameters are controlled such that only single-layer patterning of PMMA is accomplished and there is no PMMA residue layer in step (d) (See [71]) . After the step (h), we have two metal patterns in contact with P3HT: gold as ohmic contact and aluminum as Schottky contact. Such structure can be used as OMESFET in which the gold serves as the source/drain contacts and the aluminum serves as the gate control. The separation between the gold and the aluminum, which is a critical parameter for high-performance OMESFETs, is controlled by the mold structure.

Isotropic side-wings were utilized to easily realize self-aligned metallization on

an organic semiconductor. As shown in figure 21, the isotropic side-wings were

achieved through simple extensions of the existing dual-layer thermal nanoimprint

process such as the 3D mold with isotropic recesses on sidewall and additional

chromium (Cr) deposition on feeble gold patterns.

3.2.1.1 3D imprint mold fabrication

The first step of the process was the fabrication of the 3D imprint mold. A

combination of wet and dry etching shown in figure 22 was adopted to easily carve 3D

trenches on a silicon oxide wafer. For the etching pattern definition, chromium gratings

were patterned with the target of 10 μm period and 50% duty cycle on the oxidized

silicon wafer through a series of photolithography, metal evaporation, and lift-off steps

(figure 22(a)). The silicon oxide with the chromium grating patterns was dipped in

buffered oxide etch (BOE) for 2.5 min to form 155 nm deep trenches with curved

undercuts (figure 22(b)). After the isotropic oxide wet etching, reactive ion etching (RIE)

was carried out to anisotropically etch the trenches by additional 200 nm (figure 22(c))

and then the chromium patterns were removed by dipping the substrate in chrome

etchant for 10 min (figure 22(d)). After forming the 3D structures through the oxide

etching and chromium removal steps, the wafer was coated with FDTS monolayer for

the purpose of anti-adhesion (figure 22(e)) [74].

(a) Cr patterns on SiO2   (b) wet etching   (c) reactive ion etching

(d) Cr removal   (e) anti-adhesion monolayer
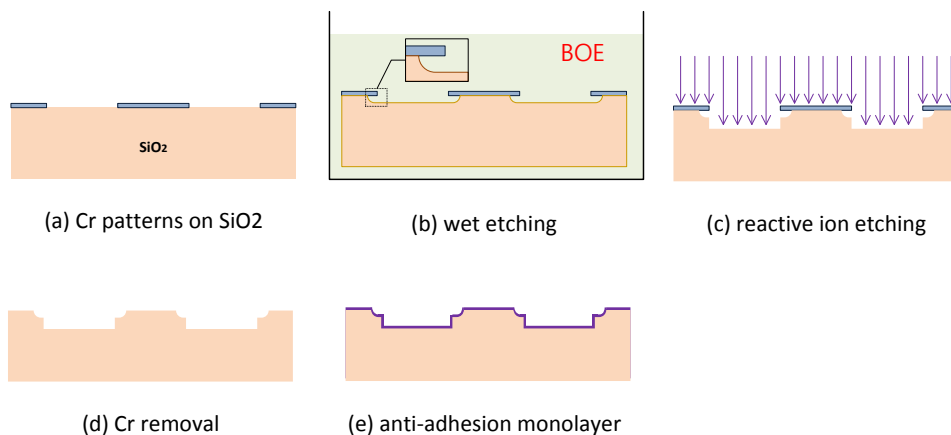
Figure 22. A schematic for the fabrication process for the 3D mold used in scheme 1. The mold has isotropic recesses formed by wet oxide etching.

3.2.1.2 Dual-layer thermal nanoimprint for 3D PMMA patterns on P3HT

In order to form 3D resist patterns on an organic semiconductor, a dual-layer thermal nanoimprint for single-layer patterning was chosen as the lithography technique [71]. The nanoimprint started from spin-coating dual polymer layers of PMMA and P3HT (figure 21(a)). Before forming the dual-polymer layer, the silicon oxide substrate was coated with amino-functionalized alkylsilane monolayer to improve the adhesion of P3HT on oxide surface [59]. After the adhesion improvement, P3HT in 1,2-dichlorobenzene (10 mg/ml) was spin-coated on the substrate at 600 rpm for 3 min and then the P3HT-coated sample was baked at 140 ˚C for 10 min in a vacuum oven. Then, 4.8 wt. % PMMA in a mixture of PGMEA and toluene (PGMEA: toluene = 2:8) was spin-coated at 3000 rpm for 1 min on the P3HT layer and the wafer was baked at 90 ˚C for 5 min to remove residue solvents. In order to minimize the dissolution of the P3HT layer during spin-coating the PMMA layer, the mixture of toluene and PGMEA was

used as PMMA solvent instead of pure toluene. After placing the 3D mold on the substrate with dual-polymer layer (figure 21(b)), the substrate and the 3D mold were heated to 180 ˚C and pressed together at a pressure of 2500 psi (figure 21(c)). After 20 min, the mold/substrate assembly was cooled down to room temperature and the 3D mold was released from the substrate (figure 21(d)).

3.2.1.3 Self-aligned metallization

3D PMMA patterns without the residual layer were used as a metal evaporation mask. For the first metal pattern, gold was deposited on the substrate through metal evaporation (figure 21(e)). Because gold is soft, the gold side-wing was not strong enough to endure ultrasonic agitation during a lift-off step as shown in figure 23, in which most gold side-wing structures were lost after ultrasound. To overcome this problem, a chromium layer was additionally deposited on top of the gold layer to increase the durability of the metal side-wing structures (figure 21(f)). However, the additional chromium layer was expected to introduce thin-film stress, which can result in the bending of the metal side-wing structures [75, 76]. In order to find an optimal condition to avoid the metal bending, different combinations of Au-Cr thicknesses (50 nm : 0 nm, 50 nm : 100 nm, and 110 nm : 60 nm) were tested. After depositing gold and chromium with different thicknesses, each sample was immerged in PGMEA and then ultrasonic agitation was applied for 20 sec to lift-off gold (figure 21(g)). After the lift-off step, each sample was investigated through SEM in order to identify the side-wing structures. As the final step of the fabrication process, an aluminum layer of 50 nm thick

was deposited on the substrate with the metal side-wings structures through metal evaporation (figure 21(h)). After completing the aluminum deposition, self-aligned metal patterns on P3HT was investigated by SEM to check the fabrication results.
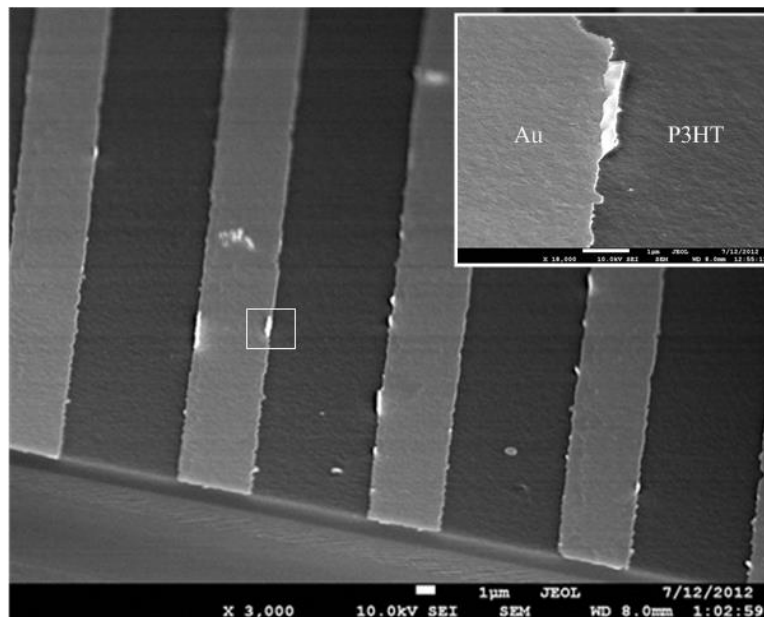
Figure 23. A prospective SEM image of the first metal patterns consisting of only gold. Most side-wing structures of the gold patterns were destroyed by the ultrasonic agitation after the lift-off step.

3.2.2 Self-aligned metallization based on anisotropic side-wings

The concept of anisotropic side-wings was devised to shrink the gap between two different metal patterns into sub-100 nm scale. In order to achieve the anisotropic side-wings, a conformal deposition of polyvinyl acetate (PVA) and following dry etching were adopted as shown in figure 24. In addition, a selective dry etching was required to generate the 3D mold with anisotropic recesses (figure 25).

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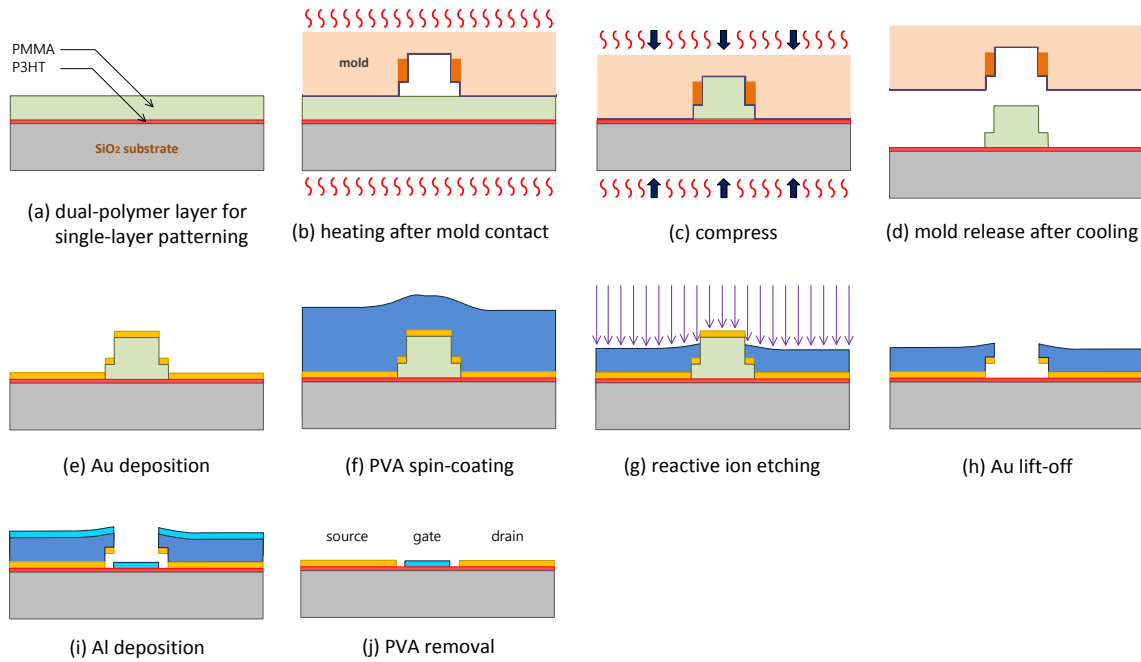
Figure 24. A schematic for the self-aligned metallization process based on anisotropic side-wings (scheme 2). The 3D mold is fabricated by a selective dry etching step.

3.2.2.1 Anisotropic 3D mold fabrication

The key steps in the fabrication of the 3D mold used in scheme 2 were shown in figure 25. First, chromium patterns with 30 nm thickness were formed on silicon oxide substrate through a series of photolithography (figure 25(a)), chromium evaporation (figure 25(b)), and lift-off (figure 25(c)). In order to create an efficient lift-off profile, exposed photoresist (Shipley S1805) was soaked in chlorobenzene for 10 sec and then rinsed in flowing water before photoresist developing [77]. The chromium patterns were transferred to the substrate through a RIE step to create anisotropic silicon oxide trenches (vertical sidewalls) with 280 nm depth (figure 25(d)). After the first dry etching, a silicon nitride layer of 70 nm thick was deposited through plasma-enhanced chemical

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vapor deposition (PECVD) on the sidewalls of the trenches (figure 25(e)). The silicon

nitride layer was then selectively etched by a RIE with O_2 at 20 sccm and CHF_3 at 20

sccm. By exploiting different etching rates for chromium, silicon nitride, and silicon

oxide, recesses with 160 nm height were created (figure 25(f)) [78, 79]. After the

selective dry etching, chromium pattern was removed by dipping in chromium etchant

for 10 min to complete the 3D mold fabrication (figure 25(g)). The surface of the imprint

mold was coated by FDTS monolayer for anti-adhesion purpose (figure 25(h)).
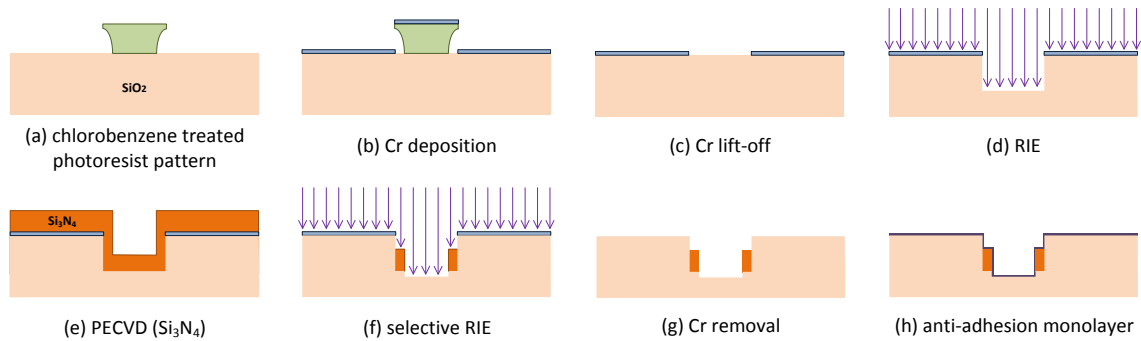
Figure 25. A schematic for the fabrication process for the 3D mold used in scheme 2.
The mold has anisotropic (vertical) recesses.

3.2.2.2 Single-layer PMMA patterning and self-aligned metallization

With the prepared imprint mold, dual-layer thermal nanoimprint for single-layer

patterning was performed on a dual PMMA and P3HT layer following the same

sequence described in section 3.2.1.2. An optimal PMMA thickness was found when 3.6

wt. % PMMA in the mixture of PGMEA and toluene (PGMEA : toluene = 2 : 8) was

spin-coated at 3500 rpm. After the dual-layer thermal nanoimprint (figure 24(d)), 50 nm

gold was deposited on the substrate through metal evaporation (figure 24(e)). Unlike

PMMA patterns with round steps in scheme 1, PMMA patterns with narrow and tall

steps in scheme 2 could not lead to a suspending side-wing through non-conformal metal

deposition due to its steep sidewall. Therefore, it needed a supporting structure to firmly

hold the side-wing. As a simple method to maintain the side-wing structure, 7 wt. %

PVA (molecular weight: 30,000 ~ 70,000, Sigma-Aldrich) in water was spin-coated at

1000 rpm after the gold deposition (figure 24(f)). In order to make openings through

which PGMEA solvent permeates and dissolves PMMA patterns, a RIE step with O_2 at

20 sccm flow rate and 50 W RF power was carried out for 400 sec (figure 24(g)). After

getting the openings, the sample was dipped in PGMEA and then ultrasonic agitation

was applied for 30 sec to facilitate the gold lift-off (figure 24(h)). The second metal

pattern was deposited through aluminum evaporation on the substrate with the PVA

supported side-wings (figure 24(i)). Self-aligned metallization was finally completed by

removing the PVA layer by immersing the sample in water (figure 24(j)). In order to

completely remove the suspending gold residue as well as the PVA supporting structure,

ultrasonic agitation was applied to the substrate for 1 min during aluminum lift-off.

3.3 Results and discussion

Self-aligned metallization on an organic semiconductor can play an important

role in realizing high-performance organic ICs because it can lead to a smaller device

size and minimal device parasitics, both are conducive to achieve faster organic devices,

through the elimination of alignment error. In the self-aligned metallization, it is crucial

to determine the minimum gap size between two metal patterns, which is directly related to pattern resolution. The minimum gap dimension is determined by the suspended side-wing structures of the first metal pattern. The side-wings are morphologically classified into isotropic (scheme 1) and anisotropic (scheme 2) ones as previously described, each achieved by a specific fabrication scheme. While the isotropic side-wings lead to a regular gap in the order of 100 nm, the anisotropic side-wings shows a capability to form sub-100 nm gap between two metal patterns.

3.3.1 Self-aligned metallization based on isotropic side-wings

3.3.1.1 3D imprint mold with isotropic recesses

The combination of wet and dry etching leads to 3D molds with isotropic side-wing structures as shown in figure 26. Due to the nature of wet etching [80], it is difficult to have a uniform undercut surface but the surface roughness is in a tolerable range (< 20 nm) compared to the intended radius of the undercut (155 nm). For a high-resolution multiple metallization, the gap is preferred to be as narrow as possible. The minimum gap is mainly determined after considering the target thickness of the second metal pattern. Because the gap size between the two metal patterns is equal to the depth of the undercut as a consequence of isotropic wet-etching profile, the depth (or the radius) of the undercut should be larger than the thickness of second metal pattern to avoid electrical connection between the two metal patterns, which will result in an unwanted short circuit between the two metal patterns. In this experiment, the undercut with 155 nm radius was created in order to provide 105 nm vertical space and 155 nm lateral gap

between the first metal pattern with side-wings and the second metal pattern with 50 nm thickness. Although there were undercut radius variation and a limitation in reducing the undercut size because of the nature of wet etching, the combination of wet and dry etching in scheme 1 presents an easy way to create a 3D imprint mold.
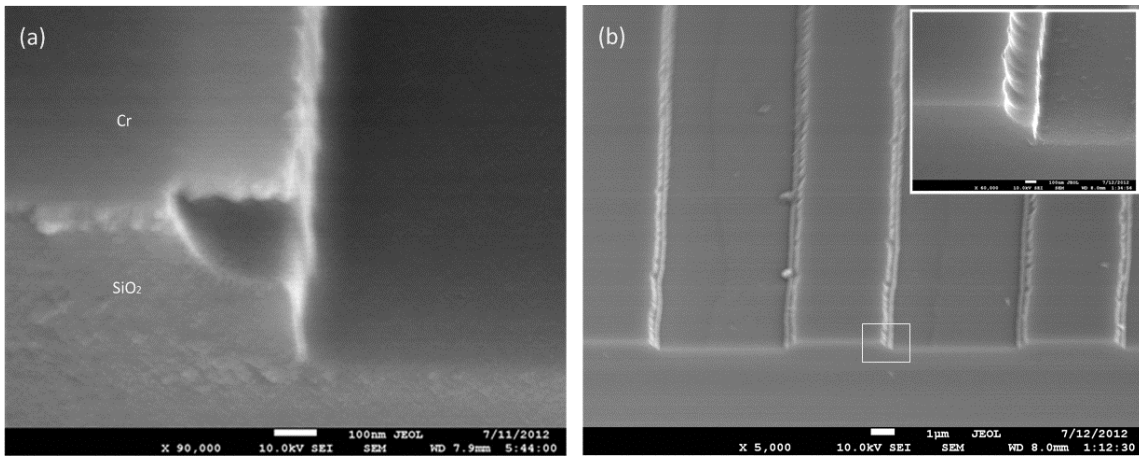
Figure 26. Prospective SEM images of the 3D mold with isotropic undercut structures before (a) and after (b) Cr removal. The undercut radius varies in a tolerable range of 20 nm.

3.3.1.2 3D PMMA patterns on P3HT

After dual-layer thermal nanoimprint with the 3D imprint mold, 3D PMMA patterns were formed on the P3HT layer without a residual layer as shown in figure 27. A noticeable structure was the round step that complied with the shape of the mold undercut. Because of the rounded PMMA footing, it enables conformal metal deposition to ensure the formation of the metal side-wing structures. However, it is inevitable to have relatively thinner metal deposition around the anchor point above the P3HT layer,

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so a structural weakness of the 3D metal pattern is expected at that region. This problem can be addressed by structural reinforcement as described in the following section.
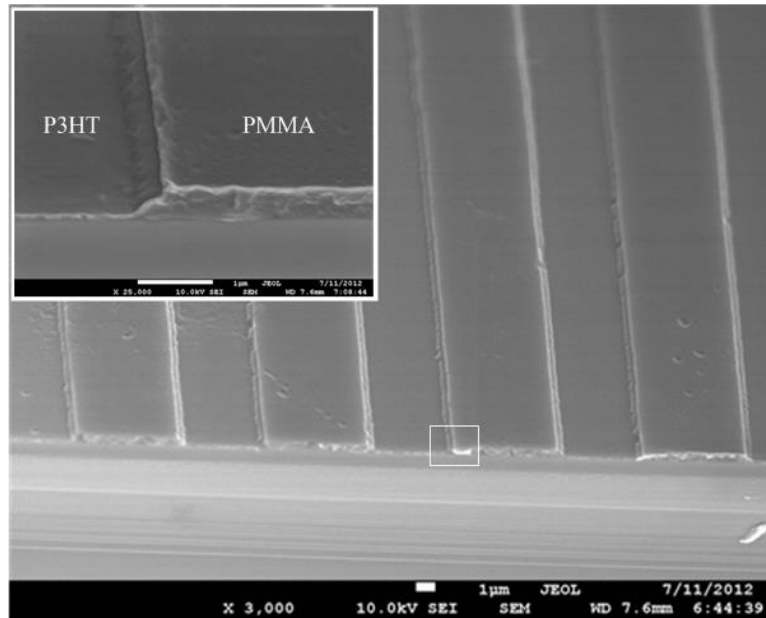
Figure 27. A prospective SEM image of the 3D PMMA patterns with rounded footings after dual-layer thermal nanoimprint.

3.3.1.3 Self-aligned metallization

In order to increase the durability of gold side-wing structures, a chromium film was evaporated after gold evaporation on the PMMA pattern. Although the chromium layer strengthens the side-wings, excessive chromium can lead to undesirable peeling of the metal film from P3HT surface, which eventually widens the gap between the first and second metal patterns as shown in figure 28(a). The metal film peeling is attributed to film stress, which comes from different thermal expansion coefficients between gold and chromium (Au: 14.2×10^{-6}/ ˚C and Cr: 4.9×10^{-6}/ ˚C at 25 ˚C) [81]. The metal film

peeling was managed by adjusting the total film stress through varying the thickness

ratio of gold and chromium. As the thickness of gold increases and that of chromium

decreases, the metal film peeling was gradually suppressed. Finally, the desired side-

wings were achieved with the combination of 110 nm gold and 60 nm chromium. As

shown in figure 28(b), the issue of metal film peeling was completely resolved and the

shape of side-wings complied with the rounded footing of the imprinted 3D PMMA

patterns.
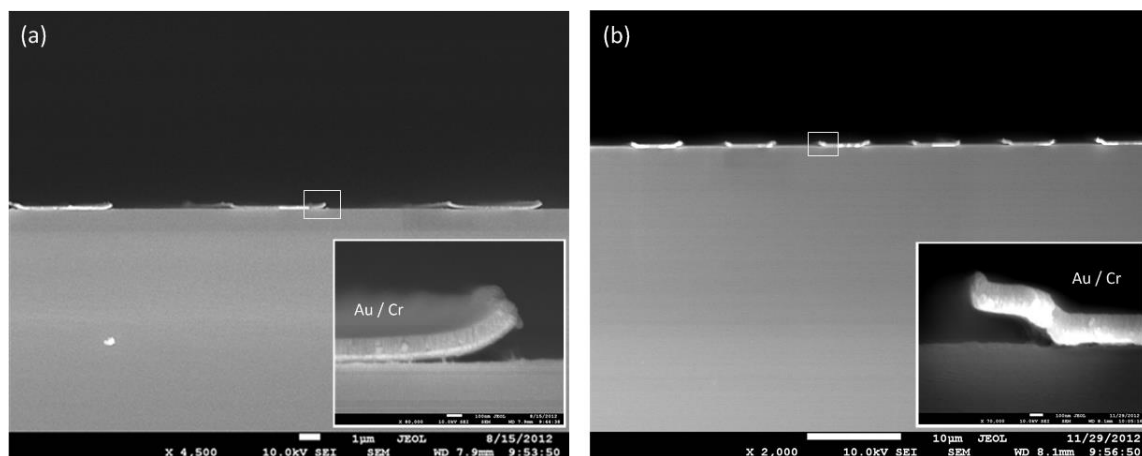
Figure 28. Cross-sectional SEM images of the first metal pattern. The side-wing shapes are affected by the Au/Cr ratio. (a): 50 nm Au / 100 nm Cr and (b): 110 nm Au / 60 nm Cr. In (a), the high compressive stress resulted from thick Cr layer led to the peeling of Au/Cr film from P3HT surface.

Due to structural reinforcement by the chromium layer, the metal side-wing

structures were obtained after lift-off in solvent, as shown in figure 29(a). The side-

wings play a key role in aligning the second metal (Al) pattern with a fixed gap from the

first metal pattern. As shown in figure 29(b), evaporated aluminum was successfully

deposited on the P3HT layer with the initial Au/Cr layer serving as the evaporation mask. Although the evaporated aluminum was also deposited on top of the first metal pattern, it does not cause deformation of the side-wings so that the vertical gap between two metal patterns was also safely secured. In OMESFET application, the aluminum layer on top of the Au/Cr layer will not affect the device operation.
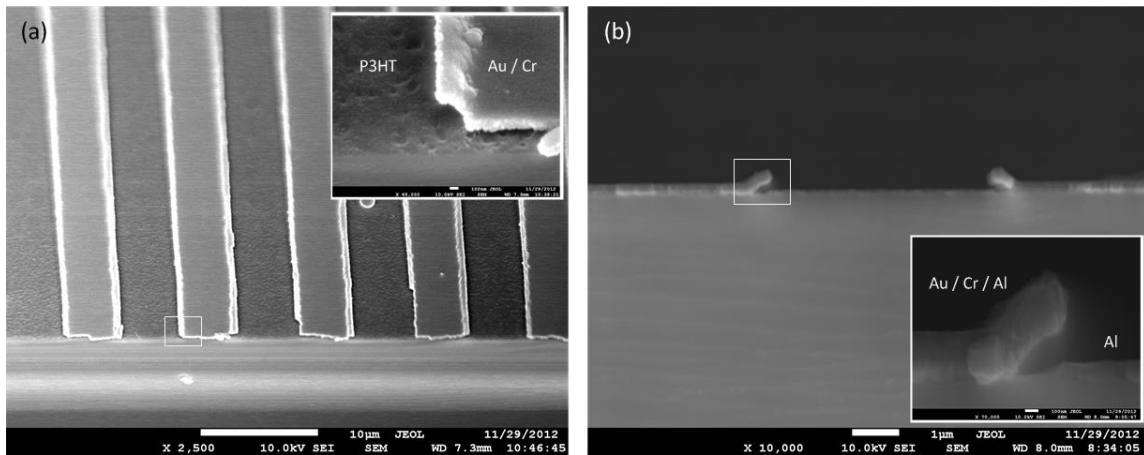
Figure 29. SEM images of metal patterns: (a) a prospective image of the first Au/Cr pattern with curved side-wings; and (b) a cross-sectional image of the self-aligned metal patterns.

3.3.2 Self-aligned metallization based on anisotropic side-wings

3.3.2.1 3D nanoimprint mold with anisotropic recesses

In the RIE step for the 3D mold fabrication, it is important to use a hard mask such as chromium to achieve vertical sidewalls in mold protrusions. In addition, the hard mask protects the flat and smooth surface of the mold protrusion which is a critical factor in dual-layer thermal nanoimprint to avoid unwanted residues that may be trapped in rough spots on the protrusion surface. Therefore, the chromium mask should be

maintained until the selective dry etching. However, the chromium mask pattern

obtained from a lift-off process with positive tone photoresist usually has edge juts

(figure 30(a)), which negatively impacts the fabrication process described in figure 25.

In the extreme case, the PECVD silicon nitride layer, which is to be coated on the

sidewalls of the mold protrusions and intended to form the mold recess, unwantedly juts

out as shown in figure 30(b). The edge protrusion of the chromium pattern can be

eliminated by a photoresist treatment with chlorobenzene during the photolithography

step. Because the treated photoresist had a reentered profile that was conducive to the

lift-off process (figure 31(a)), it eventually produced the chromium pattern as shown in

figure 31 (b).
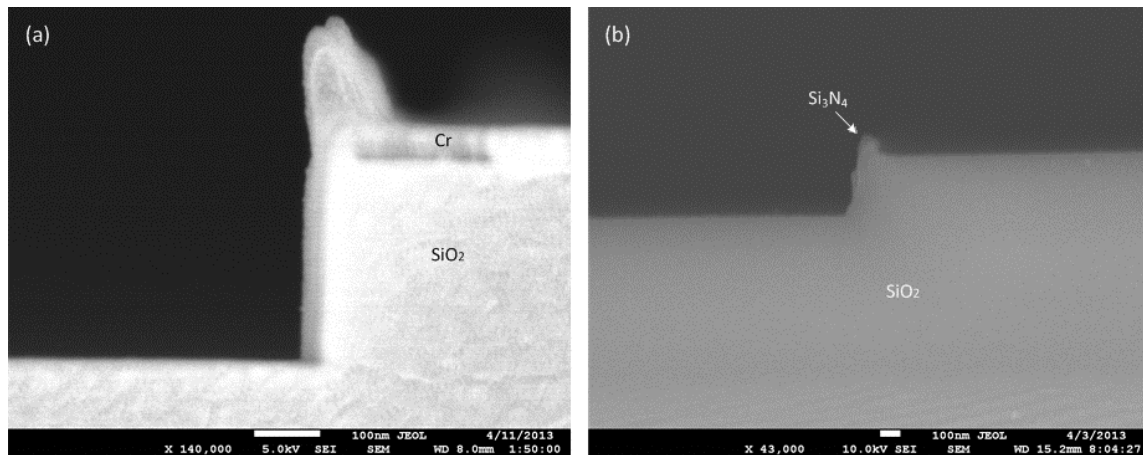
Figure 30. Cross-sectional SEM images that show the chromium mask layer with an edge jut (a) and an undesired silicon nitride protrusion (b). The edge protrusion negatively affected the PECVD deposition of silicon nitride and subsequent selective dry etching. Eventually it led to the silicon nitride protrusion after chromium removal.
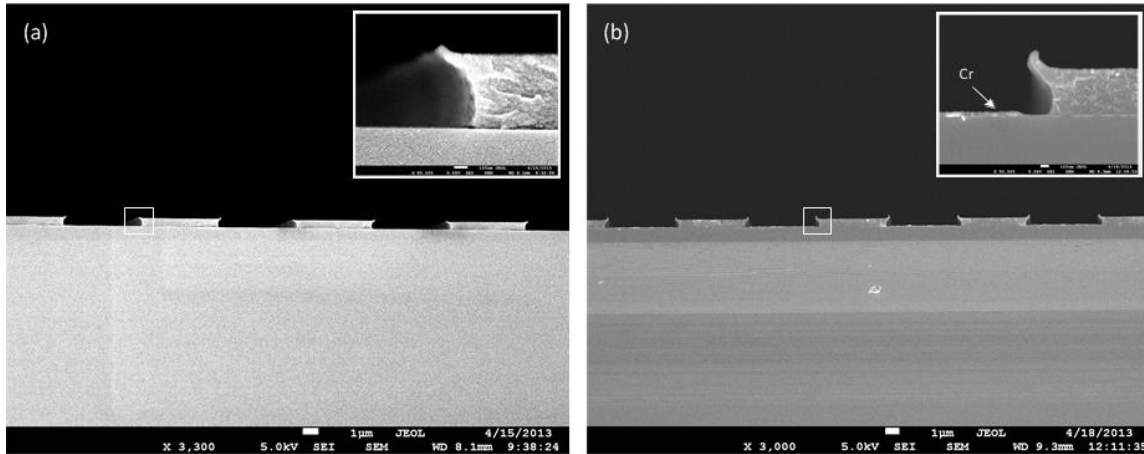
Figure 31. Cross-sectional SEM images of (a) chlorobenzene-treated photoresist pattern and (b) chromium pattern without an edge jut.

The pattern defined by the chromium mask with smooth edge was transferred into the silicon oxide substrate in the depth of 280 nm through the first dry etching (figure 32(a)). After forming the main trenches, silicon nitride was deposited through PECVD. The PECVD process showed a deposition rate ratio of 7:10 on vertical and horizontal surfaces. Therefore, 70 nm silicon nitride was deposited on the sidewall of the etched trench while 100 nm silicon nitride was deposited on the top surface of the chromium mask patterns and the bottom surface of the etched trenches (figure 32(b)). In order to have 120 nm tall recesses, silicon nitride on the sidewall was etched by 250 nm in the vertical direction. Because silicon nitride was etched 1.5 times faster than silicon oxide during the selective dry etching, silicon oxide on the bottom surface of the trenches was also etched by 100 nm after silicon nitride on the bottom surface was etched away. After removing the chromium patterns, the main trench of the mold was

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380 nm deep and the sidewall recesses had a height and width of 120 nm and 70 nm,

respectively, as shown in figure 32(c).
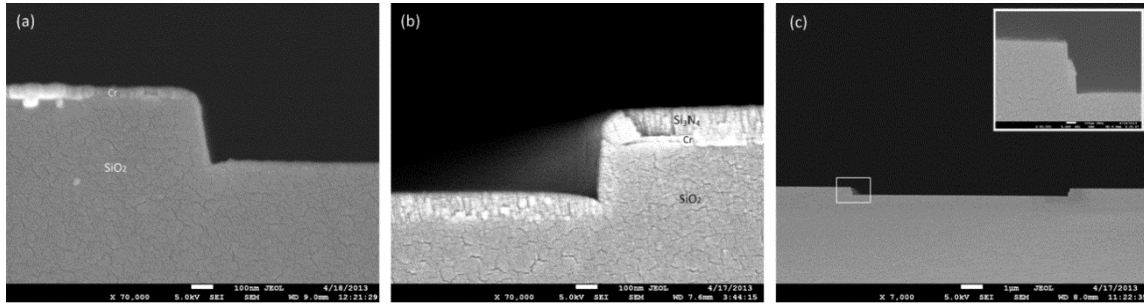
Figure 32. Cross-sectional SEM images that show the sequence of 3D mold generation: (a) initial trench after the first dry etching, (b) silicon nitride deposited by PECVD, and (c) 3D imprint mold with anisotropic recesses on sidewalls after selective dry etching of silicon nitride and chromium removal.

3.3.2.2 Self-aligned metallization

Through dual-layer thermal nanoimprint for single-layer patterning, 3D PMMA

patterns were formed on the P3HT layer. As shown in figure 33(a), the PMMA patterns

were tall with a narrow step on the sidewall. Unlike a round step, such an anisotropic

structure would result in non-conformal coverage of gold film when deposited by highly

directional evaporation technique. Therefore, a suspended side-wing was not realized

after the first metal deposition so that additional steps were required. The desired side-

wing structures can be formed through a spin-coated PVA film and a following dry

etching (figures 24(f) and (g)). As shown in figure 33(b), the spin-coated PVA film

covered the whole surface of the sample, with a relatively thinner PVA film formed

around the edge of the protrusion and a thicker PVA film inside the trenches. Therefore,

the subsequent dry etching made an opening in the PVA film on the PMMA sidewall near the edge while the PVA film still covered the PMMA at the lower step (figure 24(g)). Consequently, the gold lift-off was possible because PGMEA can permeate through the openings. Although a dry etching was applied over the sample, oxygen plasma was completely shielded by multiple layers of PMMA, gold, and PVA on the P3HT layer so that the dry etching did not damage the organic semiconductor layer. As shown in figure 33(c), the lift-off was completed as intended and the PVA film showed a strong adhesion on gold patterns so that it endured the ultrasonic agitation during the lift-off process without peeling-off. In addition, the anisotropic side-wings supported by the PVA film were also successfully formed. After the second metal deposition and the PVA film removal, self-aligned metallization was completed with a narrow lateral gap. As shown in figure 33(d), 60 nm gap was regularly kept between the aluminum and gold patterns on the P3HT layer. This gap is about 10 nm narrower than the 70 nm width of the step recess on the sidewalls of the 3D mold. It is assumed the process variations in lithography, thin-film deposition and etching contributed to this difference.
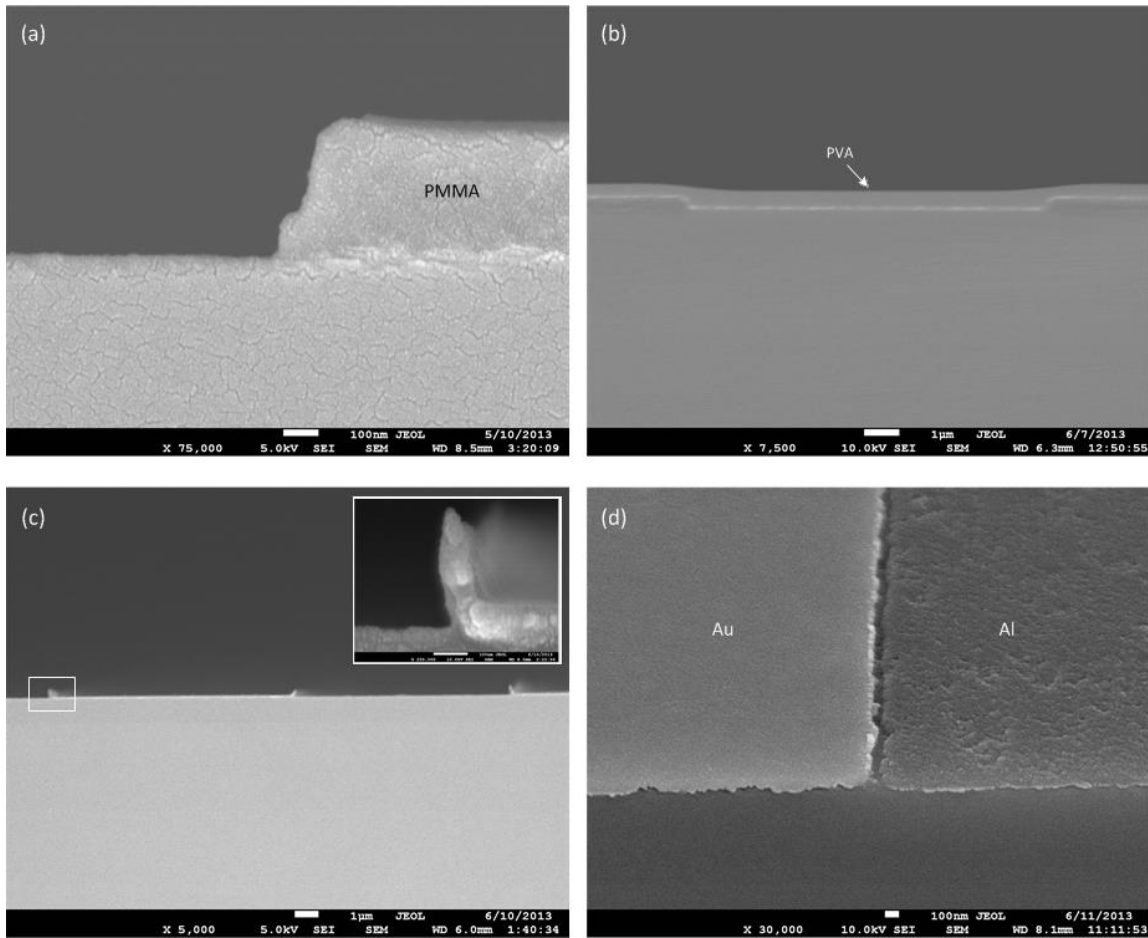
Figure 33. SEM images for the key steps of self-aligned metallization from an anisotropic side-wing: (a) 3D PMMA pattern on P3HT, (b) PVA film spin-coated after gold deposition, (c) anisotropic side-wing supported by PVA after gold lift-off, and (d) gold and aluminum patterns on P3HT with 60 nm gap after aluminum deposition and PVA removal.

3.3.3 Applications of self-aligned metallization on organic semiconductors

The self-aligned metallization techniques presented in this work can be utilized

in the fabrication of OMESFETs. In order to implement a functional OMESFET, two

different types of metal-organic semiconductor contacts, namely rectifying and ohmic

contacts, are required [82]. The rectifying contact works as the gate electrode and the

ohmic contact works as the source and drain electrodes. The contact type is determined according to the work function of a metal relative to the HOMO level and the LUMO level of the organic semiconductor [83]. Given the organic semiconductor of P3HT, aluminum forms a Schottky barrier because the work function of aluminum (4.2 eV) locates between the HOMO level (5.02 eV) and the LUMO level (2.83 eV) of P3HT. Therefore, rectifying contact is formed between P3HT and aluminum. Meanwhile, gold can be utilized for source and drain contacts because its work function (5.1 eV) is higher than the HOMO level of P3HT. Thus, an ohmic contact is formed between the p-type P3HT and gold. In this work, we demonstrate that the self-aligned metallization techniques have the capability to pattern the two types of contacts on an organic active layer.

For optimal device performance, the separation (or gap) between the source/drain and the gate contacts should be as small as possible in order to reduce parasitic resistance between source/drain and gate. The self-aligned metallization techniques have clear advantage over the shadow masking technique because we can make a gap in the order of 100 nm or even sub-100 nm. This will significantly reduce the parasitic resistance in OMESFET and lead to device performance improvement. Furthermore, the channel length of the OMESFET can be also scaled down to the nanoscale because the metal lines are patterned by the dual-layer thermal nanoimprint technique, which is well known to have nanoscale patterning resolution [71]. Finally, another important advantage is its ability to form a top-contact on organic semiconductor, which normally results in a higher mobility of organic semiconductor than a bottom-contact [84, 85].

Therefore, the self-aligned metallization techniques provide an effective fabrication route for high-performance top-contact OMESFET with nanoscale dimensions for advanced organic IC applications.

3.4 Summary

Self-aligned metallization based on a side-wing structure was developed and investigated in this work. The 3D dual-layer thermal nanoimprint was used as the lithography process to effectively create the suspending side-wing structures from the first metal pattern. With the side-wing structures serving as the evaporation mask for the second metal pattern, the metallization technique successfully formed self-aligned gold and aluminum lines on P3HT with a narrow gap. Two techniques were employed in this work to fabricate the 3D nanoimprint molds. The mold in scheme 1 was fabricated by a combination of dry and wet etching, and it was used to fabricate isotropic metal side-wings; the mold in scheme 2 was fabricated by a series of thin-film deposition and selective dry etching, and it was used to fabricate anisotropic metal side-wings. The isotropic side-wing in scheme 1 was easy to fabricate and it showed a capability to form a gap on the order of 100 nm between the two metal patterns. However, it was difficult to realize a sub-100 nm gap from the self-aligned metallization based on the isotropic side-wings. On the other hand, the width of the anisotropic side-wing can be reduced to below 100 nm. As a result, a 60 nm gap was achieved from the self-aligned metallization based on the anisotropic side-wing in scheme 2, although at a cost of increased process complexity. Because such aligned metal patterns on P3HT lead to a rectifying contact

between two ohmic contacts, this self-aligned metallization can be utilized to fabricate

high-resolution top-contact OMESFETs for high-performance organic device and circuit

applications.

CHAPTER IV

ORGANIC METAL SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

FABRICATED THROUGH 3D THERMAL NANOIMPRINT BASED SELF-

ALIGNED METALLIZATION

4.1 Introduction

Organic electronics have been gradually immersed into our everyday life with novel properties and unique advantages [86, 87]. For example, flexible and transparent organic display has already started to create a new lifestyle never before experienced with inorganic display. In addition, cost-effective organic electronics are highly competitive in large-area or ubiquitous applications such as solar cells and radio-frequency identification chips [86]. However, their chronic poor-performance critically impedes their application expansion into high-tech electronics whose core parts are mostly implemented in the form of ICs. In order to overcome the hurdle, it is essentially required to improve the performance of organic field-effect transistors (OFETs) – the fundamental components of organic ICs.

While carrier mobility of OFETs has been continuously improved through newly synthesized organic semiconductors and doping level increase [15, 88], channel lengths of OFETs still remain in micron scale because of the lack of high resolution lithography technique that can be safely applied to organic semiconductor. Furthermore, the simple structures of conventional OFETs inherently involve negative factors (figures 34(a) and (b)), large parasitic capacitance and resistance, that directly degrade their performance

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[89]. Consequently, their performance still falls far behind that of inorganic transistors. In order to effectively increase their performance, it is indispensable to resolve the structural weaknesses. One potential solution is a MESFET-like structure that completely eliminates the overlap capacitance and efficiently minimizes the parasitic residence as shown in figure 34(c).

Several OMESFETs were already reported to eliminate a low-quality gate insulator that was regarded as one of main performance degradation factors in OFETs [82, 83, 90]. However, their structures still stuck to the simple structure of conventional OFETs in which it was required to have a large overlap between electrodes in order to compensate misalignment errors. Because low-resolution lithography techniques have been commonly used for organic semiconductor devices, it has been regarded as a quite difficult challenge to shrink the large overlap area. Therefore, the performance of those OMESFETs was still restricted by the large overlap capacitance unlike inorganic MESFETs whose all electrodes were patterned side by side with a small gap. To fully exploit the structural advantages as inorganic MESFETs, it is imperative to change the strategy in patterning the electrodes of OMESFETs.

As a novel way to remove the parasitic overlap capacitance as well as the poor gate insulator from OFETs, we demonstrate a full bottom-contact type of OMESFET with a self-aligned gate electrode in this paper. As an alternative of a gate insulator, an aluminum gate under P3HT is used to form a rectifying contact which efficiently suppresses gate current in the device. The aluminum gate is patterned without overlap to source and drain electrodes while keeping a regular 30 nm gap. Such non-overlapped

electrode patterns are realized through self-aligned metallization based on three-dimensional thermal nanoimprint. Unlike conventional OFETs whose semiconductor layer is normally sandwiched by electrodes, all electrodes are placed on the bottom side of organic semiconductor so that it ultimately removes overlap capacitance from the device. Although a channel length in microscale is examined in this experiment, there is a substantial potential to shrink the channel length into nanoscale so that a nanoscale OMESFET can be achieved because the suggested metal patterning approach is based on nanoimprint lithography which has sub-10 nm patterning capability [91].

source	drain		gate		source	gate	drain
semiconductor			insulator		semiconductor		
insulator			semiconductor				
gate/substrate			source	drain	substrate		
			substrate				
(a) bottom gate type			(b) top gate type		(c) MESFET-like structure		
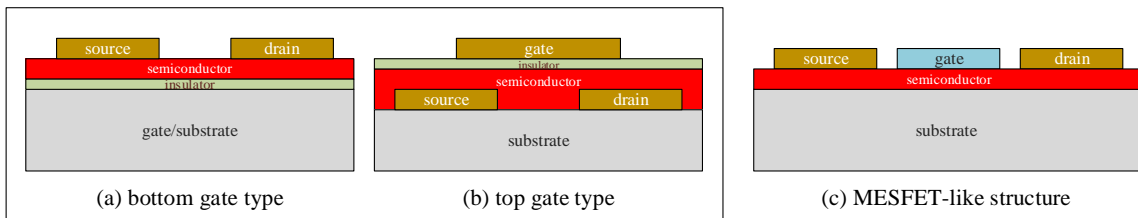
Figure 34. Cross-sectional views of OFETs. While traditional structures (a, b) includes large overlaps, the suggested MESFET-like structure (c) eliminates the overlap as well as gate insulator.

4.2 Experimental methods

4.2.1 Nanoimprint-aware layout

In order to form 3D resist patterns and have a nanoscale patterning capability, 3D thermal nanoimprint was chosen for the lithography technique. Due to the nature of the thermal nanoimprint, it is important to keep a uniform pattern density [92]. The uniformity can be achieved through dummy patterns that also facilitate the resist filling into a mold cavity during an imprinting. Therefore, it is required to reflect dummy

patterns from a layout step. As shown in figure 35, dummy patterns were applied to intended patterns as well as the other non-pattern area in a different way. Regular dummy holes in the pattern of source and drain were exploited to create separate spaces into which squeezed resist evenly moved during an imprinting process. On the other hand, isolate dummy patterns in the non-pattern area would prevent unwanted random dewetting of resist so that the resist pattern covered a large area without disconnection. The connected resist pattern was supposed to define the gate electrode and the channel of an OMESFET.
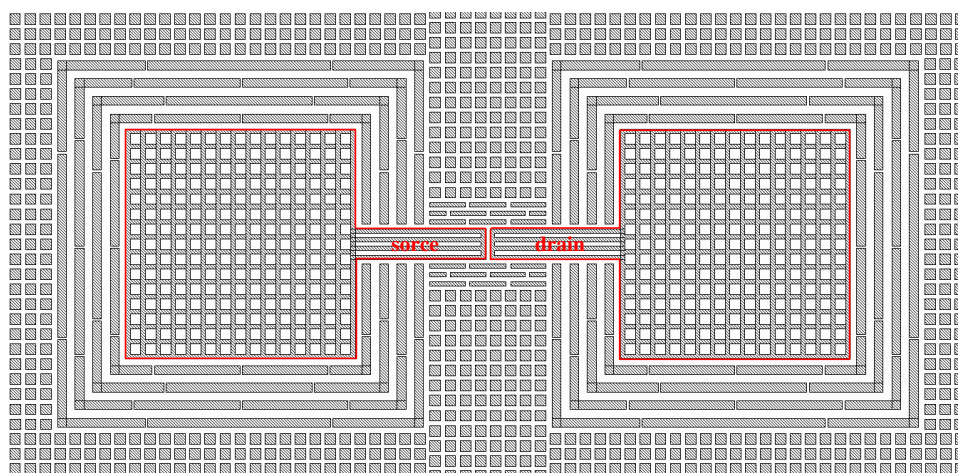
Figure 35. A nanoimprint-aware layout defining source and drain. Dummy patterns are utilized in undefined area as well as defined area to keep a uniform pattern density.

4.2.2 Fabrication of OMESFET

Before performing the fabrication process shown in figure 37, a 3D thermal nanoimprint mold with anisotropic recesses was prepared following patterns that were defined through the nanoimprint-aware layout. The mold was intended to form an

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OMESFET with the channel length of 5 μm and the channel width of 35 μm. The depth

of the mold trench was 380 nm. The mold had anisotropic shoulder on the sidewalls of

mold protrusions as shown in figure 36. The shoulder height was 200 nm and its width

was 40 nm. A selective dry etching was applied to carve the anisotropic 3D sidewall [73].
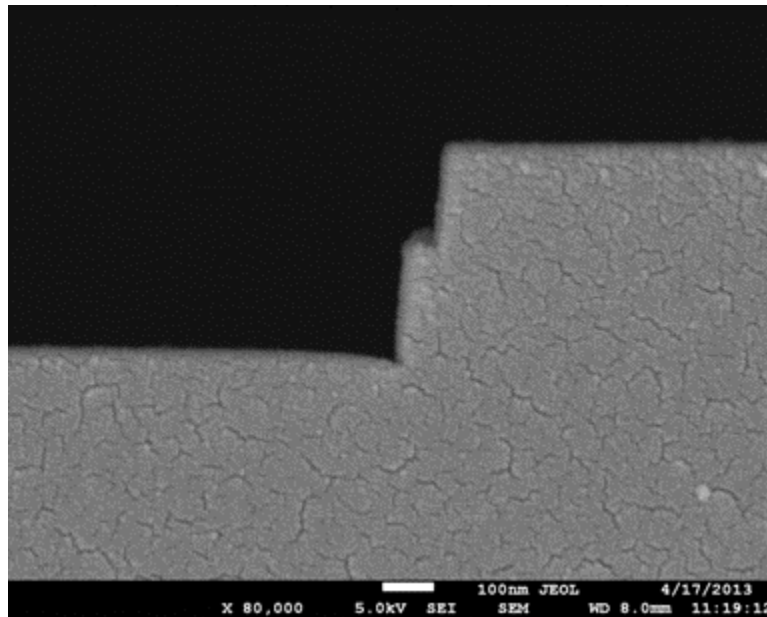
Figure 36. A cross-sectional SEM image of the 3D nanoimprint mold with an anisotropic shoulder on its sidewall

In order to form self-aligned metal patterns on a silicon oxide substrate for

electrodes of an OMESFET, 3D resist structure was utilized as a metal deposition mask.

The 3D resist structure was formed through thermal nanoimprint lithography that used

the 3D mold. The 3D thermal nanoimprint was performed on 200 nm Teflon (AF1600,

DuPont) layer that was spin-coated on the silicon oxide substrate. Applied imprinting

condition was that the temperature was 210 ˚C, the pressure was 2500 psi, and the

annealing time was 10 min. After the 3D thermal nanoimprint, residue layer was removed by a reactive ion etching (RIE) with 20 sccm oxygen and 50W RF power for 30 sec.

After completing the 3D Teflon patterns, 5 nm chromium and 50 nm gold were deposited in sequence through E-beam evaporation for source and drain electrodes. The chromium layer was used as a seed layer for the gold deposition. Before depositing aluminum for a gate electrode, it was needed to make self-aligned mask patterns that not only block the second metal deposition on the first metal patterns, but also formed side-wing structure that would provide a regular gap between gate and source/drain. In order to form the self-aligned mask patterns, 7 wt. % PVA in water was additionally spin-coated at 1000 rpm for 1 min and then openings of the PVA film near upper sidewalls were created through a RIE with 20 sccm oxygen and the 50 W RF power for 8 min. To complete the first metal patterns with the self-aligned mask, the sample was dipped in Fluorinert electronic liquid (FC-72, 3M) that dissolved only the Teflon layer and an ultrasonic agitation was simultaneously applied for 30 sec to accelerate the lift-off.

As a metal for gate electrode, 50 nm aluminum was deposited through E-beam evaporation after depositing a 5 nm chromium seed layer. After the aluminum deposition, aluminum over the first metal patterns was removed through a lift-off in water that dissolved the PVA layer. In addition, a long ultrasonic agitation for 3 min was simultaneously applied to completely remove feeble side-wing structures that were no more supported by the PVA layer. After patterning all electrodes on the silicon oxide substrate, the surface of the sample was dry-etched with 20 sccm oxygen and 50 W RF

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power for 5 sec in order to remove organic residue and change the surface characteristic from hydrophobic to hydrophilic [93]. After making the surface hydrophilic, P3HT in 1,2-dichlorobenzene (10 mg/ml) was spin-coated on the surface at 400 rpm for 3 min for an organic semiconductor layer (~ 80 nm). In order to prevent oxidation of P3HT, the sample was coated by a thin Teflon film.
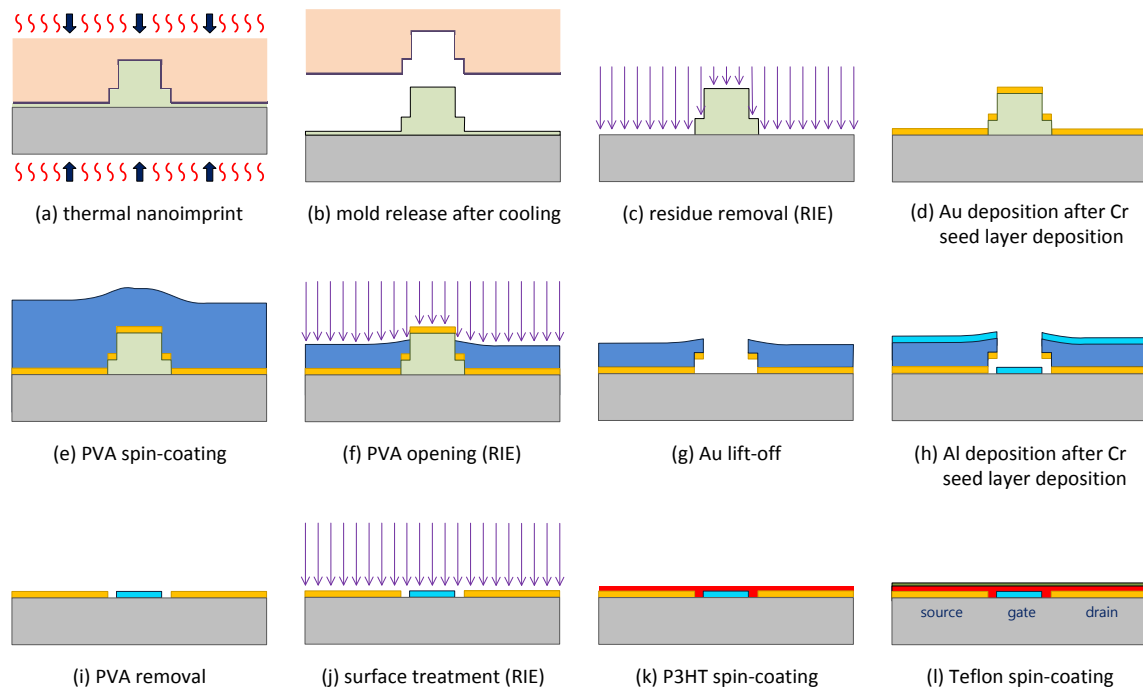
Figure 37. A schematic for the fabrication process of a full bottom contact type OMESFET with self-aligned electrodes. The anisotropic side-wing defines the regular gap between gate and source/drain.

4.2.3 Electrical characteristics

After preparing the OMESFET, the DC electrical characteristics of the device were measured at room temperature by using a HP 4145B semiconductor parameter analyzer and a micromanipulator. In order to confirm a rectifying contact between aluminum and P3HT, gate was biased by a sweeping voltage in the range of 5 V to -10 V and the gate current was measured while its corresponding source was grounded. After verifying that gate current was blocked in the reverse bias regime, each device was measured in terms of its output characteristic and transfer characteristic. In order to observe output characteristic, drain current was measured while drain voltage was swept from 0 V to -6 V and source was grounded. The output characteristic was measured at different gate biases between -1 V and 1 V. For a transfer characteristic measurement, gate voltage was swept from 3 V to -1.5 V at the drain voltage of -6 V while source was grounded.

4.3 Results and discussion

OFETs have been traditionally fabricated with large overlap between electrodes. In addition, the rough surface of organic semiconductor leads to low quality of gate insulator. Such structural weakness is innovatively overcome through OMESFET with self-aligned electrodes. The self-alignment through 3D side-wing structure achieves a nanoscale separation between the electrodes so that it minimizes parasitic resistance as well as parasitic capacitance. Additionally, a potential barrier appearing at the aluminum and P3HT interface effectively blocks the gate current under reverse bias

without the poor insulator. Such a Schottky barrier enables the device to operate in depletion mode.

4.3.1 Configuration

As explained in the equation 4 [44], parasitic capacitance and resistance as well as channel length have a significant effect on the cut-off frequency (f_T) of an OMESFET device that is regarded as one of important performance measurements.

$$f_T = \frac{g_m}{2\pi \left[C_G \left(1 + \frac{R_D + R_S}{R_{DS}} \right) + C_{GD} g_m (R_D + R_S) + C_{par} \right]} \qquad \text{[Eq. 4]}$$

where g_m is transconductance, R_S, R_D, and R_{DS} are source, drain and source-drain resistances, and C_G, C_{GD}, and C_{par} are gate, gate-drain, and parasitic capacitances. Self-aligned metallization through the 3D nanoimprint provides an effective way to reduce the parasitic capacitance and resistance. Although the nanoimprint-based lithography has a potential to realize a nanoscale channel length, this experiment focuses on achieving small parasitic capacitance and resistance through a structural improvement based on the self-aligned metallization.

Conventional OMESFET structures have a limitation in reducing the parasitic capacitance due to inevitable large overlaps that result from multiple alignment processes for electrode patterning with low resolution. However, the self-aligned metallization adopted in this experiment removes the need of the multiple alignments so

that the large overlap between electrodes is completely eliminated. As a result, the

overlap capacitance no longer exists in the OMESFET with the self-aligned electrodes.

Furthermore, the self-aligned metallization shows a remarkable capability to reduce the

parasitic resistance that is proportional to the separation length between gate and

source/drain. The regular gap in the order of 30 nm is achieved in this experiment as

shown in figure 38(b). Although the minimum gap size is partially limited by metal

deposition variation in a lateral direction, it is mostly determined by the width of the

anisotropic side-wing structure of the first metal patterns (figure 38(a)). Because there is

no critical restriction in reducing the width of the side-wing, the gap size can be shrunk

into a deeper submicron range so that the effect of the parasitic resistance can be reduced

into the ignorable level. After patterning the self-aligned electrodes, organic

semiconductor channel is simply formed through spin-coating of P3HT.
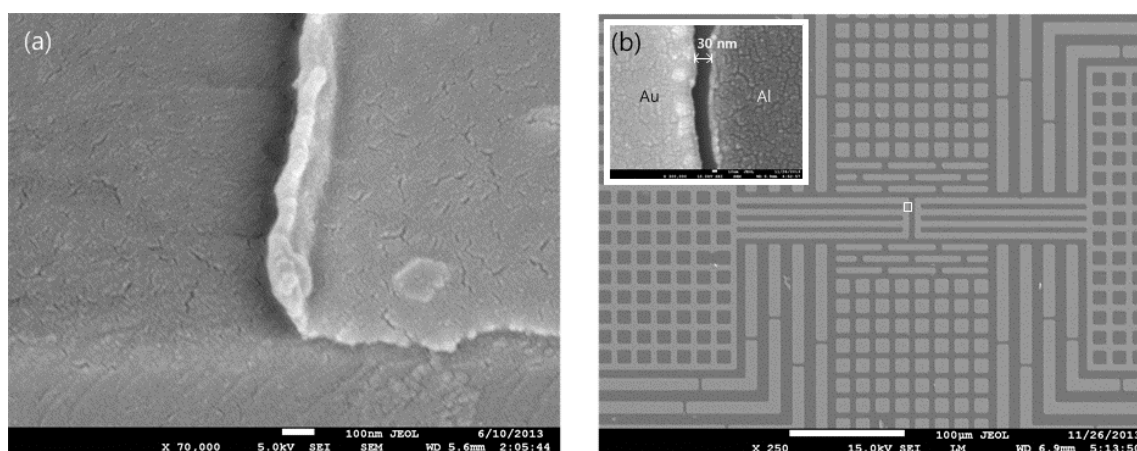
Figure 38. SEM images of metal patterns. The anisotropic side-wing of the first metal pattern is utilized as a self-align mask (a: prospective view) and 30 nm gap between electrodes is achieved after completing the self-aligned metallization (b: top view)

Because there is no insulating layer in the OMESFET, a rectifying contact is essential to block current flow from gate. In order to check the rectifying behavior, current flow across a Schottky diode that is parasitically formed between gate and source is measured as the function of gate-source voltage (V_{gs}). As shown in figure 39(a), gate current is restricted below 20 nA when a reverse bias is applied in the range of 5 V. On the other hand, a forward bias rapidly increases gate current so that current at the V_{gs} of -3V is ~10^2 times larger than current at the V_{gs} of 3V. In addition, the breakdown of the device was observed when the forward bias was increased further (figure 39(b)).
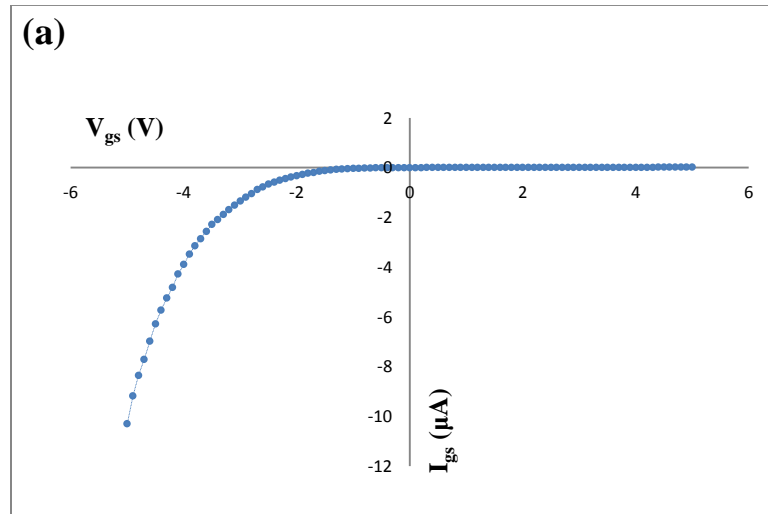
Figure 39. Rectifying characteristic (a) and break-down phenomenon (b) in the OMESFET measured from a gate-source biasing
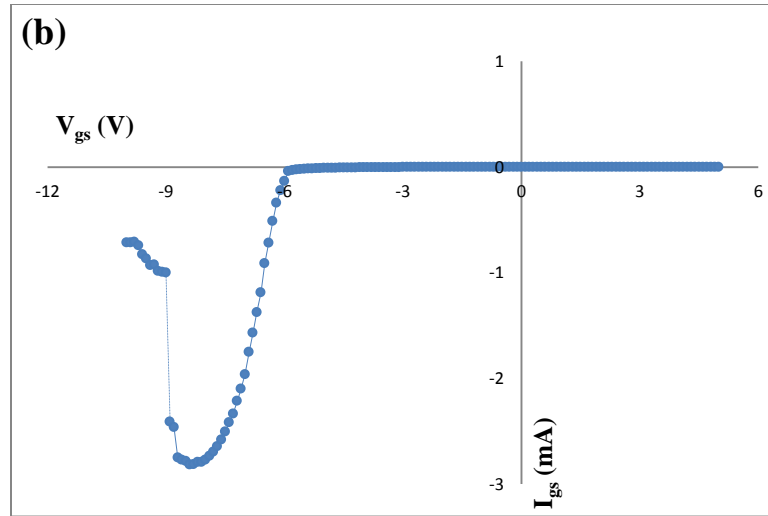
Figure 39. continued.

The rectifying behavior is explained from a relative energy level relation. The Fermi level of aluminum is higher than the HOMO level of P3HT by 0.82 eV [94, 95]. Due to the energy level difference, the potential barrier of 0.82 eV is initially formed at the junction of aluminum and P3HT. When a reverse bias is applied, the potential barrier can raise so that it retards hole-carrier diffusion from P3HT to aluminum. In spite of the rectifying effect, there exists considerable gate reverse leakage in the order of 10 nA in this experiment. The reverse leakage can be reduced by several orders of magnitude through additional surface treatments [96, 97]. However, we have not achieved satisfactory reverse leakage reduction due to our experiment environment limitation.

4.3.3 Electrical characteristics

The rapid increase of gate current at a forward bias restricts the operation mode of the OMESFET. Therefore, the device operates only in depletion mode under reverse

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bias so that current channel is directly controlled by the depletion layer thickness. From the plots of transfer characteristics of the device (figure 40(a)), it is inferred that the current channel is fully depleted around the reverse gate-source bias of 1V so that the device becomes off. Therefore, the device can operate in small gate-source bias range between 0V and 1V. In the limited gate-source bias range, on-current (-44.2 nA) at the Vgs of 0 V is only 4.3 times larger than off-current (-10.2 nA). The small on-off current ratio can be improved through the reduction of off-current that mostly comes from gate reverse leakage. Given the I_{ds}-V_{gs} curve, the transconductance (g_m) of 9.6×10^{-8} S is extracted and the saturation swing of 1.22 V/decade is observed. In addition, the plot of output characteristics of the device (figure 40(b)) shows linear region and saturation region of the device. As shown in the plot, the output conductance (g_o) of the device in linear regime reduces as positive gate-source bias increases and it eventually drops down to a quite low level (3.1×10^{-10} S) when the V_{gs} of 1 V is applied. As the amplitude of the negative drain voltage increases, the device behavior changes from linear resistive behavior to saturated one so that its operation follows the fundamental mechanism of a p-type field effect transistor (FET).
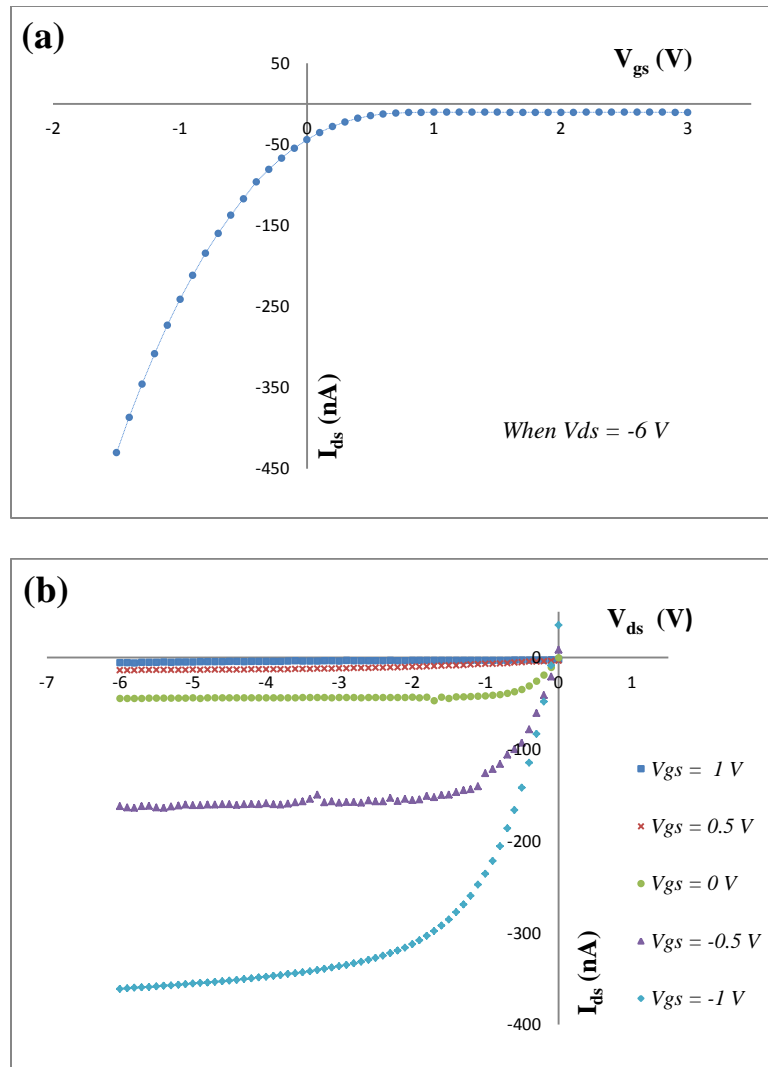
Figure 40. Transfer (a) and output (b) characteristics of the OMESFET

4.4 Summary

The full bottom-contact type OMESFET is fabricated and its DC electrical characteristics are investigated in this work. The self-aligned electrodes of the device effectively overcome the structural weakness of traditional OFETs that inherently induces a large overlap capacitance. In addition, the 30 nm gap between the aligned

electrodes is achieved harnessing the anisotropic side-wing masks. As a result, parasitic resistance is expected to be substantially reduced because it is proportional to the gap size which is otherwise formed in a micron dimension with traditional patterning techniques for organic semiconductor devices. The other advantage of the suggested fabrication is the removal of gate insulator that has been regarded as one of main performance degradation factors of OFETs. Schottky barrier formed between aluminum gate and P3HT channel blocks gate current in the reverse bias regime so that it efficiently substitutes for the poor insulating layer. The measured transfer and output characteristics show that the device operates as the p-type depletion mode OMESFET in the small operation voltage range (0V ~ 1V). Although on/off current ratio is quite low, it can be improved through additional surface treatments. As proven in this work, the fabrication process based on the self-aligned metallization provides a practical method to realize an OMESFET with minimal parasitic capacitance and resistance that has been regarded as a challenging task in traditional OFETs.

CHAPTER V

CONCLUSION

High-resolution patterning of metal structures on organic semiconductors is important to the realization of high-performance organic transistors for organic integrated circuit applications. However, traditional shadow masking and printing techniques have limited resolutions, precluding submicron metal structures on organic semiconductors. Accordingly, the channel length of organic transistors, which directly affects transistor performance, is still in microscale while an inorganic transistor achieved deep-submicron channel length a couple of decades ago. Thus, traditional organic transistors have not benefitted from scaling into deep submicron region to improve their performance.

In order to make a breakthrough that can safely pattern nanoscale metal structures on an organic semiconductor layer, the novel dual-layer thermal nanoimprint technique is devised in this work. Depending on mold depth, pattern size, and polymer layer thickness, the dual-layer thermal nanoimprint can yield two different patterning results—single-layer patterning and double-layer patterning. The single-layer patterning is successfully performed with a delicate PMMA volume control and a very thin P3HT layer. Double-layer patterning is achieved when a thick and smooth P3HT layer is formed under a thin PMMA layer. Based on the mixing temperature as well as the glass transition temperatures of both polymers, the optimal nanoimprint temperature range is determined for dual-layer thermal nanoimprint. Because the pattern definition is

completed without a dry etching step, this patterning technique can be applied to organic functional materials whose electrical properties can be critically degraded when exposed to oxygen dry etching in conventional thermal nanoimprint.

Furthermore, the application of the dual-layer thermal nanoimprint is expanded from two-dimension to three-dimension to achieve an efficient multiple-level metallization on P3HT with a deep-submicron lateral gap. By using a 3D nanoimprint mold in a dual-layer thermal nanoimprint process, self-aligned two-level metallization on P3HT is efficiently achieved. The 3D dual-layer thermal nanoimprint enables the first metal patterns to have suspending side-wings that can clearly define a distance from the second metal patterns. Isotropic and anisotropic side-wing structures can be fabricated through two different schemes. The process based on isotropic side-wings achieves a lateral-gap in the order of 100 nm. Even a gap of 60 nm can be achieved from the process with anisotropic side-wings.

Because of the capability of nanoscale metal patterning on organic semiconductors with high overlay accuracy, the dual-layer thermal nanoimprint and the self-aligned metallization techniques are expected to find important applications in the fabrication of high-performance organic transistors. Based on those techniques, the functional bottom-contact OMESFET is successfully fabricated in this work. Although the performance of the fabricated organic transistor is not satisfactory yet, it will be more improved in our future work through a stable top-contact metal patterning in a device level and an interface improvement between a gate and an active layer.

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