DESIGN OF ANALOG & MIXED SIGNAL CIRCUITS IN CONTINUOUS-TIME SIGMA-DELTA MODULATORS FOR SYSTEM-ON-CHIP APPLICATIONS

A Dissertation

by

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ABSTRACT

Software-defined radio receivers (SDRs) have become popular to accommodate multi-standard wireless services using a single chip-set solution in mobile telecommunication systems. In SDRs, the signal is down-converted to an intermediate frequency and then digitalized. This approach relaxes the specifications for most of the analog front-end building blocks by performing most of the signal processing in the digital domain. However, since the analog-to-digital converter (ADC) is located as close as possible to the antenna in SDR architectures, the ADC specification requirements are very stringent because a large amount of interference signals are present at the ADC input due to the removal of filtering blocks, which particularly affects the dynamic range (DR) specification. Sigma-delta (ΣΔ) ADCs have several benefits such as low implementation cost, especially when the architecture contains mostly digital circuits. Furthermore, continuous-time (CT) ΣΔ ADCs allow elimination of the anti-aliasing filter because input signals are sampled after the integrator. The bandwidth requirements for the amplifiers in CT ΣΔ ADCs can be relaxed due to the continuous operation without stringing settling time requirements. Therefore, they are suitable for high-speed and low-power applications. In addition, CT ΣΔ ADCs achieve high resolution due to the ΣΔ modulator's noise shaping property. However, the in-band quantization noise is shaped by the analog loop filter and the distortions of the analog loop filter directly affect the system output. Hence, highly linear low-noise loop filters are required for high-performance ΣΔ modulators.

The first task in this research focused on using CMOS 90 nm technology to design and fabricate a 5^{TH}–order active-RC loop filter with a cutoff frequency of 20 MHz for a low pass (LP) CT ΣΔ modulator. The active-RC topology was selected because of the high DR requirement in SDR applications. The amplifiers in the first stage of the loop filter were implemented with linearization techniques employing anti-parallel cancellation and source degeneration in the second stage of the amplifiers. These techniques improve the third-order intermodulation (IM3) by approximately 10 dB; while noise, area, and power consumption do not increase by more than 10%. Second, a current-mode adder-flash ADC was also fabricated as part of a LP CT ΣΔ modulator. The new current-mode operation developed through this research makes possible a 53% power reduction. The new technology also lessens existing problems associated with voltage-mode flash ADCs, which are mainly related to voltage headroom restrictions, speed of operation, offsets, and power efficiency of the latches. The core of the current-mode adder-flash ADC was fabricated in CMOS 90 nm technology with 1.2 V supply; it dissipates 3.34 mW while operating at 1.48 GHz and consumes a die area of 0.0276 mm^2.

System-on chip (SoC) solutions are becoming more popular in mobile telecommunication systems to improve the portability and competitiveness of products. Since the analog/RF and digital blocks often share the same external power supply in SoC solutions, the on-chip generation of clean power supplies is necessary to avoid system performance degradation due to supply noises. Finally, the critical design issues for external capacitor-less low drop-out (LDO) regulators for SoC applications are addressed in this dissertation, especially the challenges related to power supply rejection

at high frequencies as well as loop stability and transient response. The paths of the power supply noise to the LDO output were analyzed, and a power supply noise cancellation circuit was developed. The power supply rejection (PSR) performance was improved by using a replica circuit that tracks the main supply noise under process-voltage-temperature variations and all operating conditions. Fabricated in a 0.18 μm CMOS technology with 1.8 V supply, the entire proposed LDO consumes 55 μA of quiescent current while in standby operation, and it has a drop-out voltage of 200 mV when providing 50 mA to the load. Its active core chip area is 0.14 mm^2. Compared to a conventional uncompensated LDO, the proposed architecture presents a PSR improvement of 34 dB and 25 dB at 1 MHz and 4 MHz, respectively.

DEDICATION

To my parents, brother and parents-in-law
To my dearest wife, Joo Young Jung, and adorable son, Daniel Joonyoung Park

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I. INTRODUCTION

I.1. Background and Motivation

Recently, trends in the microelectronics industry have resulted in a multitude of system-on chip (SoC) implementations in which analog and digital parts are integrated on the same die. Next generation wireless devices will have to support many different standards with a single chipset solution to reduce the cost of products and to increase the performance competitiveness of devices [1]. Generally, it is desirable to relax the specifications for most radio frequency (RF) front-end building blocks with new architectures and digitize the signal as close as possible to the antenna, which increases the demand for high-performance analog-to-digital converters (ADCs). Especially when weak fundamental signals are delivered along with strong interferers as in multi-standard applications, high performance ADCs are required for broadband connections of different wireless networks. However, the requirements of a large bandwidth, high operating frequency and high resolution make the design of ADCs very challenging. Since significant parts of the signal processing are performed in digital domain nowadays, sigma-delta (ΣΔ) ADCs have attracted a lot of attention as digital-friendly ADC implementations with high performance and good efficiency.

The transfer function of the analog loop filter in the ΣΔ modulator defines the quantization noise-shaping behavior. Therefore, the performance of the analog loop filter is one of the main factors impacting the overall performance of the ΣΔ modulator. The selection of the loop topology greatly affects the circuit implementation options for the analog loop filter. In general, two kinds of loop filter architectures are used for single-

stage modulators. One is cascade of integrators with distributed feed-back (CIFB), and the other is a cascade of integrators with feed-forward summation (CIFF). Since the performance requirements of the subsequent stages can be relaxed compared to the first stages (at the input) in feed-forward architecture, the power consumption due to the non-critical blocks can be reduced. The CIFF requires only two accurate DACs, and the signal swing at the internal nodes of the modulator is relaxed with this architecture. However, the CIFF topology needs an additional summing stage to perform feed-forward summation for each integrator output. To guarantee loop stability, the additional summing stage should not add the extra delay. Hence, the implementation of a special summing scheme instead of the conventional voltage-mode summing stage can result in remarkable power savings.

Another SoC implementation challenge is that multi-standard SoC solutions are often designed with one or two shared power supplies for all analog/RF and digital blocks. Thus, SoC performances are frequently degraded due to the noises leaking through the supply of each building block. Therefore, high power supply rejection and low drop-out regulators are important building blocks in the single chip-set designed to establish a multi-standard solution to minimize the impacts of noises on system performance.

I.2. Design Issues

High-dynamic range ΣΔ ADC can be achieved employing a high-order loop filter that shapes the in-band quantization noise. However, there are several noise sources including the quantization noise and non-idealities in the system. The non-idealities of continuous-time ΣΔ ADCs include non-linearities from loop filter and multi-bit DAC,

excess loop delay and clock jitter. Since the ΣΔ ADC's performance can be degraded by them, their effects should be considered with regards to circuit implementation.

I.2.1.Non-linearities

The harmonic distortion in-band due to introduced non-linearities of the circuits degrades the dynamic range of the ADC. In multi-bit ΣΔ ADC, the major sources of non-linearities come from the loop filter and multi-bit DAC. First of all, any non-linearities of the loop filter directly get reflected at the output of the ΣΔ ADC as a distortion. The non-linear Op-amps within the integrators contribute to the harmonic distortions, which degrade the resolution of the ΣΔ ADC. Therefore, the non-linearities of the first loop filter stage dominate the linearity performance of the ΣΔ ADC. Secondly, if multi-bit quantizers are employed in the ΣΔ ADC, the current source mismatch in the multi-bit DAC generates the distortion. This distortion of the DAC also degrades the performance of the ΣΔ ADC since the DAC is connected to the input stage, and harmonic distortion of the DAC will pass through the system as input signal without any noise shaping.

I.2.2. Excess loop delay

The building blocks in the ΣΔ modulator including the comparator, the D flip-flops and the DACs all have propagation delay. The excess loop delay is referred to as a finite delay from the sampling clock edge to the change in the output at the feedback node. Since the modulator pulse response at the sampling instances is changed with the unwanted excess loop delay in the ΣΔ modulator, the noise shaping transfer function is

changed. As shown in [2], the excess loop delay may eventually make the continuous-time ΣΔ modulators unstable and degrade the performance of the ΣΔ ADC. The excess loop delay is a major issue in high frequency operation due to decreasing use of the affordable excess loop delay. There are two different ways to compensate for decreasing performance of the excess loop delay. One is building a direct path around the quantizer. This direct feedback path with additional feedback DAC minimizes the impact of the excess loop delay [3]. Another is to add tunability by adopting a programmable delay compensation block in the main feedback path [4].

I.2.3. Blocker

Blockers are interferers that desensitize a circuit even if the gain does not fall to zero. Several blockers appear at the ADC input and even more will appear as the ADC moves closer to the antenna. High internal voltage swings in the presence of blockers tends to push the system into a nonlinear state. Intermodulation between strong out-of-band (OOB) blockers from ADC input and high-pass shaped noise from feedback causes noise folding over the desired channel. Hence, ADC performance is degraded.

There are several methods to improve blocker tolerances. In [5], the combination of a high-pass filter (HPF) in the feedback path and low-pass filter (LPF) in the feed-forward path is used in a continuous-time (CT) ΣΔ ADC. For power savings, the reconfigurable ΣΔ architectures employing the dynamic changing of the signal transfer function (STF) roll-off are suggested [6-8].

I.2.4. Jitter

There are random variations on the transition edge of a clock or in any oscillator waveform. These random variations are defined as clock jitter. Clock jitter causes a random variation in the pulse width of DACs, and it adds a random phase noise to the output. Wideband jitter modulates both signal and shaped quantization error and fills the signal band with white noise. Therefore, jitter noise is usually one of the important reasons for limited ADC resolution with high sampling frequency. Different DAC pulse shapes will result in different levels of jitter sensitivity. In other words, the jitter effect can directly relate to the number of clock transitions in DAC pulse shape. Since the transitions always happen in the settled condition of DAC feedback in the switch-capacitor type (SC) DAC used in the discrete-time (DT) ΣΔ ADC, it has better performance on jitter than the switch-current DAC, e.g., return-to-zero (RZ), and the non-return-to-zero (NRZ) DACs in a CT ΣΔ ADC. Therefore, the effects of clock jitter are a critical issue in a CT ΣΔ ADC with a high-frequency sampling clock. The key to alleviating clock jitter effects is determining how to prevent the large level transition in feedback caused by DAC pulse shapes. Different signal shapes shown in [9] can prevent large level transitions such as those evidenced by square waves and compares between the several kinds of DAC pulse shapes.

I.3. Research Focus

The analog loop filter is a critical ΣΔ modulator component because it defines the noise-transfer function (NTF) and thereby the quantization noise-shaping behavior. Furthermore, the stability of the ΣΔ modulator mainly depends on the location of the

poles and zeros in the loop filter. Also, the noise and distortion introduced by the first stage of the loop filter directly appears at the output of ΣΔ modulator without noise shaping and often limits the overall performance of the ΣΔ modulator. Therefore, the loop filter is frequently the most critical block in a ΣΔ modulator. To avoid limiting the overall performance due to the analog loop filter, the 5^{TH}-order active-RC loop filter can perform at least to the order of 11-12 bits with less than 10 mW power consumption, which is implemented as part of a 20 MHz bandwidth (BW) low pass (LP) continuous-time (CT) ΣΔ modulator in IBM 90 nm CMOS technology.

The summing amplifier in ΣΔ ADCs requires wide bandwidth to guarantee stability of the system after compensating for the excess loop delay introduced by the parasitic poles of the filter's active components. In lieu of the power-hungry summing amplifier, a current-mode adder and quantizer are proposed to achieve low power ΣΔ ADCs without degrading the entire ADC performances. The design issues of the summing amplifier are fully addressed and analyzed in this dissertation. In addition, the comparison between voltage-mode summing and current-mode summing is presented. The current-mode summing stage is followed by the current comparison stage and strongARM comparator with SR latches as a quantizer in the CT ΣΔ modulator with feed-forward (FF) compensation. The current-mode flash ADC alleviates existing problems associated with voltage-mode flash ADCs, which are mainly related to voltage headroom restrictions, speed of operation, offsets, and power efficiency of the latches. The new design techniques are applied to the design of a 20 MHz BW 5^{TH}-order LP CT ΣΔ modulator

with FF compensation. The current-mode adder and quantizer are also implemented in IBM 90 nm CMOS technology.

Another focus in this research is to overcome the high frequency power supply rejection (PSR) limitation of external capacitor-less low drop-out (LDO) regulators. The fundamental PSR limitations due to the existing paths between the noisy supply and the output are analyzed, including the error amplifier and pass transistor, the gate-source parasitic capacitance, and finite output impedance. Although the feed-forward supply noise cancellation in high PSR LDOs is not a new approach, the LDO's performance can be maintained high under all loading conditions without requiring manual tuning by the technique presented in this dissertation. The parasitic capacitances of the pass transistor under the different loading conditions are precisely tracked by the PSR enhancement employing a replica pass transistor and a current amplifier. The robustness of the proposed scheme was demonstrated by measurement results. The proposed external capacitor-less LDO with PSR enhancement scheme was designed and fabricated in IBM 0.18 μm CMOS technology, and it achieved -40 dB PSR up to 8 MHz for all load conditions. Using the new PSR enhancement scheme, the PSR is improved more than 25 dB for 0.4 MHz - 4 MHz.

I.4 Dissertation Organization

This dissertation focuses on the design consideration of the analog and mixed-signal circuits for CT ΣΔ ADCs in broadband applications. Furthermore, the design issues for external capacitor-less low drop-out regulators with high power supply rejection for SoC applications are analyzed prior to introducing the enhancement method.

An overview of the CT ΣΔ modulator is given in Section II. The design considerations and implementation of a 5^{TH}–order active-RC loop filter for a blocker-tolerant CT LP ΣΔ ADC is also presented in Section II. The typical architecture of CT ΣΔ modulators with FF compensation is explained in Section III along with the most important design issues related to weighted summing of the outputs of various loop filter nodes and the feedback signal from the direct path around the quantizer using the second DAC for minimizing the excess loop delay effects. In addition, a comparison between voltage-mode summing and current-mode summing is made. A current-mode adder-quantizer for low-power CT ΣΔ modulators is presented in Section III. Section IV introduces an external capacitor-less high PSR LDO regulator for SoC applications and analyzes its fundamental PSR limitations at high frequencies due to the paths through which supply noise can leak to the load. Section IV also provides a literature review of research by peers who were also determined to improve PSR of LDOs. Finally, the section offers an explanation, demonstration, and analysis of measured results showing how the innovative PSR compensation scheme can be used to overcome the lack of high PSR at high frequencies with a replica circuit that tracks the main supply noise under process-voltage-temperature (PVT) variations. Section V summarizes the contributions of this dissertation.

II. 5TH-ORDER ACTIVE-RC FILTER FOR BLOCKER TOLERANT CONTINUOUS-TIME SIGMA-DELTA MODULATORS

II.1. Background and Motivation

The basic principles of the sigma-delta (ΣΔ) analog-to-digital converter (ADC) are oversampling and noise-shaping [10]. Quantization noise is spread over the whole sampling frequency through oversampling. Since the quantization noise is shaped by the ΣΔ operation, the in-band quantization noise is decreased while the out-of-band quantization noise is increased as shown in Fig. 2.1. Therefore, ΣΔ ADCs can achieve high resolution by forming a closed-loop system with an embedded loop filter to reduce the number of bits required for the quantizer in the loop. Fig. 2.2 displays the typical block diagram of a single-bit ΣΔ modulator. The loop transfer function and the proper loop topology are determined during system level design of the ΣΔ modulator, which leads to the particular specifications for each building block.

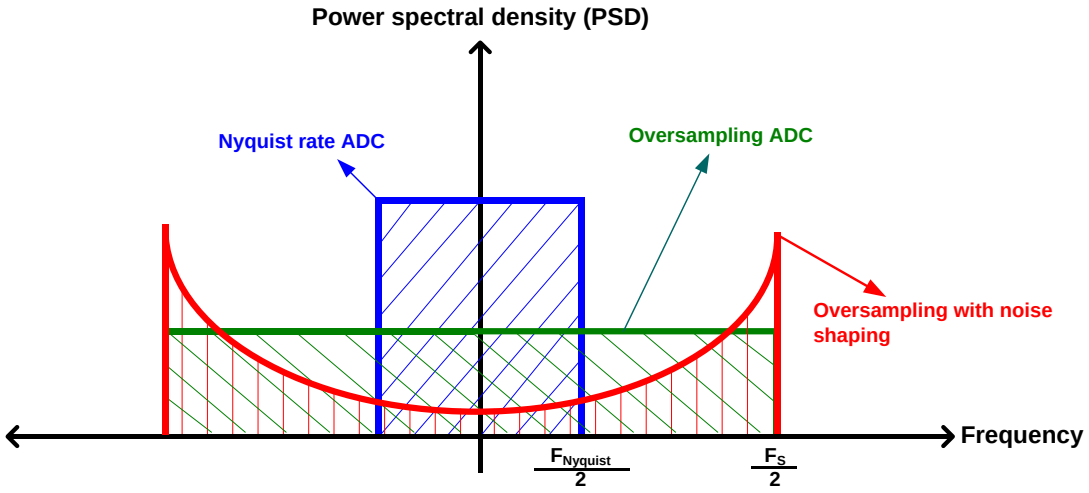


Fig. 2.1. Power spectrum density of quantization noise

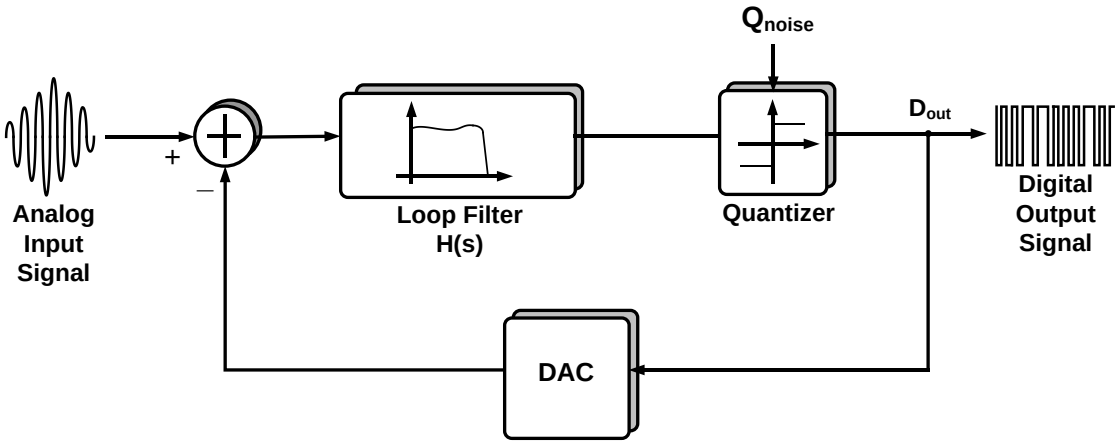


Fig. 2.2. Typical block diagram of single-bit ΣΔ modulator

Recently, the trends of the wireless receiver architecture is to move the ADC as close as possible to the antenna by eliminating the pre-filtering and most of the signal processing is done in digital domain [7, 11-12]. This approach demands stringent DR requirements on the ADC. Since pre-filtering is removed in the receiver, strong OOB blockers occupy most of the ADC dynamic range. The blockers degrade the signal-to-noise ratio (SNR) of in-band signal and also destabilize the ΣΔ loop by overloading it with huge signal swings [8]. A CT ΣΔ modulator employing feedback (FB) loop architecture can increase the blocker tolerance since its signal transfer function (STF) has faster roll-off outside the signal bandwidth. However, FB topology mainly due to the several feedback DACs consumes more power and occupies more silicon area than their feed-forward (FF) counterparts. A CT ΣΔ modulator employing feed-forward (FF) has unwanted OOB peaking and lower order STF roll-off outside the signal band. However, it consumes less power and has better area efficient than FB topology.

There are several approaches to improve blocker tolerances in previous researches [5]; i) the combination of a HPF in the feedback and a counter LPF in the feed-forward path in a CT ΣΔ ADC [5]. However, this architecture demands stringent matching requirements between HPF and LPF in order to avoid the stability issue for high frequency operation. Furthermore, noise and linearity issues arise since these additional blocks are placed at the input of the modulator. ii) To save power consumptions, reconfigurable ΣΔ architectures that dynamically change the STF roll-off depending on the blockers at the input were proposed in [7-8]. The solution reported in [7] monitors an internal node of the ADC to detect blockers and the loop order change is done by modifying the loop parameters. However, the reported approach is not very attractive for wireless applications due to its large time constants. The order of the ADC was reconfigured based on desired channel and interferer levels in [8]. A 5-bit flash ADC at the input of the ADC estimates the level of blocker power and digital signal processing (DSP). System instability may appear when strong agile blockers are present at the ADC input due to latency in DSP processing. Therefore, we proposed low power blocker tolerant CT LP ΣΔ ADC which doesn't have stability issue due to complexity and latency.

II.2. System-level Overview of the Blocker Tolerant CT LP ΣΔ ADC Architecture

The system level block diagram of 5^{TH}-order CT LP ΣΔ modulator with overload detector and non-invasive low-pass filter is depicted in Fig. 2.3. The cascade of integrators in the feed-forward (CIFF) topology is employed in the loop filter and two feedback DACs are implemented in the feedback path [13]. An extra summing stage is

added to sum multiple feed-forward outputs of each integrator. Two current-steering 3-bit unary weighted DACs are employed in the feedback path. Since the non-idealities of the main feedback DAC (DAC1) (due to unavoidable mismatches, parasitic capacitors and so on) appear at the ADC output without any noise shaping, a digitally-assisted current source calibration scheme is employed for DAC1 that has the most stringent requirements in terms of linearity and noise performance. In order to improve the blocker tolerance a non-invasive low-pass filter is employed at the input of the ADC. This filter can reduce the ADC input power by attenuating OOB blockers. The filter absorbs the OOB blocker power at the most critical frequencies, and it is built using a low-gain, high-bandwidth, class-AB amplifier that meets large signal performance requirements with good linearity and low power consumption [14]. Since OOB blockers cause peaking at internal nodes of the loop filter and overload the CT ΣΔ ADC loop, an overload detection block is designed to detect peaking and avoid saturation of the ADC loop due to blockers. The employed wide-bandwidth overload detector and variable gain attenuator are very effective in detecting and attenuating the agile blockers. The overload detection system consists of a set of simple voltage level comparators, digital logic and a signal attenuator implemented with a T-network at the ADC input [14].

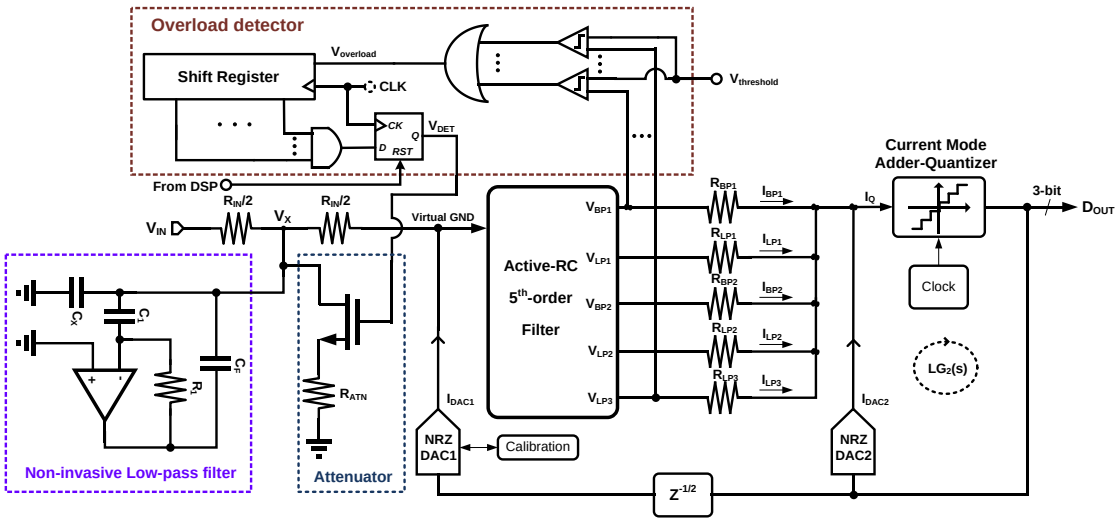


Fig. 2.3. 5[TH]-order CT LP ΣΔ ADC architecture with overload detector monitoring the critical filter nodes and controlling the attenuator.

Since the CIFF topology has the highest sensitivity to peak effects due to blockers, it was selected to evaluate the proposed scheme for blocker tolerant CT LP ΣΔ ADC. Fig. 2.4 displays the voltage gain at various filter nodes. In other words, the voltage gains are the direct trajectories from modulator input (V_{IN}) to the integrator output nodes (V_{BP1}, V_{LP1}, V_{BP2}, V_{LP2} or V_{LP3} in Fig. 2.3) of the loop filter that do not touch the loop, LG_2. The closed-loop gain from V_{IN} to V_{XPi} is expressed as [14]:

$$G_{XPi}(j\omega) = FF_{XPi}(j\omega)\left(1 + K_{fb}H_D(j\omega)e^{-i\omega T_s}\right)NTF(j\omega)\ , \qquad (2.1)$$

where $FF_{XPi}(j\omega)$ is the open-loop voltage gain, K_{fb} is the coefficient of a secondary feedback DAC (DAC2), and $H_D(j\omega)$ denotes the Laplace transform of the DAC output waveform. The important system level design parameters for CT LP ΣΔ ADC are listed in Table II.1.

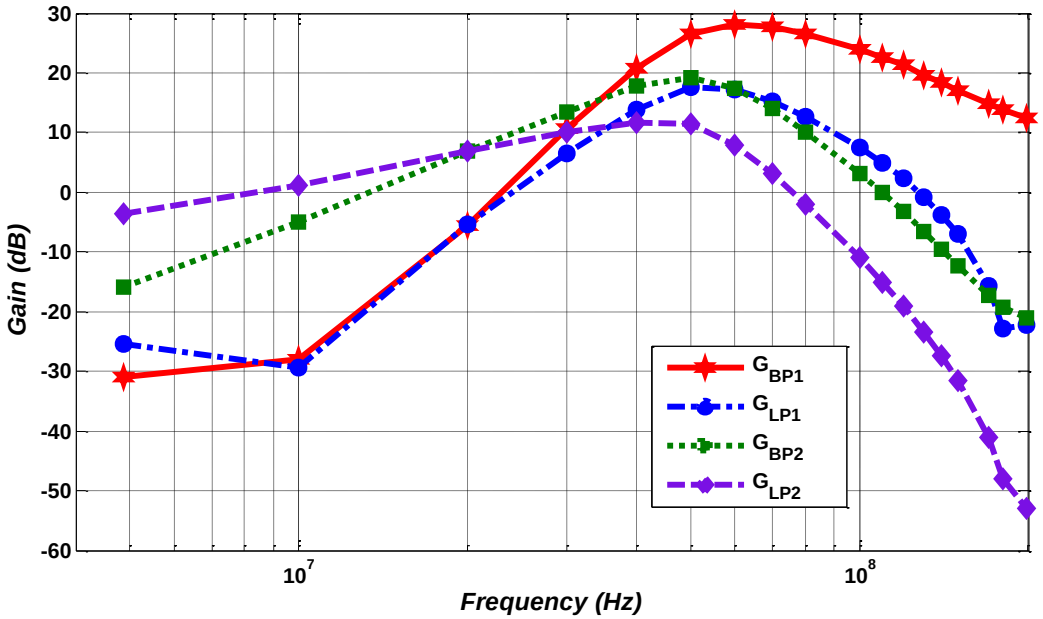


Fig. 2.4. Simulated the closed loop AC gain from input to the internal nodes of 5TH-order CT LP ΣΔ ADC with FF compensation.

TABLE II.1
SYSTEM LEVEL DESIGN PARAMETERS

Parameter	Value
Technology	CMOS 90 nm
Supply Voltage	1.2 V
Resolution	12 bits
Signal Bandwidth	20 MHz
Sampling Frequency	500 MHz
Oversampling ratio (OSR)	12.5
Order	5
Resolution of Quantizer and DACs	3 bits

II.2.1. Design challenge of the loop filter

The design of the analog loop filter is a major challenge in the implementation of a high performance low-power CT LP ΣΔ ADCs In order to achieve high signal-to-quantization-noise-ratio (SQNR), the analog loop filter should have high dynamic range [15] and a high-order to shape the in-band quantization noise. Conventionally, the loop filters of a CT ΣΔ modulator are realized with active integrators, such as active-RC or G_m-C integrators [16]. Active-RC integrators have the advantage of better linearity than G_m-C integrators due to the closed-loop operation at high frequencies [17], but at the expense of more power consumption. Also, additional tuning circuitry is required due to the large deviation of RC time-constant with PVT variations in active-RC integrators. The finite gain and gain-bandwidth product (GBW) of the amplifiers cause the main non-idealities of active-RC integrators. Furthermore, circuit noise and distortion due to the amplifiers used in integrators degrade the performance of the ΣΔ modulator. Especially, the first integrator limits the performances of the entire ΣΔ modulator since its noise and distortion directly appear at the output of the ΣΔ modulator. However, noise and distortion of the subsequent stages are shaped by the ΣΔ loop. Hence, to achieve high performance, the first stage of a ΣΔ modulator dissipates significant power consumption when compared to the overall power budget.

In the discussed example, the targeted ADC resolution is 12-bits over 20 MHz bandwidth (BW). To avoid limiting the overall performance, the loop filter should be able to perform at least to the order of 12 bits signal-to-noise and distortion rejection (SNDR). Since the analog loop filter introduces excess loop delay, the summing

amplifier has to have a wide bandwidth to guarantee stability of the system. Therefore, the design of a low-power summing stage in FF topology is another design challenge for the high-speed operation.

II.2.2. Filter transfer function

The most common method to design a CT ΣΔ modulator is to first find the equivalent DT ΣΔ modulator loop filter and then transform it to the continuous-time domain using an impulse invariant transformation (IIT) [18]. After impulse invariant transformation, the s-domain open-loop transfer function is expressed as

$$\mathrm{H(s)} = \frac{(1.224\times10^{9})s^{4} + (4.398\times10^{17})s^{3} + (1.113\times10^{26})s^{2} + (1.66\times10^{34})s + (1.221\times10^{42})}{s^{5} + (6.681\times10^{7})s^{4} + (1.822\times10^{16})s^{3} + (8.015\times10^{23})s^{2} + (6.594\times10^{31})s + (1.454\times10^{39})} \quad (2.2)$$

where the pole frequencies in the design discussed in this section are located at 10MHz, 18MHz, and 3.26MHz, respectively.

$$STF = \frac{H(s)}{1 + H(s)} \quad (2.3)$$

$$NTF = \frac{1}{1 + H(s)} \quad (2.4)$$

The corresponding transfer functions, STF, NTF and FF, are depicted in Fig. 2.5. The loop filter with feed-forward paths has 5 poles and 4 zeros. Since the poles in FF_{ff} (s) coincide with the zeros of the NTF and cancel out each other, FF_{ff} (s) exhibits first-order OOB blockers roll-off at higher frequencies around and beyond the unity gain frequency. Moreover, the STF_{ff} displays flat in-band response.

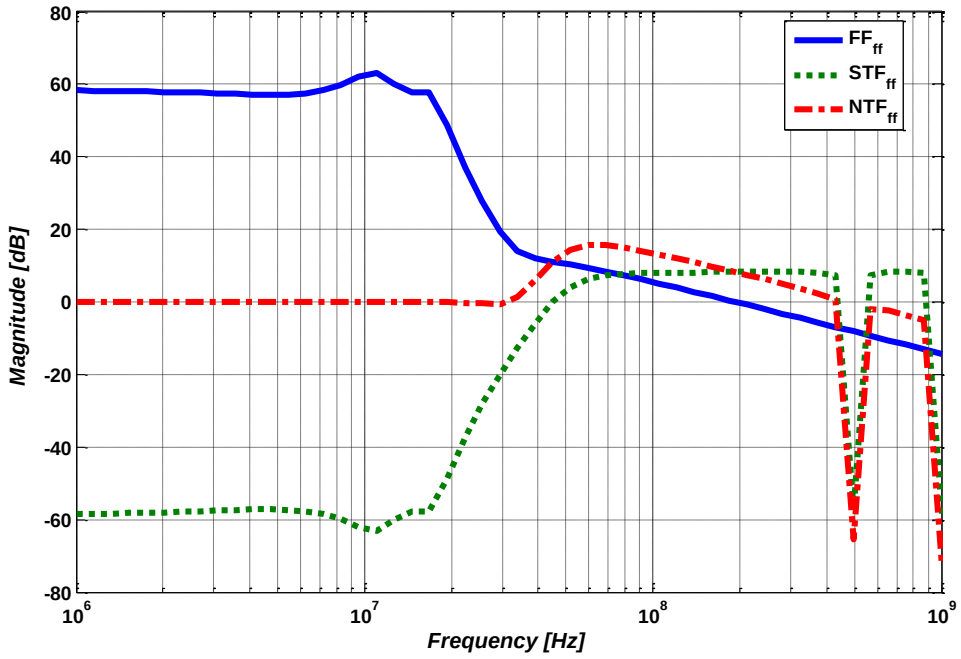


Fig. 2.5. Transfer functions in feed-forward (FF) architecture

II.3. Loop Filter Architecture

The 5TH-order transfer function of the loop filter is realized using FF architecture. As shown in Fig. 2.6; it consists of a cascade of two second-order loop biquad stages and a first-order integrator stage. The outputs of each stage are combined through multiple FF paths with a summing stage. The first stage of the loop filter is the most demanding stage because noise and distortion requirements for the first stage of the loop filter and the main feedback DAC (DAC1) have a strong impact on the overall performance of the entire ΣΔ modulator. As a result, a large transconductance (G_m) of the input stage of amplifiers used in the first stage of the loop filter is needed for noise minimization. In addition, high loop gain and large bias currents in the first stage are necessary for high linearity and tolerance to the loading from the main feedback DAC (DAC1). The loop

filter consists of the three stages. The cut-off frequencies of the first and second stages of loop biquad are placed at 10 MHz and 18 MHz, respectively. The cut-off frequency of the third integrator stage is 3.26 MHz.

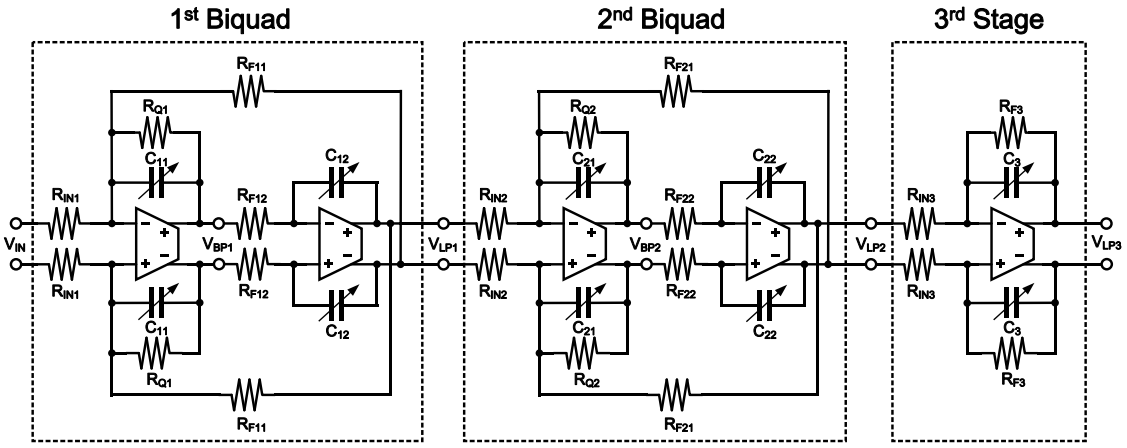


Fig. 2.6. 5TH-order active-RC loop filter

The components values used in the loop filter are listed in Table II.2.

TABLE II.2
COMPONENTS VALUES USED IN THE IMPLEMENTATION OF THE LOOP FILTER

	Parameter	Value
First stage	R_{IN1}	800 Ω
	R_{F11}, R_{F12}	10.4 KΩ
	R_{Q1}	31.2 K Ω
	C_{11}, C_{12}	1.405 pF
Second stage	R_{IN2}	4 KΩ
	R_{F21}, R_{F22}	22.4 KΩ
	R_{Q2}	134.4 KΩ
	C_{21}, C_{22}	0.37 pF
Third stage	R_{IN3}	8 KΩ
	R_{F3}	48 KΩ
	C_3	1.003 pF

Since the desired in-band signal in a ΣΔ modulator is processed by the loop filter, having a very linear loop filter is necessary. Any non-linearities in the loop filter will appear as spurs in the output spectrum of the modulator. All in-band noise corrupts the desired signal content. The most critical noise and distortion for the overall performance of the loop filter are introduced by the first stage of the loop filter. Since the non-idealities of second and third stages are noise shaped by the previous (first) stage, their performance requirements are relaxed. The thermal noise floor of the amplifier used in the first stage of the loop filter should be lower than the quantization noise for optimal performance of the ΣΔ modulator. To tolerate the presence of strong blockers at the input of the ADC, the third-order inter-modulation (IM3) of the amplifier in the first stage of the loop filter is important. An amplifier with high pass-band gain and high bandwidth is required in the first stage of the loop filter. With 20 MHz signal bandwidth and 500 MHz sampling frequency, the bandwidth requirement of the amplifier used in the very first integrator was determined as over 1 GHz with system-level simulations. Also, a DC-gain of about 50 dB is necessary for low in-band distortion in the discussed system design. The loop filter must employ fully-differential circuitry to minimize sensitivity to supply and substrate noise coupling. The important performance requirements of the 5^{TH}-order loop filter are listed in Table II.3.

TABLE II.3
PERFORMANCE REQUIREMENTS OF EACH STAGE OF THE LOOP FILTER

Block	Order	DC-gain	Cut-off frequency	Quality Factor	Noise, SNR
First stage	2	26 dB	10 MHz	3	> 74 dB
Second stage	2	15 dB	18 MHz	6	> 62 dB
Third stage	1	15 dB	3.26 MHz	-	> 52 dB
Complete Filter	5	56 dB	20 MHz	-	> 74 dB

II.3.1. Second-order loop biquad

The first and second stages of the loop filter are implemented with the same two-integrator loop configuration, which is the summed-feedback type (depicted in Fig. 2.7). The summed-feedback structure provides band-pass (BP) and low-pass (LP) outputs that are independently controlled in the filter. Assuming that the amplifiers provide large gain, the transfer functions can be expressed as follows:

$$\frac{V_{BP}}{V_{IN}} = \frac{sC_2R_2\left(\frac{R_1}{R_{IN}}\right)}{1 + sC_2\left(\frac{R_1R_2}{R_Q}\right) + s^2C_1C_2R_1R_2} \tag{2.5}$$

$$\frac{V_{LP}}{V_{IN}} = \frac{\left(\frac{R_1}{R_{IN}}\right)}{1 + sC_2\left(\frac{R_1R_2}{R_Q}\right) + s^2C_1C_2R_1R_2} \tag{2.6}$$

The design parameters can be obtained by:

$$\text{DC Gain}(A_O) = \frac{R_1}{R_{IN}} \tag{2.7}$$

$$\text{Quality Factor (Q)} = \frac{R_Q}{\sqrt{R_1R_2}}\sqrt{\frac{C_1}{C_2}} \tag{2.8}$$

$$\text{Cut\_off Frequency } (\omega_o) = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}} \tag{2.9}$$

DC-gain (A_O) and the quality factor (Q) of the biquad are determined by the ratio of resistors, and the cut-off frequency (ω_O) can be tuned using a variable resistor or capacitor. Therefore, the values of the resistors (R_{IN}, R_1, R_2, and R_Q) and capacitors (C_1 and C_2) in the biquadratic section can be determined according to the DC-gain and quality factor requirements. However, since thermal noise of the first stage directly appears at the output of the modulator, it should be minimized. The input-referred noise of the biquad can approximately be expressed as:

$$\begin{aligned} {V_{in_n}}^2 = 4kTR_{IN}\left[1 + \frac{R_{IN}}{R_1} + \frac{R_{IN}}{R_Q}\right] + 4kTR_2|sC_2R_2|^2 \\ + \left[{V_{n\_amp\_I}}^2 + {V_{n\_amp\_II}}^2|sC_2R_2|^2\right]\left|\frac{R_{IN}}{R_Q} + sC_1R_{IN}\right|^2 \end{aligned} \tag{2.10}$$

where ${V_{n,amp\_I}}^2$ and ${V_{n,amp\_II}}^2$ are the input-referred noise of the first and second amplifiers of the biquad, respectively. The first amplifier (Amplifier-I) and input resistor (R_{IN}) of the biquad are the main noise contributors at low frequencies. The value of R_{IN} is selected based on the noise requirement, and the value of the other resistors and capacitors is determined from the loop filter specifications and using equation (2.7)-(2.9).

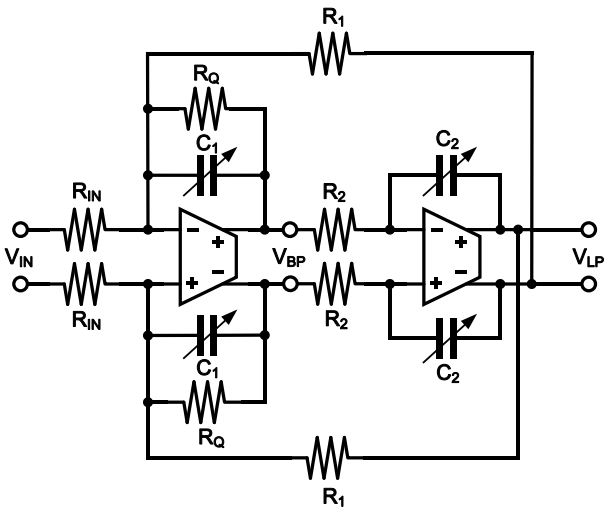


Fig. 2.7. Two integrator loop biquad.

II.3.2 First-order integrator

As shown in Fig. 2.8, the lossy integrator is realized with a first-order integrator of the third stage in the loop filter. Assuming that the amplifier provides large gain, the transfer function can be expressed as follows:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{R_F}{R_{IN}}\right)\left(\frac{1}{1 + sR_FC_1}\right) \tag{2.11}$$

The design parameters can be obtained as:

$$\text{DC Gain}(A_O) = \frac{R_F}{R_{IN}} \tag{2.12}$$

$$\text{Cut\_off Frequency } (\omega_o) = \frac{1}{R_FC_1} \tag{2.13}$$

The values of resistor ($R_{IN,}\, R_F$) and capacitor (C_1) are determined from the loop filter specifications, gain and bandwidth, and using equations (2.12)-(2.13). The integrator time constants can vary due to PVT variations of absolute values of resistors and capacitors. In order to compensate for PVT variations, the capacitor banks that can

provide ±30% tuning range are implemented for each capacitor of the loop filter to adjust the location of the pole implemented by the integrator.

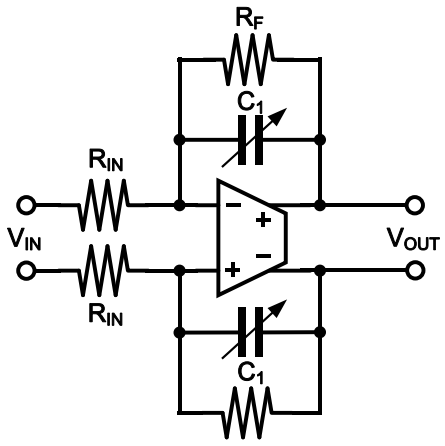


Fig. 2.8. First-order integrator for the third stage of the loop filter.

II.4. Amplifier

The thermal noise floor of the amplifier used in the first stage of the loop filter should be lower than the quantization noise for optimal performance of the modulator. To tolerate the presence of strong blockers at the input of the ADC, IM3 of the amplifier in the first stage of the loop filter is important. An amplifier with high pass band gain and high bandwidth is required in the first stage of the loop filter. With 20 MHz signal bandwidth and 500 MHz sampling frequency, the bandwidth requirement of the amplifier used in the very first integrator was determined as 1 GHz with system-level simulations. Also, a DC-gain of about 50 dB is necessary for low in-band distortion. The filter must employ fully-differential circuitry throughout to minimize sensitivity to supply and substrate noise coupling.

II.4.1. Amplifier architecture

The amplifier used in the first integrator stage needs to satisfy high gain and bandwidth requirements, which are contradicting design requirements. High-gain amplifiers typically use multi-stage architectures with long channel length devices at low bias current levels. High-bandwidth amplifiers typically use single-stage architectures with short-channel devices at high bias current levels.

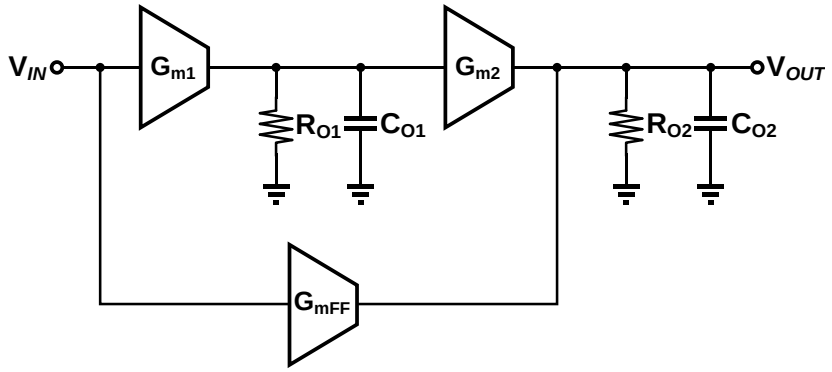


Fig. 2.9. The block diagram of a two-stage amplifier with FF compensation.

To satisfy the high gain and bandwidth requirements simultaneously, a two-stage amplifier with FF compensation is adopted [19]. Fig. 2.9 displays the block diagram of a two-stage amplifier with FF compensation. The overall voltage transfer function of the amplifier can also be expressed as follows:

$$H(s) = \frac{(G_{m1}R_{O1})(G_{m2}R_{O2})}{(1+sR_{O1}C_{O1})(1+sR_{O2}C_{O2})} + \frac{G_{mFF}R_{O2}}{(1+sR_{O2}C_{O2})} \tag{2.14}$$

Assuming that G_{m2}=G_{mFF}, equation (2.14) can be simplified as:

$$H(s) = \{G_{m2}R_{O2}(1+G_{m1}R_{O1})\}\left\{\frac{1+\frac{sR_{O1}C_{O1}}{(1+G_{m1}R_{O1})}}{(1+sR_{O1}C_{O1})(1+sR_{O2}C_{O2})}\right\} \tag{2.15}$$

With this FF technique, the negative phase shift introduced by the poles in the forward path is compensated by the positive phase shift introduced by the LHP zero in the feed-forward path. Because a LHP zero is created without using any Miller capacitor, the dominant pole is not pushed to lower frequencies. Therefore, a higher gain-bandwidth product with fast step response can be achieved. Also, the settling time requirement of the first amplifier is the most demanding due to feedback DAC.

II.4.2. Circuit implementation

The fully-differential circuit implementation of the amplifier is shown in Fig. 2.10. The first and the feed-forward stages are the main contributors to the input-referred thermal noise of the amplifier. To reduce the input-referred noise aspect and increase the gain, the transconductance (G_m) and output resistance of the first stage should be increased. Since the output swing of the first stage of the amplifier does not have to be high because the signal is further amplified by the gain of the second stage, a cascode stage and a complementary input stage were selected. The second and feed-forward stages are optimized for high bandwidth and medium gain performance. The transconductance (G_m) of the second and feed-forward stages should be increased as much as possible to the push poles to higher frequencies. For better linearity, the second stage gain also has to be large. That is why we use the complementary stage in second and feed-forward stages. Also, we use an additional differential pair connected in anti-parallel with second stage and source degeneration technique to improve the linearity [20].

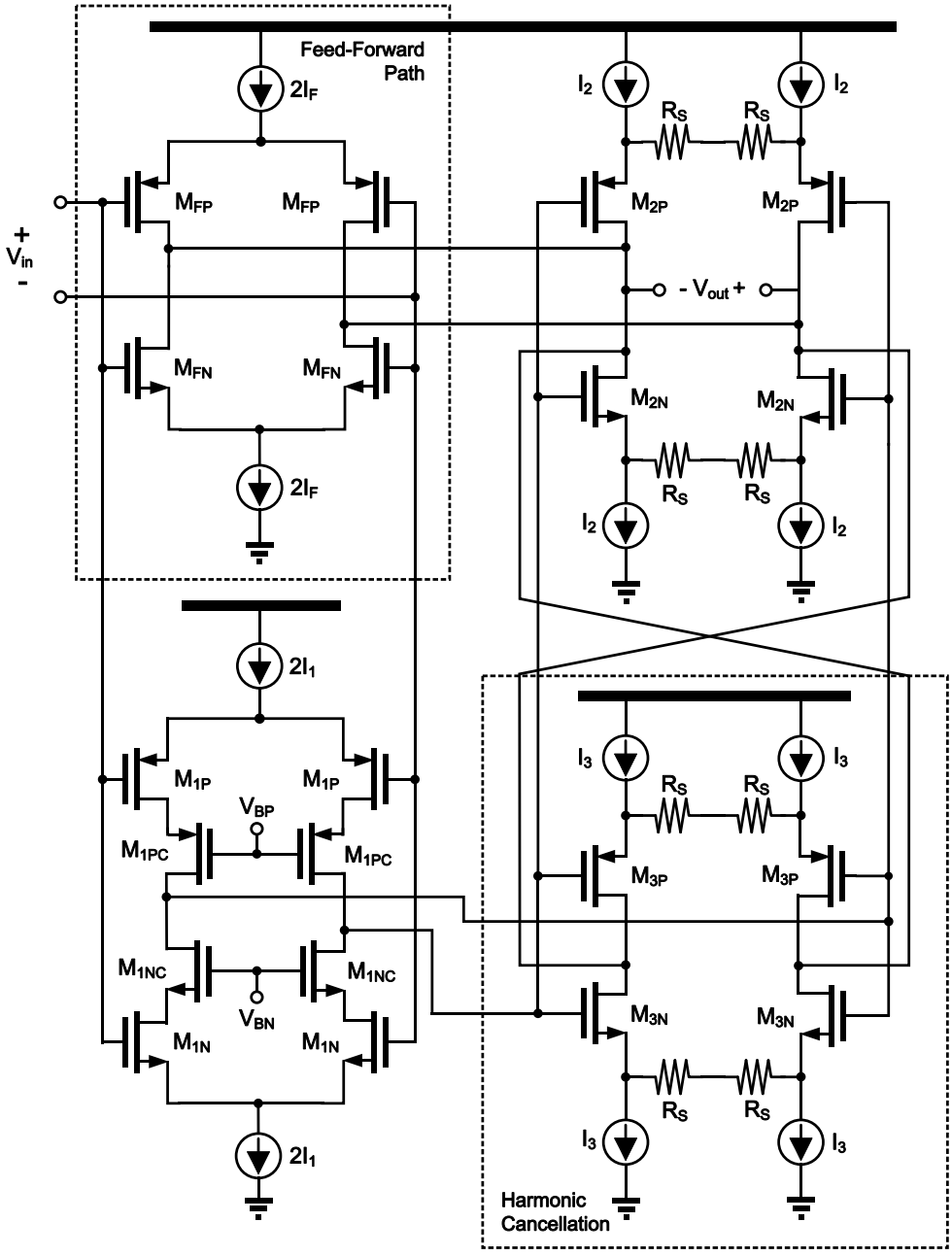


Fig. 2.10. The schematic of the Amplifier-I used in the first stage of the loop filter.

The auxiliary circuit is designed such that its main transconductance (G_m) is smaller than the transconductance (G_m) of the second stage. However, its third harmonic distortion is designed to be similar to that of the second stage transistor such that the cross-coupling circuitry partially cancels the harmonic distortion of the second stage. The DC common-mode levels at the output of the first and second stage of the amplifier are set to 0.6 V, and they are controlled by a common-mode feedback circuit (CMFB) for each stage. The amplifier was optimized with respect to stability, noise, linearity, and power. The parameters of Amplifier-I used in the first stage of the loop filter are listed in Table II.4.

TABLE II.4

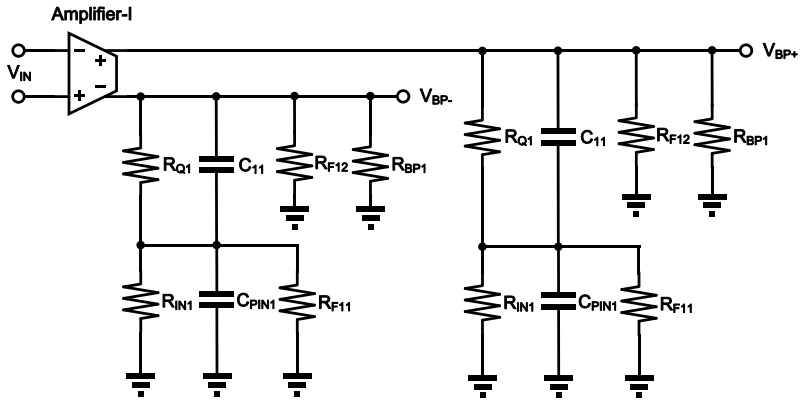
PARAMETERS OF THE AMPLIFIER-I USED IN THE FIRST STAGE OF THE LOOP FILTER.

		Dimension (W/L)	Bias current (μA)
First stage	M_{1P}	60 μm / 200 nm	200 μA
	M_{1PC}	60 μm / 200 nm	200 μA
	M_{1NC}	24 μm / 300 nm	200 μA
	M_{1N}	24 μm / 300 nm	200 μA
Second stage	M_{2P}	144 μm / 200 nm	400 μA
	M_{2N}	42 μm / 300 nm	400 μA
Feed-forward stage	M_{FP}	136 μm / 200 nm	400 μA
	M_{FN}	40 μm / 300 nm	400 μA
Anti- parallel stage	M_{3P}	36 μm / 200 nm	100 μA
	M_{3N}	10 μm / 300 nm	100 μA
R_s		20 Ω	
V_{BP}		0.4 V	
V_{BN}		0.8 V	

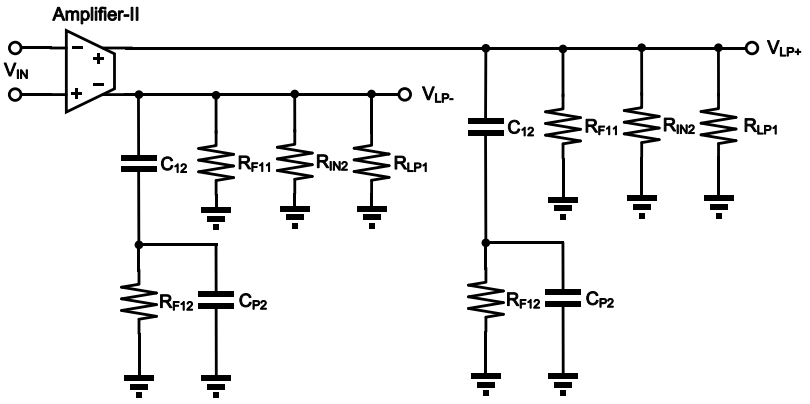
The second integrator of the first stage in the loop filter employs the same amplifier structure, but was designed to consume less power. From the third to the fifth integrator of the loop filter, the same amplifier structure is employed except that the linearization technique is removed and the power consumption is reduced.

II.4.3. Simulation results of the amplifiers

The loop gain was simulated by considering the loading of the amplifier in the two-integrator loop biquadratic structure as shown in Fig. 2.11.



(a)



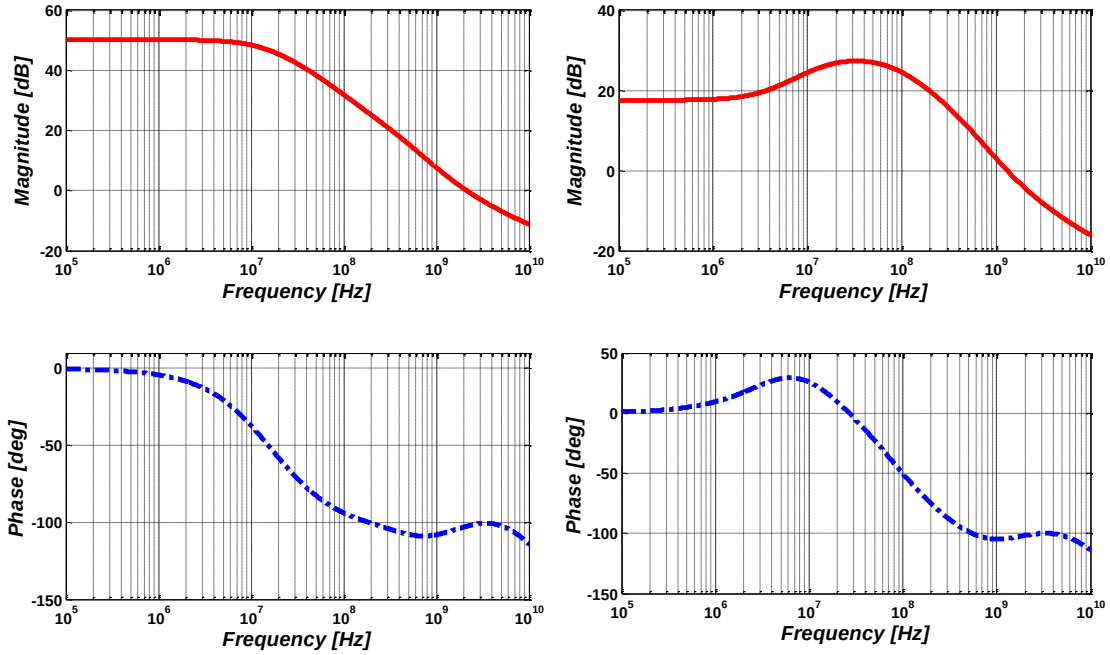
(b)

Fig. 2.11. Amplifiers test-bench with loading (a) Amplifier-I, and (b) Amplifier-II.

Fig. 2.12 and Fig. 2.13 display simulated AC magnitude and phase response plot of the Amplifier-I and Amplifier-II used in the first stage of the loop filter, yielding the following results: i) Amplifier-I (Fig. 2.12): the phase margin is 77° at the unity gain frequency of 2.1 GHz. It has an open-loop DC gain of 50 dB while the voltage gain is 45 dB at 20MHz. ii) Amplifier-II (Fig. 2.13): the phase margin is 84° at the unity gain frequency of 2.7 GHz. It has an open-loop DC gain of 47 dB, while the voltage gain is 43 dB at 20 MHz. The performances of the Amplifier-I and Amplifier-II of the first stage of the loop filter are summarized in Table II.5.

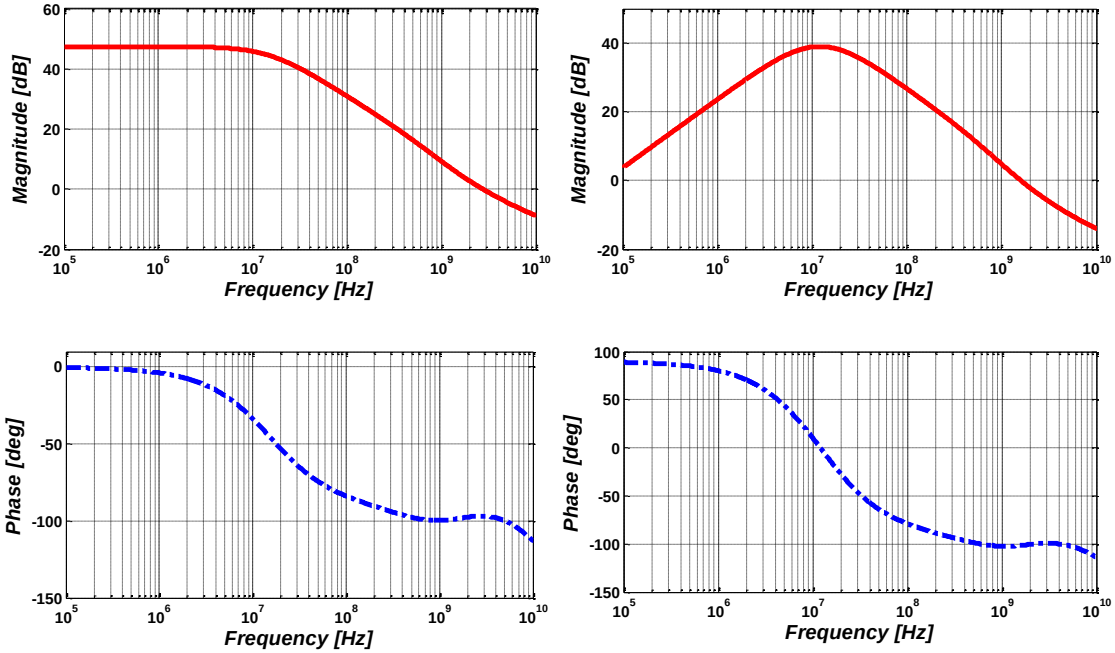
TABLE II.5
AMPLIFIER-I VS. AMPLIFIER-II OF THE FIRST STAGE OF THE LOOP FILTER

	Amplifier-I	Amplifier-II
Open-loop DC gain	50 dB	47.43 dB
Gain bandwidth product	2.1 GHz	2.7 GHz
Input referred integrated noise density (Up to 20 MHz and Temperature = 80 ℃)	13.33 uV	14.57 uV
Phase Margin	77 degree	84 degree
Spot noise (@ 20 MHz and Temperature = 80 ℃)	2.52 nV/sqrt(Hz)	2.87 nV/sqrt(Hz)
Power consumption	2.64 mW	2.11 mW



(a) (b)

Fig. 2.12. (a) Open-loop gain, and (b) loop gain of Amplifier-I.



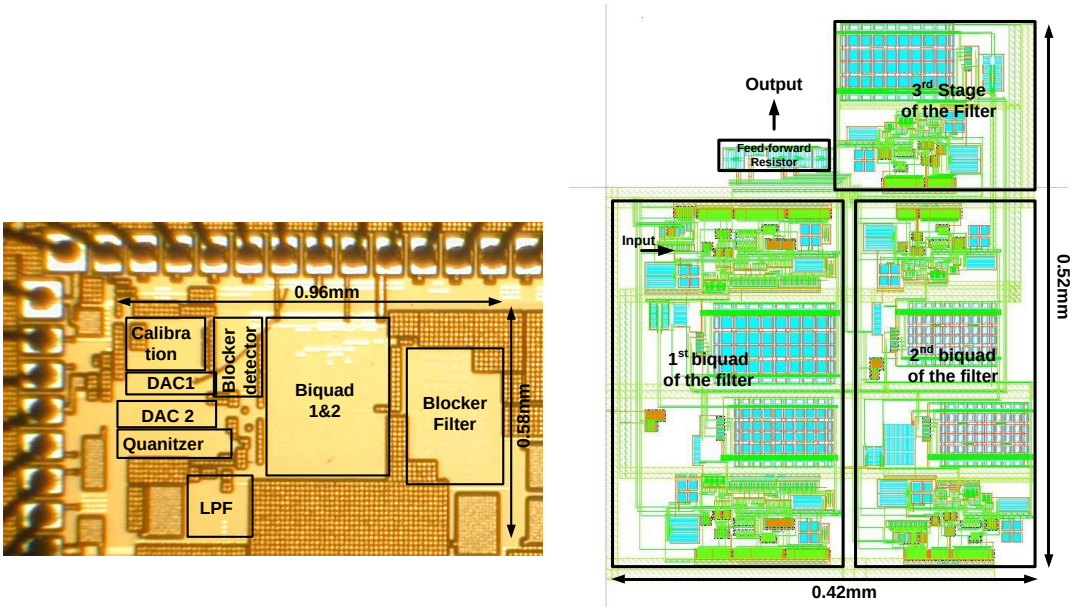
(a) (b)

Fig. 2-13. (a) Open-loop gain, and (b) loop gain of Amplifier-II.

II.5. Layout and Results

II.5.1. Layout

The microphotograph of the entire CT ΣΔ ADC including all the building blocks is shown in Fig. 2.14. The active area of the entire CT LP ΣΔ ADC occupies 0.43 mm^2 silicon area (shown in Fig. 2.14(a)). The total area of the 5^{TH}-order loop filter occupies approximately 0.22 mm^2 (shown in Fig. 2.14(b)). The CT LP ΣΔ ADC including the loop filter was designed and fabricated in a 90 nm CMOS technology.



(a) (b)

Fig. 2.14. (a) CT LP ΣΔ ADC chip microphotograph, and (b) layout of the 5^{TH}-order LP loop filter.

II.5.2. Simulation results

II.5.2.1. The first stage of the loop filter

The simulation results for the first stage of the loop filter are presented in this section. Fig. 2.15 displays the AC magnitude and phase responses of the first stage of the loop filter. The DC-gain of the first stage of the loop filter is 26 dB, and its quality factor is 3. The cut-off frequency of the first stage in the loop filter is 10 MHz.

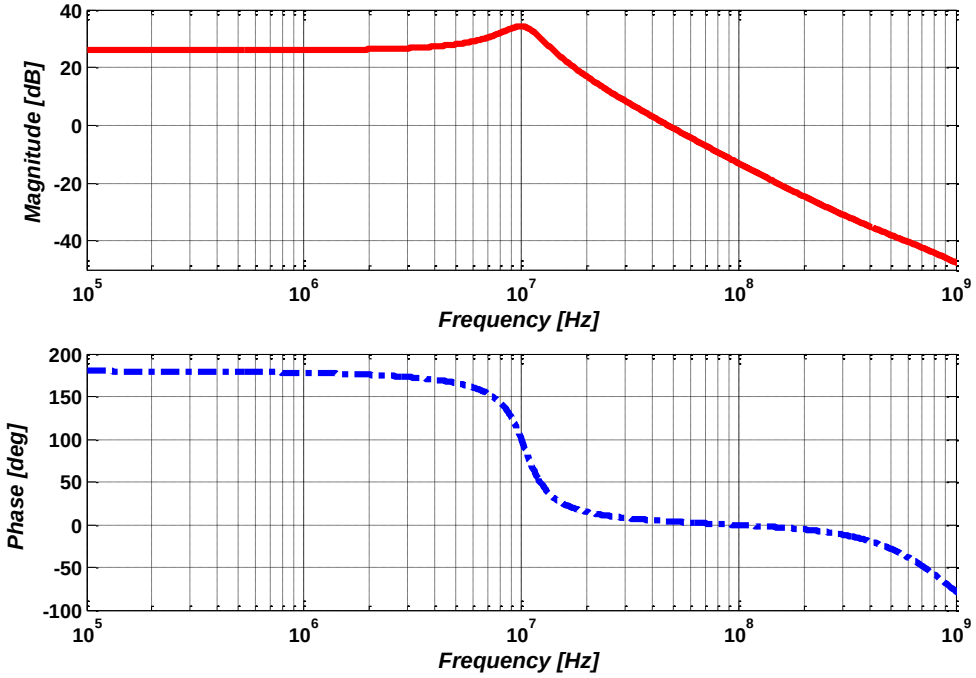


Fig. 2.15. AC magnitude and phase response of the first stage of the loop filter.

The input-referred noise spectral density of the first stage is depicted in Fig. 2.16. The in-band noise spectral density is approximately 7.78 nV/sqrt(Hz) at 20 MHz. As shown in Fig. 2.17, the IM3 is improved by around 10 dB; while noise, area, and power consumption do not increase by more than 10% with the linearization technique employing anti-parallel cancellation and source degeneration.

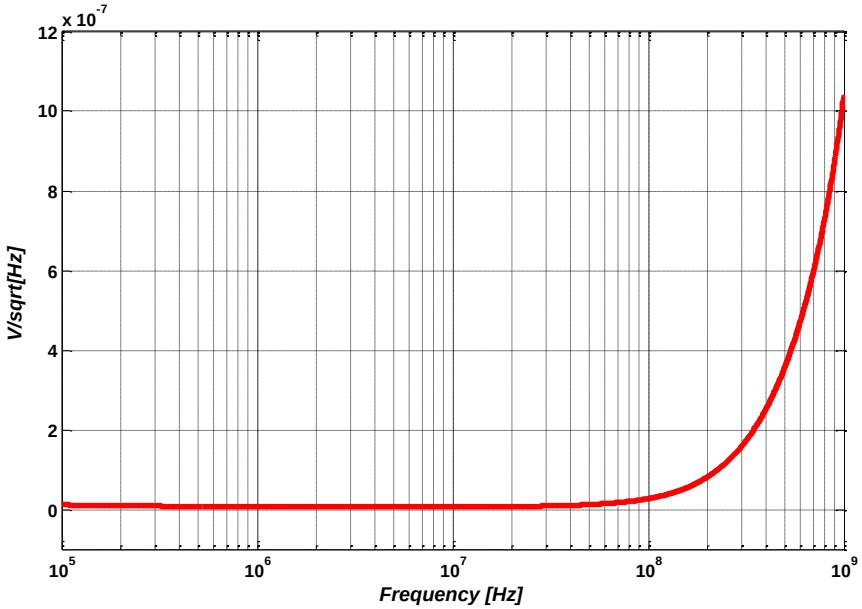
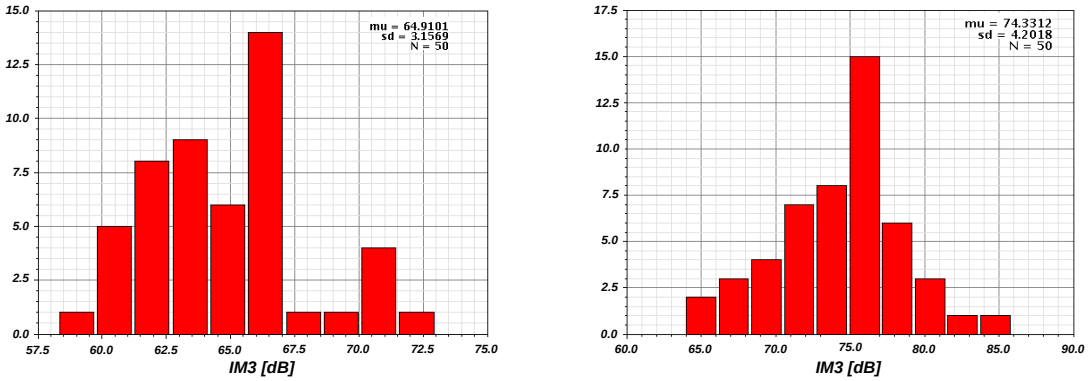


Fig. 2.16. Input referred noise density in the first stage of the loop filter.



(a) (b)

Fig. 2.17. The IM3 in the first stage of the loop filter (a) without harmonic cancellation, and (b) with harmonic cancellation @ 400mV$_{pk}$ differential output swing (Monte Carlo simulation with 10 MHz and 11 MHz two tones).

The performances of the first stage in the loop filter and the effectiveness of the harmonic cancellation scheme employing an additional differential pair connected anti-

parallel to the second stage in combination with source degeneration [16] are summarized in Table II.6.

TABLE II.6
THE FIRST STAGE OF THE FILTER W/O AND WITH HARMONIC CANCELLATION

	w/o Harmonic Cancellation	with Harmonic Cancellation
Input referred integrated noise density (Up to 20 MHz and Temperature = 80 ℃)	30.65 uV	30.96 uV
Spot noise (@ 20 MHz and Temperature = 80 ℃)	7.73 nV/sqrt(Hz)	7.78 nV/sqrt(Hz)
Power consumption	4.35 mW	4.75 mW
SNR (400 mV_{pk} @ differential output)	78.27 dB	78 dB
IM3 (400 mV_{pk} @ differential output)	- 64.9 dB	- 74.33 dB
Two tone signal	9 MHz and 10 MHz	

II.5.2.2. The second and third stages of the loop filter

As shown in Fig. 2.18, the simulated DC gain of the second stage of the loop filter is 15 dB, and quality factor is 6. The cut-off frequency of the second stage of the loop filter is 18 MHz.

The DC gain and cut-off frequency of the third stage in the loop filter are 15 dB and 3.26 MHz, respectively (depicted in Fig. 2.19). The performances of the second and third stages of the loop filter are summarized in Table II.7.

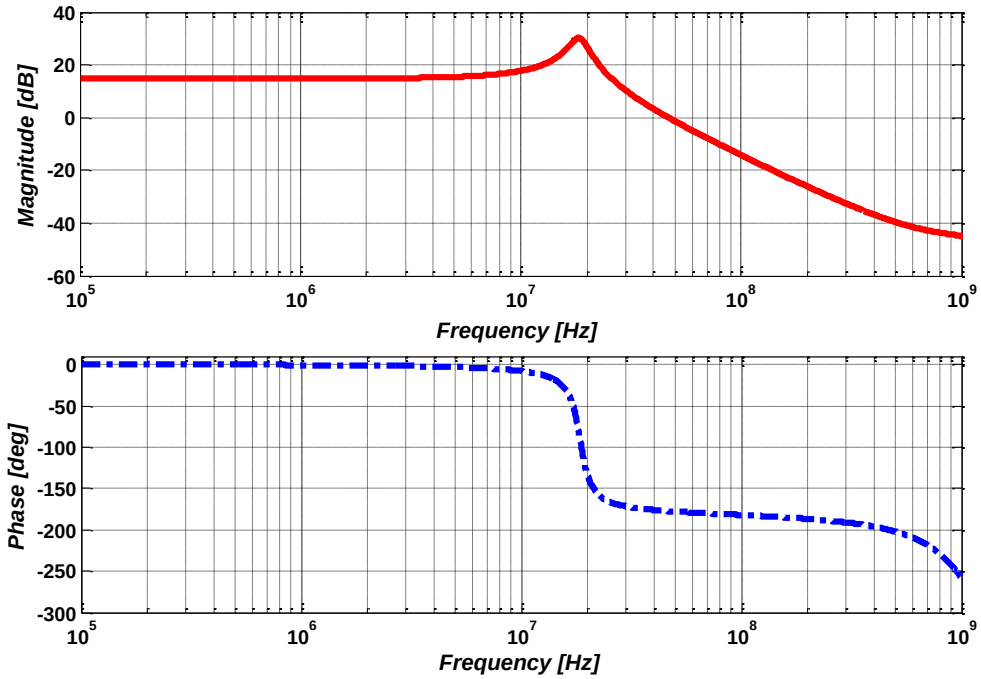


Fig. 2.18. AC magnitude and phase response of the second stage of the loop filter.

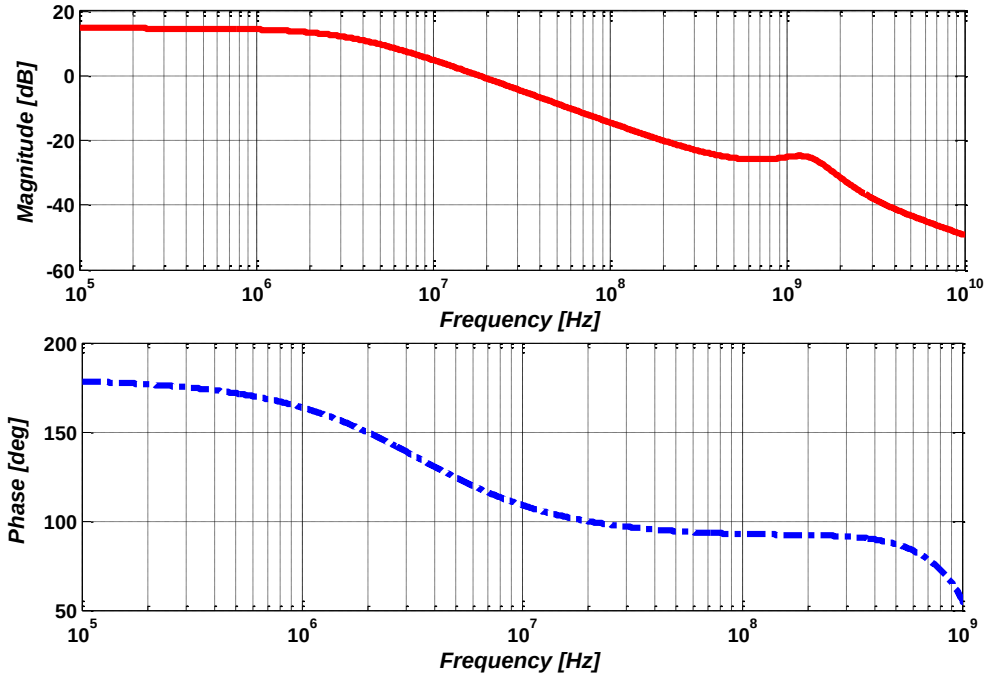


Fig. 2.19. AC magnitude and phase response of the third stage of the loop filter.

TABLE II.7

PERFORMANCES OF THE SECOND AND THIRD STAGES OF THE LOOP FILTER

	Second stage	Third stage
Input referred integrated noise density (Up to 20 MHz and Temperature = 80 ℃)	67.27 uV	88.56 uV
Spot noise (@ 20 MHz and Temperature = 80 ℃)	15.59 nV/sqrt(Hz)	20.01 nV/sqrt(Hz)
Power consumption	2.05 mW	1.025 mW

The important performance parameters of 5^{TH}-order LP loop filter are summarized in Table II.8.

TABLE II.8

PERFORMANCE PARAMETERS OF THE 5^{TH}-ORDER LOW-PASS LOOP FILTER

	Value
Technology	90 nm CMOS
DC gain	56 dB
Cut-off frequency	20 MHz
Input referred integrated noise density (Up to 20 MHz and Temperature = 80 ℃)	31.5 uV
IM3 (400 mV_{pk} @ differential output)	-72 dB
Spot noise (@ 20 MHz and Temperature = 80 ℃)	7.82 nV/sqrt(Hz)
Power consumption	7.83 mW
Area	0.22 mm^2

II.5.3. ADC chip measurements with embedded loop filter

Fig. 2.20 shows the output spectrum of the modulator with an input of -2.86 dBFS at 2.75 MHz. The measured peak SNR and SNDR in 20MHz bandwidth is 63.4 dB and 61 dB, respectively. Also, the third harmonic distortion (HD3) and second harmonic distortion (HD2) components in this case are -70.8 dBFS and -76.7 dBFS, respectively.

The measured SNR and SNDR for different input signal powers are plotted in Fig. 2.21, in which the 67 dB dynamic range (DR) is annotated. The third-order intermodulation distortion (IM3) performance was characterized by injecting two tones around 19.5 MHz with 0.61 MHz separation, where each tone had a power of -9.8 dBFS. As depicted in Fig. 2.22, the worst case of IM3 for the entire band of the ADC was -62.7 dBc because the loop gain reduces at the band edge.

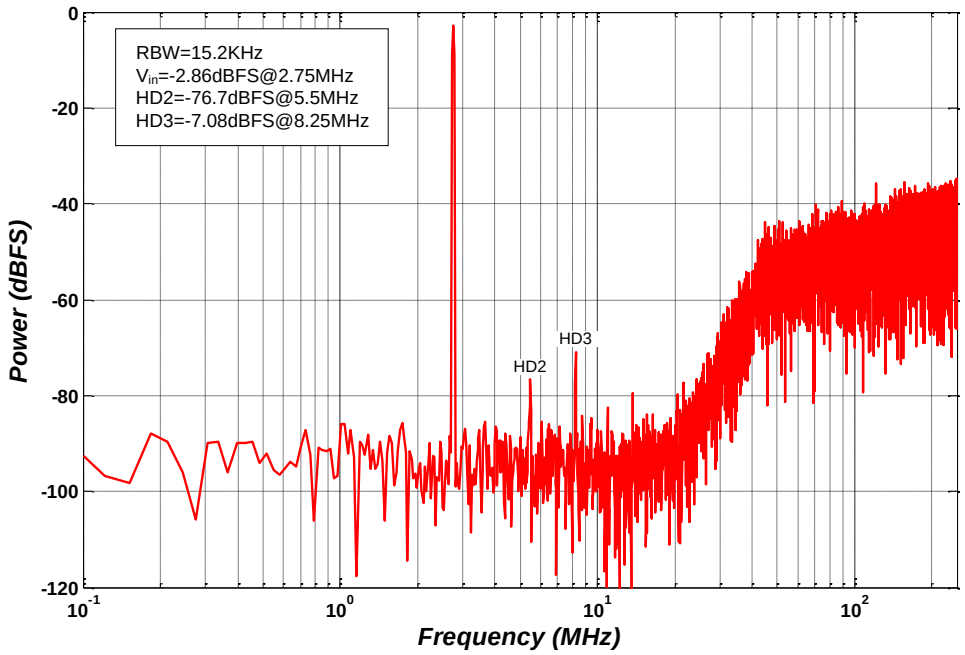


Fig. 2.20. Measured output spectrum of the CT LP ΣΔ modulator with -2.86 dBFS input signal at 2.75 MHz.

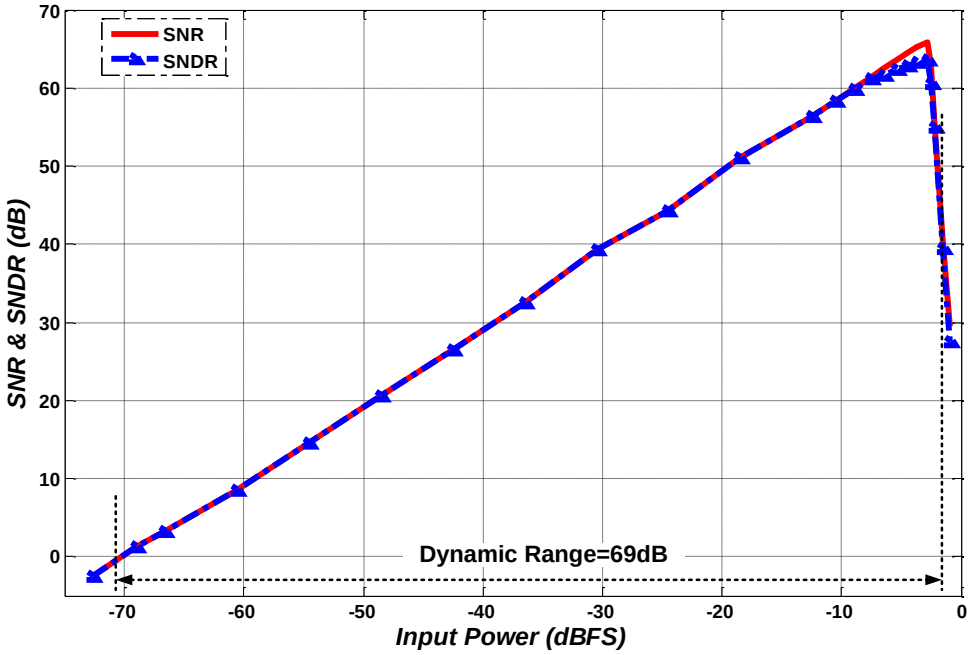


Fig. 2.21. Measured SNR and SNDR versus input signal power.

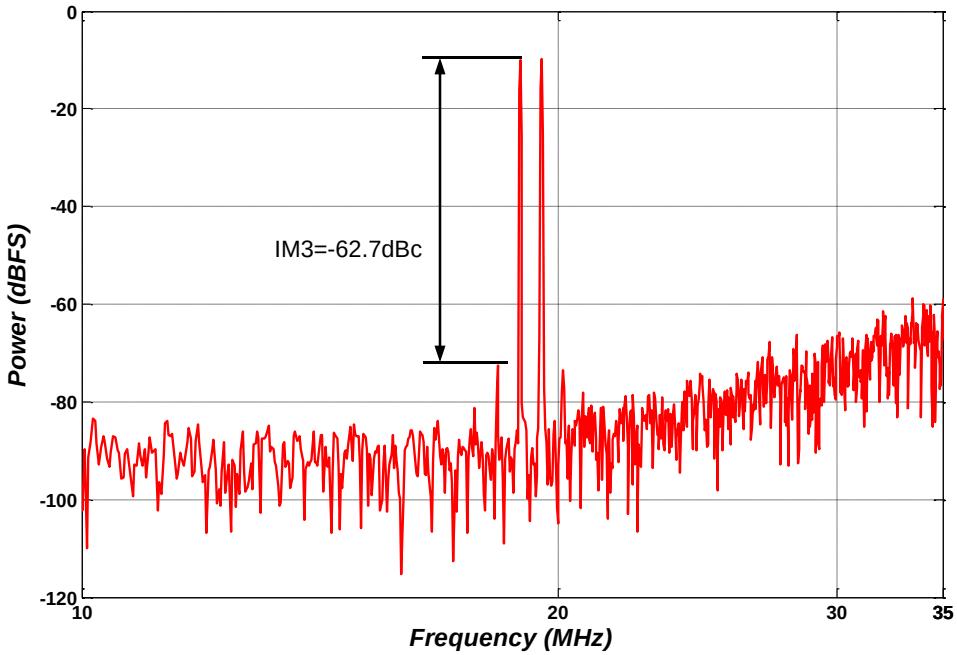


Fig. 2.22. Two tone test for IM3 performance measurement.

II.6. Summarizing Remarks

A 5^{TH}-order active-RC loop filter was designed to meet the dynamic range requirement of a 20MHz BW CT LP ΣΔ ADC. The design considerations for the loop filter in CT LP ΣΔ ADCs were discussed. The first stage of the loop filter demands a larger linear range to allow increased internal signal strength without consuming significant static power and to generate minimal noise. Therefore, the amplifiers and components used in the first stage of the loop filter are the most power hungry. To reduce the input-referred noise density of the first stage in the filter, a complementary input stage was implemented in the amplifiers. However, since the linearity and noise requirement of the second and third stages of the loop filter are shaped by the gain of the previous stage, those have relaxed specifications and are scaled to save power. To check the linearity of each stage in the loop filter, two-tone signals which are very close to the cut-off frequency of each stage were used. All simulations were performed at a temperature of 80°C. For better linearity, the amplifiers of the first stage of the loop filter were implemented with a harmonic cancellation technique that is an anti-parallel differential pair with source degeneration technique. The linearity (IM3) of the first stage in the loop filter was improved by about 10 dB via linearization. In addition, Monte Carlo simulation result showed that the linearity of the first stage of the loop filter was over -74 dB with the linearization. In summary, the filter achieves the required linearity specifications for the target system. The robustness to PVT variations was verified with Monte Carlo simulations, and the 5^{TH}-order active-RC loop filter was fabricated in a 90

nm CMOS technology. The 5^{TH}–order active-RC loop filter was embedded in a sigma-delta loop, and its high performance was verified through system level measurements.

III.CURRENT-MODE ADDER-QUANTIZER FOR BROADBAND LOW-POWER CONTINUOUS-TIME SIGMA-DELTA MODULATORS

III.1. Background

Low-voltage analog design methods have to comply with the decreasing supply voltages on mixed-signal chips. Generally, supply voltage scaling in deep sub-micrometer CMOS technologies has an adverse effect on the speed, power, and accuracy trade-offs during the design of high-speed ADCs [23]-[24]. High-speed, low-resolution quantizers are essential parts of the ADCs used in receivers for wireless communication systems. They have to combine stringent speed specifications with the demand for low-power consumption. Flash ADC architectures generally achieve the highest sampling rate with a single clock period latency, where the comparator performance typically determines maximum sampling speed. One of the applications for flash ADCs is as integrated quantizers in sigma-delta modulators. Conventional ΣΔ modulators have system architectures with feedback (FB), feed-forward (FF), or a combination of FB and FF paths. Since the output swing of the first stage of the loop filter in a FF architecture is relatively small compared to that in a feedback topology [23], high integrator coefficients are often used in FF architectures to tolerate more noise and distortion in the second and subsequent integrator stages, which can be designed with reduced bias currents to decrease the overall power consumption. In this paper, we present a 3-bit prototype current-mode flash ADC architecture implemented in a commercial 90 nm CMOS technology that can be used for low-power CT ΣΔ modulators.

The main goals for this current-mode implementation are high-speed operation, avoidance of voltage headroom constraints, and replacement of the power-hungry summing amplifier and voltage-mode quantizer with a low-power current-mode flash ADC whose signal level quantizer is around a fixed common-mode level. This paper shows how better performance is achieved with 53% less power consumption compared to the conventional voltage-mode counterpart. In addition, the proposed architecture facilitates the use of low-power latches and the use of accurate current references makes it robust to PVT variations.

III.2. Typical Summing and Flash ADC Architecture

III.2.1. Conventional ADC architecture

Fig. 3.1 displays the generalized architecture of typical FFCT ΣΔ modulators. Conventional FF CT ΣΔ modulators require a summing amplifier that performs weighted addition of the outputs of various loop filter nodes and the feedback signal from the direct path around the quantizer. The direct feedback path with the second DAC (DAC2) minimizes the impact of the excess loop delay that can cause signal-to-noise ratio degradation [3]. Excess loop delay is caused by the parasitic poles of the filter's active components as well as time delay while driving the DACs combined with the interface between DAC2 and the summing amplifier. Since the direct path around the quantizer with DAC2 ($LG_2(s)$ in Fig. 3.1) reduces the loop sensitivity to the filter's excess delay, this path should be very fast. For example, when the loop is ideally designed for a delay of T_{clk} seconds, the time delay of the fast path should be less than

$T_{clk}/2$ seconds since the quantizer uses $T_{clk}/2$ seconds to resolve the input signal. Therefore, the use of a power hungry broadband summing amplifier is mandatory.

The summing operation in Fig. 3.1 can be implemented with voltage-mode techniques (using closed loop operational amplifiers resistors/capacitors) or current-mode techniques employing transconductors [25]. The latter approach is not an option for high-performance modulators due to the limited linearity of these elements; hence, this option is not further considered in this work.

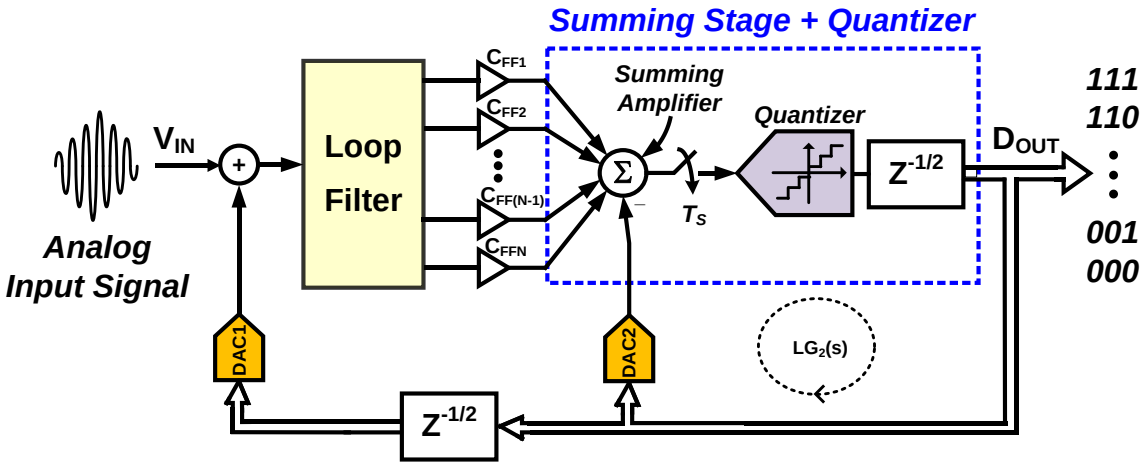


Fig. 3.1. A CT ΣΔ modulator with feed-forward (FF) compensation.

III.2.2. Voltage-mode summing and quantizer

The design of the summing stage is not trivial because it requires the use of resistors to implement the coefficients required in FF architectures. As depicted in Fig. 3.2, the loop gain is determined by the resistive feedback (R_F) as well as the load capacitance (C_L). It can be shown that the response of the summing amplifier to step current from DAC2 (I_{DAC2}) requires more than five loop time constants for a settling accuracy of 0.5%. For the case of a transconductance gain amplifier (transconductance of G_m) without any

internal pole (single stage amplifier), the loop gain is estimated as follows:

$$A_{Vloop}(\omega) = -\frac{\left(G_m - \frac{1}{R_F}\right)\beta R_{Leq}}{1 + sR_{Leq}C_L} \tag{3.1}$$

where $R_{Leq} = R_{OUT} \parallel R_F$; R_{OUT} is the output resistance of the summing amplifier and C_L is the load capacitance usually determined by the input capacitance of the quantizer. Flash quantizers require 2^N-1 comparators that increase C_L, which usually lowers the frequency of both output pole and the gain-bandwidth product (GBW). β is the feedback factor given by:

$$\beta = \frac{R_{in1} \| R_{in2} \| \cdots \| R_{inN} \| R_F}{R_F} \tag{3.2}$$

Accordingly, the DC loop gain is derived from (3.1) as

$$A_{V\_DC} = \left(G_m - \frac{1}{R_F}\right)\beta R_{Leq} \tag{3.3}$$

A_{V_DC} is required to be over 26 dB to ensure gain error due to an amplifier's finite gain within 5%. If the amplifier's slew rate limitations are ignored considering only the linear settling, then the settling time for 2% accuracy within $T_{clk}/2$ requires an amplifier gain-bandwidth product as dictated by:

$$GBW \cong \frac{\left(G_m - \frac{1}{R_F}\right)\beta}{C_L} = \frac{A_{V\_DC}}{R_{Leq}C_L} \geq \frac{4}{T_{clk}/2} \tag{3.4}$$

This result can also be expressed as follows:

$$R_{Leq}C_L \cong R_F C_L \leq \frac{T_{clk}A_{V\_DC}}{8} \tag{3.5}$$

As an example, the case f_{clk} = 500 MHz and a DC voltage gain of 26 dB demands $R_F C_L$ < 5ns. With a conservative value of β = 0.25, the required G_m/C_L should be over

$32/T_{clk}$. The realization of multiple coefficients (C_{FFi}) with values larger than unity results in smaller feedback factors, thereby demanding large transconductance values. For flash-based multi-bit quantizers the loading capacitance increases due to the large number of comparators and also due to the often large gate area per device required for maintaining small input offsets. The use of large resistors R_F is also limited by noise and area requirements. If some time is allocated for slew, then the required bandwidth is even higher because the time for linear settling is reduced. Fig. 3.3 displays the required transconductances with different feedback factors and loading capacitances for the case of 500 MHz clock frequency.

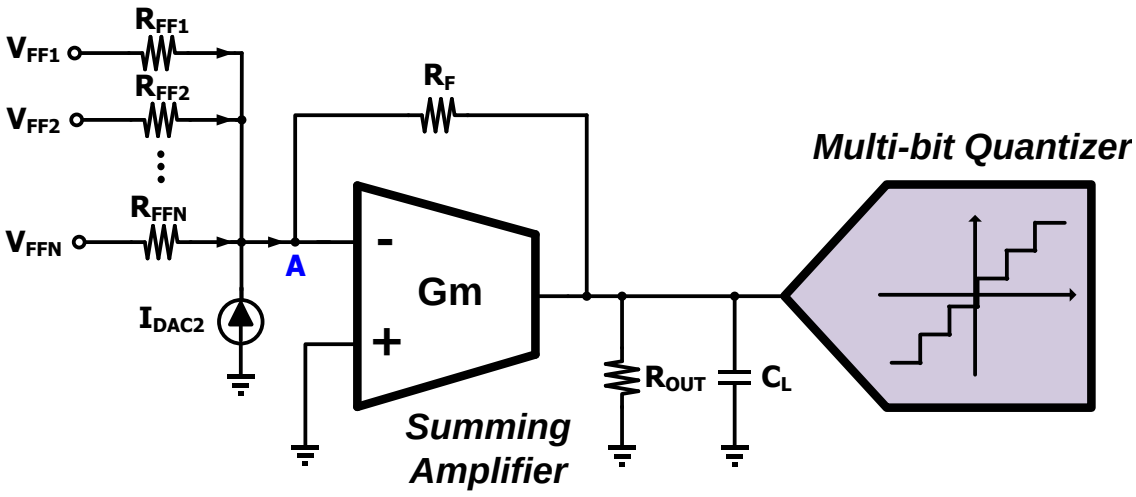


Fig. 3.2. Voltage-mode summing amplifier and quantizer.

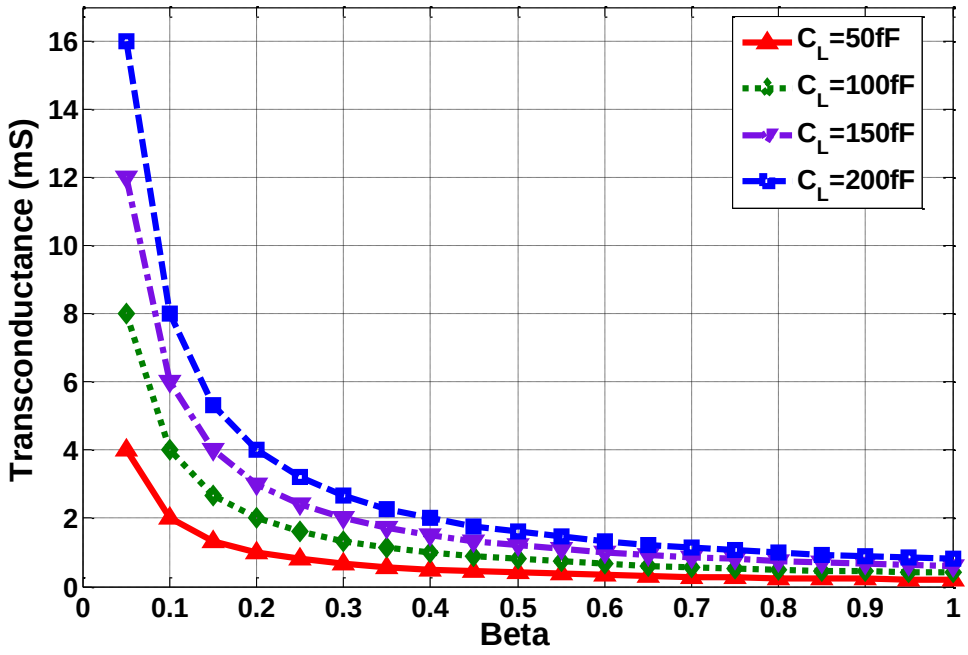


Fig. 3.3. Required transconductances (G_m) for the summing amplifier vs. β.

The required transconductance plotted in Fig. 3.3 as a function of the feedback factor with the different load capacitances may not be enough to guarantee the required DC gain in case of resistively loaded amplifiers. The minimum transconductance required may be dictated by the value of the DC loop gain requirement. For the case of 26 dB DC loop gain with a feedback factor of 0.25 where R_F = 2 KΩ, the required small signal transconductance (G_m) must be over 40 mA/V. Wide-bandwidth two-stage amplifiers may be needed in practical realizations. The above analysis reveals that the overall power consumption tends to be high when avoiding bandwidth limitations at the summing block. In other words, one of the main challenges during the design of low-power FF CT ΣΔ modulators is the high power consumption needed to meet the summing amplifier bandwidth requirement. Therefore, the replacement of the high-

power summing amplifier by a low-power current-mode flash ADC with built-in signal summation enables power savings while avoiding loop instability due to excess loop delay.

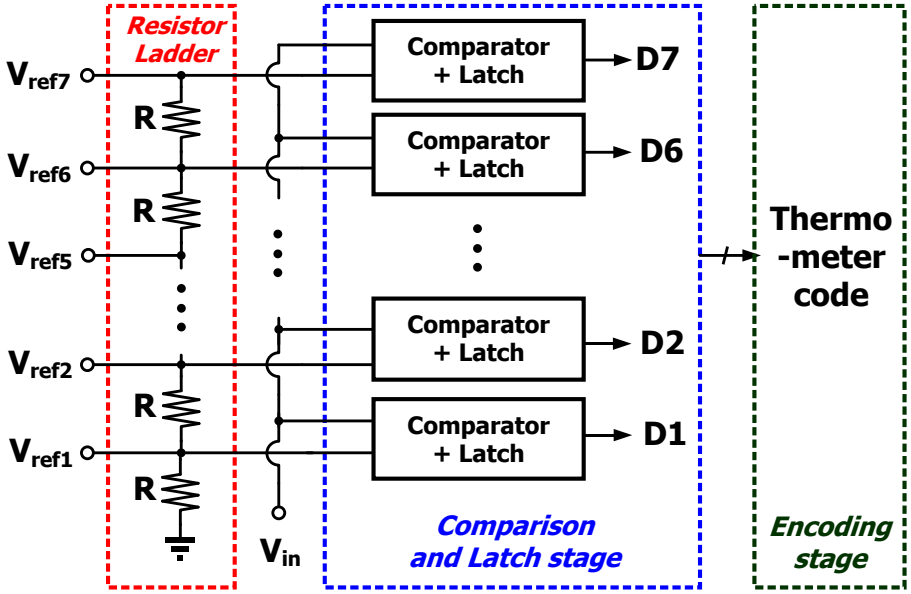


Fig. 3.4. Simplified schematic of the conventional single-ended 3-bit voltage-mode flash ADC.

Fig. 3.4 displays the single-ended version of a conventional 3-bit voltage-mode flash ADC, where the input signal V_{in} is compared to seven reference voltage levels from a resistor ladder using seven differential voltage comparators followed by latches. To minimize the impact of PVT variations, large area resistors (R) and intricate layout matching techniques are necessary to minimize reference voltage level shifts. Similarly, the input-offset voltages of the comparators become worse with increasing threshold voltage variations in deep submicron technologies. The use of larger transistor dimensions to alleviate mismatches would be counterproductive with regards to the maximum achievable speed that is limited by the layout-dependent parasitic

capacitances. In addition, to minimize the effects of the kickback noise, relatively small values are preferred for the resistors (R) at the expense of larger static power consumption.

Table III.1 shows the evolution of the typical transistor threshold voltage standard deviation $\{V_{TH}\}$ normalized by the threshold voltage (V_{TH}) for several technologies as reported in [26]. Voltage-mode flash ADCs generally suffer from the effects of the different offset voltages from device mismatches at each of the comparators. These variations cause quantizer nonlinearity errors. It should also be mentioned that the fully-differential voltage-mode flash ADC requires dual differential pairs at the input to compare the fully-differential input signal with the voltage references. As a result, the use of a pre-amplification stage is mandatory. Since voltage references derived from conventional resistor ladders are difficult to change after fabrication, several alternative methods have been proposed over the past decades to compensate for ADC nonlinearity errors due to process variations; several approaches have been reported to deal with these issues [27-31].

TABLE III.1
INTRA-DIE VARIABILITY (WITH MINIMUM DIMENSIONS) VS. CMOS TECHNOLOGY NODE

Technology	$\sigma\{V_{TH}\}/V_{TH}$
250 nm	4.7%
180 nm	5.8%
130 nm	8.2%
90 nm	9.3%
65 nm	10.7%
45 nm	16%

III.3. Proposed Summing and Flash ADC Architecture

III.3.1. Current-mode summing and quantizer

As visualized by the block diagram in Fig. 3.5, the proposed summing-quantizer topology consists of four stages: a current summing stage, a current comparison stage, a single-input comparator with SR latch, and an encoding stage. Within a CT ΣΔ ADC as the one shown in Fig. 3.1, the weighted current input signals from each of integrator in the loop filter and the DAC2 are summed at the current summing stage in Fig. 3.5.

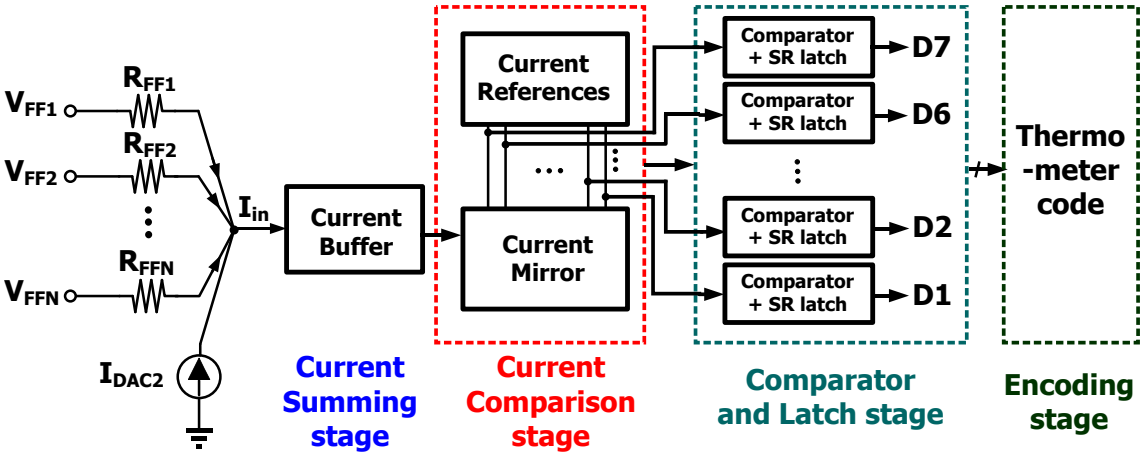


Fig. 3.5. Architecture of the summing block and flash ADC with current-mode operation: single-ended version.

III.3.2.Current summing and mirroring stage

The current summing stage is useful when input signals from different sources have to be combined before entering into the current-mode flash quantizer as required in FF CT ΣΔ modulators [14, 32]. Fig. 3.6 depicts how the current signals are summed at the low-impedance source node of a common-gate stage. The resulting AC current is replicated as many times as required by the current mirrors before it is delivered to the

high impedance nodes (V_{qN}) to resolve the individual bits. The replica currents are compared with a set of reference currents (not shown in this figure, but shown in detail in Fig. 3.10) to resolve the signal.

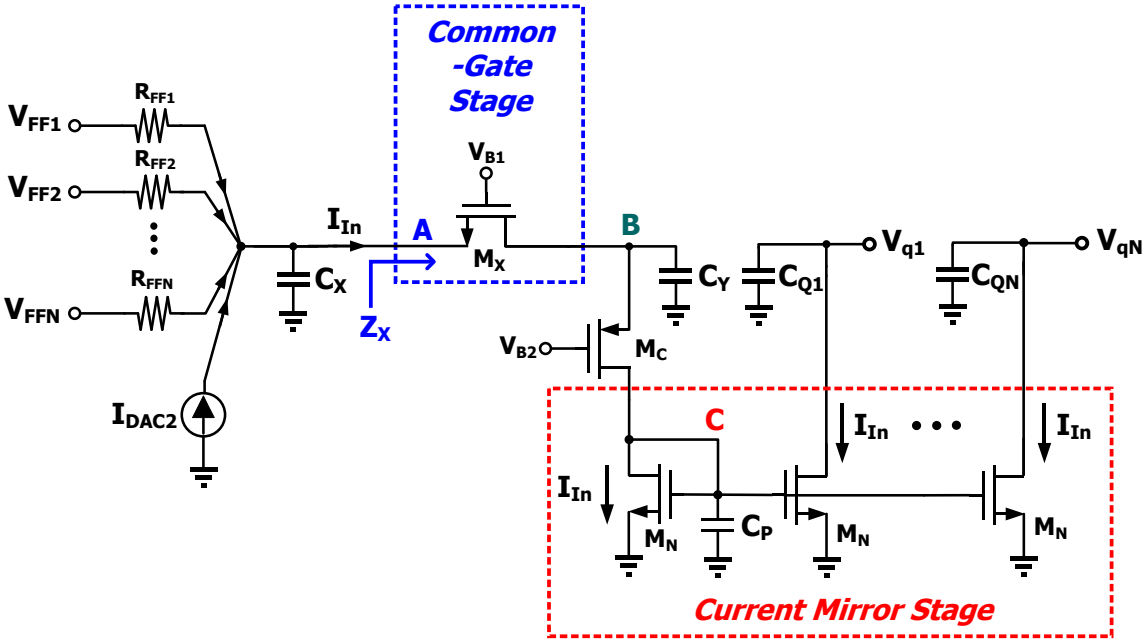


Fig. 3.6. Simplified schematic of the current-mode summing and mirroring stage.

Notice that I_{DAC2} (from the fast path of the CT ΣΔ modulator) could also be injected at node C, bypassing nodes A and B and to reduce the fast path delay. However, the bypass is not implemented in this prototype. The small signal transimpedance gain of the architecture can be expressed as follows:

$$\frac{V_{qN}}{I_{DAC2}}(s) \cong -\frac{R_{QN}}{\left(1+s\frac{C_X}{g_{mX}}\right)\left(1+s\frac{C_Y}{g_{mC}}\right)\left(1+s\frac{C_P}{g_{mN}}\right)\left(1+R_{QN}C_{QN}\right)} \tag{3.6}$$

where C_X, $C_{Y,}$ C_P and C_{QN} are the parasitic capacitances at the source node of the common-gate device (node A in Fig. 3.6), at the source node of folded cascode transistor

(node B in Fig. 3.6), at the gate of current mirror transistors (node C in Fig. 3.6) and at the comparison node (V_{qN} outputs in Fig. 3.6), respectively. R_{QN} is the equivalent resistance at node V_{qN}.

Fig. 3.7 displays the simulated frequency response from the source node of the common-gate stage to the comparison nodes (V_{qN}/I_{DAC2}) in the proposed current-mode architecture for the worse case.

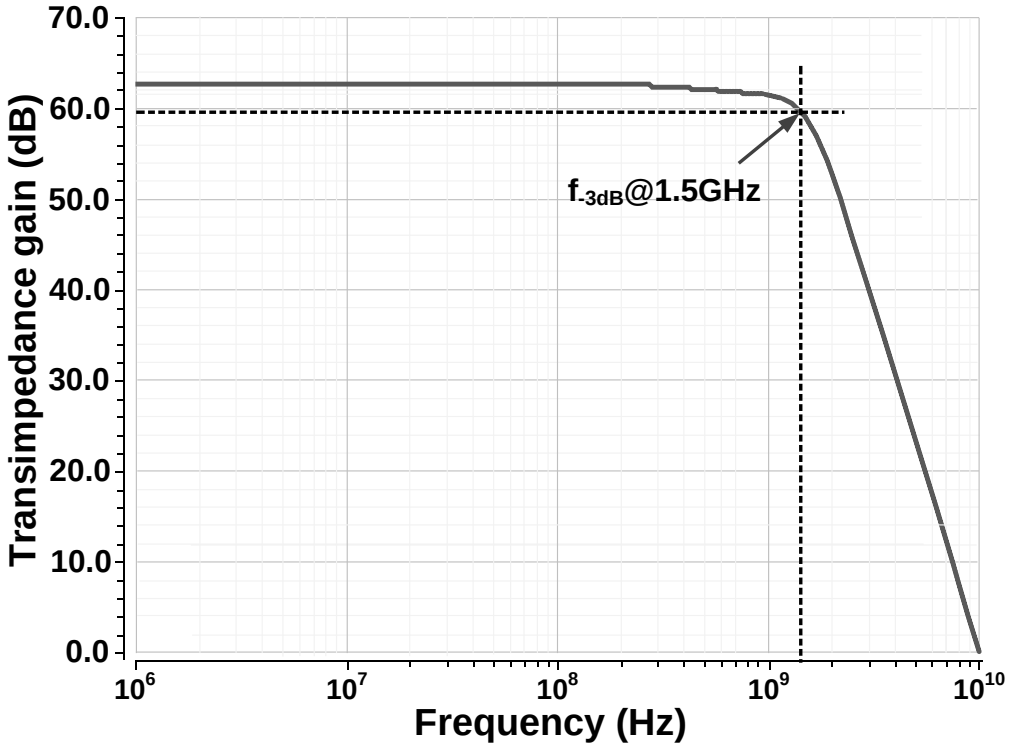


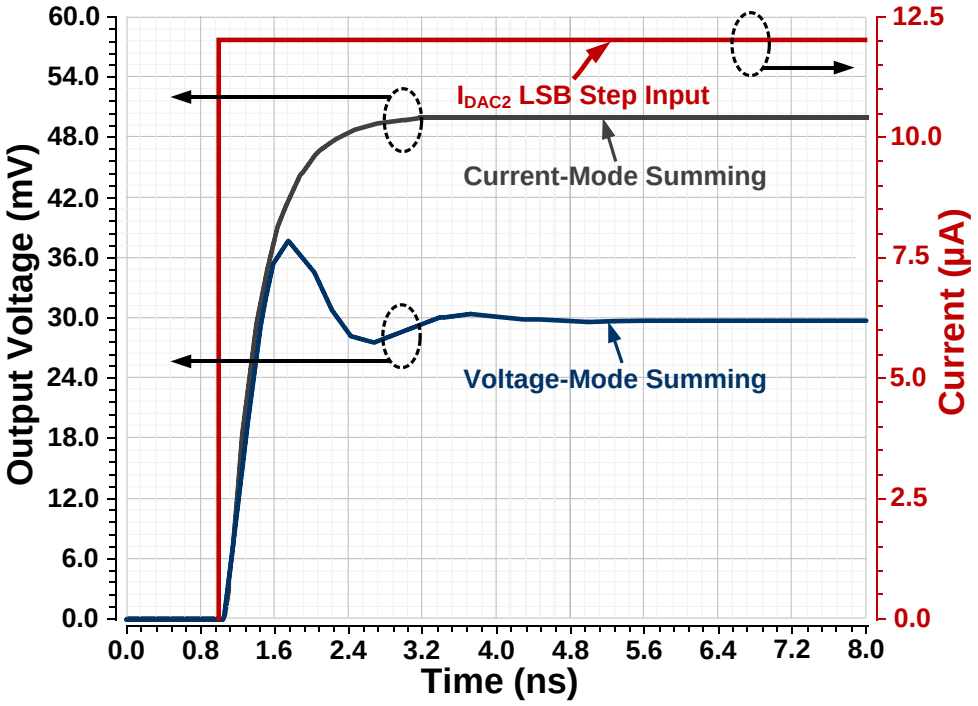
Fig. 3.7. Frequency response of the current summing and mirroring stage (V_{qN}/I_{DAC2} in Fig. 3.6).

In this simulation, the AC current was replicated seven times in the current mirror stage. The transimpedance gain of the current summing and mirroring (plotted in Fig. 3.7) was obtained by emulating the equivalent resistance due to the coefficients in the FF CT ΣΔ modulator architecture by connecting a 10 KΩ resistor between the source node of the common-gate stage and AC ground. The AC current input signal was applied at the source node of the common-gate stage and the voltage output is resolved at the comparison node. The -3 dB frequency of the current summing and mirroring stage is around 1.5 GHz. The roll-off is approximately 60 dB/decade, suggesting that three poles are close to 2 GHz. The total parasitic capacitance, C_P, at the gate of the current mirror transistors (M_N in Fig. 3.6) is one of the largest in the signal path because 2^N gate-source capacitances are loading node C as well as the C_{GD} capacitors and Miller effects due to the large signal swing at the V_{qN} outputs. On the other hand, C_{QN} is roughly 2^{N-1} times smaller than that of the conventional multi-bit voltage-mode quantizer. Nevertheless, the high impedance at the comparison node V_{qN} leads to another relevant pole. Furthermore, C_Y has a significant value due to the impact of the bias current transistors (not shown in the figure) required for the operation of the common-gate and folded cascode transistors. Therefore, the pole at node B is located close to the other two relevant poles. However, the pole at node A is usually located well beyond the frequencies of interest. Other non-dominant poles appear in the system due to the use of cascade transistors; see Fig. 10.

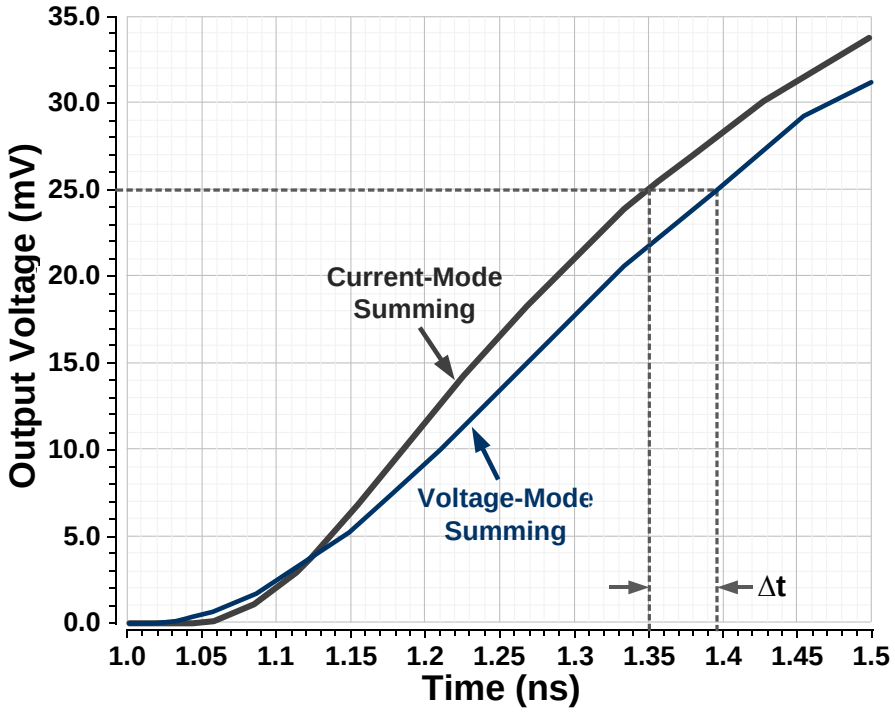
The delays introduced by the voltage-mode and proposed current-mode architectures were assessed based on step responses in differential implementation. A differential 12 μA current step (LSB) resembling the current due to DAC2 (I_{DAC2}) in Fig. 3.1 (with β =

0.25) was applied at the input node of the current summing stage (node A in Fig. 3.6) and at the negative input terminal of the summing amplifier (node A in Fig. 3.2) for voltage-mode operation. For the voltage-mode adder, the open-loop DC voltage gain and GBW were set at 14 dB (26 dB OTA gain -12 dB due to feedback factor) and 2 GHz, respectively. The feedback resistor R_F (see Fig. 3.2) was set at 10 KΩ while C_L = 300 fF. The amplifier power consumption is 6.6 mW.

Fig. 3.8 displays the step response of both voltage and current mode cases. The current-mode approach provides higher gain, mainly due to the fact that it is terminated with a high-impedance node. The zoomed-in step responses of both cases around the voltage sensitivity of the comparators (around 25 mV for this design) show that the output of the current-mode solution reaches $V_{LSB}/4$ within 0.35 ns while the voltage-mode solution reaches this level in 0.40 ns. These results reveal that the current-mode design outperforms the voltage-mode architecture in terms of speed. The key simulation results for both topologies are summarized in Table III.2. The most remarkable advantage of the current-mode approach is that it consumes 53% less power and at the same time offers superior performance. In the voltage mode case, additional power should be added to account for the reference voltages generator as well as the dual differential pair required at the input of each comparator.



(a)



(b)

Fig. 3.8. (a) Differential step response of the voltage-mode summing and current summing and mirroring stage, and (b) the zoomed-in differential step response view of both cases from 1 ns to 1.5 ns.

TABLE III.2
VOLTAGE-MODE SUMMING VS. CURRENT-MODE SUMMING

	Voltage-Mode Summing	Current-Mode Summing
Technology	90 nm CMOS	90 nm CMOS
Power	6.6 mW*	3.34 mW**
Input referred integrated noise (in 20 MHz)	31.2 μV	39 μV
Delay (@$V_{LSB/4}$)	0.396 ns	0.35 ns

* Power consumption of the summing amplifier only.
** Power consumption includes common-gate (CG) stage, Gm-boosting block and current mirroring stages.

III.3.3. Input impedance of the current-mode adder

In order to lower the effective impedance (Z_X) at the summing node, the effective transconductance of the CG device (M_X) was increased with a G_m-boosting scheme [33]. Z_X can then be approximated as:

$$Z_X \cong \frac{1}{g_{mX}(1 + A_V(s))} \tag{3.7}$$

where g_{mX} = 4.2 mS is the transconductance of transistor M_X and $A_V(s)$ is the gain of the amplifier in Fig. 3.10.

As shown in Fig. 3.9, the simulated effective impedance Z_X is below 50 Ω up to 1.2 GHz in this design. In contrast, the equivalent impedance of the biasing current source (Z_{IB1} in Fig. 3.10) is approximately 31.5 KΩ, whose effect is negligible on the accuracy of the current adder. The overall input resistance due to the FF coefficients is usually more than 1 KΩ, leading to a static summing error under 5% up to 1 GHz, which can be tolerated in most of the ΣΔ modulators.

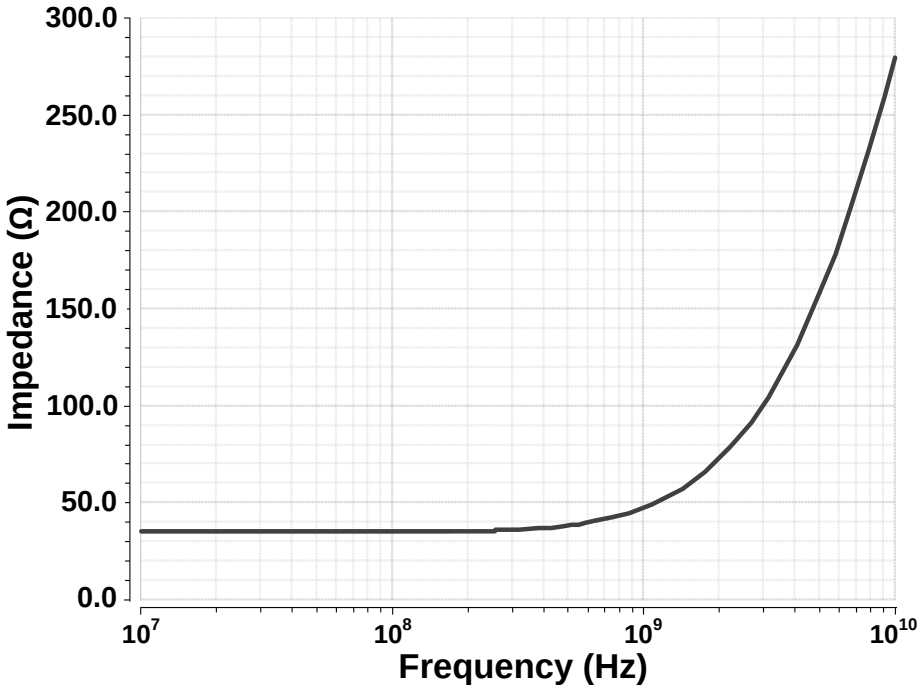


Fig. 3.9. Effective impedance at the summing node vs. frequency.

III.3.4. Current comparison stage

Fig. 3.10 displays the schematic of the proposed current-mode adder-quantizer. The summed input signal is transferred to each comparison branch through 1:1 cascode current mirrors (M_{N1}), and the output currents are then compared with the thermometer-weighted reference currents to resolve the resulting bits. For the 40 µA single-ended full-scale 7-level current-mode quantizer (equivalent to 0.4 V over a 10 KΩ resistor in single-ended voltage-mode quantizers), the least significant bit (LSB) reference current (I_{q_REFN}) is approximately 6 µA. The current differences ($I_{qN} = I_{IN\_AC} - I_{q\_REFN}$) between the input signal and the references are converted to voltage step responses at the high-impedance input nodes of the comparators (V_{qN}) after the reset switches are opened. The reset switches help in removing the previous initial conditions at the comparison nodes

and relax the specifications of the comparator. In each branch, the voltage difference is processed by the next stage comprised of a set of comparators followed by SR latches. Because the comparison nodes are high impedance cascode nodes, a reset step is performed after comparing the input signal with a reference current in order to reduce the time required to resolve the signal during each clock cycle. Reset switches are used to set the common-mode voltage around the mid-supply level to make an equally fast comparison regardless of a node's voltage level in the previous comparison phase. The StrongARM comparator from [34] was employed.

Major advantages of the current-mode approach over the conventional voltage-mode flash quantizer are: i) a high impedance node is employed to compare the AC current and the weighted reference current, which simplifies the comparator design because the pre-amplification stage can be avoided; ii) the comparators resolve the sign with a single differential configuration while the voltage-mode architecture requires a dual differential pair input to compare the fully-differential input with V_{ref+} and V_{ref-}; iii) the comparators resolve the signals around the common-mode voltage; iv) an additional resistor string is not needed to generate the reference voltages, which would demand extra buffers to drive the resistor string as well as more power and a larger silicon area.

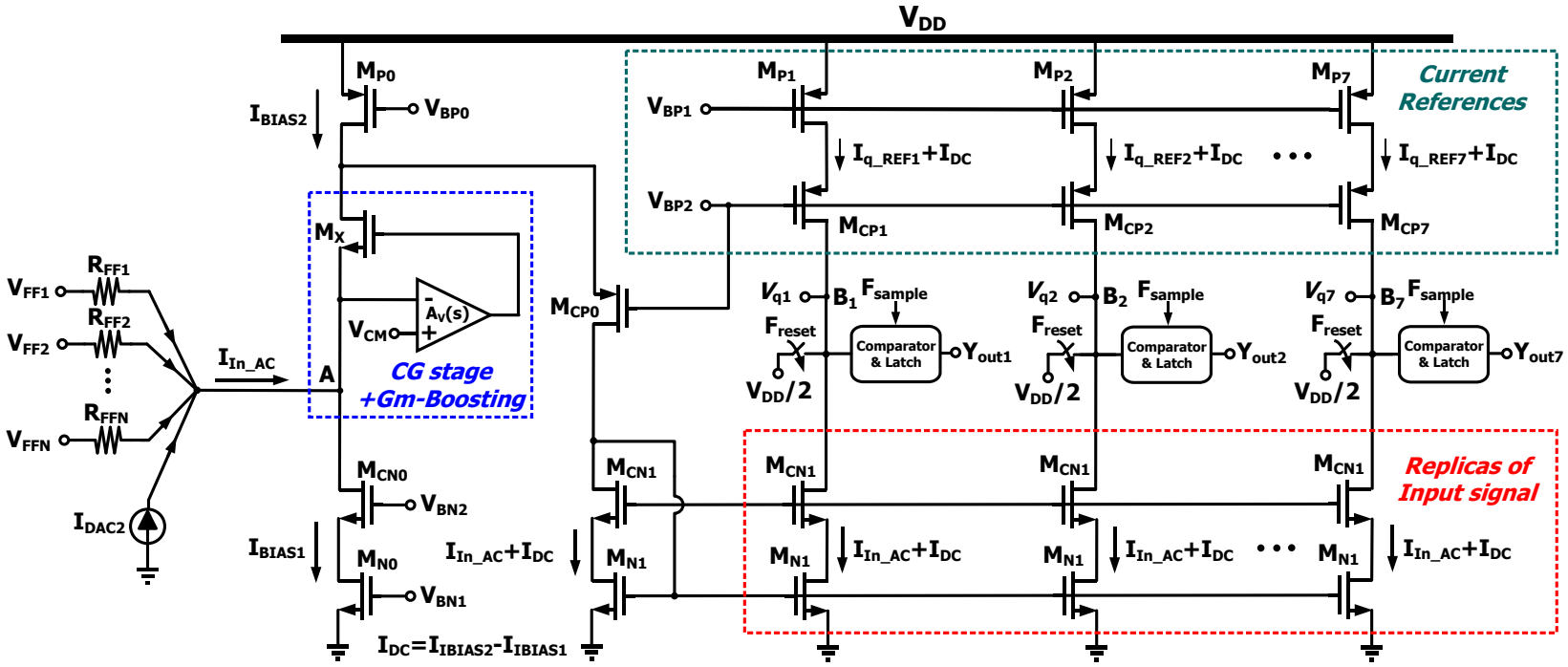


Fig. 3.10. Schematic of the proposed current-mode flash ADC with summing stage (single-ended equivalent of the differential circuit).

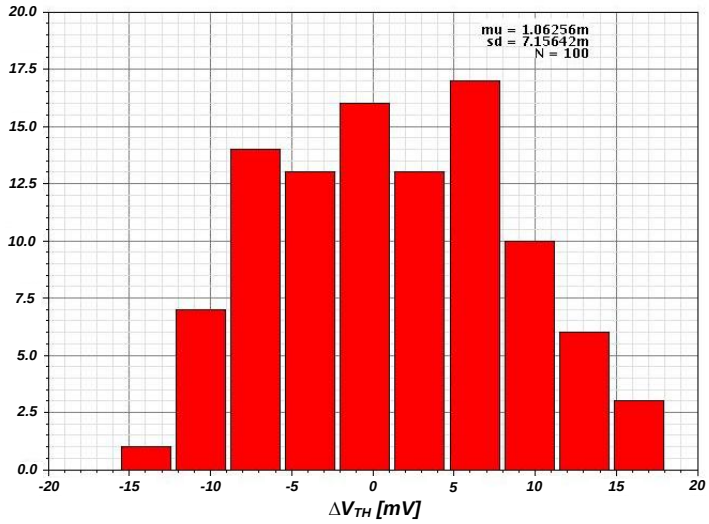
III.3.5. PVT variations

The core of the proposed current-mode flash ADC involves a comparison between the replica of input signal and reference currents. The mismatches within the current mirrors must be carefully evaluated during the design because several parameters depend on PVT variations, such as input offsets, threshold voltages, and transconductance values. First of all, there is a tradeoff between the mismatches and achievable speed based on the dimensions of the current mirror transistors (M_{N1}). The current mirror transistors must be small to avoid extra delay due to parasitic capacitances at the current mirror node. On the contrary, input offset minimization requires large transistors [35] to minimize mismatches, which implies large parasitic capacitances and decreased effective high-frequency transconductances. Therefore, the input offset assessment for M_{N1} in the comparison stage was performed using Monte Carlo simulations to identify the smallest acceptable device dimensions.

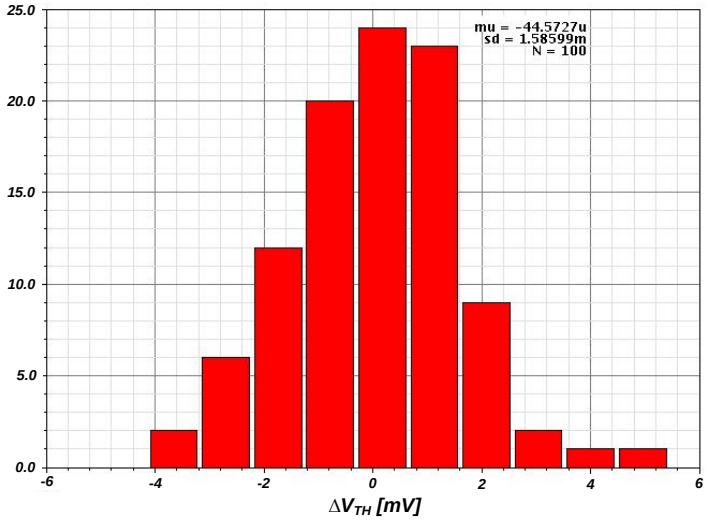
The histograms obtained from 100 Monte Carlo runs at 50 °C are shown in Fig. 3.11. If the current sources are laid out independently (unmatched case), the expected standard deviation for threshold voltage variations is around 7.16 mV. Assuming that the current transistors are matched with an inter-digitized and common-centroid layout scheme, the expected standard deviation is around 1.6 mV from Monte Carlo simulations employing correlation coefficients of 0.95 based on the procedure described in [36]. The effective input offset voltage of the current mirrors can be obtained by summation of two variances [37]:

$$V_{offset} = \sqrt{\left(\sigma_{offset\_M_{N1}(input)}\right)^2 + \left(\sigma_{offset\_M_{N1}(mirrored)}\right)^2} = \sqrt{2\left(V_{offset\_M_{N1}}\right)^2} \qquad (3.8)$$

Thus, the estimated input offset voltage of the current mirror in the comparison stage is expected to be around 6.7 mV (3 sigma of V_{offset}).



(a)



(b)

Fig. 3.11. Histogram (100 runs) of the threshold voltage differences of the current mirror devices (M_{N1} in Fig. 3.10) from Monte Carlo simulations: (a) without matched transistors in the layout, and (b) with matched transistors in the layout.

This offset causes static errors in the comparator. However, as described for the current-mode quantizer in [37], the proposed current-mode flash ADC was designed to allow reference currents tuning. To make a meaningful comparison, current mismatch is normalized to the average value:

$$\frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{W/L} - \frac{2\Delta V_{TH}}{V_{GS} - V_{TH}} \tag{3.9}$$

Therefore, the effect of threshold mismatch on the currents can be reduced by maximizing the overdrive voltage.

Equal common-mode voltage levels are ensured in the differential version of the current-mode flash ADC in Fig. 3.10 because the comparisons for all cases are made around the reset level of $V_{DD}/2$. Current-mode operation with reset switches is compatible with new CMOS technologies since there is a clear benefit from high switching speed and the reduction of power consumption as a result of technology scaling. Another scaling consideration is that ADC references are currents instead of voltages, and then the comparisons are easily implemented. Additionally, power supply limitations due to scaling have significantly less impact on the current-mode flash architecture performance in comparison to voltage-mode flash architectures that suffer from voltage headroom restrictions during the generation of the reference voltages with resistor ladders.

III.4. Chip Measurement Results

A prototype current-mode adder-quantizer was designed and fabricated in 90 nm CMOS technology to be utilized as a quantizer with summing stage in FF CT ΣΔ modulators. The differential full-scale voltage signal is set at 0.8 V_{pp} and the differential feedback current from DAC2 is 80 μA_{pp}. While characterizing the proposed current-mode adder-quantizer, the input current signal was generated externally through a voltage source and an off-chip series resistor of 10 KΩ connected to the summing node through the bond-wire inductor.

III.4.1. SNDR and SFDR versus input frequency

Dynamic performance of the ADC was evaluated with measurements at different clock frequencies up to 1.48 GHz. The input frequency has been normalized by the sampling frequency to facilitate the comparison of the results. Since CT ΣΔ modulators typically use oversampling ratios, the ADC was assessed with f_{in}/f_{clk} ratios between 0.01 and 0.1. Fig. 3.12 displays the measured SNDR for various normalized input frequencies while sweeping the clock frequency from 250 MHz up to 1.48 GHz. According to these results, the SNDR is higher than 17 dB over the entire f_{in}/f_{clk} range even in the case the input signal frequency is 150 MHz.

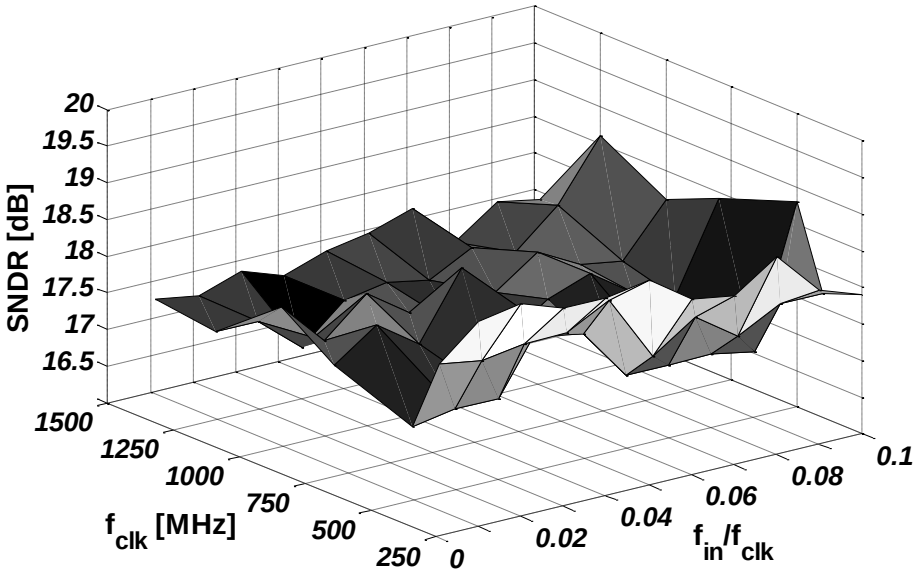


Fig. 3.12. SNDR vs. input frequency at different clock frequencies.

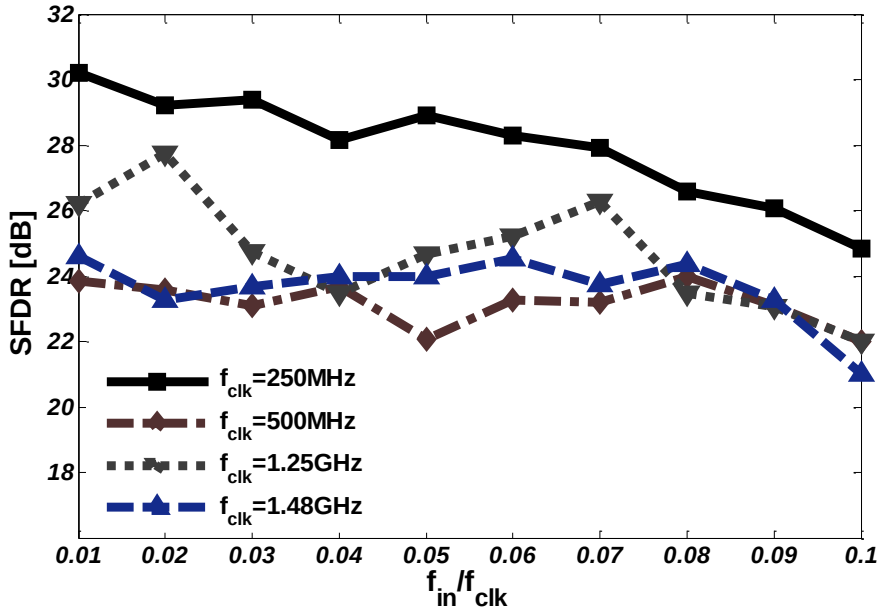


Fig. 3.13. SFDR vs. input frequency at different clock frequencies.

Fig. 3.13 displays the measured spurious-free dynamic range (SFDR) of the prototype ADC for a number of clock frequencies vs. input frequency. The worst-case SFDR is 21 dB when the clock and input frequency are 1.48 GHz and 150 MHz. The SFDR is 24 dB over the entire 20 MHz signal bandwidth which is a popular bandwidth for several wireless applications. For this prototype, quantizer performance is within 4 dB variation up to 1.48 GHz clock frequency.

III.4.2. ENOB versus clock frequency

Fig. 3.14 displays the measured effective number of bit (ENOB) at different clock frequencies. The current-mode prototype achieves beyond 2.6 bits up to 2 GHz clock frequency for a 10 MHz full-scale input signal. The analog portion of the current-mode flash ADC core consumes 3.34 mW, while the digital circuitry including clock buffer consumes 8.94 mW. Based on the Figure-of-Merit (FoM) defined in (3.10), the ADC achieves 1.01 pJ/conversion-step with a 10 MHz input signal operating at 2 GHz clock frequency, and 0.27 pJ/conversion-step when only the analog power is accounted for.

$$\text{FoM} = \frac{Power}{2^{ENOB} \times f_{clk}} \tag{3.10}$$

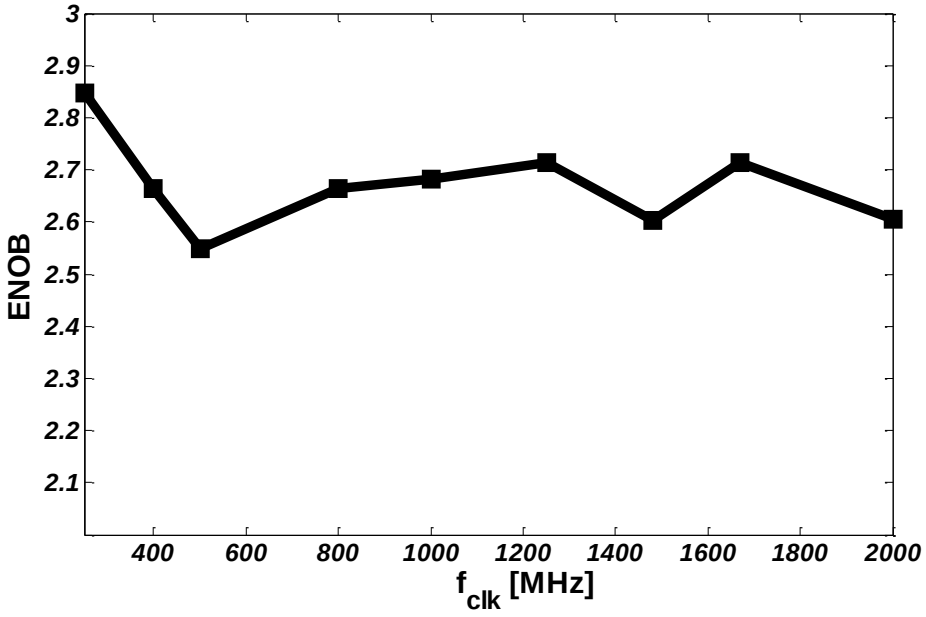
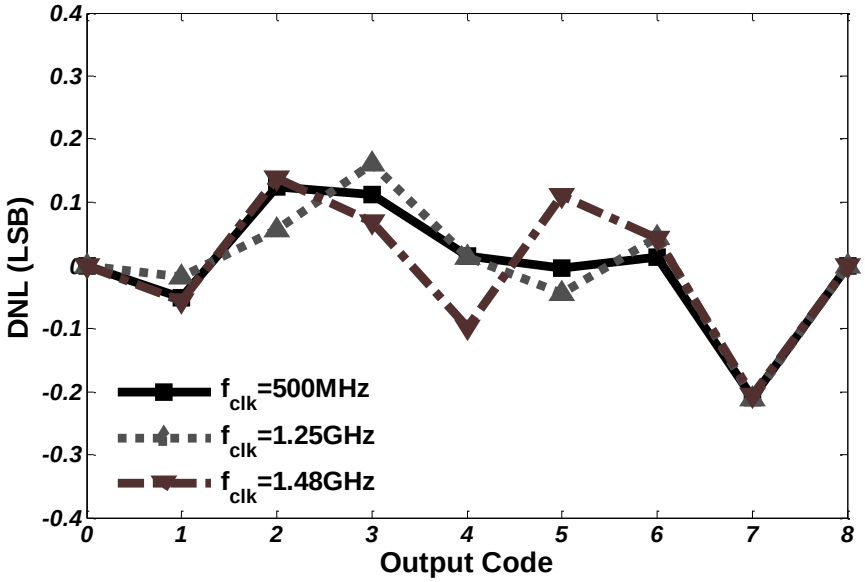


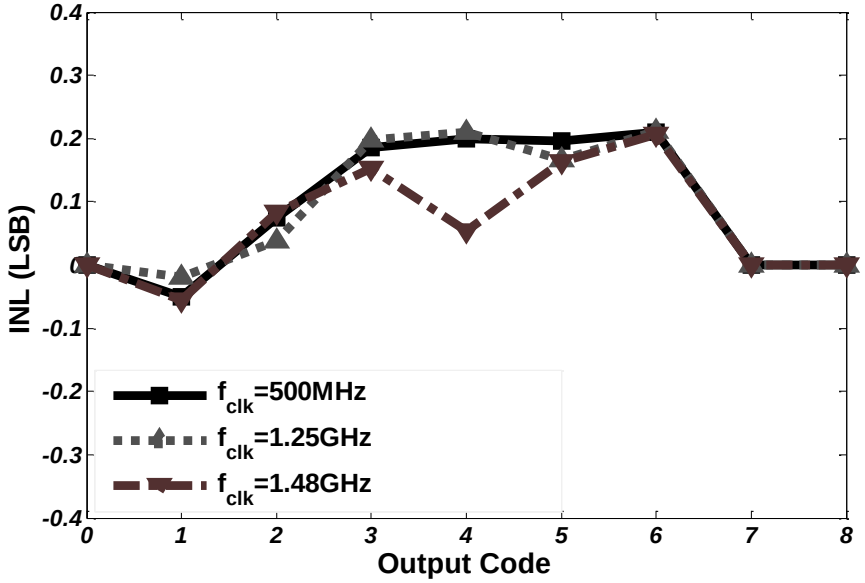
Fig. 3.14. ENOB vs. clock frequency with a full-scale 10 MHz input signal.

III.4.3. DNL and INL

The nonlinearity of the fully-differential 3-bit current-mode flash ADC was assessed at three different clock frequencies: 500 MHz, 1.25 GHz, and 1.48 GHz. Fig. 3.15 shows the measured DNL and INL from a ramp test with a full-scale (FS) differential input between -0.4 V and 0.4 V. Static offset and gain errors have been nulled in the DNL and INL evaluation. The maximum DNL and INL errors at 1.48 GHz clock frequency are within ±0.21 LSB.



(a)



(b)

Fig. 3.15. Experimental results for the fully-differential current-mode quantizer. (a) DNL, and (b) INL of the ADC at different clock frequencies. (Offset and gain error are adjusted to zero.)

III.4.4. Output spectrum

The FFT output spectrums obtained with 8192 samples and a 125 MHz sinusoidal input signal at 1.25 GHz clock frequency is displayed in Fig. 3.16. The measured SNDR for this frequency is 18.6 dB, respectively. The measured SFDR is equal to 22 dB for the aforementioned testing condition.

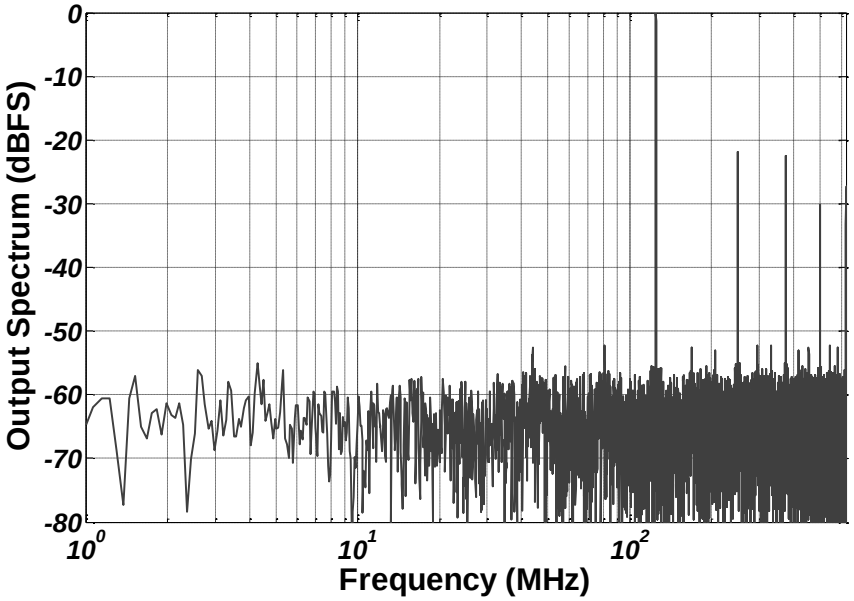


Fig. 3.16. Output spectrum for 125 MHz input at 1.25 GHz clock frequency.

Fig. 3.17 displays the chip microphotograph of the current-mode flash ADC in 90 nm CMOS technology. The ADC area including bias circuitry is 0.0276 mm^2, and the thermometer-to-binary encoder occupies 0.0072 mm^2. Even though this architecture is intended to be used as an adder-quantizer in a CT ΣΔ modulator instead of a standalone ADC, the proposed current-mode ADC achieves the second lowest FoM after the 6-bits flash ADC reported in [30]. The power consumption in voltage-mode quantizers is even

less competitive if, as previously described, the preamplifier required for reducing the kickback noise in the voltage-mode comparators and the power required for the generation of the voltage references are included in the comparison. Even if these blocks are not considered, the proposed approach occupies significantly less die area and achieves competitive linearity performance.

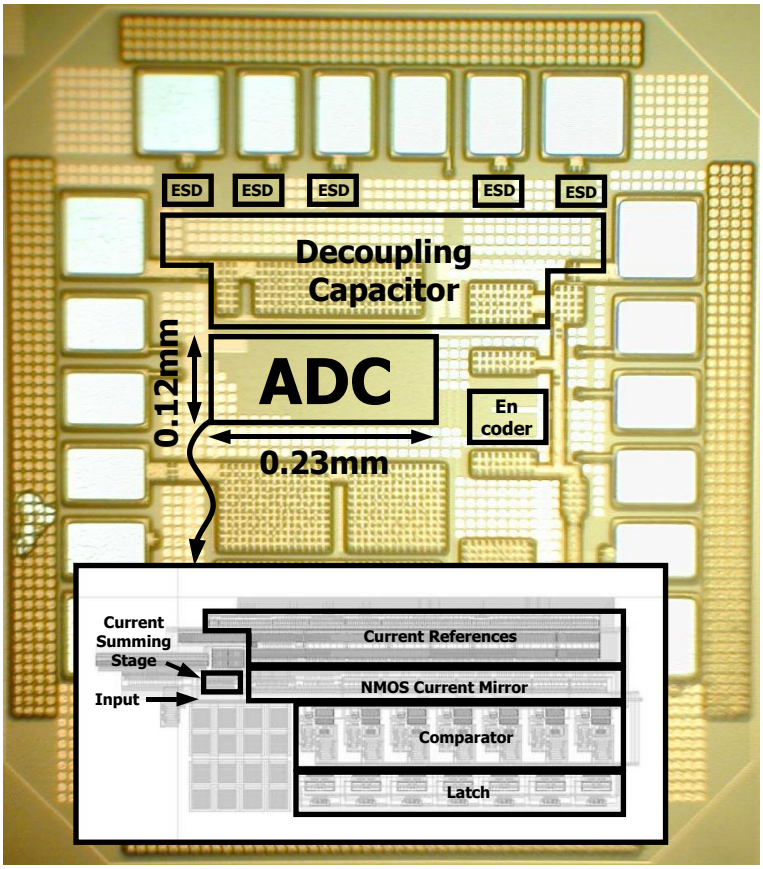


Fig. 3.17. Chip microphotograph of the prototype current-mode flash ADC.

Table III.3 compares the proposed current-mode adder-quantizer to previously reported adders and quantizers in CT ΣΔ modulators, showing that the current-mode implementation consumes the lowest power with the highest operating speed.

TABLE III.3

PERFORMANCE SUMMARY OF THE PROPOSED CURRENT-MODE ADDER-QUANTIZER AND COMPARISON WITH PRIOR ADDERS AND QUANTIZERS IN CT ΣΔ MODULATORS

	[32]		[38]		This Work	
Technology	180 nm CMOS		180 nm CMOS		90 nm CMOS	
Supply voltage	1.8 V		1.8 V		1.2 V	
Quantizer Resolution	3 bits		4 bits		3 bits	
Sampling rate	400 MHz		800 MHz		up to 2 GHz	
Input range	0.4 V_{pp}		3 V_{pp}		80 μA_{pp} (equivalent to 0.8 V_{pp})	
Power	Adder*	10 mW	Adder*	8.5 mW	Adder	1.1 mW
	Voltage-Mode Quantizer**	24 mW	Voltage-Mode Quantizer	N/A	Current-Mode Quantizer	3.04 mW

* Power consumption of the summing amplifier only.

** 3-bit two-step Flash ADC.

TABLE III.4

PERFORMANCE SUMMARY OF THE PROPOSED CURRENT-MODE FLASH ADC AND COMPARISON WITH PRIOR WORKS

	[28] *		[29] **	[30]	This Work	
Technology	180 nm CMOS		130 nm CMOS	90 nm CMOS	90 nm CMOS	
Supply voltage	Analog: 1.8 V Digital: 2.1-2.5 V		1.2 V	Analog: 1.2 V Digital: 1.5 V	1.2 V	
Resolution	4 bits		5 bits	6 bits	3 bits	
Sampling rate	up to 4 GHz		up to 3.2 GHz	up to 4.1 GHz	up to 2 GHz	
Input range	0.92 V_{pp}		0.4 V_{pp}	0.8 V_{pp}	80 μA_{pp} (equivalent to 0.8 V_{pp})	
Power	Analog	78 mW	120 mW	76 mW	Analog	3.34 mW
	Digital (Including Clock Buffer)	530 mW			Digital (Including Clock Buffer)	8.94 mW
DNL (After Calibration)	- 0.14 LSB ~ 0.15 LSB (f_{clk} = 4 GHz)		- 0.24 LSB ~ 0.18 LSB (f_{clk} = 3.2 GHz)	- 0.48 LSB ~ 0.49 LSB (f_{clk} = 4.1 GHz)	- 0.206LSB ~ 0.138LSB (f_{clk}=1.48GHz)	
INL (After Calibration)	- 0.24 LSB ~ 0.20 LSB (f_{clk} = 4 GHz)		- 0.29 LSB ~ 0.39 LSB (f_{clk} = 3.2 GHz)	- 0.74 LSB ~ 0.74 LSB (f_{clk} = 4.1 GHz)	- 0.056 LSB ~ 0.206 LSB (f_{clk} = 1.48 GHz)	
FoM (pJ/conversion-step)	10.25 (f_{in} = 10 MHz, f_{clk} = 4 GHz)		3.07 (f_{clk} = 2 GHz) 4.3 (f_{clk} = 3.2 GHz)	0.625 (f_{clk} = 4.1 GHz)	1.01 (f_{in} = 10 MHz, f_{clk} = 2 GHz)	
ENOB	3.89 bits (f_{in} = 10 MHz, f_{clk} = 4 GHz) 3.48 bits (f_{in} = 100 MHz, f_{clk} = 4 GHz) 3.47 bits (f_{in} = 800 MHz, f_{clk} = 3.4 GHz)		4.44 bits (f_{clk} = 2 GHz) 4.54 bits (f_{clk} = 3.2 GHz)	4.89 bits (f_{in} = 2.02 GHz, f_{clk} = 4.1 GHz)	2.6 bits (f_{in} = 10 MHz, f_{clk} = 1.48 GHz) 2.6 bits (f_{in} = 44.4 MHz, f_{clk} = 1.48 GHz) 2.54 bits (f_{in} = 118.4 MHz, f_{clk}=1.48 GHz)	
Area	0.88 mm^2 (excluding resistor ladder)		0.18 mm^2	0.38 mm^2 (excluding I/Os and calibration logic)	ADC: 0.0276 mm^2 (excluding encoder)	

* Includes power consumptions for analog circuitry and digital encoder. For the FoM calculation, the digital power consumption for 4GHz clock frequency

** Power consumption of output buffer was not included.

The performance of the proposed ADC is summarized and compared to previously reported results in Table III.4.

III.5. Summarizing Remarks

A 3-bit current-mode adder-flash ADC for operation up to 2 GHz to be used in FF CT ΣΔ modulators has been presented. The current-mode based scheme lessens existing problems associated with voltage-mode flash ADCs, which are mainly related to voltage headroom restrictions, speed of operation, offsets, and power efficiency of the latches. Furthermore, the proposed current-mode flash ADC with efficient current summing stage is an efficient alternative to the power-hungry summing amplifiers required in FF CT ΣΔ modulators, leading to more robust and faster solutions with up to 53% power savings. The presented flash ADC architecture was constructed with the aim to take advantage of technology scaling by relying on the speed of reset switches while minimizing the impact of supply voltage reductions. The proposed architecture can be easily extended to quantizers with higher number of bits operating beyond the GHz clock frequency range.

IV. HIGH POWER SUPPLY REJECTION (PSR) EXTERNAL CAPACITOR-LESS LOW DROP-OUT (LDO) REGULATOR

IV.1. Background

Due to the rapidly increasing demand for portable devices such as smart-phones, tablet PCs and wireless handsets, the use of efficient power management systems to prolong the battery life is becoming of primary importance. With the growing trends of complete SoC design, the entire power management system should be integrated into a single-chip solution. The conventional power management system consists of a highly efficient switching power converter (SWPC) cascaded with a low-noise power-efficient LDO regulator, as depicted in Fig. 4.1. To provide good isolation between the SWPC noise output and the highly noise-sensitive RF and/or high-performance analog blocks, the LDO's ability to reject the power supply noise is becoming a very demanding specification.

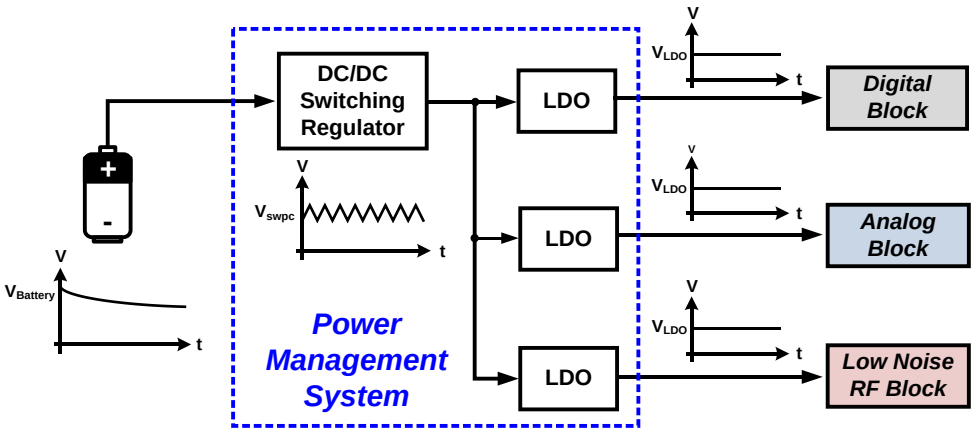


Fig. 4.1. Typical power management system for SoC applications.

With the current technology trends, the SWPC operating frequencies are increasing to allow higher level of integration [39]. Since the output ripples at high frequencies appear at the output of the SWPC, the LDO regulator must have a high PSR for frequencies up to a few megahertz with as few off-chip components as possible to reduce die/board area and cost [40]. The issue is complex since the supply noise leakage changes with the loading conditions.

IV.2. Existing Solutions

Several techniques to improve the power supply rejection of LDOs have been proposed [41]-[45]. These techniques involve: i) a feed-forward ripple cancellation path employing fixed gain that is not able to track supply noise leakage under all operating conditions [41] or an adaptive scheme [42], where the practical feasibility of the approaches is limited because bulky external output capacitors are employed (4 µF [41] and 6 µF [42]), which improve performance but increase the bill of material - in [43] bulk driven techniques are used to improve low-frequency PSR; ii) a feed-forward supply-noise cancellation (FFNC) method employing calibration techniques without an external output capacitor [44] which is an approach that is very sensitive to the control voltage of the bias current source that determines the gain of the feed-forward amplifier - hence, it cannot be a robust PSR enhancement solution for the different loading conditions under process-voltage-temperature (PVT) variations; iii) another technique provides additional isolation employing an NMOS cascade transistor with a clean gate voltage [45].

The aforementioned techniques [41]-[44] improve the high frequency PSR by cancelling the supply noise induced current before it appears at the load. To provide a suitable solution for SoC applications, we introduce an external capacitor-less LDO with a PSR enhancement technique that tracks and compensates the supply noise up to high frequencies without the use of bulky external capacitors. It is shown that the leakage of the supply noise has three main components, and all of them could be tracked; however, in this prototype only the most relevant one in the range 100 KHz - 10 MHz is tracked.

IV.3. Fundamental PSR Limitations of Conventional LDOs

LDOs typically have fundamental PSR limitations at high frequencies due to the existence of several paths between the noisy supply and the LDO output. Fig. 4.2 shows those paths for a conventional LDO architecture where supply noise couples to the output of the LDO as follows: i) Path 1: noise modulation of the gate voltage through the gate-source capacitance, C_{gs}, converted into current by the transconductance of the pass transistor, g_{mp}; ii) Path 2: through the error amplifier; iii) Path 3: noise coupled through the finite output impedance of the pass transistor, r_{dsp} and C_{db}. For the conventional LDO depicted in Fig. 4.2, the output voltage (V_{OUT}) due to power supply (V_{dd}) noise can be expressed as:

$$V_{OUT}(s) \cong \frac{1}{1 + \text{Loop Gain}(s)}\left\{\left(i_{d\_Cgs}(s) + i_{d\_EA}(s) + i_{d\_r_{dsp}\&Cdb}(s)\right) Z_{Load}\right\} \quad (4.1)$$

where $i_{d\_Cgs}(s)$, $i_{d\_EA}(s)$, and $i_{d\_rdsp\&Cdb}(s)$ are the LDO open-loop supply noise-induced currents due to the Path 1, Path 2, and Path 3, respectively. The effects of all these V_{dd}

noise components are minimized by increasing the magnitude of the loop gain, provided that loop stability can be guaranteed.

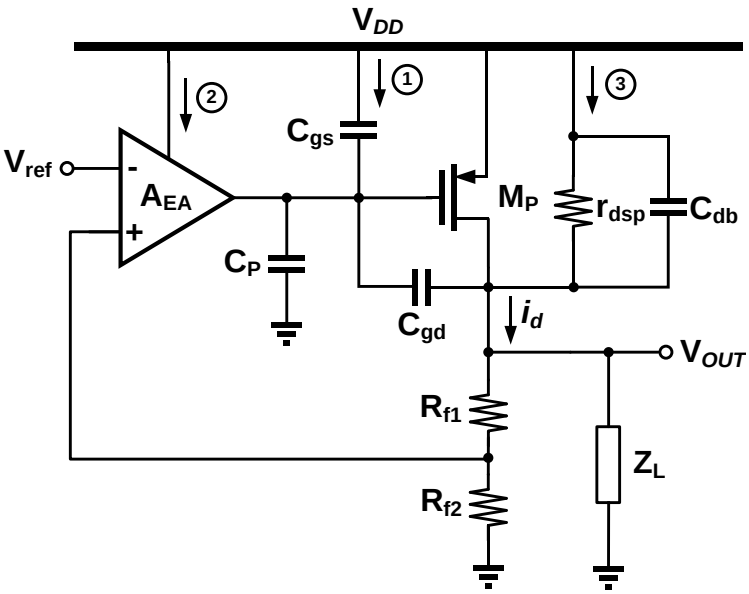


Fig. 4.2. Input to output power supply ripple paths in conventional LDOs.

The open-loop schematic of a conventional external capacitor-less LDO architecture employing a two-stage error amplifier and frequency compensation [46] is depicted in Fig. 4.3. To ease the analysis, the floating capacitor C_{gd} is represented by four circuit elements as shown in Fig. 4.3(b) [48]. The loop gain can then be expressed as

$$\text{Loop Gain}(s) = \left(g_{mp} - sC_{gd}\right)\left\{\frac{R_G R_{LT}}{(1+sR_G C_G)(1+sR_{LT}C_{LT})}\right\}\left\{\left(\frac{\alpha g_{m1} g_{m2} R_{O1}}{1+sR_{O1}C_{O1}}\right) + s\left(C_C + C_{gd}\right)\right\} \quad (4.2)$$

where $\alpha = R_{f2}/(R_{f1}+R_{f2})$ is the feedback factor and $R_{LT} = R_L||(R_{f1}+R_{f2})||r_{dsp}$. C_C is the frequency compensation capacitor for loop stability, which is usually implemented with an impedance scaling technique [46-47], [49]. High DC loop gain reduces the low-frequency V_{dd} noise at the LDO output according to (4.1). Since the loop gain decreases

at higher frequencies due to the internal poles, the PSR performance degrades at medium and high frequencies.

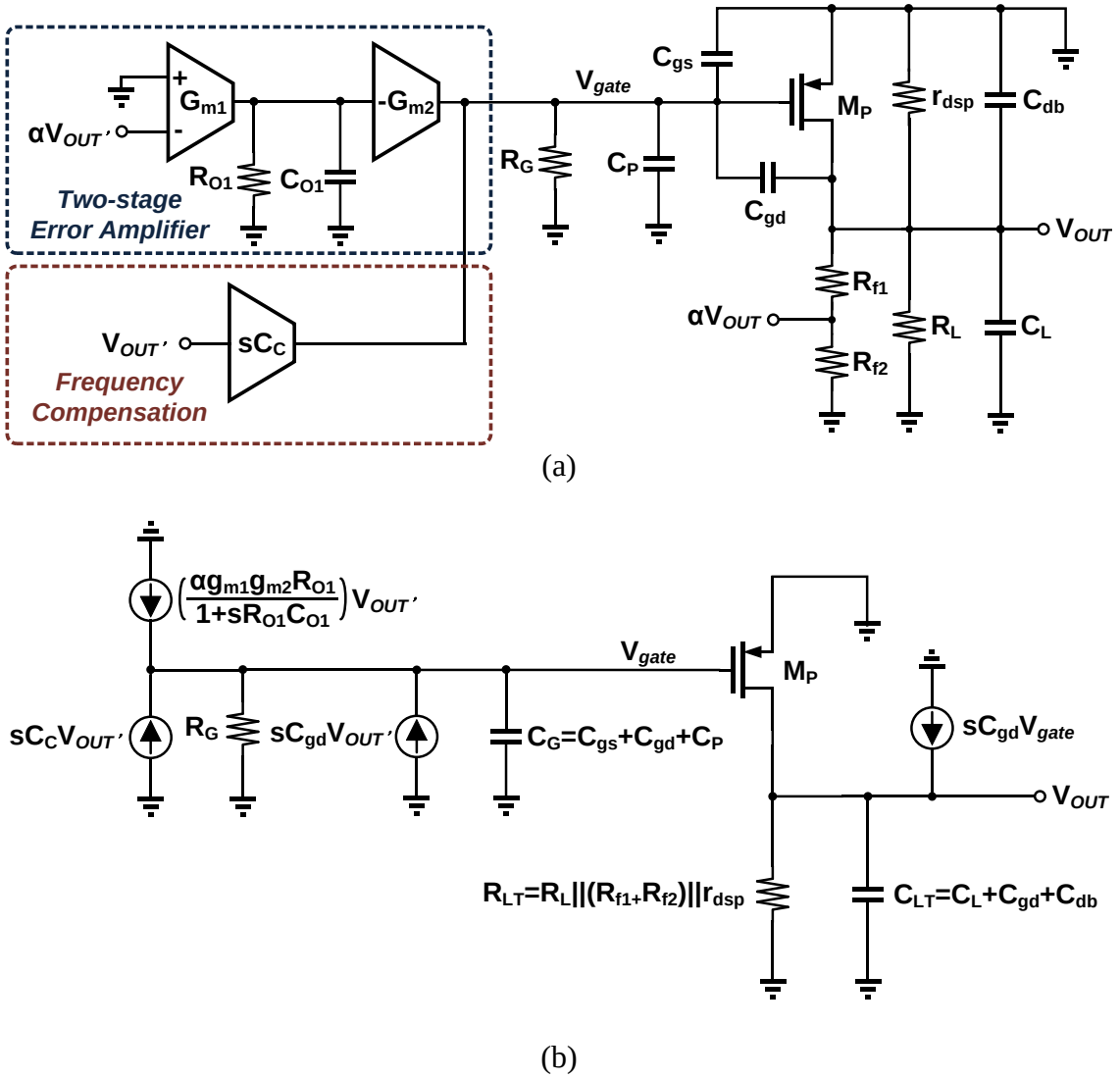


Fig. 4.3. (a) Open-loop schematic of a conventional external capacitor-less LDO with frequency compensation for a two-stage error amplifier, and (b) its small-signal equivalent circuit.

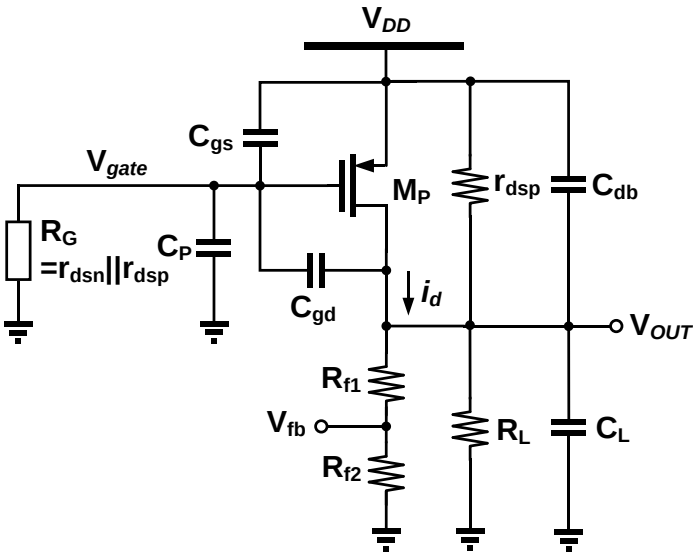
The feed-forward compensation technique with C_C in Fig. 4.3 adds a compensating zero, and the unity gain frequency is therefore dictated by the compensation path that is

strategically chosen to provide sufficient phase margin. In a case in which the LDO has a large load capacitance, the V_{dd} leakage components are also absorbed by the low output impedance due to the large load capacitance, which usually improves the PSR at high frequencies. For an external capacitor-less LDO, increasing the loop gain can partially alleviate the PSR degradation at medium and high frequencies. However, this approach may not be very attractive since designs with wide-band loop gain usually result in excessive power consumption. To obtain insights into PSR improvement possibilities at high frequencies, the fundamental PSR limitations due to each path are analyzed in more detail in the following subsections.

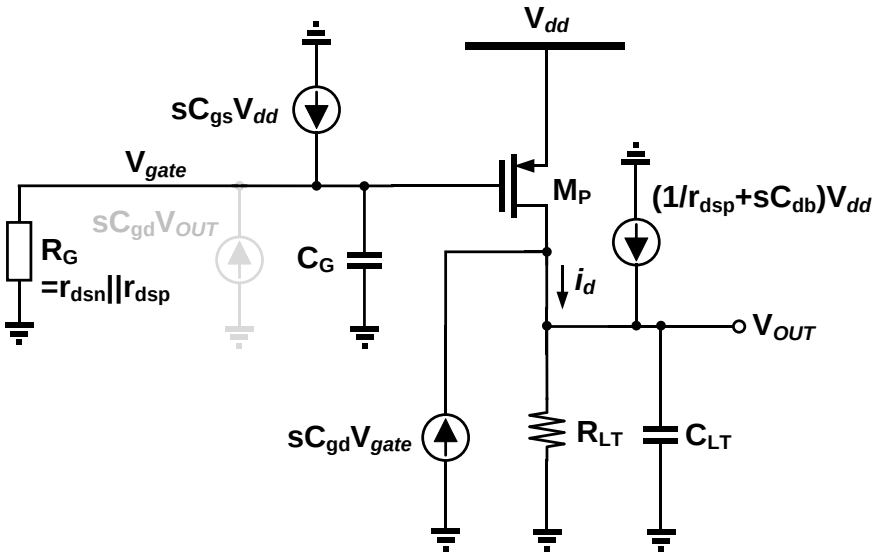
IV.3.1. PSR limitation due to the gate-source capacitance of the pass transistor

At high frequencies, the pass transistor, M_P, is the major factor that limits the LDO's PSR. As depicted in Fig. 4.4(a), the gate voltage of transistor M_P, V_{gate}, is modulated by V_{dd} through the capacitor C_{gs}. The drain current generated by V_{gate} and g_m of transistor M_P appears at the LDO output. This current is determined by the voltage difference between source and gate (V_{sg}) of M_P. Since C_{gd} generates a local feedback that makes V_{gate} a function of the output voltage, it complicates the analysis of V_{dd} noise. Following the approach in Fig. 4.3, this capacitor is split into four components consisting of two grounded capacitors and two voltage-controlled current sources (VCCS) as depicted in Fig. 4.4(b). The component $sC_{gs}V_{out}$ is a local feedback and its effect is embedded in the loop gain. The gate-source capacitor is also split into two pieces (the other two are attached to V_{dd}, and thus do not affect the analysis), which leads to the grounded

capacitor C_{gs} (one of the components of C_G) and the voltage controlled capacitive current source, $sC_{gs}V_{dd}$.



(a)



(b)

Fig. 4.4. (a) High-frequency supply noise leakage due to the pass transistor of an LDO, and (b) small-signal equivalent with floating capacitors represented by grounded capacitors and voltage-controlled current sources.

Since the pole due to equivalent resistance ($R_G \approx 500$ KΩ) and gate capacitance ($C_G \approx 30$ pF) is located at a low frequency of approximately 10 KHz, the effect of R_G can be ignored for high-frequency analysis. The gate voltage as function of V_{dd} can be approximated as follows:

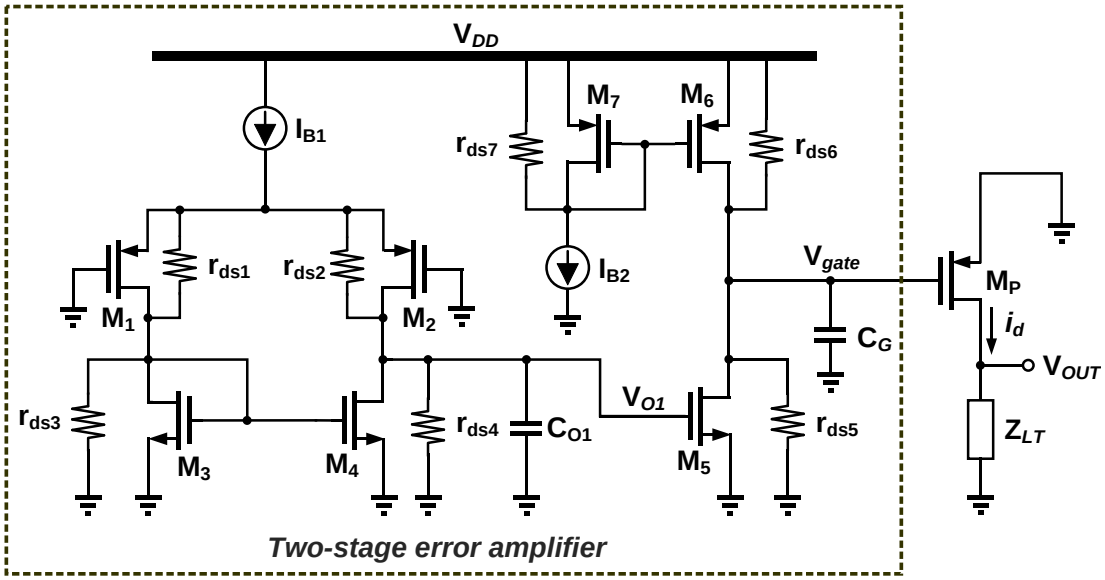
$$V_{gate} = \left[\frac{sC_{gs}}{(1/R_G) + sC_G}\right] V_{dd} \cong \left(\frac{C_{gs}}{C_G}\right) V_{dd} = \left(\frac{C_{gs}}{C_P + C_{gs} + C_{gd}}\right) V_{dd} \quad (4.3)$$

It is important to remark that C_{gs} and C_{gd} are much bigger than C_P since the dimensions of transistor M_P are much greater than those of the other transistors, and therefore C_P can be ignored in (4.3).

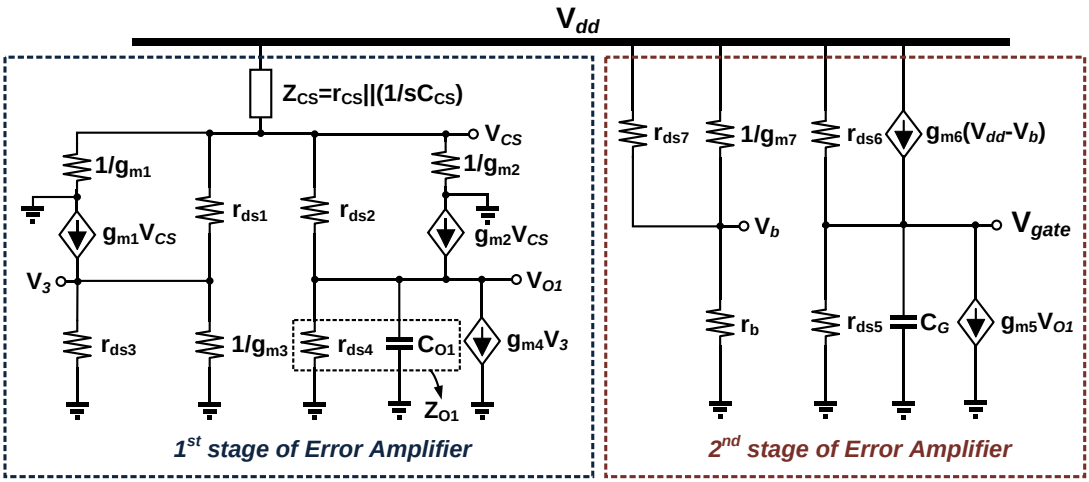
IV.3.2. PSR limitation due to the error amplifier

Most LDOs employing standard single-ended error amplifier have a limited common-mode and supply noise rejection. Since current mirrors are used for converting the differential signal to a single-ended signal, asymmetry presented in the circuit is a major issue of the single-ended error amplifier. The conventional two-stage error amplifier is shown in Fig. 4.5(a). When a PMOS differential input pair and an NMOS current mirror load are used as a the first stage, V_{dd} noise is injected into the common-source terminal due to finite output impedance of the current source, which can be modeled by a resistor (r_{CS}) and capacitor (C_{CS}) connected from the common-source terminal to the supply node as shown in Fig. 4.5(b). In the single-ended amplifier, the current is not equally split in the two arms due to unavoidable transistor mismatches in the differential pair. This non-ideality generates a differential current at the output that is proportional to the injected current that depends on the mismatch factor. Another concern is that the impedance seen

at the sources of the differential pair transistors is different due to the different loading conditions for each transistor. This increases the mismatch between the two branches and thereby further limits the rejection to supply and common-mode noise.



(a)



(b)

Fig. 4.5. (a) Typical two-stage error amplifier, and (b) small-signal model of error amplifier for PSRR

The finite output impedance of the current mirror introduces a systematic error. For the abovementioned reasons, it is advisable to use layout matching techniques and to optimize the LDO performance based on post-layout simulations with extracted parasitics. The small-signal model of the error amplifier for PSR analysis is shown in Fig. 4.5(b). Assuming that the mismatches of the PMOS differential pair and NMOS current mirror are minimized by layout matching techniques, the supply noise that appears at the output of the first stage in the error amplifier can be approximated by

$$\frac{V_{O1}}{V_{dd}} \cong \left(\frac{Z_{O1}}{Z_{CS}}\right)\left[\frac{(g_{m1}g_{m4} - g_{m2}g_{m3})r_{ds1}r_{ds2}r_{ds3} + (g_{m4}r_{ds2} - g_{m3}r_{ds1})r_{ds3} - g_{m2}r_{ds2}(r_{ds1} + r_{ds3})}{g_{m3}r_{ds1}r_{ds3}\{(g_{m1} + g_{m2})r_{ds2} + Z_{O1}g_{m1}\}}\right] \quad (4.4)$$

Assuming that the mismatches of the PMOS differential pair and NMOS current mirror are minimized by layout matching techniques, the supply noise that appears at the output of the first stage in the error amplifier can be approximated by

$$\frac{V_{O1}}{V_{dd}} \approx -\left(\frac{Z_{O1}}{Z_{CS}}\right)\left[\frac{r_{ds1} + r_{ds3}}{g_{m3}r_{ds3}(2r_{ds2} + Z_{O1})}\right] \quad (4.5)$$

where $Z_{O1} = r_{dsn4} \| (1/sC_{O1})$ is the output impedance of the first stage, and Z_{CS} represents the total impedance connecting between the common-source node and the supply node. Since the impedance of the current source for biasing the differential pair plays a critical role in (4.5), Z_{CS} in particular should be maximized at high frequencies. In addition, since the loop gain is proportional to Z_{O1}, it cannot be reduced to improve power supply noise rejection. Even if transistor mismatches are minimized, V_{dd} noise components can still be identified in (4.5). They are the result of the mismatch produced due to the different impedances seen from the sources of the differential pair transistors and due to the current loss that is caused by finite output impedance in the current mirror. As depicted in Fig. 4.5(b), the current flowing through the resistive impedance r_{ds3} in

parallel with the diode-connected transistor is not mirrored to the output of the first stage. Hence, the fully-differential to single-ended conversion leads to limited power supply rejection even when all transistors are perfectly matched. The second stage also contributes to V_{dd} noise at the gate terminal of transistor M_P. Thus, V_{gate} can be expressed as:

$$V_{gate} \cong \left\{\frac{(r_{ds5} \| r_{ds6})}{1 + s(r_{ds5} \| r_{ds6})C_G}\right\}\left[-g_{m5}\left(\frac{V_{O1}}{V_{dd}}\right) + \left(\frac{1}{r_{ds6}}\right) + \left(\frac{1}{r_b}\right)\right] V_{dd} \qquad (4.6)$$

In case the current source I_{B2} is designed such that $r_{ds5} = r_b$ and if a fully symmetric stage is used as the one discussed in the following section, then the V_{dd} noise contribution due to the first stage (V_{O1}/V_{dd}) is small. The contribution of the second stage is dominated by the effect of $r_{b,}$ r_{ds5} and r_{ds6}, therefore these resistances should be maximized by design to minimize the supply noise-induced current. Furthermore, since V_{dd} noise can be copied to V_{gate} if r_b is matched to r_{ds5}, such a design choice is an additional way to reduce the low-frequency V_{dd} noise contributed by the error amplifier.

Fig. 4.6 displays the simulated gate voltage (V_{gate}) of transistor M_P due to C_{gs} (Path 1) and the error amplifier (Path 2) versus frequeny. At medium and high frequencies V_{gate} is mainly determined by C_{gs} (Path 1), and the contribution of the error amplifier (Path 2) is negligible. The supply noise-induced current that appears at the output due to Path 1 and Path 2 can be approximated by:

$$i_{d\_Cgs+EA} \cong g_{mp}(V_{dd} - V_{gate}) + sC_{gd}V_{gate} = g_{mp}\left(\frac{C_{gd} + C_P}{C_{gs} + C_{gd} + C_P}\right)V_{dd} + sC_{gd}\left(\frac{C_{gs}}{C_{gs} + C_{gd} + C_P}\right)V_{dd} \qquad (4.7)$$

($C_{gd} + C_p$) plays the most relevant role in affecting the leakage of V_{dd} noise at medium and high frequencies. Notice that these capacitors are the culprits for causing $V_{gate} \neq V_{dd}$.

The main constraint is that it is difficult to predict (C_{gd} + C_p), making it challenging to design a robust PSR enhancing scheme for different load conditions.

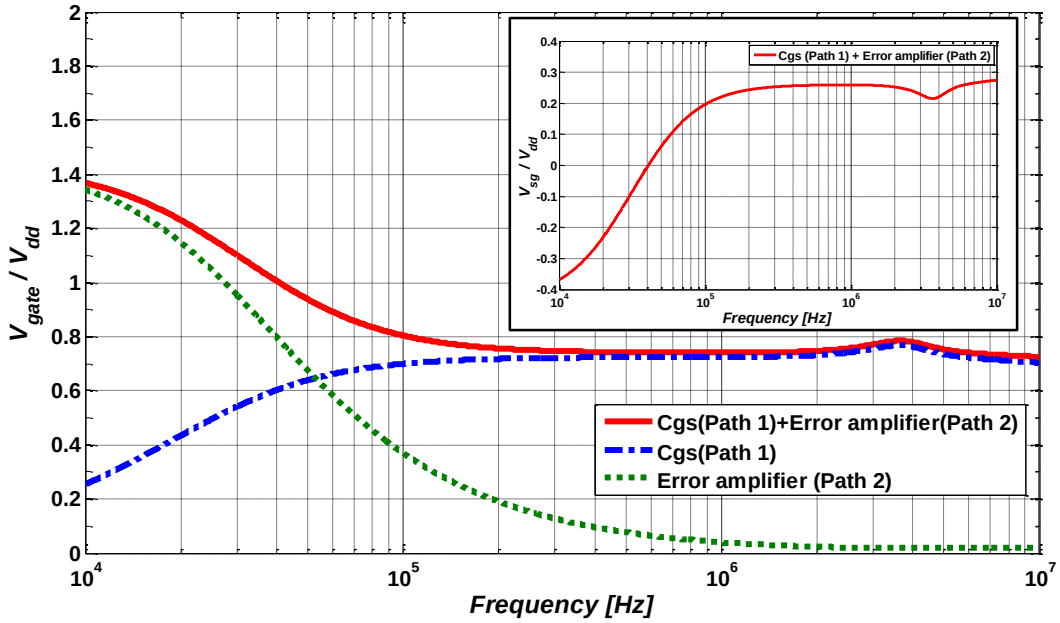


Fig. 4.6. Simulated V_{gate}/V_{dd} and V_{sg}/V_{dd} of the pass transistor due to C_{gs} (Path 1), and the error amplifier (Path 2) in the direct paths.

IV.3.3. Effect of the pass transistor's output impedance

The output resistance r_{dsp} of the pass transistor (Path 3) is another factor that limits the LDO's PSR. According to Fig. 4.4, the supply-noise induced current due to r_{dsp} reaches the load and is expressed as:

$$i_{d\_r_{dsp}\&Cdb} = \left(\frac{1}{r_{dsp}} + sC_{db}\right)V_{dd} \tag{4.8}$$

Since the zero due to r_{dsp} and C_{db} is located well beyond 10MHz, V_{dd} leakage current generated by the pass transistor's finite output impedance is dominated by r_{dsp}, which is in a first approximation frequency-independent at low and medium frequencies. This component represents the ultimate limit for high PSR.

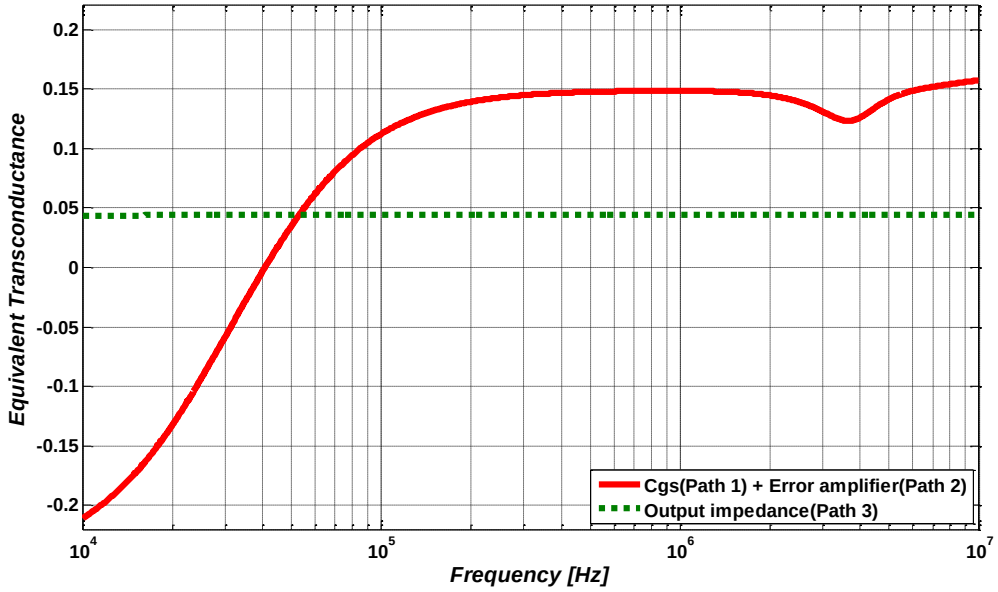


Fig. 4.7. Simulated equivalent transconductances in the direct paths.

Fig. 4.7 displays the simulated equivalent transconductance of the aforementioned factors in the direct paths that limit the LDO's PSR. As shown in Fig. 4.6 and 4.7, the error due to the source-gate voltage of the M_P transistor has the strongest impact on the LDO's high-frequency PSR. Since high-frequency V_{dd} noise modulates V_{gate} through C_{gs} (these voltages are not equal due to the effect of C_{gd} and C_P), the aim of the proposed PSR enhancement technique is to minimize the V_{dd}-V_{gate} noise voltage since it couples to the LDO output through the large transconductance of transistor M_P.

IV.4. Proposed PSR Enhancement Technique

PSR is inversely proportional to 1 + (loop gain) as shown in (4.1), but the frequency range with high gain is limited due to embedded poles in the loop, especially when designing with low power consumption. For better high-frequency PSR performance, it

is desirable to minimize the most relevant contributions of the direct paths of V_{dd} noise to the LDO output. C_{gs} of transistor M_P generates a source-gate voltage difference for transistor M_P (V_{sg}) in Fig. 4.8, which is converted into current by its transconductance gain, and this current flows into the load. We would like to track the supply noise at the gate of transistor M_P to eliminate the source-gate voltage fluctuation. Since the V_{sg} couples to the LDO output through the large transconductance of transistor M_P, the goal of the proposed PSR enhancement technique is to force $V_{sg} = 0$ AC condition for M_P by injecting the proper capacitive current, $sC_{gd}V_{dd}$, into the gate node as depicted in Fig. 4.8. However, since each capacitance (C_{gs}, C_{gd} and C_P) of transistor M_P is sensitive to the drain current of transistor M_P and it varies for the different load conditions [47], the required compensation capacitance also varies for the different loads. Therefore, the major challenge is the precise generation of the compensation current ($sC_{gd}V_{dd}$) for the different load conditions under PVT variations. Fig. 4.9 displays the conceptual schematic of the proposed PSR enhancer. A scaled replica of the pass transistor (few fingers of M_P) M_{PR} is used to recreate a scaled version of the parasitic gate capacitance of transistor M_P. The drain of transistor M_{PR} is connected to a low impedance node of a current amplifier with very small input impedance to minimize signal variations at the drain terminal of transistor M_{PR}.

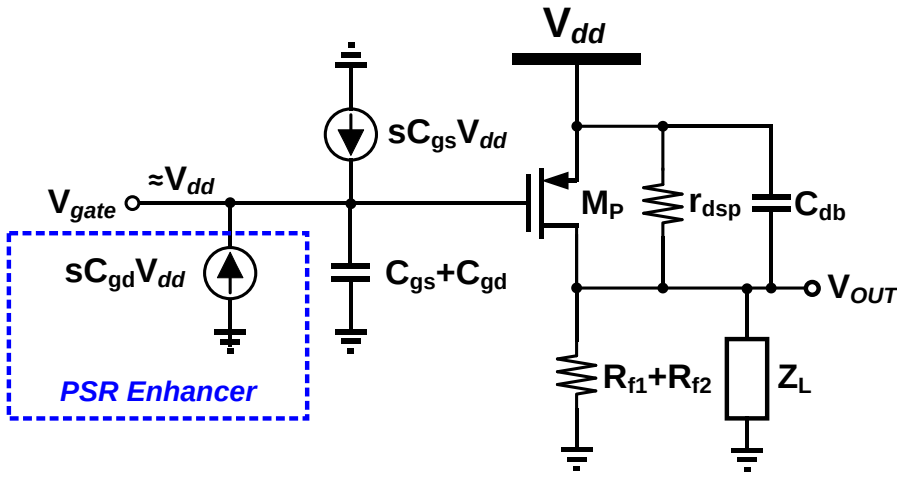


Fig. 4.8. Small-signal model of the proposed PSR enhancement technique.

The AC voltage across C_{gdr} tracks V_{dd} changes, and the corresponding scaled feed-forward AC current, i_{FFR}, is obtained as follows:

$$i_{FFR} = sC_{gdr}V_{dd} + \left(\frac{sC_{gsr}}{1 + g_{mpr}r_{dspr}}\right)\left\{\frac{1}{1 + \left(\frac{sC_{gsr}r_{dspr}}{1 + g_{mpr}r_{dspr}}\right)}\right\}V_{dd} \tag{4.9}$$

The second term in (4.9) is more ten times smaller than the first term due to the fact that the effect of C_{gsr} is by the DC gain of the transistor. Therefore, (4.9) can be simplified to

$$i_{FFR} \cong sC_{gdr}V_{dd} \tag{4.10}$$

Since the replica pass transistor was scaled-down to save power and area, i_{FFR} has to be scaled up by a factor N, where N is the ratio of the number of fingers used in transistor M_P and transistor M_{PR}, respectively. This compensation technique relies on the accuracy of the current amplifier to match the current generated by the PSR compensation circuitry and the required one ($sC_{gd}V_{dd}$).

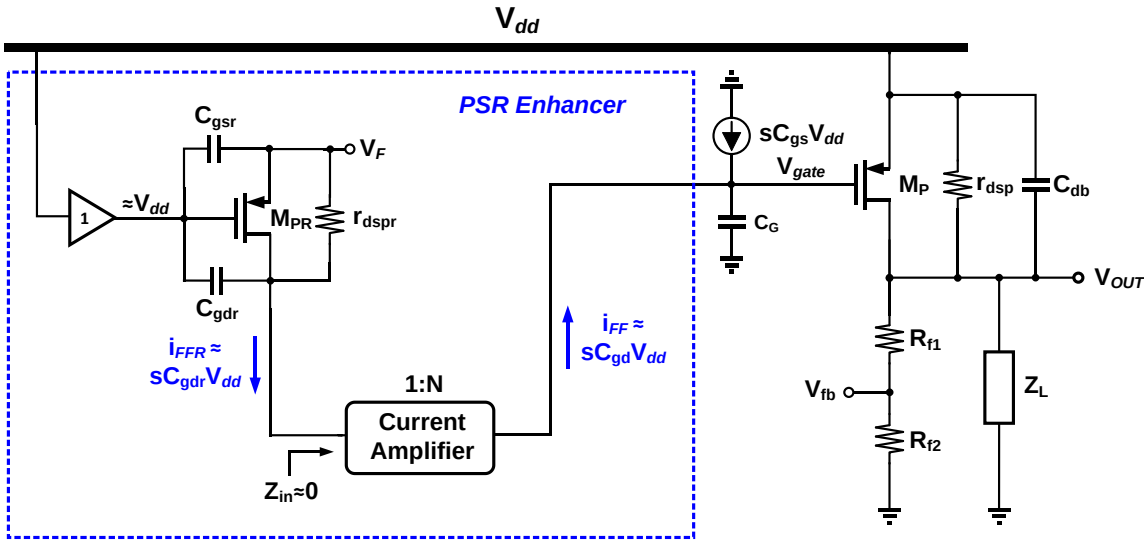


Fig. 4.9. Conceptual schematic of the proposed PSR enhancer.

After i_{FF} is summed with $sC_{gd}V_{dd}$ at the gate terminal (V_{gate}) of transistor M_P as depicted in Fig. 4.9, the gate voltage can be expressed as follows:

$$V_{gate} = \left(\frac{C_{gs} + C_{gd}}{C_G}\right) V_{dd} = \left(\frac{C_{gs} + C_{gd}}{C_{gs} + C_{gd} + C_P}\right) V_{dd} \cong V_{dd} \tag{4.11}$$

which is the desired result. A DC line regulation analysis was performed to verify that the PSR enhancement circuitry has negligible impact on the DC line regulation, which is included in the Appendix.

IV.5. Circuit Implementation

IV.5.1. PSR enhancer

A critical aspect of the PSR enhancement technique is the precise replication of the effects from the parasitic capacitances of transistor M_P. For this prototype, the ratio M_P/M_{PR} was chosen to be equal to 100, hence I_{LR} is approximately equal to $I_L/100$. The bias current I_{LR} is correlated with the load current, and it is generated through additional

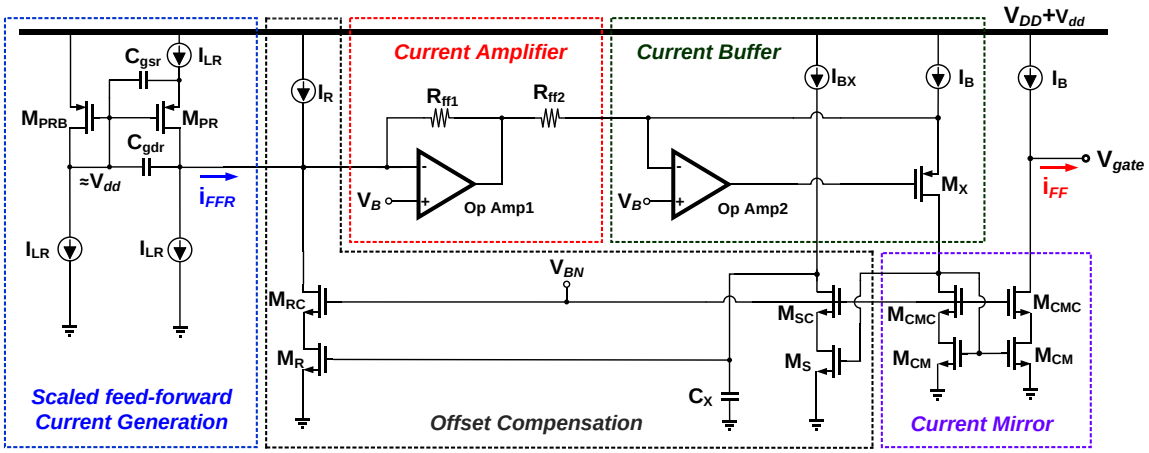
fingers similar to the ones used in transistor M_P and low-pass filtered out to remove high frequency components. The top bias current sources is used to bias transistor M_{PR}, while the bottom current source prevent large amount of current flowing through the current amplifier that otherwise may saturate Op Amp1. The proposed scheme will be more precise if the drain-source voltage of transistor M_{PR} in Fig. 4.9 is set close to the drain-source voltage of transistor $M_{P,}$ which is around the drop-out voltage to create a similar the drain-to-source voltage modulation impact due to short-channel effects in both transistors. The diode-connected transistor M_{PRB} delivers the V_{dd} noise to the gate of transistor M_{PR}. The drain of transistor M_{PR} is forced to be at V_B.

The AC voltage across C_{gdr} tracks the small-signal supply fluctuations and then generates the scaled capacitive current i_{FFR}. Since C_{gd}/C_{gdr} is defined by the ratio of the number of fingers between transistor M_P and transistor M_{PR}, the scale-down ratio of currents is quite precise. The scale-up factor of i_{FFR} is realized through a current amplifier consisting of an operational amplifier (Op Amp1) and resistors R_{ff1} and R_{ff2}. The input current i_{FFR} is converted into voltage by R_{ff1}, and converted back into current by R_{ff2} and Op Amp2, leading to a current amplifier whose gain is given by R_{ff1}/R_{ff2}. The current is then fed into the source of transistor M_X and injected into a current mirror transistor M_{CM} before driving the gate of transistor M_P. The current buffer stage in Fig. 4.10(a) helps to avoid a loss of the scaled feed-forward current. The condition $V_{gate}/V_{dd} = 1$ can be achieved if the following condition is satisfied.

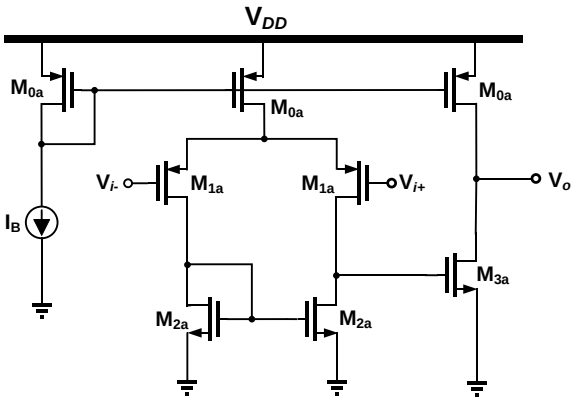
$$\frac{R_{ff1}}{R_{ff2}} = \frac{C_{gd}}{C_{gdr}} = N \tag{4.12}$$

In order to minimize mismatches, common-centroid and inter-digitized layout techniques with dummies were used for implementation of capacitor and resistor ratios. Resistor width was set at 4 times the minimum recommended by the foundry. Since the capacitor ratio is controlled by the number of transistor fingers and the current gain depends on a resistor ratio, it is expected that the proposed approach be robust to PVT variations.

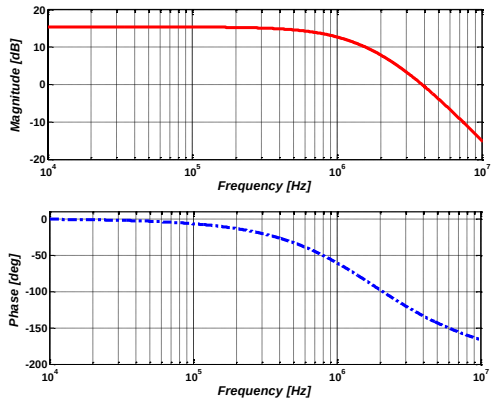
The mismatch between the top and bottom bias currents I_{LR} in the scaled feed-forward current generation block may generate significant DC offset would limit the accuracy of the solution after the amplification. For this reason, the offset is compensated by the additional loop consisting of the output current sampler transistor M_S, capacitor C_X, and transistor M_R to adjust the DC current. The DC current difference between I_R and the feedback current from transistor M_R cancels the mismatch current between the bias currents. As depicted in Fig. 4.10(b), the auxiliary amplifiers for the current amplifier and current buffer were implemented with a conventional two-stage topology, where a two-stage amplifier is needed because the amplifier is resistive terminated. Fig. 4.10(c) displays the open-loop AC response of the auxiliary amplifier (Op Amp1) from a simulation in which the loop is opened at the input but the equivalent load is connected to the amplifier's output as in the closed-loop configuration. The values of the resistors (R_{ff1} and R_{ff2}) and the parasitic capacitance at the inverting terminal are 200 KΩ, 2 KΩ and 400 fF, respectively. The DC loop gain of the amplifier is 15 dB, and the phase margin is 50°.



(a)



(b)



(c)

Fig. 4.10. (a) PSR enhancer circuitry, (b) schematic of the amplifier used in the current amplifier and current buffer, and (c) simulated Cadence open-loop AC response of Op Amp1 with R_{ff1}=200 KΩ and R_{ff2}=2 KΩ; dominant pole is located at the gate of transistor M_{3a}.

IV.5.2. Key LDO components

The proposed PSR compensated LDO architecture employs a single-ended two-stage error amplifier as well as the PSR and frequency compensation blocks. The architecture is visualized in Fig. 4.11. A brief description of the main blocks as follows.

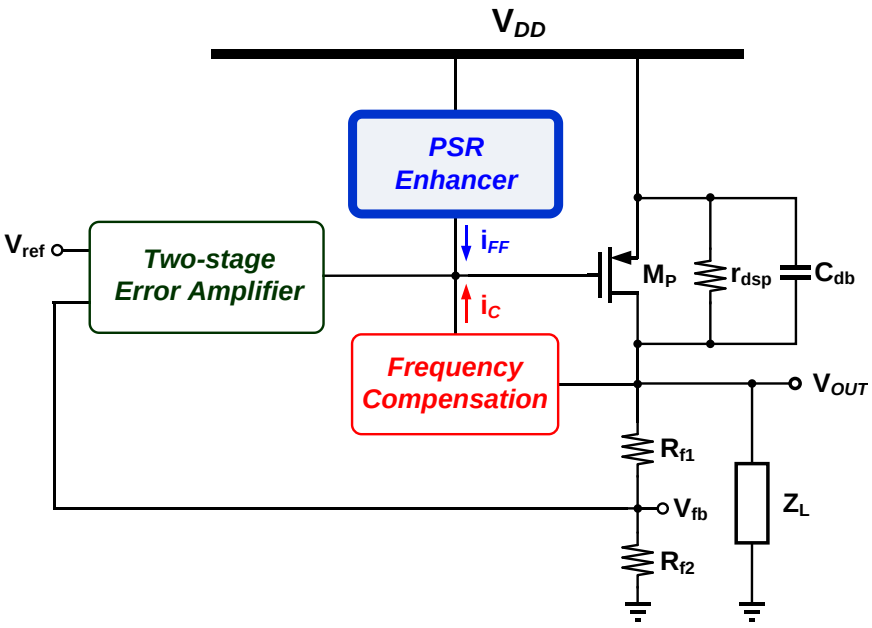


Fig. 4.11. Proposed PSR-compensated LDO architecture.

IV.5.2.1. Error amplifier

The single-ended two-stage error amplifier is depicted in Fig. 4.12. A fully-differential PMOS input stage is used to achieve high power supply noise rejection. The NMOS load transistors M_2 employ local feedback to control the gate voltage, which eases the connection to the second stage and at the same time cancels the differential signal at the common-gate node. The differential mode gain is defined by the transconductance of the input stage and the resistance of the feedback resistors R_{CMFB}. The cascode transistors (M_4) are added to the second stage of the error amplifier because

they improve the matching between M_3 transistors and increase the gain. The resulting high equivalent resistance at the gate helps to stabilize the system because the main pole in the loop is at the gate of transistor M_P in Fig. 4.11.

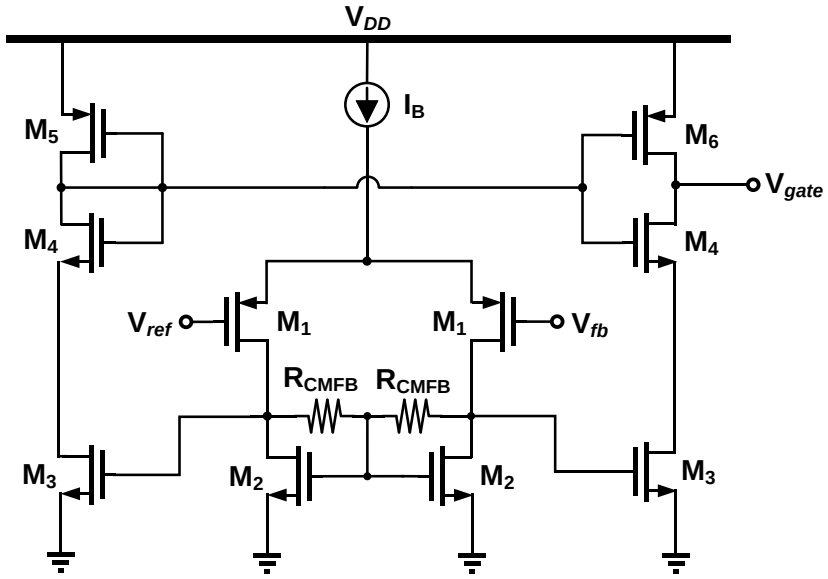


Fig. 4.12. Transistor-level implementation of the single-ended two-stage error amplifier with fully differential input stage.

It was found that the contribution of the error amplifier to the LDO's PSR at high frequencies is negligible due to its symmetry. This result is in good agreement with previous observations [50].

IV.5.2.2. Frequency compensation and fast slew enhancement circuitry

To generate a low-frequency compensation zero for loop stability, the combination of a differentiator and an amplification stage displayed in Fig. 4.13 is utilized [46-47]. The compensation current i_C is obtained after differentiating the output voltage through C_{C1} and R_{C1}, and it can be approximated as:

$$i_C \cong s(g_{m8}R_{C1}C_{C1})V_{OUT} \tag{4.13}$$

Therefore, the open-loop transfer function has two trajectories: the first one through the resistive network, error amplifier, and transistor M_P; and the second one determined by the frequency compensation loop. Hence, the open-loop transfer function is obtained as:

$$H(s) \cong -\{\alpha(g_{m1}R_{O1})(g_{m2}R_G)(g_{mp}R_{LT})\}\left[\frac{s^2\left\{\frac{g_{m8}R_{C1}C_{C1}R_GR_{O1}C_{O1}}{\alpha(g_{m1}R_{O1})\cdot(g_{m2}R_G)}\right\}+s\left\{\frac{g_{m8}R_{C1}R_GC_{C1}}{\alpha(g_{m1}R_{O1})\cdot(g_{m2}R_G)}\right\}+1}{(1+sR_{O1}C_{O1})(1+sR_GC_G)(1+sR_{LT}C_{LT})}\right]. \tag{4.14}$$

The dominant pole is at the gate of transistor M_P due to the use of cascode transistors in the error amplifier and the large dimensions of transistor M_P. The second pole is usually at the LDO output, and is a function of the load impedance. The third pole is generated at the output of the error amplifier's first stage and is usually well beyond the loop's unity gain frequency. There are two real left-hand plane zeros whose placement has to be judiciously selected to ensure loop stability [46-47].

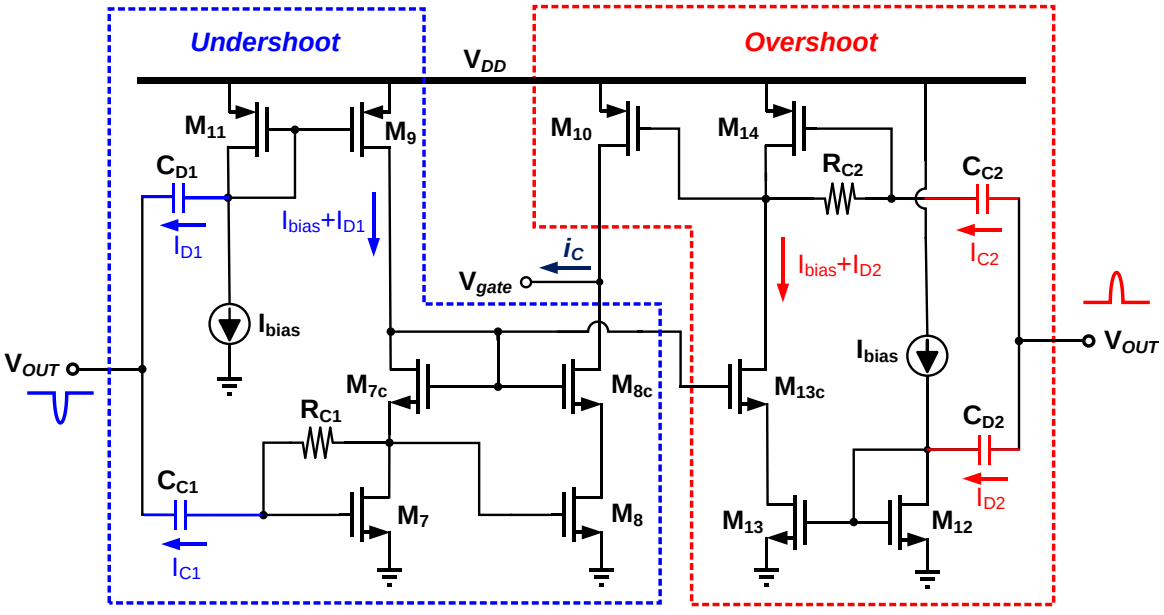


Fig. 4.13. Frequency compensation and fast slew enhancement circuitry.

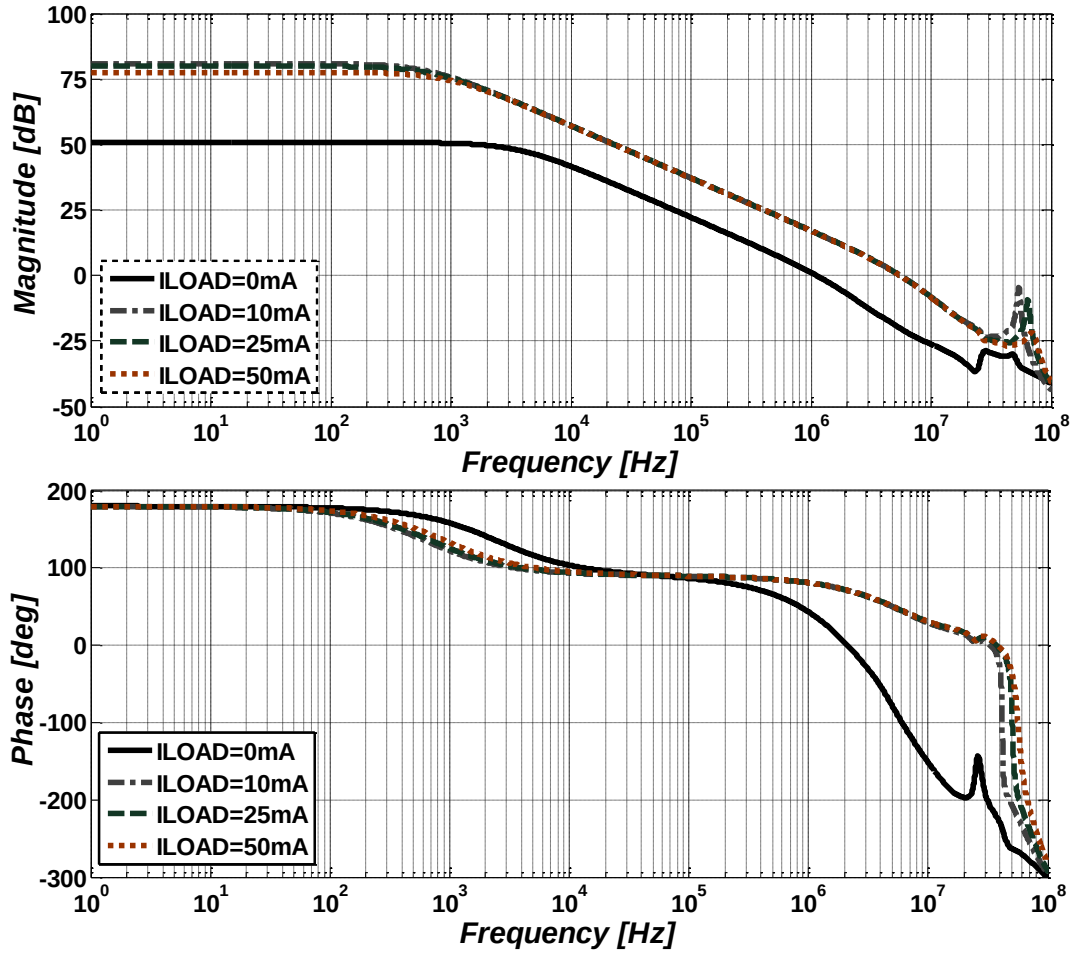


Fig. 4.14. Simulated full range open-loop AC response (0 – 50 mA).

Fig. 4.14 shows the simulated full-range (0 – 50 mA load currents) open-loop AC responses of the proposed LDO. The system is stable under all conditions and it achieves over 1 MHz unity gain frequency and 50 ° phase margin across the complete range. The worst-case gain and phase margins after simulations with process corner device models were 3.5 dB and 43.5°, showing that the LDO is stable in the presence of process variations.

The frequency compensation block is reused to improve the transient response of the proposed LDO. Fig. 4.13 depict the operation of the proposed solution during undershoot and overshoot cases, respectively. The frequency compensation circuit is split into two sections as shown in Fig. 4.13, where the two sets of components are (C_{C1}, R_{C1}, M_7, M_8) and (C_{C2}, R_{C2}, M_{14}, M_{10}). The parasitic capacitance at the gate of transistor M_P (C_G in Fig. 4. 9) is very large due to the large dimensions of transistor M_P. To overcome slew-rate limitations due to large C_G, large currents are needed to charge and discharge it quickly [54]. Since these currents are only necessary when the LDO's output is exposed to transient load current changes, operating the auxiliary feedback loop in class-AB mode would be more power efficient than in class-A. The cascode transistors (M_4, M_{7C}, M_{8C} and M_{13C}) in the error amplifier (Fig. 4. 12) and frequency compensation circuitry (Fig. 4. 13) help to minimize channel length modulation effects for improved matching performance. Furthermore, common-centroid layout was employed for current mirror transistors. It was verified through Monte Carlo simulations that the input offset voltage (mean = 0.653 µV, standard deviation = 0.782 µV) of the frequency compensation circuitry has negligible impact on the LDO operation.

A glitch detector based on capacitive coupling and class-AB operation is used with a dynamic bias current-boosting technique. The complementary operation is exploited to minimize undershoots and overshoots at the LDO's output when the load current suddenly changes. The glitch suppressor is implemented by another set of components: (C_{D1}, M_{11}, M_9) and (C_{D2}, M_{12}, M_{13}). The current through these blocks is dynamically controlled when large glitches appear at LDO output. For example, C_{D1} senses the glitch

and produces a current (i_{D1}) that adds with I_{bias} during undershoots. This mechanism adjusts the drain current of transistor M_7 dynamically in accordance to the magnitude of the detected glitch, leading to an enhanced transient response for undershoots with small bias current. The fast components of the drain current of transistor M_{11} are converted into voltage by R_{C1} and then mirrored to V_{gate} through transistor M_8. It is worth mentioning that to authors' best knowledge the capacitive coupling technique was first proposed in [55]-[58] as an output glitch detection scheme. The main parameters of the different building blocks as well as biasing conditions are given in Table IV.1. The bias current of transistor M_P under no loading condition is set at 5 μA. This current was set larger than the maximum leakage current (0.58 μA) at high temperature flowing through the feedback resistors, but the leakage current is small enough while in standby mode. This bias current is enough to guarantee loop stability in standby mode.

TABLE IV.1
DIMENSIONS AND BIAS CONDITIONS OF RELEVANT TRANSISTORS

	Device	Parameter (W/L)	Bias Current (μA)
Error Amplifier (Fig. 4.12)	M_1	8 μm / 0.8 μm	2.5
	M_2	1.6 μm / 0.8 μm	2.5
	M_3=M_4	6.4 μm / 0.8 μm	10
	M_5=M_6	8 μm / 0.8 μm	10
	R_{CMFB}	200KΩ	
Pass Transistor	M_P	12000 μm / 0.18 μm	5
PSR Enhancer (Fig. 4.10)	M_{PR}	120 μm / 0.18 μm	0.05
	M_{PRB}	4.2 μm / 0.18 μm	0.05
	M_X	8 μm / 0.36 μm	5
	M_{CM}=M_{CMC}	9.6 μm / 2 μm	5
	M_S=M_{SC}	2.4 μm / 2 μm	1.25
	M_R=M_{RC}	9.6 μm / 2 μm	5
	M_{0a}	4 μm / 2 μm	2
	M_{1a}	2 μm / 2 μm	1
	M_{2a}	1 μm / 2 μm	1
	M_{3a}	2 μm / 2 μm	2
Frequency Compensation (Fig. 4.13)	M_7=M_{7C}=M_{12}=M_{13}=M_{13C}	0.8 μm / 0.2 μm	2.5
	M_8=M_{8C}	6.4 μm / 0.2 μm	20
	M_9=M_{11}=M_{14}	1.5 μm / 0.5 μm	2.5
	M_{10}	12 μm / 0.5 μm	20

IV.6. Prototype Measurement Results

The proposed LDO voltage regulator was designed and fabricated in a 0.18 µm CMOS technology; Fig. 4.15 displays the chip microphotograph. An on-chip 100 pF load capacitor was included to emulate the effects of capacitive loading for assessment of LDO performance under extreme conditions, but it should not be considered part of the LDO. Actually, this capacitive loading pushes the output pole to lower frequencies, compromising the loop stability. The total active area of the LDO excluding the 100 pF capacitor is 0.14 mm^2. The 100 pF on-chip capacitor occupies approximately 45% of the total area, leading to an active chip area of 0.25 mm^2. Four 1 pF on-chip capacitors were used for frequency compensation and fast slew enhancement. Another 24 pF on-chip capacitor was included for offset compensation within the PSR enhancer.

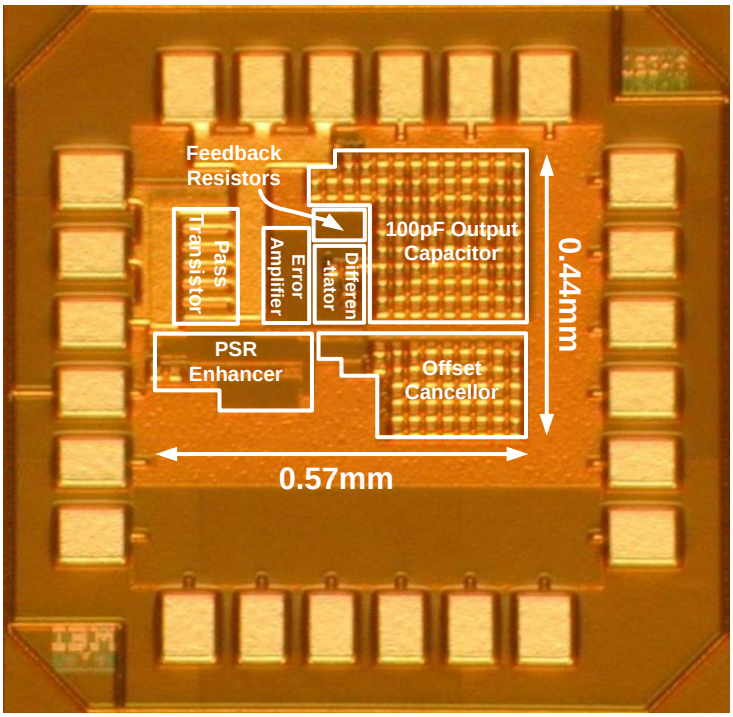


Fig. 4.15. Chip micrograph of the fabricated LDO with a total active area of 0.25 mm^2.

All on-chip capacitor values sum up to 28 pF, excluding the 100 pF load capacitor that is only used for testing purposes. The entire quiescent current of the LDO was 80 µA with an input of 1.8 V during operation mode. Under zero loading conditions, the LDO does not need to have an excellent PSR performance. In this case, the PSR enhancer is deactivated for saving power, leading to an optimized quiescent current of 55 µA. The meaning of "standby" mode in this design is referring to the deactivated state of the PSR enhancer when no load is present at the LDO output. The proposed LDO has a measured output voltage of 1.6 V for an input voltage range from 1.8 V to 2.6 V, and its drop-out voltage is 200 mV.

IV.6.1. Measurement set up

Figure 4.16 displays the PSR measurement set up. The signal level of LDO's input and output is measured by HP3588A spectrum analyzer, which has a high input impedance (Rin = 1 MΩ).

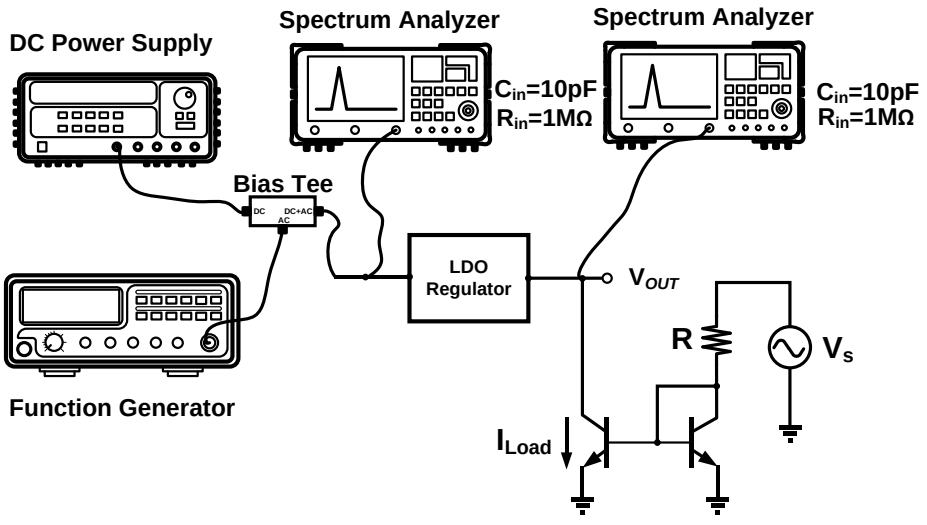


Fig. 4.16. Measurement set up for PSR.

In order to assess the PSR of the LDO, an input sine wave was swept from 10 KHz to 10 MHz; the amplitude of the sine wave was adjusted to 100mV to emulate the effect of large power supply noise. The load transient response was measured using the setup shown in Fig. 4.17. Capacitor C_S was added at the input terminal of the LDO to provide a clean ground and to compensate for any inductive effects from the measurement cables. The load current was produced with a signal generator and a BJT NPN current mirror, allowing to control the rise/fall times of the load current with the signal generator. The LDO was tested for full-range (0 - 50 mA load currents) using a 500 MHz oscilloscope to monitor its output voltage. The supply transient step for line transient measurements was applied with a waveform generator.

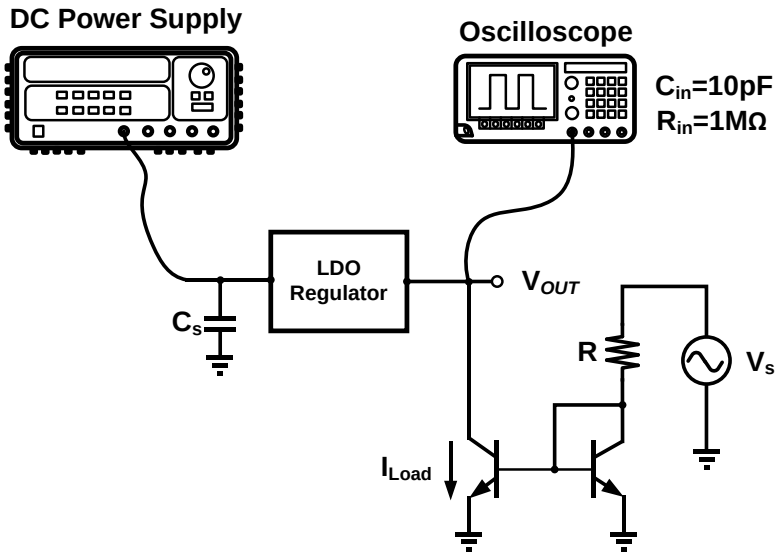


Fig. 4.17. Measurement set up for load transient.

IV.6.2. Power supply rejection (PSR)

Fig. 4.18 displays the measured PSR with and without the proposed PSR enhancer at a load current of I_{LOAD} = 50 mA. The PSR improvement with PSR enhancer is more than 25 dB for the 0.4 MHz – 4 MHz frequency range. The proposed architecture shows a remarkable high-frequency PSR improvement of 34 dB and 25 dB at 1 MHz and 4 MHz, respectively. In addition, the proposed LDO was simulated with large amplitude of input sine waves (200 mV and 500 mV) at a load current of I_{LOAD} = 50 mA in order to evaluate the effectiveness of the proposed LDO architecture under very stringent conditions. The simulated PSR of the LDO with large power supply noises at a load current of I_{LOAD} = 50 mA is depicted in Fig. 4.19. The value of power supply (V_{DD}) was properly adjusted to tolerate these extremely large supply variations while maintaining the LDO functional. The proposed LDO with PSR enhancement scheme still achieves a remarkable high-frequency PSR improvement of 24 dB and 15 dB at 1 MHz and 4 MHz, respectively.

Notice that large leakage current of transistor M_P at high temperature may affect the LDO output voltage regulation. During standby operation, the leakage current in transistor M_P flows through the feedback resistors and if excessive may produce a voltage drop in R_{f2} that exceeds the reference voltage. Under these conditions, the loop will not operate properly. For this particular case, the maximum leakage current of transistor M_P is estimated to be around 0.58 µA at high temperature (85 °C), then having negligible effects on loop operation, but it could be a limiting factor in more advanced technologies with high gate leakage. The simulated output voltage of the proposed LDO is approximately within 1% of the target voltage in the 27-85 °C range under the zero

load current condition. The measured PSR for different load current conditions follows the same trend, as shown in Fig. 4.20.

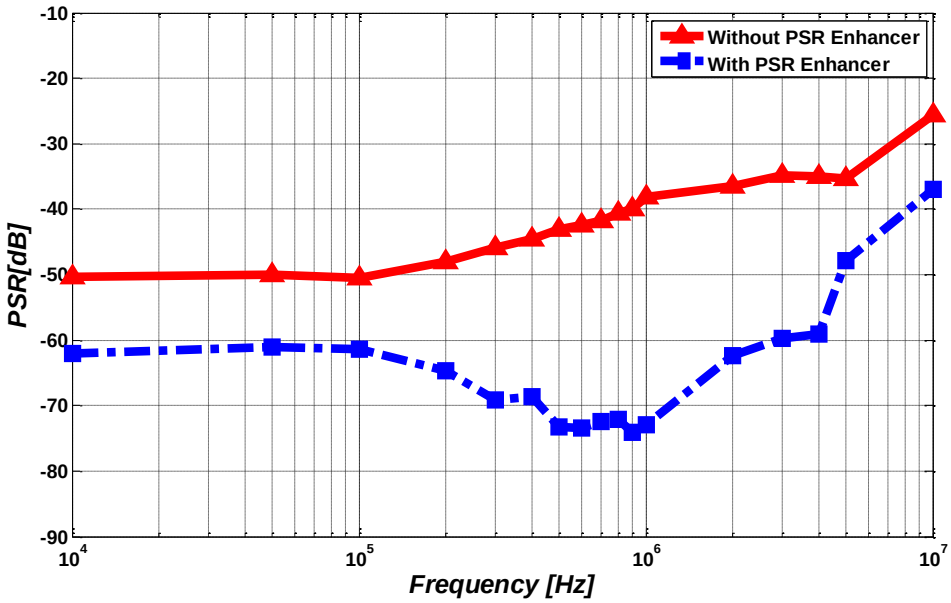


Fig. 4.18. Measured PSR with and without the proposed PSR enhancer (I_{LOAD} = 50 mA).

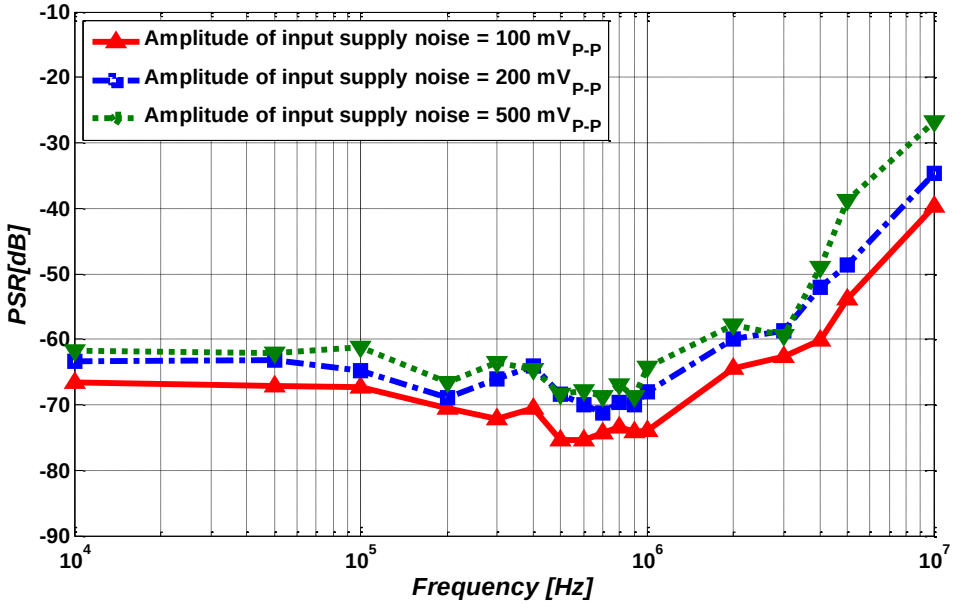


Fig. 4.19. Simulated PSR of the LDO with large power supply noises (I_{LOAD} = 50 mA).

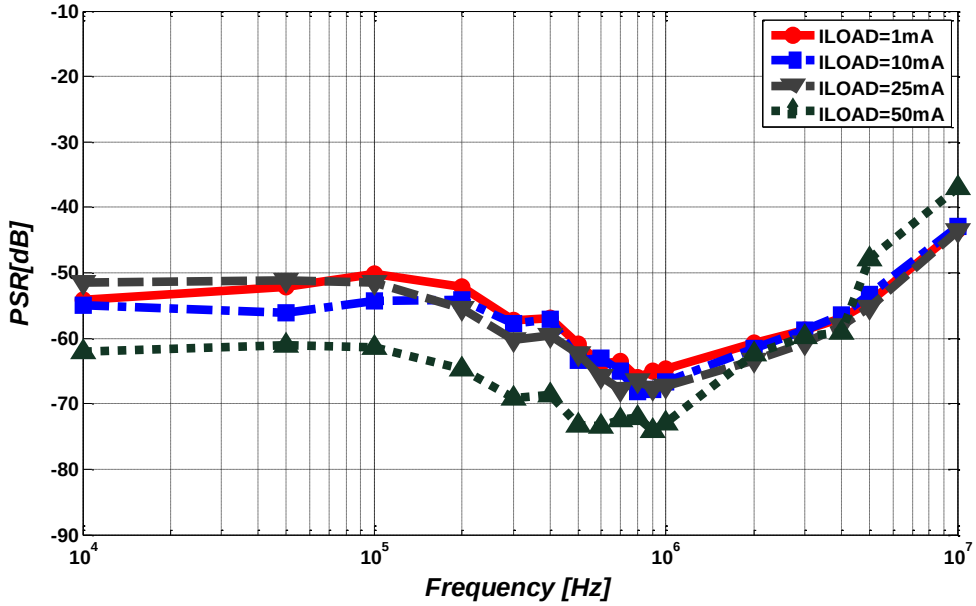


Fig. 4.20. Measured PSR with PSR enhancer for different load currents.

The LDO achieves better than -40 dB PSR up to 8 MHz for all load conditions. The PSR enhancement technique is less effective at frequencies beyond 5 MHz due to the additional poles in the current amplifier, current buffer, and current mirror. However, the proposed scheme achieves supply noise rejection better than -37 dB up to 10 MHz, demonstrating the feasibility of the proposed noise tracking scheme. If needed, the low-frequency PSR can still be improved by optimizing the error amplifier.

IV.6.3.Deflection voltage

Fig. 4.21 displays the measured load regulation for a sweep of the load current up to 100 mA. The output voltage deflection is less than 0.5% over the 0 - 50 mA operation range, and less than 1% up to 100 mA load current. Since this is a static measurement, the deflection voltage is determined by the loop gain such that increasing the gain of the

error amplifier would improve the rejection to low-frequency noise while reducing the output variation.

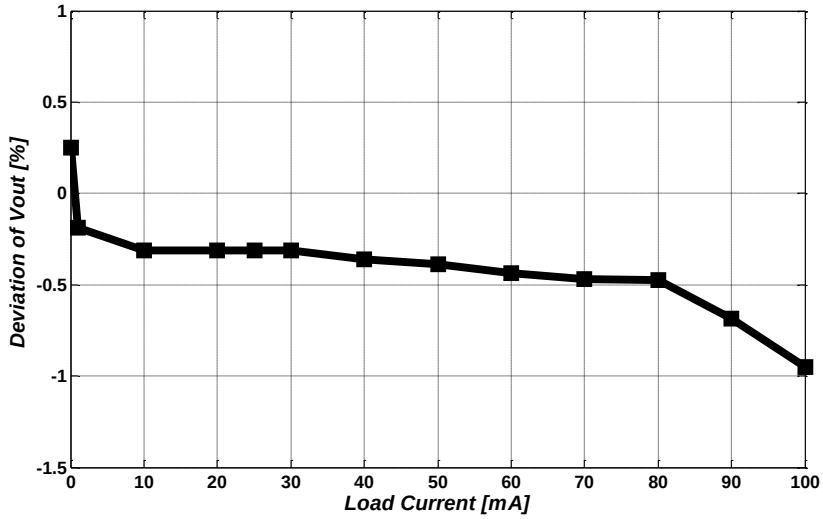
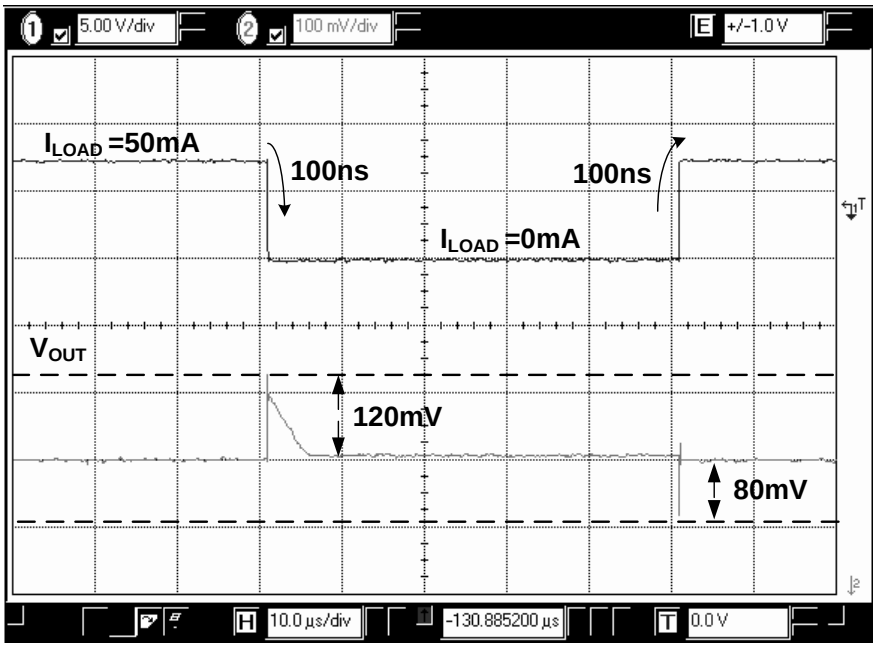


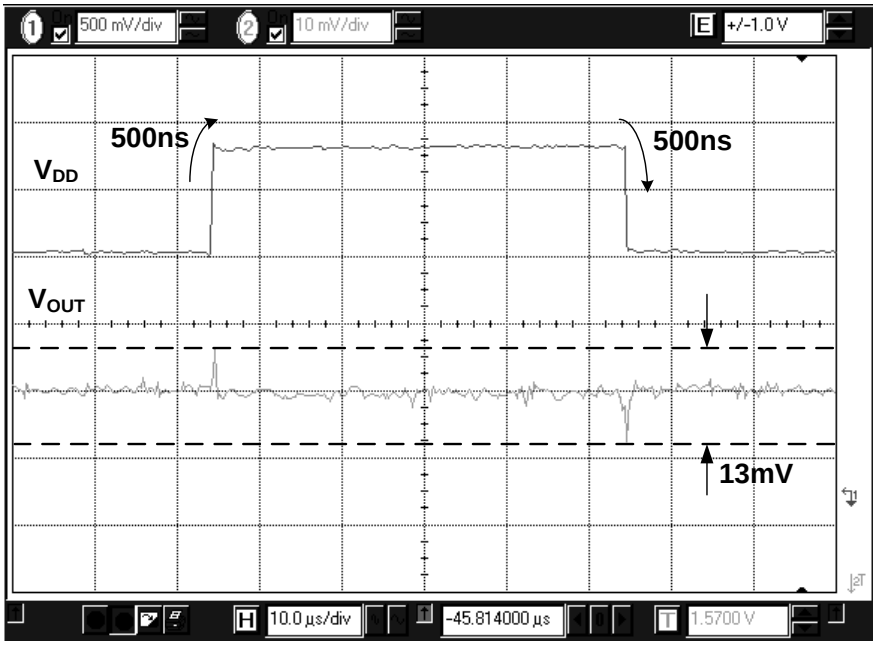
Fig. 4.21. Measured load regulation.

IV.6.4. Transient response: load and line regulation

The measurement of the 0 - 50 mA load transient response is shown in Fig. 4.22(a). The maximum overshoot and undershoot are 120 mV and 80 mV with 0 – 50 mA step load current having 100 ns rise/fall times. The spikes during the transient response reduce if the rise and fall times of the load variation are reduced, limiting the peak values to less than 100 mV in all cases. These results show that the 1% settling time is under 10 μs. The measured line transient response for an input that varies from 1.8 to 2.6 V with 500 ns rise/fall times is shown in Fig. 4.22(b). For the 50 mA load current case, the maximum variations at the LDO output are less than 13 mV.



(a)



(b)

Fig. 4.22. (a) Measured load transient response for a load current step of 50 mA, and (b) measured line transient response (I_{LOAD} = 50 mA).

IV.6.5. Output noise

The measured output power spectrum noise density (PSD) at I_{LOAD} = 50 mA is shown in Fig. 4.23. The low-frequency output noise is mainly determined by the flicker noise. The measured spot noise within the 10 KHz to 100 KHz range was roughly in the order of 250 nV/Hz$^{1/2}$. The performance of the proposed LDO is summarized and compared to previously reported high-PSR LDOs in Table IV.2. The proposed LDO achieves high PSR for a wide range of frequencies up to several megahertz. Also, it provides fast settling time and is less noisy at the high frequencies. Although fully characterized at 50 mA, the proposed architecture is able to deliver up to 100 mA. The architecture is able to maintain these performances under all loading conditions without requiring manual tuning. Since it was stabilized under different load conditions without a bulky external capacitor, this architecture is suitable for SoC applications.

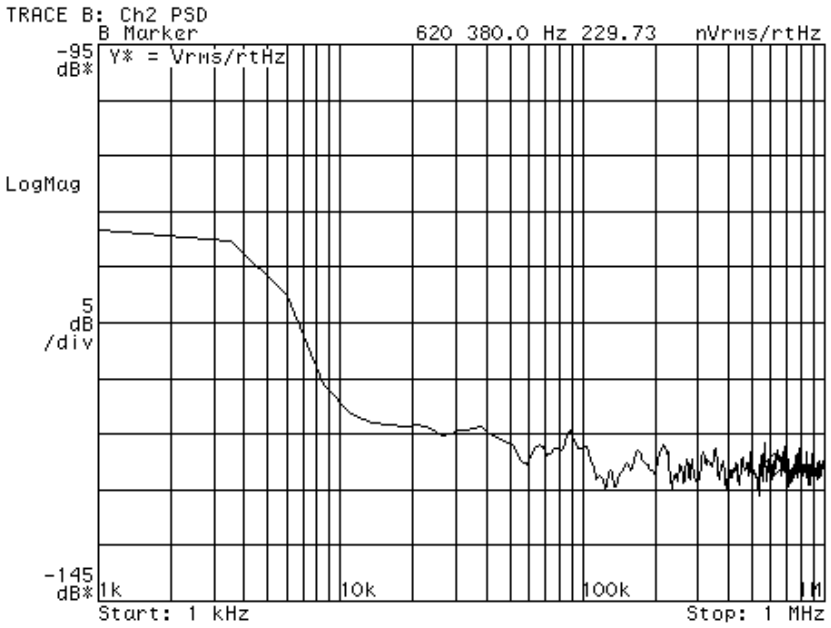


Fig. 4.23. Measured LDO output noise with I_{LOAD} = 50 mA.

TABLE IV.2
PERFORMANCE SUMMARY FOR THE PROPOSED LDO AND COMPARISON

	[41]	[43]	[44]	[46]	[53]	[59]	This work
Technology	0.13 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	1.5 µm Bipolar	0.13 µm CMOS	0.18 µm CMOS
Max. Load	25 mA	150 mA	25 mA	50 mA	5 mA	50 mA	100 mA**
V_{OUT}	1 V	1.5 V	1.5 V	2.8 V	1.2 V	1 V	1.6 V
V_{DROP}	150 mV	541 mV	300 mV	200 mV	200 mV	200 mV	200 mV
I_Q	50 µA	8.5 µA	300 µA	65 µA	56 µA*	37.32 µA	55 µA
On-chip Capacitor	5 pF	10 pF	100 pF	23 pF	170 pF	21 pF	28 pF
Load Capacitor	External 4 µF	External 1 µF	Cap-less (On-Chip 25 pF)	Cap-less (On-Chip 100 pF)	External 15 nF	Cap-less (On-Chip 20 pF)	Cap-less (On-Chip 100 pF)
Area	0.049 mm^2	0.31 mm^2	0.041 mm^2	0.12 mm^2	1.2 mm^2	0.018 mm^2	0.14 mm^2
PSR	- 67 dB@1 MHz - 56 dB@10 MHz	- 64.3 dB@1 KHz N/A @1 MHz	- 40 dB@1 MHz - 22 dB@10 MHz	- 36 dB@1 MHz - 40 dB@10 MHz	- 55 dB@1 MHz N/A@10 MHz	- 40 dB@1 MHz - 15 dB@10 MHz	- 70 dB@1 MHz - 37 dB@10 MHz
$\Delta V_{OUT}/ V_{OUT}$ (mV/V) and rise/fall times	25 / 10 ns	130 / 60 µs	N/A	32 / 1 µs	150 / 100 ns	56 / 200 ns	75 / 100 ns
Settling time (µs)	0-Imax, < 0.6	0.1mA-Imax, < 60	N/A	0-Imax, < 15	0-Imax, < 800	50µA-Imax, < 0.4	0-Imax, < 6
Transient Load Regulation (mV/mA)	0.048	0.101	N/A	0.3	0.92	0.0556	0.14
FOM*** (ns)	8	0.0737	N/A	0.000233	6.048	0.000017	0.000264
Noise (@100KHz)	N/A	N/A	N/A	0.63 µV/$Hz^{1/2}$	N/A	N/A	0.27 µV/$Hz^{1/2}$

* The quiescent current (I_Q) is calculated from current efficiency.
** Fully characterized up to 50 mA.
***FOM = $(C_{OUT} \times \Delta V_{OUT} \times I_Q) / (I_{MAX.LOAD})^2$ [60].

IV.7. Summarizing Remarks

An internally-compensated LDO was proposed with a PSR enhancer that consists of a scaled replica of the pass transistor, a current amplifier, a current buffer, and a current mirror. The proposed PSR calibration scheme precisely tracks all loading current conditions due to the use of a scaled replica circuit, such that the supply noise is compensated even under PVT variations. A fabricated prototype of the LDO with PSR enhancer achieved a PSR better than -40 dB up to 8 MHz for different load current conditions up to 50 mA. Compared to a conventional LDO, the proposed LDO improves the PSR more than 25 dB in the critical supply noise frequency range of 0.4 – 4 MHz. The LDO fabricated in a 0.18 µm CMOS technology occupies an active area of 0.14 mm^2. Measurement results demonstrate less than 0.5% output voltage error over the entire 0 - 50 mA operating range, as well as 120 mV of overshoot and 80 mV of undershoot for a 50 mA step load current with 100 ns rise/fall times; simulation result for a 1 µs rise/fall times load variation shows that the output voltage variations are within ±70 mV while settling time reduces to 3 µs. The circuit is fully functional up to 100mA load current. The current consumption is 80 µA during regular operation and 55 µA while the standby operation. The total on-chip capacitors of the LDO sum up to 28 pF which are used for the internal frequency compensation and DC current offset cancellation in the PSR enhancer.

IV.8. Supplemental: DC Line Regulation Analysis

The small-signal equivalent model of the proposed LDO is depicted in Fig. 4.23, and the transfer function from the supply input (V_{dd}) to output (V_{OUT}) was analyzed using this small-signal equivalent model.

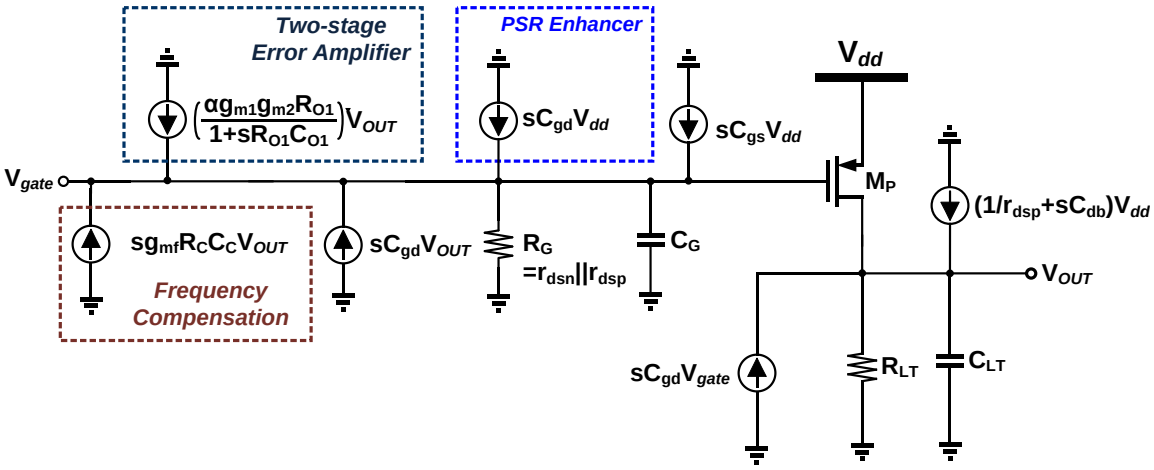


Fig. 4.24. Small-signal equivalent model of the proposed LDO.

Basic nodal analysis of the topology gives the following results:

$$V_{gate}\left(\frac{1}{R_G}+sC_G\right)=\left\{\left(\frac{\alpha g_{m1}g_{m2}R_{O1}}{1+sR_{O1}C_{O1}}\right)+s\left(C_{gd}+g_{mf}R_CC_C\right)\right\}V_{OUT}+s\left(C_{gs}+C_{gd}\right)V_{dd} \quad (4.15)$$

$$V_{OUT}\left(\frac{1}{R_{LT}}+sC_{LT}\right)=g_{mp}\left(V_{dd}-V_{gate}\right)+sC_{gd}V_{gate}+\left(\frac{1}{r_{dsp}}+sC_{db}\right)V_{dd} \quad (4.16)$$

From (4.15) and (4.16), it follows that the supply gain is computed as

$$\frac{V_{OUT}}{V_{dd}}=\frac{1+g_{mp}r_{dsp}\left[1-\left\{\frac{s\left(C_{gs}+C_{gd}\right)}{(1/R_G)+sC_G}\right\}\right]+s\left[C_{db}+C_{gd}\left\{\frac{s\left(C_{gs}+C_{gd}\right)}{(1/R_G)+sC_G}\right\}\right]r_{dsp}}{r_{dsp}\left(\frac{1}{R_{LT}}+sC_{LT}\right)+\left(g_{mp}-sC_{gd}\right)\left(\frac{r_{dsp}}{(1/R_G)+sC_G}\right)\left\{\left(\frac{\alpha g_{m1}g_{m2}R_{O1}}{1+sR_{O1}C_{O1}}\right)+s\left(C_{gd}+g_{mf}R_CC_C\right)\right\}} \quad (4.17)$$

At medium and high frequency, the supply gain is expressed by

$$\frac{V_{OUT}}{V_{dd}} \cong \frac{1+s(C_{db}+C_{gd})r_{dsp}}{r_{dsp}\left(\frac{1}{R_{LT}}+sC_{LT}\right)+(g_{mp}-sC_{gd})\left(\frac{r_{dsp}}{sC_G}\right)\left\{\left(\frac{\alpha g_{m1}g_{m2}R_{O1}}{1+sR_{O1}C_{O1}}\right)+s(C_{gd}+g_{mf}R_CC_C)\right\}} \tag{4.18}$$

The DC line regulation is obtained as follow:

$$\left.\frac{V_{OUT}}{V_{dd}}\right|_{s=0} = \frac{1+g_{mp}r_{dsp}}{\left(\frac{r_{dsp}}{R_{LT}}\right)+(\alpha g_{mp}r_{dsp}g_{m1}g_{m2}R_{O1}R_G)} \tag{4.19}$$

As shown by equation (4.19), the DC line regulation of the proposed LDO with PSR enhancer and frequency compensation is inversely proportional to the gain of the error amplifier ($g_{m1}g_{m2}R_{O1}R_G$) and the feedback factor (α). These properties are almost identical as for conventional LDOs. Hence, the PSR enhancement and frequency compensation circuitry does not significantly affect the performance of the DC line regulation of the LDO, which can be optimized during the design based on the above equations.

V. SUMMARY AND CONCLUSIONS

The ADC is one of the most critical blocks of the receiver in the wireless communication system. ΣΔ ADCs have become popular because of their "digital-friendly" architectures, high efficiency, and high resolution. In particular, CT ΣΔ ADCs that have built-in anti-aliasing filters and are good candidates for achieving high performances compared to DT ΣΔ ADCs.

To prevent the performance degradation of CT ΣΔ ADC due to the analog loop filter located in front of the sampling operation, the design considerations and performances of analog loop filters were addressed in this dissertation. Between the two popular continuous-time filter architecture types, which are active-RC and G_m-C, the 5^{TH}-order active-RC filter was implemented to meet the dynamic range requirement of the ADC in IBM 90 nm technology. Since the first biquadratic section of the loop filter has to have a wide linear range and low noise, a non-linear cancellation scheme with source degeneration technique was employed in the amplifiers of the first biquadratic section.

For the design of low-power CT LP ΣΔ modulators with feed-forward compensation the current-mode adder-quantizer with the common-gate stage and current comparison stage were presented to replace summing amplifier demands for higher power consumption at the same operating speed. Compared with a conventional voltage-mode summing amplifier and quantizer, the proposed current-mode adder-quantizer consumes 53% less power while offering superior performance. In addition, the proposed approaches do not need an additional resistor string to generate the reference voltages, and power supply limitations due to scaling have significantly less impact than voltage-

mode flash architectures, which suffer from voltage headroom restrictions during the generation of the reference voltages with resistor ladders. A 3-bit prototype design has an ENOB that is higher than 2.6 bits up to 2 GHz clock frequency with 10 MHz full-power input. At 1.48 GHz clock frequency, the static DNL and INL errors are within -0.206 LSB and 0.206 LSB, respectively. The architecture's SNDR is 18.6dB with a 125MHz input signal at 1.25 GHz clock frequency. The proposed current-mode flash ADC core dissipates 3.34 mW power from a 1.2 V supply while operating at 1.48 GHz. The core area of the ADC including its biasing circuitry is 0.0276 mm^2. It was designed and fabricated in IBM 90 nm CMOS technology.

Another circuit developed as a result of this research is the external capacitor-less LDO that has a high PSR at high frequencies is presented herein as a way to alleviate the supply noise issue between the switching power converter (SWPC) and the highly sensitive RF and/or high-performance analog blocks in the single chip solution. Fundamental PSR limitations due to several paths between the noisy supply and the LDO output in typical LDOs were analyzed, and a novel solution to improve the PSR at high frequencies without a bulky external capacitor was developed in this work. Experimentally, the effectiveness of the new technique was verified with an LDO fabricated in IBM 0.18 μm CMOS technology with a power supply of 1.8 V and a drop-out voltage of 200 mV. The active core chip area of this prototype is 0.14 mm^2, and the entire proposed LDO consumed 55 μA of quiescent current while in standby operation. Compared to a conventional uncompensated LDO, the proposed architecture presents a PSR improvement of 34 dB and 25 dB at 1MHz and 4 MHz, respectively. Furthermore,

the proposed PSR calibration scheme precisely tracks all loading current conditions (0 - 50 mA load current) due to the use of a scaled replica circuit, such that the supply noise is compensated even in the presence of PVT variations.

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