DESIGN, SIMULATION AND MODELING OF INSULATED GATE BIPOLAR TRANSISTOR

A Thesis

by

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MASTER OF SCIENCE

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ABSTRACT

The market for Insulated Gate Bipolar Transistor (IGBT) is growing and there is a need for techniques to improve the design, modeling and simulation of IGBT. In this thesis, we first developed a new method to optimize the layout and dimensions of IGBT circuits based on device simulation and combinatorial optimization. Our method leads to the optimal IGBT layout consisting of hexagons, which is 6 % more efficient in terms of performance (current per unit area) over that of squares, and up to 80 % more efficient than rectangles. We also explored several techniques to reduce the time used for device simulation. In particular, we developed an accurate Verilog-A description based on the Hefner model. For transient simulation, the time used by SPICE on the Verilog-A model is only 1/10000 of that used by device simulation on the device structure. The SPICE results, though contain some inaccuracies in the details, match device simulation in the general trend. Due to the effectiveness and efficiency of our methods, we propose their application in designing better power electronic circuits and shorter turn-around time.

DEDICATION

To my parents

ACKNOWLEDGEMENTS

I would like to thank my committee chair, Dr. Weiping Shi, and my committee members, Dr. Anxiao Jiang and Dr. Peng Li, for their guidance and support throughout the course of this research. I would like to express my gratitude to Zhixing Li for his help with running 2-D device simulations.

I would also like to thank my friends and colleagues for making my journey pleasant and motivating me throughout. I would like to express my gratitude to the department staff who helped me through various processes and enabled me to complete paperwork in a timely manner.

Finally, I would like to thank my family for all the encouragement and support during my graduate studies and research.

NOMENCLATURE

IGBT	Insulated Gate Bipolar Transistor
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
GTO	Gate Turn-Off Thyristor
IGCT	Integrated Gate Commutated Thyristor

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CHAPTER I

INTRODUCTION

Overview and Applications

Power semiconductor devices are essential to the design of large-scale power electronic circuits and systems. This has resulted in renewed focus on research about novel device materials and structures. There are many types of power semiconductor devices available today. These include the thyristor, power MOSFET, power BJT, GTO, IGCT and IGBT. Our focus in this thesis is on IGBT and its advantages over other devices are explained below.

Insulated Gate Bipolar Transistor (IGBT) has three terminals. It was invented in the 1980's [1] and is mainly used as a fast electronic switch. IGBT combines the advantages of the traditional MOSFET and BJT. It has the property of high input impedance gate control resulting in very low driving losses. The major advantage of IGBT over power MOSFET is its low forward voltage drop due to conductivity modulation. Moreover, the current density in an IGBT is significantly large, resulting in savings in device area and cost. [2]

IGBT's have found applications in areas as diverse as railway traction inverters, electric cars, renewable energy, switched mode power supplies (SMPS) and uninterruptible power supplies (UPS). IGBT's are being manufactured by several companies in the voltage range of 100 V - 2000 V with current ratings of 200 A - 1000 A.

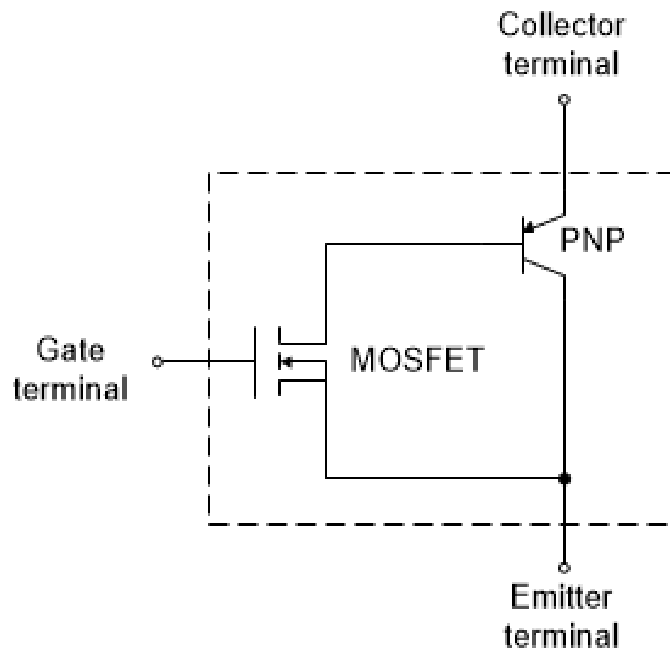

Figure 1: Simplified equivalent circuit of IGBT

Figure 1 shows the simplified equivalent circuit of IGBT. Figure 2 shows the circuit symbol of an n-Channel IGBT.

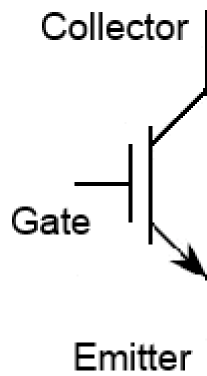

Figure 2: Circuit symbol of n-channel IGBT

Figure 3 shows the 3-D cross-section of an n-channel IGBT.

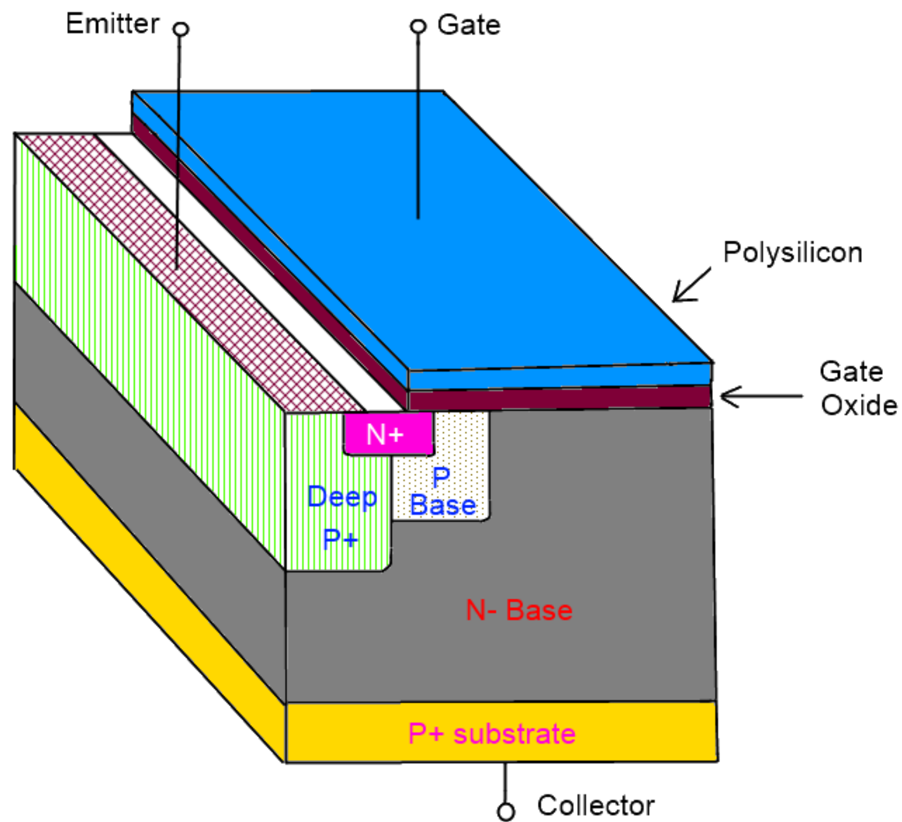

Figure 3: IGBT 3-D cross-section

Operating Modes

IGBT can operate in any of the following 3 modes:

1. Reverse-Blocking Mode- The gate and emitter are shorted together and a positive voltage is applied on the N+ emitter, while a negative voltage is applied on the P+ collector.
2. Forward-Blocking Mode- The gate and emitter are shorted together as before. But, a negative voltage is applied to the N+ emitter, while a positive voltage is applied on the P+ collector.

3. Forward-Conducting Mode- The gate and emitter are not shorted in this mode. Positive voltages are applied to the gate and collector, while a negative (or ground) voltage is applied on the N+ emitter. A large number of holes are injected from the P+ substrate and this results in high-level injection occurring in the N- base. Due to its relatively lesser doping, the N- base offers large resistance in the reverse-blocking mode. But, conductivity modulation occurs in the forward-conducting mode due to the extremely large number of holes injected. This is the root cause of the low forward voltage drop.

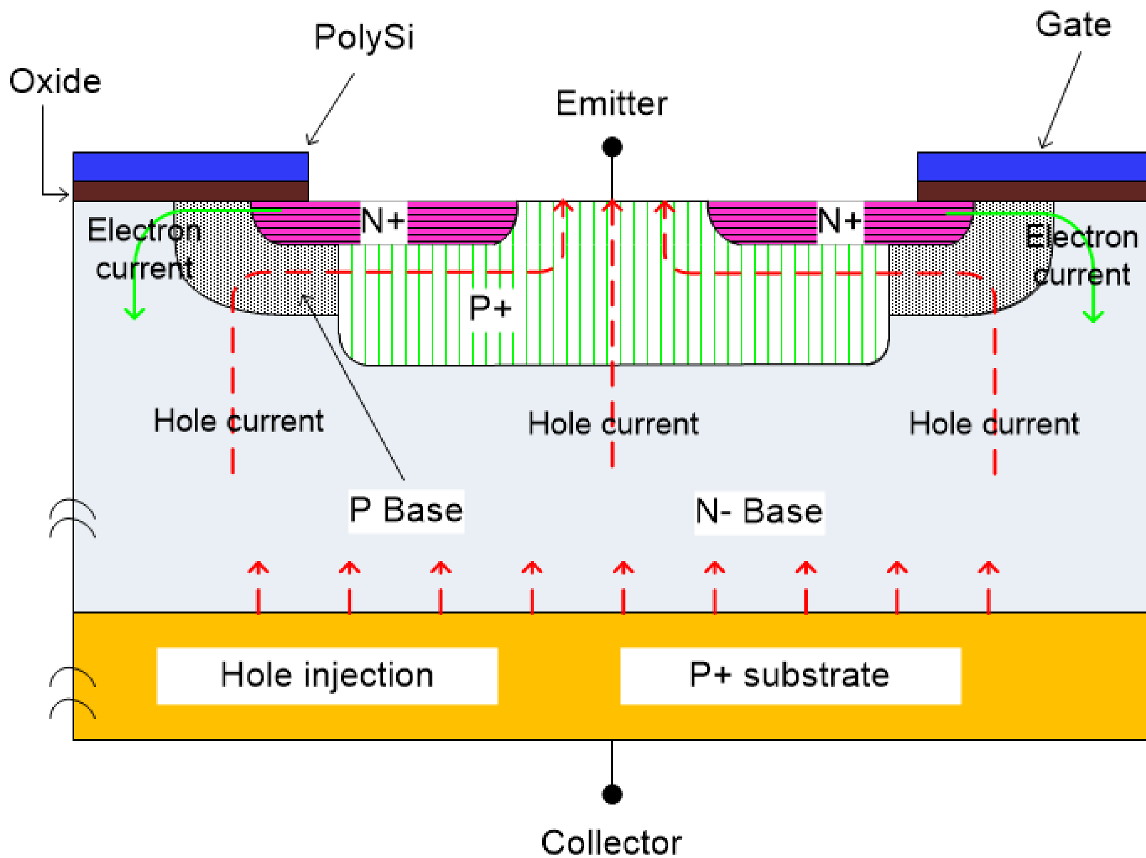

Figure 4: Explanation of internal currents

Figure 4 shows the electron and hole currents flowing inside the IGBT in forward conducting mode.

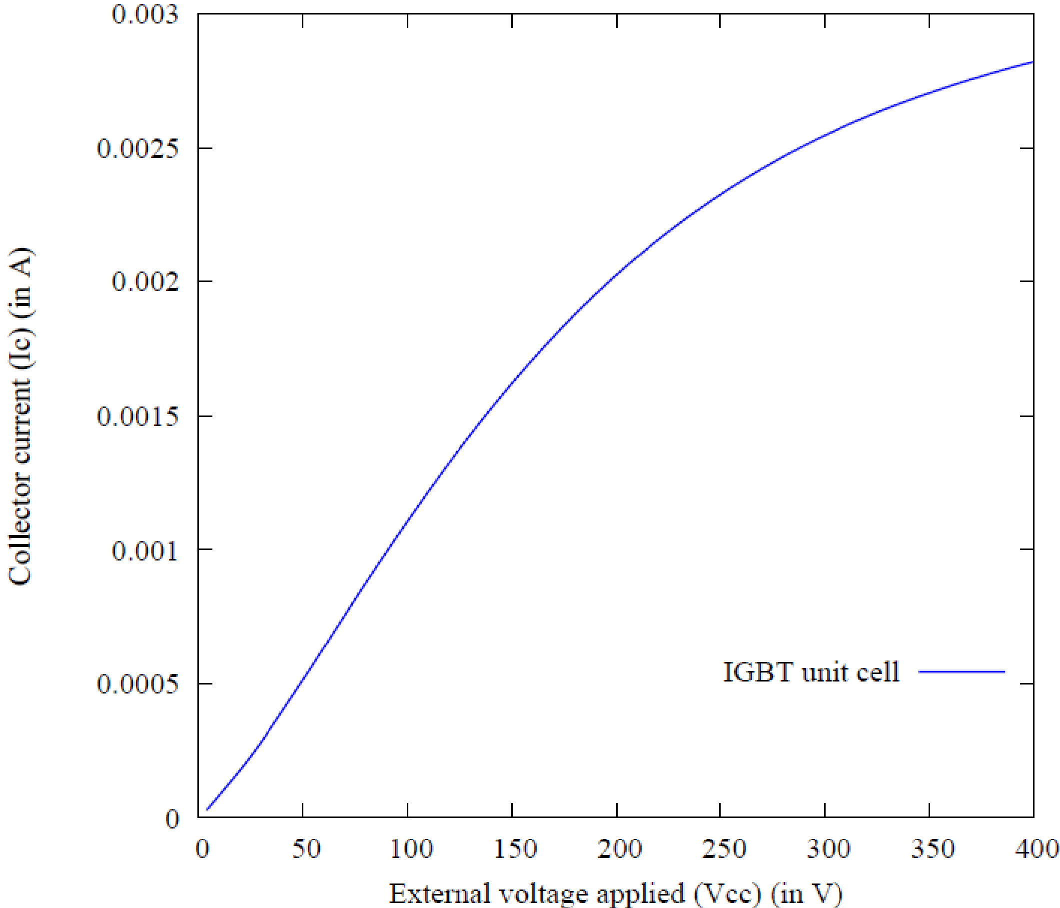

Figure 5: Typical I-V characteristics of IGBT unit cell

Figure 5 shows the typical I-V characteristics of an IGBT unit cell in forward conducting mode.

CHAPTER II

DESIGN OF IGBT

Previous Work

Cell designs for IGBT have been proposed in a 1988 paper by Baliga et al. [3]. These designs include the linear cell, square cell, rounded-end linear cell and atomic-lattice-layout cell. IGBT cell design as a latch-up prevention measure has been discussed in [2]. The cell designs proposed here include the multiple surface shorts cell and the circular cell. However, the optimization of IGBT design including sizing and layout has not been discussed in previous literature.

Design Flow

The IGBT design flow is different from the traditional MOSFET design flow shown in Figure 6. In the MOSFET design flow, the feature size (also called channel length) is chosen by the foundry. Other process parameters like doping concentration in various regions also under the control of the foundry. They perform device simulation and provide a “ready-to-use” spice model to their customers.

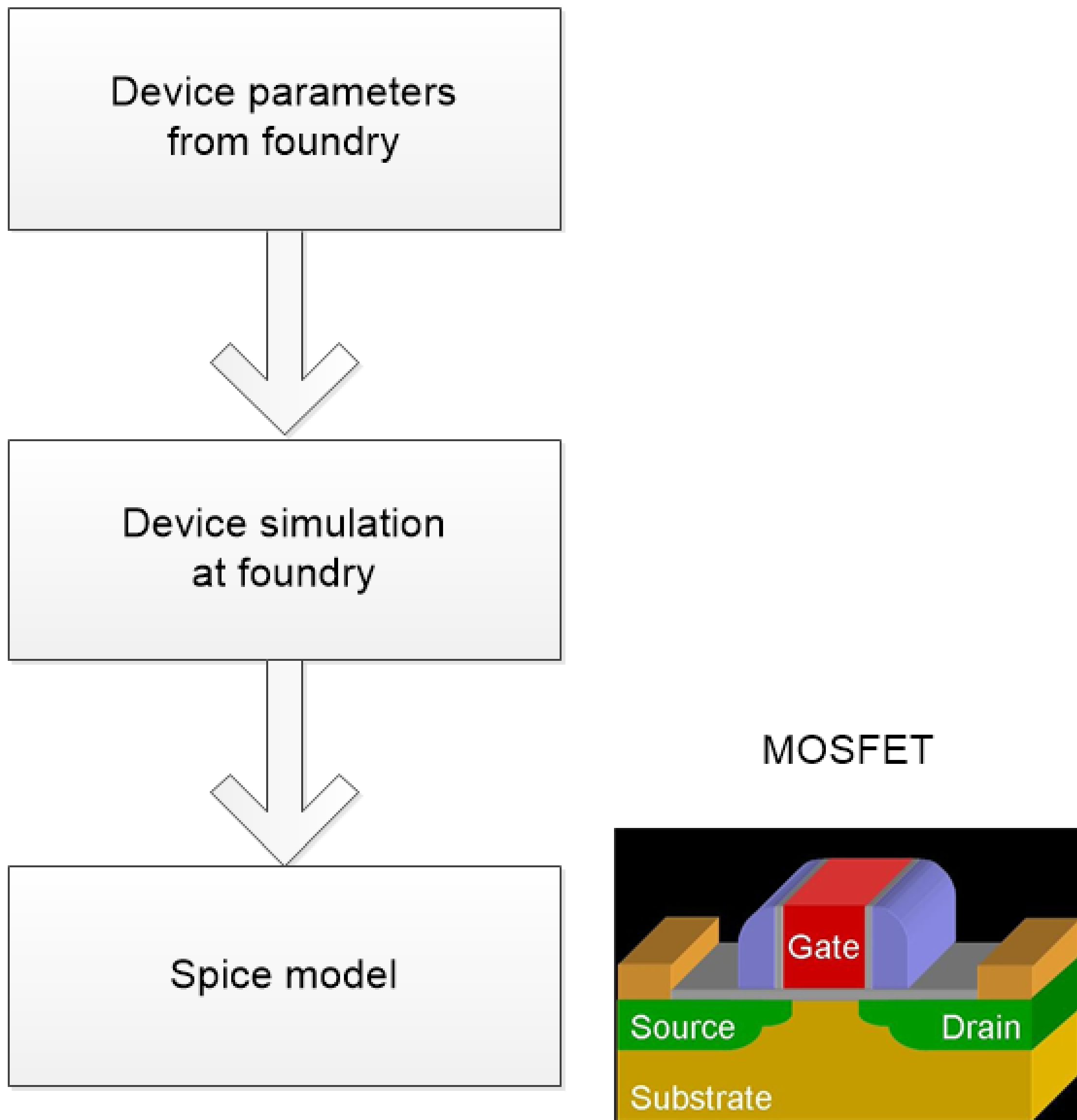

Figure 6: MOSFET design flow

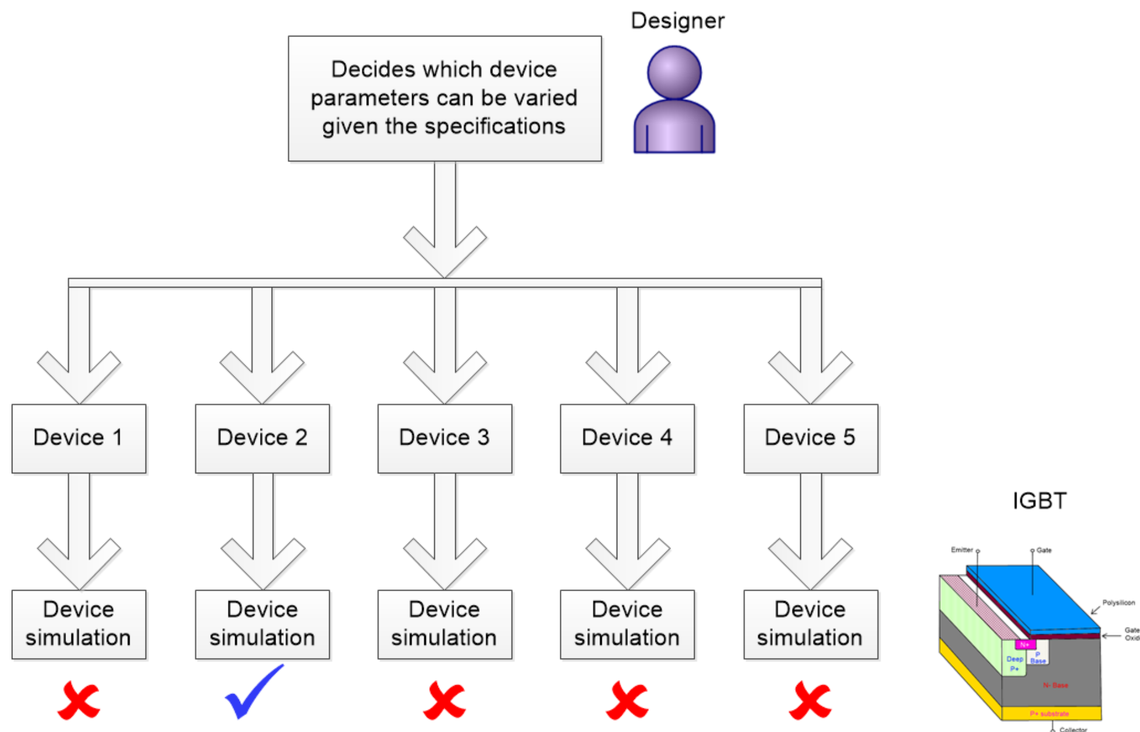

Figure 7: IGBT design flow

Figure 7 shows the IGBT design flow. As shown in the figure, the designer decides which process parameters can be varied to evaluate and eventually select the device with the best performance.

Process Parameters

We have observed that the dimensions of the device and the doping concentration in various regions need to be carefully chosen. This is required to avoid turning on of the parasitic transistor (a phenomenon known as latch-up). During latch-up, the current density increases beyond the critical limit and the device is likely to get damaged. Figure 8 from [2] shows the process parameters used to create the IGBT unit cell. We shall vary the emitter length (e) and gate length (g) as explained later.

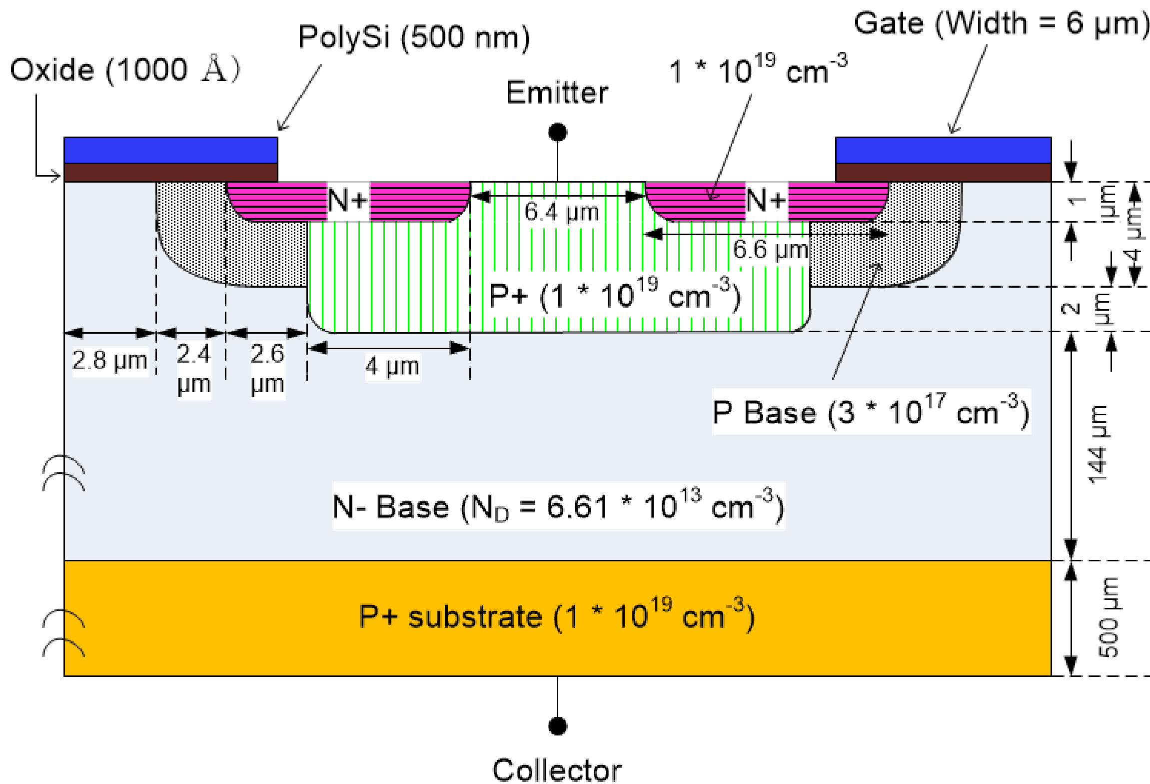

Figure 8: Process parameters used to create IGBT unit cell

Design Approach

We formulate the design problem and proceed to solve it in 3 steps.

- Problem formulation: Find the dimensions, layout and shape of IGBT unit cell which meets the objective, subject to some constraints.
- Objective: Get the best performance (current per unit area)
- Constraints: $e > e_{min}$, $n = 5$ µm, $g > g_{min}$

We have constrained n for ease of analysis. The cross-section of the IGBT is shown in Figure 9.

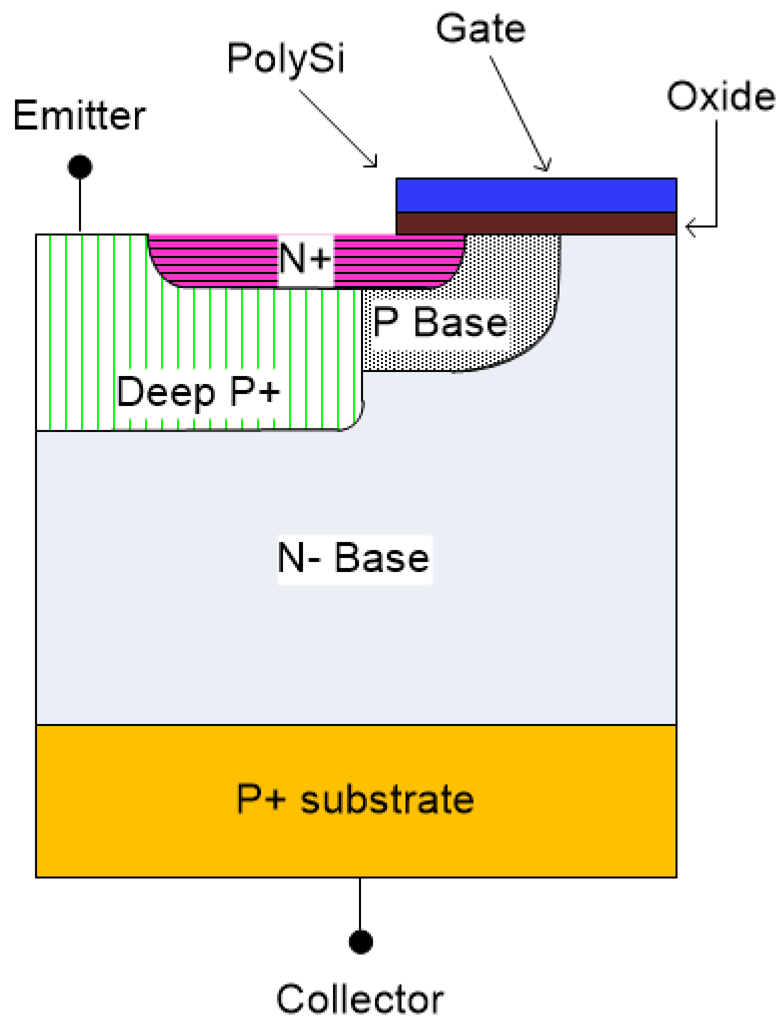

Figure 9: Cross-section of IGBT (Used in design problem)

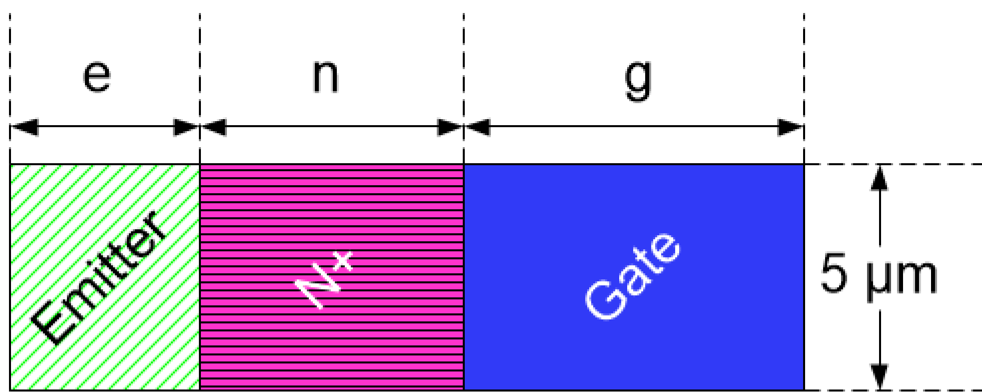

Figure 10: Top view of IGBT (Used in design problem)

Figure 10 shows the top view of the linear IGBT used in this design problem. e, n, g can be understood from this figure.

Step 1: Decide optimal dimensions

We vary e in the range 2-6 µm and g in the range 4-8 µm. We compare the various devices by applying a gate bias of 13 V and a collector bias of 400 V. The results of this experiment are shown in Table 1.

We observe that e = 2 µm, n = 5 µm, g = 8 µm gives the best performance.

Table 1: Optimization of dimensions

e (in µm)	n (in µm)	g (in µm)	Collector current (in A)	Current density (in A/cm^2)
2	5	4	3.367E-12	-
2	5	5	3.285E-06	-
2	5	6	1.041E-04	160.15
2	5	7	1.361E-04	194.42
2	**5**	**8**	**1.647E-04**	**219.60**
3	5	4	3.673E-12	-
3	5	5	4.813E-06	-
3	5	6	1.157E-04	165.28
3	5	7	1.202E-04	160.26
3	5	8	1.472E-04	184.00

Table 1 Continued

e (in µm)	n (in µm)	g (in µm)	Collector current (in A)	Current density (in A/cm^2)
4	5	4	3.937E-12	-
4	5	5	5.682E-06	-
4	5	6	9.809E-05	130.78
4	5	7	1.229E-04	153.62
4	5	8	1.347E-04	158.47
5	5	4	4.266E-12	-
5	5	5	1.203E-06	-
5	5	6	7.501E-05	93.76
5	5	7	1.396E-04	164.23
5	5	8	1.374E-04	152.66
6	5	4	3.565E-12	-
6	5	5	1.669E-06	-
6	5	6	8.978E-05	105.62
6	5	7	1.358E-04	150.88
6	5	8	1.439E-04	151.47

Step 2: Decide layout

We use the optimal dimensions (e = 2 µm, n = 5 µm, g = 8 µm). We employ the combinatorial approach to arrive at the best layout.

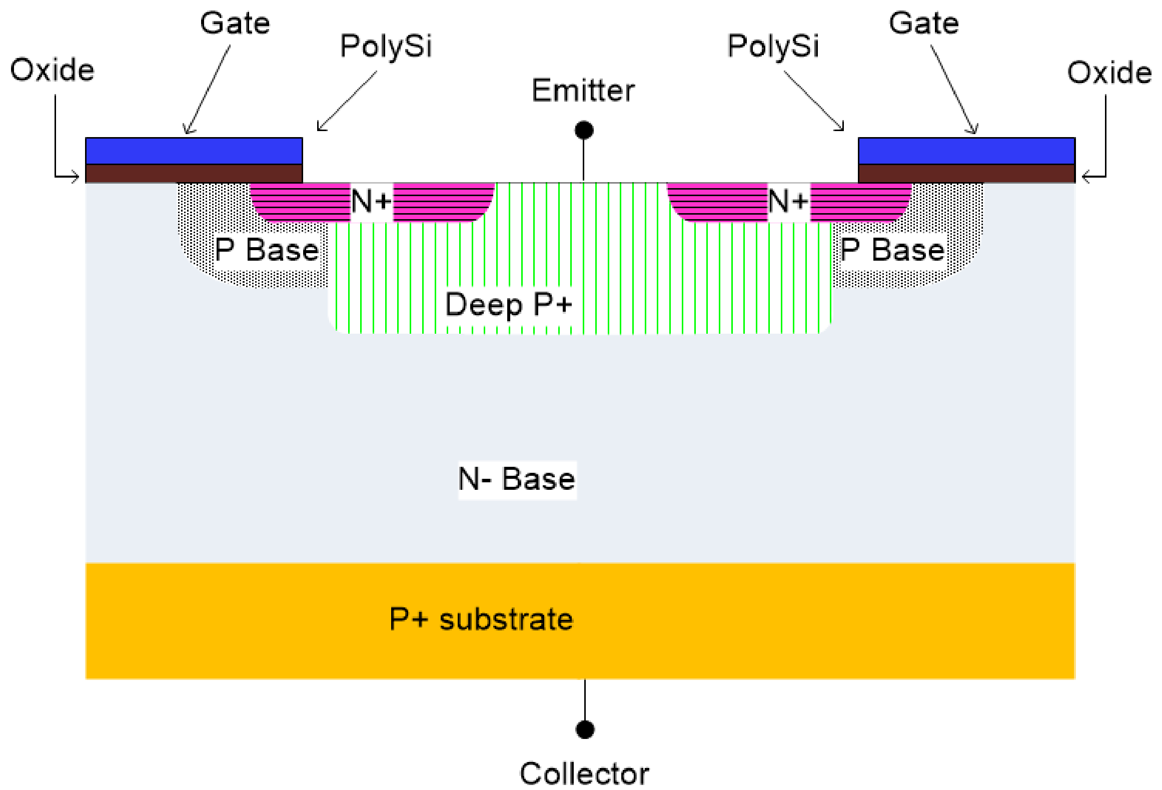

Figure 11: GNEENG cross-section

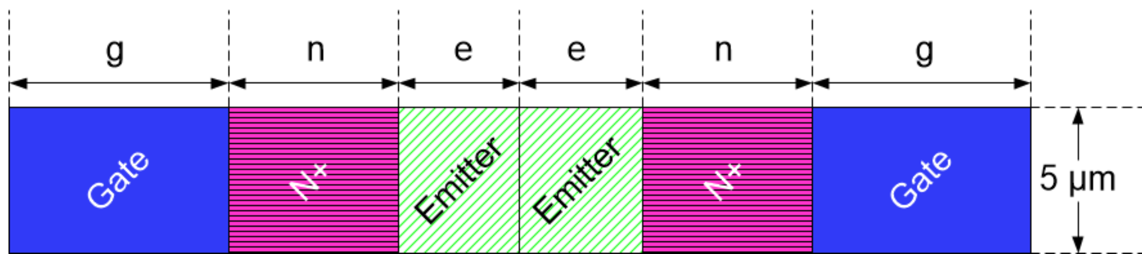

Figure 12: GNEENG top view

Figure 11 shows the cross-section of the GNEENG layout. Figure 12 shows the top view of the GNEENG layout.

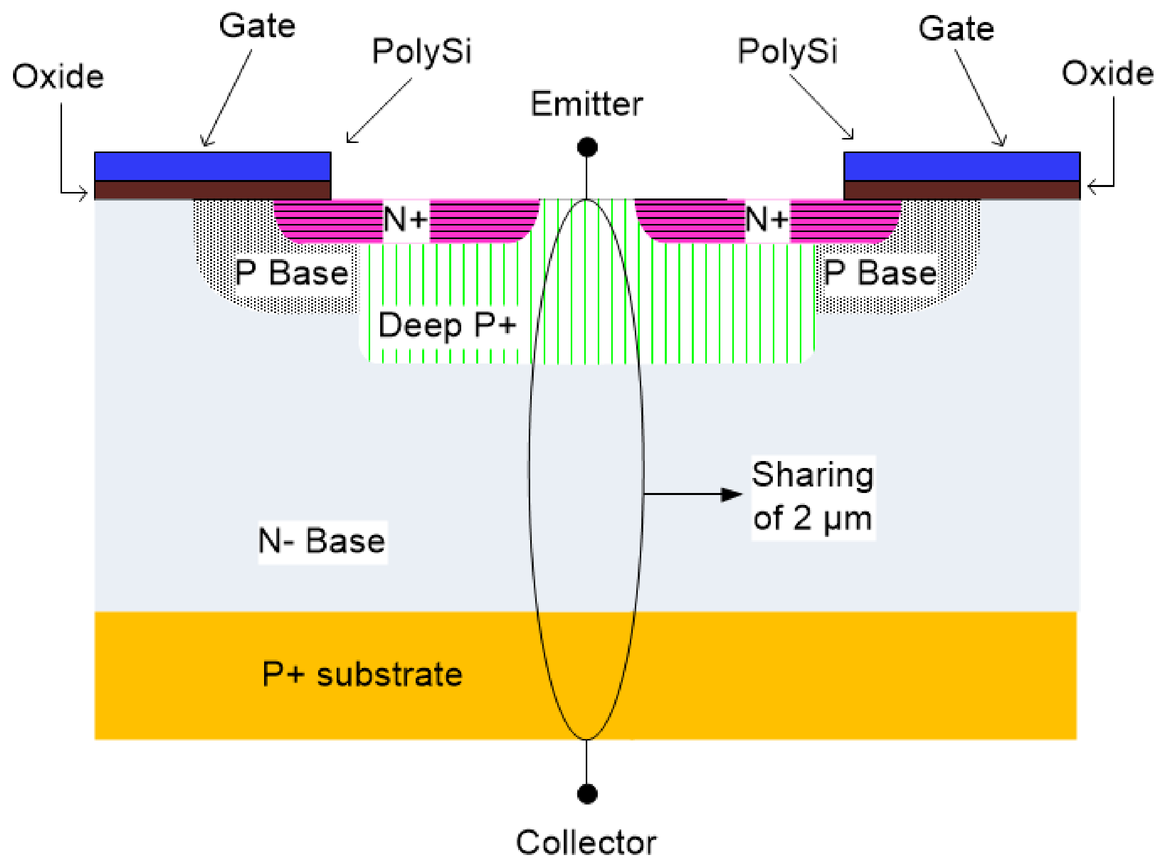

Figure 13: GNENG cross-section

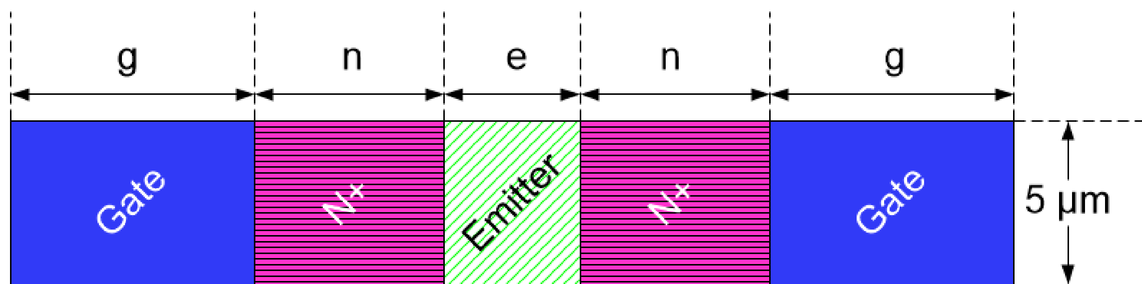

Figure 14: GNENG top view

Figure 13 shows the cross-section of the GNENG layout. Figure 14 shows the top view of the GNENG layout.

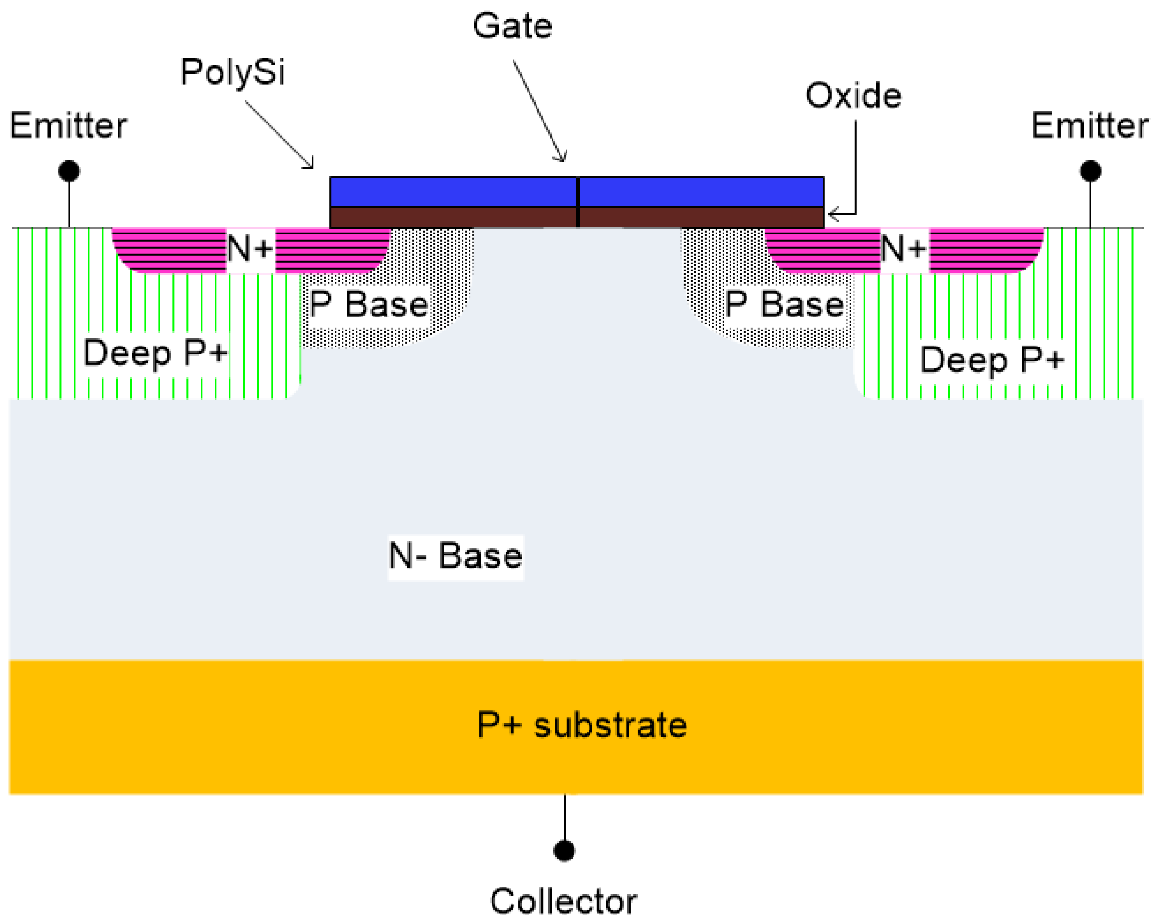

Figure 15: ENGGNE cross-section

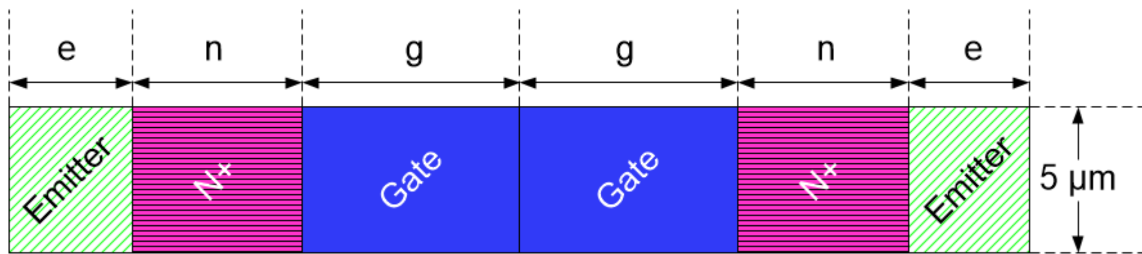

Figure 16: ENGGNE top view

Figure 15 shows the cross-section of the ENGGNE layout. Figure 16 shows the top view of the ENGGNE layout. Figure 17 shows the cross-section of the ENGNE layout. Figure 18 shows the top view of ENGNE layout.

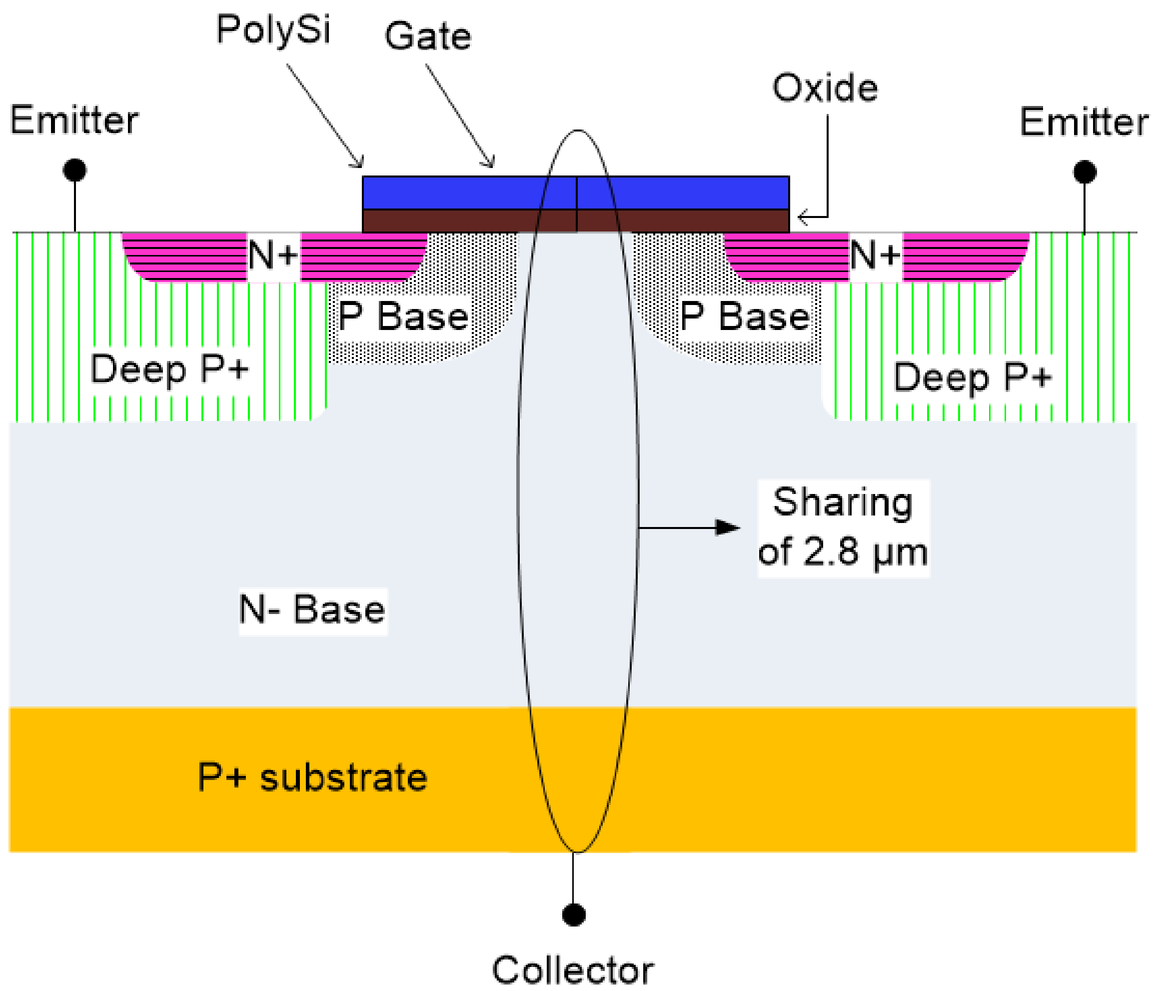

Figure 17: ENGNE cross-section

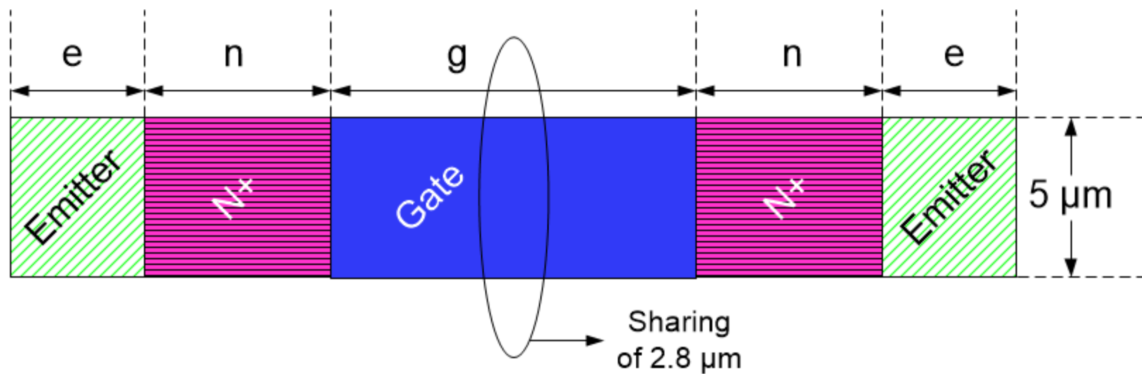

Figure 18: ENGNE top view

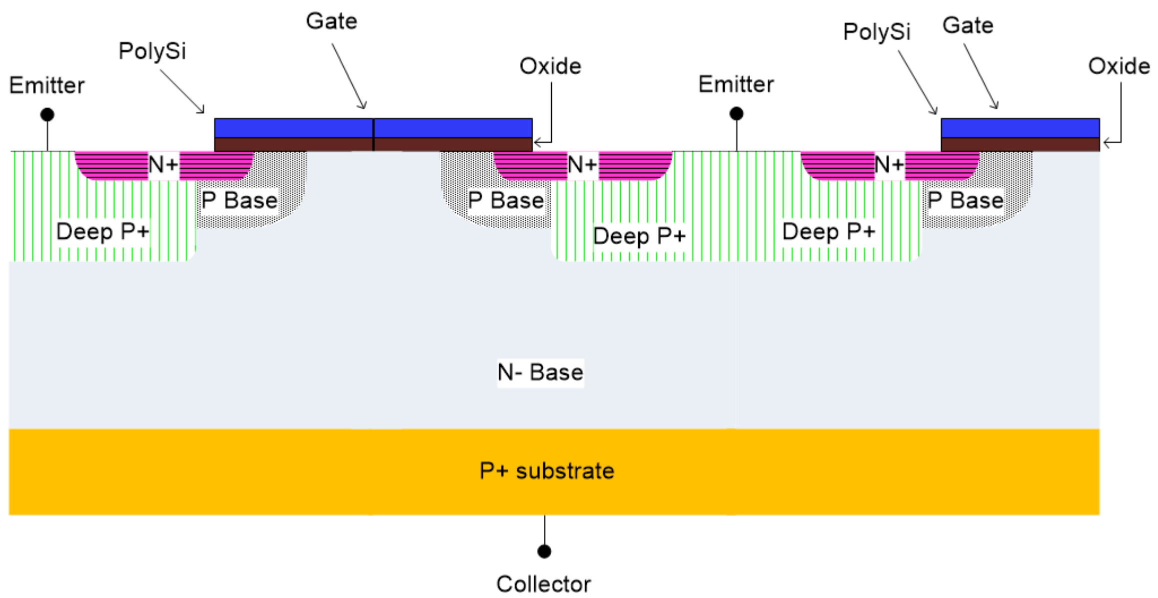

Figure 19: ENGGNEENG cross-section

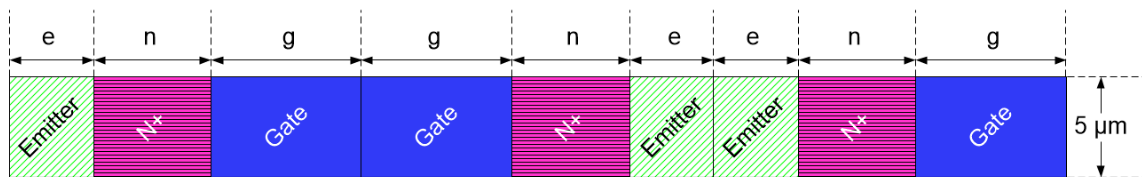

Figure 20: ENGGNEENG top view

Figure 19 shows the cross-section of the ENGGNEENG layout. Figure 20 shows the top view of the ENGGNEENG layout.

Table 2: Selection of layout

Layout style	Collector current (in A)	Current density (in A/cm^2)
ENG	1.647E-04	219.6
GNEENG	3.106E-04	207.1
GNENG (sharing of 2 μm)	**3.103E-04**	**221.6**
ENGGNE	3.476E-04	218.4
ENGNE (sharing of 2.8 μm)	3.004E-04	220.8
ENGGNEENG	4.304E-04	191.2

Table 2 compares various layout styles based on their current per unit area. GNENG layout is found to be the most optimal layout style. We can create regular arrays of GNENG layout.

Step 3: Decide shape

We explore various IGBT shapes and evaluate their performance. Figure 21 shows the top view of the linear IGBT. Figure 22 shows the top view of the rectangular IGBT.

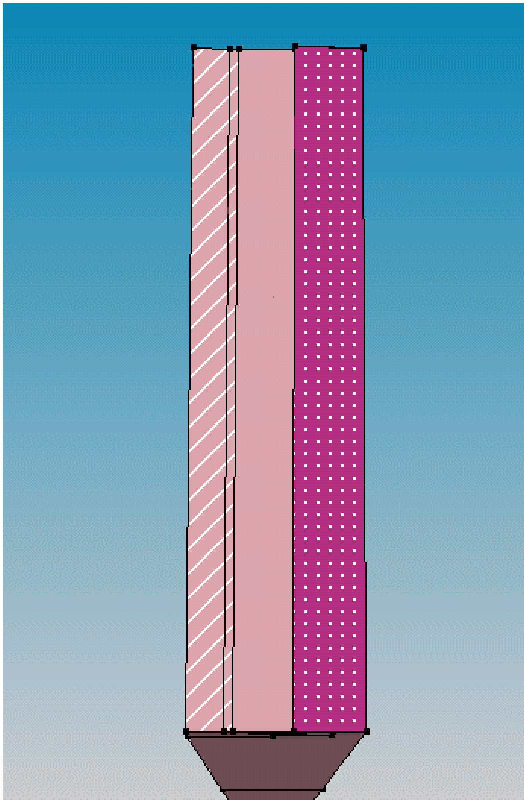

Figure 21: Linear IGBT

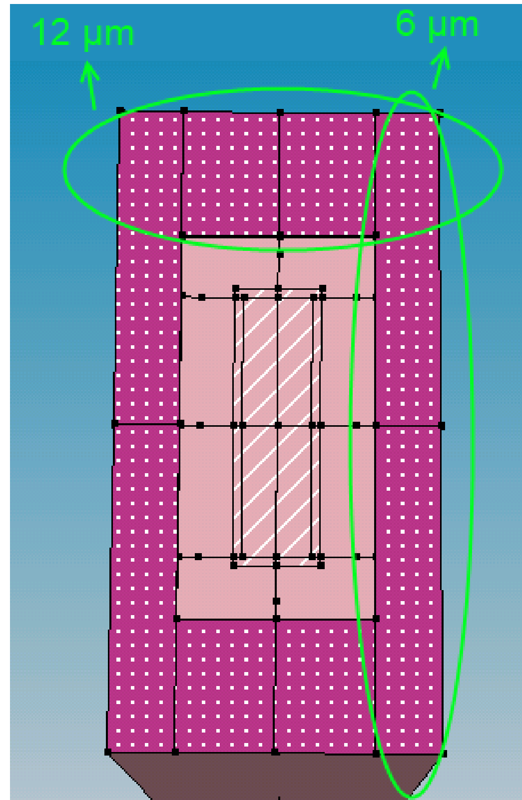

Figure 22: Rectangular IGBT

Figure 23 shows the top view of the square IGBT. Figure 24 shows the top view of the circular IGBT.

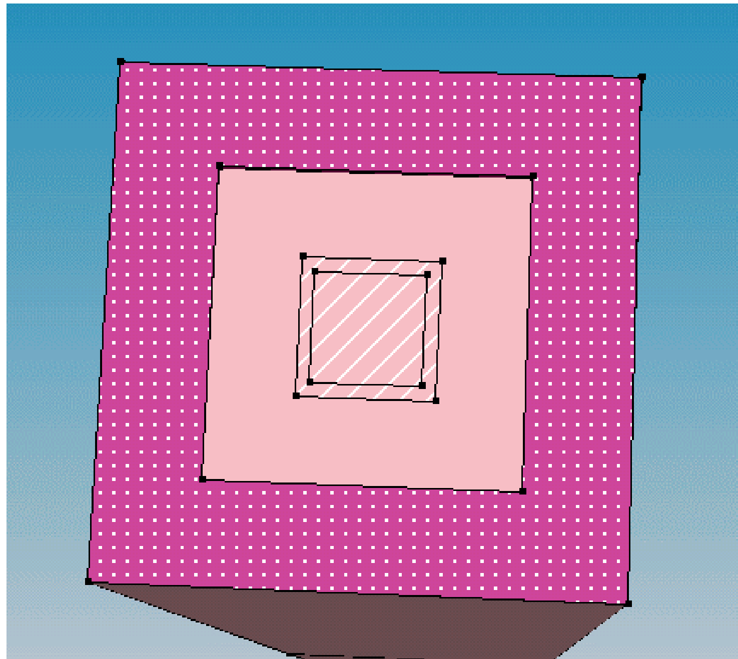
Figure 23: Square IGBT

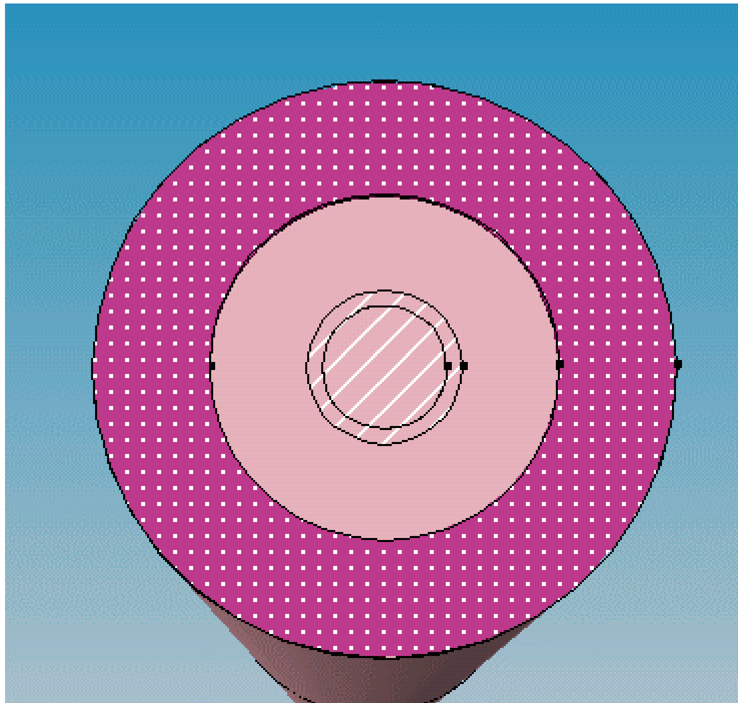
Figure 24: Circular IGBT

Table 3: Comparison of various shapes (e = 4 µm, n = 5 µm, g = 6 µm)

Type of cell	Gate type and width	Collector current (in A)	Current density (in A/cm^2)
Linear IGBT (15 µm * 60 µm)	Linear (6 µm width)	1.26E-03	140.0
Square IGBT (30 µm * 30 µm)	Square ring (6 µm width)	2.82E-03	313.3
Circular IGBT (30 µm diameter)	Circular ring (6 µm width)	1.80E-03	254.6
Rectangular IGBT (30 µm * 60 µm)	Rectangular ring (6 µm, 12 µm width)	4.65E-03	258.3

Table 3 compares various shapes according to their current per unit area. This comparison is performed at non-optimal dimensions. Table 4 compares the square and circular IGBT's at the optimal dimensions from Step 1.

Table 4: Square vs. circular IGBT (e = 2 µm, n = 5 µm, g = 8 µm)

Shape	Layout style	Collector current (in A)	Current density (in A/cm^2)
Square	GNEENG	3.008E-03	334.2
Square	GNENG (sharing of 2 µm)	Device goes into latch-up	-
Circular	GNEENG	2.506E-03	354.5
Circular	GNENG (sharing of 2 µm)	Device goes into latch-up	-

We observe that the device with GNENG layout goes into latch-up. This is because the emitter length (e) is too small. Sharing of emitter should be possible at higher values of e.

We conclude that the circular IGBT with GNEENG layout (e = 2 µm, n = 5 µm, g = 8 µm) is optimal.

IGBT Arrays

We can create regular IGBT arrays using the optimal design. However, the disadvantage of the circular array is that the space between circles in not utilized. Hence, we propose a hexagonal IGBT array.

Figure 25 shows a regular hexagonal IGBT array. Sentaurus does not allow us to create 3-D hexagonal shapes. However, the hexagonal array can be considered an approximation of the circular array. Hence, the hexagonal array is most efficient in terms of current per unit area.

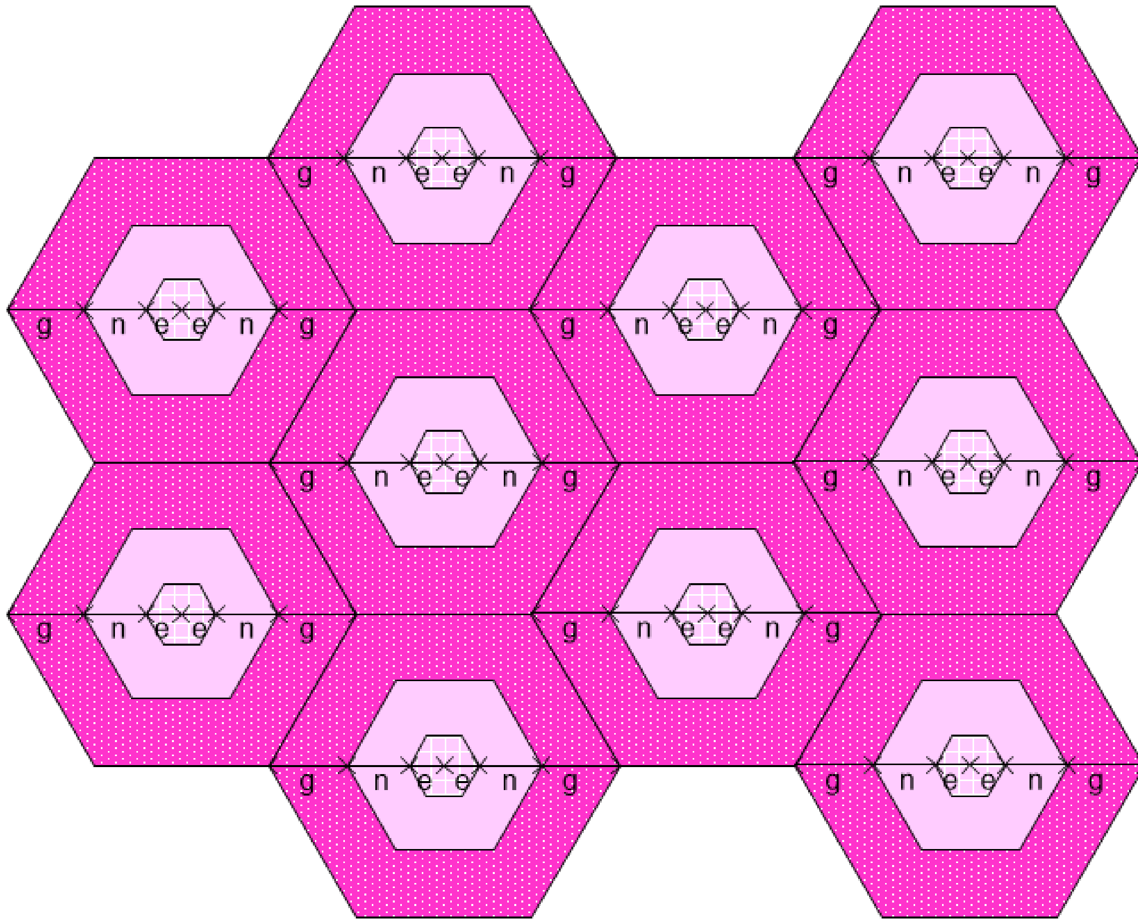

Figure 25: Proposed hexagonal IGBT array

Overall performance gain

From Table 3 and Table 4, we conclude that the performance gain (current per unit area) of the hexagonal array is 6 % over that of a square array and asymptotically approaches 80 % over that of a rectangle array.

CHAPTER III

SIMULATION AND MODELING OF IGBT

In this chapter, we describe some techniques used to reduce design time. We can use 2-D device simulations to arrive at the optimal dimensions and layout. On the other hand, we could use a Verilog-A model for faster circuit design.

Previous Work

Accurate IGBT SPICE models were first developed in the 1990's [4], [5], [6]. VHDL-AMS models have also been created recently. The VHDL-AMS model in [7] takes into account the temperature dependence of IGBT characteristics and proposes a novel electro-thermal coupling simulation. However, the existing Verilog-A models are quite basic. The model by Lauritzen et al. is described in [8]. This basic Verilog-A model uses the lumped charge approach for easier parameter extraction. In the lumped charge approach, magnitudes of electron and hole charges are calculated at few locations inside the device. Physical equations are used to derive internal voltages and currents from these charges.

2-D Simulation

The first step is to create a 2-D cross-section of the linear IGBT as shown in Figure 26.

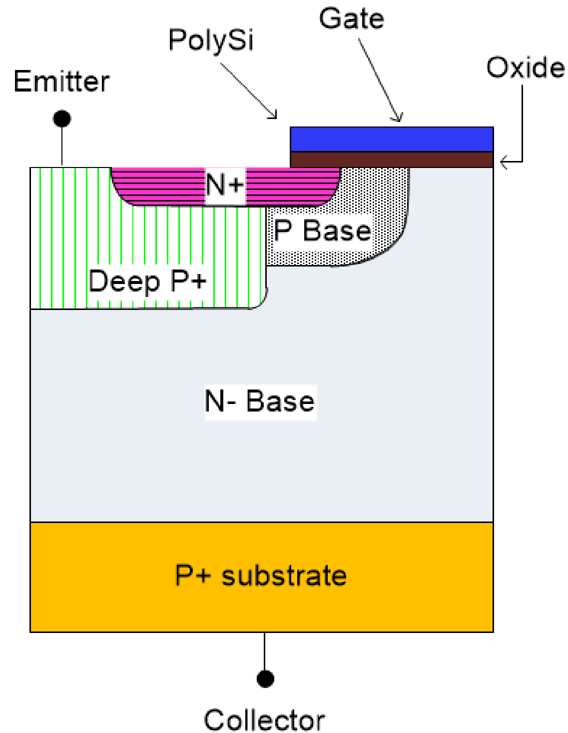

Figure 26: 2-D cross-section of IGBT

Optimization of dimensions

In our 2-D simulations, we vary e in the range 2-18 μm, n in the range 1-11 μm and g in the range 4-20 μm. Please note that in this experiment we have removed the constraint n = 5 μm and we are sweeping e, n, g over a much larger range compared to the experiment described in Chapter II. We compare the various devices by applying a gate bias of 13 V and a collector bias of 400 V.

We observe that e = 2 μm, n = 11 μm, g = 10 μm gives the best performance.

The results of this experiment are shown in the following figures. It is not possible to show all data points in one figure because all 3 parameters e, n, g were varied simultaneously.

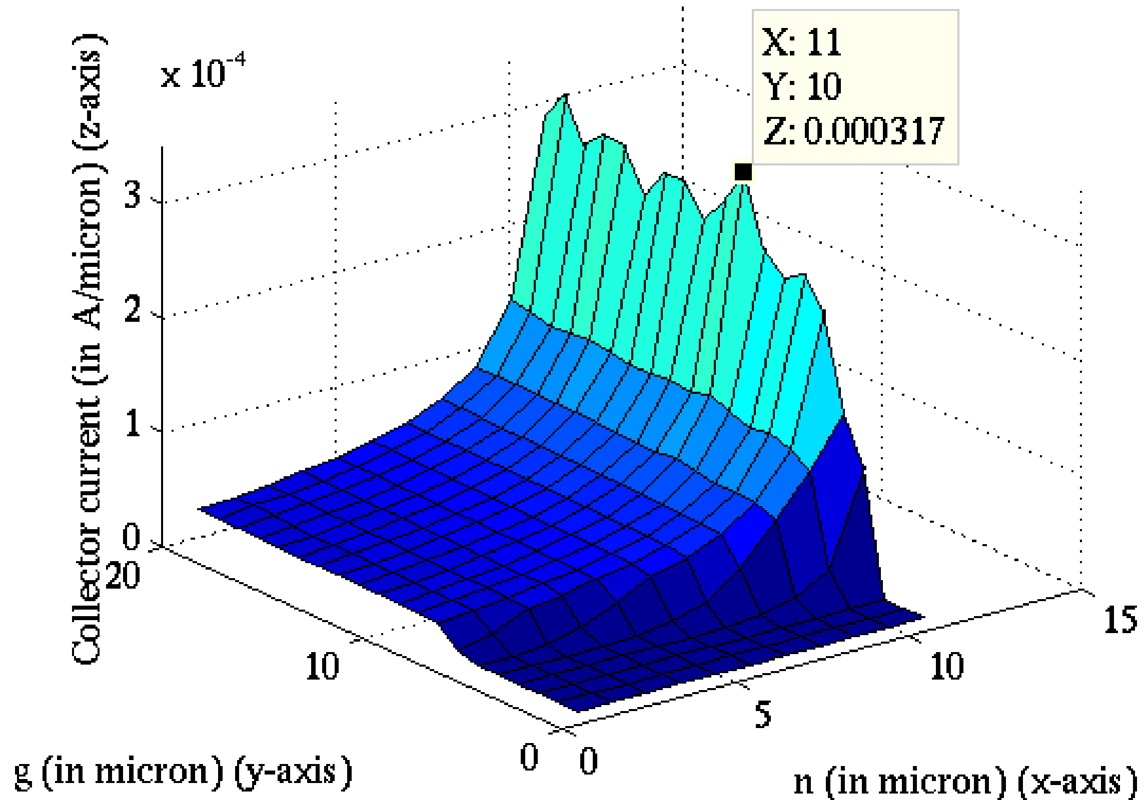

Figure 27: Collector current from 2-D simulation (e = 2 μm)

Figure 27 shows the collector current (in A/μm) from 2-D simulation keeping e fixed at 2 μm.

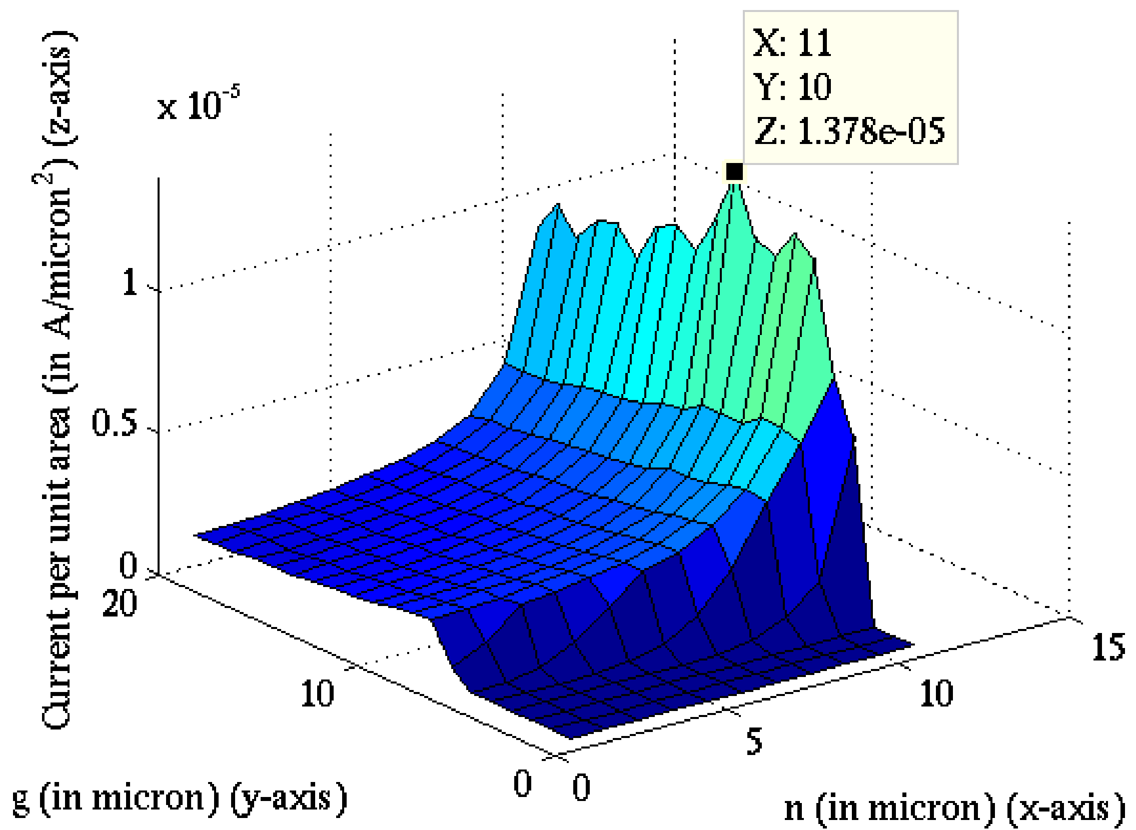

Figure 28: Current per unit area from 2-D simulation (e = 2 μm)

Figure 28 shows the current per unit area keeping e fixed at 2 μm.

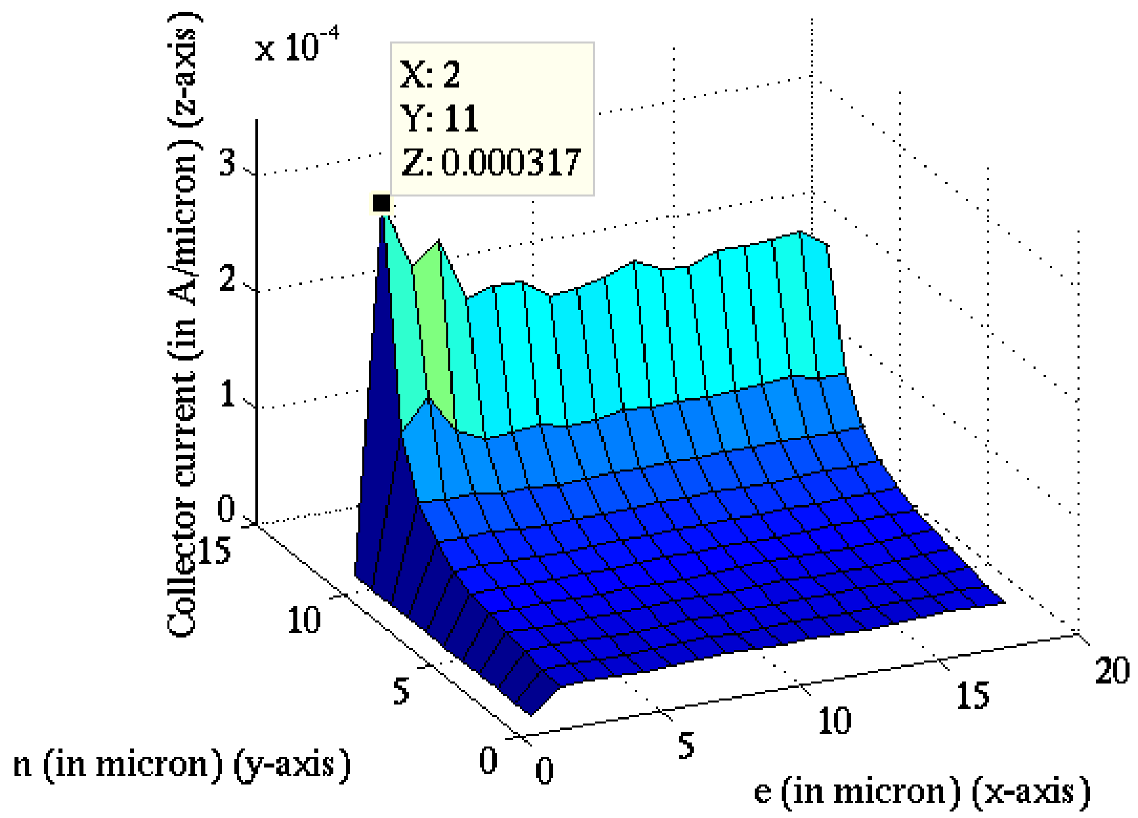

Figure 29: Collector current from 2-D simulation (g = 10 µm)

Figure 29 shows the collector current keeping g fixed at 10 µm. Figure 30 shows the current per unit area keeping g fixed at 10 µm.

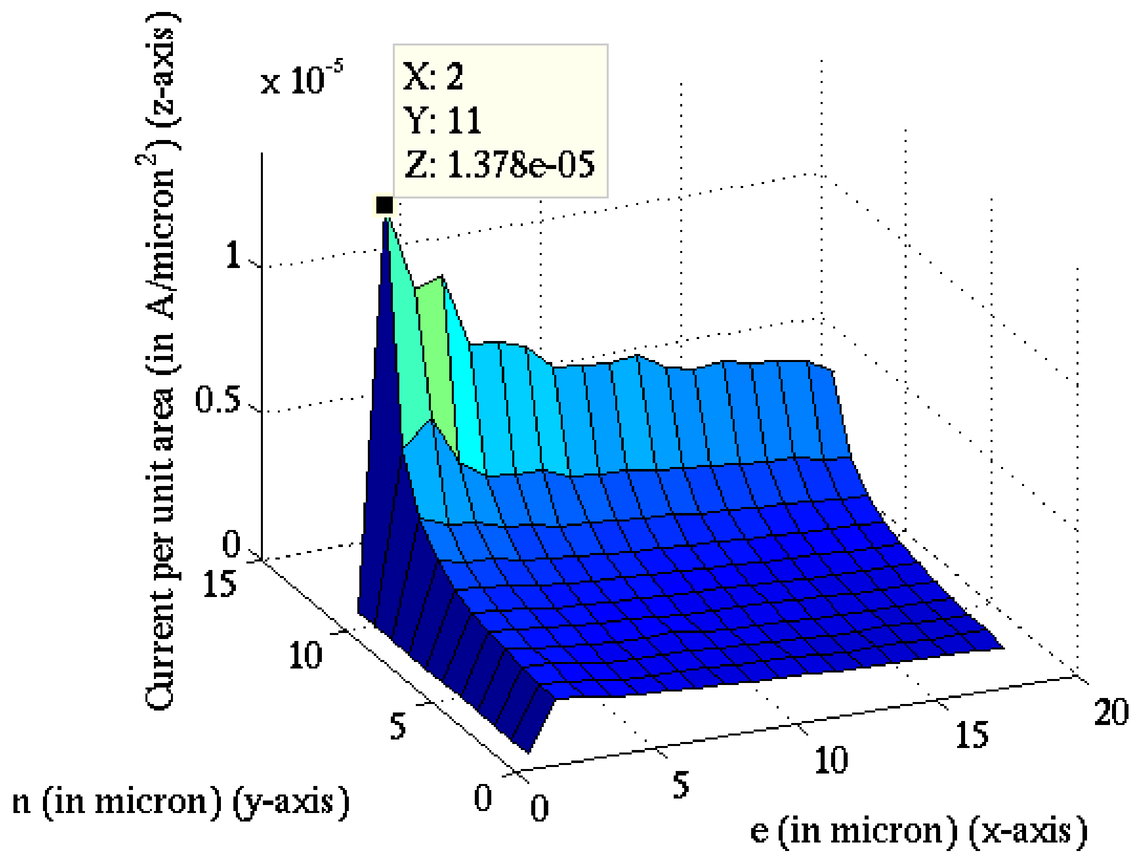

Figure 30: Current per unit area from 2-D simulation (g = 10 µm)

Verilog-A Model

Verilog-A was developed for analog and mixed-signal simulation. It was first released in 1996. Verilog-A models can be simulated using popular circuit simulators like Spectre and HSPICE.

The IGBT Hefner model developed by Dr. A.R. Hefner of National Institute of Standards and Technology (NIST) is more accurate. The device physics equations are described in a 1991 paper [9]. We have adapted the Hefner model and created the first Verilog-A model based on it. This model can be used for faster circuit design.

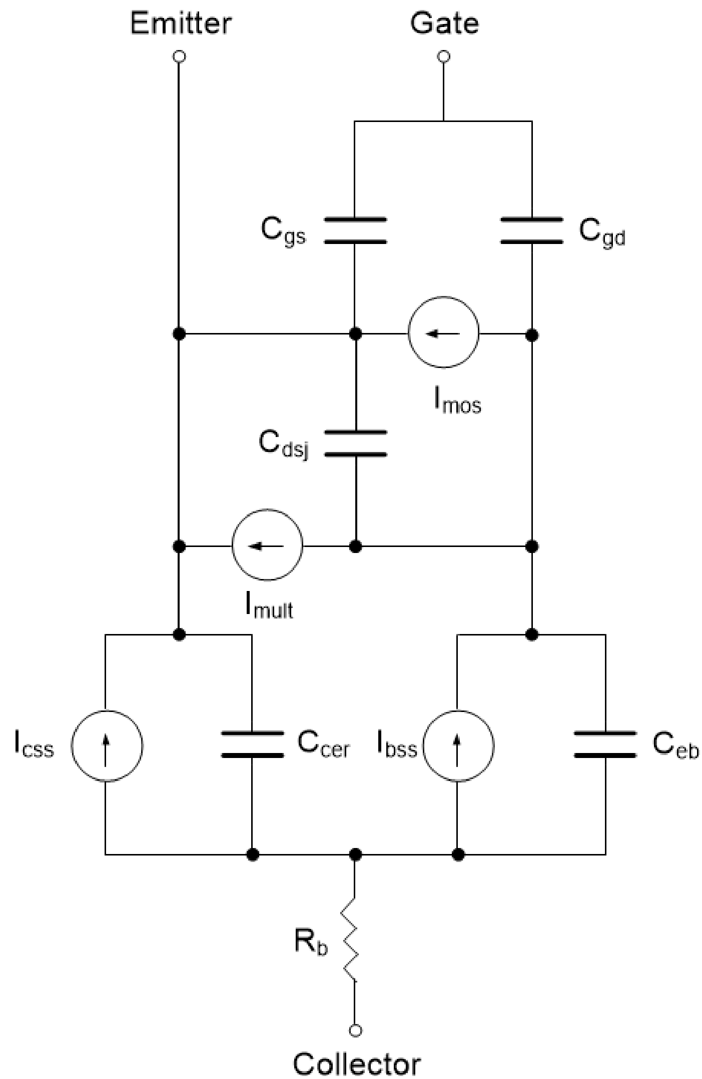

Figure 31: Analog circuit representation

Figure 31 from [4] shows the analog circuit representation of the IGBT model.

Transient simulation using Verilog-A model

We have used the Verilog-A model to perform transient simulations of the linear IGBT. We have also compared the simulation results of the Verilog-A model in Spectre with device simulation results in Sentaurus. Figure 32 shows the circuit used for the transient simulations. Table 5 shows the parameters of the pulse input at the gate.

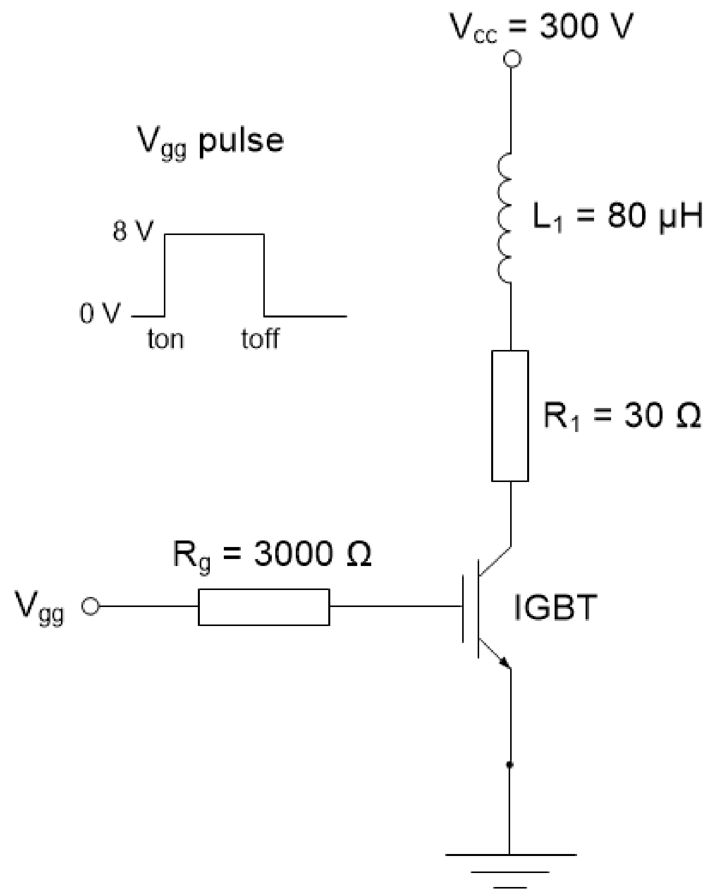

Figure 32: Circuit used for transient simulation

Table 5: Parameters of gate pulse input

Pulse parameter	Value
ton	1 µs
toff	30 µs
trise	500 ns
tfall	500 ns

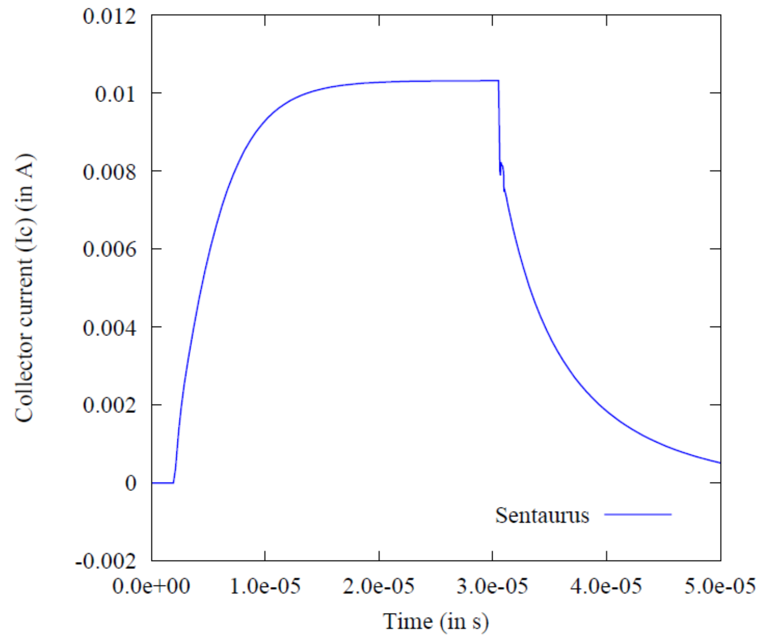

Figure 33: Collector current using Sentaurus

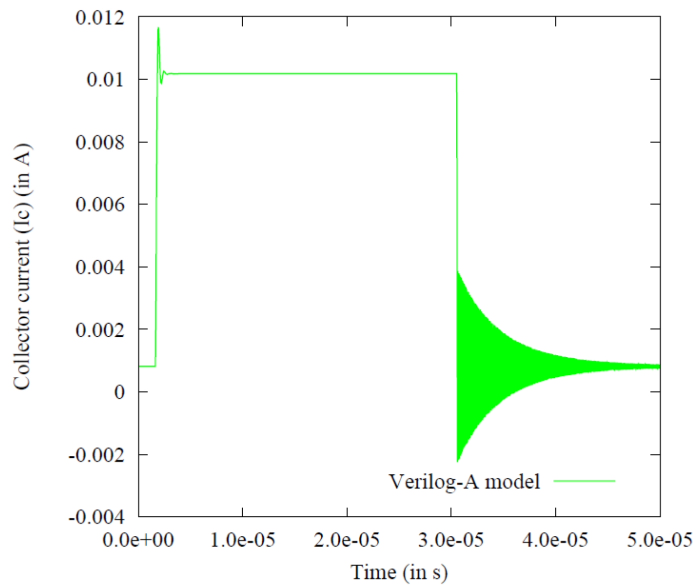

Figure 34: Collector current using Spectre

Figure 33 shows the collector current transient characteristics simulated using Sentaurus. Figure 34 shows the collector current transient characteristics simulated using the Verilog-A model in Spectre.

Figure 35 shows the gate current transient characteristics simulated using Sentaurus.

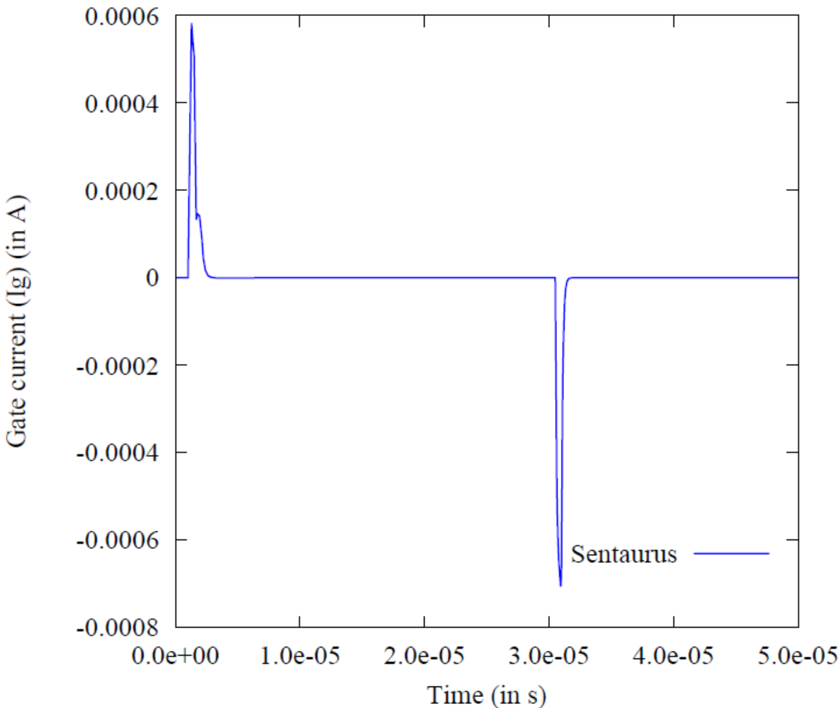

Figure 35: Gate current using Sentaurus

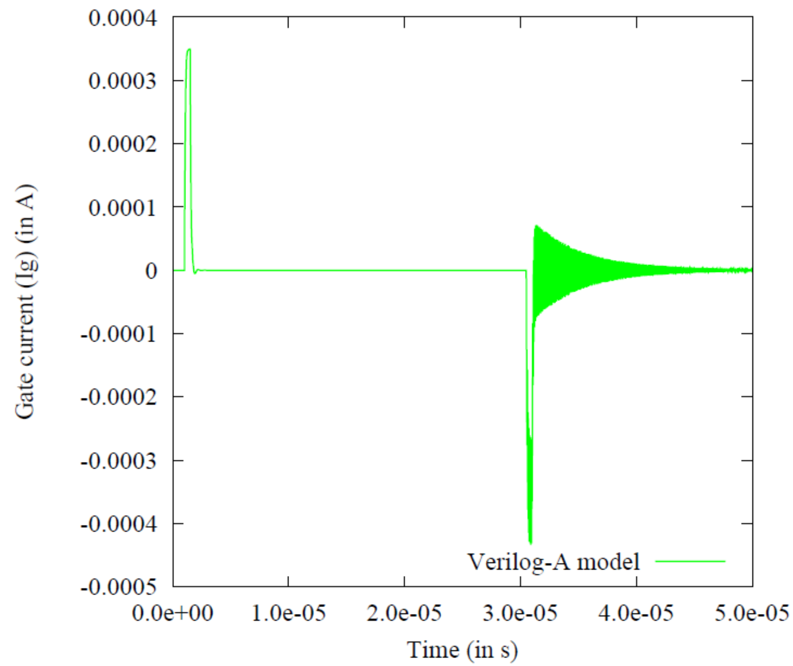

Figure 36: Gate current using Spectre

Figure 36 shows the gate current transient characteristics simulated using the Verilog-A model in Spectre.

Figure 37 shows the collector voltage transient characteristics simulated using Sentaurus. Figure 38 shows the collector voltage transient characteristics simulated using the Verilog-A model in Spectre.

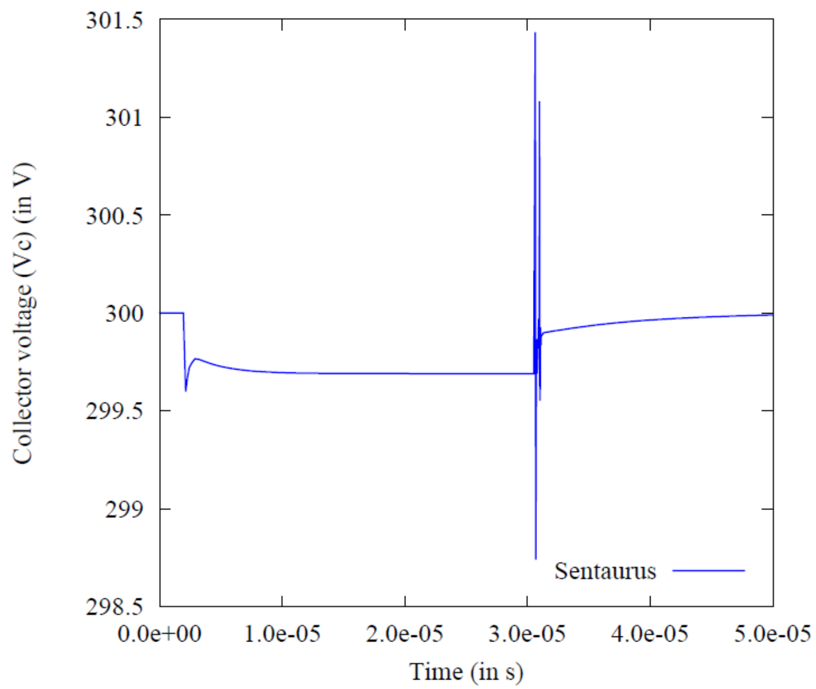

Figure 37: Collector voltage using Sentaurus

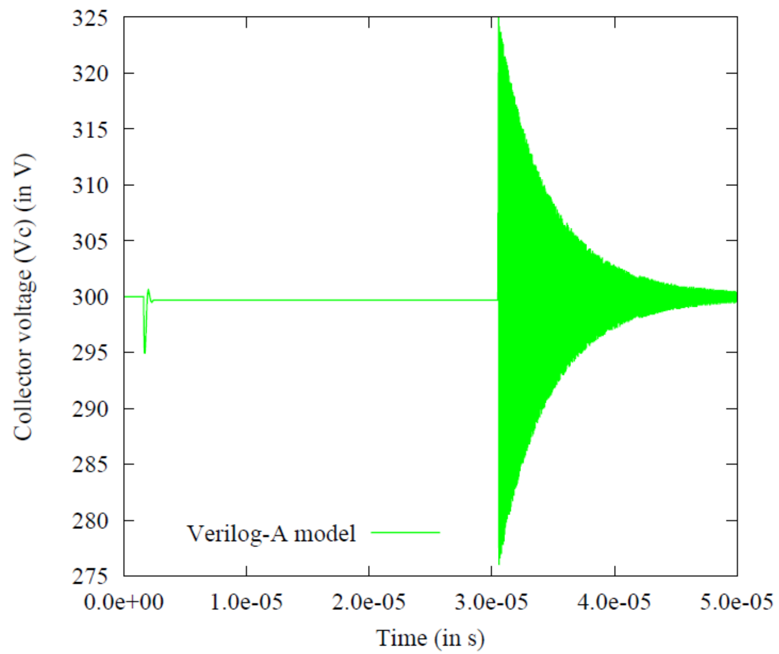

Figure 38: Collector voltage using Spectre

Figure 39 shows the gate voltage transient characteristics simulated using Sentaurus. Figure 40 shows the gate voltage transient characteristics simulated using the Verilog-A model in Spectre.

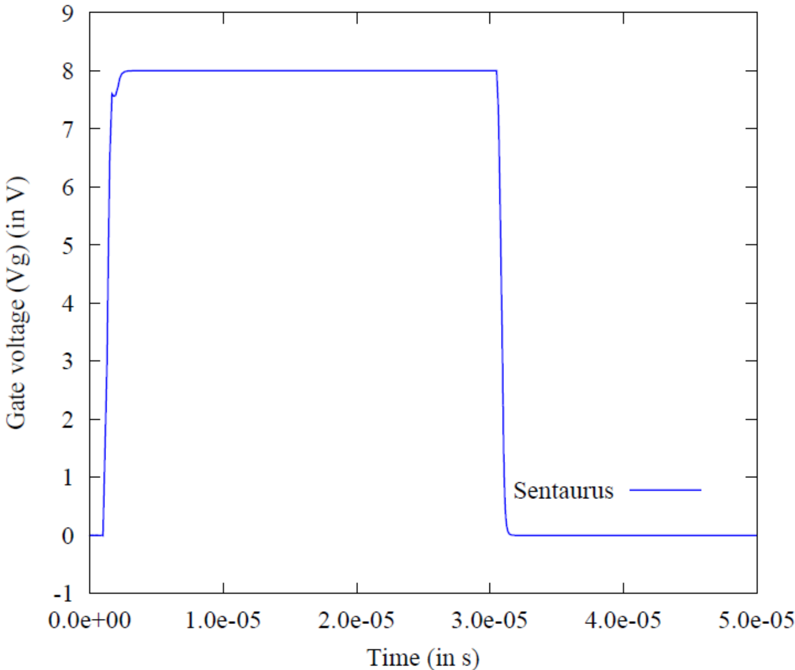

Figure 39: Gate voltage using Sentaurus

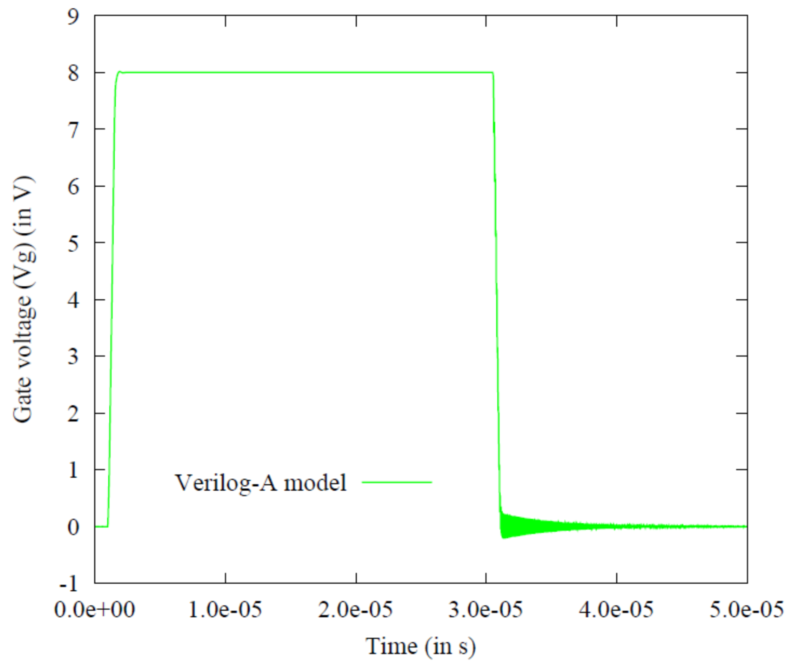

Figure 40: Gate voltage using Spectre

Buck converter transient simulation

Buck converter is a step-down DC-to-DC converter.

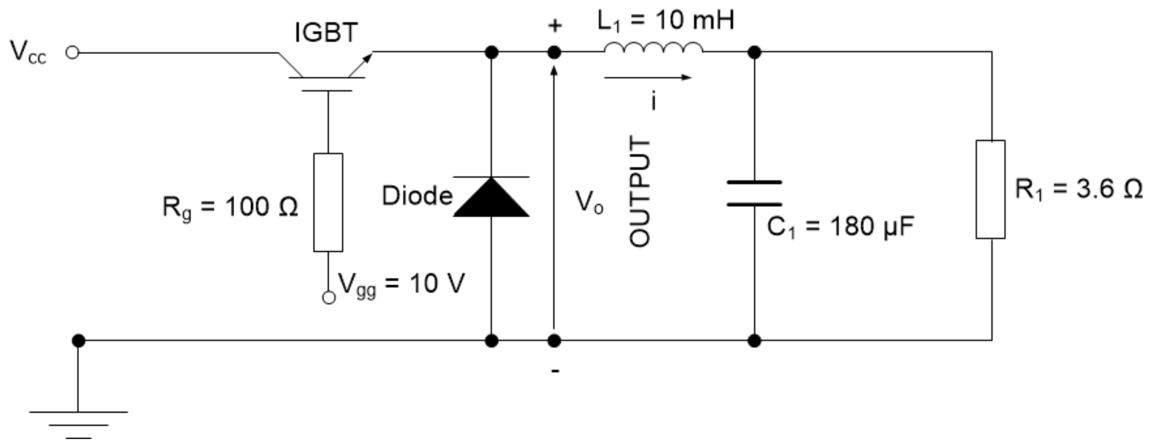

Figure 41: Buck converter circuit

Figure 41 shows the circuit of a Buck converter.

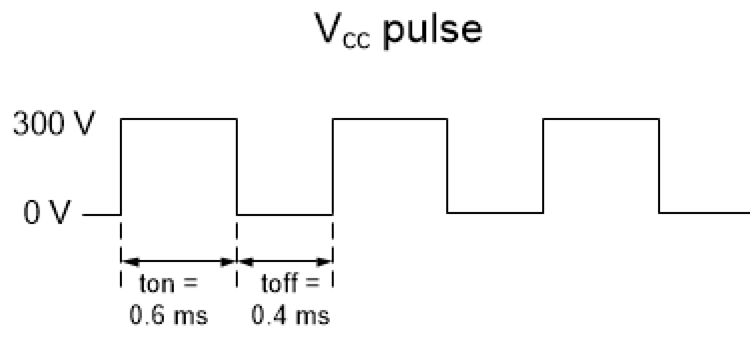

Figure 42: Buck converter input pulse

Figure 42 shows the input pulse applied to the Buck converter. Figure 43 shows the transient characteristics of the Buck converter simulated using Spectre.

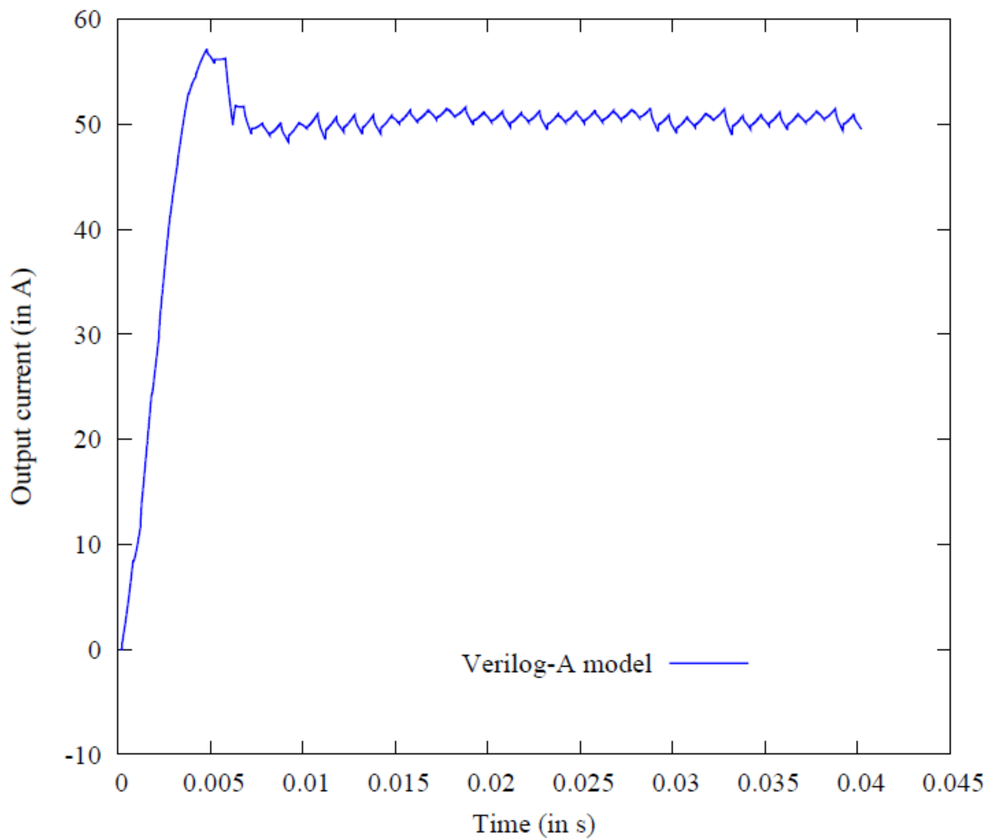

Figure 43: Buck converter transient characteristics

CHAPTER IV

CONCLUSION

We optimized the dimensions, layout and shape of IGBT using a step-by-step approach. The efficient hexagonal IGBT array was proposed. The performance gain (current per unit area) of the hexagonal array is 6 % over that of a square array and asymptotically approaches 80 % over that of a rectangle array. Techniques to reduce design time were proposed. 2-D device simulation can be used to optimize dimensions and layout of IGBT. Using 2-D simulation, we can achieve 12x improvement in runtime. We created the first accurate Verilog-A model based on the Hefner device equations. Verilog-A model can be used for faster circuit design. This has been proved using a simple test circuit involving an IGBT and an R-L load. Sentaurus takes 10 hours to simulate the transient characteristics, while Spectre takes 3 seconds to simulate the Verilog-A model. We have also simulated the transient characteristics of the Buck converter in Spectre using the Verilog-A model of the IGBT.

REFERENCES

[1] B. J. Baliga, *Fundamentals of power semiconductor devices*. Berlin, Germany: Springer, 2008.

[2] V. K. Khanna, *The insulated gate bipolar transistor : IGBT theory and design*. Piscataway, NJ Hoboken, NJ: IEEE Press ; Wiley-Interscience, 2003.

[3] B. J. Baliga, H. R. Chang, T. P. Chow, and S. Al-Marayati, "New cell designs for improved IGBT safe-operating-area," in *International Electron Devices Meeting*, San Francisco, CA, 1988, pp. 809-812.

[4] G. T. Oziemkiewicz, "Implementation and development of the NIST IGBT model in a SPICE- based commercial circuit simulator," Thesis (Engr.), University of Florida, Gainesville, FL, 1995.

[5] N. Jankovic, Z. Zhongfu, S. Batcup, and P. Igic, "An Advance Physics-Based Sub-Circuit Model of IGBT," in *International Symposium on Industrial Electronics*, Montreal, Que., 2006, pp. 447-452 vol. 1.

[6] M. Cotorogea, "Physics-Based SPICE-Model for IGBTs With Transparent Emitter," *IEEE Transactions on Power Electronics,* vol. 24, pp. 2821-2832, 2009.

[7] T. Ibrahim, B. Allard, H. Morel, and S. Mrad, "VHDL-AMS model of IGBT for electro-thermal simulation," in *European Conference on Power Electronics and Applications*, Aalborg, Denmark, 2007, pp. 1-10.

[8] P. O. Lauritzen, G. K. Andersen, and M. Helsper, "A basic IGBT model with easy parameter extraction," in *Power Electronics Specialists Conference*, Vancouver, BC, 2001, pp. 2160-2165 vol. 4.

[9] A. R. Hefner and D. M. Diebolt, "An experimentally verified IGBT model implemented in the Saber circuit simulator," *IEEE Transactions on Power Electronics,* vol. 9, pp. 532-542, 1994.