IMPEDANCE SPECTROSCOPY FRONT-END SUITABLE FOR BIOMEDICAL CELL IMPEDANCE MEASUREMENT

A Thesis

by

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Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

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August 2013

Major Subject: Electrical Engineering

ABSTRACT

Impedance spectroscopy (IS) is an important technique for monitoring and detection of biomaterials. In order to enable point-of-care systems, low-cost IS systems capable of rapidly measuring a wide range of biomaterials are required. This thesis presents two IS systems, one in Printed Circuit Board level and the other in Integrated Circuit level.

The board level system is built for preliminary experimental data collection; it is capable of measuring impedance from 1KHz to 100KHz with 200mV signal injection into cell sample. Experimental results show that magnitude and phase error are less than 6.6% and 2.2%, respectively.

An IC level IS front-end is also proposed which utilizes a time-to-digital converter (TDC) and a peak detector circuit (PDC) for quick measurement of both impedance phase and magnitude, respectively. Designed in a 0.18μm CMOS process, the front-end is capable of performing impedance measurements in 6μs at frequencies ranging from 100Hz-10MHz and with a 100Ω-1MΩ dynamic range. Simulation results with cell impedance models show that the system achieves <2.5% magnitude and <2.2^{o} phase error. The front-end consumes 28mW total power and occupies 0.4mm^{2} area.

ACKNOWLEDGEMENTS

I would like to thank my committee chair, Dr. Palermo, and my committee member, Dr. Kameoka, for their guidance and support throughout the course of this research.

Thanks also go to my friends and colleagues and the department faculty and staff for making my time at Texas A&M University a great experience. I would like specially say thanks to William Torke and Sungmin Hong for their help in my thesis work.

Finally, thanks to my mother and father for their encouragement and great support during my graduation study.

NOMENCLATURE

IS	Impedance Spectroscopy
PCB	Printed Circuit Board
TDC	Time to Digital Converter
ADC	Analog to Digital Converter
PDC	Peak Detection Circuit
MCU	Micro Controller Unit
DC	Direct Current
AC	Alternating Current
SNR	Signal to Noise Ratio
IC	Integrated Circuit
TIA	Trans-Impedance Amplifier
LPF	Low Pass Filter

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I INTRODUCTION

Electrical impedance is the measure of the opposition that a material presents when placed under an alternating electrical field. It is defined as the complex ratio of the voltage across the material to the current flowing through. Impedance possesses both magnitude and phase information.

Impedance Spectroscopy (IS) measures the impedance of a material over a frequency range. An impedance spectrum can be generated and subsequent analysis of the spectrum yield useful information about the physicochemical properties of the material. IS system consists of two parts: 1) Sensor/electrodes: IS systems inject small AC signal into a sample/material with known geometry through two or more electrodes as shown in Figure 1. 2) Impedance analyzer: the AC signal is provided and swept in frequency by an impedance analyzer; the complex voltage and current upon electrodes is then extracted to generate impedance spectrum.

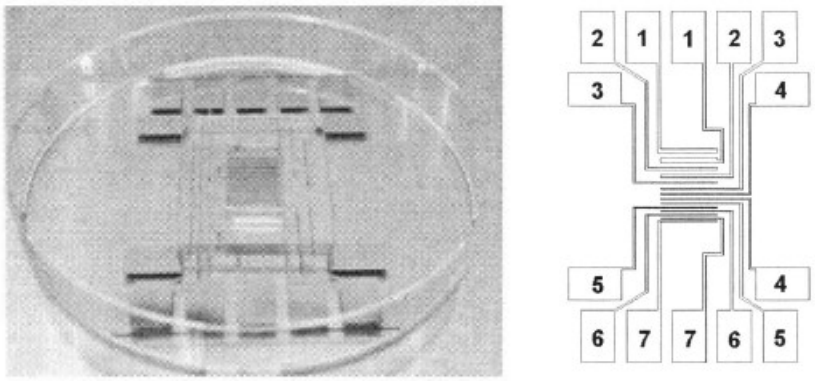

Figure 1. Electrodes used in impedance spectrocopy[1]

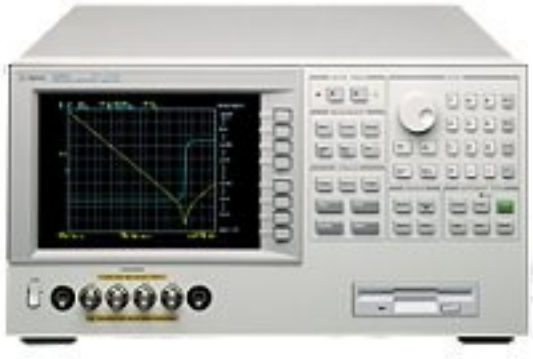

Figure 2. Commercial impedance analyzer Agilent 4294A[2]

Impedance spectroscopy has been extensively applied in electrochemistry and material science in recent years. In chemistry engineering, IS provides a non-invasive technique for investigation of complex process like the monitoring of chemical reactions and changes of composition and shapes. Since IS deals directly with complex quantities, it is also applied to measure dielectric response and conductivity of material [3].

In biomedical engineering, IS serves as a label free method to study the property of tissues [4], cells [5] and DNA [6]. Most of these studies focus on the fabrication of biosensor and use commercial impedance analyzer (shown in Figure 2) to obtain impedance spectrum. To reduce the impact caused by long connecting trace/cable and increase portability, some papers [7] directly builds the biosensor array on the top of a chip or integrate biosensor and analyzing circuit together on one board, an example is shown in Figure 3(a). The analyzing circuit they used together with some general-purpose impedance analyzing circuit [8][9] concentrate on improves sensitivity/dynamic

range and frequency range of system. However, in some applications, like flowing cytometry system [5] where cells are forced to flow through an aperture/channel for detecting shown in Figure 3(b), real-time impedance monitoring is needed which demands a fast measurement time of analyzing circuit. And this demand is not addressed by most of the studies.

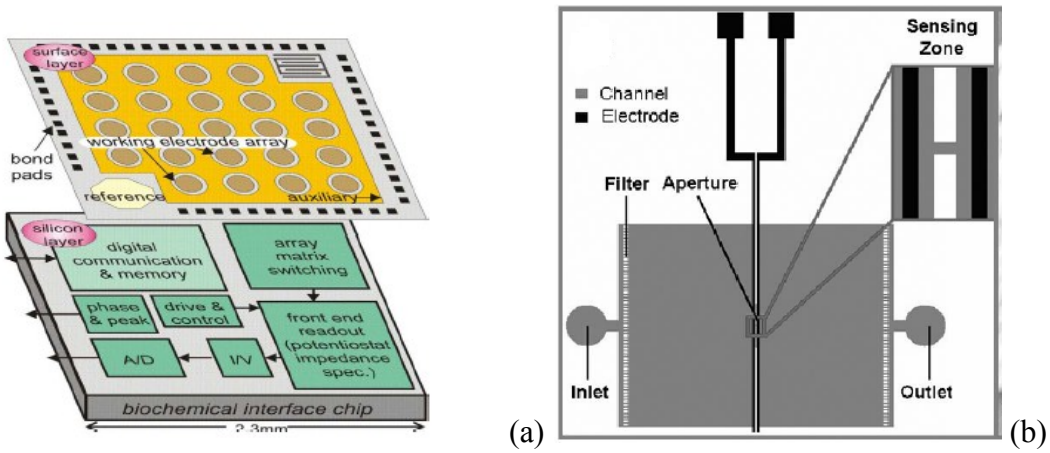

Figure 3. (a)Biosensor array integrated on IC chip[7] (b) flowing cytometry system[5]

In this work, the main focus is on building a general-purpose analyzing circuit suitable for bio-application that can extract the complex voltage/current upon material-electrodes and yield impedance spectrum. Specially, we report four parameters that biomedical application usually cares, namely, 1) AC injection amplitude 2) Measuring frequency range 3) Measurement time 4) Input dynamic range.

AC injection amplitude is kept as minimum as possible in IS system to limit its effect on sample material. Measuring frequency range, on the other hand, is chosen based on different applications typically (typically 10Hz-50MHz for bio-application).

Measurement time is a parameter that lots of studies have been ignoring and we try to optimize it in our work to enable real-time impedance monitoring. Input dynamic range is another parameter that we always want to increase in order to provide more measurement possibilities.

Two impedance measuring systems are presented in this work; the first one is implemented on board level with discrete parts and used to collect preliminary data. The second proposed system is on Integrated Circuit (IC) level and it explores a non-conventional structure to largely reduce the measuring time requirement, simulation results will be shown to demonstrate its functionality.

The following chapters will be divided into two parts; Section II will talk about the board level system and its experimental results. And Section III focuses on the proposed IC level system and its post-layout simulation result. Finally, Chapter IV will conclude all the work.

II BOARD LEVEL IMPEDANCE SPECTROSCOPY SYSTEM

System Overview

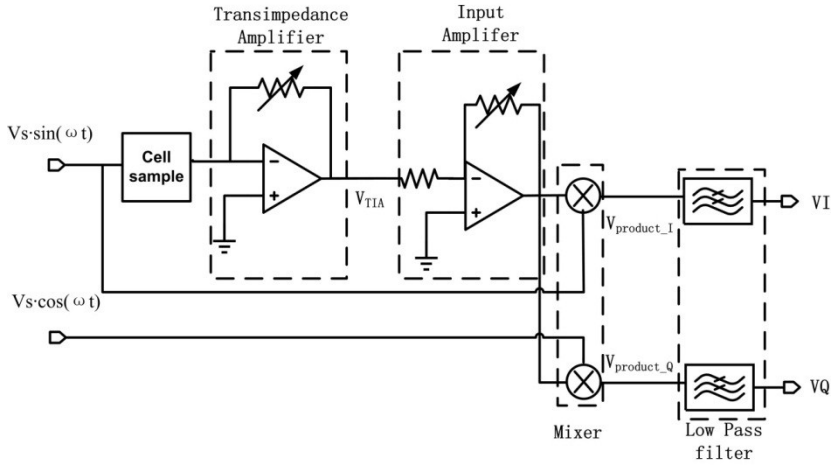

Figure 4. Board level impedance spectrocopy system overview

The board level impedance spectroscopy system is built as an initial attempt to approach the research topic due to its low cost and easiness for implementation. We use this board level IS system to collect preliminary experimental data and acquire further understanding towards IS system. The board level system uses a conventional lock-in amplifier based structure (shown in Figure 4). A signal generator is in charge of producing two sinusoidal waveforms with 90 degree phase difference. The sine waveform will serve as a stimulus signal which is applied across the sample cells via electrodes; the current following out of cells which contains impedance information at specified frequency is converted to voltage through a Trans-Impedance Amplifier (TIA). Since TIA is configured using an opamp with negative feedback resistor, its input can be

viewed as virtual ground (0 Volts). Therefore, all the voltage supplied by sine waveform falls across cell samples.

If we denote the output of TIA as V_{TIA} and the stimulus signal as $Vs \cdot \sin(\omega t)$, then following equation can be obtained:

$$V_{TIA} = -\frac{R_{TIA}}{|Z_{sample}|} V_s \cdot \sin(\omega t + \varphi)$$

Where R_{TIA} represents the feedback resistor of TIA; $|Z_{sample}|$ and φ represents the magnitude and phase of cell sample impedance respectively. V_{TIA} will then go through a gain stage which brings its magnitude level to several hundred millivolts. Then the output of gain stage will be demodulated with the sine and cosine waveform from signal generator. The product the multiplication will be:

$$V_{product\_I} = \frac{V_s^2 * K * |Z_{TIA}|}{2 * |Z_{sample}|}[\cos(\varphi) - \cos(2\omega t + \varphi)]$$

$$V_{product\_Q} = \frac{V_s^2 * K * |Z_{TIA}|}{2 * |Z_{sample}|}[\sin(\varphi) + \sin(2\omega t + \varphi)]$$

In the above equation, *K* denotes the voltage gain of the gain stage. After removing the high frequency term by passing through two low pass filters (LPF), we can have:

$$V_I = \frac{V_s^2 * K * |Z_{TIA}|}{2 * |Z_{sample}|}\cos(\varphi) \qquad V_Q = \frac{V_s^2 * K * |Z_{TIA}|}{2 * |Z_{sample}|}\sin(\varphi)$$

Then the magnitude and phase of Z_{sample} can be calculated as:

$$|Z_{sample}| = \frac{K * V_s^2 * |Z_{TIA}|}{2 * \sqrt{VI^2 + VQ^2}} \qquad \varphi = tan^{-1}(\frac{V_Q}{V_I})$$

Calibration

TIA is implemented using operational amplifier with feedback potentiometer in order to address large variation of sample impedance (ranging from KΩ to MΩ). Another potentiometer is adopted to form variable gain stage. This variable gain stage helps to adjust the magnitude of V_{TIA} such that it has an acceptable SNR and still falls within input range of multipliers.

Due to the use of potentiometer, Z_{TIA} and K become unknown and may vary with frequency which implies that impedance of sample cells cannot be calculated directly. However, by replacing the sample cells with standard resistor while keeping configuration of TIA and gain stage unchanged, we can build a set of equations which remove the requirement of Z_{TIA} and K to attain impedance of cell samples. If we denote $VI_{standard}$ and $VQ_{standard}$ as the outputs after replacing with a standard resistor R, the phase and magnitude of cell sample can be solved as following:

$$\left|Z_{sample}\right| = R * \frac{\sqrt{VI_{standard}^2 + VQ_{standard}^2}}{\sqrt{VI_{sample}^2 + VQ_{sample}^2}}$$

$$\varphi = tan^{-1}\left(\frac{VQ_{standard}}{VI_{standard}}\right) - tan^{-1}(\frac{VQ_{sample}}{VI_{sample}})$$

The standard resistor should be chosen such that it is at the same order compared to magnitude of cell impedance. In that way, we can keep the configuration of TIA and gain stage unchanged while having adequate TIA output during calibration.

Implementation Details

Board overview

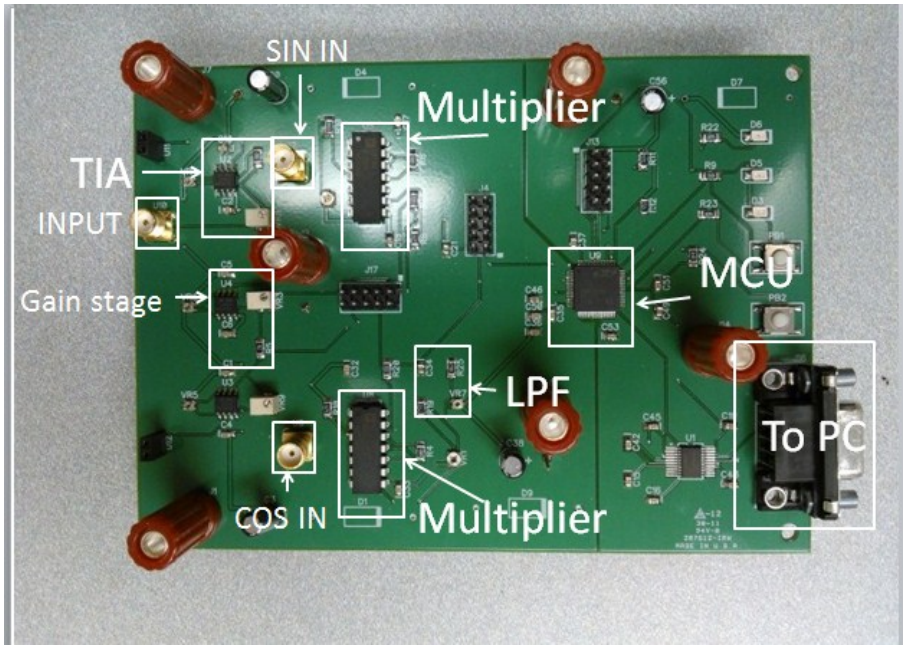

Figure 5. Board level impedance spectrocopy system implementation overview

Figure 5 shows the implemented board for impedance measurement. Aside from the elements that mentioned in section 1, the board also contains a Micro Controller Unit (MCU) which is responsible for converting V_I and V_Q into digital signal and communicating with PC through an RS232 port. The board uses two sets of power supplies, all the analog parts including opamps, multipliers are powered by +-15 Volts DC supply, and digital parts including MCU, RS232 interface chip are powered by normal 3.3V/0 DC supply.

Signal generator

Stimulus signal into the cell sample together with reference signals into lock-in amplifiers are produced by Tektronix AFG320 two-channel waveform generator. The sine reference signal and stimulus signal share one channel and cosine reference signal occupies another one. Stimulus signal will be buffered when impedance of cell samples is comparable with source impedance (50Ω) of AFG320.

Potentiometer

The potentiometer utilized by TIA limits up to 2MΩ. And the gain stage uses a feedback 50KΩ potentiometer together with a 1KΩ resistor to achieve variable gain up to 50. All the potentiometers used are single turn trimmer from Murata.

Opamp

All the operational amplifiers used are Texas Instrument OPA228. Key parameters of OPA228 are listed in the Table 1.

Parameter	Value
Noise (Input refer)	$3nV/\sqrt{Hz}$
Power supply	+-15V
Bandwidth	33MHz
Open-Loop Gain	160dB
Settling time	5us

Table.1 Key specification of OPA228

Multiplier

Two Analog Device AD734s are chosen to function as the multipliers with a unity conversion gain configuration. Table 2 shows the key specification of it. Another reason for choosing AD734 is its ability to shift output DC level based on a reference voltage. This is necessary if we want to exploit the full input range of ADC as explained later in 3.7 MCU section.

Parameter	Value
Typical Static Error	0.1 %
Power supply	+-15V
Bandwidth	10MHz
THD (X=7V,Y=10V)	-55dBc
Noise (Output)	$1uV/\sqrt{Hz}$

Table.2 Key specification of AD734

Low pass filter (LPF)

DC outputs of multipliers are extracted using RC low pass filter. The value of resistor is 10KΩ and capacitor is 1uF. Together they will provide a cutoff frequency around 16 Hz.

MCU

The main task for MCU is to convert the voltage level of V_I and V_Q into digital signal and send them to PC. Taking this into consideration, a Silicon Lab C8051F061 chip is

selected as MCU, it provide two 16-bits Analog to Digital Conversion channels with 1M sample/s speed.

The input range of ADC is from 0-3.3 volts, it is necessary to keep V_I and V_Q fall into this range. Therefore, a DC offset need to be added to the output of multipliers so that V_I and V_Q can always be positive. This DC offset is chosen to be 1.65 Volt so that the full input range can be used. Therefore, a 1.65 Volt constant voltage generated by a resistor ladder is supplied to the offset port of multiplier and changes the operating point of outputs. The sampling and communicating code for MCU can be found in Appendix.

RS232 port

In order to send sampled data of V_I and V_Q to PC, a SP3223ECY-L chip together with RS232 port are employed as an interface between MCU and PC, a Universal Asynchronous Receiver/Transmitter (UART) link is built upon this interface.

Experiment Results

System accuracy test

An impedance model is used to test accuracy of impedance spectroscopy system. The model consists of a 5KΩ resistor in parallel with a 1nF capacitor. Tests are conducted from 1 KHz to 100KHz. Phase and magnitude are recorded and compared with ideal results. Table 3 shows the comparison result.

Frequency(Hz)	$Z_{Measure}(\Omega)$	$Z_{ideal}(\Omega)$	Error(%)	$\Phi_{Measure}(^{o})$	$\Phi_{ideal}(^{o})$	Error (%)
1 K	5058.48	5105.47	0.92	-1.49	-1.77	-0.28
3 K	5023.46	5085.4	1.22	-4.85	-5.29	-0.44
5 K	4987.75	5045.95	1.15	-8.1	-8.76	-0.66
7 K	4936.59	4988.47	1.04	-11.3	-12.17	-0.87
10 K	4821.71	4872.57	1.04	-15.97	-17.11	-2.14
50 K	2852.77	2741.32	4.07	-54.14	-55.8	-1.66
70 K	2227.28	2113.57	5.38	-62.18	-63.11	-0.93
100 K	1651.9	1550.02	6.57	-68.98	-68.84	0.14

Table.3 System accuracy test result

As the frequency increases, the effect of parasitic associated with board trace and intersection become more significant which leads to a larger magnitude error. The maximum magnitude and phase error are less than 6.6 % and 3% respectively through measuring frequency range.

Measurement on different cells

The system is then applied to distinguish different cells, namely MDA231, MCF7, red blood cell and white blood cell. All the cell solutions have the same concentration of 10^6/mL. Figure 6 shows the measurement result.

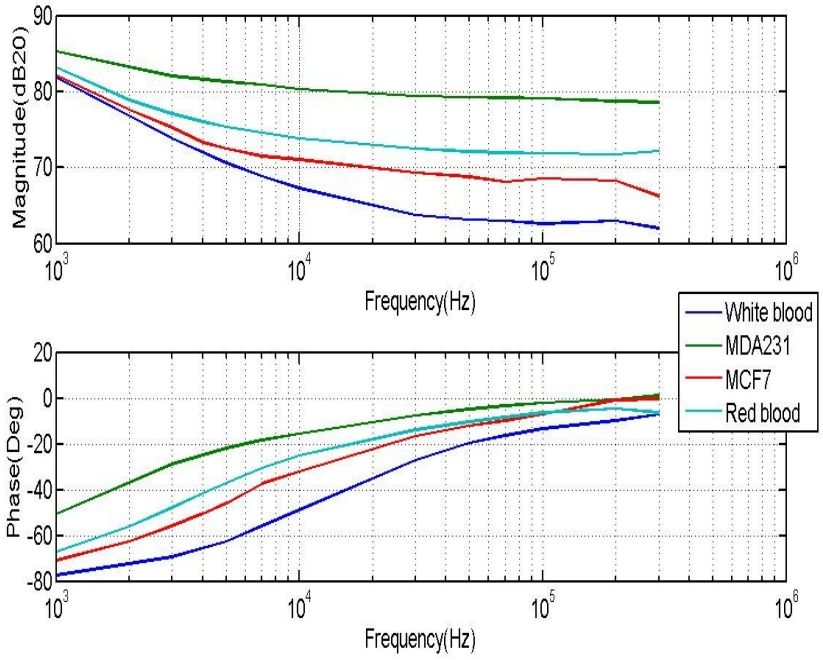

Figure 6. Measurement results on different cell solution

With frequency properly chosen, the minimum magnitude and phase difference between cell samples can be 4dB and 10^o, respectively. As the accuracy error limits up to 0.5 dB (6%) and 2^o, the difference is large enough to differentiate cell samples.

Measurement on cells with different concentrations

As the concentration of cell solution changes, it exhibits different impedance. MDA231 samples with concentration distributed exponentially from 10^5/mL to $6.7*10^6$/mL are measured. Results are shown in Figure 7.

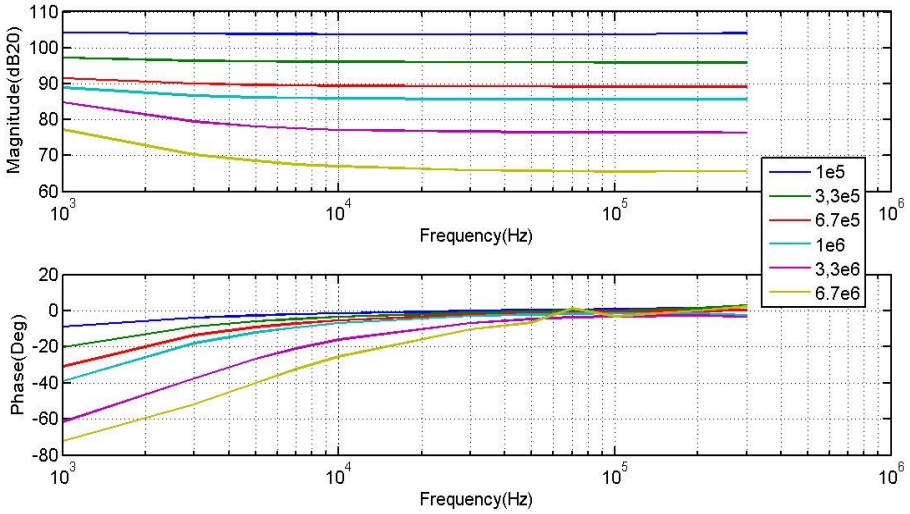

Figure 7. Impedance of MDA231 cell solutions under different concentration

With frequency properly chosen, the minimum magnitude and phase difference between cell samples can be 4dB and 10^o, respectively. Therefore, this board level system can be utilized to distinguish cell solutions with different concentrations.

Experiments Summary and System Evaluation

Experiments summary

Some observations can be drawn from the experimental results shown above (1) the magnitude of cell solution impedance ranges from KΩ to MΩ. We need large tuning range for TIA and gain stage to accommodate this variation. (2) As frequency goes high, capacitive component in cell solution contributes more to the overall impedance, and leads to a drop in magnitude.

System evaluation

The board level impedance spectroscopy system work fine with 200 mV or larger stimulus signal and a frequency range up to 500 KHz. However, an IC level system is needed if we want to achieve better performance.

When we try to use this system to measure varying impedance, like a flowing cell solution in a channel which exhibits different impedance when cells pass by electrode, a main drawback of the system appears. Due to the presence of low pass filter, fast varying impedance cannot be measured. A modification on system structure needs to be made in order to solve this issue.

III IC LEVEL IMPEDANCE SPECTROSCOPY SYSTEM

Motivation

An IC level IS system is necessary to improve the measurement frequency range. Thanks to the reduction of parasitic, measurement accuracy is usually improved. Also, a biosensor array can be implemented on the top of chip to enable large scale impedance measurement; this is another advantage of IC system.

Literature Review

Cell impedance measurement survey

Reference No.	Cell types	Frequency	Stimulus Magnitude
5	Human blood cell	100-3MHz	0.1V
10	Fibroblast cell	100-1Mhz	50mV
11	Human cervical cell	1K-100K Hz	0.1-1.5V
12	Cancer cell	1K-100K	0.2V
13	Bovine chromaffin	100-5MHz	N/A
14	Cancer cell	100-10MHz	10mV
15	Stem cell	100-10MHz	N/A
16	Endothelial cell	100-100KHz	10mV
17	Blood cell	100K-20Mhz	0.35V
18	Embroyonic cell	500k-1.5Mhz	N/A

Table.4 Survey on cell impedance measurement

In order to determine the specification of the IC level impedance spectroscopy system, we conduct a survey to find the typical frequency range and stimulus signal magnitude level that cell impedance measurement are usually done. Table 4 shows the survey results taken from ref [5] and ref[10]~[18]. Based on the survey results, the frequency range specification is chosen to be 100Hz - 10MHz which covers most of the cell measurements done above. And the minimum stimulus signal magnitude is set to 10mV.

Impedance measurement method review

There are two primary categories of Impedance Spectroscopy systems: Fast Fourier Transform (FFT) based IS and Frequency Response Analyzer (FRA) based IS.

FFT based IS

For a FFT based IS, we need to stimulus the unknown impedance with a waveform that contains the frequencies we are interested in. An ideal white noise will be a good choice. The extracted current will be sampled and digitized to perform FFT in order to calculate the impedance at different frequency.

The main advantage is that we can get impedance information of different frequencies at the same time and thus can be used to measure fast varying impedance easily. But it requires intensive hardware to sample and save data and computing power for data processing which makes it less attractive considering cost, portability.

FRA based IS

Most systems belong to FRA based IS in which one frequency impedance is obtained at one time. A stimulus signal at one frequency is sent into the cell sample and impedance information at that frequency can be acquired accordingly. The most conventional way for doing this is the lock-in amplifier based IS as we used in the board level system.

Two main drawback of lock-in amplifier based IS are (1) it requires quadrature signal generator which is not easy to implement and may cause significant error when the phase difference is not exactly 90^{o}. (2) the low pass filters need to have small cutoff frequency in order to suppress high frequency terms, but this will make the system less suitable for measuring varying impedance when the impedance varying frequency is higher than cutoff frequency of low pass filters.

Some studies have been carried out to solve these two issues. In ref [8], a system without the requirement of quadrature signal generator is proposed as shown in Figure 8.

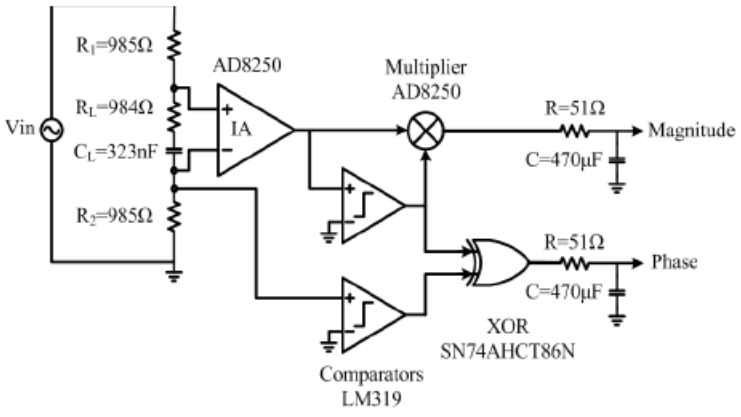

Figure 8. Proposed system by [8]

In this system, the stimulus signal and the current passing through cell sample are converted to square waveforms. These two square waves, one synchronous to the injected signal and one synchronous to the measured current are compared by a XOR gate to generate their phase difference in time domain. The output of XOR gate has different pulse widths depending on the phase shift caused by cell sample, and by extracting its DC level the phase information can be obtained.

As for the magnitude measurement, a multiplier is still applied, but with faster switching, noise can be reduced. However, as mentioned in the paper, offset canceling techniques need to be applied so that the DC level of multiplier's output is offset free.

Due to the use the RC low pass filter, the system above still needs a long settling time, this issue is addressed by ref [7]; and its main idea is shown in Figure 9.

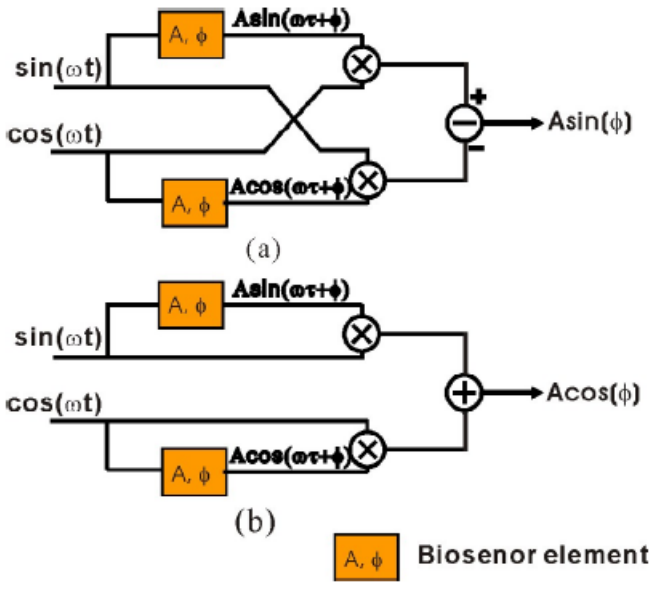

Figure 9. Fast DC extraction method proposed by [7]

In this paper, two identical cell samples are stimulated by signals in quadrature; their outputs will pass through two lock-in amplifier and be added together. In this way, the AC components of lock-in amplifier outputs can be canceled and thus faster response time will be achieved. The main drawback for this method is that it requires matching of cell samples/lock-in amplifiers which is hard to realize in IC system.

Proposed System Overview

Based on the analysis above, an IC level system is proposed. It removes the requirement of quadrature signal generator and the measurement can ideally be done in just slightly more than one cycle of the stimulus signal. Figure 10 shows the overview of proposed IC system.

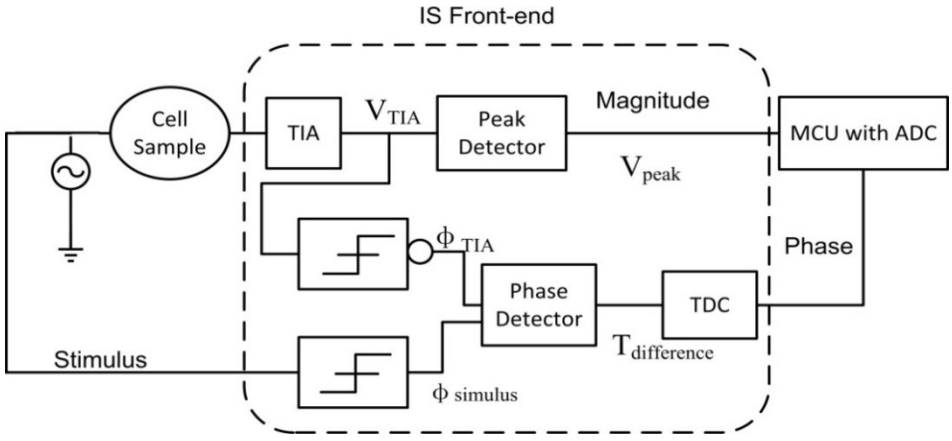

Figure 10. Proposed IC level IS Front-end

To understand how this system works, we denote the stimulus signal as $|Vs|\cdot\sin(\omega t)$

And the output of TIA is expressed as $V_{TIA} = -\frac{|Vs|*\sin(\omega t+\varphi)*|Z_{TIA}|}{|Z_{sample}|}$.

The peak detector circuit (PDC) will extract the amplitude of output of TIA, i.e.

$$V_{peak} = \frac{|Vs| \cdot |Z_{TIA}|}{|Z_{sample}|}$$

This can give us the magnitude of cell impedance as:

$$|Z_{sample}| = \frac{|Vs| * |Z_{TIA}|}{V_{peak}}$$

To calculate the phase shift φ , two comparators are employed to bring the output of TIA and the original stimulus signal to full square wave, i.e.

$$V_{comparator_1} = \mathrm{sgn}(V_{simulus}) \qquad V_{comparator_2} = \mathrm{sgn}(-V_{TIA})$$

Note, the V_{TIA} inversion is achieved by applying the TIA output into the negative input of the differential comparator. A phase detector will compare the rising edge of these two square waves and generate the time difference. Since these two square waves are synchronous with TIA output and stimulus signal, respectively. The time difference between their rising edges reflects the phase shift between TIA outputs and stimulus signal directly. Namely,

$$\varphi = \frac{T_{difference}}{T_{cycle}} * 2\pi$$

Where T_{cycle} represents the period of stimulus signal and $T_{difference}$ is the rising edge time difference. $T_{difference}$ is measured using a Time to Digital Converter (TDC) directly, and this conversion can be completed in one period cycle. In ref [9], LPF and ADC are

applied to extract and measure DC of the output of phase detector which is proportional to $T_{difference}$. However, this will restrict the system response time to the settling time of LPF.

To illustrate the working scheme of proposed IS. We plot the transient waveforms with a 40KHz stimulus signal in Figure 11.

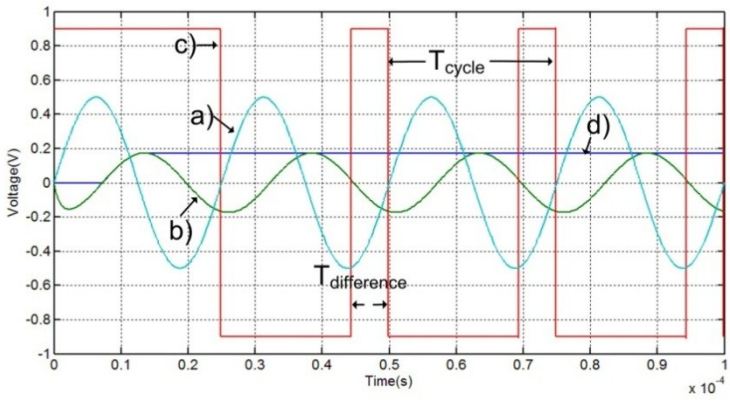

Figure 11. IS front-end operation: a) 40kHz stimulus signal (×50), b) TIA output, c) Phase detector output, d) PDC output .

Implementation Details

The proposed IS front-end is implemented using CMOS 180nm technology with +-0.9 V power supply. Each block will be discussed in following sections.

Trans-impedance amplifier

TIA overview

After stimulate the cell sample with AC signal at specified frequency, we need to collect the current flowing out of cell sample and convert it into voltage for further processing,

this conversion is carried out by a Trans-Impedance Amplifier. Figure 12 shows the overview of proposed TIA. Values of some parts are also labeled.

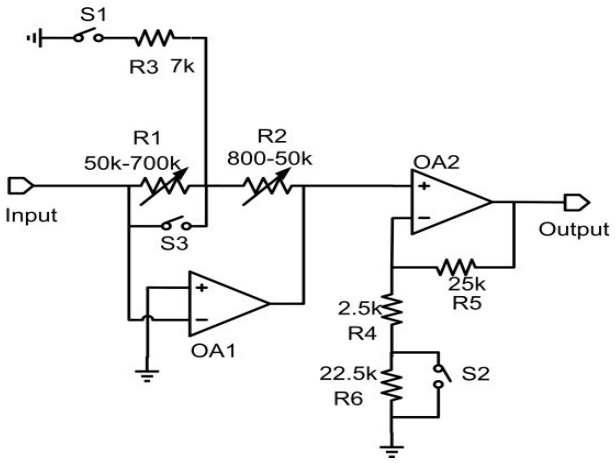

Figure 12. TIA overview

There are two stages in this TIA design. Each stage adopts an opamp. *OA1* is in charge of converting input current into voltage with the help of *R1, R2, R3*; *OA2* amplify this voltage with a constant gain K = 11 or 2.

If we apply a stimulus signal with amplitude V_s and denote the impedance magnitude under measurement as Z. The output of *OA1* can be calculated as:

$$V_{OA1\_S1\_ON} = Vs * \frac{-A1*(R1*R2+R2*R3+R1*R3)}{(R1*R2+Z*R3*A1+R1*R3+Z*R2+Z*R3+R2*R3)}$$

When *S1* is switch on

$$V_{TIA\_S1\_OFF} = Vs * \frac{-A1*(R1+R2)}{(Z*A1+R1+Z+R2)}$$

When *S1* is switch off

In the equation above, *A1* represents the open loop gain of *OA1*.

If we assume that A1 is large enough, these equations can be approximated as

$$V_{OA1\_S1\_ON} \approx Vs * \frac{-(R1*R2+R2*R3+R1*R3)}{Z*R3}$$

$$= -Vs * \left[\frac{(R1*R2)}{Z*R3} + \frac{(R1+R2)}{Z}\right]$$

$$V_{OA1\_S1\_OFF} \approx -Vs * \frac{(R1 + R2)}{Z}$$

If we compare these two equations, we can find that when *S1* is switched on, output of *OA1* will increase by $\frac{(R1*R2)}{Z*R3} * \frac{R4+R5}{R4}$, and thus larger gain can be achieved. In a conventional TIA design, the feedback resistor will directly determine trans-impedance, therefore a several MΩ resistor is needed to obtain same level trans-impedance, and this demands huge area for an on-chip solution.

Similarly, depending on the state of *S2*, the output of *OA2* can be approximated as:

$$V_{OA2\_S2\_ON} \approx -V_{OA1} * \frac{(R5+R4)}{R4} = 11 \cdot V_{OA1}$$

$$V_{OA2\_S2\_OFF} \approx -V_{OA1} * \frac{(R5 + R4 + R6)}{R4 + R6} = 2 \cdot V_{OA1}$$

Different TIA trans-impedance gain can then be achieved be tuning the value of *R1, R2* and switching *S1, S2, S3*.

OA1

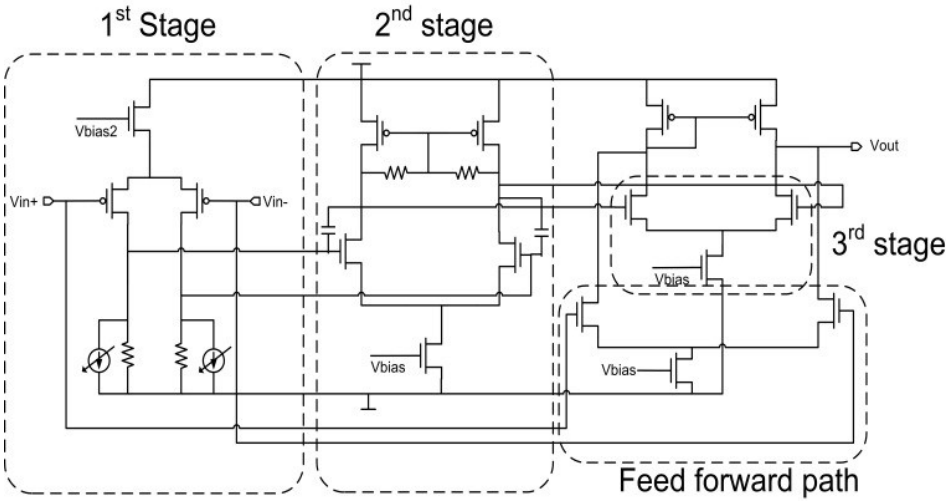

Figure 13. Schematic of OA1

Figure 13 shows the schematic of *OA1*, It consists of three gain stages and one feed-forward stage. In order to reduce input-referred flicker noise, the first stage adopts a PMOS input differential pair and passive resistor loads. The feed-forward stage provides a transmission zero in the signal path to improves phase margin. The second stage employs self-biasing technique for common-mode feedback. Table 5 shows performance.

Parameter	Value
Open loop gain	54.8dB
3dB bandwidth	7.39 MHz
Phase margin	65.36 Deg
Slew rate	800 V/us
Power consumption	10 mW

Table.5 Performance of OA1

When a stimulus signal is applied across the cell sample, it may be associated with a DC offset which is not easy to be detected/ measured. Also, the Pressure, supply Voltage, Temperature (PVT) variation and process mismatch will introduce offset into TIA. All these offset will be added and amplified, which causes a significant DC shift of the TIA output. This DC shift not only degrades the output swing of TIA which leads to a smaller impedance magnitude measuring range , it also causes asynchronies between the TIA output and its rectified waveform which introduces a phase measurement error. This offset, however, may not cause an error for magnitude measurement when a calibration technique is applied, this will be discussed later. In order to cancel this offset, we first note that all these offsets can be transferred into an equivalent DC voltage (V_{offset}) applied at the input of *OA1*. It causes unbalanced DC current through the first stage resistor loads of TIA. If we can subtract different currents from the loads and re-balance their overall DC current, the offset can be eliminated. And this is done by two digitally tunable current sources added in parallel with the first stage resistor load.

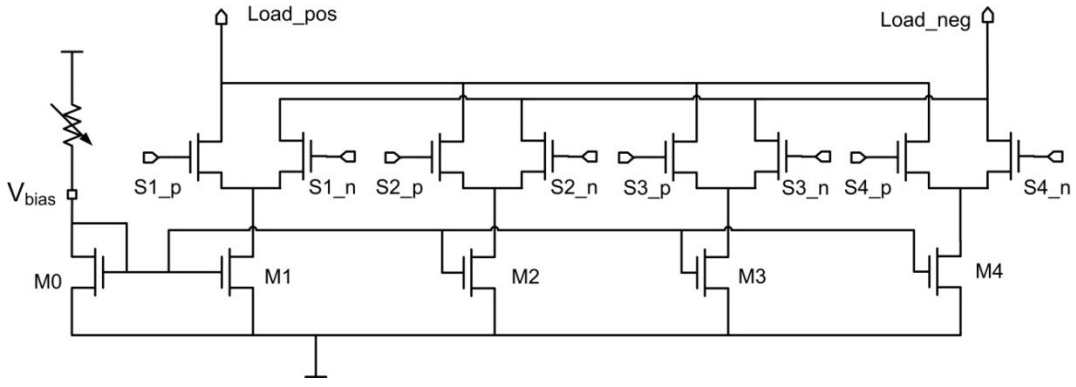

Figure 14. Digitally tunable offset cancellation circuit

The detail implementation of these two current sources is shown in Figure 14. $M_{1,2,3,4}$ acts as four binary weighted current source with

$$(\frac{W}{L})_0 : (\frac{W}{L})_1 : (\frac{W}{L})_2 : (\frac{W}{L})_3 : (\frac{W}{L})_4 = 1:1:2:4:8$$

And four pairs NMOS switches steer their current to different load branch or shut them off when they are not in use. The bias voltage of $M_{1,2,3,4}$ are controlled by an off-chip potentiometer. Therefore, the resolution and offset cancellation range are adjusted through the tuning of this potentiometer.

OA2

OA2 are intended to provide voltage gain K =2 or 10 depending on its feedback configuration. High output swing and large open loop gain need to be achieved to prevent signal distortion. A two stage opamp with PMOS self-cascode structure are used as shown in Figure 15. The Miller Compensation capacitor is connected to the internal node of PMOS self-cascode structure to remove the effect of right plane zero in a conventional two stage opamp. Performance summary are listed in Table 6.

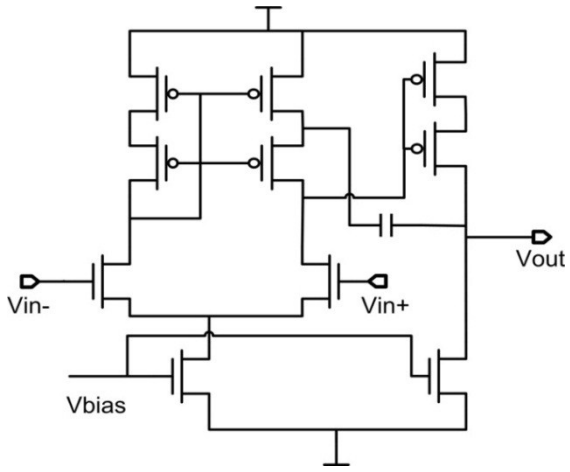

Figure 15. Schematic of OA2

Parameter	Value
Open loop gain	49 dB
3-dB bandwidth	3.04 MHz
Phase margin	69.22 Deg
Slew rate	800 V/us
Power consumption	4.6 mW

Table.6 Performance of OA2

Resistor array and trans-impedance range

The impedance magnitude of cell sample varies from 100Ω to 1MΩ according to the experimental result from the board level IS system. To accommodate this variation range while keeping the V_{TIA} essentially unchanged for further processing, the trans-impedance gain of TIA needs to be adjusted. During the measurement, trans-impedance gain of TIA is tuned at the first place so that the V_{TIA} is within 100mV to 400mV range. If V_{TIA} is beyond 400mV, non-linearity of *OA2* will introduce too much distortion. While if V_{TIA} is smaller than 100mV, both SNR and switching speed of following comparators will be degraded.

Trans-impedance gain of TIA is tuned by controlling the value of *R1, R2* and switching of *S1, S2*. *R1* and *R2* are implemented using digitally controlled resistor arrays shown in following Figure 16.

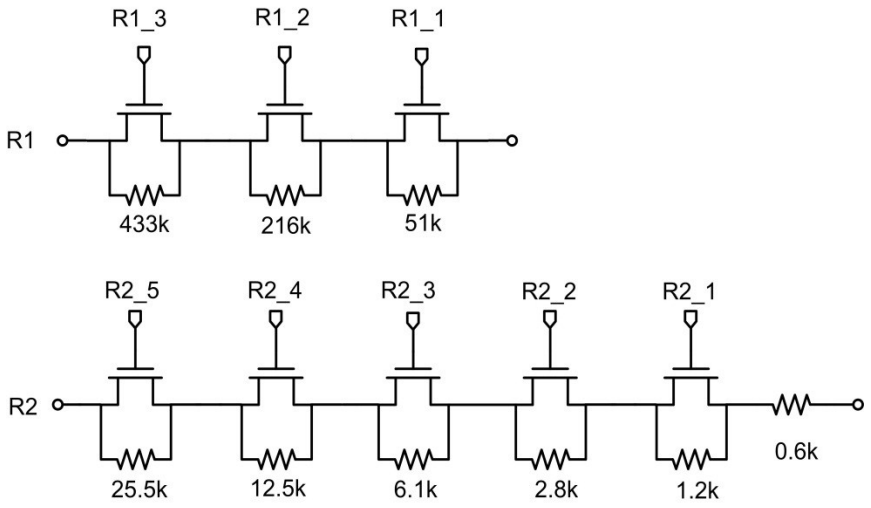

Figure 16. Schematic of R1 and R2

By applying different digital control signal, trans-impedance gain ranging from 2KΩ to 50.6MΩ can be obtained; Table 7 shows the TIA trans-impedance gain under different configurations.

R1(Ω)	R2 (Ω)	R3(Ω)	Gain (2nd Stage)	Z_{TIA}(Ω)
shorted	0.6k	Disable	2	2125
shorted	1.82 K	Disable	2	4420
shorted	3.43 K	Disable	2	7625
shorted	0.6 K	Disable	11	9830
shorted	1.82 K	Disable	11	20440
shorted	3.43 K	Disable	11	35270
shorted	7.87 K	Disable	11	75570
shorted	12.52 K	Disable	11	124300
shorted	25.4 K	Disable	11	243.1 K

shorted	50 K	Disable	11	448.8 K
50.9 K	50 K	Disable	11	915.8 K
216.5 K	0.6 K	Disable	11	1998 K
433 K	0.6 K	Disable	11	3987 K
700 K	0.6 K	7 K	11	7253 K
700 K	10.7 K	7 K	11	16.33 M
700 K	23 K	7 K	11	27.69 M
700 K	50 K	7 K	11	50.57 M

Table.7 TIA trans-impedance gain under different configurations

Peak detector circuit

Peak detector circuit (PDC) outputs the maximum value of V_{TIA}. Since V_{TIA} is a sinusoidal waveform oscillating around 0V, its maximum value equals to its amplitude, we can therefore extract the amplitude of V_{TIA} by using PDC.

Conventional method

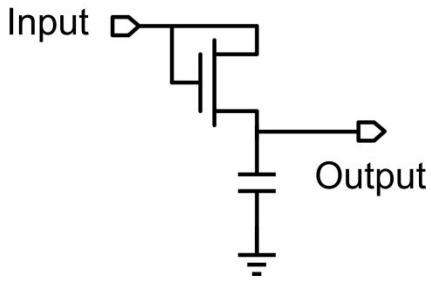

Figure 17. Peak detection solution 1 [19]

One way for peak detection mention in ref [19] is shown as Figure 17. This circuit consists of a diode connected NMOS and a hold capacitor. During the operation, NMOS is forward biased when the input voltage Vin is higher than voltage on capacitor Vc plus the threshold voltage Vth , and thus Vc will be charged up until Vc = Vin_max - Vth. When Vin drops, NMOS will be reverse biased and charges on hold capacitor will be kept which means that Vc will remain its value when Vin is less thatn Vin_max + Vth.

This circuit is simple to be implemented and doesn't consume extra power. However, it introduces DC shift between Vin_max and Vc. What's even worse is the shift's dependence on body effect of NMOS. Also, this circuit needs a buffer to avoid loading input.

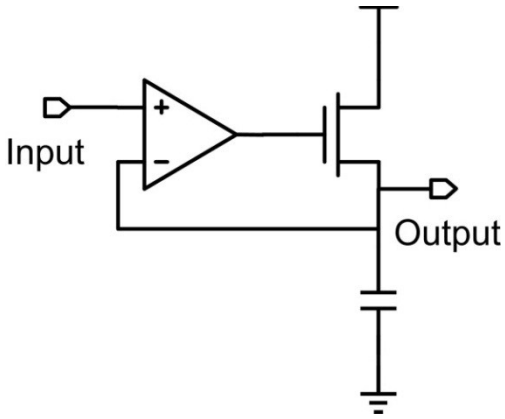

Figure 18. Peak detection solution 2 [19]

Another method for peak detection is shown in Figure 18. An opamp is employed as an error amplifier to control the conductivity of NMOS. When Vin is higher, opamp turns

on NMOS and starts charging capacitor. And when Vin is lower, NMOS is shut down and thus the voltage on capacitor can be retained.

This circuit removes the DC offset between Vin_max and output, it works well when the measurement is done at high frequency. Nevertheless, when the input signal is around KHz or even smaller, drain-to-source leakage current of NMOS slowly brings Vc to VDD and a wrong output is produced. This problem is even severer when opamp fails to completely bring NMOS into deep sub-threshold region as its input voltage difference become small. Another issue associated with this circuit comes from the NMOS transistor; it requires a Vth gate-to-source voltage drop to work in saturation region which implies that the highest output voltage can only be VDD – Vth, this voltage is quite limited in our design where VDD = 0.9 V.

Proposed structure

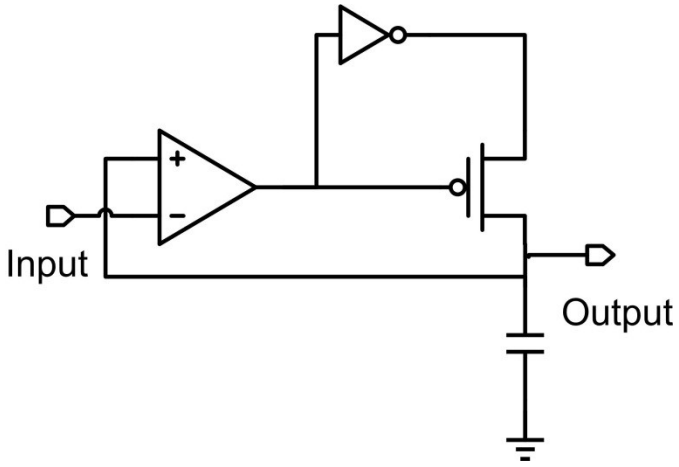

Figure 19. Proposed peak detection solution

The proposed peak detector in Figure 19 addresses these issues. Here a PMOS transistor is connected to the hold capacitor allowing for a higher peak output voltage. In order to reduce hold-stage leakage, the PMOS gate is controlled by the error amplifier output and its source is tied to an inverter also driven by the error amplifier. When the PDC input is higher than the output, the error amplifier output forces a low voltage on the PMOS gate and the inverter output forces VDD to the PMOS source, allowing the hold capacitor to charge up. In the hold state the PMOS is shut off with the gate driven to VDD and the source driven to VSS, providing much less leakage current to discharge the holding capacitor and superior low-frequency performance. The detailed PDC schematic is shown in Figure 20, which includes the transistor that resets the PDC between measurements.

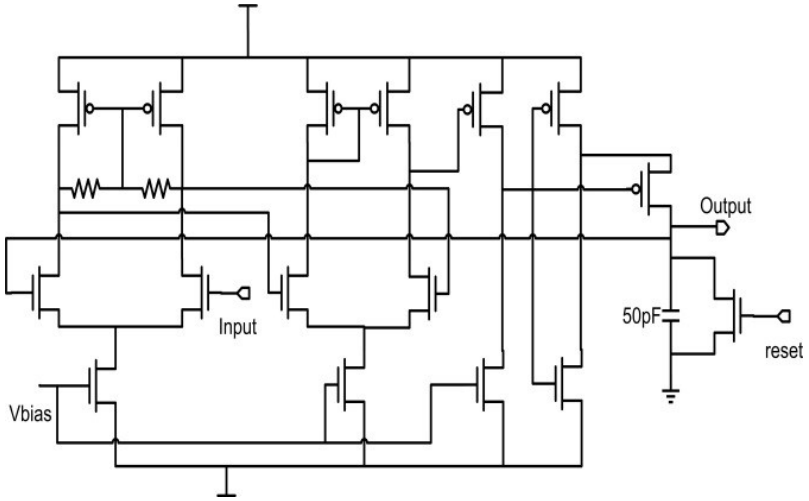

Figure 20. Proposed peak detection circuit

The capacitor used in peak detection circuit is 50 pF metal capacitor, its value is chosen such that fast response time can be achieved while the charge injection from NMOS diode and signal feed through from input capacitance of error amplifier are kept at acceptable level.

To illustrate the working process of PDC, we plot its transient responses in Figure 21 after applying 100Hz and 10MHz sinusoidal waveforms as input. The amplitude of inputs is swept from 100mV to 400mV.

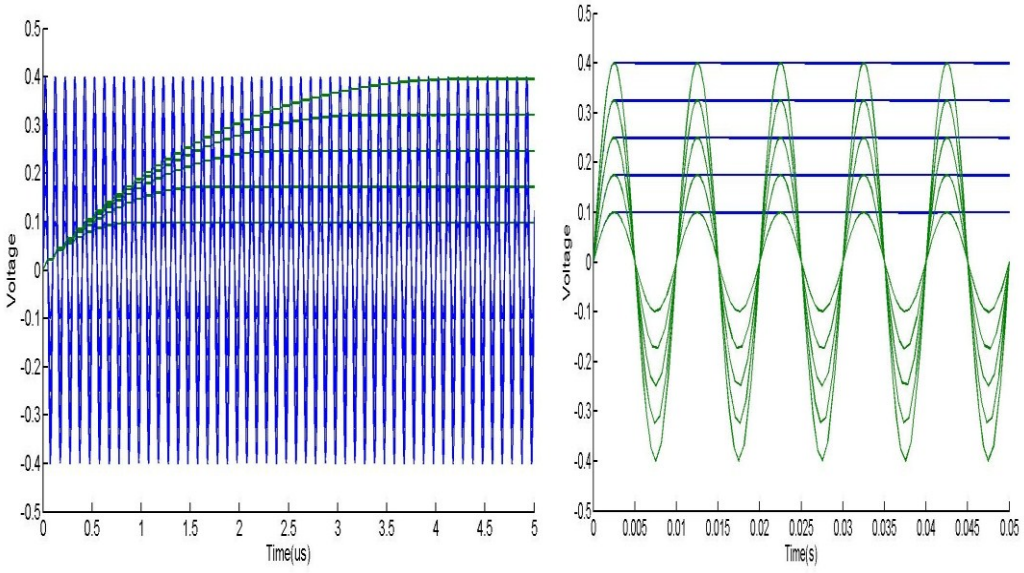

Figure 21. PDC transient response under different inputs

Comparators

Two comparators are employed to bring the output of TIA and the stimulus signal into full square waves without changing their phase. In the overview of section 2, stimulus signal is equally applied to cell sample and one comparator input; in actual measurement,

a passive power splitter is added in the signal path, it breaks the original stimulus signal into two phase-equal parts with different energy/amplitude. The one with smaller amplitude (designated to be 10 mV) is applied across cell sample; and the one with larger amplitude (typically around several hundred mV) is sent to the input of one comparator. Since both comparators deal with sinusoidal inputs with hundreds mV amplitude and convert them into ±900 mV square waves, same structure are used as shown in Figure 22.

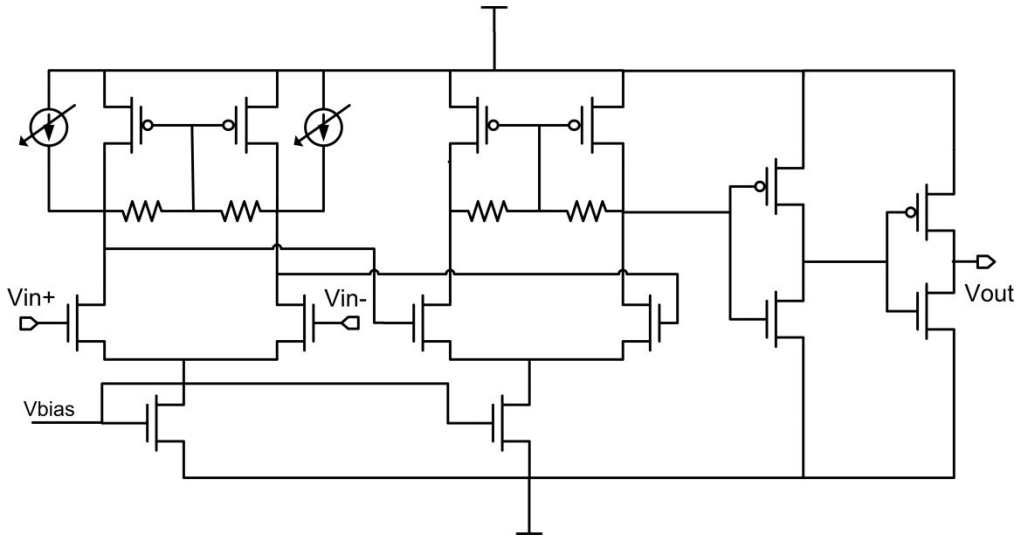

Figure 22. Schematic of comparator

This comparator can be viewed as a high gain opamp, it consists of two self-bias amplifier stages and two CMOS inverter stages. The self-bias current-steering amplifier utilizes two sensing resistors to extract common-mode voltage of its differential outputs and this common-mode voltage is used to bias the PMOS load. By this way, no extra common-mode feedback circuit is needed. By using two amplifier stages, not only DC

gain of comparator is increased, the effect of knick-back noise is also reduced due to the lengthening of signal path.

In order to cancel input offset of comparators, similar scheme as in TIA offset cancellation is used. Differently, 5 taps of PMOS current sources and PMOS current steering switch pairs are applied. Each comparator has its independent offset bias pin to adjust the bias current for offset cancellation current sources.

As a high gain opamp, the performance parameter of comparator is listed in Table 8.

Parameter	Value
Open loop gain	79.4 dB
3-dB bandwidth	60Mhz
Input Refer RMS Noise (1-10Ghz)	1.9mV
Power consumption	2.1 mW

Table.8 Performance of comparator

And a DC characteristic curve is plotted in Figure 23 as we sweep the input DC of comparator and observe the output.

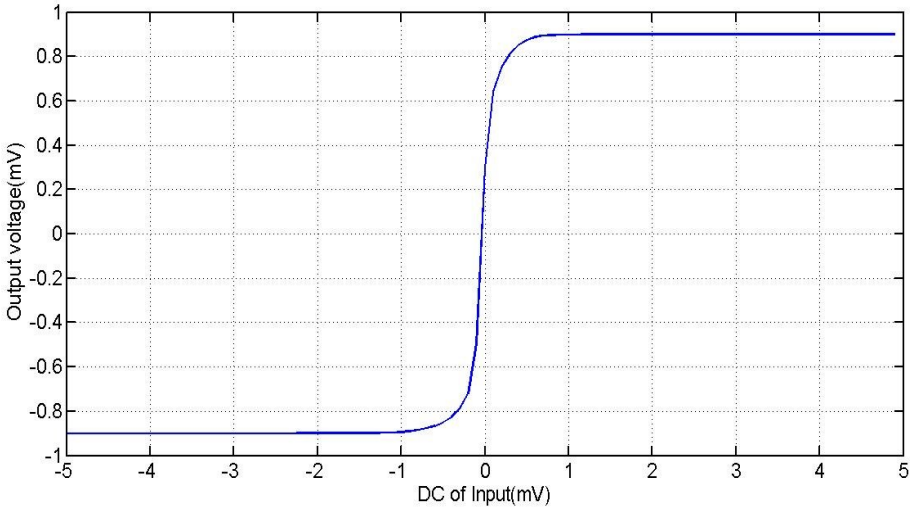

Figure 23. DC characteristic curve of comparator

Phase detector

Phase detector generates square waveform output with different duty cycle based on the phase difference of its inputs. A phase transfer characteristic curve is usually created to describe the relation between output duty cycle and input phase difference. An XOR gate can be employed as one type of phase detector like in ref [20]. Its phase transfer characteristic curve is shown in following Figure 24. As we can see, the curve has a saw-tooth shape and it is non-monolithic in the 0 to 2π region.

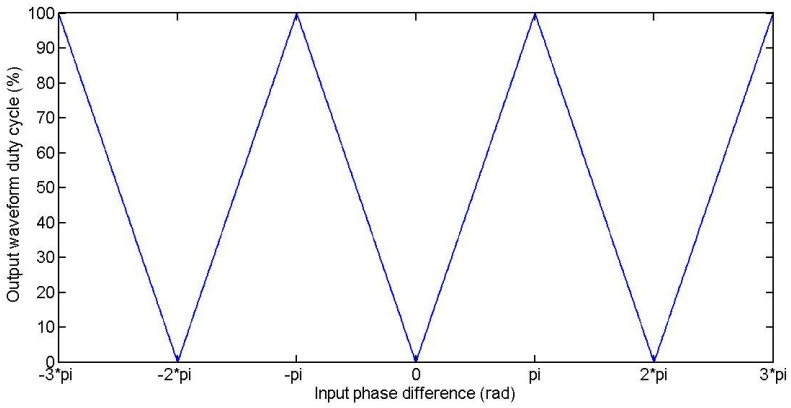

Figure 24. Phase transfer characteristic curve of XOR gate

Due to this non-monolithic property, it is impossible to differentiate a phase shift of π/2 and 3π/2 using an XOR gate. To solve this issue, a SR-latch based phase detector is used. It consists of a set-reset latch preceded by rising-edge pulse generators. This phase detector compares the rising edge of its inputs to determine their phase difference, thus, the monolithic region is expanded from 0 ~π to 0~2π. The schematic and phase transfer characteristic curve are shown in following Figure 25/26.

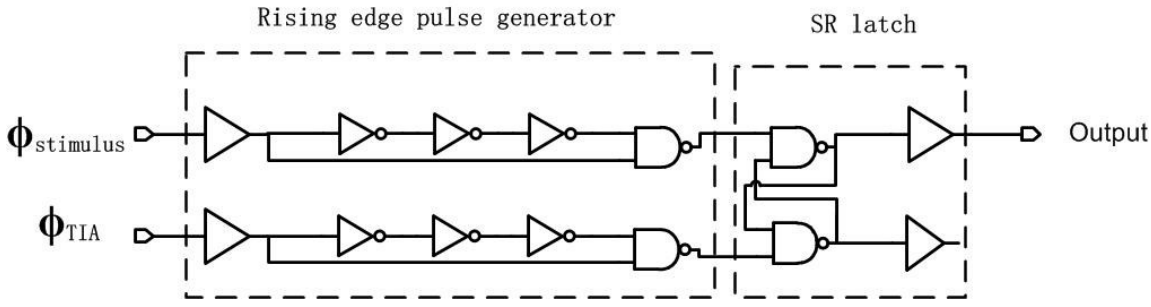

Figure 25. Schematic of SR latch based phase detector

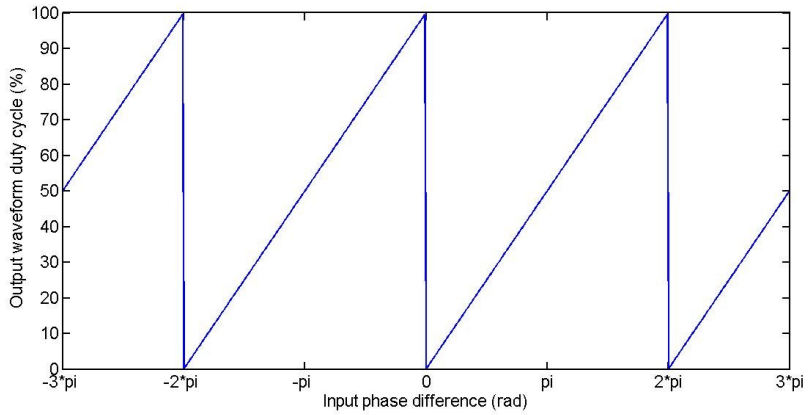

Figure 26. Phase transfer characteristic curve of SR latch based phase detector

This phase detector is capable of distinguishing a minimum 200ps time difference, which corresponds to a 0.72^{o} phase error at the maximum stimulus frequency 10MHz. Transient response in Figure 27 is plotted for functional illustration. As we can see from this illustration, pulse generator use rising edges of inputs at phase detector to produce short pulses, these short pulses will change SR latch's status and thus provide corresponding output.

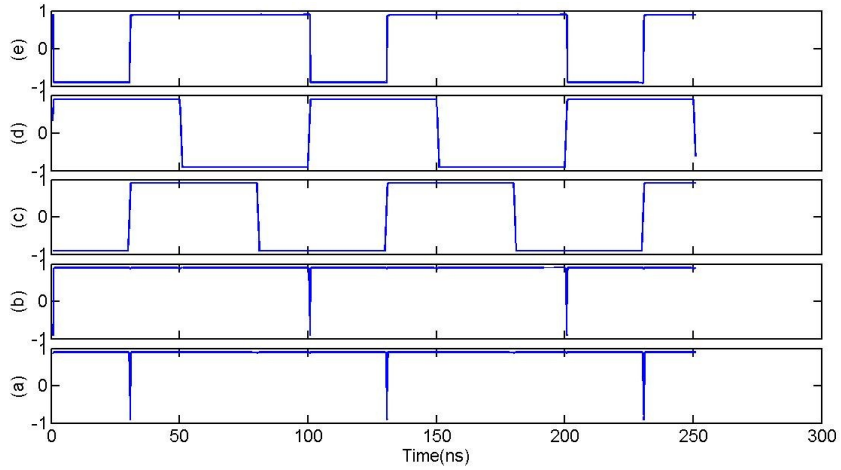

Figure 27. Functional demonstration of phase detector: (a)&(b) Rising pulse generator output, (c)&(d)inputs, (e)output

Time to digital converter

Topology overview

In order to digitize the duty cycle of phase detector output, a wide input range TDC is adopted. As shown in Figure 28, TDC consists of a time accumulator, which digitizes the time span when phase detector output is high, and a pulse counter, which counts the number of phase detector pulses. The time accumulator is implemented using 25 D-flip-flop based Clock-divde-by-2 stages. The pulse counter utilizes similar topology with only 5 stages.

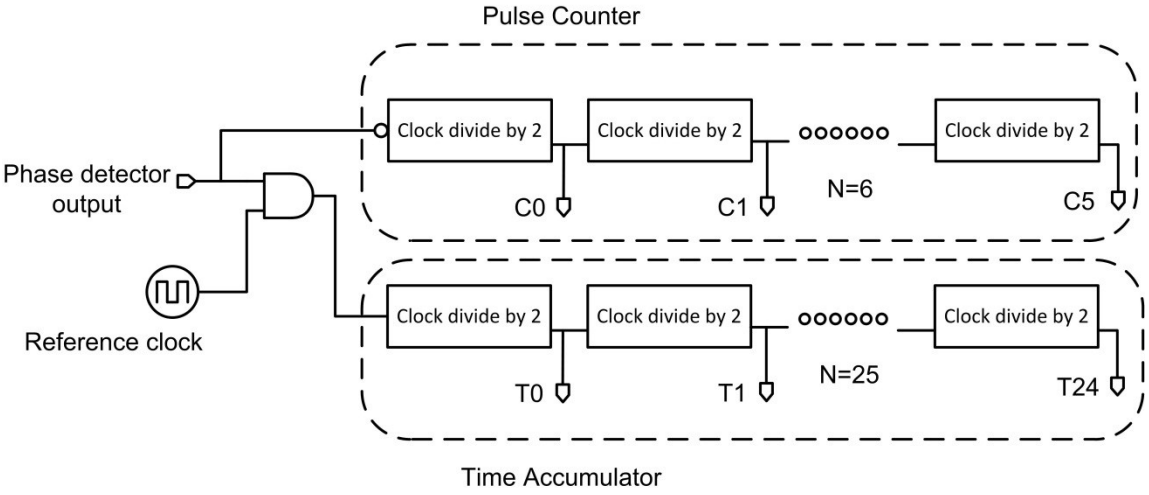

Figure 28. TDC topology

To understand how this TDC works, we first analyze the working scheme of each Clock-divide-by-2 cell. The clock-divide-by-2 cell is implemented using a D-flip-flop with its D port and Qbar port connected together as shown in Figure 29(a). A rising edge at the input toggles the output state as shown in Figure 29(b). This block can be viewed as a

rising edge triggered 1-bit counter. And its initial state can be set to 0 by assert the Reset port of D-flip-flop.

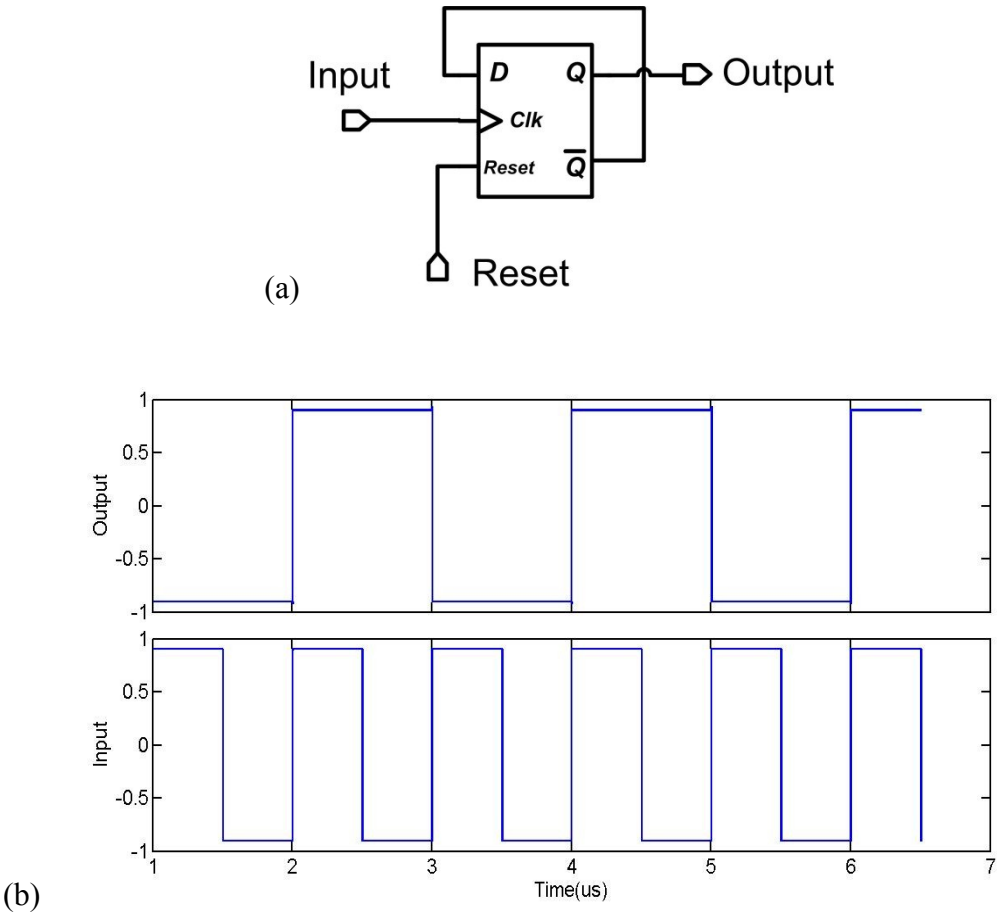

Figure 29. (a) Clock-divide-by-2 block (b) transient waveform

When N Clock-divide-by-2 cells are connected in series, an N-bit rising edge triggered counter is built. As an example, we put 3 Clock-divide-by-2 in series and plot its transient response as shown in Figure 30. It is clear from the transient waveform that every rising edge causes the output bits (with C2 as the highest bit) counting up.

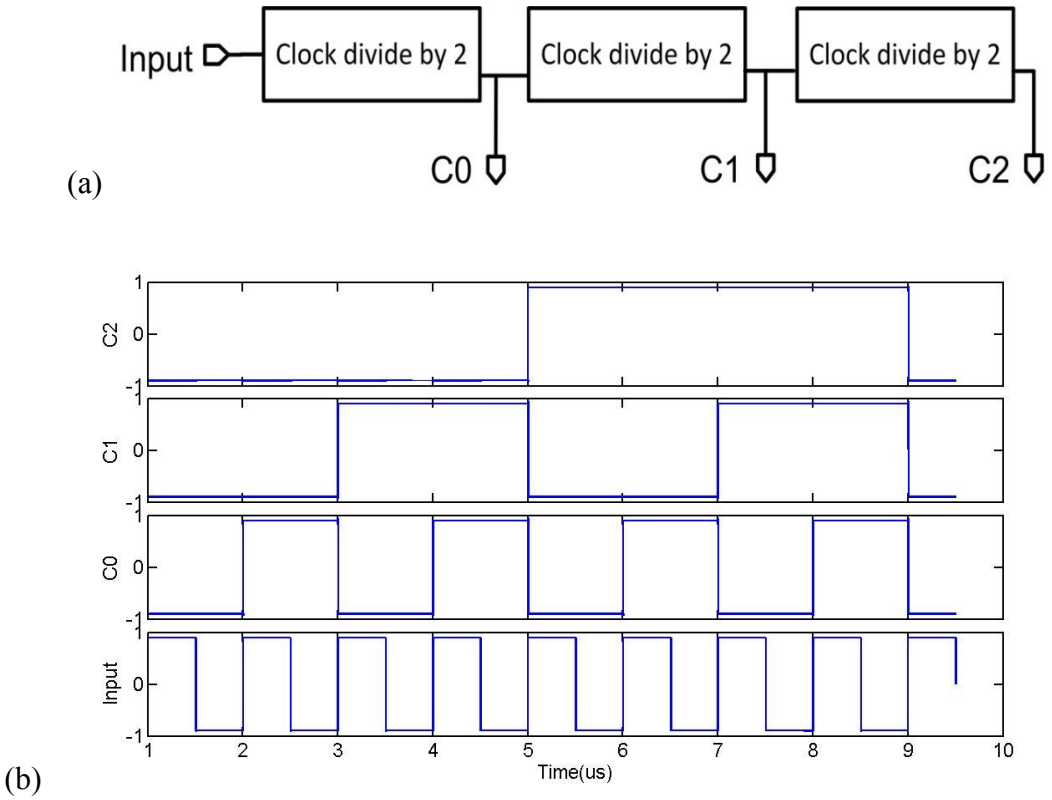

Figure 30. (a) 3-bit Clock-divide-by-2 counter (b) transient waveform

Based on the functional analyze on Clock-divide-by-2 based counter, we can move back to TDC. When phase detector output goes high, it allows the reference clock pass through AND gate and hits at the input of Time Accumulator. Then every rising edge of reference clock causes the Time Accumulator counts up and this upwards accumulating continues until phase detector output becomes low. Time Accumulator will retain its output value when phase detector outputs stays low and resume counting up when it is high again. At the same time, a falling edge of phase detector output causes the Pulse Counter counts up by 1; therefore, the Pulse counter indicates the total number of pulse

that Time Accumulator meets. To find out the time span of each phase detector output pulse, we can use following equation:

$$T_{pulse} = \frac{N_{Time\_Accumulator} \cdot T_{clock}}{N_{pulse}}$$

Where $N_{Time\_Accumulator}$ and N_{pulse} are the output number of Time Accumulator and Pulse counter, respectively; and T_{clock} is the period time of reference clock which is designated to be 300 ps in the design. The maximum number that Time Accumulator can get is $N_{max\_Time\_Accumulator} = 2^{25} = 33554432$. Therefore the input range of Time Accumulator is from 300ps to $T_{clock} \cdot N_{max_Time_Accumulator} \approx 10$ms. And this range can also be viewed as the input range of TDC.

Clock-divide-by-2 cell

The first Clock-divide-by-2 cell of Time Accumulator takes 300ps reference clock as input. Due to this high speed requirement, a dynamic D-flip-flop utilizing True Single-Phase edge-triggered flip-flop technique is employed as shown in following Figure 31. Corner condition simulation shows that this structure works fine with temperature variation from 0-127 Celsius degree and supply variation from 0.75-0.9 V.

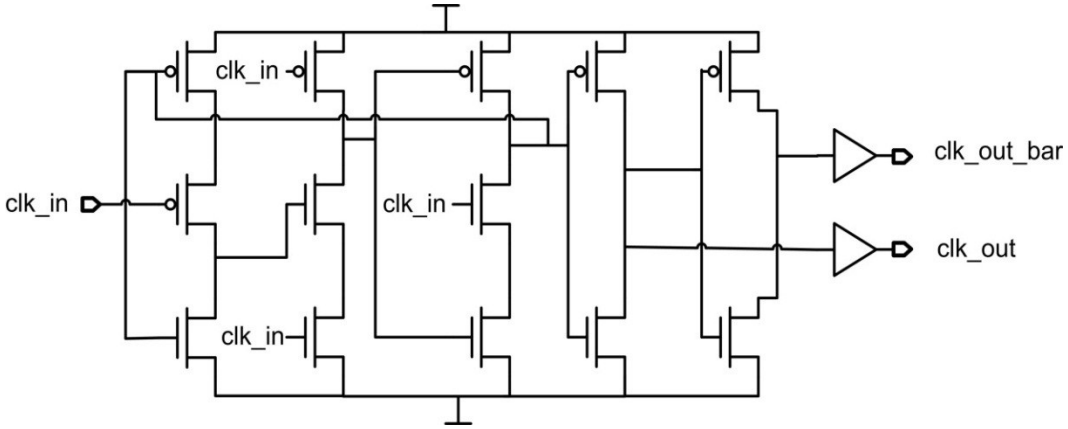

Figure 31. Clock-divide-by-2 cell based on true single-phase edge-triggered flip-flop

For the following stages of Time Accumulator and the Clock-divide-by-2 cells in Pulse Counter, static D-latched based D-flip-flop is adopted for circuit realization. Schematic of this static D-flip-flop is shown in following Figure 32.

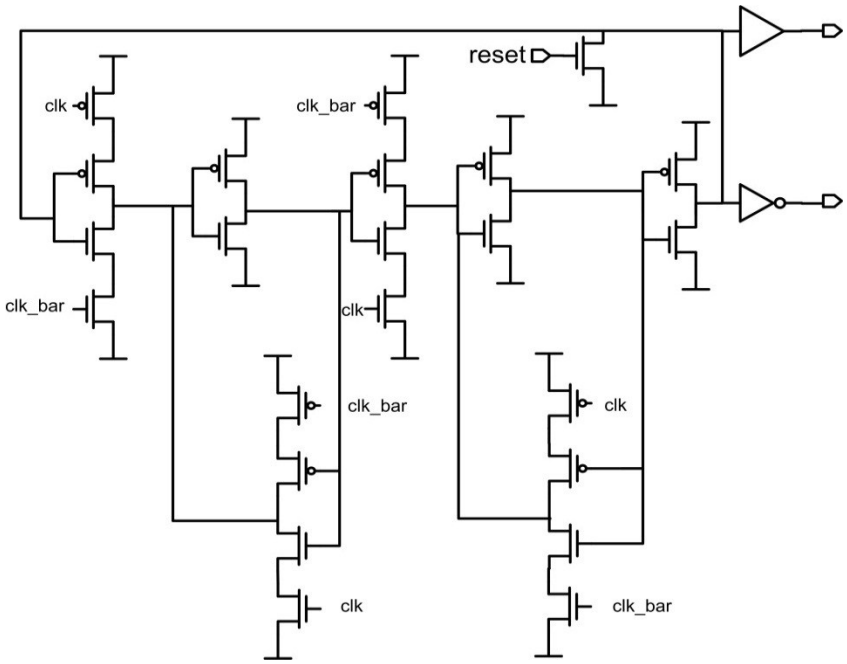

Figure 32. Clock-divide-by-2 cell based on static D-flip-flop

TDC control logic

TDC control logic is used for not only controlling the start/stop of TDC operation, but also for selecting TDC input source. In the actual IS front-end, TDC is used for measuring pulse width of a) phase detector output and its complimentary counterpart b) outputs of both comparators. By measuring pulse widths of both phase detector output and its complimentary counterpart, we can obtain accurate period time of stimulus signal after adding these two widths together. This gives us more flexibility in choosing stimulus signal source by removing requirement for accurate signal frequency control. The measurements of comparator outputs' width are conducted for comparator offset calibration, this will be discussed later.

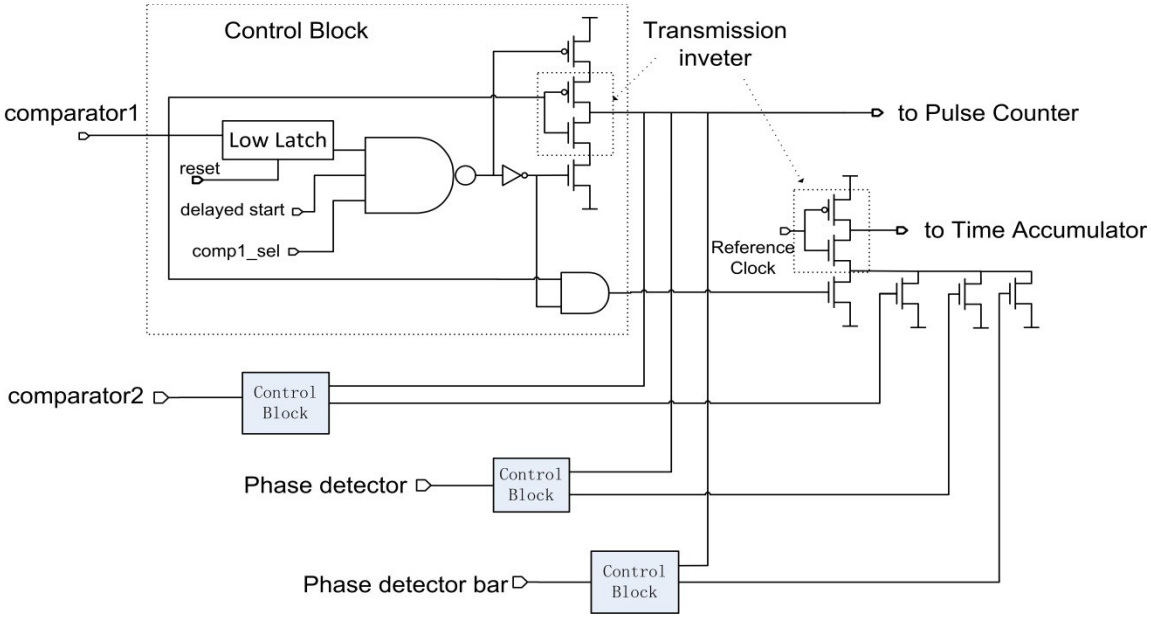

Figure 33. TDC control logic overview

The overview of the TDC control logic is shown in Figure 33. Each TDC input source (comparator 1 &2, Phase detector output & bar) goes into a control block; the outputs of these control blocks will be MUXed and fed into the Pulse Counter and Time Accumulator of TDC.

The control block utilizes a 3-input AND gate which take 1) *source selection signal* (like *comp1_sel* in comarator1's control block), 2) *delayed start signal* and 3) *source stay low indicator signal* as inputs; when its output becomes high, TDC will begin to work with corresponding source as input. The *source selection signal* is directly controlled by MCU. A Start Control block is used to generate the *delayed start signal* and distributes it to each Control block. A Low Latch block generates *source stay low indicator signal* to guarantee that source signal is low before it turns on TDC so that full pulse width is sent to TDC instead of only partial of the pulse width.

The schematic of Start Control block is shown in following Figure 34. Its input, *start* signal, comes from MCU. When *start* signal is asserted, one impedance measurement begins; when it is de-asserted, the measurement will stop, and then both PDC and TDC outputs are sent back to MCU for further processing.

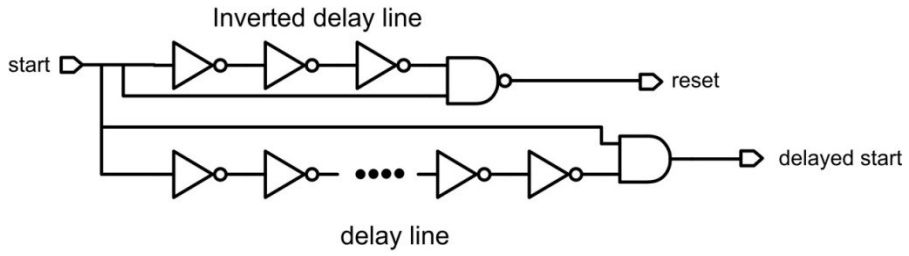

Figure 34. Schematic of start control block

Upon the assertion of *start* signal, Start Control block generates a *reset* signal pulse which clears the previous state of TDC; after the *reset* signal it will pull up *delayed start* signal to officially begin one measurement. When the *start* signal turns low, however, the *delayed start* signal is pulled down immediately so that TDC is shut off before the next pulse occurrence of source signal. A transient response of Start Control block is plotted in Figure 35 for better illustration.

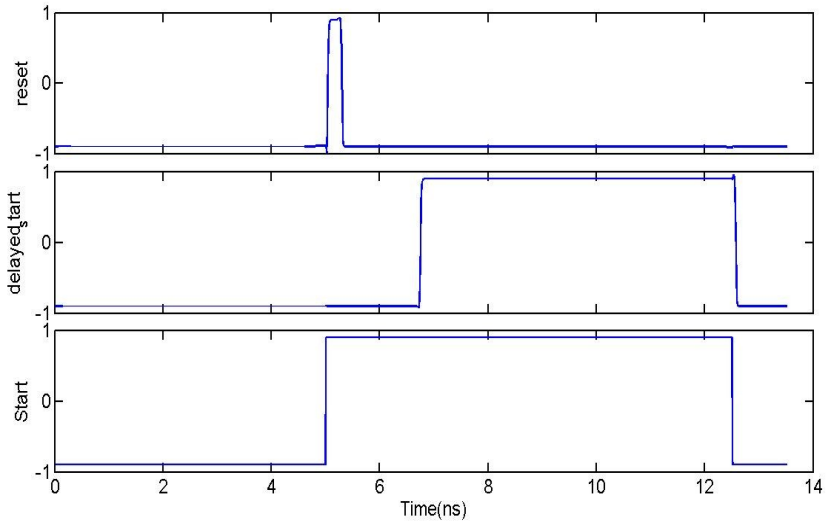

Figure 35. Transient response of start control block

The Low Latch block is introduced to make sure that when *delayed start* signal asserts during one pulse of source signal, TDC will not accumulate the rest of this pulse, instead, it will begin the conversion until the next full pulse takes place. The schematic of Low Latch block is shown in for Figure 36. Its internal latch uses two cross-connected inverters. A *reset* signal from Start Control Block clears the stored state and thus pulls down output. Right after *reset* signal, the *delayed start signal* becomes high, at this

moment, Low Latch block's output is still low if source signal is high, it will only be pulled up until source signal experiences a low level state.

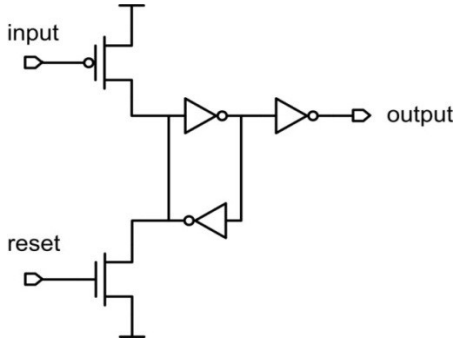

Figure 36. Schematic of low latch

Figure 37 shows the response of Low Latch block under different scenarios.

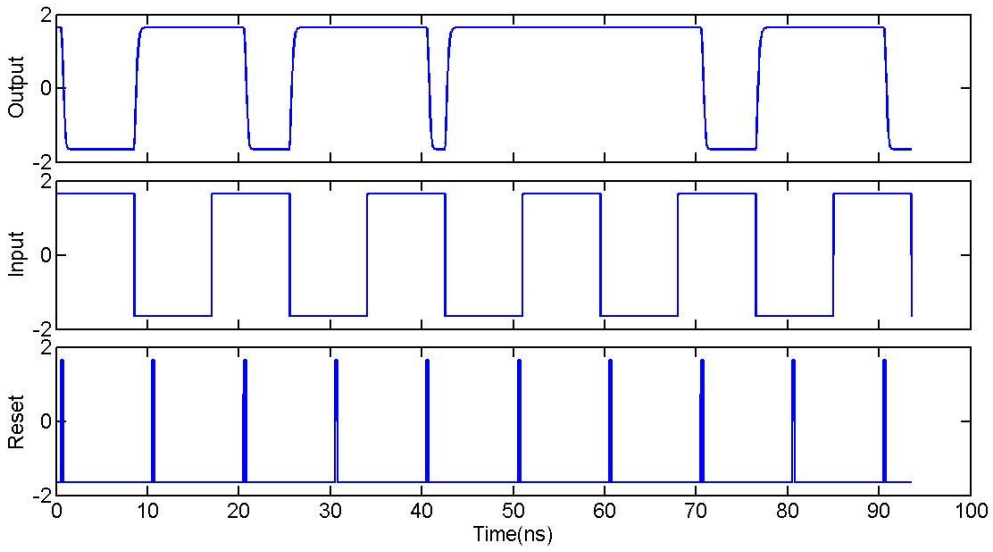

Figure 37. Transient response of low latch

When the output of 3-input AND in Control Block is high, it allows corresponding source signal transmitting to Pulse Counter by enabling the inverter in the transmission

path. Other source signals cannot control Pulse Counter since their transmission inverters are disabled and kept at high-impedance output. Similarly, when the enabled source signal is high, it allows reference clock pass through a transmission inverter and hit at the Time Accumulator. The transmission inverter of reference clock is controlled by four parallel NMOS connected to its source, whenever one of these NMOSs is turned on by certain source signal, the transmission inverter will be enabled.

Scan chain

Scan chain technique is used to write/read digital settings/outputs in a chip by combining all these digits into a series stream and flush in/out this stream. A scan chain can be viewed as a long shift register, part of this shift register is used for reading digital outputs, while the other part is used to set digital configuration.

Scan in cell

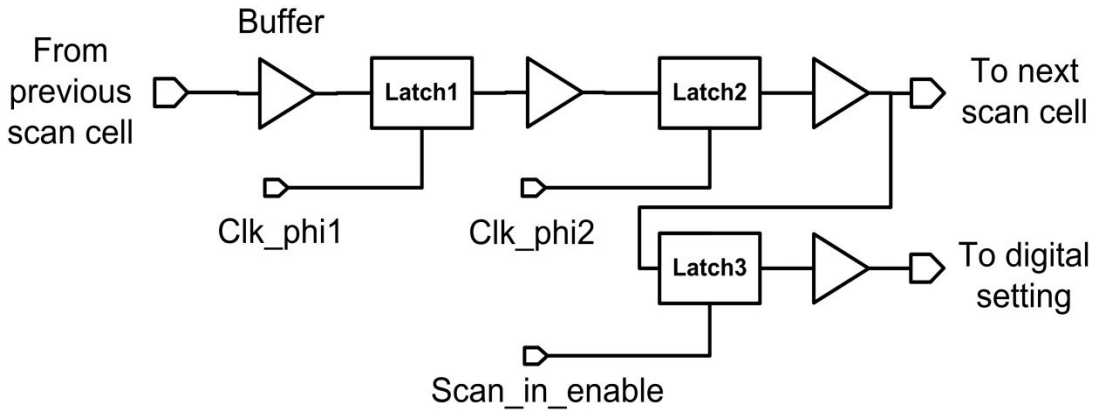

Figure 38. Scan in cell block view

Scan in cell as shown in Figure 38 is for setting digital configuration in a chip. It consists of 3 latches. *Latch1* is used to read in the state of previous scan cell, it is enabled when *Clk_phi1* signal is high. *Latch2* is used to keep the value of *Latch1* and pass it to next scan cell. *Latch3* is enabled by high state of *Scan_in_enable* signal. It acquires the output of *Latch2* during the high state of *Scan_in_enable* and uses it to set corresponding digital configuration. *Latch3* keeps output unchanged when *Scan_in_enable* is low so that a bit stream flowing through *Latch1* and *Latch2* will not directly impact digital configuration. This structure guarantees that unwanted digital combination will not appear while still keeping the arbitrariness of flushed bit stream.

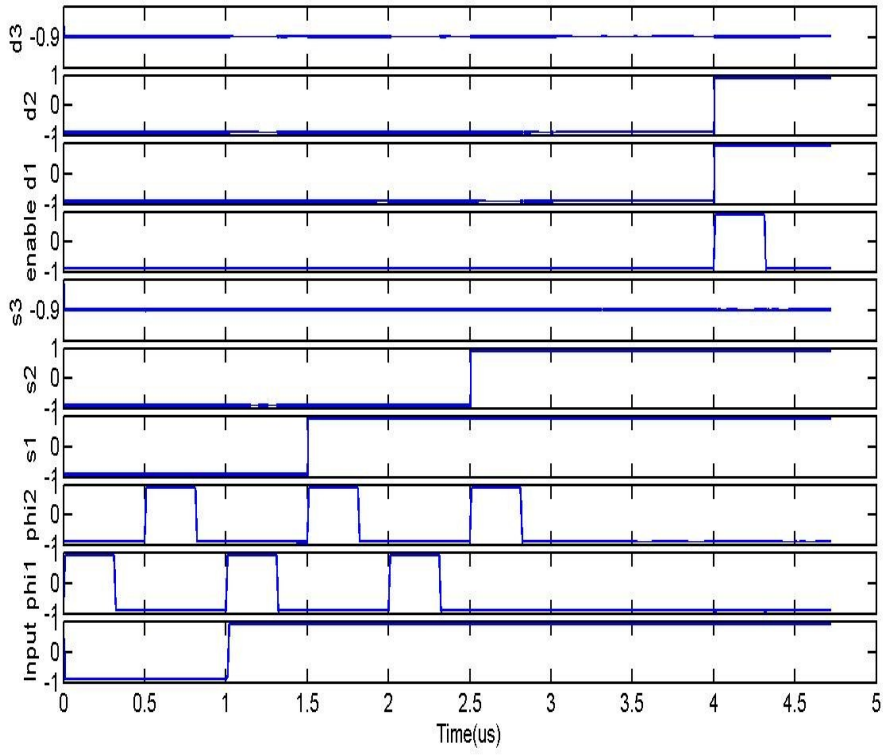

Figure 39. Transient response of 3 scan in cell series

As an example, we put 3 scan in cells in a chain, and intend to flush in a bit stream (110 in this case). Figure 39 shows the transient response of each node in this simple scan chain. In the Figure 39, *s1, s2, s3* are the outputs the *Latch2* in each scan in cell; and *d1, d2, d3* are the outputs of *Latch3*, they are the actually digital control bits. It is worth to notice that *phi1* and *phi2* are non-overlapping signals and *phi1* should be earlier. *Input* signal is sampled at during high state of *phi1*.

Scan out cell

Scan out cell as shown in Figure 40 is used to read digital output bits from a chip. It has similar structure with Scan in cell. *Latch1* and *Latch2* are used to shift bit stream along the chain. A multiplexer controlled by *Scan_out_enable* signal is used to select source of *Latch2.* A digital output bit will be read into *Latch2* when *Clk_phi2* pulse occurs during the high state of *Scan_out_enable* signal.

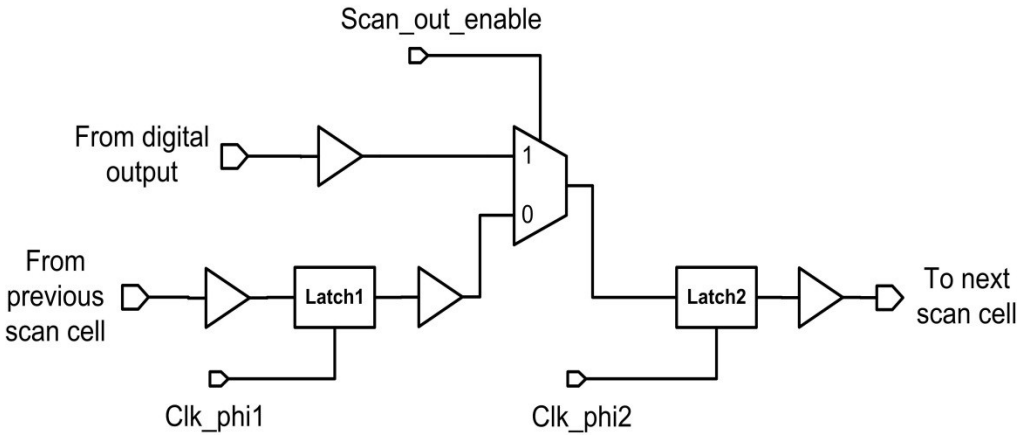

Figure 40. Schematic of a scan out cell

Again, we put 3 scan out cells in series to illustrate its working scheme. This time, we need to read digital outputs (011) out through the scan chain. The *Scan_out_enble* signal is firstly pulled high; during this time, a *phi2* pulse happens and read digital bits into each scan out cell. Then *phi1* and *phi2* are pulled up alternatively to flush these digital bits out through *s3*. Note when the output digits are flushed out, they are in reverse order comparing to their relative position in scan chain, therefore, the bits *s3* reads out is 110. The transient response is shown in Figure 41.

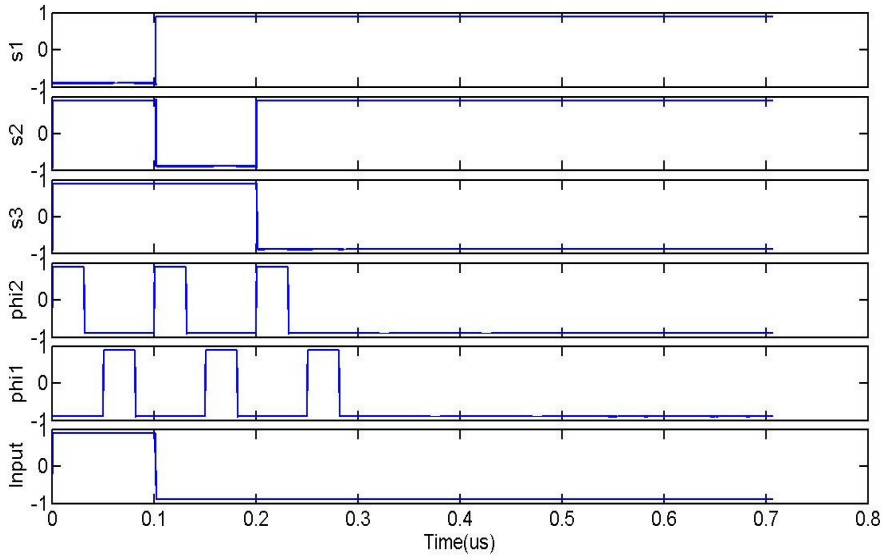

Figure 41. Transient response of 3 scan out cell series

Scan chain data series

67 scan in/out cells are connected in series as the scan chain. Note, the outputs of Pulse Counter in TDC are not scanned by scan chain. Instead, they are directly routed to pins

of chip. Thus, the outputs of Pulse Counter can be immediately read by MCU and used as a flag to terminate one measurement.

To be more detailed, 10 scan in cells are assigned for TIA configuration, 28 scan in cells are used to TIA and Comparators' offset cancellation, 4 scan in cell are used to select input source for TDC and 25 scan out cells read the outputs of Time Accumulator in TDC.

Pre-measurement Steps

We need to go through several steps before measurement in order to have more accurate results. These steps include: 1) offset cancellation for TIA and each comparator, 2) calibrations for impedance magnitude and phase measurement.

TIA offset cancellations

As we discussed in section 4.1.2, significant DC offset at TIA output limits the output swing. Offset cancellation needs to be done though the offset cancellation circuit at OA1 to reduce the effect. To carry out TIA offset cancellation, we firstly set the amplitude of stimulus signal to 0 and then measures the output of PDC. Since only DC offset of TIA is contributing to the PDC output at this time, we have a direct measurement of offset. By digitally tuning offset cancellation circuit of OA1, this offset can be adjusted. And the tuning process is completed when a less than 10mV positive offset is observed at output of PDC.

Comparator offset cancellation

Input offset of comparator will cause asynchrony between input sinusoidal and output square waveform since the rising edge of square form does not exactly occur at the zero-crossing point of sinusoidal wave. To cancel this offset, we first notice that when a sinusoidal waveform is sent to one input of comparator and an offset is presented at the other input, this offset will vary the original pulse width at output as shown in Figure 42. Therefore, measurement on the pulse width of comparator output can be used as a reference for offset cancelling. And TDC provides us the possibility for this idea.

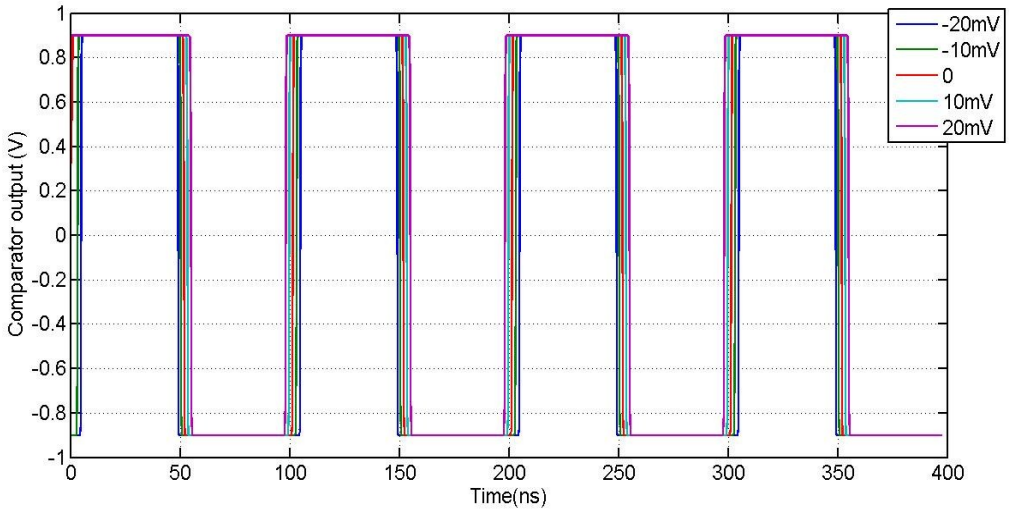

Figure 42. Transient response of comparator output upon different offsets

To eliminate the comparator offset, we turn on the stimulus signal and measure the pulse width of each comparator's output. Then the offset cancellation circuit in each comparator is digitally tuned until the comparator output has 50% duty cycle.

Calibration

Calibration for impedance magnitude measurement

After getting the amplitude of TIA output $|V_{peak}|$ from peak detection circuit, we can directly apply it to calculate the magnitude of cell impedance as

$$|Z_{sample}| = \frac{|Vs| * |Z_{TIA}|}{V_{peak}}$$

However, the value of $|Z_{TIA}|$ is not exactly known; besides, non-idealities like finite opamp gain and input offsets also introduce errors to above equations. To solve these problems, pre-measurement calibration needs to be conducted. To understand this calibration process, recall from section 3.1.1:

$$V_{TIA\_S1\_ON} = Vs * \frac{-A1 * (R1 * R2 + R2 * R3 + R1 * R3)}{(R1 * R2 + Z * R3 * A1 + R1 * R3 + Z * R2 + Z * R3 + R2 * R3)} * \frac{A2 * (R4 + R5)}{(R4 * A2 + R4 + R5)}$$

$$V_{TIA\_S1\_OFF} = Vs * \frac{-A1 * (R1 + R2)}{(Z * A1 + R1 + Z + R2)} * \frac{A2 * (R4 + R5)}{(R4 * A2 + R4 + R5)}$$

Taking the TIA offset and PDC offset which into account, we have:

$$V_{peak\_S1\_ON} = V_{TIA\_R3\_ON} + V_{TIA\_offset} + V_{peak\_detection\_offset}$$

$$V_{peak\_S1\_OFF} = V_{TIA\_R3\_OFF} + V_{TIA\_offset} + V_{peak\_detection\_offset}$$

Both of these two equations can be simplified as:

$$V_{peak} = \frac{K}{M * Z + B} + DELTA$$

In the equations above, only V_{peak} are known and we need to find out the value of Z. First, we notice that when Vs = 0 then K =0 which indicates that V_{peak} = DELTA. So the value of DELTA can be obtained by shorting TIA input to ground and measures PDC output. After that, we apply two different known-value resistors as the sample under measurement and record the output of PDC. This will gives us following equations:

$$V_{peak\_cali\_1} = \frac{K}{M * R1 + B} + DELTA$$

$$V_{peak\_cali\_2} = \frac{K}{M * R2 + B} + DELTA$$

By solve these equations, the value of M and B can be expressed as:

$$M = \frac{K \cdot (V_{peak\_cali\_2} - V_{peak\_cali\_1})}{(V_{peak\_cali\_1} - DELTA)(V_{peak\_cali\_2} - DELTA)(R1 - R2)}$$

$$B = \frac{K}{V_{peak\_cali\_1} - DELTA} - M \cdot R1$$

Substitute M and B into the equation from the actual sample measurement, we can get the value of measured sample impedance magnitude:

$$Z = \frac{(V_{peak\_cali\_1} - DELTA)(V_{peak\_cali\_2} - DELTA)(R1 - R2)}{(V_{peak\_cali\_2} - V_{peak\_cali\_1})(V_{peak} - DELTA)}$$

$$+ \frac{DELTA \cdot (R1 - R2) - R1 \cdot V_{peak\_cali\_1} + R2 \cdot V_{peak\_cali\_2}}{V_{peak\_cali\_2} - V_{peak\_cali\_1}}$$

All the variables in the above equation are known so that Z can be calculated directly. By using this calibration method, non-ideality due to finite opamp gain and TIA/PDC output offsets can be eliminated. This calibration needs to be completed for each TIA configuration. Also the values of the known value resistors R1 and R2 need be chosen for each of the calibrations so that V_{peak_cali} can always fall in 100mV to 400mV range.

Calibration for impedance phase measurement

Similar to the calibration method done in board level system, a standard known-value resistor replace the sample cell and measurement is conducted. Due to the intrinsic phase shift caused by TIA at high frequency (>1MHz), we can observe a phase value less than 0 at the Phase output. If we denote this phase value as $\varphi_{standard}$ and the phase output of sample cell as φ_{cell} , then the actual phase shift of sample cell can be calculated as:

$$\varphi = \varphi_{cell} - \varphi_{standard}$$

Chip Layout

The full chip layout is shown in Figure 43, it consists of 28 pins and the active area is 0.3 mm^2.

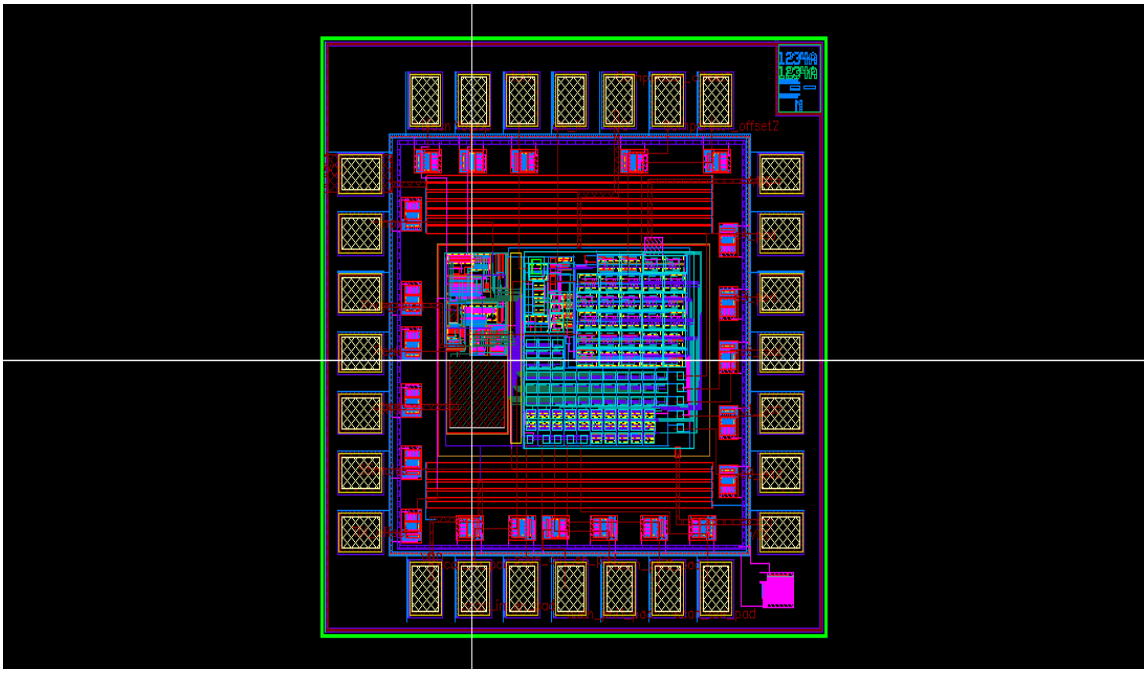

Figure 43. Chip layout of IC IS

Simulated Results

TIA performance test

TIA is the first block in signal path; therefore, it majorly determines the noise and speed performance of the whole system. We have run a series of tests under different TIA configuration, and Figure 44 shows the simulated result.

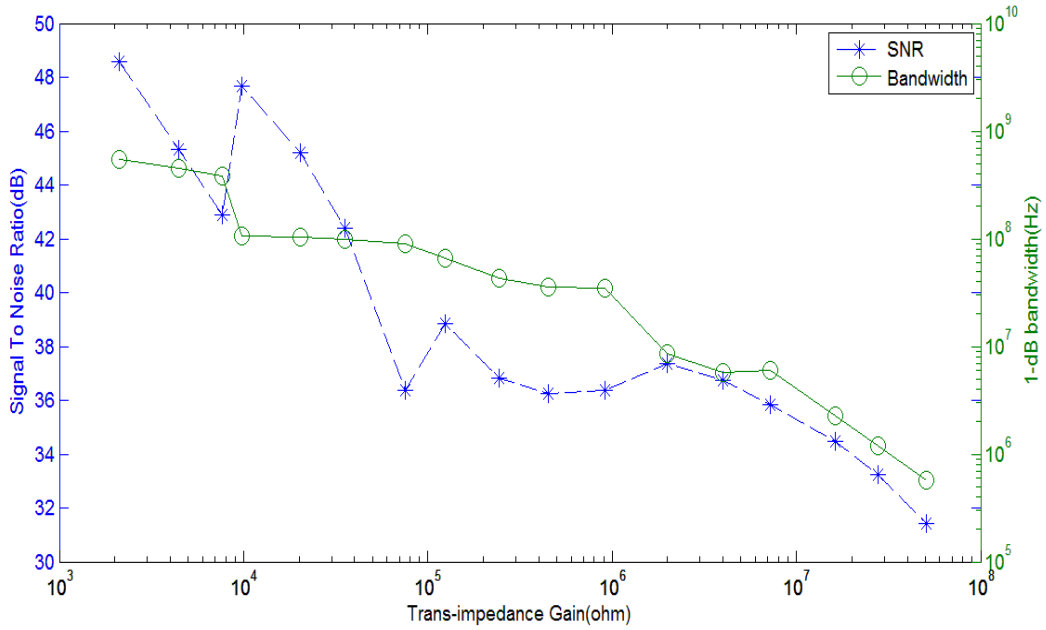

Figure 44. TIA bandwidth and output SNR

In this test, the trans-impedance gain of TIA is swept from 2KΩ to 50MΩ; corresponding 1-dB bandwidth and output SNR (noise integrated from DC to 10GHz) are plotted. The bandwidth decreases roughly proportional to the increase in TIA gain, with a >10MHz bandwidth up to a gain of 1MΩ and a 580 KHz bandwidth at the maximum gain setting. While 10MHz measurements are not possible for TIA gain settings above 1MΩ, this high gain setting is generally not required for high frequency measurements due to typical cell impedance magnitudes' frequency response. The output SNR results are for a 400mV$_{rms}$ output signal level, assuming a 10mV input and a constant ratio between the TIA gain and sample impedance. An SNR in excess of 30dB is achieved over the entire TIA gain setting range, with the discontinuities in the curve due to the different gain modes of TIA operation.

Measurement accuracy test

To test the measurement accuracy, two cell models featured at low and high impedance are used for testing. Both of them have same structure as in Figure 45. For low impedance model, Rs = 300Ω, Rp=7KΩ and Cp=2nF. As for high impedance model, Rs = 8KΩ, Rp=1MΩ and Cp=100pF

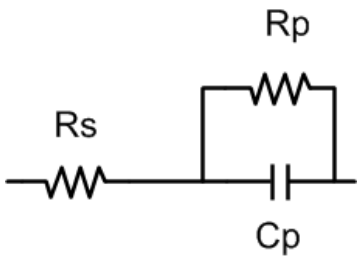

Figure 45. Cell model used for accuracy test

The measured and ideal impedance for each model (1 for low impedance model) are plotted in Figure 46. For both cell models the measurement magnitude and phase curves fit well with the ideal curves. Over a frequency range of 100Hz-10MHz, the maximum magnitude and phase errors are 2.5% and 2.2^{o}, respectively.

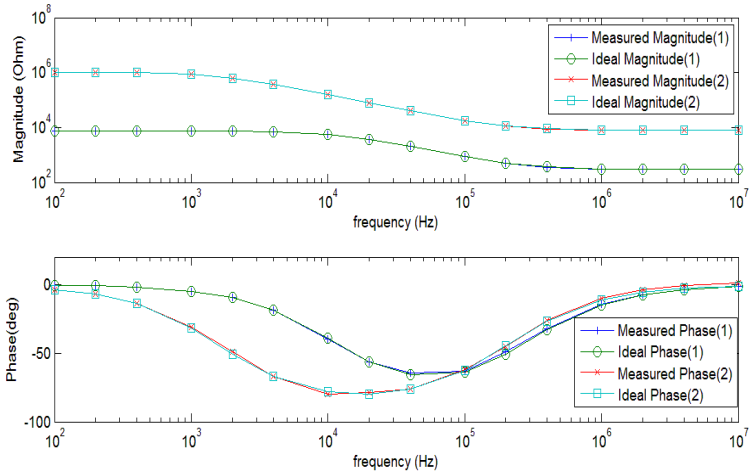

Figure 46. Accuracy test result

Performance summary

Parameter	This work	Ref [9]	Ref [21]
Technology	0.18μm CMOS	0.35 μm CMOS	0.35 μm CMOS
Supply Voltage	±0.9V	±2.5V	3.3V
Frequency range	100Hz ~ 10MHz	100Hz ~ 100KHz	10Hz ~ 50MHz
Impedance magnitude range	100Ω ~ 1MΩ	N/A	N/A
Measurement time	>Max(6μs,1/fs)	N/A	1.1s (1KHz LPF bandwidth)
Magnitude Measurement error	<2.5%	<3.5 %	N/A
Phase Measurement error	<2.2°	$<3.6^{o}$	N/A
Stimulus Signal level	10mV	N/A	10mV
Power Consumption	28mW	21mW	84mW (10 ×10 array)
Area	$0.3mm^2$	$0.4\ mm^2$	$4mm^2$

Table.9 IC solution performance summary

The performance summary for proposed IC solution is listed in Table 9, together with 2 reference work. Thanks to the elimination of LPF, the measuring time of proposed IC solution is largely reduced. Also, the current-to-voltage stage of reference [9][21] are realized using fixed resistance. Therefore, the impedance input range of these works is limited compared to the trans-impedance gain adjustable TIA structure.

IV CONCLUSION

In this work, two impedance spectroscopy systems are presented. The board level system is built with a frequency measuring range from 1KHz to 100KHz. It is used to collect preliminary experimental data and helps us gain insight towards IS system. An IC level IS front-end is then proposed which utilizes a time-to-digital converter (TDC) and a peak detector circuit (PDC) for rapid measurement of both impedance phase and magnitude, respectively. This system is capable of measuring cell impedance from 100Hz to 10MHz with 10mV minimum stimulus signal. It can be applied in cytometry systems with fast flow rates monitoring ability or used for scan massive sensor array systems with faster scan rate.

Further improvement to the IC level IS front-end involves reducing the hold capacitor size of PDC and decreasing noise. Conventional lock-in amplifier has a good noise performance since demodulation and low pass filter allows only narrow band noise around stimulus frequency to pass through. Similarly, in order to suppress flicker noise in the system, a highpass/bandpass can be added in the signal path or choking techniques may be applied.

To demonstrate the functionally of our IC level IS system, a biosensor array or a microfluidic device may be integrated on the top of chip to monitor cell behavior, this is another important aspect of future work.

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APPENDIX

SAMPLING AND COMMUNICATING CODE FOR MCU

Code for

```
//-----------------------------------------------------------------------------
// F06x_SAR16Data.c
//-----------------------------------------------------------------------------
// Copyright (C) 2005 Silicon Laboratories, Inc.
//
//
// Data Acquisition example for 'F06x
//
// Target: C8051F060TB Target Board
//
//-----------------------------------------------------------------------------
// Includes
//-----------------------------------------------------------------------------
#include <c8051f060.h>                    // SFR declarations
#include <stdio.h>

//-----------------------------------------------------------------------------
// 16-bit SFR Definitions for 'F06x
//-----------------------------------------------------------------------------

sfr16 DMA0DS   = 0xDB;                 // DMA0 XRAM Address Pointer
sfr16 DMA0CT   = 0xF9;                 // DMA0 Repeat Counter Limit
sfr16 DMA0DA   = 0xD9;                 // DMA0 Address Beginning
sfr16 DMA0CS   = 0xFB;                 // DMA0 Repeat Counter

sfr16 RCAP2    = 0xCA;                 // Timer2 capture/reload
sfr16 TMR2     = 0xCC;

sfr16 RCAP3    = 0xCA;                 // Timer3 reload value
sfr16 TMR3     = 0xCC;                 // Timer3 counter

//-----------------------------------------------------------------------------
// Global CONSTANTS
//-----------------------------------------------------------------------------

#define SYSCLK 3062500                   // SYSCLK frequency in Hz
#define BAUDRATE 1200                   // Baud Rate for UART0

// DMA INSTRUCTIONS
#define DMA0_END_OF_OP     0x00          // End-of-Operation
#define DMA0_END_OF_OP_C   0x80          // End-of-Operation + Continue
#define DMA0_GET_ADC0      0x10          // Retrieve ADC0 Data
#define DMA0_GET_ADC1      0x20          // Retrieve ADC1 Data
#define DMA0_GET_ADC01     0x30          // Retrieve ADC0 and ADC1 Data
#define DMA0_GET_DIFF      0x40          // Retrieve Differential Data
```

```
#define DMA0_GET_DIFF1     0x60           // Retrieve Differential and ADC1 Data


#define NUM_SAMPLES        1000          // Number of ADC sample to acquire (each sample 2
bytes)
#define XRAM_START_ADD     0x0000         // DMA0 XRAM Start address of ADC data log
#define SAMP_RATE          12         // ADC sample rate in Hz

sbit BUTTON = P0^6;                       // pushbutton on the target board

//-----------------------------------------------------------------------------------
// Function PROTOTYPES
//-----------------------------------------------------------------------------------
void SYSCLK_Init (void);
void UART0_Init (void);
void PORT_Init (void);
void ADC_Init (void);
void DMA0_Init (void);
void Timer3_Init (int counts);
void EMIF_Init (void);
void SendData(void);

//-------------------------
// Global Variables
//-------------------------
unsigned char Conv_Complete = 0;
unsigned int xdata * data read_ptr;

//-----------------------------------------------------------------------------------
// MAIN Routine
//-----------------------------------------------------------------------------------
void main (void)
{
   WDTCN = 0xde;                          // disable watchdog timer
   WDTCN = 0xad;

   SYSCLK_Init ();                        // initialize SYSCLK

   PORT_Init ();

   EMIF_Init ();                          // Storing ADC samples in SRAM on the
                                          // target board.
   SFRPAGE = CONFIG_PAGE;

   UART0_Init ();                         // initialize UART0

   Timer3_Init (SYSCLK/12/SAMP_RATE/2);        // Init Timer3 for 100ksps sample rate

   ADC_Init ();                          // configure ADC0 and ADC1 for single
                                          // measurement.

   while(1)
```

```
   {
   DMA0_Init ();                          // Configure DMA to move NUM_SAMP samples.


   SFRPAGE = UART0_PAGE;
   printf ("Data Acquisition in progress...\n");

   SFRPAGE = DMA0_PAGE;                   // Switch to DMA0 Page

   while (!(DMA0CN & 0x40));              // Wait for DMA to obtain and move ADC samples
                                          // by polling DMA0INT bit.

   SFRPAGE = LEGACY_PAGE;
   printf ("Data Acquisition complete.\nPress P3.7 button when ready to receive file.\n");

   while (BUTTON != 0);                   // Wait for user to press P3.7 on the TB.

   SendData();                            // Send data via the UART0.

    }                        // Done.


}

//-----------------------------------------------------------------------------
// PORT_Init
//-----------------------------------------------------------------------------
//
// Configure the Crossbar and GPIO ports
//
void PORT_Init (void)
{
char old_SFRPAGE = SFRPAGE;

   SFRPAGE = CONFIG_PAGE;              // Switch to configuration page


   XBR0    = 0x04;                     // Enable UART0 on crossbar
   XBR1    = 0x00;
   XBR2    = 0x40;                     // Enable crossbar and weak pull-ups
   P0MDOUT |= 0xFF;                    // enable Port0 outputs as push-pull

   SFRPAGE = old_SFRPAGE;              // restore SFRPAGE
}

//-----------------------------------------------------------------------------
// UART0_Init
//-----------------------------------------------------------------------------
//
// Configure the UART0 using Timer1, for <baudrate> and 8-N-1.
//
void UART0_Init (void)
```

```
{
char old_SFRPAGE = SFRPAGE;

   SFRPAGE = UART0_PAGE;               // Switch to UART0 page

   SCON0   = 0x50;                     // SCON: mode 1, 8-bit UART, enable RX
   SSTA0 = 0x15;                       // Timer 2 generates UART0 baud rate

   SFRPAGE = TMR2_PAGE;

   TMR2CN = 0x00;                      // Timer in 16-bit auto-reload up timer
                                       // mode
   TMR2CF = 0x08;                      // SYSCLK is time base; no output;
                                       // up count only
   RCAP2 = - ((long) SYSCLK/BAUDRATE/16);
   TMR2 = RCAP2;
   TR2= 1;

   SFRPAGE = UART0_PAGE;               // Switch to UART0 page

   TI0    = 1;                         // Indicate TX ready

   SFRPAGE = old_SFRPAGE;              // restore SFRPAGE

}

//-----------------------------------------------------------------------------
// SYSCLK_Init
//-----------------------------------------------------------------------------
void SYSCLK_Init (void)
{
   char old_SFRPAGE = SFRPAGE;

   SFRPAGE = CONFIG_PAGE;              // Switch to Configuration Page

   OSCICN = 0xC0;

   CLKSEL = 0x00;

   SFRPAGE = old_SFRPAGE;              // restore SFRPAGE
}

//-----------------------------------------------------------------------------
// ADC0_Init
//-----------------------------------------------------------------------------
void ADC_Init (void)
{
   char old_SFRPAGE = SFRPAGE;
   int i;

   SFRPAGE = ADC0_PAGE;                // Switch to ADC0 Page
```

```
   ADC0CN = 0x44;                      // ADC Disabled, Timer3 start-of-conversion
                                       // track 16 SAR clocks before data conversion
                                       // upon Timer3 OV.  DMA will enable ADC as needed
                                       //

   //REF0CN = 0x03;                      // turn on bias generator and internal reference.
   REF0CN = 0x02;                      // turn on bias generator and external reference.

   for(i=0;i<10000;i++);               // Wait for Vref to settle (large cap used on target
board)

   AMX0SL = 0x00;                      // Single-ended mode

   ADC0CF = (2) << 4;    // Select SAR clock frequency =~ 25MHz


   SFRPAGE = ADC1_PAGE;                // Switch to ADC0 Page

   ADC1CN = 0x44;                      // ADC Disabled, Timer3 start-of-conversion
                                       // track 16 SAR clocks before data conversion
                                       // upon Timer3 OV.  DMA will enable ADC as needed
                                       //
   //REF1CN = 0x03;                      // turn on bias generator and internal reference.
   REF1CN = 0x02;                      // turn on bias generator and external reference.

   for(i=0;i<10000;i++);               // Wait for Vref to settle (large cap used on target
board)

   ADC1CF = (2) << 4;

   SFRPAGE = old_SFRPAGE;              // restore SFRPAGE
}



//-----------------------------------------------------------------------------
// DMA0_Init
//-----------------------------------------------------------------------------
void DMA0_Init (void)
{
   char old_SFRPAGE = SFRPAGE;

   SFRPAGE = DMA0_PAGE;                // Switch to DMA0 Page

   DMA0CN = 0x00;                      // Disable DMA interface

   DMA0DA = XRAM_START_ADD;            // Starting Point for XRAM addressing

   DMA0CT = NUM_SAMPLES;               // Get NUM_SAMPLES samples

   DMA0IPT = 0x00;                     // Start writing at location 0
```

```
   // Push instructions onto stack in order they will be executed
   DMA0IDT = DMA0_GET_ADC01;            // DMA to move ADC0 data.
   //DMA0IDT = DMA0_GET_ADC1;            // DMA to move ADC1 data.
   DMA0IDT = DMA0_END_OF_OP;

   DMA0BND = 0x00;                      // Begin instruction executions at address 0
   DMA0CN = 0xA0;                       // Mode 1 Operations, Begin Executing DMA Ops
                                        // (which will start ADC0)

   SFRPAGE = old_SFRPAGE;               // restore SFRPAGE
}

//-----------------------------------------------------------------------------
// Timer3_Init
//-----------------------------------------------------------------------------
//
// Configure Timer3 to auto-reload and generate ADC sample rate
// specified by <counts> using SYSCLK as its time base.
//
void Timer3_Init (int counts)
{
   char old_SFRPAGE = SFRPAGE;

   SFRPAGE = TMR3_PAGE;                 // Switch to Timer 3 page

   TMR3CN = 0x00;                       // Stop Timer3; Clear TF3;
   TMR3CF = 0x00;                       // use SYSCLK as timebase
   RCAP3   = -counts;                   // Init reload values
   TMR3    = 0xffff;                    // set to reload immediately
   TR3 = 1;                             // start Timer3

   SFRPAGE = old_SFRPAGE;               // restore SFRPAGE
}

//-----------------------------------------------------------------------------
// EMIF_Init
//-----------------------------------------------------------------------------
//
// Configure the external memory interface to use upper port pins in
// non-multiplexed mode to a mixed on-chip/off-chip configuration without
// Bank Select.
//
void EMIF_Init (void)
{
   char SFRPAGE_SAVE = SFRPAGE;         // Save Current SFR page

   SFRPAGE = EMI0_PAGE;                 // Save SFR_PAGE
   EMI0CF = 0x00;                       // upper ports; non-muxed mode;
                                        // on chip XRAM only
   EMI0TC = 0x45;                       // timing (7-cycle MOVX)

   SFRPAGE = CONFIG_PAGE;
```

```
   SFRPAGE = SFRPAGE_SAVE;             // restore SFR_PAGE
}

//-----------------------------------------------------------------------------
// SendData
//-----------------------------------------------------------------------------
//
//Send data out UART0
//
void SendData(void)
{
   unsigned int i;
   char old_SFRPAGE = SFRPAGE;
   SFRPAGE = UART0_PAGE;               // Switch to UART0 page

   read_ptr = XRAM_START_ADD;          // Set pointer to beginning of data

   for (i=0;i<2*NUM_SAMPLES;i++)
   {
   printf ("%u",*read_ptr);          // Send data as unsigned integers
   read_ptr++;
   }

   SFRPAGE = old_SFRPAGE;

}//End
```