NYQUIST-RATE SWITCHED-CAPACITOR ANALOG-TO-DIGITAL CONVERTERS

A Dissertation

by

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ABSTRACT

The miniaturization and digitization of modern microelectronic systems have made Analog-to-Digital converters (ADC) key building components in many applications. Internet and entertainment technologies demand higher and higher performance from the hardware components in many communication and multimedia systems, but at the same time increased mobility demands less and less power consumption. Many applications, such as instrumentation, video, radar and communications, require very high accuracy and speed and with resolutions up to 16 bits and sampling rates in the 100s of MHz, pipelined ADCs are very suitable for such purposes. Resolutions above 10 bits often require very high power consumption and silicon area if no error correction technique is employed. Calibration relaxes the accuracy requirement of the individual building blocks of the ADC and enables power and area savings. Digital calibration is preferred over analog calibration due to higher robustness and accuracy. Furthermore, the microprocessors that process the digital information from the ADCs have constantly reduced cost and power consumption and improved performance due to technology scaling and innovative microprocessor architectures.

The work in this dissertation presents a novel digital background calibration technique for high-speed, high-resolution pipelined ADCs. The technique is implemented in a 14 bit, 100 MS/s pipelined ADC fabricated in Taiwan Semiconductor Manufacturing Company (TSMC) 0.13μm Complementary Metal Oxide Semiconductor (CMOS)

digital technology. The prototype ADC achieves better than 11.5 bits linearity at 100 MS/s and achieves a best-in-class figure of merit of 360 fJ/conversion-step. The core ADC has a power consumption of 105 mW and occupies an active area of 1.25 mm^2.

The work in this dissertation also presents a low-power, 8-bit algorithmic ADC. This ADC reduces power consumption at system level by minimizing voltage reference generation and ADC input capacitance. This ADC is implemented in International Business Machines Corporation (IBM) 90nm digital CMOS technology and achieves around 7.5 bits linearity at 0.25 MS/s with a power consumption of 300 µW and an active area of 0.27 mm^2.

To my dear parents, sister and niece.

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CHAPTER I

INTRODUCTION

1.1 Motivation and Goals

CMOS technologies continue to scale down and digital performance is increased at a lower cost. Consequently, more and more signal processing is performed in digital domain for increased robustness and reduced power consumption. This requires the use of Analog-to-Digital Converters (ADC) to convert the analog information into digital for Digital-Signal-Processing (DSP). Fig. 1.1 shows different ADC architectures and their respective applications, resolution and speed.

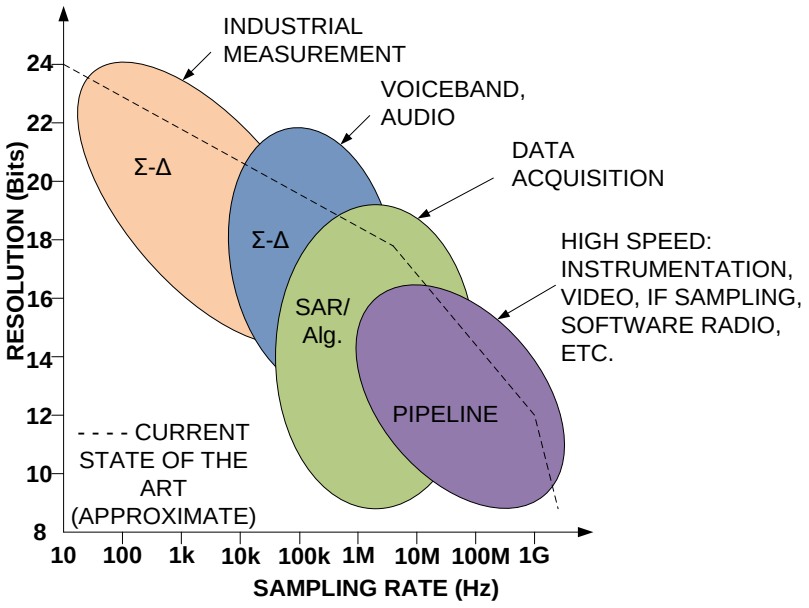


Fig. 1.1 ADC architectures, applications, resolution, and sampling rates.

For many applications that require both high-speed and high-resolution ADCs, such as instrumentation, video, radar and communications, pipelined ADCs are the ideal choice. An application example of a pipelined ADC is shown in Fig. 1.1, which shows a simplified diagram of a generic software radio receiver and transmitter.

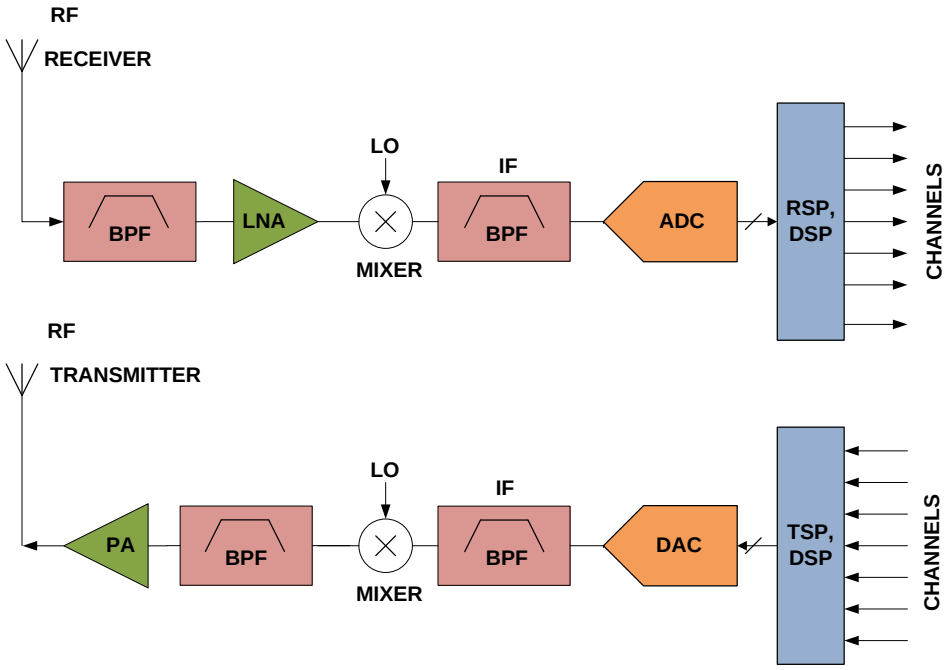


Fig. 1.2 Generic IF-sampling wideband software radio receiver and transmitter.

An essential feature of software radio is that the entire bandwidth containing many channels is digitized directly by the ADC, rather than digitizing each channel separately in the receiver. The channel-filtering, tuning, and separation are performed digitally in the receive-signal processor (RSP) by a high-performance DSP. Digitizing the frequency

band at a relatively high intermediate frequency (IF) eliminates several stages of down-conversion. This leads to a lower-cost, more flexible solution in which most of the signal processing is performed digitally, rather than in the more complex analog circuitry associated with standard analog superheterodyne radio receivers. In addition, various air standards (GSM, CDMA, etc.) can be processed by the same hardware simply by making appropriate changes in the software.

The ADC requirements for the receiver are determined by the particular air standards the receiver must process. The frequencies in the bandwidth presented to the ADC consist of the desired signals as well as large-amplitude interferers, commonly referred to as blockers. The ADC should not generate intermodulation products due to the blockers, because these unwanted products can mask smaller desired signals. The ratio of the largest expected blocker to the smallest expected signal basically determines the required spurious-free dynamic range (SFDR). In addition to high SFDR, the ADC must have a signal-to-noise ratio (SNR) compatible with the required receiver sensitivity.

The high performance requirements for many applications create great design challenges for the ADC. For very high resolutions, it may not be feasible, or too costly to design an ADC which is inherently accurate to the required resolution. This work focuses on correcting for errors caused by the non-ideal ADC components in digital domain by post-processing the digital output. A novel digital background calibration technique for pipelined ADCs [1] is presented in this dissertation. Calibration greatly relaxes the

analog performance requirements and enables power and silicon area savings. The high performance and robustness of DSPs of modern CMOS technologies make this hybrid solution very attractive.

Although digital performance continues to improve and many types of errors can be corrected for with post-processing of the digital ADC output, analog performance is still very important. The scaling of CMOS technologies impose several difficulties for analog design, such as lower supply voltage and the corresponding lower signal swing and reduced SNR, lower device gain and increased non-linearity. Errors caused by component non-linearity are especially difficult to correct for with post-processing and this work also includes several techniques to reduce the effect of component non-linearity in analog domain while maintain a low power and area consumption.

For applications that do not require a high conversion rate, a pipeline ADC may not be the best choice. This work also presents an algorithmic ADC where power and area is greatly reduced by re-using the basic hardware and performing the analog to digital conversion in a cyclic fashion [2]. Such an ADC would be a good choice for a sensing or biomedical application, where high speed is often not required. The algorithmic ADC presented in this work also reduces power consumption at system level by minimizing voltage reference generation and ADC input capacitance.

1.2 Organization

The algorithmic ADC mentioned in section 1.1 is presented in Chapter II. The architecture and system level considerations are described in detail and the architecture is compared with other ADCs. The transistor level implementation details and the design choices of the ADC are described in detail. Experimental results from the prototype ADC built in 90nm CMOS technology are presented and discussed.

Chapter III presents the pipelined ADC and digital background calibration technique mentioned in section 1.1. The calibration technique is described from an intuitive perspective and supported with mathematical models and equations. The technique is compared with previously reported calibration techniques. Simulation results are presented to show the effectiveness of the proposed technique. The transistor level implementation details of the ADC building blocks are described in detail. Layout considerations, such as clock routing and synchronization, for a high-speed, high-resolution pipelined ADC are also described. The ADC characterization setup is described and board-level considerations are presented. Experimental results from the prototype ADC built in 0.13 µm CMOS technology are presented and discussed. The performance of the ADC is compared with previously published ADCs.

The dissertation is concluded in Chapter IV.

CHAPTER II

8-BIT ALGORITHMIC ADC OPERATING WITH A SINGLE REFERENCE VOLTAGE FOR PLL-BASED CHEMICAL SENSING APPLICATIONS

2.1 Introduction

Algorithmic Analog-to-Digital Converters (ADCs) are commonly used in battery-powered integrated sensing and biomedical systems where low-power, cost-effectiveness and robustness are crucial. These types of ADCs achieve a medium resolution and low speed as a trade-off for low power and area since they re-use the basic hardware. Successive-approximation register (SAR) ADCs are also popular in low power sensor systems [3-4], however they generally require significant capacitive area for matching requirements and typically present a larger input capacitance, demanding more power from the preamplifier, which become important at the system level because the preceding stage and voltage reference have to drive this capacitive load. Although ΣΔ modulators show excellent performance [5] and could be an alternative, high over-sampling ratios are required to meet the specifications resulting in clock speeds in the range of MHz and presenting significant input capacitance and increased hardware complexity.

This chapter presents a robust, compact, low complexity and low power switched-capacitor algorithmic ADC for sensing systems. The ADC also presents a small input

capacitance, due to only one sampling capacitor connected to its input and the comparator is not connected to the input during any mode of operation. Furthermore, the ADC requires only one reference voltage for a single-ended implementation which simplifies reference generation and routing and enables power savings at system level. The reference voltage is applied through capacitors and an array of switches arranged such that they implement inverting and non-inverting operations, while a single reference voltage is employed. Typically a bandgap reference generator with output buffer is required for reference generation [6]. The speed and accuracy requirement for this buffer is similar to that of the amplifier of the ADC itself and therefore a significant amount of power is required for the voltage reference circuitry. For expensive differential references, usually two single-ended buffers or a fully-differential buffer is required. For a fully-differential implementation, a Common-Mode-Feedback (CMFB) circuit is required which may consume up to half of the power of the main amplifier [7]. A single-ended implementation enables power savings in the reference generation circuitry, while a fully-differential version of the proposed ADC requires differential references. However, a fully-differential implementation would present better Power-Supply-Rejection-Ratio (PSRR), larger ADC input range for a given power supply voltage and less sensitivity to charge injection and clock feed-through. However, for less than 10-bits resolution, usually these issues are not very critical. Furthermore, in this application, see Fig. 2.1, a fully-differential implementation would also require a single-ended to differential input driver, which would add to the total power and area consumption.

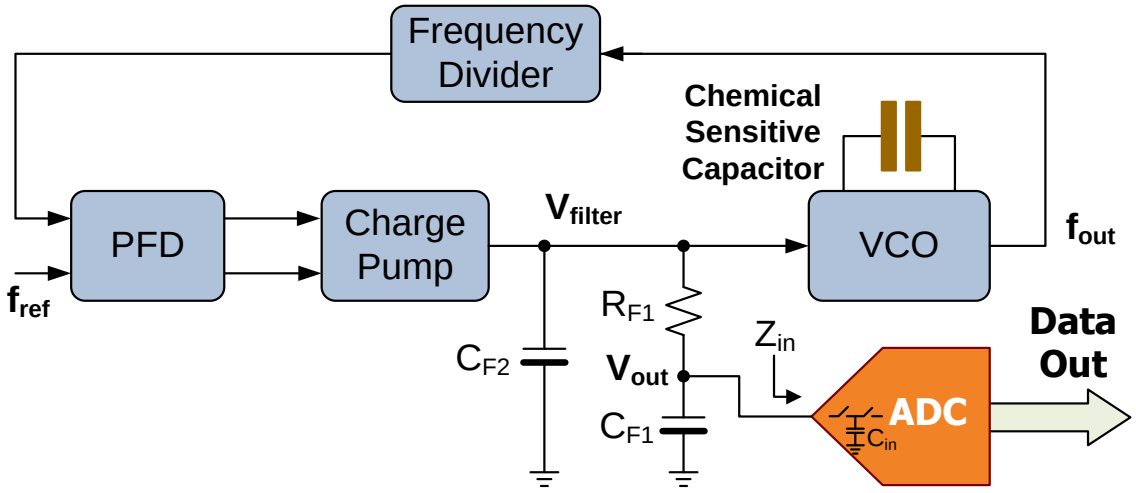


Fig. 2.1 ADC Application: PLL based dielectric constant sensor.

The ADC is an integral part of a System-On-Chip PLL based sensor [8], as shown in Fig. 2.1. The on-chip sensor detects the dielectric constant of organic chemicals. The dielectric constant of these chemicals is measured using the oscillation frequency shift of an LC voltage controlled oscillator (VCO) upon the change of the tank capacitance when exposed to the chemical to be characterized. To make the system self-sustained, the VCO is embedded inside a frequency synthesizer to convert the frequency shift into voltage that can be digitized using an on-chip ADC. Power consumption at the system level must be minimized hence the single-ended to differential conversion and use of fully-differential reference voltages are avoided; the power consumption of the PLL is 14.9mW hence < 500µW is enough for this application. The ADC input capacitance, C_{in}, should be minimized because this capacitance is in parallel with the filter capacitor C_{F1} (see Fig. 2.1), which causes a reading error C_{in}/C_{F1}. This error should be less than the

ADC effective resolution; < 0.25%. A brief overview of previous works on algorithmic ADCs is presented next.

2.1.1 Previous Work on Algorithmic ADCs

A number of algorithmic ADCs have been reported in the literature. Although the proposed ADCs is not capacitor ratio mismatch insensitive, it uses less clock-phases for conversion than such algorithmic ADCs [9-11] and can therefore operate at a higher conversion rate. Although the ADC in [12] only uses two clock-phases per converted bit, it requires a two-stage implementation which increases the area and complexity of the ADC. A more detailed comparison with [13-14] follows. [13-14] each presents an algorithmic ADC which operates on two clock phases and uses a single amplifier and comparator. The ADC in [13] uses four nominally equal capacitors, which will occupy more area than the three capacitors required for the ADC presented in this chapter and the ADC presented in [14]. For all ADCs, it is assumed that the capacitance value is based on either sampled thermal noise requirement, or matching requirement, whichever requires a larger capacitance value. In [13] one digital output bit is resolved in each clock cycle, same as for the ADC presented in this chapter, while in [14] two output bits are resolved in each clock cycle. It should be noted that the architecture of the ADC in [14] is more sensitive to mismatch than the ADC in [13] and in this chapter, because of the manner of switching the capacitors proposed in [14]. In [13] and [14] the comparator must be switched between the ADC input and the output of the amplifier, which requires

additional switches and increases the effective ADC input capacitance compared to the ADC in this chapter, where the comparator is always connected to the amplifier output. For the ADCs in [13-14] as well as for the proposed ADC, the input range is the same; [$-V_{ref}$ to $+V_{ref}$] around the common-mode level of the ADC input. The ADCs in [13-14] require both $+V_{ref}$ and $-V_{ref}$ for a single-ended implementation, while the proposed ADC requires only $+V_{ref}$ to be available.

The following analysis compares the power consumption of the proposed ADC with the ADCs in [13-14]. The comparison will be based on the same effective input sampling frequency and the power consumption will be analyzed. Power consumption can be related to the transconductance of the amplifier, which in turn depend on the required accuracy in a given settling time for a given load condition. For the same effective input sampling frequency, the ADC in this chapter, as well as the ADC in [13], will only have half the available settling time compared to [13], but the ADCs have different feedback factors and loading conditions which will affect the requirement for the transconductance of the amplifier. For comparison purposes, it is assumed that the dominant pole of each amplifier is at the output of the amplifier. The expression for the transconductance of the amplifier (2.), assumes a settling error of ½ LSB (Least-Significant-Bit) but the analysis can be extended to a settling error of any fraction of LSB.

$$g_m = \frac{1}{\beta} \frac{\ln\left(2^{N+1}\right)}{2\pi \cdot t_{settling}} C_{Load,eff} \tag{2.1}$$

Where $C_{Load,eff}$ is the effective load of the amplifier, β the feedback factor of the amplifier, N the resolution of the ADC and $t_{settling}$ the available settling time. To compare the different ADCs, their individual transconductance in each clock phase will be expressed as a multiple of a nominal transconductance, expressed in (2.2), where C is the nominal capacitance value. The comparison is shown in Table 2.1 below, where g_{m13} is the required transconductance for the amplifier in [13] etc, and where it has been taken into account the different available settling time for the amplifier in [12], and where the input capacitance of the comparator is expressed as a fraction, γ, of C. For simplicity, the expressions in Table 2.1 ignore the presence of amplifier parasitic input capacitance.

$$g_{m,nom} = \frac{\ln\left(2^{N+1}\right)}{2\pi \cdot t_{settling}} C \tag{2.2}$$

Table 2.1 Transconductance comparison.

	Clock phase ϕ_1	Clock phase ϕ_2
g_{m13}	$g_{m,nom}*(3+ 2\gamma)$	$g_{m,nom}*5$
g_{m14}	$g_{m,nom}*(1.5+ \gamma)$	$g_{m,nom}*(1.5+ \gamma)$
$g_{m,\ this\ ADC}$	$g_{m,nom}$	$g_{m,nom}*(2+3\gamma)$

It can be noted in Table 2.1 that the amplifier in [13] will require the largest transconductance in both clock phases. If the input capacitance of the comparator γ is only a small fraction of C (which is the case if the input capacitance of the comparator is only gate parasitic capacitance), then the transconductance requirement for this ADC is about 1.33 times larger than of [14] in clock phase ϕ_2. However, the proposed ADC can enable power savings at the system level in the reference generation circuitry. Furthermore, the amplifier in this ADC requires 1.5 times less transconductance in clock phase ϕ_1 than the amplifier in [14], which enables the amplifier to use less bias current in this phase to save power, and the average transconductance would be almost the same for both ADCs when looking over a whole clock cycle. Such a power saving technique however was not utilized in the implementation of the proposed ADC.

2.2 ADC Architecture

This section presents the proposed switched-capacitor algorithmic ADC. It can be noted that many ADCs require a front-end Sample-and-Hold circuit, unlike the proposed ADC

which require the input to be available only during the sampling phase. The input sample is then retained in the internal ADC conversion loop.

2.2.1 Description of Proposed Algorithmic ADC

The block diagram of the single-ended algorithmic ADC is Fig. 2.2. The ADC operates with two non-overlapping clock phases, ϕ_1 and ϕ_2, see Fig. 2.3, and uses N clock cycles to obtain an N-bit digital output. The conversion process begins with the sampling clock phase ϕ_s, where the input is sampled onto capacitor C_1, the amplifier is reset and any offset voltage present in the amplifier is sampled and stored onto capacitor C_3. The C_3 capacitor is not required for the main operation of the ADC but it improves the ADC resolution by cancelling the offset of the amplifier. All capacitors are nominally equal and set from matching requirement, whose minimum value is usually suggested by the silicon foundry.

Charge sharing occurs between the C_3 capacitor and the input parasitic capacitance of the positive node of the amplifier, C_p, then C_3 should therefore be scaled based on the estimated value of C_p. Contrary to other architectures, the comparator is always connected to the output of the amplifier and no switches are therefore required at its input node. All decisions are taken at the switched-capacitor amplifier's output.

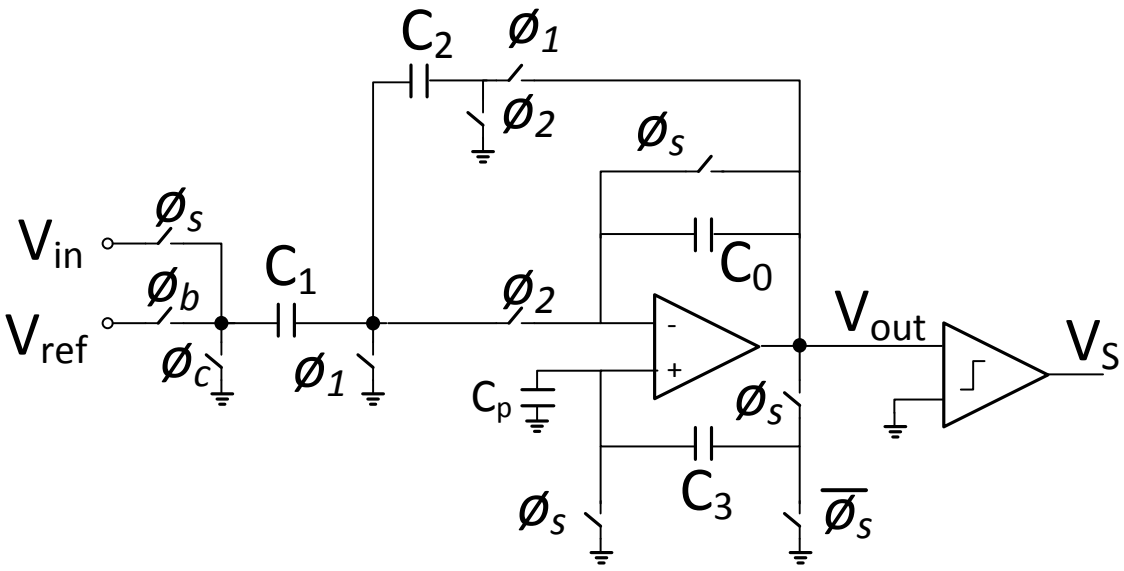


Fig. 2.2 ADC block diagram.

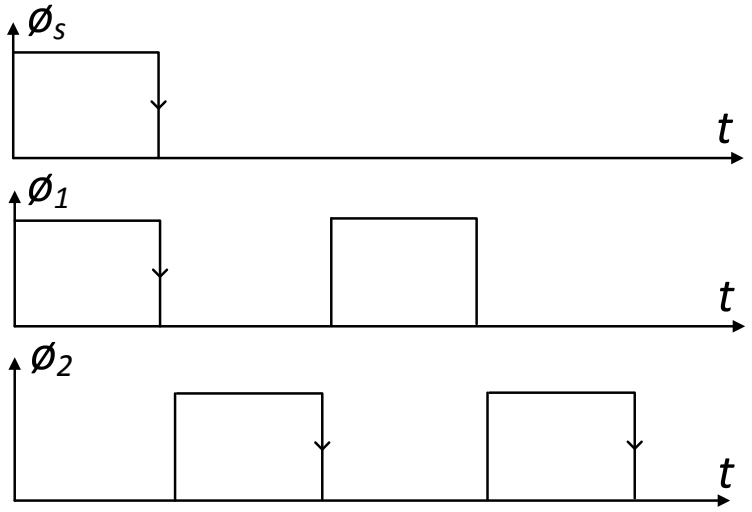


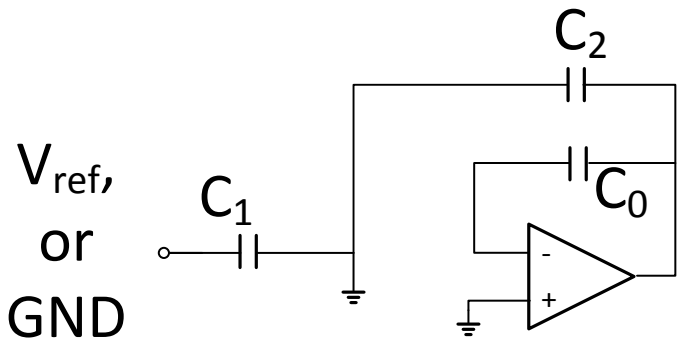
Fig. 2.3 Clocks used in the algorithmic ADC.

The control clocks, ϕ_b and ϕ_c are generated according to (2.3). These conditional clock phases should be non-overlapping as well and be made logic low during the ϕ_s phase.

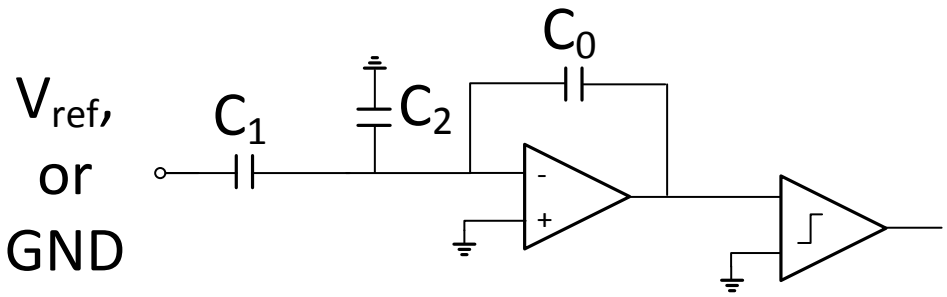
$$\begin{aligned} \phi_b &= \phi_1 V_s + \phi_2 \overline{V_S} \\ \phi_c &= \phi_1 \overline{V_S} + \phi_2 \overline{V_S} \end{aligned} \tag{2.3}$$

Disregarding the operation of capacitor C_3, during the conversion process there are two general modes of operation for this circuit, shown in Fig. 2.4 a) and b). During the first mode of operation, clock phase ϕ_1, the previous residue is sampled onto capacitor C_2. The purpose of this clock phase is to pre-charge C_2 to be able to multiply the residue by a factor of two during the next clock phase. If the output bit during the previous conversion cycle was determined to be logic high, then the C_1 capacitor is connected to GND during this clock phase. If the previous output bit was logic low then C_1 is connected to V_{ref}.

During the second mode of operation, clock phase ϕ_2, the new output is determined. If ground was connected to C_1 during the previous ϕ_1 clock phase, then V_{ref} is connected to C_1 during this clock phase, and vice versa. This process will add or subtract V_{ref} from the output. The comparator compares this output with GND and makes a decision; its logic output V_s is then used to update the ϕ_b and ϕ_c clocks. This process continues until all N bits have been determined.



a)



b)

Fig. 2.4 a) Clock phase ϕ_1 of algorithmic ADC. b) Clock phase ϕ_2 of algorithmic ADC.

During clock phase ϕ_1, the amplifier feedback factor is unity while the load capacitance is C_2=C (the unit capacitance used). During clock phase ϕ_2, the amplifier feedback factor is 1/3 while the amplifier's load capacitance is $C_0(C_1+C_2)/(C_1+C_2+C_0)$=2/3C, if the comparator's input capacitance is considered smaller than the integrating capacitors. Therefore, the amplifier's transconductance is computed from clock phase ϕ_2, since this is the most demanding clock phase.

2.2.2 Effects of Non-Idealities

Assuming that the amplifier is able to settle within the time allocated to each clock phase, the output of the first cycle can be expressed as in (2.4), where A is the amplifier DC gain, and V_{offset} the amplifier offset. This output is compared with GND to determine the MSB bit.

$$V_{out}[0] = \frac{C_1}{C_0 + \frac{C_{tot}}{A}} V_{in} + \frac{V_{offset}}{A+1}\left(1 + \frac{AC_p}{C_3 + C_p}\right)\frac{C_{tot}}{C_0 + \frac{C_{tot}}{A}} \qquad (2.4)$$

where $C_{tot}=C_0+C_1+C_2$

This output voltage is sampled by C_2 during the following clock phase, to complete the multiply-by-two operation in the following clock cycle. The sign of (2.4) determines if C_1 will be connected to V_{ref} or GND during the following clock phase. The output of cycle n+1 can be expressed as in (2.5) and is compared with GND to determine bit n+1.

$$V_{out}[n] = \frac{\left(C_0 + C_2 + \frac{C_0}{A}\right)V_{out}[n-1] - D_{n-1}C_1V_{ref}}{C_0 + \frac{C_{tot}}{A}} + \frac{V_{offset}}{A+1}\left(1 + \frac{AC_p}{C_3 + C_p}\right)\frac{C_1 + C_2}{C_0 + \frac{C_{tot}}{A}} \tag{2.5}$$

As observed in (2.4) and (2.5), capacitor mismatch, finite gain as well as amplifier offset will cause errors in the output. These non-idealities cause distortion in the output power spectrum and reduce the ADC resolution. From (2.4), it is noticed that the minimum amplifier DC gain and the capacitor mismatch requirement are given by (2.6), to have an error in the output voltage less than ½ LSB.

$$A > 3 \cdot 2^{N+1}$$
$$\left|\frac{C_1}{C_0} - 1\right| < 2^{N+1} \tag{2.6}$$

The conditions expressed in (2.6) are highly technology and layout dependent. The amplifier offset is practically cancelled if $C_3 >> C_p$, where C_p is the parasitic capacitance at the amplifier input. If the amplifier output is used as sampling ground in the ϕ_s phase, and with a few extra switches, the amplifier offset term would disappear from the

amplifier output in the first output phase, and the C_3 capacitor may not be necessary depending on the resolution and the amount of offset. However, this could increase the sampling time constant, mainly depending on the amplifier transconductance, g_m. The required amplifier GBW can be calculated from (2.1) and is listed in Table 2.2.

Thermal noise sets the lower limit for the sampling capacitance value. For an N-bit resolution, the required capacitance value can be calculated by setting the switch thermal noise contribution to a fraction (m) of the ideal noise power of the ADC, see (2.7). In (2.7) it is taken into account that there is one kT/C noise contribution in the sampling phase, and another kT/C noise contribution in the hold phase.

$$2\frac{kT}{C} < \frac{1}{m}\frac{V_{FS}^2}{2^{2N}\cdot 12}$$
$$C > \frac{2m\cdot 12kT2^{2N}}{V_{FS}^2} \qquad (2.7)$$

For an 8-bit ADC, (2.7) evaluates to only C≈14fF (with m=2). Matching requirements results in a larger capacitance value and for this prototype, the capacitor values are set at C_0=C_1=C_2=C=3pF. The effect of charge injection from the switches is minimized by utilizing early clocks.

2.2.3 ADC Components

The amplifier used in the ADC design is shown below in Fig. 2.5, which uses Miller frequency compensation. This topology was chosen due to its high DC gain and large output swing since the PLL filter output presents large signal excursions. P-type input stage is chosen to reduce flicker noise due to the input differential pair. The resistors at the source of the NMOS current mirror increase the low-frequency gain of the amplifier; the increment of the impedance at the output of the N-type current mirror reduces the frequency of the dominant pole, which allows reducing the value of the miller capacitor. The resistors also reduce the input-referred flicker noise from the NMOS current mirror.

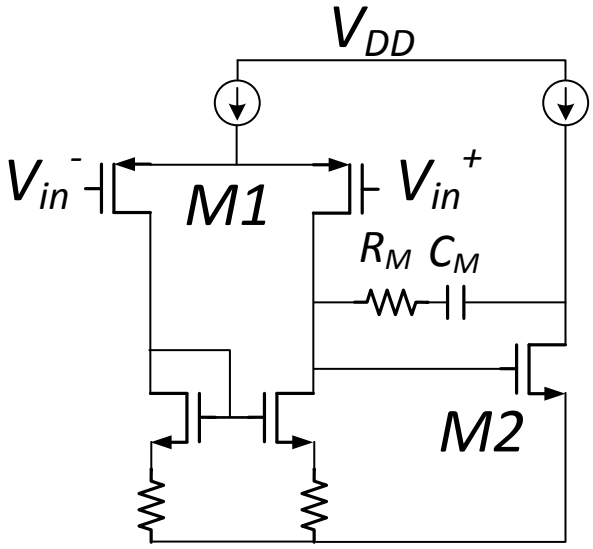


Fig. 2.5 Two-stage Miller Amplifier

The comparator used in the ADC is shown in Fig. 2.6. It is a continuous-time implementation with a high gain two-stage amplifier in open loop to allow a small input to trip the inverter threshold and to reduce the input referred offset and to minimize kickback noise. The input differential pair has a large area to improve matching and reduce the offset. The input-referred noise is dominated by flicker noise from the differential input pair and the NMOS active load in a bandwidth up to the Nyquist frequency. The first stage is resistively terminated to maintain its symmetry to further reduce the input referred offset voltage. The resistors avoid the use of an additional common-mode feedback for the first stage, while maintaining large gain if the resistance values are high. The comparator's second stage is implemented using a conventional 3-current mirror amplifier whose output drives a CMOS inverter. Since the speed of the circuit is not an issue, the un-clocked solution was found to be appropriated.

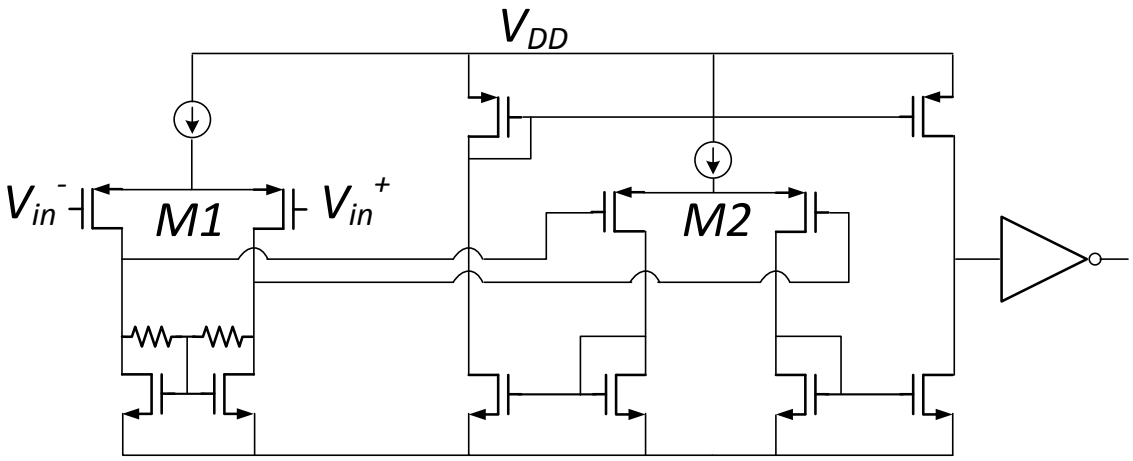


Fig. 2.6 Clock-less comparator architecture.

Amplifier and comparator parameters and performance are provided in Table 2.2. Amplifier DC gain is 63dB for the typical corner, which is equal to the calculated requirement, while the unity-gain frequency is around 16MHz when driving a load capacitance of 2pF, which is higher than the calculated requirement to ensure enough speed. Relatively large dimensions were used to improve the matching of the transistors used for the realization of the differential pair and second amplification stage. Large gate area reduces flicker noise as well.

Table 2.2 Amplifier and comparator performance.

Amplifier	
DC Gain	63 dB (cal. requirement=63dB)
GBW @ C_L=2/3C=2pF	16 MHz (cal. requirement=14.5MHz @ 0.25MS/s)
Phase Margin	80 degrees
Total Input-Referred noise up to Nyquist	6.8μV
(W/L)1;2	30μm /0.7μm; 125μm /4.5μm;
I_{bias}(First/Second stage)	50μA/100μA
Comparator	
DC Gain	46 dB
Max freq. of operation	3.3 MHz
Total Input-Referred noise up to Nyquist	2.3μV
(W/L)1;2	192μm /3μm; 96μm /1μm;
I_{bias}(First/Second stage)	25μA/75μA

The clock-less comparator achieves an open-loop gain of 46dB. It can resolve the sign of the input signal up to a frequency of 3.3 MHz. To reduce its offset voltage a minimum length of 3μm was used in the first stage; the second stage employs L=1μm. Static power consumption is 120μW and it can be reduced drastically for lower speeds. Noise for both the amplifier and comparator is only a fraction of LSB.

2.3 Characterization of the ADC

The ADC was implemented in IBM 90nm digital technology with 1.2V power supply. The chip microphotograph is shown in Fig. 2.7. The active area is 0.27 mm^2. The capacitors are located close to the amplifier to minimize routing and noise coupling. The capacitors are implemented as Metal-Insulator-Metal capacitors (MIM) because of their high linearity. The capacitors use a common-centroid layout pattern for matching purposes with dummy capacitors on the sides. The dummy capacitors make the boundary effects the same for all unit capacitors. Matched transistors and resistors use interdigitization as well as dummy devices in the layout. On-chip decoupling capacitors are used between the power supplies. These decoupling capacitors are implemented with MOS capacitors because of their high density, and placed on both sides of the active circuitry for better compensation.

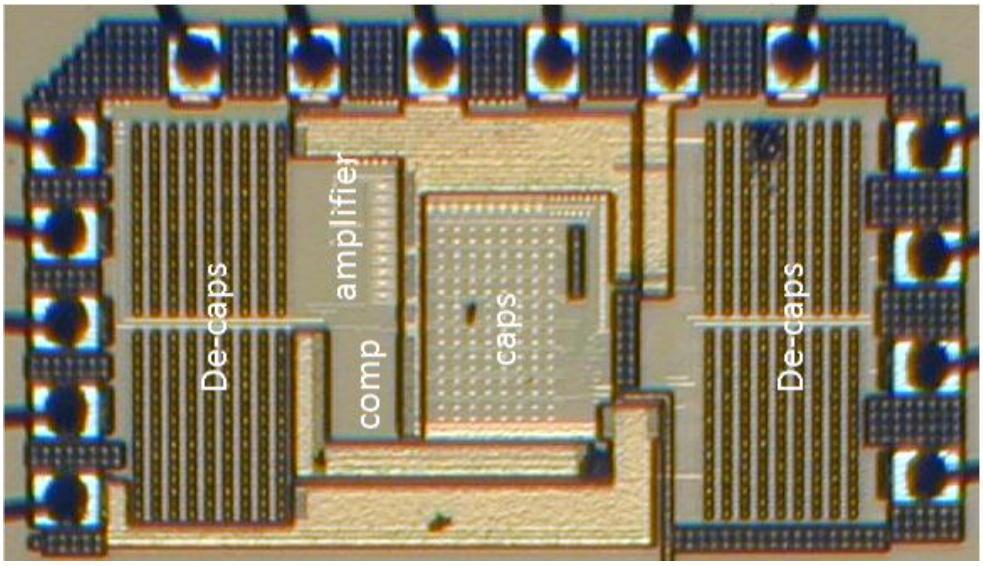


Fig. 2.7 Algorithmic ADC chip microphotograph.

The ADC was characterized using a Printed-Circuit-Board (PCB) and a diagram of the test setup used is shown in Fig. 2.8. A square-wave generator is used generate the clock for the ADC. Due to the low input signal bandwidth, clock jitter does not significantly reduce the effective ADC resolution. The input signal generators however generate large distortion and noise and these effects are difficult to filter out. Therefore, the ADC performance is characterized with a two-tone test by combining two input sine-waves. The power combiner is resistive based and is highly linear. Power supply lines were filtered using off-the-shelf line filters to remove noise and spurious tones and were further regulated using on-board adjustable regulators. The digital output bits were captured with a Logic Analyzer and exported to Matlab for post-processing.

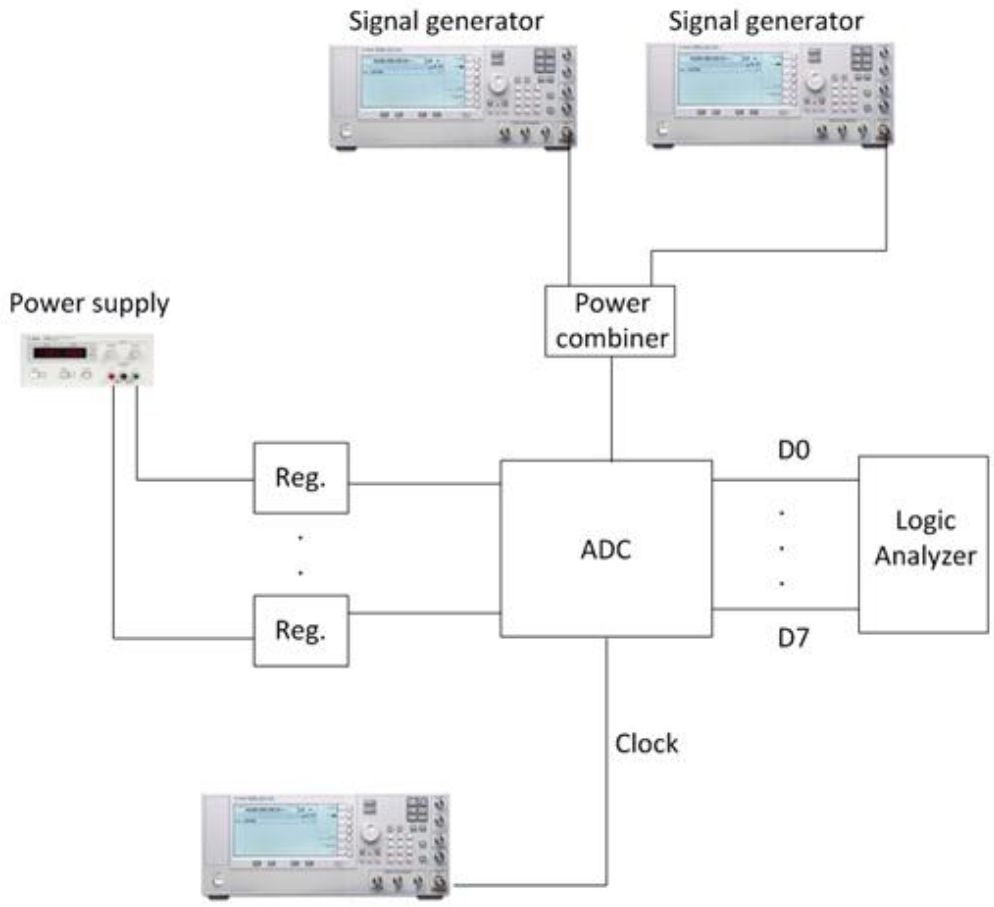


Fig. 2.8 Test setup used for characterization of the ADC.

2.3.1 Experimental Results

This section presents the experimental results and the ADC performance is analyzed and compared with previously published work.

The ADC was implemented in IBM 90-nm technology with 1.2V power supply. The nominal ADC sampling rate is 0.25 MS/s. The measured ADC output power spectrum is shown in Fig. 2.9 for a small input signal to minimize the noise contribution and harmonic distortion of the signal generator itself. Under these conditions, the Signal-to-Noise-Ratio (SNR) was measured to be 49.9 dB when a full-scale signal is considered, which is very close to the ideal value for 8-bits resolution.

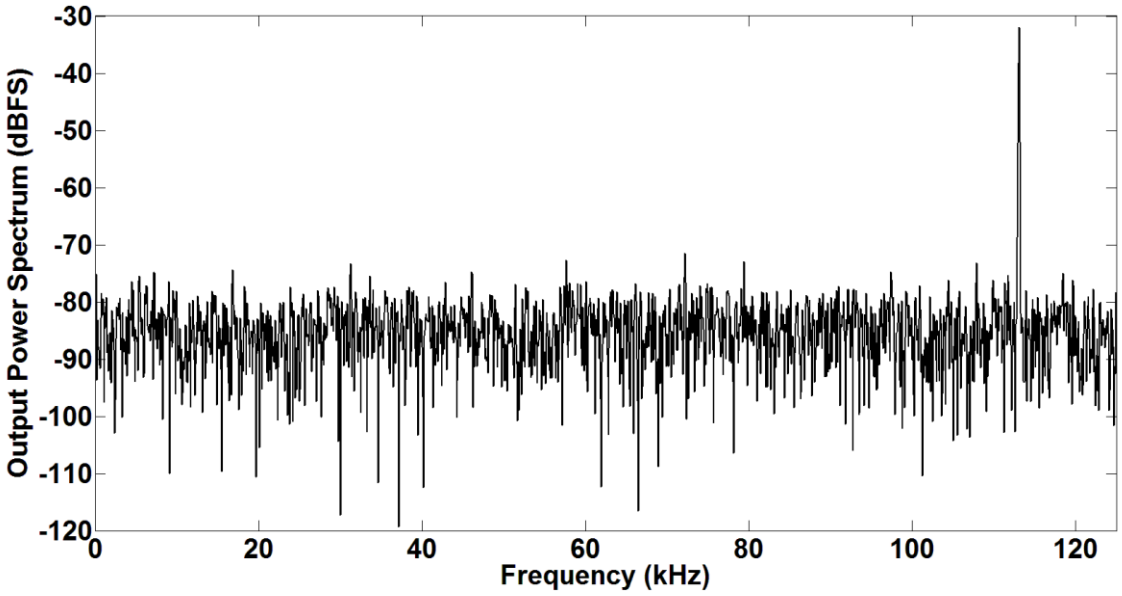


Fig. 2.9 Measured output power spectrum.

The FFT for all the plots in this section are computed by employing the Hanning window, and all post-processing is performed in Matlab.

A two-tone input signal (at 800Hz and 1.1KHz) was applied to the ADC to measure its linearity; the results are shown in Fig. 2.10 for an input power level of P_{in}=-6dBFS. The third-order-intermodulation (IM3) tones are symmetrical around the main tones and are a measure of the ADC linearity. The noise floor in Fig. 2.10 increases by more than 20 dB when compared with the noise floor of Fig. 2.9. This is mainly due to noise contribution of the signal generators themselves.

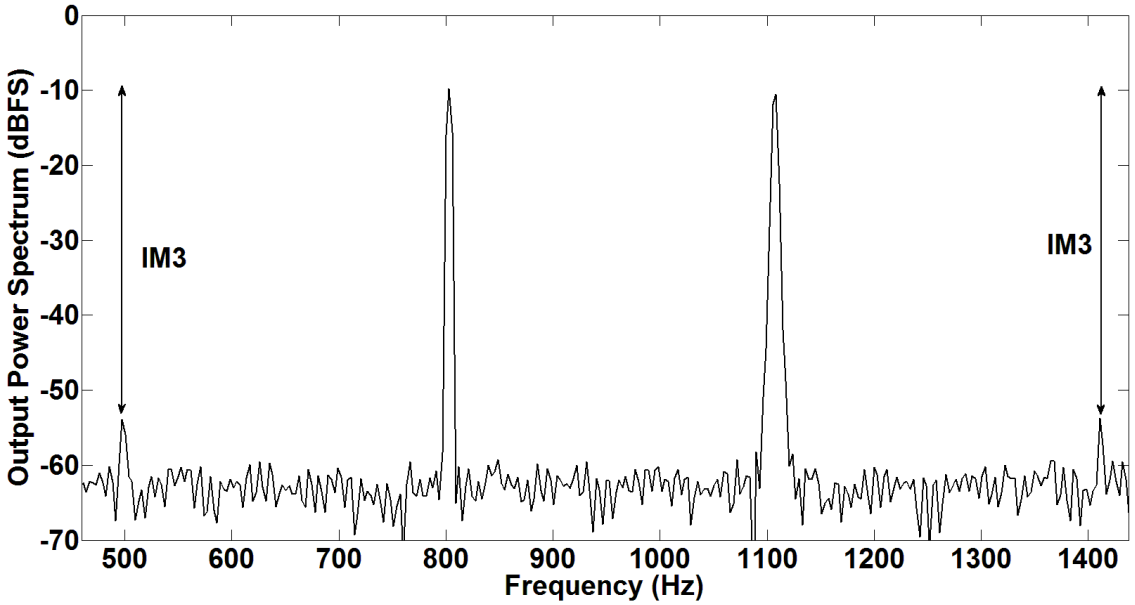


Fig. 2.10 Two-tone test to measure IM3 at P_{in}=-6dBFS.

The measured SNDR as function of the input power is shown in Fig. 2.11. The peak SNDR was measured as 46.7 dB and occurs at P_{in}=-6dBFS, with input tones centered around 1kHz. The Effective-Number-of-Bits (ENOB) is obtained as 7.45 bits, which is

in good agreement with the theoretical ENOBmax=7.5 bits for this input power level. As the combined total input power of the two tones is increased beyond -6dBFS, the ADC input range is exceeded and clipping occurs and the distortion in the ADC output increases.

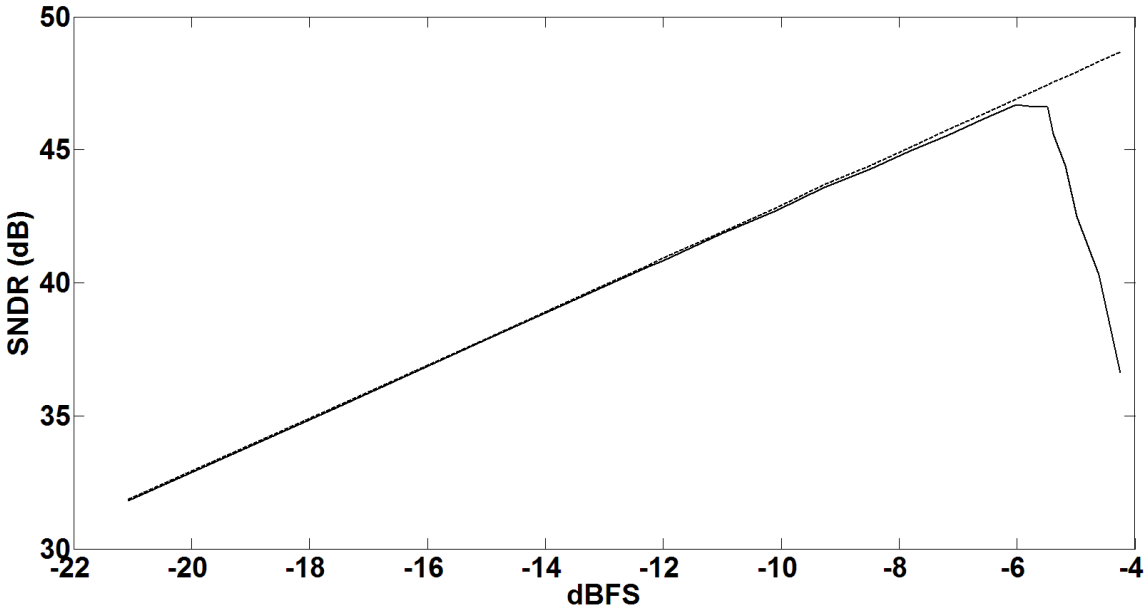


Fig. 2.11 Measured SNDR with two-tone input as function of input power.

The SNDR as a function of the effective input sampling rate is shown in Fig. 2.12. The maximum sampling rate of the ADC is 0.375 MS/s, which corresponds to a clock frequency of 3 MHz, which is close to the simulated maximum frequency of operation of the comparator. The SNDR drops down to 41.5 dB at maximum sampling rate, but stays

above 46.5dB up to 0.25 MS/s. As the clock frequency is increased, the available settling time for the amplifier and sampling network is reduced and this is a reason for increased non-linearity for the ADC. The input sampling network does not use a boot-strapped switch and the on-resistance of the sampling switch is therefore signal dependent and non-linear and the distortion becomes more severe at higher clock frequencies.

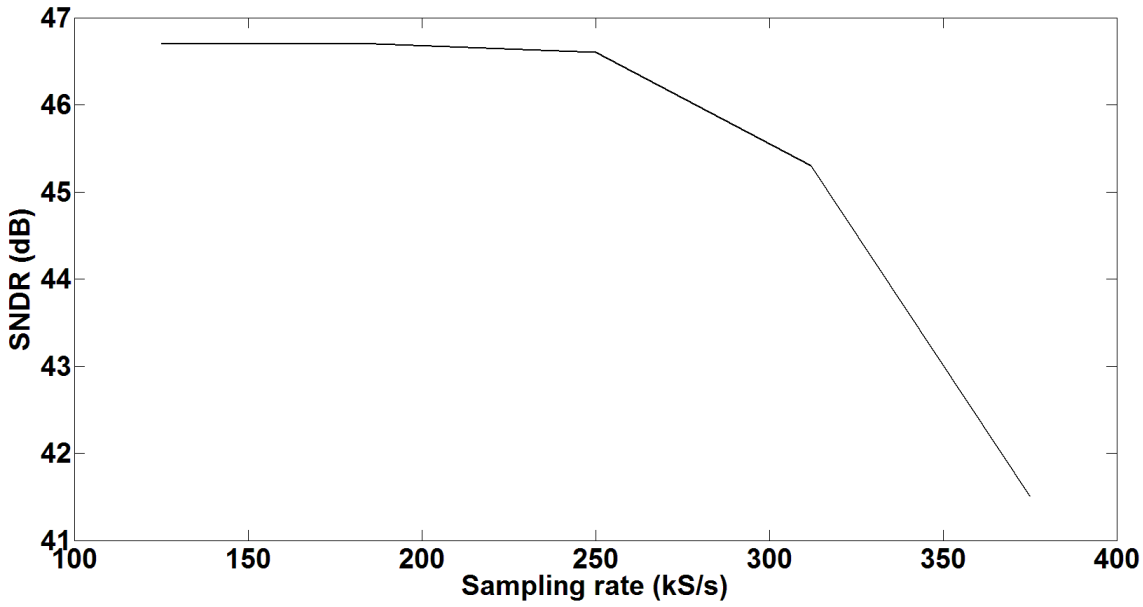


Fig. 2.12 Measured SNDR at P_{in}=-6dBFS as function of sampling rate.

The measured Differential-Non-Linearity (DNL) is shown in Fig. 2.13 and Integral-Non-Linearity (INL) in Fig. 2.14. Both DNL and INL are below 0.6 LSB for the entire ADC

range, which indicates that the ADC has 8-bit resolution. The DNL and INL were measured by applying a slow-moving ramp and obtaining the step response of the ADC.

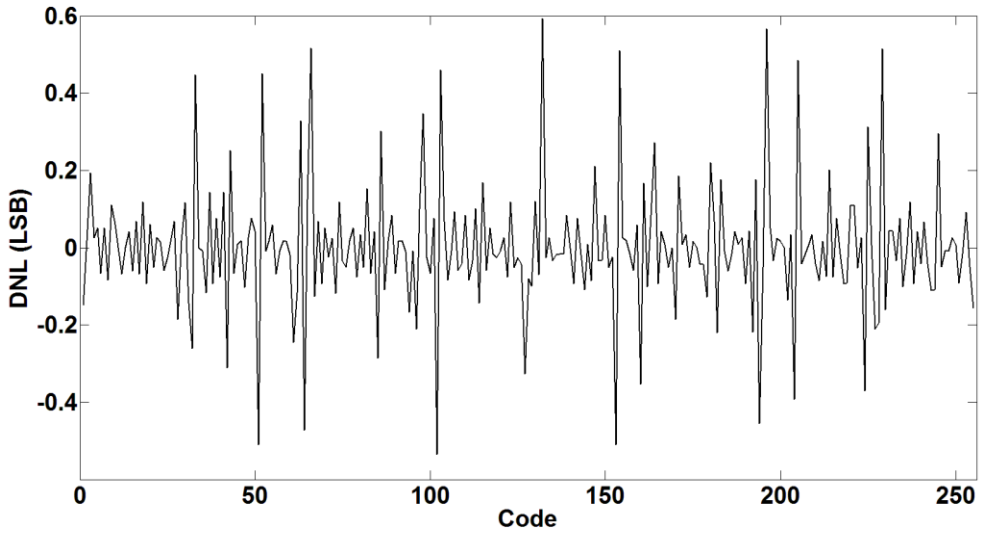


Fig. 2.13 Measured DNL.

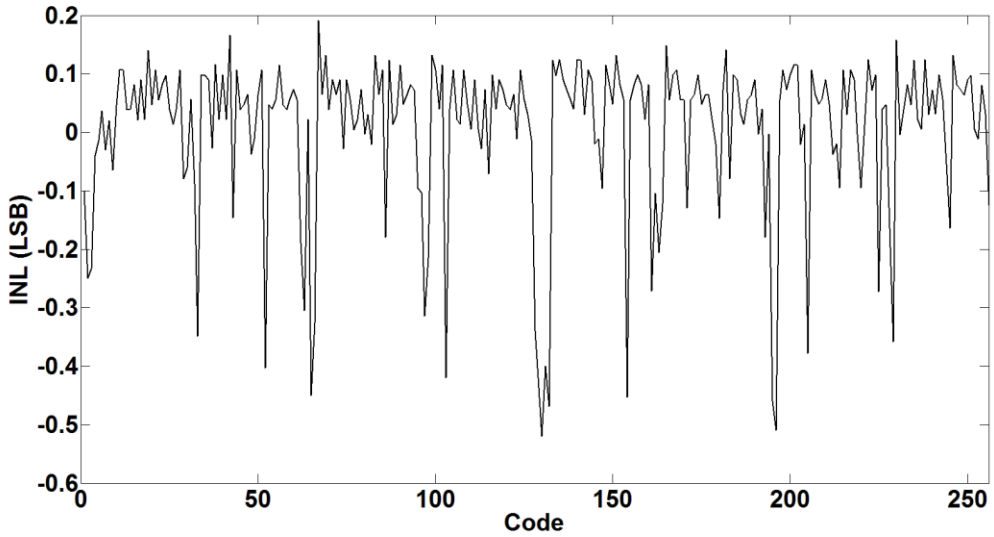


Fig. 2.14 Measured INL.

The ADC's measured results are summarized in Table 2.3 and compared with previously published ADCs in Fig. 2.15. The ADC has a figure of merit of 6.86 pJ/conversion-step. Although the power consumption of the core ADC is average compared with other ADCs, as seen in Fig. 2.15, when the power at system level is considered, this ADC would be very competitive. Furthermore, the power consumption of the core ADC could be further reduced by reducing the size of the capacitors (hence the transconductance of the amplifier could be reduced for the same settling time), they were over-dimensioned for the current resolution. The comparator could possibly also be implemented with a dynamic latch for further reduction in power consumption.

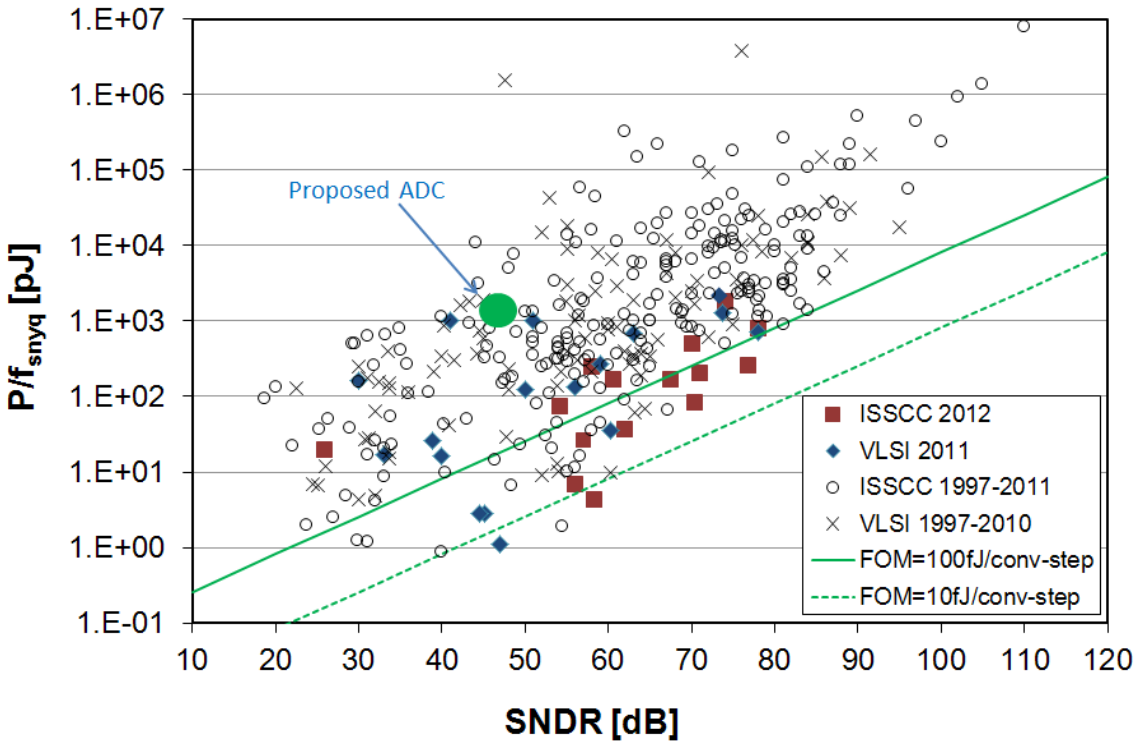


Fig. 2.15 Algorithmic ADC performance comparison.

Table 2.3 Algorithmic ADC measured performance.

Technology	90nm CMOS
Power supply	1.2V
Resolution	8 bits
Sampling rate	0.25 MS/s
Input range	$800mV_{pp}$
SNR at P_{in}=-3dBFS	49.9 dB
SNDR	46.7dB/7.45 bits
ENOB at P_{in}=-6dBFS	7.45 bits
DNL	+0.6/-0.5 LSB
INL	+0.2/-0.5 LSB
Power	300µW
Active area	$0.27mm^2$

2.4 Future Work

The ADC presented in section 2.2 is sensitive to capacitor matching and in order to achieve a high resolution a large capacitive area must be used. The algorithmic ADC presented in this section is insensitive to capacitor mismatch ratio, and therefore presents a smaller capacitive area. The trade-off however is that this algorithmic ADC has a slower conversion speed than the algorithmic ADC present earlier in this chapter.

2.4.1 Description of Proposed Algorithmic ADC

The proposed capacitor mismatch ratio insensitive algorithmic ADC is shown in Fig. 2.16. It uses one amplifier, comparator, three nominally equal capacitors and a number of offset canceling capacitor and switches.

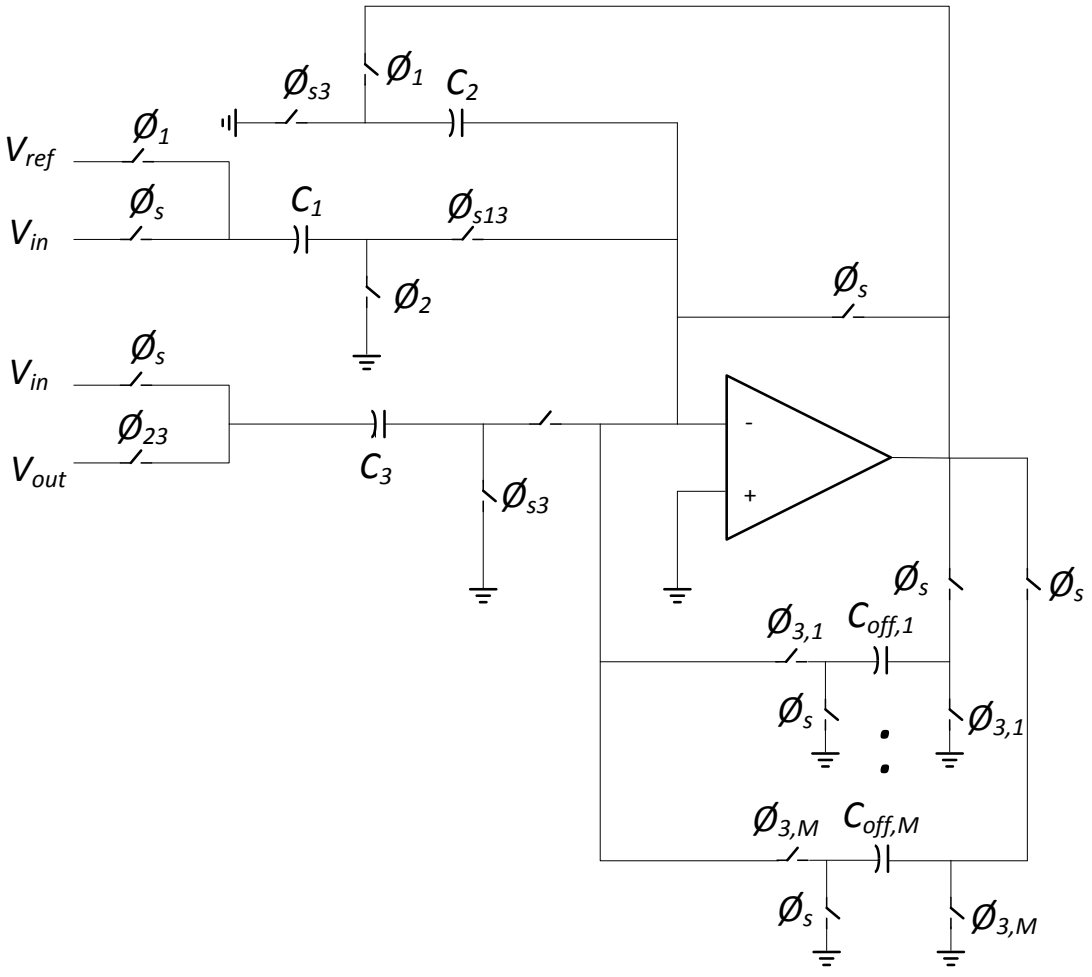


Fig. 2.16 Capacitor mismatch ratio insensitive algorithmic ADC.

The ADC in Fig. 2.16 requires 3·(N-1)+1 clock phases (compared with 2N clock phases for the ADC presented previously in this chapter, and 4·(N-1)+1 clock phases for the conventional capacitor mismatch ratio insensitive algorithmic ADCs [9-11]) for an N-bit resolution. The trade-off for the lower speed is that this ADC is insensitive to capacitor mismatch ratio. Besides three main capacitors (each based on kT/C noise requirement) there are a number of offset cancelation capacitors. These capacitors are nominally equal to the three main capacitors, but the matching of these capacitors is not critical; hence they can be high-density capacitors such as MOS capacitors.

The ADC has one sampling phase, ϕ_s, to sample a new input sample. This clock phase is then followed by three main clock phases ϕ_1, ϕ_2 and ϕ_3 per conversion bit, see Fig. 2.17. There are also a number of combined clock phases. For example, ϕ_{s3}, is a clock signal that is logic high for both phase ϕ_s and ϕ_3. The control signals for the offset canceling capacitors are denoted $\phi_{3,i}$, which means that this control signal is logic high during ϕ_3 but only for the ith cycle.

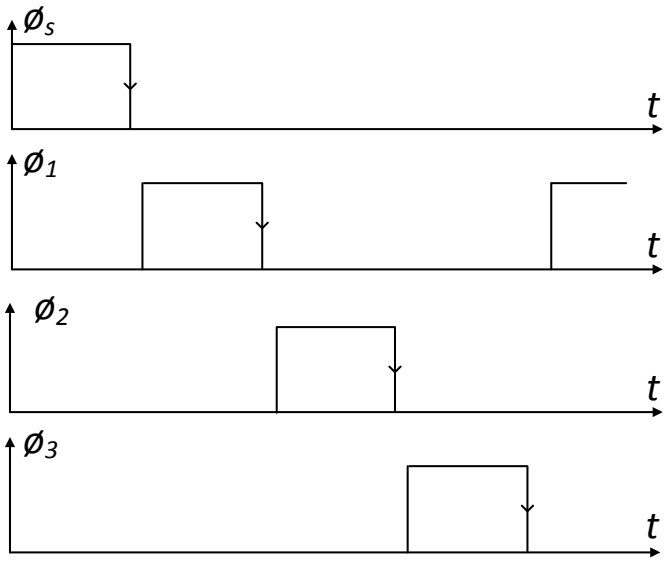


Fig. 2.17 Clocks for capacitor mismatch ratio insensitive algorithmic ADC.

The sampling phase, ϕ_s, is shown in Fig. 2.18. During this phase, the input is sampled onto capacitors C_1 and C_3 and the MSB bit is determined by the comparator. Capacitors C_2 and $C_{off,1..M}$ sample the amplifier offset.

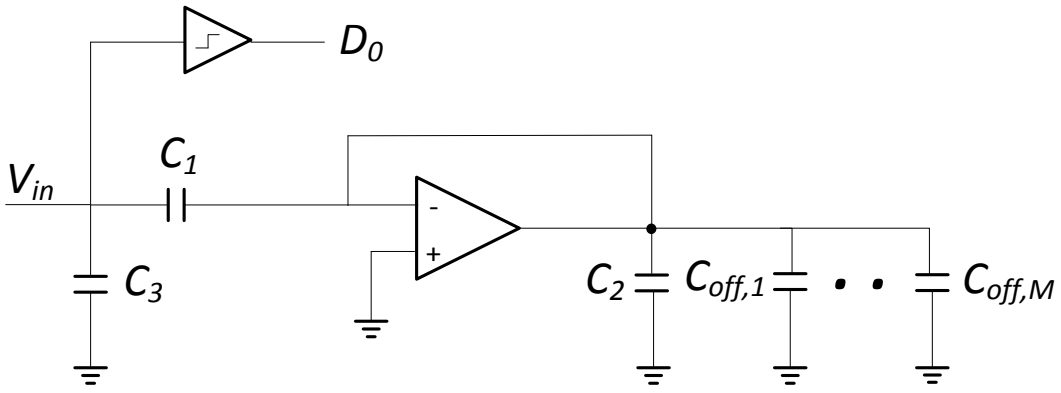


Fig. 2.18 Sampling phase ϕ_s.

During the next clock phase ϕ_1, a positive or negative reference voltage is applied to C_1 (depending on the MSB bit determined in the previous clock phase) and subtracted from the input sample at the amplifier output, see Fig. 2.19. Capacitor C_3 is not used in this phase, it is retaining the input sample which will be applied in the next phase.

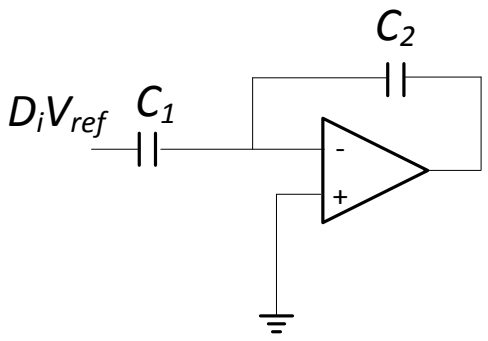


Fig. 2.19 Clock phase ϕ_1.

During phase ϕ_2, the C_1 capacitors is again charged to the original input sample, see Fig. 2.20, by placing the C_3 capacitor in feedback around the amplifier.

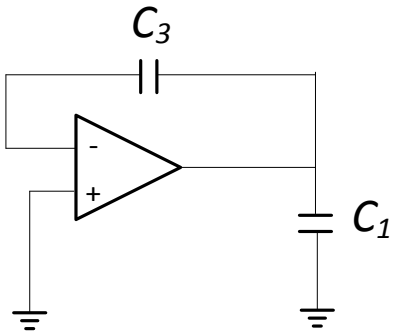


Fig. 2.20 Clock phase ϕ_2.

During phase ϕ_3, see Fig. 2.21, the amplifier output is ideally equal to $2V_{in}$ +/- V_{ref} and this value is compared with GND to determine the second output bit.

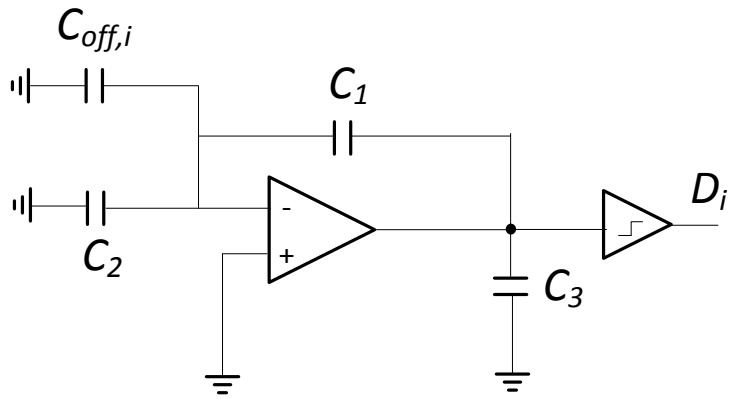


Fig. 2.21 Clock phase ϕ_3.

The actual amplifier output due to amplifier non-idealities is given by (2.8), where A is the finite amplifier gain and V_{off} the amplifier offset. The capacitor $C_{off,1}$ is connected in this phase to cancel the amplifier offset.

$$V_{out,1} = \frac{\frac{V_{in}C_1}{1+1/A} + V_{out,x}C_2\left(1+\frac{1}{A}\right)}{C_1 + \frac{C_1+C_2}{A}} + \frac{V_{off}\left(C_1 + \frac{C_1}{1+1/A} - C_{off,1} - \frac{C_{off,1}}{1+1/A}\right)}{C_1 + \frac{C_1+C_2}{A}} \tag{2.8}$$

where $V_{out,x} = \frac{V_{in}C_1 - D_0 V_{ref}C_1 + V_{off}\left(C_1 + C_2 - \frac{C_1+C_2}{1+1/A}\right)}{C_2 + \frac{C_1+C_2}{A}}$

If the amplifier gain approaches infinity, the expression in (2.8) approaches the expression in (2.9).

$$V_{out,1}\Big|_{A->\infty} -> 2V_{in} - D_0 V_{ref} + 2V_{off}\left(1 - \frac{C_{off}}{C_1}\right) \tag{2.9}$$

As seen in (2.9), with large enough amplifier gain, the output voltage is not a function of capacitor ratios. It can be shown that the minimum amplifier gain is given by (2.10).

$$A > 3 \cdot 2^N \tag{2.10}$$

It can be noted that the minimum amplifier gain is smaller than the requirement for the ADC presented previously in this chapter (equation (2.6)). The reason is that the amplifier output does not determine the MSB bit, but rather the second most significant bit, which has a lower resolution requirement.

Depending on the amount of amplifier offset and the matching between C_1 and $C_{off,1}$ there is a residual offset term. The minimum required matching between C_1 and $C_{off,1}$ is determined by (2.11), where Δ is the ADC resolution (LSB).

$$1 - \frac{C_{off}}{C_1} < \frac{\Delta}{2V_{off}} \tag{2.11}$$

As a numerical example, if V_{off}=5mV and Δ=500μV, then a 5% mismatch between C_1 and $C_{off,1}$ can be accepted.

The three main clock phases are now repeated for each conversion bit, and the output in phase ϕ_3 is given by (2.12), where $V_{out,i}$ is the output of the ith cycle (which is compared with GND to determine bit i+1).

$$V_{out,i} = \frac{\frac{V_{out,i-1}C_1}{1+1/A} + V_{out,x,i}C_2\left(1+\frac{1}{A}\right)}{C_1+\frac{C_1+C_2}{A}} + \frac{V_{off}\left(C_1+\frac{C_1}{1+1/A}-C_{off,i}-\frac{C_{off,i}}{1+1/A}\right)}{C_1+\frac{C_1+C_2}{A}} \tag{2.12}$$

where $V_{out,x,i} = \frac{V_{out,i-1}\left(C_1+\frac{C_1+C_2}{A}\right) - D_{i-1}V_{ref}C_1}{C_2+\frac{C_1+C_2}{A}}$

It can be shown that with infinite amplifier gain, the output of the ith cycle is $2V_{out,i-1}$ +/- V_{ref} plus an offset term, which depends on the matching between C_1 and $C_{off,i}$ (same term as in (2.9)). Furthermore, since the accuracy requirement is reduced by a factor of two for each cycle, for a practical implementation only the first few cycles will require offset cancellation. Due to the large loading of the amplifier in the sampling phase, the

width of this phase may have to be larger than the width of the other phases. But on the other hand, since the ADC doesn't require a perfect offset cancellation, if the sampling time is not long enough, then this effectively means that the value on the capacitors at the end of the sampling phase is a little smaller than the actual offset, and this translates into an effective mismatch error in the capacitors.

2.4.2 Simulation Results

This section presents simulation results for the algorithmic ADC presented in section 2.4.1. The intended resolution is 12 bits (Δ=488μV). With infinite amplifier gain, 5% capacitor mismatch ratio and no offset, the ADC achieves an almost ideal effective resolution, as seen in Fig. 2.22 and Table 2.4, which confirms the effectiveness of the ADC architecture.

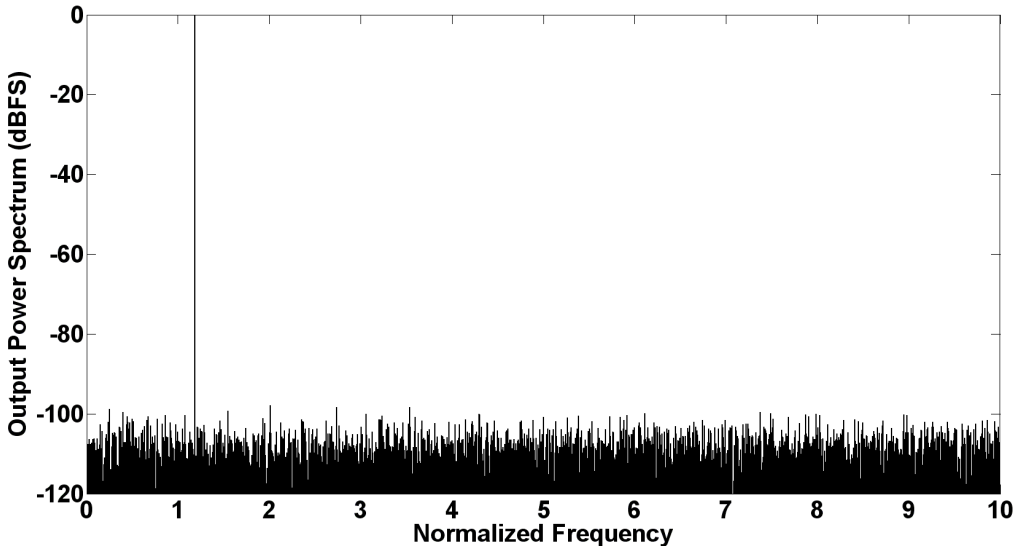


Fig. 2.22 ADC output power spectrum with 5% capacitor mismatch ratio.

Table 2.4 shows the effect of various non-idealities. As seen in Fig. 2.23 and Table 2.4, finite amplifier gain is the main source of non-linearity, while the offset cancelation capacitors increase the effective resolution as expected. The amplifier gain should be made large enough with circuit techniques. The results in Fig. 2.23, and Table 2.4, assume full settling, so that only the finite gain of the amplifier is affecting the resolution. Table 2.4 also shows that comparator offset reduces the effective resolution, which should be corrected for with a comparator offset cancellation technique.

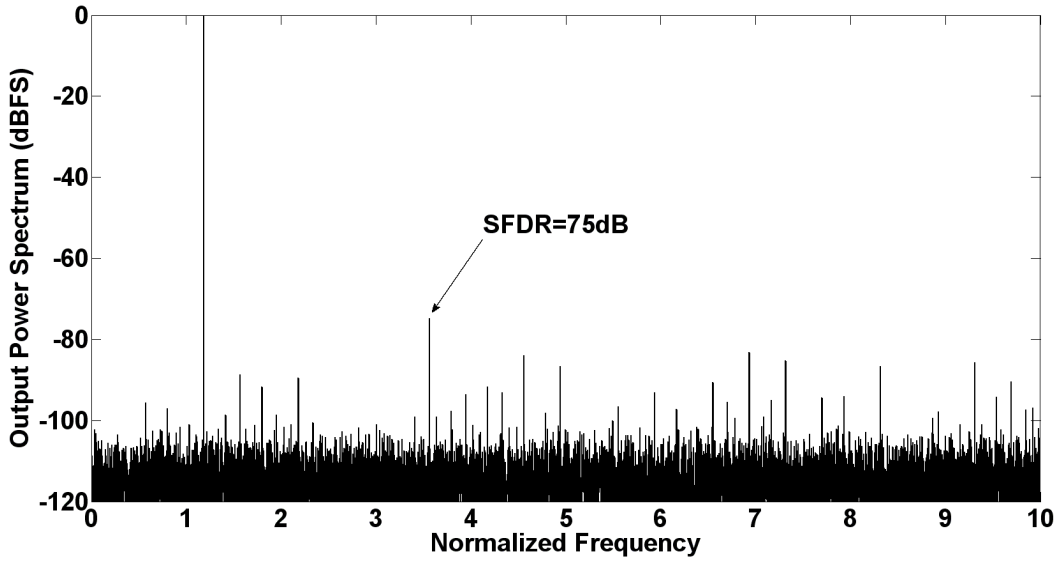


Fig. 2.23 ADC output power spectrum with finite amplifier gain.

Table 2.4 Simulation results.

Parameters	ENOB (bits)
A=∞, cap. mismatch ratio=1, V_{off}=0	11.97
A=∞, cap. mismatch ratio=0.95, V_{off}=0	11.97 (see Fig. 2.22)
A=∞, cap. mismatch ratio=1, V_{off}=5mV	10.32
A=∞, cap. mismatch ratio=1, V_{off}=5mV,$C_{off,1..5}$=0.95	11.9
A=∞, cap. mismatch ratio=0.95, V_{off}=5mV,$C_{off,1..5}$=0.95	11.9
A=$3\cdot 2^{12}$, cap. mismatch ratio=0.95, V_{off}=5mV,$C_{off,1..5}$=0.95	11.8
A=4000, cap. mismatch ratio=0.95, V_{off}=5mV,$C_{off,1..5}$=0.95	11.3 (see Fig. 2.23)
A=500, cap. mismatch ratio=0.95, V_{off}=5mV,$C_{off,1..5}$=0.95	8.65
A=4000, cap. mismatch ratio=0.95, V_{off}=5mV,$C_{off,1..5}$=0.95,$V_{comp,off}$=1mV	11.2
A=4000, cap. mismatch ratio=0.95, V_{off}=5mV,$C_{off,1..5}$=0.95,$V_{comp,off}$=5mV	10.8
A=4000, cap. mismatch ratio=0.95, V_{off}=5mV,$C_{off,1..5}$=0.95,$V_{comp,off}$=10mV	10.1

2.5 Conclusions

This chapter presented a robust, compact, low complexity and low power single-ended switched-capacitor algorithmic ADC which enables power savings at the system-level by operating with a single reference voltage and presenting a small input capacitance. The ADC was fabricated in a standard 90nm CMOS technology, and occupies an area of $0.27mm^2$. The ADC has a measured SNR/SNDR of 49.9dB/46.7dB with a sampling rate of 0.25 MS/s and a power consumption of 300µW. The measured DNL and INL are within +0.6/-0.5 LSB and +0.2/-0.5 LSB, respectively.

This chapter also presented a capacitor mismatch ratio insensitive algorithmic ADC which uses less clock phases than the conventional ADCs [9-11]. It uses only one amplifier and comparator, and a few high-density capacitors with very relaxed matching requirements for offset cancellation. Simulation shows that the proposed ADC has almost ideal performance in the presence of capacitor mismatch, while finite amplifier gain causes non-linearity. This proposed ADC should be further characterized with silicon results to verify its effectiveness.

CHAPTER III

A 360 FJ/CONVERSION-STEP, 14-BIT, 100 MS/S, 105 MW DIGITALLY BACKGROUND CALIBRATED PIPELINED ADC IN 130-NM CMOS

3.1 Introduction

Application such as instrumentation, video, radar and communications require high speed and high resolution analog-to-digital converters (ADCs) to convert the analog information to digital for post-processing with a Digital-Signal-Processor (DSP). Pipelined ADCs are often used for such applications as the pipelining of the conversion process results in a good trade-off between linearity and speed, at the cost of an increased latency. The gain in each pipeline stage relaxes the noise and linearity requirements for the subsequent stages, such that the power and silicon area requirement can be scaled down towards the end of the pipeline chain. However, the resolution in a standard CMOS process is typically limited to approximately 10 bits. For higher resolutions calibration is often necessary to achieve the required accuracy; calibration typically reduces the power and silicon area requirement because component matching is relaxed and amplifier gain might be reduced as well.

3.1.1 Previous Work on Pipelined ADCs with Calibration

Calibration of pipelined ADCs can in general be characterized as one of two types: a) foreground calibration and b) background calibration. In foreground calibration, the normal conversion process is interrupted and a known test signal is applied. Background calibration corrects for errors without interrupting the normal conversion process and the error correction process is continuously updated to compensate for time-varying errors, caused by for example temperature variations or aging effects. Background calibration techniques can in turn be divided into two major types: a) channel error identification and b) correlation-based. In the channel error identification approach the error function is constructed through the outputs of two different paths. An additional slow but accurate ADC usually generates the desired response which acts as an ideal reference for calibration [16-23], see Fig. 3.1.

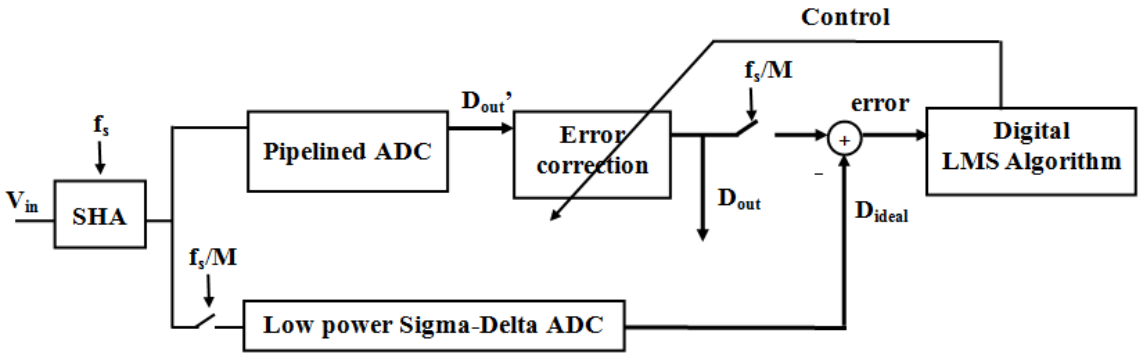


Fig. 3.1 Background calibration using a reference ADC [23].

The least-minimum-square algorithm is usually employed to determine a set of correction parameters which are then used to correct for errors in digital domain. The main disadvantages of these techniques are the need for a second ADC to sample the input and potential problems with synchronization between the signal paths. If the reference ADC is connected between pipeline stages, then it will also load the stage amplifiers which could increase the power consumption of these amplifiers or require a power control implementation (depending on whether the pipeline stage is under calibration or not).

Correlation-based techniques allow performing a background calibration of the errors without the necessity of a reference ADC [24-34]. These techniques employ a known digital signal N to introduce a perturbed component in the output code of the ADC depending on its two possible values. As a result of this component injection, the output code becomes modulated by the digital sequence. Under these conditions, a statistical estimation of the errors can be obtained, and it is therefore possible to calibrate the ADC by correlating the injected sequence with the converter output code.

This chapter presents a true digital background calibration technique which doesn't require the generation of digital correlation signals and obtaining statistical estimates of the errors, nor the sampling of the input signal with a redundant low-speed high-performance reference ADC. The technique presented in this chapter utilizes the inherent unique points in the stage residue curve to determine digital correction

parameters for the pipeline ADC. These parameters are then used to correct for errors in digital domain, with only a small memory required and few binary multiplications and addition operations. The technique calibrates for errors resulting from capacitor mismatch, finite amplifier gain, voltage reference errors and differential offsets and linearizes the ADC without requiring any extra analog calibration components.

The proposed technique is a general extension of the foreground techniques presented in [35-36]. Unlike [35-36], the proposed technique in this chapter is a background technique, with a much simpler algorithm implemented completely in digital domain. The final result is a state of the art solution that achieves a remarkable figure of merit of 360 fJ/conversion step.

3.2 Description of Pipelined ADC

This section gives an overview of the pipelined ADC architecture. The circuit level details and inherent error sources are described, and a motivation for employing calibration is given.

3.2.1 Principles of a 1.5 Bits/Stage Pipelined ADC

The architecture of the pipelined ADC implemented in this chapter is shown in Fig. 3.2. The ADC is based on the 1.5-bit /stage pipeline and is implemented fully differential to

minimize common-mode and power supply noise, charge injection and clock feedthrough in the analog output of the pipeline stage. The implementation in Fig. 3.2 uses two non-overlapping clocks, $\phi 1$ and $\phi 2$, as well as early clocks and a separate latch clock. Kickback noise from the comparators disturb the voltage being sampled onto the sampling capacitors but with a separate early clock, the transient disturbance at the sampling instant becomes negligible. It can be noted that at 14-bit resolution, the peak kickback noise disturbance on the input signal line can be a significant fraction of an LSB, even with preamplifiers in the comparators, due to device parasitic capacitance and parasitic coupling in the layout. There is also the issue that at the moment of opening the early sampling switches, transient disturbances will appear at the input voltage lines, which could affect the decision of the comparator.

There are 16 pipeline stages in the ADC plus one final stage which is comprised of only a comparator. The extra pipeline stages increase the resolution of the backend and reduces the power of the quantization noise floor, so that the ADC noise floor is limited by circuit noise. There are a total of 33 output bits and one clock output to enable synchronization for testing purposes. The ADC is designed for 14-bits resolution at 100 MSamples/s.

The starting point for determining the capacitance value is the thermal noise contribution to the output voltage. All capacitors in the pipeline stage are nominally equal with value C. The pipeline stage is fully differential and the noise power from the switches is

4kT/2C, when considering the noise contributions from both sampling and hold phases. Similar to (2.7), the capacitance requirement for a 14-bit system (with m=1) is 2C>13pF. This is a very large value and it would require very large power consumption in the amplifier and a very small on-resistance of the switches to meet the settling requirement. If the capacitance value is reduced then the thermal noise floor is increased, but for a practical implementation there will be other error sources that will dominate the performance; the capacitance value was chosen as 2C=4pF for the MSB stage.

It can be noted that the pipeline stages (capacitor value, amplifier bias currents and switches) scale by roughly a factor of two for each stage towards the backend. The smallest value for C is 125fF, at which point the pipeline stages no longer scale and are replicated.

The output voltage of the pipeline stage depends on in which region the input sample is present, as shown in Fig. 3.3. The three regions are defined by the two comparators. Their thresholds are usually placed at $\pm V_{ref}/4$, to allow for a large comparator offset and to avoid overshoot, where V_{ref} is the differential reference voltage that defines the input range. Non-idealities in the pipeline stage cause the ideal output curve to have an offset and gain error, as shown in Fig. 3.3.

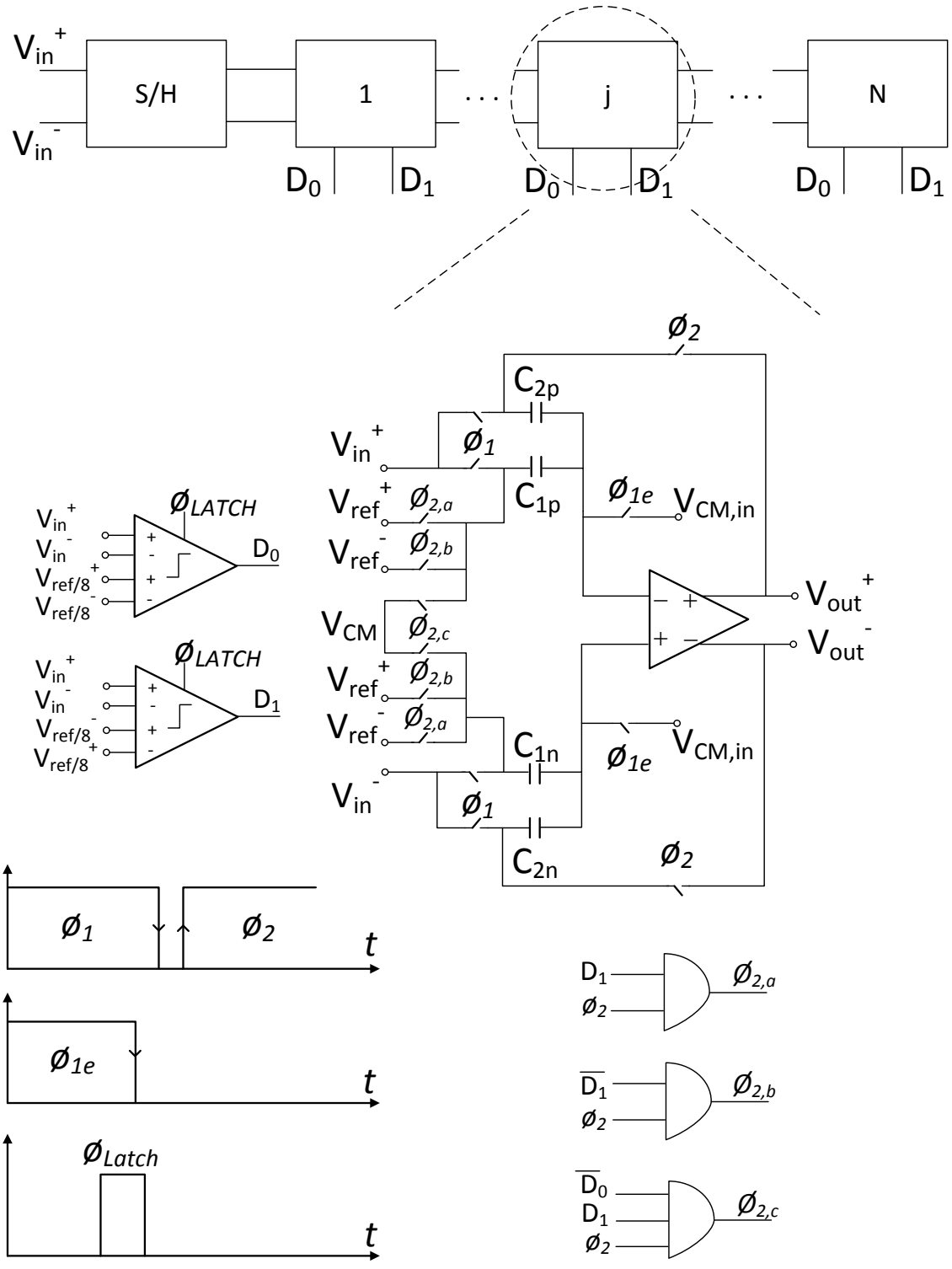


Fig. 3.2 Differential pipeline ADC with 1.5 bits/stage conversion.

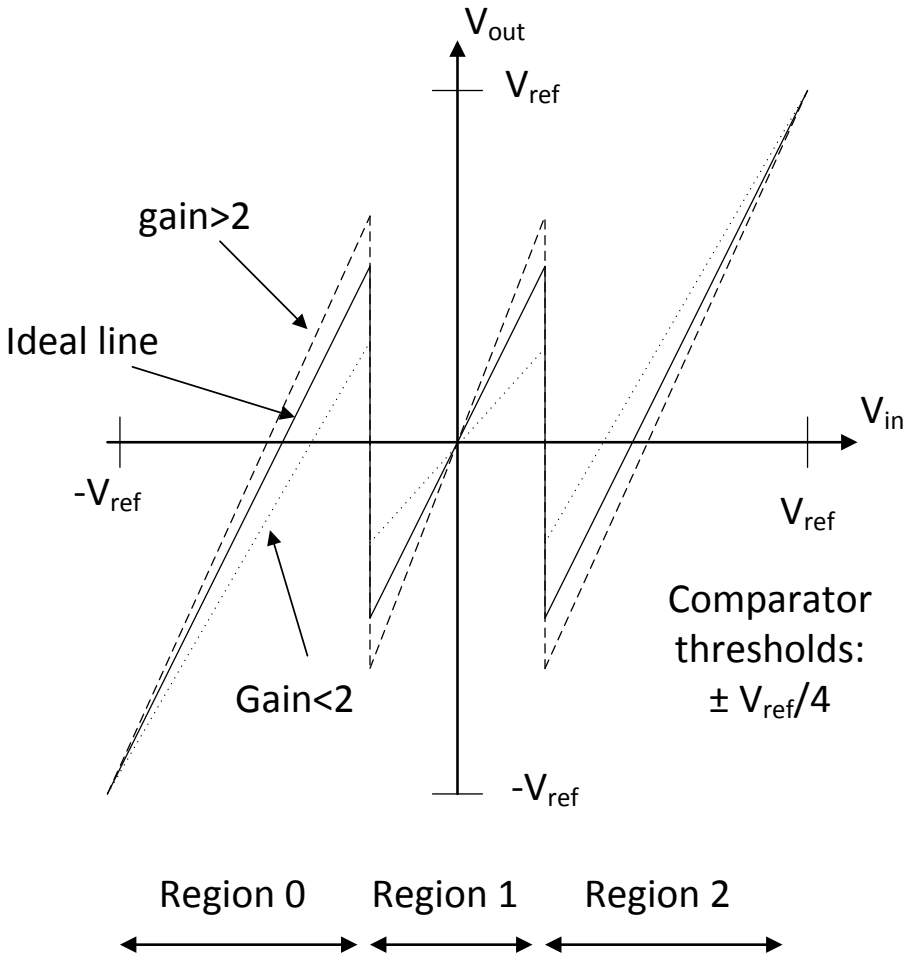


Fig. 3.3 Pipeline stage residue curve.

The differential output voltage in each region can be expressed as in (3.1), where A is the finite amplifier gain, V_{offset} is the output-referred differential offset, α is the error in the reference voltage and V_{CM} the common-mode voltage.

$$V_{out}^{+} - V_{out}^{-} = G((1+k_p)V_{in}^{+} - (1+k_n)V_{in}^{-} + k_n V_{ref,x} - k_p V_{ref,y} + V_{offset}) \tag{3.1}$$

where $G = \frac{2A}{2A+2+k_p+k_n}$; $k_p = \frac{C_{1p}}{C_{2p}}$ and $k_n = \frac{C_{1n}}{C_{2n}}$.

The reference voltages are defined as follows:

$$V_{ref,x}, V_{ref,y} = \begin{cases} V_{ref}^{+}, V_{ref}^{-}, \text{region} \quad 0 \\ V_{CM}, V_{CM}, \text{region} \quad 1 \\ V_{ref}^{-}, V_{ref}^{+}, \text{region} \quad 2 \end{cases} \qquad \begin{aligned} V_{ref}^{+} &= V_{CM} + \alpha \frac{V_{ref}}{2} \\ V_{ref}^{-} &= V_{CM} - \alpha \frac{V_{ref}}{2} \end{aligned}$$

$$V_{ref,diff} = \begin{cases} V_{ref}, \text{region} \quad 0 \\ 0, \quad \text{region} \quad 1 \\ -V_{ref}, \text{region} \quad 2 \end{cases}$$

The ideal differential output voltage is expressed in (3.2).

$$\left(V_{out}^{+} - V_{out}^{-}\right)_{ideal} = 2(V_{in}^{+} - V_{in}^{-}) + V_{ref,diff} \tag{3.2}$$

From (3.1) it is observed that finite amplifier gain, capacitor mismatch ratio, errors in the reference voltages and differential offsets will cause an error in the output voltage. The errors present in every stage are assumed to be uncorrelated. In order to achieve an error less than ½ LSB in the output voltage, the minimum required amplifier gain, the required capacitor matching, and the maximum error in the reference voltages are given by (3.3).

$$\begin{aligned} &A > 2^{N+1} \\ &\left| \frac{k_p + k_n}{2} - 1 < \frac{2}{2^N} \right| \\ &|1-\alpha| < \frac{1}{2^N} \end{aligned} \tag{3.3}$$

For a high-resolution, high-speed ADC, the minimum amplifier gain can be costly to achieve because of low device gain. The area and power requirements will be high, and a multistage topology may be required, which may have inherent stability problems. The required capacitor matching will require a very large capacitive area, and on-chip matching is usually limited to 10-12 bits. The stringent accuracy requirement for the voltage references will be very difficult to achieve with gain and offset errors in CMOS reference buffers.

Instead of designing the analog components to meet these high accuracy requirements, the requirements can be relaxed by correcting for the errors caused by these non-idealities in the ADC output.

The next section presents a technique to correct for the errors introduced by the non-ideal analog components by post-processing the digital ADC output.

3.3 Description of the Proposed Calibration Technique

The proposed digital background calibration technique is described in detail in this section. The technique is first explained from an intuitive perspective and then described with more mathematical details. The technique can generally be described to determine a number of digital parameters which are then used to perform error-correction in digital domain. Simulation results are also presented as proof-of-concept. For a practical implementation, only the first few stages require calibration, the remaining stages (the backend) will then be accurate to its intended resolution. In this prototype ADC, the first six stages are calibrated.

3.3.1 Calibration Principle

The principle of the calibration technique is shown by the block diagram in Fig. 3.4. The backend is used to obtain information from the last stage requiring calibration, and when this stage is calibrated, it becomes part of the backend and the preceding stage is then calibrated, and so on.

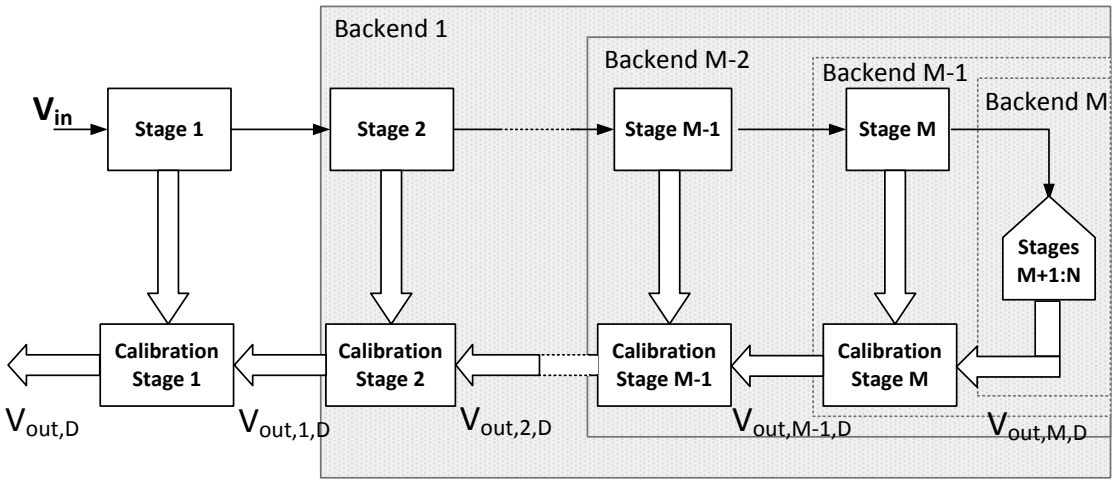


Fig. 3.4 Block diagram of calibration principle.

The pipeline stage non-idealities described in (3.1) cause the output residue curve to deviate from the ideal curve, as shown in Fig. 3.3. The basic idea behind the calibration technique can intuitively be described as follows: a deviation in a linear segment can be corrected for by multiplying the output with a correction parameter and adding it with another parameter, which values depends on in which region of the residue curve the input sample is present; the corrected output is then expressed in terms of the calibration parameters as described in (3.4). The slope of the output curve is corrected for with the a_i parameter, while the zero-crossing is corrected for by employing the b_i parameters, as shown in Fig. 3.5. $V_{out,i,D}$ is the output of the ith stage in digital domain (given by the backend) and M stands for the number of pipeline stages requiring calibration.

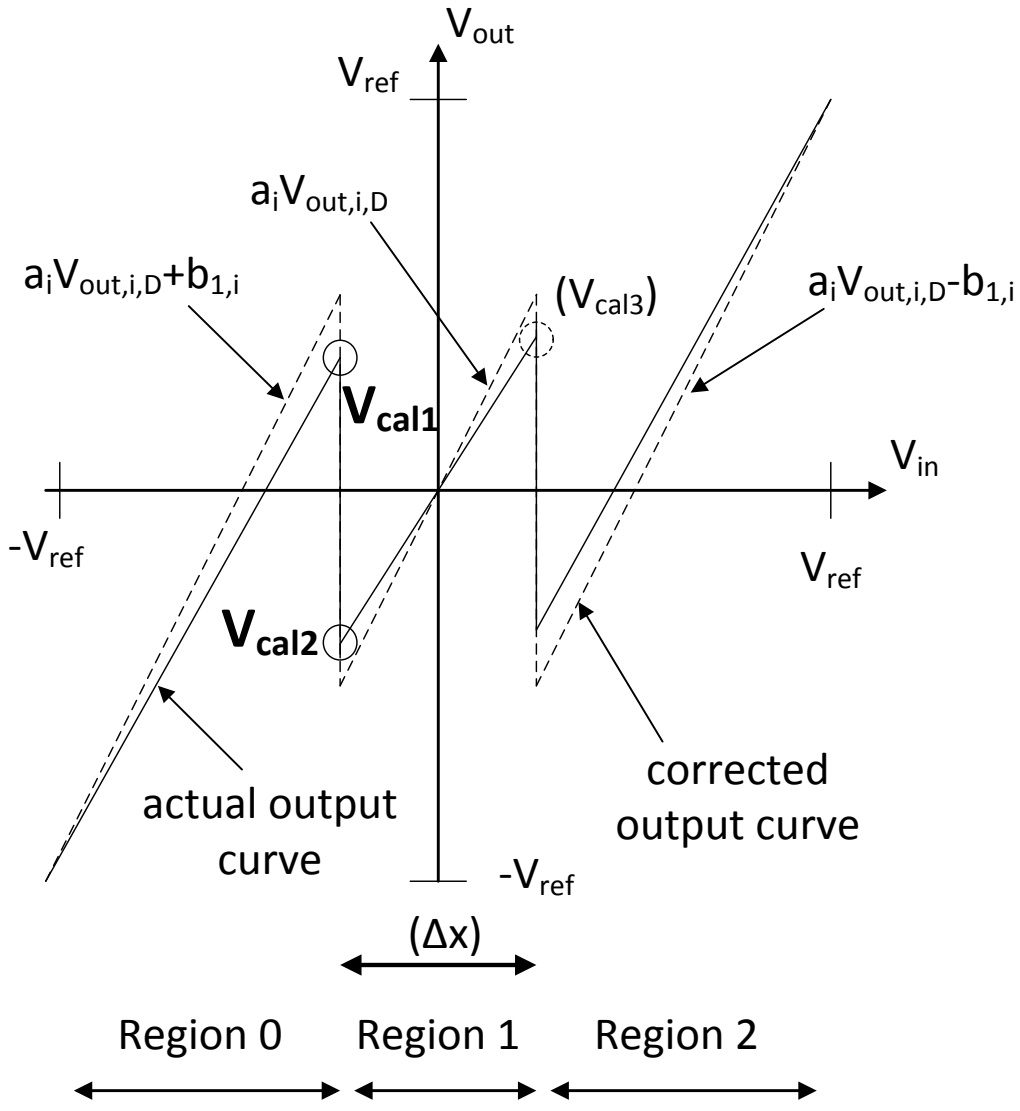


Fig. 3.5 Output residue curve with correction.

$$V_{out,i,D,corrected} = \begin{cases} a_i V_{out,i,D} + b_{1,i} = 2\left(V^{+}_{out,i-1} - V^{-}_{out,i-1}\right) \\ +V_{ref} \quad , region \quad 0 \\ a_i V_{out,i,D} + b_{2,i} = 2\left(V^{+}_{out,i-1} - V^{-}_{out,i-1}\right) \\ \qquad , region \quad 1 \qquad i = 1..M \\ a_i V_{out,i,D} + b_{3,i} = 2\left(V^{+}_{out,i-1} - V^{-}_{out,i-1}\right) \\ -V_{ref} \quad , region \quad 2 \end{cases} \tag{3.4}$$

The analytical expressions for the calibration parameters are obtained from (3.4) and (3.1), leading to (3.5):

$$\begin{aligned} a_i &= \frac{2(2A_i + 2 + k_{p,i} + k_{n,i})}{A_i(2 + k_{p,i} + k_{n,i})} \\ b_{1,i} &= \frac{2V_{ref} + V_{ref}\left(k_{p,i} + k_{n,i}\right)(1 - 2\alpha_i)}{2 + k_{p,i} + k_{n,i}} - \frac{4V_{offset,i}}{2 + k_{p,i} + k_{n,i}} \\ b_{2,i} &= \frac{-4V_{offset,i}}{2 + k_{p,i} + k_{n,i}} \\ b_{3,i} &= -\frac{2V_{ref} + V_{ref}\left(k_{p,i} + k_{n,i}\right)(1 - 2\alpha_i)}{2 + k_{p,i} + k_{n,i}} - \frac{4V_{offset,i}}{2 + k_{p,i} + k_{n,i}} \end{aligned} \tag{3.5}$$

From (3.5) it is observed that the $V_{offset,i}$ term is common to all b parameters and causes a small offset error in the residue output curve. This constant offset does not affect the linearity of the pipeline stage and is not estimated in the proposed algorithm; hence it is considered that $b_{2,i}=0$ and $b_{3,i}=-b_{1,i}$. Notice that the slope of the line in each region is the same and therefore only one a parameter is required, because the gain error of all regions of the ith stage is due to the same amplifier and same set of capacitors.

There are unique points along the residue curve which will be used to determine the calibration parameters. The points circled in Fig. 3.5, denoted V_{cal1} and V_{cal2} are used for this purpose. For the intuitive description of the calibration technique, the point denoted V_{cal3} will now also be used, but it will be demonstrated that it is not required in order to linearize the pipeline. It can be noticed that the vertical difference between V_{cal1} and V_{cal2} is independent of any shift in the comparator threshold and only a function of the finite amplifier gain, capacitor mismatch ratio and reference voltages of the pipeline stage. For the last stage requiring calibration, these three output voltages (V_{cal1}, V_{cal2} and V_{cal3}) are directly provided by the backend, which is accurate to its intended resolution. Once this stage has been calibrated by employing the proposed calibration scheme, it then becomes part of the backend and the preceding stage is then calibrated, and this procedure is repeated until the entire pipeline is calibrated. By evaluating (3.4) in region 1, and equating the actual slope of the line (see Fig. 3.5) to the ideal value of 2, it can be obtained that the correcting slope parameter a_i must be computed by (3.6), where Δx_i is the difference between the two comparator thresholds.

$$a_i = \frac{2}{\lambda_i} = 2\frac{\Delta x_i}{V_{cal3,i} - V_{cal2,i}} \tag{3.6}$$

Similarly, the offset correcting parameters in regions 0 and 2 can be computed as in (3.7(3.7):

$$b_{1,i} = V_{ref} - a_i(V_{cal1,i} - V_{cal2,i}) \tag{3.7}$$

The parameter Δx_i in (3.6) is difficult to estimate because the two comparator thresholds depend on internal comparator offsets and errors in the reference voltages. However, it will be demonstrated that a_i does not have to be determined, and therefore Δx_i and $V_{cal3,i}$ do not have to be determined either. It is demonstrated in the Appendix that the calibration parameter a_i is inversely proportional to the product of the a's of the succeeding stages: $a_{i+1}..a_M$. When the digital output is referred to the input, the a_i parameters are multiplied and the a_i parameters cancel each other. The only remaining parameter is a_{MSB}, which can be estimated by recording $V_{cal3,MSB}$ and estimating Δx_{MSB}. If a_{MSB} is not estimated, then there will be a small gain error in the final ADC output but it is distortion free because the linear gain coefficient is not input signal dependent. This is intuitively true because a pipeline stage with a slope error is still linear. The process of applying the $b_{1,i}$ parameters is a linearization technique, as illustrated by Fig. 3.6.

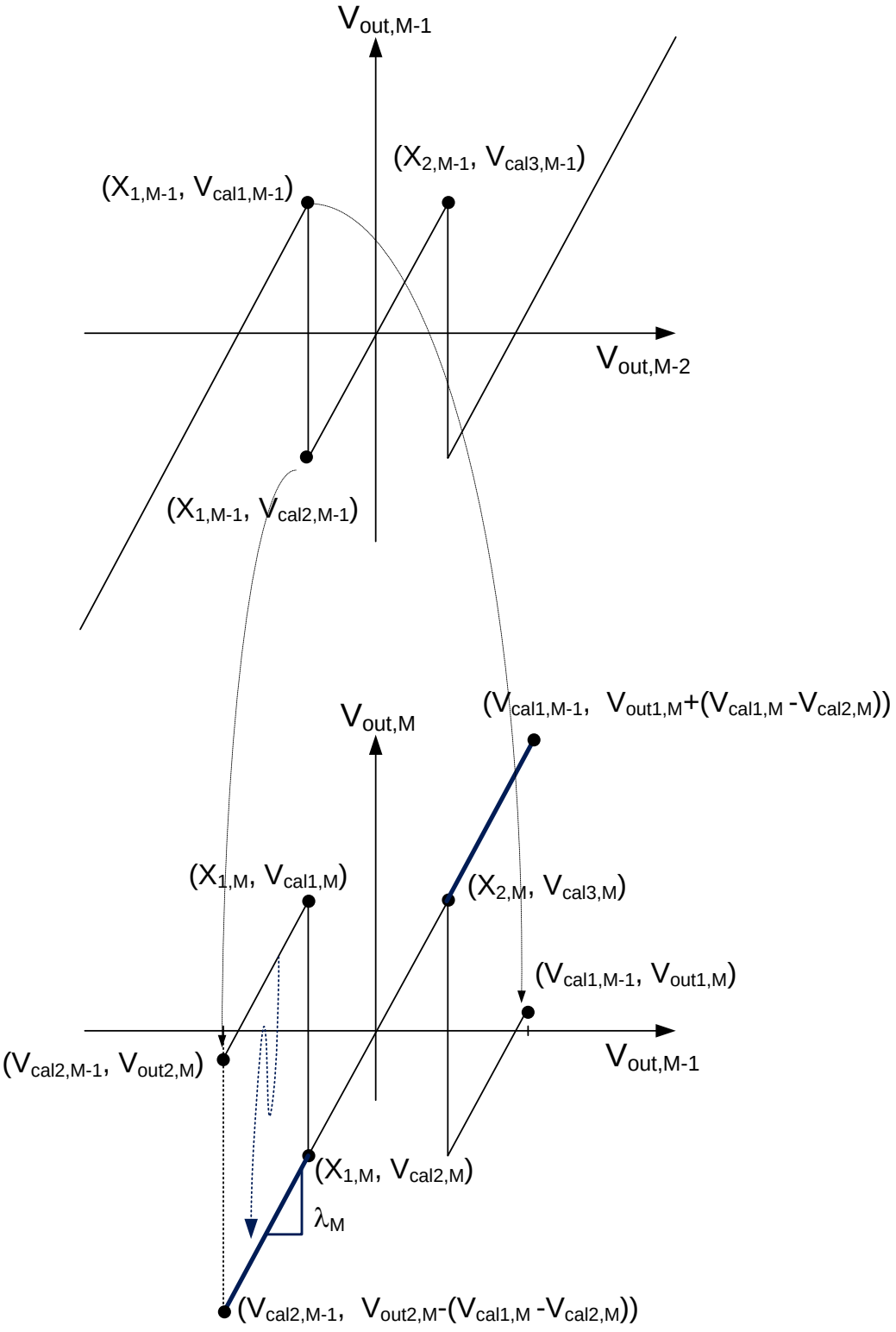


Fig. 3.6 Linearization of pipeline stage in digital domain.

Fig. 3.6 shows how the calibration points of one stage are mapped into either region 0 or region 2 of the following stage (which is already calibrated) and can be digitized by the backend. Once the vertical distance between the linear segments of the stage residue curve is known in digital domain, then the discontinuities in the stage output residue curve (at the two comparator thresholds) are removed in the digital output equivalent.

The calibration technique starts with the last stage requiring calibration (stage M) and then continues with the preceding stages. The calibration parameters of the succeeding stages are applied as the output sample is input referred from the backend, to correct for the errors introduced by those stages. The calibration technique for the ith stage is illustrated in Fig. 3.7.

The calibration technique uses the residue output values denoted V_{cal1}, V_{cal2} (see Fig. 3.5), which are determined by the backend. It is noted that if the input to any given pipeline stage is not present around the threshold of the comparator in region 0 of that pipeline stage then V_{cal1} and V_{cal2} would not appear in the output code and this pipeline stage would not be calibrated. However if the input to the ADC is uniform and present in the range between the two thresholds of the comparators in the MBS stage, and if we use coherent sampling (so that continuously different values of the input are sampled), then input samples around the comparator thresholds for all pipeline stages will be present (because the output residue of each pipeline stage is a linear function of its input).

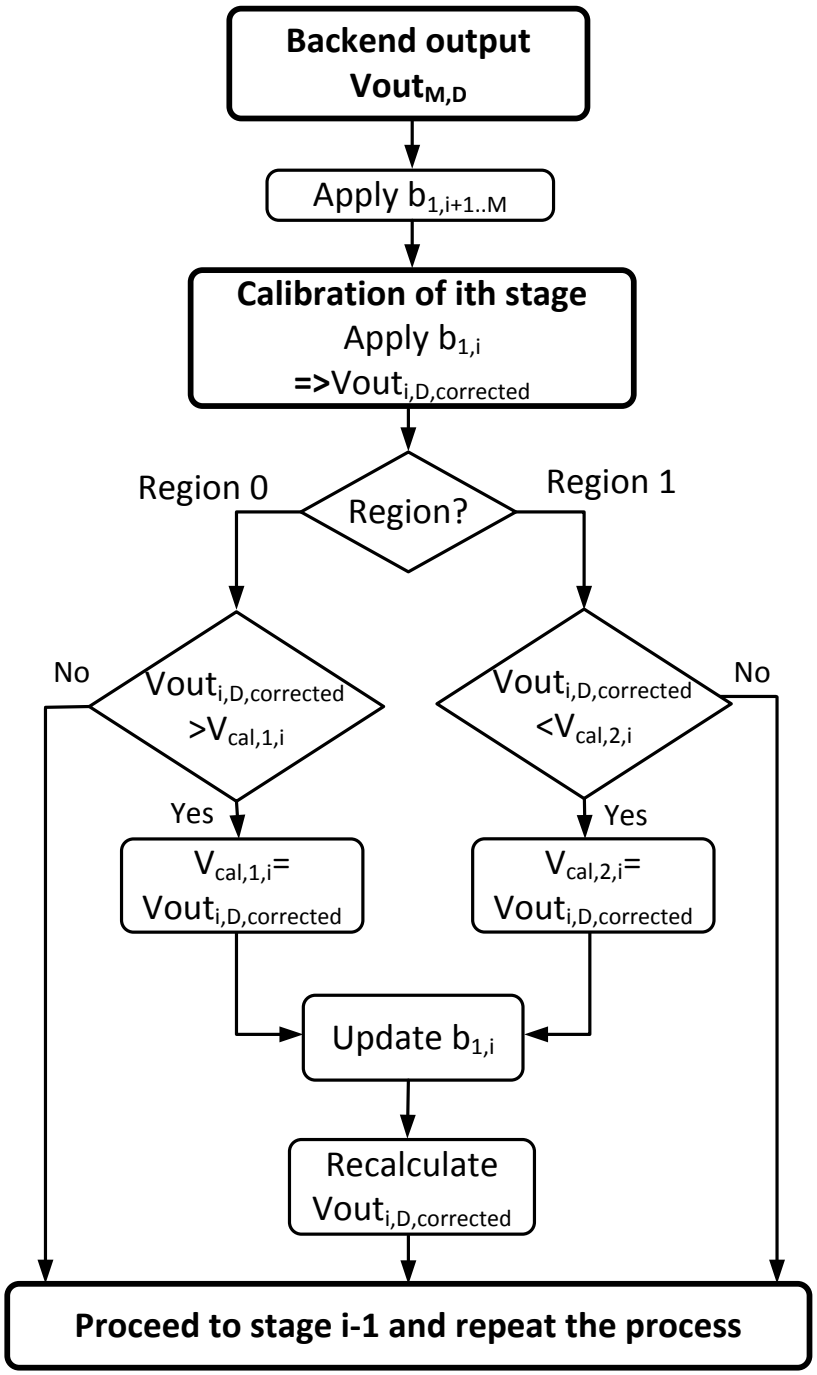
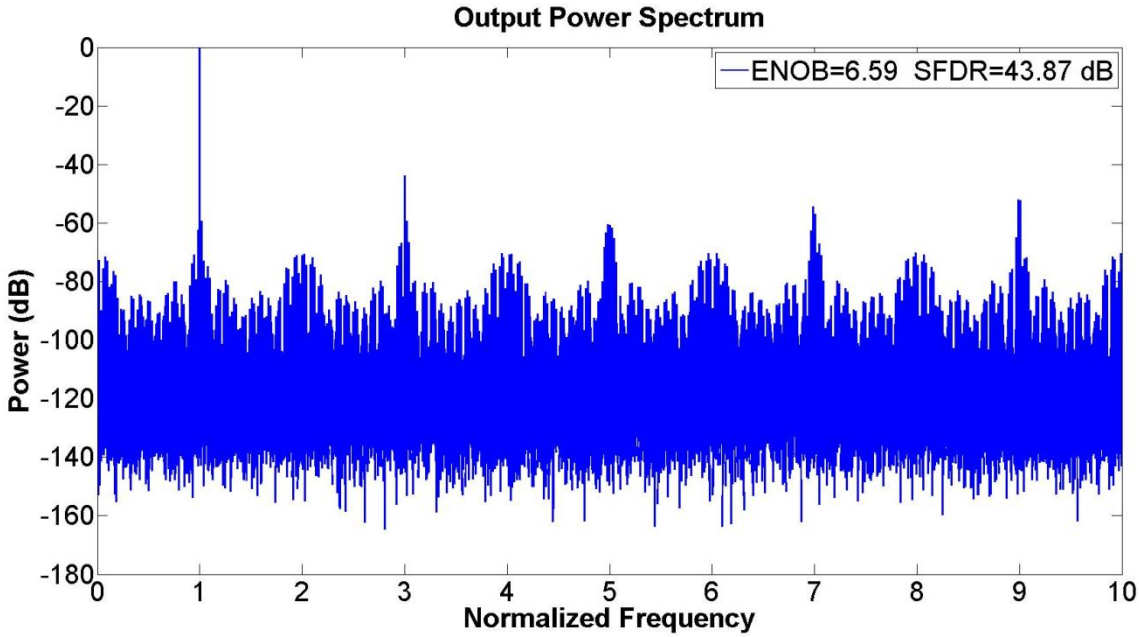


Fig. 3.7 Flowchart used for the computation of critical calibration values

The algorithm in the digital domain is simply to record the maximum value in region 0 (the region in which an input sample is present can be determined by the output bits of the comparators), and the minimum value in region 1. When a larger (or smaller) value is found compared to the value stored in memory, assume that this is the maximum value and re-calculate the calibration parameter. Since this is a background calibration technique, this process is repeated continuously. If the errors in the pipeline stages are slowly variant in time (due to temperature variations for example), then the calibration technique will automatically correct for the new errors by finding new maximums and minimums and re-calculating the calibration parameters. For a 100 MS/s ADC, and with a uniform input and with coherent sampling, it will take roughly 164μs to process 2^{14} samples and amongst these 2^{14} samples, there will be enough samples around the comparator thresholds. With six stages requiring calibration, it would take about 1ms worst-case to calibrate the entire ADC.

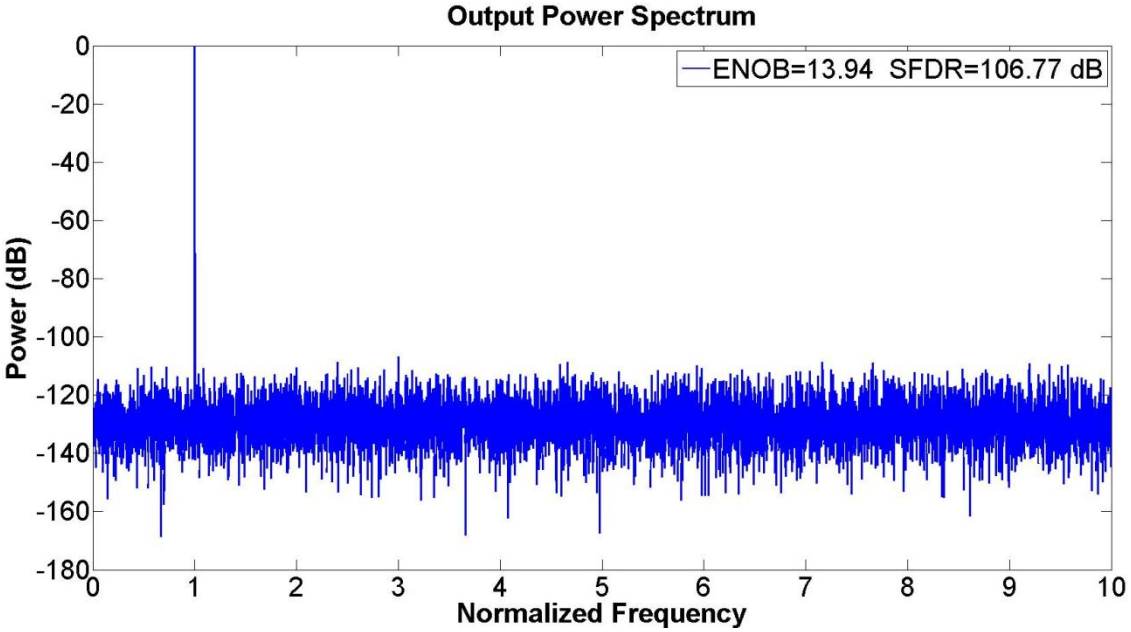
The calibration technique is designed to correct for linear errors (time-invariant or slowly time-variant). Non-linear errors will only be corrected for with a linear approximation. Shown in Fig. 3.8 are simulations results for a 14-bit pipeline ADC with the described calibration technique. The simulations are performed with the non-idealities modeled as Gaussian random-variables for each pipeline stage, with mean and standard deviation listed in Table 3.1. Fig. 3.8 shows the simulation results for the output power spectrum, with and without calibration and with non-linear amplifier gain, where the amplifier gain is a function of the output voltage of the amplifier. The non-linearity

is modeled as a tanh(x)/x function, where the gain at maximum output swing is 10% less than at zero output swing. The results in Fig. 3.8, and Table 3.1, assume full amplifier settling. There are 16 pipeline stages in the ADC and one final stage with only one comparator. The purpose of the extra pipeline stages is to increase the resolution of the backend, but they consume only a fraction of the overall ADC power consumption. The first six stages are calibrated. As seen in Fig. 3.8, the calibration technique increases the resolution of the ADC by roughly seven bits. When amplifier non-linearity is introduced, small tones appear at odd-power harmonics, but with 10% amplifier non-linearity, the effective resolution is only slightly reduced.

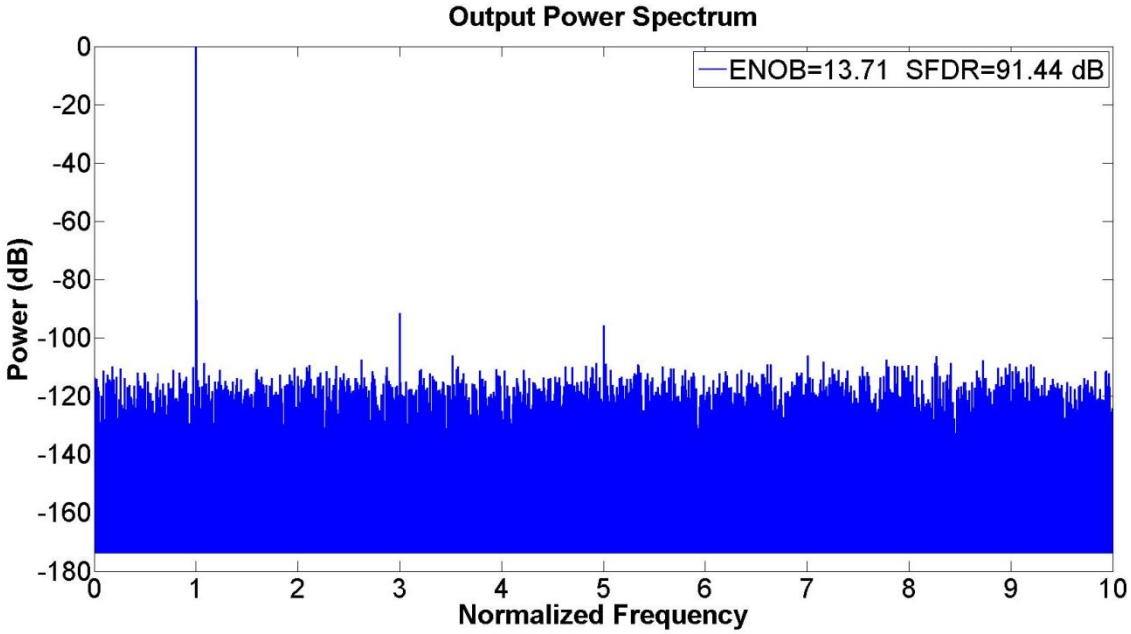


a)

Fig. 3.8 a) Without calibration. b) With calibration. c) With calibration and non-linear amplifier gain.



b)



c)

Fig. 3.8, continued

Table 3.1 Simulation non-idealities.

Parameter	Mean	3σ
A	1000	500
k_p, k_n	1	1%
V_{offset}	0	5mV
V_{ref}^{+}-V_{ref}^{-}	V_{ref}	5mV

Gaussian random noise is then added to the pipeline stage output voltage (uncorrelated between stages) and to the comparators thresholds. Noise will cause an error in the calibration parameters due to incorrect readings of the stage calibration voltages. However, if several calibration parameters (for the same stage) are collected and then averaged then the noise will be averaged out.

The noise is modeled as zero-mean and with 3σ as shown in Table 3.2. The effective resolution is shown for the case of no averaging and with averaging of N samples of the calibration parameters. The mean and standard deviation of a 100-point Histogram is shown in Table 3.2, which indicate that the mean is higher and standard deviation smaller with averaging. Using more than four samples for averaging has only marginal improvement.

Table 3.2 ADC performance with noise present.

	Mean ENOB (bits)	Std. Dev ENOB (bits)	Mean SFDR (dB)	Std. Dev SFDR (dB)
N=1; 3σ=1LSB	13.52	0.15	96.3	6.2
N=4; 3σ=1LSB	13.63	0.05	102.4	5.5
N=8; 3σ=1LSB	13.65	0.02	104.2	5.1
N=1; 3σ=2LSB	12.95	0.21	91	5.8
N=4; 3σ=2LSB	13.1	0.1	96.4	6.9
N=8; 3σ=2LSB	13.15	0.04	98.4	5.7
N=1; 3σ=3LSB	12.46	0.22	87.4	5.64
N=4; 3σ=3LSB	12.65	0.1	93	7.1
N=8; 3σ=3LSB	12.71	0.05	96.4	6.0

The power and area required for the implementation of the digital calibration algorithm is estimated in Table 3.3, using the following numbers for 0.13 μm CMOS technology: operational power: 6nW/gate/MHz and 5μm^2/gate. The estimate in Table 3.3 is for the case of N=4 averages. It is noted in Table 3.3 that the memory cells occupy the most area and power.

Table 3.3 Power and area estimate of digital calibration algorithm.

Block	Gates	Power (μW)	Area (um^2)
Comparator	80	48	400
2x Adder	168	100	840
2x Divider	192	116	960
10-bit counter	60	36	300
4-bit counter	20	12	100
4-bit clock divider	20	12	100
Memory	960	576	4800
Additional logic	100	60	500
Total:	1600	960	8000

The implementation of the digital calibration algorithm requires less than 1% of the overall ADC power consumption and almost negligible area compared with the total ADC area.

It can be noticed that this calibration technique can be extended to pipeline stages that convert more than 1.5 bits/stage, by introducing additional calibration parameters.

3.3.2 Gain Calibration Comparator

In order to perform the second part of the calibration technique, the difference between the two thresholds of the MSB stage must be known (Δx), see Fig. 3.5 and Fig. 3.9. The MSB stage uses a special comparator that enables Δx to be estimated.

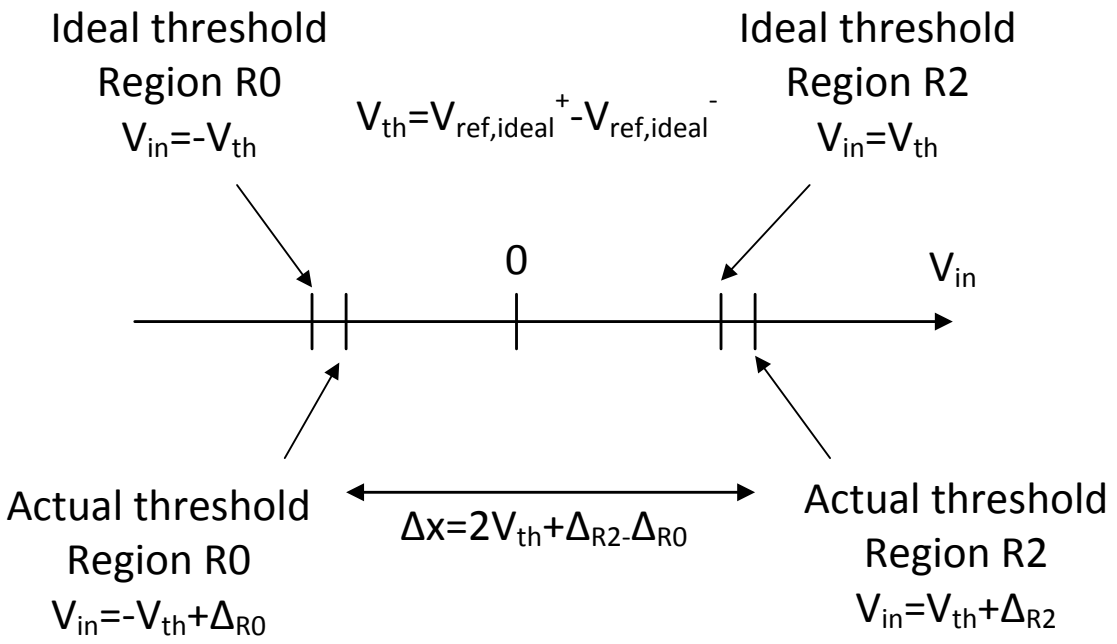


Fig. 3.9 Thresholds of gain calibration comparator.

A CMOS comparator will typically have a large offset and would require an offset cancellation technique if a very low offset is required. But even with offset cancellation the resulting offset can be larger than the resolution of the ADC. However, the

calibration technique does not require a low offset comparator, as long as the internal comparator offset is not input-dependent and the same for both regions of operations. Since the threshold in region R0 is negative, and positive in the other region, this means that the absolute value of the voltages at the comparator inputs will be different for each region and the input differential pair of the comparator will therefore produce an input referred offset that is not constant. This can be avoided by using a structure shown below in Fig. 3.10 and Fig. 3.11, where the absolute values of the voltages at the comparator inputs remain the same for both regions.

Desired operation: $V_{in}^{+} - V_{in}^{-} > V_{ref}^{+} - V_{ref}^{-} \quad \Leftrightarrow \frac{V_{in}^{+} - V_{ref}^{+}}{2} - \frac{V_{in}^{-} - V_{ref}^{-}}{2} > 0$

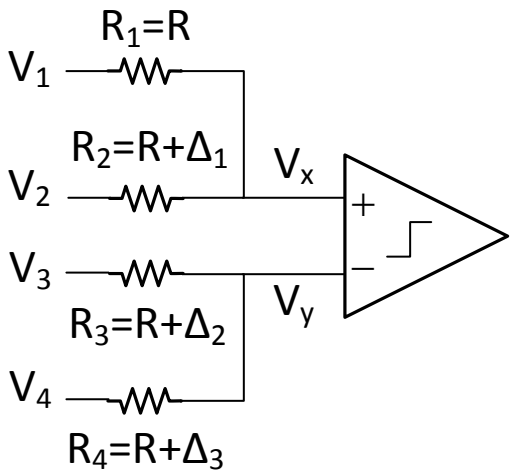


Fig. 3.10 Basic principle of gain calibration comparator.

The effective threshold of the comparator in Fig. 3.10 can be expressed as in (3.8) below, where $V_{cmpoffset}$ is the internal comparator offset.

$$\begin{aligned} &V_x - V_y > V_{cmpoffset} \quad \Leftrightarrow \\ &\frac{V_2 - V_3}{2} - \frac{V_4 - V_1}{2} > \frac{\Delta_1}{4}(V_2 - V_1) + \frac{V_3\Delta_3 + V_4\Delta_2}{2} \\ &- \frac{\Delta_2 + \Delta_3}{4}(V_3 + V_4) + V_{cmpoffset} \end{aligned} \tag{3.8}$$

In (3.8) above, it is observed that the effective threshold of the comparator in Fig. 3.9 is a function of the internal comparator offset and resistor mismatch.

The final implementation of the calibration comparator is shown below in Fig. 3.11. It should be noted that the calibration comparator is used in both region 0 and in region 2, and switches control which region of operation the comparator operates in. The calibration comparator replaces one of the regular stage comparators in the MSB stage and the power consumption of the ADC is therefore not increased, but the area is slightly increased because of the extra four resistors and the input switches.

In Fig. 3.11, region ϕ_{R0} set the threshold to be negative and region ϕ_{R2} set the threshold to be positive. While region ϕ_{R0} is enabled, V_{cal1} and V_{cal2} are found, and while region ϕ_{R2} is enabled, V_{cal3} is found.

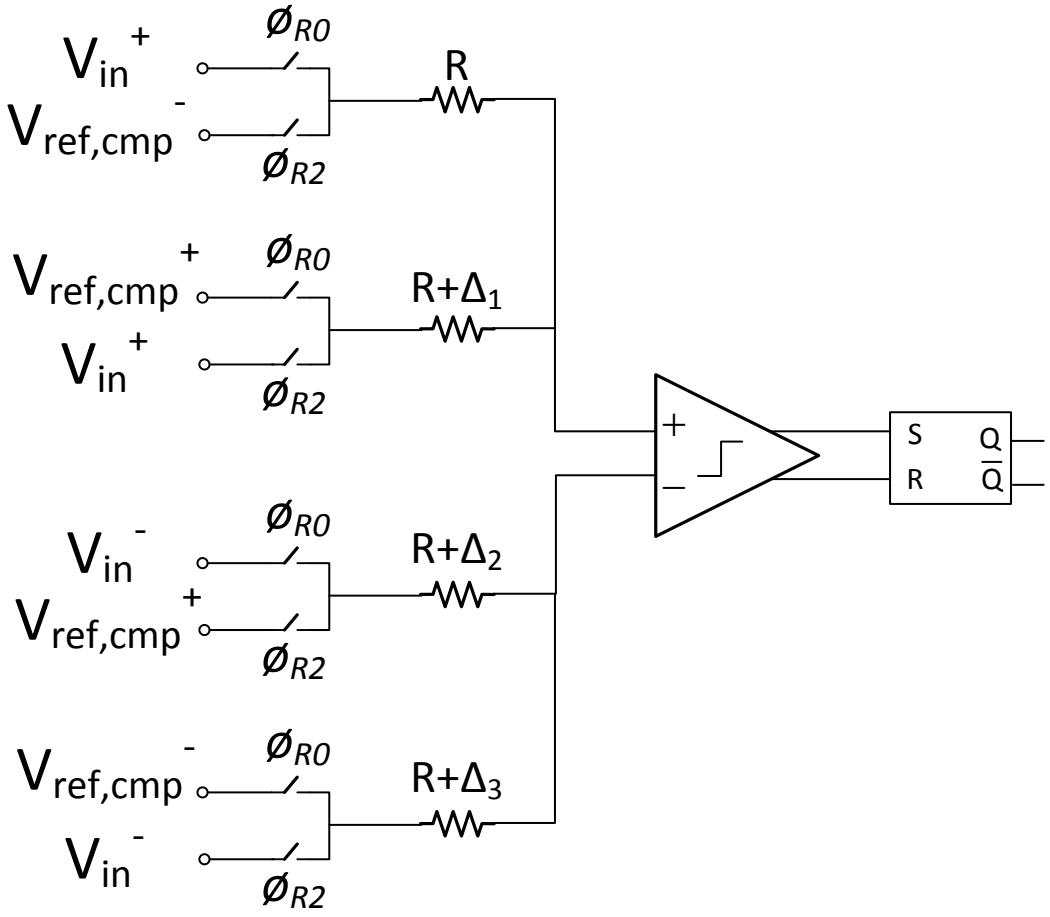


Fig. 3.11 Gain calibration comparator.

The expressions for the effective thresholds in each region is found below, where the switches are assumed to be ideal. The effect of the real switches is discussed later in the chapter.

Definitions:

$$V_{ref}^{+} = V_{CM,ref} + \frac{V_{th}}{2} + \frac{V_{ref,err}}{2}$$

$$V_{ref}^{-} = V_{CM,ref} - \frac{V_{th}}{2} - \frac{V_{ref,err}}{2}$$

The notation for the error in the reference voltage is slightly different here, for convenience of the analysis in this section. The error in the reference voltage was previously denoted α, here it is shown as an additive term, $V_{ref,err}$. V_{th} is the desired differential threshold (for example $V_{ref}/4$, see Fig. 3.9). $V_{CM,ref}$ is the common-mode level of the reference voltages, which may be different from the common-mode level of the inputs.

Definitions region ϕ_{R0} (negative threshold: V_{in}^{+}-V_{in}^{-} < 0)

$$V_{in}^{+} = V_{CM,in,R0} - \frac{V_{th}}{2} + \frac{\Delta_{R0}}{2}$$
$$V_{in}^{-} = V_{CM,in,R0} + \frac{V_{th}}{2} - \frac{\Delta_{R0}}{2}$$

Definitions region ϕ_{R2} (positive threshold: V_{in}^{+}-V_{in}^{-} > 0)

$$V_{in}^{+} = V_{CM,in,R2} + \frac{V_{th}}{2} + \frac{\Delta_{R2}}{2}$$
$$V_{in}^{-} = V_{CM,in,R2} - \frac{V_{th}}{2} - \frac{\Delta_{R2}}{2}$$

Where $V_{CM,in}$ is the common-mode of the inputs (which is the output common-mode level of the S/H) in each region. Δ_{R0} and Δ_{R2} is the difference between the actual threshold and the ideal threshold in each region (the additional input that is required to trip the comparator threshold).

It can be shown that the effective threshold in each region is given by (3.9).

$$
\begin{aligned}
&V_{th,R0} = -V_{th} + \Delta_{R0} \cong V_{ref,err}\left(-1+\frac{\Delta_1-\Delta_2+\Delta_3}{4}\right) \\
&+ V_{th}\frac{\Delta_1-\Delta_2+\Delta_3}{2} + \left(V_{CM,ref} - V_{CM,in,R0}\right)\frac{\Delta_1+\Delta_2-\Delta_3}{2} \\
&+ 2V_{cmpoffset} \\
&V_{th,R2} = V_{th} + \Delta_{R2} \cong V_{ref,err}\left(1+\frac{\Delta_1-\Delta_2+\Delta_3}{4}\right) \\
&+ V_{th}\frac{\Delta_1-\Delta_2+\Delta_3}{2} - \left(V_{CM,ref} - V_{CM,in,R2}\right)\frac{\Delta_1+\Delta_2-\Delta_3}{2} \\
&+ 2V_{cmpoffset}
\end{aligned}
\tag{3.9}
$$

The difference between the two thresholds is given by (3.10).

$$
\begin{aligned}
&\Delta x = V_{th,R2} - V_{th,R0} \cong 2V_{th} + 2V_{ref,err} - \\
&\left(2V_{CM,ref} - V_{CM,in,R2} - V_{CM,in,R0}\right)\frac{\Delta_1+\Delta_2-\Delta_3}{2}
\end{aligned}
\tag{3.10}
$$

In (3.10) it can be observed that the main source of error in the difference between the thresholds is given by the error in the reference voltages. The different common-mode levels also introduce an error but it is expected to be much smaller than the resolution of the ADC. For example, if the difference in common-mode levels is 10mV and with 0.1% resistor mismatch then the resulting error is in the order of 5μV. This can be compared with 1 LSB of the ADC which is 125μV. 0.1% resistor mismatch can be achieved on-chip with careful layout and by increasing the layout area of the resistors. Since there is

only one calibration comparator in the entire ADC, the area occupied by its resistors is a negligible fraction of the entire ADC area.

The error in the reference voltages must be estimated, because this error is expected to be greater than the resolution of the ADC. This error can be estimated with a very low power and area sigma-delta A/D converter. Since the reference voltages are DC, the clock speed of this ADC can be in the kHz range and still have an almost infinite Over-Sampling-Ratio (OSR) and therefore have a resolution that is higher than the resolution of the pipeline ADC. The sigma-delta A/D converter for this prototype chip was not implemented on-chip but its power consumption is estimated to be about 0.1% of the total ADC power consumption [37].

When the real switches at the input of the calibration comparator are introduced, it can be noted that the R_{ON} of these switches can be incorporated into R in Fig. 3.11 and the above discussion still holds true. However two of the switches operate with a larger V_{GS} than the other two and will therefore have a different R_{ON} than the other two (see Fig. 3.12). This difference in R_{ON} will add to the mismatch Δ parameters. This difference in R_{ON} can be minimized by placing the two thresholds close together (for example $V_{th}=V_{ref}/8$, which can be compared to the regular stage comparators which have $V_{th}=V_{ref}/4$). There is a lower bound on how close the thresholds can be, based on $V_{cmp,offset}$ and the expected non-idealities in the MSB stage (to avoid overshoot). Although the R_{ON} can have a large range across the entire input range, it is only when

the input is close to the comparator thresholds that performance of the comparator is critical, and effectively there are therefore only two discrete V_{GS} values for the switches (see Fig. 3.12).

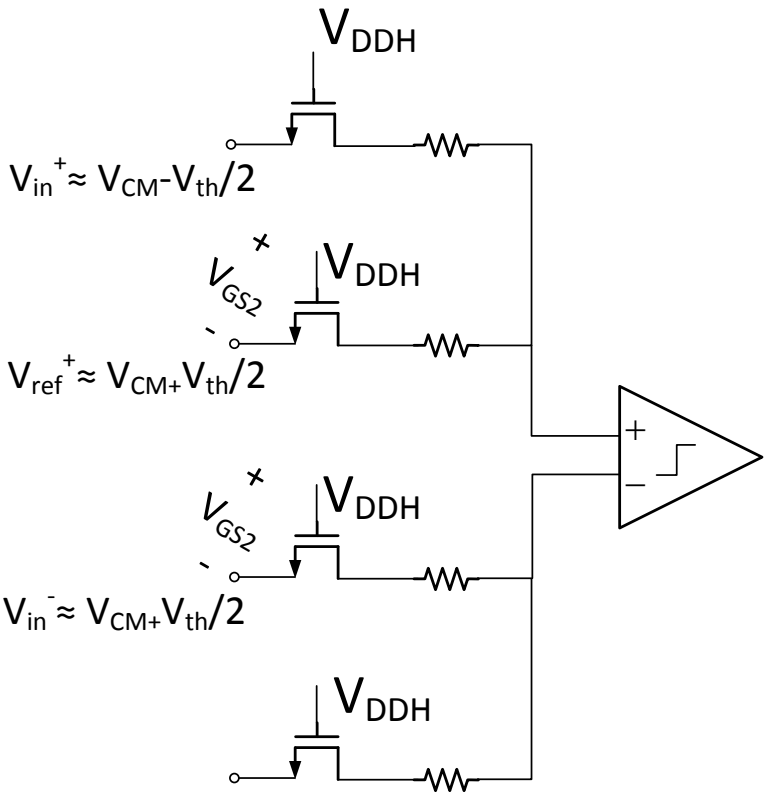


Fig. 3.12 V_{GS} of switches (region R0 shown, similar for R2)

The on-resistance for a switch can be expressed as in (3.11).

$$R_{ON} = \frac{1}{\mu\ C_{ox}\frac{W}{L}(V_{GS} - V_t)} \tag{3.11}$$

From Fig. 3.12 it is observed that $V_{GS1}=V_{GS2}+V_{th}$ and the difference between the two R_{ON} values can be expressed as in (3.12), where R_{ON2} corresponds to the on-resistance of the switches operating with V_{GS2}.

$$\begin{aligned}\Delta R_{ON} &= \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS2} - V_t)} - \frac{1}{\mu C_{ox}\frac{W}{L}(V_{GS1} - V_t)} \\ &\approx \frac{V_{th}}{(V_{GS2} - V_t)} R_{ON2}\end{aligned} \tag{3.12}$$

With $V_{th} = V_{ref}/8$, $V_{ref}=1V$ and with a thick-oxide device with a $V_{DDH}=2.5V$ gate voltage, the ΔR_{ON} is roughly around 10% of R_{ON2}. With a nominal value of $R_{ON2}=50\ \Omega$, the ΔR_{ON} is roughly 5Ω. With $R=10k\Omega$, this is about 0.005% mismatch. It can also be noted in Fig. 3.12 above that for any given switch, its V_{GS} is the same for both regions of operation, so its R_{ON} does not change with region of operation, and therefore the Δ parameters do not change with region of operation either, which is one of the assumptions for the expressions in (3.9) and (3.10). It can also be noted that another choice for the input switched for the calibration comparator is the use of boot-strapped switches, at the cost of additional area and increased loading of the S/H.

A large R is preferred to minimize the effect of R_{ON} of the switches. In general, a large resistor can produce a large thermal noise, but the impact of this thermal noise depends on the bandwidth of the system of interest. For this system (the comparator), there are only two samples of interest, $V_{in}=\pm V_{th}$ (other input values are ignored by the non-linear latch) and the bandwidth can therefore practically speaking be said to be zero (there is no sampling operation).

3.3.3 Layout Considerations for the Calibration Comparator

A block diagram view of the calibration comparator and related blocks is shown in Fig. 3.13. The line resistance between the Sample & Hold and the calibration comparator, $R_{line,\ Cal.\ comp}$, should be matched to the line resistance between the reference generator and the calibration comparator, $R_{line,\ Vref}$, because these resistances can then be incorporated into R and no additional error term is introduced. This can be achieved by using metal lines of the same width, length and metal layer. The matching is however not critical because the absolute value of the line resistance is expected to be small. Note that $R_{line,\ S/H}$ should be minimized by connecting the lines that go to the calibration comparator as close as possible to the S/H output.

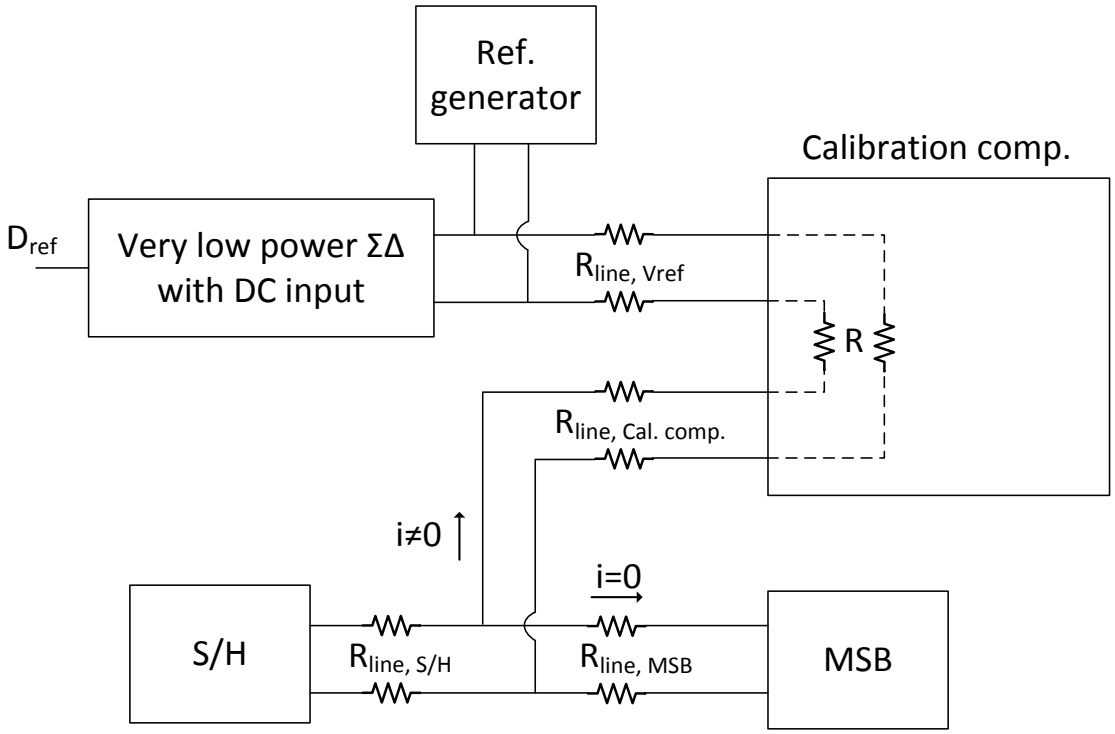


Fig. 3.13 Block diagram with metal wire resistance.

At the end of the sampling phase of the MSB stage, there is no current flowing into this stage, but there is current flowing into the calibration comparator, and therefore also through $R_{line, S/H}$. This current depends on the value of the output of the S/H and creates an input dependent voltage drop across $R_{line, S/H}$. Effectively, the MSB stage is therefore not sampling the output of the S/H but the actual S/H output minus the voltage drop across $R_{line, S/H}$. Although this voltage drop is a linear function of the input, it has a different sign in the two regions of operations and would complicate the calibration

algorithm. However, $R_{line,\ S/H}$ can easily be made as small as a fraction of an Ohm in the layout and will not introduce errors in practice.

Using a large R in the calibration comparator minimizes the current flowing through any residual $R_{line,\ S/H}$ that may be present in the layout, and it relaxes the design specifications for the S/H amplifier, which drives this resistive load.

3.4 Design of ADC Building Blocks

This section describes the circuit level implementation details and design choices of the ADC building blocks. Simulations results for the S/H circuit are presented as well as additional layout considerations for the ADC and its components.

The analog power supply is 2V, which is higher than the recommended supply voltage of 1.2V of the core devices. The higher power supply allows for higher signal swing and single-stage amplifier topologies. Cascode structures are used throughout the chip to limit the gate-source, gate-drain and source-drain voltages to less than 1.2V for all core devices. High voltage thick-oxide devices are also used in key positions in the analog design.

Cascode current mirrors are used throughout the chip for increased accuracy. The amplifier biasing circuitry is distributed across the chip, rather than based from a single

biasing current. Amplifier DC gain is designed to be high enough for all process coroners to ensure the required linearity at the amplifier output.

3.4.1 Sample and Hold Topology

Shown in Fig. 3.14 is the Sample and Hold (S/H) stage, commonly referred to as the flip-around S/H. Each capacitor has a value C=4pF. Since the errors from S/H are not corrected for, any distortion created by this block will appear in the ADC output after calibration. Boot-strapped switches [38] are employed at the input, see section 3.4.5. The common-mode level $V_{CM,in}$ is generated and buffered on-chip and then distributed across the ADC, see section 3.4.6.

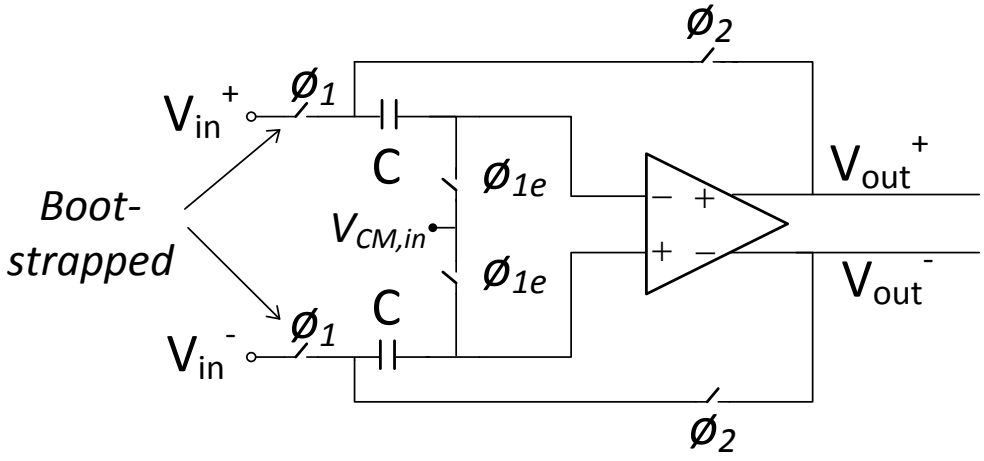


Fig. 3.14 Flip-around S/H topology.

The two-stage amplifier for the S/H is shown in Fig. 3.15, and was chosen for its ability to provide large DC gain, GBW and the ability to drive the resistive loading. It is also robust across process corners.

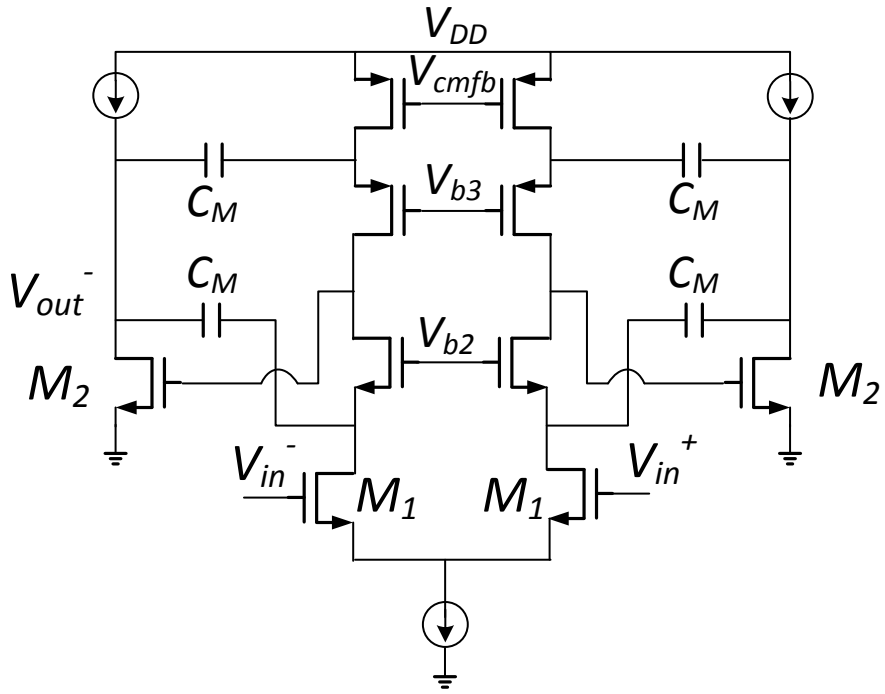


Fig. 3.15 S/H amplifier.

The S/H amplifier uses Miller frequency compensation with C_M=0.5pF. NMOS input differential pair was chosen to increase the closed-loop gain of the amplifier and to reduce the silicon area and noise. A PMOS input differential pair has lower flicker noise but because of the high transconductance requirement the input referred noise is only a

fraction of an LSB as shown in Table 3.4. A continuous-time Common-Mode-Feedback (CMFB) circuit was used, as shown in Fig. 3.16.

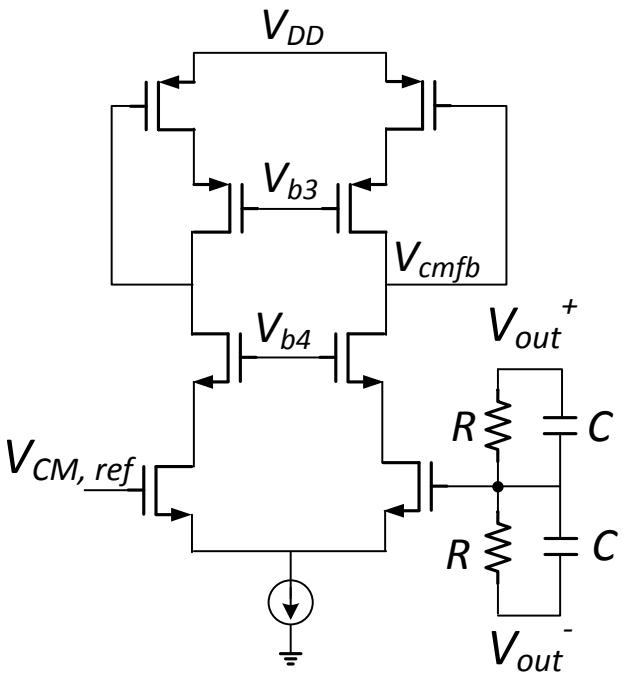


Fig. 3.16 S/H amplifier CMFB circuit.

A switched-capacitor (SC) implementation for CMFB is an alternative [39] but in order to have a good CM control large capacitors are required as CM detectors, which load the amplifier. A continuous-time CMFB implementation occupies a small area and does not load the amplifier and has a better Power-Supply-Rejection-Ratio [7], which is important for high resolution ADCs. The network used as CM detectors use R=15kΩ and C=100fF.

The design parameters for the S/H amplifier are summarized in Table 3.4.

Table 3.4 S/H amplifier parameters.

I_{bias} - stage 1	650μA
I_{bias} - stage 2	3mA
I_{bias} - CMFB	650 μA
(W/L) – stage 1	13μm/0.16μm
(W/L) – stage 2	192μm/0.40μm
DC Gain	80 dB
Phase Margin	66 degrees
GBW	550 MHz (cal. requirement=475 MHz)
Integrated noise up to Nyquist	18μV

The bias current in stage two is much higher than in stage one, in order to push the non-dominant pole to higher frequency for stability reasons. The DC gain is 80 dB, which is high enough to ensure that the linearity of the S/H amplifier is higher than that of the overall ADC. Fig. 3.17 shows the post-layout simulation results for the S/H with a full-scale sinewave input at full sampling rate. As seen in Fig. 3.17, the Fast-Fourier-Transform (FFT) of the S/H output shows an equivalent effective resolution of 15.65 bits. The highest spurious tone is given by the tone at $3F_{in}$-F_s.

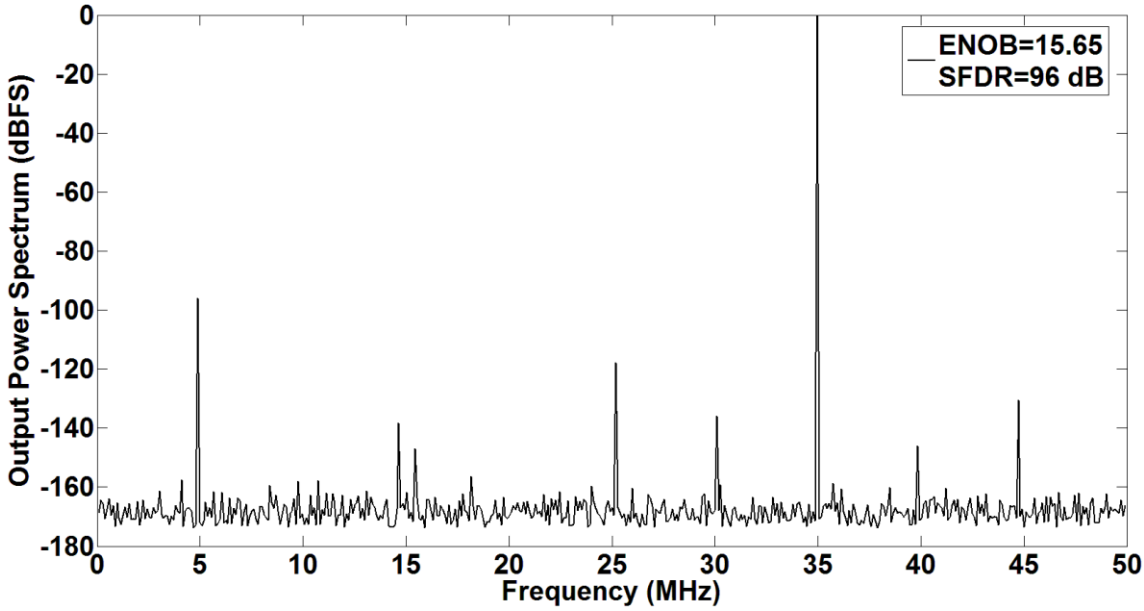


Fig. 3.17 FFT from post-layout simulation for S/H.

3.4.2 Stage Amplifier Topology

The amplifier topology used in the pipeline stages is shown in Fig. 3.18. A telescopic topology with gain boosting amplifiers was chosen to provide a large gain and large GBW. NMOS input differential pair was chosen to increase the closed-loop gain of the amplifier and to reduce the silicon area and noise. A PMOS input differential pair has lower flicker noise but because of the high transconductance requirement, the input referred noise is only a fraction of an LSB as shown in Table 3.5.

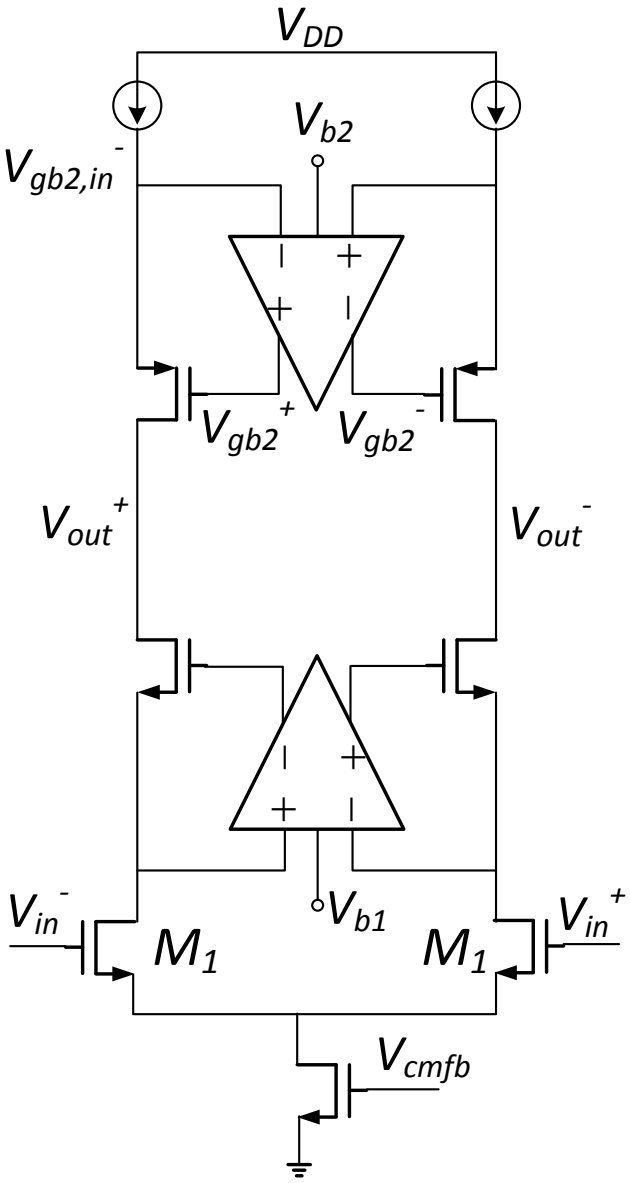


Fig. 3.18 Pipeline stage amplifier topology.

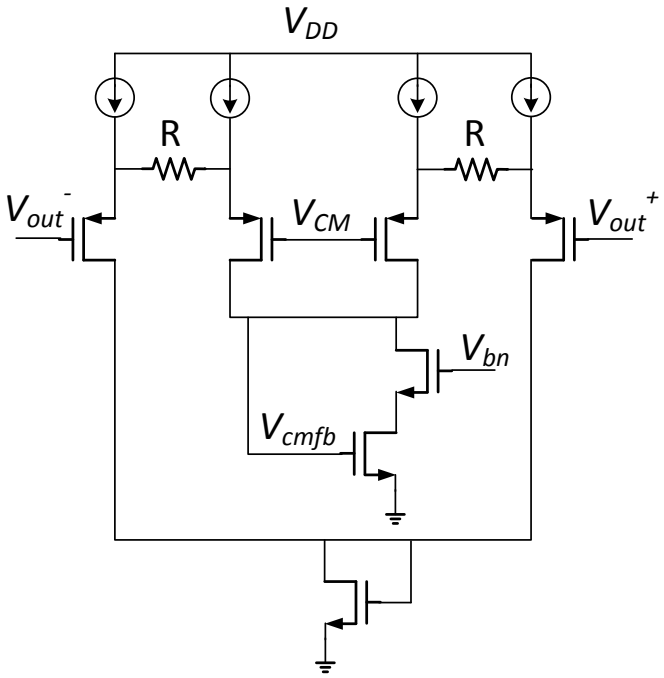


Fig. 3.19 Pipeline stage amplifier CMFB circuit.

A continuous-time Common-Mode-Feedback (CMFB) circuit was used as shown in Fig. 3.19. The resistors in Fig. 3.19 increase the linear range of the CMFB input circuit (R=365Ω for the MSB stage), which operates with a full-scale input. The N-type gain boosting amplifier used in the upper regulated cascode amplifier is shown in Fig. 3.20. The bottom amplifier uses PMOS input pair due to the different common-mode voltage level needed, as shown in Fig. 3.21. The extra device connected to the source of the differential pair set the DC operating point at the drain of transistors M_1 [40]. No separate CMFB circuit for these gain boosting amplifiers is required.

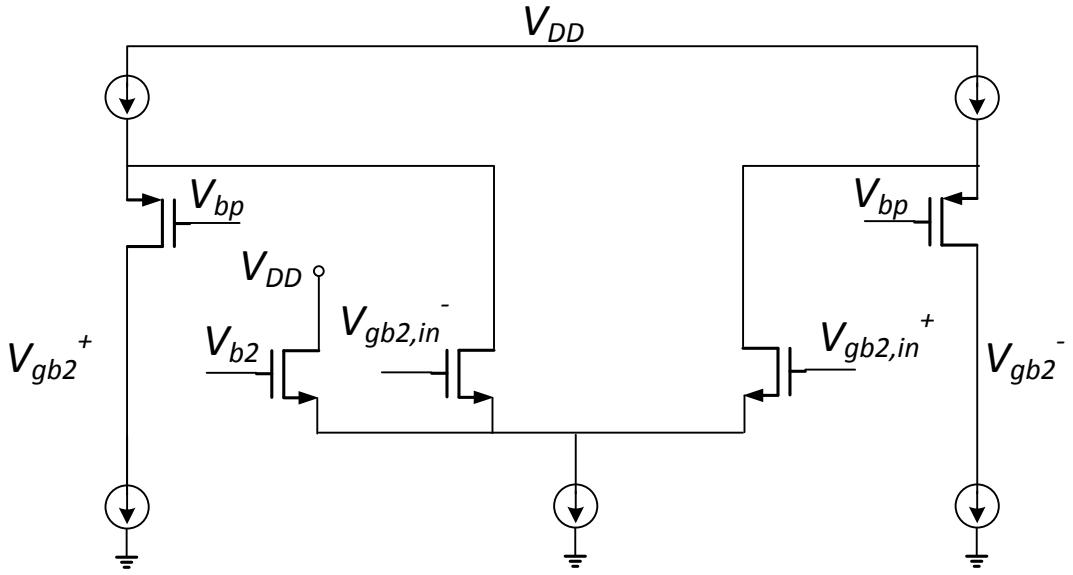


Fig. 3.20 N-type gain boosting amplifier.

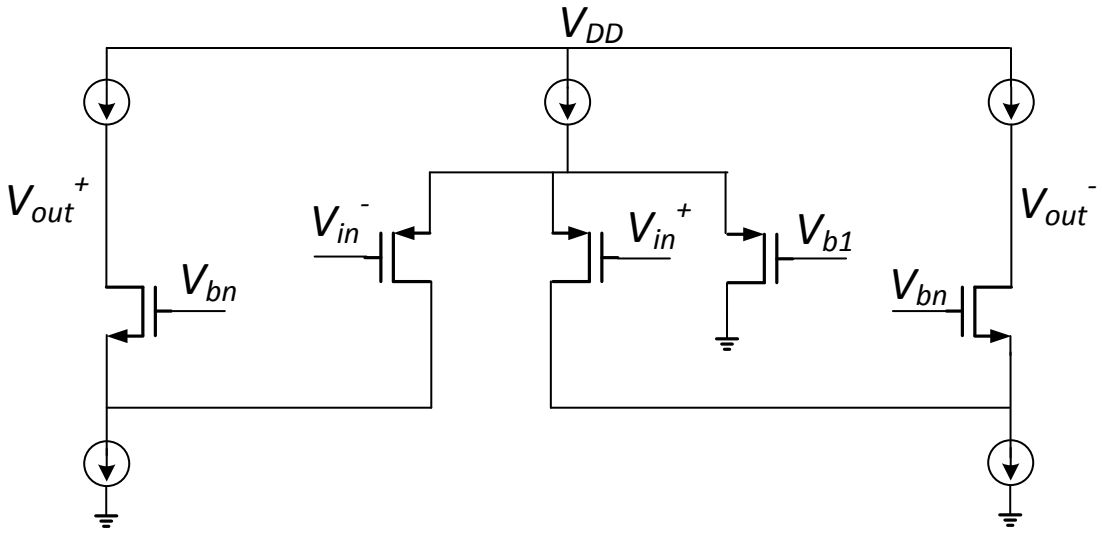


Fig. 3.21 P-type gain boosting amplifier.

The design parameters for the MSB amplifier are summarized in Table 3.5.

Table 3.5 MSB amplifier parameters.

I_{bias} - main/Boosters/CMFB)	5.5mA
I_{bias} - boosters	380μA
I_{bias} - CMFB	2.5mA
$(W/L)_1$	87μm/0.13μm
DC Gain	80 dB
Phase Margin	80 degrees
GBW	1.1 GHz (cal. requirement=950 MHz)
Integrated noise up to Nyquist	18μV

The bias currents of the boosters is only about 7% of the bias current in the main amplifier, which is a very power efficient way to increase the DC gain. The DC gain is high enough to ensure that the linearity of the amplifier is higher than that of the overall ADC. The bias current in the CMFB circuitry is about half that of the main amplifier, which is a reasonable trade-off between power and performance of the CMFB circuit [7].

The bias currents and device sizes scale down by a factor of roughly two for each succeeding stage in the pipeline, while the DC gain, GBW and phase margin remain the

same for each amplifier. A phase margin of 80 degrees ensures stable operation while the speed of the amplifier is higher than the calculated requirement.

3.4.3 *Comparator Topology*

The comparator topology for the pipeline stage comparator is shown in Fig. 3.22. The differential input pair is PMOS with no body-effect to minimize the dependence in the effective threshold on any variation in the common-mode level of the preceding stage output. The comparator's first stage is implemented employing a folded-cascode topology loaded by a P-type current-source and common-mode resistive feedback to avoid the use of a dedicated CMFB. A folded-cascode preamplifier provides inherent level shifting at the output. A second preamplifier is added to increase the total preamplifier gain, see Fig. 3.23, to reduce the kick-back noise effect, which otherwise is severe for the targeted 14-bit resolution ADC. The resistors R provide continuous-time CMFB control at the expense of slight DC gain reduction. R is set at 18kΩ in this design to provide a total gain of 29 dB for both preamplifiers. The gain can be increased by increasing R, but it is noted that a pole is created by R and C_{gd} of the PMOS load, which limits the maximum value of R.

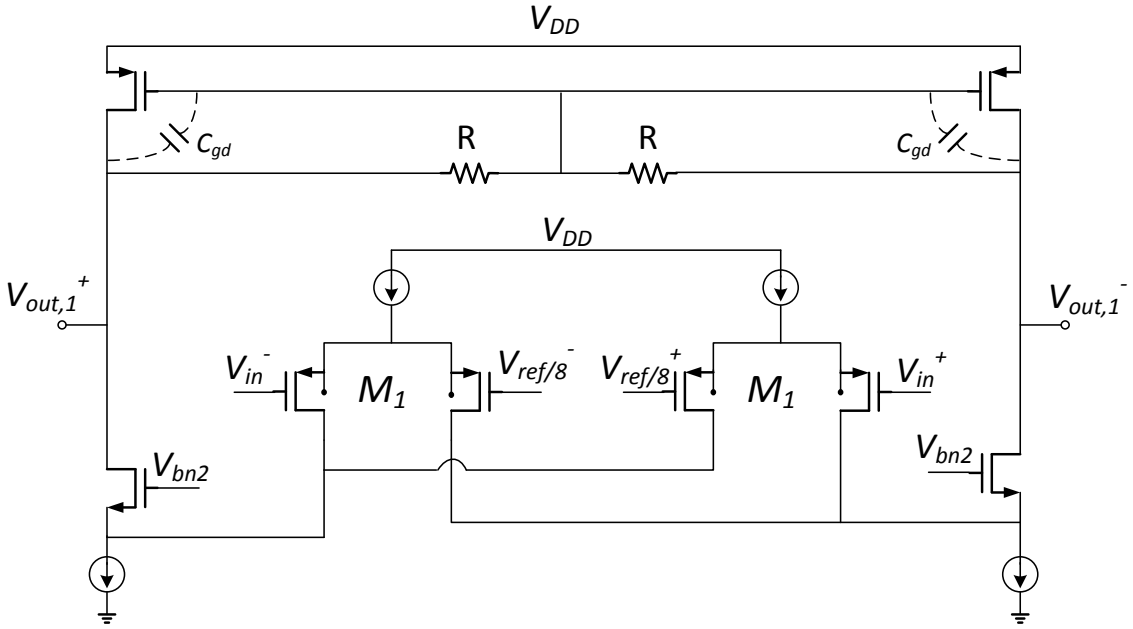


Fig. 3.22 First stage of preamplifier.

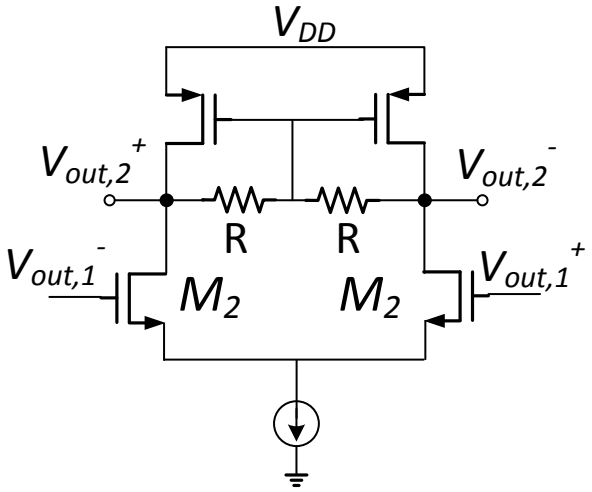


Fig. 3.23 Second stage of preamplifier.

The output of the second stage of the preamplifier is connected to a dynamic latch [41], see Fig. 3.24. The latch operates with a single latch clock and has no static power consumption; it consumes current only during the latching instant. The latch is followed by an SR latch which holds the latch output during the reset phase. The latch operates with a higher digital power supply, to be able to drive the switches in the pipeline stage without level shifting, see next section.

The design parameters for the comparator are summarized in Table 3.6. The bias currents for the comparators are only a fraction of the bias current for the amplifiers in the S/H and the first few stages of the ADC, but because there are two comparators in each pipeline stage, and 16 stages in total, the power consumed by the comparators is a significant portion of the overall ADC power consumption.

The latch regeneration time is only 150ps, which means that only a small fraction of the available settling time has to be devoted to latching, most of the available settling time can be used for amplifier settling.

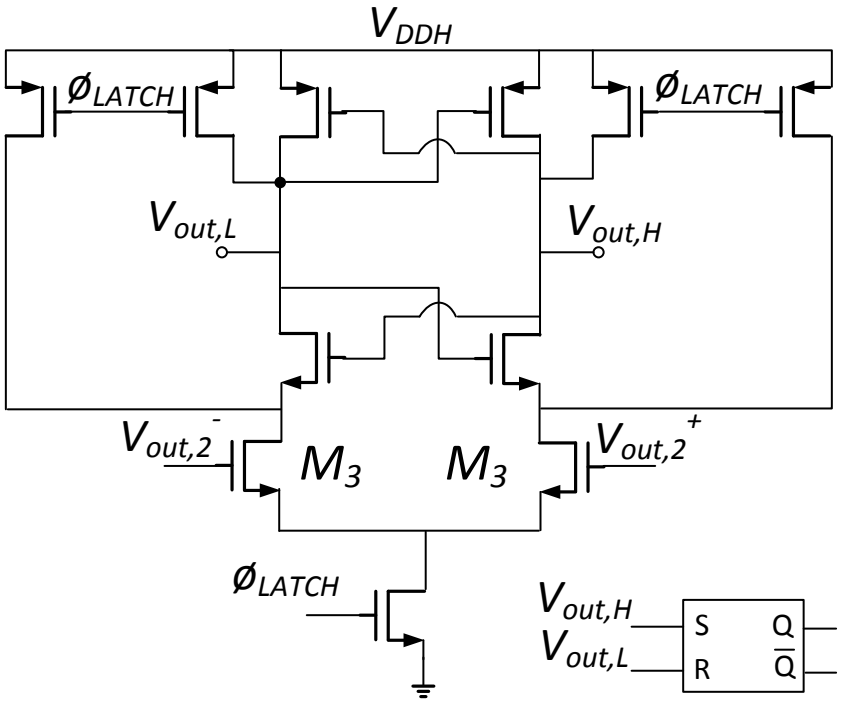


Fig. 3.24 Dynamic latch.

Table 3.6 Comparator parameters.

Ibias – stage 1	200μA
Ibias – stage 2	50μA
$(W/L)_{M1}$	3μm/0.13μm
$(W/L)_{M2}$	0.80μm/0.13μm
$(W/L)_{M3}$	6μm/0.28μm
Total DC Gain (Preamplifiers)	29 dB
Latch regeneration time for 1 LSB input	150ps
Input-referred noise up to Nyquist	50μV

The gain calibration comparator has only two inputs and it has a slightly different first stage configuration, see Fig. 3.25, while the second stage and latch are the same as for the pipeline stage comparator.

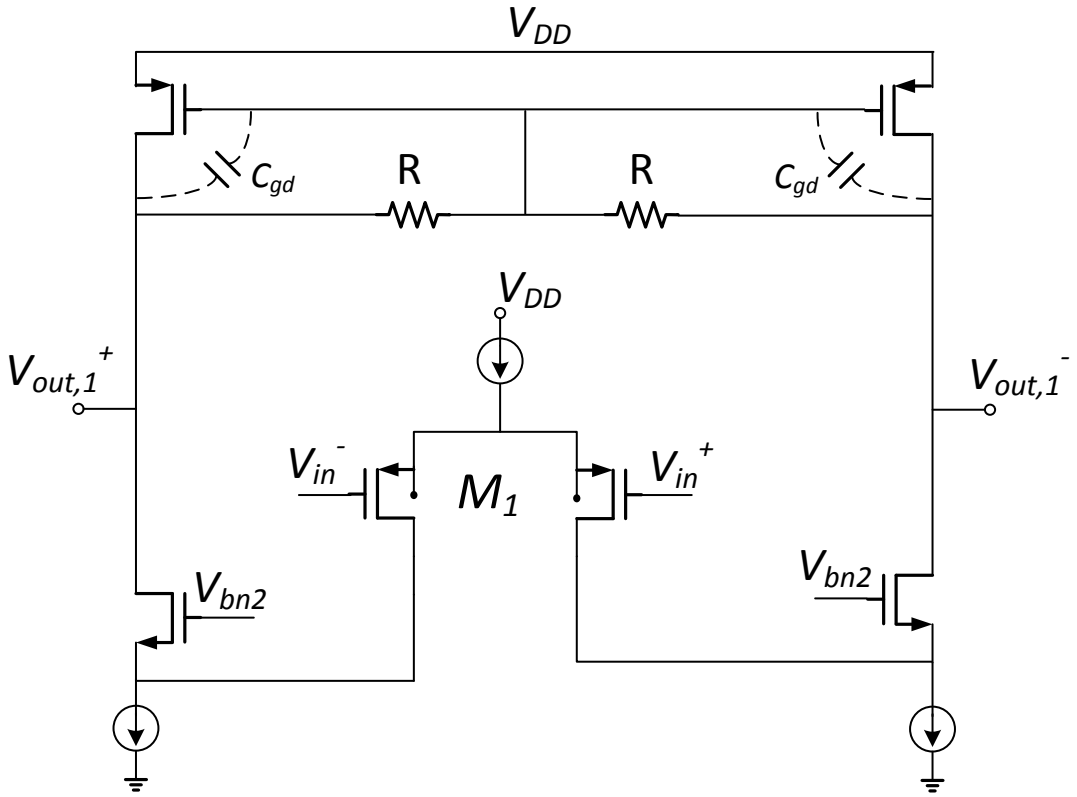


Fig. 3.25 First stage of gain calibration comparator.

3.4.4 Clock-Generation and Switch Design

The switches are implemented as thick-oxide NMOS switches with a 2.5V gate voltage, which for this technology has a smaller on-resistance than a complimentary switch using core-devices, for a comparable parasitic capacitance. Another advantage of this approach is that each switch requires only one clock signal, which facilitates clock signal routing. However, simulations show that the clock-generator, see Fig. 3.26, has a better performance across process corners when implemented with 1.2V core devices. The amount of non-overlapping and the early clocks have less spread across process corners with core devices, which is important because the more time for the non-overlapping time and the early clocks, the less time is available for settling for the amplifiers.

The clock generator, see Fig. 3.26, is implemented with cross-coupled NAND gates to generate non-overlapping clocks. Dummy NMOS and PMOS devices added to the clock lines increase the non-overlapping and early-clock times. Extra devices right before the final buffers ensure that all clock outputs rise at the same time instant.

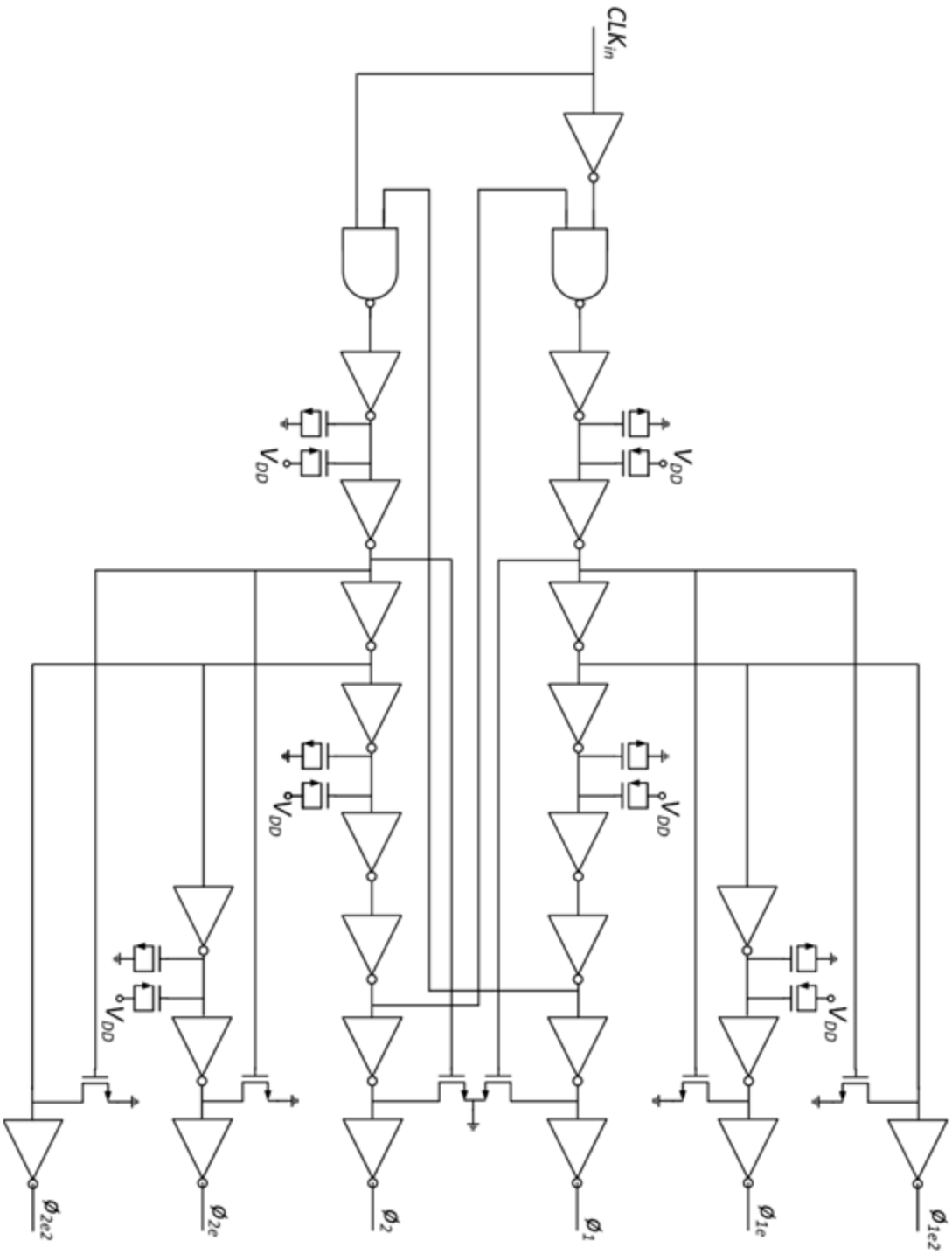


Fig. 3.26 Clock generator.

On-chip level shifting is implemented to produce the 2.5V clock signals from the 1.2V clock signals. The level shifter is shown in Fig. 3.27, which is an extension of the level shifter in [42]. The signal amplitude at the gate of the output stage devices is a function of the ratio between the capacitors and the parasitics at the gate and to have enough amplitude, the capacitors in the clock level shifter are 100fF each. The amplitude of the signal at the nodes at the left of the level shifter is not important, and hence the capacitors at these nodes can be minimal size. These capacitors can be MOS capacitors, which occupy a smaller area than Metal-Insulator-Metal (MIM) capacitors.

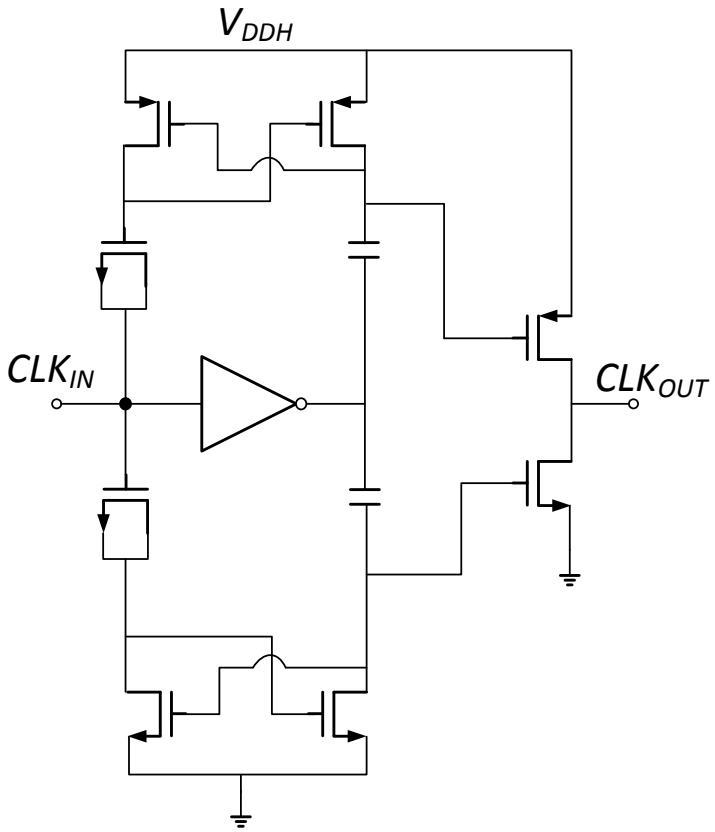


Fig. 3.27 Level shifter.

3.4.5 Boot-Strapped Switch

The input switch of the S/H circuit is shown in Fig. 3.28 [38].

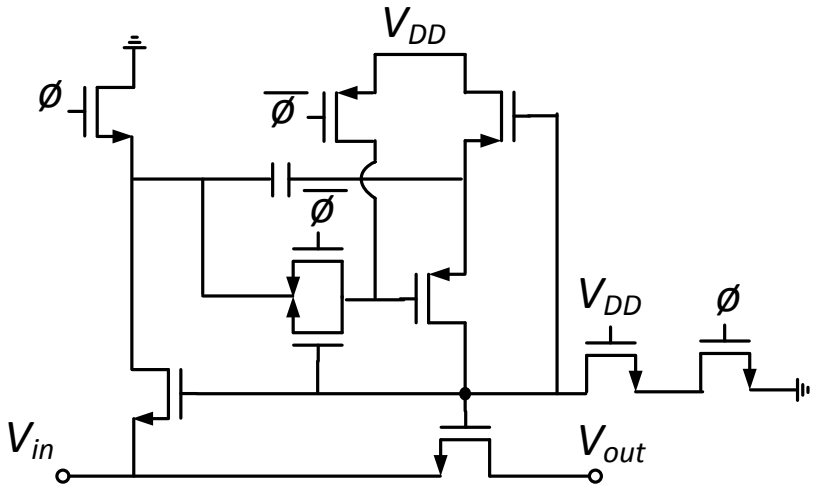


Fig. 3.28 Boot-strapped switch.

The boot-strapped switch in Fig. 3.28 uses only one capacitor, unlike the conventional boot-strapped switch [42] which uses three, and therefore requires a larger area. The switch in Fig. 3.28 is designed for maximum reliability because the V_{GS}, V_{GD} and V_{DS} for any device is always less than or equal to V_{DD}. The capacitor has a value of 1pF. The switch in Fig. 3.28 has been verified in simulations to have the same performance as the conventional switch in [42], and was therefore chosen for this ADC. Both switch designs operate on the same principle; a capacitor is first charged to V_{DD} in one clock phase, and in the next, it is applied between the source and the gate of the NMOS pass device, so

that the effective V_{GS} of the pass device is very close to V_{DD} for all input samples. This technique linearizes the switch and reduces its on-resistance. This also prevents an input dependent sampling instant, which is a large source of non-linearity. With this switch, the sampling instant is not a function of the input signal. Clock jitter however will limit the effective resolution of the sampling network. The maximum clock jitter for an ADC for a given resolution N and input signal bandwidth f, is given by (3.13) for a full-scale input.

$$\text{jitter}_{\text{RMS}} = \frac{1}{2^{N}\pi f} \tag{3.13}$$

For a Nyquist 14-bit ADC operating at 100MS/s with a full-scale input, the maximum jitter is about 400fs RMS.

3.4.6 Input CM Voltage Reference Generation and Buffering

Shown in Fig. 3.29 is the input common-mode voltage reference generation and buffering circuit. The input common-mode voltage is process corner dependent and must therefore be generated on-chip. The error amplifier and the corresponding NMOS pass device are connected in an internal control loop for increased stability. The output voltage is mirrored into an output stage with a high current capability to provide for very low output impedance and fast settling. The current in the output stage is about 1mA while the current in the internal loop is about 100μA.

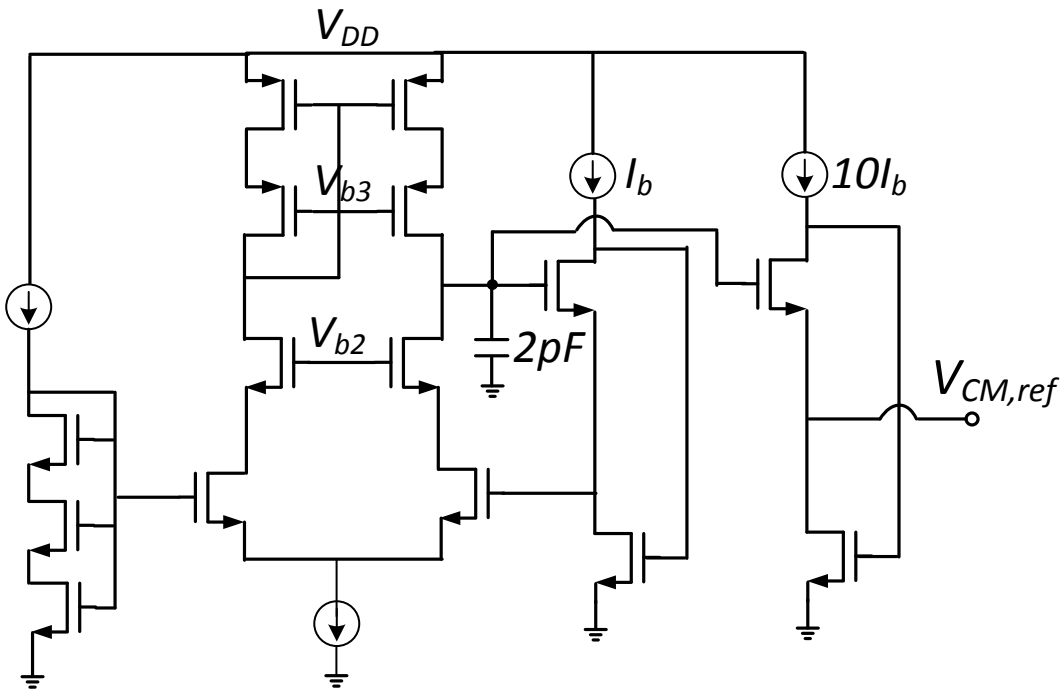


Fig. 3.29 Input common-mode voltage reference generation and buffering circuit.

3.4.7 Clock Front-End Circuit

It is difficult to generate a low-jitter, high-frequency square-wave as clock input to the ADC. Therefore, the ADC clock input is a sine-wave and it is converted into a square-wave by the circuit shown in Fig. 3.30, [43]. The circuit compares the input sine-wave with $V_{DD}/2$ (provided by the matched resistors, which operate as a voltage divider) and produces a high and a low output level. The two inverters then produce a rail-to-rail square-wave.

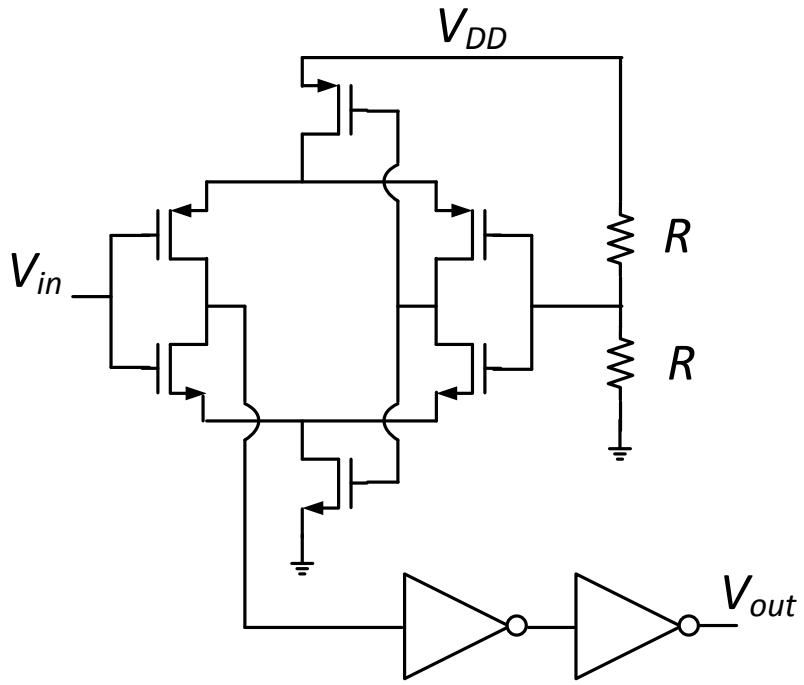


Fig. 3.30 Clock front-end circuit.

3.4.8 Layout Considerations

The layout of a high-speed, high-resolution ADC is critical, especially clock synchronization. The clock must be well synchronized throughout the chip; if the sampling clock of one stage goes low after the hold clock of the preceding stage goes low, then the pipeline stage will sample the common-mode voltage of the preceding stage and the signal propagation is then interrupted. Early clocks and non-overlapping must also be guaranteed throughout the chip. The layout should be as symmetrical as possible. The delay from the clock generator to one part of the chip should be the same

as for another part of the chip. Therefore, the clock generator should be placed in the middle of the chip and the lock lines routed with equal length and metal layer. If the distance from the clock generator to the pipeline stage is very long, then buffers may be required on the clock lines to refresh the clock signal along the way. However, post-layout simulations with all parasitics extracted show that for the layout of this ADC, the clock lines do not require buffers. Another critical issue is the side-wall capacitance between two parallel metal lines, if they are not spaced far enough apart. This capacitance will increase the delay for the clock line and may require the use of clock buffers. For this design however, the clock lines are spaced sufficiently far apart that this capacitance is negligible.

Another critical issue is that clock synchronization should be ensured at the gate of the switches in the pipeline stages. Therefore, not only should the clock bus be synchronized, but the delay of the clock buffers that drive the switches should also be matched. Since the switches scale down for each pipeline stage, this becomes a difficult task since as large buffer with a large load may have a different delay from a scaled buffer with scaled load. Dummy loads may be required to ensure proper delay. Since early clocks and non-overlapping is critical, a little extra non-overlap time is added to the clocks to account for any mismatch in the delay between the clock signals.

The clocks are routed as 2.5V signals because the level shifters occupy a large area (due to a low MIM capacitance density and Design-Rule-Check (DRC) rules) and in this

manner, only one level shifter is required per clock signal. The non-overlapping clock generator also occupies a relatively large area, and therefore there is only one non-overlapping clock generator in the chip. Another option, if area permits, is to have a non-overlapping clock generator for each set of four pipeline stages, this will ensure non-overlapping clocks, but post-layout simulation show that non-overlapping is maintained even with only one non-overlapping cock generator in the middle of the chip.

Shown in Fig. 3.31 is the chip microphotograph. As seen in Fig. 3.31, the clock generator is placed in the middle and the 16 pipeline stages are placed symmetrically around it. The S/H is placed close to an input pin, and to the MSB stage. Voltage reference lines run parallel to the pipeline stages in the middle (vertical lines), and all the output bit lines are routed horizontally to the right. Digital output buffers are used to send the digital bits to the output pins and drive test probes, see next section. These buffers generate a large amount of digital noise and they are separated from the analog portion of the chip by the use of a high-resistivity isolation layer.

Decoupling capacitors are inserted between the power supplies throughout the chip. These capacitors are MOS capacitors because of their high density. The purpose of these decoupling capacitors is to suppress transients on the power supply lines, caused by switching activity in the ADC.

The chip package is an 80-pin QFN package. There are a total of 80 pins plus 12 ground pads. The pad pitch is 80 μm. These extra pads are bounded to the QFN package bottom plate ground. This enables the use of short ground bondwires to reduce the bondwire inductance. The bondwire inductance can be approximated as 1nH/mm. The most sensitive pins (differential analog inputs and clock input) are routed to the pins with the shortest bondwires. The clock pin is adjacent to power supply pins for shielding. There are multiple power supply pins in order to reduce the effective bondwire inductance.

All of the comparator output bits are routed to pins in order to have maximum control and flexibility during testing. However, due to a limited number of pins, this limits the number of pins available for reference voltages and power supplies.

The chip top-layout is shown in Fig. 3.32. The process has 8 metal layers and 1 poly layer. Only standard NMOS and PMOS devices are used, no low threshold-voltage devices are used. In order to reduce the line resistance, stacked metal layers are used.

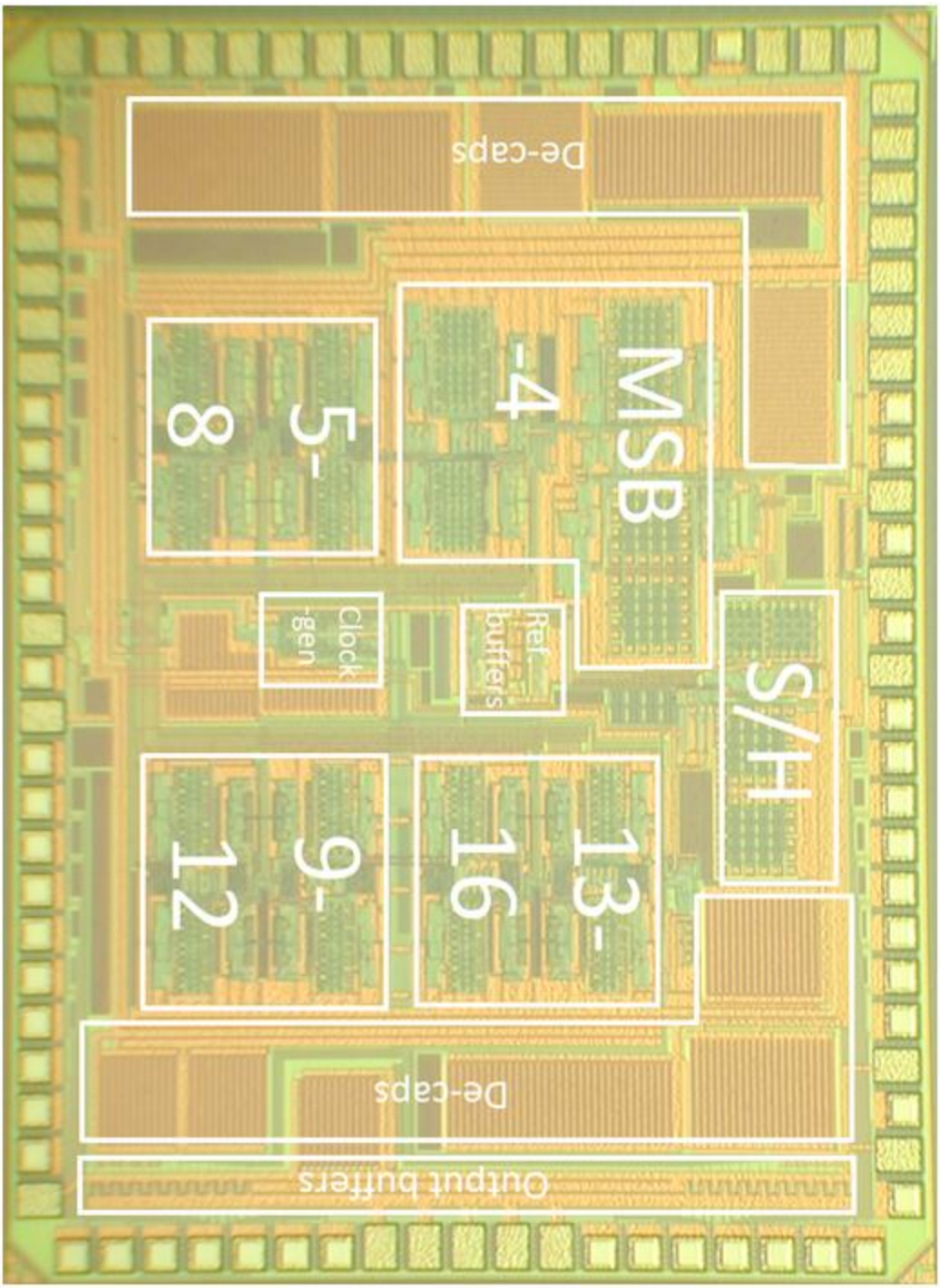


Fig. 3.31 Pipeline ADC chip microphotograph.

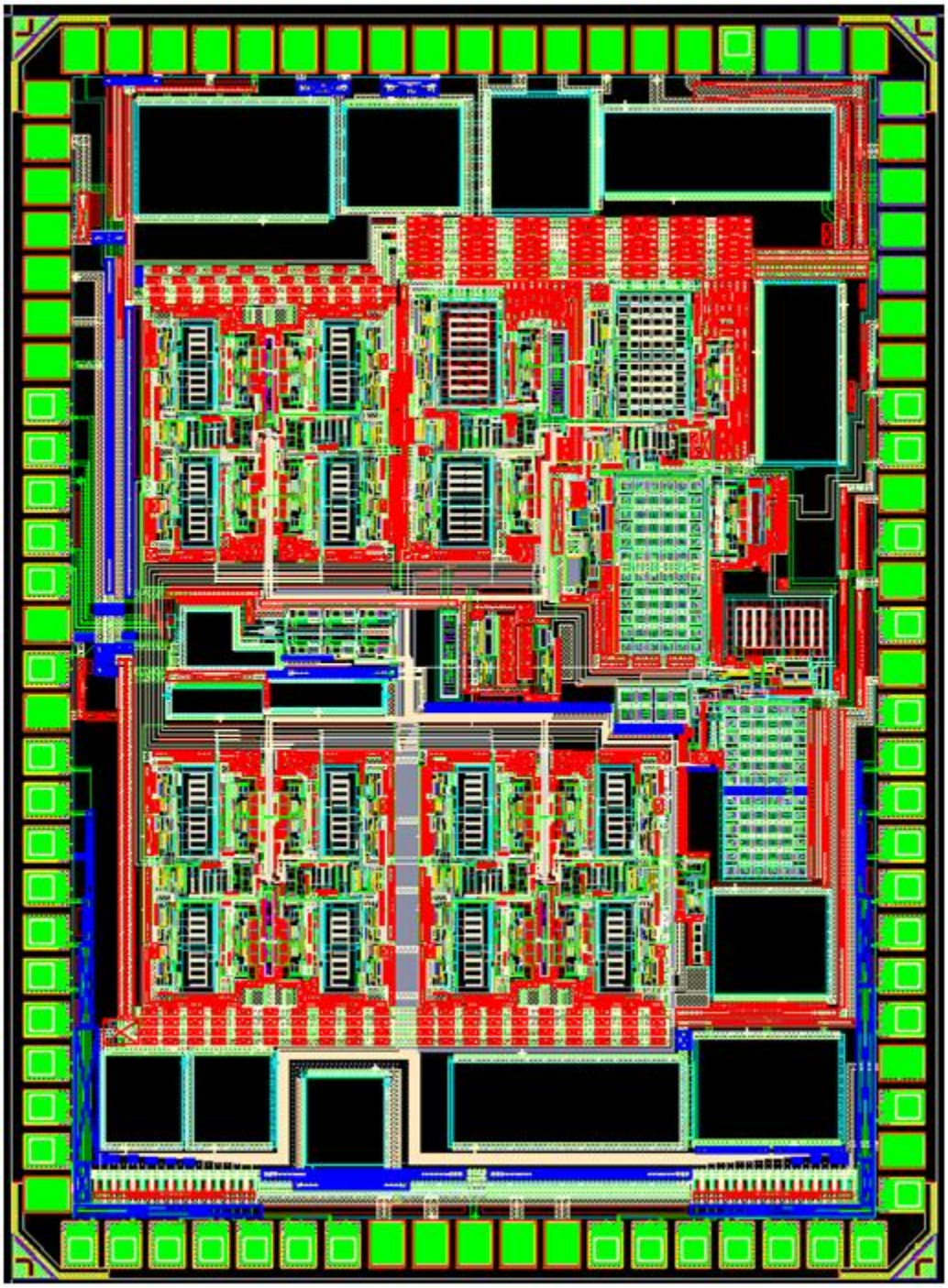


Fig. 3.32 Pipeline ADC chip top-layout.

A more detailed view of the layout of a set of four pipeline stages is shown in Fig. 3.33.

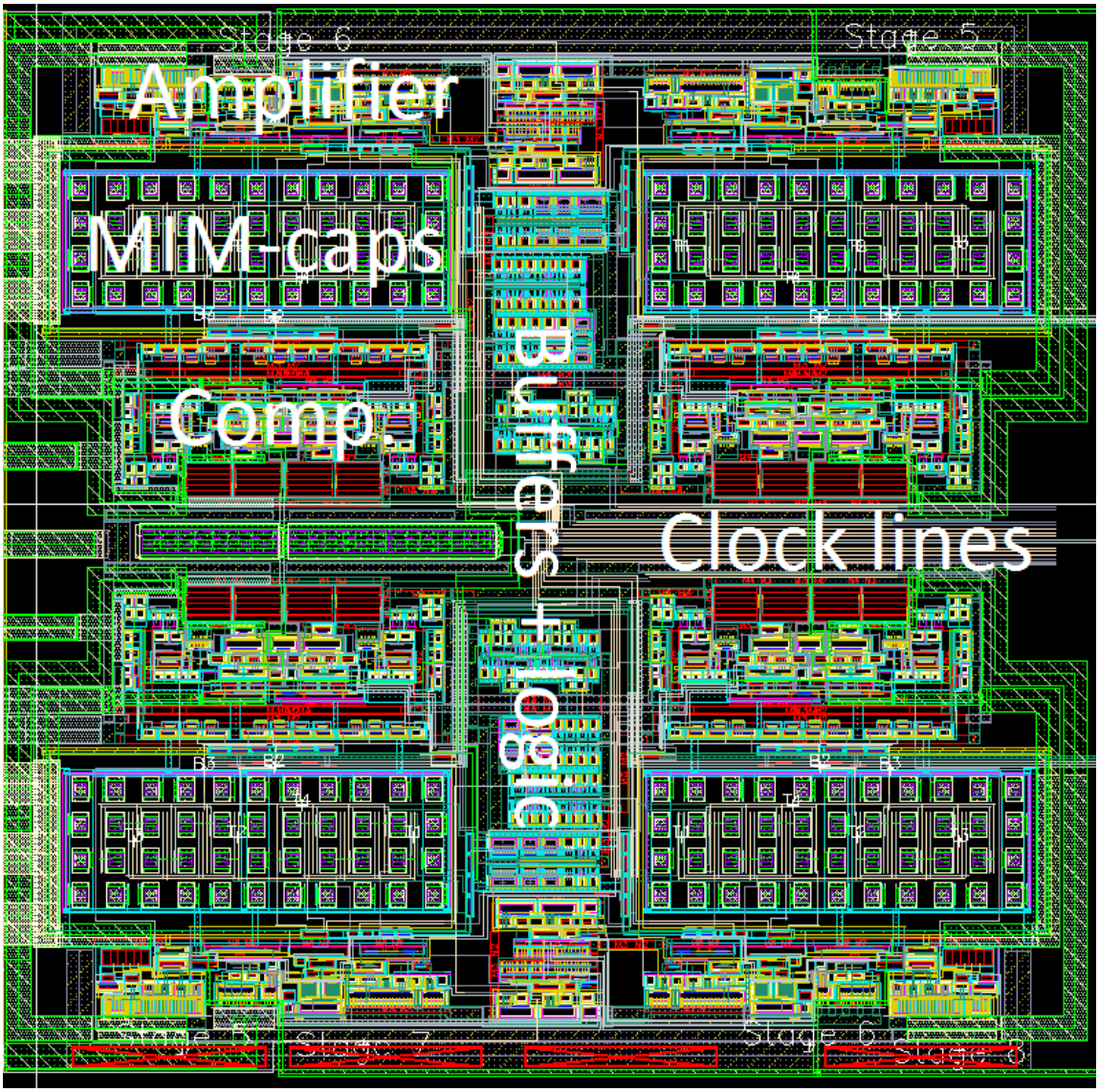


Fig. 3.33 Layout of set of four pipeline stages.

As shown in Fig. 3.33, the capacitors are placed close to the amplifier of each pipeline stage to minimize routing and noise coupling. The capacitors use about half the area of the pipeline stage. The layout is symmetrical with respect to a central line in the middle. Clock lines run in the middle from the central clock generator and are divided symmetrically between the upper and bottom half of the pipeline stages. All the clock buffers and logic are placed in the middle. Wide power lines run on all sides of the pipeline stages.

3.5 PCB Design and Description of Characterization Technique

The ADC has been characterized with the use of a Printed-Circuit-Board (PCB). The design of the PCB is a critical part of the ADC characterization; the performance should ideally be limited by the silicon performance and not the board itself.

High performance ADCs are in general sensitive to power supply noise and clean power supplies are crucial for good performance. Voltage regulators with capacitors at the output provide the power supply for the ADC, see Fig. 3.34. The capacitors are of different sizes and types (aluminum and ceramic) to ensure good performance across a wide range of frequencies. The DC value is set by a resistors divider in the internal voltage regulator loop. A potentiometer is used to change the DC value by a small amount, for fine tuning. Different types of voltage regulators are used, depending on the DC output value, as the minimum output value of a given regulator depends on its

internal reference voltage. The power supply for these regulators is also regulated by on-board regulators.

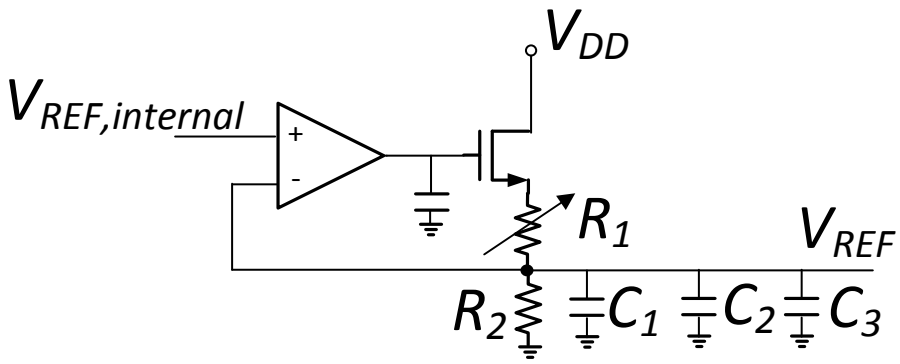


Fig. 3.34 On-board voltage regulator.

The design of the PCB is shown in Fig. 3.35. Besides voltage regulators and bias currents generation for the chip, there is an on-board crystal oscillator, a low-noise, low-distortion, high-bandwidth single-ended to differential input signal driver, components for the logic analyzer and a bandpass filter.

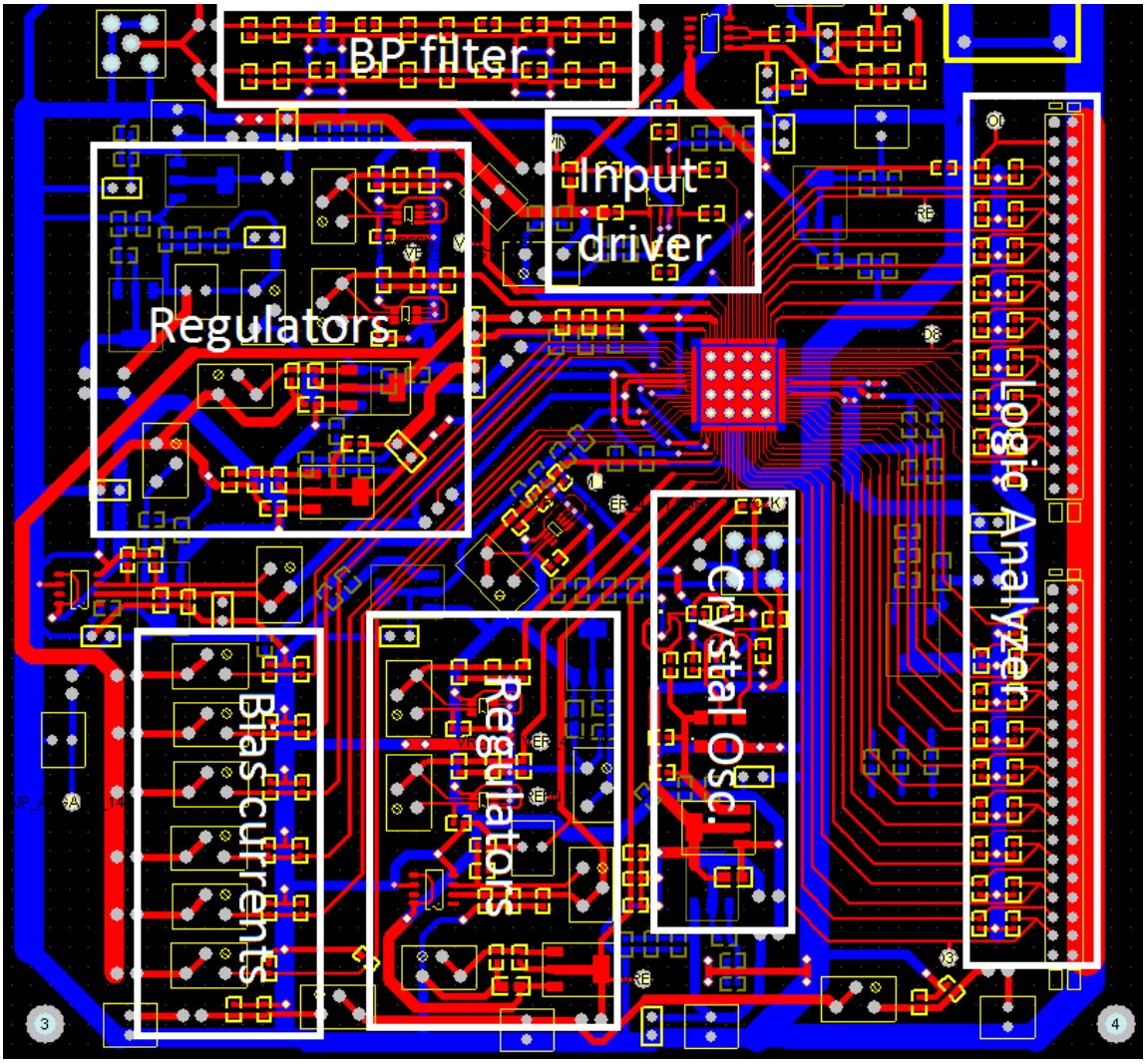


Fig. 3.35 PCB design.

The on-board crystal oscillator circuitry is shown in Fig. 3.36. A low-noise BJT amplifier is used as level shifter, to generate an input clock signal from 0-1.2V for the chip. The crystal oscillator has low jitter according to the datasheet but it is sensitive to power supply noise and even with regulated power supply, the performance of the

crystal oscillator was not adequate. A signal generator was instead used for clock generation, see next section.

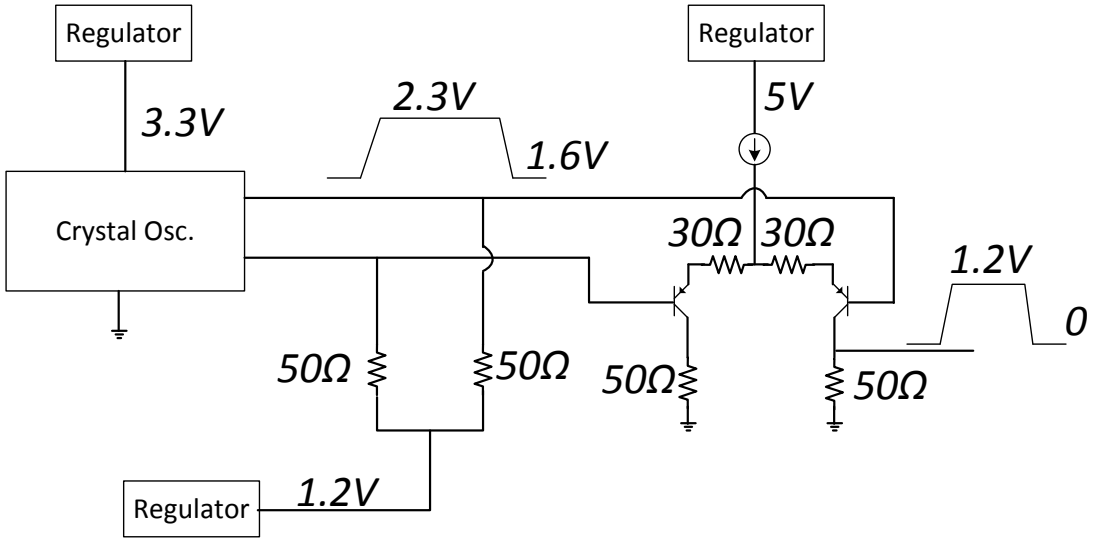


Fig. 3.36 On-board crystal oscillator circuitry.

An on-board 10th order Chebyshev I LC-ladder bandpass filter was designed to filter out the harmonics of the input signal. However, the filter was not very linear (probably due to not very linear inductors) and its effective attenuation of the harmonics was small. Therefore, a stand-alone passive bandpass filter was used to filter the input, see next section.

The digital output bits are captured by a logic analyzer. According to the datasheet, the amplitude of these output signals must be > 500mV$_{pp}$. The output buffers and PCB setup

for the digital output bits are shown in Fig. 3.37. There is one buffer for each digital output bit. The logic output levels are V_{DD}=2.5V and V_{DD}-5mA*150Ω=1.75V, and the logic analyzer threshold is set in the middle at 2.125V. The 20kΩ resistor limits the rise and fall time of the digital signal at the gate of the NMOS device, which reduces the amount of ringing in the output node caused by the bondwire.

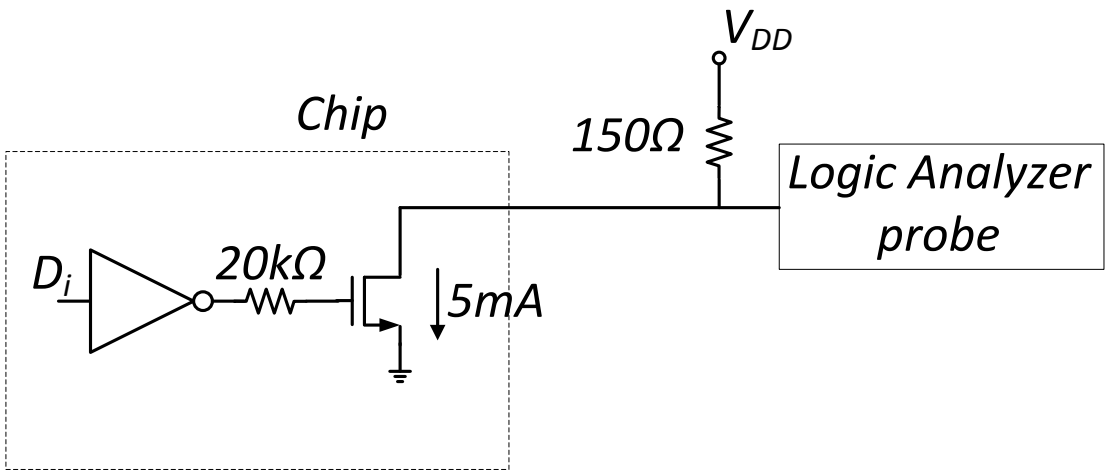


Fig. 3.37 Digital output buffer.

The general setup for the characterization of the ADC is shown in Fig. 3.38. The input signal generators generate large distortion and noise and these effects are difficult to filter out completely. Therefore, the ADC performance is characterized with a two-tone test by combining two input sine-waves. The power combiner is resistive based and is highly linear. The digital output bits were captured with a Logic Analyzer and exported to Matlab for post-processing

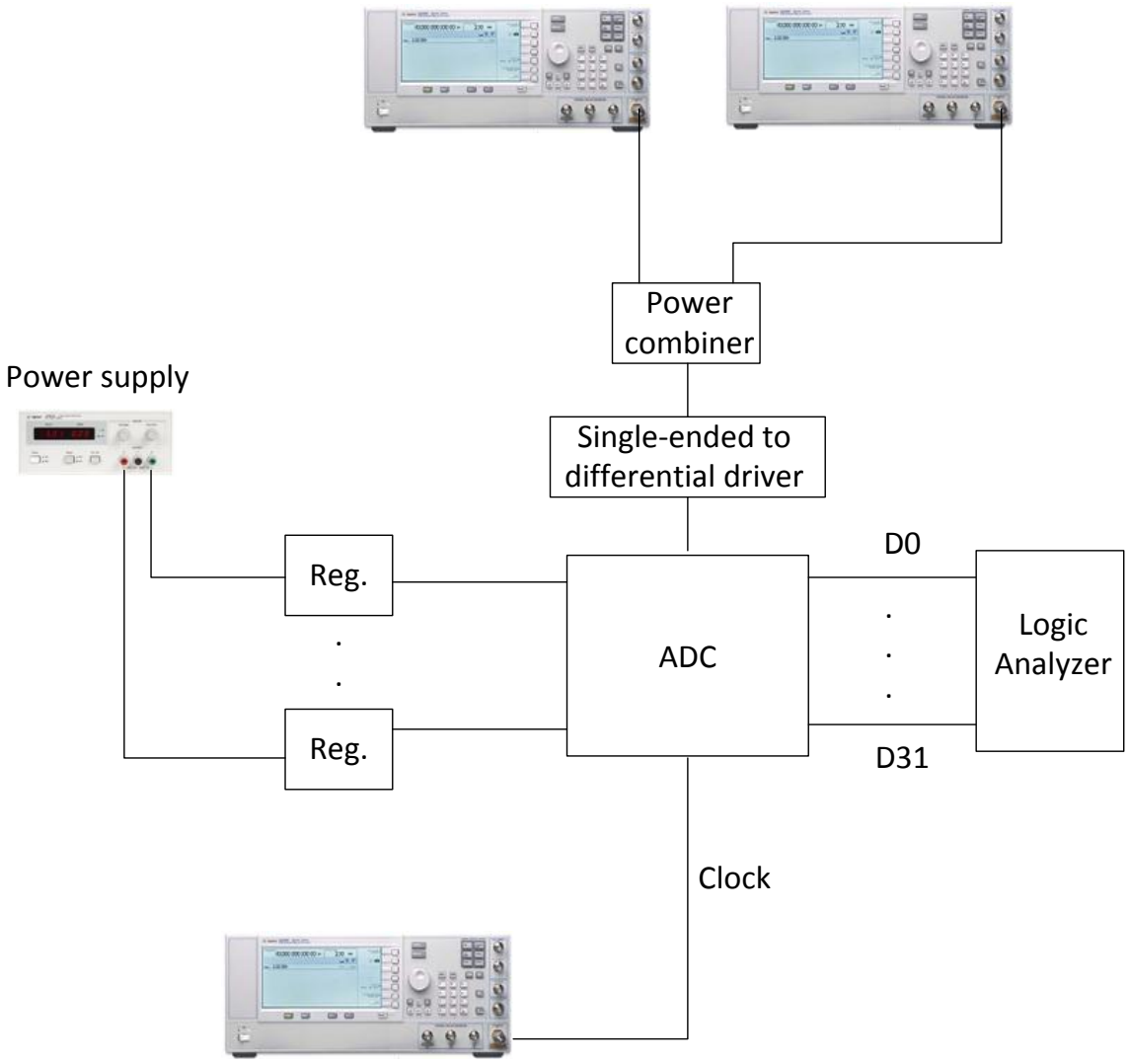


Fig. 3.38 Characterization setup.

3.6 Experimental Results

This section presents the experimental results and the ADC performance is analyzed and compared with previously published work.

The ADC was implemented in TSMC 130-nm technology with 2V power supply and a 2.5V digital supply used for boosted clocks. The nominal ADC sampling rate is 100 MS/s. The measured ADC output power spectrum is shown in Fig. 3.39 for the case of P_{in}=-60 dBFS. At this power level, the harmonic components of the signal generator fall in the noise floor after being attenuated by a stand-alone passive bandpass filter. The bandpass filter also reduces the noise contribution of the signal generator. Under these conditions, the Signal-to-Noise-Ratio (SNR) was measured to be 82 dB when a full-scale signal is considered.

The FFT for all the plots in this section are computed by employing the Hanning window, and all post-processing is performed in Matlab.

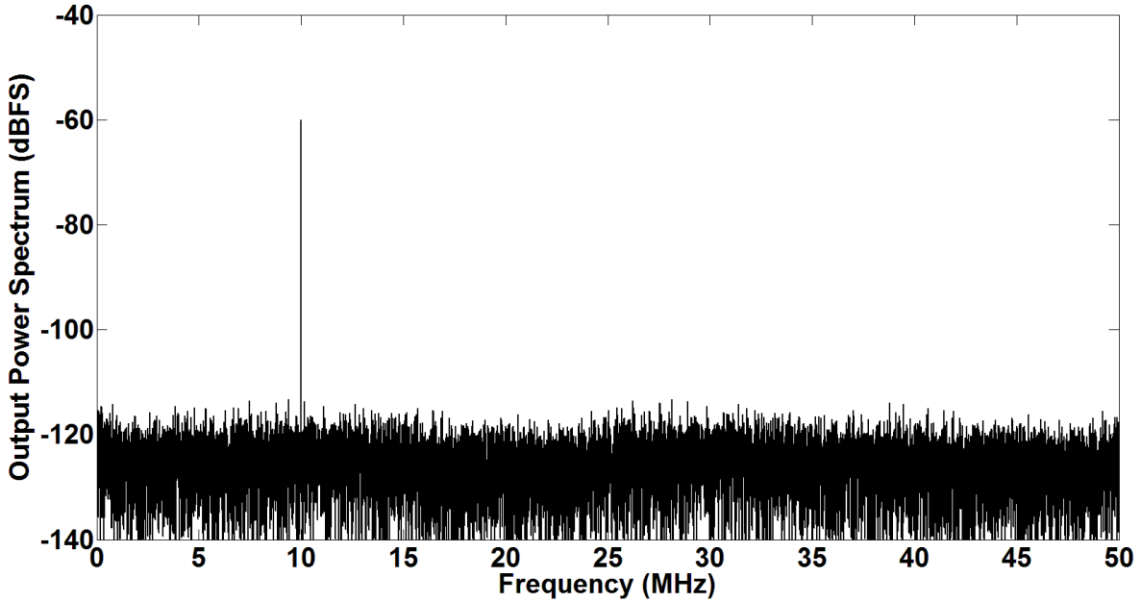


Fig. 3.39 Measured output power spectrum at P_{in}=-60dBFS.

A two-tone input signal was applied to the ADC to measure the linearity and to test the effectiveness of the proposed calibration scheme. The results are shown in Fig. 3.40 before calibration and in Fig. 3.41 after calibration, with input signal frequencies at 4.75MHz and 5.25MHz at an input power level of P_{in}=-6.48dBFS. As seen in Fig. 3.40 and in Fig. 3.41, the third inter-modulation product (IM3) decreases by more than 15dB after calibration.

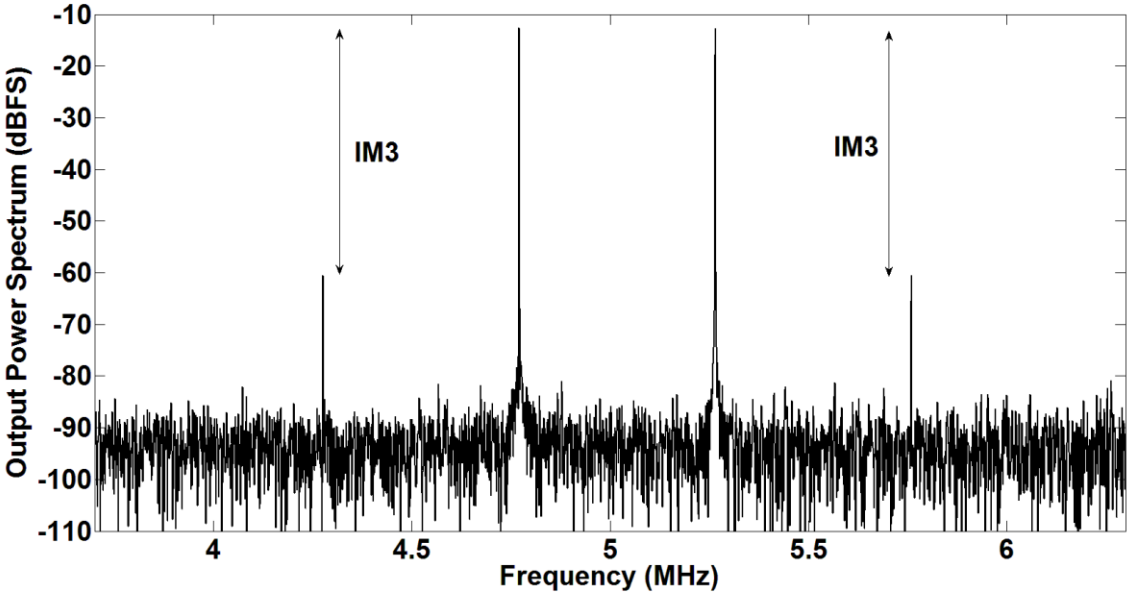


Fig. 3.40 Measured output power spectrum with two-tone input before calibration.

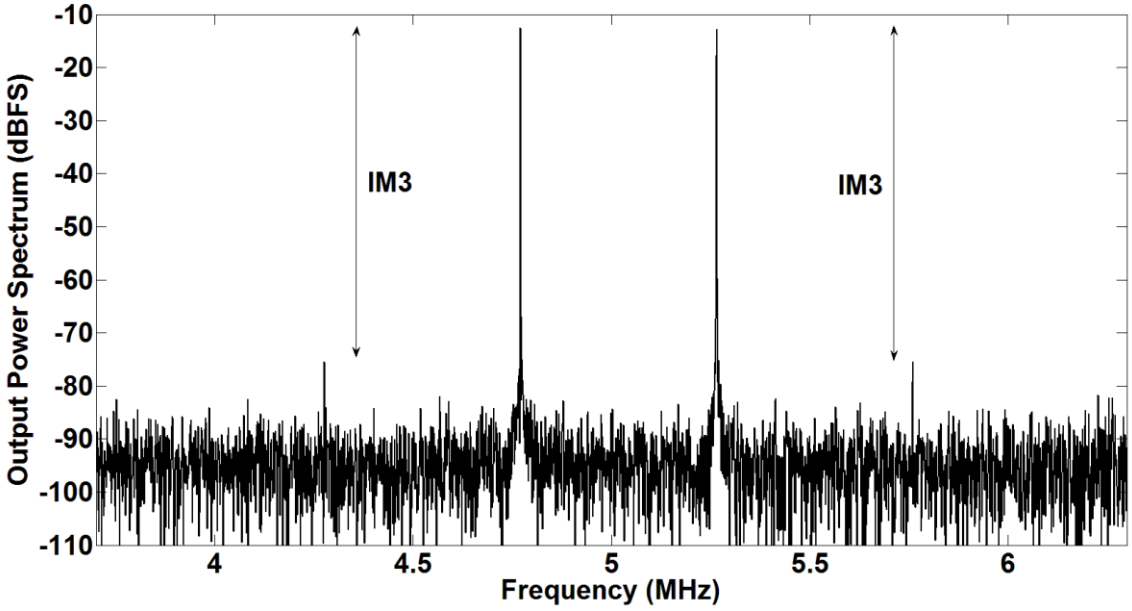


Fig. 3.41 Measured output power spectrum with two-tone input after calibration.

The noise floor in Fig. 3.40 and Fig. 3.41 increases by more than 15 dB when compared with the noise floor of Fig. 3.39. This is mainly due to noise contribution of the signal generators themselves, and because of high clock jitter effects due to the large signal used. The SNDR vs. input power for a two-tone test is shown in Fig. 3.42.

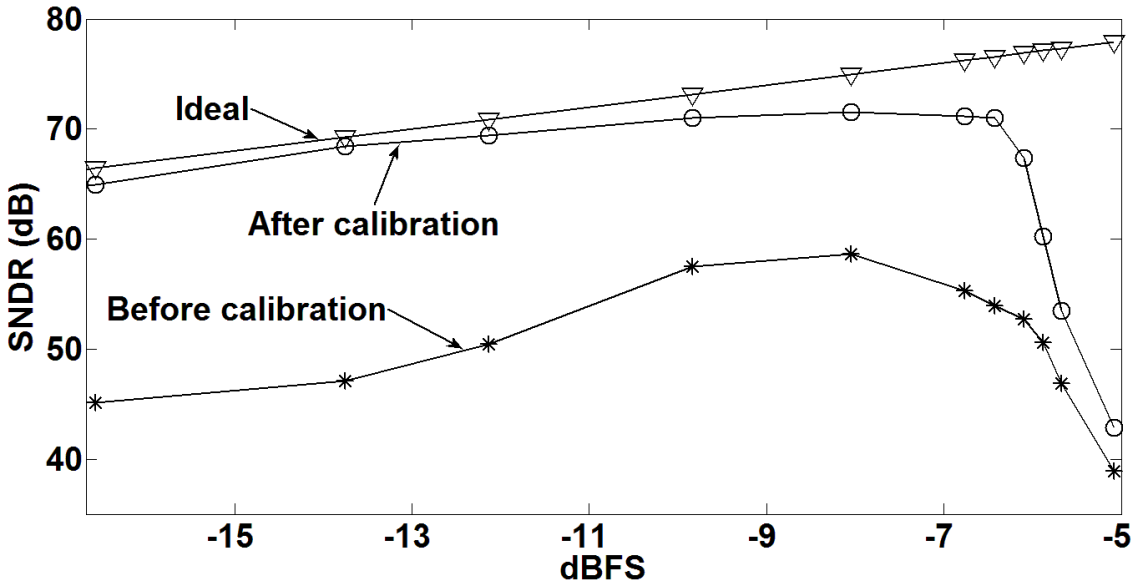


Fig. 3.42 Measured SNDR with two-tone input vs P_{in} with f_{center}=5MHz.

The SNDR after calibration is 71.1 dB, compared with an SNDR of 53.9 dB before calibration at P_{in}=-6.48dBFS, corresponding to about 3 bits improvement after calibration. When P_{in} > -6dBFS clipping occurs in the time domain waveform and the distortion increases rapidly when the input power is increased beyond this level. The calibration technique is less effective when clipping is present due to the extra distortion

not caused by the inherent non-idealities of the pipeline. The SNDR vs. input center frequency is shown in Fig. 3.43 for a two-tone test.

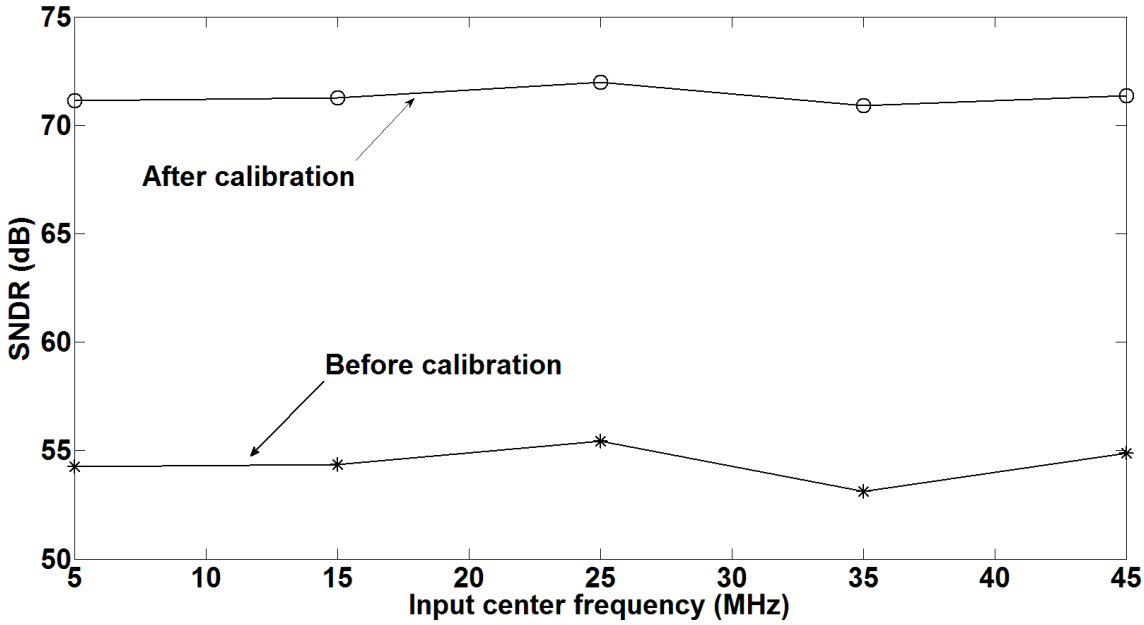


Fig. 3.43 Measured SNDR at P_{in}=-6.48dBFS as function of the input frequency.

The SNDR after calibration is approximately at the same value up to the Nyquist frequency, which indicates that the input sampling network is properly designed and with the required linearity up to Nyquist frequency. The SNDR vs. sampling rate is shown in Fig. 3.44 for a two-tone test.

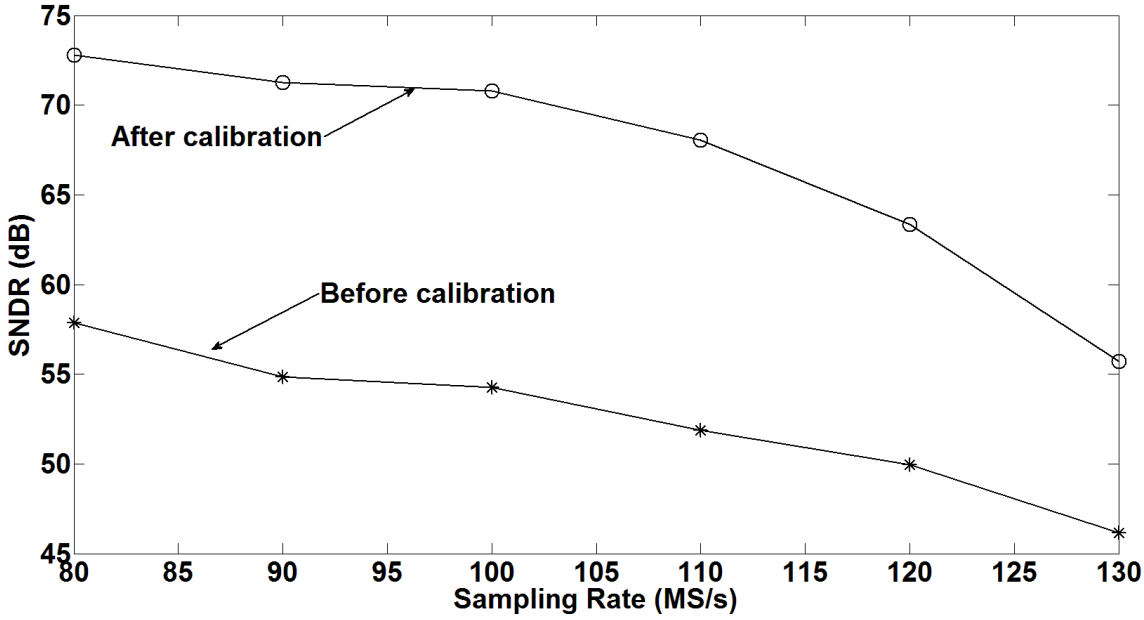


Fig. 3.44 Measured SNDR at P_{in}=-6.48dBFS vs sampling rate.

The resolution of the ADC reduces with increased sampling frequency, due to less settling time available for the amplifiers and in the input sampling network. The maximum sampling rate of the ADC is 130 MS/s.

The worst-case INL (in LSBs) can be calculated from the power of the intermodulation tones according to (3.14) [44].

$$\frac{P_{in}}{P_{IM3}}(\text{dB}) \approx 20 \cdot \log_{10}\left(\frac{1}{|\text{INL}|_{max}\ 2^{-14}}\right) \tag{3.14}$$

The worst-case INL vs. input power is shown in Fig. 3.45 before and after calibration. The INL is reduced from 32.9 LSBs to 4 LSBs after calibration at P_{in}=-6.48dBFS, which is another indication of the effectiveness of the calibration technique.

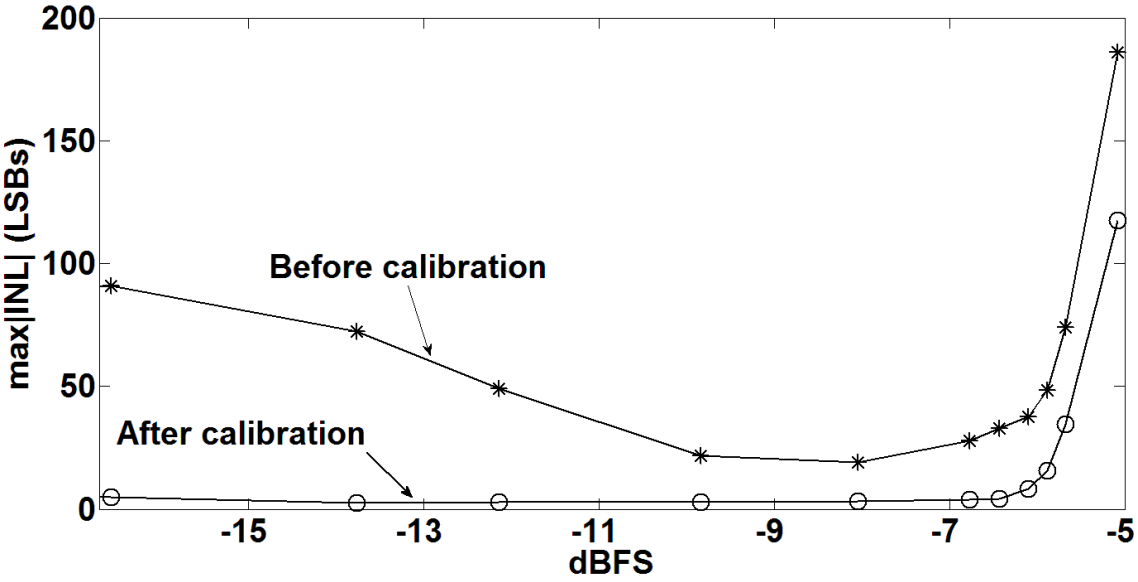


Fig. 3.45 Measured worst-case INL vs P_{in} with f_{center}=5MHz.

The power consumption of the core ADC (excluding the power of reference generation circuitry but including the total dynamic power) is 105 mW and the ADC has a figure of merit of 360 fJ/conversion-step. The ADC's measured results are summarized in Table 3.7. Fig. 3.46 compares the performance of the ADC with previously published work [15], which indicates that this ADC is very competitive among all topologies. Table 3.8 compares recently reported architectures of the same class. The proposed ADC

architecture achieves the best in-class figure of merit, which proves the effectiveness of the calibration technique.

Table 3.7 Pipeline ADC measured performance.

Technology	130-nm CMOS
Differential input range	$2V_{pp}$
Sampling rate	100 MS/s
SNR/SNDR/ENOB	82dB/71.5dB/11.52 bits
INL before/after calibration	32.9 LSBs/4 LSBs
Analog/Digital Power:	96 mW/9 mW
Active area	1.25 mm^2

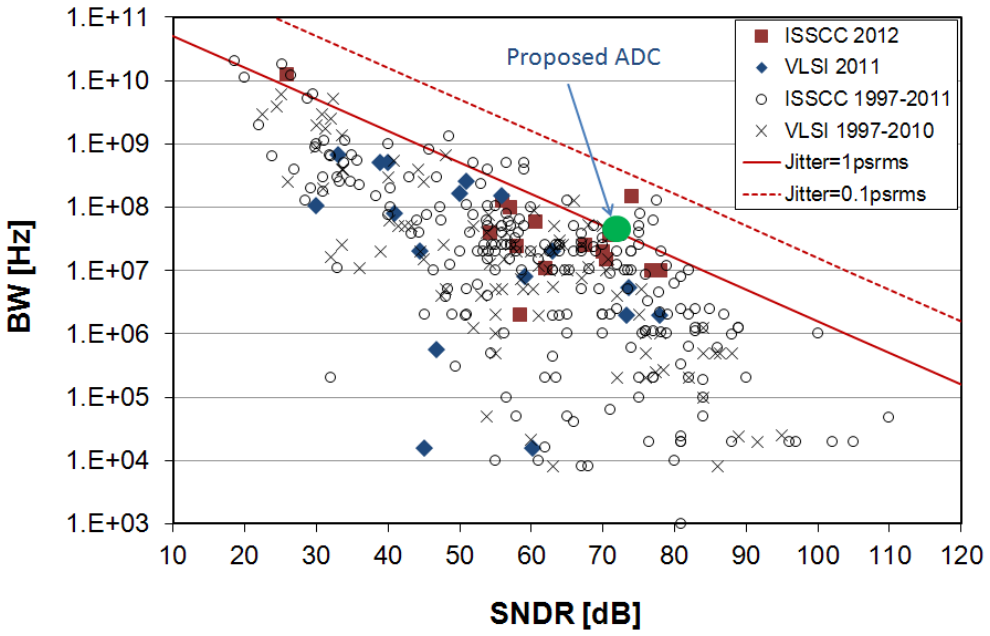


Fig. 3.46 Algorithmic ADC performance comparison.

Table 3.8 Performance comparison with published data.

Ref.	Technology	Power (mW)	Sampling rate (MS/s)	ENOB (bits)	FOM (pJ/conv-step)
[19]	0.35µm	254	20	11.47	4.47
[21]	0.35µm	56.3	20	11.8	0.78
[24]	0.25µm	370	40	11.91	2.40
[26]	180-nm	285	20	11.85	3.86
[27]	65-nm	180	200	10.04	0.85
[32]	90-nm	200	100	11.83	0.55
[33]	90-nm	348	200	10.0	1.7
[34]	180-nm	385	125	12.76	0.44
[37]	180-nm	98	12	12.25	1.67
[45]	180-nm	69	80	9.29	1.37
[46]	90-nm	130	100	11.17	0.56
[47]	180-nm	12	50	9.04	0.45
This work	**130-nm**	**105**	**100**	**11.52**	**0.36**

3.7 Conclusions

A digital background calibration technique used for the design of a 14-bit 100 MS/s pipelined ADC was presented. The proposed calibration technique linearizes the digital output to correct for errors resulting from capacitor mismatch, finite amplifier gain, voltage reference errors and differential offsets. The ADC has a measured SNDR of 71.1 dB after calibration with a sampling rate of 100 MS/s and a power consumption of 105 mW. The measured worst-case INL is reduced from 32.9 LSBs down to 4 LSBs after calibration. Although not fabricated in the most advanced technologies available, the proposed ADC shows a best in-class figure of merit of 360 fJ/conversion-step.

3.7.1 Future Work

Although the ADC exhibits excellent performance, improved results can be obtained by implementing on-chip reference buffers. This will also reduce the complexity of the board. The board is quite noisy and the noise on each reference line appears to be uncorrelated, at least when observed on the oscilloscope. Noise on reference lines can only be corrected for with a linear approximation. Using an on-board crystal oscillator should be further investigated since it would in theory be able to provide a lower jitter clock than the signal generator.

The ADC can be designed to operate at higher conversion speeds, but in this case, boot-strapped switches may be necessary in the pipeline stages, depending on the technology used and the supply voltage. If the gain calibrator comparator is not necessary, then the design of the S/H amplifier should be changed to a one-stage amplifier, possibly similar to the pipeline stage amplifier topology.

CHAPTER IV

CONCLUSIONS

Pipelined ADCs is the preferred architecture for many applications that require both high speed and high resolution. However, non-calibrated pipelined ADCs are very costly for very high resolution. This work describes a novel digital background calibration technique that corrects for errors in the ADC. This relaxes the requirements for the analog components and enables power and area savings. Digital calibration is preferred over analog calibration due to higher robustness and accuracy. The calibration technique is implemented in a 14-bit, 100 MS/s pipelined ADC manufactured in TSMC 0.13 µm. The core ADC has a power consumption of 105 mW and an active area of 1.25 mm^2. An effective resolution of over 11.5 bits is achieved with a near Nyquist input at full sampling rate. The ADC achieves a best-in-class figure of merit of 360 fJ/conversion-step.

An 8-bit algorithmic ADC was also presented. This ADC reduces power consumption at system level by minimizing voltage reference generation and ADC input capacitance. This ADC is implemented in IBM 90nm digital CMOS technology and achieves around 7.5 bits linearity at 0.25 MS/s with a power consumption of 300 µW and an active area of 0.27 mm^2.

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APPENDIX

In this appendix it is demonstrated that the calibration parameters a_i do not need to be determined and hence the calibration point V_{cal3}, see Fig. 3.5, and Δx are not needed. The calibration algorithm starts at the output of stage M (because its output is directly available from the backend) and input-refers this output and applying the calibration parameters to correct for the errors of the stages 1..M. The input-referred signal of a pipeline stage is expressed below (which follows from (3.4)):

$$V_{out,i-1,D} = \begin{cases} \dfrac{a_i V_{out,i,D} + b_{1,i} - V_{ref}}{2}, & \text{region } 0 \\ \dfrac{a_i V_{out,i,D}}{2}, & \text{region } 1 \quad i = 1..M \\ \dfrac{a_i V_{out,i,D} - b_{1,i} + V_{ref}}{2}, & \text{region } 2 \end{cases} \tag{A1}$$

Let us consider the transfer characteristic of stage M-1 shown in Fig. 3.5. The calibration point V_{cal1} of stage M-1 is mapped into region 2 of stage M and the corresponding value of the backend, $V_{out,1,M}$ (which is the maximum of $V_{out,M}$ in region 2 while the data is in region 0 of stage M-1) is recorded. The output voltage $V_{out1,M}$ is then input-referred to the input of stage M and $V_{cal1,M-1}$ can then be expressed as below:

$$V_{cal1,M-1} = \frac{a_M \cdot V_{out1,M,D} - b_{1,M} + Vref}{2} = \frac{a_M}{2}\left(V_{out1,M,D} + V_{cal1,M} - V_{cal2,M}\right) \quad \text{(A2)}$$

Similarly, the calibration points $V_{cal2,M-1}$ and $V_{cal3,M-1}$ are expressed as below:

$$V_{cal2,M-1} = \frac{a_M \cdot V_{out2,M,D} + b_{1,M} - Vref}{2} = \frac{a_M}{2}\left(V_{out2,M,D} - V_{cal1,M} + V_{cal2,M}\right) \quad \text{(A3)}$$

$$V_{cal3,M-1} = \frac{a_M \cdot V_{out3,M,D} - b_{1,M} + Vref}{2} = \frac{a_M}{2}\left(V_{out3,M,D} + V_{cal1,M} - V_{cal2,M}\right) \quad \text{(A4)}$$

From (3.6), it follows that a_{M-1} and b_{M-1} are expressed as below, where it is noted that a_{M-1} is inversely proportional to a_M.

$$a_{M-1} = \frac{2\Delta x_{M-1}}{V_{cal3,M-1} - V_{cal2,M-1}} = 4\frac{\Delta x_{M-1}}{a_M}\frac{1}{V_{out3,M,D} - V_{out2,M,D} + 2\left(V_{cal1,M} - V_{cal2,M}\right)} \quad \text{(A5)}$$

$$b_{1,M-1} = V_{ref} - a_{M-1}\left(V_{cal1,M-1} - V_{cal2,M-1}\right) \qquad \text{(A6)}$$
$$= V_{ref} - \frac{a_{M-1}a_M}{2}\left(V_{out1,M,D} - V_{out2,M,D} + 2\left(V_{cal1,M} - V_{cal2,M}\right)\right)$$

The corrected output voltage of stage M-1 (which is the input-referred output voltage of stage M) for any input is proportional to a_M, as shown below:

$$V_{input,ref,M,D} = V_{out,M-1,D} =$$
$$\begin{cases} \dfrac{V_{out,M,D}\cdot a_M \pm \left(b_{1,M} - V_{ref}\right)}{2} \\ = \dfrac{a_M}{2}\left(V_{out,M,D} \pm \left(V_{cal1,M} - V_{cal2,M}\right)\right) = a_M\gamma_1, & \text{region } 0,2 \\ \dfrac{V_{out,M,D}\cdot a_M}{2} = a_M\gamma_2, & \text{region } 1 \end{cases} \qquad \text{(A7)}$$

where γ_1 and γ_2 are functions of known values ($V_{cal1,M}$, $V_{cal2,M}$, $V_{out,M,D}$). The corrected output voltage of stage M-2 (which is the input-referred output voltage of stage M-1) for any input is proportional to the product of a_{M-1} and a_M, as shown below:

$$V_{input,ref,M-1,D} = V_{out,M-2,D} =$$

$$\begin{cases} \dfrac{V_{out,M-1,D} \cdot a_{M-1} \pm \left(b_{1,M-1} - V_{ref} \right)}{2} \\ = a_{M-1} a_M \gamma_3 = \dfrac{\Delta x_{M-1}}{a_M} a_M \gamma_4, \quad \text{region } 0,2 \\ \dfrac{V_{out,M-1,D} \cdot a_{M-1}}{2} = a_{M-1} a_M \gamma_5 \\ = \dfrac{\Delta x_{M-1}}{a_M} a_M \gamma_6, \quad \text{region } 1 \end{cases} \tag{A8}$$

where γ_3, γ_4, γ_5 and γ_6 are functions of known values (γ_1,γ_2, $V_{cal3,M}$, $V_{cal1,M-1}$, $V_{cal2,M-1}$, $V_{cal3,M-1}$). Similarly, the corrected output voltage of stage M-3 is proportional to the product of $a_{M-2}..a_M$, as shown below:

$$V_{input,ref,M-2,D} = V_{out,M-3,D} =$$

$$\begin{cases} = \dfrac{V_{out,M-2,D} \cdot a_{M-2} \pm \left(b_{1,M-2} - V_{ref} \right)}{2} = a_{M-2} a_{M-1} a_M \gamma_7 \\ = \dfrac{\Delta x_{M-2}}{a_{M-1} a_M} a_{M-1} a_M \gamma_8 = \Delta x_{M-2}\ \gamma_8, \quad \text{region } 0,2 \\ \dfrac{V_{out,M-2,D} \cdot a_{M-2}}{2} \\ = a_{M-2} a_{M-1} a_M \gamma_9 = \dfrac{\Delta x_{M-2}}{a_{M-1} a_M} a_{M-1} a_M \gamma_{10} = \Delta x_{M-2}\ \gamma_{10} \quad \text{region } 1 \end{cases} \tag{A9}$$

where the γ's are functions of known values. Similarly, it follows that the final output is proportional to $a_{MSB}..a_M$ and therefore $a_2..a_M$ cancel out (hence $\Delta x_2..\Delta x_M$ also cancel out) and the only remaining parameter is a_{MSB}, which is a function of Δx_{MSB}. If Δx_{MSB} is estimated then the calibrated final output will be gain-error free.