DC-DC CONVERTER CURRENT SOURCE FED NATURALLY COMMUTATED BRUSHLESS DC MOTOR DRIVE

A Thesis

by

RAHUL VIJAYKUMAR KHOPKAR

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2003

Major Subject: Electrical Engineering

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ABSTRACT

DC-DC Converter Current Source Fed Naturally Commutated Brushless DC Motor Drive. (August 2003)
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Chair of Advisory Committee: Dr. Hamid A. Toliyat

The aim of this work is to reduce the cost and size of a brushless dc motor (BLDC) drive as well as increase the reliability and ruggedness of that drive. Traditional BLDC drives use Voltage Source Inverters (VSI) that utilize hard switching, thereby generating switching losses and entail the use of large heatsinks. VSI needs a huge dc link capacitor that is inherently unreliable and is one of the most expensive components of a drive. Hence, a Current Source Inverter (CSI) is used to replace the hard switchings by natural turn-off, thereby eliminating the heatsinks as well as the large dc link capacitor. A controlled rectifier together with a large inductor act as the current source. The only disadvantage is the large value of the dc link inductor and the huge number of turns needed to achieve these values of the inductances lead to huge resistive losses.

Therefore, it is shown that it is possible to replace the controlled rectifier and the large inductor with a suitable dc-dc converter based current source switching at high frequencies and a much smaller value of the dc link inductor. Switching at high frequencies makes it possible to reduce the value of the dc link inductor without increasing the current ripple. Hence, it is possible to have the advantages of using a CSI as well as reduce the value of the dc link inductor without a corresponding increase in the heat sink and snubber requirements.

To my parents and all my well-wishers

ACKNOWLEDGMENTS

I wish to thank Dr. Hamid A. Toliyat for his guidance and advice throughout the course of this research and also Dr. S.M. Madani for defining and supervising this work. Dr. Enjeti's advice was instrumental in many aspects of the project, for example, the analysis of the drive. Dr. Bhattacharyya's suggestions and the course that he had taught helped in designing the controllers that are used in this drive. Dr. Langari's coures on Mechatronics prepared a firm base for the implementation aspects of this project. Mr. Rayner's and Mr. Gopinath's cost-conscious approach to design was worth emulating. I wish to thank Dr. Parker and Prof. Tyler for their encouragement and support.

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I. INTRODUCTION

1. Need for drives

Speed control of motors is essential in many applications, for example, the speed of a conveyor belt, a lathe machine, spinnerets in a textile mill, etc. Because of its nearly flat torque versus speed characteristics, the speed of a dc motor is the easiest to control [1, 2].

2. Dc motors, commutators, brushes and their problems

The block diagram of a dc motor is shown in Fig. 1.

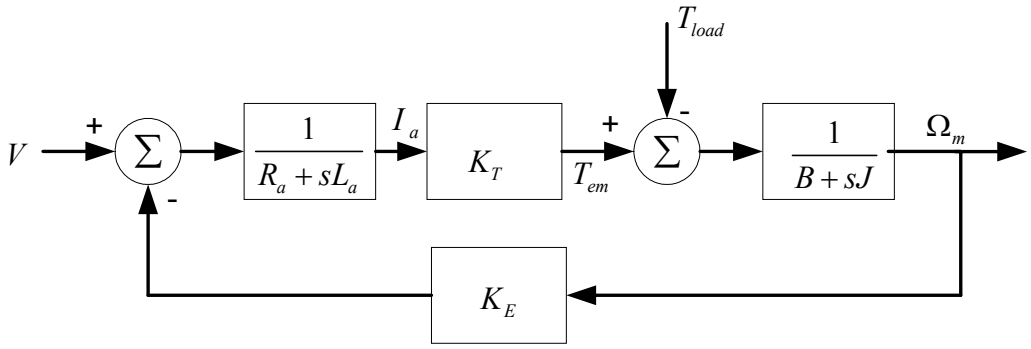

Fig. 1. Model of a dc motor

In order to change the direction of the current flowing in the armature coils when the magnetic field direction 'seen' by an armature coil changes, thus maintaining the direction of rotation, a brush and commutator arrangement is used [2, 3]. Fig. 2 shows an illustration of the commutation process, assuming an anti-clockwise direction of rotation. Therefore, the current in coil 'd', earlier to this time interval, was flowing towards coil 'e'. In order to reverse the direction of the current in coil 'd', that coil has to be short circuited by the

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[1] This dissertation follows the style and format of *IEEE Transactions on Industry Applications.*

brush. After the rotor has rotated anti-clockwise by an arc distance of one commutator segment, current in coil ‘d’ flows towards coil ‘c’, thus completing the process of commutation.

Since the back-emf generated in the coil is short-circuited by the brush, a large current flows, causing sparking at the interface of the commutator and the brushes as well as causing heating and the production of braking torque. In order to minimize this problem, commutation is carried out in the magnetic field crossover region. Even after taking these measures, because of the distortion of the effective magnetic flux due to the armature reaction, some back-emf is still generated in the coils in the magnetic field crossover region. It is desirable to minimize the crossover region in order to maximize the utilization of the motor.

The friction between the brush and the commutator causes the brush and the commutator to wear out, requiring maintenance and an eventual replacement of this apparatus. It also precludes the use of a dc motor in hazardous environment where sparking is not permitted. There is a potential drop called ‘contact potential difference’, associated with this arrangement, and is usually in the range of 1–1.5 V, leading to a drop in the effective input voltage.

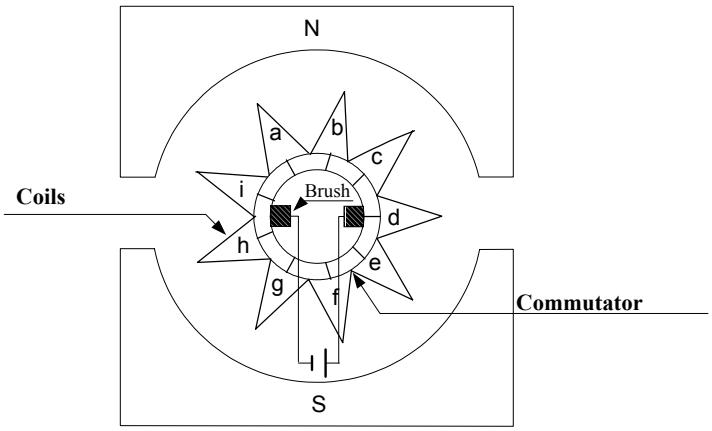

Fig. 2. Commutator and brushes

3. Permanent magnet motors

In permanent magnet motors, the field is generated by permanet magnets mounted on the rotor, and the rotating field is generated by means of stator windings. A permanent magnet rotor field can be of two shapes, sinusoidal and trapezoidal. The motors having a sinusoidal rotor field, and hence a sinusoidal back-emf (Fig. 3) behave like synchronous ac machines and are usually called Permanent Magnet Synchronous Machine (PMSM). In PMSM machines, the slip rings are eliminated and the stator windings are equivalent to the stator windings in synchronous ac machines. While no power is required for field excitation, leading to elimination of rotor losses, the disadvantage is that the rotor field is fixed at a constant value (except when saturation effects show up), whereas in a synchronous ac machine, the rotor field is permitted to change by supplying appropriate amounts of the field excitation current [3].

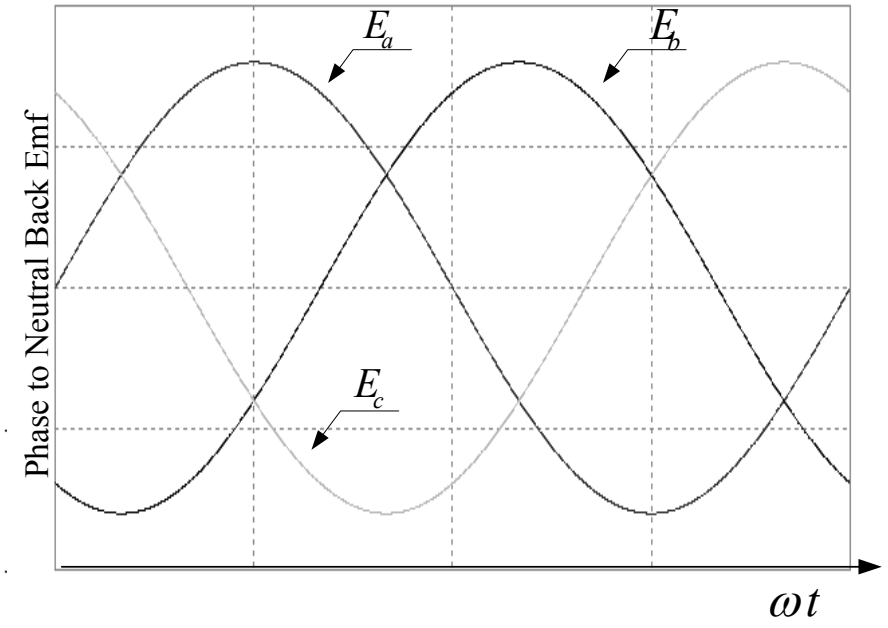

Fig. 3. Back-emf of a three-phase PMSM

In a PMSM motor, there are two types of mountings of the magnets on the rotor. Where an arc shaped magnet is used, rotor field corresponds to a smooth rotor synchronous ac machine, and the reluctance torque is zero. It is the fundamental component of the power as shown in Fig. 4. If the back-emf is E, the input voltage is V, the load angle is δ, the frequency is ω, X_{direct} and $X_{quadrature}$, respectively, are the direct and quadrature axis reactances, then the synchronous power $P_{synchronous}$ is given by

$$P_{synchronous} = \frac{VE}{\omega X_{direct}} \sin\delta \tag{1.1}$$

If the permanent magnets mounted on the rotor are rectangular, it corresponds to a salient pole synchronous ac motor and this motor develops a reluctance power P_{reluct} [2], of frequency 2δ as illustrated in Fig. 4.

$$P_{reluct} = V^2 \left(\frac{X_{direct} - X_{quadrature}}{2X_{direct}X_{quadrature}}\right) \sin 2\delta \tag{1.2}$$

The total power is the sum of the synchronous and the reluctance components.

$$P_{total} = P_{synchronous} + P_{reluct} \tag{1.3}$$

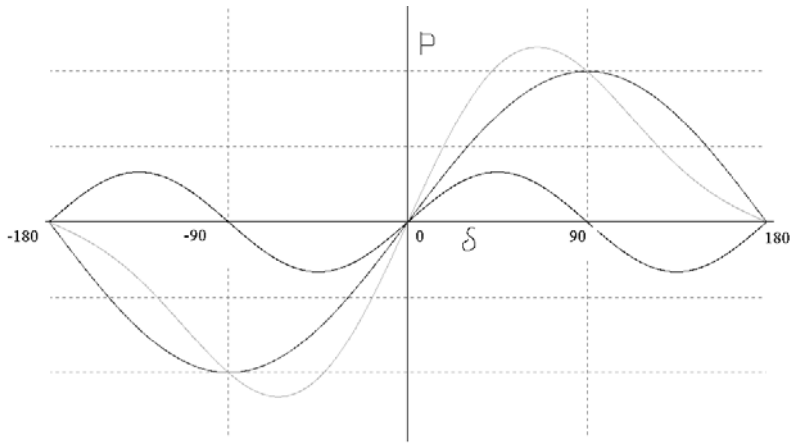

Fig. 4. Power generated by the synchronous and reluctance components

Therefore the maximum power, and hence the maximum torque, generated by a salient pole synchronous machine is higher than that generated by a smooth pole synchronous machine [2]. It can be clearly seen in Fig. 4, where the total is represented by a non-sinusoidal function of δ.

For a brushless dc (BLDC) motors, the rotor field and hence the back-emf is trapezoidal as shown in Fig. 5.

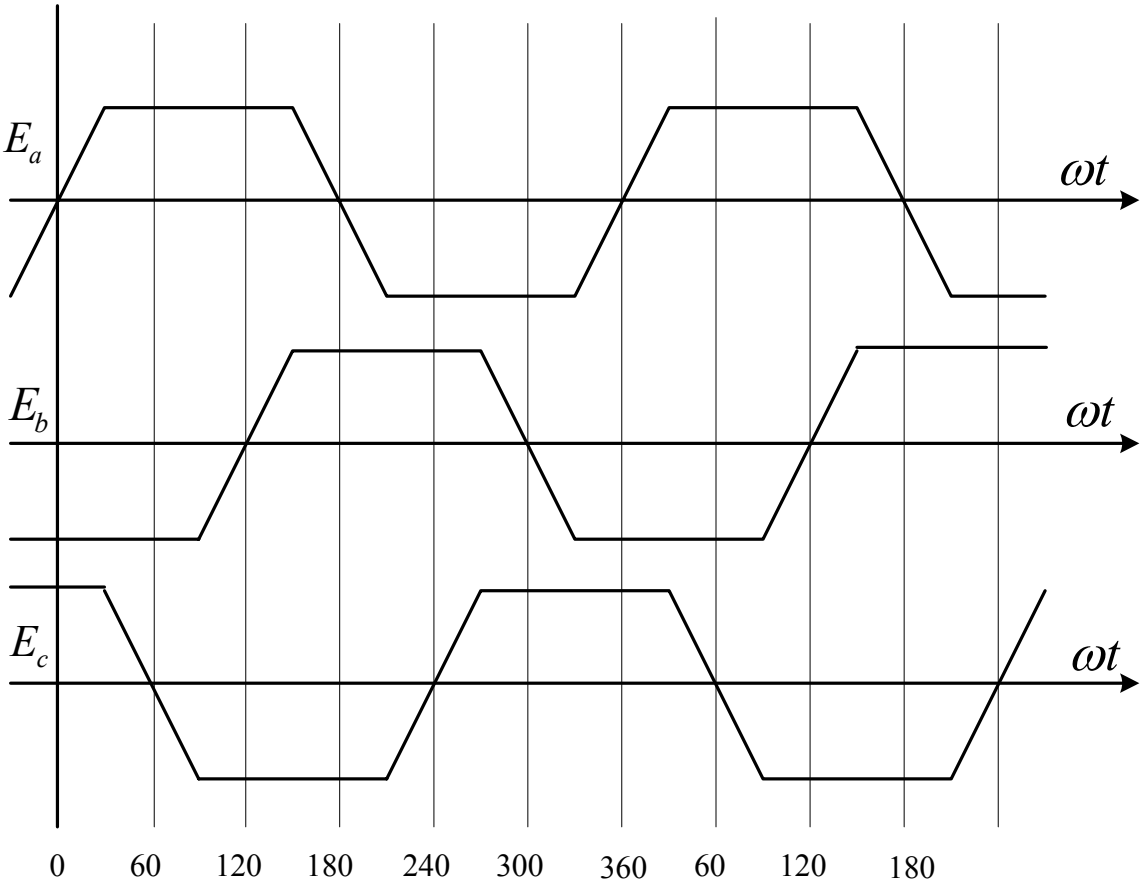

Fig. 5. Trapezoidal back-emf of a three-phase BLDC

The cheapest permanent magnets are usually made from ferrite (have low coercive strength), whereas the more expensive and rare-earth type stronger ones (have high coercive strength) contain Samarium-Cobalt or Neodium-Iron-Boron [4]. Because the rare-earth type magnets have a higher coercive strength, they usually withstand the demagnetization effects better than the ferrite magnets, and hence are usually preferred. The magnets are made into desired shapes, put in an appropriate jaw and then magnetized by a pulse of high current obtained from a capacitor bank. At low power ratings, especially the fractional horsepower range, permanent magnet motors are economical. As the rating of the motor increases, the cost of permanent magnets and their manufacture becomes costlier relative to the motors in which the field is generated by applying an external source.

The smaller of the permanent magnet motors, usually in the fractional horsepower range may have less than three phases. Motors with large ratings may contain more than three phases so as to distribute the power over more inverter legs, thus permitting the use of power semiconductor switches with smaller ratings.

II. INTRODUCTION TO BLDC MOTOR DRIVES AND DC-DC CONVERTERS

1. Brushless dc motor background

A brushless dc motor is a dc motor turned inside out, so that the field is on the rotor and the armature is on the stator. The brushless dc motor is actually a permanet magnet ac motor whose torque-current characteristics mimic the dc motor. Instead of commutating the armature current using brushes, electronic commutation is used. This eliminates the problems associated with the brush and the commutator arrangement, for example, sparking and wearing out of the commutator-brush arrangement, thereby, making a BLDC more rugged as compared to a dc motor. Having the armature on the stator makes it easy to conduct heat away from the windings, and if desired, having cooling arrangement for the armature windings is much easier as compared to a dc motor.

In effect, a BLDC is a modified PMSM motor with the modification being that the back-emf is trapezoidal instead of being sinusoidal as in the case of PMSM. The "commutation region" of the back-emf of a BLDC motor should be as small as possible, while at the same time it should not be so narrow as to make it difficult to commutate a phase of that motor when driven by a Current Source Inverter. The flat constant portion of the back-emf should be 120° for a smooth torque production.

The position of the rotor can be sensed by using an optical position sensors and its associated logic. Optical position sensors consist of phototransistors (sensitive to light), revolving shutters, and a light source. The output of an optical position sensor is usually a logic signal. This is especially useful when unipolar switching is used to drive the BLDC motor, as shall be explained in section 3.2.

Another option is using Hall effect position sensors [1], namely Hall_A, Hall_B, and Hall_C, each having a lag of 120° w.r.t. the earlier one. Three Hall position sensors are used to determine the position of the rotor field. These particular Hall position sensors, based on Hall effect principle, generate a TTL compatible output. In the motor which is being used, when the phase back-emf starts rising, the corresponding Hall sensor generates a logic high signal that goes low when the corresponding back-emf starts falling and

remains low till that back-emf starts rising. This implies that for the given motor, Hall sensor outputs lead the corresponding back-emfs by 30°. Thus for a P pole motor, we have 3P transitions of the Hall position sensor per revolution of the motor shaft. Fig. 8 shows the relationship of the phase back-emfs and the corresponding Hall position sensor outputs. As can be observed, the logic high of a Hall position sensor is maintained for 180°. This can be a significant disadvantage, since timers may have to be used in order to reduce the switching times to 120° (two-thirds of the Hall position sensor output high of 180°) [3].

Single and two-phase BLDC motors are usually in the fractional horsepower category, where cost is a major factor; a reduction in the number of phases implies a reduction in cost. One of the other advantage is that for a two-phase motor, two Hall position sensors are sufficient [3].

Some BLDC motors have armature windings on the interior shaft and the permanent magnet on the exterior enclosure that rotates, thus it is an inverted BLDC, commonly used in VCRs and other electronic apparatus. In many cases, the windings are ‘printed’ on a PCB for ease of winding, and may have an air core [3].

2. Principle of a BLDC drive

A conventional BLDC drive is illustrated in Fig. 6. It consists of a dc supplied by a rectifier arrangement, a dc link capacitor for energy storage, a Voltage Source Inverter (VSI) consisting of transistor switches, and finally, the three-phase output of the inverter is supplied to the motor. Although not explicitly shown, for position sensing purposes, either a Hall position sensor or an optical shutter arrangement is used along with some sort of microcontroller/microprocessor. Although snubbers are not shown, it is a practice to include snubbers to protect the transistor switches from voltage spikes generated by switching.

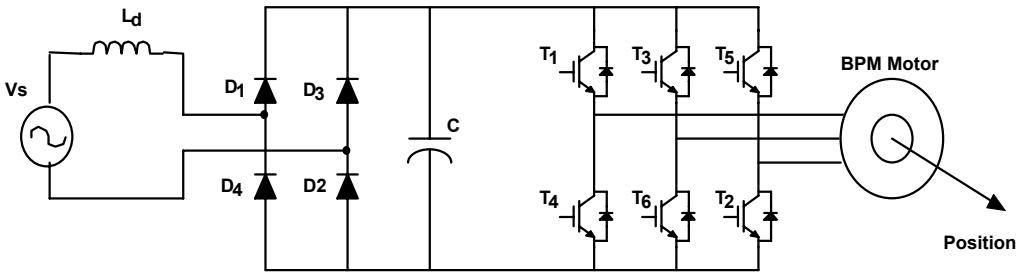

Fig. 6. Voltage Source Inverter BLDC drive

In order to achieve a constant torque that is ideally free from ripple, the desired current be a rectangular ac wave, 120° broad. Torque is given by expression (2.1) [4].

$$T_{em} = \frac{e_a i_a + e_b i_b + e_c i_c}{\omega_m} \tag{2.1}$$

e_a = phase-to-neutral back-emf of phase A (in volts),

e_b = phase-to-neutral back-emf of phase B (in volts),

e_c = phase-to-neutral back-emf of phase C (in volts),

i_a = current in phase A (in amperes),

i_b = current in phase B (in amperes),

i_c = current in phase C (in amperes) and

ω_m = angular velocity of the rotor shaft (in radians/second).

A profile for each phase of the motor with respect to the corresponding back-emfs as a function of the rotor position is shown in Fig. 7. At each rotor position, a constant current multiplies the constant part of the back-emf; hence the sum of the products of a phase back-emf and the corresponding phase current is constant.

The desired current profile is achieved by supplying the BLDC motor from either a VSI or a Current Source Inverter (CSI). When using a VSI, the desired current profile is

achieved by controlling the switching of the transistors [1]. The natural shape of the current supplied by a CSI conforms to the desired profile. At any given time, only two switches out of the six switches of an inverter are conducting. This means that only two phases are conducting at any instant, with current entering one of the phases and leaving through the other. The convention being used in this thesis is that the current entering any phase of a motor is assigned a positive sign, and the current that is leaving any phase of a motor is assigned a negative sign. Therefore, the upper switches of the inverter, namely, T1, T3 and T5, carry a current (flowing into the motor) which is assigned a positive sign. The lower switches of the inverter, namely, T2, T4 and T6 carry a negative current (flowing out from the motor). As can be seen from Fig. 7, there is a definite relation between the the back-emfs and the current waveforms, as a function of the rotor position. Hence, in order to have proper operation of this motor, it is necessary to synchronize the phase currents with the phase back-emfs. This is achieved by the use of Hall position sensors which detect the position of the rotor field, and hence the position of the rotor shaft and then corresponding to the rotor field, the Hall position sensors output a combination of binary numbers. Moreover, the rising and falling pulse edges of the Hall position sensors are used as triggers for timing circuits used in the control algorithm. A motor with synchronized switching is able to produce a positive torque.

As seen from Fig. 8, there is a definite sequence in which the phases conduct and turn off. The current commutation from one phase to the other phase corresponding to that particular state of the back-emfs is synchronized by these Hall position sensors, and it occurs after every sixty electrical degrees. It takes a finite interval of time for commutation, that is, to transfer the current from one phase to the other one in the appropriate sequence.

There may be cases where the neutral of the motor is not accessible, however the phase-to-phase back-emfs are accessible for measurement.

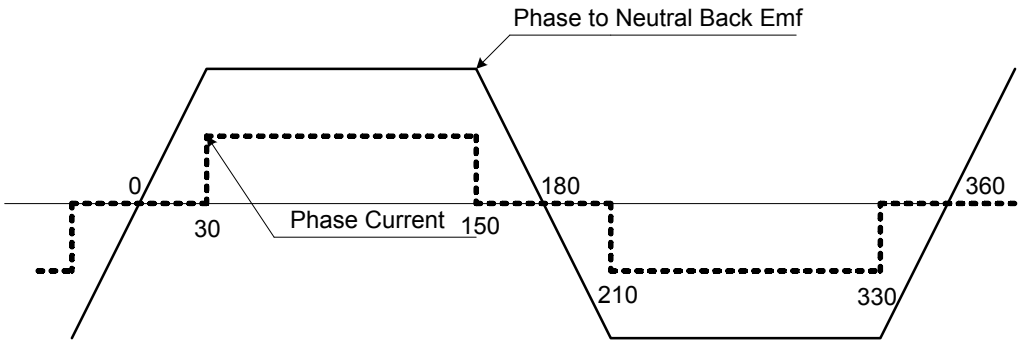

Fig. 7. Phase back-emf and phase current

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3. Model of a BLDC motor

Since a BLDC motor is easy to control, it is the motor of choice in many applications requiring precise control of speed [3].

The BLDC motor model is explained in this section. The electromagnetic torque, T_{em}, is linearly proportional to the armature current i_a, i.e.

$T_{em} = K_T i_a$, where K_T is the torque constant. (2.2)

The back-emf in a BLDC motor is linearly proportional to the rotational speed of the shaft. The back-emf is proportional to the speed of the motor and its direction is given by Fleming's right-hand rule. Considering that in a magnetic field of intensity B, a conductor of length l on the edge of a rotor of radius r is rotating at an angular velocity of ω radians per second. Then the speed of the conductor is given by (2.3).

$$vel = \omega \times r \tag{2.3}$$

By Fleming's right hand rule, the emf e generated in that conductor is given by (2.4).

$$e = \omega r B l \tag{2.4}$$

Conventionally, the number of conductors in an electrical machine is given by Z, and if the number of conductors in series is $\frac{Z}{2}$, the series back-emf is given by e as

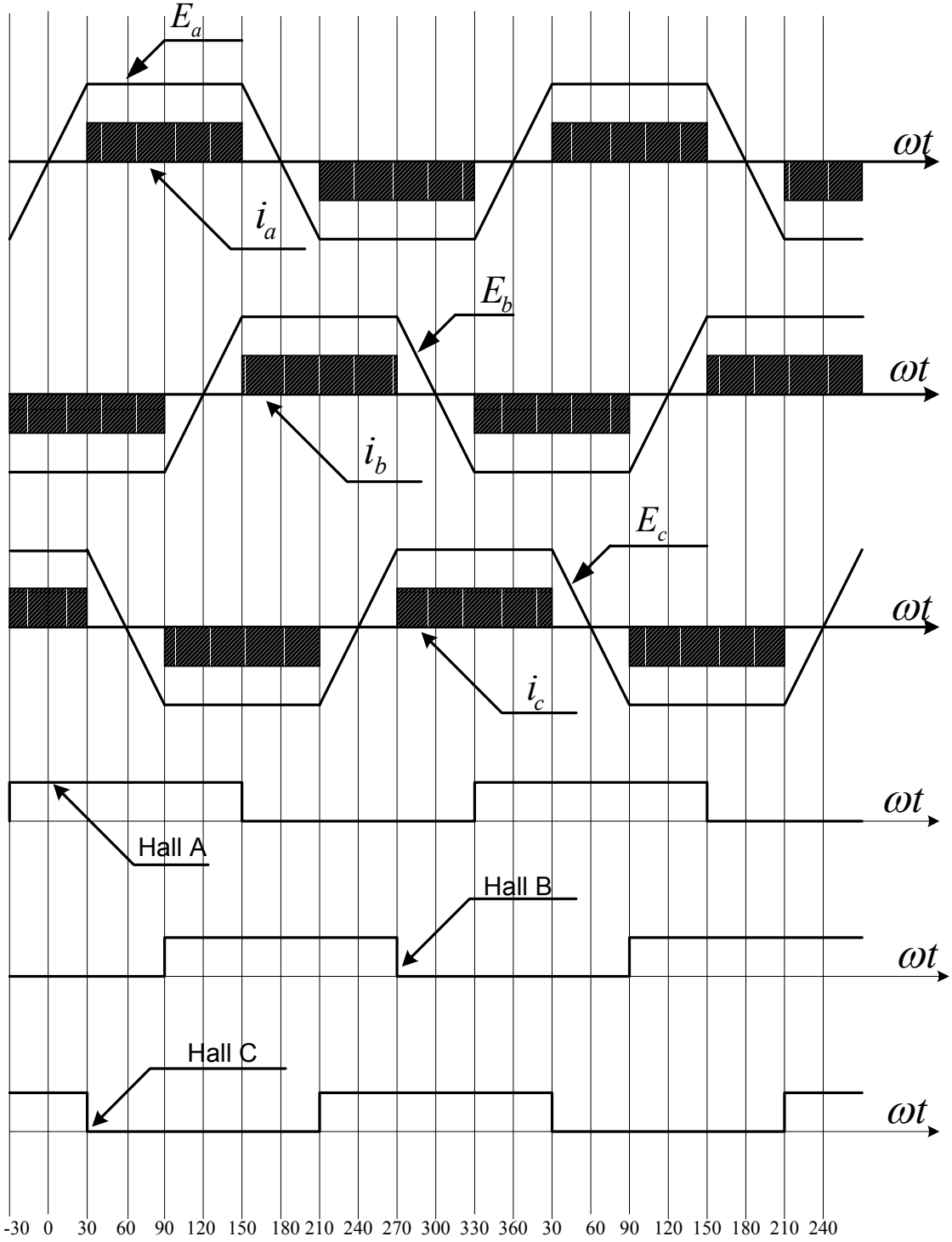

Fig. 8. Back-emfs, current waveforms and Hall position sensors for a BLDC

$$e = \omega_m r B l \frac{Z}{2} \tag{2.5}$$

In terms of the magnetic flux,

$e = K_E \omega_m$ where K_E is the back-emf constant. (2.6)

The model of a BLDC consisting of three phases is explained by means of equations. Since there is no neutral used, the sum of the three phase currents must add up to zero, i.e.

$$i_a + i_b + i_c = 0 \tag{2.7}$$

$$i_a + i_b = -i_c \tag{2.8}$$

Referring to the figure shown in Fig. 9 [5], the following equations are used to model the two pole three-phase BLDC motor.

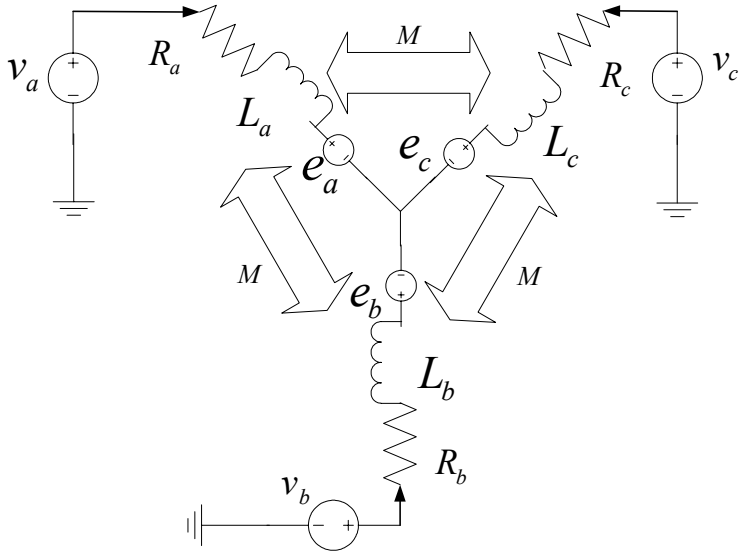

Fig. 9. R, L and back-emf BLDC model

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R_a & 0 & 0 \\ 0 & R_b & 0 \\ 0 & 0 & R_c \end{bmatrix} + \frac{d}{dt}\left[\begin{bmatrix} L_a & L_{ba} & L_{ca} \\ L_{ab} & L_b & L_{cb} \\ L_{ac} & L_{bc} & L_c \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}\right] + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{2.9}$$

If the permanent magnet inducing the rotor field is in the shape of an arc, it requires that the inductances be independent of the rotor position, hence

$$L_a = L_b = L_c = L_p \tag{2.10}$$

Considering the symmetry of the above matrix in addition to independence w.r.t. the rotor position,

$$L_{ab} = L_{ba} = L_{bc} = L_{cb} = L_{ca} = L_{ac} = M \tag{2.11}$$

Equation (2.9) reduces to

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R_a & 0 & 0 \\ 0 & R_b & 0 \\ 0 & 0 & R_c \end{bmatrix} + \begin{bmatrix} L_p & M & M \\ M & L_p & M \\ M & M & L_p \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{2.12}$$

From equations (2.8), (2.10), (2.11) and (2.12) , we have

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} R_a & 0 & 0 \\ 0 & R_b & 0 \\ 0 & 0 & R_c \end{bmatrix} + \begin{bmatrix} L_p - M & 0 & 0 \\ 0 & L_p - M & 0 \\ 0 & 0 & L_p - M \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \tag{2.13}$$

Rearranging the equations, we have obtained equations in a form suitable for simulation. Thus, the model of the BLDC reduces to that in Fig. 10. The back-emf waveforms $e_a, e_b \,\&\, e_c$ are trapezoidal in nature and can be represented by either the Fourier Series or by Laplace Transforms.

In Laplace domain, since the back-emf waveforms are periodic, we can represent them by means of a function of the period.

$$v = R_a i_a + K_E \omega_m + L_a \frac{di_a}{dt} \tag{2.14}$$

$$I_a(s) = \frac{V(s) - K_E \Omega_m}{R_a + sL_a} \tag{2.15}$$

This implies that the torque T is given by

$$T_{em} = \frac{K_T (V(s) - K_E \Omega_m)}{R_a + sL_a} \tag{2.16}$$

The transient model of a BLDC motor is illustrated in Fig. 11. It consists of R, L and back-emf circuit.

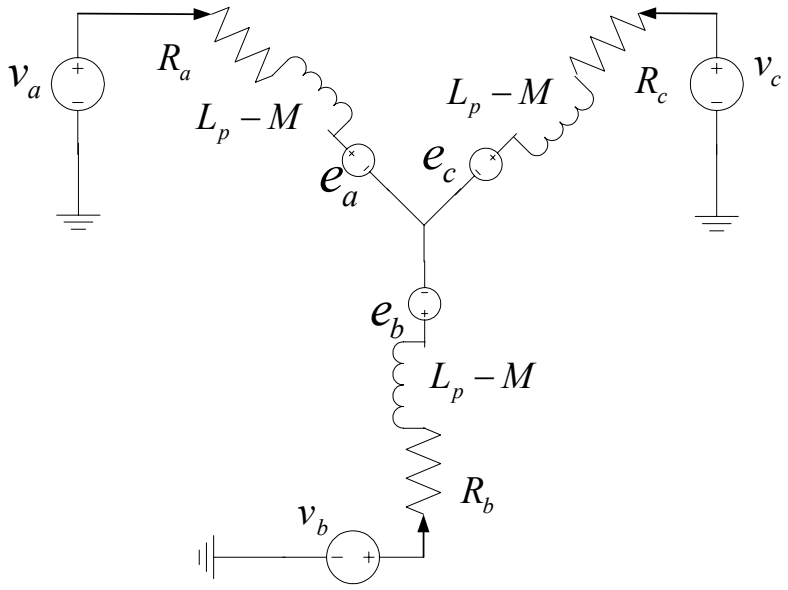

Fig. 10. Simplified R, L and back-emf BLDC model

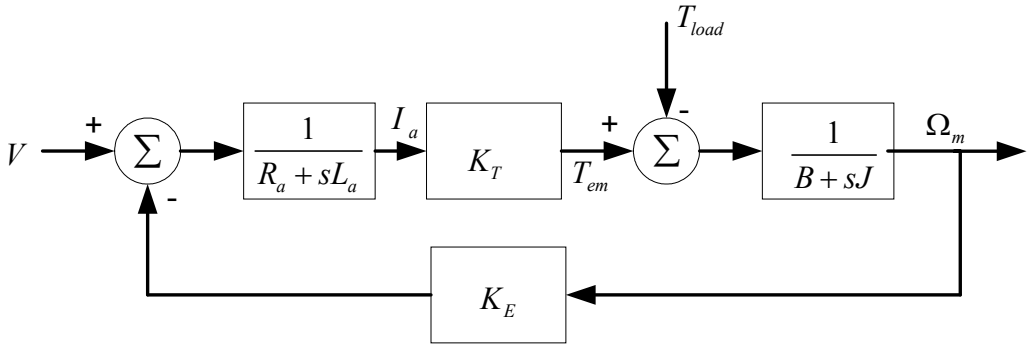

Fig. 11. Model of a BLDC motor

Equations (2.17) – (2.20) respectively illustrate the stator phase current, electromagnetic torque, back-emf, and the mechanical speed.

$$\frac{di_a}{dt} = \frac{v(t)}{L_a} - \frac{R_a}{L_a} i_a(t) - \frac{e(t)}{L_a} \tag{2.17}$$

$$T_{em} = K_T i_a \tag{2.18}$$

$$e(t) = K_E \omega_m \tag{2.19}$$

$$\frac{d\omega_m(t)}{dt} = \frac{T_{em}(t)}{J} - \frac{T_{load}(t)}{J} - \frac{B}{J}\frac{\omega_m(t)}{dt} \tag{2.20}$$

4. Analysis of a BLDC motor

For the block diagram illustrated in Fig. 11, the transfer function is denoted by (2.21) [6].

$$\frac{\Omega_m(s)}{V(s)} = \frac{\frac{K_T}{JL_a}}{s^2 + (\frac{JR_a + BL_a}{JL_a})s + (\frac{BR_a + K_T K_E}{JL_a})} \tag{2.21}$$

$$K_T = K_E \text{ (if there are no losses and only in SI units)} \tag{2.22}$$

$$\frac{\Omega_m(s)}{V(s)} = \frac{\frac{K}{JL_a}}{s^2 + (\frac{JR_a + BL_a}{JL_a})s + (\frac{BR_a + K_T K_E}{JL_a})} \tag{2.23}$$

From the Root-Locus plot shown in Fig. 12, we conclude that a BLDC motor is an inherently stable sytem, since there exists a range of $K_T K_E$ for which the poles of this system lie in the Left Half Plane (L.H.P.). The root locus starts from the poles $-\frac{R_a}{L_a}$ and $-\frac{B}{J}$ on the real axis and diverges as the product $K_T K_E$ increases, but it remains in the L.H.P. Therefore, a BLDC motor is ideally suited for speed control [7].

5. Necessity of dc-dc converters

There exists a need for changing a given value of a dc voltage supply to a desired value. This can be achieved by the use of a Linear Regulated Supply, typically used for supplying Integrated Circuits and other applications where the power supplied is relatively less as compared to motor drives. The disadvantages of a Linear Regulated Supply are that the output voltage is invariably less than the input supply voltage, and since the main output supply transistor operates in the linear region, there is a great deal of power loss (as heat dissipation) associated with this arrangement, thereby leading to a poor efficiency [8].

Dc-dc converters satisfy the need for converting a given dc voltage to a desired dc voltage at relatively high efficiencies [8]. “Buck” converters step down the input supply voltage, whereas “boost” converters step up the input supply. “Buck-boost” and “Cuk” converters can either step down the input voltage or step it up. In this thesis, only the “buck” and the “Cuk” converters are discussed since they have an inductor at their output, making them ideal for driving Current Source Inverters.

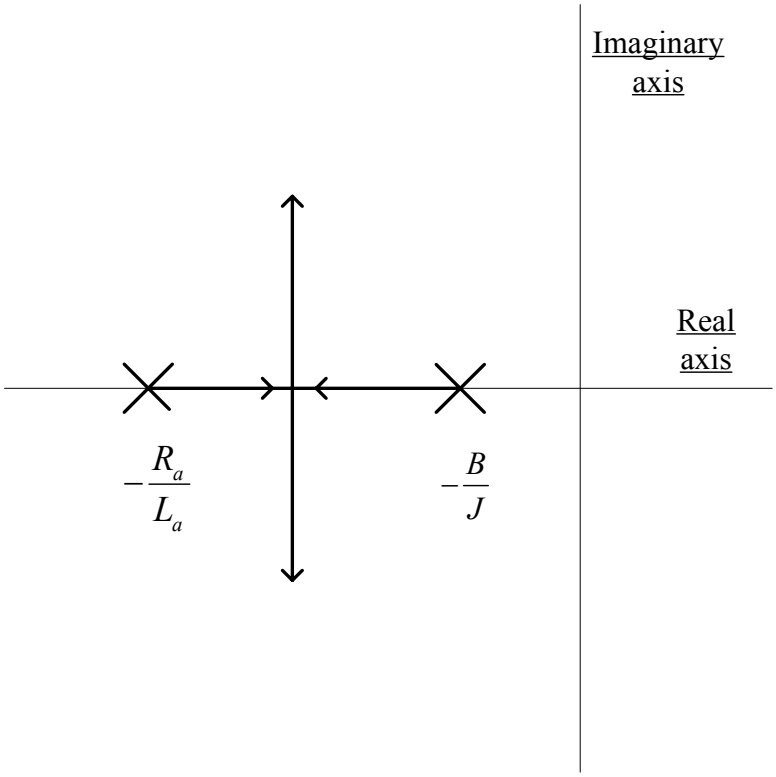

Fig. 12. Root-Locus for a BLDC motor

6. Buck dc-dc converter

The diagram of a buck dc-dc converter [9, 10] is shown in Fig. 13. Since the average voltage across an inductor during one switching period is zero, (positive and the negative parts of the areas are equal in magnitude), we get a relation between the output voltage and the input supply voltage. The relation between the output voltage and the input voltage is a function of the duty cycle D ($0 \le D \le 1$), given in (2.26).

$$\int_0^{T_S} v_L dt = \int_0^{t_{ON}} v_L dt + \int_{t_{ON}}^{T_s} v_L dt = 0 \tag{2.24}$$

$$(V_{input} - V_{output}) t_{ON} = V_{output} (T_s - t_{ON}) \tag{2.25}$$

$$\frac{V_{output}}{V_{input}} = D \tag{2.26}$$

If the losses in the circuit are neglected, the relationship between the input and the output currents is given by (2.27).

$$\frac{I_{output}}{I_{input}} = \frac{1}{D} \tag{2.27}$$

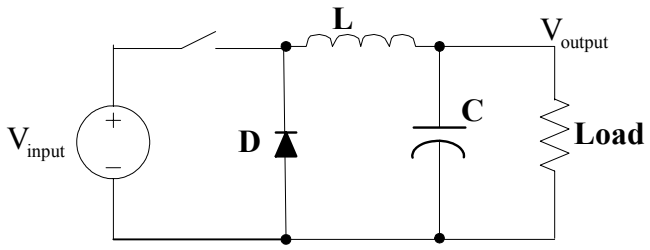

Fig. 13. Buck converter

Using a current feedback, a buck converter can be made to mimic a current source. The current feedback controls the duty cycle D of this converter till a constant current output is achieved, and it is the topic of discussion in the next section.

The current ripple is given by (2.28).

$$\Delta I_L = \frac{V_{output}}{L}(1-D)T_S \tag{2.28}$$

7. Average model of a buck converter

The diode in a buck converter can be represented by an effective voltage source of magnitude $V_{effective\_diode}$ given by (2.29) [11].

$$V_{effective\_diode} = DV_{input} \tag{2.29}$$

Since the average voltage drop across the inductor is zero, this voltage appears at the output of the buck converter (Fig. 14). The lowpass LC filter smoothens the output voltage, therefore the $V_{effective\_diode}$ appears across the load. Thus,

$$V_{output} = DV_{input} \tag{2.30}$$

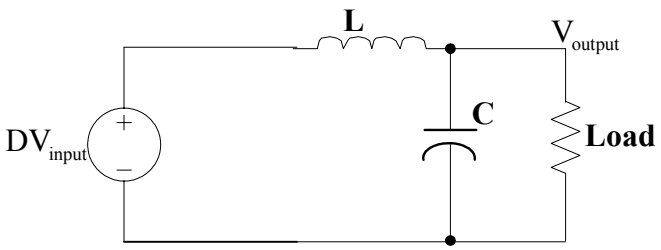

Fig. 14. Average model of a buck dc-dc converter

8. Cuk dc-dc converter

As mentioned previously, the Cuk converter [9, 10] is capable of stepping down the input voltage as well as boosting the input voltage. Fig. 15 illustrates the topology of a Cuk converter. The average current flowing through the coupling capacitor C_{out} is zero, and hence the ratio of the output voltage V_{output} to the input voltage V_{input} is given by (2.31).

$$\frac{V_{output}}{V_{input}} = \frac{D}{1-D} \tag{2.31}$$

and for current

$$\frac{I_o}{I_i} = \frac{1-D}{D} \tag{2.32}$$

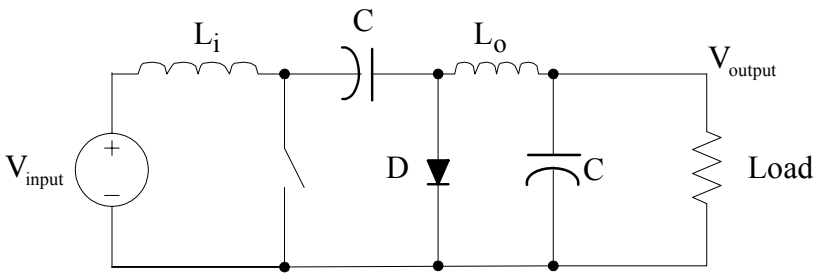

Fig. 15. Cuk converter

III. EXISTING TOPOLOGIES

1. Bipolar switching Voltage Source Inverter based drive

The most popular drive for a BLDC motor is the topology supplied by a Voltage Source Inverter [3, 4], illustrated in Fig. 16 and the control part is shown below the inverter and the motor. The main components of a VSI are the six transistor switches and an anti-parallel diode across each switch to maintain the current continuity. It consists of an inner current loop — three current sensors, I_a, I_b and I_c, and compared constantly with the reference currents I_a^*, I_b^* and I_c^* (obtained from the speed control) by means of hysteresis Schmitt Trigger.

The speed is controlled by means of an outer speed loop that generates a speed error from the difference between the desired speed and the speed measured from Hall position sensor outputs using a PI regulator.

The position of the rotor shaft field is sensed by means of Hall position sensors, thus synchronizing the back-emfs and the respective phase currents, and a rectangular 120° current waveform is supplied to each of the phases of the BLDC motor. The current profile is maintained by means of PWM switching of the VSI switches.

Since a VSI needs sufficient deadband between the turning-off of a switch and the turning-on of the complementary switch in the same inverter leg, this topology may suffer from a fatal short circuit in any of the inverter legs. Also, in order for the current to follow a rectangular profile, high switching frequency has to be used. If the switching frequency is high, the anti-parallel reverse recovery diodes have to be of the fast-recovery type. The disadvantages are obviously, the switching losses in the inverter switches. In order to reduce the switching stresses, particularly at turn-off, snubbers (consisting of capacitors, diodes and resistors to reduce the voltage spikes due to the inductive elements in the circuit) have to be used across the power switches. These switching losses entail the use of heatsinks for dissipating the power generated in the hard switchings [5]. A high switching frequency also gives rise to undesirable high frequency electromagnetic noise that may

require to be suppressed. Thus, the overall cost of the system is composed of not only the power transistor switches, but also includes the cost of the heatsinks, fast-recovery diodes and noise suppressors.

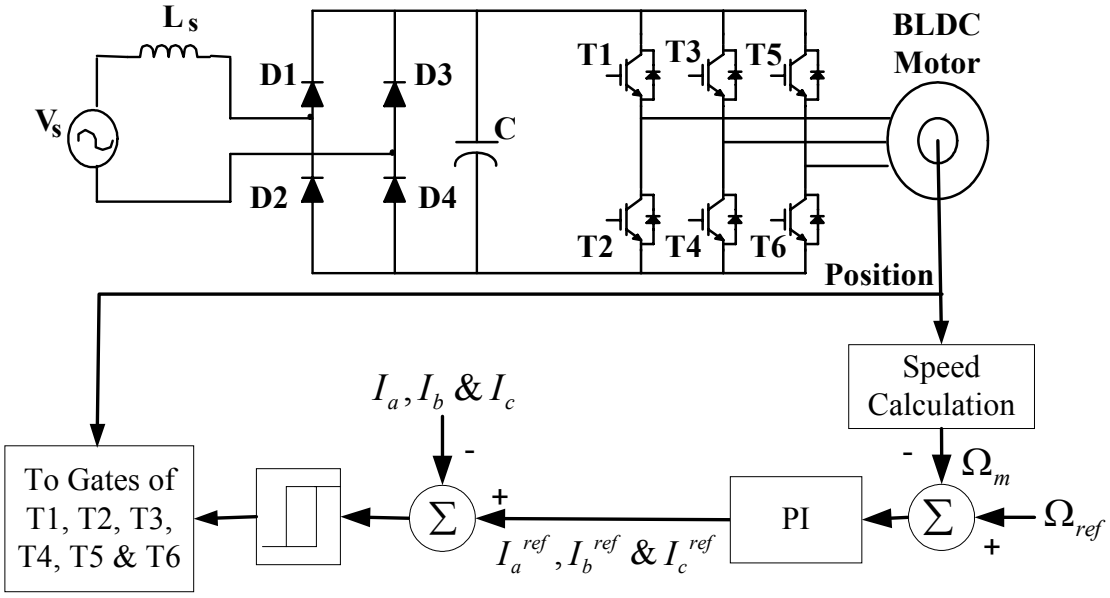

Fig. 16. Voltage Source Inverter BLDC drive topology

2. Unipolar switched drives

Unipolar switched BDLC drives (Fig. 17) have the advantage that the flow of the current is limited to one direction [3, 12]. Another advantage is that the voltage drop induced by the devices is halved; and this fact is critical in drives supplied by low voltages, thereby, increasing the efficiency of the drive. Since all the switches have the same ground as the control part of the circuit, expensive isolated transistor drivers can be eliminated. As can be observed from Fig. 18, the sum of the three phase currents does not equal zero, that is

$$i_a + i_b + i_c \neq 0 \tag{3.1}$$

This implies that a neutral connection is required. Another disadvantage is that the winding utilization of the motor is halved, leading to a halving of the torque as compared to the bipolar switching topology in Fig. 16.

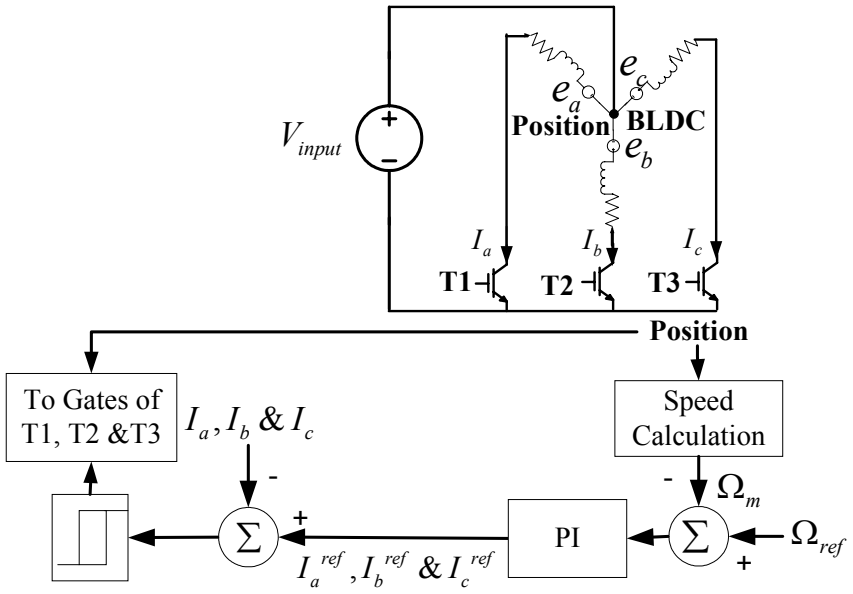

Fig. 17. Unipolar switched BLDC drive

3. Rectifier and Current Source Inverter topology

In a VSI (a six-switch inverter), a large dc link capacitor is used for holding the dc bus at a 'stiff' voltage. This capacitor also sinks in the harmonics that are generated, and high frequency harmonics adversely affect the life of this capacitor. Since the dc bus is 'stiff', the input current is highly discontinuous and has a high frequency component that adversely affects the utility grid. Consequently, the displacement factor and the distortion factor are highly unfavorable. An active filter arrangement may be needed to improve the power factor.

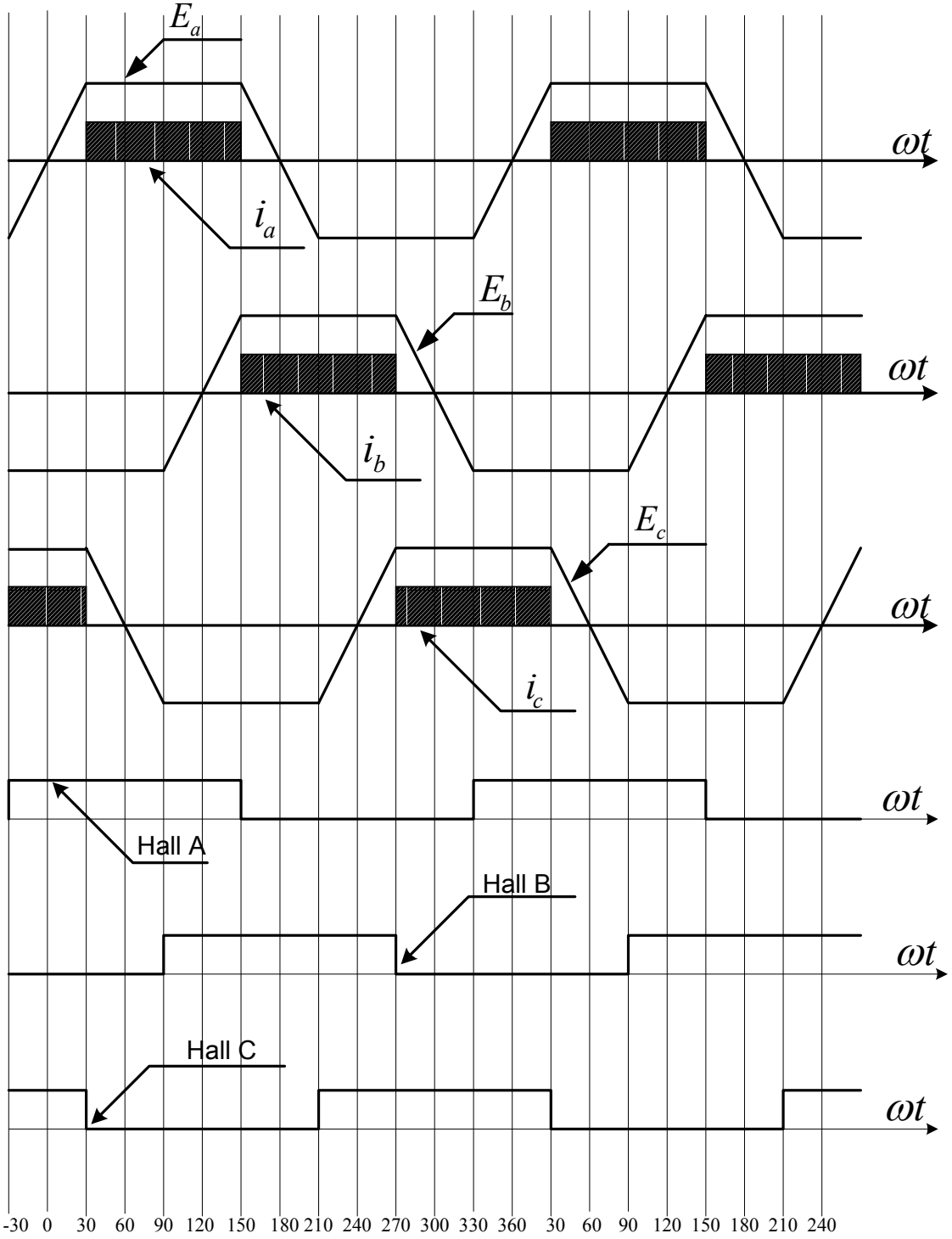

Fig. 18. Back-emfs, currents and Hall sensor outputs - Unipolar switching

If a synchronous machine operates with a leading power factor, then it is well known that a Current Source Inverter (CSI) can be used to drive it. This fact is used in large drives and in starting gas-turbines/engines connected to synchronous machines which act as motor drives during startup, and then as generators.

The CSI topology (Fig. 19) uses thyristors as switches instead of IGBTs for driving the motor. A controlled rectifier and a dc link inductor mimic a current source supply for the CSI. The CSI drives the BLDC motor by supplying it with a three-phase rectangular waveform. The size of the dc link inductor is determined by the difference in voltage across the inductor, that is, the maximum difference between the motor back-emf and the input supply voltage. The controlled rectifier could be either a three-phase rectifier [13] or a single-phase rectifier [5]. Since the voltage ripple in a three-phase rectifier arrangement is lower than that of a single-phase rectifier arrangement, for a given BLDC motor and load, the value of the three-phase dc link inductor is less than the value of a single-phase dc link inductor.

If the phase current leads the phase back-emf, natural commutation of thyristors can take place [5, 13]. This is essential for CSI, since the next thyristor has to be gated a few degrees before it is supposed to be switched on, else it may not have sufficient time to turn on and the desired switching state may not be achieved. Since no heatsink is required for thyristors, the cost and weight of the inverter is reduced substantially. The main advantage of this topology is that the switching losses are kept to a minimum [14].

4. Calculation of inductance of rectifier and CSI drive

The required inductance, for a half horsepower Electro-Craft®, full-load current of 5.4 A, rotating at 1800 r.p.m. (it is the standard of comparison for all the topologies) is estimated in this section. Assume that the ripple induced by the fact that the current leads the phase back-emf is negligible. The inductor would be most stressed when the rectified ac supply is zero and current has to be supplied to the motor in order to maintain the speed. The phase-to-neutral back-emf (E) induced in the motor is given by

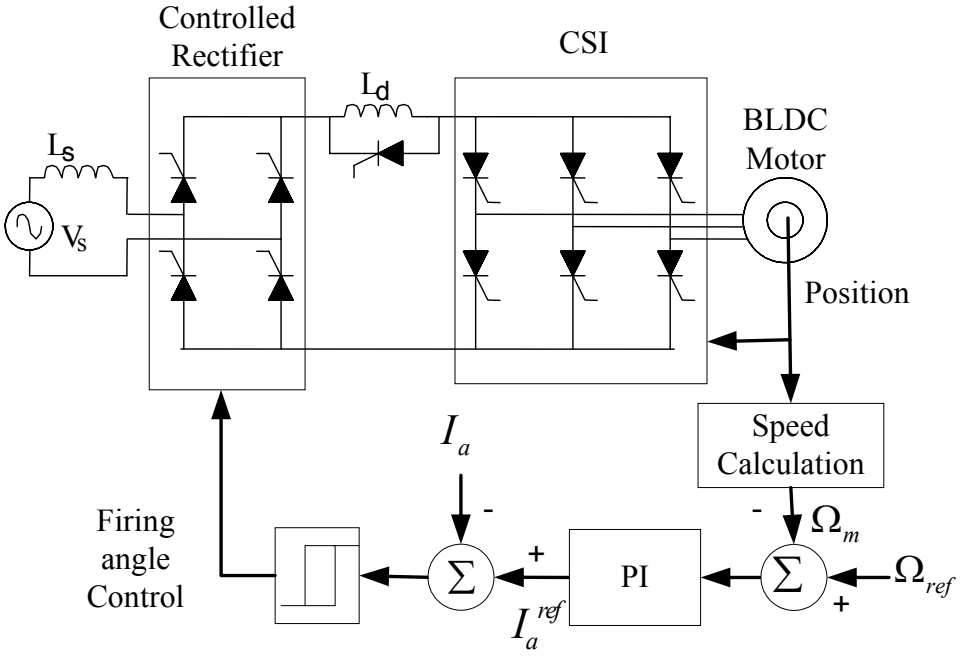

Fig. 19. Controlled rectifier fed BLDC drive

$$E = K_E \omega_m = 33.255 \text{ V} \tag{3.2}$$

The rectified ac supply is of the form

$$v_{rectified} = 157 \sin(\omega t) \tag{3.3}$$

Therefore, the inductor has to supply current for time t_{hold} till the rectified ac voltage equals or exceeds the motor back-emf, [15]

$$33.255 = 157 \sin(\omega t_{hold}) \tag{3.4}$$

Solving the above equation,

$$t_{hold} = 5.6615 \times 10^{-4} \approx 1\text{ms} \tag{3.5}$$

This implies that the rectified ac and the motor back-emf coincide at an electrical angle of 12.227°, assuming a frequency of 60 Hz.

Since current loop has to be much quicker than 1 ms, the dc link inductor must be able to withstand a drop of 33.255 volts for approximately 1 ms, without having a current ripple of more than 5%. Therefore, equating the voltage drops [16] in (3.6) we get

$$Vdt = Ldi \tag{3.6}$$

This gives that the value of the dc link inductance is approximately 120 mH. An accurate analysis that takes into account the area under the difference in voltages gives a value of 90 mH.

Therefore, in order to maintain the speed of the motor, the dc link inductor releases its stored energy and makes up for the difference between the motor back-emf and the rectified ac supply.

From weight considerations, a disadvantage of this topology is the size and value of the inductor used to mimic a current-source. For a half horsepower BLDC motor (Electrocraft® E-3633 Series) drive, a 120 mH inductor (5 p.u.) was used. The cost of this inductor was mentioned to be $5.22. The dc resistance of the inductor was 7.7 Ω (approximately 1 p.u.) [5]. This can cause a large power dissipation leading to a reduced efficiency. In the proposed topology, this problem is addressed by reducing the size of the inductor.

5. Current commutation phenomenon in CSI

The transfer of current from one phase to another phase, as per the desired pattern of current and voltages is called ‘commutation’ [10]. Ideally, the transfer of current should occur without a glitch, but because of imperfections, there may be a ‘dip’ at the midpoint of a 120° conduction interval of the current waveform. This dip causes a decrease in torque production during commutation, thus causing torque ripple. Assuming that the BLDC is a ‘three-phase voltage source’, the analysis during the commutation interval is the same as that of a three-phase controlled rectifier.

If the phase currents lead the corresponding motor back-emfs, natural commutation of the thyristor is possible, assuming that the commutation interval (μ) is negligible in comparison to the conduction interval. In Fig. 20, phase 'A' is conducting and transfer of current is supposed to take place from phase 'B' to phase 'C', that is thyristor T4 turns off, and thyristor T6 turns on. Current i_a is assumed to be constant and equals the dc link current. Before the commutation interval, i_b was the other phase which was conducting, and as soon as T6 is turned on, it is assumed that the current transfers from T4 to T6. This makes use of the fact that a thyristor turns off if its cathode potential exceeds its anode potential, and the back-emf of the BLDC motor makes it possible to commutate. Since the back-emf of the motor is proportional to the motor speed, at low speeds, the back-emf may not be sufficient to commutate the thyristors, hence the dc link current may have to be forced to zero for commutation to take place. In other words, when the CSI is operated in the rectifier mode (the gating signals of the lower and upper thyristors are interchanged), the dc voltage e_{out} (may contain ripples), is observed at the output of this rectifier. This is used as a test to check the proper performance of the drive logic in the open-loop without risking any damage to the system.

The commutation interval (μ), [5] is given by

$$u^2 - \frac{\pi}{3}u + \frac{2\pi\omega L}{3E} I_{dc} = 0 \tag{3.7}$$

where

μ = Commutation interval

ω = Electrical frequency of motor

L = Motor phase inductance

I_{dc} = Magnitude of motor phase current just before commutation interval

E = Peak of the back-emf of the motor

The commutation waveforms are illustrated in Fig. 21.

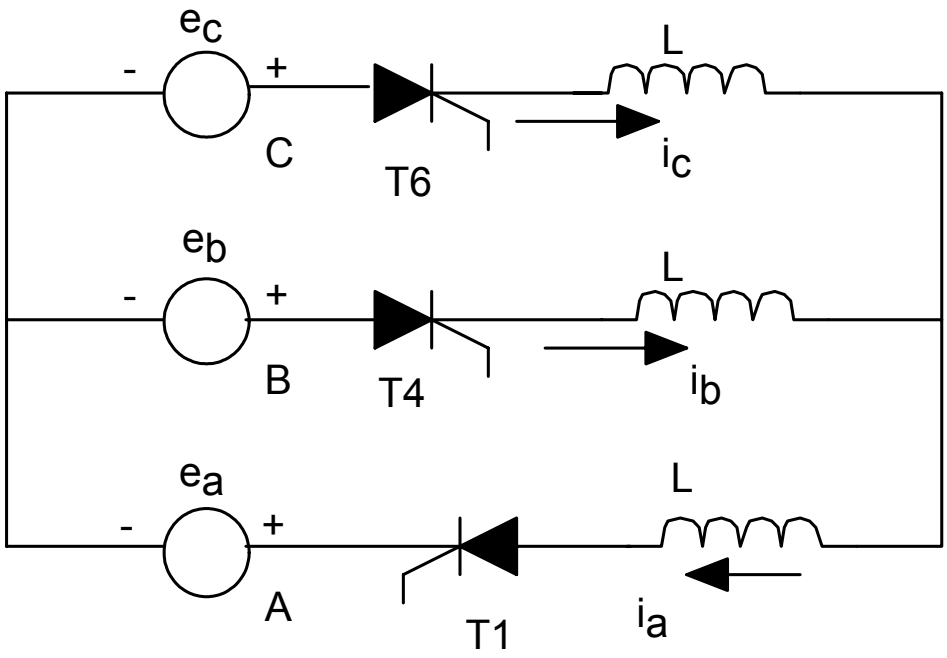

Fig. 20. Circuit during commutation

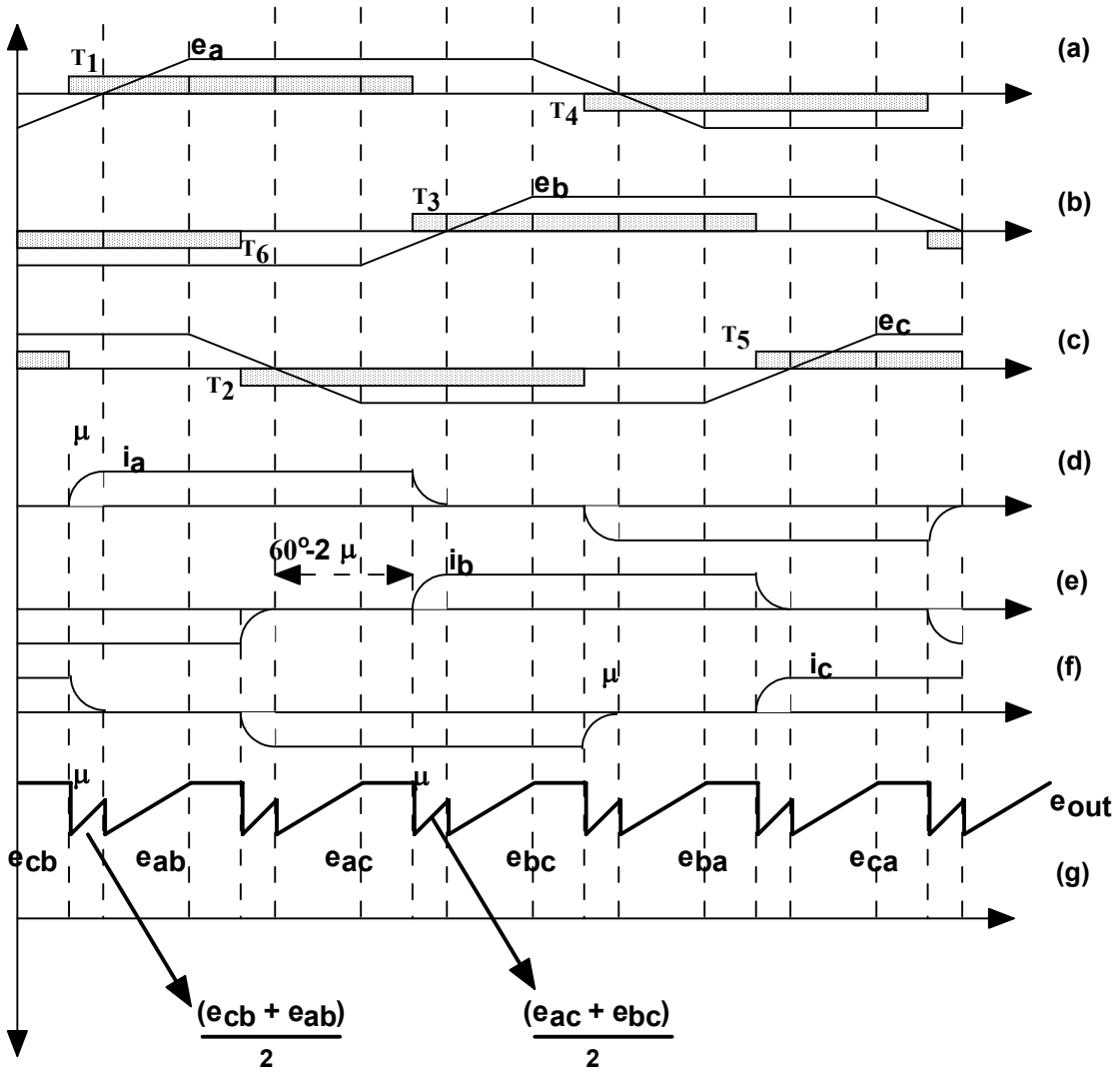

Fig. 21. Waveforms illustrating commutation

IV. PROPOSED DRIVE TOPOLOGIES

1. Limitations of a traditional Current Source Inverter drive

Under the best of conditions, assume that the dc voltage source is a constant and the CSI is supplied by a constant voltage source through an inductor. The value of the inductor (4 p.u.) as calculated in section 3.4 is significant and needs to be reduced in order to reduce the weight as well as the resistive losses in the system. The drive topologies that are proposed to reduce the value of the dc link inductance are explained in this section.

2. Proposed buck fed topology

The aim is to design a rugged and low-cost drive, supplied by a battery, using a BLDC motor. In Fig. 16, the VSI inverter uses IGBTs and requires a heatsink. A thyristorized drive is the obvious choice for ruggedness and lack of heatsinks. The use of thyristors implies that load commutation has to be utilized for proper operation of the CSI. As previously known, the relatively big size of the dc link inductor implies a sluggish dynamic response of the drive. For applications that depend on a battery supply for input, the cost of the topology in Fig. 19 is heavily dependent on the cost of the inductor.

It has been demonstrated by simulation that it is possible to reduce the size of the inductor to approximately 2 mH (an identical motor has been used for comparison) by using a current source incorporating high frequency switching (Fig. 22). This improves the dynamic response of the drive by allowing the current profile to change rapidly in order to correspond to the changing speed profile. Therefore, it is possible to use either a buck or a Cuk converter since they have an inductor in their output that makes it possible to supply a CSI. The size of the inductor can be reduced if the frequency is increased because the current ripple (and hence the torque ripple) is inversely proportional to Lf_s where f_s is the frequency of the chopper switchings [10]. For a buck converter, the current ripple is determined by (4.1)

$$\Delta i_L \approx \frac{1}{L}\int_0^{DT_s} V_{dc}\,dt = \frac{V_{dc}DT_s}{L} = \frac{V_{dc}D}{Lf_s} \tag{4.1}$$

It is very pertinent to note that the dc supply be relatively constant, else a larger size of the dc link inductor would be required, thus degrading the response of the system.

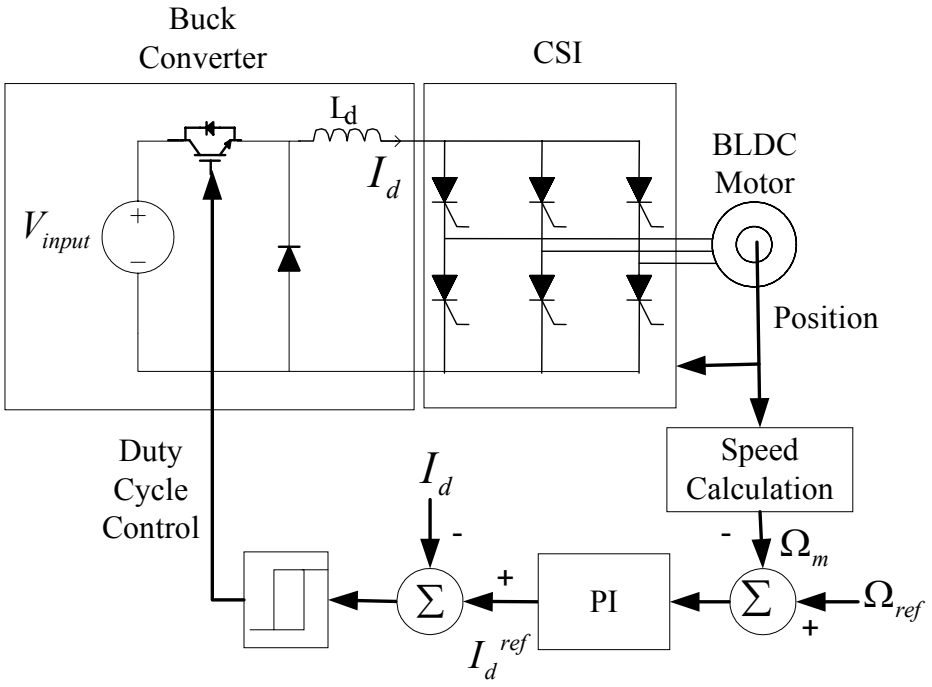

Fig. 22. Proposed buck fed CSI drive

3. Analysis and modeling of the proposed buck fed drive

The block diagram is shown in Fig. 23. The CSI has been represented by a power amplifier block called “Load Commutated Inverter (LCI)”. The dc-dc converter is a buck converter, hence can only step down the battery voltage. Therefore, the battery needs to have sufficient voltage to overcome the back-emf of the motor at the highest speed in the desired control range.

The DSP Controller is a fixed point TMS320F243 from Texas Instruments, and that is enclosed in a block responsible for all the control functions. As observed, the DSP processor is very powerful, compact and multi-functional, containing many inbuilt modules like the Analog-to-Digital converter, Capture Units for sensing the change in rotor field position, and the computations performed on it implement the hysteresis current control and the PI speed regulator.

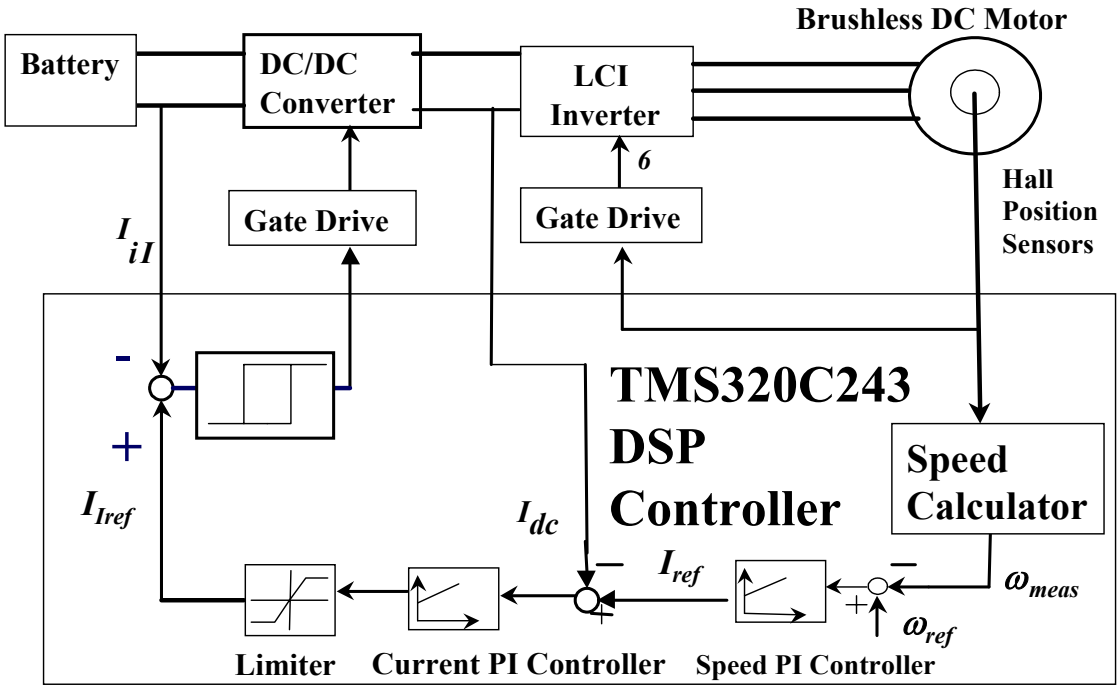

Fig. 23. Plan of action – Overall system block diagram

Using the transfer function for a BLDC motor we get

$$\frac{\Omega_m(s)}{V(s)} = \frac{\frac{K_T}{JL_a}}{s^2 + (\frac{JR_a + BL_a}{JL_a})s + (\frac{BR_a + K_T K_E}{JL_a})} \tag{4.2}$$

where $V = DV_{input}$, D being the duty cycle of the buck converter.

Using another form of the transfer function, we have (4.3)

$$[JL_a s^2 + (JR_a + BR_a)s + K_T K_E]\Omega_m(s) = K_T V(s) + R_a T_{load}(s) \tag{4.3}$$

If a PI control is applied to this system, then the applied voltage is a sum of the speed error scaled by a proportional constant and the error sum scaled by an integral constant. [17].

$$v = k_p \omega_{error} + k_I \sum \omega_{error} \tag{4.4}$$

With a PI controller for feedback, the transfer function becomes

$$[JL_a s^2 + (JR_a + BR_a)s + K_T K_E]\Omega_m = (k_P + \frac{k_I}{s})K_T(\Omega_{ref} - \Omega_m) + R_a T_{load}(s) \tag{4.5}$$

Rationalizing, and collecting coefficients of the same order, we have

$$[JL_a s^3 + (JR_a + BR_a)s^2 + sK_T K_E]\Omega_m = (sk_P + k_I)K_T(\Omega_{ref} - \Omega_m) + sR_a T_{load}(s) \tag{4.6}$$

$$[JL_a s^3 + (JR_a + BR_a)s^2 + (K_T K_E + k_P K_T)s + k_I K_T]\Omega_m = (sk_P + k_I)K_T\Omega_{ref} + sR_a T_{load} \tag{4.7}$$

At steady state, $s = 0$, (4.7) reduces to

$$k_I K_T \Omega_m = k_I K_T \Omega_{ref} \tag{4.8}$$

If $k_I \neq 0$, it is observed that the measured speed equals the reference speed as in (4.9)

$$\Omega_m = \Omega_{ref} \tag{4.9}$$

From (4.7),

$$\Omega_m = \frac{(sk_P + k_I)K_T\Omega_{ref} + sR_aT_{load}}{JL_as^3 + (JR_a + BR_a)s^2 + (K_TK_E + k_PK_T)s + k_IK_T} \tag{4.10}$$

Assume $\Omega_{ref} = 0$ and $T_{load} = \frac{T_0}{s}$ and applying the final value theorem to (4.10), we get

$$\lim_{t\to\infty} \omega_m = \lim_{s\to 0} s\Omega_m(s) \tag{4.11}$$

$$\lim_{t\to\infty} \omega_m = \lim_{s\to 0} s\frac{(sk_P + k_I)K_T\Omega_{ref} + sR_aT_{load}}{JL_as^3 + (JR_a + BR_a)s^2 + (K_TK_E + k_PK_T)s + k_IK_T} \tag{4.12}$$

$$\text{or } \lim_{t\to\infty} \omega_m = 0 \tag{4.13}$$

and hence, a PI controller can be used to control the speed of a BLDC motor. Fig. 24 represents the closed loop model of a BLDC drive.

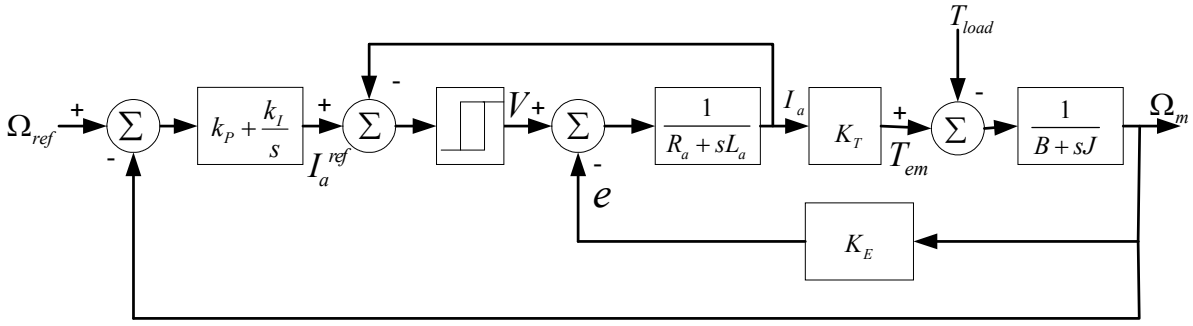

Fig. 24. Closed loop control of a BLDC motor by buck converter and CSI

4. Simulation results of the proposed buck fed drive

The simulation was performed using the circuit simulator "PSIM" [18]. The results in Fig. 25 prove that the measured speed of the proposed drive follows the speed profile

The parameters of the drive used were:

Rotor moment of inertia = 0.0032 kg.cm.s^2

Damping constant = 0.0024 kg.cm/rpm

Square wave (K_T) torque constant = 2.3 kg.cm/A

Voltage constant (K_E) = 0.024 V/rpm

Winding resistance, phase-to-phase = 0.63 Ω

Winding resistance, phase-to-neutral (R_a)= 0.315 Ω

Winding inductance, phase-to-phase = 3.4 mH

Mutual inductance (M) = 0.68 mH

Continuous stall torque (τ_{stall}) = 11.2 kg.cm

Peak torque (τ_{peak}) = 52.2 kg.cm

Number of poles (P) = 4

Lead angle for commutation (θ_{lead}) = 10°

Mechanical time constant = 0.1 s

Conduction pulse width = 120°

Fig. 26 illustrates the phase current waveform of a BLDC motor, Fig. 27 shows the dc link current. Fig. 28, Fig. 29 and Fig. 30, respectively illustrate the produced torque, the source current and the motor phase voltages.

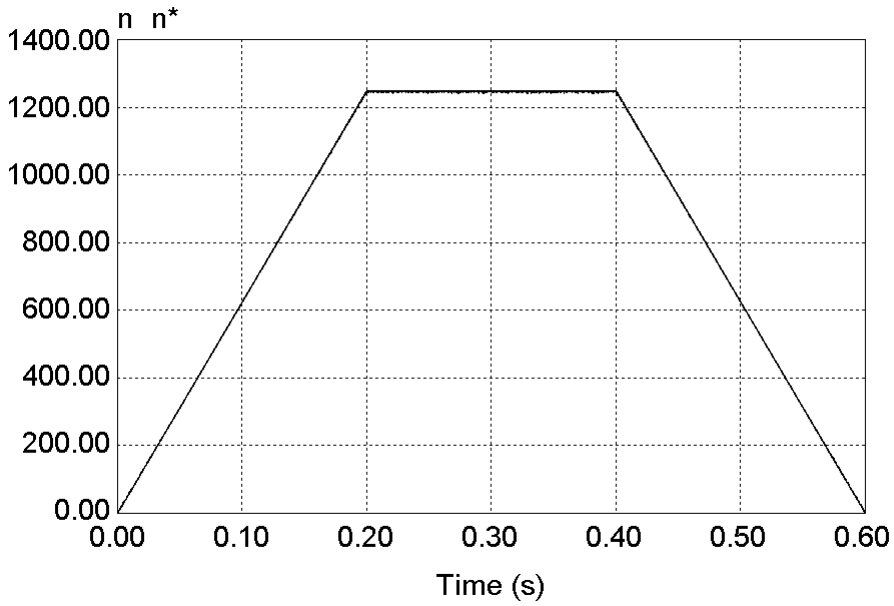

Fig. 25. Reference and measured speeds for a buck fed BLDC drive

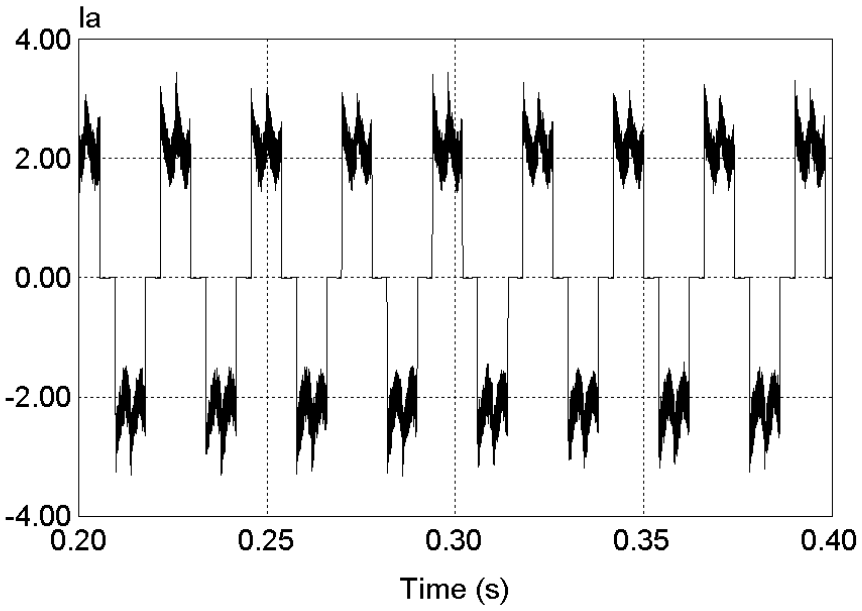

Fig. 26. Phase current waveforms of a buck fed BLDC drive

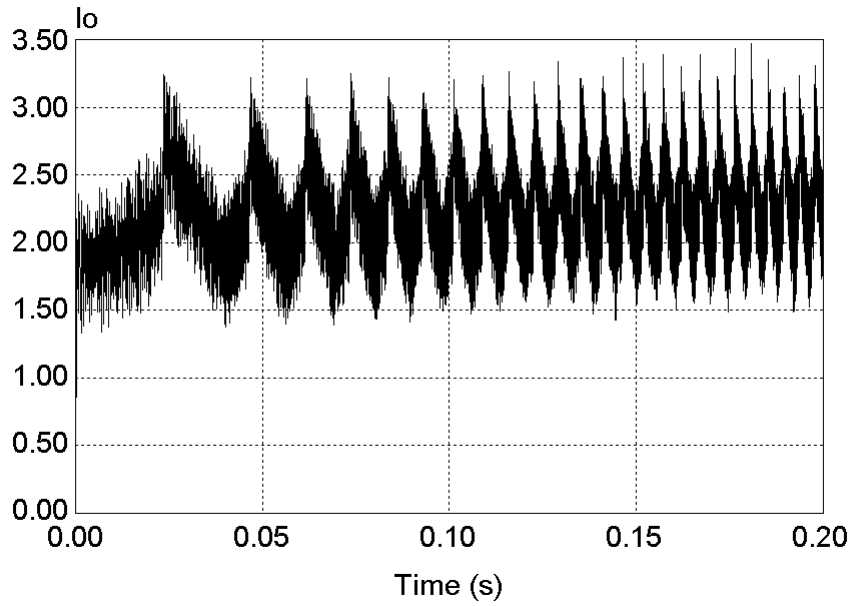

Fig. 27. Dc link current of a buck fed BLDC drive

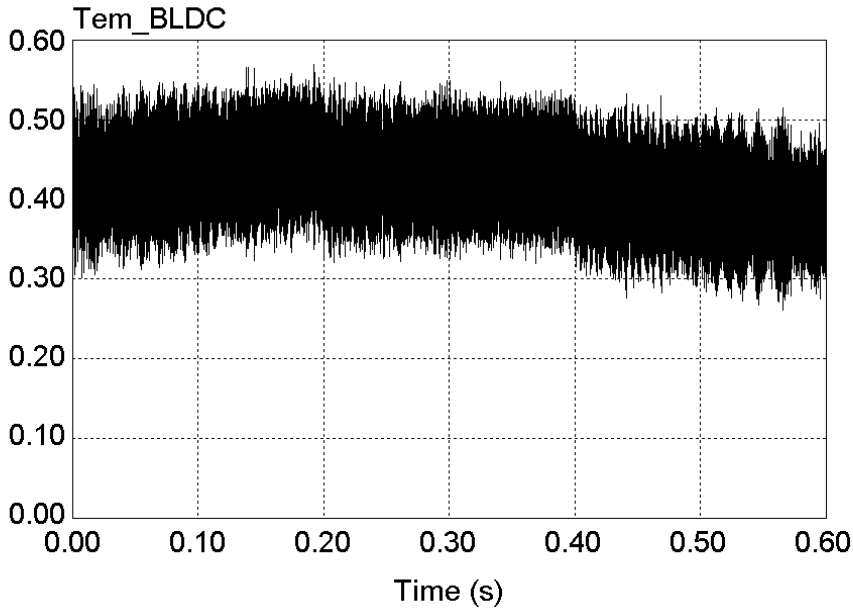

Fig. 28. Torque – rising, constant and falling part of speed profile of a buck fed drive

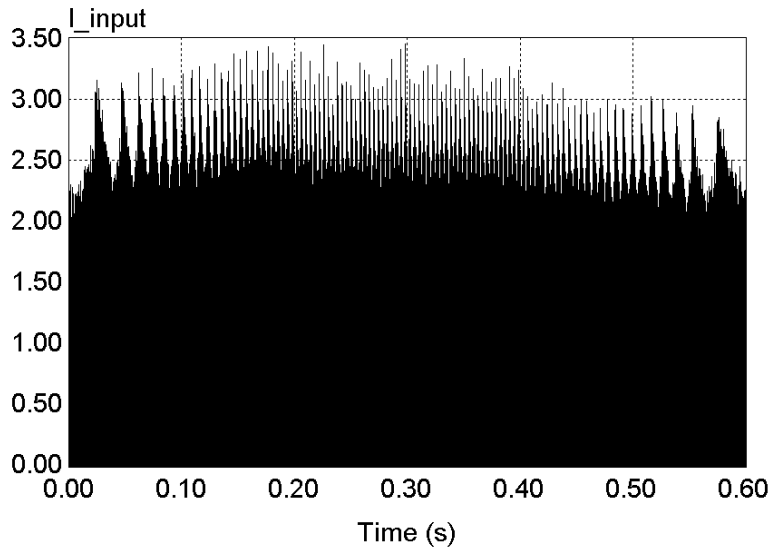

Fig. 29. Input current drawn from source by a buck fed BLDC drive

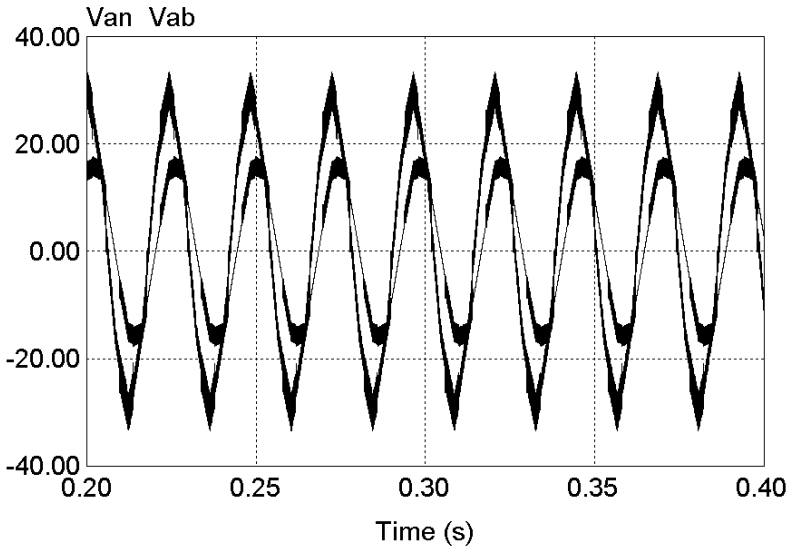

Fig. 30. Phase-to-neutral voltage and phase-to-phase voltage of buck fed drive

5. Design of inductor

Since hysteresis technique has been used to control the current, the switching frequency varies from 1 kHz to 20 kHz; an approximate value of the inductor is calculated by putting an inductor and observing the minimum frequency of switching. The dc link inductor should be able to supply the required current without saturating. At 1800 rpm, the back-emf of the motor is 33.255 V. When the voltage across the free-wheeling diode is zero; and across the inductor, a voltage of 33.255 V should be induced in 1 ms. Using analysis techniques described in section 3.4, the approximate value of the dc link inductance is found to be 2 mH.

6. Comparison — dc supplied VSI and CSI BLDC drive

The cost comparison of the proposed drive is given in Table I.

TABLE I

COST ANALYSIS OF BUCK FED CSI DRIVE IN FIG. 22

Component	Proposed Drive		VSI Drive	
	Quantities	$	Quantities	$
IGBT	1	0.75	6	4.50
SCR	6	1.5	---	---
Inductor	1 (few mH)	1	1 (few mH)	1
Fast Recovery Diode	1	0.45	1	0.45
Heat Sink for IGBT's	1	1	7	3.5
Gate drive		4.00		$3.00
PCB, DSP, Op-amps etc.		4.85		$4.85
Total material cost		**$13.55**		**$17.30**
Cost reduction	**21.6%**		**0%**	

7. Proposed topology for ac supplied BLDC drive

Compared with the IGBT based inverter used in conventional drives, this SCR based inverter (Fig. 31) has the following advantages. First, the SCR based inverter reduces the drive cost by about 30%. Second, it has negligible switching losses, and therefore it is more efficient and reliable than an IGBT based inverter [19].

Since the dc-dc converter used in this drive has an inductor at its front-end, the input current drawn from the ac source can be controlled to achieve better power factor. Moreover, since the ac-dc converter works like a buck-boost converter, it is able to boost the supply voltage to the motor. When supplied from a battery, the output voltage of the battery drops with time and the it has to be boosted; this ability can make the drive more efficient and compact.

8. Small signal analysis of the proposed ac supplied drive

The proposed BLDC drive consists of three parts (1) diode bridge rectifier (2) dc-dc voltage to current converter and (3) the SCR based inverter and the BLDC motor. The models of these three parts are shown in Fig. 32 a, b and c respectively. The diode bridge and the sinusoidal ac source are modeled by a rectified sinusoidal ac voltage source. Assuming that the CSI is ideal, we need to consider only the distortion due to the phase advance in the thyristor gating. The CSI rectifies the back-emf of the BLDC so that it appears as if it were a dc motor. Thus, the problem reduces to that of controlling a dc motor with a slightly distorted back-emf. The SCR based inverter together with the BLDC motor is modeled by a voltage source $E_{t.}$

where:

e_{ph} = back-emf voltage induced in each conducting motor phase winding (V)

v_c = voltage ripple due to commutation (V)

ω = rotor angular speed (rad/sec)

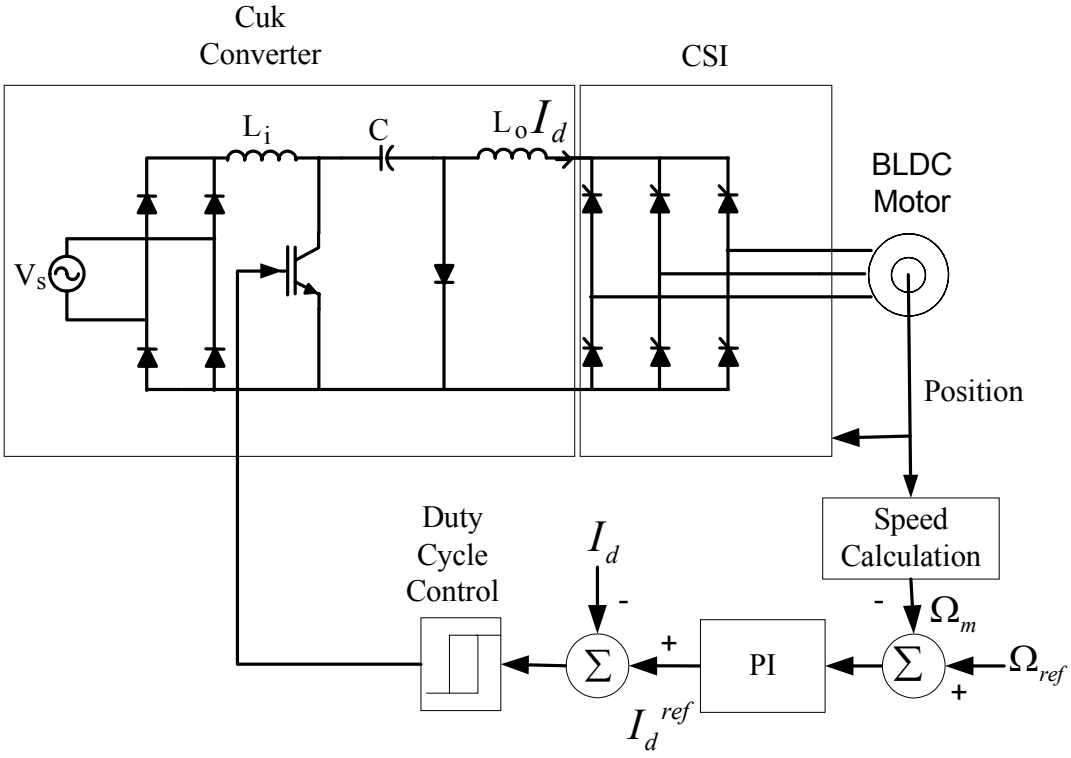

Fig. 31. Cuk converter fed CSI BLDC drive

The voltage source E_t can also be considered as a rectified three-phase source of magnitude corresponding to the phase-to-phase back-emfs of a BLDC motor. Viewed from the side looking into the motor, the CSI mimics a controlled rectifier, and the pulsation of E_t depends on the firing angle of the SCRs, which in our case is 10°.

The voltage ripple v_c is due to the current commutation in the SCR-based inverter. The shape, peak value and the frequency of this ripple depend on load current, the motor leakage inductance and the motor speed. The detailed analysis of this ripple for BLDC motor is presented in [5].

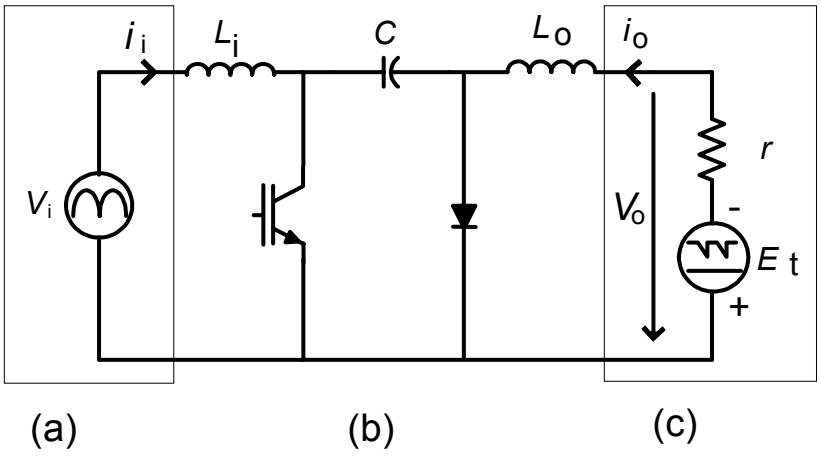

Fig. 32. Electrical model of the proposed Cuk fed CSI BLDC drive

9. Average model of the Cuk fed drive

The dc-dc voltage to current converter behaves like an adjustable dc current source, which supplies the motor via the inverter. This converter is made by modifying the Cuk converter. In this converter, the average output current is regulated by controlling the on and off durations (t_{on} and t_{off}). By employing a constant switching frequency of $f_s=1/T_s$, we have

$$T_s = t_{on} + t_{off} \tag{4.14}$$

To analyze the converter operation at steady state, we assume that

(1) Both inductors are very large and their currents are constant.

(2) The capacitor is very large and the voltage across it is constant

(3) For the duty ratio *D,* the switch is closed for DT_s and open for $(1-D)T_s$

(4) The switch and diode are ideal

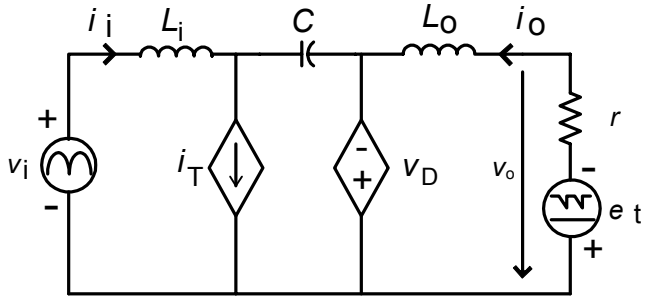

Fig. 33. Average model of Cuk fed CSI BLDC drive

The average model, (Fig. 33) has the diode replaced by a voltage source V_D equal to the average voltage across the diode and the switch is replaced by a current source i_T. At steady state, the average inductor voltages V_{L_i} and V_{L_o} are zero. Therefore

$$V_C = V_i + V_o \tag{4.15}$$

Hence the diode D sees the average voltage across the capacitor C [11]. Therefore

$$V_D = DV_C \tag{4.16}$$

For the time duration DT_s, when the switch is on, the diode is off and the current in the capacitor is given by (4.17).

$$(i_c)_{on} = -i_o \tag{4.17}$$

For the time duration $(1\text{-}D)T_s$, the switch is off, the diode is on and the current in the capacitor is given by (4.18).

$$(i_c)_{off} = i_i \tag{4.18}$$

For periodic operation, the average capacitor current is zero. Thus

$$-I_o DT_s + I_i(1-D)T_s = 0 \text{, or } \frac{I_o}{I_i} = \frac{1-D}{D} \tag{4.19}$$

The ripple in C can be estimated by computing the changes in v_c over the interval when the switch is open, i.e., (1-D)T_s. Assuming the current L_i to be constant at its average value I_i,

$$\Delta v_c \approx \frac{1}{C}\int_{DT_s}^{T_s} I_i dt = \frac{I_i}{C}(1-D)T_s = \frac{I_i(1-D)}{Cf_s} \tag{4.20}$$

The change in L_i current can be estimated based on its voltage drop ($V_{L_i} = V_i$) while the switch is closed.

$$\Delta i_{L_1} = \Delta i_i \approx \frac{1}{L_i}\int_{0}^{DT_s} V_i dt = \frac{V_i DT_s}{L_i} = \frac{V_i D}{L_i f_s} \tag{4.21}$$

When the switch is open, the voltage across L_2 is V_o, therefore, the L_o current change is

$$\Delta i_{L_o} = \Delta i_o \approx \frac{1}{L_o}\int_{DT_s}^{T_s} V_o dt = \frac{V_o(1-D)T_s}{L_o} = \frac{Vo(1-D)}{L_o f_s} \tag{4.22}$$

10. Controlling the proposed Cuk fed drive

For designing a controller, the transient behavior of the proposed drive must be analyzed. Therefore, we need to obtain the small signal model of the drive system. The dc-dc converter shown by its average model in Fig. 33, is given an ac biased signal. In this figure, the switch is replaced by a dependent current source i_T and the diode is replaced by a dependent voltage source v_D as follows

$$i_T = d(i_i + i_o) \tag{4.23}$$

$$v_d = d.v_c = d(v_i + v_o) \tag{4.24}$$

where

$$v_o = V_o + \tilde{v}_o \tag{4.25}$$

$$i_o = I_o + \tilde{i}_o \tag{4.26}$$

$$i_i = I_i + \tilde{i}_i \tag{4.27}$$

$$d = D + \tilde{d} \tag{4.28}$$

The steady state or dc term is represented by the upper case letter, the "~" (tilde) quantity represents the ac term or small signal perturbation, and the sum is the total quantity, represented by the lower case letter.

For small signal analysis, we have to calculate the average (dc) quantities, as shown in (4.14) – (4.22). To determine the ac quantities of i_T, from equations (4.23) – (4.28) we have

$$i_T = I_T + \tilde{i}_T = (D + \tilde{d})(I_i + \tilde{i}_i + I_o + \tilde{i}_o) \cong DI_i + (I_i + I_o)\tilde{d} + D(\tilde{i}_i + \tilde{i}_o) \tag{4.29}$$

$$\tilde{i}_T = (I_i + I_o)\tilde{d} + D(\tilde{i}_i + \tilde{i}_o) \tag{4.30}$$

Similarly, the ac value of v_D is derived as follows

$$\tilde{v}_D = (V_i + V_o)\tilde{d} + D(\tilde{v}_i + \tilde{v}_o) \tag{4.31}$$

The ac component of v_o is

$$\tilde{v}_o = 2k\tilde{\omega} + v_c \tag{4.32}$$

By introducing these quantities in Fig. 33, the small signal model of the drive system is obtained.

11. Simulation results for the proposed Cuk fed drive

The motor parameters are assumed to remain the same. The only difference is that we use a rectified ac source as the input. This makes the control more challenging, but nevertheless it is the ideal topology for commercial applications that are supplied from the utility.

Fig. 34 shows that the measured speed tracks the reference speed except for the overshoot at the beginning of the speed profile; Fig. 35 and Fig. 36 respectively show the produced torque and the phase current. Fig. 37, Fig. 38 and Fig. 39, respectively, illustrate the dc link current, the source input current and the motor phase voltages.

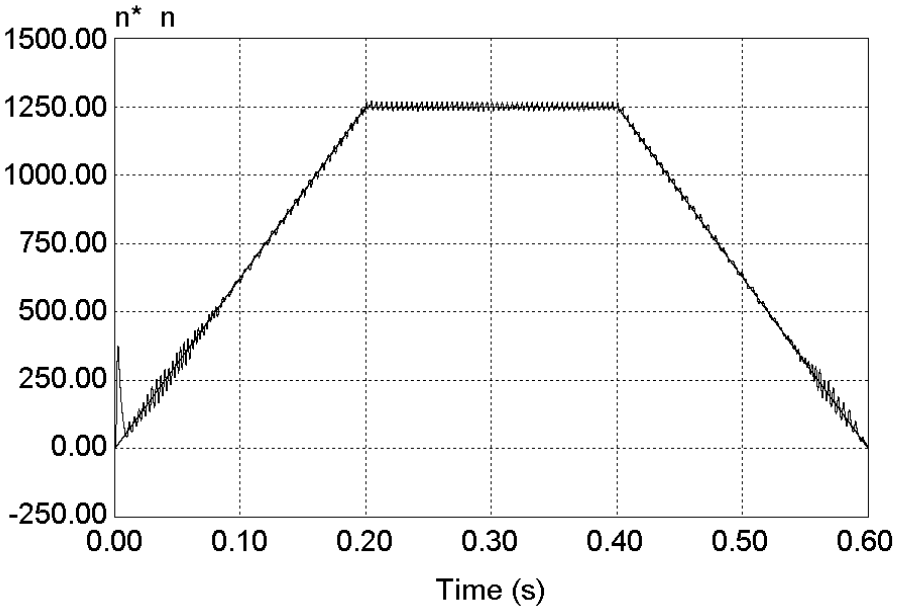

Fig. 34. Reference speed and measured speed of a Cuk fed BLDC drive

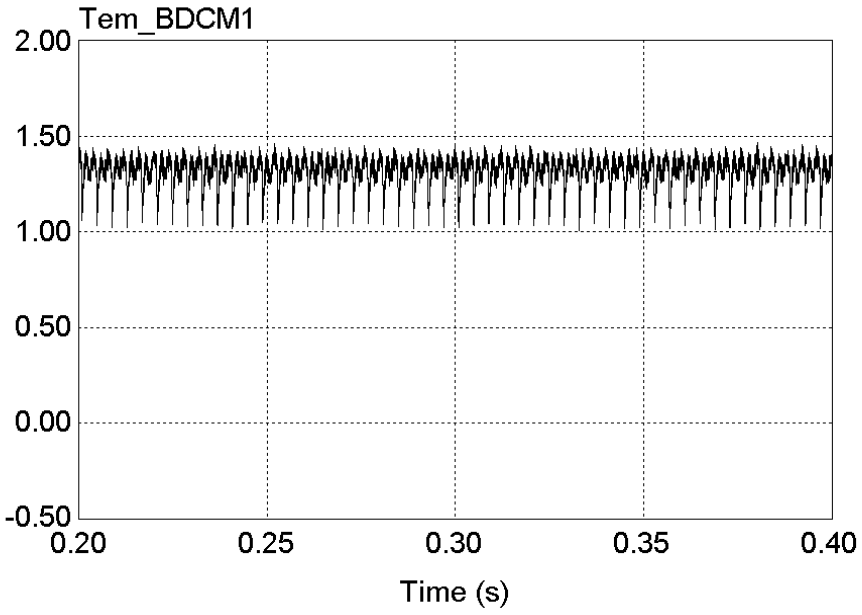

Fig. 35. Torque produced by a Cuk fed BLDC drive

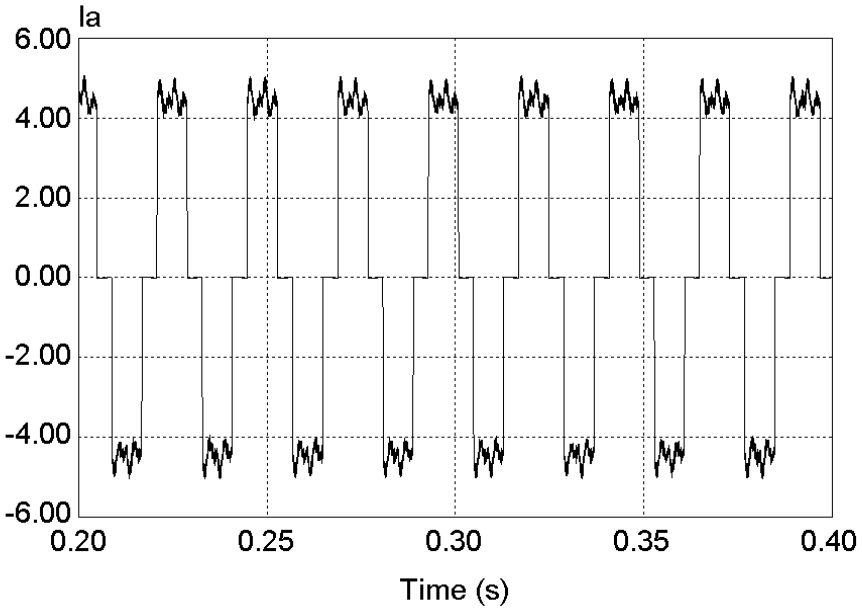

Fig. 36. Motor phase current of a Cuk fed BLDC drive

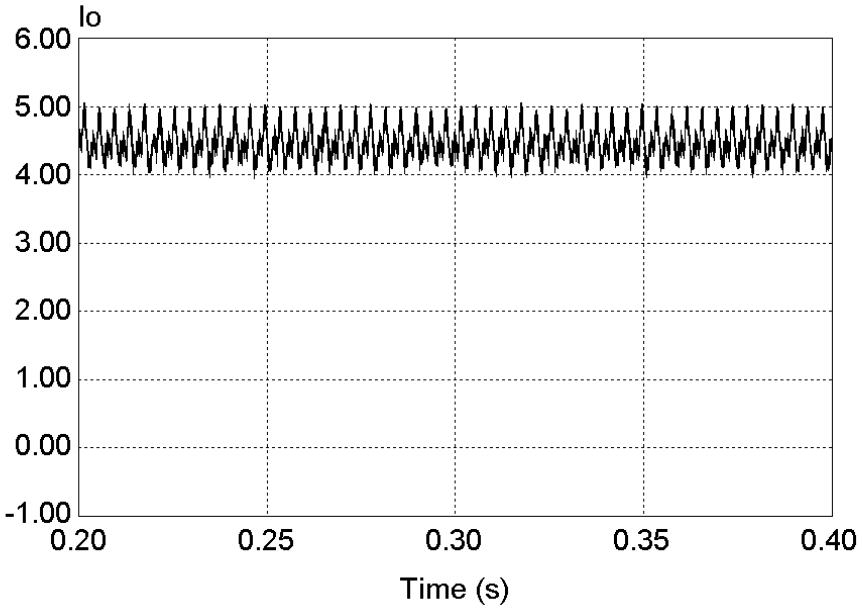

Fig. 37. Dc link current of a Cuk fed BLDC drive

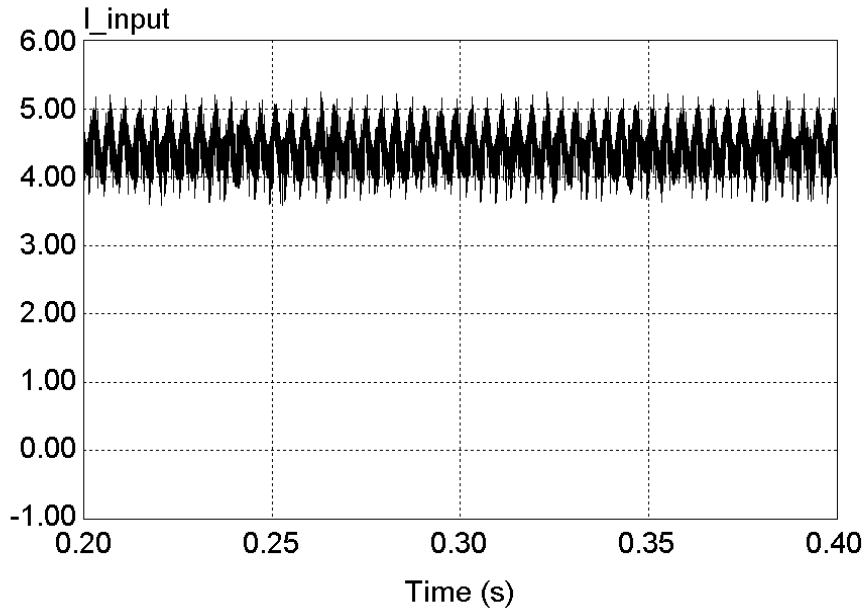

Fig. 38. Current drawn from source by a Cuk fed BLDC drive

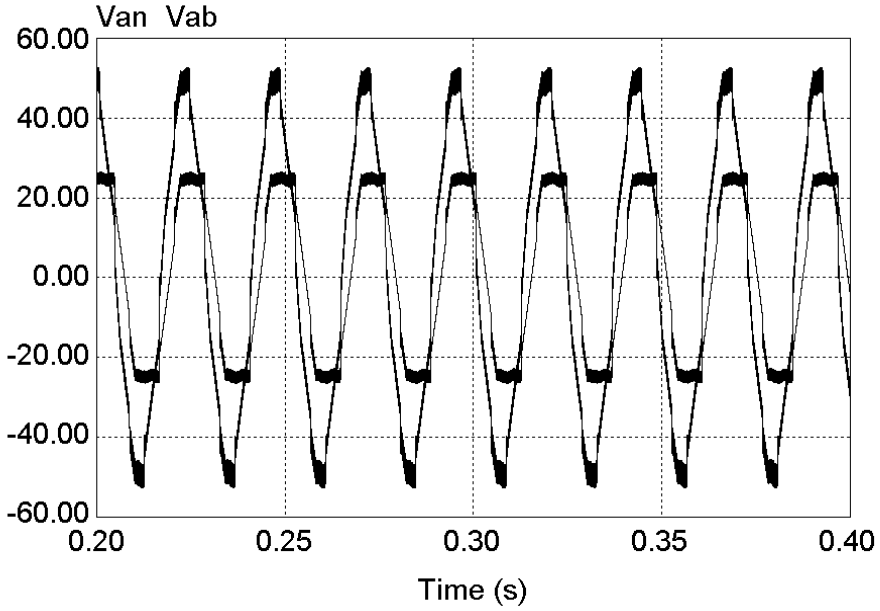

Fig. 39. Phase-to-neutral voltage and phase-to-phase voltage of a Cuk fed drive

12. Cost analysis of the Cuk fed CSI BLDC drive

Table II clearly displays the economic advantage of using the proposed topology. A cost reduction of almost 30% is achieved by using this topology. Moreover, the absence of heatsinks makes it compact and the use of thyristors makes it very rugged. Since it contains a CSI, it can recover from a short-circuit. The requirements on the coupling capacitor are that it should have a very low Effective Series Resistance (ESR). From simulation results, it is observed that the proposed BLDC drive topology is possible. For the Cuk converter supplied drive topology, only the simulation results are shown.

TABLE II

COST ANALYSIS OF THE CUK CONVERTER SUPPLIED CSI BLDC DRIVE IN FIG. 31

	Cuk converter drive		Conventional drive	
	Quantities	$	Quantities	$
IGBT	1	0.75	6	4.50
SCR	6	1.5	---	---
Inductor	2 (few mH)	2	1 (few mH)	1
Fast Recovery Diode	1	0.45	1	0.45
Rectifier	1	0.2	1	0.2
Heat Sink for IGBT's	1	1	7	3.5
Capacitor	1 (0.1 mF)	1	1 (about mF)	$4.9
Gate drive		4.00		$3.00
PCB, DSP, Op-amps etc.		4.85		$4.85
Total material cost		**$15.75**		**$22.40**
Cost reduction	**29.6 %**		**0 %**	

V. DESIGN OF HARDWARE

1. Overview of implementation

Since the simulation results were promising, the buck converter fed CSI BLDC drive has been implemented. Each block of the implementation is described and the relevant experimental results are presented. The hardware blocks that have been described are the motor, the Hall position sensor, the Capture Unit, the Analog-to-Digital converter, the Digital-to-Analog converter, the current sensors, the Current Source Inverter, the thyristor drivers, the dc link inductor and the buck converter.

2. Motor

An E-series Electro-Craft® E-3633 motor, manufactured by Reliance Electric is used for experimentation [20]. The continuous stall-torque of this motor is 12.9 kg·cm, the torque constant (K_T) is 2.3 kg·cm/A, implying that the maximum current that can be safely supplied to the motor is given by (5.1).

$$I_{\max} = \frac{T_{stall}}{K_T} \tag{5.1}$$

$$\text{or } I_{\max} = 5.4\,\text{A} \tag{5.2}$$

Although the neutral is not available, a waveform that is identical to the phase-to-neutral back-emfs except for the absence of third harmonics can be measured by creating a 'pseudo-neutral' (by connecting three resistors in the 'star-pattern'). The third harmonic is not present because of the absence of a 'true neutral' point. Hence, the back-emf which is measured between each of the phases and the 'pseudo-neutral' lacks the third harmonic and hence, it is not as flat as the true phase-to-neutral back-emf. However, the phase-to-neutral back-emf measurements with respect to the 'pseudo-neutral' give an approximate indication of the point where the back-emf starts rising as well as where it starts falling. This 'pseudo phase-to-neutral' voltage and the Hall position sensor outputs give us a clear

picture of the switching sequence of the thyristors that comprise the Current Source Inverter.

3. DSP processor

Instead of using an analog PI controller for the proposed drive, a digital controller was implemented on a TMS320F243 DSP processor from Texas Instruments [21]. Although the analog PI controller may have a greater bandwidth than a digital PI controller, it is subject to deviation due to the drifts in nominal values of its components. Another fact is that it is much more difficult to adapt an analog PI controller to changes in the system parameters, for example, replacement of the motor by another BLDC motor, and other factors. For a digital PI controller, all that needs to be done in order to adapt it to a new system is to change the parameters of the controller by reprogramming the DSP.

Although a traditional micro-controller/microprocessor has a CPU, the corresponding arithmetic and logic functions as well as some non-volatile memory on-board, many peripherals ICs and components have to be added in order that a suitable system for motor control is built. The TI family of DSPs for motor control has incorporated many functions that were previously performed by off-chip ICs and components by integrating various modules on the chip, thereby, greatly increasing the speed and reliability of the overall system.

TMS320F243 is a fixed-point DSP processor, meaning that the DSP does not have an inbuilt architecture for handling non-integer parts of decimal numbers. That is, the system designer has to interpret the non-integer parts by means of using scaled numbers. An added precaution when using fixed point processors is to protect against numerical overflows that may lead to errors, while at the same time, not to scale down each number so small that precision is lost. This is explained in greater detail in the section on current control and PI regulators.

The DSP board contains the following modules:

(1) 16 k of on-chip non-volatile memory (Flash)

(2) 544 words of dual access RAM

(3) 4 k of read-only memory

(4) Upto 32 k of external memory

(5) A collection of modules known as the Event Manager (EV)

(6) A PLL clock

(7) 10-bit Analog-to-Digital converter (ADC)

(8) Serial Communications Interface (SCI)

(9) Serial Peripheral Interface (SPI)

(10) Controller Area Network (CAN)

(11) Watchdog Timer, to bring the CPU to reset in case of a fault that causes either CPU disruption or the execution of an improper loop

(12) JTAG Port for communication to and from the computer through an emulator pod

Perhaps the collection of modules, collectively known as the Event Manager [22], is probably the most important feature that enhances the functionality of a motor control DSP and give it an advantage over the traditional microcontrollers. The Event Manager, as its name implies, is used to manage timing of the various events without the processor core having to do almost each of the tasks; leaving the processor free to perform more important tasks, thereby, speeding up the system. The Event Manager is commonly referred to as EV2 in the TMS320F243 user manuals. It consists of the following important units:

(1) Event Manager control registers and control logic

(2) General Purpose Timer (GPT1), a programmable 16-bit hardware timer that is connected to six PWM output channels

(3) General Purpose Timer 2 (GPT2), another programmable 16-bit hardware timer

(4) Capture Units that are used for detecting either rising or falling edges of pulse inputs

(5) Two compare outputs with programmable frequency and duty cycle D, corresponding to each General Purpose Timer.

(6) Quadrature Encoder Pulse (QEP) circuit for sensing the speed and position information from a rotary encoder.

(7) Space Vector PWM (SVPWM) unit

(8) Dead band generators for introducing a dead-band time in the switching of inverter legs in order to prevent cross-conduction faults.

4. Hall position sensors

As previously described, the triggering of thyristors is a function of the rotor field, and hence, a function of the rotor position. The combination of the Hall position sensor outputs is unique for an interval of 60° (electrical) as the rotor position changes. The sequence of these combinations is useful in deciding the direction of rotation. The rotor position is sensed by means of Hall position sensors that detect the position of either the main rotor field or an an equivalent field generated by a magnet ring on the rotor shaft. Three Hall position sensors are sufficient to uniquely determine the position of the rotor. The angular distance between each of the Hall position sensors is 120° (electrical). As per the datasheet of this motor (Electrocraft E-3633), there are four poles, implying that the Hall position sensors are placed at an angular distance of 60° (mechanical). The Hall position sensors, based on the Hall effect, output a voltage that is a function of the magnetic field direction. The output of this position sensor is of the open-collector type and requires an external pull-up resistor to interface the output to the Capture Units on the DSP. The output is TTL compatible, and therefore, either a high or a low, depending on the position of the rotor magnet field that is interacting with the Hall position sensor.

5. Capture Units

Capture Units [22] sense either a rising or a falling edge input, that is, they respond to the transitions of the input signal. There are three Capture pins, each sensing the change in position as a Hall position sensor output changes from either low-to-high or high-to-low. Either GPT1 or GPT2 can be chosen as the time base for operation of the Capture Unit. Capture 1 and Capture 2 form a pair and have to be always connected to the same time base, and Capture 3 may be connected to either the same time base or to the other remaining General Purpose Timer. In order for a Capture transition to be recorded as a valid input, after transition, the input signal must retain its state for at least two cycles of

the time base clock. This prevents spurious noise pulses to be recorded as valid transitions. Whenever the Capture function is chosen, the QEP function is disabled.

A Capture Unit is controlled by the following registers:

(1) 16-bit Capture control register (CAPCON)

(2) 16-bit Capture status register (CAPFIFO)

(3) 2-level-deep FIFO stack for each Capture pin

If the transition of Hall position sensors is not sharp, the Capture Units may not sense the pulse. Although the Capture inputs have inbuilt Schmitt Triggers, as a matter of practice, it is safer to put a CMOS Schmitt Trigger before feeding the output of the Hall position sensor to the Capture Units.

The CAPFIFO register contains the description of the state of the Capture Unit. In EV2, the EV2 Interrupt Mask Register C (EVIMRC) has to be configured to enable the CPU core to receive the Capture interrupts. The EV2 Flag Register C (EVIFRC) contains the description of the interrupt generation in a corresponding bit in that register. If a Capture interrupt is received by the CPU, the corresponding peripheral flag in EVIFRC is set. If the interrupt level corresponding to Capture interrupt is enabled (level 4), then the CPU recognizes the Capture interrupt and issues an interrupt acknowledge, and the code in the interrupt corresponding to the Capture Unit (interrupt 4) is executed. It is worth noting that the interrupt flag in EVIFRC has to be cleared by an explicit statement in the Interrupt Service Routine, since for EV2 interrupts, clearing of peripheral flags is not automatic.

6. Analog-to-Digital converter

Many of the real-world input signals are in the analog domain whereas the CPU does all the processing in the digital domain. In order that the CPU get the analog domain signals for processing, it is essential to translate them into a format that makes sense to the CPU. This is achieved by using an Analog-to-Digital converter (ADC) that does the required translation [22]. The principle behind the ADC used in this DSP is the Successive Approximation Principle, based on the well-known Binary Sorting Algorithm. Although it

appears as if there are two ADCs in the DSP, in fact, the control logic makes it appear as if there are two ADC converters, named as pseudo-ADC#1 and pseudo-ADC#2.

A bank of switched capacitors provides the sample-and-hold function. For accurate conversion, the reference voltages to the ADC, namely VREFHI (the high reference voltage) and VREFLO (the low reference voltage) have to be precise. In the implementation of the proposed system, VREFHI has been set to 5 V and VREFLO to 0 V.

Depending on the conversion time, the ADC clock can be prescaled to certain frequencies that are multiples of the CPU clock. The ADC can be set in either the single conversion mode or the continuous conversion mode. The ADC conversion can be started by an external signal transition (only a rising edge has any effect) or by software. Certain EV2 events, for example, a GPT1 period completion by setting of the flag corresponding to T1PER starts the conversion process. The ADC Start-of-Conversion (ADCSOC) bit has to be set for starting the conversion either by an external signal or by EV2 events, and after the corresponding ADC service routine, the ADC Interrupt Flag (ADCINTFLAG) has to be cleared explicitly.

7. Digital-to-Analog converter

It is pertinent to note that the Digital-to-Analog converter (DAC) is not built in the TMS320F243 DSP, but it is added external to the DSP and is on the EVM development board [23]. It is a 4-channel, 12-bit, double-buffered DAC from EXAR Corporation. Hence this DAC can output 4096 distinct values in the range 0 – 5 V. Alternatively, it implies that the DAC can increment in steps of 0.001220703125 V.

8. Current sensing

Current sensing is carried out by means of a Hall effect current transducer for isolating the sensing and the control circuit from the power circuit, thereby preventing any damage. The transducer used is “LTS 6-NP” from LEM [24]. The output of this transducer is a voltage in the range from 2.5 V – 4.5 V for the positive direction of current, increasing as the current magnitude in the positive direction increases and 2.5 V – 0.5 V for the negative direction of current, decreasing as the current magnitude increases in the negative

direction. The power supply required for the current transducer is given from a 5 V linear regulated voltage source. Since the range of output voltages is safely in the range that can be tolerated by the DSP ADC inputs, this current sensor can be directly interfaced to the TMS320F243 ADC inputs without any need for signal conditioning, although a lowpass filter and output voltage limitation may be added for supplying the output to a 3.3 V ADC. For maximum sensitivity, three turns of the current carrying wire link this transducer, and for three turns the maximum current that can possibly be sensed is 6.4 A. The rated stall-current of the BLDC that is used is 5.6 A, hence, three turns can be used safely without impairing sensing in the expected current range.

9. Current Source Inverter

The CSI is a practical implementation of a three-phase ac current source. Since line commutation is used, the cheaper rectifier grade thyristors can be used instead of the expensive inverter grade thyristors. The BLDC motor back-emf takes care of commutation, and hence there is no need of extra commutation circuits. There are 3P switchings of the thyristors per revolution, implying that the switching frequency (at rated speed) is not more than 120 Hz. Because of these features, the switching losses are negligible and the need for heatsinks is eliminated.

The thyristors used, MCR-310 [25], manufactured are of the ultrasensitive type, that is, the gate current requirement for triggering is extremely low, and approximately 250μA of current applied to the gate of this thyristor is sufficient to switch on these thyristors. Although a TMS320F243DSP can provide the necessary current to trigger on these thyristors, thyristor driver circuits have been used to provide isolation as well as buffering.

The CSI can be considered as a controlled rectifier with a delay angle (α) of 165° and trapezoidal three-phase input supply. In this mode, the rectified back-emf is shown in Fig. 40.

10. Thyristor driver

The low-power DSP may not have sufficient current output to drive the thyristors of the CSI. Moreover, even if the lower thyristors were driven by the DSP through a buffer, the DSP on the signal-side would not be isolated from the power-side of the drive. Therefore, either optocouplers (optically isolated gate drivers) or pulse transformers are used to achieve isolation between the power-side and the signal-side. Pulse transformers are a type of transformers that can handle a high frequency input with a dc bias. The pulse transformers should have sufficient time between the high level interval of the signal and the next high level interval of the signal to 'reset', that is get rid of the saturation induced by a unidirectional supply. If the pulse transformers do not have sufficient time to 'reset', saturation may cause the output of the pulse transformers to have insufficient magnitude to trigger the thyristors. As compared to an optically isolated driver, pulse transformers have the advantage of not requiring isolated power supply for each thyristor driver, but require a train of pulses as the input signal for an interval the corresponding thyristor is to be switched on. The pulse tranformer output current should be sufficient to trigger the thyristors to a conducting state. At the output of each pulse transformer is a circuit consisting of diodes and resistors, and it supplies unidirectional pulses to the thyristors. This circuit aids in resetting the flux buildup in the pulse transformers.

A commercially available thyristor firing board, FCOAUX60 from ENERPRO [26] is used to drive the thyristors and consists of six pulse transformers with isolated outputs. The input signal for each pulse tranformer is a PWM of 50% duty cycle, having a high of 10 V and a low of 0 V, in the frequency range 18 kHz – 25 kHz, and 20 kHz is the frequency used in this implemenation. It requires a 30 V input power supply that has the same ground as the DSP. This eliminates the need for six isolated power supplies, and the cost of driving the thyristors is greatly reduced. The driver IC (ULN2004A) that performs the task of driving is the main component of the thyristor driver. As a matter of precaution, the inputs to the thyristor driver must be initialized to zero in order to protect the driver IC, else the flow of a dc current may cause the pulse transformers to saturate for long periods.

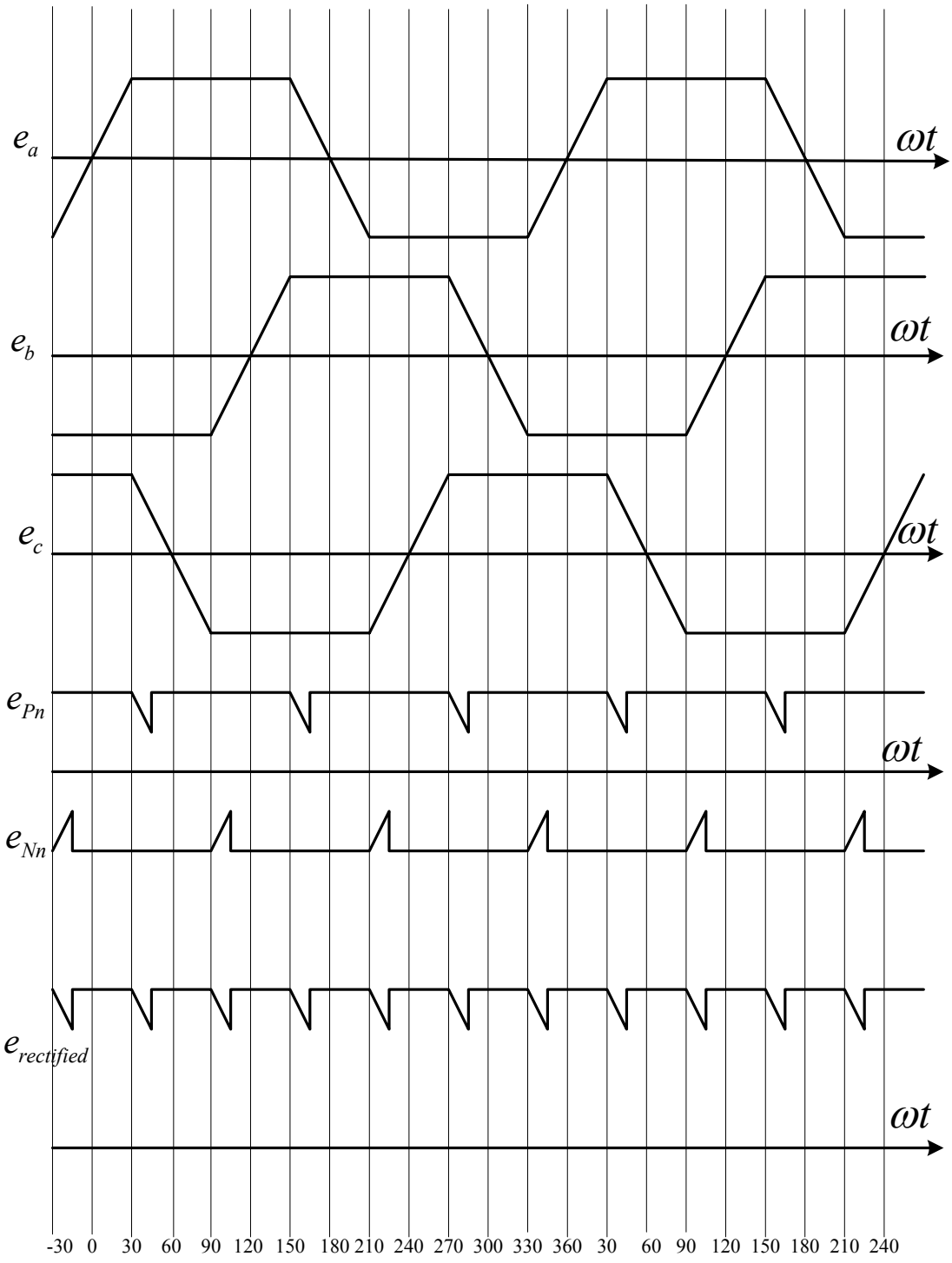

Fig. 40. Back-emf with 15° triggering lead angle to CSI

ULN2004A is a high-voltage, high-current transistor Darlington array that buffers the input signals and is capable of supplying a peak current of upto 500 mA. The 2:1 pulse transformer further doubles the current capacity by a factor of two, and this arrangement is able to trigger the thyristors to turn on. The upper and lower thyristors in each of the inverter legs are connected as a pair to the supply since at a given instant, only one of the thyristors in an inverter leg is turned on, thereby optimizing the energy utilization in the thyristor driver. Also, at any given instant, only two out of the six thyristors are triggered, hence the power supply to the thyristor gate driver may be rated to supply a maximum of two thyristor gates.

Since the DSP cannot supply the input signal to the thyristor drivers at the necessary voltage level, non-inverting Schmitt Triggers [27] are used to boost the output signal from the DSP to 10 V. This is achieved by means of a simple circuit (Fig. 41) having the output of each op-amp comparator clamped to 10 V. From cost as well as speed considerations, LM 339 op-amp comparator is used for this signal level translation. The lower threshold (V_L) of this Schmitt Trigger is kept at a potential that is slightly higher than the V_{OL} (0 – 5 V logic) and the upper threshold (V_H) is slightly lower than V_{IH} (0 – 5 V logic) for a faithful translation of the voltage levels. The reference voltage for the comparator is set at the midpoint of V_{OL} and V_{IH}. The hysteresis width (V_H) is adjusted to be equal to the difference between V_{IH} and V_{OL}. The values of the resistors are calculated as follows, given by (5.3) – (5.5).

$$V_{ref} = \frac{V_{CC} R_1}{R_{ref} + R_1} \tag{5.3}$$

$$R_2 = \frac{R_1 R_{ref}}{R_1 + R_{ref}} \tag{5.4}$$

$$V_H = \frac{R_2 (V_{out(\max)} - V_{out(\min)})}{R_2 + R_3} \tag{5.5}$$

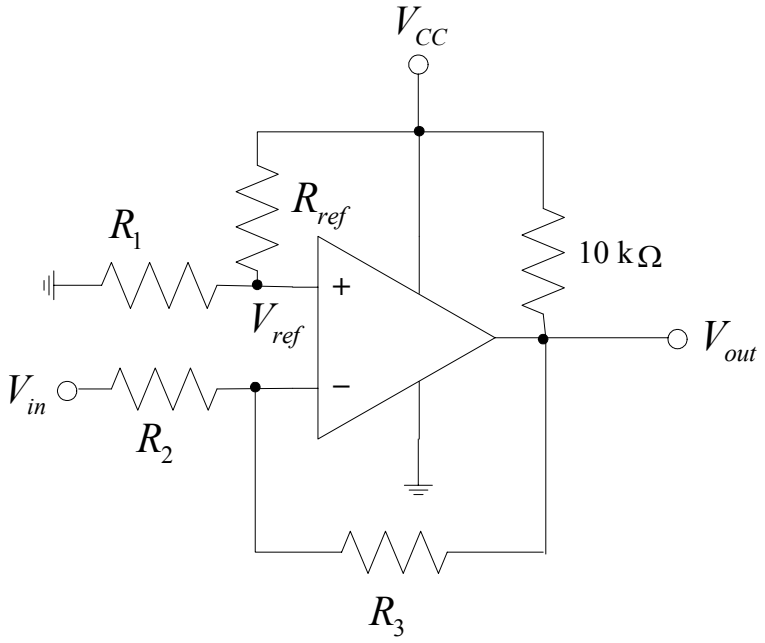

Fig. 41. LM 339 based non-inverting Schmitt Trigger

11. Inductor choice and design

Since, in practice there does not exist a true ‘current source’ to supply the inverter, an inductor placed in the dc input maintains the current supplied to the load approximately constant. Bigger the inductor, the more ideal the current source, but it also implies a sluggish dynamic response, since the current flowing through a large inductor cannot change instantaneously in response to the reference current. The difference in the voltages across the inductor should not saturate the inductor for proper operation of the drive. Since the controlled voltage source (from buck converter) can track even the back-emf voltage ripple of frequency six times the fundamental, we can use a small value of the inductance. The current ripple that can be tolerated decides the value of the inductor.

An inductor with a dc bias needs to be designed to take into account the constant dc current that is flowing through the inductor. At high frequencies, either ferrite [28] or iron-

powder cores [29] are used in the design of these inductors. The advantges and disadvantages of a ferrite and iron-powder cores are considered in Table III.

TABLE III
COMPARISON OF FERRITE AND IRON-POWDER CORE INDUCTORS

Comparison criterion	Ferrite	Iron-Powder
Magnetizing current	Low	High
Inductance per turn	High	Low
Number of turns	Low	High
Resistance	Low	High
Saturation	Less A-turns required	More A-turns required
Airgap required for inductors with dc bias	Yes	No

For the inductor design, the following conditions need to be satisfied:

(1) It should not saturate, even at the maximum current for which it is designed

(2) Losses should be minimal

If the above conditions are satisfied by a particular size of the core, a core of lower size is selected to test if the above conditions are satisfied. The lowest size of the core that satisfies the above conditions is usually selected. Freely available programs to design inductors, either from Ferroxcube® [28] or from Micrometals® [29] are used. A sample program to design the inductors, written in MATLAB® is listed in appendix A. While using this program, in order to avoid saturation in the inductor core, care must be taken to

ensure that the required number of turns for a given inductor do not exceed the maximum possible turns.

In order to minimize the resistance and hence the resistive losses, toroid ferrite cores were selected and stacked in order to increase the inductance per turn. The core used was 'FERRITKERN / B64290A 711X830' from EPCOS Inc. [30]. Litz wire was used to reduce the skin effect on the windings of the inductor [31].

12. Buck converter

A buck converter is made using a single leg of an inverter and an inductor at the output. The transistor in the upper part of the inverter leg is used as the switch of the buck converter and the anti-parallel diode of the lower transistor is the diode of the buck converter. The buck converter, as explained previously, has a R-L and back-emf load. This load and the switching frequency determines the value of the inductor.

13. Constant torque load

A constant torque load can be achieved by using a hysteresis magnetic brake (Model HB-210-3) from Magtrol®. The applied torque is constant irrespective of the shaft speed and the ratio of output torque to the input voltage is 0.1236 N·m per volt. The maximum torque load that can be applied is 1.483 N·m at an input voltage of 12 V.

14. Noise problems and shielding

Noise problems associated with either the switching of the thyristors or other environmental factors may create glitches in the correct reading of Hall position sensors. This may cause false triggering and loss of synchronization. Hence, a copper metal enclosure is put around the Hall position sensor input and output cables and such an enclosure is connected to earth to provide a shielding.

VI. SOFTWARE DEVELOPMENT

1. Overview of the system and software development process

This chapter describes the development of the necessary software required for the proposed buck-fed CSI BLDC drive. C language is used to develop the necessary code for the TMS320F243 EVM. The TMS320F243 EVM manufactured by Spectrum Digital Inc., has a TMS320F243 DSP chip from TI at its heart. In addition, the EVM contains additional components like external memory, the Digital-to-Analog converter (DAC) for ease of testing and development, a XDS 510 PP emulator pod for interfacing the PC to the EVM, making it possible to develop code using a PC based environment. The compiler used is Code Composer Version 4.12 [32]. Real-Time monitor, a utility from TI is added to enable online tuning of various control parameters.

Since it is a fixed point DSP, the only way to handle fractional and non-integral quantities is to scale them to some range and then work with the scaled quantities as if they were integers and then correctly interpret the obtained results (in the integer formats). Q formats are used to represent non-integer numbers.

The program is divided into two categories, namely the ‘main’ program and its various functions. The various functions are nothing but various interrupt service routines, each having its designated priority. The Real-Time monitor is, in fact, a lowest priority interrupt that keeps track of the global variables during the spare time between interrupt request processing, and it displays these variables in a watch window on the computer screen. The complete flowcharts are described in this section.

The following software modules have been described:

(1) Main module

(2) Position detection and speed calculation

(3) Digital-to-Analog conversion

(4) Hysteresis current controller

(5) PI-speed regulator

2. Main module

It is equivalent to a ‘main’ program in the ANSI C standard, except that when the processor has come to the end of the main program, it is waiting in an infinite loop for any interrupt to be generated, and as soon as it is generated, the corresponding Interrupt Service Routine (ISR) is called. As soon as the execution of the code is started, the main module (Fig. 42) does the various initializations of different registers, unmasks the required interrupts and calls the Real-Time monitor. GPT1 is configured to generate a 20 kHz PWM that samples the current using the ADC.

This module also detects the position of the rotor when it is stationary and then, depending on the direction of rotation, the appropriate CSI thyristors are triggered to generate an initial movement of the rotor (Table IV). This leads to the Capture interrupt being generated by the Hall position sensors and then the motor tries to attain the reference speed.

TABLE IV

SWITCHING TABLE FOR SCRS AT START-UP

A (C4)	B (C3)	C (C2)	PCDATDIR	Switching states (at startup)
1	0	1	0x0014	T4 and T5
1	0	0	0x0010	T1 and T4
1	1	0	0x0018	T1 and T6
0	1	0	0x0008	T3 andT6
0	1	1	0x000C	T2 and T3
0	0	1	0x0004	T2 and T5

3. Capture interrupt module (priority level – 4)

This module is called whenever a Hall position sensor output has a transition. This occurs after every 60° (electrical) interval and preparations are made to load the appropriate triggering for the next switching state, with a delay of at least 30° with respect to the

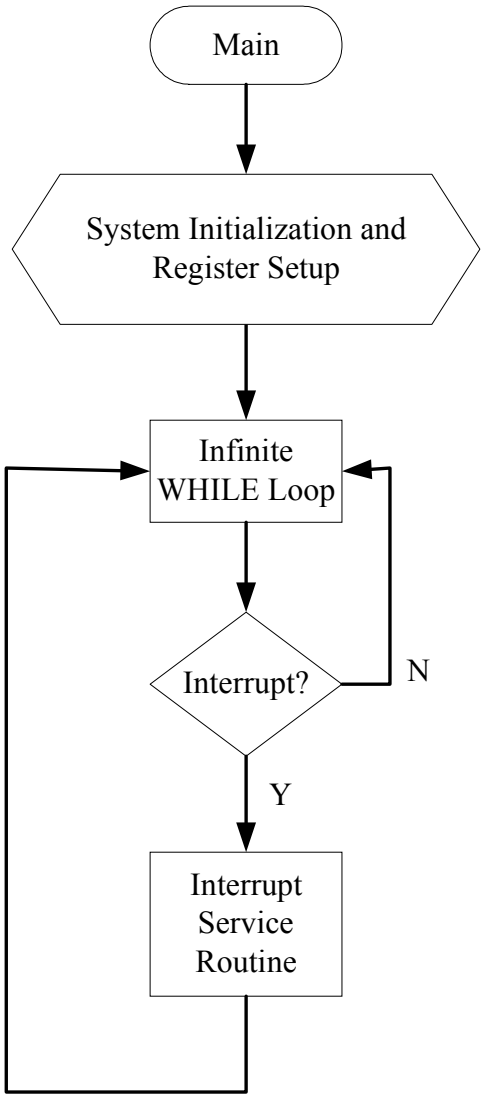

Fig. 42. Structure of main program

current interval (that is a leading angle of less than 30° with respect to the next switching state). The most critical thing in this module is to calculate the time between the previous and the current Capture interrupt, and it is obtained by means of the count in the T2CNT register of GPT2. After obtaining this count, the timer GPT2 is reset to count till the next Capture interrupt is generated. The count that is obtained corresponds to 60°, and hence, in order to trigger the thyristors corresponding to the next switching state, with a 15° advance, a delay of 45° is generated. It is done by loading a count that is $\frac{45^{\circ}}{60^{\circ}}$ times the obtained T2CNT into the T2CMPR register to generate a T2CMPR interrupt (as soon as T2CNT corresponds to a delay of 45°). But the timer GPT2 keeps on counting till the next Capture interval arrives.

Just before exiting this interrupt, the peripheral interrupt flags in the register EVIFRC are cleared and the interrupts are once again enabled to allow the next interrupts of this type to be generated. This interrupt is the most important one and has a relatively high priority because even the loss of a single Capture interrupt due to the processor being busy with other interrupts can cause the system to lose synchronization, thus bringing the motor to a halt with the CSI switches in an unpredictable/locked-out state. Fig. 43 shows the functioning of the Capture interrupt module.

4. Angle advance thyristor triggering interrupt (priority level – 3)

As soon as this interrupt is generated, it implies that next switching state would be reached after an electrical angle of 15°. Since a leading angle of 15° is sufficient for the thyristors to commutate, the thyristors in the next switching state (corresponding to Table V) are switched on. The ACTR register is then loaded with a value that corresponds to the required switching state. The PWM outputs corresponding to the thyristors to be turned-on are made ‘active high’ and the other PWM outputs are forced to zero. Since very little processing is done in this ISR (Fig. 44), there is plenty of time till the next Capture interrupt arrives; speed calculation and its normalization is done in this interval. The PI parameters, if changed during the execution of the program, are also updated in this ISR.

$$Speed_{measured} = \frac{1}{Time\_Period} \tag{6.1}$$

As is the practice before exiting the interrupt, the peripheral interrupt flag corresponding to T2CMPR interrupt in EVIFRB is cleared and all the interrupts are re-enabled to allow the next interrupts of this type to be generated.

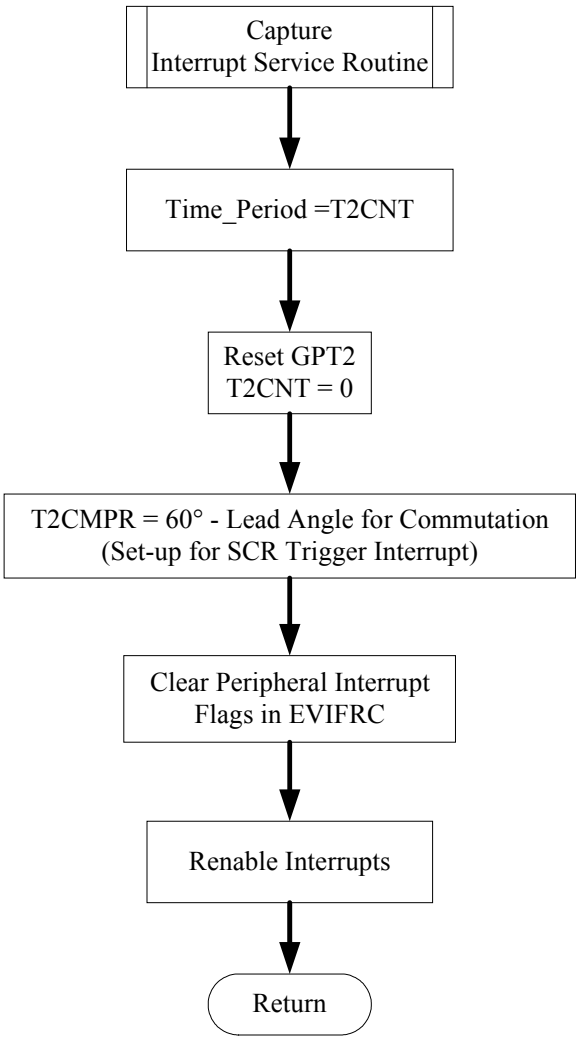

Fig. 43. Capture ISR

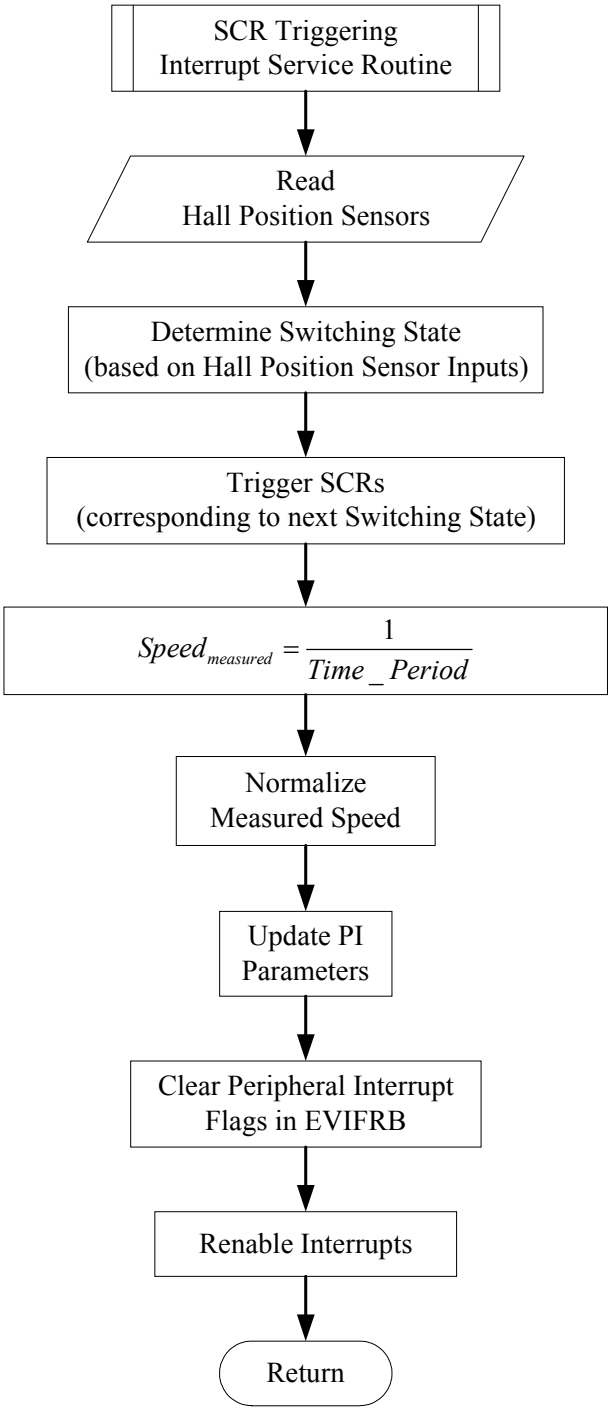

Fig. 44. SCR triggering ISR

TABLE V

SWITCHING TABLE FOR SCRS IN SCR TRIGGERING INTERRUPT

A (C4)	B (C3)	C (C2)	PCDATDIR	Switching state (after startup)
1	0	1	0x0014	T1 and T4
1	0	0	0x0010	T1 and T6
1	1	0	0x0018	T3 andT6
0	1	0	0x0008	T2 and T3
0	1	1	0x000C	T2 and T5
0	0	1	0x0004	T4 and T5

5. Current sensing and current control interrupt (priority level – 6)

This interrupt is generated whenever the ADC completes its conversion. The ADC Start-of-Conversion (SOC) is triggered by the setting of T1PER (GPT1 Period) flag, and as soon as the ADC completes a conversion, the ADCINTFLAG is set and the ADCINT6 ISR is called. Since the frequency of GPT1 is 20 kHz, the current will be sampled at approximately 20 kHz. In order that the ADC interrupt not interfere with the Capture interrupt, instead of choosing the highest interrupt priority level, the ADC interrupt is set to the lowest priority (interrupt priority level 6). The ADC channel 0 (ADCIN0) is connected to the output of the dc link current sensor.

The PI controller is called in this ISR and based on the measured speed, the reference speed and the PI parameters, the reference current command is generated. There is a counter loop that calls the speed PI regulator once every 10 or 20 ADC interrupts since the speed change is not going to be at the same rate as the variations in the current.

The current control is implemented by using a hysteresis block that keeps the measured current in a permitted band around the reference current. If the measured current is less

than the reference current minus the hysteresis band, the chopper (transistor of the buck converter) is switched on to permit more current to flow. If the measured current is more than the reference current plus the hysteresis band, the chopper transistor is switched off. Although the frequency of switching is not fixed, the maximum switching frequency of the chopper is equal to the maximum frequency of this ISR, that is, approximately 20 kHz.

Before the ISR is exited, the ADCINTFLAG is cleared and all the interrupts are re-enabled to allow the future ADC interrupts to be generated. Fig. 45 illustrates the functioning of the ADC ISR.

6. Real-Time monitor interrupt (priority level – 7)

This is the interrupt that monitors global variables and displays them in a watch window on the screen. This interrupt can refresh variables at a maximum rate of 10 Hz.

7. PI controller

The equation of a PI controller [33, 34] illustrated in Fig. 46 is given by (6.2).

$$I_k^{reference} = K_{pi} e_k + K_i e_k + \sum_{n=0}^{k-1} e_n \tag{6.2}$$

where

$I_k^{reference}$ = reference current at the k^{th} sampling instant

K_{pi} = proportional multiplier term

K_i = integral multiplier term

e_k = speed error at the k^{th} sampling instant

This structure may saturate and cause overflow, and this may lead to enormous errors, especially in fixed point implementation. In order that this PI regulator does not ‘wind-up’, an ‘anti-windup’ structure of a PI controller [17] is implemented such that it prevents the

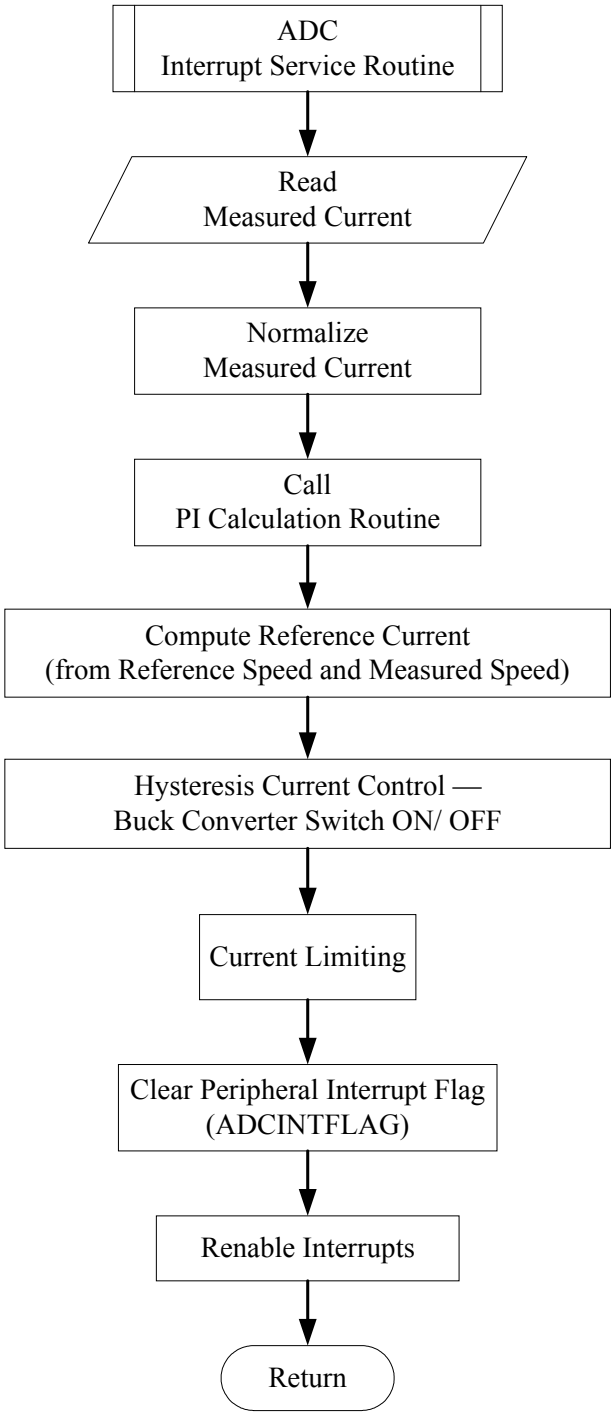

Fig. 45. ADC ISR

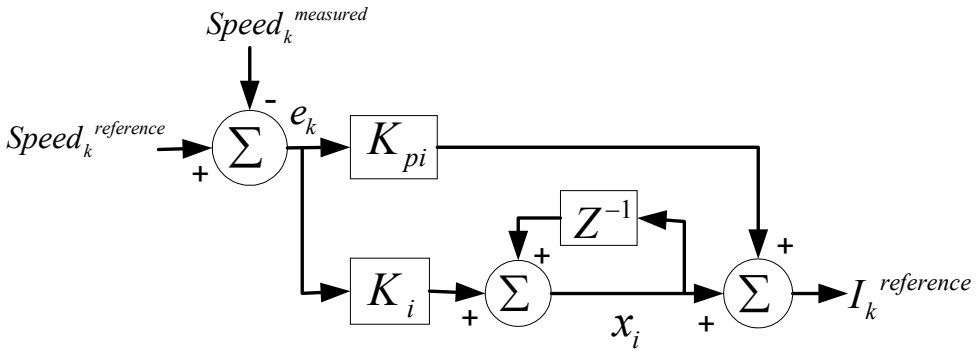

Fig. 46. Classical PI regulator

reference current from attaining extreme values. As per (6.3) – (6.9), the required regulator is obtained [35].

$$e_k = Speed_k^{reference} - Speed_k^{measured} \tag{6.3}$$

$$I_k^{reference} = x_i + K_{pi} e_k \tag{6.4}$$

$$I_k^{reference\_antiwindup} = I_k^{reference} \tag{6.5}$$

If $I_k^{reference} > I_{\min}^{reference}$, then $I_k^{reference\_antiwindup} = I_{\max}^{reference}$ (6.6)

If $I_k^{reference} < I_{\max}^{reference}$, then $I_k^{reference\_antiwindup} = I_{\min}^{reference}$ (6.7)

$$e_k^{antiwindup} = I_k^{reference\_antiwindup} - I_k^{reference} \tag{6.8}$$

$$x_i = x_{i-1} + K_i e_k + K_{cor} e_k^{antiwindup} \tag{6.9}$$

An anti-windup speed PI regulator is illustrated in Fig. 47.

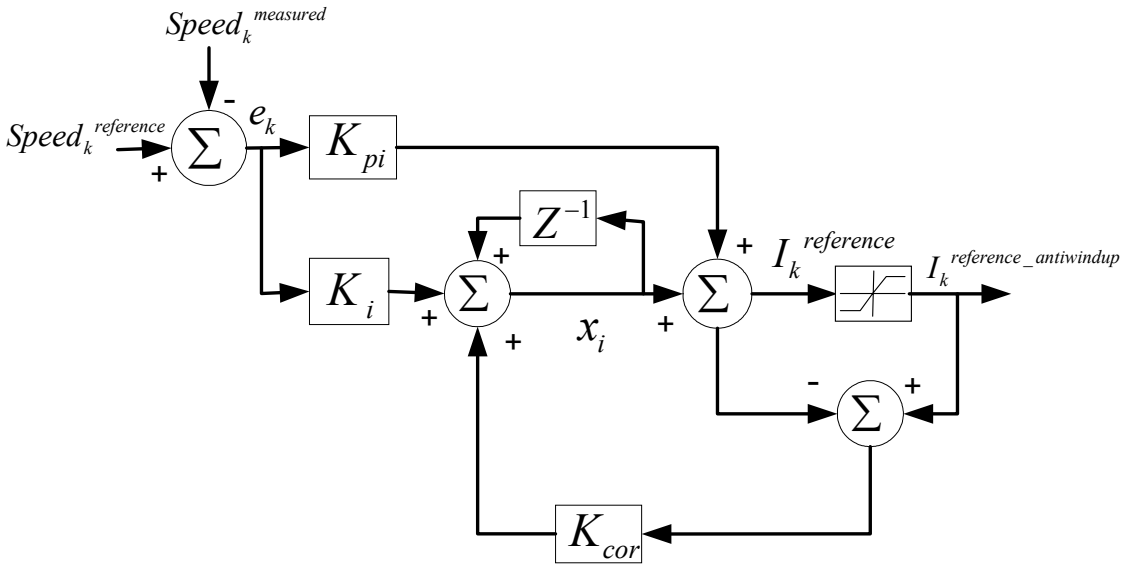

Fig. 47. PI regulator with anti-windup

VII. RESULTS AND CONCLUSIONS

In this section, the individual blocks that constitute the motor drive have been tested and the measurements thus obtained are interpreted. After putting them together, the drive has been tested for proper performance. Proportional control has been implemented for speed regulation, therefore, there is a steady state error in the measured speed and the reference speed. PI control is in the process of being implemented. An example of implementation using VSI is in [36].

1. Testing of thyristor driver modules

An input PWM of 20 kHz, 50% duty cycle, and a magnitude of 10 V was applied to the inputs of the thyristor driver and the desired output was observed. Under no load, the output of the driver was an amplified replica of the input PWM (Fig. 48), with a high of 15 V. Although the voltage output dropped when a SCR, similar to the one used to construct the inverter, was driven using this module, the output current provided was sufficient to switch on that SCR. The input to the thyristor driver unit must be a buffered output of the DSP outputs, and this has been achieved using Schmitt Triggers. Referring to Fig. 49, V_1Neutr, V_2Neutr and V_3Neutr are back-emfs of the motor phases, Hall_A, Hall_B and Hall_C are the outputs of the Hall position sensors and Thy1Gate, Thy2Gate, Thy3Gate, Thy4Gate, Thy5Gate and Thy6Gate, respectively, are the triggering signals applied to the gates of thyristors 1–6. It is observed that the phase-to-neutral voltages, measured with respect to each of the phases and the 'pseudo-neutral' are not flat because of the loss of the third harmonic that is common to all the three phases.

2. Testing of switching logic

The switching logic has been tested for anti-clockwise direction of rotation (when seen from the motor face having the longer output shaft). The switching has been obtained from switching tables in the previous section. The results of the inputs applied to the thyristor gates are shown in Fig. 49. Please note that the switching signals applied to the thyristor gates is a solid dark block due to the fact that it consists of a PWM pattern. In order to

protect the drive while testing the switching logic, the switching signals applied to the upper and lower SCRs of an inverter leg were reversed, the BLDC motor was rotated using an external power source (a dc motor) and it was observed that the CSI behaved like a controlled rectifier.

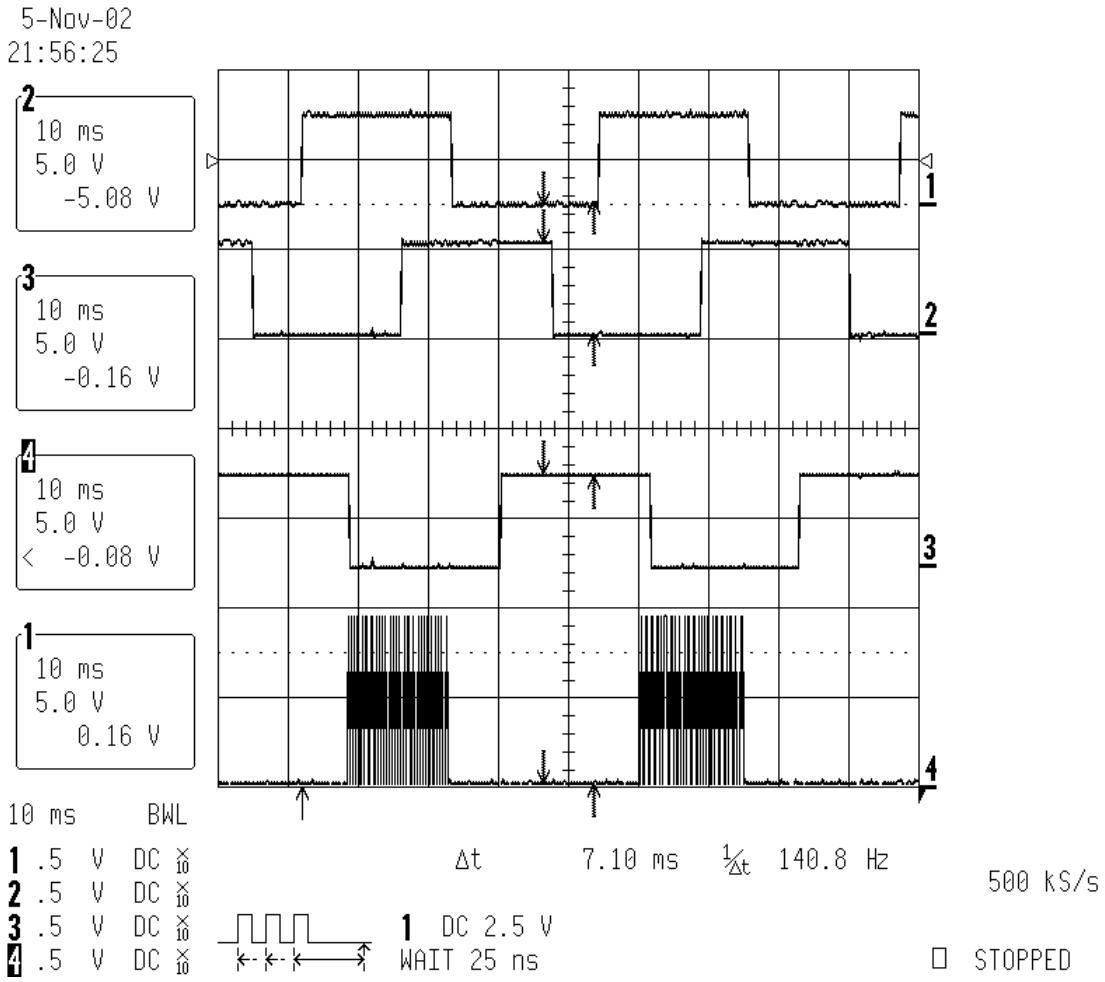

Fig. 48. Gate triggering to thyristor 1 and Hall position sensors

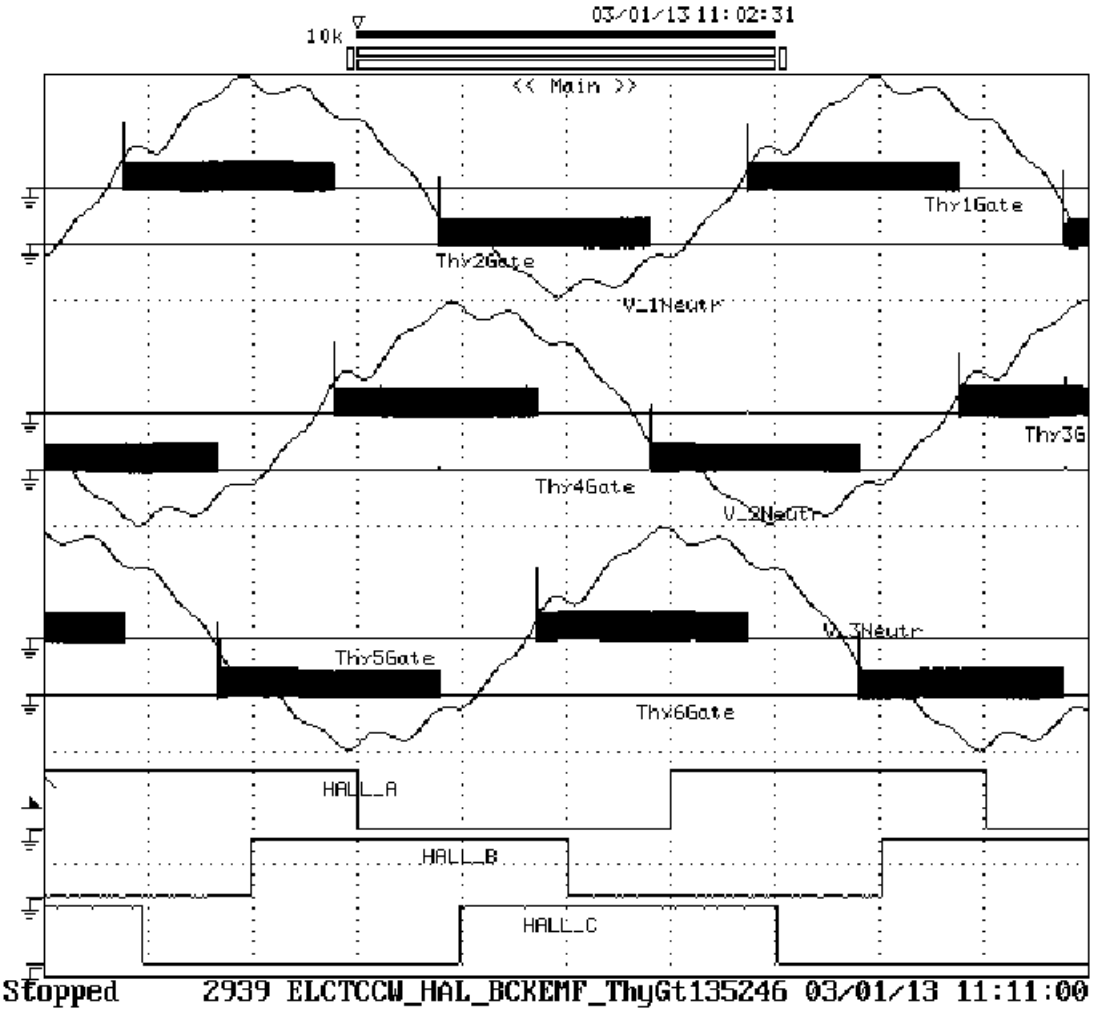

Fig. 49. Observed Hall sensors, back-emfs and thyristor triggering

Fig. 50 shows the rectified back-emf of the BLDC motor. The phase advance leads to a voltage ripple as is observed. The attenuation in the probe reduced the magnitude of the rectified back-emf. It is observed that the measurements agree closely with the output obtained from simulation and theoretical drawings.

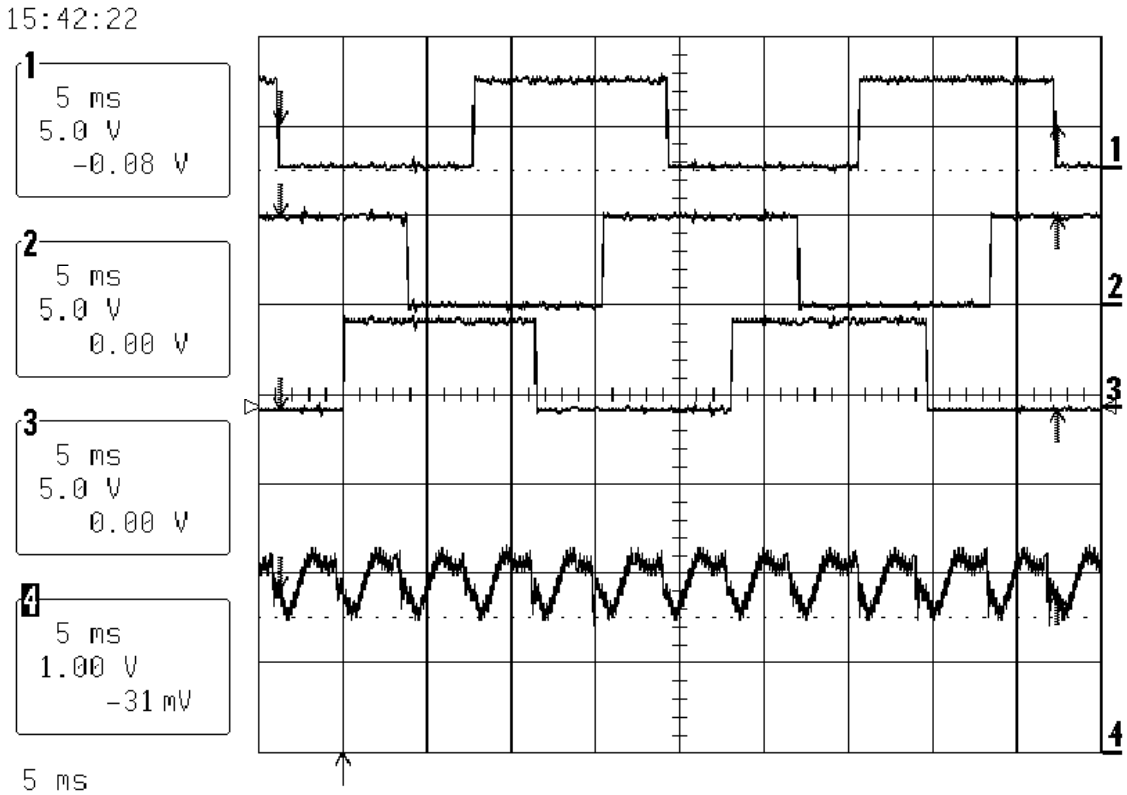

Fig. 50. CSI in the rectifier mode and dc output (rectified back-emfs)

3. Current sensing

In order to test this system, an input current of known magnitude is fed through the current sensor and the reading is then output to the DAC on the EVM board. The scaling constant, as expressed in the current sensor data sheet is confirmed and depending on the range, the number of turns through the current sensor are fixed. The following equation gives the output voltage of the current sensor when a current of I amps flows through the current sensor having three turns of the current carrying wire. To predict the output voltage of the current sensor V_{out}, expression (7.1) is used [24].

$$\frac{V_{out} - V_{out\_zero\_current}}{I_{measured}} = \frac{3.125 - 2.5}{I_{PN}} \tag{7.1}$$

The reading in the ADCFIFO register for a 10 bit ADC, shown in Table VI is given by

$$\text{ADCFIFO\_Register\_value} = (2^{10} - 1)(2.5 + I(0.3125)) \tag{7.2}$$

As the input current increases, the saturation effects in the current sensor take over and the error increases. The error is upto 5% when the measured current sensor voltage is read from the ADC and output to the DAC. In order to convert it into Q15 format in the current range 0–6.4 A, the the value corresponding to the zero current reading is subtracted from the value in the ADCFIFO register obtained from the current measurement. The resultant is multiplied by 0x0050 for further processing in the Q15 format.

TABLE VI

CURRENT SENSOR MEASUREMENTS

Input current	Predicted ADCFIFO register value	Measured ADCFIFO register value
1 A	0x023F	0x023A
2 A	0x027F	0x0270
5 A	0x033F	0x0330
5.3 A	0x0352	0x0341

4. Buck converter

The buck converter is tested with a series of R-L loads in order to test for current controlled mode of operation. At a switching frequency of 20 kHz, the current control mode with a passive R-L load is shown in Fig. 51, and the reference current is 1.2 A.

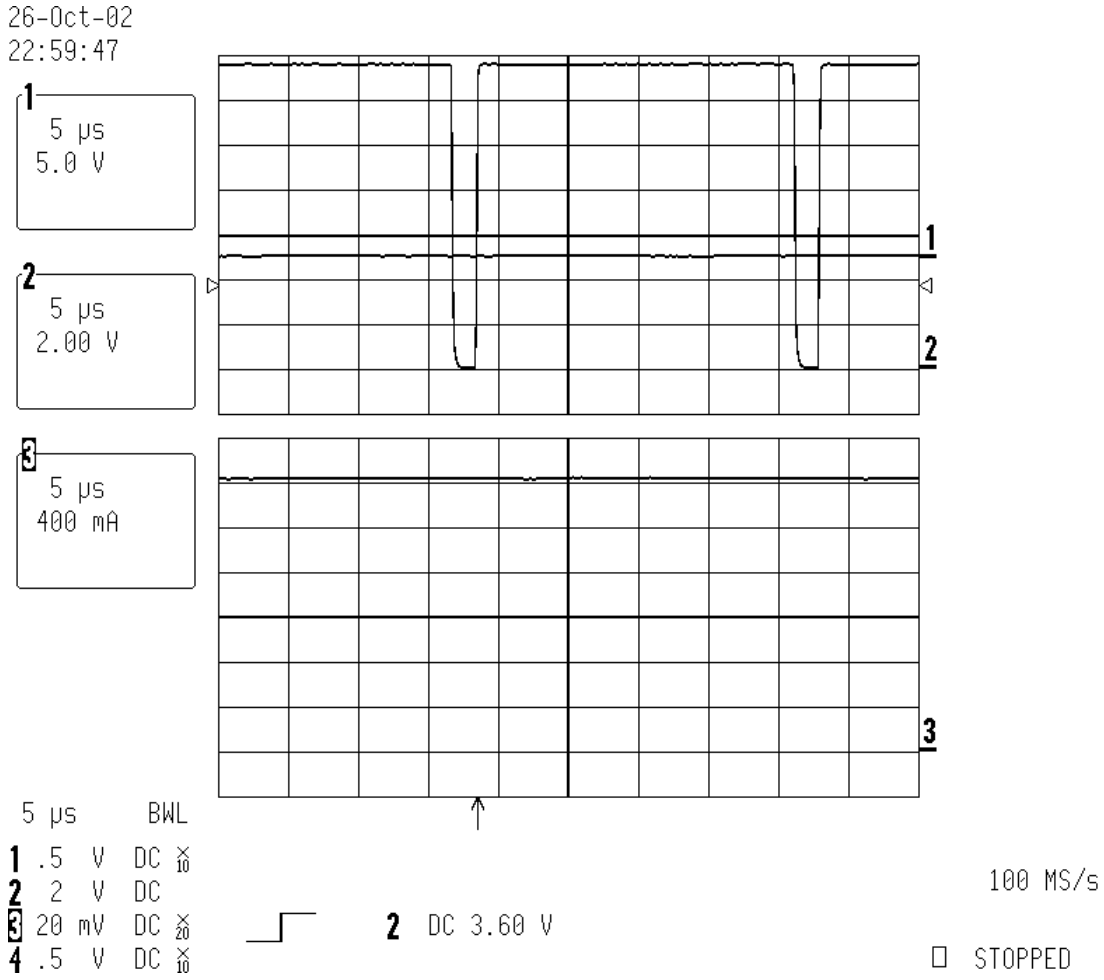

Fig. 51. Buck converter with passive load

5. Interpreting the calculated speed of the motor

The main aim is to correspond the calculated speed to the actual speed in rpm. The BLDC is driven by a dc motor in order to maintain the speed as constant as possible. The speed calculated in the SCR triggering interrupt is scaled and output to a DAC (Table VII).

TABLE VII

ACTUAL, MEASURED, CALCULATED AND DSP-CALCULATED SPEEDS

Speed (rpm) tachometer	Measured DAC voltage corresponding to speed	Calculated speed (as a voltage output to DAC)	Speed in register
0	0.05	0.0000	0x0000
140.844	0.234	0.22830	0x000B
185.04	0.305	0.29994	0x000F
277.62	0.451	0.45000	0x0017
336.9	0.551	0.54610	0x001B
428.58	0.695	0.69471	0x0023
515.04	0.836	0.83486	0x002A
612.24	0.991	0.99241	0x0032
702.6	1.142	1.13888	0x003A
797.34	1.295	1.29245	0x0042
886.92	1.443	1.43766	0x0049
905.64	1.468	Used as reference value for other calculations	0x004B
1800	Beyond range of dc motor	2.9177	0x0095

6. Hysteresis current loop

This is the innermost loop of the system. The buck converter, the CSI and the BLDC are connected to test the preliminary working of the system. However, no speed control is possible at this stage. Although a PI current control is ideal, due to the fact that all the available on-chip timers are assigned to higher priority tasks, no timer can be spared for the PWM driving the buck converter switch, and a hysteresis current control has to be used. The dc link current is shown in Fig. 52 and the one of the motor phase currents is shown in Fig. 53. Since hysteresis current control is used, the switching frequency is arbitrary and the inductor has to be designed for the lowest switching frequency of approximately 1 kHz.

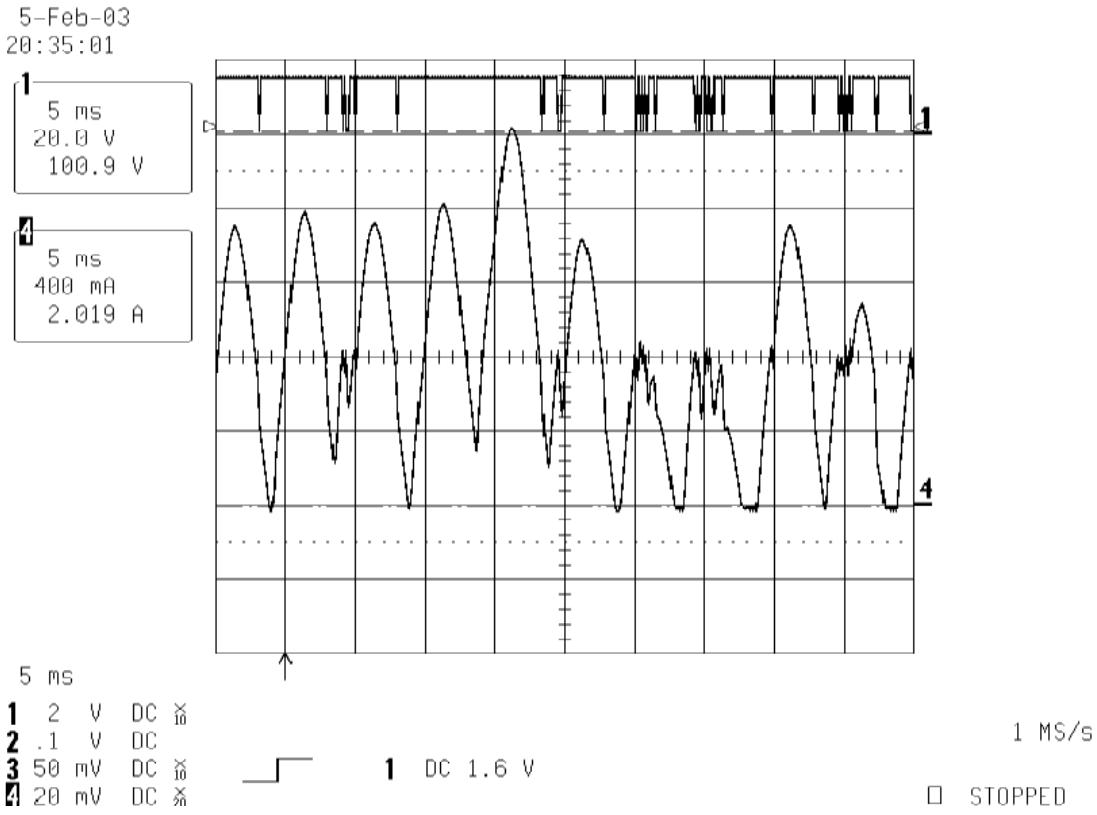

Fig. 52. Hysteresis current control — dc link current

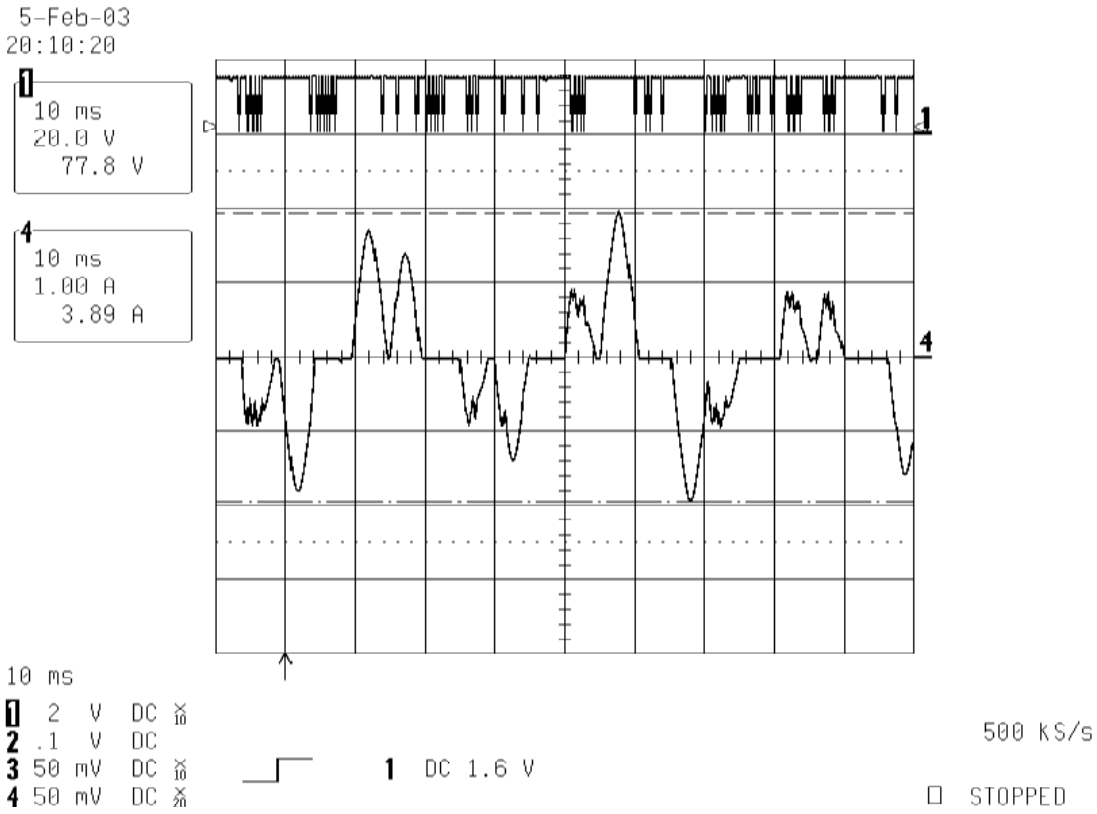

Fig. 53. Hysteresis current control — phase current

7. Speed control

Although proportional speed control (the one that was used) has steady state errors, it is the easiest to implement. A disadvantage of this regulator is the limited speed range.

The speed loop is closed by using the 'anti-windup' PI described in the previous section. Initially, the integral term in the PI regulator is made zero and the performance is similar to a proportional regulator. Presently, there are some hardware and memory issues with an integral controller and more work needs to be done in order to eliminate those problems.

Initially, under no load, a speed is set in the watch window of the Real-Time monitor. From Fig. 54, it is observed that the duty cycle of the buck converter is very low. Then the

load is increased and it is observed that the controller responds to the increase in load by increasing the supplied current as illustrated in Fig. 55. Although the speed decreases, it decreases in magnitude by a mere 5% under a load torque of 0.38 N·m.

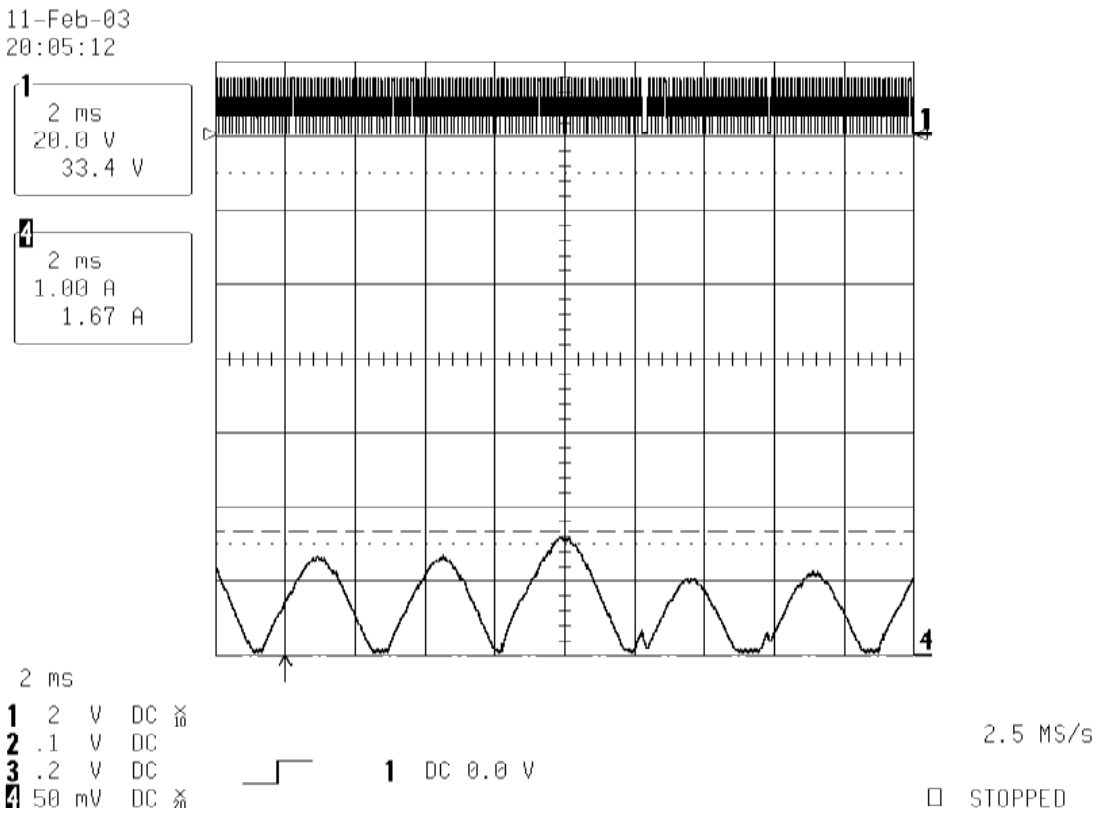

Fig. 54. Buck duty cycle and dc link current at no load

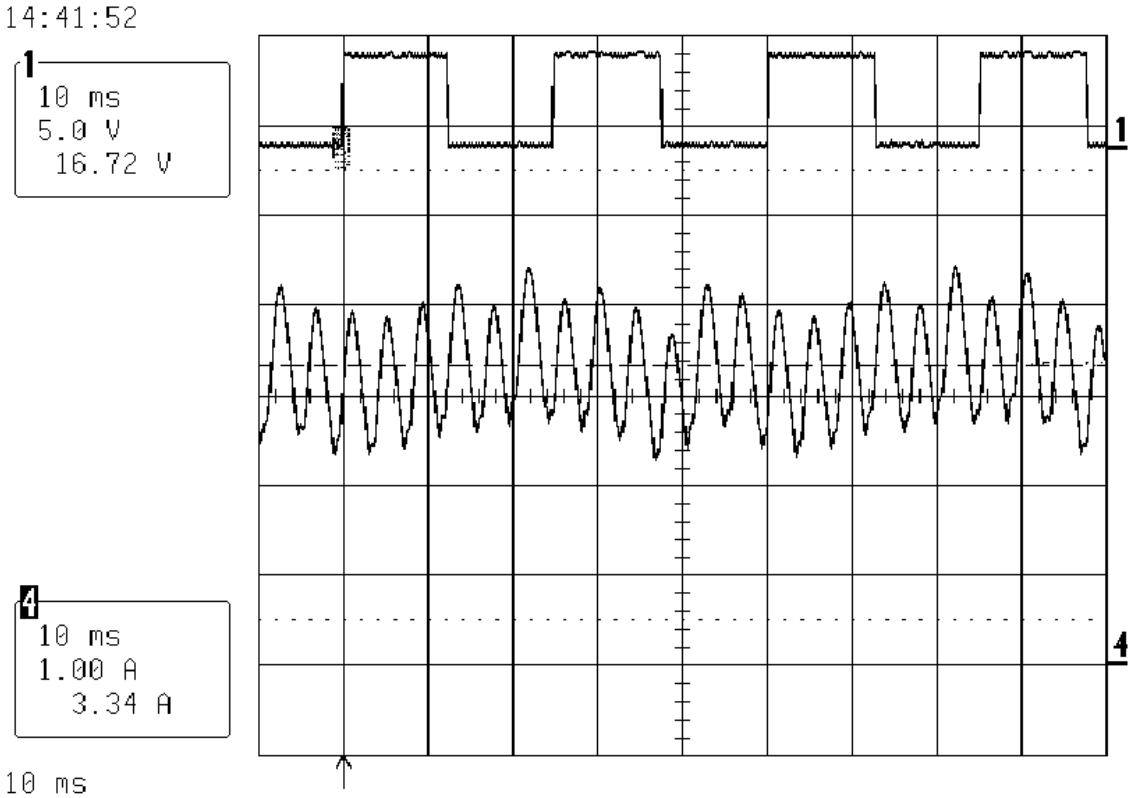

Fig. 55. Hall sensor output and dc link current under a load of 0.38 N·m

One of the motor phase currents is shown in Fig. 56. The commutation ripple is unavoidable during the transfer of current from one phase to another.phase.

8. Discussion of results

The results have shown that the speed control using a buck fed CSI is a cheaper alternative to the traditional VSI based BLDC drive. The only disadvantage is that the switching harmonics are transferred to the input source. This advantage can be overcome by replacing the buck converter with a Cuk converter. This makes the control more challenging, but nevertheless it is the ideal topology for commercial applications since it is supplied from an ac source.

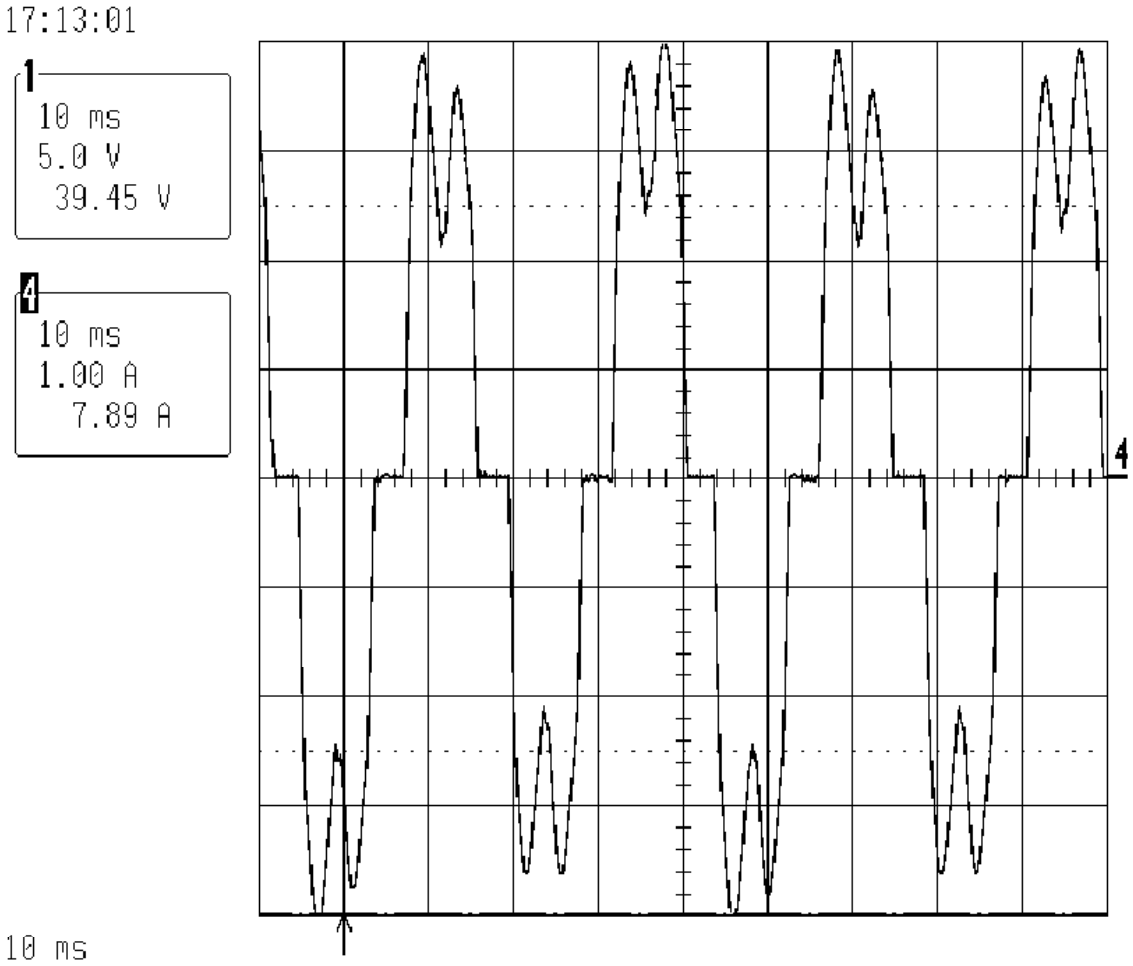

Fig. 56. BLDC phase current under a load of 0.38 N·m

9. Conclusions

We conclude that it is possible to reduce the cost of a BLDC drive by splitting the task of current control and synchronization into two separate modules, the dc-dc converter module controlling the magnitude of the current and the CSI implementing the task of synchronizing the conduction of the motor phases w.r.t. the rotor field positions. Following this approach, we can reduce the cost of the drive by approximately 30%. The only

disadvantage of using a CSI is the unavoidable current ripple of approximately 33%. This current ripple and the resulting torque ripple has to be considered if the proposed drive is to be chosen for a particular application.

10. Future work

The Cuk supplied CSI BLDC drive needs to be implemented as a part of future work. Better modeling of the drive, including the non-ideal behaviour of the switches is essential for accurately comparing the simulation with the experiment. Optimizing the inductor and capacitor values of the dc-dc converter would enable minimizing the cost of the proposed drive. Sensorless schemes should be considered for a further reduction in the cost of the drive.

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APPENDIX

MATLAB Program for inductor design

```
clear all;
B_sat_N30 = 0.39;
u_0 = 4*pi*1e-7;
u_i = 3700;
l_e = 550.5e-3;
L = 2e-3;
A_l = 5200e-9;
I_max = 5.6;
Num_turns = sqrt(L/A_l)
MMF = Num_turns*I_max;
H = MMF/ l_e
B = (u_0*u_i)*H
Nmax = (B_sat_N30*l_e)/(u_i*u_0*I_max)
```

VITA

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