

**DESIGN OF HIGH SPEED FOLDING AND INTERPOLATING
ANALOG-TO-DIGITAL CONVERTER**

A Dissertation

by

YUNCHU LI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2003

Major Subject: Electrical Engineering

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ABSTRACT

Design of High Speed Folding and Interpolating

Analog-to-Digital Converter. (May 2003)

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High-speed and low resolution analog-to-digital converters (ADC) are key elements in the read channel of optical and magnetic data storage systems. The required resolution is about 6-7 bits while the sampling rate and effective resolution bandwidth requirements increase with each generation of storage system. Folding is a technique to reduce the number of comparators used in the flash architecture. By means of an analog preprocessing circuit in folding A/D converters the number of comparators can be reduced significantly. Folding architectures exhibit low power and low latency as well as the ability to run at high sampling rates. Folding ADCs employing interpolation schemes to generate extra folding waveforms are called “Folding and Interpolating ADC” (F&I ADC).

The aim of this research is to increase the input bandwidth of high speed conversion, and low latency F&I ADC. Behavioral models are developed to analyze the bandwidth limitation at the architecture level. A front-end sample-and-hold unit is employed to tackle the frequency multiplication problem, which is intrinsic for all F&I ADCs. Current-mode signal processing is adopted to increase the bandwidth of the folding amplifiers and interpolators, which are the bottleneck of the whole system. An operational transconductance amplifier (OTA) based folding amplifier, current mirror-based interpolator, very low impedance fast current comparator are proposed and designed to

carry out the current-mode signal processing. A new bit synchronization scheme is proposed to correct the error caused by the delay difference between the coarse and fine channels.

A prototype chip was designed and fabricated in 0.35 μm CMOS process to verify the ideas. The S/H and F&I ADC prototype is realized in 0.35 μm double-poly CMOS process (only one poly is used). Integral nonlinearity (INL) is 1.0 LSB and Differential nonlinearity (DNL) is 0.6 LSB at 110 KHz. The ADC occupies 1.2 mm^2 active area and dissipates 200mW (excluding 70mW of S/H) from 3.3V supply. At 300MSPS sampling rate, the ADC achieves no less than 6 ENOB with input signal lower than 60MHz. It has the highest input bandwidth of 60MHz reported in the literature for this type of CMOS ADC with similar resolution and sample rate.

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CHAPTER I

INTRODUCTION

The analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are required between the analog signal and the digital signal processor (DSP) to take advantage of digital signal processing, because most signals in use are analog in nature.

1.1 Applications of High Speed ADCs

1.1.1 Digital Video and LCD Display

The operation of communication and entertainment systems is increasingly based on digital signal processing (DSP), while the physical signals needed to be handled at the input and output nodes of these systems remain continuous-time analog ones. Hence, such a system typically needs an analog-to-digital converter (ADC) at its input end and a digital-to-analog converter (DAC) at its output end (Figure 1).

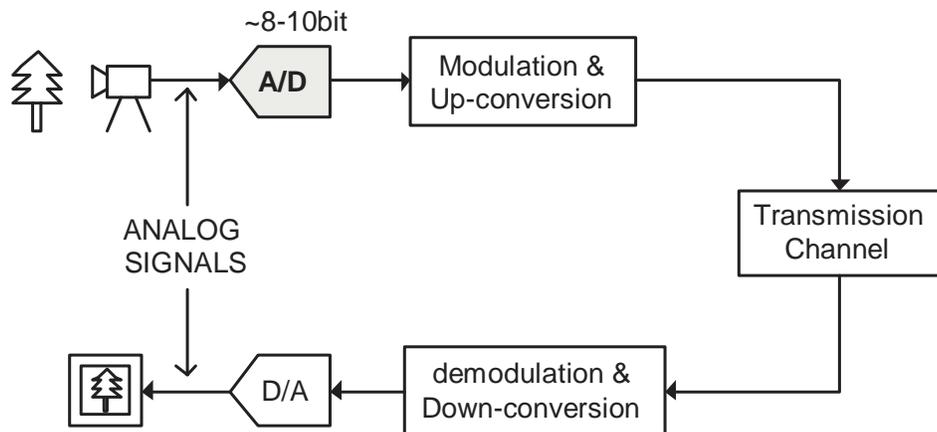


Figure 1 A typical digital TV system

A/D converters generally require more power and circuitry complexity than D/A converters to achieve a given speed and resolution, thus ADCs frequently limit performance in signal processing systems. Since A/D conversion limits overall system performance, development of improved A/D conversion algorithms and circuitry represents an extremely important area of research for the foreseeable future.

Digital television systems rely on digital transmission standard utilizing powerful image compression algorithms developed to reduce the transmission data rate. Such a system (Figure 1) requires an A/D converter to convert incoming analog video signal from a video camera. After digital processing and modulation, the signal sent out for transmission. The receiver demodulated received signal and converted back to analog video signal for display. A resolution is required for standard TV applications, while for high definition TV (HDTV) that number should be at least 10.

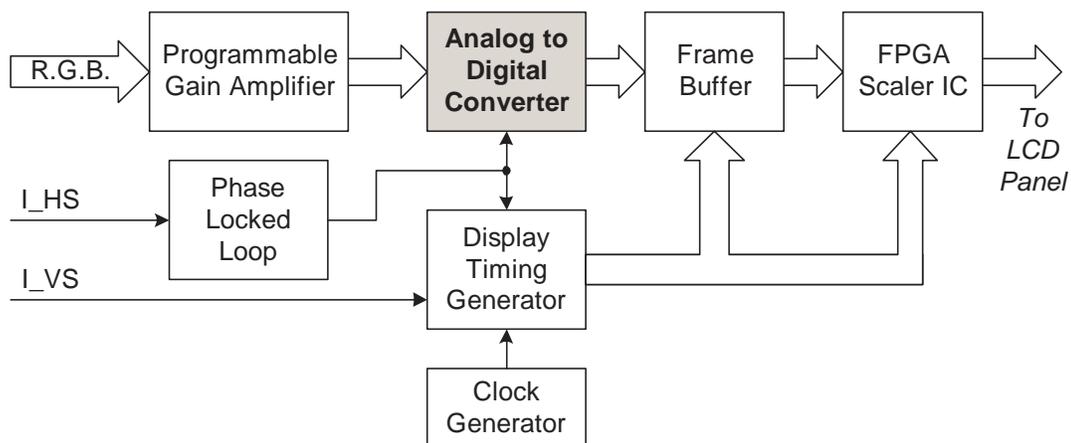


Figure 2 A typical LCD monitor's front end

High speed ADCs also found their applications in LCD display system. A recent trend is to use Liquid-Crystal-Display (LCD) to replace Cathode-Ray-Tube (CRT) monitors. Unlike their CRT counterparts, LCD monitors need digital driving signal, while many video sources are analog. A/D converters are required to convert these analog video signals to digital pixels (Figure 2). Depends on the resolution and refresh rate, the conversion rate varies from tens MSPS (mega-sample per second) to a few hundred MSPS.

1.1.2 Digital Measurement Equipment

Digital Sampling Oscilloscope (DSO) is another area requires high speed ADCs. A DSO comprises signal conditioning circuitry, a high speed ADC, a buffer memory, and a display (Figure 3)[80]. Many DSOs utilize high speed sampling circuitry with small aperture time to sample very high bandwidth input signals in GHz range. The sampling clock rates of these circuits, however, are relatively slow, about a few mega-samples per second. This technique is only suitable for narrow band, periodic input signals. When broadband signals need to be digitized, very high clock rate A/D converters are necessary. Non-periodic or broadband signals must be digitized mandating Nyquist rate sampling, which implies a sample rate greater than twice the bandwidth of the incoming signal.

Traditional DSOs require only 8-bit A/D conversion because the display is limited to that resolution; however, as more emphasis is placed upon digital storage and analysis of captured waveforms, limitation of display resolution no longer determine ADC accuracy. Therefore, newer DSOs are migrating to 10-12bit A/D converters and are functioning as digital waveform recorders, not merely oscilloscopes [11].

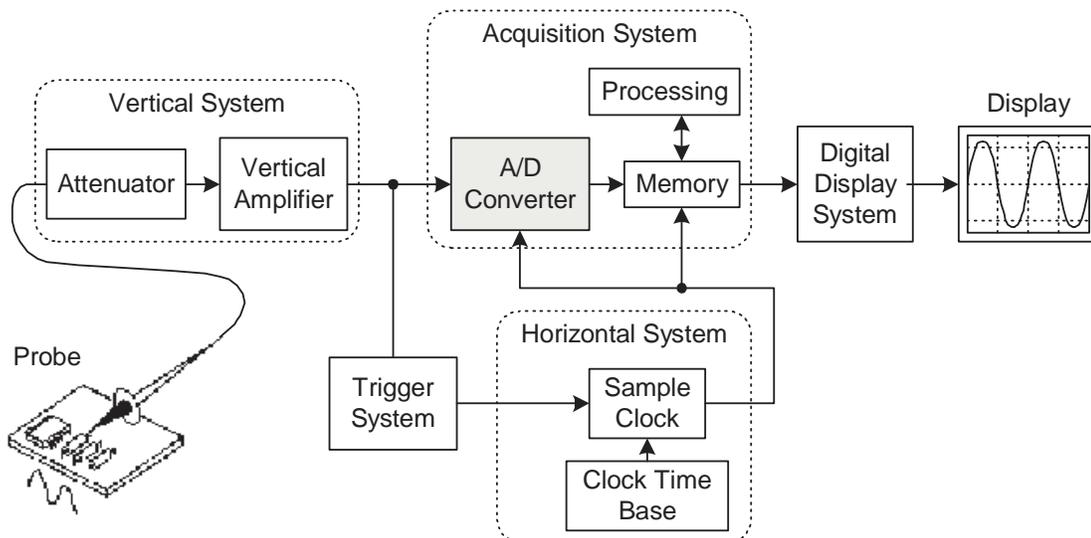


Figure 3 Block diagram of a digital sampling oscilloscope system

1.1.3 Disk Read Channel

ADCs have found their way into systems that would normally be considered as being entirely digital as these digital systems are pushed to higher levels of performance. Data storage is one example of such a system. As storage density in disk drive systems is increased, the signals handled by the read circuitry have become increasingly analog in character. Presently, 6-7-bit ADCs are commonly used in the read circuits of disk drives[60],[63].

Disk drive read channel signal processing is increasingly dominated by partial-response maximum likelihood (PRML) techniques which allow users to increase the data density by up to 100% compared to peak detect channels. However, this increase in performance is achieved at the expense of more sophisticated equalization and detection methods. This implies good dynamic performance from the analog-to-digital converter (ADC) over a wide range of input frequencies up to Nyquist frequency.

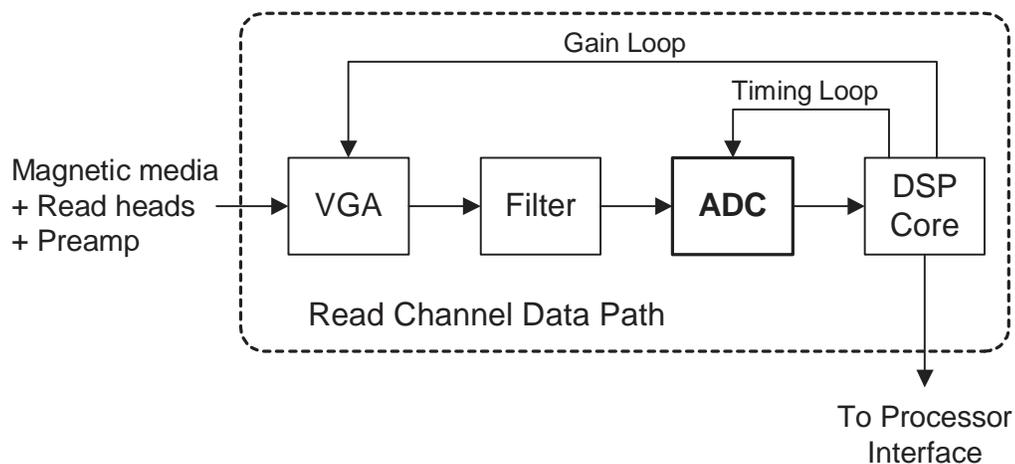


Figure 4 Disk read channel data path

Figure 4 shows the data path within a typical disk drive read channel[60]. The data are retrieved from the magnetic media using read heads, which generate a corresponding analog signal.

The signal from read heads is preamplified and fed into the integrated read-channel system, which converts and decodes the original data, and also provides for the digital interface. After passing through a variable-gain amplifier (VGA), the signal is further conditioned by a low-pass filter. The filter can perform equalization and/or anti-aliasing before driving the ADC [60]. The ADC provides digital samples of the filter output to the digital signal processing (DSP) core, which controls the sampling frequency (timing loop) and the gain of the VGA (gain loop) and ultimately recovers the data symbols.

The key requirement for the ADC is to achieve better than 5.5 ENOB for input frequencies up to $f_s / 4$ and better than five ENOB up to Nyquist frequency ($f_s / 2$) [99]. The required resolution is low (6-7b), while the sampling rate and effective resolution bandwidth requirements increase with each generation of storage system. For example, a 16× DVD system demands a 7-bit 432MS/s A/D converter [99]. Since the sampling rate can exceed 400 MHz, a wide input bandwidth is necessary. Also, due to the presence of various loops mentioned earlier, the ADC should exhibit low latency and good linearity. Low power and area are additional constraints, although less critical than the dynamic and noise performance.

1.2 Design Goals

The folding and interpolating (F&I) ADC architecture seeks to reduce the power and area of a flash converter, while maintaining its “one-step” nature. Folding architectures exhibit low power and low latency as well as the ability to run at high sampling rates. However, in some F&I ADCs, the effective number of bits (ENOB) decreases sharply as the input frequency increases [64],[19].

This project aimed to look into the speed as well as input bandwidth bottlenecks of F&I ADCs and find out solutions to increase the bandwidth of folding A/D converters at both architecture level and circuit level. This design is not targeted to one special application, so the design specifications (Table 1) are not strictly following any application standard. The general guideline is to design a high speed, low latency, low power F&I ADC with wide input bandwidth.

Considering this ADC may be used as a building block in a pipeline-folding hybrid A/D converter system, which has a conversion speed between 100-200MS/s, I didn't try to push either the speed or the resolution to the process limit. A resolution of 7-bit is a reasonable choice of a sub-ADC in a 12-bit pipeline-folding hybrid converter system[12].

TABLE 1 Specifications of the high speed folding and interpolating ADC design

Sampling clock rate	300Ms/s
Output data width	7-bit
Signal to Noise Ratio	39dB
Signal to Noise and Distortion Ratio	36dB
Input bandwidth	150MHz
Power supply voltage	3.3V
Power consumption	$\leq 200\text{mW}$
Technology of fabrication	TSMC 0.35um CMOS

1.3 Terminology and Notations

1.3.1 Sample and Hold

A sample-and-hold (S/H) or track-and-hold (T/H) circuit is frequently required to capture rapidly varying signals for subsequent processing by slower circuitry. The function of the S/H circuit is to track/sample the analog input signal and to hold that value while subsequent circuitry digitizes it. Although a S/H refers to a device which spends an infinitesimal time acquiring signals and a T/H refers to a device which spends a finite time in this mode, common practice will be followed and the two terms will be used interchangeably throughout this discussion as will the terms *sample* and *track*.

The function of a track-and-hold circuit is to buffer its input signal accurately during track mode providing at its output a signal which is linearly proportional to the input, and to maintain a constant output level during hold mode equal to the T/H output value

at the instant it was strobed from track to hold by an external clock signal. Figure 5 shows the waveforms of a practical sample-and-hold circuit.

Several parameters describe the speed and accuracy with which this operation is performed. The *track mode* is the state when the T/H output follows the T/H input. The *hold mode* refers to the period when the T/H output is maintained at a constant value. *Track-to-hold transition* is the instant when the circuit switches from the track mode to the hold mode and the *hold-to-track transition* refers to the switch from hold mode back to track mode. The time between successive *track-to-hold transitions* is the *sample period* whose reciprocal is the *sample rate*.

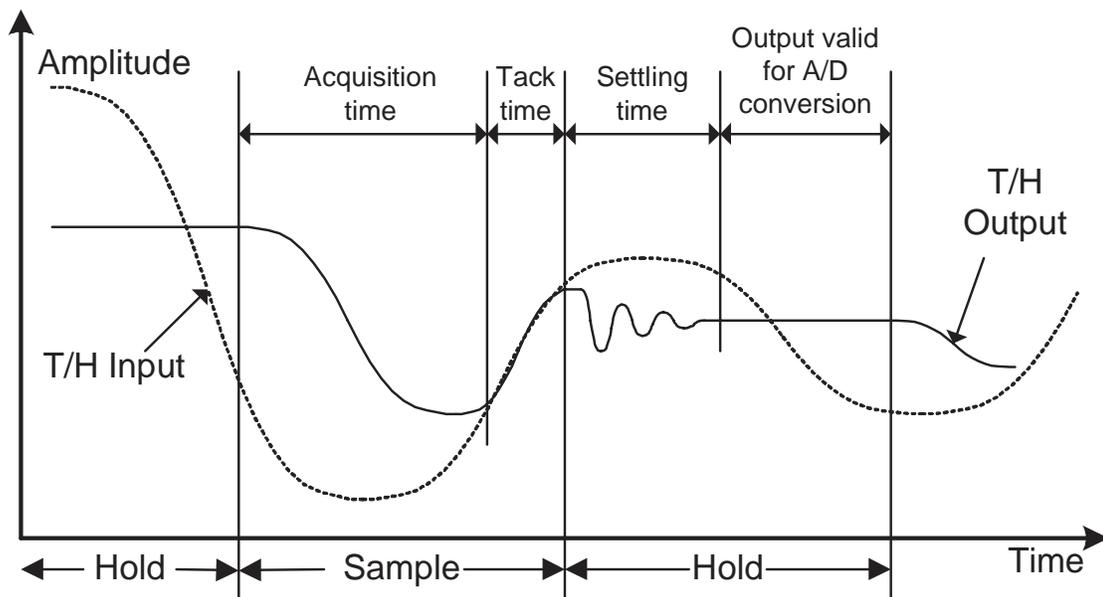


Figure 5 Track-and-hold terminologies

In track-or sample-mode, the T/H functions as a simple buffer amplifier. While in the hold mode two effects are of primary importance. The first is *droop* which describes the decay of the output signal as energy is lost from the storage element (usually a capacitor) within the T/H circuit. This is usually not a problem for CMOS amplifiers which have infinite DC input impedance. The second important aspect of hold mode performance is *feedthrough*, which describes the unwanted presence at the T/H output of a signal

component proportional to the input signal. The *signal feedthrough* is usually described as the ratio of the unwanted output signal to the input signal amplitude.

The *acquisition time*, is the time during which the sample-and-hold circuit must remain in the sample mode to ensure that the subsequent hold mode output will be within a specified error band of the input level that existed at the instant of the sample-and-hold conversion. The acquisition time assumes that the gain and offset effects have been removed. The remainder of time during the track mode exclusive of acquisition time is called the *track time* during which the T/H output is a replica of its input.

The *settling time*, is the time interval between the sample-and-hold transition command and the time when the output transient and subsequent ringing have settled to within a specified error band. Thus, the minimum sample-and-hold time is equal to the sum of acquisition time and settling time. The remainder of the time during the hold mode represents the maximum time available for A/D conversion if the T/H is used for that purpose. *Conversion time* of an A/D converter is the interval between the convert command and the instant when the digital code is available at the ADC output. Therefore, the minimum sample period of a practical A/D converter system is the sum of acquisition time, settling time, and conversion time.

The track-to-hold transition determines many aspects of sample-and-hold performance. The *delay time* is the time elapsed from the execution of the external hold command until the internal track-to-hold transition actually begins. In practical circuits this switching occurs over a non-zero interval called the *aperture time* measured between initiation and completion of the track-to-hold transition. Practical circuits do not exhibit precisely the same sample period for each sample. This random variation from sample to sample is caused by phase noise on the incoming clock signal and further exacerbated by electronic noise within the sample-and-hold itself. The standard deviation of the sample period is termed the *aperture jitter*. The time jitter causes an amplitude uncertainty, which depends on the rate of rise of the signal at the sample point. Finally, at the track-to-hold transition, circuit effects frequently give rise to a perturbation at the sample-and-hold output. This effect which manifests itself as a

discontinuity in the sample-and-hold output waveform called *hold jump* or *hold pedestal* can depend on the input signal giving rise to distortion.

1.3.2 Quantizer

A *quantizer* is a device that converts a continuous range of input amplitude levels into a finite set of discrete digital code words. Theoretically an *analog-to-digital conversion* process comprises a sampling and quantization processes. An A/D converter system usually consists of a quantizer along with other signal conditioning circuitry such as amplifiers, filters, sample-and-hold circuits etc. Despite this difference, the terms quantizer and A/D converter are often used synonymously.

A quantizer can be uniquely described by its transfer function or quantization characteristic, which contains two sets of information: the first includes the digital codes associated with each output state, and the second includes the *threshold levels* which are the set of input amplitudes at which the quantizer transitions from one output code to the next.

Figure 6 shows the transfer characteristic of an ideal 3-bit quantizer. The analog input voltage normalized to full scale (FS) is shown on the horizontal axis. The digital output code is given on the vertical axis. The quantizer has been designed so that the output digital word changes when the analog input is at odd multiples of FS/16. The LSB of the digital output code changes each time the analog input changes by $FS/2^n$ where n is equal to the number of digital bits. A change of $FS/2^n$ in the analog input is called an LSB. In Figure 6, an LSB is the length of the horizontal part of the staircase, or FS/8. The ideally quantized ranges of the analog input are shown just above the horizontal axis on Figure 6. These ranges are centered about even multiples of FS/16 except for the rightmost and leftmost, which have no right or left limits, respectively.

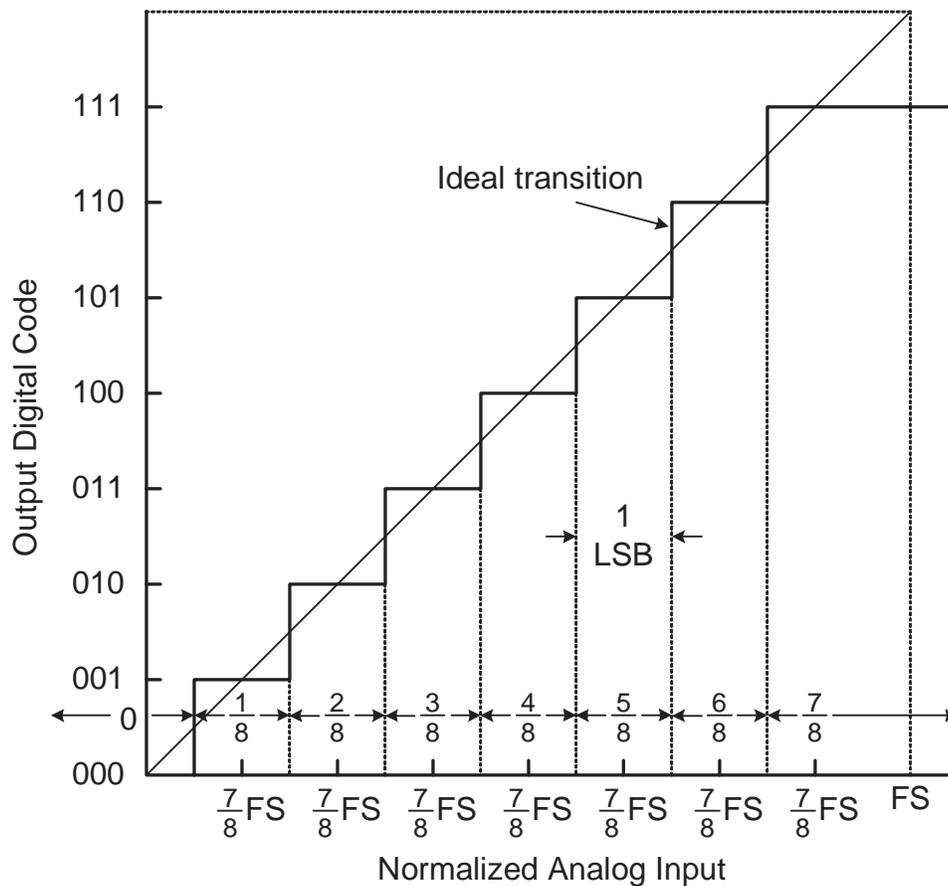


Figure 6 Ideal input-output characteristics for a 3-bit quantizer

Graphically, the quantizing process means that a straight line representing the relationship between the input and the output of a linear analog system is replaced by a transfer characteristic that is staircase-like in appearance. The quantizing process has a two-fold effect: (i) the peak-to-peak range of input sample values is subdivided into a finite set decision levels or decision thresholds that are aligned with the “risers” of the staircase, and (ii) the output is assigned a discrete value selected from a finite set of representation levels or reconstruction values that are aligned with the “treads” of the staircase. The transfer characteristic of uniform quantizer is shown in Figure 7(a) for midtread type, and in Figure 7(b) for midriser type. The separation between the decision thresholds and the separation between the representation levels of the quantizer have a common value called the *step size* Δ .

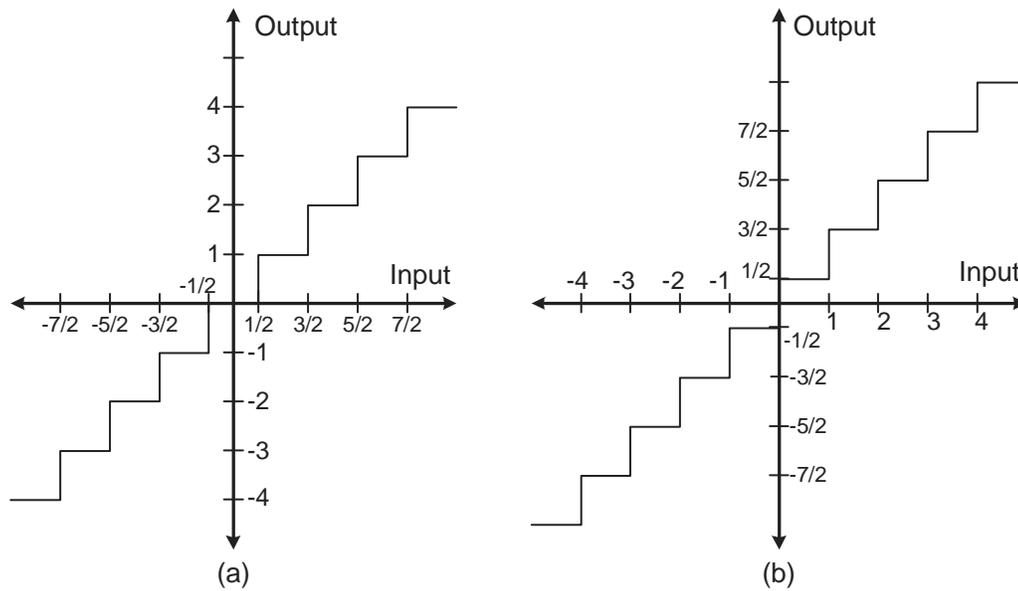


Figure 7 Ideal quantizer transfer characteristic. (a) midtread (b) midriser

An ADC's actual threshold levels are denoted by T_k where the index k ranges from 0 to M giving a total of $M+1$ values. Correspondingly, ideal thresholds levels are denoted T_k^* . For an N -bit bipolar quantizer, a midtread characteristic has $M = 2^N$ thresholds and has one quantization level with value zero. A midriser characteristic has $M + 1 = 2^N + 1$ thresholds, one of which has value zero. By convention, $T_0 \equiv -\infty$, and $T_M = +\infty$ and for each characteristic so only $M - 1$ physical thresholds actually exist.

Based on the locations of thresholds, quantizers can be divided to two categories: uniform and non-uniform (Figure 8). The thresholds of uniform quantizers are evenly distributed while in non-uniform quantizers thresholds locations match the probability density function of the incoming signal (such as human speech). Uniform quantizers are most commonly used and will be dealt with exclusively here.

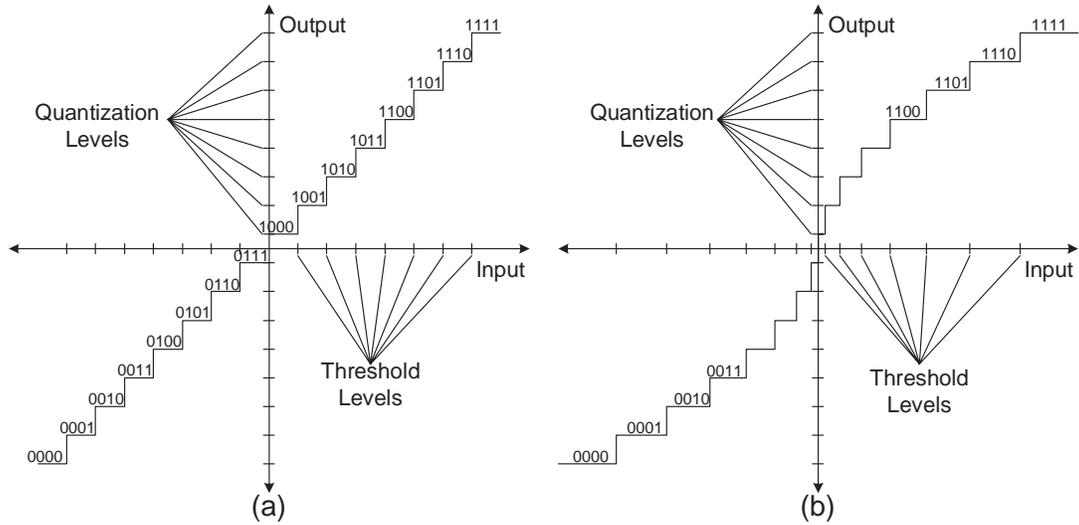


Figure 8 Quantizer transfer characteristics (a) uniform quantizer. (b) non-uniform quantizer

The *Full-Scale Range*, *FSR*, of a quantizer represents full scale input range. The length of adjacent intervals is called the *quantization step* or simply Δ . For a N -bit quantizer, the relationship between the Full-Scale Range and the quantization step can be described by

$$\Delta = \frac{FSR}{2^N} \quad (1.1)$$

A term related to Full-Scale Range is *Full-Scale*, *FS*, which is the magnitude of the Full-Scale Range's maximum excursion from the transfer function origin. For a bipolar quantizer with origin located at the center of full-scale range, $FS = FSR/2$. For a unipolar quantizer, $FS = FSR$.

Real quantizer transfer functions fall short of the ideal because imperfections in fabrication cause actual thresholds to deviate from their desired placement. Such non-idealities can be expressed in several ways (Figure 9). An error which causes all thresholds to shift from their ideal positions by an equal amount is called an *offset* (V_{off}). Non-ideality which results in an erroneous quantizer step size, Δ , is called *gain error*. Δ can be defined as a function of FSR (Eq. 1.1).

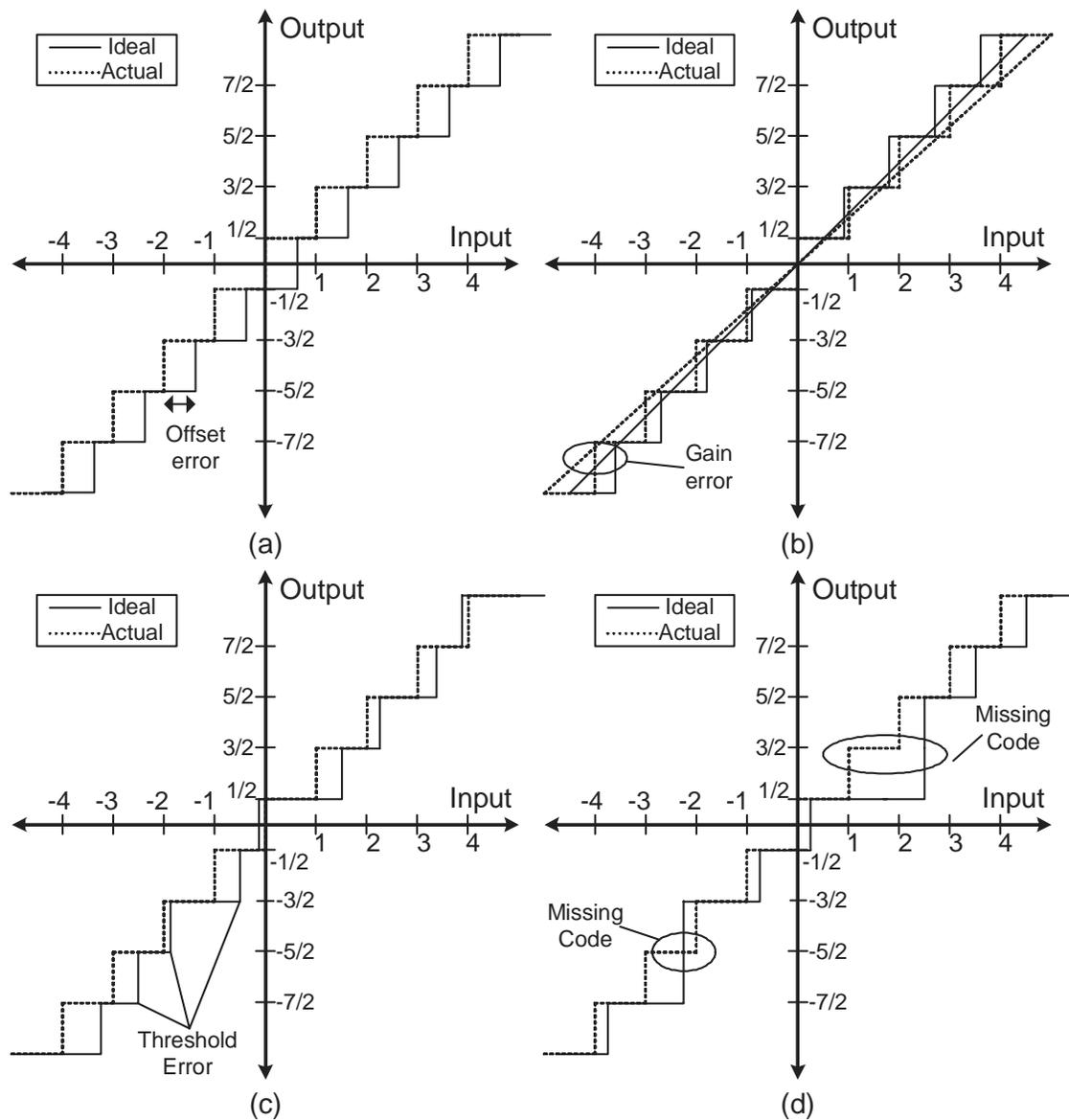


Figure 9 Quantization transfer functions including error sources (a) offset error. (b) gain error. (c) linearity error. (d) missing codes

The step size Δ can be assigned the value which minimizes threshold errors as calculated by linear regression. In the latter case Eq. (1.1) still holds, but FSR is a function of Δ instead of vice-versa. *Linearity error* refers to the deviation of the actual threshold levels from their ideal values after offset and gain errors have been removed. Excessive linearity error results in *missing codes*, a condition wherein a valid output

code, say Δ_i , never occurs because its defining interval $[T_i, T_{i+1}]$ has become vanishingly small, $T_{i+1} \leq T_i$. Linearity error is quantified by the *threshold level errors*,

$$\varepsilon_k = T_k - V_{\text{off}} - T_k^* \quad (1.2)$$

where k is defined for thresholds 0 through M but has meaning only for the real thresholds 1 through $M-1$. This array of error terms, also called *Integral Nonlinearity* or simply INL. Here, INL is defined for each digital word, but one should be aware that sometimes the term “INL” is defined as the maximum magnitude of the INL values.

Related to *INL* is the *Differential Nonlinearity* or *DNL*:

$$d_k = T_k - T_{k-1} - \Delta \quad (1.3)$$

Since DNL is defined by a first-order difference equation, it is valid only for the range $1 \leq k \leq M$ and only has physical meaning over $2 \leq k \leq M-1$. The element array of DNL values is also frequently described by its statistical properties such as peak and rms. The terms integral and differential arise when describing the above two error measures because DNL can be defined as the first-order difference of the INL sequence.

$$\begin{aligned} d_k &= T_k - T_{k-1} - \Delta \\ &= T_k - T_{k-1} - (T_k^* - T_{k-1}^*) \\ &= (T_k - T_k^* - \Delta) - (T_{k-1} - T_{k-1}^* - \Delta) \\ &= \varepsilon_k - \varepsilon_{k-1} \end{aligned} \quad (1.4)$$

Several terms are commonly used to describe the relative power of the analog input to an A/D converter. The *loading factor*, LF, expresses the RMS amplitude of the input waveform relative to the quantizer FSR:

$$LF = \frac{V_{RMS}(\text{Input})}{FSR/2} \quad (1.5)$$

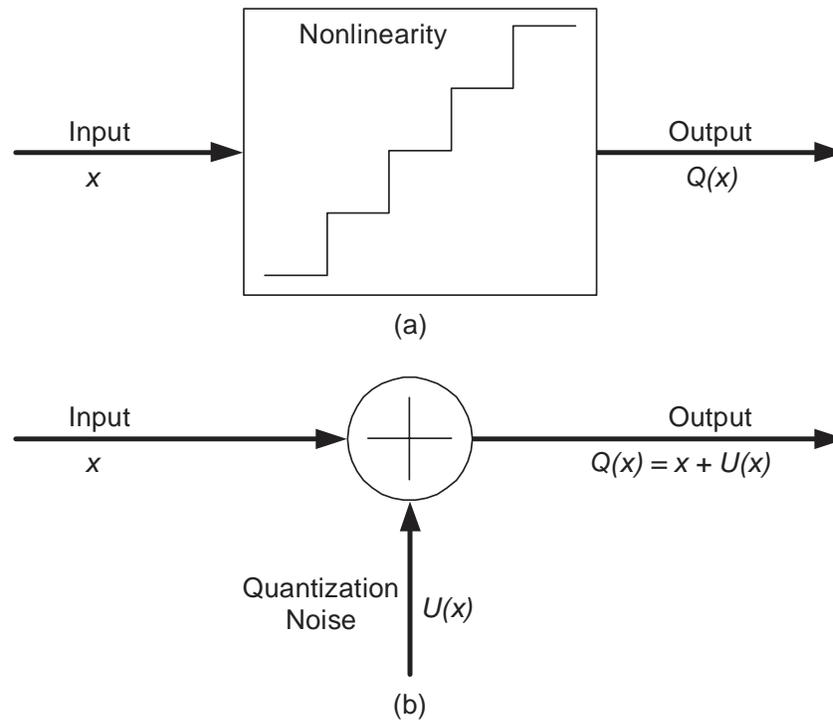


Figure 10 Quantizer models. (a) nonlinear deterministic model. (b) statistical model

1.3.3 Quantization Noise [35]

The quantization process can be described by a nonlinear input–output transfer function as depicted in Figure 10. The quantized output signal, $Q(x)$, is the sum of the original input signal, x , and a quantization error, where

$$U(x) = Q(x) - x \quad (1.6)$$

Here $U(x)$ is the error resulting when the input signal, x , is quantized with finite resolution. This quantization error, as shown in Figure 11, is a deterministic function of the input signal, x .

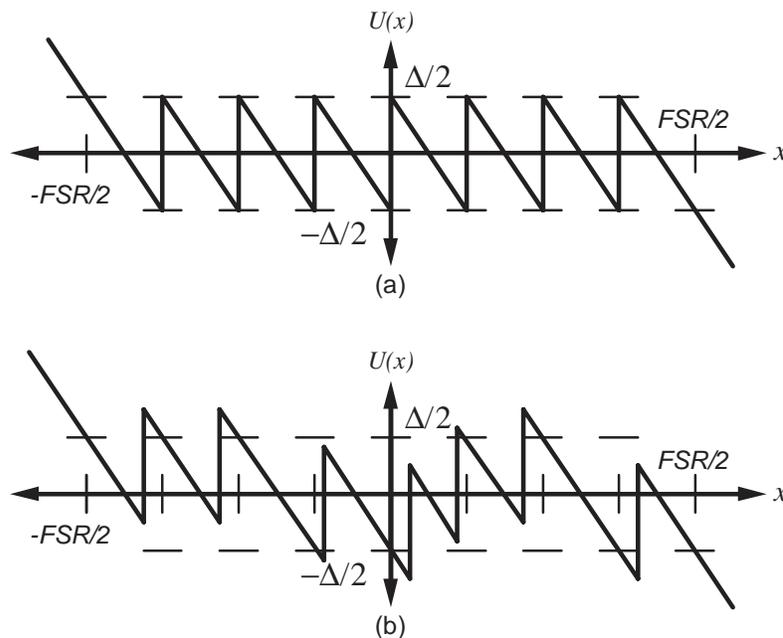


Figure 11 Quantization noise models. (a) ideal quantizer. (b) quantizer with threshold level errors

However, subject to certain simplifying constraints [22],[27]; can be approximated as a random noise component. The constraints necessary to justify this statistical model are:

- $U(x)$ is a stationary process
- $U(x)$ is uncorrelated with x
- The elements of are $U(x)$ uncorrelated with each other
- The probability density function of $U(x)$ is uniform over $(-\Delta/2, \Delta/2)$

Under these constraints $U(x)$ is often modeled as a uniformly distributed random variable thereby simplifying the analysis of quantizer performance.

Quantizer operation is frequently characterized by signal-to-noise ratio (SNR), which expresses (usually in decibels) the ratio of the output signal power to the output noise power. Since the quantization noise is assumed to be uniformly distributed on $(-\Delta/2, \Delta/2)$ the output noise power can be easily calculated as

$$\begin{aligned}
\sigma^2(\Delta) &= \int_{-\infty}^{+\infty} x^2 p_{\Delta}(x) dx \\
&= \int_{-\Delta/2}^{+\Delta/2} x^2 \frac{1}{\Delta} dx \\
&= \frac{\Delta^2}{12}
\end{aligned} \tag{1.7}$$

The power of the full swing sinusoidal input signal is

$$P_s = (FSR/2)^2 / 2 = FSR^2 / 8 = (2^N \Delta)^2 / 8 \tag{1.8}$$

The quantizer SNR is therefore given by

$$\begin{aligned}
SNR_Q &= 10 \log \left(\frac{2^{2N} \cdot \Delta^2 / 8}{\Delta^2 / 12} \right) \\
&= 10 \log (3 \times 2^{2N}) \\
&= 6.02N + 1.76(dB)
\end{aligned} \tag{1.9}$$

where the subscript Q modifying SNR refers to quantization noise as distinct from thermal noise or other deleterious error sources which compromise overall signal to noise ratio. Eq. (1.9) is a frequently used equation for predicting optimum A/D performance. For a 7-bit converter maximum SNR is 43.9 dB, and for an 8-bit converter the maximum SNR is 49.92dB.

Eq. (1.9) can be used to assess the performance of any quantizer relative to the ideal. By replacing the maximum achievable SNR by the actual SNR and solving for the equivalent resolution, N , a figure of merit called the Effective-Number-Of-Bits (ENOB) results.

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{1.10}$$

The effective-number-of-bits is a commonly used metric for summarizing the performance of non-ideal quantizers. In practice, A/D converters encounter inputs which are more complicated than simple sinusoids. Under conditions with such complicated signal environments, the A/D converter may have different achievable maximum SNR.

1.4 Fundamental Limits to Performance

Many factors impact overall system operation and can limit performance below the ideal, such as thermal noise, aperture jitter and comparator metastability, etc. Based on analysis in [11], several such factors, which present limits on A/D converter performance, will now be discussed.

1.4.1 Thermal Noise

In a $50\ \Omega$ system, thermal noise induced by the source resistance limits A/D converter resolution to a sub-ideal value which can be calculated if the system bandwidth, Δf , and signal amplitude, $V_{FSR}/2$, are known [46]. The noise power available from the source resistance is

$$P_n = kT\Delta f \quad (1.11)$$

where k is Boltzmann's constant, T is the temperature in degrees Kelvin, and as Δf previously defined is the bandwidth of the system. The maximum signal power is

$$P_s = \frac{1}{2} \left(\frac{V_{FSR}}{2} \right)^2 \frac{1}{R} \quad (1.12)$$

where R is the source resistance and full-scale sinusoidal input is assumed. The maximum achievable SNR of an A/D converter operating under such circumstances is:

$$SNR_T = \frac{P_s}{P_n} = \frac{V_{FSR}^2}{8kTR\Delta f} \quad (1.13)$$

By using this expression for SNR in Eq. (1.10) the maximum attainable quantizer resolution or effect number of bits, as limited by thermal noise is seen to be

$$ENOB = \frac{1}{2} \log_2 \left(\frac{2}{3} \times \frac{V_{FSR}^2}{8kTR\Delta f} \right) \quad (1.14)$$

For a given quantizer input range, V_{FSR} , achievable resolution, $ENOB$, is inversely proportional to bandwidth and absolute temperature as shown in Figure 12. As can be seen from this graph, 7-bit resolution is within the thermal limit for bandwidths well above the 150MHz design goal.

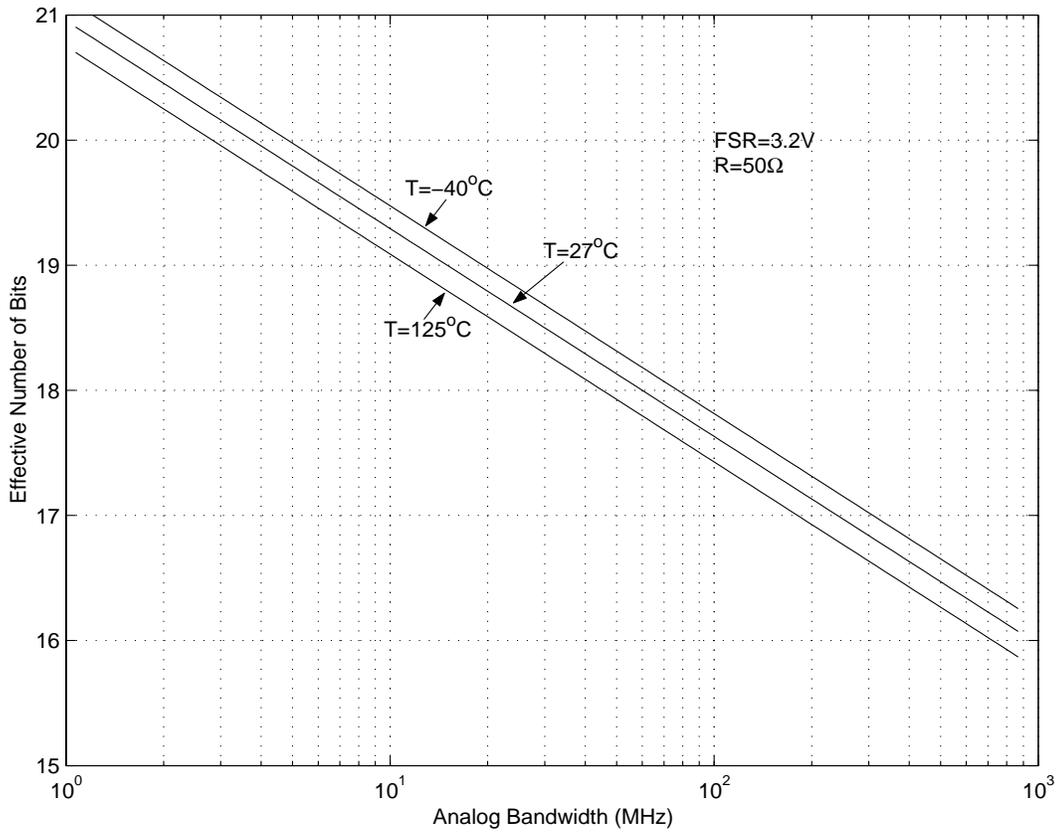


Figure 12 Limit of thermal noise on the resolution of ADC

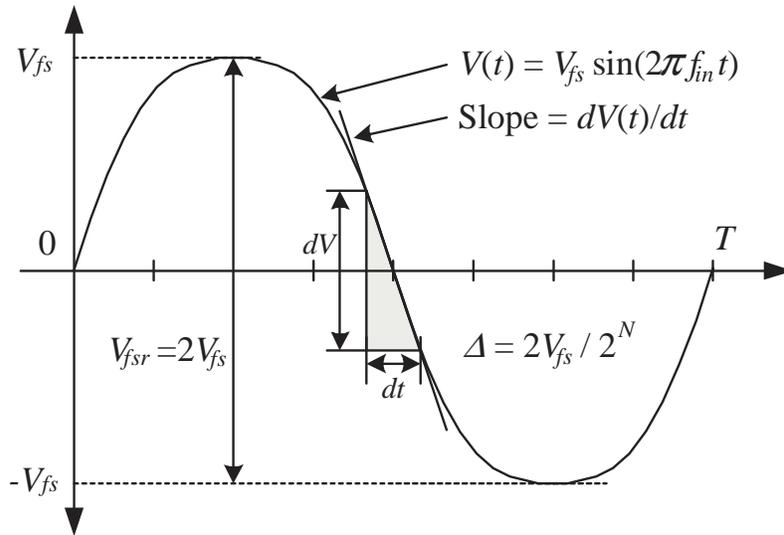


Figure 13 Aperture uncertainty causes amplitude errors

1.4.2 Aperture Jitter

Aperture jitter, which is the noise-induced uncertainty in the otherwise periodic sampling interval, also places a fundamental limit on achievable resolution [46], [73], [97], [84] for the following reason. If a signal is changing in time with a maximum slew rate equal to S , and its value is to be determined with error less than $\Delta/2$, then the sampling instant, T must be defined with accuracy dT (Figure 13) such that

$$dT \leq \frac{\Delta}{2S} \quad (1.15)$$

where the timing uncertainty, dT , is referred to as the aperture jitter, .If the A/D converter requires N bit resolution, then to ensure amplitude error less than $\pm 1/2$ LSB, must be limited such that

$$dT \leq \frac{V_{FSR}/2^N}{2S} \quad (1.16)$$

If the input is a sinusoid with amplitude of $V_{FSR}/2$, then the maximum slew rate is

$$S = 2\pi f_{in} \frac{V_{FSR}}{2} = \pi f_{in} V_{FSR} \quad (1.17)$$

Substitute Eq. (1.17) to (1.16) yields,

$$dT \leq \frac{2^{-(N+1)}}{\pi f_{in}} \quad (1.18)$$

This constraint shows the maximum aperture jitter consistent with N -bit resolution. (Figure. 14)

Alternatively, Eq. (1.11) may be solved for N in terms of τ_{jitter} giving

$$ENOB \leq \log_2 \left(\frac{1}{\pi f_{in} \tau_{jitter}} \right) - 1 \quad (1.19)$$

This relationship, plotted in Figure 14 for various values of τ_{jitter} , shows that to achieve 7 effective bits of resolution at 150MHz, τ_{jitter} must be kept well below 10ps; and to maintain adequate margin for this parameter a value close to 5ps is desirable. This constraint on acceptable jitter mandates use of a track-and-hold circuit preceding the 7-

bit quantizer and further implies that on-chip clock buffer circuitry must be designed specifically to prevent degradation of the phase noise from that presented to the A/D converter from outside clock and signal sources.

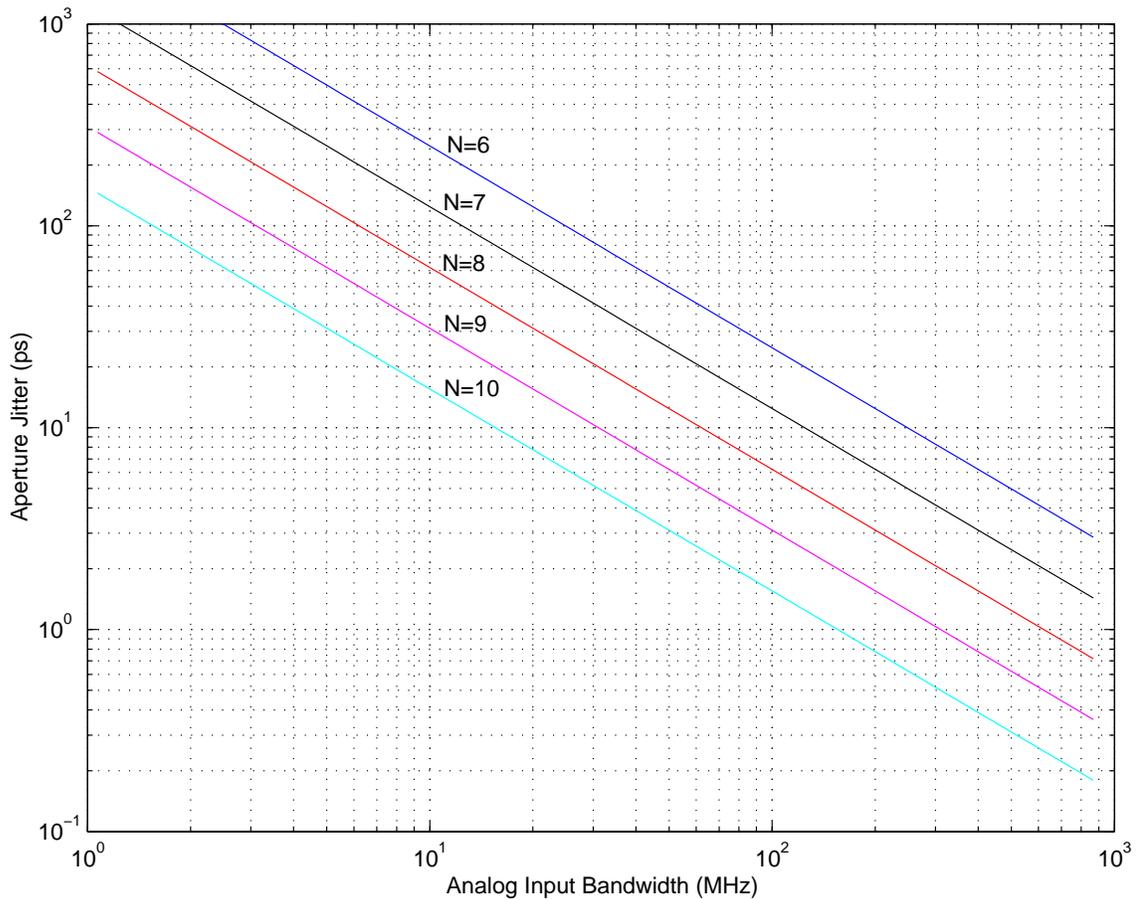


Figure 14 Maximum aperture jitter consistent with $\frac{1}{2}$ LSB errors for different resolutions

1.4.3 Comparator Metastability

Comparator regeneration time also places a fundamental limit on achievable resolution [21],[28],[29],[41],[46],[104] for the following reason. If a comparator is given a finite time to regeneratively produce a logic-level output, then for some range of differential input values near zero, the comparator output will not be large enough to be unambiguously interpreted by succeeding encoding logic. This logic can therefore

produce erroneous output codes which increase the noise power in the quantizer output waveform thereby diminishing SNR. Such coding errors have been called conversion errors, rabbit errors, sparkle codes, and metastability errors. The nature of the digital output produced under conditions of metastability errors depends greatly on the output coding format used. With most forms of binary coding, metastability errors manifest themselves as output code errors, which can be modeled as a random N -bit word. The power contributed to the quantizer output noise in this case is:

$$E\{n^2 | ConversionError\} = \frac{(2^N \Delta)^2}{12} \quad (1.20)$$

Note that this result follows directly from Figure 12 and Eq. (1.12) that predict the quantizer output noise to be $\Delta^2/12$ for outputs uniformly distributed on $(-\Delta/2, +\Delta/2)$. In the present case, the output (under the conditions of a metastability error and binary coding) is presumed to be uniformly distributed on $(-FSR/2, +FSR/2)$. Eq. (1.20) follows directly. The output noise due to metastability errors becomes

$$\begin{aligned} \sigma^2(n) &= E\{n^2 | MetastabilityError\} \cdot p_{ME} \\ &= \frac{\Delta^2}{12} \times 2^{2N} p_{ME} \end{aligned} \quad (1.21)$$

If Gray coding is used rather than binary, metastability errors manifest themselves as a single bit error in an otherwise accurate output codeword. This beneficial effect arises because in Gray coded A/D converters each comparator influences one *and only one* output bit. Therefore, a metastable comparator causes the corresponding bit to become indeterminate, but all other bits behave correctly (ignoring the unlikely event of two metastable comparators during one conversion). In fact, this characteristic is the chief rationale for implementing Gray encoding in A/D converters. When a metastability error gives rise to an erroneous output bit, the amount of noise added to the output corresponds to an amplitude error equal to one quantizer step, Δ ; however, with probability 1/2 the bit in question will assume the correct value. Therefore, the expected mean-square noise given a metastability error is

$$E\{n^2 | ConversionError\} = \frac{(\Delta^2 + 0^2)}{2} \quad (1.22)$$

Thus the noise power due to metastability errors in Gray coded converters becomes

$$\begin{aligned} \sigma^2(n) &= E\{n^2 | MetastabilityError\} \cdot p_{ME} \\ &= \frac{\Delta^2}{2} p_{ME} \end{aligned} \quad (1.23)$$

which is less than the noise power in a binary converter (Eq.1.21) by the factor $2^{2N}/6$. This factor represents an extreme noise reduction for even modest resolution A/D converters.

The maximum SNR with metastability errors can be calculated by replacing the denominator of Eq. (1.24) which is the noise due to quantization with the noise expressions developed for metastability errors (Eq. 1.21 and 1.23) the maximum achievable SNR given metastability errors results. For binary encoding

$$SNR_{Metastability} = \frac{2^{2N} \Delta^2 / 8}{(\Delta^2 / 12) \times 2^{2N} p_{ME}} = \frac{3}{2 p_{ME}} \quad (1.24)$$

and for Gray encoding

$$SNR_{Metastability} = \frac{2^{2N} \Delta^2 / 8}{(\Delta^2 / 2) \cdot p_{ME}} = \frac{2^{2N}}{4 p_{ME}} \quad (1.25)$$

Eq. (1.20) can be used to convert the above SNR expressions into effective bits. For binary encoding

$$ENOB_{ME} = -\frac{1}{2} \log_2(p_{ME}) \quad (1.26)$$

and for Gray encoding

$$ENOB_{ME} = N - \frac{1}{2} \log_2(p_{ME}) - \frac{1}{2} \log_2 6 \quad (1.27)$$

The probability of a metastability error depends upon the statistics of the input signal, but if a uniformly distributed input is assumed, p_{ME} is given by [104]

$$p_{ME} = \frac{2V_{Logic}}{A \cdot \Delta} \quad (1.28)$$

where V_{Logic} is the minimum amplitude voltage which will unambiguously be interpreted as an appropriate logic level (so represents the range of ambiguous voltages), A is effective gain of a comparator at the end of the latch mode, and Δ is the quantizer step size. p_{ME} is seen to be the ratio of the ambiguous voltage range (referred to the comparator input) divided by total input range seen by the same comparator. The effective comparator gain, A , which is dependent upon the dynamic comparator response and the time allowed to regeneratively establish an output state can be described as

$$A = A_0 e^{t/\tau} \quad (1.29)$$

where A_0 is the the combined gain of the preamplifier and the latch's gain in the transparent state, τ is the regenerative time-constant (assumed first order) for the latch. The metastability error probability of then becomes

$$p_{ME} = \frac{2V_{Logic}}{A_0\Delta} e^{-t/\tau} \quad (1.30)$$

where t , the amount of time the comparator is allowed to regenerate, is nominally one half of the clock period less the propagation delay of the decode circuitry. To first order the metastability error probability is independent of the analog input frequency.

For a differential latch, the regenerative time constant can be approximated by

$$\tau \approx C/g_m \quad (1.31)$$

where C is the total capacitance at a regenerative node, and g_m is the transconductance of a regenerative element in the latch biased at its switching point [104].

Eq. (1.31) can be used with Eq. (1.27) to predict maximum effective resolution as limited by metastability errors with binary encoding

$$ENOB_{ME} = \frac{T_s}{4 \ln 2 \cdot \tau} - \frac{1}{2} \log_2 \left(\frac{2V_{Logic}}{A_0\Delta} \right) \quad (1.32)$$

The achievable resolution for Gray encoding can be calculated in a similar fashion to Eq.(1.32) giving

$$ENOB_{ME} = N + \frac{T_s}{4 \ln 2 \cdot \tau} - \frac{1}{2} \log_2 \left(\frac{2V_{Logic}}{A_0\Delta} \right) - \frac{1}{2} \log_2 6 \quad (1.33)$$

where N is the number of bits in the Gray-encoded output word. Eq. (1.33) is plotted in Figure 15 to show how the achievable effective number of bits is limited by the latch metastability, which depends on the RC time constant of the latch. Notice that the achievable resolution as limited by metastability errors in this case is greater than that achievable in the binary case so long as $N > 0.5 \log_2 6 = 1.29$; that is, for all resolutions of practical interest. For a Gray encoded A/D converter to achieve the same ENOB, the latch time-constant can be 3 times higher than that of a binary encoded A/D converter.

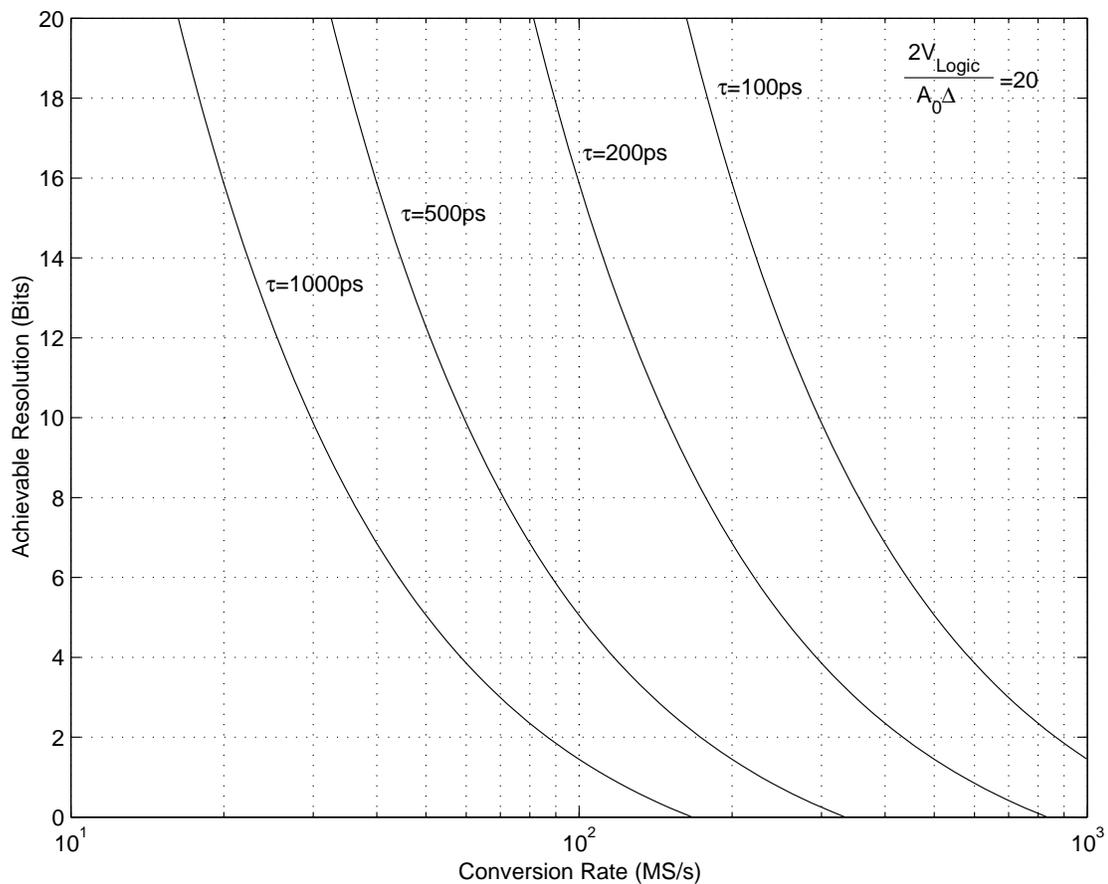


Figure 15 Achievable resolution as limited by metastability errors

In some applications, notably video signal processing, SNR is not the most important measure of performance degradation due to metastability errors. Rather, peak error is the metric used for such characterization because large code errors when reconstructed via

D/A conversion appear on a video monitor as noticeable pixel amplitude discontinuities. These momentary discontinuities, a white pixel on a dark background or vice-versa, seem to the human visual system like sparkles—hence the name sparkle codes. Gray encoding helps greatly in this regard by limiting the maximum metastability-induced error to one LSB.

CHAPTER II

HIGH SPEED A/D CONVERTER ARCHITECTURES

A brief comparison of A/D converter architectures that are suitable to implement a high-speed medium resolution is presented in this chapter.

2.1 Fully Parallel (Flash) A/D Converter

A simple way to make a high-speed A/D converter is to use a full-flash structure [1], [4],[9],[23],[32],[45],[59],[65],[67],[85],[97],[100],[103] as shown in Figure 16. This type of converter consists of an array of $2^n - 1$ comparators with n being the number of bits. Each comparator is connected with one input to the input voltage and with the other input to a reference voltage. This reference voltage is generally generated by a resistor ladder. The outputs of the comparators are fed into encoding logic that generates the data bits. The collection of digital outputs from this comparator bank is called a *thermometer code* because every comparator output below some point along the array is a logic “1” (corresponding to the mercury-filled portion of a thermometer) while all comparator outputs above this position are logic “0” (corresponding to the empty portion of a thermometer).

Flash A/D conversion is by far the fastest and conceptually simplest conversion process, because the flash converter needs only one clock cycle per conversion. Moreover, since references are made by a resistor string, they are monotonic, resulting in low differential nonlinearity. The advantage of this full-flash converter is its ease of design and its inherently good high frequency behavior. For resolutions larger than 7b, offset compensation is required in order to avoid using large transistors in the comparators for matching reasons[69].

However, there are several drawbacks. One is that the hardware complexity increases exponentially with the resolutions because it needs a $2^N - 1$ comparator circuits. This also means that the power dissipation and the chip area increase exponentially with the resolution. The second drawback is that the analog input must drive the large nonlinear input capacitance of the comparators. Since this input capacitance for the 8-bit is

typically 15-30pF and the driving current reaches 30-60mA for a 100 MHz, 3 V p-p input signal, large signal distortion may occur, further aggravated by the nonlinearity of the input capacitance.

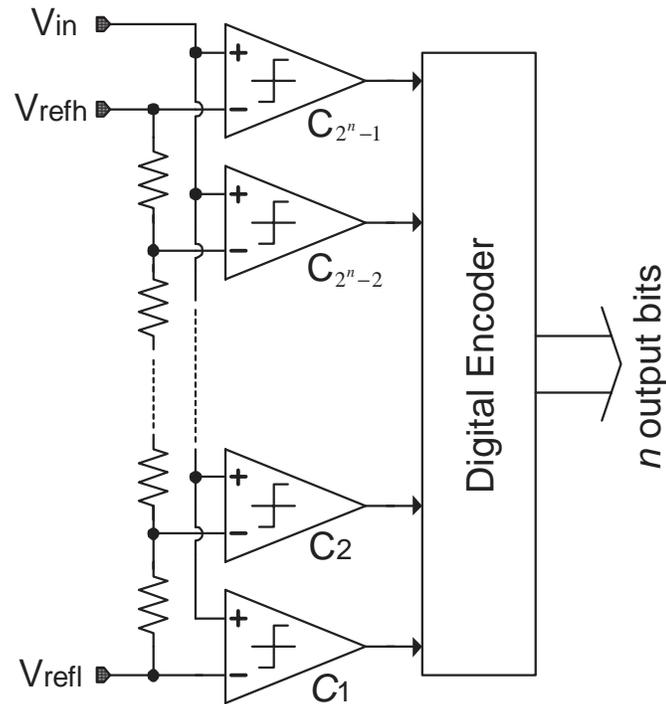


Figure 16 Fully parallel (flash) A/D converter architecture

The third disadvantage is that the mismatch in the resistor reference ladder and the unequal input offset voltage of comparators limits the resolution to about 8-bit in CMOS technologies [85]. The mismatches in offset voltage can be represented by V_{be} mismatches in bipolar process and V_T mismatches in CMOS process. Mismatch of V_{be} is 1~2 mV for medium emitter current ($\gg 200\mu\text{A}$) or less with the emitter area larger than $0.2 \times 2.3\mu\text{m}^2$ [81]. The local doping density variation causes a V_T mismatch in a CMOS process, and the standard deviation of length of $1\mu\text{m}$ and width of $9\mu\text{m}$ device mismatch fabricated in $1\mu\text{m}$ process with 20nm thin oxide thickness is about 5 mV [68]. To obtain a 7-bit resolution with a 3.2 V p-p input signal, the comparator should resolve 25 mV. To implement higher resolution, several schemes, such as adding a chopper amplifier

[45] and auto-zero scheme to sample an offset in the capacitor in front of the latch, or inserting a preamplifier [103] in front of the latch, have been developed to decrease DNL of the ADC.

Although the flash topology is very effective for lower resolution converters [31], [36],[97],[58], and has been used widely to implement 8-bit ADCs [30],[32],[67],[100], the increased ADC resolution leads to dramatic growth in the required number of comparators which in turn causes the following detrimental effects:

- Large die size which implies high cost
- Large device count leading to low yield
- Complicated clock and signal distribution with significant capacitive loading (both device and parasitic)
- Large input capacitance requiring high power dissipation in the T/H driving the A/D converter and degrading dynamic linearity
- High power supply noise due to large digital switching current
- Significant errors in threshold voltages caused by comparator input bias current flowing through the resistive reference ladder

2.2 Interpolating Flash A/D Converter

Interpolating converters are proposed to reduce the input capacitance and number of preamplifiers in flash architectures. This kind of A/D converters make use of input amplifiers, as shown in Figure 17. These input amplifiers behave as linear amplifiers near their threshold voltages but are allowed to saturate once their differential inputs become moderately large. As a result, no critical latches need only determine the sign of the amplifier outputs since the differences between the input signal and threshold voltages have been amplified.

Although this approach is often combined with a “folding” architecture, the interpolating architecture has also been used quite successfully by itself. [25], [43], [79], [98].

The main benefit of an interpolating architecture is the reduction in the number of differential pairs attached to the input signal. Such a reduction results in a lower input

capacitance, which is quite high for a flash converter, slightly reduced power dissipation, and a lower number of accurate reference voltages that need to be created.

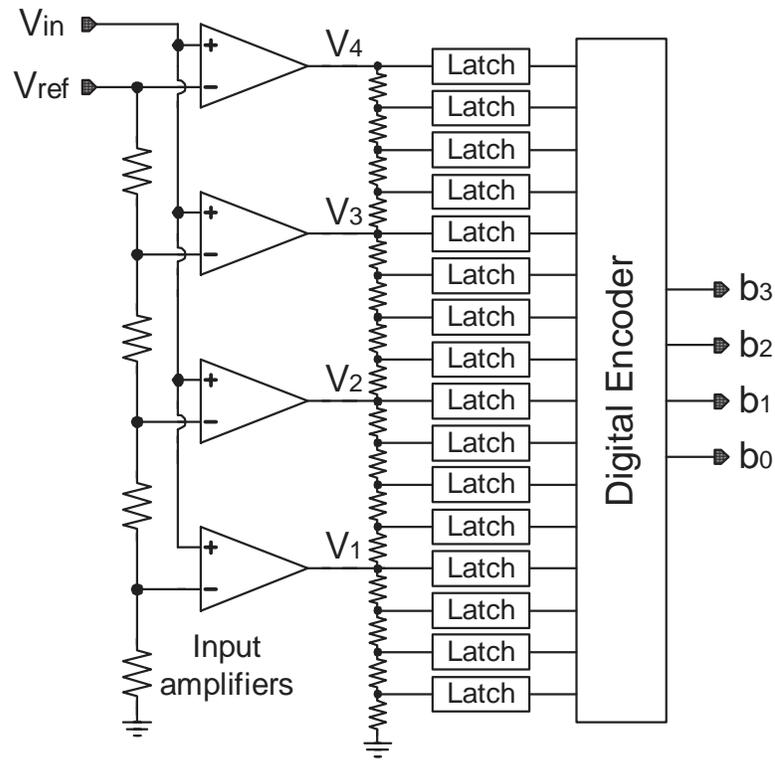


Figure 17 A 4-bit interpolating A/D converter

Circuit techniques other than resistive strings can be used to realize this interpolative approach. In [79], current mirrors were used to interpolate eight times between comparators resulting a 100MHz 8-bit A/D converter realized with a 1.5- μm CMOS process. In another implementation, two stages of interpolation using capacitors to interpolate resulted in a 10-bit 20-MHz A/D converter.

2.3 Subranging and Two-Step A/D Converter

The subrange and two-step architecture[14],[17],[20],[82] was developed to reduce hardware complexity, reduce power dissipation and die area, and also to reduce input capacitance which loads the preceding circuit. The two-step approach is one of the most popular techniques nowadays in CMOS technology to deal with power and area[20].

This topology requires a sample-and-hold operation and has the advantage that the number of comparators can be significantly lower than that of the full flash resulting in a saving of power and area. Conceptually, these types of converter need $2^m + 2^n - 2$ comparator instead of $2^N - 1$ comparators where $N = m + n$. For example, the 10-bit 2-stage (5bit+5bit) subranging converter needs 62 ($2^5 + 2^5 - 2$) comparators instead of 1023 ($2^{10} - 1$) comparators in flash type. However, the conversion in subrange and two-step ADC does not occur instantaneously like a flash ADC, and the input has to be held constant until the sub-quantizer finishes its conversion. Therefore, the sample-and-hold circuit is required for subranging and two-step A/D converters to operate.

Although multi-stage (>2) converters are theoretically possible, these types of ADC must be 2-stage because of the delay in the sub-stage.

2.3.1 Subranging A/D converter

A subrange ADC which consists of 2^N resistors, $2^{N/2} - 1$ comparators, a switch bank, and a S/H [14],[17],[82] is illustrated in Figure 18. In the first step, the S/H samples the input signal and the sampled input is quantized by the first quantizer which consist of $2^{N/2} - 1$ comparator referenced on a resistor string every $2^{N/2}$ taps apart. In the second phase, the previous quantized result (MSB) determines the selected interval of a resistor string for the second quantization where the fine conversion (LSB) has to be made. One with $2^{N/2} - 1$ comparators can perform both the MSB and LSB quantization.

The sample holding capability has been added to the 2nd comparator circuit to increase a conversion speed, especially in CMOS ADC so that the S/H can acquire a new input signal after the MSB has been determined. The extra comparators were added to the 2nd quantizer, and a digital error correction scheme was used to increase conversion linearity [20],[54],[90].

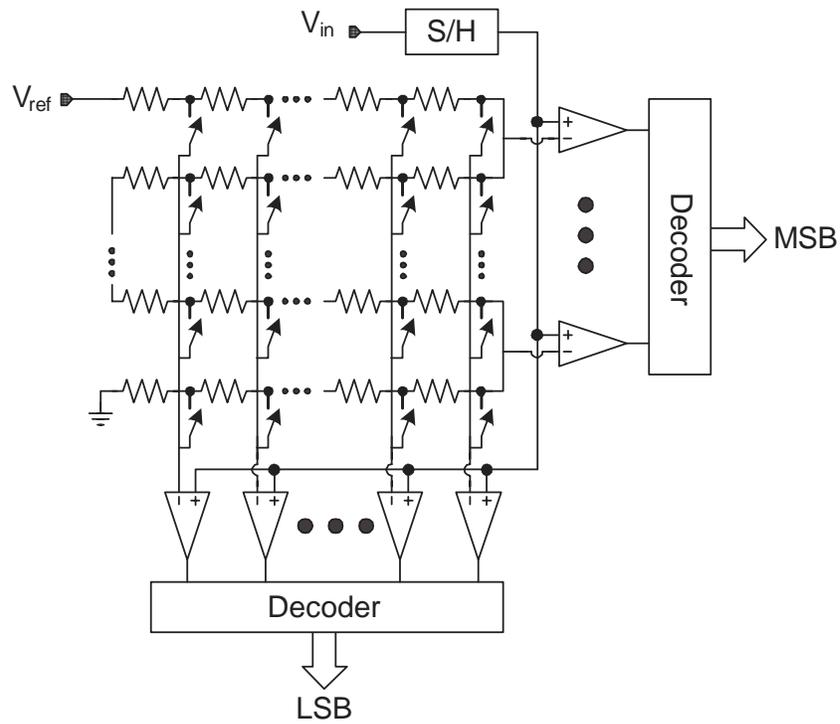


Figure 18 Subranging A/D converter architecture

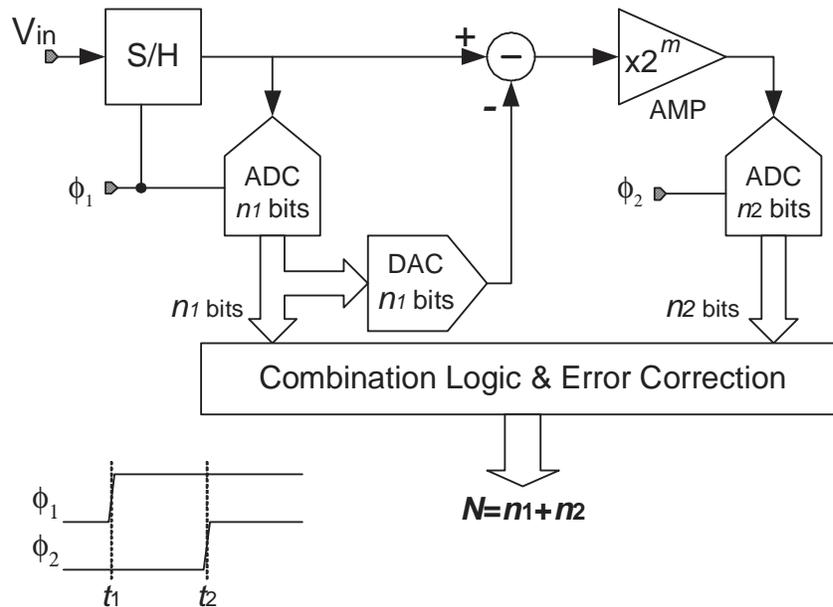


Figure 19 Two-step A/D converter architecture

2.3.2 Two-Step A/D Converter

A two-step converter consists of a sample-and-hold (S/H), two quantizers, DAC, subtractor and gain block as shown in Figure 19. The S/H samples and holds the input signal. This sampled signal from the S/H circuit is quantized by the first coarse quantizer. The first quantizer output selects the DAC output, and the residue is made from the difference between a sampled input signal and DAC output. The residue is amplified and is quantized by a 2nd quantizer. The S/H output is held until the 2nd quantizer finishes the conversion. In a subrange architecture, the second quantizer can only tolerate a $\pm 1/2$ LSB of N -bit offset for the N -bit ADC, even though the precision of the first quantizer can be relaxed by adding some of the extra comparator at both ends of the second quantizer and by adopting an error correction scheme. But in a two-step architecture, both the first and second quantizers can tolerate more than a $\pm 1/2$ LSB of N -bit offset for the N -bit ADC because the residue amplifier can amplify the residue signal to the full input scale. Figure 20 shows accuracy requirements of each block in an 8-bit two-step ADC.

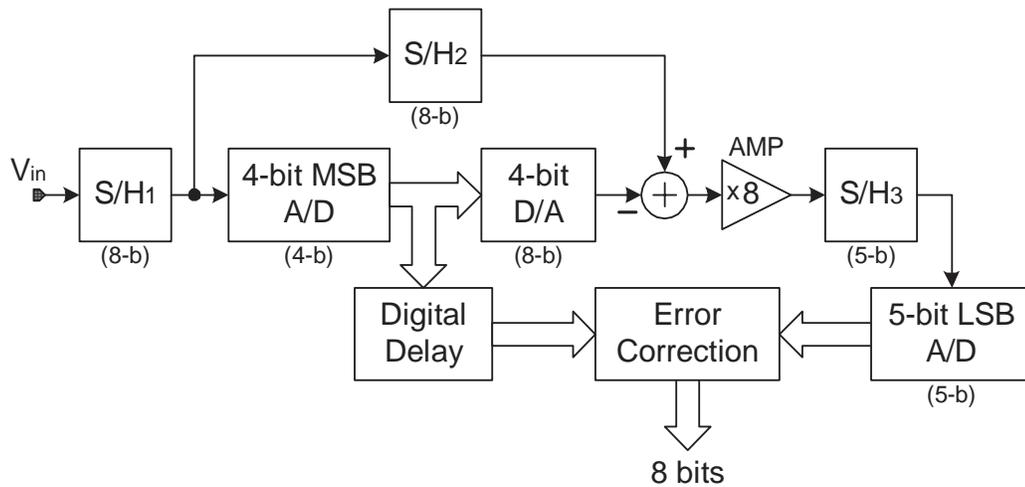


Figure 20 The accuracy requirement of each blocks for an 8-bit two-step ADC [35]

However, there are several disadvantages in the two-step architecture in comparison with the flash architecture. The two-step ADC requires a DAC whose linearity should be

better than N -bits for N -bit ADC, and also requires a subtractor (or a subtractor and residue amplifier), which can be the speed bottleneck. In addition, the conversion time is longer than a flash ADC because the two-step ADC has to wait until the residue signal is settled and quantized. 10-bit resolution has been reported in a two-step converter [16],[17],[61],[83], [71], [90]. Furthermore, the 12-bit two-step ADC has been achieved with the supports of a self-calibration circuit and a trimming feature [37],[38], [47].

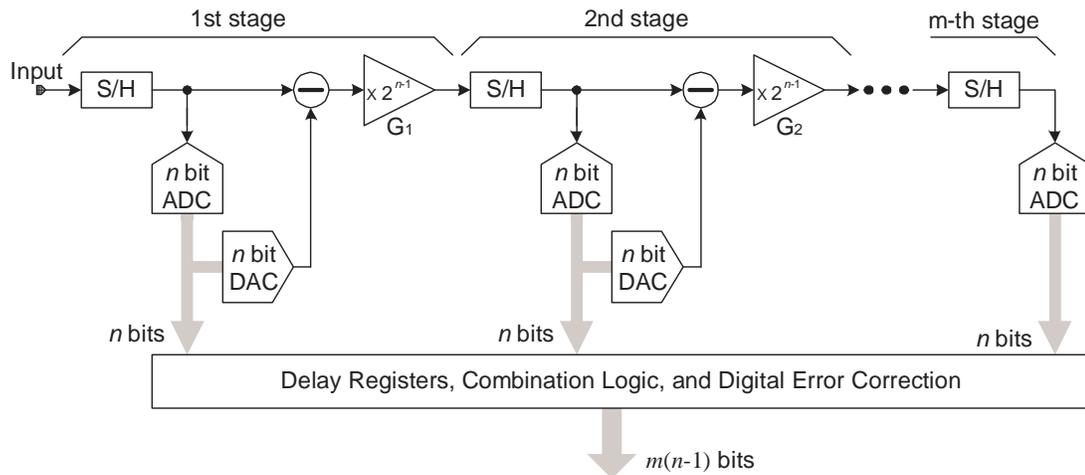


Figure 21 Multi-stage pipeline A/D converter architecture

2.4 Multi-Stage Pipeline A/D Converters

The pipeline A/D architecture as shown in Figure 21 utilizes a sample-and-hold (S/H) in each stage to increase the throughput [5], [7], [12], [48], [49], [52], [55], [56], [57], [87], [88], [89], [94]. Each stage consists of a S/H, an N -bit flash ADC, a reconstruction DAC, a subtractor, and a residue amplifier. Pipelined converters are more commonly used to realize high conversion rates since they provide effective signal bandwidths equal to one-half the sampling rate. Pipelining decouples the conversion rate from the conversion time, allowing power-efficient multiple-flash converters to be implemented with signal bandwidths of 10-100MHz (sample rates of 20-200MHz).

The conversion mechanism is similar to that of subranging conversion in each stage. Now the amplified residue is sampled by the next S/H, instead of being fed to the

following stage. All the N -bit digital outputs emerging from the quantizer are combined as a final code by using the proper number of delay registers, combination logic and digital error correction logic.

Although this operation produces a latency corresponding to the sub-conversion stage before generating a valid output code, the throughput is determined by each stage's conversion time, which is dependant on the reconstruction DAC and residue amplifier settling time. In some applications, i.e., digital communications, latency is not critical[26]. The multi-stage pipeline structure combines the advantages of high throughput by flash converters with the low complexity, power dissipation, and input capacitance of sub-ranging converters. Furthermore, the S/H function can be obtained free if a switched capacitor amplifier is used in a residue amplifier circuit in CMOS technology.

A 10-bit ADC which converts 1 effective bit per stage and consists of nine stages, nine opamps, and 19 comparators has been reported [48]. A power dissipation of 50 mW or less is obtained in 10-bit 20 MHz ADC using the 1 effective bit per stage concept [7], [92]. Pipeline architecture can easily be combined with other technologies, i.e., over-sampling and folding, to implement high speed high resolution ADC [5], [11], [12].

However, the limitation of the low power approach in converting less bit per stage is that the gain accuracy of the first residue amplifier becomes more stringent, because the accuracy requirement is dependent on the remaining number of bits to be converted. For example, in 10-bit ADC using a one effective bit per conversion, the tolerable gain error in the first residue amplifier is less than $\pm 2^{-9}/2$. Since the capacitor matching is about 0.1%, the gain of the first several residue amplifiers may need trimming or calibration.

2.5 Time-Interleaving A/D Converter

The throughput rate can be increased further by using a parallel architecture [3], [13] [40], [76],[101],[102]. A two-channel time-interleaving ADC is shown in Figure 22. All 2 channels operate in a time-interleaving manner, i.e. the first channel samples the input while the other channel is evaluating previously sampled input. Theoretically, the

conversion rate can be increased by the number of parallel paths, at the cost of a linear increase in power and chip area.

This time-interleaving architecture has three major sources of distortion. One error source is that a timing mismatch among the input samplers of each channel can degrade spectrum purity. The timing mismatch among the channels is unavoidable because of asymmetry among the clock distribution in the layout, and also due to mismatch of devices such as clock buffer devices.

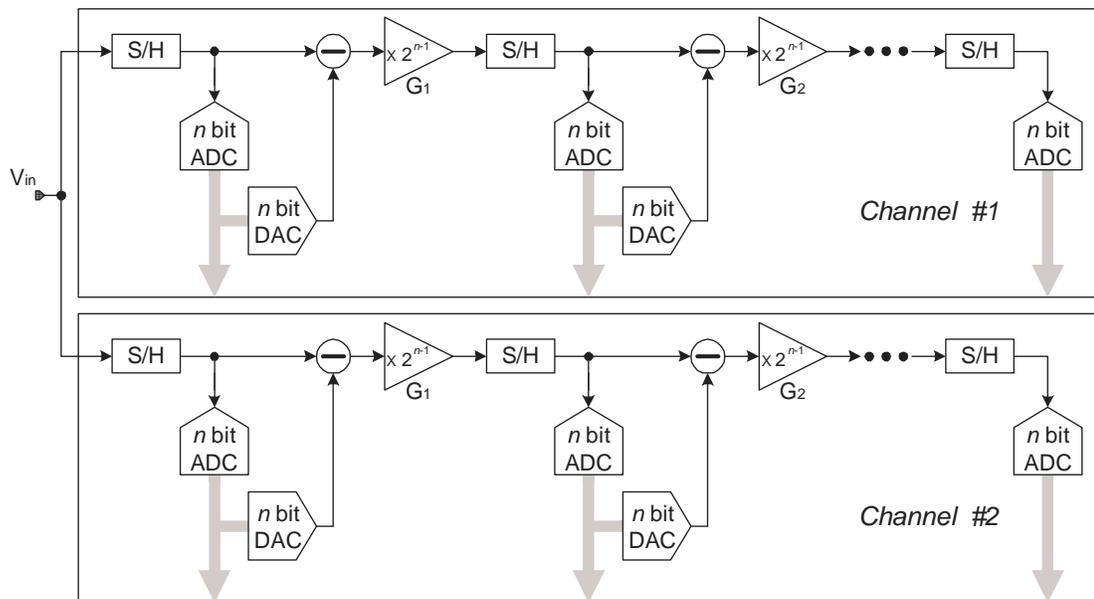


Figure 22 Two-channel time-interleaving pipeline A/D converter

The other sources of distortions are the offset and gain mismatch among these channels. The inter-channel offset mismatch gives rise to fixed pattern noise (distortion). This can be found in the frequency domain as a tone at multiples of f_s / N where N is the number of channel and $n=1, 2, \dots, N$. The inter-channel gain mismatch can generate spurious tones at $m \frac{f_s}{N} \pm f_{in}, m=1, 2, \dots, N-1$. The offset mismatch generates a tone at

$m \frac{f_s}{N}, m = 1, 2, \dots, N-1$. In addition, the first S/H in each channel must have enough tracking bandwidth to acquire an input frequency up to the Nyquist frequency.

Figure 23 shows the maximum achievable signal to noise and distortion ratio (SNDR) from a time interleaving ADC system with gain and time mismatch.

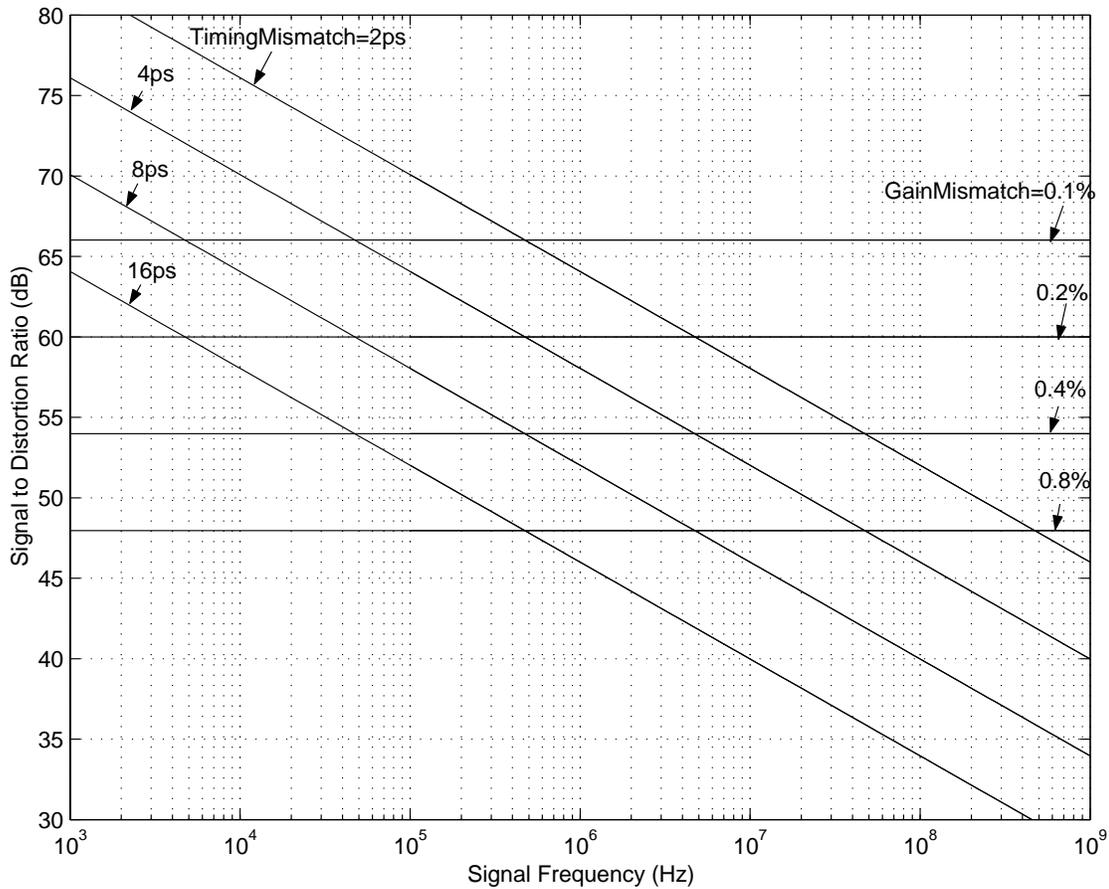


Figure 23 Two-channel time-interleaving A/D converter: maximum achievable SNR with timing mismatch and inter-channel gain mismatch

In comparison with timing mismatch, offset and gain mismatches are easier to compensate or calibration. The effects of timing mismatch can be dramatically reduced by adding a single sample-and-hold circuit in front of each channel. The timing mismatch among the channels is no longer an issue when the parallel pipeline

architecture has a single front-end S/H, because S/H is distributing sampled signals instead of dynamic signals [76],[101]. Since the high speed S/H is the most difficult part in high-speed converter design, adding a single S/H is something against the original motivation of time-interleaving.

2.6 Folding A/D Converter

The number of input amplifiers (preamplifiers) can be reduced through the use of an interpolating architecture. However, the number of latch comparators remains at 2^N for an N -bit converter. This large number of latch comparators can be significantly reduced through the use of a folding architecture [6],[8], [10], [11], [18], [19], [34], [39], [44], [53], [73], [74], [75], [77], [91], [95], [96].

The concept of Folding A/D converter was first introduced by Arbel and Kurz [2] in 1975. The main motivation was the dramatic reduction of the number of comparators required in the design. Different implementations of producing the folding signals have been proposed since then, but the most popular method involves the use of coupled differential pairs (CDPs)[73]. Almost concurrent with the introduction of the CDPs is the concept of resistive interpolation, which produces additional folding signals without requiring additional CDPs. Folding A/D converters with interpolation are often called “folding and interpolating” ADC.

A folding A/D converter is similar in operation to a two-step (or subranging) converter in that a group of LSBs are found separately from a group of MSBs. However, whereas a two-step converter requires an accurate D/A converter to reconstruct analog signal for subtraction, a folding converter determines the LSB set more directly through the use of analog preprocessing while the MSB set is determined at the same time. This arrangement obviates the need for a T/H between the coarse and fine quantizer by forming the residue signal without going through an A/D-D/A combination with its concomitant clock delay.

The folding converter depicted in Figure 24 corresponds to a two-step implementation with a $\log_2 F$ -bit coarse quantizer and a $(N - \log_2 F)$ -bit fine

quantizer, where F is the folding factor, which is the number of periods or folds in the transfer function of the analog folding block. This folding amplifier performs the function of the DAC and the subtraction element from the two-step architecture described previously, but does so in an unlocked manner enabling simultaneous operation of the coarse and fine quantizers. This folding A/D architecture offers low complexity along with potentially high-speed operation.

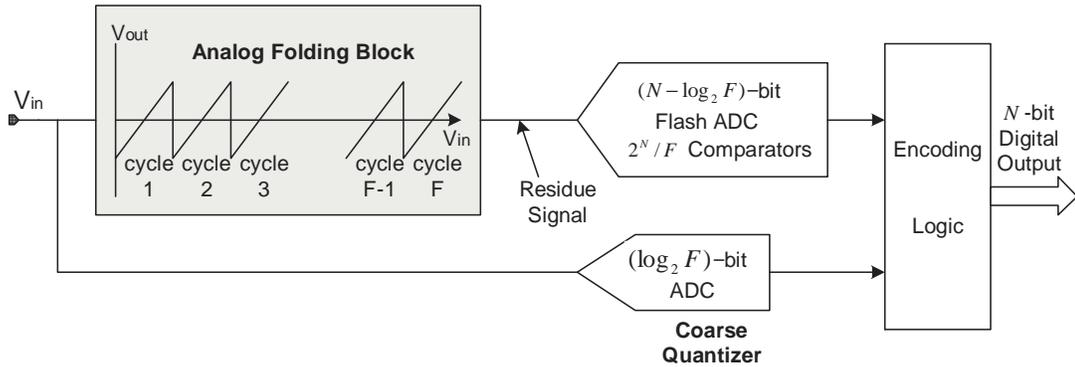


Figure 24 Folding A/D converter topology

The number of transistors in a flash quantizer is proportional to the number of comparators required, $2^N - 1$, where the proportionality constant equals the number of transistors necessary for each comparator (including associated circuitry such as a preamplifiers and logic gates for encoding). Likewise, the number of transistors required for a folding quantizer equals the sum of the transistors comprising the analog folding block, the coarse quantizer, and the fine quantizer (see Figure 24). The analog folding block and the coarse quantizer complexity depend only upon F_F , the number of periods in the folding characteristic, and not upon N , the quantizer resolution, whereas the fine quantizer complexity is proportional to $2^N / F_F$. Therefore, the total complexity of a folding quantizer equals a constant proportional to F_F plus a term proportional to $2^N / F_F$.

2.7 Structure Comparisons

Table 2 includes a summary comparison among the architectures described above.

TABLE 2 Comparison among several high-speed converter architectures

Architecture	Advantages	Disadvantages
Full-parallel (Flash)	Very fast Basically monotonic No D/A required	Very high transistor count Very high power dissipation Resolution limited by input range and transistor mismatch High input capacitance (limit speed)
Subrange/ Two-step	Moderate transistor count Error correction possible Low input capacitance	Moderate sample rate Moderate latency
Interpolating	High speed Basically monotonic No D/A required Lower input capacitance in comparison with Flash ADCs	Very high power dissipation Resolution limited by input range and transistor mismatch
Pipelined multi-stage	High throughput Error correction possible Low input capacitance	Multiple T/H circuits required Latency depends on number of stages
Time- Interleaving	Very high throughput Error correction possible	Gain, offset and timing mismatch introduce distortions
Folding	High speed Folding amplifier replace the D/A and subtractor Lower transistor count Low input capacitance	Resolution limited Input bandwidth limited due to the frequency multiplication effect “Piecewise Linear” folding ADC is not used

CHAPTER III

FOLDING AND INTERPOLATING A/D CONVERTER

Folding and interpolating A/D converters have been shown to be an effective means of digitization of high bandwidth signals at intermediate resolution [73],[75]. In comparison with fully parallel (flash) architectures; they require fewer comparators while maintaining the advantages of high speed and low latency. Due to the reduced number of comparators required, converter architectures employing folding and interpolating are good architectures employing folding and interpolating are good candidates for low-power implementations of medium resolution (6 to 10b), high speed (tens or hundreds MSample/s) ADCs. The reduction in the number of comparators is obtained by the use of folding amplifiers, or “folders,” while interpolation is used to keep the number of such amplifiers small. Although such converters were initially realized in bipolar technologies [11],[73],[74],[75], a number of CMOS and BiCMOS implementations have been reported[6],[8],[10],[18],[19],[62],[91],[96].

3.1 Concept of Folding

As described in chapter II, a two-step A/D converter gains efficiency by partitioning an N -bit quantization into two lower-resolution quantizations. In such a converter (Figure 25a) an n_1 -bit coarse quantizer digitizes the input signal with low resolution, and applies the resultant codeword to reconstruction DAC. The analog output of the DAC is subtracted from the original input to form a residue signal (Figure 25b), which is quantized by an n_2 -bit quantizer. The advantage of this approach arises because the combined complexity of the n_1 -bit coarse quantizer and the n_2 -bit fine quantizer can be far less than the complexity of a single N -bit quantizer.

The object of a folding A/D converter is to form the residue signal with simple analog circuits thereby obviating the need for the coarse quantizer, DAC, and subtractor components of Figure 25a. In such an implementation (Figure 26), the low dynamic-range residue signal generated by the analog folding circuit directly drives the fine quantizer. Because of the periodic nature the residue signal; however, the digitized

output from the fine quantizer is ambiguous, and a coarse quantizer is still necessary to ascertain in which period of the folding circuits transfer characteristic the quantizer input signal lies. The input-output characteristic of the analog folding circuit can be parameterized by the number of piece-wise linear segments, or *folds*, which it contains.

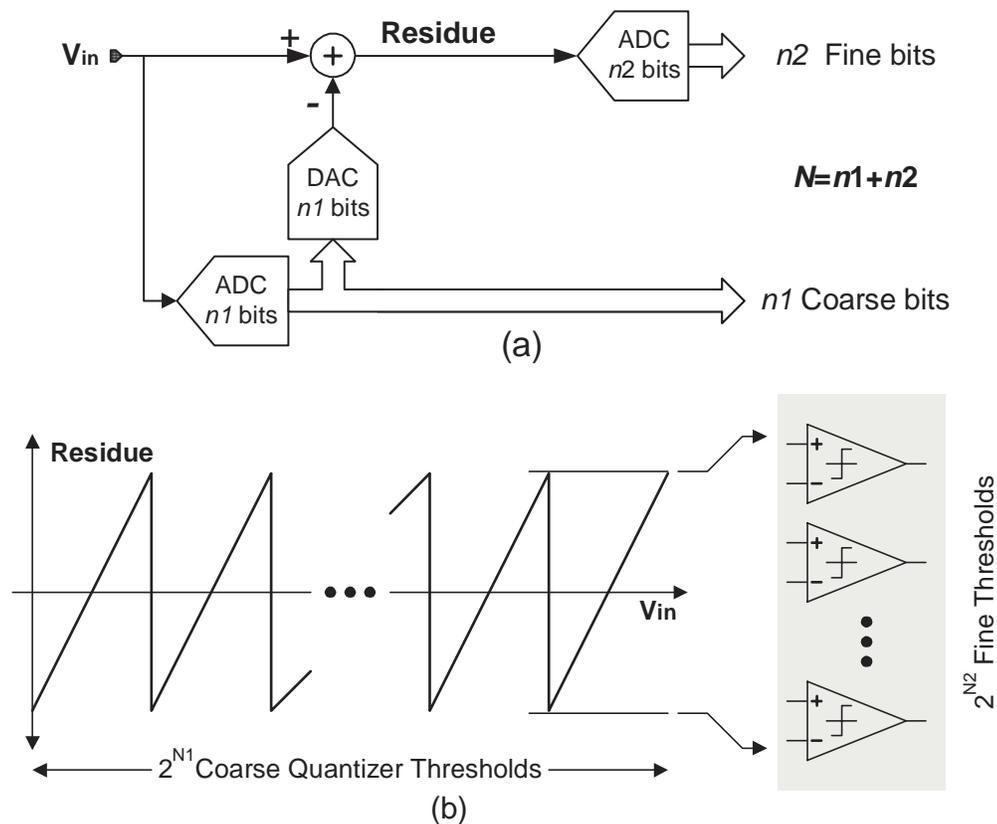


Figure 25 Architecture of two-step A/D converter (a) block diagram (b) basic principle

The idea of folding is similar to a two-step ADC: both structures utilize two lower resolution quantizers to implement one higher resolution ADC. However, folding ADCs use analog preprocessing to generate “residue” at the same time instant when the MSBs from the coarse quantizer are produced. Also the coarse quantizer determines where the input lies for the folding amplifier (analog preprocessing). The total resolution of the folding ADC is $N_B = n_{MSB} + n_{LSB}$, where n_{MSB} and n_{LSB} are the numbers of bits resolved in the coarse and fine quantizers, respectively.

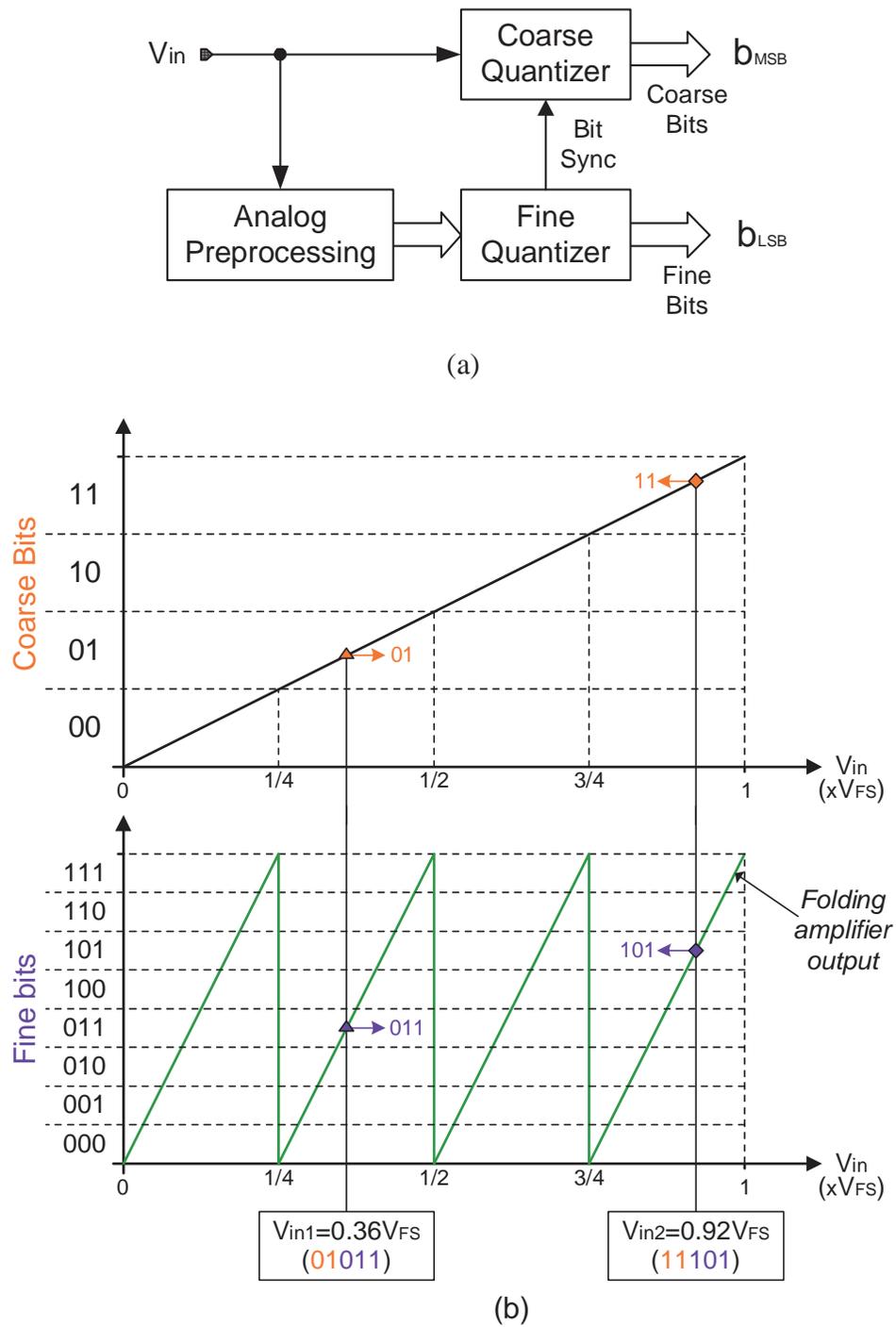


Figure 26 A 5-bit example: 2 coarse bits plus 3 fine bits (a) block diagram (b) generation of coarse and fine bits

A 5-bit ADC (Figure 26) is used as an example to explain the basic idea of folding and interpolating ADCs. Figure 27(a) shows the saw-tooth shaped transfer characteristic of the $4\times$ folding amplifier. The output repeated four times when the input voltage sweeps through the full ADC range. Thus a comparator in a folding ADC will detect four zero crossing points while a comparator in the flash ADC will detect only one. In this 5-bit folding ADC, a total of 10 (3 for coarse quantizer and 7 for fine quantizer) comparators are needed while a 5-bit full-flash ADC needs 31 comparators. Generally speaking, a folding ADC reuses comparators so that the total number of comparators can be reduced by a folding factor (F_F), i.e., $F_F=4$ in Figure 26. Table-3 compares the number of comparators in flash and folding ADCs. As the resolution increases, the number of comparators in a folding ADC is much smaller than that of a full flash ADC.

TABLE 3 Number of comparators comparison between flash and folding ADC

	5-bit	6-bit	7-bit	8-bit	9-bit	10-bit
Full Flash	31	63	127	255	511	1023
Folding (2-bit coarse)	10	18	34	66	130	258
Folding (3-bit coarse)	10	14	22	38	70	134
Folding (4-bit coarse)	16	18	22	30	46	78

For the 5-bit folding ADC example shown in Figure 26, the whole input range of ADC is divided into four (2^2) regions, and a 2-bit coarse quantizer can determine one of the four regions where the input voltage falls into. In general, for $F_F = 2^{n_{MSB}}$, a n_{MSB} -bit coarse quantizer is required. At the same time, the “residue” generated by the folding amplifier is digitized by a 3-bit (n_{LSB}) fine quantizer. Thus, the total number of comparators of this folding A/D converter is 10 (three for the coarse and seven for the fine quantizer), while a 5-bit full-flash ADC need 31 comparators. Although both F&I ADC and two-step ADC have similar principle, folding ADCs exhibits smaller latency. In a F&I ADC, fine and coarse information are generated simultaneously, and

independent of each other, therefore this structure does not strictly require a S/H and a DAC.

3.2 Linear Folding

Folding A/D converters based on the architecture of Figure 26 would be possible if simple analog circuits could easily realize the piece-wise linear input-output characteristics indicated (Figure 27a). The saw-tooth shaped transfer characteristic is not easy to implement due to its discontinuity. At these discontinued points the slew rate should be infinite, thus a triangular characteristic (Figure 27b) is preferred.

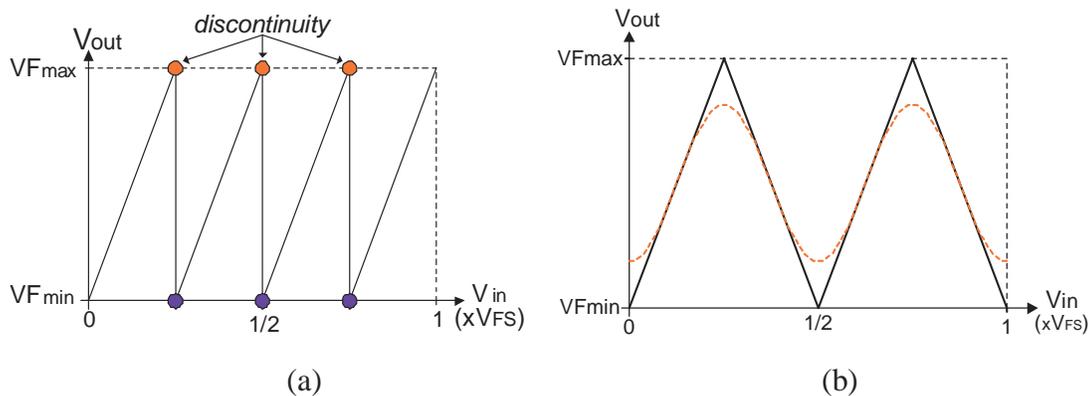


Figure 27 Sawtooth, triangular shaped and pseudo-sinusoidal transfer characteristics (a) sawtooth (b) triangular

Several implementations have been developed which approximate the triangle wave folding characteristic of Figure 27b. Some of them are based on the rectifier characteristic of diodes [24], [74] and others are based on current mirrors [50].

3.2.1 Diode Based Linear Folding [74]

The basic configuration of a diode based $4\times$ folding amplifier and its I - V transfer characteristics is depicted in Figure 28. The input signal is in current form, which is compared with the four reference currents I . The collectors of the odd-numbered transistors of the common base stages $Q1$ - $Q4$ are interconnected, and so too are the even-numbered transistors. If the input current is equal to zero, currents I will flow through

3.2.2 Current-Mirror Based Folding Amplifier[50]

Current mirror can be used to implement piecewise linear transfer characteristic of the folding amplifier. The idea is to use basic building block with “S” shaped current-to-current transfer characteristics to construct triangular shaped folding waveform. Schematic of the basic building block is shown in Figure 29a and its transfer curve is shown in Figure 29b.

The parameters of the “S” shaped transfer curve shown in Figure 29b can be determined by bias currents and transistor sizes. Their relationship is described by Eq.(3.1a-d).

$$I_{E1} = I_{B1} \quad (3.1a)$$

$$I_{E2} = I_{B2} \frac{P_4}{P_3} - I_{B3} \quad (3.1b)$$

$$I_{E3} = I_{B2} \frac{P_1}{P_2} - I_{B1} \quad (3.1c)$$

$$I_{E4} = I_{B3} \quad (3.1d)$$

where $P_i, i = 1..4$ is the width/length ratio of transistors comprising the current mirrors.

The basic folding block is a current limiting amplifier. Its gain can be adjusted by changing the gain of the two current mirrors, and two transition points are determined by gain and bias currents.

Figure 30 shows how the current mode folding amplifier is constructed by connecting basic folding blocks in parallel. The current copier can be implemented with a PMOS current mirror, which has one input and multiple outputs. By connecting several currents together, a current adder is naturally realized.

Although simple current mirrors are shown in Figure 29 and Figure 30, cascode current mirrors may be used in practical designs. In very low voltage design, i.e. when VDD is less than 1.2V, one can use simple current mirrors to build folding amplifier. However, the length of transistor should be large to obtain adequate accuracy. The disadvantage of using long channel transistor simple current mirror is low speed.

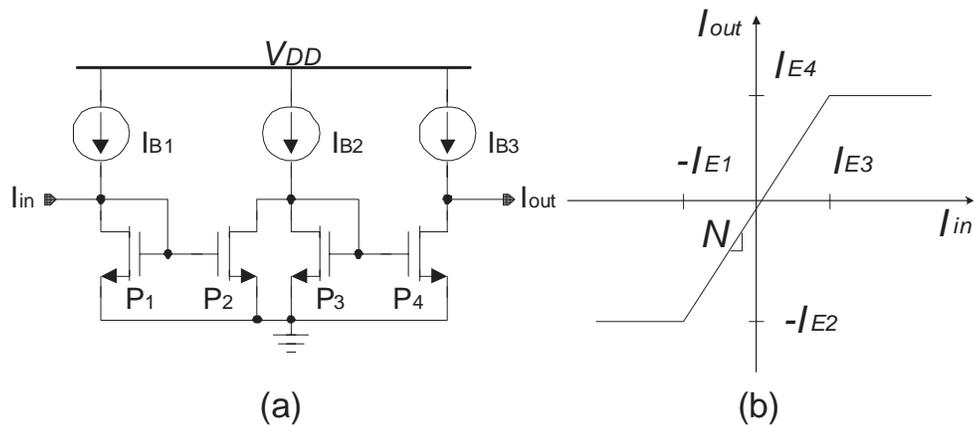


Figure 29 Basic building block of the current mirror based folding amplifier (a) schematic (b) transfer characteristic

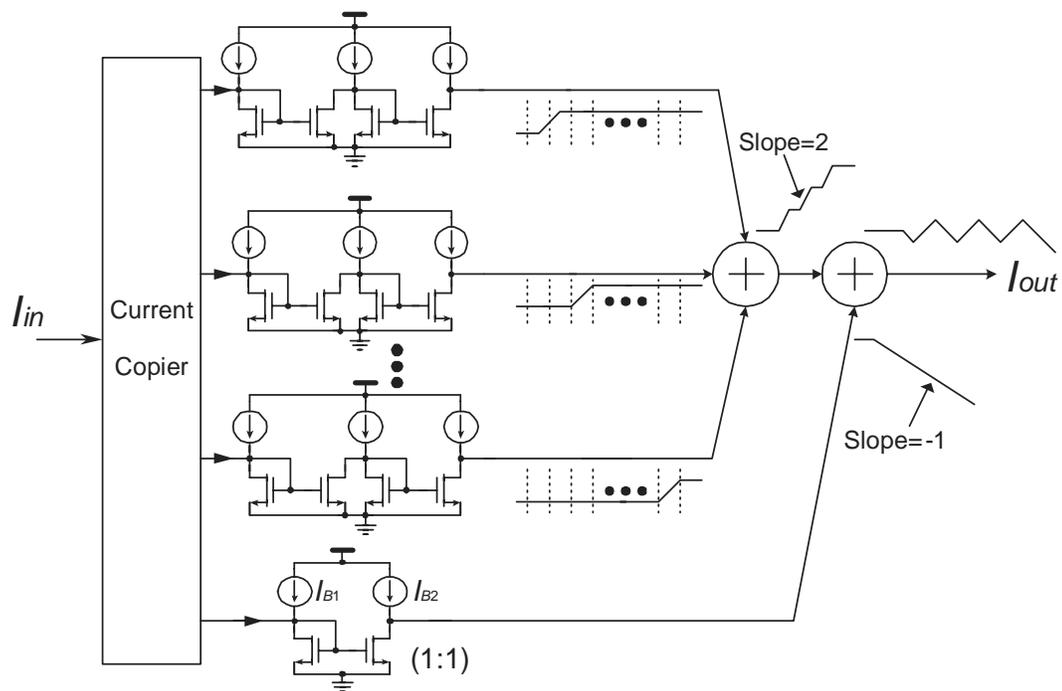


Figure 30 Topology of the current mirror based current mode folding amplifier

If cascode current mirrors are used, this implementation can approximate triangular-shaped folding transfer characteristics very well. The problem is the speed is limited due to the switch “on” and “off” of current mirrors. Usually current mirrors are thought to

have large bandwidth, but that means small signal bandwidth under a large bias current. In the folding amplifier case, the current mirrors deal with large signals, thus the bias condition of each current mirror can be quite different depends on the input signal. In one word, to implement the nonlinear folding transfer characteristic, current mirrors and transistors comprising them constantly change between “OFF” and “ON” operating states. This will slow down the folding amplifier response.

Generally, circuits with discontinuous input-output characteristics are difficult to realize and are not amenable to high-speed applications. Therefore, folding converters which do not rely upon piece-wise linear folding functions prevail. Folding amplifiers with a “pseudo-sinusoidal” transfer characteristic are much easier to implement than those with a piecewise linear triangular shape transfer characteristic. With this nonlinear transfer characteristic, direct digitization of magnitude of folding amplifier outputs prove to be impractical.

3.3 Sinusoidal Folding

Folding amplifiers built with differential pairs [2] have input-output transfer characteristics resembling a sinusoidal signal. Strictly speaking, they are not sinusoidal, the actual shape depends on the transistors used: BJT or CMOS.

Folding amplifier shown in Figure 31(a) relies on the hyperbolic tangent transfer function of a voltage driven bipolar differential pair to approximate a sinusoid. An input signal, gradually increasing from a low to a high value, will first pass the amplifier threshold on the left, which at that moment will make the output transition from high to low. Further increasing the input signal will, at some point, bring it close to the reference point of the second amplifier, and as this amplifier has reversed polarity, it will cause the output to go from low to high. At the moment the input signal passes the amplifier on the right, the comparator will again change from high to low. The above described behavior is depicted by Figure 31(b). The output voltage will go up, down, and then up again when a rising input signal is applied, thus showing the *folded* nature of this technique.

By selecting the voltage separation between the reference voltages $V_{REF1}-V_{REF5}$ appropriately, a “sinusoidal” folding transfer characteristics can be obtained. The circuit

of Figure 31(a) suffers some important drawbacks. The input is single-ended so, bias currents flowing into the folding circuit's differential pairs will perturb the apparent reference voltages thereby distorting the desired shape of the sinusoid. Additionally, the output current from the folding circuit consists of a large common-mode component with only a small differential component. Lastly, if many folds are desired, mandating many differential pairs in the folding circuit, then the capacitive loading on the output node becomes large adversely affecting settling time.

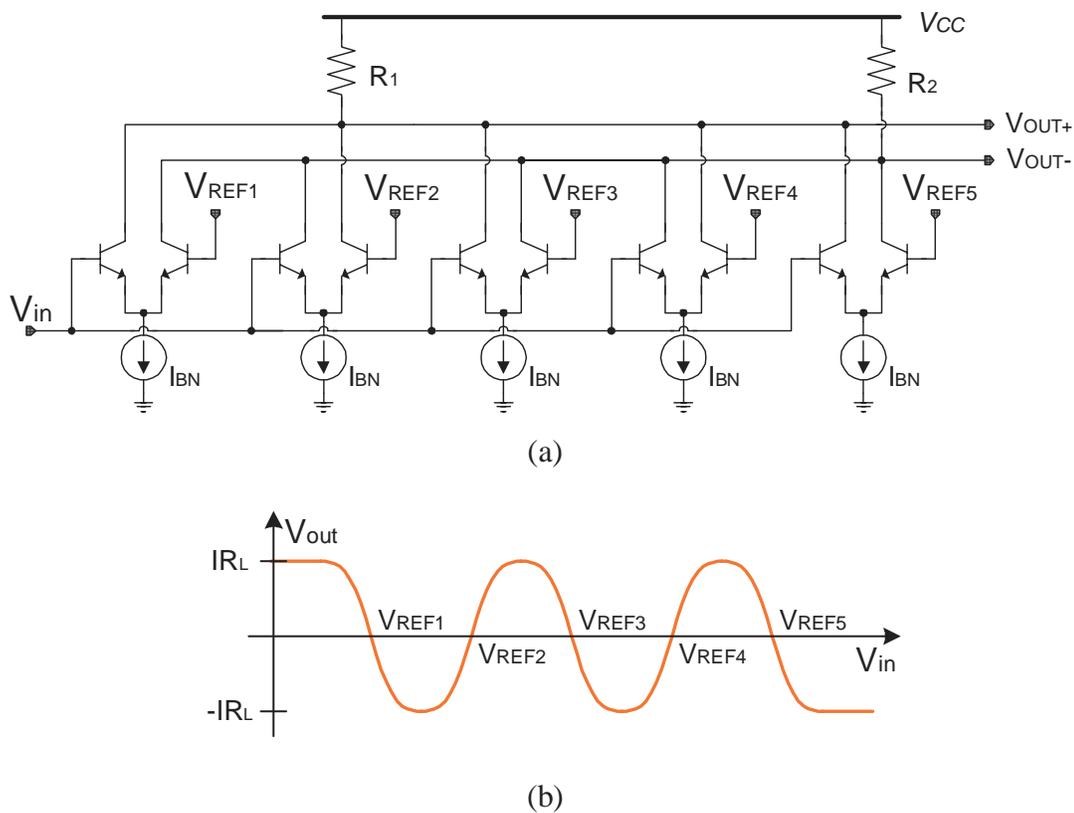


Figure 31 Folding amplifier based upon hyperbolic tangent transfer function of voltage driven differential pairs (a) schematic, (b) transfer characteristics

Some of these drawbacks are overcome by the circuit shown in Figure 32 [73], [75], which uses a wired-OR configuration at the differential pair outputs to reduce the common-mode output signal and to provide buffering. This circuit still suffers from the

threshold perturbing effects of a single-ended reference scheme. To eliminate this error source, fully differential structure must be adopted.

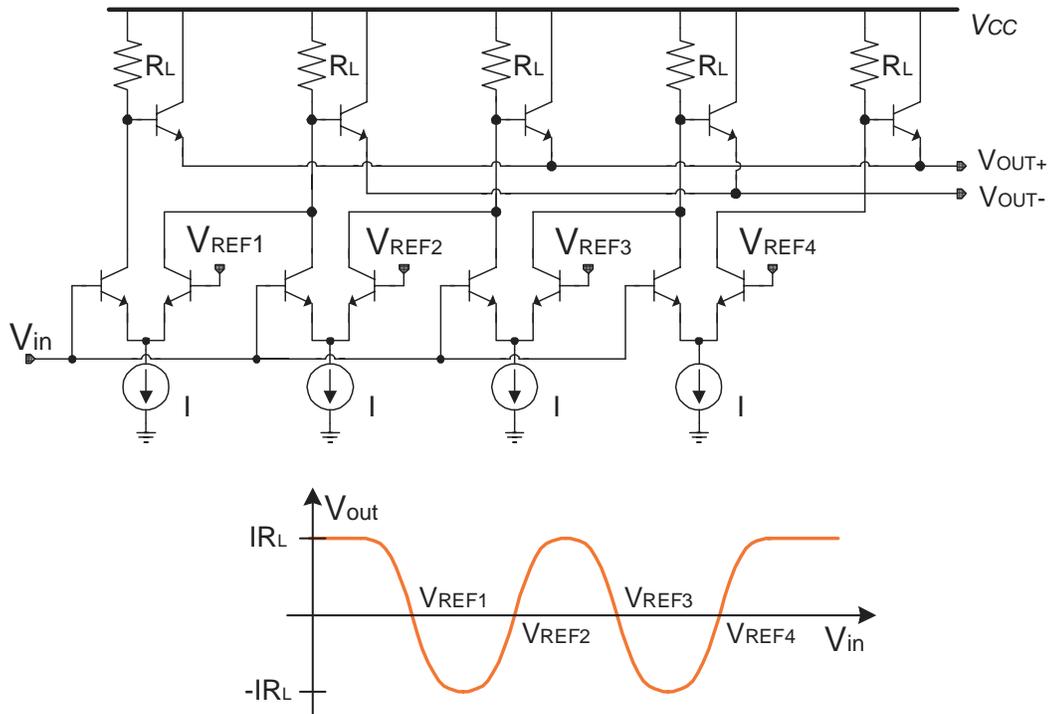


Figure 32 Folding amplifier based on wired-OR interconnection

3.4 Double Folding

It is noted that the tops of the folding signals of Figure 31&32 are rounded. This need not to be a problem if we consider Figure 33. Double folding is proposed to circumvent the folding amplifier linearity problem [74]. Here, in a single folding system (upper part), the full scale input of the ADC is divided into 4 segments (1-4) and each segment corresponds to full range of the 3-bit quantizer, thus a strict piece-wise linear transfer characteristic is desired. In a double folding system, the ADC full input range is divided into 8 segments, each of the 2 quantizers handle 4 segments, i.e. quantizer (A) digitize 1A-4A while segments 1B-4B belong to quantizer (B). The selection logic block always chooses the output of the quantizer which folding amplifier is in linear region. If one folding signal is in its nonlinear region, the other is in its linear region and vice versa.

Thus, instead of needing one good folding signal with the detection of 8 levels, which a 3-bit quantizer demands, we also can take two folding signals with the detection of 4 levels for each folding signal.

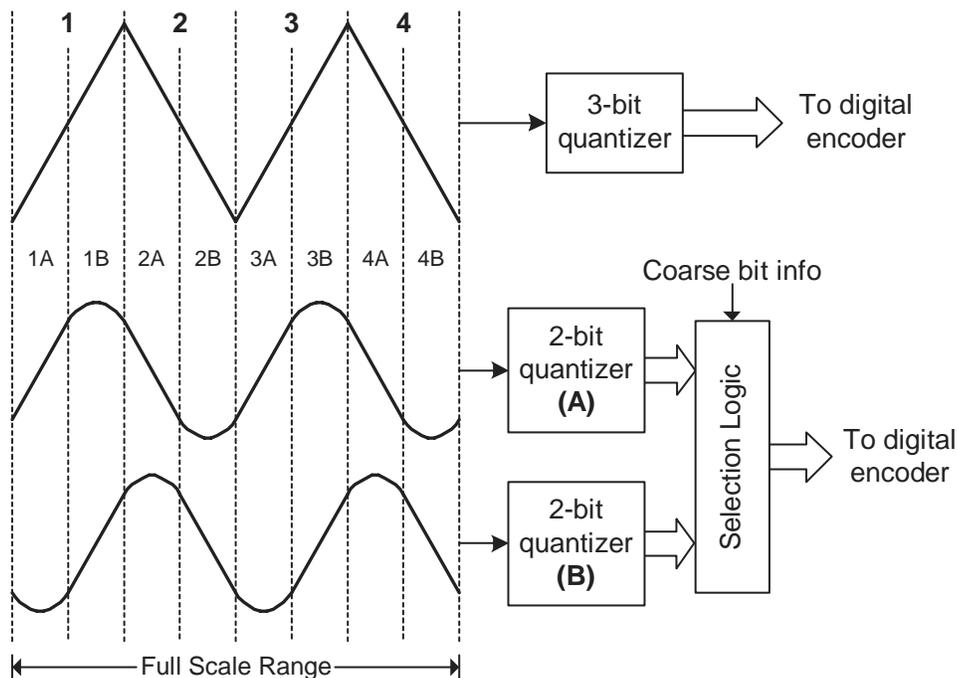


Figure 33 Comparison of single and double folding system

The linear range requirement on the folding amplifiers can be reduced by half by employing the double folding scheme. For the 5-bit ADC shown in Figure 26, in the single folding case, the folding amplifier linearity range should cover 2^3 quantization steps (LSB). While in the double folding case, each folding amplifier linearity range should cover 2^2 quantization steps (LSB).

This reasoning can be expanded up to 4 folding signals with the detection of only one level per signal. Again we consider the fine quantizer shown in Figure 26, if we use 4 folding amplifiers, what is the linearity requirement on each quantizer? Clearly, the resolution of quantizers following these folding amplifiers is 1-bit, the quantizer is degenerated to a single comparator.

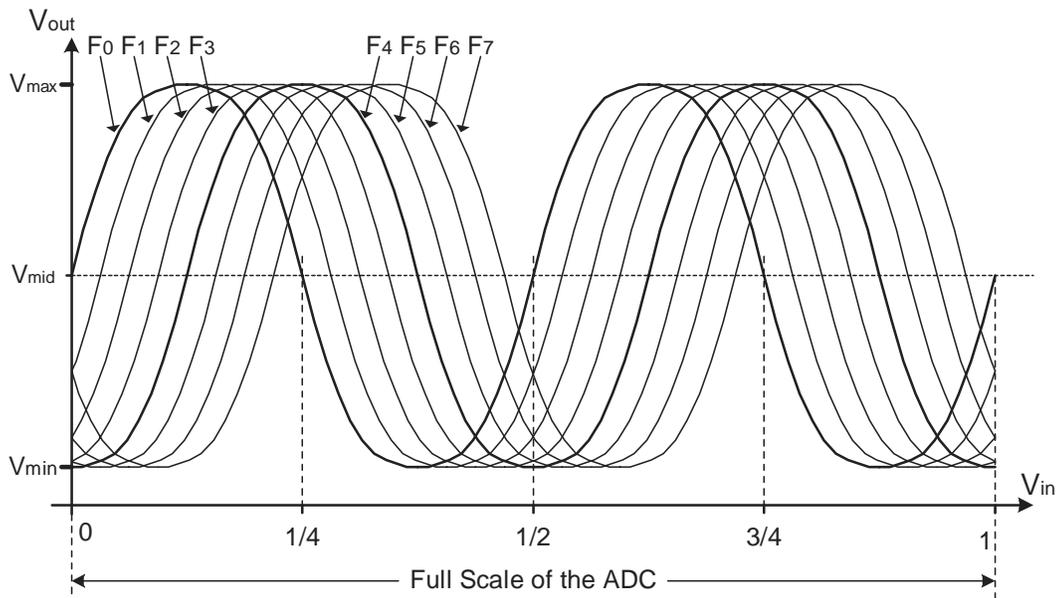


Figure 34 8 Folding waveforms generate all 32 zero crossings of a 5 bit ADC

Figure 34 shows all the 8 waveforms of an 8-folding system. These eight folding waveforms generate 32 (5-bit) equidistant zero-crossing points along the full ADC input range. Thus, linearity of each folding waveform is no longer critical, only the positions of zero crossing points are of interest, which affect the linearity of the folding ADC. For the folding ADC example shown in Figure 34, the number of zero crossing detection comparators is 8(fine quantizer) plus 3(coarse quantizer). A 5-bit full-flash will need 31 comparators. The problem is now that the generation of 8 folding signals with 8*5 differential pairs is as much hardware as a full-flash converter. Interpolation can be used to circumvent this dilemma.

3.5 Interpolation

A straightforward approach to generate all 8 folding waveforms in Figure 35(a) is to use 8 folding amplifiers. However, such a “pure” folding scheme is rarely adopted in practical ADC implementations because of cost consideration (area and power). Instead, interpolation is employed to generate large quantity of folding waveforms. Folding A/D

converters utilizing interpolation are called “folding and interpolating ADC” (F&I ADC).

Figure 35(b) shows the principle of interpolation. Three folding amplifiers generate 3 folding signals with a mutual offset equal to 4 times of the offset between two neighboring folding amplifiers in Figure 35(a). In the configuration of Figure 35(b), 6 additional folding signals are generated by a resistor ladder from the existing three, resulting in a total of 8 folding signals.

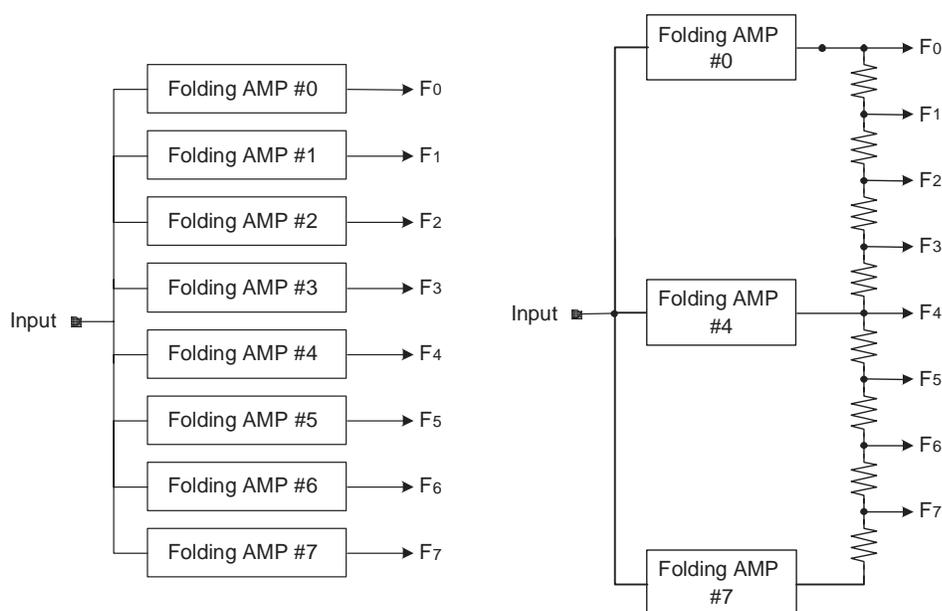


Figure 35 Different ways to generate multiple folding waveforms (a) pure folding (b) folding plus interpolation

3.5.1 Voltage Interpolation

The most common interpolation is based on resistive voltage division (Figure 36). The linear portion of two interpolating folding waveforms must extend to the zero crossing point of each other to avoid error in the interpolated folding waveforms. The interpolatable region is half of the linear region of folding waveforms. A special case is 2x interpolation, where nonlinearity does not affect the accuracy of the interpolated zero crossing point, so long the interpolating folding waveforms possess symmetry and are

identical in shape. In case of well-behaved nonlinearity, non-uniform interpolation can be utilized to compensate for the nonlinearity. In extreme case, the entire folding waveforms can be generated from two I and Q phase sinusoidal folding characteristics. Although interpolation is a method to generate extra folding waveforms with lower cost, large extent of interpolation suffers uneven delay in the interpolation network (interpolation delay variation)[73].

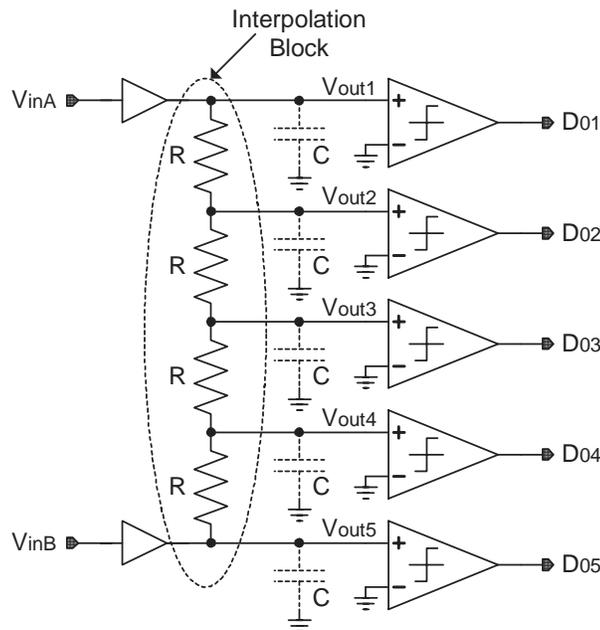


Figure 36 Voltage mode interpolation

3.5.2 Current Interpolation

When signal is in the form of current, impedance in the signal path is small, voltage swings are limited, and speed is fast. Therefore current mode interpolation is suitable for low voltage and high-speed applications. The interpolating currents are split with cascode current mirrors into various fractions proportional to the current mirror size and are summed to form the fine current divisions (Figure 37). [19]. The current offsets from the interpolating devices (i.e., the current mirrors) cause error in the interpolated zero crossing points. With MOSFET current mirrors, the major source of current offset is the

random variation in threshold voltage. A large channel length is favorable because it yields a larger effective gate voltage, which makes the threshold offset less significant referred to the signal input.

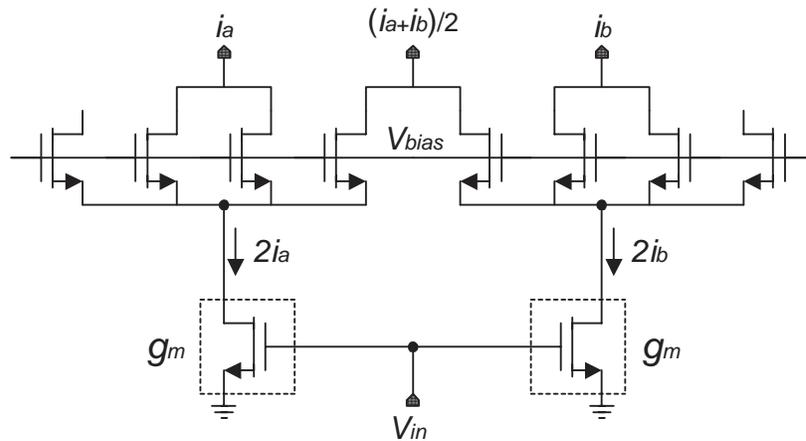


Figure 37 Current mode interpolation based on current splitting

Current mirrors can be used to build current mode interpolation block, which will be described in chapter 5. In comparison with voltage mode interpolation, current mode interpolation circuits' delay variation is much smaller.

3.6 Digital Encoder

The code generated by the comparator bank in a flash A/D converter is called "thermometer code". Due to the folding and interpolating, the output code comparator bank in a folding A/D converter is not thermometer code but something similar. It's called cyclical thermometer code. Cyclical thermometer code can be easily converted to gray code through pure Exclusive-Or operation (XOR). Figure 38 shows the schematic of an encoder which convert 31-bit cyclical thermometer code to 5-bit Gray code. Gray code can be easily converted to binary code also through pure XOR operation (Figure 39).

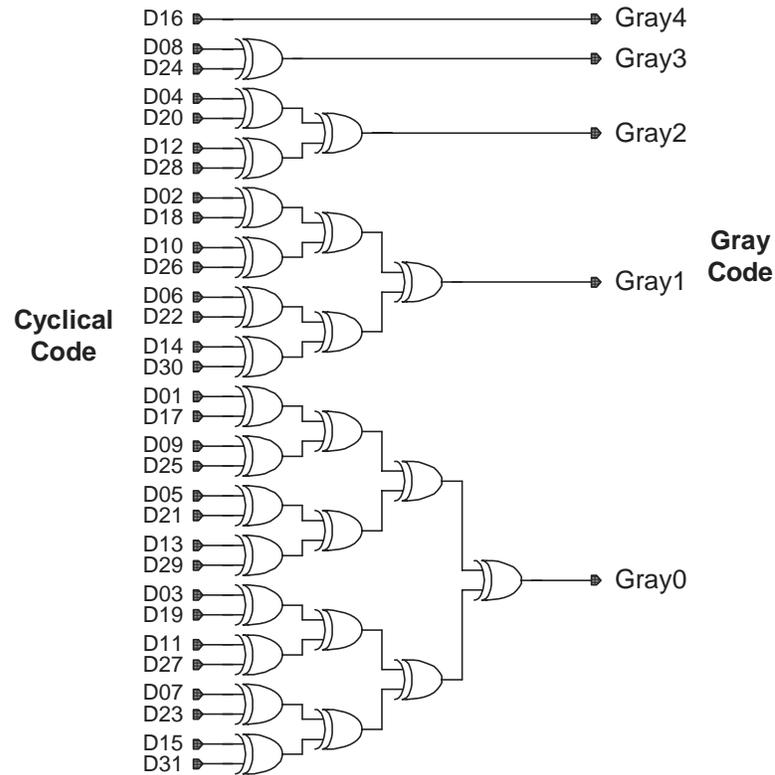


Figure 38 Cyclical to gray code conversion

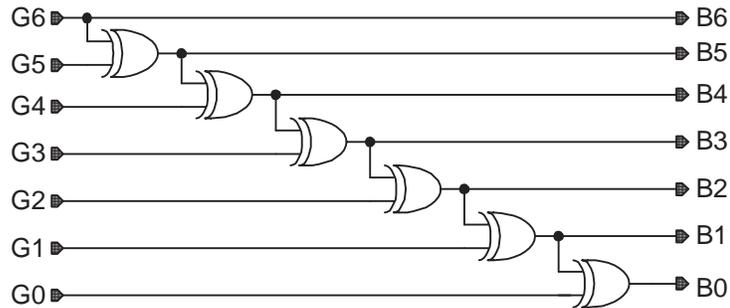


Figure 39 Gray to binary code conversion

The encoder shown in Figure 38 and Figure 39 can be represented by logic expressions (3.2a-e) and (3.3a-g), respectively.

$$G_0 = D_{01} \oplus D_{03} \oplus D_{05} \oplus D_{07} \oplus D_{09} \oplus \dots \oplus D_{27} \oplus D_{29} \oplus D_{31} \quad (3.2a)$$

$$G_1 = D_{02} \oplus D_{06} \oplus D_{10} \oplus D_{14} \oplus D_{18} \oplus D_{22} \oplus D_{26} \oplus D_{30} \quad (3.2b)$$

$$G_2 = D_{04} \oplus D_{12} \oplus D_{20} \oplus D_{28} \quad (3.2c)$$

$$G_3 = D_{08} \oplus D_{24} \quad (3.2d)$$

$$G_4 = D_{16} \quad (3.2e)$$

Once the 31-bit cyclical thermometer code is converted to 5-bit gray code, the 5-bit fine quantizer outputs can be combined with 2-bit coarse quantizer outputs to produce whole 7 bits of the F&I ADC. If the 2 coarse bits are generated in gray code as G_5 and G_6 , 7-bit gray code can be easily converted to 7-bit binary code. Their relationship is

$$B_0 = G_0 \oplus G_1 \oplus G_2 \oplus G_3 \oplus G_4 \oplus G_5 \oplus G_6 \quad (3.3a)$$

$$B_1 = G_1 \oplus G_2 \oplus G_3 \oplus G_4 \oplus G_5 \oplus G_6 \quad (3.3b)$$

$$B_2 = G_2 \oplus G_3 \oplus G_4 \oplus G_5 \oplus G_6 \quad (3.3c)$$

$$B_3 = G_3 \oplus G_4 \oplus G_5 \oplus G_6 \quad (3.3d)$$

$$B_4 = G_4 \oplus G_5 \oplus G_6 \quad (3.3e)$$

$$B_5 = G_5 \oplus G_6 \quad (3.3f)$$

$$B_6 = G_6 \quad (3.3g)$$

3.7 Folding and Interpolating ADC: An Example

We have talked about all unique blocks in a folding and interpolating ADC, such as folding amplifier, interpolator, and digital encoder. Comparators are also important, but they are not unique in a folding and interpolating ADC so we don't elaborate it here.

To illustrate the system structure of a F&I ADC, a simple 5-bit F&I ADC system is shown in Figure 40. The 5-bit F&I ADC includes two $4\times$ interpolator, interpolation factor is 4. Resolution of such a F&I ADC is related to the folding factor (F_F) and interpolation factor (F_I) by

$$N_B = \log_2(m \cdot F_F \cdot F_I) \quad (3.4)$$

where m is the number of folding amplifiers. Sometimes it's called "number of primary folding waveforms". For the F&I ADC shown in Figure 40, $m=2, F_F=4, F_I=4$.

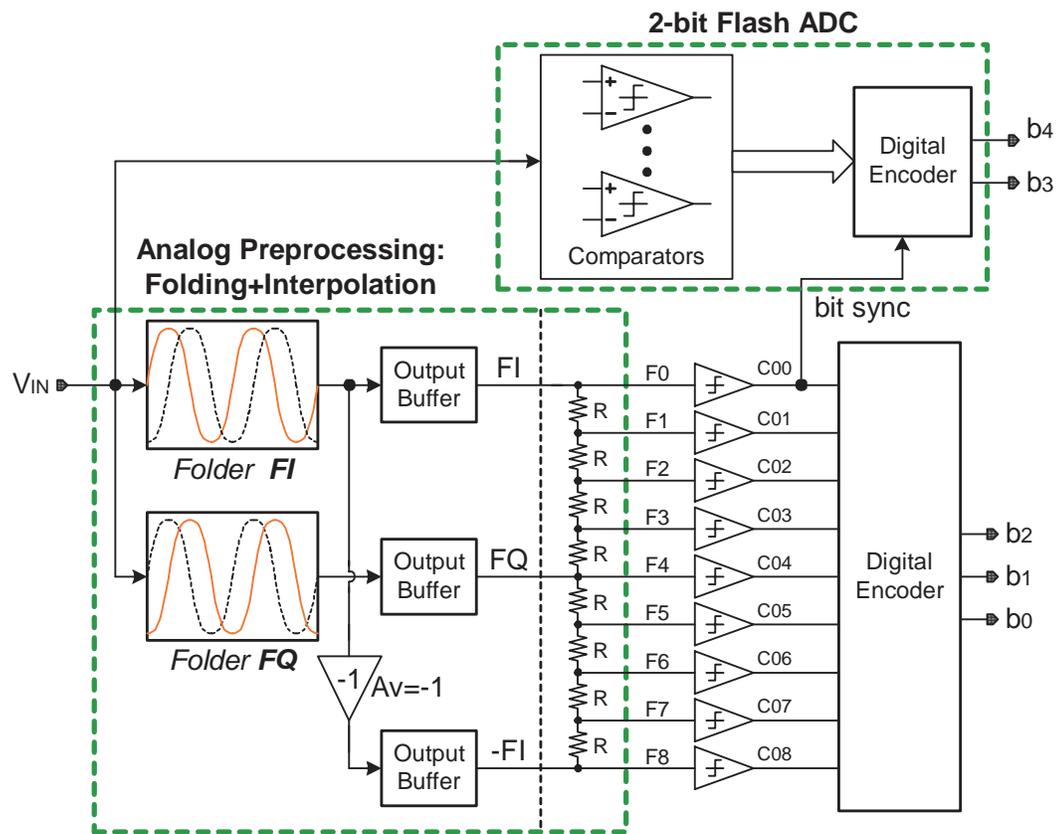


Figure 40 Schematic of a simple 5-bit F&I ADC ($F_F = 4$, $F_I = 4$, $N_F = 2$)

CHAPTER IV

SYSTEM LEVEL CONSIDERATION AND BEHAVIORAL MODELING

In this chapter, a behavioral model of F&I ADCs was developed and simulated in MATLAB SIMULINK. The model is used to analyze various non-idealities in an F&I ADC, such as folder bandwidth limitation, folder and comparator offset, folder and interpolator gain mismatch, and interpolator delay variation. The results aid the design of F&I ADCs by providing a comprehensive set of design criteria that must be satisfied by each building block.

4.1 Behavioral Model of F&I ADC Fine Quantizer Path

As mentioned in Chapter III (see Figure 26a), an F&I ADC consists of two signal paths: the coarse and fine paths. The coarse path is just a simple flash quantizer, which is comprised by a bank of comparators. All the analog preprocessing, including folding and interpolating, takes place in the fine path. Generally speaking, the performance of an F&I ADC is limited by the non-idealities in its analog preprocessing block. Thus, our behavioral model is aiming at modeling of those non-idealities in the analog preprocessing block.

Since the digital encoders, which consist of logic gates, are not likely to be the performance bottleneck of an F&I ADC, we assume all encoders, including cyclic-to-Gray and Gray-to-binary encoders, are ideal. SIMULINK provides models of basic logic gates to build these encoders.

Figure 41(a) shows an ideal model of the fine path of the simple 5-bit F&I ADC shown in Figure 40. The fine path is comprised by folders I&Q, 2 interpolators, and 9 comparators. Figure 41(b) shows the same behavioral model, with non-idealities introduced into it. Non-idealities included in the behavioral model include: non-linear folding characteristics, limited folder bandwidths (BW_{FI} & BW_{FQ}), interpolation errors

(ϵ_{1-16}), limited interpolator bandwidths (BW_{1-4}), and input referred comparator offsets (Δ_{1-9}).

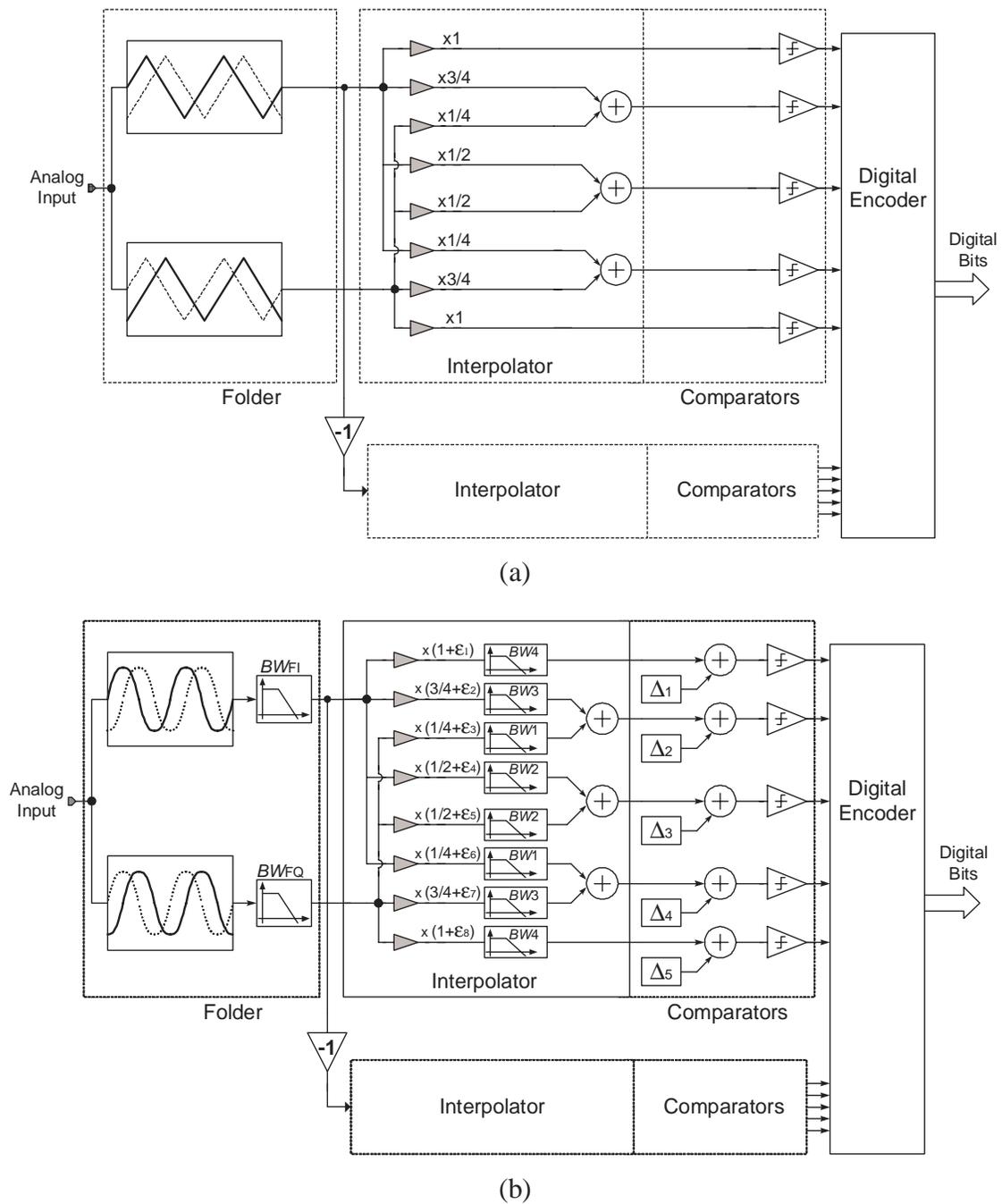


Figure 41 Behavioral model of fine quantizer path of an F&I ADC (a) ideal (b) with non-idealities

4.2 Behavioral Model of Major Building Blocks

Unlike filters and other linear or simple circuits, whose parameters can be derived analytically, the F&I ADC is a complex non-linear system, and non-idealities affect the ADC performance, which cannot be solved analytically. Behavioral modeling is a very useful tool to choose system parameters and determine bounds of non-idealities. A variety of error mechanisms could be enabled or disabled through the introduction of non-ideal components into the simulation model.

4.2.1 Folding Amplifier Model

The concept of signal F&I ADCs was first introduced by Arbel and Kurz [2] in 1975. The main motivation was the dramatic reduction of the number of comparators required in the design. Different methods of producing the folding signals have been proposed since then, but the most popular method involves the use of coupled differential pairs (CDPs)[73]. The periodic form of a folder's transfer characteristics is composed of segments that correspond to a differential pair's transfer characteristic. For a given input, all but one of the differential pairs in a folder are saturated. The one differential pair that is active produces the shape of the fold around the reference voltage connected to one of its inputs. If it is assumed that the MOS transistors have a square law I - V characteristic, then the transfer characteristic [51] of a differential pair is described by

$$V_{out} = A_{V0} \cdot (V_{in} - V_{REF}) \cdot \sqrt{1 - \frac{(V_{in} - V_{REF})^2}{4I_B / \beta}} \quad (4.1)$$

where $A_{V0} = g_{m0}R_L$ is the voltage gain of the differential pair when $V_{in} = V_{REF}$, I_B is the differential pair's tail current, $\beta = \mu C_{ox}(W/L)$, and R_L is the load of the differential pair. g_{m0} is the transconductance of the transistors comprising the differential pair. The voltage difference between V_{in} and V_{REF} that is required to switch the pair's tail current completely to one of the branches is simply

$$\Delta V = \sqrt{2I_B / \beta} \quad (4.2)$$

The transfer characteristic of a folding amplifier, or folder, was approximated by a periodic function based on segments given by (4.1). The behavioral model of a $4\times$ folding amplifier is shown in Figure 42(b). The same approach can be used to build an $8\times$ folding amplifier. In MATLAB SIMULINK, a nonlinear transfer characteristics can be implemented with a look-up table. The transfer characteristics curve of a differential pair block, or any other nonlinear transfer characteristics, can be described by two vectors: input vector $\vec{x} = (x_1, x_2, \dots, x_9)$ and output $\vec{y} = (y_1, y_2, \dots, y_9)$.

The non-idealities of a folding amplifier includes:

- Input referred offset, which is caused by the mismatch between the two transistors comprising the differential pair
- Nonlinear gain segments, which is caused by the nonlinear transconductance of the differential pair. Ideally a folding amplifier should have piecewise linear transfer characteristics.
- Gain mismatch, which is caused by the mismatch between differential pairs. Ideally all differential pairs should have the same transconductance value.
- Limited bandwidth, due to the limited bandwidth of the differential pairs, the folding amplifier acts like a low pass filter.

Figure 43 shows some non-ideal transfer characteristics mentioned above, where F_I and F_Q are part of two folding amplifier transfer characteristics, and z' is the zero crossing point of interpolated waveform $F_I/2 + F_Q/2$, and $\Delta z = z - z'$ is the interpolated zero crossing point error. In Figure 43(a), F_Q has an offset, which causes the interpolated zero crossing point z shifted from its ideal position z' . In this case, $\Delta z_{\max} = \text{offset}$. In Figure 43(b), the slope of F_Q is not constant, and zero crossing point shift results. The error term Δz depends on the shape of F_Q . In Figure 43(c), because F_I and F_Q have different slopes, the interpolated zero crossing point z is also displaced. In this case, Δz_{\max} is equal to gain mismatch, which is in percentage, multiplied by $|Z_Q - Z_I|$.

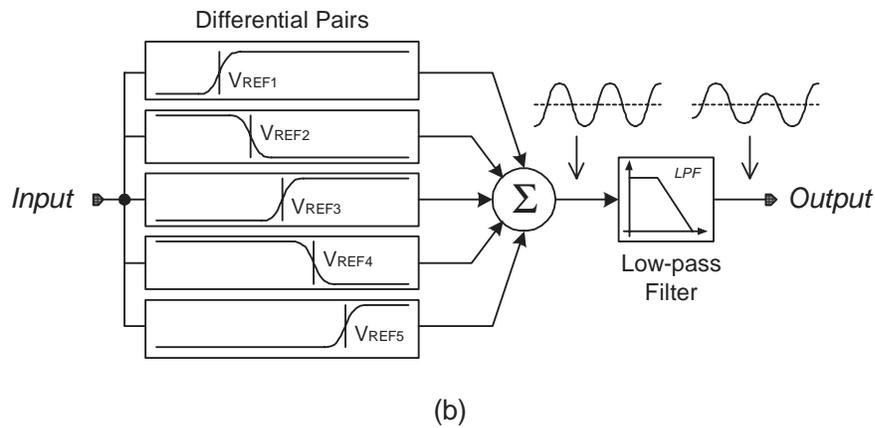
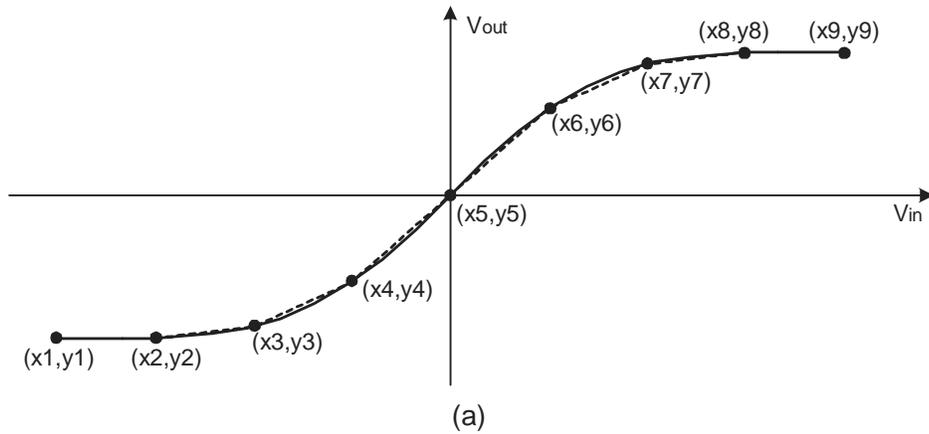


Figure 42 Differential pair and a $4\times$ folding amplifier behavioral models (a) differential pair modeled with vectors \vec{x} and \vec{y} . (b) folder behavioral model

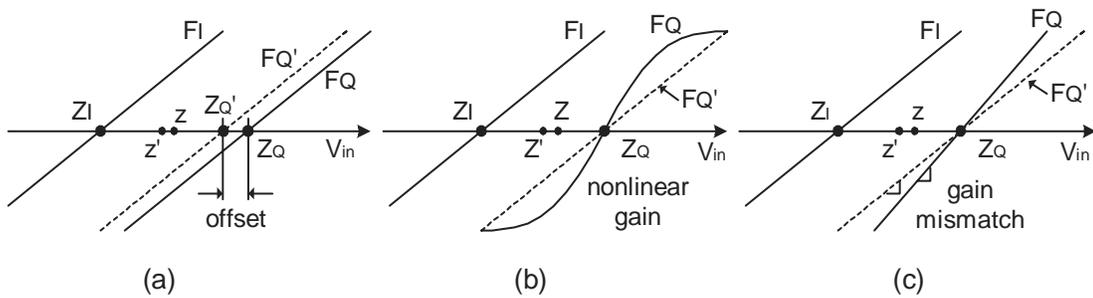


Figure 43 Non-ideal folding amplifier transfer characteristics F_Q . (a) input referred offset (b) nonlinear gain (c) gain mismatch

Limited bandwidth affects the output of the folder in three ways [51]: (i) it attenuates the waveform; (ii) it introduces group delay; (iii) it alters the relative position of the zero-crossings. There are other non-idealities for folding amplifier (i.e. slewing), but these *four* nonidealities, namely *offset*, *nonlinear gain*, *gain mismatch* and *limited bandwidth*, are most important ones in terms of effect on the whole A/D converter performance. Among all non-idealities mentioned above, the input referred offset, nonlinear gain and gain mismatch limit the resolution of folding ADC, while the limit bandwidth limits the input bandwidth.

Figure 44 is obtained from SIMULINK simulation on the model shown in Figure 42(b), with a 49MHz sinusoidal input signal. Zero crossing points are displaced from original positions, and constant shift doesn't cause distortion. Unfortunately, if the bandwidth is too low, the displacement distance is not constant, and distortion results. The effect of zero crossing point displacement on the ADC performance can be evaluated by doing FFT to the ADC output.

Signal to Noise and Distortion Ratio (SNDR) is used as the performance criteria in our evaluation. Table 4 shows the bandwidth requirements on the folding amplifiers with $4\times$ and $8\times$ folding factors. We can draw the following conclusions: (1) Higher resolution ADCs demand larger folder bandwidth; (2) At the same resolution, folders with $8\times$ folding factor require larger bandwidth than $4\times$ folders; (3) Lower bandwidth results in higher SNDR degradation.

TABLE 4 Bandwidth requirements on the folder

Resolution (bit)	Folder Bandwidth degrades SNDR by 2dB		Folder Bandwidth degrades SNDR by 1dB	
	$F_F=4$	$F_F=8$	$F_F=4$	$F_F=8$
6	$5\times f_{in}$	$8\times f_{in}$	$7\times f_{in}$	$12\times f_{in}$
7	$8\times f_{in}$	$11\times f_{in}$	$10\times f_{in}$	$14\times f_{in}$
8	--	$15\times f_{in}$	--	$18\times f_{in}$

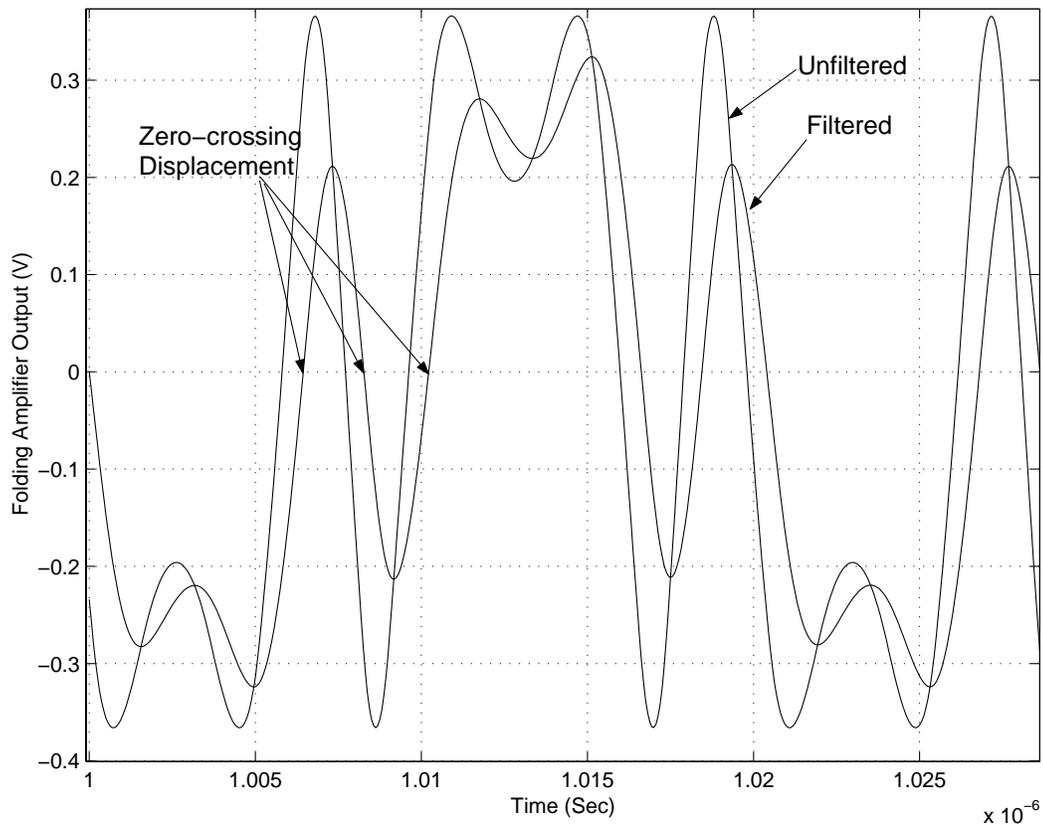


Figure 44 A $4\times$ folder output waveform deformed by limited folder bandwidth. The input signal is full-swing sinusoidal signal with frequency of $f_0=49\text{MHz}$, and the folder bandwidth is $4\times f_0=196\text{MHz}$.

The model shown in Figure 41(a) can be used to introduce non-idealities such as the nonlinear gain, gain mismatch, and input referred offsets, by adjusting the values of vectors \bar{x} and \bar{y} . As shown in Figure 41(b), a low-pass filter block succeeding the adder models the limited bandwidth of the folding amplifier. Thus, this behavioral model can model all *four* major non-idealities in a folding amplifier.

4.2.2 Interpolator Model

Almost at the same time as the folding concept was proposed, resistive interpolation was introduced to generate more folding waveforms without additional folding amplifiers. A simplified circuit and behavioral model of a $4\times$ interpolator is shown in Figure 45(a) and Figure 45(b), respectively.

An ideal interpolation block is a weighted adder: different interpolated voltages are generated by varying the weight coefficients. However, the interpolation circuit shown in Figure 45(a) has non-idealities such as: interpolation gain error and delay variation. The interpolation gain error is caused by the mismatch between interpolation resistors. The delay variation is caused by the RC constant formed by the interpolation resistors and input capacitances (and node parasitic capacitances) of succeeding comparators. Using Figure 45(a) as an example: the signal path from V_{inA} to V_{out2} include one resistor, while the signal path from V_{inB} to V_{out2} include three resistors, different signal paths will cause different delay. Higher values of resistance and capacitance give rise to delay variation.

Both non-idealities of the interpolation circuit mentioned above are modeled in the behavioral model shown in Figure 45(b). The interpolation gain error is modeled by adding an error term to the weight coefficients. The delay variation is modeled by inserting low pass filters between adder inputs and input signals. By varying the cut off frequencies of these low pass filters, we can model different delays caused by different RC constant.

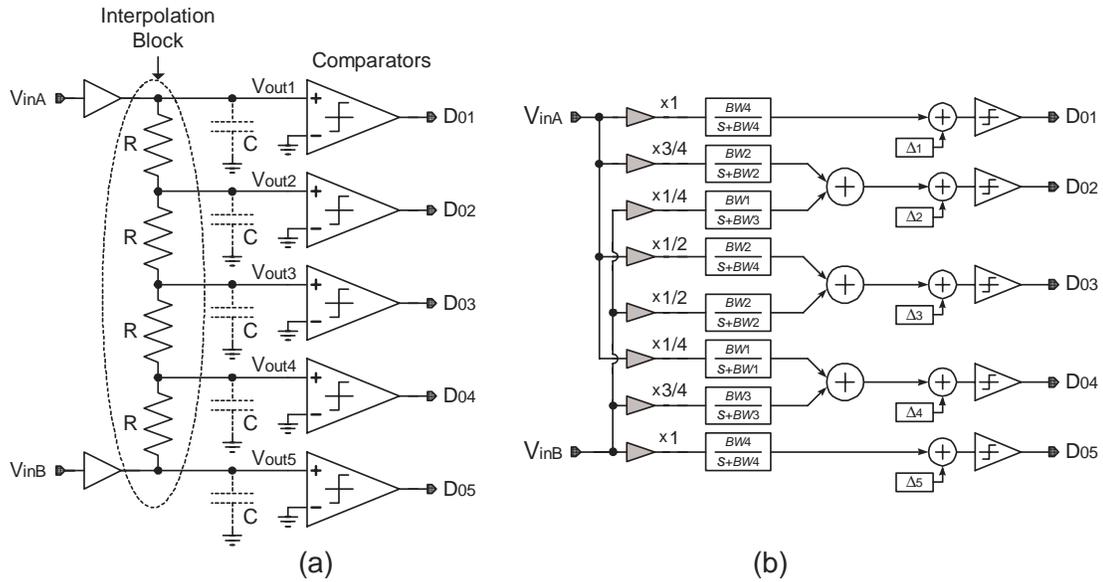


Figure 45 Interpolation block (a) resistor-based interpolator implementation
(b) behavioral model of interpolation block and comparators

4.2.3 Comparator Model

Comparators are used to detect zero crossings of the folding waveforms generated by folders and interpolators. Comparators have two major non-idealities: offset and limited bandwidth. Comparator offsets alter the locations of zero crossings and give rise to DNL and INL errors. The effect of the comparator offset is reduced by analog preprocessing gain, which is the combination gain of the folder and interpolator. The limited bandwidths of comparators succeeding interpolators have similar effect as the folding amplifier bandwidth. As long as the comparator preamplifier bandwidth is much larger than the folder bandwidth, the latter dominates. Usually it is true in practical cases. Based on this observation, we did not model it in our comparator behavioral model.

SIMULINK provides comparator model in its library. To model the comparator offset, which is a Gaussian distribution random variable, the user need to specify the mean (usually 0) and variance. The simulator then generates the random numbers as offset voltages for each comparator.

4.2.4 F&I ADC System Behavioral Model

Using the behavioral model of folder, interpolator, comparator and other blocks, we can build a folding A/D converter system in MATLAB SIMULINK. The behavioral model of a 7-bit F&I ADC system, including a reconstructing DAC, is shown in Figure 46. Detailed schematics of major building blocks are shown in Figure 47(a)-(f).

In Figure 46, the user can simulate different configurations: with or without front-end S/H (S/H1) through the multiport switch. The signal then feed the folding block and S/H2, which is used to balance the time delay on the fine and coarse paths. The upper part of Figure 46 is the fine path, which includes the folding block (Figure 47a), the interpolator (Figure 47b), comparator block (Figure 47c), and cyclic-to-Gray encoder (Figure 47d). The lower part is the coarse path, which includes S/H2 and coarse quantizer (see Figure 47e). Two coarse bits and 5 fine bits are combined in the Gray-to-Binary encoder block (see Figure 47f), which generate 7-bit binary code as the output of F&I ADC. A 7-bit ideal DAC is used to reconstruct the 7-bit binary code back to analog signal for analysis purpose. The analog output signal is saved as a data sequence.

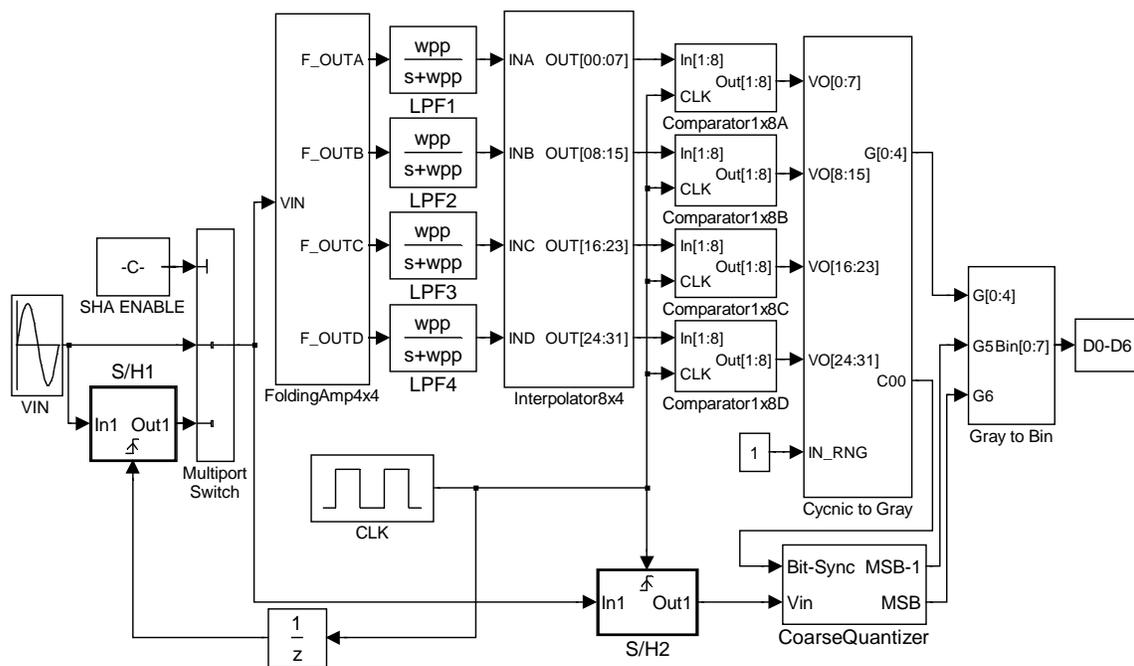


Figure 46 Behavioral model of the F&I ADC built in SIMULINK

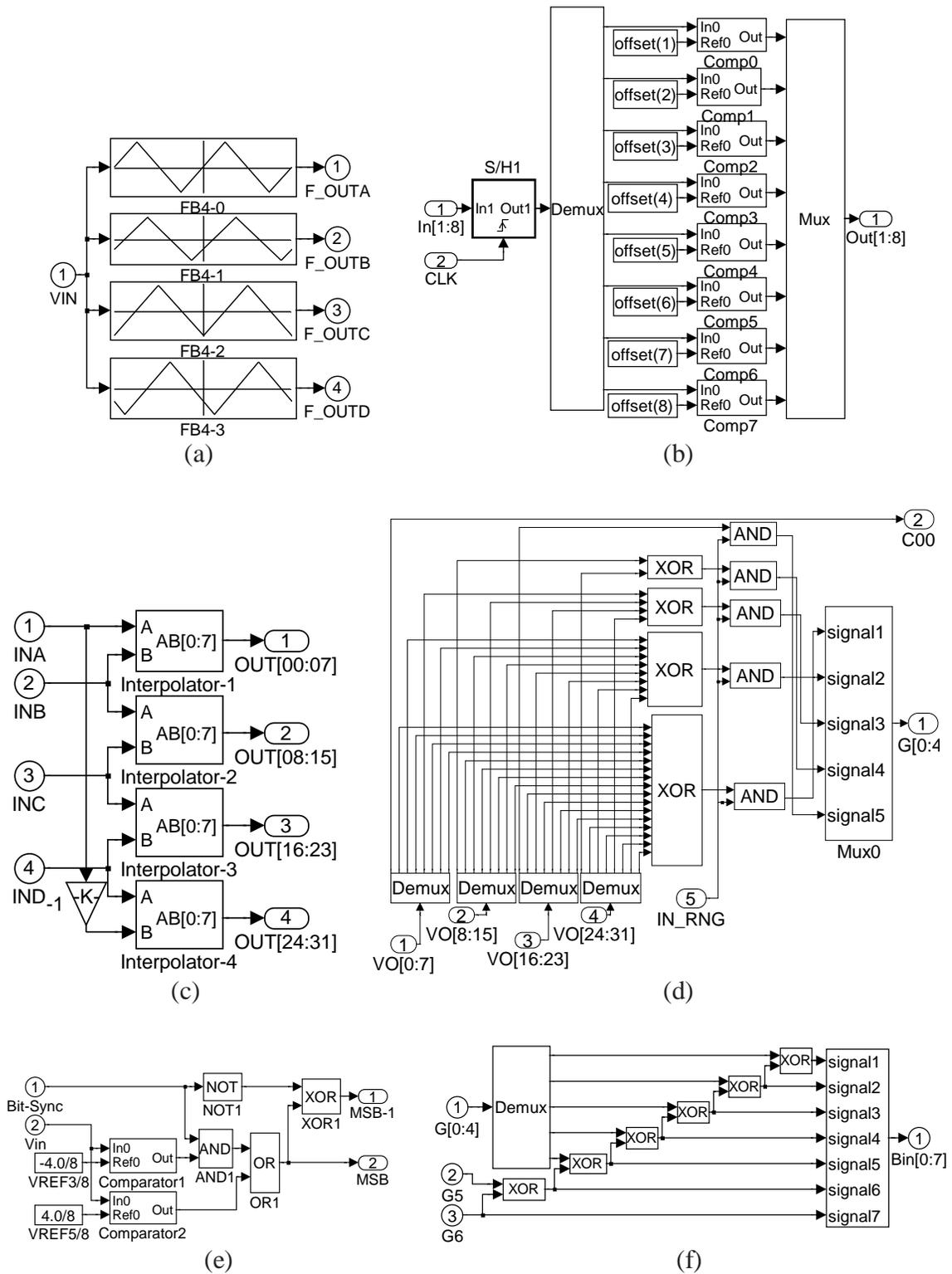


Figure 47 7-bit F&I ADC behavioral model blocks. (a) folder (b) comparator (c) interpolator (d) cyclic to gray encoder (e) coarse quantizer (f) gray to binary encoder

Discrete Fourier Transform (DFT) is performed on the saved data sequence to evaluate the performance of the F&I ADC. Signal to Noise and Distortion Ratio (SNDR) is chosen as performance criteria because it calculates both the quantization noise and harmonic distortion. For the sake of simplicity, an 8-point FFT is chosen as an example to show how the SNDR is calculated. For a time domain sinusoidal signal $S[n]$, $n=1, \dots, 8$, its frequency domain representation can be calculated through FFT as $F[m]$, $m=1, \dots, 8$. The magnitude of $F[m]$ can be calculated, denote them as $A[m]$, $m=1, \dots, 8$. Note because of $A[m]$ is symmetrical, we have $A[j]=A[8-j]$, $j=1, \dots, 8$, thus all signal and noise plus distortion information are contained in $A[m]$, $m=1, \dots, 4$, and one of them represents signal amplitude, say $A[2]$. The SNDR is $SNDR = A[2]^2 / (A[3]^2 + A[4]^2)$. $A[1]^2$ is not included because it is DC energy, which is usually not counted as noise or distortion.

Figure 48 shows the behavioral model of one of the four $8 \times$ interpolators in Figure 46(b), which generates 8 interpolated outputs from 2 input signals. Random number with zero mean Gaussian distribution is used to model the interpolation gain error, i.e., a amplifier with nominal gain of $1/8$ may be modeled as $1/8 \times (1 + \varepsilon)$, where ε is the interpolation gain error term. The user need to specify the variation based on the process parameters such as resistor and transistor mismatch boundaries.

The bandwidth limitation effect in the interpolator due to the interpolation resistance and comparator input capacitance is like a complex multi-pole low pass filter. For the sake of simplicity we use single pole low pass filters to model this effect.

The bandwidth of the low pass filters depends on the gain of the amplifier preceding it. For example, the bandwidth of the low pass filter after an amplifier with gain of $7/8$ is estimated to be $1/RC$, because the signal passes through one RC network. Similarly, if the gain is $i/8$, the corresponding bandwidth is $\frac{1}{RC(8-i)}$, where $i=1, 2, \dots, 7$. Of course

there are some errors introduced when we use a single pole system to approximate a multi-pole system. Also the impedances of the folders driving the interpolator are assumed to be zero, which may not be negligible in practical cases. For these reasons,

one should not solely rely on the behavioral model to determine the interpolation resistance. Since the behavioral model is just used to get some design guidelines, thus its accuracy is not comparable to that of circuit level simulators.

For current mode interpolators based on current mirrors, the bandwidths for all the interpolator outputs are the same, which is the bandwidth of the current mirror. Thus, there is no delay mismatch in current mirror based interpolator. The behavioral model shown in Figure 48 can still be used to model current mirror based interpolators, but all low-pass filters in Figure 48 have the same bandwidth.

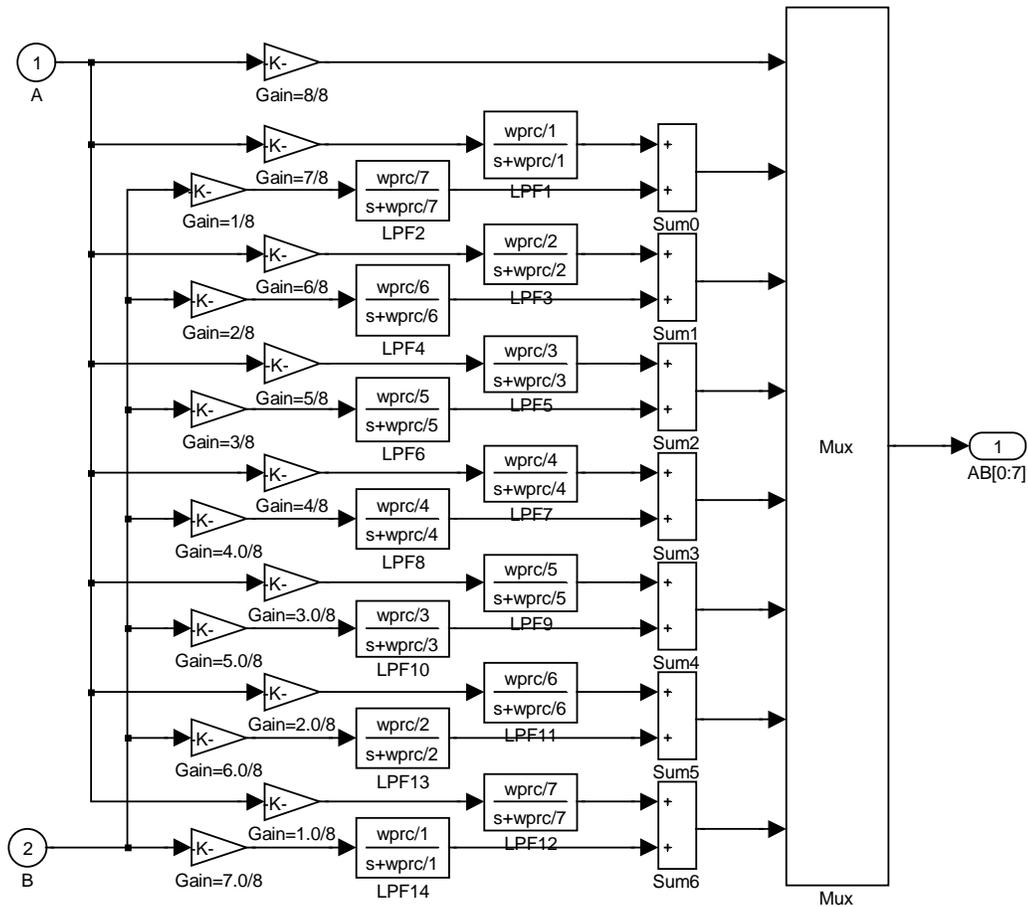


Figure 48 Behavioral model of the interpolator in SIMULINK

4.3 Behavioral Simulation of Folding ADCs with Non-idealities

In this section the behavioral model shown in Figure 46 is used to simulate some major non-idealities of F&I ADC. The effects of major non-idealities such as folder bandwidth limitation, gain mismatch, interpolation gain error, folder and comparator offsets, on the F&I ADC performance are analyzed.

4.3.1 Frequency Multiplication Effect

Frequency multiplication effect is inherent to folding ADCs due to the “folding” transfer characteristic of the folding amplifier. Figure 49 shows the input and output of a 4 \times -folding amplifier. After the folding operation, a 1 MHz full swing continuous-time sinusoid input signal is converted to a complicated signal with much higher frequency components. In this example, the most significant harmonic term is the 5th harmonic. This does not mean the 5th harmonic is always the largest component among all harmonics for a 4 \times folder, depends on the transfer characteristics, 6th harmonic might be the largest one. That is the name frequency multiplication effect comes from. It is clear that multiplication factor is approximately proportional to the folding factor of the folder, thus for a folder with larger folding factor, the frequency multiplication effect is more serious.

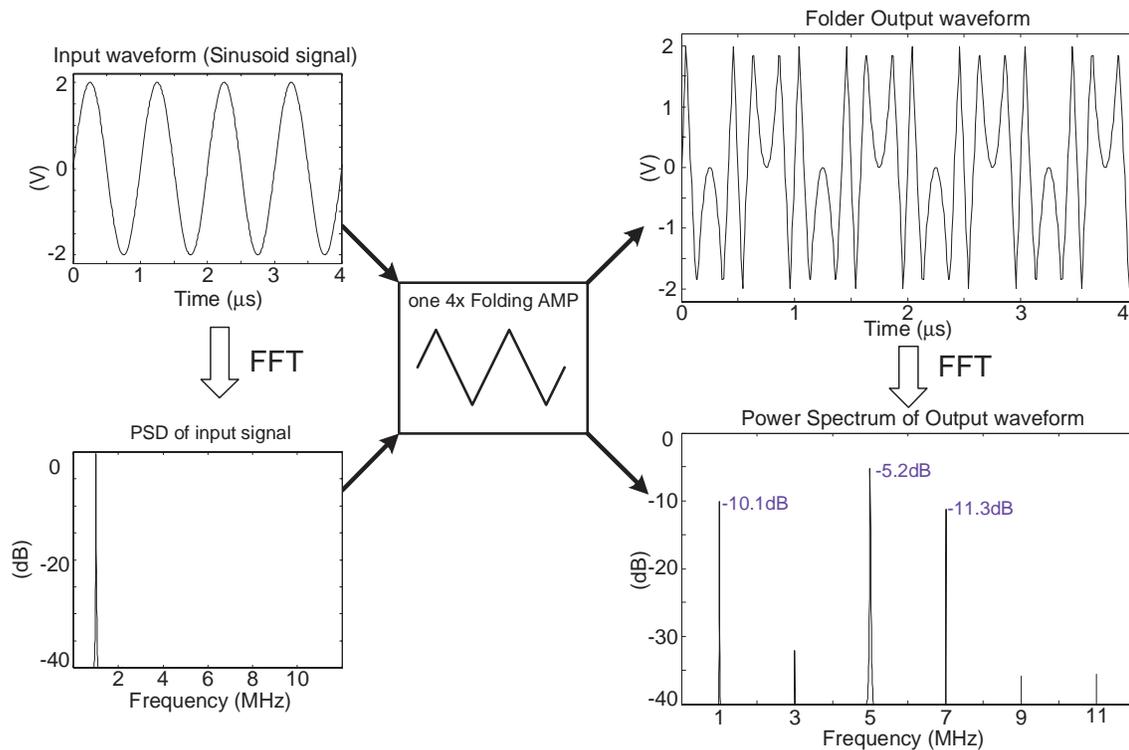


Figure 49 Frequency multiplication effect of a 4× folding amplifier

If the bandwidth of folding amplifier (or other analog preprocess blocks) is not large enough, this high frequency internal signal would cause the degradation of the dynamic performance of an F&I ADC. First, it requires the analog preprocessing blocks, including folders and interpolators, to have large bandwidth, i.e., an order of magnitude higher than the maximum operating frequency. For example, if the input signal frequency is 150MHz, the folding amplifier bandwidth should be higher than 1.5GHz to avoid severe performance degradation. Second, the slew rate of the folding amplifier and interpolators also should be large enough to prevent the signal slew. Both large bandwidth and slew rate demand large bias current. For low power ADCs [18],[19], a limited input analog bandwidth is imposed.

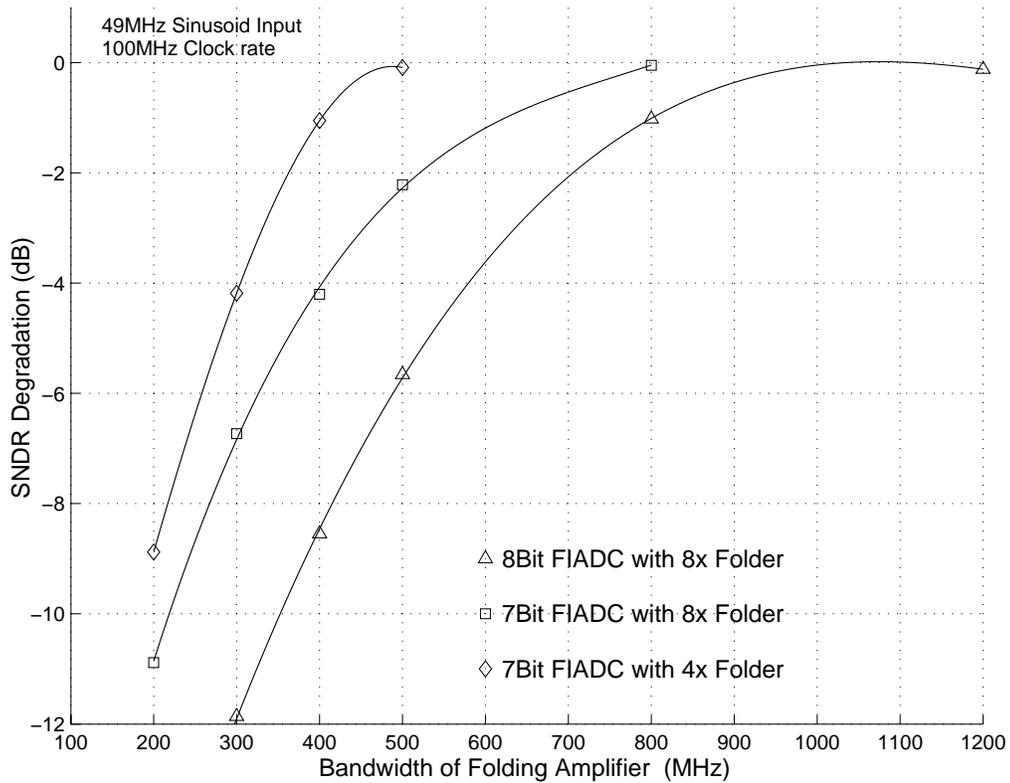
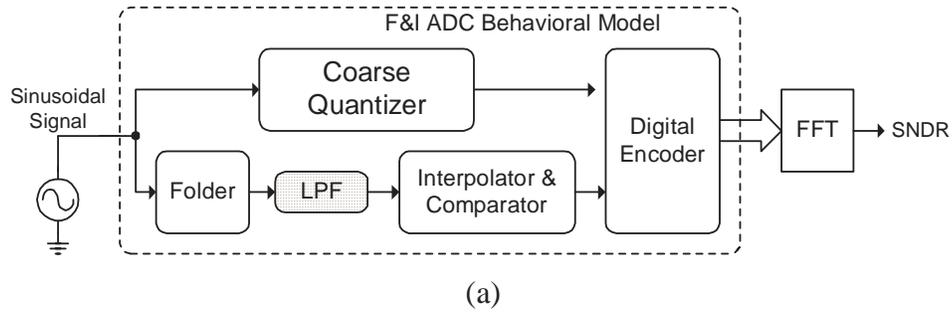


Figure 50 SNDR degradation due to limited folding amplifier bandwidth (a) simulation setup (b) results

Performance degradation due to frequency multiplication effect can be simulated with the behavioral model. Figure 50(a) shows the behavioral simulation setup, in which a low pass filter is placed after the ideal folder to model the limited folder bandwidth. Figure 50(b) shows the SNDR degradation depends on the folding factor and resolution

of the F&I ADC. For F&I ADCs with same folding factor ($8\times$) but different resolutions, higher resolution requires higher bandwidth. For F&I ADCs with same resolution (7-bit) but different folding factors, the higher folding factor ($8\times$) one requires larger folder bandwidth. For the 7bit ADC with $4\times$ folding amplifier, the bandwidth should be greater than 500MHz with a sinusoidal input signal of 49MHz. At the same resolution that bandwidth requirement is increased to 800MHz if the folding factor is 8. Increased folding factor means more power and area saving by reducing the number of comparators, but frequency multiplication effect also becomes more severe, thus, there is a tradeoff.

4.3.2 Folding Amplifier Offset

Due to the transistor mismatch, amplifiers comprising differential pairs have offsets. In A/D converter design, offsets often degrades linearity, thus limit the resolutions. In the folding amplifier case, the offsets of differential pairs alter the ideally evenly distributed zero crossings, thus cause linearity degradation and this will reflect in the decreased SNDR.

Figure 51a shows the behavioral simulation setup, in which the X-axis is the standard deviation of the folder offset voltages. The full swing of the F&I ADC is 4V, thus one LSB of the 7-bit ADC is 31.25mV, whereas one LSB is 16.125mV for 8-bit ADC. Each of the zero crossing point of all folders are assigned a random variable with Gaussian distribution. The average value (mean) and standard deviation of the random variables are determined by the user based on process mismatch parameters. For example, if the offset is lower than 10mV, then one can assume the standard deviation is one third of that value, i.e. $3\sigma=10\text{mV}$. Figure 51b shows simulation results. As expected higher resolution ADCs have more stringent requirements on folder offsets, and degradation due to folder offset is almost independent of folding factor. The usual upper boundary of the offset value is a quarter to half of one LSB.

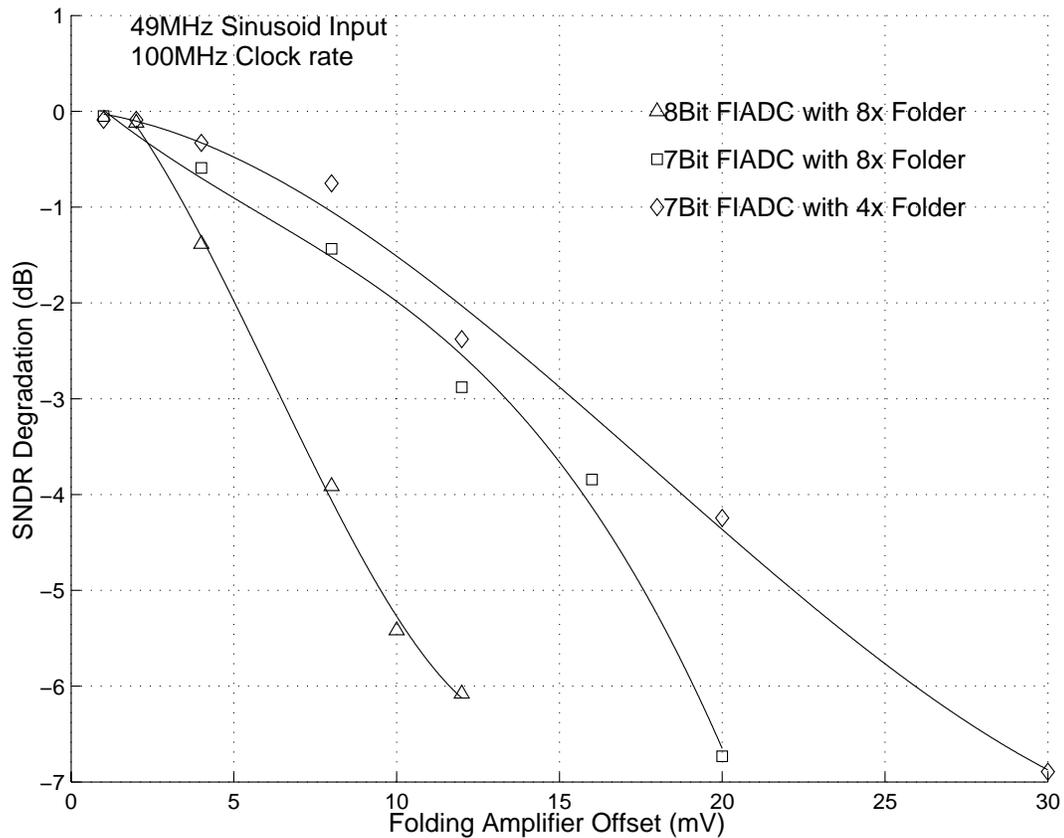
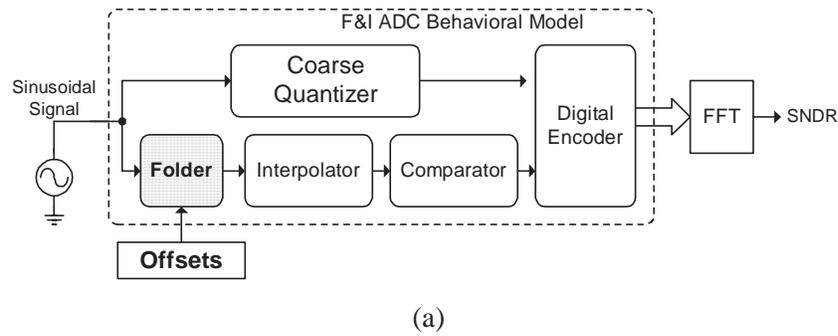


Figure 51 SNDR degradation due to the folding amplifier offset (a) simulation setup
(b) results

4.3.3 Folding Amplifier Gain Mismatch

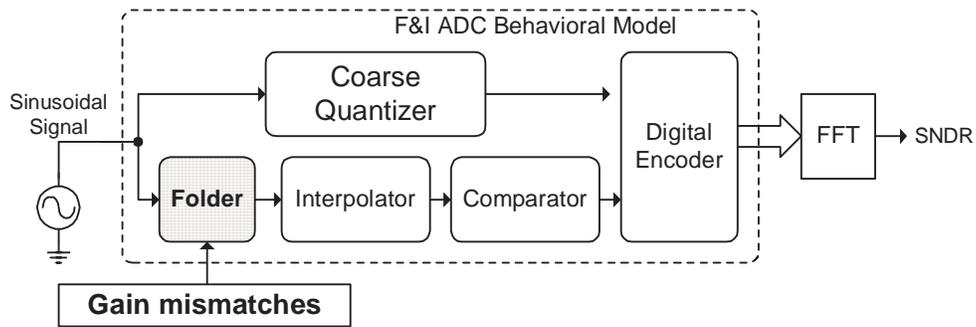
Ideally the folding amplifier should have piecewise linear transfer characteristics, but due to the mismatch between different differential pairs in the folding amplifier, the slopes of each linear segment may be different. Due to the gain mismatch, zero crossings

generated by the interpolator may be displaced from ideal positions, as shown in Figure 43.

As mentioned in previous sections, a $4\times$ folder consists of 5 differential pairs, and an adder is used to combine the 5 differential pair outputs to obtain a pseudo-sinusoidal or triangular shaped folding transfer characteristic. To model the gain mismatch, a gain stage is placed between each differential pair and the adder. The gain is $(1+\epsilon)$, where ϵ is a Gaussian distribution random variable to model the gain mismatch. The user needs to specify the mean (usually zero) and standard deviation σ . The behavioral simulation setup is shown in Figure 52(a) and results are plotted in Figure 52(b).

It is shown in the plot that for F&I ADCs with same folding factor of 8, the SNDR of the 8bit ADC decreases more rapidly than that of the 7bit ADC. This result is expected, for the high resolution ADCs require higher interpolation accuracy. However, with the same resolution of 7-bit, the F&I ADC with $4\times$ folding factor has worse performance than the F&I ADC with $8\times$ folding factor. The reason is because the $8\times$ folding 7bit ADC has a smaller interpolation factor ($4\times$) while the other 7bit ADC's interpolation factor is 8. With same slope mismatch, the higher interpolation factor cause more linearity error, and the non-linear slope of the folding factor deteriorates the performance further.

Figure 52 reveals that gain mismatches with standard deviation of less than 4% causes negligible SNDR degradation. In practical cases, gain mismatch is unlikely to be higher than 4%, thus it is usually not a major source of distortion.



(a)

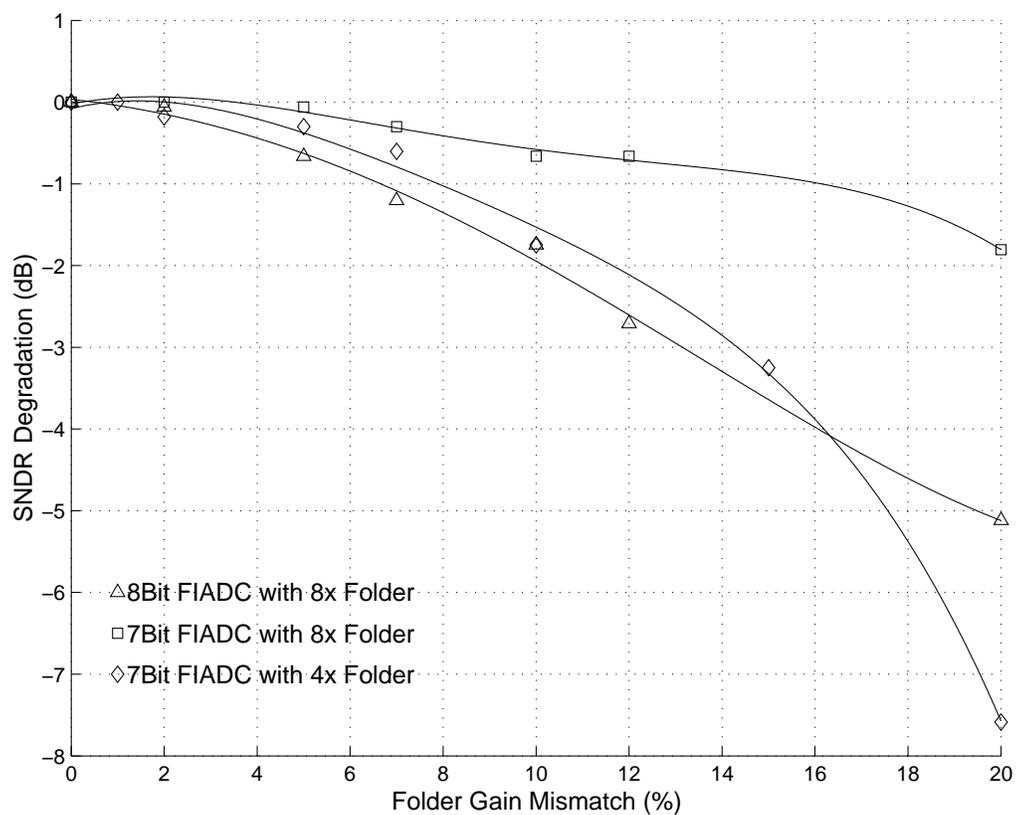


Figure 52 SNDR degradation due to the folding amplifier gain mismatch (a)
simulation setup (b) results

4.3.4 Interpolation Gain Error

An interpolator is used to generate more zero crossing points from two primary folding waveforms. For example, for a $4\times$ interpolator with two input voltages V_A and V_B

, it should generate 3 more extra folding waveforms: $0.75V_A+0.25V_B$, $0.5V_A+0.5V_B$, $0.25V_A +0.75V_B$. The interpolation gains, i.e. coefficients, from 0.75 to 0.25, are determined by interpolation resistors (or transistor sizes in the current interpolator case).

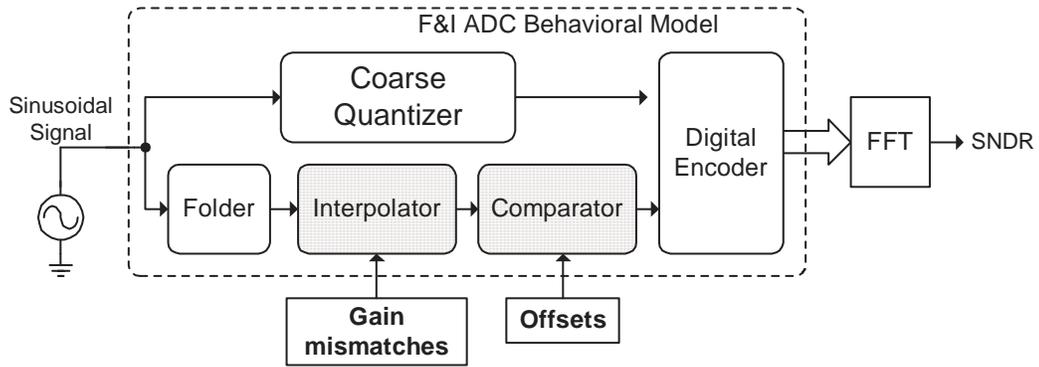
Because of the resistor (transistor) mismatch, the interpolation coefficients are not equal to their ideal values, i.e. they have errors. Figure 53 shows how the SNDR varies with combination of two non-idealities including interpolation gain error (in percentage) and comparator offset. The simulation is on a 7bit ADC with $4\times$ folding factor and $8\times$ interpolation factor. The folder bandwidth is $10\times$ input frequency and no S/H is placed before the folder. As expected, in all 3 cases the SNDR decreases with increasing interpolation gain error. When the interpolation error is low, the comparator offset dominates. Interpolation errors less than 5% causes no significant SNDR degradation.

4.3.5 Comparator Offset

Comparator offsets are always one of the major limiting factor of ADC linearity. ADCs with higher resolutions require the comparators have no offset voltages. SIMULINK provides the ideal comparator model. To simulate the offset voltages, one can use random variables with Gaussian distribution, the mean and standard deviation of which are determined based on the resolution requirement of the whole ADC.

Figure 54 shows the behavioral simulation results of a 7-bit F&I ADC with $F_F=4$ and $F_I=8$. The X-axis is the ratio between folder bandwidth and input frequency, and Y-axis is the SNDR degradation in dB. For F&I ADCs with comparator offsets standard deviation of $1/6\text{LSB}$, the performance is acceptable.

In general, to ensure the offset to be lower than $1/2\text{LSB}$, the upper limit of the standard deviation is one third of $1/2\text{LSB}$, i.e., $1/6\text{LSB}$. Note that this is the offset referred to the F&I ADC input, which is the actual comparator offset divided by the analog preprocessing gain. If that gain is larger than one, then the requirement on the comparators can be relaxed, i.e., if the analog preprocess gain is 2, the $1/6\text{LSB}$ requirement in above example can be relaxed to $1/3\text{LSB}$. Because of this, an analog processing gain lower than one is not desired. However, if the analog preprocessing gain is too high, bandwidth would be limited.



(a)

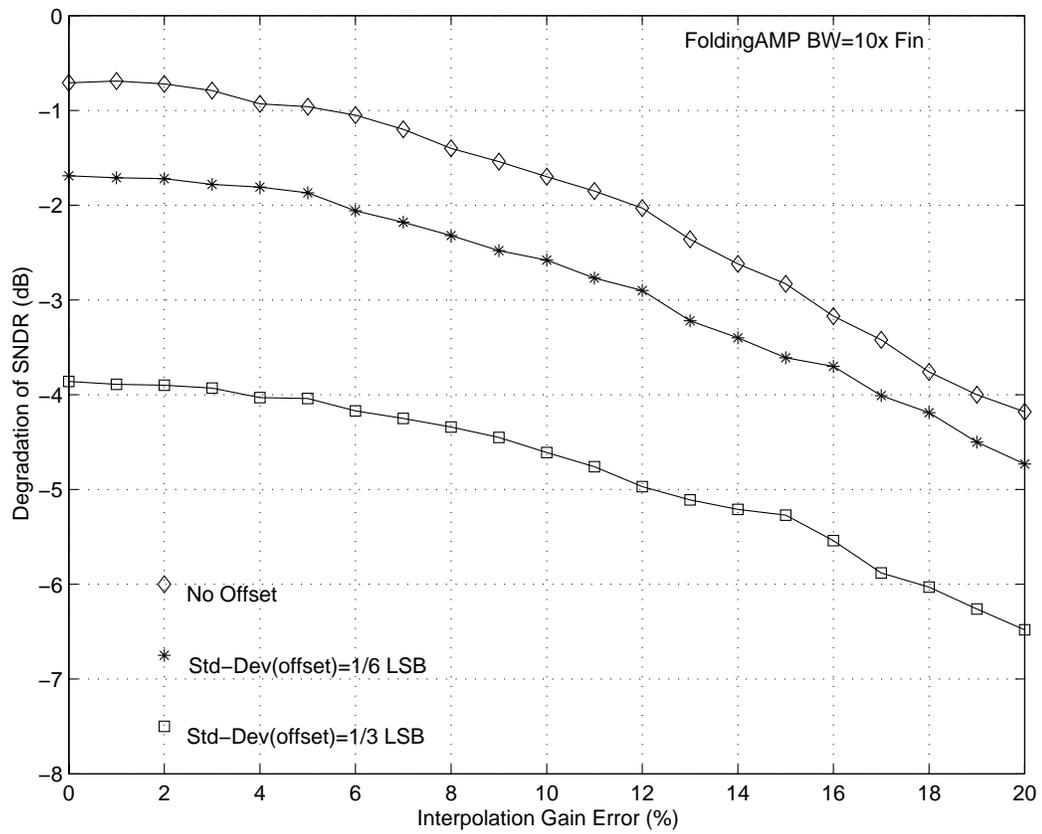
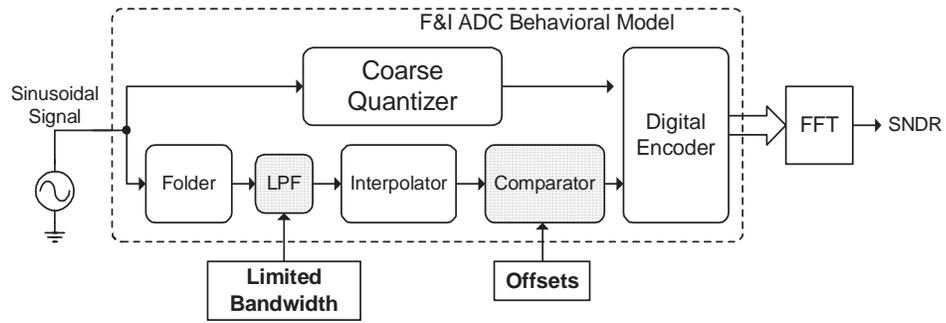
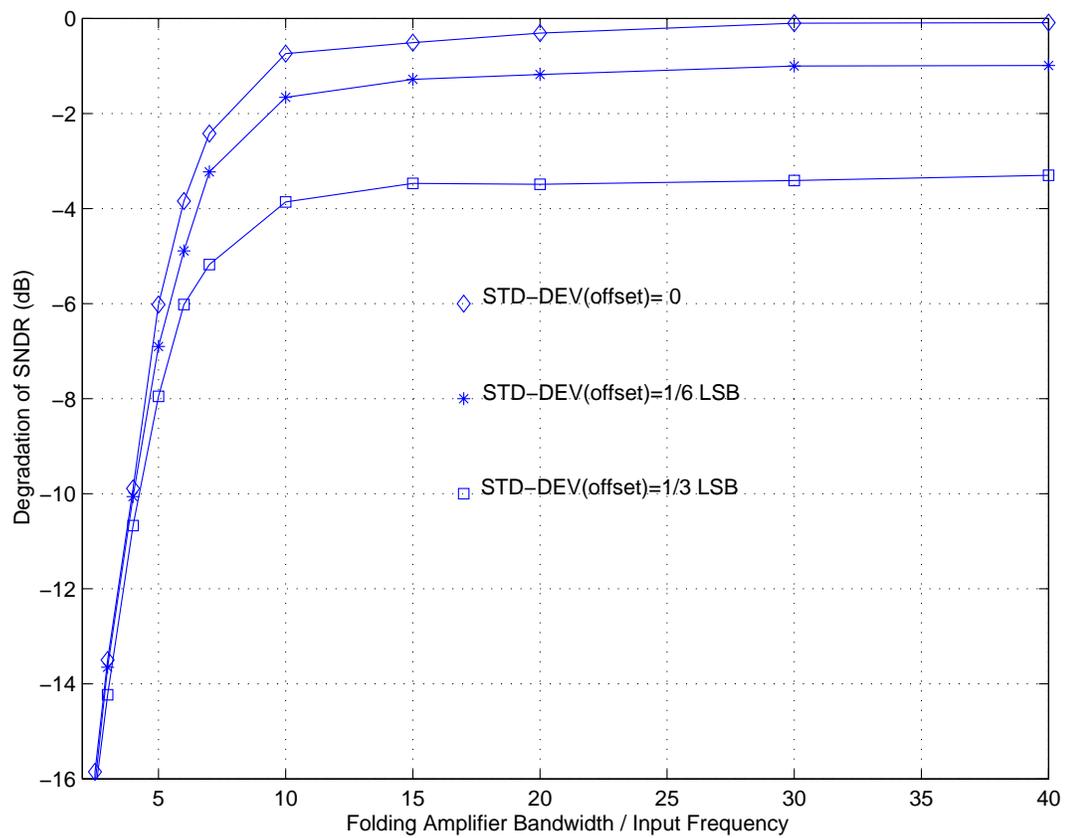


Figure 53 SNDR degradation vs. interpolation gain error and comparator offset (a) simulation setup (b) results



(a)



(b)

Figure 54 Effect of composite non-idealities: folder bandwidth and comparator offset

(a) simulation setup (b) results

4.3.6 Interpolator Delay Variation

Interpolation consists in constructing a new signal through weighted summation of two input signals, i.e., signal C is the interpolation of signal A and B , if $C = w_1 \cdot A + w_2 \cdot B$. Parameters w_1 and w_2 are weighting coefficients. In real designs, resistor network and current mirror are the popular choices for voltage and current mode interpolators.

The non-idealities of an interpolator, as illustrated in Figure 55(a), can be modeled with behavioral model shown in Figure 55(c). The non-idealities considered here include interpolation coefficient error (ε), and bandwidth limitation in the form of delay mismatch, which depends on the RC constant formed by the interpolation resistor and comparator input capacitance. In the behavioral model shown in Figure 55(c), the interpolation coefficient error is modeled with an error term (ε) in the interpolation weighting coefficients. Error terms ε_1 and ε_2 in Figure 55(c) represent resistor mismatch in percentage. The delay mismatch is modeled with a low pass filter, whose bandwidth varies with different taps on the interpolation network. The total capacitance including the comparator input capacitance and parasitic capacitance, can be as high as $100fF$. The effect of RC constant can be significant when the input signal frequency is high.

Figure 55(a) shows an ideal voltage mode interpolator based on resistor network. Figure 55(b) shows the non-idealities, including a nonzero folder output impedance and comparator input capacitance C . These non idealities, plus the resistor mismatch, cause interpolation error ε_1 and ε_2 , and bandwidth limitation, in the behavioral model shown in Figure 55(c). In Figure 55(c), the two low-pass filters have different bandwidths, because one signal from V_A to V_O and another signal from V_B to V_O pass different number of RC low pass stages, thus they have different delays.

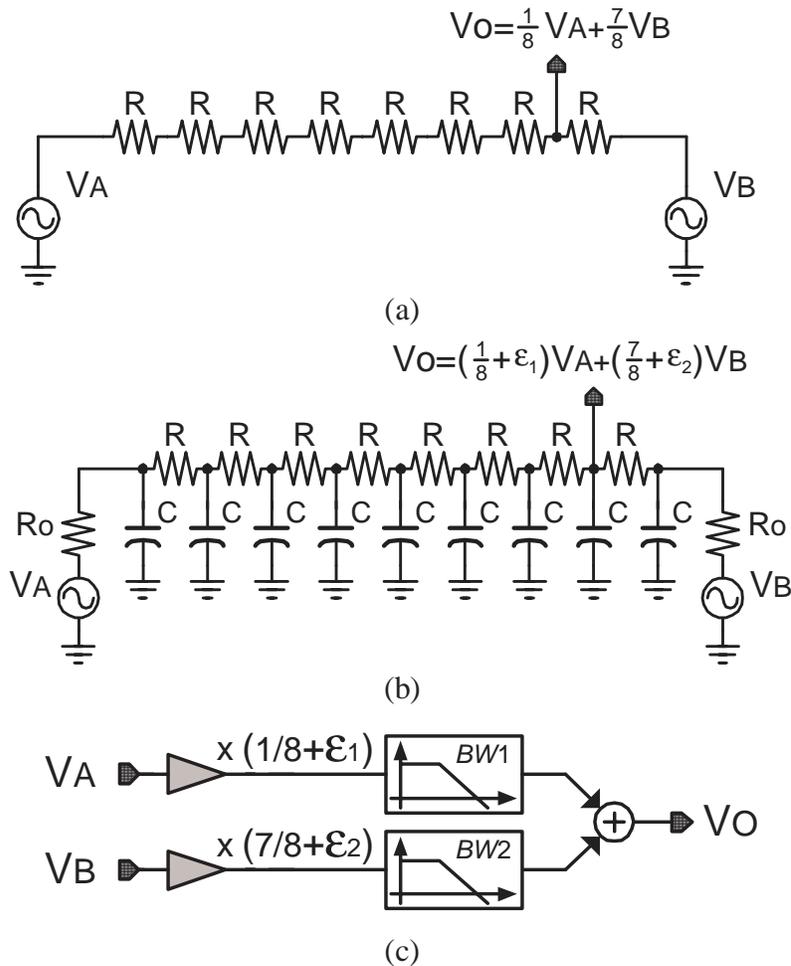


Figure 55 Voltage mode interpolator based on resistor network (a) ideal voltage mode interpolation (b) with non-idealities including node capacitance C and folder output impedance R_o . (c) behavioral model of the circuit shown in (b)

In a resistor based interpolating system, the interpolation accuracy (measured by gain error) is limited by resistor mismatch. That mismatch will affect the resolution of ADC. From the speed point of view, the resistance value of these interpolation resistors should be low. The RC constant, formed by these resistors and the input capacitances of comparators and parasitic capacitance, slows down the whole system. Another problem is the delay difference caused by different impedances looking back into the interpolator from the input terminals of each comparator.

Figure 56 shows the simulation results on the effect of RC constant on a 7-bit F&I ADC. The plot indicates that the RC time constant should be less than 4ps to avoid significant SNDR degradation. Here is an example: assuming input signal frequency is 100MHz and node capacitance is 0.1pF, the value of interpolation resistor should be less than 40Ω . To drive such a low impedance interpolating resistor-ladder, folding amplifiers output voltages need to be buffered and these wide band low output impedance buffers are power hungry. For example, in a bipolar design [11], emitter followers are used as the buffer between the folder and resistor based interpolator.

Current mode interpolation, which is based on current mirrors, can be used to solve the delay variation problem. This is discussed in next section.

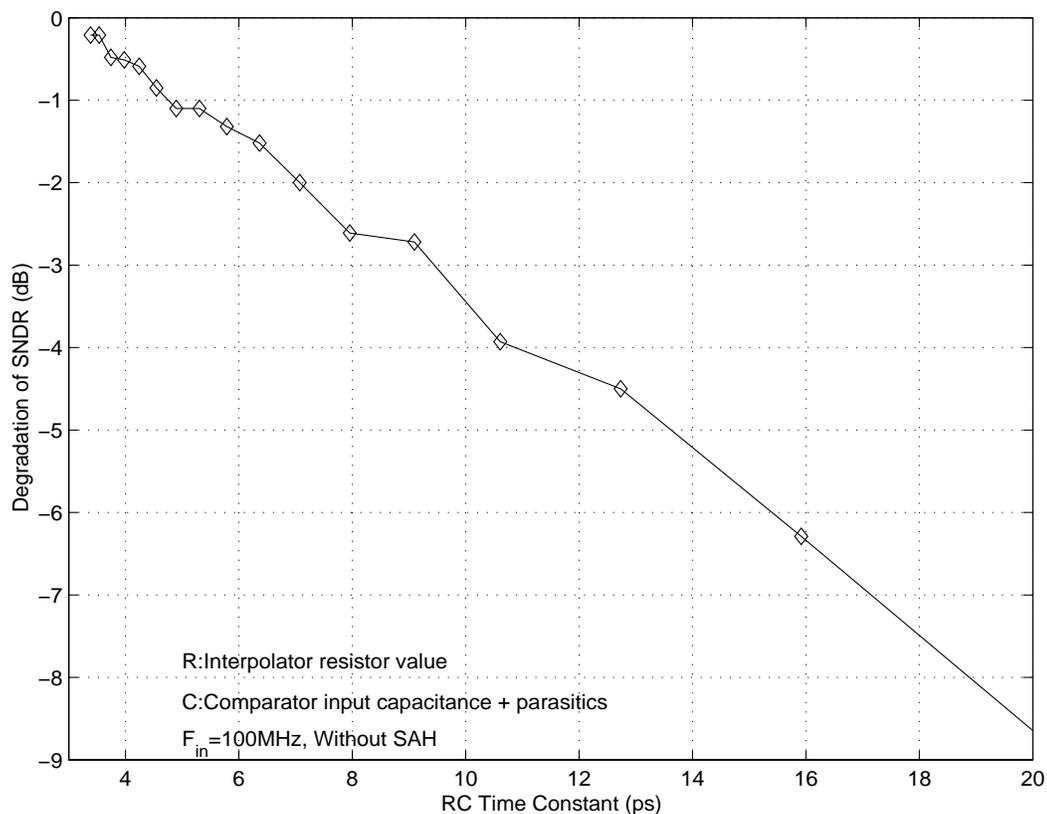


Figure 56 Effect of delay variation on the SNDR of ADC in a resistive voltage mode interpolator

4.4 Proposed Solutions

We have discussed the effect of several non-idealities on the resolution and speed of folding and interpolating A/D converters. Among them, the interpolation gain error, folding amplifier offset, comparator offset depend on component mismatch (resistor and transistor), thus can be controlled by choosing proper component sizes. However, we have two problems.

First is the folding amplifier bandwidth, one can increase bias current to increase it. However, this will be problematic when input signal frequency is high, i.e., 150MHz. As mentioned in previous discussion, in a $4\times$ folding factor system, the folder bandwidth should be around $10\times$ higher than the input frequency (for $8\times$ folding factor system, that number is even higher). If the input frequency is 150MHz, the requirement of the folder bandwidth would be higher than 1.5GHz. Even if we can design a folding amplifier with such high bandwidth, the power consumption will be significant.

Second is the delay variation. Although the resistive interpolator was quite popular, it has delay variation problem. As we already know, to circumvent these non-idealities, the interpolation resistor value should be very low, i.e. 40Ω for 100MHz input signal. Power hungry buffers are required to drive such low impedance loads.

Front-end S/H is proposed to solve the frequency multiplication effect and alleviate the delay variation problem. From behavioral simulation, we will see it require much lower folding amplifier bandwidth. Current mode interpolation can be used to reduce the effect of delay variation in interpolators.

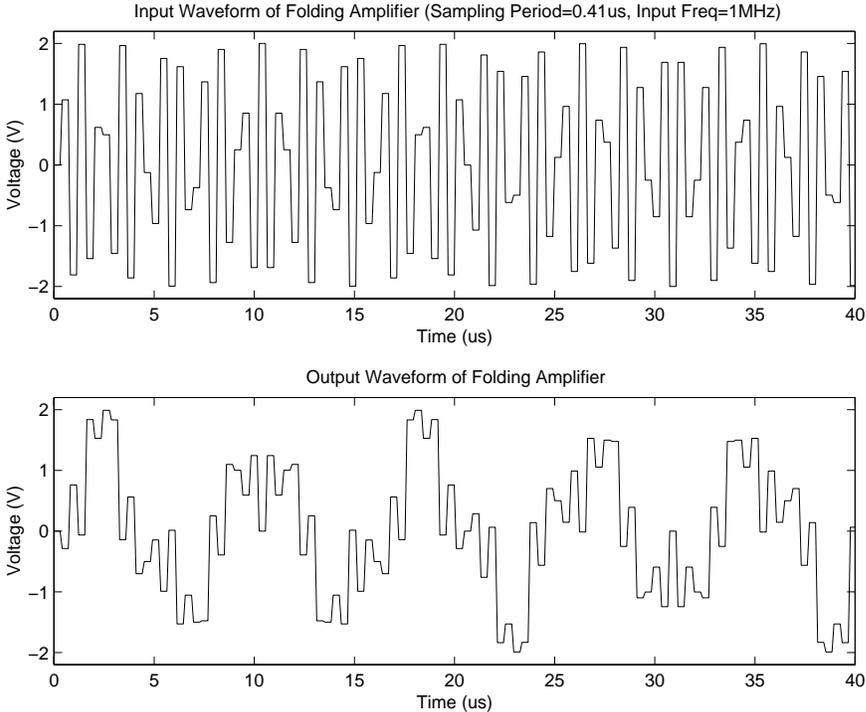
4.4.1 Front-End Sample-and-Hold

From architecture level, a front-end sample-and-hold unit can be used to alleviate the frequency multiplication problem. For a sampled-data system, the maximum signal frequency is Nyquist frequency, which is half of the sampling rate. With a front-end sample-and-hold amplifier (S/H) preceding the folding amplifier, the maximum internal frequency generated by the frequency multiplication effect is also limited in the Nyquist range.

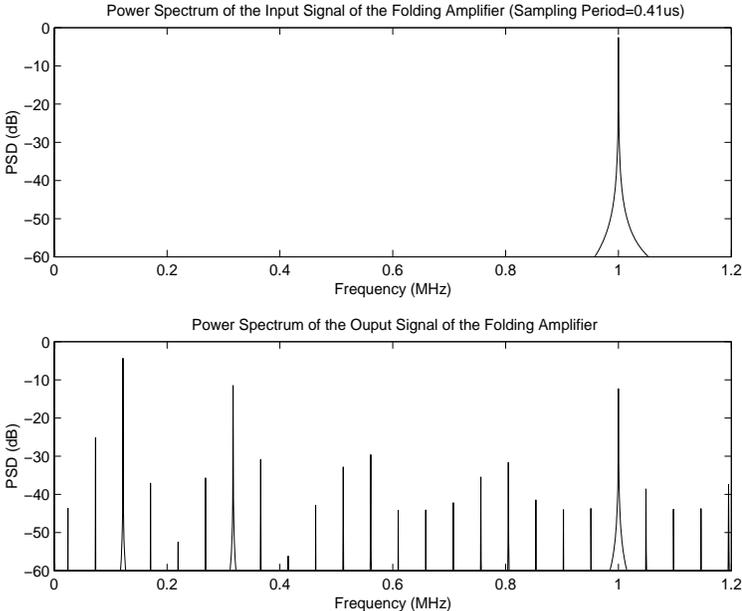
Figure 57(a) shows the input and output waveforms of a folding amplifier with a preceding S/H unit. From Figure 57(b), we can see the output signal's spectrum lines are lower than the input frequency. Indeed, in time-domain waveforms shown in Figure 57(a), the output signal is somewhat “slower” than the input signal.

The reason is due to the discrete-time nature of a sampled data system. For a discrete-time system with a sampling frequency F_s , the signal frequency cannot exceed Nyquist frequency ($F_s/2$). Our sampled data ADC system is not an exception, although the folding amplifier tries to convert input signal to higher frequencies, these high frequencies are reflected back into Nyquist range.

Again, we use behavioral model simulations are used to compare performances of F&I ADCs with and without front-end S/H. Figure 58(a) shows the simulation setup. A switch is placed before the F&I ADC to determine whether the S/H is included or not. Input signal frequency is swept from low frequency to Nyquist rate. Figure 58(b) plots the SNDR degradation vs. input frequency. It is obvious that, under the same folding amplifier bandwidth, which is $1.2\times$ sampling rate, the F&I ADC with S/H has much lower SNDR degradation in the whole Nyquist range. However, for the F&I ADC without front-end S/H the SNDR drops more than 2dB when the input frequency is merely higher than 15% of the sampling clock frequency. In theory, for an F&I ADC with front-end sample and hold, a folding amplifier bandwidth of $1\times$ sampling rate is enough to obtain acceptable performance. However, in practical designs, a bandwidth wider than that is required to provide some safety margin.



(a) Time domain representation



(b) Frequency domain representation

Figure 57 Frequency multiplication effect of a 4× folding amplifier with a front-end sample and hold (sampling period is 0.41μs, signal frequency 1MHz)

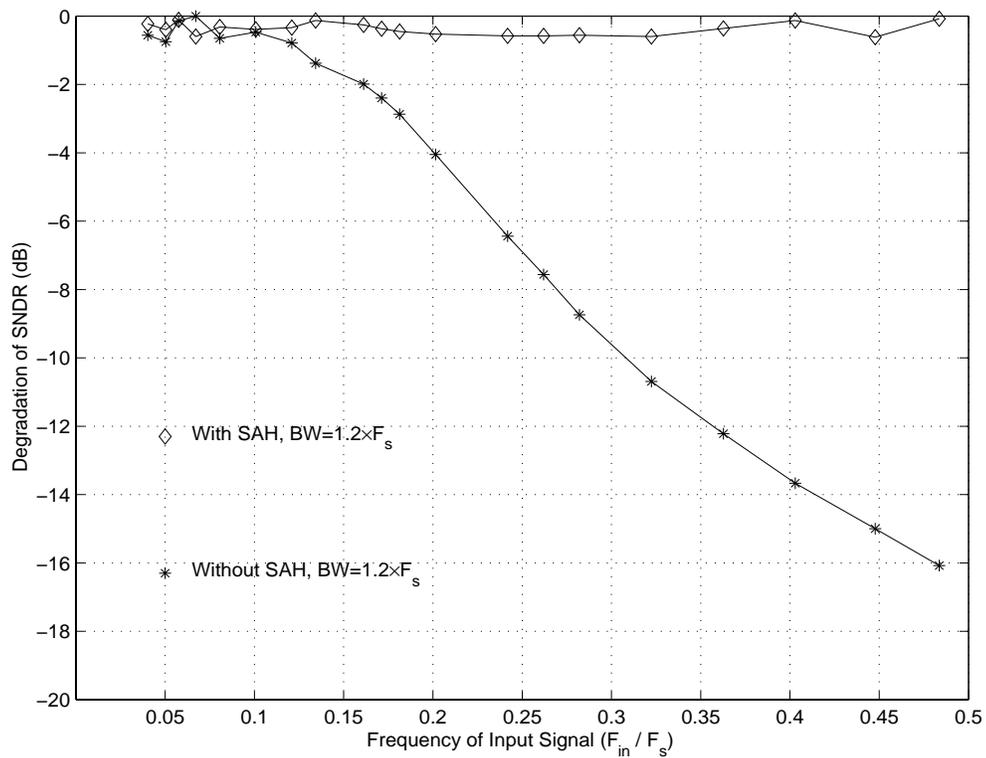
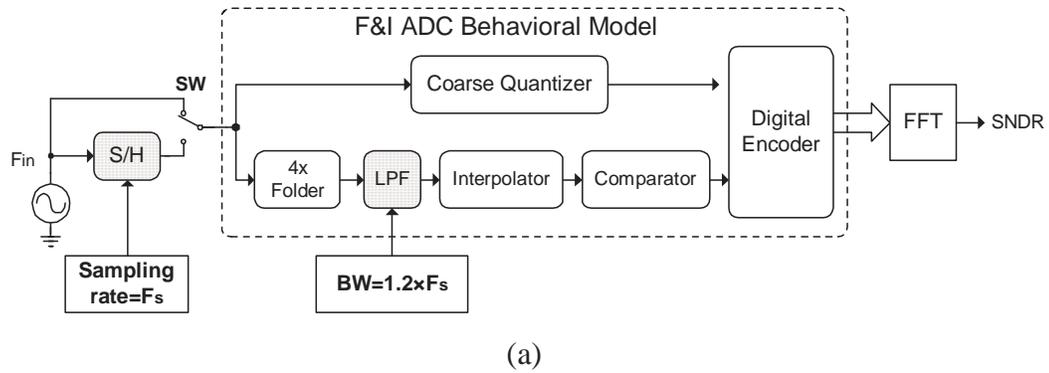


Figure 58 Performance comparison: F&I ADC with/without front-end S/H (folding factor=4). (a) simulation setup (b) results

4.4.2 Current Mode Signal Processing

To further alleviate the slew rate problem, we proposed OTA based folding amplifier. Compare to a conventional voltage based folding amplifier, that OTA based folding amplifier has low impedance internal nodes. Thus the voltage swings on these nodes are much smaller than that of a voltage-mode folding amplifier. Thus, the slew rate problem is also alleviated in our proposed transconductance-mode folding amplifier. The transconductance-mode folding amplifier is described in detail in the next chapter.

Since the output of the transconductance-mode folding amplifier is current, the current mirror based current mode interpolator is a natural choice for interpolation. Figure 59 shows the schematic of a simple $2\times$ current mode interpolator. To build an interpolator with higher interpolation factor (F_I) is similar, one can place more output transistors on the right hand side. As the interpolation factor F_I increases, the total gate-source capacitance C is also increased. C is proportional to $F_I + F_I^2$. Thus, interpolators with higher interpolation factor usually have lower bandwidth.

In comparison with voltage mode interpolator, current mode interpolator do not have delay mismatch between different outputs, because the delay from gate to drain is almost the same for each of the transistors sharing the same gate node. However, unlike voltage mode resistive interpolators, monotonicity is not guaranteed in current mirror based interpolators. As F_I increases, the bandwidth of current mode interpolator decreases, since the loading effect becomes more significant with more transistors connected to the shared gate node.

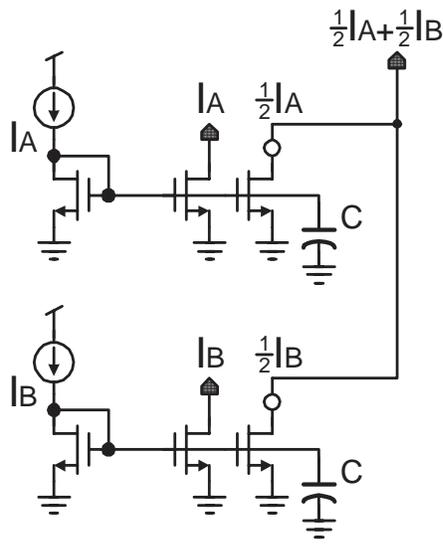


Figure 59 Current mirror based interpolator (C is the total gate-source capacitance)

4.5 F&I ADC System Level Consideration

Given the specifications of accuracy (resolution) and speed (sampling rate), there are many possible ways to implement a F&I ADC, but what is the criteria to choose a proper folding factor (F_F) and interpolating factor (F_I)? Before circuit level design, a designer must make architecture choice, i.e., with or without S/H, and determine optimally system level parameters, such as folding factor F_F , interpolating factor F_I and number of primary folds N_F . Because F&I ADCs' resolutions are usually low, thermal noise does not have significant impact on performance.

A 7-bit 300MS/s F&I ADC is used as an example here to elaborate the system-level design. This section describes how the folding factor, interpolating factor and number of primary folds can be determined from a given set of F&I ADC specifications.

4.5.1 Folding Factor

For an F&I ADC with resolution of N -bit and folding factor of F_F , the number of comparators for the fine and coarse quantizers are $2^N/F_F + 1$ and F_F (including out-of-

range detection¹), respectively. Table I shows the number of comparators required to implement F&I ADCs with different resolutions.

The selection of folding factor involves cost and speed tradeoffs. On the one hand: Higher F_F requires less number of comparators. On the other hand, folder bandwidth is roughly inversely proportional to the folding factor. Higher folding factor results in lower bandwidth. The folding factor cannot be arbitrarily increased, and the reason is explained below.

Here we consider a typical differential-pair based folder as an example. In such a folder, the number of differential pairs is equal to the folding factor, and one more differential pair is used as a dummy². To fully utilize the tail current swing, the reference voltage difference, ΔV_{REF} , between two adjacent reference voltages in a folder should satisfy Eq. (4.1). The relationship between the ADC full swing (V_{FS}) and ΔV_{REF} should satisfy

$$V_{FS} = F_F \cdot \Delta V_{REF} \quad (4.2)$$

Because ΔV_{REF} should satisfy (3) and the V_{FS} is fixed, in our example it is 1.6V, thus the folding factor of 16 is out of consideration, otherwise the gate-source voltage would be too low and transistors would operate in weak inversion.

Table 4 shows the bandwidth requirement on the folders in F&I ADC with different resolutions. We choose SNDR, which is widely used in evaluation of ADC performance and can be easily calculated through FFT, as the performance target. The results are from [51] and also verified by our behavioral model simulations. If we allocate a 2dB budget of SNDR degradation for the folder bandwidth limitation, and the desired bandwidth of the 7-bit F&I ADC is Nyquist frequency, which is 150MHz (f_{in}) for 300MS/s sampling rate, the minimum folder bandwidth can be determined through behavioral simulation. As shown in Table 4, a 4× folder requires 1.2GHz bandwidth and

¹ In some systems with an pre-amplifier preceding the ADC, an out-of-range indicator is desired to adjust the gain of the pre-amplifier to a proper value. Out of range is TRUE when under- and over-flow happens.

² Dummies are used to ensure the slopes of folder at boundaries are identical with other internal slopes

that number is 1.65GHz for an $8\times$ folder. These bandwidths are very difficult, if not impossible, to achieve in MOS technology.

We need to look at other ways, i.e., a front-end S/H, to alleviate this bandwidth challenge. Through the behavioral model simulation results shown in Figure 58, we can observe the S/H's effect on the folder bandwidth requirement in an F&I ADC. If a front-end S/H is used, the SNDR degrades less than 1dB in the whole Nyquist range.

The front-end S/H improves the dynamic performance of the F&I ADC system. However, the tradeoff is that the sample-and-hold circuit itself may introduce distortion and increase power consumption. Also the design of a S/H operating at very high frequency with acceptable accuracy is a tough task.

Nevertheless, to design a high speed F&I ADC operating at Nyquist rate, front-end S/H is practically mandatory, otherwise the bandwidth requirements for all analog preprocessing blocks, i.e., folder, interpolator, comparator preamplifier, would be too high and might not be feasible with real circuits.

Based on above discussion, a front-end S/H is used and the folding factor is set to be 4. Folding factor of 8 is not chosen because 360MHz is still a challenge for CMOS folding amplifiers. High folding factor folders, implemented with cascaded stages of low folding factor folders, find their applications in high resolution low speed F&I ADCs [96]. Note, however, this cascaded approach does not alleviate the inherent frequency multiplication challenge.

4.5.2 Interpolation Factor and Number of Folders

To circumvent the delay mismatch problem, we prefer the current mode interpolation based on current mirrors. Note the aforementioned bandwidth requirement on the folder also applies to the interpolator, i.e., the bandwidth of the interpolator must also be higher than 360MHz, because the bandwidth of the whole analog preprocessing block should be larger than $1.2\times$ sampling rate. The next task is to determine the interpolation factor F_I .

A 7-bit ADC needs to resolve 128 zero crossings, and because $F_F=4$, thus 4 zero crossings can be resolved from each folding signal, the number of total folding signals yields: $128/4=32$. If we choose the number of folders to be 2, then the interpolation

factor should be $32/2=16$, which is the most efficient solution in terms of chip area and power consumption. Unfortunately this is not feasible, however, because of concerns on the interpolator bandwidth and folder non-linearity. First, if $F_I=16$, a bandwidth of 360MHz or higher would be impossible because of the loading effect on the shared gate node of the current mirror. Second, Interpolation zero crossing points shift due to the non-linear transfer characteristic of the folder would produce non-even spacing (see Fig. 12), which would degrade the DC linearity of the F&I ADC. Based on above observations, we increase the number of folders (N_F) from 2 to 4, thus the interpolator factor is set to be 8.

We have made the decision on the S/H and determined system parameters: $F_F=4$, $F_I=8$, $N_F=4$.

4.5.3 Interpolator Choice

In the signal chain, the interpolator sits between the folder block and the comparator block. The choice of interpolator affect the other two, i.e., if the interpolator is current mode, the folder must be a transconductance stage, and the comparator must be a current comparator.

For voltage mode resistive interpolators, interpolation error caused by the delay difference, and the bandwidth limitation would become unacceptable if interpolating factor is too high. The upper limit of F_I depends on the ADC resolution and speed specifications, and the value of interpolation resistance (R) and comparator input capacitance (C). On the other hand, if the F_I is determined and C is fixed, i.e., size of comparator input transistors must be large enough to minimize offsets, the interpolation resistor value has an upper limit. From the behavioral simulation results shown in Figure 56. For 100MHz input signal, the RC constant need to be smaller than 4ps to ensure less than 2dB of SNDR degradation. If the comparator input capacitance is assumed to be 0.1pF, the interpolation resistance should be less than 40Ω . With $F_I=8$, the total interpolation resistance is 320Ω . To drive such a low impedance load, power hungry buffers must be inserted between the folder block and interpolator block.

We consider a current mode interpolator based on current mirrors, shown in Figure 59. One important design requirement on this block is the bandwidth must be higher than 360MHz ($1.2\times$ sampling rate). Transistor size in the current mirror must be large enough to ensure the mismatch does not seriously degrade the linearity of the F&I ADC.

4.5.4 F&I ADC Design Guidelines

F&I ADC system level design involves tradeoffs of circuitry complexity and performance. There is no single optimum strategy for all cases with different performance requirements. The following are some general guidelines to make the architecture choice, and determine system parameters.

For F&I ADC aimed to high sampling rate high bandwidth applications, i.e. input bandwidth equal to or greater than Nyquist rate, a front-end S/H is mandatory.

Adopting high folding factor in F&I ADC means more area (and power consumption) savings. However, one should consider the sacrifice on the input bandwidth. In general, low folding factor is recommended for high sampling rate high bandwidth F&I ADCs.

Interpolators with lower F_I have wider bandwidth. To alleviate the effect of RC constant, one can decrease the interpolation resistance or reduce the comparator input transistor size. However, buffers are required to drive those low impedance interpolation resistors. By using smaller size transistors, offset results.

A proper analog preprocessing gain is needed to circumvent the comparator offsets, which are reduced by the analog preprocessing gain when referred to the input. It cannot be too high, otherwise the bandwidth would be limited. In our 7bit F&I ADC example, the analog preprocessing gain is $2V/V$.

To achieve higher bandwidth, F_F and F_I have to be reduced. The number of primary folds must be increased to implement F&I ADCs with higher resolutions. Also by increasing N_F , the interpolation error caused by the nonlinear slope of folder is decreased.

The ultimate resolution of an F&I ADC is limited by the component mismatches, i.e. resistor and transistor mismatches. A designer has to estimate these nonidealities from process parameters. Behavioral simulation must be performed to make sure these

nonidealities would not deteriorate the performance significantly. For an F&I ADC to meet the specified resolution and speed requirements, boundary limits of all these nonidealities can be determined through behavioral simulation.

CHAPTER V

TRANSISTOR LEVEL CIRCUIT DESIGN

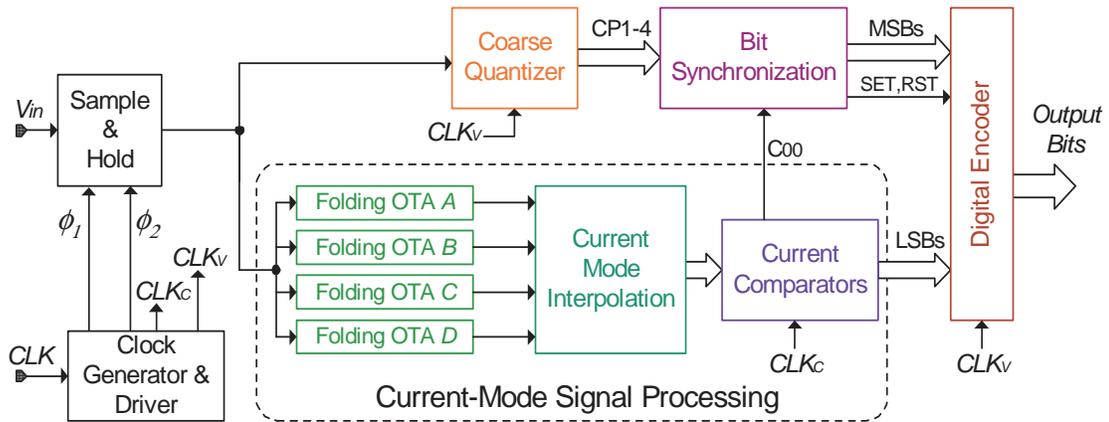
In previous chapter, it is explained why the S/H is required for a wide bandwidth F&I ADC, and system parameters of a 7-bit 300MS/s F&I ADC are obtained. Transistor level design of major building blocks is discussed in detail next.

5.1 F&I ADC with S/H and Current Mode Interpolation

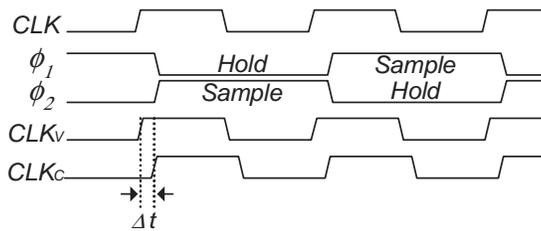
The system block diagram of the proposed wide bandwidth F&I ADC system is presented in Figure 60. The use of S/H and current mode signal processing are two major characteristics of this system. Current mode signal processing is carried out by combining the OTA-based folding amplifier with current mirror based interpolator to achieve wide input bandwidth. The aforementioned S/H block precedes the F&I ADC to alleviate the frequency multiplication effect and boost the dynamic performance.

Figure 61 illustrates the architecture of the time interleaving S/H. The interleaving scheme has two advantages. First, the acquisition time available for each T/H is twice that which would be available if a single S/H circuit was used. This makes the design of the T/H circuit more manageable. A second important advantage of interleaving is that the final output of the S/H is a 'held' signal for an entire clock interval. This dramatically improves the settling behavior of the folding amplifiers.

A potential problem with interleaving is the mismatch between the two channels. There are three possible sources of mismatch. Any timing mismatch or gain mismatch results in an intermodulation between the input frequency and one half of the sampling frequency. Any offset mismatch results in a tone at half the sampling frequency. Clock edge reassignment circuit is used to suppress timing mismatches in two interleaving paths.



(a)



(b)

Figure 60 F&I ADC with a front-end S/H. (a) block diagram (b) clock timing

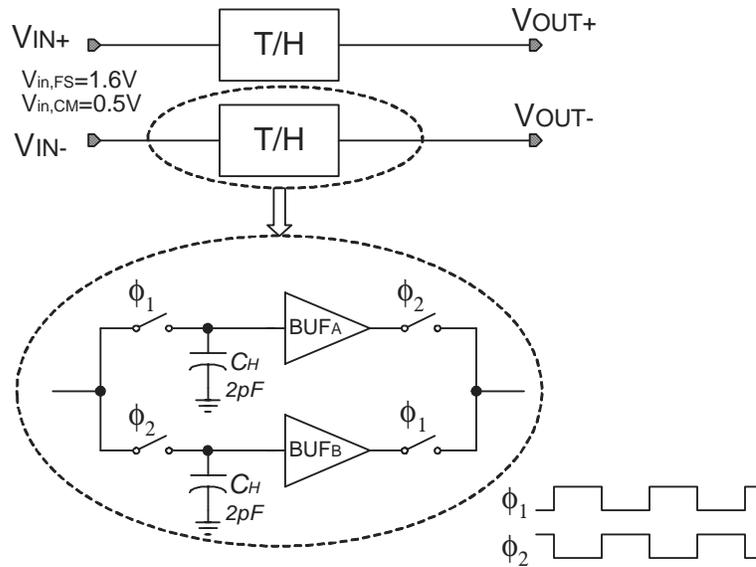


Figure 61 Sample and hold circuit topology

5.2 Sample-and-Hold

The function of the S/H circuit is to track/sample the analog input signal and to hold that value while subsequent circuitry digitizes it. In MOS technologies, this function is implemented by storing the input signal voltage on a sampling capacitor through a MOS transistor switch and holding the voltage for subsequent stages usually with some active circuitry such as op amps. Since the achievable precision of the S/H function is limited by the initial accuracy of the sampled signal, the fundamental accuracy is limited by the accuracy of the sampling circuit, not the active circuitry which holds the value.

The limitations of sampling can be studied with a simple MOS S/H circuit implemented with one MOS transistor and one capacitor as shown in Figure 62. During the sampling phase of the clock, the voltage on the sampling capacitor C_S tracks the input voltage through the MOS transistor switch. Then, in the next clock phase when the clock V_g goes low at time instant t_s , the transistor turns off, and the input voltage is sampled and held on the capacitor for further processing.

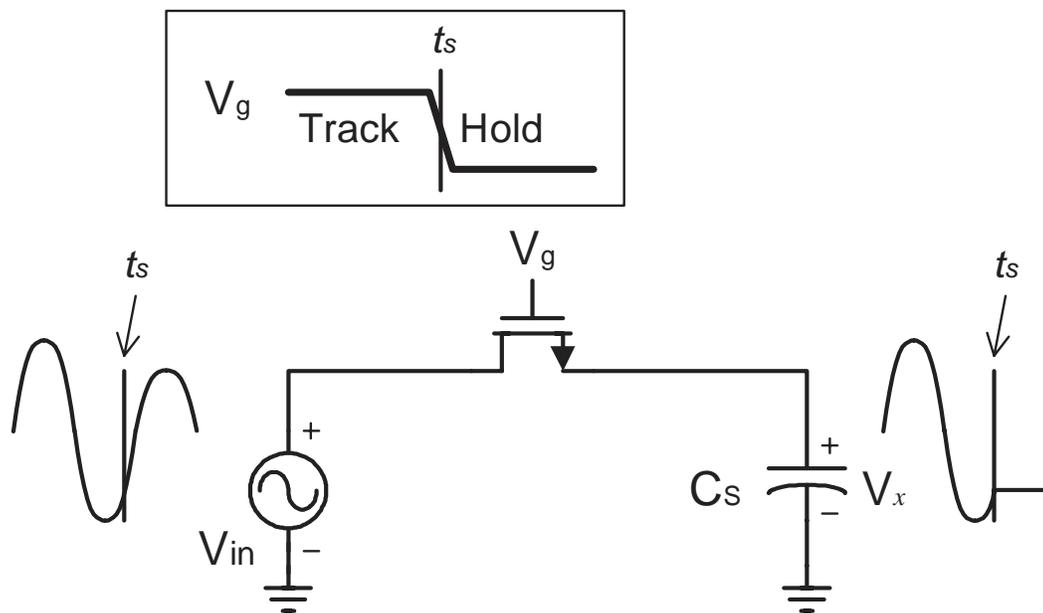


Figure 62 A simple MOS S/H circuit

In this simple MOS S/H circuit, a number of non-idealities produce errors, and they can be categorized into two groups, deterministic components and random components. The term “deterministic component” refers to an error source whose relationship with the signal is known to be consistent from sample to sample, such as the finite bandwidth in the sample mode, the signal-dependant charge injection from the MOS transistor, clock feedthrough. Various circuit techniques have been developed to cancel or to suppress these effects to achieve high sampling accuracy (Table 5).

TABLE 5 Deterministic error components and possible solutions

Error Sources	Possible Solution/Techniques
Finite Bandwidth	Advanced technologies to lower the switch on-resistance Gate voltage bootstrapping [7]
Charge Injection	Bottom plate sampling [52],[89] Dummy switch [42]
Clock Feedthrough	Differential signal path [13]

The other error components are “random errors”, errors that may be unpredictable from sample-to-sample, and the dominant source in the circuit of Figure 62 is thermal noise. In conventional resistors, noise is generated due to the random thermal motion of electrons and is unaffected by the presence or absence of direct current. Therefore, this noise appears as additive noise to the signal. Another noise source present in MOS transistor is the Flicker noise or “1/f noise” whose noise spectral density has a 1/f frequency dependence.

Within the sample and hold circuit, two noise sources are significant: the sampling switches and the sample and hold amplifier. The sampling switch is used to sample the input signal onto a sampling capacitor. As this happens, noise from the sampling switch is sampled with it onto the sampling capacitor. This source of thermal noise is commonly referred to as kT/C noise because the noise power is proportional to kT/C where C is the size of the sampling capacitor. The sample and hold amplifier also contributes thermal noise degradation to the signal being processed. The contribution of the sample and hold amplifier is also inversely proportional to a capacitance. In a single stage amplifier, it is inversely proportional to the load capacitance. In a Miller compensated amplifier it is inversely proportional to the compensation capacitance.

5.2.1 Time Interleaved Sample-and-Hold

The proposed S/H circuit employs a pseudo-differential architecture consisting of two single-ended S/H circuits, as shown in Figure 63(a). The schematic of each single-ended S/H circuit is similar to the one used in [42]. To reduce the distortion caused by body effect, a PMOS source follower is used as the buffer. An important feature of this architecture is that it uses two interleaved track and hold (T/H) circuits operating at half of the sampling frequency. These are used in a time-interleaved manner to achieve one S/H function.

Bootstrapping is usually employed to sample and hold to alleviate the signal dependent charge injection problem, but the bootstrapping circuit itself may become the speed bottleneck when sampling is as high as 300MHz. Also considering the resolution of this F&I ADC is just 7bit, therefore bootstrapping is not used here.

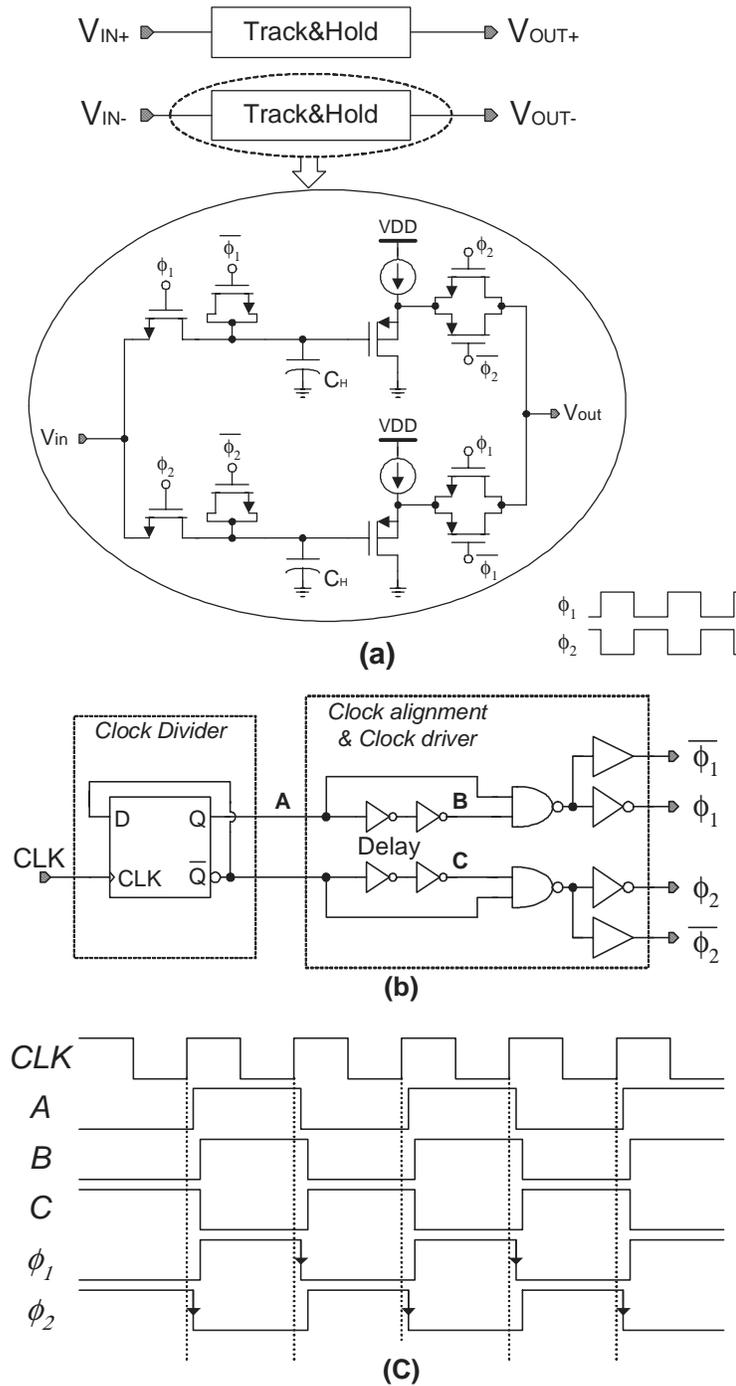
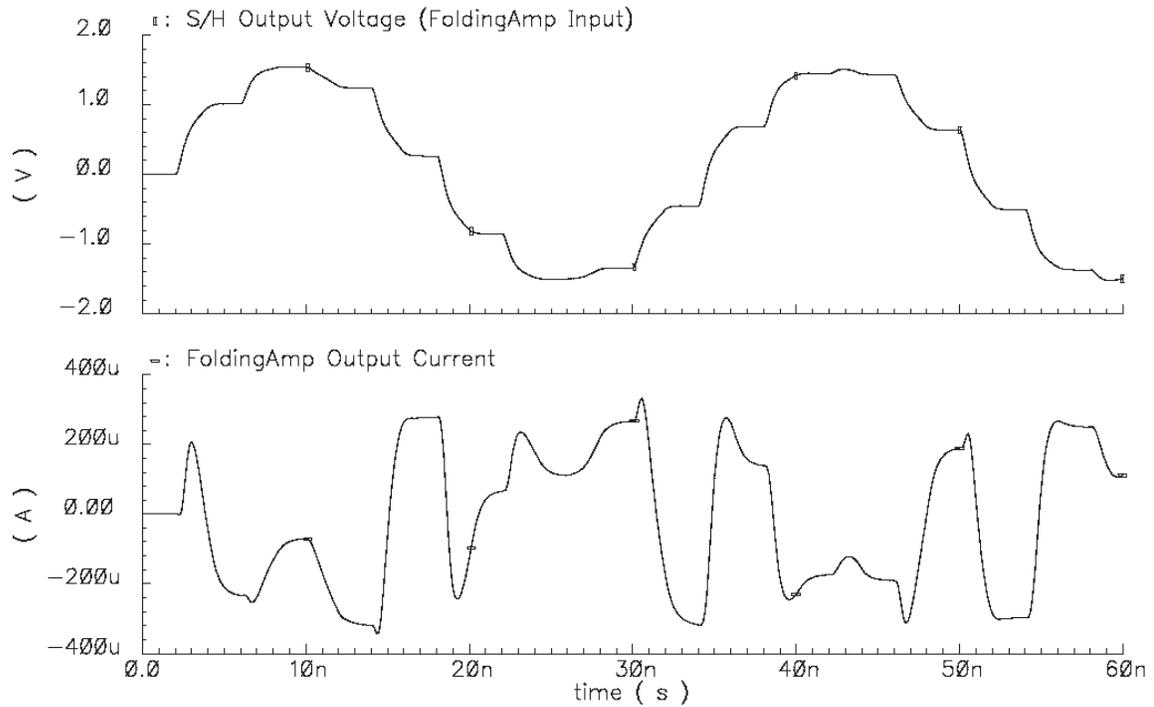
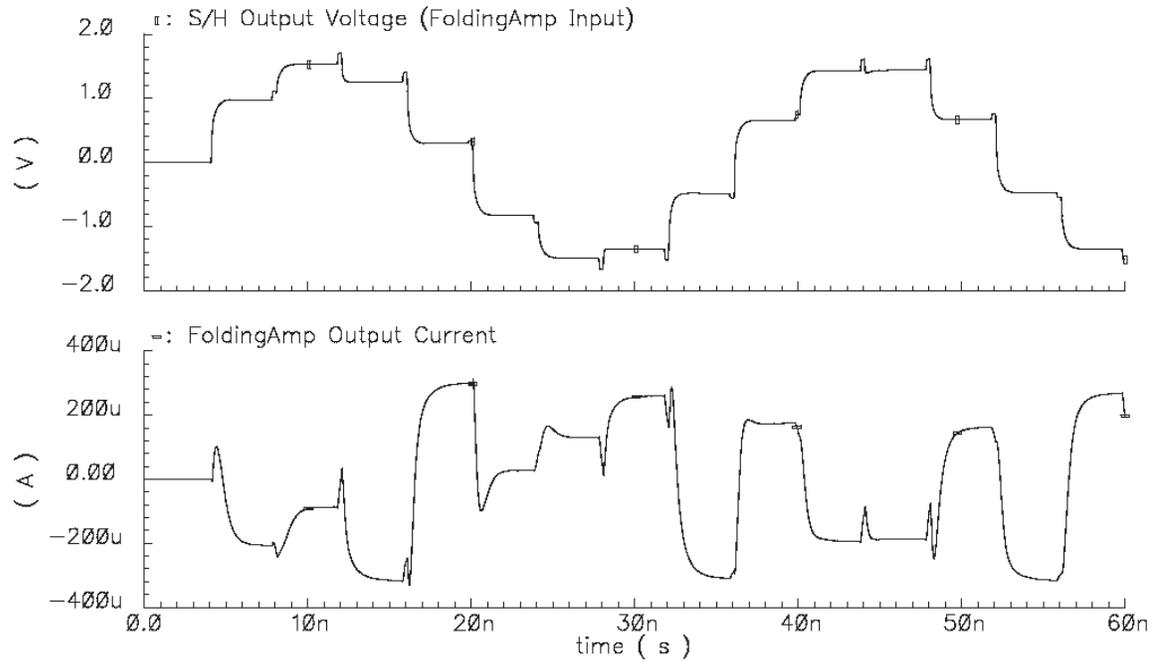


Figure 63 The time-interleaving S/H circuit and clock alignment block (a) block diagram and simplified schematic the whole S/H building block, (b) clock alignment block, (c) timing of the clock alignment circuit



(a) Without time-interleaving, settling of the folding amplifier is not completed



(b) With time-interleaving, the folding amplifier has more time to settle

Figure 64 Comparison of the sample-and-hold with/without time-interleaving

The basic ideal of time-interleaving is described in Chapter II Section 5. The same method can be applied to the design of a high speed S/H. The interleaving scheme has two advantages. First, the acquisition time available for each T/H is twice that which would be available if a single S/H circuit was used. Second, the final output of the S/H is a 'held' signal for an entire clock interval. This dramatically improves the settling behavior of the folding amplifiers, as shown in Figure 64.

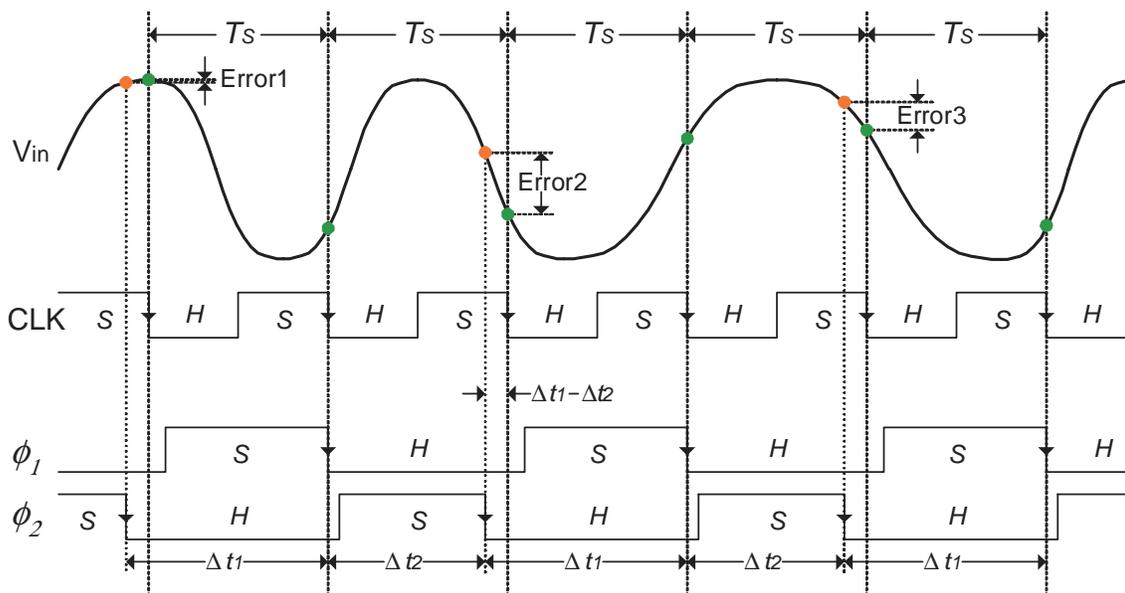


Figure 65 Sampling error caused by timing mismatch

A potential problem with interleaving is the mismatch between the two channels. Any timing mismatch or gain mismatch results in an intermodulation between the input frequency and half the sampling frequency. Any offset mismatch results in a tone at half the sampling frequency. Clock edge reassignment circuit should be used to suppress timing mismatches in two interleaving paths (Figure 65). Among all these mismatch the timing mismatch is most difficult to calibrate, because the other can be corrected in the digital domain.

From Figure 23 we can draw the following conclusion: For a 7-bit ADC to achieve greater than 50dB of SFDR at 100MHz input frequency, timing mismatch should be smaller than 8ps and the gain mismatch must be controlled within 0.5%

Each switch consists of a NMOS transistor in series with a dummy driven by the complement of the switch clock. Charge injection cause distortion by adding/removing charge, which is signal dependent, on the hold capacitor (C_H) when the switch shuts off. The value of the holding capacitor affects the distortion and speed. Size of switches and holding capacitors are determined to yield fast speed with a moderate distortion.

The low-input common-mode voltage of 0.5V allows a larger gate overdrive to turn on the switch, which lowers track-mode distortion effect from the nonlinear channel resistance. The source terminal of the source follower transistor is connected to well of the PMOS to eliminate the non-linear body effect. Simulations show that when acquiring samples of a 160MHz 1.6Vpp (3.2Vpp differential) sine wave at 300MSample/s, the S/H delivers samples to the quantizer input with third-harmonic distortion of about -57dBc , which is suitable for a 7-bit ADC.

5.2.2 Analysis of Non-ideal Effect of Multi-channel Architectures

Multi-channel parallelism in a sample-and-hold or ADC can increase conversion speed by the number of channels, but there are well known problems such as *offset*, *gain* and *timing* mismatches among the channels which do not arise in digital systems [3], [13],[33],[70],[76].

Timing mismatch

The effect of timing mismatch among the channels has been analyzed and documented [33]. The analysis can be summarized as follows. Let the original sampled data sequence $S = [x(t_0), x(t_1), x(t_2), \dots, x(t_m), \dots, x(t_M), x(t_{M+1}), \dots]$ be divided into M subsequences $S_0, S_1, S_2, \dots, S_{M-1}$ as follows:

$$S_0 = [x(t_0), x(t_M), x(t_{2M}), \dots]$$

$$S_1 = [x(t_1), x(t_{M+1}), x(t_{2M+1}), \dots]$$

...

$$S_m = [x(t_m), x(t_{M+m}), x(t_{2M+m}), \dots]$$

...

$$S_{M-1} = [x(t_{M-1}), x(t_{2M-1}), x(t_{3M-1}), \dots] \quad (5.1)$$

It's clear that the m -th subsequence S_m is obtained by uniformly sampling the signal $x(t + t_m)$ at the rate $1/(MT)$. To reconstruct the original sequence S , we first insert $(M-1)$ zeros between samples in all subsequences S_m , for $m=0$ to $M-1$, i.e.

$$\bar{S}_m = [x(t_m), (M-1)\text{zeros}, x(t_{M+m}), 0, 0, \dots] \quad (5.2)$$

we can represent the original sequence, S , as

$$S = \sum_{m=0}^{M-1} \bar{S}_m z^{-m} \quad (5.3)$$

Then, the digital spectrum, $X(\omega)$, of S can be represented as

$$X(\omega) = \frac{1}{M \cdot T} \cdot \sum_{m=0}^{M-1} \left[\sum_{k=-\infty}^{\infty} X^a \left(\omega - \frac{2\pi k}{M \cdot T} \right) e^{j(\omega - 2\pi k / MT)t_m} \right] e^{-jm\omega T} \quad (5.4)$$

Let r_m be the ratio of $mT - t_m$ to the average sampling period T , i.e., let

$$t_m = m \cdot T - r_m \cdot T \quad (5.5)$$

then Eq. (5.4) can be rewritten as

$$X(\omega) = \frac{1}{T} \cdot \sum_{k=-\infty}^{\infty} \left[\frac{1}{M} \sum_{m=0}^{M-1} e^{-j(\omega - 2\pi k / MT)r_m T} e^{-jkm(2\pi/M)} \right] X^a \left(\omega - \frac{2\pi k}{M \cdot T} \right) \quad (5.6)$$

Since the Fourier transform of the sinusoidal input with the frequency f_0 , is

$$X^a(\omega) = 2\pi\delta(\omega - \omega_0) \quad (5.7)$$

and $\omega_0 = 2\pi f_0$,

Eq. (5.6) becomes

$$X(\omega) = \frac{1}{T} \cdot \sum_{k=-\infty}^{\infty} A(k) 2\pi\delta \left(\omega - \omega_0 - \frac{2k\pi}{MT} \right), \quad (5.8)$$

where

$$A(k) = \sum_{m=0}^{M-1} \left(\frac{1}{M} e^{-jr_m 2\pi f_0 / f_s} \right) e^{-jkm 2\pi / M} \quad (5.9)$$

From Eq. (5.8) and (5.9), we can find some important consequences of timing offset in the multi-channel sample-and-hold or A/D converter with sinusoidal input. First, from

(5.9), the sequence $A(k)$ is periodic on k with the period M , hence the spectrum $X(\omega)$ given by Eq. (5.8) is periodic on ω with a period equal to $2\pi/T (= 2\pi f_s)$. The M line spectra uniformly spaced on the frequency axis is comprised in one period of the spectrum with neighboring spectra separated by the amount of f_s/M . The main signal is located at f_0 and the magnitude is $|A(0)|$, while the m -th spectral line is located at $f_0 + (M + m)f_s$ and with magnitude $|A(m)|$ as shown in Figure 66. Since $A(k)$ in Eq.(5.9) is a discrete Fourier transform of the sequence of $\left[\frac{1}{M} e^{-jr_m 2\pi f_0 / f_s}, m = 0, 1, 2, \dots, m-1 \right]$, by Parseval's theorem,

$$\sum_{k=0}^{M-1} |A(k)|^2 = 1 \quad (5.10)$$

Therefore, the signal-to-distortion ratio (S/D), due to timing offset sampling in the multiple-channel[33], can be expressed as

$$SDR = 10 \log_{10} \left(\frac{|A(0)|^2}{1 - |A(0)|^2} \right) \quad (\text{dB}) \quad (5.11)$$

Let's consider the A/D converter with two channels. By definition of r_m , $r_0 = 0$ and r_1 is in the range $(-1, +1)$, hence,

$$|A(0)|^2 = \cos^2(\pi r_1 f_0 / f_s) \quad (5.12)$$

and from Eq. (5.11), we have

$$SNR = 20 \log_{10} \left(\frac{|\cos(\pi r_1 f_0 / f_s)|}{|\sin(\pi r_1 f_0 / f_s)|} \right) \quad (5.13)$$

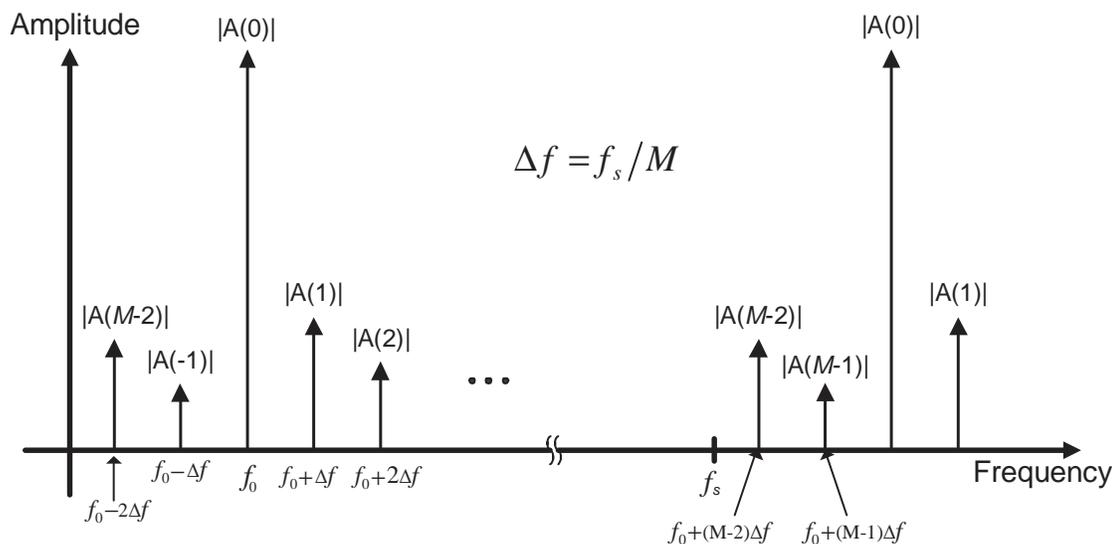


Figure 66 Digital spectrum of non-uniformly sampled sinusoids

5.3 OTA-based Folding Amplifier

In order to generate the folding signal, a circuit used in bipolar folding converters (see Figure 31) [75] is converted to CMOS. The circuit is shown in Figure 67(a). The circuit consists of 5 differential pairs with the outputs of the odd- and even-numbered differential pairs cross coupled. The inputs of the differential pairs are connected to the converter input voltage and reference voltages ($V_{REF1} \dots V_{REF5}$) generated by a resistor ladder. The currents are summed at the output nodes through resistors.

The differential output voltage versus input voltage is plotted in Figure 67(b). The tops of this folding signal are somewhat rounded compared to a triangular shape. A typical range of V_{in} is $1 \dots 2V_{pp}$, and since the 5 input windows of the differential pairs have to fit within this voltage, the transistors have small $V_{gs} - V_t$ values and thus operate in moderate or weak inversion. The consequence of this is a large W/L ratio for the input devices and small tail currents of the differential pairs. The resulting parasitic capacitances at the output nodes are large (maybe several pF). On the other hand, the values of the resistors R in Figure 67(a) have to be large (a few k Ω) to allow large output voltages. The latter is required to reduce sensitivity to offsets in the rest of the converter. Note that the 4 times folded signal has a bandwidth of 7-10 (see Table 4 in Chapter 4) of

the full swing input signal bandwidth due to the nonlinear folding operation. The large R and C_{par} therefore give rise to serious analog bandwidth limitations.

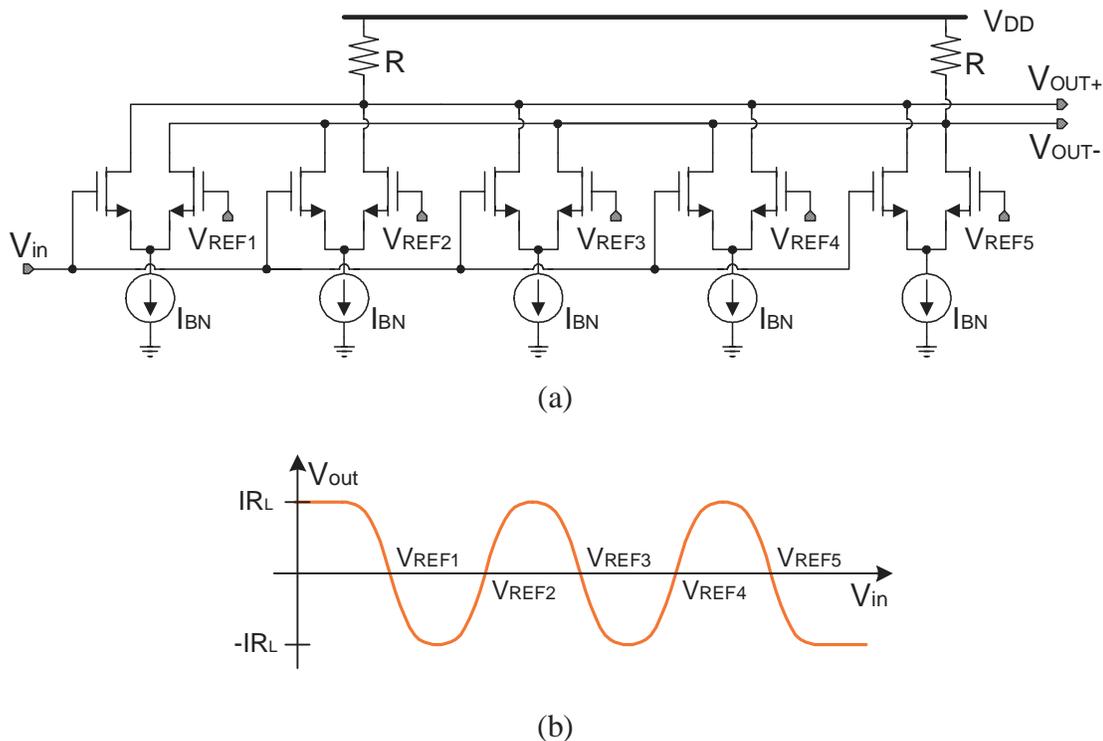


Figure 67 Differential pair based CMOS folding amplifier (a) schematic (b) transfer characteristics

To avoid this problem, an OTA based folding amplifier is proposed. The block diagram and basic waveforms of the OTA based folding amplifier is presented in Figure 68. Here five OTAs are used to implement a $4\times$ folding amplifier (in fact, it is folding by 5, but only 4 are useful). When the input voltage sweep from the lower to upper limit of the ADC input full scale, OTA1, OTA3, OTA5 will generate positive slopes while OTA2 and OTA4 will generate negative slopes. The combination of all five OTA output currents produce a “pseudo-sinusoidal folding” transfer characteristic (Figure 68b). A PMOS common gate amplifier is used as current buffer to reduce the loading effect at the current summation nodes. By changing the value of five reference voltages

connected to these five OTAs, we can obtain different folding transfer characteristic curve with different “phase”, such as *FI* and *FQ*.

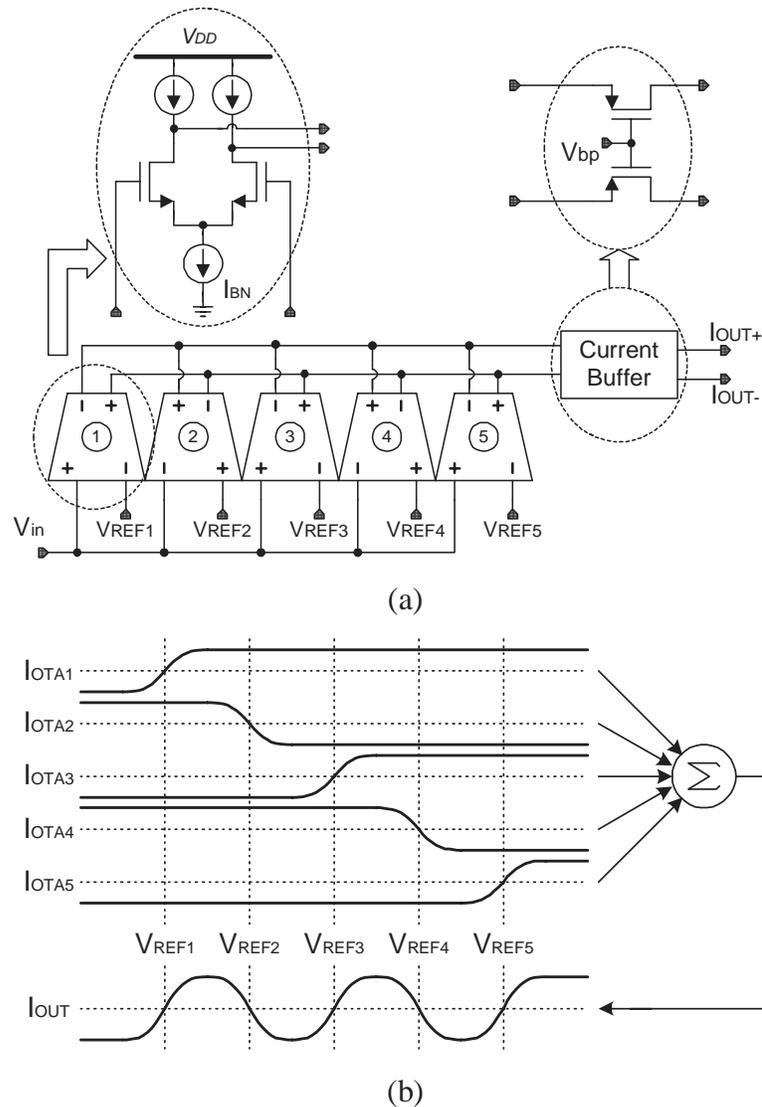


Figure 68 Basic idea of the OTA based folding amplifier (a) schematic (b) transfer characteristics illustration

The aforementioned OTA can be implemented by a simple differential pair (Figure 68a). A simplified schematic of the folding amplifier is shown in Figure 69. For a given input, all but one of the differential pairs is saturated. The one differential pair that is

active produces the shape of the fold around the reference voltage connected to one of its inputs. The positions zero-crossing points are controlled by reference voltages, therefore the offset of each differential pair affect the linearity of the ADC directly. Offset of differential pairs can be predicted by the law of $1/\sqrt{WL}$ [68]. For normal gate-source potentials, the mismatch in threshold voltage dominates the transistor performance. The variance of the offset voltage is

$$\sigma(V_{T0}) = \frac{A_{VT0}}{\sqrt{WL}} \quad (5.14)$$

where σ is the standard deviation of the offset voltage, A_{VT0} is a process dependent parameter, which is inversely proportional to gate oxide thickness. For $2.5\mu\text{m}$ CMOS N-channel transistor, $A_{VT0}=30\text{mV}\mu\text{m}$, for $2.5\mu\text{m}$ CMOS P-channel transistor, $A_{VT0}=35\text{mV}\mu\text{m}$. Lower geometry CMOS processes can achieve better transistor match. For $0.35\mu\text{m}$ CMOS N-channel transistor, $A_{VT0}<8\text{mV}\mu\text{m}$.

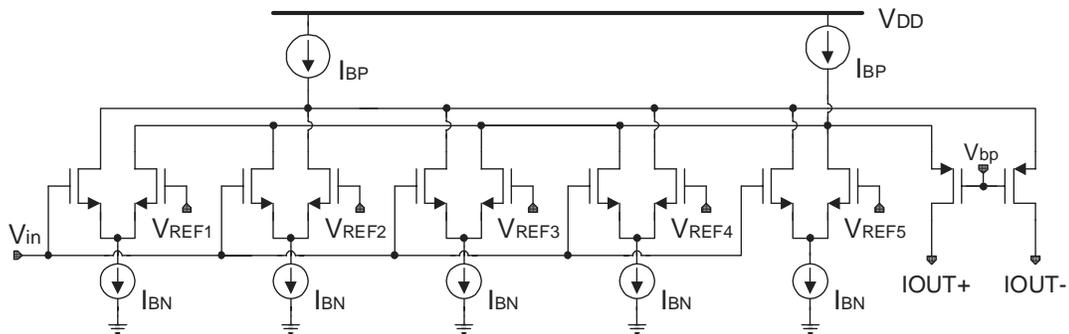


Figure 69 Simplified schematic of the folding amplifier based on folded-cascode OTA

Transistors size must be large enough to make sure the offset voltage is much smaller than one LSB of the ADC. Special auto-zeroing or offset canceling scheme also can be used to reduce the offset [53], thus improving INL and DNL of the ADC, but unfortunately the auto-zeroing process takes long time so that they are suitable only for very low speed ADCs.

Although the circuits in Figure 67(a) and Figure 69 both use cross coupled differential pairs to generate folding waveforms, there are important difference between them. The impedance on the summing nodes V_{out+} and V_{out-} are different in these two cases. In the OTA folding amplifier case, this node impedance is low (a few hundred ohms) compare to the voltage mode folding amplifier (a few kilo ohms). Since the parasitic capacitances are similar in both cases, the OTA based folding amplifier has much wider bandwidth than the voltage mode folding amplifier.

In order to generate fully differential folding current signals, the voltage difference, ΔV_{REF} , between two adjacent references voltages in a folding block should satisfy

$$\Delta V_{REF} = |V_{REF}(i+1) - V_{REF}(i)| > 2 \cdot \sqrt{\frac{2I_{BN}}{\beta}} = 2\sqrt{2}(V_{GS} - V_T) \quad (5.15)$$

The above expression means that, the linear regions of two adjacent differential pairs should not overlap with each other.

5.4 Current-Mode Interpolator

As mentioned in chapter III, there are two different ways to implement an interpolator. If the output of folding amplifier is a voltage signal, the resistor based voltage mode interpolator is a natural choice. However, in our case, the output of OTA based folding amplifiers are current signals, thus current mirrors are employed to perform interpolation.

The ratio of output and input currents of a current mirror can be controlled by the size ratio of transistors. This is the basic principle of a current mode interpolator based on current mirrors. Current mirrors have wide bandwidth, thus they are suitable building blocks for high-speed design.

Figure 70 shows the schematic of a current mirror based interpolator. The accuracy of such an interpolator is limited by the mismatch of current mirrors. Obviously the transistor mismatch depends on the size of transistors. Although minimum sized transistors may achieve high speed operation due to the smaller parasitic capacitances, they may suffer from large mismatch. In the following section, we will discuss this

tradeoff and derive the minimum size of transistors comprising the current mirror based interpolator. We can expect that minimum size is a function of the F&I ADC resolution.

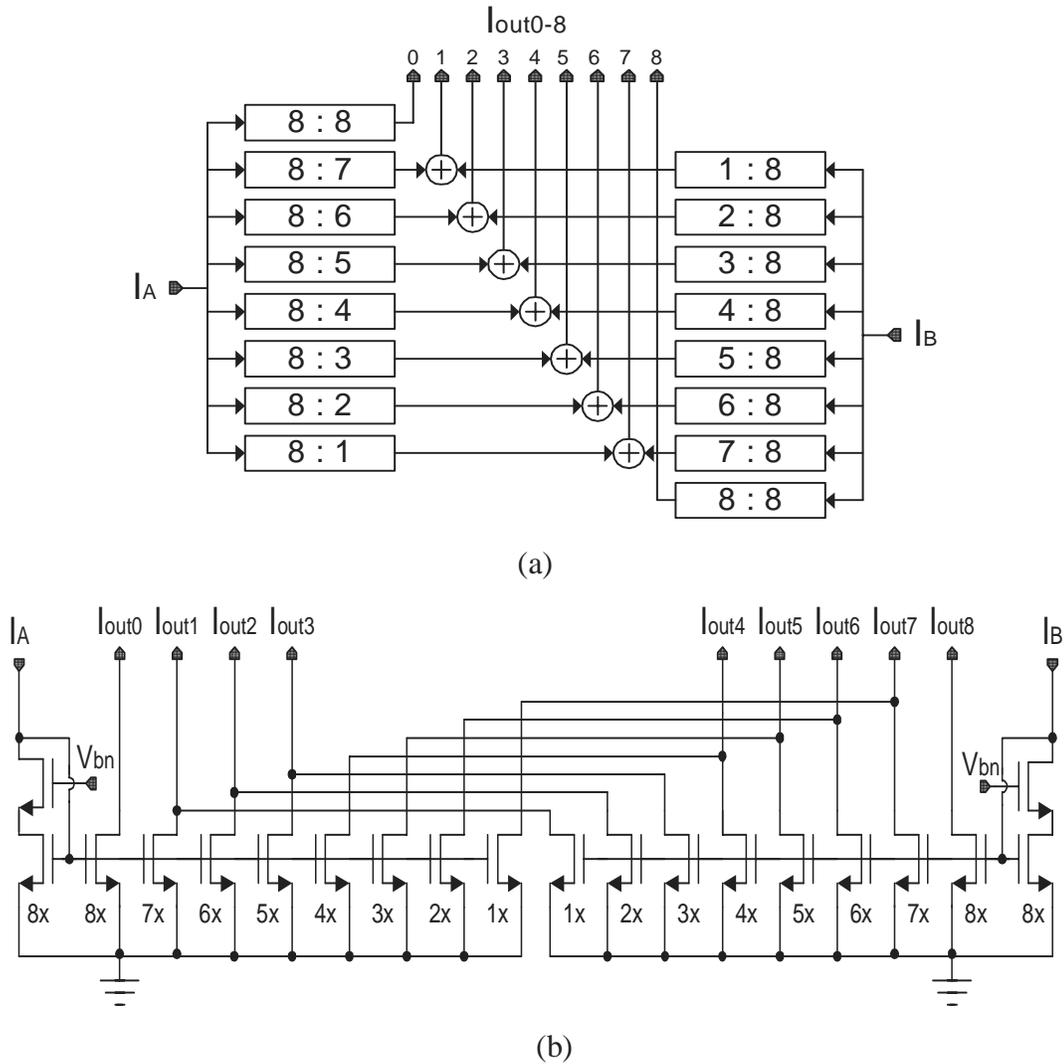


Figure 70 Current mode interpolator (a) block diagram (b) schematic

Offset Calculation

For a current mirror, if we assume the V_T mismatch is dominant and ignore other mismatches, the current mismatch [68] can be described as

$$\frac{\sigma(I_d)}{I_d} = \frac{2\sigma(V_T)}{(V_{GS} - V_T)} \tag{5.16}$$

Next we consider current mismatch of a series of current mirrors with 8 unit transistors as the input and m ($m=1, \dots, 8$) unit transistors (in parallel) as the output. V_{GS} will vary because of the variation of V_T .

For the input branch, the input current is the sum of currents flow through all 8 unit transistors

$$I_A = \frac{1}{2} \beta \sum_{i=1}^8 (V_{GS} - V_{T,i})^2 \quad (5.17)$$

where $\beta = \mu C_{ox} W/L$.

The input current variation ΔI_A is a function of V_{GS} variation and V_T variation,

$$\Delta I_A = \beta \sum_{i=1}^8 (V_{GS} - V_{T,i}) \Delta V_{GS} - \beta \sum_{i=1}^8 (V_{GS} - V_{T,i}) \Delta V_{T,i} \quad (5.18)$$

Now we assume the input currents I_A (and I_B) are deterministic signals, thus $\Delta I_A = 0$, and Eq. (5.18) can be rewritten as

$$\Delta V_{GS} = \frac{\sum_{i=1}^8 (V_{GS} - V_{T,i}) \cdot \Delta V_{T,i}}{\sum_{i=1}^8 (V_{GS} - V_{T,i})} \quad (5.19)$$

Assuming that variances ($\sigma^2(V_T)$) of all threshold voltages are the same. (5.19) yields

$$\sigma^2(V_{GS}) = \frac{\sum_{i=1}^8 (V_{GS} - V_{T,i})^2}{\left[\sum_{i=1}^8 (V_{GS} - V_{T,i}) \right]^2} \sigma^2(V_T) \quad (5.20)$$

When $V_{GS} - V_T(i) \gg \sigma(V_T)$, which is satisfied in real cases, we can assume that all over drive voltages are equal to each other. Thus, (5.20) becomes

$$\sigma^2(V_{GS}) = \frac{\sum_{i=1}^8 V_{OD}^2}{\left(\sum_{i=1}^8 V_{OD} \right)^2} \sigma^2(V_T) = \frac{1}{8} \sigma^2(V_T) \quad (5.21)$$

On the output side, the output current I_m is the sum of currents flowing through m unit transistors, e.g.

$$I_m = \frac{1}{2} \beta \sum_{i=1}^m V_{OD,i}^2 \quad (5.22)$$

The variation of the output current, ΔI_m , is a function of ΔV_{GS} and $\Delta V_T(i)$,

$$\Delta I_m = \beta \sum_{i=1}^m V_{OD,i} \cdot \Delta V_{OD,i} = \beta \sum_{i=1}^m V_{OD,i} \cdot \Delta V_{GS} - \beta \sum_{i=1}^m V_{OD,i} \cdot \Delta V_T(i) \quad (5.23)$$

Because variations of over-drive voltage V_{OD} of different unit transistors are independent with each other, from (5.23) we have

$$\begin{aligned} \sigma^2(I_m) &= \beta^2 \left(\sum_{i=1}^m V_{OD,i} \right)^2 \sigma^2(V_{GS}) + \beta^2 \sum_{i=1}^m V_{OD,i}^2 \sigma^2(V_T) \\ &= (m\beta V_{OD})^2 \sigma^2(V_{GS}) + m(\beta V_{OD})^2 \sigma^2(V_T) = \left(\frac{m^2}{8} + m \right) (\beta V_{OD})^2 \sigma^2(V_T) \end{aligned} \quad (5.24)$$

The output current of the interpolator $I_{out,m}$, is the sum of two output currents I_m and I_{8-m} , (i.e. I_1 combine with I_7 and I_2 combine with I_6 , etc., see Figure 70)

$$I_{out,m} = I_m + I_{8-m} \quad (5.25)$$

Variations of I_m and I_{8-m} are not co-related because they are derived from different inputs, therefore

$$\sigma^2(I_{out,m}) = \sigma^2(I_m) + \sigma^2(I_{8-m}) \quad (5.26)$$

By substituting (5.24) into (5.26), we obtain

$$\sigma^2(I_{out,m}) = \left[\frac{m^2}{4} - 2m + 16 \right] \cdot (\beta V_{OD})^2 \sigma^2(V_T) \quad (5.27)$$

Thus, the worst case is $m = 0, 8$, (when variance of $I_{out,m}$ reaches its maximum value), and best case is when $m=5$. Let us consider the worst case

$$\sigma^2(I_{out,m}) = 16(\beta V_{OD})^2 \sigma^2(V_T) \quad (5.28)$$

According to [68], the variance of the threshold voltage can be expressed as:

$$\sigma(V_{T0}) = \frac{A_{VT0}}{\sqrt{WL}} \quad (5.29)$$

where A_{VT0} is a process dependent parameter, which is inversely proportional to gate oxide thickness. For 0.35 μm CMOS process, A_{VT0} is assumed to be 8mV $\cdot\mu\text{m}$. By substitute (5.29) into (5.28), yields

$$\sigma(I_{out,m}) = \sqrt{16\beta(V_{OD})^2 \cdot \mu C_{OX} \cdot \frac{A_{VT0}^2}{L^2}} = 2\sqrt{\mu C_{OX} I_A} \cdot \frac{A_{VT0}}{L} \quad (5.30)$$

where L is the length of interpolation transistors, I_A is the input current of the interpolator, μ is mobility and C_{OX} is the capacitance per unit area gate oxide. A_{VT0} is a V_T mismatch parameter related to process [68]. From Eq.(5.30) we can see the accuracy of the current interpolator is limited by the mismatch of current mirror. The accuracy of the ADC is proportional to the length of the interpolation transistors, whereby there is another tradeoff between speed and resolution. Although minimum transistor length benefits high-speed operation, it may not satisfy the accuracy requirement.

5.5 Current Comparator

Comparators are used to detect zero-crossing points of all the folding waveforms from interpolator. Because of current-mode interpolation, current comparators must be used. Simple current mirrors are used in the interpolation block. Errors caused by short channel effect must be minimized. Our solution is to keep the voltages of interpolator output nodes constant. To achieve this, the input impedance of current comparators should be very low. We proposed a very low input impedance current comparator, which is depicted in Figure 71. The input currents are converted to voltages by the I-to-V transresistance stage. Transistors M1 and M2 form a feedback loop to reduce the input impedance.

The small signal input impedance of the I-to-V stage (Figure 71b) is

$$R_{in} = \frac{1}{g_{m1}} \cdot \frac{g_{o2}}{g_{m2}} \quad (5.31)$$

and the transresistance gain is

$$R_m = \frac{V_{out}}{I_{in}} = \frac{1}{g_{m1}} \quad (5.32)$$

The input impedance is small enough to make the voltage swing at current mirror outputs negligible. Except the input current-to-voltage converter, other parts of the current comparator are the same as voltage comparators. Thirty-two current comparators are arranged into one bank.

The voltage mode comparator after the I-to-V stage is a normal clocked comparator. Figure 71c illustrates the schematic of the voltage comparator. When the latch signal is high (in track mode), transistor M7 enters triode region and acts as a resistor to reset the output. The comparator is in amplifying period, and the gain is $A_v = g_{m1} / (2g_{m7} - g_{m8})$, where g_m of M8 and M9 act as negative resistance whilst M7 acts as positive resistance. However, this gain has to be optimized to that the latch output can be reset at the given clock rate. Once the latch signal goes low, transistor M7 is turned off and the amplifier becomes a positive feedback latch due to the cross-coupled transistors M8 and M9. Because M8 and M9 are in an active region at the moment when the latch signal goes off and start the regeneration with initial amplified output voltage from the end of the amplifying period, the latch is very fast. The disadvantage of this latch is that it dissipate power even when the output is fully developed.

Transistors M7 acts as resistors, which can track the negative resistors M8-M9 very well since they have similar sizes and bias currents. Although M7 can be replaced by two diode connected transistors like the comparator designed by Song[90], one disadvantage of Song's design is large parasitic capacitance load on Vo+ and Vo- nodes, which increases the time constant of the regenerative network and lower down the comparator speed dramatically. Note in this design the gate of M7 is not directly driven by latch clock, thus the "ON" resistance is not sensitive to power supply voltage.

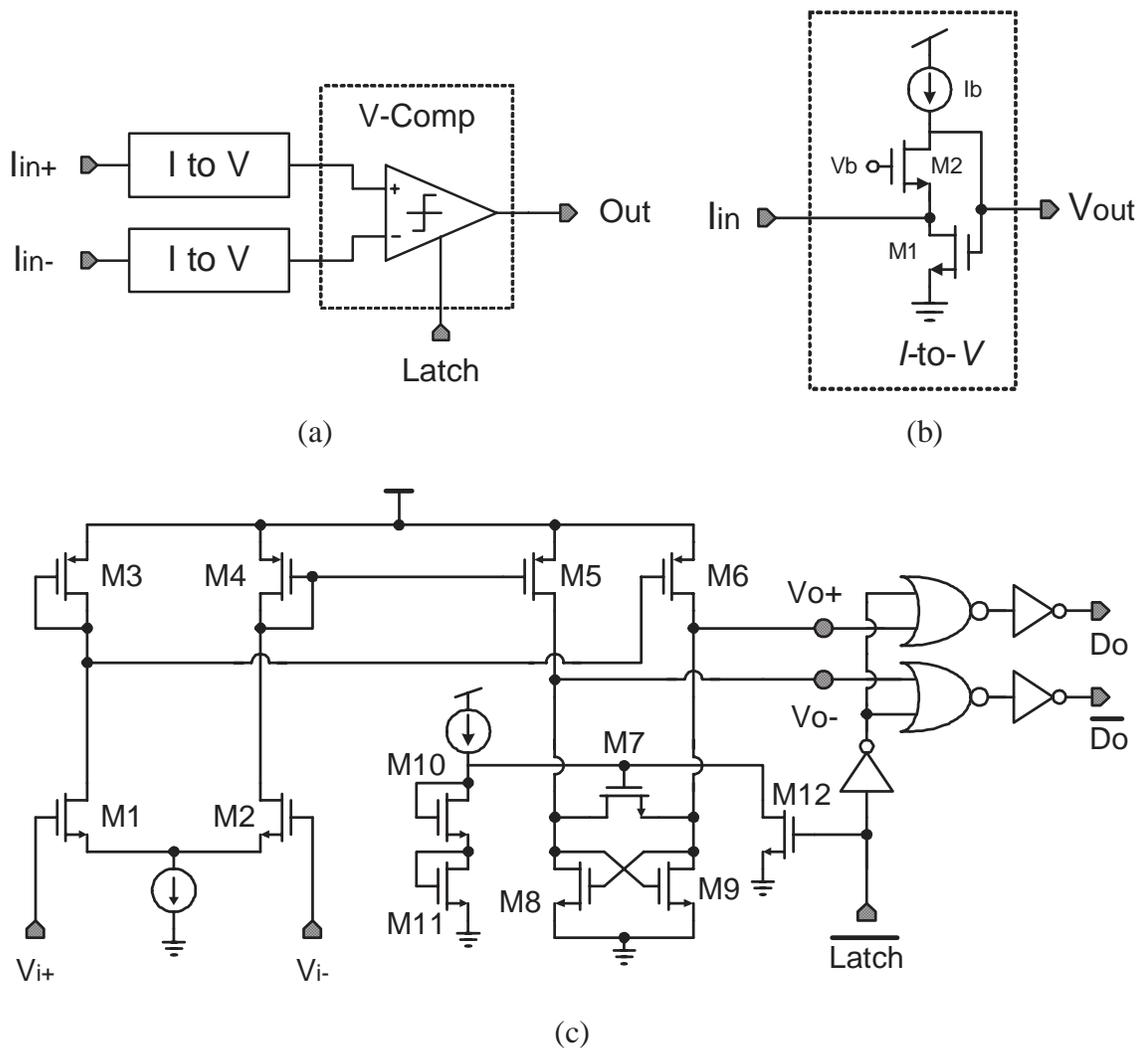


Figure 71 Current comparator. (a) block diagram (b) schematic of the I-to-V block
(c) voltage comparator

5.6 Coarse Quantizer

Because coarse and fine bits are generated independently, all folding ADCs potentially have the bit synchronization problem. That is, the coarse and fine quantizers digitize input signal at different time due to the different delays along the coarse and fine signal paths. Without S/H, this problem is more serious. Although care can be taken to “equalize” the delays such that delay difference is minimized, bit synchronization and

error correction circuit must be adopted to solve this problem [72]. Sensitive regions are shown in Figure 72. In these sensitive regions, if transition points of MSBs and LSBs are not synchronized, a glitch error will appear in the reconstructed analog output.

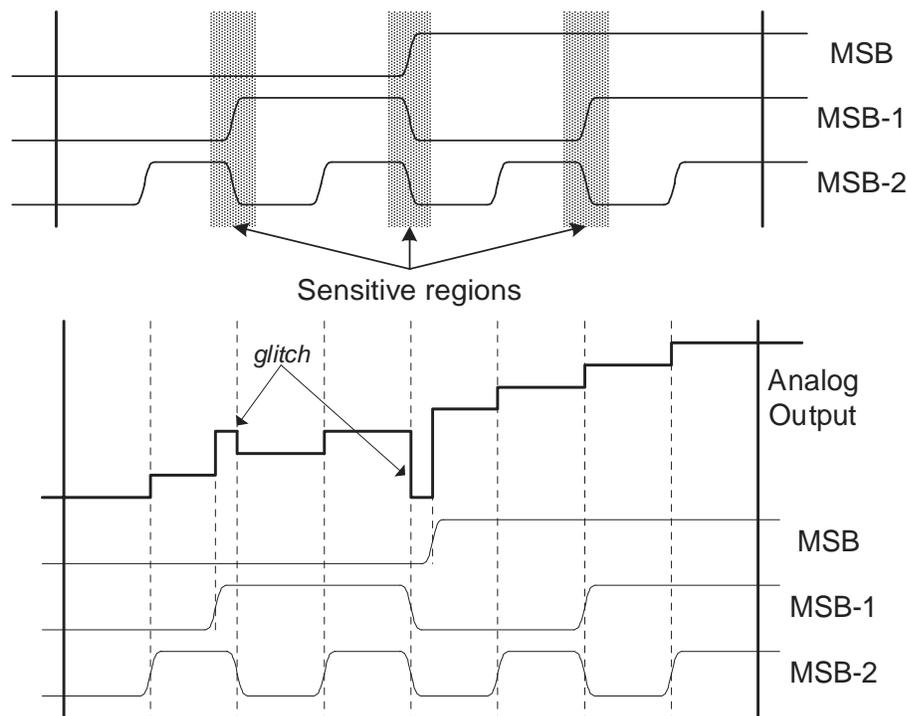


Figure 72 Sensitive regions in a $4\times$ folding system. 2 MSBs (MSB and MSB-1) are generated by coarse quantizer while fine quantizer produces MSB-2 and other LSBs.

Figure 73 illustrates a bit error correction scheme to synchronize MSBs and LSBs. Although three comparators are enough to generate two coarse bits with full-flash structure, we prefer using the coarse quantizer to define the sensitive regions and use the bit synchronization signal from the fine quantizer to generate the MSBs. Four comparators are required to define 3 sensitive regions shown in Figure 72.

The coarse quantizer uses four voltage comparators to generate four cycle pointers (CP_1 to CP_4). The comparator schematic is shown in Figure 71(c). Together with a bit-sync signal, C_{00} , coming from the fine quantizer, these 4 cycle pointers are used to generate the MSB and MSB-1. Waveforms are shown in Figure 74. Generally speaking,

cycle pointers CP_1 and CP_4 are used for overflow and underflow detection, and CP_2 and CP_3 are used to define the MSB sensitive region. IN-RNG is a signal to indicate the input signal falls into the ADC input range. This information can be used to adjust the gain the signal conditioning circuit preceding the ADC. Figure 75 shows the waveforms of a folding system with 8x folding factor. In this case 8 comparators are required to generate 8 cycle pointers ($CP_i, i=1\dots 8$).

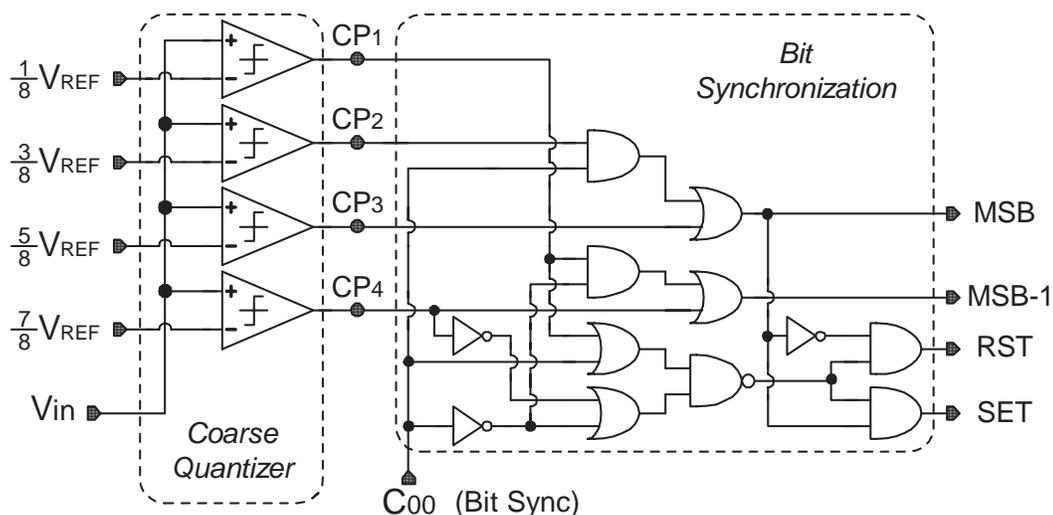


Figure 73 Coarse quantizer and bit synchronization block (bit-sync signal C_{00} comes from fine quantizer and is the output of a comparator, which input is a folding signal FI)

One advantage of this bit synchronization scheme is that the zero crossing points of cycle pointers need not to be very accurate, because they are used only to define sensitive regions. The MSB and MSB-1 bits are not derived directly from the coarse quantizer; instead, they are determined by bit-sync signal C_{00} , which comes from the fine quantizer (See Figure 74). Because the bit-sync signal C_{00} is always synchronized with other fine quantizer bits, thus MSB and MSB-1 are also synchronized with all fine quantizer bits.

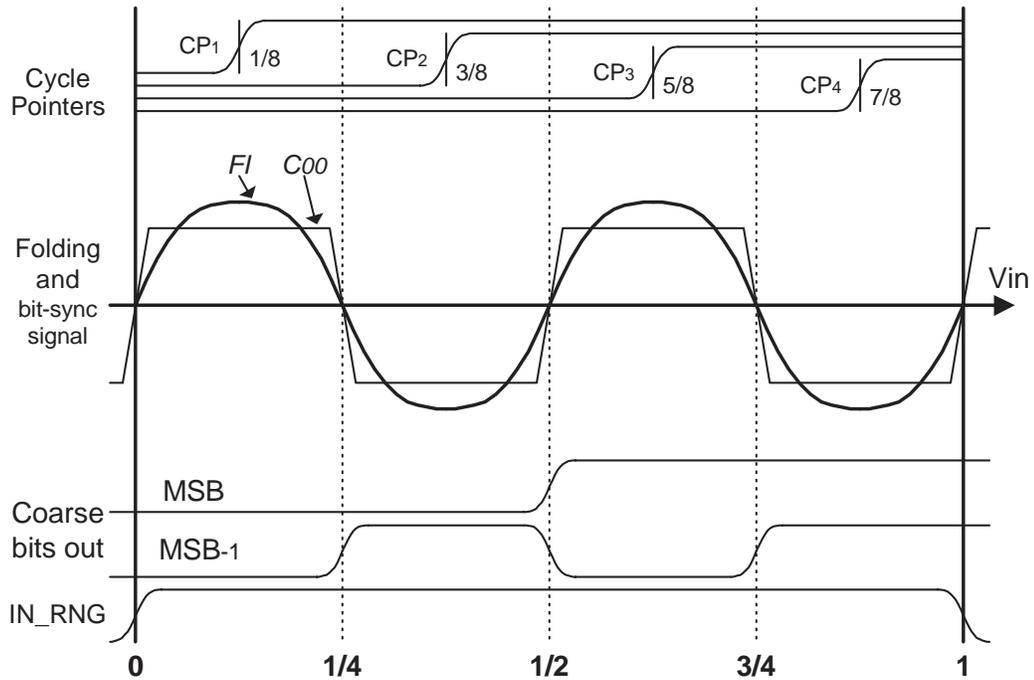


Figure 74 Waveforms of the coarse quantizer including bit error correction and synchronization. (*FI* is the folding waveform and bit-sync signal C_{00} is its comparison output, *IN_RNG* is a logic flag to indicate the input voltage is inside the ADC full range.)

The folding ADC also needs an over-range flag indicating when the input signal has exceeded the converter's full-scale range. When the input voltage is higher than the upper limit, the output of ADC is set to maximum output (all ones), and when it is lower than the lower limit, the ADC outputs all zeros. This flag can also be used to reduce the gain of the front end signal conditioning circuitry. The over-range flag and SET/RST signals can be derived from cycle pointers CP_1 and CP_5 .

$$\text{Inside Range Flag: } IN_RNG = (C_{00} + CP_1) \cdot (\overline{C_{00}} + \overline{CP_4}) \quad (5.33)$$

$$\text{Reset Signal: } RST = \overline{IN_RNG} \cdot \overline{MSB} \quad (5.34a)$$

$$\text{Set Signal: } SET = \overline{IN_RNG} \cdot MSB \quad (5.34b)$$

The two most significant bits can be determined by the combination logic of cycle pointers and bit-sync signal C_{00} from the fine quantizer.

$$MSB = C_{00} \cdot CP_2 + CP_3 \quad (5.35)$$

$$MSB_{-1} = \overline{C_{00}} \cdot CP_1 + CP_4 \quad (5.36)$$

The two most significant bits, which are generated from cycle pointers (CP_1 - CP_4) and bit-sync signal C_{00} Eq. (5.35) and Eq. (5.36), are synchronized with 5 least significant bits produced by the fine quantizer.

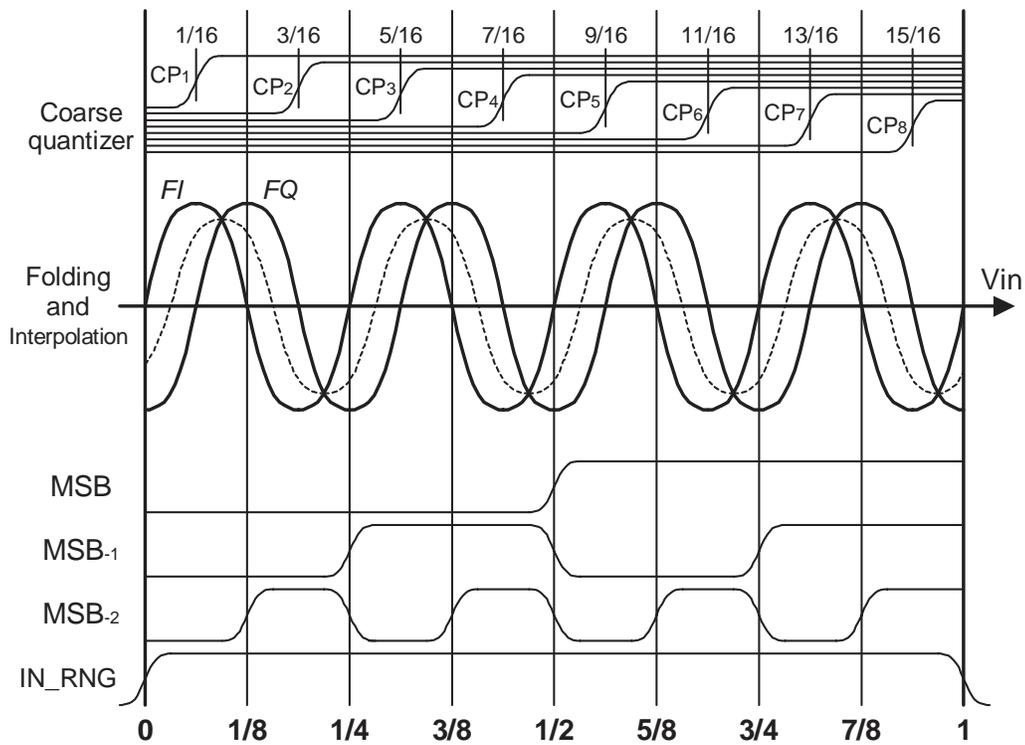


Figure 75 Bit synchronization (8x folding factor)

5.7 Digital Encoder Implementation

If Eq. (3.2a-e) and Eq. (3.3a-g) are implemented as two-step operation, the delay will be at least two clock cycles; this is not desired in some cases. We propose a one-step operation (Figure 76) to convert cyclical code to binary code directly. Only exclusive-OR operation is used in Eq. (3.2) and Eq. (3.3), and both are triangular shaped, so by

combine them together we can share some gates and reduce the latency to one clock cycle.

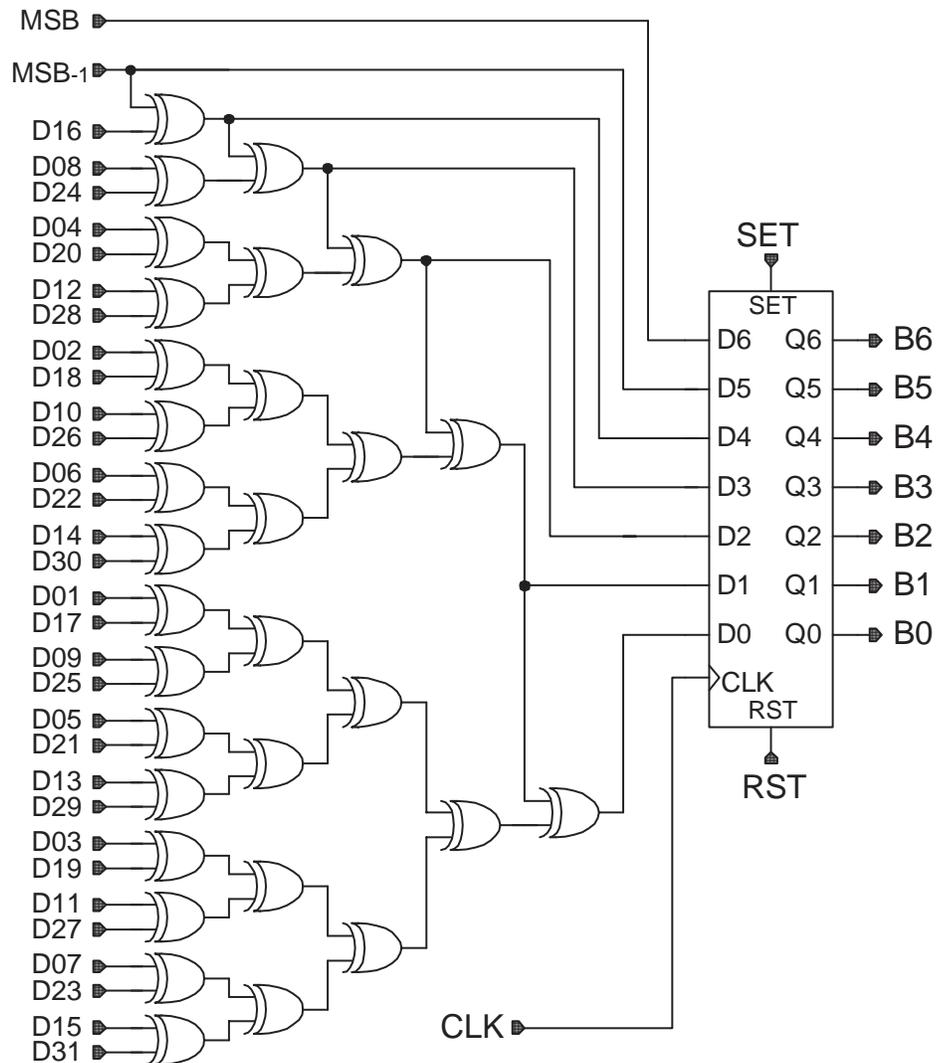


Figure 76 Cyclical code to binary code encoder

Circuit noise, comparator metastability and other interference may cause bubble errors. Bubble error correct circuit should be used in high-speed flash and folding A/D converters to keep the bit error rate low[75]. Figure 77 shows the schematic of a bubble error correction circuit consists of democratic cells. Each democratic cell has 3 inputs, if any two of the inputs is logic 1(0), then the output is logic 1(0).

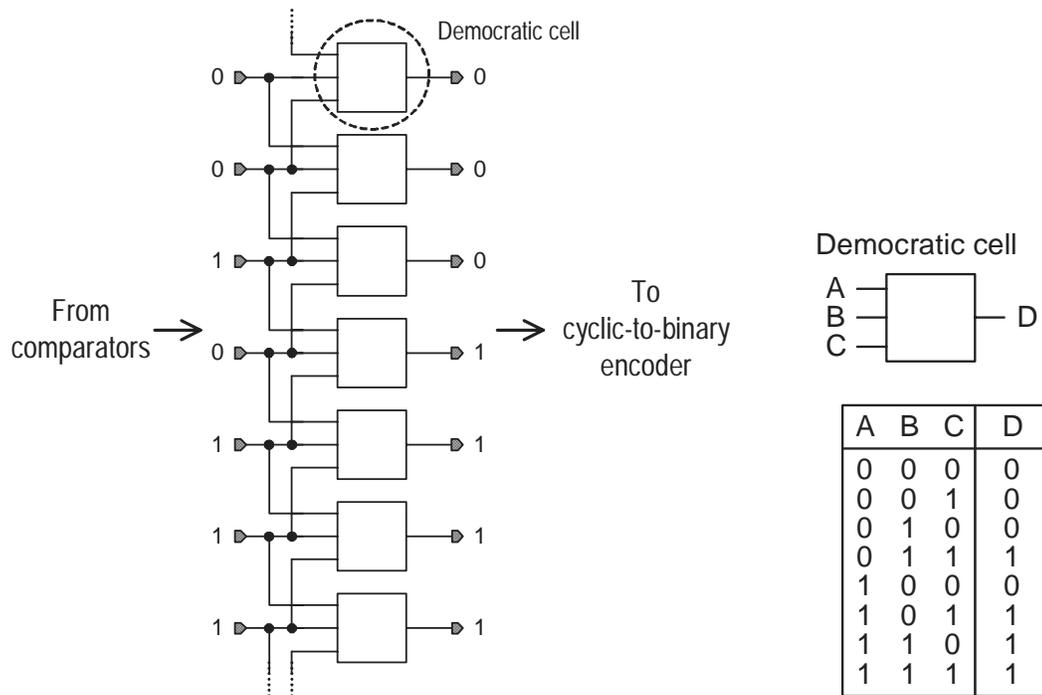


Figure 77 Bubble error correction

5.8 Peripheral Circuits

5.8.1 Clock Receiver

A small clock jitter in the high speed Nyquist analog-to-digital converter is required so as not to reduce signal-to-noise ratio, especially at input frequencies near Nyquist input. Usually square wave clock waveforms with sharp edges (i.e. short rise and fall time) are desired. However, for high speed A/D converter with sampling clock frequency be as high as 300MHz, square wave low jitter clock signal source is not easy to find. Also the rise and fall time will be much longer due to the parasitic capacitance of the chip package and circuit board.

The average error power due to clock jitter is given by

$$E_j = \frac{1}{M} \sum_{i=1}^M (\hat{x}_i - x_i)^2 \quad (5.39)$$

where M is the number of samples in one period and \hat{x}_i is the sampled value of x_i .

For a sinusoidal input waveform, and ideal samplers which exhibit a timing skew,

$$x_n = A \cdot \sin(\omega \cdot nT) \quad (5.40)$$

and

$$\hat{x}_n = A \cdot \sin(\omega \cdot (nT - \delta)) \quad (5.41)$$

where x_n is the value sampled at nT and \hat{x}_n is the value sampled at nT with the timing jitter noise δ . For the values of x_n and \hat{x}_n , the error power, in Eq.(5.39) becomes

$$\begin{aligned} E_j &= \frac{A^2}{M} \sum_{i=1}^M (\sin(\omega \cdot (nT - \delta)) - \sin(\omega \cdot nT))^2 \\ &= \frac{A^2}{M} \sum_{i=1}^M (1 - \cos(\omega\delta))^2 \sin^2(\omega \cdot nT) \\ &= A^2 \left(\frac{\omega^2 \delta^2}{2!} + \frac{\omega^4 \delta^4}{4!} + \dots \right) \end{aligned} \quad (5.42)$$

for small values of timing jitter, ignore the higher order term, we can obtain

$$E_j \cong A^2 \left(\frac{\omega^2 \delta^2}{2} \right) \quad (5.43)$$

Therefore, the signal-to-noise ratio (SNR) in dB due to clock jitter is

$$\begin{aligned} SNR &= 10 \log \left(\frac{A^2/2}{A^2 \omega^2 \delta^2 / 2} \right) \\ &= -20 \log(\omega\delta) \end{aligned} \quad (5.44)$$

where δ is the RMS value of clock timing jitter. The SNR vs. δ is plotted in Figure 78. This plot shows that the clock timing jitter should be less than 5 ps (rms) to avoid reducing the SNR by 3 dB from 7-bit quantized noise at 150 MHz input frequency.

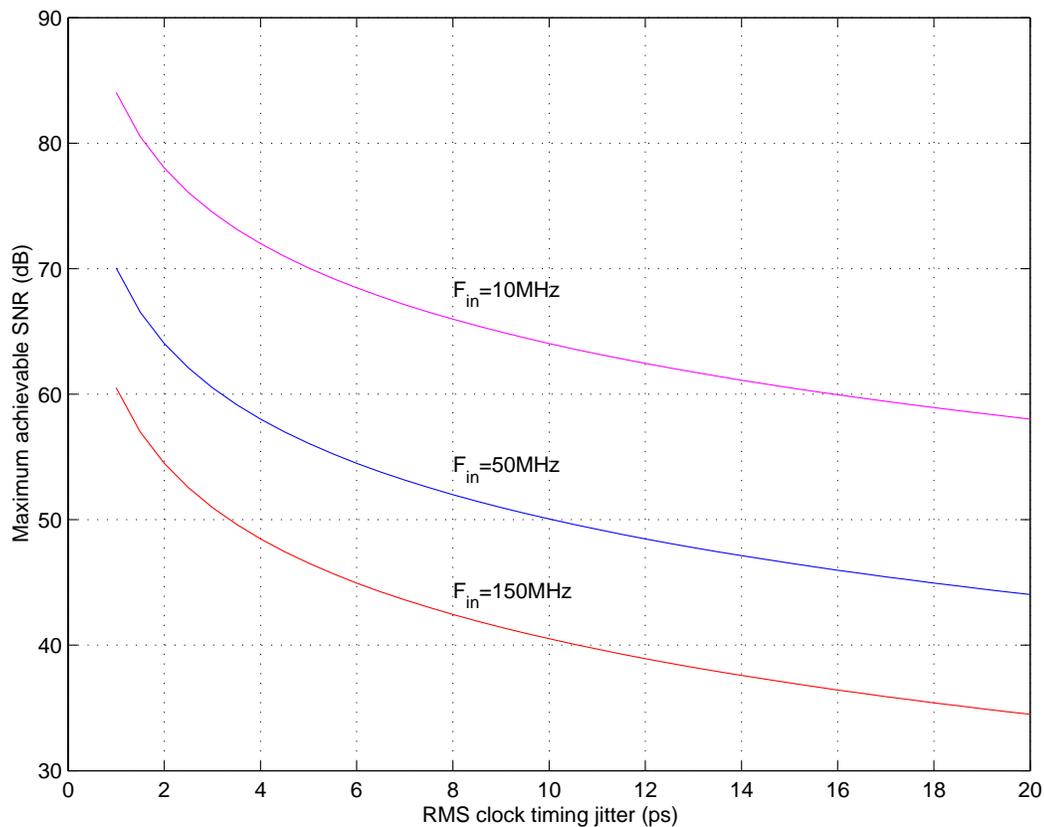


Figure 78 Signal-to-noise ratio due to clock timing jitter at 10MHz, 50MHz, and 150MHz input frequency

All clocks are generated on-chip from an external low phase noise balanced sinewave. On-chip clock circuitry synthesizes two non-overlapping phases and distribute them all over the chip. Figure 79 illustrates the schematic of a clock receiver, which converts differential sinusoidal clocks to square wave clocks[66]. The front-end clock receiver consists of three differential amplifiers, which sharpen the received 1Vp-p sinewave into a single-ended rail-to-rail square wave with 0.3ns rise/fall time. A subsequent stage comprising a three- and a two-inverter chain in parallel generates complementary clocks.

The clock jitter generated from these circuits must be smaller than 5ps to meet the 7b SNR requirement at Nyquist rate. The power supply and ground bounce of clock buffers contributes negligible sampling jitter because they are synchronized with the clock. The

zero-crossings of the clock buffer outputs are sharpened just enough to make the thermal noise contribution to jitter negligible. Local clock buffers provide the required rise/fall edge. Therefore, the front-end receiver stages dominate the clock jitter and are designed carefully.

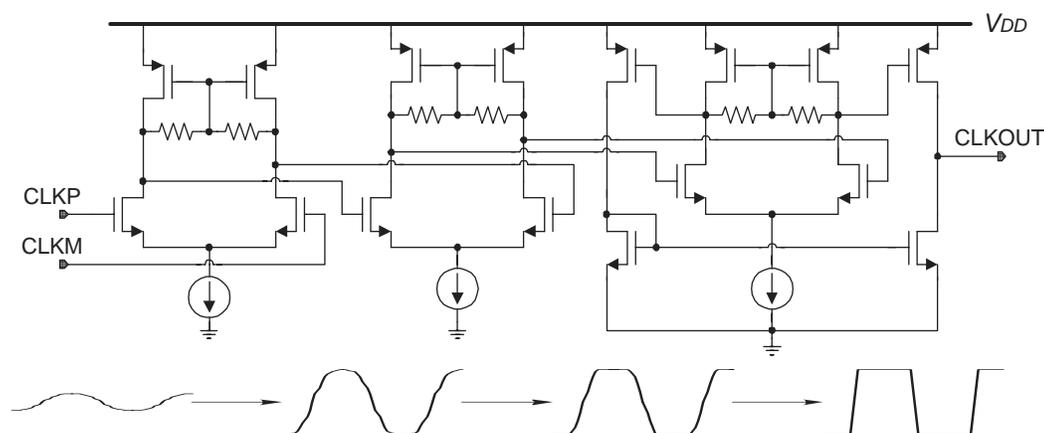


Figure 79 Schematic of the clock receiver and waveform for each stage

The input effective gate voltage ($V_{GS}-V_T$) of the first amplifier is maximized to 0.5V for minimum current clipping. The bandwidth of this amplifier is designed to be close to clock frequency. Zero-crossing slope gain is maximized to 7 without being too much deviated from the AC gain at the clock frequency. Since the slope is maximized with minimum bandwidth and DC gain, the noise (RMS) to slope ratio, i.e. the jitter (RMS) is minimized. The cascaded amplifiers decreases successively in DC gain but increases in unity gain bandwidth to accommodate the increasingly sharpened zero-crossings.

5.8.2 Output Buffer

Driving the digital outputs is a problem in very high-speed A/D converters because of the large currents required to charge and discharge the load capacitances. This can lead to a large bounce on the supply and ground leads. To minimize this, current steering type output buffers (see Figure 80) have been used in this device. The output swing is 400mV compare to 3.3V for CMOS logic. The advantage of a lower logic voltage swing is lower interference to analog circuitry and lower current consumption to charge and

discharge node capacitance. High speed comparators are used to convert these low swing differential signals back to ECL logic levels.

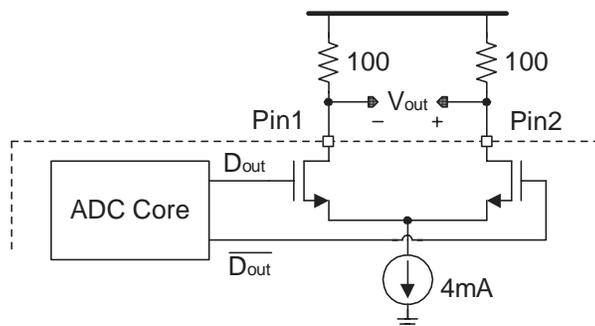


Figure 80 Schematic of the output buffer

5.9 Design Procedure

In chapter IV we talked about the system level design of a F&I ADC, i.e., how to determine system level parameters such as folding factor, interpolation factor, number of folding amplifiers, and system architecture choice such as with/without front-end S/H, from a set of specifications, namely sample rate and resolution. In this section we will talk about the transistor level design of major building blocks, such as the folding amplifier, interpolator and current comparators. The 7-bit 300MS/s F&I ADC is used as an example to illustrate the procedure. We already know the folding factor is 4, interpolation factor is 8 and number of folding amplifier is 4. In practical mixed-signal designs, fully differential structures are employed because of their immunity to noise and interferences. However, for the sake of simplicity, the following discussions are based on the simplified signal chain schematic of the analog preprocessing block shown in Figure 81. In Figure 81, the signal chain consists of the OTA based folding amplifier, current mirror based interpolator, current comparator comprising of an I-to-V stage and a regular voltage comparator.

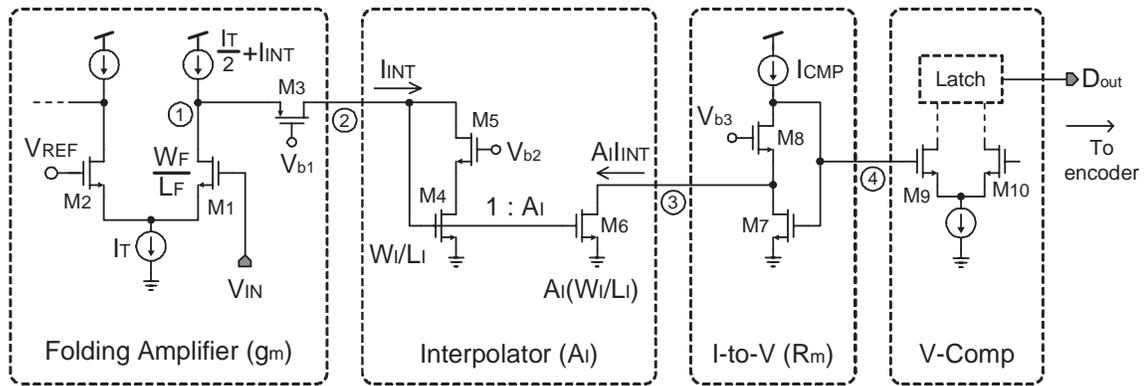


Figure 81 Signal chain of the analog preprocessing in F&I ADC consists of OTA based folder, current mirror based interpolator, and current comparator

The first step is to define the input Full Scale (FS) of the F&I ADC. The tradeoff is that ADCs with higher FS can tolerate larger offset and noise since they have larger LSB, whereas ADCs with lower FS can achieve higher speed. With a power supply voltage of 3.3V, the FS of 1.6V is chosen as the full scale of the F&I ADC as a result of tradeoff between speed and accuracy. Then we can calculate the LSB of this 7-bit ADC, which is $1.6V/128=12.5mV$.

5.9.1 Folding Amplifier

The threshold offset between two neighboring folders can be calculated from FS. For an I-Q double folding system shown in Figure 33, this offset is $FS/8$. However, in our 7-bit 300MS/s F&I ADC, 4 folders are used, thus the offset is $FS/16$, which is 0.1V. This is an important parameter for the folders.

We start from the folder offset, which is the major source of the nonlinearity of the whole ADC, since the offsets of comparators are attenuated by the analog preprocessing gain. To avoid severe performance degradation, offsets should be smaller than half of LSB, i.e., half of 12.5mV. Assuming the offsets are Gaussian distributed, we have $3\sigma(V_{T0})=12.5/2$, thus we know the standard deviation $\sigma(V_{T0})=3.2mV$. Based on Eq. (5.14), we can calculate the size of transistors comprising the differential pairs in the folders.

$$\frac{A_{VT0}}{\sqrt{W_F L_F}} = 3.2 \quad (5.45)$$

Where W_F and L_F are the width and length of folding amplifier transistors. Assuming $A_{VT0}=8\text{mV}\mu\text{m}$, and minimum length transistors are used to achieve high speed, thus $L_F=0.35\mu\text{m}$. From Eq. (5.45) the width of differential pair transistor can be calculated as

$$W_F = \frac{A_{VT0}^2}{\sigma(V_{T0})^2 L_F} = \frac{8^2}{3.2^2 \times 0.35} = 63 (\mu\text{m}) \quad (5.46)$$

The gate-source voltage can be calculated from the linearity requirement, which depends on the offset voltage between two neighboring folders, which is $FS/16$ in our case. We know the linear range of a differential pair is $2\sqrt{2}(V_{GS} - V_T)$. Thus we can calculate the minimum gate-source overdriving voltage as

$$V_{GS} - V_T = \frac{(FSW / 16)}{\sqrt{2}} = 71 (\text{mV}) \quad (5.47)$$

With the size of transistors and gate-source overdriving voltage, the tail current can be calculated as

$$I_T = 2 \times \frac{1}{2} K_N \frac{W_F}{L_F} (V_{GS} - V_T)^2 \quad (5.48)$$

For $0.35\mu\text{m}$ NMOS transistor $K_N=90\mu\text{m}/\text{V}^2$. Thus, Eq. (5.48) yields $I_T=86\mu\text{A}$, this is the minimum tail current. Note that the tail current is also the output current swing of the OTA based folding amplifier (folder). Biased with this tail current, the transconductance of the differential pair transistors is

$$g_m = K_N \frac{W_F}{L_F} (V_{GS} - V_T) = 1.2 (\text{mS}) \quad (5.49)$$

This is also the transconductance gain of the folding amplifier.

5.9.2 Current Mirror based Interpolator

Next, we will calculate the transistor size of the current mirror (W_I/L_I) based interpolators. Eq. (5.30) can be rewritten as by replacing $K_N = \mu C_{ox}$.

$$\sigma(I_{INT}) = 2\sqrt{K_N I_{INT}} \cdot \frac{A_{VT0}}{L_I} \quad (5.50)$$

where I_{INT} is the bias current of the current mirror, which obviously should be higher than half of the folding amplifier output current swing, i.e., half of I_T . Let's choose $I_{INT} = 86\mu\text{A}$ as the bias current for the current mirrors, thus the current swings between $43\mu\text{A}$ and $129\mu\text{A}$. A_{VT0} is assumed to be $8\text{mV}\mu\text{m}$ for $0.35\mu\text{m}$ NMOS transistors. The current offset in Eq. (5.50) can be referred back to the input as an input referred offset,

$$\frac{\sigma(I_{INT})}{g_m} = \frac{2\sqrt{K_N I_{INT}}}{g_m} \cdot \frac{A_{VT0}}{L_I} \quad (5.51)$$

The offset due to the interpolation transistor mismatch should be smaller than one half LSB. Thus the standard deviation of the input referred offset in Eq. (5.51) should be smaller than $\text{LSB}/6$. We have

$$\frac{2\sqrt{K_N I_{INT}}}{g_m} \cdot \frac{A_{VT0}}{L_I} \leq \frac{\text{LSB}}{6} \quad (5.52)$$

Substitute $g_m = 1.2\text{mS}$, $\text{LSB} = 12.5\text{mV}$, $A_{VT0} = 8\text{mV}\mu\text{m}$, $K_N = 90\mu\text{A}/\text{V}^2$, $I_{INT} = 86\mu\text{A}$ into Eq. (5.52), we can calculate the minimum length of interpolator transistor is $L_{min} = 0.56\mu\text{m}$. Apparently we don't want to make this length too large, otherwise the speed is slowed down, so we choose $L_I = 0.6\mu\text{m}$.

Assuming a moderate gate-source overdriving voltage, i.e., $V_{GS} - V_T = 200\text{mV}$, we can calculate the width of the transistor comprising the interpolating current mirrors.

$$W_I = \frac{2I_{INT} \cdot L_I}{K_N (V_{GS} - V_T)^2} = 28.7 \text{ } (\mu\text{m}) \quad (5.53)$$

We choose $W_I = 28.8\mu\text{m}$. Note this transistor consists of 8 unit transistors, thus the size of each unit transistor is $3.6\mu\text{m}/0.6\mu\text{m}$.

5.9.3 Current Comparator: I-to-V Stage

The next block is the I-to-V transresistance stage. To circumvent the comparator offset, the analog preprocessing gain should be large enough, i.e., greater than 1V/V. The combinational gain from the input (node V_{in}) to the input of voltage comparator, node 4 in Figure 81, is

$$A_V = g_m \cdot A_I \cdot R_m \quad (5.54)$$

The tradeoff here is the speed and accuracy again: higher analog preprocessing gain alleviate the offset requirement on the voltage comparators, while lower analog preprocessing gain is easier to achieve wider bandwidth. The design rule here is to maximize the gain while keeping the bandwidth higher than the bandwidth requirement, i.e., higher than sampling rate in the front-end S/H case.

Assuming a combinational gain of 4V/V, and the interpolator current gain $A_I=1A/A$. The minimum transresistance gain of the I-to-V stage can be calculated as

$$R_m = A_V / (g_m \cdot A_I) \quad (5.55)$$

Substitute $A_V=4$, $A_I=1$, $g_m=1.2mS$, and Eq. (5.55) yields $R_m=3.3K\Omega$. From Eq. (5.32) can calculate the transconductance of the transistor M7 in Figure 81

$$g_{m7} = \frac{1}{R_m} = 300 \text{ } (\mu S) \quad (5.56)$$

The bias current of I-to-V stage I_{CMP} should be larger than the interpolator output current, which varies from 43 μA to 129 μA if we assume the current gain is 1A/A. We can choose $I_{CMP}=150\mu A$. Thus the nominal bias current of M7 is 150 μA -86 μA =64 μA . With this bias current and Eq. (5.56), the size of M7 can be calculated as

$$\frac{W_{M7}}{L_{M7}} = \frac{g_{m7}^2}{2K_N \cdot I_7} \quad (5.57)$$

Another restriction on the size of transistor M7 is the offset due to V_T mismatch, which should be much smaller than half LSB when referred to ADC input, i.e., divided by the analog preprocessing gain. With the analog preprocessing gain of 4, this requires

the standard deviation of the offset due to V_T mismatch on M7 should be smaller than $2\text{LSB}/3=8.3\text{mV}$. Again, based on Eq. (5.14), we have

$$\frac{A_{VT0}}{\sqrt{W_{M7}L_{M7}}} = \frac{1}{3} \frac{\text{LSB}}{2} A_V \quad (5.58)$$

Combine Eq. (5.57) and Eq. (5.58), and substitute $A_{VT0}=8\text{mV}\mu\text{m}$, $\text{LSB}=12.5\text{mV}$, $A_V=4$, $g_{m7}=300\text{mS}$, $I_7=64\text{mA}$, $K_N=90\mu\text{A}/\text{V}^2$. We have $W_{M7}=2.8\mu\text{m}$, and $L_{M7}=0.35\mu\text{m}$.

The above hand calculations just provide an initial configuration for simulation. For advanced CMOS processes, the input-output transfer characteristics may not follow the square law, which is an assumption in hand calculation. Also the bandwidth of each stage must be verified with transistor level simulation. It is quite possible that a designer has to repeat the above design process several times to reach an optimum solution.

CHAPTER VI

EXPERIMENTAL RESULTS

6.1 Layout

The ADC was laid out by Virtuoso layout editor from Cadence. The layout extraction, DRC and LVS check were also performed in Cadence. The fully differential balanced signal is applied to the ADC from the bottom side of the chip, and a fully differential 300 MHz clock is applied from the left side of the chip.

The effect of the digital circuit noise [54], [93] has been one of the major sources of degradation in performance in the ADC. To avoid the digital noise coupling, the analog signal is kept away from the digital area. All the noisy clock buffers which generate 300MHz/150MHz clock signals, and the output buffers, are located in the top left part of the chip. The clock buffers are surrounded by p+ substrate contacts and the n-well guard ring, and the large p+ substrate contacts are added in-between the digital data output buffer and the core circuitry.

The A/D converter was fabricated in a four-level metal double-poly 0.35- μm CMOS process (only one poly layer is used) using standard MOS field-effect transistors (FETs). We use only the components available in digital process technology. The active chip area is 1.2mm². A photomicrograph of the chip is shown in Figure 82.

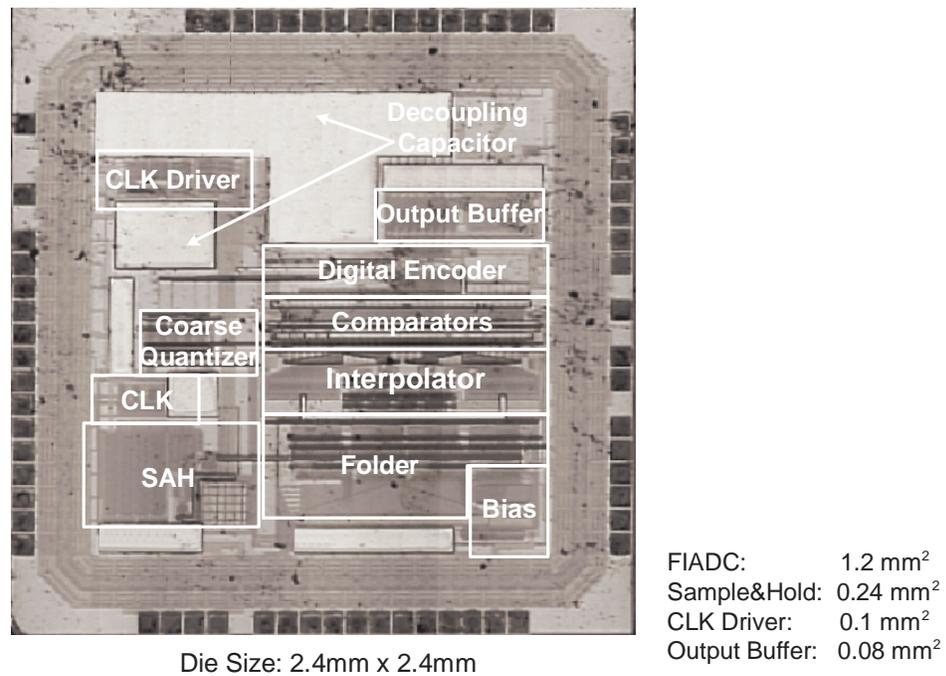


Figure 82 Chip microphotograph

6.2 Test Methodology and Test Setup

The A/D converter chips were tested by supplying sinusoidal input signals and sinusoidal clocks to the device under test(DUT) and capturing the resultant digital output data with mixed-signal oscilloscope. The simplified schematic of the test system is shown in Figure 83. High speed comparators are used to convert low swing ADC outputs back to ECL logic levels. A high speed DAC is used to reconstruct analog signals for qualitative evaluation purpose. It does not affect the quantitative performance evaluation.

Additionally, calculating histograms from large sets of output data generated in response to input signals with known probability density functions enables determination of the ADC's dynamic integral and differential linearity error (INL and DNL)[15], [78]

A high-speed 7bit DAC (in fact, we use 7 bits of a 12-bit DAC) reconstructs the digitized signal for analysis with an oscilloscope and spectrum analyzer. The reconstruction DAC in the test set-up is used to generate qualitative information for debugging and trouble-shooting, and does not affect the accuracy of the performance test data.

The test setup, a photograph of the PCBs are shown in Figure 84. To facilitate testing of many devices, the test circuit is implemented in 3 PCBs. On the first PCB is a bias generator, which generates all bias currents and voltages the ADC requires. The second one is the ADC board with input and clock conditioning circuits and decoupling capacitors. The third one is the data collection board consists of high speed comparators, logic translators, clock divider, and reconstruction DAC.

To test different chips, we just need to make several PCBs for the ADC board and the bias board and data collection board can be shared. Usually the most convenient way is using chip sockets, however, at such high frequency the socket likely will affect the performance significantly.

A high speed DAC is used to convert ADC output data back to analog waveform to verify the functionality of the ADC. Figure 85 shows two waveforms with different sample rate. In the first case, a slow 12MHz sinusoidal signal was sampled with 161MHz clock rate, and the reconstructed analog waveform resemble a quantized version of the input signal. In the second case, a 263 MHz input sinusoidal signal was sampled with 256MHz clock rate, it seems the reconstructed output waveform doesn't resemble input signal in any sense. Why? When the input signal is higher than Nyquist frequency, the A/D converter front-end sample and hold acts as a mixer, and the reconstruct DAC acts as a low pass filter. Thus the final output frequency is the difference between clock and signal frequencies: $|F_{clk} - F_{sig}|$. In this case the frequency difference is 7MHz, so the output is a 7MHz sinusoidal waveform.

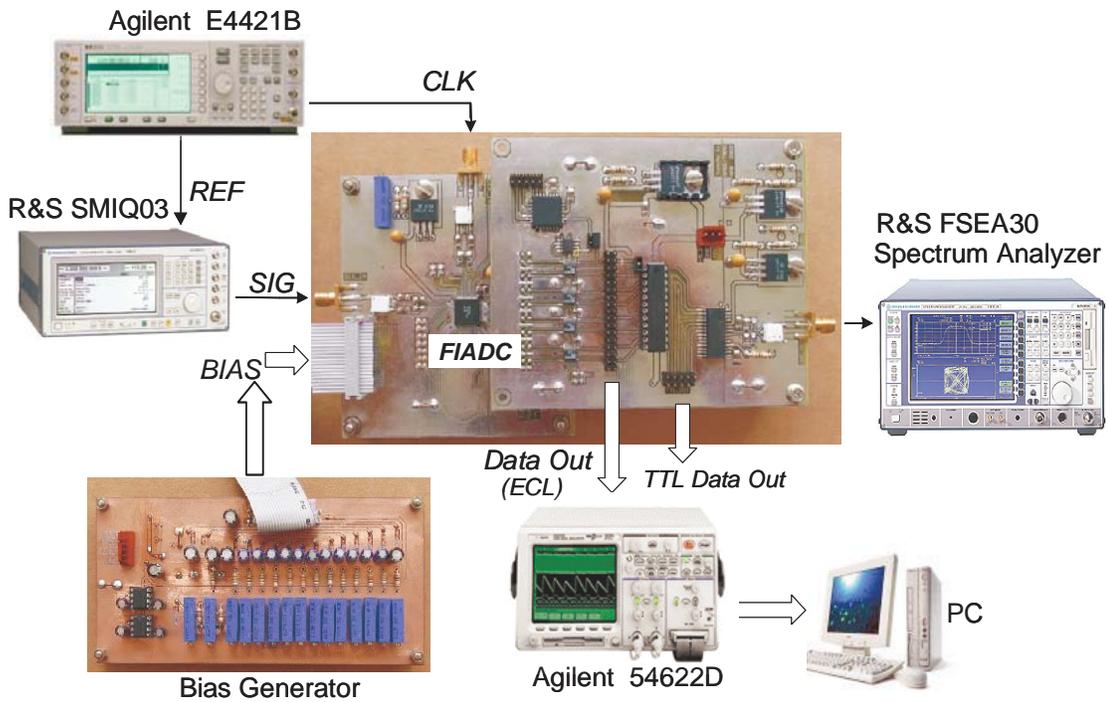
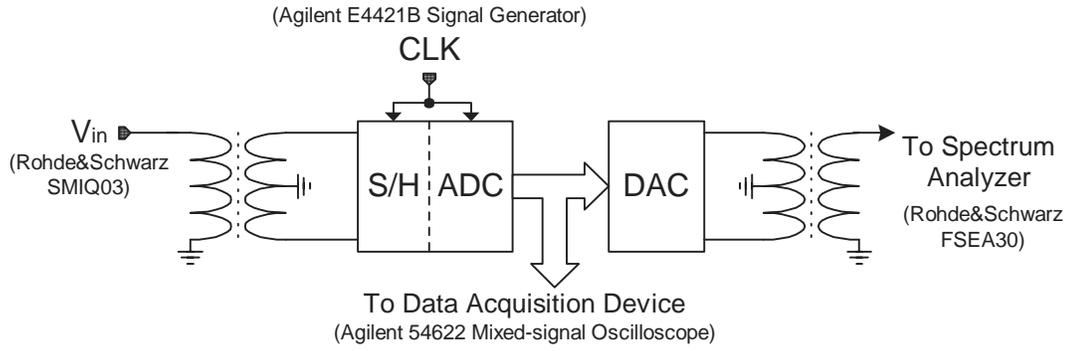


Figure 84 Folding A/D converter test setup

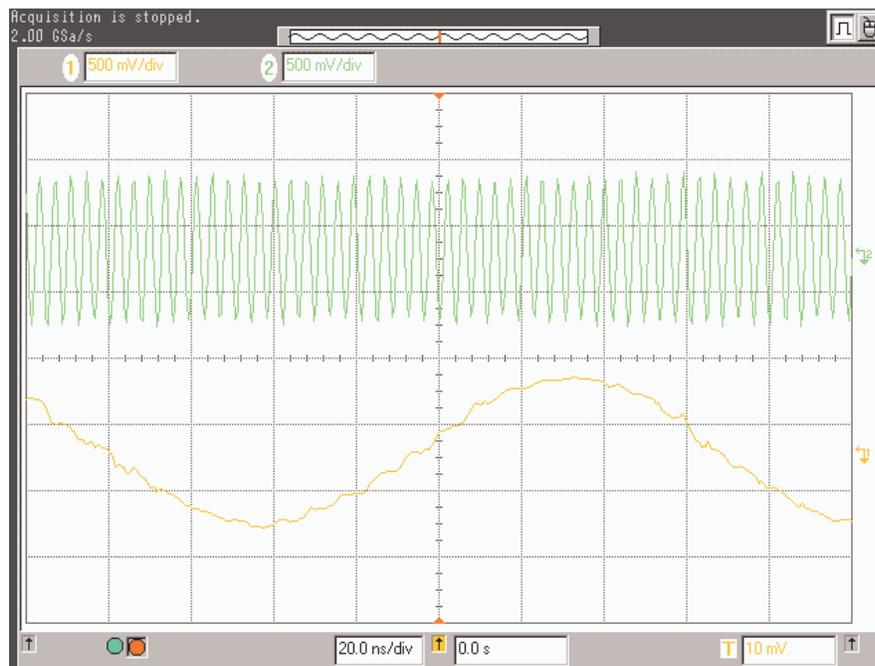
(a) $F_{in}=12\text{MHz}$, $F_{sample}=161\text{MS/s}$ (b) $F_{in}=263\text{MHz}$, $F_{sample}=256\text{MS/s}$

Figure 85 Reconstructed waveform at the output of high speed DAC (a) $F_{in}=12\text{MHz}$,
 $F_{sample}=161\text{MS/s}$ (b) $F_{in}=263\text{MHz}$, $F_{sample}=256\text{MS/s}$

6.3 Sinusoidal Fitting

FFT can be used to measure the SNR, SNDR, THD and other dynamic performance of ADC. However, the limitation is that the signal frequency must be the integral times of the bin resolution. For example, if the sampling clock frequency is f_s and number of FFT is N , the bin resolution frequency is

$$f_{res} = \frac{f_s}{N} \quad (6.1)$$

The input frequency must satisfy

$$f_{in} = m \cdot \frac{f_s}{N} \quad (m = 1, 2, \dots, \frac{N}{2} - 1) \quad (6.2)$$

If the condition in Eq. 6.2 is not met, then the noise and distortion power calculation from FFT results are not correct due to the “spectrum leakage”. In this case, we can use sinusoid fitting to calculate the amplitude of fundamental and harmonics.

Assume the output of A/D converter is expressed as the sum of signal and noise

$$X(n) = S(n) + N(n) \quad (6.3)$$

where $S(n)$ is signal, and $N(n)$ is quantization noise plus distortion.

Because the input signal is sinusoid signal, it can be represented as

$$S(n) = A \cdot \sin(\Omega n + \Phi_0) \quad (6.4)$$

where A is the amplitude, and Φ_0 is the initial phase. $\Omega = 2\pi f_{in} / f_s$.

The amplitude and phase can be estimated as

$$\hat{\Phi}_0 = \arctan \left(\frac{\sum_n X(n) \cdot \sin(\Omega n)}{\sum_n X(n) \cdot \cos(\Omega n)} \right) \quad (6.5)$$

$$\hat{A} = \frac{\sum_n X(n) \cdot \sin(\Omega n + \hat{\Phi}_0)}{\sum_n \sin^2(\Omega n + \hat{\Phi}_0)} \quad (6.6)$$

Estimated signal can be reconstructed as

$$\hat{S}(n) = \hat{A} \cdot \sin(\Omega n + \hat{\Phi}_0) \quad (6.7)$$

Subtract the signal from the ADC output $X(n)$, we have the noise plus distortion:

$$\hat{N}(n) = X(n) - \hat{S}(n) \quad (6.8)$$

Thus the SNDR can be calculated as:

$$SNDR = 10 \times \log_{10} \left(\frac{\sum_n \hat{S}^2(n)}{\sum_n \hat{N}^2(n)} \right) \quad (6.9)$$

Eq. (6.5) and (6.6) can also be used to estimate amplitude and phase of harmonics, just replace the fundamental frequency f_{in} with harmonics frequency $2f_{in}, 3f_{in}$, etc.

Once all the harmonics amplitudes and phases are estimated, THD can be calculated.

6.4 Performance Summary

At low frequency, the SNDR is approximately 40dB, which is close to the theoretical limit for a 7-bit ADC, 44dB. The SFDR is about 47dB.

When the analog input frequency is increased toward the target Nyquist rate of 150MHz, distortion increases as expected (Figure 86). For a 61MHz full-scale input and a 300MHz conversion rate, the SNDR degrades to 38dB, while the SFDR, dominated by the 3rd harmonic, degrades to 45dB.

For a 161MHz full-scale input and a 300MHz conversion rate, the SNDR is 33dB and SFDR drops to 38dB. Generally speaking, at lower frequency, the quantization noise dominates while the harmonic distortion dominates at higher input frequency.

Measured performance is summarized in Table 6. The effective number of bits drops to 6 when the input signal frequency reaches 60MHz. At 300MSamples/s, with 3.3V power supply, the A/D converter consumes 200mW of power.

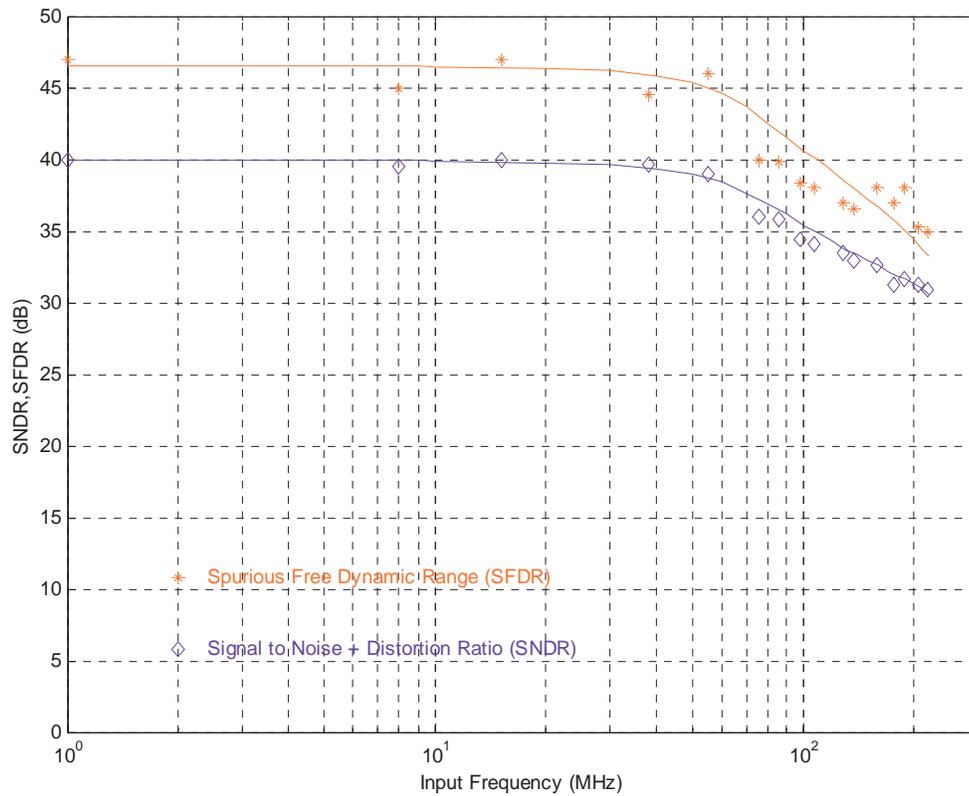


Figure 86 Measured dynamic performance of the A/D converter (clock rate: 300MS/s)

TABLE 6 A/D converter experimental performance summary

CMOS Technology	2-poly, 4-metal, .35 μ m	
Supply Voltage	3.3V	
Input Range	1.6V p-p	
Active Area	1.2mm ²	
Resolution	7-bit	
Latency	2 Clock Cycles	
Conversion Rate	300MSamples/s	
Power Dissipation	200mW (@300MHz, excluding S/H)	
Differential Non-linearity	<0.6LSB	
Integral Non-linearity	<1.0LSB	
SNDR	38dB	33dB
Fin for SNDR measurement	60MHz	160MHz
SFDR	45dB	38dB
ADC input capacitance	2pF	
Chip Package	TQFP64	

Although INL and DNL are not among the most important electrical characteristics that specify the high-performance data converters used in communications and fast data-acquisition applications, because they are considered static linearity parameters, they gain significance in the higher-resolution imaging applications.

DNL error is defined as the difference between an actual step width and the ideal value of 1LSB. For an ideal ADC, in which the differential nonlinearity coincides with $DNL = 0\text{LSB}$, each analog step equals 1LSB ($1\text{LSB} = V_{FSR}/2^N$, where V_{FSR} is the full-scale range and N is the resolution of the ADC) and the transition values are spaced exactly 1LSB apart. DNL is specified after the static gain error has been removed. INL error is described as the deviation, in LSB or percent of full-scale range (FSR), of an actual transfer function from a straight line.

INL and DNL can be measured with either a quasi-DC voltage ramp or a low-frequency sine wave[15] as the input. A simple DC (ramp) test can incorporate a logic analyzer, a high-precision DC source for sweeping the input range of the device under test (DUT), and a control interface to a PC.

For an ideal ADC with a full scale ramp input and random sampling, an equal number of codes is expected in each bin. Differential nonlinearity is the deviation from one least significant of the range of input voltages that give the same output code. Integral nonlinearity is the deviation of the transfer curve from ideality. At first glance, the choice for an input would be a ramp or triangle wave. An equal number of samples per bin is expected, except for the first and last bins which would accumulate all counts from inputs outside the converter's range. The fundamental drawback to this is the distortion or nonlinearity in the ramp. Brief consideration makes it clear that the input source must be known with better precision than the converter being tested. A sine wave signal source is much better than the ramp signal [15]. It is precisely known mathematically, and commercial ultralow distortion oscillators are widely available and their signal purity can be easily confirmed by a spectral analyzer, whereas for a ramp signal it is very difficult to verify its linearity, if not impossible.

Figure 87 presents DNL and INL measurement results by performing code density test. The input signal frequency is 150KHz and the sample rate is 40MS/s.

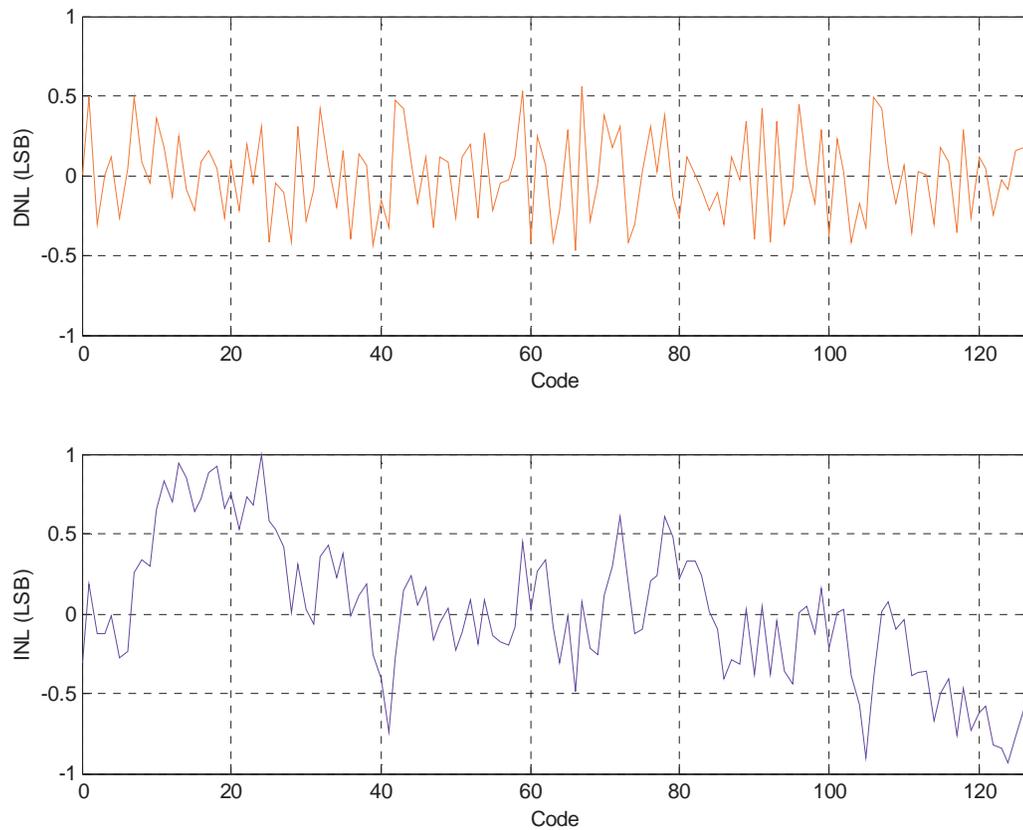


Figure 87 Measured DNL and INL

Figure 88 shows the output spectrum of the reconstructed analog signal; the SFDR is 39dB for $F_{in}=119.9MHz$, $F_S=256MS/s$. Because the maximum clock rate of the DAC is 165MS/s, the output data of ADC is undersampled (decimated) by 2. In this case the DAC refresh rate is 128MS/s.

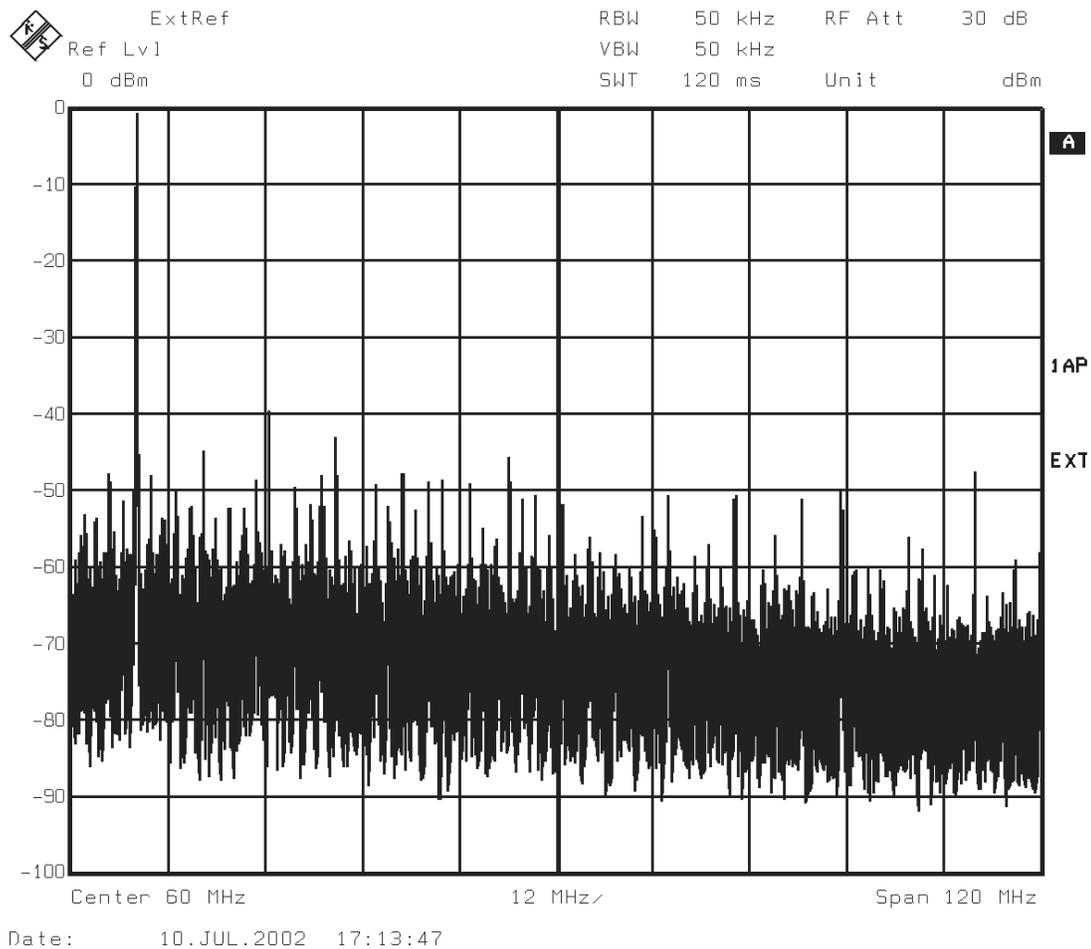


Figure 88 Measured spectrum of the reconstructed sinusoidal signal. $F_{in}=119.9\text{MHz}$,
 $F_{sample}=256\text{MS/s}$, undersample ratio=2

The reconstructed analog output signal from the output of high speed DAC can be used to verify the functionality of the A/D converter. However, it's not appropriate to use it to measure the performance of the ADC, because the DAC and its peripheral analog components will contribute error sources to the reconstructed signal, thus measure results with this method is not accurate. A more accurate method is to sample the digital data directly from the output of A/D converter and save to a computer. Software (like MATLAB) can be used to reconstruct analog signal from those sampled

data. SNR, THD and other parameters can be calculated from the computer reconstructed signal.

Figure 89 shows the power spectrum of a 2.05MHz input sinusoid sampled with 100MHz clock rate. The FFT length is 1024. The total signal to noise plus distortion ratio is 39dB which means the effective number of bit is about 6.2-bit.

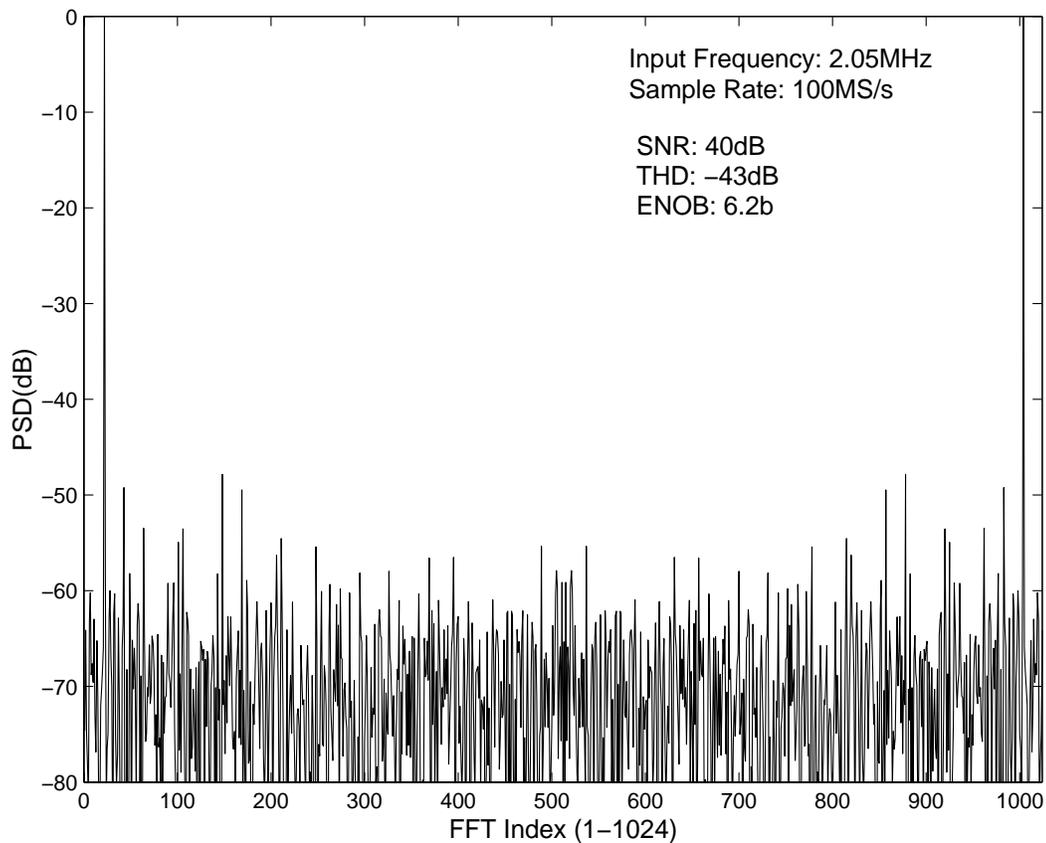


Figure 89 FFT calculated power spectrum from the sampled ADC output data

Table 7 lists performances of some F&I ADCs appeared in the literature and this work, where the figure of merit is defined as: $FM = \frac{2^n \cdot BW}{Power}$ (MHz/mW). Input bandwidth (BW) is defined as the input signal frequency at which the effective number of bits dropped to 1 bit below nominal resolution. In comparison with reported results,

the proposed ADC achieves ENOB of 6 at 60MHz. The proposed F&I ADC yields a wide input bandwidth with relatively low power consumption.

TABLE 7 State of the art high speed low resolution CMOS folding and interpolating A/D converters

Process	Bits	CLK (MHz)	Input BW (MHz)	Power (mW)	Area (mm ²)	Figure of Merit	Publication
0.5μm BiCMOS	6	400	30	200@3.2V	0.6	9.6	JSSC1998 [19]
0.7μm CMOS	6	175	12	160@3.3V	1.2	4.8	JSSC1996[79]
0.8μm CMOS	8	70	6	110@3.3V	0.7	14	JSSC1995 [64]
1μm CMOS	8	125	1	225@5V	4	1.2	JSSC1996[18]
0.35μm CMOS	8	200	10	210@3.0V	0.96	12.2	ISCAS2001[42]
0.5μm CMOS	8	100	3	165@5V	1.68	4.7	JSSC2001[8]
0.5μm CMOS	8	80	6	80@3.3V	0.3	19.2	ISSCC1996 [95]
0.18μm CMOS	8	30	4	18@1.8V	0.96	57	VLSI2001 [86]
0.35μm CMOS	8	10	1.5	105@3.3V	5	3.7	JSSC2001 [53]
0.35μm CMOS	7	300	60	200@3.3V	1.2	38.4	This work

CHAPTER VII

CONCLUSION AND FUTURE WORK

The key features of this work are now summarized. A front-end S/H for this 7-b F&I ADC alleviate the frequency multiplication effect. Through current mode signal processing, all internal nodes are low impedance nodes, no common mode feedback is needed and voltage supply can be low due to the low voltage swings. A very low input impedance current comparator is proposed to compare high speed interpolated currents. Reset switches in the preamplifier and latch provide fast overdrive recovery. Source follower and cascode structures are utilized to reduce the kick-back noise from the latch. A new bit synchronization scheme is proposed to not only correct errors caused by the delay difference between the coarse and fine quantizer paths, but also detect the overflow and underflow. The result is a high-speed low power ADC with a wide input bandwidth.

Major contributions in this work are:

- At the architecture level, analyzed the effect of frequency multiplication effect, which is inherent to F&I ADC, and proposed a front-end S/H as solution
- Use current mode signal processing to obtain wider folding amplifier bandwidth and reduce the delay variation caused by RC constant in the voltage mode interpolator
- Proposed a novel folding amplifier implementation based on operational transconductance amplifiers (OTA). With a folded cascode structure, the proposed folding amplifier is suitable for low voltage high speed applications.
- Proposed another folding amplifier implementation based on current mirrors. This current mode folding amplifier can provide perfect piecewise linear folding transfer characteristic.
- A low impedance I -to- V front-end is proposed to facilitate the current comparison. The desired input impedance of a current comparator is 0. In the proposed current comparator, negative feedback is used to reduce the input impedance to tens of ohms, thus the second order effect of the interpolating transistors can be negligible.

- A new bit synchronization scheme is proposed to synchronize the MSBs and LSBs. Because they are generated independently from different channel, the time mismatch must be corrected.

Several opportunities exist to extend the analysis presented here or to enhance the performance of the circuits developed. Some of the more promising areas are delineated below.

The folding and interpolating ADCs are classified as high speed low resolution. Usually they can be used as alternatives to flash ADCs. Their conversion rate is comparable to flash ADCs'. However, the resolution of folding ADCs is limited by component mismatch, i.e. resistor and/or transistor mismatch, which depends on manufacturing process. Due to the IC fabrication processes limit, the resolution of folding or flash ADCs usually can't be higher than 8-9 bits. For wireless communication and some instrumentation applications, which usually demands 12-16bit resolution, folding ADC's resolution is far less than enough. Obviously the resolution needs to be increased.

Calibration can be used to increase the resolution. However, if we limit our choice to pure folding and interpolating ADC, not much can be done. Some calibration can be employed to cancel folding amplifier and comparator offsets, but most likely the conversion speed will be sacrificed. We may consider adopting some other A/D converter architecture which can be calibrated without sacrificing much speed.

Multistage pipeline and sigma-delta are two architectures developed with redundancy to circumvent some non-idealities such as comparator offsets. Folding structures can be used as stages in a pipeline architecture. For example, to design a 14bit ADC, one can use two-stage (6+9,7+8,etc.) or three-stage(5+5+6, 4+5+7, etc.). Traditional multistage pipeline design use 1.5bit per-stage, but many designers believe a multi-bit (especially multi-bit first stage) design may yield better performance. There are many possible configurations to implement a 14bit multistage pipeline ADC. Not one single of them can be optimum in all applications. Different choices can be made depends on different

design criteria. One can develop a cost function with variables such as chip area, power, conversion speed, resolution, etc.

In multistage A/D converters employing digital error correction, A/D errors are corrected as long as they are below a threshold, thus converter resolution is primarily limited by the accuracy of the internal D/A converters and by the relative accuracy the gain matching between the composite stages. D/A converter design is relatively a mature field, and many ingenious techniques exist to produce high-accuracy, high-resolution DACs.

Accurate gain matching among multistage A/D components remains as the factor limiting resolution. Untrimmed matching of pipelined A/D converter components is limited by the intrinsic matching of integrated circuit components to about 0.1%.

Sigma-delta is usually classified as a low speed high resolution architecture. Utilizing folding ADC in this kind of architecture is not as promising as pipeline structure. Quantizers used in sigma-delta ADCs are usually low resolution (<5bit), thus the advantage of using folding structure is not significant in terms of area and power.

In high speed A/D converter design, sample-and-hold amplifier (S/H) becomes more and more important. For an ADC to achieve high input bandwidth, the S/H is mandatory. Again, there are two challenges in S/H design: resolution and sample rate. Signal dependent charge injection is a major source of distortion at high input frequencies, which will limit the SFDR and resolution. Bootstrapping can be used to alleviate this problem, but the speed of bootstrapping circuit itself may become a bottleneck. Multi-channel time-interleaving scheme can be used to increase the sampling rate dramatically. That sounds very nice, but one must solve the mismatch problem among different channels (gain, offset, timing mismatch). Some calibration schemes have been published to compensate these mismatches.

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