DESIGN METHODOLOGIES FOR BUILT-IN TESTING OF INTEGRATED RF TRANSCEIVERS WITH THE ON-CHIP LOOPBACK TECHNIQUE

A Thesis

by

MARVIN OLUFEMI ONABAJO

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2007

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
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ABSTRACT

Design Methodologies for Built-In Testing of Integrated RF Transceivers with the On-Chip Loopback Technique. (December 2007)

Marvin Olufemi Onabajo, B.S., The University of Texas at Arlington

Chair of Advisory Committee: Dr. Jose Silva-Martinez

Advances toward increased integration and complexity of radio frequency (RF) and mixed-signal integrated circuits reduce the effectiveness of contemporary test methodologies and result in a rising cost of testing. The focus in this research is on the circuit-level implementation of alternative test strategies for integrated wireless transceivers with the aim to lower test cost by eliminating the need for expensive RF equipment during production testing.

The first circuit proposed in this thesis closes the signal path between the transmitter and receiver sections of integrated transceivers in test mode for bit error rate analysis at low frequencies. Furthermore, the output power of this on-chip loopback block was made variable with the goal to allow gain and 1-dB compression point determination for the RF front-end circuits with on-chip power detectors. The loopback block is intended for transceivers operating in the 1.9-2.4GHz range and it can compensate for transmitter-receiver offset frequency differences from 40MHz to 200MHz. The measured attenuation range of the 0.052mm^2 loopback circuit in 0.13μm CMOS technology was

26-41dB with continuous control, but post-layout simulation results indicate that the attenuation range can be reduced to 11-27dB via optimizations.

Another circuit presented in this thesis is a current generator for built-in testing of impedance-matched RF front-end circuits with current injection. Since this circuit has high output impedance (>1kΩ up to 2.4GHz), it does not influence the input matching network of the low-noise amplifier (LNA) under test. A major advantage of the current injection method over the typical voltage-mode approach is that the built-in test can expose fabrication defects in components of the matching network in addition to on-chip devices. The current generator was employed together with two power detectors in a realization of a built-in test for a LNA with 14% layout area overhead in 0.13μm CMOS technology (<1.5% for the 0.002mm^2 current generator). The post-layout simulation results showed that the LNA gain (S_{21}) estimation with the external matching network was within 3.5% of the actual gain in the presence of process-voltage-temperature variations and power detector imprecision.

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It has been a pleasure and learning experience to collaborate with Xiaohua Fan and Felix Fernandez during the research by merging our test circuitry and circuits-under-test. To be more specific, Felix designed the RMS detectors/PA and Xiaohua the LNAs/down-conversion mixer of the test systems that are discussed in this thesis. In addition, countless ideas originated from discussions and problem solving sessions that I had together with my project partners and advisors.

Many thanks also go out to fellow AMSC group members for helpful conversations regarding research and course projects. Special thanks to Chinmaya Mishra, Sang Wook Park, Manisha Gambhir, Vijay Dhanasekaran, Mohamed Mobarak, Faisal Hussien, Jason Wardlaw, and Didem Turker for their recommendations during the preparations for fabrication and ongoing characterization of the chip. I would like to thank Ella Gallagher for helping to facilitate events and completion of paperwork on a regular basis; it has been nice to have an enthusiastic guide in the bureaucratic jungle.

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I am grateful for the love, encouragement, and support from my parents and brother over the years. Their influence and motivation has inspired me in many aspects of life, including education.

TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

LIST OF TABLES

I. INTRODUCTION*

Most semiconductor product improvements over the past decades are direct or indirect consequences of the perpetual shrinking of devices and circuits, allowing performance enhancements at lower fabrication cost. Yet, in the particular case of wireless mixed-signal integrated systems, the trend towards increasing integration and complexity has been paralleled by technical challenges and rising cost of testing, which can amount up to 40-50% of the total manufacturing cost [1], [2]. In recent years, built-in self-test (BIST) and design-for-test (DFT) methods for analog and mixed-signal circuits have received growing attention as part of a cost reduction effort that will allow more people globally to benefit from access to cellular communication.

The concepts of using BIST and DFT methods to facilitate the manufacturing test of digital integrated circuits are not new, and their development has led to widespread utilization and standardization in the industry over the years. In contrast, analog/RF BIST techniques are significantly less mature because failure mechanisms are more complicated and specification-based test of analog circuits requires more instrumentation resources. Another problematic aspect during the test of analog circuits is that they are more sensitive to crosstalk as well as process, voltage, and temperature (PVT) variations

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This thesis follows the style and format of the *IEEE Journal of Solid-State Circuits*.

than their digital counterparts; which entails that verification of individual blocks may not be sufficient to guarantee the desired performance when the whole system is operating [3]. With the existing challenges, current research efforts in the analog BIST field are focused on both, the improvement of fault models to enable more effective defect-oriented/structural testing as well as the development of novel specification-based/functional test approaches to verify system-level performance.

In this work, the system under investigation with respect to testability is the integrated RF transceiver, which is an essential component in wireless communication devices. It will be discussed how the proposed on-chip circuitry can be employed to route the test signal from the transmitter to the receiver sections of the transceiver. This on-chip loopback approach has the benefits of allowing built-in test (BIT) of analog blocks with integrated power detectors in combination with simultaneous system-level functional verification during production test.

I.1. Economical motivation for built-in testing of wireless integrated circuits

Comprehensive but time-consuming characterization testing is currently conducted during design debug and prior to high-volume production in order to ensure product compliance to specifications. However, the purpose of production testing is to quickly screen out substandard parts due to processing defects and variations; a more detailed discussion about the impact of test time on cost in the production phase is provided in [4], [5]. Fig. 1 shows high-level charts of the traditional post-fabrication test flow and the test flow for known-good-die testing, which is in rising demand due to the emergence of multi-die assemblies and increasing packaging cost. The needs for

continued development of DFT/BIST methods for analog cores and wafer-level burn-in tests have both been emphasized in the 2005 International Technology Roadmap for Semiconductors [6]. Regarding the flow charts in Fig. 1, test cost reduction efforts typically fall into three categories [7]:

- "Test faster" – increased equipment throughput, operational efficiency (technicians, management, process engineers), test program improvements
- "Test earlier" – early identification of faulty devices to prevent incurrence of packaging and additional test cost from further processing
- "Test less" – removal of redundant or non-critical tests based on statistical data correlations (i.e. final vs. wafer test), selection of less parts for sampled testing.

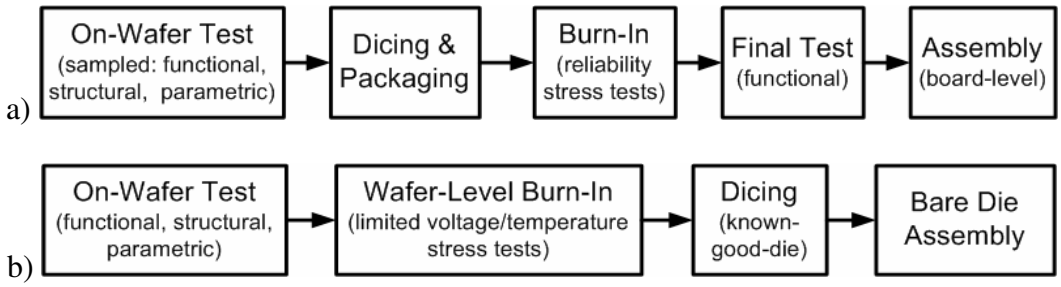


Fig. 1. Production test flows: (a) traditional (b) known-good-die

With the advent of more complex and costly system-in-a-package (SIP) and multi-chip module (MCM) technologies, there is an increased incentive for known-good-die testing at wafer sort to avoid the rising cost of subsequent packaging and final test. But, on-wafer verification at RF frequencies requires high performance and costly hardware for high-volume production testing with automatic test equipment (ATE) [8].

Replacement of conventional tests with BISTs is typically conducted with the goal to reduce test interface hardware and ATE requirements.

I.2. Alleviating manufacturing test issues

A key prerequisite to reduce RF test cost with on-chip circuitry is that the test input and output signals are limited to low frequencies in order to allow the replacement of expensive RF ATE with low-cost digital ATE. Based on the definition in [9], complete BIST requires the on-chip generation of test stimuli, analysis of the signal at the output of the circuit under test (CUT), and generation of the pass/fail result. Due to the analog nature of the signals, a full BIST of RF circuits requires long test times and significant die area overhead for on-chip signal processing [9]. Alternatively, substantial measurement circuitry and signal processing can be realized on-chip, while some remaining post-processing is still left to the external ATE. In this thesis, the latter approach will be referred to as built-in test (BIT), which is a more appropriate description since it is not a true built-in *self*-test because of the need for off-chip resources. The term BIT is also becoming more popular in the literature to distinguish between BIT and BIST. The objective of BIT is to make the use of low-cost ATE possible by simplifying the external processing to tasks such as DC output measurements or comparisons of low-frequency digital output bitstreams with stored reference vectors.

Off-chip generation of RF test input signals for a BIT should be avoided because it requires more expensive test hardware for signal generation and the use of impedance matching networks. Efficient ATE hardware development for RF test involves additional

cost considerations [8], [10] that need to be taken into account during conception of BIT methodologies. Table I provides a summary of key factors and their technical impact in the development of alternative test strategies with on-chip analog BIT circuitry.

Table I. Alternative strategies for test cost reduction

Cost Factor	**Technical Implications for Alternative On-Chip Built-In Test Approaches**
Test time	- Develop circuitry for on-chip measurements in the analog domain to avoid long signal paths to ATE and long computation time with DSP-based algorithms.
Number of inputs/outputs	- Minimize test pins as they drive up the die size and package cost. - Design on-chip circuitry to maximize coverage of internal nodes. → Multiplex test output signals.
Batch-mode testing	- Avoid test stimuli that are difficult to generate with low-cost/low-frequency (preferably below 100MHz) digital ATE signals on multiple channels. Use robust resources that are available such as clock signals. - Design for parallel testing of multiple parts (on-wafer test offers more cost-saving opportunities in batch-mode via multi-site testing; mechanical handling time at final test is longer because individual packages are processed).
Test fixture design	- Use robust on-chip circuitry to generate high frequency test signals or to up-convert signals (impedance matching and RF ports require costly test fixture designs and more expensive RF measurement equipment). - Implement communication schemes between on-chip circuitry and testers that are compatible with low-speed digital ATE.

I.3. Technical challenges associated with RF transceiver built-in testing

Consistent progress has been made towards integrating the analog and digital portions of RF transceivers using CMOS technology, which allows cost, component

count, and power consumption reduction for mobile phones and other wireless products. Single-chip transceivers have become available on the market, but the high level of integration currently presents significant test challenges due to limited access to internal analog signals and an increasing number of functions that have to be verified [5], [11]. A simplified block diagram of a system-on-chip (SOC) transceiver is shown in Fig. 2. It includes the RF front-end, analog baseband, and mixed-signal data conversion circuits at the interface between the antenna and the digital signal processor.

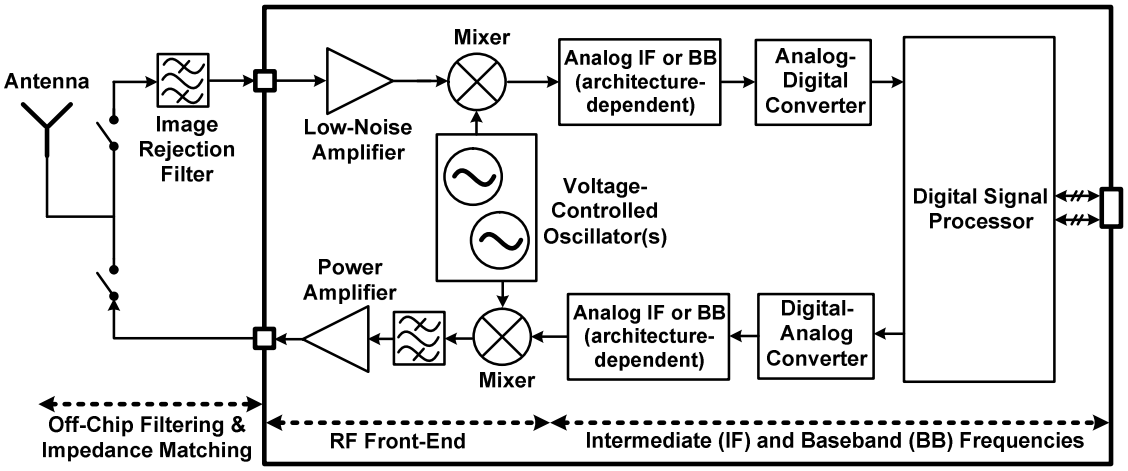


Fig. 2. Generalized block diagram of an integrated RF transceiver

Conventional on-wafer or chip-package tests of SOC transceivers similar to the one in Fig. 2 involve the generation of a RF test signal that is applied at the low-noise amplifier (LNA) input pin in order to verify the functionality of the receiver path by monitoring the baseband output of the digital signal processor (DSP). In a separate transmitter test, an input bitstream is provided to the DSP, and the corresponding output of the power amplifier or pre-power amplifier (PA) is measured and processed by the

external ATE. One issue with this method is the need for external RF signals at the LNA and PA, which mandates the technically challenging tasks of developing a test setup with impedance-matched interface hardware and expensive RF signal generation/ measurement equipment. Parallelization of tests is also problematic because the RF signal generation and measurement require dedicated ATE equipment resources as well as time-consuming digital signal processing and test synchronization [5].

I.4. On-chip measurement circuitry for RF transceiver front-ends

Another concern during production testing of transceiver SOCs is the limited availability of block-level data. Increased integration leads to more interference between blocks in addition to manufacturing process variation. For this reason, the improvement of power detectors has received growing research attention in order to perform characterization of individual blocks rather than just monitoring a few nodes with received signal strength indicators (RSSIs). Several power and signal amplitude detector topologies have been presented [12]-[15] that demonstrated promising results to provide gain and linearity estimates for pass/fail decisions in production test scenarios. Key attributes of these detectors are minimized die area, robustness to process variations, and small parasitic input capacitance to avoid degradation of the RF signal path. More extensive block-level BITs have also been proposed to extend on-chip test coverage to noise figure, input matching, and other parameters [16]-[18]. With ongoing efforts, the on-chip measurement techniques show vast potential for gaining access to internal nodes and block-level parameters, which offers more on-chip fault coverage and information for debugging designs as well as decision-making during the product ramp phase.

The first problem addressed in this thesis is a circuit-level realization of an on-chip loopback block in complementary metal-oxide-semiconductor (CMOS) technology with the capabilities of programmable attenuation and frequency translation between transmitter and receiver. System-level concepts and design constraints related to this BIT approach are discussed in section II, which also contains an elaboration why the two aforementioned features are necessary to ensure power-level compatibility and to compensate for the frequency difference between transmitter and receiver sections of transceivers that have separate uplink and downlink specifications, such as in the W-CDMA and CDMA2000 standards. The development of the proposed circuit topologies, design details, and a discussion of the post-layout simulation as well as measurement results for the loopback block can be found in section III. Another problem under investigation is the design of a test current generation circuit for built-in testing of RF transceiver front-ends, which is the focus of section IV. The target application is a novel current injection BIT technique for impedance-matched RF front-ends that permits an extension of the fault detection capability to off-chip components in the matching network. A resulting benefit is that the current injection BIT can be utilized at final package or board-level test stages in addition to wafer test. Finally, concluding remarks and opportunities for further research concerning the on-chip loopback and current injection BIT techniques are presented in section V.

II. TRANSCEIVER TESTING WITH ON-CHIP LOOPBACK

II.1. Applications

II.1.1. Functional testing

An advantage of the high integration levels in modern transceiver chips comparable to the one in Fig. 2 is that comprehensive system-level functional tests can be performed to simultaneously verify multiple blocks. It is possible to employ higher-level tests involving bit error rate (BER) or error vector magnitude (EVM) analysis instead of block-level measurements. These system-level functional tests can replace several lower-level tests, thus reducing test time and cost [4], [5], [19]. When all transceiver components are integrated on a single die, on-chip resources can be used to perform modulation, up-/down-conversion, and some digital signal processing. For specified test conditions, all blocks in the signal path must work properly to guarantee passing BER/EVM results. Since modulated signals are processed in the RF front-end, these tests also allow to detect amplitude, phase, and thermal noise problems as well as synchronization and frequency deviations of on-chip frequency synthesizers [5]. It is common practice to perform BER-based tests separately for the transmitter and receiver [5], which means that high-frequency signals still have to be generated, captured, and analyzed in the discrete time domain with large data sets due to the short sampling time requirement for high-frequency signals. With on-chip loopback, the transmitter and receiver tests could be conducted concurrently without the need for external high-frequency signals. When the modulator and demodulator are implemented on the

transceiver SOC, on-chip loopback offers the opportunity for more widespread use of EVM-based test approaches because the ATE does not require digital modulation or RF resources. EVM-based testing is not heavily used yet in the production phase [5] and the main factors that currently drive up the cost are the RF/modulation ATE requirements and prolonged test time unless alternative algorithms are used as proposed in [19].

II.1.2. On-chip calibration

If the on-chip loopback scheme is achieved without any external RF signal generation or capture, then a periodic transceiver self-check could be performed during in-field operation. With on-chip generation of the RF test signal, such a self-check creates the opportunity to utilize self-calibration schemes ([20], [21]) for compensation of manufacturing process variations, different thermal conditions, and optimization of impedance matching to external components [18]. A realization of such a true BIST (based on the definition in section I.2) would require that the digital signal processing tasks in the last column of Table II have to be executed on-chip. If the SOC does not already include sufficient resources that can be used for these tasks, then the cost of adding digital circuitry and an analog-to-digital converter to measure the DC output voltages of the power detectors must be weighted against the need for the autonomous self-check. In this thesis, the primary goal is the utilization of the loopback to reduce the technical requirements and cost associated with the ATE resources by limiting the external processing to low-frequency digital signal generation and measurements as elaborated in the following section. This approach still leaves room for one-time calibration during production testing.

Table II. Conventional transceiver tests vs. coverage with BIT
(**Rx** = receiver, **Tx** = transmitter, **LO** = local oscillator, **LB** = loopback block in sect. III, **CI** = current injection method in sect. IV, **PD** = on-chip power detector)

Typical Test	**Typical ATE Resource Requirements**	**Coverage with BIT Circuitry**	**ATE Resource Requirements with BIT**
Rx BER	- RF source to generate modulated test signal - digital output capture & comparison with stored reference	Yes (LB)	- digital signal generation (<200MHz) - digital output capture & comparison with stored reference
Tx/Rx EVM	- vector signal analyzer (phase & symbol info) or digitizers for I/Q paths (then Fast Fourier transform) - ATE host computer for intensive EVM calculations - Rx: RF source to generate the modulated test signal - Tx: RF capture and demodulation	Yes (LB)	- vector signal analyzer (baseband frequency) - ATE host computer for intensive EVM calculations
Tx output power	- RF capture, spectrum analysis with Fast Fourier transform (or spectrum analyzer)	in-band power: Yes (LB, PD) spectrum: No	- DC voltage measurement
Rx VSWR, Rx/Tx return loss (RL), Rx insertion loss (IL)	- RF network analyzer	Yes, indirect verification (CI)	- DC voltage measurement - arithmetic with complex numbers to calculate S_{21} (section IV.2.1), which depends on S_{11} (VSWR, RL, IL → calc. from S_{11})
Rx/Tx gain	- Separate tests for Rx & Tx - Rx: RF source, digital baseband capture - Tx: digital baseband input signal generation, RF output capture	Yes (LB, PD)	- digital baseband signal generation - DC voltage measurement - Simultaneous Tx & Rx verification
Rx noise figure (NF)	- direct method at room temp.: digital output capture; NF calc. from measured gain, bandwidth - or Y-factor method: requires a noise source and tests at two temperatures	Yes (LB, PD)	- direct method at room temp.: digital output capture; NF calc. from measured gain, bandwidth - or indirectly: high NF degrades BER result

Table II. continued

Typical Test	Typical ATE Resource Requirements	Coverage with BIT Circuitry	ATE Resource Requirements with BIT
Rx dynamic range	- same as for BER (using min./max. power settings)	Yes (LB, PD)	- same as for BER (using min./max. power settings)
Rx/Tx 1-dB compression points	- same as for BER (several power settings)	Yes (LB, PD)	- same as for BER (several power settings)
Rx/Tx third-order intermodulation product (IP3)	- same as for BER, but with two tone input signal (several power settings)	Yes, indirect verification (LB, PD)	- same as for BER (several power levels) - IP3 extrapolation from 1-dB comp. point with arithmetic
Rx harmonic distortion	- Fast Fourier transform and digital signal processing of digital baseband output	Yes (LB, PD)	- Fast Fourier transform and digital signal processing of digital baseband output
Rx/Tx bandwidth	- same as for BER (several RF frequency settings)	Yes (LB, PD)	- same as for BER (several on-chip LO frequency settings)
Rx RF-LO rejection	- same as for Tx output power spectrum - calculation of RF-LO rejection from spectral components	**No**, but LO leakage degrades BER	- indirect verification: same as for BER
Tx adjacent channel power ratio (ACPR)	- same as Tx output power	**No**	
Rx I/Q offset, amplitude/phase match	- same as Rx harmonic distortion (if processing is performed on outputs of the analog-to-digital converters in the I/Q paths) - or: fault detection via BER/EVM degradation	Yes, indirect verification (LB, PD)	- same as for BER (I/Q offset & mismatches degrade BER) - or: directly if I/Q digital output can be accessed prior to demodulation (same resources as Rx harmonic distortion)
Tx/Rx phase noise & carrier suppression	- same as Tx/Rx EVM - separate for Tx and Rx	Yes, indirectly (LB, PD)	- same as for Rx I/Q amplitude/phase match - only for Tx/Rx loopback combination - I/Q baseband output of Rx must be processed by ATE

II.2. The loopback testing method and related works

The system-level concept of loopback self-testing of transceivers has been introduced in the mid-nineties [22], [23]. It involves generation of the test signal in the digital baseband processor, analog-to-digital conversion, and up-conversion to the RF frequency in the transmitter section. The output of the transmitter is then routed back to the input of the receiver where it is amplified, down-converted to the baseband frequency, converted back to the digital domain, and analyzed for functionality verification of the complete transceiver. In this decade, algorithms have been demonstrated with system-level validations to improve test coverage and fault identification based on BER results [24] and spectral analysis of the receiver output [25]. With behavioral models and novel algorithms, recent works have also addressed test time reduction by using optimized bitstreams for the loopback test [26], statistical sampling circuits along the RF path [27], and demonstration of a feasible method for wafer-level production testing [28].

The aforementioned works were conducted with behavioral simulations, implementation of the transceiver system with discrete components, or off-chip realization of the loopback using on-board or ATE resources. An on-chip loopback would entail further benefits of avoiding any off-chip high-frequency interfaces and allowing post-production transceiver self-checks without measurement equipment. Moving towards this goal, on-chip block-level characterization of critical loopback components (switches, attenuator) was performed in [29].

II.2.1. Test coverage and accuracy limitations

The selection of tests that are conducted during production testing of a transceiver depend on the communication standard in use, pre-production characterization results, fabrication yield, and customer requirements among other manufacturer-specific factors. Table II provides an overview of the test coverage with the proposed BIT techniques in comparison to the common system-level RF SOC tests given in [5]. ATE resource requirements are also listed for each test, and in contrast, the BITs would allow almost identical coverage without necessitating RF equipment and off-chip high-frequency impedance matching. The exceptions are the local oscillator-RF (LO-RF) rejection and transmitter adjacent channel power ratio (ACPR), which may or may not be required in the high-volume manufacturing phase, depending on the manufacturer's test plan and initial product characterization results.

Table II lists the common tests at the final (in-package) test stage assuming proper impedance terminations. In general, cost-saving initiatives with BIT do not necessarily imply the complete replacement of testers with RF resources by low-cost digital testers during final test. At the present time, the accuracy of on-chip measurement circuits is too low to rely on them exclusively. Instead, the reduced tester resource requirements offer improved opportunities to conduct the tests in batch-mode at the wafer test stage to prevent the cost of further processing and lengthier device handling time at final test. In the high-volume production phase, test data correlations between the on-wafer and final test could then be used to screen out faulty devices early or to cautiously reduce the coverage at final test for test time reduction. The inherently lower accuracy of the BIT

can be taken into account by widening the guardbands of the pass/fail limits according to statistical correlations of the BIT data with the conventional measurement results. Such an action does not necessarily imply lower yield, especially when the measurement error with the BIT is small (e.g. 5%). The fraction of devices whose test results fall within the guardbands of the specification limits could be re-tested with conventional off-chip equipment at final test. Only a small percentage of parts should be within a guardband of 5% or less around the pass/fail limits because the measurement data typically has a Gaussian distribution and the pass/fail limits are often three standard deviations or more away from the mean. Thus, the majority of the devices could receive a pass/fail classification based on the BIT, which still reduces the overall utilization of the more expensive ATE and avoids longer device handling times at final test.

II.3. System-level overview to investigate on-chip loopback

Further evidence for the feasibility of the loopback technique can be obtained by designing the test system displayed in Fig. 3, which contains the front-end blocks of the generalized transceiver from Fig. 2. While the focus in this thesis is on the development of a loopback block, the verification was conducted together with front-end circuits designed by colleagues for a realistic proof-of-concept that takes practical concerns such as impedance-matching, parasitic loading by the test circuitry, and layout issues into account. The system was designed to target the general requirements of transceiver standards that make use of frequency bands in the 1.9GHz to 2.4GHz range.

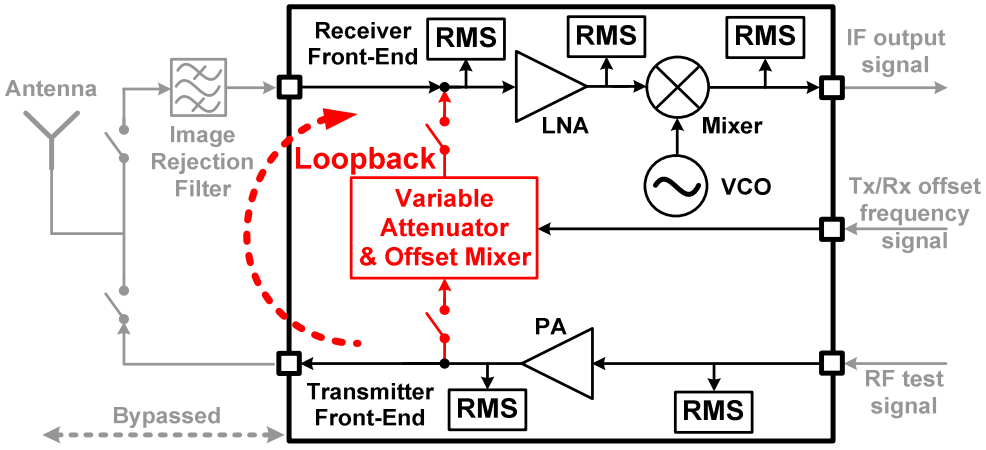


Fig. 3. Transceiver front-end test system with on-chip loopback

As shown in Fig. 3, a variable attenuator and an offset mixer are required for closing the signal path between the transmitter and receiver subsystems to simultaneously test all blocks of the transceiver at the customary power levels and

different transmit/receive frequencies mandated by standards. Strategic placement of root-mean-square (RMS) power detectors along the high frequency signal path improves the test coverage and identification of fault locations by permitting to measure output power levels, gains, and 1-dB compression points of the RF blocks [13]. In the future, an extension of the RMS detector utilization may include the self-correction of blocks with soft faults by adjusting DC bias conditions based on the measured power levels. From a system-level perspective, the gains in the RF transmitter and receiver chains are important performance indicators with respect to the achievable signal-to-noise ratio. The 1-dB compression point measurements give insights into the linearity of the analog blocks, which directly relates to the integrity of the signal and the associated bit error rate after the demodulation process.

II.4. Generalized block-level requirements for the front-end test system

As a proof-of-concept, the RF front-end circuits in Fig. 3 were realized with typical topologies and parameters for transceivers operating around 2GHz (Table III).

Table III. Proof-of-concept RF front-end parameters

Parameter	**Value**
Tx frequency	2GHz
PA output power	0dBm
Rx frequency	2.1GHz
LNA gain	21dB
Mixer gain	6.9dB

In addition to operating under the boundary conditions in Table III, the loopback block should be able to cover 40-200MHz frequency offset between transmitter (Tx) and receiver (Rx) as well as to operate up to 2.4GHz for compatibility with modern standards in this range. Table IV lists the general requirements for the proposed on-chip loopback testing approach. Besides meeting the targets in the tables, it is essential that the BIT circuits do not significantly affect the performance of the front-end blocks during normal operation. Also, the goal in this loopback implementation is to enable gain and 1-dB compression point characterization of the front-end blocks with RMS detectors, which is done at relatively high power levels. On-chip attenuators similar to those in [29] or [31] could be inserted after the loopback block to achieve lower power levels at the LNA input in case more attenuation is desired to perform BER testing closer to the sensitivity level of the receiver.

Table IV. High-level loopback block specification targets

Parameter	**Value**
Input impedance	50Ω (matched to PA)
Tx/Rx offset frequency range	40-200MHz
Attenuation range (continuous)	10-25dB
Operating frequency	< 2.4GHz
Tx/Rx isolation (loopback deactivated)	> 80dB
Output noise	communication standard-dependent*

* Integrated noise specification over the channel bandwidth must be met at the LNA input. The W-CDMA standard is used as reference in this thesis to assess noise performance because of its stringent noise requirement due to the wideband nature, which mandates a SNR of -7.3dB over the 3.84MHz channel BW [30].

II.5. Implementation overview of the loopback block

An on-chip loopback circuit without frequency shifting between transmitter and receiver has been reported in [29]. It consists of RF switches and a fixed passive attenuator. The switches were optimized for compactness and insertion loss with slightly reduced isolation compared to traditional RF switches. The π-type attenuator in [29] has high linearity because it consists of polysilicon resistors; but multiple attenuators would have to be connected in cascade or in parallel with additional switches to implement discrete attenuation settings. Adding frequency translation and continuously variable attenuation capabilities in the loopback block would accommodate to the requirements of more communication standards as well as gain and 1-dB compression testing with power detectors. As an alternative, the loopback block shown in Fig. 4 is proposed in this work to meet the requirements outlined in the previous subsection. It consists of switches with high isolation to activate the loopback in test mode and to disconnect it during normal operation. The input of the loopback is impedance-matched to the PA output and the output stage designed to drive the low-impedance node at the LNA input gate. A fixed attenuator at the loopback input reduces the power level of the test signal to ensure linear operation in the offset mixer stage. Finally, the programmable attenuation is achieved in the mixer using continuously variable loads.

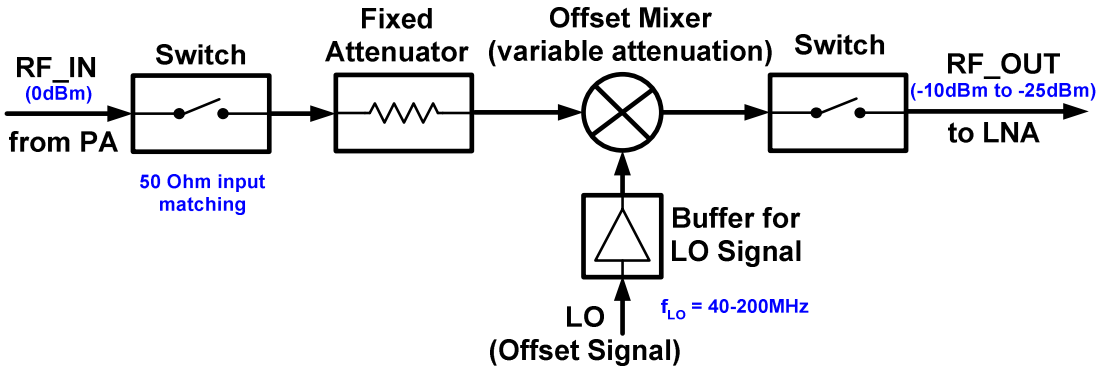


Fig. 4. Block-level loopback representation

II.5.1. Switches

Low insertion loss is a key requirement when the switches are closed. The on-resistance of the switch should be small enough to avoid degradation of the matching between the PA and the attenuator. Additionally, the switch at the PA output must have sufficient linearity to be placed at that node, which has relatively large voltage swings due to the high power level of the signal. In the off-state, high isolation is desired to avoid power leakage from the transmitter to the receiver during normal operation.

II.5.2. Attenuation

The characterization of the transceiver front-end circuitry will have to be performed at a power level well below the 1-dB compression points of all blocks for uncompressed gain measurements as well as at higher levels to determine the 1-dB compression points from the RMS detector outputs. Assuming 0dBm as output power level for the PA in an integrated transceiver to drive the off-chip load, which could be another high-power PA on a separate chip, the attenuation requirement of 10-25dB was selected to guarantee the necessary range at the LNA input for the gain and 1-dB compression point tests. Most

transceivers have multiple gain settings in various transmitter/receiver stages, which would add more flexibility and extend the attenuation range beyond the minimum requirement.

II.5.3. Frequency translation

Depending on the communication standard, the loopback block might have to provide 40-200MHz frequency shifting between the transmitter and receiver sections, which requires an offset mixer. In a production test environment, the offset signal for the mixer can be supplied by the ATE or an on-chip local oscillator (if available). Due to the relatively low frequency of the offset signal, it can be supplied to the offset mixer in the form of a digital square wave, which is easy to generate and also allows to relax the design requirements when a switching mixer is used (section III.2).

II.5.4. Design challenges

Several design challenges and constraints are associated with the loopback target specifications outlined in section II.4:

Linearity

Due to the high power levels of the PA output and the goal to test around the 1-dB compression point of the LNA, the 1-dB compression points of the circuits within the loopback block must be high enough to accommodate the test conditions. This linearity must be achieved with a low supply voltage (1.2V with 0.13μm technology). In general, BIT circuitry must be realized with minimum area overhead to be cost efficient and with minimum complexity to reduce the probability of false fails due to fabrication defects in

the BIT circuits themselves. For this reason, linearization schemes are undesirable, especially those that require additional input pins for bias circuitry or tuning. Thus, meeting the linearity requirement becomes an intricate circuit design task under the constraints.

Input impedance matching

Effective test of the on-chip power/pre-power amplifier requires that the loopback input impedance is matched to the PA output, which is 50Ω in the following design example. Resonant networks with inductors cannot be used for that purpose because they would make the loopback block too area expensive. Consequently, resistive impedance matching is a better solution because of its simplicity; but it has the trade-off of higher noise.

Transmitter-receiver isolation and loading effects

High isolation of the transmitter and receiver section is critical during normal operation to avoid SNR degradation on the receiver side due to signal leakage from the transmitter. It must also be assured that the parasitic capacitances of the switches at the loopback terminals are small enough to avoid significant influence on the equivalent impedances at these nodes at the operating frequency. Therefore, it is beneficial to add multiple switches in the signal path as well as to ground critical nodes within the loopback during normal operation in order to disconnect it with high isolation. A problem associated with the switches is that they introduce losses, which are unwanted when minimum attenuation is needed to perform block-level 1-dB compression tests. Losses due to switches are especially high when they are designed with smaller

dimensions to limit the parasitic capacitances at the loopback terminals, since smaller transistor sizes (W/L ratios) also increase the on-resistances of the switches.

Design reconfigurability

Due to the multitude of communication standards in the 1.9-2.4GHz range, an ideal loopback topology should be compatible with a large number of them and also cover a high offset frequency range. Variable attenuation should be implemented without feedback loops that are often used for dB-linear attenuators to maintain matched terminal impedances as discussed in section III. In addition, the loopback output signal should be available for single-ended or differential processing in the receiver front-end.

Noise

Another concern is adherence to the noise specifications. Being a wideband standard with a stringent noise requirement, W-CDMA will be brought into the picture as a reference to check that the noise integrated over the bandwidth is generally acceptable. At the downlink receiver, W-CDMA requires a signal-to-noise (SNR) ratio of -7.3dB over the 3.84MHz channel bandwidth [30]. Under the assumption of an approximately flat noise level over the bandwidth, the spot noise at the operating frequency will be used to estimate this integrated SNR according to:

$$SNR_{\text{integrated (dB)}} \approx SNR_{\text{spot(dB)}} - 10\log(BW_{\text{channel}}) \quad (1)$$

At the W-CDMA sensitivity specification of -106.7dBm/3.84MHz, the allowable integrated noise power is -99.4dBm/3.84MHz, which translates to an allowable spot noise of 1.2nV/√Hz at the receiver frequency. If, for example, the loopback BIT is conducted with a power level of approximately -30dBm at the LNA input, the

permissible integrated noise power is -22.7dBm/3.84MHz, which corresponds to 8.4μV/√Hz allowable spot noise. This demonstrates that the output noise requirement for the loopback block mainly depends on the power level at which the transceiver is tested and the allowable noise specified in the standard.

In this section, the loopback testing method for transceivers was discussed from a system-level perspective to show how the application-specific constraints give rise to the specifications for the loopback block. The proposed implementation was introduced together with a high-level description of the design challenges, which will be revisited in the discussion of the circuit-level performance considerations in next section.

III. ATTENUATOR AND OFFSET MIXER FOR TRANSCEIVER BIT

III.1. RF attenuator design

III.1.1. Background

Fig. 5 displays generalizations of typical RF attenuator realizations. Attenuation is achieved by selecting the proper impedances (Z_x), which also have to meet input/output matching requirements. Both, active and passive devices can be utilized as impedances, but active elements are usually preferred in applications that require continuous variation of the attenuation or multiple attenuation steps with minimal die area. Resistors are normally used if the application demands high linearity, low power consumption, or precise attenuation ratios. The T-attenuator in Fig. 5b is a good choice to match the input and output terminals to high source and load impedances, which is not the case in the loopback application. Matching to low terminal impedances is simplified with the bridge-T attenuator (Fig. 5c), but high attenuation ratios are impractical because Z_1 and Z_3 are the low-impedance elements used for the matching, creating a low-impedance connection between the input and output ports. The π-type attenuator in Fig. 5a was selected as basis for the loopback block because it is suitable for low-impedance matching with sufficient attenuation range. Furthermore, high-frequency performance of the π-attenuator is excellent since short RC time constants are formed with the parasitic capacitances due to the low-impedance nodes.

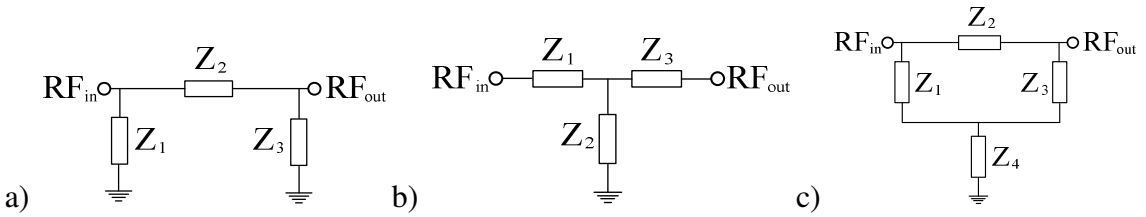


Fig. 5. RF attenuator topologies: (a) π-type (b) T-type (c) bridge-T-type

Table V. Comparison of RF attenuators

Ref.	**Type**	**Techn.**	**Freq.**	**Atten.**	**NF***	**1-dB Comp. Pt.**	**Area**	**Power**
[31]	MOS: dB-linear	0.13µm CMOS	DC -10GHz	0.8dB -35dB	1dB	5dBm	0.29mm^2	1.8mW
[32]	MOS: dB-linear	0.8µm CMOS	DC -900MHz	3.3dB -28dB	1dB	5dBm	1.57mm^2	12mW
[33]	MOS: dB-linear	0.35µm CMOS	DC-1GHz	3.4dB -23dB	0.1dB	n/a	0.21mm^2	15mW
[29]	poly resistors: discrete steps	0.25µm BiCMOS	<5GHz	<40dB	n/a	n/a (>>0dBm)	9×10^{-4}mm^2	0
[34]	poly resistors: 5dB steps	0.18µm CMOS	2.45GHz	0dB -30dB	n/a	n/a (>>0dBm)	n/a	0

* Incremental noise figure = NF - attenuation.

An overview of integrated RF attenuator performance results relevant to the loopback application is presented in Table V. Several attenuators have been reported that utilize MOS transistors to obtain linearly variable attenuation at RF frequencies [31]-[33]. These circuits allow up to 35dB attenuation range that can be adjusted linearly-in-dB. But, one issue associated with that approach is that MOS transistors in triode region are employed to vary the impedances in the attenuators (typically π-type), which results

in changes of the terminal impedances that degrade the 50Ω matching dynamically. For this reason, control circuitry was added in [31]-[33] to preserve impedance matching as the attenuation is varied. In [31], for example, the control scheme for impedance matching and control voltage linearization requires a replica attenuator and an operational amplifier in a feedback loop. Similarly, two attenuators and a reliable 50Ω reference resistor are needed in [32] and [33]. With such a high complexity and associated risk increase for failure in the test circuitry as well as large area overhead (>0.2mm^2), these attenuators are not good candidates for the loopback BIT application.

III.1.2. Input switch/attenuator: proposed implementation

The proposed loopback input stage (Fig. 6) comprises the switch/fixed attenuator and has two purposes: to terminate the PA output with 50Ω as during normal operation and to reduce the signal power at the input of the offset mixer, which relaxes the linearity requirement for the mixer. Impedance matching and attenuation is carried out in broadband fashion based on the resistive divider formed by R_{att1} / R_{att2} and the switch transistor's on-resistance [$R_{ON(M1)}$] in triode region. Based on the voltage division principle and the assumption that the impedance contribution of C_c is negligible, the resulting attenuation is:

$$Atten_{fixed(dB)} = -10\log\left(\frac{R_{att2}}{R_{att1}+R_{att2}+R_{ON(M1)}}\right) = -10\log\left(\frac{R_{att2}}{R_{att1}+R_{att2}+[\mu_n C_{ox}(W/L)_{M1}\times(V_{sw}-V_{TH}-V_{ds(M1)})]^{-1}}\right) \quad (2)$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, W is the gate width, V_{TH} is the threshold voltage, and L is the effective channel length of the device.

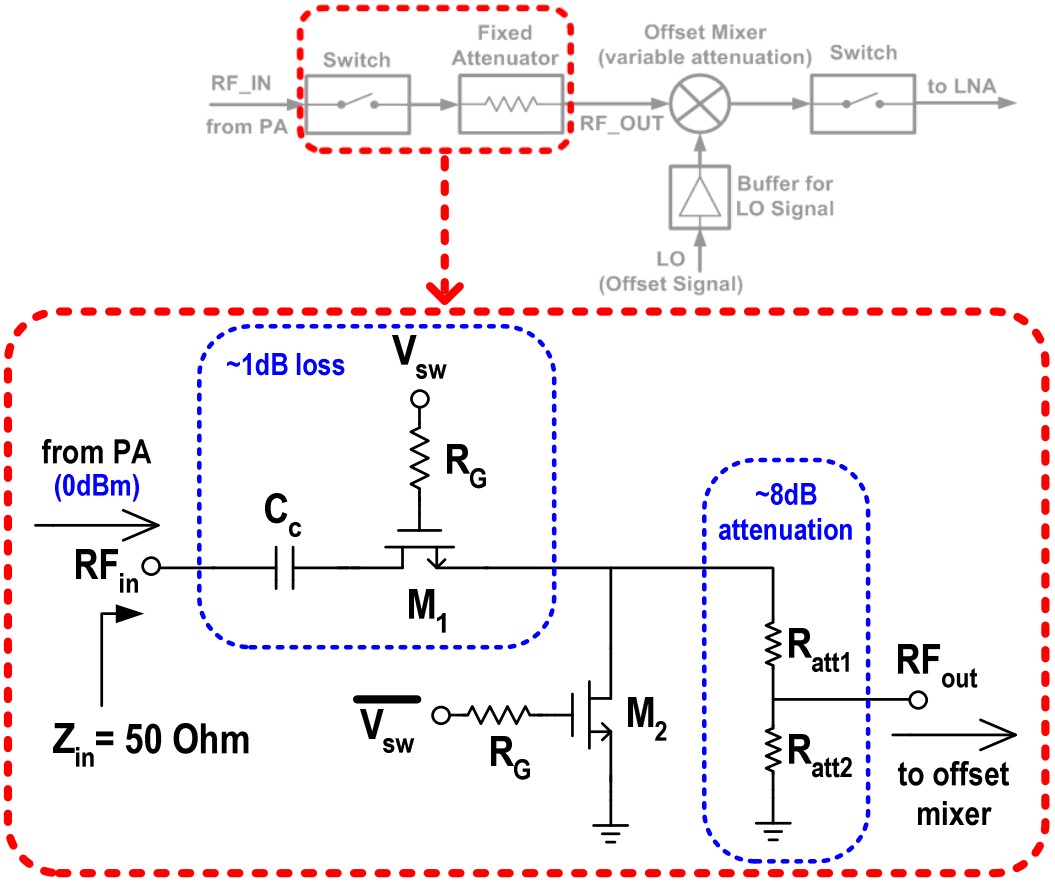


Fig. 6. Loopback input stage: RF switch and fixed input attenuator

Transistors M_1 and M_2 of the input stage compose a standard RF switch, in which M_2 increases the isolation in off-state, and the gate bootstrap resistors (R_G) enhance the linearity by lowering the variation of the channel resistance in response to the large voltage swing at the attenuator input [35]. These merits were assessed with an analysis based on preliminary simulations of the switches in Fig. 7 and the equivalent model for a single switch transistor with gate resistor R_G shown in Fig. 8. First, the parasitic

capacitances and their equivalent impedances at 2GHz were obtained with a simulation in Cadence using UMC 0.13μm technology with a 1.2V supply voltage:

$$C_{gd} \approx C_{gs} \approx 40\text{fF} \rightarrow |Z_{eq}\{C_{gd}\}| \approx 2\text{k}\Omega \text{ at } 2\text{GHz}$$

$$C_{db} \approx C_{sb} \approx 2\text{fF} \rightarrow |Z_{eq}\{C_{gd}\}| \approx 40\text{k}\Omega \text{ at } 2\text{GHz}$$

The simulated on-resistance of the switch in triode region (R_{ds}) was approximately 5Ω, and the time-dependency of the channel resistance is clear from the simplified MOS model equation for the transistor operating in triode region:

$$r_{ds(t)} = \frac{1}{(W/L)\times\mu_n C_{ox}\times(V_{G(t)}-V_{S(t)}-V_{TH}-[V_{D(t)}-V_{S(t)}])} = \frac{1}{(W/L)\times\mu_n C_{ox}\times(V_{G(t)}-V_{D(t)}-V_{TH})} \quad (3)$$

Based on the impedances of the elements in Fig. 8 and the resulting voltage divisions, it can be observed that the following conditions are desired to reduce variations of $V_{gs(t)} = V_{G(t)} - V_{S(t)}$ and $V_{ds(t)} = V_{D(t)} - V_{S(t)}$, which improves linearity:

- $R_G > |Z_{eq}\{C_{gd}\}| \rightarrow$ less $V_{gd(t)}/V_{gs(t)}$ variation (volt. drop across R_G instead of C_{gd}/C_{gs})
- $R_L > R_{ds} \rightarrow$ less $V_{ds(t)}$ variation

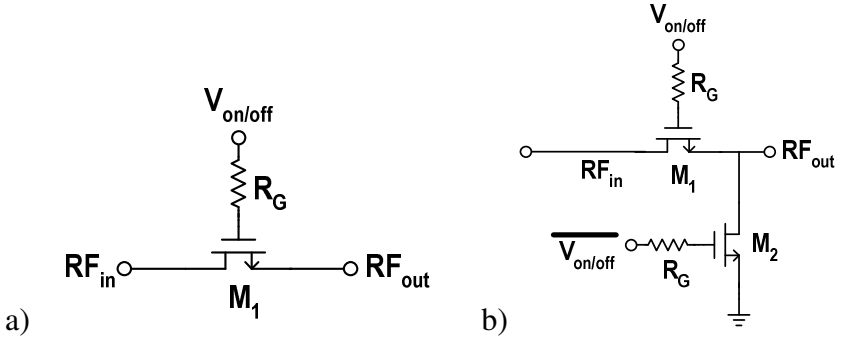


Fig. 7. (a) Simple RF switch (b) switch with shunt transistor

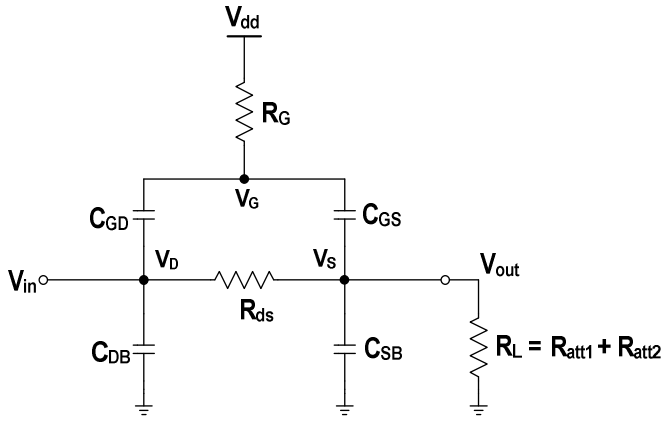


Fig. 8. Equivalent model of simple switch with gate resistance (triode region)

From a mathematical perspective, the positive effect of the gate resistance becomes clear by examining the two boundary cases with $R_G=0$ and $R_G=\infty$. Defining $V_{ds(t)}$ as the transient voltage across the channel due to the high-frequency signal $V_{in(t)}$ that is slightly larger than the output signal $V_{out(t)}$:

$$V_{ds(t)} = V_{D(t)} - V_{S(t)} = V_{in(t)} - V_{out(t)} \tag{4}$$

When $R_G=0$ and the switch is closed by applying a DC voltage of V_{dd} at the gate, then $V_{gs(t)} = V_{G(t)} - V_{S(t)} = V_{dd} - V_{out(t)}$. Substituting this expression together with (4) into equation (3) yields:

$$r_{ds(t)|R_G=0} = \frac{1}{(W/L)\times\mu_n C_{ox}\times(V_{dd}-V_{in(t)}-V_{TH})} \tag{5}$$

On the other hand, with $R_G=\infty$ and approximately equal parasitic capacitances across the gate channel junctions ($C_{gd} \approx C_{gs}$), the voltage at the gate becomes a superposition of V_{dd} and the transient average of $V_{in(t)}$ and $V_{out(t)}$ due to the voltage division between the two equal impedances of the capacitances C_{gd} and C_{gs}.

Consequently, $V_{G(t)} = V_{dd} + (V_{in(t)} + V_{out(t)})/2$. Substituting this new expression for $V_{G(t)}$, $V_{S(t)}=V_{out(t)}$, and $V_{ds(t)}$ from (4) into (3) simplifies to:

$$r_{ds(t)|R_G=\infty} = \frac{1}{(W/L)\times\mu_n C_{ox}\times(V_{dd}+\frac{V_{out(t)}}{2}-\frac{V_{in(t)}}{2}-V_{TH})} = \frac{1}{(W/L)\times\mu_n C_{ox}\times(V_{dd}-\frac{V_{ds(t)}}{2}-V_{TH})} \quad (6)$$

Comparing equations (5) and (6), it can be observed that the on-resistance of the switch without gate resistor changes linearly with the large-swing signal $V_{in(t)}$. But, with very large gate resistance, the on-resistance is significantly less sensitive and only depends on the transient voltage $V_{ds(t)}/2$, which is small since $R_{ds} << R_L$ by design.

The $V_{gs(t)}$ plots from transient simulations with a sinusoidal input at 2GHz under the anticipated operating conditions for the switch in Fig. 7a are plotted in Fig. 9. They demonstrate how the peak-to-peak voltage fluctuation from gate to source ($V_{gs\_p\text{-}p}$) decreased when the value of the gate resistor (R_G) was increased, therefore reducing the variation of the channel resistance and improving the linearity. Based on the preliminary simulations, a value of R_G=2kΩ is enough for this design to improve linearity without sacrificing too much layout area for the resistor. As shown in Table VI, inclusion of the bootstrapping resistor at the gate improved the input third-order intercept point (IIP3) by ~4dB. Notice that transistor M_2 (Fig. 7b) improves the isolation in off-state by ~8dB without significantly affecting the linearity of the switch or insertion loss in on-state.

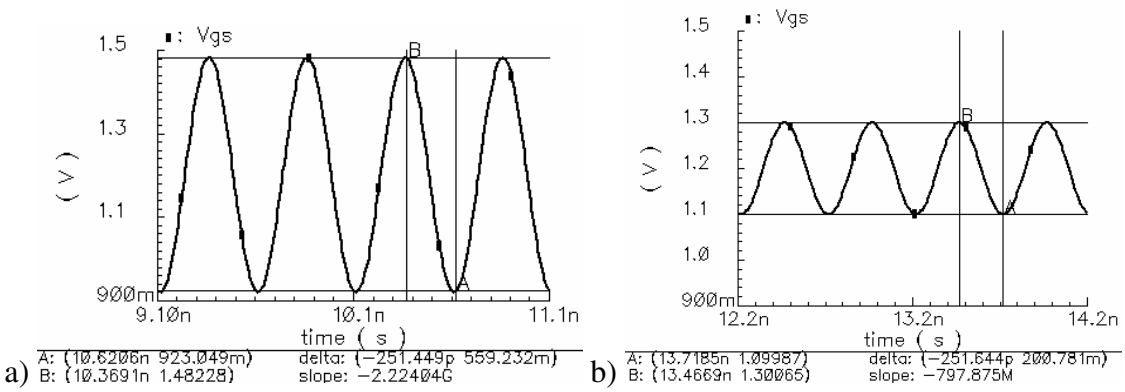


Fig. 9. RF switch: $V_{gs(t)}$ (a) R_G=0 [$V_{gs\_p\text{-}p}$=0.56V] (b) R_G=2kΩ [$V_{gs\_p\text{-}p}$=0.20V]

Table VI. RF switch preliminary simulations at 2GHz

Parameter	**Simple Switch (Fig. 7a)**	**Switch with Shunt Transistor (Fig. 7b)**	**State**
Insertion Loss	0.96dB	0.97dB	on
IIP3 without R_G	20.5dBm	20.5dBm	on
IIP3 with R_G = 2kΩ	24.3dBm	24.2dBm	on
Isolation	34.5dB	42.3dB	off
Switch Resistance	5.4Ω	5.4Ω	on

III.1.3. Component dimensions and layout

The system was designed in UMC 0.13μm mixed-mode 1P8M CMOS technology. The selection of appropriate sizes for the transistors in the switch (M_1, M_2 in Fig. 6) was done under consideration of the trade-offs involving insertion loss, linearity, and die area. Large W/L ratios are desirable to minimize the on-resistance in triode region according to equation (3) and thereby the insertion loss, but also to improve the linearity of the switch as shown by the analysis in the previous subsection. However, the drawbacks of using large W/L ratios are the die area requirement and the effect of the

parasitic capacitances from larger devices. For this BIT application, the area overhead must be minimized and the parasitic capacitances associated with the switches reduce its isolation in off-state, resulting in undesired signal feedthrough from the PA output to the LNA input. With these constraints, optimization of the switch dimensions required several iterations based on block- and system-level simulations of the layout with extracted parasitics.

Table VII lists the component values of the loopback input stage and its layout is displayed in Fig. 10. The input switch transistor (M_1) was implemented with three large RF devices in parallel and a large number of fingers in order to allow the relatively high RF current from the PA to pass with little voltage drop when the switch is on and to distribute the current flow over a sufficient number of metal contacts/vias. The high-resistivity poly resistors available in UMC 0.13μm technology were used as gate resistors (R_G) of the switches to save die area. Since the attenuation is realized with two resistors valued less than 50Ω, the cut-off frequency due to the resistor and the parasitic capacitance at the attenuator output is around 5GHz. In general, large resistances should be avoided in the attenuator to ensure low RC time constants.

Table VII. Input attenuator component sizes (UMC 0.13µm CMOS technology)

Device	Dimensions	Comments
M_1	W/L of finger = 1.6µm/0.12µm, fingers = 16, multiplier = 3	wide device to minimize loss
M_2	W/L of finger = 1.2µm/0.12µm, fingers = 10, multiplier = 1	
R_G	2.02kΩ (W=2µm, L=4.4µm)	type: high resistance poly in n-well
R_{att1} , R_{att2}	25Ω (W=5µm, L=15.6µm)	type: poly in n-well; R_{att1}=R_{att2}=22.5Ω would result in ideal resistive matching since $R_{ds(M1)}$=5Ω.
C_C	3.1pF (W=45µm, L=45µm)	type: metal-insulator-metal (MIM)

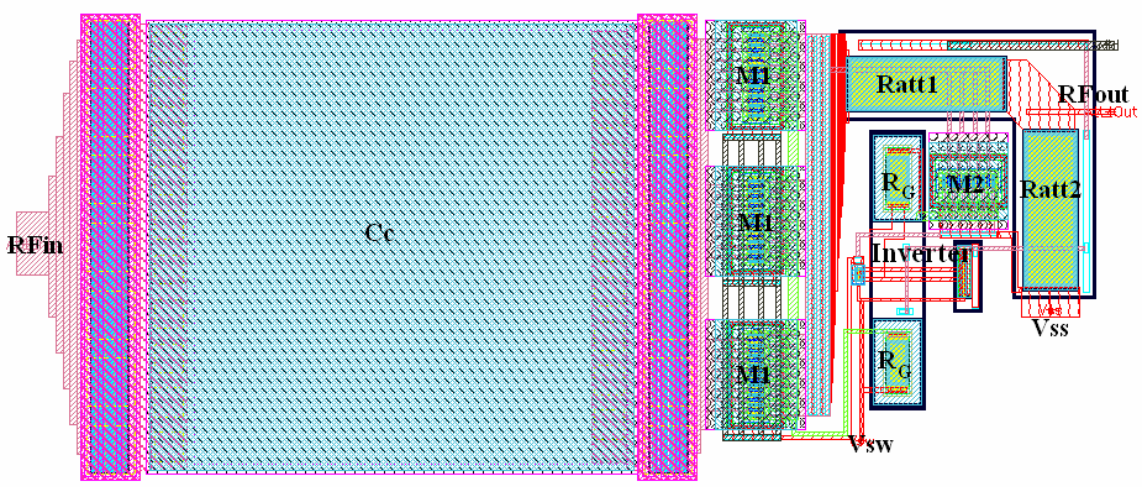


Fig. 10. Input switch and attenuator layout (50µm × 115µm)

III.1.4. Post-layout simulation results

To assess the performance of the loopback input stage in Fig. 10, the parasitic capacitances, resistances, and inductances were extracted from the layout. A 50Ω test signal port was connected to the input (RF_{in}) and the load in the simulation was equivalent to the capacitance at the attenuator output (RF_{out}) when it is connected to the offset mixer in the loopback. Table VIII contains a summary of the post-layout simulation results for the input switch/attenuator combination. Fig. 11 shows that the attenuation is relatively flat from 1.9GHz to 2.4GHz with a change of 0.3dB. Adequate input matching was achieved with S_{11} < -10.2dB over the frequency range of interest in the post-layout simulation (Fig. 12).

Table VIII. Input switch and attenuator simulation results

Parameter (at 2GHz)	**Specification**
Attenuation	8.2dB
S_{11} (1.9-2.4GHz)	< -10.2dB
Input 1-dB Compression Point	11.5dBm
IIP3	20.3dBm
Isolation (off-state)	54.8dB
Incremental Noise Figure*	0.7dB
Power Consumption	0W
Supply Voltages (Vdd/Vss)	1.2V / 0V
Area	$5.8\times10^{-3}mm^2$

* Incremental noise figure = NF – attenuation.

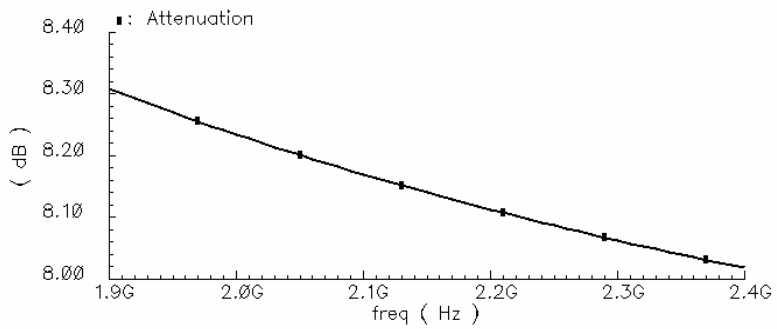


Fig. 11. Input switch and attenuator: attenuation vs. frequency

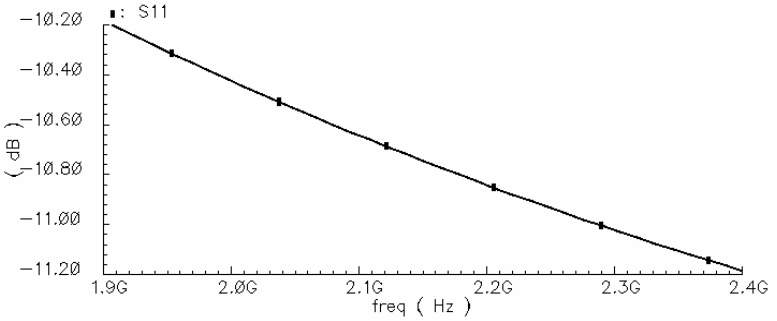


Fig. 12. Input switch and attenuator: S_{11} vs. frequency

The simulated input-referred 1-dB compression point of the input stage is 11.5dBm as indicated in Fig. 13, which ensures linear operation with the 0dBm signal at the attenuator input in the prototype front-end. Fig. 14 includes plots of the noise figure (NF), attenuation, and incremental NF vs. frequency. The incremental NF isolates the noise added by the circuitry because the effect of the attenuation on the SNR degradation is excluded (incremental NF = NF - attenuation). For this reason, the incremental NF is often reported in the literature as a basis for comparing attenuators with different attenuation ratios. With an incremental NF of 0.7dB at the operating frequency, the noise added by this attenuator is similar to the others in Table V. Fig. 15 shows that the simulated isolation of the input stage alone is more than 53dB when it is switched off.

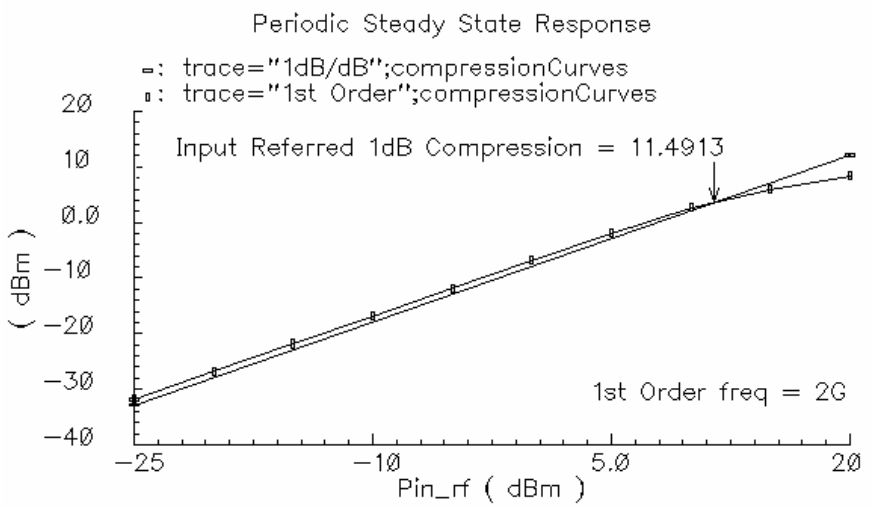


Fig. 13. Input switch and attenuator: input 1-dB compression point

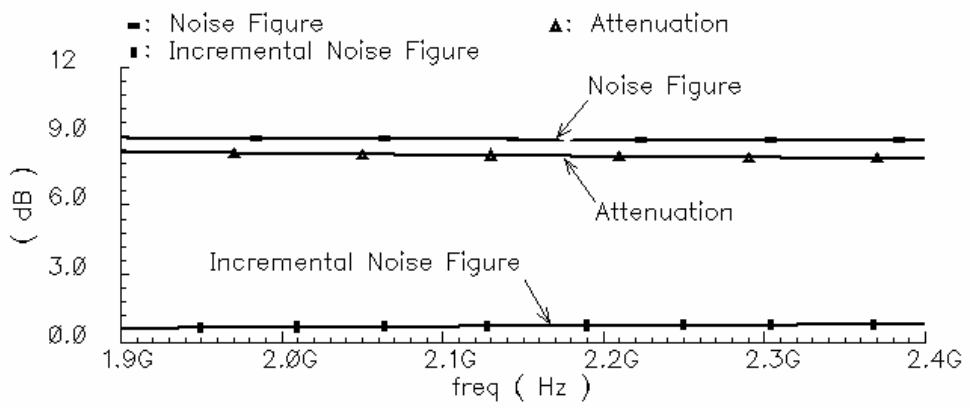


Fig. 14. Input switch and attenuator: noise figure and incremental noise figure

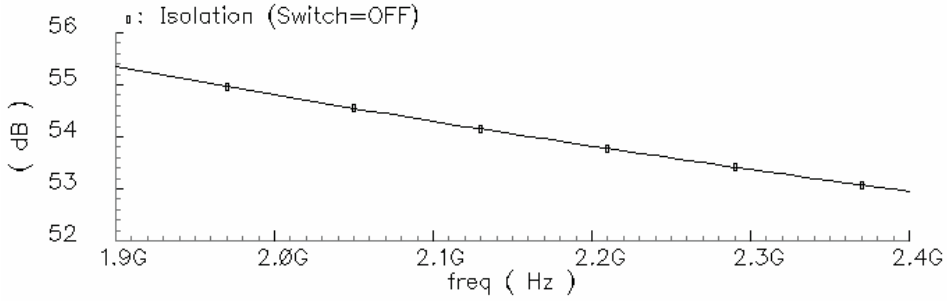


Fig. 15. Input switch and attenuator: isolation in off-state

III.2. Offset mixer with variable gain for loopback testing

III.2.1. Background and application-specific constraints

It is important to keep in mind that the offset mixer requirements are different from the typical up- and down-conversion mixer design constraints. The following conditions and their effects played key roles in the construction of a suitable mixer topology:

- Extensive signal conditioning is not practical because the input and output signals are both at RF frequencies. This eliminates many conventional single-balanced topology options used in down-conversion applications with subsequent baseband filters or DC offset cancellation schemes.
- Harmonic cancellation mixers for up-conversion applications tend to be too complex and area expensive for usage in a BIT circuit.
- With a signal power of 0dBm at the input of the loopback block and ~9dB attenuation prior to the mixer, a minimum conversion gain of -3dB is needed to test around the -11.4dBm 1-dB compression point of the LNA in this work. Higher mixer gain improves the robustness of the BIT to PVT variations by allowing the measurement of a higher 1-dB compression point that might incur, but in a production scenario only a pass/fail test at the expected 1-dB compression point can be used to determine whether the part meets the minimum specification, which is why testing at higher power levels is optional. Even with 9dB attenuation in the loopback input stage, the input 1-dB compression point of the mixer should be better than -9dBm, which translates into an IIP3 requirement of >1dBm. In combination

with the limited voltage headroom due to the 1.2V supply, meeting the linearity specification is not trivial without the use of area-consuming inductors in the bias scheme that would save headroom.

- The local oscillator (LO) signal frequency is equal to the frequency offset between transmitter and receiver, which is only 40-200MHz. Since the LO signal can be supplied by the ATE in a production environment, a rail-to-rail digital signal is a good choice for ease of generation. It also has the benefits of short switching transition times and small on-resistance of the switched transistor due to the large overdrive voltage. Since the parasitic capacitances have higher impedances at the relatively low offset frequency, the LO signal leakage via gate-drain and gate-source capacitances is not as critical as with high-frequency LO signals.

Thus far, only one specialized offset mixer for the loopback application has been published to the best knowledge based on recent literature searches. The passive offset mixer topology in [36] was proposed for the loopback scenario that involves system-level tests at customary power levels. This mixer is optimized for loopback testing without the need of any filtering, since the quadrature mixing scheme results in attenuation of the undesired mixing by-products of more than 40dB below the wanted signal. However, a drawback of the scheme is that the transmitter output and offset signals must be supplied in quadrature form. Consequentially, the single-ended output buffer (PA) cannot be included in the test loop and a tunable on-chip ring oscillator was added to provide the offset signal. As explained in II.3, the offset mixer in this thesis

work must also support block-level characterization of the front-end circuits to improve the fault coverage of the loopback test. Therefore, the required loopback output power level has to be higher than during normal operation in order to verify the 1-dB compression point of the LNA. Additionally, the loopback also has to provide a large attenuation tuning range for testing linear characteristics. The passive mixer in [36] can generate an output power of up to -20dBm, which is not high enough for the proposed loopback test approach that is the target application for the mixer in this thesis.

Table IX. Comparison of relevant mixer performance specifications

Ref.	**Type**	**CMOS Techn. / V_{dd}**	**f_{in} / f_{LO}**	**f_{out}**	**Conv. Gain**	**IIP3**	**NF (SSB)**	**Power**
[37]	active (Gilbert)	0.35µm / 3V	1.8GHz / (n/a)	IF n/a	10.4dB	-6dBm	7.2dB	15.6mW
[37]	passive	0.35µm / 3V	1.8GHz / (n/a)	IF n/a	-7.5dB	16dBm	10.0dB	0
[38]	active (Gilbert, inductors)	0.18µm / 1.8V	2.45GHz /f_{in}±25MHz	IF 25MHz	27dB	-3.7dBm	12.5dB	n/a
[39]	active (double-balanced)	0.18µm / 1.5V	5.8GHz / 5.6GHz	IF 0.2GHz	10.4dB	-10.7dBm	13.6dB	11.8mW
[40]	active (I/Q subharm. cancel.)	0.18µm / 1.8V	baseband / 0.96-0.99GHz (8 phases)	RF 1.92-1.98GHz	14.5dB	0.5dBm	n/a	18.0mW
[41]	active (switched -Gm)	0.18µm / 1V	f_{LO}±10MHz / 2GHz	IF 10MHz	10.0dB	6dBm	24.2dB	1.1mW

Table IX summarizes results that have been reported for mixer designs intended for diverse applications to emphasize the trade-offs between gain, linearity, active vs.

passive types, up- vs. down-conversion. With the exception of [41], high conversion gains were typically achieved with linearity lower than the requirement for the loopback application (>1dBm in this work). But, a disadvantage of the mixer in [41] and high-performance mixers in general is that they are typically double-balanced to be able to suppress even-order harmonics. The on-chip signal from the transmitter is usually single-ended and it is also desired to have a circuit-level loopback solution with single-ended or differential output option. Avoiding circuitry in the loopback for single-ended to differential conversion and differential to single-ended conversion is in the best interest to minimize the area overhead of the BIT. An active single-ended to differential converter prior to the mixer would also be hard to design due to the large input signal swing in combination with the strict gain/phase mismatch requirements for fully-differential RF circuits. Up-conversion mixers as the ones reported in [37] and [42] are frequently implemented as passive types followed by one or more amplifiers in the transmitter whose RLC loads also perform filtering. This approach is not suitable for the loopback block since employing inductors in the BIT circuitry would be too costly in terms of die area.

III.2.2. Proposed mixer topology

Based on the design constraints addressed in the previous subsection, an active switching mixer with tunable gain and minimized die area is needed for the anticipated loopback application. The single-balanced structure displayed in Fig. 16a is a good starting point for the discussion of the offset mixer operation. In this circuit, transistor M_1 converts the RF input voltage signal to a current signal. It is biased by resistor R_{B1}

and decoupled from the input attenuator stage by capacitor C_{c1}. Transistor M_2 is switched on/off by the differential digital rail-to-rail LO signal, which results in alternate steering of M_1's output current into the loads R_L of the two branches. The problem created by this operation is that the voltages V_x and V_y consist of the RF signal component superimposed by a periodic fluctuation between the DC level when M_2 is switched on and V_{dd} when M_2 is switched off, as visualized in Fig. 16b. With typical values of R_L, the periodic voltage fluctuation is much larger than the small-signal RF voltage signal and it has the same period (T_{LO}) as the LO, resulting in undesired spectral components as demonstrated by the mathematical analysis in Appendix A. In the loopback application, the voltage fluctuation effect is particularly problematic because the large signal energies of the spectral components at the LO frequency and its harmonics cause saturation of the LNA.

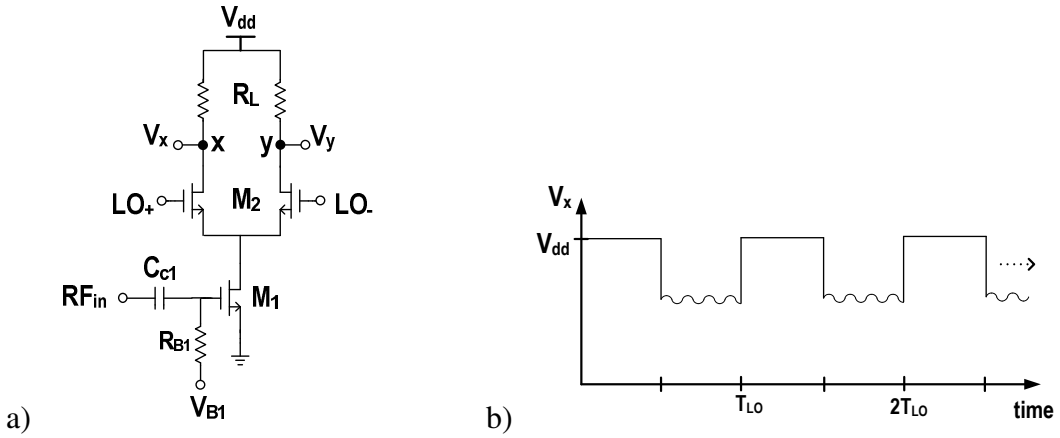


Fig. 16. (a) Simple single-balanced mixer (b) transient V_x
(switching operation: M_2 turned on/off by digital LO signal)

Fig. 17a illustrates a modification that was made to the single-balanced mixer in order to alleviate the periodic voltage variation problem. Transistors M_3 and M_4 were added to stabilize the DC voltages at nodes "x" and "y". Similar to the traditional Gilbert mixer, M_2 and M_4 produce the benefit of LO even-harmonic cancellation when they are sized and biased identically, which also makes balanced mixing possible when it is necessary to apply a differential input signal at the gates of M_1/M_3. In single-ended operation, M_3 is biased with the same voltage (V_{B1}) as M_2, so that the DC voltage levels in the auxiliary branches are identical to the ones in the single-balanced core. Since the phases of the LO signal at the gates of M_4 and M_2 are reversed, nodes "x" and "y" are always connected to one switch transistor that is turned on. Thus, a constant DC voltage level can be maintained and ideally the only transient voltage variation at V_x is due to the RF signal component, which is visualized in Fig. 17b and derived mathematically in Appendix A.

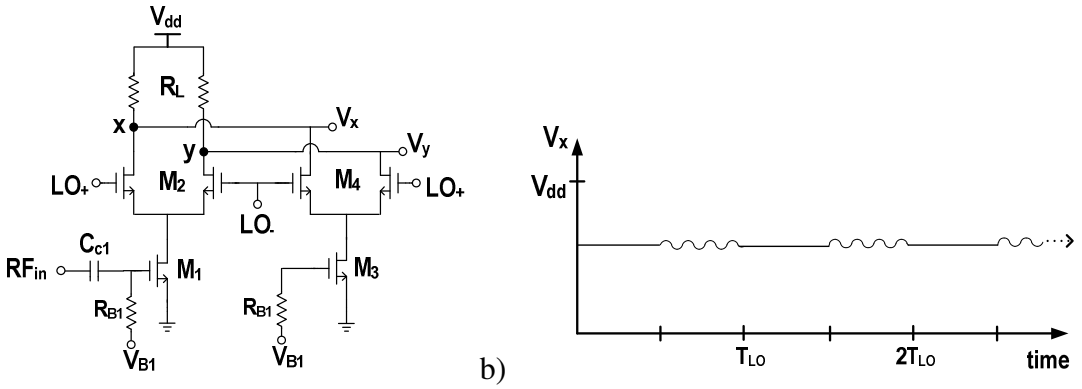


Fig. 17. (a) Single-balanced mixer with DC voltage stabilization (b) transient V_x

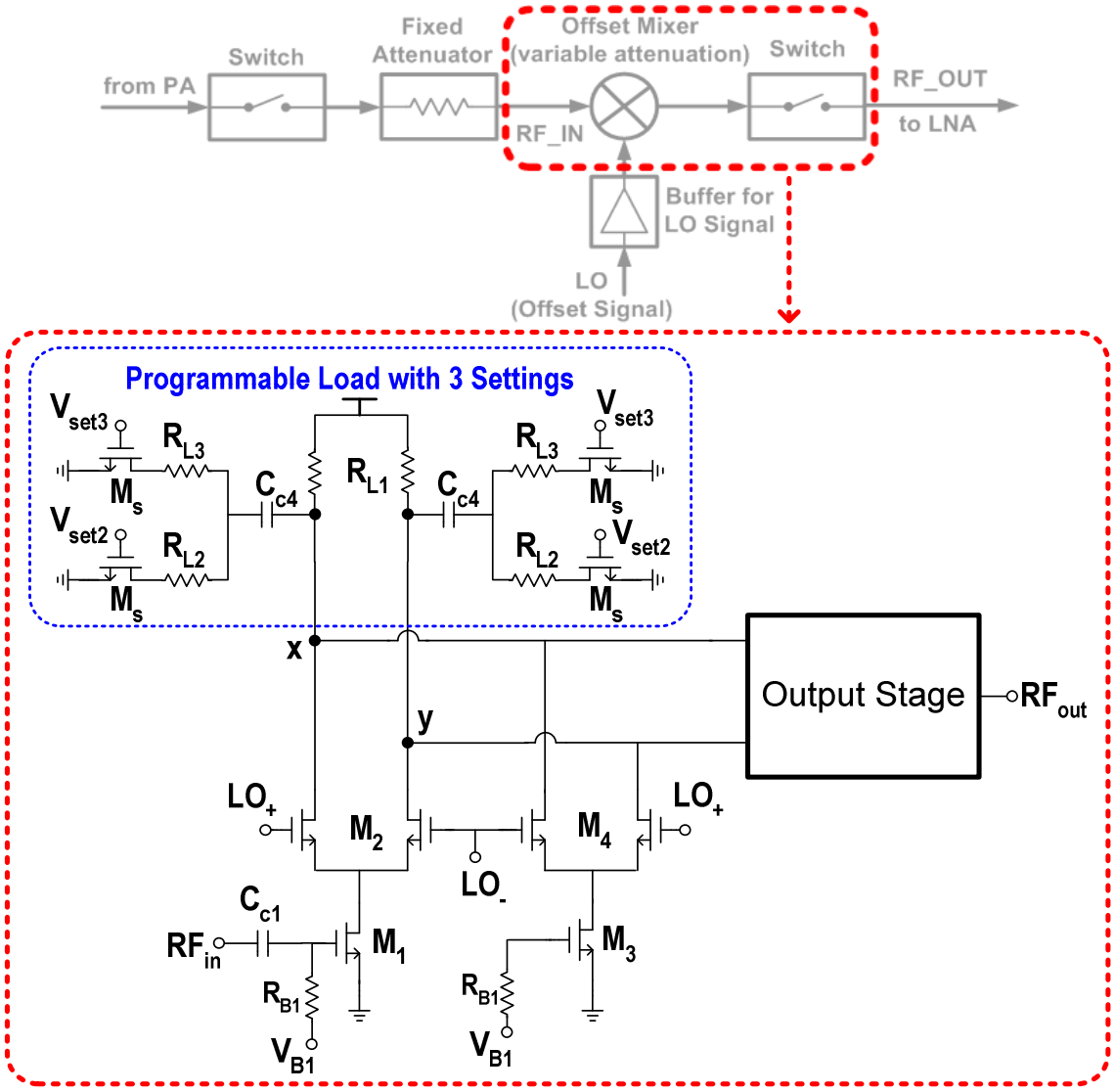


Fig. 18. Offset mixer schematic

Fig. 18 shows the proposed offset mixer, which is based on a single-balanced structure (M_1 and M_2) with a single-ended RF input and a differential rail-to-rail low-frequency LO signal that results in hard-switching of M_2. As explained above, transistors M_3 and M_4 in the auxiliary branch serve in stabilizing the DC operating points at nodes "x" and "y". Discrete gain steps can be realized by reducing the loads at nodes "x" and

"y" with the switched parallel resistors R_{L2} and R_{L3}. In this design, two additional settings were implemented with control voltages V_{set2} and V_{set3} to achieve a gain range of approximately 14dB in the core of the mixer. A load-switch scheme with a coupling capacitor (C_{c4}) helps to prevent DC operating point differences in the mixer core with the three settings. Using decoupling also has the advantage that NMOS switch transistors (M_s) can be employed instead of PMOS devices, which allows to achieve low on-resistance with smaller device size and therefore less parasitic capacitance at the critical nodes "x" and "y".

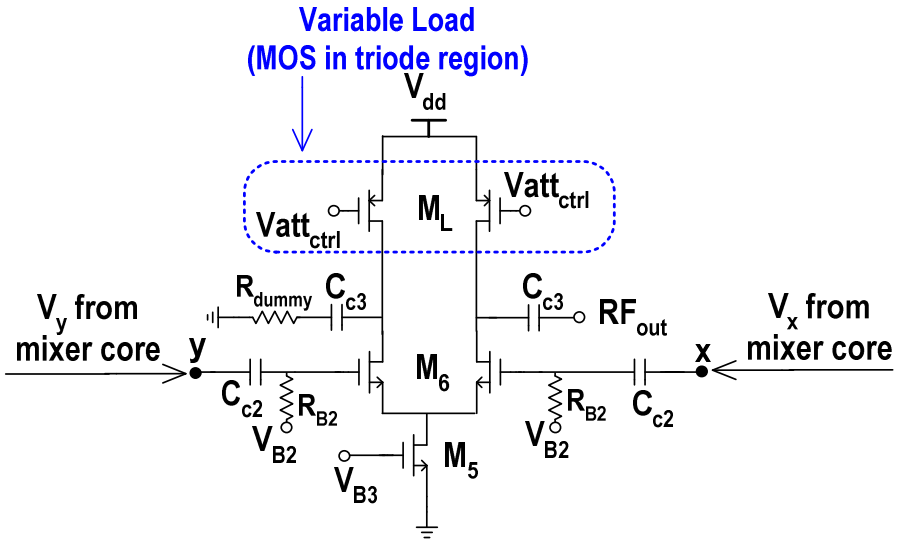


Fig. 19. Offset mixer output stage

The output stage (Fig. 19) of the mixer consists of a differential pair (M_6) with a common tail current source (M_5). This stage provides the capacity to drive the low-impedance node at the gate of the LNA as well as further gain tuning. The resistance of

the triode-region load (M_L) at the output can be varied with the control voltage $Vatt_{ctrl}$, which allows changing the mixer gain ~6dB in continuous fashion. Hence, the overall gain range in this offset mixer design is approximately 20dB. Notice that resistor R_{dummy} is added for more balanced operation since only a single-ended output (RF_{out}) is used. Without R_{dummy}, the second output can be used to connect to a fully-differential LNA.

Voltage headroom in the mixer core (Fig. 18) is limited with a 1.2V supply and M_1 being biased with a relatively large saturation voltage ($V_{dsat} \approx 250mV$ in this case) in order to design for the high linearity requirement. Sufficient voltage margin is required for M_1 to remain in saturation region despite of the large signal swings due to the high input power level and the voltage drop across R_{L1}. For this reason, M_1 and M_3 do not have a common tail current source, which together with the single-balanced nature of the mixer core leads to the appearance of the RF input signal as common-mode signal at nodes "x" and "y" (Fig. 18). A detailed mathematical analysis of the spectral components resulting from the mixing can be found in Appendix A. RF feedthrough suppression of the common-mode signal at the input frequency (ω_{RFin}) is accomplished in the output stage (Fig. 19) by the common-mode rejection property of the differential pair (M_6) with a shared tail current source (M_5). From the derivation in Appendix B, it is found that the common-mode gain (A_{v_cm}) in the output stage is:

$$A_{v\_cm} = A_{v(\omega_{RFin})} = \frac{v_{RFout+}}{v_{mix+}} = \frac{g_{m6} R_{ON(ML)}}{1 + 2 g_{m6} (r_{ds5} \| \frac{1}{j\omega C_p})} \tag{7}$$

where g_{m6} is the transconductance of M_6, r_{ds5} the drain-source resistance of M_5 in saturation region, $R_{ON(ML)}$ the channel resistance of M_L in triode region based on

equation (3), and C_p the parasitic capacitance at the source node of M_5. Selecting $g_{m6}\times[r_{ds5}\|1/(j\omega C_p)] > g_{m6}\times R_{ON(ML)}$ by design, the undesired common-mode component is attenuated based on (7).

The conversion gain of the mixer with a single-ended output ($G_{mix\_s\text{-}e}$) can be derived by combining the gains from the single-balanced mixer core (M_1, M_2) and the differential pair at the output (from Appendix A):

$$G_{mix\_s-e} = \frac{v_{RFout+} - v_{RFout-}\,(@\ \omega_{RFout} = \omega_{RFin} + \omega_{LO})}{v_{RFin}\,(@\ \omega_{RFin})} = \frac{2 g_{m1} R_L}{\pi} \times \frac{g_{m6} R_{ON(ML)}}{2} \tag{8}$$

where a square wave LO waveform with amplitude of "1" was assumed to model the switching operation. If the output is taken in differential fashion, then the conversion gain becomes (from Appendix A):

$$G_{mix\_diff} = \frac{v_{RFout+} - v_{RFout-}\ \ (@\ \omega_{RFout} = \omega_{RFin} + \omega_{LO})}{v_{RFin}\ \ (@\ \omega_{RFin})} = \frac{2 g_{m1} R_L}{\pi} \times g_{m6} R_{ON(ML)} \tag{9}$$

Output switch

Disconnection of the loopback block from the LNA input is possible by setting $Vatt_{ctrl}$ high (V_{dd}) and V_{B2}/V_{B3} low (ground) during normal operation. Turning M_1 off by setting V_{B1} low further increases the isolation between PA and LNA. As a consequence, the loopback block can be connected directly to the LNA without an additional switch in the signal path that would attenuate the signal.

DC biasing

The offset mixer in Fig. 18/Fig. 19 was designed with the biasing scheme shown in Fig. 20 for transistors M_1, M_3, and M_5. An external variable resistor is required to adjust

the bias current during the test of the prototype chip. In practice, the bias voltages (V_{Bx}) could also be supplied with an on-chip voltage reference. Alternatively, ATE current sources could provide the bias currents (I_x) instead of using external resistors (R_{pot}).

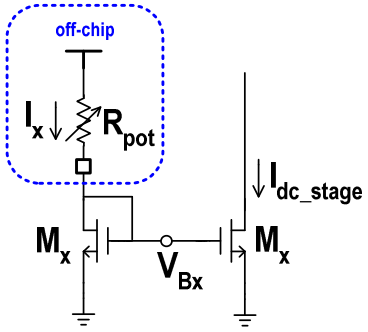


Fig. 20. Biasing scheme for M_1, M_3, and M_5 in the offset mixer

III.2.3. Component dimensions and layout

The device sizes for the offset mixer in Fig. 18/Fig. 19 are listed in Table X and the layout is displayed in Fig. 21. Small sizes were used for the RF input transistors in the mixer core, which were biased with a large saturation voltage to meet the linearity requirement. Since the LNA under test is single-ended, resistor R_{dummy} was connected to one output of the differential stage to emulate the load presented by the equivalent impedance looking into the gate of the LNA at the resonance frequency. This has the advantage of better balanced operation in the mixer. Coupling capacitor C_{c1} was implemented with a MOS capacitor to reduce the mixer area, but the other coupling capacitors were implemented with metal-insulator-metal (MIM) types to avoid parasitic

capacitances to ground at nodes that have higher impedances, which was done to minimize RC time constants for improved RF performance.

Table X. Offset mixer component sizes (UMC 0.13μm CMOS technology)

Device	Dimensions	Device	Dimensions
$\mathbf{M_1}$, $\mathbf{M_3}$	W/L of finger = 2.32μm/0.12μm, fingers = 4	$\mathbf{R_{L1}}$	290Ω (W=0.36μm, L=13μm), [poly]
$\mathbf{M_2}$, $\mathbf{M_4}$	W/L of finger = 2.88μm/0.12μm, fingers = 6	$\mathbf{R_{L2}}$	190Ω (W=0.36μm, L=8.6μm), [poly]
$\mathbf{M_S}$	W/L of finger = 4.98μm/0.12μm, fingers = 4	$\mathbf{R_{L3}}$	80Ω (W=0.36μm, L=3.6μm), [poly]
$\mathbf{M_5}$	W/L of finger = 3.26μm/0.48μm, fingers = 12, multiplier = 2	$\mathbf{R_{dummy}}$	160Ω (W=0.36μm, L=7.2μm), [poly]
$\mathbf{M_6}$	W/L of finger = 2.64μm/0.12μm, fingers = 16	$\mathbf{C_{c1}}$	1.5pF (W=L=11.4μm), [MOS Cap. to save area]
$\mathbf{R_{B1}}$	44.5kΩ (W=0.5μm, L=20μm), [high resistance poly in n-well]	$\mathbf{C_{c2}}$	0.3pF (W=L=14μm) [metal-insulator-metal Cap.]
$\mathbf{R_{B2}}$	2.8kΩ (W=2μm, L=6μm), [high resistance poly in n-well]	$\mathbf{C_{c3}}$, $\mathbf{C_{c4}}$	3pF (W=L=45μm), 5pF (W=L=58μm) [metal-insulator-metal Cap.]

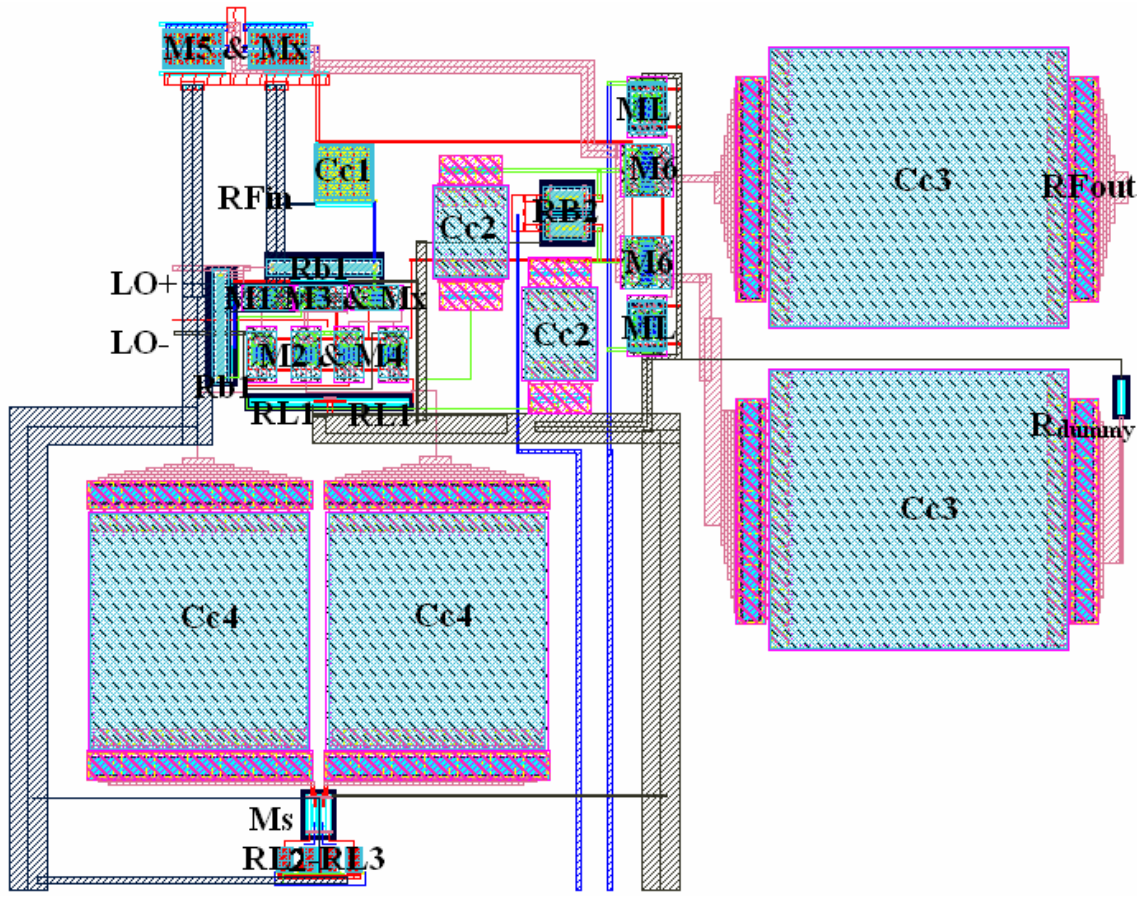


Fig. 21. Offset mixer layout (185µm × 230µm)

III.2.4. LO input buffer

An input buffer (Fig. 22) was designed to enable testing with a single-ended sinusoidal or square wave LO signal that has slow transition times, which reduces the ATE requirements. For example, with a single-ended rail-to-rail sinusoidal input at 100MHz, the differential square wave output signal of the LO has transition times of ~50ps, which has the advantage of better mixer performance due shorter on/off overlap duration of the switching transistors in the two branches. The digital inverters in path 1 were sized with minimum channel length and a slightly larger W/L ratio in the last stage

to optimize for speed (transition times). The inverters in path 2 have equal sizes and smaller channel widths to obtain a comparable propagation delay.

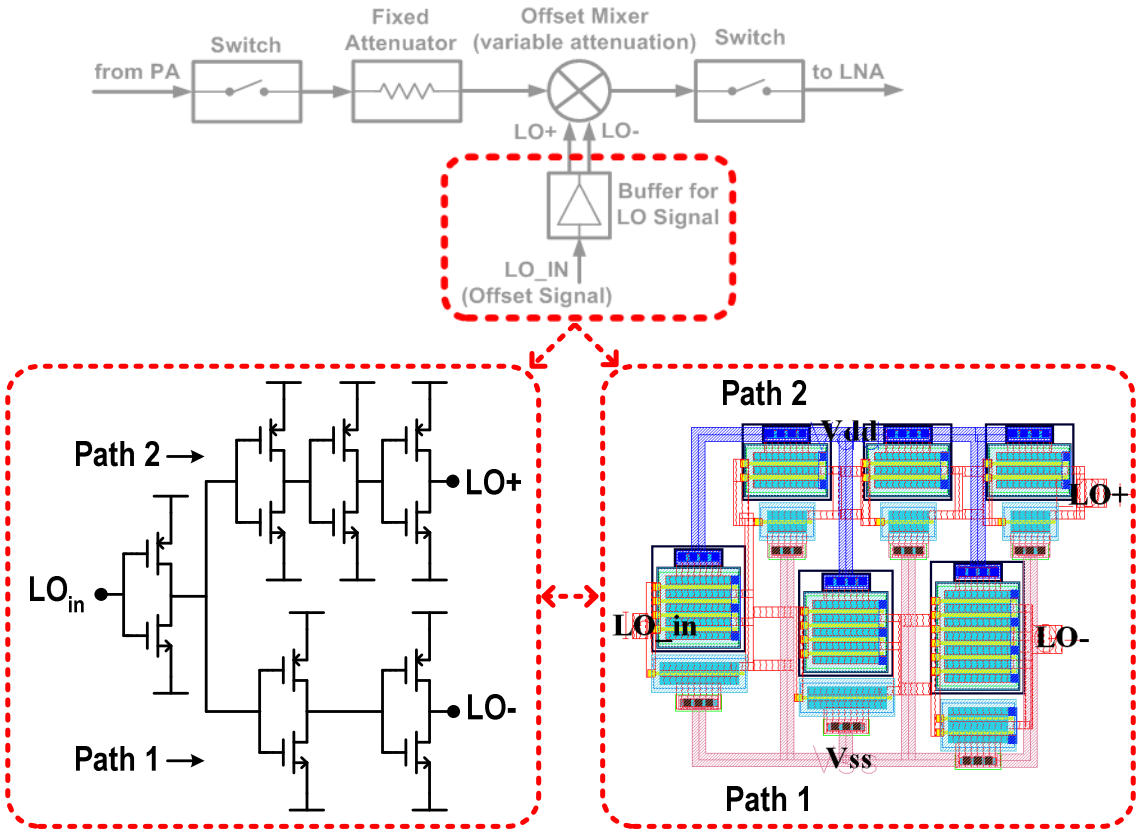


Fig. 22. LO input buffer schematic and layout (15μm × 20μm)

III.2.5. Post-layout simulation results

This section includes the characterization data obtained from simulations of the offset mixer in Fig. 18 together with the LO input buffer in Fig. 22. Unless noted otherwise, a 100MHz sinusoidal signal was applied to the LO buffer input to represent the worst-case transition times, which will be shorter if a square waveform is supplied.

The simulation results for the unloaded offset mixer are listed in Table XI. It has a conversion gain of 0.9dB, which changes approximately 0.8dB from 1.9GHz to 2.4GHz (Fig. 23). The input 1-dB compression point with maximum mixer gain is -9.8dBm (Fig. 24), therefore the fixed attenuator at the PA output (0dBm) is needed to achieve acceptable performance.

Table XI. Offset mixer simulation results

Parameter (f_{RFin}/f_{RFout} = 2GHz/2.1GHz)	**Setting: Min. Mix. Gain (Max. Loopback Atten.)**	**Setting: Max. Mix. Gain (Min. Loopback Atten.)**
Conversion Gain	-20.6dB	0.9dB
Input 1-dB Compression Point	-4.1dBm	-9.8dBm
IIP3	8.3dBm	0.1dBm
Noise Figure (SSB)	29.8dB	24.1dB
Power Consumption	7.8mW	7.7mW
Supply Voltages (V_{dd}/V_{ss})	1.2V / 0V	
Area	$42.6\times10^{-3}mm^2$	

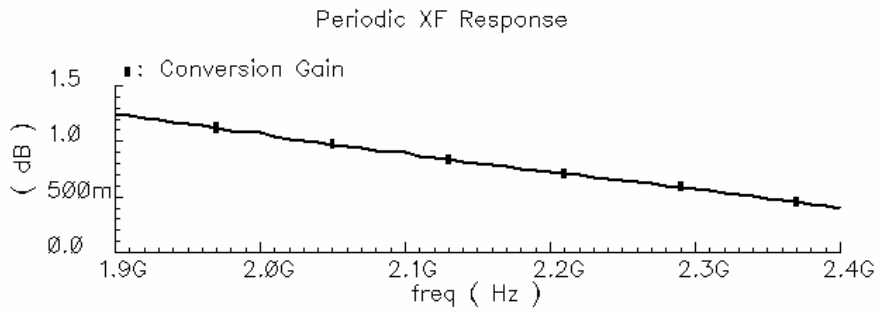


Fig. 23. Offset mixer: max. voltage conversion gain vs. RF frequency

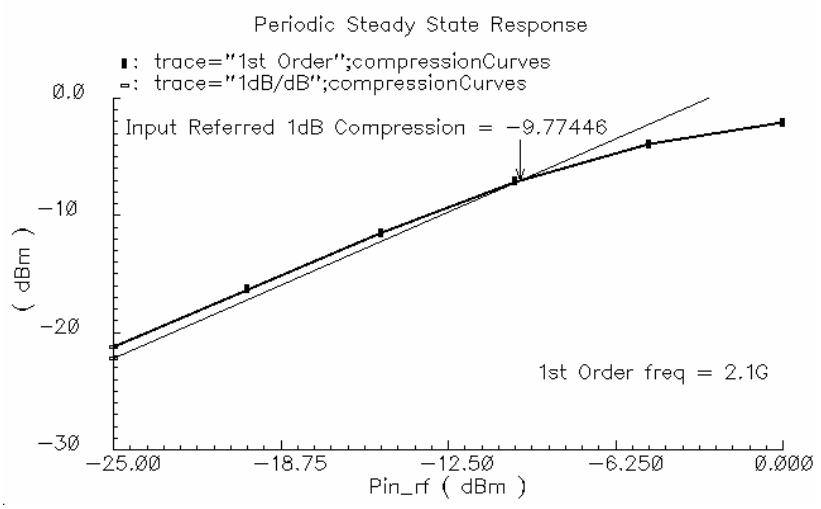


Fig. 24. Offset mixer: 1-dB compression curve (max. gain setting)

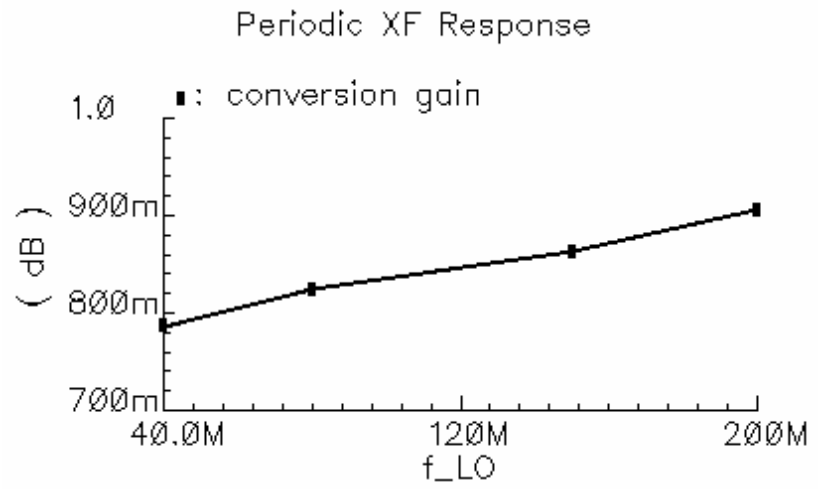


Fig. 25. Offset mixer: max. conversion gain vs. LO frequency (f_{RFout} = 2.1GHz)

As shown in Fig. 25, the mixer conversion gain is flat (Δgain ≈ 0.1dB) for the offset (LO) frequency range of 40-200MHz that can be encountered in practical loopback test cases.

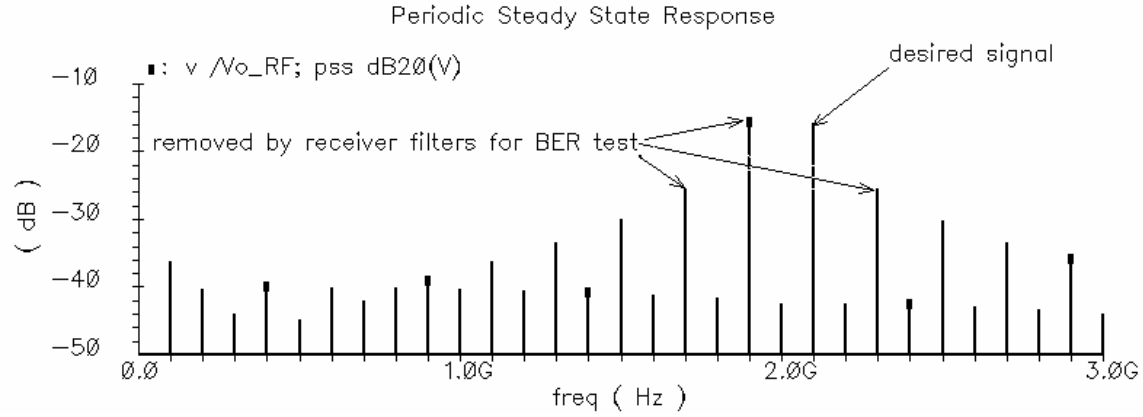


Fig. 26. Offset mixer output voltage spectrum
(f_{RFin}=2GHz, f_{LO}=100MHz, f_{RFout}=2.1GHz)

Fig. 26 gives insights into the spectral characteristics of the mixer output signal. In this example, the RF input signal frequency is 2GHz and the frequency offset between transmitter and receiver is 100MHz. The mixer output spectrum has several up-converted harmonic components at RF frequencies due to the switching with a square wave, for which the mathematical analysis is included in Appendix A. Furthermore, a supplemental derivation of the common-mode gain is provided in Appendix B that shows the rejection property for the spectral component at 2GHz (f_{RFin}) in Fig. 26, which is a common-mode signal at the differential pair in the mixer output stage as evident from the expressions in Appendix A. With the front-end gain characterization approach that involves measurement of the RF power using RMS detectors, the spectral

components at $f_{RFout}+2f_{LO}$ and $f_{RFout}-2f_{LO}$ do not significantly affect the measurement accuracy since both frequencies are within the typical corner frequencies of the on-chip LNA gain. Signal distortion during on-chip RMS measurements is also not critical because proper AC characterization is possible even if the total harmonic distortion is as high as 10% [43].

On the other hand, if the loopback signal is intended for BER testing in the baseband, then the mixing by-products are undesired and must be removed by the filters in the receiver chain. Fortunately, extensive filtering in the receiver path is mandatory in all designs to meet blocking requirements that necessitate the suppression of much stronger interferers at frequencies closer to the wanted signal than the by-products of the offset mixer. For example, a receiver implementation and discussion of the circuit design issues associated with the filtering and amplification steps has been published in [44] for the W-CDMA standard, which requires rejection of blockers by more than 50dB and only 10MHz away from the frequency of the desired signal. In comparison, the offset mixer by-products are only of equal or lesser power than the wanted signal and at least $2\times f_{LO}$ (>80MHz) away from it. Therefore, it can be assumed that they are filtered out by the signal processing operations in the receiver.

III.3. Loopback block consisting of attenuator and offset mixer

System-level simulations were performed to verify the assumptions about the operating conditions at the terminals of the loopback block and to realistically model the loading effects during normal operation. The results presented in III.3.2 were obtained by simulating the complete loopback block integrated with the RF front-end circuits designed by colleagues in a joint effort to realize the on-chip loopback BIT. Gain characterization with power detectors is outside the scope of this work, but has been addressed in [13]-[16]. The focus in the following assessment is to confirm that the loopback output signal in test mode generates sufficient adjustable power at the LNA input for gain and 1-dB compression testing in the presence of coupling losses and pad parasitics, while providing high isolation between transmitter and receiver during normal operation. Measurements of key loopback parameters are provided and compared to the simulation results in III.3.3.

III.3.1. Prototype chip with RF front-end circuits and loopback test option

The block diagram of the proof-of-concept system is repeated in Fig. 27, in which DC bias, control, and RMS detector DC output voltages are omitted to emphasize the AC signal paths. The on-chip routing and pins allow the front-end to be interfaced with external signal generators and measurement equipment to characterize the transmitter and receiver sides separately during normal operation. In test mode, the equipment at the PA output and LNA input can be removed so that the loopback is utilized to route the signal between transmitter and receiver sections. To compare the results from the two

operating modes, buffered inter-stage signals and DC outputs of the RMS detectors can be monitored as well as the spectrum at the down-conversion mixer output.

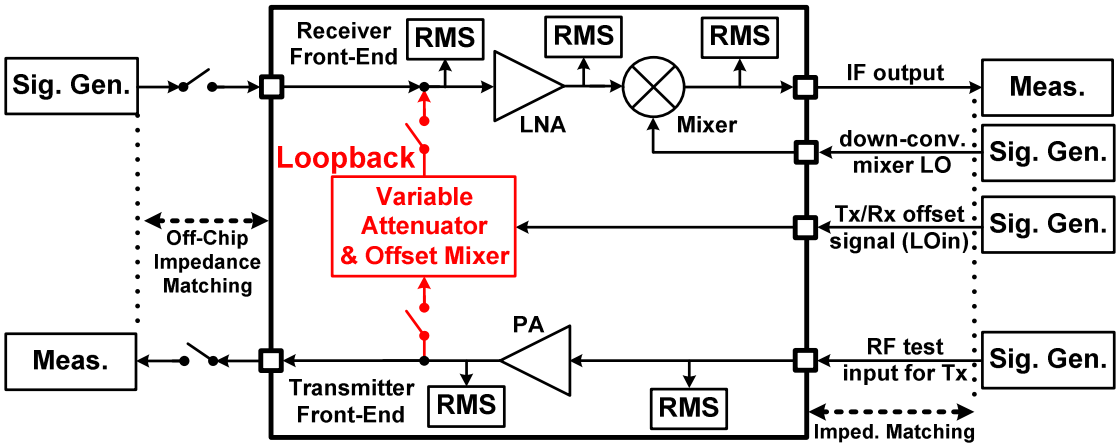


Fig. 27. Test chip block diagram

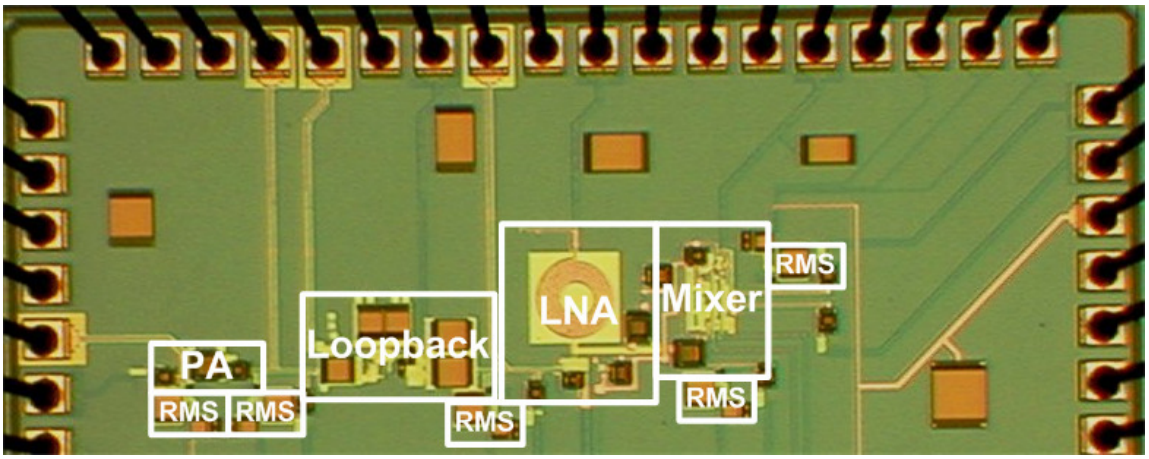


Fig. 28. Test chip micrograph

Fig. 28 shows the part of the test chip that contains the blocks in Fig. 27. The loopback circuit consumes an area of ~0.052mm^2, which is ~37% of the combined PA, LNA, and down-conversion mixer area (~0.14mm^2). But, a fair overhead comparison

should be made with the total area of the integrated transceiver (at least 10-50mm^2) since this BIT enables functional verification of the analog and digital portions. When the area of extra pads for the loopback and RMS detectors is included in the approximation, such a comparison would result in roughly 1-4% area overhead depending on the transceiver implementation.

III.3.2. Post-layout simulation results

The PA and LNA were characterized separately by running Cadence Spectre simulations without any BIT circuits, but including models to account for the other loading effects such as pad and interconnect parasitics from the extracted layout. Appendix C contains a summary of the PA and LNA parameters in comparison with repeated simulations after connecting the RMS detectors and loopback BIT circuits, which were powered down. Only negligible changes occurred in LNA S_{11}/S_{21} (~0.2dB difference), LNA linearity (IIP3/1-dB compression point difference $\leq$ 0.5dB), PA power gain/S_{22} (~0.3dB difference), and PA linearity (IIP3/1-dB compression point difference $\leq$ 0.5 dB). Thus, the results in Appendix C demonstrate that the loading effects of the BIT circuitry do not significantly degrade the performance of the circuits under test when the optimum LNA gate inductance value is selected during the design by taking the parasitic capacitance of the BIT circuits into account.

Table XII. Loopback block simulation results

Parameter (f_{RFin}/f_{RFout} = 2GHz/2.1GHz)	**Setting: Max. Atten.** (P_{in} = 0dBm)	**Setting: Min. Atten.** (P_{in} = 0dBm)
Power Attenuation ($P_{in} - P_{LNA\text{-}Gate}$)	27.3dB	10.9dB
ΔAtten. over: 1.9GHz < f_{RFin} < 2.4GHz	< 2dB	
ΔAtten. over: 40MHz < f_{LO} < 200MHz	< 0.9dB	
Input 1-dB Compression Point	-18.5dBm	-20.0dBm
Gain Compression (with P_{in} = 0dBm)	1.6dB	2.0dB
S_{11} (50Ω, 1.9-2.4GHz)	< -9.4dB	
Noise Figure (SSB)	36.4dB	28.5dB
Incremental Noise Figure	9.1dB	17.6dB
Power at LNA Gate (1-dB $Comp._{[LNA]}$ = -11.4dBm)	9.7mV_{rms} / -27.3dBm	63.4mV_{rms} / -10.9dBm
Output Spot Noise	0.9nV/√Hz	2.8nV/√Hz
Integrated SNR*	77.8dB	84.3dB
Power Consumption	12.2mW	11.8mW
Isolation in Off-State	> 89dB	
Supply Voltages (V_{dd}/V_{ss})	1.2V / 0V	
Area	0.052mm^2	

* With equation (1) and W-CDMA bandwidth of 3.84MHz (discussed on page 23).

Table XII summarizes the simulated specifications of the loopback block embedded into the RF front-end as shown in Fig. 27. Graphs for key parameters are discussed in this section, while the remaining graphs are included in Appendix D for completeness.

With a PA output power of 0dBm, the loopback block operates with ~2dB gain compression as shown by the compression curve in Fig. 29, which is linear enough to allow RMS gain measurements with the detectors used in this project. Within the offset frequency range for typical standards around 2GHz, the change of the gain was ~0.9dB with an LO sweep from 40-200MHz (see Fig. 30), which should be taken into account in case the loopback is integrated into multi-standard transceivers. Similarly, if a multi-standard transceiver with significantly different transmit frequencies is tested, the gain difference should be taken into account, which is approximately 2dB for loopback input frequencies from 1.8GHz to 2.4GHz (Fig. 31). This change is predominantly caused by the capacitive contribution of the mixer's load and the fact that the impedance looking into the input gate of the LNA is frequency-dependent. The gain difference is negligible for testing of a single-standard transceiver with a typical offset frequency change of up to a few megahertz to cover the various channels.

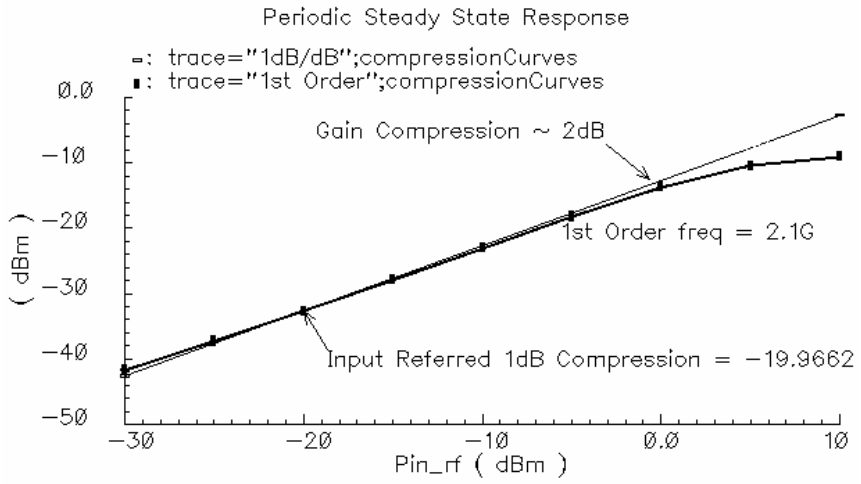


Fig. 29. Loopback gain compression curve (min. atten. setting)

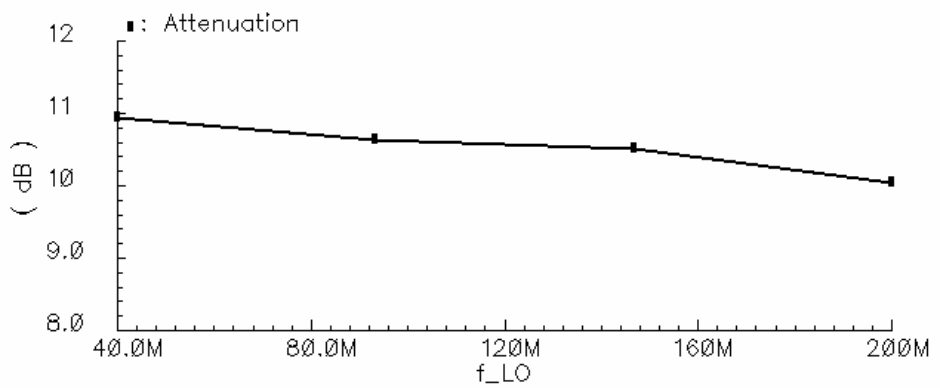


Fig. 30. Loopback min. attenuation vs. LO frequency (f_{RFin} = 2GHz)

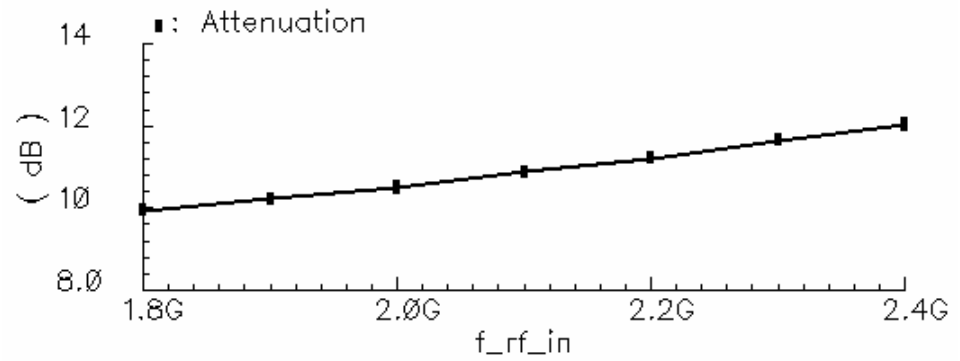


Fig. 31. Loopback min. attenuation vs. input frequency (f_{LO} = 100MHz)

The continuous control of the overall attenuation in the loopback block from 11dB to 27dB is visualized in Fig. 32 - Fig. 34. In these figures, the control voltage of the second stage in the offset mixer (see Fig. 19) was swept for each one of the three different settings. With this attenuation range, the power at the gate of the LNA can be adjusted to measure its uncompressed gain 16dB below the 1-dB compression point as well as at the 1-dB compression point.

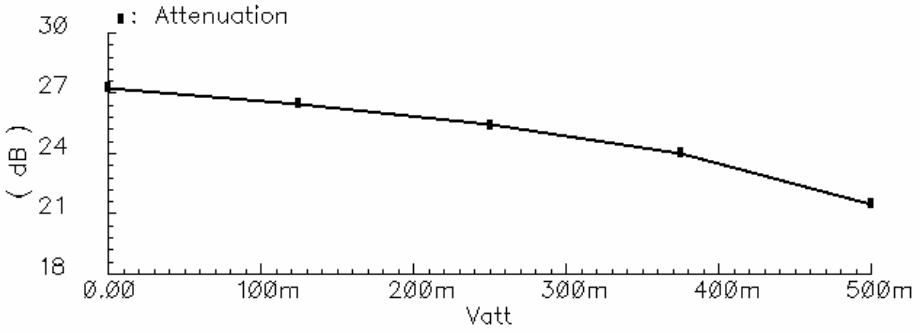


Fig. 32. Loopback attenuation vs. control voltage, $Vatt_{ctrl}$ in Fig. 18 (setting 1) [V_{set2}=V_{set3}=V_{dd}, f_{RFin} = 2GHz, f_{LO} = 100MHz]

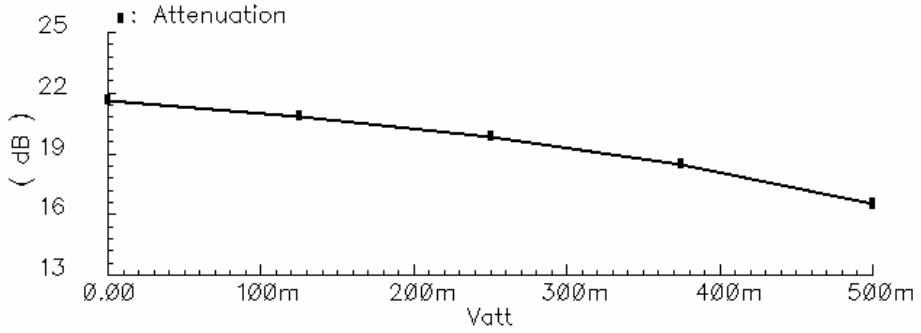


Fig. 33. Loopback attenuation vs. control voltage, $Vatt_{ctrl}$ in Fig. 18 (setting 2) [V_{set2}=V_{dd}, V_{set3}=0V, f_{RFin} = 2GHz, f_{LO} = 100MHz]

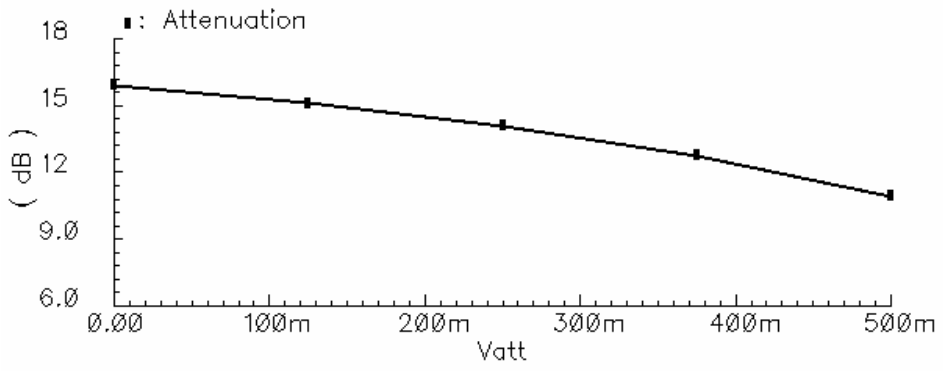


Fig. 34. Loopback attenuation vs. control voltage, $Vatt_{ctrl}$ in Fig. 18 (setting 3) [V_{set2}=V_{set3}=0V, f_{RFin} = 2GHz, f_{LO} = 100MHz]

III.3.3. Measurement results

The characterization of the test chip is still in progress, but preliminary measurements have been taken for the embedded loopback block, which are discussed in this subsection. An 80-pin quad flat no-lead (QFN) package was used to gain access to all 76 bias/RF pads of the system and standalone blocks on the die for initial functionality checks. Since the die size is 2.1mm×2.1mm, the length of the bonding wires between the pads and the QFN-80 package pins is between 4mm to 5mm, resulting in approximately 4-5nH parasitic inductance. In addition, some RF inputs/outputs (I/Os) had to be connected to nearby package pins due to the large number of I/Os, which further degraded high-frequency performance due to coupling. On the printed circuit board (PCB) level, another consequence was that the SMA connectors had to be spaced close to each other for placing them near the chip. With restricted clearance between the connectors and traces on the PCB (Appendix E), the isolation between them was poor to modest (~30-50dB). Steps under consideration as test setup modifications are placement of another die into a package with smaller cavity size, bonding only to selected pads, and reducing the number of connectors on the PCB; since these promise improvements with respect to RF feedthrough, coupling effects, and impedance matching conditions for more accurate measurements of specific blocks/performance parameters.

Table XIII contains a comparison of the measurements with the post-layout simulation results for the key loopback parameters. The functionality, offset frequency range (40-200MHz), and continuous attenuation range (~15dB) could be verified in agreement with the simulation results using this first chip/PCB assembly. However, the

combined attenuation in the cascaded circuits of the loopback block was approximately 15dB lower than in the post-layout simulations due to variations of the load resistances and parasitics capacitances. Besides increasing design margins, the layout can still be optimized to avoid losses, especially by replacing the metal-oxide-semiconductor (MOS) coupling capacitor in the offset mixer (C_{c1} in Fig. 21) by a metal-insulator-metal (MIM) capacitor with significantly less parasitic capacitance (~275fF in this case). A MOS capacitor was selected to save die area, but in retrospect, this choice was not optimal because the parasitic capacitance to the substrate causes signal leakage to ground that is highly dependent on process variations. Using a MIM capacitor would increase the mixer area ~5% with the benefit of more robust post-fabrication performance.

Table XIII. Loopback block: comparison of post-layout and measurement results

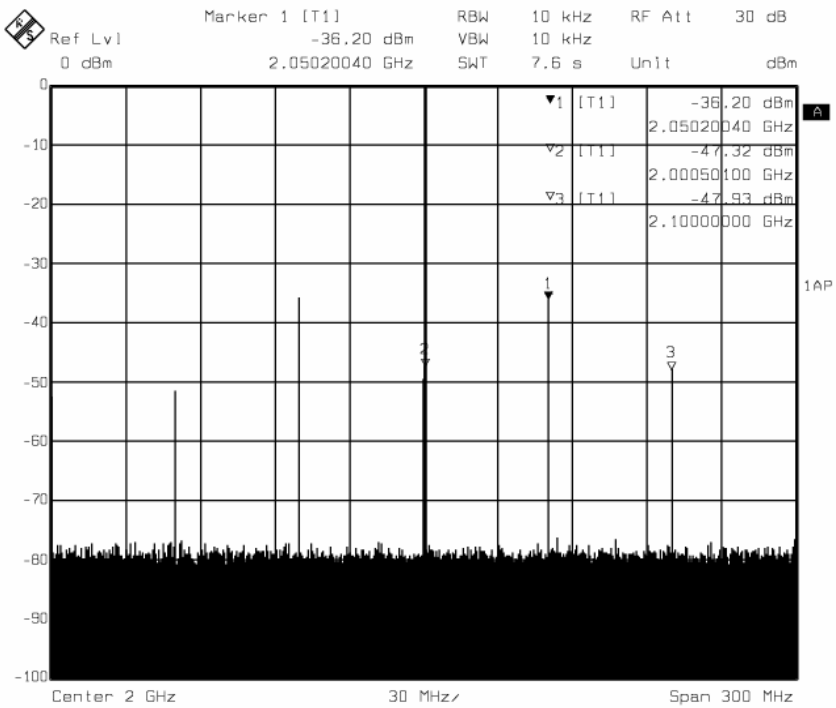
Parameter	**Target**	**Post-Layout Sim.**	**Measured**
Input impedance	50Ω (matched to PA)	50Ω	50Ω on-chip resistor (subject to PVT var.)
Tx/Rx offset frequency range	40-200MHz	40-200MHz	40-200MHz
Attenuation range (continuous)	10-25dB	10.9-27.3dB (f_{RFout} = 2.1GHz)	25.9-41.5dB (f_{RFout} = 2.1GHz)
Operating frequency	< 2.5GHz	< 2.5GHz	< 2.5GHz
Tx/Rx isolation (deactivated)	> 80dB	> 89dB	> 27.4dB*

* Measurement setup does not permit verification of isolation with more certainty.

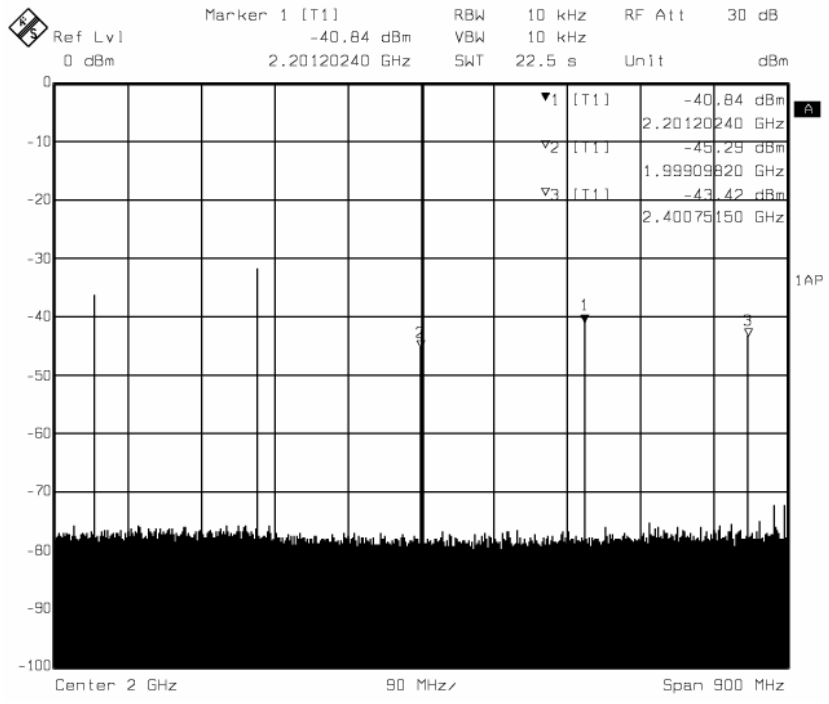
Identical on-chip buffers were used at the inputs and outputs of all blocks to monitor the power levels in this prototype front-end. The results in Table XIII and the

measurements below were de-embedded based on the attenuation of the buffers at the operating frequency as well as 2dB loss associated with the cable from the SMA connector to the spectrum analyzer. From the characterization of an on-chip standalone buffer, the gain was determined to be -7.9dB around 2GHz. Another limitation in the test setup was that the maximum power at the loopback input was limited to -3.5dBm instead of the 0dBm target because of impedance mismatch on the prototype PCB.

Fig. 35 displays the output spectra with a single-tone RF input of -4.9dBm and two different offset frequencies (50MHz, 200MHz). In both cases, the setting for the maximum achievable gain in the offset mixer was used, resulting in a minimum attenuation in the loopback block of 21.3dB (RF_{out} at 2.0GHz) and 25.9dB (RF_{out} at 2.2GHz) after accounting for the losses of the cable (2dB) and output buffer (8dB). The locations of the spectral components at the loopback output agree with the mixer simulations in section III.2.5, but the relative attenuation of the feedthrough at the RF input frequency was only 4.5dB at f_{RFout}=2.2GHz. The feedthrough is still acceptable with respect to the tolerable interference discussed in section III.2.5, but the suppression is less effective compared to the simulations (>20dB).



a)



b)

Fig. 35. Measured loopback output spectrum (RF_{in} = -4.9dBm at 2GHz) (-10dB from buffer/cable losses).
(a) f_{offset} = 50MHz → desired RF_{out} at 2.05GHz
(b) f_{offset} = 200MHz → desired RF_{out} at 2.2GHz

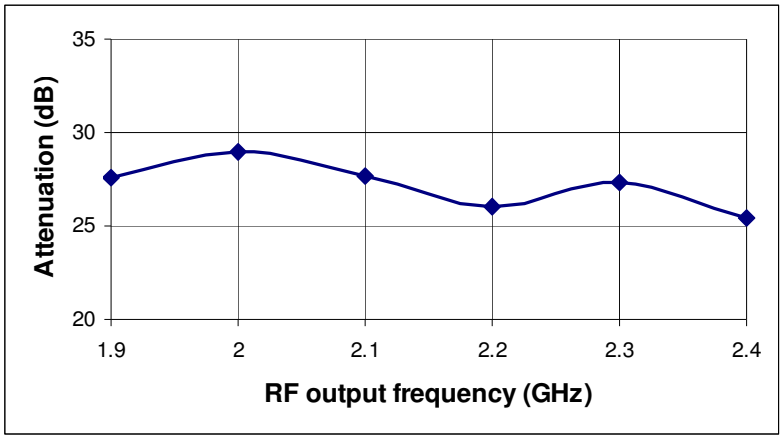


Fig. 36. Loopback attenuation vs. RF output frequency
(P_{in} = -3.5dBm, f_{offset} = 100MHz, min. attenuation setting)

The measured attenuation vs. RF output frequency change (Fig. 36) was ~4dB with ~2dB more variation and an unevenness that was not observed during simulations, since the measurements were impacted by additional parasitics from the bonding wires and PCB. This change in attenuation vs. RF output frequency would be relevant in multi-standard transceivers as addressed in III.3.2.

Table XIV provides an overview of the attenuation settings for built-in testing of the front-end circuits at different power levels (ideally up to the 1-dB compression point). The sensitivity to changes of the load impedance with the switching scheme in the offset mixer core was ~3dB lower than in simulations, which, as the reduced gain, also points to variation of the resistors and parasitic capacitances in the mixer stage. But, with the extended range of the continuous gain control shown in Fig. 37, the overall measured attenuation range was ~15dB, which is comparable to the ~16dB from the post-layout simulations.

Table XIV. Loopback attenuation (measured at f_{RFout}=2.1GHz)

Control Mechanism	Attenuation
Discrete setting 1 (switched resistance value)	25.9dB
Discrete setting 2 (switched resistance value)	28.6dB
Discrete setting 3 (switched resistance value)	30.2dB
Control voltage (load transistor in triode region → continuous mixer gain change)	+ (0dB-11.3dB)
Combined	25.9dB-41.5dB

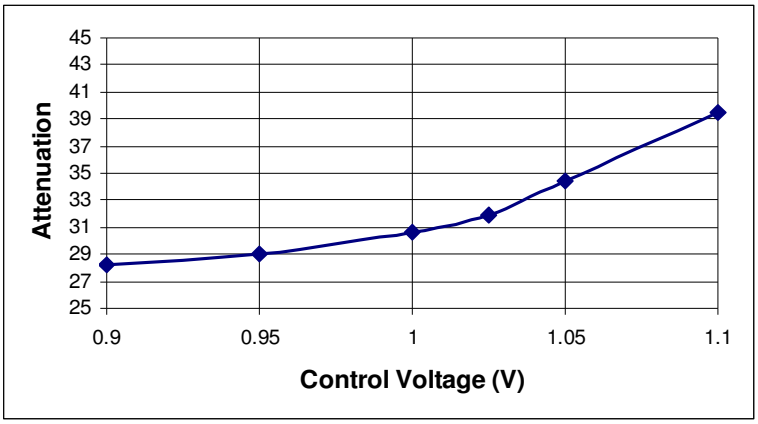


Fig. 37. Continuous attenuation range with the loopback control voltage (Pin=-12.5dBm, f_{RFout}=2.1GHz)

The isolation between transmitter and receiver when the loopback is deactivated could only be assured to be >27.4dB because the on-board RF feedthrough interfered with the measurement. Furthermore, the on-chip buffers in parallel with the RMS detectors at the loopback input and output (Fig. 27) share bias voltages lines, resulting in leakage through the buffer parasitics in addition to the expected on-chip coupling

through the substrate and supply voltage lines. Thus, the present measurement conditions do not permit to determine the amount of leakage through the loopback block itself, and it can only be said that this leakage is less than the measurement in Fig. 38, which represents the cumulative on- and off-chip feedthrough.

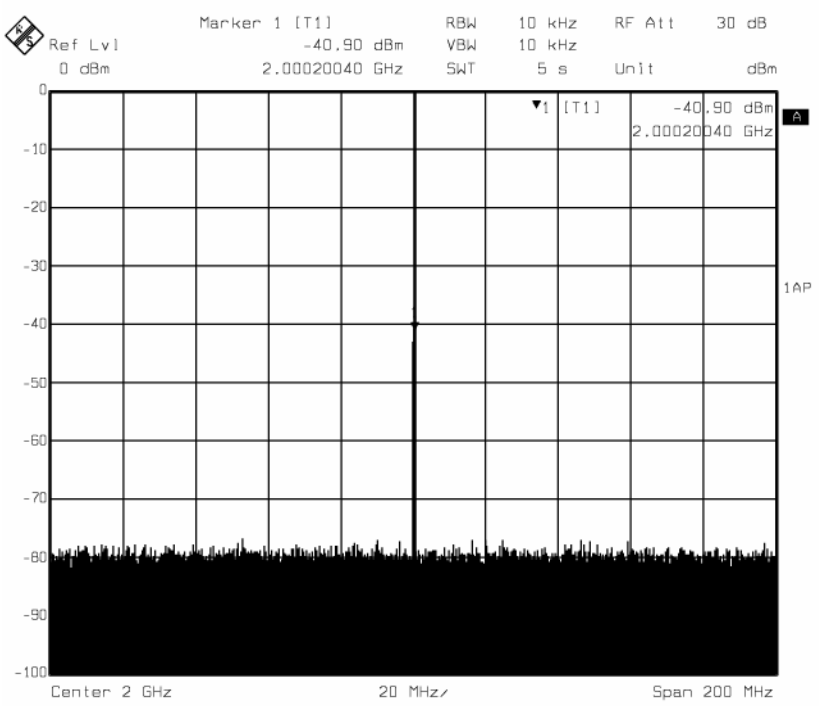


Fig. 38. Input-output isolation when the loopback block is deactivated (P_{in} = -3.5dBm at 2GHz, P_{out} = -40.9dBm + $2dB_{cable\_loss}$ + $8dB_{buffer\_loss}$ = -30.9dBm → isolation = 27.4dB)

III.3.4. Discussion

Each circuit in the proposed loopback block was designed with a focus on the unique requirements of the application, which was done by different design optimization trade-offs in comparison to similar circuits at their conventional locations in the RF transmit/receive chain. For instance, the continuous attenuation control was not implemented in dB-linear fashion as high performance variable attenuators ([31]-[33]) in Table V on page 26. Instead, a fixed resistive attenuator was used for broadband input impedance matching, and the attenuation control was realized in the mixer without the need for a feedback control scheme to keep the input impedance of the attenuator constant. This alternative allowed a reduction of the attenuator complexity, die area, and power, but with less linear attenuation (in dB) vs. control voltage characteristics (Fig. 32 - Fig. 34). Nevertheless, it provides the necessary range for 1-dB compression testing and more flexibility than switching between different resistive attenuators with discrete steps (as in [29], [34]) because continuous attenuation control is accomplished.

It was described in sections III.2.1 and III.2.2 how the unusual operating conditions of the offset mixer influenced the conception of the presented topology. A major difficulty in the loopback application is to achieve an acceptable conversion gain because the mixer has to drive the low-impedance node at the LNA gate, which contains a real component created by the inductor-degenerated common-source LNA as well as capacitive loading from pad parasitics and the LNA's gate-source capacitance. Since the mixer input and output are at RF frequencies, critical node resistances must be kept at a minimum to avoid low gain corner frequencies due to RC time constants.

In comparison to typical up-/down-conversion mixers (Table IX on page 40) that have one low-frequency input or output, it is more challenging to optimize the offset mixer for good linearity and gain since the input and output signals both are at high frequencies. For this reason, conversion gain was sacrificed in the design to achieve the required linearity for processing the relatively high-power signals in the loopback. As a result, the simulated maximum unloaded offset mixer conversion gain of 0.9dB is approximately 10dB lower compared to other active mixers [37], [39]-[41]; and its worst-case linearity (IIP3 = 0.1dBm) can be considered slightly better than that of average mixers (IIP3 ranges from -10.7dBm to 6dBm in references [37], [39]-[41]). In post-layout simulations, the active mixer topology still allowed to generate -10.9dBm at the LNA gate for the loopback testing approach with sufficient output power to verify the 1-dB compression point, which is more than the simulated -20dBm maximum output power level of the passive offset mixer in [36]. However, the initial measurement results showed that more design margin should be added for the mixer gain as discussed in the previous section in order to enable 1-dB compression point testing of the LNA.

IV. RF BIT WITH ON-CHIP CURRENT INJECTION*

IV.1. Background and Motivation

In the conventional on-chip characterization of RF front-end circuits, the test input signal is typically supplied by a voltage source and the block-level gain is measured by on-chip power detectors at the input and output of the circuit under test, which is adequate for on-chip voltage gain measurements. However, voltage-mode testing of impedance-matched RF circuits involves some previously unaddressed concerns that are discussed in [45], in which a current injection based built-in test (BIT) technique for impedance-matched RF front-ends is proposed. The main goal of the current injection approach is to extend the BIT's fault detection capability to off-chip components in the matching network, which would have the benefit that the BIT can be utilized at final package or board-level test stages. This BIT entails verification of the gain (S_{21}) under the influence of parasitic effects and input impedance matching conditions. In this section, the current injection methodology for RF front-end testing will be introduced briefly, followed by an explanation of a test current generation circuit for this purpose. Basic simulation results from a current injection BIT case study for a low-noise amplifier (LNA) will also be presented to demonstrate the concept, but the emphasis in this thesis is on the current generator topology. A more detailed analysis of the voltage-

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mode drawbacks, the current injection methodology, and simulation results to verify the theory for testing impedance-matched RF front-ends can be found in [45].

IV.2. BIT extension to components of the impedance matching network

Accurate performance prediction during final test (package or board-level) requires that the receiver front-end is properly terminated by the off-chip matching network. A block diagram of such a scenario is shown in Fig. 39 for the typical (voltage-mode) on-chip testing technique. Power detectors are used to monitor the power level at the LNA's input and output for the gain measurement. In the voltage-mode BIT of the LNA, the test voltage signal (v_{ts}) is applied at the gate of the input transistor, which leads to loading of the input matching network by the low output impedance (R_{ts}) of the on-chip source. As a result, the off-chip matching network is partially bypassed due to the RF voltage source impedance. Hence, application of the ordinary voltage-mode BIT is limited to on-chip gain measurements.

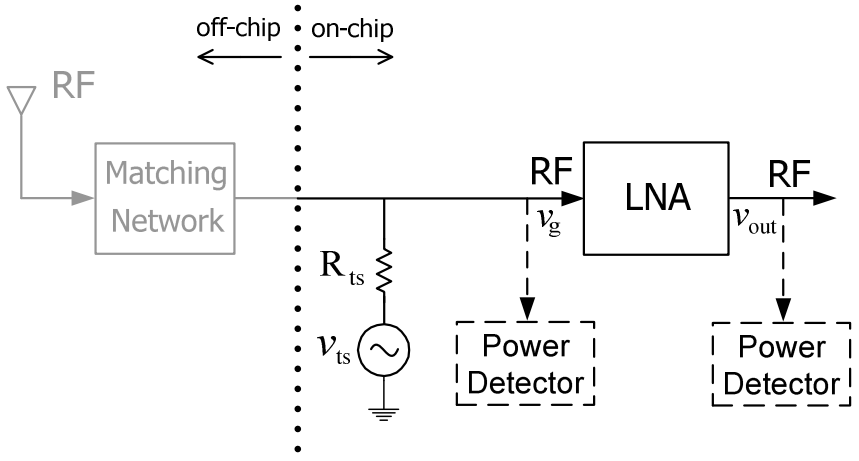

Fig. 39. Conventional voltage-mode on-chip testing scheme

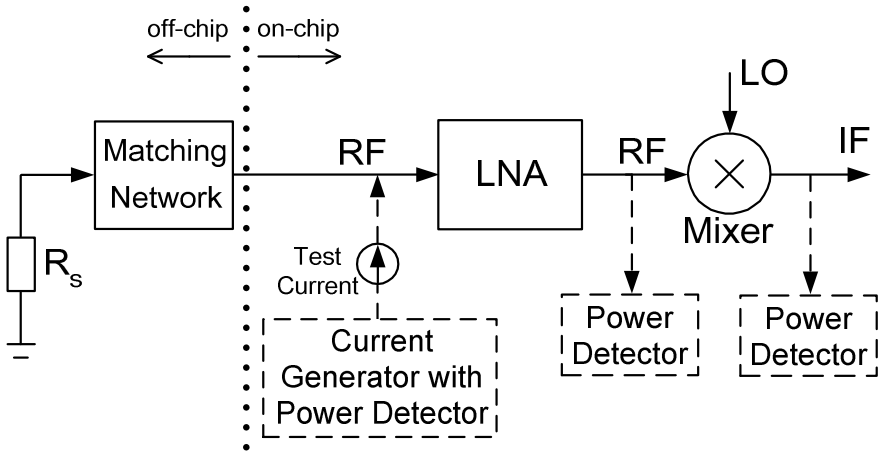

Fig. 40. Current injection testing scheme
(© 2007 IEEE)

Fig. 40 displays the proposed current injection technique. The LNA is terminated by the external matching network and source resistance (R_s) that are encountered under normal operation, but they could also be emulated as part of the test interface hardware. An on-chip current generation circuit with high output impedance is used to inject the test signal at the LNA input. This has the advantage that the impact on the resonance circuit at the input is negligible. As displayed in Fig. 40, power detectors can be placed along the RF signal path for gain measurements of subsequent blocks on the chip with the conventional voltage mode approach.

Fig. 41 visualizes the Thévenin-Norton transformation to obtain a current source from a voltage source with a series resistor (R_s) and an inductor (L_g) at the input of the circuit. The transformation is independent of the elements to the right of point "x" in the figure, which usually include the circuit under test (CUT), electrostatic discharge (ESD) circuitry, and parasitic elements due to the input/output (I/O) bonding pad. The

equivalent Thévenin voltage (v_{in}) and the voltage gain (G) can be expressed in terms of the output voltage and the input current source as follows:

$$v_{in} = i_{test} \times (R_s + j\omega L_g) \tag{10}$$

$$G = \frac{v_{out}}{v_{in}} = \left(\frac{1}{R_s + j\omega L_g}\right)\left(\frac{v_{out}}{i_{test}}\right) \tag{11}$$

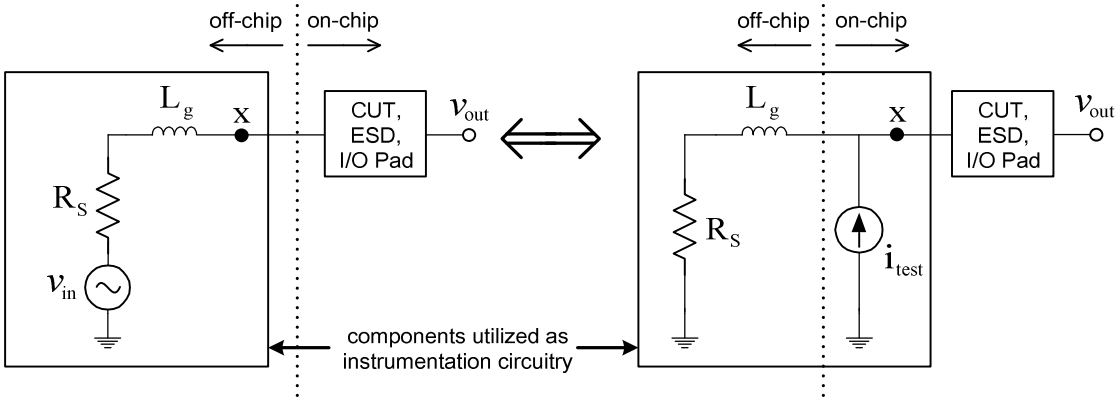

Fig. 41. Equivalence of voltage and current domain test input signals
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Thus, to fully characterize the circuit, it is necessary to measure the test current and the output voltage for prediction of the voltage gain with equation (11). Since this is a relative gain measurement, the equality of the voltage and current source magnitudes in (10) does not have to be determined numerically. Other factors are used to select the appropriate test current magnitude, which are discussed in section IV.3.2. In the following derivation it will be exemplified how the voltage gain of the LNA can be estimated based on (11). ESD circuitry and I/O bonding pads are not included in the mathematical expressions for simplicity, but it has been shown in [45] that the final

results are valid in the general case if the appropriate models for parasitics are incorporated.

IV.2.1. Example test scenario: impedance-matched low-noise amplifier

Most RF front-ends have some off-chip components as part of the input matching network to fulfill the low noise requirement and to absorb the impedance of the package bonding wire. Thus, it is necessary to preserve the impedance matching conditions for final test (in-package or board-level). The inductor-degenerated common-source LNA shown in Fig. 42a has an inductor at the source, which allows the generation of a real impedance at the gate of transistor M_1 to achieve impedance matching that provides significant noise figure (NF) improvements [46], [47]. If the resistive losses in the signal path, gate resistance, and the parasitic capacitances except gate-source capacitance are ignored, the input impedance Z_{in} simplifies to an equivalent series of an inductor, capacitor, and resistor as follows:

$$Z_{in}(s) = s(L_s + L_g) + \frac{1}{sC_{gs}} + g_{m1}\frac{L_s}{C_{gs}} \tag{12}$$

where g_{m1} is the transconductance of M_1 and $s=j\omega$. The input impedance Z_{in} is usually matched to $R_s=50\Omega$ at the operating frequency (ω_o). If the parasitic capacitances of the cascode transistor M_2 are ignored, the overall voltage gain, G, of the LNA can be expressed as

$$G = \frac{v_{out}}{v_{in}} = -\frac{\frac{g_{m1}Z_o}{sC_{gs}}}{R_s + g_{m1}\frac{L_s}{C_{gs}} + s(L_g + L_s) + \frac{1}{sC_{gs}}} \tag{13}$$

where Z_o is the output impedance at the drain of M_2. Under impedance-matched conditions at ω_o, the LNA is designed such that the following conditions are satisfied: $\omega_o(L_g+L_s) = 1/(\omega_o C_{gs})$ and $R_s = g_{m1}L_s/C_{gs}$.

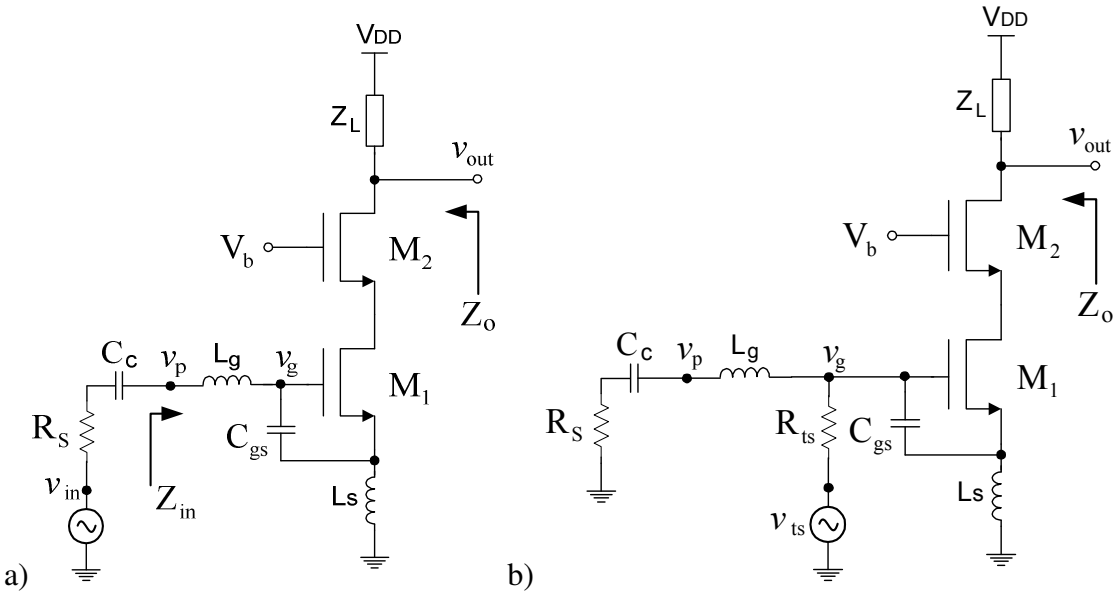

Fig. 42. LNA testing: (a) normal operation (b) voltage-mode on-chip testing (R_{ts} is the output impedance of the on-chip voltage source v_{ts})

IV.2.2. Voltage-mode testing

If the voltage-mode technique is applied to the LNA by grounding the input (v_{in}) in Fig. 42a and inserting an on-chip test voltage source (v_{ts}) at the gate node (v_g), the gain (G_{test}) from the on-chip voltage source to v_{out} in test-mode (Fig. 42b) is given by [45]:

$$G_{test} = -\frac{\frac{g_{m1}Z_o}{sC_{gs}}}{\left(1+\frac{R_{ts}}{R_s+sL_g}\right)\left(g_{m1}\frac{L_s}{C_{gs}}+sL_s+\frac{1}{sC_{gs}}\right)+R_{ts}} \tag{14}$$

where R_{ts} is the output impedance of the on-chip test voltage source, which is usually around 50Ω. The magnitude of equation (14) is significantly different than the voltage gain in (13), which complicates the assessment of the LNA performance. Unfortunately, the low output impedance of the on-chip signal generator (R_{ts}) has unfavorable effects on the input matching properties that are crucial for the proper operation of the RF front-end. The impedance matching is a strong function of the carefully-designed resonant circuit at the gate of the LNA, but the loading effect of the low source impedance alters the equivalent impedance at the input gate node when the circuit is under test, making this method prone to matching errors.

IV.2.3. Current-mode testing: proposed approach

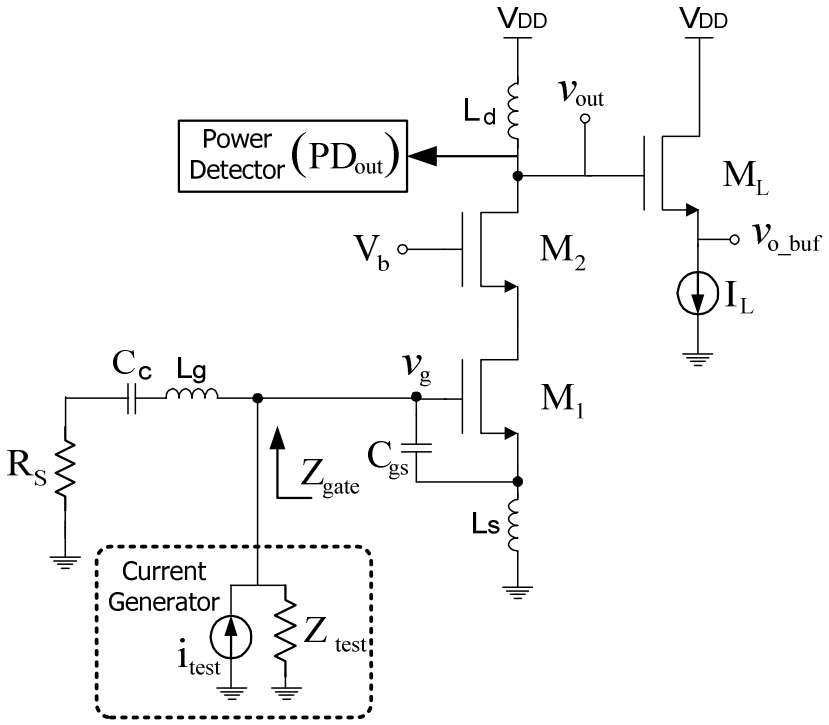

Fig. 43. Current injection BIT configuration
(Z_{test} is the current generator's output impedance), (© 2007 IEEE)

For enhanced LNA characterization, it is desirable that the test source does not significantly load the impedance matching network, which can be achieved with the current injection testing scheme in Fig. 43. In this BIT setup, an on-chip current generator is placed at the input gate of the LNA, and a non-intrusive power detector is located at the LNA output node under test (v_{out}). These circuits have high terminal impedances, which can be ignored in the analysis because they do not significantly load the nodes under test at the operating frequency. This property has been established for the power detector in [13], [45]; and it will be demonstrated for the current generation circuit in section IV.3.3. Furthermore, the off-chip coupling capacitor C_c is large enough to ignore its low impedance at RF frequencies. The buffer transistor M_L embodies the load of the mixer stage that follows the LNA in a receiver. For the test setup in Fig. 43, the magnitude of the transimpedance gain, Z_M, is found as

$$|Z_M| = \left|\frac{v_{out}}{i_{test}}\right| = \frac{\left(\frac{1}{\omega C_{gs}}\right)\left(\sqrt{R_s^{\,2} + (\omega L_g)^2}\right)\left(g_{m1}|Z_o|\right)}{\sqrt{(R_s + g_{m1}\frac{L_s}{C_{gs}})^2 + (\omega(L_g + L_s) - \frac{1}{\omega C_{gs}})^2}} \tag{15}$$

From (11) and (15) it follows that the voltage gain, ideally given by (13), can be determined with a current input signal by employing the following function:

$$|G| = \left|\frac{v_{out}}{v_{in}}\right| = \frac{|Z_M|}{\sqrt{R_s^{\,2} + (\omega L_g)^2}} \tag{16}$$

According to (16), if $\sqrt{R_s^{\,2} + (\omega L_g)^2}$ is determined by reliable components, then finding $Z_M = v_{out}/i_{test}$ allows the accurate calculation of the LNA's gain even if the input is

not impedance-matched. In the Cadence simulation, the S_{21} of the LNA in Fig. 42a is determined based on the output voltage (v_{out}) and the terminal voltage (v_p) after R_s of the s-parameter port. But the voltage gain, |G|, and transimpedance gain, $|Z_M|$, in (16) are based on the input voltage (v_{in}) before R_s. Since the input is matched to 50Ω, the terminal voltage is attenuated by half (-6dB) relative to the source voltage within the port, which requires adding 6dB to account for the reference point difference in (16):

$$S_{21,dB} = 20\log(|Z_M|) - 10\log(R_s^2 + (\omega L_g)^2) + 6 \tag{17}$$

The control over the external components R_s and L_g is typically good enough because they are part of the well-controlled off-chip matching network in a board-level test scenario. Components that are implemented on the chip can also be checked during wafer or in-package test without L_g by making a minor modification of the current injection method as explained in [45] or by mounting L_g as reliable discrete component on the tester load board. In general, the accuracy of (17) relies predominantly on the precision of the on-chip Z_M measurement.

IV.3. Test current signal generation circuit

RF voltage test input signals can be produced on-chip using voltage-controlled oscillators already present in integrated transceivers. An alternative voltage signal source would be the loopback configuration presented in sections II and III. In the following discussion, it is assumed that a RF voltage signal is available on-chip, which still requires the generation and measurement of the test current.

IV.3.1. Proposed topology and design considerations

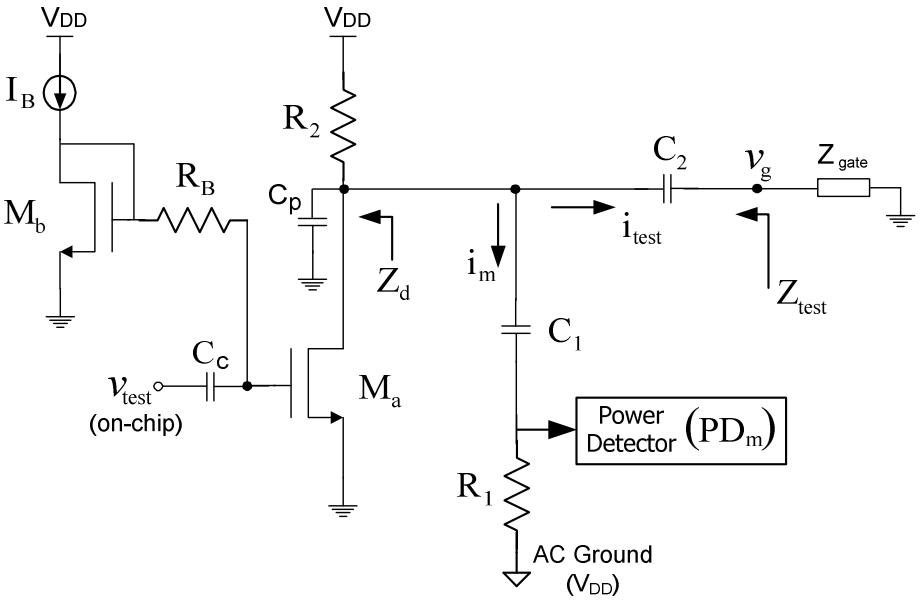

Fig. 44. RF test current generator
(© 2007 IEEE)

Circuit description

The RF test current generator schematic is shown in Fig. 44. Transistor M_a in this circuit performs the conversion from a voltage to a current signal. The resulting current

flows through the load components, leading to current components flowing through R_2 and the parasitic capacitance C_p, as well as i_m and i_{test}. The linearity of the current is not a critical issue; it can be shown that proper AC characterization is possible even if the total harmonic distortion is as high as 10% [43]. The current of interest is i_{test}, which must be measured for proper characterization of the circuit under test. For that purpose, a current divider consisting of C_1, R_1, C_2, and Z_{gate} is used to generate the auxiliary current i_m. Z_{test} in Fig. 44 is the equivalent output impedance of the current generator expressed in equation (20) and Z_{gate} is the impedance looking into the gate node of the LNA, which is also pointed out in Fig. 43. Contrary to the low output impedance requirement for voltage sources, Z_{test} of the current generator can be designed sufficiently large to avoid loading effects as discussed later in this section. Thus, an important design consideration that is needed to test the LNA without drastically affecting its input impedance matching network is to maintain $Z_{test} >> Z_{gate}$. Under this condition, the ratio of the measured current (i_m) and the test current (i_{test}) relies predominantly on the matching ratio of the capacitors C_1 and C_2 ($m=C_1/C_2$), having the advantage of robustness to process variations. The measured current and test current are related according to:

$$\frac{i_m}{i_{test}} = \frac{Z_{gate} + \frac{1}{j\omega C_2}}{R_1 + \frac{1}{j\omega C_1}} = m \times \left(\frac{Z_{gate} + \frac{1}{j\omega C_2}}{mR_1 + \frac{1}{j\omega C_2}} \right) \tag{18}$$

The above ratio of the two currents depends mainly on the small-valued capacitors C_1 and C_2 in the two branches because the impedances of C_1 and C_2 are larger than R_1 and Z_{gate} at the operating frequency (Table XV on page 86). The impedance seen at the gate of the LNA (Z_{gate} in Fig. 43) is equal to the equivalent impedance of the resonant circuit

at the operating frequency. In the LNA under test, the magnitude $|Z_{gate}|$ at resonance is approximately 110Ω. If R_1 is chosen to be m times smaller than Z_{gate}, then optimal precision in predicting i_{test} by measuring i_m is obtained with the relation $i_m=m\times i_{test}$. An additional criterion for the selection of R_1 is to match the root-mean-square (RMS) voltage drop across the resistor with the dynamic range of the power detector.

BIT accuracy considerations

According to (18), the magnitude of i_{test} can be accurately predicted by measuring the voltage across R_1, as shown in Fig. 44. When a RMS power detector is used for measurements of i_{test} (through the voltage across R_1) and v_{out} of the LNA, then the measurement error due to the power detectors is cancelled, except for the errors from unavoidable mismatches between the two detectors. These errors, however, do not significantly affect the precision of the characterization. In [13], this differential method was used to achieve less than 5% deviation between the estimated RMS voltages and the theoretical values. From the simulation results in [45], in which the overall gain estimation error was approximately 3.3% with process corner models and temperature variations (-15°C to 65°C), it can be concluded that the magnitude of the test current is not critical because the BIT scheme relies on the test current measurement relative to the LNA output power rather than the absolute values. It is only required for the output current to be large enough to satisfy the linear range of the LNA and RMS detector at resistor R_1. To ensure these conditions, design margin can be added during the selection of the resistor value and test current magnitude, leaving sufficient room for power level changes from process-voltage-temperature variations.

LNA voltage gain estimation

According to (18), the RMS values of the generated test current (i_{test_rms}) and the current through the measurement resistor (i_{m_rms}) in Fig. 44 are related by a factor of m. The differential measurement is conducted with one power detector at the LNA output (PD_{out}) to measure v_{out_rms} and a second one (PD_m) to find v_{m_rms} across resistor R_1 of the current generator. Substituting $i_{m\_rms}=m\times i_{test\_rms}$ into $Z_M=v_{out\_rms}/i_{test\_rms}$ in equation (17) and using $i_{m\_rms}=v_{m\_rms}/R_1$, S_{21} can be predicted as follows:

$$G_I = S_{21,dB} = 20\log\left(mR_1 \times \frac{v_{out\_rms}}{v_{m\_rms}}\right) - 10\log\left(R_s^2 + (\omega L_g)^2\right) + 6 \qquad (19)$$

Alternatively, the RF current through R_1 could be measured using the approach described in [18], in which a sense amplifier and peak detector are utilized together with other processing circuitry in a self-calibration scheme. With any implementation, the main criterion for the selection of parameters i_m and R_1 is the resulting RMS voltage level, which has to fall within the linear range of the detector PD_m.

Required resistance measurement prior to the BIT

Being an on-chip resistor, the absolute value of R_1 falls within typical variations (30%), which may introduce errors in the order of 2.5dB in equation (19). For this reason, the proposed BIT should be preceded by a quick DC measurement of R_1 to determine its accurate value for the gain estimation. In the remainder of the discussion, it is assumed that the value of R_1 has been determined with the automatic test equipment prior to the BIT using a conventional method (e.g. force-current, measure-voltage) with an error low enough to be disregarded. The resistor R_1 could also be connected to a

multiplexed test bus for DC measurements such as quiescent current tests to avoid the cost of an extra pin. Depending on the amount of parasitics that would be introduced by accessing the node at the input of detector PD_m, a replica of R_1 that is matched with layout techniques could be placed on the chip to be measured instead. In such a case, internal mismatches due to process tolerances and temperature gradients between the R_1 used in the BIT and the local replica being measured may not exceed 5%; therefore the error with such an indirect measurement should not exceed 0.4dB.

Avoidance of loading effects

Another relevant parameter is the current generator output impedance (Z_{test} in Fig. 44) connected to the LNA gate at the resonant frequency (ω_o), which is

$$Z_{test} \approx \frac{1}{j\omega_0 C_2} + \left(\left(R_1 + \frac{1}{j\omega_0 C_1}\right) \parallel R_2 \parallel r_{oa} \parallel \frac{1}{j\omega_0 C_p}\right) \tag{20}$$

where r_{oa} is the output resistance of transistor M_a. The small-sized capacitors (C_1, C_2) allow to increase the output impedance ($Z_{test}>10\times Z_{gate}$). This leaves sufficient freedom in the design to optimize M_a and R_2 for the test current magnitude, voltage headroom, and noise performance.

IV.3.2. Component dimensions and layout

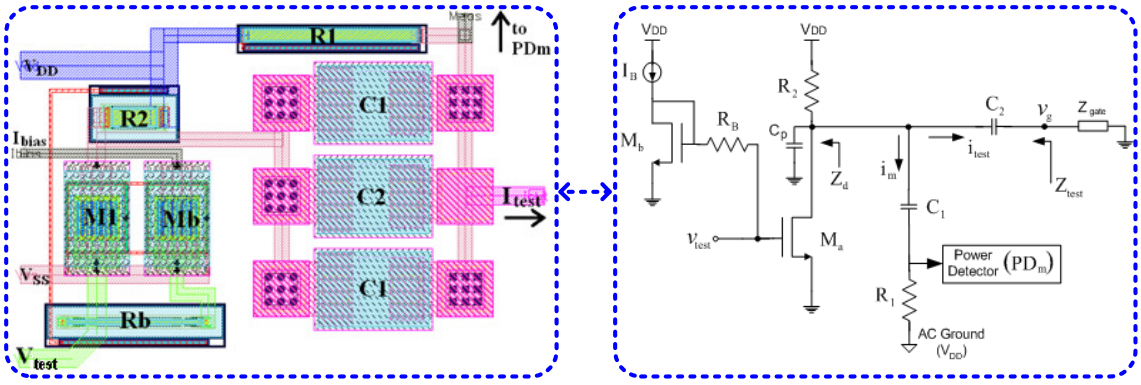

Fig. 45. Current generator layout (40µm × 50µm)

The current generator in Fig. 45 consumes a small layout area of approximately 0.002mm^2 with UMC 0.13µm CMOS technology. Its component sizes are listed in Table XV. An implementation of the current injection BIT method for the LNA (specifications in Appendix F) is shown in Fig. 46, which contains the layout of the LNA with the current generator and two RMS power detectors. The total layout area of LNA and BIT circuitry is 0.16mm^2; and 14.4% of this area is taken up by the two power detectors (each 6.3%), current generator (1.3%), and extra metal routing.

Table XV. Current generator component dimensions

Device	**Dimensions**	**Device**	**Dimensions**
M_a, M_b	W/L = 30.72µm/0.12µm	**I_b**	360µA
R_1	125Ω (W=1.25µm, L=19µm) [poly]	**C_1**	162fF (W=L=2×7.1µm) [metal-insulator-metal Caps.]
R_2	2.32kΩ (W=2µm, L=5µm) [high resistance poly in n-well]	**C_2**	81fF (W=L=7.1µm) [metal-insulator-metal Cap.]
R_B	33kΩ(W=0.5µm, L=15µm) [high resistance poly in n-well]	**Load (Z_{gate})**	~110Ω

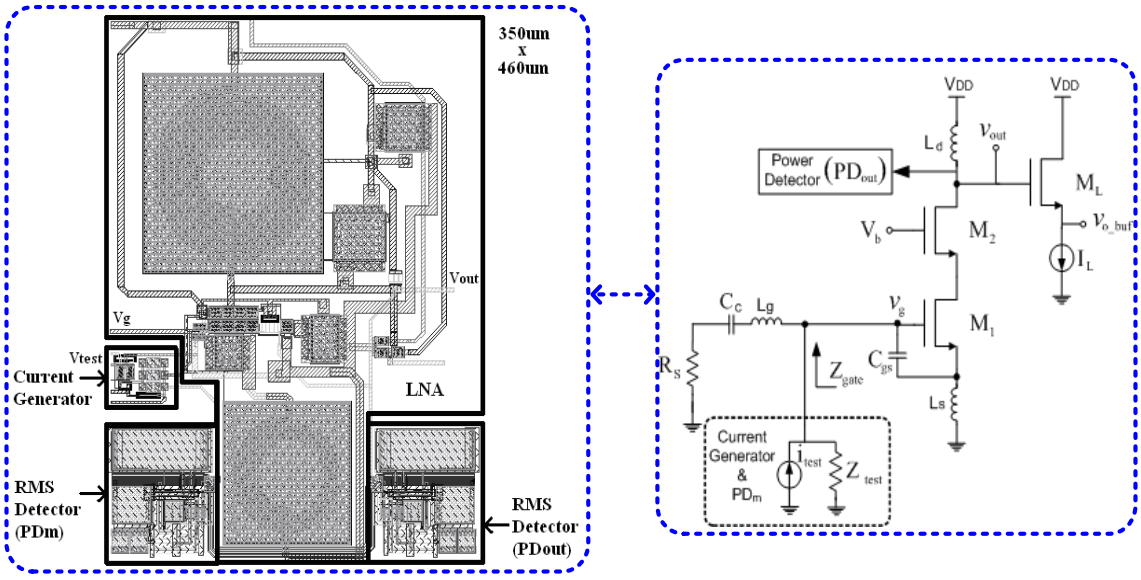

Fig. 46. Layout of LNA BIT with current injection
(© 2007 IEEE)

In general, the design requirements for the test current generator depend on the available voltage source, the typical input power level of the LNA, and the dynamic range of the on-chip power detectors. In this example case, a -15dBm input signal from on-chip loopback or an attenuator fed by a local oscillator is expected and the value of the output current was selected to generate approximately $8mV_{rms}$ at the LNA input gate for compatibility with the linear range of the LNA and RMS detectors. With the choice of R_1, the power level at the LNA gate is ~5dB lower than across R_1 so that the dynamic range of the power detectors PD_{out}-PD_m has to cover 5dB less than the gain from the gate of M_1 to the drain of M_2 in Fig. 46. The current i_m (~$120\mu A_{rms}$) through resistor R_1 creates a voltage drop of $15mV_{rms}$, which corresponds to -23.5dBm to be detected by PD_m. Thus, the current generator design was synchronized with the specific range

(approximately -30dBm to 5dBm) of the RMS detectors, ensuring that the measured power levels fall within this range even with worst-case process and temperature variations.

IV.3.3. Post-layout simulation results

The LNA under test was evaluated with and without the circuitry for the current injection BIT; and the results confirmed that the BIT circuitry only has minor impact on the simulated LNA performance. From the comparison in Appendix F, negligible differences were observed for S_{21}/NF (Δ<0.1dB) and IIP3/1dB compression point (Δ<0.5dB) from the Cadence Spectre simulations. But, the parasitic capacitance of the BIT circuits must be taken into account during the simulations to optimize S_{11}, mainly by selecting the appropriate gate inductance (L_g) value. In this case, S_{11} was minimized with the BIT circuitry, resulting in a S_{11} that is 3.65dB better than for the standalone LNA. This optimization is adequate because the current generator remains connected during normal operation even though no test signal is applied.

Standalone current generator

Table XVI gives an overview of the post-layout simulation results for the standalone current generator with its internal RMS power detector. The corresponding plots are attached in Appendix G. A sinusoidal voltage signal with the expected power of -15dBm was applied at the current generator input for this characterization. The simulations were conducted at the 2.1GHz operating frequency of the LNA and with the anticipated load of $|Z_{gate}| \approx 110\Omega$. With this load impedance, the current generator output

impedance (Z_{test}) was designed to be more than ten times higher than Z_{gate} at the operating frequency of 2.1GHz. This condition holds up to 2.34GHz as demonstrated by the plot in Fig. 47, and the output impedance at 2.4GHz (Z_{test}=1.07kΩ) is still adequately high to avoid any significant loading effects.

Table XVI. Current generator simulation results

Parameter (at 2.1GHz*)	**Value**
g_{test} (i_{test} / v_{test} in Fig. 44)	1.55×10^{-3} I/V
1-dB Compression Point	-10.8dBm
IIP3	-0.9dBm
Spot Noise (output)	2.0×10^{-18} V^2/Hz
Output Impedance, $\|Z_{test}\|$	1.22kΩ
Supply Voltages (V_{dd}/V_{ss})	1.2V / 0V
Power Consumption	0.43mW
Area	0.002mm^2

* See Appendix G for parameter vs. frequency plots.

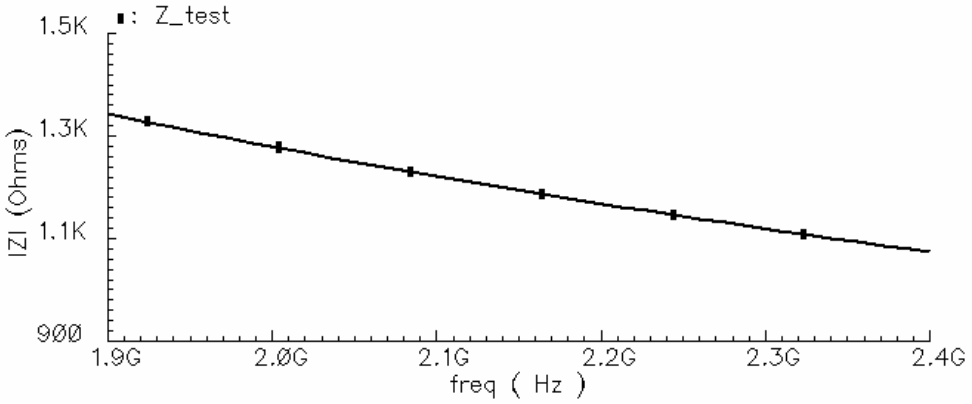

Fig. 47. Current generator output impedance (Z_{test}) vs. frequency

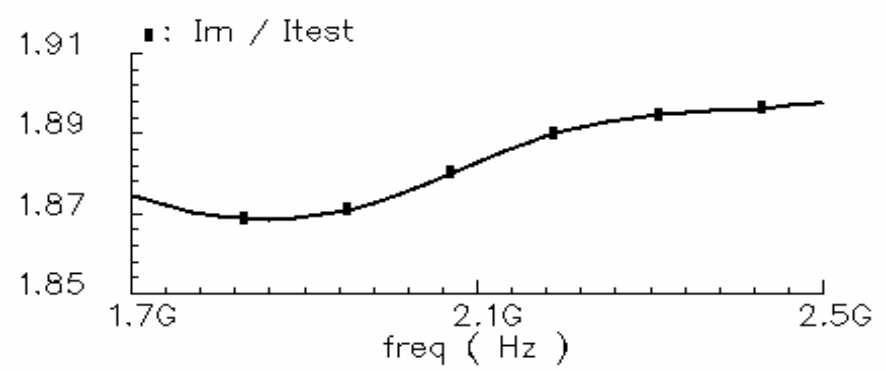

Fig. 48. Ratio of measured current (i_m) and test current (i_{test}) vs. frequency

In the current-mode BIT, the accuracy of the characterization is further affected by the ratio i_m/i_{test}, which is illustrated by the i_m/i_{test} vs. frequency plot in Fig. 48. Ideally, the ratio of i_m and i_{test} is 2 in this design, but it changed from 1.87 to 1.90 over the 1.7-2.5GHz frequency range. The fact that the deviation of the ratio was within 7% of the ideal value and varied only +/-1% over the frequency range can be credited to the accuracy of the matched capacitors used in the current divider. In addition to being minimally affected by process variations, the ratio of the capacitor impedances in the divider remains relatively constant over frequency.

With approximately $8mV_{RMS}$ signal at the gate of the LNA and spot noise around 2×10^{-18} V^2/Hz at 2.1GHz, the SNR is approximately 135dB–10×log(BW), where BW is the channel bandwidth defined by the targeted communication standard. Sufficient room exists for attenuation of the current generator input signal to generate voltages down to several micro-volts at the LNA gate if testing at lower power levels is desired.

LNA BIT with current injection

The current generator was embedded into the LNA layout together with the two power detectors as displayed in Fig. 46. Comprehensive simulations of the RLC extracted layout were used to assess the current injection BIT technique. In [45], several practical concerns related this BIT configuration are covered with more depth, which include the modeling and effects of process variations (device corner models for all components), temperature (-15°C to 65°C), tolerance to ±5% gate inductance (L_g) variation, and defect capacitance at the gate. Table XVII summarizes the overall gain estimation error for the current-mode BIT using the current generator.

Table XVII. LNA S_{21} estimation error with current injection at 2.1GHz

Model Type / Temperature	**Gain (S_{21}) Estimation Error**		
	G_I (S_{21} estimation with matching network)	**RMS Detectors**	**Total**
Typical / 27°C	0.16dB+0.1dB*	0.28dB	0.54dB (2.26%)
Slow / 27°C	0.15dB+0.1dB*	0.48dB	0.73dB (3.06%)
Fast / 27°C	0.15dB +0.1dB*	0.39dB	0.64dB (2.68%)
Typical / -15°C	0.25dB+0.1dB*	0.31dB	0.66dB (2.76%)
Typical / 65°C	0.04dB+0.1dB*	0.39dB	0.53dB (2.22 %)

* 0.1dB added to account for mismatch of C_1/C_2 due to PVT variations.

The testing methodology based on equation (19) was applied to estimate G_I, which is the S_{21} gain of the LNA terminated by its input impedance matching network. A correction factor was derived in [45] for the voltage-mode approach to estimate S_{21} when impedance-matching is guaranteed and the circuit under test is fault free:

$$\left|G_v\right| = S_{21,dB} = 20\log\left(\frac{v_{out\_rms}}{v_{g\_rms}} \times \frac{\sqrt{R_s^2 - (\omega \times L_g)^2}}{2R_s}\right) + 6dB \tag{21}$$

where v_{g_rms} and v_{out_rms} are the RMS voltages at the LNA gate (v_g) and output (v_{out}) in Fig. 42a, respectively, and R_s/L_g are the external resistor/inductor according to the same figure.

A comparison between S_{21} of the LNA and the estimated gains is plotted in Fig. 49. From this figure, it can be observed that the current-mode testing technique is able to predict S_{21} over a wide frequency range. This is because the matching network and therefore the circuit performance are not significantly affected during characterization. Since the voltage-mode prediction with equation (21) is based on the assumption that the circuit is operating at resonance, the estimation error has a strong frequency-dependence.

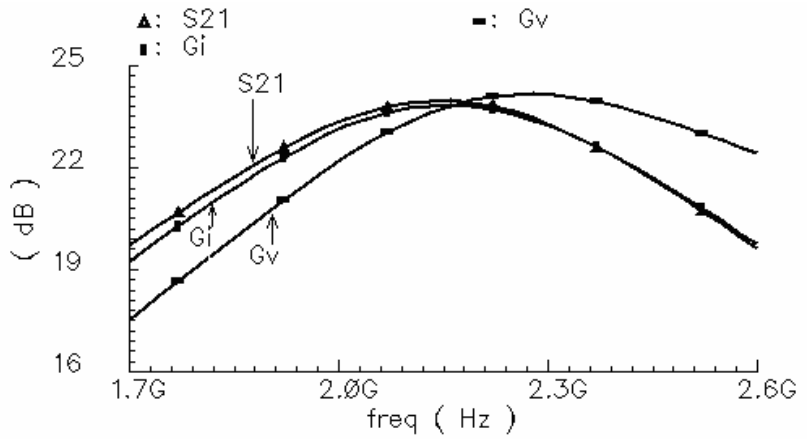

Fig. 49. Current-mode (G_I) and voltage-mode (G_V) estimation of S_{21} [G_I: equation (19), G_V: equation (21)]; (© 2007 IEEE)

With current injection, the frequency-dependent error was approximately 0.5dB even 400MHz away from the resonant frequency. Current injection characterization error is mainly caused by high-frequency parasitic effects and by the load impedance

change at the output of the current generator when the LNA input matching circuit is not at resonance. Both of these adverse effects result in a small frequency-dependency of the ratio between the measured current (i_m) and the actual test current (i_{test}) in Fig. 48.

Additional benefits of the current-mode BIT technique are that it can detect variations of components in the external matching network and it does not require impedance-matched conditions for the gain estimation as the voltage-mode extrapolation with equation (21). In a faulty device, unexpected leakage paths to ground could exist due to fabrication defects. This leakage was introduced during the simulations by connecting a grounded capacitor (C_{leak}) at node v_g in Fig. 43. Furthermore, simulation models for the electrostatic discharge (ESD) protection diodes were also included at that node. Fig. 50 shows the plots of S_{21} and the estimated gains at 2.1GHz from simulations with a sweep of the leakage capacitor value. S_{21} degradation from 23.9dB to 12.5dB was tracked correctly by the current-mode estimation (G_I) with a maximum error of 0.45dB, while the voltage-mode approximation had errors up to 10dB.

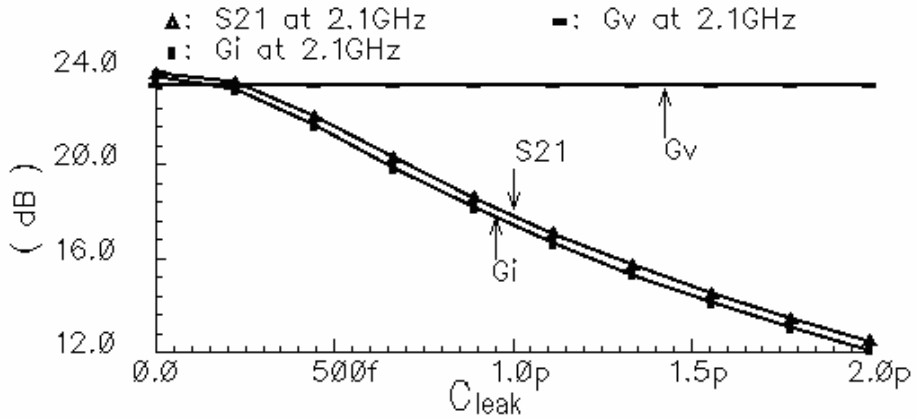

Fig. 50. S_{21} estimation with ESD protection diodes and leakage due to defects [G_I: current-mode with equ. (19), G_V: voltage-mode with equ. (21)]; (© 2007 IEEE)

V. SUMMARY AND CONCLUSIONS

V.1. On-chip loopback test method for integrated transceivers

The objective in this work was to develop an on-chip loopback block with the capability to attenuate and frequency shift the test signal between the transmitter and receiver sections of integrated transceivers operating in the 1.9-2.4GHz range. Besides the requirements for loopback testing, the output power level of the circuit should meet the variability that allows block-level gain and 1-dB compression point characterization in the RF front-end for improved fault coverage. System-level evidence regarding the feasibility of functional verification with the loopback method has been provided in related research through simulations and implementations with discrete components. As a next step towards enabling more efficient production testing of transceivers with the loopback approach, the aim of the research described in this thesis was to develop a circuit-level solution in response to the unique constraints imposed by the combination of loopback and the characterization of RF front-end circuits with on-chip power detectors.

A loopback block was proposed that consists of an attenuator, offset mixer, switches, and an input buffer for the offset signal. Its single-ended RF input is impedance-matched to include the power/pre-power amplifier (PA) of the transmitter in the test loop, and the output can be provided in single-ended or differential form to the low-noise amplifier (LNA). To cover the frequency offset of popular standards in the 1.9-2.4GHz range, the 40-200MHz offset signal can be supplied by an on-chip source or external equipment as sinusoid or square wave. Continuous attenuation control from

11dB to 27dB was achieved in post-layout simulations and from 26dB to 41dB in measurements due to on-chip losses and process variations. Starting points to eliminate this post-fabrication deficiency would be leaving more design margin and replacing a lossy MOS capacitor with a MIM capacitor in the layout. The loopback block has been integrated in a generalized RF front-end test system with power detectors to assess the effects of parasitics and coupling. From comparisons with post-layout simulation results prior to merging the individual circuits, inclusion of the BIT circuitry did not have a significant impact on the PA and LNA performance such that their s-parameters changed less than 0.3dB, linearity parameters less than 0.5dB, and the isolation between transmitter and receiver remained ~90dB when the loopback was switched off. The area overhead of the 0.052mm^2 loopback block is approximately 40% of the combined PA, LNA, and down-conversion mixer area, which would amount to roughly 1-4% for a transceiver with on-chip integration of the analog front-end, mixed-signal, and digital baseband sections.

It can be observed from the simulation and measurement results that the change of the attenuation is insignificant for the testing of single-standard transceivers with a fixed transmit frequency and a typical offset frequency change of up to a few megahertz to cover the various channels. On the other hand, in case a multi-standard transceiver is under test, it is advisable to take into account that the loopback attenuation changes with frequency from 1.9GHz to 2.4GHz (simulated: ~2dB, measured: ~4dB).

V.2. RF front-end testing with current injection

Block-level measurements with the voltage-mode approach and power detectors fit well when the test application requires on-chip voltage gain data such as during on-wafer test. Alternatively, current injection enables to detect faults associated with package parasitics or off-chip components of the input matching network at the RF receiver front-end in addition to on-chip gain verification. As discussed in section IV, this feature also makes the current injection method suitable for final package or board-level testing of integrated transceivers. The two main reasons of the aforementioned benefit are:

- Current-mode testing is based on a Thévenin-Norton transformation, which allows an accurate gain measurement without any restrictions on the circuitry under test.
- High output impedance of the current generator circumvents loading effects at the node under test ($Z_{current\text{-}generator\text{-}out} > 10 \times Z_{node}$).

In this thesis work, both of the above properties have been confirmed theoretically and by the simulation results for a current generator design in UMC 0.13μm CMOS technology. The proposed current generation circuit exhibits a high output impedance (>1kΩ up to 2.4GHz), small size (0.002mm^2 → 1.3% of LNA-BIT area), and constant ratio of the test/measurement currents (±1% change from 1.7GHz to 2.5GHz), which are critical requirements for on-chip testing with current injection at RF frequencies.

Further evaluation of the current generator was conducted by embedding it together with a 2.1GHz impedance-matched low-noise amplifier and two power detectors, which required a 14% layout area overhead for the test circuitry. The simulation results obtained from the extracted layout of the current injection built-in test arrangement

indicate that the methodology and test circuitry are robust to process, voltage, and temperature variations. A gain (S_{21}) estimation error below 3.5% was observed under the influence of process corner models, -15°C to 65°C temperature variations, and power detector measurement error.

V.3. Opportunities for further research

Loopback method

The next phase of this project will involve additional characterization of the test chip. Optimizations of the test setup are necessary to obtain a better performance assessment, but the preliminary measurements of the loopback block helped to identify some design and layout improvements for more robust post-fabrication performance (section III.3.3).

Future research could involve a combination of the loopback method with current injection. This would provide opportunities to reduce the on-chip losses in the loopback, but also to shrink the layout area of the loopback block because the dimensions of the transistors and coupling capacitor in the output stage of the offset mixer could be reduced. In the voltage-mode loopback circuit, the devices in the output stage of the offset mixer are sized relatively large to apply the voltage at the low-impedance gate node of the LNA while minimizing coupling losses. With direct current injection as described in section IV, smaller capacitors (both < 200fF) could be used at the output in comparison with the voltage-mode approach (one ~3pF capacitor).

In general, the anticipated outcome of this research is to obtain experimental verification of the proposed testing techniques as an assessment of the practical

achievability of the loopback method based on measurement results from the proof-of-concept RF front-end test chip. Since the system-level algorithms for this approach are already available, a circuit level solution to support on-chip loopback would facilitate the adaptation of this alternative test approach in the industry. This still leaves the design and integration tasks related to realizing a complete transceiver with on-chip loopback and system-level functional verification based on bit error rate (BER) or error vector magnitude (EVM) analysis of the digital output in the baseband section.

Current injection BIT

In the discussed example design, the value of the current injected into the LNA was fixed. For applications in which a variable power level at the LNA input is desired, several options could be investigated:

- Change of the current division ratio in the generator by implementing C_1 and C_2 (in Fig. 44) with capacitor banks and digitally-controlled switches to alter their ratio m.
- Adjustment of the current generator's input signal power (at v_{test} in Fig. 44) through a variable attenuator.
- Sweep of the test current magnitude via a variable resistor (R_2 in Fig. 44) to change the current flow into the divider, which would be the most efficient option since a PMOS transistor operating in triode region may serve for that purpose.

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APPENDIX A

MATHEMATICAL DERIVATION:

OFFSET MIXER GAIN AND SPECTRAL COMPONENTS AT THE OUTPUT

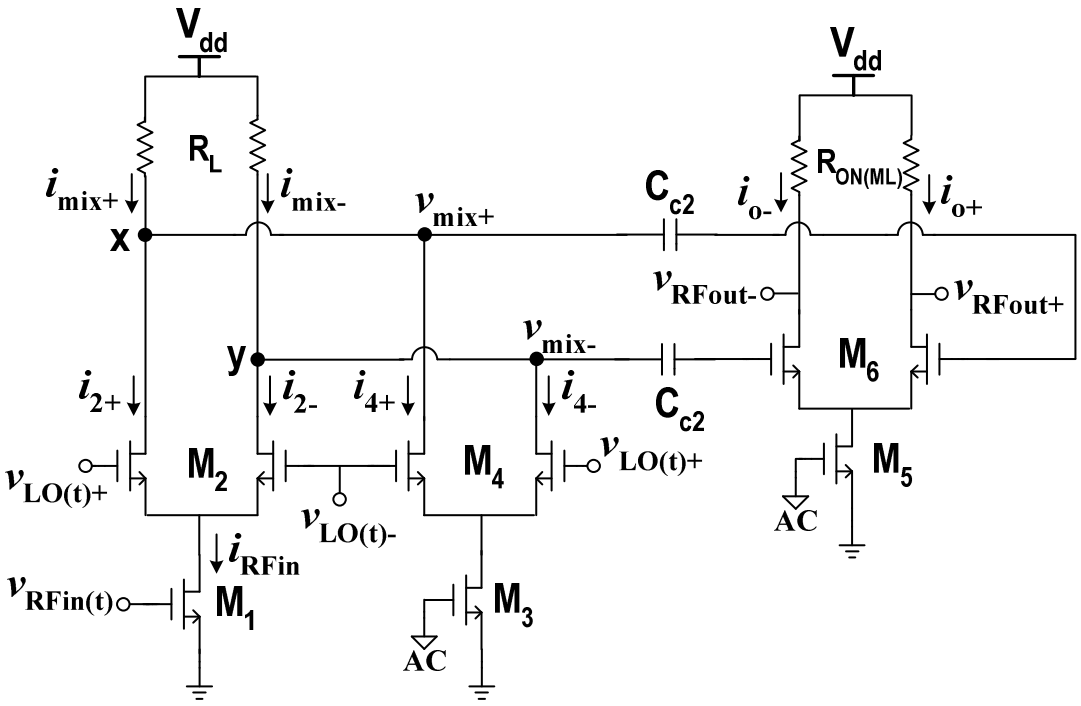


Fig. 51. Simplified offset mixer schematic

Assuming a sinusoidal RF input signal and a digital rail-to-rail local oscillator (LO) signal, the following derivation helps to assess the offset mixer conversion gain with respect to the various harmonic components that are present in the output signal. Fig. 51 has been simplified and labeled to emphasize the relevant mixer components/quantities:

$$i_{RF} = I_{DC(M1)} + g_{m1} v_{RFin} \cos(\omega_{RFin} t) \tag{A1}$$

where $I_{DC(M1)}$ is the average current through M_1, g_{m1} is the small-signal transconductance of M_1, and $v_{RFin(t)} = v_{RFin}\cos(\omega_{RFin}t)$ is the sinusoidal input signal. Since M_2/M_4 are

switched on and off by the LO signal, the switching operation can be expressed using the Fourier series representation of a square wave with a frequency of ω_{LO} and low/high levels of zero/one:

$$LO_{(t)+} = \tfrac{1}{2} + \tfrac{2}{\pi}\cos(\omega_{LO}t) - \tfrac{2}{3\pi}\cos(3\omega_{LO}t) + \tfrac{2}{5\pi}\cos(5\omega_{LO}t) - \ldots \quad \text{(A2)}$$

$$LO_{(t)-} = \tfrac{1}{2} - \tfrac{2}{\pi}\cos(\omega_{LO}t) + \tfrac{2}{3\pi}\cos(3\omega_{LO}t) - \tfrac{2}{5\pi}\cos(5\omega_{LO}t) + \ldots \quad \text{(A3)}$$

Using (A1)-(A3), the modulated currents in the mixer core are:

$$i_{2+} = i_{RF} \times LO_{(t)+} = I_{DC\_M1} \times LO_{(t)+} + g_{m1} v_{RFin} \cos(\omega_{RFin} t) \times LO_{(t)+}$$

$$i_{2+} = I_{DC\_M1} \times [\tfrac{1}{2} + \tfrac{2}{\pi}\cos(\omega_{LO}t) - \tfrac{2}{3\pi}\cos(3\omega_{LO}t) + \tfrac{2}{5\pi}\cos(5\omega_{LO}t) - \ldots]$$

$$+ g_{m1} v_{RFin} \cos(\omega_{RFin} t)[\tfrac{1}{2} + \tfrac{2}{\pi}\cos(\omega_{LO}t) - \tfrac{2}{3\pi}\cos(3\omega_{LO}t) + \tfrac{2}{5\pi}\cos(5\omega_{LO}t) - \ldots] \quad \text{(A4)}$$

$$i_{2-} = i_{RF} \times LO_{(t)-} = I_{DC\_M1} \times LO_{(t)-} + g_{m1} v_{RFin} \cos(\omega_{RFin} t) \times LO_{(t)-}$$

$$i_{2-} = I_{DC\_M1} \times [\tfrac{1}{2} - \tfrac{2}{\pi}\cos(\omega_{LO}t) + \tfrac{2}{3\pi}\cos(3\omega_{LO}t) - \tfrac{2}{5\pi}\cos(5\omega_{LO}t) + \ldots]$$

$$+ g_{m1} v_{RFin} \cos(\omega_{RFin} t)[\tfrac{1}{2} - \tfrac{2}{\pi}\cos(\omega_{LO}t) + \tfrac{2}{3\pi}\cos(3\omega_{LO}t) - \tfrac{2}{5\pi}\cos(5\omega_{LO}t) + \ldots] \quad \text{(A5)}$$

In the auxiliary branch, the gate of M_3 is an AC ground because only DC bias is supplied to the transistor. Thus, the currents through M_4 only consist of the DC components that are modulated with a 180 degree phase shift in comparison to the corresponding currents in the mixer core:

$$i_{4+} = I_{DC\_M3} \times LO_{(t)-}$$

Substituting (A3) and $I_{DC\_M1} = I_{DC\_M3}$ (M_1/M_3 have identical sizes and bias conditions):

$$i_{4+} = I_{DC\_M1} \times [\tfrac{1}{2} - \tfrac{2}{\pi}\cos(\omega_{LO}t) + \tfrac{2}{3\pi}\cos(3\omega_{LO}t) - \tfrac{2}{5\pi}\cos(5\omega_{LO}t) + ...] \quad \text{(A6)}$$

Similarly,

$$i_{4-} = I_{DC\_M1} \times [\tfrac{1}{2} + \tfrac{2}{\pi}\cos(\omega_{LO}t) - \tfrac{2}{3\pi}\cos(3\omega_{LO}t) + \tfrac{2}{5\pi}\cos(5\omega_{LO}t) - ...] \quad \text{(A7)}$$

Cancellation of the undesired components from the modulation of I_{DC_M1} with the LO harmonics [cost(ω_{LO}t), cost(3ω_{LO}t), cost(5ω_{LO}t),…] is achieved by the current summation at nodes "x" and "y":

$$i_{mix+} = i_{2+} + i_{4+}$$

$$i_{mix+} = g_{m1} v_{RFin} \cos(\omega_{RFin}t)[\tfrac{1}{2} + \tfrac{2}{\pi}\cos(\omega_{LO}t) - \tfrac{2}{3\pi}\cos(3\omega_{LO}t) + \tfrac{2}{5\pi}\cos(5\omega_{LO}t) - ...] + I_{DC\_M1}$$

where the DC component (I_{DC_M1}) can be removed because the voltage drop from it (across R_{L1}) is blocked by the capacitor C_{c2} in Fig. 51 between the mixer core and the output stage, resulting in:

$$i_{mix+} = g_{m1} v_{RFin} \cos(\omega_{RFin}t)[\tfrac{1}{2} + \tfrac{2}{\pi}\cos(\omega_{LO}t) - \tfrac{2}{3\pi}\cos(3\omega_{LO}t) + \tfrac{2}{5\pi}\cos(5\omega_{LO}t) - ...]$$

$$i_{mix+} = g_{m1} v_{RFin} [\tfrac{1}{2}\cos(\omega_{RFin}t) + \tfrac{1}{\pi}\cos([\omega_{RFin} \pm \omega_{LO}]t) - \tfrac{1}{3\pi}\cos([\omega_{RFin} \pm 3\omega_{LO}]t) + ...] \quad \text{(A8)}$$

Similarly,

$$i_{mix-} = g_{m1} v_{RFin} [\tfrac{1}{2}\cos(\omega_{RFin}t) - \tfrac{1}{\pi}\cos([\omega_{RFin} \pm \omega_{LO}]t) + \tfrac{1}{3\pi}\cos([\omega_{RFin} \pm 3\omega_{LO}]t) - ...] \quad \text{(A9)}$$

From the above currents, the output voltages of the mixer core that pass C_{c2} and appear at the gate of M_6 can be calculated with:

$$v_{mix+} = i_{mix+} \times R_L \quad \text{(A10)}$$

$$v_{mix-} = i_{mix-} \times R_L \tag{A11}$$

Notice that the output spectrum contains mixing by-products (ω_{RFin}-ω_{LO}, ω_{RFin}±3ω_{LO}, ω_{RFin}±5ω_{LO},…) that are around the output frequency $\omega_{RFout} = \omega_{RFin}+\omega_{LO}$. The expressions below can be formed from (A8)-(A11) with the appropriate substitutions and rearrangements for any relevant spectral components at the output.

Differential mixer core gain at $\omega_{RFout} = \omega_{RFin}+\omega_{LO}$:

$$\boxed{G_{core\_diff} = \frac{v_{mix+} - v_{mix-}}{v_{RFin}} = \frac{2 g_{m1} R_L}{\pi}} \tag{A12}$$

Another component at ω_{RFin}-ω_{LO} that is undesired for BER testing, but can be removed by the filtering operations in the receiver chain as explained in the discussion of Fig. 26 in section III.2.5 on page 54 is:

$$G_{unwanted\ @(\omega_{RFin} - \omega_{LO})} = \frac{v_{mix+} - v_{mix-}}{v_{RFin}} = \frac{2 g_{m1} R_L}{\pi} \tag{A13}$$

Direct common-mode feedthrough at ω_{RFin}:

$$G_{feedthrough\ @\ \omega_{RFin}} = \frac{v_{mix+} + v_{mix-}}{v_{RFin}} = g_{m1} R_L \tag{A14}$$

Since this strong RF component is only distance ω_{LO} away from ω_{RFout} on the frequency axis, a mixer output stage was used that provides common-mode rejection in addition to further amplification. This common-mode rejection property to attenuate the spectral component at ω_{RFin} in (A14) is derived in Appendix B. Fig. 52 displays the spectral content of the voltage signal (v_{mix+}) in the mixer core, which agrees with the terms above.

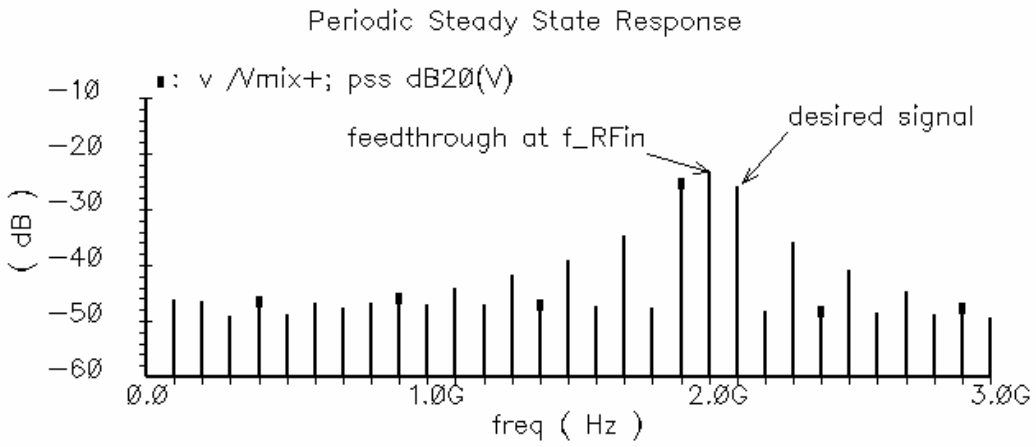


Fig. 52. Mixer core output voltage spectrum

In the output stage, $R_{ON(ML)}$ (Fig. 51) represents the resistance of M_L in triode region and the output voltages are:

$$v_{RFout+} = i_{o+} \times R_{ON(ML)} = g_{m6} v_{mix+} R_{ON(ML)} \tag{A15}$$

$$v_{RFout-} = i_{o-} \times R_{ON(ML)} = g_{m6} v_{mix-} R_{ON(ML)} \tag{A16}$$

Thus, the gain of the differential pair at the output is:

$$\boxed{G_{stage2\_diff} = \frac{v_{RFout+} - v_{RFout-}}{v_{mix+} - v_{mix-}} = g_{m6} R_{ON(ML)}} \tag{A17}$$

Since $v_{mix+} = -v_{mix-} \rightarrow v_{RFout+} = -v_{RFout-}$, the gain of the second stage with a single-ended output is:

$$\boxed{G_{stage2\_s-e} = \frac{v_{RFout+}}{v_{mix+} - v_{mix-}} = \frac{v_{RFout+}}{2v_{mix+}} = \frac{g_{m6} R_{ON(ML)}}{2}} \tag{A18}$$

The overall conversion gain at $\omega_{RFout} = \omega_{RFin}+\omega_{LO}$ can be obtained by combining the gains of the two stages, resulting the expressions below.

Differential output:

$$\boxed{G_{mix\_diff} = G_{core\_diff} \times G_{stage2\_diff} = \frac{2g_{m1}R_L}{\pi} \times g_{m6}R_{ON(ML)}} \quad \text{(A19)}$$

Single-ended output:

$$\boxed{G_{mix\_s-e} = G_{core\_diff} \times G_{stage2\_s-e} = \frac{2g_{m1}R_L}{\pi} \times \frac{g_{m6}R_{ON(ML)}}{2}} \quad \text{(A20)}$$

APPENDIX B

MATHEMATICAL DERIVATION:

SUPPRESSION OF RF FEEDTHROUGH IN THE OFFSET MIXER

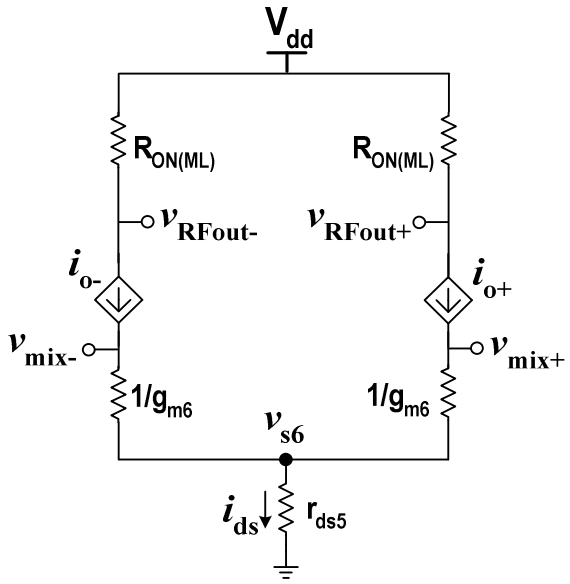


Fig. 53. Simplified small-signal equiv. circuit for the offset mixer output stage

Transistors M_5 and M_6 in the second stage of the offset mixer (Fig. 51) on page 104 are both biased in saturation region and represented with the T-Model in Fig. 53, which was simplified by removing the drain-source resistance of M_6 ($r_{ds6} >> 1/g_{m6}$) and the transconductance of the bias current source M_5 (no small-signal input: $v_{gs5} = 0$). Transistor M_L is biased in triode region and was replaced with $R_{ON(ML)}$ to model the channel resistance. The objective in the following analysis is to investigate the common-mode rejection property of this mixer stage rather than the high-frequency characteristics, which is why parasitic capacitances are ignored for simplicity. Noting

from the expressions in Appendix A that the unwanted signal component at ω_{RFin} appears as common-mode signal (v_{cm}) at nodes v_{mix+} and v_{mix-}:

$$v_{cm} = v_{mix(@\omega_{RFin})} = v_{mix+} = v_{mix-} \tag{B1}$$

The sources of M_6 on both sides are connected together, hence it follows from (B1) that their small-signal currents due to the common-mode input at the gates are the same:

$$i_{cm} = i_{o+} = i_{o-} \tag{B2}$$

Summing the currents in the two branches yields the small-signal current (i_{ds5}) through the drain-source impedance of M_5. Knowing that $i_{ds5} = i_{o+} + i_{o-} = 2\ i_{cm}$ allows to express the voltage at the source of M_6 (v_{s6}) in terms of the common-mode current:

$$v_{s6} = 2\, i_{cm}\ r_{ds5} \tag{B3}$$

Another observation that can be made from Fig. 53 is:

$$i_{cm} = (v_{cm} - v_{s6}) g_{m6} = g_{m6}(v_{cm} - 2\, i_{cm}\ r_{ds5}) \tag{B4}$$

Solving (B4) for i_{cm} results in:

$$i_{cm} = i_{o+/-} = \frac{g_{m6} v_{cm}}{1 + 2 g_{m6} r_{ds5}} = \frac{g_{m6} v_{mix+/-}}{1 + 2 g_{m6} r_{ds5}} \tag{B5}$$

The small-signal voltage at each output terminal due to common-mode input is:

$$v_{RFout+/-} = i_{o+/-} R_{ON(ML)} = \frac{g_{m6} R_{ON(ML)} \times v_{mix+/-}}{1 + 2 g_{m6} r_{ds5}} \tag{B6}$$

With a single-ended output, equation (B6) can be rearranged to express the common-mode gain of the mixer output stage:

$$\boxed{A_{v\_cm} = A_{v(\omega_{RFin})} = \frac{v_{RFout+}}{v_{mix+}} = \frac{g_{m6} R_{ON(ML)}}{1 + 2 g_{m6} r_{ds5}}} \tag{B7}$$

From (B7) it is clear that the differential pair (M_6) in the output stage provides common-mode rejection when the design satisfies: $g_{m6} \times r_{ds5} > g_{m6} \times R_{ON(ML)}$. This property is thanks to the shared tail current source (M_5) and it was taken advantage of in the offset mixer design to suppress the common-mode signal at ω_{RFin}.

If the LNA has a differential input, then improved suppression of the common-mode signal is possible:

$$A_{v-diff\_cm} = \frac{v_{RFout+} - v_{RFout-}}{v_{mix+} - v_{mix-}} = \frac{i_{o+} R_{ON(ML)} - i_{o-} R_{ON(ML)}}{v_{mix+} - v_{mix-}} = \frac{i_{cm} R_{ON(ML)} - i_{cm} R_{ON(ML)}}{v_{mix+} - v_{mix-}} = 0 \qquad \text{(B8)}$$

where (B8) was obtained by substitution of (B6) and (B2). Based on the above expression, the common-mode signal is entirely suppressed, which is not the case in practice as a result of device mismatches ($R_{ON(ML)}$ and g_{m6} are not exactly identical in both branches due to process variations). Nevertheless, the common-mode rejection in the differential case is significantly better than with a single-ended output.

The attenuation of the undesired spectral content at f_{RFin} can also be observed by comparing the single-ended voltage spectra in the mixer core (Fig. 52 in Appendix A) and at the output of the second stage in Fig. 54 below.

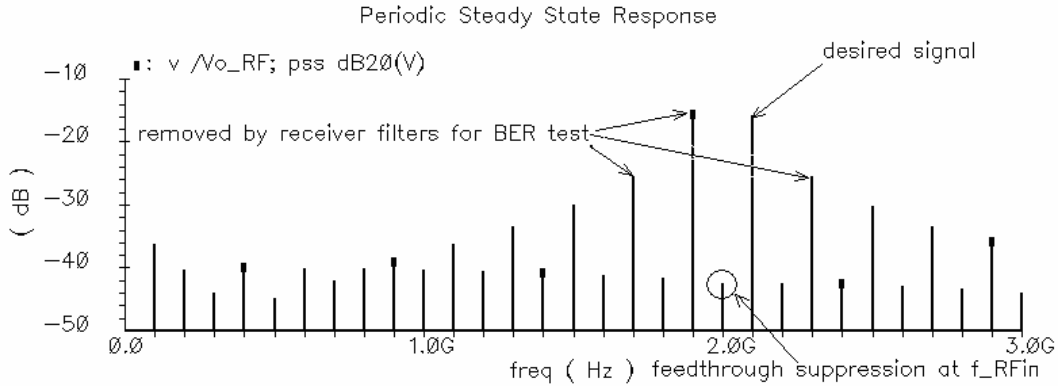


Fig. 54. Mixer stage 2: single-ended output voltage spectrum

APPENDIX C

SUMMARY OF SIMULATION RESULTS:

EFFECTS OF THE LOOPBACK BLOCK AND RMS DETECTORS ON LNA/PA PERFORMANCE

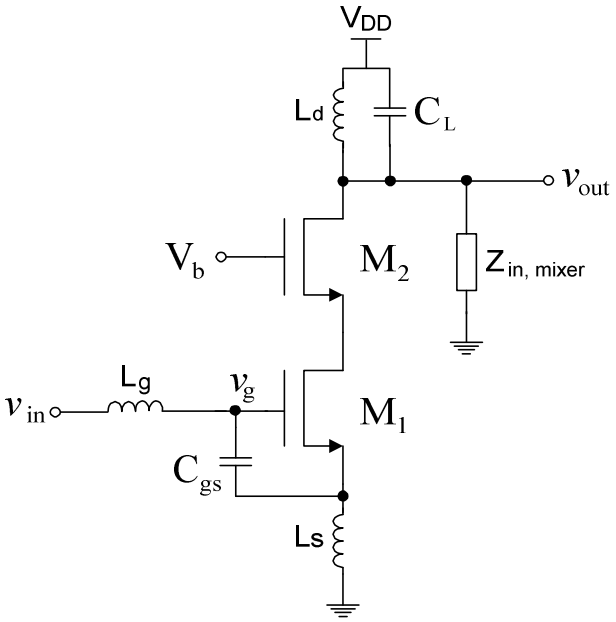


Fig. 55. LNA schematic (UMC 0.13μm techn./1.2V supply)

Table XVIII. LNA performance comparison

Parameter (at 2.1GHz)	**Without BIT Circuitry Connections***	**With BIT Circuitry Loading****
S_{21}	20.2dB	20.0dB
S_{11}	-9.9dB	-9.7dB
NF	0.9dB	0.9dB
1-dB Compression Point	-11.4dBm	-11.9dBm
IIP3	1.2dBm	1.5dBm
Power Consumption	4.4mW	

* With 8.5nH gate inductance.

** With 7.0nH gate inductance, RMS detectors at v_{out}/v_g, loopback at v_g in Fig. 55.

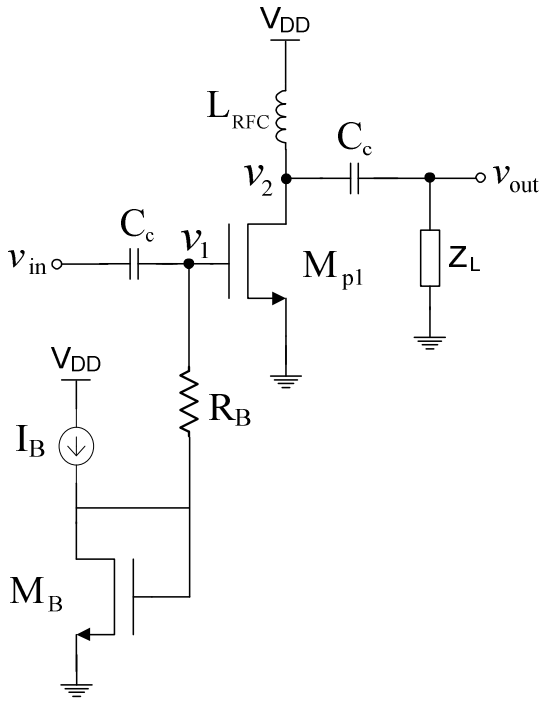


Fig. 56. PA schematic (class A, UMC 0.13μm techn./1.2V supply)

Table XIX. Transmitter buffer (PA) performance comparison

Parameter (at 2GHz)	**Without BIT Circuitry Connections (driving pad & 50Ω)**	**With BIT Circuitry Loading* (driving pad & 50Ω)**
RMS Power Gain	2.7dB	2.5dB
1-dB Compression Point	-4.4dBm	-4.5dBm
IIP3	9.4dBm	8.9dBm
S_{22}	-8.8dB	-9.1dB
Output Power	-0.02dBm	-0.21dBm
Power Consumption	6.8mW	

* RMS detectors at v_1/v_2, loopback at v_{out} in Fig. 56.

APPENDIX D

ADDITIONAL PLOTS FROM THE LOOPBACK BLOCK SIMULATIONS

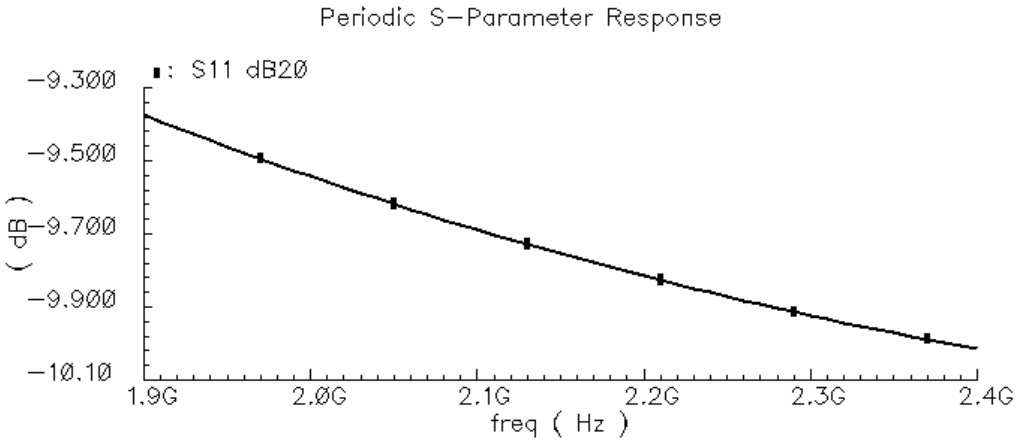


Fig. 57. Loopback block: S_{11} vs. frequency

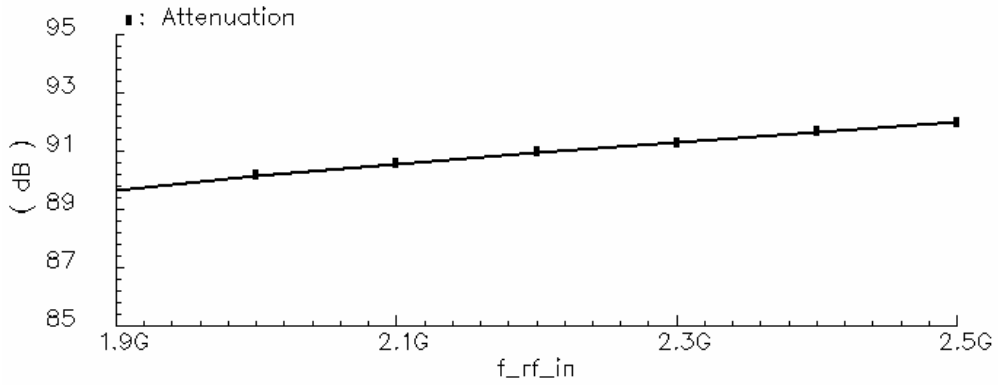


Fig. 58. Loopback block: Tx/Rx isolation (attenuation in off-state)

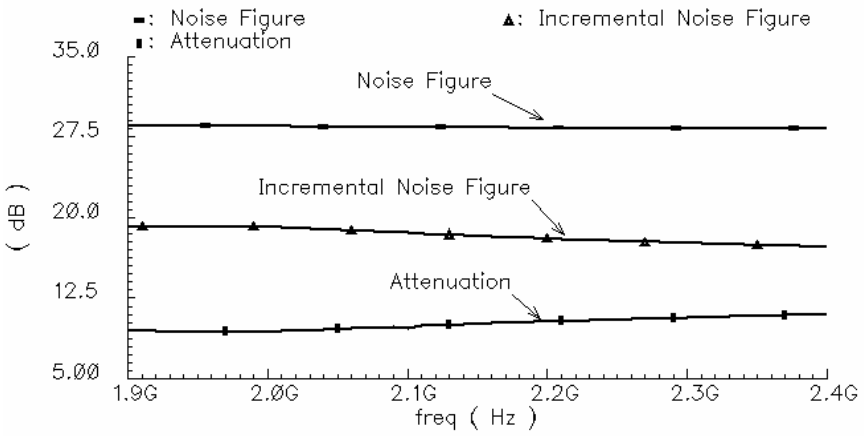


Fig. 59. Loopback block: noise figure vs. frequency (min. atten. setting)

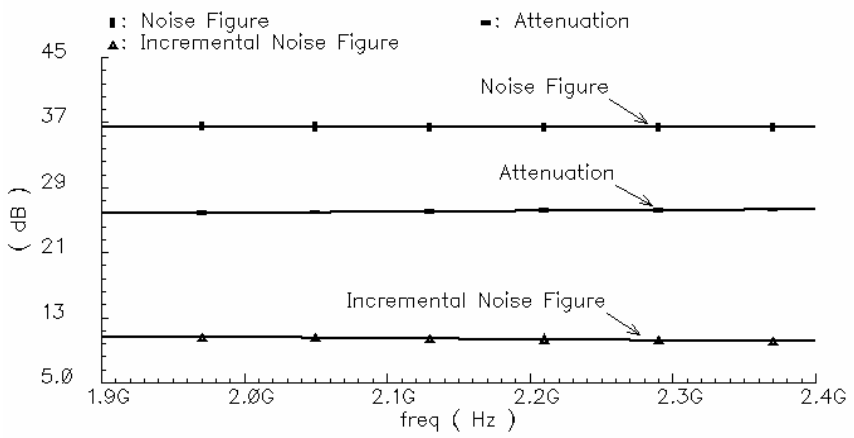


Fig. 60. Loopback block: noise figure vs. frequency (max. atten. setting)

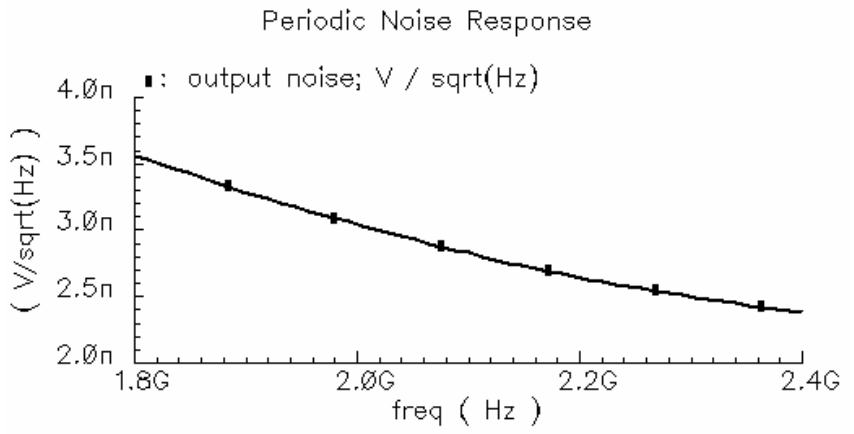
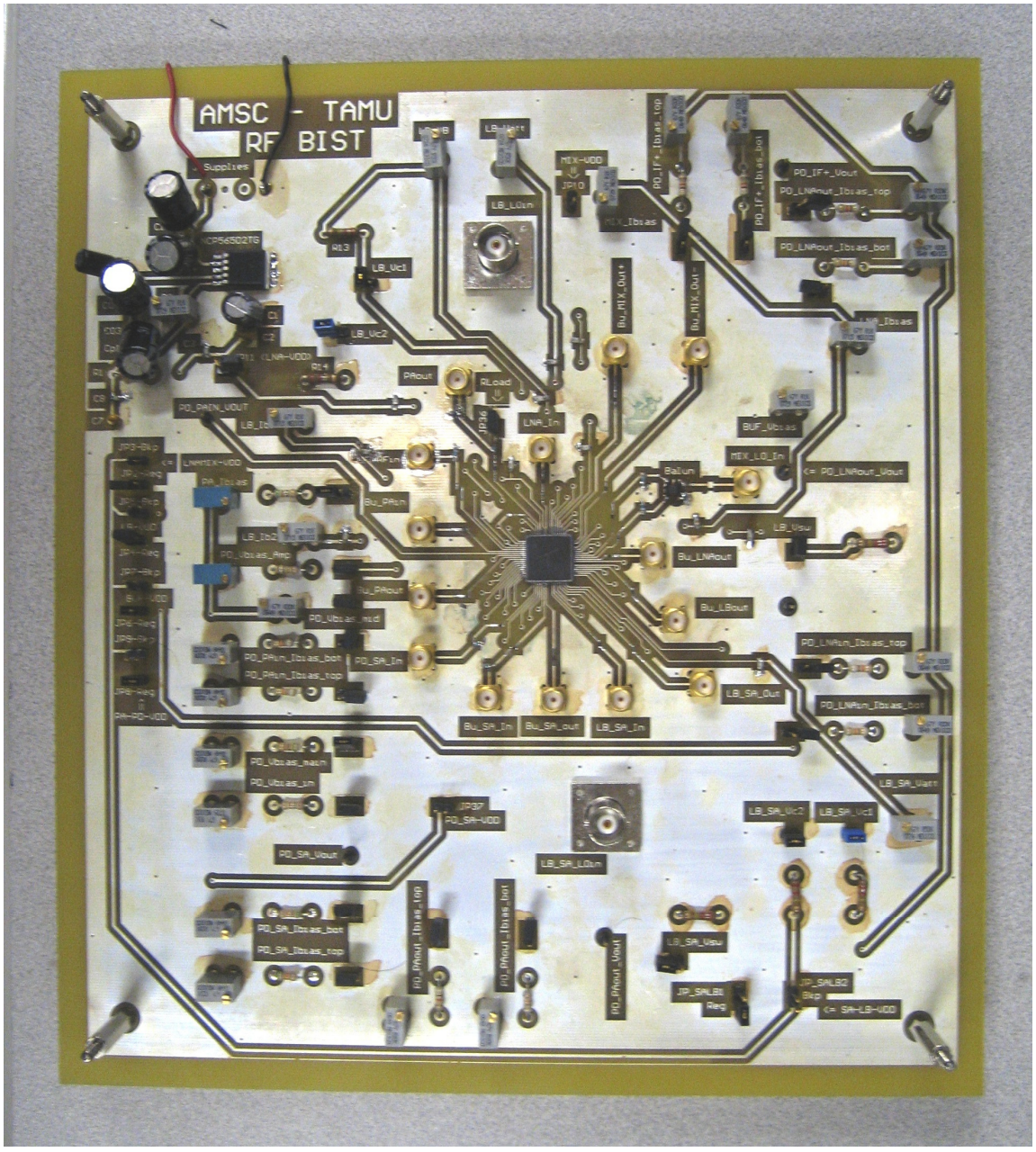


Fig. 61. Loopback block: worst-case output noise (V/√Hz) vs. frequency

APPENDIX E

PRINTED CIRCUIT BOARD FOR

SYSTEM-LEVEL FUNCTIONALITY ASSESSMENT



APPENDIX F

SUMMARY OF SIMULATION RESULTS:

EFFECTS OF THE CURRENT GENERATOR AND RMS DETECTOR ON LNA PERFORMANCE

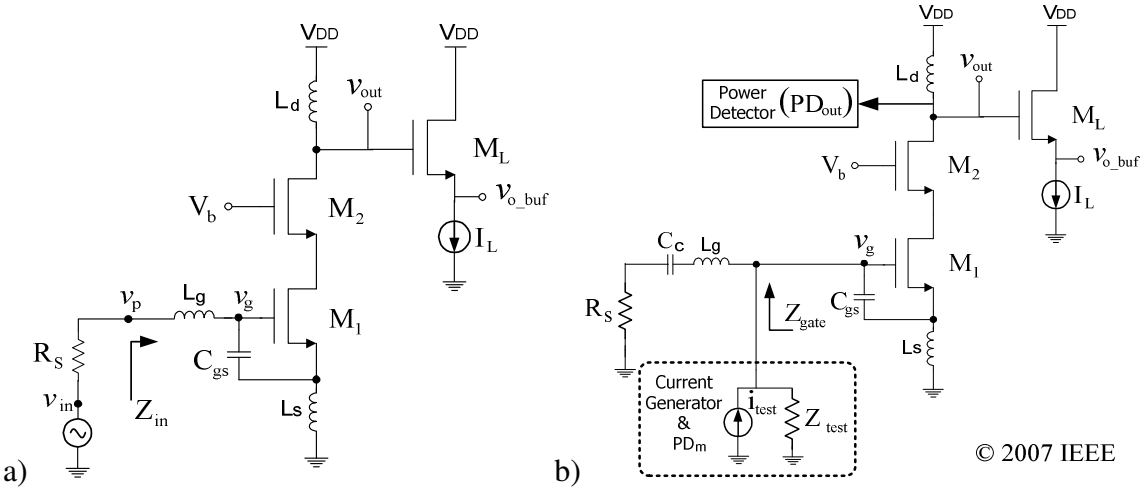


Fig. 62. LNA & output buffer (M_L): (a) normal config. (b) current injection BIT

Table XX. LNA performance comparison – current injection BIT

Parameter (at 2.1GHz)	**Without BIT Circuitry Connections (Fig. 62a)**	**With BIT Circuitry Loading (Fig. 62b)**
S_{21} @ v_{out}	23.89dB	23.92dB
S_{11} @ v_{out}	-12.11dB*	-15.76dB*
NF @ v_{out}	0.61dB	0.66dB
S_{22} @ v_{o_buf}	-15.53dB	-15.52dB
Input 1-dB Compression Point	-14.55dBm	-14.78dBm
IIP3	-2.03dBm	-2.54dBm

* S_{11} was optimized with parasitic capacitance of BIT circuitry, which remains connected during normal operation.

APPENDIX G

ADDITIONAL PLOTS FROM THE CURRENT GENERATOR SIMULATIONS

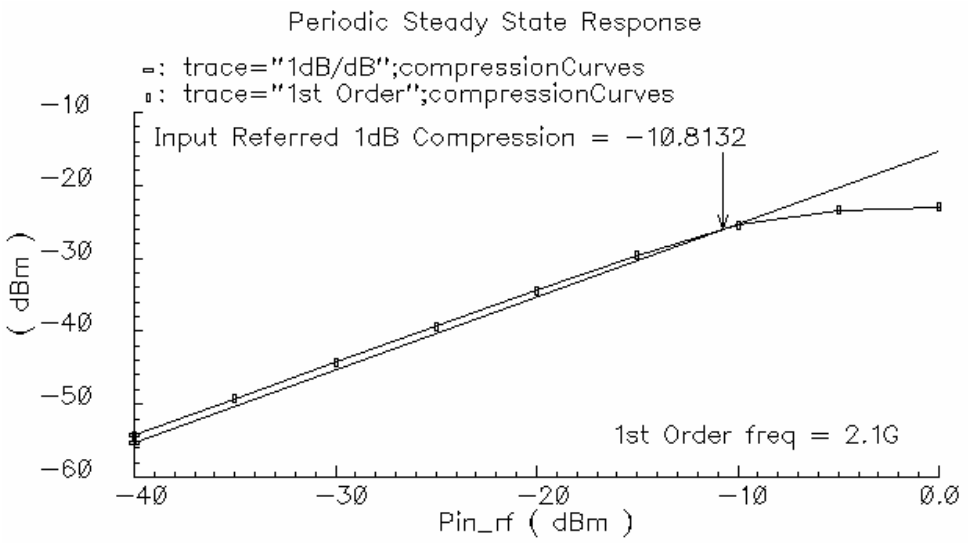


Fig. 63. Current generator: 1dB compression curve

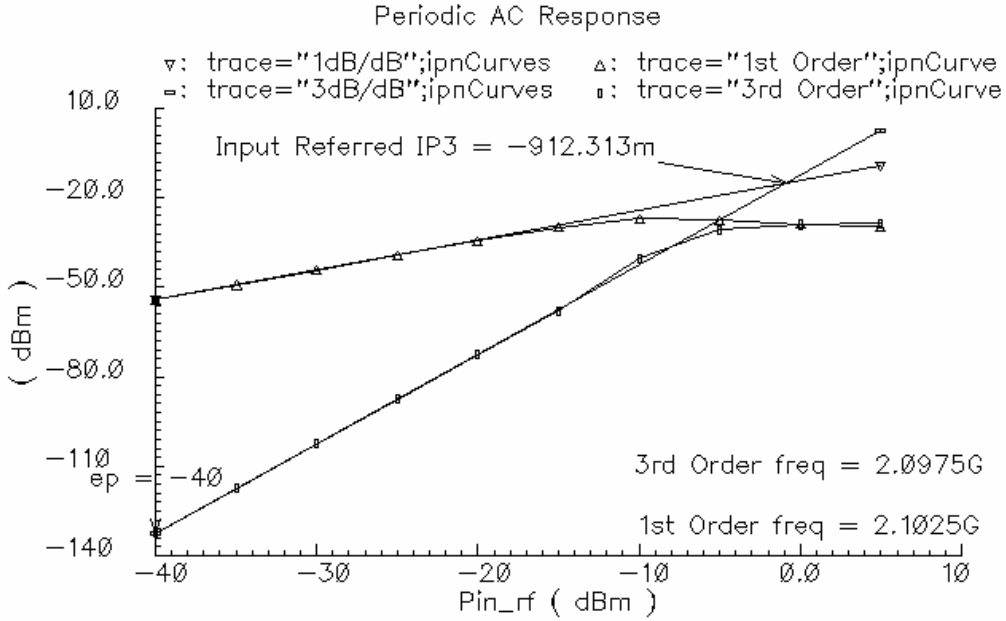


Fig. 64. Current generator: input third-order intercept point (IIP3)

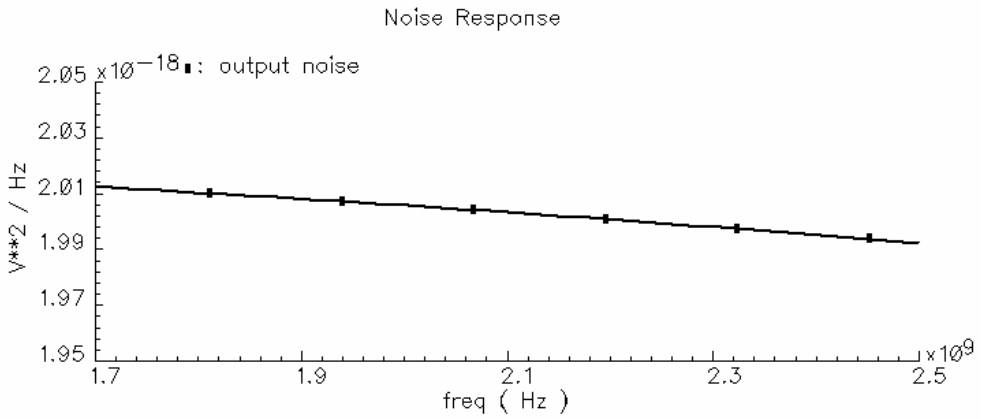


Fig. 65. Current generator: output noise (V^2/Hz) vs. frequency

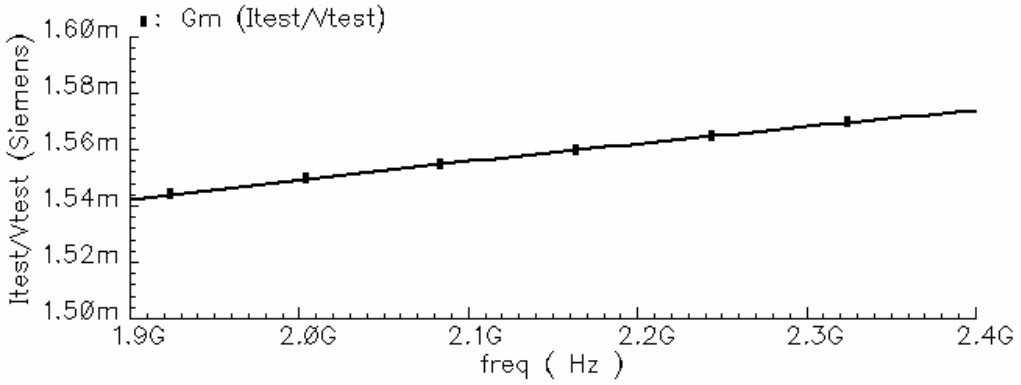


Fig. 66. Current generator: g_{test} (i_{test} / v_{test}) vs. frequency

VITA

Marvin Onabajo was born in Lengerich, North Rhine-Westphalia, Germany in 1982. He received his B.S. in electrical engineering from The University of Texas at Arlington in December 2003, where he worked in the analog and mixed-signal IC group during his final year in affiliation with the National Science Foundation's Research Experiences for Undergraduates program. From 2004 to 2005, he was Electrical Test Process/Product Engineer at Intel Corp. in Hillsboro, Oregon. He has been a member of the Analog and Mixed-Signal Center at Texas A&M University since August 2005 and is currently engaged in research projects involving analog built-in testing and dataconverters. He received his M.S. degree in December 2007 and can be contacted through the Department of Electrical & Computer Engineering at Texas A&M University:

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