DESIGN AND IMPLEMENTATION OF FREQUENCY SYNTHESIZERS FOR 3-10 GHZ MULTIBAND OFDM UWB COMMUNICATION

A Dissertation

by

CHINMAYA MISHRA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2007

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	Jose Silva-Martinez
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ABSTRACT

Design and Implementation of Frequency Synthesizers for 3-10 GHz Multiband OFDM UWB Communication. (December 2007)

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The allocation of frequency spectrum by the FCC for Ultra Wideband (UWB) communications in the 3.1-10.6 GHz has paved the path for very high data rate Gb/s wireless communications. Frequency synthesis in these communication systems involves great challenges such as high frequency and wideband operation in addition to stringent requirements on frequency hopping time and coexistence with other wireless standards. This research proposes frequency generation schemes for such radio systems and their integrated implementations in silicon based technologies. Special emphasis is placed on efficient frequency planning and other system level considerations for building compact and practical systems for carrier frequency generation in an integrated UWB radio.

This work proposes a frequency band plan for multiband OFDM based UWB radios in the 3.1-10.6 GHz range. Based on this frequency plan, two 11-band frequency synthesizers are designed, implemented and tested making them one of the first frequency synthesizers for UWB covering 78% of the licensed spectrum. The circuits are implemented in 0.25μm SiGe BiCMOS and the architectures are based on a single VCO

at a fixed frequency followed by an array of dividers, multiplexers and single sideband (SSB) mixers to generate the 11 required bands in quadrature with fast hopping in much less than 9.5 ns. One of the synthesizers is integrated and tested as part of a 3-10 GHz packaged receiver. It draws 80 mA current from a 2.5 V supply and occupies an area of 2.25 mm^2.

Finally, an architecture for a UWB synthesizer is proposed that is based on a single multiband quadrature VCO, a programmable integer divider with 50% duty cycle and a single sideband mixer. A frequency band plan is proposed that greatly relaxes the tuning range requirement of the multiband VCO and leads to a very digitally intensive architecture for wideband frequency synthesis suitable for implementation in deep submicron CMOS processes. A design in 130nm CMOS occupies less than 1 mm^2 while consuming 90 mW. This architecture provides an efficient solution in terms of area and power consumption with very low complexity.

DEDICATION

To my Parents and Brother,

For their unconditional love and support.

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CHAPTER I

INTRODUCTION

1.1 Motivation

The insatiable need to transfer information at very high speeds and to be able to do so anywhere in the world and at any time, has been the driving force for the growth of wireless communication industry. The growth in personal wireless communications has been possible due to the constant advancement in the semiconductor industry. Silicon technology has significantly matured to allow lower costs of implementation of wireless communication integrated circuits (ICs) while allowing integration of radio frequency (RF), analog and digital functionalities on a single chip with minimum external components [1,2].

There are many wireless communication standards existing today that differ in terms of data rate, range and frequency of operation. They fall under three main categories: wireless personal area network (WPAN), wireless local area network (WLAN) and wireless wide area network (WWAN) as shown in Fig. 1.1 [3]. WPAN and WLAN are short-range communication standards with range of 100 meters or less with bandwidths limited to few tens of MHz and with data rate less than 100 Mb/s. The ever-increasing demand for higher data rates has lead to the use of larger bandwidths. The allocation of frequency spectrum by the federal communications commission (FCC) for Ultra Wideband (UWB) communications in the 3.1-10.6 GHz range has paved the path

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This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits*.

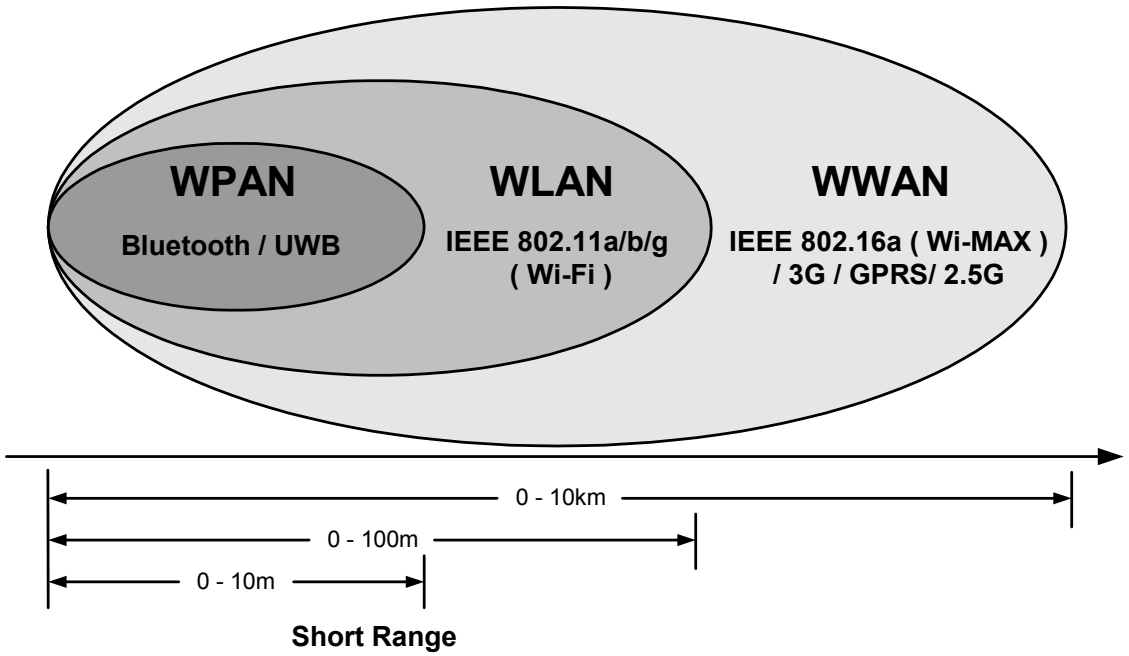

Fig. 1.1 Main categories of wireless communication standards.

for short-range, very high data rate, Gb/s wireless communications.

Due to the extremely wideband nature of these communication ICs, narrowband circuit techniques that are conventionally used are not suitable to implement UWB radios. Frequency translation is used in a radio transceiver to move the information from RF to baseband and vice versa. A local oscillator (LO) signal is integral to any radio to perform this up-conversion and down-conversion in one or many steps. The process of creating this LO signal is known as frequency generation or synthesis. Contrary to narrowband radios, frequency synthesis in UWB communication systems involves great challenges such as high frequency and wideband operation in addition to stringent requirements on frequency hopping time and coexistence with other wireless standards.

This dissertation explores different methods for realizing such frequency generation systems in standard silicon technologies. Special emphasis is placed on efficient frequency planning and system level considerations for building compact and practical systems for carrier frequency generation in an integrated UWB radio.

1.2 Organization

A brief introduction to UWB systems is presented in Chapter II with special emphasis on multiband orthogonal frequency division multiplexing (MB-OFDM) based UWB radios. To provide a better appreciation, other approaches to implementing a UWB system are also presented and their main features highlighted.

Chapter III introduces the problem of frequency synthesis in ultra wideband systems. The need for efficient frequency planning and evaluating synthesizer architectures based on macromodel simulations is emphasized and demonstrated via examples. A frequency band plan is proposed which greatly relaxes the design of a 3-10 GHz frequency synthesizer. The specifications for the LO signal in an integrated radio are provided based on system level simulations. Finally, various possible synthesizer solutions are evaluated based on these performance specifications.

The next two chapters discuss circuit level implementations of the synthesizers in silicon-based technologies. Chapter IV discusses two different 11-band, 3-10 GHz frequency synthesizer implementations that were designed in 0.25 μm SiGe BiCMOS technologies. The architecture descriptions are provided along with the design details and layout considerations for different building blocks. One of the synthesizer

implementations was integrated in a 3-10 GHz MB-OFDM UWB receiver. These synthesizers were one of the first implementations covering the entire 3-10 GHz range to be reported.

Chapter V explores the realization of a UWB frequency synthesizer based on a multiband VCO in CMOS. A band plan is proposed that greatly relaxes the tuning range requirement of the multiband VCO and leads to a very digitally intensive architecture for wideband frequency synthesis. Design and implementation details are presented with different circuit examples.

Finally, conclusions are provided in Chapter VI with discussion on future possible implementations for such wideband synthesizers.

CHAPTER II

ULTRA WIDEBAND (UWB) SYSTEMS

2.1 Short-Range Wireless Communication

Short-range wireless is a complimentary class of emerging technologies meant primarily for indoor use over very short distances (less than 10 meters) [3]. The need for sending large volumes of data over very long distances and at very high speeds, while providing good quality service to a large number of users all at the same time, serves as the driving force for the ever-growing RF and wireless industry. The growing presence of high speed wired access to the internet in enterprises, homes, and public spaces has paved the way for the launch of short-range wireless standards such as Bluetooth, Wi-Fi (the leading technologies for wireless PANs and LANs respectively), and an emerging technology called Ultra Wideband (UWB).

The goal of UWB technology is to provide very high data rates (up to 480Mbps) at modest cost and low power consumption. In 2002, the United States Federal Communications Commission (FCC) allowed UWB communications in the 3.1 – 10.6 GHz band having a -10 dB bandwidth greater than 500 MHz and a maximum equivalent isotropic radiated power (EIRP) spectral density of -41.3 dBm/MHz [4] as shown in Fig. 2.1. This low emission limit ensures that UWB devices do not pose as a source of interference to existing wireless standards. However, as can be seen from Fig. 2.1 that the Unlicensed National Information Infrastructure (U-NII) band from 5.15-5.825 GHz overlaps with the UWB spectrum. The interference from 802.11a devices can render the

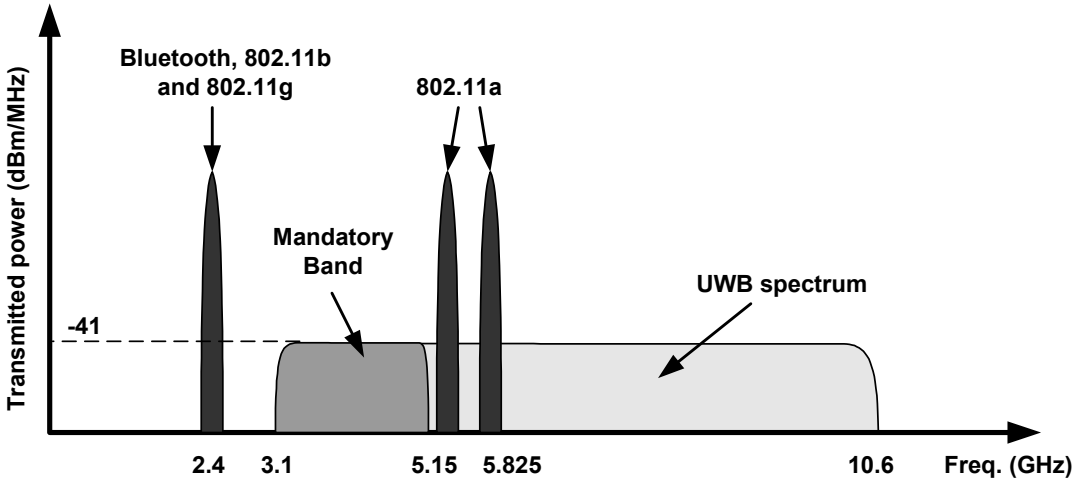

Fig. 2.1 Spectrum of UWB signal in comparison to other wireless standards.

communication between UWB devices using this band useless. This is because while the maximum output power of a UWB transmitter can reach about –10 dBm when using 1584 MHz of bandwidth (three bands of 528 MHz), the devices operating in the mentioned U-NII band can have a transmit power of 16 dBm or higher [5]. This is one of the reasons why the band from 3-5 GHz is considered mandatory and the other higher frequency bands are optional.

2.2 Need for UWB Technology

The main advantage of UWB technology is the high channel capacity that it offers. This can be understood from Shannon's capacity limit theorem [6] according to which, the maximum capacity (C in bits/sec) of a communication channel is given by

$$C = B\log_2(1+SNR) \tag{2.1}$$

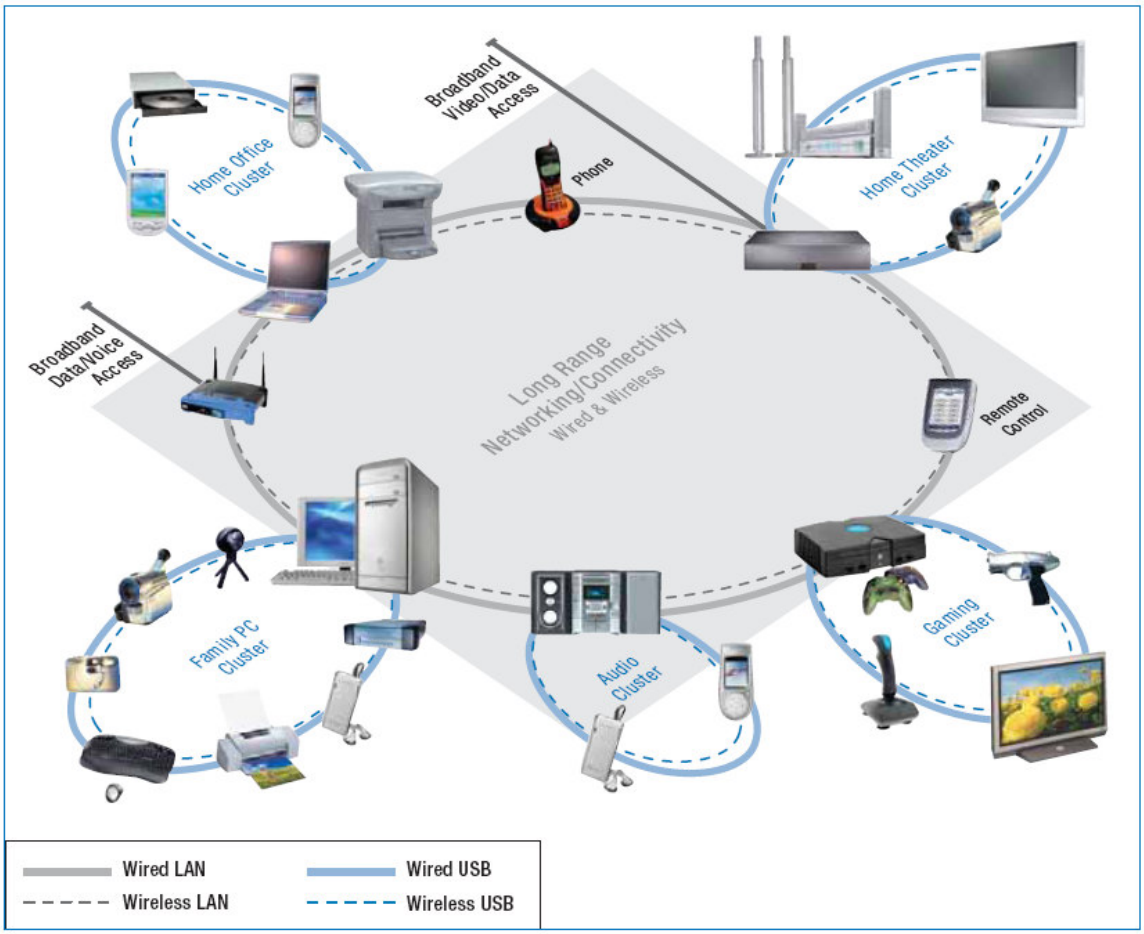

Fig. 2.2 Home usage scenario with wireless USB.

where B is the channel bandwidth in Hz and SNR is the signal to noise ratio. According to the above equation the capacity of a channel grows linearly with the used bandwidth while only logarithmically with the SNR. In this way, by significantly increasing the signal bandwidth with respect to existent narrowband technologies, UWB can achieve a higher channel capacity with a lower power spectral density (PSD) and hence provide an effective solution to the ever-increasing data rate demands in the space of wireless personal area networks (WPAN).

A short-range wireless technology with high data rate capabilities (>50MB/s), such as UWB, is demanded by a wide range of applications. Some of the applications are shown in Fig. 2.2 [7]. Wireless Universal Serial Bus or wireless USB (WUSB) is pitted as one of the most important application that will be based on UWB technology. USB is one of the most widely used interfaces for inter device communication. However, the increase in number of devices at home and or office and the need to exchange large amount of data among such devices requires the elimination of wires together with increased data rates close to 480 Mb/s or higher. That is where WUSB finds its use.

Some of the applications at home would include data transfer from devices such as digital camera, MP3 player, DVD player to the PC or TV. At office a very useful application would be transfer of information (especially multimedia presentation) from the laptop to the projector wirelessly. With the increase in performance and quality of storage devices that can store huge amount of good quality audio and video, the need for sharing them between devices effectively and quickly has become a necessity. UWB aims at providing a solution to such requirements.

2.3 Different Approaches to Implement UWB Systems

There are two main approaches for the implementation of very high data rate UWB communication devices. These are: (1) Direct sequence spread spectrum (DS-SS), (2) and Multiband OFDM (MB-OFDM). Although the MB-OFDM approach has received the strongest support from the consumer electronics industry and is the focus of this dissertation, it is still important to understand the key features of the other approach.

2.3.1 Direct Sequence Spread Spectrum (DS-SS) UWB

According to the DS-SS UWB proposal UWB communication uses pulses with a bandwidth of 2.1 GHz modulated using binary orthogonal keying [8], [9]. Multiple users share the same bandwidth and are separated by the digital codes that are employed to perform the spreading of the signal. A pseudorandom code is used to spread each data bit with a large number of chips, where a chip interval is much smaller than a bit interval. This results in the spreading of energy in the frequency domain to large bandwidths [10]. Important advantages of this technique include propagation benefits of UWB pulses that experience no Rayleigh fading and scalability to achieve data rates beyond 1 Gbps [10].

2.3.2 Multiband Orthogonal Frequency Division Multiplexing (MB-OFDM) UWB

MB-OFDM which is considered to be the most popular technology for high data rate UWB communication, combines orthogonal frequency division multiplexing (OFDM) with multibanding. OFDM has been successfully used in different wired and wireless communication systems such as, asymmetric digital subscriber line (ADSL) and IEEE 802.11a [5]. OFDM distributes the information over a set of carriers, which are orthogonal to each other in frequency. Each individual sub-carrier is modulated in phase and amplitude according to a given constellation format such as QPSK or 16-QAM.

To divide the available UWB spectrum into several sub-bands in combination with OFDM modulation is an effective technique to capture multi-path energy, achieve spectral efficiency and gain tolerance to narrow-band interferences for a very high data

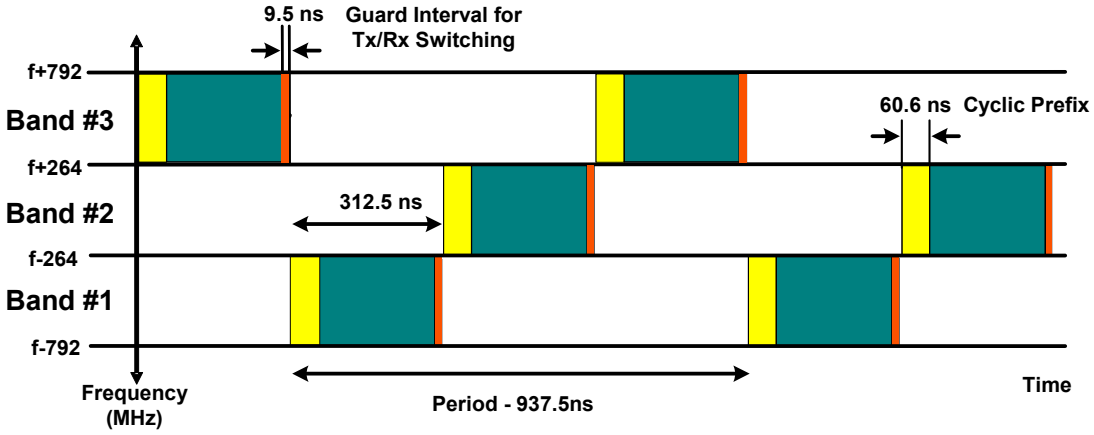

Fig. 2.3 Band hopping in MB-OFDM UWB approach.

rate (>200 Mbps) system [11]. The multiband approach allows to selectively discard the use of certain bands for UWB communication such as 802.11a at 5 GHz. The MB-OFDM approach divides the available 7500 MHz UWB spectrum into 14 bands of 528 MHz each. The bands are grouped into 5 band groups. Only the first group of 3 bands, corresponding to the lower part of the spectrum (3.1-4.8 GHz), is considered as mandatory. The remaining band groups have been defined and left as optional to enable a structured and progressive expansion of the system capabilities. For the OFDM symbol, the standard considers 128 carriers, from which 100 tones contain information and the rest are either guard tones or pilot sub-carriers, which are employed for synchronization. Each sub-carrier is modulated with a QPSK constellation.

The UWB communication (transmission and reception) takes place based on a time-frequency code that determines what frequency to use at which time. The radio switches between three adjacent frequencies that are separated by 528 MHz in frequency as shown in Fig. 2.3 [12-13]. In Fig. 2.3, the first OFDM symbol is transmitted on band

#3, the second on band #1 and the third on band #2. A cyclic prefix is inserted before every OFDM symbol and a guard interval is appended to every OFDM symbol. The 9.5 ns of guard interval allows for the change in the local oscillator signal in the radio translating to the fast hopping characteristic of the frequency synthesizer. The standard takes into account different specifications, coding characteristics, and modulation parameters for different data rates from 55 Mb/s to 480 Mb/s, which are meant to support transmission distances from 10m to 2m, respectively. The details of the standard specifications can be found in [12].

CHAPTER III

FREQUENCY SYNTHESIS FOR MULTIBAND OFDM UWB RADIOS*

3.1. Introduction

As was discussed in Chapter II, in the MB-OFDM proposal [11] the 7500 MHz UWB spectrum is divided into 14 bands of 528 MHz each. These bands are grouped into 5 band groups as shown in Fig. 3.1. Only the first band group, corresponding to the lower part of the spectrum (3.1-4.8 GHz), is considered as mandatory by the current standard proposal [13]. Current efforts from semiconductor companies for the implementation of UWB devices focus on the first band group to achieve a faster time-to-market and affordable power consumption with CMOS [14] and BiCMOS [15] technologies. The realization of UWB radios for operation in the entire 3.1-10.6 GHz range is an open research area, which leads to various design challenges at both the system and circuit levels.

Fig. 3.2 illustrates the role of a UWB frequency synthesizer in a MB-OFDM direct conversion transceiver. As in other wireless systems, the frequency synthesizer has the crucial function of generating the local oscillator (LO) signal that drives the down-converter in the receiver path and the up-converter in the transmitter. There are at least two demanding requirements that make a frequency synthesizer for a MB-OFDM UWB radio significantly different from the widely explored synthesizers for narrowband

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*Part of this chapter is reprinted with permission from C. Mishra et. al., "Frequency planning and synthesizer architectures for multiband OFDM UWB radios", *IEEE Trans. on Microwave Theory and Tech.,* vol. 53, no. 12, pp. 3744-3756, Dec. 2005.

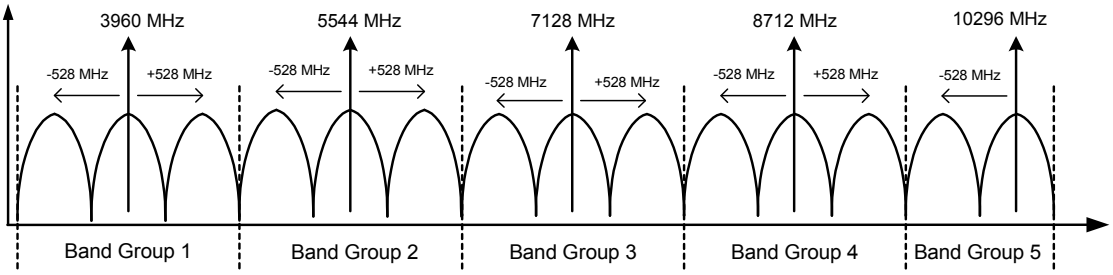

Fig. 3.1 Frequency band plan according to MB-OFDM proposal.

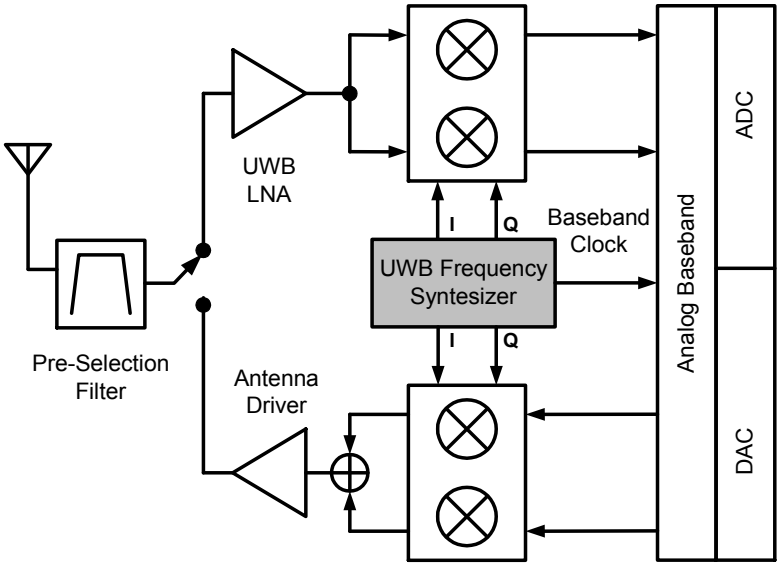

Fig. 3.2 Frequency synthesizer in a UWB radio. (© [2005] IEEE)

wireless systems: (i) The range of frequencies to be generated spans several GHz. For better appreciation, tuning range requirement for UWB synthesizers as compared to other conventional synthesizers for narrowband wireless applications is presented in Table 3.1. (ii) The time to switch between different band frequencies within a band group should be less than 9.47 ns as was explained in Chapter II. This requirement

prevents the use of a standard phase-locked loop (PLL) based synthesizer for this application as it translates to a large loop bandwidth (>20 MHz) requirement [16].

Table 3.1 Synthesizer tuning range requirement for various wireless standards

Wireless Standard	Frequency Band (MHz)	Tuning Range (MHz)
Bluetooth	2400 - 2480	80 MHz (3.28%)
802.11a	5180 – 5805	625 MHz (11.38%)
802.11b	2412 - 2472	60 MHz (2.46%)
802.11g	2412 - 2472	60 MHz (2.46%)
UWB	3100 - 10600	7.5 GHz (109.5%)

3.2 Frequency Planning and Synthesizer Architectures

Some possible ways of performing the frequency generation in a UWB radio are discussed in [16]. Some of the existing implementations are described in the next section. It must be mentioned here that these implementations are described here for the sake of completeness. The designs presented in Chapter IV were designed either before or at the time of publication of the following implementations.

3.2.1 Existing Implementations

The most obvious solution for a multiband UWB system is to have multiple frequency sources (VCO/PLL), one each for every band frequency. The synthesizer presented in [17] generates 4, 5, 6 and 7 GHz tones using a PLL for each frequency. [14] follows a similar approach by having three fixed-modulus PLLs, one for each of the three frequencies in band group 1. Such solutions are not very practical in terms of size

and power especially for the entire UWB band as this would imply 14 PLLs on the same chip.

[18] uses two PLLs (to generate 3960 MHz and 528 MHz) and a single sideband mixer to span the frequencies in band group 1. In [19] again two PLLs are used but this time in a different fashion to generate 7 bands from 3-8 GHz. [20] uses two frequency sources (implying two PLLs) and external inputs that are not generated within the system. It generates 8 tones from 3.25-6.75 GHz, with a spacing of 500 MHz between each tone. A more practical strategy however, is to generate one frequency with a PLL and indirectly generate the other frequencies from auxiliary signals generated in parallel [16]. This technique is used in [13], [21] and [22]. From here onwards, the term auxiliary signals or tones would refer to signals that are generated within the division loop of the PLL. [21] presents a synthesizer for band group 1 based on a divide by 7.5 structure (which uses standard dividers and single sideband mixers); both the reference tone (3960 MHz) and a 528 MHz tone for up/down conversions are generated using a single PLL. The synthesizer used in [22] is based on a 16 GHz quadrature VCO, 8 divide by 2 structures, 2 SSB mixers and 2 multiplexers to generate 7 bands from 3.1-8.2 GHz. The diverse characteristics of the UWB synthesizers presented here so far is a clear sign of the challenge involved in the search for an optimum solution. Moreover, none of these architectures span the entire UWB spectrum licensed by the FCC and considered by the MB-OFDM proposal. Significant work must be performed first at the system level to develop an efficient synthesizer solution (in terms of performance and power consumption) for the requirements of a completely integrated MB-OFDM UWB radio.

3.2.2 Frequency Planning

The frequency band plan introduced in [11] is shown in Fig. 3.1. Each band in any band group is 528 MHz away from its adjacent band. Each band's center frequency is given by:

$$f_C = (2904 + 528 \times n) MHz \tag{3.1}$$

where n = 1, 2, 3 (band number). The main objective of frequency planning is to maximize the number of usable bands in the available spectrum while keeping the architecture of the frequency synthesizer simple, compact and power efficient. As mentioned earlier, generating each band frequency using a single PLL is impractical due to the very fast switching time requirement. The MB-OFDM standard proposal [11] considers that when two UWB devices communicate they do so using the three (or two) adjacent frequencies of a band group. This implies that the synthesizer needs to hop very fast only between the frequencies of a particular band group. A relatively simple solution for the synthesis of these frequencies is to generate a reference tone (the center frequency in a band group except band group #5 as shown in Fig. 3.1) for each band group and the adjacent frequencies through an up or down-conversion by 528 MHz. A reference tone in a band group is that tone from which the required adjacent frequencies are derived.

From the above discussion it is clear that for the generation of any band frequency in any band group the 528 MHz tone always needs to be available apart from the reference frequency of that band group. A very practical approach involves a PLL based architecture where the output frequency of the PLL is fixed and the reference

tones in the different band groups and the 528 MHz tone are generated (either directly or indirectly) from the auxiliary frequencies (frequencies generated in the process of deriving the PLL reference frequency from the VCO output). The auxiliary frequencies in a PLL will depend on the division ratio and the dividers used in its implementation. In order to have maximum possible auxiliary frequencies that could be derived from a fixed VCO frequency the division ratio should be implemented with small divisors such as 2 and 3. With the assumption that a divide by 2 and a divide by 3 serve as the basic cells in the division loop of a PLL, a frequency tree diagram can be generated as depicted in Fig. 3.3. This diagram shows the different possible VCO frequencies that can result in a 528 MHz tone by successive division by 2, 3 or both. The tree also shows the different auxiliary frequencies generated in the PLL during the process of generation of the 528 MHz tone. In this way, separate synthesis of 528 MHz is avoided. The reference frequency of the PLL could be further derived from the 528 MHz. Fig. 3.3 provides various choices for the VCO frequency (shown in bold ellipses). In order to reduce the number of components and simplify the architecture, the VCO frequency should be chosen such that most of the auxiliary frequencies are same as the reference tones. Based on Fig. 3.3 a band plan and a set of auxiliary frequencies can be defined to obtain an efficient synthesizer architecture.

A different but not less important factor to consider in the choice of the frequencies to be used by the MB-OFDM UWB radio is the overlap between the U-NII band from 5.15-5.825 GHz and the UWB spectrum. The interference from WLAN radios using the IEEE 802.11a standard are of particular concern due to their widespread

use. In [11] it is estimated that an attenuation of 30 dB in the 5.15-5.825 GHz spectrum is required from a front-end filter to tolerate the presence of a 802.11a transmitter at a distance of 0.2 m. Due to the nature of their target applications, MB-OFDM and 802.11a radios will coexist in most environments preventing the effective use of a band group that overlaps with the U-NII band. For these reasons, the synthesizer architectures described in the following sections do not consider a band group in the range of 5.15-5.825 GHz. This implies that 11 is the maximum number of frequencies that need to be generated in a practical MB-OFDM UWB radio.

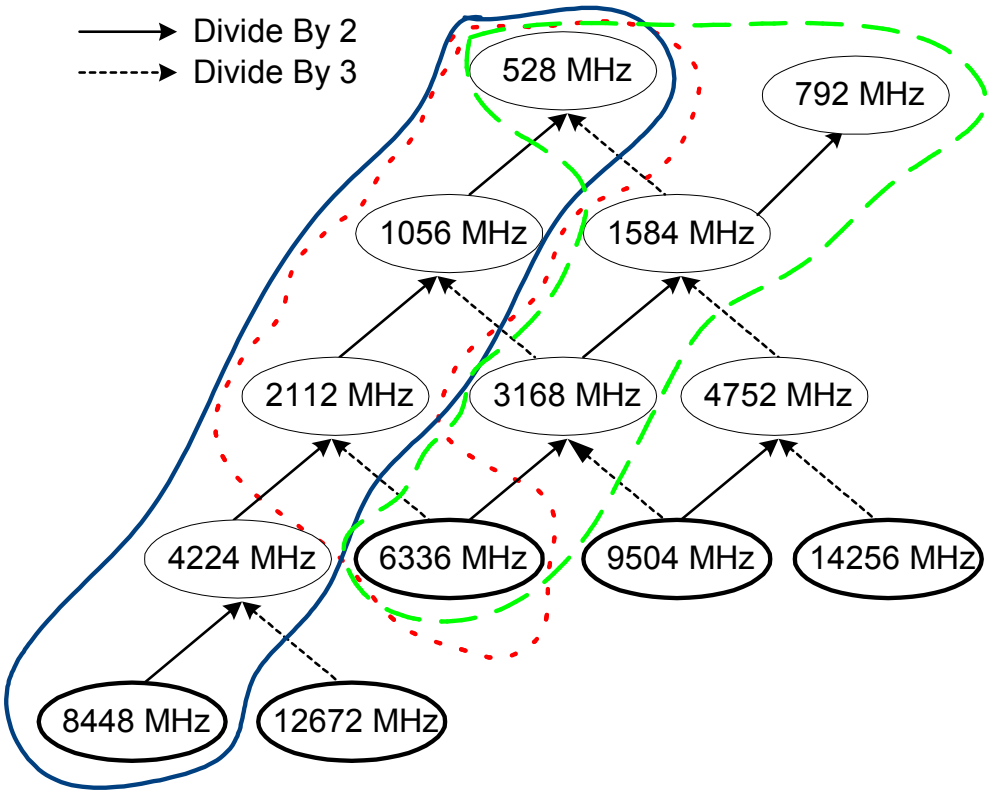

Fig. 3.3 Frequency tree diagram for choosing VCO frequency. (© [2005] IEEE)

3.2.3. Synthesizer Architecture for Band Plan Based on MB-OFDM Proposal

The frequency tree diagram in Fig. 3.3 is useful to define the architecture for the frequency synthesizer; each VCO frequency results in different auxiliary frequencies and choices for the architecture. Based on this analysis, an efficient synthesizer architecture for the existing band plan is presented in this section. The architecture presented in [23] for the generation of 7 frequencies (between 3.432-7.920 GHz while avoiding U-NII bands) is based on a PLL that generates a tone at 6336 MHz, and is considered as a starting point for the discussion. Choosing the VCO frequency as 6336 MHz and following the path enclosed by the dotted lines (Fig. 3.3) a possible architecture for the current band plan can be defined as shown in Fig. 3.4. In contrast to the architecture in [22] this architecture generates 11 frequencies. The shaded italicized frequencies in Fig. 3.4 correspond to the reference tones for the current band plan shown in Fig. 3.1. It is important to note that the switching time between bands within a given band group depends only on the switching of the final multiplexer. This feature is common to all other architectures present in this dissertation.

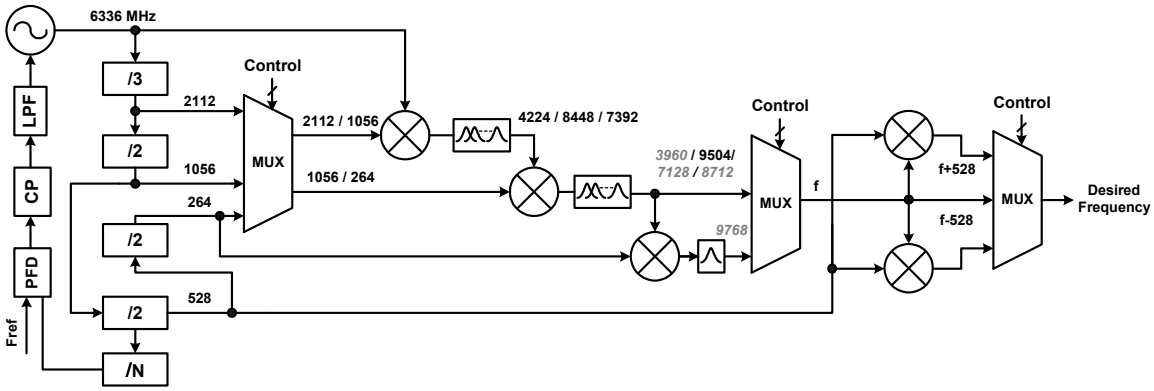

Fig. 3.4 Synthesizer architecture (I) based on MB-OFDM proposal. (© [2005] IEEE)

In this architecture option, the employed mixers need to be single sideband (SSB) and broadband since they cannot be optimized for a single input or output frequency. In addition, intermediate filtering stages are required to maintain the spectral purity of the signals, which undergo a series of up/down conversions for the generation of a particular frequency. As shown in Fig. 3.4 one option would be to have band pass filters at the output of such mixers, either dedicated or tunable over a wide range of frequencies. This would involve a significant amount of passives, which would increase the required area. Due to the high frequency and wide band nature of the components involved, the power consumption of this synthesizer implementation may also become a major portion of the entire transceiver power. Hence, to obtain a suitable performance from this solution would be at the cost of significant area and power. A strategy to reduce the power and complexity in the frequency synthesizer is to identify auxiliary frequencies that can be used to generate most of the reference tones with few or no frequency translation operations. From the frequency tree diagram it can be found that following the path enclosed within the dashed shaded line two of the frequencies i.e. 6336 MHz and 3168 MHz are equally spaced (792 MHz) from their reference tones as shown in Fig. 3.1. Therefore having these frequencies at hand, one stage of mixing could be avoided in the generation of the reference tones. Based on these auxiliary frequencies, Table 3.2 shows the proposed synthesis of the reference tones for the current band plan.

A compact frequency synthesizer architecture is proposed based on the frequency synthesis described in Table 3.2 and is shown in Fig. 3.5. From Table 3.2 it can be seen that the architecture (I) was modified such that all the reference tone generations involve

Table 3.2 Synthesis of frequencies for current band plan f_o = 6.336 GHz

Band #	f_o (MHz)	Frequency Synthesis
1	3432	$f_o/2 + f_o/8 - f_o/12$
2	3960	$f_o/2 + f_o/8$
3	4488	$f_o/2 + f_o/8 + f_o/12$
4	6600	$f_o + f_o/8 - f_o/12$
5	7128	$f_o + f_o/8$
6	7656	$f_o + f_o/8 + f_o/12$
7	8184	$f_o + f_o/4 + f_o/8 - f_o/12$
8	8712	$f_o + f_o/4 + f_o/8$
9	9240	$f_o + f_o/4 + f_o/8 + f_o/12$
10	9768	$f_o + f_o/2 + f_o/8 - f_o/12$
11	10296	$f_o + f_o/2 + f_o/8$

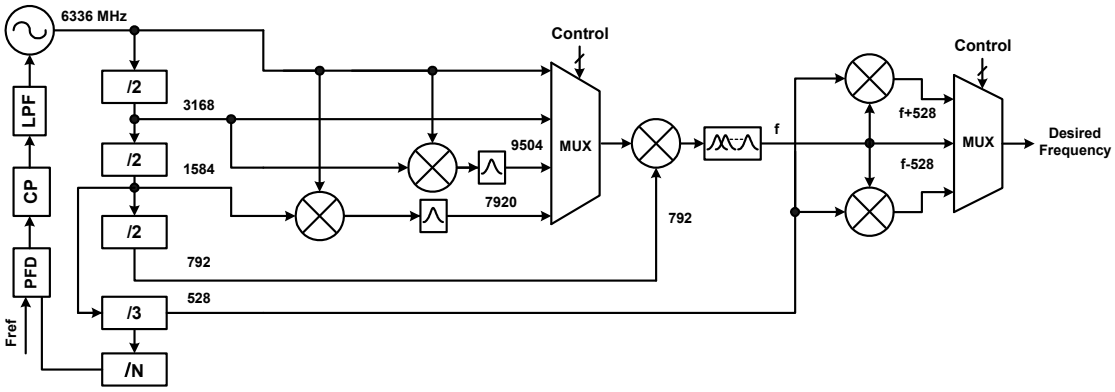

Fig. 3.5 Synthesizer architecture (II) based on MB-OFDM proposal. (© [2005] IEEE)

a final up conversion by a 792 MHz tone, which is the $f_o/8$ term in the frequency synthesis column for all frequencies. It is important to mention that the reference tone in

band group 5 has changed from 9768 MHz in architecture (I) to 10296 MHz in architecture (II). A significant reduction in power and area is expected due to the reduced number of mixers with multiple frequency output. However, this architecture still needs a broadband SSB up converter for the generation of all the reference tones (up conversion with 792 MHz).

Harmonics can be curtailed by low pass filtering at different stages, but suppressing the unwanted sidebands demands additional filtering (band pass or band notch) for the different intermediate frequencies generated in the synthesizer. In the above architecture this would imply a wide tuning range band-pass (or notch) filter to cater to the wide range of intermediate frequencies (IF) generated (especially after the up conversion with 792 MHz) apart from the dedicated filtering wherever required (see Fig. 3.5). One possibility is to have dedicated SSB mixer blocks and filtering for generation of each reference tones, but that would be at the expense of higher power consumption. It must be mentioned here that the last two mixers used to generate the bands adjacent to the reference frequency (up/down conversion by 528 MHz) also have a multiple frequency input and output and would have to be broadband. However, this structure with two mixers and one multiplexer at the end of the frequency synthesizer is common to all of the architectures presented in this work. Since filtering at the final stage would demand a broadband tunable filter spanning several GHz it is not practical and is hence not employed at the output of the last mixers in any of the architectures. Hence, the aim is to have the reference frequency as spectrally pure as possible before the final up/down conversion. Therefore, an important consideration is to minimize the number of up/down

conversion operations in the generation of any reference frequency to reduce the spurs within the UWB spectrum. The above discussion highlights some of the most important considerations for the design of a frequency synthesizer in an UWB system.

3.2.4 Proposed Band Plan and Synthesizer Architecture

From the frequency tree diagram in Fig. 3.3, it can be noted that different sets of auxiliary frequencies can be generated in the PLL. In order to further reduce the number of multiple frequency output SSB mixers and avoid reconfigurable filtering schemes, a branch in the frequency tree can be selected such that most of the reference tones are directly generated in the divider chain (path from the selected VCO frequency to the 528 MHz tone). Looking carefully it can be found that by moving the first three bands in band group 1 by 264 MHz to the higher side of the frequency spectrum and moving the band groups 3, 4 and 5 by 264 MHz to the lower side of the spectrum (as shown with gray arrows in Fig. 3.6), two of the reference tones (8448 MHz and 4224 MHz) are generated in the divider chain of the PLL which completely eliminates the need of any multiple frequency output mixer for the generation of any reference frequency [24]. The corresponding set of auxiliary frequencies for the modified band plan is enclosed with a solid line in the frequency tree of Fig. 3.3. It is important to mention that this proposed modification in the band plan overlaps with the radio astronomy bands in Japan, however, it does not introduce any overlap with the U-NII band in the United States.

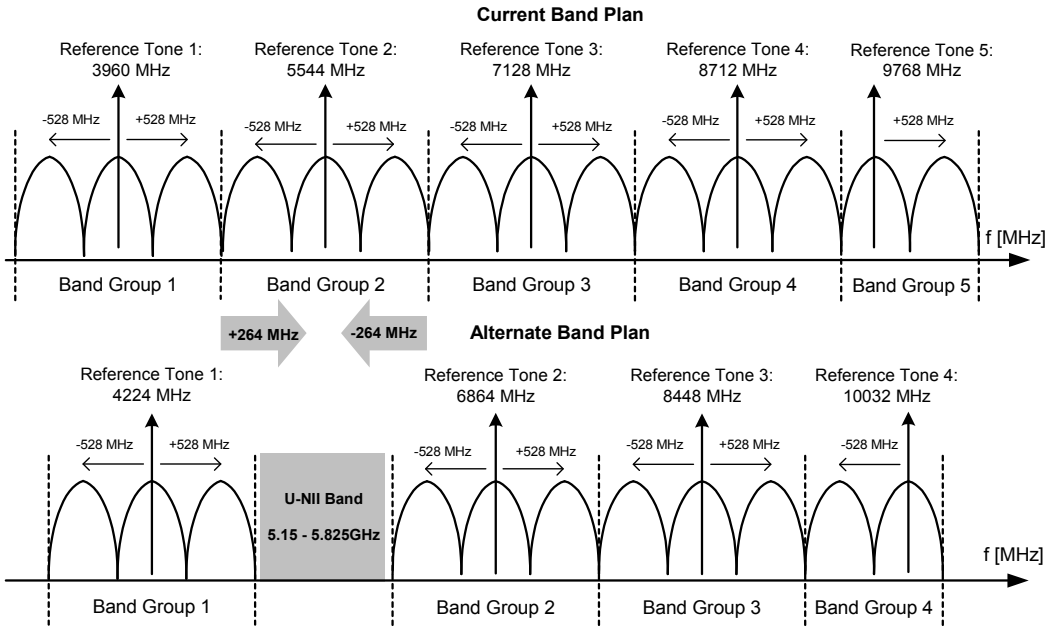

Fig. 3.6 Current band plan from MB-OFDM proposal and proposed band plan. (© [2005] IEEE)

Table 3.3 Synthesis of frequencies for proposed band plan with $f_o = 8.448$ GHz

Band #	f_o (MHz)	Frequency Synthesis
1	3696	$f_o/2 - f_o/16$
2	4224	$f_o/2$
3	4752	$f_o/2 + f_o/16$
4	6336	$f_o - f_o/8 - f_o/16 - f_o/16$
5	6864	$f_o - f_o/8 - f_o/16$
6	7392	$f_o - f_o/8 - f_o/16 + f_o/16$
7	7920	$f_o - f_o/16$
8	8448	f_o
9	8976	$f_o + f_o/16$
10	9504	$f_o + f_o/8 + f_o/16 - f_o/16$
11	10032	$f_o + f_o/8 + f_o/16$

Based on the frequency generation table (Table 3.3), a modified architecture (synthesizer architecture (III)) is proposed [24] as shown in Fig. 3.7. This architecture employs dedicated SSB mixers since each of them generates only one frequency. The most significant advantage of this architecture is that dedicated filtering can be employed at every stage wherever required to obtain a clean spectrum, thereby eliminating the need of reconfigurable filtering schemes. The generation of two reference tones within the divider chain also helps in reducing the complexity. As it will be shown in the later sections, the spurs in this architecture are diminished because of the reduced number of up/down conversions involved in the generation of the reference frequencies. In general, for a MB-OFDM UWB system, a frequency synthesizer architecture, which minimizes the number of up/down conversions, would be preferred.

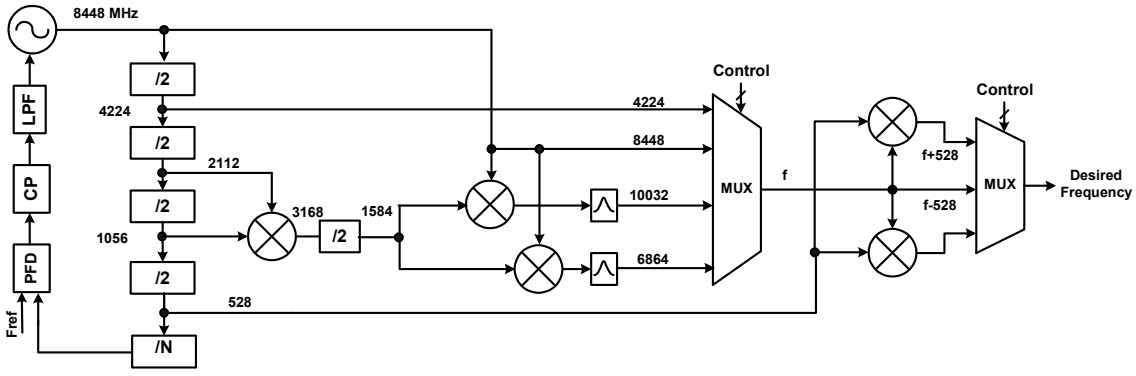

Fig. 3.7 Synthesizer architecture (III) based on proposed band plan. (© [2005] IEEE)

3.3 Synthesizer Specifications

In addition to generating all the carrier frequencies efficiently and guaranteeing fast hopping in a band group, the LO signal must comply with other requirements to

ensure proper operation of the MB-OFDM UWB radio. The specifications outlined in this section assume the OFDM parameters and BER requirements described in [11] for a 480Mb/s data transmission and an additive white Gaussian noise (AWGN) channel. A quadrature phase-shift keying (QPSK) constellation is considered for the individual sub-carriers. For a packet error rate of 8% with a 1024 byte packet, the target BER when using a coding rate R=3/4 is 10^{-5}, which corresponds to an un-coded BER of approximately 10^{-2}. Although, current UWB systems employ QPSK constellation of the baseband data to achieve a peak raw data rate of 640 Mb/s, however, in order to maximize the usage of the available 528 MHz bandwidth, future systems will use modulation schemes such as 16-QAM to achieve peak raw data rates beyond 1 Gb/s [25]. A direct implication is an increased system signal to noise ratio (SNR) at the demodulator to maintain similar bit error rate (BER) as QPSK and better phase noise requirement from the local oscillator (LO).

3.3.1 Phase Noise

The phase noise from the local oscillator in an OFDM receiver has two different effects on the received symbols. It introduces a phase rotation of the same magnitude in all of the sub-carriers and creates inter-carrier interference (ICI) [26]. The first undesired effect is eliminated by introducing pilot carriers with a known phase, in addition to the information carriers. On the other hand, phase noise produces ICI in a similar way as adjacent-channel interference in narrow band systems. Assuming that the data symbols on the different sub-carriers are independent, the ICI may be treated as Gaussian noise.

The power spectral density (PSD) of a locked PLL can be modeled by a Lorenzian spectrum described by:

$$\left|\Phi(f)\right|^2 = \frac{1}{\pi} \cdot \frac{\beta}{f^2 + \beta^2} \tag{3.2}$$

where β is the 3 dB bandwidth of the PSD, which has a normalized total power of 0 dB.

The degradation (D in dB) in the signal-to-noise ratio (SNR) of the received sub-carriers due to the phase noise of the local oscillator in an OFDM system can be approximated as [27]:

$$D \cong \frac{11}{6\ln 10} \cdot 4\pi \cdot \beta \cdot T \cdot \frac{E_s}{N_o} \tag{3.3}$$

where T is the OFDM symbol length in seconds (without the cyclic extension), β defines the Lorenzian spectrum described above and Es/No is the desired SNR for the received symbols (in a linear scale, not in dB). For this system, 1/T=4.1254 MHz and the Es/No for the target coded BER of 10^{-5} is 5.89 (7.7 dB). For D=0.1 dB and the mentioned parameters, β can be computed with (3.3) and is 7.7 KHz. The corresponding Lorenzian spectrum has a power of –86.5 dBc/Hz @ 1 MHz. Changing the modulation scheme from QPSK to 16-QAM implies an increase in SNR by 4dB for the same BER, without increase in bandwidth. This translates to a value of β equal to 2.787 KHz. Knowing β for both the constellations (QPSK and 16-QAM) we can plot equation (3.3) as shown in Fig. 3.8. From this figure it is evident that the phase noise requirement of the LO signal does not change drastically (from -86.5 dBc/Hz @ 1MHz to -90.6 dBc/Hz @ 1MHz). If the phase noise of the LO signal is better than -91dBc/Hz @ 1MHz then the synthesizer can

meet the phase noise requirements for both the current and future systems. However, this phase noise specification is not necessarily the phase noise specification of the frequency source (VCO/PLL) from which the LO signal is derived. To derive the phase noise specification of the LO source we need to evaluate the phase noise degradation due to the other components (such as mixers and dividers) used in generating the LO signal. To derive this number the knowledge of the architecture of the frequency synthesizer is very critical.

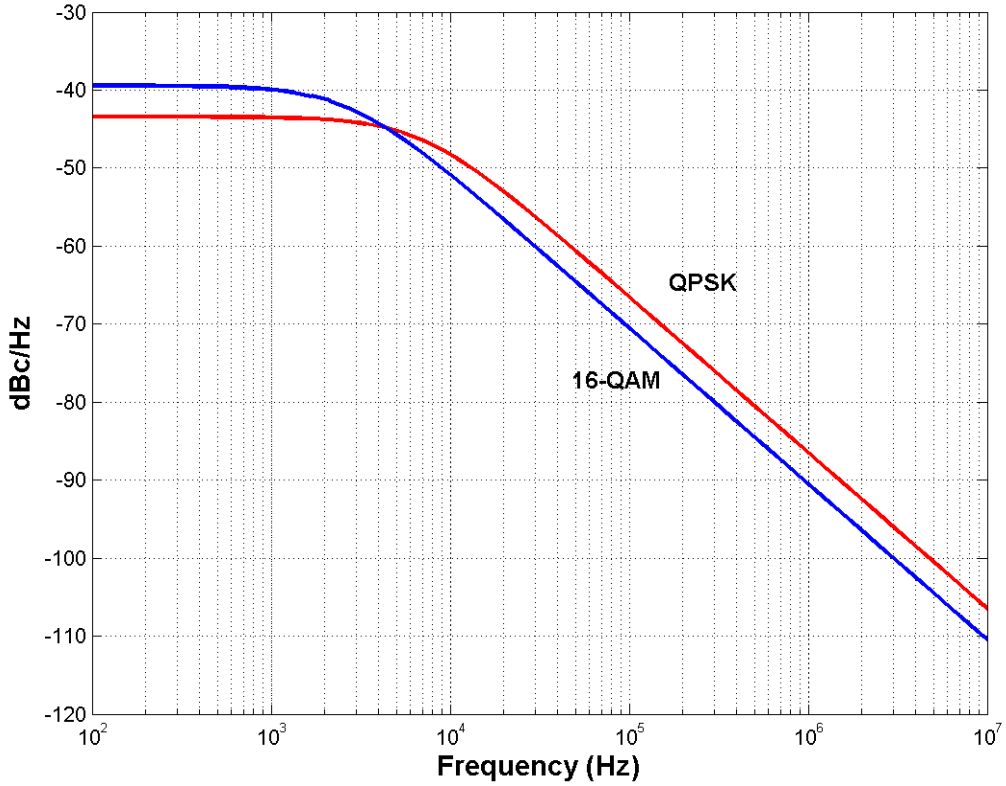

Fig. 3.8 PSD of a locked PLL modeled as a Lorenzian spectrum.

General guidelines for the analysis of phase noise in component cascades are provided in [28]. For this application, the most relevant components for phase noise degradation are the mixers employed in the frequency translation operations across the synthesizer architecture. For a given offset frequency Δf , the phase noise at the output of a mixer can be estimated as the rms sum of the individual input noise contributions. Hence, given phase noise relative power densities $L_1\{\Delta f\}$ and $L_2\{\Delta f\}$ (in dBc/Hz) at the input of each port of the mixer, the output phase noise can be expressed as:

$$L\{\Delta f\} = 10 \cdot \log\left(10^{\left(\frac{L_1\{\Delta f\}}{10}\right)} + 10^{\left(\frac{L_2\{\Delta f\}}{10}\right)}\right) \tag{3.4}$$

Even though in this case the two signals are indirectly derived from the same reference, their noise can be assumed in general to be uncorrelated since the delay from the PLL to each input of a given mixer would be significantly different. The size of an integrated implementation would be small in comparison to the wavelengths involved but the frequency dividers and the poles in the signal path introduce a delay. As it can be noted from Figs. 3.5 and 3.6, there is at least 1 frequency divider between the inputs of each mixer. The gain or loss of the mixer amplifies or attenuates all of the frequency components around the frequency of operation by the same amount and hence does not affect the phase noise. Moreover, due to the relatively large amplitude (tens of mV) of the signals within the synthesizer, the contribution of the thermal noise of the mixers to the phase noise is negligible. For a given UWB synthesizer architecture, the path with the largest number of frequency translations can be analyzed with the use of (3.4) to find the phase noise specification for the source PLL.

Fig. 3.9 shows the best and worst case overall phase noise of the LO signal for different band groups, based on the PLL phase noise and the phase noise enhancement/degradation due to the dividers and mixers in the LO path. The dashed lines represent the worst-case phase noise that assumes no phase noise improvement due to successive divisions and the solid lines represent the best case assuming a 6 dB improvement for every division by 2. Band group # 4 will follow a similar trend as band group # 2, however, it might degrade due to its higher frequency of operation. Fig. 3.9 also plots the desired specification for the phase noise of the LO signal indicating that in a VCO/PLL with phase noise better than -97 dBc/Hz @ 1 MHz can meet worst case phase noise requirement for all bands.

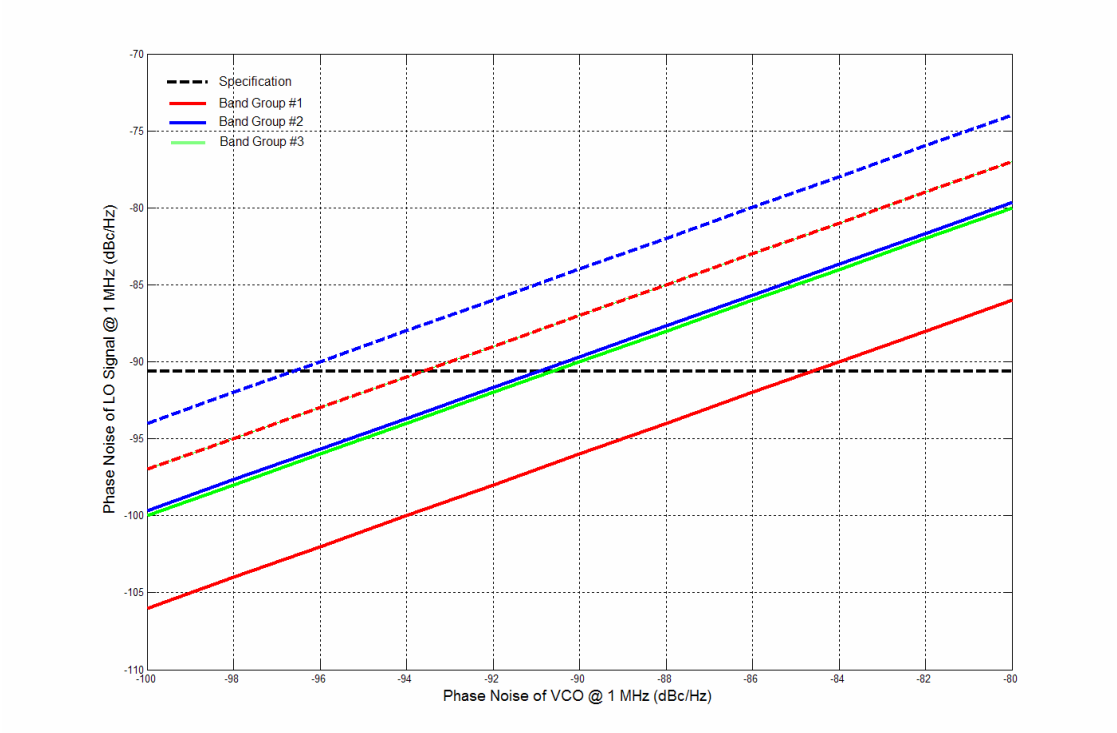

Fig. 3.9 Phase noise of the LO signal with respect to phase noise of LO source.

3.3.2 Spurious Tones

As in other communication systems, the most harmful spurious components of a LO signal are those at an offset equal to multiples of the frequency spacing between adjacent bands (528 MHz in this case), since they directly down-convert the transmission of a peer device on top of the signal of interest as shown in Fig. 3.10. In order to gain understanding on the impact of unwanted tones from the synthesizer, the effect of an uncorrelated down-converted peer interferer on the bit error rate (BER) performance of a MB-OFDM UWB receiver is evaluated through a baseband equivalent model in SystemView [29]. A conceptual description of the model is shown in Fig. 3.11. As shown with gray blocks in Fig. 3.11, in the SystemView model the down-converted interferer is implemented with an independent random bit stream and an OFDM modulator with QAM constellation. Before adding it to the signal of interest, each interferer is scaled by a factor *k*, which represents the carrier to interference ratio at baseband. For example, if the interferer at frequency *x* is received with a power 6 dB higher than the signal of interest and the synthesizer spur at frequency *x* has a power of –26 dBc with respect to the tone of interest, then *k* corresponds to –20 dB.

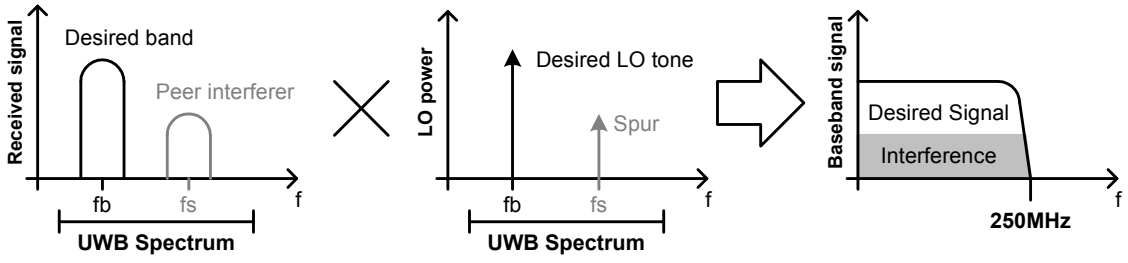

Fig. 3.10 Signal corruption at baseband due to impact of LO spurs. (© [2005] IEEE)

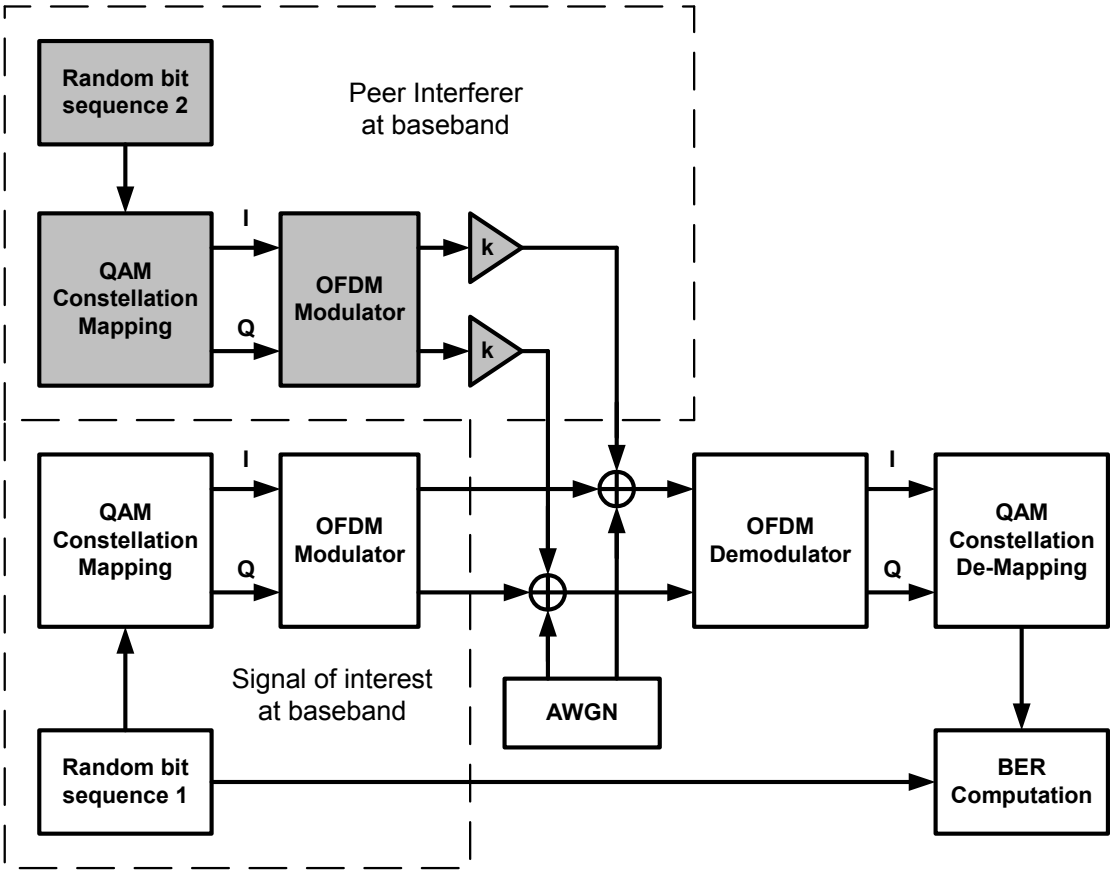

Fig. 3.11 SystemView macromodel for the evaluation of synthesizer spurs on the BER of the UWB receiver. (© [2005] IEEE)

Fig. 3.12 shows the degradation (increase) in the minimum signal to noise ratio (SNR_{min}) required at the demodulator input to meet the target BER (10^{-2}) as a function of the signal to interference ratio (SIR) or equivalently the spur level, assuming the peer interferer is at the same power level as the RF signal of interest. This degradation can also be interpreted as loss in sensitivity. For example, a spur at -20 dBc that down-converts a peer interferer at same power level as the signal of interest results in SIR of 20 dB and 1 dB degradation in SNR_{min}. Similar simulations were carried out with

uncoded 16-QAM constellation and the results plotted alongside QPSK in Fig. 3.12. For spur levels below 24dBc the SNR degradation in both cases is almost identical implying that the same synthesizer could be used in a future UWB system employing 16-QAM. It is important to mention here that, bit interleaving and forward error correction techniques employed in a complete MB-OFDM radio [11] are expected to further reduce the SNR degradation due to interference from peer UWB devices. Hence, the strategy should be to minimize spurs as much as possible without extra power, area and complexity in the implementation of the frequency synthesizer.

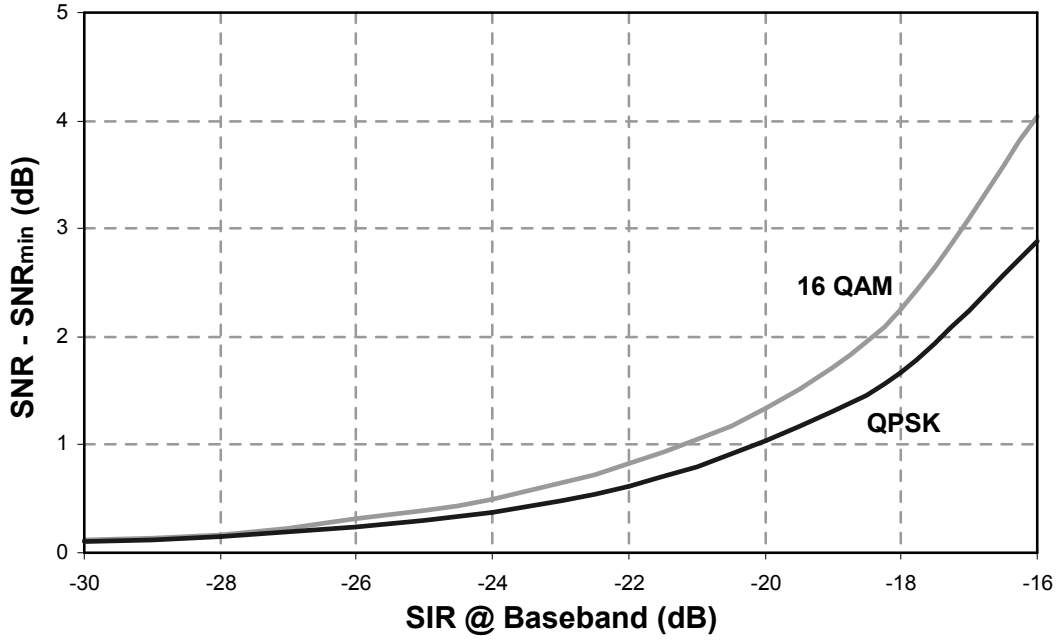

Fig. 3.12 Impact of spurs on SNR degradation.

3.3.3 I-Q Imbalance

In an OFDM system, the amplitude and phase imbalance between the *I* and *Q* channels transform the received time-domain vector **r** into a corrupted vector $\mathbf{r}_{iq}$ which

consists of a scaled version of the original vector combined with a term proportional to its complex conjugate $\mathbf{r}^*$. This transformation can be written as [30]:

$$\mathbf{r}_{iq} = \alpha \cdot \mathbf{r} + \beta \cdot \mathbf{r}^* \tag{3.5}$$

where α and β are complex constants, which depend on the amount of *I-Q* imbalance. This alteration on the received symbols can have a significant impact on the system performance. The effect of a phase mismatch in the quadrature LO signal on the BER vs. SNR performance of the receiver was evaluated considering the system characteristics outlined at the beginning of this section and using a model built in SystemView. Simulation results for un-coded data over an AWGN channel showed that the degradation in the sensitivity is 0.6 dB for 5° of mismatch. This degradation can be reduced with the use of coding and compensation techniques [30]. The LO signals generated by the frequency synthesizer drive the quadrature up/down-conversion mixer in the RF front-end. The amplitude level of the LO signal is very important especially in the RX path as it directly affects the noise figure of the mixer and hence the SNR degradation. A summary of the synthesizer specifications is provided in Table 3.4.

Table 3.4 Summary of synthesizer specifications

Band spacing	528 MHz
Switching time between adjacent bands	< 9.47 ns
Phase Noise of the LO signal	< -91 dBc/Hz @1 MHz
Aggregate power of spurs at band frequencies	< -24 dBc
Phase I/Q mismatch	< 5°

3.4 Macromodel Simulations and Performance Analysis

In order to obtain further insight on the performance of the proposed architectures (II and III), a macromodel was built in SystemView [29] for each of them. The models consist of divide by 2 or 3 blocks, SSB mixer blocks composed of active mixers, low pass filters and band pass filters at intermediate stages. Fig. 3.13 shows a block diagram of the schematic in SystemView for architecture II generating the 3960 MHz and 4488 MHz frequencies. Since not all frequencies are available at the same time a block diagram for the generation of all frequencies is not shown. The results presented in this section do not include any multiplexing. Hence, coupling and switching issues have not been considered here.

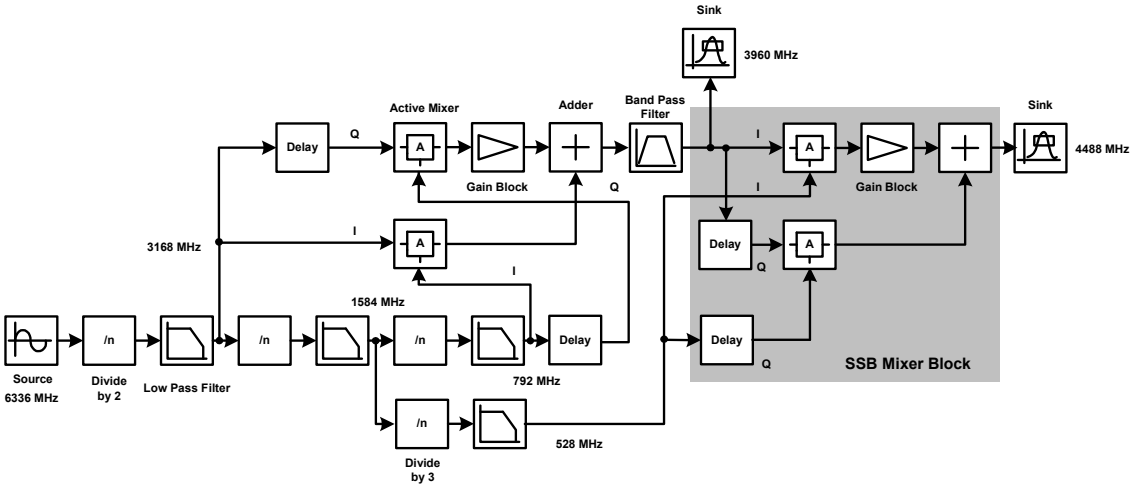

Fig. 3.13 SystemView setup for the macromodel. (© [2005] IEEE)

The SystemView model as shown in Fig. 3.13 consists of a sinusoidal source, which models the oscillator. A divide by N token of the communications library is used with N=2 or 3 for the divide by 2 or 3 implementation. The input to this token could be a

sine or square wave whereas the output is always a rectangular wave. The output of a divide by 2 circuit has significant harmonic content, which results in multiple spurious tones after subsequent mixing in the later stages of the synthesizer. This is also an issue in an integrated circuit implementation. For this reason, a first-order low pass filter is employed at the output of each divider in the macromodel to partially filter out the harmonics. To provide additional suppression for unwanted tones (harmonics, intermodulation products, leakage and sidebands) dedicated second order band pass filters are placed at the output of the SSB mixer blocks. The aim is to have as clean a signal as possible till the final up/down conversion with 528 MHz. The filters used in the macromodel are from the linear systems/filters operator group and they are of continuous time analog type. The band pass filters used in the macromodels have a quality factor (Q) of 5, which is a realistic assumption for an implementation in current deep submicron CMOS technologies.

The SSB mixers are built using two double sideband (DSB) active mixers as shown in Fig. 3.14 [31]. The active mixers are taken from the RF/Analog library. The specifications used for each of the DSB mixers that are shown in Table 3.5 are close to typical values provided in [32] and [33]. Whether the upper or lower sideband is rejected depends on the placement of the phase shifts and or the polarity of the summing block. Since a divide by 2 circuit can result in both, *I* and *Q* signals, the divider outputs can directly form the inputs to the SSB mixer. However, in the macromodel the quadrature signals of the divider are generated by adding a time delay token of the delay operator group. Finally, an analysis sink was used to capture each output frequency.

Table 3.5 Double sideband mixer specifications

Parameter	Specification
Conversion Gain	0 dB
RF Isolation	-30 dB
LO Leakage	-30 dB
Noise Figure	20 dB
IIP3	2 dBm

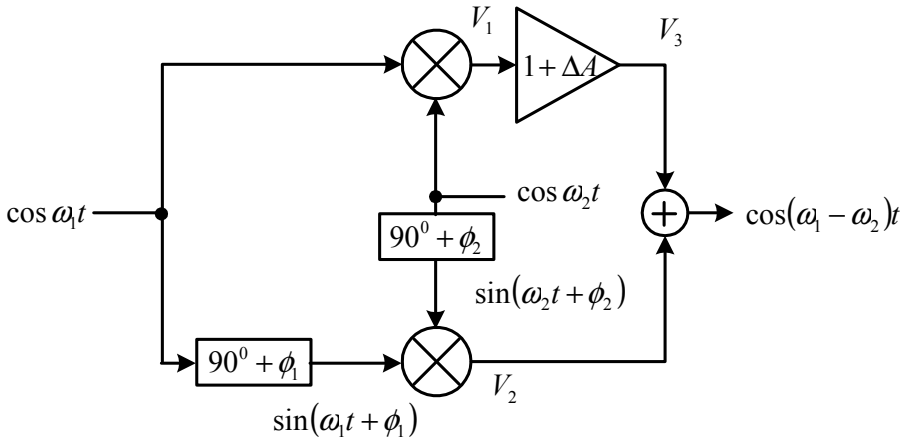

Fig. 3.14 A single sideband mixer block with phase and amplitude error. For an ideal SSB mixer $\Delta A = 0$ and $\phi_1 = \phi_2 = 0$. (© [2005] IEEE)

Perfect rejection of one of the sidebands is obtained if there is no gain and phase mismatch in the signal paths [31]. Fig. 3.14 shows the SSB mixer block with the non-idealities expected from an actual circuit implementation. The sideband rejection ratio (SBRR) in a SSB mixer with a proportional amplitude error between the two DSB mixer

outputs ΔA and phase errors ϕ_1 and ϕ_2 in each of the quadrature input signals is given by (see Appendix):

$$SBRR = 10\log\left[\frac{1+(1+\Delta A)^2+2(1+\Delta A)\cos(\phi_1-\phi_2)}{1+(1+\Delta A)^2-2(1+\Delta A)\cos(\phi_1+\phi_2)}\right] \tag{3.6}$$

A plot showing the sideband rejection versus amplitude and total phase error ($\phi_1+\phi_2$) is shown in Fig. 3.15. For a particular case of $\Delta A = 0.05\,(5\%)$ and $\phi_1 = \phi_2 = 5^o$ (equal to a total phase error of 10^0), the sideband rejection is 20.86 dB.

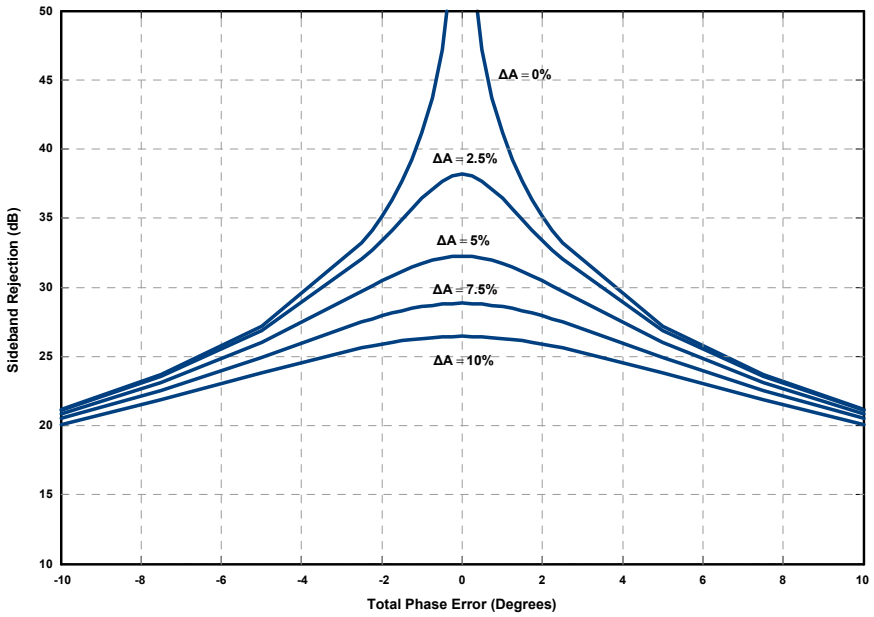

Fig. 3.15 Sideband rejection with amplitude and phase error. (© [2005] IEEE)

Simulations are performed for architectures II and III with the component models described above but assuming no phase or amplitude mismatch in the SSB mixer blocks or any shift in frequencies in the intermediate filters. In that case, for the generation of all the required tones in both architectures the level of each spur is at least 26 dB below

the desired frequency. This could be tolerated according to the specifications outlined in section 3.3.2. An analysis of these macromodel simulation results reveals that the most significant spurs are due to the finite LO leakage to the IF port since, under no amplitude or phase mismatch, the image rejection of the SSB mixer is very high. The isolation between these ports can be improved by proper circuit and layout design techniques. It must be mentioned here that the LO leakage in the macromodel is implemented by a feed forward path from the LO port adding at the output via a gain stage (with attenuation) and not through the LO leakage parameter of the model.

Table 3.6 Spurs associated with each band frequency for synthesizer architecture (II) with non-idealities

Band (MHz)	Generated spurs: Power in dB below the tone of interest (Spur frequency in MHz)							
3432	20.8 (4488)	21.3 (5544)	24.7 (3960)	29.8 (2640)	30.3 (4224)	31.5 (528)	31.9 (10296)	-
3960	24.3 (3168)	-	-	-	-	-	-	-
4488	20.8 (3432)	21.3 (2376)	24.6 (3960)	29.8 (3696)	30.6 (10560)	31.2 (5280)	31.5 (528)	-
6600	21.3 (7656)	21.3 (8712)	24.8 (7128)	25.4 (5808)	26.7 (7392)	30.2 (5016)	30.8 (8184)	31.5 (528)
7128	19.8 (6336)	24.8 (5544)	-	-	-	-	-	-
7656	21.3 (6600)	21.4 (5544)	24.8 (7128)	25.3 (6864)	26.8 (8448)	28 (6072)	-	31.5 (528)
8184	20.4 (9240)	21.3 (10296)	24.7 (8712)	25.6 (7392)	27.2 (8976)	27.9 (6600)	27.5 (9768)	31.5 (528)
8712	19.9 (7920)	23 (7128)	34 (5544)	-	-	-	-	-
9240	20.4 (8184)	21.3 (7128)	24.9 (8712)	25.6 (8448)	27.4 (7656)	27.1 (10032)	31.5 (528)	-
9768	23 (8184)	24.3 (10296)	25.5 (8976)	28 (10560)	31.5 (528)	-	-	-
10296	17.7 (8712)	20 (9504)	29 (7128)	-	-	-	-	-

Next, simulations are performed for a worst-case scenario with several non-idealities incorporated in the macromodels. These include I-Q phase mismatch (5^{o}) in all quadrature paths, amplitude mismatch (5%) between the two signal paths in the SSB mixer blocks (see Fig. 3.14) and a frequency deviation of 10% in the center frequency of the band pass filters. These are the most important non-idealities expected from an integrated implementation. Even though circuit implementations of frequency dividers are known to yield accurate quadrature outputs, signal routing effects such as crosstalk, loading, mismatch of parasitic components, etc. become relevant at GHz frequencies. For this reason, the effect of amplitude and phase mismatch for the signals across the synthesizer must be taken into account. The amplitude and phase mismatches are introduced in the macromodel by changing the gain factor of the gain block and changing the value in the delay token respectively. It is also important to mention that the deviation considered for the center frequency in each of the bandpass filters is in a way that they enhance a spur while attenuating the fundamental tone. For example the bandpass filter centered at 3960 MHz (Fig. 3.13) is shifted by 10% to lower frequencies, that is, towards that of the alternate sideband frequency.

Tables 3.6 and 3.7 show the spurious tones produced during the synthesis of each of the 11 frequencies for architectures (II) and (III) respectively in the above described worst-case conditions. Since in architecture (III) the 8448 MHz tone is the oscillator output and the 4224 MHz tone is generated by a divide-by-2, these tones do not create any spurious tones in the spectrum of interest and hence no spurs are shown for them in Table 3.7. It must be stressed here that because of the intermediate band pass filters used

in both the architectures, not many spurs appear in the generation of the reference tones. Fig. 3.16 and 3.17 show the output spectrum of synthesizer architecture (II) and (III) respectively for the generation of one particular frequency. The spectrum is normalized with respect to the power of the frequency tone of interest. Fig. 3.16 shows the generation of the 8184 MHz tone by architecture (II). The most prominent spurious tones are at 9240 MHz, 10296 MHz, 8712 MHz and 7392 MHz. Likewise, Fig. 3.17 shows the generation of 9504 MHz tone by architecture (III), the most significant spurious tones being 10560 MHz, 10032 MHz and 7920 MHz.

Table 3.7 Spurs associated with each band frequency for synthesizer architecture (III) with non-idealities

Band (MHz)	Generated spurs: Power in dB below the tone of interest (Frequency in MHz)				
3696	20.6 (4752)	24.75 (4224)	27.9 (5808)	32.4 (528)	-
4224	-	-	-	-	-
4752	20.6 (3696)	24.75 (4224)	27.9 (2640)	32.4 (528)	-
6336	19.4 (7392)	25.5 (6864)	28 (7920)	28.3 (8448)	31.5 (528)
6864	27 (8448)	37 (10032)	-	-	-
7392	19.8 (6336)	25.5 (6864)	28 (5280)	28.5 (5808)	31.5 (528)
7920	20.6 (8976)	24.6 (8448)	27.9 (10032)	31.7 (528)	-
8448	-	-	-	-	-
8976	20.6 (7920)	24.6 (8448)	27.9 (6864)	31.7 (528)	-
9504	20 (10560)	26 (10032)	26.5 (7920)	31.5 (528)	-
10032	21.3 (8448)	34 (6864)	-	-	-

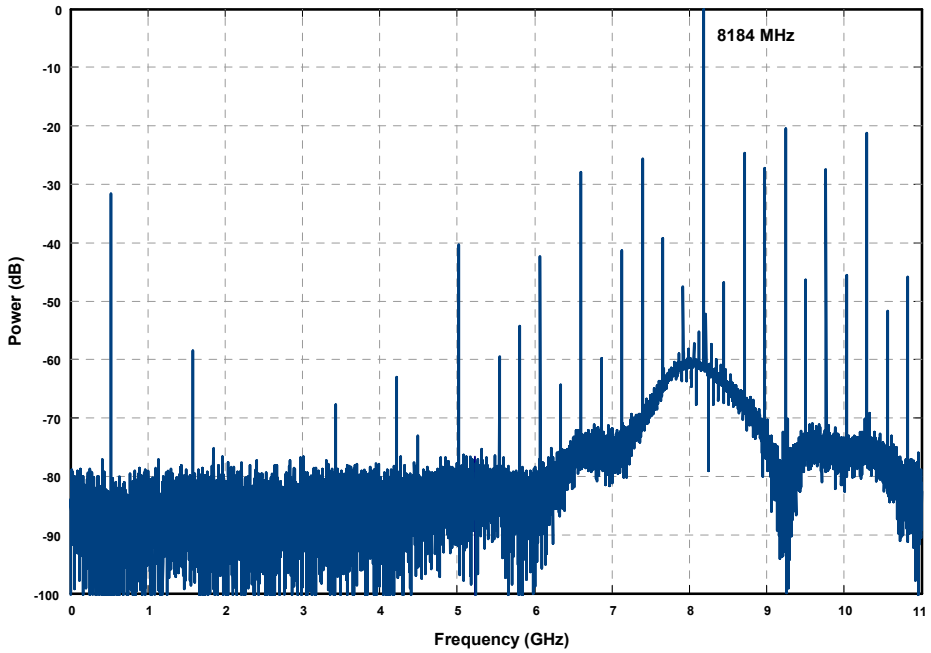

Fig. 3.16 Output spectrum for synthesizer architecture (II). (© [2005] IEEE)

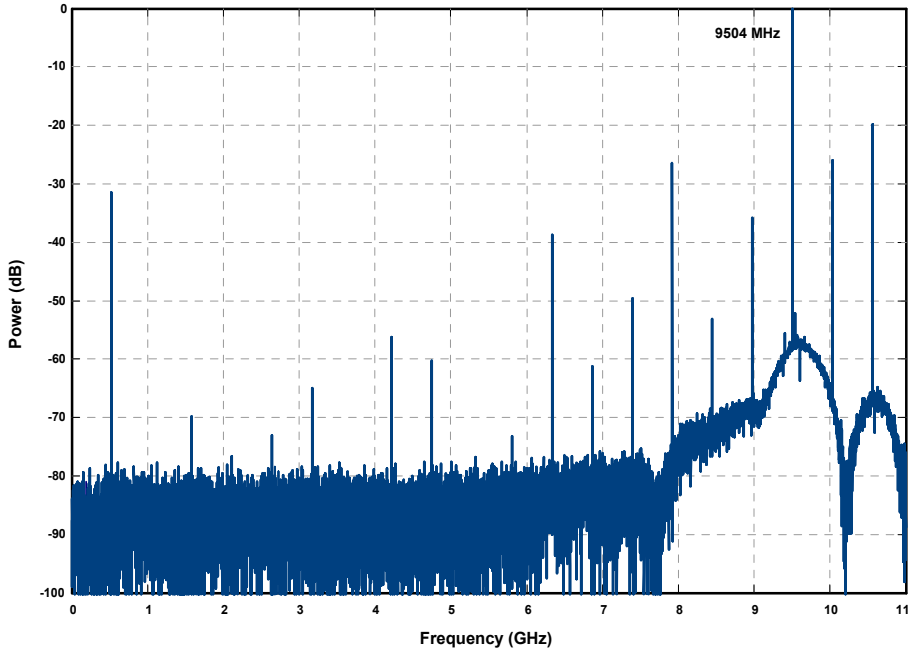

Fig. 3.17 Output spectrum for synthesizer architecture (III). (© [2005] IEEE)

The spurious tones generated by the synthesizer that are outside the UWB spectrum can cause interference to other communication systems and down-convert their emissions; thereby corrupting the received signal. The first effect must be suppressed by proper antenna design and off-chip filtering. On the other hand, if the down-converted interference from other non-UWB devices is narrow-band, it can be tolerated to a certain degree by the inherent interference rejection capabilities of OFDM with coded QPSK constellation modulation format employed [23]. From Tables 3.6 and 3.7 it can be noted that both architectures produce spurs at 5808 MHz and 5280 MHz, which fall in the U-NII band. Architecture (II) produces a tone at 5544 MHz, which overlaps with the band used by the HIPERLAN standard. The tones at 2376 MHz and 2640 MHz are close but not at the populated 2.4 GHz ISM band. It is important to note that neither of the architectures produces any spur in the range of 800 MHz to 2 GHz where the mobile phone (GSM, DECT) and GPS standards are located. Moreover, the spurs generated by both architectures comply with the FCC spectral mask requirements for UWB emissions.

As shown in Fig. 3.10, the adverse effect of unwanted tones at frequencies within the UWB spectrum is that they down-convert the signals from peer UWB devices transmitting at the frequency of the spur, corrupting the signal from the band of interest. Based on Fig. 3.11 a simulation setup is created assuming that there is a UWB peer device transmitting in each of the 10 bands different from the one of interest. In this pessimistic scenario, any spur from the synthesizer within the UWB spectrum down-converts an undesired peer transmission. For each architecture, a simulation is performed for the reception of each of the two bands for which the synthesizer shows the largest

amount of spurs. The considered simulation scenarios are summarized in Table 3.8. The simulation results are shown in Figs. 3.18 and 3.19.

Table 3.8 Different evaluation scenarios of BER degradation due to the interference from peer devices

Synthesizer Architecture	Band of interest (LO frequency)	Power of peer interferers in all other bands	BER Curve
II/III	Ideal case, LO signal with no spurs		a in Fig. 3.18, 3.19
II	10296	Same as band of interest	b in Fig. 3.18
II	8184	Same as band of interest	c in Fig. 3.18
II	10296	6dB above the band of interest	d in Fig. 3.18
II	8184	6dB above the band of interest	e in Fig. 3.18
III	6336	Same as band of interest	f in Fig. 3.19
III	8796	Same as band of interest	g in Fig. 3.19
III	6336	6dB above the band of interest	h in Fig. 3.19
III	8796	6dB above the band of interest	i in Fig. 3.19

Two different cases are evaluated for each received band; when each of the interferers has the same power as the signal of interest and when it has 6 dB higher power. In both figures, curve ‘a’ represents the performance of the ideal receiver with no spurs in the LO, which is also equivalent to not having any interferer. Fig. 3.18 depicts the receiver performance in the worst spur scenarios for architecture (II) which correspond to the reception of the band at 10296 MHz and the one at 8184 MHz. Fig. 3.19 shows the receiver performance in the worst spur scenarios for architecture (III),

which are the reception of the band at 6336 MHz and the band at 8976 MHz (equivalent in terms of spurs to the reception of the 7920 MHz band).

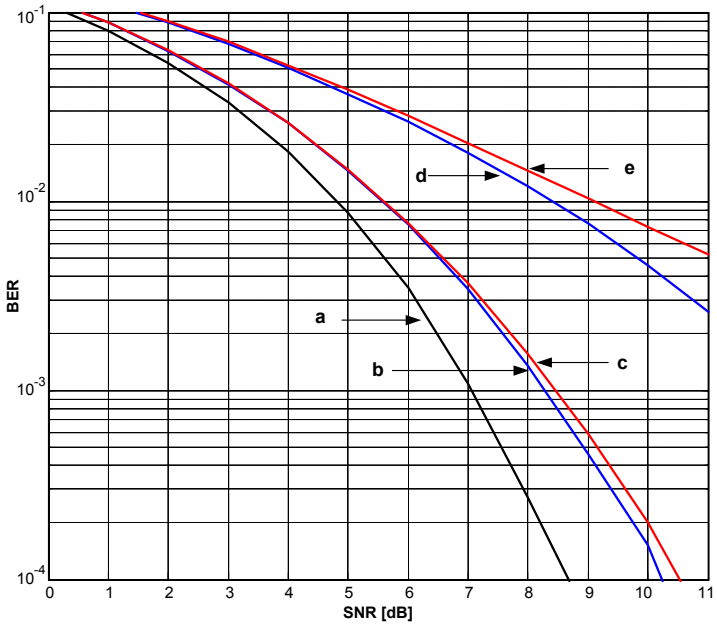

Fig. 3.18 BER degradation in the presence of peer interferences due to spurs in the LO from synthesizer architecture (II). (© [2005] IEEE)

From the BER plots it is important to observe that when the interferers have the same power as the signal of interest, the degradation in the performance is not significant (<1 dB in SNR) and the amount of spurs does not seem to make a relevant difference. That is, the degradation is dominated by the strongest spur. However, when the power of the interferers grows, the degradation in the performance is apparently stronger for the reception cases with a larger number of spurs. It is important to mention that the bit interleaving and forward error correction techniques employed in a complete MB-

OFDM radio [11] are expected to reduce the BER degradation due to interference from other UWB devices. Nevertheless, the obtained results for a pessimistic scenario with un-coded data remark the importance of a frequency planning and architecture design that yields the smallest amount of spurs for each generated frequency.

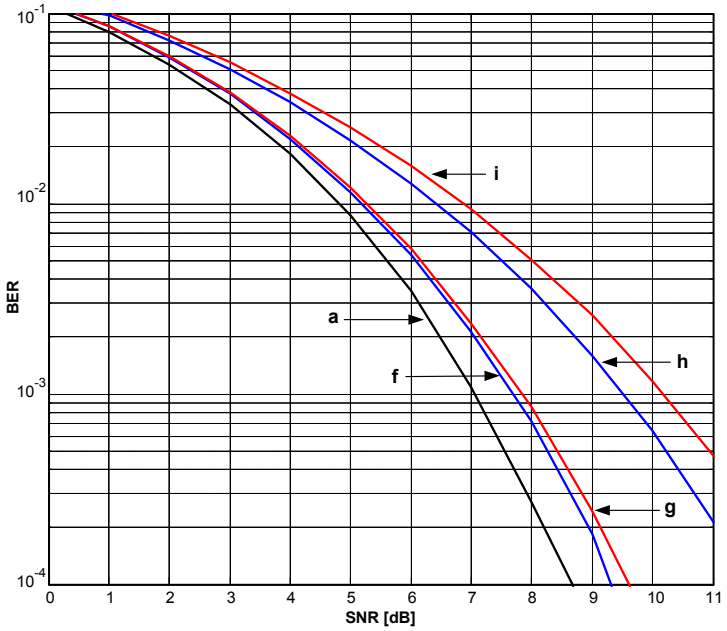

Fig. 3.19 BER degradation in the presence of peer interferences due to spurs in the LO from synthesizer architecture (III). (© [2005] IEEE)

CHAPTER IV

3-10 GHZ, 11 BAND FREQUENCY SYNTHESIZERS IN SIGE BICMOS*

In this chapter, two different hardware implementations of 11 band 3-10GHz frequency synthesizers in 0.25μm SiGe BiCMOS are presented. These synthesizers are based on the proposed band plan and architecture of the previous chapter, which were designed with the objective of attaining a synthesizer solution that uses the minimum number of components and reduces the generation of spurs. These architectures discussed in this chapter rely on the fact that band switching occurs within a particular band group and hence not all frequencies need to be simultaneously present.

4.1 Implementation I

4.1.1 Architecture Description

The underlying idea of this implementation is to generate the reference tones (shown as f in Fig.4.1) in any band group and thereby derive the other tones in the same band group by a final up/down conversion with a 528MHz tone [34]. From a single frequency source at 8448 MHz, which is the reference tone in band group #3, the reference tone 4224 MHz in band group #1 is derived using a divide by 2 only. Two other reference tones according to the band plan described in Chapter III, 6864 MHz and

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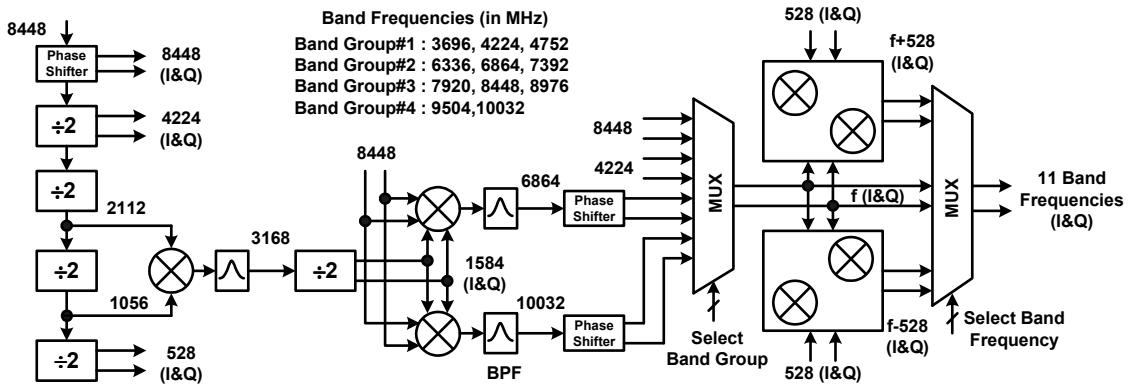

Fig. 4.1 3-10 GHz, 11-band synthesizer implementation I. (© [2006] IEEE)

10032 MHz are generated by a down conversion and an up conversion of 8448 MHz with a 1584 MHz tone. As shown in Fig. 4.1 the generation of 1584 MHz tone requires the up conversion of 2112 MHz with 1056 MHz followed by a division by 2 [34]. Both 2112 MHz and 1056 MHz are provided via direct division of 8448 MHz tone. Band-pass filtering is employed at the output of the mixer to reduce the level of the unwanted sideband.

Single side-band (SSB) mixers are used for the generation of 6864 MHz, 10032 MHz and all other frequencies that require the final up/down conversion. Dedicated band-pass filtering is used at the output of the mixers that generate 6864 MHz and 10032 MHz. This is possible because the output is at a single frequency, unlike the outputs of the mixers that perform the final up/down conversion with 528 MHz. The mixers shown enclosed in a box are SSB mixers with inputs as the reference tones and 528 MHz all in quadrature. Each mixer generates one of f+528 or f-528 in either in-phase or quadrature-phase. Two multiplexers are used to choose the band group and the band frequency in

the chosen band group. This shows that the band hopping time is primarily dominated by the switching time of the final multiplexer as all the carrier frequencies in a particular band group are always available in quadrature at its input.

4.1.2 Circuit Implementation of Building Blocks

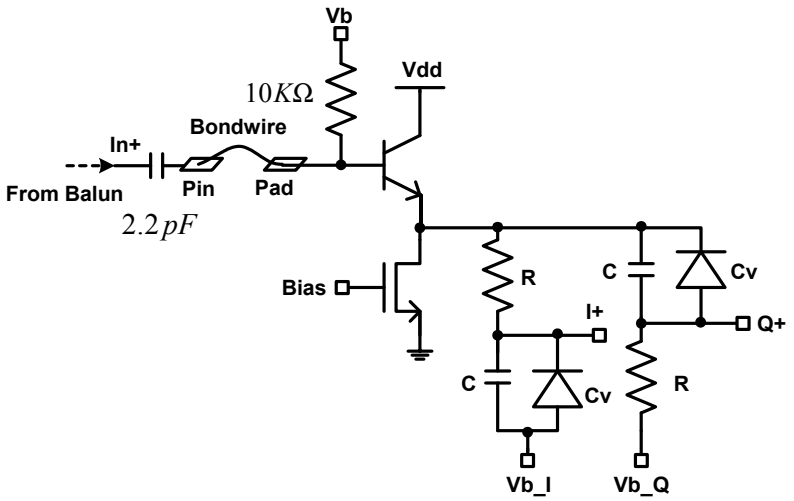

Fig. 4.2 Phase shifter schematic (Only half of the circuit is shown).

The different circuit blocks include the phase shifters, dividers, SSB mixers and multiplexers. The circuits are implemented in a 0.25μm BiCMOS technology where the peak f_T of the bipolar transistor is 47GHz [34].

A. Phase Shifter

The phase shifter splits the phase of the input signal such that the outputs are in quadrature. It is a high-pass low-pass RC-CR network as shown in Fig. 4.2. The input to

this circuit in this implementation is an external differential signal at 8.448 GHz. Only half circuit is shown in Fig. 4.2. for simplicity. Amplitudes of the I and Q signals are equal at the corner frequency of each of the low-pass and high-pass structure. The phase shifter is a first order tunable network that is implemented on-chip with a 100 Ω resistor and a 160 fF capacitor along with varactors to tune the cut-off frequency for process variations. Dedicated phase shifters could be used because of the uniqueness of the frequencies involved. The phase shifters at 6.864 GHz and 10.032 GHz are implemented in a similar way as shown in Fig. 4.2 without the external input connection via bondwire.

B. Dividers

The dividers are based on two current-mode logic type high-speed D flip-flops connected in a configuration as shown in Fig. 4.3. The synthesizer architecture uses the inherent property of the divider to generate *I* and *Q* signals to its advantage. Each of these I and Q signals drive any of the following stages through intermediate buffers implemented using emitter follower configuration.

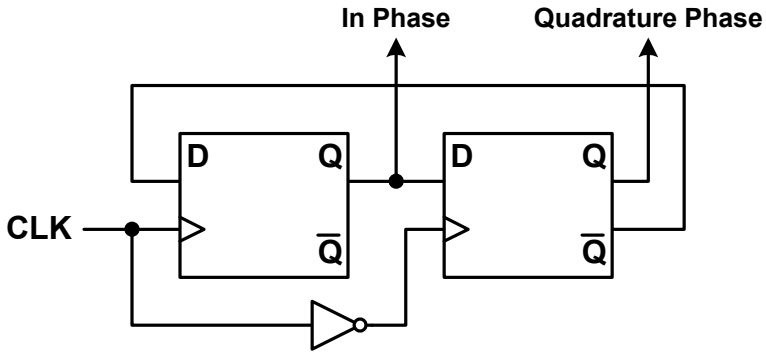

Fig. 4.3 Divide by 2 circuit based on flip-flop connected in feedback.

C. SSB Mixers

Fig. 4.4 shows the schematic of a SSB mixer. Conceptually, it consists of two mixers with quadrature inputs at two frequencies and a common output where the signal outputs from both the mixers are either added or subtracted from each other. Since all signals required for mixing are available in quadrature or are derived using phase shifters, SSB mixers could be used. To provide further attenuation to the unwanted sidebands and spurs, filtering in the form of LC tanks are used as loads of some of the SSB mixers. Because of the multi-frequency output of the mixers employed for final up/down conversion such dedicated filtering could not be used. Instead resistive loads were used in those mixers for broadband operation. The transistors were properly chosen so as to operate very close to their peak f_T for a given bias current. MOS transistors were used for biasing so as to use less voltage headroom. Amplitude and phase mismatches are minimized by using symmetry in the layout.

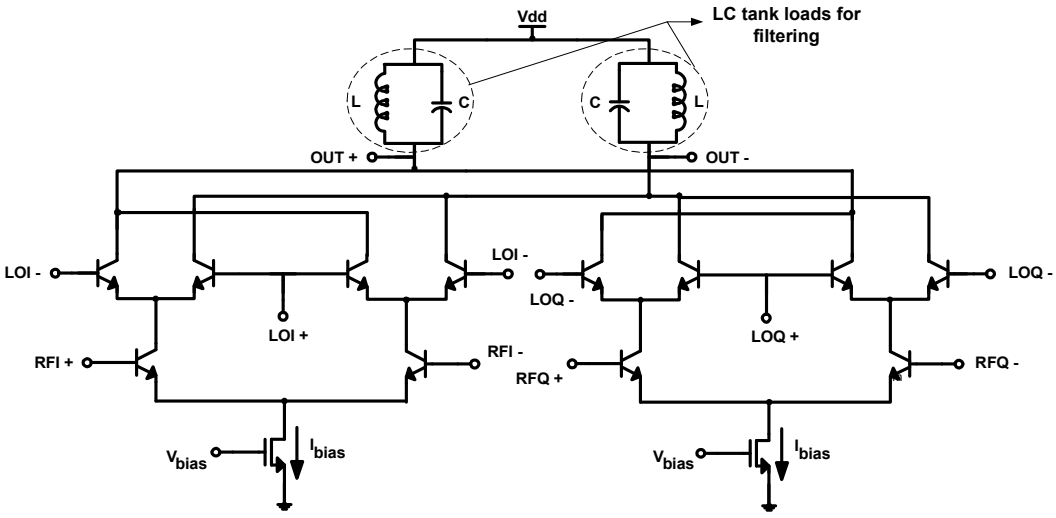

Fig. 4.4 Single side-band (SSB) mixer with LC tank load. (© [2006] IEEE)

D. Multiplexers

The multiplexers are based on several differential pairs sharing a common resistive load. Their activation and deactivation is through a clock signal to enable or disable the tail current. Cascode transistors are used in the differential pairs to improve isolation between the stages. Apart from providing frequency selection, these stages also helped in boosting the signal strength. It must be mentioned here that because of intensive routing there was significant loss in signal levels. The final multiplexer feeds an open-collector output buffer that is loaded by the instrument via the bonding wire and the package.

4.1.3 Experimental Results

The chip microphotograph is shown in Fig. 4.5. The active area excluding pads is 2.2×1.9 mm^2. The measurement results are obtained from a chip in a QFN64 package when mounted on a FR-4 printed circuit board (PCB) as shown in Fig. 4.6. No input or output was wafer-probed.

Fig. 4.7 shows the spectrum for the first band frequency in band group#1. In the spectrum it can be seen that there is significant leakage of the input signal at 8448 MHz to the output. This signal at 8448 MHz is fed into the chip differentially through a 5315A 17 GHz balun from Picosecond Pulse Labs, which has an attenuation of 8 dB. All results shown in this section are based on single ended measurements. The spur in the UWB spectrum is below 20 dBc, which would result in about 1 dB degradation in SNR for the required BER as was shown in the previous chapter. Spurs in U-NII band in the 5-6GHz

range are below 30dBc. Spurious tones could be further reduced by improving quadrature accuracy at 8448MHz. Another possibility would be to use a quadrature VCO at 8448MHz or a VCO at 16896MHz followed by a divide by 2. Fig. 4.8 shows the output spectrum when band frequency 7392MHz in the band group #2 is generated. This is one case where the generation of a frequency involves a cascade of three mixers. Because of dedicated filtering the spur levels are much lower. The power of the tone is low because of higher attenuation of the buffer and the PCB at such frequencies.

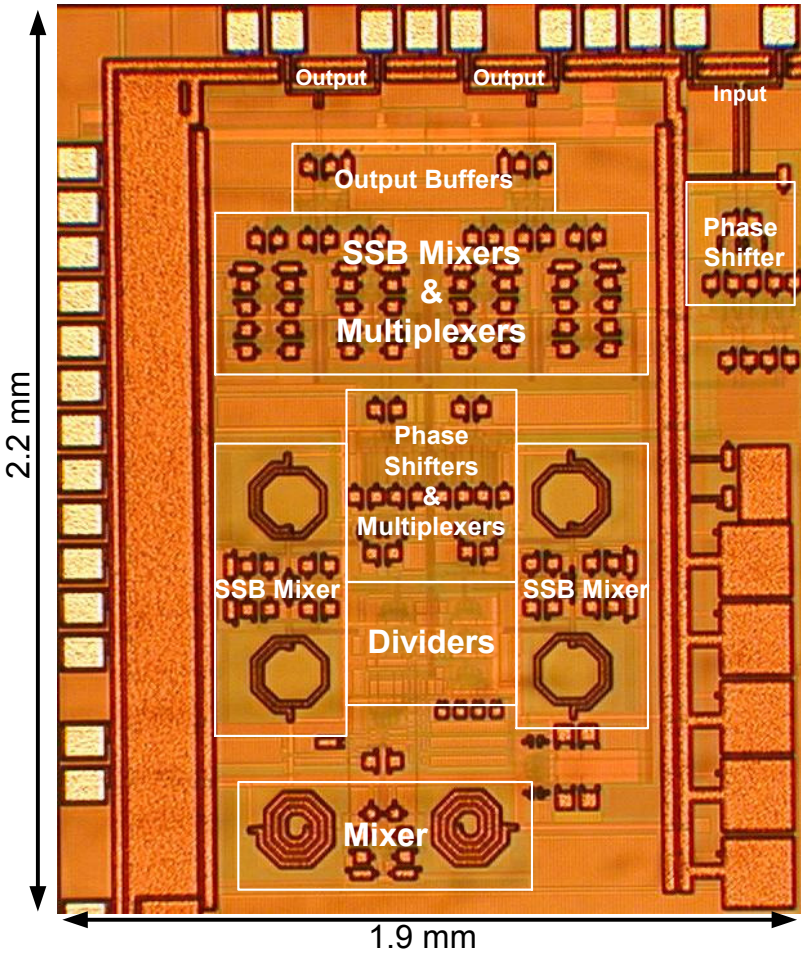

Fig. 4.5 Chip microphotograph of synthesizer implementation I. (© [2006] IEEE)

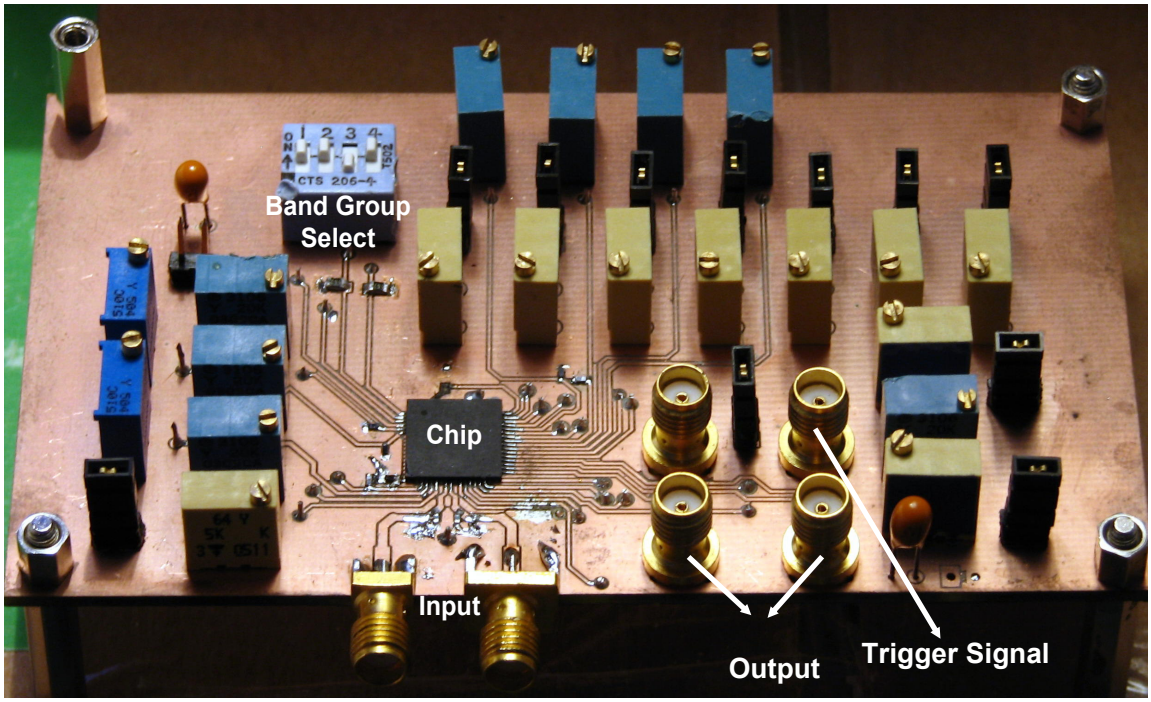

Fig. 4.6 PCB prototype of synthesizer implementation I.

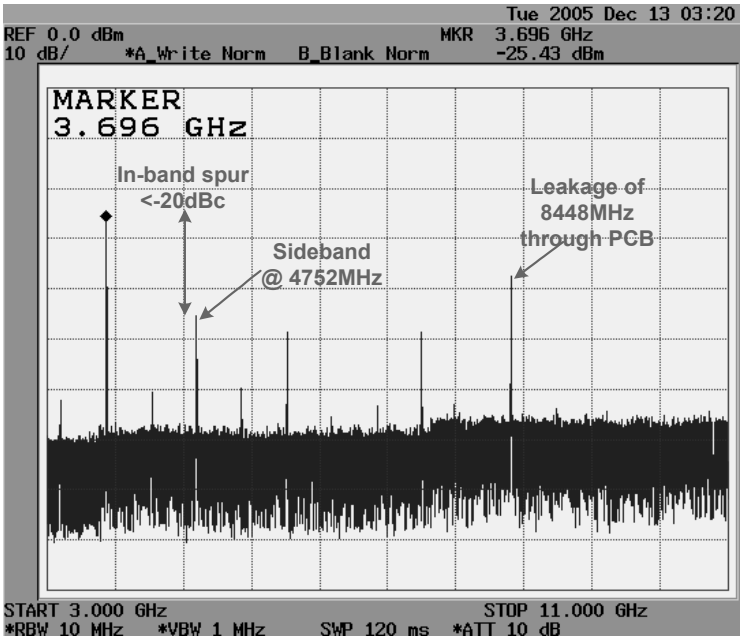

Fig. 4.7 Measured output spectrum for band frequency #1. (© [2006] IEEE)

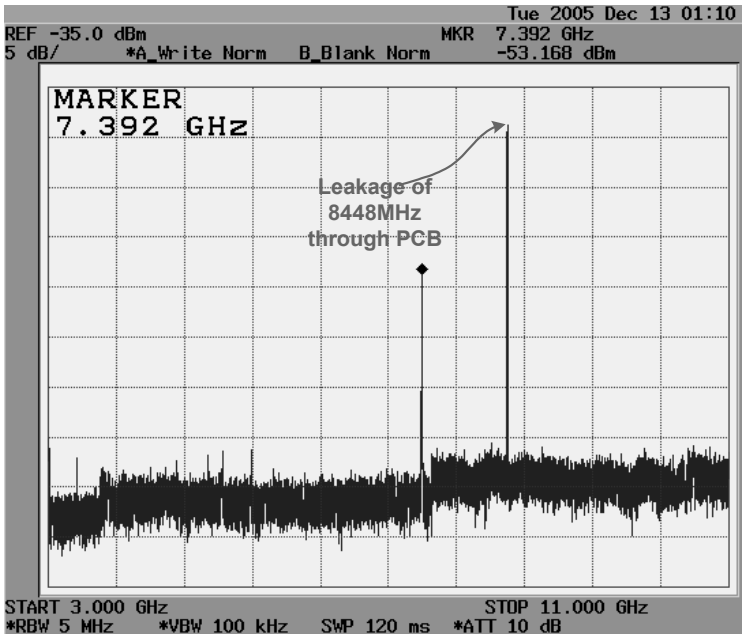

Fig. 4.8 Measured output spectrum for band frequency #6. (© [2006] IEEE)

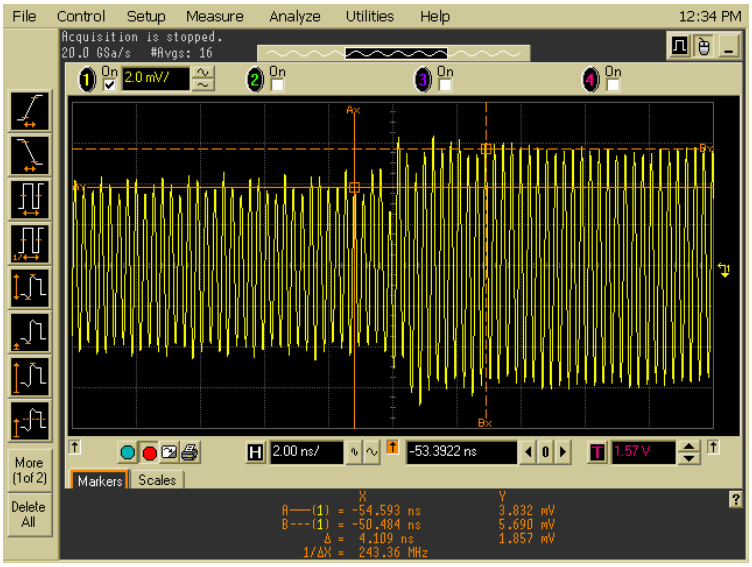

Fig. 4.9 Transient switching from 4752 MHz to 3696 MHz. (© [2006] IEEE)

The fast switching property of the carrier frequency generator is shown in Fig. 4.9. A clock generator was used to trigger the control of the multiplexer. From Fig. 4.9 it is clearly seen that the switching time is close to 4 ns. It must be mentioned here that this measurement includes the effects of the package and the PCB. Hence if package effects and delay due to PCB trace is ignored the actual internal switching time would be smaller.

4.2 Implementation II

4.2.1 Architecture Description

The frequency synthesis scheme employed in this architecture is detailed in Table 4.1. In comparison to the architectures presented in [24] and [34], this architecture shown in Fig. 4.10, is more compact and involves less hardware while providing more functionality. This is mainly due to the avoidance of dedicated or tunable filtering at the mixer outputs thereby reducing hardware complexity at the expense of spur performance.

The architecture of the frequency synthesizer includes a phase shifter, a chain of dividers, SSB mixers with and without quadrature outputs, multiplexers and a single frequency source, which in this particular implementation is external. The input frequency is chosen to be 8448 MHz as it results in a very simple and less hardware intensive architecture. This frequency forms the input to a phase shifter which splits the signal into its I and Q phases. One of the phases goes through a divide by 2 circuit to result in 4224 MHz. The 8448 MHz and 4224 MHz tones form the reference tones in

band groups 1 and 3 respectively. The 4224 MHz tone after successive division results in 2112, 1056 and 528 MHz tones. The tones at 528 MHz and 1056 MHz can serve as the clock for the baseband analog to digital converter (ADC) in a radio depending on the sample rate and architecture of the ADC. This architecture uses a down conversion between 4224 MHz and 1056 MHz contrary to an up conversion between 2112 MHz and 1056 MHz as in [30]. This results in equal loading of the outputs of the dividers by the SSB mixers as shown in Fig. 4.10 thereby reducing *I-Q* imbalance. Also, since 3168 MHz happens to be the lower sideband in this case, filtering the unwanted upper sideband is easier in this case.

Table 4.1 Frequency synthesis scheme implemented in the frequency synthesizer

Band Group	Band #	f_c (MHz)	Frequency Synthesis
1	1	3696	$f_o/2 - f_o/16$
	2	4224	$f_o/2$
	3	4752	$f_o/2 + f_o/16$
2	4	6336	$f_o - \{(1/2) \times (f_o/2 - f_o/8)\} - f_o/16$
	5	6864	$f_o - \{(1/2) \times (f_o/2 - f_o/8)\}$
	6	7392	$f_o - \{(1/2) \times (f_o/2 - f_o/8)\} + f_o/16$
3	7	7920	$f_o - f_o/16$
	8	8448	f_o
	9	8976	$f_o + f_o/16$
4	10	9504	$f_o + \{(1/2) \times (f_o/2 - f_o/8)\} - f_o/16$
	11	10032	$f_o + \{(1/2) \times (f_o/2 - f_o/8)\}$

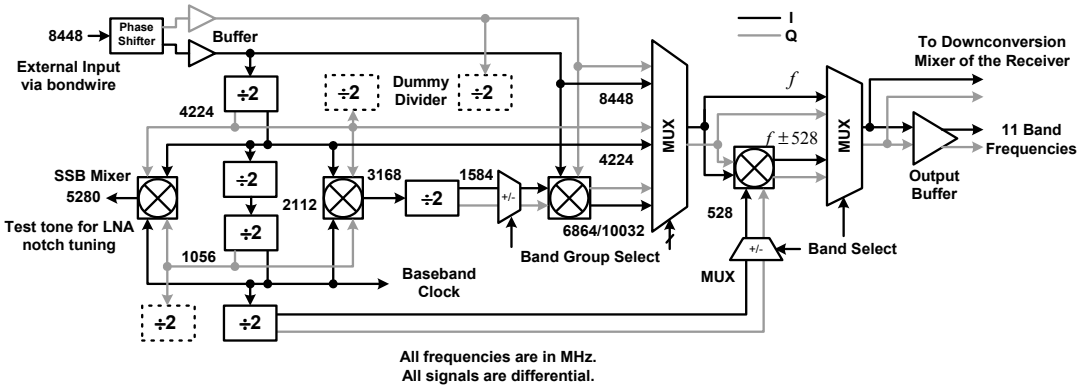

Fig. 4.10 Architecture of the 11-band frequency synthesizer.

Dummy dividers are placed at different stages to reduce imbalance between *I* and *Q* paths. The reference tones for band group 2, ($f_{c,5}$) and 4 ($f_{c,11}$) are generated from the 8448 MHz tone (f_o) using (4.1) and (4.2).

$$f_{c,5} = f_o - \frac{1}{2}\times\left(\frac{f_o}{2} - \frac{f_o}{8}\right) \Rightarrow 6864 = 8448 - \frac{1}{2}\times(4224 - 1056) \tag{4.1}$$

$$f_{c,11} = f_o + \frac{1}{2}\times\left(\frac{f_o}{2} - \frac{f_o}{8}\right) \Rightarrow 10032 = 8448 + \frac{1}{2}\times(4224 - 1056) \tag{4.2}$$

Divide by 2 circuits ensure quadrature phases at most of the frequencies. Quadrature SSB mixers are used to produce signals in quadrature phases where necessary. Since dedicated filtering is avoided to save area and reduce circuit complexity, most of the blocks have a broadband behavior. The band-hoping time is given by the switching time of the multiplexer or that of the final SSB quadrature mixer. For a band hopping taking place between the extreme two tones in a band group (not involving the reference tone) the multiplexer does not switch and it is only the SSB mixer that switches from the

upper sideband to the lower sideband or vice versa. In case of band hopping involving a reference tone, only the multiplexer switches.

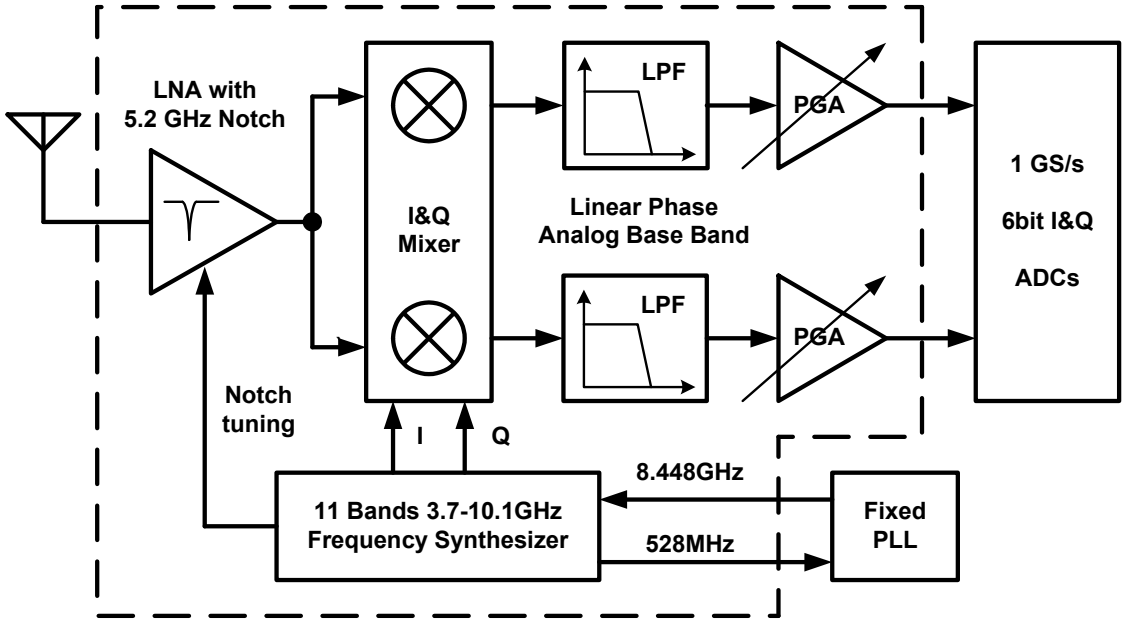

Fig. 4.11 11-band 3-10 GHz direct conversion receiver architecture.

This frequency synthesizer is integrated in an 11-band 3-10 GHz direct conversion receiver [35-36] shown in Fig. 4.11. The receiver includes a 3-10 GHz front-end with on-chip notch filter at 5.2 GHz and a 264 MHz linear phase analog baseband with 42 dB of digitally programmable gain apart from the 11-band synthesizer. The synthesizer has provision to generate a test tone at 5280 MHz for on-chip tuning of a notch filter in the receiver's LNA that rejects interferences in the range of 5.15-5.35 GHz as shown in Fig. 4.11. This on-chip tunable notch filter in the front-end along with

the off-chip pre-select filter relaxes the spur requirements from the synthesizer in the 2.4 GHz and 5-6 GHz ISM bands.

An additional benefit of this synthesizer architecture is the ease with which power saving modes for the different blocks can be introduced. Since fast-hoping UWB communication takes place within a band group, circuits that are not used in the generation of band frequencies in that band group can be powered down thereby resulting in a more power efficient solution when used in multi-mode scenarios. From Fig. 4.10 it can be seen that, during the generation of frequencies in band group 1 and 3, two mixers, a divider and a multiplexer could be turned off. Hence, for the generation of 6 out of 11 frequencies, about 25% of the total power could be saved. Next, the description of different blocks of the synthesizer is described.

4.2.2 Current Mode Logic (CML) Divider

The D flip-flops used in the CML divider are based on current mode logic as shown in Fig. 4.12.The output of the first flip-flop feeds the next flip-flop directly and the output of the next flip-flop feeds the input of the first flip-flop with reverse phases to result in quadrature signals at the outputs (Fig. 4.3). Each of these *I* and *Q* signals drive the next stage divider in the divider chain through intermediate buffers implemented using emitter follower configuration.

The frequency at the output of the flip-flops is limited by the pole formed by the resistive load and any parasitic capacitance. The tail current is scaled down (1:0.5:0.25) and the load resistor is scaled up (1:2:4) when the divider operating frequency is scaled

down (8.4 GHz: 4.2 GHz: 2.1 GHz) to save power while having similar voltage swings. Fig. 4.12 also shows some fixed capacitors that are used at the output of the flip-flops as well as the output of the buffers connected to the flip-flops. These capacitors were used only to filter out any harmonics present in the divided signals thereby spectrally purifying the signals as much as possible. No instability is observed in the operation due to the capacitors. This helps in reducing spurs in the mixers following the dividers as each port of the mixer is now spectrally pure. Also, dummy dividers were used to minimize amplitude and phase imbalance between the *I* and *Q* paths. However, the buffers are deactivated in these dummy circuits to save power.

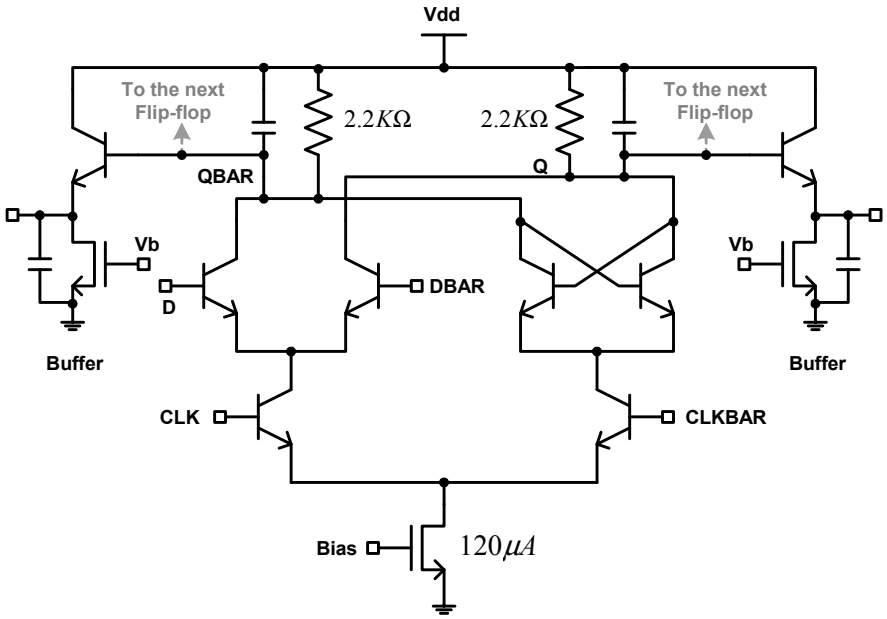

Fig. 4.12 Schematic of the current mode logic based D-flip flop used in the implementation of the divider (only one D-flip flop shown).

4.2.3 Broadband Single Sideband Mixer

The availability of quadrature signals from the divider chain makes it suitable to use SSB mixing. SSB mixing helps in suppression of the sideband created as a result of mixing of two frequencies. Fig. 4.13 shows the concept of SSB mixing for both up and down conversion as well as for *I* and *Q* phase outputs. A SSB mixer takes quadrature inputs of two signals and results in either the sum or the difference of the two frequencies. By swapping the *I* phase with the *Q* phase at the input or by applying the input with an inverted polarity, different outputs can be obtained as shown in Fig. 4.13. Two such SSB mixers can be combined to result in quadrature outputs of the sum or the difference of two frequencies.

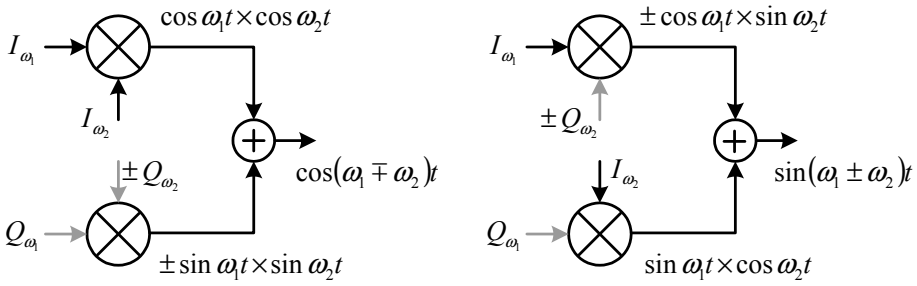

Fig. 4.13 Conceptual block diagram showing SSB mixing.

The mixers generating the 3168 MHz tone and 5280 MHz tone are simple SSB mixers without quadrature outputs. But the other mixers are quadrature SSB mixers. Fig. 4.14 shows the schematic of the employed quadrature mixer. When the outputs of a similar quadrature mixer (with the *Q* phase of frequency ω_1 as its input) are added to the outputs of this mixer as shown in Fig. 4.13, the structure results in SSB quadrature

outputs. The sum or the difference of the two frequencies can be obtained by using similar techniques as explained above. Multiplexers are used to choose between the opposite polarities of *I* or *Q* signals thereby resulting in the upper or the lower sideband (Fig.4.10). A digital control switches between those inputs thereby switching the output of the SSB mixer between the upper and the lower sideband. Because of the broadband nature of the output resistive loads were used and dedicated filtering was avoided. This reduces the area and complexity with little penalty in spurious performance.

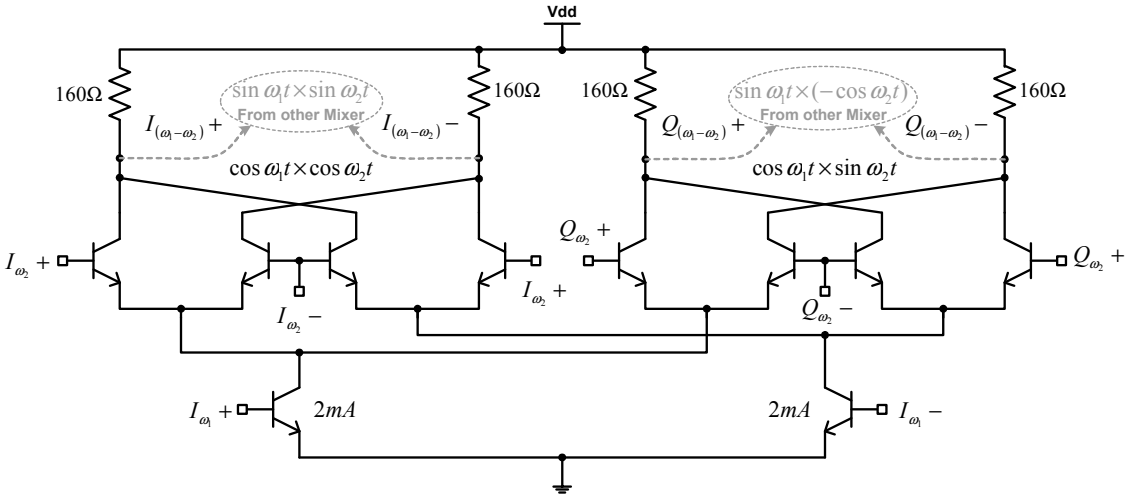

Fig. 4.14 Broadband SSB mixer with quadrature outputs (only one mixer shown).

The tail current is avoided in these mixers to gain voltage headroom. Since these mixers operate at very high frequencies, having the transistors operate at the maximum f_T is very critical. The collector to base voltage for every transistor is maximized in order to reduce the parasitic capacitance C_μ to increase the frequency of operation, thereby requiring higher collector voltages. Non-linearity due to the mixing was curtailed

because signals appearing at its input were spectrally very pure due to the filtering employed in the dividers. Harmonics of the high frequency input signals for the bottom pseudo-differential transistors are shunted largely by the capacitance at the common source node of the two upper differential pairs thereby minimizing spurious mixing. The resistive loads for the mixers are chosen after extracting the parasitics due to interconnects at those nodes.

4.2.4 Multiplexer

Fig. 4.15 shows the schematic of the employed 2:1 multiplexer [36]. The same structure can be extended to more inputs. The multiplexers used in the architecture consist of several differential pairs with a common load. The digital bits b and $\bar{b}$ enable or disable the biasing to both the cascode transistors as well as the tail current transistors. Cascode transistors help in improving isolation between the stages.

Except for the final multiplexer that drives the down conversion mixer of the UWB front-end all other multiplexers use resistive loads. The final multiplexer uses inductive peaking to boost signals at higher frequencies. This is to provide equal amplitude signals over the entire range of frequencies at the input of the down conversion mixer. This is because the noise figure of the mixer greatly depends on the amplitude of the LO signal. This is the only circuit in the entire system that uses any inductors. No inductors are used in the circuits involved in the frequency synthesis thereby resulting in significant area reduction compared to [30].

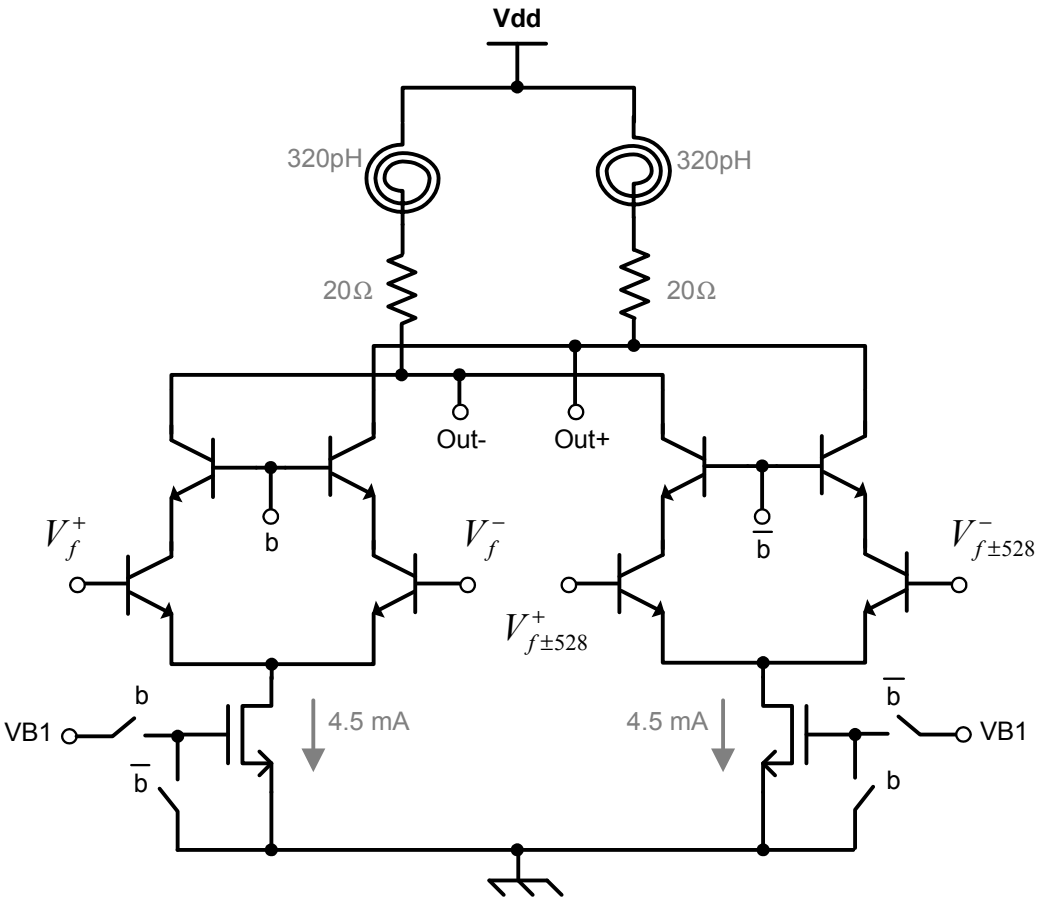

Fig. 4.15 LO buffer and multiplexer (Only one path (I/Q) shown). (© [2007] IEEE)

4.2.5 Output Buffer

An open collector buffer (Fig. 4.16) serves as the output buffer to drive the instrument for external test. The output of the final multiplexer is coupled to both this output buffer as well as the down conversion mixer. The buffer is biased via an external RF choke and one of the differential outputs is terminated by a 50 Ω and the other output drives the instrument. The synthesizer is characterized from a single ended output to avoid the use of another wideband balun. The inputs and the outputs are all capacitively coupled.

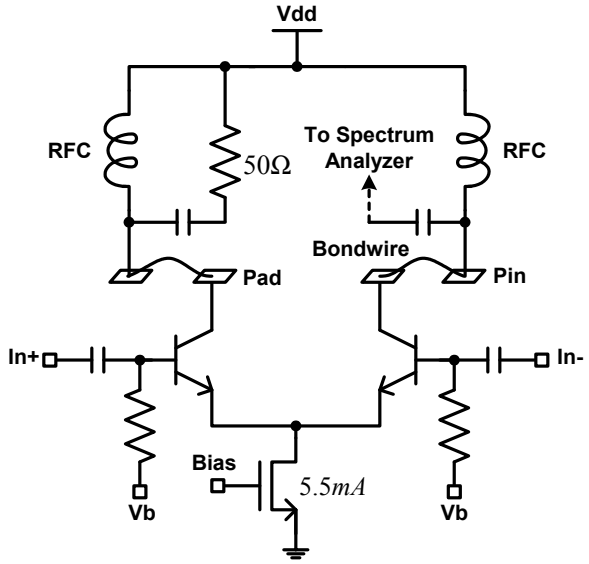

Fig. 4.16 Open collector output buffer that drives the measuring instrument.

4.2.6 Design and Layout Considerations

In the design and layout of the above circuits the following guidelines are followed. The bipolar transistors are chosen properly to operate very close to their peak f_T for a given bias current. Care is taken to account for process variations. MOS transistors are used for biasing wherever necessary to use less voltage headroom. Inter stage coupling is done via high pass (CR) network to eliminate dc offsets. Amplitude and phase mismatch between quadrature phase signals is reduced by using symmetric loading with dummy circuits, and symmetric routing of signal lines. Top metal lines are used for interstage routing to reduce coupling to substrate. The lines are not too thin (<1μm) to be highly resistive nor are they too wide (>5μm) to introduce more capacitance. Wide (~50μm) ground planes made of heavily doped P+ areas are used beneath high frequency lines to prevent unwanted coupling between adjacent signal

lines. Since the entire system is in a package, effects of bond wire on the input and the output are simulated and considered in the design. Large on-chip bypass capacitors of various sizes are placed between power and ground lines to prevent supply bouncing and also on critical DC bias lines to prevent coupling of high frequency transients through them. Multiple power and ground pins are used in the chip to minimize the effective series bonding inductance.

4.2.7 Experimental Results

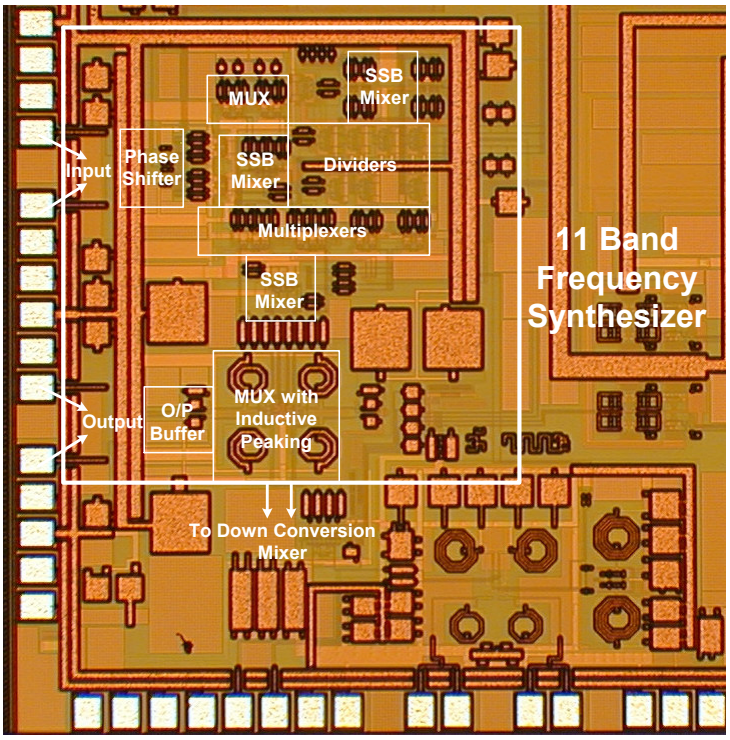

Fig. 4.17 Chip microphotograph of synthesizer implementation II.

The frequency synthesizer is integrated in an UWB receiver prototype [36] and is fabricated in a 0.25µm SiGe BiCMOS process. It has an active area of 1.5x1.5 mm^2 and almost 30% of it comprises of inductors used in the final quadrature multiplexer, bypass capacitors and other empty areas. Fig. 4.17 shows the chip microphotograph highlighting the circuits described in the previous sections.

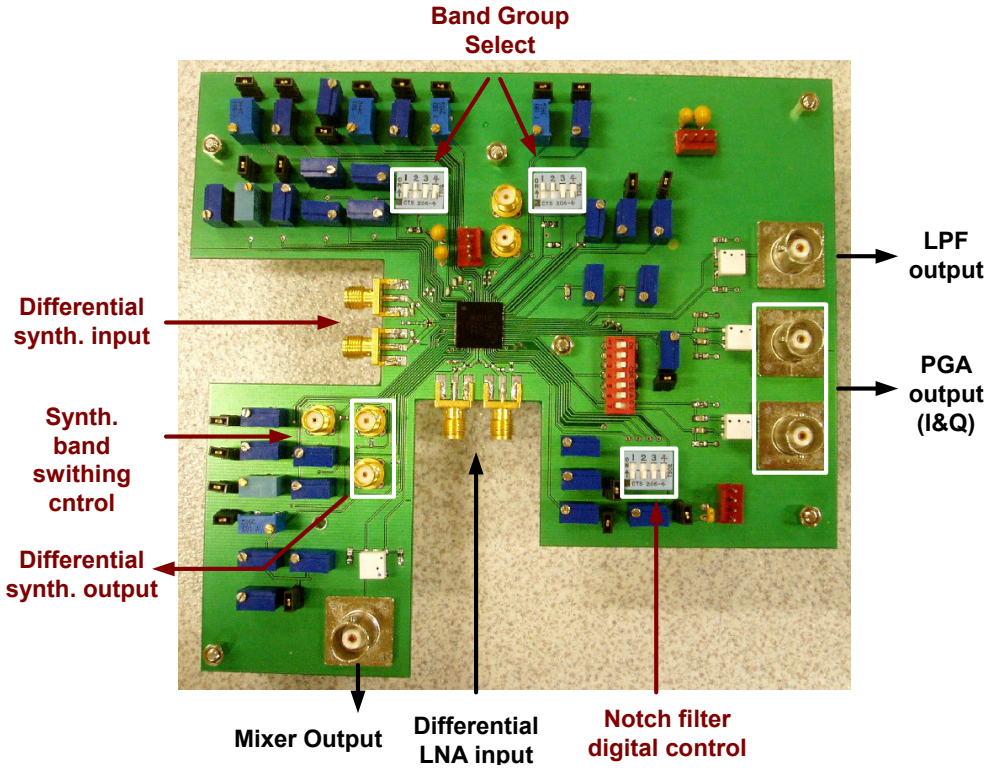

Fig. 4.18 PCB prototype for the UWB receiver. (© [2007] IEEE)

The packaged die is mounted on a FR-4 substrate for characterization as shown in Fig. 4.18. Fig. 4.19 presents the test setup for the characterization of the frequency synthesizer. The input is provided from a signal generator via a high frequency cable to

the 5315A wideband balun from Picosecond Pulse Labs. The balun produces a differential signal at 8448 MHz. There is 8 dB loss from the balun and 1 dB loss from the cables.

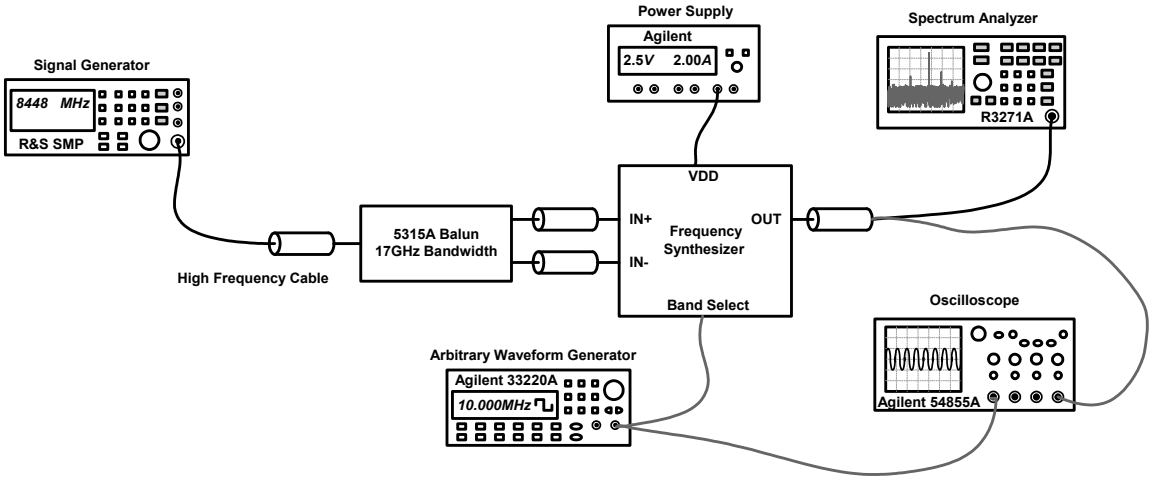

Fig. 4.19 Test setup for characterization of the frequency synthesizer.

For the frequency spectrum characterization, the single ended output of the output buffer is connected to the spectrum analyzer. Figs. 4.20, 4.21 and 4.22 show the output frequency spectrum for 4752 MHz, 6336 MHz and 10032 MHz bands respectively. In all the three spectrums there is a significant leakage of the 8448 MHz input tone. The power of the signal at the input of the PCB is about 0 dBm in order to overcome any loss in the PCB. The coupling through the stand alone PCB from the input of the synthesizer to its output was measured (with the IC powered down) to be close to -30 dB. The spectrum of 6336 MHz is one of the worst case scenarios in terms of spurs as its generation involves three mixing operations. The spurs at in-band frequencies for all

frequency bands up to 8.5 GHz are better than -18dBc, which is tolerable according to analysis, presented in Chapter III. For frequencies greater than 8.5 GHz, the measured spur rejection is not very accurate. At such frequencies, the effect of the bond wire and the loss in PCB reduce the power level of the desired tone and hence the rejection for spurs at lower frequencies appears to be lower. The loss is due to the low pass characteristic of the output buffer with a 3-dB cut-off at 7 GHz (from post layout simulation including bondwires, off chip components and estimated PCB parasitics) resulting in an attenuation of 10 dB at frequencies close to 9 GHz.

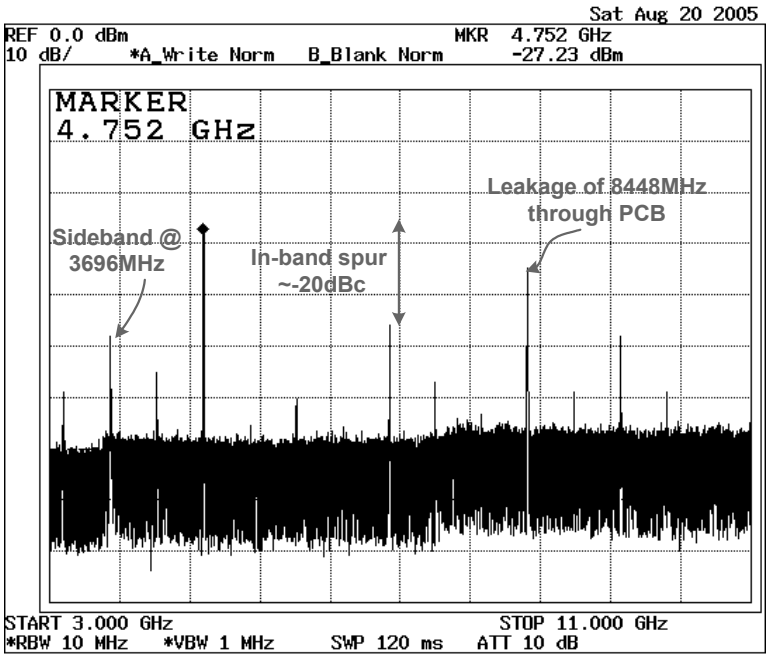

Fig. 4.20 Measured output spectrum for band #3.

Most of the spurs obtained from measurement are either sidebands as a result of SSB mixing or a result of harmonic mixing (especially in the final mixer where one of

the inputs is the low frequency 528 MHz tone). Certain other spurs such as 6864 MHz during the generation of 4752 MHz can only be attributed partially to the leakage and partially due to non-linearity at the LO port as explained. Spur at 5280 MHz (test tone for LNA notch tuning) is also due to a similar reason.

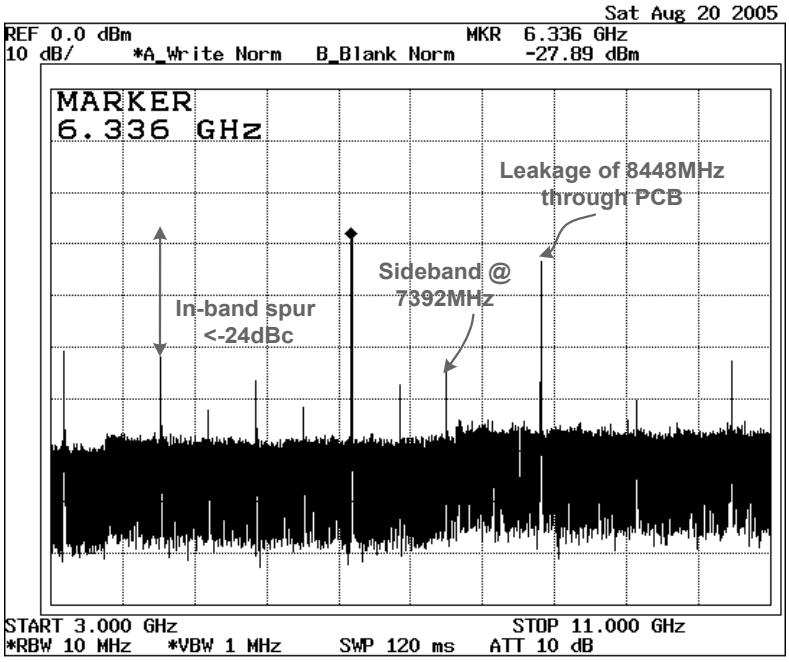

Fig. 4.21 Measured output spectrum for band #4.

The connections shown with shaded lines are for the transient characterization (Fig. 4.17). For the switching time measurement the control of the final multiplexer was switched with the help of an arbitrary waveform generator and the output of the synthesizer as well as the control signal were captured using an Agilent Infinium 54855A oscilloscope. Fig. 4.23(a) and (b) show the post layout simulated and measured band switching from 4224 MHz to 3696 MHz. The hopping time is approximately 7.3 ns

which is slightly more than that predicted by post layout simulation results for all cases. This is partly due to the large rise time of the trigger signal used as compared to a very fast trigger signal used in simulation (rise time of 100 ps). Furthermore, this measurement includes the effect of the bond wire and the PCB trace. In fact the actual internal hopping time at the LO port of the quadrature mixer is close to 5 ns and was verified at the mixer output as shown in Fig. 4.24. To perform this test the RF input to the LNA was fixed at 4.124 GHz and the LO frequency was switched from 4.224 GHz to 3.696 GHz resulting in a baseband output switching from 100 MHz to 428 MHz at the positive edge of the trigger signal. Fig. 4.24 shows the response at the negative edge of the trigger signal.

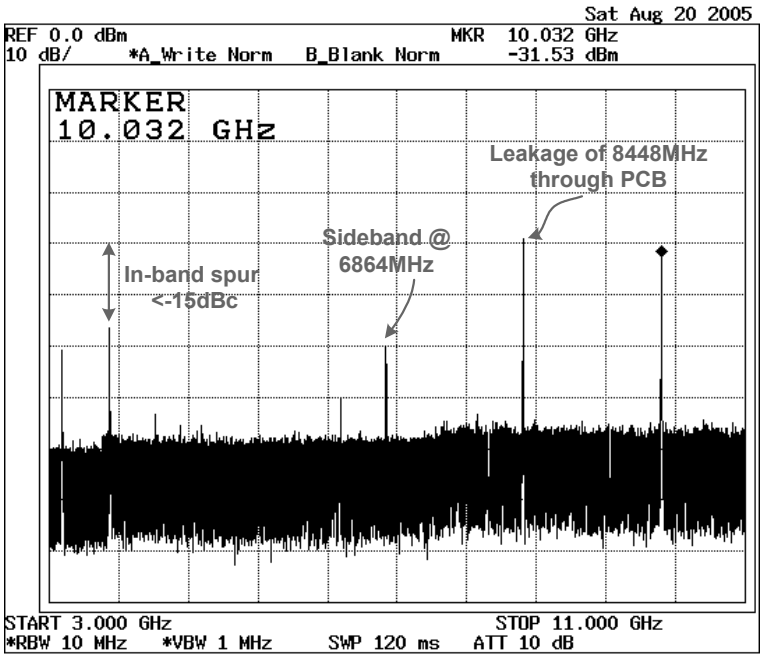

Fig. 4.22 Measured output spectrum for band #11. (© [2007] IEEE)

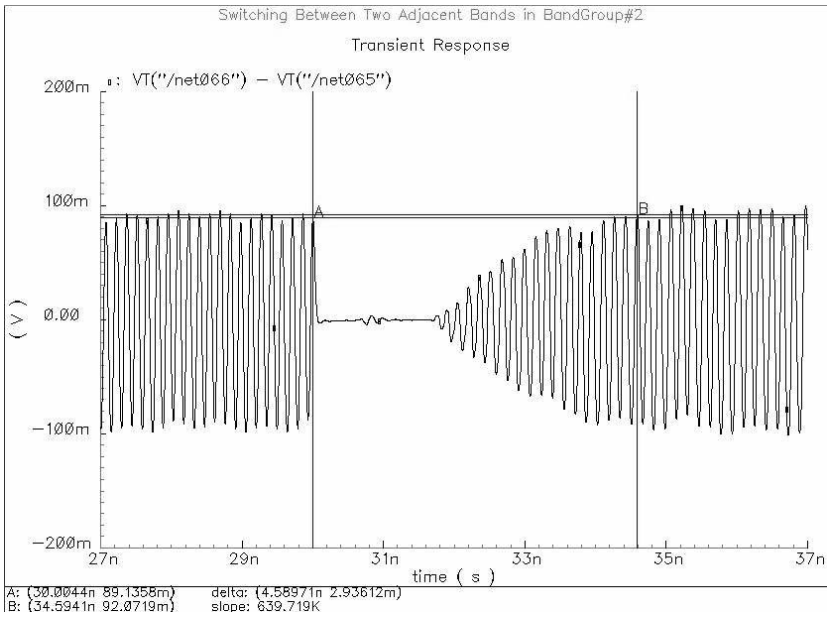

Fig. 4.23(a) Post layout simulation showing band switching.

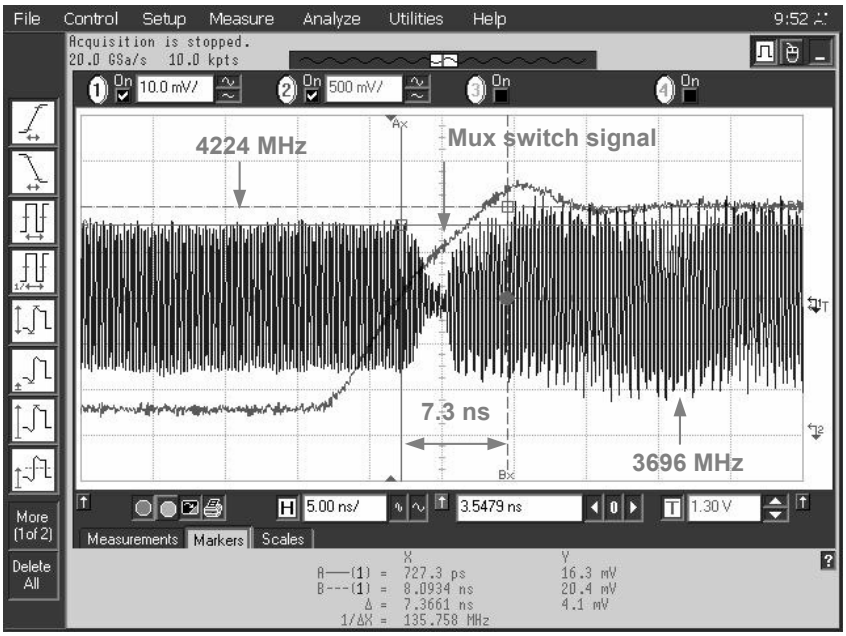

Fig. 4.23(b) Measured band switching from 4224 MHz to 3696 MHz.

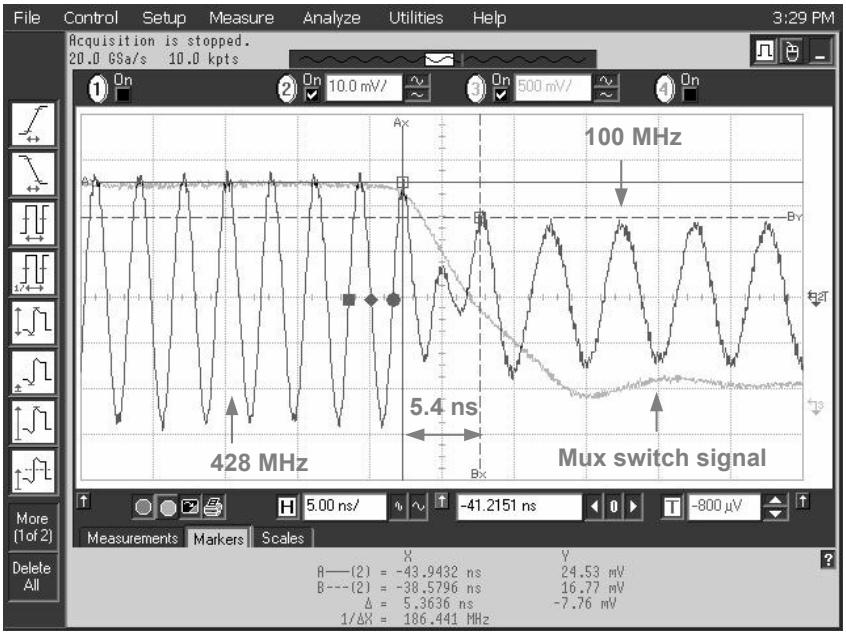

Fig. 4.24 Measured band switching at baseband of the receiver. (© [2007] IEEE)

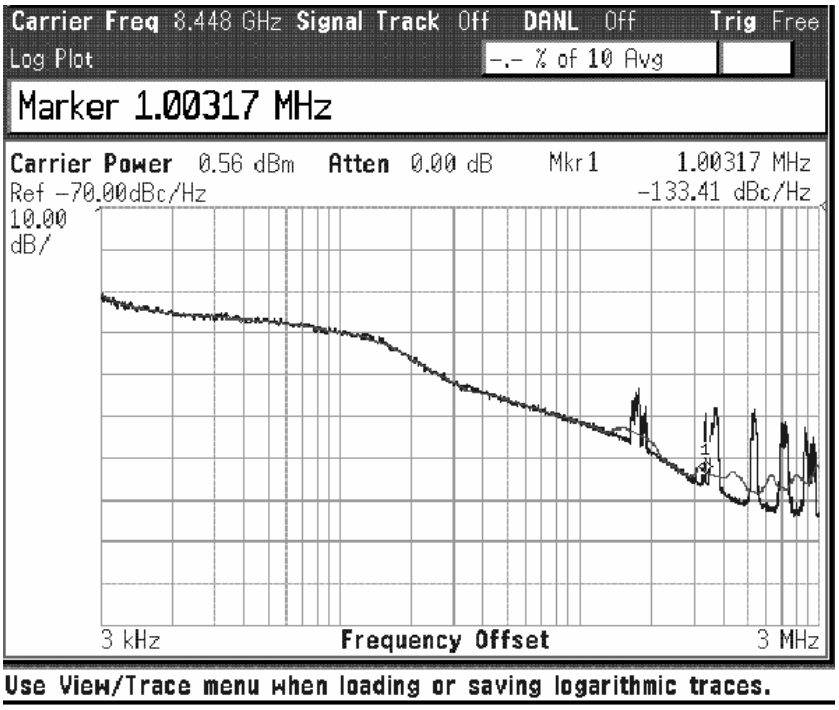

Fig. 4.25(a) Phase noise of the LO source at the input of the PCB.

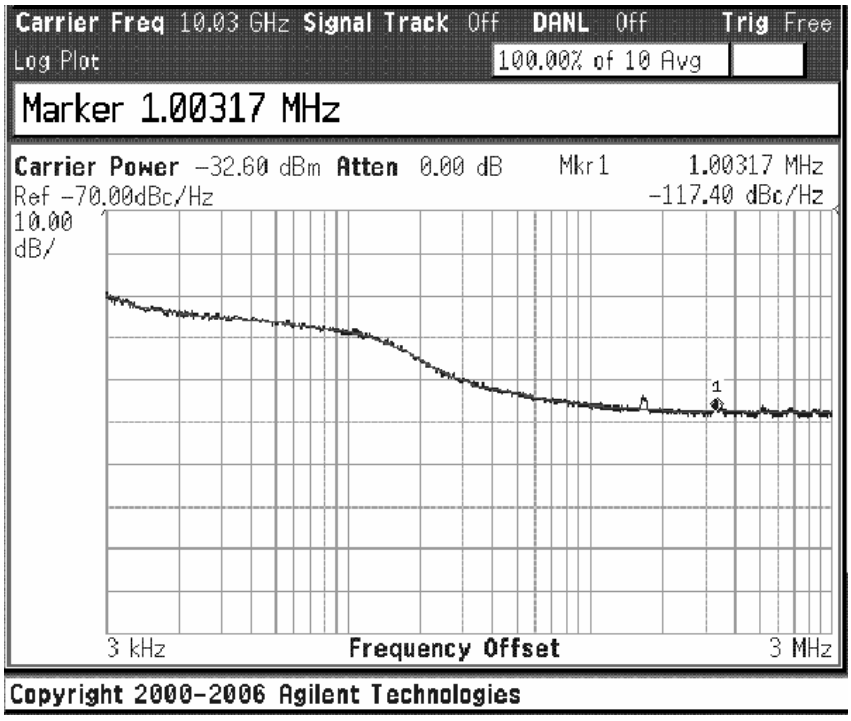

Fig. 4.25(b) Phase noise for band #11 at synthesizer output.

Figs. 4.25(a) and (b) show the single ended phase noise measurement of the input LO source and the synthesizer output for band#11 at 10 GHz. This shows the possible degradation that the phase noise of the LO source can undergo due to possible mixing and division. However, the degradation seems severe due to reduced carrier power. The degradation in the phase noise measured at 1 MHz offset for most frequencies is within 15 dB when compared to the phase noise of the source measured at the input of the PCB that is equal to -133.4 dBc/Hz. This degradation is partly due to reduced carrier amplitude at the output. Fig. 4.26 shows the I/Q mismatch at the output of the programmable gain amplifier of the receiver. To measure this mismatch the synthesizer produces a tone at 4224 MHz and the LNA input is set to 4304 MHz such that the

baseband frequency is 80 MHz. The observed phase mismatch is 2.1^{o} and the amplitude mismatch is 1.05 dB.

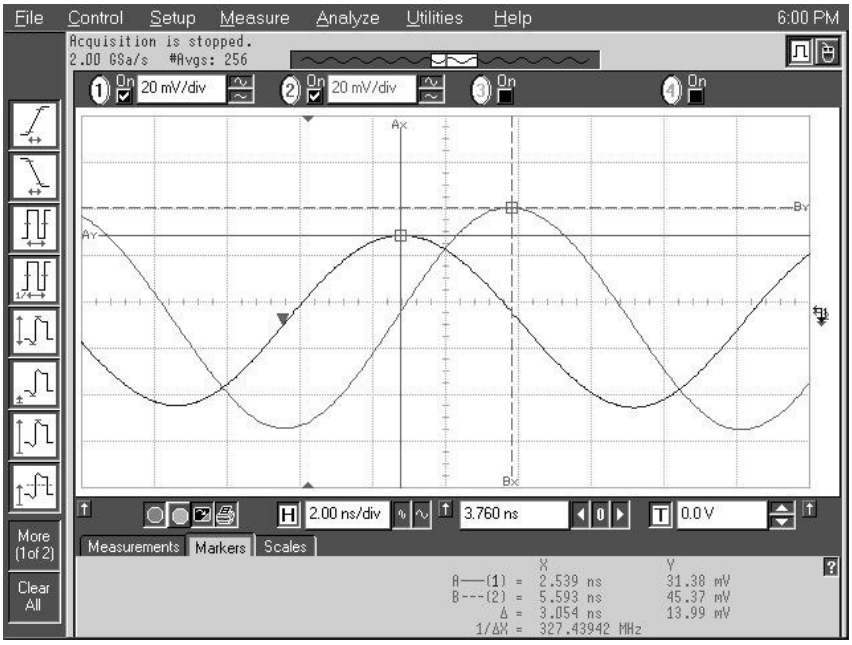

Fig. 4.26 I/Q mismatch at the baseband output of the receiver.

4.2.8 Summary

Contrary to all other implementations with the exception of [34] this implementation generates the maximum number of band frequencies in quadrature and extends the range up to 10 GHz. Unlike the previous implementation by the author [34], this system is integrated in a receiver and includes features such as low area (area in implementation [34] was 2.2 × 1.9mm^2) and low power with additional functionality such as test tone for notch filter tuning in the LNA. In the evolution of UWB frequency

synthesis solutions, the proposed implementation represents a step forward in the reduction of area and complexity with respect to the number of covered bands.

4.3 State of the Art and Comparisons

Table 4.2 summarizes the state-of-the art in UWB carrier frequency generators. Due to the varied nature of implementations as can be seen in Table 4.2 a direct comparison is not meaningful. Although 12 and 14-band solutions have been recently proposed but they are not practical in UWB radios due to the presence of the 802.11a interferers. Thus far, this work is the only synthesizer up to 10 GHz that is integrated in a UWB receiver and tested in a QFN package on a FR-4 PCB. The 14-band synthesizer is a stand-alone synthesizer and is not part of a UWB radio.

Table 4.2 Summary of state of the art in UWB carrier frequency generators

Reference	Range (GHz) (# of Bands)	Current @ Vdd	Area (mm^2)	Process / Peak f_T (GHz)
[18]	3.4 – 4.5 (3)	39mA@2.7V	1.1	0.25µm BiCMOS/70
[14]	3.4 – 4.5 (3)	20mA@1.5V	-	0.13µm CMOS/90**
[21]	3.4 – 4.5 (3)	10mA*@1.8V	0.68	0.18µm CMOS/50**
[19]	3.4 – 8 (7)	21.8mA@2.2V	1.43	0.18µm CMOS/50**
[22]	3.4 – 8 (7)	46mA*@2.7V	4	0.18µm BiCMOS/90
This Work I	3.7 – 10 (11)	75mA*@3V	4.18	0.25µm BiCMOS/47
This Work II	3.7 – 10 (11)	80mA*@2.5V	2.25	0.25µm BiCMOS/47
[37]	3.4 - 9.3 (12)	42.7mA @1.1V	-	90nm CMOS/140**
[38]	3.4 – 10.3 (14)	90mA @1.8V	1.524	0.18µm CMOS/50**

* Without VCO and/or PLL. **Estimated from [39]

CHAPTER V

MULTIBAND VCO BASED UWB FREQUENCY SYNTHESIZER

5.1 Introduction

Most of the existing synthesizer solutions use one of the following three approaches (i) multiple VCOs/PLLs, (ii) multiple VCOs along with division, SSB mixing and multiplexing and (iii) single VCO operating at a single frequency along with division, SSB mixing and multiplexing. The diversity in these implementations can be seen from Table 5.1, which presents the number of different components used by these synthesizers. The last of the three approaches is more preferable due to reduced number of PLLs required in the system, which reduces lot of implementation issues. However, the complexity is still high for synthesizers spanning the entire 3-10 GHz range. Furthermore, the power consumption and area of these synthesizers tend to be a significant part of the entire UWB transceiver. Hence, there is still the need for low complexity low power synthesizer solutions.

Table 5.1 Distribution of different building blocks in UWB synthesizers

References	VCOs	Dividers	SSB Mixers	Multiplexers	No. of Bands
[18]	2	3	1	1	3
[14]	3	0	0	1	3
[21]	1	3	3	0	3
[19]	2	3	1	2	7
[22]	1	8	2	2	7
[34]	1	5	5	2	11
[36]	1	5	3	4	11
[37]	1	5	2	3	12
[38]	2	2	3	2	14

UWB radio implementation in CMOS processes is desired due to its low cost and easy of integration. Low feature size CMOS technology has advantages such as high transistor f_T and low power operation but at the same time creates design challenges under low voltage operation [40]. This chapter explores the design of a 3-10 GHz UWB synthesizer in CMOS based on a single multiband VCO with the aim of reducing area, power and design complexity compared to existing solutions.

5.2 Frequency Plan and Synthesizer Architecture

The central idea is to eliminate as many mixing operations as possible during the generation of the carrier frequencies. From Table 5.1, it is evident that minimizing the number of mixing operations could translate to increase in the number of VCOs. It is also clear that the final SSB mixer that performs the frequency translation of the reference tone in a band group by 528 MHz is unavoidable. This is due to the requirement of a fast switching time within a band group. A possible synthesizer architecture that uses a single VCO and a single SSB mixer is shown in Fig. 5.1. It is based on a multiband wideband VCO that generates all the reference tones in the UWB spectrum according to the current band plan. A programmable divider in the feedback path always provides a division ratio such that the output frequency is equal to 528 MHz that is required for the final frequency translation. If the VCO gain is constant for the different reference tones then the loop dynamics remain the same for the different frequencies and the loop needs to settle only for different band groups for which there is enough time. Hence, the switching time in this case is not limited to the loop settling.

The architecture seems very simple and has the potential of being a very efficient solution. Next, some of the important challenges are discussed that ultimately demand frequency planning.

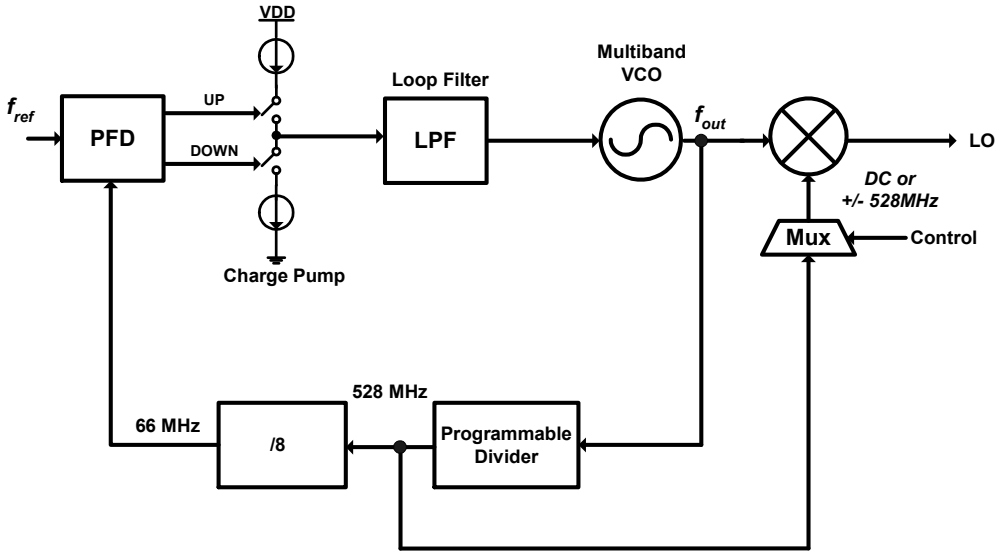

Fig. 5.1 Possible multiband VCO based UWB synthesizer solution.

The multiband VCO in this architecture needs to cover a very wide range almost 6.4 GHz as shown in Fig. 5.2. This is a very wide range even though the VCO does not need to tune continuously. Hence, a frequency plan is proposed to relax the tuning range of the VCO. This is achieved by translating the reference tones at lower frequencies to higher frequencies such that the new set of reference tones are closely spaced as shown in Fig. 5.2. This reduces the frequency range requirement of the VCO from 6.4 GHz to 4 GHz. Instead of directly generating 3960 MHz and 5544 MHz from the VCO, they are indirectly generated from 7920 MHz and 11088 MHz by using a divide by 2. Since the

use of band group #2 is impractical due to the presence of strong 802.11a interferers, the VCO frequency range could be further reduced to 3.2 GHz.

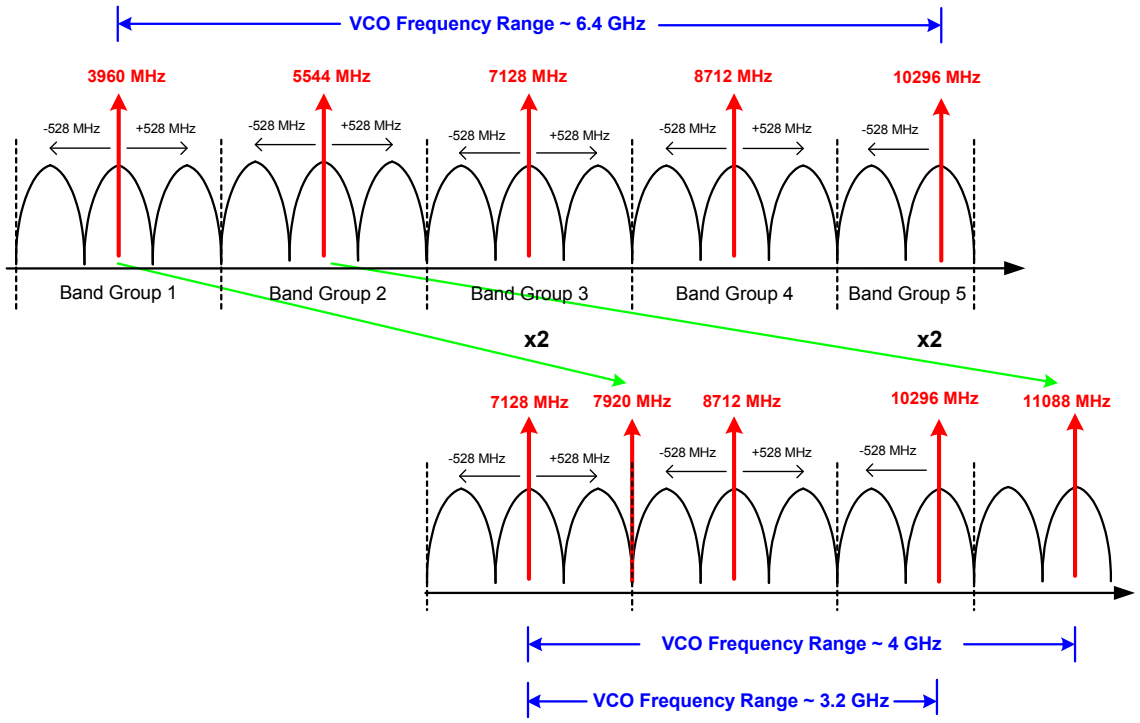

Fig. 5.2 Frequency plan to relax the requirements of the multiband VCO.

After having set the VCO range, the next step is to synthesize 528 MHz from the different reference tones from the VCO without using additional mixing. Table 5.2 shows the frequency synthesis procedure. An important fact is that the SSB mixer performing the final mixing requires a 50% duty cycle 528 MHz tone to reduce the possibility of spur generation. By having the programmable divider to be an integer only divider a 50% duty cycle 528 MHz tone can be easily generated and the implementation will be simple. However, since direct division of the reference tones to realize 528 MHz

always results in a fraction, a common factor of 1.5 is used to reduce each of the divisors to an integer (even or odd) as shown in Table 5.2. This implies that each of the reference tone is first divided by 1.5 and is then followed by a programmable division to synthesize 528 MHz. The ratio f/F is the intermediate frequency created after division by 1.5. The resulting frequency synthesizer architecture is shown in Fig. 5.3.

Table 5.2 Frequency synthesis.

Reference Tone (f) (MHz)	f/528 (N)	N=F*I (Fraction*Integer)	f/F or 2f/3 (Fraction = 1.5)
3960	7.5	1.5*5	2640
5544	10.5	1.5*7	3696
7128	13.5	1.5*9	4752
8712	16.5	1.5*11	5808
10296	19.5	1.5*13	6864
7920 (3960*2)	15	1.5*10	5280
11088 (5544*2)	21	1.5*14	7392

The proposed frequency synthesizer features a multiband quadrature voltage controlled oscillator (QVCO), a dual-mode divide by 2/buffer, a fixed divide by 1.5 circuit, a programmable integer divider, quadrature generation circuit, multiplexer and a SSB mixer. Due to the reduced number of divisions and SSB mixing this architecture will consume less area and power. The synthesizer is designed in a 130nm CMOS process.

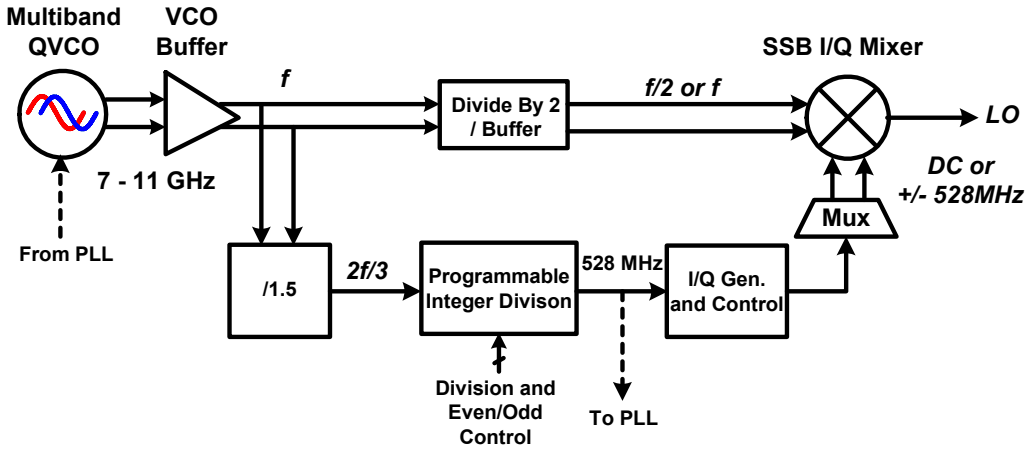

Fig. 5.3 Proposed CMOS UWB frequency synthesizer.

5.3 Multiband Quadrature VCO

As was mentioned in the previous section a multiband QVCO is at the heart of the proposed frequency synthesizer architecture. Before delving into the architectural description of the VCO, it is important to understand the need for a QVCO. From the frequency plan in Fig. 5.2 it is clear that the VCO needs to cover a range from 7.1-11.1 GHz or 7.1-10.3 GHz depending on whether or not band group #2 is used. Now since the carrier frequencies for the UWB radio need to be in quadrature and also the usage of SSB mixer requires that too, this leads to two options (i) a VCO ranging from 14-22 GHz followed by a divide by 2 or (ii) a quadrature VCO covering the 7-11 GHz range. It is obvious that generating frequencies by division puts a stringent tuning range requirement on the VCO even though continuous tuning range is not required. Hence, the option of using a quadrature VCO is chosen.

5.3.1 Possible Topologies

There have been various topologies proposed to realize wideband VCOs [41], [42], and [43]. All of them are wideband in nature while providing almost continuous tuning in the tuning range. In this particular case, we need broadband discrete tuning and a quadrature realization with less passives. The architecture described next is derived from [44], which allows for wideband operation and provides good quadrature accuracy.

5.3.2 Multiband QVCO

The schematic of the multiband quadrature VCO is shown in Fig. 5.4. The figure shows only one of the two VCO circuits of the QVCO. The VCO core is composed of a cross-coupled NMOS pair (M1 and M2) and series coupling PMOS transistors (M3 and M4). A PMOS current mirror is used for less flicker noise contribution. This topology is suitable primarily because it allows the use of a non-center tapped circular inductor and reduces the need for four inductors as in conventional quadrature VCO circuits [44]. In this particular case, only discrete frequency bands are needed and hence the wide band operation is achieved using switched metal-insulator-metal (MIM) capacitors of the process. Three bit tuning with scaled MIM capacitors are used. A $P^{+}N$ well junction varactor is used for fine-tuning and to account for process variations.

The coupling factor α is defined as the ratio of the coupling transistors (PMOS in this case) to that of the switching transistors (NMOS in this case). An α of 3 was chosen in this design [44] as a good compromise between phase noise and tuning range. The inductor used in this design is a 870 pH non center-tapped inductor.

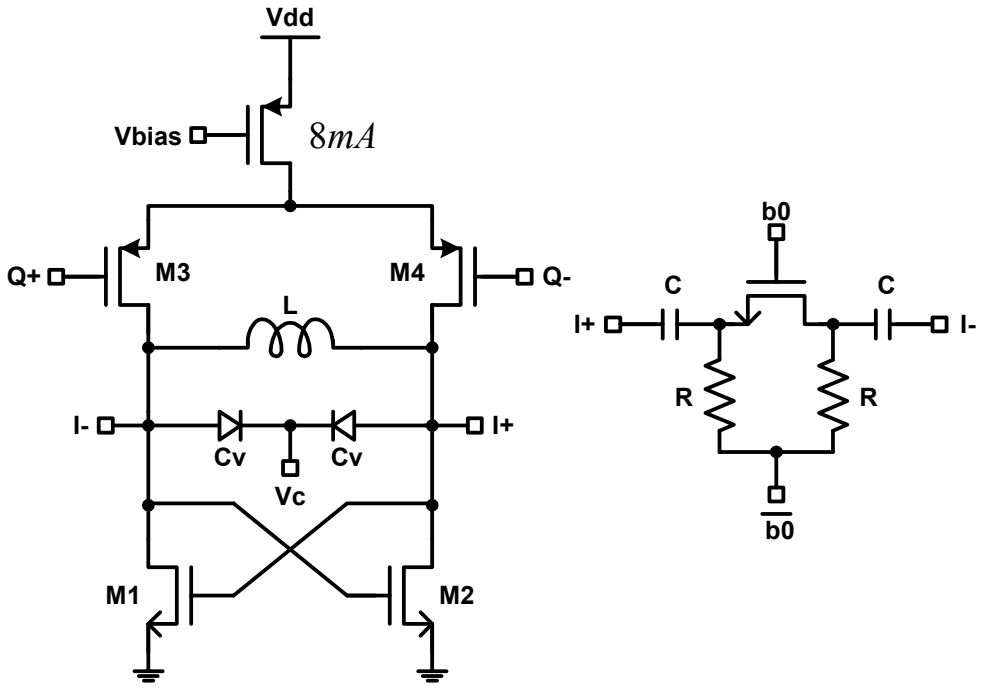

Fig. 5.4 Half-section of the multiband quadrature VCO.

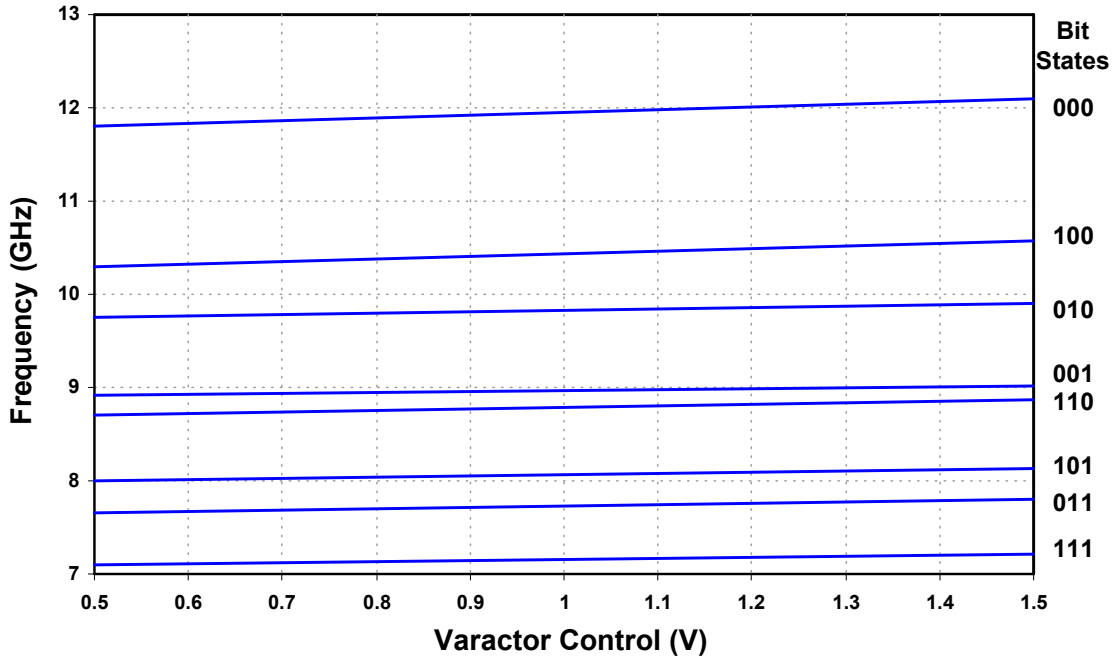

Fig. 5.5 Simulated frequency tuning of the VCO.

Post layout simulation results show that this circuit can almost cover the required range (Fig. 5.5) except for band group #2. However, with the use of a center-tapped inductor and with accurate modeling of the passives all the reference tones could be covered by this VCO. Fig. 5.6 shows the simulated phase noise for different reference frequencies. The phase noise is better than -98 dBc/Hz for most of the frequencies, which is better than the requirement according to Chapter III. The structure could be further improved by including an amplitude control mechanism to ensure less variation in phase noise over the bands. Furthermore, switched current mirrors could be used to control the amplitude over different band groups. The QVCO operates from a 1.5 V supply and draws 8 mA per VCO.

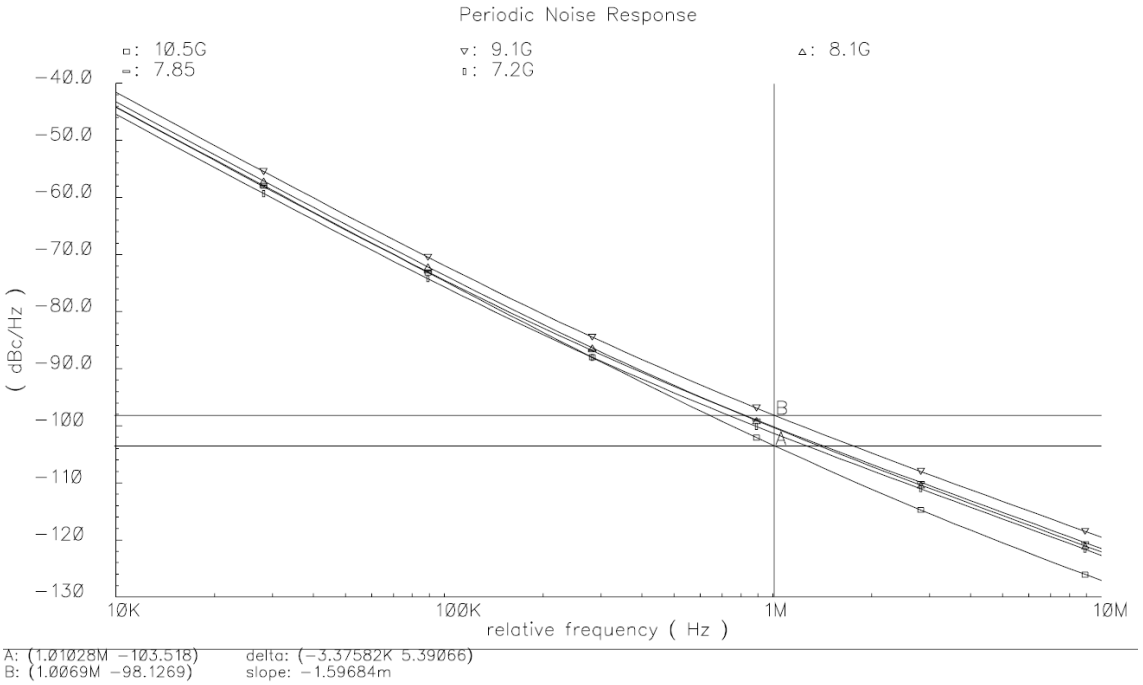

Fig. 5.6 Simulated phase noise performance for different VCO frequencies.

5.4 Divide by 1.5

In this particular synthesizer architecture, the requirement of a divide by 1.5 circuit was stressed in section 5.2. A divide by 1.5 structure can be conventionally built [45] but however, not with 50% duty cycle, which is critical in driving the next stage, which is a divider, based on 50% duty cycle clocks. Furthermore, standard CMOS static logic based dividers are difficult to operate at the VCO frequency, which in this particular case is 7-11GHz. Hence, the need for a analog multiplier based regenerative Miller divider [46]. Fig. 5.7 shows the block diagram of the divide by 1.5 circuit. A SSB mixer with a programmable band pass load is used along with a buffer and CML based divide by 2 in the feedback path.

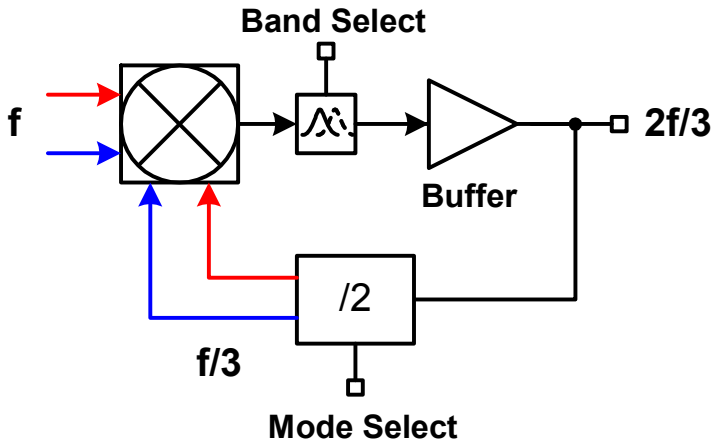

Fig. 5.7 Conceptual block diagram of the divide by 1.5 circuit.

A common source buffer isolates the capacitance from the divider as well as the integer programmable divider that the divide by 1.5 circuit drives thereby providing more tuning range to the LC load. The divide by 2 circuit generates signals in

quadrature, which mix with the quadrature signals at the SSB mixer input and allow the divide by 1.5 frequency to be produced at the output provided there is enough loop gain at that frequency [47]. The programmable band pass load further augments the loop gain for different frequencies by providing selectivity and thereby guarantees finite loop gain. This also results in a spectrally pure tone at the output.

5.4.1 Multiband Single Sideband Mixer

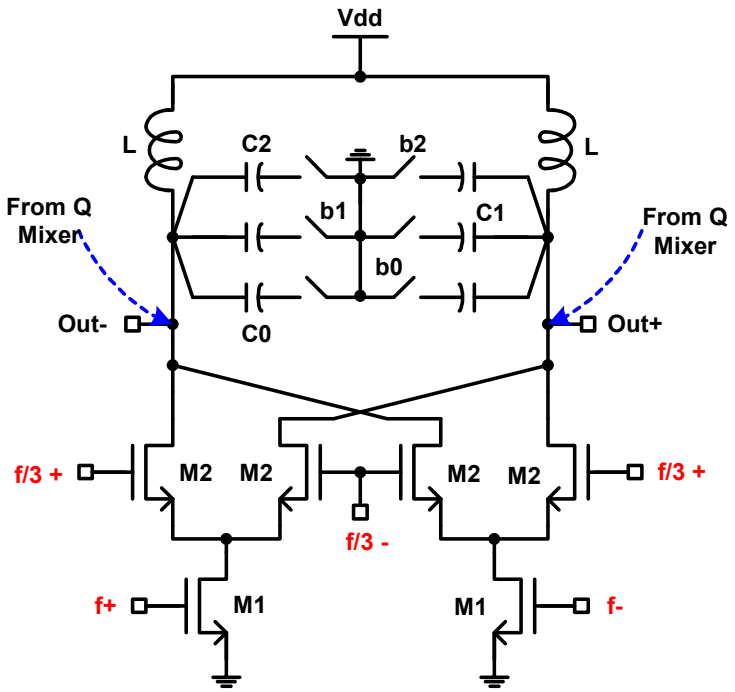

Fig. 5.8 SSB mixer with programmable multiband load (Only half section shown).

Fig. 5.8 shows the circuit schematic of the SSB mixer with LC tank composed of spiral inductors and MIM capacitor bank. Both the *I* and *Q* mixers share the same band pass load. In Fig. 5.8 only the *I* mixer is shown. With three bits of tuning, the entire

range (4.7 – 7.4 GHz from Table 5.1) can be covered. Fig. 5.9 shows the load impedance variation of the SSB mixer for different tuning words. This tuning range allows to compensate for process variations. With the availability of a center-tapped inductor the number of inductors could be further reduced.

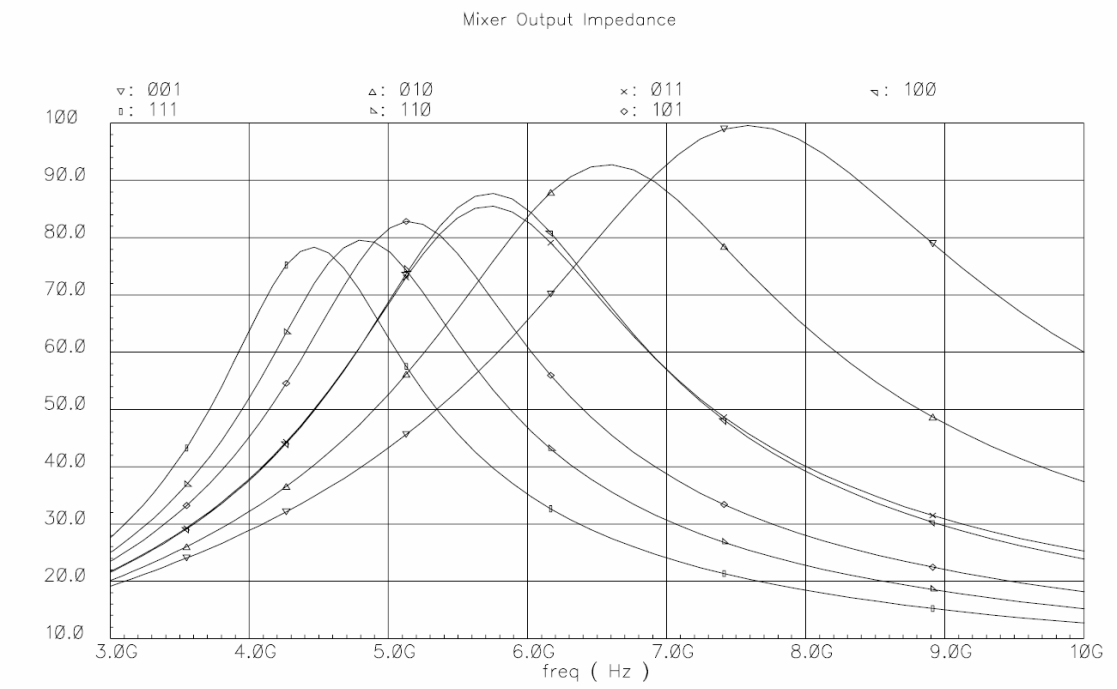

Fig. 5.9 Tuning of the band pass load of the SSB mixer.

The output of the mixer depends on the phase relation of the signals appearing at its two inputs (i.e. *f* and *f/3*). For example if the in-phase or the quadrature-phase of either of the two inputs are exchanged a different sideband is obtained. This is explained via expressions (5.1) and (5.2) as follows:

$$\cos(\omega t)\cos\left(\frac{\omega t}{3}\right)+\sin(\omega t)\sin\left(\frac{\omega t}{3}\right)=\cos\left(\frac{2\omega t}{3}\right) \tag{5.1}$$

$$\sin(\omega t)\cos\left(\frac{\omega t}{3}\right)+\cos(\omega t)\sin\left(\frac{\omega t}{3}\right)=\sin\left(\frac{4\omega t}{3}\right) \tag{5.2}$$

This is a practical problem and is referred to as phase ambiguity in a quadrature VCO. The *I* and *Q* outputs of the VCO could be swapped depending on startup conditions [48]. To guarantee the desired sideband at the mixer output there has to be a way to swap the other input as shown below:

$$\sin(\omega t)\sin\left(\frac{\omega t}{3}\right)+\cos(\omega t)\cos\left(\frac{\omega t}{3}\right)=\cos\left(\frac{2\omega t}{3}\right) \tag{5.3}$$

This is realized by having a provision of either having the original or the swapped outputs from the divider. The next section explains the operation of such a divider. Such ambiguity occurring in the final mixer can be corrected using the multiplexer that can swap the 528 MHz *I* and *Q* tones easily. Detection of the above-mentioned ambiguity in the chip could be done via power detectors and/or comparators. However, such a system to automatically detect and correct for this ambiguity has not been implemented here.

5.4.2 Dual-Mode Divider

A conventional divider based on two flip-flops in feedback configuration is shown in Fig. 5.10(a) along with its waveforms. In normal operation, the output of the second flip-flop follows that of the first flip-flop. By swapping the connections of the outputs of the first flip-flop to the input of the second flip-flop the outputs of the two flip-flops are swapped as shown in Fig. 5.10(b). Now integrating the two modes into one circuit would implement the capability of choosing one or the other depending on the

mode select signal in Fig. 5.7. A circuit implementation that was reported in [49] has been used here.

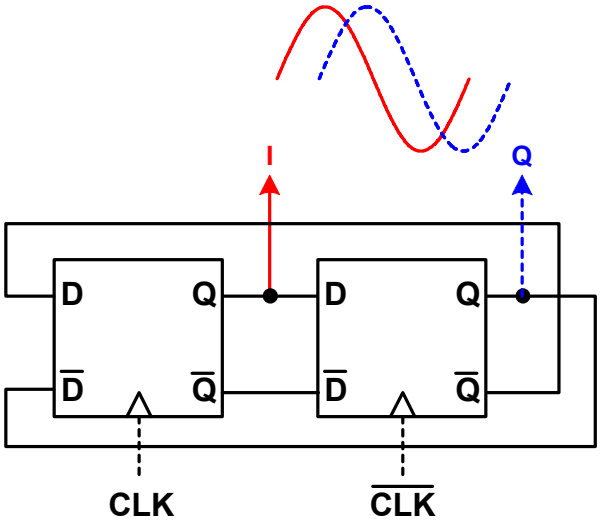

Fig. 5.10(a) Divide by 2 circuit in the normal mode.

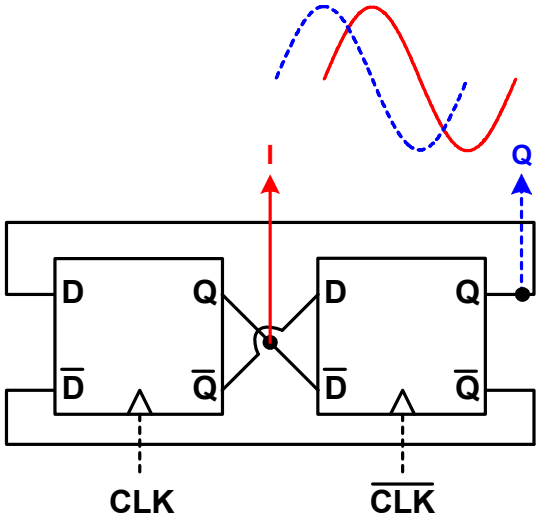

Fig. 5.10(b) Divide by 2 circuit in the alternative mode.

5.5 50% Duty Cycle Programmable Integer Divider

Following the divide by 1.5 circuit there is a programmable integer divider that translates all input frequencies to 528 MHz. This is explained in Table 5.2. The key idea is explained in [50]. The divider generates 50% duty cycle at even and odd division ratios. The division ratio N is related to the number of flip-flops K by

$$N = 2K - P \tag{5.4}$$

where P is 0 for even division and is 1 for odd division.

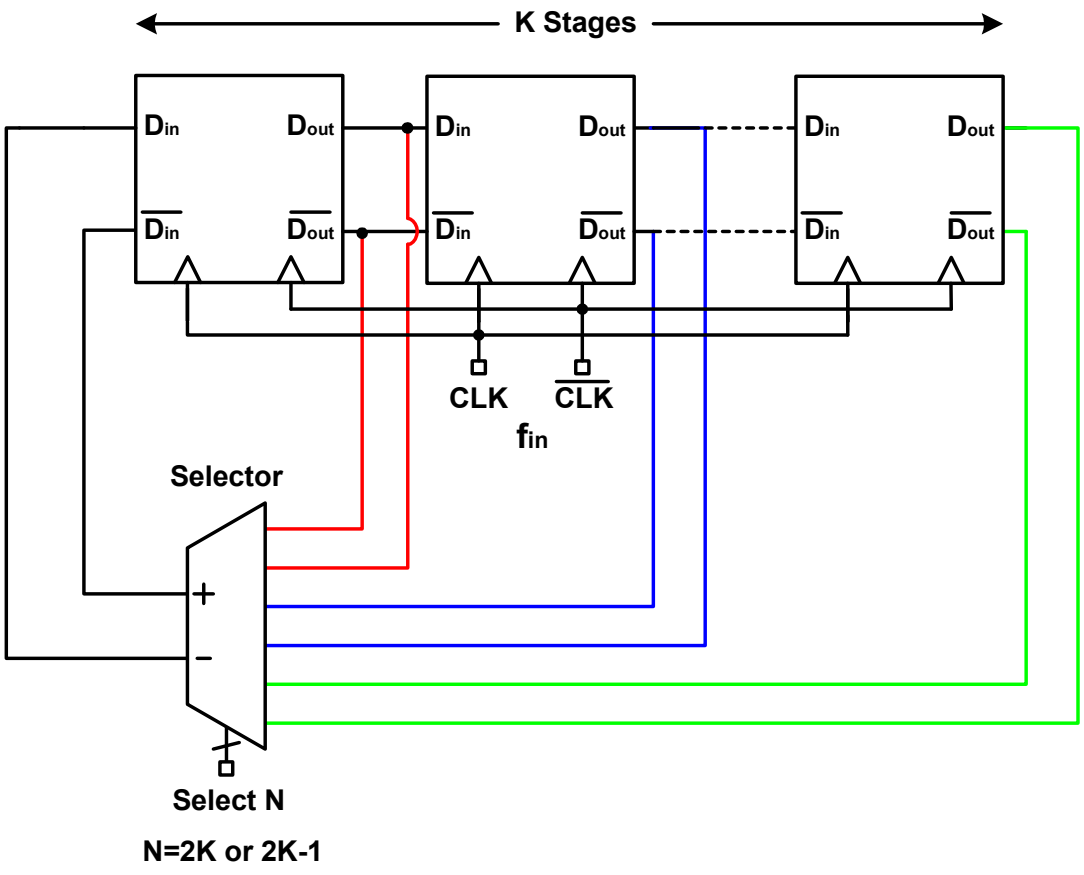

Fig. 5.11 50% duty cycle programmable integer divider.

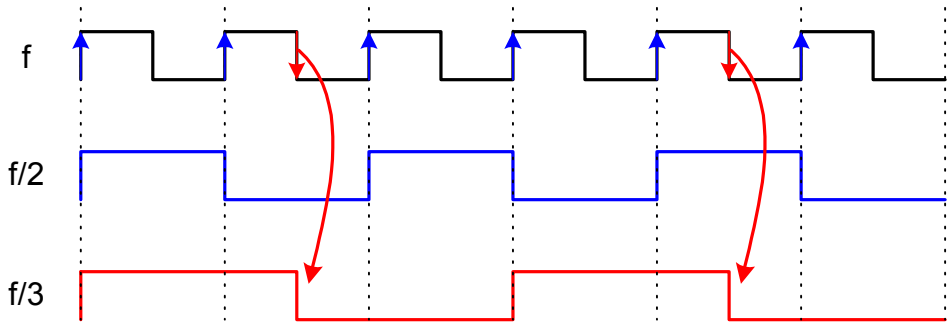

Fig. 5.12 Operating principle for even and odd division.

The operation principle of such a divider is explained next. Fig. 5.12 shows a clock signal and its divide by 2 and divide by 3 versions. It can be seen that for odd divisions with 50% duty cycle output, transition at both edges of the clock is essential, hence, there needs to be a mechanism by which the flip-flop changes its triggering point i.e. if it was triggering at positive edges of the clock it should be able to trigger at negative clock edges dynamically. This allows for the change of state at the middle of the input clock that is required to obtain 50% duty cycle. So, a double edge triggered master-slave flip-flop is required for this architecture. From Fig. 5.11 it can be seen that depending on the maximum division ratio the number of flip-flops in cascade are chosen. These flip-flops share the same input clock. The outputs of each of these flip-flops feed a multiplexer, the output of which feeds the *D* (data) input of the first flip-flop such that there is a negative feedback. The change in this input is reflected at the divider output. The outputs of any of these flip-flops can be used as the output of the programmable divider. For even division ratios, each of the flip-flops are configured such that they trigger only at one edge of the clock signal. For odd division ratios, each

of the flip-flops are configured such that they normally trigger on one edge of the clock signal and also trigger at the second edge of the clock signal if the mode is selected to indicate odd division (i.e. $P = 1$) and the outputs of the corresponding flip-flops are high. This makes intuitive sense because when output is high the next D input is low (negative feedback via the multiplexer) and triggering at the falling edge of the next clock would imply an odd division (assuming normal triggering was at rising edge). The number of delays for both even and odd division is determined by the multiplexer that decides which flip-flop's output is chosen. This provides programmable integer divisions.

5.5.1 Double Edge Triggered Flip-Flop

A double edge triggered master-slave flip-flop is at the heart of this implementation. A block diagram of the master-slave flip-flop along with its circuit implementation is shown in Fig. 5.13. According to [50], a separate dedicated circuitry is required to change the triggering of the flip-flop. In the presented flip-flop structure, the control circuitry is embedded into the flip-flop as shown in Fig. 5.12. The four transistors (M2) connected in between the clock and the data transistors implement the change in edge triggering. They act as switches to steer either the positive or negative clock signal to the (M3) data and latch transistors. This allows for the positive and negative edge triggering of the flip-flop. The signals *A* and *B* carry both bias as well as signal information. The signal information for each flip-flop is derived from its master-slave configuration's output. When *P*, the control signal is 1 the switches are on and all the M2 transistors share the same bias whereas when *P* is 0 the switches are off and only

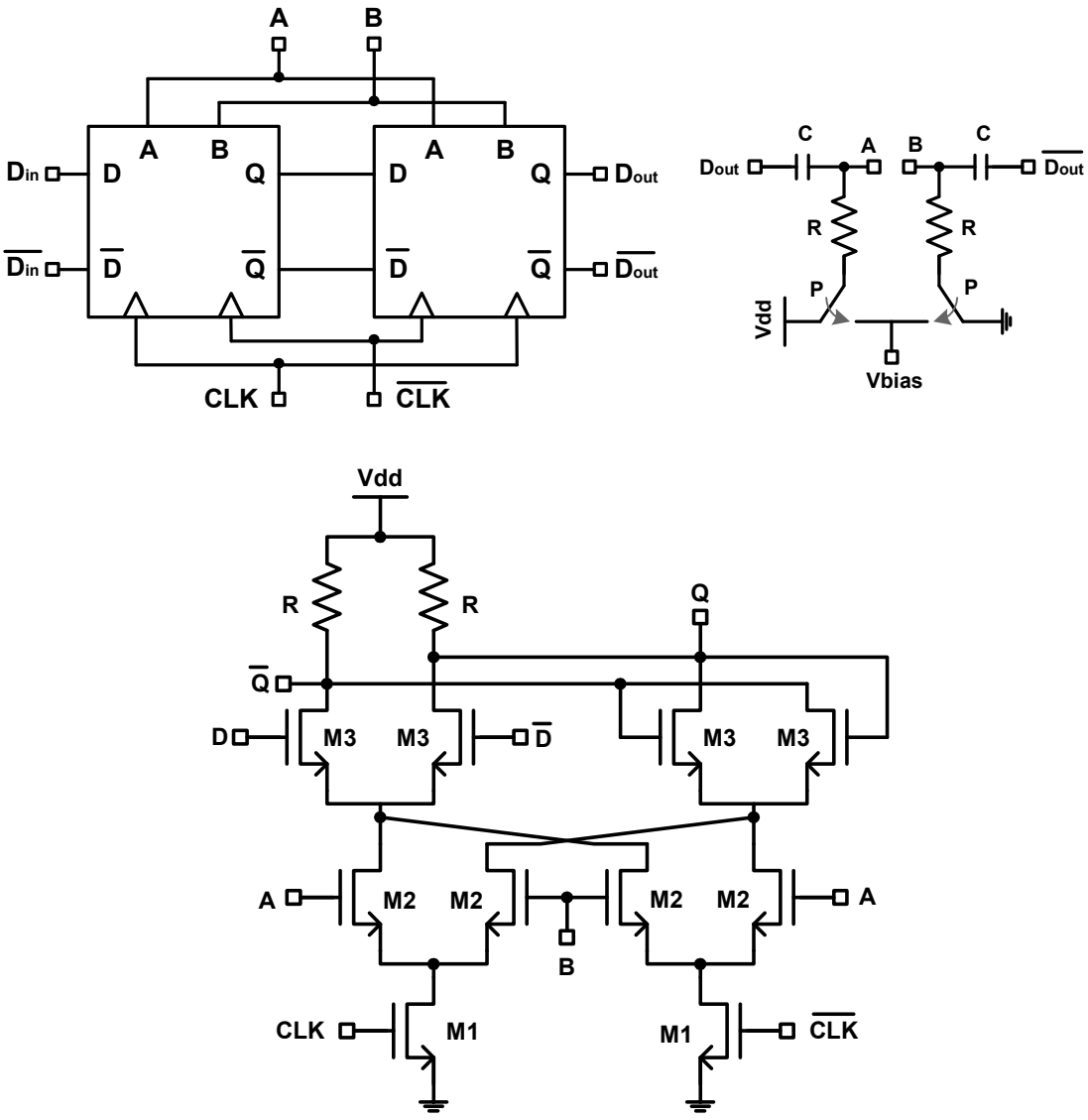

Fig. 5.13 Double edge triggered flip-flop.

two of the transistors are on and the other two are off. In the first case (odd division), the M2 transistors act like the current commuting cell in a Gilbert mixer and toggle or change the triggering direction only when the signal is high at one of the outputs. In the case of the divide by even integer, only two of the transistors are active there by

resulting in a structure similar to a conventional current mode logic based flip-flop. The signal at the output is limited so that none of the M2 transistors enter the on state due to the signal swing when there bias voltage is set to 0.

The programmable divider used in this implementation requires 7 master-slave flip-flops to provide integer division from 9 to 14. The multiplexer used here comprises of different cascode differential pairs sharing a common load (similar to Fig. 4.15 with resistive loads). AC coupling via RC high pass structure is used wherever required.

5.6 Other Circuit Blocks

There are certain other miscellaneous blocks in this synthesizer, which include:

(i) Phase shifter based (I/Q) generator: It comprises of first order RC-CR circuit with buffering, similar to those in the SiGe implementations [34, 36] explained in Chapter IV. This is required to generate quadrature signals at 528 MHz.

(ii) I-Q amplitude and phase compensator: This circuit follows the 528 MHz phase shifter and is similar to the one used in [49].

(iii) Multiplexer: Multiplexers based on multiple differential amplifiers sharing a common resistive load are used. Digital logic provides the switching between dc and 528 MHz signals (in-phase and anti-phase).

(iv) Divide by 2/Buffer: This is a current mode logic based divide by 2 along with a common source differential buffer. The circuit works in two modes i.e. either as a divide by 2 or as a buffer. This is possible by sharing the resistive loads between the two circuits. This enables to save power as only one of the circuits is used at a time.

(v) Single sideband I/Q mixer: The SSB *I*/*Q* mixer as has been discussed earlier is a structure comprising of two Gilbert cell based mixers. In this particular implementation resistive source degeneration is used for LO transistors to reduce the spurs due to non-linearity at the LO port. Most of the non-linearity is due to the harmonics of the 528 MHz tone which in this case serves as the LO signal in the mixer. Resistive degeneration is achieved for the LO transistors by splitting the RF transistors to avoid any voltage drop as was shown in [49].

5.7 Layout

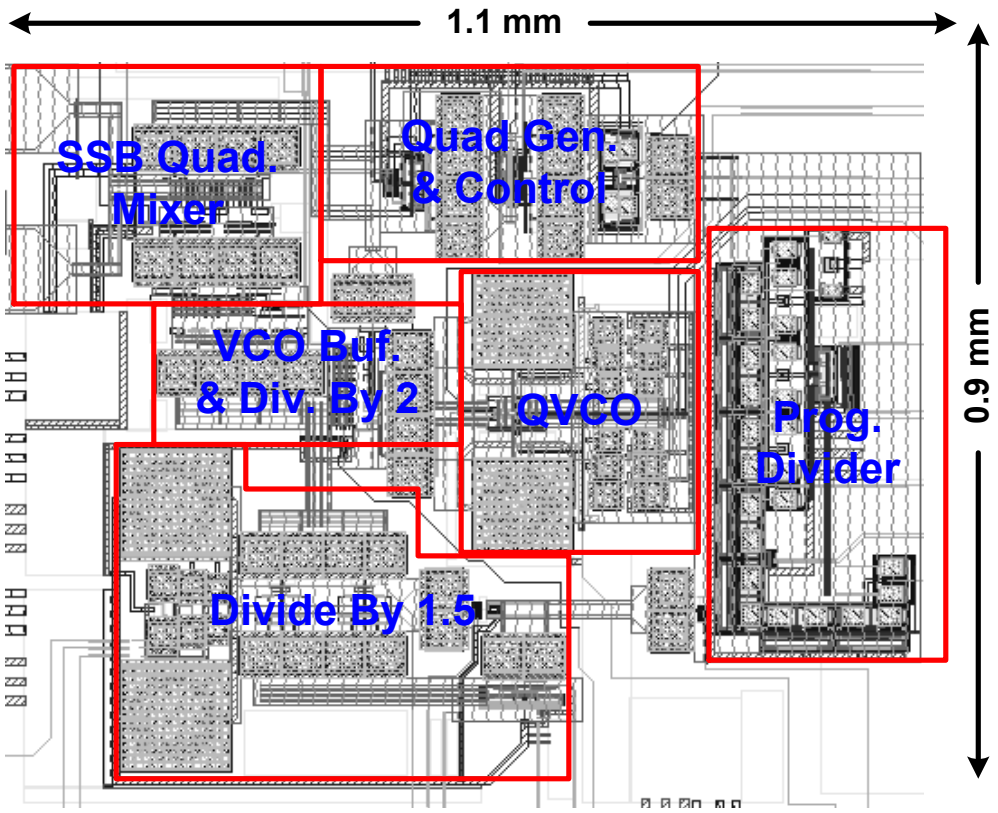

Fig. 5.14 Layout of the CMOS UWB synthesizer.

The circuits are implemented in UMC's 130nm CMOS technology. The layout of the chip is shown in Fig. 5.14. The active area is close to 1 mm^2. A total of 4 inductors are used in the entire design. It can be reduced to 3 by using symmetric center-tapped inductors. Top metal (metal 8) is used for the high frequency routing. Decoupling capacitors realized using MOS capacitors are used to reduce noise from supply and bias lines. Most of the sensitive RF circuits were isolated from the digital circuits by putting the circuits in n-well and by providing individual supply and ground pins to each of these circuits.

5.8 Simulation Results

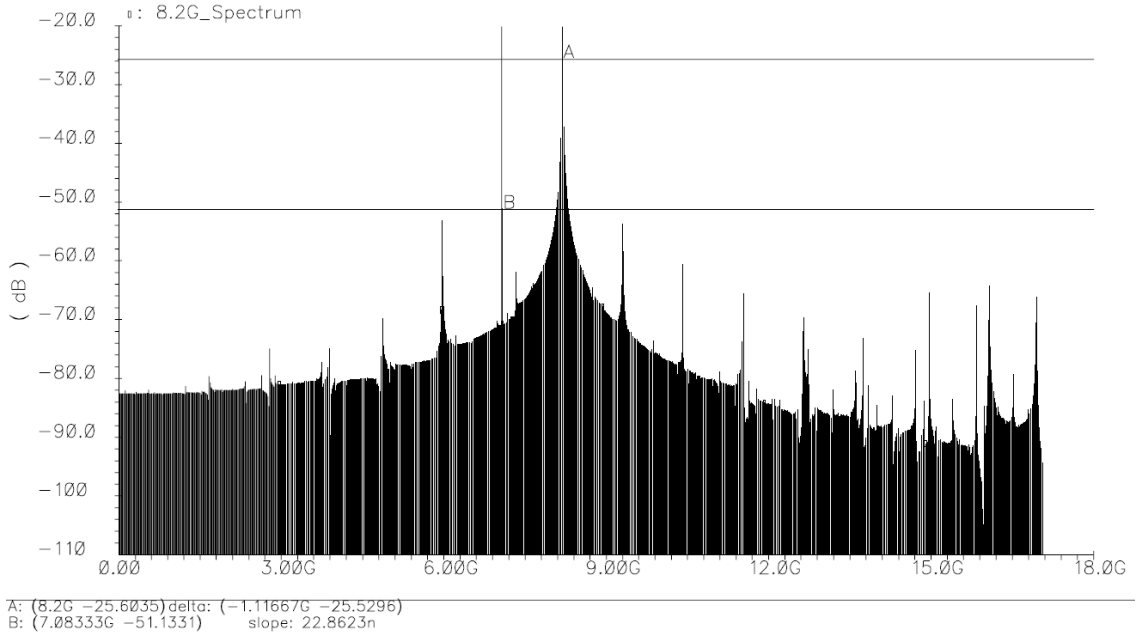

Fig. 5.15 Synthesizer output spectrum at 8.2 GHz (Band #10).

This section presents some post layout simulation results for the overall system after parasitic resistance, capacitance and inductance extraction. Fig. 5.15 shows the spectrum at 8.2 GHz, which is band #10. The sideband spurs are less than 25 dB. Fig. 5.16 shows the VCO output spectrum and the quadrature accuracy for the I and Q signals. The quadrature accuracy is very good at 8 GHz (close to 7920 MHz) which is reference tone for band group #1. Fig. 5.17 shows the transient switching of the 528 MHz signal. The switching time is less than 2 ns allowing for a very fast switching of the LO.

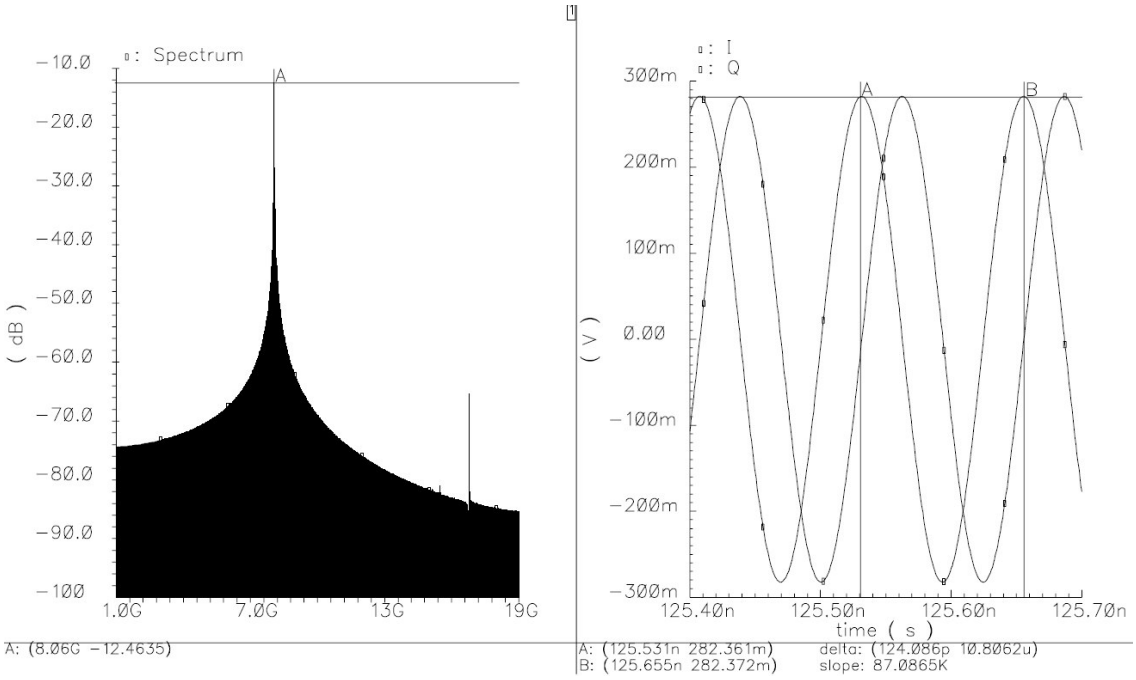

Fig. 5.16 VCO output spectrum and quadrature waveforms.

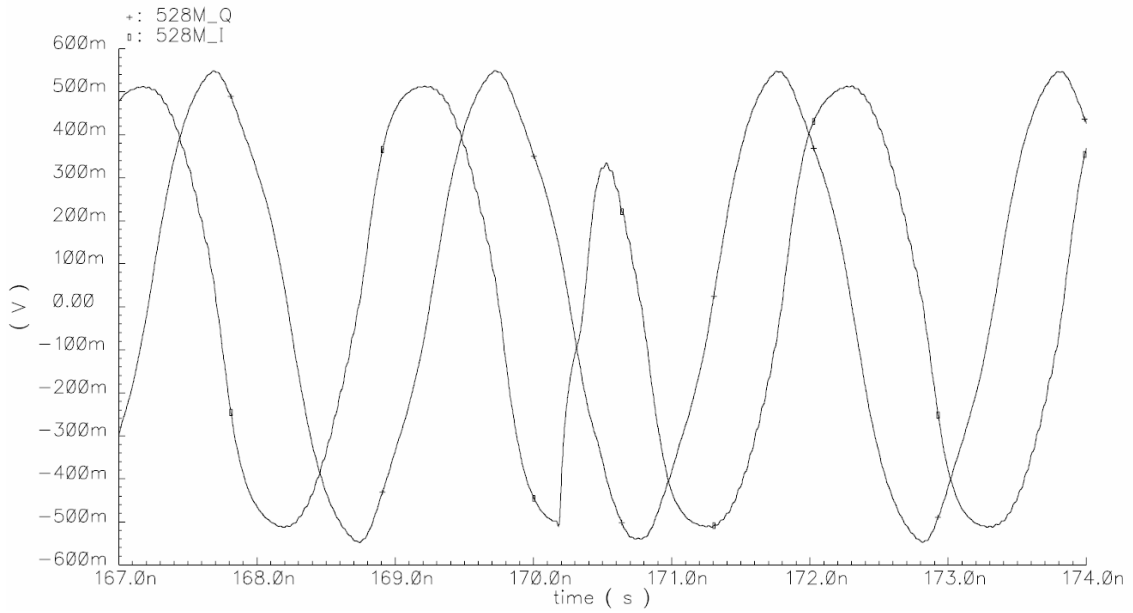

Fig. 5.17 Band switching at 528 MHz.

5.9 Summary

This section summarizes the key performance parameters of the frequency synthesizer presented in this chapter. Table 5.3 presents the performance summary. This architecture shows promise for full band UWB synthesizer realizations in digital CMOS processes with reduced complexity, area and power.

Table 5.3 Performance summary

Frequency range	3.1 – 10.6 GHz (Except the U-NII Band)
Spur power level	< -25 dBc across all bands
Band hopping time	< 2 ns
Phase noise	-98 dBc/Hz to -103 dBc/Hz @ 1 MHz
Active area	<1 mm^2
Power	90 mW from 1.2V/1.5V

CHAPTER VI

CONCLUSIONS

The increased congestion in the radio frequency spectrum up to 5GHz has resulted in a growing interest in higher frequency bands. This has spurred significant activity in the UWB spectrum that spans from 3.1-10.6 GHz. Furthermore, UWB communication enables information transfer at very high data rates within short distances.

6.1 Summary

In this dissertation, system and circuit design of carrier frequency synthesizers for 3-10 GHz MB-OFDM based UWB radios are presented. First, specifications for a 3-10 GHz UWB frequency synthesizer are presented based on system level simulations for both QPSK and 16-QAM modulated OFDM carriers used for UWB communication. Special attention is paid to spurious tones generated during the frequency generation process and rigorous system level analysis is performed to evaluate various non-idealities from a circuit implementation. These top-level simulations help in frequency planning and choosing the suitable synthesizer architecture. Based on the above analysis a frequency band plan is proposed that greatly relaxes the design of the frequency synthesizer. Various possible synthesizer architectures are proposed, analyzed and compared at system level to gain further insight.

Based on the proposed frequency plan, two different 11-band frequency synthesizers are designed, implemented and tested making them one of the first 3-10 GHz frequency synthesizers for UWB covering 78% of the licensed spectrum. The circuits are implemented in a 0.25μm SiGe BiCMOS process. The architectures are based on a single VCO at a fixed frequency followed by an array of dividers, SSB mixers and multiplexers to generate the 11 required bands in quadrature. The synthesizers demonstrate very fast hopping times with acceptable spurious performances.

Finally, an architecture for a 3-10 GHz UWB synthesizer is proposed that relies on a single multiband quadrature VCO, a programmable integer divider with 50% duty cycle and SSB mixers. This architecture provides a very compact low power solution that is suitable for implementation in deep submicron technologies.

6.2 Recommendations for Future Work

Different ways of implementing a frequency synthesizer for a MB-OFDM Radio are presented in this dissertation. Significant challenges still exist in terms of implementation in small feature size technologies, under low voltage-low power operation constraints while using minimum passives.

The architectures presented in chapter IV can be realized in a pure digital CMOS process. Further improvements in power consumption could be achieved in a finer CMOS technology with large f_T. The Gilbert cell based SSB mixers could be replaced with passive mixers for power saving and for operation with low supply voltages.

The architecture presented in Chapter V is very well suited for a fast digital process. But, in order to further minimize the passives, the VCO could be a ring oscillator type. Although, this would require slightly more power for the same phase noise, it would definitely be more easily tunable as compared to LC based VCOs. However, depending on the spectral purity of signals from ring oscillators, additional filtering may or may not be required to provide a clean signal at the input of the SSB mixer. Another motivation for using a ring oscillator is the each with quadrature phases are generated and the lack of phase ambiguity as compared to LC based quadrature VCOs.

In the future as more and more communication standards find there way into a cellular device, the requirement on the LO signal will get more and more stringent especially in terms of the frequency of operation, tuning range and other specifications. Intelligent frequency planning and synthesizer architectures would be required to minimize the number of LO sources or VCOs on the same die and as well as to reduce the complexity of the synthesizer realization.

In conclusion, this dissertation has opened different possible research directions in the design and implementation of multiband multi-mode radios especially, in the task of efficient LO generation.

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APPENDIX

From Fig. 3.14, the sideband rejection ratio (SBRR) can be derived as follows:
The output of each mixer is given by

$$V_1 = \frac{1}{2}\left[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t\right] \tag{A.1}$$

$$V_2 = \frac{1}{2}\left[\cos(\omega_1 t - \omega_2 t + \phi_1 - \phi_2) - \cos(\omega_1 t + \omega_2 t + \phi_1 + \phi_2)\right] \tag{A.2}$$

V_3 is a scaled version of V_1 with the amplitude error and is given by

$$V_3 = \frac{1}{2}(1 + \Delta A)\left[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t\right] \tag{A.3}$$

Adding V_2 and V_3 at the output we have

$$V_2 + V_3 = \frac{1}{2}(1 + \Delta A)\cos(\omega_1 - \omega_2)t + \frac{1}{2}\cos(\omega_1 t - \omega_2 t + \phi_1 - \phi_2)$$

$$+ \frac{1}{2}(1 + \Delta A)\cos(\omega_1 + \omega_2)t - \frac{1}{2}\cos(\omega_1 t + \omega_2 t + \phi_1 + \phi_2) \tag{A.4}$$

The fundamental tone and the sideband are given by

$$V_{Fund} = \frac{1}{2}(1 + \Delta A)\cos(\omega_1 - \omega_2)t + \frac{1}{2}\cos(\omega_1 - \omega_2)t\cos(\phi_1 - \phi_2) \tag{A.5}$$

$$- \frac{1}{2}\sin(\omega_1 - \omega_2)t\sin(\phi_1 - \phi_2)$$

$$V_{SB} = \frac{1}{2}(1 + \Delta A)\cos(\omega_1 + \omega_2)t - \frac{1}{2}\cos(\omega_1 + \omega_2)t\cos(\phi_1 + \phi_2) \tag{A.6}$$

$$+ \frac{1}{2}\sin(\omega_1 + \omega_2)t\sin(\phi_1 + \phi_2)$$

SBRR is a ratio of the power level of the desired (fundamental) signal to that of the sideband and hence only the power of the signals at the fundamental and the sideband is required.

$$\left|V_{Fund}\right|^2 = \frac{1}{4}\left\{\left[(1 + \Delta A) + \cos(\phi_1 - \phi_2)\right]^2 + \sin^2(\phi_1 - \phi_2)\right\} \tag{A.7}$$

$$\left|V_{SB}\right|^2 = \frac{1}{4}\left\{\left[(1+\Delta A)-\cos(\phi_1+\phi_2)\right]^2+\sin^2(\phi_1+\phi_2)\right\} \tag{A.8}$$

Hence the sideband rejection ratio (SBRR) is given by

$$SBRR = 10\log\frac{\left|V_{Fund}\right|^2}{\left|V_{SB}\right|^2}10\log\left[\frac{1+(1+\Delta A)^2+2(1+\Delta A)\cos(\phi_1-\phi_2)}{1+(1+\Delta A)^2-2(1+\Delta A)\cos(\phi_1+\phi_2)}\right] \tag{A.9}$$

VITA

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