BROADBAND RF FRONT-END DESIGN FOR MULTI-STANDARD RECEIVER WITH HIGH-LINEARITY AND LOW-NOISE TECHNIQUES

A Dissertation

by

JU SUNG KIM

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Edgar Sanchez-Sinencio
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	Duncan M. Walker
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ABSTRACT

Broadband RF Front-End Design for Multi-Standard Receiver
with High-Linearity and Low-Noise Techniques. (December 2011)
Ju Sung Kim, B.S., Yonsei University
Chair of Advisory Committee: Dr. Jose Silva-Martinez

Future wireless communication devices must support multiple standards and features on a single-chip. The trend towards software-defined radio requires flexible and efficient RF building blocks which justifies the adoption of broadband receiver front-ends in modern and future communication systems. The broadband receiver front-end significantly reduces cost, area, pins, and power, and can process several signal channels simultaneously. This research is mainly focused on the analysis and realization of the broadband receiver architecture and its various building blocks (LNA, Active Balun-LNA, Mixer, and trans-impedance amplifier) for multi-standard applications.

In the design of the mobile DTV tuner, a direct-conversion receiver architecture is adopted achieving low power, low cost, and high dynamic-range for DVB-H standard. The tuner integrates a single-ended RF variable gain amplifier (RFVGA), a current-mode passive mixer, and a combination of continuous and discrete-time baseband filter with built-in anti-aliasing. The proposed RFVGA achieves high dynamic-range and gain-insensitive input impedance matching performance. The current-mode passive mixer achieves high gain, low noise, and high linearity with low power supplies.

A wideband common-gate LNA is presented that overcomes the fundamental trade-off between power and noise match without compromising its stability. The proposed architecture can achieve the minimum noise figure over the previously reported feedback amplifiers in common-gate configuration. The proposed architecture

achieves broadband impedance matching, low noise, large gain, enhanced linearity, and wide bandwidth concurrently by employing an efficient and reliable dual negative-feedback.

For the wideband Inductorless Balun-LNA, active single-to-differential architecture has been proposed without using any passive inductor on-chip which occupies a lot of silicon area. The proposed Balun-LNA features lower power, wider bandwidth, and better gain and phase balance than previously reported architectures of the same kind.

A surface acoustic wave (SAW)-less direct conversion receiver targeted for multi-standard applications is proposed and fabricated with TSMC 0.13μm complementary metal-oxide-semiconductor (CMOS) technology. The target is to design a wideband SAW-less direct coversion receiver with a single low noise transconductor and current-mode passive mixer with trans-impedance amplifier utilizing feed-forward compensation. The innovations in the circuit and architecture improves the receiver dynamic range enabling highly linear direct-conversion CMOS front-end for a multi-standard receiver.

To my parents and brother

ACKNOWLEDGMENTS

Many people have contributed in countless ways throughout my program and this dissertation would not have been possible without the help of numerious people. First and foremost, I would like to express my sincere appreciation to my advisor, Dr. Jose Silva-Martinez for his guidance and encouragement during my study at Texas A&M University. I have acquired the fundamental of analog integrated circuit design through his in-depth knowledge and pioneering expertise. His great personality also made my research experience more joyful and encouraging. I am very grateful for his kind support and supervision on the technical and personal levels in making the reseach possible.

I would like to thank and acknowledge Dr. Edgar Sanchez-Sinencio, the director of the Analog and Mixed-Signal Center (AMSC). His courses on analog circuit, radio-frequency circuit, and filter design have educated me a lot in the technical details and the intuitive approach to the problem.

I would like to thank Dr. Shankar P. Bhattacharyya and Dr. Duncan M. Walker for serving my committee members and for their valuable inputs and suggestions. Their expertise on control theory and VLSI strengthened my knowledge and intuition on analog and RF integrated circuit.

My family has also played a great role throughout the years, supporting me unconditionally. My parents have always allowed me to pursue what I am intereted in, and they never complained on my indulgence on electrical engineering although they wanted their first son to pursue financially rewarding careers. My younger brother, Dongkyu Kim, is a great mentor and friend as well. I have often been a bad influence on him but he has been always with me despite that.

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I would like to thank Hyungjoon Jeon, Joungwon Park, Younghoon Song, and Jongwon Lee for their unending friendship. We spent many nights altogether on never-ending projects for ECEN 474 and 607. My knowledge and experiece on analog circut design would not be possible without invaluable discussions and collaborations with them. I would like to thank Raghavendra Kulkarni as my mentor and friend throughout my progam. He first guided me with his DTV tuner project and I interacted with him in every aspect from which I learned a lot. His rigorous approach to the problem made our project slow and steady but, I believe, his attitude and approach is what doctor of philosophy students should pursue. I also would like to thank all of colleagues in AMSC for their kindly help and sharing ideas. I can not leave out my wonderful fellow workers at Korean Church of A&M and A&M Korean Student Church. They made my long journey much more joyful under the grace of God.

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CHAPTER I

INTRODUCTION*

The demand for a multi-standard transceiver is expanding rapidly because of huge markets ranging from cell phones, WLAN terminals, and GPS to DAB/DVB enabled PDAs. Ultimately, software radio* (SWR) is the most flexible and efficient realization of RFIC transceiver but it is not a reality yet due to various design challenges. The SWR transceiver initially proposed by Mitola [3] puts very stringent requirements on the A/D and D/A conversion in terms of dynamic range, speed, noise, and linearity. Even if this A/D and D/A conversion is realizable with today's technologies, its power consumption may reach unreasonable values prohibiting the concept of SWR for practical hand-held devices.

CMOS technologies with aggressive scaling improve area and power consumption with high enough f_t to accomodate most existing commerical applications under 10GHz. Compatibility with the digital part of the transceiver mandates the use of advanced (scaled down) CMOS process. With its ability of highest level of integration, low cost, and low power consumption, CMOS is a MUST for SOCs consumer electronic products.

In this dissertation, we focus on the analysis and realization of a broadband receiver architecture and its various building blocks (LNA, Active Balun-LNA, Mixer, and trans-impedance amplifier) for multi-standard applications in CMOS technology. Two contrasting requirements, noise and linearity, which set the dynamic range per-

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´This dissertation follows the style of *IEEE Journal of Solid-State Circuits*.

*Part of this chapter is reprinted with permission from "Frequency Translation Techniques for Interference-Robust Software-Defined Radio Receivers", by Z. Ru, Ph.D. dissertation, University of Twente, Enschede, Netherlands, 2009.

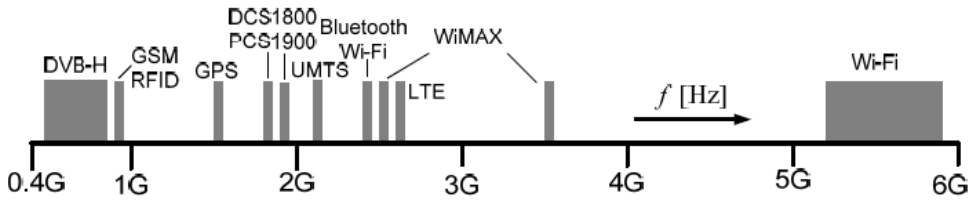


Fig. 1. Various mobile standards and allocated spectrums (excerpted from [1]).

formance of RFICs are tackled from the circuit to the architecture level. The proposed architecture and its building blocks improve dynamic range enabling highly a linear CMOS front-end for multi-standard receivers.

A. Motivations and Origins

Wireless communication came to existence with Guglielmo Marconi's successful radio signal transmission across the Atlantic Ocean in 1901 [4]. The consequences of this demonstration is simply astonishing. Different communication standards exist currently where most of them are allocated in the spectrum from 400MHz to 6GHz as shown in Fig. 1 [1]. Traditionally, each standard requires separate RF front-end and digital resources for baseband processing. To minimize cost and power, there has been a strong interest towards merging many applications and its functionality into a single mobile radio device [1]. The realization of flexible and efficient hardware that is controlled by software can make the device smaller, lighter, flexible, and low-cost, and this trend of radio evolution leads to the term, software radio (SWR) [1, 3].

The use of an analog to digital converter (ADC) is mandatory for the SWR receiver because the received analog radio signal is handled by the DSP employing its digital representation. In contrast to the popular super-heterodyne receiver and other

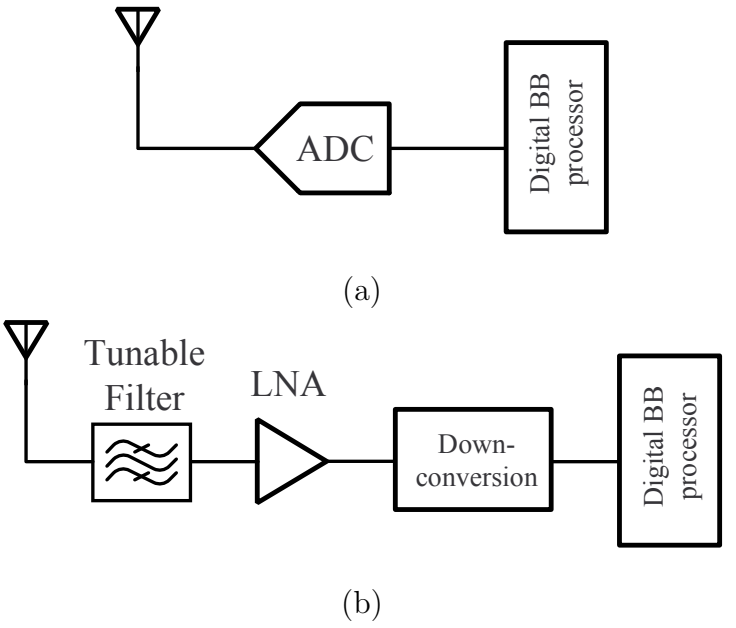


Fig. 2. (a) Ideal SWR receiver and (b) Practical SDR (multi-standard) receiver.

variants, the SWR receiver moves the ADC right after antenna as shown in Fig. 2(a). The burden on the ADC becomes extremely challenging without any amplification, filtering, and down-conversion. Therefore, the realization of an ideal SWR receiver is almost impossible with even state of the art technology. Mitola also suggested that a practical SWR can have the ADC located after down-conversion, and it can be defined as software-defined radio (SDR) [1]. The realization of SDR does not have to be fully software configurable like SWR, but SDR has to accept and process different standards with as much programmability as possible.

Fig. 2 shows the conceptual diagram of ideal SWR receiver and practical SDR receiver with a flexible RF front-end. Ideal SWR in Fig. 2(a) may be the ultimate dream of consumer electroncic designers but is not realizable as described before. On the other hand, the RF front-end in Fig. 2(b) should be at least broadband to cover different standards within the frequency range that a practical SDR should cover. Moreover, its performance must be comparable to or even better than the

conventional narrowband RF front-end due to concurrent reception of multi-standard unfiltered signals. The challenges for the design of the broadband RF front-end boils down to two contrasting scenarios: one challenge is to achieve a low noise figure while satisfying impedance matching over several gigahertz bandwidth when the signal strength is very small (around the sensitivity level of the standard), while another challenge is the high linearity requirement due to several channels received without any filtering but with high enough signal power. These two issues define the dynamic range of the RF front-end and dictate the required performance of the baseband ADC. This dissertation focuses on the design and optimization of the RF front-end for practical SDR receiver with high-linearity and low-noise techniques.

B. Research Focus and Dissertation Overview

Most of the narrowband receivers in the literature used super-heterodyne architecture proposed by Armstrong in 1918. The architecture was adopted widely since the architecture provides sensitivity and selectivity simultaneously. This approach, however, has multiple drawbacks especially for monolithic integration. The architecture requires an off-chip SAW filter for image rejection. Also, the architecture consumes huge power due to the power matching requirement with off-chip components. To achieve the full integration and low power, architectural solutions as well as circuit-level solutions are proposed and following chapters are the realizations of broadband receiver architecture and its various building blocks (LNA, Active Balun-LNA, Mixer, and trans-impedance amplifier) with detailed analysis.

In Chapter II, a direct-conversion receiver architecture is adopted achieving low power, low cost, and high dynamic-range for DVB-H standard. RFVGA, as the most critical block for the tuner application, adjusts the RF front-end gain to achieve

the maximum dynamic range of the tuner. A single-ended architecture is adopted to reduce the number of I/O and power consumption. A novel matching scheme is proposed to enable gain-insensitive impedance match. Low noise and high linearity with wide gain range of 30dB is achieved with the implemented RFVGA and serves as the first block in the proposed tuner. Single-to-differential conversion with a single ended RFVGA is achieved with a CMOS type differential pair with a single input AC grounded. An active-balun also serves as a transconductor driving a current-mode passive mixer. A passive mixer with current-in and current-out shows high dynamic range and is free of flicker noise suitable for direct conversion receivers. More importantly, the proposed topology can work with very low voltage supply and is a promising cadidate for future scaled-down technology.

Chapter III proposes a wideband common-gate (CG) LNA with dual negative feedback that overcomes the fundamental trade-off between power and noise match without compromising its stability. The proposed architecture can achieve the minimum noise figure (NF) over the previously reported feedback amplifiers in common-gate configuration. The proposed architecture achieves broadband impedance matching, low noise, large gain, enhanced linearity, and wide bandwidth concurrently by employing an efficient and reliable dual negative-feedback. An amplifier prototype was realized in 0.18μm CMOS, operates from 1.05 to 3.05GHz, and dissipates 12.6mW from a 1.8V supply while occupying 0.073mm^2 active area. The LNA provides 16.9dB maximum voltage gain, 2.57dB minimum NF, better than -10dB input matching, and -0.7dBm minimum IIP_3 across the entire bandwidth.

In Chapter IV, a wideband inductor-less low-noise-amplifier (LNA) with single-to-differential conversion is proposed for multi-standard radio applications. Exploiting common-gate (CG) and common-source (CS) stage with negative feedback, the proposed architecture features lower power, wider bandwidth, and better gain and

phase balance than previously reported active-balun based on CG-CS topology. Noise-suppressed current-mirror based biasing is utilized to ensure stable operation under process, voltage, and temperature (PVT) variations. Inherent inverting gain of CS stage is reused to boost the trans-conductance of CG stage and, hence, noise and power efficient design is achieved with better bandwidth. The gain and phase balance is improved by employing a compensation scheme in CS stage. The prototype was realized in 0.13μm CMOS, operates from 0.5 to 4GHz, and dissipates 2.6mW from 1.2V supply while occupying 0.075mm^2 active area. The Balun-LNA provides 17.4dB maximum voltage gain, 3.56dB minimum NF, better than -10dB input matching, and -0.45dBm IIP_3.

Chapter V describes the receiver architecture based on a single low-noise trans-conductor (LNTA) driving a current-mode passive mixer loaded by low-impedance. The proposed architecture exhibits beneficial features in terms of noise and linearity. Due to the current-mode passive mixer, it shows a drastic reduction in its flicker noise void of static DC current. Noise optimized trans-impedance amplifier (TIA) after down-conversion further optimizes the noise performance of receiver in direct-conversion architecture. Regarding linearity, distortion associated with a large voltage swing present in Gilbert cell mixer and voltage-mode passive mixer is eliminated by virtual ground of the TIA. Out-of-band interference performance is improved by avoding voltage swing before the signal experiences first-order low-pass filtering via I-V conversion in the TIA. The prototype receiver has been integrated in 0.13μm CMOS process with an on-chip frequency divider. The chip has an active area of 1mm^2 with the entire RF signal path operated from 1.2V and LO portion operated from 1.5V. The prototype receiver achieves >22dB conversion gain, <7dB NF, and >0.5dBm IIP_3 from 2 to 6GHz. The performance degradation at high frequency is due to in-sufficient LO swing and S_{11} is below -10dB from 2 to 7.7GHz.

CHAPTER II

CMOS DIRECT CONVERSION RECEIVER FRONT-END FOR DVB-H UHF BAND*

A. Introduction

Demand for personal multimedia services continues to increase leading to popularity of mobile digital TV (DTV). Emerging DTV services provide real-time digital television programs on mobile handsets. A high performance tuner front-end is a critical component for DTV reception. Such a tuner receives broadband mobile DTV channels, down converts the desired channel to baseband, and ensures adequate signal quality for further processing (demodulation and decoding). The received signal is then displayed on an LCD screen.

Multiple DTV standards suitable for mobile applications have emerged in recent years. DVB-H standard is used mainly in Europe and the USA, while ISDB-T and DMB are mainly used in Japan and Korea. While some of the earliest mobile tuner solutions were implemented in BiCMOS process [5–7]. However, integrated CMOS solutions have recently emerged as well [8–10]. Some recent solutions integrate multi-standard, multi-band (UHF, VHF and L-band) tuners in advanced CMOS technology [10].

This chapter* presents UHF band (470-862MHz) tuner with a single-ended RF input (without requiring external balun) implemented using IBM 0.18μm RF CMOS technology. The RF front-end consists of an RF variable gain amplifier (RFVGA) us-

*Part of this chapter is reprinted with permission from "UHF Receiver Front-End: Implementation and Analog Baseband Design Consideration", by R. Kulkarni *et al.*, accepted for future publication in *IEEE Transactions on VLSI systems* with DOI: 10.1109/TVLSI.2010.2096438.

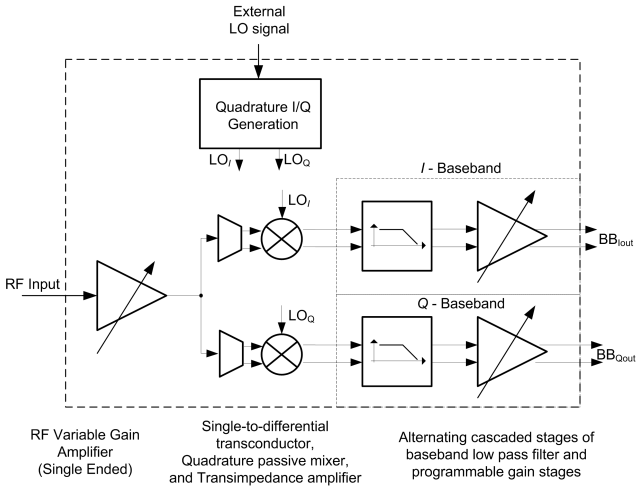
ing a modified shunt feedback structure that provides gain independent input matching without using shunt peaking inductor. The single-ended output of the RFVGA drives two linear broadband transconductors (I and Q) each of which also provide on-chip single-ended to differential signal conversion. Each transconductor drives a current-mode passive mixer. The downconverted signal is further processed by the baseband section implemented using a hybrid combination of continuous- and discrete-time filters with built in anti-aliasing.

This chapter is organized as follows. Section B provides an overview of specifications for the DVB-H standard and system-level design, and detail the RF front-end circuit blocks in Section C. Baseband section is not covered in Section C but detailed analysis on baseband section can be found in [11]. Characterization setup and experimental results are provided in Section D with brief conclusions in Section E.

B. Specification and Architecture

Dynamic range performance requirements of the mobile tuner are set by two contrasting scenarios. The weakest input signals power (sensitivity level) that can be received to guarantee sufficient signal-to-noise ratio sets the noise figure (NF) of the system. On the other hand, at high input power levels, non-linearity contributions degrade the system performance which sets the linearity requirements (specified in terms of IIP3) of the system.

To maintain an overall demodulator performance in terms of bit error rate (B.E.R.), the threshold signal to noise ratio (called C/N ratio) can be obtained for a given modulation scheme. For a demodulator B.E.R. requirement of 2×10^{-4}, tuner threshold C/N performance requirements in a Gaussian channel for QPSK ($\frac{1}{2}$ rate), 16 QAM ($\frac{3}{4}$ rate) and 64 QAM ($\frac{3}{4}$ rate) are 5.6dB, 15.1dB and 20.8dB respectively.



SENSITIVITY AND SNR REQUIREMENTS

Modulation	Sensitivity	SNR
QPSK	*-95 dBm*	*5.6 dB*
16-QAM	*-86 dBm*	*15.1 dB*
64-QAM	*-75 dBm*	*24.8 dB*

Fig. 3. Direct conversion DVB-H tuner system.

This C/N performance requirement is 24.8dB for the Mobile channel. Based on the C/N requirements, DVB-H tuner sensitivity level can be obtained as -94.6dBm, -86dBm and -75dBm for QPSK, 16 QAM and 64 QAM respectively from which noise figure specifications can be obtained for the system as a maximum of 5dB for the most stringent case.

Non-linearity contributions from the tuner front-end degrade the system performance. Undesired digital or analog channels inside the UHF signal band cannot be pre-filtered prior to channel down conversion. Linearity pattern requirement for DVB-H standard indicates that, the desired channel (channel N) can be embedded within two strong interferers located at channels N + 2 and N + 4 with over 45dBc higher power. This requirement has been analyzed previously in [5,7,9,12]. Assuming worst case input power (minimum) of -75dBm for 64 QAM and maximum possible interferer power of -35dBm, it can be shown that the worst case IIP3 requirement of the system is -1dBm [12].

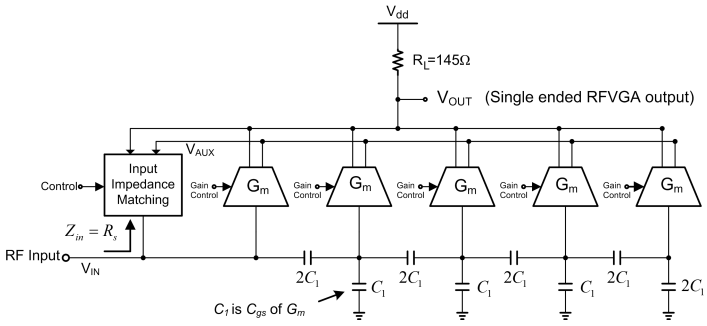
Given an input RF frequency band of 470-862MHz, we chose a direct conversion architecture shown in Fig. 3 since (1) Local oscillator (LO) harmonic frequencies

used for down conversion are out of band, eliminating harmonic mixing, and (2) the channel selection filter is a low pass filter (LPF) instead of a bandpass filter (BPF), and hence can be integrated on chip. The baseband LPF selectivity is determined from the undesired analog adjacent channel (N + 1) which can be up to 38dBc higher in power [12]. Using two AGC loops (RF and baseband) in the design helps to maximize the dynamic range of the tuner system [5, 12]. Variable input power level (sensitivity to maximum power level) sets the total AGC requirements of the system which can be conveniently partitioned between RF front-end and baseband.

Table I. Desired block level specifications.

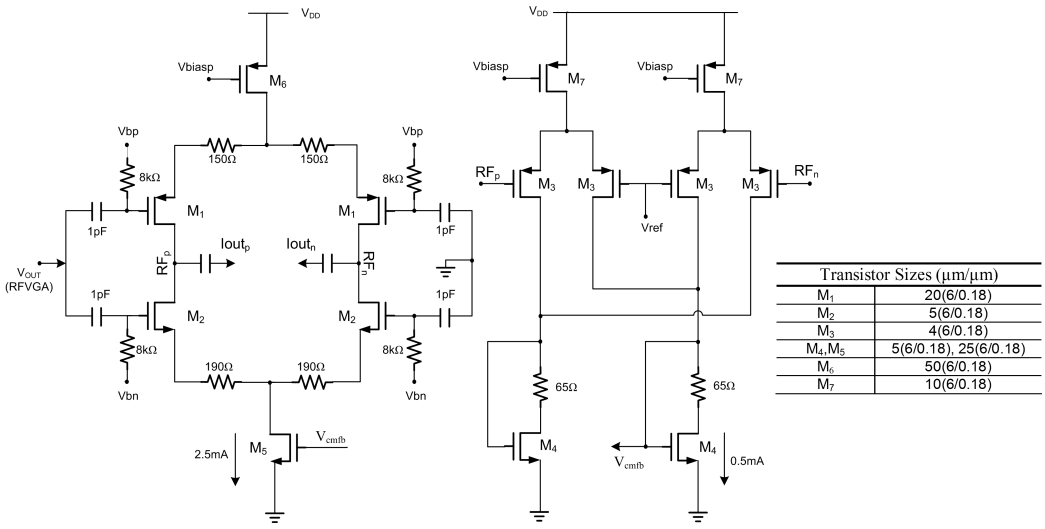
Performance	RFVGA	Mixer	Baseband
Gain (dB)	-14 to +16	18	-6 to +53
Noise Figure (dB)	3 at +16dB gain	12	35 at 53dB gain
	30 at -14dB gain		
IIP3 (dBm)	0 at +16dB gain	13	Outband > 30
	20 at -14dB gain		Inband > 30

Following the methodology outlined in [4,12], we partition the block specifications as shown in Table I. A gain range of 30dB is required in the RFVGA to ensure that the mixer and baseband stages do not saturate. When the power level at the RFVGA output exceeds -20dBm (RF take-over point), the RFVGA switches from gain to attenuation. The system can tolerate the higher noise figure at low gain settings since the input power is also higher. For the baseband, the variable gain range is distributed between baseband PGA and filter to ensure sufficient output C/N performance. The low pass filter bandwidth is programmable between 3MHz and 4MHz. For the 4 MHz option, the channel selectivity dictates attenuation >29dB at 5.25MHz and >45dB at 5.75MHz with minimum passband ripple. The baseband



Gain Range (dB)	Input Matching Scheme
+10 to +16	Shunt Feedback (First G_m stage)
+4 to +10	Shunt Feedback (Second G_m stage)
-2 to +4	Resistive
-8 to -2	Resistive
-14 to -8	Resistive

Fig. 4. RFVGA with gain independent shunt feedback input matching.



Transistor Sizes (μm/μm)	
M_1	20(6/0.18)
M_2	5(6/0.18)
M_3	4(6/0.18)
M_4,M_5	5(6/0.18), 25(6/0.18)
M_6	50(6/0.18)
M_7	10(6/0.18)

Fig. 5. Single-to-differential converting transconductor (G_m) driving the mixer switches.

signal chain should also provide automatic gain control range of -6 to +53dB to deliver -8dBm output power. The baseband noise figure should be <33 dB with both in-band and out-band IIP3>30dBm.

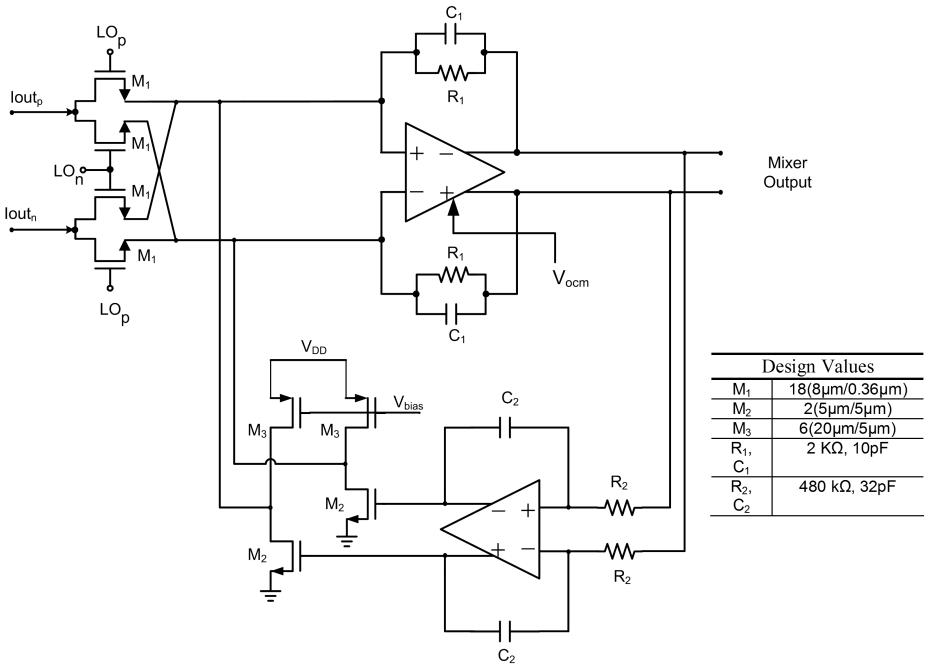


Fig. 6. Current-mode passive mixer terminated at TIA input with DC offset cancellation.

C. Circuit Design

1. RF Variable-Gain Amplifier

The RF front-end consists of an RF variable gain amplifier (cf. Fig. 4) followed by transconductor (cf. Fig. 5) and current-mode quadrature mixers (cf. Fig. 6). We use a single ended RF input to reduce the system cost by obviating the external balun. The variable gain helps maximize the output signal-to-noise-plus-distortion ratio (SNDR). We modify the wide dynamic range RFVGA of [13] and use MIM (Metal-Insulator-Metal) capacitors instead of deep N-well MOS transistors to enhance the capacitor divider accuracy. The RFVGA implements a modified shunt feedback scheme to achieve wideband input matching independent of gain without a shunt peaking inductor. The RFVGA consists of five identical Gm stages that are connected with a capacitive divider configuration as shown in Fig. 4. This cascaded arrangement

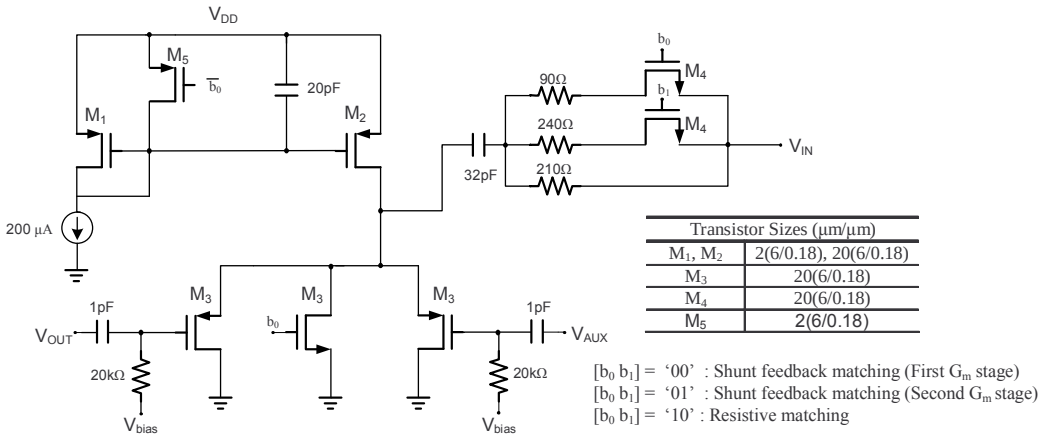


Fig. 7. Input impedance matching block (using modified shunt feedback).

facilitates a 6dB coarse gain setting in the RFVGA. Fine gain steps with smooth gain adjustment are implemented with a current steering scheme (not shown in the figure) with a process independent control block as reported in [13]. The shunt feedback matching is used for the first and the second Gm stages and simple resistive matching is used for the third through the fifth Gm stages. Fig. 7 displays the impedance matching/termination scheme as well as the control logic truth table. Operating with a 1.8V supply, RFVGA provides a gain range of -14dB to +16dB with a targeted NF of 3dB at maximum gain and IIP3 performance of +20dBm at 14dB RF attenuation.

2. Current-Mode Passive Mixer and Trans-Impedance Amplifier

Every building block except for the RFVGA is fully differential to minimize common mode noise and even order harmonic distortion. The RFVGA drives a single-ended to fully-differential converting Gm stage (cf. Fig. 5), which in-turn drives the mixer. The transconductor utilizes source-degenerated complementary NMOS and PMOS differential pairs to achieve high linearity and power efficiency through current reuse. The common mode feedback circuitry shown in Fig. 5 ensures proper biasing of the output nodes for the transconductor. The transconductor and the mixer switches

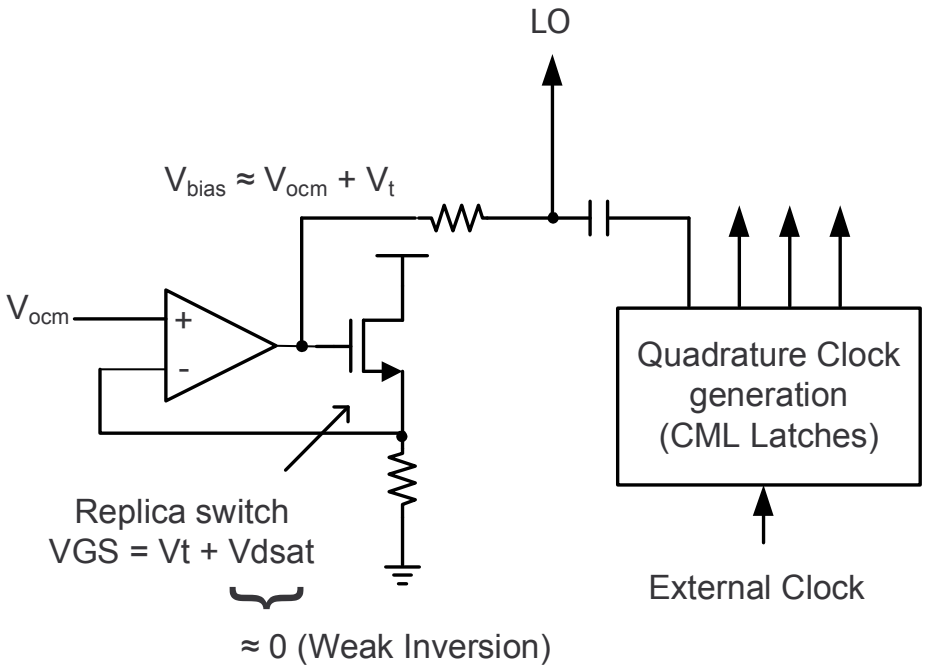
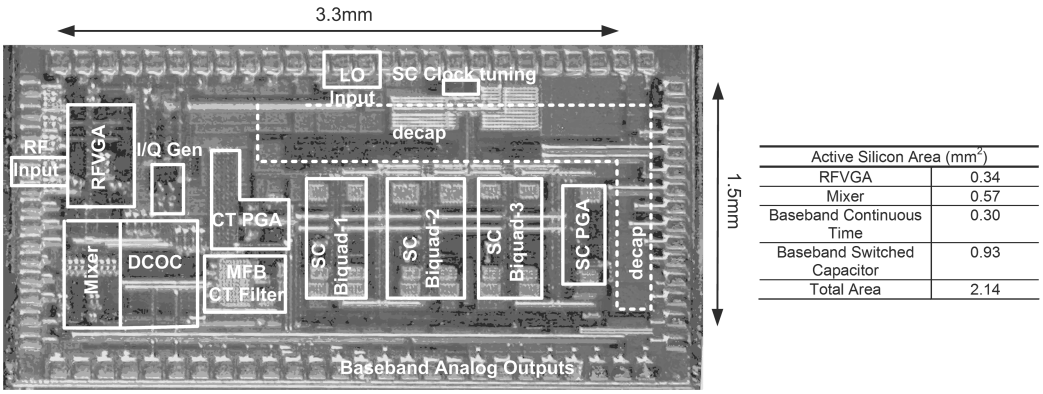


Fig. 8. Replica biasing for mixer switches.

are AC coupled to suppress flicker noise, DC offset and to provide biasing flexibility. This mixer combines source degeneration to provide superior nonlinearity, embedded single-ended to fully-differntial conversion and higher channel bandwidth (4 MHz vs 250kHz) compared to the mixer previously reported in [14]. The passive mixer as shown in Fig. 6 is terminated at the virtual ground of a transimpedance amplifier (TIA) stage, which provides the necessary current to voltage conversion. TIA provides broadband low impedance current path for the down converted signal within the signal bandwidth (up to 4MHz) using a wide gain-bandwidth (460 MHz), fully differential, two-stage Miller-compensated amplifier [15]. As indicated in Fig. 8, mixer switches are biased at the onset of inversion to minimize clock feed-through and even order harmonic distortion components. The biasing loop depicted in Fig. 8 biases the source of the NMOS transistor (M1) at the same level as TIA input (set by CMFB in the TIA amplifier). The gate of M1 is connected to the mixer switches DC bias to track



Active Silicon Area (mm^2)	
RFVGA	0.34
Mixer	0.57
Baseband Continuous Time	0.30
Baseband Switched Capacitor	0.93
Total Area	2.14

Fig. 9. Chip micrograph of DVB-H tuner.

threshold voltage (V_{th}) variation. On-chip frequency divider generates the required quadrature LO signals. Also a DC-offset cancellation loop is included around the TIA stage (cf. Fig. 6) which provides a highpass corner frequency of 2.4kHz. Operating with a 1.8V supply, mixer (along with TIA) provides a gain of +18dB with a targeted NF and IIP3 performance of 12dB and 13dBm respectively.

D. Measurement Results

The tuner system was fabricated in IBM 0.18μm RF CMOS technology. Fig. 9 shows the chip mircrograph for this design. Only one baseband channel was realized (out of I and Q) due to area constraints; however analog performance verification only requires testing of one channel. The system occupies $2.14mm^2$ of active area ($4.95mm^2$ including decoupling capacitors distributed throughout the chip) and was tested in a QFN80 package.

Fig. 10 illustrates the measurement setup used for characterization of the tuner system. The RF signal source is single ended, while all remaining signal I/Os are fully differential. An external broadband balun converts the single-ended external clock source to fully differential for the on-chip I/Q generator. Baseband outputs

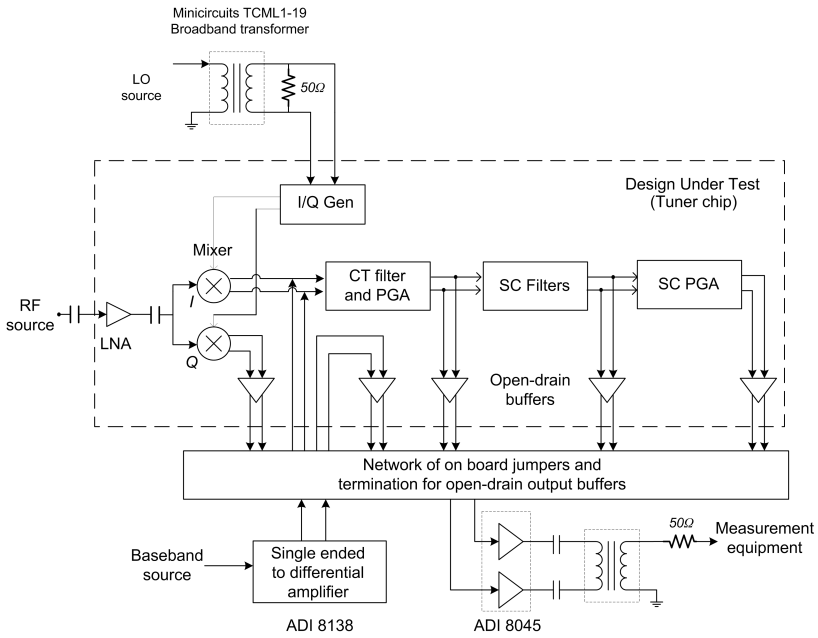
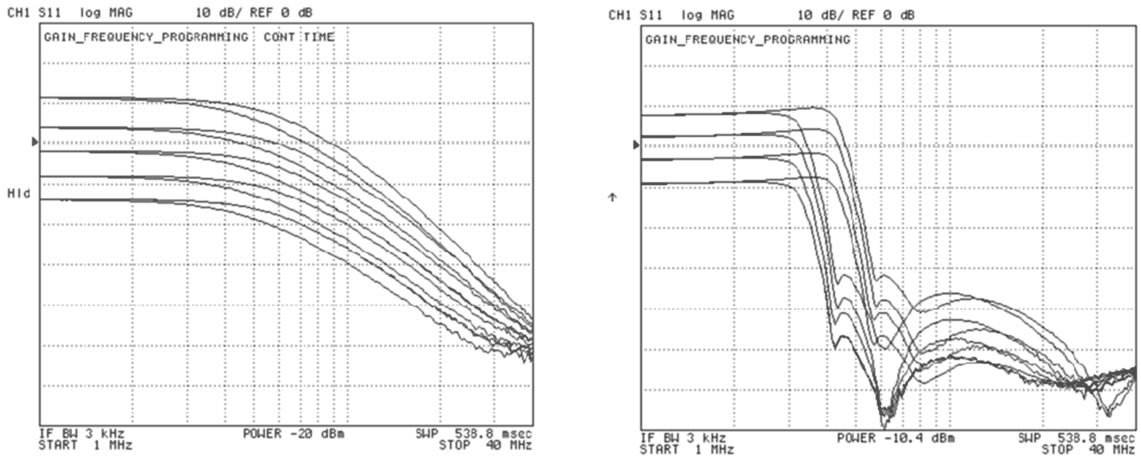


Fig. 10. Measurement set-up.

tapped at intermediate points in the signal chain are buffered using on-chip open drain buffers, which are terminated on the board. In order to accommodate large output signal swings in the baseband outputs (around the common mode voltage 0.8V), we designed the output buffers with source degenerated triple well NMOS devices with separate negative supply voltages. An independent additional buffer was included for characterization and de-embedding. All the differential outputs share a single termination on the board and only one output buffer is active at a time. The differential signal outputs are buffered separately using highly linear commercial amplifiers, which also provide low output impedance to drive the measurement equipment. Baseband blocks can also be characterized separately as using this setup as indicated in Fig. 10. A highly linear commercial single-ended to differential amplifier circuit is used for baseband characterization. The key advantage of this measurement setup is the option of characterizing the external amplifiers and open drain buffers



(a) (b)

Fig. 11. Measured baseband transfer function: (a) Continuous-time section and (b) Continuous and discrete-sections together.

separately to facilitate de-embedding.

The measured baseband transfer functions are shown in Fig. 11(a) and Fig. 11(b). Fig. 11(a) shows the frequency (3/4MHz) and gain programmability (-6dB to +18dB with 6dB per step) of the continuous time baseband filter. Fig. 11(b) shows frequency programmability of the entire baseband filter (3/4 MHz options) along with gain programmability of the SC section (0 to +18dB range with 0 or 6dB per biquad). For the 4 MHz setting, the measured frequency response indicates a stopband attenuation of >42dB for frequencies >5.75MHz.

The desired input impedance of the RFVGA is targeted for 75Ω (video standard). Since all the measurement equipment is based on 50Ω, the measured S11 response from the network analyzer is post-processed to reflect the matching performance with respect to a 75Ω. This post-processed S11 performance is indicated in Fig. 12. As explained previously in Section C.1, modified shunt feedback system is used for first and the second Gm stages while resistive matching is employed for rest of the cases. Fig. 12 indicates the S11 performance for two cases of shunt feedback matching and

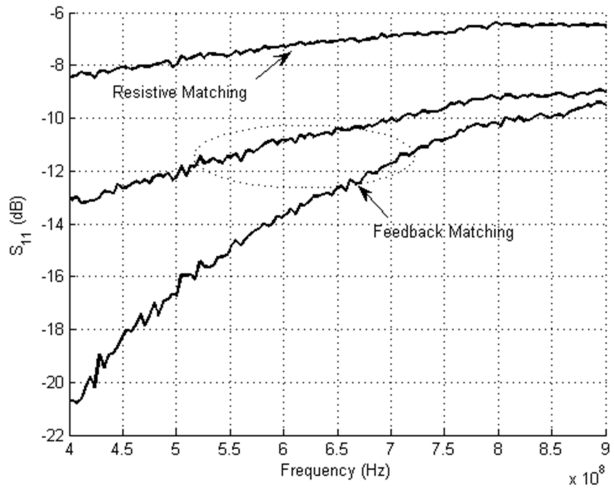
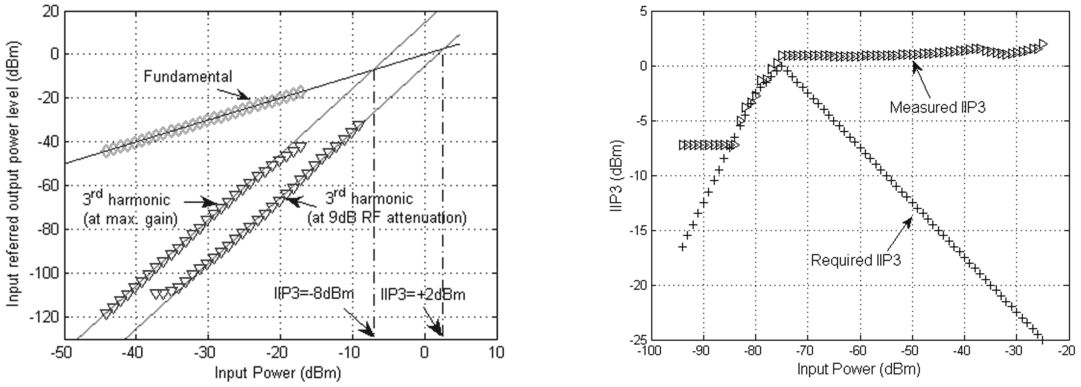


Fig. 12. Measured S_{11} performance (after post-processing for 75Ω input impedance).

resistive matching in the frequency range from 400 to 900MHz. We measured a NF of 7.9dB at maximum gain using the Y-factor method with an NC346B noise source. We attribute the additional NF penalty of 2.5dB with respect to the simulation result to (1) insertion loss of interconnections between the noise source and LNA, (2) the noise contribution of the gain control block in the RFVGA, and (3) RC routing parasitics between the RFVGA and the mixer.

Based on the L2 linearity test pattern specified in the DVB-H standard, the desired IIP3 is -8.5dBm at the 16QAM sensitivity level and -1dBm at 64 QAM sensitivity level. Since L2 pattern in DVB-H standard is the most stringent requirement, two RF tones located at N + 2 (516MHz) and N + 4 (531MHz) are injected, and the in-band distortion tone located at 1 MHz after the down conversion is measured. In-band gain at 501MHz was measured with the appropriate LO frequency to calculate the IIP3 (f_{LO} set to 500MHz). The outband tone input power is varied from -42dBm to -20dBm for the highest gain setting and from -34dBm to -16dBm for 9dB RF gain attenuation setting in steps of 1dB. The plot in Fig. 13(a) shows an IIP3



(a) (b)

Fig. 13. Measured linearity performance: (a) Two-tone measurement results for the system and (b) System IIP3 performance.

of -8 and +2dBm for the highest gain and 9dB RF attenuation cases respectively. Fig. 13(b) clearly indicates that the system IIP3 performance meets the desired IIP3 requirements for the system as the input power is varied.

E. Conclusion

A low power tuner IC was implemented in IBM 0.18μm RF CMOS technology targeting DVB-H specifications in the UHF band. This solution integrates an RFVGA, a linear current-mode passive mixer with a transimpedance amplifier, a baseband implementation using continuous and discrete-time partitioning, and an all digital tuning scheme for non-overlap clock generation. Using a single-ended RF input eliminates the requirement of an external balun, reducing the overall cost of the system. The hybrid baseband implementation achieves sharp roll-off with precise stopband zeroes without requiring elaborate tuning schemes. The approach outlined in this work can be extended to multi-band solutions implemented in deep-submicron processes

CHAPTER III

WIDEBAND COMMON-GATE CMOS LNA EMPLOYING DUAL NEGATIVE FEEDBACK WITH SIMULTANEOUS NOISE, GAIN, AND BANDWIDTH OPTIMIZATION*

A. Introduction

Future wireless communication devices must support multiple standards and features on a single chip. In particular, the LNA must have low noise and high linearity over a wide frequency range. The conventional solution is to employ several LC-tuned LNAs in parallel [16, 17]. This approach requires significant die area for several narrowband LNAs and RF switches for band selection, which hurts the sensitivity and complicates the receiver design. Reconfigurable LNAs [18–20] enable hardware sharing and reduce form factor, cost, and power with respect to parallel narrowband LNAs. However, simultaneous operation of several signal channels (e.g., cellular communications at 900MHz and 1800MHz, global positioning system at 1.2GHz and 1.5GHz, and WiFi at 2.4GHz and 5.2GHz) is prohibited with the reconfigurable operation. The concurrent dual-band architecture was proposed in [21], which requires multiple LC resonance circuitry at the input and the output increasing the die area, cost, and more importantly noise due to the finite Q of the inductors at the input. Furthermore, input match and band selection due to the LC resonators must occur at the same frequency to achieve the optimum performance. This is difficult to achieve without extremely accurate passive device models. Then, this chapter* presents a

*Reprinted with permission from "Wideband Common-Gate CMOS LNA Employing Dual Negative Feedback with Simultaneous Noise, Gain, and Bandwidth Optimization", by J. Kim *et al.*, *IEEE Trans. on Microwave Theory and Tech.*, vol. 58, no. 9, pp. 2340-2351, Sep. 2010.

wideband common-gate CMOS LNA for multi-standard applications.

The trend towards software-defined radio (SDR) requires flexible and efficient RF building blocks, which justifies the adoption of wideband LNAs in modern and future communication systems. Wideband LNAs significantly reduce cost, area, pins, and power, and can process several signal channels simultaneously. However, the design of wideband LNAs is challenging in several aspects. One challenge is to achieve a low noise figure (< 3dB) while satisfying impedance matching ($S_{11} < -10$dB) over several gigahertz bandwidth. The inductor-degenerated LNA used in conventional wireless receivers can offer simultaneous noise and power match by shifting the optimum noise impedance Z_{opt} to the desired value, but only in a narrowband around a single frequency [22]. Reducing the Q factor for the input matching network can increase the bandwidth at the cost of higher NF [23]. Another challenge is the high linearity requirement due to several channels received without any filtering. Chen *et al.* [24] reported a broadband linearization scheme, but, due to the higher order non-linear terms of the MOSFET, their linearization scheme is not effective for a high input power signal ($P_{in} > -20$dBm).

The common-gate (CG) LNA's NF is no better than $1 + \frac{\gamma}{\alpha}$ at the input matched condition, and recent research as of yet can not fully decouple the tradeoff between noise and power match [18,19,25–27]. We demonstrate that a dual negative-feedback amplifier in CG configuration can achieve low noise and high gain in a wideband fashion. The proposed CG-LNA with dual negative-feedback achieves simultaneous noise and power match without compromising other design parameters. Due to the nature of negative feedback, the LNA enhances the linearity regardless of variations in input power. We also show that the proposed LNA is able to achieve the orthogonality of design parameters between impedance matching, linearity, noise, gain, and bandwidth. The proposed techniques can also be used for BJTs and MESFETs and

are compatible with device scaling and technology evolution trends.

This chapter presents an analysis and realization of wideband common-gate CMOS LNA employing dual negative feedback. Section B reviews the properties of CG-LNA and low-noise techniques employing feedback. Section C describes the proposed dual negative-feedback LNA and derives analytical expressions for input impedance, gain, bandwidth, NF, and IIP_3. The amplifier design and layout issues are discussed in Section D. Section E provides measurement results, and the concluding remarks are given in Section F.

B. Propertis of CG-LNA and Its Low-Noise Techniques

As f_t increases with the scaling of CMOS devices, it becomes more promising to employ feedback in the design of wideband LNAs. Before exploring the design details of the dual negative-feedback CG-LNA, it is helpful to review the properties of CG-LNAs and their low-noise techniques.

1. Properties of CG-LNA

Fig. 14(a) shows the conventional CG-LNA where the inductor resonates with the parasitic capacitance of the impedance matching device and the input pad. Then, within the signal bandwidth, the reacitive part of the input impedance is canceled and the real part of the input impedance is determined by $1/(g_m + g_{mb})$. Also, the input matching network of the CG-LNA is a parallel resonance as opposed to the series resonance of inductor-degenerated LNA. Hence, a low Q (quality factor) of the input matching network results in a wider bandwidth and CG-LNA is more robust to process, voltage, and temperature (PVT) variations.

The power gain of CG-LNAs is relatively low due to the impedance matching

constraint. Ignoring the transconductance of the back-gate transistor (g_{mb}), input impedance matching requires $1/g_m = R_s$ and the CG-LNA's effective transconductance under input matching condition is

$$G_{m,CG-LNA} = \frac{1}{2}g_m = \frac{1}{2R_S}. \tag{3.1}$$

CG-LNAs exhibit superior stability and reverse isolation due to the absence of the Miller effect by C_{gd}. Although CG-LNAs feature desirable properties for wideband operation, their high NF under input matching condition prevents its extensive use. The NF including channel noise, induced gate noise, and resistive load under the input matching condition is expressed as [25]

$$NF_{CG-LNA} \approx 1 + \frac{\gamma}{\alpha} + \frac{\delta\alpha}{5}\left(\frac{\omega_0}{\omega_T}\right)^2 + \frac{4R_S}{R_L}, \tag{3.2}$$

where γ, α, and δ are bias-dependent parameters [28], R_L is the load impedance, R_S is the source impedance, ω_o and ω_T are operating and unity current gain frequencies, respectively. The dominant noise source in CG-LNA is due to the channel noise $4kT\frac{\gamma}{\alpha}g_m$ of the MOSFET device. The gate induced noise in a CG-LNA is usually negligible in contrast to an inductor-degenerated LNA under simultaneous noise and power match condition [29]. The fourth term shows that a large resistive load is desirable for low NF, but this condition is usually detrimental for wideband operation of LNAs.

In summary, CG-LNAs achieve a broadband impedance match, superior reverse isolation, stability, and a high linearity. Recently reported CG feedback amplifiers aim at decoupling the noise and power (input) match tradeoff without degrading other rel evant LNA parameters.

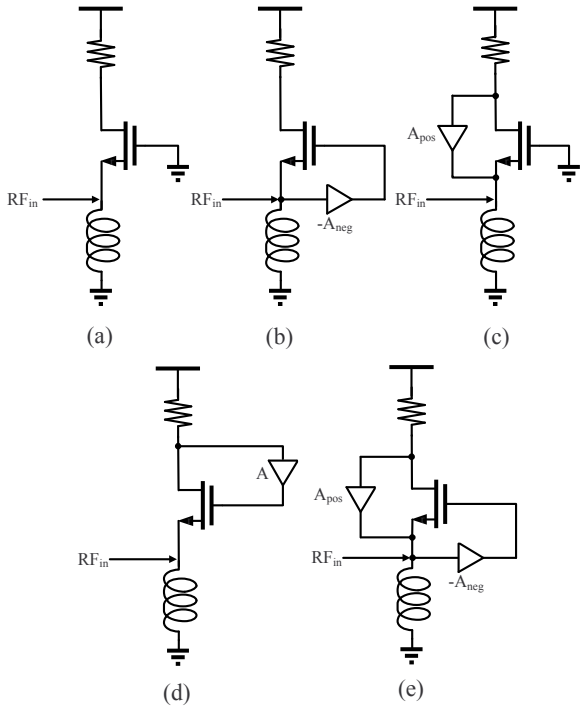


Fig. 14. Conventional CG-LNA and low-noise techniques employing feedback.

2. Low-Noise Techniques Employing Feedback in CG-LNA

The capacitor cross-coupled CG-LNA [25] in Fig. 14(b) reduces its NF and power consumption by employing negative feedback. g_m-boosting with inverting amplification, A_{neg}, reduces the noise contribution due to the channel noise by a factor of $1 + A_{neg}$ under input matching condition. At the same time, the intrinsic transconductance of the impedance matching device can be halved, which reduces the power consumption by the same factor. The drawbacks of the capacitor cross-coupled CG-LNA are that the passive g_m-boosting dictates that the inverting amplification must be less than 1 taking into account the parasitic capacitance (C_{gs}). Furthermore, the unilateral behavior of the CG-LNA is affected by the scheme where input-output feedthrough and stability are deteriorated.

In [18], shunt-shunt positive feedback is used to add a degree of freedom in deter-

mining the g_m of the impedance matching device, as shown in Fig. 14(c). However, the amplifier's stability must be carefully evaluated when the positive feedback is employed. Also, increasing the loop gain in positive feedback reduces the overdrive voltage of the transistor and consequently its linearity.

Negative-feedback around a common-base amplifier has been employed to break the lower bound of noise performance in [19]. The simplified CMOS version schematic of the LNA is shown in Fig. 14(d). In this topology, the feedback network is passive, limiting the choice of the g_m of the impedance matching device. Low gain and a large parasitic capacitance at the output node makes this approach unsuitable for wideband LNAs.

Woo *et al.* [27] demonstrated that positive feedback in combination with passive g_m boosting can achieve the best theoretical noise performance with low power. Compared to [18], this work, shown in Fig. 14(e), requires half the power consumption for the same power gain and features further suppression of channel noise from the impedance matching device.

All the reported works are based on feedback amplifiers taking advantage of the high f_t of scaled CMOS devices. However, none of these designs achieve the full decoupling of noise and power match in CG-LNAs. Also, other design parameters (e.g. stability, reverse isolation, and wide bandwidth) are sacrificed in order to improve noise performance. The main properties of feedback based CG-LNA topologies are summarized in Table II.

C. Dual Negative-Feedback Wideband CG-LNA

Fig. 15 shows the proposed wideband CG-LNA with dual negative feedback (shunt-series) along with its simplified model. Impedance matching device M_1 amplifies the

Table II. Comparison of characteristic in feedback based CG-LNA.

	Neg. FB (type I) CG-LNA [25]	Pos. FB CG-LNA [18]	Pos.-Neg. FB CG-LNA [27]	**This Work**
Z_{in}	$\frac{1}{g_m(1+A_{neg})}$	$\frac{1}{g_m(1-A_{pos})}$	$\frac{1}{g_m(1+A_{neg})(1-A_{pos})}$	$\boldsymbol{\frac{R_L+1/g_{m1}}{1+g_{m2}/g_{m3}}}$
A_V* @ input match	$\frac{1}{2}\frac{R_L}{R_S}$	$\frac{R_L}{R_S}$	$\frac{R_L}{R_S}$	$\boldsymbol{\frac{1}{2}\left(\frac{g_{m1}R_L}{1+g_{m1}R_L}\right)\left(1+\frac{g_{m2}}{g_{m3}}\right)}$
Bandwidth** (ω_{3dB})	$\frac{1}{R_L C_p}$	$\frac{1}{R_L C_p}$	$\frac{1}{R_L C_p}$	$\boldsymbol{\frac{1+g_{m1}R_L}{R_L C_p} \approx \frac{g_{m1}}{C_p}}$
NF* wo R_L	$1+\frac{\gamma}{2\alpha}$	$1+\frac{\gamma}{2\alpha}+g_{mp}R_S\frac{\gamma}{\alpha}$	$1+\frac{\gamma}{4\alpha}+g_{mp}R_S\frac{\gamma}{\alpha}$	$\boldsymbol{1+\frac{\gamma}{\alpha}\frac{1}{g_{m2}R_S}}$***
NF due to R_L	$\frac{4R_S}{R_L}$	$\frac{9R_S}{4R_L}$	$\frac{9R_S}{4R_L}$	$\boldsymbol{\frac{R_S}{R_L}}$
NF† total (dB)	4.47	4.23	3.32	3 (with $I_{DC,fb}$=5mA) 2.1 (with $I_{DC,fb}$=10mA)

*$A_{neg}=1$, $A_{pos}=0.5$ are assumed under perfect input matching condition
**C_p is the parasitic capacitance at the output node of the CG-LNA
***Thermal noise due to M_1 is negligible and is not shown here
†Numerically estimated with $A_{neg}=1$, $A_{pos}=0.5$, $\frac{\gamma}{\alpha}=2$, and $R_L=250$

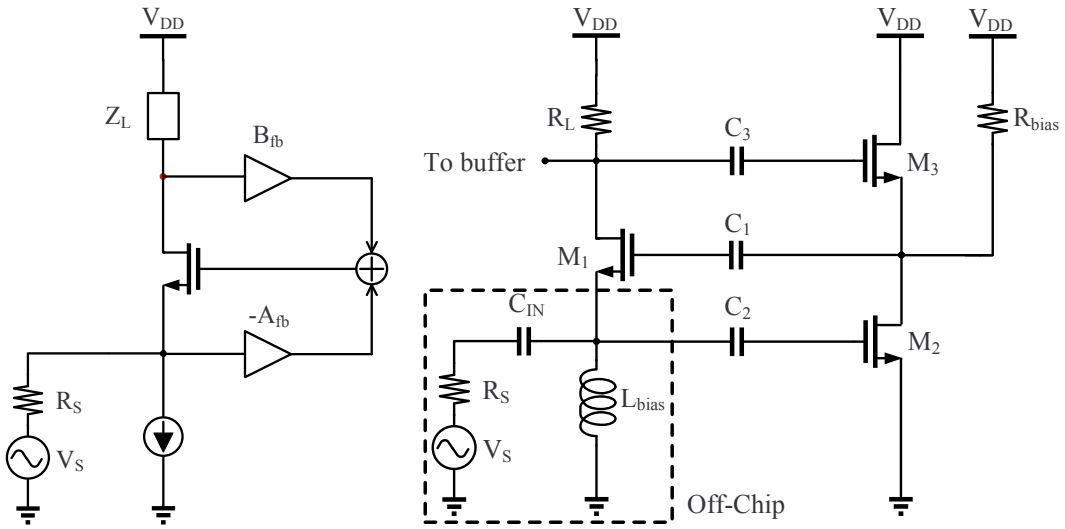


Fig. 15. (a) Simplified LNA model and (b) Schematic of the dual negative-feedback CG-LNA (biasing not shown).

signal and provides the main forward signal path. The common-source amplifier A_{fb} in Fig. 15(a) boosts g_{m1} (g_m of M_1). The source follower M_3 controls the LNA input impedance with the ratio g_{m2}/g_{m3}, which governs the amount of g_m boosting as well as the contribution of R_L to the LNA input impedance. R_{bias} sets the loop gain and supplies the difference in bias current between M_2 and M_3.

To minimize the power consumption, we employ a single-ended configuration and use only NMOS transistors, as they have a higher f_t than PMOS for a given current. Note that while our proposed architecture allows for a single-ended implementation, those in [25, 27] do not, for they rely on capacitor cross-coupling to achieve sign inversion with passive devices. Hence, those previous approaches require a balun worsening the NF due to its insertion loss, thus offsetting the advantage of low-noise techniques.

1. Input Match

The in-band LNA input impedance can be found as

$$Z_{in} \approx \frac{R_L + 1/g_{m1}}{1 + g_{m2}/g_{m3}} \parallel sL_{bias} \parallel \frac{1}{sC_p} \tag{3.3}$$

where parasitic capacitor C_p arises from the input pad, M_1, and M_2. The input matching network is a parallel resonance where the quality factor of the parallel LC resonator is

$$Q_{match} = \frac{\omega C_p R_S}{2}. \tag{3.4}$$

A lower Q_{match} results in a wider bandwidth since the sensitivity of Z_{in} to parasitic components is proportional to the quality factor of the matching network [30]. The parasitic capacitor C_p is absorbed into the LC network and the imaginary part of Z_{in} is negligible within the bandwidth. The real part of Z_{in} mainly depends on R_L, which is transformed to the input through the embedded dual negative feedback. Therefore, g_{m1} is no longer constrained by the input match condition and can be chosen $> \frac{1}{R_S}$.

2. Noise Analysis

Noise cancellation using feed-forward techniques [24, 31, 32] can decouple the input matching from the NF by cancelling the impedance matching device's noise. However, mismatch and parasitic effects limit the performance of the technique, and the effective bandwidth of noise cancellation is limited. In feedback based approaches [18,19,25–27], the noise cancellation of the impedance matching device comes from the degree of freedom provided by the feedback network.

The dominant noise sources in the proposed LNA are M_1, M_2, M_3, and R_L. Within the LNA's bandwidth, the power spectral density components at the output

can be obtained as

$$V_{m1}^2 = 4kT\frac{\gamma}{\alpha}g_{m1}\left(\frac{R_L}{H}\right)^2, \tag{3.5}$$

$$V_{m2}^2 = 4kT\frac{\gamma}{\alpha}g_{m2}\left(\frac{g_{m1}R_L}{Hg_{m3}}\right)^2, \tag{3.6}$$

$$V_{m3}^2 = 4kT\frac{\gamma}{\alpha}g_{m3}\left(\frac{g_{m1}R_L}{Hg_{m3}}\right)^2, \tag{3.7}$$

$$V_{RL}^2 = 4kTR_L\left\{\frac{1+g_{m1}R_S\left(1+g_{m2}/g_{m3}\right)}{H}\right\}^2, \tag{3.8}$$

$$V_{RS}^2 = 4kTR_S\left\{\frac{g_{m1}R_L\left(1+g_{m2}/g_{m3}\right)}{H}\right\}^2, \tag{3.9}$$

where H is

$$H = 1 + g_{m1}R_S\left(1+\frac{g_{m2}}{g_{m3}}+\frac{R_L}{R_S}\right). \tag{3.10}$$

Thus, the total NF is approximately

$$NF = 1+\frac{V_{m1}^2+V_{m2}^2+V_{m3}^2+V_{RL}^2}{V_{RS}^2} \tag{3.11}$$

$$= 1+F_{M_1}+F_{M_2}+F_{M_3}+F_{R_L} \tag{3.12}$$

$$\approx 1+\underbrace{\frac{\gamma}{\alpha}\frac{1}{g_{m1}R_S}\frac{1}{\left(1+g_{m2}/g_{m3}\right)^2}}_{M_1\ contribution}+\underbrace{\frac{\gamma}{\alpha}\frac{1}{\left(g_{m2}+g_{m3}\right)R_S}}_{M_{2,3}\ contribution}+\underbrace{\frac{R_S}{R_L}}_{R_L\ contribution}. \tag{3.13}$$

The second term in (3.13) represents the noise contribution of the main transistor M_1 and is minimized when g_{m1} and g_{m2}/g_{m3} are large. The third term accounts for the noise contribution of M_2 and M_3 and is minimized if $(g_{m2}+g_{m3}) > \frac{1}{R_S}$. The last term represents the thermal noise contribution of R_L. Under the same bandwidth condition, the proposed LNA presents the lowest noise contribution due to R_L when compared to other LNAs. With an unconstrained power specification, the proposed LNA can achieve the theoretical minimum NF. With a constrained power specification, the power budget determines the NF, which in this topology is decoupled from other design parameters.

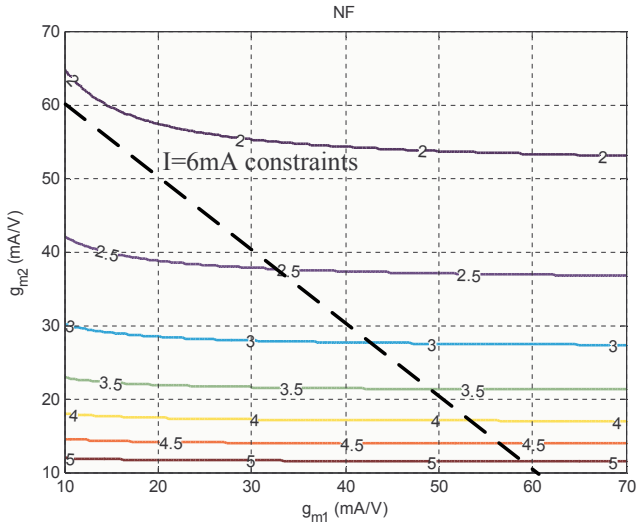


Fig. 16. NF countour plot with different g_{m1} and g_{m2} at $R_L = 370\Omega$, $\frac{g_{m2}}{g_{m3}} = 5$, $\gamma = \frac{4}{3}$, and $\alpha = 0.8$.

From (3.13), the LNA NF improves by increasing g_{m1}, g_{m2}, g_{m3}, and R_L while determining the g_{m2}/g_{m3} ratio from the input matching condition. The maximum values for design parameters, however, are bounded by two constraints: available voltage headroom, and Q of the input matching network. Fig. 16 shows the NF contour by varying g_{m1} and g_{m2} given that g_{m2}/g_{m3} is unaltered and R_L is maximized. The dashed line in Fig. 16 corresponds to a constant current consumption of 6mA for M_1 and M_2 under the same g_m/I_D condition.

The LNA power consumption factor, or equivalently $\sum g_m = g_{m1} + g_{m2}$ can be taken into consideration by substituting g_{m2} with $\sum g_m - g_{m1}$. Hence, (3.13) can be rewritten as

$$\begin{aligned} NF \;\approx\; & 1 + \frac{\gamma}{\alpha}\frac{1}{g_{m1}R_S}\frac{1}{\left(1+g_{m2}/g_{m3}\right)^2} \\ & + \frac{\gamma}{\alpha}\frac{1}{\left(\sum g_m - g_{m1}\right)\left(1+g_{m3}/g_{m2}\right)R_S} + \frac{R_S}{R_L}. \end{aligned} \tag{3.14}$$

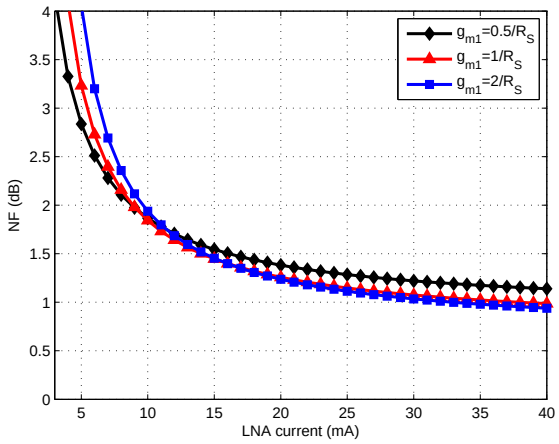


Fig. 17. NF and g_{m1} with different LNA current levels at $R_L = 370\Omega$, $\frac{g_{m2}}{g_{m3}} = 5$, $\gamma = \frac{4}{3}$, and $\alpha = 0.8$..

Fig. 17 shows the theoretical NF w.r.t. LNA current consumption for different g_{m1} values. As expected, the plot shows an inverse relationship with current. The thermal noise due to M_1 is minimized, regardless of current, by the dual feedback factor g_{m2}/g_{m3}. Notice that at lower current levels, the NF for small g_{m1} shows better performance since, in this region, feedback transistors M_2 and M_3 dominate the noise performance. As current increases, the noise contritution due to M_1's noise becomes more prominent, indicating that large g_{m1} is desirable for low noise performance. Regardless of current levels, R_L's noise imposes the lower bound on the NF. Based on the trend of noise performance w.r.t. current consumption levels, a power-efficient region of operation can be found by equating $F_{M_1} = F_{M_2} + F_{M_3}$. Hence

$$g_{m2} = A_2 \left(1 + A_2\right) g_{m1}, \tag{3.15}$$

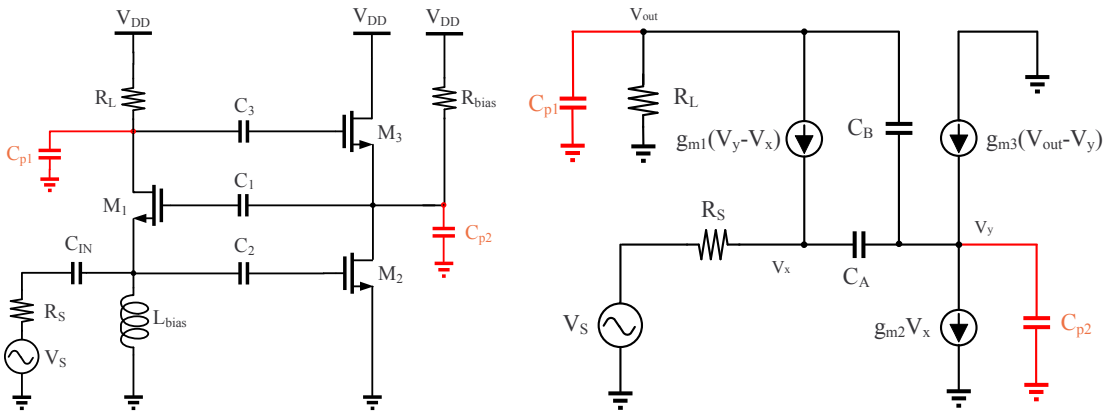
where $A_2 = g_{m2}/g_{m3}$. Increasing current beyond this point results in diminishing marginal returns.

3. Gain and Bandwidth Analysis

Like other topologies, conventional CG-LNAs must trade gain for bandwidth. In [18] and [27], active current gain is added by employing positive-feedback, thereby increasing the gain by a factor of 2 compared to conventional CG-LNA and the topology reported in [25] for input matched condition. Still, gain, bandwidth, impedance matching, and NF can not be optimized simultaneoulsy, as depicted in Table II. However, the dual negative feedback in the proposed architecture can simultaneously optimize all these parameters. The high transconductance ratio g_{m2}/g_{m3} provides a high voltage gain and allows us to use larger output load (R_L) as shown by the impedance matching condition given in (3.3). Large R_L gives a low NF and does not affect the 3-dB bandwidth, because the bandwidth is chiefly a function of only g_{m1} and the parasitic capacitances at the LNA output.

To derive the voltage gain and bandwidth of the proposed ampflifier, we consider two dominant parastitic capacitances as shown in Fig. 18(a) and its AC model in Fig. 18(b). The parasitic capacitors at the input node v_x are canceled by LC resonance and thus not considered. C_{p1} is the total capacitance due to M_1, M_3, and the input capacitance of the next stage. C_{p2} is the parastitic effects at the drain of M_2 and source of M_3. In the practical implementation, C_{p1} dominates C_{p2} because C_{p1} includes the appreciable parasitic capacitance of the next stage. $C_A \approx C_{gs1} + C_{gd2}$ and $C_B \approx C_{gd1} + C_{gs3}$ create an undesired feedback path. Impedance matching and low NF condition dictate that M_1 and M_2 be much larger than M_3, so $C_A >> C_B$. Hence, for simplicity, we neglect C_B in the following analysis. The effects of C_B on LNA frequency response is included in Appendix A.

AC coupling capacitors C_1, C_2, and C_3 attenuate low-frequency signals, and the parasitic capacitors $C_{p1,p2}$ attenuate high-frequency signals. In the mid-band



(a) (b)

$A_1 = g_{m1}R_L$	$\omega_{p1} = 1/R_L C_{p1}$
$A_2 = g_{m2}/g_{m3}$	$\omega_{p2} = g_{m3}/(C_A + C_{p2})$

(c)

Fig. 18. (a) Proposed LNA with parasitic capacitors, (b) Equivalent circuit model for voltage gain and bandwidth analysis, and (c) Design parameters.

Table III. Pole, zero, and Q parameters versus relative location of two poles.

	$\omega_{p1} \gg \omega_{p2}$	$\omega_{p2} \gg \omega_{p1}$	$\omega_{p1} \approx \omega_{p2}$
$\omega_{dominant}$	$\omega_{p2}(1+A_1)$	$\omega_{p1}(1+A_1)$	$\sqrt{\omega_{p1}\omega_{p2}(1+A_1)}$ *
ω_{zero}	$\frac{g_{m3}}{C_{p2}}(1+A_2)$	$\frac{g_{m3}}{C_{p2}}(1+A_2)$	$\frac{g_{m3}}{C_{p2}}(1+A_2)$
Q (quality factor)	–	–	$\frac{\sqrt{\omega_{p1}\omega_{p2}(1+A_1)}}{\omega_{p1}+\omega_{p2}}$

*Natural frequency (ω_n)

frequency, AC coupling capacitors and parasitic capacitors can be ignored yielding

$$\begin{aligned} A_{vo} &= \left(\frac{Z_{in}}{R_S+Z_{in}}\right)\left(\frac{g_{m1}R_L}{1+g_{m1}R_L}\right)\left(1+\frac{g_{m2}}{g_{m3}}\right) \\ &\approx \left(\frac{Z_{in}}{R_S+Z_{in}}\right)\left(1+\frac{g_{m2}}{g_{m3}}\right). \end{aligned} \tag{3.16}$$

Note that the mid-band gain of the amplifier is mainly determined by the dual feedback transconductance ratio (g_{m2}/g_{m3}) rather than the load and source impedance ratio (R_L/R_S). Small signal analysis of Fig. 18(b) shows that the high-frequency voltage gain is approximately given by

$$A_v(s) \approx A_{vo}\frac{1+\frac{C_{p2}}{g_{m3}(1+A_2)}s}{1+\left(\frac{1}{\omega_{p1}}+\frac{1}{\omega_{p2}}\right)\frac{1}{1+A_1}s+\frac{1}{\omega_{p1}\omega_{p2}(1+A_1)}s^2}, \tag{3.17}$$

where A_1, A_2, ω_{p1}, and ω_{p2} are circuit dependent parameters defined in Fig. 18(c).

Depending on the relative location of the two poles, the pole, zero, and Q values for each case change and are shown in Table III. When either ω_{p1} or ω_{p2} is much greater than the other, the dominant pole is shifted away from the origin by the factor of $1+A_1$. When no dominant pole exists (i.e., two poles are close to each other), the transfer function becomes second order and has complex poles. The natural frequency ω_n is $\sqrt{\omega_{p1}\omega_{p2}(1+A_1)}$ and the system Q is given in Table III. Regardless of the location of the poles, dual negative feedback increases the amplifier's bandwidth.

Fig. 19 displays the surface plots of normalized 3-dB bandwidth $\frac{\omega_{3dB}}{\omega_{p1}}$ vs. the forward path gain $g_{m1}R_L$ and the feedback loop gain $\frac{g_{m2}}{g_{m3}}$ for $\frac{\omega_{p2}}{\omega_{p1}} \in \left\{\frac{1}{2}, 1, 2, 4\right\}$. As

seen in the figure, the feedback loop gain does not change the bandwidth appreciably, provided that it is sufficiently high. This behavior occurs because the loop gain only affects the zero, while the forward path gain determines the pole shifting. In all cases, $\frac{\omega_{3dB}}{\omega_{p1}} > 1$ when $g_{m1}R_L > 1$ (normal operation), demonstrating higher bandwidth than the conventional CG-LNA.

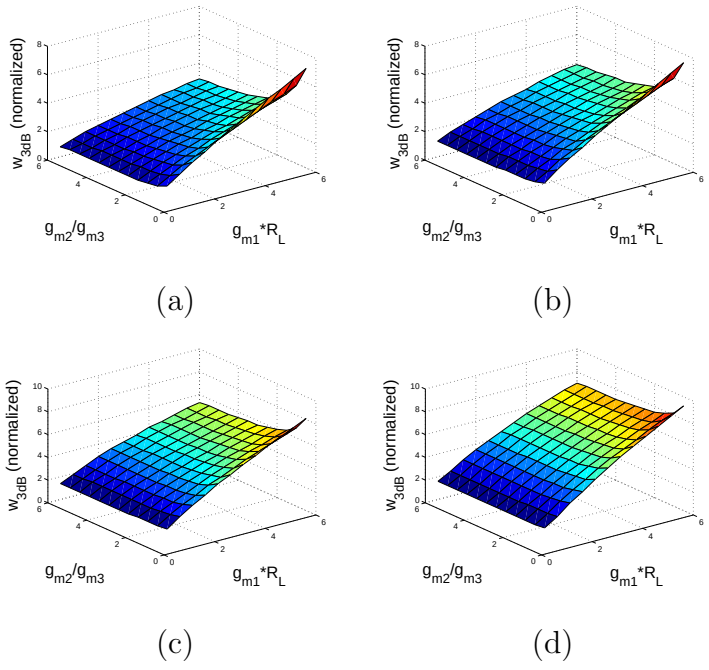


Fig. 19. Bandwidth dependence on feedback characteristics: (a) $\omega_{p2} = \frac{1}{2}\omega_{p1}$, (b) $\omega_{p2} = \omega_{p1}$, (c) $\omega_{p2} = 2\omega_{p1}$, and (d) $\omega_{p2} = 4\omega_{p1}$.

The bandwidth enhancement due to the dual negative feedback is limited by the f_t of the device and the LNA's driving capability. When the proposed LNA is realized in a receiver, the dominant pole is located at ω_{p1} ($\ll \omega_{p2}$) due to the parasitic capacitance of the next stage (e.g., mixer or off-chip SAW filter). Hence,

the expression for the dominant pole can be derived as

$$\begin{aligned} \omega_{dominant} &= \omega_{p1}\left(1+A_1\right) \\ &\approx \frac{g_{m1}}{C_{next}+\xi\frac{g_{m1}}{2\pi f_t}}, \end{aligned} \tag{3.18}$$

where C_{next} is the capacitance of the next stage and ξ is the proportionality constant between the parasitic capacitance of the amplifier output and C_{gs1}. Therefore, the bandwidth enhancement ($1/R_L C_{p1} \rightarrow g_{m1}/C_{next}$) is effective only when the LNA's driving capacitance (C_{next}) is dominant. If not, the dominant pole is f_t limited ($\approx 2\pi f_t/\xi$).

4. LNA's Linearity

The LNA linearity is typically described using IIP_3 and 1-dB compression point, where the former is the metric for small signal power and the latter is for large signal power. Multi-Gate transistor (MGTR) based linearization methods for MOSFETs rely on the fact that the second-order g_m derivative's polarity is different in weak and strong inversions. MGTR scheme is not effective for large input signals because of higher-order non-linearity. Although the published works in [24, 33, 34] report large IIP_3 values, they typically work only for $P_{in} \leq -20$dBm. On the other hand, feedback suppresses all the harmonic terms [35, 36] and, therefore, is effective regardless of the input signal power.

Consider a single NMOS transistor in saturation region with drain current given by

$$I_{DS} = \frac{\mu C_{ox}}{2}\frac{W}{L}\frac{\left(V_{GS}-V_{th}\right)^2}{1+\theta\left(V_{GS}-V_{th}\right)} \tag{3.19}$$

where θ models mobility degradation. Its nonlinear transconductance is represented

by a power series around the bias point:

$$i_{ds} = g_m v_{gs} + K_{2g_m} v_{gs}^2 + K_{3g_m} v_{gs}^3 + \cdots \tag{3.20}$$

where g_m is the transconductance, and $K_2 g_m = \frac{1}{2!}\frac{\partial^2 I_{DS}}{\partial V_{GS}^2}$ and $K_3 g_m = \frac{1}{3!}\frac{\partial^3 I_{DS}}{\partial V_{GS}^3}$ are higher order nonlinear coefficients. For simplicity, we neglect V_{DS} dependence of the drain current and assume linear intrinsic NMOS capacitances.

An intuitive but frequency independent explanation of the enhanced linearity of a closed loop feedback system is provided in [35]. The source degeneration due to R_S inherently linearizes the amplifier. The dual feedback network in the proposed circuit further linearizes the system with a loop gain of G_{loop}. The analytical expression for the overall amplifier IIP_3, denoted as $IIP_{3,closed}$, is given by

$$IIP_{3,closed} \approx IIP_{3,open} \cdot \left|1 + G_{loop}\right|^3, \tag{3.21}$$

where $IIP_{3,open}$ is the open loop amplifier IIP_3 without the dual negative feedback loops. To verify the preceding analysis, the circuits shown in Fig. 15(a) were simulated in Spectre RF with ideal linear elements for A_{fb} and B_{fb}, showing 6.2dB improvement at the designed bias point. However, the linearity of the closed-loop LNA has an upper bound that is set by the linearity of the feedback amplifier. The final LNA has a linearity enhancement of 2dB compared to the open-loop CG-LNA.

To calculate the frequency dependency of IIP_3, we apply a Volterra analysis [37] (detailed in Appendix B) to the simplified circuit shown in Fig. 20. Fig. 21 plots the resultant IIP_3 vs. the gate overdrive voltages (V_{eff}) of $M_{1,2}$. M_3 has a large overdrive voltage and hence a much smaller distortion. The device parameters used in the simulation are from the final LNA design bias point at $V_{\text{eff},1} = 180mV$ and $V_{\text{eff},2} = 130mV$ for M_1 and M_2 respectively. The IIP_3 performance is better with large effective gate voltage for the transistors M_1 and M_2, and is more sensitive with

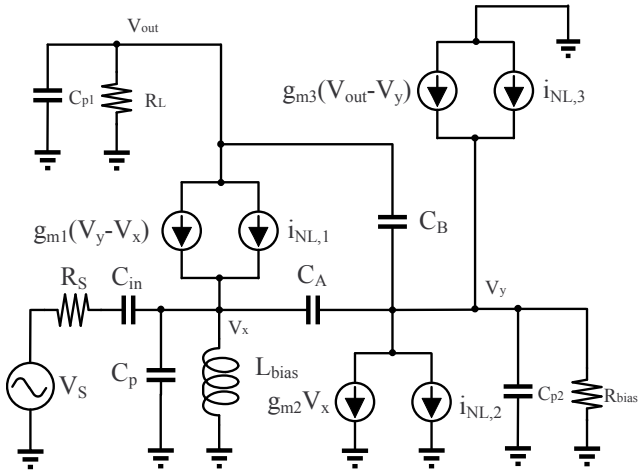


Fig. 20. Equivalent model for non-linearity computation in the proposed LNA.

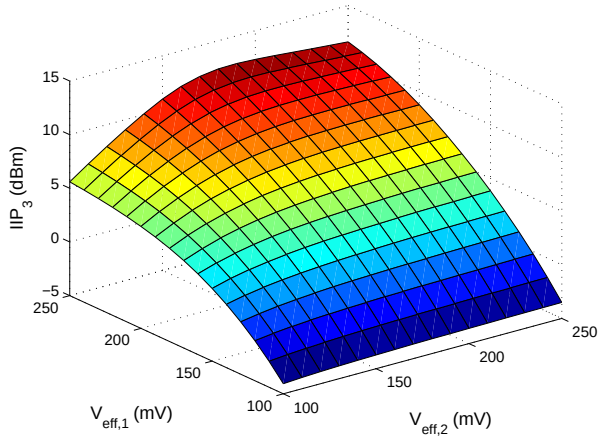
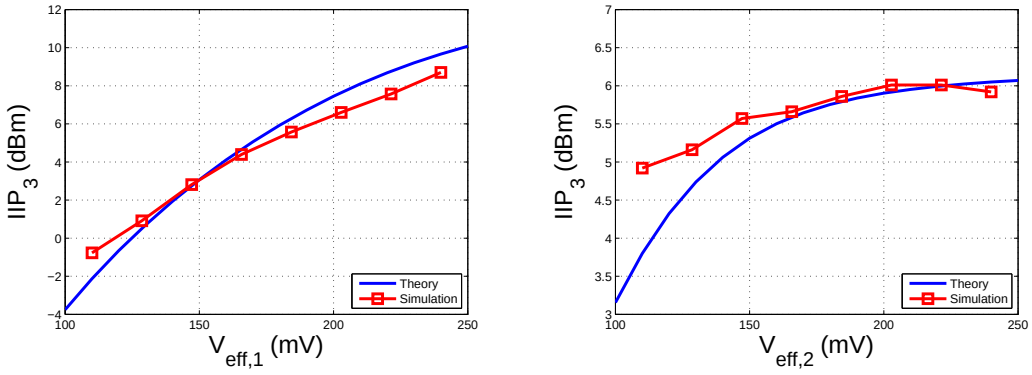


Fig. 21. Theoretical IIP3 at 2.4GHz versus $V_{\text{eff}} = V_{GS} - V_{th}$ of M_1 and M_2.



(a) (b)

Fig. 22. Theoretical (solid line) and simulated (dots) IIP3 at 2.4GHz versus (a) $V_{\text{eff},1} = V_{GS,1} - V_{th,1}$ and (b) $V_{\text{eff},2} = V_{GS,2} - V_{th,2}$.

the main transistor M_1 as expected. Fig. 22 shows the theoretical and simulated IIP_3 when the effective gate voltage of M_1 or M_2 is varied and the other is fixed at the designed LNA bias point. In the simulation for Fig. 22(a), the power supply is adjusted such that V_{DS} of the transistor M_1 is fixed after $I \cdot R$ drop due to resistive load. The theoretical and simulated IIP_3 match very well within 2dB difference.

D. Circuit Design and Layout Issues

1. Circuit Design

A dual negative feedback CG-LNA targeted for 1.2-5.2GHz was designed with triple-well RF transistors and metal-insulator-metal (MIM) capacitors in TSMC 0.18μm CMOS. Fig. 23 shows the final wideband CG-LNA with the source follower buffer. The target specifications are: 1) 17dB voltage gain; 2) NF $<$ 3dB; 3) current budget of 10mA; and 4) $IIP_3 >$ 0dBm. In this design, we set $g_{m1} = 1/R_S$, i.e. the conventional impedance-match value for a CG-LNA. The IIP_3 specifications require $V_{eff,1} = 200$mV and $V_{eff,2} = 130$mV. Given g_{m1}, we maximize R_L to minimize its

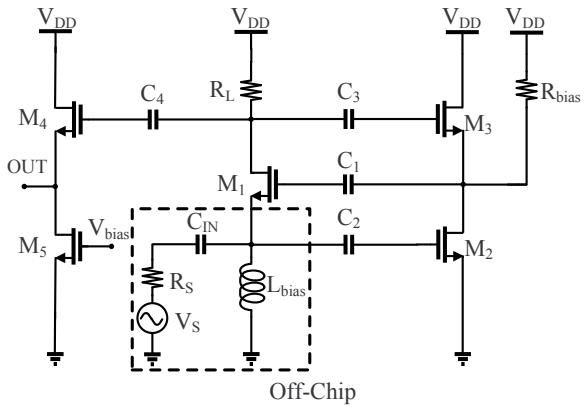


Fig. 23. Schematic of the proposed LNA with the buffer (biasing not shown).

noise contribution. From the voltage headroom constraint, we choose $R_L = 400\Omega$ ensuring M_1 operates in saturation region with a sufficient margin.

Based on the NF target specification, the total current consumption of 6mA is determined where (3.13) shows 2.4dB of NF. The induced gate noise and the gate resistance increases the predicted NF and this safety margin is necessary to achieve the targeted NF. Finally, the ratio g_{m2}/g_{m3} is determined from input matching condition given g_{m1} and R_L. The LNA is biased with a current mirror, which is not shown in Fig. 23 for simplicity. The final values of the device sizes are summarized in Table IV.

Table IV. Device dimension.

M_1	$(3\mu m/0.18\mu m) \times 16$
M_2	$(3\mu m/0.18\mu m) \times 64$
M_3	$(3\mu m/0.18\mu m) \times 10$
$C_{1,3}$	0.4 pF
C_2	1 pF
R_L	370Ω
R_{bias}	350Ω

We added a source follower to drive the 50Ω external measurement equipment. The g_m of the source follower is intentionally designed to be less than $1/R_{ext}$ with smaller device size to improve S_{22} at high frequency. A separate 1.8V power supply

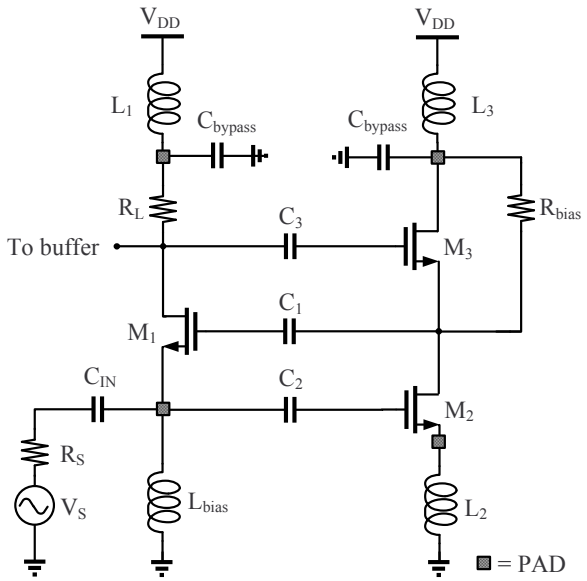


Fig. 24. Schematic of the proposed LNA with bondwire inductors.

is used with independent current mirror biasing for the design of the buffer.

2. Layout Issues

Wide-use of RF-MIM coupling capacitors gives design flexibility but causes signal loss because of parasitic substrate capacitance. Hence, we minimize AC coupling capacitance size to maximize the LNA's bandwidth. Shielded pads [38] are employed for RF input and output to prevent signal loss and noise from the resistive substrate. Shielded RF pads exhibit more capacitance to RF ground (Metal 1 shorted to ground), but this is not a major issue since it is resonated out with an off-chip inductor.

The schematic in Fig. 24 shows the pads and bondwire inductors. On-chip bypass capacitors null the effects of bondwire inductances L_1 and L_3. Bondwire inductance L_2 requires careful consideration since it alters the input impedance with a parasitic pole-zero pair. Assuming other parasitic effects are cancelled by the input-mathcing

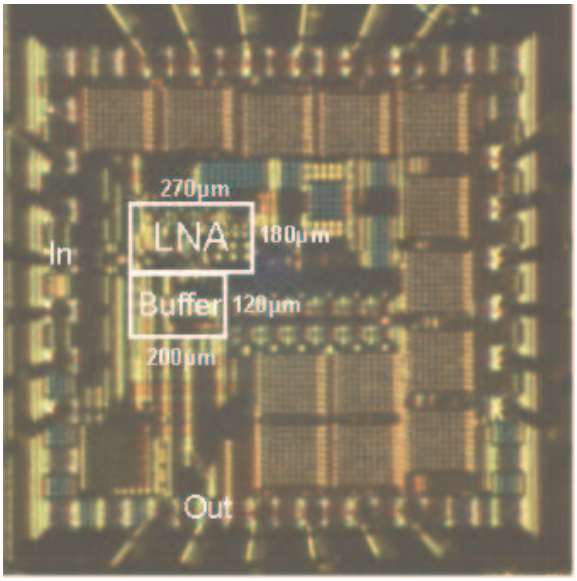


Fig. 25. Die photograph of the LNA.

LC resonator yields the following expression for input impedance:

$$Z_{in} = \frac{R_L + 1/g_{m1}}{1 + g_{m2}/g_{m3}} \cdot \frac{1 + sg_{m2}L_2}{1 + \frac{sg_{m2}L_2}{1+g_{m2}/g_{m3}}} \tag{3.22}$$

Then, multiple pads are connected but not in adjacent pads to decrease effective L_2 and mutual inductance.

E. Measurement Results

The circuit was designed and fabricated in TSMC 0.18μm CMOS technology and encapsulated in a QFN package. Fig. 25 shows the die photograph of the LNA. The active area is only 0.073mm^2 since no inductor is used on-chip. The chip was measured on FR-4 PCB.

Fig. 26 shows the measured and simulated S_{11}. The measured S_{11} is close to simulation up to 2.5GHz but degrades rapidly above the point. The measured S_{11} is below -10dB between 1.05 and 3.1GHz. We attribute the discrepancey to (1) insufficient self-resonant frequency (<10GHz) of off-chip inductor L_{bias} and (2) board

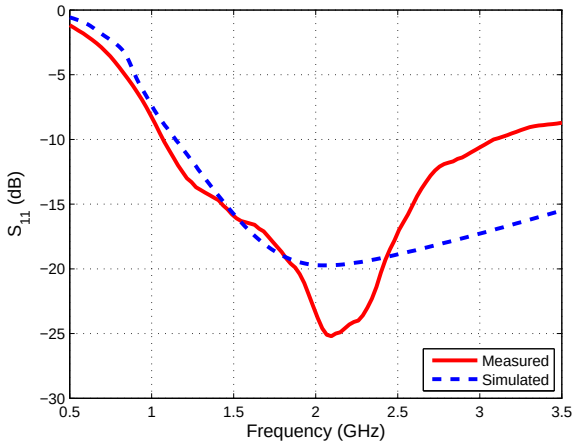


Fig. 26. Measured and simulated S_{11}.

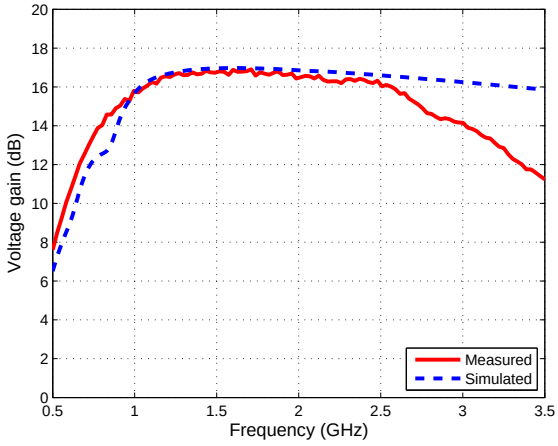


Fig. 27. Measured and simulated voltage gain versus frequency.

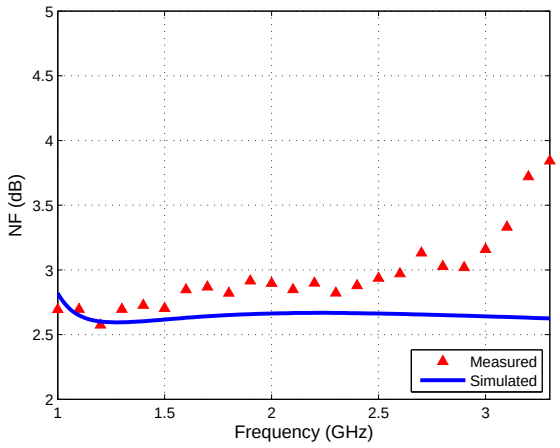


Fig. 28. Measured and simulated NF versus frequency.

parasitics in FR-4 substrate. Fig. 27 shows the measured voltage gain versus simulated voltage gain after deembedding the buffer effect. We measure a maximum voltage gain of 16.9dB and remains 1-dB flatness from 1.1 to 2.5GHz. The lower and upper 3-dB bandwidth is measured at 0.8GHz and 3.05GHz. The gain roll-off also starts at 2.5GHz where impedance matching degrades due to the board parasitics. Note that the 3-dB bandwidth (3.05GHz) almost exactly corresponds with the -10dB S_{11} bandwidth (3.1GHz).

The NF is measured within amplifier's 3dB bandwidth. As shown in Fig. 28, the NF varies between 2.57dB to 3.15dB within the amplifier's bandwidth. IIP_3 measurement was performed with the LNA and buffer as shown in Fig. 29. Two tones are applied with equal amplitude and a frequency spacing of 4MHz. The measured IIP_3 is 0.3dBm at 2.2GHz. Fig. 30 displays the IIP_3 as the location of the two tones are varied within the bandwidth. IIP_3 has a minimum of -0.7dBm for f_o =2GHz.

The measured performance of the dual negative-feedback LNA is summarized in Table V. Recently published works in wideband LNAs are compared with the proposed architecture. The circuit benefits from low NF and high linearity with

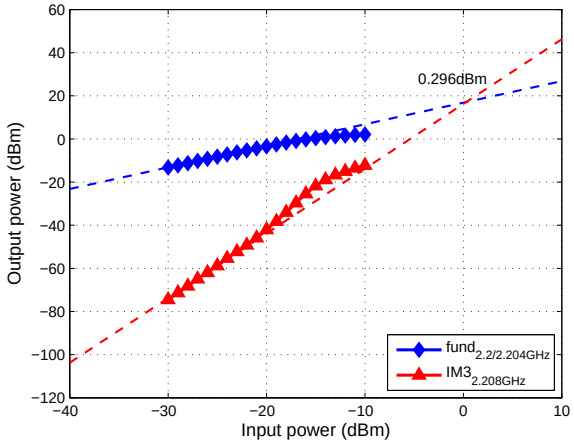


Fig. 29. Two-tone IIP_3 measurement results (f_o=2.2GHz).

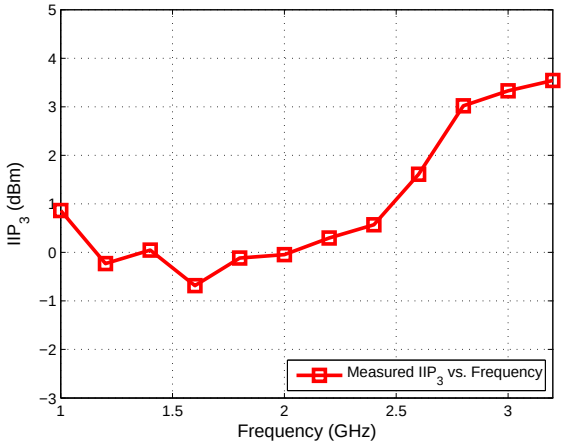


Fig. 30. Measured IIP_3 versus frequency.

Table V. Comparison of CG-LNA to recently published works.

	Technology	Frequency [GHz]	Gain [dB]	NF [dB]	IIP_3 [dBm]	Power [mW]	Supply [V]	Architecture	Area [mm^2]
[24]	$0.18\mu m$ CMOS	0.8-2.1	14.5	2.6***	16	17.4	1.5	single	0.099
[27]	$0.18\mu m$ CMOS	0.3-0.92*	21**	2 2.8***	-3.2	3.6	1.8	differential	0.33
[31]	$0.25\mu m$ CMOS	0.2-1.6*	13.7**	2.4	0	35	2.5	single	0.075†
[39]	$0.13\mu m$ CMOS	1.0-7.0	17**	2.7***	-4.1	25	1.4	differential	0.019†
[40]	$90nm$ CMOS	0-6.0*	17.4**	2.5	-8‡	9.8	1.2	single	0.002†
[41]	$90nm$ CMOS	0.5-6.0	25**	2	-14	42	2.7	single	0.025†
[42]	$0.18\mu m$ CMOS	2.3-9.2*	9.3	4 5.2***	-6.7	9	1.8	single	0.66†
[43]	$65nm$ CMOS	0.2-5.2*	15.6**	< 3.5	> 0	21	1.2	balun◇	0.01†
This Work	**$0.18\mu m$ CMOS**	**1.05-3.05***	**16.9****	**2.57 2.86*****	**-0.7**	**12.6**	**1.8**	**single**	**0.073†**

*Minimum of 3-dB bandwidth and S_{11}¡-10dB
**Voltage gain
***Average NF
†Active area size
‡Graphically estimated
◇Single-to-differential conversion

moderate power consumption.

F. Conclusions

A new wideband CG-LNA architecture is proposed with a detailed analysis and design guidelines. Theoretical analysis of the amplifier architecture demonstrated that the fundamental tradeoff between noise match (NF) and power match (S_{11}) can be overcome without degrading other design parameters.

Measurement results of the dual negative-feedback CG-LNA realized in 0.18μm CMOS demonstrate 16.9dB maximum voltage gain, 2.57dB minimum NF, better than -10dB input matching and -0.7dBm minimum IIP3 from 1.05 to 3.05GHz, while dissipating 7mA from 1.8V supply. A comparison of measurement results with the recently published wideband LNAs shows that the proposed dual negative-feedback CG LNA achieves superior noise and linearity performance with moderate power consumption using a mainstream technology.

CHAPTER IV

WIDEBAND INDUCTOR-LESS BALUN-LNA EMPLOYING FEEDBACK WITH NOISE AND DISTORTION CANCELLING

A. Introduction

Recently, multi-standard radio receivers have drawn strong attention and future wireless communication devices must support multiple standards and features on a single chip. Low-noise-amplifier (LNA), as the first active block in receiver, must have good impedance matching, low noise, and high linearity across a wide frequency band. The conventional solution is to employ several LC-tuned LNAs in parallel to cover dedicated small band over the wanted frequency span [16, 17]. The other extreme is a wideband LNA [44] with more flexibility and better efficiency in terms of form factor, cost, and power, but its performance must be comparable to or even better than narrowband tuned LNAs due to concurrent reception of multi-standard signals unfiltered.

Balanced and symmetrical architecture is preferred to an unbalanced one due to its robustness to power supply and substrate noise. Second-order distortion in the receive chain is significantly reduced when differential (balanced) signaling in the receive chain is adopted. However, antennas and RF filters typically produce single-ended I/O and, thus, adding a single-to-differential circuitry in the receiver chain is a must [45, 46]. Passive components have been used to implement the single-to-differential but the form-factor is usually excessive and, therefore, is not suitable for integrated circuit operations [47, 48]. Also, passive balun is lossy and narrowband so that several components dedicated to each frequency band are required for wideband operation, leading to higher costs. Current state of the art RF systems with high

sensitivity requirement demands high performance balun, which are not lossy and area efficient. Active-Balun fits the requirements very well, which provides positive gain and small noise contribution in a wideband fashion. Several topologies have been devised and those include a single transistor with common-source and common-drain (source follower) outputs [45, 49], a differential pair with a single input AC grounded [50–52], and common-source (CS) and common-gate (CG) pair for 180 degree phase shift [43, 53, 54].

In this chapter, we present an inductorless Balun-LNA based on the CG-CS topology. Previous works [43, 53] have shown that CG-CS topology with trans-conductance scaling in CS stage can achieve sufficient low noise figure (< 3dB) with balanced output, noise and distortion cancellation. However, the noise and headroom issue due to the biasing of CG stage was not fully accounted for, and the previous works used either noisy resistor bias in [43], or noiseless and bulky inductor in [53]. The passive device acting as a current source suffers from process, voltage, and temperature (PVT) variations as well, in contrast to the stable operation with an active device based on current-mirror. The proposed architecture employing negative feedback features lower power and wider bandwidth with minimal noise contribution due to the active current source. The frequency compensation in CS stage ensures better gain and phase balance, whereas previous works [43, 53] show different frequency response between CG and CS stage due to trans-conductance scaling.

This chapter is structured as follows. Section B reviews the active-balun topologies and their properties. Section C describes the proposed inductorless balun-LNA and derives analytical expressions for input impedance, gain, bandwidth, NF, and output balancing. Section D provides simulation results, and the concluding remarks are given in Section E.

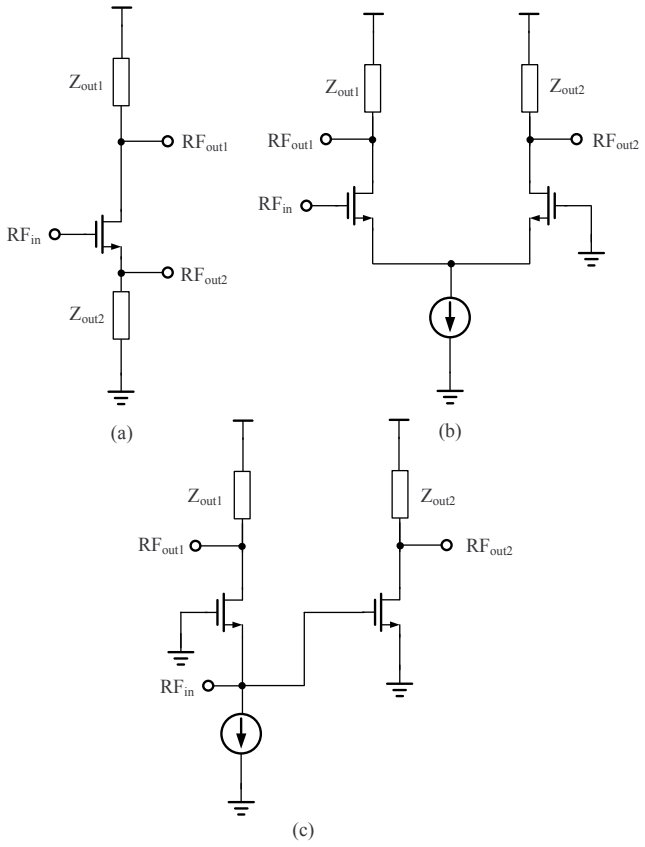


Fig. 31. Active-balun topologies: (a) A single transistor topology, (b) Differential topology with a single input AC grounded, and (c) CG-CS topology.

B. Active-Balun Topologies and Their Properties

There exists passive and active differential phase shifters or baluns. Passive balun due to its lossy and bukly nature, is not suitable for integrated circuit operations and, thus, are not considered further.

Fig. 31 shows several active-balun topologies that have been proposed in past and present literature [43, 45, 49–54]. A single transistor topology in Fig. 31(a) with 180 anti-phase outputs at drain and source of transistor is probably the simplest implementation of active-balun. The single transistor topology, however, do not have even signal leakage to the drain and source at high frequency due to assymetric

parasitics at both outputs. In order to achieve a good balance at high frequency ($>$ 1GHz), a dummy transistor to compensate for unequal parasitics is deliberately added in [45], but requires careful simulation to ensure gain and phase balance. Cross connection of three single transistor phase shifter is utilized to cancel the imbalance between differential output in [49] at the expense of degradation in other performances (e.g., noise and linearity) due to the cascaded structure.

Fig. 31(b) shows the differential topology where one arm of differential pair is AC grounded. RF signal applied to the gate of one of differential pair transistor ideally flows through two symmetric branches with the same magnitude and an inverse direction [55]. Two non-idealities limit the balance of differential pair topology, which are finite impedance of current source and feed-forward path mainly due to C_{gd} of differential pair transistor. The effect of non-idealities on output balance performance can be analyzed separately without losing its generosity. When the parasitic capacitance of common-source node and the finite resistance of current source are included with $C_{gd} = 0$, the differential output voltage can be obtained as follows.

$$v_{out1} = -\frac{g_m}{2} \cdot \frac{\left(1 + \frac{g_x}{g_m}\right)\left(1 + s\frac{C_{gs}+C_x}{g_m+g_x}\right)}{\left(1 + \frac{g_x}{2g_m}\right)\left(1 + s\frac{C_x+2C_{gs}}{g_x+2g_m}\right)\frac{1}{Z_{out1}}} \cdot v_{in}, \tag{4.1}$$

$$v_{out2} = \frac{g_m}{2} \cdot \frac{\left(1 + s\frac{C_{gs}}{g_m}\right)}{\left(1 + \frac{g_x}{2g_m}\right)\left(1 + s\frac{C_x+2C_{gs}}{g_x+2g_m}\right)\frac{1}{Z_{out2}}} \cdot v_{in}, \tag{4.2}$$

where C_x is parasitic capacitance at the common-source node, g_x is the finite conductance of current source, and g_m is the trans-conductance of differential pair. It is seen from (4.1), (4.2) that there are two source of error; low-frequency magnitude mismatch and location of the zero.

The effect due to C_{gd} only incurs imbalance for differential output, whose expression is shown below

$$v_{out1} = -\frac{\frac{g_m}{2} - sC_{gd}}{\frac{1}{Z_{out1}} + sC_{gd}} \cdot v_{in}, \tag{4.3}$$

$$v_{out2} = \frac{\frac{g_m}{2}}{\frac{1}{Z_{out2}} + sC_{gd}} \cdot v_{in}. \tag{4.4}$$

A right-hand-plane (RHP) zero has been introduced at the inverting output due to feed-forward path, whereas it is not present in the expression of the non-inverting output voltage.

The imbalance due to these effects prevents the use of differential pair topology at high frequency. One solution is to feed back a fraction of the single-ended output signal to the second transistor [52]. Feed-forward path from the input node to non-inverting output node can be employed to shift the zero of non-inverting output voltage to a lower frequency [55].

CG-CS topology in Fig. 31(c) has drawn close attention due to its advantageous properties such as noise and distortion cancellation [43, 53, 54]. Blaakmeer et al. [43] demonstrated that, by trans-conductance scaling, CG-CS topology can provide wideband matching, noise and distortion cancellation, and output balancing. This work shows the output balacing condition at low frequency but does not explictly show how differential output can be balanced at high frequency especially when trans-conductance of CS stage is scaled ($>$ 4x) although the measurement shows good gain and phase balance up to 3.5GHz. In [54], local feedback is utilized to boost the trans-conductance of CG stage. However, the feedback signal is from cascode node of CS stage where low signal swing is desired to minimize the miller effect and enhance the frequency response. Also, the resistor bias is used for CG stage susceptible to PVT variations.

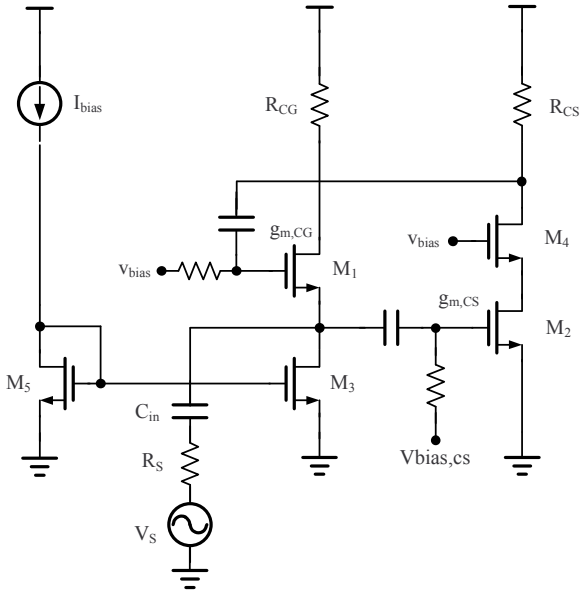


Fig. 32. Schematic of inductor-less balun-LNA employing feedback.

C. Wideband Inductor-Less Balun-LNA

Fig. 32 shows the proposed wideband inductor-less balun-LNA employing feedback. The compensation scheme for output balance is not shown here not to clutter the schematic of the proposed balun-LNA. Impedance matching device M_1 amplifies the signal and provides the main non-inverting signal path in CG configuration. The common-source (CS) amplifier due to M_2 ideally shows 180 degree phase shift with respect to non-inverting CG stage. The inherent inverting gain of the CS stage is utilized to boost the trans-conductance of M_1 and, therefore, the required $g_{m,CG}$ can be reduced by a factor of $1 + A_{V,CS}$, where $A_{V,CS}$ is the gain of CS stage. Device size and its power consumption in CG stage is reduced as well and its reduction factor is design dependent. Additional benefit from the feedback is noise-suppression of CG stage bias transistor (M_3) with minimal headroom due to M_3. With the given

bias current from input match ($R_{in} = 50\Omega$) condition, the only way to minimize the noise contribution due to M_3 is to lower its noise source ($\overline{i_n^2/\Delta f} = 4kTg_{m,M3}$) at the expense of headroom ($V_{ov,M3}$). Hence, there is a trade-off between noise contribution due to CG stage bias transistor and its headroom. Low noise design dictates the high supply required and both can not be optimized at the same time. Previous works in [43, 53] used either noisy resistor bias with large resistance ($> 300\Omega$) to minimize noise at the expense of voltage drop, or noiseless and area-inefficient inductor. The proposed architecture maintains the noise and distortion cancellation property of the original circuit with lower power and better bandwidth. Two frequency compensation schemes to balance gain and phase of differential outputs are proposed and will be discussed in Section C.3.

1. Input Match

The input impedance of the inductorless balun-LNA employing negative feedback at low frequency can be easily evaluated by the Blackman's formula [56, 57] as

$$Z_{in} = Z_{in,open} \cdot \frac{1 + RR(port\ short\ circuited)}{1 + RR(port\ open\ circuited)}, \tag{4.5}$$

where $Z_{in,open}$ is the input impedance with the feedback broken. Since the input impedance of CS stage is capacitive, the real part of input impedance with the feedback broken is given from $1/g_{m,CG}$ of CG stage. For the series-shunt (voltage-voltage) feedback in the proposed architecture, shorting the port kills the feedback. Then, (4.5) can be further simplified to

$$Z_{in} = \frac{Z_{in,open}}{1 + RR(port\ open\ circuited)}, \tag{4.6}$$

The input impedance of Balun-LNA in terms of device parameters can be found

as

$$Z_{in} = \frac{1}{g_{m,CG}\left(1 + g_{m,CS} \cdot \left(R_{CS} \parallel \frac{1}{sC_2}\right)\right)} \parallel \frac{1}{sC_p} \tag{4.7}$$

where R_{CS} and C_2 are output resistance and capacitance of CS stage respectively, and parasitic capacitor C_p arises from the input pad, M_1, M_2, and M_3. The device size in the proposed architecture is much smaller and, furthermore, the circuitry does not suffer from miller effect due to C_{gd} of M_2 in contrast to the architecture in [54].

2. Noise Analysis

CG-CS topology is a well known architecture and has been widely used [58,59]. Property of noise and distortion cancellation due to CG stage was not cleary stated before, and recent works in [43, 53, 54] better utilized the property with trans-conductance ($g_{m,CS}$) scaling of CS stage. The detailed analysis for noise figure (NF) of previous work without series-shunt feedback is a little tedious and is shown below without proof.

$$\begin{aligned} NF \;=\; 1 &+ \underbrace{\frac{\gamma g_{m,CG} \cdot \left(R_{CG} - R_S \cdot g_{m,CS} \cdot R_{CS}\right)^2}{R_S \cdot A_V^2}}_{M_1(CG)\ contribution} \\ &+ \underbrace{\frac{\gamma g_{m,CS} \cdot R_{CS}^2 \cdot \left(1 + g_{m,CG} \cdot R_S\right)^2}{R_S \cdot A_V^2}}_{M_2(CS)\ contribution} \\ &+ \underbrace{\frac{\left(R_{CG} + R_{CS}\right) \cdot \left(1 + g_{m,CG} \cdot R_S\right)^2}{R_S \cdot A_V^2}}_{load\ resistor\ contribution} + \underbrace{\gamma \cdot g_{m,bias} \cdot R_S}_{M_3(bias)\ contribution} \end{aligned} \tag{4.8}$$

where A_V is differential voltage gain expressed as

$$A_V = g_{m,CG} \cdot R_{CG} + g_{m,CS} \cdot R_{CS}. \tag{4.9}$$

Assuming square-law behavior of MOS transitor in saturation under impedance match condition ($R_S = 1/g_{m,CG}$), (4.8) can be rewritten as

$$\begin{aligned} NF &= 1 + \underbrace{\frac{\gamma g_{m,CG} \cdot \left(R_{CG} - R_S \cdot g_{m,CS} \cdot R_{CS}\right)^2}{R_S \cdot A_V^2}}_{M_1(CG)\ contribution} \\ &\quad + \underbrace{\frac{\gamma g_{m,CS} \cdot R_{CS}^2 \cdot \left(1 + g_{m,CG} \cdot R_S\right)^2}{R_S \cdot A_V^2}}_{M_2(CS)\ contribution} \\ &\quad + \underbrace{\frac{\left(R_{CG} + R_{CS}\right) \cdot \left(1 + g_{m,CG} \cdot R_S\right)^2}{R_S \cdot A_V^2}}_{load\ resistor\ contribution} + \underbrace{\gamma \cdot \frac{V_{ov,CG}}{V_{ov,bias}}}_{M_3(bias)\ contribution} \end{aligned} \tag{4.10}$$

where $V_{ov,CG}$ and $V_{ov,bias}$ are overdrive voltage of M_1 and M_3, respectively. It is explicit from (4.10) that the noise contribution due to current source (M_3) has a direct trade-off with its headroom ($V_{ov,bias}$). A similar conclusion can be drawn if the resistor is used for CG bias [43]. The thermal noise of resistor ($\overline{i_n^2/\Delta f} = 4kT/R_{bias}$) can be reduced if its value is increased at the expense of headroom (voltage drop). 350Ω resistor is used for CG bias to minimize its noise contribution in [43]. The work in [53] is free of noise due to bias since noiseless inductor (RF choke) is used to bias the CG stage at the expense of chip area.

Fig. 33 shows NF of CG-CS topology when negative series-shunt feedback is not used. The trans-conductance scaling of CG stage is represented by $N = g_{m,CS}/g_{m,CG}$ and $g_{m,CG}$ is set to be 20mS to ensure ideal input impedance matching with reactive terms ignored. $R_{CG} = 200\Omega$ is given from the assumption that both M_1 and M_3 have 0.3V of overdrive voltage with 1.2V supply. From the input impedance match condition ($g_{m,CG} = 20mS$), $R_{CG} = 200\Omega$ requires 0.6V of voltage drop under classic square-law behavior of MOS in saturation ($g_m = \frac{2 \cdot I}{V_{ov}}$). The noise contribution due to

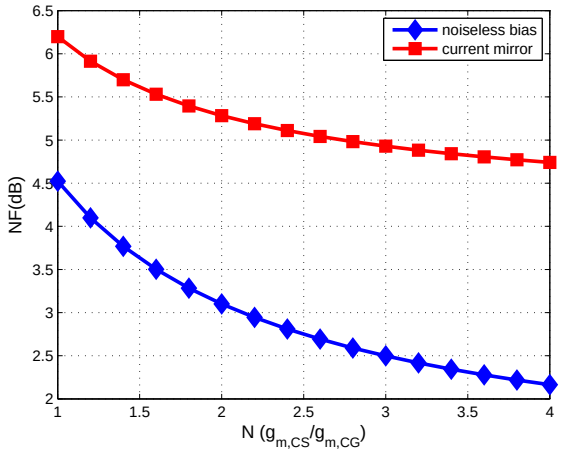


Fig. 33. NF vs. $g_{m,CS}$ scaling with and without noise contribution due to CG bias at $R_{CG} = 200$, $R_{CS} = 200/n$, and $\gamma = \frac{4}{3}$.

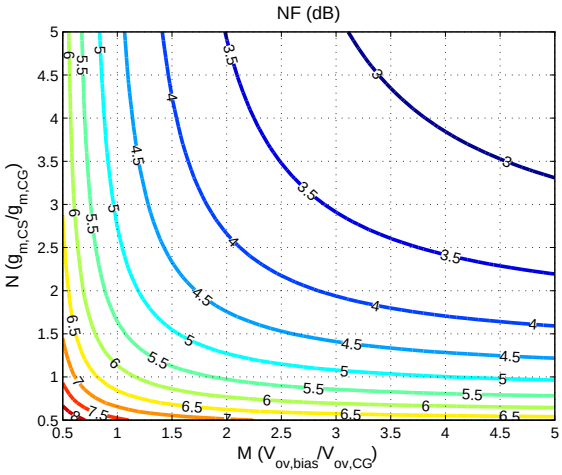


Fig. 34. NF vs. $g_{m,CS}$ and $V_{ov,bias}$ scaling at $R_{CG} = 200$, $R_{CS} = 200/n$, and $\gamma = \frac{4}{3}$.

current mirror bias with $\overline{i_n^2/\Delta f} = 4kT\gamma g_{m,bias}$ is not negligible and should be carefully evaluated. Noise performance can be enhanced when the headroom due to current mirror is sacrificed. V_{ov} scaling denoted as M in addition to $g_{m.CS}$ scaling can further improve NF of the active-balun based on CG-CS topology. Fig. 34 clearly shows that only due to scaling of both the $g_{m,CS}$ and $V_{ov,bias}$ scaling, denoted as N and M respectively, can the converntional CG-CS topology achieve sufficient low NF. NF of the proposed architecture employing feedback can be expressed as

$$\begin{aligned} NF &= 1 + \underbrace{\frac{\gamma g_{m,CG} \cdot (R_{CG} - R_S \cdot g_{m,CS} \cdot R_{CS})^2}{R_S \cdot A_V^2}}_{M_1(CG)\ contribution} \\ &\quad + \underbrace{\frac{\gamma g_{m,CS} \cdot R_{CS}^2 \cdot (1 + g_{m,CG} \cdot (R_{CG} + R_S))^2}{R_S \cdot A_V^2}}_{M_2(CS)\ contribution} \\ &\quad + \underbrace{\frac{(R_{CG} + R_{CS}) \cdot (1 + g_{m,CG} \cdot (1 + A_{V,CS}) \cdot R_S)^2}{R_S \cdot A_V^2}}_{load\ resistor\ contribution} \\ &\quad + \underbrace{\gamma \cdot \frac{V_{ov,CG}}{V_{ov,bias} \cdot (1 + A_{V,CS})}}_{M_3(bias)\ contribution} \end{aligned} \tag{4.11}$$

where A_V is differential voltage gain of the proposed architecture and $A_{V,CS}$ is the $g_{m,CG}$ boosting factor expressed as

$$A_{V,CS} = g_{m,CS} \cdot R_{CS}. \tag{4.12}$$

$$A_V = g_{m,CG} \cdot (1 + A_{V,CS}) \cdot R_{CG} + g_{m,CS} \cdot R_{CS}. \tag{4.13}$$

The second term in (4.11) represents the noise contribution of CG transistor M_1 and its noise is totally cancelled when the output is balanced. The third term

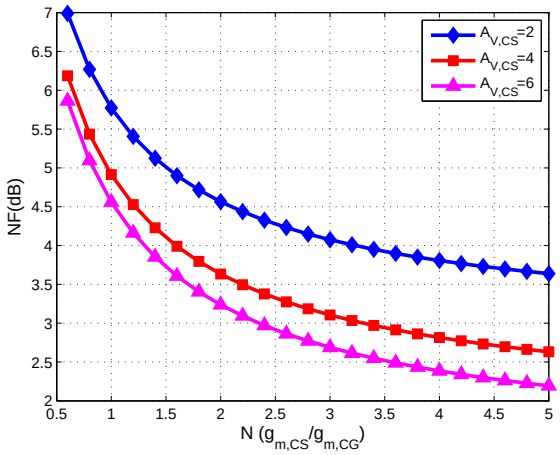


Fig. 35. NF vs. $A_{V,CS}$ at $\gamma = \frac{4}{3}$ and $\frac{V_{ov,bias}}{V_{ov,CG}} = 1$.

represents the thermal noise contribution of CS transistor M_2. It is not apparent but can be shown that the noise due to M_2 is minimized with larger loop gain ($A_{V,CS}$). The last term accounts for the noise due to CG stage bias and its noise is suppressed by the factor, $1 + A_{V,CS}$, compared to the conventional topology [43, 53]. Fig. 35 shows that the noise performance with enough loop gain ($A_{V,CS} > 2$) can achieve the sufficient low NF even without V_{ov} scaling.

3. Gain and Phase Balance and Their Compensation

The transfer function from v_x to the non-inverting and inverting stage output is derived to obtain the gain and phase error of the proposed Balun-LNA with parasitic capacitance effects shown in Fig. 36. The transfer function from the port to v_x does not incur imbalance and, thus, not considered in the derivation. C_a is the total capacitance due to M_1, M_2, and M_3. C_b is the parastitic effects at the drain of M_2

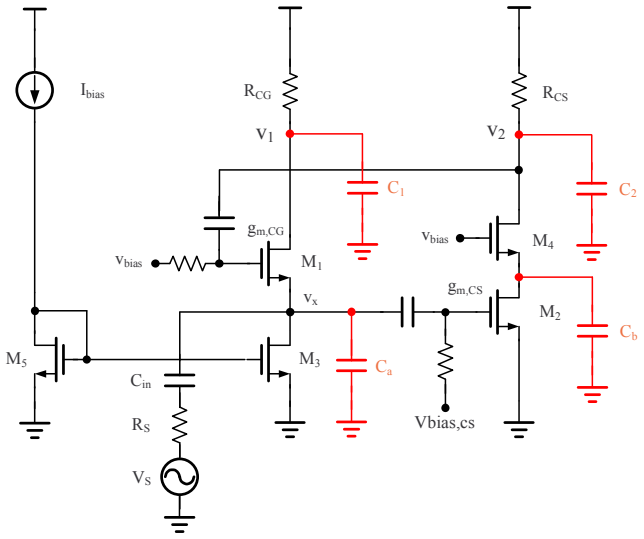


Fig. 36. Balun-LNA with parasitic capacitance for gain and phase imbalance analysis.

and source of M_4. The approximate capacitance of C_a and C_b is given by

$$\begin{aligned} C_a &\approx C_{gd3} + C_{db3} + C_{gd2}(1 + g_{m,CS}/g_{m4}) \\ &\quad + C_{gs2} + C_{sb1} + C_{gs1}(1 + g_{m,CS} \cdot R_{CS}) \qquad (4.14) \\ C_b &\approx C_{gd2} + C_{db2} + C_{gs4} + C_{sb4}, \qquad (4.15) \end{aligned}$$

where miller approximation is utilized to capture the capacitance boosting due to feedback. The voltage gain from v_x to the CS (inverting) stage output is derived as

$$\frac{v_2}{v_x} = -\frac{g_{m,CS} \cdot R_{CS}}{1 + sR_{CS} \cdot C_2} \cdot \frac{1}{1 + s \cdot \frac{C_b}{g_{m4}}}. \qquad (4.16)$$

The non-dominant pole (g_{m4}/C_b) due to the cascode device is order of magnitude higher than the dominant pole ($=1/R_{CS} \cdot C_2$) at the output of the CS stage and is neglected in the following derivation. Small signal analysis of Fig. 36 shows that the

high-frequency voltage gain of CG (non-inverting) stage is given by

$$\frac{v_1}{v_x} = \frac{g_{m,CG} \cdot (1 + g_{m,CS} \cdot R_{CS}) \cdot R_{CG} \cdot (1 + s\frac{R_{CS} \cdot C_2}{1 + g_{m,CS} \cdot R_{CS}})}{(1 + sR_{CG} \cdot C_1)(1 + sR_{CS} \cdot C_2)}. \tag{4.17}$$

From (4.16) and (4.17), the output balance at low-frequency is satisfied when noise and distortion canceling conditions are met. The dominant pole of the CS stage generates the pole and zero pair in the CG stage due to the feedback in addition to the pole at the output of CG stage. Since the pole at $(=1/R_{CS} \cdot C_2)$ is common for CG and CS stage, the gain and phase imbalance can be expressed as

$$\begin{aligned} \Delta\phi &= \phi_{v_1} - \phi_{v_2} \\ &= \tan^{-1}\left(\frac{\omega \cdot R_{CS} \cdot C_2}{1 + g_{m,CS} \cdot R_{CS}}\right) - \tan^{-1}(\omega \cdot R_{CG} \cdot C_1) \end{aligned} \tag{4.18}$$

$$\begin{aligned} \Delta v &= 20\log_{10}(v_1) - 20\log_{10}(v_2) \\ &= \log_{10}\left(\sqrt{\frac{1 + \left(\frac{\omega \cdot R_{CS} \cdot C_2}{1 + g_{m,CS} \cdot R_{CS}}\right)^2}{1 + (\omega \cdot R_{CG} \cdot C_1)^2}}\right) \end{aligned} \tag{4.19}$$

Taking into consideration the effect of $g_{m,CG}$ boosting $(T = g_{m,CS} \cdot R_{CS})$ and $g_{m,CS}$ scaling $(g_{m,CS} = N/R_S)$, the gain and phase imbalance due to the zero are negligible. The dominant pole is determined by $1/R_{CG} \cdot C_1$ and the zero is pushed to high frequency by the factor $N \cdot T$.

The imbalance in gain and phase is predictable in the proposed Balun-LNA at high frequency due to the pole at the output of CG stage. The capacitor between CG and CS stage output shown in Fig. 37 can be included to compensate for the gain and phase imbalance. With the compensation capacitor C_3 only (i.e., $R_{gate} = 0$), the

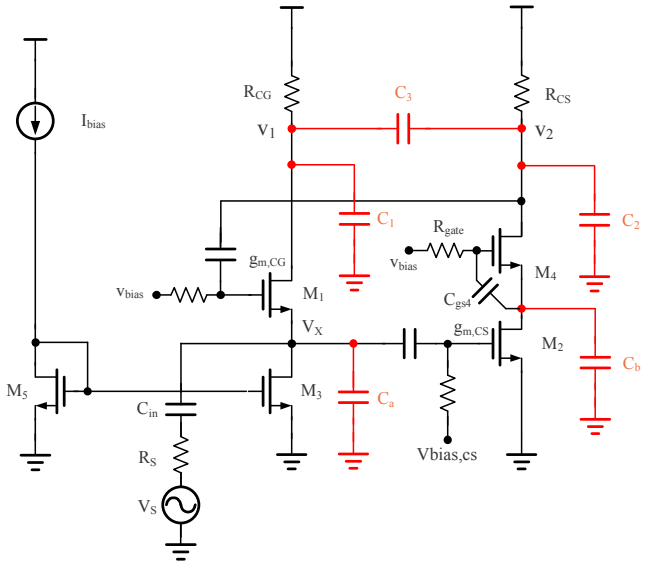


Fig. 37. Balun-LNA with gain and phase compensation network.

transfer function can be derived as

$$\begin{aligned}\frac{v_2}{v_x} &= -\frac{g_{m,CS}\cdot R_{CS}\cdot\left\{1+s\cdot R_{CG}\cdot\left(C_1+C_3-\frac{g_{m,CG}}{g_{m,CS}}\cdot C_3\right)\right\}}{1+a\cdot s+b\cdot s^2}\\ \frac{v_1}{v_x} &= \frac{g_{m,CG}\cdot(1+g_{m,CS}\cdot R_{CS})\cdot R_{CG}\cdot\left\{1+s\frac{R_{CS}\cdot C_2}{1+g_{m,CS}\cdot R_{CS}}\right\}}{1+a\cdot s+b\cdot s^2},\end{aligned} \tag{4.20}$$

where a and b are as follows.

$$\begin{aligned}a &= R_{CG}\cdot C_1+R_{CS}\cdot C_2\\ &\quad +(R_{CG}+R_{CS}+g_{m,CG}\cdot R_{CG}\cdot R_{CS})\cdot C_3 \qquad (4.21)\\ b &= R_{CG}\cdot R_{CS}\cdot(C_1+C_2)\cdot C_3 \qquad (4.22)\end{aligned}$$

Perfect balance in gain and phase can then be achieved by equating two transfer functions. Since the natural response (pole) of the system are equivalent, the condition

of equal zero in inverting and non-inverting output stage leads to the following:

$$C_3 = \frac{k \cdot C_2 - C_1}{1 - k} \tag{4.23}$$

where $k = \frac{g_{m,CG}}{g_{m,CS}} (= \frac{1}{N \cdot (1+T)}) \ll 1$ is the ratio of common-gate and common-source amplifier transconductance.

The short-coming of the proposed compensation is the dependency on the parasitic capacitance value of differential outputs (C_1 and C_2) and, therefore, the required compensation component can be either capacitive or inductive. The loading due to the next stage (e.g., mixer) is symmetrical and usually more dominant than the parasitic of Balun-LNA at the differential output node in the typical implementation, and therefore C_3 is negative (inductive) with $k \ll 1$ and $C_1 \approx C_2$.

The alternative compensation scheme that is employed for the proposed balun-LNA is the use of gate resistance for the cascode transistor. The gate resistance of the cascode transistor can be beneficial for both differential output symmetry (balance) and stability. As capacitively degenerated device exhibits negative real impedance in contrast to positive real impedance synthesis widely adopted for inductor degenerated LNA [20,29], parasitic inductance at the gate of cascode can form a colpitts oscillator. Therefore, the gate resistance added de-Q the resonator and improves the stability [60]. From the current transfer perspective from CS stage to CG stage due to cascode transistor, the gate resistance added modifies the frequency response in CS (inverting) stage. The voltage gain from v_x to the CS (inverting) stage output with R_{gate} only is now expressed as

$$\frac{v_2}{v_x} = -\frac{g_{m,CS} \cdot R_{CS}}{1 + sR_{CS} \cdot C_2} \cdot \frac{1}{1 + s \cdot \frac{C_{gs4}+C_b}{g_{m4}} + s^2 \cdot \frac{R_{gate} \cdot C_{gs4} \cdot C_b}{g_{m4}}}. \tag{4.24}$$

where R_{gate} is the gate resistance added for the cascode transistor. The current

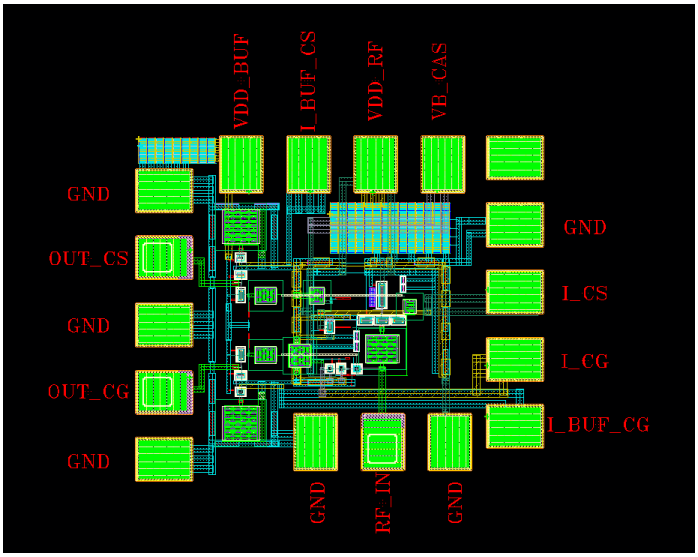


Fig. 38. Die photograph of the balun-LNA.

transfer due to cascode transistor is second-order with R_{gate} added and can serve as a compenation network. Without R_{gate}, non-dominant pole due to the cascode is much higher than the dominant pole as shown in (4.16) and is negligible. A stabilizing and compensating resistor of $R_{gate} = 140\Omega$ is chosen based on the trade-off between output symmetry and NF degradation due to R_{gate}.

D. Simulation Results

The circuit was designed in TSMC 0.13μm CMOS technology and extracted with calibre. Fig. 38 shows the die photograph of the Balun-LNA with probe buffer. The active area of the chip and Balun-LNA core are only 250μm $\times$ 300μm and 170μm $\times$ 150μm respectively, since no inductor is used on-chip.

Fig. 39 shows simulated impedance matching performance (S_{11}) and power gain (S_{21}) of Balun-LNA core and the probe buffer. The simulated S_{11} is below -10dB between 0.5 and 4GHz. The maximum power gain (S_{21}) is 7.6dB and remains 1-dB

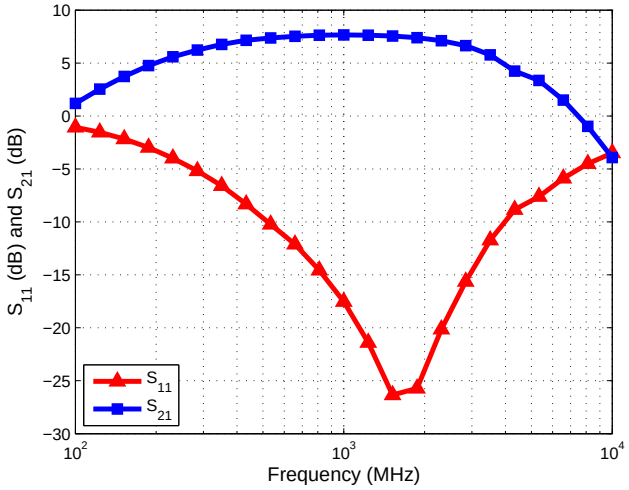


Fig. 39. Simulated S_{11} and S_{21}.

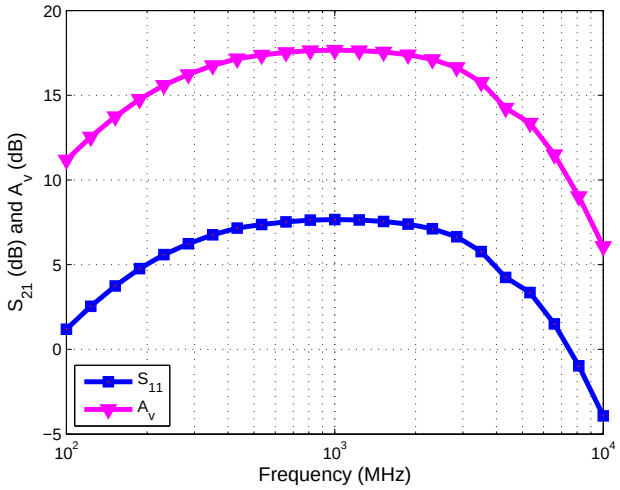


Fig. 40. Simulated power gain (S_{21}) and voltage gain (A_V) of Balun-LNA core.

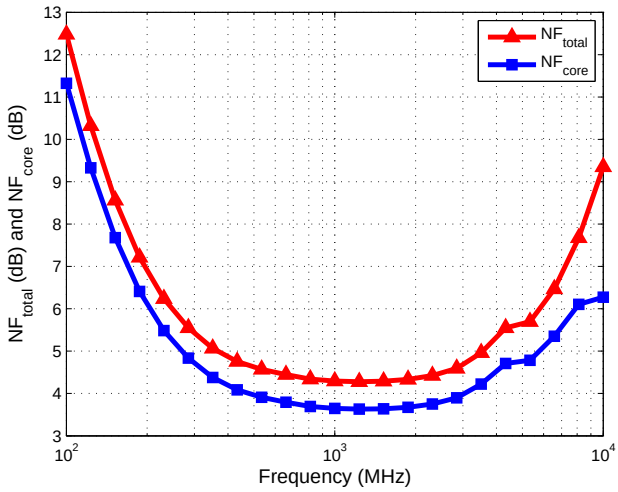


Fig. 41. Simulated NF and NF of balun-LNA core versus frequency.

flatness from 0.35 to 2.8GHz. The lower and upper 3-dB bandwidth is measured at 0.2GHz and 4GHz. AC coupling capacitors attenuate low frequency signals, and the parasitic capacitors C_a, C_b, C_1, and C_2 attenuate high-frequency signals. Therefore, the proposed Balun-LNA shows band-pass type of response in its impedance matching and power gain although the circuit itself is broadband from DC.

Fig. 40 shows the simulated voltage gain after deembedding the probe buffer effect. The probe buffer output impedance ($\frac{1}{g_{m,buffer}}$) is designed to be larger than 50Ω with smaller parasitics to extend the output matching bandwidth. Then, the loss due to the probe buffer is 6.8dB. Another 3dB is added to reflect the conversion from 50Ω input to 100Ω output.

Fig. 41 shows the simulated NF of Balun-LNA and the probe buffer and NF of Balun-LNA core only after de-embedding the probe buffer effect. The de-embedding procedure is detailed in Appendix C. The NF varies between 3.56dB to 4.2dB within the amplifier's bandwidth. The linearity test (IIP_3) was performed with the Balun-LNA and the probe buffer as shown in Fig. 42. Two tones are applied with equal

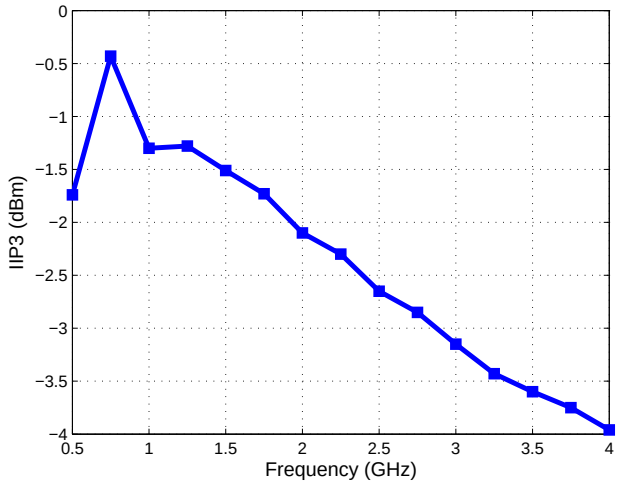


Fig. 42. Simulated IIP_3 versus frequency.

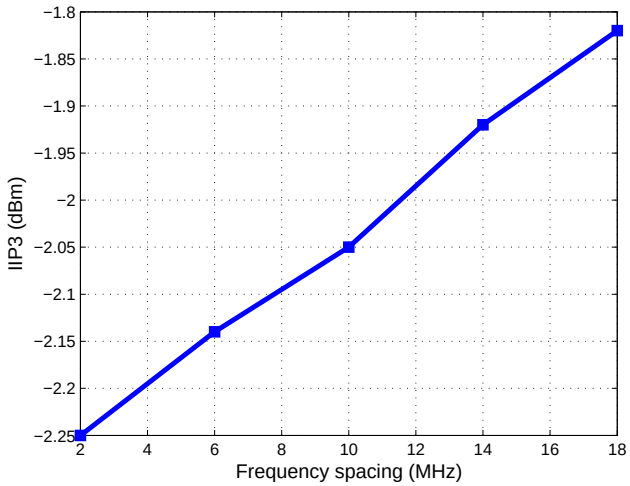


Fig. 43. Simulated IIP_3 versus two-tone frequency spacing.

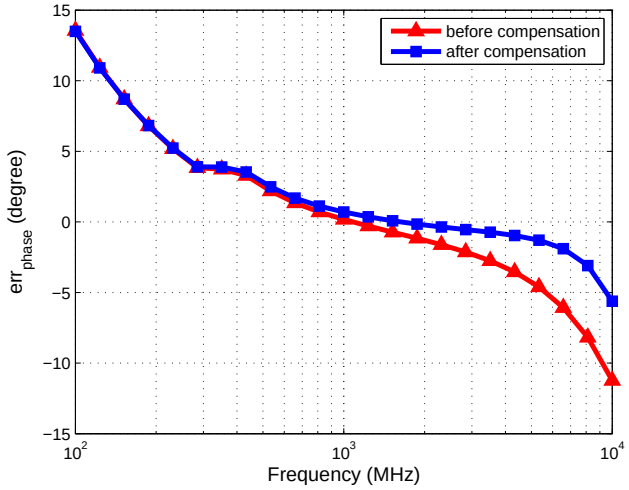


Fig. 44. Phase balance with and without compensation network.

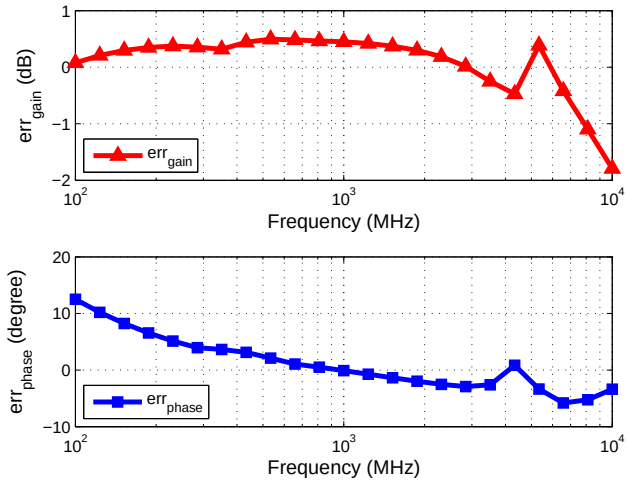


Fig. 45. Gain error (dB) and Phase error (degree) of the proposed Balun-LNA.

amplitude and a frequency spacing of 10MHz. The simulated IIP_3 shows the maximum of -0.45dBm with two tones at 0.7GHz and 0.8GHz. IIP_3 shows the degradation when frequency of two tone test signal increases. The degradation in its linearity is due to the lack of perfect linearity cancellation as frequency increases since gain and phase im-balance in CG (non-inverting) and CS (inverting) stage increases. The frequency spacing between two tones are varied from 4MHz to 20MHz and shows very little variation as shown in Fig. 43.

Fig. 44 shows the phase im-balance between non-inverting and inverting stage with and without the compensation network. It clearly shows that the compensation circuitry equalizes the phase imbalance at high frequency. Less than 0.5dB of gain imbalance and 3 degree of phase-imbalance is satisfied within the balun-LNA's bandwidth as shown in Fig. 45.

The simulated performance of the dual negative-feedback LNA is summarized in Table VI. Recently published works in balun-LNAs are compared with the proposed architecture.

E. Conclusions

This chapter presents a new Balun-LNA architecture, and provides a detailed analysis on its performance; gain, NF, bandwidth, and differential symmetry (balance). Inherent gain of CS (inverting) stage is utilized to reduce the power consumption and improve performance with noise and linearity cancellation property of CG-CS balun topology preserved. Current-mirror based biasing scheme is used to ensure stable operation under PVT variations. The noise contribution due to active current source is suppressed with less voltage headroom when the proposed feedback scheme is employed. Two gain and phase compensation schemes are introduced in Section

Table VI. Comparison of Balun-LNA to recently published works.

	Technology	Frequency [GHz]	Gain [dB]	NF [dB]	IIP_3 [dBm]	Power [mW]	Supply [V]	Architecture	Area $[mm^2]$
[24]	$0.18\mu m$ CMOS	0.8-2.1	14.5	2.6***	16	17.4	1.5	single	0.099
[27]	$0.18\mu m$ CMOS	0.3-0.92*	21**	2 2.8***	-3.2	3.6	1.8	differential	0.33
[31]	$0.25\mu m$ CMOS	0.2-1.6*	13.7**	2.4	0	35	2.5	single	$0.075^{\dagger}$
[39]	$0.13\mu m$ CMOS	1.0-7.0	17**	2.7***	-4.1	25	1.4	differential	$0.019^{\dagger}$
[42]	$0.18\mu m$ CMOS	2.3-9.2*	9.3	4 5.2***	-6.7	9	1.8	single	$0.66^{\dagger}$
[43]	$65nm$ CMOS	0.2-5.2*	15.6**	< 3.5	> 0	21	1.2	balun$^{\diamond}$	$0.01^{\dagger}$
[54]	$0.13\mu m$ CMOS	0.2-3.8	19**	2.8	-4.2	5.7	1	balun$^{\diamond}$	$0.025^{\dagger}$
[61]	$0.13\mu m$ CMOS	0.1-6.5*	19**	3	1	12	1.8	balun$^{\diamond}$	Not reported
[62]	$90nm$ CMOS	0.8-6*	20**	3.5	-3.5	12.5	2.5	balun$^{\diamond}$	Not reported
This Work	**0.13μm CMOS**	**0.5-4.0***	**17.4****	**3.56**	**-0.45**	**2.6**	**1.2**	**balun$^{\diamond}$**	**$0.075^{\dagger}$**

*Minimum of 3-dB bandwidth and S_{11} <-10dB
**Voltage gain
***Average NF
†Active area size
$^{\diamond}$Single-to-differential conversion

C.3 and latter scheme is utilized due to nearly equal loading to Balun-LNA. Theoretically, former scheme equalizes CG and CS stage without hurting other performance but required passive device can be either capacitive or inductive depending on the loading due to the next-stage (e.g., mixer or off-chip SAW filter)

Simulation results of the proposed balun-LNA realized in 0.13μm CMOS demonstrate 17.4dB maximum voltage gain, 3.56dB minimum NF, better than -10dB input matching and -0.45dBm IIP3, while dissipating only 2.6mA from 1.2V supply. A comparison of measurement results with the recently published wideband LNAs shows that the proposed balun-LNA with negative feedback achieves lower power, wider bandwidth, better gain and phase symmetry without using any inductors on-chip.

CHAPTER V

LOW-POWER, LOW-COST CMOS DIRECT CONVERSION RECEIVER FRONT-END FOR MULTI-STANDARD APPLICATIONS

The strong demand for multi-standard receiver encouraged research centers and companies to find architectural solutions to maximize the SOC integration and reduce bill of materil (BOM). Direct conversion receivers are widely adopted in state-of-the-art wireless communication systems for their high level of integration and reconfigurability in the baseband. Its critical drawbacks such as 1/f noise, DC-offset, and high requirement for matching are still challenging and should be tackled at both the system level as well as circuit level.

Compatibility with the digital part of transceiver mandates the use of advanced (scaled down) CMOS process. However, CMOS introduces more flicker noise (1/f noise) than other processes and the only way to mitigate the low-frequency noise from device perspective is to increase the device size, which is contradictory to the necessity of scaled CMOS process in modern transceiver design. The most promising way to alleviate the 1/f noise is to have zero DC current in the switching core [63, 64]. Although, it is shown that non-zero time-varying current void of DC current can still generate the flicker noise [65], the passive mixer shows order of magnitude lower flicker noise compared to gilbert cell mixer, where mixer dissipates DC currrent.

The receiver architecture based on a single low-noise trans-conductor (LNTA) driving a current-mode passive mixer loaded by low-impedance has been widely adopted recently due to its beneficial feature in terms of noise and linearity [53, 64, 66–68]. The architecture shows a drastic reduction in its flicker noise due to current-mode passive mixer void of static DC current. Further optimization can be done on TIA after down-conversion by increasing its device size for flicker noise reduction

and burning more current for thermal noise reduction. Regarding linearity, distortion associated with a large voltage swing present in gilbert cell mixer and voltage-mode passive mixer is minimized thanks to the TIA's virtual ground. Out-of-band interference performance is improved by avoding voltage swing before the signal experiences first-order low-pass filtering via I-V conversion on TIA.

However, the design of broadband receiver based on the architecture is challenging in several aspects. Since there is a single V-I conversion before reaching the mixer, LNTA's trans-conductance should be large enough to guarantee low noise-figure (NF) of the system. Inductor degenerated LNTA can be adopted in narrowband implementation [66, 68, 69], where large trans-conductance (>40mS) with 50Ω input impedance synthesis is allowed. Broadband LNTA (e.g., shunt-feedback LNTA and CG-LNTA) has a fixed relation between input impedance, trans-conductance, and the load impedance and, thus, trans-conductance of LNTA is limited by input matching condition. Low mixer input impedance creates another difficulty because feedback based amplifiers rely on large loop gain that LNTA can not provide. Noise amplification due to TIA [65] can be significant in broadband design, whereas LC tank for LNTA is utilized for narrowband design to mitigate the switch capacitor effects [66, 68, 70]. Frequency-dependent input impedance of TIA deserves a careful attention as well in wideband systems. At high frequency, the feedback gain drops with the increase in virtual ground impedance. The conventional solution is to add a shunted capacitor at virtual ground to mitigate the impedance rises at high baseband frequency [68, 70]. However, this solution drastically limits the open-loop OTA high frequency gain, and incurs noise peaking of TIA and non-ideal filtering for out-of-band interfernece [64].

In this chapter, we present an broadband low-power, low-cost receiver front-end with a dual feedback CG-LNTA driving a current-mode passive mixer loaded by a

virtual ground of wideband feed-forward compensated TIA. CG-LNTA utilizes capacitor cross-coupling and positive feedback from the cascode node of the amplifier such that LNTA can break the trade-off between input impedance, trans-conductance, and LNTA load impedance. A topology for the quadrature sampling mixer [2] is employed to realize 25% duty-cycle with 50% quadrature LO. Quadrature mixing scheme significantly saves power consumption related to LO and improves noise performance with the proposed receiver architecture. For TIA implementation, a feed-forward compensated operational trans-conductance amplifier (OTA) realizes wideband low input impedance compared to miller compensated OTA with pole separation. TIA filtering is realized employing conventional technique. This chapter is organized as follows. The system description is discussed in Section A. Section B describes the chip design details for CG-LNTA, Quadrature sampled mixer, feed-forward OTA, and frequency divider, followed by simulation results in Section C. The concluding remarks are given in Section D.

A. System Description

1. Receiver Architecture

The receiver block diagram is depicted in Fig. 46. The front-end employs a direct conversion architecture for its lower cost and power with a reconfigurability in the baseband. The receiver front-end comprises a low-noise trans-conductance amplifier (LNTA), two separate passive mixers for in-phase (I) and quarature-phase (Q) and a trans-impedance single-pole filter. A local oscillator (LO) generation consists of a divide-by-two circuit to generate 50% duty-cycle LO from the external $2f_{LO}$ source and chains of self-biased CMOS inverters to provide rail-to-rail swing to the passive mixer. Since the output of LNTA is current (trans-conductance), 50% duty-cycle

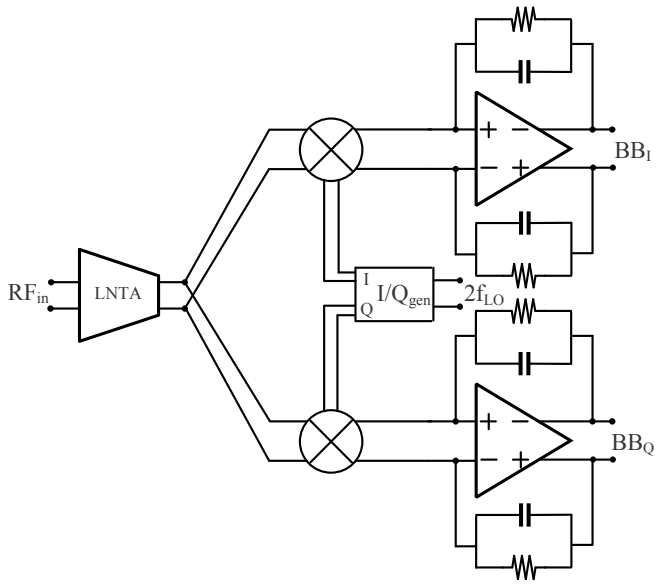


Fig. 46. Receier architecture: LNTA, passive mixer, trans-impedance single-pole filter with I/Q generator (divide by 2 and mixer buffer).

LO with a relative delay of 1/4 period gives 6dB (1/2) of gain loss and significant NF increase due to the overlap between LO I and LO Q pulses. 25% duty-cycle LO scheme [53] provides isolation between I- and Q- current-path in time and, therefore, conversion gain loss and subsequent NF increase is prevented. However, the power dissipation to generate required 25% duty-cycle LO might be prohibitively large. AND operation to provide 25% duty-cycle can be done within the mixer swithes instead of LO [2]. In this work, a topology for the quadrature sampling is utilized to implement non-overlapping switching mixer between I and Q path with 50% duty-cycle LO. The increase in on-resistance due to quadrature sampling does not impact the receiver performance significantly by employing LNTA load impedance boosting and wideband low input impedance TIA in the proposed architecture. Size of the mixer switches can be increased as well with the penalty in bandwidth (frequency response) of the passive mixer. All the RF and LO paths are differential (balanced) in order to enhance sensitivity to power supply and substrate noise. By using current-

mode passive mixer and careful design of baseband OTA used for TIA, the flicker noise issue of the proposed architecture is significantly reduced.

The proposed receiver architecture improves the linearity and maximize dynamic range by avoiding large voltage swings before the first-order low pass filtering on TIA. Low input impedance presented by the virtual ground of TIA reduces the distortion related to the passive mixer [71]. The selectivity from the low pass filtering on TIA also helps mitigating the impact of out-of-band interferences (OBI). Tolerance to OBI is more important for broadband receiver in contrast to narrowband receiver with RF band-selection [67].

The most critical aspects of the receiver front-end is its sensitivity (NF) performance. To ensure low NF of the receiver, large amplification with low-noise performance early in the chain is mandatory [72]. Thus, a single trans-conductor of the proposed receiver front-end should be large and this requirement has been met in previous works [66,68,69] with inductor-degenerated LNAs. Effective trans-conductance (G_m) of the inductor-degenerated LNAs can be expressed as below and, therefore, is independent of its input impedance.

$$G_m = Q_{in} \cdot g_m = \frac{\omega_T}{2 \cdot \omega_o \cdot R_S}, \tag{5.1}$$

where R_S is the source impedance, ω_o and ω_T are operating and unity current gain frequencies, respectively. However, broadband LNAs (e.g., shunt-feedback and common-gate LNTA) present a fixed relationship between input impedance, trans-conductance, and the load impedance. Shunt-feedback LNTA is discarded in this application for the following reasons. Firstly, due to the trade-off between input impedance, trans-conductance, and the load impedance, it is difficult to achieve good NF and required input impedance with reasonable current consumption. The work in [73] shows excellent broadband performance but consumes excessive power of 42mW. Secondly,

shunt-feedback LNTA requires large loop gain but, due to the low input impedance passive mixer and virtual ground of TIA, loop gain of LNTA is drastically reduced when cascaded with the mixer.

CG-LNTA features desirable properties for broadband operation [44]. However, their high NF under input matching condition prevents its extensive use. Its effective transconductance under input matching condition is

$$G_m = \frac{1}{2} g_m = \frac{1}{2R_S}. \tag{5.2}$$

In 50Ω R_S system, this requirement dictates that $G_{m,CG-LNTA}$ is only 10mS and CG-LNTA is not feasible for the proposed architecture where larger trans-conductance is needed to ensure good system NF performance. With the scaling of CMOS devices and high f_t transistors available, it becomes more promising to employ feedback in the design of broadband CG-LNTA. In the proposed architecture, dual feedback, shunt-series negative feedback [25] and shunt-shunt positive feedback [18], are utilized in order to decouple the trade-off between critical design parameters and to enable high effective trans-conductance (>20mS). Woo *et al.* [27] reported similar architecture with LNA only but it is not applicable to LNTA for the proposed system.

The proposed architecture features efficient current transfer between LNTA and passive mixer, and improved linearity (in-band and out-of-band) by employing LNTA load impedance boosting and a wideband low input impedance OTA with feed-forward compensation. With the limited power supply of 1.2V, a shunt-peaking inductor is used to boost the load impedance at the receiver bandwidth. The optimum inductor size is derived analytically in Section B.1. Low input impedance of TIA over a wideband is ensured by employing feed-forward compensation technique, where the dominant pole does not have to be placed at low frequency as in miller-compensated OTA. Large swing due to OBI is sigficantly reduced, resulting in better large-signal

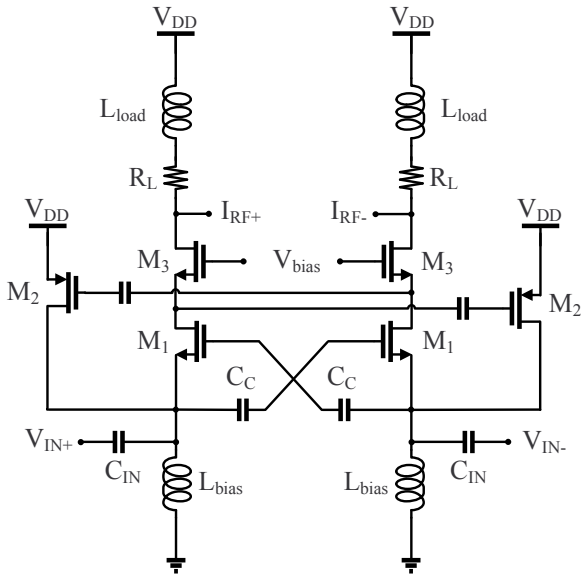


Fig. 47. Schematic of dual feedback CG-LNTA (LNTA block in Fig. 46).

linearity (e.g., P_{1dB}) performance.

2. Receiver Performance

Fig. 47 shows RF trans-conductor used for the receiver performance analysis. RF trans-conductor is based on dual feedback LNTA and is cascaded with the quadrature sampling mixer switches. The current transfer from LNTA to quadrature sampling switch is enhanced through a load boosting inductor. Frequency translated signal after switching flows into a single-pole RC low-pass network. The conversion gain of the proposed architecture can be expressed as

$$\frac{V_{out}\left(f_{out}\right)}{V_{in}\left(f_{in}\right)} \approx \frac{\sqrt{2}}{\pi} \cdot \left| \frac{Z_{in}}{Z_{in}+R_S} \right| \cdot g_{mn} \cdot \left(1+A_n\right) \cdot \left|Z_F\right|, \tag{5.3}$$

where f_{out} is the output frequency after down-conversion, f_{in} is the input RF frequency, A_n is the negative feedback factor (≈ 1), and $\sqrt{2}/\pi$ (=c) is the conversion gain of 25% switching alone. Z_{in} is the input impedance of LNTA as shown in (5.18)

and Z_F is expressed as

$$Z_F = \left(\frac{R_F}{1 + j2\pi f_{out} R_F C_F} \right), \tag{5.4}$$

The dominant noise sources in the proposed architecture are M_1 (g_{mn}), M_2 (g_{mp}), R_L, R_F, and V_{amp}. Noise from the switches are neglected because of low average on-resistance and small DC current [74]. Noise at the output of TIA from dominant noise sources can then be obtained as

$$V_{R_S}^2 = n \times 4kTR_S \left(\frac{g_{mn}(1 + A_n)}{H} \right)^2 c^2 |Z_F|^2 \tag{5.5}$$

$$V_{M_1}^2 = n \times 4kT \frac{\gamma}{\alpha} g_{mn} \left(\frac{1}{H} \right)^2 c^2 |Z_F|^2 \tag{5.6}$$

$$V_{M_2}^2 = n \times 4kT \frac{\gamma}{\alpha} g_{mp} \left(\frac{g_{mn}(1 + A_n) R_S}{H} \right)^2 c^2 |Z_F|^2 \tag{5.7}$$

$$V_{R_L}^2 = n \times 4kTR_L \left(\frac{1}{R_L + j2\pi f_{in} L} \right)^2 c^2 |Z_F|^2 \tag{5.8}$$

$$V_{R_f}^2 = 4kTR_F \left| \frac{1}{1 + j2\pi f_{out} R_F C_F} \right|^2 \tag{5.9}$$

$$V_{amp}^2 = v_{n,amp}^2 \left| 1 + \frac{2Z_F}{Z_{LNTA}} \right|^2 \tag{5.10}$$

where γ and α are bias-dependent parameters [28]. n (noise aliasing factor) and H are expressed as

$$n = 2 \left(1 + \frac{1}{3^2} + \frac{1}{5^2} + \cdots \right) = \frac{\pi^2}{4} \tag{5.11}$$

$$H = 1 + g_{mn}(1 + A_n)(1 - A_p) R_S. \tag{5.12}$$

Thus, the single-sideband (SSB) NF is approximately

$$NF_{SSB} = \frac{V_{R_S}^2 + 2\left(V_{M_1}^2 + V_{M_2}^2 + V_{R_L}^2 + V_{R_f}^2\right) + V_{amp}^2}{4kTR_S\left(\frac{V_{out}(f_{out})}{V_{in}(f_{in})}\right)^2} \tag{5.13}$$

$$= n + F_{M_1} + F_{M_2} + F_{M_L} + F_{R_f} + F_{TIA} \tag{5.14}$$

$$\approx n + 2n\frac{\gamma}{\alpha}\frac{1-A_p}{1+A_n} + 2n\frac{\gamma}{\alpha}g_{mp}R_S + n\frac{8R_S}{R_L}(1-A_p)^2\left|\frac{R_L}{R_L + j2\pi f_{in}L}\right|^2 + \frac{8R_S}{R_F}(1-A_p)^2\frac{1}{c^2} + \frac{4R_S}{kT}v_{n,amp}^2(1-A_p)^2\frac{1}{c^2\left|Z_{LNTA}\right|^2} \tag{5.15}$$

The factor of 2 for the numerator in (5.13) is due to the double balanced mixer operation and $Z_F \gg Z_{LNTA}$ is used for the approximation in (5.15). TIA noise amplification due to the switched capacitor (SC) effects is more pronounced as input RF frequency goes up. The value of this SC impedance with L_{LNTA} neglected is expressed as

$$R_{LNTA} = \frac{1}{4f_{LO}C_{par}} \tag{5.16}$$

where the factor of 4 arises from parallel connection of SC resitor in quadrature (I/Q) mixer. This effect can be nullified in narrowband receiver by employing LC tank load for LNTA [66, 68, 69], whereas broadband receiver's NF degrades due to TIA noise amplication effect.

The receiver NF improves as a result of both negative feedback (A_n) and positive feedback (A_p). A_p has more impact on NF than A_n because positive feedback improves LNTA signal-to-noise ratio (SNR) as well as effective trans-conductance of the system. The conventional CG-LNTA and the negative feedback (A_n) does not enhance the current gain and, thus, effective transconductance remains equal to $\frac{1}{2R_S}$ while satisfying matching condition, whereas the effective trans-conductance with the

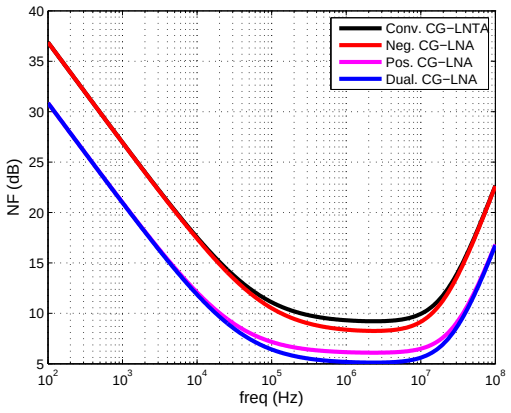


Fig. 48. Receiver NF performance with different broadband CG-LNTAs.

positive feedback (A_p) is proportional to g_{mn}. The benefits of the positive feedback (A_p) becomes evident from (5.15) that noise contribution due to M_1, R_L, R_F, and V_{amp} are drastically suppressed when the positive feedback (A_p) approaches unity. Fig. 48 shows the double side-band (DSB) NF performance when different types of CG-LNTAs are used and supports the previous analysis. $A_p = 0.5$ is used for positive feedback gain but the conclusions can be extrapolated to any other A_p. Flicker noise corner frequency of OTA at 200KHz and single-pole RC filter at 1.92MHZ (UMTS signal bandwidth) is used to capture these effects at system NF performance. Fig. 49 shows the receiver NF and power consumption (current used for LNTA) as a function of the positive feedback factor (A_p). High A_p improves NF by enhancing SNR of LNTA and RF trans-conductance (G_m) at the expense of power consumption and potential in-stability. When generating these results, v_{dsat} of 0.2V is assumed for LNTA. Hence, its power consumption can be expressed as the following according to classical square-law MOS model.

$$I_{LNTA} = \frac{1}{2}\left(g_{mn} + g_{mp}\right) v_{dsat} \tag{5.17}$$

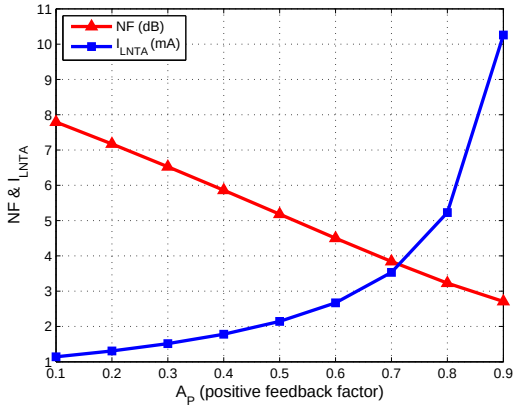


Fig. 49. NF and power consumption (I_{LNTA}) with different positive gain factor (A_p) with $v_{dsat} = 0.2V$.

B. Building Block Designs

1. Low-Noise Trans-Conductance Amplifier

The RF trans-conductor (LNTA) of the proposed receiver is shown in Fig. 47. Impedance matching device M_1 provides the main forward signal path. g_m boosting is implemented with noiseless capacitor cross-coupling [25] with almost unity negative feedback gain ($A_n = \frac{C_C - C_{gs}}{C_C + C_{gs}}$). Shunt-shunt positive feedback through M_2 enables the current gain larger than 1 and increases the input impedance of conventional CG-LNTA. The previous works utilized positive feedback [18, 27] that senses the signal at the output of the amplifier. However, in the proposed architecture, RF trans-conductor drives low impedance mixer terminated by virtual ground and, therefore, positive feedback loop gain from the output can not be employed. Instead, the signal is sensed at the cascode node, leading to loop gain ratio of two trans-conductance ($A_p = \frac{g_{mp}}{g_{m,cas}}$). Possible increase of the parasitic capacitance at the input is nulled by bias inductor (L_{bias}).

The in-band LNA input impedance can be found as

$$Z_{in} \approx \frac{1}{g_{mn}\left(1+A_n\right)\left(1-A_p\right)} \parallel sL_{bias} \parallel \frac{1}{sC_{par}} \tag{5.18}$$

where parasitic capacitor C_{par} arises from the contributions of the input pad, M_1, M_2, and C_C. The input matching network is a parallel resonance where the quality factor of the parallel LC resonator is

$$Q_{match} = \frac{\omega C_{par} R_S}{2}. \tag{5.19}$$

Low Q_{match} results in a wider bandwidth since the sensitivity of Z_{in} to parasitic components is proportional to the quality factor of the matching network [30].

Shunt-peaking inductor is used at LNTA output to enhance the current transfer into the mixer and to minimize the noise contribution due to the OTA. Fig. 50 (a) shows the equivalent circuit diagram for broadband current-trasfer optimization. R_{in} is the mixer input impedance when the switch is on and can be expressed as

$$R_{in} = 2R_{switch} + \frac{R_F}{1+A_{OTA}}. \tag{5.20}$$

where the factor of 2 comes from quadrature sampling mixer and A_{OTA} is the open-loop gain of the OTA. The current transfer into the mixer can be obtained as

$$\begin{aligned} \frac{I_{Gm}}{I_{LNTA}} &= -\frac{R_L}{R_L+R_{in}} \frac{1+s\frac{L}{R_L}}{1+s\left(\frac{L}{R_L+R_{in}}+\frac{R_{in}R_LC_P}{R_L+R_{in}}\right)+s^2\frac{R_{in}C_PL}{R_L+R_{in}}} \\ &= -\frac{\rho\left(1+s\tau_1\right)}{1+s\rho\left(\tau_1+\tau_2\right)+s^2\rho\tau_1\tau_2} \end{aligned} \tag{5.21}$$

where ρ $(= \frac{R_L}{R_L+R_{in}})$ is low frequency current-transfer gain. τ_1 $(= \frac{L}{R_L})$ and τ_2 $(= R_{in}C_P)$ are time constants present in the equivalent circuit. To facilitate subsequent derivations, we introduce a factor m $(= \frac{\tau_1}{\tau_2})$, defined as the ratio of two time constants. The damping factor (ζ) and the undamped natural frequency (ω_n) of the current

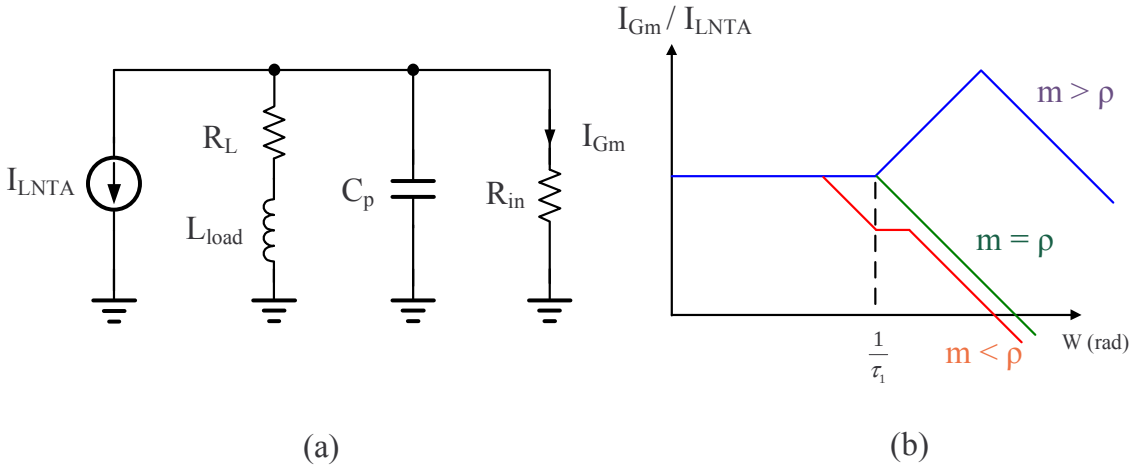


Fig. 50. (a) Equivalent circuit diagram for current-transfer optimization and (b) Transfer function vs. relative location of two poles.

transfer function can be derived as

$$\zeta = \frac{1}{2}\sqrt{\rho}\left(\sqrt{\frac{\tau_1}{\tau_2}}+\sqrt{\frac{\tau_2}{\tau_1}}\right) \geq \sqrt{\rho} \tag{5.22}$$

$$\omega_n = \frac{1}{\sqrt{\rho\tau_1\tau_2}} \tag{5.23}$$

Depending on the relative location of two poles, the trans-conductance follows the trends shown in Fig. 50(b). Notice that $1/\tau_1$ does not correspond to the bandwidth of current transfer function without shunt-peaking inductor, which is given by $1/\left(R_{in} \parallel R_L\right) C_P$.

2. Switches

Fig. 51 (a) shows the 25% duty-cycle mixer switches, which is drawn with single-ended RF input only not to clutter the schematic. It is fundamentally the double balanced topology with the benefit of rejecting LO feedthrough and noise due to LO circuitry. Also, the double balanced structure improves IIP2 performance with less self-mixing [70, 75]. The switching topology in Fig. 51 (a) realizes 25% duty-cycle

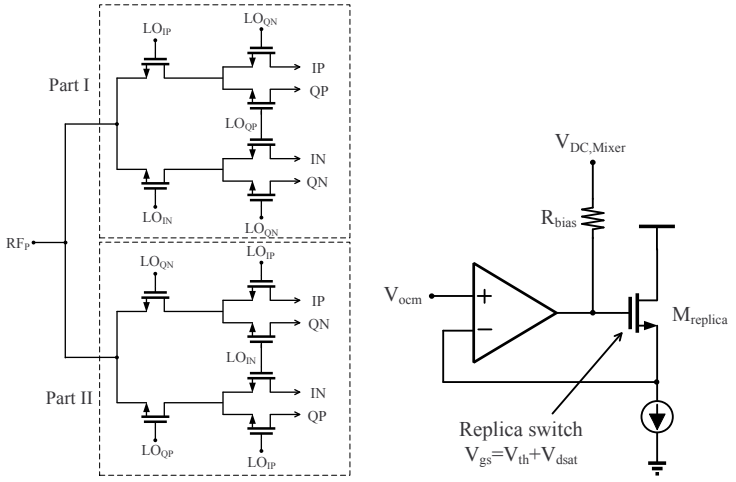


Fig. 51. (a) 25% duty-cycle qudarature sampling mixer (single-ended RF input only) [2] and (b) Replica circuitry for mixer switch DC bias.

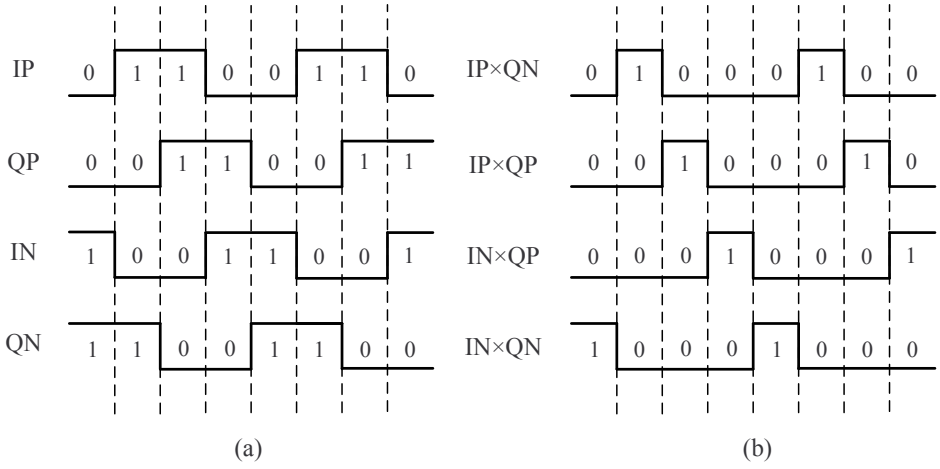


Fig. 52. (a) 50% duty-cycle LO and (b) 25% duty-cycle LO by ANDing of two 50% I-Q LO signals with a relative delay of 1/4 period.

by ANDing two 50% I-Q LO signals with a relative delay of 1/4 period. Timing diagram illustrating AND operation of the quadrature switching topology is also shown in Fig. 52. Switching part I and II together achieves the equal loading from 50% I-Q LO, whereas each of them introduces I-Q mismatch since in-phase LO drives one switch and quarature-phase LO drives two switches in switching part I and vice versa in switching part II. Potential residual side-band (RSB) performance reduction is prevented by the scheme. Previous works in [53, 76] implement 25% duty-cycle switching with either 50% duty-cycle $2f_{LO}$ or 25% duty-cycle f_{LO}, both of which consumes significant power for LO buffers.

Depending on the DC gate bias of the switches, passive mixer can operate in either ON or OFF overlap. ON overlap results in lowered conversion gain and, more importantly, noise amplification due to OTA becomes significant. It is evident from (5.10) that ON overlap of the switches results in a significant gain of OTA input referred noise voltage (V_{amp}^2) due to very small on-resistance of the switches. On the other hand, OFF overlap results in linearity degradation [74, 77]. Fig. 51 (b) shows the replica circuitry to bias the gate of passive mixer switches. The replica transistor ($M_{replica}$) is biased at weak inversion where its V_{gs} is near threshold voltage (V_{th}) and tracks with process variation. V_{ocm} represents the common-mode voltage used for common-mode feedback (CMFB) circuitry of op-amp, which set the DC bias voltage at the source (drain) of the passive mixer switches. The replica circuitry provides DC gate bias for the switches at the threshold of conduction for the switches ($V_g \approx V_{ocm} + V_{th}$). The receiver simulation results show that the optimum NF with respect to DC gate bias is several tens of mV smaller than the replica bias circuit provides but the difference is very minimal.

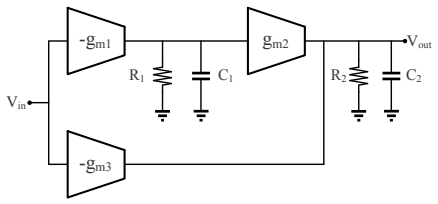
3. Baseband Trans-Impedance Amplifier

The trans-impedance amplifier (TIA) converts the base-band current into the voltage with very small input impedance that allows the current-mode passive mixer to be functional. To accomodate high-power blockers, single pole RC filtering is typically employed where the bandwidth is determined by the location of the pole. The main limitation on the TIA design is to achieve high gain and wide-bandwidth without burning significant power. The conventional solutions [74, 78] employ two-stage OTA with miller compensation and nulling resistor. This approach requires significant power consumption to achieve good stability and large gain-bandwidth-product (GBW) at the same time. Furthermore, the pole splitting inherent in miller compensation [36, 79] reduces the amplifier dominant pole significantly. As a result, the input impedance of the TIA shows inductive behavior after the dominant pole of the amplifier. Previous works [68, 70, 80] added an extra capacitance at the virtual ground node to suppress the inductive input impedance but the frequency dependent transconductance of the previous stage degrades and the effects on noise and gain are detrimental especially for wide-band communication systems.

In the proposed receiver front-end, feed-forward two-stage OTA [81] is employed to achieve the wide-band low input impedance and ideal single-pole response in its trans-impedance gain. The block diagram of the feed-forward compensation for two-stage OTA and the design parameters are shown in Fig. 53. The feed-forward path due to g_{m3} introduces a LHP zeros and compensates for the negative phase shifts due to the poles. The amplifier transfer function based on Fig. 53 (a) is derived as

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{(A_{v1}A_{v2} + A_{v3})\left(1 + \frac{A_{v3}s}{(A_{v1}A_{v2}+A_{v3})\omega_{p1}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}. \tag{5.24}$$

The location of LHP zero is approximately k times the gain-bandwidth product of



(a)

$A_{v1} = g_{m1}R_1$	$\omega_{p1} = 1/R_1C_1$
$A_{v2} = g_{m2}R_2$	$\omega_{p2} = 1/R_2C_2$
$A_{v3} = g_{m3}R_2$	$\omega_{p3} = \omega_{p2}$

(b)

Fig. 53. (a) The block diagram of feed-forward compensation scheme for two-stage amplifier and (b) Design parameters.

the first stage [81], where k is the ratio of two trans-conductance ($\frac{g_{m2}}{g_{m3}}$). Miller compensation realizes stability at the expense of reduced dominant pole location and, therefore, the inductive behavior of TIA input impedance kicks in at rather lower frequency. Out-of-band peaking in the trans-impedance transfer function moves to a lower frequency as well and hurts ideal sing-pole RC filtering. Broadband receiver front-end without any pre RF-filtering is susceptible to OBI interference and wideband low-impedance before RC low-pass filter is indispensable to maintain the superior linearity of the proposed architecture.

TIA input-impedance and its transfer function can be derived from Fig. 54. The equivalent circuit model includes RC feedback components. After some simplifications, TIA input impedance can be obtained as

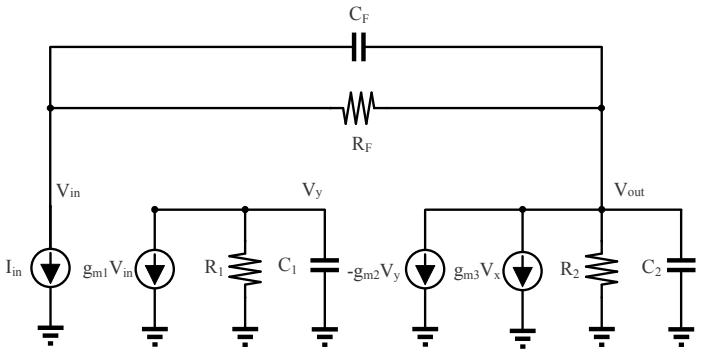


Fig. 54. Equivalent circuit model of TIA with feed-forward compensation.

$$\begin{aligned} \frac{v_{in}}{i_{in}} &= Z_{in}(s) \\ &\approx \frac{R_F + R_2}{1 + A_v}\left(1 + sR_1C_1\right)\frac{A(s)}{D(s)}, \end{aligned} \tag{5.25}$$

where A_v ($\approx g_{m1}R_1g_{m2}R_2$) is the DC open-loop gain of the OTA, and $A(s)$ and $B(s)$ are

$$A(s) = \frac{1 + s(R_2 \| R_F)(C_2 + C_F)}{1 + sR_FC_F} \tag{5.26}$$

$$D(s) = 1 + s\frac{g_{m3}}{g_{m1}g_{m2}}C_1 + s^2\frac{C_1C_2}{g_{m1}g_{m2}} \tag{5.27}$$

$A(s)$ represents pole-zero pair located around the single-pole RC filtering bandwidth (3-dB) and does not incur inductive impedance behavior of TIA. The increase in TIA input impedance is due to the OTA dominant pole at $\frac{1}{R_1C_1}$ in contrast to $\frac{1}{R_1C_m(1+g_{m2}R_2)}$ for miller-compensated OTA with C_m being miller capacitor. The damping factor (ζ) and the undamped natural frequency (ω_n) of $D(s)$ can be derived as

$$\zeta = \frac{1}{2}\kappa\frac{g_{m3}}{g_{m2}} \tag{5.28}$$

$$\omega_n = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}} = \kappa\frac{g_{m1}}{C_1} \tag{5.29}$$

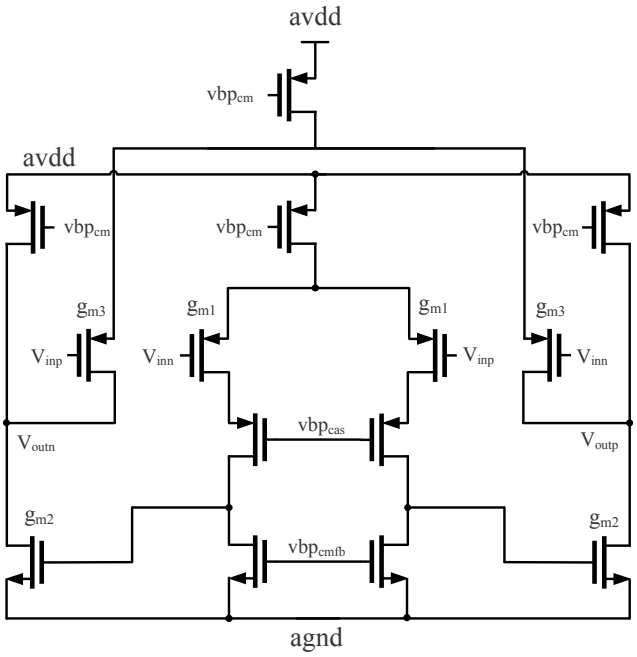


Fig. 55. The schematic of feed-forward compensated OTA (CMFB is not shown).

where $\kappa = \sqrt{\frac{g_{m2}/C_2}{g_{m1}/C_1}}$ is a proportionality constant that relates the gain-bandwidth product of each stage in OTA. The characteristics of TIA input impedance can then be adjusted by properly selecting the parameters of the frequency dependent $D(s)$. Similar conclusions can be drawn for TIA trans-impedance gain expressed below

$$\frac{v_{out}}{i_{in}} \approx -\frac{A_v}{1+A_v}\frac{R_F}{1+sR_FC_F}\frac{G(s)}{D(s)} \tag{5.30}$$

where $D(s)$ is given in (5.27) and $G(s)$ is expressed as

$$G(s) = 1 + s\frac{1}{g_{m1}g_{m2}}\left(g_{m3}C_1 - \frac{C_F}{R_1}\right) - s^2\frac{C_1C_F}{g_{m1}g_{m2}} \tag{5.31}$$

The schematic of the OTA, depicted in Fig. 55, employs a two-stage amplifier with feed-forward compensation. PMOS instead of NMOS inputs are chosen

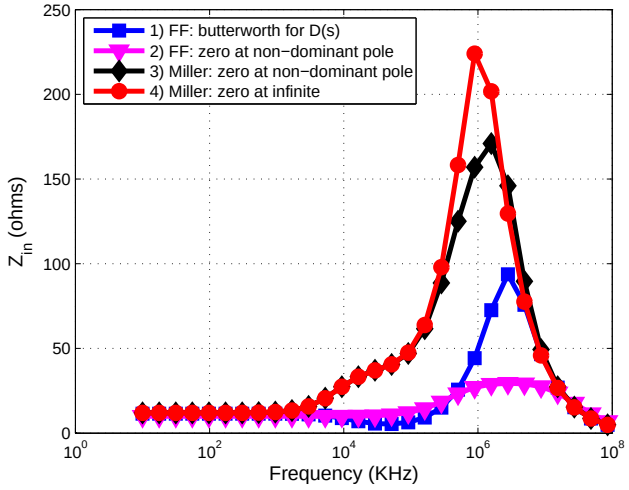


Fig. 56. TIA input impedance (Z_{in}).

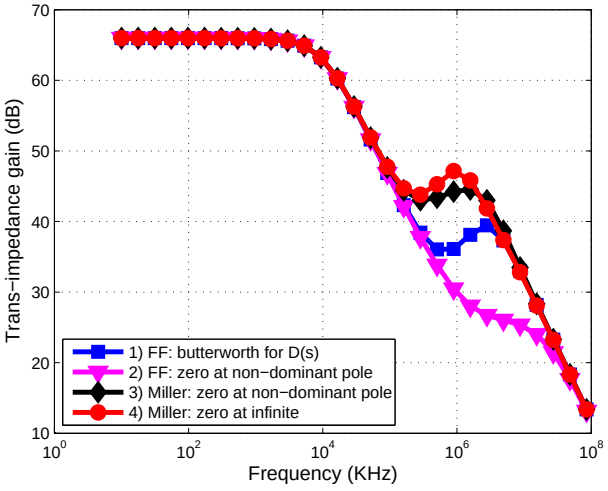


Fig. 57. TIA trans-impedance gain ($\frac{v_{out}(s)}{i_{in}(s)}$).

for reduced flicker noise performance and large input devices biased at moderately high current is employed to reduce the equivalent input noise voltage [78]. The output stage in common-source configuration without cascode transistor achieves large output swing. RC feedback component sizes were chosen based on noise and gain performance of the receiver front-end and available chip-area.

To verify the previous analysis with fair comparison to miller-compensated OTA, the circuit shown in Fig. 55 was designed and simulated in Spectre RF. Feed-forward compensation is added and its parameter (g_{m3}) is chosen based on two design considerations; 1) butterworth response for $D(s)$ and 2) placing the frequency of the LHP zero such that it cancels the non-dominant pole ($\frac{1}{R_2C_2}$). Nulling resistor in miller-compensated OTA was used as a design paramter and the zero ($\omega_z = -\frac{1}{C_m(1/g_{m2}-R_Z)}$) was varied and placed at 3) non-dominant pole ($\omega_{p2} \approx \frac{g_{m2}}{C_1+C_2}$) and 4) infinite frequency (∞). TIA input impedance behavior for both amplifiers is shown in Fig. 56. For the case of the proposed TIA, inductive behavior of input impedance is pushed to higher frequency and roll-off due to $D(s)$ compensates for the effect and enables very low input impedance over a wideband, whereas miller-compensated OTA can not maintain low impedance property of the proposed TIA. Better OBI filtering is also achieved with feed-forward OTA as shown in Fig. 57.

4. Frequency Divider and LO Buffer

LO generation circuitry is shown in Fig. 58. An off-chip $2f_{LO}$ signal is injected through balun. Divide-by-two circuitry produces 50% duty-cycle f_{LO} on-chip. An edge-triggered master/slave flip-flop (DFF) implemented using current-mode logic (CML) style implements the divide-by-two circuitry. The required operating frequency is between 4GHz and 12GHz, twice the frequency of internal LO frequency. Frequency-divider is directly connected to the pin without any input buffer to min-

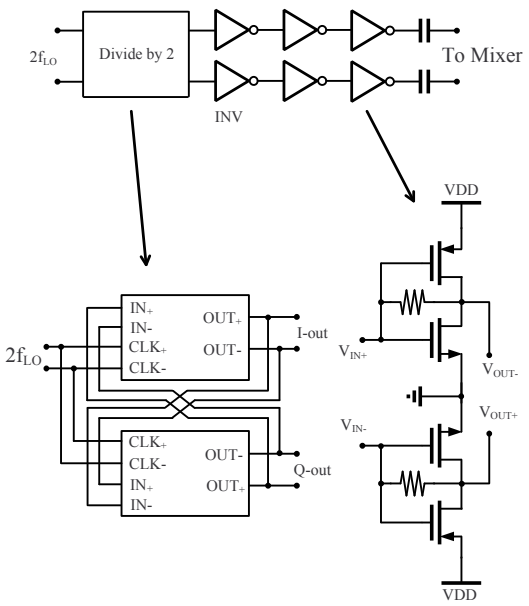


Fig. 58. LO generation circuitry (divider by two and chains of CMOS inverters).

imize the dynamic power of LO chain. Required clock swing for proper generation of f_{LO} on-chip is getting smaller until self-oscillating frequency of divider based on CML latch, which obviates the need for input-buffer [82]. Chains of self-biased CMOS inverters provide rail-to-rail signals that improves passive mixer NF and IIP_2 performance [63, 75]. CML type inverters may provide faster operating frequency than CMOS inverters. However, it is not adopted since required power consumption is excessively large with much less voltage swing.

C. Measurement Results

The circuit was designed in TSMC 0.13μm CMOS technology and extracted with calibre. Fig. 59 shows the die photograph of the prototype receiver. The active area of the chip is $1.1mm \times 1mm$, and CG LNTA occupies $0.45mm \times 0.9mm$ due to differential inductors used for input match and load boosting.

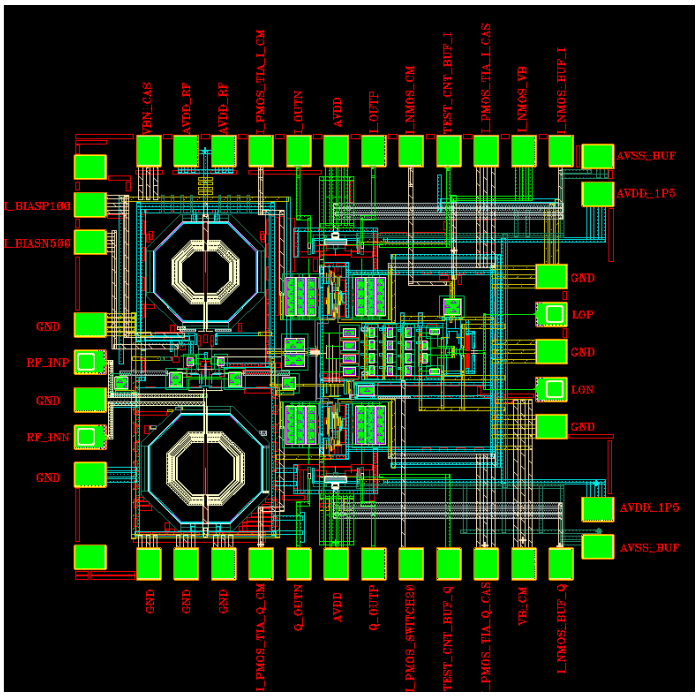


Fig. 59. Die photograph of the balun-LNA.

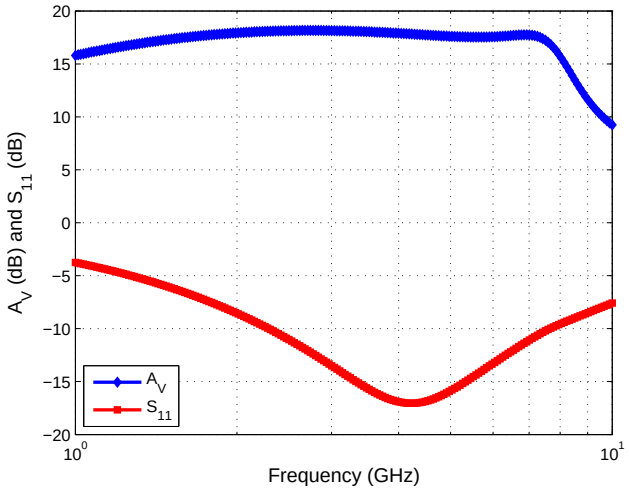


Fig. 60. Simulated $A_{V,LNTA}$ and S_{11} of stand-alone LNTA.

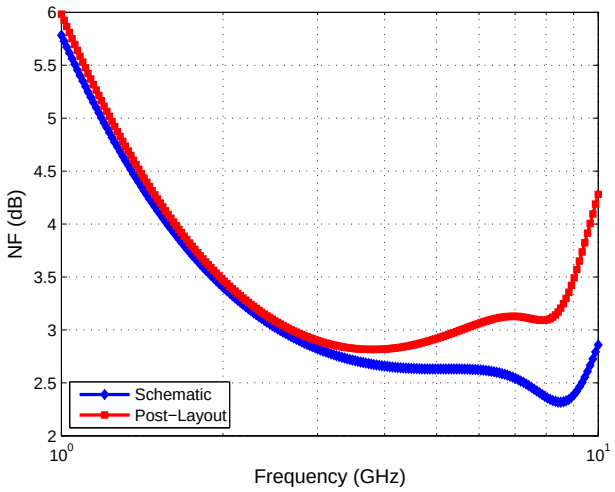


Fig. 61. Simulated NF (dB) of stand-alone LNTA.

Fig. 60 shows simulated impedance matching performance (S_{11}) and voltage gain ($A_{V,LNTA}$) of stand-alone LNTA. The simulated S_{11} is below -10dB between 2.2GHz and 7.7GHz. The maximum $A_{V,LNTA}$ is 18.1dB and remains 1-dB flatness from 1.3GHz to 7.5GHz. The lower and upper 3-dB bandwidth is measured at 0.8GHz and 8.1GHz. Fig. 61 shows the simulated NF of stand-alone LNTA. The NF varies between 2.8dB to 3.1dB between 2GHz and 7GHz in post-layout simuation.

Conversion gain ($A_{V,RX}$) and NF of the proposed receiver are simulated and shown in Fig. 62 and Fig. 63, respectively. The degradation of $A_{V,RX}$ and NF at high frequency is noticeable but is not due to the bandwidth limitation of receiver signal path design. For higher LO frequncies, LO buffer driving the passive mixer switch shows slow rise and fall times as well as insufficient swing. LO swing at the gate of passive mixer switch is shown in Fig. 64, where LO swing rapidly degrades from 5GHz. Note that $A_{V,RX}$ and NF of the proposed receiver degrades where LO pulse amplitude is getting lower, showing close correlation.

Fig. 65 shows simulated 1/f corner sweeping the LO frequency. 1/f noise is

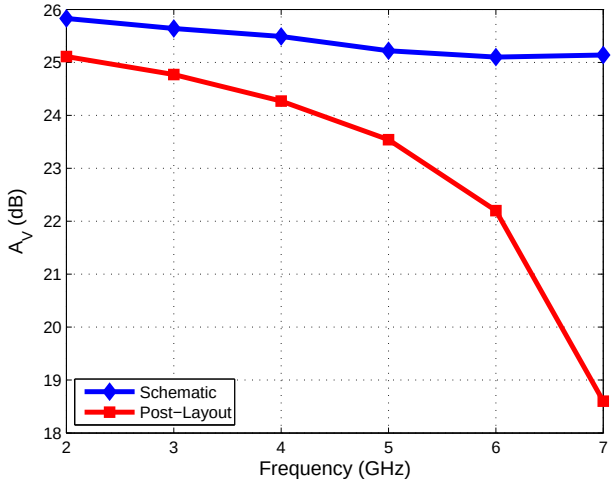


Fig. 62. Simulated $A_{V,RX}$ of the proposed receiver.

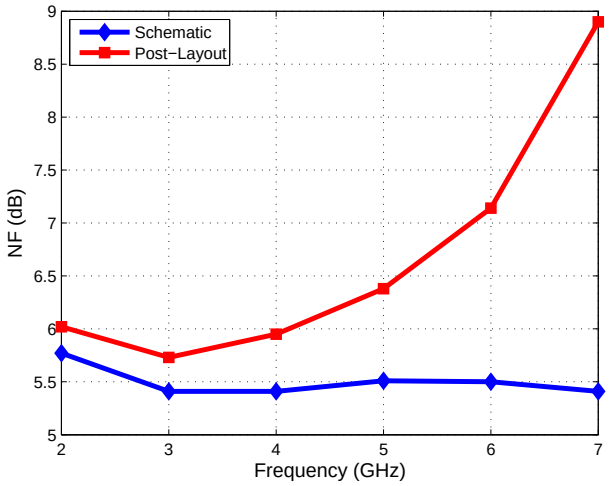


Fig. 63. Simulated NF (dB) of the proposed receiver.

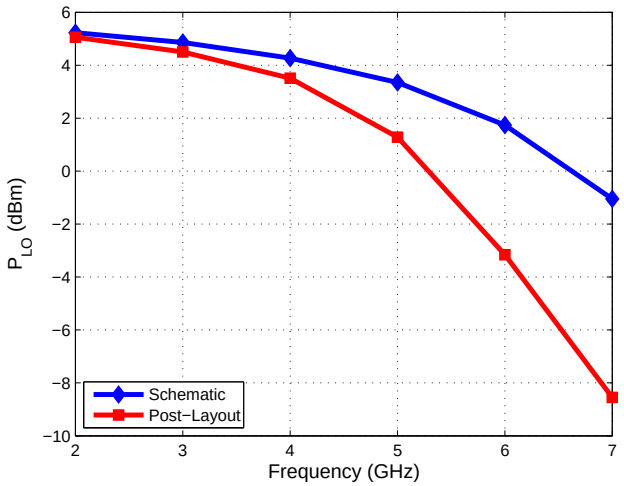


Fig. 64. LO swing (dBm) versus frequency.

mainly determined by OTA because of current-driven passive mixer operation and AC coupling from LNTA to the mixer. The degradation in $A_{V,RX}$ at high LO frequency entails the increase in OTA's noise contribution. Then, 1/f corner also increases with higher LO frequency as shown in Fig. 65.

The simulated performance of the proposed receiver is summarized in Table VII. Recently published works in the same architecture are compared with the prototype receiver.

D. Conclusions

This paper presents a broadband CMOS direct-conversion quadrature receiver architecture fabricated in 0.13-μm CMOS. The prototype receiver demonstrates that a single LNTA driving a current mode passive mixer terminated by a low input impedance TIA can achieve a high and flat gain with low NF over a wide bandwidth. Large voltage swing due to I-V conversion is deferred till the output of TIA and, thus, the receiver shows improved OOB interference and in-band linearity performance. By

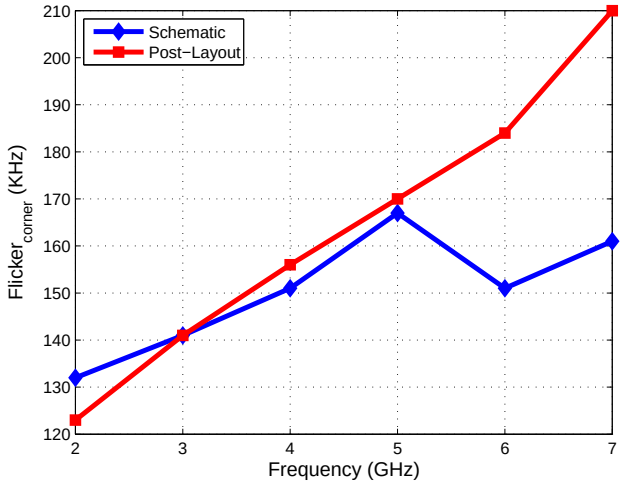


Fig. 65. 1/f corner versus frequency.

Table VII. Comparison of proposed receiver to recently published works.

	Technology	Frequency [GHz]	Gain [dB]	NF [dB]	IIP_3 [dBm]	Power [mW]	Supply [V]
[68]	0.13μm CMOS	5.15-5.825	26	3.5	-2	36* 36**	1.2* 2.5***
[66]	0.18μm CMOS	0.869-0.894	44	2.4	4.65$^{\diamond}$	35.7*	2.1
[64]	0.18μm CMOS	1.55-2.3	22.5-25	7.7-9.5	$\geq$7	10*	2
[83]	90nm CMOS	0.1-3.85	20	8.4-11.5‡	-3.23$^{\diamond\diamond}$	9.8*	1.2
[74]	0.13μm CMOS	0.9-2.3	34.5-35.5	9.5-11.5	4-11	30-36 (total)	1.5
[53]	90nm CMOS	0.5-7$^{\triangleright}$	18	4.5-5.5	-3	16* 4-28**	1.2
[62]	90nm CMOS	0.8-6	3-36 (variable-gain)	5-5.5	-3.5	29*	2.5
This Work	**0.13μm CMOS**	**0.8-6.2**	**25.1**	**5.73**	**0.9**	**13* 35****	**1.2* 1.5****

*RX portion (including baseband)
**LO portion
***Baseband only portion
†Active area size
‡Single side-band NF
$^{\diamond}$Inferred from Triple-Beat (TB) performance, where $TB = 2\,(T_X - IIP_3)$
$^{\diamond\diamond}$Inferred from P_{1dB} performance, where IIP_3=P_{1dB}+9.6dB
$^{\triangleright}$1-dB bandwidth; others use 3-dB bandwidth

ensuring low impedance along the RF signal path, the receiver operates over a wide range of frequencies from 2GHz to 6GHz and the bandwidth limitation comes mainly from in-sufficient LO swing.

The trade-off between input impedance, trans-conductance, and the load impedance of broadband LNTA can be overcome by the proposed CG LNTA with dual feedback. Trans-conductance (G_m) is not limited by source impedance (R_S) and, therefore, improved current gain of LNTA enables large gain and low NF of the receiver in a wideband fashion. Neither 50% duty-cycle $2f_{LO}$ nor 25% duty-cycle f_{LO} is required by overlapping of two 50% I-Q LO signals with a relative delay of 1/4 period. The feed-forward compensation scheme is employed to achieve wideband low input impedance and ideal single-pole filtering of TIA. Measurement results of the proposed receiver demonstrate >22dB conversion gain, <7dB NF, and >0.5dBm IIP_3 from 2GHz to 6GHz. Better than -10-dB input matching is achieved from 2GHz to 7.7GHz, while dissipating 13mW from RF and baseband signal path with 1.2-V supply. A comparison of measurement results with the recently published broadband receiver with a single LNTA shows that the proposed architecture achieves superior noise and linearity performance with low power consumption using a mainstream technology.

CHAPTER VI

CONCLUSION

The SWR receiver is not a reality yet and, as an intermediate step prior to the realization of SWR receiver, a broadband multi-standard receiver is highly desired leading to the significant reduction in its form factor, cost, and power. Due to the ability of highest level of integration, low cost, and low power, the use of advanced (scaled down) CMOS processes is also mandatory along with the compatibility with the digital part of trasceiver. This dissertation is dedicated to the analysis and realization of a broadband receiver architecture and its various building blocks (LNA, Active Balun-LNA, Mixer, and TIA) for multi-standard applications in mainstream CMOS technology. The efforts have been given to both the system level (Chapters II & V) and circuit-level (Chapters III & IV) implementation.

In Chapter II, a fully integrated ultra high-frequency (UHF) broadband direct-conversion receiver (tuner) for DVB-H standard is presented. Given specifications from DVB-H standard, we partition the block specifications with automatic gain control (AGC) in both RF front-end and baseband. Employing two AGC loops (RF and baseband) in the design maximizes the dynamic range of the tuner system with power optimization. No harmonic rejection scheme is employed since LO harmonic frequencies used for down conversion are out of band eliminating harmonic mixing. RFVGA with a modifed shunt feedback structure provides gain independent matching regardless of variable gain setting. A single ended RF input reduces the system cost without the use of the external balun. Complementary NMOS and PMOS input transconductor with source degeneration provides on-chip single to differential conversion (active-balun) with high linearity. Current mode passive mixer follows the transconductor and the down converted signal is processed by filters with built in anti-

aliasing. Targeted to operate between 470-862 MHz, the tuner system achieves a noise figure of 7.9dB, an IIP3 of -8dBm at maximum gain, and an IIP3 of +2dBm at 9dB RF attenuation. The gain- and frequency-programmable baseband section implements an 8th order inverse Chebyshev low pass approximation achieving >42dB attenuation at an offset of 1.75MHz for the 4MHz frequency setting. Overall, the tuner consumes 120mW from 1.8V analog/2.5V digital dual supply and occupies $2.14mm^2$ in IBM 0.18-μm RFCMOS technology.

In Chapter III, a wideband CG-LNA architecture employing dual negative feedback is presented. Properties of the CG-LNA and its low-noise techniques are discussed prior to the analysis of the proposed CG-LNA architecture. The detailed analysis on the architecture shows that the proposed scheme enables broadband impedance matching, low noise, large gain, enhanced linearity, and wide bandwidth concurrently by employing an efficient and reliable dual negative-feedback. An amplifier prototype was realized in 0.18μm CMOS, operates from 1.05 to 3.05GHz, and dissipates 12.6mW from a 1.8V supply while occupying 0.073mm^2 active area. The LNA provides 16.9dB maximum voltage gain, 2.57dB minimum NF, better than -10dB input matching, and -0.7dBm minimum IIP_3 across the entire bandwidth.

In Chapter IV, an inductor-less active-balun architecture based on the CG-CS topology for multi-standard radio applications is proposed. Current state of the art RF systems require very low sensitivity level, and an active balun, which provides gain and occupies small area, is desirable eliminating the lossy and narrowband external balun. The proposed architecture employing negative feedback features lower power and wider bandwidth with minimal noise contribution due to the active current source. On the other hand, previous works [43, 53, 54] used the passive device as a current source susceptible to PVT variations. The frequency compensation in CS stage ensures better gain and phase balance. The prototype was realized in 0.13μm

CMOS, operates from 0.5 to 4GHz, and dissipates 2.6mW from 1.2V supply while occupying 0.075mm^2 active area. The Balun-LNA provides 17.4dB maximum voltage gain, 3.56dB minimum NF, better than -10dB input matching, and -0.45dBm IIP_3.

In Chapter V, a broadband quadrature receiver architecture with a single LNTA is proposed. A current mode passive mixer void of DC current shows a significant reduction in its flicker (low-frequency) noise. The baseband TIA is further optimized in its noise performance. Therefore, the proposed receiver is suitable for a direct-conversion receiver where the signal resides around DC frequency. Distortion associated with a large voltage swing in Gilbert cell mixer and voltage-mode passive mixer is eliminated thanks to TIA's virtual ground. The receiver achieves improved OOB interference performance as well with a single pole filtering prior to I-V conversion. The proposed LNTA in CG configuration utilizes capacitor cross-coupling and positive feedback from the cascode node of the amplifier and breaks the trade-off betweeen input impedance, trans-conductance, and LNTA load impedance. Effective trans-conductance (G_m) of the proposed CG LNTA can be increased more than $1/2R_S$ and improved current gain of LNTA allows large gain and low NF for the proposed receiver. The proposed quadrature sampling mixer switches do not require 50% duty-cycle $2f_{LO}$ nor 25% duty-cycle f_{LO} and therefore, power consumption on the LO portion is significantly reduced. A miller compensation scheme is avoided and feed-forward compensation is employed featuring wideband low input impedance and non out-of-band peaking in its single-pole filtering response. Simulation results of the proposed receiver demonstrate >22dB conversion gain, <7dB NF, and >0.5dBm IIP_3 from 2GHz to 6GHz. Better than -10dB input matching is achieved from 2GHz to 7.7GHz, while dissipating 13mW from RF and baseband signal path with 1.2V supply. The chip has an active area of 1.1mm^2 and is fabricated in 0.13μm CMOS process.

REFERENCES

[1] Z. Ru, "Frequency translation techniques for interference-robust software-defined radio receivers," Ph.D. dissertation, University of Twente, Enschede, Netherlands, 2009.

[2] O. Ikeuchi, N. Saito, and B. Nauta, "Quadrature sampling mixer topology for SAW-Less GPS receivers in 0.18μm CMOS," in *Symp. on VLSI Circuits*, Jun. 2010, pp. 177–178.

[3] S. Chehrazi, A. Mizraei, R. Bagheri, and A. Abidi, "The software radio architecture," *IEEE Commun. Mag.*, vol. 33, no. 5, pp. 26–38, May 1995.

[4] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice Hall, 1998.

[5] P. Antoine, P. Bauser, H. Beaulaton, M. Buchholz, D. Carey, T. Cassagnes, T. K. Chan, S. Colomines, F. Hurley, D. T. Jobling, N. Kearney, A. C. Murphy, J. Rock, D. Salle, and T. Cao-Thung, "A direct-conversion receiver for DVB-H," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2536–2546, Dec. 2005.

[6] M. Womac, A. Deiss, T. Davis, R. Spencer, B. Abesingha, and P. Hisayasu, "Dual-band single-ended-input direct-conversion DVB-H receiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 610–611.

[7] K. Iizuka, H. Kawamura, T. Fujiwara, K. Kagoshima, S. Kawama, H. Kijima, M. Koutani, S. Toyoyama, and K. Sakuno, "A 184mW fully integrated DVB-H tuner with a linearized variable gain LNA and quadrature mixers using cross-coupled transconductor," *IEEE J. Solid-State Circuits*, vol. 42, no. 4, pp. 862–871, Apr. 2007.

[8] I. Vassiliou, K. Vavelidis, S. Bouras, S. Kavadias, Y. Kokolakis, G. Kamoulakos, A. Kyranas, C. Kapnistis, and N. Haralabidis, "A 0.18mum CMOS dual-band direct-conversion receiver," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 606–607.

[9] Y. J. Kim, J. W. Kim, V. N. Parkhomenko, D. Baek, J. H. Lee, E. Y. Sung, L. Nam, and B. H. Park, "A multi-band multi-mode CMOS direct-conversion DVB-H tuner," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 608–609.

[10] I. Vassiliou, K. Vavelidis, N. Haralabidis, A. Kyranas, Y. Kokolakis, S. Bouras, G. Kamoulakos, C. Kapnistis, S. Kavadias, N. Kanakaris, E. Metaxakis, C. Kokozidis, and H. Peyravi, "A 65nm CMOS multistandard, multiband TV tuner for mobile and multimedia applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1522–1533, Jul. 2008.

[11] R. Kulkarni, "Analog baseband filters and mixed signal circuits for broadband receiver systems," Ph.D. dissertation, Texas A&M University, College Station, Texas, 2011.

[12] J. Xiao, "Cmos RF front-end design for terrestrial and mobile digital television systems," Ph.D. dissertation, Texas A&M University, College Station, Texas, 2007.

[13] J. Xiao, I. Mehr, and J. Silva-Martinez, "A high dynamic range CMOS variable gain amplifier for mobile DTV tuner," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 292–301, Feb. 2007.

[14] N. Poobuapheun, W.-H. Chen, Z. Boos, and A. Niknejad, "A 1.5-V 0.7-2.5-GHz CMOS quadrature demodulator for multiband direct-conversion receivers,"

IEEE J. Solid-State Circuits, vol. 42, no. 8, pp. 1669–1677, Aug. 2007.

[15] M. Banu, J. M. Khoury, and Y. Tsividis, "Fully differential operational amplifiers with accurate output balancing," *IEEE J. Solid-State Circuits*, vol. 23, no. 6, pp. 1410–1414, Jun. 1988.

[16] K. Vavelidis, I. Vassiliou, T. Georgantas, A. Yamanaka, S. Kavadias, G. Kamoulakos, C. Kapnistis, Y. Kokolakis, A. Kyranas, P. Merakos, I. Bouras, S. Bouras, S. Plevridis, and N. Haralabidis, "A dual-band 5.15-5.35-GHz, 2.4-2.5-GHz 0.18μm CMOS transceiver for 802.11a/b/g wireless LAN," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1180–1184, Jul. 2004.

[17] M. Zargari, M. Terrovitis, S. H.-M. Jen, B. J. Kaczynski, M. Lee, M. P. Mack, S. S. Mehta, S. Mendis, K. Onodera, H. Samavati, W. W. Si, K. Singh, A. Tabatabaei, D. Weber, D. K. Su, and B. A. Wooley, "A single-chip dual-band tri-mode CMOS transceiver for IEEE 802.11a/b/g wireless LAN," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2239–2249, Dec. 2004.

[18] A. Liscidini, M. Brandolini, D. Sanzogni, and R. Castello, "A 0.13μm CMOS front-end for DCS1800/UMTS/802.11b-g with multi-band positive feedback LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 981–988, Apr. 2006.

[19] P. Rossi, A. Liscidini, M. Brandolini, and F. Svelto, "A variable gain RF front-end, based on a voltage-voltage feedback LNA, for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368–374, Feb. 2004.

[20] M. El-Nozahi, E. Sánchez-Sinencio, and K. Entesari, "A CMOS low-noise amplifier with reconfigurable input matching network," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 5, pp. 1054–1062, May 2009.

[21] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers–theory, design, and applications," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 288–301, Jan. 2002.

[22] T.-K. Nquyen, G. Ihm, M. Yang, and S. Lee, "CMOS low-noise amplifier design optimization techniques," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 5, pp. 1433–1442, May 2004.

[23] C. Kim, M. Kang, P.-T. Ahn, H. Kim, and S. Lee, "An ultra-wideband CMOS low-noise amplifier for 3-5-GHz UWB system," *IEEE J. Solid-State Circuits*, vol. 40, no. 2, pp. 544–547, Feb. 2005.

[24] W.-H. Chen, G. Liu, B. Zdravko, and A. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1164–1176, May 2008.

[25] W. Zhuo, X. Li, S. Shekhar, S. H. K. Embabi, J. P. de Gyvez, D. J. Allstot, and E. Sánchez-Sinencio, "A capacitor cross-coupled common-gate low-noise amplifier," *IEEE Trans. Circuits Syst. II*, vol. 52, no. 12, pp. 875–879, Dec. 2005.

[26] X. Guan and A. Hajimiri, "A 24GHz CMOS front-end," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 368–374, Feb. 2004.

[27] S. Woo, W. Kim, C. Lee, K. Lim, and J. Laskar, "A 3.6mW differential common-gate CMOS LNA with positive-negative feedback," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 218–219.

[28] Y. Cheng, C.-H. Chen, M. Matloubian, and M. J. Deen, "High-frequency small signal ac and noise modeling of MOSFETs for RF IC design," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 400–408, Mar. 2002.

[29] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[30] Q. Huang, F. Piazza, P. Orsatti, and T. Ohguro, "The impact of scaling down to deep submicron on CMOS RF circuits," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 1023–1036, Jul. 1998.

[31] F. Bruccoleri, E. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal-noise cancelling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[32] C.-F. Liao and S.-I. Liu, "A broadband noise-canceling CMOS LNA for 3.1-10.6-GHz UWB receivers," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 2, pp. 329–339, Feb. 2007.

[33] V. Aparin and L. E. Larson, "Modified derivative superposition method for linearizing FET low-noise amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 2, pp. 571–581, Feb. 2005.

[34] T. W. Kim, B. Kim, and K. Lee, "Highly linear receiver front-end adopting MOSFET linearization by multiple gated transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 223–229, Jan. 2004.

[35] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Trans. Circuits Syst. II*, vol. 46, no. 3, pp. 315–325, Mar. 1999.

[36] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits and 4th ed.* New York, NY: Wiley, 2001.

[37] P. Wambacq and W. Sansen, *Distortion Analysis of Analog Integrated Circuits.* Boston, MA: Kluwer Academic, 1998.

[38] A. Rofougaran, J. Y.-C. Chang, M. Rofougaran, and A. A. Abidi, "A 1-GHz CMOS RF front-end IC for a direct-conversion wireless receiver," *IEEE J. Solid-State Circuits*, vol. 31, no. 7, pp. 880–889, Jul. 1996.

[39] R. Ramzan, S. Andersson, J. Dabrowski, and C. Svensson, "A 1.4V 25mW inductorless wideband LNA in $0.13\mu m$ CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 424–425.

[40] J. Borremans, P. Wambacq, and D. Linten, "An ESD-Protected DC-to-6GHz 9.7mW LNA in $90nm$ digital CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2007, pp. 422–423.

[41] J.-H. C. Zhan and S. S. Taylor, "A 5GHz resistive feedback CMOS LNA for low-cost multi-standard applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 721–730.

[42] A. Bevilacqua and A. M. Niknejad, "An Ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259–2268, Dec. 2004.

[43] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "A wideband Balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, no. 6, pp. 1341–1350, Jun. 2008.

[44] J. Kim, S. Hoyos, and J. Silva-Martinez, "Wideband common-gate CMOS LNA employing dual negative feedback with simultaneous noise, gain, and bandwidth optimization," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 9, pp. 2340–2351, Sep. 2010.

[45] J. Ryynanen, K. Kivekas, J. Jussila, A. Parssinen, and K. A. I. Halonen, "A dual-band RF front-end for WCDMA and GSM applications," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp. 1198–1204, Aug. 2001.

[46] J. Ryynanen, K. Kivekas, J. Jussila, L. Sumanen, A. Parssinen, and K. A. I. Halonen, "A single-chip multimode receiver for GSM900, DCS1800, PCS1900, and WCDMA," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 594–602, Apr. 2003.

[47] S. Parisi, "180 degree lumped hybrid," in *IEEE MTT Symposium*, May 1989, pp. 1243–1246.

[48] M. Goldfarb and A. Platzker, "A wide range analog MMIC attenuator with integral 180 degree phase shifter," *IEEE Trans. Microw. Theory Tech.*, vol. 42, no. 1, pp. 156–158, Jan. 1994.

[49] M. Goldfarb, J. B. Cole, and A. Platzker, "A novel MMIC biphase modulator with variable gain using enhancement-mode FETS suitable for 3V wireless applications," in *IEEE MTT-S Int. Microwave Symp*, May 1994, pp. 99–102.

[50] S. Joo, T. Y. Choi, J. Y. Kim, and B. Jung, "A 3-to-5 GHz UWB LNA with a low-power balanced active balun," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Jun. 2009, pp. 303–306.

[51] M. Rajashekharaiah, P. Upadhyaya, D. Heo, and E. Chen, "A new gain controllable on-chip active balun for 5GHz direct conversion receiver," in *IEEE ISCAS*, May 2005, pp. 5115–5118.

[52] H. Ma, S. J. Fang, F. Lin, and H. Nakamura, "Novel active differential phase splitters in RFIC for wireless applications," *IEEE Trans. Microw. Theory Tech.*,

vol. 46, no. 12, pp. 2597–2603, Dec. 1998.

[53] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, "THE BLIXER a wideband Balun-LNA-I/Q-Mixer topology," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2706–2715, Dec. 2008.

[54] H. Wang, L. Zhang, and Z. Yu, "A wideband inductorless LNA with local feedback and noise cancelling for low-power low-voltage applications," *IEEE Trans. Circuits Syst.*, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.

[55] G. Zhang, "CMOS front-end ampliifier for broadband DTV tuner," Master's thesis, Texas A&M University, College Station, Texas, May 2005.

[56] R. B. Blackman, "Effect of feedback on impedance," *Bell Syst. Tech. J.*, vol. 23, pp. 269–277, Oct. 1943.

[57] P. J. Hurst, "A comparison of two approaches to feedback circuit analysis," *IEEE Trans. Education*, vol. 35, no. 3, pp. 253–261, Aug. 1992.

[58] K. Bult and H. Wallinga, "A class of analog CMOS circuits based on the square-law characteristic of an MOS transistor in saturation," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 3, pp. 357–365, Jun. 1987.

[59] B. Gilbert, "The MICROMIXER: A highly linear variant of the Gilbert mixer using a bisymmetric Class-AB input stage," *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1412–1423, Sep. 1997.

[60] B. Afshar and A. M. Niknezad, "X/Ku band CMOS LNA design techniques," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2006, pp. 389–392.

[61] S. Chehrazi, A. Mizraei, R. Bagheri, and A. Abidi, "A 6.5 GHz wide-band CMOS low noise amplifier for multi-band use," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2005, pp. 796–799.

[62] R. Bagheri, A. Mizraei, S. Chehrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang, and A. Abidi, "An 800-MHz-6 GHz software-defined wireless receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860–2876, Dec. 2006.

[63] H. Darabi and A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, Jan. 2000.

[64] N. Kim, V. Aparin, and L. E. Larson, "A resistively degenerated wideband passive mixer with low noise figure and high IIP_2," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 4, pp. 820–830, Apr. 2010.

[65] W. Redman-White, D. M. Leenaerts, and W. Leenaerts, "1/f noise in passive CMOS mixers for low and zero IF integrated receivers," in *Proc. Eur. Solid-State Circuits Conf.*, Sep. 2001, pp. 41–44.

[66] N. Kim, L. E. Larson, and V. Aparin, "A highly linear SAW-less CMOS receiver using a mixer with embedded Tx filtering for CDMA," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2126–2137, Aug. 2009.

[67] Z. Ru, N. A. Moseley, E. A. M. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.

[68] M. Valla, G. Montagna, R. Castello, R. Tonietto, and I. Bietti, "A 72-mW CMOS 802.11a direct conversion front-end with 3.5-dB NF and 200-kHz 1/f

noise corner," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, Apr. 2005.

[69] B. R. Carlton, J. S. Duster, S. S. Taylor, and J. C. Zhan, "A 2.2dB NF, 4.9-6 GHz direct conversion multi-standard RF receiver front-end in 90 nm CMOS," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Jun. 2008, pp. 617–620.

[70] Y. Feng, G. Takemura, S. Kawaguchi, and P. Kinget, "Design of a high performance 2-GHz Direct-Conversion Front-End With a Single-Ended RF Input in 0.13μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1380–1390, May 2009.

[71] H. Khatri, P. S. Gudem, and L. E. Larson, "Distortion in current commutating passive CMOS downconversion mixers," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 11, pp. 2671–2681, Nov. 2009.

[72] H. T. Friis, "Noise figure of radio receivers," *Proc. IRE*, pp. 419–422, Jul. 1944.

[73] J.-H. Zhan and S. S. Taylor, "A 5 GHz resistive-feedback CMOS LNA for low-cost multi-standard applications," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 721–730.

[74] N. Poobuapheun, W.-H. Chen, Z. Boos, and A. M. Kiknezad, "A 1.5-V 0.7-2.5-GHz CMOS quadrature demodulator for multiband direct-conversion receivers," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1669–1677, Aug. 2007.

[75] D. Manstretta, M. Brandolini, and F. Svelto, "Second-order intermodulation mechanisms in CMOS downconverters," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394–406, Mar. 2003.

[76] R. S. Pullela, T. Sowlati, and D. Rozenbilt, "Low flicker-noise quadrature mixer topology," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2006, pp. 1870–1879.

[77] A. Shahani, D. K. Shaeffer, and T. H. Lee, "A 12-mW wide dynamic range CMOS front-end for a portable GPS receiver," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2061–2070, Dec. 1997.

[78] J.-H. Zhan, B. R. Carlton, and S. S. Taylor, "A broadband low-cost direct-conversion receiver front-end in 90nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1132–1137, May 2008.

[79] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY: McGraw-Hill, 2001.

[80] J. Crols and M. S. J. Steyaert, "A 1.5-GHz highly linear CMOS downconversion mixer," *IEEE J. Solid-State Circuits*, vol. 30, no. 7, pp. 736–742, Jul. 1995.

[81] B. K. Thandri and J. Silva-Martinez, "A robust feedforward compensation scheme for multistage operational transconductance amplifiers with no miller capacitors," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 237–243, Feb. 2003.

[82] B. Razavi, *Design of Integrated Circuits for Optical Communications*. New York, NY: McGraw-Hill, 2002.

[83] A. Amer, E. Hegazi, and H. F. Ragaie, "A 90-nm wideband merged CMOS LNA and mixer exploiting noise cancellation," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 323–328, Feb. 2007.

APPENDIX A

EFFECT OF C_B ON AMPLIFIER'S BANDWIDTH

Including the effect of C_B, the high frequency voltage gain becomes

$$A_v(s) = A_{vo}\frac{N(s)}{D(s)}. \tag{A.1}$$

where $N(s)$ and $D(s)$ are

$$N(s) = 1 + \frac{g_{m1}(C_B + C_{p2}) - g_{m2}C_B}{g_{m1}(g_{m2} + g_{m3})}s + \frac{C_A C_B}{g_{m1}(g_{m2} + g_{m3})}s^2, \tag{A.2}$$

$$\begin{aligned} D(s) &= 1 + \frac{g_{m1}C_B R_L + g_{m3}C_{p1}R_L + (C_A + C_B + C_{p2})}{g_{m3}(1 + g_{m1}R_L)}s \\ &\quad + \frac{(C_{p1} + C_B)(C_{p2} + C_A)R_L + C_{p1}C_B R_L}{g_{m3}(1 + g_{m1}R_L)}s^2. \end{aligned} \tag{A.3}$$

Assuming $g_{m1}R_L > 1$, $C_{p1} >> C_B$, and $g_{m2} >> g_{m3}$, (A.1) can be approximated as

$$A_v(s) = A_{vo}\frac{1 + \left(\frac{C_B + C_{p2}}{g_{m2}} - \frac{C_B}{g_{m1}}\right)s + \frac{C_A C_B}{g_{m1}g_{m2}}s^2}{1 + \left(\frac{C_B}{g_{m3}} + \frac{C_{p1}}{g_{m1}} + \frac{C_A + C_B + C_{p2}}{g_{m1}g_{m3}R_L}\right)s + \frac{C_{p1}(C_A + C_B + C_{p2})}{g_{m3}g_{m1}}s^2}. \tag{A.4}$$

An additional zero is created by the feed-forward path from the input to the output due to parasitic capacitance C_B. Therefore, small C_B in the design should be ensured not to hurt the reverse isolation and stability. The pole location under dominant pole assumption can be derived as

$$\omega_1 \approx \frac{g_{m1}}{C_{p1}}, \quad \omega_2 \approx \frac{g_{m3}}{C_A + C_B + C_{p2}}, \tag{A.5}$$

or

$$\omega_1 \approx \alpha\frac{g_{m3}}{(C_A + C_B + C_{p2})}, \quad \omega_2 \approx \frac{1}{\alpha}\frac{g_{m1}}{C_{p1}}, \tag{A.6}$$

where ω_1 is the dominant pole and ω_2 is the non-dominant pole. Coefficient α is given by

$$\alpha = \left(\frac{1}{g_{m1} R_L} + \frac{C_B}{C_A + C_B + C_{p2}} \right)^{-1}. \tag{A.7}$$

In the first case (A.5), bandwidth is enhanced by the factor of forward path gain $g_{m1}R_L$ for $\frac{1}{R_L C_{p1}}$ as before. The non-dominant pole is shifted down from $\frac{g_{m3}}{C_A+C_{p2}}$ to $\frac{g_{m3}}{C_A+C_B+C_{p2}}$ with C_B included in the analysis. In the second case (A.6), the dominant pole at the feedback summing node is enhanced by α, the design dependent parameter.

APPENDIX B

NON-LINEAR ANALYSIS USING VOLTERRA SERIES

Here, the numerical computation of the Volterra series up to the third-order coefficients is evaluated with the direct calculation method.

First, the small signal gate-source voltages for nonlinear transistor M_1, M_2, and M_3 is modeled by the Volterra kernels in terms of the excitation voltage v_s:

$$v_a = v_y - v_x = A_1(s) \circ v_s + A_2(s_1, s_2) \circ v_s^2 + A_3(s_1, s_2, s_3) \circ v_s^3, \tag{B.1}$$

$$v_b = v_x = B_1(s) \circ v_s + B_2(s_1, s_2) \circ v_s^2 + B_3(s_1, s_2, s_3) \circ v_s^3, \tag{B.2}$$

$$v_c = v_{out} - v_y = C_1(s) \circ v_s + C_2(s_1, s_2) \circ v_s^2 + C_3(s_1, s_2, s_3) \circ v_s^3, \tag{B.3}$$

where $s(= j\omega)$ is the Laplace variable, and the operator "$\circ$" means that the magnitude and phase of each spectral component of v_s^n is to be changed by the magnitude and phase of the corresponding n_{th} order Volterra kernels [33]. As in (3.20), nonlinear drain current for M_1, M_2, and M_3 can be expanded by power series:

$$i_{ds,M1} = g_{m1} v_a + K_{2g_{m1}} v_a^2 + K_{3g_{m1}} v_a^3, \tag{B.4}$$

$$i_{ds,M2} = g_{m2} v_b + K_{2g_{m2}} v_b^2 + K_{3g_{m2}} v_b^3, \tag{B.5}$$

$$i_{ds,M3} = g_{m3} v_c + K_{2g_{m3}} v_c^2 + K_{3g_{m3}} v_c^3. \tag{B.6}$$

Applying the Kirchhoff's current law equations for each node of the circuit in Fig. 20, we have

$$\frac{v_x - v_s}{Z_s(s)} + \frac{v_x}{Z_x(s)} + (g_{m1} + sC_A)(v_x - v_y) = i_{NL,1}, \tag{B.7}$$

$$(g_{m3} + sC_B)(v_y - v_{out}) + g_{m2} v_x + \frac{v_y}{Z_y(s)} + sC_A (v_y - v_x) = i_{NL,3} - i_{NL,2}, \tag{B.8}$$

$$\frac{v_{out}}{Z_L(s)} + g_{m1}(v_y - v_x) + sC_B (v_{out} - v_y) = -i_{NL,1}, \tag{B.9}$$

$$\begin{bmatrix} g_{m1}+sC_A+\frac{1}{Z_x(s)}+\frac{1}{Z_s(s)} & -(g_{m1}+sC_A) & 0 \\ g_{m2}-sC_A & g_{m3}+sC_A+sC_B+\frac{1}{Z_y(s)} & -(g_{m3}+sC_B) \\ g_{m1} & sC_B-g_{m1} & -\left(sC_B+\frac{1}{Z_L(s)}\right) \end{bmatrix} \begin{bmatrix} v_{x,n} \\ v_{y,n} \\ v_{out,n} \end{bmatrix} = \begin{bmatrix} \frac{v_s}{Z_s(s)}+i_{NL,1} \\ i_{NL,3}-i_{NL,2} \\ i_{NL,1} \end{bmatrix} \tag{B.15}$$

where

$$Z_s(s) = R_s + \frac{1}{sC_{in}}, \tag{B.10}$$

$$Z_x(s) = \frac{sL_{bias}}{1+s^2L_{bias}\left(C_{pad}+C_{gs2}+C_{gb2}+C_{sb1}\right)}, \tag{B.11}$$

$$Z_y(s) = \frac{R_{bias}}{1+sR_{bias}\left(C_{ds2}+C_{db2}+C_{sb3}\right)}, \tag{B.12}$$

$$Z_L(s) = \frac{R_L}{1+sR_LC_L}. \tag{B.13}$$

Regardless of the order of Volterra kernel, the calculation can be represented by the solution of the following general matrix equation [37]

$$Y(s)H_n(s) = IN_n(s), \tag{B.14}$$

where $Y(s)$ is the admittance matrix of the circuit, $H_n(s)$ is the vector of n_{th} order Volterra kernel, and $IN_n(s)$ is the vector of excitations and n_{th} order nonlinear current sources. The matrix equation for the proposed LNA is derived from (B.7), (B.8), and (B.9) as shown in (B.15) at the top of the page.

To find the linear transfer function $A_1(s)$, $B_1(s)$, and $C_1(s)$, set excitation voltage ($v_s \leftarrow 1$) and nonlinear current sources ($i_{NL,j} \leftarrow 0$). $v_{a,1} = v_{y,1} - v_{x,1}$, $v_{b,1} = v_{x,1}$, and $v_{c,1} = v_{out,1} - v_{y,1}$ determines the desired transfer function after the matrix inversion. To find the second-order transfer function, nonlinear current sources of order two is applied to the linearized network in (B.15) with short-circuited excitation voltage

(v_s). Nonlinear transconductance of order two is as follows.

$$i_{NL,j} = K_{2gm,j} H_{1j}(s_1) H_{1j}(s_2) \tag{B.16}$$

where $K_{2gm,j}$ is second-order nonlinearity coefficient for the transistor M_j. $H_{1j}(s)$ is the first-order transfer function of the corresponding gate-source voltage for the transistor M_j. Then, second-order volterra kernels $A_2(s_1, s_2)$, $B_2(s_1, s_2)$, and $C_2(s_1, s_2)$ are derived from

$$Y(s_1 + s_2) H_2(s_1, s_2) = IN_2(s_1, s_2). \tag{B.17}$$

The computation of third-order kernels are similar to the second-order computation. The desired third-order output voltage kernel, $C_3(s_1, s_2, s_3)$ is derived from the solution of the following matrix equation with nonlinear current source shown below.

$$Y(s_1 + s_2 + s_3) H_3(s_1, s_2, s_3) = IN_3(s_1, s_2, s_3) \tag{B.18}$$

$$i_{NL,j} = K_{3gm,j} H_j(s_1) H_j(s_2) H_j(s_3) + 2K_{2gm,j} \overline{H_{1j}(s_1) H_{2j}(s_2, s_3)} \tag{B.19}$$

where the bar indicates the averaging of the transfer function over all possible permutations of the Laplace variables [33]. $H_{1j}(\cdot)$ and $H_{2j}(\cdot)$ are the first-order and second-order transfer function of the corresponding gate-source voltage. For a two tone excitation at ω_a and ω_b, IIP_3 as the available power of the signal generator at the third-order intercept point is given by [33]

$$IIP_3\,(2\omega_b - \omega_a) = \frac{1}{6\Re\,(Z_1(s_a))} \left| \frac{C_1(s_a)}{C_3(s_b, s_b, -s_a)} \right|. \tag{B.20}$$

APPENDIX C

DE-EMBEDDING NF FOR STAND-ALONE BALUN-LNA

The stand-alone buffer for de-embedding purpose was not implemented. Then, the effect of probe buffer is de-embedded from the simulation results of stand-alone buffer. The probe buffer's input-referred voltage noise is the double the quantity of a source-follower, which is

$$\overline{v_{buffer,in}^2/\Delta f} = 2\left[4kT\gamma/g_{m5} + 4kT\gamma g_{m6}/g_{m5}^2\right] \tag{C.1}$$

where g_{m5} and g_{m6} are trans-conductance of source-follower device and current-source device respectviely in the probe buffer. NF measured in the lab includes the noise due to balun-LNA and probe buffer as well, which can be expressed as

$$NF_{mea} = 1 + \frac{v_{core,out}^2/\Delta f + v_{buffer,in}^2/\Delta f}{4kT \cdot R_S \cdot \left(\frac{R_{in}}{R_{in}+R_S}\right) \cdot A_V^2} \tag{C.2}$$

$$A_V = \frac{S_{21,mea}}{\frac{1}{\sqrt{2}} \cdot \left(\frac{g_{m5}}{g_{m5}+1/R_L}\right)} \tag{C.3}$$

where $v_{core,out}$ is output-referred noise voltage due to balun-LNA core and $v_{buffer,in}$ is input-referred noise voltage due to probe buffer. Denominator in (C.3) is the combined effect of signal loss at the buffer output and the conversion from 50Ω input to 100Ω output. The anlytical expression, (C.2), is derived at the output of balun-LNA and the input of probe buffer, but de-embedding buffer's noise can be applied to (C.2) with NF_{mea} and $S_{21,mea}$ at the probe buffer output.

Then, NF of stand-alone balun-LNA denoted as NF_{core} can be derived from measured NF_{mea} and $S_{21,mea}$, and simulated g_{m5} and g_{m6}. as shown below.

$$NF_{core} = NF_{mea} - \frac{v_{buffer,in}^2/\Delta f}{4kT \cdot R_S \cdot \left(\frac{R_{in}}{R_{in}+R_S}\right) \cdot A_V^2} \tag{C.4}$$

VITA

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