ENERGY HARVESTING FOR SELF-POWERED WIRELESS SENSORS

A Dissertation

by

JASON LEE WARDLAW

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2011

Major Subject: Electrical Engineering

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ABSTRACT

Energy Harvesting for Self-Powered Wireless Sensors. (December 2011)

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A wireless sensor system is proposed for a targeted deployment in civil infrastructures (namely bridges) to help mitigate the growing problem of deterioration of civil infrastructures. The sensor motes are self-powered via a novel magnetic shape memory alloy (MSMA) energy harvesting material and a low-frequency, low-power rectifier multiplier (RM). Experimental characterizations of the MSMA device and the RM are presented. A study on practical implementation of a strain gage sensor and its application in the proposed sensor system are undertaken and a low-power successive approximation register analog-to-digital converter (SAR ADC) is presented. The SAR ADC was fabricated and laboratory characterizations show the proposed low-voltage topology is a viable candidate for deployment in the proposed sensor system. Additionally, a wireless transmitter is proposed to transmit the SAR ADC output using on-off keying (OOK) modulation with an impulse radio ultra-wideband (IR-UWB) transmitter (TX). The RM and SAR ADC were fabricated in ON 0.5μm CMOS process.

An alternative transmitter architecture is also presented for use in the 3-10GHz UWB band. Unlike the IR-UWB TX described for the proposed wireless sensor system, the presented transmitter is designed to transfer large amounts of information with little concern for power consumption. This second method of data transmission divides the 3-10GHz spectrum into 528MHz sub-bands and "hops" between these sub-bands during data transmission. The data is sent over these multiple channels for short distances (≈3-10m) at data rates over a few hundred million bits per second

(Mbps). An UWB TX is presented for implementation in mode-I (3.1-4.6GHz) UWB which utilizes multi-band orthogonal frequency division multiplexing (MB-OFDM) to encode the information. The TX was designed and fabricated using UMC 0.13μm CMOS technology. Measurement results and theoretical system level budgeting are presented for the proposed UWB TX.

To Dorothy, Neuman, Martha, N.J., and Kelly.

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not have been able to complete this.

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CHAPTER I

RESEARCH MOTIVATION

Concrete gained popularity over marble with the Romans for two reasons: 1) it was easier to mold into desired shapes; and 2) it was less costly than other hard materials. The concrete which the Romans used had a comparable compressive strength to the concrete which is used today. The main difference between the concrete used by the Romans and the concrete used today is the reinforced steel, or rebar, in modern concrete. The rebar is a steel rod which is textured to provide better anchoring to the concrete. It is used within modern concrete structures to provide a greater tensile strength than the concrete used by the Romans. One of the main applications of concrete, at least in the U.S., is the construction of roads, highways, and bridges.

A. Introduction

With concrete being such a widely used material in the world it is necessary to insure a robust performance to day-to-day use. However, concrete is usually exposed to elements, changes in the Earth (e.g., earthquakes, mudslides, etc.), and a host of other events which compromise the integrity of concrete structures. Even with the introduction of rebar to improve the tensile strength of concrete, there is only so much damage and abuse a structure can take before it must either be repaired or replaced. One cause of deficient concrete is cracking due to the introduction of water into porous regions which then expand and corrode the concrete's internal structure. Over a period of years this corrosion may lead to larger cracks, holes, or even the eventual collapse of a structure. To avoid accidents, injuries, and deaths it is necessary

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to identify and mitigate any issues which may occur with concrete structures.

1. Structural Health Monitoring

In the U.S. alone there are more than 55,000 interstate bridges in use today, of which approximately 25% are deemed as structurally deficient [1]. It is estimated that it will cost more than $9 billion USD and more than 20 years to fix all deficient bridges while costing even more to maintain the bridges on this list. These reports do not go into full detail on the status of other infrastructures in the U.S. (buildings, roads, etc.). Often times these deficiencies are not a major threat to individuals and their daily routine. Even though the threats are not apparent on a daily basis, the potential to cause damage and injury is there. For example, in late 2007 a portion of I-35 in Minnesota collapsed killing 13 people and injuring 145. According to the National Transportation Safety Board (NTSB), the crash was attributed to an inherent design flaw in the structure and a larger load than the bridge had been designed for [2]. While design flaws are not something that are intended, they do occur. Had a fault detection system been in place during the bridge's operation, perhaps the danger could have been predicted and avoided.

To help mitigate the threats posed by civil infrastructures to people it is necessary to implement methods of determining the state of these civil infrastructures. The term used to describe the analysis and determination of the state of a civil infrastructure is dubbed Structural Health Monitoring (SHM). One of the first implemented, as well as one of the most common methods, of SHM in use today is visual inspection. Road crews drive, walk, climb, etc., along roads and bridges, buildings and other structures, to see if there are any major deficiencies. These inspectors are trained on what types of things to look for (cracks, rigidness, etc.) as well as locations of the most common failures (corners, girder connections, bolts, etc.). One of the drawbacks to this method

is by the time there is visual confirmation of concrete damage it is often beyond repair or the damage has progressed to a stage which cannot be detected through visual methods alone [3]. According to [4], visual inspection has significant shortcomings which affect the ability to properly determine the reliability and accuracy of visual inspection techniques. This is attributed to personal feelings and comfort levels of the evaluators. An example of one factor is an individual's comfort level with heights and their inability to perform an in-depth analysis due to fear.

Although visual inspection should still remain as a method of monitoring civil infrastructures, it is necessary to implement a system based on sensors. To this end, the sensors would provide an unbiased record of the structure. As such, more focus needs to be turned to a system based on mechanical and/or electronic systems to determine if there are structural deficiencies. These SHM systems can typically be classified into two main categories: destructive and non-destructive. Destructive damage evaluation (DDE) is performed when a building, road, bridge, etc., must be torn apart to determine the integrity of the material and to make a determination about any issues which are present. Non-destructive damage evaluation (NDE) is usually performed by studying different properties of the bridge without modifying the structure in any way. Some of the parameters which are evaluated are strain or stress at different points on or within the structure, frequency and modes of vibration, impedance changes and others [3].

An issue with many of the forms of NDE is they either require regular human interaction with the system or they require cables to be distributed throughout the infrastructure to provide power, send and receive information, etc. Ideally, human interaction should be minimized with the system due to inconvenient and/or dangerous sensor placement making it difficult for an individual to access. For typical SHM systems where cables are used to transmit the data to a central data processing point,

it is necessary to have the cables placed appropriately during initial construction of the structure. If the cables become exposed to the elements there is a potential these cables may become damaged. Additionally, if any issues occur where there is a break or a crack in the concrete structure around the cables, a great deal of stress may be placed on the cables causing them to break and require replacement. For systems which are battery powered, the batteries may only last a few days, months, or years before requiring replacement. This is not only an inconvenient task, but it is also one which could prove costly in the event many sensors are used in a given location.

2. Methods of SHM

Since visual inspection in itself is not the most efficient method to determine deficiencies in a structure, SHM has taken on many forms. In [5–10] the authors describe the fact that when a vehicle passes over a bridge or roadway, there is a vibration in the bridge at a specific frequency which is related to the speed of the vehicle, the relative ratio of the masses of the vehicle and the bridge span, as well as the length of the bridge section, among other things. In [11] the authors devise a system which looks at the electrical impedance change of a section of concrete when cracks appear. In [12] Eddy currents are detected through a coil placed along a section of road and impedances are measured and shown to change when a damage is near. Additionally, the impedance difference will be greater the closer one gets to the damage, thus allowing one to determine where the damage is located. In [13] the authors use a method of visual inspection using cameras to determine where faults may be located.

3. Vibration Based SHM

Regardless of how well any system is secured, how much mass a system contains, the ambient/core/operating temperature of a system, etc., everything vibrates. Whether

it is from moving parts within the system, a passer-by driving or walking near the system, or from the rotation of the Earth, everything vibrates. While this is an issue in many cases, for the purpose of powering a sensor network for SHM this is a benefit. Over the past 20 years there has been extensive research in using the vibrational properties of bridges and other structures to determine faults in the system [5–10] and [14–20]. When dealing with vibrations and determining what information should be extracted, there are typically two things that one can look at: frequency of vibration and modal shapes (i.e., the amplitudes and general waveform shapes of the oscillations). Both of these characteristics for a bridge are characteristic of the type of bridge, length of the bridge, length of the bridge span, and other factors. Therefore, these properties must be determined soon after the bridge is completed in order to track any changes. One method of doing this is to measure the driving frequency of the bridge. The driving frequency is determined by using a vehicle with a well-known mass and driving the vehicle over a span of the bridge in question. The data of the bridge vibration is then gathered and the frequencies of vibration of the bridge are then computed using an FFT. The relationship between the speed of a vehicle and its driving frequency is

$$\omega_d = \frac{\pi v}{L} \text{ rad/s} \tag{1.1}$$

where v is the vehicles velocity in meters per second and L is the span of the bridge section. For vehicle speeds of 5, 10 and 15 m/s (11.18, 22.36 and 33.54 mph) the driving frequencies are 0.1, 0.2 and 0.4Hz, respectively. This is typically well below the bridges natural frequency (typically 2-20Hz) and therefore oscillation is avoided. Since most of these vibrations are at low frequencies, the detection of the oscillations should be done with devices having a fairly low input impedance at these frequencies (e.g., inductive and not capacitive as in the case of piezo based measurement equipment)

to facilitate measurements and circuit design.

It has been shown in [7] that the bridge natural frequency changes when there is a damaged section of the bridge. Therefore, it can be concluded that proper detection of this frequency can allow for determination of the state of the bridges health. Once this is done, the information must then be sent back to a data collection center for processing. One method to do this would be running cables throughout the structure, but this may lead to problems as the cables themselves could easily become damaged and would require replacement. To this end, the information should be transmitted wirelessly and the sensors would then be powered from a different source. One method of obtaining power for use in circuits is the use of a battery. However, for SHM, batteryless devices are a better approach as they inherently require less maintenance. Therefore, efforts have been made to scavenge energy from the bridge vibration to power the sensor system [21].

B. Proposed Solution

In this work a self-powered wireless sensor system is proposed with an intended application for NDE SHM of civil infrastructures with a targeted application of bridges, although the system could be applied to any concrete structure. The proposed system is comprised of a a vibrational energy harvesting component, power conditioning circuitry, a sensor, a low-power circuit to convert the sensor information into an electrically digital signal, and a low-power transmitter to send the data to a central data processing location. The proposed system contains no external battery which provides the benefit of fewer human interactions and therefore a lower cost. A general diagram of the proposed system is shown in Fig. 1.

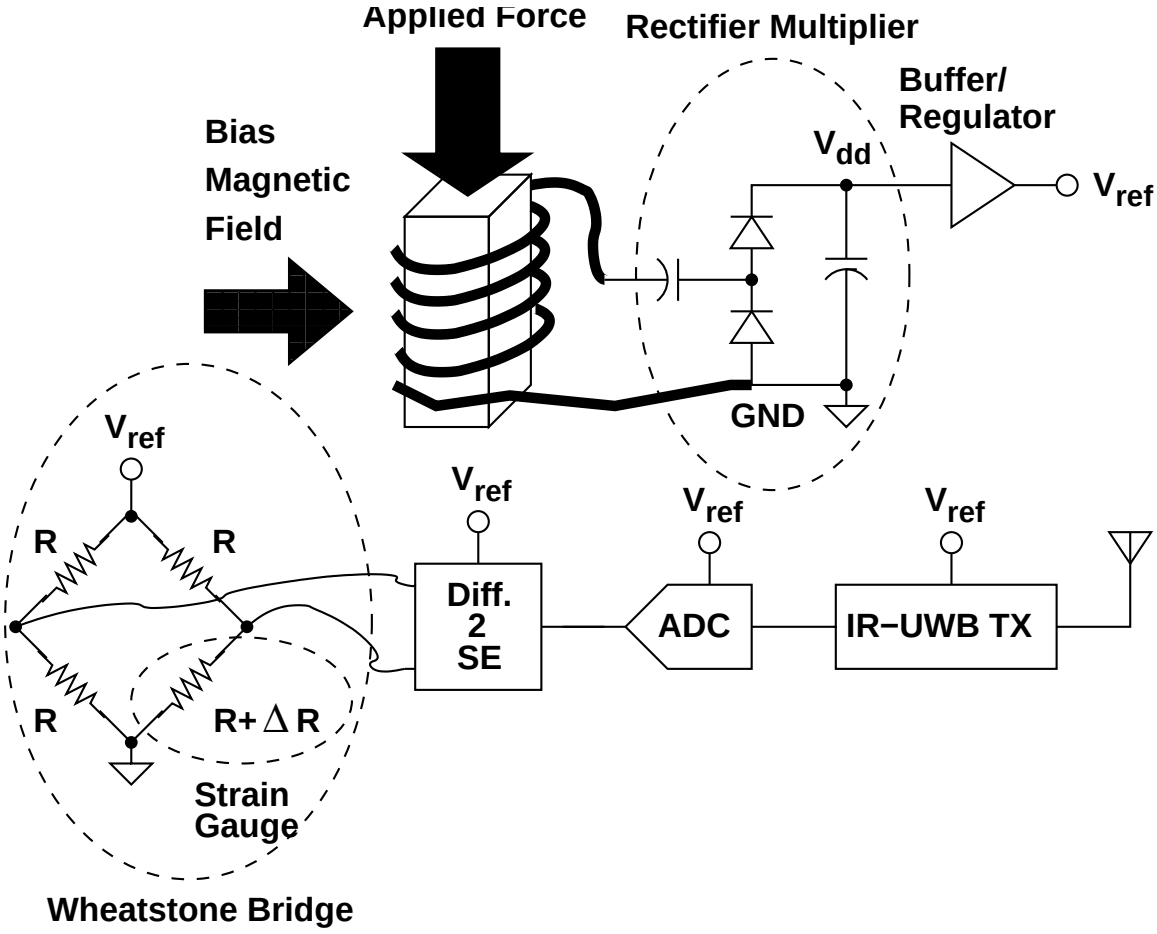

Fig. 1.: Generalized SHM sensor architecture.

C. Dissertation Organization

The dissertation is organized as follows: chapter 2 discusses a Magnetic Shape Memory Alloy (MSMA) material which is intended to serve as the energy harvesting mechanism; chapter 3 discusses some methods of DC power extraction from the MSMA material using low-power and efficiency-enhanced AC-DC converters (rectifiers); chapter 4 provides a discussion on data modulation choices for the sensor information as well as information on the proposed sensor for the wireless sensor system; chapter 5 provides information about the implementation of a wireless transmitter; and chap-

ter 6 is focused on the design, simulation, and measurement of a low-power ADC. In addition to the proposed low-power wireless sensor system, chapter 7 gives the background, design and chip measurement of a mode-I multi-band OFDM ultra-wideband transmitter (MB-OFDM UWB TX). Finally, chapter 8 provides some conclusions and future work.

CHAPTER II

MAGNETIC SHAPE MEMORY ALLOY

A shape memory alloy (SMA) is an alloy which 'remembers' its original shape and will return to this state after deformation. The ability of the SMA to return to its original shape implies the strain applied to the material is in the material's elastic region meaning Hooke's Law (2.1),

$$\sigma = \epsilon E \tag{2.1}$$

where the tensile stress (σ) is equal to the strain (ϵ) times a constant (E =Young's Modulus), still holds. The elastic ability of SMAs have recently made them a viable solution in sensing, actuation, power generation and magnetic refrigeration applications. One of the driving forces behind using these materials for these applications is their structural robustness compared to more brittle devices, namely piezoelectrics. SMAs are typically compounds of CuZnAlNi, NiTi, NiMnX (where X can be Ga or CoIn) or CuAlNi, to name a few. For sensing and power generation applications, systems will typically directly adapt mechanical changes into an electrical signal (as in the case of piezoelectrics). However, this is usually done with a very low conversion efficiency as mechanical changes are typically fairly low frequency ($<$ 1kHz) and the components used to perform the mechanical-to-electrical conversion (MEC) are better suited for higher frequency applications ($>$ 10kHz).

In [22] a method of improving the efficiency of the MEC is proposed where first the magnetic flux change of the material induced by a mechanical change is subsequently converted into an electrical signal. It is shown in this paper that the potential harvestable electrical energy from low frequency vibrations is significant enough to power a sensor and its associated wireless circuitry ($> 100\mu$W). The SMA

used in [22] is slightly different in nature than those which are typically studied as it converts mechanical changes into magnetic flux changes putting it in a class of SMA devices which are known as magnetic shape memory alloys (MSMAs). These MSMA devices are very well-suited for applications where a force will be applied regularly and in a system which will experience regular vibrations. Table I provides a list of different theoretically attainable powers and/or energies from different energy harvesting methods [23]. As is seen from the table, vibrational energy harvesting has the potential to obtain enough energy to power an array of electronic and sensing devices.

A. MSMA

As mentioned previously, to help improve the efficiency of the MEC at lower frequencies, MSMA devices show a greater promise than other materials which are currently employed (namely piezoelectric devices). One of the main reasons why is because piezoelectric materials tend to have an electrical impedance which is capacitive. As such, if the load of the piezoelectric device is not a relatively high impedance at the frequency of excitation then the efficiency of the conversion is limited. Additionally, the piezoelectric device must be excited at a high enough frequency to help lower the effective source impedance and produce a usable output level. Some recently reported results show that practical power levels may be obtained by using piezoelectric devices, but these results still rely on fairly high frequencies and/or the addition of batteries to power the harvesting circuitry [24, 25]. For piezoelectric systems, the mechanical system then becomes the limiting factor as most mechanical systems do not work well and/or are incapable of operating at as high of a frequency as the corresponding electrical circuitry. Although civil structures such as bridges

Table I.

Comparison of different power sources for sensor networks, (modified from [23]).

Power Source	$\frac{\mu W}{cm^3}$	$\frac{J}{cm^3}$	$\frac{\frac{\mu W}{cm^3}}{yr.}$	Add. Storage Req.'d	Volt. Reg.	Easily Obtained
Prim. Batt.	-	2880	90	No	No	Yes
Sec. Batt.	-	1080	34	-	No	Yes
Micro-Fuel Cell	-	3500	110	Maybe	Maybe	No
Heat Engine	-	3346	106	Yes	Yes	No
Radioactive(^{63}Ni)	0.52	1640	0.52	Yes	Yes	No
Solar (out)	$15k^*$	-	-	Usually	Maybe	Yes
Solar (in)	10^*	-	-	Usually	Maybe	Yes
Temp.	40^{**}	-	-	Usually	Maybe	Soon
Human	330	-	-	Yes	Yes	No
Air Flow	380^{***}	-	-	Yes	Yes	No
Vibration	200	-	-	Yes	Yes	Yes*

and buildings have modes of oscillation which occur at higher frequencies, the low frequency vibrations are typically ones with larger amplitudes and therefore larger forces on the power conversion device which then result in larger harvestable output powers. However, the factors which are a severe bottleneck with piezoelectric devices in these systems are an advantage for systems which utilize MSMAs. With MSMA devices, the MEC is performed by sensing a magnetic flux change within the material and then converting the magnetic flux change into an electrical signal via a

pick-up coil. The methods in which this magnetic change occurs is typically through martensitic variant reorientation or martensite phase transformation of the MSMA device [22, 26, 27].

Previous work on energy harvesting using MSMAs has been performed utilizing NiMnGa MSMA single crystalline samples [22]. MSMAs can convert mechanical work, such as from mechanical vibrations, first into a magnetic induction change in the material in the presence of a constant bias magnetic field, which can then be converted into electrical energy through pick-up coils. There are two major mechanically-induced microstructural changes that manifest themselves as large magnetization changes in MSMAs. The first one is the stress/strain-induced rotation of martensite variants (the microstructural change) within the material [22, 28, 29]. Magnetic domains are strongly coupled with martensite variants in the material exhibiting this mechanism such that martensite variant rotation leads to magnetic domain rotation, and thus magnetic flux change. NiMnGa MSMAs utilize this mechanism to harvest energy from mechanical vibrations or otherwise waste mechanical work [22]. The level of current which can be generated in the pick-up coils, and thus the amount of power which may be delivered to a load, depends on the magnetic induction change upon martensite variant rotation, which is measured to be on the order of 0.15 to 0.2 Tesla in near stoichiometric Ni_2MnGa MSMAs [22, 29]. We have recently demonstrated in these materials that the power output levels on the order of a Watt are within reach, upon the conversion of relatively large amplitude mechanical vibrations under 200Hz frequency [22].

The second mechanism of mechanically-induced microstructural and magnetic changes in MSMAs is the stress-induced martensitic phase transformation from a ferromagnetic to a para/antiferro-magnetic phase [26, 27], which is fully reversible upon unloading the stress. This mechanism can cause a large magnetic flux change

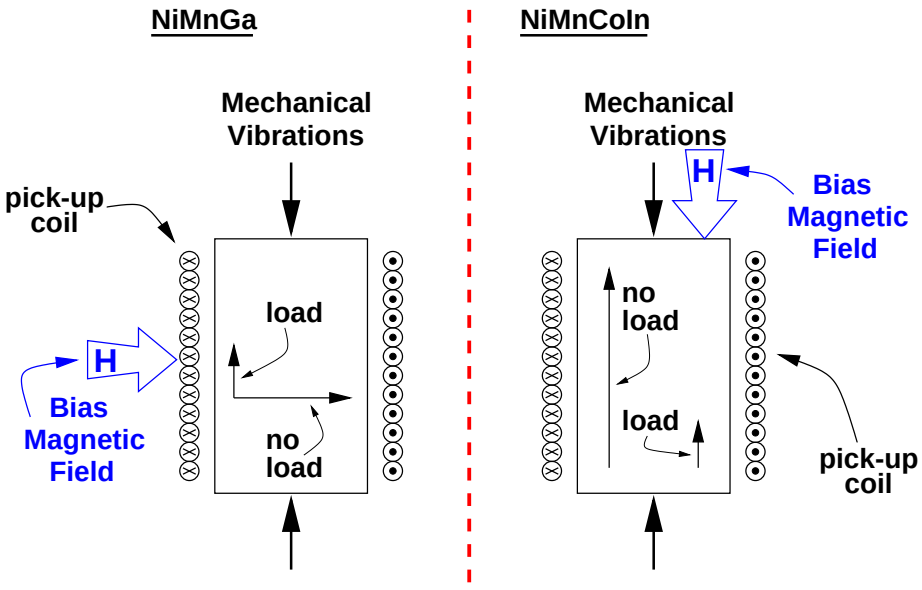

Fig. 2.: Different methods of flux change in NiMnGa and NiMnCoIn MSMAs upon mechanical loading/unloading in the presence of a bias magnetic field.

in the presence of a bias field due to large differences in the saturation magnetizations of the transforming phases. Typical MSMAs exhibiting this large change are NiMnCo(In,Sn,Sb) alloys. They are also called meta-magnetic SMAs because of the simultaneous magnetic and structural phase transitions [27, 30–36]. As compared to the magnetic induction change associated with the mechanically-induced martensite variant rotation, the magnetic induction change during the stress-induced martensitic transformation in these materials can be multiple times higher, depending on the bias field levels [27]. Thus, using meta-magnetic SMAs as energy harvesting materials is more beneficial in terms of power output levels for a given vibrational loading. In addition, the magnetization rotations and the nature of the flux change in these two mechanisms are notably different, as shown in Fig. 2 for a NiMnGa and a NiMnCoIn MSMAs. In NiMnGa, the magnetization direction usually changes from horizontal to vertical in the figure upon loading and vice versa upon unloading (depending on

the single crystal orientation), but this configuration is the best one per [22, 28]. In meta-magnetic SMAs such as NiMnCoIn alloys, the magnetic flux can be aligned perpendicular to the pick-up coil at all times and the magnetization can change from almost zero to maximum (i.e., saturation magnetization) upon loading/unloading. This implies in NiMnCoIn that the maximum flux change can be sensed by the coil and then generate the maximum output voltage. Moreover, since magnetic domains are strongly coupled with microstructure in NiMnGa, it is necessary to use very expensive single crystals. However, in meta-magnetic SMAs, because saturation magnetization levels of the transforming phases dictate the magnetic induction change upon structural phase transformation, relatively inexpensive polycrystals can be used. In the present study, we, thus, implement a NiMnCoIn meta-magnetic SMA as a potential energy harvesting material to convert the mechanical vibrations into a usable electrical signal.

In both MSMA MEC systems, the equivalent source impedance is better suited for low frequency applications as it may typically be modeled by a series combination of a resistor and inductor as opposed to a series resistor and capacitor as is the case in piezoelectric devices. The values of these components are dependent on geometry and choice of material used to extract the electrical signal but may be practically limited to less than 200Ω and $20nH$. While compared to values associated with integrated circuits these values are large, the implementation produces a fairly small physical device (approximately the size of a sugar cube [$\approx 1\text{cm}^3$]).

B. Electromagnetism in the MSMA

Assuming the applied strain/stress/force/etc., is sinusoidal in nature, it is safe to say the magnetic field will have an equation represented by

$$B = B_0 r \sin(\omega t). \tag{2.2}$$

The value of B_0 is half the reversible magnetic flux density change, r is the volume fraction of the material undergoing reorientation and is defined as ϵ/ϵ_{max}, ϵ is the applied strain range, ϵ_{max} is the maximum reorientation strain, and $\omega = 2\pi f$ where f is the frequency of excitation of the material. The values of ϵ and ϵ_{max} are important values as they determine many of the characteristics of the alloy and define a range of energy which may be harvested.

Since the mechanical changes induce a magnetic flux change within the material, a coil is needed to capture the electric field change (as described by Faraday's law of electromagnetic induction). More discussion on the design of the coil, as well as the coil's electrical parameters, will be provided in the following section. The induced voltage may be determined from Faraday's equation

$$V = N\frac{\mathrm{d}\phi}{\mathrm{d}t} = NA\frac{\mathrm{d}B}{\mathrm{d}t}. \tag{2.3}$$

In (2.3) the value of N is the number turns of the coil, ϕ is the magnetic flux within the material, A is the cross sectional area of the magnetic field and B is the induced magnetic field within the material.

Solving for the derivative and the maximum of (2.2) and then substitution of the

simplified form of (2.2) into (2.3) results in

$$\begin{aligned} \frac{\mathrm{d}B}{\mathrm{d}t} &= \frac{\mathrm{d}B_0 r \sin(\omega t)}{\mathrm{d}t} \\ &= \omega B_0 r \cos(\omega t) \\ \left.\frac{\mathrm{d}B}{\mathrm{d}t}\right|_{\max} &= \omega B_0 r \\ V_{rms} &= \frac{NA\omega B_0 r}{\sqrt{2}}. \end{aligned} \tag{2.4}$$

The value shown in (2.4) is the maximum obtainable RMS voltage from the MSMA device. While there are many non-idealities which may be considered, this result provides an intuitive prediction which relates many known and/or quantifiable parameters to the available output voltage. If the value of the peak induced voltage is desired then the value in (2.4) should be multiplied by $\sqrt{2}$ to obtain the wanted result.

1. Coil

To determine the available power from the flux change of the MSMA material it is necessary to first relate the mechanical parameters to electrical parameters for further optimization. Assuming the coil appears as in fig. 3, we must begin with the standard equation for the resistance of a material.

$$R = \rho \frac{L}{A} \tag{2.5}$$

In (2.5), R is the resistance of the coil material used (copper (Cu) in this case), ρ is the resistivity of the coil material in Ω·m L is the length of the material in m and A is the cross-sectional area in m^2. In a practical situation, and for numerous turns of the coil, it may be difficult to know the exact number of turns obtained

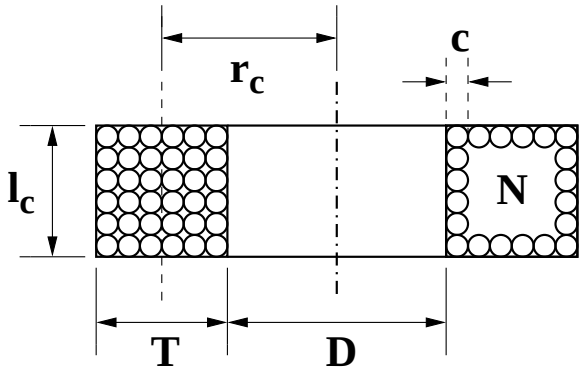

Fig. 3.: Side cross-sectional view of the pick-up coil used with the MSMA material.

by the pickup coil. However, the number of turns may be estimated from readily available physical parameters which can be measured and/or selected when choosing the wire. Figure 3 shows the physical parameters of the coil which may be measured or selected. The parameters are: l_c, the vertical height of the coil; c, the diameter of the copper wire; r_c, the distance from the center of the coil to the center of the winding; D, the inner diameter of the coil (this is where the MSMA material fits); T, the thickness of the winding; and N, the number of turns. Since, for large N, actually counting the number of turns may be difficult and tedious, it may be better to determine an approximate value for these based on measured parameters (l_c, c and T). From (2.5), we know that ρ is a physical parameter of copper and is equal to $1/6\times10^{-7}\Omega\cdot$m. Another way to represent this is by representing this same information as a conductivity (σ) instead of with the wire's resistivity (conductivity is the inverse of resistivity). The value of A in (2.5) may be determined by assuming the copper wire is uniform in diameter and it is a perfect circle giving $A = \pi c^2/4$. Finally, the length of the wire used to wrap around the coil may be estimated by taking a few assumptions: 1) the wire does not extend far from the material itself (i.e., T is small); 2) the coil is wrapped in such a way that there is almost no space between the coil and the MSMA device (i.e., the width of the MSMA is approximately equal to D, the

inner diameter of the coil). Knowing this, we may say that the length of the wire, L in (2.5), is equal to πND. Now, the resistance may be written as

$$R_{coil} = \frac{\pi ND}{\sigma \pi \frac{c^2}{4}} = \frac{4ND}{\sigma c^2}. \tag{2.6}$$

At this point, the majority of the parameters in (2.6) may be measured and/or selected during the initial design of the coil. However, knowing the actual value of N may be challenging for values greater than a few hundred. Therefore, if we assume that there is no space between the coil turns and that they are all aligned in perfect rows and columns, it is possible to estimate the number of turns. The number of rows may may be estimated by l_c/c and the number of columns may be estimated by T/c. Another way to view this is to assume the Cu wire is a square with side length of c. The overall rectangular area of one side of the cross-section of the coil is given by the product of the length and the width, l_c and T. The number of turns may be determined by dividing the overall cross-section area, l_cT, by the cross-sectional area of the wire, c^2. The total number of turns is then estimated as

$$N \approx \frac{l_cT}{c^2}. \tag{2.7}$$

Substituting (2.7) into (2.6) provides us with our desired result as

$$R_{coil} \approx \frac{4l_cTD}{\sigma c^4}. \tag{2.8}$$

Although the frequencies of excitation in mechanical systems are relatively low (when compared to radio frequency (RF) integrated circuits (ICs)), the inductance of the coil may still play an issue in the amount of power which can be extracted from the MEC. Therefore, it is necessary to determine this value based on known physical quantities of the pick-up coil. In [37] and [38] physical parameters of inductors are used to estimate inductance. The author in these papers takes into great account

the different parameters and how they relate to each other and how they will change based on physical dimensions. From these papers it is therefore reasonable to say that the coil inductance is approximately

$$L_{coil} = \frac{\mu\pi N^2 r_c^2}{l_c + 0.9r_c}, \text{ for } l_c > \frac{2}{3}r_c \tag{2.9}$$

where μ is the permeability of the coil material; N, l_c and r_c are the same as previously described. By substituting in our previous approximation for N and taking into account $r_c = T/2 + D/2$ results in

$$L_{coil} = \frac{\mu\pi \left[l_c T \left(D + T\right)\right]^2}{4c^4 \left[l_c + 0.45 \left(D + T\right)\right]}. \tag{2.10}$$

Depending on the volume of the MSMA, the inner dimensions and height of the coil are fixed since the MSMA must fit in the center of the coil and, to maintain as uniform a magnetic field as possible, the coil should not be taller than the MSMA sample [37,38]. Since the equivalent impedance of the coil determines, in conjunction with the equivalent input impedance of the rectifier, the amount of power which may be transferred from the energy harvester to the AC-DC converter the pick-up coil design is crucial.

Assuming the magnetic flux change may be sensed by the coil without any loss, and the time varying magnetic field within the MSMA is $B = B_0 r \sin\left(\omega t\right)$ the output voltage of the coil with no load may be expressed as [22]

$$\hat{V}_{coil} \quad = \quad N A_c \frac{\mathrm{d}B}{\mathrm{d}t} \approx \frac{\pi^2 l_c T D^2 B_0 r f}{2c^2}. \tag{2.11}$$

With the approximated output voltage from the coil known, and assuming the rectifier stage has an input resistance of R_L, it is possible to predict the amount of power delivered to and voltage across R_L as well as determine the overall efficiency

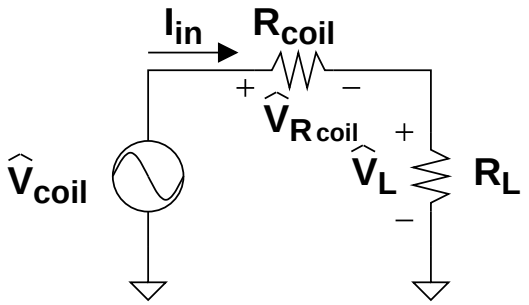

Fig. 4.: Equivalent electrical model of MSMA harvested voltage and coil resistance R_{coil} with rectifier input resistance R_L.

η of the electrical power delivery. Although the efficiency of converting the mechanical vibration into a change in magnetization and thus a voltage is important, this efficiency will be assumed ideal (i.e., 1) and the only efficiency in question will be the conversion of the power delivered from the coil to the input of the rectifier. The resistance of the coil was found in (2.8) and therefore, using voltage division on the equivalent model shown in Fig. 4, the peak load voltage $\hat{V}_L$ may be given as

$$\hat{V}_L = \hat{V}_{coil} \frac{R_L/R_{coil}}{1 + R_L/R_{coil}}. \tag{2.12}$$

In energy harvesting systems, the amount of energy scavenged is typically low and therefore any losses within the system impose limitations on the overall system performance. Therefore, it is necessary to achieve a high power conversion efficiency η so as to not waste the harvested energy while obtaining the required amount of energy for the system. In addition to η, it is also beneficial to study the power delivered P_{load} to the load R_{load} and how this power level effects the peak AC voltage (V_{pk}) across R_L. For maximum power transfer the value of R_L should be set to R_{coil} which is defined by the maximum power transfer theorem. Calling P_{max} the power delivered to R_L when it is equivalent to R_{coil}, the ratio of P_{load}/P_{max} may now be taken into account for the analysis. Therefore, the electrical efficiency η may be defined as the

power delivered to the load R_L divided by the power put into the system. This power, P_{in}, is equal to the power dissipated on R_{coil} plus the power delivered to R_L.

$$\eta = \frac{P_{load}}{P_{in}} = \frac{\hat{V}_L I_{in}}{\hat{V}_L I_{in} + \hat{V}_{R_{coil}} I_{in}} = \frac{R_L/R_{coil}}{1 + R_L/R_{coil}} \tag{2.13}$$

$$\frac{P_{load}}{P_{max}} = \frac{4R_L/R_{coil}}{(1 + R_L/R_{coil})^2} \tag{2.14}$$

One important observation about η is that it is equal to the ratio $\hat{V}_L/\hat{V}_{coil}$. This means the larger the efficiency, the larger the peak voltage which appears across R_L. This is an important observation and will be revisited later when discussing the AC-DC conversion.

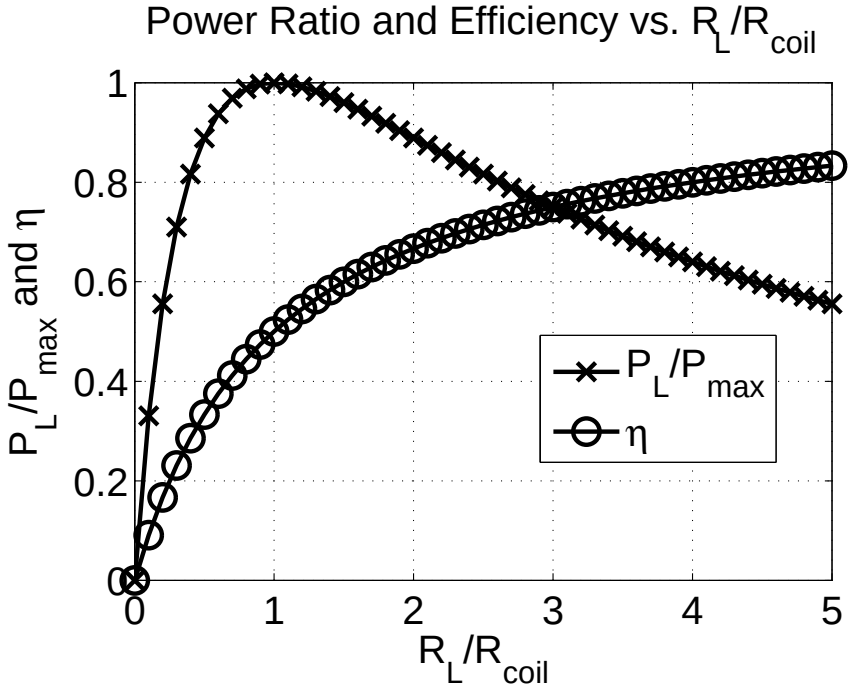

Fig. 5.: Plots of (2.13), η, and (2.14), P_L/P_{max}, versus ratio of load resistance R_L and coil resistance R_{coil} to determine optimum value of RM input resistance and coil resistance to obtain a high efficiency and a reasonable power delivered to the RM.

Since the proposed system does not contain any external batteries and is intended to operate solely on the harvested energy from the MSMA, a method of converting the AC signal from the coil into a DC level is necessary. The value of R_L is a model for the input resistance of a passive rectifier-multiplier (RM) architecture. A single stage RM implemented with diodes and capacitors is shown in Fig. 1 as the stage to which the coil connects. As will be discussed in the following section, obtaining the largest voltage as efficiently as possible while simultaneously producing adequate power for the remaining circuitry is critical. Therefore, rather than being concerned with maximum power, the overall efficiency may be a more critical parameter. To gain an insight, η and the ratio P_{load}/P_{max} are plotted in Fig. 5 as a function of R_L/R_{coil}. It can be shown that these two functions intersect when $R_L/R_{coil} = 3$ which leads to $\eta = 0.75$ and $P_{load}/P_{max} = 0.75$. Conversely, if the system were designed for maximum power, i.e., $R_L/R_{coil} = 1$, leads to $\eta = 0.5$ and $P_{load}/P_{max} = 1$.

As an example, assuming a reasonable value of $\hat{V}_{coil} = 0.3V$ [22] may be obtained from an MSMA sample, with $R_{coil} = 50\Omega$ and $R_L/R_{coil} = 10$, $\hat{V}_L \approx 0.273V$, $\eta = 0.91$, and $P_{load} = 148.76\mu W$. Conversely, if one were to use the value $R_L/R_{coil} = 1$ for maximum power transfer, the values would then be $\hat{V}_L = 0.150V$, $\eta = 0.50$, and $P_{load} = 450\mu W$. Although roughly three times as much power is delivered to R_L in the maximum power case, there is almost half as much voltage swing at the same node. For operating semiconductor devices, which will comprise the RM structure, having a larger voltage swing at the node would be more beneficial than having a larger power. Additionally, although $148.76\mu W$ is not a large power, it is a significant amount and, with proper design, can be enough to power the remaining circuitry as long as the rectifier itself performs an efficient AC-DC conversion. This is because the amount of DC power available to the remaining circuitry is equal to the RMs AC-DC conversion efficiency multiplied by the amount of power delivered to the input

resistance of the RM, which has been modeled by the resistor R_L. So, assuming the case where $R_L/R_{coil} = 10$ to produce a larger input voltage swing to the RM and a RM efficiency of 10%, a power of approximately 15μW will be available for the sensor, ADC, transmitter and any other remaining circuitry. Therefore, low-voltage and low-power circuit design techniques must be employed. These techniques include choosing an appropriate integrated circuit process for circuit design (minimum feature length of devices, threshold voltages, bipolar or CMOS devices, etc.), operating the devices in weak or moderate inversion to save power at the expense of speed, etc. Many of these design choices will be addressed in the following sections.

It is seen from these physical parameters that proper selection of N, wire material, and c, once the MSMA is selected, give degrees of freedom in determining the amount of voltage (and therefore power) which may be harvested. It should be noted that there is a great control on the selection of these parameters as Cu wire is readily available in numerous sizes. So, the coil design as well as the rectifier design may be done concurrently to provide an optimum power harvesting solution.

2. Calculations

We have shown that the induced magnetic flux change stems from the change in applied strain/force/pressure/etc., to the MSMA device. It was also shown that the coil used to extract the electric field change has a significant impact on the available voltage which may be extracted from vibrating the material. The output of the MSMA harvesting device and its associated coil will be connected to an electrical load for further power conditioning and for energy storage. For the time being we will neglect the inductor associated with the coil and only assume a resistive source and load for the MSMA and the following power conditioning circuitry. From here, it can be shown in (2.15) that the available power delivered to the load resistor (R_{load})

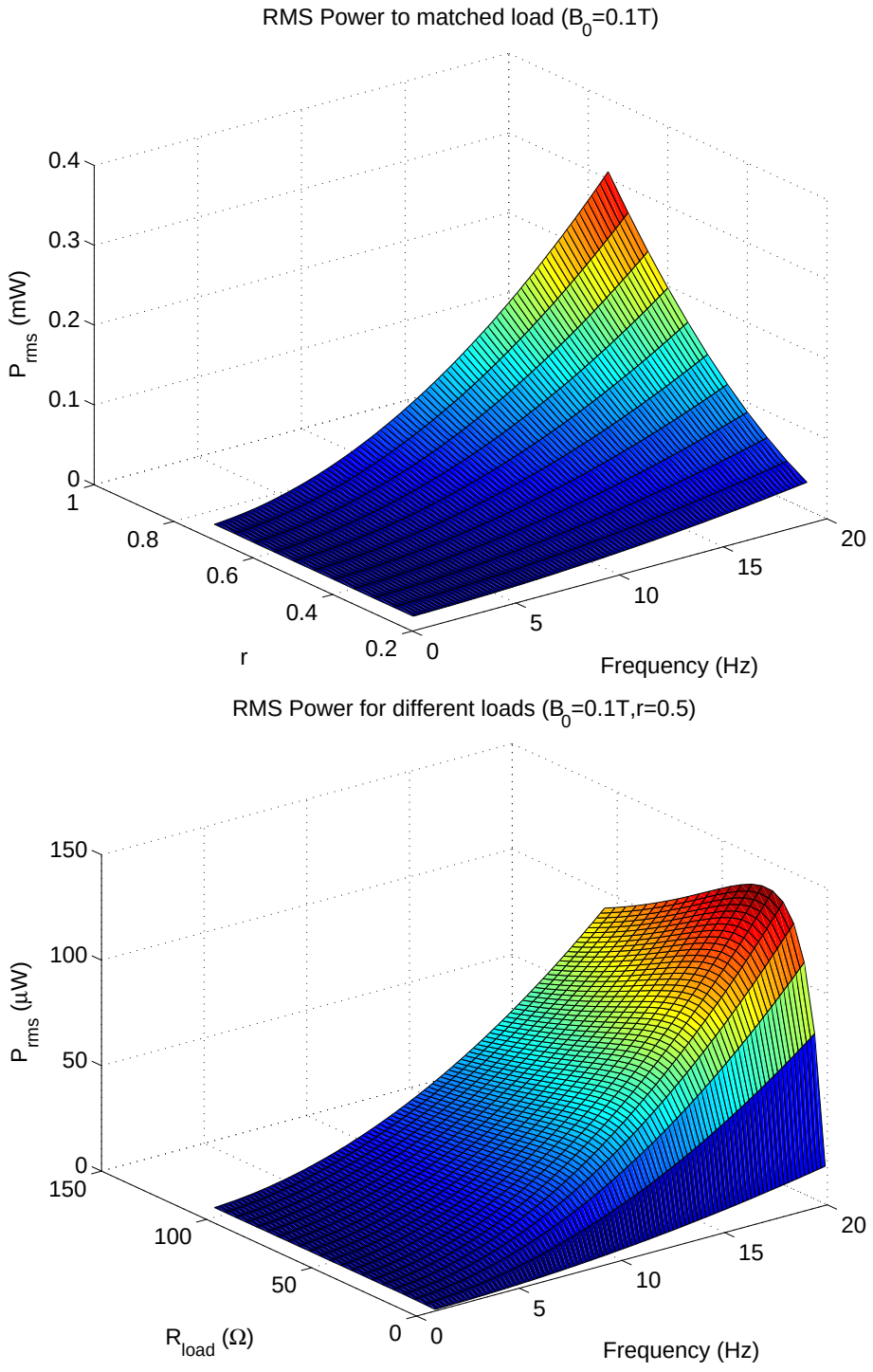

Fig. 6.: Theoretical values of harvested RMS power.

is a function of many design parameters. It is also well known for maximum power transfer that the value of R_{coil} and R_{load} should be set equal. If this is done, we obtain the resulting value of $P_{rms,max}$ as

$$\begin{aligned} P_{rms} &= \frac{V_{rms}^2}{R_{load}} \cdot \frac{1}{\left(1+\frac{R_{coil}}{R_{load}}\right)^2} \\ &= \frac{(\pi D)^4 \left(l_c T B_0 r f\right)^2}{8c^4 R_{load}} \cdot \frac{1}{\left(1+\frac{R_{coil}}{R_{load}}\right)^2} \end{aligned} \tag{2.15}$$

$$P_{rms,max} = \frac{\pi^4 D^3 \sigma l_c T \left(B_0 r f\right)^2}{128}. \tag{2.16}$$

From the previously developed equations for the amount of voltage and power which are available from the MSMA device we are able to see what some readily attainable values are. Figs. 6 and 7 shows the results from a MATLAB simulation where, for low-frequency excitations, there is a significant amount of power which may be harvested. For simulation purposes where R_{coil} and R_{load} are not assumed to be matched, the value estimated from (2.8) is substituted to make the equations a function of simulation parameters or measurable physical parameters. The values used were: $l_c = 4.6$mm; $c = 0.14$mm; $D = 6$mm; $T = 6$mm; $\sigma = 6 \times 10^7$ S $\cdot$ m^{-1}; $B_0 = 0.1$T.

From Figs. 6 and 7 it is seen that from moderate strain levels and frequencies (ones which are typically associated with the natural frequencies of bridges), that power delivered to a matched (and even unmatched loads in some cases) are in excess of 50-100μW. With efficient power conversion circuitry ($> 10\%$), it is possible that this amount of energy/power is sufficient to power a small sensor node. If larger specimens and more turns are used for the coil, it is possible to predict that the power will be increased even further. For the plots in Figs. 6 and 7 it was assumed that the number of turns was fixed to 1000. If the value for N is left in the previous

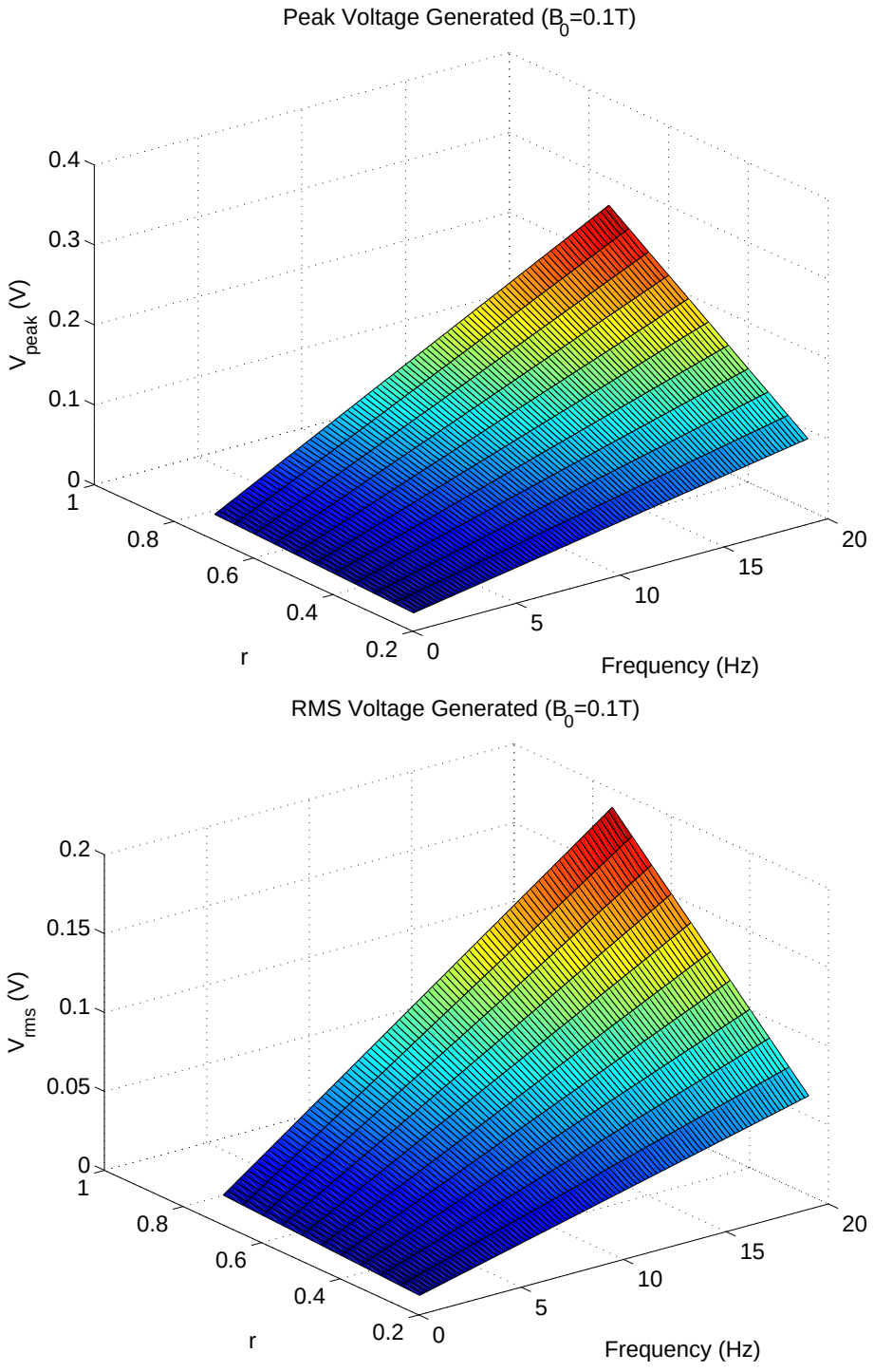

Fig. 7.: Theoretical values of harvested peak and RMS voltages.

equations instead of substituting in the value $N \approx l_c T/c^2$, it is possible to see that there is a direct increase in deliverable power if the turns are increased leaving a great opportunity for power harvesting.

C. NiMnCoIn Measurements

An ingot of $Ni_{45}Mn_{36.5}Co_5In_{13.5}$ (at atomic %) was prepared using vacuum induction melting. Single crystals were grown using the Bridgman technique in a helium atmosphere. They were cut into rectangular prisms with dimensions of 4mm × 4mm × 16mm using wire electro discharge machining. In the austenite high temperature phase, the normal vectors of the prism faces were along the [100], [011], and [01$\bar{1}$] directions.

The single crystalline sample was placed in a bias magnetic field of 1 Tesla where a copper coil with 1000 turns was used to convert the magnetic flux change within the material due to a sinusoidal mechanical excitation, applied along the long axis of the sample. This mechanical excitation led to the transformation of austenite to martensite upon loading and reverse transformation back to austenite upon unloading. The two leads of the copper pick-up coil were then connected to an oscilloscope to monitor the output voltage. The measured coil outputs from the material with 2.5, 5 and 7.5Hz sinusoidal excitations are shown in Fig. 8. As can be seen from the measurements, there is an increased voltage at the output of the coil as the frequency increases. This is as expected since the output voltage V_{coil} of the MSMA sample should be frequency dependent as seen in (2.11). A typical value of the volume fraction of the martensite after transformation,r, is approximately 1.0 for this sample. Assuming the coil has a small width compared to the material, $D + 2T \approx D$, and an ideal magnetic coupling between the material and the coil, the predicted output voltages at 2.5, 5 and 7.5Hz are approximately 20mV, 40mV and 60mV, respectively,

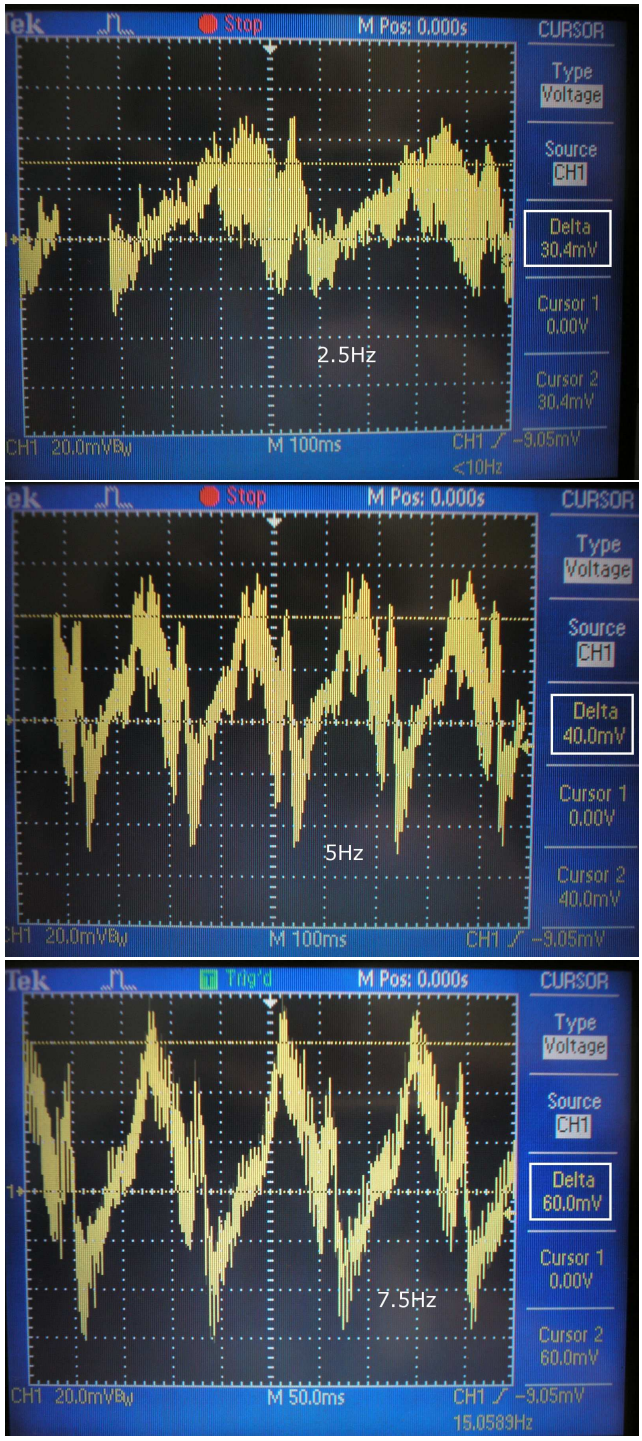

Fig. 8.: Measured MSMA output voltage of the energy harvesting sample at three different frequencies of sinusoidal mechanical excitation: 2.5, 5, and 7.5Hz.

for $r = 1$. These values closely match the measured values of 30mV, 40mV, and 60mV.

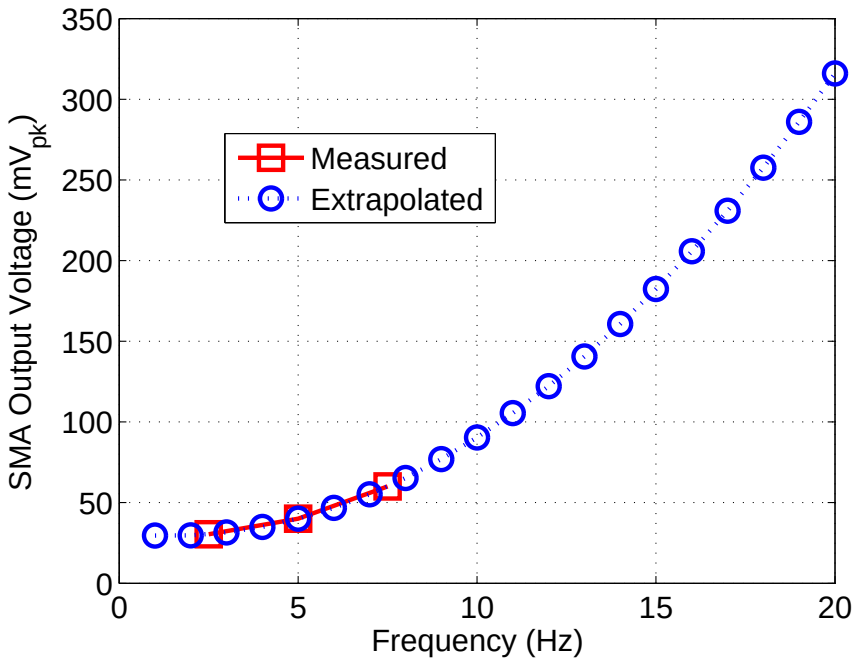

Fig. 9.: Extrapolated MSMA output voltage vs. frequency.

Although these results are promising, it is necessary to produce larger output voltages from the MSMA material. One method of doing this would be to increase the number of turns on the coil N. Assuming the material can withstand higher loading frequencies (>10Hz), it could also be possible to obtain larger output voltages from the coil under slightly higher loading frequencies as shown in Fig. 9 where the measured data was extrapolated using a second order curve fit. Unfortunately, the response of NiMnCoIn MSMAs under relatively high loading frequencies and high cycle numbers is not known and further studies are needed. However, since NiMnGa MSMAs can survive loading cycles up to 10^8 cycles [39], NiMnCoIn MSMAs are also expected to show similar cyclic resistance and survive under high loading frequencies

on the order of tens of Hz.

CHAPTER III

DC POWER GENERATION[1]

An overview of the proposed SHM system was shown in chapter 1 and measurement results and an electrical output model were shown for an MSMA energy harvester in chapter 2. Due to the time-varying excitation of the MSMA harvester, the voltage output of the pick-up coil is also time-varying. In order to power the remaining circuitry in the proposed SHM system, it is necessary to convert this signal into a usable DC voltage. As shown in Fig. 9, the extrapolated output of the MSMA harvester at an excitation frequency of 20Hz is approximately 320mV_{pk}. Assuming the number of turns increases from 1000 to 3000, this means approximately 1V_{pk} output voltage is possible at this frequency. However, the main challenge lies in converting this low-frequency signal into a DC voltage.

In this chapter a self-powered rectifier (SPR) is proposed for low-frequency (≈20Hz) energy harvesting applications in embedded structural health monitoring (SHM) of bridges where the output voltage from the energy harvester is less than 1V_{pk}. To help overcome the low input amplitudes, the circuit utilizes a low-voltage clocked comparator to provide the gate drive to the switches to help reduce their ON resistance and speed up the comparison process which aides in the overall rectifica-

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tion. The low-voltage comparator is solely powered by the generated DC output of the rectification circuitry, thus eliminating the need for an external battery (specifically Li-ion or other rechargeable batteries) whose lifetime is typically less than that of the structure being monitored. The clock signal for the comparator is generated from the input signal of the rectifier and a clock doubler is used to increase the voltage swing of the clock signals within the comparator to reduce switch ON resistance which reduces comparator latency and improves the overall rectification efficiency (voltage and power).

A. Background

The use of rectifiers for energy harvesting applications is necessary because the mechanical excitation of the system is often a time varying signal and must be converted into a DC signal to power the remaining circuitry. Standard rectification techniques are not always plausible for a few reasons. First, the electrical output of the mechanical-to-electrical converter (MEC) may not be large in amplitude and must be amplified to overcome inherent limitations of the diodes. Usually the largest limitation present in the rectifying diodes is the forward voltage drop associated with the diode itself which limits the achievable output voltage. Secondly, to help avoid the voltage drop of standard diodes, Schottky diodes are often employed to provide a forward voltage drop in the order of 200-300mV [40, 41]. However, in integrated circuit solutions, employing Schottky diodes is not always possible due to process or cost limitations. Therefore, often times external batteries are used to power circuitry to help reduce the conduction losses of diodes by powering switches or other circuits and using the rectifier to recharge the battery when possible [42–44]. However, using batteries is usually not desired since these add cost to the overall system, access to the

sensor locations may be hindered or unavailable, the limited rechargeable life cycle of the battery is less than the sensor and the structure in need of monitoring, and they defeat the main purpose of energy harvesting which is to have a system that utilizes available energy to power the circuitry [45–47]. Regardless of the system, the need for an energy storage element is necessary and viable alternatives exist, such as supercapacitors, that have longer life cycles than batteries [45–47].

B. Energy Harvesting

Although large levels of energy may be scavenged from solar panels and thermo-electric converters, these devices are not able to work properly in all locations due to their need for direct access to sunlight and larger temperatures (or temperature gradients), respectively. However, vibration energy is available in more structures than solar and thermal energy due to wind, vehicles, moving parts, etc. In order to provide a broader application base for the proposed SPR, vibration energy harvesting is assumed.

In these applications, devices exhibiting the piezoelectric effect can be employed to extract energy to power additional circuitry [48, 49]. While these materials can provide usable output powers with output levels on the order of 2V DC, the materials themselves usually suffer from having a capacitive input impedance and are constructed using a brittle material [49]. The magnitude of a capacitor's impedance may be expressed as

$$|Z_c| = \frac{1}{2\pi f C} \tag{3.1}$$

where f is the frequency of interest and C is the equivalent input capacitance of the piezoelectric material. If f is 20Hz and an equivalent impedance of 100Ω is desired this necessitates an effective equivalent capacitor of approximately 80μF. This value

is three orders of magnitude larger than the equivalent capacitance of some known piezoelectric energy harvesters [49] and may be difficult to reliably construct. Conversely, if the capacitance is set to the value obtained in [49] of approximately 33nF, at a 20Hz excitation frequency this results in an equivalent impedance of approximately 240kΩ. This relatively large impedance implies the rectifier's input impedance must also be relatively large in order to obtain a maximum, or near maximum, power transfer. To help mitigate the issues from the equivalent impedance, the input frequency of these devices is generally required to be larger than a few hundred Hz in order to reduce the equivalent impedance to allow for a larger power transfer and, therefore, a larger efficiency [48]. The fragility of the device is dependent on material selection and manufacturing, but these devices still may break easily when placed in harsh environments or when large forces are applied as in bridge or road applications.

It has been shown that depending on the material used (piezoelectric, shape memory alloys (SMAs), etc.) and the excitation frequency, the DC voltages obtained from a MEC are in the range of 50-400mV [49, 50]. While piezoelectric devices have been shown to work well at producing larger voltages than SMAs [49], they typically require an excitation frequency in the kHz range to overcome their highly capacitive input impedance. However, this frequency is much larger than the typical bridge natural frequency of 10-20Hz [7], making piezoelectric devices unsuited for these applications. For low frequency vibrations, an energy scavenging material whose output impedance is inductive and/or resistive in nature may help mitigate impedance matching difficulties and promote an improved power transfer compared to piezoelectric devices. Magnetic shape memory alloys (MSMAs) are a viable alternative to piezoelectric materials and are well-suited for low frequency energy harvesting applications [50]. They provide an output impedance that can be modeled as a series combination of a resistor and inductor whose values depend on geometry and material choice.

C. Previous Work

In the early 1900s, physicists were studying the atom and needed a way to generate large electric fields to assist with particle acceleration [51–53]. Since the 1800s, it was well-known that the use of two coils in close spatial proximity (called a transformer) could produce a larger voltage amplitude on the secondary winding of the coupled coils, provided the number of turns on the secondary was greater than the number of turns on the primary. However, for the extremely large fields required by particle accelerators, using coils would prove to be inefficient and nearly impossible due to the large volume of space required. Therefore, a need developed for implementing a "transformer-like" result without using coils. It was at this time inductorless

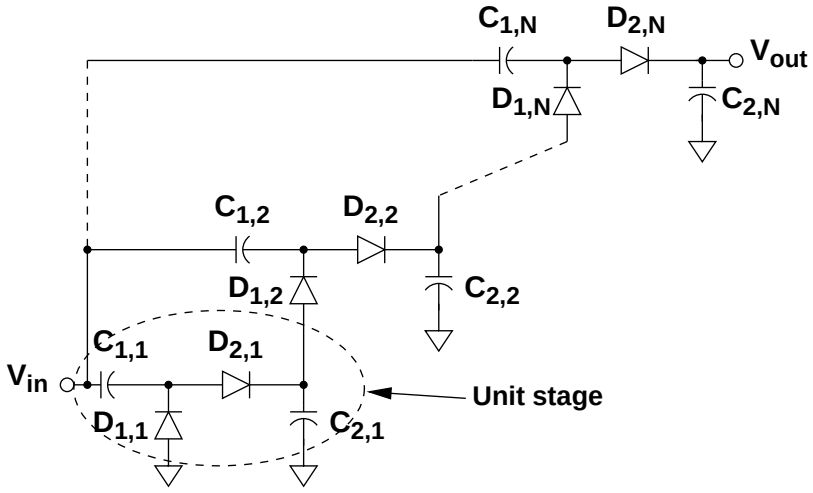

Fig. 10.: Greinacher/Cockroft-Walton N-stage inductorless transformer.

transformers were invented separately by Greinacher and the team of Cockroft and Walton. A basic figure of the Greinacher/Cockroft-Walton inductorless transformer is shown in Fig. 10 which utilizes cascaded stages of diodes and capacitors to generate a larger DC output voltage than the amplitude of the input signal. This circuit is

also known as a rectifier-multiplier (RM).

After the invention of the integrated circuit, researchers began to miniaturize active and passive components to help reduce the overall cost of a chip. Around this time, computers began to take on more tasks and perform more efficiently than they had previously when circuits were based on vacuum tubes and/or discrete components. In electronic systems, there are applications and scenarios which develop within the same system where different functions require different supply voltages. However, it is impractical to use different power supply connections for every level change because this will ultimately create issues with cost and functionality of the end system. Instead, it became necessary to generate these different voltages off of a reduced number of supplies without greatly reducing the overall power efficiency. In the 1970s Dickson [54] modified the original architecture proposed by Greinacher/Cockroft-Walton by using anti-phase clocks to effectively 'pump charge' from one capacitor to another to double a DC voltage. At this time many new applications began to take form where on-chip supply generation was required. Some of these include: Dynamic Random Access Memory (DRAM), cellular telephones, data converters, etc.

Although batteries have the ability to provide a sufficient amount of energy to cell phones, toys, and sensors, they need to be recharged and/or replaced more frequently than one desires. For a sensor network, even when using advanced low-power design techniques, it may be necessary to replace the batteries in wireless sensors fairly often ($\approx$ 1-5 years). Although the necessity to replace or recharge batteries is the main drawback of wireless sensors, it is still more cost-efficient and plausible than wired networks due to limits on accessibility and overall functionality.

1. Rectifier Multiplier

The RM promoted by Greinacher/Cockroft-Walton is one of, if not the most used topology for passively increasing the output voltage of an integrated AC-DC converter. Its operation is best understood if a single stage is viewed as a combination of two sub-stages. Capacitor C_1 and diode D_1 are a stage which are used as an input voltage sampler/level-shifter. Capacitor C_2 and diode D_2 together comprise a peak detector with an output filter. If the input to the rectifier-multiplier is assumed to be sinusoidal with a zero average (i.e., no DC component) and an ideal diode (no forward drop) is assumed, when the input signal is in its negative half cycle the diode D_1 will be forward biased (ON) and D_2 will be reverse biased (OFF). The amount of charge that is stored on C_1 is then equal to

$$Q_{in} = C_1 V_{in}. \tag{3.2}$$

An alternative way of stating this is that the voltage drop across C_1 will then be equal to

$$V_{C_1} = V_{in} = \frac{Q_{in}}{C_1}. \tag{3.3}$$

However, since the input signal is actually lower than ground the polarity of the voltage across C_1 is such that the positive terminal is at the node where C_1, D_1, and D_2 are connected. As the signal becomes positive, the voltage drop across the capacitor remains constant (equal to the magnitude of the input voltage) and thus causes D_1 to become reverse biased while simultaneously forward biasing D_1. Then, as the input voltage increases further, the voltage across C_2 becomes $2V_{in}$.

Although this is an idealized version of the operation of the rectifier-multiplier, it gives the maximum potential which may be obtained from this architecture. In actuality, during each cycle, the diode drops will each reduce the amount of voltage

which may be built up across the capacitors. If the diode drop, V_d, is taken into consideration the equation for the output voltage may now be written as

$$V_{out} = 2\left(V_{in} - V_d\right). \tag{3.4}$$

In the event that the voltage level obtained from a single stage is not enough, there are three ways to increase the output voltage with the Greinacher architecture.

1. Increase the input amplitude.
    - Easiest method.
    - May not be possible depending on the system.
2. Cascade multiple stages.
    - Simple method and good option if area is not an issue.
    - Can cause issues due to variations in diode drops limiting obtainable voltages.
    - Can reduce power conversion efficiency if not designed properly.
    - Output voltage becomes $2N\left(V_{in} - V_d\right)$, where N is the number of cascaded rectifier stages.
3. Reduce or eliminate the diode voltage drop.
    - Standard diodes cannot be used, Schottky diodes can be used instead.
    - Native V_{th} MOSFETs can be used in diode configuration.
    - Other V_{th} cancellation techniques can be used to improve efficiency.
    - If input voltage is limited and/or area is not an issue, has promising potential.

- Typically requires advanced techniques, clocks, periodic charging/discharging of capacitors, etc.

In the event that the input voltage can be increased and depending on the relative levels of the amplitude and the diode losses, other methods of increasing the output voltage may not be necessary. For example, if the diode drop is 0.4V and the input amplitude is equal to 3V, the predicted output voltage for a single stage will be equal to

$$V_{out} = 2(3 - 0.4) = 5.2\,\text{V}. \tag{3.5}$$

For CMOS processes at 0.5μm and below, this is more than enough voltage to power circuitry, even after regulation. However, in many applications, the input amplitude may be limited to a value that is significantly lower than 3V and therefore multiple stage rectifiers, or diode voltage drop cancellation techniques must be implemented to increase the output voltage.

D. CMOS Rectifiers

1. Standard and Schottky Diode Rectifiers

Figure 11(a) shows the basic architecture of a single step-up stage in the inductorless transformer (also called a rectifier-multiplier, RM). The first part of the circuit consists of capacitor C_1 and diode D_1. Assuming a sine wave input equal to $V_{in} = \hat{V}_{in}\cos(2\pi ft)$, this circuit samples the incoming input signal during the negative half cycle and stores this peak voltage on capacitor C_1. During the positive half cycle of the input signal, diode D_2 and capacitor C_2 form a rectifier circuit which will produce a DC voltage across C_2 equal to $2\hat{V}_{in}$. While this is a simplified description of this circuit's operation, it provides insight into how this circuit should work. If

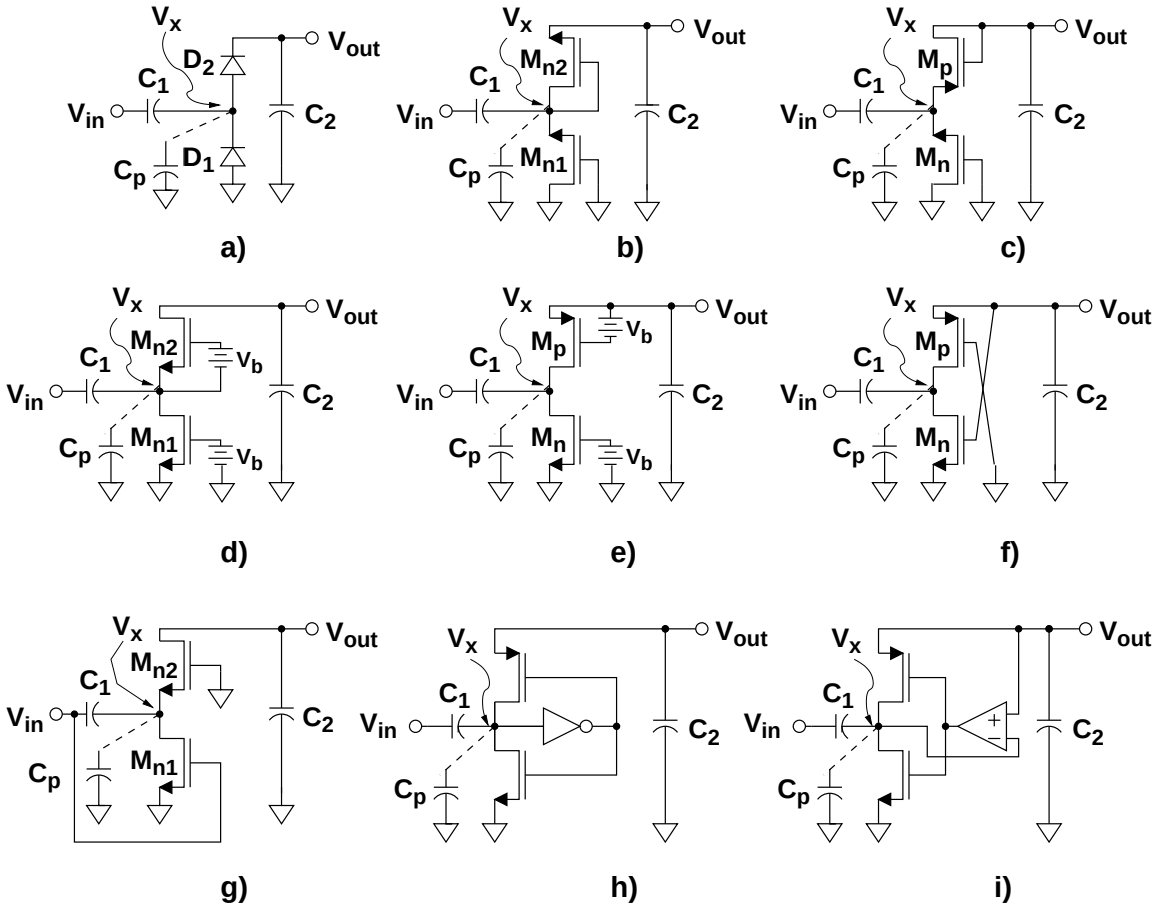

Fig. 11.: Different rectifier architectures with: a) diodes, b) NMOS, c) CMOS, d) EVC, e) IVC, f) SVC, g) bootstrapped, h) inverter-based, i) comparator-based.

the diode voltage drops are taken into account during the analysis and assumed to be constant and equal, this results in an expression of the output DC level of

$$V_{out} = 2\hat{V}_{in} - 2V_d. \tag{3.6}$$

The value of V_d in these cases can range from approximately 200mV for Schottky diodes and may go up to 700mV for standard diodes. As can be seen from (3.6), minimizing the diode voltage drop would increase the achievable output voltage for a single stage RM.

2. MOS Diode Rectifiers

Although Schottky diodes are a viable solution, they are often not available in standard CMOS processes or cost additional mask layers. Instead, one may use the circuits in Figs. 11(b) and (c) as a replacement for the standard diodes. These architectures utilize diode-connected transistors to mimic the operation of a standard diode. The DC output voltage which may be obtained from these circuits can be written as

$$V_{out} = 2\hat{V}_{in} - 2V_{th}, \tag{3.7}$$

where V_{th} is the threshold voltage of the MOS devices. The main difference between Figs. 11(b) and (c) is that the NMOS-only architecture suffers from the body effect whereas the CMOS architecture does not. Depending on the level of the input signal and the selected process, this body effect can produce a large loss in the overall conversion. In order to overcome the lower hole mobility in PMOS devices compared to the electron mobility in NMOS devices, larger PMOS structures are often employed. This increase in device size directly increases the parasitic capacitance C_p. Since the output voltage is directly related to the voltage swing at this node (V_x), it is imperative to keep parasitics at a minimum. If all parasitics at this node are considered to be lumped into a grounded capacitor C_p, the AC voltage at V_x is

$$V_x = V_{in}\frac{C_1}{C_1 + C_p}. \tag{3.8}$$

3. Efficiency Enhancement Techniques

In many cases, especially in energy harvesting applications and RFID, the input levels to the rectifier may not be large and are typically in the range of 100mV-1V. Therefore, the attainable DC voltage will not be very large using standard or MOS diodes. Instead, the threshold voltage, or loss, of the MOS diodes can be reduced in

a few ways. Zero-V_{th} devices may be employed [55] at the cost of extra mask layers and at the risk of ±100mV shift in the threshold voltage [56]. Instead, additional circuitry can be added to effectively lower the threshold voltage. Figs. 11(d) and (e) show two methods of doing this. The circuit in Fig. 11(d) was reported in [56] and is known as an External V_{th} Cancellation (EVC) rectifier. The name stems from the use of external components to provide the gate bias to the NMOS diodes, which is the main drawback of this architecture. In [57, 58] the authors use matched PMOS and NMOS devices and an RC sampling network to generate a DC voltage proportional to the input signal and the output DC voltage. This type of network is known as an Internal V_{th} Cancellation (IVC) rectifier and requires the use of fairly large valued resistors and good device matching to achieve the required battery voltage. This new voltage V_b is then applied across the gates of the MOS devices to effectively reduce the threshold voltage, and thus the loss of the diodes. For these systems the generated output voltage for a single stage may be expressed as

$$V_{out} = 2\hat{V}_x - V_{drop} + V_b. \tag{3.9}$$

In addition to the EVC and IVC structures, some attention has been paid to reducing the threshold voltage of the MOS devices without adding additional circuitry. One method of doing this has been reported in [59, 60]. This structure is known as the Self V_{th} Cancellation (SVC) architecture and is depicted in Fig. 11(f). This structure utilizes the DC output voltage to lower the effective V_{th} of the NMOS and PMOS devices by increasing the gate-source and source-gate voltages. Under these conditions the MOS devices behave more like voltage controlled-switches than diodes. Depending on the technology used as well as input and loading conditions, the SVC structure has shown it is capable of producing DC output levels greater than 1V for 400mV$_{\text{pk}}$ input amplitudes [59–61]. However, since there is no way to control the

voltage at the gates of the MOS devices, the efficiency of this architecture begins degrading once the input amplitude exceeds the V_{th} of the devices.

The EVC and IVC architectures add circuitry to help reduce the effective threshold voltage and improve the overall conversion efficiency. Floating gates have also been used to effectively reduce the effective threshold voltage in CMOS rectifiers [24,62–64]. The main drawback of using these structures is the necessity to occasionally reprogram the threshold voltage via the floating gate pin. A solution to this issue has been reported in [65] and is shown in Fig. 11(g).

As a solution to the efficiency degradation due to the static gate biasing in the SVC structure, the circuit shown in Fig. 12 has been proposed [61,64,66–70] along with efficiency enhanced versions of this circuit [71] and a complementary bipolar version of this circuit [72]. This structure is known as a High Efficiency Differential Drive

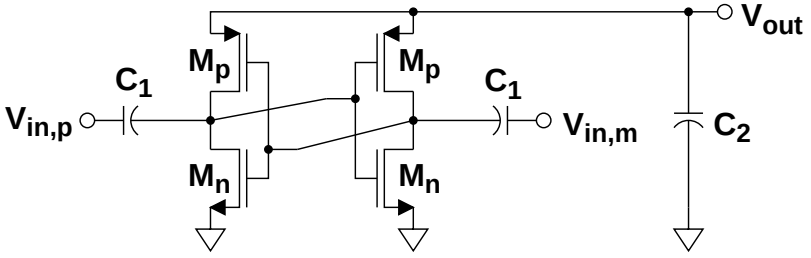

Fig. 12.: Self-driven rectifier (Four Transistor Cell/Differential Drive Rectifier/Negative Voltage Converter).

Rectifier (DDR), a Negative Voltage Converter (NVC), a Four Transistor Cell (4TC), and a Differential Self V_{th} Cancellation Rectifier (DSVC) among other names. Much like the SVC structure, the DSVC structure operates the MOS devices as switches instead of diodes. However, the gate voltages of the devices are dynamically biased by the differential AC voltage which helps reduce the unwanted reverse conduction

as the input level increases and the effective drain-source voltage is reduced [59, 60]. The output of this voltage is thus

$$V_{out} = 2\hat{V}_x - V_{ds,n} - |V_{ds,p}| \,. \tag{3.10}$$

One of the main drawbacks to this architecture is the necessity to have a differential source referenced to the same ground as the rectifier and load. Although this is often the case, it may not be possible to obtain a differential signal in every situation.

In the DSVC architecture, the efficiency is degraded by reverse conduction as the magnitude of the drain-source voltage of the devices increases. Additionally, these circuits require a differential source to drive the circuit. To help mitigate these issues the circuits shown in Figs. 11(h) and (i) may be implemented. The configuration in Fig. 11(h) [73] creates a dynamic gate bias by applying an inverter to the gates of the switches. This effectively generates the required differential drive as in the DSVC architecture without the requirement of a differential source voltage. This circuit, however, has an efficiency reduction due to the finite gain of the inverter, the propagation delay which leads to unwanted conduction, and the fact that the inverter only makes a decision based on the voltage at V_x without considering its relative voltage compared to V_{out}. When V_x is large enough to make the inverter's output go low, the gate of the PMOS switch is at ground. This means V_x is larger than the inverter decision level but the output level is greater than V_x for a finite amount of time. This means some charge is lost due to reverse conduction which will degrade the efficiency. To mitigate this issue, the architecture shown in Fig.11(i) may be implemented [74]. This circuit is a self-driven rectifier which is able to dynamically adapt the gate voltages to help improve the overall efficiency due to the decrease in reverse conduction losses. A comparator is placed to perform the same general operation as the inverter, however it makes a "smart" decision of when to move the

gate connection. Instead of just waiting for the voltage at V_x to be larger than the threshold of the inverter, it waits until $V_x > V_o$ to switch. This way, the finite time when $V_x < V_o$ and the output of the inverter is low allowing charge to flow from the output may be eliminated. The main challenge with this approach is designing a low voltage comparator which operates with very low static power. The authors in [74] use a current-mode approach and utilize current mirrors and a differential pair as a comparator.

E. Proposed Self-powered Rectifier

1. Motivation

In recent years, research has been reported for low frequency vibrational energy harvesting applications using piezoelectric materials as an input source for the system [75–77]. The authors use a comparator-based rectifier modified from the topology presented in [78] to convert the low frequency output voltage from the piezo device into a DC voltage and then, using a system to track the maximum power point, they use a buck converter to drive a load at a specified DC voltage. Additionally, the comparators are implemented to minimize reverse conduction losses and improve the power conversion efficiency (PCE) of the rectifier and are comprised of devices designed to operate in the subthreshold region. For a low power solution, this region of operation is the most power efficient and the authors of [78] report a DC power consumption of 120-390nW for their comparator. This value is dependent on the output voltage of the rectifier which ranges from 2-6.5V. While the work presented in [75, 76] produces efficiencies on the order of 90% with output powers near 100μW, the applied input voltage to the rectifier is not stated since the focus of the work is on a complete energy harvesting system. However, the circuit in [78] is shown to require

a minimum operating input voltage of $1.5V_{pk}$. In many energy harvesting applications amplitudes of this magnitude may not be available [50]. The authors in [79] also implement a similar rectifier topology as the one presented in [78]. Measured results for the proposed rectifier chip show PCEs greater than 80% with load resistances on the order of a couple kΩ.

As previously stated, input amplitudes larger than 1V may not be available in all energy harvesting applications due to limited light, vibrational energy, heat, device limitations, etc. Therefore, there is a necessity to develop AC-DC conversion units with turn-on voltages below 1V that are still able to generate usable amounts of DC power. The following section will discuss some design considerations for a low frequency rectifier for vibrational energy harvesting applications. For the proposed design, the input amplitude to the rectifier is assumed to be less than 1V at a frequency of 20Hz to emulate harvestable low frequency vibrational energy [50]. The intended application for the proposed rectifier is embedded structural health monitoring of bridges.

2. Basic Architecture

In the event an ideal comparator can be implemented, the circuit shown in Fig. 11(i) is one of the most viable options for providing a highly efficient rectifier while producing a large output voltage. This is because the comparator is able to intelligently select appropriate times to turn on and turn off the MOS switches and transfer charge to the output based on the relative voltages between V_x, V_{out} and GND . Although threshold voltage cancellation, in theory, is the best option, practically it becomes an issue due to the reverse conduction and leakage currents of the MOS devices. In other words, having a V_{th} on the order of a few hundred mV works as a built-in safe guard to inhibit reverse conduction and promote a more efficient rectifier. However,

having V_{th} be too large, on the order of 700mV or higher, necessitates a larger input signal to continually charge the output capacitor and lower the ON resistance of the rectifier switches [64]. Therefore, a smart switch that opens and closes at appropriate

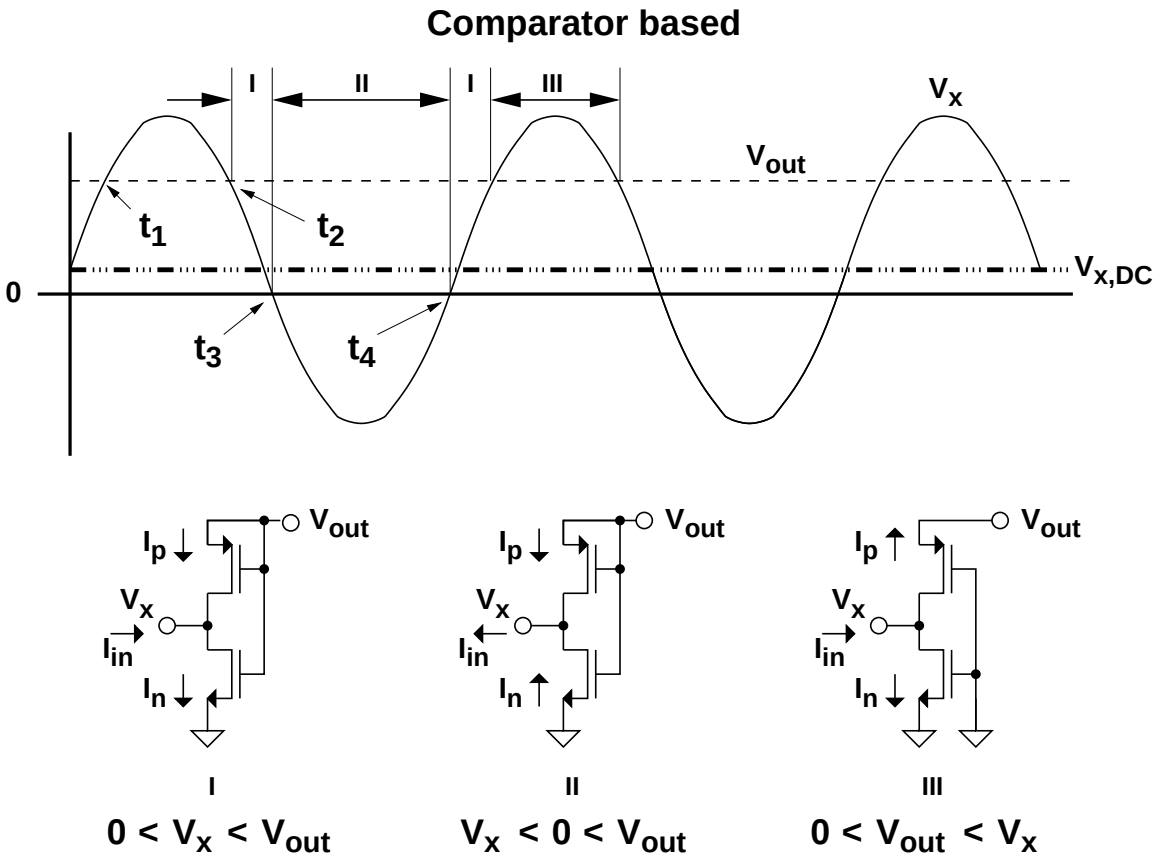

Fig. 13.: Principle of operation of an ideal comparator based rectifier.

instances could potentially be a better option for efficiency enhancement rather than developing a scheme based on canceling V_{th}. Assuming an ideal comparator can be used in the circuit in Fig. 11(i), the different waveforms related to the circuit and the effective circuit configurations of the comparator-based RM are shown in Fig. 13. Although this gives an idealized version of the circuit's operation, it is apparent that an ideal comparison is a more optimum solution than using a single inverter to drive

the rectifier switches.

Comparator-based rectifiers have been proposed previously [74] but they depend on static power consumption and typical comparator operation to achieve an improved performance. It has been shown that switched-capacitor devices are more accurate for low frequency applications. Additionally, for speed purposes and voltage headroom limitations as in energy harvesting applications, limiting the number of stacked devices can be very beneficial to the overall system's performance. Therefore, inverters are an ideal candidate as amplifiers within the comparator due to their low headroom requirements. However, since a comparison is required, switched capacitors may be employed to, during different clock phases, sample the appropriate voltages and allow the comparator to make a decision and optimally switch the rectifier switches.

Additionally, since this rectifier is to be employed as a low frequency rectifier with the ability to optimize the source impedance [50], reasonable off-chip capacitors may be employed to optimize the design of the entire system simultaneously while achieving the desired output levels. As such, Fig. 14 shows the proposed SPR where all of the main rectification circuitry and the supporting devices are powered by the output of the rectifier. The comparator in this architecture is implemented by a cascade of three inverter stages for amplification, transmission gates for biasing the inverter inputs at their toggle point for maximum gain and for storing the voltage difference on a capacitor prior to amplification, and a clock doubler to increase the voltage amplitude of the switches which minimizes the ON resistance of the transmission gates and increases the speed of the decision [80]. This is important because the latency of the comparison directly effects the efficiency of the rectifier.

Since a comparison must be completed in one half clock cycle (half of the rectifier

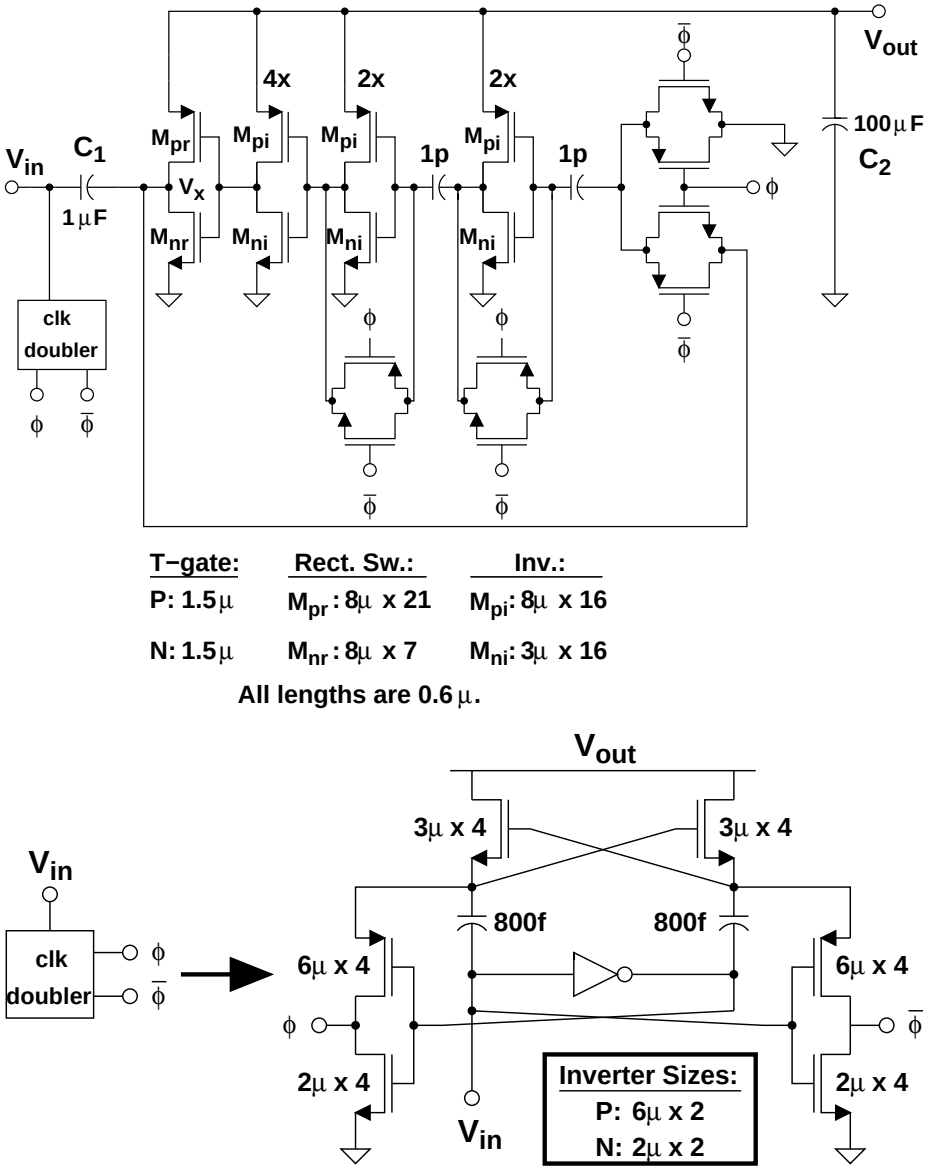

Fig. 14.: Proposed SPR with comparator (top) and detailed view of the clock doubler (bottom).

input period), this sets a limit for the maximum latency:

$$\tau_{comp} \leq \alpha \left(t_2 - t_1\right) \tag{3.11}$$

where τ_{comp} is the time required for the comparator to transition its output based on a change in input conditions, α is the fraction of the conduction period required for the comparator to make a decision, t_1 is the time instance when V_x becomes larger than V_{out} and t_2 is the time instance when V_x becomes less than V_{out}. At these instances, assuming there is a DC level at node X we may write

$$t_1 = \frac{T}{2\pi} \sin^{-1}\left(\frac{V_{out} - V_{x,DC}}{\hat{V}_x}\right) \tag{3.12}$$

$$t_2 = \frac{T}{2} - t_1 \tag{3.13}$$

$$\begin{aligned} \Delta t &= t_2 - t_1 \\ &= \frac{T}{2}\left[1 - \frac{2}{\pi}\sin^{-1}\left(\frac{V_{out} - V_{x,DC}}{\hat{V}_x}\right)\right] \end{aligned} \tag{3.14}$$

where T is the period of the input signal V_x, Δt is the portion of T where the comparator output is low and thus V_x is connected to the DC output voltage V_{out}, $V_{x,DC}$ is the DC voltage at node X, and V_a is the amplitude of V_x. These results are important because it provides some insight into the rectifier operation. In an ideal RM architecture where all devices match perfectly and there are no losses we have $V_{x,DC} = V_{out}/2 = \hat{V}_x$ which implies $t_2 = t_1$ and the output voltage remains at the largest possible value implying the comparator output does not toggle. It is apparent that due to any loading or leakages within the system (as in $t_2 < t < t_1 + T$), the value of t_1 will be closer to the start of the period and t_2 will be closer to $T/2$. For the system to be able to deliver the maximum amount of charge to the load the comparator must make a decision in a small fraction of the time when $V_x > V_{out}$. Therefore, assuming α is the fraction of time where $V_x > V_{out}$ and is assumed to

always be less than 1, we may say

$$\tau_{comp} \leq \frac{\alpha T}{2}\left[1 - \frac{2}{\pi}\sin^{-1}\left(\frac{V_{out} - V_{x,DC}}{\hat{V}_x}\right)\right]. \tag{3.15}$$

Ideally the value of V_{out} will be $2\hat{V}_x$ and the value of $V_{x,DC}$ is $\hat{V}_x$. Substituting these values into the previous expression for τ_{comp} results in the argument of the arcsine becoming 1. This implies $t_2 = t_1$ and the output of the comparator will never change. However, the output will not reach this ideal value due to leakages, losses in the switches, and any static current dissipation. Additionally, due to parasitics at node X and mismatches between the PMOS and NMOS devices the value of $V_{x,DC}$ will not reach $V_{out}/2$ (i.e., the ideal value of $\hat{V}_x$).

Without assuming ideal voltage levels, or perfect matching between the PMOS and NMOS switches, the value of V_b will be a DC value that is a fraction of the input amplitude which will be denoted as $\beta\hat{V}_x$. Also, the output voltage will be less than the ideal value of $2\hat{V}_x$ and will be denoted as $\kappa\hat{V}_x$. If these values are substituted into the equation for the maximum comparator latency one obtains

$$\tau_{comp} \leq \frac{\alpha T}{2}\left[1 - \frac{2}{\pi}\sin^{-1}(\kappa - \beta)\right] \tag{3.16}$$

where $\kappa \geq \beta$. As κ and β become equal, this implies the value of τ_{comp} approaches $T/2$ and the comparator will conduct for a longer period of time. The increased PMOS conduction mainly occurs during two situations: (1) when the loading of the rectifier is too large for the circuit to supply enough charge to keep the output relatively constant; and (2) when the output voltage is low due to a low input voltage amplitude or at initial start-up and an input amplitude larger than a few hundred millivolts.

The low-voltage comparator shown in Fig. 14 is used to apply a large amplification and a quick decision to the gates of the rectifier switches. The chain of inverters

acts as an amplifier that senses the difference between V_x and the output voltage V_{out} and switches ON and OFF the NMOS and PMOS devices [80], accordingly. If the voltage at V_x is larger than GND, the comparator output is low and the PMOS gate is connected to ground while the gate of the NMOS device is connected to its source. Therefore, the charge injected from the source will mainly be conducted by the PMOS device and will be delivered to C_2 which will then give rise to an increase in output voltage. At the same time, the current that the NMOS device conducts will be equal to its leakage current which may be given by

$$I_{leak} \approx I_0 \left(1 - e^{-V_x/\phi_t}\right) \tag{3.17}$$

where I_0 is a process and design dependent value proportional to the W/L and V_{th} of the device. When V_x is lower than GND, the comparator output goes high and pulls the gates of the MOS devices high. At this point, the drain and source terminals of the devices change places and the PMOS device now only conducts leakage current while the NMOS device conducts the majority of the current provided by the source. The transmission gates in the proposed design are used to set the input and output nodes of the inverters to their toggle point before the compare decision is made. Setting the inverters to their toggle point allows them to have the maximum amount of available gain prior to making a decision, thus the largest amplification and a faster switching time is obtained compared to a single inverter stage [80]. This process is vital for the efficiency enhancement since any delay or ON overlap of the main rectifier switches causes an overall efficiency degradation.

To assist in the efficiency enhancement, a differential clock doubler is employed to drive the transmission gates [81]. The increased drive reduces the ON resistance of the transmission gates and helps in minimizing conduction losses by allowing the capacitor storing the voltage differences between V_x and GND to charge faster. The main

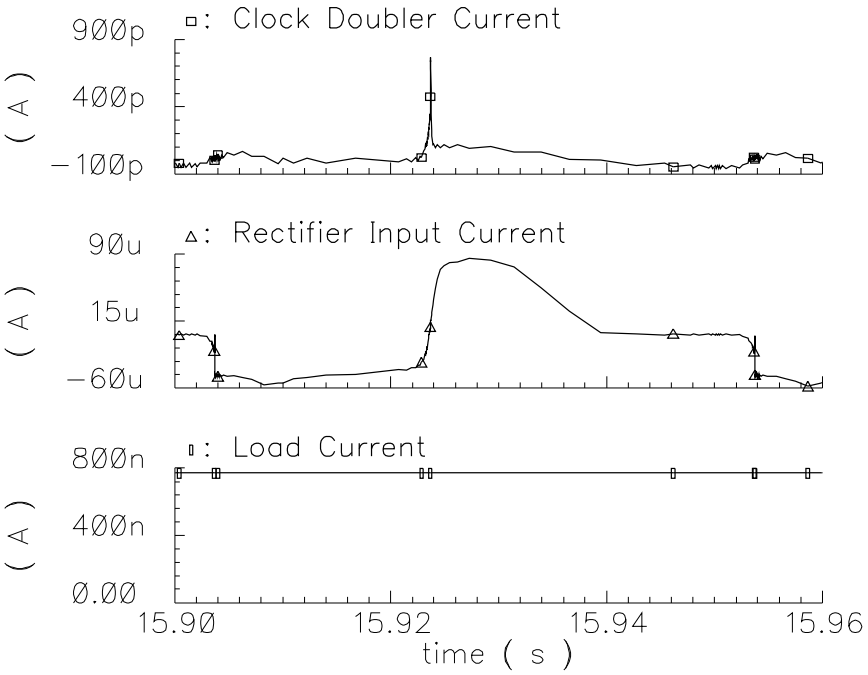

Fig. 15.: Current waveforms for the proposed SPR.

advantage, in terms of circuit components, of the SPR is there is only a maximum of two stacked devices in any given location throughout the system. This minimizes the amount of voltage drop, and therefore power loss, in the system. All supporting circuitry in the SPR is powered by the output voltage of the system and does not require any external battery thus making it well-suited for self-powered SHM sensors.

The differential clock doubler is implemented to reduce the ON resistance of the transmission gates. However, since this circuit is powered by the rectifier's DC output, it can reduce the overall efficiency of the rectifier. Therefore, the circuit must be designed carefully to insure there are no detrimental effects. Fig. 15 shows the simulated current waveforms in the proposed rectifier. The top plot shows the current for the clock doubling circuitry, the middle plot shows the input current, and the bottom graph shows the load current. The input signal was a 20Hz sinusoidal signal with an amplitude of 1V with a load resistance of 1MΩ. Although the input

appears to have a large current, the average current is on the order of a few μA.

In addition to DC output voltage, the power conversion efficiency (PCE) is also simulated to verify proper performance. Fig. 16 shows the simulated DC output voltages and PCE for 100kΩ and 1MΩ are both over 10% for a broad range of input amplitudes. It is seen that as the load resistance decreases, the input drive must increase to reach the maximum efficiency. Additionally, the peak PCE is seen to be larger for lower load resistances which can be attributed to the increased load current which can be delivered.

F. Design Considerations

There are generally many considerations when designing rectification circuitry, like any circuit, and there are trade-offs which one must consider when choosing values for components and the overall system architecture. In this section, some considerations for the design of the proposed SPR will be presented along with the impacts of the design choices on the overall system performance.

1. Start-up

For input amplitudes significantly smaller than the threshold voltage of the transistors ($V_{thn} \approx 0.7V$ and $|V_{thp}| \approx 0.9V$), the rectifier is unable to start-up. However, as the input amplitude approaches the threshold voltage of the devices, the output is able to converge to a DC steady-state value by charging the capacitor C_2 through the subthreshold source-drain current of the PMOS device which is approximately

$$I_{sd,p} = I_0 e^{\frac{V_{sg}-\left|V_{thp}\right|}{\phi_t}} \left(1 - e^{-\frac{V_{sd}}{n\phi_t}}\right), \tag{3.18}$$

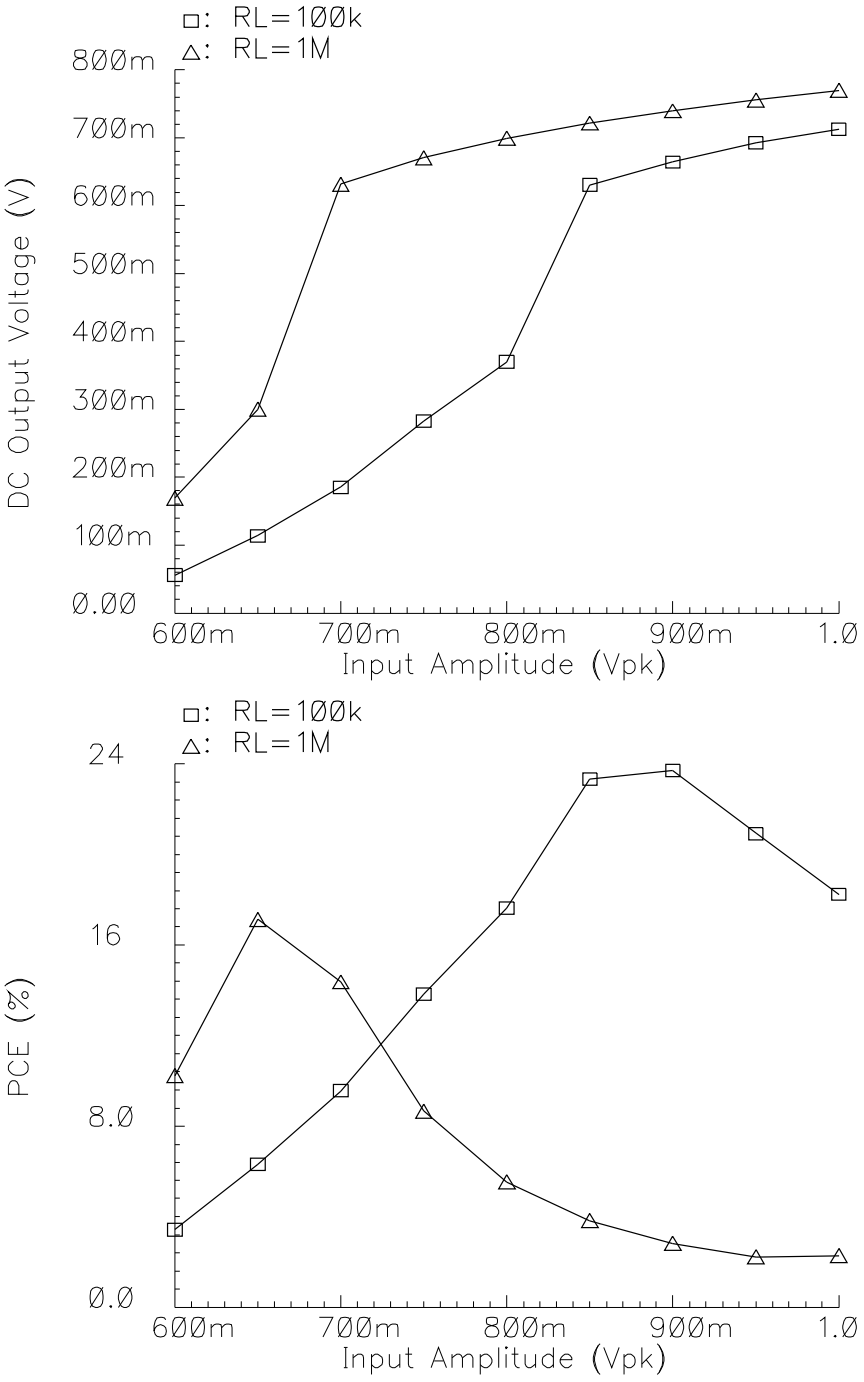

Fig. 16.: Simulated SPR DC output voltage (top) and power conversion efficiency (bottom) for load resistances of 100kΩ and 1MΩ with a 20Hz input frequency.

where I_0 is dependent on C_{ox}, μ_p or μ_n depending on the device, the subthreshold slope factor n, and ϕ_t is the thermal voltage. Since $C_1 \gg C_p$ at node V_x, the amplitude of the AC signal at V_x is almost identical to the input amplitude. Assuming the input sinusoid initially starts high, V_x will act as the drain for the NMOS device and the source for the PMOS device. Since there is no initial charge stored in any part of the circuit, and the output voltage is initially zero, this implies the NMOS device will only conduct leakage current initially and the PMOS device will charge the output capacitor C_2. As the input voltage goes below the output voltage level and starts going negative, node V_{out} becomes the source of the PMOS device since it is now at a higher potential than the input signal. The source and drain terminals of the NMOS device also change positions and this device conducts current from its drain terminal (GND) to its source terminal (V_x) as its V_{gs} value is no longer zero. The PMOS device will also conduct current into the V_x terminal but it will be a smaller value than the charging current applied to capacitor C_2. This reduction in PMOS current is because V_{out} is the source of the PMOS device during the negative half cycle of the input and will not be charged to the full DC value until after a few cycles have occurred. Therefore, its V_{sg} value is smaller than it was during the positive half cycle, which results in a lower current. After a few cycles, the steady-state DC output voltage is large enough to activate the comparator and begin its normal operation. As the input amplitude becomes larger than the threshold voltages of the devices, the forward conduction currents increase and the output voltage is able to charge to a steady-state value significantly faster than when the input amplitude is near the device threshold voltage.

Two conditions must be met for start-up to occur as described though: first, during the positive half cycle of the input, the current through the PMOS device must be larger than the required current draw through the load resistor and any

other parasitics or supporting circuitry; and secondly, during the negative half cycle of the input voltage the reverse conduction current of the PMOS, plus the draw through the resistive load and any other parasitics, must be less than the forward charging current during the positive half cycle of the input. To verify the zero state start-up as described, the proposed SPR was simulated in Cadence using the ON 0.5μm CMOS design kit. As can be seen in Fig. 17, the rectifier starts up without any difficulties and converges to a steady-state DC value of approximately 770mV for a 20Hz, 1V_{pk} input signal with a 1MΩ load resistor connected in parallel with C_2.

2. Comparator Design

The main constraints with the design of the comparator are to have a low enough input offset to not cause large errors in the decision, low power dissipation, and have a low latency compared to the period of the rectifier's input signal. Once the input signal passes the threshold of the inverter, the output signal will change with the delay of the inverter. Therefore, the inverters in the comparator must be designed to have low rise and fall times and proper sizing of the devices must be accounted for in the design. This is also accounted for in the design of the clock doubling circuitry. While this circuit can potentially reduce the overall rectifier efficiency, it must be designed with care. The maximum obtainable output swing is related to the sizes of the gate cross-coupled NMOS devices used to connect to V_{out} as well as the capacitors used for level-shifting. These impose area limitations in some designs and also effect the overall speed of the clock doubler output. The sizes of the inverters used to drive the transmission gates are one of the most critical aspects of the clock doubler. This is because they must be able to drive all switches within the comparator and must be larger than most of the other inverters in the design.

Finally, the transmission gates should be sized to not load the V_x and V_{out} nodes

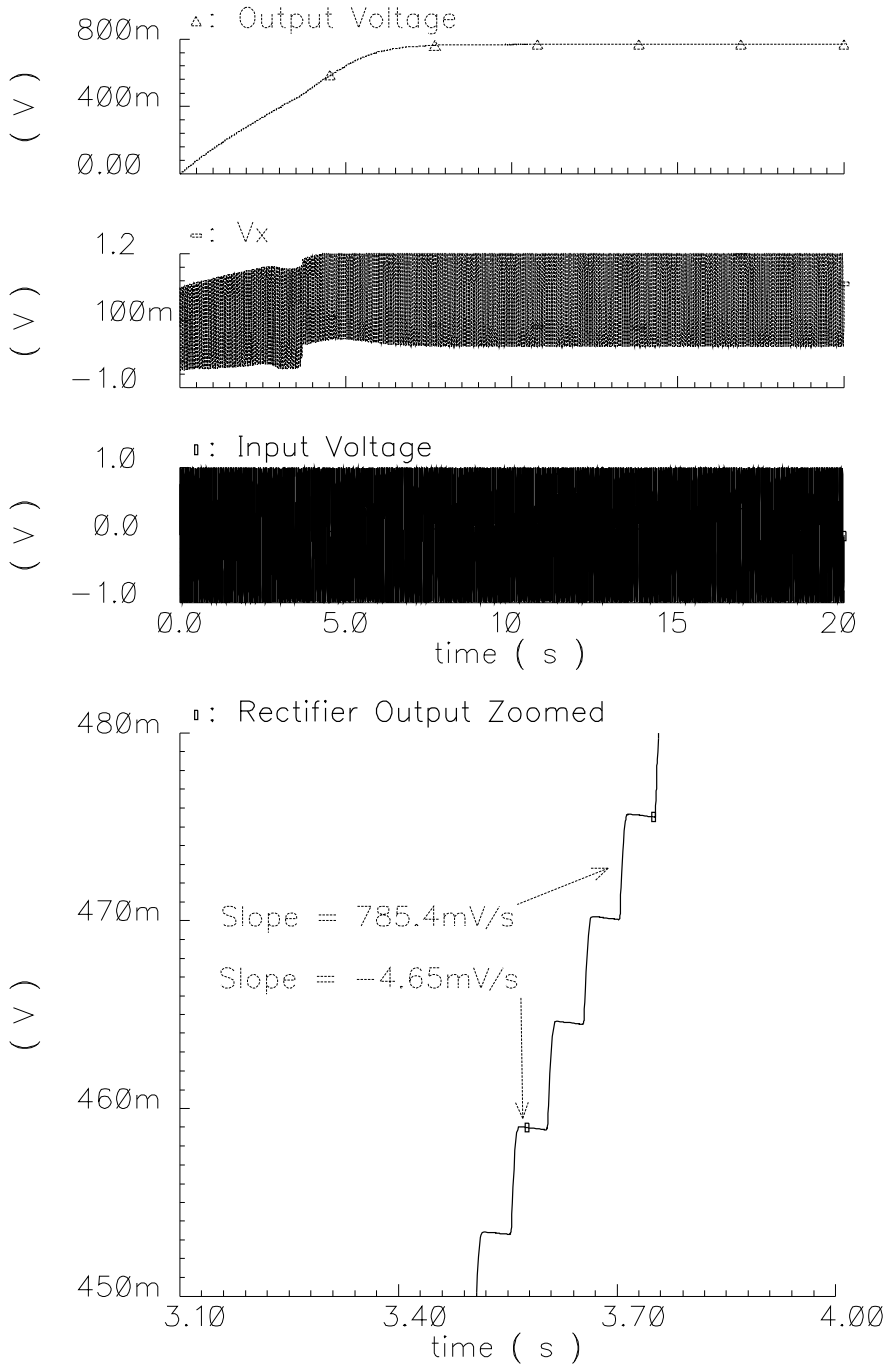

Fig. 17.: Simulated rectifier voltage waveforms (top) and zoomed in view of the rectifier output voltage during start up showing the charging and discharging of the output capacitor (bottom).

with significant amounts of parasitic capacitance while still providing a low enough ON resistance such that the comparator can make a decision in a reasonable amount of time so as to not degrade the rectifier efficiency. In Fig. 14, the RC time constant formed by the ON resistance of the transmission gates and the input capacitor of the comparator plays a role in the overall latency of the comparator. The value of the input capacitor should be selected so that it is larger than any parasitics but is practically limited due to area constraints. So, a range of values is set for the C used at the comparator input. In order to minimize the RC product, the ON resistance of the transmission gates should then be minimized. Assuming these devices, when ON, operate in the linear region, their ON resistance (R_{ON}) may be approximately given as

$$R_{ON} \approx \frac{1}{\beta_n \left(V_{gs,n} - V_{th,n}\right)} \parallel \frac{1}{\beta_p \left(V_{sg,p} - |V_{th,p}|\right)} \tag{3.19}$$

where $\beta_n = \mu_n C_{ox} \frac{W_n}{L_n}$ and $\beta_p = \mu_p C_{ox} \frac{W_p}{L_p}$. Since there is a limit to the size of the devices which can be used due to parasitic capacitance constraints, the main parameter which can be adjusted is the gate voltage of the devices. To decrease R_{ON}, the gate voltage should be made as large as possible without damaging the devices. To do this, a clock doubler can be used to apply the gate voltage to the transmission gates. However, the additional circuitry used to implement the clock doubling circuitry can potentially decrease the efficiency of the system. Therefore, it is necessary to verify the reduced R_{ON} is worth the area and additional power consumption. A simulation was performed where the input voltage was used to generate the signals ϕ and $\bar{\phi}$ using two different methods. The first method utilizes chains of inverters to drive the transmission gates using the sinusoidal input voltage. The inverter chain was comprised of three inverters to generate the signal $\bar{\phi}$ and, to generate ϕ, the sinusoidal input signal was applied to a chain consisting of an inverter, a delay stage consisting of a

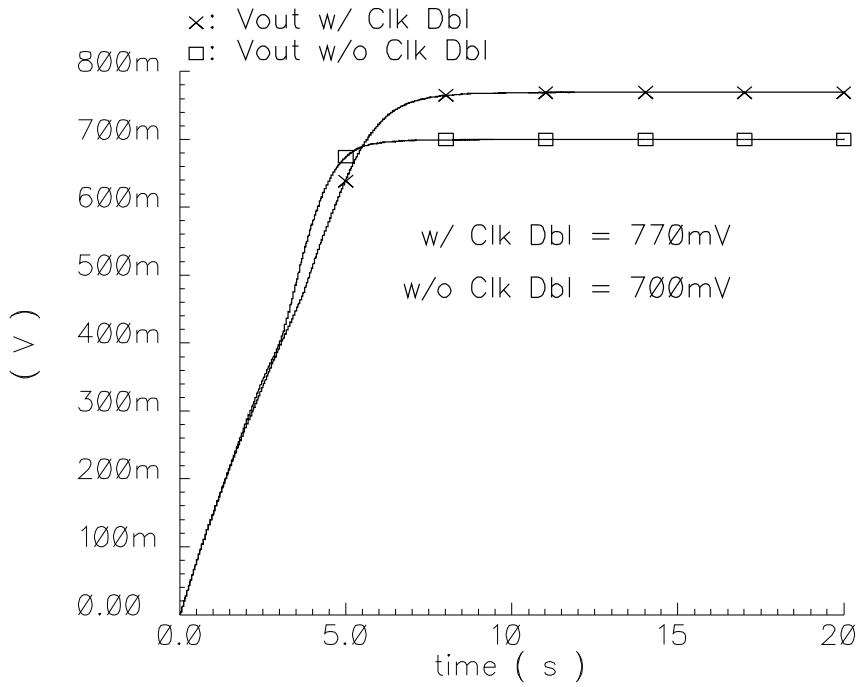

Fig. 18.: Simulated DC output voltages of proposed SPR with clock doubling circuitry in the comparator to drive the transmission gates and without clock doubling circuitry where inverters are used to drive the transmission gates. The input signal was a 20Hz sinusoid with a 1V amplitude. The load was a 1MΩ resistor while $C_1 = 1\mu$F and $C_2 = 100\mu$F.

transmission gate with the NFET gate tied to V_{dd} and the PFET gate tied to GND, followed by another inverter. Fig. 18 shows the improvement in obtainable output

voltage of the proposed SPR with the clock doubling circuitry compared to standard voltage driven transmission gates. As can be seen from this plot, the proposed circuit offers 10% more output DC voltage for the same input and loading conditions.

3. Switch Sizing

The sizes of the rectifier switches are chosen based on a few considerations. A comparison of simulation results is performed based on the overall system to be designed and the most optimum switch sizes for the given loading and input conditions is then selected. For example, the simulation set-up will be different for an RFID system than it would for a system which would employ a single sensor and no other circuitry which would then lead to a different circuit. Ideally, the switches should be made infinitely large to minimize the ON resistance and therefore conduction losses. However, this cannot be done since there is typically an area limitation in any IC design and increasing the switches directly increases C_p since

$$C_p \propto C_{ox} W L. \tag{3.20}$$

Therefore, a limitation on C_p is enforced based on the technology used, the frequency of operation, and the input amplitude. For matching purposes, it may be beneficial to size the N and P devices in such a way that their equivalent transconductances are equal as long as this does not degrade the overall efficiency. Conversely, the switches cannot be made too small either. As mentioned previously the ON resistance of these devices effects the overall latency of the comparator's decision. Therefore, proper choice of switch sizes must be made on the system being designed.

4. Capacitor Selection

The input capacitor C_1 should be chosen such that it is significantly larger than C_p and less than or equal to C_2. Since the PMOS device and C_2 act as the actual rectifier in these architectures, the larger the value of C_2 one can employ is typically better for storing more energy and reducing output voltage ripple. This will allow the

circuit to maintain a relatively constant DC output level and will be able to supply instantaneous current caused by dynamic operation. However, if the output capacitor and input capacitor are too large, it may take a significant amount of time to charge these devices to their steady state values due to their large time constants and the circuit may take too long to start-up or may not be capable of reaching a steady-state value.

As mentioned in [78], as the frequency of operation decreases the size of the capacitors used in the rectifier topology must increase to keep the conversion efficiency (voltage and power) at a higher value. However, for low frequency signals, as is the case in this work, using too large a time constant results in extremely large charging times (up to a few hours) depending on the input amplitude. Therefore, there is a trade-off between maximum achievable performance and practical use. The change in capacitor voltage with respect to time may be expressed as

$$\Delta V = \frac{I}{C_2}\Delta t. \tag{3.21}$$

Assuming the rectifier's input signal is in the negative half cycle (PMOS is shut off) and the current flowing through the PMOS device can be neglected, the value of the current I in the previous equation is equal to V_{out}/R_L. For a fixed output voltage and $\Delta t \approx T/2 = 1/2f$, the only two parameters which may be adjusted to minimize ΔV, the output voltage fluctuation, are R_L and C_2. Since, for a given V_{out}, lowering R_L implies a larger DC power delivered to the load, this value should be kept as low as possible. It should be mentioned that lowering this value too low will cause the output to discharge before the rectifier can fully recharge the output capacitor. So, this sets a minimum for R_L which the rectifier can drive. Therefore, the value of C_2 should be chosen to keep a reasonable ΔV to deliver the required DC power to the load while still allowing the rectifier circuit to re-charge the capacitor during the

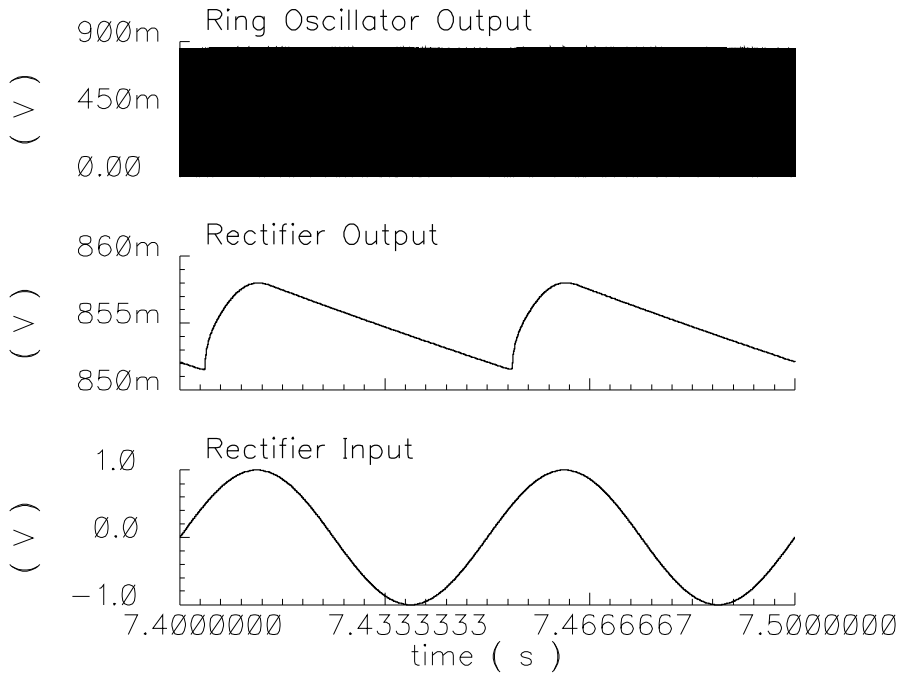

Fig. 19.: Simulated 5-stage ring oscillator start-up powered by single stage proposed SPR with $1V_{pk}$, 20Hz input signal with $C_1 = 1\mu F$ and $C_2 = 100\mu F$. Oscillation frequency is approximately 6.3kHz.

positive half cycle of the input signal.

Lastly, although maximum power transfer from the source to the input of the rectifier occurs when the reactance of the source and the input of the rectifier are complex conjugates and the resistances are equal, this does not necessarily promote the largest power delivered to the load of the rectifier. This is because under input power matching conditions the voltage V_x will be half of what it was at the output of the source. This greatly effects the overall output voltage that is obtainable as seen in Fig. 16 and was also mentioned as a key design point in [69]. This implies that a proper choice of C_1 should be made to correspond with the source impedance while providing the maximum obtainable output power.

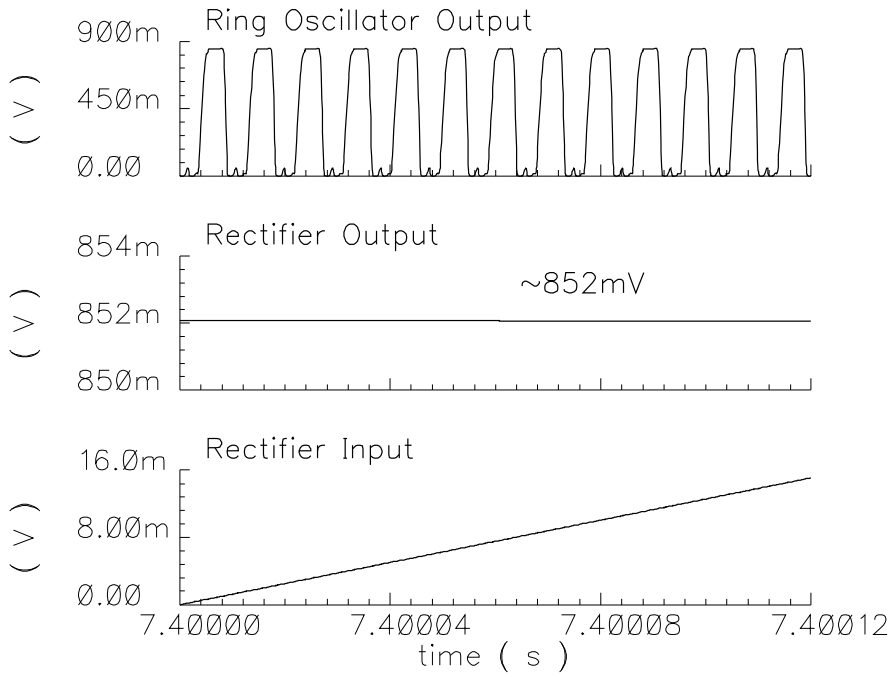

Fig. 20.: Zoomed view of Fig. 19.

5. Ability to Power Other Circuits

The proposed SPR and 4-stage rectifier are intended to be implemented in a larger system where they will provide DC power to additional circuits. For many low-power circuits, a clock signal is needed in order to power digital circuitry and/or transmit circuitry. Therefore, the proposed SPR was simulated in Cadence with a 1V amplitude sinusoidal signal with a frequency of 20Hz and the DC output was used to power a 5 stage ring oscillator. The results of the simulation are shown in Figs. 19 and 20. The rectifier is shown to start-up without any issues and settle to a final DC value of approximately 770mV and the ring oscillator frequency is approximately 6kHz.

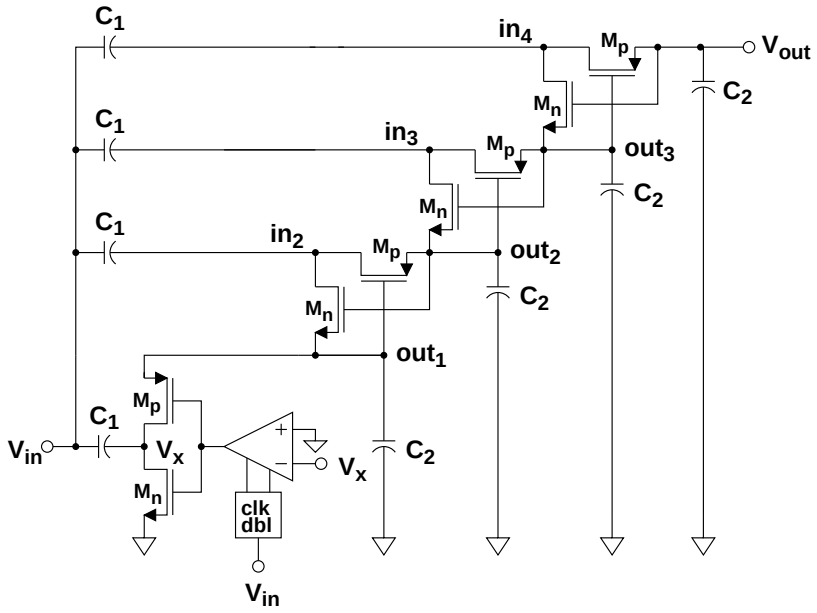

Fig. 21.: 4-stage rectifier with proposed SPR and three cascaded SVC structures.

G. Measurement Results and Discussion

1. Measurement Results

The circuit shown in Fig. 14 was fabricated in ON 0.5μm CMOS technology. Additionally, for comparison purposes, an SVC structure was also fabricated and measured. To show the versatility of the proposed SPR, a 4-stage RM was fabricated utilizing the SPR as the first stage with three cascaded SVC stages. A schematic of this circuit is shown in Fig. 21. For comparison, a 4-stage SVC-only structure was also fabricated and measured. Fig. 22 shows the die photographs of the fabricated rectifiers with detailed connections of the off-chip 1μF and 100μF capacitors for the proposed 4-stage rectifier with corresponding names as in the schematic shown in Fig. 21.

To verify the performance of the proposed rectifier, a 20Hz sinusoidal signal was applied to the input of the SPR and the input voltage amplitude was swept.

Different values of load resistors were applied to the circuits to emulate next-

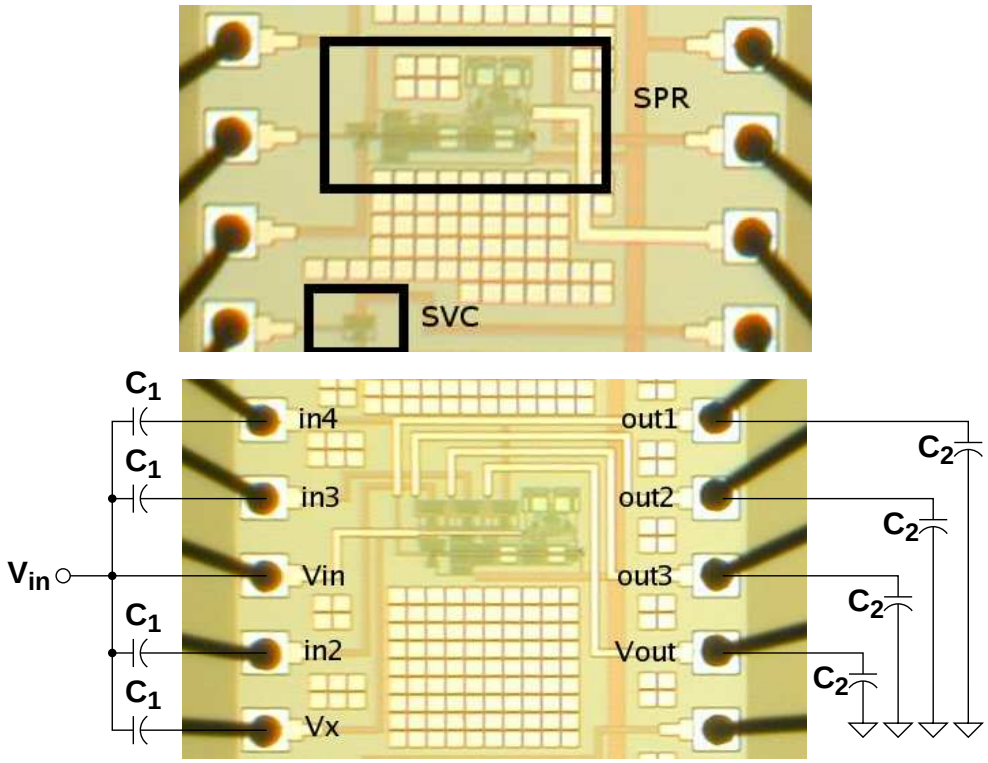

Fig. 22.: ON 0.5μm CMOS SVC and SPR (top) and 4-stage rectifier with SPR and three cascaded SVC stages (bottom).

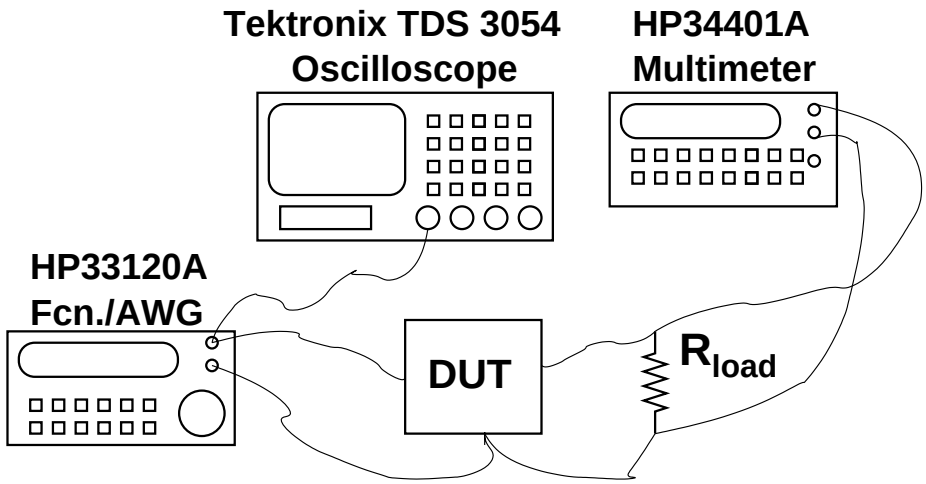

Fig. 23.: Test-bench for rectifier measurements.

stage loading and to characterize the driving capabilities of the RMs. A diagram of the test set-up for the rectifiers is shown in Fig. 23. The 1μF and 100μF capacitors used were implemented using off-chip electrolytic capacitors.

The size of the capacitors were selected large to obtain the largest possible output voltage since the amount of loss due to the capacitors is inversely proportional to the frequency of excitation. Although these capacitors are large compared to other sensor networks such as RFID, for the proposed low frequency application these capacitor sizes are only a small portion of the overall sensor network size. In the event the proposed SPR is employed in a higher frequency application, smaller capacitors can be implemented. It should be noted that although Fig. 23 shows the output of the function generator connected to the D.U.T. and the oscilloscope, this is only done momentarily to verify the actual input amplitude. The short duration of the oscilloscope's connection to the circuit is due to its finite input impedance which increases the minimum voltage required for starting the rectification process.

The measured output voltages for the SVC and proposed SPR architectures are shown in Figs. 24 and 25, respectively, and the measured output voltages of the 4-stage SVC structure and the 4-stage structure with the proposed SPR is the first stage are shown in Figs. 26 and 27. Although the single stage SVC produces a larger maximum output voltage than the proposed SPR structure, the 4-stage architecture utilizing the SPR as the initial stage produces an output voltage approximately 500mV larger than the 4-stage SVC structure under the same input and loading conditions. This increase in performance can be attributed to the loading effect of the comparator being a dominant limitation in the single stage case and being isolated from the output in the 4-stage architecture. This is because in the single stage SPR, the positive terminal of the comparator is connected directly to the output of the circuit and is directly in parallel to any load present. This then limits the maximum voltage in a single

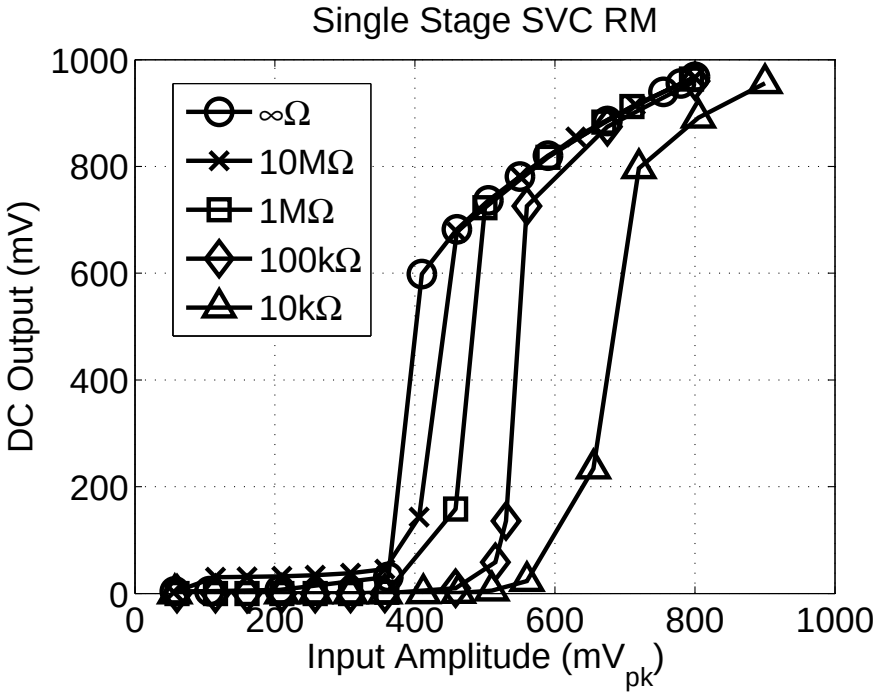

Fig. 24.: Measured single stage SVC DC output voltage.

stage. However, in a multi-stage structure with an SPR as the first stage, its load is the second stage rectifier and remains fairly constant in steady-state. Therefore, the output produced becomes much larger than the typical 4-stage SVC structure.

Figs. 28 and 29 show the calculated output powers for the different architectures under different loading and input conditions. It is worth mentioning that the maximum deliverable output power for the 4-stage SPR-based rectifier is higher than the 4-stage SVC structure.

2. DC Power Delivery

To demonstrate the ability of the proposed 4-stage rectifier with the SPR's ability to deliver DC power, its output was connected as the DC supply for a low-power circuit which could be used in an energy harvesting application. The proposed 4-stage rectifier was connected as shown in Fig. 23 where, in place of the load resistor,

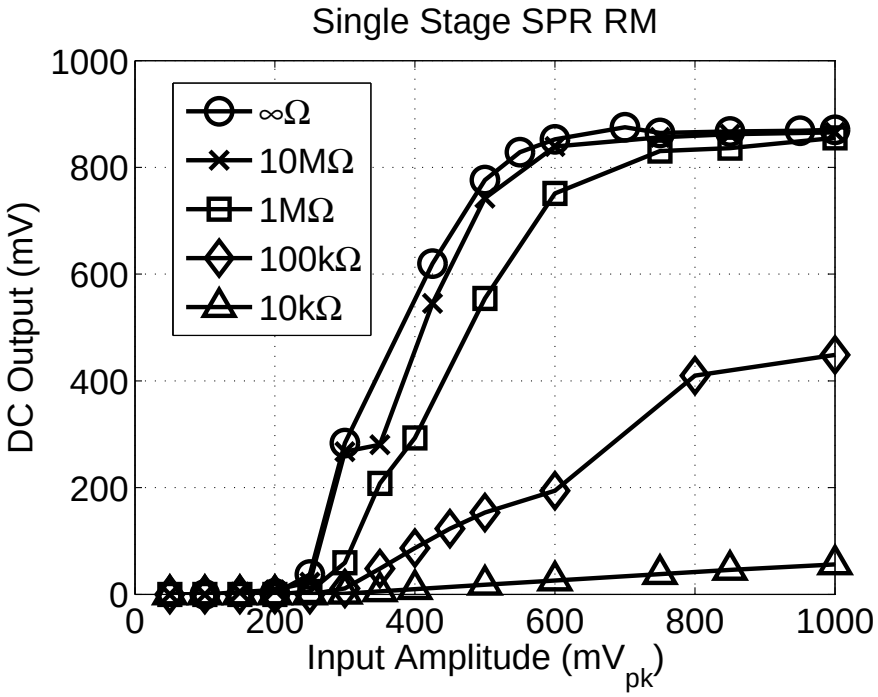

Fig. 25.: Measured single stage SPR DC output voltage.

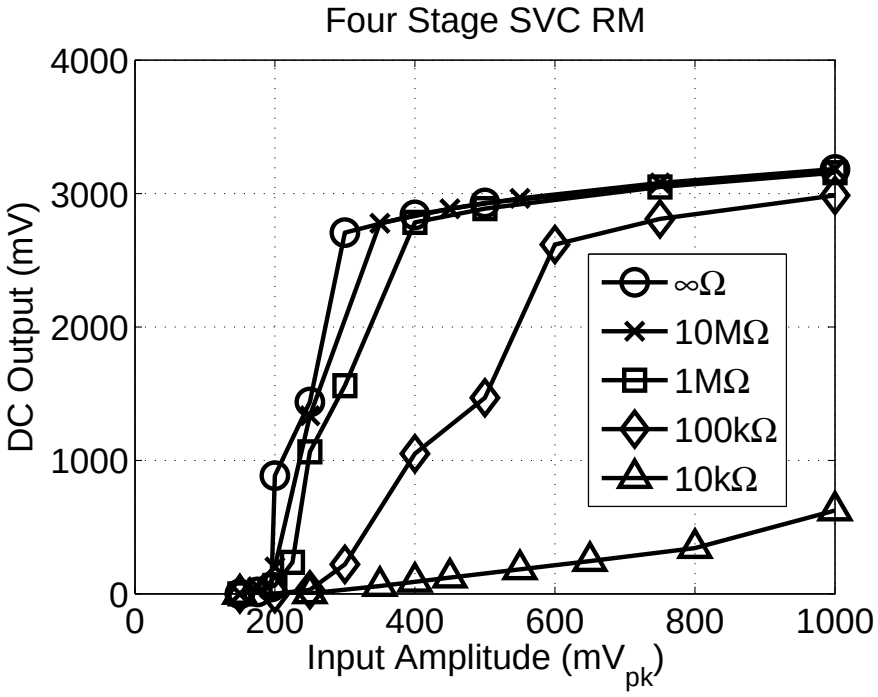

Fig. 26.: Measured 4-stage RM SVC DC output voltage.

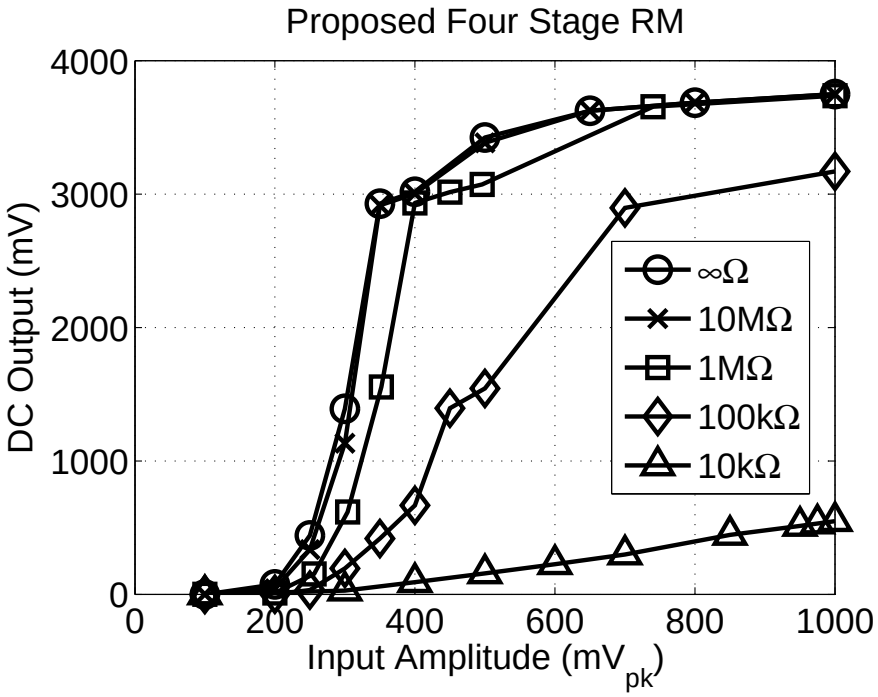

Fig. 27.: Measured 4-stage RM utilizing the proposed SPR DC output voltage.

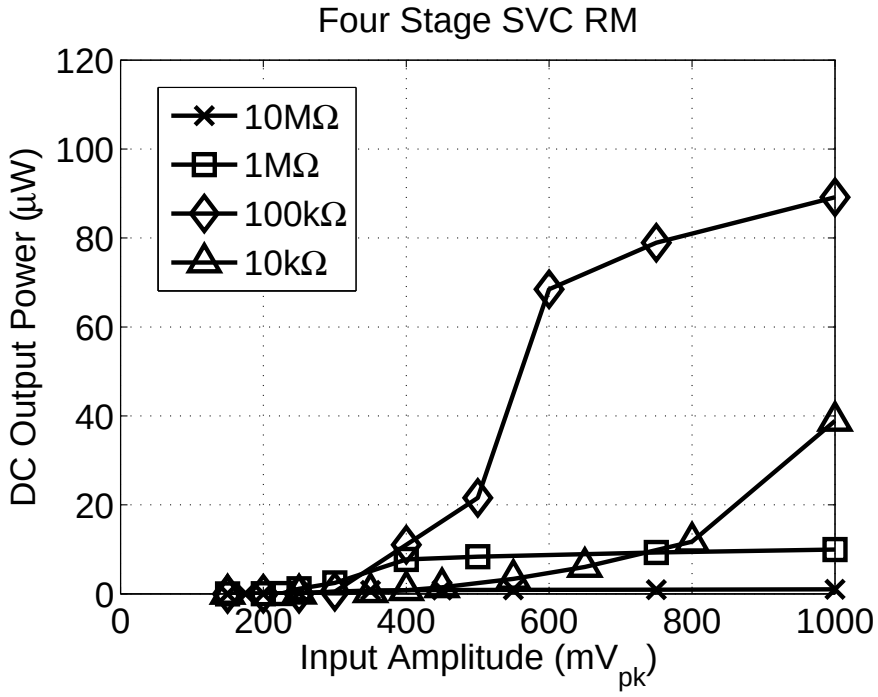

Fig. 28.: Measured 4-stage SVC DC output power.

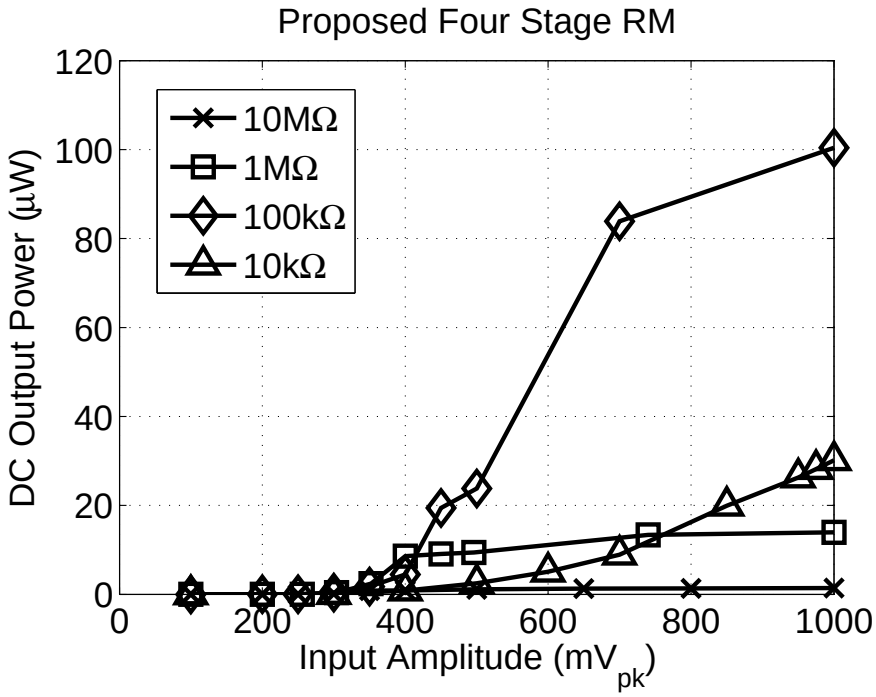

Fig. 29.: Measured 4-stage RM utilizing the proposed SPR DC output power.

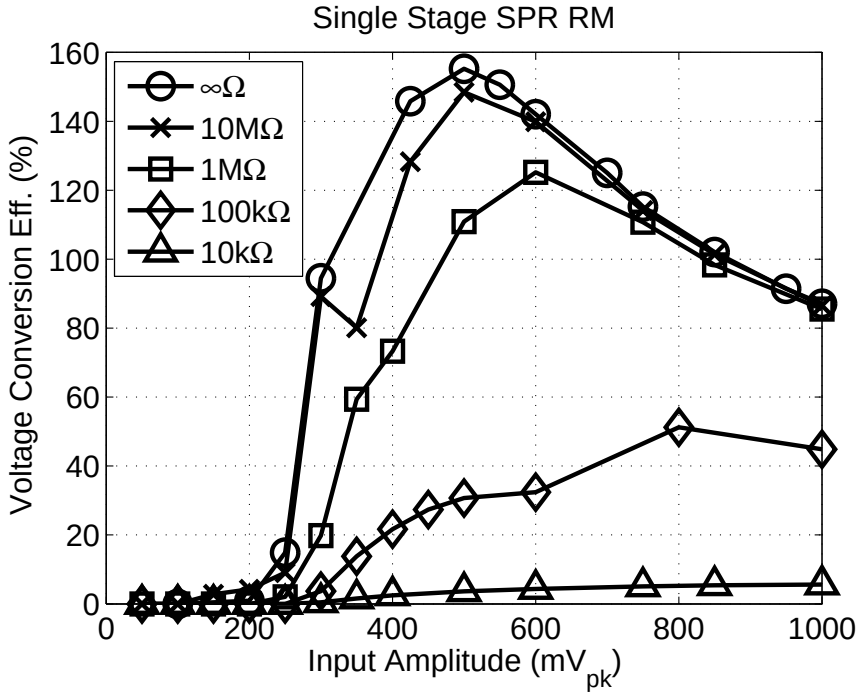

Fig. 30.: Measured single stage SPR VCE.

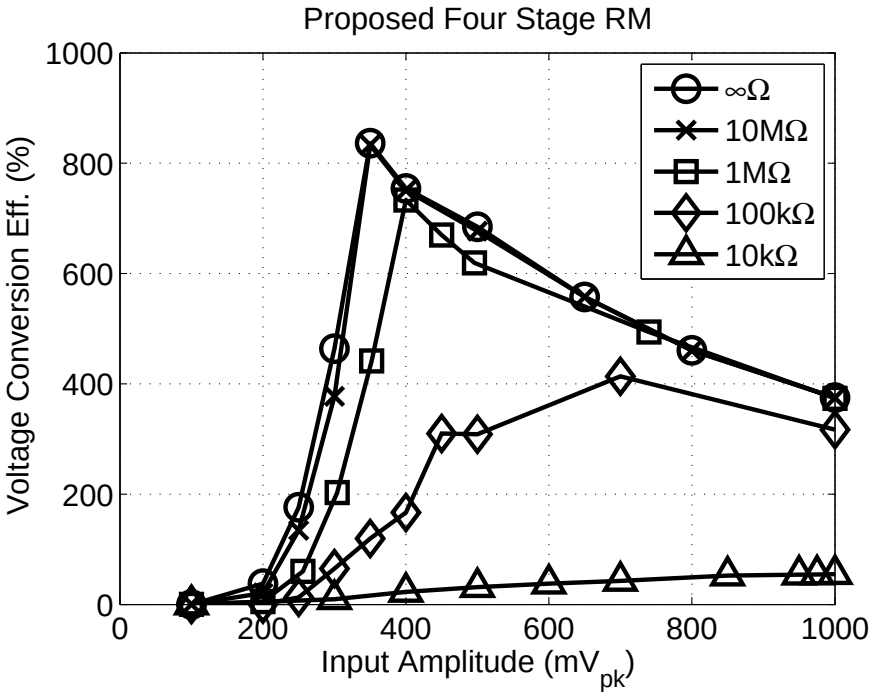

Fig. 31.: Measured 4-stage RM utilizing the proposed SPR VCE.

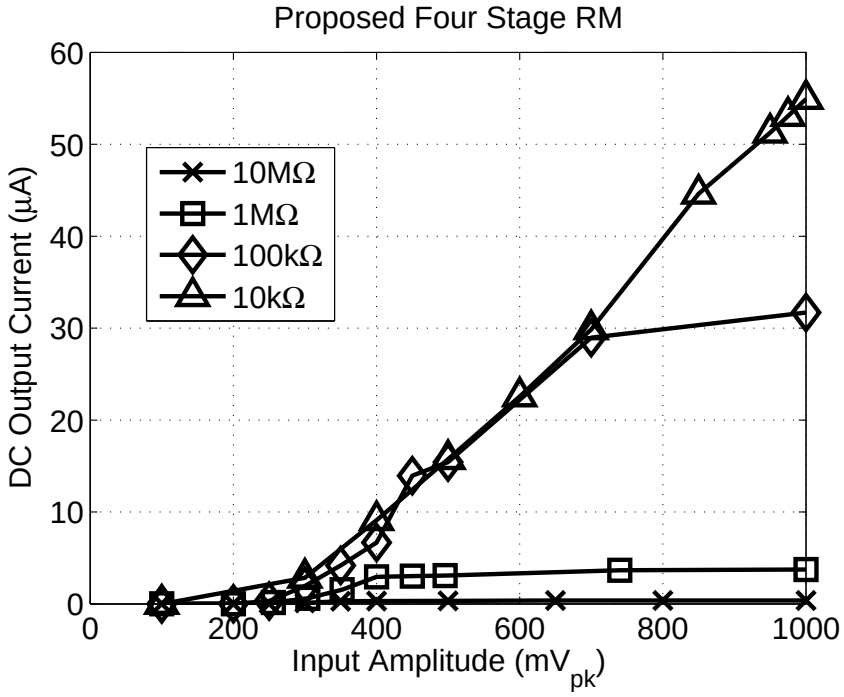

Fig. 32.: Measured 4-stage RM utilizing the proposed SPR DC output current.

the rectifier output was connected as V_{dd} for a 6-bit successive approximation register analog-to-digital converter (SAR ADC) that was designed for operation with low-power and low-voltage. The input to the rectifier was a 20Hz sinusoid with a peak input voltage of 1.2V. The values for C_1 and C_2 were 1μF and 100μF, respectively. Prior to connecting the SAR ADC as the load to the 4-stage rectifier, the DC output with an infinite load was measured to be over 3V. When the ADC was connected as the load, the DC output voltage dropped to approximately 1.6V. This implies, according to Fig. 27, that the SAR ADC has an effective loading resistance to the proposed 4-stage rectifier of somewhere between 10k and 100kΩ. The results of this measurement are shown in Fig. 33.

3. Discussion

As can be seen from Fig. 25 and 27, the proposed SPR and 4-stage rectifier are able to provide DC output voltages of greater than 700mV and 3V for input signals between 400mV$_{\text{pk}}$ and 1000mV$_{\text{pk}}$, respectively, with load resistances larger than 100kΩ. Although these results are promising, they are still limited by the necessity of loading the rectifier with resistances greater than a few 10s or 100s of kΩ which limits the amount of output power that can be delivered. Nevertheless, the DC levels (voltage and current) are large enough to power circuitry which only requires a few μW of power. This is the main limitation of the proposed SPR. However, the greatest benefits of the proposed system are its ability to operate at low input frequencies and with amplitudes that are comparable to the threshold voltages (V_{th}) of the FETs used in the circuit design. While other rectifiers are able to provide a larger output power to similar or smaller loads, obtain a higher efficiency (power conversion or voltage conversion) [59, 60, 64, 78, 79], these rectifiers require input amplitudes larger than required in this design. This is a great advantage for the proposed SPR since

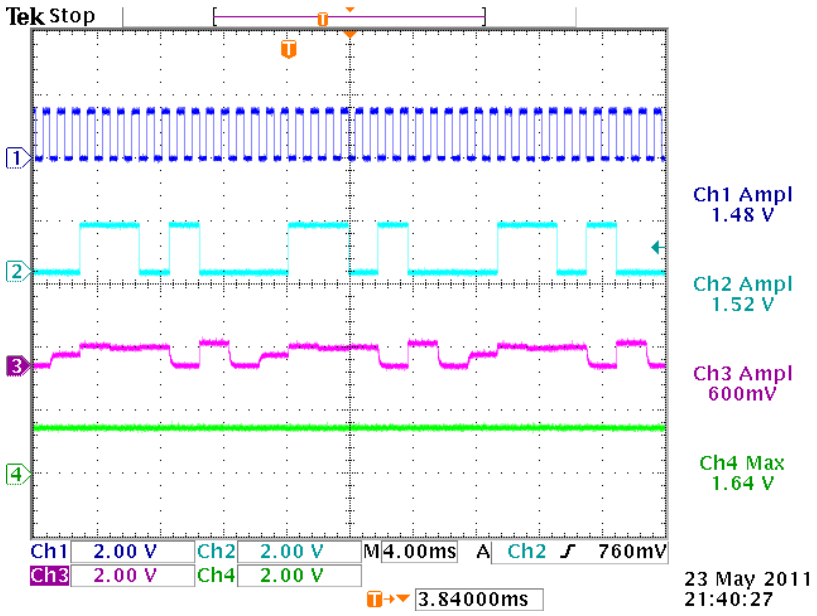

Fig. 33.: Measurement results of the proposed 4-stage rectifier powering a low-voltage, low-power 6 bit successive approximation register analog-to-digital converter (SAR ADC). The input to the 4-stage rectifier was a 20Hz sinusoid with a 1.2V amplitude. From top to bottom, the measurement shows the output of the on-chip SAR ADC clock generator, the serial output of the 6 bit SAR ADC, the output of the DAC used in the SAR ADC, and the DC voltage produced by the 4-stage rectifier.

in energy harvesting applications one is not always able to generate input signals on the order of $2V_{pk}$ as required in many other designs. Table II shows a comparison of the SPR with other state of the art rectifiers. As seen from this comparison, the proposed SPR's maximum input amplitude is equal to the minimum input amplitude required for most the other rectifiers to achieve their reported performances making the proposed SPR more suitable for low voltage energy harvesting applications since the output voltage/current from the energy harvester may not be large. The design presented in [82] shows good performance at a frequency of 10Hz and similar out-

Table II.

Performance comparison with recently reported rectifiers.

	[82]	[83]	[79]	This Work
Tech.	$0.35\mu^*$ CMOS	0.35μ CMOS	0.35μ CMOS	0.5μ CMOS
f_{in} (Hz)	10-10k	100 & 200	200k & 1.5M	20
$\|V_{in}\|$ (V_{pk})	0 – 1	1 – 6.5	1.2 – 2.4	0.1 – 1
$V_{out,DC}$ (mV)	0 – ≈1	0 – 6500	1130 – 2280	0 – 850
$\frac{V_{out}}{\|V_{in}\|}$ (V/V)	0.95	0.95***	0.915	≈0.88
PCE_{max} (%)	≈90** R_L=50k	– R_L="several" k	65-89 R_L=1.8k	≈24** R_L=100k

* – low-V_{th} process

** – Simulation *** – Estimated from figure

put resistance and capacitance values, however this design utilizes a low-V_{th} process which adds extra processing costs during fabrication. The work in [83] is focused on an entire energy harvesting system and the minimum input amplitude for the rectifier was equal to the largest input amplitude in this work. Further investigation would be necessary to compare the two topologies for this application.

H. Conclusions

A self-powered rectifier for low frequency vibration energy harvesting for SHM of bridges has been presented. Based on the extrapolated electrical model of the MSMA energy harvester shown in chapter 2, the rectifier was simulated and tested using these same conditions at the input (i.e., series source resistance and inductance, 20Hz excitation frequency, 100 to 1000mV$_{pk}$ AC input signal). Measurement results show the proposed rectifier topology is capable of providing power for additional circuitry to be employed in a structural health monitoring environment.

CHAPTER IV

SENSOR AND MODULATION CHOICE

The proposed SHM sensor system presented in chapter 1 is shown again in Fig. 34 for clarity. In chapter 2 an MSMA energy harvester was presented and an extrapolated electrical model of the output of the energy harvester was also shown. In chapter 3 the model of the MSMA output was used as the input for an AC/DC converter to generate a usable DC voltage/power for the remaining circuitry in the proposed system. Knowing the limitations of the energy harvester and AC/DC converter, as well as how much power they are able to provide for the system, one is now able to pare down the options and design considerations for the remaining system components. One of these is the amount of DC power which may be tolerated in each of the subsequent blocks attached to the output of the rectifier. This power is a function of the equivalent loading impedance of the sensor. Additionally, the power consumption, in practical terms, for the transmission circuitry is dependent on the modulation format which is employed in the transmit circuitry. In this chapter, a strain gage sensor is analyzed and assumed to be the sensor in the proposed system, although other sensors may be implemented as well (i.e., temperature, fiber-bragg grating, accelerometer, etc.). Finally, different modulation methods are compared in terms of practical implementations, bit-error-rates (BERs), and power consumption issues.

A. Strain Gage Analysis

For the proposed wireless sensor system, one main concern is the implementation of the sensor itself and its impact on the overall system efficiency. This is because depending on the sensor's operation, it may affect the overall power consumption

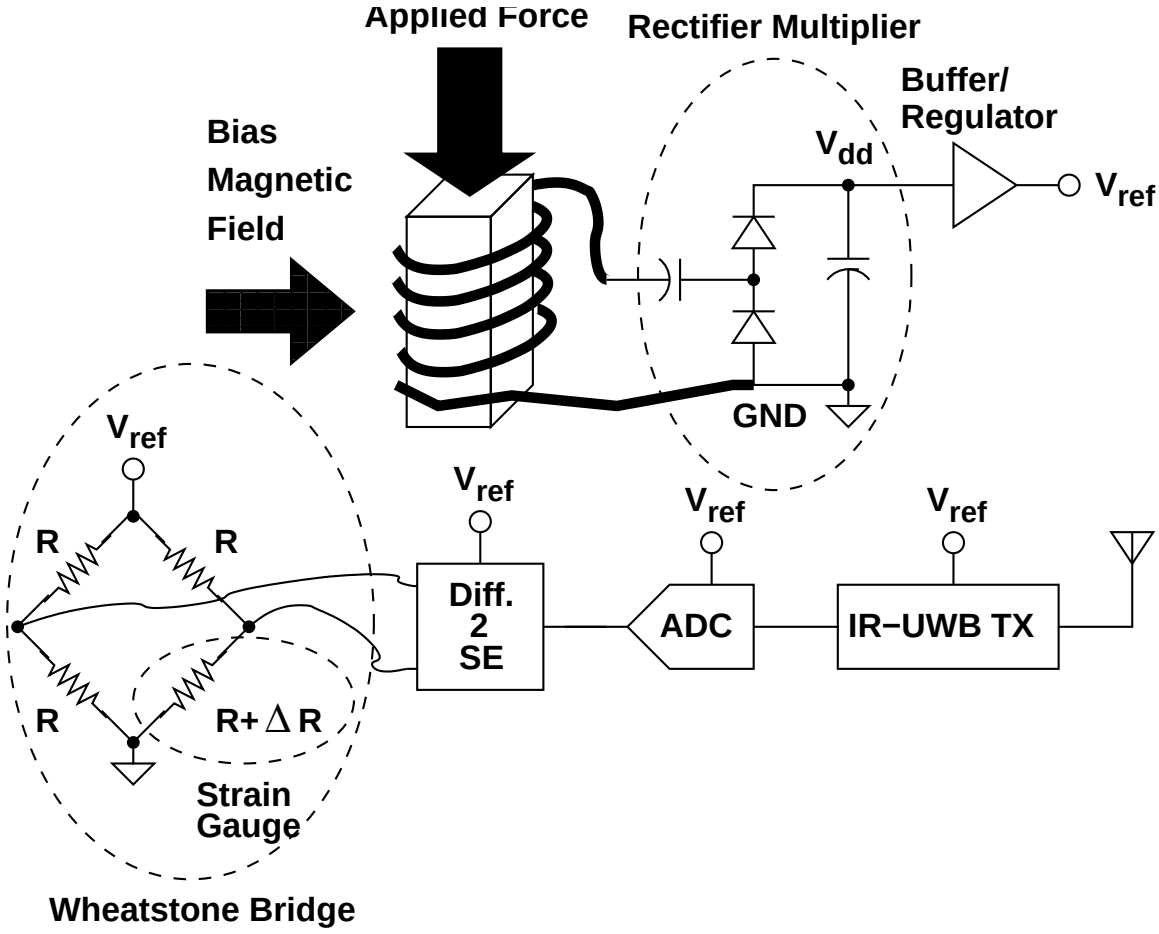

Fig. 34.: Generalized SHM sensor architecture.

which will then have an impact on how well the AC-DC converter works. While there are many different types of sensors (pressure, temperature, etc.), there is one specific sensor which is well-suited for applications where materials are expected to move/deform/vibrate. These sensors are commonly referred to as strain gages. A rough idea of what an implementation of a strain gage may look like is shown in Fig. 35. Here, the gage factor (GF), also called K_s, is shown to be

$$K_s = \frac{\frac{\Delta R}{R}}{\epsilon}. \tag{4.1}$$

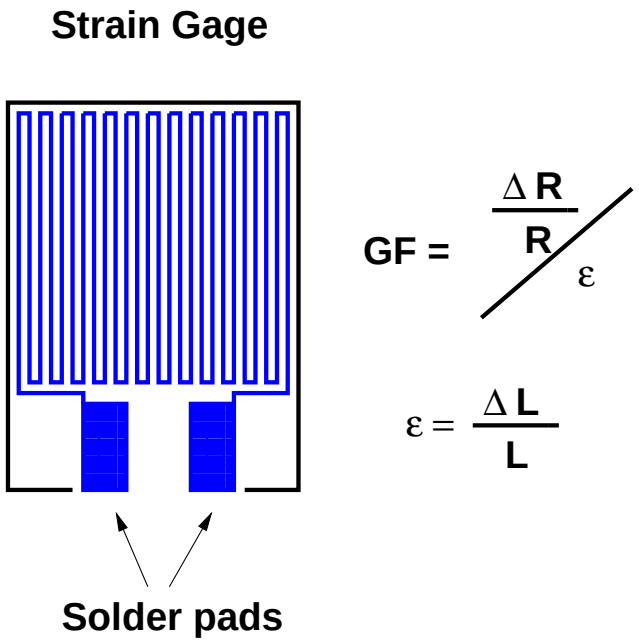

Fig. 35.: Typical strain gage.

equal to the change in resistance over nominal resistance value divided by the applied strain. The strain gage itself is often a patch design and may be fixed to the area in question in any desired orientation. Solder pads are then used to connect the strain gage to the appropriate measurement set-up or allow one to use probes for measurement. Typically strain gages are not used alone for detecting strain. Often they are employed as part of a Wheatstone bridge as shown in Fig. 34.

Assuming a Wheatstone Bridge configuration for the proposed wireless sensor system and only one strain gage where the nominal strain gage and other resistances are all equivalent, the differential output voltage of the bridge is

$$V_{out} = V_{ref}\left[\frac{1}{2} - \frac{R + \Delta R}{2R + \Delta R}\right]. \tag{4.2}$$

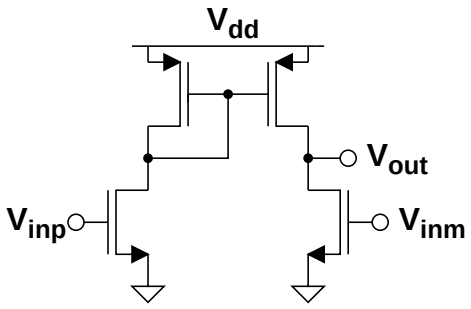

Fig. 36.: Differential to single-ended converter/lowpass filter.

After some manipulation, this expression may be presented as

$$|V_{out}| = V_{ref}\frac{\frac{\Delta R}{R}}{4 + 2\frac{\Delta R}{R}}. \tag{4.3}$$

Assuming that $\Delta R \ll R$ it is possible to simplify the output voltage to

$$|V_{out}| = \frac{V_{ref}}{4}\frac{\Delta R}{R} \tag{4.4}$$

$$= \frac{V_{ref}}{4}K_s\epsilon. \tag{4.5}$$

The output of the strain sensor is differential in nature which is usually desired for noise and common mode immunity (common mode immunity is a circuit's ability to remove signals which are the same on each line). However, in this application, it is undesirable to support the power consumption of differential circuits. Instead, the signal should become single ended and digital as soon as possible. Therefore, the differential output of the strain Wheatstone bridge is fed into a differential to single-ended converter which also implements a lowpass filter when loaded by a capacitor. This circuit is shown in Fig. 36. The output of this circuit is nominally kept slightly higher than mid-rail and the differential signal between the two outputs will then either pull up or pull down the voltage which is then fed into the sample and hold stage for the ADC.

Since the output of the strain gage is proportional to the applied strain, this change in output voltage from its nominal point is directly reflected as a change in strain. Therefore, the sensitivity of the ADC to resolve changes in strain is a factor in determining the required number of bits. For the ADC to resolve the strain change, the differential voltage change from the Wheatstone bridge must be greater than 1 least significant bit (LSB) of the ADC. An LSB is the smallest size, or quantization level, that the ADC is able to resolve and, is usually related to a reference voltage (V_{ref}) and the total number of levels the ADC can produce (2^N, where N is the number of bits). Therefore, it is safe to say

$$\Delta V_{out} \geq 1 \text{ LSB} \tag{4.6}$$

$$\frac{V_{ref}}{4} K_s \epsilon \geq \frac{V_{ref}}{2^N}. \tag{4.7}$$

It is helpful to express the result from (4.7) in two different ways. One is to express the minimum required ADC bit number as a function of strain change.

$$N \geq 2 - \log_2 \left[K_s \Delta \epsilon \right] \tag{4.8}$$

The other manner which the former equation may be presented as useful is to place the minimum detectable strain change as a function of ADC bit number.

$$\Delta \epsilon \geq \frac{1}{K_s 2^{2-N}} \tag{4.9}$$

Fig. 37 shows plots of these two different equations.

Strain is usually expressed as either a decimal or a percent. Often times, as the case with voltage or current, the strain is expressed in terms of mϵ or $\mu\epsilon$ much like voltages are often expressed as mV or μV. In order to obtain a detectable strain change of greater than 30mϵ, an ADC resolution of approximately 6 bits is required

for all gage factors. However, as the gage factor increases, the system is also able to resolve significantly smaller values of strain due to the increased sensitivity of the gage itself. It should be noted that a typical strain gage has a gage factor of approximately 2.

It was previously mentioned that the sensor has an effect on the overall system performance, namely the system efficiency. Assuming no applied strain and all nominal resistance are equal within the Wheatstone bridge and have a value of R, the equivalent impedance seen by the power conditioning circuitry is R. Therefore, the amount of current which will flow through the strain gage is DC and has a value of V_{ref}/R. As can be seen from the results shown in chapter 3, the AC-DC converter is able to produce larger voltages when its load resistance is larger. Therefore, it is necessary to increase R as large as possible while still making the system spatially and financially viable. Engineers at SMD Sensors are able to make strain gages using a sputtered thin film technique with nominal resistance values of $4\text{k}\Omega/\text{mm}^2$. This implies that as long as the sensor occupies an area larger than 25mm^2 the value of the strain gage's resistance may be larger than $100\text{k}\Omega$. Assuming the power conditioning circuitry is able to generate 1V for the circuitry, this impedance value would correspond to a nominal DC power consumption of 10μA. Although this may be too large, the option of manufacturing a custom strain gage allows one to increase the nominal strain resistance to lower the power consumption and improve overall system efficiency at the cost of a larger area.

B. Choice of Modulation

While there are many different types of data modulation, the choice of modulation for the sensor network has a dramatic impact on the overall system efficiency. Ad-

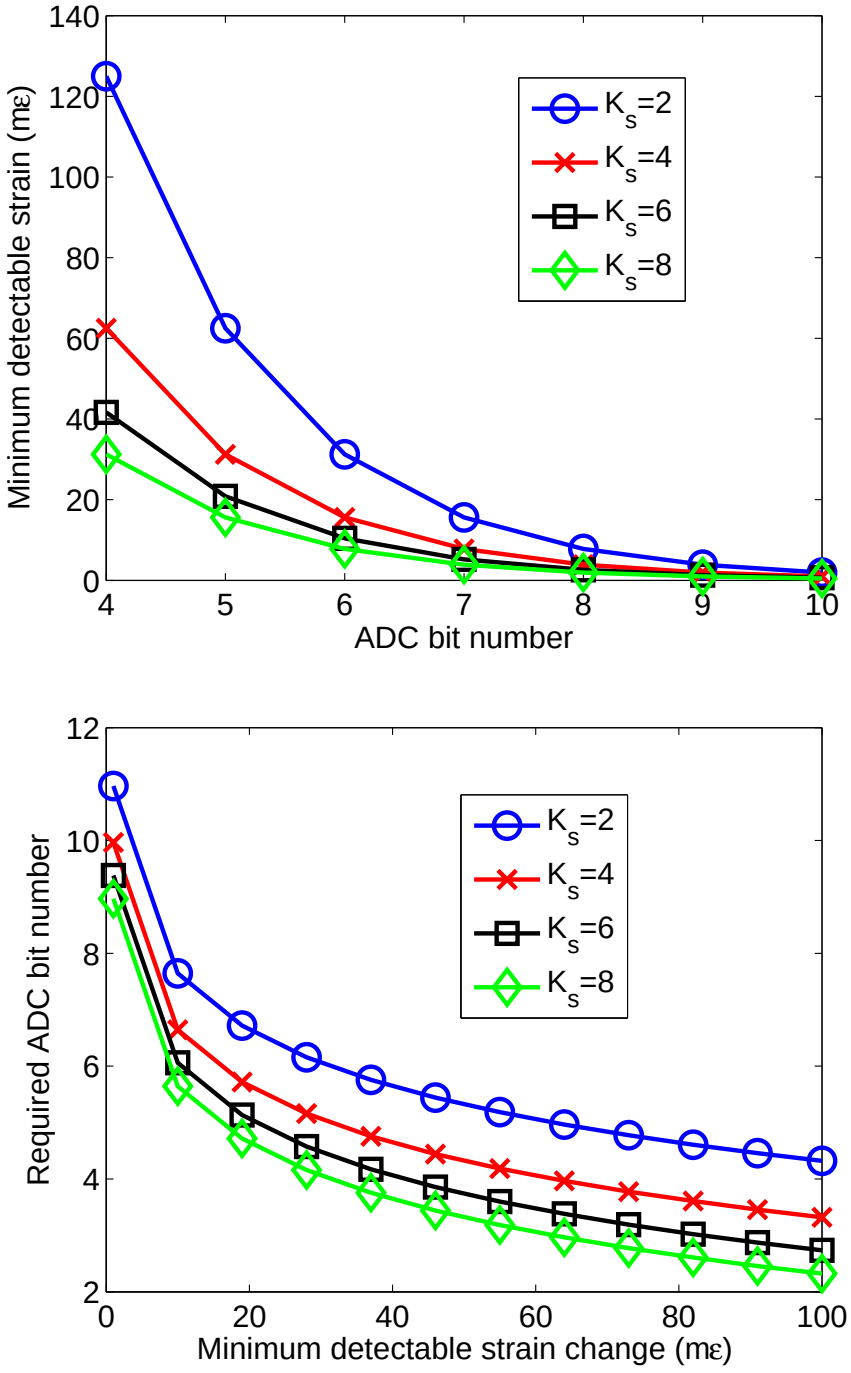

Fig. 37.: ADC resolution and minimum detectable strain change for different gage factors: ADC bits as variable (upper); minimum detectable strain change as variable (lower).

ditionally, because the MSMA material will be supplying the energy for the sensor itself, there is a major limitation on power consumption during data transmission. Due to this limitation, the modulation options are greatly reduced. Since a low-power ADC is implemented to convert the strain data into a digital output code, it makes sense to use a digital modulation format for data transmission. While there are a few options for digital modulation, each has their own advantages and drawbacks in terms of efficiency, probability of error, and ease of implementation.

In terms of comparing the probabilities of bit error for the different modulation formats, it is constructive to understand the equations which will be presented. In communication theory, the probability of bit error is often times expressed in terms of the Q-function for a given bit energy (E_b) and noise (N_0). In the following discussions and graphs, the noise is assumed to be an additive white Gaussian noise (AWGN) with a specific mean and is distributed normally about the mean. In that case, it may be stated that

$$Q(x) = \frac{1}{2}\mathrm{erfc}\left(\frac{x}{\sqrt{2}}\right) \tag{4.10}$$

$$\mathrm{erfc}(x) = 1 - \mathrm{erf}(x) = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-t^2}\, \mathrm{d}t \tag{4.11}$$

$$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2}\, \mathrm{d}t. \tag{4.12}$$

With these definitions, a brief discussion on the different possible modulation formats may begin. In digital modulation, there are three main sub-sets of modulation formats: phase-shift keying (PSK), frequency-shift keying (FSK), and amplitude-shift keying (ASK). In each of these modulation formats there are even further classifications which provide their own distinct advantages in disadvantages. This discussion, however, will be limited to the most basic cases of each sub-set.

1. FSK

FSK is one of the simplest forms of digital modulation. The basic idea is that the information is transmitted through a discrete frequency change of a carrier wave. The simplest form of FSK is binary FSK, or BFSK, where each transmission corresponds to a single bit represented by a "mark" (binary 1) or a "space" (binary 0). Assuming a carrier wave of f_c, a shift frequency of f_s and a digital bit value equal to $n = 0\,\text{or}\,1$, the general form of a BFSK signal is

$$s_b(t) = \sqrt{\frac{2E_b}{T_b}}\cos\left(2\pi\left[f_c + nf_s\right]t\right). \tag{4.13}$$

This result corresponds to a space and a mark signal of

$$s_{b,0}(t) = \sqrt{\frac{2E_b}{T_b}}\cos\left(2\pi f_c t\right) \tag{4.14}$$

$$s_{b,1}(t) = \sqrt{\frac{2E_b}{T_b}}\cos\left(2\pi\left[f_c + f_s\right]t\right) \tag{4.15}$$

respectively.

Following the analysis and discussion in [84], the probability of error of a BFSK signal may be given as

$$P_{b,PSK} = Q\left(\sqrt{\frac{2E_b}{N_0}}\right) = \frac{1}{2}\text{erfc}\left(\sqrt{\frac{E_b}{N_0}}\right). \tag{4.16}$$

The meaning behind the bit error probability is for a given signal to noise ratio (SNR) (or energy to noise) how likely one would detect an incorrect bit. So, if the probability of a bit error is 0.1, then it is likely that 1 out of every 10 bits will be incorrect. Therefore, depending on the communication standard or the allowable system error, a target SNR should be met to give the maximum allowable bit error probability.

2. PSK

Another digital modulation format which is often used is PSK. PSK gets its name from the fact that it adjusts the phase of the transmitted bits by a specified number. In the case of a binary PSK (BPSK) signal, the transmitted bits are sent with a phase shift of π to distinguish between a 1 and a 0. In a general BPSK system, the signal will appear as

$$s_b(t) = \sqrt{\frac{2E_b}{T_b}} \cos\left(2\pi f_c t + \pi\left[1 - n\right]\right),\ n = 0, 1. \tag{4.17}$$

This translates to a transmitted 0 and a transmitted 1 signal of

$$s_{b,0}(t) = \sqrt{\frac{2E_b}{T_b}} \cos\left(2\pi f_c t + \pi\right) = -\sqrt{\frac{2E_b}{T_b}} \cos\left(2\pi f_c t\right) \tag{4.18}$$

$$s_{b,1}(t) = \sqrt{\frac{2E_b}{T_b}} \cos\left(2\pi f_c t\right). \tag{4.19}$$

As before, one of the main concerns when choosing the modulation format is knowing the probability of an incorrectly transmitted bit. Thus, following the discussion in [84] again, the probability of a bit error for a BFSK signal may be determined to be

$$P_{b,FSK} = Q\left(\sqrt{\frac{E_b}{N_0}}\right) = \frac{1}{2}\mathrm{erfc}\left(\sqrt{\frac{E_b}{2N_0}}\right). \tag{4.20}$$

3. ASK

Another digital modulation technique is ASK. In ASK, the amplitude of the signal is varied to represent the different bits for transmission. How this is done totally depends on the system to be designed due to limitations of noise, power, pins, speed, etc. In this modulation scheme, the full-scale signal is divided into an equal number of levels to represent each bit level. Radio Frequency Identification (RFID) tags are a common system which typically employ an ASK modulator to backscatter the data from the tag back to the reader [85]. In these systems, a signal is transmitted to an

RFID tag which will then take the incoming energy and convert it to DC power and supply the entire tag chip. Then, data is read out of an on-chip EEPROM as bits and sent into the RFID tag's ASK modulator. This circuit will then adjust the input impedance of the RFID tag so that the amplitude of the reflected input signal will change depending on whether or not a 1 or a 0 is intended for transmission.

a. OOK

A subset of ASK systems is on-off keying (OOK). In this format, the data is transmitted at a fixed data rate. If a signal is present during a clock period this corresponds to a 1 and if there is no signal present during a clock period this corresponds to a 0. The general equation for an OOK signal is

$$s_b(t) = n\sqrt{\frac{2E_b}{N_0}}\cos\left(2\pi f_c t\right),\ n = 0, 1. \tag{4.21}$$

Again, following the analysis in [84] the probability of error for an OOK signal with two levels is

$$P_{b,OOK} = 2Q\left(\sqrt{\frac{2E_b}{N_0}}\right) = \text{erfc}\left(\sqrt{\frac{E_b}{N_0}}\right). \tag{4.22}$$

4. Modulation Choice

From the preceding discussions of PSK, FSK and OOK(ASK), it is seen that the main difference between these modulation formats is what is adjusted for representing the different bits. However, as seen from their respective probabilities of bit error, each of these modulation formats actually plays a large factor in the overall accuracy of the system. Therefore, the probabilities of error for each of these modulation formats is plotted in Fig. 38 as a function of energy per bit (E_b) and the noise floor (N_0). Although these show differing values, this does not tell the whole story. A PSK signal is one that can only be de-modulated coherently, meaning a carrier signal must be

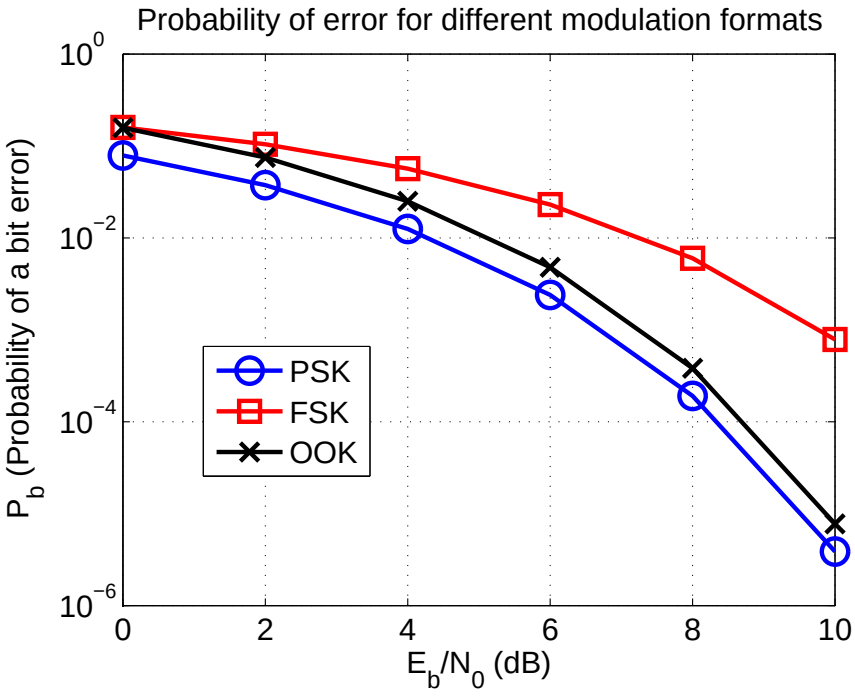

Fig. 38.: Probability of bit error for three different modulation formats.

used and must be detected in order to determine the values of a 1 and a 0. However, OOK and FSK signals may be de-modulated non-coherently because they do not require knowledge of the carrier in order to determine a 1 and a 0. This is because in each of these formats, the amount of energy in a given bandwidth can be detected to determine the values of a 1 and a 0. This means that, in the case of OOK there will be less energy when a 0 is transmitted and more when a 1 is transmitted. The same thing is true for a FSK signal since, in most cases, a higher frequency will be transmitted during one bit than the other. Therefore, determining the amount of energy in a given period will allow one to determine a 1 or a 0.

In addition to the need for carrier signal information, PSK systems are just more difficult to implement than OOK or FSK systems. Additionally, FSK is often superior to OOK systems in terms of de-modulation because it only requires information

about the bit period (T_b), whereas OOK de-modulators require information about the amplitude and bit period.

Although most of these drawbacks point to FSK as being the best choice for digital de-modulation, OOK still has many advantages over FSK in terms of **modulation** systems. Specifically, for the SHM wireless sensor system, the transmitted data will greatly effect the overall power consumption of the system. In the event that an FSK transmitter is implemented, regardless of whether or not the system is transmitting a 1 or a 0 the system will be dissipating power since FSK systems have a continuous output. However, an OOK transmitter will only dissipate power when a 1 is required. Therefore, since the probability of a bit error is relatively low for OOK signals and it also has the advantage of dissipating power only when a 1 is transmitted, this is the best choice for a self-powered wireless sensor system.

CHAPTER V

IMPULSE ULTRA WIDEBAND TRANSMITTER

For the proposed SHM system there has already been discussion and results presented on the energy harvesting material, AC/DC converter, the sensor and modulation format of the sensor data to be transmitted. Knowing the data will be transmitted using a digital modulation format, OOK, considerations about the circuitry to perform the data transmission must also be discussed. An introduction to ultra-wideband (UWB) technology will be discussed in this chapter and ideal candidates for implementation in the proposed SHM sensor system will also be presented.

A. Introduction

In 2002 the FCC opened the frequency band from 3.1-10.6 GHz for unlicensed use. Fig. 39 shows the FCC regulated spectral mask for indoor and hand-held ultra-wideband (UWB) emissions. Prior to the de-regulation of the UWB band, these frequencies were generally reserved for military radar applications and sub-surface sensing. However, there has been recent investigation in the past decade to utilize this frequency band for low-power sensor networks. The main issue one typically encounters when dealing with this frequency band is the expected power consumption of such a wideband system at a fairly high frequency compared to the typical sensor data. Although this is generally the case in systems which use a carrier signal to upconvert and transmit the baseband data, the sensor systems were typically avoiding the commonly power-hungry blocks of wideband mixers, power amplifiers, and frequency synthesizers by utilizing very narrow time-domain pulses which would then correspond to a wideband frequency signal.

Generating short time-domain pulses lends itself to two fundamental challenges:

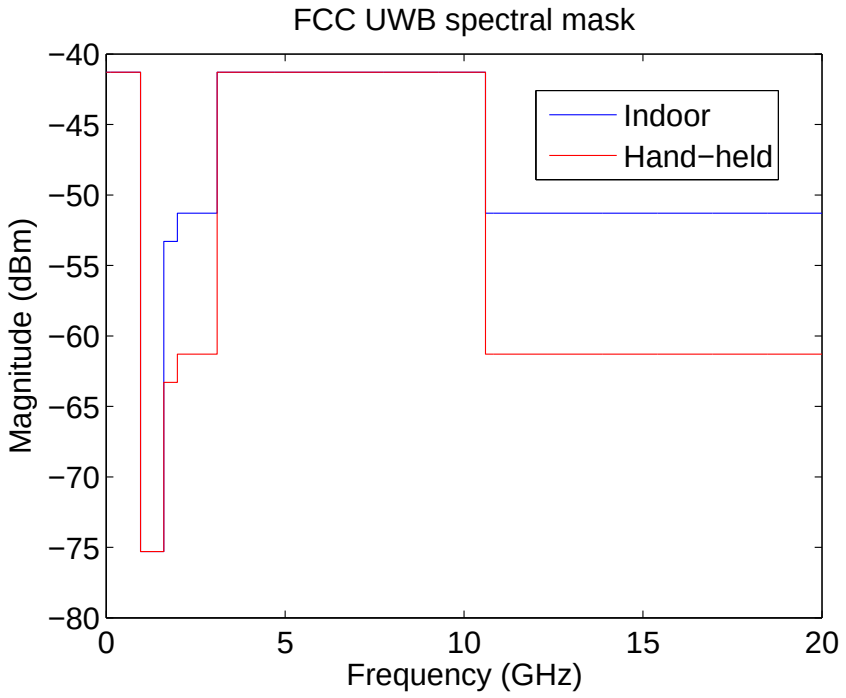

Fig. 39.: FCC UWB spectral mask for indoor and outdoor transmissions.

1) having components which are able to turn on/off and charge/discharge at the desired speed, and 2) what shape the pulses should take on. The main candidates which have been studied are square/rectangular, triangular, and Gaussian, to name a few. In general, Gaussian pulses are favored since they represent an exponential function which may be approximated by charging and discharging a capacitor. Therefore, a Gaussian pulse is assumed for the IR-UWB to be employed in the self-powered sensor system. The expression for a Gaussian pulse is

$$y(t) = \frac{A}{\sqrt{2\pi}\sigma} e^{-\frac{t^2}{2\sigma^2}} \tag{5.1}$$

where A is the amplitude, t is time, and σ is a constant related to the time constant of the system.

To better understand the application of the Gaussian pulse in the impulse radio

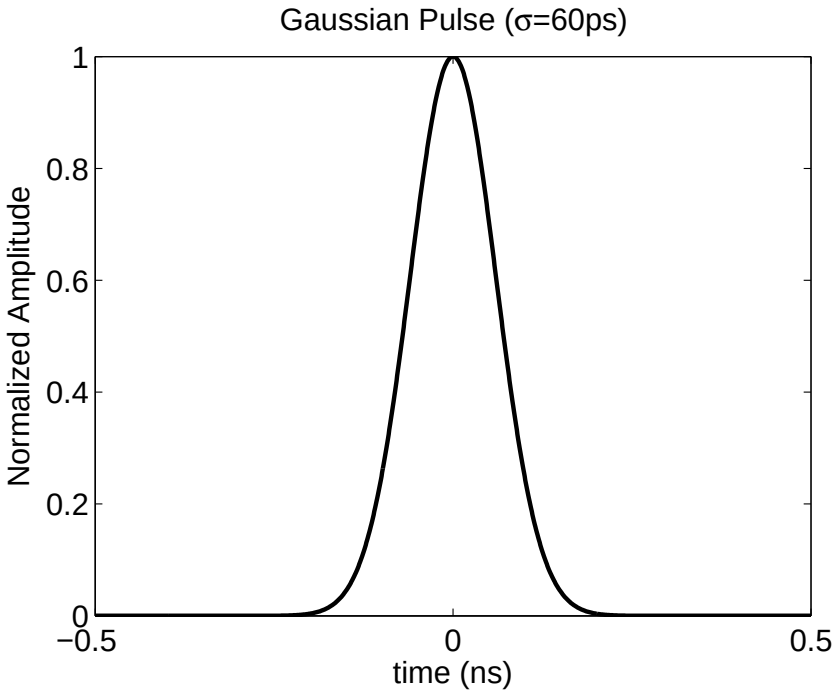

Fig. 40.: Normalized response of the Gaussian pulse $\sigma = 60$ps.

UWB (IR-UWB) system it is necessary to characterize the signal and its derivatives in both time and frequency domains. Using standard techniques, the 1^{st}, 2^{nd}, 5^{th} and 7^{th} derivatives of the Gaussian pulse may be obtained as

$$y^{(1)}(t) = -\frac{At}{\sqrt{2\pi}\sigma^3} e^{-\frac{t^2}{2\sigma^2}} \tag{5.2}$$

$$y^{(2)}(t) = A\left[\frac{t^2}{\sqrt{2\pi}\sigma^5} - \frac{1}{\sqrt{2\pi}\sigma^3}\right] e^{-\frac{t^2}{2\sigma^2}} \tag{5.3}$$

$$y^{(5)}(t) = -A\left[\frac{t^5}{\sqrt{2\pi}\sigma^{11}} - \frac{10t^3}{\sqrt{2\pi}\sigma^9} + \frac{15t}{\sqrt{2\pi}\sigma^7}\right] e^{-\frac{t^2}{2\sigma^2}} \tag{5.4}$$

$$y^{(7)}(t) = -A\left[\frac{t^7}{\sqrt{2\pi}\sigma^{15}} - \frac{21t^5}{\sqrt{2\pi}\sigma^{13}} + \frac{105t^3}{\sqrt{2\pi}\sigma^{11}} - \frac{105t}{\sqrt{2\pi}\sigma^9}\right] e^{-\frac{t^2}{2\sigma^2}}. \tag{5.5}$$

The plots of these signals represented by (5.1)-(5.5) are shown in Figs. 40, 41, 42, 43, and 44.

Although these equations are useful, it is also necessary to view the spectra of

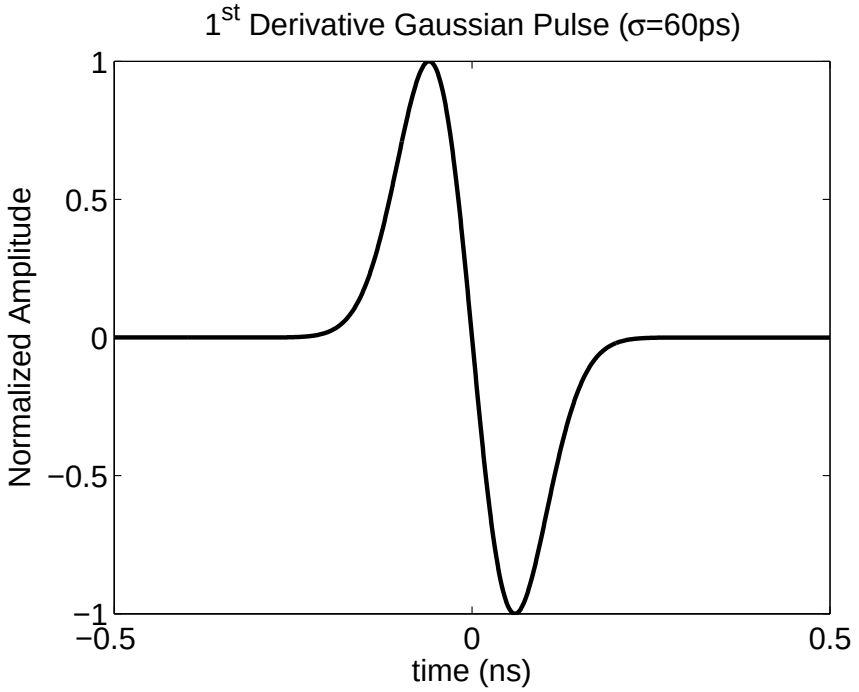

Fig. 41.: Normalized response of the Gaussian pulse 1^{st} derivative $\sigma = 60$ps.

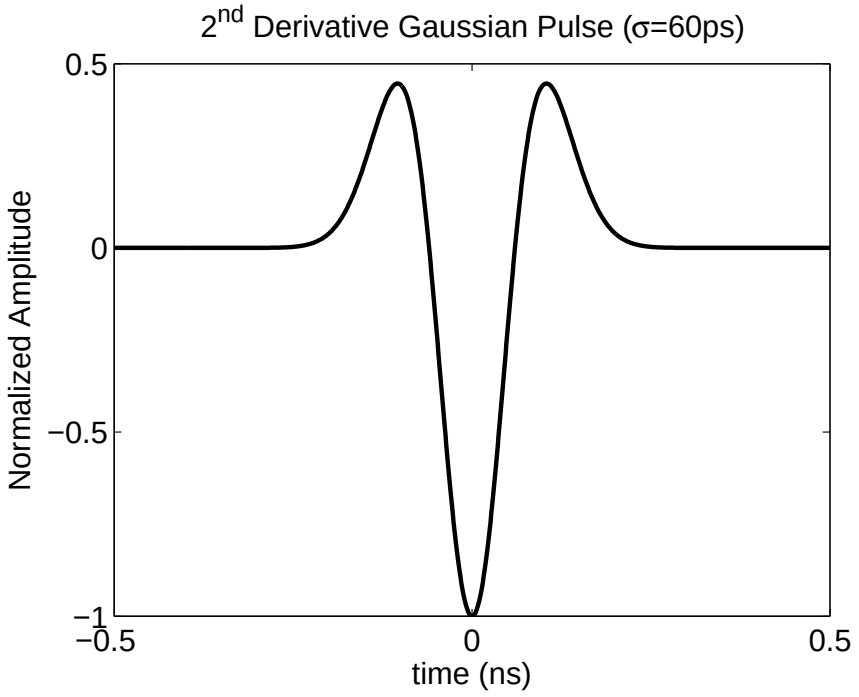

Fig. 42.: Normalized response of the Gaussian pulse 2^{nd} derivative $\sigma = 60$ps.

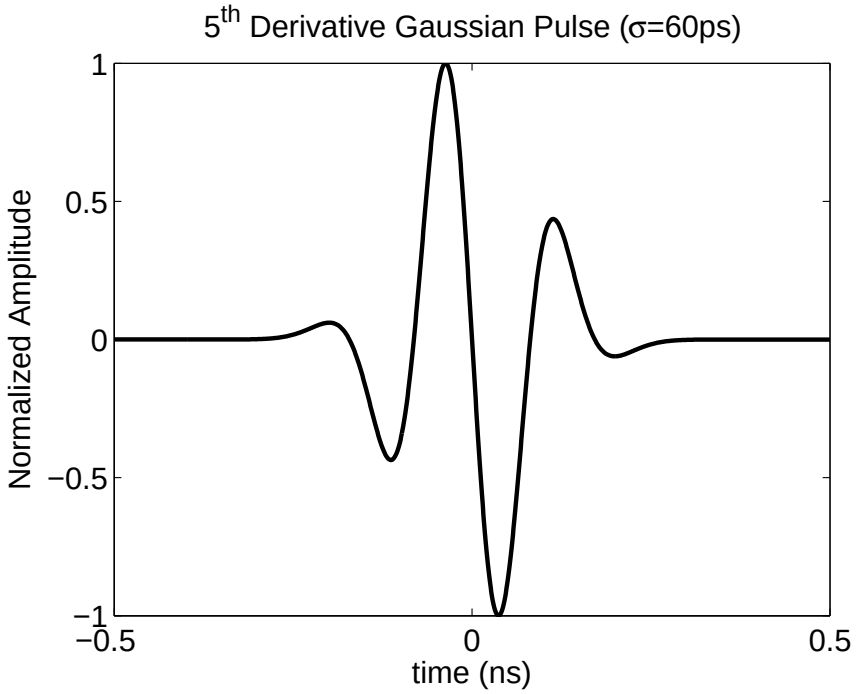

Fig. 43.: Normalized response of the Gaussian pulse 5^{th} derivative $\sigma = 60$ps.

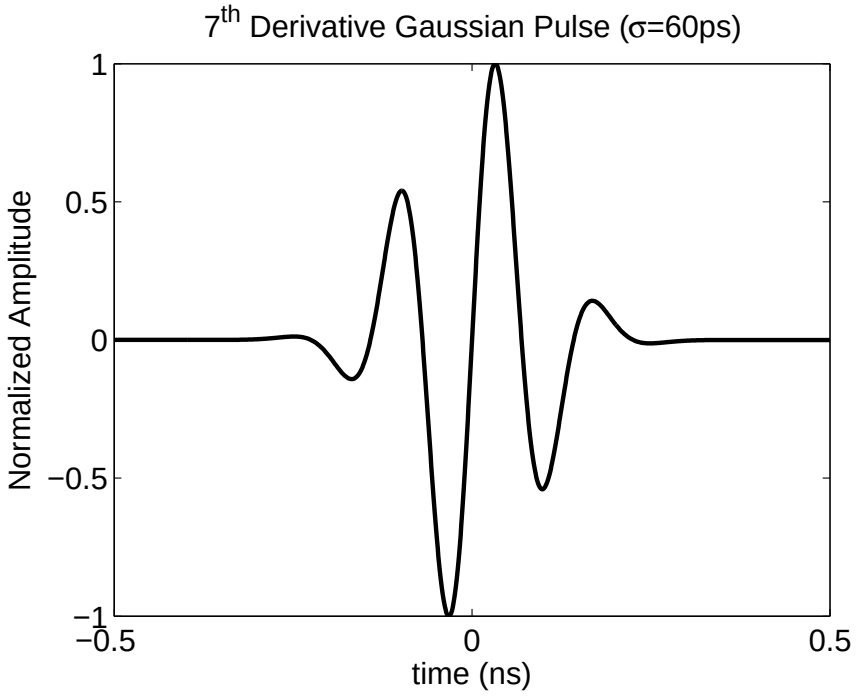

Fig. 44.: Normalized response of the Gaussian pulse 7^{th} derivative $\sigma = 60$ps.

these signals to determine which would be ideal candidates for deployment in an IR-UWB system. Therefore, the Fourier transform of $y(t) \overset{\mathcal{F}}{\rightarrow} Y(\omega)$ may be derived as

$$Y(\omega) = \int_{-\infty}^{\infty} y(t)e^{-j\omega t}\mathrm{d}t = \int_{-\infty}^{\infty} \frac{A}{\sqrt{2\pi}\sigma} e^{-\frac{t^2}{2\sigma^2}} e^{-j\omega t}\mathrm{d}t = \frac{A}{\sqrt{2\pi}\sigma} \int_{-\infty}^{\infty} e^{-\left(\left[\frac{t}{\sqrt{2}\sigma}\right]^2 + j\omega t\right)}\mathrm{d}t. \tag{5.6}$$

In order to compute the integral in (5.6), it is necessary to use the substitution method. However, before this can be done, it is necessary to complete the square in the argument of the exponential. To do this, the equation can be modified to facilitate the computation without changing the actual problem. Recalling a property of the exponential where $e^a e^{-a} = 1$ allows one to do this effectively. Currently, the argument of the exponential is in the form $(at)^2 + jbt$. The final form of the equation should be $(at)^2 + jbt + c$ such that this may be written as $[at + jd]^2$. Expanding this equation gives $(at)^2 + j2adt - d^2$. Based on this and viewing the current version of the spectrum one may see

$$2ad = \omega \tag{5.7}$$

$$d = \frac{\omega}{2a} = \frac{\sqrt{2}\sigma\omega}{2} \tag{5.8}$$

$$d^2 = \frac{(\sigma\omega)^2}{2}. \tag{5.9}$$

This implies $Y(\omega)$ may now be written as

$$Y(\omega) = \frac{A}{\sqrt{2\pi}\sigma} e^{-\frac{(\sigma\omega)^2}{2}} \int_{-\infty}^{\infty} e^{-\left(\left[\frac{t}{\sqrt{2}\sigma}\right]^2 + j\omega t\right)} e^{\frac{(\sigma\omega)^2}{2}}\mathrm{d}t \tag{5.10}$$

$$= \frac{A}{\sqrt{2\pi}\sigma} e^{-\frac{(\sigma\omega)^2}{2}} \int_{-\infty}^{\infty} e^{-\left(\left[\frac{t}{\sqrt{2}\sigma}\right]^2 + j\omega t - \left[\frac{\sigma\omega}{2}\right]^2\right)}\mathrm{d}t \tag{5.11}$$

$$= \frac{A}{\sqrt{2\pi}\sigma} e^{-\frac{(\sigma\omega)^2}{2}} \int_{-\infty}^{\infty} e^{-\left(\frac{t}{\sqrt{2}\sigma} + j\frac{\sqrt{2}\sigma\omega}{2}\right)^2}\mathrm{d}t. \tag{5.12}$$

Using a change of variables such that $u = \left(\frac{t}{\sqrt{2}\sigma} + j\frac{\sqrt{2}\sigma\omega}{2}\right)$ and $\mathrm{d}u = \frac{1}{\sqrt{2}\sigma}\mathrm{d}t$ and recognizing the integral becomes $\sqrt{\pi}$, the equation for the Gaussian spectrum may then be written as

$$Y(\omega) = \frac{\sqrt{2}A\sigma}{\sqrt{2\pi}\sigma} e^{-\frac{(\sigma\omega)^2}{2}} \overbrace{\int_{-\infty}^{\infty} e^{-u^2}\mathrm{d}u}^{=\sqrt{\pi}} = Ae^{-\frac{(\sigma\omega)^2}{2}}. \tag{5.13}$$

This is an interesting phenomenon to note since the spectrum of a Gaussian function is also a Gaussian function.

While it may be possible to find the spectra of the derivatives of the Gaussian function, it may be tedious to do this analytically or it may be fairly complex to do so as was done with the Gaussian function. Instead, one may utilize a property of the Fourier transform which states the derivative in time is equal to a multiplication by $j\omega$ in the frequency domain. Stated formally,

$$\frac{\mathrm{d}}{\mathrm{d}t}y(t) \xrightarrow{\mathcal{F}} j\omega Y(\omega). \tag{5.14}$$

Therefore, since the Fourier transform of the Gaussian signal was previously obtained, the remaining spectra may be determined from this result.

$$Y^{(1)}(\omega) = j\omega Y(\omega) = j\omega Ae^{-\frac{(\sigma\omega)^2}{2}} \tag{5.15}$$

$$Y^{(2)}(\omega) = (j\omega)^2 Y(\omega) = -\omega^2 Ae^{-\frac{(\sigma\omega)^2}{2}} \tag{5.16}$$

$$Y^{(5)}(\omega) = (j\omega)^5 Y(\omega) = j\omega^5 Ae^{-\frac{(\sigma\omega)^2}{2}} \tag{5.17}$$

$$Y^{(7)}(\omega) = (j\omega)^7 Y(\omega) = -j\omega^7 Ae^{-\frac{(\sigma\omega)^2}{2}}. \tag{5.18}$$

A plot of these functions is shown in Fig. 45. Although a σ of 60ps is small, it may be possible to generate this signal in a modern process making the higher order derivatives feasible. It should be noted that, for this value of σ, although the 5^{th} and 7^{th} derivatives meet the FCC requirement, in a practical sense the 5^{th} order

term may violate the mask if noise and PVT considerations are taken into account, unless one performs good design and layout practices when implementing the chip as well as insuring robust performance to PVT. Otherwise, a 7^{th} order derivative should be employed since this signal has more tolerance to variations but would be more expensive in terms of components due to the need of two additional derivatives.

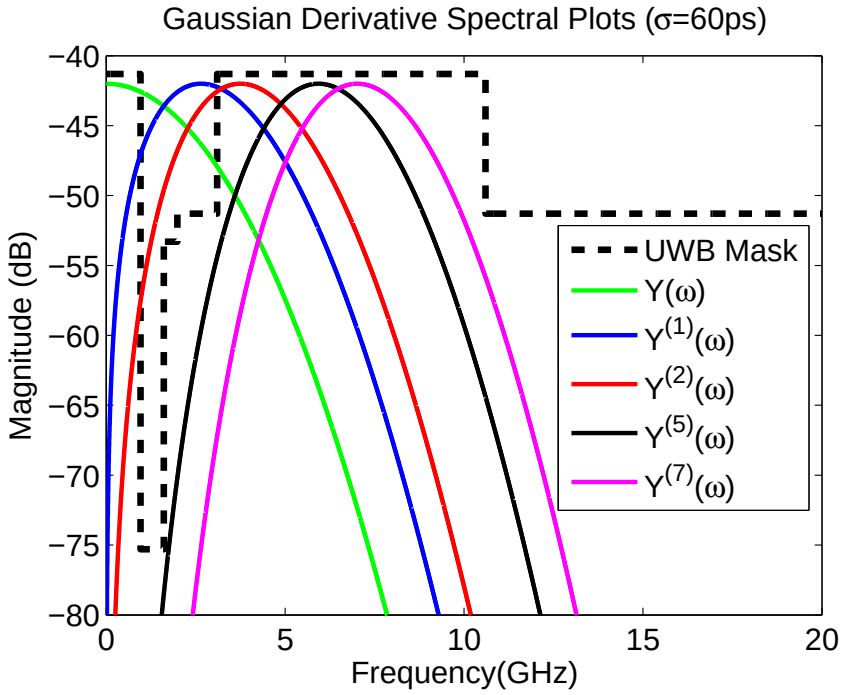

Fig. 45.: Normalized spectra of the Gaussian pulse and its 1^{st}, 2^{nd}, 5^{th} and 7^{th} derivatives and the UWB spectral mask provided by the FCC.

It should also be noted that, in most wireless transmissions, the antenna will perform an additional derivative to the signal which should be transmitted. Therefore, for an N^{th} derivative Gaussian IR-UWB TX one only needs to generate $N-1$ derivatives using circuit components and the final derivative will be taken by the antenna.

B. Application in Sensor System

Previously it was mentioned the data collected from the sensor would be wirelessly transmitted to a central processing location. While there are many ways to do this, there are also many methods which are inappropriate for applications in low-power systems. It has been shown one leading candidate for applications in low-power sensor networks are UWB transmitters [86].

UWB systems have been in use for many years but have garnered a greater attention since the FCC allocated the UWB spectrum for unlicensed use in 2002. Until this time, most applications were limited to radar and other imaging applications. After the FCC allowed unlicensed use of this spectrum, much research went into developing large-bandwidth, high data rate systems for wireless personal area networks (WPANs). However, additional research was done utilizing the frequency spectrum to create large-bandwidth, low data rate systems.

Although at first glance it seems strange that these two paths were taken utilizing the same frequency spectrum, the main difference came in the way data was encoded and transmitted (or conversely, received and decoded). For many of the high data rate applications, it was assumed the frequency spectrum was divided into many smaller sub-bands with equal bandwidths of 528MHz. Within these sub-bands there were 128 channels with different information placed in each channel. Implementing the sub-bands implied needing a wideband frequency synthesizer to generate the required tones to down-convert the signal for further processing. Although this method can be efficient and can be fairly robust, the need to encode the information using complex techniques as well as at least one frequency synthesizer to up/down-convert the signal caused large power consumptions and is not suitable for a sensor system.

The second implementation of a UWB system for low data rate systems achieves

a wideband signal differently. In this application, very short time-domain pulses are generated which corresponds to a large bandwidth in the frequency domain. However, there are many different methods of generating pulses for an impulse radio-UWB (IR-UWB) transceiver, some of these methods are more energy efficient than others while others are more easily implemented [86–88].

1. Previous Solutions

In [86] an IR-UWB transceiver is designed and fabricated using a 90nm CMOS process. This architecture was designed and implemented with the intent of transmitting up to 5Gb/s of information. The system utilized an OOK-modulated impulse generator for data transmission. The system obtained an overall power consumption of 9mW where 3mW of the overall power was allocated for the transmitter.

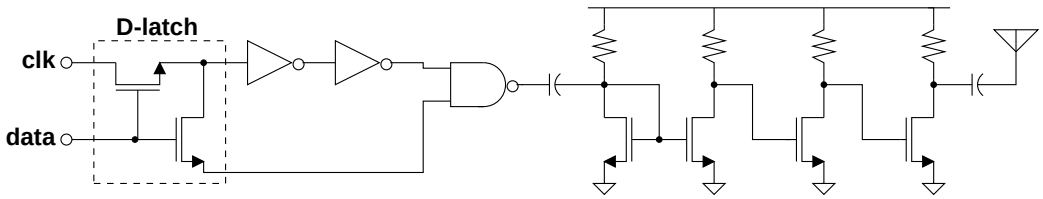

Fig. 46.: Impulse radio UWB TX from [86].

In [87] an IR-UWB TX was fabricated and had an overall system architecture shown in Fig. 47. The output of the LC-VCO was directly connected to the antenna for signal transmission. The data was directly input into one input of an AND gate while the same data was also input into a 3 stage delay line consisting of inverters. The load capacitance of the inverters and AND gate were all controlled via a tuning voltage to vary the amount of delay within the system. The output of the AND gate would then be short pulses due to the operation of the AND function which

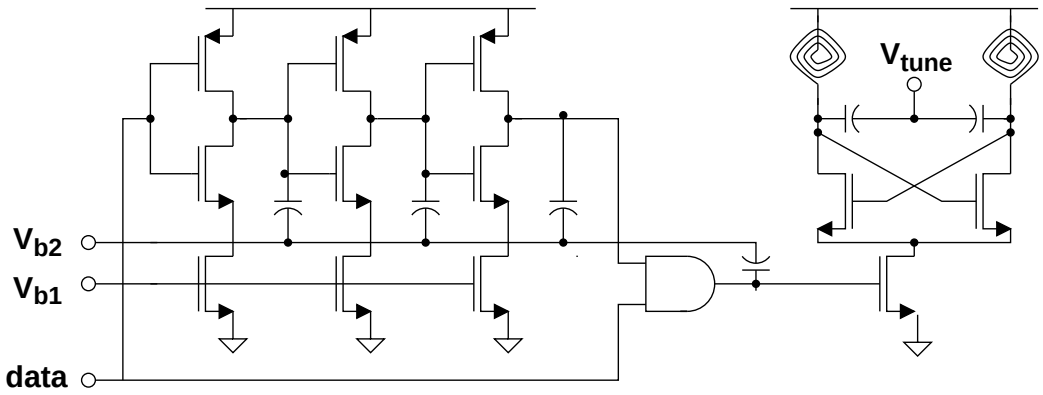

Fig. 47.: Impulse radio UWB TX from [87].

then controlled the switch which controlled the VCO. With the switch activated, the sinusoidal output of the second order system (the LC-VCO) would then begin to rise with an exponential envelope. When the tail switch is disconnected due to the AND gate output going low, the sinusoidal output of the VCO would then decay at an exponential rate. This system then emulated the desired Gaussian function and provided a relatively low power consumption of 236μW with a 1.8V V_{dd} at a pulse-repetition-rate (PRR) of 2Mb/s in a 0.18μm CMOS process.

In [88], another LC-VCO based IR-UWB TX was fabricated and is shown in Fig. 48. This systems operation is fairly similar to the one of [87], however this system has two main modifications. First, this circuit assumed a baseband processor would be available to provide a clock to the AND gate as opposed to relying on a delayed ANDing of the data with itself, and secondly it implemented two switches during disconnect to stabilize the output to a fixed quantity when not transmitting and placed a series switch with the tail current source to have a constant current system. At a PRR of 100kHz, this system consumed only 1.2μA of dynamic current from a 1.5V supply voltage in a 0.18μm CMOS process. While this is a low power system, the necessity of having a clock to drive the AND gate limits its application

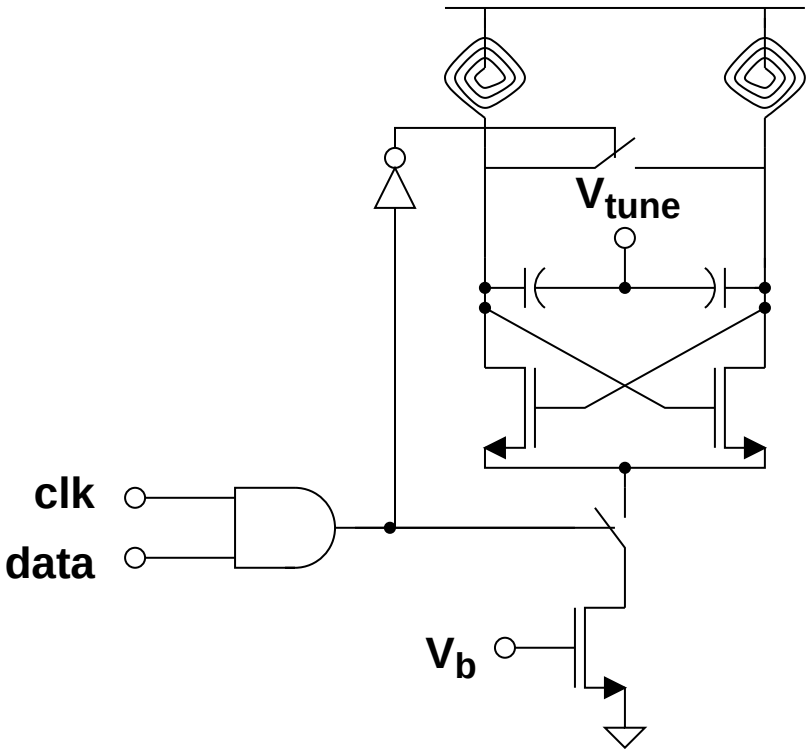

Fig. 48.: Impulse radio UWB TX from [88].

in a sensor network. However, the results are promising and this system is a viable candidate for deployment in the proposed sensor system.

Recently, studies have been performed on changing the envelope shape of the signal which generates the impulses [46, 89]. The main concept behind the pulse generation in these works is shown in Fig. 49. In this system, a ring oscillator with two different enable capabilities is used to drive the gate of an antenna amplifier. The signal shown as $\overline{SHAPE}$ is implemented such that the output of the inverter is approximately equal to a triangle. The authors show how under nominal conditions a sinusoidal signal which generates a triangular output that is shown to fit the FCC UWB mask better than a Gaussian signal. The overall system consumes 5.7μW at 100kb/s PRR from a 0.5V supply. Although the system in [46, 89] is strictly a pulse generator, the system may be modified by using the binary data from the ADC in the

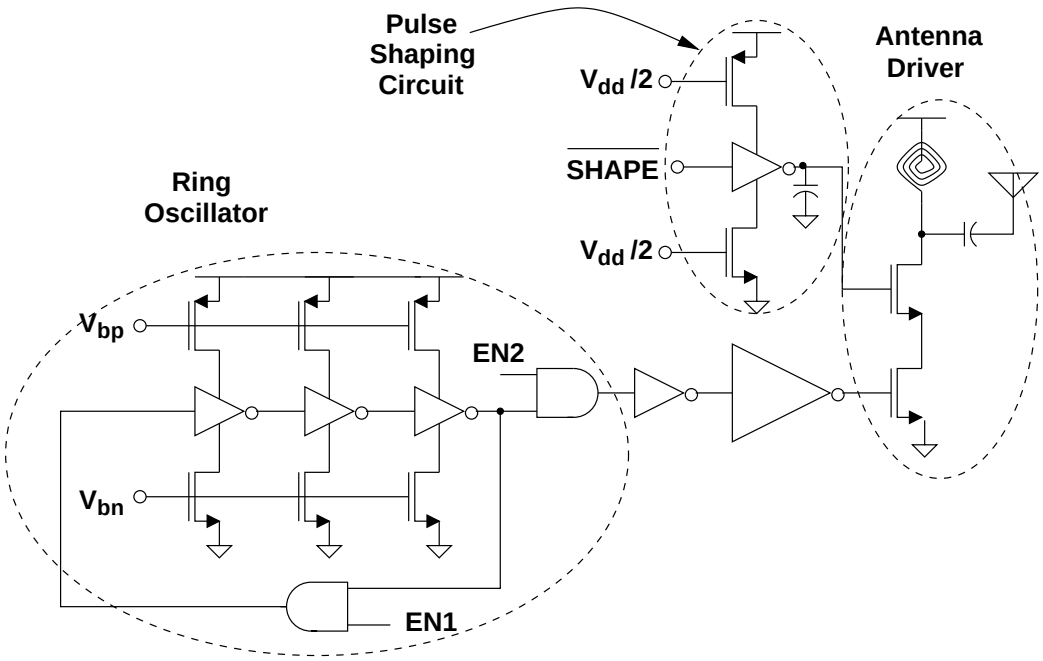

Fig. 49.: Impulse radio UWB TX from [46].

proposed sensor network to control the $SHAPE$ function. This would then perform the desired OOK function without adding circuitry to this system. Additionally, the system shown in Fig. 49 operates from a low supply voltage and consumes extremely low power in a 90nm CMOS process.

C. Conclusions

Although there are many different techniques for implementing an IR-UWB TX and many methods for generating an FCC compliant impulse, the constraint of low complexity, low power, and being robust take priority over most other challenges. Therefore, it is assumed that a transmitter similar to Fig. 49 is implemented to drive the antenna and provide an overall low system level power consumption.

CHAPTER VI

LOW-VOLTAGE LOW-POWER SUCCESSIVE APPROXIMATION ADC[2]

For the proposed sensor system shown in chapter 1, a large challenge was generating a large enough DC voltage/power for the circuitry required in the system and this was addressed in chapters 2 and 3. Knowing the modulation format for the data to be transmitted, as discussed in chapters 4 and 5, now leaves room for discussion and implementation of another major component of the proposed system, the analog-to-digital converter (ADC). This block is necessary in order to convert the analog output from the sensor into a digital signal for modulating the IR-UWB TX while consuming low power (on the order of a few tens or hundreds of microWatts). In this chapter, a discussion on different ADC topologies will be conducted and conclusions will be drawn as to which architecture will be best-suited for the proposed sensor system. Simulation and measurement results of the proposed low-power ADC will be presented from a prototype designed in a standard 0.5μm CMOS process.

A. Introduction

In sensor networks, the information which must be transmitted is slow (i.e., low data rate) compared to other wireless networks (cell phones, media, etc.). Therefore, one is

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not typically as concerned with speed as they are with the overall power consumption to perform the desired conversion. The concern with power consumption is mainly because there are 1 to a few 100, or even 1,000s, sensor motes in a given location. Assuming a wireless sensor mote, it very cumbersome to change the batteries of every unit regularly. This is why, for most sensor applications, a low-data rate, low-power ADC is employed. The best-suited topologies are typically Integrating ADCs (single or dual slope) and Successive Approximation Register (SAR) ADCs. For a bit count greater than 4-5, these architectures are more energy efficient than other ADCs, such as Flash or $\Sigma\Delta$ [90].

B. Low-Power ADCs

1. Integrating ADC

Integrating ADCs (IADCs) are typically implemented as single-slope or dual-slope ADCs. In a single-slope architecture, the sampled input signal is applied to an integrator and compared to a known reference voltage. The amount of time taken to reach the reference level is then read out as the digital value of the input. Once the sampled signal is larger than the reference, the integrator is reset, the input signal is sampled again, and the conversion process begins again. The operation of this ADC is extremely simple, in theory, and may be designed fairly easily. The major drawback of this architecture is that the integration time is completely dependent on the accuracy of the R and C used to implement the integrator. Additionally, the reference voltage applied to the comparator must be extremely stable and well-known, otherwise this results in a large number of bit errors.

A solution to the issues in the single-slope architecture is found by using a dual-slope architecture. The conversion cycle begins much like in the single-slope architec-

ture, however instead of integrating until the input is equal to a reference voltage, the input voltage is integrated for a predetermined amount of time (i.e., M clock cycles). After the input integration is complete, the ADC then applies a well-known reference level and "de-integrates" for an unknown amount of time that is tracked using a counter. The main improvement here, compared to the single-slope architecture, is the errors due to the absolute value of the R and C used appear in the integration and de-integration phases. Thus, the errors due to these values are eliminated and the major design concern lies within designing clock signals which are more accurate (jitter) than the required ADC resolution.

Assuming ideal opamps and components, the equation defining the output of the integration stage is

$$i_{in} = \frac{V_{in}}{R} = -\frac{1}{C}\int V_c \, \mathrm{d}t. \tag{6.1}$$

During the integration and de-integration phases, the areas of the triangles created by the ramp up and ramp down must be equal due to the law of conservation of charge. Therefore, one may say

$$\frac{1}{2}V_{in}T_{int} = \frac{1}{2}V_{ref}T_{de-int}. \tag{6.2}$$

From here we can see that the value of

$$T_{de-int} = T_{int}\frac{V_{in}}{V_{ref}}. \tag{6.3}$$

The dual slope architecture is a vast improvement for determining the value of V_{in} since the resulting output is dependent on a ratio. Still, this architecture requires the use of at least two analog comparators as well as a few counters for converting the input level into an output code. The basic idea and a low-level implementation of the Single and Dual Slope Integrating ADCs are shown in Fig. 50. Additionally, the main drawback of the IADC architecture is the inherent need to integrate for a

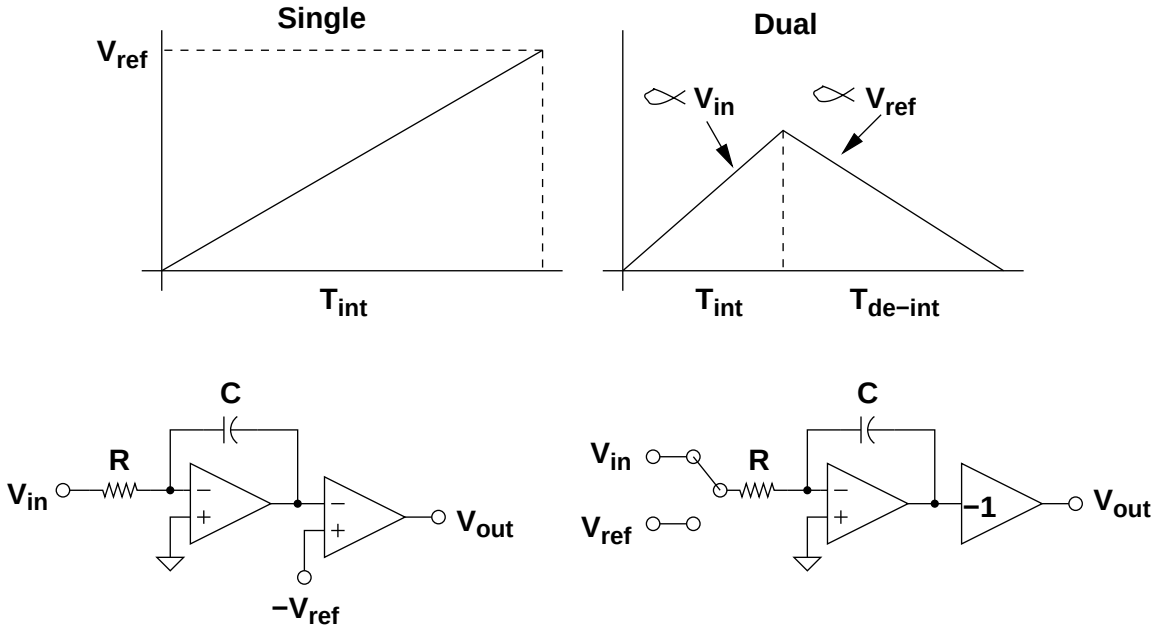

Fig. 50.: Principle of single and dual-slope IADCs.

maximum of 2^N, where N is the number of ADC bits, clock cycles to perform a single conversion.

2. Successive Approximation Register ADC (SAR ADC)

Another class of low-power ADCs is the Successive Approximation Register ADC (SAR ADC). This architecture may be classified in the counting ADC category, but provides a greatly reduced conversion time compared to the single and dual-slope IADCs. A SAR ADC takes an initial guess at the sampled input value by using a binary search algorithm to determine an estimate of the input signal using an internal digital-to-analog converter (DAC). Another way of viewing a SAR ADC is it is a feedback system which, on successive clock cycles, provides an adaptive reference voltage to a comparator which then determines whether or not the sampled value is greater than or less than the estimate. Based on the comparator output in a given clock period, each bit, beginning with the MSB of the ADC, is then read out

and stored for further processing until the conversion process begins again. The basic architecture of a SAR ADC is shown in Fig. 51. These structures have been typically

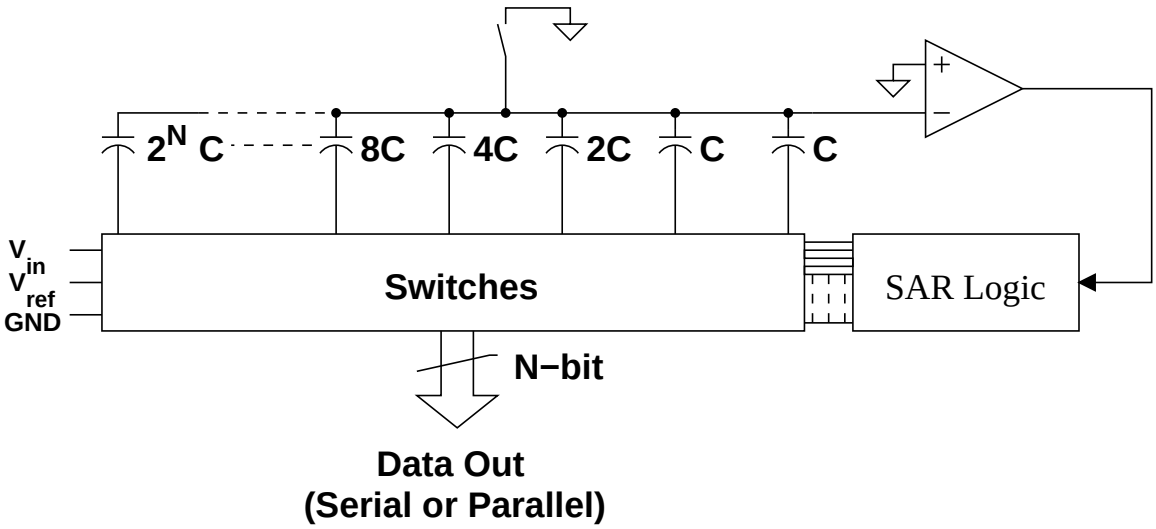

Fig. 51.: Top-level view of a SAR ADC.

used for high precision and low-power applications [91, 92]. The overall architecture consists of an input sampling stage (either stand alone sample-and-hold (SAH) stage or having the SAH incorporated into the DAC), a DAC, a comparator, and logic. While any DAC may be used in a SAR ADC (resistor string, current steering, etc.), for low-power ADCs a capacitive DAC is generally implemented due to its lower overall power consumption compared to current steering or voltage division DACs. For large bit counts (greater than 6 or 8 bits), the DAC array may be segmented to reduce component size or it may evolve into a hybrid architecture where some of the bits are comprised of capacitors and others come from a resistor string. One of the main advantages of the capacitive DAC is the SAH circuit may be implemented within the DAC, thereby providing better matching between the compared voltages [93].

Unlike IADCs which potentially take 2^N clock cycles per conversion, SAR ADCs

make an initial estimate of the sampled input. Then, the sampled value and the estimate are compared. If the sampled value is larger than the estimated value, the bit is kept and the next bit is then set high for comparison with the sampled input. If the sampled value is lower than the DAC value, the bit that was just set is thrown out and the next bit is set for comparison. This continues until all bits have been utilized in the comparison process (N clock cycles), then the DAC is reset, the input is sampled again, and the digital estimate is read-out. The DAC voltage estimated by the SAR ADC is given by

$$V_{DAC} = V_{ref} \frac{\sum_{i=1}^{N} B_{N-i} 2^{N-i}}{2^N}. \tag{6.4}$$

Figure 52 gives an overview of the binary search algorithm which is typically implemented in SAR ADCs. Although this is still not as fast as a flash or $\Sigma\Delta$ architecture, the SAR ADC is very simple to implement and is well-suited for low-power, relatively low-speed applications. For the proposed SHM sensor network, the SAR ADC is an ideal candidate due to the low input frequency from the bridge oscillations (on the order of 10-20Hz in most cases) as well as the necessity to use very low-power and implement a low-complexity system. The maximum input frequency, to avoid aliasing, of a SAR ADC is given by

$$f_{in,max} = \frac{f_{clk}}{2\left(N + \alpha\right)} \tag{6.5}$$

where α is an integer value and is typically either 1 or 2 and represents additional clock cycles used for resetting the SAR logic, sampling the input signal, and any other operations which need to be performed prior to starting the conversion process again. This equation is a modification of the Nyquist criterion where typical data converters have a maximum input frequency equal to $f_{clk}/2$. The additional reduction in input bandwidth is attributed to the number of clock cycles required to obtain a digital

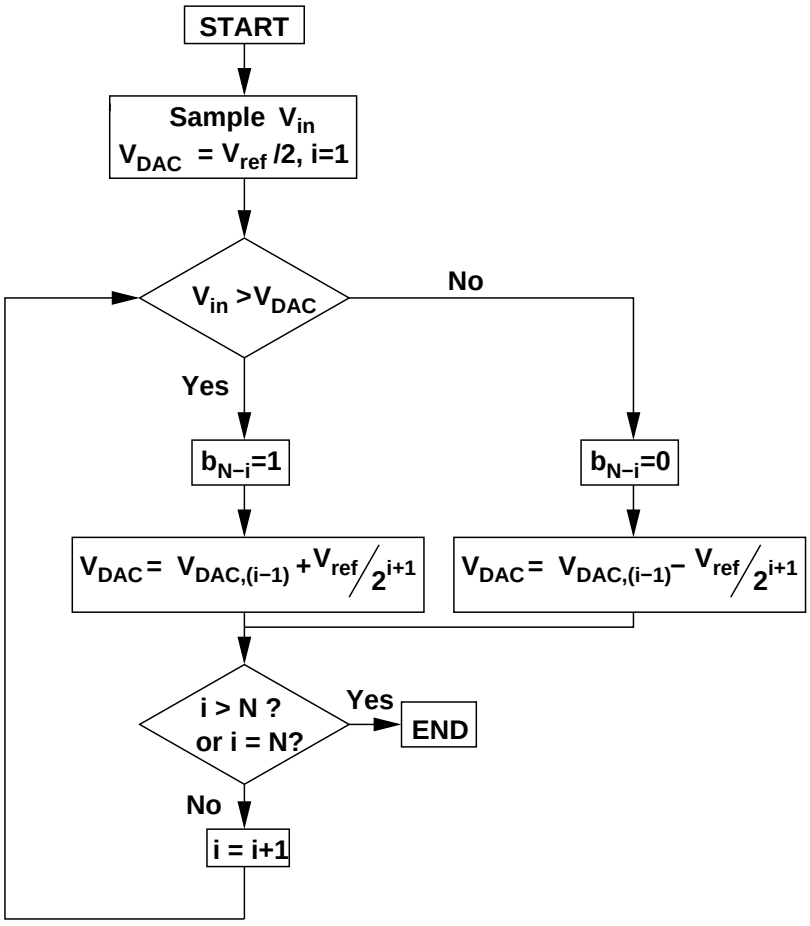

Fig. 52.: Binary Search Algorithm.

output (N clock cycles) as well as α. To help avoid any issues which may occur during sampling or resetting, the proposed SHM SAR ADC uses $\alpha = 2$.

C. SAR ADC Design

Two design parameters which must be chosen are the clock frequency of the ADC and the required ADC resolution. From (6.5) there is a maximum allowable input frequency before aliasing occurs for a given clock frequency and ADC bit number. For bridge monitoring an input frequency up to at least 20Hz must be tolerated to account for the natural vibration frequency. However, this value is the lower limit

for the clock frequency. To obtain the upper limit for the clock frequency, one must make an estimate of the overall power consumption of the circuitry. However, this cannot be done until the number of ADC bits is defined from the targeted accuracy. Having a larger clock frequency will allow for a faster conversion and for a larger input bandwidth, but is detrimental to the overall power consumption. This is seen when one views the power consumption of a digital circuit switched at a frequency of f_{clk}, which is approximately given by

$$P_{dig} = \lambda C_{tot} V_{dd}^2 f_{clk} \tag{6.6}$$

where λ is a constant and is usually equal to $1/2$, C_{tot} is the total capacitance being charged or discharged during a clock cycle, and V_{dd} is the supply voltage of the circuit being clocked. From (6.6) increasing the clock frequency directly increases the dynamic power of a single digital circuit. Once the number of bits is selected, an estimate of the overall number of gates may then be performed and an overall power consumption may be estimated from this equation, the estimate of C_{tot} and V_{dd}. Since there is a limited power budget for the wireless sensor network, there is also an upper limit for the clock frequency. Additionally, to reduce power consumption and also the required clock frequency, a lower number of bits would be desired. However, doing so will limit the accuracy of the analog-to-digital conversion and would not yield a result which would be accurate enough.

Assuming a V_{dd} of $1V$, the LSB size of the ADC may be given by

$$LSB = \frac{V_{dd}}{2^N}. \tag{6.7}$$

As N increases, the LSB size decreases logarithmically and the need for calibration circuitry will arise to overcome offsets which would appear in the comparator. More discussion on considerations for choosing N will be discussed in the following sec-

tion. From these descriptions, it is apparent there is a maximum limit for N to help minimize system complexity and, therefore, power consumption of the overall ADC. However, if N is reduced too far, another issue arises due to the inability to detect changes in the external stimulus. To determine the actual requirement for the required number of bits, N, and therefore the required clock frequency, a few assumptions and realizations must be discussed.

1. Number of Bits

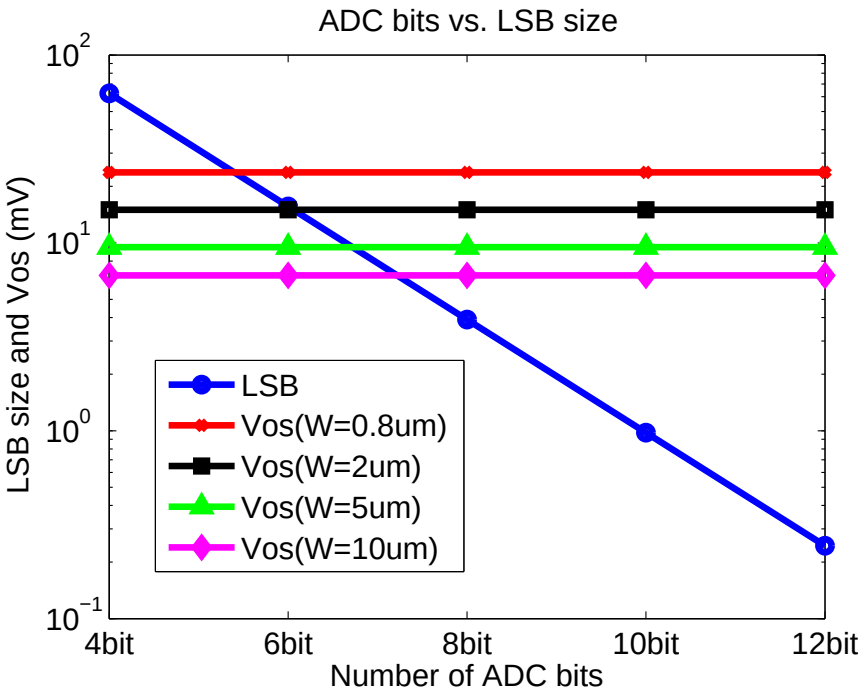

Fig. 53.: ADC LSB size and NMOS transistor input referred offset voltage for 0.5μm CMOS and minimum length device.

N is an important designation in the overall system design. Too few and one is not able to accurately determine the state of the bridge. Too many and the power consumption and cost (monetary, complexity, power, etc.) of the system will increase

drastically. So, one observation about the structure of the sensor is made first. Since a Wheatstone bridge is used for determining the strain applied the bridge, this structure may be viewed as a voltage divider. Ideally, the output of the balanced Wheatstone bridge is equal to zero with each corresponding output being equal to $V_{ref}/2$. When a strain appears on the bridge at or near the location of the sensor, the voltage difference between a standard resistive voltage divider and a voltage divider comprised of a standard resistor and a strain gage is proportional to the applied strain. Although the sensed voltage difference is small, this value is applied to the sample and hold circuitry via a low-pass filter whose output is centered around $V_{ref}/2$. As the strain increases, the voltage difference will then increase as well, thus causing the sample and hold stage to see a larger and larger deviation from $V_{ref}/2$. If the difference in the fixed voltage of the Wheatstone bridge and the strain gage section of the Wheatstone bridge becomes greater than $V_{ref}/2$, one would typically be concerned with saturating the sensor. However, if the applied force to the system is this large, then damage would likely be incurred and this would send a flag that the civil infrastructure is damaged and someone should investigate the issue.

Regardless of what sensor is employed in the final design, it is assumed the majority of the sensor outputs will be centered around $V_{ref}/2$ which means the system must have a good enough resolution to detect more than 2 levels, thus requiring at least 2 bits to obtain more than 2 levels. To determine the maximum number of bits, it is best to determine the maximum tolerable power consumption as well as whether or not it is necessary to implement calibration circuitry to correct offset from the comparator. Since, for power purposes, offset calibration circuitry should be minimized or avoided altogether, the limit of the 3σ variation of the comparator offset voltage is set to less than 1/2LSB. This may be determined using process characterization plots and statistical analysis. The expected value of the offset of an

NMOS transistor due to threshold voltage variation in 0.5μm CMOS may be obtained from

$$\sigma_{V_{th}} \approx \frac{A_{V_{th}}}{\sqrt{WL}} \,(\text{mV}). \tag{6.8}$$

The value of $A_{V_{th}}$ may be taken from process characterization and is approximately 20-30mv·μm for a 0.5μm technology. From here, a plot is generated, assuming minimum length devices, for the input referred offset of the device for various transistor widths. Additionally, the LSB size for different ADC bit numbers is plotted for comparison. Figure 53 shows the results of this plot. Although this plot is not 100% accurate, it does give insight into the selection of N as well as sizing the input stage of the comparator. For resolutions larger than 7 bits the LSB size becomes smaller than the expected value of the input offset voltage due to V_{th} mismatch of the devices plotted. Therefore, to avoid offset correction circuitry or extremely large devices, the maximum size (W) of all unit devices is limited to a maximum of 10μm. This limit also sets an upper limit for avoiding calibration circuitry of approximately 6 bits (i.e., $N = 6$). The required number of bits for the ADC with the given constraints are then set between 2 and 6 to keep power consumption at a moderate level, allow for the bandwidth of the input signal while minimizing the clock frequency, and avoiding the use of offset calibration circuitry. To obtain the best resolution for the given specifications, N is set at to its maximum value of 6.

With the number of bits set at 6, the minimum clock frequency required to obtain a bandwidth of at least 20Hz is

$$f_{clk,min} \geq f_{in} \times 2(N+2) = 20 \times 2(6+2) = 320\,\text{Hz}. \tag{6.9}$$

We see that even with the largest bit size allowable before calibration is required, this clock frequency is still very low and will help keep the overall power consumption very

low. Assuming that $V_{dd} = 0.8\text{V}$, $C_{tot} = 1\text{nF}$, $f_{clk} = 1\text{kHz}$ and $\lambda = 0.5$, the dynamic power dissipation is approximately

$$P_{dyn} = \frac{1}{2} \cdot 10^{-9} \cdot 0.8^2 \cdot 1000 = 320\,\text{nW}. \tag{6.10}$$

Although this is a fairly low value, this is assuming an equivalently low V_{dd} for

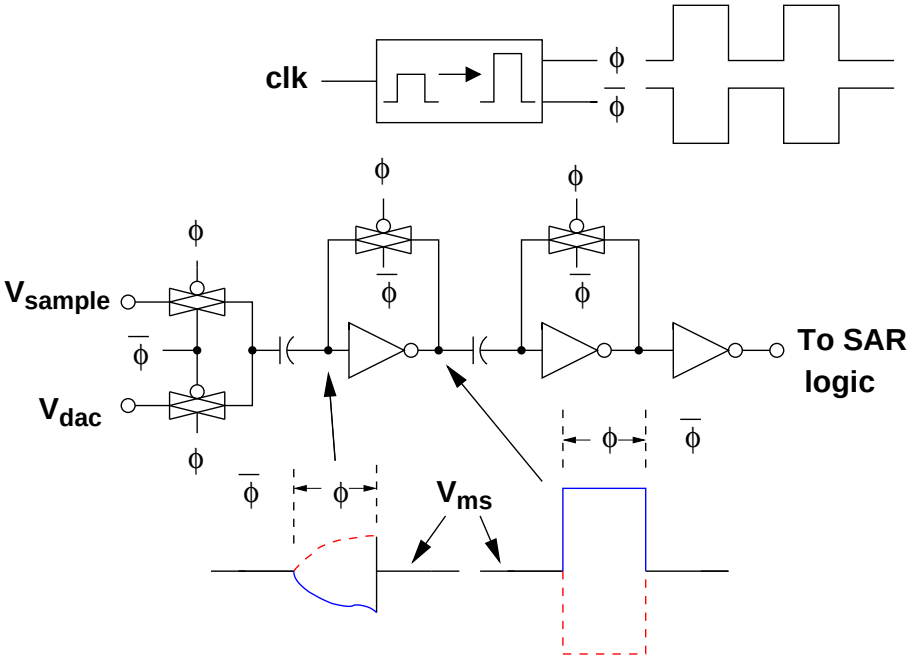

Fig. 54.: Low-voltage Low-power Inverter Based Comparator.

the given process, a large total capacitance C_{tot} of 1nF instead of a more reasonable 100pF value, and a clock frequency which is 3× its minimum were used for the calculation. However, this estimate may be viewed in a different way. The dynamic power of a single gate is given as $\lambda C_{tot} f_{clk} V_{dd}^2$. For P total gates in the system, the dynamic power may then become $\lambda P C_{tot} f_{clk} V_{dd}^2$. Since a 6 bit ADC is desired for this work, this implies a fairly large gate count for implementing the SAR logic since approximately $2(N+\alpha)$ D flip-flops (DFF) are used to implement the control logic. If

a more reasonable V_{dd} estimate of 2V is assumed, C_{tot} for each gate of approximately 2pF, and f_{clk} is 800Hz, this translates to a single gate dynamic power of $3.2nW$. Therefore, as long as there are approximately $P = 100$ gates in the SAR logic, the previous estimate will be reasonable for the total dynamic power. This implies for each DFF there should be approximately 5 gates.

2. Comparator

In CMOS and BiCMOS technologies, the comparator structure typically has a topology consisting of an input stage, or pre-amplifier, and a latch stage [94]. How these are implemented can vary greatly providing a wide range of strengths and weaknesses for each topology. However, for a low power situation, most of these topologies suffer from the need to burn static power. To avoid static power consumption, a comparator based on digital circuits would be ideal. If one uses a switched capacitor technique to charge and/or discharge a capacitor while comparing the DAC voltage and the sampled voltage, one can use a digital inverter to amplify the signal. In order to obtain the maximum analog gain from the inverter, it is biased at its maximum gain point by connecting its input and output together prior to making a decision. The basic architecture of the comparator is shown in Fig. 54 [95] and is the same architecture as the one implemented in chapter 3 for the SPR. The main disadvantage of this circuit is its power supply rejection performance, but this may be mitigated by using a large capacitor at the supply node [95]. The size of the transmission gates and the capacitors used for auto-zeroing and comparison directly have an impact on the ability of the comparator to produce a valid result in the required clock period. This is because the comparator must be able to make a decision within one half clock cycle so that the logic is able to perform the correct operation on the previous bit. To assist in the decision process the comparator is clocked at twice the frequency of

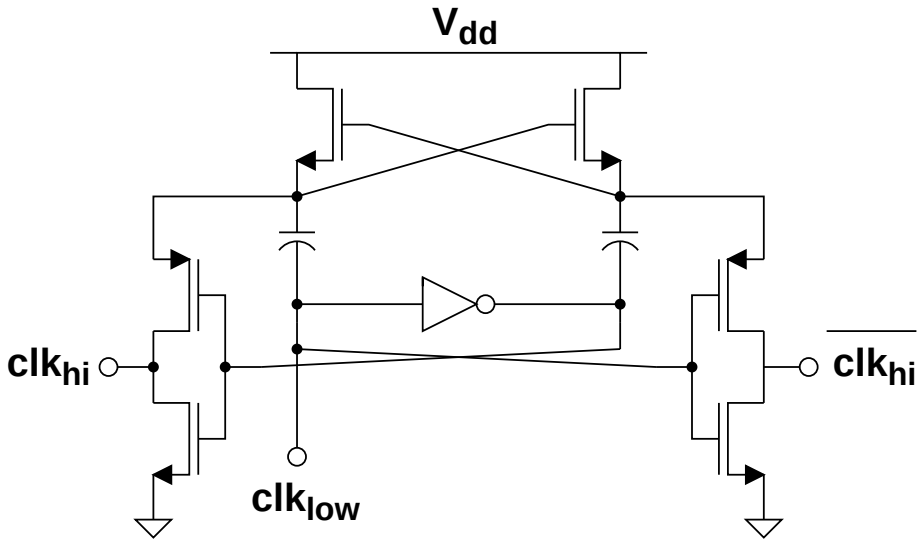

Fig. 55.: Clock Voltage Doubler.

the other digital circuitry. Therefore, the RC product of the input switches and the capacitor must be able to settle to its final value (≈5 time constants) in a half clock cycle. Therefore,

$$RC < \frac{5T_{clk}}{2} = \frac{5}{2f_{clk}}. \tag{6.11}$$

Assuming the comparator clock frequency is approximately 1kHz, this corresponds to

$$RC < 2.5\,\text{ms}. \tag{6.12}$$

If a capacitor of 1pF is assumed, this will correspond to a required switch on resistance of

$$R_{on} < \frac{2.5 \times 10^{-3}}{C} = \frac{2.5 \times 10^{-3}}{10^{-12}} = 2.5\text{G}\Omega. \tag{6.13}$$

While this is a large value, it may be further reduced to improve accuracy. Since the ON-resistance of a MOS device is highly dependent on the applied gate to source voltage, a clock voltage doubler (also called a clock boosting circuit) is designed to increase the applied voltage. Figure 55 shows the architecture of this circuit [96]

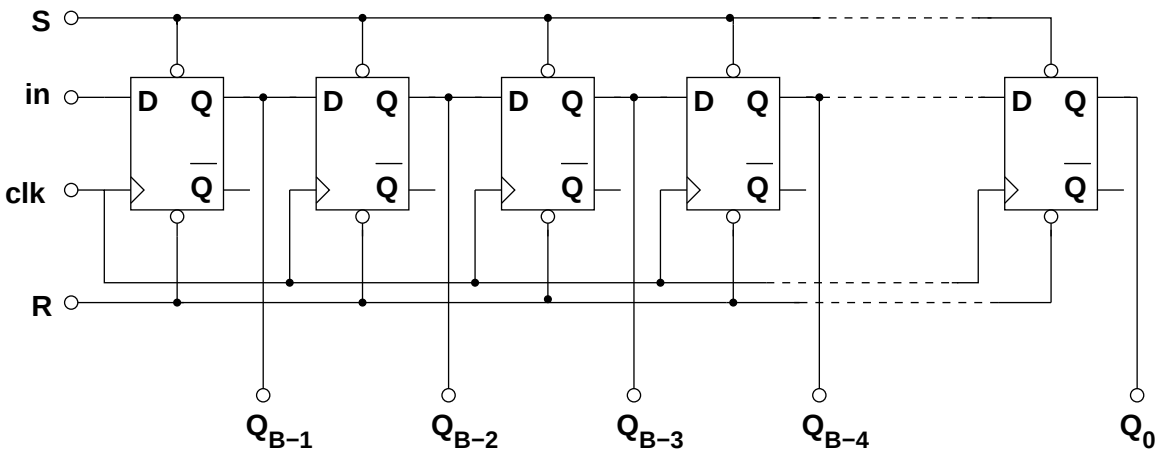

Fig. 56.: Shift register.

which is implemented to increase the gate voltage. If one assumes the MOS device is operating in the linear (ohmic) region then the ON-resistance, $R_{on,MOS}$ may be expressed as

$$R_{on,MOS} = \frac{1}{K_p \frac{W}{L}(V_{clk} - V_{source} - V_{th})}. \tag{6.14}$$

(6.14) is valid as long as the gate-source voltage is larger than the magnitude of the threshold voltage. If the gate source voltage is less than the threshold voltage, one must use

$$R_{on,sub-V_{th}} = \frac{1}{\frac{\partial I_d}{\partial V_{ds}}} = \frac{\phi_t}{2n\mu C_{ox}\frac{W}{L}\phi_t^2 e^{\frac{V_{clk}-V_{source}-V_{th}}{n\phi_t}} e^{-\frac{V_{ds}}{\phi_t}}}. \tag{6.15}$$

In either case, it is seen that increasing the actual magnitude of the clock voltage will reduce the overall on resistance and therefore improve comparator decision time. Since the comparator itself must drive all of the decision logic, the output stage is designed as a parallel combination of multiple inverters to increase drive strength at the expense of added area, power and capacitance. Additionally, in order to insure a proper comparison, the clock frequency of the comparator is set to be twice that of the remaining SAR logic. This is done since, in a single clock period, the comparator may not reach a decision before the registers store the comparator output and decide

whether or not to keep the DAC bit. Therefore, the master system clock is directly applied to the comparator, and a clock divider is used to divide the master clock by a value of 2 which is then supplied to the SAR logic.

3. SAR Logic

The logic for the SAR ADC is designed using a combination of two sequential circuits. The first circuit is a shift register which is necessary and acts as a counter. A basic implementation of a shift register using DFFs is shown in Fig. 56. The number of

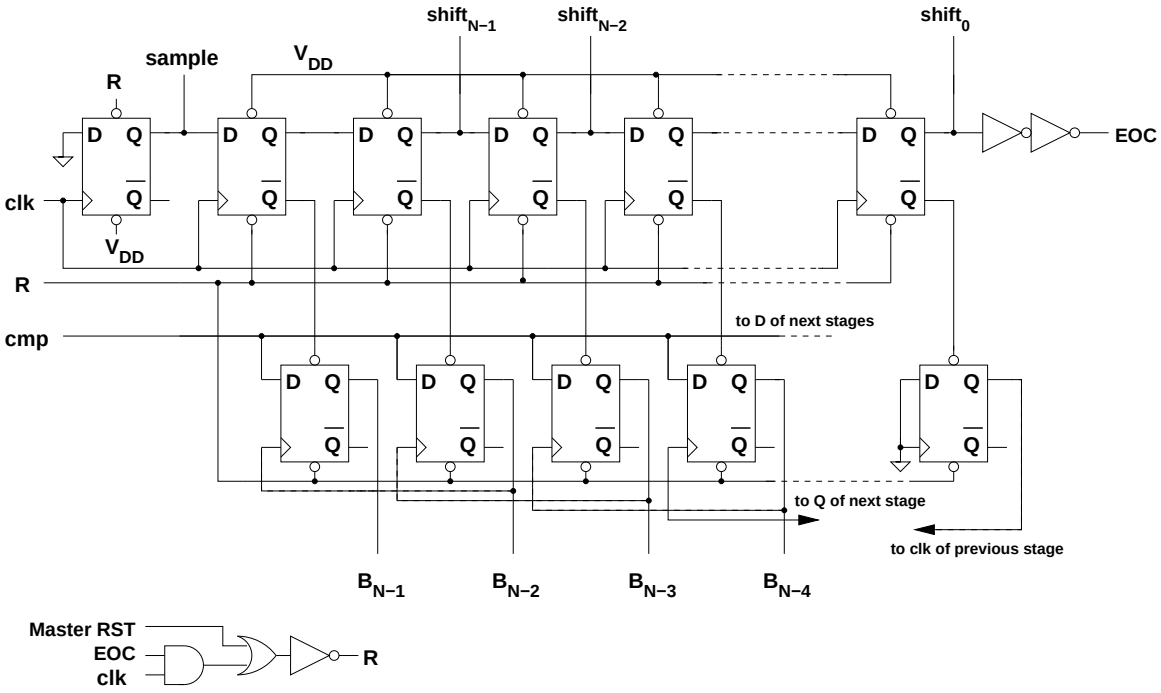

Fig. 57.: SAR logic used to implement the binary search algorithm.

DFFs required for the shifting operation is at least equal to $N + 1$, where N is the ADC bit number. The outputs of the shift register are then fed into the 'SET' input of another DFF, which in turn controls the DAC bits. When 'SET' is high, the output of the corresponding DAC driving DFF is also high. A comparison is then made and

the output of the comparator after a decision has been made is then fed back into the second row of DFFs. During this second clock cycle of the logic (the 4th for the comparator) a decision is made as to whether the bit should be kept or thrown away and the output is then stored in this DFF until a reset signal is given. This occurs when the shift registers, or a 'master reset' signal, is applied to these DFFs. Figure 57 shows the top level view of the implemented SAR logic with the shift registers being located in the upper row, and the DAC controlling DFFs in the bottom row. The additional outputs labeled as '*shift*<*X*>' are used for generating a serial output from

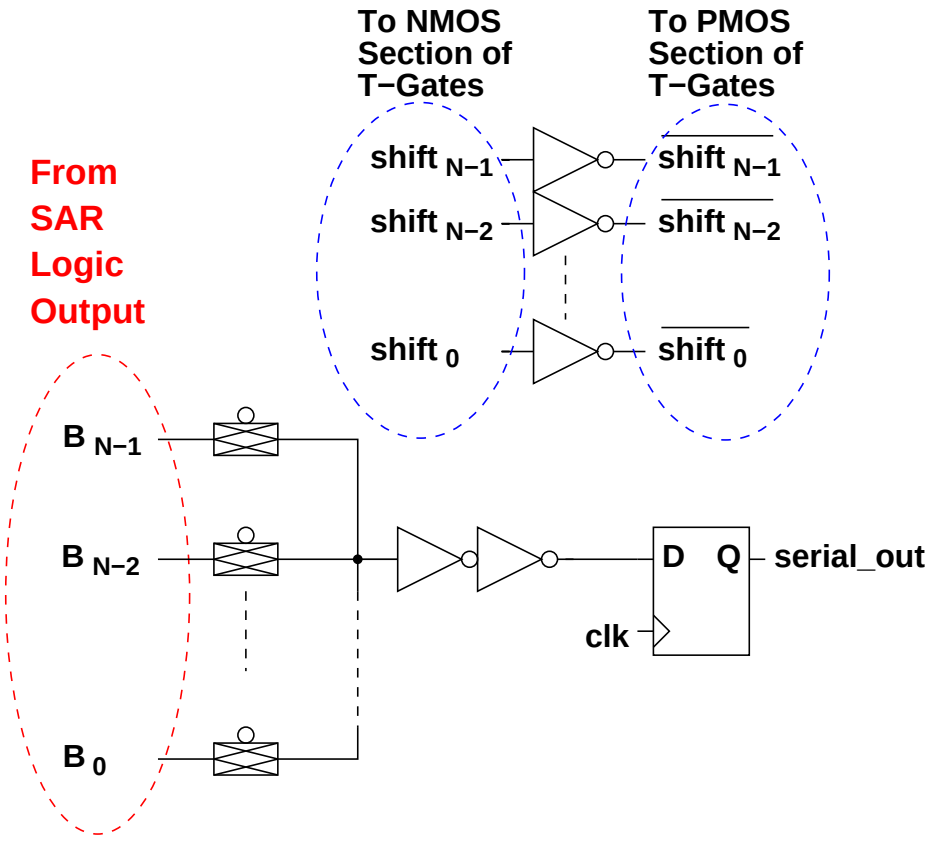

Fig. 58.: Multiplexer used to implement the parallel to serial conversion.

the ADC since the SAR ADC has an inherently parallel output. To generate a serial

output from this parallel data, a multiplexer is implemented and is shown in Fig. 58.

It should be noted that almost all of the digital circuitry is constructed using

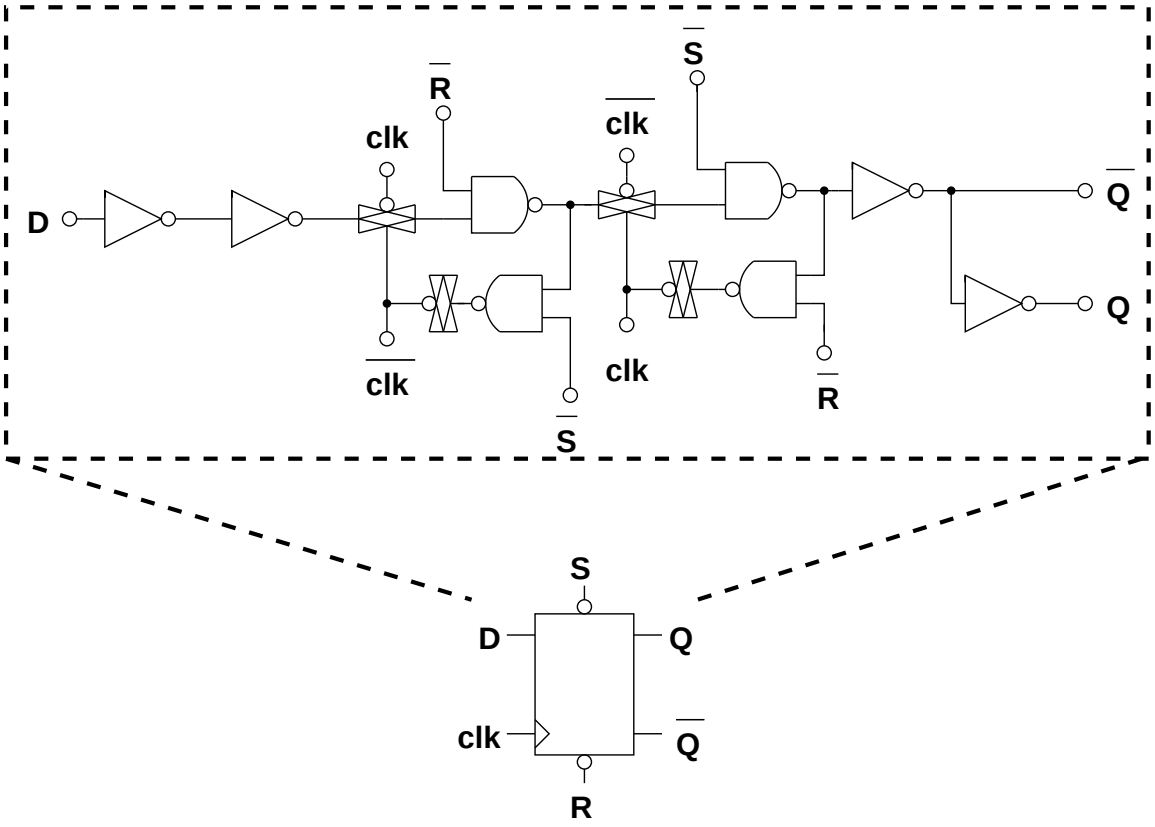

Fig. 59.: Pass Transistor Logic D-Flip Flop based on NAND gates.

DFFs. This means the design and layout of these structures provides an important consequence into the overall power consumption and area of the system. The DFF structure implemented is given by Fig. 59. The architecture of this DFF diverges from the typical architecture because the overall system is designed to work in sub-threshold and/or low-voltage applications and this DFF has a superior performance to the standard architecture under these circumstances [97]. As was seen in (6.6), the power dissipated by the digital circuitry is proportional to V_{dd}. For this design, to help minimize the power consumption, a $V_{dd} \leq 1$V is desired with an absolute

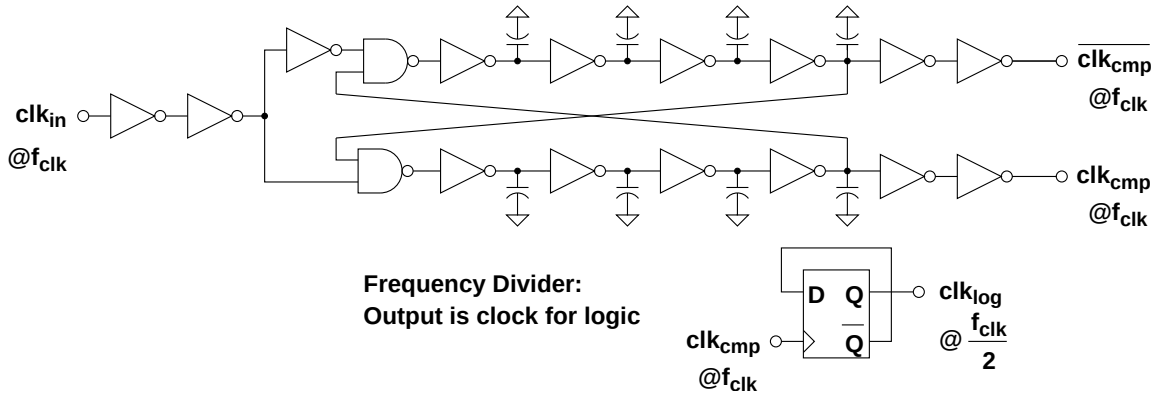

Fig. 60.: Non-overlapping Clock Generator and Frequency Divider.

maximum of approximately $2V$. It should also be noted that the NAND gates are implemented using inverters and transmission gates as well making the overall SAR logic and comparator reliable only on inverters, transmission gates and capacitors (pass transistor logic (PTL)).

4. Clock Generation

Only a single clock is needed for the proposed SAR ADC, a master clock, and this signal is then used to derive all other required clock signals. The first circuit the master clock encounters is a non-overlapping clock generator. Once bi-phase, non-overlapping clocks are generated, a frequency divider is used to generate a signal with half the master clock frequency. The overall architecture of the clock generation circuitry is shown in Fig. 60. The non-overlapping, bi-phase master clock is used to drive the comparator while the divided clock signal is used to drive the remaining SAR logic.

5. DAC

The final circuit designed for the SAR ADC is a capacitive DAC. As stated previously, a capacitive DAC was chosen to help reduce the overall static power consumption. This is because a resistive ladder DAC and a current steering DAC both dissipate continuous power, whereas the charge sharing capacitive DAC only dissipates energy during switching sequences. A basic structure of the DAC was presented earlier in this chapter in Fig. 51. The fundamental design points of the DAC are selecting a large enough unit capacitor size to neglect parasitics and reduce the integrated noise at the input of the comparator to less than $1/2LSB$ but selecting a small enough capacitor to help insure proper settling to within $1/2LSB$ of its final value during one half clock cycle. The implemented switches will possess a finite on resistance, $R_{on,MOS}$, as stated previously and, in conjunction with the DAC capacitors, will result in an RC time constant settling. Assuming a linear system then the DAC voltage will exhibit an exponential behavior giving rise to (6.16).

$$LSB \cdot e^{\frac{-T}{2RC}} < \frac{1}{2}LSB \tag{6.16}$$

(6.16) implies that the RC product set by the switch and capacitor must be able to settle properly within its given period. For noise purposes, we want the overall integrated noise to be less than 1/2LSB which implies

$$\frac{kT}{C} < \frac{1}{2}LSB. \tag{6.17}$$

From 6.16 and 6.17, a minimum capacitance value may be determined from the noise specification. Then, the required ON-resistance of the DAC switch may be determined from 6.16. For the given specifications, the unit capacitor size was determined to be approximately 1pF and the on resistance of the switches was determined to be in the

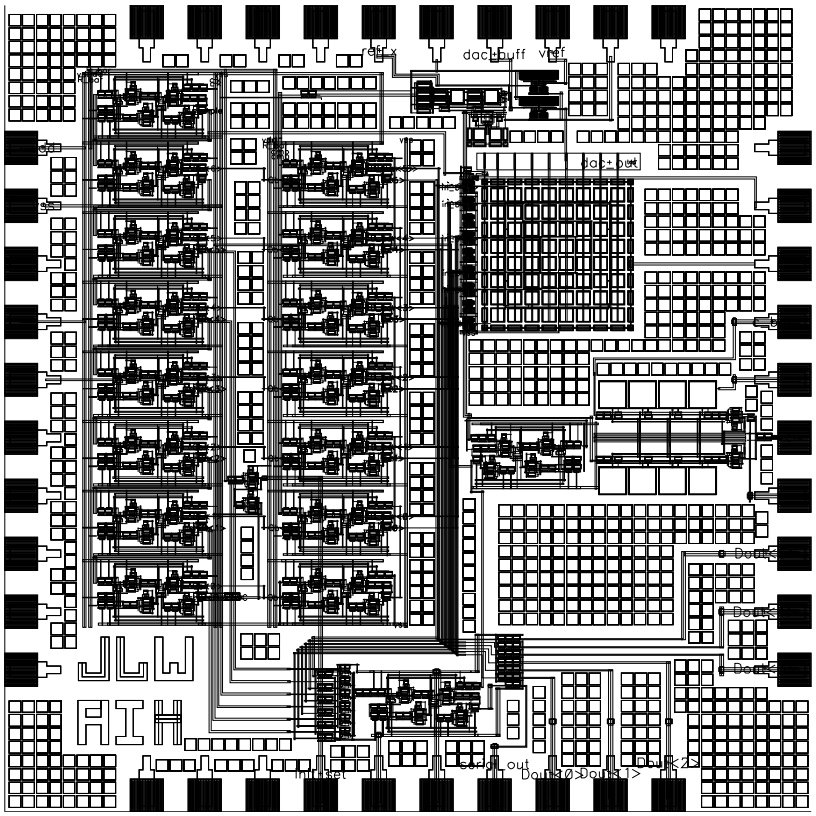

Fig. 61.: Layout of the 6-bit SAR ADC.

same order of magnitude as that of the comparator. Therefore, instead of scaling the size of the switches to correspond to the appropriate bit, unit switches were used for all capacitors. The gates of the switches are controlled by the Q outputs of the DAC driving DFFs (the bottom row of DFFs) in Fig. 57.

D. Simulation Results

The SAR ADC was designed in ON 0.5μm CMOS and simulated using Spectre. The layout of the 6-bit SAR ADC is shown in Fig. 61 and was performed using Virtuoso while verification was done using Calibre. Including the 40 pins required for bonding, the total size of the ADC is 3mm $\times$ 3mm. Post-layout simulation results verifying correct operation of the SAR ADC are shown in Figs. 62 and 63. Through simulations,

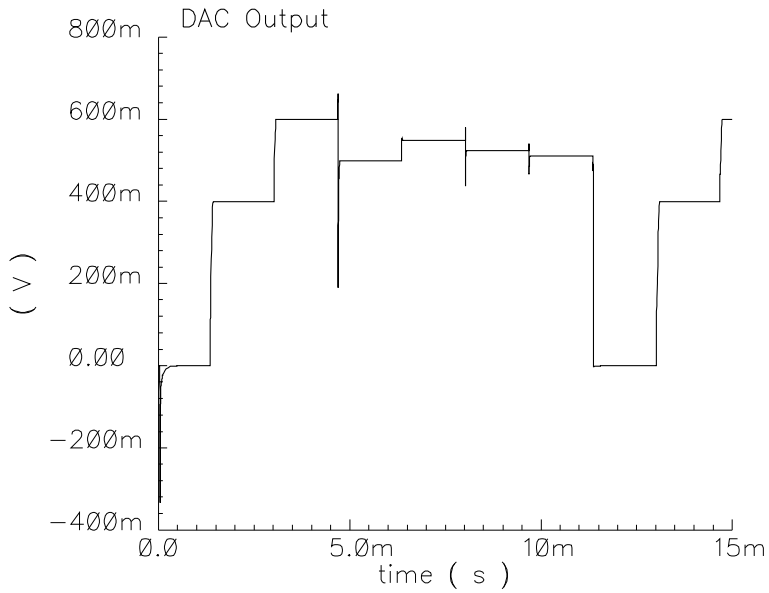

Fig. 62.: DAC output for a 513mV sampled value.

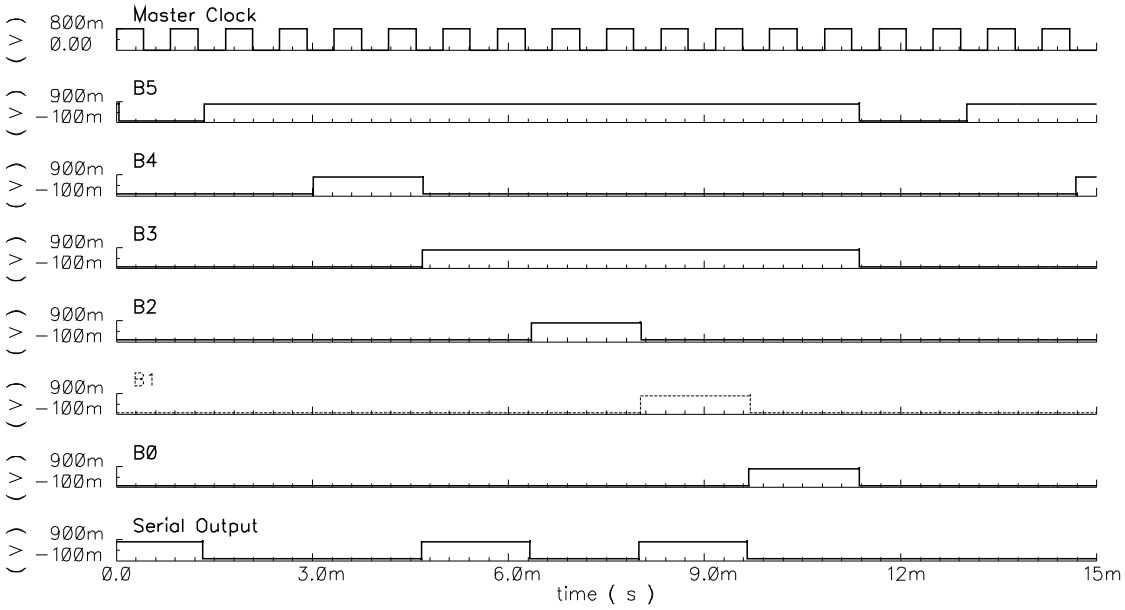

Fig. 63.: ADC output and master clock signal.

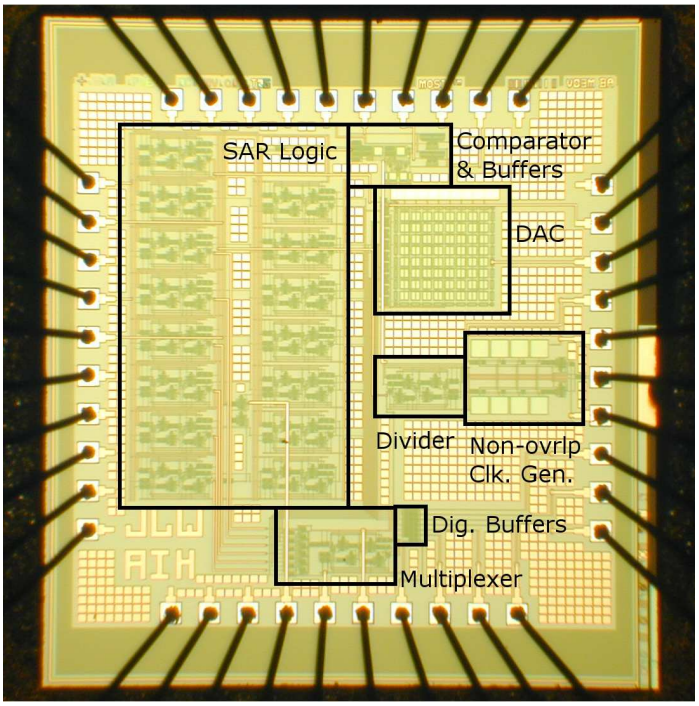

Fig. 64.: Chip micrograph of ON 0.5μm CMOS SAR ADC.

the minimum operating V_{dd} of the chip was 0.8V at a master clock frequency of 1kHz.

E. Measurement Results

The proposed 6 bit SAR ADC was fabricated using ON 0.5μm CMOS using standard CMOS devices and poly-poly MiM capacitors. The chip micrograph of the fabricated ADC is shown in Fig. 64. The circuit was tested using an Agilent 1673G Logic Analyzer, an HP33102A Function/Arbitrary Waveform Generator for the ADC clock as well as for the input signal for characterization, and an Agilent E3360A Triple Output DC Supply to power the chip. Functionality of the proposed ADC at different V_{dd} levels was tested as well as static performance with the proposed system. The proposed low-power ADC with a 0.9V V_{dd} and a DC input level of 513mV produces a logic output as shown in Fig. 65. In Fig. 65 the output bits are listed as Bit 0

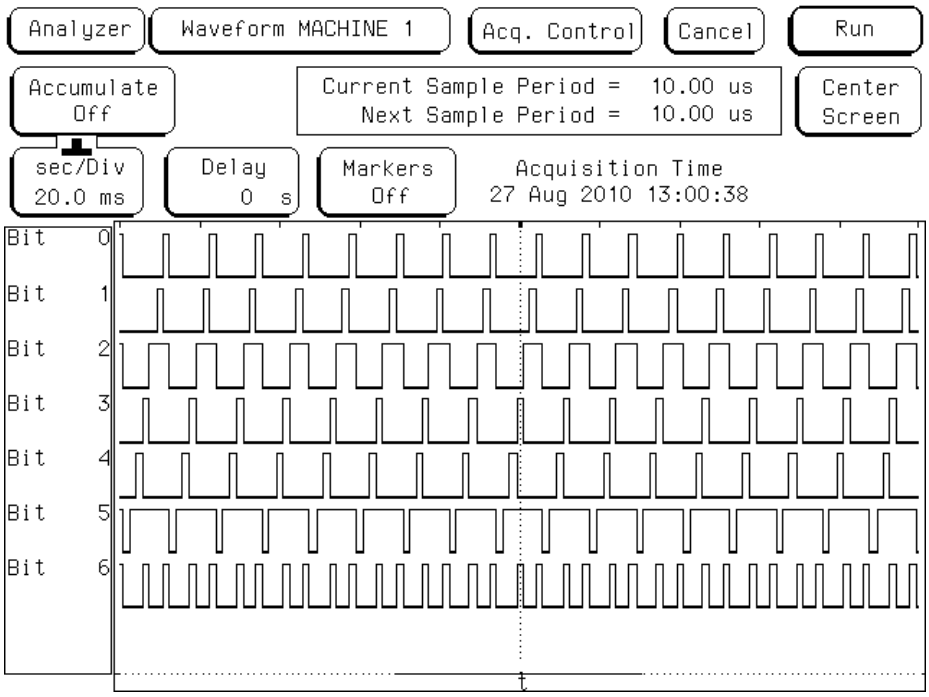

Fig. 65.: Measured SAR ADC outputs for $V_{dd} = 0.9V$ and $V_{in} = 513mV$.

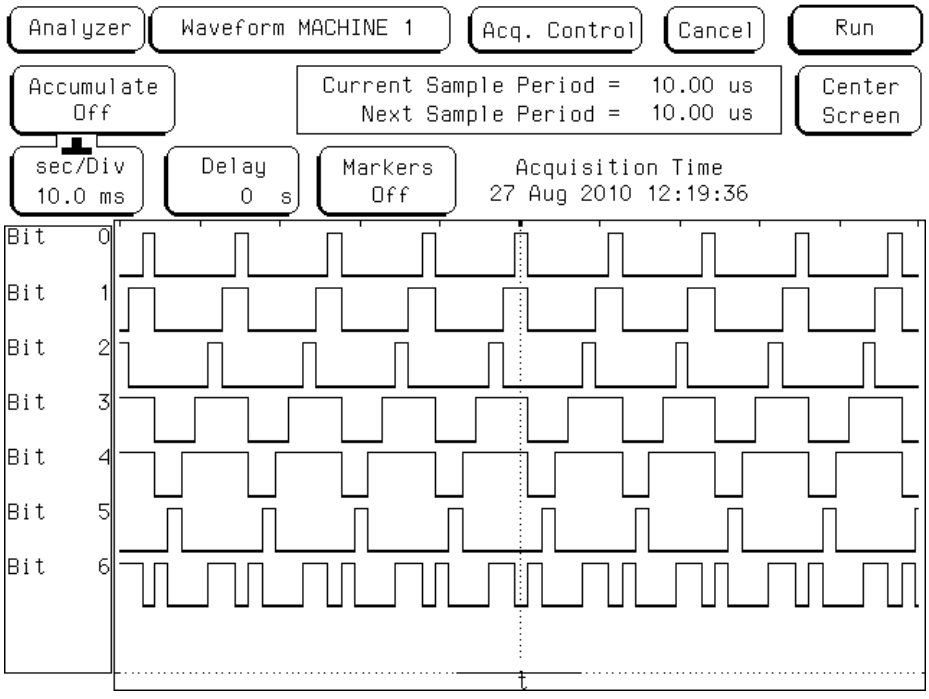

Fig. 66.: SAR ADC output bits for $V_{ref} = 0.3V_{DC}$, $V_{dd} = 0.9V$, $f_{clk} = 1.2kHz$.

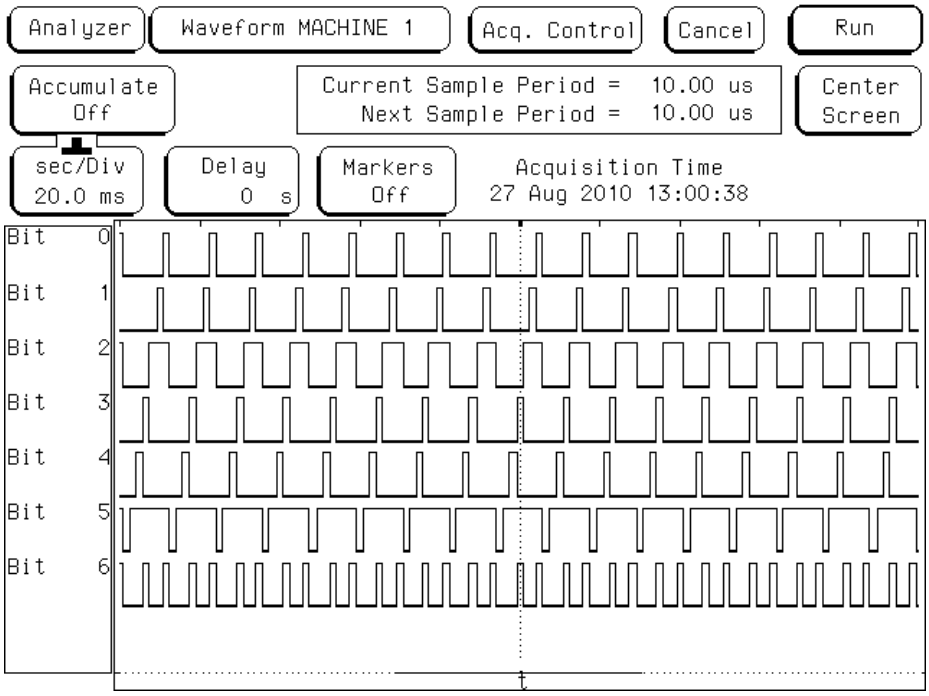

Fig. 67.: SAR ADC output bits for $V_{ref} = 0.5V_{DC}$, $V_{dd} = 0.9V$, $f_{clk} = 1.2kHz$.

(LSB) to Bit 5 (MSB). Bit 6 in this figure is the serial output of the multiplexer which would be used to control the IR-UWB TX. The average power consumption of the ADC at this supply level was measured to be approximately 880μW, which was in good agreement with the simulated value of 820μW. Although this is larger than desired, this power consumption is mainly attributed to three factors: 1) large parasitic capacitances, 2) requiring a large V_{dd}, and 3) large ON/OFF overlap within the circuits due to the large V_{th} of the NMOS and PMOS devices (approximately 0.7V and -0.9V, respectively). Thus, the overall power consumption was larger than desired. In the event a process with a smaller minimum feature size may be utilized, the power consumption can be decreased. To verify this, the proposed ADC was re-implemented in a 0.18μm process with nominal V_{th} of 0.4 and -0.45 for NMOS and PMOS, respectively. For the same power supply and input level, the simulated

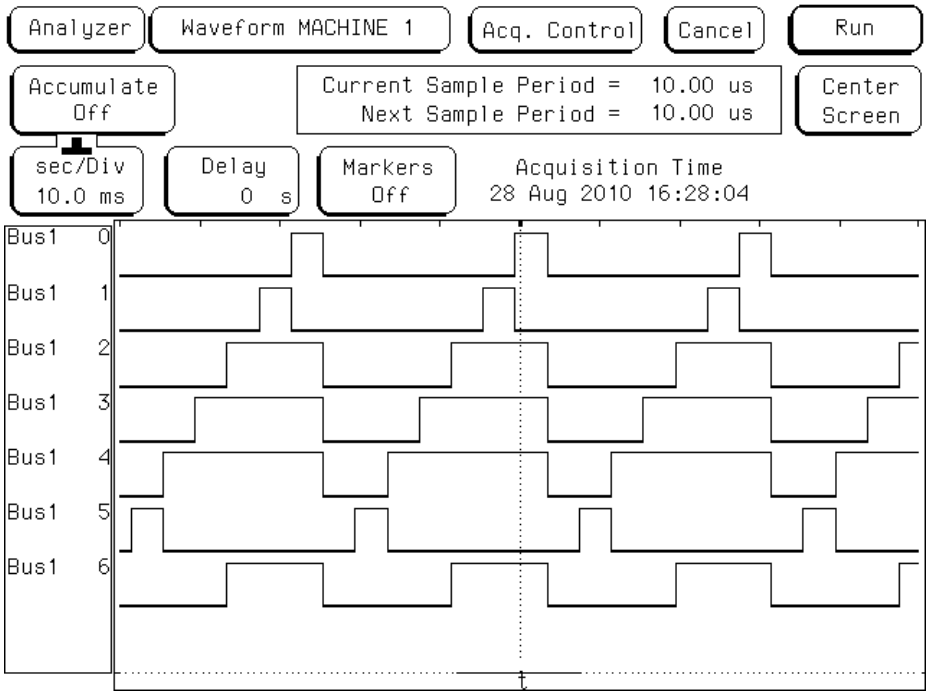

Fig. 68.: SAR ADC output bits for $V_{ref} = 0.8V_{DC}$, $V_{dd} = 1.8V$, $f_{clk} = 1.2kHz$.

average power consumption was only 30nW.

To verify performance over different power supply voltages and sampled values, the SAR ADC was also tested with sampled voltages of 0.3V and 0.5V and a 0.9V V_{dd}. These results are seen in Figs. 66 and 67. Although the system is operational at this supply level, performance was limited by the buffers used at the input of the comparator. Improved performance is seen when the supply voltage is elevated to 1.8V with sampled voltages of 0.8V and 1.72V seen in Figs. 68 and 69.

A plot of the buffered DAC voltage is shown in Figs. 70 and 71. A sine wave input was applied to the circuit with a value of $0.35\sin(2\pi 11.7t) + 1.25\,V$. The DAC is then shown to track this sine wave input in Fig. 70 while a zoomed view of the DAC voltage is shown in Fig. 71 to see a closer view of the SAR algorithm at work.

For static testing of the ADC, a low frequency ramp signal was applied to the

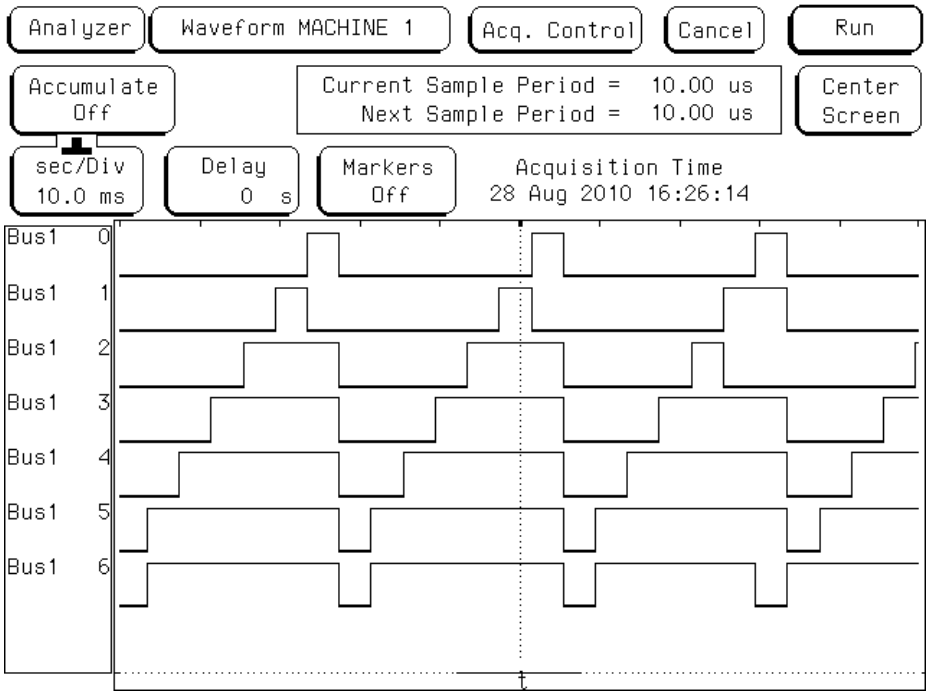

Fig. 69.: SAR ADC output bits for $V_{ref} = 1.72V_{DC}$, $V_{dd} = 1.8V$, $f_{clk} = 1.2kHz$.

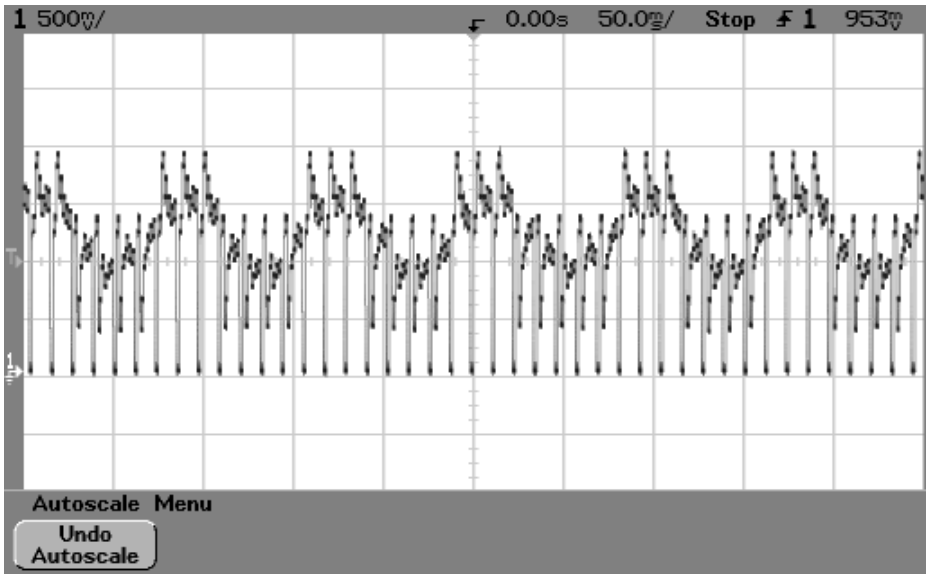

Fig. 70.: Oscilloscope plot of the DAC output with a sine wave input.

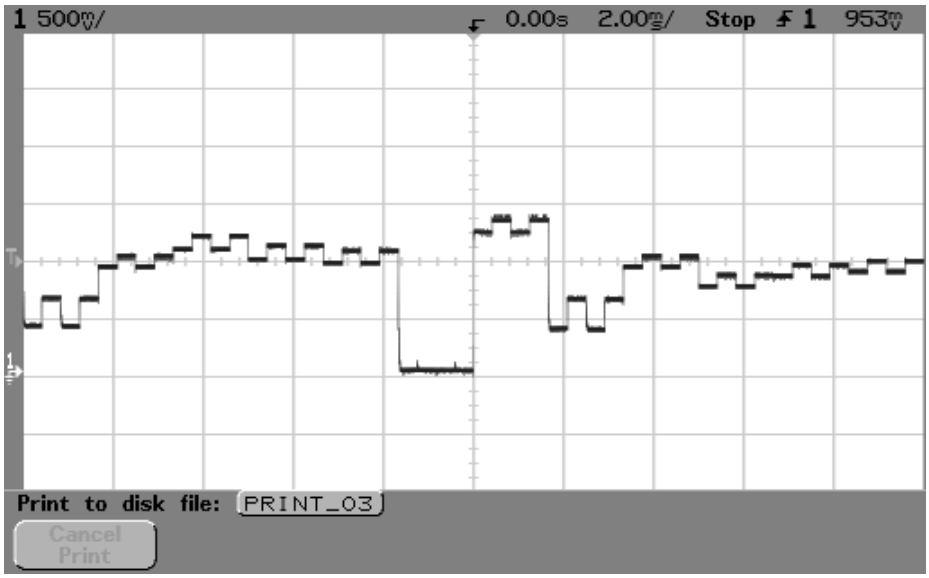

Fig. 71.: Zoomed view of oscilloscope plot of the DAC output with a sine wave input.

input of the ADC with a sampling frequency of approximately 800Hz. The data from the logic analyzer was then exported into MATLAB for post-processing. The measured INL and DNL of the fabricated SAR ADC with a V_{dd} of 1.8V are shown in Fig. 72. In this design, the performance of the INL and DNL were limited by the implementation of a voltage buffer between the capacitive DAC and the comparator. This buffer did not have a full-scale common-mode input range and therefore limited the achievable performance. Additionally, a common figure-of-merit (FOM) applied to ADCs is given in (6.18) [98].

$$FOM = \frac{P_{diss}}{f_{clk}2^N} \text{ J/bit} \tag{6.18}$$

Substitution of the measured results ($P_{diss} = 880\mu W$, $f_{clk} = 1.2kHz$, $N = 6$) results in a FOM of 11.46 nJ/bit for the presented design.

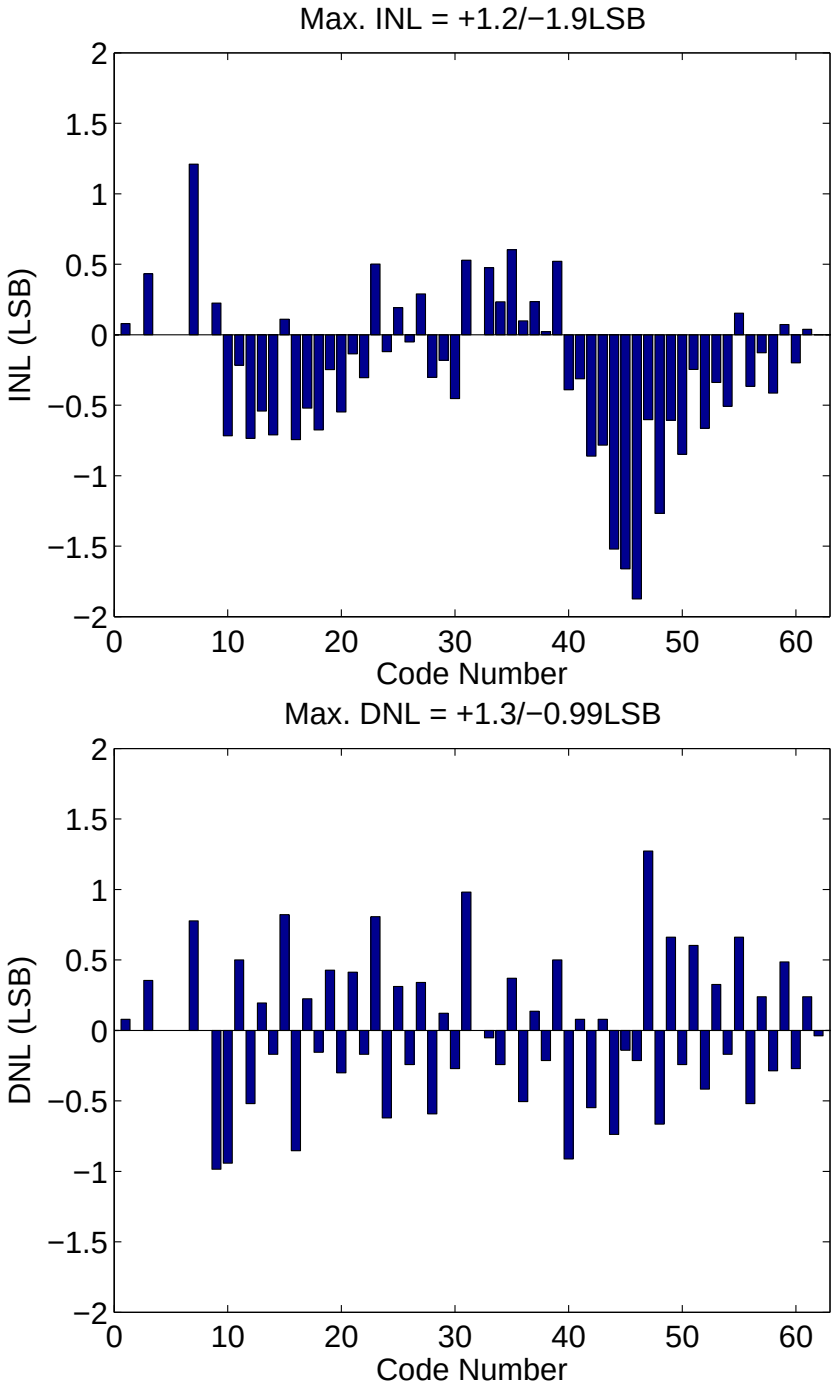

Fig. 72.: Measured INL and DNL of the SAR ADC.

F. Conclusions

A 6-bit successive approximation register (SAR) analog-to-digital converter (ADC) for digitizing the output of the sensor for the proposed wireless sensor system was presented. Measurement results showing operation from a 0.9V power supply were provided and recommendations for future designs were also given. The main limitation of the proposed circuitry lies in the process chosen for implementation (0.5μm CMOS) and the voltage buffers used at the input of the comparator. In a future design, a technology of 90nm may be a more appropriate choice for the proposed wireless sensor system and a low-power rail-to-rail buffer should be used to drive the comparator inputs. Nevertheless, the presented circuitry is promising and the results are well within the expected performance values.

CHAPTER VII

MULTI-BAND OFDM ULTRA WIDEBAND TRANSMITTER

In chapter 5 there was a discussion on UWB transmitters based on impulse signals using OOK modulation. These architectures are extremely power efficient compared to an upconversion system (one employing a frequency synthesizer) but are limited by the data rate of the system. In the event larger data rates are necessary, greater than a few hundred kbps and closer to a few hundred Mbps, the same spectrum may be utilized to send much more data at the expense of power and area. In this chapter, a multi-band orthogonal-frequency-division-multiplexing (MB-OFDM) UWB TX is presented for high data rate WPANs. The circuit was fabricated in a 0.13μm CMOS process using standard process options. Design considerations, simulation and measurement results will be presented.

A. Introduction

In 2002 the FCC opened the frequency spectrum from 3.1-10.6GHz for unlicensed use. Since this time a debate between which modulation format would be the best option for these Ultra Wideband (UWB) systems ensued. The two front-runners for this position were Direct Sequence Code Division Multiple Access (DS-CDMA) and Multi Band Orthogonal Frequency Division Multiplexing (MB-OFDM), [99,100]. For much of this time the front runner seemed to be MB-OFDM due to its robustness to narrowband interference. The strength of this modulation scheme stems from its use of many narrowband low data rate carriers as opposed to modulating one wide-band signal with a high data rate (as in DS-CDMA).

Until 2002 UWB systems were mainly targeted towards sensor networks and radar imaging systems. In these applications, instead of having multiple data carriers,

the systems were composed of very narrow, low energy time-domain pulses. These small time-domain pulses translate to a very wideband signal when viewed in the frequency domain. The main difference between these impulse radio UWB (IR-UWB) networks and the MB-OFDM and DS-CDMA UWB systems was the data rate. It was at this time it became apparent that the UWB spectrum could be used for wireless personal area networks (WPANs) to send large amounts of data over a small distance at a higher rate than Bluetooth or other wireless standards.

In this chapter, we present the system and circuit design of a MB-OFDM UWB TX which was fabricated in UMC 0.13μm CMOS. System level budgeting and block level specifications will be determined. The UWB TX was fabricated using standard library components and operates from a single 1.2V power supply while consuming approximately 60mA of current. The overall system consists of a low-pass filter (LPF), an I/Q Mixer, an antenna driver and a power detector.

B. UWB

For the MB-OFDM scheme presented in [100] the frequency spectrum contained many different sub-bands, each with a bandwidth of 528MHz. The initial intent of the task group was to have the first devices operate on the three lower bands (3.1-4.7GHz) and would be noted as "Mode I" devices. The remaining bands would be allocated for later use and/or more high-end products. While Mode I devices only use part of the allocated spectrum, this was necessary to obtain a system which met the specifications and generated high frequency carrier signals efficiently. The implementation of only the lower-most bands was also attributed to having the UNII band located near the middle of the UWB spectrum. This played a major role because UNII signals have a significantly larger signal power than UWB signals. Because of these issues (among

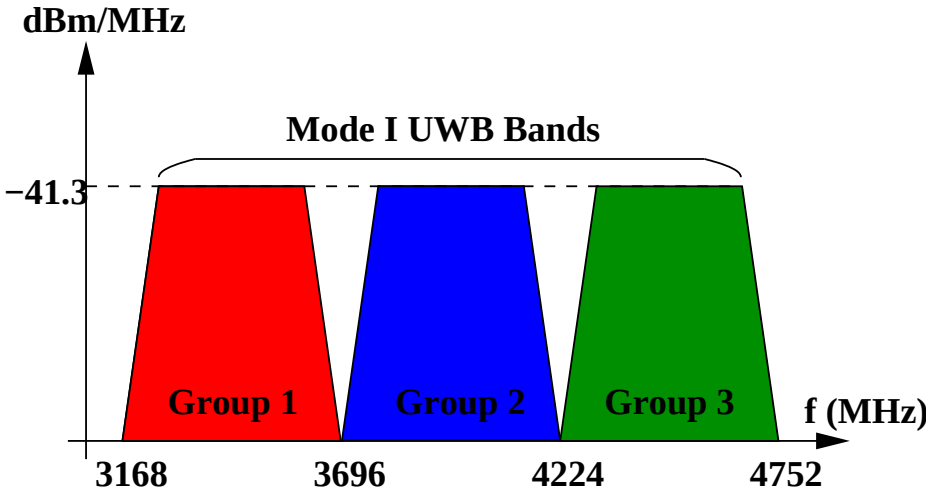

Fig. 73.: MB-OFDM UWB spectrum.

others), it has since been a topic of discussion as to how to properly allocate the remaining spectrum, [101–104].

In Fig. 73, the frequency spectrum for a Mode I MB-OFDM system is shown. The spectrum is divided into three sub-bands each with a bandwidth of 528MHz. Within each sub-band, there are 128 channels available for information transfer with a bandwidth of 4.125MHz. After a symbol has been sent through the channel, the system will hop to a different band. This band-hopping scheme helps to promote greater security, as well as some immunity to noise. This may occur because if the information is not being received clearly on one channel, the system may adapt and transmit on a different channel which will potentially provide a better quality signal to the receiver. This action is shown in Fig. 74.

In Fig. 74, the OFDM symbol length (T_{SYM}) is determined by the allocation of the different sub-carriers in the different bands. Each UWB sub-band occupies 528MHz and is divided into 128 equally spaced channels which gives a frequency spacing of $\Delta f = \frac{528\times10^6}{128} = 4.125\,\text{MHz}$. The frequency spacing of each channel allows one to calculate the time required for the FFT as $T_{FFT} = \frac{1}{\Delta f} = 242.42\,\text{ns}$. To help

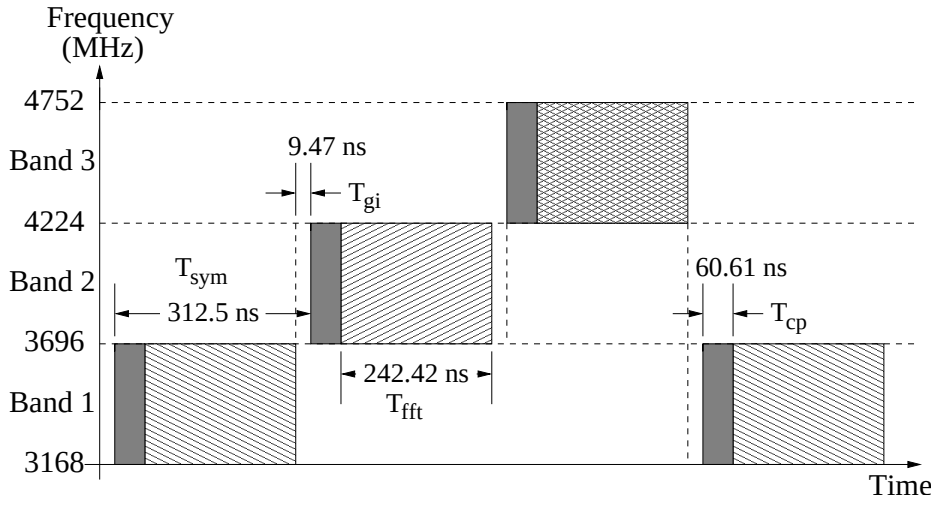

Fig. 74.: UWB band-hopping scheme.

mitigate the possibility of inter symbol interference (ISI) a guard interval is used between each frequency hop, $T_{GI} = \frac{5}{528M} = 9.47$ ns. A cyclic prefix is specified to account for any necessary settling time in the multipath environment and may be computed as $T_{CP} = 2\left[2T_{GI} + \frac{6}{528M}\right] = 60.61$ns. In the previous calcluation, the extra factor of two is used since the cyclic prefix (CP) appears at the beginning and end of the MB-OFDM symbol. This insures that the beginning and end of the symbol will have very little effect on future symbols, and will not be affected by previous symbols. Therefore, it may be noted that the overall time for the symbol may be computed as:

$$T_{SYM} = T_{GI} + T_{CP} + T_{FFT} = 9.47\,\text{n} + 60.61\,\text{n} + 242.42\,\text{n} = 312.5\,\text{ns}.$$

The sub-carrier allocation is defined in Table III, where T_{GI} is only 9.47ns which does not allot much time for the synthesizer, or the rest of the system, to settle to a steady state value. This has been noted as one of the most challenging aspects of designing a MB-OFDM UWB system [101, 103], but is not addressed here.

Table III.

MB-OFDM sub-carrier allocation.

# of Carriers	MBOA Use
100	data
12	pilot carrier
10	guard
6	included in CP

C. UWB TX Design

From [102], it is known that for a peak-to-average power ratio (PAR) of 9dB, a 4-bit ADC will provide an optimum signal-to-quantization noise ratio (SQNR). If the TX is assumed to have a DAC with the same number of bits, then there will also be a 9dB PAR on the TX information. It is necessary to know this information for setting the gain and IIP3 (among other parameters) of the TX blocks. This will be discussed in further detail shortly. Hence, a 4-bit DAC is assumed for this design but will not be presented here.

1. System

According to [100], the FCC has limited the transmit power to -41.3dBm/MHz. Therefore, the average transmit power may be calculated as

$$P_{TX,avg} = -41.3 + 10\log\left(N \times BW\right) - 1\,(\text{dBm}). \tag{7.1}$$

In (7.1), N is the number of sub-bands used and BW is the bandwidth of each sub-band in MHz. For Mode I UWB, $N = 3$ and $BW = 528$. The additional 1dB in (7.1) is used as a safety margin to insure the system does not violate the FCC mask.

Substituting the appropriate numbers (7.1) yields $P_{TX,avg} = -10.3$dBm.

Since each UWB sub-band contains 128 channels, linearity is a concern in the design of the system. With multiple carriers traveling through the system at a given time, it is difficult to obtain the required system performance. In [105], the required system IP3 is derived taking in account the number of carrier signals. The resulting equations which are used to determine the system level linearity for the UWB system may be expressed as

$$\begin{aligned} ACPR &= IMR2_{dBc} + 10\log\left(\frac{n^3}{4M_4 + 16N_4}\right) && (7.2)\\ IMR2_{dBc} &= 2\left(IP3_{dBm} - P_{OUT,dBm}\right) + 6_{dBc} && (7.3)\\ M_4 &= \frac{n^2 - \epsilon}{4} && (7.4)\\ N_4 &= \frac{2n^3 - 3n^2 - 2n}{24} + \frac{\epsilon}{8} && (7.5)\\ \epsilon &= \mod\left(\frac{n}{2}\right). && (7.6) \end{aligned}$$

In (7.6) $ACPR$ is the adjacent channel power ratio, $IMR2$ is the two-tone intermodulation ratio (often referred to as $IM3$), $P_{OUT,dBm}$ is the total output power of the system expressed in dBm (total power of all combined carriers) and n is the number of information carriers in the channel. The transmit mask given in [100] contains the required ACPR for the MB-OFDM UWB TX. Therefore, in (7.6) it is possible to solve for the overall output third order intercept point (OIP3) for the UWB TX. If this is done, one obtains

$$IP3 = P_{out,dBm} + \frac{ACPR - 10\log\left(\frac{n^3}{4M_4+16N_4}\right) - 6}{2}. \qquad (7.7)$$

Substituting in the appropriate values for the previous equation, $OIP3 \approx -2.6$ dBm is obtained.

Until now, there has been no distinction on which type of TX will be implemented

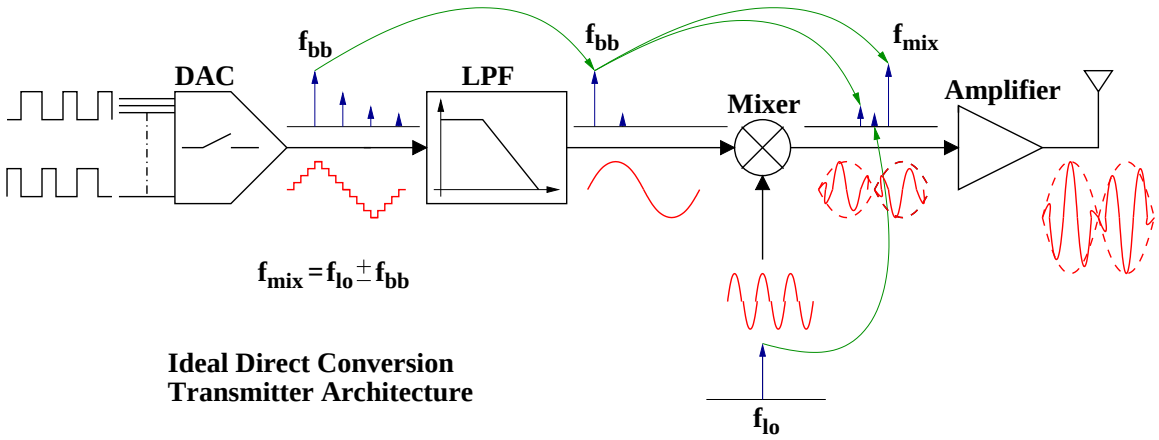

Fig. 75.: Ideal Direct Conversion TX with frequency and time domain signals.

because the previous explanations are for any MB-OFDM UWB system. However, since the system is fairly high-speed and to minimize the overall cost, a direct conversion system is assumed. This serves a few purposes in the overall system level design. First, this avoids the necessity of costly image reject filters (either on-chip or off-chip). Secondly, this choice of topology allows for the minimum number of components in a given TX architecture. Fig. 75 shows the assumed TX topology in the system level design. It is necessary to discuss the topology at this point in order to begin allocating design parameters for each of the blocks. Previously, the $OIP3$ was calculated from the given system level parameters. Assuming the direct conversion architecture and a $PAR = 9$dB, it is still necessary to determine the DAC output voltage and/or the overall TX gain. Since the DAC to be designed is a 4-bit Nyquist rate DAC, the LSB of the circuit does not need to be too small. Therefore, we will consider a TX gain of $G_{TX,dB} = -10$ dB, resulting in the output of the 4-bit DAC as

$$V_{pk,DAC} = \sqrt{2 \times 50 \times 10^{\frac{P_{out} + PAR_{dB} - G_{TX,dB} - 30}{10}}} \approx 0.0861 \text{ V}_{\text{pk}}.$$

Assuming the use of a Nyquist rate DAC ($F_s = 528$MHz) and knowing the peak-

to-peak output of the 4-bit DAC, the DAC LSB may be calculated as $V_{pk,DAC}/2^N = Vpk, DAC/2^4$. Knowing the sampling frequency, the required number of bits and the maximum single tone output peak-to-peak value for the DAC is enough to begin the design.

From the TX spectrum mask, it is possible to calculate the required filter order to obtain the required $ACPR$. Additionally, once the filter order is known, it is possible to calculate the amount of harmonic rejection which will be obtained from the DAC output. From here, it is determined that the LPF should be 6^{th} order and have a cut-off frequency of approximately 264MHz. Due to the large number of input tones, the linearity of the LPF is also a challenge. It is determined that a multi-tone power ratio ($MTPR$) of approximately 25dB is necessary for this design. Since a direct conversion architecture has been chosen to be implemented, flicker noise and DC offsets will degrade the performance of the overall system. To help alleviate these problems, the input of the LPF is designed to have a zero at the input with a corner frequency of approximately 1MHz. Although the data is centered around baseband (BB), this zero will not degrade the data greatly due to the large number of carriers as well as the fact that the first OFDM symbol does not appear until a little higher than 1MHz. The passband gain should be designed to be 0dB with minimal ripple.

The next stages in the TX are the in-phase (I) and quadrature (Q) mixers. Since the system is designed for mode-I operation, the LO tones are known to be located at 3432, 3960 and 4488MHz. For ease of integration, the output of the I/Q mixers should be single-ended so that a single ended antenna may be used and the mixer output should suppress the undesired sidebands as much as possible. The overall gain for this combined block should be at least -10dB. Since the required output power is so low, power amplification is usually unnecessary as the final stage of the system. Instead, an antenna driver is used to isolate the output of the mixer from

the antenna. Often times a source follower may be used to create a low output

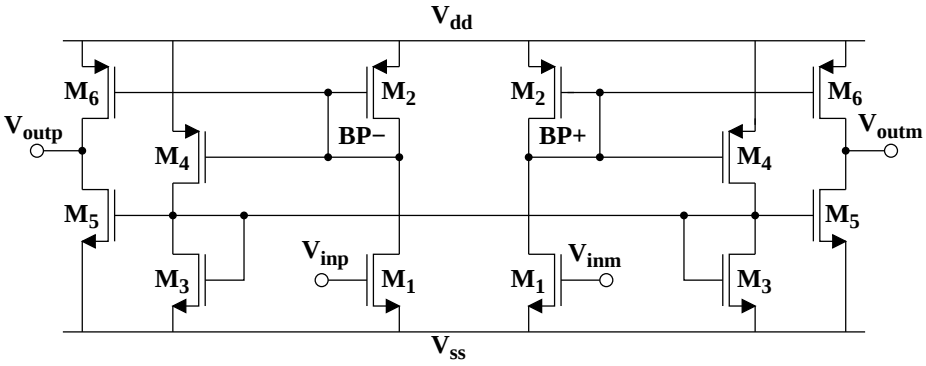

Fig. 76.: UWB LPF biquad schematic.

impedance and drive the load. However, for stability concerns at RF, this is not an ideal output stage. Instead, it is more common to use a common source stage with a gain of 1 to act as a buffer.

2. Filter

Since the linearity of the system is a large challenge due to the high number of carriers, each block must be fairly linear. Therefore, the biquad used in the low-pass filter is implemented using a pseudo-differential architecture as shown in Fig. 76. Although this architecture is more linear than a typical differential pair based OTA, it does suffer from a lowered common mode rejection. The 6^{th} order filter architecture is shown in Fig. 77.

The biquad shown in Fig. 76 is usually viewed as a simple 3-current mirror OTA. However, if additional capacitance is added at the diode connected PMOS stage and a significant capacitance is added at the output, this is also a representation of a common 2-integrator loop biquad stage. The additional capacitance added to the diode connected PMOS works as an effective lossy integrator. The additional

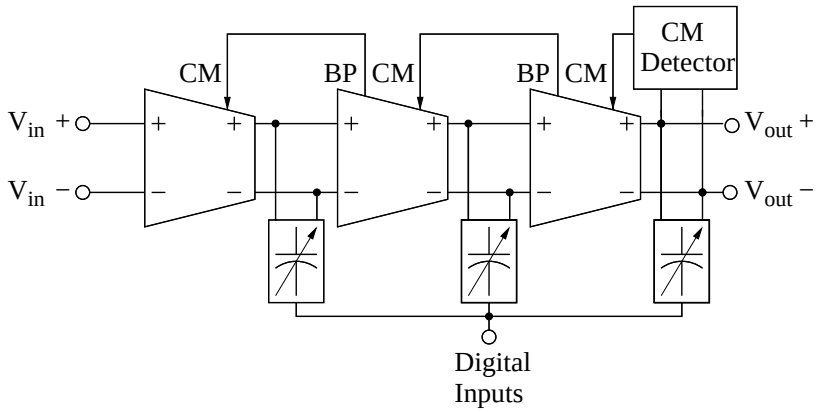

Fig. 77.: UWB LPF schematic.

capacitance added to the output acts as a lossless integrator. Therefore, there are both lowpass and bandpass outputs available for this biquad section. Using Mason's rule, we may obtain the transfer function of this block to be

$$\frac{V_o(s)}{V_i(s)} = \frac{g_{m1}\left[g_{m6}\left(g_{m3}+g_{o3}+g_{o4}\right)-g_{m4}g_{m5}\right]}{\left(g_{m2}+g_{o2}+g_{o1}\right)\left(g_{o5}+g_{o6}\right)\left(g_{m3}+g_{o3}+g_{o4}\right)} \times \ldots \frac{\frac{(g_{m2}+g_{o2}+g_{o1})(g_{o5}+g_{o6})}{C_1C_2}}{s^2+s\left[\frac{g_{m2}+g_{o2}+g_{o1}}{C_1}+\frac{g_{o5}+g_{o6}}{C_2}\right]+\frac{(g_{m2}+g_{o2}+g_{o1})(g_{o5}+g_{o6})}{C_1C_2}} \tag{7.8}$$

The LPF was simulated using Spectre and post-layout simulations are shown in Figs. 78 and 79. In Fig. 79, the input tones are designed to have the required PAR of 9dB as previously discussed. The resulting plots show that the filter satisfies the initial design constraints specified in the system level design.

3. Mixer

In a 0.13μm process, the headroom for stacked devices all but disappears. Although the signal levels for UWB are low (compared to typical wireless systems like GSM), the large number of data channels requires a fairly linear and simple mixer. As such, the implemented mixer is based on a Gilbert cell structure with the tail current removed

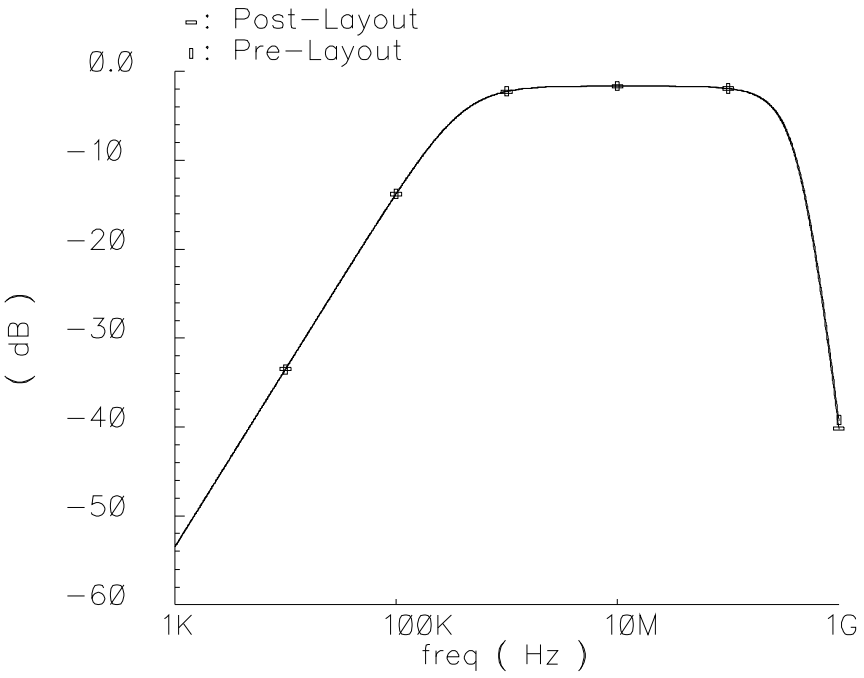

Fig. 78.: UWB LPF pre and post-layout AC simulation results.

from the baseband input device. The mixer used in this design is shown in Fig. 80. The LO signals are driven by on-chip buffers which follow an on-chip polyphase filter. Due to the large input swing of the LO, the signal may be assumed to be a square wave with signals appearing at odd harmonics (i.e. 3ω, 5ω, ...). The Fourier series coefficients may be found by solving

$$a_k = \frac{1}{k\pi} \sin\left(k\frac{\pi}{2}\right) \tag{7.9}$$

and the approximate LO signal ($sq(t)$) may be approximated as

$$sq(t) = \sum_{k=1}^{k=\infty} a_k \cos(k\omega t),\ k = 1, 3, \ldots \tag{7.10}$$

The single stage output voltage is equal to $G_m R_L sq(t) V_{bb}(t)$. Assuming the baseband input ($V_{bb}(t)$) is $A_{bb}\cos(\omega_{bb}t)$ and the first harmonic of the LO signal is

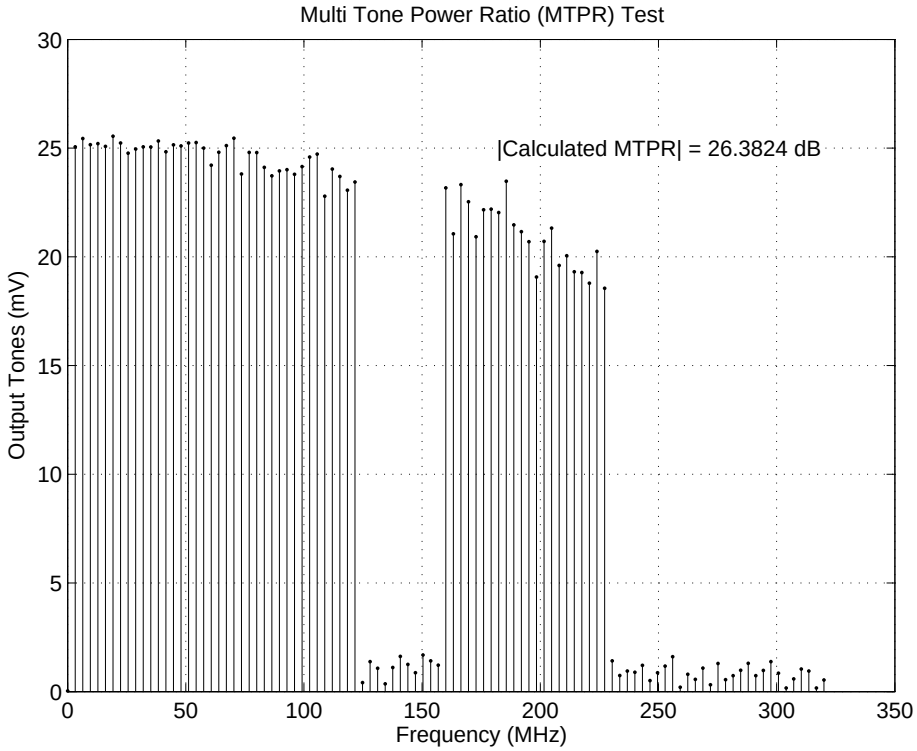

Fig. 79.: UWB LPF post-layout MTPR results.

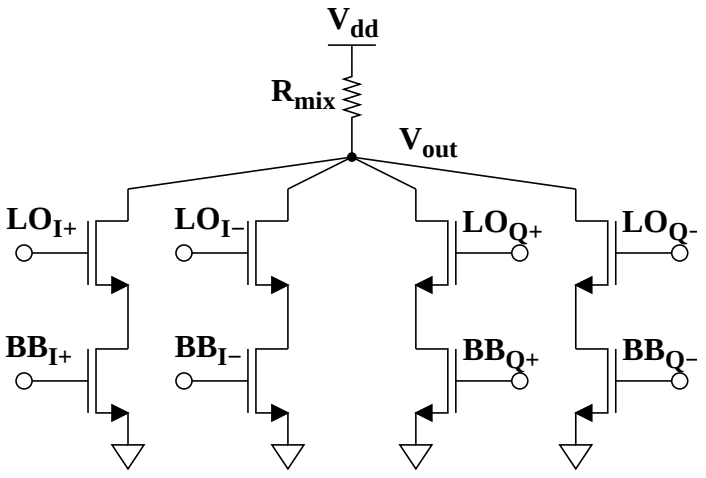

Fig. 80.: UWB up-conversion mixer schematic.

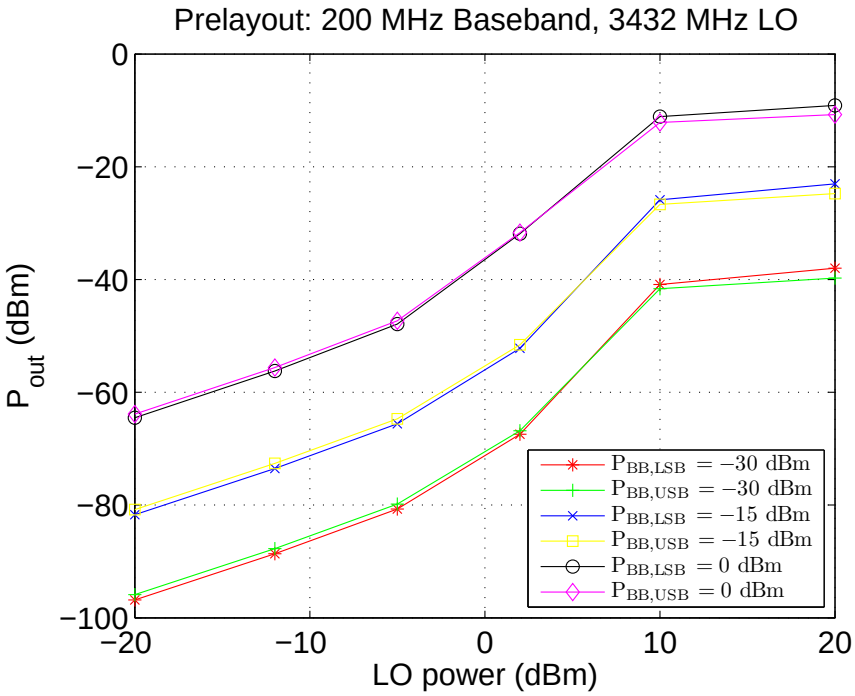

Fig. 81.: UWB mixer pre-layout sims. 200MHz baseband and 3432MHz LO.

$A_{LO}\cos(\omega_{LO}t)$ we may solve for the overall output voltage of a single stage of the mixer. Knowing that the LO signal and the baseband signals are all in phase will result in four equivalent outputs in magnitude. Therefore, the approximate output voltage of the mixer may be expressed as

$$V_o(t) \approx \frac{8}{\pi} g_m R_L A_{bb} A_{LO} \cos\left([\omega_{LO} - \omega_{bb}]\, t\right). \tag{7.11}$$

Figs. 81-86 show the pre and post-layout simulation results of the UWB mixer.

4. Power Detector

The implemented power detector is intended to be used in a complete UWB system. The output of the power detector will sense if the signal level is higher than the maximum allowed level and feedback a DC signal to a variable gain/amplitude stage within the TX signal path. A way this can be done is to have the DC output feed

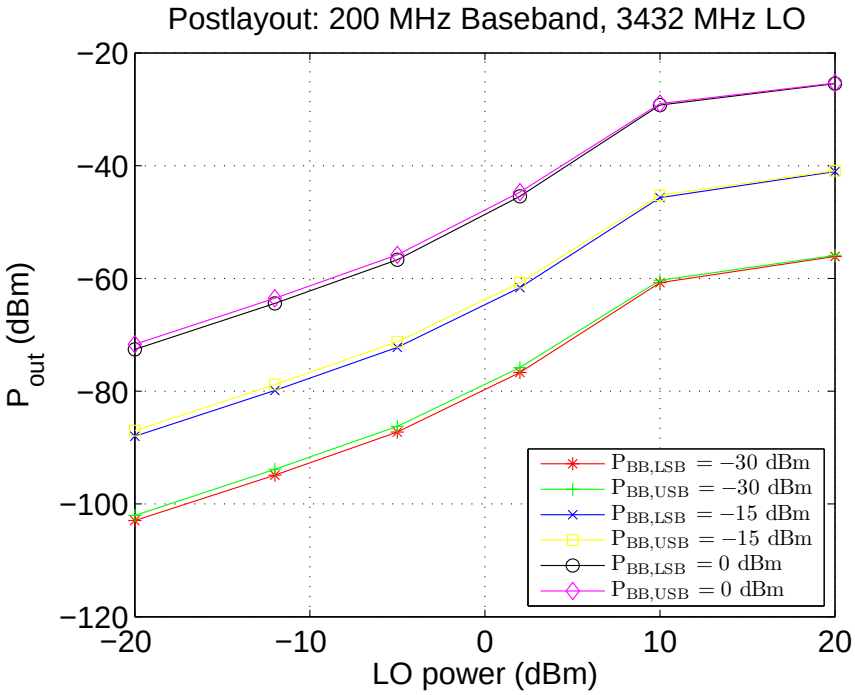

Fig. 82.: UWB mixer post-layout sims. 200MHz baseband and 3432MHz LO.

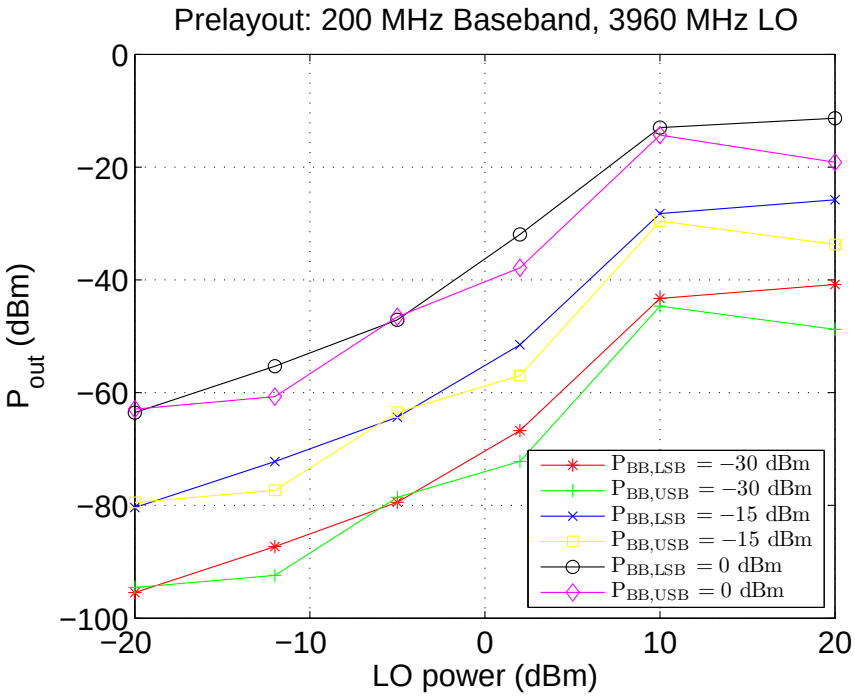

Fig. 83.: UWB mixer pre-layout sims. 200MHz baseband and 3960MHz LO.

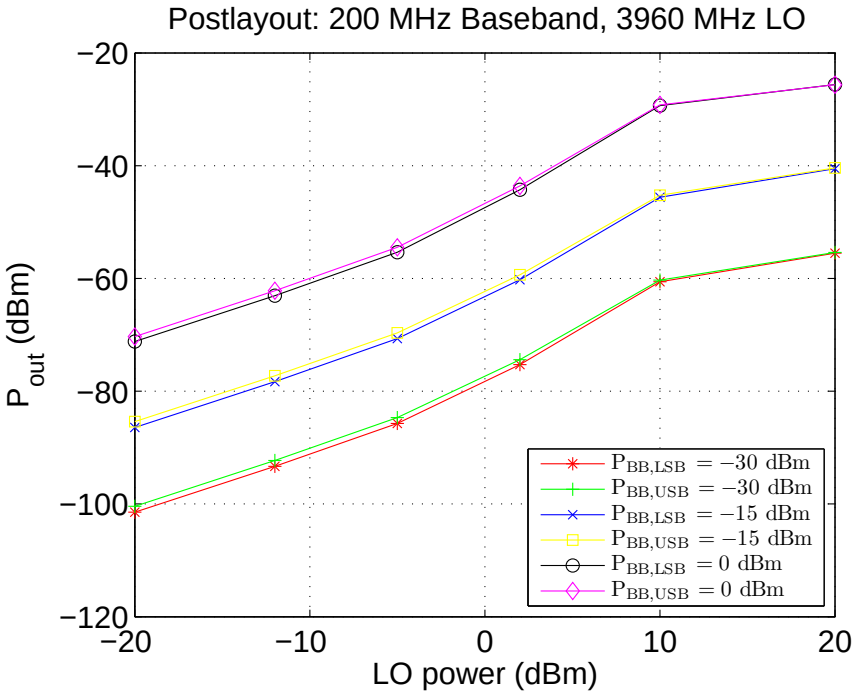

Fig. 84.: UWB mixer post-layout sims. 200MHz baseband and 3960MHz LO.

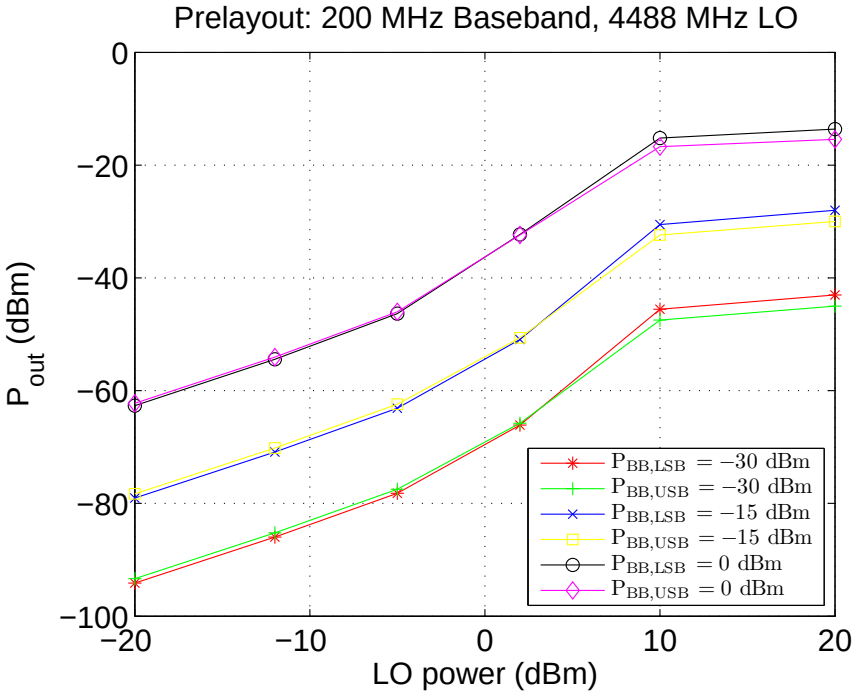

Fig. 85.: UWB mixer pre-layout sims. 200MHz baseband and 4488MHz LO.

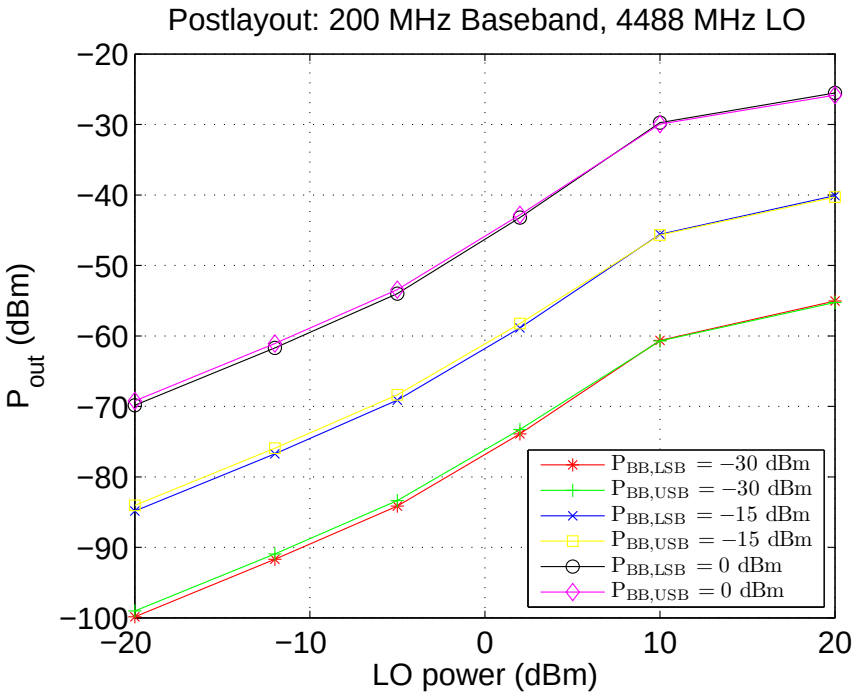

Fig. 86.: UWB mixer post-layout sims. 200MHz baseband and 4488MHz LO.

back and control the LSB of the DAC. If the signal level is too high, reducing the LSB of the DAC will also reduce the output swing of the signal. Therefore, with the designed PAR, this will help mitigate any issues arising from too large of a signal level.

The circuit is based on the Meyer power detector [106] with an additional feedback path added to the negative output. The peak detector, shown in Fig. 87, is then followed by a second-order passive LPF and a differential to single-ended converter which acts as a buffer for the output of the filter to reduce loading. The post-layout simulation results are shown in Fig. 88 for all three mode-I UWB sub-bands.

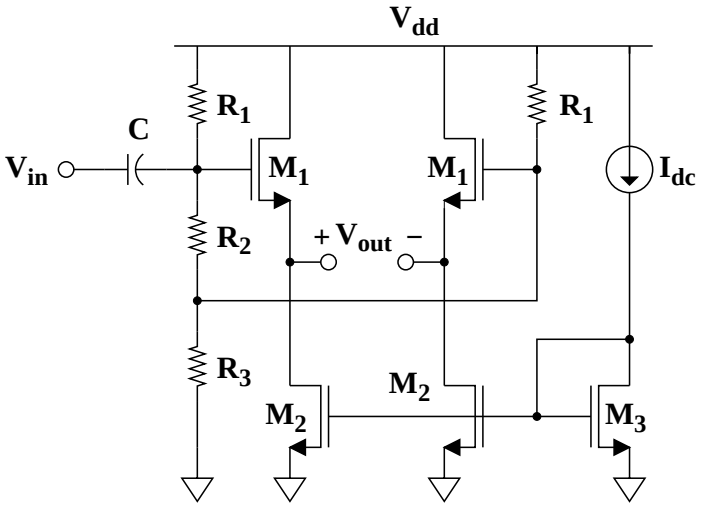

Fig. 87.: UWB power detector schematic.

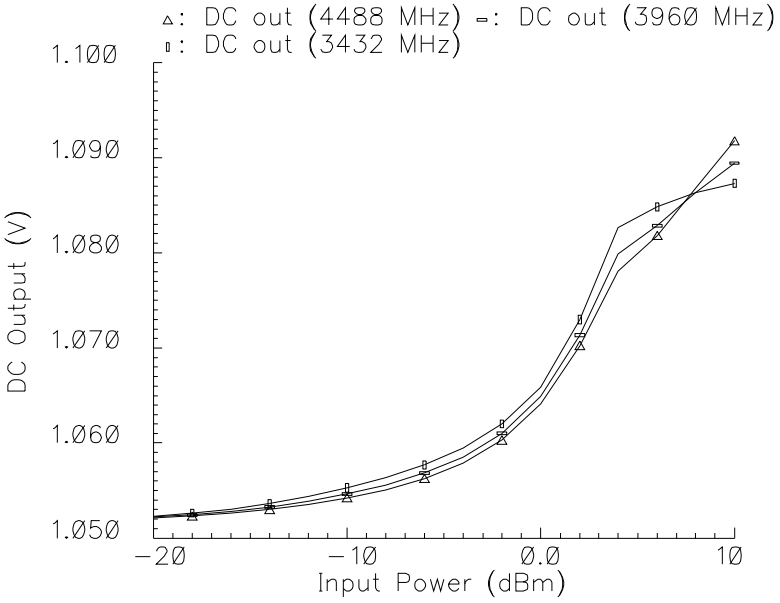

Fig. 88.: UWB power detector post-layout DC output.

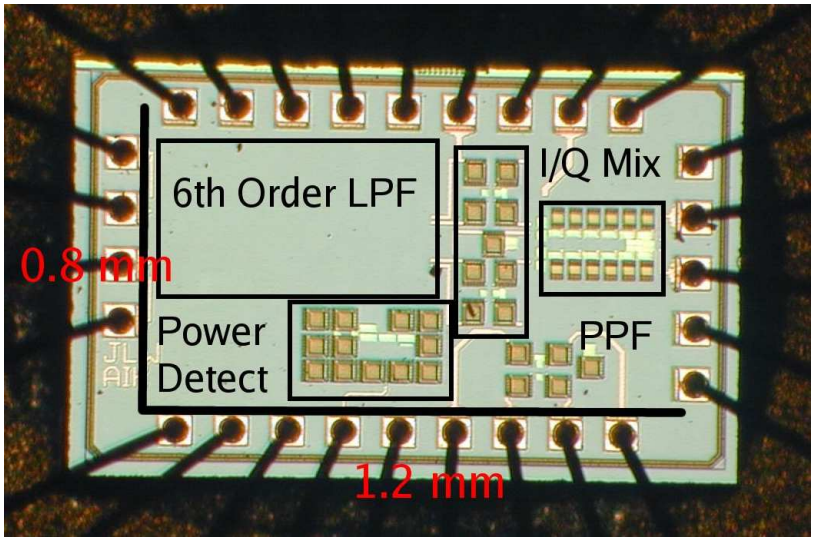

Fig. 89.: UWB TX chip micrograph.

D. Measurement Results

The chip micrograph of the UWB TX is shown in Fig. 89. Simulations and layout were carried out using Cadence and the fabrication was provided by United Microelectronics Corporation (UMC). The circuit was packaged in a QFN 28 pin package and mounted on a 2 sided FR4 substrate PCB. The output of the I mixer is shown in Fig. 90. The LO-to-RF isolation is only approximately 30 dB (as seen from the figure). Fig. 93 shows the measured mixer output level vs. LO amplitude. Based on measurement results, there is an approximate 15 dB additional attenuation due to board and chip parasitics than was initially considered during circuit design. To compensate for these effects, the baseband signal level for the measured results is 15dB higher than the simulation results. However, the measurement and simulation results are in good agreement. Figs. 90, 91, 92, and 93a show the measurement results for the UWB mixer at different LO frequencies. Fig. 93b shows the measured power detector output at the center of all UWB bands. Although there is some deviation

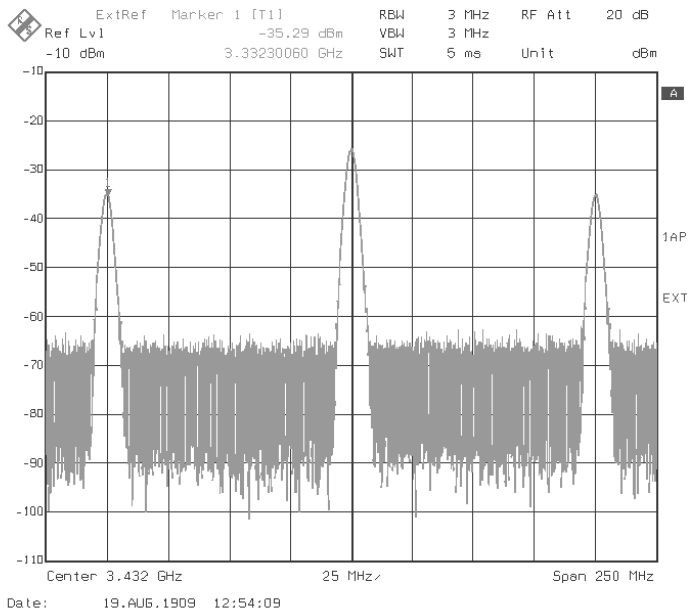

Fig. 90.: Measured I channel mixer output 3432MHz LO 100MHz BB.

between bands, the output is relatively consistent and provides a good measure of predicting the signal strength.

E. Conclusion

A TX designed for mode-I MB-OFDM UWB has been presented. The system consists of a LPF, mixer, driver amplifier and power detector. The entire system was fabricated in UMC 0.13μm CMOS using standard components. The LPF consisted of three identical pseudo-differential biquad stages with 5-bit digital programmability. The mixer is a pseudo-differential Gilbert-cell mixer and the antenna driver is a simple common source amplifier with resistive load. The implemented power detector is based on the Meyer power detector and simulations show it is relatively constant within the bands of interest. The system level block allocation as well as the block designs were discussed then simulation and measurement results were presented.

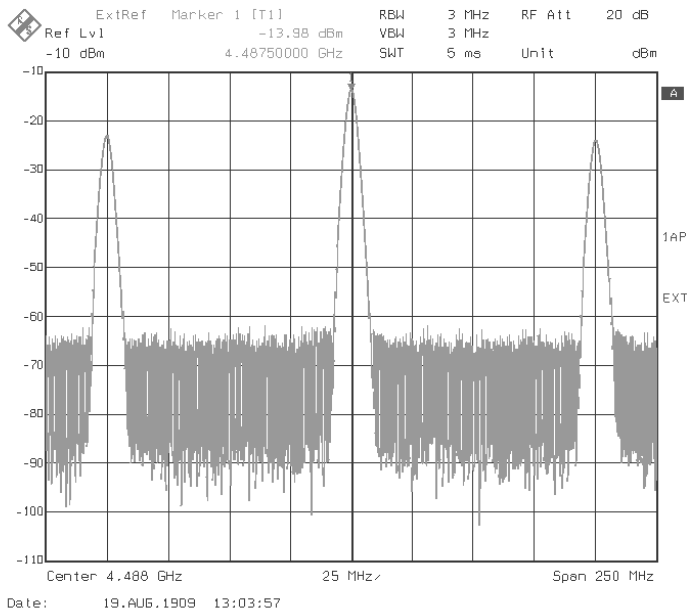

Fig. 91.: Measured I channel mixer output 4488MHz LO 100MHz BB.

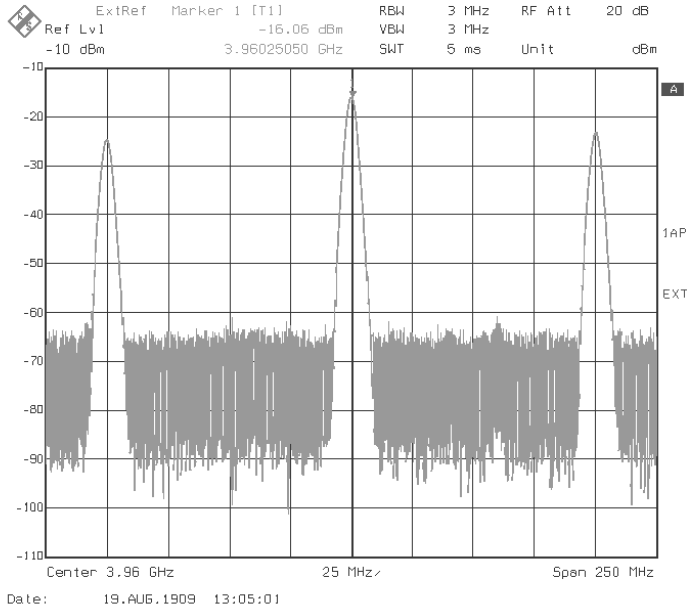

Fig. 92.: Measured I channel mixer output 3960MHz LO 100MHz BB.

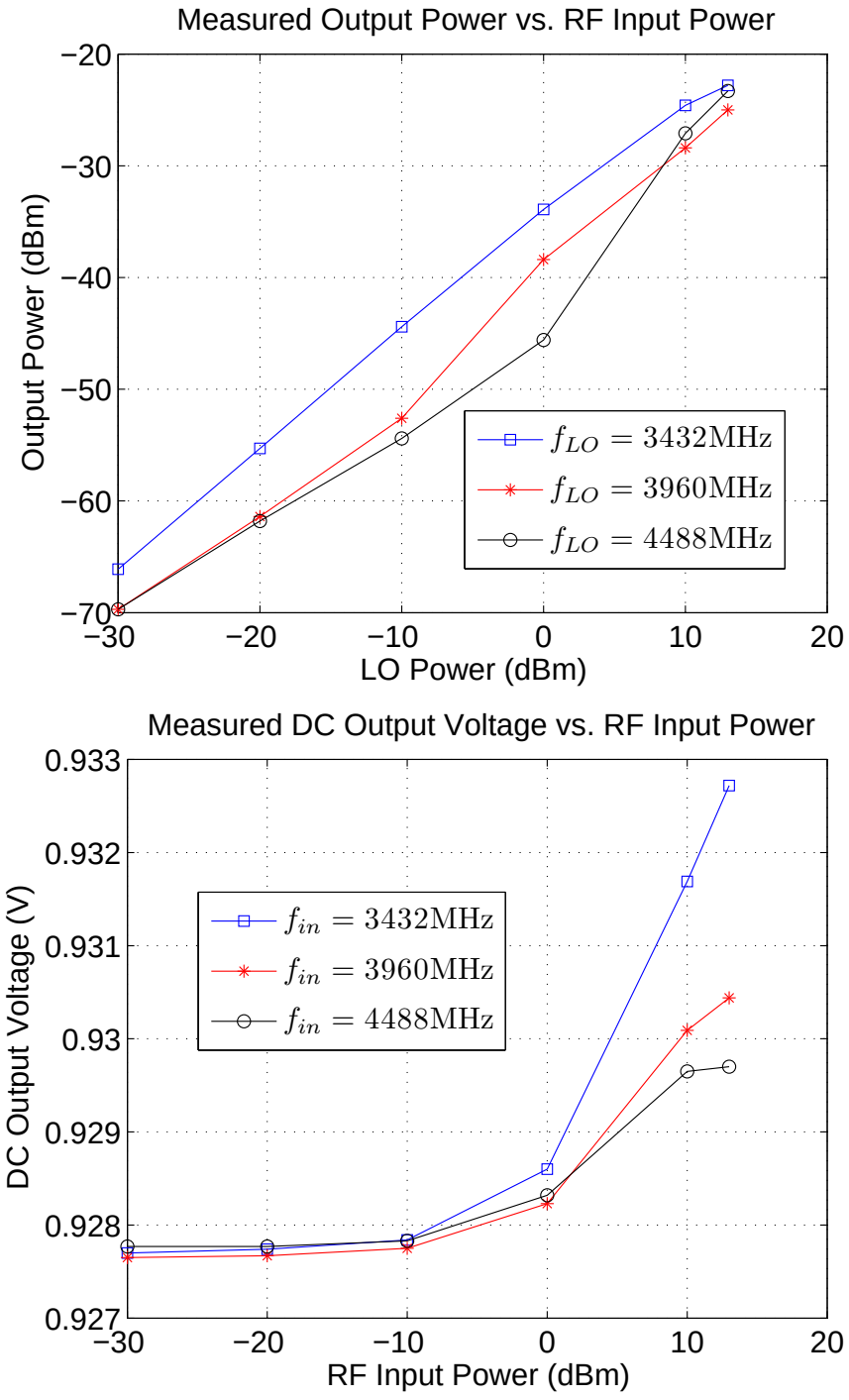

Fig. 93.: a) Measured I channel mixer output power as a function of LO amplitude; b) Measured power detector output.

CHAPTER VIII

CONCLUSIONS AND FUTURE WORK

It has been shown that magnetic shape memory alloys (MSMAs) are a viable candidate to be used for low-frequency energy harvesting for structural health monitoring (SHM) of highway bridges. A low-voltage, low-power, high conversion efficiency rectifier multiplier (RM) architecture as designed, fabricated, and tested to convert the AC output from the MSMA pick-up coil into a usable DC voltage. Different load resistances were used to emulate next-stage loading circuitry and obtain numerical results for practical power delivery. A commercially available strain gage was suggested to collect strain data from a bridge and a low-power successive approximation register analog-to-digital converter (SAR ADC) was designed, fabricated, and tested. The proposed SAR ADC provided a low-power and relatively accurate solution for digitizing the analog sensor information. Additionally, an impulse radio ultra-wideband (IR-UWB) transmitter (TX) study was presented and a low-power topology was shown to be a viable solution for wireless transmission of the SAR ADC output. The RM and the SAR ADC were fabricated in ON 0.5μ CMOS.

Furthermore, a mode-I MB-OFDM UWB TX was presented and utilized standard components and no special process options at achieving the desired target. The fabricated TX consisted of a 6^{th} order low pass filter, an I/Q upconversion mixer, an antenna driver and a power detector. Measurement results show the output of the mixer was able to work at the proposed frequency range. The circuit was fabricated in UMC 0.13μm CMOS.

A. Future Work/Research Suggestions

The work presented was a case study into the plausibility of generating usable DC levels out of very low input amplitudes as well as whether or not MSMAs would be suitable for deployment in SHM systems. There are a few main areas within the overall system which could be addressed for further research endeavors.

- Fabrication of a single chip comprising the RM, power conditioning circuitry, ADC, and IR-UWB TX.
- Deploying a test system on a bridge and obtaining real-time measurements.
- Further characterization and research into different materials for energy harvesting.
- Rectifier studies using low-V_{th} CMOS devices and/or using the RM to re-charge a battery instead of using a passive system.
- Re-design of all blocks in an optimum process of either 90, 130, or 180nm CMOS (optimum due to size, design kit options, and V_{th} of all devices in the range of 400mV.
- Designing a sensor for deployment in the proposed system.

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