FREQUENCY SYNTHESIZERS AND OSCILLATOR ARCHITECTURES BASED ON MULTI-ORDER HARMONIC GENERATION

A Dissertation

by

MOHAMMED MOHSEN ABDUL-SALAM ABDUL-LATIF

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2011

Major Subject: Electrical Engineering

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ABSTRACT

Frequency Synthesizers and Oscillator Architectures Based on Multi-Order Harmonic Generation. (December 2011)

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Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Frequency synthesizers are essential components for modern wireless and wireline communication systems as they provide the local oscillator signal required to transmit and receive data at very high rates. They are also vital for computing devices and microcontrollers as they generate the clocks required to run all the digital circuitry responsible for the high speed computations. Data rates and clocking speeds are continuously increasing to accommodate for the ever growing demand on data and computational power. This places stringent requirements on the performance metrics of frequency synthesizers. They are required to run at higher speeds, cover a wide range of frequencies, provide a low jitter/phase noise output and consume minimum power and area. In this work, we present new techniques and architectures for implementing high speed frequency synthesizers which fulfill the aforementioned requirements.

We propose a new architecture and design approach for the realization of wideband millimeter-wave frequency synthesizers. This architecture uses two-step multi-order harmonic generation of a low frequency phase-locked signal to generate

wideband mm-wave frequencies. A prototype of the proposed system is designed and fabricated in 90nm Complementary Metal Oxide Semiconductor (CMOS) technology. Measurement results demonstrated that a very wide tuning range of 5 to 32 GHz can be achieved, which is costly to implement using conventional techniques. Moreover the power consumption per octave resembles that of state-of-the art reports.

Next, we propose the *N*-Push cyclic coupled ring oscillator (CCRO) architecture to implement two high performance oscillators: (1) a wideband *N*-Push/*M*-Push CCRO operating from 3.16-12.8GHz implemented by two harmonic generation operations using the availability of different phases from the CCRO, and (2) a 13-25GHz millimeter-wave *N*-Push CCRO with a low phase noise performance of -118dBc/Hz at 10MHz. The proposed oscillators achieve low phase noise with higher *FOM* than state of the art work.

Finally, we present some improvement techniques applied to the performance of phase locked loops (PLLs). We present an adaptive low pass filtering technique which can reduce the reference spur of integer-*N* charge-pump based PLLs by around 20dB while maintaining the settling time of the original PLL. Another PLL is presented, which features very low power consumption targeting the Medical Implantable Communication Standard. It operates at 402-405 MHz while consuming 600μW from a 1V supply.

DEDICATION

To my beloved parents,

my dear wife Yomna, and my son Ibraheem

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CHAPTER I

INTRODUCTION

1.1 Motivation

Semiconductor circuits have become an integral part of our everyday life. Computers, portable electronics, communication devices, home entertainment and medical devices are just few examples. All these devices rely heavily on digital and analog circuits. From a birds eye view these devices always possess some kind of transmission and reception circuits to transmit and receive the needed data, voice, images or videos. They also have processing units which are responsible of manipulating the data and transforming it to intelligible information. Also, nowadays, demand for more bandwidth is ever increasing; data rates are getting higher and higher. This enables browsing the internet over cell-phones or watching video on demand on laptops and makes it available for a huge number of uses simultaneously. This requires that the circuits processing these amounts of data work at increasingly faster rates. The maestro of these circuits is the clock generating circuits producing the required fast clocks which drive the digital circuits and synchronizes their operation so they are able to correctly process the data and accommodate these fast rates concurrently. In addition, for wireless transmission and reception to accommodate these large bandwidths, wireless circuits now have to work at higher frequencies and cover wider ranges of frequencies as well.

This dissertation follows the style of *IEEE Journal of Solid-State Circuits.*

In addition, for wireless transmission and reception to accommodate these large bandwidths, wireless circuits now have to work at higher frequencies and cover wider ranges of frequencies as well. Again, clock generator circuits or in this case called frequency synthesizers are needed to transform the voice and date which are at lower frequencies to these higher frequencies.

Hence, frequency synthesis circuits or clock generators are essential building blocks in nearly every electronic system. Therefore, they have received a lot of attention by designers in academia and industry alike and have developed greatly across the past years. However, as described above, improved performance is required from frequency synthesizers to be able to supply the required frequencies/clocks to the increasingly faster circuits. Performance of frequency synthesizer is measured using a number of metrics: 1) the frequency of operation, 2) the bandwidth covered (also called tuning range), 3) the phase noise of the output signal, 4) the output amplitude, 5) the power consumption and 6) the consumed area.

In this work, we propose new architectures and techniques to improve the performance metrics of state of the art frequency synthesizers. We propose an architecture that enables high frequency (millimeter-wave frequencies) and wideband operation simultaneously. We also propose ways to lower the phase noise of voltage controlled oscillators while operating at high frequencies. Finally, we propose a phase locked loop design that features a low-reference spur performance and a second that features very low power consumption for medical applications.

1.2 Organization

Chapter II starts with a survey on the wideband millimeter-wave (mm-wave) frequency generation techniques and their drawbacks and points to the bottle necks of these designs. A new architecture for wideband mm-wave frequency synthesis is then proposed. This architecture uses two-step multi-order harmonic generation of a low frequency phase-locked signal to generate wideband mm-wave frequencies. Detailed architecture and circuit analysis and design is then presented. This design uses inductor-based oscillators. Finally, measurement results are shown illustrating the performance of the design circuits.

In Chapter III, we propose to use *N*-Push cyclic coupled oscillators to improve the performance of ring oscillators (inductor-less oscillators). We first analyze the operation of CCROs using the concept of injection locking described by the generalized Adler's equation and we derive the phase noise expression. Next, we present two high performance *N*-Push CCRO design examples based upon the proposed technique. The oscillator prototypes are fabricated in a 90nm digital CMOS process and measurement results are provided.

Chapter IV focuses on enhancing the performance of phase locked loops (PLL). In the first design we are concerned with reducing the reference spur in integer-N frequency synthesizers. We propose an adaptive low-pass filtering technique and apply it to an integer-N charge pump based PLL. Measurement results show that the reference spur suppression is improved by 20 dB over a conventional frequency synthesizer. The second design is a very low power PLL for the Medical Implantable Communications

Standard (MICS). The designed PLL consumes 750 μW which makes it suitable for implantable transceivers. Chapter V concludes this work.

CHAPTER II

A WIDEBAND MILLIMETER-WAVE FREQUENCY SYNTHESIS ARCHITECTURE USING MULTI-ORDER HARMONIC-SYNTHESIS AND VARIABLE N-PUSH FREQUENCY MULTIPLICATION*

2.1 Introduction

Millimeter-wave (mm-wave) frequencies offer large bandwidths not available at lower frequencies and hence have numerous potential applications such as: personal area networking with speeds of hundreds of Mbps, high definition multimedia and uncompressed HDTV. Consequently several standards have emerged which make use of this bandwidth such as IEEE 802.16 (10-66 GHz), IEEE 802.16a (2-11GHz) and recently IEEE 802.15.3c (57-66 GHz). In addition, emerging software defined radios and cognitive radios are also required to operate over wide range of frequencies [1]. Furthermore, the advancement of silicon-based submicron-CMOS technologies has pushed the f_T of transistors to frequencies higher than 300 GHz and hence, can realize mm-wave circuits at an affordable cost.

Implementing flexible mm-wave transceivers which can cover these wide frequency ranges while efficiently maintaining acceptable performance is challenging. In particular, frequency synthesizers (FS) or phase-locked loops (PLLs) are one of the main

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design bottle-necks. The above-mentioned standards require tuning ranges (TR) (defined as the ratio of the bandwidth to the band center frequency) from 14.6% to 147%, which impose unique challenges on the FS design. The FS should provide phase-locked frequency tones for a large range of mm-wave frequencies with accurate channel frequency selection, fine resolution and reasonable power consumption. Conventional PLL-based frequency synthesizers cannot operate at such frequencies and bandwidths without great cost or severe performance degradation. The main design bottlenecks are the dividers and the voltage controlled oscillators (VCOs). Dividers at mm-wave frequencies usually employ injection-locked architectures which unfortunately suffer from narrowband characteristics and high power consumption [2]. Moreover, mismatches between the VCO and the divider tuning characteristics can reduce the usable portion of the VCO tuning range significantly [3]. In addition, these dividers have small division ratios and hence obtaining a large ratio between the reference frequency and the VCO output frequency (needed to realize closely spaced channels at mm-wave frequencies) requires multiple stages of these dividers until the frequency is low enough for a static divider, resulting in huge power consumption [2]. Also, VCOs with wide tuning ranges usually have large and/or varying frequency gain (K_{vco}). A large K_{vco} degrades the PLL's phase noise and spur suppression due to higher sensitivity to the control voltage perturbations while a varying K_{vco} affects the loop dynamics and degrades its stability.

Several design techniques have been reported to generate phase-locked mm-wave frequencies. Most of these techniques employ VCOs with LC tanks to achieve high

output frequencies. One example is to provide a phase-locked signal by operating a lower frequency VCO within a PLL and then extracting its harmonics using Push-Push techniques [4-6] or up-converting its output using an up-conversion mixer [7],[8]. Another technique uses one of the harmonics of this lower frequency PLL to injection-lock a higher frequency VCO [1], [9-11]. Although these techniques have wider tuning ranges than conventional PLLs, their tuning ranges are less than 36%.

On the other hand, different approaches have been adopted to widen the VCO tuning range. Examples include VCOs which employ switched-varactor banks [12], switched inductors [13], coupled resonators [14], triple-mode coupled resonators [15], standing wave oscillators [16], and triple-tuned VCOs [17]. However, most of the above bandwidth-extension techniques were reported in standalone VCO structures. PLLs incorporating such wideband VCOs, will suffer from the varying K_{vco} and the limited tuning range of mm-wave dividers.

Another technique to generate a wide range of phase-locked frequencies (prevalent in UWB frequency synthesizers) is to have a PLL operating at a high frequency and then follow it with a group of dividers and mixers to generate the required frequency tones [18]. However, these tones are spread out in frequency with limited tuning range and hence, do not provide a continuous tuning range. Also, this method suffers from high power consumption as the PLL is operating near the highest frequency.

Recently, PLLs tuned over an octave of frequency (6-12GHz) were employed and then lower frequency tones are generated through divide by two circuits [19].

However, obtaining an octave of tuning range at mm-wave frequencies is not practically feasible. The LC budget is limited by device parasitics and cannot be tuned widely. According to [3], recent reports in CMOS technology operating near 40–60 GHz have tuning ranges of less than 5 GHz such as references [16]–[18] in [3]. Also [20] covered the range of 20-28GHz (tuning range of 33%) using two VCOs with tuning ranges of 15% and 18% and then divided down using different division ratios to generate the lower frequencies. A tuning range of 0.125-26GHz was reported in [21]. This work uses four VCOs to generate frequencies from 8-16GHz. This prevents each VCO from having a large and varying K_{VCO} which deteriorates the dynamics of the PLL. However, this is in-efficient in area and power. It also uses CML dividers which consume 108mW at 8GHz. The complete PLL consumes nearly 1W of power which limits its use in portable devices. In addition, it uses mixers to generate the higher frequencies which can generate undesired tones that would have to be filtered-out over a wideband of frequencies which again adds more complexity, area and power penalties.

This work provides an architectural solution to wideband mm-wave frequency synthesis. The proposed architecture exploits multiple multi-factor frequency multiplications to achieve a tuning bandwidth of 27GHz over the range of 5-32GHz (tuning range of 146%). We propose a realization to this architecture using a digital harmonic synthesis block (DHSB) combined with a wideband multi-phase injection-locked VCO (IL-VCO) followed by a variable *N*-Push frequency multiplier. This chapter is organized as follows: Section 2.2 presents the proposed system and frequency planning, Section 2.3 presents the implementation details and simulation results of the

system building blocks while Section 2.4 presents the phase noise analysis of the system. Section 2.5 presents experimental measurement results while Section 2.6 concludes the chapter.

2.2 Proposed Frequency Synthesizer Architecture

2.2.1 Proposed System Architecture

Fig. 1 illustrates the block diagram of the proposed architecture. A low frequency PLL provides an input phase-locked signal (S_1). This signal then gets shaped using a digital harmonic-synthesis block (DHSB) such that one of its higher-order harmonics is enforced and amplified and the neighboring harmonics are attenuated. This enforced harmonic tone injection-locks a wideband *N*-phase injection-locked VCO (IL-VCO). By choosing different harmonic orders in the DHSB, we can achieve a wider phase-locked tuning range at the output of the oscillator (S_2). In addition, suppression of the harmonics of S_1 by the DHSB reduces the amount of spurs in the output of the IL-VCO. In our system, we propose to use injection locked VCOs as their tuning range and phase noise is independent of their frequency gain, K_{VCO}. The *N*-phase oscillator provides *N* equally-spaced phase-shifted output signals. These phase-shifted signals are then combined, in a second harmonic generation step, using a variable *N*-Push frequency multiplier [22] to increase the frequency and bandwidth even more (S_3). Finally, a wideband amplifier boosts the signal amplitude and drives the 50Ω of the testing equipment. The two harmonic-generation steps “up-convert” the low frequency output of the PLL to mm-

wave frequencies and the different harmonic-generation factors provide a wide tuning range.

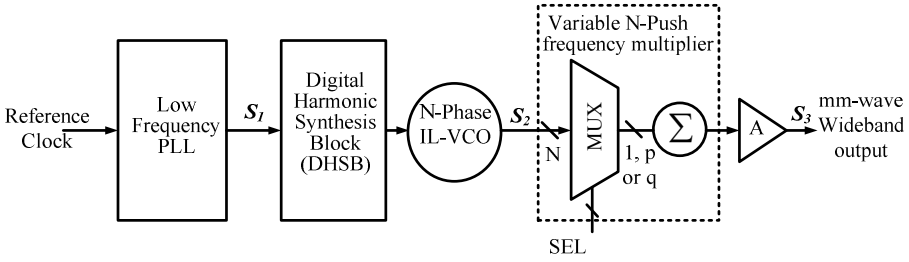
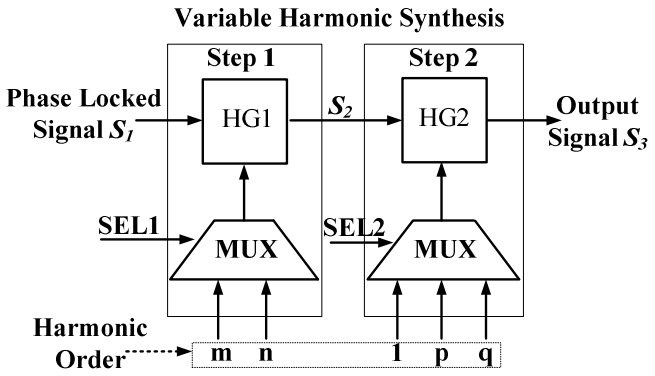
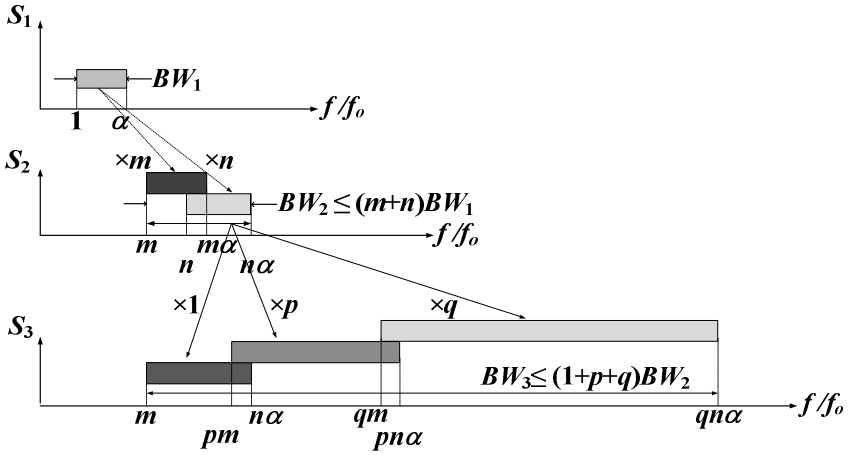


Fig. 1 Block diagram of the proposed system

In contrast to conventional PLLs, this technique has several advantages. First it uses a low frequency PLL which could be easily optimized. Second, the operation of the mm-wave IL-VCO is independent of the value of K_{VCO}. Third, using an IL-VCO avoids the use of power hungry dividers. Finally this architecture can readily leverage the already reported wideband stand-alone VCO structures provided these VCOs can be modified to work as multi-phase injection-locked VCOs (which can be realized in most cases).



(a)



(b)

Fig. 2 (a) Conceptual block diagram of the proposed system with the harmonic generation (HG) (b) Spectrum showing the bandwidth extension at different points in the system

2.2.2 Frequency Planning

A conceptual block diagram of the proposed FS is shown in Fig. 2(a) along with an illustrative frequency-spectrum diagram in Fig. 2(b). A phase-locked input signal S_1 with a frequency range from f_o to αf_o (where $\alpha > 1$ is the input frequency ratio across the

input frequency band) and a tuning bandwidth BW_1 (where $BW_1 = f_o(\alpha - 1)$) is frequency multiplied by one of two integer factors: m or n (where $n>m$). Frequency multiplication is practically implemented by the harmonic generation of the mth or nth harmonics. This operation results in a higher frequency signal S_2 with a frequency range from mf_o to nof_o and an extended tuning bandwidth BW_2 which is less than or equal to $(m+n)BW_1$. Similarly, the frequency multiplication (or harmonic generation) process is repeated once more with one of the integer factors: *1*, *p,* or *q*, (where $q>p$) producing the signal S_3 (ranging from mf_o to $qnof_o$) with a tuning bandwidth BW_3, where BW_3 is less than or equal to $(1+p+q)BW_2$. This multi-step multi-factor frequency multiplication enables the final signal S_3 to reach mm-wave frequencies and have a very wide tuning range simultaneously. BW_1, *m*, *n, p, and q* can be chosen to provide continuous or discontinuous frequency tuning ranges depending on the application requirements to achieve the best efficiency and cover the required frequency ranges simultaneously. Moreover, this multiplication process, in principle, could be repeated several times using two or more frequency multiplication factors at each step. Fig. 3 depicts the spectrum of the signal at each point along the proposed system. It can be observed how the desired harmonics are enforced and the undesired ones are attenuated.

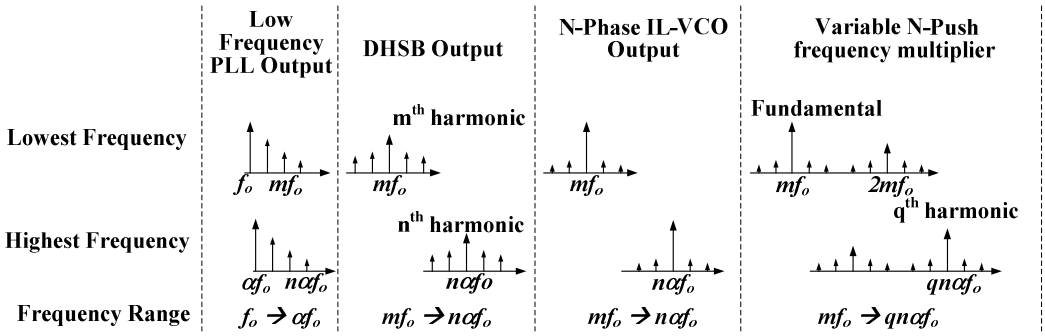


Fig. 3 Frequency spectrum at each point along the proposed system

As shown in Fig. 2(b), to obtain a continuous tuning range the following inequalities should be satisfied: $n \le \alpha m$, $p \le n\alpha/m$, and $q \le pn\alpha/m$. The maximum tuning range is achieved when,

$$\alpha = n / m \tag{2.1}$$

$$p = n\alpha/m \tag{2.2}$$

$$q = pn\alpha/m = p^2 \tag{2.3}$$

Substituting (2.1) in (2.2) leads to,

$$p = (n / m)^2 \tag{2.4}$$

However *m*, *n* and, *p* are integers; so (2.4) cannot be satisfied in a general sense. Hence, *p* may be increased or decreased to the nearest integer. However, from (2.2) decreasing *p* means decreasing α and hence the first inequality ($n \le \alpha m$) will be violated. Thus, we choose the next larger integer for *p*. In this case there will be some overlap in the first frequency range as $\alpha > n / m$. Thus, to obtain a continuous tuning range, *p*, α and *q* are given by,

$$p \geq \left(\frac{n}{m}\right)^2 \text{ where } p \in \mathbb{Z}^+ \tag{2.5}$$

$$\alpha = \left(\frac{m}{n}\right) p \tag{2.6}$$

$$q = p^2 \tag{2.7}$$

In practice, some overlap between the frequency bands is desirable for reliable operation. Since p is the next larger integer, several values of m and n could yield the same p. However the value of α will be different in each case. For example, (m,n) equal (5,7) and (7,9) yield p=2 while α=1.43, 1.56. These are represented by the first two points of the curves shown in Fig. 4. Table 1 lists the tuning range (TR) at each point in the system for the continuous output tuning range determined by equations (1)-(3). Fig. 4 plots these tuning ranges for different values of α and p, produced by different combinations of m and n each ranging from 2 to 9. Note that there is a greater tuning range enhancement after two frequency-multiplication steps (TR_3 of the signal S_3) than after one multiplication step (TR_2 of the signal S_2). Furthermore, the output tuning range is constant for a certain p and hence choosing the smallest input frequency ratio (α) reduces unnecessary overlap in the frequency bands. For our design, we choose p=2 (hence q=4) which can be implemented using different combinations of m and n. We choose m=5 and n=7 and accordingly the smallest corresponding α is 1.43. Table 2 presents the frequency plan adopted in this work. Hence, starting with a low frequency PLL with a tuning range of 35%, we can theoretically reach a final frequency range of 5-40GHz, with a much wider tuning range of 155%, using the proposed architecture.

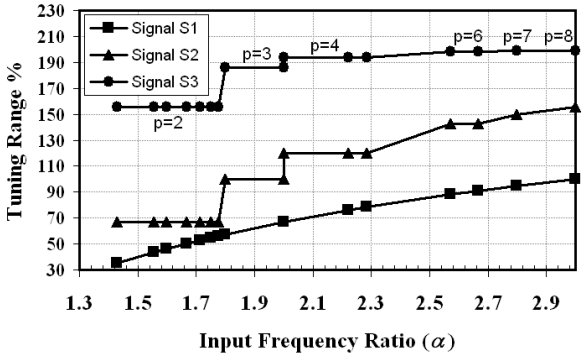


Fig. 4 Tuning range at different points in the system

Table 1 Tuning range expressions at different points in the system

Signal	Tuning Range
S_1	$TR_1 = \frac{2(\alpha-1)}{(\alpha+1)}$
S_2	$TR_2 = \frac{2(\left(\frac{n\alpha}{m}\right)-1)}{(\left(\frac{n\alpha}{m}\right)+1)}$
S_3	$TR_3 = \frac{2(\left(\frac{n\alpha}{m}\right)^3-1)}{(\left(\frac{n\alpha}{m}\right)^3+1)}$

Table 2 Frequency plan of the proposed frequency synthesizer

Low PLL Frequency (S_1)	**Harmonic Synthesis**	**Operating Freq. of IL- VCO (S_2)**	***N*-Push Multiplication**	**Output Frequency (S_3)**
1 – 1.43 GHz (TR~35%)	5th harmonic	5 – 7.15 GHz	x 1 ➔ 5 – 10 GHz	5 – 40 GHz (TR~155%)
	7th harmonic	7 – 10 GHz	x 2 ➔ 10 – 20 GHz x 4 ➔ 20 – 40 GHz	

2.3 Circuit Implementation

The first block in the system is the low frequency PLL. The tuning range of the VCO within this PLL is 35%. In most cases, this range is divided into bands controlled by a bank of digitally controlled varactors. This helps reduces the gain of the VCO and keeps it constant over all bands. Also, the bias current should be scaled to maintain the phase noise performance. The VCO gain and phase noise could be optimized also by dividing the band among two or more VCOs, each optimized in a much smaller band as in [19]. These are low frequency VCOs and hence, the power penalty is much lower. Another technique employs amplitude control to maintain the VCO performance over the whole tuning range [23]. Since, the low frequency PLL is well documented in literature it is not included in our proof-of-concept prototype. The following sub-sections present the circuit details of the implemented building blocks. A block diagram of the implemented part of the system is shown in Fig. 5. Analysis and design of each block is also presented in this section.

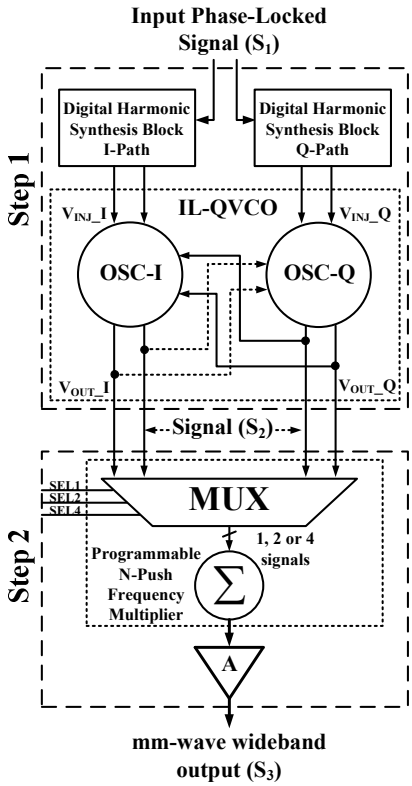


Fig. 5 Block diagram of the implemented prototype

2.3.1 Digital Harmonic Synthesis Block (DHSB)

The principal role of this block is to provide a clean tone at the *m*th or *n*th harmonic of the phase-locked input signal by amplifying the desired harmonic and attenuating the surrounding ones. Previously, sub-harmonic pulsed injection was used in literature to do this function [24]. However, sub-harmonic pulsed injection works poorly in the presence of neighboring harmonics with comparable amplitude, resulting in spurious tones in the output spectrum. Pulsed injection also suffers from low injection amplitude due to the limited energy of the injected pulse, which translates to a narrow

locking range in the IL-VCO. The latter problem has been addressed by adding a correction technique [25] to make the IL-VCO track the input signal frequency; however, it uses a highly-digital tuning loop which has narrow band operation as well. In this work, we modify a technique used to generate highly-linear sinusoidal oscillators in MHz ranges [26] to create the required injection tones with higher amplitude and hence wider locking range while simultaneously suppressing the spurious tones. The basic idea of this technique relies on the fact that *time shifts* or *delays* of a signal in the time domain translates to *phase changes* to the signal in the frequency domain. By choosing certain time shifts for a certain number of signals and then adding them together we can preserve a certain harmonic and cancel out others. The simplest illustrative case occurs in a differential pair where subtracting 180^{o}-out-of-phase signals cancels the even harmonics. We term this harmonic cancellation "*the synthesis process*". For a more general case, consider a periodic time-domain signal $x(t)$ with a frequency f_o. Its frequency-domain representation is $X(\Omega)$ where $\Omega=k\Omega_0$ and $\Omega_0=2\pi f_0$ and k is an integer because periodic signals have discrete line spectra. Hence, $x(t-\Delta t) \leftrightarrow X(\Omega)e^{-j\Omega\Delta t}$. Adding M signals with different time shifts yields,

$$\begin{aligned} y(t) &= x(t-t_1)+x(t-t_2)+\ldots.+x(t-t_M) \\ &= x(t-n_1\Delta t)+x(t-n_2\Delta t)+\ldots.+x(t-n_M\Delta t) \end{aligned} \tag{2.8}$$

where $t_1, t_2, .. , t_M$ have Δt as the greatest common factor and n_i is an integer. The frequency domain signal of the sum, $Y(\Omega)$, is given as,

$$\begin{aligned} Y(\Omega) &= X(\Omega)[e^{-j\Omega n_1\Delta t}+e^{-j\Omega n_2\Delta t}+\ldots+e^{-j\Omega n_M\Delta t}] \\ Y(k\Omega_0) &= X(k\Omega_0)[e^{-jk(n_1\Delta\phi)}+e^{-jk(n_2\Delta\phi)}+\ldots+e^{-jk(n_M\Delta\phi)}] \end{aligned} \tag{2.9}$$

where $\Delta\phi=\Omega_0\Delta t$ and k is the harmonic order. Hence, the transfer function of this *synthesis process* for the *k*th harmonic is given by,

$$H(k,\phi_1,\phi_2,...,\phi_M) = H(k,\phi_i) = \frac{Y(k\Omega_0)}{X(k\Omega_0)} = [e^{-jk\phi_1} + e^{-jk\phi_2} + ... + e^{-jk\phi_M}] \text{ where } \phi_i = n_i\Delta\phi \tag{2.10}$$

The frequency-planning scheme and the overall system design determine the synthesis-process requirement, i.e. which harmonics to be enforced and the amount of suppression required for the adjacent harmonics. Thus, the chosen phase shifts $\phi_1, \phi_2, ... \phi_M$ should maximize $H(k=k_i,\phi_i)$, where k_i is the desired harmonic, and minimize $H(k \neq k_i,\phi_i)$ to achieve the required adjacent harmonic rejection. As mentioned in Section II-A, the first multiplication step requires two multiplication factors (*m* or *n*). These two factors are realized by selecting one of two harmonics (either the *m*th or *n*th harmonics) of the input signal. Hence, a different set of phase delays are needed for each harmonic to synthesize its corresponding transfer function ($H(m,\phi_i)$ or $H(n,\phi_i)$).

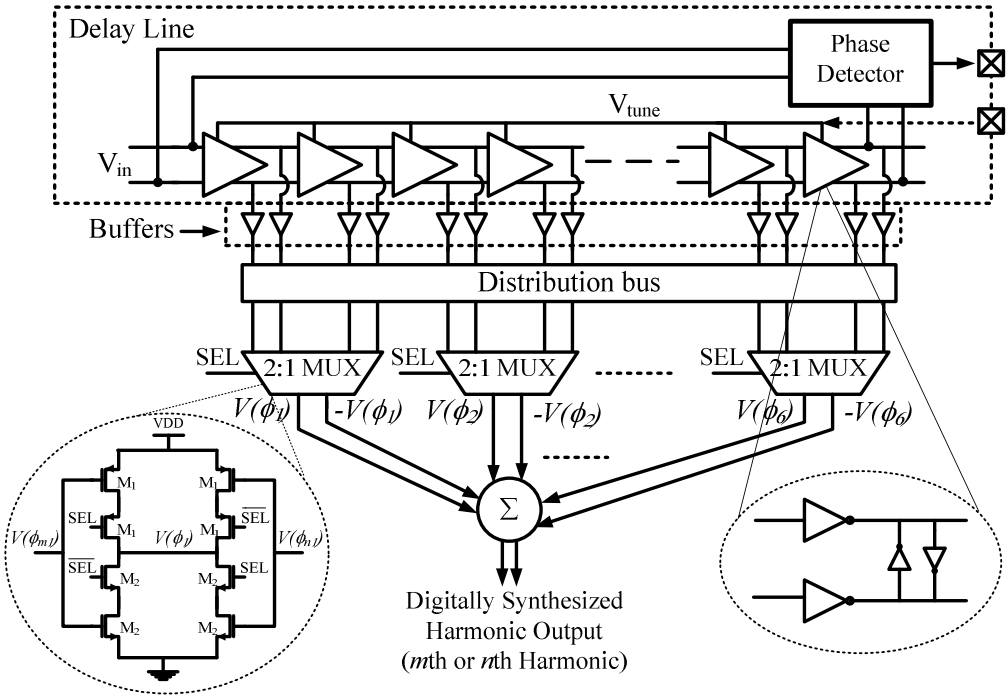


Fig. 6 Block diagram showing the DHSB

The proposed DHSB is shown in Fig. 6. A delay line time-shifts the input square-wave signal coming from the low-frequency PLL and provides the required discrete time shifts at its output nodes. A two-path delay line [27] is used as shown in Fig. 6. The delay line incorporates simple inverters as its delay elements as well as back-to-back inverters at each node to ensure a differential signal at both nodes. This delay line provides phases from 0 to 360^o using half the number of continuously-cascaded delay cells as compared to a one-path delay line. Hence, less supply-induced jitter accumulates along the line [27] and the line is less prone to mismatches among its delay elements. Each delay cell, consisting of one inverter in each path and the back-to-back inverters, is laid out as one unit and then repeated to minimize mismatches between the two delay

line paths. A phase detector (PD) compares the phase of the input of the delay line with the phase of its output and produces an error signal which is used to manually tune the supply of the inverters to change their delay (according to the input frequency) ensuring a complete 360^{o} phase shift along the delay line. A DLL could automate this procedure. The two sets of time-shifted signals are tapped out from the delay line using tapered buffers to reduce the loading on the delay line. These signals are then transmitted through a distribution bus to a group of digital multiplexers. The distribution bus ensures that all the signals arrive at the multiplexers with the same delay. The multiplexers, shown also in Fig. 6, choose between the set of signals required to synthesize the *m*th or *n*th harmonics. The last stage in the DHSB is the adder, shown in Fig. 7, which sums the individual signals of each set to produce the final synthesized output. Note that all signals are differential to suppress the even harmonics. Differential pairs acting as switching pairs convert the delayed voltage waveforms to current ones. These currents are then summed at the output using a linear poly resistor. The resistor value is chosen to produce adequate voltage swing at the output without limiting the bandwidth of the adder. The principal advantage of this structure is its ability to provide strong injection strength at the high-frequency synthesized harmonics such that a wide locking range can be achieved in the IL-VCO. We match the differential pairs to suppress even harmonics and also match the current sources to ensure that harmonics of the time shifted-signals have equal gains and hence cancel properly.

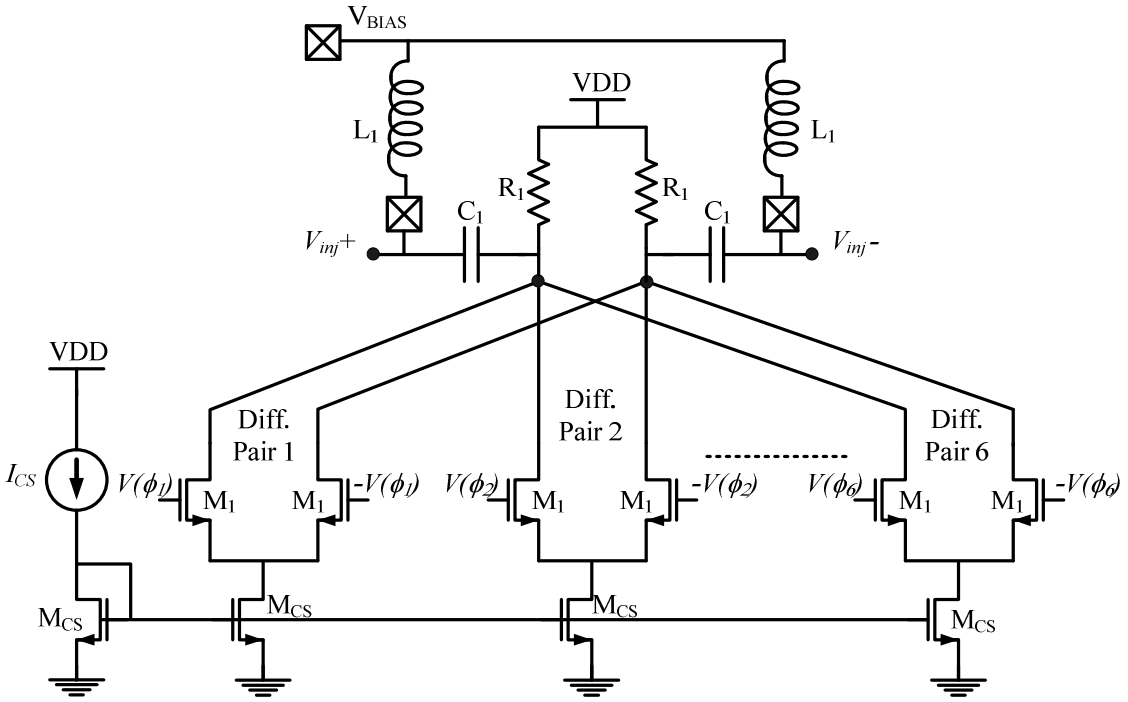


Fig. 7 Circuit diagram of the adder stage

Several practical considerations arise when designing the DHSB. First, using one delay line only while two sets of delays are needed (one for each harmonic) requires finding a common phase shift unit $\Delta\phi$ for both cases. This minimum $\Delta\phi$ is determined by the maximum number of delay stages employed in the delay line as well as the minimum achievable inverter-delay (at the maximum input frequency). The larger the number of delay stages, the smaller $\Delta\phi$ that can be achieved and the more accurate the cancellation process. However, increasing the delay line length decreases the maximum allowable input frequency and makes the delay line more prone to mismatches among the distant delay cells. Second, increasing the number of signals *(M)* which are added leads to more degrees of freedom in the synthesis process and hence more cancellation

of the adjacent harmonics. On the other hand, the maximum M is determined by the implementation/layout complexity to preserve symmetry among the different signal paths. Due to the above considerations, we choose six differential signals and a phase shift unit, $\Delta\phi$, of 10^{o}. Fig. 8 shows the phasor diagram for the phases employed in the DHSB. Selection of the 5th and 7th harmonics requires the addition of six signals with the phase shifts of (0^{o}, $\pm 70^{o}$, $\pm 140^{o}$, 360^{o}) and (0^{o}, $\pm 50^{o}$, $\pm 100^{o}$, 360^{o}), respectively.

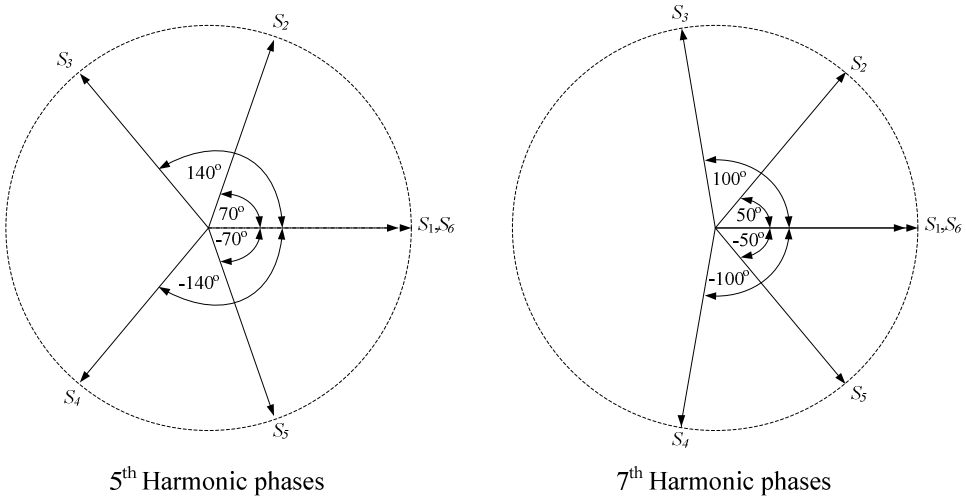
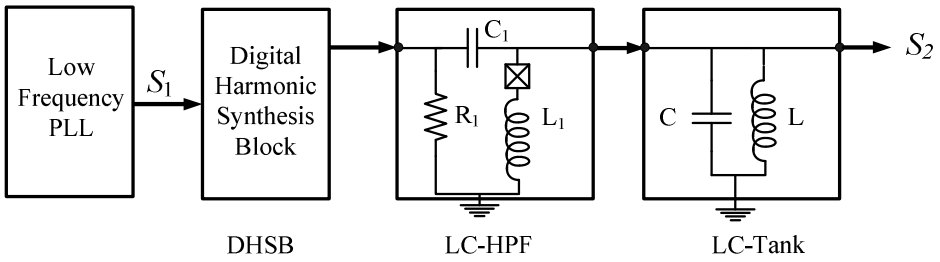


Fig. 8 Phasor diagram of the phase shifted signals used in the DHSB

Fig. 9(a) shows the filtering components of the building blocks used for the first multiplication step while Fig. 9(b) presents the Matlab® simulations of the normalized filtering transfer function of those blocks as well as the amplitudes of the different harmonics at the output of each filtering stage. The amplitude of the fundamental tone is suppressed by 15dB and 6db relative to the 5th and 7th harmonics, respectively. This

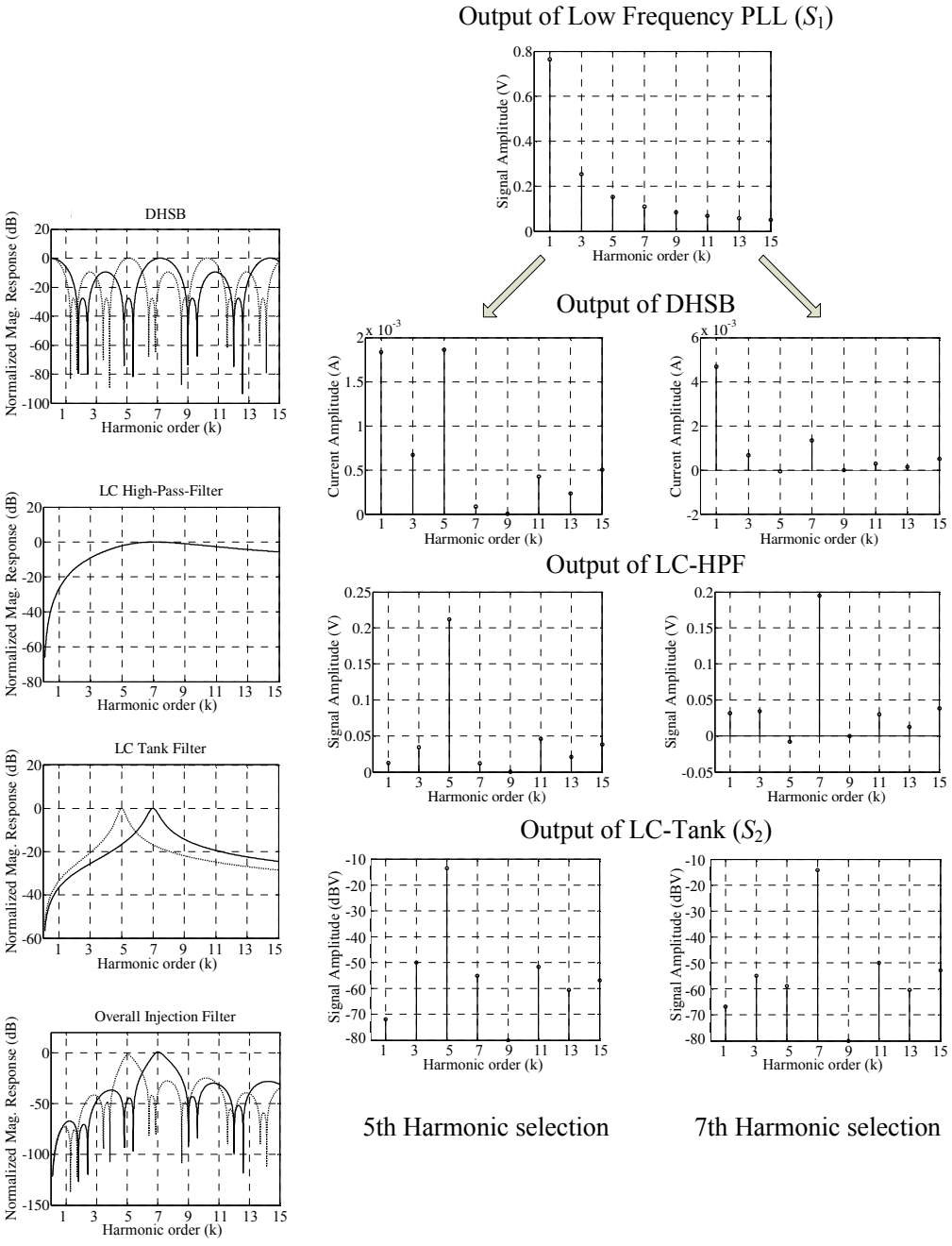
causes the amplitude of the fundamental tone to be nearly equal to the 5th harmonic in the first mode and 10dB larger than the 7th harmonic in the second mode. Although the fundamental tone is roughly 5GHz or 7GHz away from the required tone, it modulates the DC level of the injected higher-order-harmonic signal. As a result the DC operating point of the injection circuit changed periodically and hence the oscillator's output frequency as well. Thus, an LC high pass filter (HPF) was added to filter out this tone. This LC-HPF filter was formed using the bias-T circuit (L_1=2.5nH and C_1=0.5pF shown in Fig. 7) required to bias the next stage (the injection circuit) and it provided nearly 28dB of attenuation to the fundamental tone. The inductor was implemented using the bond wire of the package to save chip. The load resistor of the adder reduces the quality factor of the filter ($Q \approx 0.4$) and hence allows similar pass band characteristics to the 5th and 7th harmonics. The synthesized harmonic is then injected into the *N*-phase IL-VCO. In our design, an LC-tank VCO (described in the next section) is employed to provide low-phase-noise over the operating frequency range. Moreover, the LC tank provides additional filtering to the adjacent harmonics and hence helps relax the DHSB requirements. In this design the adjacent tones are roughly 1GHz away and their suppression is arbitrarily chosen to be around 40dBc at the output of the oscillator. Using this filtering requirement, and taking into account the filtering of the LC-HPF (formed at the load of the adder circuit) and the LC tank of the VCO, the required amount of filtering from the DHSB are calculated through Matlab® simulations and consequently the corresponding time shifts are determined. At the output of the LC-tank of the VCO all adjacent harmonics were suppressed by around 38 dBc. More attenuation can be

achieved by using more degrees of freedom in the DHSB (i.e. more signals or more time shifts) but at the expense of more complexity and power consumption. Fig. 10 shows the transistor-level simulation results of the output of the DHSB before and after the LC-HPF. Fig. 10 (c) and (d) show that the enforced 5th and 7th harmonics are higher than the neighboring harmonics by at least 18dB and 10dB, respectively.



(a)

Fig. 9 (a) Block diagram and (b) output signal spectra of the DHSB and subsequent filtering stages for the first multiplication step



(b)

Fig. 9 Continued

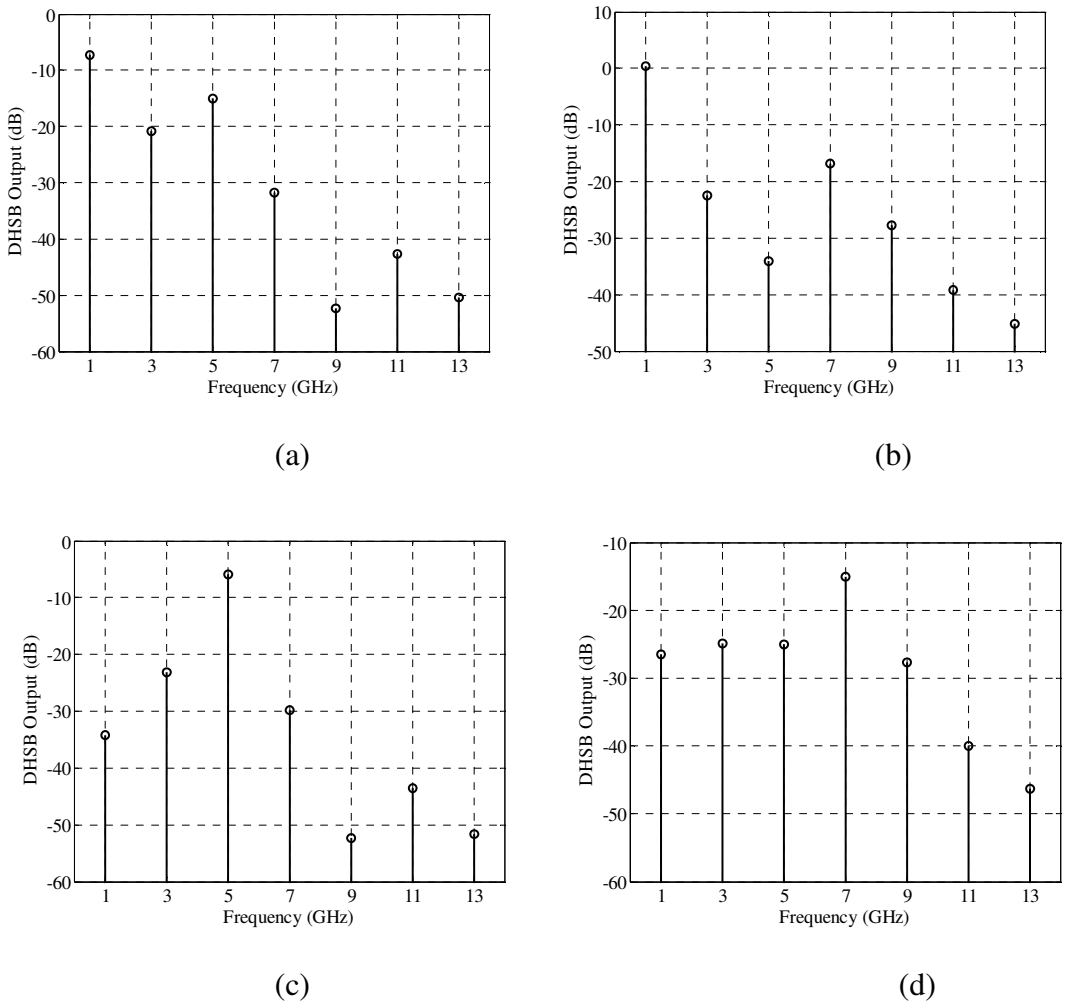


Fig. 10 Simulation results of the output signal spectra from the DHSB before the LC-HPF for (a) 5th harmonic, (b) 7th harmonic and after the LC-HPF for (c) 5th harmonic and (d) 7th harmonic

2.3.1.1 Mismatch Analysis of the DHSB

Mismatches in the delay line can reduce the achieved harmonic suppression. To quantify the sensitivity of the DHSB to mismatches in the different delay cells we perform the following mismatch analysis. The phase shift at the output of one delay cell depends on the mismatches in the phase shifts of all the preceding delay cells. As

mentioned before, a two-path 18-stage delay line is employed. Hence, we denote the phase of the signals to be added as ϕ_{x_y}, where *x* corresponds to the delay-line number (1 or 2,) and *y* corresponds to delay-stage number in the line (0-18). ϕ_{x_y} is given as,

$$\phi_{x\_y} = (x-1)\pi + y\frac{\pi}{18} \tag{2.11}$$

According to the designed prototype, and recalling Fig. 8 for the employed phase shift numbers, the phases of the added signals are [ϕ_{1_0}, ϕ_{1_7}, ϕ_{1_14}, ϕ_{2_4}, ϕ_{2_11},ϕ_{2_18}] when enforcing the fifth harmonic and [ϕ_{1_0}, ϕ_{1_5}, ϕ_{1_10}, ϕ_{2_8}, ϕ_{2_13},ϕ_{2_18}] when enforcing the seventh harmonic. Recalling equation (6), the transfer function of the DHSB for the *k*th harmonic is given by:

$$H(k,\phi_i) = \sum_{i=1}^{M} e^{-jk\phi_i} \tag{2.12}$$

In our design, *M=6* and ϕ_i should be substituted by the ϕ_{x_y} array. Assuming the phase mismatch error introduced by each delay cell is $\delta\phi$, the phase error in ϕ_{x_y} is given by,

$$\Delta\phi_{x\_y} = \sum_{i=1}^{y} \delta\phi_i \tag{2.13}$$

Thus, we define the rejection of the DHSB for the *n*th harmonic as the amplitude of the *n*th harmonic relative to the *k*th harmonic (to be enforced). We denote it as R_{nk} and is given by,

$$R_{nk} = \frac{\sum_{M} \exp^{-jn(\phi_{x\_y} + \sum_{i=1}^{y}\delta\phi_i)}}{\sum_{M} \exp^{-jk(\phi_{x\_y} + \sum_{i=1}^{y}\delta\phi_i)}} \tag{2.14}$$

Random phase mismatches $\delta\phi_i$ are introduced in the above equation and R_{nk} is calculated. Fig. 11 shows the rejection of the DHSB for the different harmonics versus the standard deviation of the phase mismatch error $\delta\phi$. The rejection of the fundamental tone and the third harmonic does not nearly change while the rejection of the 9th harmonic changes rapidly but stays less than -20dB for a 10% mismatch. These results conform to the normalized magnitude response of the DHSB shown in Fig. 9.

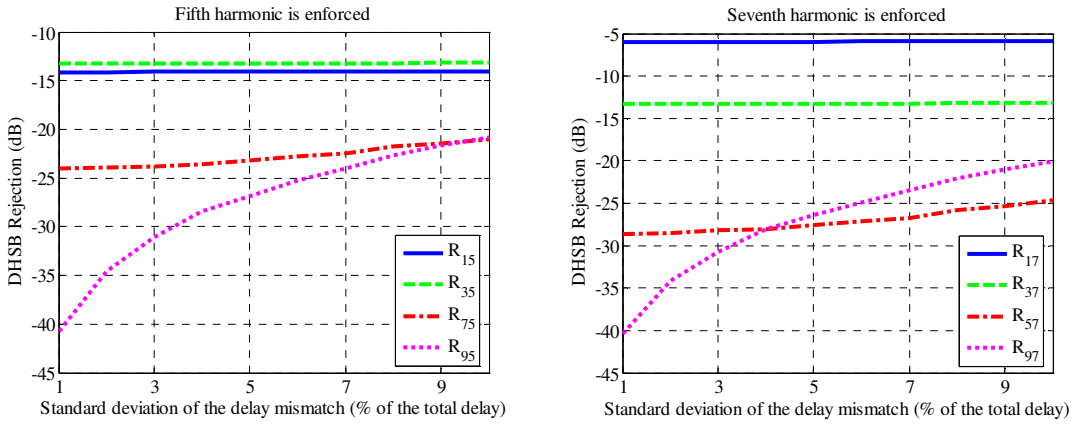


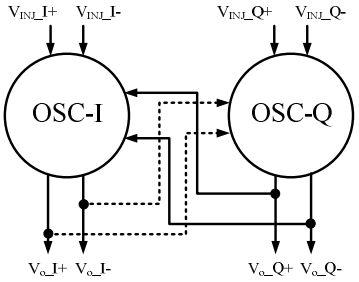
Fig. 11 Simulation results of the rejection of the DHSB versus delay mismatches in the delay elements

The slope of the curve of this response at the fundamental and third harmonic is small and hence their suppression is resistant to mismatches, except at the 9th harmonic which has a high slope and thus is more vulnerable to mismatches. It should be noted that in a complete system the DHSB would be controlled through its power supply by the DLL loop. So, any uniform process and temperature variations will be compensated by the DLL Loop.

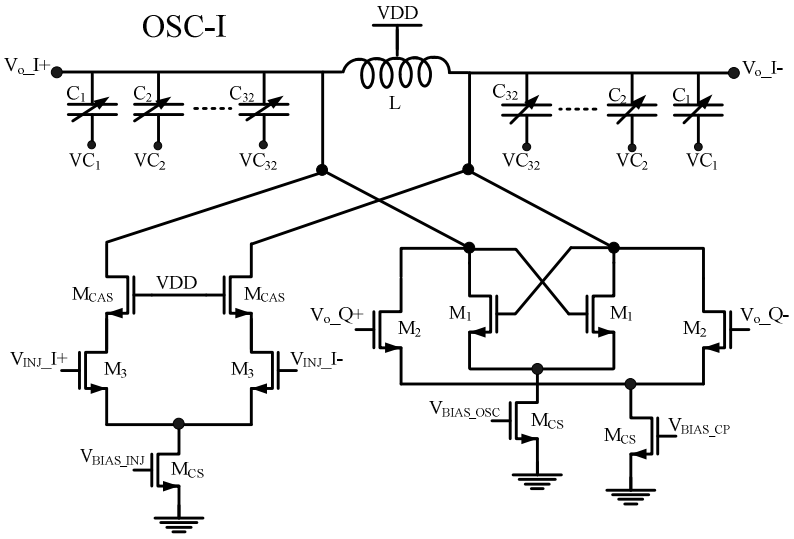
2.3.2 *N*-Phase IL-VCO

Cascading oscillators in a ring structure, with each stage feeding a scaled copy of its output into the successive stage, leads to a ring-oscillator-like structure but with an oscillator as the delay element. This connection locks the oscillators to a common frequency. However, the phases of the output voltage of each oscillator will depend on the number of oscillators (N) in the loop. The phase difference will be $180^o/N$ with an odd number of inversions around the loop or 0^o with an even number of inversions [28]. These different phases enable the *N*-Push operation [21] required for the second frequency multiplication step.

In this work, we use two "stages" yielding the classic cross-coupled differential I-Q LC-VCO [29] shown in Fig. 12. This structure provides 90^o phase difference between the two oscillator outputs. Since each oscillator is fully differential, then phases of 0^o, 90^o, 180^o and 270^o are available at the output. Tapping any of these outputs provides the fundamental tone; while adding the anti-phase signals provides the second harmonic but cancels the fundamental tone; and adding all four signals preserves the fourth harmonic but cancels the fundamental tone and the second harmonic. Therefore, selective addition of these four signals can implement frequency multiplication by 1, 2 or 4 which are needed to implement the second frequency multiplication step.



(a)



(b)

Fig. 12 (a) Block diagram of the 2-stage IL-VCO (b) Circuit diagram for the I-path oscillator

The oscillator core uses an NMOS cross-coupled transistor pair to enable high frequency oscillation. The tank circuit consists of a differential inductor, with its center tab tied to VDD to allow for a high output swing. The inductor value ranges from 0.83-0.9nH at 5-10GHz, respectively. A bank of 7 binary weighted switched varactors (with LSB capacitance of 50fF) is used to tune the tank from 5-10GHz. The varactors are

binary weighted with the last two most significant bits having the same weight. The number of bits is determined such that the locking range of the IL-VCO is larger than the tuning provided by the least significant bit of the varactor bank and hence continuous tuning can be achieved. As we add more capacitors to decrease the frequency the current is increased to maintain the output swing. Fig. 13 shows the VCO tuning curve versus the employed digital codes. A differential pair with an independent current source couples the output of each oscillator into its counterpart. Another differential pair with cascode transistors couples the injected harmonic created by the DHSB into the oscillator. The cascode transistors shield the injection differential pair from the high voltage swing at the oscillator output node. This maintains a constant V_{ds} across the differential pair, or equivalently a constant transconductance g_m, and hence a constant injection strength.

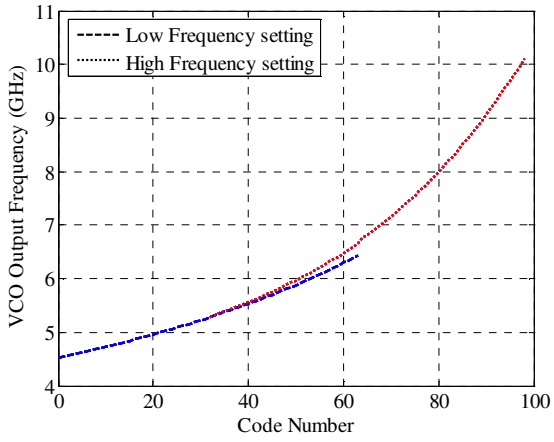


Fig. 13 The IL- VCO free running output frequency versus the tuning digital code

2.3.3 Variable *N*-Push Frequency Multiplier

The I-Q IL-VCO provides 4 different phases. When these phases are added in different combinations, different multiplication factors can be achieved by selecting the 1st, 2nd or 4th harmonics. Since the LC tank filters out higher order harmonics, we need to generate the even harmonics required to implement the second frequency multiplication step. Thus, a common-source amplifier biased in a class-B mode is employed as a frequency multiplier. This common-source amplifier clips the spectrally-pure sine-wave produced by the oscillator producing the harmonics of this signal Fig. 14 displays the variable *N*-Push frequency-multiplier circuit. The four output phases of the oscillator are AC-coupled to four common-source driver transistors. Selection transistors are used to select which inputs are operative and to provide isolation between the output and the input. The currents of the drivers are added at the output node using a resistive load. Shunt peaking (using the on-chip inductor L_2) is employed to extend the bandwidth for the summation of the signals.

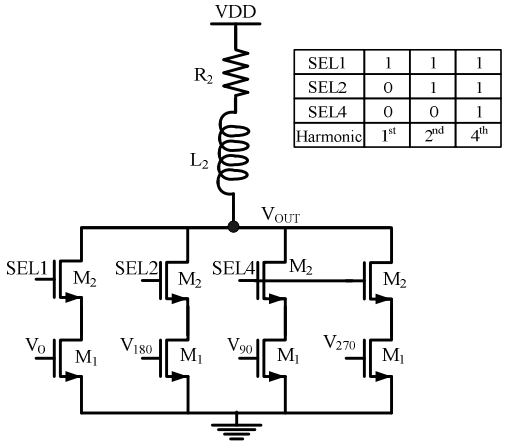


Fig. 14 Circuit diagram of the variable *N*-Push frequency multiplier

Fig. 15 shows the drain current of one branch of the variable *N*-Push frequency multiplier. This current is the drain current of a common source amplifier biased in class-B mode which can be approximated as a clipped sine-wave. In practice two types of clipping occur. The first is clipping all or part of the negative half cycle of the input sine-wave by changing the bias point of the driver transistor and is defined by the conduction angle γ. The second is clipping of the peak of the sine-wave due to the limited voltage headroom driving the amplifier into triode region and is defined by the clipping angle β. The current in the driver transistor can, thus, be written in terms of the conduction and clipping angles as,

$$I(\omega t) = \begin{cases} 0 & \pi > |\omega t| > \gamma/2 \\ I_o(\cos(\omega t) - \cos(\gamma/2)) & \gamma/2 > |\omega t| > \beta/2 \\ I_o(\cos(\beta/2) - \cos(\gamma/2)) & |\omega t| < \beta/2 \end{cases} \tag{2.15}$$

The Fourier series coefficients of the drain current waveform are given as [30],

$$\begin{aligned} I_n = & -\frac{2I_o\cos(\gamma/2)}{n\pi}[\sin(n\gamma/2) - \sin(n\beta/2)] \\ & + \frac{I_o}{(n-1)\pi}[\sin((n-1)\gamma/2) - \sin((n-1)\beta/2)] \\ & + \frac{I_o}{(n+1)\pi}[\sin((n+1)\gamma/2) - \sin((n+1)\beta/2)] \\ & + \frac{2I_o(\cos(\beta/2) - \cos(\gamma/2))}{n\pi}\sin(n\beta/2) \end{aligned} \tag{2.16}$$

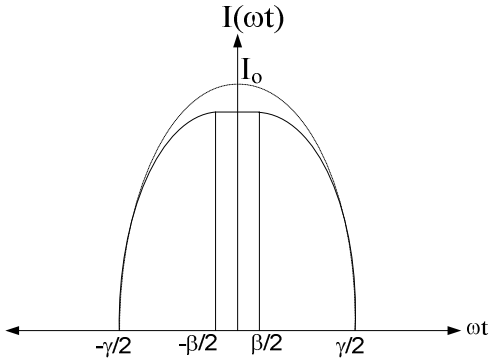
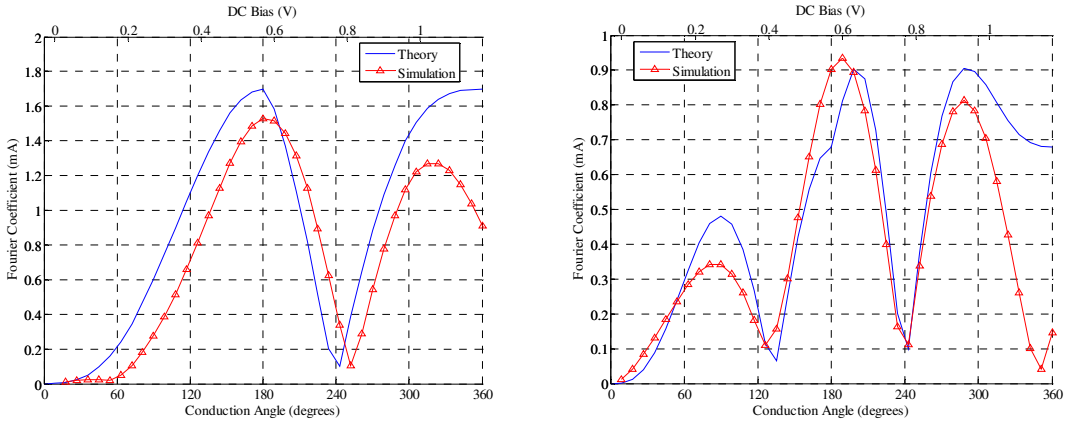


Fig. 15 Output drain current of the common-source amplifier of the frequency multiplier showing double clipping

It should be noted that changing the conduction angle also changes the clipping angle as the two sources of clipping (threshold voltage of the driver transistor and the available headroom) are fixed. Hence, the term $(\cos(\beta/2)-\cos(\gamma/2))$ is constant and from simulations is found to be nearly unity. To determine the bias point of the amplifier which provides the highest output amplitude, the amplitude of the Fourier series coefficients for the second and fourth harmonics are plotted versus different conduction angles using equation(2.16) . These amplitudes are also plotted versus different gate bias voltages using circuit simulations and Fig. 16 shows both plots. Simulation results are plotted for an output frequency of 8GHz for both harmonics (i.e. the fundamental tone is 4GHz and 2GHz for the cases of 2nd and 4th harmonics, respectively) to provide equal gain response by the load. A conduction angle of nearly 190^{o} provides the highest amplitude for the second and fourth harmonics simultaneously. This corresponds to a DC bias of 0.6V for a 1.2V supply.



(a) (b)

Fig. 16 Fourier series coefficients of the (a) 2nd and (b) 4th harmonics of the frequency multiplier output for different conduction angles

2.3.4 Output Amplifier

The final stage is an amplifier stage, shown in Fig. 17, used to boost the signal amplitude and drive the off-chip 50Ω loading of the testing equipment. Three common-source amplifier stages are used which combine shunt and series inductive peaking to extend the bandwidth. Three stages are employed to reduce the gain requirement from each stage allowing wider bandwidth. Fig. 18 shows the simulated voltage conversion gain of the frequency multiplier as well as the voltage gain of the output amplifier across the frequency range. The amplifier gain drops beyond 32 GHz which is the limiting factor of the achieved bandwidth.

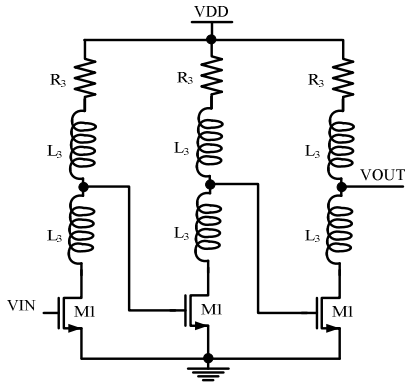


Fig. 17 Output amplifier stages

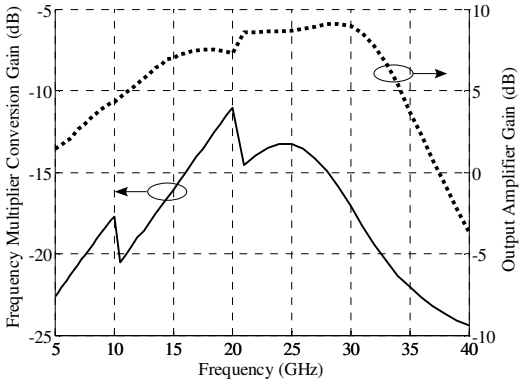


Fig. 18 Simulation results of the voltage conversion gain of the Variable *N*-Push frequency multiplier and the voltage gain of the output amplifier

2.4 Phase Noise Analysis

The proposed architecture is a cascade of circuits through which the input signal generated by the low frequency PLL propagates. The phase noise of this signal may degrade as it passes through each block depending on the added noise of this block. The phase noise $\mathfrak{L}_B(f_m)$ of a certain block at an offset frequency f_m is defined as its output noise normalized to the output carrier amplitude. In general, when an input signal with

phase noise $\mathfrak{L}_i(f_m)$ passes through a block with a phase noise $\mathfrak{L}_B(f_m)$, the output phase noise is given as the addition of both quantities[31]:

$$\mathfrak{L}_o(f_m) = \mathfrak{L}_i(f_m) + \mathfrak{L}_B(f_m) \tag{2.17}$$

Equation (2.17) shows that if the block has a phase noise equal to the input phase noise, the output phase noise will degrade by 3dB. For a frequency multiplier circuit which multiplies the input frequency by a factor *M*, (2.17) becomes,

$$\mathfrak{L}_o(f_m) = M^2\mathfrak{L}_i(f_m) + \mathfrak{L}_B\big|_M(f_m) \tag{2.18}$$

Hence, the output phase noise is equal to the input phase noise multiplied by M^2 (to account for the frequency multiplication) added to the frequency multiplier's phase noise calculated for the *M*th harmonic ($\mathfrak{L}_B\big|_M(f_m)$). The quantity $\mathfrak{L}_B\big|_M(f_m)$ takes into account the conversion gain of this block. Recalling the system architecture shown in Fig. 19 the main blocks in the system are the DHSB, the IL-VCO and the variable *N*-Push frequency-multiplier (VNFM) combined with the output amplifier. The DHSB and the variable *N*-Push frequency-multiplier are frequency multiplication circuits and hence (2.18) should be used to calculate the phase noise of their output signals.

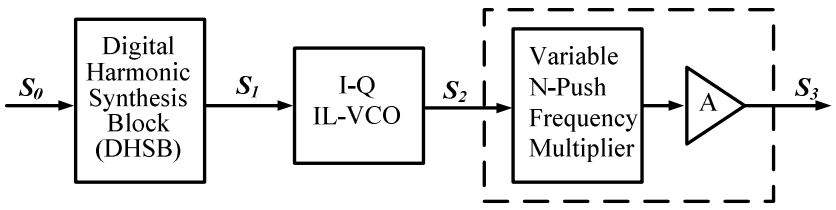


Fig. 19 Proposed system architecture

The phase noise of the output signal of an injection locked oscillator is similar to a first order PLL [32] . It follows the phase noise of the injected signal for frequency offsets less than the locking range ω_L (low pass filtering of the injection signal) and then follows that of the oscillator for frequency offsets higher than the locking range (high pass filtering of the oscillator noise) [33]. Hence, the phase noise of the IL-VCO output is a function of the injection signal and oscillator's phase noise as well as the locking range. It can be given as follows [34],

$$\mathfrak{L}_{vco\_out}(f_m) = \mathfrak{L}_{inj}(f_m)\left|NTF_{in}\right|^2 + \mathfrak{L}_{vco}(f_m)\left|NTF_{vco}\right|^2 \tag{2.19}$$

NTF_{in} and NTF_{vco} are the low pass and high pass noise transfer functions of the injection signal and the oscillator noises, respectively, and are given by,

$$NTF_{in} = \frac{1}{1 + j(\omega/\omega_L)} \tag{2.20}$$

$$NTF_{vco} = \frac{j(\omega/\omega_L)}{1 + j(\omega/\omega_L)} \tag{2.21}$$

To follow the phase noise through this cascade of blocks, we simulated the phase noise of these blocks in Spectre® for an input clock of 2GHz. The input clock is obtained from a lab source in measurements and hence the phase noise of this source $\mathfrak{L}_{S0}(f_m)$ is characterized and used in this analysis. We then use equations (2.17), (2.18) and (2.19) to find the intermediate and final outputs. This analysis gives an estimate of the output phase noise expected from such system and provides insights of which blocks' noise is more crucial. Fig. 20 shows the simulated phase noise of the DHSB, VCO and the VNFM combined with the output amplifier. The DHSB has two curves for the 5th and

7th Harmonic while the VNFM has 3 curves. Since the DHSB employs a delay line with minimum length transistors and small widths to minimize loading effects and provide sharp square waves, the flicker noise corner frequency is relatively high at nearly 1MHz offset. Using larger transistors can reduce the flicker and thermal noise of the DHSB but will reduce the maximum frequency it can process. The input clock is divided-by-two on chip to provide I-Q signals. Thus, the output of the DHSB S_1 has a phase noise $\mathfrak{L}_{S1}(f_m)$ given by,

$$\mathfrak{L}_{S1}(f_m) = (M/2)^2 \mathfrak{L}_{S0}(f_m) + \mathfrak{L}_{DHSB}\big|_M (f_m) \tag{2.22}$$

Next applying (2.19) and substituting $\mathfrak{L}_{S1}(f_m)$ for $\mathfrak{L}_{inj}(f_m)$ we can find the phase noise of the IL-VCO output $\mathfrak{L}_{S2}(f_m)$. Finally, the phase noise of the output $\mathfrak{L}_{S3}(f_m)$ can be obtained by,

$$\mathfrak{L}_{S3}(f_m) = N^2 \mathfrak{L}_{S2}(f_m) + \mathfrak{L}_{VNFM-AMP}\big|_N (f_m) \tag{2.23}$$

Fig. 21 depicts the phase noise of the signals S_0-S_3 for the different multiplication factors in the VNFM while the DHSB is set to select the 7th Harmonic. It is noticed that the phase noise of the VCO output follows that of the injected signal for frequencies up to the locking range (35MHz). The locking range doubles and quadruples for the case of N=2 and N=4. The phase noise of the final output for these different values of N is presented in Fig. 22. We can see that for N=4 the locking range is the largest (140MHz) and hence the curve stays flat up to nearly 100MHz. The curves have 6dB difference in phase noise due to frequency doubling. Fig. 23 shows the phase noise of the signals S_1-S_3 overlaid with the phase noise of the DHSB and the VNFM for the specific case of

M=7 and *N*=4. We can observe that the injected signal to the IL-VCO is dominated by the multiplied clock frequency at offsets less than 1MHz while the DHSB phase noise dominates at higher frequency offsets and hence limits the phase noise performance up to the locking range. Also, we notice that the output phase noise curve starts decreasing at frequency offsets larger than 100MHz (to follow the VCO phase noise) and then flattens again near 1GHz due to the dominance of the phase noise of the VNFM at this offset. From this analysis we conclude that the phase noises of the input clock as well as the DHSB are crucial in determining the overall phase noise at frequency offsets below the locking range. On the other hand for frequency offsets higher than the locking range the VCO and the VNFM phase noises determine the output phase noise.

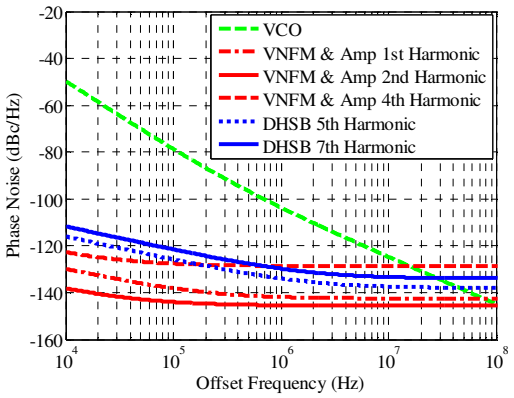


Fig. 20 Phase noise of the main blocks of the proposed system

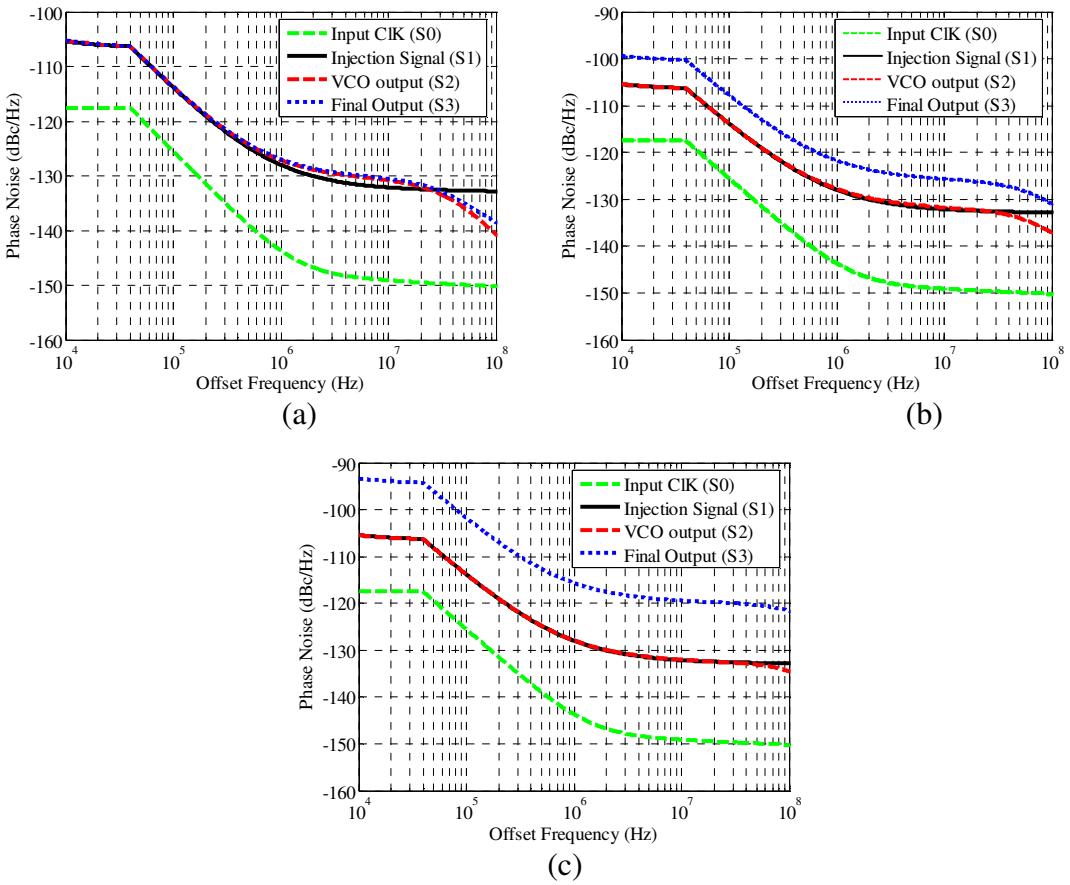


Fig. 21 Phase noise of the signals S_0-S_3 for M=7 in the DHSB and (a) fundamental tone selected, (b) 2nd harmonic selected, and (c) 4th harmonic selected in the VNFM

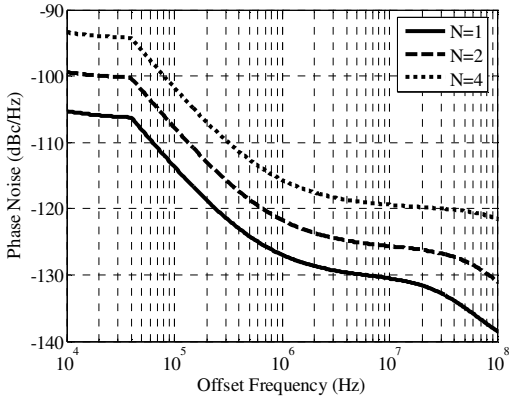


Fig. 22 Comparison of the phase noise of the final output for different selections of N in the VNFM

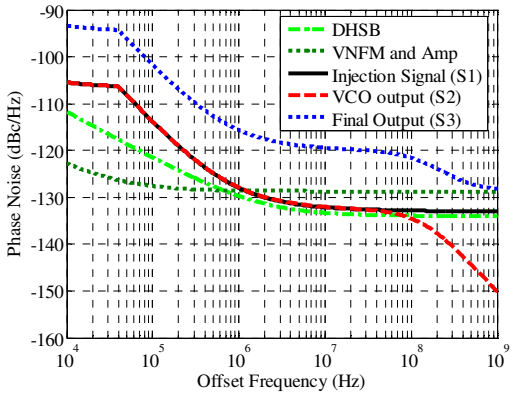


Fig. 23 Phase noise of the signals S_1-S_3 overlaid with the phase noise of the DHSB and the VNFM for the case of M=7 and N=4

2.5 Measurement Results

The proposed circuits are implemented in a 90nm RF-CMOS process with 8 metal layers. The chip micrograph is shown in Fig. 24 and occupies an active area of 0.6 mm^2. In our test setup the input signal was supplied form the Agilent E8267 vector signal generator. The input signal to each delay line is designed to be a square-wave with a frequency range of 1-1.43 GHz. However, since we need quadrature phases which the signal generator cannot provide, the input signal frequency is doubled and an on-chip divide-by-two circuit is added to provide the I and Q signals. The divide-by-two circuit is preceded by a chain of buffers to convert the input sine-wave into a square-wave. An on-chip phase detector outputs a signal proportional to the phase difference between the first and last square wave signals of the delay line. The supply of the delay line is then tuned manually to minimize this difference. On-chip 50Ω resistors at the input are added to provide wideband matching for the input signal. All pads of the chip are bonded

except for the output high frequency signal pads. The chip was mounted on a PCB placed on the probe station for probing with DC biases provided from another PCB. The output was tested using on-wafer probing and was measured using the Agilent E4446, 44GHz, power spectrum analyzer.

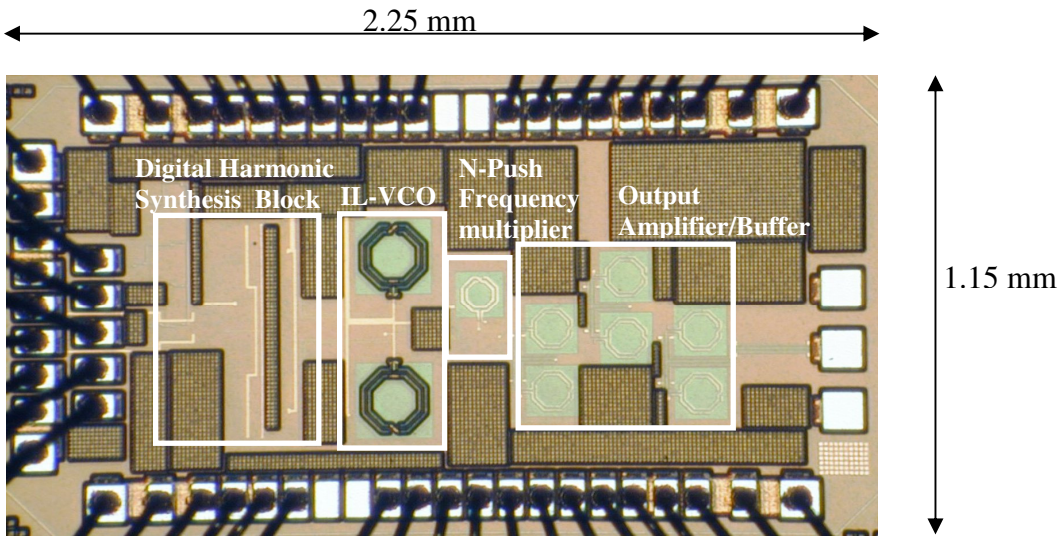


Fig. 24 Micrograph of the test chip showing the building blocks

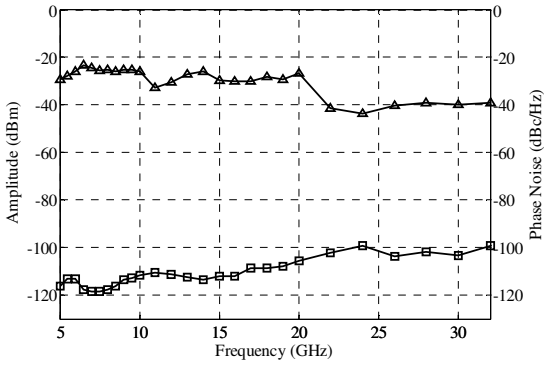


Fig. 25 Amplitude and phase noise (at 1MHz offset) of the output over the output frequency range

Fig. 25 shows the measured output amplitudes of the desired harmonic. The output covers a tuning bandwidth of 27 GHz from 5 to 32 GHz, which corresponds to a tuning range of 146%. Fig. 26 plots the measured output spectrum of the lowest (5GHz) and highest (32GHz) frequencies of operation. The output amplitude ranges from -24 to -42dBm. The low output amplitude at the high frequency end is observed due to several factors. The measurement setup introduces losses of 7-10 dB in the cables and bias-T. In addition, the VNFM and the output amplifier have a single-ended structure. Hence, the inductance introduced in the power supply paths (due to the bond wires) reduced their gain due to source degeneration. Including the model of the bond wires in the simulation reduced their gain by around 10dB for the high end of the frequency range.

Fig. 27 shows the degradation in the gain of the VNFM and the output amplifier due to including the bond wire model. Finally, layout mismatches are more pronounced at higher frequencies and hence reduce the amplitude of the synthesized harmonic.

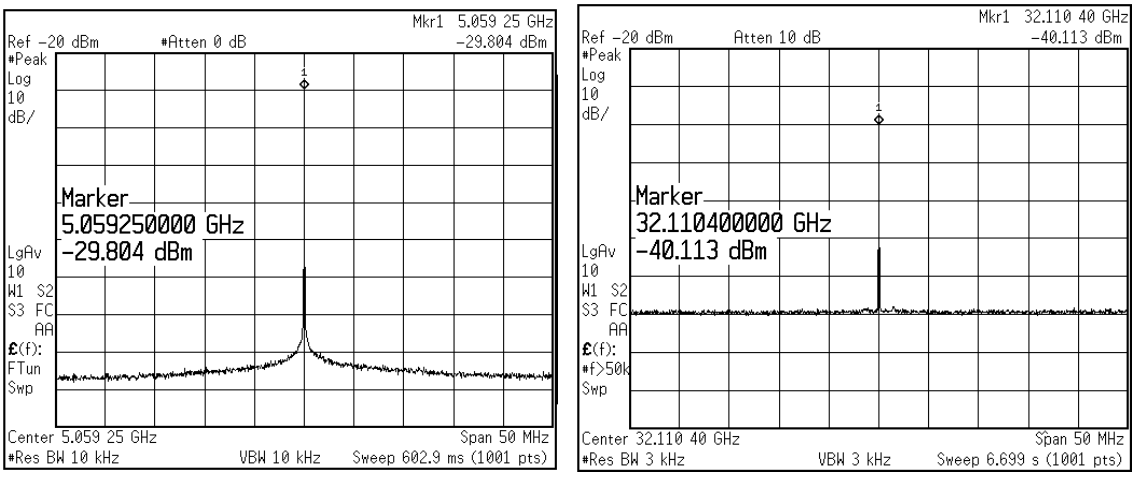


Fig. 26 Output spectrum at 5GHz and 32 GHz

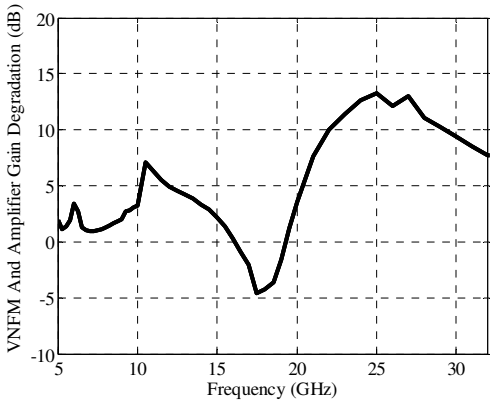


Fig. 27 Simulated voltage gain degradation of the VNFM and the output amplifier due to bond wires' inductance

Fig. 25 also depicts the phase noise of the output signal at 1 MHz offset ranging from -99 to -116 dBc/Hz. The phase noise plots of the output at 6.5GHz, 13GHz and 26GHz are shown in Fig. 28. The measured phase noise at frequencies less than the locking range follows that of the DHSB. This is clear from the small slope of the phase noise curve starting at very low frequency offsets as seen in Fig. 28. Hence, to quantify the in-band noise degradation of the input clock, we consider the phase noise at a frequency offset of 40KHz. In Fig. 29 we plot the measured in-band phase noise of the output signal and the input clock. We also plot the phase noise of the clock after adding the 20log10(M/2) factor due to divide-by-two circuit followed by the DHSB frequency multiplication by M. It is observed that the degradation is within 4dB for the frequencies from 6.5GHz-8.5GHz and gets worse outside this range. Outside this range, we cannot see the flat part of the phase noise curve of the input clock (for offsets less than 40 KHz as was shown in Fig. 21), but rather it takes a shape that resembles the phase noise of the

DHSB. Hence we attribute this degradation to higher noise coming from the DHSB which dominates over the input clock.

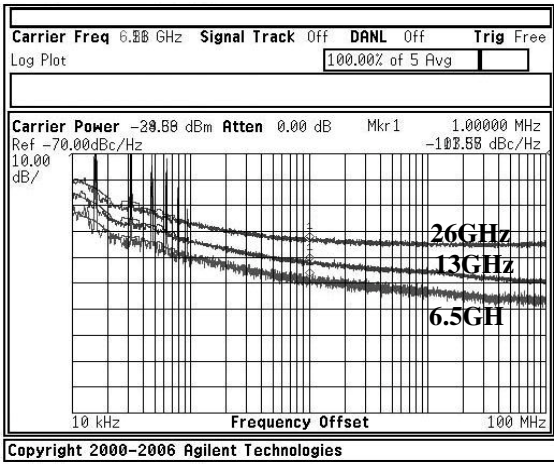


Fig. 28 Phase noise plots of the output signal at 6.5, 13 and 26 GHz

It is noticed from Fig. 28 that the phase noise flattens back again at frequency offsets above the locking range. This is because the phase noise of the VNFM and the output amplifier is higher than the VCO's. The phase noise is degraded due to the lower output amplitude of the VNFM and the output amplifier because of their single-ended structure. This drop in amplitude can be overcome by increasing the amplitude of the voltage swing in the VCO by increasing its bias current. However, this will reduce the achieved locking range. The phase noise at frequency offsets below the locking range increases by nearly 6 dB from one curve to the next, as expected, due to frequency multiplication. Spurs at low frequency offsets (less than 10KHz) are due to power supply noise.

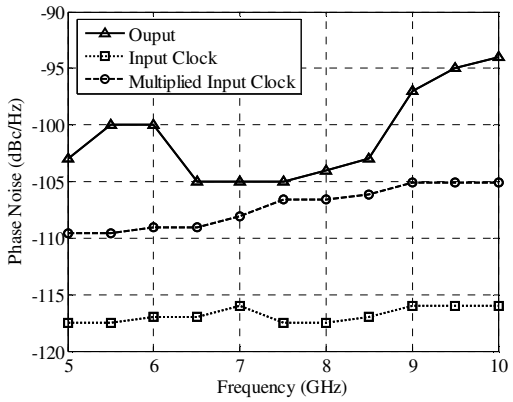


Fig. 29 Phase noise (at 40KHz offset frequency) of the input clock, the multiplied input clock and the output signal

The overall injection filter shown in Fig. 9(b) and formed by combining the effects of the DHSB, LC-HPF and the VCO tank suppresses the harmonics of the input frequency (f_o) and hence reduces the spurs in the output spectrum of the VCO. Fig. 30 shows the measured output spectrum for a 7.46GHz signal. Spurs appearing at nf_o offset from the carrier are below -39dBc except for the second harmonic which is higher due to coupling on the testing PCB board (verified by turning off the circuit and still observing an output tone at this frequency). On average, the injected harmonics are around -36 dBc which is close to the designed value of -38dBc. The locking behavior to the 7^{th} harmonic is apparent in the figure with 6 harmonics below the oscillator's output tone.

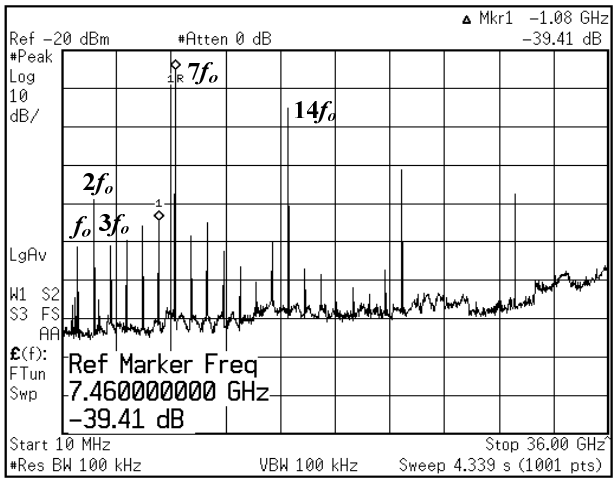
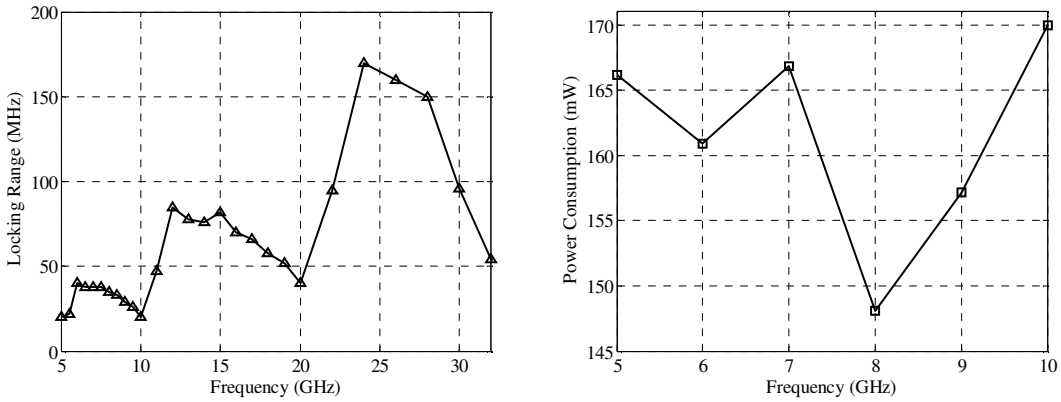


Fig. 30 Output spectrum for the case of 7.46GHz output showing the harmonic cancellation of the neighboring harmonics from the DHSB

Fig. 31(a) shows the measured locking range of the oscillator over the operating frequency range. It should be noted that the locking range decreases with frequency because the inductor quality factor increases with frequency. Also, the locking range doubles for the second harmonic and quadruples for the fourth harmonic due to frequency multiplication as shown in Fig. 31(a).

Fig. 31(b) depicts the power consumption of the proposed system at the different frequency points which ranges from 148 to 170mW. After 7 GHz we switch from the 5th harmonic selection to the 7th in the DHSB and use the lowest input frequency. Hence, power consumption drops in the delay line of the DHSB reducing the total consumed power as shown in Fig. 31(b). The power consumption break down of the individual blocks is presented in Fig. 32. The main power consumers are the delay line, I-Q VCO and the adder.



(a) (b)

Fig. 31 (a) Locking range values for different frequencies (b) Power consumption of the circuit over the operating frequency range

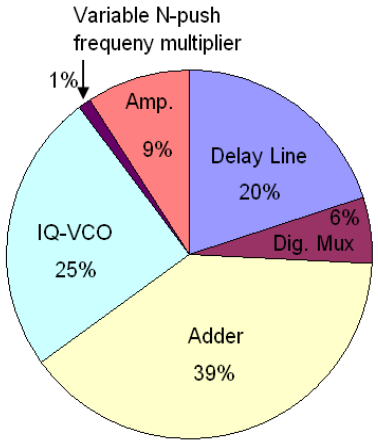


Fig. 32 Break down of the power consumption for different blocks in the system

Finally, Table 3 compares the performance of this system to recently published work. This work achieves a 146% tuning range which is equivalent to continuous tuning over 2.8 octaves. Although, the power consumption is high, yet normalizing this power to the tuning range shows that this work has competitive power consumption per octave.

Table 3 Comparison of the performance of the proposed system with previously published work

	This Work	[6]	[21]	[35]	[36]	[20]	[37]
Frequency Range (GHz)	5-32	17.5- 20.9 / 35-41.8	0.125-26	56-65	7.6-8.7	0.64 - 4.6 / 5.1 - 6.9 / 10.2 - 13.8 / 20.4 - 27.6	3-10
Tuning Range (%)	146	17.4 / 17.4	198	14.8	13	112.5 / 30 / 30 / 30	107.7
Tuning Range (Octave)	2.8	0.6 / 0.6	5.8 (2.8 above 4GHz)	0.58	0.57	2.9 / 0.67 / 0.67 / 0.67	1.834
Architecture	Multi-order Multi-step Harmonic Synthesis	Integer-N PLL with Push-Push	PLL followed by mixers and dividers	Sub-harmonic IL	Sub-harmonic IL	PLL with high speed dividers	PLL with SSB mixing
Phase noise @ 1MHz (dBc/Hz)	-112 @ 16GHz	-100 @ 20.8GHz	-110.7 @ 12GHz	-112 @ 60.6GHz	-112 @ 8.7GHz	-108 @ 24GHz	-98 @ 8.4GHz
Power consumption (mW)	148-170	80	1000	23.8	36	680	117
Area (mm^2)	0.600	3.040	2.56 (estimated)	0.800	0.074	4.800	5.500
Technology	90nm	65nm	0.18µm SiGe BiCMOS	90nm	90nm	0.25µm SiGe BiCMOS	180nm
Power/Octave (mW/Octave)	57-65*	66.67	172.4	178.96**	63.16	138.5	63.8

* 20 mW are added to the power consumption to account for the input low frequency PLL [38].
** 80 mW are added to the power consumption to account for the 20.2GHz input frequency [6].

For a fair comparison, an additional 12mW (twice the power in [38] which used a 0.65V supply) are added to account for the power of the low frequency PLL not included in this design. The same was done for the results of [35].

The proposed system achieves a very wide tuning range as well as state-of-the-art power consumption per octave of continuous tuning range. It also achieves 0.23*psec* of rms jitter over the band from 10KHz to 100MHz at 16GHz. This corresponds to a Figure of Merit (FOM) of synthesizers of -230dB. This FOM is defined in [39] as,

$$FOM = 10\log\left[(\frac{\sigma_t}{1s})^2 \frac{P_{dc}}{1mW}\right] \tag{2.24}$$

2.6 Conclusion

A wideband mm-wave frequency synthesizer architecture is presented which uses multi-step multi-factor frequency multiplication. This architecture avoids the problems associated with injection-locked dividers. Mismatches could arise between the input PLL and the IL-VCO; however, oscillators can be aligned easily (compared to injection-locked dividers) using frequency measurement techniques and digital control from the DSP [40]. The DHSB allows high amplitude injection to the VCO while it reduces the spurs in the VCO output. Measurement results demonstrated that a very wide tuning range of 5 to 32 GHz can be achieved, which is costly to implement using conventional techniques. Moreover the power consumption per octave resembles that of state-of-the art reports.

CHAPTER III

LOW PHASE NOISE WIDE TUNING RANGE N-PUSH CYCLIC-COUPLED RING OSCILLATORS*

3.1 Introduction

Oscillators are essential components in numerous circuits such as frequency synthesizers for wireless and wireline transceivers, clock generators for microprocessors and clock and data recovery systems. The high demand on data and bandwidth requires that these oscillators work at higher frequencies to process more data and provide more bandwidth. Higher data rates also require that oscillators have lower phase noise. In addition, oscillators are required to provide multi-phase clocks; for example in-phase and quadrature-phase clocks in fully integrated image reject receivers [41] or multi-phase clocks employed in high speed sampling in time-interleaved applications [42].

Coupled oscillators have been used historically to provide multi-phase outputs for power combining and beam scanning applications [43]. They have the advantage of reduced phase noise: *M* coupled oscillators have *M* times less phase noise than a single oscillator (given the coupling network is reciprocal) [44]. However, for LC-tank coupled oscillators, the phase noise improvement is not 1/*M* because phase noise of the individual oscillators degrades due to de-tuning of the oscillator output frequency from the tank's resonance frequency [45][46]. Moreover, the area penalty of using on-chip

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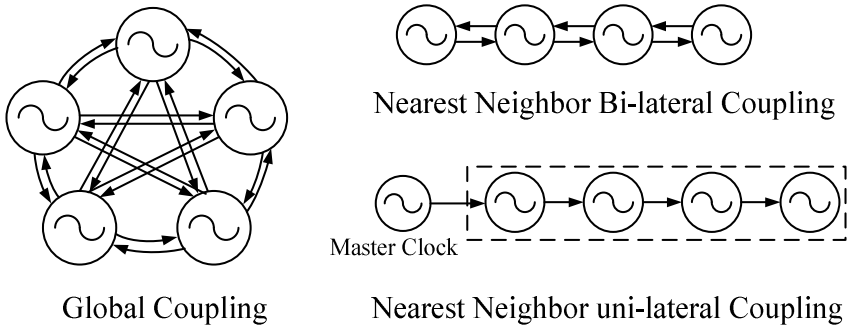
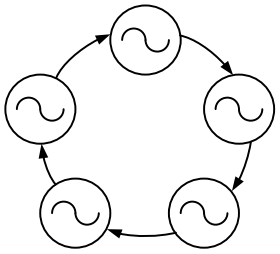
* Reprinted, with permission, Mohammed M. Abdul-Latif, Edgar Sánchez-Sinencio, **"**A 3.16 – 12.8 GHz Low Phase Noise N-Push/M-Push Cyclic Coupled Ring Oscillator", in *IEEE RFIC Symp. Dig.*, June 2011, pp. 405-408. © 2011 IEEE.

inductors limits the number of achievable phases and the narrowband characteristics of the LC-tanks limits wideband frequency operation. On the other hand, ring oscillators inherently provide multi-phase clocks as well as wide tuning ranges. In addition, they are compatible with the low cost digital CMOS processes and scale with technology promising higher operating frequencies for newer deep submicron technologies. However, their phase noise performance is inferior to LC oscillators.



(a)



Nearest Neighbor uni-lateral
cyclic Coupling

(b)

Fig. 33 Different configurations of coupled oscillators

In this work we propose to exploit the advantages of ring oscillators while improving their phase noise performance through the use of coupled oscillators. Fig. 33(a) shows different architectures of coupled oscillators reported in [44]. Fig. 33(b)

shows a cyclic coupled oscillator structure where oscillators are placed in a ring structure with each oscillator injecting a scaled copy of its signal into the succeeding oscillator [45]-[47]. Cyclic coupled ring oscillators (CCROs) were reported in [48] to provide high resolution multi-phase outputs. Here we revisit the cyclic coupled ring oscillators and propose to use the different sets of phase-shifted outputs in the implementation of *N*-Push frequency multiplication [49]. We show that the combined *N*-Push CCRO architecture can provide wideband and mm-wave frequency outputs with low phase noise. First, we present a wideband oscillator based on this technique which can operate from 3.16-12.8GHz using a ring oscillator core operating at 1-2.56GHz by leveraging two sets of multi-phase outputs available from the CCRO [50]. Second, we use this architecture to design another *N*-Push CCRO operating from 13-25GHz with a low phase noise performance. In addition, we analyze the CCRO, derive the different oscillation modes and their stability as well as derive the phase noise expression of an *M*-stage CCRO. We confirm analytically and experimentally that the phase noise for this cyclic coupled topology improves by *M* times over that of a single ring oscillator. We also show that the phase noise improvement bandwidth is proportional to the coupling strength.

This chapter is organized as follows: Section 3.2 presents the architecture of the CCRO as well as the oscillation modes analysis, their stability, and phase noise analysis. Section 3.3 presents the designed *N*-Push CCRO structures and their advantages. Measurement results are presented in Section 3.4 while the chapter is concluded in Section 3.5.

3.2 Cyclic Coupled Ring Oscillator

3.2.1 Architecture

Fig. 34 (a) shows a cyclic coupled ring oscillator which presents a special case of the oscillator array proposed in [48]. It is composed of M identical ring oscillators, each composed of N main delay cells (D_1-D_N). Coupling delay cells (D_{C1}-D_{CN}) inject a scaled version of each oscillator's current into the next oscillator stage. The transconductances of the coupling delay cells (D_{C1}-D_{CN}) are k times smaller than those of the main delay cells (D_1-D_N), where k is called the coupling factor and is less than unity. The M oscillators form a ring structure such that output of each stage feeds the next and the Mth stage feeds the first stage. In other words, each N-stage ring oscillator is injection-locked to the previous ring oscillator using progressive phase injection at every node. This multi-point injection keeps the phase balance between all the nodes [51]. This coupled oscillator structure can also be viewed as M horizontal oscillators (with N stages each: D_1-D_N) combined with N vertical oscillators (with M stages each: D_{C1}-D_{CN}). The vertical oscillators are designed to be weaker than the horizontal ones by a factor of k. In this work, a single ended architecture is adopted so M and N must be odd numbers; however, the proposed methodology can be also applied to differential structures. The delay cells of the ring oscillator as well as the coupling cells are implemented as static CMOS inverters.

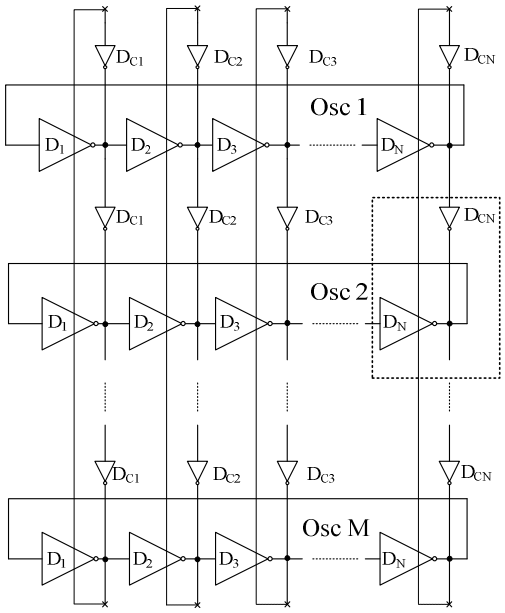


Fig. 34 Circuit diagram of the CCRO

3.2.2 Analysis of CCRO

In this section we analyze the CCRO to determine its oscillation frequency and phase noise and compare it to a single-loop *N*-stage ring oscillator. We also determine the modes of oscillation and their stability. The analysis in [52] describes how to analyze a system of coupled oscillators to arrive at the different oscillation modes and determine their stability using Adler's equation for injection locking. However, the above work uses tuned LC oscillators and not ring oscillators and hence, cannot be directly applied to our CCRO. Here we follow an approach similar to that proposed in [46] and [51] while taking into consideration the cyclic nature of the architecture.

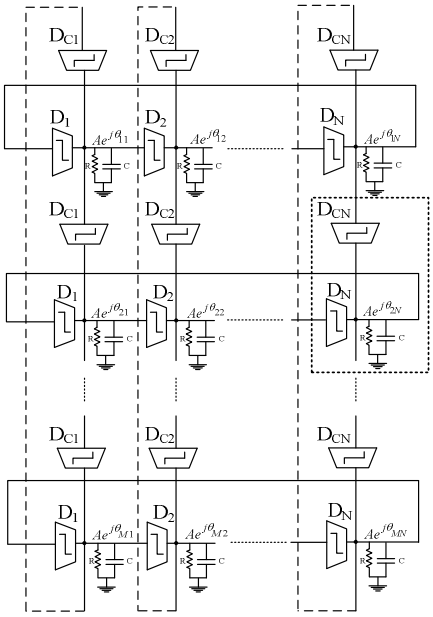


Fig. 35 Circuit model of the CCRO

We model the main delay cells and the coupling delay cells as ideal transconductors with an RC load as shown in Fig. 35. This model works for both single ended and differential delay cells. In the case of inverter based transconductances, the generated current is out-of-phase with the input voltage. Fig. 36 indicates the current generated by the main delay cell's transconductance (I_{osc}) and that generated by the coupling delay cell's transconductance (I_{cp}). Both currents are injected and added into the output node. Writing KCL at the output node of the second delay cell of the second horizontal oscillator (node (2,2)) yields,

$$\frac{A e^{j\theta_{22}}}{R} + C\,\frac{d\,(A e^{j\theta_{22}})}{dt} = I_{osc} e^{j(\theta_{21}+\pi)} + I_{cp} e^{j(\theta_{12}+\pi)} \tag{3.1}$$

where A is the oscillation amplitude.

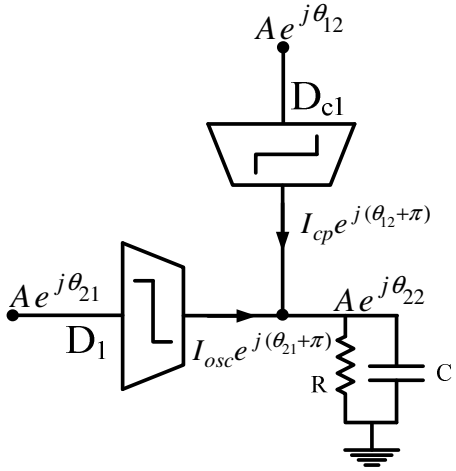


Fig. 36 Circuit model of node (2,2) in the CCRO

Assuming hard limiting transconductors such that we can neglect dA/dt in (3.1) [51], we can solve the real and imaginary equations to obtain,

$$\frac{d\theta_{22}}{dt} = \frac{1}{RC}\frac{I_{osc}\sin(\theta_{21}-\theta_{22}) + I_{cp}\sin(\theta_{12}-\theta_{22})}{I_{osc}\cos(\theta_{21}-\theta_{22}) + I_{cp}\cos(\theta_{12}-\theta_{22})} \tag{3.2}$$

Generalizing to any arbitrary node (*i*,*j*) (*i* is the row index (*i*=1 … *N*) and *j* is the column index (*j*=1 … *M*) we have,

$$\frac{d\theta_{ij}}{dt} = \frac{1}{RC}\frac{\sin(\theta_{ij-1}-\theta_{ij}) + k\,\sin(\theta_{i-1j}-\theta_{ij})}{\cos(\theta_{ij-1}-\theta_{ij}) + k\,\cos(\theta_{i-1j}-\theta_{ij})} \tag{3.3}$$

where $k = I_{cp}/I_{osc}$ is the coupling factor.

Defining the horizontal phase shift $\phi_j = \theta_{ij-1} - \theta_{ij}$ and the vertical phase shift $\psi_i = \theta_{i-1j} - \theta_{ij}$ for all values of *i* and *j*, and since $\theta_{ij} = \omega_{osc,i}t$ and $d\theta_{ij}/dt = \omega_{osc,i}$, then (3.3) can be re-written as,

$$\omega_{osc,i} = \frac{1}{RC}\frac{\sin(\phi_j) + k\ \sin(\psi_i)}{\cos(\phi_j) + k\ \cos(\psi_i)} \tag{3.4}$$

If all oscillators lock to the same frequency, ω_0, and given the symmetry of the system, then $\phi_j = \phi_0$ for all j, $\psi_i = \psi_0$ for all i and the oscillation frequency of the CCRO is given as,

$$\omega_0 = \frac{1}{RC}\frac{\sin(\phi_0) + k\ \sin(\psi_0)}{\cos(\phi_0) + k\ \cos(\psi_0)} \tag{3.5}$$

It should be noted that the oscillation frequency of a single unit oscillator can be obtained by putting k=0 in (3.5) to yield the same result as given in [51],

$$\omega_{osc,\text{single}} = \tan(\phi_0)/RC \tag{3.6}$$

To obtain ϕ_0, we have to note that the horizontal ring oscillator is composed of N inverter stages and the total phase shift around the loop has to be $2n\pi$. However, since the injected current (I_{cp}) is much smaller than the oscillators intrinsic current (I_{osc}), then each main delay cell of the horizontal ring oscillator can only supply a phase shift which is less then $\pi/2$, i.e. n=1 only. Therefore, there is only one solution for ϕ_0 given by,

$$\phi_0 = \pi + \frac{\pi}{N} \tag{3.7}$$

However, for the vertical ring oscillator, the number of inverter stages is M and the injected current (I_{osc}) is much larger than its intrinsic current (I_{cp}) and hence each coupling delay cell of the vertical ring oscillator can supply a phase shift which is larger then $\pi/2$, i.e. the phase shift around the loop can be multiples of 2π. Therefore, there might be more than one solution for ψ_0 given by,

$$\begin{aligned} &\mathrm{M}\psi_0 = 2n\pi \\ &\psi_0 = n(\frac{2\pi}{M}) \quad \text{where } \frac{M}{2} < n < M \end{aligned} \tag{3.8}$$

where different values of n correspond to different oscillation modes. For example, given M=5, n=3 or 4, i.e. ψ_0=216^o or 288^o.

To test the stability of the different oscillation modes derived in (3.8), we perform the perturbation analysis [46]. Adding a small signal perturbation $\hat{\theta}_{ij}$ to each θ_{ij} we can write,

$$\begin{aligned} \theta_{22} &= \omega_0 t + \hat{\theta}_{22} \\ \theta_{12} &= \omega_0 t + \hat{\theta}_{12} + \psi_0 \\ \theta_{21} &= \omega_0 t + \hat{\theta}_{21} + \phi_0 \end{aligned} \tag{3.9}$$

Substituting (3.9) in (3.2) and linearizing the equations assuming small perturbations, yields,

$$RC\,\frac{d\hat{\theta}_{22}}{dt} = X\,\hat{\theta}_{21} + kY\,\hat{\theta}_{12} - (X + kY)\hat{\theta}_{22} \tag{3.10}$$

where,

$$\begin{aligned} X &= \frac{1 + k\cos(\phi_0 - \psi_0)}{[\cos(\phi_0) + k\cos(\psi_0)]^2} \\ Y &= \frac{k + \cos(\phi_0 - \psi_0)}{[\cos(\phi_0) + k\cos(\psi_0)]^2} \end{aligned} \tag{3.11}$$

Also,

$$RC\,\frac{d\hat{\theta}_{32}}{dt} = X\,\hat{\theta}_{31} + kY\,\hat{\theta}_{22} - (X + kY)\hat{\theta}_{32} \tag{3.12}$$

Hence, the phase equation relating the difference in phase perturbations is given by subtracting (3.12) from (3.10),

$$RC\frac{d\Delta\hat{\theta}_{22}}{dt} = X\,\Delta\hat{\theta}_{21} + kY\,\Delta\hat{\theta}_{12} - (X + kY)\Delta\hat{\theta}_{22} \tag{3.13}$$

where $\Delta\hat{\theta}_{22} = \Delta\hat{\theta}_{22} - \Delta\hat{\theta}_{32}$, $\Delta\hat{\theta}_{21} = \Delta\hat{\theta}_{21} - \Delta\hat{\theta}_{31}$ and $\Delta\hat{\theta}_{12} = \Delta\hat{\theta}_{12} - \Delta\hat{\theta}_{22}$. Writing it in a matrix form to represent all nodes in the CCRO,

$$\frac{d}{dt}[\Delta\hat{\theta}] = [A][\Delta\hat{\theta}] \tag{3.14}$$

$$\frac{d}{dt}\begin{bmatrix} \Delta\hat{\theta}_{11} \\ \vdots \\ \Delta\hat{\theta}_{1N} \\ \Delta\hat{\theta}_{21} \\ \vdots \\ \Delta\hat{\theta}_{2N} \\ \vdots \\ \Delta\hat{\theta}_{M1} \\ \vdots \\ \Delta\hat{\theta}_{MN} \end{bmatrix}_{MN\,x1} = \frac{-1}{RC}\left[\begin{array}{c|c|c|c|c} \underline{P} & \underline{\mathbf{0}} & \cdots & \underline{\mathbf{0}} & \underline{C} \\ \hline \underline{C} & \underline{P} & \underline{\mathbf{0}} & \cdots & \underline{\mathbf{0}} \\ \hline \underline{\mathbf{0}} & \underline{C} & \ddots & \ddots & \vdots \\ \hline \vdots & \ddots & \ddots & \ddots & \underline{\mathbf{0}} \\ \hline \underline{\mathbf{0}} & \cdots & \underline{\mathbf{0}} & \underline{C} & \underline{P} \end{array}\right]_{MN\,x\,MN} \begin{bmatrix} \Delta\hat{\theta}_{11} \\ \vdots \\ \Delta\hat{\theta}_{1N} \\ \Delta\hat{\theta}_{21} \\ \vdots \\ \Delta\hat{\theta}_{2N} \\ \vdots \\ \Delta\hat{\theta}_{M1} \\ \vdots \\ \Delta\hat{\theta}_{MN} \end{bmatrix}_{MN\,x1} \tag{3.15}$$

where the primary and coupling matrices, $\underline{P}$ and $\underline{C}$, are given by,

$$\underline{P} = \begin{bmatrix} X + kY & 0 & \cdots & 0 & -X \\ -X & X + kY & 0 & \cdots & 0 \\ 0 & -X & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & -X & X + kY \end{bmatrix}_{N\,x\,N} \tag{3.16}$$

$$\underline{C} = \begin{bmatrix} -kY & 0 & \cdots & 0 \\ 0 & -kY & \ddots & \vdots \\ \vdots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & -kY \end{bmatrix}_{N \times N} \tag{3.17}$$

and $\underline{\mathbf{0}}$=zeros(*N*,*N*).

This above analysis arrives at a matrix [*A*], defined in (15)-(17) which defines the stability of the different oscillation modes. By finding the eigen values of the matrix [*A*] for each available solution for ψ_0 we can determine the mode stability. Eigen values with a negative real part correspond to a stable mode. Since, the given equations are complicated to find an analytical solution, numerical methods were used for specific numbers of *N* and *M*. Results show that all modes calculated from (3.8) are stable modes. However, practically only the mode which undergoes the highest amplification grows faster and hence is sustained by the loop [46], as will be shown from the graphical analysis. Nevertheless, for the proposed application anyone of these modes will suffice as will be shown later.

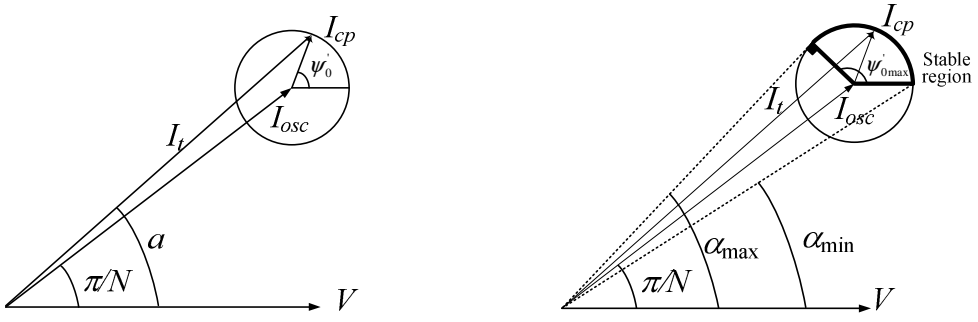
Next we carry out the graphical analysis of the CCRO model shown in Fig. 36 to determine the region of stable modes (allowable values of ψ_0). We take the voltage at node (2,2), $A e^{j\theta_{22}}$, as the reference so we can plot the phasor diagram of the currents as shown in Fig. 37(a) [46]. The total current entering the RC load, I_t, consists of two components: I_{osc} with a phase of $\phi_0' = \phi_0 + \pi = \pi$N and I_{cp} with a phase of $\psi_0' = \psi_0 + \pi$. Hence, I_t now lags the voltage by an angle α given by (3.18) which depends on ϕ_0, ψ_0 and *k*.

$$\tan(\alpha) = \frac{\sin(\phi_0) + k\ \sin(\psi_0)}{\cos(\phi_0) + k\ \cos(\psi_0)} \tag{3.18}$$

The region of stable modes can be determined using the perturbation analysis outlined in [46] and is illustrated as the bolded area in Fig. 37(b) defined by $\alpha_{\min}$ to $\alpha_{\max}$. $\alpha_{\max}$ happens when I_t is tangent to the circle whose radius is I_{cp}. The angle $\psi'_{0,\max}$ in this case determines the upper boundary of the stable region of operation. In addition, since the delay cells are inverters $\pi < \psi_0 < 2\pi$, so $0 < \psi'_0 < \pi$ and hence $\psi'_{0,\min} = 0$ determines the lower bound of the stable region. From the geometry in Fig. 37(b) $\psi'_{0,\max}$ can be determined and used to identify the region of stable modes and is found to be,

$$\psi'_{0,\max} = \frac{\pi}{N} - \cos^{-1}(k) + \pi \tag{3.19}$$

Therefore, for a mode to be stable the value of the corresponding ψ_0 (calculated from (3.8)) should be less than $\psi_{0,\max} = \psi'_{0,\max} - \pi$ and larger than π. This is an easier way to determine mode stability.



(a) (b)

Fig. 37 (a) Phasor diagram of the currents of the CCRO (b) Region of mode stability

Next, we determine the frequencies of the stable modes of the CCRO. We note that the oscillation frequency of the CCRO deviates from that of a single oscillator as indicated by (3.5) and (3.6). Hence, we can write the oscillation frequency of a CCRO as,

$$\omega_0 = \omega_{osc,\text{single}} + \Delta\omega = \omega_p \tan(\alpha) \tag{3.20}$$

where $\omega_p = 1/RC$. Using (3.18) and assuming $k << 1$, ω_0 can be derived to be,

$$\omega_0 = \omega_{osc,\text{single}} + k \frac{\omega_0}{\frac{1}{2}\sin(2\phi_0)} \sin(\psi_0 - \phi_0) \tag{3.21}$$

Hence, the frequency of the stable mode depends on the corresponding ψ_0. In other words, if $\psi_0 < \phi_0$ then $\Delta\omega < 0$ and frequency decreases (α decreased), while if $\psi_0 > \phi_0$ then $\Delta\omega > 0$ and frequency increases (α increased) and if $\psi_0 = \phi_0$ then $\Delta\omega = 0$ and frequency is equal to that of a single ring oscillator. It should be noted that the shift in the oscillation frequency of the CCRO is scaled down by *k* indicating that frequency shift is much smaller than the oscillation frequency.

Fig. 38 shows the gain and phase responses of a transconductance stage with a RC pole load. The gain response shows that different modes will encounter different amplification factors during startup of the oscillator. However, only the mode with the highest gain will be sustained [46]. This is because this mode will grow faster than the other modes saturating the gain of the ring oscillator and forcing all other modes to attenuate and decay. Therefore, the oscillator will only sustain the oscillations of this mode. Fig. 38 also illustrates that as frequency increases the phase shift α increases and

the gain decreases. Hence, the mode with the lowest frequency, i.e. smallest α (or smallest ψ_0') will be sustained.

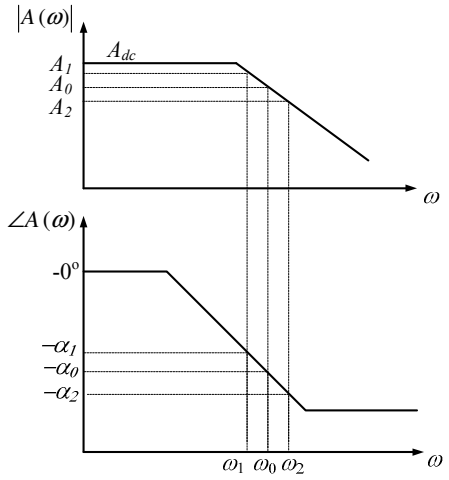


Fig. 38 Magnitude and phase plots of the gain of a single delay stage

3.2.3 Phase Noise Analysis

One of the advantages of the coupled oscillators is their low phase noise performance compared to a single oscillator. Power is increased *M* times due to the presence of *M* oscillators but there are also *M* more noise sources. However, noise increases by $\sqrt{M}$ which results in an overall improvement in the phase noise performance by $\sqrt{M}$ times or $10\log(M)\ dB$. The mechanical analogy in [53] provides an intuitive insight of the mechanism of noise reduction. Several coupled systems have more mass and hence more inertia than a single one and hence are more resistant to impulse displacements than a single system. However, some might argue that the phase noise improvement in *M* coupled oscillators should be different than the case where the

power is increased by M times in a single oscillator because the coupling factor is much less than unity. An intuitive explanation can be made as follows: A single oscillator dissipating M times the power is equivalent to a coupled system of M oscillators with a unity coupling factor. In both systems, any noise perturbation affects the whole system of oscillators and thus gets rejected by their large collective power (mass/inertia in the mechanical model) and hence, the phase noise is improved. On the other hand, for a weakly coupled system, the oscillators inject small currents into each other and hence require more time to correct for any perturbation that happens. Thus, noise perturbations will affect the coupled system differently according to the frequency of the noise. Low frequency noise perturbations will allow the weakly coupled system enough time to respond and correct for this perturbation and hence achieve the phase noise improvement while fast perturbations or high frequency noise will experience less rejection from the coupled system. Hence, as will be seen from the results of the following analysis, the value of the coupling factor mainly affects the bandwidth of the phase noise improvement and not its value, i.e. the larger the coupling factor, the wider the bandwidth of phase noise improvement and vice versa.

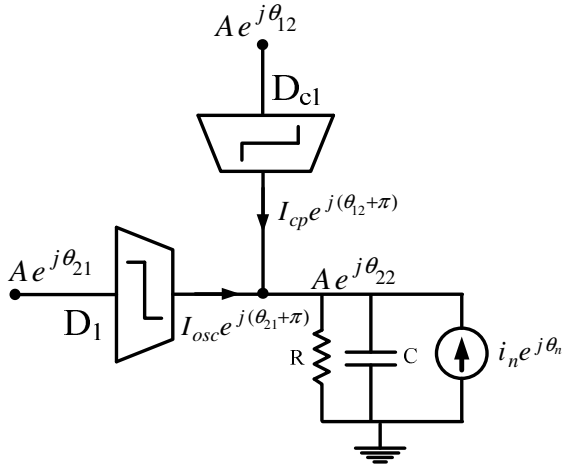


Fig. 39 Circuit model of node(2,2) including the noise source

The circuit model shown in Fig. 39 is similar to that in Fig. 36 except for an additional noise current modeling the noise of the active devices. The noise current can be viewed as an injection-locking signal which pulls the oscillator frequency and hence, changes it phase [51]. We model the noise in a 1Hz bandwidth at a frequency ω_m offset from the oscillation frequency ω_0 as $i_n e^{j\theta_n}$ where $\theta_n = (\omega_0 + \omega_m)t$. Accordingly, we can apply the previous analysis but including this noise current. The phase equation given in (3.2) is modified to be,

$$\frac{d\theta_{22}}{dt} = \frac{1}{RC}\frac{I_{osc}\sin(\theta_{21}-\theta_{22}) + I_{inj}\sin(\theta_{12}-\theta_{22}) - i_n\sin(\theta_n-\theta_{22})}{I_{osc}\cos(\theta_{21}-\theta_{22}) + I_{inj}\cos(\theta_{12}-\theta_{22}) - i_n\cos(\theta_n-\theta_{22})} \tag{3.22}$$

We perform the perturbation analysis to determine the phase noise expression of the CCRO. Simplifying (3.22) we get,

$$RC\frac{d\hat{\theta}_{22}}{dt} = X\,\hat{\theta}_{21} + kY\,\hat{\theta}_{12} - (X + kY)\hat{\theta}_{22} + \frac{i_n\sqrt{a^2+b^2}}{I_{osc}b^2}\cos(\omega_m t + \gamma) \tag{3.23}$$

where X and Y are the same as defined before and a, b and γ are defined as,

$$\begin{aligned} a &= \sin(\phi_0) + k\ \sin(\psi_0) \\ b &= \cos(\phi_0) + k\ \cos(\psi_0) \\ \gamma &= \tan^{-1}(b\,/\,a) \end{aligned} \tag{3.24}$$

Assuming that this periodic noise perturbation results in a periodic change in the phases at ω_m, we can write (3.23) in a phasor form as,

$$\left[(X + kY) + j\,\omega_m RC\right]\hat{\Theta}_{22} = X\,\hat{\Theta}_{21} + kY\,\hat{\Theta}_{12} + \frac{i_n\sqrt{a^2+b^2}}{I_{osc}b^2}e^{j\gamma} \tag{3.25}$$

which in matrix form for all nodes of the CCRO becomes,

$$[\hat{\Theta}] = [A]^{-1}[n] \tag{3.26}$$

$$\begin{bmatrix} \hat{\Theta}_{11} \\ \vdots \\ \hat{\Theta}_{1N} \\ \hline \hat{\Theta}_{21} \\ \vdots \\ \hat{\Theta}_{2N} \\ \hline \vdots \\ \hat{\Theta}_{M1} \\ \vdots \\ \hat{\Theta}_{MN} \end{bmatrix}_{MN\ x\ 1} = \left[\begin{array}{c|c|c|c|c} \underline{P} & \underline{\mathbf{0}} & \cdots & \underline{\mathbf{0}} & \underline{C} \\ \hline \underline{C} & \underline{P} & \underline{\mathbf{0}} & \cdots & \underline{\mathbf{0}} \\ \hline \underline{\mathbf{0}} & \underline{C} & \ddots & \ddots & \vdots \\ \hline \vdots & \ddots & \ddots & \ddots & \underline{\mathbf{0}} \\ \hline \underline{\mathbf{0}} & \cdots & \underline{\mathbf{0}} & \underline{C} & \underline{P} \end{array}\right]^{-1}_{MN\ x\ MN} \begin{bmatrix} 0 \\ \vdots \\ 0 \\ \hline 0 \\ n_{22} \\ \vdots \\ 0 \\ \hline \vdots \\ 0 \\ \vdots \\ 0 \end{bmatrix}_{MN\ x1} \tag{3.27}$$

where $n_{22} = \dfrac{i_n\sqrt{a^2+b^2}}{I_{osc}b^2}e^{j\gamma}$ which corresponds to the noise current injected at node (2,2), i.e. second row and second column. The matrix $\underline{C}$ is the same (3.17) but $\underline{P}$ changes to,

$$\underline{P} = \begin{bmatrix} X + kY + j\omega_m RC & 0 & \cdots & 0 & -X \\ -X & X + kY + j\omega_m RC & 0 & \cdots & 0 \\ 0 & -X & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots & 0 \\ 0 & \cdots & 0 & -X & X + kY + j\omega_m RC \end{bmatrix}_{N\ x\ N} \tag{3.28}$$

The inversion of [*A*] can be proven to take this form,

$$[A]^{-1} = \frac{1}{\det(\underline{P}^M + \underline{C}^M)} \begin{bmatrix} \underline{P}^{M-1} & \underline{C}^{M-1} & \cdots & \underline{P}^{M-2}\underline{C} \\ \underline{P}^{M-2}\underline{C} & \underline{P}^{M-1} & \cdots & \underline{P}^{M-3}\underline{C}^2 \\ \underline{P}^{M-3}\underline{C}^2 & \underline{P}^{M-2}\underline{C} & \cdots & \underline{P}^{M-4}\underline{C}^3 \\ \vdots & \vdots & \cdots & \vdots \\ \underline{C}^{M-1} & \underline{P}\underline{C}^{M-2} & \cdots & \underline{P}^{M-1} \end{bmatrix}_{MN\ x\ MN} \tag{3.29}$$

It should be noted that successive rows and columns of the above matrix contain the same terms but shifted by one position. From (3.26) and (3.29), we observe that the noise n_{22} injected at node (2,2) affects all other nodes in the coupled oscillator. Hence, to find the effect of the noise currents injected into all nodes of the coupled oscillator, the noise vector n is modified to $[n] = \frac{i_n\sqrt{a^2+b^2}}{I_{osc}b^2} e^{j\gamma}\begin{bmatrix}1 & 1 & \cdots & 1\end{bmatrix}^T_{MN\ x\ 1}$ and all phase variations are added as the mean square to yield,

$$\begin{aligned} \left[\overline{\hat{\Theta}}_i^2\right]_{N\ x\ 1} &= \frac{\overline{i}_n^{\,2}(a^2+b^2)}{I_{osc}^2 b^4} \frac{1}{\left|\det(\underline{P}^M + \underline{C}^M)\right|^2} \\ &\times\left[\left|\underline{P}^{M-1}\underline{I}\right|^2 + \left|\underline{P}^{M-2}\underline{C}\,\underline{I}\right|^2 + \left|\underline{P}^{M-3}\underline{C}^2\underline{I}\right|^2 + \cdots + \left|\underline{C}^{M-1}\underline{I}\right|^2\right] \quad i = 1\ldots M \end{aligned} \tag{3.30}$$

The injected noise is assumed to be white with two noise components at $\omega_0 - \omega_m$ and $\omega_0 + \omega_m$. The noise power spectral density of each component is

$S_n(\omega_m) = i_n^2 / 2 = 4kT / R$. Hence, the single side band phase noise expressions at the nodes of the i^{th} oscillator can be given as,

$$\begin{aligned}\left[\mathfrak{L}(\omega_m)\right]_{N\,x\,1} = \frac{S_\theta(\omega_m)}{2} = \frac{8kT}{R}\frac{(a^2+b^2)}{I_{osc}^2 b^4}\frac{1}{\left|\det(\underline{P}^M + \underline{C}^M)\right|^2} \\ \times\left[\left|\underline{P}^{M-1}\underline{I}\right|^2 + \left|\underline{P}^{M-2}\underline{C}\,\underline{I}\right|^2 + \left|\underline{P}^{M-3}\underline{C}^2\underline{I}\right|^2 + \cdots + \left|\underline{C}^{M-1}\underline{I}\right|^2\right] \quad i = 1\ldots M\end{aligned} \tag{3.31}$$

where $S_\theta(\omega_m)$ is the phase power spectral density. The phase noise of a single-loop ring oscillator can be obtained by substituting k=0 in the analysis above and is given by,

$$\mathfrak{L}(\omega_m) = \frac{2S_n(\omega_m)}{I_{osc}^2}\frac{1}{\left|(1+jRC\,\omega_m\cos^2(\pi/N))^N - 1\right|^2}\frac{\left|1+jRC\,\omega_m\cos^2(\pi/N)\right|^{2N} - 1}{\left|1+jRC\,\omega_m\cos^2(\pi/N)\right|^2 - 1} \tag{3.32}$$

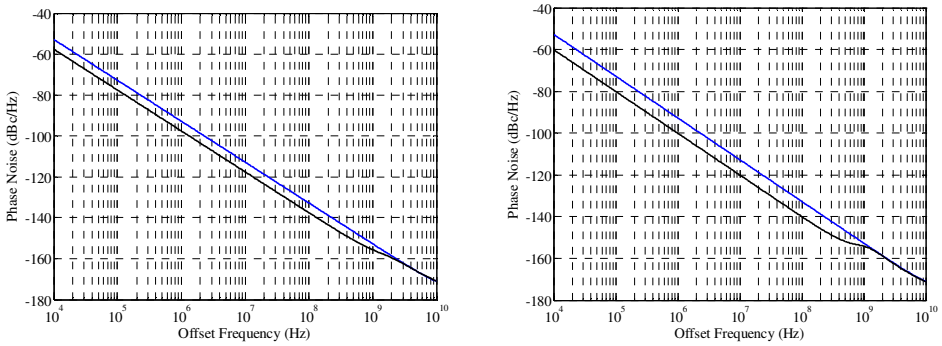
This expression can be proven to match the expression derived in [51]. For a fair comparison between the phase noise of the CCRO and a single ring oscillator, we should note the following:

1. The total current used in one stage of the CCRO should be equal to that of the single-loop oscillator case. From the analysis done before: $I_t = I_{osc}\sqrt{a^2+b^2}$.
2. For the case where $N \neq M$ in the CCRO, the oscillation frequency of the CCRO deviates from that of the single-loop ring oscillator as given in (3.20). This change in frequency should also be accounted for when calculating the final phase noise improvement because phase noise degrades at higher frequencies.

We now substitute with numerical values in (3.31) and (3.32), and compare the phase noise of the CCRO with that of a single-loop ring oscillator. A 3GHz oscillator

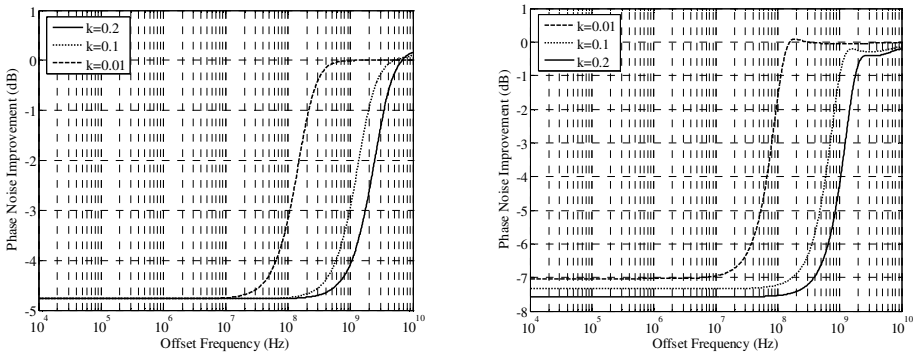
with a current of I_{osc}=7mA and k=0.1 is assumed for the calculations and only thermal noise is considered.

Fig. 40 plots the phase noise for the cases of N=3, M=3 and N=3, M=5. As can be observed from the figure, the phase noise of the CCRO is less than that of a single ring oscillator by $10log(M)$ over a the lower range of frequency offsets (the phase noise improvement bandwidth) and then degrades and follows that of the single ring oscillator for higher frequencies offsets. Fig. 41 shows the phase noise improvement bandwidth for coupling factors k=0.01, 0.1 and 0.2, for the cases of N=3, M=3 and N=3, M=5. As mentioned before the coupling factor affects the bandwidth only and not the value of the phase noise improvement.



(a) (b)

Fig. 40 Calculated phase noise plot for the case of (a) N=M=3 CCRO and (b) N=3, M=5 CCRO, with k=0.1



(a) (b)

Fig. 41 Calculated phase noise improvement for the case of (a) N=M=3 CCRO and (b) N=3, M=5 CCRO, for k=0.01, 0.1 and 0.2

3.3 *N*-PUSH CCRO

3.3.1 *N*-Push Technique

N-Push techniques have been used in literature to generate a higher frequency signal from a lower frequency oscillator [3], [49], [55] – [55]. The simplest example used for illustration is that adding two out-of-phase signals cancels the fundamental tone as well as the odd harmonics and preserves the even ones. This can be extended to *N*-signals with $2\pi/N$ phase differences to produce the *N*th harmonic while cancelling all lower order ones. Table 4 shows examples detailing the number of needed signals and their phase shifts that when added together cancels some harmonics and enforces others. It also details the number of phases needed for single, differential and I-Q outputs for the case of frequency doubling. Consequently to apply the *N*-Push techniques to the output of an oscillator, it needs to have a multi-phase output providing the required phases as well as a limiting circuit that ensures that these signals are rich in harmonics. The order of the phase shifted signals is not important in the *N*-Push operation as long as all phase

shifts are available. The price of having a higher frequency is an increase in the power and area of the *N*-Push oscillator. Also, phase noise degrades by a factor of N^2 or $20\log(N)\ dB$ due to frequency multiplication.

Ring oscillators inherently provide different phase shifted signals, and so the *N*-Push technique can be used with significantly less area and power overhead than the LC counterparts. In this work we propose to use the *N*-Push technique with CCROs to obtain a low phase noise wideband oscillator as well as a low phase noise mm-wave oscillator. We illustrate that for the proposed *N*-Push CCRO, a higher FOM can be obtained as described in the two design cases presented next.

Table 4 Phase shifts required for different *N*-Push operations

Number of Signals	Phase shifts	Preserved Harmonics	Cancelled Harmonics	Output type
2	0^o,180^o	2, 4, 6, …	1, 3, 5, …	Single
2	0^o, 90^o, 180^o, 270^o	2, 4, 6, …	1, 3, 5, …	Differential
2	(0^o, 90^o, 180^o, 270^o), (45^o, 135^o, 225^o, 315^o)	2, 4, 6, …	1, 3, 5, …	I,Q
3	0^o,120^o, 240^o	3, 6, 9, …	1, 2, 4, 5, …	Single
3	0^o, 60^o, 120^o, 180^o 240^o, 300^o	3, 6, 9, …	1, 2, 4, 5, …	Differential
4	0^o, 90^o, 180^o, 270^o	4, 8, 12, …	1, 2, 3, 5, 6, 7, …	Single
5	0^o, 72^o, 144^o, 216^o, 288^o	5, 10, 15, …	1, 2, 3, 4, …	Single

3.3.2 Design Cases of *N*-Push CCRO

3.3.2.1 A Wideband 3-12.8GHz *N*-Push/*M*-Push CCRO

The first design demonstrates a wideband oscillator with a very wide tuning range using an oscillator with a smaller tuning range [50]. As mentioned before, the proposed CCRO provides *N* signals phase shifted by $\phi_0 = \pi + \pi / N$ and provide *M* sets of those *N*-signals shifted by $\psi_0 = \pi + (2n+1)\pi / M$ (where $n \in \mathbb{Z}$ and $0 < n < M/2$). Hence, we can apply the *N*-Push technique to the *N* signals and *M*-Push to the *M* signals to provide two output signals. By suitable choice of the ring oscillator's operating frequency, *N*, and *M*, a wide tuning range can be achieved.

In this work, five three-stage ring oscillators (*N*=3, *M*=5) operating at 1-2.5 GHz using CMOS inverters as delay cells are coupled to form the CCRO shown in Fig. 42. The three vertical outputs are added together using an adder stage made of three CMOS inverters with the outputs tied together to generate the third harmonic tone and cancel the fundamental tone. The five horizontal signals are added in a similar fashion to produce the fifth harmonic as shown in Fig. 42. The *N*-Push/*M*-Push CCRO is tuned by changing the supply voltage of the delay cells. Illustration of the proposed frequency planning is depicted in Fig. 43. The *N*-Push output range is 3-7.5GHz (frequency multiplication by 3) while the *M*-Push range is 5-12.5GHz (frequency multiplication by 5) giving an overall continuous range of 3-12.5GHz. This output has a tuning range (defined as the bandwidth divided by the center frequency) of 122.6%. Moreover, including the 1-2.5GHz range increases the tuning range to 163%. Potential applications of such oscillator would be software defined radios supporting several standards and the

IEEE 802.16a (2-11 GHz) standard. This *N*-Push/*M*-Push CCRO can also be used with UWB if employed within a digital PLL with fast settling times satisfying the stringent requirements of UWB.

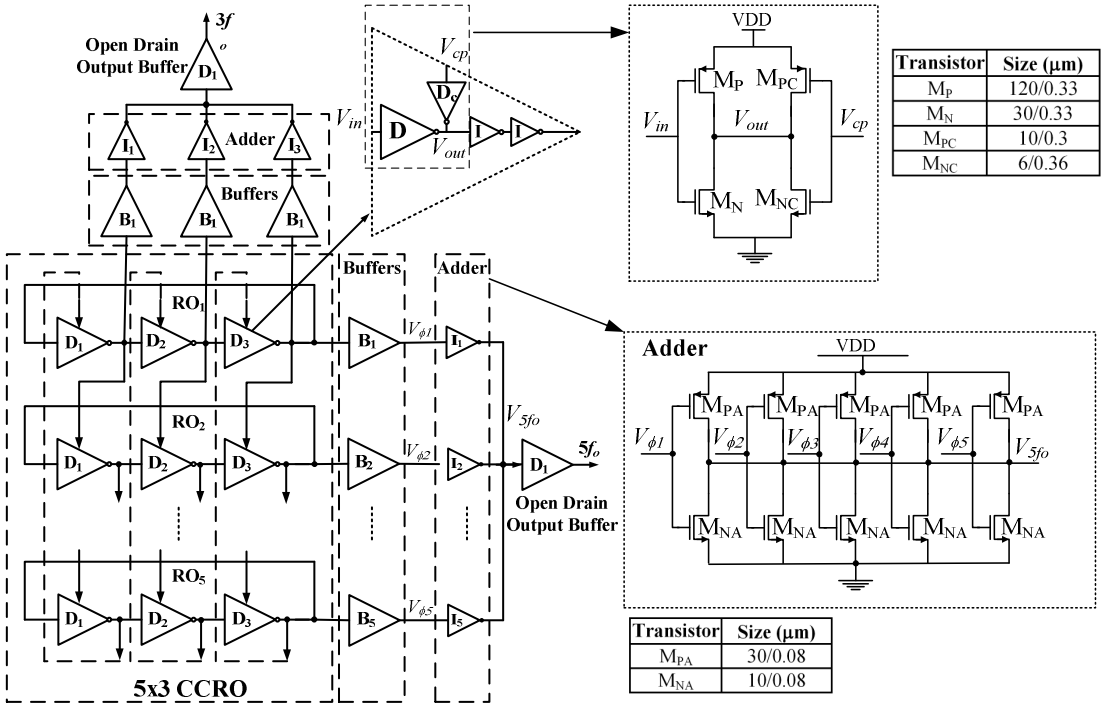


Fig. 42 Circuit diagram of the wideband *N*-Push/*M*-Push CCRO

This great boost in frequency tuning range can relax the design of oscillators required for wideband application. Fig. 44 illustrates a conceptual PLL employing the proposed oscillator. The core oscillator integrated in the PLL will have a tuning range at most (*N*+*M*) times smaller than the required tuning range and can hence be designed to have a lower frequency gain, K_{VCO}. This reduces the sensitivity of the oscillator to the control voltage perturbations and thus improves the phase noise performance and

reference spur suppression. It also relaxes the requirements on the divider and reduces its power consumption as it now operates at a significantly lower frequency and a smaller tuning range. In addition, this topology enables the core ring oscillator of the CCRO to run at a lower frequency. Hence, we can use larger devices for the delay cells (120μm/330nm for the PMOS and 30μm/330nm for the NMOS) which lowers the phase noise as well as reduces the mismatches between transistors. Moreover the CCRO has a lower phase noise than a single ring oscillator by *M* times.

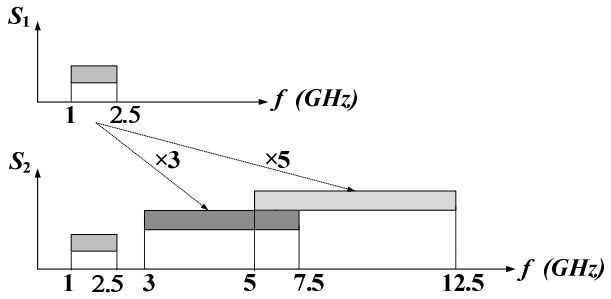


Fig. 43 The output frequency spectrum of the wideband CCRO showing the bandwidth extension due to the combined *N*-Push/*M*-Push operation

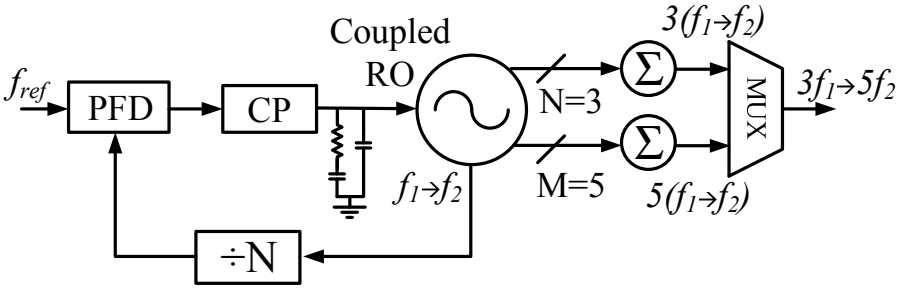


Fig. 44 Block diagram of a PLL employing the proposed oscillator

We should recall here that several modes given by (3.8) can be stable within the CCRO as proved before. We notice that these modes have the same set of equally spaced phase shifted signals but in different order, as illustrated in Fig. 45 for the case of M=5, and also with slightly different frequencies (depending on ψ_0 as given by (3.21)). We have mentioned that only the mode with the highest gain will survive, however, if for any reason another mode becomes stable the M-Push CCRO will still work properly. This is because the M-Push technique only needs M equally spaced phase-shifted signals (in any order) to work correctly. There will be a slight shift in the output frequency which can be compensated by the PLL loop.

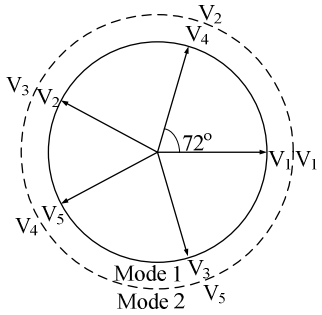


Fig. 45 The phasor diagram of the relative voltage phases of the different ring oscillators within the CCRO showing the two stable modes for M=5

3.3.2.2 Millimeter-Wave 13-25GHz N-Push CCRO

The second design illustrates the advantage of the CCRO in providing a low phase noise multi-phase millimeter-wave (mm-wave) frequency output. Recall that the M coupled ring oscillators have M times less phase noise than a single-loop ring oscillator. Also, increasing the power consumption by M times in ring oscillators reduces

the phase noise by *M* times due to faster transitions for the output signal. Hence, some might argue that to achieve a phase noise performance similar to that of the CCRO we can just spend the same amount of power in a single ring oscillator. This might be true for lower frequencies; however, it has practical limitations at mm-wave frequencies. High currents flowing in the transistors and interconnects necessitates that metal lines have enough width to accommodate those high currents without inducing reliability issues such as electro-migration problems. Doing so adds more parasitic capacitances to the transistors' output node which limits the highest achievable frequency of operation. In particular at mm-wave frequencies, transistors are sensitive to any slight addition of capacitance. In [56], the upper bound of the achievable phase noise in a ring oscillator was derived and proven to be dependent on the f_T of the process. However, here we use the coupled structure to reduce the phase noise beyond what is achievable from a single ring oscillator.

In addition, the *N*-Push operation allows the ring oscillator to run at a lower frequency. This permits the use of non minimum dimensions in the delays cells of the ring oscillator. Since flicker noise current is inversely proportional to the transistor length and width as given by (3.33), [57], increasing *W* and *L* while maintaining a constant g_m reduces flicker noise significantly.

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{K}{f}\frac{g_m^2}{WLC_{ox}^2} \tag{3.33}$$

Also, by sizing the PMOS to be 3-4 times the NMOS, symmetry is ensured in the output signal, which reduces the up-conversion of the flicker noise [58][59]. Also, the

symmetry leads to a 50% duty cycle signal which means absence of lower order even harmonics, providing a clean spectrum.

The final advantage of the *N*-Push CCRO is the availability of different phases of this mm-wave frequency signal. Applying *N*-Push to the outputs of each ring oscillator within the CCRO can provide *M* multi-phase signals. These mm-wave multi-phase signals can be used in mm-wave image reject receivers [41], high speed samplers or time interleaved applications [42] increasing their frequencies of operation.

A three five-stage CCRO (*N*=5, *M*=3) is presented where *N*-Push operation is applied to the two sides of the CCRO as shown Fig. 46. The core ring oscillator has a frequency range of 2.6-5GHz and uses non-minimum lengths of 140nm. The five output signals are then combined to produce the output signal of 13-25GHz. Another set of five signals are combined to produce a similar signal but with a 120^{o} phase shift as a proof of concept of the multi-phase outputs.

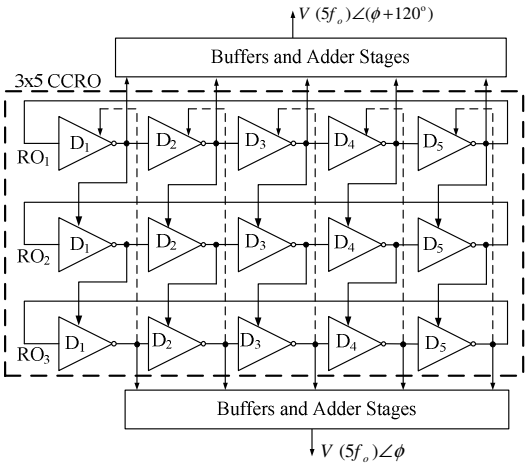


Fig. 46 Circuit diagram of the mm-wave *N*-Push CCRO showing the two outputs having different phases

3.3.2.3 Mismatch Analysis

Mismatch between delay cells can change the phase difference within one ring oscillator or between the different oscillators of the CCRO. This can have adverse effects on the results of the *N*-Push CCRO. In this section we present the Monte Carlo simulations of the wideband 3-12.8GHz 5x3 *N*-Push/*M*-Push CCRO as well as that of the millimeter wave 13-25GHz 3x5 *N*-Push CCRO in Fig. 47 and Fig. 48 respectively. Monte Carlo simulation results are carried out with the process and mismatch variations enabled. In the first oscillator there are two phase differences: one within each ring oscillator and the second between the outputs of the different ring oscillators. We notice that the standard deviation of the former is within half a degree while that of the latter is within one degree. This results in reduction of the suppression of the harmonics for the *N* and *M*-Push operations. The rejection of the fundamental tone for the *N*-Push operation is 40dB with a standard deviation of 6dB. While the rejection of the fundamental tone and the 3rd harmonic of the *M*-Push operation are 34dB and 31dB with variation limited to 6dB. Frequency of oscillation changes within 39MHz while the output amplitudes variations of the *N* and *M* Push operations are limited to 0.2dB. For the second oscillator, the variation of the phase difference within each oscillator increased to be within one degree. This is because the frequency of this oscillator is double that of the first one and the number of stages used is larger (5stages). Hence, the effects of mismatch effects increase and as a consequence the mean of the rejection of the fundamental and 3rd harmonics decreased to 28.5dB and 29.5dB, respectively. Automatic tuning or calibration circuits can increase the harmonic rejection values if needed.

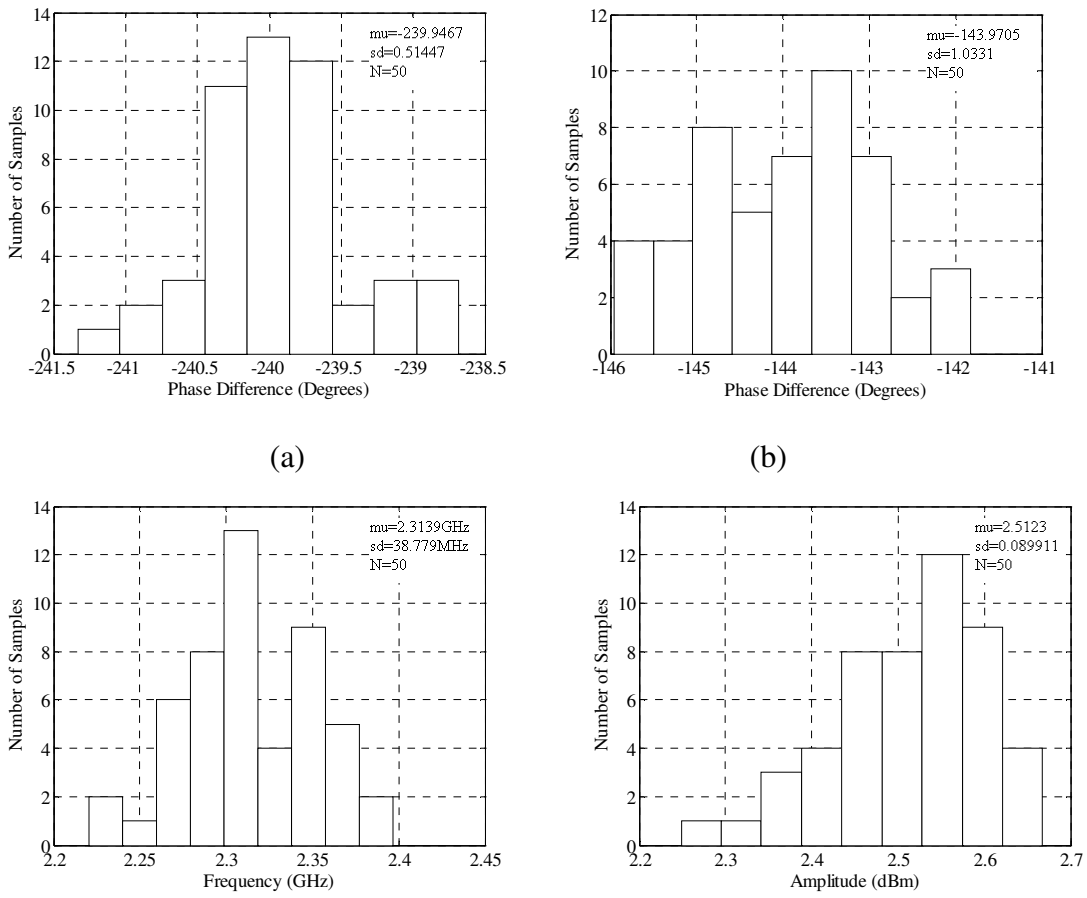
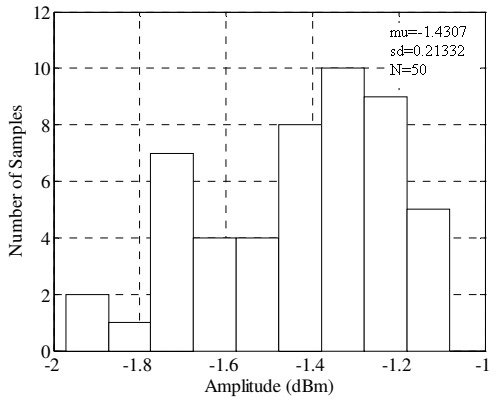
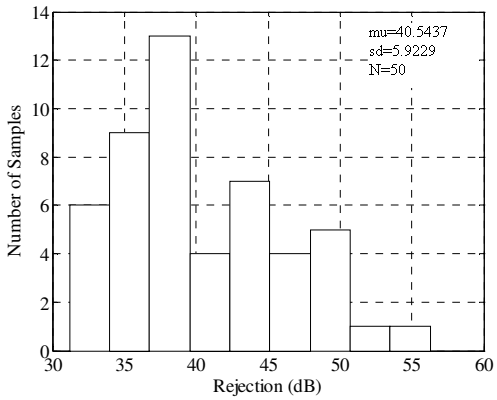
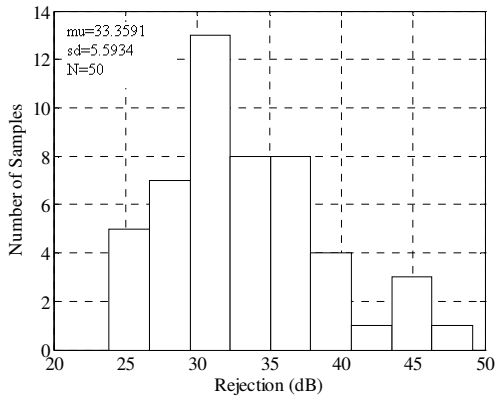


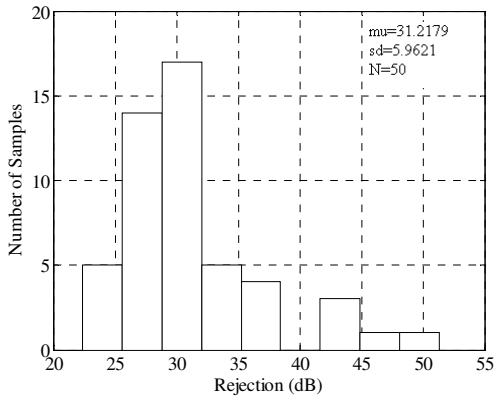
Fig. 47 Monte Carlo simulation results of the wideband 3-12.8GHz 5x3 *N*-Push/*M*-Push CCRO: (a) Phase difference within the each ring oscillator, (b) Phase difference among different ring oscillators, (c) Frequency of oscillation, (d) Amplitude of the 3rd harmonic (*N*-Push operation), (e) Amplitude of the 5th harmonic (*M*-Push operation), (f) Rejection of the fundamental tone for the *N*-Push operation, (g) Rejection of the fundamental tone for the *M*-Push operation, and (h) Rejection of the 3rd harmonic for the *N*-Push operation





(e) (f)





(g) (h)

Fig. 47 Continued

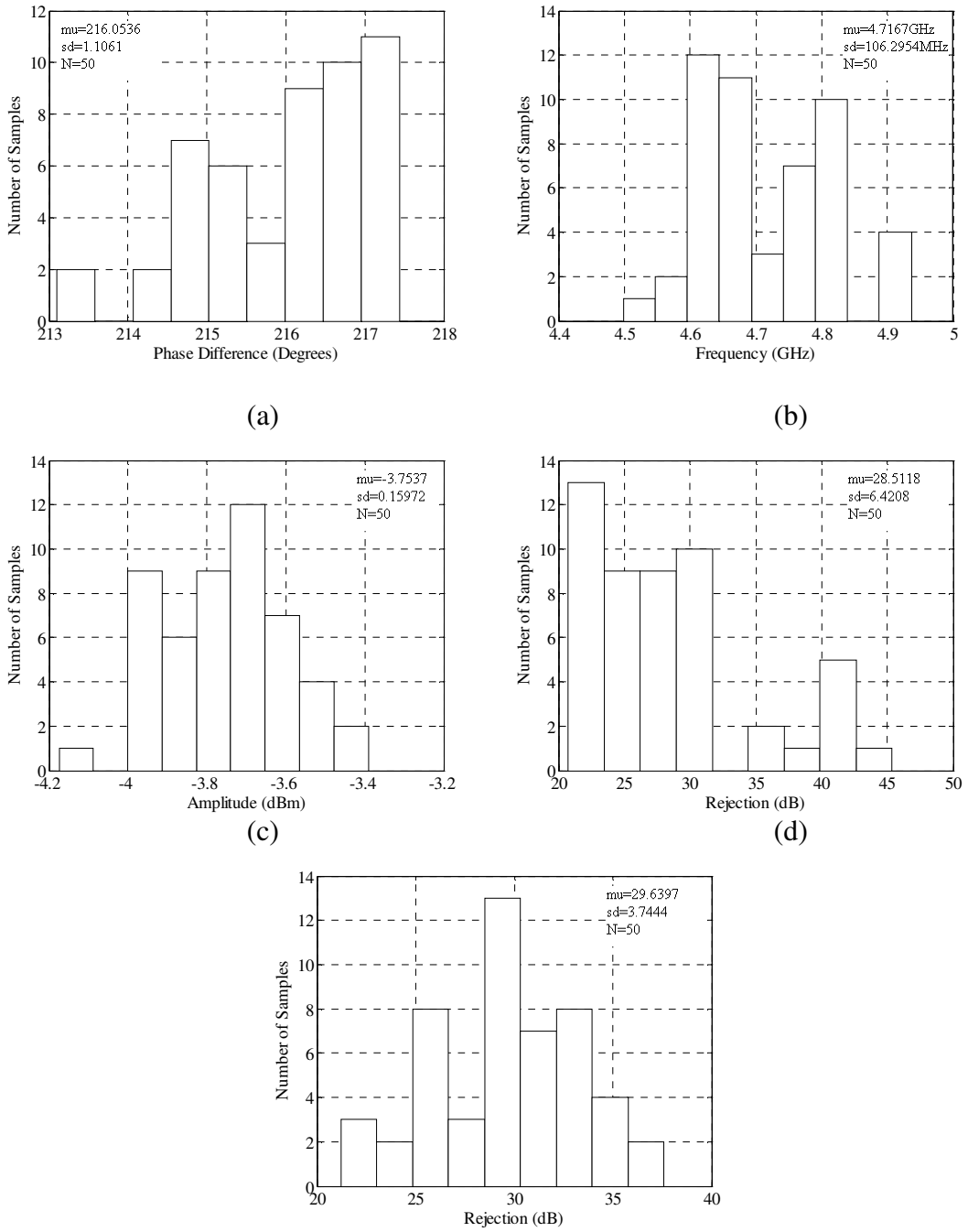


Fig. 48 Monte Carlo simulation results of the millimeter wave 13-25GHz 3x5 *N*-Push CCRO: (a) Phase difference within the each ring oscillator, (b) Frequency of oscillation, (c) Amplitude of the 5th harmonic, (d) Rejection of the fundamental tone, and (e) Rejection of the 3rd harmonic

3.4 Measurement Results

The proposed cyclic coupled ring oscillators are implemented in a 90nm digital regular V_T CMOS process with 9 metal layers. The chip micrograph, shown in Fig. 49, depicts the two designs: the wideband 3-12.5GHz 5x3 *N*-Push/*M*-Push CCRO and the mm-wave 13-25GHz 3x5 *N*-Push CCRO. They occupy an active area of 0.145mm^2 and 0.135mm^2, respectively. The outputs were tested using on-wafer probing, and the spectrum was measured using the Agilent E4446, 44GHz, power spectrum analyzer. However, since both ring oscillators are free running, measuring the phase noise using the E4446 is not accurate due to drifting of the oscillator tone. Thus, we used the Agilent E5052B 10MHz-7GHz signal source analyzer combined with the Agilent E5053A 3GHz-26.5GHz microwave down-converter to be able to accurately measure the phase noise. Agilent E5052B uses a wideband frequency discriminator technique which can capture the phase noise of drifting signals.

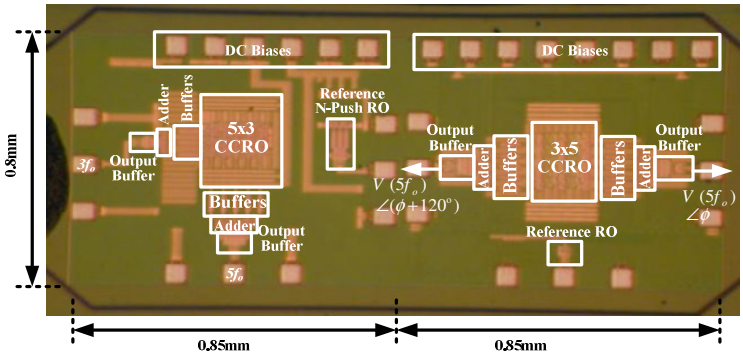


Fig. 49 Chip micrograph

3.4.1 Wideband 3-12.8GHz *N*-Push/*M*-Push CCRO

We first present the measurement results of the wideband 3-12.8GHz *N*-Push/*M*-Push CCRO with *N*=3, *M*=5. Fig. 50 shows the frequency of the *N*-Push output of this oscillator at $3f_o$ as well as the *M*-Push output at $5f_o$ versus the tuning voltage. The oscillators are tuned by changing their supply voltage. This figure illustrates the continuous frequency operation from 3.16-12.8GHz with a frequency overlap from 7.24-7.6GHz. Fig. 51(a) and (b) present the output harmonics for the *N*-Push and *M*-Push outputs respectively. They also show the cancelled lower order harmonics. The fundamental tone has more than 30dB of rejection for the *N*-Push and 40dB for the *M*-Push. Although simulations predict 45dB of suppression for the third harmonic (similar to the fundamental tone), it is observed to have only 11dB of rejection in the *M*-Push case. This is attributed to supply coupling from the *N*-Push output to the *M*-Push output, as buffers and adders of both stages share the same supply lines. A more optimized design could turn off the output not in use to avoid this effect.

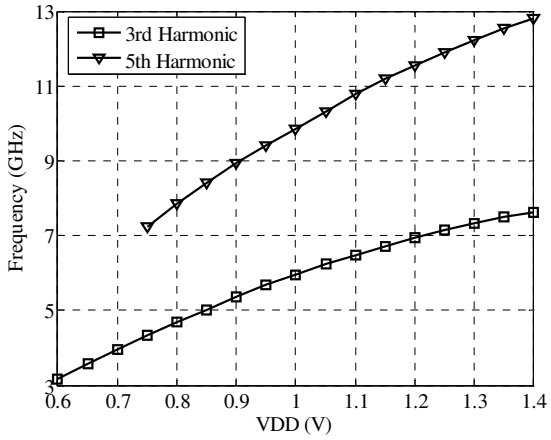
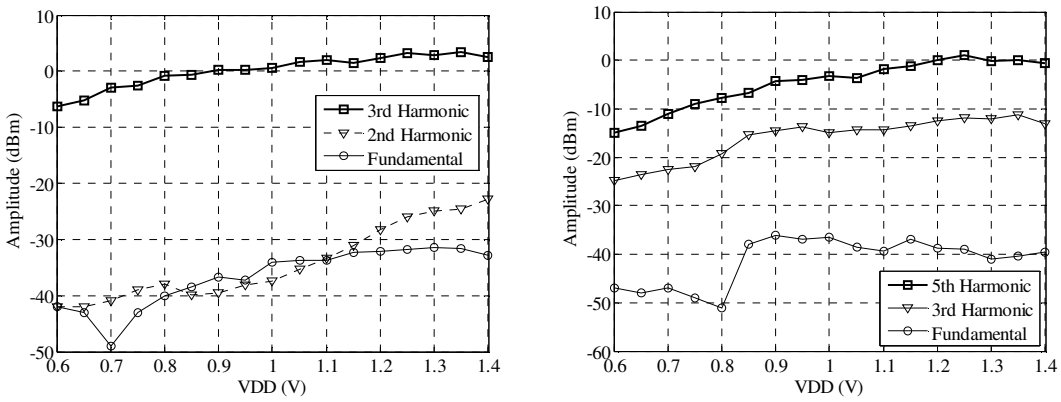


Fig. 50 Measured frequency tuning curve of the wideband 5x3 *N*-Push/*M*-Push CCRO



(a) (b)

Fig. 51 Measured amplitudes of the fundamental and harmonics tones for (a) The *N*-Push (*N*=3) and (b) *M*-Push (*M*=5) outputs

A reference *N*-Push oscillator with a single-loop three stage ring oscillator (*M*=1, *N*=3) is designed and included for comparison of the phase noise. The core ring oscillator uses inverters with transistors having the same sizes as the proposed CCRO. It runs from 1.11-2.74GHz with the *N*-Push output at 3.35-8.23GHz, which is close to the frequency of the proposed CCRO. The phase noise curves of both oscillators are plotted in Fig. 52. A difference of around 8 dB is observed over the frequency range which is close to the theoretical value of 7.57dB for a coupling factor of 0.2 as shown before in Fig. 40 This confirms the 10*log*(*M)* phase noise improvement for the proposed coupled topology experimentally.

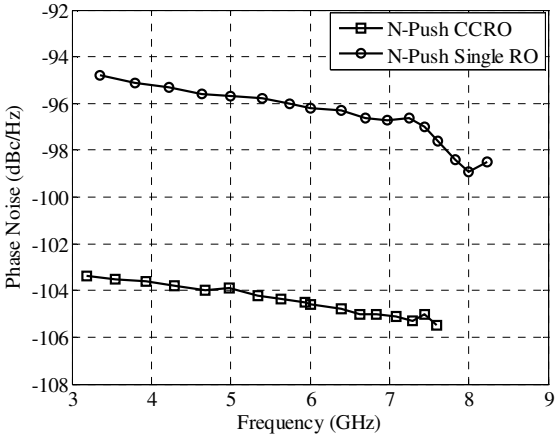


Fig. 52 Measured phase noise improvement at 1MHz offset of the CCRO

Fig. 53(a) and (b) illustrate the amplitude and phase noise of both the *N*-Push and *M*-Push outputs of the wideband oscillator versus the output frequency. We observe nearly 2dB degradation in phase noise due to the shift from frequency multiplication by 3 to multiplication by 5. Power consumption is conserved by switching between the two outputs, as the supply voltage can then be lowered, as shown in Fig. 53(c). The rms jitter (integrated from 100KHz to 10MHz) at the lowest (3.16GHz) and highest (12.8GHz) frequencies is measured to be 2.13psec and 0.76psec, respectively. To the best of the authors' knowledge, the performance of the proposed wideband *N*-Push/*M*-Push CCRO is one of the best reported in literature as shown in Table 5. The proposed oscillator has the highest Figure of Merit for Tuning (FOM_T) defined as [60],

$$FOM_T = \mathfrak{L}(\Delta f) - 20\log(\frac{f_0}{\Delta f}\frac{TR}{10}) + 10\log(\frac{P_{dc}}{1mW}) \tag{3.34}$$

where $\mathfrak{L}(\Delta f)$ is the phase noise at an offset frequency Δf, TR is the tuning range percentage and P_{dc} is the power consumption in mW.

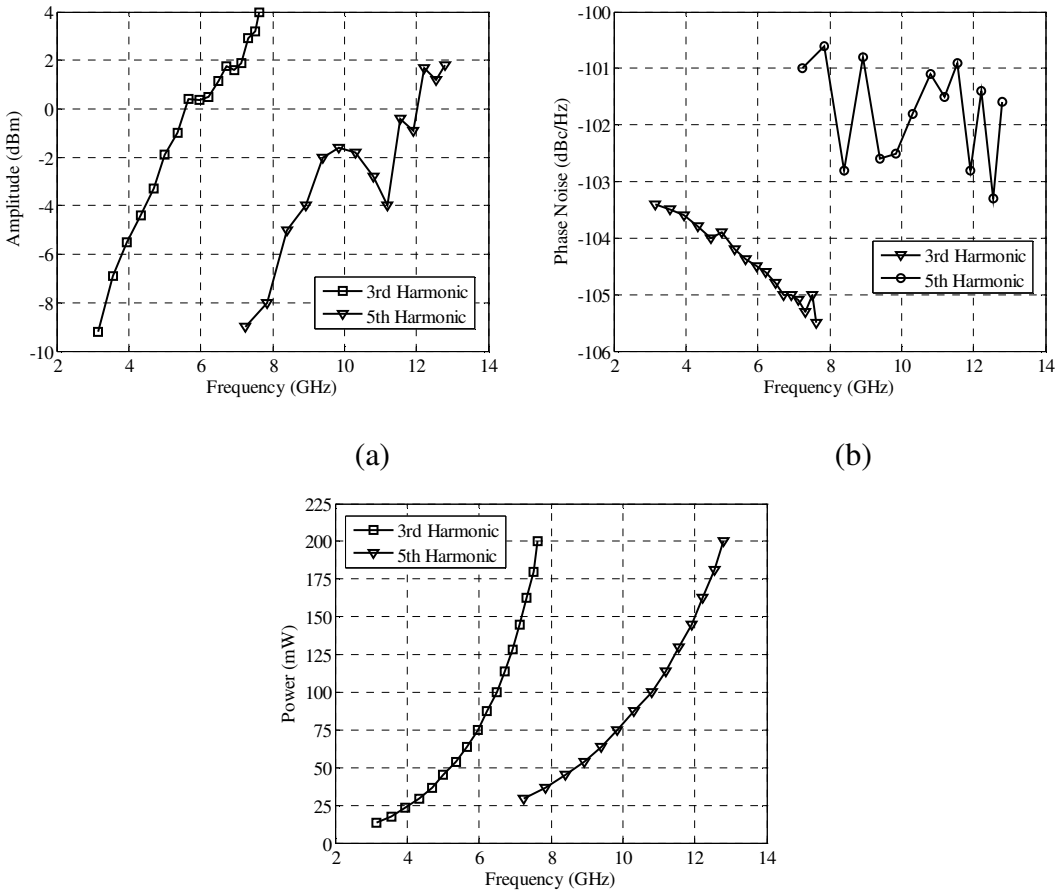


Fig. 53 (a) Measured amplitude and (b) Phase noise of the output as well as (c) The power consumption of the wideband 5x3 *N*-Push/*M*-Push CCRO

Table 5 Comparison of the performance of the wideband 5x3 *N*-Push/*M*-Push CCRO with previously published work

	Frequency Range (GHz)	Tuning Range (%)	Phase noise @ 1MHz (dBc/Hz)	Power consumption (mW)	Technology (CMOS)	FOM_T
This Work	1 – 2.56 3.16 – 12.8	163	-105.5 @ 7.7GHz	13-200	90nm	-184.4 – -190.4
[61]	1.82 – 10.18	139.4	-88.4 @ 5.65 GHz	5	130nm	-179.34
[62]	2.5 – 9	113	-85 @ 5 GHz	135	180nm	-158.7
[63]	3 – 11	114	-88 @ 5 GHz	85	190nm	-163.8
[64]	1 – 9.4	161.5	-112.3 @ 10MHz @ 6GHz	7.4	130nm	-183.33
[65]	0.8 – 10	170.37	-90 @ 6.4GHz	6	120nm	-162.97
[66]	3 – 10	107.7	-	0.3-1	90nm	-
[67]	1 – 10.3	164.6	-	3.5-17.25	130nm	-

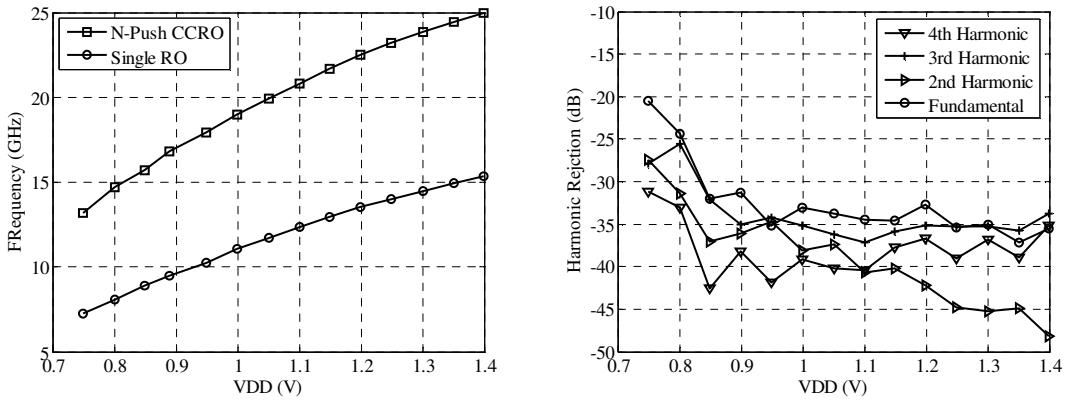
3.4.2 Millimeter-Wave 13-25GHz *N*-Push CCRO

Second, we present the measurement results of the proposed millimeter wave 13-25GHz 3x5 *N*-Push CCRO. We also designed and fabricated a reference oscillator to compare with. This reference oscillator represents the fastest three-stage single loop inverter-based ring oscillator that the process allows. The loading to the oscillator is minimized through a six stage tapered buffer to drive the output buffer. Fig. 54(a) shows the frequency tuning curve of both oscillators. The reference oscillator has an output frequency range of 7.25-15.35GHz, while the proposed oscillator has a higher frequency range of 13-25GHz. The rejection of all the lower order harmonics is more than 35dB over most of the tuning range as shown in Fig. 54(b). The phase noise performance of the proposed CCRO as well as the reference one is shown in Fig. 55. Phase noise of the

proposed oscillator is less than that of the reference oscillator by 10-20dB over the tuning range. Since, the output frequencies and power consumptions are different it is more accurate to compare the Figure of Merit (*FOM*) of oscillators defined as,

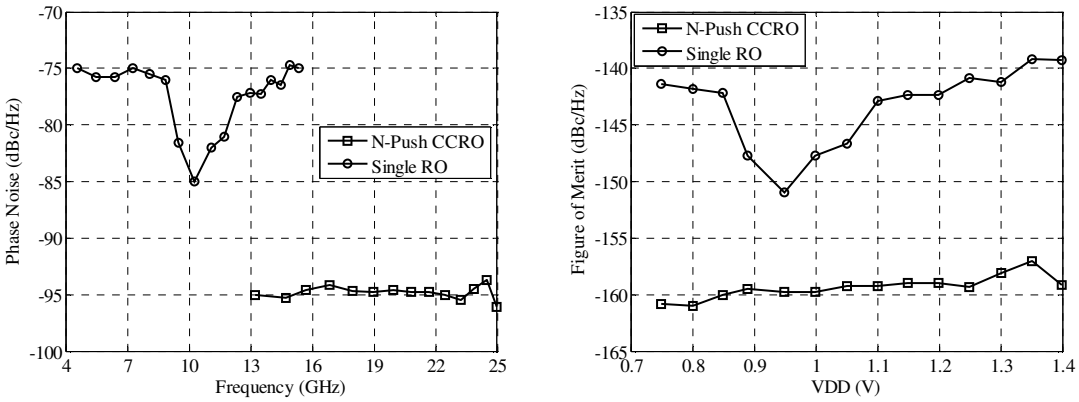
$$FOM = \mathfrak{L}(\Delta f) - 20\log(\frac{f_0}{\Delta f}) + 10\log(\frac{P_{dc}}{1mW}) \tag{3.35}$$

Fig. 55(b) shows that there is an improvement of 8.7-20.4dB in the *FOM* of the proposed oscillator across the tuning range. Fig. 56 depicts a snapshot of the phase noise of the proposed oscillator at the highest output frequency of 25GHz achieving a phase noise of -120.4dBc/Hz at a 10MHz offset frequency.



(a) (b)

Fig. 54 (a) Measured frequency tuning curve of the mm-wave 3x5 *N*-Push CCRO as well as the reference oscillator (b) The amplitudes of the lower order harmonics for the mm-wave 3x5 *N*-Push CCRO



(a) (b)

Fig. 55 (a) Phase noise at 1MHz offset and (b) *FOM* comparison of the mm-wave *N*-Push CCRO and the reference single loop oscillator

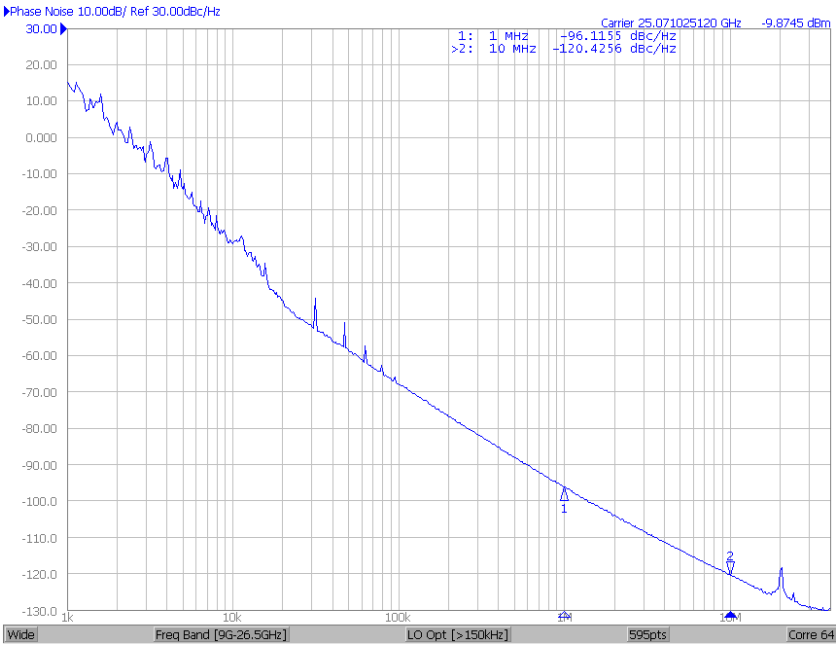


Fig. 56 Measured phase noise snapshot of the output of the mm-wave 3x5 *N*-Push CCRO at 25GHz

Measuring the phase difference of 120^{o} between the two high frequency *N*-Push outputs was not possible in the lab due to its sensitivity to any path mismatches between the two outputs. However, the concept has been proved in the previously proposed oscillator where the *M*-Push output produced the expected output. Finally, Table 6 shows a comparison with state of the art inductor-less ring oscillators at mm-wave frequencies.

Table 6 Comparison of the performance of the mm-wave 13-25GHz *N*-Push CCRO with previously published work

	Freq Range (GHz)	Tuning Range (%)	Phase noise @ 1MHz (dBc/Hz)	Power (mW)	Area (mm^2)	Technology / f_T (GHz)	Available Output phases	FOM
This Work	13-25	63.16	-96.11 @ 25GHz	37-257	0.1350	90nm/140	0, 120, 240 (simulated)	-159.2 to -161.8
[68]	28.36-31.96	11.94	-85.3 @ 31.96GHz	87	0.0108	SiGe -HBT/120	Differential	-156
[69]	22.5-25.5	10.53	-87 @ 25GHz	240	0.0225	SiGe/45	Differential	-151.89
[70]	18.33 – 21.19	14.47	-83.33 @ 21.2 GHz	152	0.0180	SiGe- HBT /120	I/Q	-148.03
[71]	13.75-21.5	43.97	-90 @ 18.69GHz	130	0.1972	InP – HBT /100	Differential	-154.29
[72]	0.1-65.8	199.4	-86@ 25GHz	1.2-26.4	0.0168	90nm CMOS / 110	Single ended	-160
	0.2-34	197.66	-69.2 @ 34GHz	2-70	0.0247	0.13µm CMOS / 98	Single ended	-141.4
[73]	18.5-25	29.89	-85 @ 24.3GHz	105.6	0.1472	0.12µm SiGe BiCMOS /200	I/Q	-152.7

Our proposed mm-wave *N*-Push oscillator provides competitive performance as well as the state of the art *FOM*. Although, [72] uses a ring oscillator as well to carry out the triple push operation, however, the advantage of our design is the reduced phase

noise due to the use of the CCRO and a CMOS structure with a symmetric waveform as well as the availability of several phases for the output at the high frequency.

3.5 Conclusion

In this work, *N*-Push cyclic coupled ring oscillators are used to implement a low phase noise wideband oscillator as well as a low phase noise mm-wave oscillator. Wide tuning range is achieved because of the availability of multiple sets of phase shifts from the CCRO. Low phase noise is possible because the core ring oscillator runs at lower frequencies and hence can have non-minimum length dimensions which reduce the noise contribution. In addition, the use of this coupling topology improves the phase noise by $10log(M)$. The CCRO is analyzed using the generalized form of Adler's equation for injection locking. We prove that phase noise improvement due to coupling happens within a certain bandwidth which depends on the coupling strength. Outside this bandwidth the phase noise follows that of a single ring oscillator. The proposed oscillators achieve low phase noise with higher *FOM* than state of the art work.

CHAPTER IV

HIGH PERFORMANCE PHASE LOCKED LOOPS

4.1 Introduction

Phase locked loops are essential blocks in all communication systems. They are responsible for generating the local oscillator signal which up converts the data to higher frequencies to be transmitted or down converts the received data to lower baseband frequencies. They are also used in providing the clock for CPUs and digital circuits to run. The main block in the PLL is the oscillator which generates the oscillating signal. The feedback loop within the PLL maintains a constant frequency of oscillation and prevents the drift of frequency due to temperature and process variations or due to aging effects.

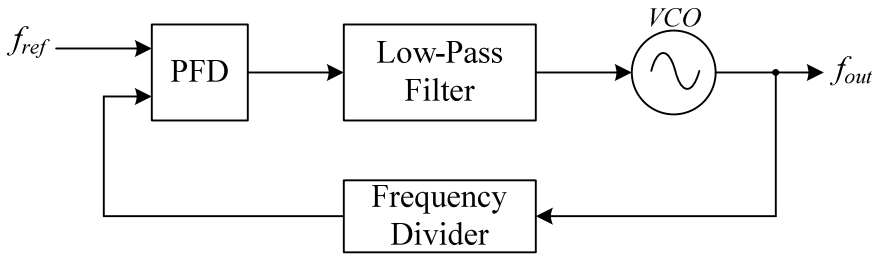


Fig. 57 Block diagram of a generic PLL

A block diagram of a PLL is shown in Fig. 57. The voltage controlled oscillator's output is applied to a divider which divides it down to a lower frequency. The frequency and phase of the divided signal is then compared to that of a reference signal produced

by a stable and clean reference. Reference frequencies are usually produced from crystal oscillators. The error signal is then applied to a filter to extract the DC component or the average of this signal. This DC component is used to control the VCO and keep it running in synchrony with reference signal.

4.2 PLL Overview

One of the most widely used PLL architectures is the Type II third order charge pump based PLL shown in Fig. 58. The type refers to the number of loss-less integrators in the loop and the order refers to the order of the closed loop system.

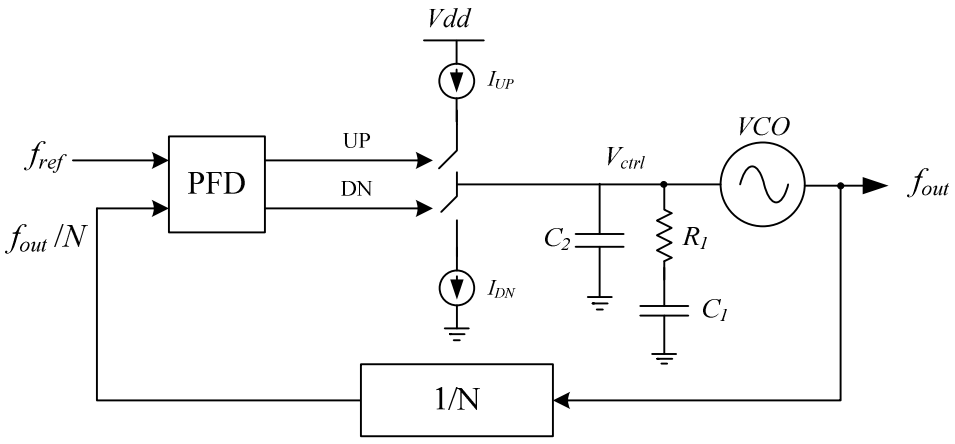


Fig. 58 Type II third order charge pump based PLL

The first block in the PLL is the Phase-Frequency Detector. This block is responsible for resolving the differences in phase between the reference signal and the divided signal and output an error signal whose pulse width is proportional to this error.

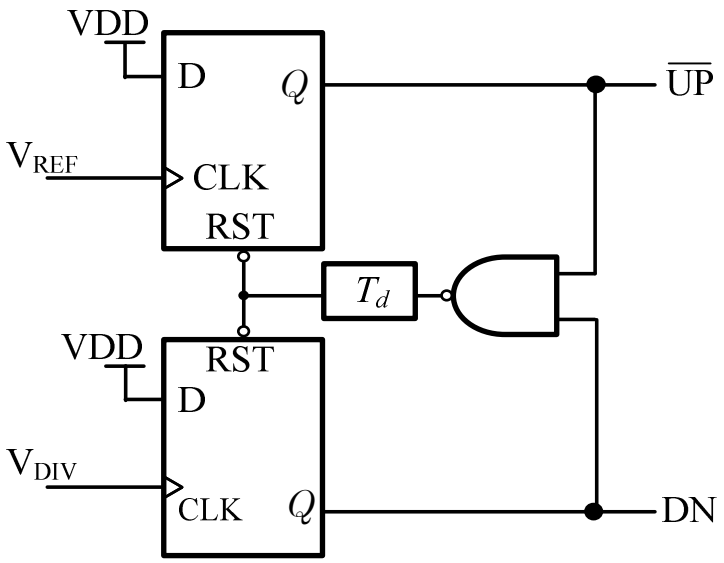


Fig. 59 Block diagram of the Phase-Frequency Detector (PFD)

The PFD shown in Fig. 59 is called a tri-state PFD and can resolve phase and frequency errors. It consists of two D-flip flops whose D-inputs are connected to VDD. The reference signal and the divided signal act as the clock to each flip flop. If the reference signal comes first it activates the UP signal signaling that the control voltage of the VCO should increase because its output signal is slower than the reference and needs to be sped up. Then the rising edge of the divide signal arrives which activate the DN (down) signal. When both signals are active, the reset path is enabled and immediately both flip flops are cleared to the PFD will then wait for the next edge to do

another comparison. The opposite happens if the divided signal arrives first. The DN (down) signal is then activated signaling that the control voltage of the VCO should be decreased to slow down the VCO.

If the rising edges of the two signals are aligned but their time periods are not equal, they will become consequently loose this alignment in the next comparison cycle pushing the VCO to correct its frequency. Once, the frequency is correct, then the phase will align after that reaching a complete lock.

The time delay in the feedback avoids the dead zone problem. It ensures that at lock the UP and DN signals stay active for enough time (before they get cleared) to activate the charge pump. This avoids making the PLL work in open loop which degrades its in-band phase noise performance.

The UP and DN signals are applied to the Charge Pump. The charge pump converts the width of the time pulse to a voltage by injecting/sinking a proportional amount of current into the impedance of the loop filter. This increases or decreases the VCO control voltage as needed. A circuit diagram of the charge pump employed in our designs is shown in Fig. 60. Transistors MBP and MBN are current sources providing the charging and discharging currents of the charge pump. Transistor MP and MN act as switches to allow the currents to pass to the loop filter. The differential structure of the switching pairs prevents the current source from turning off and hence provide better current matching and hence, reference spur performance. The dummy transistors MPD and MND are employed to reduce the effect of clock feed-through and charge injection due to the switches MP and MN. Hence they are connected to opposite polarities of MN

and MP. This topology has only four transistors in the stack allowing for low voltage operation. In addition by minimizing the overdrive voltage of the current sources and high swing can be obtained at the output.

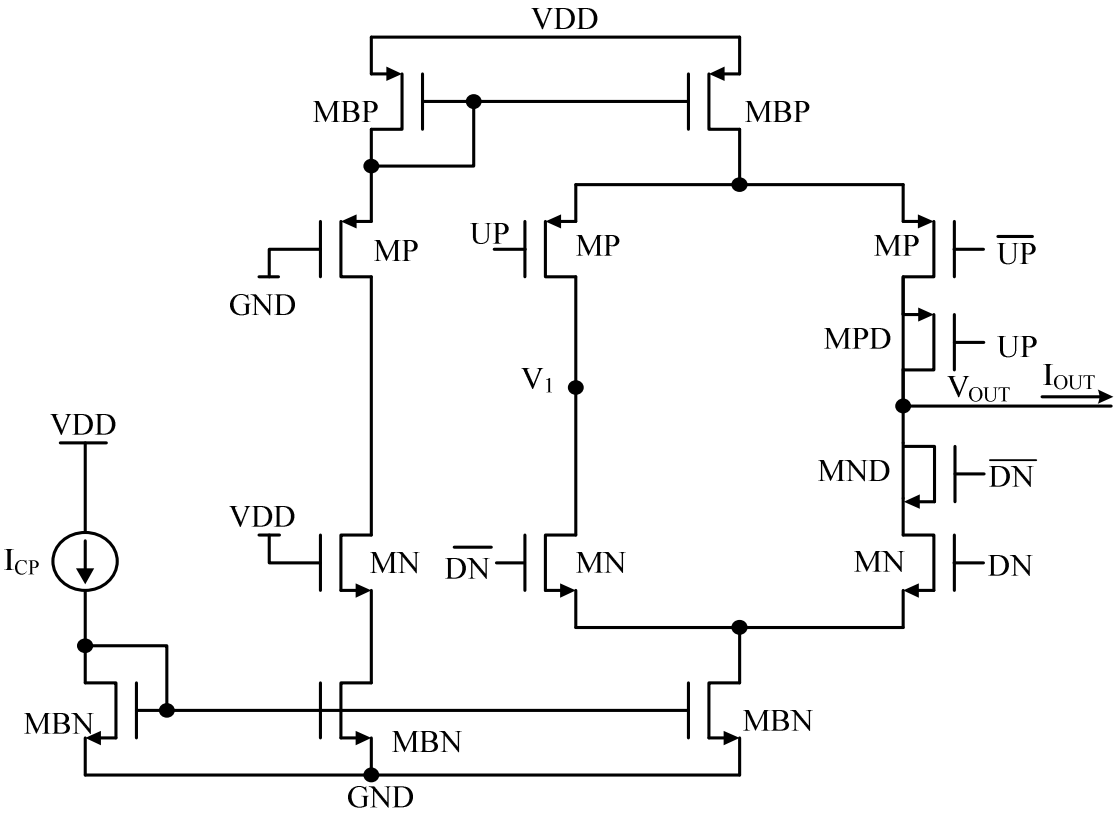


Fig. 60 Circuit diagram of the charge pump

One way to improve the reference spur suppression is to add a buffer between nodes V_1 and V_{OUT} as shown in Fig. 61 [74]. This buffer ensures that the voltage V_1 follows V_{OUT} when either the MP or MN of the branch connected to V_1 is off. This keeps

the voltage of the drain of the current sources constant during switching, hence again reducing the current mismatches and reducing the reference spur.

The charge pump injects a current proportional to the phase error signal between the reference and the divided signal into the loop filter. The transfer function of the PFD and charge pump combined can be given as,

$$\frac{I_{out}}{\Delta\phi_{in}} = \frac{I_{CP}}{2\pi} \tag{4.1}$$

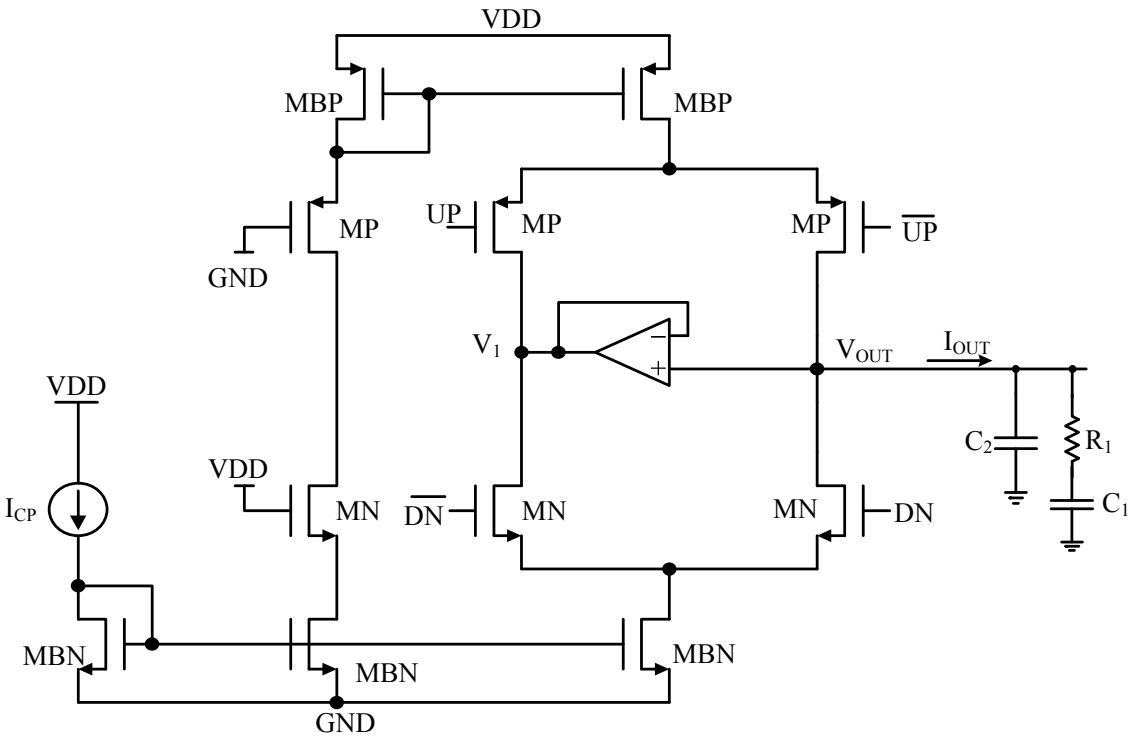


Fig. 61 Circuit diagram of the modified charge pump

The main function of this filter is to provide the DC component of this error signal. The VCO uses this voltage to correct its frequency. Hence, the phase-voltage transfer function of the VCO presents an integrator and is be given as,

$$\frac{\Delta\phi_{out}(s)}{V_{cntrl}(s)} = \frac{K_{vco}}{s} \tag{4.2}$$

The loop filter could be as simple as a single capacitor. However, in this case, the loop will contain two poles at Dc which makes the loop unstable. Hence, a zero is added by making the second integrator lossy; in other words adding a resistor in series with the capacitor (R_1 and C_1 in Fig. 61). The loop filter trans-impedance function is given by,

$$Z_{LF} = \frac{(1+sR_1C_1)}{sC_1} \tag{4.3}$$

One of the main problems associated with integer-*N* PLLs is the reference spur problem. During the locked state the amount of current injected by the UP pulse should exactly match that injected by the DN pulse. However, mismatches in the values of the up and down currents as well as mismatches in the timing of the UP and DN pulses can lead to a net current being injected into the loop filter. This drives the PLL away from the locked state. Hence, the PLL tries to correct this error by skewing the UP and DN pulses (i.e. depending on the polarity of the mismatch one of the UP or DN pulse becomes larger than the other). This leads to zero net current injected into the loop filter. However, the skewed UP and DN pulses leads to a ripple on the control voltage with as shown in Fig. 62 . This ripple is periodic with a period T_{ref}. which can be decomposed into its Fourier series components given as,

$$V_{cntrl}(t) = \sum_{i=1}^{n} a_i \cos\left(i\omega_{ref}t\right) \tag{4.4}$$

The DC value of the control voltage determines the oscillation frequency. The ripple on the control voltage modulates the oscillation frequency resulting in the appearance of spurious tones at the reference frequency. The output voltage of the oscillator is given as,

$$V_{out} = V_0 \cos\left(\omega_o t + K_{vco}\int_0^t v_{cntrl}(t)\,dt\right) \tag{4.5}$$

Substituting $v_{cntrl}(t) = a_1 \cos(\omega_{ref} t)$

$$\begin{aligned} V_{out} &= V_0 \cos\left(\omega_o t + K_{vco}\int_0^t a_1 \cos(\omega_{ref} t)\,dt\right) \\ &= V_0 \cos\left(\omega_o t + \frac{a_1 K_{vco}}{\omega_{ref}} \sin(\omega_{ref} t)\right) \end{aligned} \tag{4.6}$$

For $\omega_{ref} << \omega_o$, the narrowband FM approximation can be used, thus,

$$\begin{aligned} V_{out} &\approx V_0 \cos(\omega_o t) - V_0 \frac{a_1 K_{vco}}{\omega_{ref}} \sin(\omega_{ref} t)\sin(\omega_o t) \\ &\approx V_0 \cos(\omega_o t) - V_0 \frac{a_1 K_{vco}}{2\omega_{ref}} \cos(\omega_o - \omega_{ref})t + V \frac{a_1 K_{vco}}{2\omega_{ref}} \cos(\omega_o + \omega_{ref})t \end{aligned} \tag{4.7}$$

Hence, in the frequency domain, two tones appear around the main oscillation tone at offsets of ω_{ref} and are called the reference spurs. The amplitudes of these tones relative to the oscillator's output amplitude is given by,

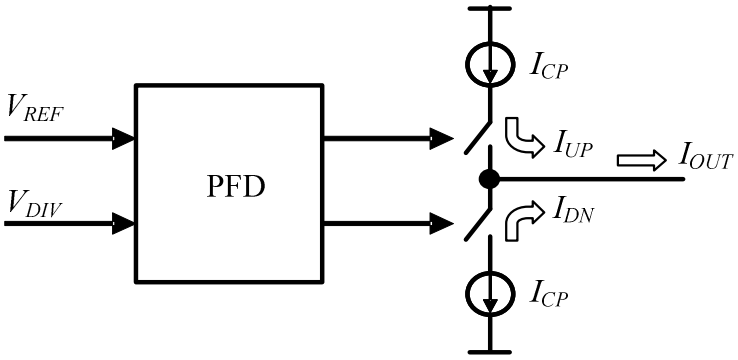
$$A_{spur} = \frac{a_1 K_{vco}}{2\omega_{ref}}\ (dBc) \tag{4.8}$$

Since, a_1 is related to the fundamental component of the charge pump current and the loop filter impedance at ω_{ref}, the relative spur can be re-written as,

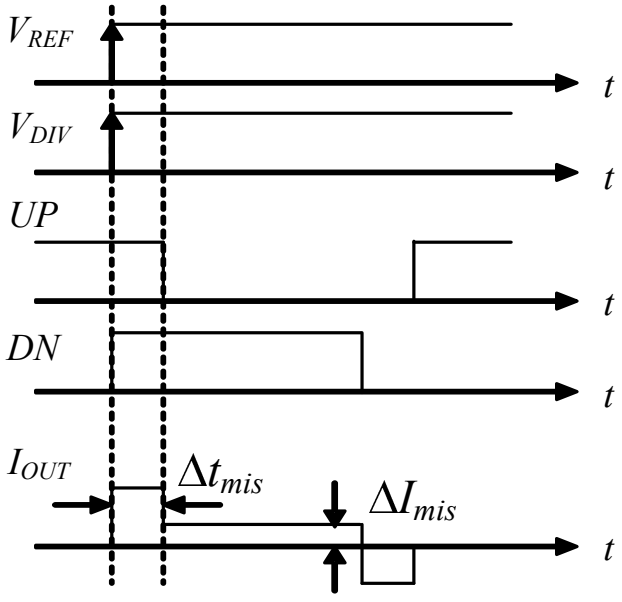
$$A_{spur} = i_{CP} R . \frac{K_{vco}}{2\omega_{ref}} \frac{\omega_p}{\omega_{ref}} = i_{CP} R . \frac{K_{vco}}{2\omega_{ref}} . \frac{\omega_{GBW}}{\omega_{ref}} . \frac{\omega_p}{\omega_{GBW}} \tag{4.9}$$

which in dB becomes,

$$A_{spur}\Big|_{dBc} = 20\log\left(i_{CP}R\right) + 20\log\left(\frac{\omega_p}{\omega_{GBW}}\right) + 20\log\left(\frac{K_{vco}}{2\omega_{ref}}\right) + 20\log\left(\frac{\omega_{GBW}}{\omega_{ref}}\right) \qquad (4.10)$$



(a)



(b)

Fig. 62 (a) Illustration of the UP and DN currents generated by the charge pump (b) Timing diagram showing the mismatches in the time and current of the UP and DN currents generated by the charge pump

These reference spurs are undesirable as will be described below. However, we should note that the above analysis applies to any noise disturbances originating on the control voltage or even from within the oscillator itself. Noise signals appear at all frequencies and are treated in a similar fashion, resulting in sidebands around the oscillation tone. However, these phase noise sidebands are continuous with frequency and their amplitude fall as their offset frequency increases. The phase noise component and the spur tone located around the reference channel, both, have undesirable effects. This is because the reference frequency usually coincides with the adjacent channel in wireless receivers. This channel might be transmitting data concurrently with the desired channel and at even higher power levels. For the setting shown in Fig. 63 , the local oscillator (LO) signal will down convert the desired channel to the intermediate frequency (IF). In addition the component of the phase noise at a frequency offset of BW (signal bandwidth) from the LO signal as well as the reference spur at the same offset frequency will mix with the adjacent channel (which is higher than the desired channel) and down convert to the IF frequency. These components will corrupt the desired signal. Hence, from a system design point of view, we want to maintain a certain SNR_{min} when these two components exist simultaneously with the minimum detectable signal. We can write,

$$(P_{SIG} + P_{LO}) - (P_{INT} + P_{SPUR}) > SNR + 3dB \tag{4.11}$$

$$(P_{SIG} + P_{LO}) - (P_{INT} + P_{NOISE} + 10\log(BW)) > SNR + 3dB \tag{4.12}$$

where the 3dB is added to account for the two components existing concurrently. From which we can find the spur suppression A_{SPUR} requirement and the phase noise PN should be,

$$A_{spur} = P_{LO} - P_{SPUR} \ (dBc) \tag{4.13}$$

$$PN = P_{LO} - P_{NOISE} \ \ (dBc/Hz) \tag{4.14}$$

A simple solution that alleviates part of the effect of the reference spur is to add the capacitor C_2 shown in Fig. 58 to filter out the high frequency ripples at ω_{ref}. We should also note that good layout techniques for the charge pump will minimize the current mismatches and hence the reference spurs. We have to ensure matching of the switching pairs (MP and MN) as well as the current sources (MBP and MBN). More discussion about solutions to this problem will be discussed in the coming sections.

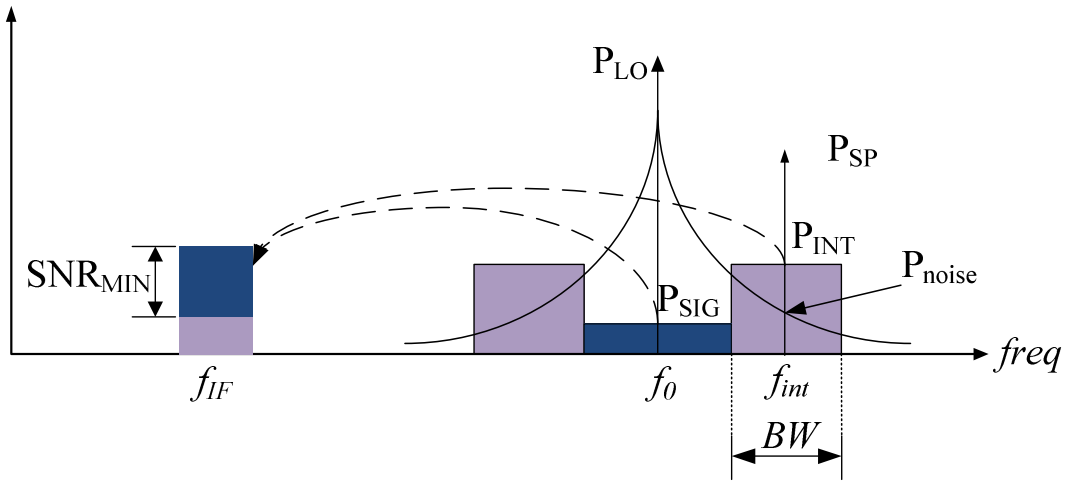


Fig. 63 Power spectrum showing the effect of the phase noise and the reference spur of the PLL on the system SNR

In the proposed PLLs, an LC tank based oscillator is used. This oscillator consists of an inductor and capacitor to form the tuned circuit which determines the frequency of the oscillation. However, since in practice, these inductors and capacitors have finite resistive part, i.e. finite quality factor, any oscillation will decay with time. Hence, a negative resistance is needed to cancel out these losses and sustain the oscillations. This is implemented using the cross-coupled differential pair (a positive feedback circuit). In out implementation we use the complementary CMOS architecture with cross coupled NMOS and PMOS pairs. This allows for more voltage swing, for the same current consumption, and also provides a more symmetric waveform which reduces the close-in phase noise [58]. The implemented circuit is shown in Fig. 64. Tuning is done using coarse steps and fine ones. The coarse steps are achieved using a bank of varactors which are switched between their on and off states resulting in a discrete frequency jump. A bank of binary weighted varactors is used to cover a range of $\pm$15% to account for any process and temperature variations in the tank's center frequency. The fine tuning can be achieved by continuously tuning the control voltage of the varactor. For high K_{VCO} a MOS capacitor can be used which can achieve values from 100-200MHz/V while for lower K_{VCO} we can use junction varactors which can achieve values around 10-50MHz/V.

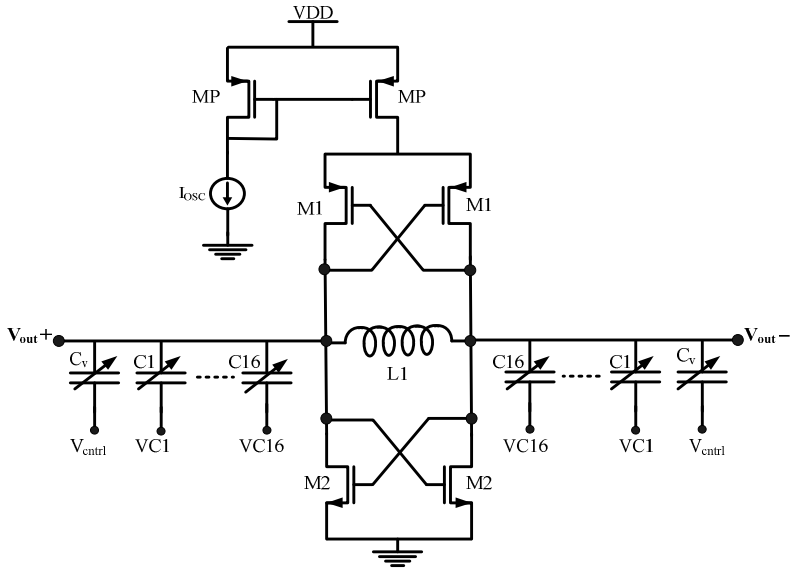


Fig. 64 Complementary CMOS LC VCO

After detailing each block, we can now carry out the loop parameter design. It was designed as a conventional type-II third-order PLL as shown in Fig. 58 since the proposed techniques to enhance a suppression of reference spurs can be added without modifying the existing conventional design. The loop parameters design procedure is as follows [75]:

(1) Determine the reference frequency. For an integer *N* PLL the reference frequency is equal to the channel spacing dictated by the wireless standard as this is the minimum frequency resolution which can be achieved.

(2) Determine the loop bandwidth frequency (the crossover frequency, ω_c). The maximum allowed ω_c is ten times lower than f_{REF} according to Gardner's stability limit such that the linearized continuous time model holds [12]. A wider bandwidth leads to faster settling while lower bandwidth suppresses the reference spurs.

(3) Choose the damping factor (ζ). Normally a critically damped loop (ζ=1) works best for the optimal settling time and loop stability. In this work, the second-order approximation (ζ) is used as the damping factor.

(4) The non-zero pole frequency (ω_p) and the zero frequency (ω_z) are placed at 4 and 1/4 times resulting the placement ratio of $\alpha^2 = 4$. These conditions yield a phase margin of 62º. Note that the third-order loop transfer function will slightly over-damped with a pseudo-damping factor of ζ'=1.5.

(5) The natural frequency ω_n is given as $\omega_n = \omega_c / (2\zeta)$

(6) The averaged dividing ratio N can be calculated from the median of output frequency range divided by the reference frequency. $N = (f_{max} + f_{min}) / (2 \times f_{REF}) = (5740 + 5830) / 5 = 1157$. The phase margin and the settling time depend on N and hence we should make sure that the different values of N satisfy the required specs. Normally, in narrow band application where the variation of N is not large, the averaged dividing ratio is a good approximation.

(7) The loop filter components can be calculated as $C_1 = (I_{CP}K_{VCO}) / (2\pi N\omega_n^2)$, $R_1 = 1 / (\omega_{z1})$ and $C_2 = 1 / (\omega_p C_1)$, given the charge pump current and VCO gain are known.

(8) The settling time can be estimated from ζ and ω_n using the second-order closed-loop transfer function. The second-order loop is used as it provides simple solutions. Knowing the frequency step Δf and the settling accuracy in ppm, in a critically-damped system, the settling time is $t_s \approx ln(\Delta f / \delta f_0) / (\zeta \alpha\omega_n)$. Since the calculated settling time is estimated from the second-order loop system, the actual settling time will be longer.

4.3 High Performance PLL Design Examples

In this section we present two design examples for high performance PLLs. The first PLL uses a new technique to lower reference spurs without sacrificing other loop parameters. The second design presents a very low power PLL designed for medical applications.

4.3.1 Low reference spur PLL

4.3.1.1 Introduction

High performance frequency synthesizers often require fast settling times (to switch between channels) and low reference spurs (as dictated by wireless standards) simultaneously. However, there is always a trade-off between these two parameters. The magnitude of the spurs depends on the VCO gain, the amount of filtering, the value of the reference frequency as shown in (4.10) as well as the design of the PFD and CP. Lower reference spur levels can be achieved by utilizing higher order loop filters and, [76] and [77] have demonstrated a reasonable spur level as below -65 dBc with third-order loop filters. However, higher order loop filters decrease a phase margin of the loop making the system unstable and high overshoot voltages. A smaller loop bandwidth and VCO gain also help to reduce spurs at the cost of the increased settling time and reduced frequency range, respectively [78]. Dual loop architectures have been proposed to overcome the tradeoff between the settling time and spur reduction [79]. The main drawbacks in using this approach are the complicated system design and the instability that may occur due to the change of the loop dynamics. Another method is to move the reference spur from ω_{ref} to $N\omega_{ref}$ through the use of N-path delay elements, so the spur is

shifted to a higher frequency [80] . This approach requires the use of the exact delay elements, which are practically difficult to implement. Also randomizing the delay shift has the effect of spreading the spur into a Sinc function, which does not provide enough spur suppression [80].

In this work, a spur reduction technique is used to disengage the trade-off between the settling time and spur suppression, hence giving the designer enough flexibility to optimize the design of the PLL to achieve the settling time and spur suppression requirements.

4.3.1.2 PLL Specifications

In this work we adopted the frequency plan of IEEE 802.16 standard (WiMax) [81]. A part of the frequency band in WiMax standard is located at the upper Unlicensed National Information Infrastructure (U-NII) band when the regulatory domain is the USA. The output frequency range of the frequency synthesizer was determined as 5740 MHz ~ 5830 MHz with 5 MHz of a channel space in order to cover both 10 MHz and 20 MHz channelizations. Since, this is a proof of concept prototype for the spur reduction techniques, other performance specifications are not considered. Table 7 summarizes the designed loop parameters using the previously outlined methodology. Fig. 65 presents the Bode plot of the open loop transfer function while Fig. 66 shows the step response of the closed loop transfer function.

Table 7 Summarized table for the designed loop parameters

Parameter	Designed value
$f_{out,min}$, $f_{out,max}$	5740 MHz, 5830 MHz
f_{REF}	5 MHz
N	1157
ζ	1
ω_c, ω_n	$2\pi \times 100$ KHz, $2\pi \times 50$ KHz
ω_p, ω_z	$2\pi \times 400$ KHz, $2\pi \times 25$ KHz
R_1	50 KΩ
C_1	128 pF
C_2	8 pF
Phase margin	62 °
K_{VCO}	$2\pi \times 240$ MHz/V
I_{CP}	60 μA
Settling time	24.1 μs

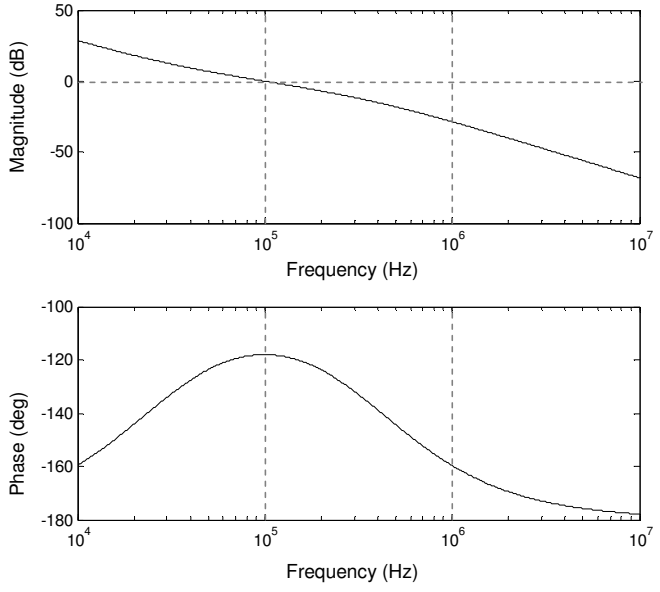


Fig. 65 Magnitude and phase response of the open-loop transfer function

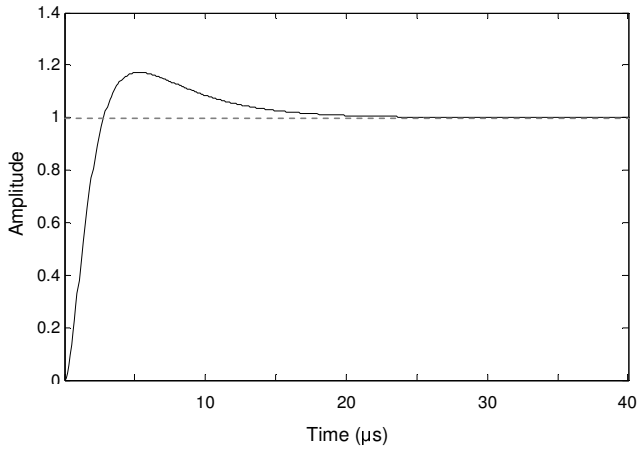


Fig. 66 Step response of the closed-loop transfer function

4.3.1.3 Proposed Adaptive Low Pass Filtering Technique

The goal of this work is to suppress the reference spurs without degrading the settling time of the PLL. Adding any additional low pass filtering poles after the loop filter will degrade the phase margin and result in ringing in the step response of the PLL, leading to a longer settling time. However, we should notice that the phase margin affects the settling time only during the transient part of the step response. Hence, we propose to add the low pass filtering poles only after the transient part of the step response is over, i.e. the PLL has approached the locking condition.

Fig. 67 shows the additional two poles added after the loop filter. A buffer is placed after each pole so we can accurately place the poles. These poles are placed at 1MHz which one decade higher than the loop bandwidth (100KHz) so their effect on the phase margin is minimal. At the same time they are 5 times lower than the reference spur at 5MHz. With the additional two poles, the phase margin is decreased from 62º to 51º

while the suppression of reference spurs is improved by 28 dB over the conventional architecture.

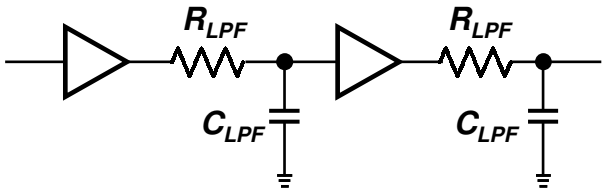


Fig. 67 The additional low-pass filtering poles

The architecture of the proposed PLL is shown in Fig. 68. The two buffered low pass poles are inserted between the loop filter and the VCO. The capacitors of these poles are connected to the control voltage node through switches. A lock detector compares the reference and divided signals and determines that the PLL is locked when these two signals remain phase locked (within a certain phase error) for a number of consecutive reference cycles. During the transient state and before locking the capacitors are disconnected and the loop acts as a conventional third order loop. Once, lock state is achieved the LCK signal is activated which turns on the switches to connect the capacitors and hence introducing the filtering function to suppress the reference spurs. Another buffer is used to make the capacitors' voltage follow the control voltage value such that when they are connected no charge sharing happens (which if it existed could take the loop out of lock). We should also note that the clock feed-through and charge injection resulting from turning on the switches will result in a small error on the control voltage which could slightly increase the settling time.

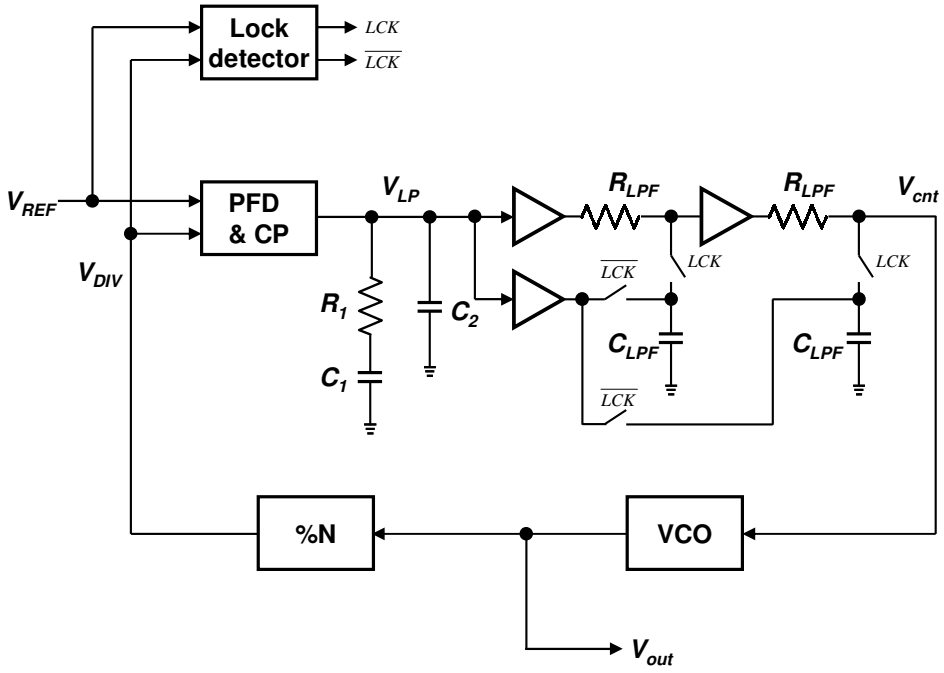


Fig. 68 Architecture of the proposed low spur PLL

4.3.1.4 Measurement Results

The proposed PLL is designed and fabricated in 0.13µm CMOS RF technology with 8 metal layers provided by UMC. The chip shown in Fig. 69 occupies a die area of 1.86 ×1.2 mm^2, and the active area is 0.34 mm^2. The designed circuit is encapsulated using QFN-56 open cavity package. It has 56 pins and a lead pitch is 0.5 mm and, a body size is 8 mm x 8 mm. A control circuit, shown in Fig. 70, is introduced within the design to enable testing the PLL in the conventional mode without introducing the poles and also in the proposed mode for the sake of comparison.

The measurement result reveal that the VCO frequency band is shifted down by 18 % compared to the post layout simulation. This is attributed to the underestimation of

the parasitic inductances as well as the capacitances in the simulation. The measured VCO free running frequency makes us adjust the reference frequency so that the PLL can lock. As a result, the reference frequency is set to 4.48 MHz instead of 5 MHz, and hence, we would expect a decrease in the improvement of spur suppression.

The VCO output spectrum is measured by the Agilent E4446 Power Spectrum Analyzer and plotted in Fig. 71. The carrier frequency is measured as 5.11 GHz and a reference spur is seen at 4.48 MHz offset frequency from the carrier frequency. The proposed frequency synthesizer improves the spur suppression by 20 dB over the conventional mode.

The step response of the PLL is measured using the oscilloscope, and is shown in Fig. 72. Before the *LCK* signal is activated, the proposed PLL exhibits the same behavior as the conventional one including the overshoot. When the *LCK* signal goes high and the additional poles are added the system becomes a higher rder on and the settling time increases. The settling time is measured as 40 μs and 44 μs in the conventional and proposed synthesizers, respectively. A slight change in the control voltage is observed during the transition of the LCK signal. As mentioned before, this is attributed to the clock feed-through and the charge injection of the switch transistors.

Fig. 73 illustrates the measured phase noise of the proposed and conventional settings of the PLL. The phase noise performance is nearly the same since the addition of the capacitors only filter out noise at offsets higher than the loop filter and at these offsets the noise of the VCO is dominant. Finally, the PLL consumes 9mW with a 1.3 V

power supply under the normal operation. Table 8 summarizes the performance metrics and compares it to state of the art work reported in literature.

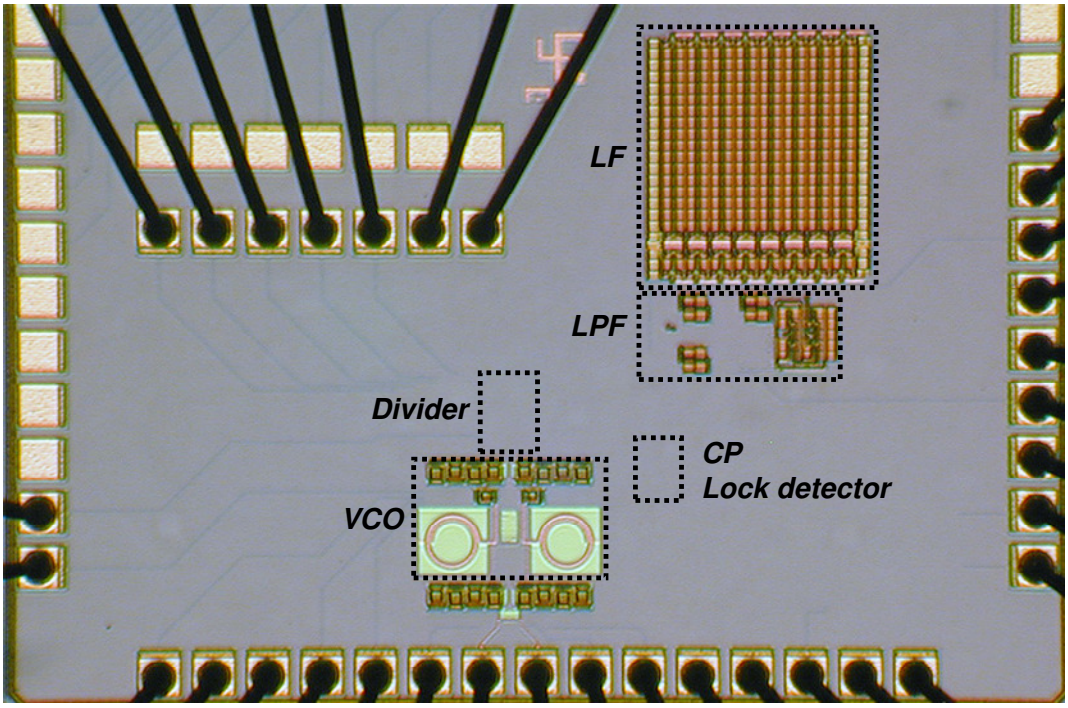
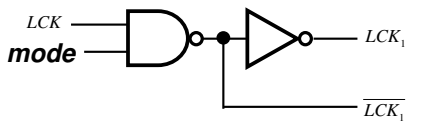


Fig. 69 Chip micro photograph



mode	LCK_1	Operation
0	0	Conventional
1	LCK	Proposed

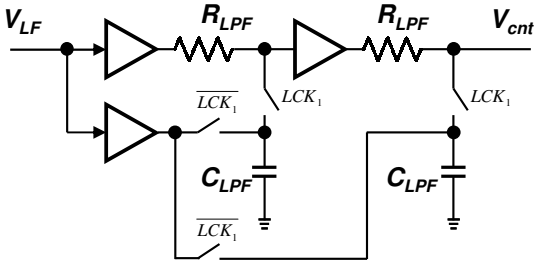
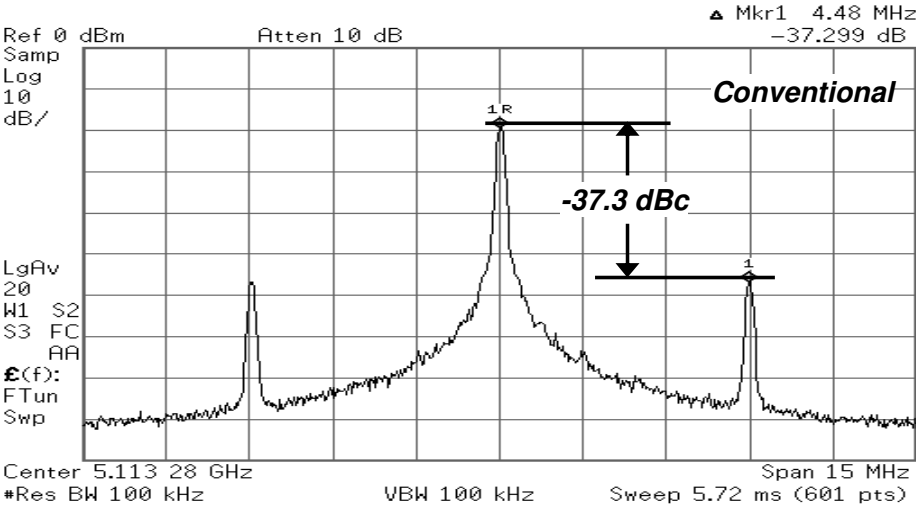
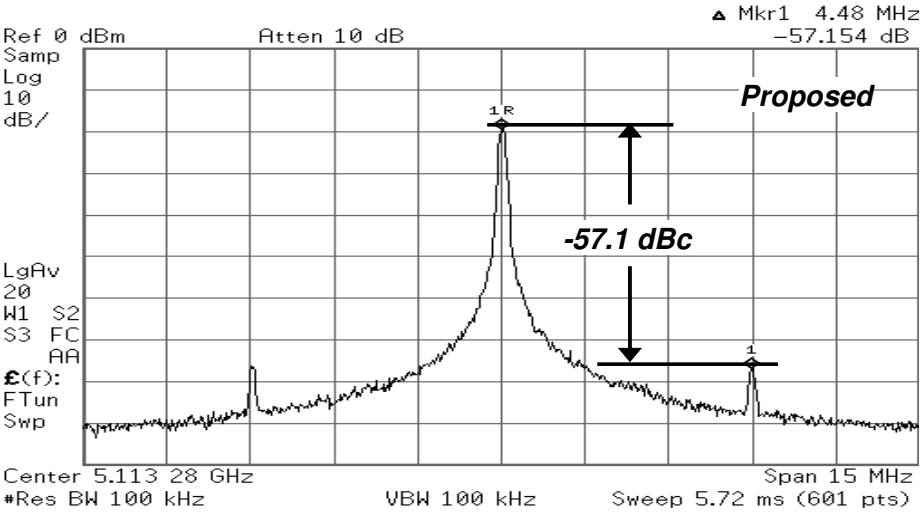


Fig. 70 Operation mode of a frequency synthesizer

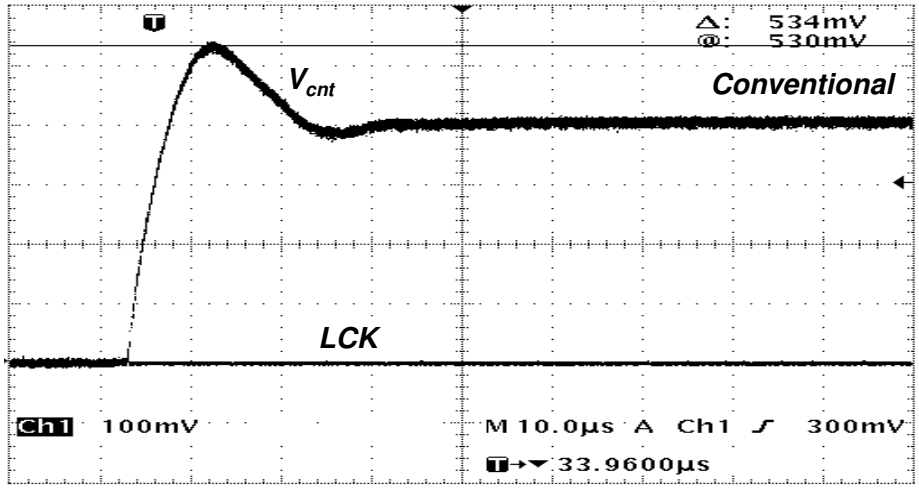


(a)

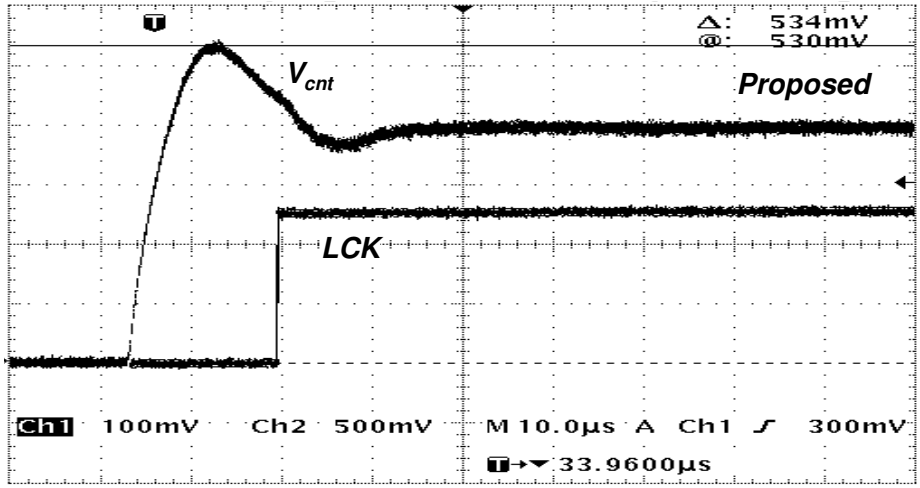


(b)

Fig. 71 Measured 5.11GHz frequency spectrum (a) Conventional (b) Proposed

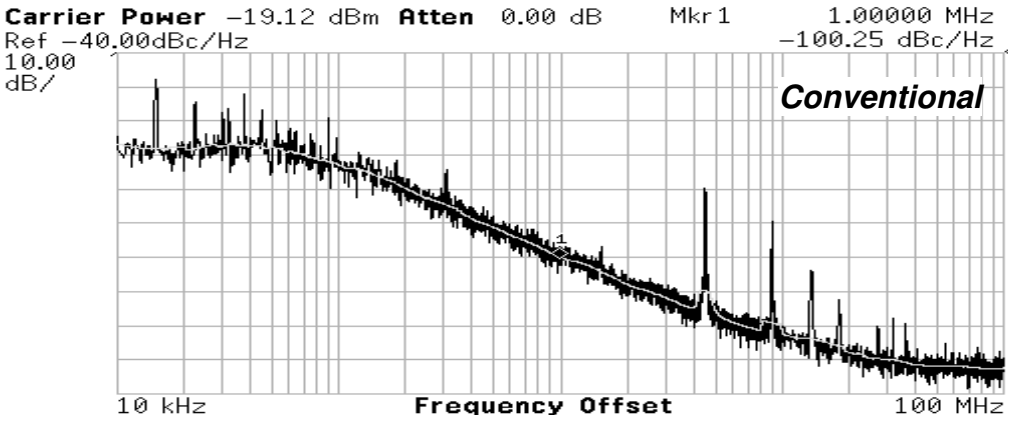


(a)

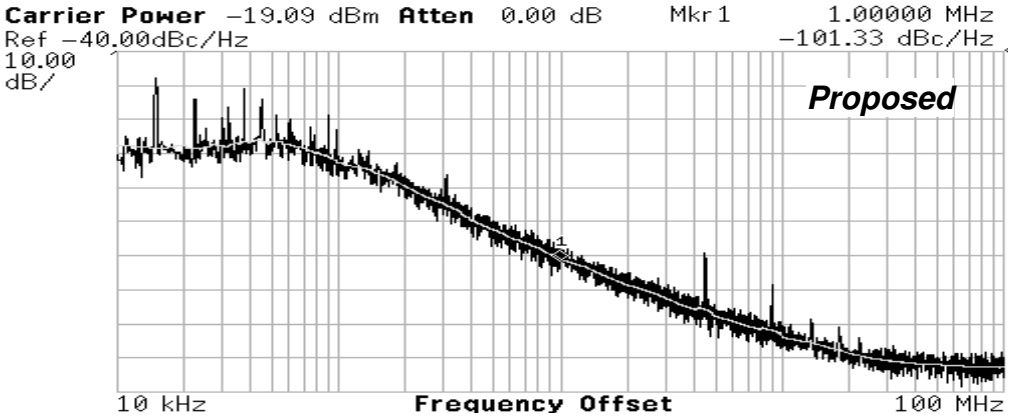


(b)

Fig. 72 Locking transient behavior (a) Conventional (b) Proposed



(a)



(b)

Fig. 73 Phase noise of the PLL in locked status (a) Conventional (b) Proposed

Table 8 Performance summary and comparison with other published solutions

	This Work (Proposed)	This Work (Conventional)	[80]	[82]	[83]	[77]
Frequency (GHz)	5.11 ~ 5.19	5.11 ~ 5.19	4.8	5.23 ~ 6.16	4.9 ~ 5.95	5.14 ~ 5.7
Phase noise (dBc/Hz)	-101 @1 MHz	-100 @1 MHz	-104 @1 MHz	-113 @1 MHz	-110 @1 MHz	-116 @1 MHz
Spur (dBc)	-57 @4.48 MHz	-37 @4.48 MHz	-55 @1 MHz	-74 @20 MHz	-66 @40 MHz	-70 @10 MHz
Settling time (μs)	44	40	--	76	--	100
Power (mW)	9	9	18	36	--	13.5
Process	0.13 μm CMOS	0.13 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.18 μm CMOS	0.25 μm CMOS

4.3.2 Very Low Power PLL For MICS

4.3.2.1 Introduction

The advances in the semiconductor area and especially CMOS circuits have enabled the development of numerous medical devices which can benefit a wide spectrum of patients worldwide. The low cost, small form factor and high volume fabrication of CMOS circuits will make medical treatment devices more ubiquitous and affordable to most patients, thus promising a better quality of life.

One of the new areas which are evolving in the field of medical devices is the use of medical implantable devices which employ CMOS circuits. Implantable devices have been used historically to carry out treatment roles such as pacemakers, implantable cardioverter/defibrillator, Neuro-stimulators, pain and suppression devices. Recently more functionality is becoming possible such as drug infusion and dispensing devices, implanted sensors, control of artificial organs and heart assisting devices.

Previously these devices were controlled using inductive telemetry which employed a coil within the device to transmit/receive the control and data signals. However, the connection had to be within very close proximity (<10cm), using frequencies less than 1MHz and data rates less than 50KHz. This made the implantable devices bulky and they had to be placed just underneath the skin.

The recent advances in wireless technologies and the low power operation of CMOS based transceivers has made researchers look into the possibility of implementing these devices using the CMOS technology. Concurrently, and due to the realization of the importance of RF/wirelessly operated implantable devices, the FCC

approved the Medical Implantable Communication Standard (MICS) in 1999 [84] . This standard allocates part of the spectrum to RF communications of implantable devices and allows the flexibility to design very low power transceivers. Since then this standard has gain worldwide acceptance and adoption with slight changes in frequency bands and companies such as Biotronik, Medtronic, Guidant and St. –Judes started releasing version of devices compliant with the MICS.

4.3.2.2 MICS Overview

The MICS allows the operation of implantable devices within the 402-405MHz frequency band. The reason of choosing this band is that the characteristics of the human body allows the transmission of the radio signals at these frequencies with minimal attenuation as shown in Fig. 74. In addition the only other standard using the same frequency range is the metrological weather balloons which would rarely interfere with the implanted devices. The frequency range is divided into 10 channels each with a bandwidth of 300KHz. The implantable devices should be able to communication with a base station that is located within 2m range. The maximum effective isotropic radiated power as dictated by the standard is 25mW. In addition, out-of-band emissions, as well as in-band emissions that are more than 150 kHz away from the intended center frequency, must be attenuated by at least 20 dB. The local oscillator/ frequency synthesizer of the implantable device must maintain a frequency stability of +/-100 ppm of the operating frequency.

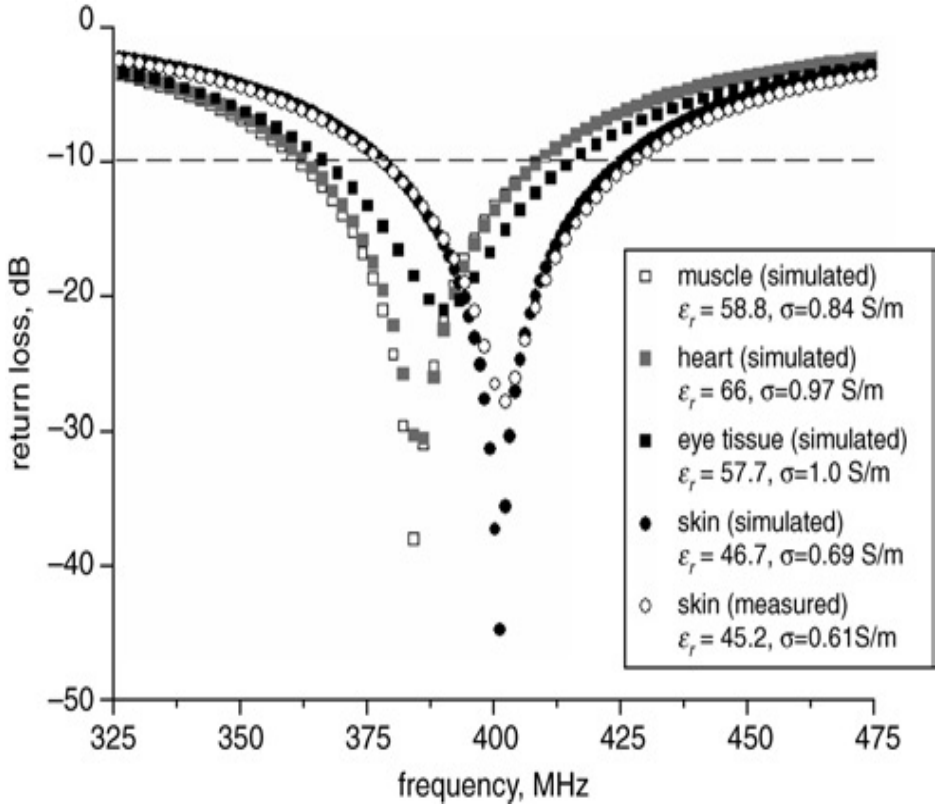


Fig. 74 Measured and simulated return loss for a stacked implantable planar antenna implanted into different biological tissue [85]

4.3.2.3 PLL Specifications

Now, using the information provided from the MICS we can now start finding the specifications of the frequency synthesizer or the PLL to be used for a MICS transceiver. First of all, we have to notice that the rate of information transmitted from the human body is very slow compared to the speed of nowadays circuits. Hence, the transceiver will be in a sleep/off more for most of the time. It will wake up periodically to transmit the available data and then turn off again to conserve power and minimize the time window of interference if any. Also, when awake, it will transmit power at

reasonably high data rates to minimize the ON time and hence the power consumption. The target is to have the transceiver operate with 1mW of power consumption from a 1V supply with a 1% duty cycle which means an effective power consumption of 10μW. As a rule of thumb frequency synthesizers usually consume around half the power of the transmitter or the receiver. Hence, we allocate 0.6mW of power consumption to the PLL. It should be noted that since the system will turn on and off periodically, the wake-up time of the synthesizer has to be minimized to conserve power. This is achieved by reducing the settling time of the PLL required to reach 100ppm of the oscillation frequency.

System design of the transceiver is carried out and a low-IF architecture is found to be the most suitable architecture to avoid the problems of flicker noise and DC offset associated with Zero-IF architectures and problems of poor sensitivity and selectivity associated with the super-regenerative architecture. The minimum detectable sensitivity is found to be -103dBm. An SNR of 14 dB is required at the output of the modulator to ensure a BER of 10^{-3}. The MICS also specifies that any channel should not transmit 10dB power more than the adjacent channel. So using this number, the sensitivity of the receiver and the SNR we can determine the requirement on the reference suppression and phase noise of the PLL output signal as mentioned before,

$$A_{spur} = P_{LO} - P_{SPUR} > 27\,dBc \tag{4.15}$$

$$PN = P_{LO} - P_{NOISE} > 81\,dBc/Hz \tag{4.16}$$

4.3.2.4 PLL Implementation

The MICS PLL system parameters are determined using the steps outlined before. Table 9 summarizes the value of these parameters. As it was mentioned before, the frequency synthesizer is the most critical block from power consumption point of view as it usually consumes around 50% of the total power of any transceiver. Fig. 75 shows the proposed breakdown of the power consumption of the transmitter and receiver for the MICS transceiver. Hence several considerations where applied to minimize power consumption. From a system level perspective, since, the transceiver operates in sleep mode most of the time and is only awake a small percentage of the time, minimizing this waking time is crucial in limiting the power consumption. This is achieved by minimizing the settling time of the synthesizer through increasing the loop bandwidth of the PLL as much as possible without compromising the stability of the loop. Fig. 76 shows the Bode plot of the open loop transfer function illustrating a loop bandwidth of 20KHz while Fig. 77 show the closed loop step response showing the settling behavior of the PLL loop.

On the circuit level, a 1V supply is used for all the blocks to minimize the power consumption. Also, a complementary LC oscillator structure as shown in Fig. 64 is adopted. It is chosen to operate at 1.6GHz which is 4 times the required frequency due to several advantages. First, operating at a higher frequency allows the integration of the tank inductor on chip, hence reducing the off chip components which is a big advantage in the area of implantable devices. Second the LC VCO provides a phase noise and power consumption performance superior to that of a ring oscillator operating directly at

the required frequency (~400 MHz). Since dividers were used to divide down the frequency, the in-phase and quadrature phase LO signals were readily available after a divide-by-two circuit. The low voltage low spur charge pump presented in Fig. 61 is used. In addition, static CMOS logic circuits are used in the divider and PFD to take advantage of the low frequency operation for reducing the power consumption.

Table 9 MICS PLL system parameters

Parameter	Designed value
$F_{OUT,MIN}$, $F_{OUT,MAX}$	401.4 MHz, 404.7 MHz
F_{REF}	300 KHz
N	1338 – 1349
ζ	1
ω_c, ω_n	$2\pi \times 20$ KHz, $2\pi \times 10$ KHz
ω_p, ω_z	$2\pi \times 80$ KHz, $2\pi \times 5$ KHz
R_1	622 KΩ
C_1	51 pF
C_2	3.2 pF
Phase margin	61.9 °
K_{VCO}	$2\pi \times 27$ MHz/V at 1.6GHz
I_{CP}	30 μA
Settling time	120 μs

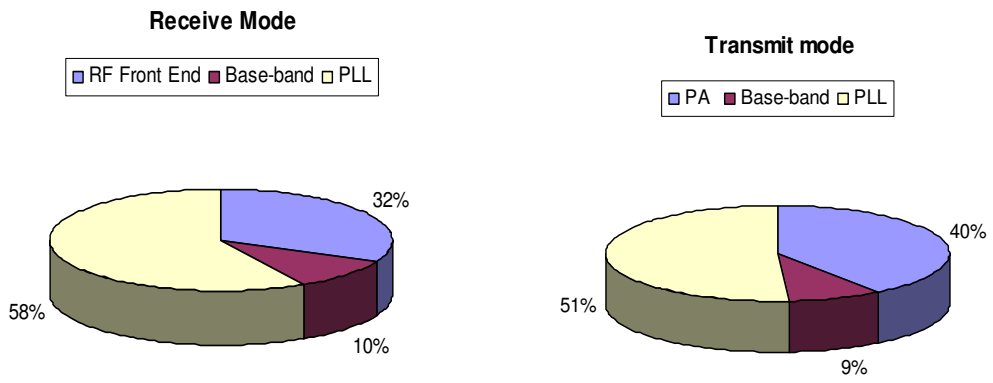


Fig. 75 Break down of power consumption of different blocks in the transmitter and receiver

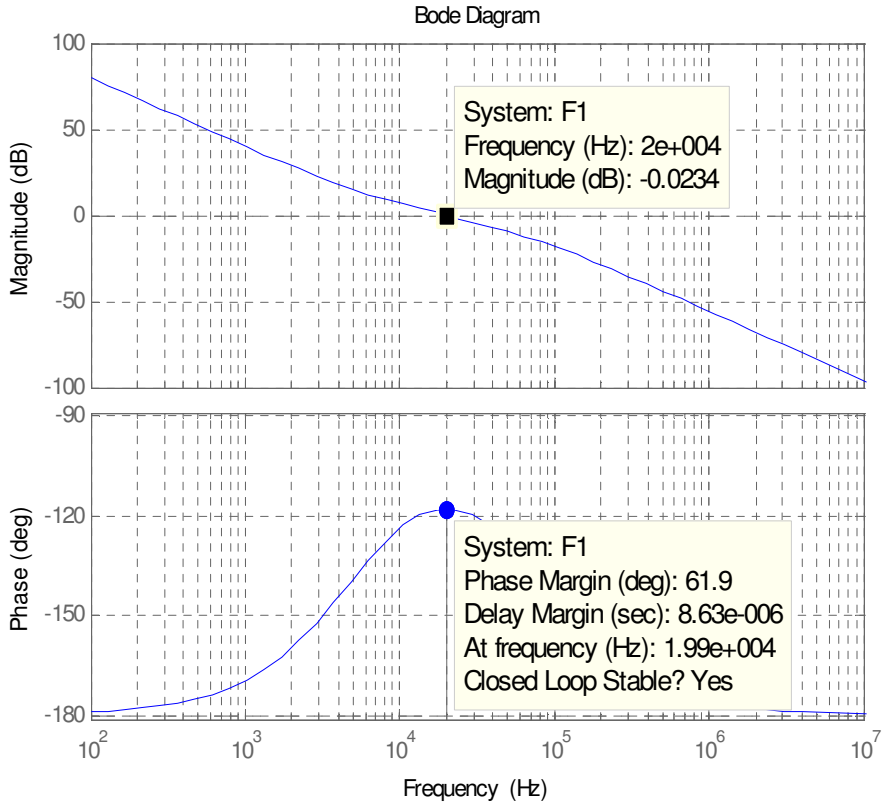


Fig. 76 Open loop transfer function

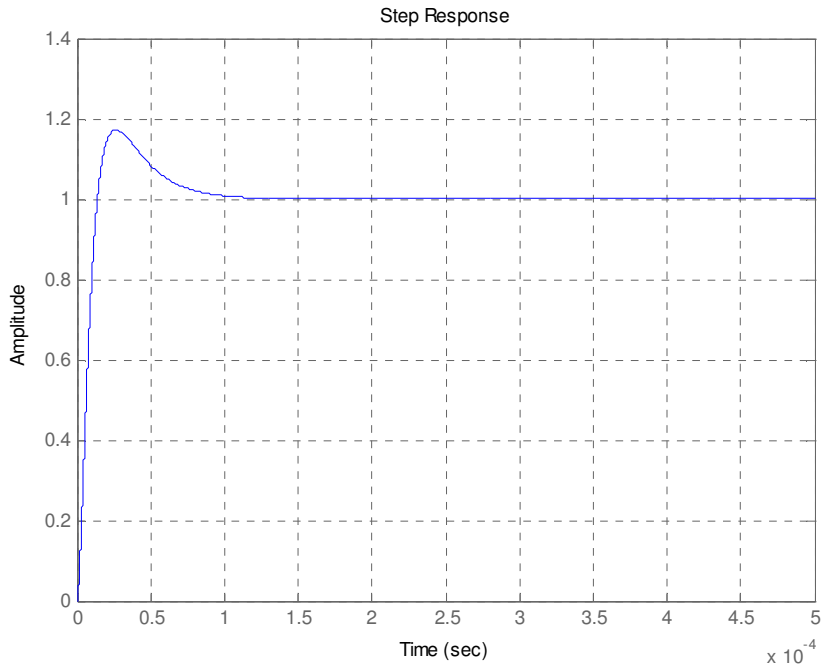


Fig. 77 Closed loop step response

4.3.2.5 Simulation Results

The MICS PLL is designed and simulated in 0.13µm RF CMOS technology. The PLL occupies an area of 1.375mm^2 including the pad area. A power supply of 1V is used and the total power consumption of the PLL is 600µW of which the VCO consumes 550µW. The output swing of the VCO operating at 1.6GHz is presented in Fig. 78 showing a peak to peak swing of around 450mV. This signal then gets divided by four to reach the 400MHz band. The divider is a static CMOS divider and hence the output signal is rail to rail. Fig. 79 illustrates the output of the divide-by-four circuit showing the in-phase and quadrature phase outputs of the divider. The I and Q phases

are needed for the operation of the image reject mixer for the Low-IF receiver. The tuning curve of the VCO is presented in Fig. 80 showing a K_{VCO} of 6.6MHz for the VCO and the divider circuits combined. The phase noise of the VCO, at 1.6GHz, is -107.37 dBc/Hz at an offset frequency of 300.7 KHz as shown in Fig. 81. The VCO is also coarsely tuned by a bank of discretely tuned varactors to cover a range of $\pm$ 15% of the oscillation frequency to account for any process or temperature variations. Fig. 82 and Fig. 83 show the phase noise of the VCO and the divider circuits combined as well as their power dissipation, respectively. The simulated step response of the PLL system for worst case switching (when switching from the first channel to the last and vice versa) is shown in Fig. 84. Finally, the summary of the performance of the frequency synthesizer is presented in Table 10, indicating compliance with the MICS standard. Fig. 85 depicts the layout of the PLL system within the transmitter chip.

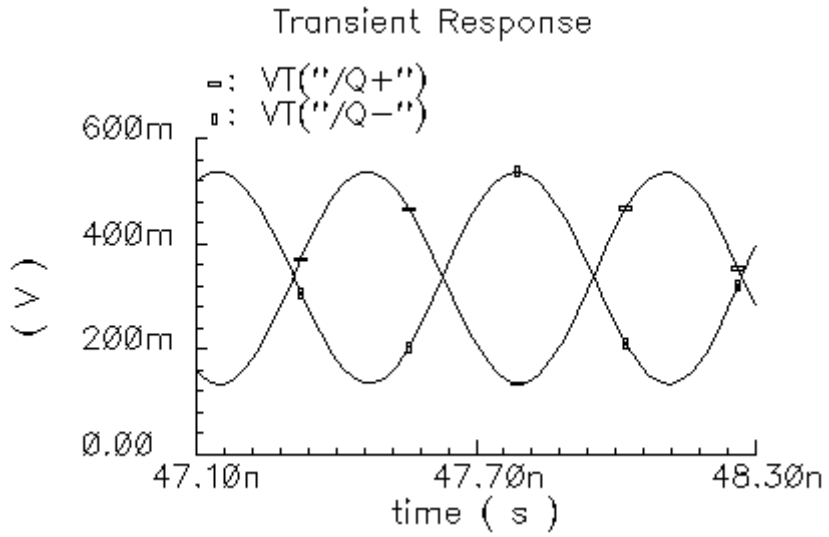


Fig. 78 Transient response of the VCO output

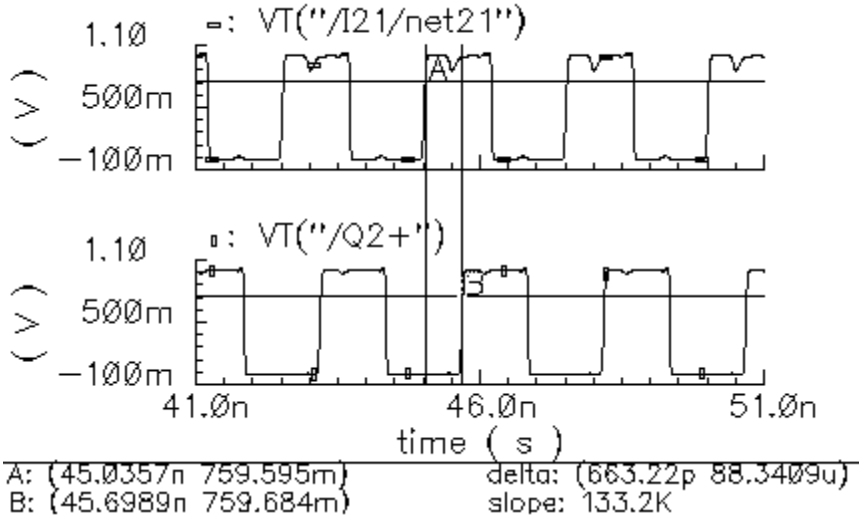


Fig. 79 Output signal of the divide-by-four circuit

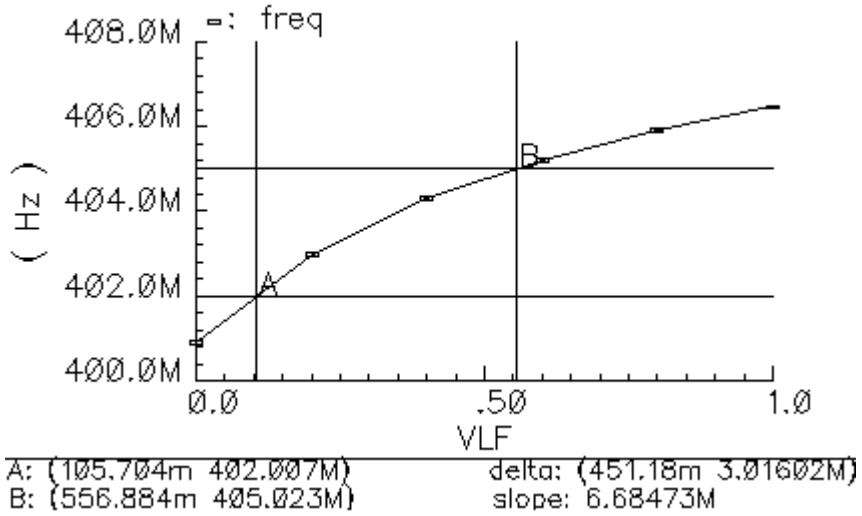


Fig. 80 Tuning curve of the oscillator output after division by four

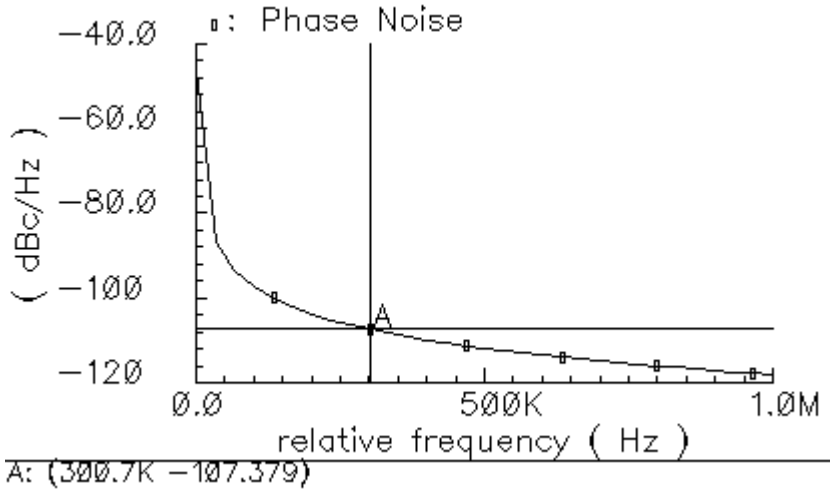


Fig. 81 Phase noise plot of the VCO output at 1.6GHz

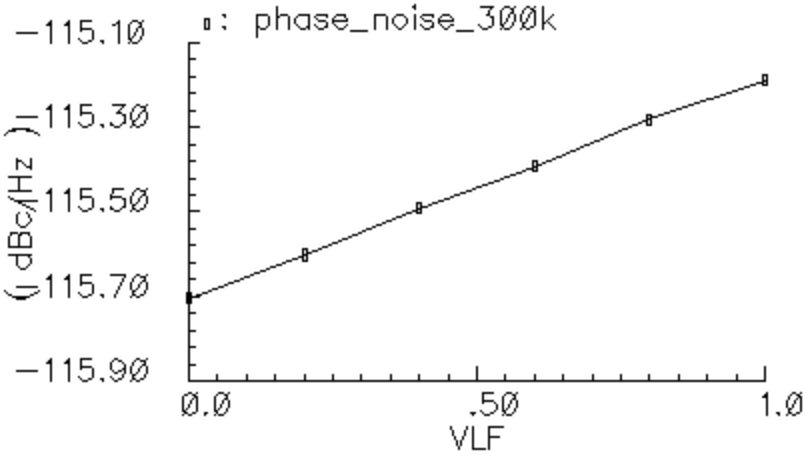


Fig. 82 Phase noise plot of the VCO versus the tuning voltage

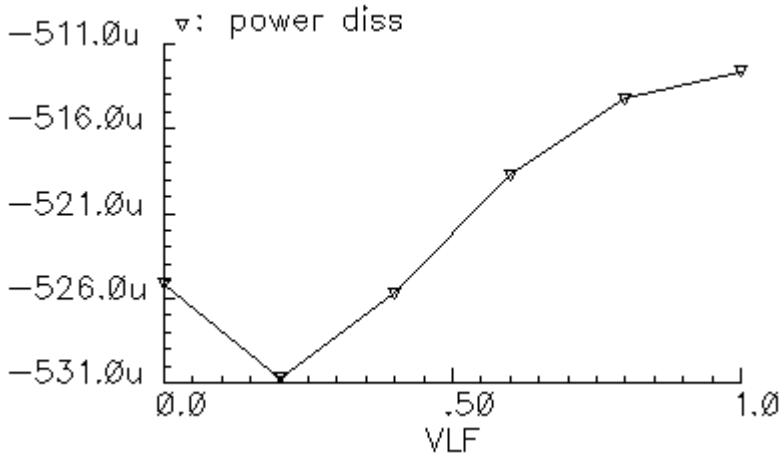


Fig. 83 Power dissipation of the oscillator and divider circuit versus the tuning voltage

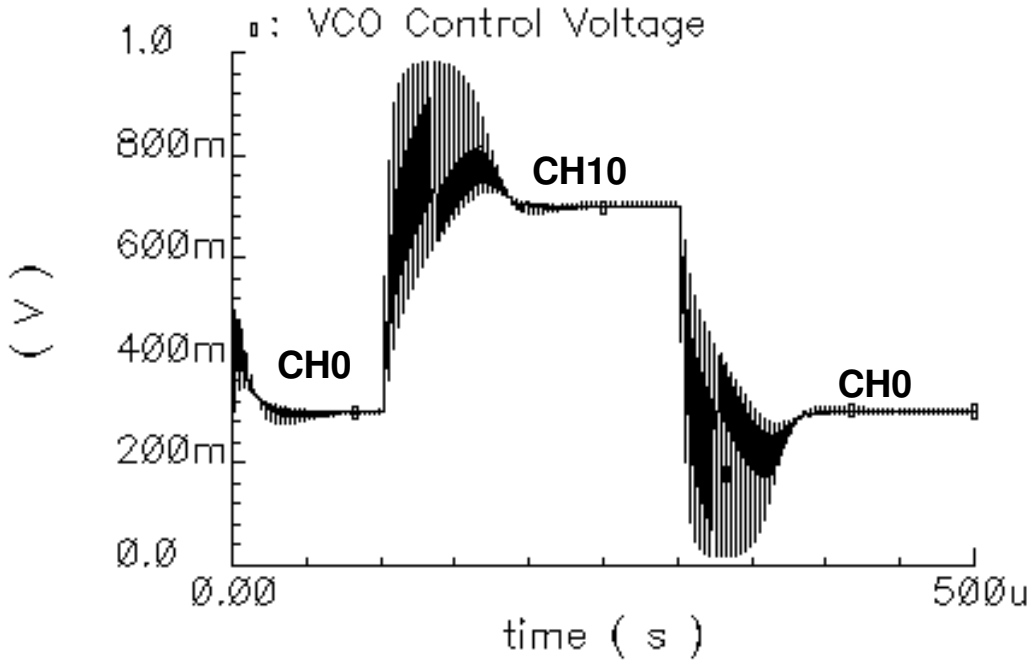


Fig. 84 Step response of the PLL system for maximum frequency jumps

Table 10 Simulated results of the MICS PLL system

Carrier Frequency	402.9-406.2 MHz
Reference Frequency	300 KHz
Phase noise at 300 KHz offset	-112 dBc/Hz
Reference spur level	-61 dBc
Settling time	150 μsec
Power Dissipation	600 μW
Supply Voltage	1.0 V
PLL Die Area	1.25 x 1.1 mm^2
Technology	0.13 μm CMOS

4.4 Conclusion

An adaptive low pass filtering technique to reduce the reference spurs for integer-*N* PLLs is proposed. An improvement of 20dB of the reference spur rejection was achieved yielding a spur suppression of -57 dBc. Another very low power PLL is also designed. Power is conserved by operating the voltage controlled oscillator at a higher frequency where the quality factor of the inductor is higher and then dividing down to the required frequency. Also, a wide loop bandwidth is used for fast settling of the PLL. The PLL outputs a frequency of 402-405 MHz and consumes a 750 μW of power from a 1V supply.

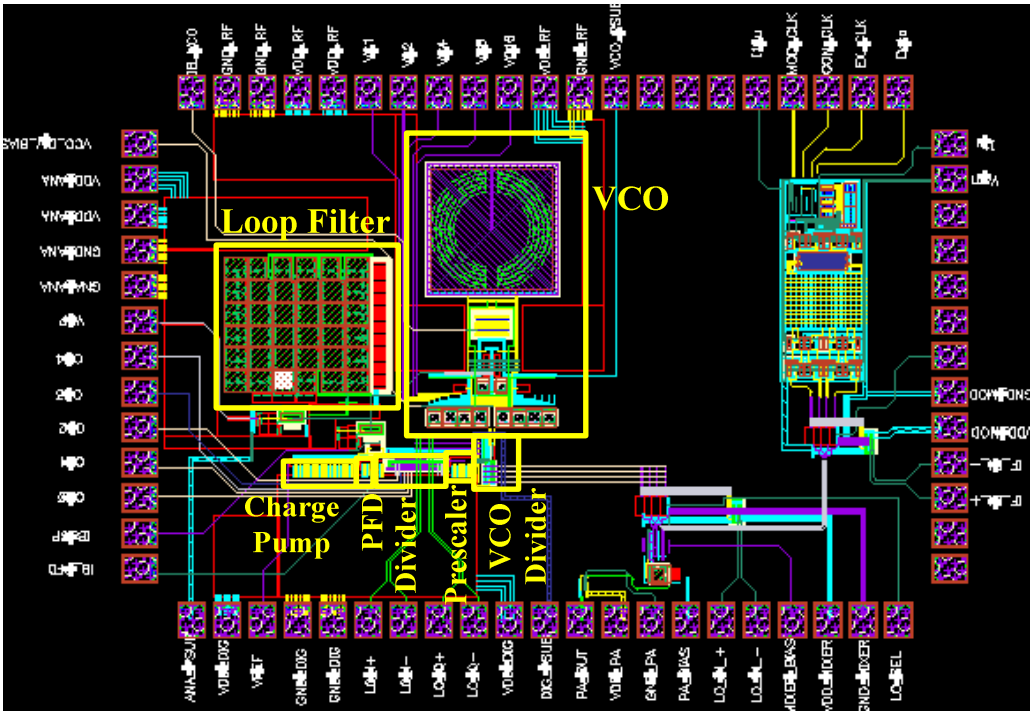


Fig. 85 Snap shot of the layout of the transmitter chip showing the PLL with its different components

CHAPTER V

CONCLUSION

In this dissertation, we discuss several aspects in designing high performance frequency synthesizers. We present several techniques and architectures to enhance the performance of frequency synthesizer and PLLs whether they employ inductors or are inductor-less.

A wideband mm-wave frequency synthesizer architecture is presented which uses multi-step multi-factor frequency multiplication. This architecture avoids the problems associated with injection-locked dividers. Measurement results demonstrated that a very wide tuning range of 5 to 32 GHz can be achieved, which is costly to implement using conventional techniques. Moreover the power consumption per octave resembles that of state-of-the art reports.

Next cyclic coupled ring oscillators are studied. Their oscillation modes and phase noise performance are analyzed using the generalized form of Adler's equation for injection locking. We prove that more than one stable mode exist in such oscillators but the RC pole allows only the one with the highest gain to survive. We also prove that an improvement in phase noise of $10log(M)$ is achieved for M coupled stages within a certain bandwidth which depends on the coupling strength. We then propose to combine N-Push operation with cyclic coupled ring oscillators. Two high-performance N-Push CCROs are presented and compared to their reference oscillator counterparts as well as

to state of the art oscillators. Improvement in oscillator performance metrics are achieved and confirmed by measured results.

Finally, an adaptive additional lowpass filtering technique to reduce the reference spurs for integer-N based frequency synthesizers is proposed. An additional RC low-pass filter next to the loop filter was adaptively introduced; hence the reference spur is additionally suppressed without degrading the settling time or jeopardizing stability. An improvement of 20dB of the reference spur rejection was achieved yielding a spur suppression of -57 dBc. Another very low power PLL is also designed. Power is conserved by operating the voltage controlled oscillator at a higher frequency where the quality factor of the inductor is higher and then dividing down to the required frequency. The PLL outputs a frequency of 402-405 MHz and consumes a 750 μW of power from a 1V supply.

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