NANOCRYSTALS EMBEDDED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K GATE DIELECTRIC FILMS

A Dissertation

by

CHEN-HAN LIN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2011

Major Subject: Materials Science and Engineering

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ABSTRACT

Nanocrystals Embedded Zirconium-doped Hafnium Oxide High-k Gate Dielectric Films.

(August 2011)

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Chair of Advisory Committee: Dr. Yue Kuo

Nanocrystals embedded zirconium-doped hafnium oxide (ZrHfO) high-k gate dielectric films have been studied for the applications of the future metal oxide semiconductor field effect transistor (MOSFET) and nonvolatile memory. ZrHfO has excellent gate dielectric properties and can be prepared into MOS structure with a low equivalent oxide thickness (EOT). Ruthenium (Ru) modification effects on the ZrHfO high-k MOS capacitor have been investigated. The bulk and interfacial properties changed with the inclusion of Ru nanoparticles. The permittivity of the ZrHfO film was increased while the energy depth of traps involved in the current transport was lowered. However, the barrier height of titanium nitride (TiN)/ZrHfO was not affected by the Ru nanoparticles. These results can be important to the novel metal gate/high-k/Si MOS structure. The Ru-modified ZrHfO gate dielectric film showed a large breakdown voltage and a long lifetime.

The conventional polycrystalline Si (poly-Si) charge trapping layer can be replaced by the novel floating gate structure composed of discrete nanodots embedded in the high-k film. By replacing the SiO_2 layer with the ZrHfO film, promising memory

functions, e.g., low programming voltage and long charge retention time can be expected. In this study, the ZrHfO high-k MOS capacitors that separately contain nanocrystalline ruthenium oxide (nc-RuO), indium tin oxide (nc-ITO), and zinc oxide (nc-ZnO) have been successfully fabricated by the sputtering deposition method followed with the rapid thermal annealing process. Material and electrical properties of these kinds of memory devices have been investigated using analysis tools such as XPS, XRD, and HRTEM, electrical characterizations such as C-V, J-V, CVS, and frequency-dependent measurements. All capacitors showed an obvious memory window contributed by the charge trapping effect. The formation of the interface at the nc-RuO/ZrHfO and nc-ITO/ZrHfO contact regions was confirmed by the XPS spectra. Charges were deeply trapped to the bulk nanocrystal sites. However, a portion of holes was loosely trapped at the nanocrystal/ZrHfO interface. Charges trapped to the different sites lead to different detrapping characteristics. For further improving the memory functions, the dual-layer nc-ITO and -ZnO embedded ZrHfO gate dielectric stacks have been fabricated. The dual-layer embedded structure contains two vertically-separated nanocrystal layers with a higher density than the single-layer embedded structure. The critical memory functions, e.g., memory window, programming efficiency, and charge retention can be improved by using the dual-layer nanocrystals embedded floating gate structure. This kind of gate dielectric stack is vital for the next-generation nonvolatile memory applications.

DEDICATION

For my whole family and lovely wife, Wan-Chen

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CHAPTER I

INTRODUCTION

1.1 High-K Gate Dielectrics for Si-MOSFET

1.1.1 General Background

Since the silicon-based metal oxide semiconductor field effect transistor (Si-MOSFET) was first invented in the mid-60s, for past decades, shrinking its physical feature size has been a driving force for the development of the semiconductor industry. Figure 1 shows the schematic diagram of the typical N-channel MOSFET (NMOSFET).[1] With decreasing the channel length (L), the device's performances, e.g., switching speed and driving channel current (I) can be greatly enhanced. At the same time, more transistors can be integrated into a single chip, which significantly lowers the cost of integrated circuit (IC) production. The driving channel current (I) of the NMOSFET can be expressed by Eq. 1,[2]

$$I = \frac{1}{2}\left(\frac{W}{L}\right)\mu_n C_{ox} V_{DS} (V_{GS} - V_T) \qquad [1]$$

where W is the channel width, L is the channel length, μ_n is the effective mobility of electrons in the channel, C_{ox} is the capacitance of the gate structure, V_{DS} is the channel potential (drain to source), V_{GS} is the gate voltage (gate to source), and V_T is the threshold voltage of the device.

This dissertation follows the style of *Journal of the Electrochemical Society*.

Equation 1 indicates that decreasing the channel length (L) and increasing the gate capacitance (C_{ox}) are the two effective ways to enhance the channel current. However, many challenges are raised for this purpose. One of them is to decrease the thickness (d) of the gate dielectric film in order to maintain the proper gate control.

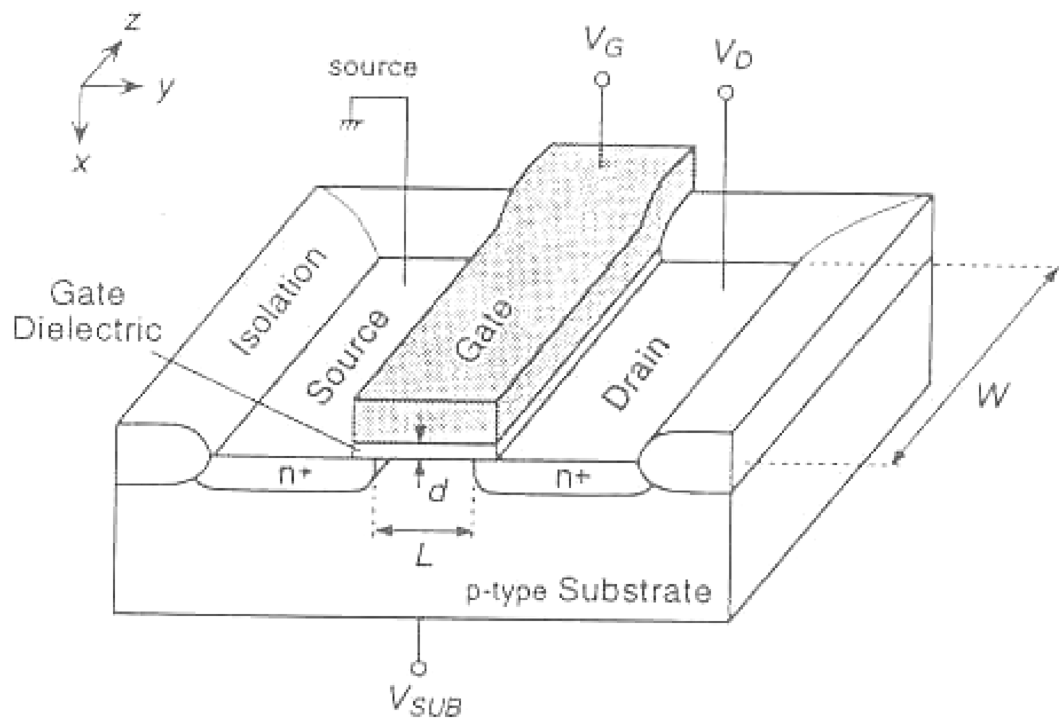

Figure 1. Schematic diagram of NMOSFET.[1]

The thermally-grown silicon dioxide (SiO_2) film has been used as the gate dielectric for decades due to its excellent bulk and interfacial properties, such as high energy band gap (E_g ~9 eV), high dielectric breakdown strength (~15 MV/cm), high amorphous-to-polycrystalline temperature (>1100 ^oC), low interface (SiO_2/Si) state density (<10^{11} $eV^{-1}cm^{-2}$), and high conduction (3.5 eV) and valance band (4.4 eV) offsets with respect to Si wafer.[3-5] However, when the SiO_2 film is kept scaling down to less than 3 nm, the gate leakage current becomes very intensive due to the direct tunneling effect. This causes the power consumption and device reliability concerns.[6-7] It also has been reported that the gate tunneling current increases by two orders as lowering SiO_2 film thickness by each 0.5 nm.[8] Apparently, the SiO_2 thickness scaling down is not unlimited. It will meet a material and electrical limitation, e.g., 1 nm, however, which is required for the 45 nm technology node.[9] Fortunately, spin-offs still exists. Equation 2 expresses a MOS structure's gate capacitance (C_{ox}) under the accumulation or strong inversion condition,

$$C_{ox} = \frac{k\varepsilon_0 A}{d} \quad [2]$$

where k is the gate dielectric film's dielectric constant, ε_0 is the vacuum permittivity (8.85×10^{-14} F/cm), and A is the gate electrode's area. Since the unavoidable thickness scaling of the SiO_2 film is due to its low dielectric constant (k~ 3.9), it can be replaced by a high-k material, i.e., k > 3.9, to not only obtain a high gate capacitance but also increase the physical film thickness. Therefore, by using the high-k MOS structure, the promising device characteristics, e.g., gate control ability, low leakage current, and sufficiently large channel current, can be simultaneously achieved.

1.1.2 HfO_2 High-K Gate Dielectric

Not all high-k materials are suitable for the MOSFET technology. They must be compatible to the modern IC processes, such as dopants activation, etching, lithography, and back end metallization. In addition, unlike the thermally-grown SiO_2, high-k materials need to be deposited on the Si wafer. Apparently, the interfacial quality of the Si/high-k interface is not comparable to the Si/SiO_2 interface because of the former's heterogeneous deposition process. Therefore, a high-k candidate for the MOS structure is not expected to achieve as same excellent properties as those of SiO_2, e.g., very low interface state density and amorphous phase throughout the fabrication process. However, it is possible to optimize above properties through tailoring the deposition conditions. The most important advantage of the high-k film to be employed as the gate dielectric is its physical thicker thickness than the SiO_2 film under the same equivalent oxide thickness (EOT). EOT is a critical parameter of the MOS structure, and can be defined as the thickness of a SiO_2 film that provides as same capacitance as a high-k film does. The criteria and requirements of a high-k candidate for the MOSFET technology are summarized in Table 1.[10]

K Value and E_g

Although a high k value is no questionably preferable, it should be in the reasonable range, e.g., 15-60. If the gate dielectric film has an insufficient k value, it would not fully satisfy the requirements of the EOT scaling down. In contrast, materials with very high k values generally have poor thermal stability, and suffer field-induced barrier lowering effect (FIBL).[11] This makes the threshold voltage unstable, and further degrades the gate control ability.

Table 1. Criteria and requirements of high-k film for MOSFET application.[10]

Criteria	Requirements
EOT < 1 nm	K > 15
Negligible FIBL Effect	K < 60
Leakage < 1 A/cm^2	Eg > 5 eV
Thermal Stability	Minimum Reduction and Reaction with Si Substrate
Interface State Density	$< 10^{11}\ eV^{-1}\ cm^{-2}$
Hysteresis	< 20 mV
Reliability	> 10 years

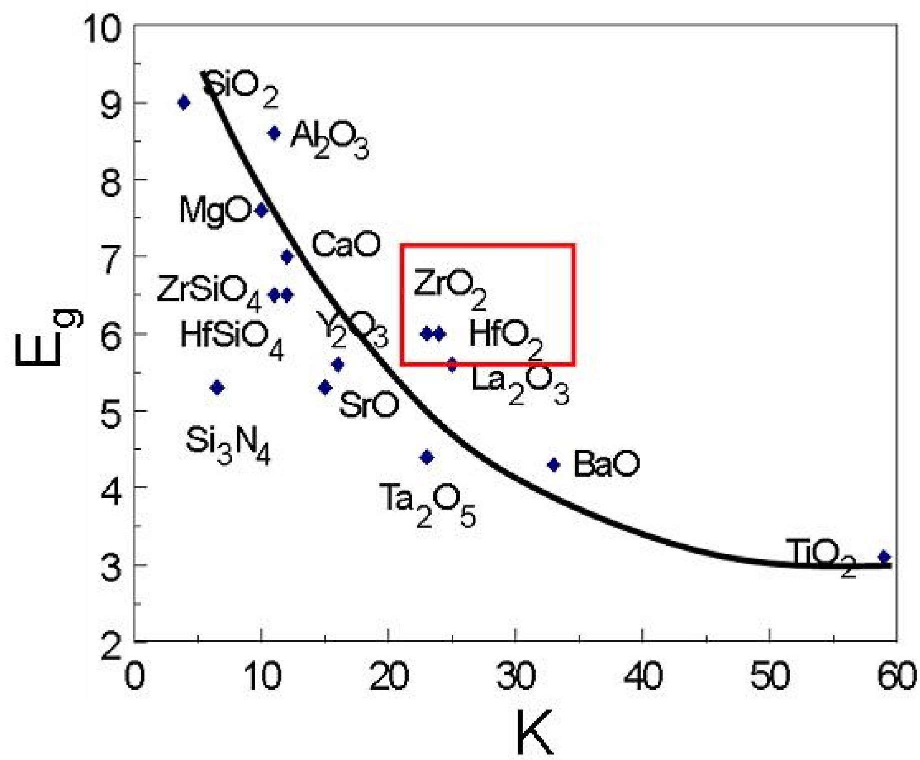

Figure 2. Band gap (E_g) vs. dielectric constant (k) of high-k gate dielectric candidates.[12]

On the other hand, the gate leakage current is the biggest issue for a MOS structure. From Table 1, a band gap (E_g) > 5 eV is required to limit the gate leakage current < 1 A/cm^2. Figure 2 shows the relationship between the k value and E_g of several gate dielectric candidates.[12] The general trend between these two material properties can be expressed by the following equation:[12]

$$E_g = 20\left(\frac{3}{2+k}\right)^2 \quad [3]$$

which shows that the E_g increases reversely with the k value. Judged from Table 1 and Fig. 2, both hafnium oxide (HfO_2) and zirconium oxide (ZrO_2) films are likely best high-k candidates because they have relatively high E_g's (~6 eV) and suitable k values (~20-25).

Thermal Stability and Interfacial Quality

A high temperature treatment is required to fabricate the MOSFET, e.g., post deposition annealing and dopants activation.[13] If the high-k film is not thermally stable, the amorphous-to-polycrystalline phase transition may occur, which creates a number of grain boundaries to serve as diffusion paths.[14] In this case, the gate leakage current is greatly increased.[15-16] On the other hand, the interfacial quality of the Si/high-k interface is also substantial because it affects the interface density states and the carrier mobility in the channel. It was reported that most high-k films have two kinds of interfacial stability concerns during the high temperature process, i.e., reduction of the high-k film and reaction with the Si substrate.[17] After the reduction, the out-diffused metal atoms may react with Si and O to form an unfavorable interface layer at the Si/high-k interface. Additionally, the high-k film may directly react with the Si substrate to form the metal-

silicide,[18] which increases the leakage current. The interface layer formed between the high-k film and Si wafer has a relatively low k value, therefore, reduces the effective dielectric constant of the whole MOS stack. In fact, how to inhibit the interface layer formation has been widely studied since the high-k MOS technology was proposed.[19-21] Among high-k gate dielectric candidates, HfO_2 has a relatively high free energy of reaction with Si (47.6 Kcal/mol),[10] therefore, it is expected to be more stable on the Si substrate compared with other high-k materials. Although another high-k candidate ZrO_2 was also reported that has a thermal stable interface with the Si,[22] HfO_2 still has more potential for the MOSFET application than ZrO_2 does, i.e., lower free energy of formation, lower thermal expansion coefficient, and lower self diffusivity.[10,23] The comparison of the thermal stability properties between the HfO_2 and ZrO_2 are listed in Table 2.[10,23-24] In general, both high-k films have similar thermal properties.

Table 2. Thermal stability properties of HfO_2 and ZrO_2. [10,23-24]

	HfO2	**ZrO2**
Heat Formation (Kcal/mol)	271	261.9
Free Energy of Formation (KJ/mol)	-1088	-1040
Thermal Expansion Coefficient (10^{-6} K^{-1})	5.3	7
Self Diffusion Coefficient at 900K	2.8×10^{-17}	6×10^{-10}

Conduction and Valance Band Offsets with Respect to Si

Since the high-k gate dielectric directly contacts with the Si substrate, its band alignments, i.e., the conduction band and valance band offsets with respect to Si, are strongly related to the carrier transport phenomenon. Usually, a large band alignment favors a low gate leakage current.[25] The reported band alignments of the important high-k gate dielectric candidates are shown in Fig. 3.[26] HfO_2 has the conduction and valance band offsets of 1.5 eV and 3.4 eV with respect to Si, respectively. This number is relatively larger than that of the other high-k candidates which have comparable k values.

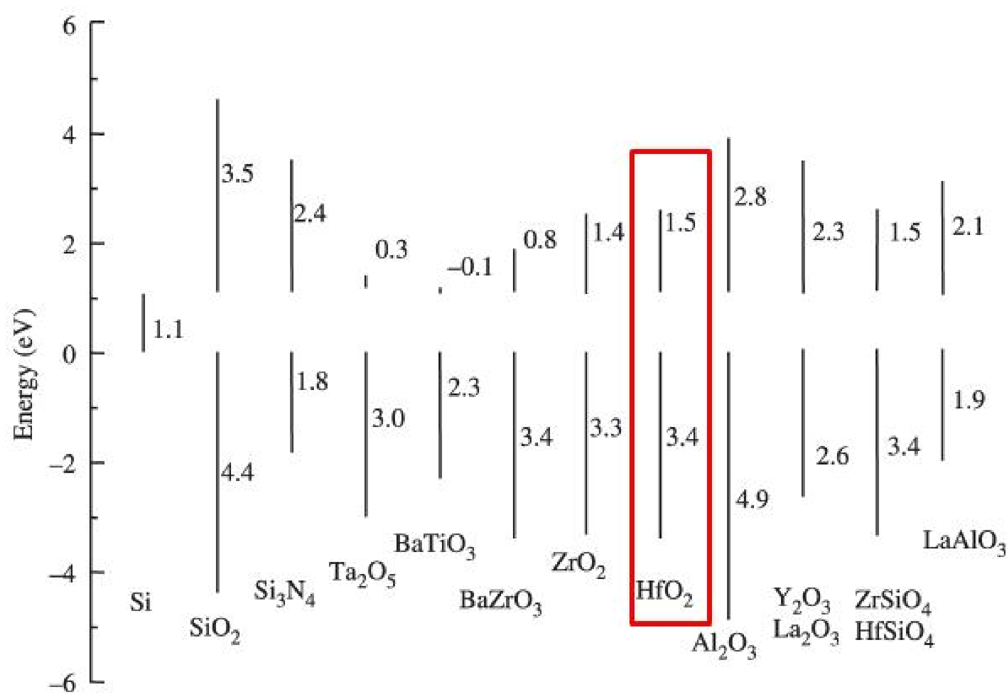

Figure 3. Band alignments of high-k gate dielectric candidates.[26]

1.1.3 Zr-Doped HfO_2 (ZrHfO) High-K Gate Dielectric

HfO_2 has been considered as a promising high-k gate dielectric due to its advantageous materials properties, such as high dielectric constant, wide band gap, good thermal stability, and relatively large band offsets with respect to Si. However, HfO_2 has a big drawback for the Si-MOSFET application, i.e., low crystallization temperature (< 600 ^{o}C).[27] This problem can be solved by doping with other metal oxides that have a high crystalline temperature. For example, Si or Al can be added into the HfO_2 film to increase the amorphous-to-polycrystalline transition temperature because among promising gate dielectrics, only SiO_2 and Al_2O_3 can sustain the amorphous phase under the high temperature process.[28] The Si- and Al-doped HfO_2 film also show improved reliability properties.[29-30] However, the effective k value is reduced because either SiO_2 or Al_2O_3 has a lower intrinsic dielectric constant than HfO_2. In addition, these doped-HfO_2 films show phase decomposition at a high temperature (> 900 ^{o}C), which degrades the device characteristics.[31-32] Recently, ZrO_2 has been proposed to dope with HfO_2 for the gate dielectric applications because it has a higher permittivity than SiO_2 or Al_2O_3. Moreover, judged from the ZrO_2-HfO_2 phase diagram as shown in Fig. 4, ZrO_2 is totally miscible with HfO_2.[33] Therefore, the phase decomposition problem can be ruled out in the ZrHfO film. In addition, both HfO_2 and ZrO_2 films have similar gate dielectric properties, e.g., band gap, thermal stability, and large band offsets, as discussed in the section 1.1.2. The crystallization temperature of the ZrHfO film is also expected to be higher than that of the un-doped HfO_2 film because the Zr dopant can interfere the long-range-order formation of the HfO_2 film's crystalline structure. The similar concept has been demonstrated in the Zr-doped tantalum oxide (Ta_2O_5) film.[34] The addition of Zr may

change the surface energy constraint and the bulk crystal growth mechanism, which increases the crystallization temperature of the Ta_2O_5 film.

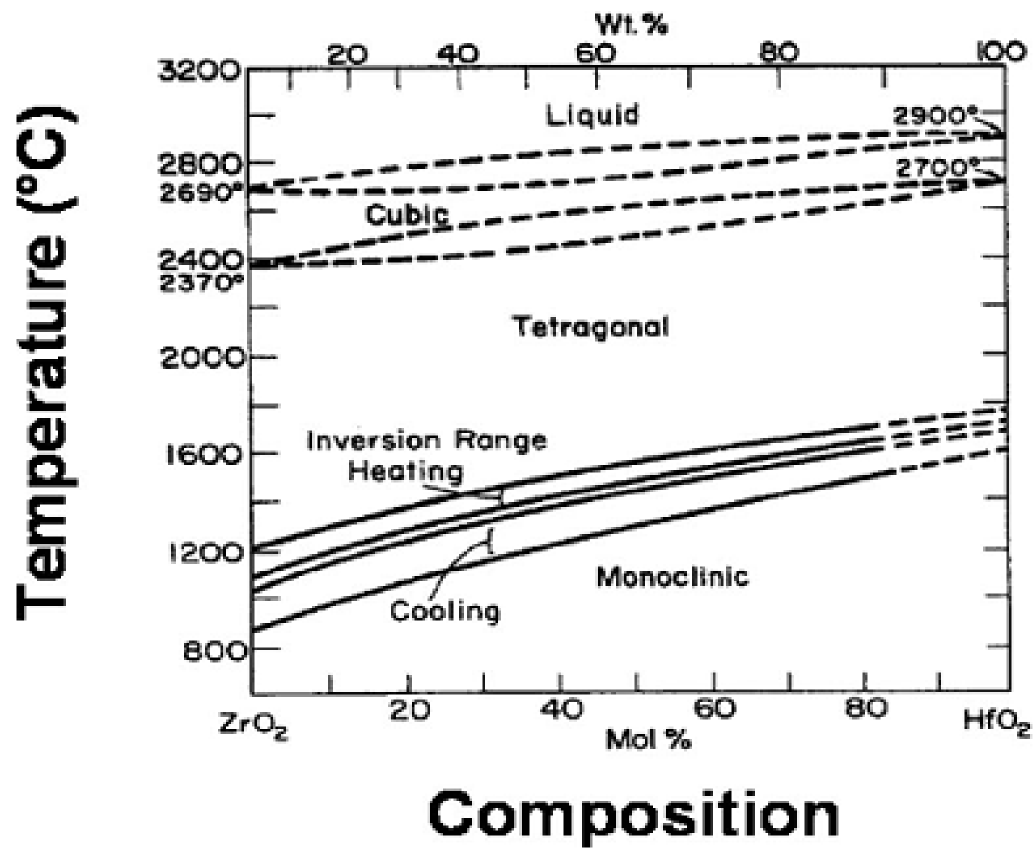

Figure 4. ZrO_2-HfO_2 phase diagram.[33]

1.1.4 Metal Incorporation in High-K Film

Recently, metallic materials have been proposed to replace the polycrystalline Si (poly-Si) as the gate electrode for the Si-MOSFET technology.[35-36] This is because the boron dopants from the conventional poly-Si gate can penetrate the underneath gate dielectric film during the source and drain thermal activation step,[37] which causes the threshold voltage unstable. Sun *et al.* also reported that when the high-k HfO_2 gate dielectric was contaminated with boron, the device's channel mobility and gate leakage current were degraded due to the band offset reduction and induced gap states in the high-k film.[38] By using the metal gate structure, the boron penetration effect can be eliminated. Among many metal gate candidates, ruthenium (Ru) is very promising for P-channel MOSFET (PMOSFET) due to its relatively high work function and theoretical chemical and thermal stability with respect to HfO_2.[39-40] However, many works regard for the thermal response of the Ru/HfO_2/Si MOS structure have been reported.[41-44] The results indicate the unstable thermal performance of this kind of structure. For example, Ru may diffuse into the HfO_2 film during the rapid thermal process at temperature as low as 800 ^{o}C.[41] Also, Ru may react with the bottom HfO_2 film to form a thin ruthenium oxide (RuO) interface layer at the Ru/HfO_2 contact region.[42] On the other hand, the high-k film changes its material and electrical properties with the inclusion of the metal nanoparticles. Chen *et al.* reported that the effective work function of the TiN/HfO_2/SiO_2/Si MOS capacitor can be modified by ion implanting aluminum (Al) nanoparticles into the stack due to the Al-induced dipole formed at the HfO_2/SiO_2 interface.[45] Ravindran reported that the Al_2O_3 film's permittivity can be increased by adding silver (Ag) nanoparticles in the film because the injected carriers from the Si

substrate can be trapped to the silver nanoparticle, and result in the dipole enhancement effect.[46] The similar phenomenon was also reported in the $SiO_2/Al_2O_3/Li_2O$ dielectric stack with the inclusion of the gold (Au) clusters.[47] In this dissertation, the Ru modification effects on the material and electrical properties of the ZrHfO MOS capacitor containing Ru nanoparticles will be thoroughly investigated and discussed.

1.2 Nanocrystal Nonvolatile Memory

1.2.1 General Background of Flash Nonvolatile Memory

A nonvolatile memory is defined as the two memory states that can be distinguished (data-sustain capability) at least for 10 years without power. With the dramatic progress of the Si-MOSFET technology in past decades, Flash memory attracts most attention compared with other types of nonvolatile memories due to its process compatibility.[48] Flash memory was first proposed by Masuoka in 1980 while he was working in Toshiba. The word "Flash" was named from the memory's erase process, which impressed Masuoka's colleague, Ariizumi, and reminded him of a camera flash. Flash memory has been widely exploited for the modern portable electronics because of many promising advantages, such as low power consumption, high density, and low cost. A Flash memory chip is composed of core memory cells and peripheral circuits. Many transistors are used in the peripheral circuit to operate the programming or erasing process of the core memory cell. Figure 5 shows (a) the schematic cross-sectional structure and (b) the circuit symbol of a Flash memory core cell.[49] The core cell is similar to the typical NMOSFET, but has an additional gate electrode called floating gate (FG). The conventional FG is made of a continuous poly-Si layer, which acts as a potential well

to trap charges. As long as charges are trapped in this potential well, they will not escape without an external electric field. Therefore, the memory cell can be programmed (trapping charges) or erased (detrapping charges) by applying a positive or negative gate bias, respectively, i.e., inducing carriers injected from the substrate channel into the FG or pushing them back to the channel. Both programming and erasing operations will result in tunnel currents through the insulator 1. Therefore, the insulator 1 is usually called “tunnel oxide”. The insulator 2 is usually thinker than the insulator 1 to prevent from the interactions between the FG and control gate; thus, the insulator 2 is usually called “control oxide”.

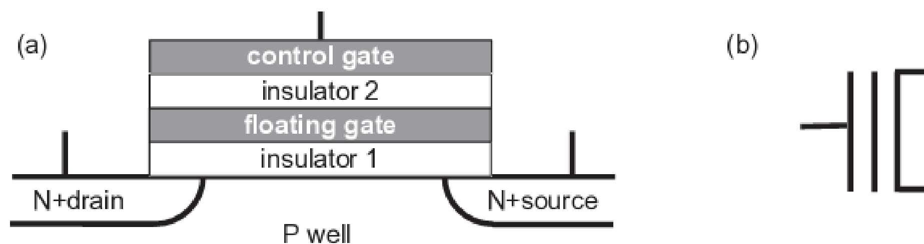

Figure 5. (a) Schematic cross-sectional structure and (b) circuit symbol of Flash memory core cell.[49]

1.2.2 Scaling of Flash Nonvolatile Memory

Although Flash memory that is consisted of a continuous poly-Si FG structure fits most requirements of the modern nonvolatile memory applications, compared with the volatile dynamic random access memory (DRAM), Flash memory still has drawbacks such as a slower programming/erasing speed (1 ms/100 ms vs. 50 ns/50 ns of DRAM) and a higher programming/erasing voltage (18 V vs. 1 V of DRAM).[50] Apparently, further improvements are needed in order to achieve the future ultra-high density and energy-saving nonvolatile memories. For this purpose, the tunnel oxide thickness must be scaled down. A recent study showed that the programming/erasing speed can achieve ~100 ns when the tunnel oxide SiO_2 layer is thinned to about 2 nm.[51] However, the charge retention time drops to only seconds, which makes it not applicable to the nonvolatile memory applications. Therefore, the currently commercial Flash memory cell consists of a ~6-7 nm tunnel oxide SiO_2 and a ~12 nm control oxide SiO_2 to guarantee the retention time > 10 years.[52] Table 3 shows the 2007 International Technology Roadmap for Semiconductor (ITRS) report for Flash nonvolatile memory (NAND structure).[52] The tunnel oxide thickness is projected to maintain 6-7 nm before 2016, while it will need to be scaled down to 4 nm afterwards.

Table 3. 2007 ITRS report for Flash (NAND Structure) nonvolatile memory.[52]

Year of Production	2010	2011	2012	2013	2014	2015
NAND Flash Technology (nm)	36	32	28	25	22	20
Tunnel Oxide Thickness (nm)	6-7	6-7	6-7	6-7	6-7	6-7
Highest P/E Voltage (V)	15-17	15-17	15-17	15-17	15-17	15-17
Endurance (P/E cycles)	10^5	10^5	10^5	10^5	10^5	10^5
Retention (years)	10-20	10-20	10-20	10-20	10-20	10-20

Year of Production	2016	2017	2018	2019	2020	2021
NAND Flash Technology (nm)	19	18	16	14	13	11
Tunnel Oxide Thickness (nm)	4	4	4	4	4	4
Highest P/E Voltage (V)	15-17	15-17	15-17	15-17	15-17	15-17
Endurance (P/E cycles)	10^4	10^4	10^4	10^4	10^4	10^4
Retention (years)	5-10	5-10	5-10	5-10	5-10	5-10

1.2.3 Nanocrystals Embedded FG Structure

Since the memory device's charge retention performance degrades with the tunnel oxide thickness scaling down, replacing the conventional poly-Si charge trapping layer by a charge loss-immune FG structure is required for the future Flash memory. Recently, a novel FG structure composed of the discretely-dispersed silicon nanocrystals (nc-Si) was proposed by Tiwari in 1996 to beat the tradeoff between the tunnel oxide thickness scaling down and the charge retention performance.[53] Figure 6 illustrates why the nc-Si FG structure can alleviate the charge loss when the tunnel oxide is thinned.[54] Figure 6(a) shows that the conventional FG structure contains a continuous poly-Si layer. Since the poly-Si is conductive, the charges stored in the FG are mobile. If there is one defect chain across the tunnel oxide, all stored charges will easily leak through the defect chain. This is why the conventional FG structure needs to exploit a thick tunnel oxide to prevent from the charge leaking. In contrast, the nc-Sis are separated from each other, and discretely embedded in the insulating tunnel and control oxide, as shown in Fig. 6(b). Therefore, the stored charges are immobile. Only the charges stored in the nc-Si located right above the defect chain will leak. Since the nc-Si FG structure is more immune to the defect chains in the tunnel oxide, the tunnel oxide layer could be thinned to achieve a fast programming/erasing speed and a low power consumption as well as a long retention time. Figure 6(c) shows the cross-sectional TEM views of the memory structure presented in the Tiwari's study.[53] The nc-Sis (indicated by circles) are separately embedded in the tunnel and control oxide. Obviously, the discretely-dispersed distribution of the nc-Sis is demonstrated. The size of nc-Si is varied from 2 nm to 10 nm in diameter. Different Si orientations are also observed. The spatial density of nc-Si is ~3-

10×10^{11} cm^{-2}.

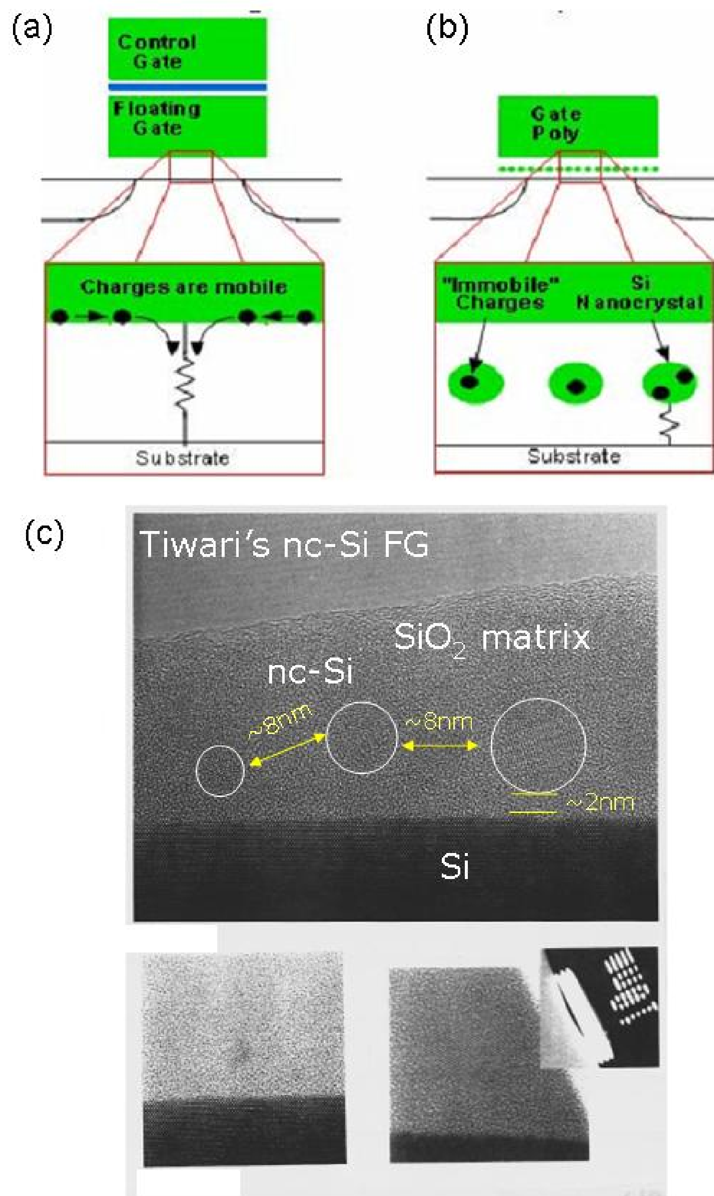

Figure 6. Schematic diagram illustrates how a defect chain affects the charge loss in (a) conventional FG structure and (b) nc-Si FG structure. (c) Cross-sectional TEM views of the memory structure presented in the Tiwari's study.[53-54]

1.2.4 Nanocrystal Engineering

Either the conventional poly-Si FG Flash memory or the nc-Si FG Flash memory, Si is selected as the charge storage medium due to its compatibility to the stand MOSFET technology. However, the nc-Si memory will suffer the degraded retention characteristics due to the quantum confinement effect (QCE) and the Coulomb blockade effect (CBE).[55-56] The two effects are briefly introduced as follows:

Quantum Confinement Effect (QCE)

QCE can be described as: when the size of Si comes to the nanoscale, its band gap becomes larger. This implies that the energy band offset of the nc-Si/tunnel oxide is lower than that of the bulk-Si/tunnel oxide, as shown in Fig. 7(a). The shift of the conduction band edge due to QCE, i.e., $\Delta E_c = E_c$ (nc-Si) - E_c (bulk Si), is given as:[57]

$$E_c(d_{Si}) - E_c(\infty) = \frac{1.39}{d_{Si}^{2} + 1.788\, d_{Si} + 0.668}(eV) \qquad [4]$$

where E_c (d_{si}) is the conduction band edge of the nc-Si, E_c (∞) is the conduction band edge of the bulk Si, and d_{si} is the nc-Si size in diameter. From Eq. 4, the conduction band edge of a 5 nm nc-Si is higher than that of a bulk-Si by 0.04 V, i.e., about 3.57 % increase.

Coulomb Blockade Effect (CBE)

CBE can be described as: when an electron is trapped in a nanocrystal, its electrostatic potential will be increased by q^2/C,[58] as shown in Fig. 7(b), i.e.,

$$\Delta E = \frac{q^2}{C} \qquad [5]$$

where q is the electron charge, C is the self capacitance of the nanocrystal and equals to $2\pi\varepsilon d$ (where ε is the dielectric constant of the tunnel oxide, and d is the nanocrystal size in diameter). For an electron trapped in a 5 nm nc-Si, the increased electrostatic potential

energy is about 0.074 eV.[53] Therefore, after charges are first trapped in the nc-Si, other charges are more difficult to be subsequently injected through the tunnel oxide due to the deduced electric field across the layer. In consequence, the number of the stored charges in the nc-Si is limited. The density of the stored charges (Q) can be estimated by measuring the threshold voltage shift (ΔV_t) of the memory device, then calculated from the below equation:[53]

$$\Delta V_t = \frac{Q}{\varepsilon_{tun}}(t_{con} + \frac{\varepsilon_{tun} d}{2\varepsilon_{Si}}) \qquad [6]$$

where t_{con} is the thickness of the control oxide; ε_{si} is the dielectric constant of the nc-Si; d is the nc-Si size in diameter, and ε_{tun} is the dielectric constant of the tunnel oxide. In addition, as the nc-Si's electrostatic potential increases, the energy barrier of the nc-Si/tunnel oxide becomes lower. This will also result in the degraded retention performance.

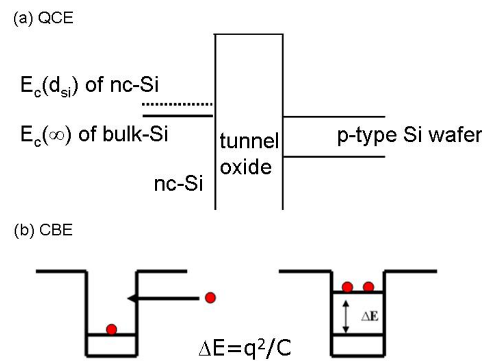

Figure 7. Illustrations of (a) QCE and (b) CBE.

Due to QCE and CBE, the stored charge in the nc-Si has a high potential energy, therefore, will tunnel back to Si substrate easily. One solution to overcome this challenge is to replace the nc-Si by another nanocrystal material that has a higher work function. This is because using high work function (usually > 4.5 eV) nanocrystals as the charge storage medium can create a deep potential well for better retention performance.[59] Recently, metal nanocrystals have attracted a lot of attention for this purpose due to their wide range of available high work functions. In addition, metal nanocrystals have other advantages over the nc-Si such as smaller energy perturbation, stronger coupling with the conduction channel, and higher density of states around the Fermi level, which may increase the charge store density.[60] Many metal nanocrystals, e.g., Ag, Pt, Au, Co, Ni, W, Mo, Ru, etc., have been demonstrated that can be embedded into the gate dielectric for memory applications.[61-68] However, in this dissertation, conductive oxide materials, i.e., ruthenium oxide (RuO), indium tin oxide (ITO), and zinc oxide (ZnO), rather than metals are selected for serving as charge trapping medium. This is because nc-conductive oxide materials may offer advantages of both metals and semiconductors due to their high work functions and large band gaps.[69-71] For example, they can provide a large density of states around the Fermi level (similar to metal),[60] meanwhile allow mid-gap trap states for a high capacity and deep charge trapping (similar to semiconductor).[72]

1.2.5 Tunnel Oxide Engineering

Although the memory device's charge retention performance is promised to be improved by using a high work function nanocrystal as the charge storage medium, this kind of memory device still suffers the high programming power consumption and the

slow programming speed due to the large tunnel oxide thickness. Therefore, the tunnel oxide layer still has to be scaled down in order to achieve the extreme goal of the nanocrystal Flash memory, e.g., as fast programming speed as DRAM, a long retention time > 10 years, and an ultra-high integrated density. This reminds nanocrystal memory researchers of the similar progress history of the MOSFET technology, i.e., finding a proper high-k gate dielectric to replace the conventional thermally-grown SiO_2 tunnel oxide. In 2003, Lee *et al.* first presented the nc-Si Flash memory that employs HfO_2 as the tunnel and control oxide layers.[73] Figure 8 shows that, based on the same EOT of 1.6 nm, HfO_2 has a much larger physical thickness of 4.5 nm, which efficiently inhibits the stored charge loss through the direct tunneling effect back to the Si substrate.[73] In addition, the programming voltage and speed can be also improved because the energy barrier of the Si/HfO_2 is much smaller than that of the Si/SiO_2, i.e., 1.5 eV vs. 3.5 eV. The low energy barrier favors the electron injection and therefore, improves the programming efficiency and power consumption. In this dissertation, the ZrHfO film is exploited as the tunnel and control oxide layers due to its excellent gate dielectric properties.

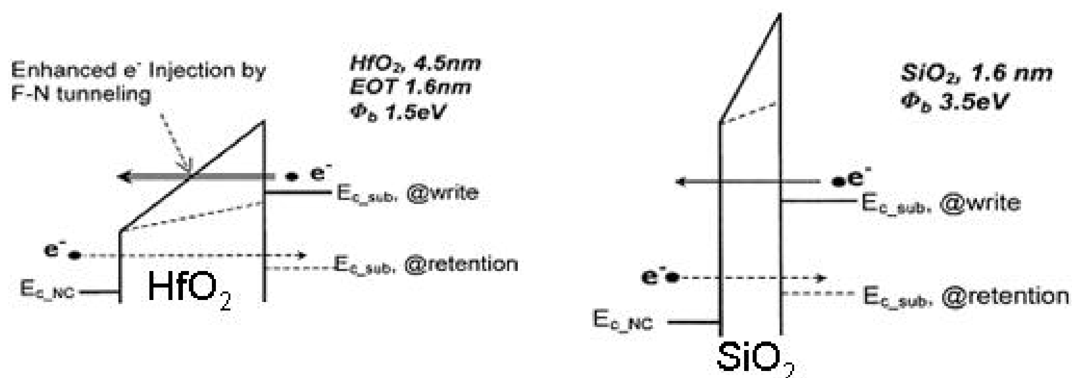

Figure 8. Energy band diagram of Si/HfO_2 (left) and Si/SiO_2 (right) during programming and retention conditions. Both HfO_2 and SiO_2 tunnel oxides have the same EOT of 1.6 nm.[73]

1.2.6 Fabrication of Nanocrystals Embedded FG Structure

The preparation of the nanocrystals embedded FG structure depends on the nanocrystals' intrinsic properties and their interfacial properties with the surrounding oxides. For example, the surface energy difference between the nanocrystal and the surrounding oxide will play a big role in the nanocrystal layer formation mechanism.[74-75] Moreover, the fabrication process must be compatible to the standard MOSFET technology. Several methods such as the chemical vapor deposition (CVD),[53,76-77] ion beam synthesis (IBS),[78-80] and thin film self-assembly process,[81-83] have been proposed to prepare the discretely-dispersed nanocrystals embedded in the gate dielectric stack. For the CVD method, the evolution of the nanocrystal density and size goes through four stages, as shown in Fig. 9(a).[84] In the incubation stage, only a little amounts of the nuclei are formed, and then nanocrystal density increases with the deposition time in the

nucleation stage. Later, in the growth stage, the nanocrystals grow with the deposition time but remain the similar density. In the final coalescence stage, the nanocrystals start to merge, which increases the nanocrystal size but lowers the density. Apparently, the growth stage is desired for preparing the high density discrete nanocrystals. However, this process window can be easily narrowed by the deposition conditions, which limits the successful formation of the discrete nanocrystals. On the other hand, the IBS method consists of two steps to fabricate nanocrystals, i.e., a low energy (~30-150 keV) ion implantation and a subsequent thermal annealing at the high temperature (~950-1050 °C) for 30-60 min, as shown in Fig. 9(b).[78] By adjusting the implant does and the accelerating voltage, the desired concentration profile can be obtained. However, the IBS method still lacks of the controllability of the size and spatial distribution of the nanocrystals in the gate dielectric.[85] Compared with the CVD and IBS methods, the thin film self-assembly process is more popular due to its easy operation. Figure 9(c) illustrates how the self-assembly process works.[60] At first, a 2-5 nm thick film is deposited on the tunnel oxide. The as-deposited film naturally contains the thickness perturbation and internal stress due to its ultra-thin layer structure. Then a heat treatment (usually > 700 ^{o}C) is needed to drive the nanocrystal formation along the initially-built perturbation in the film. This self-assembly process is contributed by the driving forces, e.g., stress relaxation and surface energy minimization. In addition, the repulsion force and the dispersion force created after the formation of nanocrystals further stabilize the discrete structure. In this dissertation, the nc-RuO, -ITO, and -ZnO embedded ZrHfO gate stack are fabricated based on the concept of the thin film self-assembly process. The thin nanocrystal layer will be deposited by the sputtering technique and subjected to a rapid thermal process.

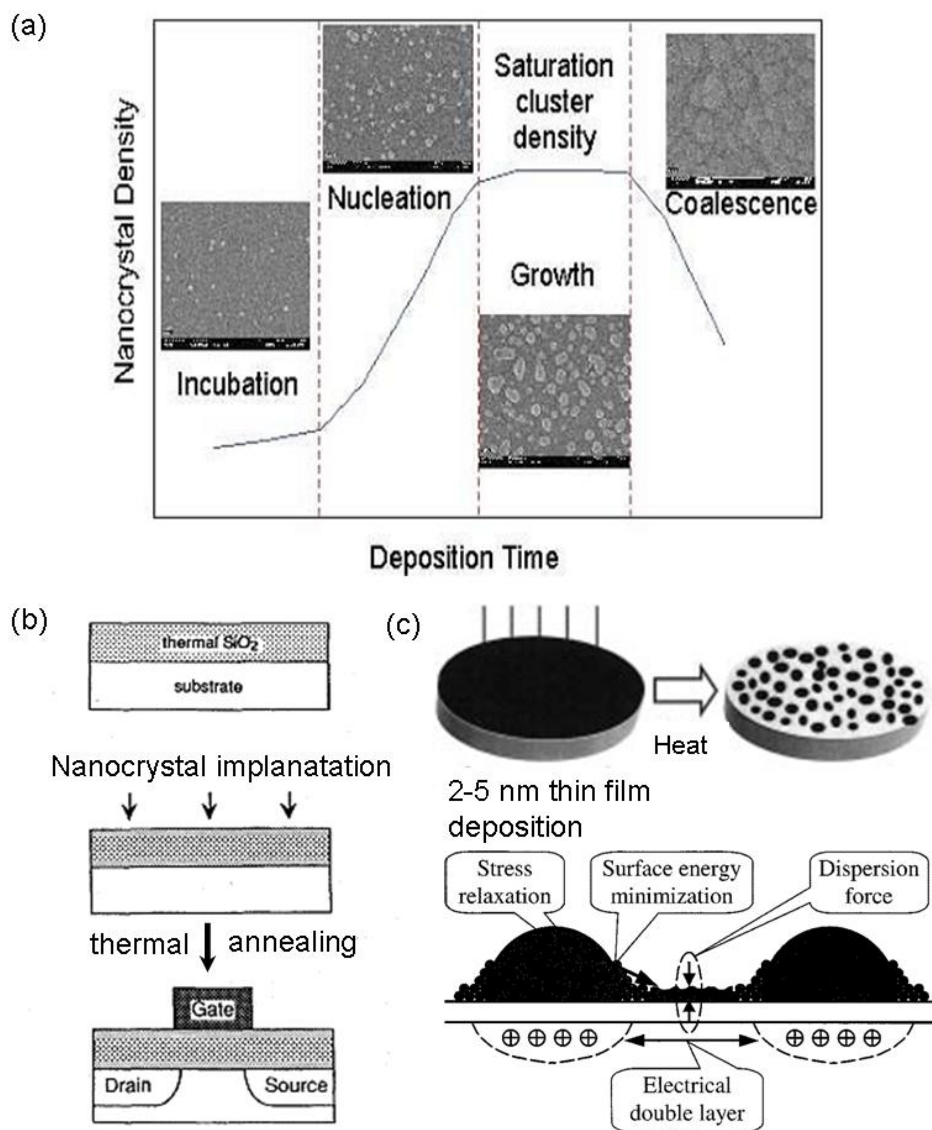

Figure 9. Illustrations of (a) CVD, (b) IBS, and (c) thin film self-assembly process methods for preparing nanocrystals.[60,78,84]

1.3 Outline of the Dissertation

Chapter II focuses on the experimental methods utilized in this dissertation. Their corresponding background knowledge and the related equipment operations will be described. At first, the process flow of fabricating the high-k ZrHfO MOS capacitor will be described in detail. Then, the fundamental background of the radio frequency (RF) magnetron sputtering technique will be reviewed since all the high-k films and the nanocrystal layers are deposited by this method. The instruments and the background knowledge of the material characterizations, e.g., profilometer, XRD, XPS, and HRTEM will be introduced. The electrical characterizations of the high-k MOS capacitor, such as the system setup, C-V, NCSU CVC, and J-V measurement methodologies, will be also discussed in this chapter.

Chapter III focuses on the Ru modification effects on the material and electrical properties of the ZrHfO MOS capacitor. After including a small amount of Ru nanoparticles into the high-k stack, the capacitor's EOT (measured at 100 kHz) can be significantly decreased from 1.88 nm to 1.43 nm, while the bulk high-k film becomes thicker, i.e., from 3 nm to 6.5 nm. The Ru modification effects are further investigated by TEM, XPS, G-V, C-V, and J-V measurements. The detailed discussions on the current transport mechanisms and the reliability performance will be also presented.

Chapter IV focuses on the nanocrystalline RuO (nc-RuO) embedded ZrHfO high-k gate dielectric stack for the nonvolatile memory applications. The detailed material and electrical investigations of this kind of memory device will be presented. The discrete nc-RuO shows significant charge trapping capability. The interface formation at the nc-RuO/surrounding ZrHfO contact region has been confirmed by the XPS analysis.

Charges can be deeply trapped at the bulk nc-RuO sites or loosely trapped at the nc-RuO/ZrHfO interface. The device can sustain the long-term data storage capability, i.e., retention time > 10 years. The nc-RuO embedded ZrHfO MOS capacitor is a promising memory device for the future nonvolatile memory applications.

Chapter V focuses on the fabrication and investigation of the single and dual nc-ITO and nc-ZnO layers embedded ZrHfO MOS capacitor for further improving the nonvolatile memory performance. The memory capacitors have been successfully fabricated by the one-pump-down sputtering deposition process followed with a high temperature rapid thermal annealing. The vertical separation of two discrete nanocrystal layers has been obtained. The improved memory characteristics, e.g., in terms of the charge trapping density, charge trapping capacity, charge retaining capability, programming efficiency, and retention time, have been achieved by using the dual-layer embedded structure. The comparisons of the memory functions among capacitors, which separately contain the embedded nc-RuO, nc-ITO, and nc-ZnO, will be discussed in views of the bulk and interfacial material properties.

Chapter VI summarizes all studies in this dissertation and draws conclusions.

CHAPTER II

EXPERIMENTAL

2.1 Introduction

This chapter focuses on the experimental methods utilized in this dissertation. In the first part, the process flow of fabricating the high-k MOS capacitor will be described in detail. From the Si wafer clean to the gate electrode pattern lithography, the experiment conditions of each step will be discussed. Plus, the process-related equipments, e.g., the systems of the load-lock sample transferring, sputtering, and rapid thermal annealing (RTA), will be also introduced. Moreover, the RF magnetron sputtering technique will be reviewed since all the high-k films and nanocrystal layers will be prepared by this kind of thin film deposition method. In the second part, the background knowledge of the material characterization methods, e.g., profilometer, X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), and high-resolution transmission electron microscope (HRTEM), will be reviewed. In the third part, the electrical characterizations of the high-k MOS capacitors, e.g., high frequency capacitance-voltage (C-V) curve, current density-voltage (J-V) curve, measurement methodologies, and system setup, will be discussed as well.

2.2 Process Flow of MOS Capacitor Fabrication and Equipment Setup

Figure 10 shows the process flow chart of fabricating a high-k MOS capacitor. In this dissertation, all the MOS capacitors will be fabricated on the (100) p-type Si substrate (resistivity 11-20 Ω·cm, doping concentration at 10^{15} cm^{-3}, supplied from

MEMC). The sample size is about 1 inch×1 inch.

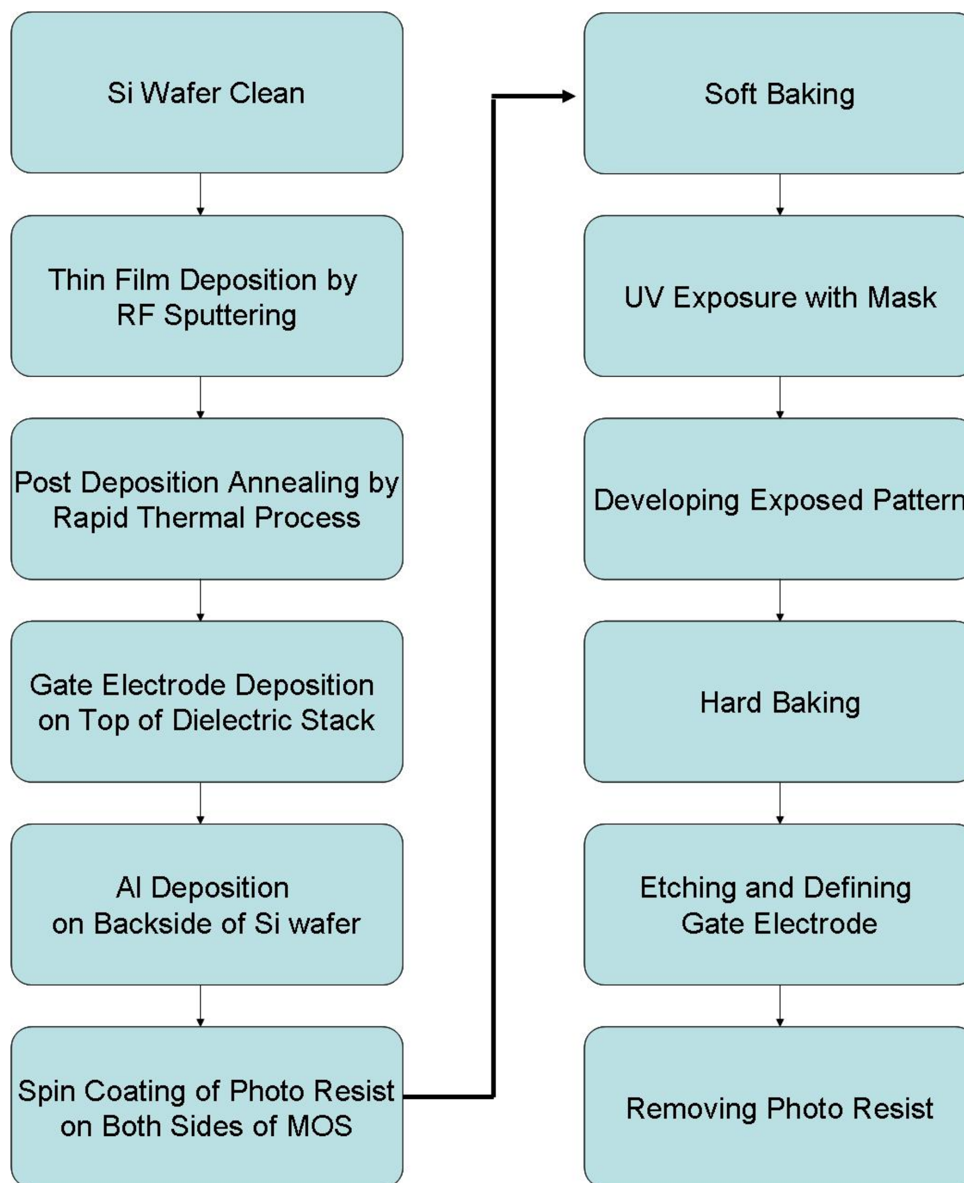

Figure 10. Process flow chart of high-k MOS capacitor fabrication.

2.2.1 Si Wafer Clean and Load-Lock Sample Transferring System

The bare Si substrate was cleaned by a dilute hydrofluoric acid (DHF, 2 %) solution for 5 min to remove the native oxide formed at the Si surface. The Si surface became hydrophobic after the native oxide was removed. Then, the sample was fully rinsed by dipping in the deionized water (DI, resistivity > 18 MΩ·cm) for 5 min. After drying with the N_2 blow gun, the sample was immediately loaded into the load-lock chamber, which was subsequently pumped down to about 10^{-5} Torr by the combination of the mechanical pump (Edwards, E2M8) and turbo pump (Pfeiffer, TPU 170). This pumping process took only about 20 min due to the load-lock chamber's small volume (15 L). Then, the sample was transferred into the sputtering chamber that was already in the high vacuum environment, i.e., < 10^{-6} Torr. After the thin film deposition process, the sample was unloaded from the sputtering chamber to the load-lock chamber without breaking the high vacuum environment in the former. Since pumping down the sputtering chamber usually takes a long time to achieve the high vacuum, i.e., > 4 hrs, due to its large volume (65 L), using the load-lock sample transferring system can greatly increase the production of the thin film deposition process. In addition, the water vapor contamination in the sputtering chamber can be alleviated due to the decreased frequency of exposing the sputtering chamber to the air.

2.2.2 Thin Film Deposition by RF Sputtering

In this dissertation, all the thin film deposition processes, including the high-k gate dielectric, nanocrystal layer, gate electrode, and bottom contact, were carried out by the magnetron radio frequency (RF, 13.56MHz) sputtering machine. Figure 11 shows its

schematic diagram. The sputtering chamber is made of the stainless steel, and vacuum sealed with the fluoroelastomers (Viton) o-rings and copper (Cu) gaskets. Before the deposition process, the chamber was pumped down to the high vacuum condition, i.e., background pressure < 10^{-6} Torr, by the combination of the mechanical pump (Alcatel, 2063 CP1) and turbo pump (Leybold, Turbovac 360). The sputtering system has three guns (i.e., three targets) available for the co-sputtering deposition process at the same time. Each gun is equipped with a permanent NdFeB magnet to magnetron control the plasma, and with a shutter to mechanically start/shut off the deposition process. In addition, both the turbo pump and sputtering gun are water cooled by the cycling chiller system (Neslab, CFT-33). The sample holder can not be heated but can rotate at the speed of 15 RPM for better deposition uniformity. The distance between the sputtering gun and sample holder was about 15 cm. A RF generator and a matching network (box) are needed to carry out the sputtering process. The target size is 2" in diameter and 0.25" thick. Benefitted from the RF power, various target options can be used in this sputtering system, i.e., from the conductive to insulating materials. The gas feedthrough consists of argon (Ar, 99.999 %, research grade), oxygen (O_2, 99.993 %), and nitrogen (N_2, 99.999 %) gases. Ar has its own mass flow controller (MFC), while O_2 and N_2 share the same MFC. Therefore, the deposition ambient can be adjusted to three options, i.e., pure Ar, mixed Ar/O_2, and mixed Ar/N_2.

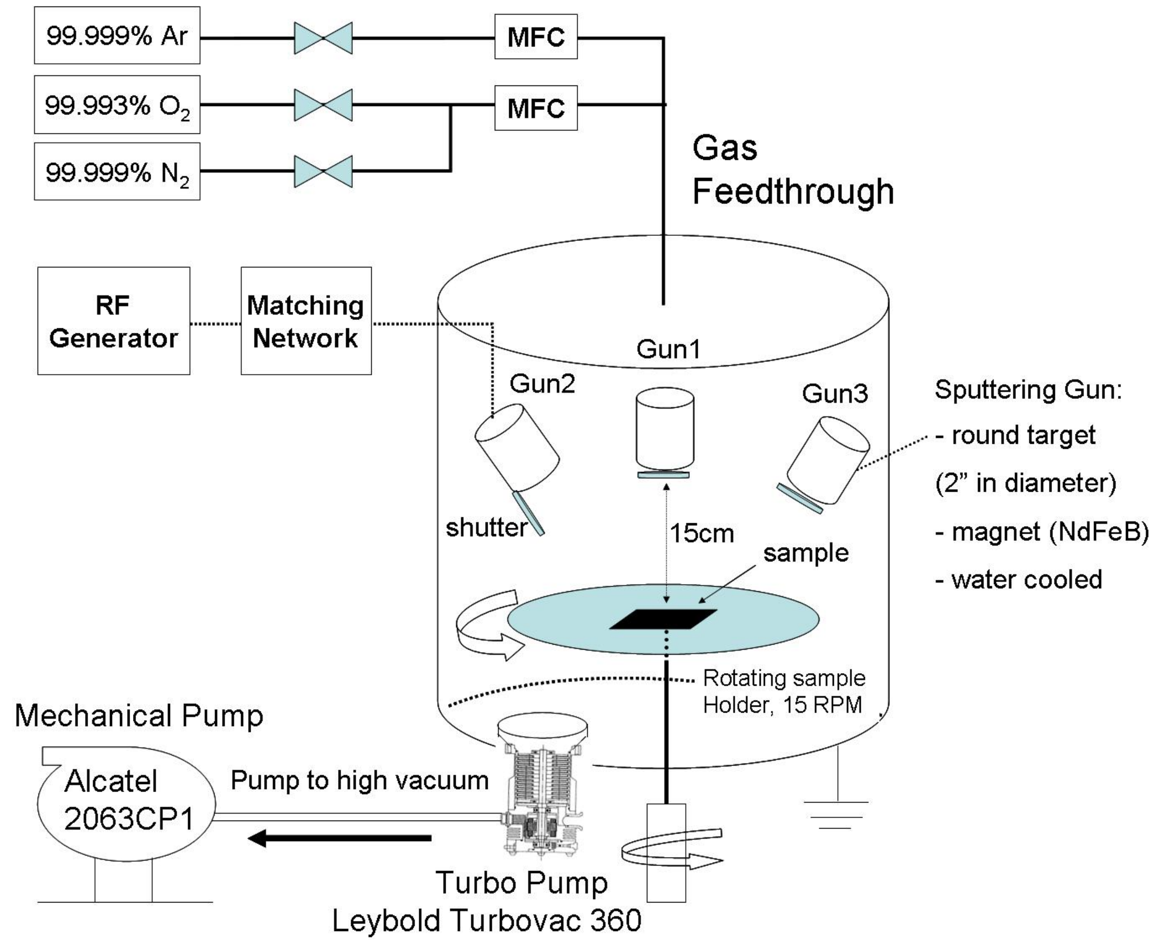

Figure 11. Schematic diagram of RF sputtering system.

In this dissertation, the sputtering power was set to 60-100 W. This is because the high power process may cause the strong ion bombardment effect to damage the sample surface,[86] while the low power process may decrease the deposition rate and degrade the film quality due to the low energized sputtered atoms. The working pressure during the sputtering process was 5 or 10 mTorr. For example, the ZrHfO high-k gate dielectric film was reactively sputtered from a Hf/Zr (88/12 in wt %) composite target (99.8 %) at 5 mTorr in a Ar/O_2 (1/1) mixed ambient (total flow rate of 40 sccm). However, the nanocrystal ZnO layer was reactively sputtered from a Zn target (99.99 %) at 10 mTorr, but in the same gas ambient condition. In addition, the Ru and ITO layers were also sputter deposited at 5 mTorr in pure Ar ambient from Ru (99.95 %) and ITO targets (99.99 %), respectively. Plus, a pre-sputtering step was required to clean the target surface before the deposition. This step can be done with the pure Ar plasma for 15 min.

2.2.3 Post Deposition Annealing by Rapid Thermal Process

After depositing the gate dielectric film on the Si wafer, a post deposition annealing (PDA) process was carried out with the rapid thermal annealing (RTA) method to densify the as-deposited film and to remove the defects. Figure 12 shows the schematic diagram of the RTA system (Modular, RTP 600-S).[87] The sample was placed on the Si wafer holder and heated in the quartz tube. The tungsten-halogen lamps combined with the closed-loop temperature control system and the water cooled assembly can provide a rapid heating and cooling speed. In addition, the temperature profile of the annealing process can be precisely controlled by this RTA system. Therefore, compared with the traditional furnace annealing, RTA process can greatly lower down the thermal budget.

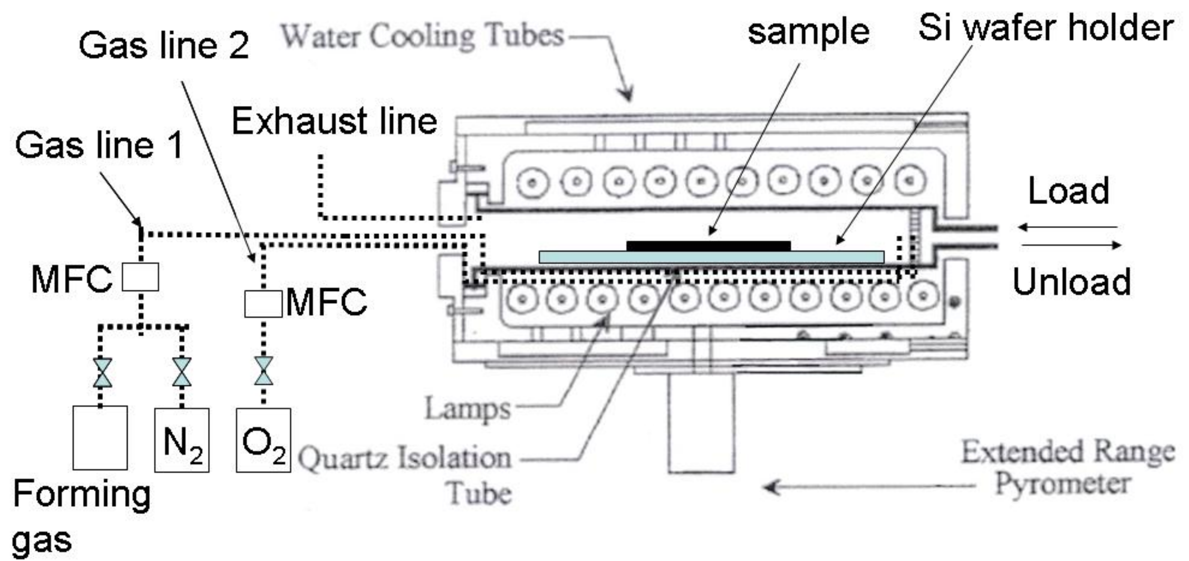

Figure 12. Schematic diagram of RTA system. (After Ref. 87)

The RTA chamber was not vacuumed during the annealing process, however, a large gas flow, i.e., > 5 SLPM, and a strong gas exhaust design can guarantee the purity of the annealing ambient. Three kinds of gases were used in the RTA system, i.e., N_2 (99.999 %), O_2 (99.993 %), and forming gas (H_2/N_2 : 1/9). O_2 has its own MFC, while N_2 and forming gas share the same MFC. Therefore, the mixed N_2/O_2 ambient is also available. In this dissertation, the as-deposited high-k films and nanocrystsal layers were annealed at 800 ^oC to 1000 ^oC for 10 s to 1 min in the pure N_2 or mixed N_2/O_2 ambient depending on the process requirements. The heating speed was set to 50 $^oC/s$ to reach the desired steady-state temperature.

2.2.4 Depositions of Gate Electrode and Backside Contact

After the PDA process, the gate electrode layer was deposited on the high-k gate dielectric stack in order to fabricate the MOS capacitor. For the study of the Ru-modified ZrHfO high-k MOS capacitor related to the low EOT application, titanium nitride (TiN) was employed as the gate electrode due to its excellent interfacial properties with respect to HfO_2, which has been reported in the literatures.[88,89] Figure 13 shows the cross-sectional TEM view of the TiN/ZrHfO/Si high-k gate dielectric stack. Apparently, no interface layer was formed between the TiN and ZrHfO layers. The TiN film was reactively sputtered from a Ti target (99.995 %) at 5 mTorr in a Ar/N_2 (50/1) mixed ambient. Then, a post metal deposition annealing (PMA), i.e., at 350 ^oC for 5 min in forming gas, was performed by RTA to further remove the defects in the bulk TiN film or at the TiN/ZrHfO interface.

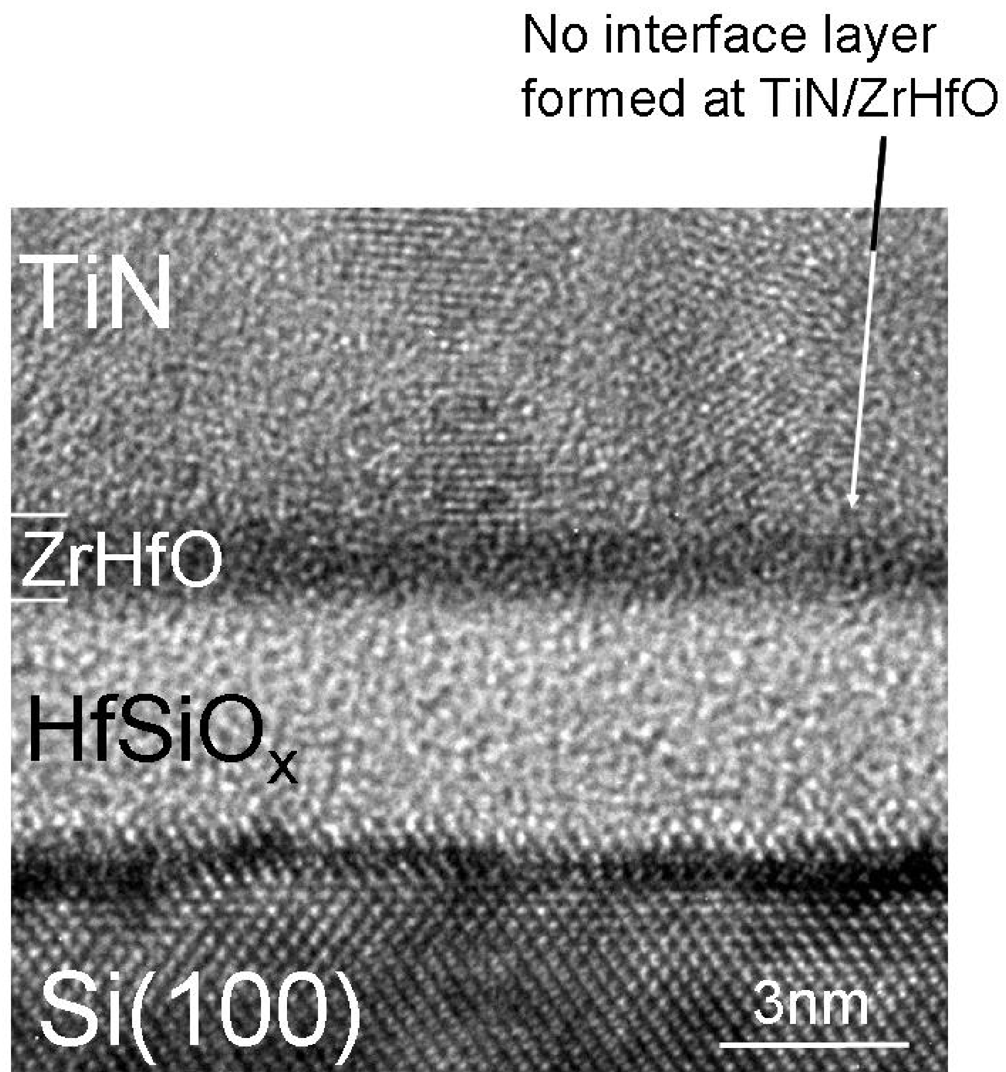

Figure 13. Cross-sectional TEM view of TiN/ZrHfO/Si high-k gate stack.

Consecutively, a 150 nm thick aluminum (Al) layer was deposited on the backside of the Si wafer for better contact. The backside of the Si wafer was pre-scratched for removing the grown oxide, and then followed by the Al deposition sputtered from a Al target (99.999 %) at 5 mTorr in pure Ar ambient. On the other hand, for the study of the nanocrystals embedded MOS capacitor related to the nonvolatile memory applications, a 120 nm thick Al layer was deposited as the gate electrode due to its well-developed deposition and lithography processes.

2.2.5 Patterning Gate Electrode by Lithography Process

In order to fabricate numbers of MOS capacitors on the same Si wafer, a lithography process was carried out to pattern the gate electrode layer. At first, the positive photo resist (AZ Electronics, AZ 5214-E, mixture of acetate, resin, and esters) was spin coated on the top of the gate electrode and backside of the Al contact. Figure 14 illustrates the spin coating process,[90] which includes the dispensation, accelerating, outflow (maximum spin speed), and evaporation steps. The maximum spin speed of the spin coater (Chemat Technology, KW-4A) was set to 4000 RPM, which deposited an around 1.6 μm thick photo resist. The sample was then subjected to a soft baking process done with a hot plate at 90 °C for 1 min to drive away the solvent and enhance the adhesion. Later, the sample was loaded to the contact aligner (Quintel, Q4000), and directly covered with a patterned quartz mask for the UV exposure, i.e., in contact mode. The exposure process took 20 s under the UV power density of 10 mW/cm^2. Then, the exposed pattern was developed in the solution that contains 2 parts of the developer (AZ Electronics, MIF 300) and 1 part of the DI. The MIF 300 developer was composed of

tetramethylammonium hydroxide, which dissolved the UV-exposed photo resist. The develop process took a shot time, e.g., ~3 min, therefore, the pattern distortion was minimized. The sample was further heated again in the oven at 125 °C for 5 min to solidify the photo resist, i.e., hard baking process. The gate electrode layer was subsequently patterned by etching areas that were not covered with the hard-baked photo resist. For the TiN gate, the etching solution consisted of NH_4OH: H_2O_2: H_2O (1:1:5). For the Al gate, the etching solution consisted of H_3PO_4 : HNO_3 : CH_3COOH : H_2O (16 : 1 : 1 : 2). The etching time depended on the layer thickness. In this dissertation, the averaged etching rate of the TiN gate and Al gate was about 15 nm/min and 200 nm/min, respectively.

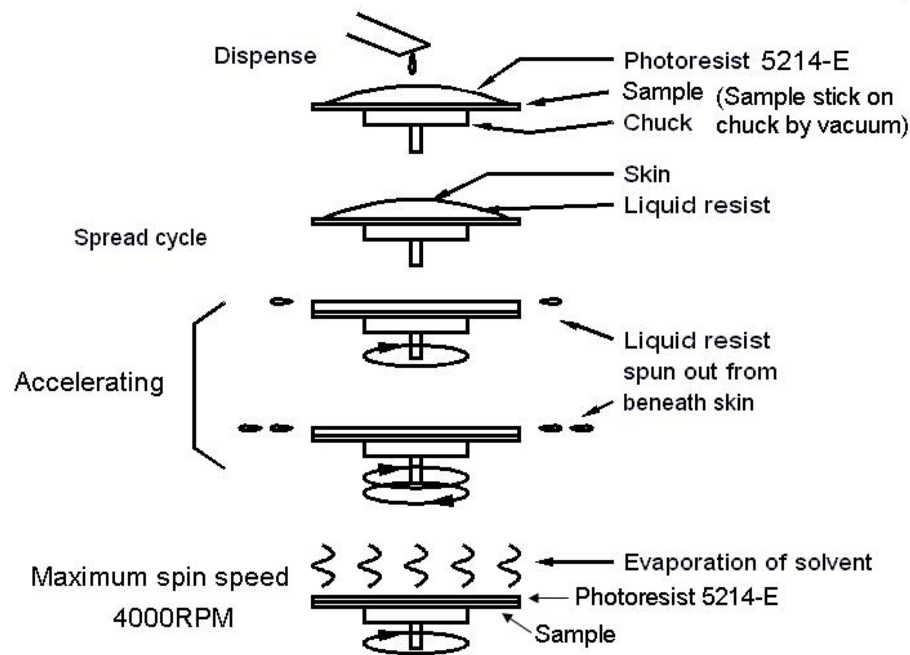

Figure 14. Illustration of spin coating process. (After Ref. 90)

After successfully defining the gate electrode pattern, the photo resist remover (AZ Electronics, 300T Stripper, mixture of propanediol, methylpyrrolidone, and tetramethylammonium hydroxide) was used to remove the residual hard-baked photo resist. Since the AZ 5214-E is a positive photo resist, the lithography process can directly transfer the mask's pattern to the gate electrode. Figure 15 illustrates this pattern transferring process.[13] Finally, the complete MOS capacitor was subjected to a RTA process again at 250 °C or 300 °C for 5 min in forming gas. Under this annealing process, not only the H atom (from the H_2 ambient) can passivate the remaining interface defects,[13] but also the Al atom (from the bottom Al layer) can diffuse into the Si wafer to form the backside ohmic contact.[91]

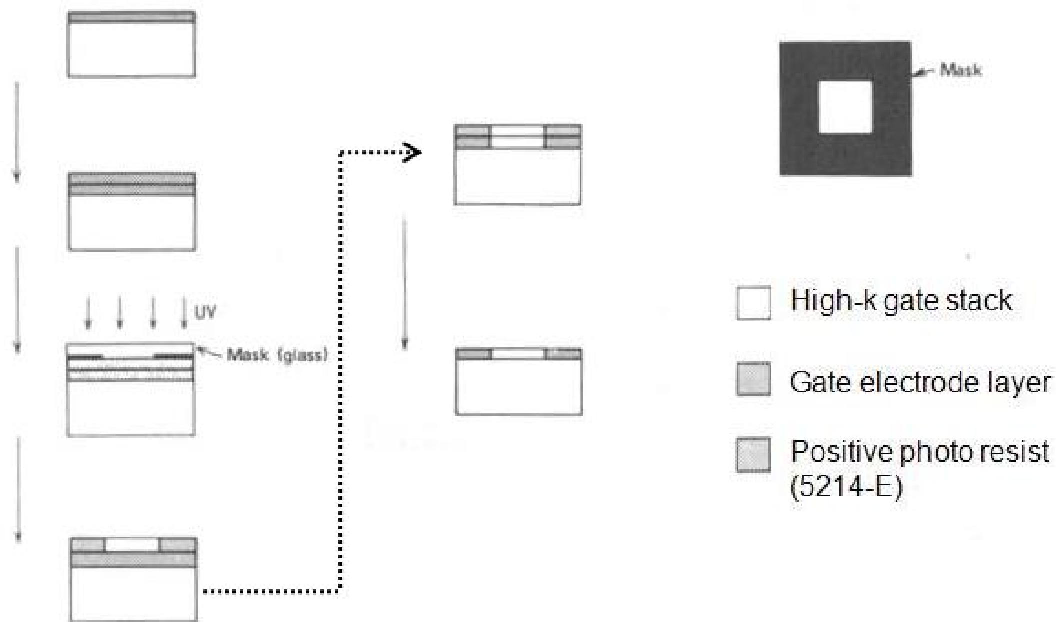

Figure 15. Illustration of pattern transferring process. (After Ref. 13)

2.3 RF Magnetron Sputtering Technology for Thin Film Deposition

In this dissertation, all the high-k films, TiN and Al gate electrodes, and nanocrystalline RuO, ITO and ZnO layers were prepared by the RF magnetron sputtering method. Compared with the direct current (DC) sputtering that can be only applied to the conductive targets, RF sputtering is more widely utilized to deposit various kinds of materials. For example, even though the target material is insulating, the charge build up phenomenon (on the target) would be minimized by using an RF alternating power. In addition, the ionization effect in the plasma would be greatly enhanced due to the rapid change in the electric field. Since the mass of an electron is about three orders lower than that of an ion, under the RF condition, the electrons can respond instantaneously to the rapidly changing electric field, while the ionized gas cations (e.g., Ar^+) are inertial. Therefore, the entire energy distribution of the electrons can be increased through the oscillation collisions, which further efficiently produces more Ar^+ ions. In addition, there is an automatically formed negative bias drop on the cathode (target).[92] The ion bombardment effect between the Ar^+ ion and target can be pronounced. Consequently, the enhanced ionization effect increases the feasibility of RF sputtering at a low working pressure (e.g., < 10 m Torr), which improves the sputtering efficiency because the sputtered target atoms can reach to the sample surface without being scattered.

Figure 16(a) shows the schematic configuration of the RF sputtering system utilized in this dissertation.[93] A matching box (L-type) that connects the RF generator and chamber is needed to fix the impedance mismatch among the RF generator, sputtering gun, and chamber, to reduce the power loss, i.e., making reflected power < 3 W.

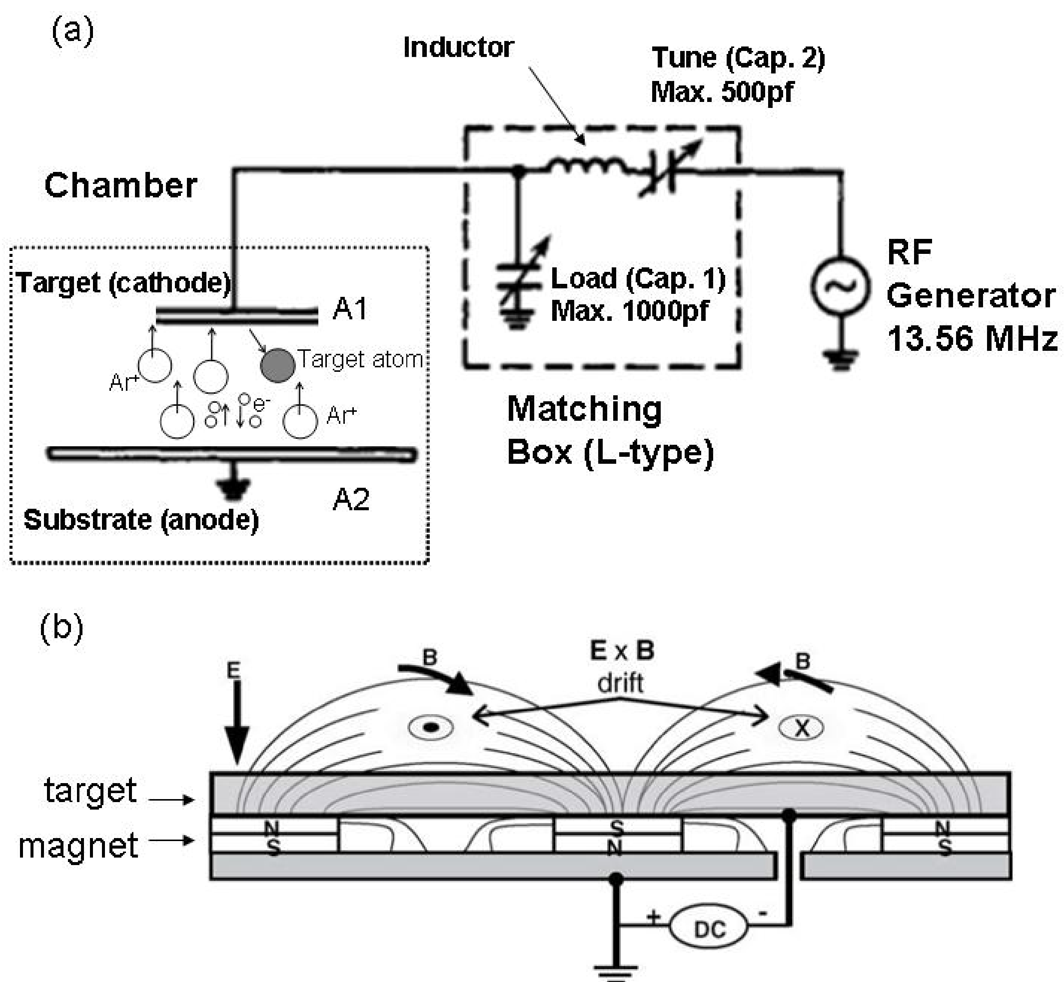

Figure 16. (a) Schematic configuration of RF sputtering system. (After Ref. 93) (b) Illustration of magnetron control.[94]

The matching box is consisted of two adjustable capacitors, i.e., load capacitor (Cap. 1, 1000 pf in maximum) and tune capacitor (Cap. 2, 500 pf in maximum), and one fixed inductor. By adjusting the load/tune capacitance, the impedance of the whole system can be matched to a certain value, e.g., 50 Ω for most common RF generators. In addition, for the RF sputtering system, the geometric system design is also very important. Since the capacitive potential of the powered area is different from that of the grounded area, the potential drop near the target (cathode) strongly depends on its area. This relationship can be expressed by the following equation:[95]

$$\frac{V_1}{V_2} = (\frac{A_2}{A_1})^N \qquad [7]$$

where V1 & A1 are the potential drop & area of the electrode 1, and V2 & A2 are the potential drop & area of the electrode 2, respectively. The N value is equal to 4 for the ideal RF sputtering system, while it is usually about 1 to 2 for the practical system.[95] Equation 7 indicates that for a RF sputtering system, the powered area (A1) must be smaller than the grounded area (A2), as shown in Fig. 16(a), to increase the potential drop on the target and simultaneously minimize the potential drop on the substrate. Under such design, the ion bombardment effect between the target and Ar^+ can be greatly enhanced to increase the sputtering efficiency, while the substrate (sample) would not be seriously damaged. On the other hand, the RF sputtering system utilized in this dissertation is also featured with the circularly-arranged magnetron control ability. A set of magnets are placed around the cathode area (i.e., behind the target) to provide the magnetic filed (B) perpendicular to the electric filed (E). Under this kind of field configuration, the electron movement would be confined into the E×B direction, and its movement path changes

from a linear to a spiral style. Therefore, the magnetron control confines the plasma above the target in annular rings, which enhances ionizing Ar atoms and in consequence, increases the sputtering efficiency. The concept of the magnetron control sputtering is illustrated in Fig. 16(b).

2.4 Material Properties Characterization

Material properties of the bulk high-k films and interface layers in the nanocrystals embedded high-k gate dielectric stack were investigated thoroughly in this dissertation. In addition, the profilometer (Veeco, Dektak^3 stylus) technique, which was used to measure the thickness and the area of the gate electrode pattern, will be also introduced. For precisely extracting the electrical characteristics of the MOS capacitor, the device's gate area is critical and needs to be measured carefully. X-ray diffractometry (XRD, Bruker, D8-Focus) was utilized to detect the crystalline structure of the bulk high-k films and nanocrystal layers. X-ray photoelectron spectroscopy (XPS, Kratos) was used to analysis the chemical bonding structures of the essential elements in the bulk high-k films and in the interface layers. High-resolution transmission electron microscope (HRTEM, JEOL, JEM-2010) was utilized to investigate the subtle material properties in the nanoscale, i.e., ultra-thin film thickness determination, interface layer formation, and discrete nanocrystals identification. Moreover, the energy dispersive spectroscopy (EDS, Oxford Instrument) and select area diffraction (SAD) methods associated in the same TEM instrument were utilized to study the chemical component and crystalline structure of the specific layer. The background knowledge of each material characterization will be also introduced in this section.

2.4.1 Profilometer

The vertical profile of a sample surface can be obtained by the profilometer technique that utilizes a diamond stylus to horizontally scan the sample surface. From the vertical profile, the thickness and diameter of the gate electrode pattern can be precisely determined. During the horizontal scan, the stylus was kept distant to the sample surface by a contact force. This force is in the micron newton (mN) range and can be maintained as constant due to the cantilever system operating on the spring mechanic principle. The resolution in the horizontal direction is governed by the scan speed and stylus radius, while that in the vertical direction is governed by the stylus radius and cantilever system. The profilometer utilized in this dissertation has a stylus radius of 5 μm and a resolution of 1 nm.

2.4.2 X-Ray Diffractometry (XRD)

The crystalline structure information of the high-k films and nanocrystal layers, such as the structure phase, preferred orientation, crystallinity, and grain size in average, can be obtained by using XRD analysis. For the high-k gate dielectric study, XRD can be also used to determine the onset of the high-k film's amorphous-to-crystalline transit temperature. The XRD instrument utilized in this dissertation adopts the monochromatic Cu Kα X-ray (λ= 1.5418 Å). Figure 17 illustrates the XRD analysis.[96] After the Cu Kα X-ray impinges the sample with an incident angle (θ), the x-ray can be reflected by the crystalline planes. The reflected X-rays from the two consecutively parallel crystalline planes can form the constructive or destructive interference. Only the former can be detected by the scintillation detector, which reflects a XRD peak in the XRD pattern.

Judged from the XRD pattern and referred XRD peaks to the Joint Committee on Powder Diffraction Standards (JCPDS) database, the sample's crystalline structure, phase, and orientation can be determined. The condition to form the constructive interference must meet the Bragg's law, i.e.,

$$2d \sin \theta = n\lambda \quad [8]$$

where d is the spacing between the two consecutively parallel crystalline planes, n is an integer, and λ is the wavelength of the Cu Kα X-ray (1.5418 Å). In addition, the averaged grain size (thickness) of each orientated grain (crystallite) in the polycrystalline sample can be also calculated from the XRD peak's location and full width at half maximum (FWHM) by the Scherrer equation,[97] i.e.,

$$t = \frac{0.9\lambda}{B \cos \theta} \quad [9]$$

where t is the averaged grain size, λ=1.5418 Å, θ corresponds to the half of the peak location (2θ), and B is the peak's FWHM in radiant unit.

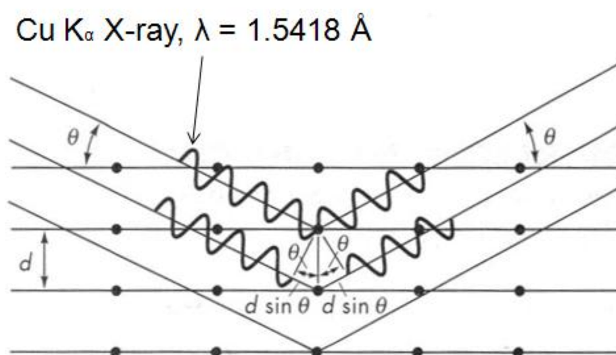

Figure 17. Illustration of XRD analysis. (After Ref. 96)

2.4.3 X-Ray Photoelectron Spectroscopy (XPS)

The chemical bonding structures of the bulk high-k films, nanocrystal layers, and Si/ZrHfO interface layers were investigated by the XPS analysis in this dissertation. Figure 18 illustrates the principle of the XPS analysis.[98] When the incoming monochromatic Al X-ray (Kα, 1486.6 eV) impinges the sample, the core level electrons can absorb the X-ray energy and then emit out of the sample. The emitted electron is also called photoelectron, which has a kinetic energy (KE). Therefore, the bind energy (BE) of the core level electron can be estimated from the following equation:

$$BE = h\upsilon - KE - \varphi \qquad [10]$$

where $h\upsilon$ is the X-ray energy (Al Kα, 1486.6 eV), and ϕ is the work function of the spectrometer, which is usually in the range of 3-4 eV. KE of the emitted photoelectron can be detected by the analyzer. Since the different bonding states of the core level electrons correspond to the different binding energies, the chemical bonding states of an element can be determined by comparing the binding energy shift. Therefore, the element either in the neutral molecular state or in the charged compound state can be distinguished. However, XPS technique still has some drawbacks, e.g., the relatively big X-ray spot (i.e., poor spatial resolution ~1 cm^2) and low detection sensitivity (atomic concentration limitation > 0.5 %). In addition, due to the short mean free path of the emitted electron, XPS technique only can provide the chemical information at near surface region, i.e., about 10 nm depth. Moreover, the charge accumulation effect should be taken into account because in this dissertation, many investigated thin films are not conductive. Therefore, the detected XPS spectrum needs calibration to truly represent the chemical bonding information. The carbon (C) 1*s* peak at 284. 8 eV, which is related to

the common environmental contamination, is usually used as the calibration reference. Also, the referenced peak can be the Si 2*p* peak at 99.3 eV, which is related to the bottom Si wafer. On the other hand, the peak deconvolution is usually required to separate several similar bonding states that generally have peaks close to each other. In this dissertation, XPS peak41 software was used to carry out the peak deconvolution process based on the Shirley/linear background adjusting and Gaussian/Lorentzian functions. In addition, for a dielectric material, its XPS O 1*s* energy loss spectrum can be used to extract the band gap.[99] The energy band gap of the high-k ZrHfO film and Ru-modified ZrHfO film were determined by this method, which will be shown in Chapter III.

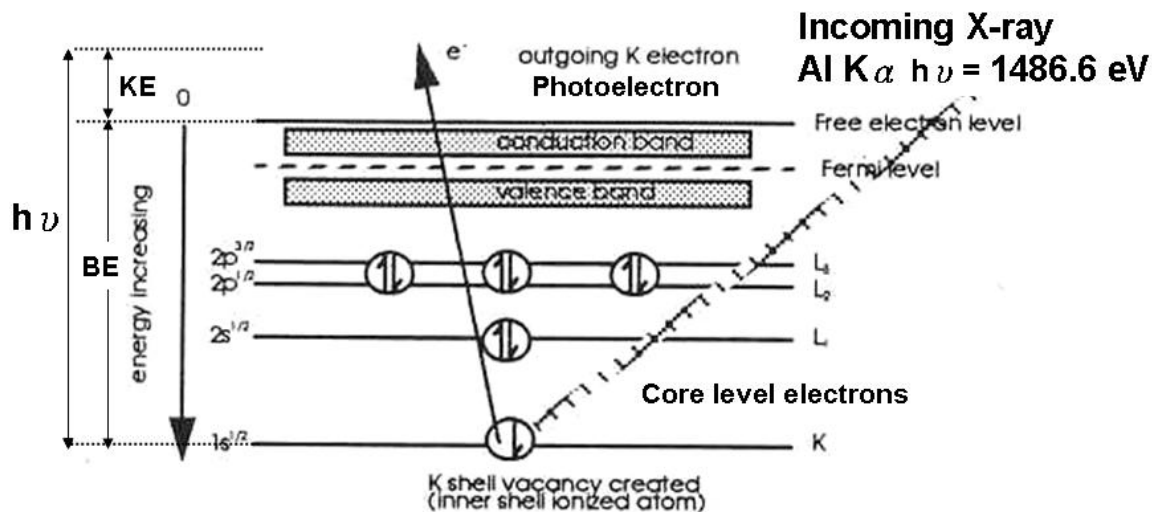

Figure 18. Illustration of XPS analysis. (After Ref. 98)

2.4.4 High-Resolution Transmission Electron Microscope (HRTEM)

In this dissertation, HRTEM technique was utilized to characterize the subtle material properties of the bulk high-k films, Si/ZrHfO interface layers, and embedded nanocrystal layers. Since all above layers in the high-k gate dielectric stack are ultra-thin, i.e., < 10 nm, it is critical to investigate each layer thickness and to identify the discrete nanocrystals embedded in the bulk ZrHfO film.

Figure 19 shows the schematic diagram of the HRTEM system (JEOL, JEM 2010) utilized in this dissertation.[100] Electrons are generated from the lanthanum hexaboride (LaB_6) filament by the thermo-ionic emission mechanism. Then, the electrons are accelerated by a 200 kV voltage, which produces a very short wavelength, i.e., ~ 0.006 nm. The specific ~ 0.23 nm point resolution can be achieved in the JEM 2010. The accelerated electrons are focused on the sample by the two condenser lens. Due to the very thin sample thickness, e.g., < 50 nm, the electrons can transmit through the sample to form the diffraction pattern on the back focal plane. Since the diffraction phenomenon is strongly affected by the sample's crystalline characteristics, the select area diffraction (SAD) pattern can be used to investigate the structural information. By the projector lens, the magnified TEM image can be projected on the image plane based on the transmission electrons. This kind of imaging mode is called "bright-field" due to the high energy nature of the transmitted electrons. On the other hand, the image formed based on the scattered electrons is called "dark-field" due to the relative low energy of the scatter electrons. The image contrast is contributed by many parameters, such as the mass contrast, thickness contrast, diffraction contrast, and phase contrast.[101] In this dissertation, all TEM micrographs were recorded with the bright-field imaging mode. In addition, the

energy dispersive spectroscopy (EDS) associated in the same TEM instrument, i.e., from the same electron beam, was utilized to study the component information of the specific layer in the high-k gate dielectric stack.

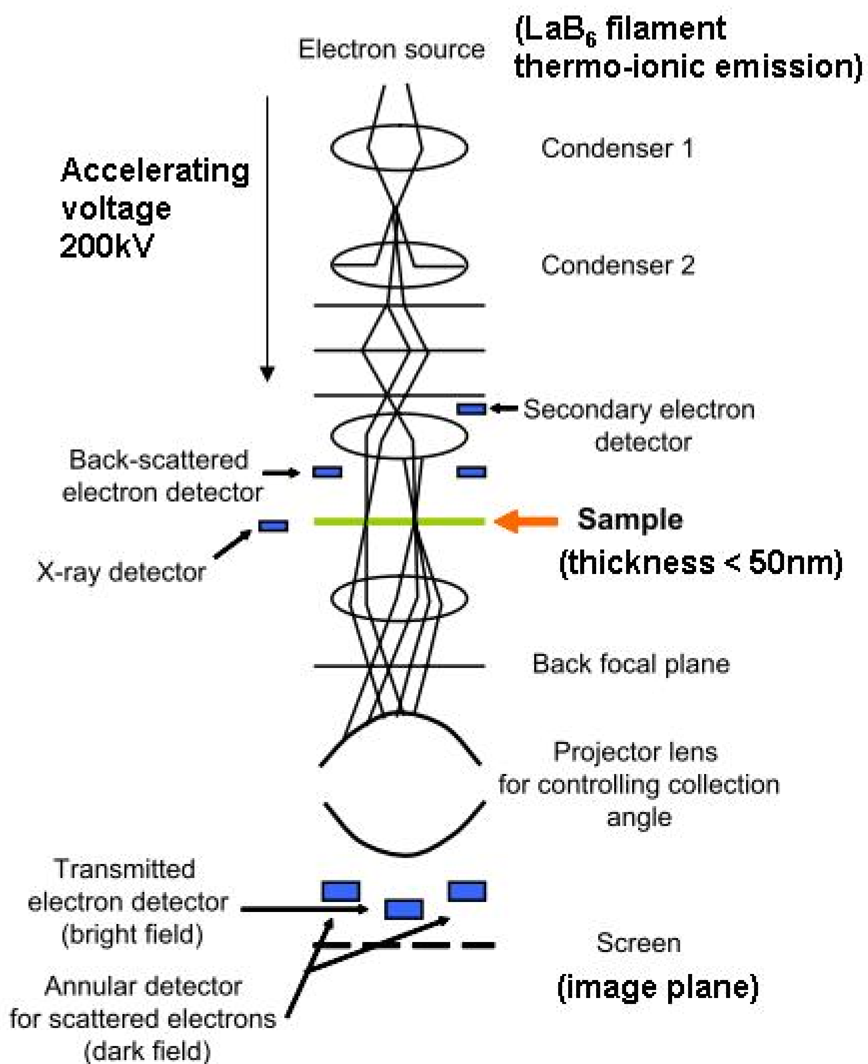

Figure 19. Schematic diagram of TEM. (After Ref. 100)

2.5 Electrical Properties Characterization

Electrical characterizations of the Ru-modified and nanocrystals embedded ZrHfO high-k MOS capacitors, e.g., high frequency (100 kHz to 1 MHz) capacitance-voltage (C-V) and current density-voltage (J-V) measurements, were performed to investigate the gate dielectric properties and nonvolatile memory functions. Since the size of the capacitor is very small, i.e., in the range of 4.91×10^{-6} cm^2 to 7.85×10^{-5} cm^2, the measured electrical signals can be very weak. For example, the measured capacitance can be as small as 10^{-12} F, and the current density can be as small as 10^{-9} A/cm^2. Therefore, the entire measurement process should be carried out very carefully, and be insulated from the outside environment disturbance, such as lights, noises, heats, and vibrations.

2.5.1 Electrical Characterization System Setup

Figure 20 shows the entire electrical characterization system setup in this dissertation. The measurement was performed on the probe station (Signatone, S-1160) in the grounded Al box. All the Al box's surfaces are painted to flat black in order to avoid any light radiation. The sample was placed on the gold alloy-plated chunk, which can be vacuumed for preventing from the sample shock during the measurement, and be heated for the temperature-dependent electrical characterizations. In addition, the chunk was used to receive the measured signals from the backside of the Si substrate, therefore, it should be electrically floated to prevent from driving signals to the ground. The measurement probe tip is made of tungsten, and has a diameter of 1 μm. High frequency C-V and J-V curves were measured with the Agilent 4284A LCR meter and the Agilent 4155C semiconductor parameter analyzer, respectively. The triaxial cables (for C-V) and

biaxial cables (for J-V) were used to connect the measurement instrument and probe station in a way of minimized electrical interference and signal loss. The National Instruments Labview 7 program was used to control the whole measurement process through the GPIB interface.

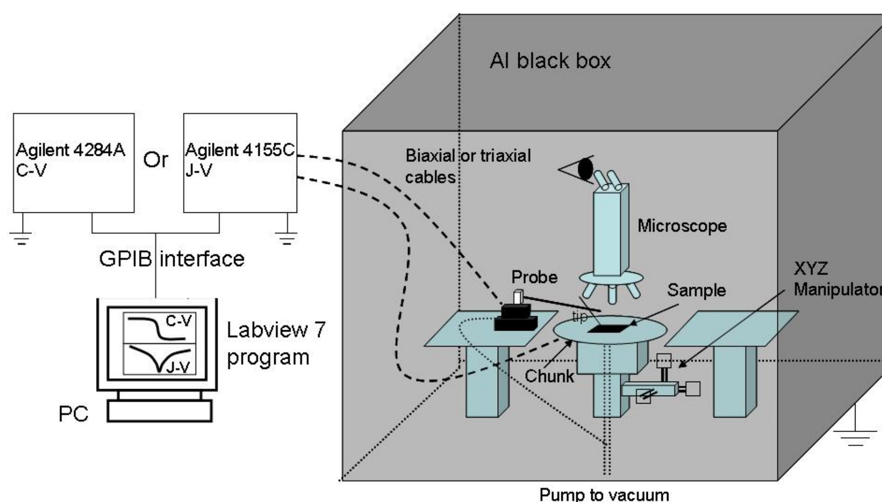

Figure 20. Schematic diagram of electrical characterization system setup.

2.5.2 High Frequency C-V Curve Measurement

The high frequency C-V curves of the ZrHfO high-k MOS capacitors were characterized in this dissertation. Many critical electrical properties of the device, such as EOT, flat band voltage (V_{FB}), density of the fixed charges, interface states, and mobile ions, can be extracted from the high frequency C-V curve.[100] Also, the inversion capacitance can reflect the doping concentration in the Si wafer. Moreover, from the frequency-dependent (100 kHz to 1 MHz) C-V measurements, the defects either in the

bulk high-k film or at the corresponding interfaces can be determined. The principle of the C-V measurement is to use a linear DC bias swept in the desired gate voltage range, and simultaneously a high frequency small (0.25 V) sinusoidal AC voltage signal is superimposed to extract the differential capacitance (C') and the conductance (G). C' and G can be expressed as Eqs. 11 and 12, respectively.

$$C' = \frac{dQ}{dV} \quad [11]$$

$$G = \frac{dI}{dV} \quad [12]$$

Usually, the CPG mode, i.e., C and G are parallel to each other in the G-C circuit, is selected to perform the high frequency C-V measurement. By measuring the impedance of the parallel G-C circuit, i.e., ratio of the output AC current to the input AC voltage, the capacitor's G and C values can be obtained at the same time.[100] The impedance (Z) of the G-C circuit can be expressed as:[100]

$$Z = \frac{G}{G^2 + (\omega C)^2} - \frac{j\omega C}{G^2 + (\omega C)^2} \quad [13]$$

where ω is the angular frequency, i.e., 2π f, and f is the frequency of the superimposed AC voltage signal. Another important concern to correctly measure the C-V curve is how to minimize the series resistance that unavoidably exists in the measurement system. The series resistance is contributed by many causes, such as the poor contact at the gate electrode/probe tip or at the Si substrate/chuck. Due to the series resistance, the AC voltage signal may suffer energy loss, which consequently deteriorates the accuracy of the C-V measurement.[102] In order to minimize the series resistance, except physically improving the good electrical contacts, the separate correction processes in the "open"

mode (i.e., no contact between the probe tip and chunk) and in the "short" mode (i.e., the probe tip and chunk contact each other) were developed.[25] On the other hand, since the high-k film can be very thin, i.e., < 3 nm, for the low EOT study, the conventional C-V measurement method should be modified to fix the issues contributed by the high gate leakage current.[103] Plus, the carrier confinement (quantum mechanical) effects on the Si wafer surface should be also considered. Figure 21 shows the two major quantum mechanical effects:[103] (a) the confined surface carriers in the localized energy levels above the conduction band edge may cause an additional band bending, i.e., Δε, and (b) the charge centroid may shift into the Si wafer further from the surface than the conventional theory predicts, i.e., ΔZ. In consequence, a depletion region may be formed at the Si/gate dielectric interface to result in the decrease of the measured capacitance.[103]

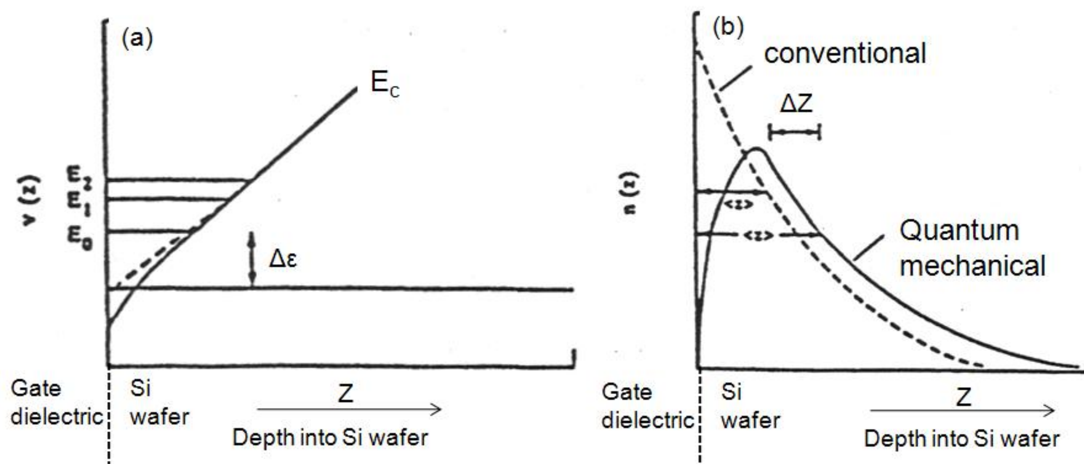

Figure 21. Quantum mechanical effects occur at Si wafer/gate dielectric interface: (a) band bending Δε and (b) charge centroid shift ΔZ. (After Ref. 103)

Recently, Hauser *et al.*[103] of North Carolina State University have proposed a simple model to appropriately correct the measurement errors raised from the above quantum mechanical effects. Their approach was based on the approximations[104] such as (1) the total Si wafer surface potential is a combination of the classical result and $\Delta\varepsilon$, and (2) the total Si wafer bulk charges should include the additional amount due to the corresponding charge centroid shift ΔZ. Their model predicts that $\Delta\varepsilon$ has a 2/3 power dependence on the surface electric field to achieve the lowest quantized energy level. Also, it was reported that ΔZ is a relatively constant of about 1.2 nm.[105] By using their model, or so called "NCSU CVC" program, the V_{FB} and oxide trapped charge density can be appropriately extracted from the measured C-V curve.

2.5.3 J-V Curve Measurement

The gate leakage J-V measurements were performed on the ZrHfO high-k MOS capacitors in this dissertation. The current transport mechanism and charge trapping/detrapping phenomena in the nanocrystals embedded ZrHfO high-k gate stack can be also characterized from the J-V curve. Moreover, with applying a gate voltage constantly, the high-k gate dielectric stack may breakdown and therefore, its reliability characteristics can be investigated. Benefited from the feasibility of the heated chunk, the carrier transport mechanisms through the high-k stack can be also studied. The Agilent 4155C semiconductor parameter analyzer was utilized to measure J-V curves. The basic principle of the J-V measurement is to apply a DC bias on the capacitor via the probe tip, and then receive the current signals from the same probe tip. The voltage profile of the DC bias can be either in the ramp mode or in the stepwise mode. For the ramp mode, the

measured current may be contributed by the gate leakage current and displacement current. In order to minimize the latter, therefore, the DC bias ramping with a very slow speed, i.e., 0.01 V/s, is usually used.[106] For the stepwise mode, a relatively long delay time between each step, e.g., about 500 ms, can be also adopted to achieve the same purpose.[106] However, it should be noted that this delay time can not be too long because the DC bias during such long delay time may induce a high gate leakage current, which degrades the dielectric properties.

CHAPTER III

RUTHENIUM-MODIFIED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K GATE DIELECTRIC FILM WITH LOW EQUILVALENT OXIDE THICKNESS*

3.1 Introduction and Motivation

The Zr-doped HfO_2 film (ZrHfO) has been demonstrated that has excellent dielectric properties, e.g., a low EOT, a low leakage current, a low interface state density, a high amorphous-to-polycrystalline transition temperatures, and good reliability.[107-109] When ZrHfO is used as the gate dielectric of the MOSFET, it shows excellent transistor characteristics, such as a high transconductance, a high drive current, and a low threshold voltage.[110] On the other hand, the high-k thin films can be prepared by many different methods, such as the atomic layer deposition, chemical vapor deposition, and sputtering.[27,29,108] Sputtering, which is a well-developed method in the ULSI industry, can be used to deposit films with various types of compositions and structures. The room temperature deposited high-k film needs to be annealed at a high temperature to reduce the defect density, which is critical for the gate dielectric application. However, after thermal annealing, a low quality interface layer is often formed between the high-k film and Si substrate, which drastically decreases the effective k value.

*Part of data reported in this chapter is reproduced from "Ruthenium Modified Zr-Doped HfO_2 High-k Thin Films with Low Equivalent Oxide Thickness", by Chen-Han Lin and Yue Kuo, *Journal of The Electrochemical Society*, 158(7), G162-G168 (2011), by permission of ECS-The Electrochemical Society.

It has been reported that the dielectric film's permittivity could be increased by dispersing metal particles into the structure.[46-47] The conductive particles could behave as induced dipoles or carrier trapping sites to enhance the dielectric constant. In this work, authors modified the ZrHfO film by including ruthenium (Ru) or ruthenium oxide (RuO_x) into the structure and investigated its influence on the film's material and electrical properties. Ru and RuO_x are selected in this study because they are stable conductors with high work functions (~5 eV),[111] which can provide a high density of states around the Fermi energy level for carrier trapping.[60] Ru and RuO_x have been used as the metal gate electrodes in MOSFETS for their excellent thermal stability and chemical properties.[112] However, during high temperature annealing, they may react with HfO_2[42] or diffuse to the HfO_2/Si interface to form Ru-silicide,[44] which may change the device's electrical characteristics.

3.2 Experimental

MOS capacitors containing ZrHfO and Ru-modified ZrHfO (abbreviated as Ru-ZrHfO from now on) films were fabricated on the p-type Si (100) wafer (doping concentration at 10^{15} cm^{-3}) that was pre-cleaned with a dilute hydrofluoric acid (DHF) solution. The ZrHfO film was deposited from a Hf/Zr (88:12 wt %) composite target by reactive sputtering for 20 seconds. The Ru-ZrHfO film was prepared by sequential sputter depositions of the ZrHfO (10 seconds)/Ru (10 seconds)/ZrHfO (10 seconds) in one pumpdown without breaking the vacuum. All sputtering processes were carried out at 100 W in a 1:1 Ar/O_2 atmosphere at 5 mTorr with a total flow rate of 40 sccm. The backside of the target was water cooled. The post-deposition annealing (PDA) step was

done by rapid thermal annealing (RTA) at 800 °C to 1000 °C for 10 seconds in a N_2/O_2 (20:1) atmosphere. The 80 nm thick titanium nitride (TiN) gate electrode was deposited by sputtering from a Ti target in the Ar/N_2 (50:1) gas at 100 W for 40 minutes. The post metal deposition annealing (PMA) step was carried out at 350 °C for 5 minutes in the forming gas H_2/N_2 (10:90) ambient. The gate pattern (100 μm diameter) was defined with lithography and was wet etched with the NH_4OH: H_2O_2: H_2O (1:1:5) solution. The backside of the Si wafer was cleaned with a DHF solution followed by the aluminum (Al) deposition. The final annealing step was done by RTA at 250 °C for 1 minute in forming gas. Figure 22 shows that in general, the ZrHfO sample showed improved gate dielectric properties with increasing the PDA temperature. For example, the capacitor's EOT and C-V hysteresis can be decreased when the PDA temperature became higher. Also, the flat band voltage (V_{FB}) shifted to a lower negative magnitude. The improved gate dielectric properties can be attributed to the better bulk high-k film quality, i.e., denser film structure and less inherent trapped charge density. Therefore, the Ru modification effects were investigated only for the 1000 °C-annealed samples in this study. The high-k film's bulk and interface layer (IL) properties were examined with the high resolution transmission electron microscopy (HRTEM) and angle resolved x-ray photoelectron spectroscopy (ARXPS). The MOS capacitor's capacitance-voltage (C-V), conductance-voltage (G-V), and current density-voltage (J-V) characteristics were measured with the Agilent 4284A LCR Meter and Agilent 4155C semiconductor parameter analyzer. The EOT of the high-k stack was calculated from the capacitance measured at the gate voltage (V_g) of -3 V. The V_{FB} was extracted from the C-V curve using the NCSU CVC program. [103] All electrical measurements were performed on the probe station in the black box.

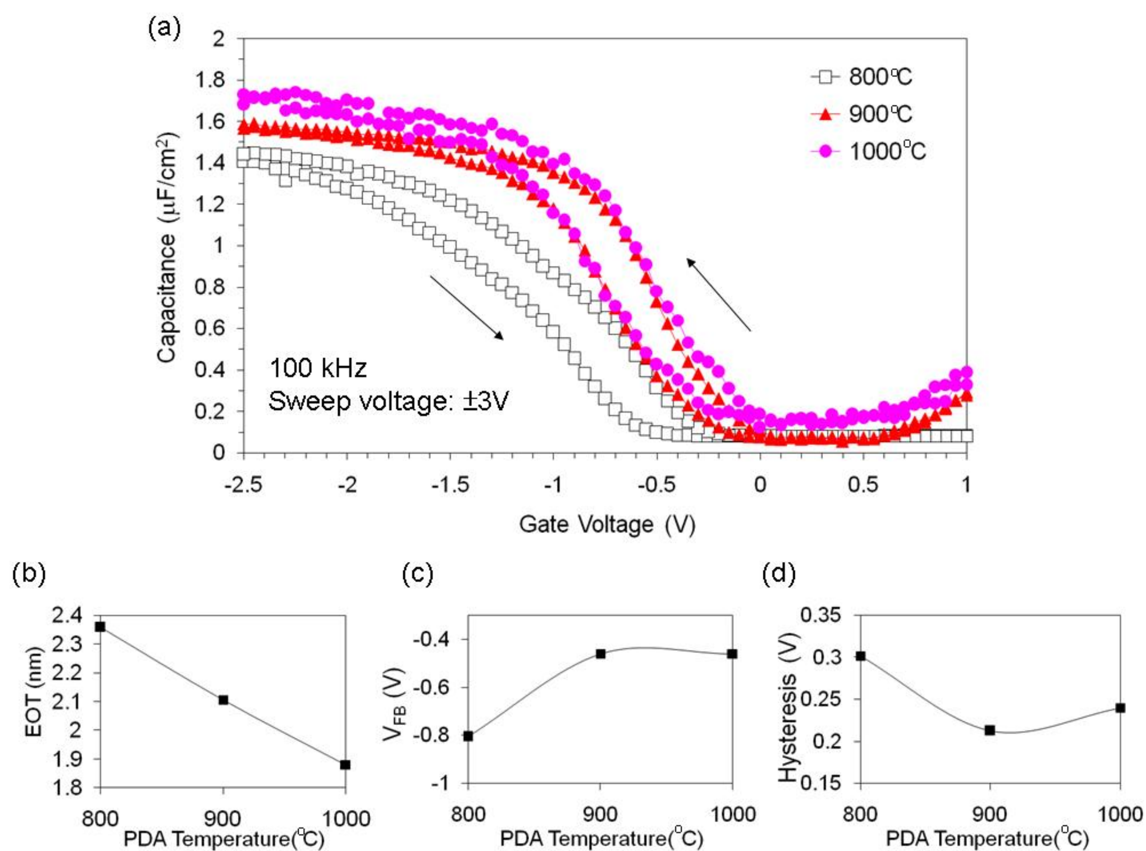

Figure 22. (a) C-V hysteresis curves (measure at 100 kHz) of the ZrHfO sample annealed at 800 °C to 1000 °C for 10 seconds in a N_2/O_2 (20:1) atmosphere. Corresponding gate dielectric properties, i.e., (b) EOT, (c) V_{FB}, and (d) hysteresis as a function of PDA temperature.

3.3 Ru Modification Effects on Material Properties of ZrHfO High-K Gate Dielectric Film

3.3.1 Physical and Chemical Properties of Bulk ZrHfO High-K Film and Interface Layer with Inclusion of Ru Nanoparticles

Figure 23 shows the cross-sectional HRTEM views of the (a) ZrHfO and (b) Ru-ZrHfO films on the Si wafer. The bulk ZrHfO film is about 3 nm thick and amorphous. Therefore, the properly Zr doped HfO_2 film can withstand the 1000 ^oC annealing condition without crystallization. The homogeneous amorphous film is less prone to current leakage than the polycrystalline film. An interface layer (IL ~ 2.2 nm) is formed between ZrHfO and Si due to the reaction among Si, O and Hf atoms. It has a Hf-silicate ($HfSiO_x$) structure, which will be discussed later. The bulk Ru-ZrHfO film is much thicker than the bulk ZrHfO film, i.e., 6.5 nm vs. 3 nm. The exact reason why the Ru-ZrHfO film thickness is more than twice of that of the control sample is not clear. There are several possibilities. For example, the introduction of the Ru layer contributes to the thickness increase. The thickness of the two separate 10-sec sputtered ZrHfO films may be larger than that of the 20-sec sputter deposited film. Also, part of the as-deposited Ru may be oxidized during the top ZrHfO deposition. There is a small number of separately-spread lattice fringes with spacing ~ 0.205 nm in the film, which can be contributed to the Ru (101) crystal.[113] The interface layer of the Ru-ZrHfO sample is slightly larger than that of the ZrHfO sample, i.e., 2.4 nm vs. 2.2 nm. It may be due to the process variation. However, since these two interfaces have different structures, which will be discussed later in this chapter, it may also be contributed by the additional Ru in the former.

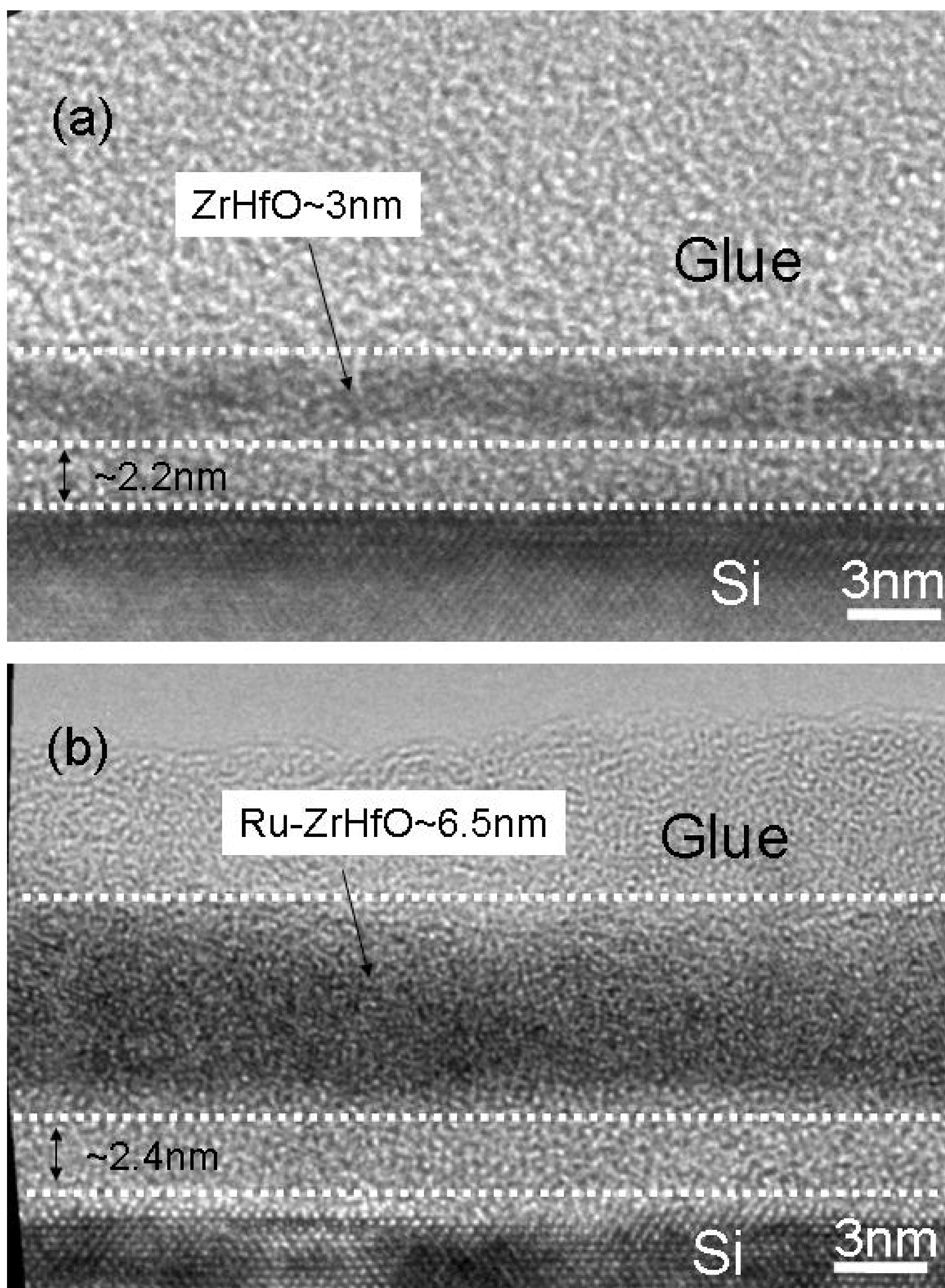

Figure 23. HRTEM cross-sectional views of (a) ZrHfO and (b) Ru-ZrHfO films on Si.

Figure 24 shows the top-view TEM micrographs of (a) ZrHfO and (b) Ru-ZrHfO films and corresponding selected area diffraction (SAD) patterns. It confirms that the ZrHfO film has a continuous and amorphous structure and the Ru-ZrHfO film contains discrete nanodots distributed in an amorphous matrix. The SAD pattern corresponds to the Ru (101) crystalline structure. From Fig. 24(b), the size of discretely-dispersed Ru dots is in the range of 2.5 nm to 5 nm and its two dimensional density is estimated to be ~ 7×10^{11} cm^{-2}.

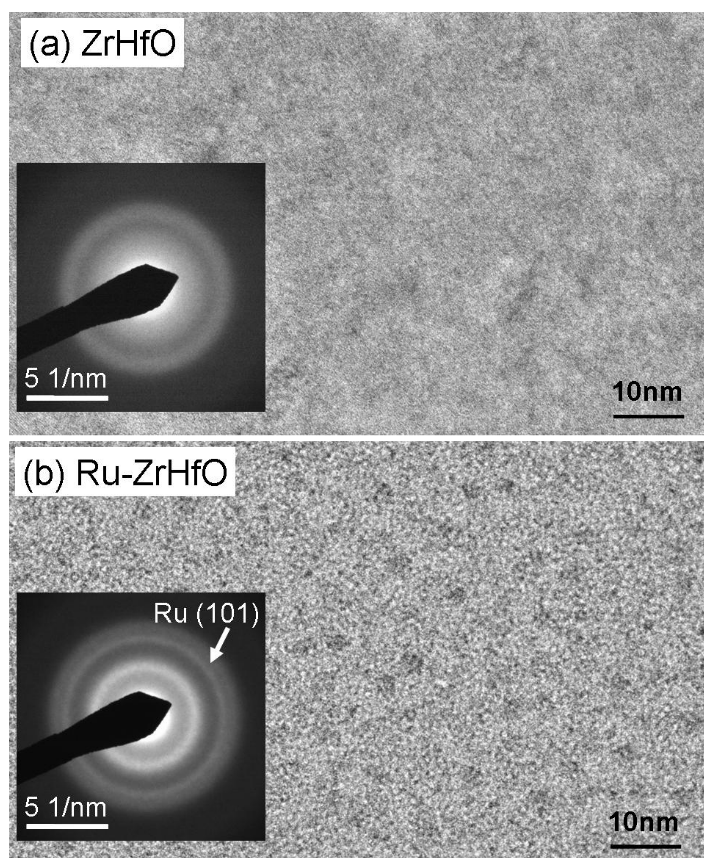

Figure 24. HRTEM top views of (a) ZrHfO and (b) Ru-ZrHfO films. Insets: corresponding SAD patterns.

Figure 25 shows XPS Ru 3*d* core level spectra of the ZrHfO and Ru-ZrHfO samples. Both samples were pre-sputtered in the XPS chamber by Ar^+ ions (at 500 eV) for 35 seconds to remove possible surface contaminants. Apparently, Ru $3d_{3/2}$ and Ru $3d_{5/2}$ peaks are absent in the ZrHfO sample. The Ru-ZrHfO sample contains a peak with the binding energy (BE) 280 eV corresponding to the Ru-Ru metallic state. The broadening of the peak may be due to the existence of a small amount of RuO_2.[114] The inset in the figure shows the deconvolution of the Ru 3*p* peak, which has s small portion of RuO_2 (about 6.9 %). Therefore, Ru in the ZrHfO film mainly remains in the metallic state with minor portion in the oxidized state.

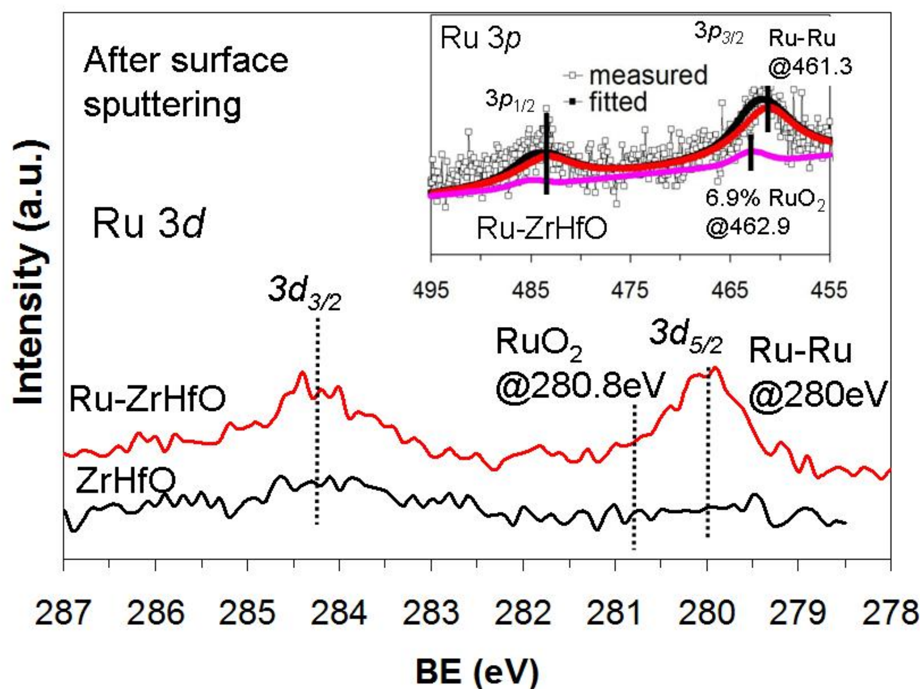

Figure 25. Ru 3*d* XPS spectra of ZrHfO and Ru-ZrHfO samples. Inset: deconvoluted Ru 3*p* spectrum of Ru-ZrHfO sample.

Figure 26 shows XPS spectra of (a) Hf 4*f*, (b) Zr 3*p*, and (c) O 1*s* in the ZrHfO and Ru-ZrHfO samples. There is no obvious difference in Hf 4*f* and Zr 3*p* peak locations in these samples. The Hf $4f_{7/2}$ peak at BE around 17.2 eV indicates possible existence of both HfO_2 and $HfSiO_x$.[18] The Zr $3p_{3/2}$ peak at BE around 333.2 eV is from ZrO_2. No peaks corresponding to Zr-silicate were detected. Therefore, the inclusion of Ru in the ZrHfO film does not affect the chemical bonding states of Hf and Zr. However, the O 1*s* peak in the Ru-ZrHfO sample has a higher BE than that in the ZrHfO sample, i.e., 532 eV vs. 531.6 eV. This means the former probably contains SiO_x group close to the SiO_2 structure while the latter does not. In addition, the energy band gap of the ZrHfO and Ru-ZrHfO samples can be extracted from their O 1*s* energy loss spectra,[99] as shown in Fig. 27. From the onset of the loss peak increase, i.e., the threshold energy of the energy loss spectrum, E_g of the ZrHfO sample and the Ru-ZrHfO sample can be determined to be about 6 eV and 5.8 eV, respectively. The latter shows a lower E_g because it contains RuO_2 that has a relatively low band gap, i.e., ~2.9 eV.[115]

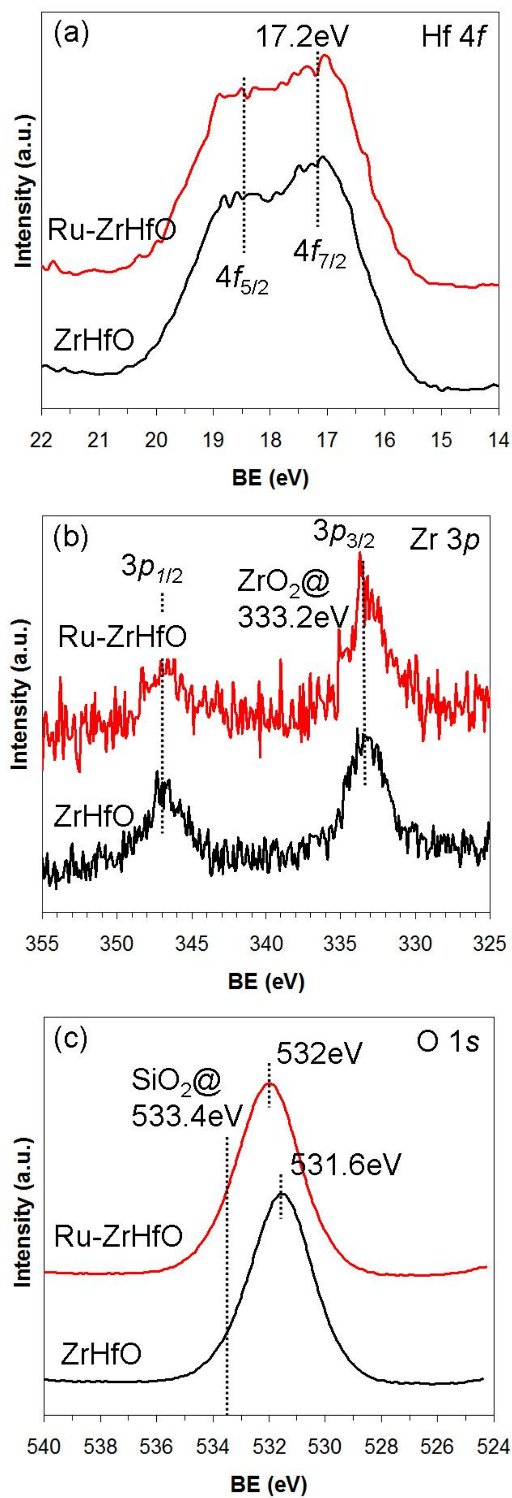

Figure 26. (a) Hf 4*f*, (b) Zr 3*p*, and (c) O 1*s* XPS spectra of ZrHfO and Ru-ZrHfO samples.

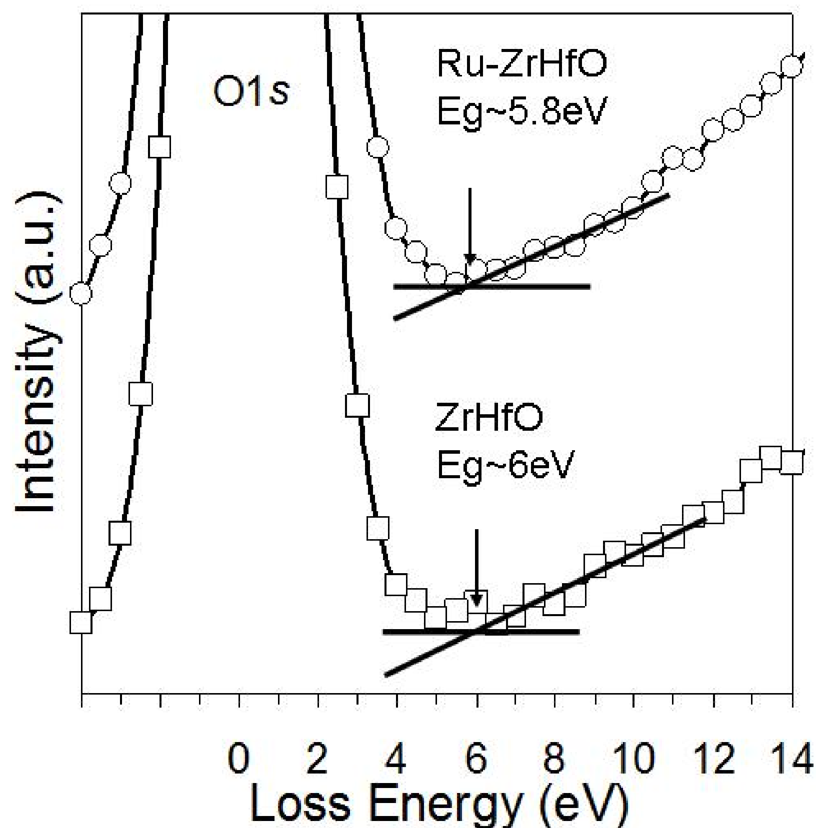

Figure 27. O 1*s* energy loss spectra of ZrHfO and Ru-ZrHfO samples.

3.3.2 Composition Change of Interface Layer with Inclusion of Ru Nanoparticles

Figure 28 shows Si 2*p* peaks of (a) ZrHfO and (b) Ru-ZrHfO samples. Both samples contain Si 2*p* peaks at 99.3 eV and below 103.4 eV. The former is attributed by the Si-Si bonding state from the Si substrate. The shoulder peak at 99.8 eV is the spin-orbit-split of the Si $2p_{1/2}$, which is often observed with the high resolution XPS instrument.[116] The Si 2*p* peak in the Ru-ZrHfO sample has a higher BE than the ZrHfO sample has, i.e., 102.8 eV vs. 102.4 eV. Again, this is another indication that the interface layer of the Ru-ZrHfO sample contains more SiO_2-like component than the ZrHfO

sample does. For the ZrHfO sample, the broad Si 2*p* peak at BE ~ 102.4 eV can be deconvoluted into two sub-peaks, i.e., that at 102 eV corresponding to HfO_2-rich $HfSiO_x$ (about 40.3 %) and that at 102.8 eV corresponding to SiO_2-rich $HfSiO_x$ (about 59.7 %).[21] However, for the Ru-ZrHfO sample, the 102.8 eV peak can be deconvoluted into three sub-peaks, i.e., the previous two peaks plus an additional peak at 103.4 eV corresponding to SiO_2 (about 18.3 %). Therefore, the ZrHfO/Si interface is modified with the inclusion of Ru in the bulk film. It was reported that for the sputter deposited HfO_2 film after the high temperature RTA treatment, it could be decomposed to form excessive oxygen vacancies (V_o) and Hf-dangling bonds.[117] Hakala *et al*[118] reported that Hf was diffused to the Si interface to form the Hf-Si bond to passivate the Hf-dangling bonds. Since the ZrHfO film in this study was prepared under the similar condition as that of Ref. 117, it probably contains V_o and Hf-dangling bonds as well as $HfSiO_x$ at the interface. On the other hand, for the Ru-ZrHfO sample, the Hf-dangling bonds may be compensated by forming Ru-Hf or Ru-V_o-Hf bond similar to the Pt-Hf or Pt-V_o-Hf bond reported in the literature.[119-120] The inclusion of Ru in the film may reduce the V_o density and the Hf diffusion process, which explains the formation of the SiO_2-like composition at the interface. The above result is consistent with the O 1*s* peak change shown in Fig. 26(c). The Ru-ZrHfO sample has a higher O 1*s* BE than the ZrHfO sample.

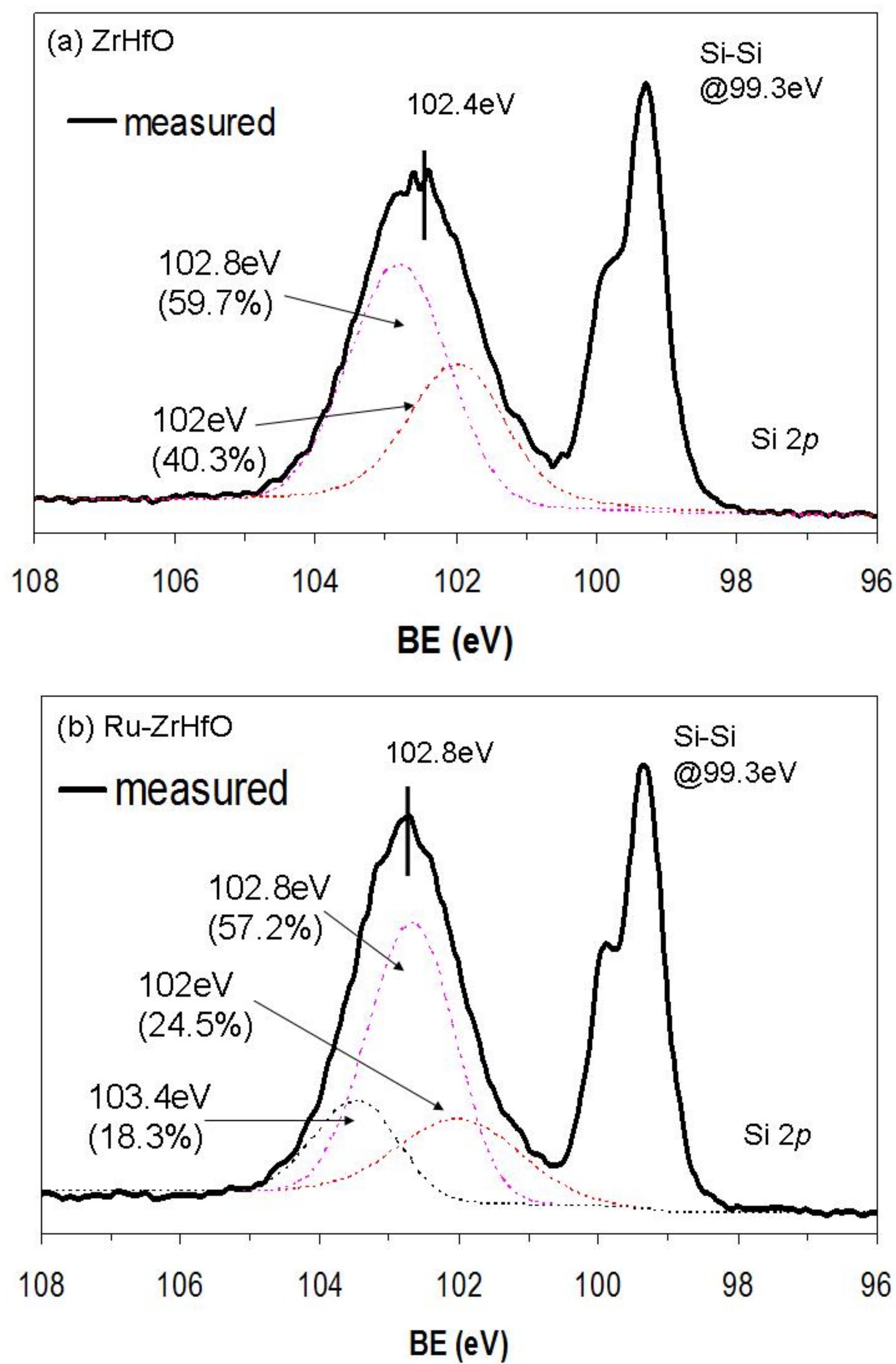

Figure 28. Si 2*p* XPS spectra of (a) ZrHfO and (b) Ru-ZrHfO samples. 102.4 eV peak in (a) deconvoluted into 102. 8 eV and 102 eV peaks; 102.8 eV peak in (b) deconvoluted into 102.8 eV, 102 eV, and 103.4 eV peaks.

3.4 Ru Modification Effects on Electrical Properties of ZrHfO High-K MOS Capacitor

3.4.1 Change of C-V and G-V Characteristics with Inclusion of Ru Nanoparticles

Figure 29 shows C-V hysteresis curves of the MOS capacitors containing ZrHfO and Ru-ZrHfO films, separately. The gate voltage was swept from -3 V to +3 V (forward) and back to -3 V (backward). Both samples show counter-clockwise hysteresis. The separation of the forward and backward curve indicates that charges were trapped in the V_g sweeping process. The capacitance in the accumulation region was increased after the inclusion of Ru in the ZrHfO film. The EOT of the ZrHfO sample is 1.88 nm and that of the Ru-ZrHfO sample is 1.43 nm. The TEM micrographs in Fig. 23 shows that, compared with the ZrHfO sample, the Ru-ZrHfO sample has a thicker bulk layer (~ 6.5 nm vs. ~ 3 nm) but a comparable interface layer (~ 2.4 nm vs. ~ 2.2 nm). Therefore, the high capacitance of the former is contributed by the increase of bulk film's permittivity. This is consistent with the theory that the film's dipole can enhance the dielectric constant.[47] By assuming that the interface layers (with Si) of the both ZrHfO and Ru-ZrHfO samples have the same dielectric constant of 7.5, which is the typical value of $HfSiO_x$,[121-122] the dielectric constants of the bulk ZrHfO and Ru-ZrHfO films are 15.9 and 139.3, respectively, measured at 100 kHz. In addition, the small amount of the conductive Ru/RuO_2 nanoparticles in the ZrHfO film could serve as quantum trapping centers to trap carriers through tunneling from the Si substrate. The trapped charges may induce the dipole polarization effect to increase the capacitance. Similar phenomenon was observed in the silver nanoparticles embedded aluminum oxide.[46] The dipole enhancement effect is further supported by the existence of a hump in the Ru-ZrHfO sample's C-V curve. This hump emerges at near -0.5 V, which is lower than its flatband voltage near 0 V.

Previously, it was shown that the interface layer of the Ru-ZrHfO sample contains a small portion of SiO_2-like structure while the ZrHfO sample does not. The former should be less responsive to capacitance delay during the V_g sweep.[123] Since no hump is detected in the ZrHfO sample's C-V curve despite its $HfSiO_x$ interface structure, the hump in the Ru-ZrHfO sample's C-V curve is probably due to charges trapped at the Ru/RuO_2 site rather than the poor high-k/Si interface quality. Separately, the V_{FB} of the forward C-V curve of the Ru-ZrHfO sample is more positive than that of the ZrHfO sample, i.e., 0 V vs. -0.46 V. This means that the inclusion of Ru makes the film less prone to positive charge trapping. In addition, the charge trapping density Q_{ot} of the ZrHfO sample, i.e., 2.7×10^{12} cm^{-2}, is higher than that of the Ru-ZrHfO sample, i.e., 1.1×10^{12} cm^{-2}, which were calculated from the V_{FB} differences of the hysteresis curves. The high charge trapping densities of these two samples reflect the high initial defect densities. They are probably generated due to the high PDA temperature, i.e., 1000 ^{o}C. It was reported that the sputter deposited HfO_2 high-k film could be decomposed to form excessive oxygen vacancies and therefore, the high defect density.[117] For the Ru-ZrHfO sample, the alleviated positive charge trapping density and the reduction of Q_{ot} can be explained by the reduction of the oxygen deficiencies or vacancies in the film.[124]

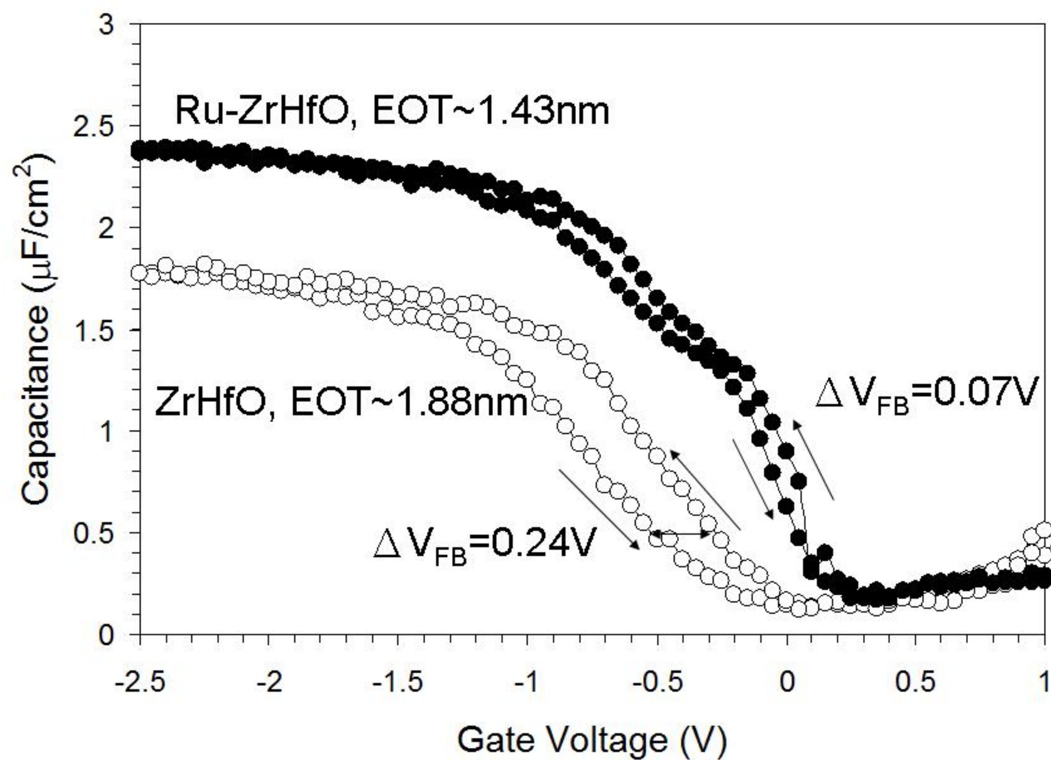

Figure 29. C-V hysteresis curves of ZrHfO and Ru-ZrHfO samples measured at 100 kHz. V_g swept from -3 V to 3 V (forward) and then back to -3 V (backward). Capacitor size: 25 μm in diameter.

Figure 30 shows the conductance-voltage (G-V) curves of the ZrHfO and Ru-ZrHfO samples. For the Ru-ZrHfO sample, in addition to the peak conductance (G_{max}), which occurs at the V_{FB}, an additional small hump located at the hump position of its C-V curve is observed. This is because the charge trapping process occurs in the nanoparticles embedded MOS capacitor may increase its conductance.[125] Compared with the ZrHfO sample, Ru-ZrHfO sample has a higher G_{max} and a lower leakage current, which will be discussed later. The G-V result also supports the previous carrier tunneling effect statement because carriers trapping to the Ru/RuO_2 site can increase G_{max} value.[125]

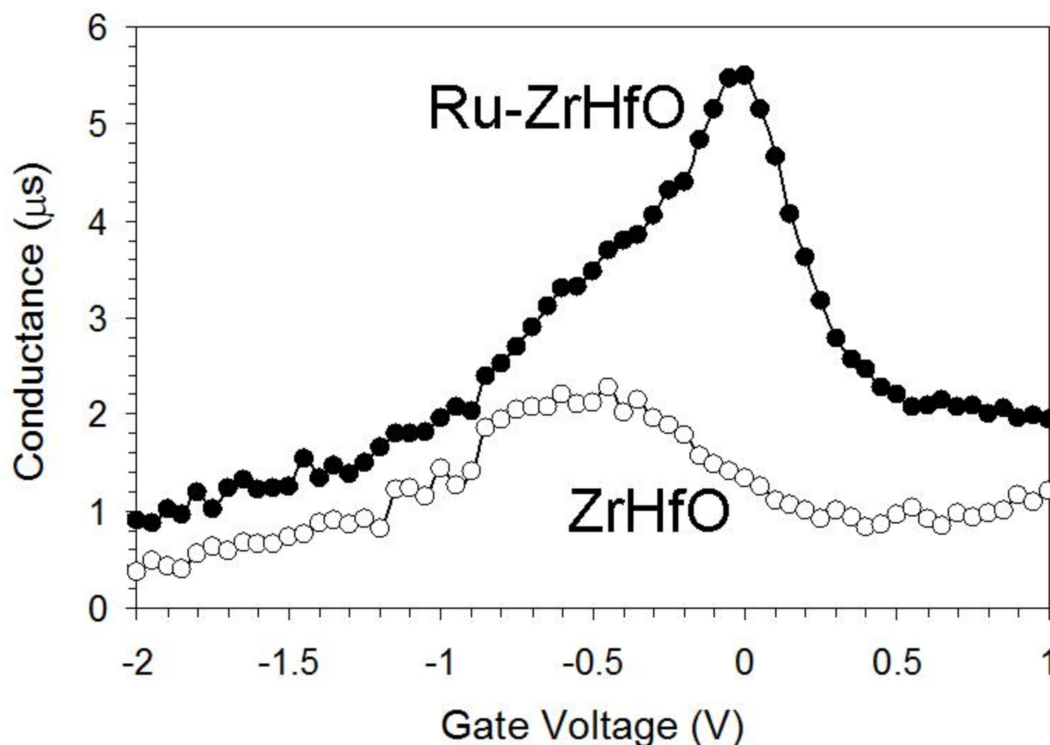

Figure 30. G-V curves of ZrHfO and Ru-ZrHfO samples measured at 100 kHz.

3.4.2 Change of Frequency-Dependent C-V Curve with Inclusion of Ru Nanoparticles

There are various types of polarization which contribute to the permittivity of a dielectric film, including electronic, ionic, orientational, dipolar, defect, and space-charge polarization. Some of them can follow the GHz frequencies while some can not. In order to further verify the dipole enhancement effect via carrier tunneling, the C-V curves were measured with various frequencies, i.e., 100 kHz, 500 kHz, and 1 MHz, as shown in Fig. 31. The ZrHfO sample has a small frequency-dependent capacitance dispersion in the accumulated regime, which is caused by intrinsic defects in the film, e.g., oxygen vacancies. In addition, the C-V curve shape is not influenced by the measure frequency. In contrast, the Ru-ZrHfO sample has a large frequency-dependent dispersion of the capacitance. A hump in the C-V curve is observed, which becomes more obvious with the decrease of the measure frequency. These results are consistent with the previous discussion that the interface layer, which contains either $HfSiO_x$ or SiO_2-like structure, is not responsible for the delay of the capacitance response with respect to the frequency, i.e., hump in the C-V curve. It is probably due to charges trapping via carrier tunneling effect, which is enhanced by decreasing the measure frequency.[123] In addition, the inclusion of Ru into the ZrHfO film enhances the frequency dispersion effect. Furthermore, since more charges can be accumulated at the Ru/RuO_2 site at the low measure frequency than at the high measure frequency, the increase of capacitance is enhanced by the dipole polarization phenomena. The frequency dispersion phenomenon of the Ru-modified film indicates that the increase of the bulk film’s permittivity from the inclusion of Ru is limited by the high frequency operation.

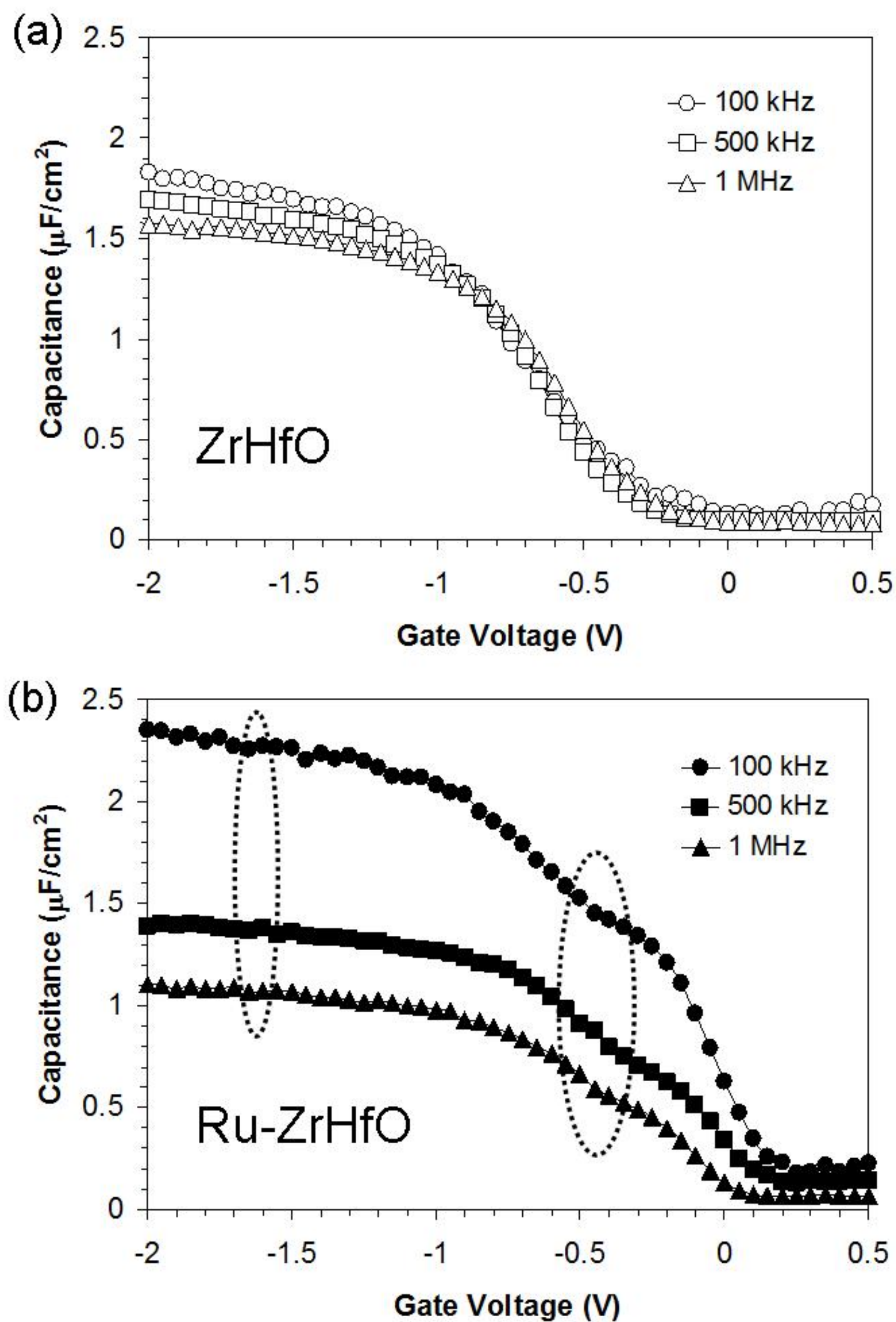

Figure 31. C-V curves of (a) ZrHfO and (b) Ru-ZrHfO samples measured at 100 kHz, 500 kHz, and 1 MHz. V_g swept from -3 V to 3 V.

3.4.3 Change of J-V and J-E Curve with Inclusion of Ru Nanoparticles

Figure 32(a) shows the gate leakage current density-voltage (J-V_g) curves of the ZrHfO and Ru-ZrHfO samples. Both samples show the similar shape in the V_g range of ±3 V. The Ru-ZrHfO sample has a consistent lower J than the ZrHfO sample, e.g., 1.1×10^{-4} A/cm^2 vs. 1.4×10^{-4} A/cm^2 at V_g = -1 V, due to its larger physical thickness. The inset in Fig. 32(a) shows J (at V_g = -1 V) as a function of the EOT of these two samples and that of a poly-silicon/thermal SiO_2 gate stack.[126] The leakage currents of both high-k samples are five orders of magnitude lower than that of the poly-silicon/thermal SiO_2 stack based on the same EOT. The low leakage current characteristic of the Ru-ZrHfO sample is attributed to its thickness. Figure 32(b) shows the J-gate electric field (E) curves of the two high-k capacitors. The curves were measured with negative V_g, i.e., electrons injection from the electrode or holes injection from the substrate. Both samples have similar leakage current when the electric field is low, i.e., | E | < 2.5 MV/cm. However, when the filed is larger than 2.5 MV/cm, the Ru-ZrHfO sample shows a higher leakage current than the ZrHfO sample. The inclusion of Ru in the film makes it more leaky at a high electric field. In addition, the Ru-ZrHfO sample has a lower breakdown strength than the ZrHfO sample, i.e., 6 MV/cm vs. 10.6 MV/cm. However, the dielectric strength of the Ru-ZrHfO sample is comparative to other high-k films with similar EOT's.[127-128]

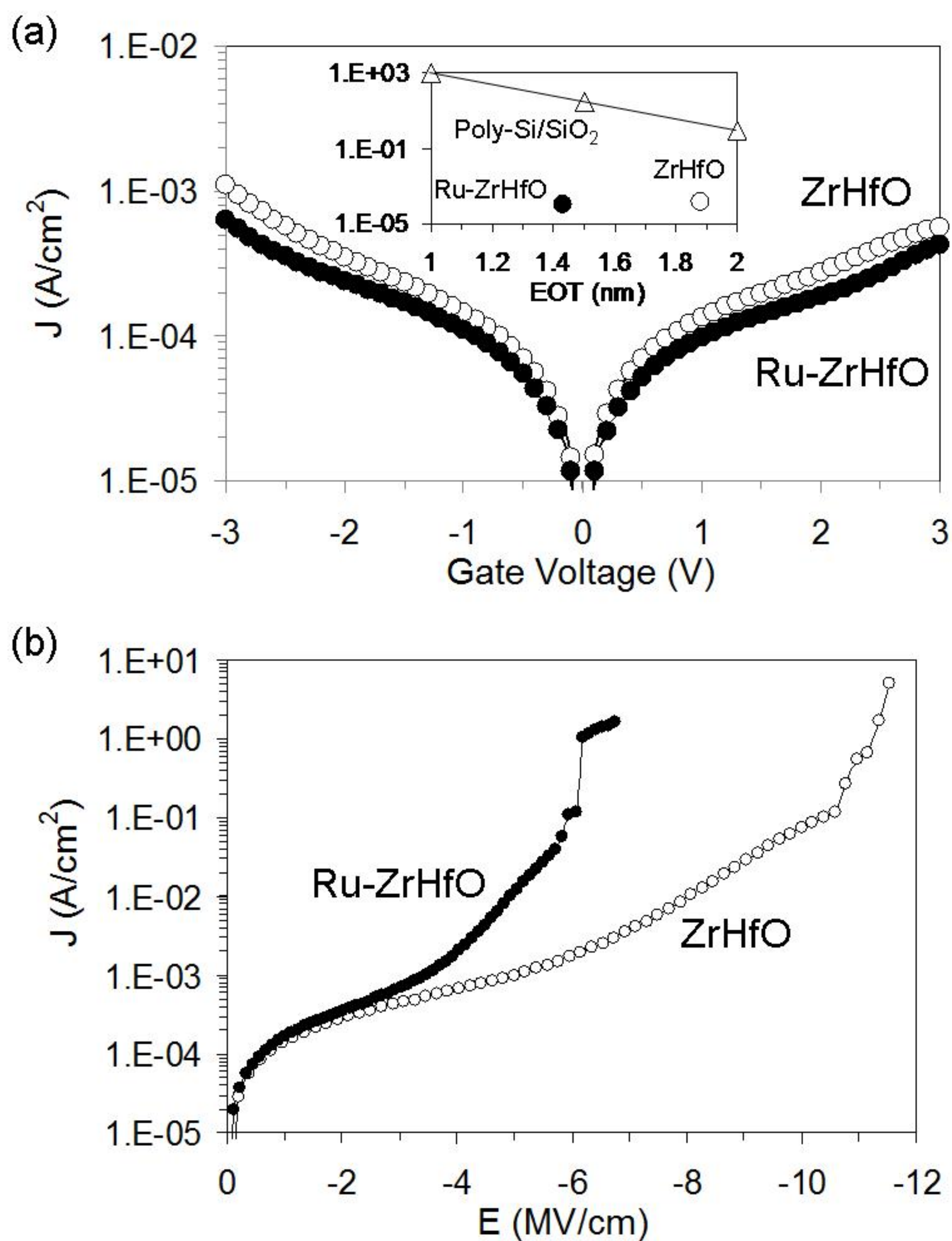

Figure 32. (a) J-V_g and (b) J-E (measured in negative V_g's) curves of ZrHfO and Ru-ZrHfO samples. Inset in (a): J's (at -1 V) of ZrHfO, Ru-ZrHfO, and poly-Si/SiO_2.[126]

3.4.4 Change of Current Transport Mechanism with Inclusion of Ru Nanoparticles

In order to study the carrier transport characteristics of the ZrHfO and Ru-ZrHfO samples, the temperature-dependent leakage current-voltage (J-V) curves were measured and compared, as show in Fig. 33(a) and (b). The curves were measured from $V_g = 0$ V to -3 V in the temperature range of 25 ^oC to 125 ^oC. Since the measurement V_g is low and the conduction band offset between TiN and ZrHfO (~ 1.8 eV to 2.2 eV)[109,129] is much smaller than the valance band offset between ZrHfO and Si (~ 3.4 eV)[130], the current conduction in this range is probably dominated by the electron injection from the gate rather than the hole injection from the substrate.[131] Since both samples show the temperature-dependent current leakage, charges are probably transported by the Schottky emission (SE) or Frenkel-Poole (F-P) tunneling mechanism.[132]

Figure 34 shows the schematic illustrations of the SE and F-P tunneling current transport mechanisms. For the former, carriers need to climb across the energy barrier at the Si/high-k. For the latter, the current transport can be assisted by the traps in the high-k film, i.e., carriers can first tunnel into the traps, and then jump across the energy depth of the trap involved in the F-P current transport.

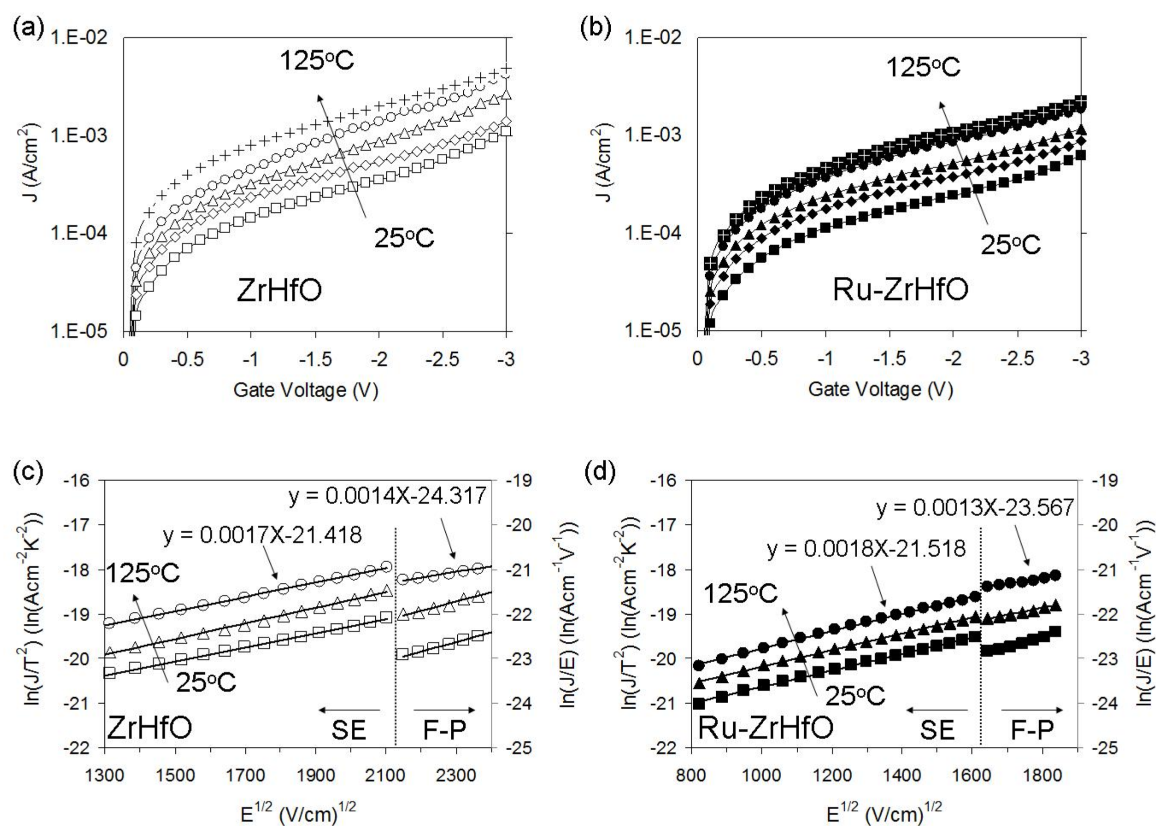

Figure 33. J-V curves of (a) ZrHfO and (b) Ru-ZrHfO samples measured from 25 °C to 125 °C. SE and F-P plots of J-V curves measured at 25 °C, 75 °C, and 125 °C, of (c) ZrHfO and (d) Ru-ZrHfO samples. Symbols represent: □ (ZrHfO) ■ (Ru-ZrHfO) 25 °C, ◇ ◆ 50 °C, △ ▲ 75 °C, ○ ● 100 °C, + ⊞ 125 °C.

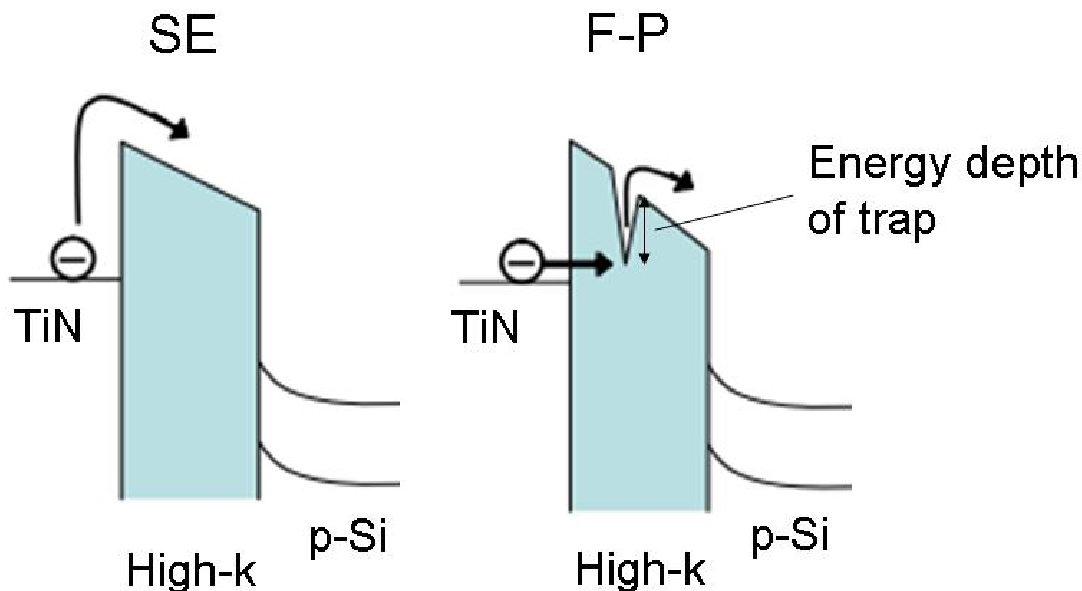

Figure 34. Schematic illustrations of SE and F-P current transport mechanisms.

Figure 33(a) and (b) were redrawn into the SE and F-P plots, as shown in Fig. 33(c) and (d). For both samples, the SE relation fits well at the low electric field regime while the F-P relation is suitable in the high electric field regime. These relationships are independent of the measurement temperature. This is consistent with the literature report that the SE mechanism occurs at the low electric field while the F-P tunneling process requires a high electric field.[133-134] It is also noted that when the current transport is dominated by SE, both samples show no obvious difference in the equation of linearly fitted trend, i.e., at 125 ^{o}C, the slopes are 0.0017 and 0.0018, and the y-axis interception (at $E^{1/2} = 0$) are -21.418 and -21.518, for the ZrHfO and Ru-ZrHfO samples, respectively. Since there is only a very small amount of Ru/RuO_2 nanoparticles discretely dispersed in the amorphous ZrHfO film, the chance of diffusion of Ru/RuO_2 to the top interface is

probably low. Previously, it was reported that the effective barrier height between the metal gate and the underneath high-k dielectric could be changed due to the formation of a dipole layer, which is resulted from the charge transfer from V_o to the gate electrode.[135] Therefore, judged from the similarity in the SE fitting equations of the Ru-ZrHfO and ZrHfO samples, the TiN/ZrHfO interface properties were not influenced by the inclusion of Ru in the bulk film. On the other hand, when the current transport is dominated by F-P mechanism, the linear equation for the Ru-ZrHfO sample (measured at 125 ^{o}C) has a smaller y-axis interception than that for the ZrHfO sample has, i.e., -23.567 vs. -24.317. Therefore, the energy depths of traps contributed to the F-P conduction are estimated to be 0.23 eV and 0.46 eV for the Ru-ZrHfO and ZrHfO samples, respectively.[132] Furthermore, the F-P mechanism of the Ru-ZrHfO sample occurs at a much lower electric filed than that of the ZrHfO sample, i.e., $E^{1/2}$ ~ 1642 $(V/cm)^{1/2}$ vs. ~ 2148 $(V/cm)^{1/2}$. This means that carriers can tunnel across the metal/high-k film interface at a relatively small electric field if the high-k film contains conductive Ru nanoparticles. This phenomenon also explains why both high-k samples have similar J when $| E | < 2.5$ MV/cm, but when $| E | > 2.5$ MV/cm, the Ru-ZrHfO sample has a higher J and a larger slope in the J-E curve than the ZrHfO sample has. This is because the dominant current transport mechanism of the Ru-ZrHfO sample changes from SE to F-P at | E | ~ 2.5 MV/cm ($E^{1/2}$ ~ 1581 $(V/cm)^{1/2}$), and the energy depth of the traps responsible for the F-P conduction mechanism is lower than that of the ZrHfO sample as previously discussed.

3.4.5 Reliability of Ru-Modified ZrHfO High-K MOS Capacitor

The reliability characteristics of the Ru-ZrHfO sample has also been studied using the constant voltage stress (CVS) method, as shown in Fig. 35. The J vs. stress time curve was measured at room temperature under V_g = -4.25 V. Under this CVS condition, both Ru-ZrHfO and ZrHfO samples have similar J's, i.e., 0.009 A/cm^2 vs. 0.01 A/cm^2. The time to failure (TTF) of the film has been extended from 250 seconds to 306 seconds when Ru is included in the ZrHfO sample. The longer TTF of the Ru-ZrHfO sample could be attributed to its large physical thickness. For the Ru-ZrHfO sample, the soft breakdown, i.e., the small jump of J occurs at 60 seconds, from 10^{-2} A/cm^2 to 0.78 A/cm^2, is due to the beginning of formation of some current leakage paths.[136] Therefore, the small Ru/RuO_2 nanoparticles can cause the quick formation of the leakage path in the film. However, since the Ru-ZrHfO sample is thicker than the ZrHfO sample and the nanoparticles are dispersed discretely in the amorphous matrix, it takes a long time for the film to breakdown. The lifetime of the dielectric film can be projected by extrapolating the curve of TTF as a function of the applied gate stress voltage.[2] Figure 36 shows the TTF vs. the inverse of gate stress voltage of the Ru-ZrHfO sample in the V_g range of -4 V to -4.75 V, which is much higher than the typical MOS gate voltage. From the curve extrapolation, the lifetime of the Ru-ZrHfO sample can be 10 years at the gate bias voltage of -2 V.

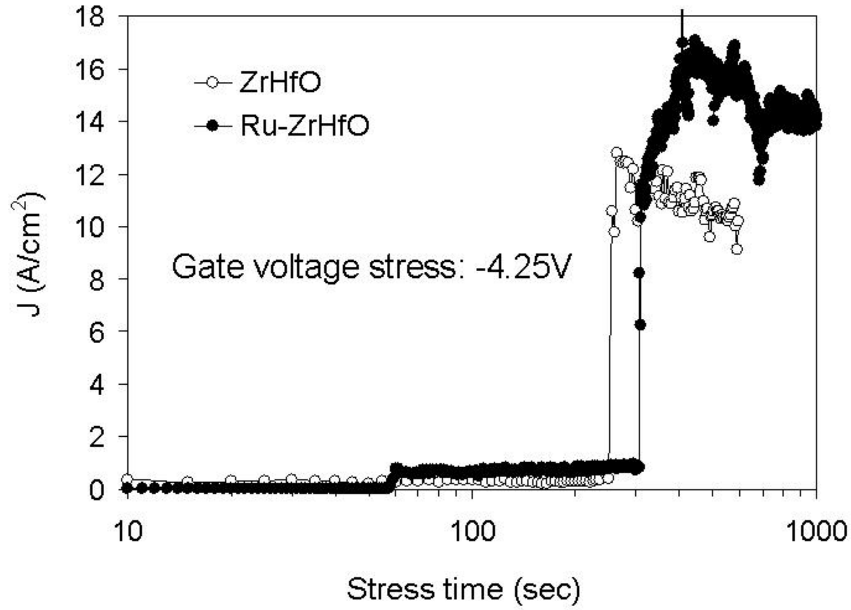

Figure 35. Constant voltage stress (at V_g = -4.25 V) curves of ZrHfO and Ru-ZrHfO samples.

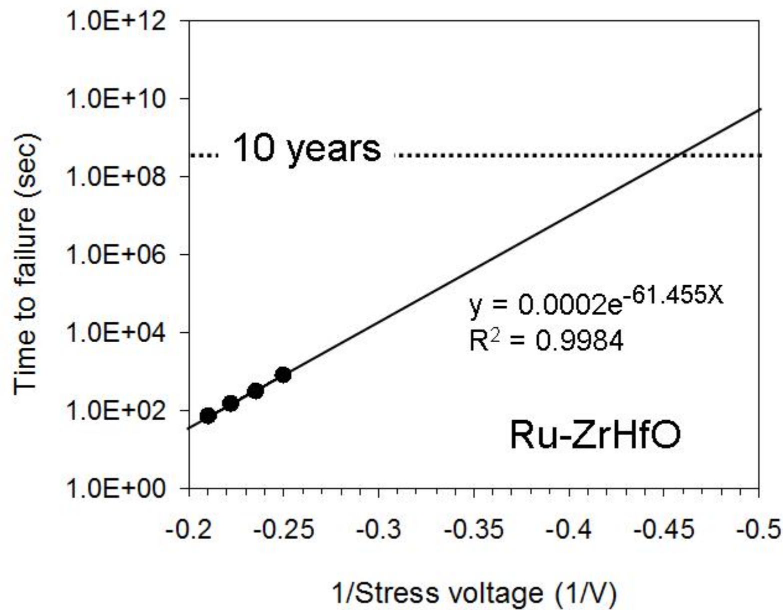

Figure 36. Time to failure vs. inverse of stress voltage curve of Ru-ZrHfO sample.

3.5 Summary

The addition of Ru into the ZrHfO high-k film changed its materials and electrical properties. Discrete nanoparticles composed of Ru and RuO_2 were detected by TEM and XPS. The high-k/Si interface layer contains the SiO_2-like structure due to the inclusion of Ru in the bulk film. The Ru-ZrHfO sample shows a more positive V_{FB} and a smaller V_{FB} difference of the hysteresis curve than that of the ZrHfO sample probably due to the decrease of the oxygen vacancy density. The high permittivity of Ru-ZrHfO film could be explained by the dipole enhancement mechanism induced from carrier capture. This is supported by the frequency-dependent C-V and G-V curves. The Ru-ZrHfO sample has a leakage current density five orders of magnitude lower than that of the poly-silicon/thermal SiO_2 structure, and has a comparative breakdown strength to other high-k films of the same EOT. The temperature-dependent J-V measurement indicates that Schottky emission and Frenkel-Poole tunneling are dominant current conduction mechanisms in the Ru-ZrHfO sample at the low and high electric field regimes, respectively. The inclusion of Ru in the ZrHfO film lowers the energy depth of traps involved in F-P conduction but does not affect the TiN/high-k barrier height. The Ru-ZrHfO film has a large breakdown voltage and a long lifetime due to its unique film structure. There is one disadvantage in the Ru-modified high-k film, i.e., the poor response to the high frequency, which may limit its application to the very high frequency device. More detailed studies are required on this subject.

CHAPTER IV

NANOCRYSTALLINE RUTHENIUM OXIDE EMBEDDED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K NONVOLATILE MEMORIES*

4.1 Introduction and Motivation

Recently, the nanocrystal structure has been proposed to replace the poly-Si layer in the future-generation floating gate (FG) nonvolatile memory device to improve the charge retention characteristics.[53-54] As mentioned in Chapter I, HfO_2 film with a low EOT can be used as the tunnel and/or control oxide in the FG memory device to achieve the high charge retention efficiency.[73] In addition, HfO_2 has lower electron and hole energy barriers with respect to Si substrate than SiO_2, i.e., 1.5 eV and 3.4 eV vs. 3.5 eV and 4.3 eV, respectively, which favors the low programming power. The nanocrystals embedded HfO_2 memory device has been reported.[137-138] Since the ZrHfO film has been demonstrated that has a lower EOT, a thinner interface thickness, and a lower interface state density compared to the un-doped HfO_2 film,[108,139] it has great potential to serve as the tunnel and control oxides in the FG memory. In addition, it has been reported that conductive materials, e.g. metals or metal oxides, could be prepared into nanocrystals embedded in a high-k or SiO_2 film.[140-141]

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Ruthenium oxide (RuO) is a conductive oxide that has excellent thermal and chemical stability.[142] It was also reported that nanocrystals with a large work function and a high density of states around the Fermi level can be embedded into dielectrics to form the deep charge trapping well.[60] Since RuO has a large work function, e.g., ~5 eV,[143] it can be prepared into nanocrystalline (nc) dots and embedded into a dielectric film to achieve good memory characteristics. Maikap *et al*.[144] reported a nc-RuO embedded memory capacitor composed of a $Si/SiO_2/HfO_2$/nc-RuO/Al_2O_3 structure that shows good memory functions. However, there is lack of detailed information in the charge trapping mechanism and reliability of the nc-RuO embedded high-k memory device. In this study, the memory functions and related material properties of the MOS capacitors with the nc-RuO embedded ZrHfO gate dielectric structure were prepared and investigated thoroughly. This kind of information is critical for the practical application of the memory device.

4.2 Experimental

MOS capacitors composed of the nc-RuO embedded ZrHfO gate dielectric were fabricated on the dilute HF cleaned p-type Si (100) wafer (resistivity 11-20 Ω·cm). The gate dielectric composed of the bottom ZrHfO (tunnel oxide)/Ru/top ZrHfO (control oxide) structure was sequentially deposited by RF magnetron sputtering at 5 mTorr in a one-pump-down process without breaking the vacuum. The tunnel and control ZrHfO films were deposited using a Zr/Hf (wt % 12:88) composite target at 100 W in an Ar/O_2 (1:1) ambient for 2 min and 4 min, respectively. Ru films with three different thicknesses were separately deposited from a Ru target at 80 W in the Ar ambient for 1 min, 2 min,

and 3 min. The post deposition annealing (PDA) step was done at 950 °C for 1 min in a N_2/O_2 (1:1) ambient using a RTA method. Then, a 120 nm thick Al film was sputter-deposited on top of the nc-RuO embedded high-k stack. It was subsequently defined with a lithography step and etched into the round-shaped gate electrodes with an area of 7.85×10^{-5} cm^2. An Al film was also deposited on the backside of the wafer for the ohmic contact formation. The complete capacitor was annealed at 300 °C for 5 min under the H_2/N_2 (1:9) atmosphere. The control sample, i.e., without the embedded nc-RuO in ZrHfO, was prepared under the same condition. The capacitor's C-V and J-V curves were measured using the Agilent 4284A LCR meter and Agilent 4155C semiconductor parameter analyzer, respectively. The flatband voltage (V_{FB}) was extracted from the C-V curve using the NCSU CVC program.[103] The chemical bond structure and composition of the bulk and interface layers of the gate dielectric stack were characterized with XPS using the monochromatic Al Kα x-ray emission at 1486.6 eV. Figure 37 shows the J-V curves of the three capacitors that separately contain 1 min-, 2 min-, and 3 min-deposited Ru films. The V_g was swept from -3 V to +3 V then back to -3 V. Only the capacitor containing 1 min-deposited Ru film showed a typical J-V curve of the nanocrystals embedded gate dielectric stack, i.e., including a negative differential resistance (NDR) peak.[145] On the contrary, both the capacitors that contain 2 min- and 3 min-deposited Ru films showed intensive leakage currents, which probably can be attributed to the inclusion of a large amount of conductive Ru in the device. Therefore, in this study, only the capacitor that contains 1 min-deposited Ru film was investigated.

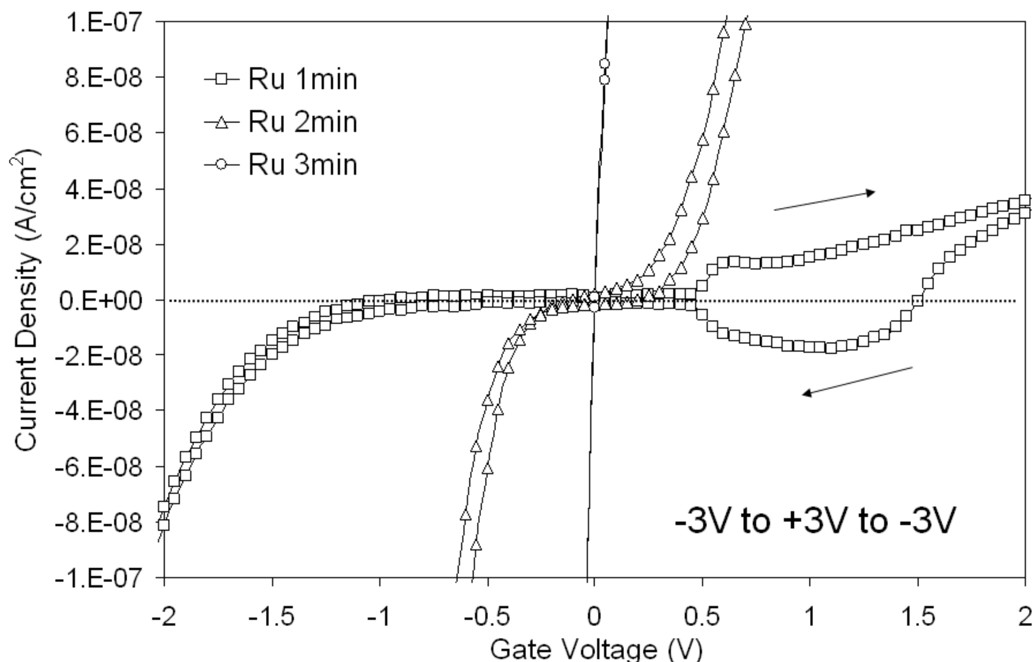

Figure 37. J-V curves (swept from -3 V to + 3 V then back to -3 V) of the capacitors that separately contain 1 min-, 2 min-, and 3 min-deposited Ru films.

4.3 Material Properties of nc-RuO Embedded ZrHfO High-K Gate Dielectric Stack

4.3.1 Formation of Discrete nc-RuO Structure after PDA

Figure 38 shows the top-view TEM micrographs of the Ru thin film (1 min-deposited) (a) before and (b) after PDA with corresponding SAD patterns shown in the insets. The as-deposited Ru is a continuous polycrystalline film. After PDA, it becomes discrete nanocrystalline dots with a 2-D spatial density of about 8×10^{11} cm^{-2}. The original Ru and final nc-RuO structures are confirmed from the SAD patterns. Figure 38(c) shows the HRTEM top view of the single nc-RuO dot, which has a lattice fringe spacing of 0.318 nm belong to the RuO (110) structure.[146]

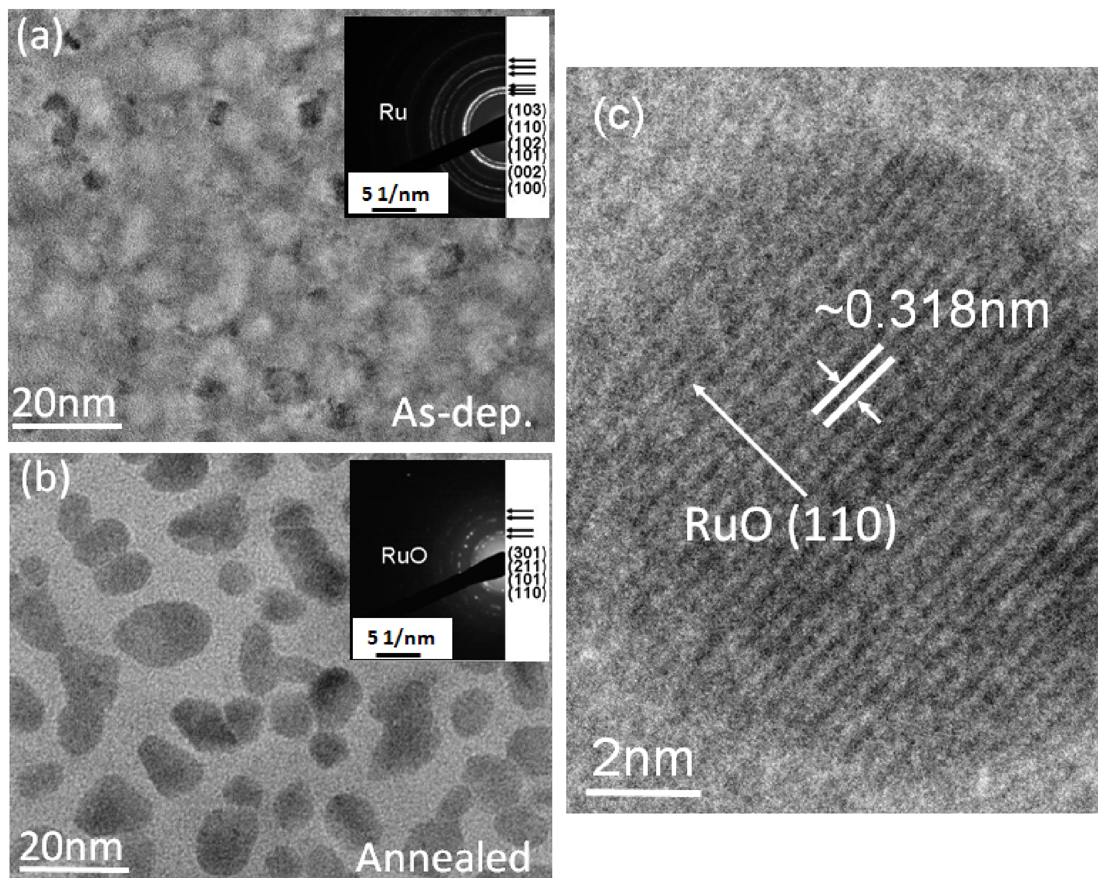

Figure 38. Top-view TEM micrographs of (a) as-deposited and (b) annealed Ru films. Insets in (a) and (b) are the corresponding SAD patterns. (c) HRTEM top view of the single nc-RuO dot.

Figure 39 shows Ru 3*d* XPS spectra of (a) as-deposited and (b) annealed Ru films. The former shows two metallic Ru 3*d* peaks at 279.7 eV and 283.9 eV, while the latter contains Ru 3*d* peaks at 282.6 eV and 286.8 eV, which are contributed by RuO.[147-148] Figure 39(b) also contains two C 1*s* peaks at 283.1 eV and 284.5 eV, which are from the environmental contaminations. Therefore, the XPS analysis is consistent with the SAD result that the as-deposited Ru film can transform to RuO structure after PDA.

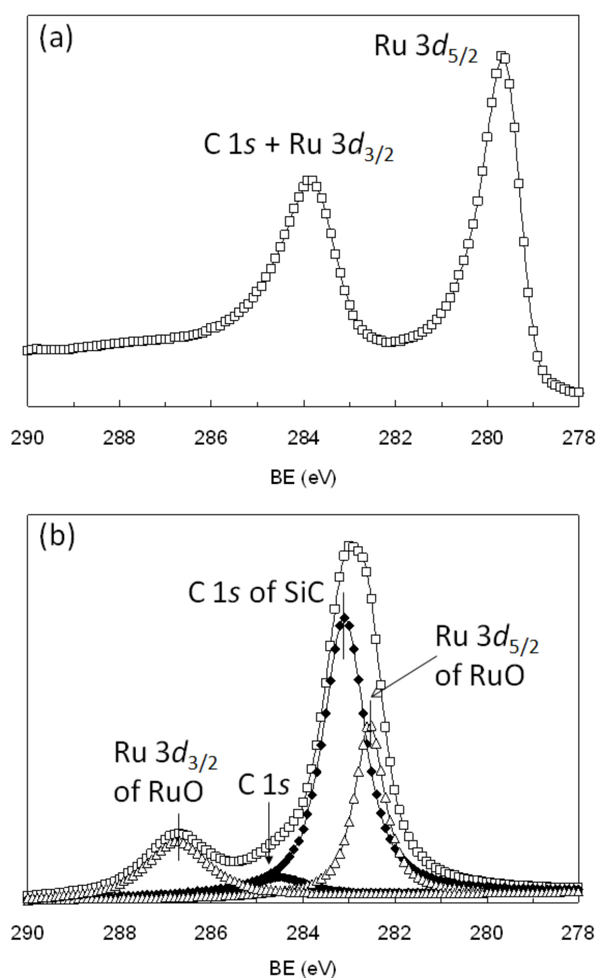

Figure 39. Ru 3*d* XPS spectra of (a) as-deposited and (b) annealed Ru films.

4.3.2 Physical and Chemical Properties of Bulk nc-RuO Embedded ZrHfO High-K Film and Interface Layer

The high resolution cross-sectional TEM micrographs of (a) the control and (b) the nc-RuO embedded ZrHfO samples after PDA are shown in Fig. 40. No visible lattice fringes were observed in the control sample, which indicates the amorphous structure of the ZrHfO film. The nc-RuO embedded sample contains 5-7 nm size nanodots highlighted in circles and surrounded by the amorphous ZrHfO film. Each nanodot shows lattice fringes with the 0.317 nm spacing, which corresponds to the RuO (110) structure.[146] The bulk ZrHfO film in the control sample is about 5 nm thick. The total thickness of the nc-RuO embedded ZrHfO film is about 7.1 nm, which is consisted of 1.2 nm ZrHfO tunnel oxide layer, 4.5 nm of nc-RuO layer, and 1.4 nm ZrHfO control oxide layer. In addition, a 1.4 nm thick interface layer was formed between the Al gate and top ZrHfO layer. Figure 40(c) shows the Al 2*p* XPS spectrum of this interface layer, which has a binding energy (BE) of 74.6 eV corresponding to that of Al_2O_3.[149] This interface layer, which has a large electron barrier height of 2.8 eV to the Al gate electrode,[150] should be counted as part of the control oxide layer in the nc-RuO embedded sample. Another interface layer (IL) is formed between the Si wafer and tunnel ZrHfO layer. Figure 40(d) shows the EDS spectrum of this IL, which is consisted of Hf, Si, and O. It probably is a Hf-silicate ($HfSiO_x$) layer as reported in Ref. 108. The XPS analysis of this layer, which will be shown and discussed later in this chapter, also confirms this structure. This IL has lower electron and hole energy barriers (with respect to Si) than those of SiO_2,[130] which favors the high programming efficiency of the memory function.

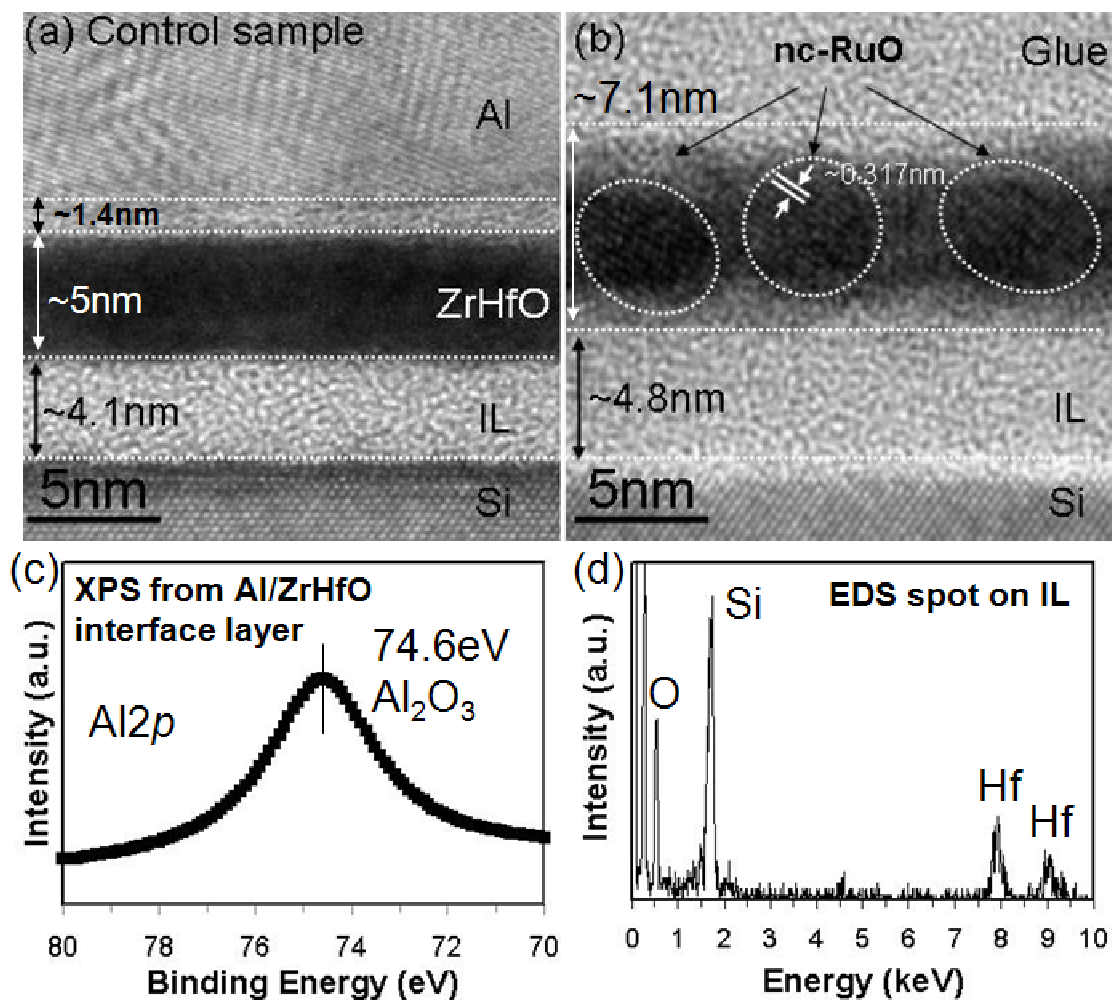

Figure 40. Cross-sectional TEM micrographs of (a) the control sample and (b) the nc-RuO embedded ZrHfO stack. (c) Al 2*p* XPS spectrum of the Al/ZrHfO interface layer. (d) EDS spectrum from the Si/ZrHfO interface layer.

The IL thickness of the nc-RuO embedded sample is larger than that of the control sample, i.e., 4.8 nm vs. 4.1 nm. It was reported that the growth of the Si/high-k interface layer is strongly related to the oxygen supply during the PDA process.[151] In addition, Brossmann *et al*.[152] reported that the oxygen diffusion in the high-k film containing grain boundaries is enhanced in comparison to the amorphous film. The embedding of the nc-RuO into the amorphous ZrHfO film may create extra defects, e.g., at the nc-RuO/ZrHfO interface, which may be responsible for the thickening of the IL. A detailed discussion on the nc-RuO/ZrHfO interface will be included later in this chapter.

Figure 41 shows the XRD pattern of the nc-RuO embedded ZrHfO sample, which contains a $2\theta=28.2^{o}$ peak corresponding to RuO (110).[153] The average nc-RuO size is estimated to be 6.8 nm calculated from the Scherrer equation.[97] The inset is the XRD pattern of the control sample, which does not contain any crystalline structure. This confirms the TEM result that the ZrHfO film remains amorphous after PDA.

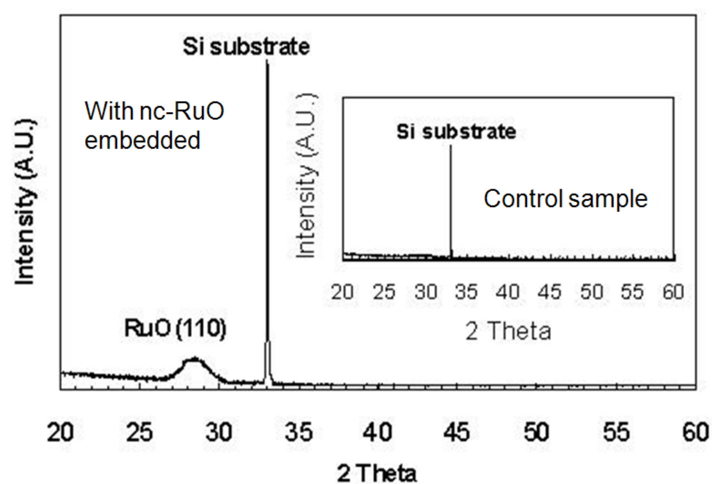

Figure 41. XRD patterns of the nc-RuO embedded sample and the control sample (inset).

Figure 42 shows the XPS Hf 4*f* spectra of both the control and nc-RuO embedded samples. The control sample contains a Hf $4f_{7/2}$ peak at BE 17.2 eV. The nc-RuO embedded sample has an additional Hf $4f_{7/2}$ peak at 17.9 eV. The BE 17.2 eV peak is contributed by the Hf-O (BE 16.8 eV) and Hf-Si-O (BE 17.6 eV) bonding states.[154] The former is from the bulk ZrHfO film while the latter is from the $HfSiO_x$ formed at the Si interface. The inset of Fig. 42 shows that the intensity of the Si 2*p* peak in the nc-RuO embedded sample is much lower than that in the control sample due to the former's thicker layer structure. Therefore, the extra BE 17.9 eV peak in the nc-RuO embedded sample is most probably from the bulk high-k stack instead of from its interface with the Si substrate. Both the bulk nc-RuO and nc-RuO/ZrHfO interface can contribute to this peak. The interface formation phenomenon between the nanodot and surrounding oxide after PDA process has been reported.[155] Since the area ratio of the BE 17.9 eV peak to the BE 17.5 eV peak in the nc-RuO embedded sample is about 29 %, the contribution of this interface to the charge trapping is not negligible.

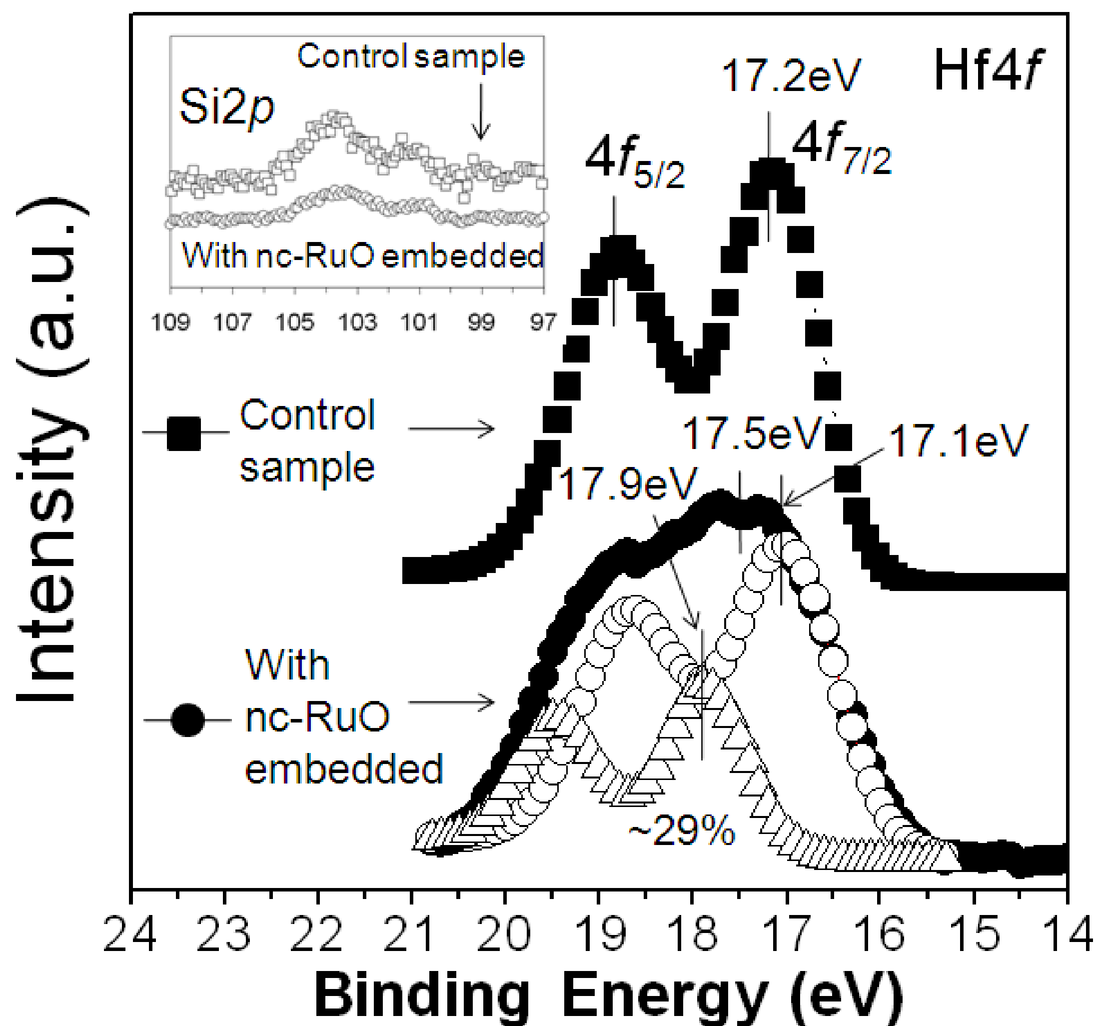

Figure 42. XPS Si 2*p* (inset) and Hf 4*f* spectra of the control sample and the nc-RuO embedded ZrHfO capacitor. The Hf 4*f* peaks of the latter were deconvoluted.

4.4 Electrical Properties of nc-RuO Embedded ZrHfO High-K MOS Capacitor

4.4.1 Memory Functions Contributed by Hole and Electron Trapping

Figure 43 shows the high frequency (1 MHz) C-V hysteresis curves of the control sample and nc-RuO embedded capacitor. V_g was swept from the negative value to the positive value, i.e. the forward direction, and then back to the negative value, i.e. the backward direction, in the range of ±9 V. Since the memory window (i.e., defined as the V_{FB} difference between the V_{FB} of the forward curve and that of the backward curve) of the control sample is very small, the embedded nc-RuO is responsible for the large memory window of 1.72 V. The inset of Fig. 43 shows the V_{FB}'s of the nc-RuO embedded sample in the forward and backward directions as functions of the V_g sweep ranges from ±3 V to ±9 V. The corresponding memory window is increased from 0.08 V in the sweep range of ±3 V to 0.51 V in the range of ±6 V to 1.72 V in the range of ±9 V. Since the increase of the memory window is mostly contributed by the negative V_{FB} shift in the forward sweep direction, especially at the large V_g sweep range, the hole-trapping phenomenon is not negligible. The V_{FB} of the backward curve swept from +6 V is more negative than that of the backward curve swept from +3 V, which indicates that holes trapped during the forward sweep were not completely removed at the positive V_g condition. The hole-removal efficiency increases when the magnitude of the V_g of the backward sweep is increased, i.e., to + 9 V.

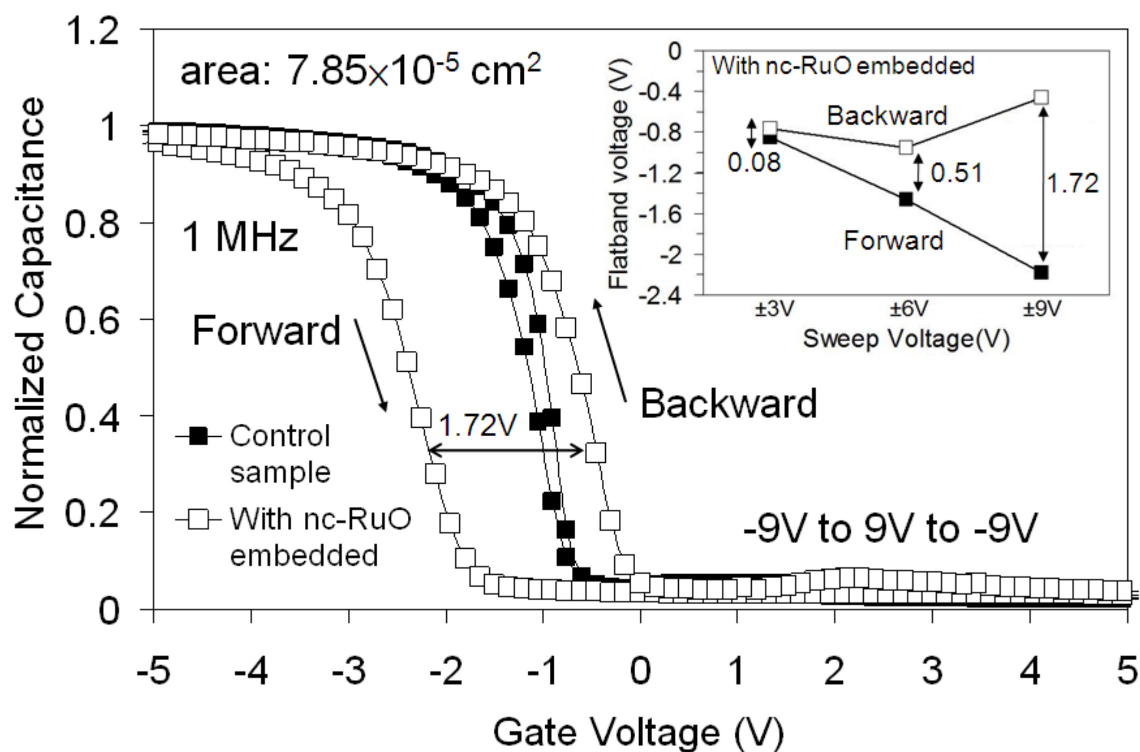

Figure 43. C-V hysteresis curves of the nc-RuO embedded ZrHfO MOS capacitor and the control sample. V_g was swept from negative to positive (forward) and then back to negative (backward). V_{FB}'s of forward and backward curves and corresponding memory windows are shown in the inset.

Figure 44(a) further shows C-V hysteresis curves of the nc-RuO embedded ZrHfO high-k MOS capacitor swept from different negative voltages, e.g., -3 V, -6 V, and -9 V, respectively, to the same +9 V (forward sweep), and then backward to the original voltages (backward sweep). Figure 44(b) and (c) show hysteresis curves that were swept with the same method as those in Fig. 44(a) except the smaller end voltages in the forward sweep direction, i.e., +6 V and +3 V, respectively. Before the C-V hysteresis measurement, the V_{FB} of the fresh nc-RuO embedded device was estimated from the C-V curve swept in a small V_g range, i.e., -2 V to +1 V, which trapped a negligible amount of charges in the dielectric layer. Figure 45 summarizes V_{FB}'s of Fig. 44(a), (b), and (c) curves in forward and backward directions. Several conclusions can be summarized from these figures. First, the forward V_{FB} shifts to more negative V_g direction with the increase of the starting -V_g in the forward curve, i.e., -0.87 V, -1.38 V, and -2.18 V with the starting voltage of -3 V, -6 V and -9 V, respectively. Therefore, the hole-trapping efficiency increases with the increase of the magnitude of the negative V_g. Second, with the same starting V_g = +9 V, all backward V_{FB}'s are more positive than that of the fresh device, i.e., -0.77 V. However, when the backward starting voltages are less than +9 V, their V_{FB}'s are more negative than -0.77 V. This phenomenon indicates that, during the forward sweep, the injected holes are strongly trapped in the capacitor and are not fully erased by the subsequent small backward sweep. Whereas, when the backward starting voltage is large enough, not only the previously trapped holes are released but also electrons are injected from the Si substrate to the high-k stack. Third, for the same starting +9 V in the backward sweep curve, the memory window increases with the increase of the starting -V_g in the forward curve, e.g., 0.56 V, 0.98 V, and 1.72 V for the

starting V_g of -3 V, -6 V, and -9 V in the forward sweep, respectively. Therefore, the hole-trapping process is critical to the capacitor's memory function.

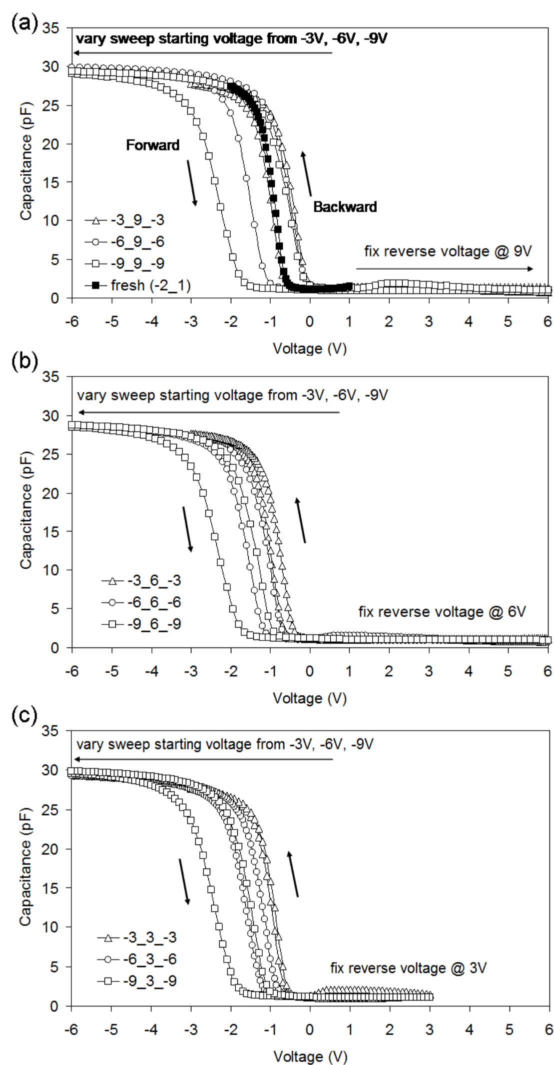

Figure 44. C-V hysteresis curves (at 1MHz) of the nc-RuO embedded ZrHfO MOS capacitor with fixed backward reverse voltages at (a) +9 V, (b) +6 V, and (c) +3 V. Each figure contains 3 curves with the forward starting voltage of -3 V, -6 V and -9 V, respectively.

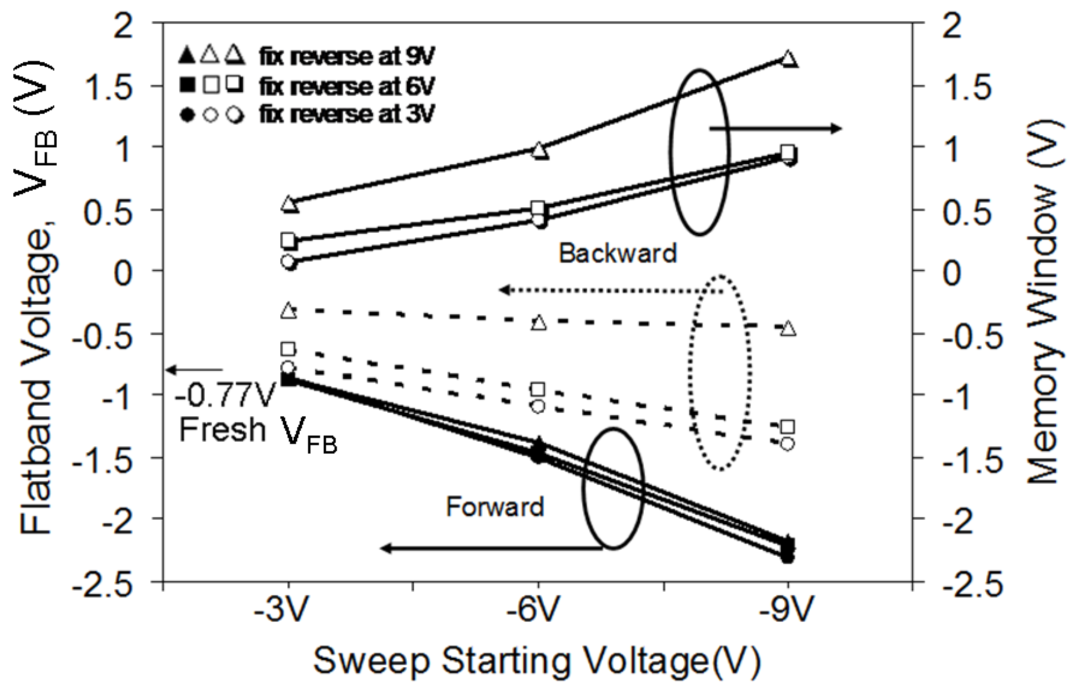

Figure 45. Summarized forward V_{FB}'s, backward V_{FB}'s, and memory windows of C-V curves shown in Fig. 44.

4.4.2 Differentiation of Hole and Electron Trapping

In order to differentiate the electron- and hole-trapping characteristics in the device, the constant voltage stress (CVS) method was carried out by applying a V_g of +9 V or -9 V to the gate electrode for 10 s. Before the V_g stress was applied, the device's fresh C-V curve was measured for comparison. The V_{FB}'s of the capacitor before and after the CVS were estimated from the C-V curves that were measured over a small V_g range, i.e., -2.5 V to 0.5 V at 1 MHz. Again, this small V_g introduces negligible amount of charges to the device. Therefore, the C-V shift from the "fresh" curve after the CVS is due to the trap of charges during stress. Figure 46 shows the CVS curves of the control and nc-RuO embedded samples under various CVS conditions. The control sample has very limited charge trapping capability after either +9 V or -9 V stress. Therefore, neither the bulk ZrHfO nor the interface layer between Si and ZrHfO can trap an appreciate amount of charges. However, the nc-RuO embedded ZrHfO sample shows large V_{FB} shifts (ΔV_{FB}'s), i.e., -1 V (negative shift) and 0.58 V (positive shift) after -9 V and +9 V CVS, respectively. The former corresponds to a hole-trapping density (Q) of 2.2×10^{12} cm^{-2}; the latter corresponds to an electron-trapping density of 1.3×10^{12} cm^{-2}, according to the equation of

$$Q = \frac{C_{acc}\Delta V_{FB}}{q} \tag{14}$$

where C_{acc} is the device's unit capacitance at the accumulation regime (3.82×10^{-7} F/cm^2), and q is the electron charge.

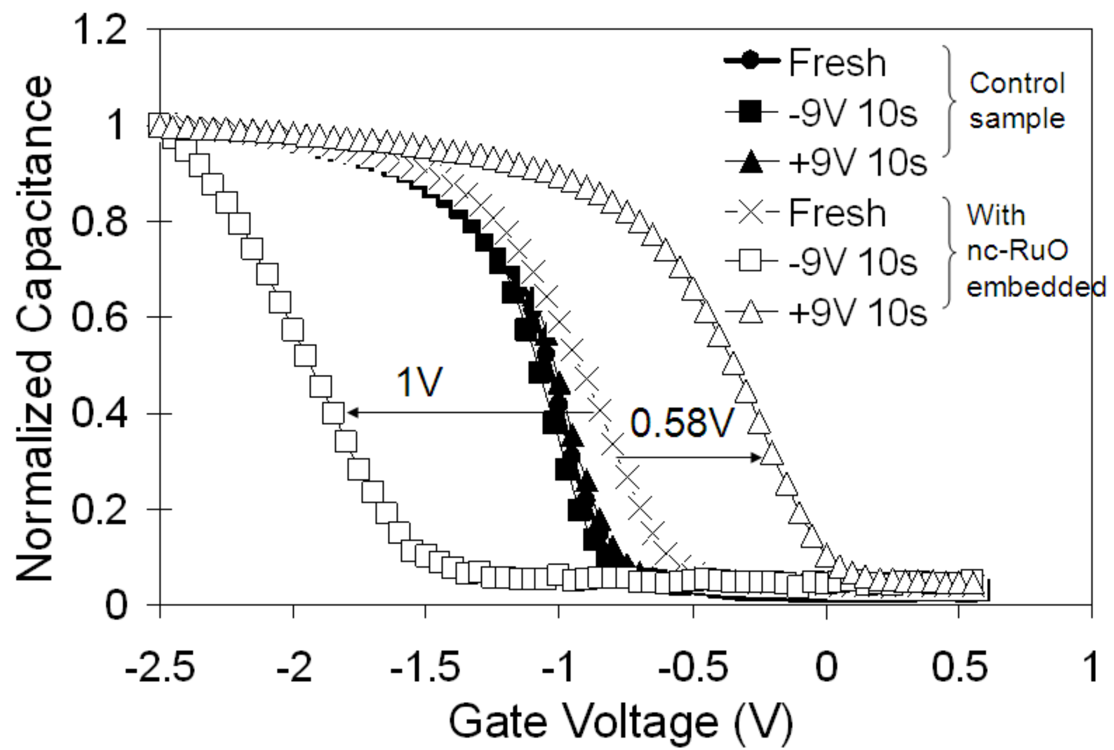

Figure 46. C-V curves of the control sample and the nc-RuO embedded ZrHfO MOS capacitor before (fresh) and after CVS at ±9 V for 10 s. Fresh C-V was measured from V_g = -2.5 V to 0.5 V.

The nc-RuO embedded device traps more holes than electrons under the same magnitude of stress voltage for the same period of time. There are several possible explanations. For example, in the p-type Si, it is easier to form the hole-accumulation layer than the electron-rich inversion layer under the same magnitude of V_g stress condition. The concentration of hole in the accumulation layer (under $-V_g$) is higher than that of electron in the inversion layer (under $+V_g$). Also, holes and electrons may have different charge trapping sites in the high-k stack. In addition, it is observed that the fresh C-V curve of the nc-RuO embedded capacitor is less sharp than that of the control sample. The former is on the positive V_g direction of the latter. The slightly stretched C-V shape of the nc-RuO embedded capacitor may be related to the nc-RuO/ZrHfO interface layer quality. This interface can be physically closer to the Si surface than the bulk nc-RuO layer. Charges may interact with this interface during V_g sweep, which results in the delayed C-V response.[156] The shift of the C-V curve might be related to the thickness of the IL. For example, it was reported that for some p-Si MOS capacitors containing the same HfO_2 high-k film, the V_{FB} shifts more positively when the IL thickness increases.[157-158] When the oxygen supply is sufficient during the post deposition annealing, the IL tends to growth thicker and contains less amount of the inherent positive charges, i.e., the oxygen vacancies, in the gate dielectric stack.[159] This phenomenon is also consistent with the previous discussion, i.e., compared with the non nanocrystal-embedded ZrHfO film, the existence of the nc-RuO in the ZrHfO film favors for oxygen diffusion through the high-k stack.

Figure 47 shows the V_{FB} shift (ΔV_{FB}) of the nc-RuO embedded capacitor with respect to the fresh capacitor, i.e., V_{FB} (after bias)-V_{FB} (fresh), with respect to the stress

time at various stress V_g's. All V_{FB}'s were extracted from the C-V curves measured over a small V_g range of -2 V to +0.5 V, which had negligible effects on the actual V_{FB} values. After V_g = -5 V or -6 V stress, the ΔV_{FB} is negative and its magnitude increases monotonically with the stress time. Therefore, the capacitor's hole-trapping capacity is enhanced with the stress time and the magnitude of the stress V_g. On the contrary, after the V_g = +5 V bias, the ΔV_{FB} is negligibly small even for a long period of stress time. When the stress V_g is increased to +6 V, the ΔV_{FB} is a small positive value for the first 1 s. It increases slowly with the increase of stress time and reaches a saturation value at 40 s. The same phenomenon occurs under the V_g = +8 V stress condition except the ΔV_{FB} is much larger than that of the V_g = +6 V condition. Therefore, for the same magnitude of the V_g stress, the hole-trapping efficiency is higher than the electron-trapping efficiency. Since the capacitor was fabricated on the p-type Si wafer, under the negative V_g stress condition, the hole accumulation layer was easily formed. Holes can be injected into the gate dielectric layer when enough energy is provided. However, in order to form an electron-rich inversion layer for the subsequent injection into the high-k stack, a large positive V_g is required. Under the -5 V or -6 V stress condition, the ΔV_{FB} increases monotonically with stress time indicating that not all injected holes are trapped in the dielectric stack.[160] For example, some of the holes may tunnel through the whole high-k stack to reach the gate electrode. On the other hand, since the saturation phenomenon shown in the electron-trapping process does not occur in the hole-trapping process, the hole-trapping mechanism may be different from the electron-trapping mechanism. The details will be discussed later in the bias-dependent charge trapping process section.

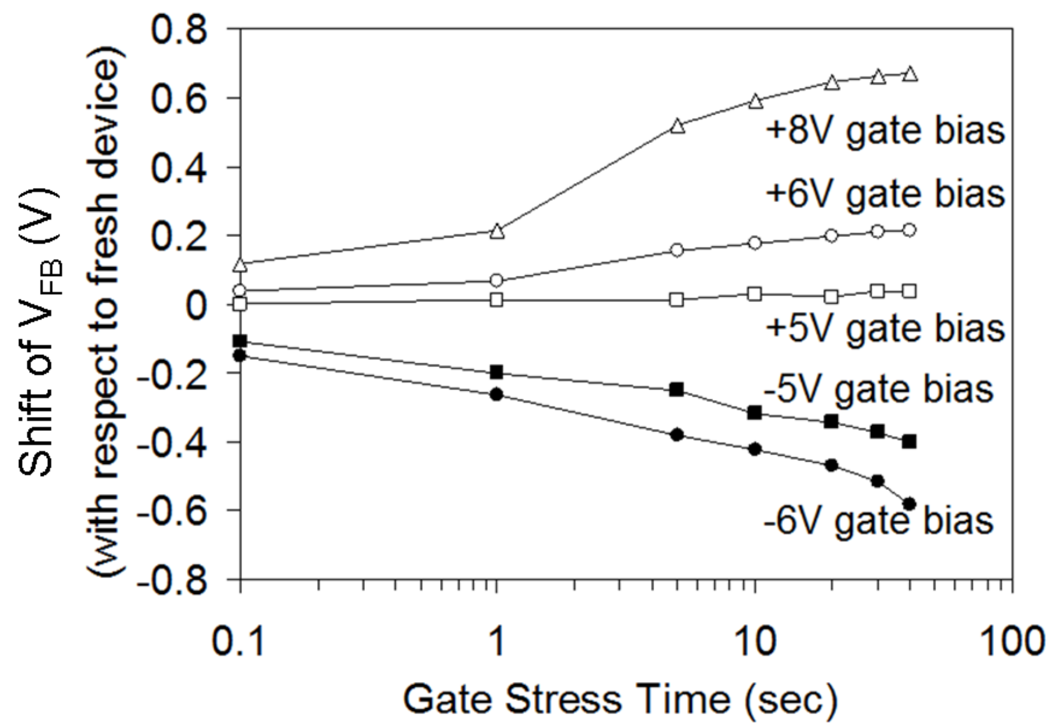

Figure 47. Shift of V_{FB} as a function of gate stress time under different constant negative or positive gate stress biases.

Figure 48(a) shows C-V curves (measured at 1 MHz) of the nc-RuO embedded capacitor after being stressed at different V_g's for a period of 5 s. Figure 48(b) is the ΔV_{FB} vs. the magnitude of stress V_g. Under the negative V_g stress condition, the ΔV_{FB} increases almost linearly with the magnitude of V_g. The corresponding hole-trapping density is 1.8×10^{12} cm^{-2} after V_g = -10 V stress. Under the positive V_g stress condition, the ΔV_{FB} increases only when the gate bias is below +8 V. Beyond that, it saturates to a value of 0.55 V, which equals a charge density of 1.2×10^{12} cm^{-2}. The saturation of trapped electron density is higher than the density of nc-RuO (8×10^{11} cm^{-2}) in the gate dielectric stack. In average, each nc-RuO traps 1-2 electrons. Therefore, the saturation phenomenon may be due to 1) the Coulomb blockade effect, i.e., the previously-trapped electrons in the deep charge trapping sites may hinder further electron trapping during the trapping process, and 2) the limited supply of electrons in the inversion layer of the p-type Si wafer. On the other hand, the hole-trapping process did not show the saturation phenomenon, and the hole-trapping density is consistently higher than the electron-trapping density.

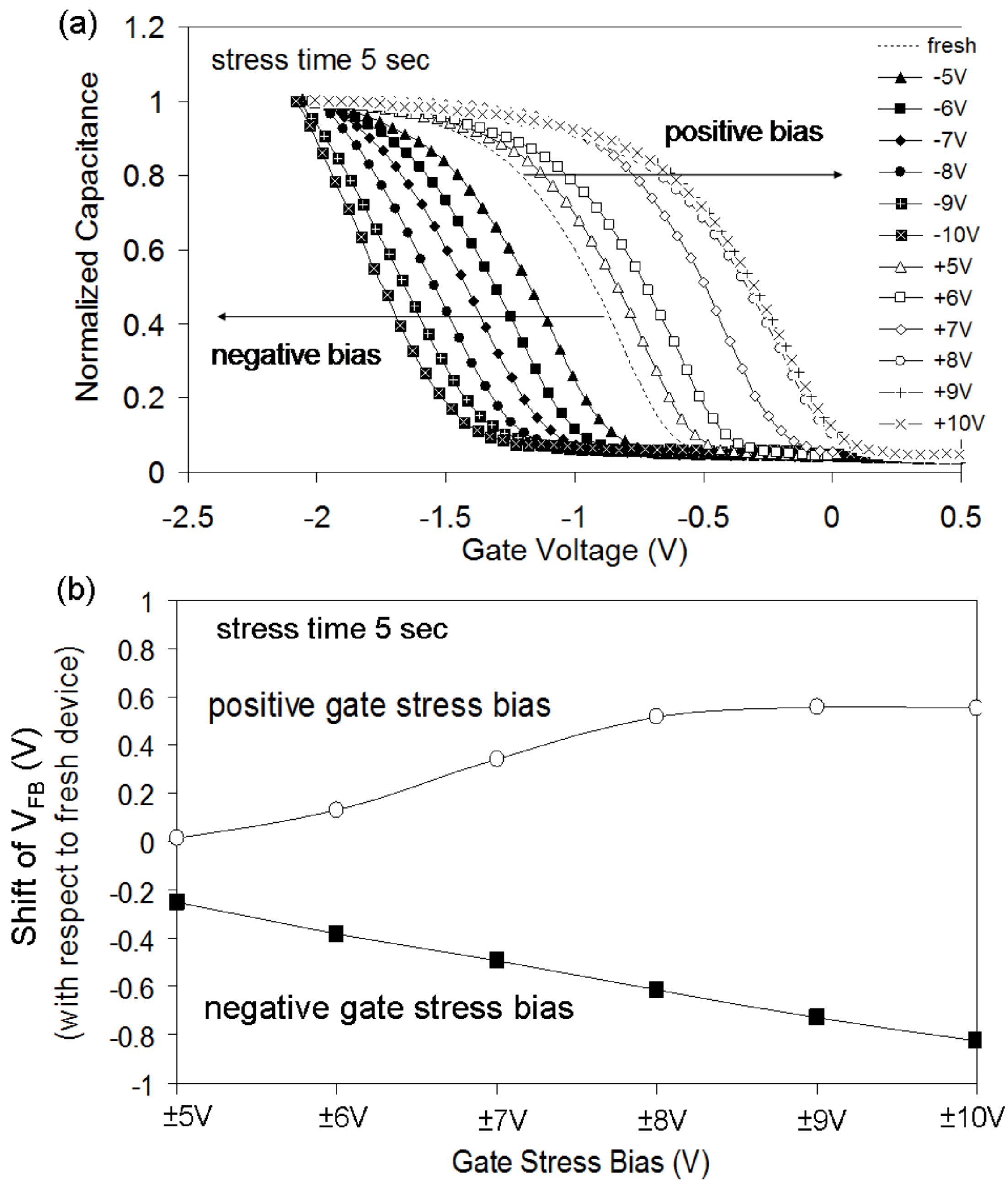

Figure 48. (a) C-V curves (at 1 MHz) before and after stressed at different negative (-5 V to -10 V) and positive (+5 V to +10 V) gate biases and (b) shift of V_{FB} as a function of gate stress bias. The stress time was fixed at 5 s.

4.4.3 Differentiation of Charge Trapping Sites

The large number of trapped charges in the nc-RuO embedded sample may be located in the bulk nc-RuO or at the nc-RuO/ZrHfO interface. In order to distinguish these charge trapping sites, the frequency-dependent C-V and G-V measurements, i.e., from 100 kHz to 1 MHz, were carried out on capacitors. The V_g was swept from -9 V to +9 V to simulate the hole-trapping condition, and swept from +9 V to -9 V to simulate the electron-trapping condition. The results of the frequency-dependent C-V and G-V measurements are shown in Figs. 49 and 50, respectively, which indicate that only the trapped holes, not the trapped electrons, respond to the frequency change. The C-V curves (normalized by the accumulation capacitance) and G-V curves (normalized by the angular frequency and capacitor area) of the control sample are independent of the measure frequency, as shown in insets of Fig. 49 and Fig. 50(a), respectively. Therefore, neither the bulk ZrHfO nor the Si/ZrHfO interface layer is responsible for the frequency-dependent curve shift. For the nc-RuO embedded device, the hole-trapped C-V curve was stretched and the V_{FB} shifted to the positive V_g direction when the measure frequency was decreased from 1 MHz to 100 kHz. Previously, it was reported that charges stored at the nanocrystal/surrounding oxide interface responded to the low measure frequency.[161] Therefore, it is possible that holes trapped at the nc-RuO/ZrHfO interface are responsible for the frequency-dependent C-V shift. The trapped holes may tunnel toward the Si substrate when the band structure moves to near the flat band condition. This is consistent with the hump in the low frequency C-V curve near the V_{FB}.

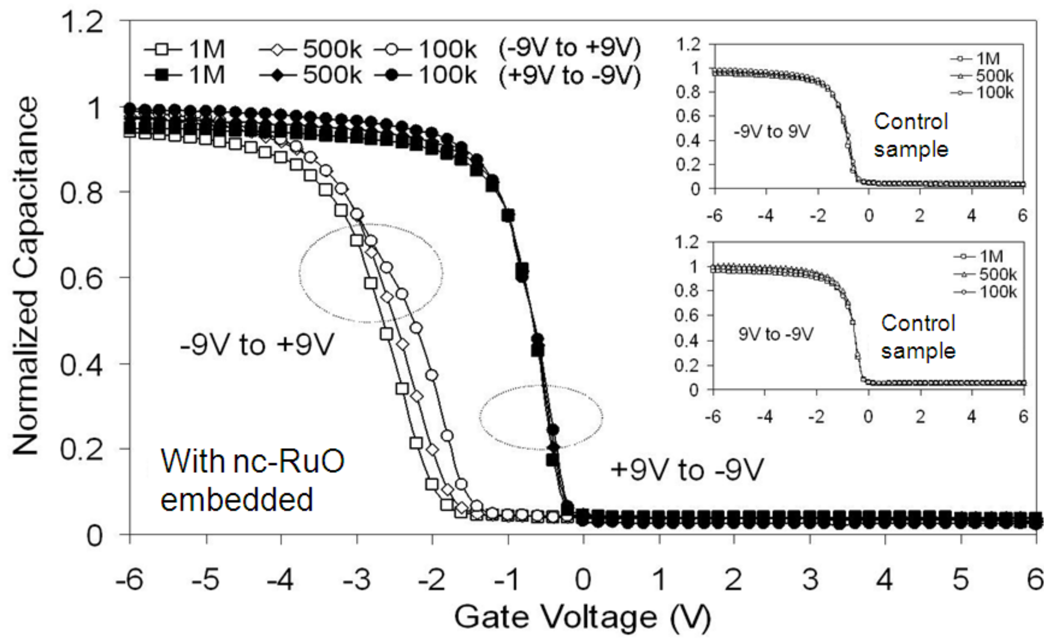

Figure 49. Frequency-dependent C-V curves of the nc-RuO embedded ZrHfO MOS capacitor and the control sample (inset). V_g was swept from -9 V to +9 V and from +9 V to -9 V for hole-trapping and electron-trapping study, respectively.

On the other hand, an obvious frequency dispersion on the hole-trapped G-V curve is also observed, i.e., the peak height lowers and the location moves toward the positive direction when the measure frequency decreases. It was reported that charges trapped to the nc-RuO/ZrHfO interface are subject to the frequency change because they are physically closer location to Si surface.[156,161] Since the nc-RuO/ZrHfO interface traps can keep pace with the low measure frequency, holes trapped at this interface will tunnel back to Si when the V_g is swept to the voltage near the G-V curve's peak position, i.e. V_{FB}. The exchange of holes between the nc-RuO/ZrHfO and ZrHfO/Si interface regions will reduce the energy loss of the capacitor.[125] There will be fewer trapped holes at the low measure frequency than those at the high frequency. This is reflected on the lowering of the G-V peak height and the positive shift of the peak position at the low frequency condition. Therefore, majority of the trapped electrons are located in the bulk nc-RuO site. However, holes are trapped to both the bulk nc-RuO site and nc-RuO/ZrHfO interface.

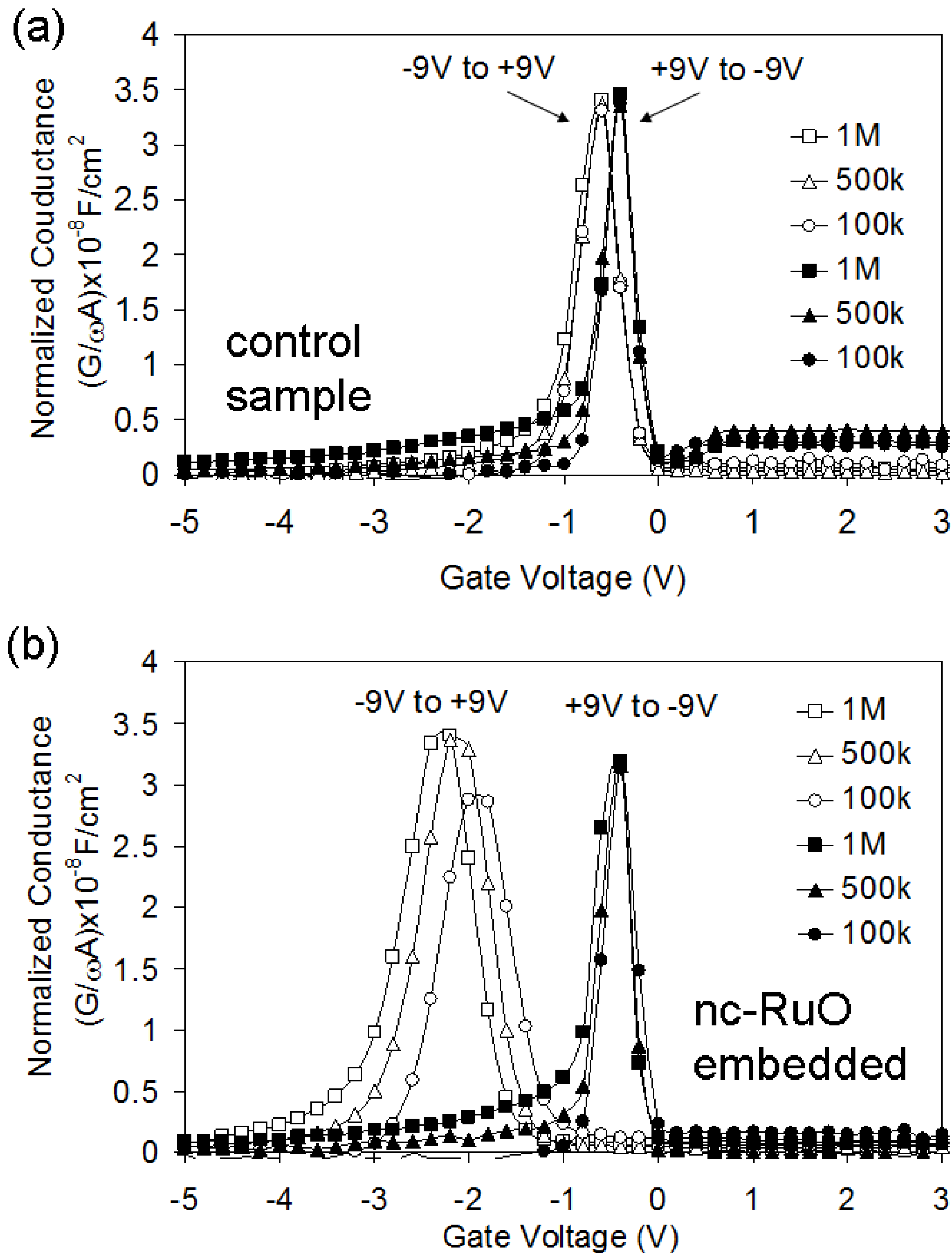

Figure 50. Frequency-dependent G-V curves of (a) control sample and (b) nc-RuO embedded ZrHfO MOS capacitor. V_g was swept from -9 V to +9 V and +9 V to -9 V for hole-trapping and electron-trapping study, respectively.

4.4.4 Differentiation of Deeply- and Loosely-Trapped Charges

Figure 51 shows the schematic energy band diagrams of the nc-RuO embedded ZrHfO MOS capacitor under the (a) unbiased, (b) electron-, and (c) hole-injection conditions, separately. For simplicity, the trap states instead of a thin interface layer at the nc-RuO/ZrHfO contact region are included in the band diagram since the latter's energy band gap and conduction/valance band offsets with respect to the surrounding materials are still unclear. By assuming that the band gap and work function of the nc-RuO are the same as those of the bulk RuO, the conduction band and valance band offsets of nc-RuO with respect to Si are different. According to this diagram, in addition to the bulk nc-RuO site, holes have a high probability to be trapped at the nc-RuO/ZrHfO interface site under the negative V_g bias condition. Shi *et al*.[162] reported that the trapped charges can tunnel back to the Si substrate through the interface defects at Si/tunnel oxide. Therefore, it is reasonable to assume that charges are loosely trapped at the nc-RuO/ZrHfO interface due to the existence of defects. They are easier to detrap than those trapped to the bulk nc-RuO site at the low frequency condition.

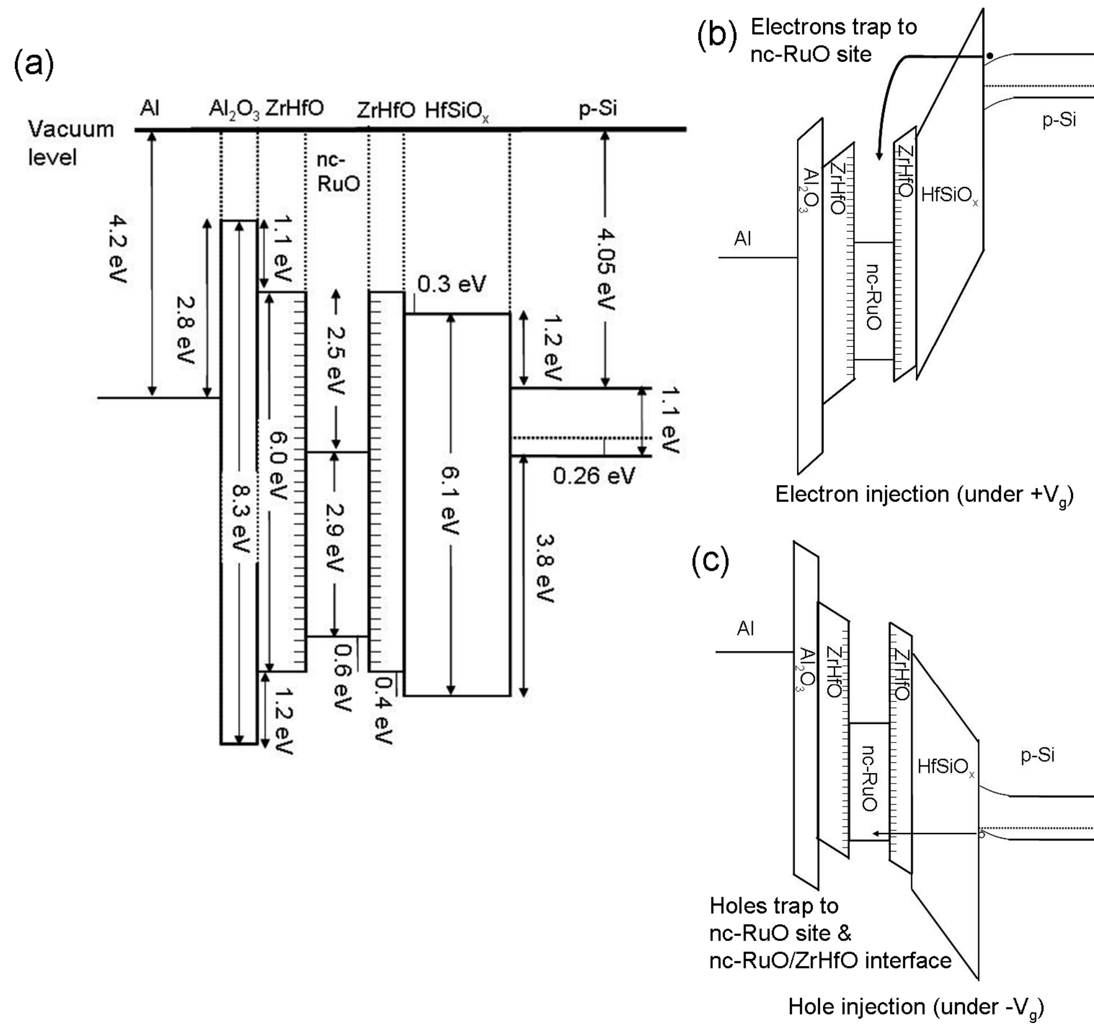

Figure 51. Energy band diagrams of the nc-RuO embedded ZrHfO MOS capacitor under (a) unbiased, (b) electron-injection, and (c) hole-injection conditions.

Figure 52 shows the relaxation current decay characteristics of the nc-RuO embedded sample and the control sample. The capacitor was stressed with a constant V_g of -9 V or +9 V for 10 s. Then, the change of the relaxation current density (J_{relax}) with time was measured at a very small V_g of 0.01 V. The relaxation current is defined as the current leaking through the stack after releasing an applied gate bias. It has an opposite direction to that of the traditional leakage current induced by the applied V_g. The relaxation current of the nanocrystals embedded capacitor is contributed by two components, i.e., the detrapping of trapped charges and polarization/relaxation of the embedded dielectric film.[109] In the nc-RuO embedded capacitor, since holes and electrons may be trapped at different sites, their detrapping characteristics can be different. Their relaxation currents have different behaviors. Figure 52 shows that the nc-RuO embedded sample has a larger J_{relax} than the control sample has, especially for the release of the trapped holes. Although the control sample has poor charge trapping capability, the high-k material's bond polarization or relaxation can contribute to the small J_{relax} upon the release of the stress V_g. However, the high J_{relax} in the nc-RuO embedded capacitor is due to the release of charges trapped to the nc-RuO site. In the frequency-dependent C-V and G-V sections, it was concluded that majority of the trapped electrons are deeply trapped in the bulk nc-RuO, which are difficult to release under the very small V_g measurement condition. On the contrary, since a portion of the trapped holes are loosely retained at the nc-RuO/ZrHfO interface, they may be easily released with the application of a small V_g, which shows as the large J_{relax} in Fig. 52.

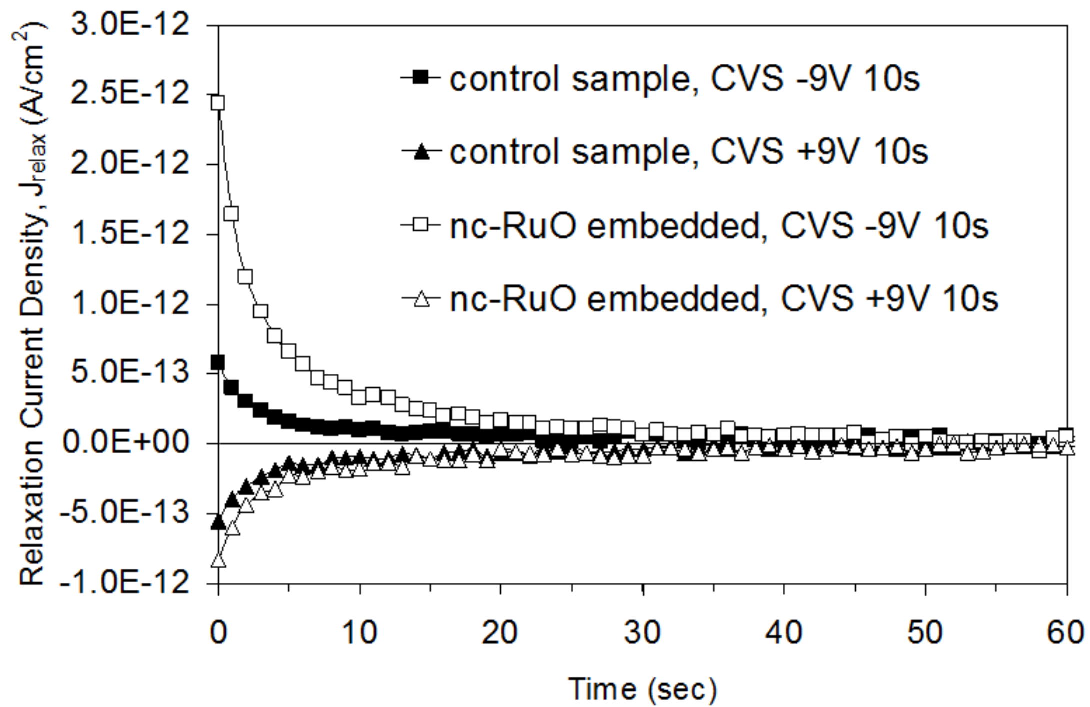

Figure 52. Relaxation current density of the control sample and the nc-RuO embedded ZrHfO MOS capacitor as a function of time after releasing CVS.

4.4.5 Current Transfer Characteristics Contributed by Charge Trapping and Detrapping

The hole-trapping and -detrapping processes of the nc-RuO embedded capacitor were further studied using the J-V curves, as shown in Fig. 53. The polarity of J is defined as positive when the current flows toward substrate and negative when the current flows toward the gate. Figure 53 shows that the significant J-V hysteresis phenomenon is detected when the V_g is swept from 0 V to -5 V (step 1) then immediately back to +5 V (step 2). A reference J-V curve, which was measured from 0 V to +5 V is also included in this figure, which does not trap holes. In step 1, the polarity of J is negative and its magnitude increases with the increase of the $-V_g$. With the increase of $-V_g$, more holes are accumulated to the Si/high-k interface and at the same time, injected to the embedded nc-RuO sites. However, in step 2, the J quickly changes its polarity with a small change of V_g in the -5 V to -4.5 V region. Then, it remains positive with the increases of V_g to the positive direction due to the detrapping of holes. The hysteresis J-V phenomenon can be explained by the Coulomb blockade effect that has been observed in other nanocrystal-based memory devices.[163-164] The trapped holes during step 1 can pose an energy barrier to prevent the subsequently-injected holes from passing through the dielectric stack to the gate electrode in step 2. Since the 2-D spatial density of nc-RuO is $\sim 8\times10^{11}$ cm^{-2}, and the charge trapping density under the sweep range of ±6 V is calculated to be $\sim 1.2\times10^{12}$ cm^{-2} by Eq. 14, in average, no more than 2 charges are trapped by one nc-RuO dot. Therefore, the Coulomb blockade effect plays an important role in the current leakage process.

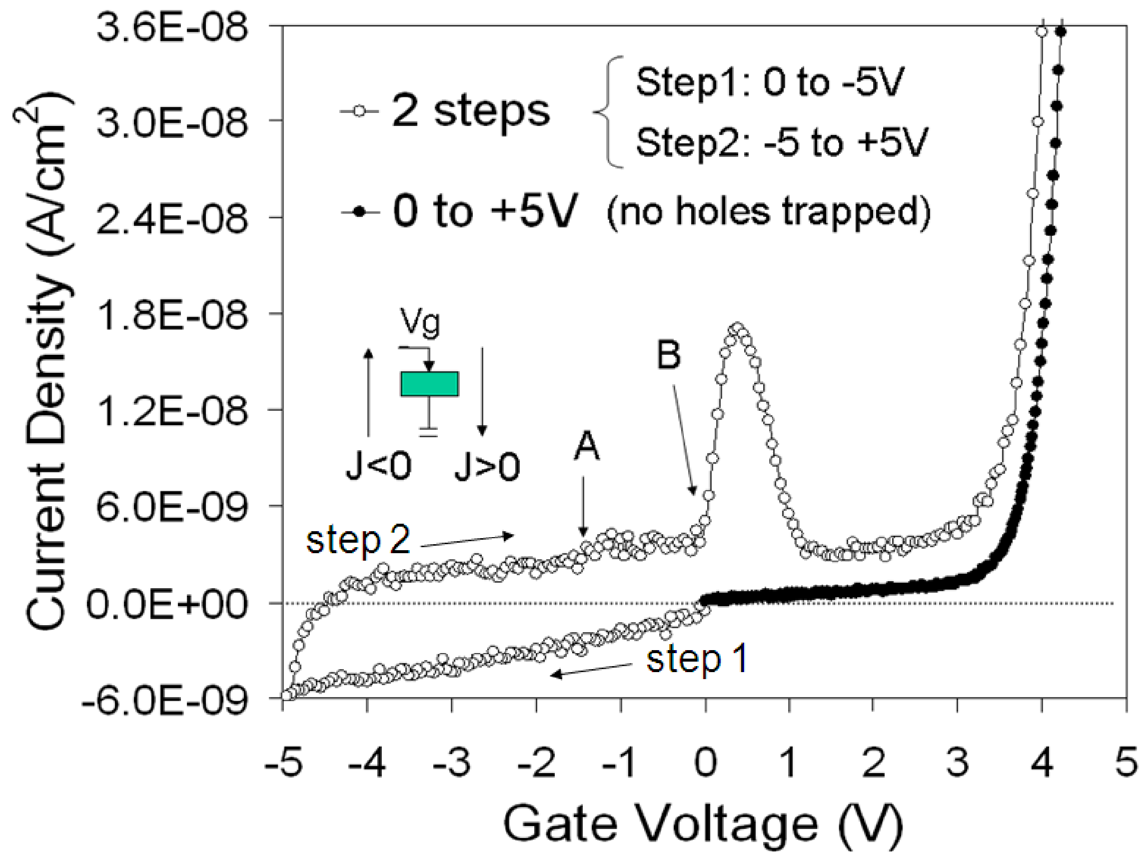

Figure 53. J-V curves of the nc-RuO embedded ZrHfO MOS capacitor with V_g swept from 0 V to -5 V (step 1), then immediately to +5 V (step 2). J-V measured from 0 V to 5 V is also attached.

On the other hand, the step 2 curve contains two jumps while no jumps are observed in the reference J-V curve. The hole-detrapping process is responsible for these jumps. In step 2, when the V_g is moved from -4.5 V toward 0 V, a small jump at point A is observed near V_g = -1.5 V, which is close to the V_{FB} of the forward C-V curve, as shown in the inset of Fig. 43. This current jump is contributed by the sudden detrap of the loosely-trapped holes, which are probably located at the nc-RuO/ZrHfO interface as previously discussed. This detrapping phenomenon becomes obvious when the band structure turns to the flatband condition. A more pronounced current jump at point B is observed at around V_g = 0 V. The change of the V_g polarity causes the further release of a large number of the remaining trapped holes. In the V_g range of +1 V to +3 V, very few remaining holes are released or electrons are injected from the Si substrate, which shows as the very slight increase of J with the increase of V_g. When the V_g is larger than +3 V, the electron injection phenomenon becomes obvious and a significant increase of the J with the increase of V_g is observed.

To further investigate the charge detrapping mechanisms, the capacitor's ramp and relaxation currents, i.e., J_{ramp} and J_{relax}, were measured using the ramp-relax method.[165] First, a stepwise ramping voltage is applied to the capacitor to measure the J_{ramp}. Then, in each step, the J_{relax} is measured at V_g = 0.01 V immediately after removing the gate bias for a short period, i.e., 0.5 s. In general, the J_{ramp} and J_{relax} have opposite polarities. However, once the gate dielectric film breaks down, the J_{rela} abruptly jumps up to a high value and shows the same polarity as the J_{ramp}.

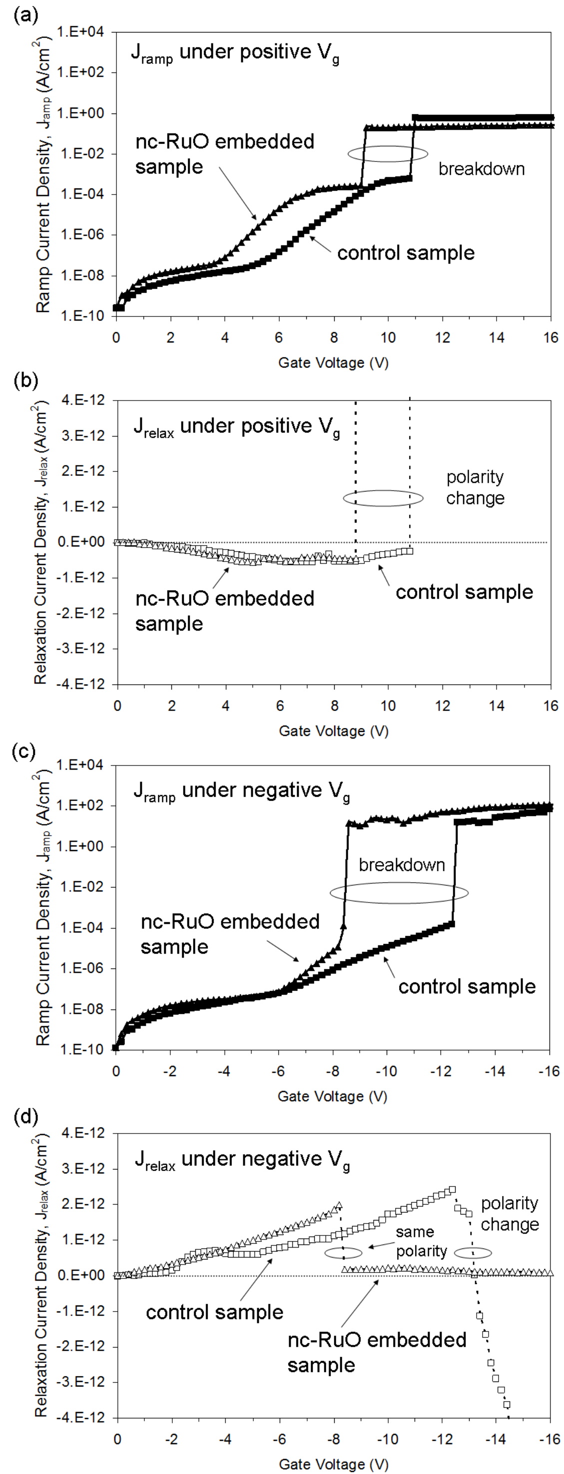

Figure 54. Ramp leakage current-relaxation current curves measured under (a) & (b) positive V_g sweep regime; (c) & (d) negative V_g sweep regime.

The J_{ramp}-V_g and J_{relax}-V_g curves of the control and nc-RuO embedded samples in the positive V_g range are shown in Fig. 54(a) and (b), respectively. Those in the negative V_g range are shown in Fig. 54(c) and (d). The polarity of J_{ramp} is positive when the current flows to the substrate; it is negative when the current flows to the gate electrode. The nc-RuO embedded sample breaks down at a lower V_g than the control sample does because the nc-RuO is conductive. In addition, Fig. 54(b) shows that both samples have similar J_{relax} when the V_g was swept in the positive V_g regime. However, when the V_g was swept in the negative regime, the nc-RuO embedded sample has a larger J_{relax} than the control sample has, as shown in Fig. 54(d). This is especially obvious at the large -V_g condition. The above results are in agreement with the previous discussion that the injected electrons can be deeply trapped in the bulk nc-RuO site while a portion of the injected holes are loosely trapped at the nc-RuO/ZrHfO interface. The detrapping of the loosely-trapped charges is for the cause of the large initial J_{relax}. However, the deeply-trapped charges are difficult to release at the small V_g, which do not contribute to the additional relaxation current. Previously, it was reported that the J_{relax} of the non-embedded high-k capacitor changed the polarity abruptly when the dielectric layer broke.[166] The same phenomenon occurs on the control sample in both the negative and positive V_g regimes. It is also observed on the nc-RuO embedded sample in the positive V_g regime, i.e., electrons-trapped condition. Therefore, even though the high-k film breaks down, the deeply-trapped electrons are still strongly held in the bulk nc-RuO sites. On the contrary, for the nc-RuO embedded sample swept in the negative regime, i.e., holes-trapped condition, the J_{relax} retains the same polarity before and shortly after the breakdown. This is because the loosely-trapped holes, i.e., at the nc-RuO/ZrHfO interface, can be released

in spite of the breakdown of the bulk ZrHfO film.

4.4.6 Retention Characteristics of Holes and Electrons

Figure 55 shows the charge retention characteristics of the nc-RuO embedded capacitor. For the electron retention condition, the capacitor was stressed at V_g = +9 V for 10 s. For the hole retention condition, the capacitor was stressed at V_g = -9 V for 10 s. The inset of Fig. 55 shows the short-term, i.e., < 200 s, retention curves. About 25 % of the trapped holes were lost in the first 50 s after the release of the stress V_g. This is similar to the other report on the hole-detrapping phenomenon.[167] However, a very small portion of the trapped electrons were released in the first 50 s. After release of the stress V_g for 100 s, both holes and electrons were slowly released with a logarithmic decay rate of 0.025 and 0.024, respectively. The difference in electron and hole retention characteristics is consistent with previous discussions that electrons are strongly trapped in the bulk nc-RuO site but holes are either strongly trapped in the bulk nc-RuO site or loosely trapped at the nc-RuO/ZrHfO interface. The loosely-trapped holes are quickly detrapped after the removal of the bias V_g. Afterwards, the strongly-trapped holes are slowly and gradually released. Figure 55 shows that a large gap of 0.98 V between the two curves is obtained after 3.6×10^4 s. This kind of charge retention characteristics is suitable for the memory application.[168] The long-term retention curves of holes and electrons can be separately fitted by the logarithmic approximation, which projects a distinguishable 0.53 V window after 10 years.

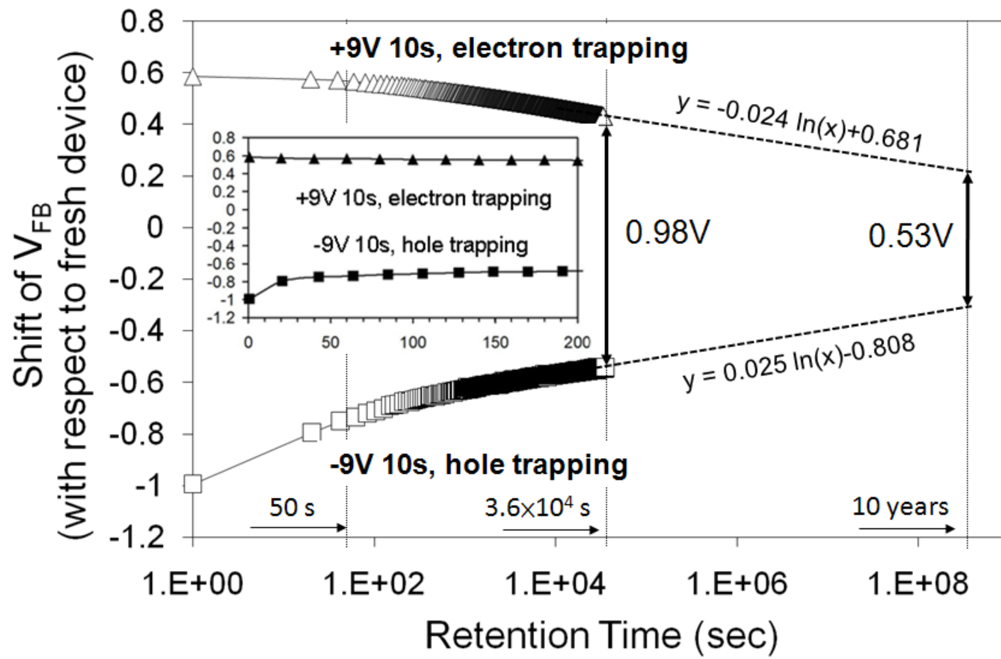

Figure 55. Electron and hole retention characteristics of the nc-RuO embedded ZrHfO MOS capacitor. Electrons were injected at +9 V for 10 s and holes were injected at -9 V for 10 s. The first 200 s measurement of the retention curves are shown in the inset.

4.5 Summary

Material properties and memory functions of the nc-RuO embedded ZrHfO MOS capacitor have been studied in a fundamental way, i.e., trapping and detrapping mechanisms of holes and electrons. The formation of discretely-dispersed nc-RuO dots within the amorphous ZrHfO high-k film after the 950 °C RTA condition has been confirmed. An interface layer between the nc-RuO and surrounding ZrHfO, which has a structure different from that of the bulk ZrHfO film, was detected by XPS. This device has a large memory window of 1.72 V with the V_g sweep range of ±9 V, which is mainly contributed by the hole-trapping mechanism. The control sample has negligible charge trapping capability. Both V_g bias- and time-dependent charge trapping tests show that hole trapping is more efficient than electron trapping, which may be due to the different charge supply mechanisms and trapping sites. Frequency-dependent C-V and G-V measurement results show that the trapped holes are sensitive to the measure frequency, while the trapped electrons are not. The hole- and electron-trapping mechanisms can be explained with the detailed energy band diagram. Both holes and electrons can be deeply trapped to the bulk nc-RuO site, while a portion of holes are loosely trapped to the nc-RuO/ZrHfO interface. This phenomenon is also reflected in the different charge detrapping properties such as different magnitude of the relaxation currents and ramp-relax current response when the capacitor is broke down. The retention result shows that the loosely-trapped holes at the nc-RuO/ZrHfO interfaces are released quickly, while the deeply-trapped holes and electrons in the bulk nc-RuO sites can be strongly held. The nc-RuO embedded ZrHfO high-k dielectric structure can provide a large memory window for a long period of time, which is suitable for the nonvolatile memory application.

CHAPTER V

DUAL-LAYER NANOCRYSTALLINE INDIUM TIN OXIDE AND ZINC OXIDE EMBEDDED ZrHfO HIGH-K NONVOLATILE MEMORIES*

5.1 Introduction and Motivation

In Chapter IV, discrete nc-RuO dots embedded ZrHfO high-k MOS capacitor has been fabricated and studied. This kind of device showed promising memory characteristics that can meet the nonvolatile memory operation requirements. Although nc-RuO has been demonstrated that can serve as good charge trapping medium, its valence band offset with respect to the surrounding ZrHfO is relatively low, i.e., ~ 0.6 eV. In this case, the trapped holes may tunnel back to Si substrate without overcoming a large energy barrier. Therefore, replacing nc-RuO with other conductive oxide materials that have a higher energy band offset structure with respect to ZrHfO is important. In addition, when nano-size conductive oxides are used as the charge trapping media, they can offer advantages of both metals and semiconductors due to their high work functions and large band gaps.[72] For example, they may provide a large density of states around the Fermi level,[60] meanwhile allow mid-gap trap states for a high capacity and deep charge trapping.

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*Part of data reported in this chapter is reproduced from "Nonvolatile Memories with Dual-Layer Nanocrystalline ZnO Embedded Zr-Doped HfO_2 High-k Dielectric", by Chen-Han Lin and Yue Kuo, *Electrochemical and Solid-State Letters*, 13(3), H83-H86 (2010), by permission of ECS-The Electrochemical Society.

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Among conductive oxide films, indium tin oxide (ITO) and zinc oxide (ZnO) are particularly promising due to their well-known material properties and compatibility to the standard MOSFET process. ITO is an important nanocrystal candidate for the FG memory structure because of its large work function (~4.7 eV) and wide band gap (~3.5 eV).[169-170] ITO has been also used as the hole-injecting anode in the organic light emitting device and many other optoelectronic products,[171] which demonstrate the charge conducting capability of ITO. On the other hand, ZnO is also a wide band gap (~3.3 eV) semiconductor with a large work function (~4.5 eV).[71,172] ZnO can be prepared into the nanocrystalline form for various electronic and optoelectronic applications.[173-174] The sputtered ZnO film is a n-type semiconductor containing a large number of defects, such as Zn interstitial (Zn_i) and oxygen vacancy (V_o), which may work as deep trapping sites, i.e., below the conduction band edge.[175-177] Table 4 compares the band structure characteristics among nc-RuO, -ITO and -ZnO, e.g., band gap, work function, and conduction band (E_c) and valence band (E_v) offsets with respect to ZrHfO film. For the nc-ITO and -ZnO, their E_c and E_v offsets with respect to ZrHfO are both in a good range, therefore, good charge retention properties are expected.

Table 4. Comparison of energy band gap, work function, conduction band, and valence band offsets with respect to ZrHfO film of nc-conductive oxide candidates: nc-RuO, -ITO, and -ZnO.

unit: eV	E_g	work function	E_c offset to ZrHfO	E_v offset to ZrHfO
nc-RuO	~2.9	~5	~2.5	**~0.6**
nc-ITO	~3.5	~4.7	**~1.3**	**~1.2**
nc-ZnO	~3.3	~4.5	**~1.4**	**~1.3**

Moreover, for the nc-RuO embedded ZrHfO capacitor discussed in Chapter IV, not all the injected carriers can be totally trapped in the FG structure during the programming process. This is judged from the monotonic relationship in the gate stress-time dependent charge trapping process. Some of them can keep tunneling toward the gate electrode, which degrades the programming efficiency. In order to overcome this concern, the FG memory that contains dual nanocrystal layers structure has been fabricated and studied in this study. Figure 56 illustrates the advantages of the dual-layer FG structure over the single-layer counterpart: (a) higher nanocrystal (i.e., charge trapping site) density, (b) better programming efficiency, and (c) better retention properties. During the programming condition, the programming efficiency can be improved by adding the top nanocrystal layer in the gate dielectric stack, which not only increases the opportunity to trap charges, but also prevents charge leaking from the bottom nanocrystal layer from reaching the gate electrode. In addition, during the retention condition, the charge loss from the top nanocrystal layer can be alleviated due to the Coulomb blockade effect caused by the charges trapped in the bottom nanocrystal sites.[178] In this study, the single- and dual-layer nc-ITO and -ZnO embedded ZrHfO MOS capacitors have been fabricated and studied for their material and electrical properties. This kind of FG structure is potentially important for next-generation nonvolatile memory applications.

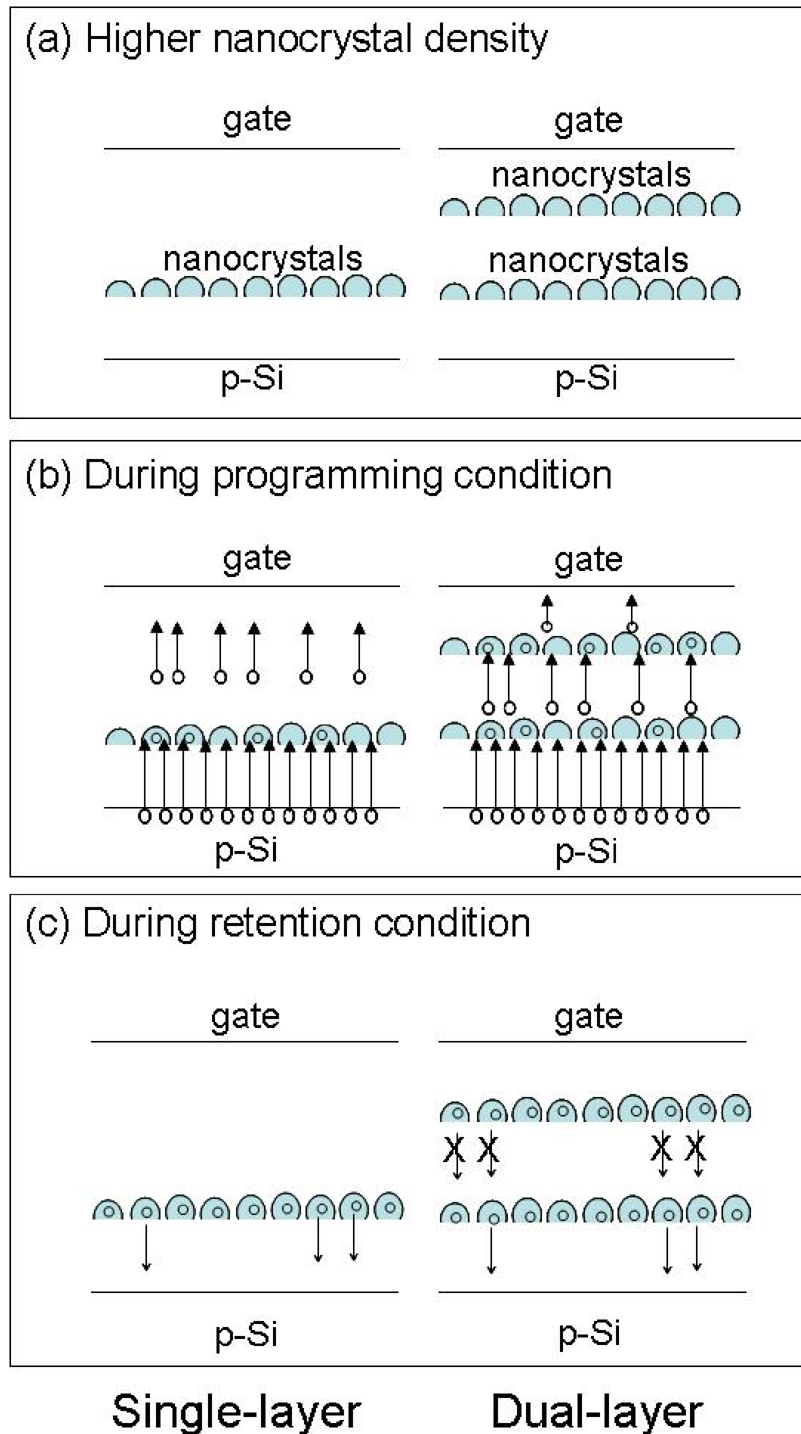
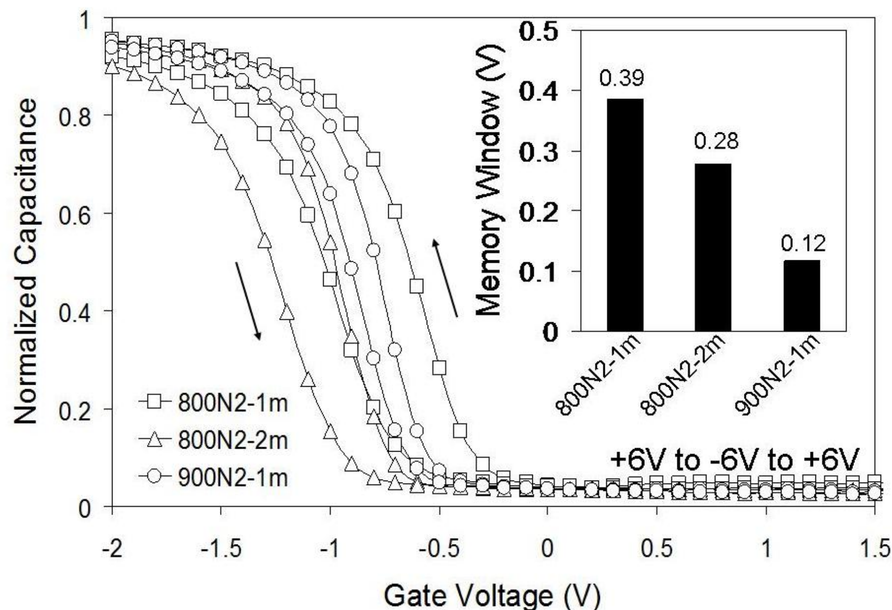


Figure 56. Illustrations of advantages of using dual-layer FG structure: (a) Higher charge trapping site density, (b) better programming efficiency, and (c) better retention properties.

5.2 Experimental

MOS capacitors composed of single and dual nc-ITO and -ZnO layers embedded in the ZrHfO high-k film were fabricated on the p-type Si (10^{15} cm^{-3}) wafer. For the single-layer nc-ITO and nc-ZnO embedded samples ("single nc-ITO" and "single nc-ZnO" from now on), the bottom ZrHfO (tunnel oxide)/ITO or ZnO/top ZrHfO (control oxide) stack was sputter-deposited sequentially in one-pump-down without breaking the vacuum. Both ZrHfO layers were deposited from the same Zr/Hf (12/88 wt %) target at 60 W in the 1:1 Ar/O_2 ambient, i.e., 2 min for the tunnel oxide and 10 min for the control oxide, respectively. The ITO layer was sputtered from a ITO (In/Sn:90/10 wt %) target at 80 W in the Ar ambient for 30 s. The ZnO layer was sputtered from a Zn target at 60 W in the 1:1 Ar/O_2 ambient for 3 min. The above ITO and ZnO sputtering deposition conditions could deposit a ~2 nm film based on the experienced deposition rate under the same sputtering conditions. Recall the experimental part in Chapter IV, the optimized Ru deposition time is 1 min, which also can deposit a ~2 nm film, to be embedded in the ZrHfO stack for memory applications. On the other hand, for the dual-layer nc-ITO and nc-ZnO embedded samples ("dual nc-ITO" and "dual nc-ZnO" from now on), the film deposition conditions are the same as those of the single-layer samples except that the control ZrHfO layer in the latter was replaced with the ZrHfO (5 min)/ITO (30 sec) or ZnO (3 min)/ZrHfO (5 min) tri-layer. The control sample, i.e., containing only the ZrHfO gate dielectric without the embedded nanocrystals layer, was prepared, i.e., with a sputtering time of 12 min, for comparison. All samples were treated with the post deposition annealing (PDA) step using a RTA system at either 800 ^oC or 900 ^oC under the N_2 ambient for 1 min. Another PDA at 800 ^oC under the N_2 ambient for a longer time,

i.e., 2 min, was also carried out. The gate electrode was composed of the sputtered aluminum (Al), which was patterned with a lithography step and wet etched into dots of the 100 μm diameter. The backside of the wafer was deposited with Al for the ohmic contact. The complete capacitor was annealed by RTA in forming gas (N_2/H_2:90/10) at 300 ^oC for 5 min. Figure 57 shows the 1 MHz C-V hysteresis curves and corresponding C-V windows (insets) of (a) single nc-ITO and (b) single nc-ZnO samples prepared under different PDA conditions. Both samples show a largest memory window under the PDA at 800 ^oC for 1 min. The memory window decreases with the increase of the annealing temperature and annealing time may be attributed to the thicker Si/ZrHfO interface layer grown. The decreased electric filed drop across the tunnel oxide layer lowers the coupling between the FG and Si substrate, which decreases the charge trapping phenomenon. Therefore, in this study, only the capacitors annealed at 800 ^oC for 1 min were investigated.



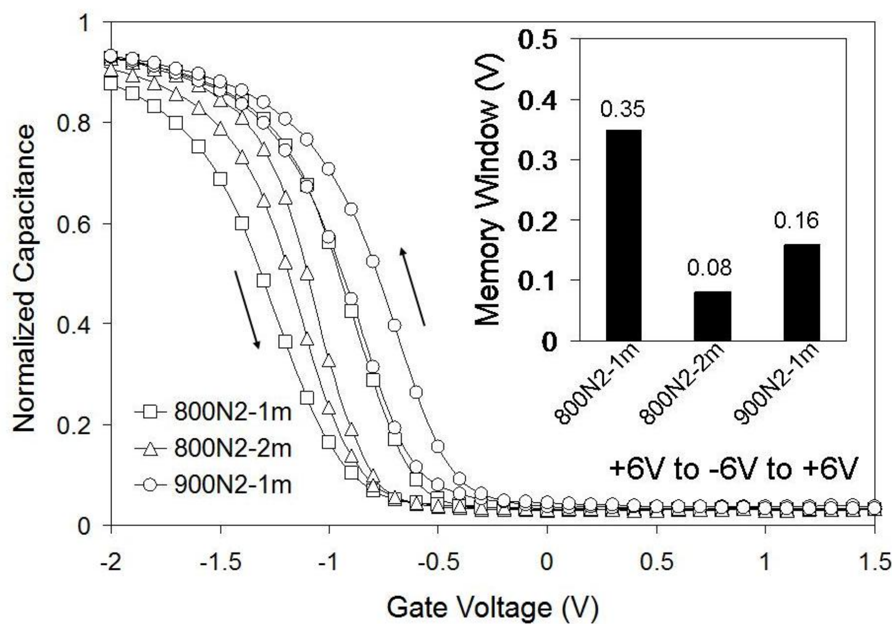


Figure 57. C-V hysteresis curves (measured at 1 MHz) and corresponding memory windows (insets) of (a) single nc-ITO and (b) single nc-ZnO samples prepared under different PDA conditions, i.e. at 800 ^{o}C for 1 min (800N2-1m) and 2 min (800N2-2m), and at 900 ^{o}C for 1 min (900N2-1m).

5.3 Material and Electrical Properties of Single and Dual nc-ITO Embedded ZrHfO High-K Gate Dielectric Stacks

5.3.1 Physical and Chemical Properties of Single and Dual nc-ITO Embedded ZrHfO Bulk High-K Films and Interface Layers

Figure 58(a) shows the HRTEM micrograph of the control sample. There is no visible lattice fringe observed, therefore, the ZrHfO film is amorphous even after the high temperature PDA step. The XRD pattern of the control sample does not contain ZrHfO crystalline peaks, as shown in Fig. 58(b), also confirms the amorphous structure in the ZrHfO film. Figure 59 shows the HRTEM micrographs of the (a) single- and (b) dual-layer ITO embedded ZrHfO gate samples. For the single nc-ITO sample, the discrete nanodot, as highlighted in the circle, embedded in the amorphous ZrHfO film is clearly observed. The nanodot has a lattice spacing of about 0.296 nm corresponding to the ITO (222) orientation.[179] For the dual nc-ITO sample, two separate layers of discrete nanodots are observed. The separation of the top and bottom nc-ITO layers is important to the device's leakage current and charge retention characteristics.[178] Figures 58(a) and 59 show that the total thickness of the complete high-k stack increases with the inclusion of the nc-ITO film, i.e., from 5.4 nm (control sample) to 6.7 nm (single nc-ITO sample) and 8.3 nm (dual nc-ITO sample). An interface layer (IL) is observed between the Si wafer and the ZrHfO layer. The IL thickness increases with the increase of the number of the embedded nc-ITO layer, i.e., 3.4 nm in the control sample, 4.3 nm in the single nc-ITO sample, and 4.6 nm in the dual nc-ITO sample. Previously, it was reported that oxygen diffusion through the high-k film, which contains grain boundaries or defects, is easier than that through the amorphous one.[152] Compared with the control sample that contains

amorphous ZrHfO film, the nc-ITO embedded sample contains defects, e.g., the nc-ITO/ZrHfO interface region. The ITO sputtering process also contains oxygen. They all enhance the Si/ZrHfO interface layer growth.

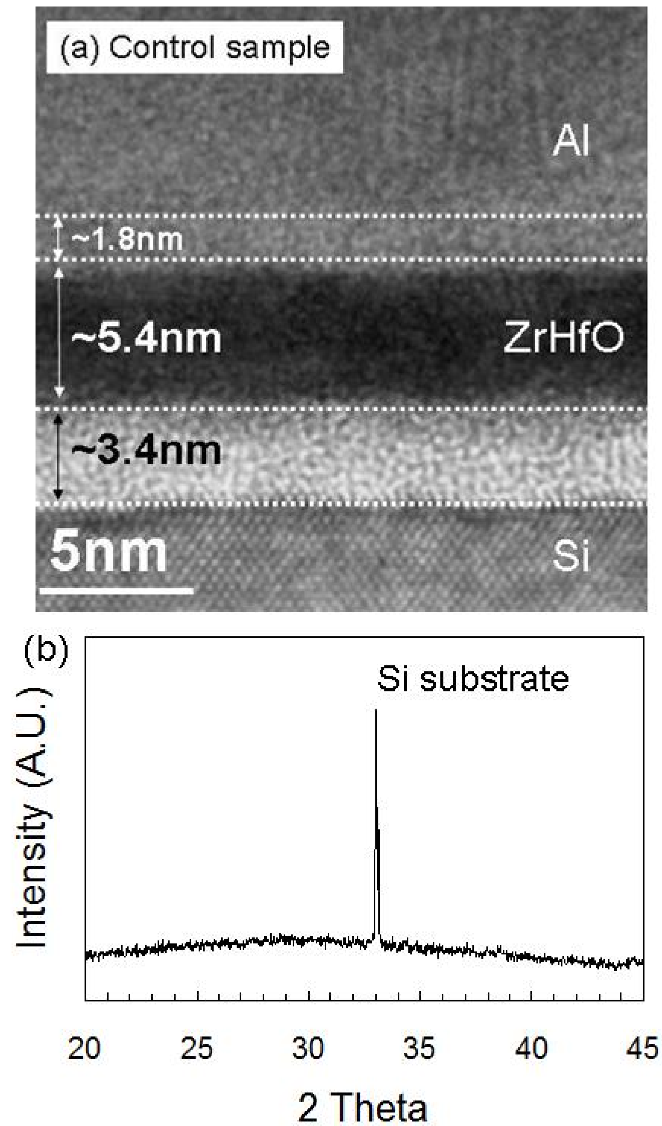


Figure 58. (a) Cross-sectional HRTEM micrograph and (b) XRD pattern of control sample.

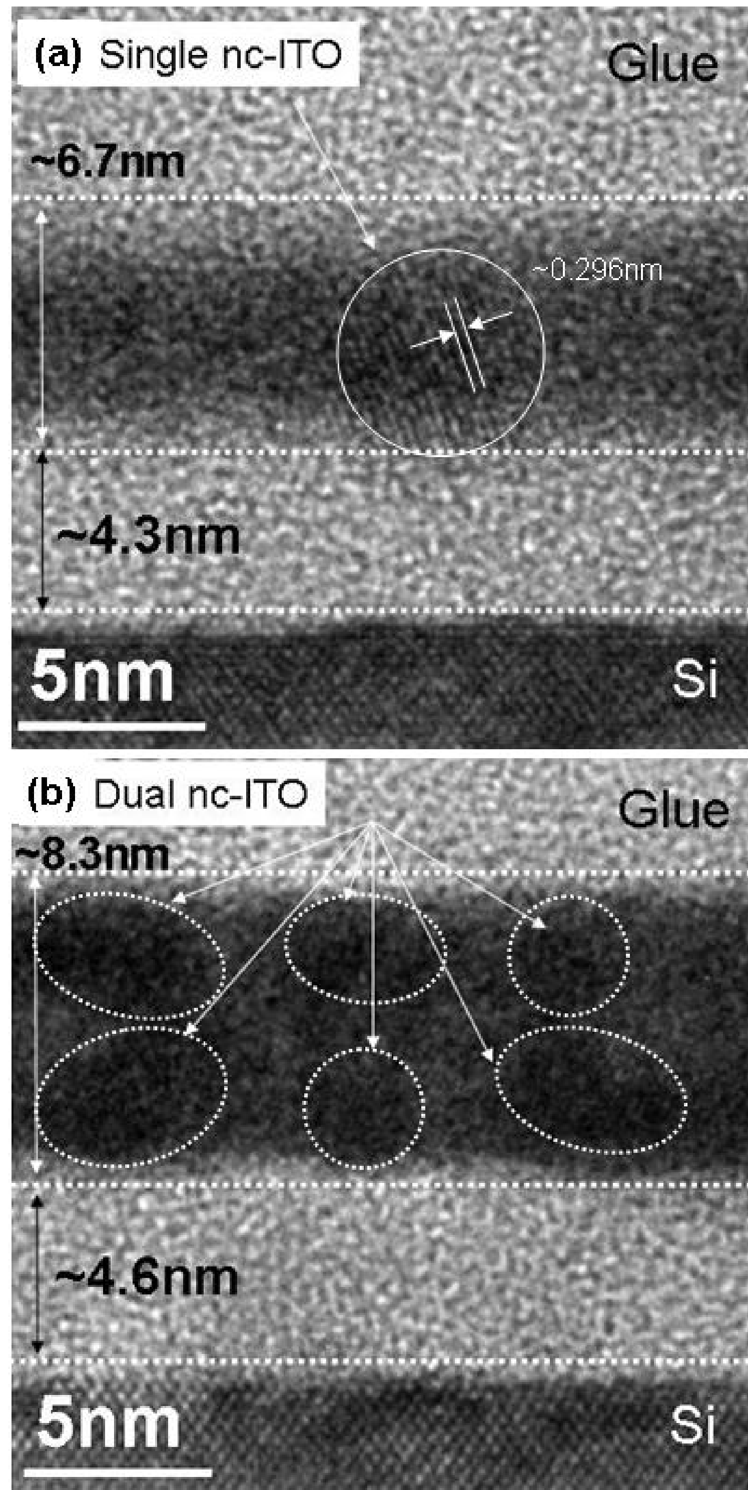


Figure 59. Cross-sectional TEM micrographs of (a) single-layer nc-ITO and (b) dual-layer nc-ITO embedded ZrHfO gate stacks on Si.

Figure 58(a) shows that another interface layer, e.g., 1.8 nm thick, was formed between the Al electrode and underneath ZrHfO. It has the Al_2O_3 structure judged from the Al 2*p* XPS spectrum, as shown in Fig. 60(a). This interface layer has a high energy barrier with respect to the Al gate, i.e., 2.8 eV.[150] It adds to the effective thickness of the control oxide layer, which greatly reduces the possibility of injection of electrons from the gate electrode to the high-k stack under the negative gate bias condition. Figure 60(b) shows the EDS spectrum of the Si/ZrHfO interface layer. It contains Hf, Si, and O, probably contributed by the Hf-silicate ($HfSiO_x$) structure.[180] Since $HfSiO_x$ has relatively low conduction and valance band offsets with respect to Si compared with those of SiO_2,[130] charges can be easily injected to the high-k stack, which favors the programming efficiency.

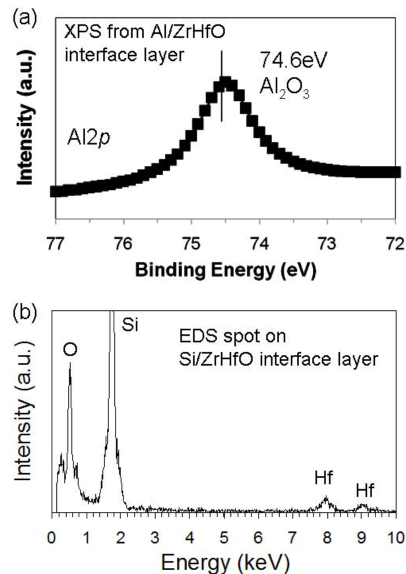


Figure 60. (a) Al 2*p* XPS spectrum of Al/ZrHfO interface layer. (b) EDS spectrum of Si/ZrHfO interface layer.

Figure 61(a) shows the top-view TEM micrograph of the single-layer nc-ITO on top of the ZrHfO film, which has a 2-D spatial density of about 1.8×10^{12} cm^{-2}. The grain size of nc-ITO dots is 3 nm to 5 nm. Figure 61(b) shows the XRD pattern of the dual-layer nc-ITO embedded ZrHfO sample, which confirms the (222) crystalline structure of the ITO.

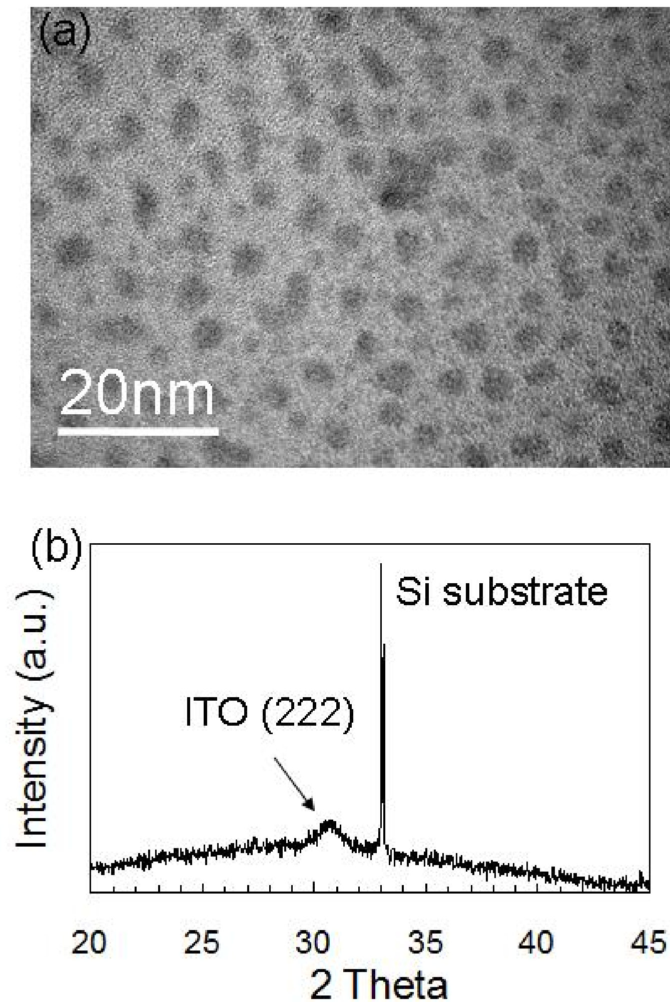


Figure 61. (a) Top-view TEM micrograph and (b) XRD pattern of single- and dual-layer nc-ITO embedded ZrHfO films, respectively.

Figure 62 shows the XPS Hf 4*f* spectra of the (a) control, (b) single, and (c) dual nc-ITO embedded samples. All figures contain the Hf $4f_{7/2}$ peak with a binding energy (BE) of 17.2 eV, which can be deconvoluted into the Hf-O and Hf-Si-O components. These components are probably contributed by the bulk ZrHfO film and $HfSiO_x$-like interface at the Si wafer contact region.[154] The intensity difference between the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peaks decreases with the increase of the number of the embedded nc-ITO layers. Compared with the control sample, both nc-ITO embedded samples contain an extra Hf $4f_{7/2}$ peak with the BE 17.8 eV, which is contributed by the $HfSiO_x$-like structure at the Si interface or other Hf-related bonds in the bulk high-k film. The latter is more possible than the former because 1) the area ratio of the 17.8 eV peak to the complete Hf 4*f* peak increases from 28 % in the single nc-ITO sample to 40 % in the dual nc-ITO sample, and 2) the Si 2*p* peak (shown in Fig. 63(a)) is barely detectable in these samples and its intensity decreases in the order of the dual nc-ITO, the single nc-ITO and the control samples due to the change of the high-k stack layer thickness. Therefore, it is possible that an interface layer is formed at the nc-ITO/ZrHfO interface region within the bulk high-k stack.

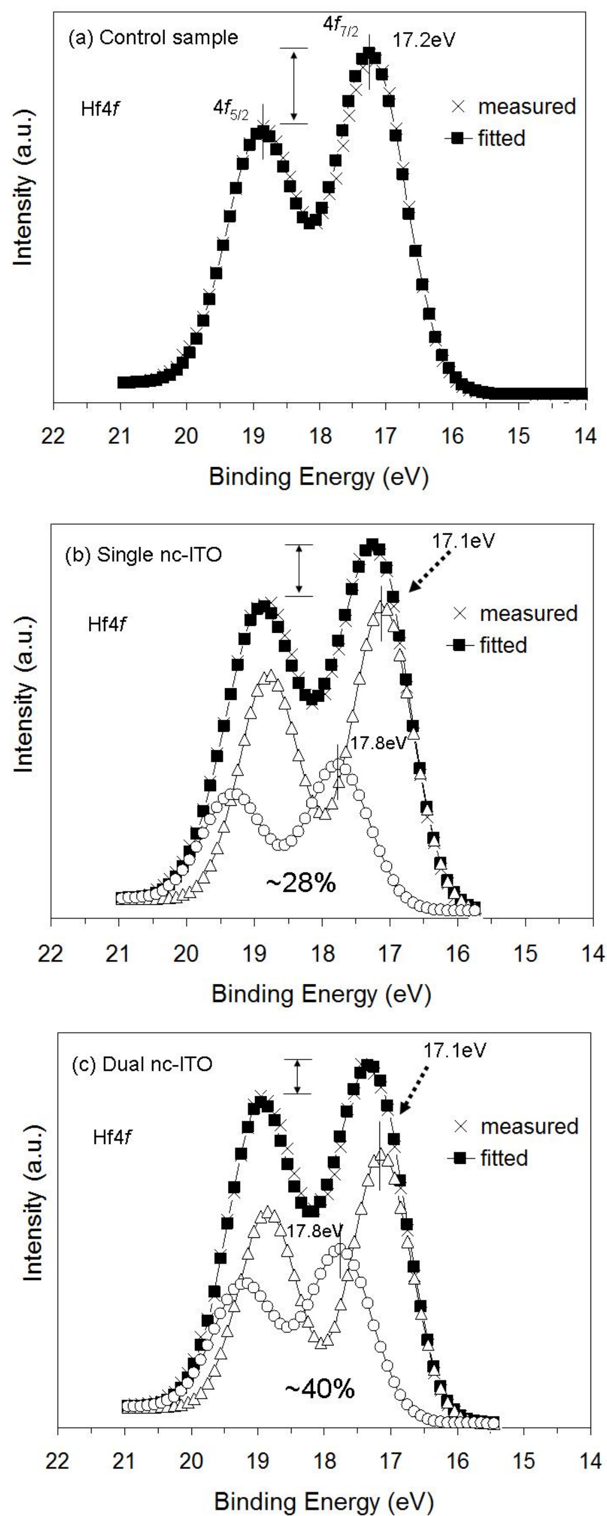


Figure 62. XPS Hf 4*f* spectra and corresponding peak deconvolution of (a) control, (b) single nc-ITO, and (c) dual nc-ITO samples.

Figure 63(b) shows that the intensity difference between the Zr 3$d_{5/2}$ and Zr 3$d_{3/2}$ peaks decreases with the increase of the number of the nc-ITO layers, which follows the same trend as the change of the Hf 4*f* peak intensity. Therefore, Zr may be also involved in the formation of the nc-ITO/ZrHfO interface layer. Figure 63(c) and (d) show the XPS spectra of In 3*d* and Sn 3*d* of the single and dual nc-ITO embedded samples, respectively. Both In and Sn are fully-oxided, i.e., in the In_2O_3 and SnO_2 forms. The peak height and size of these elements increase with the number of the embedded ITO layers because the dual nc-ITO sample contains more In and Sn than the single nc-ITO sample does.

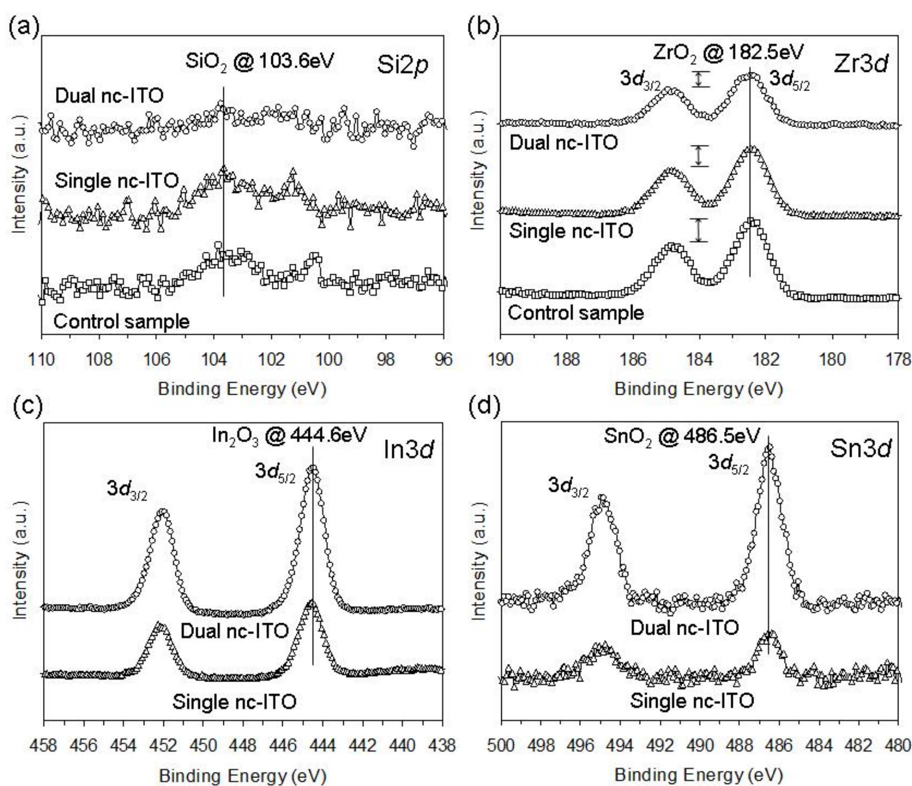


Figure 63. (a) Si 2*p*, (b) Zr 3*d*, (c) In 3*d*, and (d) Sn 3*d* XPS spectra of control, single and dual nc-ITO samples.

5.3.2 Electrical Properties of Single and Dual nc-ITO Embedded ZrHfO High-K MOS Capacitors

Dual-Layer Effects on Memory Functions Contributed by Charge Trapping

Figure 64 shows the C-V hysteresis curves (measured at 1 MHz) of (a) single and (b) dual nc-ITO samples with the V_g being swept from positive to negative (forward), and then back to positive (backward), in the range of ±3 V to ±7 V. Figure 64(c) shows the C-V hysteresis curve of the control sample measured at V_g = ±7 V. The very small gap between the forward and backward curves of the control sample indicates its poor charge trapping capability. However, when the nc-ITO dots are embedded in the ZrHfO film, the C-V hysteresis phenomenon becomes obvious. For example, the charge trapping densities (Q's) of the single and dual nc-ITO samples under the V_g = ±7 V condition are estimated to be 1.8×10^{12} cm^{-2} and 3.1×10^{12} cm^{-2}, respectively, based on Eq. 14. Therefore, the embedded nc-ITO is an effective charge trapping medium in the bulk ZrHfO film. For both nc-ITO embedded samples, all the forward C-V curves overlap with that of the fresh sample regardless of the magnitude of the initial sweep V_g. This means that the addition of the nc-ITO dots does not enhance the electron-trapping capability. In contrast, their backward C-V curves shift with respect to the magnitude of the -V_g. This means that holes were trapped to the nc-ITO embedded ZrHfO layer, and the amount of holes injected and trapped to the nc-ITO site increases with the magnitude of the -V_g. The forward and backward flatband voltages (V_{FB}'s) and corresponding memory windows, i.e., the difference between the forward and backward V_{FB}'s, of the nc-ITO embedded samples are shown in Fig. 64(d). The dual nc-ITO sample has a larger memory window than the single nc-ITO sample in the same V_g sweep range because the former contains a

larger number of nc-ITO dots.

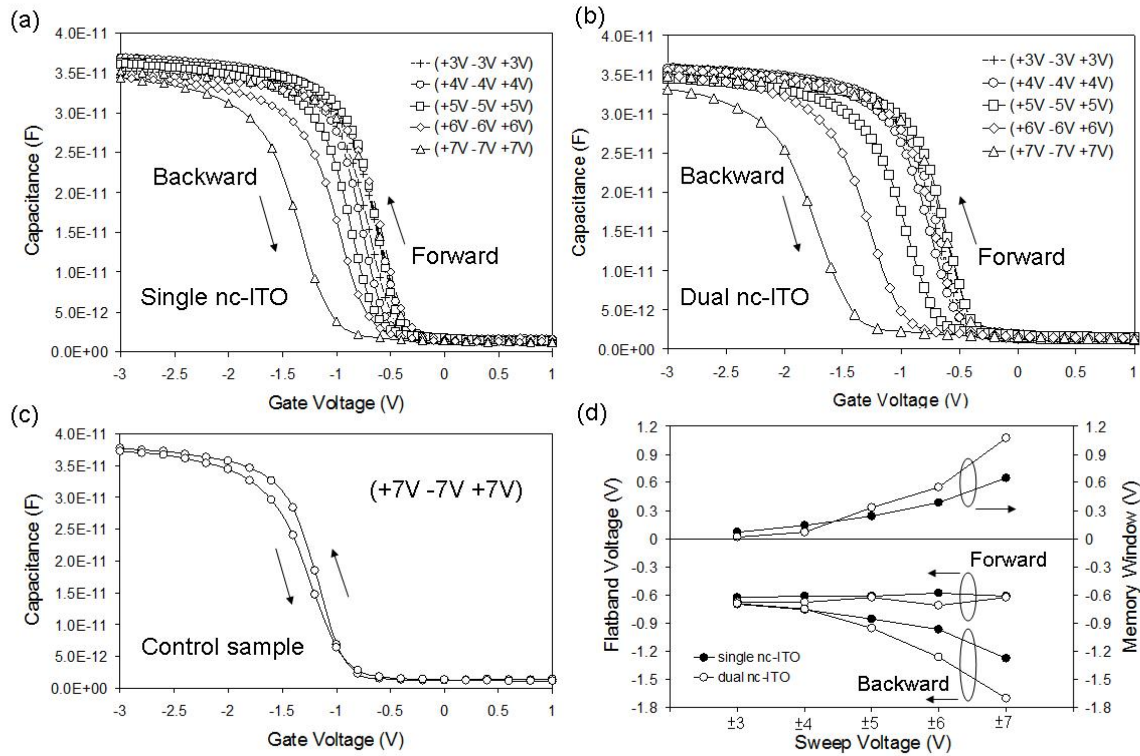


Figure 64. C-V hysteresis curves of (a) single nc-ITO and (b) dual nc-ITO samples in the V_g range of ±3 V to ±7 V, and (c) control sample in the V_g of ±7 V. V_g was swept from positive to negative (forward) then back to positive (backward) in all measurements. (d) Comparison of forward and backward V_{FB}'s and corresponding memory windows summarized from C-V curves in (a) and (b).

Differentiation of Hole and Electron Trapping

In order to further understand the charge trapping mechanism in the nc-ITO embedded sample, C-V curves after the positive and negative V_g stresses were measured. For example, it was stressed at V_g = -8 V for 10 ms to imitate the hole-trapping condition or at V_g = +8 V to imitate the electron-trapping condition. The methodology of this CVS method can be found in Chapter IV. The control sample was also tested under the same condition. Figure 65(b) shows that the control sample has negligible C-V shifts after either +8 V or -8 V stress condition, which further confirms the lack of charge trapping capability of the ZrHfO high-k film and its interface layers. In contrast, the V_g = -8 V stressed nc-ITO embedded samples show negative C-V shifts due to the hole trapping, as shown in Fig. 65(a). The V_{FB} shift of the dual nc-ITO embedded sample is more than doubled that of the single nc-ITO embedded sample, i.e., 0.61 V vs. 0.25 V. Therefore, the embedding of the second nc-ITO layer increases the nc-ITO density and enhances the hole-trapping capability. Since the ZrHfO film and its interfaces lack the charge trapping capability, the embedded nc-ITO layers are responsible for the hole-trapping characteristics. On the other hand, C-V curves of the V_g = +8 V stressed nc-ITO embedded samples are almost the same as that of the fresh sample indicating the lack of electron-trapping capability. This is probably related to the ITO's unique electrical properties, e.g., it is a highly-degenerated n-type semiconductor.[181] When the capacitor is positively biased, the injected electrons may be trapped to the conduction band of the nc-ITO, which has a high potential energy.[72] They may be easily released back to the Si wafer when the gate bias is released. The result of V_g bias stress test as shown in Fig. 65 is consistent with that of the C-V hysteresis measurement, i.e., the memory functions of

the nc-ITO embedded memory capacitor is mainly contributed by the hole-trapping mechanism. Currently, most reports on the nanocrystal-based nonvolatile memories are operated by the principle of electron-trapping and -detrapping phenomena. If the memory device can be also operated by the hole-trapping and -detrapping mechanism, the design and applications of memory products can be greatly broadened.

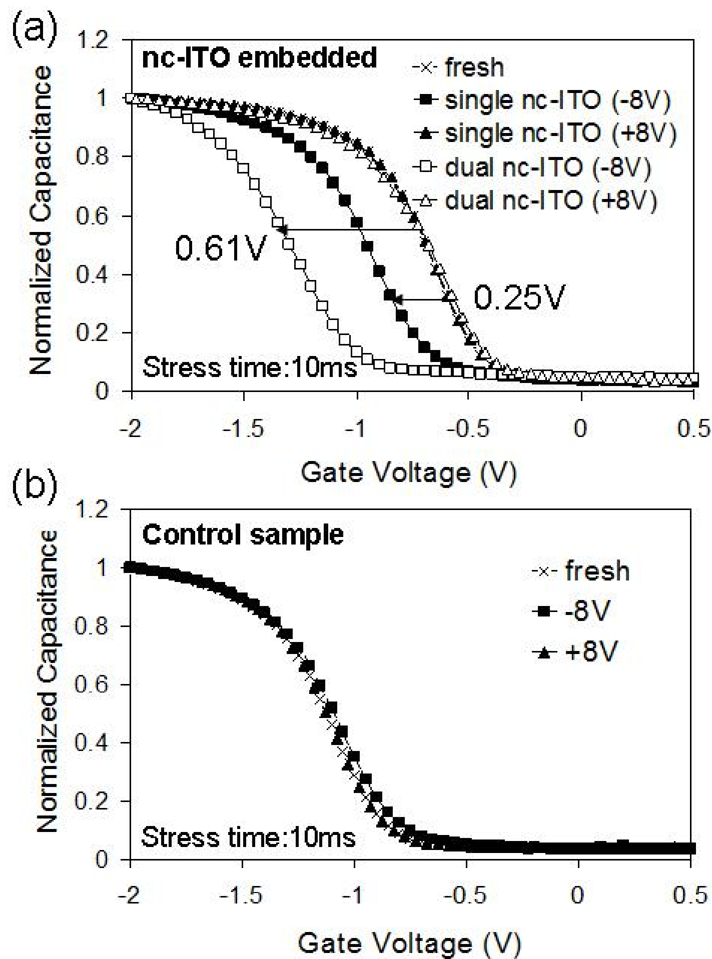


Figure 65. C-V curves (measured from -2 V to 1 V) of (a) single and dual nc-ITO and (b) control samples before (fresh) and after being stressed at V_g = -8 V and +8 V for 10 ms.

In addition, it has been observed that the fresh V_{FB} of the control sample is more negative than those of the nc-ITO embedded samples. This indicates that the nc-ITO embedded sample contains less positive charges, e.g., oxygen vacancies, than the control sample. Previously it was discussed that the nc-ITO embedded sample has a thicker IL layer than the control sample due to the enhanced oxygen diffusion through the high-k stack during the PDA process. The amount of oxygen vacancy in the gate stack is reduced due to the additional oxygen supply.[159] The ITO sputter process involves oxygen, which also favors the growth of the IL.

Dual-Layer Effects on Hole-Trapping Process

Since the hole-trapping mechanism is critical in the performance of the nc-ITO embedded ZrHfO device, it is imperative to study effects of magnitude of the stress V_g and the stress time on the hole-trapping efficiency. Figure 66(a) shows shifts of the V_{FB} of the single and dual nc-ITO samples (with respect to V_{FB} of the fresh device) after being stressed with various V_g's, e.g., V_g = -5 V to -9 V, for 10 ms. For both samples, the magnitude of the negative V_{FB} shift increases with the increase of the magnitude of the V_g. The increase is more pronounced for the dual nc-ITO sample than for the single nc-ITO sample, i.e., the former has a larger hole-trapping density and is more sensitive to the magnitude of bias V_g than the latter. On the other hand, Fig. 66(b) shows shifts of the V_{FB} with the stress time, i.e., from 0.1 ms to 1 s, of the single and dual nc-ITO embedded samples at the fixed V_g of -8 V. For the single nc-ITO embedded sample, the magnitude of the V_{FB} shift increases monotonically with the stress time, which is due to the charge leaking phenomenon.[162] The shift of V_{FB} of the dual nc-ITO embedded sample is much larger than that of the single nc-ITO embedded sample at the very short stress time, i.e.,

less than 10 ms. This means that under the large negative V_g stress condition, the programming efficiency can be greatly improved by adding the second nc-ITO layer to the high-k film.

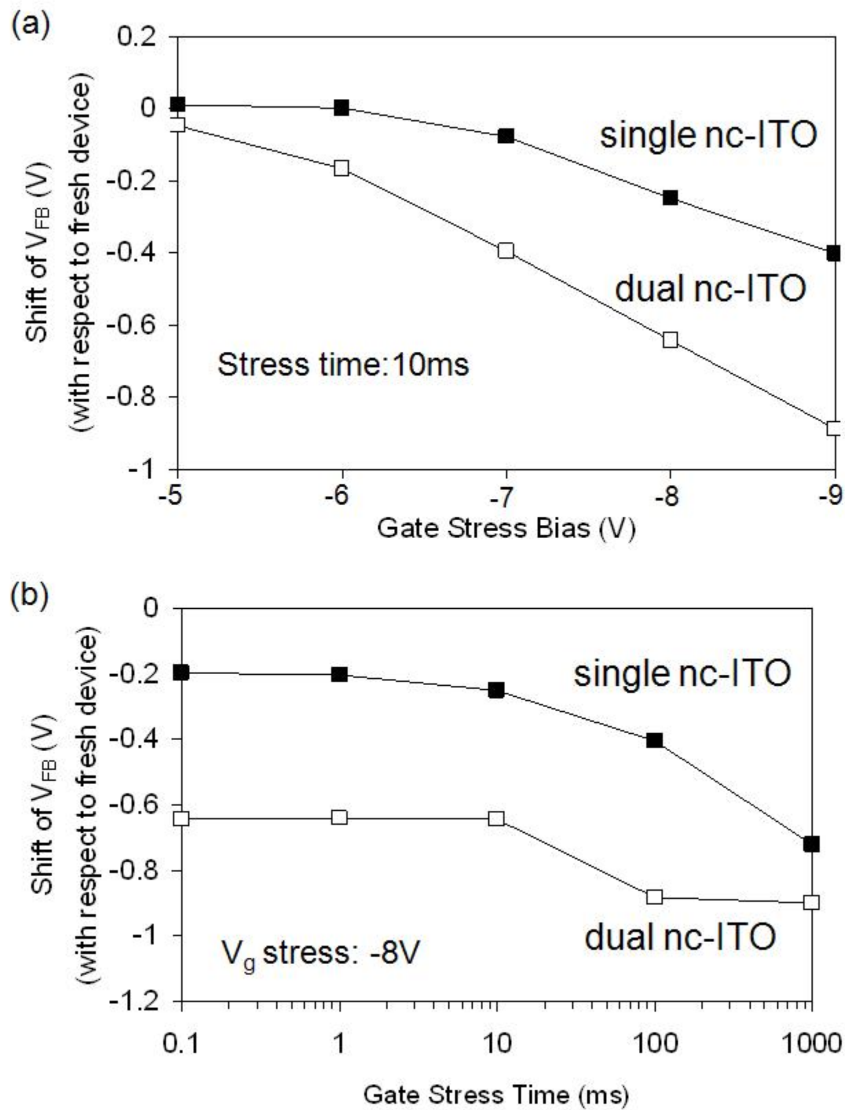


Figure 66. Shifts of V_{FB} of single and dual nc-ITO samples vs. (a) V_g stress at fixed stress time of 10 ms and (b) stress time at fixed V_g stress of -8 V.

The high hole-trapping density of the dual nc-ITO sample is contributed to the large density of nc-ITO dots. Moreover, the vertical separation of two embedded nc-ITO layers is beneficial to the retention of injected holes in the high-k stack. During the charge injection process, holes could tunnel through the whole dielectric layer if the magnitude of V_g is large enough. In the dual nc-ITO sample, holes are first trapped to the bottom nc-ITO site. Then, the rest holes can be trapped to the top ITO site. Holes trapped to the top nc-ITO sites could hinder other holes from passing by them to reach the top Al electrode due to the Coulomb block effect.[178] Therefore, the second nc-ITO layer not only increases the number of hole-trapping sites but also enhances the hole retention capability.

Investigation of Hole-Trapping Sites

Similar to the nc-RuO embedded capacitor discussed in Chapter IV, there are two possible charge trapping sites in the nc-ITO embedded sample, i.e., the bulk nc-ITO dot and nc-ITO/ZrHfO interface. Holes trapped at different sites may have different retention characteristics. It is important to investigate the charge trapping and detrapping characteristics of holes in the nc-ITO embedded sample. Figure 67 shows the frequency-dependent C-V and G-V curves measured at 100 kHz and 1 MHz of the (a) control and (b) single and dual nc-ITO embedded samples. The V_g was swept from -7 V to 3 V to investigate the hole-trapping characteristics. For the control sample, the peak location shifts slightly but the height remains the same with the change of the measure frequency. This may be contributed by the relatively small number of interface states at the high-k/Si contact region. The slightly flattening of the C-V curve at the low frequency also reflects this kind of defect.[2]

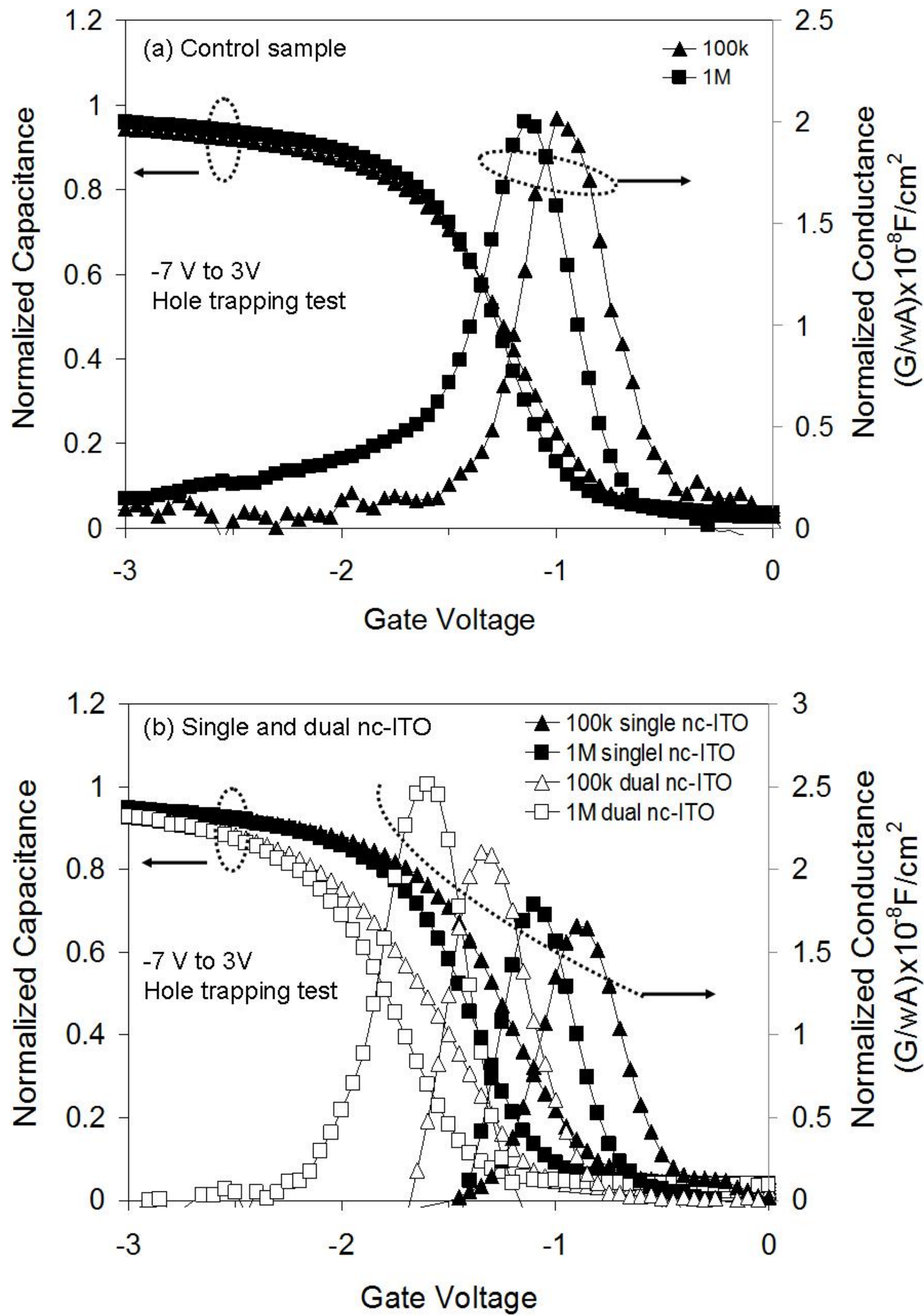


Figure 67. Frequency-dependency on normalized C-V and G-V curves of (a) control and (b) single and dual nc-ITO samples. V_g was swept from -7 V to 3 V for hole-trapping investigation.

However, for the nc-ITO embedded samples, the dispersions of C-V and G-V curves are pronounced. Compared with the high frequency C-V and G-V curves, the low frequency C-V curve shifts more positive and appears to respond to the V_g sweep slower, i.e., flattened off. The G-V curve also shifts to the positive V_g direction with a lower height. The frequency-dependent phenomena indicate that some holes may be loosely trapped at the nc-ITO/ZrHfO interfaces.[182] These holes are physically close to the high-k/Si interface. They may respond to the low measure frequency slowly and are easy to tunnel back to the Si substrate.[125] Therefore, during the V_g sweep, the detrap of the loosely-trapped holes may occur when the energy band structure reaches the flatband condition. This is why under the low measure frequency, the C-V curve is flattened off and shifts positively when the V_g is swept to around V_{FB}. The frequency-dependent phenomena are more obvious in the dual nc-ITO sample than those in the single nc-ITO sample because the former has more nc-ITO dots and therefore, nc-ITO/ZrHfO interface areas.

Dual-Layer Effects on Hole-Detrapping Properties Related to J-V and Retention

In order to further investigate the hole-detrapping phenomena in the nc-ITO embedded samples, the J-V measurements were carried out, as shown in Fig. 68. The V_g was swept from -6 V to +6 V so that holes can be trapped in the negative V_g range and be detrapped in the positive V_g range. There are obvious current jumps in both J-V curves. The jump A is mainly contributed by the release of the trapped holes at the nc-ITO/ZrHfO interface when the V_g was moved from the large value to near V_{FB}. At the jump A point, the J is increased from 3.7×10^{-8} A/cm^2 to 4.7×10^{-8} A/cm^2 for the dual nc-ITO sample and from 2.1×10^{-8} A/cm^2 to 2.5×10^{-8} A/cm^2 for the single nc-ITO sample.

The larger jump in the former is related to the larger number of the originally trapped holes. The jump B occurs near $V_g = 0$ V. It is due to the change of the V_g polarity. The dual nc-ITO sample has another large jump at C, which is not obvious in the single nc-ITO sample. This is because holes trapped at the top nc-ITO layer require a higher positive V_g to push them out.

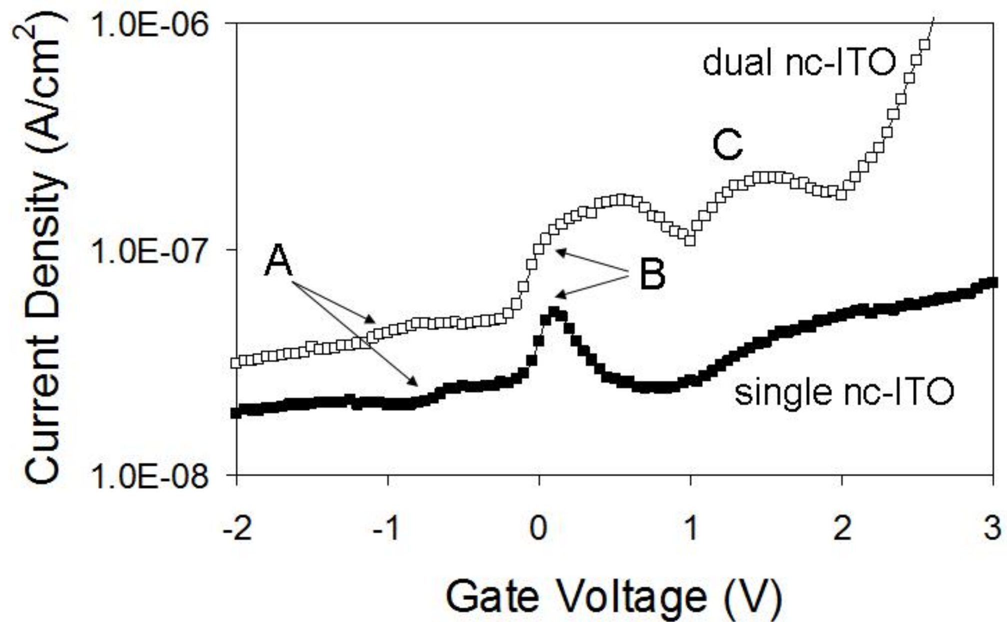


Figure 68. J-V curves (measured from -6 V to +6 V) of single and dual nc-ITO samples. Three kinds of current jumps are also denoted.

Figure 69 shows the charge retention properties of the single and dual nc-ITO embedded samples after being stressed at V_g = -8 V for 1 s. Since the dual nc-ITO sample can trap a larger amount of holes than the single nc-ITO does after the same gate stress condition, the charge remaining should be calculated from the following equation to better represent the charge retention properties, i.e.,

$$\text{Charge remaining (\%)} = \frac{V_{FB}(t) - V_{FB}(fresh)}{V_{FB}(stress) - V_{FB}(fresh)} \qquad [15]$$

where V_{FB}(stress) is the device's V_{FB} after the V_g stress, V_{FB}(fresh) is the V_{FB} of the fresh device, i.e., before the stress, and V_{FB}(t) is the device's V_{FB} after releasing the stress V_g for time t. The V_{FB}'s were determined from the C-V curves measured over a very small V_g range of -2 V to 1V, which traps a negligible amount of charges. The two retention curves in Fig. 69 show similar trend. For the first 100 s, both samples lose charges drastically, e.g., 40 % for the single nc-ITO sample and 25 % for the dual nc-ITO sample. Then, the charge loss rates reduce slowly, e.g., 4 % from 100 s to 10,000 s for both samples. For the single nc-ITO embedded sample, the first big drop is due to the detrap of the loosely-trapped holes from the nc-ITO/ZrHfO site to the Si wafer immediately after the release of the stress V_g. Then, the strongly-trapped holes in the bulk nc-ITO sites are gradually released. Eventually, a large portion of the originally trapped holes, i.e., >50 %, are retained in the device after 10,000 s. The dual nc-ITO sample has a much larger charge retaining capability than the single nc-ITO sample because the Coulomb blockade effect of the bottom nc-ITO layer hinders the hole leakage from the top ITO layer to the Si wafer. The inset in Fig. 69 shows that about 40 % and 55 % of trapped holes still remain in the single and dual nc-ITO sample, respectively, after releasing the stress V_g for 10 years. This is a desirable characteristic for the nonvolatile memory.

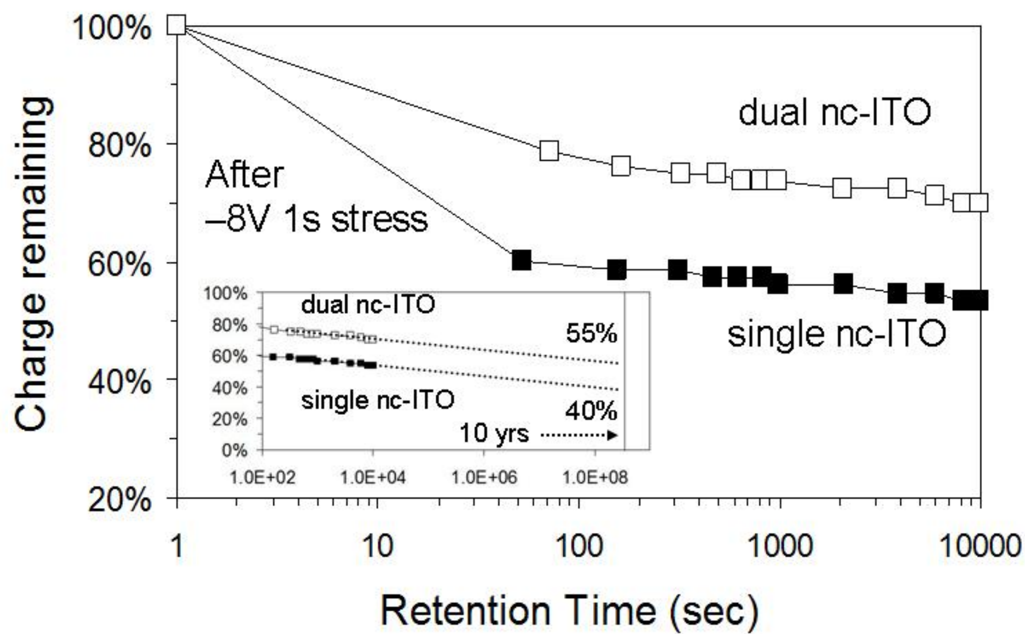


Figure 69. Retention properties of holes trapped in single and dual nc-ITO samples. Holes were injected into the device by a V_g stress of -8 V for 1 s. Inset shows the curve extrapolation to ten years projection.

5.4 Material and Electrical Properties of Single and Dual nc-ZnO Embedded ZrHfO High-K Gate Dielectric Stacks

5.4.1 Physical and Chemical Properties of Single and Dual nc-ZnO Embedded ZrHfO Bulk High-K Films and Interface Layers

Figure 70(a) shows the top-view TEM micrograph of the single-layer nc-ZnO embedded ZrHfO film. The grain size of nanodots is 3 nm to 8 nm, and the 2-D spatial density is about 1.43×10^{12} cm^{-2}. The nanodots are crystalline ZnO with (100) orientation[183] detected by XRD, as shown in Fig. 70(b). The absence of crystalline ZrHfO peaks in the XRD pattern confirms that the ZrHfO part is amorphous, which is consistent with the result of the nc-ITO embedded ZrHfO film. Therefore, the amorphous structure of the ZrHfO film did not change with embedding nc-ZnO. Figure 71(a) and (b) show the cross-sectional TEM micrographs of the single- and dual-layer ZnO embedded ZrHfO gate stacks without the top Al gate layer, respectively. In the single-layer embedded sample, discrete nanodots, as highlighted in circles, are dispersed in the amorphous ZrHfO matrix. In the dual-layer embedded sample, two layers of discrete nanodots are observed. They are vertically separated, which is similar to the dual-layer nc-ITO structure. The total thickness of the complete high-k stack increases with the inclusion of the nc-ZnO film, i.e., from 5.4 nm (control sample) to 6 nm (single nc-ZnO sample) and 6.6 nm (dual nc-ZnO sample). Also, the amorphous $HfSiO_x$ IL's with thickness 3.7 nm were formed in both single- and dual-layer embedded samples between ZrHfO and Si. Again, $HfSiO_x$ has relatively low band alignments with respect to Si compared with those of SiO_2, which favors the programming process.

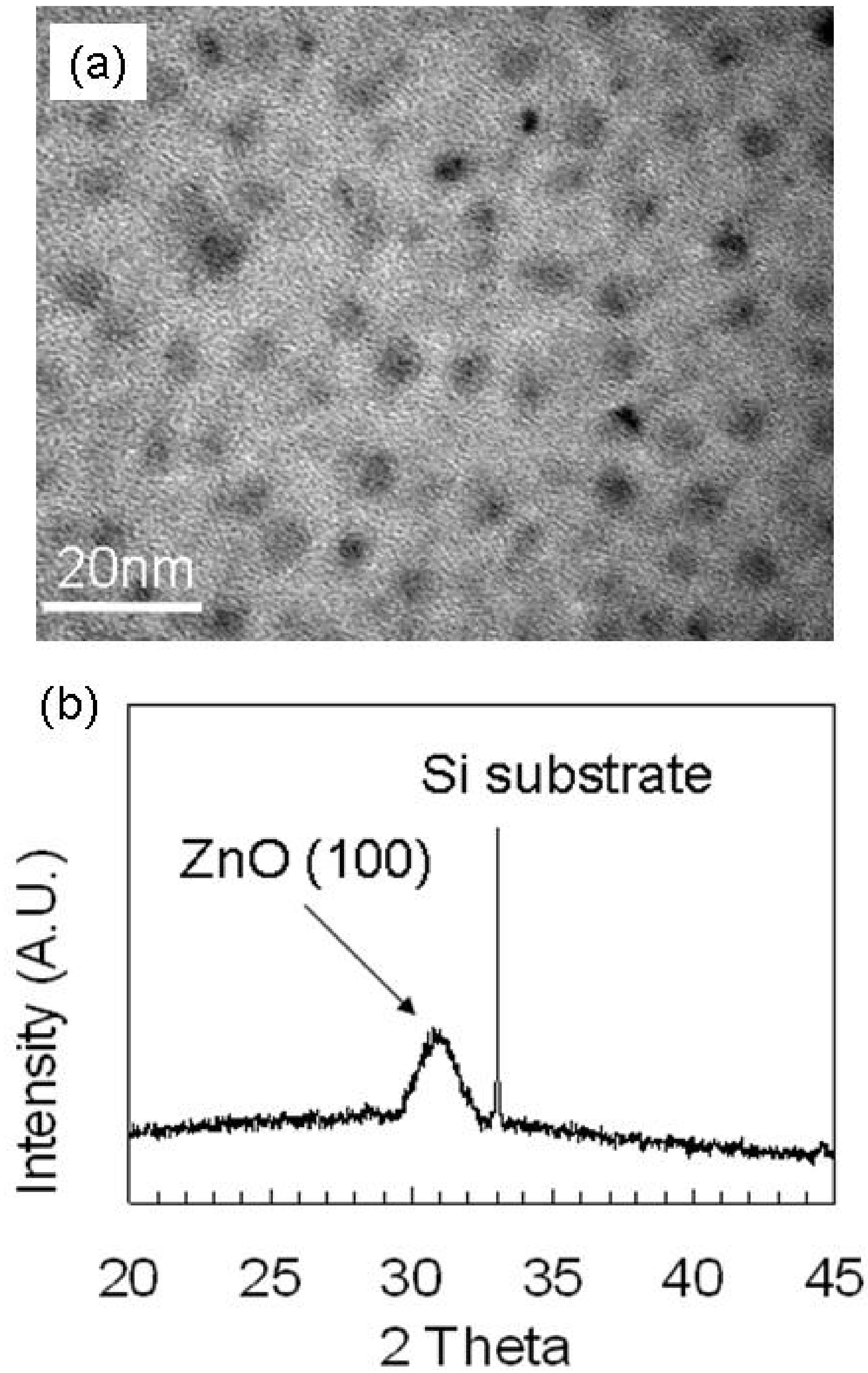


Figure 70. (a) Top-view TEM micrograph and (b) XRD pattern of single- and dual-layer nc-ZnO embedded ZrHfO films, respectively.

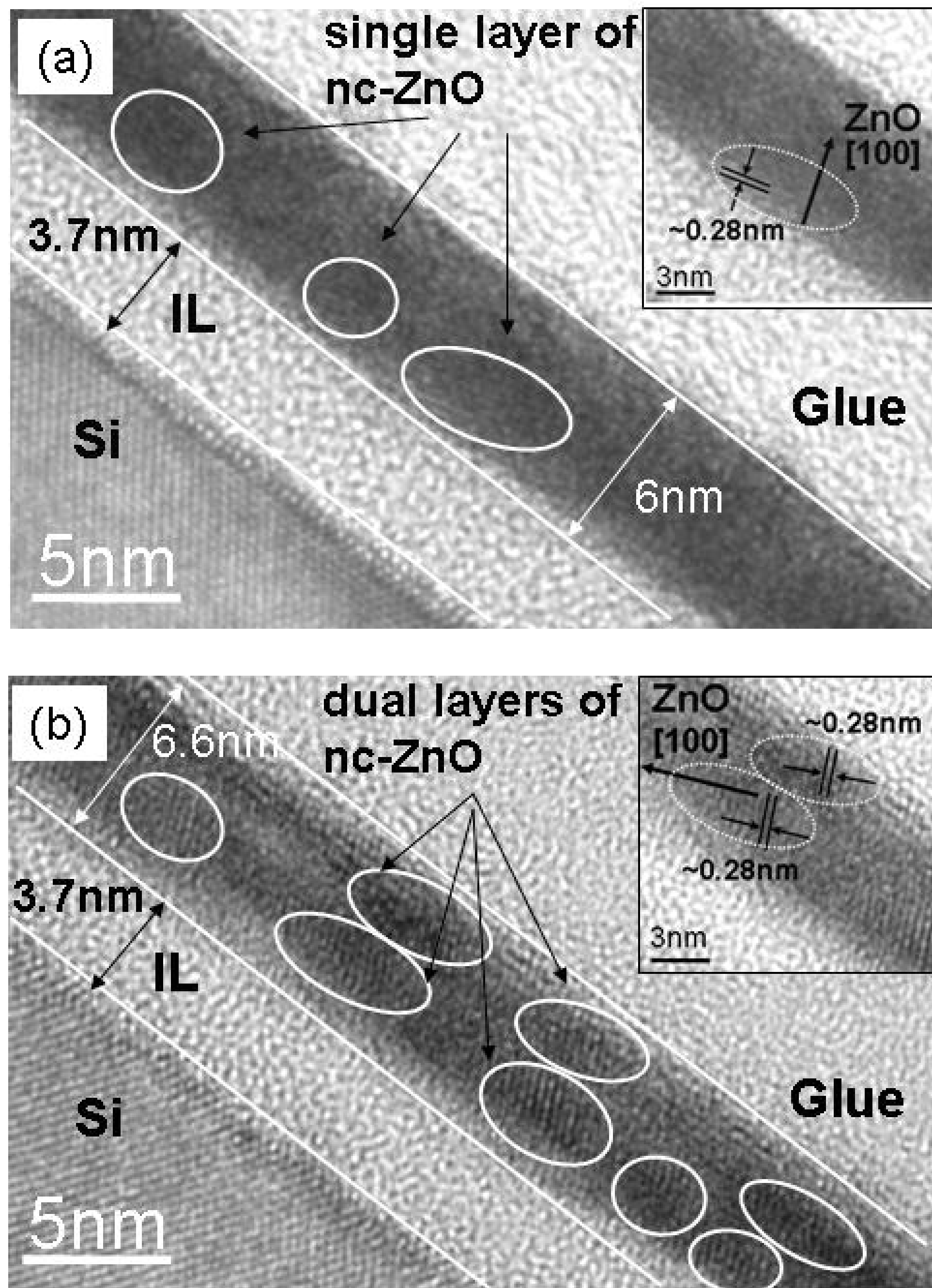


Figure 71. Cross-sectional TEM micrographs of (a) single-layer nc-ZnO and (b) dual-layer nc-ZnO embedded ZrHfO gate stacks on Si.

In contrast to the nc-ITO embedded samples that show a significant IL growth with the inclusion of the nc-ITO after PDA, the IL thickness only slight increased with the nc-ZnO embedded in the high-k stack, i.e., from 3.4 nm (control sample) to 3.7 nm (both single and dual nc-ZnO samples). This difference may be attributed to the different oxygen diffusion phenomena in these two nanocrystals-embedded high-k stacks. The detailed causes will be discussed later in this chapter. The insets of Fig. 71(a) and (b) show that the periodic lattice fringes of nanodots in both single- and dual-layer embedded samples have spacing about 0.28 nm, which corresponds to the ZnO (100) layer.[183]

Figure 72(a) shows the XPS Hf 4*f* spectra of the (a) control, (b) single, and (c) dual nc-ZnO embedded samples. All figures contain the Hf $4f_{7/2}$ peak with a binding energy (BE) of 17.2 eV, which is contributed by two components, i.e., bulk ZrHfO film (BE = 16.8 eV) and $HfSiO_x$-like interface at the Si wafer contact region (BE = 17.6 eV).[154] However, in contrast to the nc-ITO embedded results, the intensity difference between the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ peaks in the nc-ZnO embedded samples is independent on the inclusion of nc-ZnO layer in the high-k stack. In addition, Fig. 72(b) shows that the intensity difference between the Zr $3d_{5/2}$ and Zr $3d_{3/2}$ peaks is also independent on the embedded nc-ZnO layers. These results imply that not only the formation of the interface layer (at nc-ZnO/ZrHfO contact region) is not obvious, but also the embedded nc-ZnO layers do not change the chemical bonding structures of Hf and Zr elements in the bulk high-k film or in the IL. Figure 72(c) shows the Zn 2*p* XPS spectra of the single and dual nc-ZnO embedded samples. The peak at BE = 1020.9 eV corresponds to the ZnO structure.[184] The height and size of the Zn 2*p* peak are much higher in the dual nc-ZnO sample than those in the single nc-ZnO sample because the former contains more Zn

atoms in the stack. Figure 72(d) shows that the Si 2*p* XPS spectra were hardly detected, and its intensity slight decreased in the order of the dual nc-ZnO, the single nc-ZnO and the control samples due to the slight change of the high-k stack layer thickness.

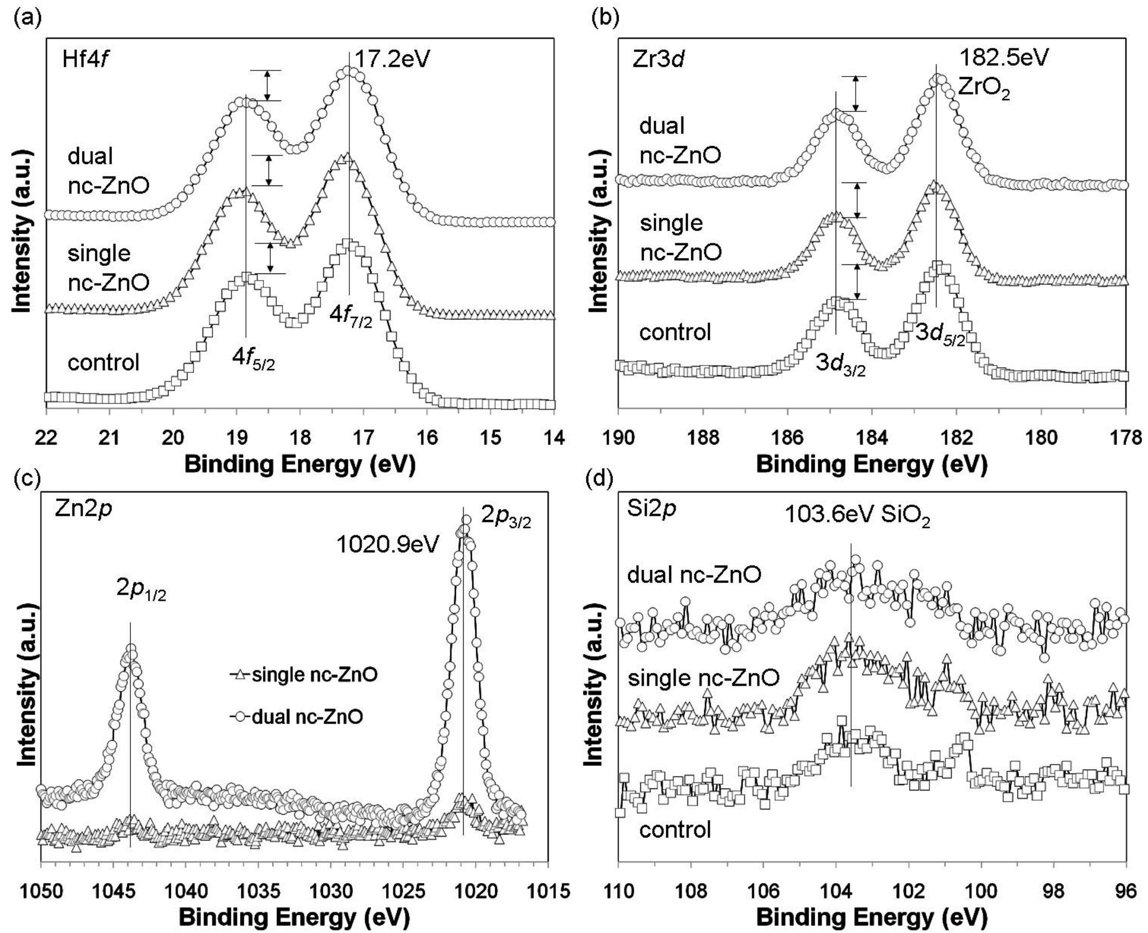


Figure 72. (a) Hf 4*f*, (b) Zr 3*d*, (c) Zn 2*p*, and (d) Si 2*p* XPS spectra of control, single and dual nc-ZnO samples.

5.4.2 Electrical Properties of Single and Dual nc-ZnO Embedded ZrHfO High-K MOS Capacitors

Differentiation of Hole and Electron Trapping

Figure 73 shows C-V curves of (a) single and (b) dual nc-ZnO samples before (fresh) and after being stressed for 10 ms with a constant V_g of -8 V or +8 V. The C-V curves were measured at 1MHz over a small voltage range, i.e., -2 V to 1 V. The -8 V stress condition induced a hole-rich accumulation layer and the +8 V stress condition induced an electron-rich inversion layer near the Si/high-k interface. Again, the control sample has negligible C-V shift under either +8 V or -8 V stress condition, as shown in the inset of Fig. 73(a). Figure 73(a) and (b) show that after +8 V stress, the C-V curve shift to the positive direction in both single and dual nc-ZnO samples, i.e., ΔV_{FB} = 0.43 V and 0.98 V, separately, which corresponds to electron-trapping densities (Q's) of 1.34×10^{12} cm^{-2} and 3.06×10^{12} cm^{-2}, separately. The latter is comparable to that of the dual-layer nc-Si embedded SiO_2 capacitor.[185] Judged from the Q of the single nc-ZnO sample and nc-ZnO density, in average, each nc-ZnO dot stores about one electron, which is in the same order of magnitude as that of nc-Si in SiO_2.[186-187] The increase of the electron-trapping density from the addition of the second nc-ZnO embedded layer is consistent with the increase of the number of the nc-ZnO dots in the dielectric structure. Therefore, the electron-trapping effect is critical to the memory functions of the nc-ZnO embedded ZrHfO capacitors. Figure 73(a) also shows that after -8 V stress, the C-V curve of the single nc-ZnO sample shifts slightly to the negative direction, i.e., ΔV_{FB} = -0.15 V, which indicates the trap of a small amount of holes. It is not contributed by the ZrHfO part of the film, as shown in the inset of Fig. 73(a). The low hole-trapping capability is

probably related to nc-ZnO properties. Defects, such as Zn_i and V_o, in nc-ZnO are sub-conduction band trapping centers for electrons instead of holes.[175-177] Therefore, only a small portion of the injected holes were retained at the nc-ZnO site. For the dual nc-ZnO sample, the negative shift of the C-V curve after -8 V stress is negligible, as shown in Fig. 73(b). Since the dual nc-ZnO sample has a thinner top control dielectric layer than the single nc-ZnO sample, as shown in Fig. 71 (a) and (b), it may be easier to inject electrons from the Al electrode to the dielectric film or to detrap holes from the nc-ZnO sites to the Al electrode under the strong gate bias condition. However, more studies are required to verify the exact mechanism.

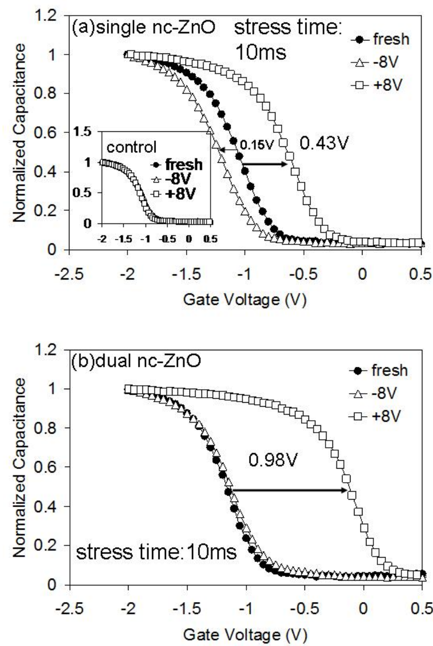


Figure 73. C-V curves (measured from -2 V to 1 V) of (a) control (inset) and single nc-ZnO and (b) dual nc-ZnO samples before (fresh) and after being stressed at V_g = -8 V and +8 V for 10 ms.

Dual-Layer Effects on Memory Functions Contributed by Electron Trapping

Figure 74 shows C-V hysteresis curves (measured at 1 MHz) of (a) single and (b) dual nc-ZnO samples swept from the fixed negative V_g = -2 V to positive V_g (forward) then back to -2 V (backward). In order to investigate the electron-trapping effect dependent on the positive gate bias, the forward sweep starting V_g is fixed at a small magnitude (-2 V) while the backward sweep starting V_g is varied from +4 V to +8 V. Figure 74(c) also shows a small memory window in the C-V hysteresis curve of the control sample swept from -2 V to +8 V to -2 V, i.e., 0.1 V, which further confirms the poor charge trapping capability of the amorphous ZrHfO film. However, under the same sweep condition, the memory window was increased to 0.47 V for the single nc-ZnO sample and to 0.98 V for the dual nc-ZnO sample. The electron-trapping densities (Q's) of 1.47×10^{12} cm^{-2} and 3.06×10^{12} cm^{-2} were obtained for the single and dual nc-ZnO samples, separately. This is consistent with the Fig. 73 result that the dual nc-ZnO sample traps much more electrons than the single nc-ZnO sample does under the +8 V stress condition. Separately, it was observed that the memory window was enlarged with the increase of the forward direction V_g, as summarized in Fig. 74(d). For example, for the dual nc-ZnO sample, the memory window was increased from 0.12 V to 0.42 V and 0.98 V when the end of the forward V_g was increased from +4 V to +6 V and +8 V, separately. Under the same V_g sweep condition, for the single nc-ZnO sample, the corresponding memory windows were 0.12 V, 0.3 V, and 0.47 V, separately. The magnitude of the memory window difference between the dual and single nc-ZnO samples increases with the increase of the gate sweep voltage. The high positive V_g enhances the formation of an electron-rich interface layer and promotes electron injection into the dielectric layer.

Figure 74 demonstrates that there are two major factors affecting the electron-trapping capability of the nc-ZnO embedded device: (1) the supply of energetic electrons from the substrate, and (2) the density of the embedded nc-ZnO dots in the dielectric layer.

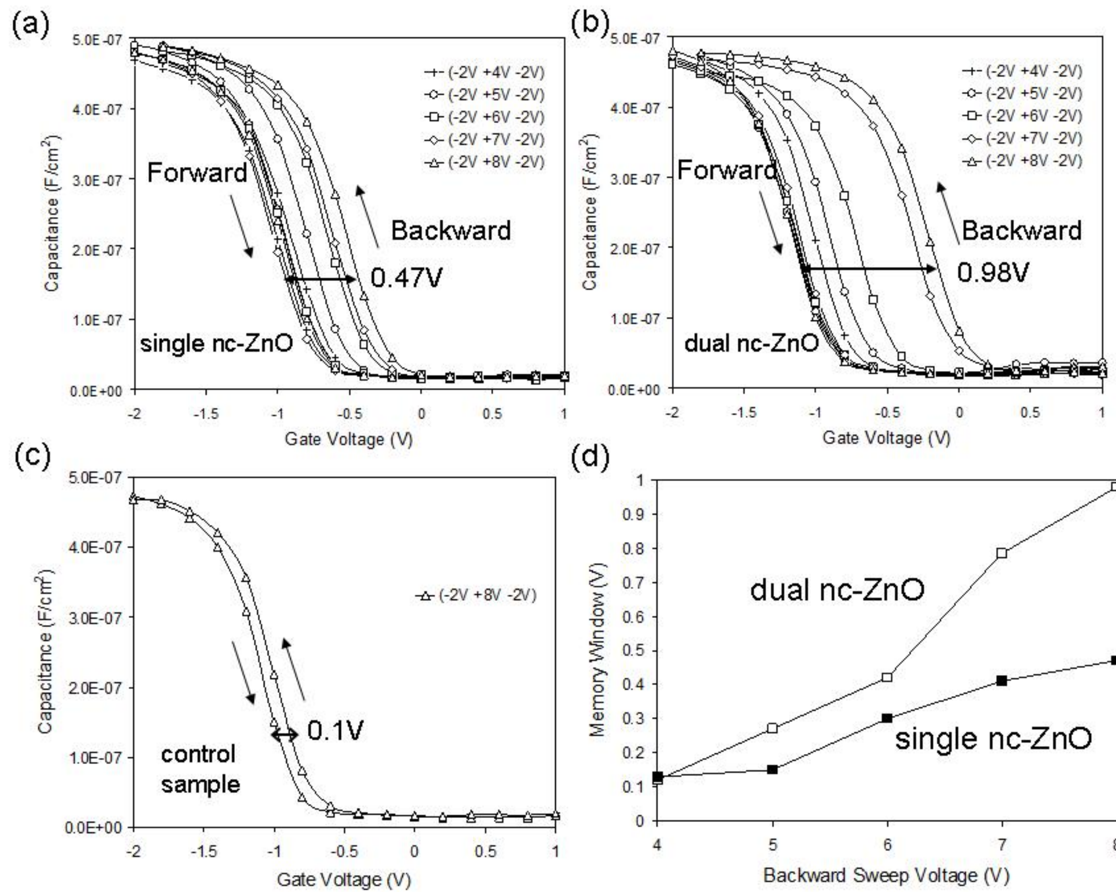


Figure 74. C-V hysteresis curves of (a) single nc-ZnO and (b) dual nc-ZnO samples swept from fixed negative V_g = -2 V to positive V_g (forward) then back to -2 V (backward). Backward sweep starting V_g is varied from +4 V to +8 V. (c) C-V curve of control sample swept from -2 V to +8 V to -2 V. (d) Comparison of memory windows summarized from C-V curves in (a) and (b).

Dual-Layer Effects on Electron-Trapping Process

Since the electron-trapping effect is critical to the memory function of the nc-ITO embedded ZrHfO device, it is important to study the electron-trapping process as a function of magnitude of the stress V_g and the stress time. Figure 75(a) shows shifts of the V_{FB} (ΔV_{FB}) of the single and dual nc-ZnO samples (with respect to V_{FB} of the fresh device) after being stressed with various V_g's, e.g., V_g = +5 V to +9 V, for 10 ms. For both samples, the magnitude of the positive ΔV_{FB} increases with the increase of the magnitude of V_g. In addition, for the dual nc-ZnO sample, the ΔV_{FB} is consistently larger than that of the single nc-ZnO sample. Therefore, the former has a larger electron-trapping density and is more sensitive to the magnitude of V_g than the latter. It is also noted that under the V_g = +5 V stress, the single nc-ZnO sample traps negligible amount of electrons while the dual nc-ZnO sample shows a significant electron-trapping effect, i.e., ΔV_{FB} = 0.41 V. This is because under such short stress time of 10 ms, the injected electrons may have a larger opportunity to be trapped in the dual-layer nc-ZnO embedded dielectric stack than in the single-layer embedded counterpart due to the former's higher trapping site density and unique vertically-separated dual-layer structure.

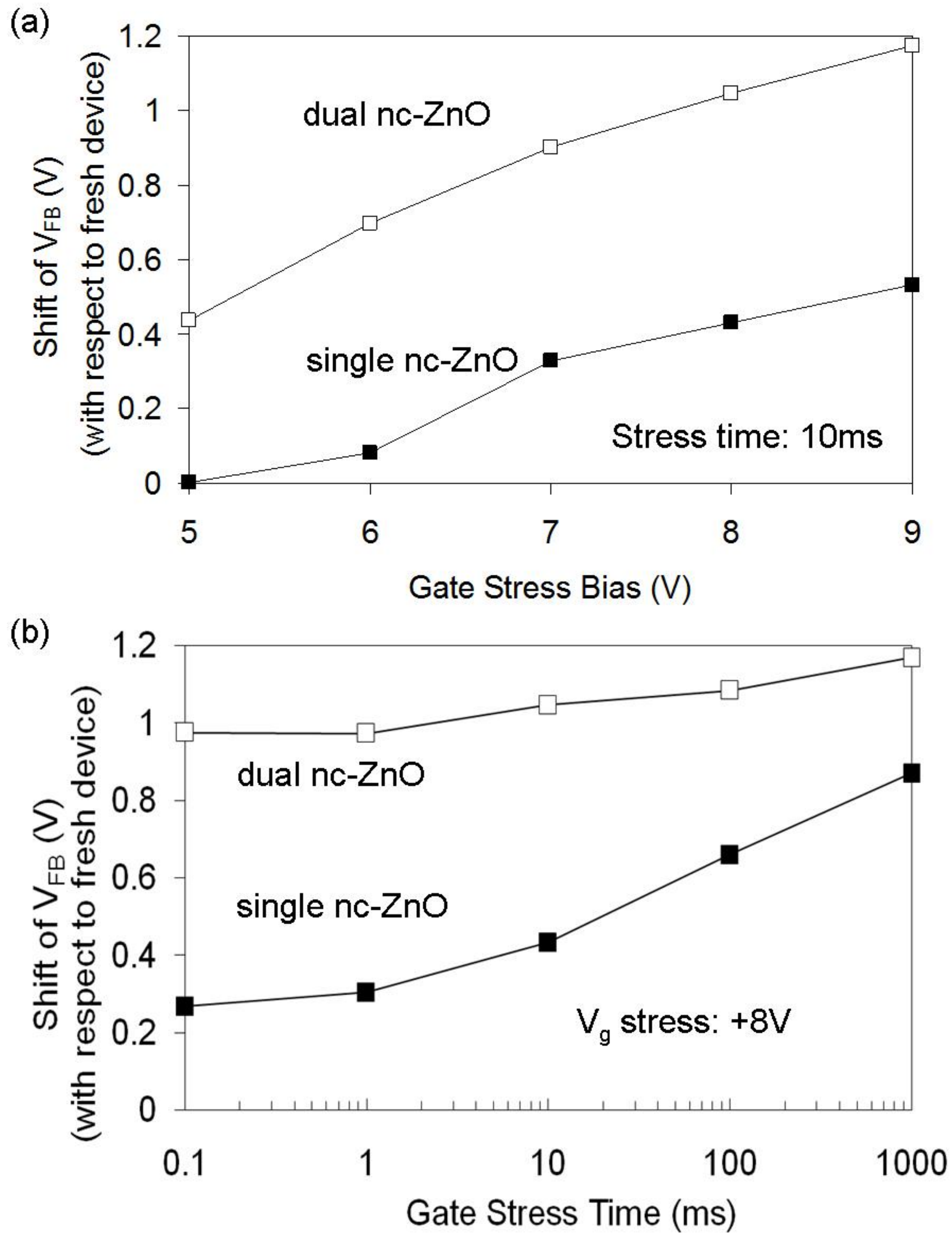


Figure 75. Shifts of V_{FB} (ΔV_{FB}) of single and dual nc-ZnO samples vs. (a) V_g stress at fixed stress time of 10 ms and (b) stress time at fixed V_g stress of +8 V.

On the other hand, Fig. 75(b) shows the ΔV_{FB} of the nc-ZnO embedded samples after V_g = +8 V bias as a function of the stress time. For the single nc-ZnO sample, the magnitude of ΔV_{FB} increases monotonically with the stress time, which is similar to the single nc-ITO sample and other nonvolatile memory devices, e.g., nc-tungsten embedded in HfAlO and nc-ruthenium oxide embedded in ZrHfO.[188-189] Again, this kind of relationship implies that some of the trapped charges probably were lost to the gate electrode during gate stress.[162] In addition, electrons injected from the substrate may not be completely retained by the nc-ZnO dots in the single nc-ZnO sample. In the dual nc-ZnO sample, the loss of electrons from the bottom nc-ZnO layer during gate stress could be reduced because they have to overcome the Coulomb blockade effect generated from electrons trapped to the top nc-ZnO layer before reaching the gate electrode.[190] Since the ΔV_{FB} of the dual nc-ZnO sample is much larger than that of the single nc-ZnO sample within a very short stress time, e.g., $<$ 10 ms, the data programming speed is greatly improved with the addition of the extra nc-ZnO layer. In addition, the ΔV_{FB} of the dual nc-ZnO sample is less dependent on the stress time than the single nc-ZnO sample is. This is probably due to limited supply of electrons from the substrate or saturation of the nc-ZnO charge trapping site within a short period of stress time.

Investigation of Electron-Trapping Sites

Similar to the nc-ITO embedded capacitors, there should be two possibly physical charge trapping sites in the nc-ZnO embedded sample, i.e., the bulk nc-ZnO site and nc-ZnO/ZrHfO interface. However, judged from the XPS results shown in Fig. 72, the interface layer formation at the nc-ZnO/ZrHfO contact region is not obvious. The injected electrons may not be trapped at this interface. Whereas, the detection limit of XPS analysis only reaches about 0.1 %, which is not sensitive enough to rule out the possibility that electrons indeed are trapped at the nc-ZnO/ZrHfO interface. In order to clarify the electron-trapping sites in the nc-ZnO embedded sample, the frequency-dependent C-V and G-V curves measured at 100 kHz and 1 MHz were carried out. The V_g was swept from 7 V or 8 V to -2 V or -3 V for investigating the electron-trapping characteristics. Figure 76 shows the corresponding results of the (a) control and (b) nc-ZnO embedded samples. Similar to the control sample swept from -7 V to 3 V (shown in Fig. 67(a)) that shows negligible dispersion, the control sample measured with sweep V_g from 7 V to -3 V also shows non-dispersion phenomenon, as shown in Fig. 76(a). This can be attributed to the poor charge trapping capability of the control sample. However, Fig. 76(b) shows that the C-V curve did not flatten off, and the peak and location of the G-V curve also did not shift when the measure frequency was decreased. Therefore, the trapped electrons do not respond to the low measure frequency. It is very likely that most electrons are deeply trapped in the bulk nc-ZnO sites.

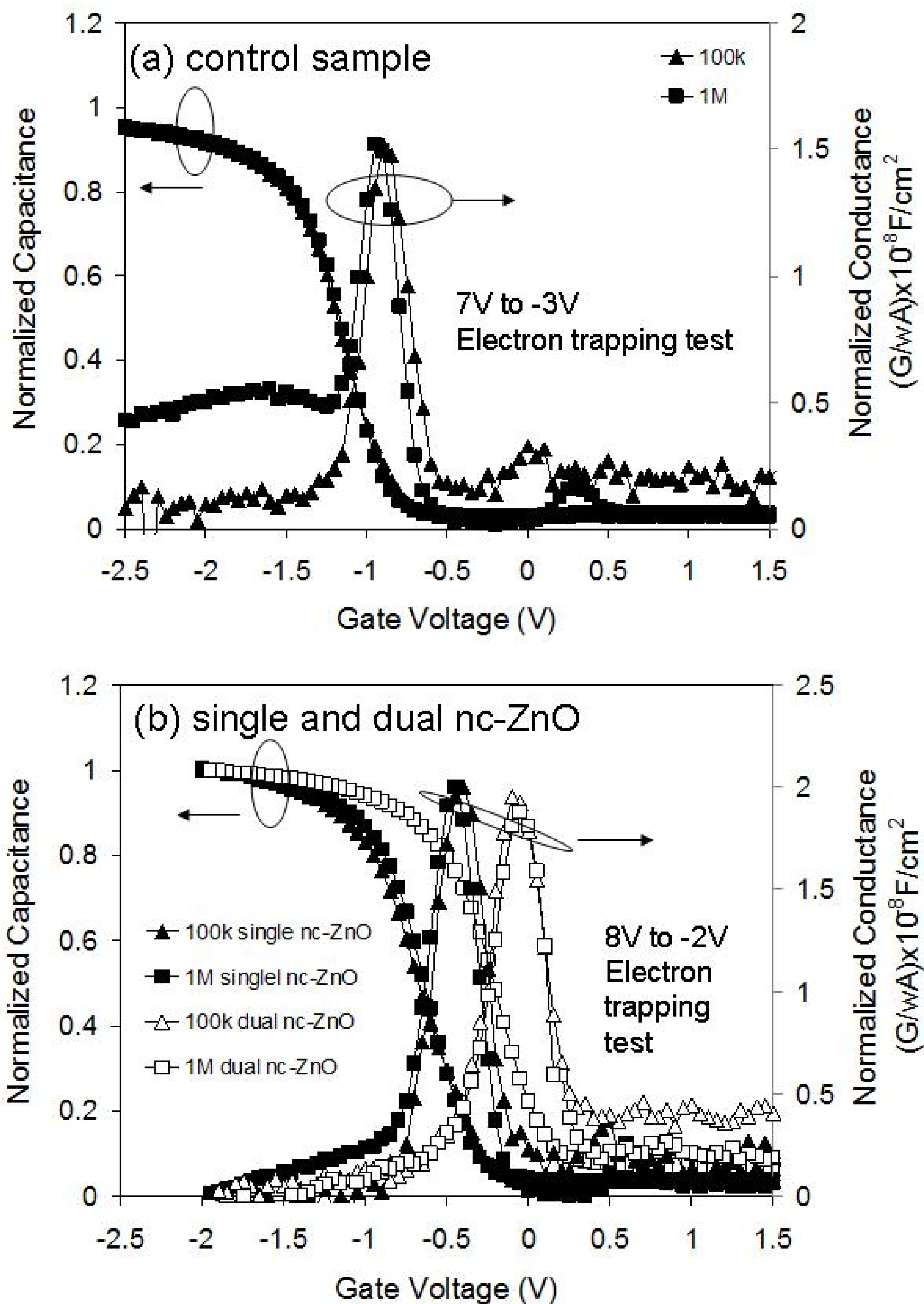


Figure 76. Frequency-dependency on normalized C-V and G-V curves of (a) control and (b) single and dual nc-ZnO samples. V_g was swept from positive to negative for electron-trapping investigation.

Dual-Layer and Trapping Site Effects on Electron-Detrapping Properties Related to J-V and Retention

Figure 77 shows the J-V curves of the single and dual nc-ZnO samples measured from +6 V to -6 V to investigate the electron-detrapping process with respect to the V_g. The V_g was swept from +6 V to -6 V so that electrons can be trapped in the positive V_g range. Figure 77 shows that the polarity of J changed from positive to negative when the V_g reached around 3 V. This is because, during the V_g sweep range of 6 V to 3 V, the injected electrons can be trapped into the high-k stack. Then, the trapped electrons can inhibit the subsequently-injected electrons from passing through the high-k stack to reach the gate electrode when the V_g is < 3 V. The negative J is probably contributed by the detrapping of electrons that are not strongly held by the bulk nc-ZnO dots. Even though the Fig. 76 results indicate that most trapped electrons are deeply trapped in the bulk nc-ZnO sites, some of them may not be strongly held. The dual nc-ZnO sample shows a slight higher negative J than the single nc-ZnO sample since the former contains a higher density of nc-ZnO in the bottom embedded nc-ZnO layer. Therefore, the dual nc-ZnO sample may also contain a higher density of the trapped electrons that are not strongly held by the bulk nc-ZnO dots. Recall that the loosely-tapped charges, which are located at the interface between the nanocrystal and surrounding dielectric film, can be suddenly detrapped when the V_g is swept to near V_{FB}, and significantly detrapped when the V_g is released. These kinds of charge detrapping phenomena can cause obvious current jumps in the J-V curve, as discussed in the nc-RuO and nc-ITO embedded capacitors. The J-V curves shown in Fig. 77 did not contain current jumps, instead, J dropped to near zero when the V_g reached 0 V. This phenomenon implies that the amount of the loosely-

trapped electrons in the nc-ZnO embedded capacitor may be small, and they are already thoroughly detrapped before the V_g reaches to the negative region. This kind of unique J-V characteristics confirms the lack of the interface formation at the nc-ZnO/ZrHfO contact region in both single and dual nc-ZnO samples.

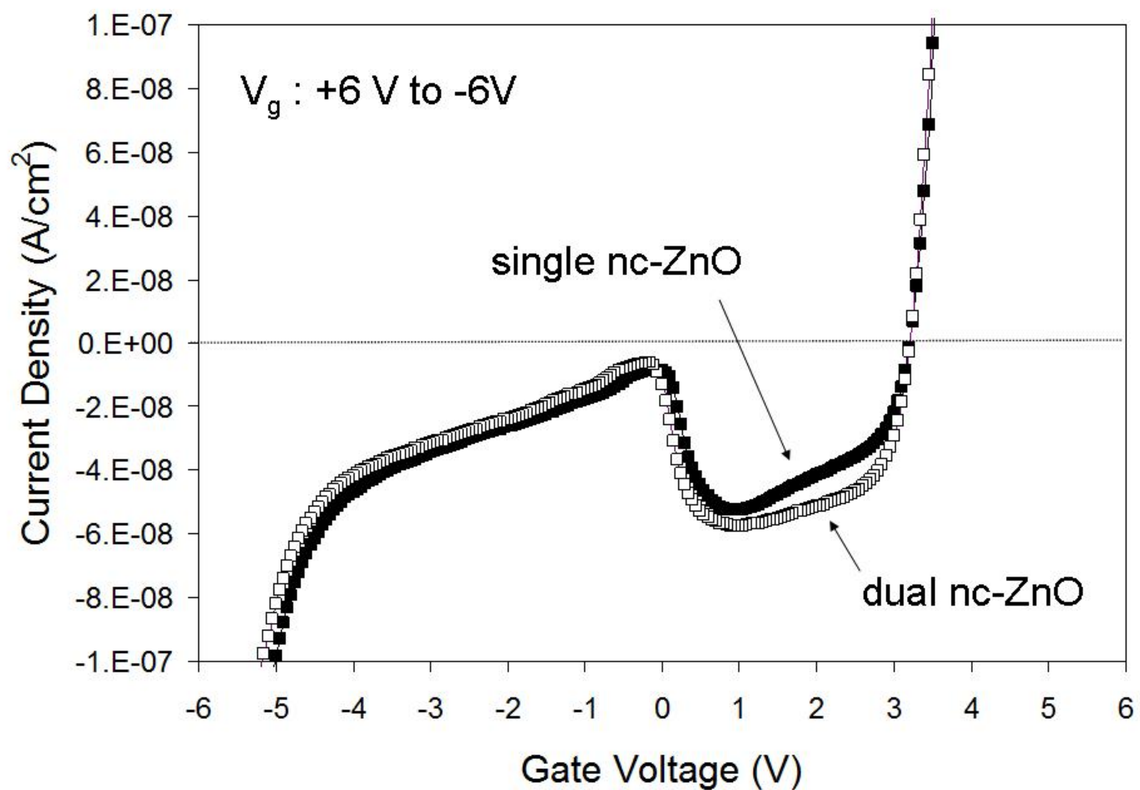


Figure 77. J-V curves (measured from +6 V to -6 V) of single and dual nc-ZnO samples.

Figure 78 shows the electron retention properties of the single and dual nc-ZnO embedded samples after being stressed at V_g = +8 V for 1 s. In contrast to the retention property of the nc-ITO embedded capacitor, no quick charge loss phenomenon which occurred in the short-term retention stage was observed in the nc-ZnO embedded samples. This further confirms the lack of loosely-trapped charges in the capacitor. Compared with the single nc-ZnO sample, the dual nc-ZnO sample shows a better retention property benefited from its dual-layer structure, i.e., a larger 10-years charge remaining of 29 % vs. 10 %.

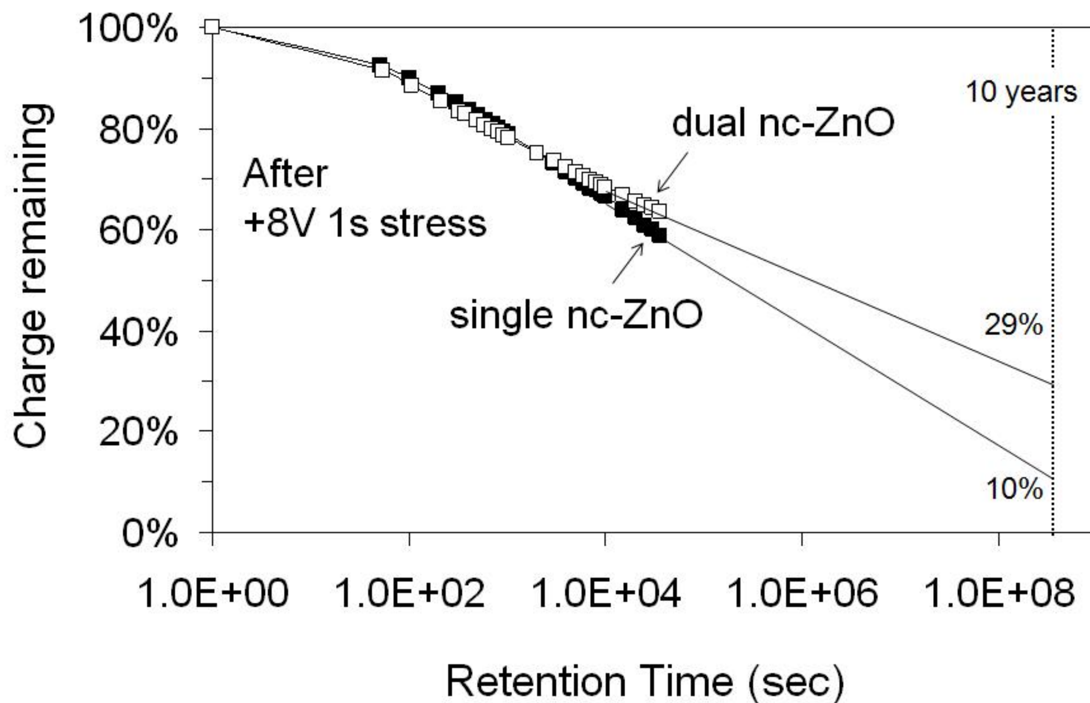


Figure 78. Retention properties of electrons trapped in single and dual nc-ZnO samples. Electrons were injected into the device by a V_g stress of +8 V for 1 s.

5.5. Comparisons among Nanocrystalline Conductive Oxides Embedded ZrHfO High-K Gate Dielectric Stacks: nc-RuO, nc-ITO, nc-ZnO

5.5.1 Correlation between Electrical Property and Interface Layer at Nanocrystals/ZrHfO

The material properties of the interface layer formed at the nanocrystal/ZrHfO contact region can be investigated by the XPS analysis. Both Hf and Zr elements get involved in the formation of this interface. Charges trapped at the nanocrystal/ZrHfO interface are sensitive to the low measure frequency due to its physically close location to the Si surface. Therefore, the frequency dispersion phenomenon of the C-V and G-V curves can be observed. Charges are loosely trapped at the nanocrystal/ZrHfO interface sites, and easily detrap when the band structure turns to the flat band condition or changes the V_g polarity. The charge detrapping phenomenon contributed by the loosely-trapped charges can be reflected as current jumps in the J-V curve, increased relaxation current density, and quick loss in the short-term retention curve. Moreover, the formation of the nanocrystal/ZrHfO interface layer may facilitate the oxygen diffusion through the high-k stack during PDA process, which favors the Si/ZrHfO interface layer (IL) growth. In consequence, the density of the oxygen vacancy in the IL is decreased, which causes the V_{FB} shift in positive direction. Figure 79 shows the change of the IL thickness and V_{FB} shift with respect to the embedded nanocrystals.

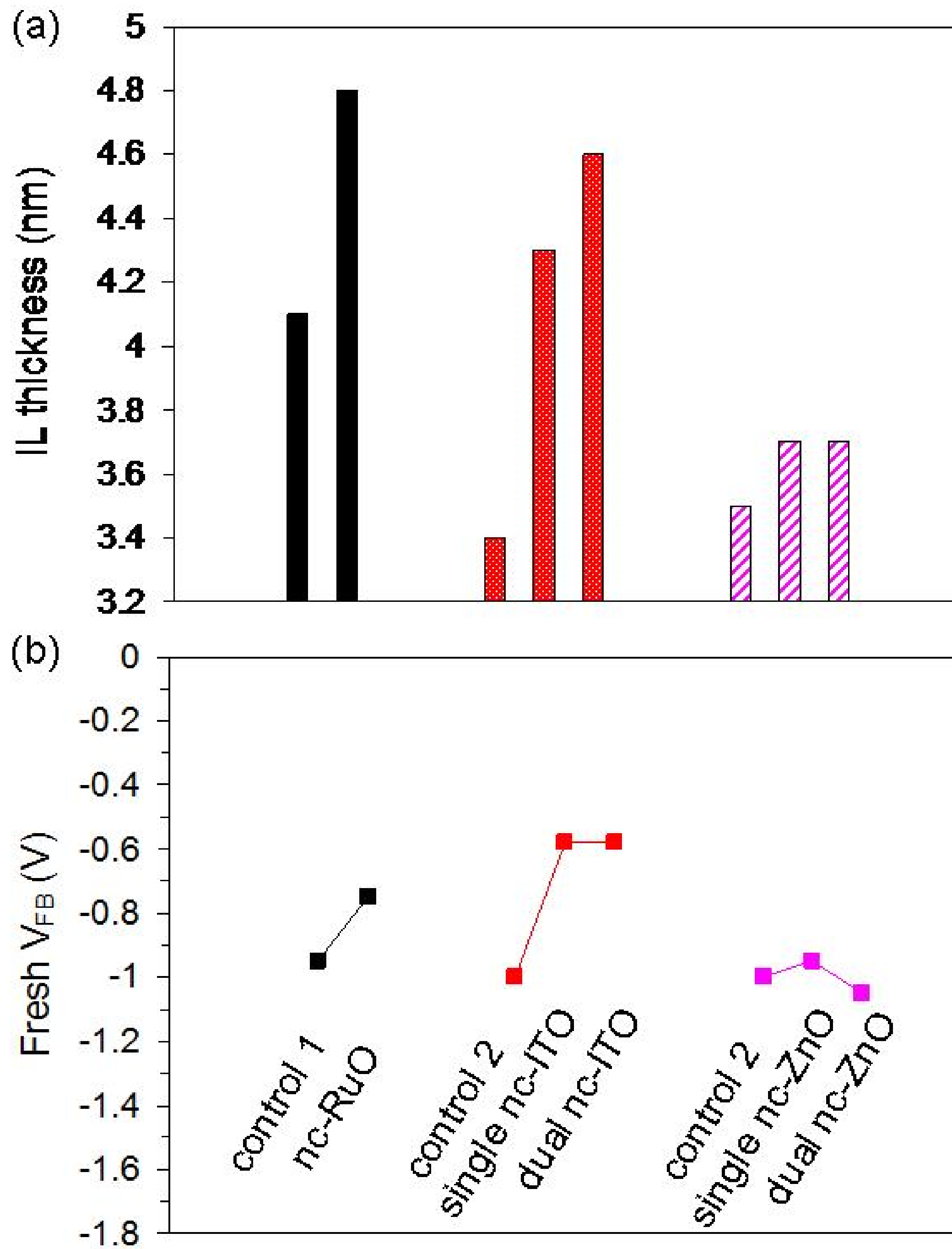


Figure 79. Change of IL thickness and V_{FB} shift with respect to different embedded nanocrystals: nc-RuO, nc-ITO, and nc-ZnO.

Figure 79 shows that for both nc-RuO and nc-ITO embedded capacitors, they have a thicker IL and a more positive V_{FB} than those of their corresponding control samples. For example, for the nc-RuO embedded sample, the increased IL thickness is 0.7 nm (from 4.1 nm to 4.8 nm) and the positive V_{FB} shift is 0.2 V (from -0.95 V to -0.75 V). Also, for the single nc-ITO sample, the increased IL thickness is 0.9 nm (from 3.4 nm to 4.3 nm) and the positive V_{FB} shift is 0.4 V (from -1 V to -0.6 V). The XPS analysis also confirms the formation of nc-RuO/ZrHfO and nc-ITO/ZrHfO interface layers. On the contrary, the nc-ZnO capacitor does not show this kind of significant change, i.e., only slight change in IL thickness from 3.4 nm to 3.7 nm, and in V_{FB} from -1 V to -0.95 V. This difference can be correlated to the different material properties of the nc-ZnO embedded capacitor, i.e., non obvious formation of the nc-ZnO/ZrHfO interface layer, judged by the XPS analysis. Therefore, different electrical characteristics were observed in the different nanocrystals embedded capacitors in this study. The detailed cause to explain why the nc-ZnO/ZrHfO interface layer was not formed after PDA is still not clear. One possibility is the thermodynamic consideration, i.e., the free formation energy of ZnO at 800 ^{o}C (-236 KJ/mol)[191] is smaller than that of In_2O_3 (-576 KJ/mol)[192] and SnO_2 (-358 KJ/mol).[193] Therefore, compared with the In_2O_3 and SnO_2 films, the inter-reaction between the ZnO film and surrounding ZrHfO film is less likely.

On the other hand, although the free formation energy of RuO is even smaller (-120 KJ/mol at 800 ^{o}C)[194] than that of ZnO, the experiment results still show the nc-RuO/ZrHfO interface formation after PDA process. Since the Ru-to-RuO transformation is also involved in this PDA process, the oxygen supply for oxidizing the as-deposited Ru film may be also from the ZrHfO matrix. Therefore, the inter-reaction between the nc-RuO (or as-deposited Ru film) and ZrHfO is still likely. However, the exact mechanism of the nanocrystal/ZrHfO interface formation may be more complicated and need more studies.

5.5.2 Retention Characteristics of Holes and Electrons

Figure 80 shows the comparisons of (a) hole and (b) electron retention characteristics among three kinds of capacitors investigated in this dissertation. The charge retention properties are strongly related to the band offsets between the charge trapping sites and surrounding dielectric films. The comparisons of conduction band and valence band offsets between the ZrHfO film and nc-RuO, -ITO, and -ZnO, are summarized in Table 4. Also, the distribution of internal defects in the ZrHfO tunnel oxide may be also critical. For the hole retention, the charge loss rate of the nc-ITO embedded samples is smaller than that of the nc-RuO embedded sample. This is attributed to the larger E_v offset between nc-ITO and ZrHfO tunnel oxide in the former, i.e., 1.2 eV vs. 0.6 eV. The better retention property (e.g., long-term charge remaining) can be further obtained by using the dual-layer nc-ITO embedded structure.

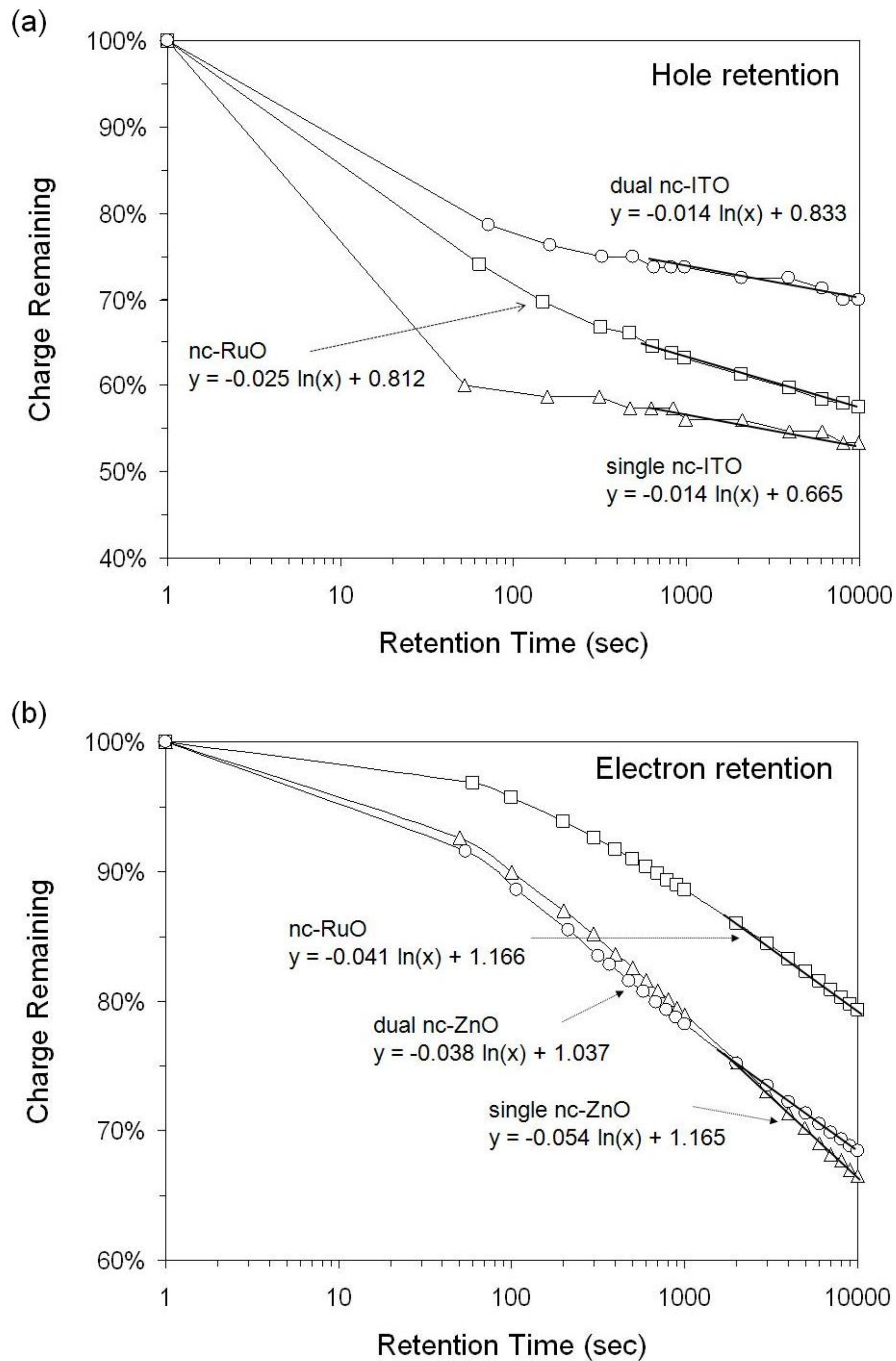


Figure 80. Comparisons of (a) hole and (b) electron retention properties of memory capacitors embedded with nc-RuO, single and dual nc-ITO and nc-ZnO.

For the electron retention, the charge loss rate of the single nc-ZnO sample is larger than that of the nc-RuO embedded sample due to the smaller E_v offset between nc-ZnO and ZrHfO tunnel oxide in the former, i.e., 1.4 eV vs. 2.5 eV. However, both charge loss rate and retention property can be improved by using the dual-layer nc-ZnO structure. Moreover, for the nc-RuO embedded capacitor, the hole loss rate is smaller than the electron loss rate even though the E_v offset between the nc-RuO and ZrHfO is smaller than the E_c offset, i.e., 0.6 eV vs. 2.5 eV. This is because according to the band structure of the nc-RuO embedded ZrHfO gate dielectric stack, as shown in Fig. 51(a), the nc-RuO's E_c edge is aligned to near the middle of the ZrHfO's band gap. It was reported that the concentration of the deep states, i.e., at mid-gap position, is higher than the shallow states in the HfO_2 film.[195] Therefore, the trapped electrons can tunnel back to Si substrate assisted by the deep states in the ZrHfO tunnel oxide. Table 5 summarizes the logarithmically-fitted equations separately for the long-term hole and electron retention conditions of all memory capacitors investigated in this dissertation. The charge remaining after 10 years were also estimated.

Table 5. Fitted equations for long-term hole and electron retention trends of memory capacitors embedded with nc-RuO, single and dual nc-ITO and nc-ZnO. 10-years charge remaining was also estimated.

Hole Retention Trend		10 Years Hole Remaining
nc-RuO	y = -0.025 ln(x) + 0.812	~32%
Single nc-ITO	y = -0.014 ln(x) + 0.665	~40%
Dual nc-ITO	y = -0.014 ln(x) + 0.833	~55%

Electron Retention Trend		10 Years Electron Remaining
nc-RuO	y = -0.041 ln(x) + 1.166	~36%
Single nc-ZnO	y = -0.054 ln(x) + 1.165	~10%
Dual nc-ZnO	y = -0.038 ln(x) + 1.037	~29%

5.6 Summary

Single and dual nc-ITO and nc-ZnO layers embedded ZrHfO high-k memory capacitors have been successfully prepared by the one-pump-down sputtering process followed by the rapid thermal annealing. For the single-layer embedded structure, discrete 3-5 nm size nc-ITO dots with a 2-D spatial density of 1.8×10^{12} cm^{-2} and 3-8 nm nc-ZnO dots with a density of 1.43×10^{12} cm^{-2} were formed in the amorphous ZrHfO high-k film. The formation of the nc-ITO/ZrHfO interface was detected from the XPS spectra, while no obvious formation of the nc-ZnO/ZrHfO interface was observed. The concentration of the nc-ITO/ZrHfO interface increases with the increase of the number of the embedded nc-ITO layers. The C-V hysteresis and gate bias stressed tests indicate that the nc-ITO embedded sample majorly has the hole-trapping capability while the nc-ZnO embedded sample majorly shows the electron-trapping phenomenon. The different charge trapping tendency in the nc-ITO and nc-ZnO embedded samples can be attributed to the difference in the intrinsic material and electrical properties such as defect and band structures. Holes trapped at the nc-ITO/ZrHfO interface were separated from those trapped in the bulk nc-ITO using the frequency-dependent C-V and G-V measurements. However, electrons were deeply trapped in the bulk nc-ZnO sites. The loosely-trapped holes at the nc-ITO/ZrHfO interfaces could tunnel back to Si easily when the energy band structure turns to the flat band condition. This detrapping phenomenon is confirmed from the current jumps in the J-V curve and the large initial charge drop in the retention curve. The dual-layer embedded sample has two separate nanocrystal layers with a higher density than the single-layer embedded sample. The top nanocrystal layer hinders the charges from reaching the gate electrode during the programming process. A large

memory window, high programming efficiency, and long charge retention time can be achieved by using the dual-layer embedded structure. This kind of FG structure can be vital for the future nonvolatile memory applications. The correlation between the electrical properties and formation of the nanocrystal/ZrHfO interface were discussed. The comparisons of the charge retention properties among the nc-RuO, nc-ITO, and nc-ZnO embedded capacitors were also studied.

CHAPTER VI

SUMMARY AND CONCLUSION

Nanocrystals embedded ZrHfO high-k gate dielectric films, i.e., inclusion of Ru nanoparticles and nc-RuO, -ITO, and -ZnO, have been studied for the future Si-MOSFET and nonvolatile memory applications. These kinds of MOS capacitors were prepared in the one-pump-down deposition process by the RF magnetron sputtering technique and followed by the rapid thermal annealing method. Lithography of TiN and Al films has been developed to pattern the gate electrode layer. Physical and chemical properties of the nanocrystals embedded ZrHfO bulk high-k films and interface layers were investigated by the XPS, XRD, HETEM, and EDS analysis. Electrical properties of the nanocrystals embedded ZrHfO MOS capacitor were characterized by the C-V, J-V, CVS, and frequency-dependent measurements.

ZrHfO thin film with an EOT less than 2 nm has been prepared by including Ru nanoparticles into the gate dielectric stack. In addition to forming discrete Ru nanoparticles in the amorphous ZrHfO film, the bulk and interfacial properties, e.g., density of oxygen vacancies and layer composition, were changed with the addition of Ru. The permittivity of the high-k film was increased due to the dipole enhancement, which was supported from the frequency-dependent C-V and G-V measurements change. The Ru-modified ZrHfO gate dielectric film shows a comparative breakdown strength to other high-k films of the same EOT. The temperature-dependent J-V measurement indicates that the Schottky emission mechanism was observed in the low electric field regime while the Frenkel-Poole conduction mechanism was applicable in the high

electric field regime. The inclusion of Ru nanoparticles in the ZrHfO film lowers the energy depth of traps involved in F-P conduction but does not affect the TiN/ZrHfO barrier height. The Ru-modified ZrHfO film has a large breakdown voltage and a long lifetime due to its unique film structure. A 10-years life expectance is estimated at the gate voltage of 2 V. However, the Ru-modified ZrHfO film may have limitation to be applied to the very high frequency devices due to its poor frequency dispersion performance.

MOS capacitors made of the nc-RuO embedded ZrHfO high-k gate dielectric film have been fabricated and investigated for the nonvolatile memory properties. The as-deposited Ru thin film changed into discrete crystalline RuO nanodots with a density of 8×10^{11} cm^{-2} after the 950 °C thermal annealing step. The interface formation at the nc-RuO/ZrHfO contact region was detected by the XPS analysis. The device shows a large memory window of 1.72 V in the gate sweep range of ±9 V mainly due to the hole-trapping mechanism. Its charge trapping and detrapping characteristics and trapping sites differentiation have been studied using the CVS method, stress time- and bias-dependent tests, and frequency-dependent C-V and G-V measurements. Holes and electrons were deeply trapped to the bulk nc-RuO site. However, a portion of holes were loosely trapped at the nc-RuO/ZrHfO interface. The current jumps in the J-V curves together with the retention results confirmed the above charge trapping and detrapping mechanisms. The nc-RuO embedded ZrHfO high-k gate dielectric stack can provide a large memory window for a long charge retention life time, which makes it promising for the future nano-size nonvolatile memory applications.

Dual nc-ITO and nc-ZnO layers embedded ZrHfO high-k MOS capacitors have been successfully fabricated. Replacing the nc-RuO by other nc-conductive oxide materials and using the dual-layer nanocrystals embedded structure is for further improving the nonvolatile memory functions. Discrete 3-5 nm nc-ITO dots and 3-8 nm nc-ZnO dots were formed in the amorphous ZrHfO high-k film. XPS spectra indicate the interface formation at the nc-ITO/ZrHfO contact region. No obvious formation of the nc-ZnO/ZrHfO interface was detected. The memory function of the nc-ITO embedded ZrHfO capacitor is contributed by the hole-trapping mechanism, while that of the nc-ZnO embedded capacitor is mainly contributed by the electron-trapping mechanism. Judged from the frequency-dependent C-V and G-V measurement results, holes trapped at the nc-ITO/ZrHfO interface have different detrapping characteristics from those trapped in the bulk nc-ITO. Most electrons were deeply trapped in the bulk nc-ZnO sites. The dual-layer embedded structure contains two nanocrystal layers with a higher density than the single-layer embedded counterpart. Benefitted from the vertically-separate dual-layer embedded structure, a large memory window, high data programming efficiency, low charge loss rate, and long charge retention time can be achieved. Therefore, the dual-layer nanocrystals embedded floating gate structure is vital for the next-generation nonvolatile memory applications.

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- **C.-H. Lin** and Y. Kuo, "Nonvolatile Memories with Dual-layer Nanocrystalline ZnO Embedded Zr-Doped HfO_2 High-k Dielectric," *Electrochem. Solid-State Lett.*, **13(3)**, H83 (2010).
- **C.-H. Lin**, and Y. Kuo, "Ruthenium Modified Zr-Doped HfO_2 High-k Thin Films with Low Equivalent Oxide Thickness," *J. Electrochem. Soc.*, **158(7)**, G162 (2011).
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- **C.-H. Lin**, and Y. Kuo, "Charge Trapping and Detrapping in nc-RuO Embedded ZrHfO High-k Thin Film for Nonvolatile Memory Applications," **Submitted** to *J. Electrochem. Soc.*, (2011).