# A RADIATION TOLERANT PHASE LOCKED LOOP DESIGN FOR DIGITAL ELECTRONICS

A Thesis

by

RAJESH KUMAR

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2010

Major Subject: Computer Engineering

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Approved by:

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| Chair of Committee, | Sunil P. Khatri |
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| | Duncan M. Walker |
| Head of Department, | Costas N. Georghiades |

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# ABSTRACT

A Radiation Tolerant Phase Locked Loop Design for Digital Electronics. (August 2010)

Rajesh Kumar, B. Tech., Indian Institute of Technology-Roorkee, India

Chair of Advisory Committee: Dr. Sunil P. Khatri

With decreasing feature sizes, lowered supply voltages and increasing operating frequencies, the radiation tolerance of digital circuits is becoming an increasingly important problem. Many radiation hardening techniques have been presented in the literature for combinational as well as sequential logic. However, the radiation tolerance of clock generation circuitry has received scant attention to date. Recently, it has been shown that in the deep submicron regime, the clock network contributes significantly to the chip level Soft Error Rate (SER). The on-chip Phase Locked Loop (PLL) is particularly vulnerable to radiation strikes. In this thesis, we present a radiation hardened PLL design. Each of the components of this design – the voltage controlled oscillator (VCO), the phase frequency detector (PFD) and the charge pump/loop filter – are designed in a radiation tolerant manner. Whenever possible, the circuit elements used in our PLL exploit the fact that if a gate is implemented using only PMOS (NMOS) transistors then a radiation particle strike can result only in a logic 0 to 1 (1 to 0) flip. By separating the PMOS and NMOS devices, and splitting the gate output into two signals, extreme high levels of radiation tolerance are obtained. Our design uses two VCOs (with cross-coupled inverters) and charge pumps, so that a strike on any one is compensated by the other. Our PLL is tested for radiation immunity for critical charge values up to 250fC. Our SPICE-based results demonstrate that after exhaustively striking all circuit nodes, the worst case jitter of our hardened PLL is just 37.4%. In the worst case, our PLL returns to the locked state in 2 cycles of the VCO clock, after a radiation strike. These numbers are significant improvements over those of the best previously reported approaches.

To my family

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I would like to thank my family and Anil for the support they have given over the years. Without their encouragement and understanding, it would have been impossible for me to reach this level.

I am grateful to STMicroelectronics colleagues, Manish Trivedi, Sachin Gulyani, Piyush Jain, and Jitendra Dasani, who helped me to learn basic concepts of VLSI design, as well as advanced concepts on memories. Especially Manish who not only helped me to learn circuit design concepts during my stay at ST, but also talked to me over the phone for several hours to clear my doubts.

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TABLE OF CONTENTS

# LIST OF TABLES

# LIST OF FIGURES

FIGURE Page

# CHAPTER I

## INTRODUCTION

With relentless device scaling, lowered supply voltages and higher operating frequencies, the noise margins of VLSI designs are reducing. Thus VLSI circuits are becoming more vulnerable to noise due to crosstalk, power supply variations and single event upsets (SEUs or soft errors. SEUs are caused when radiation particles such as protons, neutrons, alpha particles, or heavy ions strike sensitive diffusion regions in VLSI designs.

Historically, SEUs were troublesome for military and space applications. This is mainly due to the abundance of radiation particles in the operating environment of such systems. However, with device scaling, SEUs are also becoming problematic for terrestrial applications. There are critical applications like biomedical, military and space which demand highly reliable systems. Therefore, it is important to design radiation tolerant circuits.

Radiation hardening is often employed to improve the reliability of the system. Most of the existing approaches focus on hardening combinational and sequential designs [1, 2, 3, 4, 5, 6, 7, 8, 9]. Very little attention has been paid to SEU due to radiation particle strikes on clock nodes, despite their significant contribution to the chip level SEU. Clock node upsets account for nearly 20% of the overall sequential SER [10]. The global clock distribution network is relatively immune to upsets [10] since it typically contains large buffers and large node capacitances, and has a large RC time constant, thereby acting like a low pass filter. The authors in [10] report that the contribution to the SER of the global clock grid is negligible (0.1%) compared to that of the regional regenerator circuits and the clock PLL. Strikes in these sections of the clock generation circuitry can result in *radiation-*

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*induced clock jitter* and voltage glitches (also referred to as *radiation-induced race*) in the clock nodes. These effects can cause incorrect data to be latched by the sequential elements in the design, potentially resulting in catastrophic failures. The clock distribution network in a chip consists of a global clock generation and distribution network followed by regional clock regeneration buffers. The globally distributed clock signal is relatively immune to radiation strikes due to the large node capacitances [10] of the clock distribution network. However, most modern designs require an on-chip Phase Locked Loop (PLL) to synchronize an external reference clock with the clock signal on-chip. The PLL contains extremely sensitive analog circuitry, and therefore a radiation strike in this circuit can cause catastrophic failures in the design. Similarly, regional clock regenerators are also very sensitive to radiation strikes.

In this thesis, we present a radiation hardened PLL design. Our design consists of a radiation hardened phase frequency detector (PFD), charge pump (CP) and low pass filter (LPF), voltage controlled oscillator (VCO) and clock divider. Our VCO design consists of two current starved ring oscillator structures, with cross-coupled signals which help to ensure that the effect of a radiation strike on one ring is compensated by the other ring. Also, two charge pumps drive the control signals of the two ring oscillators again ensuring that any VCO compensates for a radiation strike on its counterpart. All the components of the PLL utilize extremely radiation tolerant split-output gates whenever possible. These gates exploit the fact that if a node is driven using only PMOS (NMOS) transistors then a radiation particle strike can result only in logic 0 to 1 (1 to 0) flip [6, 8].

In the remainder of this chapter, subsection I-A provides background information about single event upsets and subsection I-B discusses the basic operation of a PLL and its main applications.

## I-A. Single Event Upset (SEU)

Cosmic rays present in the atmosphere are the main source of radiation particles like protons, neutrons and heavy ions. These particles generate free electron-hole pairs along their path when they pass through a semiconductor material. These particles come to rest after losing their energy. The energy transferred by radiation particles is described by its Linear Energy Transfer (LET) value. LET is defined as the energy transferred by a radiation particle per unit length, normalized by the density of the target material. A radiation particle strike deposits charge in the material. The amount of collected charge varies from material to material, and in silicon it is given by equation

$$Q = 0.01036 \cdot L \cdot t$$

Here $L$ is the Linear Energy Transfer (LET) of the ion (expressed in MeV/cm$^2$/mg), $t$ is the depth of the collection volume (expressed in microns), and $Q$ is charge in pC.

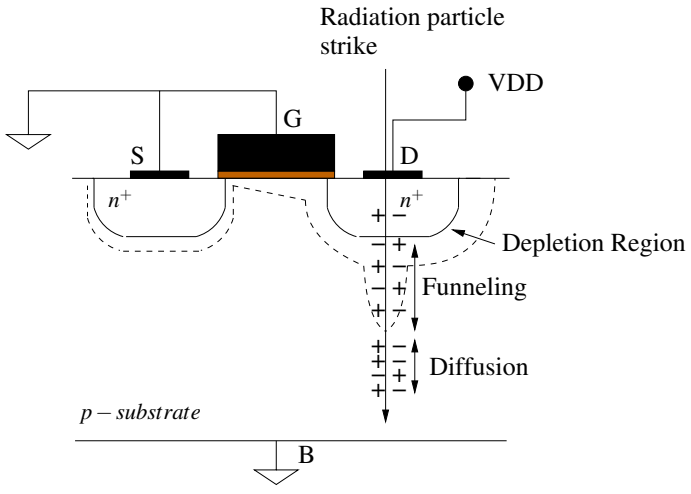


Fig. I.1. Charge deposition and collection by a radiation particle strike

When charge is deposited due to a radiation particle strike, the deposited charge is

collected by the different electrical terminals of the device, which results in current and voltage transients. The charge deposited by radiation particles is collected through drift and diffusion process. Consider an NMOS transistor shown in the Figure I.1. The gate, source and bulk terminals are connected to *GND* and the drain is connected to *VDD*. The junction between drain and bulk terminal is reverse biased, therefore there will a strong electric field in the depletion region of drain-bulk junction. Since a radiation particle strike generates free electron-hole pairs, the electric field present in the depletion region will lead to the collection of electrons at the drain terminal and holes at bulk terminal. Thus, a reverse electric field in the depletion region leads to the collection of charge at the drain terminal. Therefore, all reverse biased p-n junctions in the circuit are sensitive to radiation particle strikes. For example, if a radiation particle strikes at the drain terminal (as shown in Figure I.1), it will generate free electron-hole pairs along its path. In the presence of the electric field in the depletion region, electrons and holes are separated by the *drift* process. This phenomenon reduces the width of depletion region. As a result the potential drop across the depletion region reduces, since the voltage between the drain and bulk terminals is still *VDD*. The reduction in potential drop across the depletion region will lead to a voltage drop into the substrate region. Therefore, the electric field present in the depletion region penetrates into the substrate region. This electric field further enhances the flow of electrons from the substrate to the bulk. The enhanced electron flow process is called *funneling*. The electrons which are not collected at the drain terminal through the drift process, diffuse towards the drain terminal due to the concentration gradient. Therefore, charge is also collected at the drain terminal by the *diffusion* process. Overall the radiation particle strike at drain terminal causes electrons to flow from the bulk to the drain terminal. In other words, any radiation particle strike induces a current which flows from n-diffusion to p-diffusion. This induced current results in a voltage glitch at the drain terminal. A system failure may result if the voltage glitch at drain terminal is captured by a memory

element in the design. This phenomena is called a single event upset (SEU) or soft error. A radiation strike in a combinational logic circuit is often referred to as a single even transient (SET).

The current pulse that results from a particle strike is traditionally modeled as a double exponential function [11]. The expression for the pulse is

$$i_{seu}(t) = \frac{Q}{(\tau_\alpha - \tau_\beta)}(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}) \tag{1.1}$$

Here $Q$ is the amount of charge deposited as a result of the ion strike, while $\tau_\alpha$ is the collection time constant for the junction and $\tau_\beta$ is the ion track establishment time constant. The time constants $\tau_\alpha$ and $\tau_\beta$ depend on several process related parameters, and typically $\tau_\alpha$ is of the order of 200ps and $\tau_\beta$ is of the order of tens of picoseconds [4, 12].

## I-B. Phase Locked Loop Operation

There are several digital applications that require the on-chip generation of a clock signal. Current microprocessors and high performance digital circuits operate at or above gigahertz clock frequencies. Crystal oscillators can generate low jitter clocks over a frequency range from tens of MHz to 200MHz. A phase locked loop (PLL) is often used to multiply the frequency of a reference clock (which is typically generated from a crystal oscillator) to produce an on-chip clock in the gigahertz range. Another important application of a PLL is *clock synchronization*. A PLL is also used to synchronize an internal on-chip clock to an external clock. This makes a PLL an essential component in digital system designs.

The basic architecture of a PLL is shown in Figure I.2. The PLL usually consists of a phase frequency detector, a charge pump, a low-pass filter (LPF), a voltage controlled oscillator and a frequency divider.

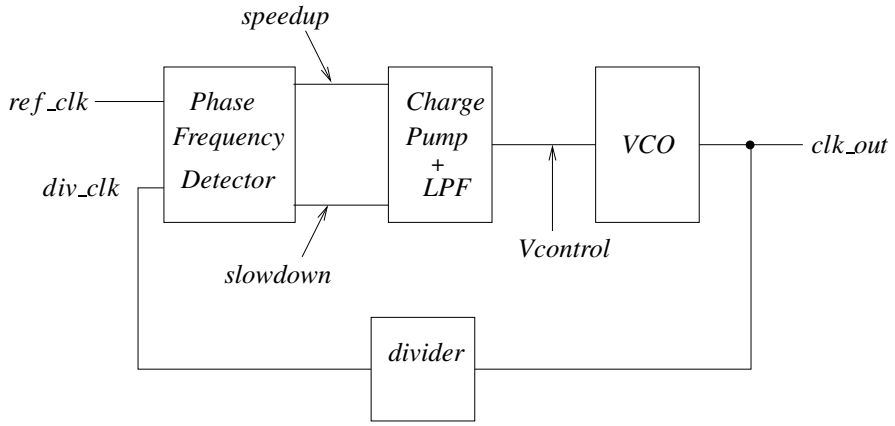


Fig. I.2. Block diagram of a generic PLL

The phase frequency detector (PFD) outputs *speedup* (*slowdown*) pulses based on whether the divided clock *div_clk* lags (leads) the reference clock *ref_clk*. The width of these pulses is proportional to the phase difference between the reference and divided clocks. These pulses drive a charge pump (CP) and low pass filter (LPF). Charge is dumped onto output node *Vcontrol* of the CP and LPF whenever a *speedup* pulse occurs, thereby increasing the voltage of the *Vcontrol* node. Likewise, charge is removed from the *Vcontrol* node when a *slowdown* pulse occurs, thereby reducing its voltage. The *Vcontrol* node drives a voltage controlled oscillator (VCO), whose frequency increases when *Vcontrol* increases. The output of the VCO is the system clock (*clk_out*) which drives the clock distribution network of the IC. It is divided appropriately to generate *div_clk*. Note that division is frequently required since the internal clock in a modern IC can have a significantly higher frequency (in the GHz range) than the *ref_clk*, which is typically generated by an off-chip crystal oscillator operating below 200MHz.

### I-B.1. Voltage Controlled Oscillator (VCO)

A voltage controlled oscillator generates a periodic signal with a frequency that varies (ideally linearly) with the input control voltage *Vcontrol*. A VCO is implemented using a ring oscillator with a slight modification. The standard ring oscillator is modified by replacing inverters with current-starved inverters (which we call *ring inverters*), as shown in Figure I.3. The frequency of the VCO is determined by the delay of a ring inverter. The delay of each ring inverter is controlled by the varying gate voltage *Vcontrol* of its current starved transistor. The maximum discharge current (and hence delay of the ring inverter) is limited by the current starved transistor. Lowering *Vcontrol* reduces the discharge current and hence increases the propagation delay. The ability to alter the propagation delay per stage allows us to control the frequency of the ring oscillator structure.

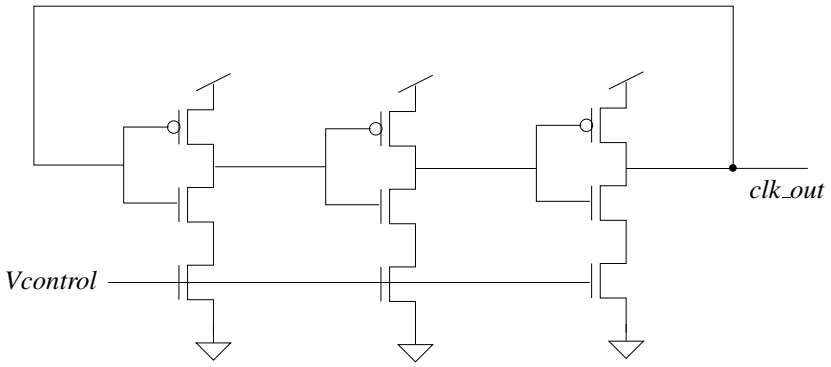


Fig. I.3. Conventional VCO

### I-B.2. Phase Frequency Detector (PFD)

The schematic of a traditional phase frequency detector is shown in Figure I.4. The inputs of the PFD are *ref_clk* and *div_clk* and the outputs are the *speedup* and *slowdown* signals. The outputs - *speedup* and *slowdown* – are dependent on the phase and frequency difference

of input signals (*ref_clk* and *div_clk*).

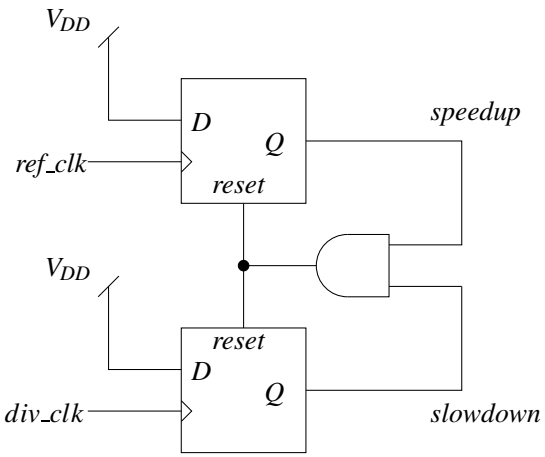


Fig. I.4. Conventional PFD

The PFD consists of two D flip-flops and an AND gate. The inputs of D flip-flops are connected to the supply voltage *VDD*. The clock input of the two flip-flops are connected to *ref_clk* and *div_clk*. There could be three possible scenarios based on the arriving times of the *div_clk* and *ref_clk* signals. Consider the waveforms shown in Figure I.5 for first case (when *div_clk* is lagging behind *ref_clk*). The *speedup* signal goes high when a low to high transition is encountered at *ref_clk*, whereas the *slowdown* signal goes high as soon as a low to high transition is encountered on *div_clk*. At this time, both the *speedup* and *slowdown* signals are high, and as a result, the *reset* signal is asserted by the AND gate. The *reset* signal sends both *speedup* and *slowdown* back to zero. In this particular case, when *ref_clk* leads the *div_clk*, the *speedup* pulse is wider than the *slowdown* pulse (and its width is proportional to the phase difference between *div_clk* and *ref_clk*). In the second case (when *div_clk* is leading *ref_clk*), the *slowdown* pulse will be wider than *speedup* pulse and it's width will again be proportional to the phase difference between the *div_clk* and *ref_clk* signals. In the third case, when both signals *div_clk* and *ref_clk* are in phase, there

will be short pulses at *speedup* and *slowdown* signals.

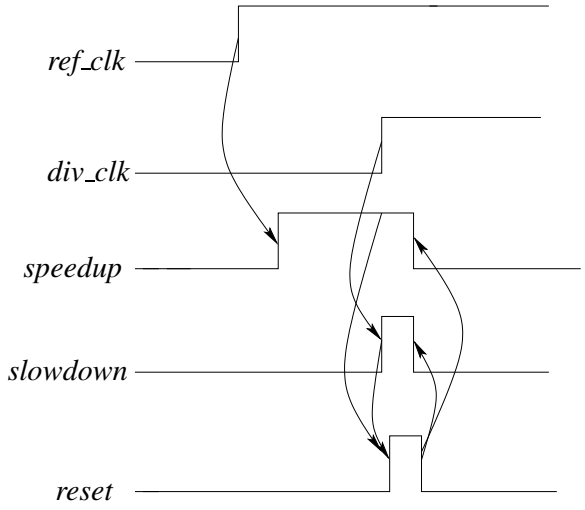


Fig. I.5. Waveform for PFD when *div_clk* is lagging behind *ref_clk*

### I-B.3. Charge Pump and Low Pass Filter

A charge pump typically uses two current mirrors (as shown in Figure I.6) to convert pulses at the *speedup* and *slowdown* signals into an analog control voltage *Vcontrol*. The *Vcontrol* signal is fed to the VCO to control its frequency.

A pulse on the *speedup_b* signal adds charge to the capacitor $C_1$ (proportional to the width of the *speedup_b* pulse), while a pulse on the *slowdown* signal removes charge from $C_1$ (proportional to the *slowdown* pulse width). If the pulse width of the *speedup_b* is larger than that of *slowdown* pulse, there is a net increase in the control voltage *Vcontrol*. This effectively increases the frequency of the VCO.

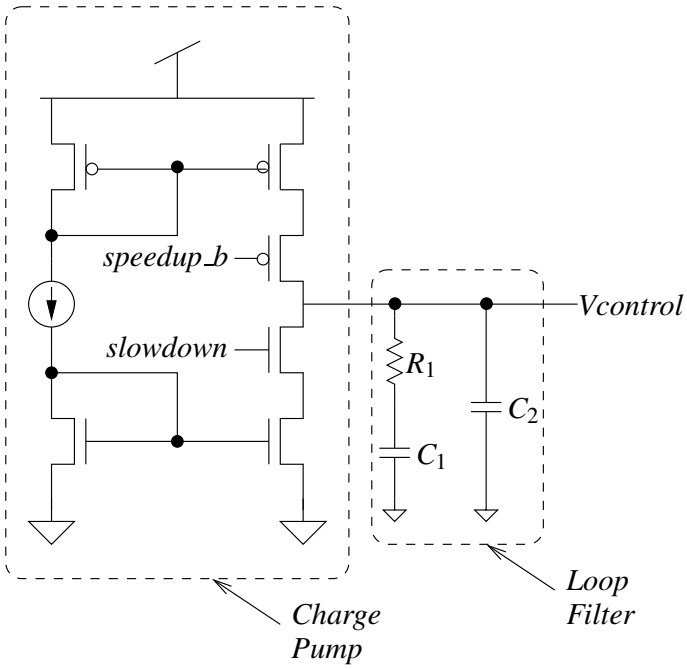


Fig. I.6. Charge pump with low pass filter

### I-B.4. Frequency Divider

A frequency divider is used to divide the frequency of the clock generated by the VCO, to produce *div_clk*. The frequency divider determines the relationship of the output frequency with respect to the input reference frequency. The most common circuits used in the frequency divider are binary counters. An $n$-bit binary counter divides the input clock frequency by $2^n$. There are two types of binary counters - synchronous and asynchronous. Each has its own advantages and disadvantages for a PLL design. Each stage of an asynchronous counter operates at lower frequency (which results in reduced power dissipation). However, an asynchronous counter results in high jitter, since jitter is accumulated at every stage. This is due to the fact that output of one stage is fed to the clock input of the next stage. In contrast, a synchronous counter results in reduced jitter, but with a power over-

head. The reason for the high power consumption of the synchronous design is that each stage of a synchronous counter operates at the input clock's frequency (which is high).

# CHAPTER II

## PREVIOUS WORK

There has been a great deal of work on radiation hardened circuit design approaches. Many papers report the results of experimental studies in the area of hardened logic circuits [4, 5, 13, 14], while others focus on radiation hardened memory designs [15, 16, 17, 18, 19, 20]. Since memories are particularly susceptible to SEU/SET events, these efforts were crucial for space and military applications. Yet other approaches address the modeling and simulation of radiation events [21, 22, 23].

In [24], the authors proposed an analytical model for SEU induced transients in combinational circuits. Their model computes the pulse width of the voltage glitch that results from a SEU particle strike. The transistor $I_{DS}$ model was used for the analysis, which increases the accuracy of results. In [25], a closed-form analytical expression was proposed to compute the shape of the voltage glitch induced by a radiation particle strike. A load current model of the gate was used for the SET analysis. The load current model results in better accuracy in comparison to a transistor $I_{DS}$ model. The authors also considered the effect of the ion track establishment constant $\tau_\beta$ of the radiation induced current pulse. In [26], authors proposed a model for dynamic stability of a 6-T SRAM cell in the holding state, under the influence of an SEU event. Their model can predict the effect of error events accurately, and the average critical charge estimation error of their model was 2.5% (compared to SPICE simulation).

Circuit hardening approaches can be classified as device level, circuit level [1, 2, 4, 5, 8, 9] and system level [17]. The device and circuit level approaches are typically based on fault *avoidance*, while system level approaches typically depend on error *detection and tolerance* mechanisms. Triple modular redundancy (TMR) is a classical example of a system level design approach. Device level approaches require processing changes to improve

the radiation immunity of a design, whereas circuit level hardening approaches use special circuit design techniques that reduce the vulnerability of a circuit to radiation strikes.

Although much work has been published in the literature on hardening techniques for combinational and sequential circuits, little attention has been devoted to the problem of clock node upsets and their effect on the chip level sequential SER. The authors of [27] performed an experimental analysis to calculate the contribution of clock node upset to SER on the ”RH1020” chip in high energy radiation environments. They suggest that the clock upset rate has a strong and linear dependence on clock frequency. They suggest ad-hoc methods to reduce clock node upsets, such as reducing clock frequency and using redundancy in the clock network. However, no experimental results or design approaches were presented. Recently, the authors of [10] studied the effect of radiation particle strikes on clock nodes. They partitioned the radiation induced transients on the clock into two categories: *radiation-induced clock jitter* and *radiation-induced race*. The latter category of clock transients is characterized by a missing clock pulse, and can cause catastrophic system failure. The first category can be designed around by guard-banding, provided the jitter is not too large. The authors of [10] report that 20% of total sequential SER is due to clock node upsets. The contribution of radiation-induced jitter is less than 2% of the total sequential SER. This means that most of the upsets occur due to radiation-induced race. Another important conclusion of their experiments was that the contribution of the global clock distribution network is 0.1% of the overall SER due to clock node upsets. Hence, we can conclude that radiation particle strikes on the regional clock regenerators and the clock PLL itself are primarily responsible for the SER due to radiation strikes on the clock network.

In [28], authors proposed two radiation hardened designs for the regional clock regenerators - a TMR approach and a split-output SEU tolerant inverter approach. Their hardened regenerator circuits suppress glitches due to SEU strikes, and also improves the

clock jitter as compared to a regular clock regenerator. They showed that the split-output inverter based design achieves smaller area overhead, better jitter and improved glitch suppression compared to the TMR approach. Their design only protects clock regenerators from radiation particle strikes.

The vulnerability of conventional digital phase locked loops (D-PLLs) to a radiation particle strike was observed through simulations and experiments [29, 30]. The SET response of the PLL is dominated by the SET response of the charge pump module [29, 30]. In [29], the authors present a hardened PLL operating at 700 MHz. The authors study strikes only on the charge pump output, and observe that a 200 fC strike causes their hardened PLL to require 98ns (68 cycles) to recover lock, with at least one clock pulse being displaced by more than $2\Pi$ radians. It was reported in [30] that a radiation particle strike on their proposed hardened PLL (operating at 200 MHz) induced transients that result in a loss of lock for 54 cycles.

In contrast to [29, 30], we exhaustively strike each node[1] of our hardened PLL (including the charge pump output) with a $Q$ value of 250 fC (higher than that of [29]). We strike a node at 10 equally spaced time instants in the reference clock period. Also, we utilize a more radiation sensitive 65nm process in comparison to a 130nm process for [29]. In the worst case, we find that we require 2 cycles of the VCO clock to return to the locked state. The maximally disturbed clock pulse exhibits a phase displacement of just 2.35 radians (i.e. a worst case jitter of 37.4% of the VCO clock period).

In this thesis, we present a radiation hardened PLL design. Each of the components of our PLL are radiation hardened. Our VCO design consists of two current starved ring oscillators, with cross-coupled signals which ensure that the effect of a radiation strike on one ring is suppressed by the other ring. Also, two charge pumps drive the control signals of

[1] We strike all nodes in the circuit, except nodes that are electrically symmetrical.

the two ring oscillators again ensuring that any VCO compensates for a radiation strike on its counterpart. All the above components of the PLL utilize extremely radiation tolerant split-output [31] gates whenever possible. These gates exploit the fact that if a node is driven using only PMOS (NMOS) transistors then a radiation particle strike can result only in logic 0 to 1 (1 to 0) flip [6, 8].

# CHAPTER III

# OUR APPROACH

In this chapter we describe our radiation hardened PLL design. We first describe the architecture of our PLL in subsection III-A, then in subsection III-B, we describe the radiation hardened gates and flip-flops that are used in all the blocks of the PLL. We next discuss the different blocks of our PLL, starting with the VCO (subsection III-C), phase frequency detector (subsection III-D), charge pump and low pass filter (subsection III-E) and clock divider (subsection III-F). The system level approach we followed to design the closed loop system is outlined in subsection III-G.

## III-A. Phase Locked Loop Operation

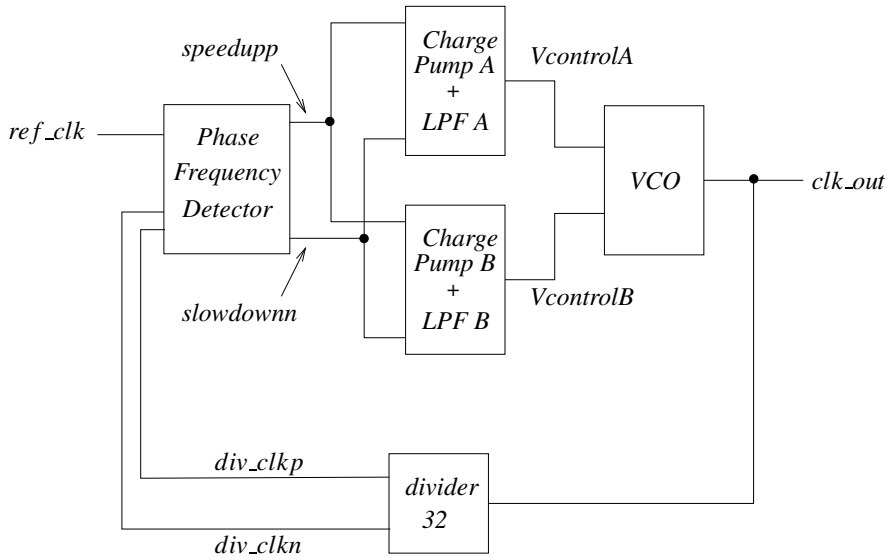


Fig. III.1. Block diagram of our PLL

The block diagram of our radiation hardened PLL is shown in Figure III.1. It is con-

ceptually similar to Figure I.2, but with significant circuit level differences to achieve radiation hardening. First, it utilizes two independent CP/LPF blocks, which drive two separate VCOs. The VCOs are implemented as current starved ring oscillators (using 3 ring inverters in the ring). A unique feature of these two VCOs is that their internal nodes are cross-coupled to ensure that if one of them is struck by a radiation particle, the corresponding signals from the other VCO compensate for the strike. The *VcontrolA* and *VcontrolB* nodes drive 6 current starved NMOS transistors of each ring oscillator, as shown in Figures III.4 and III.5. When the voltage of the *VcontrolA* and *VcontrolB* signals is low, the ring oscillates at a lower frequency than when these voltages are high. The gates and flip-flops in all the blocks of our VCO are implemented in a split-output manner [31] to achieve radiation hardening.

### III-B. Radiation Hardened Flip-flops and Logic Gates

Logic gates and flip-flops in all the blocks of our PLL are implemented in a radiation hardened manner. A radiation particle strike on the diffusion region of a MOSFET induces a current which always flows from the n-type diffusion to the p-type diffusion through a pn junction [8]. This implies that if a gate output is driven using only PMOS (NMOS) transistors then a radiation particle strike cannot flip the node voltage from 1 to 0 (0 to 1). In other words, if a particle strikes the diffusion of a PMOS transistor of an inverter whose output is at logic 1, then this particle strike will not cause the output node voltage to flip if the output of a logic circuit is driven only by PMOS transistors. Similarly, a particle strike at the diffusion of a NMOS transistor of the inverter (with an output node at logic 0) will not result in a SET if the output is driven only by NMOS transistors. This key idea suggests that if the output of a logic circuit is driven only by PMOS (NMOS) transistors, then that logic circuit will be tolerant to node flips from 1 to 0 (0 to 1). In [8, 9], this idea was used

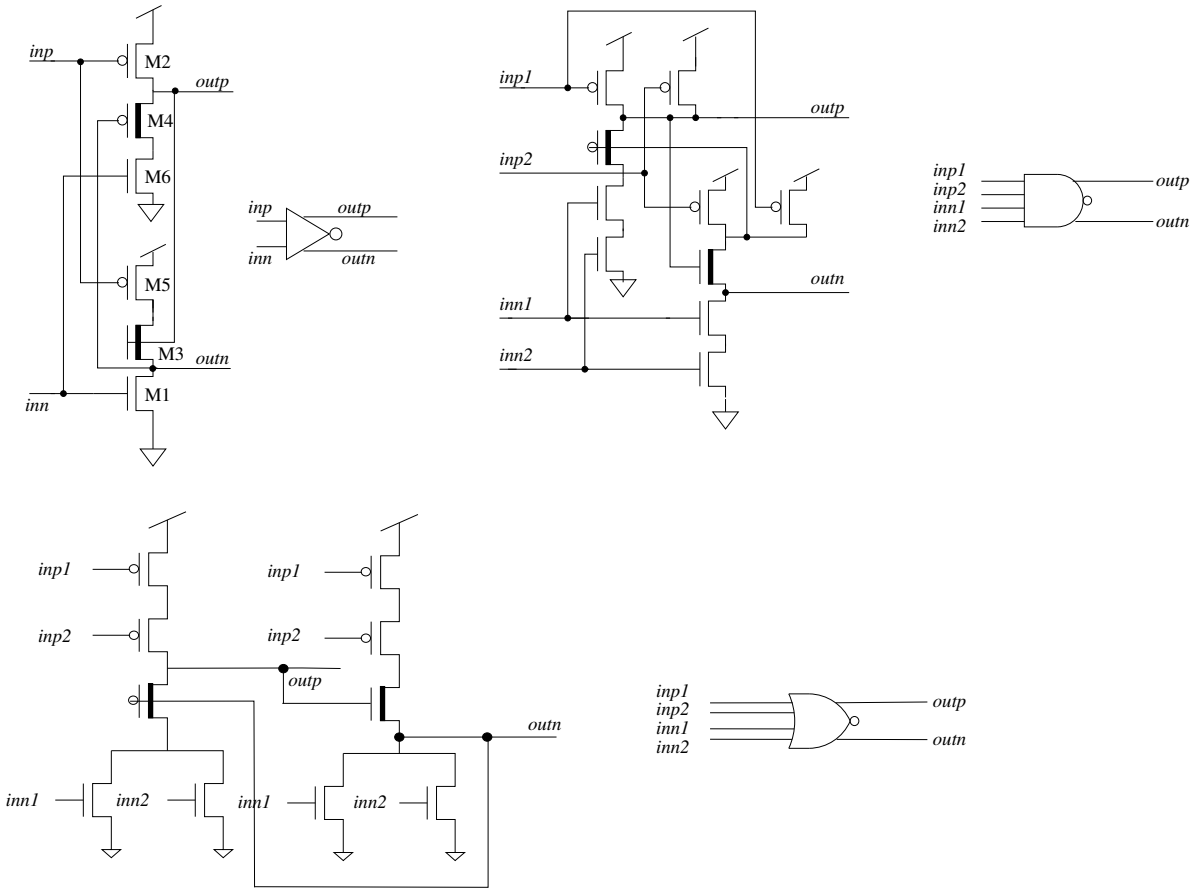


Fig. III.2. Radiation hardened logic gates (INV, NAND2 and NOR2) used in our PLL

to design radiation hardened SRAM and flip-flop cells, while in [31], it was used to design highly SEU tolerant standard cell gates. The flip-flop and logic gates used in our design (shown in Figures III.3 and III.2 respectively, are designed using the approach of [8, 9] and [31]).

A traditional inverter can experience both positive or negative glitches[1] since both PMOS and NMOS transistors are connected to the output node. We refer the reader to [8,

[1] A positive glitch is defined as the condition in which the node voltage switches from 0 to 1 and then back to 0. Similarly, a negative glitch is defined as a node voltage transition from 1 to 0 to 1.

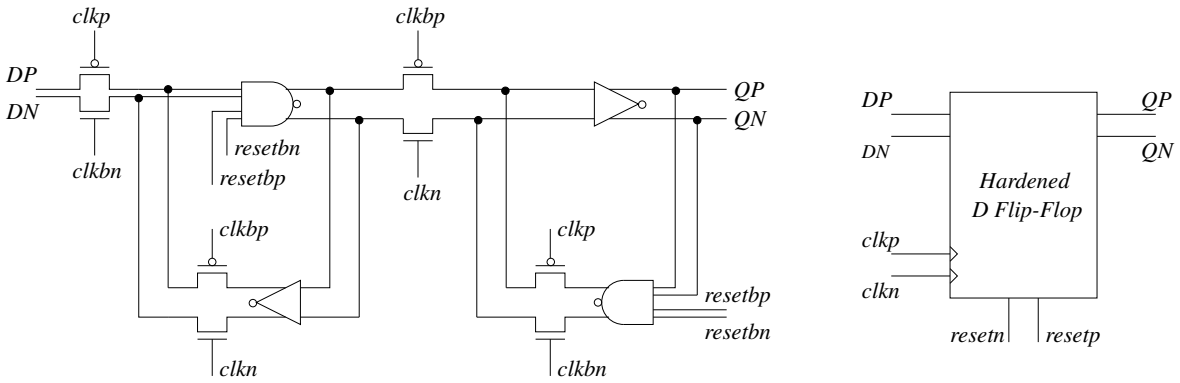


Fig. III.3. Radiation hardened flip-flop used in our PLL

9, 31] for a detailed description about why the gates in Figure III.2 and the flip-flop of III.3 are radiation tolerant, and also functionally correct.

Before proceeding further, we briefly state some observations that were made in [8, 9, 31] about the split-output hardened gates [31] and flip-flops [8, 9] that we used in our PLL. Note that the split-output hardened inverter shown in Figure III.2 has 2 inputs ($inp$ and $inn$) and 2 outputs ($outp$ and $outn$). Both inputs and both outputs are of the same polarity during normal operation. Note that the output nodes $outp$ and $outn$ of the inverter respectively drive only PMOS or NMOS transistors of the gates in their fanout. Note that in general, such a split-output gate has $2n$ inputs (compared to $n$ inputs for any unmodified gate) and 2 outputs (of the same polarity), as indicated in the gate symbols beside each of the gates in Figure III.2. Note that the transistors M3 and M4 of the inverter in Figure III.2 are selected to be low threshold voltage transistors (indicated by a thicker line in the figure). This is done so as to increase the voltage swing at nodes $outp$ and $outn$, and to bring them closer to the rail voltages. Also, note that the reduced voltage swings at $outp$ and $outn$ do not increase the leakage currents in a similar split-output gate in its fanout. This is because, when the node $outp$ is at $|V_T^{M4}|$ then $outn$ is at GND, due to which the NMOS device of

the fanout gate is completely turned off (while its PMOS device is turned on). A similar argument holds for the case when $outp$ is at VDD and $outn$ is at VDD-$V_T^{M3}$ Therefore, the leakage currents in a fanout gate do not increase due to non-rail voltage swing at its inputs.

Note, as stated in [8, 9, 31], that these approaches result in radiation immunity to extremely high energy particle strikes. The width of the voltage glitch induced by a radiation particle strike at $outp$ should be less than the clock period $T$ for correct operation. Hence the critical charge ($Q_{cri}$) for the circuit is the maximum amount of charge dumped by a radiation particle such that a voltage glitch of pulse width $T$ is encountered in the circuit. Even for the smallest (most sensitive to radiation) inverter in a circuit operating at 1.5 GHz, (implemented in a 65nm process) the authors of [31] show that a radiation strike with deposited charge as high as 650fC can be tolerated.

Our flip-flop design is shown in Figure III.3, along with its circuit symbol. Our flip-flop is conceptually a traditional resettable D flip-flop, with the individual gates implemented in a radiation hardened manner (using the split output approach described above).

### III-C. Radiation Hardened VCO

Our radiation hardened VCO is shown in Figure III.4. It consists of two ring oscillators (labeled *ringA* and *ringB*) in contrast to traditional VCO (shown in Figure I.3). Each ring oscillator consists of three current starved *ring inverters*. Two VCO control voltage signals (called *VcontrolA* and *VcontrolB* respectively) each drive two NMOS devices in the ring inverter, which acts as a current starved inverter. A low value of *VcontrolA* or *VcontrolB* causes the rings to operate at a lower frequency, and vice versa. Under normal operation, the voltages of *VcontrolA* and *VcontrolB* track exactly.

Just like the inverter shown in Figure III.2, each of the ring inverters in the 2 ring oscillators are radiation hardened. However, unlike the inverter shown in Figure III.2, each

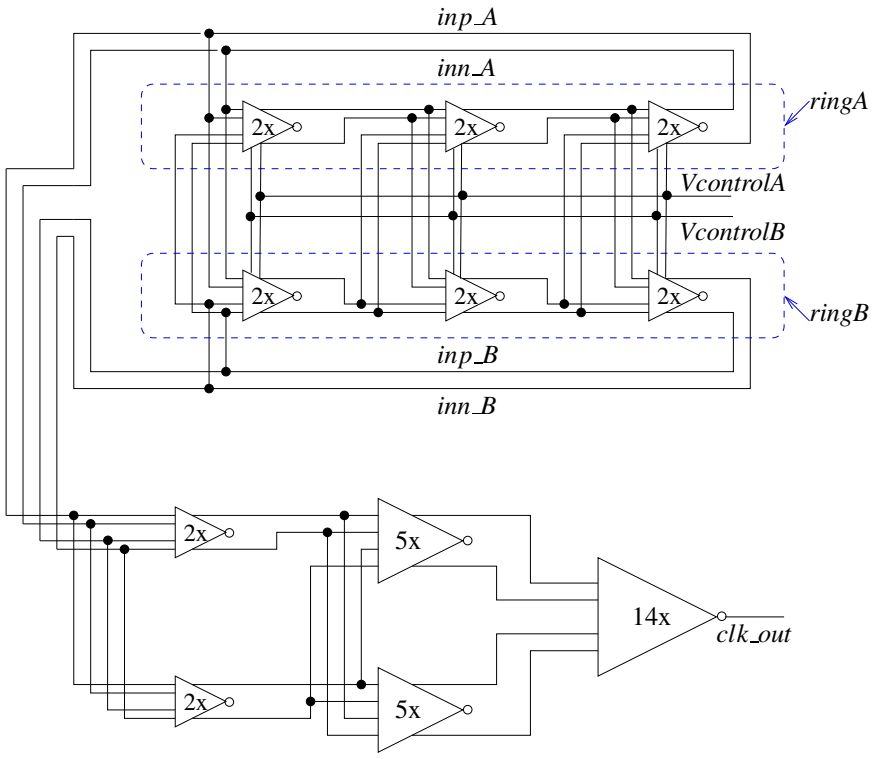


Fig. III.4. Radiation hardened VCO

of the ring inverters in the any of the ring oscillators has 4 inputs. Two of these inputs are driven by an inverter in the same ring, while the other two inputs are driven by an inverter in the other ring. The design of the ring inverter is shown in Figure III.5 (which shows the circuit of a ring inverter of *ringA*). Effectively, the ring inverter of Figure III.5 consists of two copies of the hardened inverter of Figure III.2, whose outputs (*outp_A* and *outn_A*) are shorted together. One of the two hardened inverters in Figure III.5 is connected to a driving ring inverter from *ringA* (via signals *inp_A* and *inn_A*), while the other is connected to the corresponding driving ring inverter from *ringB* (via signals *inp_B* and *inn_B*). A ring inverter of *ringB* is constructed similarly.

Each ring inverter is radiation hardened since it uses two copies of the hardened in-

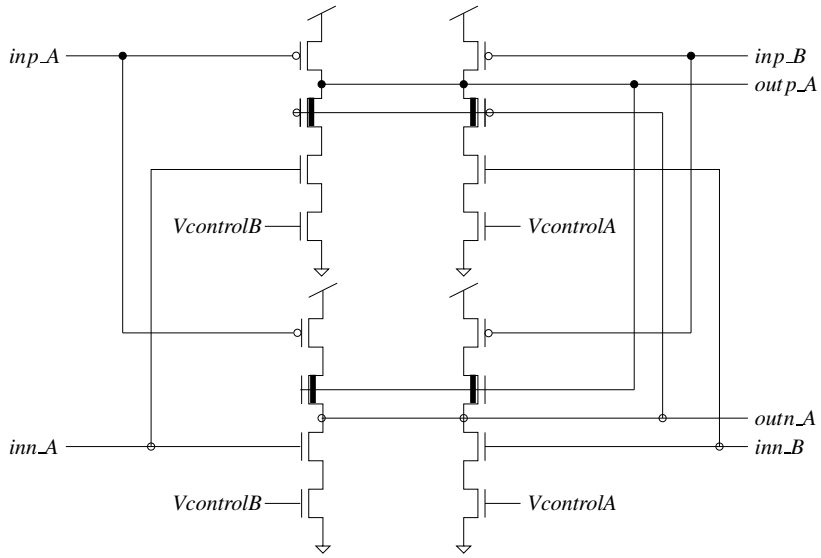


Fig. III.5. Ring inverter design

verter of Figure III.2. Since the outputs of these two hardened inverters are shorted, each ring compensates for radiation strikes in the other ring. For instance, in Figure III.5, consider the situation where all 4 inputs are high, and just about to fall. Now if there is a strike on the *inp_A* input such that it experiences an upward voltage glitch (which causes its falling transition to be delayed), then *ringA* would ordinarily experience a delayed rising transition on *outp_A*, causing the two rings to lose synchronization (in case we did not use ring inverters but rather just used the inverter from Figure III.2). However, in our ring inverter there is an alternate inverter driving *outp_A*, and therefore the rising transition on *outp_A* would be minimally delayed, since the input signals from the other ring (*inp_B* and *inn_B*) are unaffected by the strike. In this manner, the ring inverters of each ring help compensate for radiation strikes on the other ring. Alternately stated, there is never a time when the output of any ring inverter in either ring is at a high impedance (something that would be possible if we used the hardened inverters of Figure III.2 instead of the ring inverter of Figure III.5).

Note that each ring is driven by two control voltages - *VcontrolA* and *VcontrolB*. The two control voltages are driven by two independent charge pumps in our design, as we will explain in the sequel. These control voltages each drive 2 current starving NMOS devices in every ring inverter (of either ring). This helps to compensate for a radiation strike on any one of these control voltages.

The final output of the ring oscillator consists of 4 signals (two output signals from each ring). These drive a chain of inverters (also implemented in the same manner as ring inverters) shown in the bottom of Figure III.4. When the drive strength of both inverter chains is sufficiently strong, a single inverter is used to produce the final output *clk_out* of the VCO.

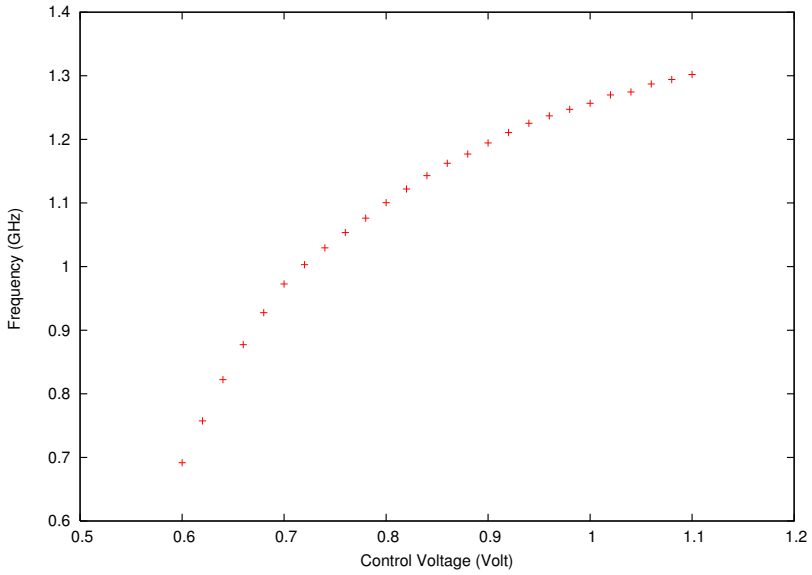


Fig. III.6. VCO Frequency versus control voltage

Figure III.6 shows our VCO's frequency transfer characteristic. Note that the ring inverter devices were sized to achieve a VCO center frequency of 1.06 GHz, with a operating range of 800 MHz to 1200 MHz.

III-D. Phase Frequency Detector

The PFD of our design is shown in Figure III.7. It consists of two hardened D flip-flops, whose clock signals are connected to the reference clock *ref_clk* and the divided VCO output *div_clk*. Note that the *div_clk* signal is a split output signal, driven by the frequency divider. The split *D* signals (*DP* and *DN*) of each hardened flip-flop are connected to *VDD*. If the *ref_clk* signal leads the *div_clkp* and *div_clkn* signals, then the signals *speedupp* and *speedupn* rise. When the *div_clkp* and *div_clkn* signals rise, then *slowdownp* and *slowdownn* rise, causing both the hardened flip-flops to reset. Therefore, in this case, the width of the *speedupp* and *speedupn* signals is larger than that of the *slowdownp* and *slowdownn* signals (by an amount which is proportional to the amount by which the *ref_clk* leads the *div_clkp* and *div_clkn* signals). A similar discussion applies for the case when the *ref_clk* signal lags the *div_clkp* and *div_clkn* signals.

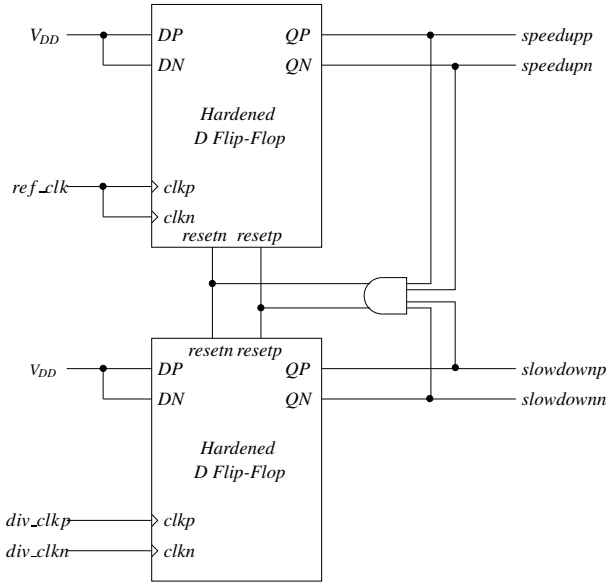


Fig. III.7. Phase frequency detector

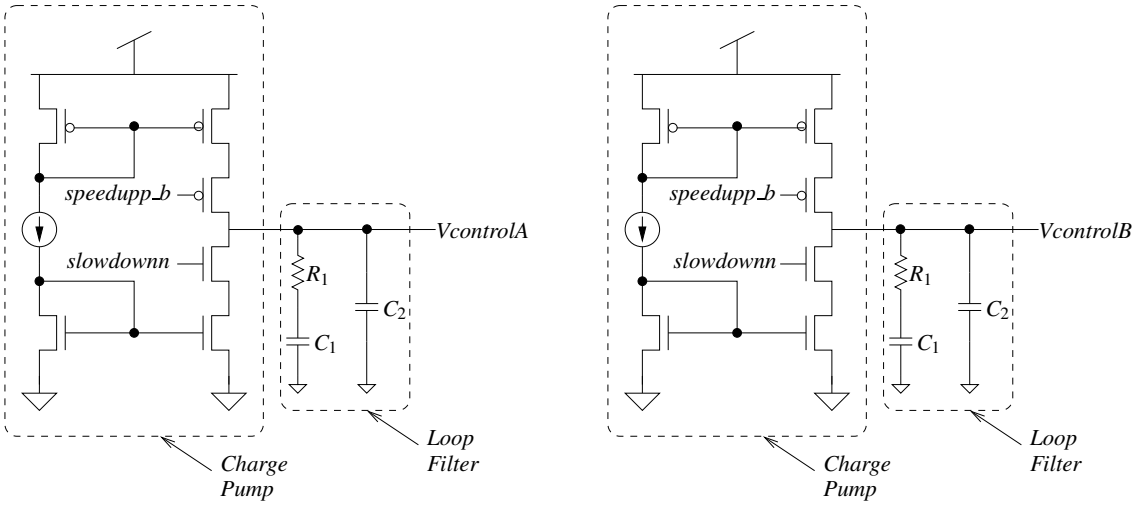


Fig. III.8. Charge pump and low pass filter

## III-E. Charge Pump

Our PLL uses two traditional charge pumps to improve radiation immunity. The outputs of the two charge pumps are labeled as *VcontrolA* and *VcontrolB*, as shown in Figure III.8. In contrast to a traditional charge pump, the input *speedupp_b* (*slowdownn*) of a charge pump is connected to only PMOS (NMOS) devices. Both *speedupp_b* and *slowdownn* signals are driven by a hardened phase frequency detector which has been implemented in a split output manner. The hardened PFD produces two copies of *speedup* and *slowdown* signals - (*speedupp*, *speedupn*) and (*slowdownp*, *slowdownn*). We use a split output inverter (with inputs *speedupp* and *speedupn*) to produce outputs *speedupp_b* and *speedupn_b*. We use the *speedupp_b* signal to drive the PMOS device of the charge pump. This is due to the fact that a radiation particle strike on the *speedupp_b* signal results only in positive glitch, and as a result, a glitch at the *speedupp_b* node will not affect the voltage of the charge pump output nodes *VcontrolA* or *VcontrolB*. For a similar reason, we used the *slowdownn* signal to drive the NMOS devices of charge pumps.

The advantage of using two charge pumps is that if a radiation particle strikes the output node of the charge pump *VcontrolA*, it will affect only those current starved transistors of the ring inverters which are driven by *VcontrolA*. In this scenario, the current starved transistors which are driven by *VcontrolB* will help to reduce the effect of the radiation strike. The other significant advantage of using two charge pumps is that it makes our PLL more robust to process variations. In advanced technologies, process variations have become a severe issue. Analog circuits such as PLLs are most sensitive to process variations. Since the charge pump is one of the most crucial analog blocks in a PLL, device variations in its transistors can lead to significant jitter. We could have used a single charge pump with a large filter capacitor, thereby making the *Vcontrol* node radiation tolerant. However, when considering process variations and device mismatch, such a design would nominally introduce a larger jitter in the VCO clock. A two charge pump design reduces jitter by compensating device mismatch and process variations of one charge pump through the other, when they interact with the cross coupled ring oscillators of the VCO.

A discussion on the loop filter and the selection of the resistor and capacitor values for this block is presented in subsection III-G.

### III-F. Frequency Divider

The frequency divider of our radiation hardened PLL is shown in Figure III.9. Conceptually it is a simple 5-bit synchronous counter, except that all the gates and flip-flops used in its implementation are based on the radiation hardened split-output standard cells described in subsection III-B. Note that the *DP/DN* inputs of all of the flip-flops are driven by a 15X inverter. The hardened flip-flop does not ensure correct functionality if a glitch is introduced by a radiation particle during setup or hold time window of the flip-flop. The flip-flop can go into a metastable state if a glitch appears at the *DP/DN* inputs during the

setup or hold time window. In order to avoid this, we have buffered the *DP/DP* inputs of all of the flip-flops used in our divider. This is not an issue for the flip-flops used in the PFD, because the *DP/DN* inputs of the hardened flip-flops of the PFD are connected to *VDD*.

The outputs of the frequency divider are the signals *div_clkp* and *div_clkn*. Since the center frequency of our PLL is 1.06 GHz, the frequency of the divided clock is about 33 MHz. This is also the frequency of the reference clock (*ref_clk*) in our simulations. A frequency of about 33MHz is easily realized using crystal oscillators, and is commonly used as the external reference clock frequency in modern VLSI systems. We tested our radiation hardened divider and found that it can operate at a maximum frequency of 2GHz in stand-alone operation.

### III-G. System Level Considerations

The loop filter in our PLL consists of resistor $R_1$ and capacitors $C_1$ and $C_2$. Since this is a second order filter, the PLL is therefore a third order system. If we only used a capacitor at the charge pump output, this would result in an open loop transfer function of second order, with both poles located at the origin. This would result in an unstable system, since each pole causes a phase shift of 90°, resulting in 180° phase shift before the unity gain crossover frequency, thereby causing the system to oscillate. Hence we introduce a zero in the loop gain by adding a resistor $R_1$ in series with the loop filter capacitance $C_1$. This stabilizes the system. In this situation, the series combination of $R_1$ and $C_1$ could result in a significant ripple in the voltage of *VControl*. Hence an additional capacitance $C_2$ was added for ripple suppression. We next discuss how we chose the values of $R_1$, $C_1$ and $C_2$.

The set of equations that can be derived for maintaining a particular phase margin to ensure stability are:

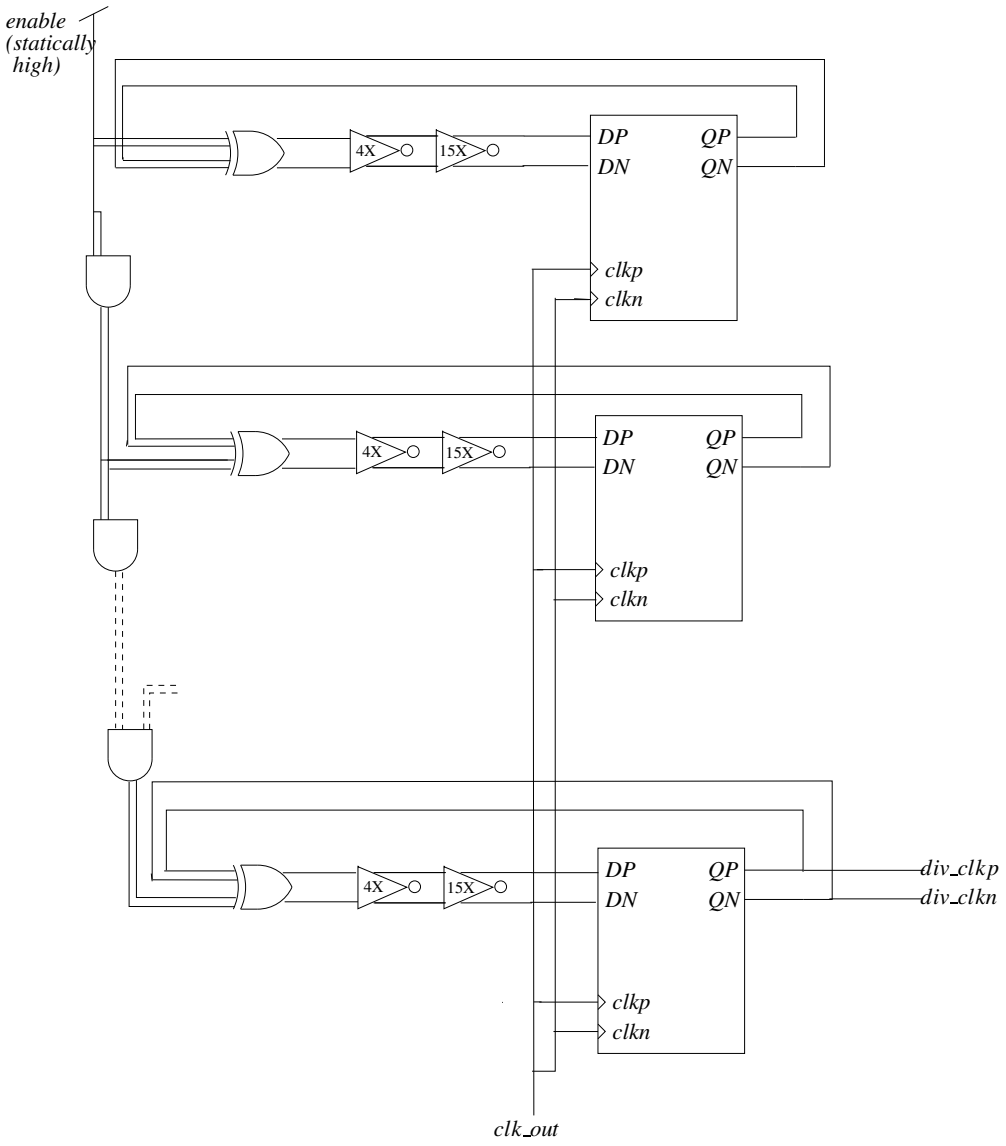


Fig. III.9. Frequency divider

$$PM = atan(\sqrt{b+1}) - atan(\frac{1}{\sqrt{b+1}}) \tag{3.1}$$

where

$$b = C_1/C_2 \tag{3.2}$$

Also, if

$$\omega_c = \frac{\sqrt{b+1}}{R_1 C_1} \tag{3.3}$$

then

$$C_1 = \frac{I}{2\pi}\frac{K_0}{N}\frac{b}{\sqrt{b+1}}\frac{1}{\omega_c^2} \tag{3.4}$$

In the above set of equations $\omega_c$ is the loop bandwidth, $K_0$ is the VCO gain, $I$ is the charge pump current, and $N$ is the ratio of the frequency of *clk_out* to *div_clk*, which is 32 in our system. We used $\omega_c$ = 586 KHz ($\sim \frac{1}{20}^{th}$ of the reference frequency). The phase margin $PM$ was chosen to be 60°. The value of $K_0$ is nominally 1200 MHz/V. Choosing the value of $I$ to be 150 $\mu$A we end up with three equations in three unknowns ($R_1$, $C_1$ and $C_2$). Solving these equations yields the values of $R_1$, $C_1$ and $C_2$ as 4.5 $K\Omega$, 200 pF and 20 pF respectively.

We implemented a linear model of our PLL using MATLAB Simulink to verify the stability of the system. The model is graphically shown in Figure III.10. Note that the PLL is described with a linear model if the PLL is operating within the lock range. The linear model is not valid for the other regions of operation because of the non-linearity of the PLL. The loop bandwidth and phase margin is verified with this linear model as shown in III.11. The waveform of the control voltage *Vcontrol* is shown in Figure III.12. The voltage of the *Vcontrol* node settles to 0.64V after locking, which matches our HSPICE simulations with an error of 0.47%. The reason for this mismatch is that our VCO characteristic is not linear in the operating range of 0.8GHz to 1.2GHz, as shown in Figure III.6.

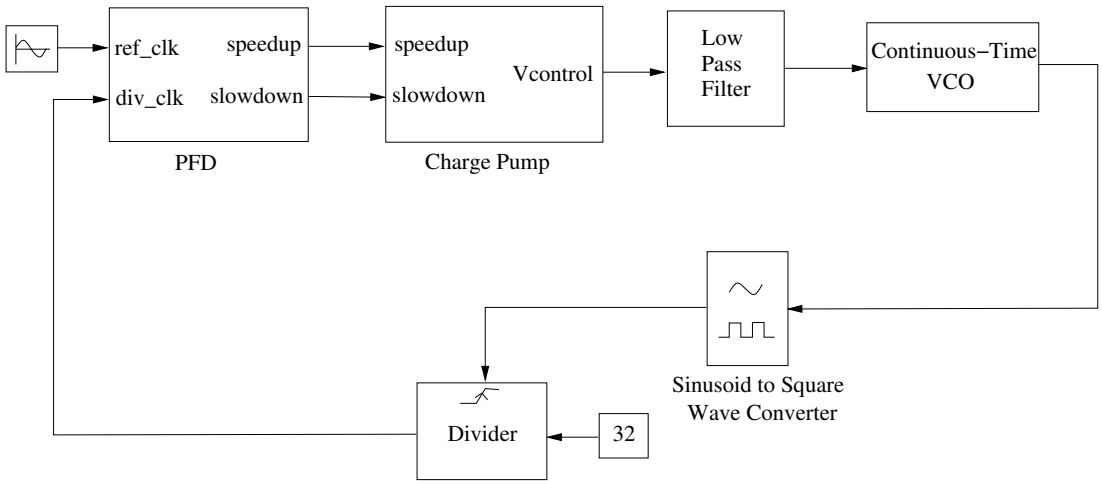


Fig. III.10. MATLAB simulink based linear model of our PLL

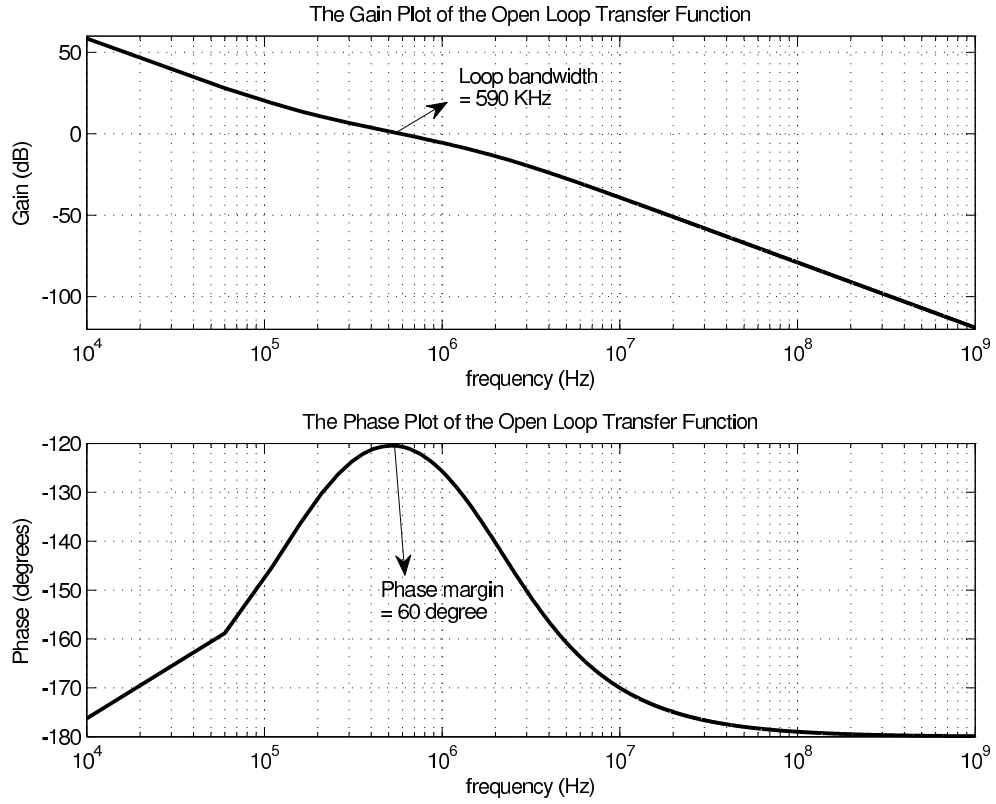


Fig. III.11. Frequency response of the PLL

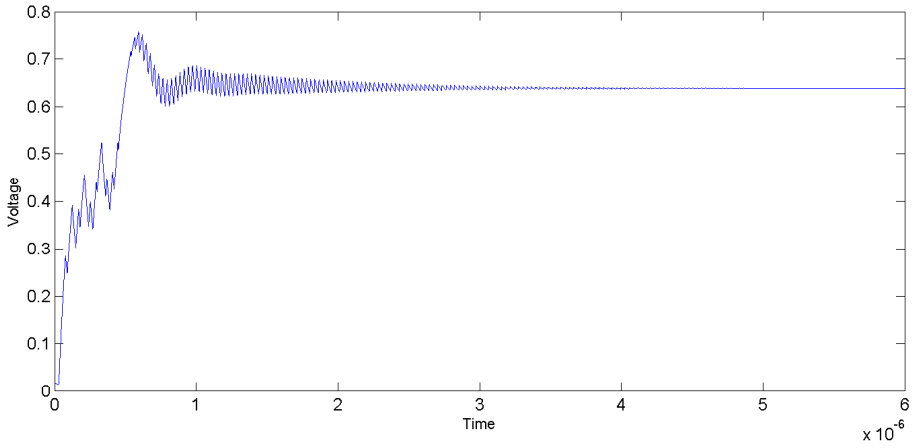


Fig. III.12. *Vcontrol* waveform

# CHAPTER IV

## EXPERIMENTAL RESULTS

To evaluate the performance of our hardened PLL, we conducted several circuit level simulations. We verified the locking capability of our PLL, and also conducted simulations of radiation strikes on all the nodes (modulo electrical symmetry) of the PLL. All simulations were conducted in HSPICE, using 65nm PTM [32] model cards, with VDD = 1.1V. The reference clock frequency was 33.3 MHz. Since the output clock is divided by 32 in our PLL, the nominal operating frequency of our PLL was 1.06 GHz. Our VCO was tuned to operate in the range of 800 MHz through 1200 MHz, with a center frequency of 1060 MHz.

As discussed earlier, the individual components of our radiation hardened PLL were first individually tested for radiation hardness. For all our radiation hardening tests, we utilized the double exponential current pulse of Equation 1.1 to model the radiation strike. For all our radiation strikes, we utilized $\tau_\alpha = 150ps$ and $\tau_\beta = 38ps$, which are reasonable numbers for a 65nm process [4]. Also, we used a value of $Q$ 250fC.

Our experiments consisted of first starting up the PLL and waiting for it to reach a locked condition. At this point, we collected 1000 cycles of statistics on the *clk_out* signal. We computed the clock period of the *clk_out* signal for each of these cycles. Let $T_{max}$ be the maximum period, and $T_{min}$ be the minimum period of *clk_out* over these 1000 cycles. From this information, we computed the worst case jitter of the PLL under a radiation-free locked condition as follows, where $T$ = 938ps is the nominal period of the PLL.

$$jitter = \frac{T_{max} - T_{min}}{T} \tag{4.1}$$

Figure IV.1 illustrates the waveform of the *VcontrolA* node as locking is accomplished

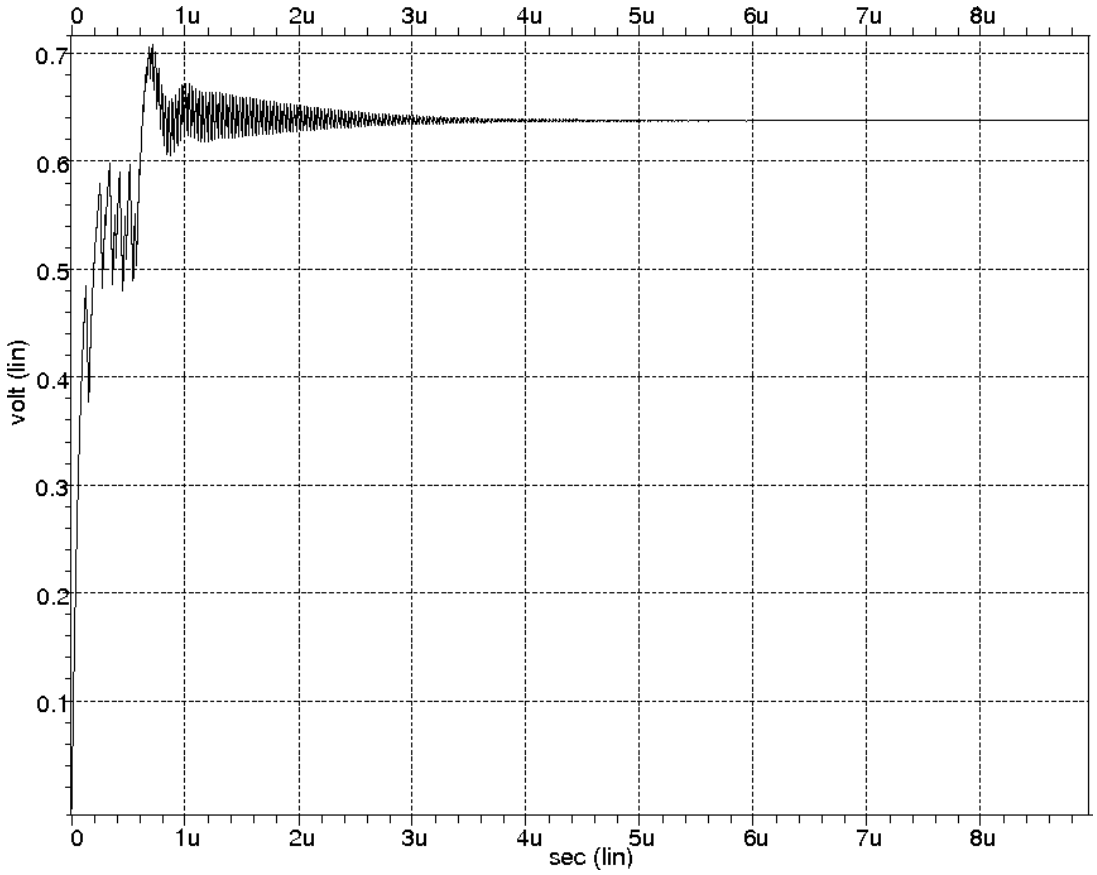


Fig. IV.1. Waveform of *VcontrolA* during lock condition

by our PLL. The locking time of our PLL is 150 reference clock cycles. We define the locking time as the time after which the clock period is within 5% of the nominal period of 938ps. We found the power of our PLL (under a radiation-free locked condition) to be 0.75 mW. The worst jitter of our PLL under a radiation-free locked condition is 0.70%.

To evaluate the performance of our PLL under radiation particle strikes, we struck each node of the PLL (modulo electrical symmetry) at 10 equally separated points in a reference clock cycle. The effect of a radiation particle strike at the same node will be different at different time instants. To explain this, consider a radiation particle strike at the output node of the charge pump at time $t_1$ as shown in the Figure IV.2 . The waveforms

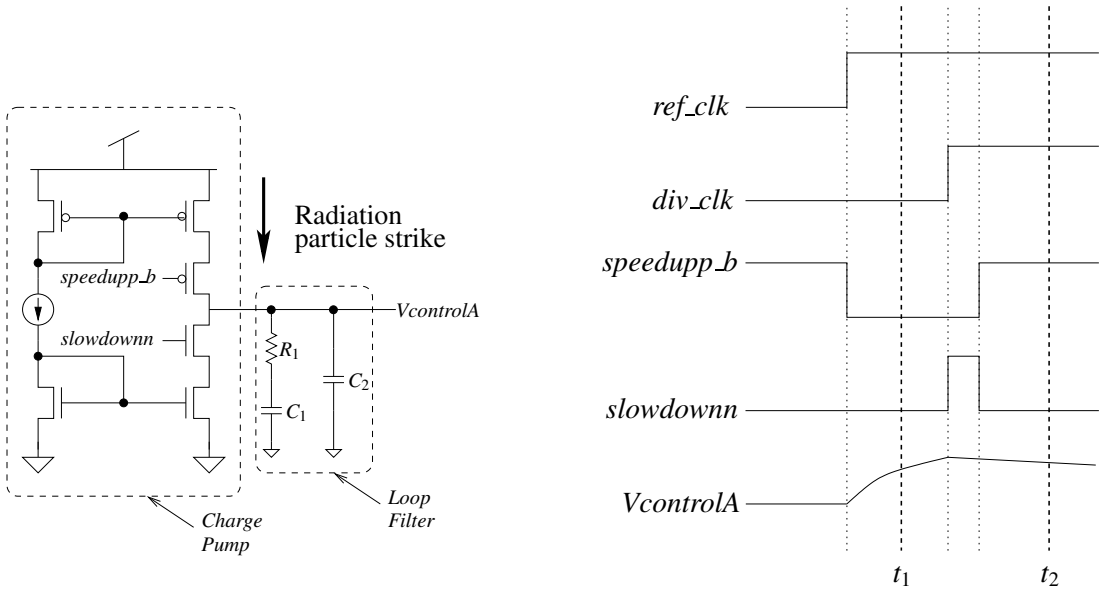


Fig. IV.2. Charge pump with waveforms for the case when *div_clk* is lagging *ref_clk*

shown are for the case when *div_clk* is lagging *ref_clk*. At time $t_1$, the pullup network of the charge pump is ON and the pulldown network is OFF, since the *speedupp_b* and *slowdownn* signals both are zero. The pullup network will try to recover from a radiation particle strike at the charge pump output node *VcontrolA*. However, if the same node is struck at time $t_2$, the effect of the radiation strike will be different from the previous case because both the pullup and pulldown networks of the charge pump are OFF at time $t_2$. Therefore, the effect of a radiation particle strike on the same node will be different at different time instants. For this reason, we struck each node of our PLL at 10 different equally spaced time instants within a reference clock cycle. We collected clock period data for 1000 VCO clock cycles after each strike, to calculate the radiation induced jitter using Equation 4.1, and also the number of cycles to regain lock after the radiation particle strike.

In order to reduce simulation time we pruned electrically symmetrical nodes in our design. For example, the two charge pumps of our design are identical. Therefore, it is

Table IV.1. Jitter and relock time statistics for our PLL

| Category | No. of nodes | No. of strikes | $T_{max}$ (ps) | $T_{min}$ (ps) | % Jitter | Maximum cycles to relock |
|---|---|---|---|---|---|---|
| VCO | 36 | 520 | 1266.20 | 915.85 | 37.39 | 2 |
| PFD | 40 | 540 | 945.04 | 935.49 | 1.01 | 0 |
| CP | 5 | 60 | 940.37 | 934.29 | 0.65 | 0 |
| Divider | 75 | 1050 | 943.47 | 927.43 | 1.71 | 0 |
| Global Signals | 14 | 150 | 1065.20 | 934.57 | 13.94 | 1 |

sufficient to consider all the nodes of any one charge pump for radiation strikes. Table IV.1 summarizes the effect of radiation particle strikes on our PLL. We grouped all the nodes of our PLL into five categories based on the blocks that each node belongs to. The categories are VCO, PFD, CP, Divider and Global Signals. The second column of Table IV.1 reports the number of nodes in the corresponding category, while the third column lists the total number of radiation strikes. Note that if a category has $n$ nodes, the total number of strikes are greater than or equal to $10n$, but less than or equal to $20n$, since some of the $n$ nodes might not be connected to both PMOS and NMOS devices. Nodes which are driven by both PMOS and NMOS device are struck twice - once with a positive glitch and and also with a negative glitch. Therefore, the total number of strikes for any category will be equal to $((n-m)+2m)\times 10$, where $m$ is the number of nodes which are connected to both PMOS and NMOS devices. Column 4 of Table IV.1 reports $T_{max}$, while Column 5 reports $T_{min}$, over 1000 VCO cycles after a radiation strike. The maximum percentage jitter over all nodes in any category (computed as shown in Equation 4.1 above) is listed in Column 6. The last column of Table IV.1 reports the relocking time of our PLL. The relock time is defined as the number of VCO cycles required for the PLL's frequency to return within 5% of its nominal value after a radiation particle strike. Note that for any category, the $T_{max}$ and $T_{min}$ values listed correspond to the maximum and minimum clock periods (over 1000 VCO cycles following the strike) of the node that results in the largest jitter for that category.

Table IV.2. Jitter and relock time statistics for our PLL when charge pump nodes are stuck

| Strike Number | Node name | Glitch type | $T_{max}$ (ps) | $T_{min}$ (ps) | % Jitter | Maximum cycles to relock |
|---|---|---|---|---|---|---|
| 1 | xpump1.gaten | DOWN | 940.03 | 934.46 | 0.61 | 0 |
| | xpump1.gatep | UP | 940.30 | 934.40 | 0.63 | 0 |
| | xpump1.intn | DOWN | 940.42 | 934.74 | 0.61 | 0 |
| | xpump1.intp | UP | 940.27 | 935.23 | 0.54 | 0 |
| | VcontrolA | UP | 939.82 | 935.15 | 0.50 | 0 |
| | VcontrolA | DOWN | 940.04 | 935.12 | 0.53 | 0 |
| 2 | xpump1.gaten | DOWN | 939.88 | 935.31 | 0.49 | 0 |
| | xpump1.gatep | UP | 939.82 | 935.34 | 0.48 | 0 |
| | xpump1.intn | DOWN | 940.37 | 934.29 | 0.65 | 0 |
| | xpump1.intp | UP | 939.86 | 934.36 | 0.59 | 0 |
| | VcontrolA | UP | 939.83 | 935.23 | 0.49 | 0 |
| | VcontrolA | DOWN | 940.09 | 934.40 | 0.61 | 0 |
| 3 | xpump1.gaten | DOWN | 939.88 | 934.95 | 0.53 | 0 |
| | xpump1.gatep | UP | 940.02 | 934.36 | 0.60 | 0 |
| | xpump1.intn | DOWN | 939.91 | 934.27 | 0.60 | 0 |
| | xpump1.intp | UP | 940.13 | 935.19 | 0.53 | 0 |
| | VcontrolA | UP | 940.00 | 934.31 | 0.61 | 0 |
| | VcontrolA | DOWN | 939.79 | 934.39 | 0.58 | 0 |
| 4 | xpump1.gaten | DOWN | 939.88 | 935.18 | 0.50 | 0 |
| | xpump1.gatep | UP | 940.01 | 934.39 | 0.60 | 0 |
| | xpump1.intn | DOWN | 940.02 | 935.22 | 0.51 | 0 |
| | xpump1.intp | UP | 940.06 | 935.14 | 0.53 | 0 |
| | VcontrolA | UP | 939.97 | 935.15 | 0.51 | 0 |
| | VcontrolA | DOWN | 939.86 | 934.38 | 0.58 | 0 |
| 5 | xpump1.gaten | DOWN | 940.03 | 934.36 | 0.61 | 0 |
| | xpump1.gatep | UP | 940.30 | 934.40 | 0.63 | 0 |
| | xpump1.intn | DOWN | 940.42 | 934.74 | 0.61 | 0 |
| | xpump1.intp | UP | 940.27 | 935.23 | 0.54 | 0 |
| | VcontrolA | UP | 940.11 | 934.62 | 0.59 | 0 |
| | VcontrolA | DOWN | 939.75 | 934.23 | 0.48 | 0 |
| 6 | xpump1.gaten | DOWN | 939.88 | 935.23 | 0.50 | 0 |
| | xpump1.gatep | UP | 940.00 | 934.40 | 0.60 | 0 |
| | xpump1.intn | DOWN | 939.90 | 934.39 | 0.59 | 0 |
| | xpump1.intp | UP | 939.55 | 935.11 | 0.47 | 0 |
| | VcontrolA | UP | 939.86 | 935.22 | 0.50 | 0 |
| | VcontrolA | DOWN | 939.98 | 934.32 | 0.60 | 0 |
| 7 | xpump1.gaten | DOWN | 939.88 | 935.13 | 0.51 | 0 |
| | xpump1.gatep | UP | 939.79 | 935.40 | 0.47 | 0 |
| | xpump1.intn | DOWN | 939.77 | 935.22 | 0.49 | 0 |
| | xpump1.intp | UP | 940.07 | 934.67 | 0.58 | 0 |
| | VcontrolA | UP | 940.01 | 934.67 | 0.57 | 0 |
| | VcontrolA | DOWN | 939.89 | 934.44 | 0.58 | 0 |
| 8 | xpump1.gaten | DOWN | 940.03 | 935.05 | 0.53 | 0 |
| | xpump1.gatep | UP | 940.27 | 934.30 | 0.64 | 0 |
| | xpump1.intn | DOWN | 939.91 | 935.09 | 0.51 | 0 |
| | xpump1.intp | UP | 940.03 | 934.62 | 0.58 | 0 |
| | VcontrolA | UP | 939.98 | 935.17 | 0.51 | 0 |
| | VcontrolA | DOWN | 939.80 | 934.33 | 0.58 | 0 |
| 9 | xpump1.gaten | DOWN | 939.98 | 934.27 | 0.61 | 0 |
| | xpump1.gatep | UP | 939.82 | 935.05 | 0.51 | 0 |
| | xpump1.intn | DOWN | 940.20 | 935.23 | 0.53 | 0 |
| | xpump1.intp | UP | 940.11 | 934.32 | 0.62 | 0 |
| | VcontrolA | UP | 939.85 | 934.38 | 0.58 | 0 |
| | VcontrolA | DOWN | 940.08 | 934.60 | 0.58 | 0 |

Table IV.2 Continued

| Strike Number | Node name | Glitch type | $T_{max}$ (ps) | $T_{min}$ (ps) | % Jitter | Maximum cycles to relock |
|---|---|---|---|---|---|---|
| 10 | xpump1.gaten | DOWN | 940.17 | 934.89 | 0.56 | 0 |
| | xpump1.gatep | UP | 939.82 | 935.24 | 0.49 | 0 |
| | xpump1.intn | DOWN | 939.84 | 935.17 | 0.50 | 0 |
| | xpump1.intp | UP | 939.80 | 934.66 | 0.55 | 0 |
| | VcontrolA | UP | 939.94 | 934.82 | 0.55 | 0 |
| | VcontrolA | DOWN | 939.57 | 935.22 | 0.46 | 0 |

Detailed results for radiation strikes on all nodes of all category are not presented for the sake of brevity. Instead, we present detailed results for all nodes in the CP category, in Table IV.2. Column 2 of Table IV.2 represents the node names, while Column 3 reports the nature of the glitch due a radiation particle strike. Columns 4 through 7 have the same meaning as in Table IV.1.

From Table IV.1, we observe that strikes on the nodes of the various categories result in different values of jitter. The worst case is when the input *inn_A* or *inn_B* of the ring inverter is struck. This results in a percentage jitter of about 37.4%. A waveform of *clk_out* during this worst case strike is shown in Figure IV.3. Note that the strike occurs at 11.003 $\mu$s, and that frequency lock is lost for only one clock cycle as we see that the first pulse after 11.003 $\mu$s is wider than the remaining pulses. This is a significant improvement over past radiation hardened PLL approaches.

Over all the strikes, our PLL takes just 2 VCO cycles to return to a locked state. Note that in general, the node that results in the maximum jitter is not necessarily the node that takes the largest number of cycles to relock. The main reason for the robustness of our design is that each of the components (down to gates and flip-flops) is designed in a manner that is extremely radiation tolerant. In past approaches [29, 30], the focus was on the hardening the charge pump alone. Our approach has an estimated 105% higher active area than a traditional unhardened PLL. In this estimate, we accounted for the area of the resistors and capacitors of the loop filter. However, the area of a PLL is usually a very small

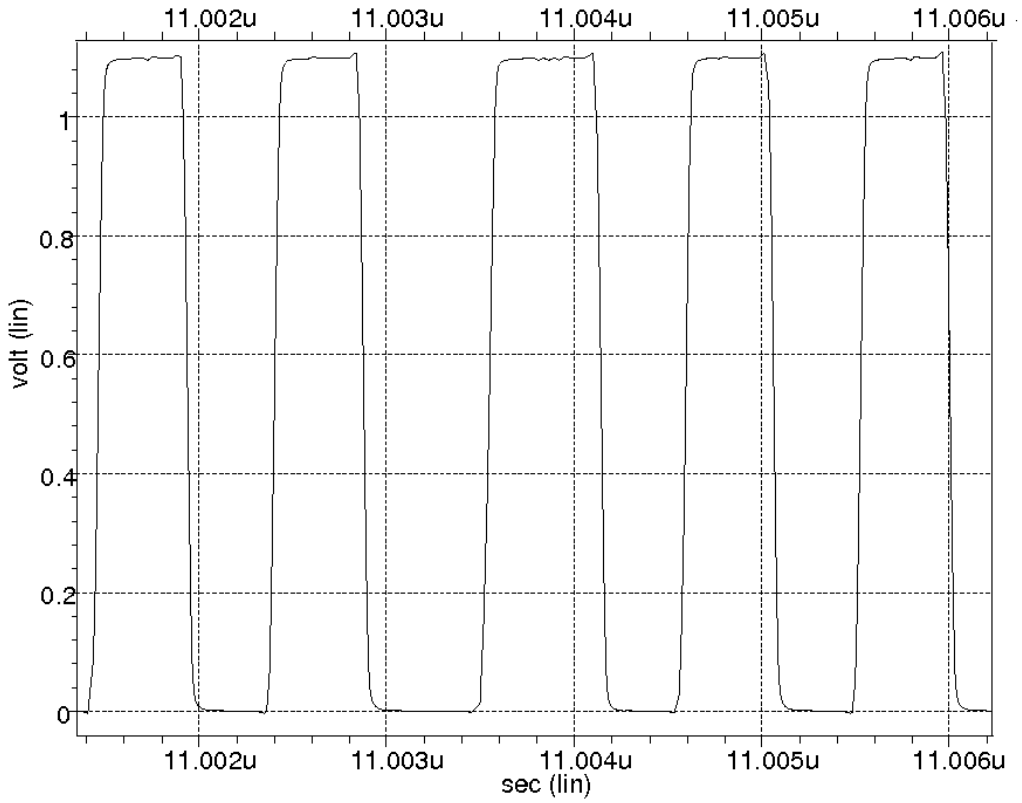


Fig. IV.3. Waveform of *clk_out* during worst strike

portion of the area of an IC, so this increase in area is

In [29], the authors present a hardened PLL operating at 700 MHz. The authors study strikes only on the charge pump output since the goal of their paper is to harden the charge pump alone. No other nodes were struck, and the radiation resilience of the PLL is therefore not conclusively known. The authors observe that a 200 fC strike causes their hardened PLL to require 98ns (68 cycles) to recover lock, with at least one clock pulse being displaced by more than 2Π radians. It was reported in [30] that a radiation particle strike on their proposed hardened PLL (operating at 200 MHz) induced transients which results in a loss of lock for 54 clock cycles.

In contrast, we have performed experiments where we strike each node (modulo electrical symmetry) of our hardened PLL (including the charge pump output). Our simulations are performed in a more radiation susceptible 65nm process (compared to the 130nm process used in [29]). We strike our nodes with a $Q$ value of 250 fC (as compared to 200 fC in [29]). In the worst case, over all these strikes, we find that we return to the locked state after just 2 cycles of the VCO clock. The single disturbed clock pulse exhibits a worst case phase displacement of just 2.35 radians (i.e a worst case jitter of 37.4% of the clock period).

# CHAPTER V

## CONCLUSIONS

With reduced feature sizes, lowered supply voltages and increasing operating frequencies, the radiation tolerance of digital circuits is becoming an increasingly important problem. Radiation hardening techniques have been presented in the literature for combinational as well as sequential logic. However, the radiation tolerance of clock generation circuitry has received scant attention to date. It has been shown that in the deep submicron regime, the clock network contributes significantly to the chip level Soft Error Rate (SER). The on-chip Phase Locked Loop (PLL) is particularly vulnerable to radiation strikes. In this thesis, we present a radiation hardened PLL design. Each component of this design – the voltage controlled oscillator (VCO), the phase frequency detector (PFD) and the loop filter – is designed in a radiation tolerant manner. Our PLL utilizes two VCOs and two charge pumps, configured in such a way that a radiation strike on one is compensated by the other. Whenever possible, the circuit elements used in our PLL exploit the fact that if a gate output is driven using only PMOS (NMOS) transistors, then a radiation particle strike on that output can result only in a logic 0 to 1 (1 to 0) flip. By separating the PMOS and NMOS devices, and splitting the gate output into two signals, extremely high levels of radiation tolerance are obtained. Our PLL is tested for radiation immunity for critical charge values up to 250fC for all possible radiation strikes (modulo electrical symmetry), and it demonstrates a remarkable ability to recover rapidly (within 2 cycles) from the radiation event.

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# VITA

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