ULTRA LOW POWER IEEE 802.15.4/ZIGBEE COMPLIANT TRANSCEIVER

A Dissertation

by

FAISAL ABDEL-LATIF ELSEDDEEK ALI HUSSIEN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2009

Major Subject: Electrical Engineering

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Approved by:

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ABSTRACT

Ultra Low Power IEEE 802.15.4/ZIGBEE Compliant Transceiver.

(December 2009)

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Low power wireless communications is the most demanding request among all wireless users. A battery life that can survive for years without being replaced, makes it realistic to implement many applications where the battery is unreachable (e.g. concrete walls) or expensive to change (e.g underground applications). IEEE 802.15.4/ZIGBEE standard is published to cover low power low cost applications, where the battery life can last for years, because of the 1% duty cycle of operation.

A fully integrated 2.4GHz IEEE802.15.4 compliant transceiver suitable for low power, low cost ZIGBEE applications is implemented. Direct conversion architecture is used in both receiver and transmitter, to achieve the minimum possible power and area. The chip is fabricated in a standard 0.18um CMOS technology. In the transmit mode, the transmitter chain (Modulator to PA) consumes 25mW, while in the receive mode, the

receiver chain (LNA to Demodulator) consumes 5mW. The integer-N frequency synthesizer consumes 8.5mW.

Other low power circuits are reported; A 13.56 passive RFID tag and a low power ADC suitable for built-in-testing applications.

DEDICATION

To my Parents,

To my Wife and Daughter,

To my Brothers and Sisters,

For their Love and Support

ACKNOWLEDGEMENTS

This dissertation does not only hold the results of years of study and research, but also reflects the relationships with many generous and stimulating people. This is the time where I have the opportunity to present my appreciation to all of them.

First, to my advisor, Dr. Edgar Sánchez-Sinencio, I would like to express my sincere gratefulness and appreciation for his excellent guidance, caring, patience, and immense help in planning and executing the work in a timely manner. His great personality and creativity provided me with an excellent atmosphere for work, while his technical insight and experience helped me a lot in my research. His company and support at the time of crisis will always be remembered.

I would like also to thank Dr. José Silva-Martínez who was always there for any research questions, providing precious advice and sharing his time and experience. Thanks also go to my committee members, Dr. Costas Georghiades and Dr. Alexander Parlos, for their valuable comments on my research.

Special thanks and words of appreciation are due to my friend, and ex-roommate Ahmed Emira. I was his roommate during the first year of my PhD studies. He made my arrival in College station a lot smoother than I thought it would be. He was like my family from

home. The same goes for my sincere friend Ahmed Mohieldin who supported me a lot and whom I learned much from our numerous technical discussions. He provided me the emotional support I much needed at first.

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And of course I will always be grateful and never forget the most important of all: my wife, Rania, for her continuous love, patience, support and companionship. Her constant faithfulness, encouragement and understanding enabled me to confront many challenges of the past years.

Finally, I will never find words enough to express the gratitude and appreciation that I owe to my father, Prof. Dr. Abdel-Latif Elseddeek, my great mother, my brothers and sisters. Their tender love and support have always been the cementing force for building the blocks of my career. The all round support rendered by them provided the much needed stimulant to sail through the phases of stress and strain.

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CHAPTER I

INTRODUCTION

1.1 Research Motivation

Low-cost low-power dissipation solutions are the main requirement for wireless applications nowadays. Moreover, many applications such as concrete sensors, smart tags, home applications, and underground tags for blind navigation systems require long battery life, either for difficulties of changing the battery or for being more robust and reliable with entire cost reduction.

In the last decade, multiple standards and systems are initiated to suit such application. IEEE 802.15.4/ZIGBEE, as an example of Wireless Personal Area Networks (WPANs), is one of the main low power standards. It supports low data rates and small range of operation, while its battery lasts more than 10 times Bluetooth battery lifetime. IEEE 802.15.4/ZIGBEE operates less than 1% of its "ON" time (low duty cycle), thus reducing the active power consumption. Also, it has much relaxed electrical specifications that make it easier for analog designers to squeeze the required power for proper operation.

This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits*.

RFID system is another example of low power systems. RFID operates in a master-slave environment. The interrogator (high power unit) acts as the master, while the transponder (low power units) act as slaves. The interrogator sends an RF signal to the surrounding transponders carrying power, commands and data. Each transponder generates its needed power from the incident signal, interprets its commands and sends back the required response. Responding to the interrogator is done by controlling the reflected (backscattered) wave from the transponder antenna. This is done by controlling the antenna matching and is so called “Backscatter modulation”. Transponders depending on the incident signal to operate are defined as “passive transponders”. Other transponders contains batteries necessary for power up, thus reducing the interrogator dependence and increase their read ranges and processing capabilities, and is defined as “active transponders”.

Low power target us extended from wireless applications to other time-cost critical applications such as Integrated circuits production characterization. Production test is one of the main cost-driving steps in any commercial chip. Systems that require complicated and time consuming measurements at production have higher cost compared to competing systems that have simpler production tests. Built-in testing emerges to reduce the test cost. Fully built-in testing leads to less complicated and much faster test procedure. The main challenges of such systems are; (1) silicon area used for the overhead circuitry that controls the die cost, (2) power consumption that controls the

test cost. Different standards suggest proper ways for built-in testing techniques such as IEEE 1149.4 test standard.

1.2 Dissertation Overview

Chapter II introduces a brief summary of short range wireless communications, followed by a description of IEEE 802.15.4/ZIGBEE as a Low Rate Wireless Personal Area Network (LR-WPAN). An overview of IEEE 802.15.4/ZIGBEE is covered illustrating targeted applications, frequency bands, spreading and modulation format, sensitivity requirements, dynamic range, required transmit power, power spectral density mask, and required Error Vector Magnitude (EVM). Coexistence with other IEEE standards is discussed as viewed by IEEE 802.15.4/ZIGBEE standard. A comparison between different wireless standards concludes Chapter II.

As a step towards implementing a fully integrated IEEE 802.15.4/ZIGBEE transceiver, Chapter III introduces different possible architectures mentioning the pros and cons of each architecture. A direct conversion system is chosen, where complete transceiver systems design is performed, obtaining different blocks' specifications and expected non-idealities.

Chapter IV discusses the circuit level design of the transceiver. Each building block is covered showing the design parameters trade-offs and design considerations for each

block. Circuit design performed starting from the system specifications down to the circuit metrics. The analysis includes the receiver front end (LNA and down-conversion mixer), a third order Butterworth LPF, VGA, and O-QPSK demodulator. On the other hand, the transmitter front end (PA and up-conversion mixer) is introduced followed by O-QPSK modulator and frequency synthesizer. Chapter IV is concluded with experimental results for the full transceiver chain as well as individual building blocks.

Chapter V covers RFID systems, defining both elements of the system; Interrogator and Transponder. A complete system design methodology is illustrated for a passive RFID system. A 13.56MHz passive RFID tag is taken as a design example, where system design is performed to derive building block specifications. Circuit design for the most critical blocks is shown with trade-offs and design considerations. Measurements and post-layout results are presented.

For built-in testing applications, Chapter VI proposes a magnitude and phase on chip characterization. It sweeps the input frequency of the Circuit Under test (CUT) and calculates its magnitude and phase response for each frequency step. The output is digitized and serially taken to save area and number of pads used for testing. An ultra low power 7-bit ADC is designed to be used in the proposed system. A complete discussion is provided for the idea and the circuit design. Full measurements of the characterization system and separate measurements for the ADC are provided to conclude Chapter VI.

CHAPTER II

SHORT-RANGE COMMUNICATION STANDARD:

IEEE 802.15.4/ZIGBEE

2.1 Short Range Wireless Communications

Recently, wireless data transfer invaded all applications in our life. The need for mobile, efficient, and connected device proved its importance in many fields; wireless internet services at cafes or airports, industry management, tagging, data show devices and Machine to Machine (M2M) systems. Short range of operation (<100m) is a common requirement in such applications. Each application has its own specifications as data throughput, power consumption, and range of operation; this identifies the preferred frequency band, the required BW, and the transmitted power.

Due to the limited available Bandwidth (BW), and the fear of destructive interference between different transmitted data that can destroy both, regulations have been established for each region (Europe, Japan, Canada, and USA). These regulations specify the permissible frequency bands that can be used for customized applications, the maximum allowable transmitted power for each frequency, and the restricted bands. This facilitates the coexistence of two or more applications within the same neighborhood.

Short range wireless communication standards has been developed in the last decade to cover all possible short range applications. In 1997, IEEE releases the original Wireless Local Area Network (WLANs) 802.11, to achieve 2 Mbps data rate.

Nowadays, 802.11b with an 11Mbps and 802.11a with a 54Mbps are more popular [1]. These standards has large data rate making them suitable for many applications. After all, WLANs are optimized for portable computing devices as notebook computers [2]. These portable devices are mostly used at fixed places and powered using mains supply.

Recently more applications targeting lower power, shorter range of operation (<10m), and even lower data rate arise. Wireless Personal Area Networks (WPANs) starts to evolve to cover these applications that use mobile devices operating on batteries. Figure 2.1 shows the chart of short range wireless communications.

IEEE 802.15.1 (Bluetooth) is first released and optimized for low power consumption and low cost devices. In November 1999, and even before the Bluetooth standard was completed [2]. Several companies found the need of wireless standard for digital cameras and multimedia traffic that requires high data rate. Thus the High Rate Wireless Personal Area Networks (HR-WPANs) IEEE 802.15.3 started to develop.

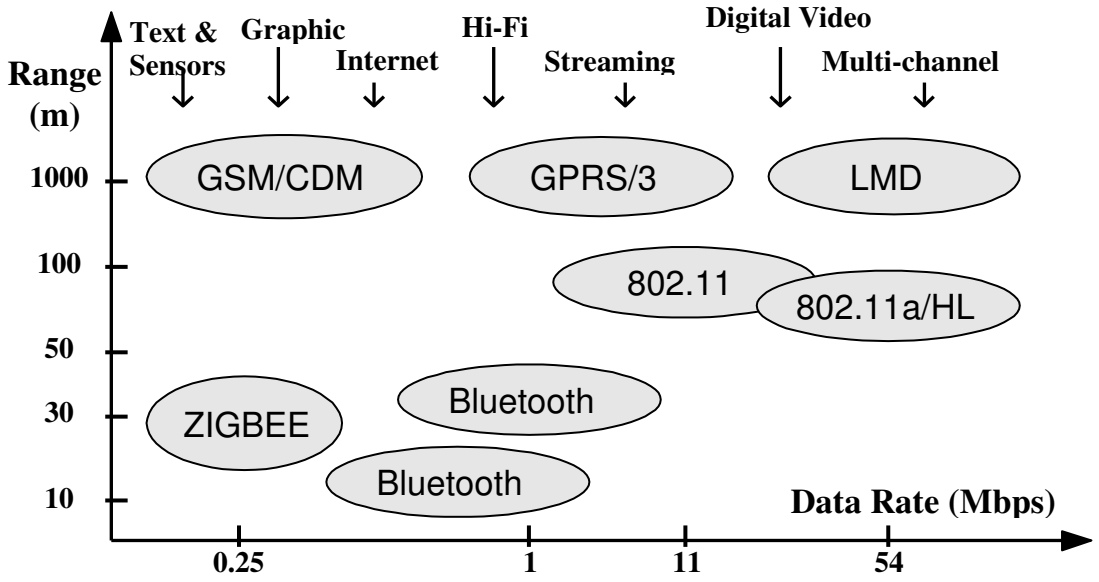


Figure 2.1 Short Range Wireless Communications Chart

Even more, some other applications as sensors, smart tags, and home applications require ultra low power consumption and ultra low cost. Bluetooth and IEEE 802.15.3 are not suitable for such applications. IEEE 802.15.4 (WPAN-LR) started by the end of 2000 to meet those applications' requirements till it is completely released by 2003.

2.2 IEEE 802.15.4/ZIGBEE Standard Definition

The IEEE 802.15.4 is a LR-WPAN standard optimized for low data rate and low power applications. As shown in Figure 2.2 It defines the Physical layer (PHY) and Media Access Control layer (MAC). PHY layer describes low level network functions such as: data spreading, bits transmission, and reception complying with the air interface requirements. On the other hand, MAC layer assembles data packets and determines data destination in transmission mode, while it determines the source of transmission and

decomposes the received frames in reception mode. It also provides channel access control and run channel multiple access protocols. The upper network layers are defined by ZIGBEE [3]; the routing protocol designed to run over 802.15.4 and supported by the ZIGBEE Alliance. It consists of a set of layers performing the link between the application layer run by the user and the MAC layer. ZIGBEE layer interprets software commands and passes the new set of commands to MAC layer. Also, it implements higher network functions such as: starting a network, adding or removing devices from existing network, and route discovery and storing routing table.

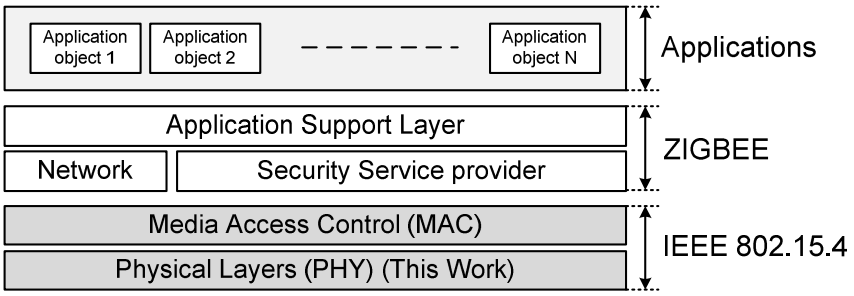


Figure 2.2 ZIGBEE Protocol Stack

The battery life can be extended by reducing the power consumption of the devices in operation. For a transceiver in operation, the average power consumption is the weighted sum of its active and inactive power consumption, as shown in equation (2.1). The active power is the power consumed while transmitting or receiving data (during Power-On), while the inactive power is the consumed power in the standby mode (during Power-Off). The *duty cycle* is defined to be the time percentage in a transmission session where the device is active.

$$Average\ Power\ Consumption = \\ [Active\ Power * Duty\ Cycle] + [Inactive\ Power * (1 - Duty\ Cycle)] \quad (2.1)$$

Reducing the duty cycle, will decrease the average consumed power significantly. IEEE 802.15.4 is tailored to operate at a very low duty cycle (less than 1%). This is achieved by reducing the peak power transmission duration (network beacon packet) relative to the steady state allowed transmitted power duration (superframe period, time between beacons) [3].

IEEE 802.15.4 network can be peer-to-peer or star network, as shown in Figure 2.3 [3], depending on the targeted application requirements. Two main devices used to build up the ZIGBEE network; Full Functional Device (FFD) and Reduced Functional Device (RFD). FFD has the complete set of MAC services which allow it to work as a Personal Area Network (PAN) coordinator. An example of MAC services to be performed by the FFD is to perform Energy Detection (ED) and active scans, starting a new Personal Area Network (PAN), and setting its address. On the other hand, RFD has a reduced set of services and is intended to be used in simple applications with simpler data manipulations. RFD uses lower resources as well as low memory capacity.

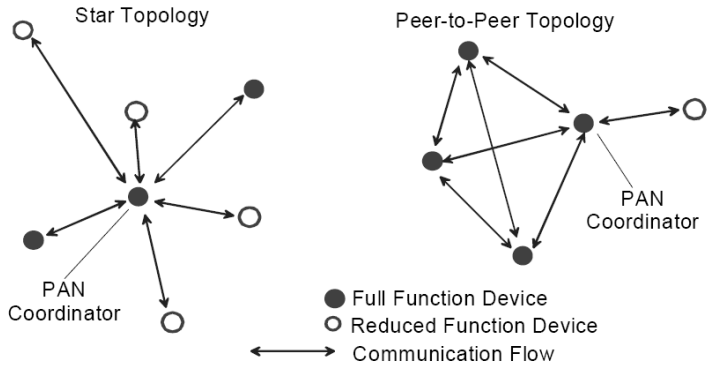


Figure 2.3 Star and Peer-to-Peer Topologies

Address structures used by the LR-WPAN supports either 16-bit short or 64-bit extended addresses to allow thousands of nodes to join the expandable network with the same infrastructure. This emphasizes the low cost expectation of each individual node and guarantees less hardware resources implementations

The IEEE802.15.4 standard can support data rates of 20 Kbps, 40 Kbps, and 250 Kbps. It also uses Direct Sequence Spread Spectrum (DSSS) as one of the techniques of increasing the signal BandWidth (BW) to gain a lower Bit Error Rate (BER) for the same received Signal-to-Noise (SNR) ratio, as shown in Chapter III. Other techniques of spectrum spreading such as Frequency Hopping Spread Spectrum (FHSS) are avoided, since the DSSS has higher interference immunity and allows more networks per unit area. Moreover, DSSS is more power-efficient requiring less transmit-power than FHSS, thus more efficient in Power Amplifier (PA) utilization usage especially for data rates up to 1MHz [4].

Other techniques such as, fully acknowledged protocol, Energy Detection (ED) and Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA) are chosen to increase the data transfer reliability and reduce the session time and thus the power consumption.

Data Encryption is also added as a security service, where a symmetric key is used to encrypt the transmitted data and to avoid being read by other unauthorized parties.

2.2.1 ZIGBEE Applications

Any Low Data Rate application that requires energy management and efficiency, and matches the RF characteristics of the IEEE 802.15.4, can perfectly use ZIGBEE standard. This spans a wide range of applications in many fields. In the Industrial fields; monitors, sensors and production chain automation as in pulp and paper industry [5]. Also, Environmental control [6], Building Automation [7], Intelligent transportation systems [8], Remote controls for TVs and DVDs, mouse, keyboards and home security and networking applications [9] can use the IEEE 802.15.4/ZIGBEE. Health care is a fast growing field in the wireless communications and ZIGBEE is an optimum standard for many of its applications [10, 11]. Figure 2.4 summarizes the most important applications that uses IEEE 802.15.4/ZIGBEE standard. All these applications can work on the 2.4GHz Industrial, Scientific and Medical (ISM) band. Some of them may require multichannel access, which is also supported by ZIGBEE, as in home security,

simultaneous PC peripherals and sensor arrays, while others can work on a single channel as remote control devices. Moreover, various bit rate supported by ZIGBEE, 20kbps to 250kbps, is sufficient for such applications.

2.2.2 Frequency Bands

IEEE 802.15.4 covers three different frequency bands [3]. The first band is at 868 MHz and it has only one channel with 20 kbps bit rate using BPSK modulation scheme. This band is supported in Europe only. The second band is at 915 MHz, it has 10 channels, each with a 40 kbps using BPSK modulation scheme. This band is supported in North America, Australia, New Zealand, and some countries in South America only [10]. The third frequency band is located at 2.4 GHz where it has 16 channels running at 250 Kbps each. This band uses OQPSK with half sine wave shaping as its modulation scheme. This results in a Minimum Shift Keying (MSK) signal. This band is supported almost worldwide since its unlicensed frequency allocation is available.

An IEEE 802.15.4/ZIGBEE compliant receiver should cover either the first two bands (868 MHz and 915 MHz) or the third band (2.4GHz). Figure 2.5 shows the frequency bands allocations for IEEE 802.15.4. Channel numbering follow the nomenclature specified in Table 2.1.

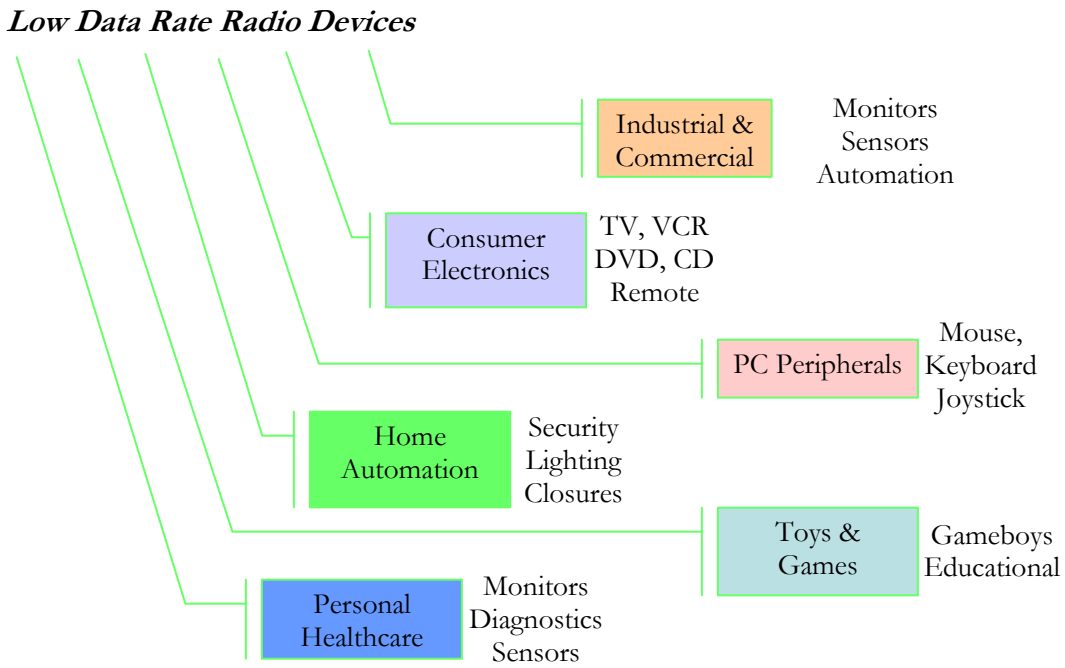


Figure 2.4 IEEE 802.15.4/ZIGBEE Standard Applications

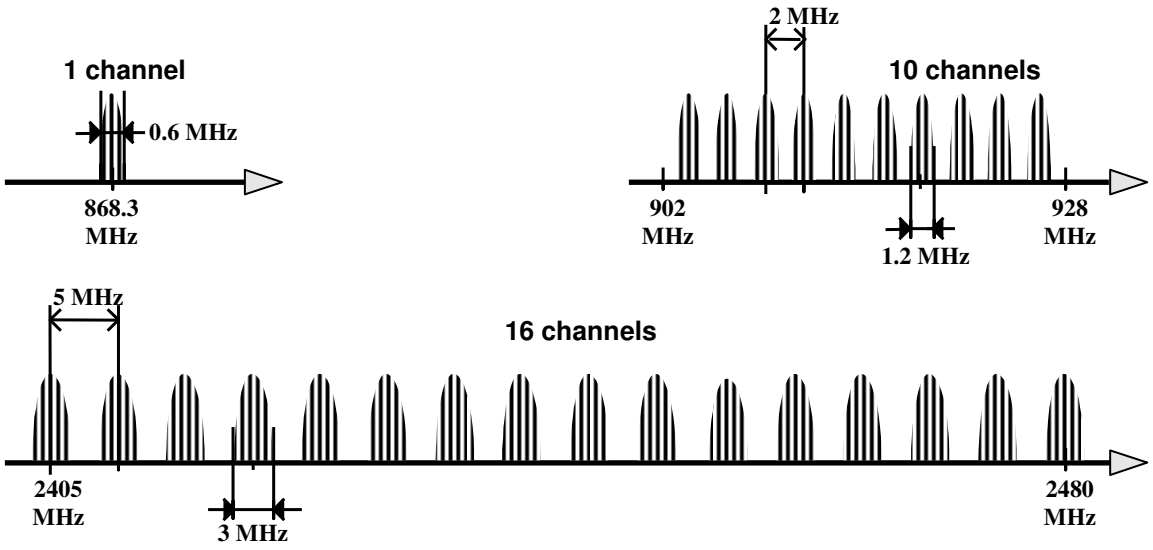


Figure 2.5 IEEE 802.15.4/ZIGBEE Frequency Bands

Table 2.1 Channel Numbering Nomenclature [3]

Band	*Channel center Frequency*	*Channel number*	*Channel Spacing*
868 MHz	868.3 MHz	K = 0	0
915 MHz	906+2(k-1) MHz	K = 1, 2, 3, …, 10	2 MHz
2400 MHz	2405+5(k-1) MHz	K = 11, 12, 13, …, 26	5 MHz

The 2.4 GHz band is covered through out this work, since it is used worldwide and it represents the highest challenge in terms of power consumption.

2.2.3 Spreading and Modulation Format

For the 2.4 GHz band, the modulation scheme used is OQPSK with sine wave shaping followed by DSSS to improve the BER for a given SNR at the receiver side.

OQPSK with half sine wave shaping reduces to a Minimum Shift Keying (MSK) signal. MSK signal has a continuous phase and a constant envelope which relaxes the Power Amplifier (PA) specifications as shown in Chapter V. Also, MSK Power Spectral Density (PSD) has a minimum side lobes power to inherently overcome interference effects. The serial data bits are grouped into symbols (4 bits each). Each symbol is mapped into a nearly orthogonal 32-chip Pseudo-random Noise (PN) sequence as specified in Table 2.2 [3], this converts a 250Kbps data rate signal to a 2 MChip/sec chip rate sequences to achieve a Processing Gain (PG) of 9dB. For the same BER, DSSS relaxes the required SNR by the processing gain. Thus the SNR-BER curve is shifted by

9dB to the left, improving the sensitivity by 9dB. The PN sequences are derived from each others using cyclic shifts and/or conjunction. This acquires the sequence many features to reduce the BER as shown in Chapter III.

Table 2.2 Symbol to Chip Mapping

Symbol		Chip PN Sequences
Decimal	Binary	
0	0000	1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1	1000	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
2	0100	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
3	1100	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
4	0010	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
5	1010	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
6	0110	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
7	1110	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
8	0001	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1
9	1001	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1
10	0101	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1
11	1101	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
12	0011	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
13	1011	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
14	0111	1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
15	1111	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0

After being created, the chips are split into I and Q branches, where even-numbered chips goes to the I branch while odd-numbered chips goes to the Q branch. Then, the Q branch encounters a delay of 1 Chip duration (0.5 μsec), as shown in Figure 2.6 [3].

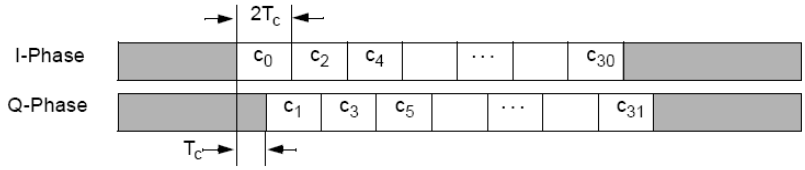


Figure 2.6 OQPSK Chip Stream

Pulse shaping is performed on both branches, where each chip takes a half sine wave shape instead of the square wave nature, as shown in Figure 2.7 [3]. By upconverting the two branches using quadrature Local Oscillator (LO), and by adding them together, the constant envelope MSK signal is obtained. Figure 2.8 shows the spreading and modulation steps of the IEEE 802.15.4 [3], while Figure 2.9 shows the signal at each intermediate point (Bits, Symbols, Chips and Modulated shaped signal).

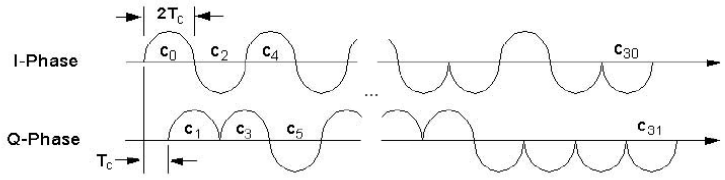


Figure 2.7 Sample Baseband Chip Sequence After Pulse Shaping

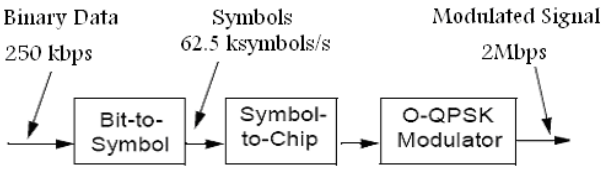


Figure 2.8 Spreading and Modulation Steps

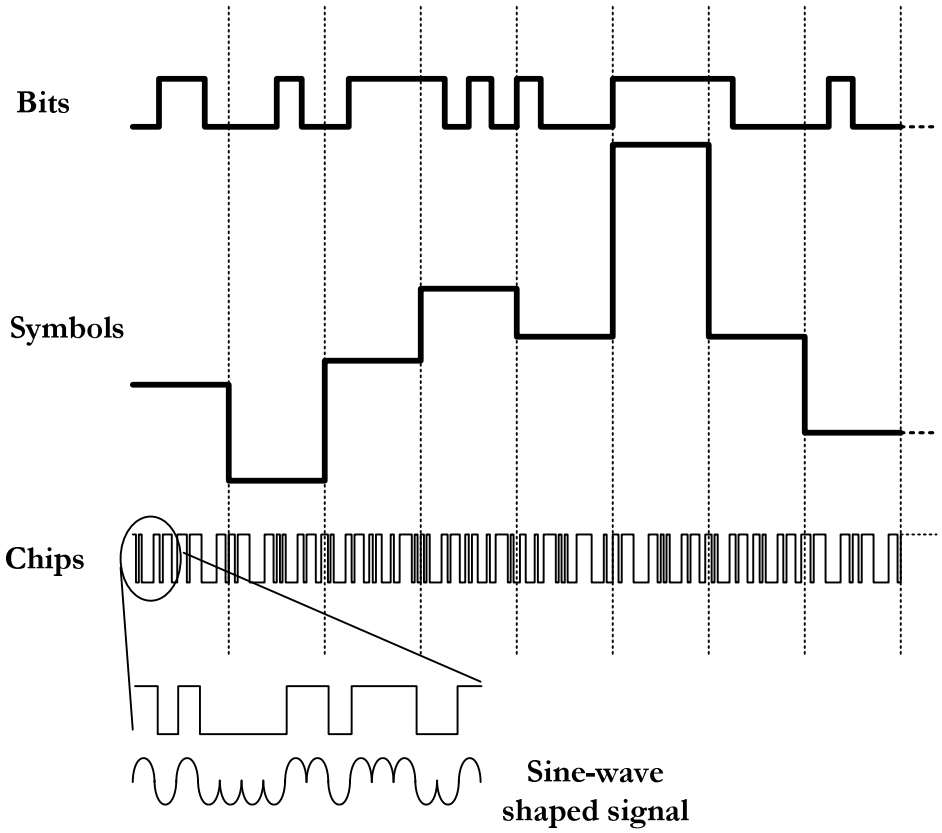


Figure 2.9 An Example of a Typical Signal Across the Modulation Process

2.2.4 Sensitivity Requirement

Receiver sensitivity is the minimum detectable signal at which the receiver can interpret with the maximum allowable BER. The IEEE 802.15.4 compliant receiver should be able to achieve a sensitivity of -85 dBm or better. For this signal level at the input, the receiver Packet error rate should be less than 1%. The packet error rate is the percentage of the received erroneous packets. A packet is erroneous if it has an error that can not be corrected by the receiver decoding scheme. The packet structure [3] is shown in Figure 2.10.

Octets: 4	1	1		variable
Preamble	SFD	Frame length (7 bits)	Reserved (1 bit)	PSDU
SHR		PHR		PHY payload

Figure 2.10 Packet Format

Preamble field: composed of 32 binary zeros and used for chip and symbol synchronization.

SFD field: Start of Frame Delimiter, 8 predefined bits indicating the end of the preamble and the start of the packet data. The SFD content is 11100101.

Frame length field: a 7-bit field specifies the PHY Service Data Unit (PSDU) Length (in octets). It can range from 0 to 127.

PSDU field: it has a variable length and carries the PHY packet data. It may contain MAC sublayer frame (MPDU) if the length is 5 octets or more than 7 octets.

2.2.5 Blocker Requirement

The receiver jamming resistance (channel rejection) is the ability of the receiver to achieve the required PER with the co-existence of large blockers adjacent to the channel of interest. To measure the adjacent or alternate channel rejection, the desired signal should be a compliant 2450 MHz IEEE 802.15.4 signal with a 3dB larger power than the receiver sensitivity. On the other hand, the adjacent or alternate channel should be either

at 0dB or 30 dB relative to the desired channel power level respectively. Only one interfering signal is allowed at a time, either the adjacent or the alternate channel.

2.2.6 Dynamic Range

The maximum allowed power level at the receiver input is -20 dBm, this leads to a dynamic range of 65 dB or more.

2.2.7 Transmit Power and Power Spectral Density Mask

A compliant IEEE 802.15.4 shall be able to transmit at least -3dBm signal, while programmability is allowed to reduce this level when needed to avoid interference. The maximum power transmitted should not exceed 10dBm as stated by Federal Communications Commission (*FCC*) regulations. The Power Spectral Density Mask is defined to be the boundaries of the transmitted signal, as shown in Figure 2.11. IEEE 802.15.4 PSD mask, should follow the limits shown in Table 2.3. All measures should be performed using a 100 KHz resolution bandwidth. The reference level is the maximum average power measured within ±1MHz from the center frequency.

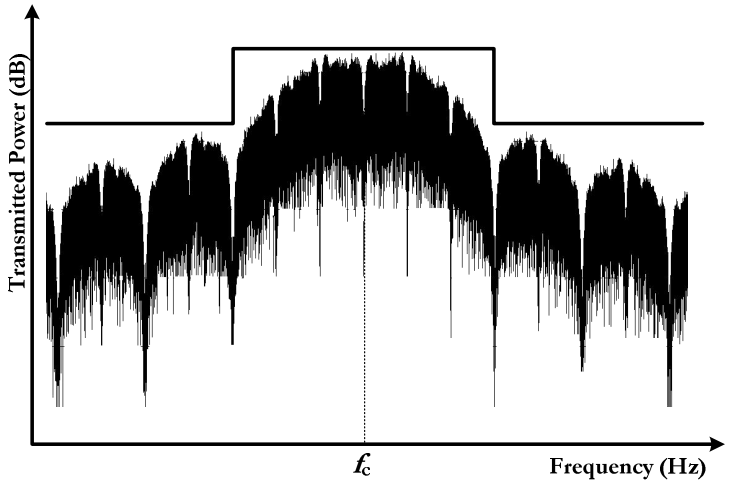


Figure 2.11 PSD Mask for a Typical Transmitted Signal

Table 2.3 Transmit PSD Mask [3]

Frequency	Relative Limit	Absolute Limit
$\|f-f_c\|>3.5$ MHz	-20 dBm	-30 dBm

2.2.8 Error Vector Magnitude (EVM)

Error vector magnitude is a measure of the modulation accuracy. It measures the average deviation of N received complex chip values ($\tilde{I}_j, \tilde{Q}_j$) from the ideal values (I_j, Q_j), Figure 2.12 shows the EVM calculations [3]. This can be done by averaging the error vector ($\delta I_j, \delta Q_j$) through these N values, as shown in equation (2.2). Where, S is the magnitude of the vector of the ideal constellation point.

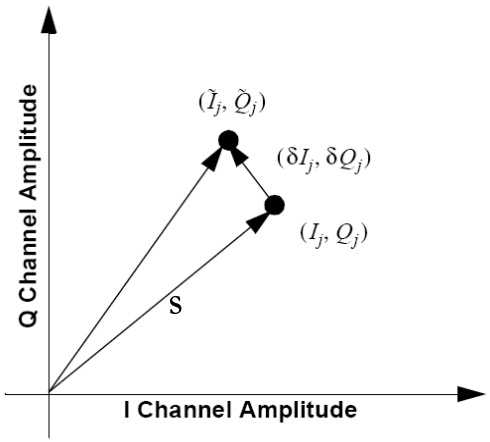


Figure 2.12 EVM Calculations

$$EVM = \sqrt{\frac{\frac{1}{N}\sum_{j=1}^{N}(\delta I_j^2 + \delta Q_j^2)}{S^2}} \quad X\ 100\%, \quad where\ S^2 = I_j^2 + Q_j^2 \tag{2.2}$$

IEEE 802.15.4 requires an EVM less than 30% for 1000 chips. The test shall be made on baseband I and Q after recovery through a reference receiver. For example, if the average error power (the sum of δI^2 and δQ^2) over 1000 chips (N) is 0.09 the ideal transmitted power (S^2), the result EVM will be 30%.

2.2.9 TX-to-RX and RX-to-TX Turn Around Time

TX-to-RX turn around time is the time from the trailing edge of the last transmitted symbol until the receiver is ready to receive the next PHY packet. It shall be 12 symbol periods. On the contrary, RX-to-TX turn around time is the time between the trailing

edge of the last symbol of a received packet until the transmitter is ready to transmit the next packet. It shall be also 12 symbol periods.

2.2.10 Coexistence with Other IEEE Standards

Coexistence with other wireless standards is one of the main issues to be analyzed in any newly added standard. IEEE 802.15.4 covers three different bands; the 868 MHz band and the 915 MHz band do not have the coexistence problem as they do not have significant interaction with other IEEE 802 standards [3].

The international band, 2.4 GHz, has the maximum interaction with IEEE wireless standards such as: IEEE Std 802.11b (2400 MHz DSSS), IEEE Std 802.15.1 (2400 MHz FHSS), IEEE P802.15.3 (2400 MHz DSSS), IEEE Std 802.11 (2400 MHz FHSS, and infrared 333 GHz AM), IEEE Std 802.16-2001 (2400 MHz OFDM), and IEEE Std 802.11a-1999 (5.2GHz DSSS).

Precautions and procedures stated in the IEEE 802.15.4 are discussed through this context. DSSS, using PN chip sequence, provides IEEE 802.15.4 robust performance towards interference, and also its low power transmission make it act as wide band interference for other coexisting standards.

Using multiple algorithms and functions such as Energy Detection (ED), Link Quality Indication (LQI), and Clear Channel Assessment (CCA) in its Carrier Sense Multiple Access with Collision Avoidance (CSMA-CA) mechanism provide a channel selection criteria, collision avoidance and retransmission techniques. These algorithms assure a good quality wireless session in the coexistence of other IEEE wireless standards. Annex E in the IEEE 802.15.4 standard [3] describes the functionality of each of these functions. Some of these coexistence issues are analytically analyzed and new BER rate equations are derived in the literature [11-14].

2.2.11 Summary of Specifications from Standard

Table 2.4 shows the summary of IEEE 802.15.4/ZIGBEE specifications from the standard that is used in Chapter III.

Table 2.4 IEEE 802.15.4 Standard Summary of Specifications

Name	Value	Name	Value
Frequency band (MHz)	2400-2483.5	Receiver Sensitivity	-85 dBm
# of Channels	16	Max. Receiver Input	-20 dBm
Channel Spacing (MHz)	5	Jamming Res. (adj. Ch.)	0 dB
Data Rate (Kbps)	250	Jamming Res. (alt. Ch.)	30 dB
Chip Rate (Kchips/s)	2000	Rx to Tx turnaroundtime	12 symbols
Modulation Scheme	O-QPSK	Preamble field for Synch.	32 binary zeros
Packet Error Rate	< 1%	Accuracy	± 40 ppm

2.3 ZIGBEE vs. Other Short Range Wireless Communications

IEEE 802.15.4/ZIGBEE has a lower transmission power as well as lower power consumption compared to other short range wireless standards; it has 30 m of nominal distance of operation and 250 Kbps. Also it uses low system resources, and can be applied for large network sizes. Transferring text and security information and authentication procedures are the most adequate use for the ZIGBEE Standard. Table 2.5 and Figure 2.1 summarizes the main differences between ZIGBEE and other short range wireless standards.

Table 2.5 Short Range Wireless Communications Summary

Standard	IEEE802.15.1 Bluetooth	IEEE802.11b WiFi	IEEE802.11g	IEEE802.11a	IEEE802.15.4 ZIGBEE
Max. data rate	1 Mb/s	11 Mb/s	54 Mb/s	24 Mb/s mandatory 54 Mb/s optional	250 Kb/s
Max. distance	10 m	100m	100m	50 m	30 m
Frequency band	2.4 GHz	2.4 GHz	2.4 GHz	5.15 to 5.35 & 5.725 to 5.825 GHz	2.4 GHz
Channel BW	1 MHz	25 MHz	25 MHz	20 MHz	3 MHz
Cost	$	$$	$$$	$$$	$
Power	Low	Moderate	High	High	Very Low

CHAPTER III

IEEE 802.15.4/ZIGBEE:

TRANSCEIVER ARCHITECTURE AND SYSTEM DESIGN

3.1 Existing Architectures

Different architectures have been reported compliant with IEEE 802.15.4 to match ZIGBEE applications. A Low-If receiver is reported in [15] integrated with a direct VCO modulation transmitter. This forces the synthesizer to be able to lock at 0.5 MHz around each channel beside the 5MHz apart channels. Thus an Integer-N synthesizer should have a reference frequency equal to 0.5MHz, leading to a higher settling time and in-band spurs. On the other hand, Fractional synthesizer increases the design complexity, power, and fractional in-band spurs. In [16-18] a low IF receiver with a direct conversion transmitter is reported leading to a similar LO spurs' problem, otherwise an extra frequency synthesizer is used. In-band spurs results in in-band shifted versions of the signal of interest, as illustrated in Figure 3.1.

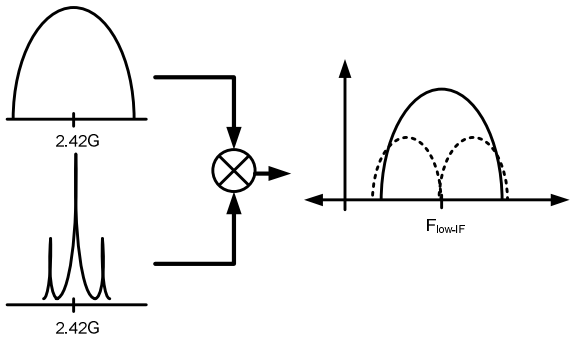


Figure 3.1 Effect of In-band LO Spurs on the Down-Converted Signal (Example)

3.2 Proposed Architecture: Direct Conversion

From the IEEE 802.15.4 signal study, an Offset-QPSK (OQPSK) is a continuous phase signal that doesn't have any information at DC. It is generated by splitting the incoming data bits into I and Q alternating. Then the Q branch is shifted by half a bit duration, to avoid having both I and Q bit streams toggling at the same time, so the transmitted signal will have less phase transitions creating an amplifier-friendly signal that can operate in nonlinear environments.. The result streams are shaped using half sine wave shaping filter to reduce the side lobes of the transmitted signal results in less signals interference. The two shaped branches (I and Q) is up converted with a 90 degrees phase shifted signal and transmitted at 2.4GHz. Figure 3.2 shows the transmitted signal.

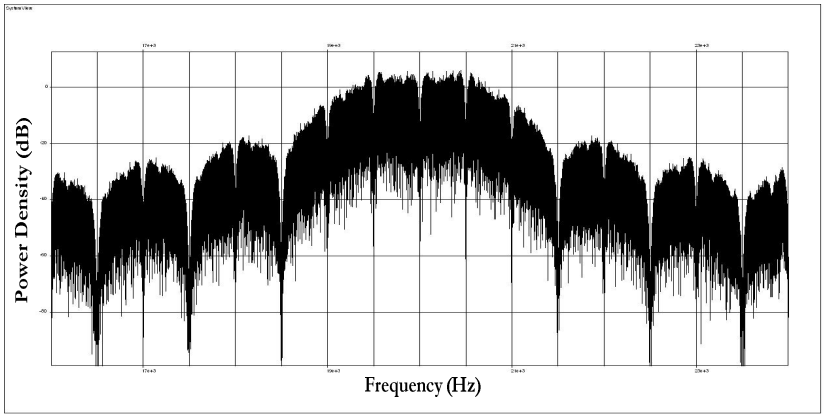


Figure 3.2 OQPSK Transmitted Signal

Due to the offset feature and the sine wave shaping, the signal matches the Minimum Shift Keying (MSK) signal format. This signal can be detected either coherently using direct conversion receiver on noncoherently using a Low-IF receiver.

Low IF receivers [18, 19] do not have the famous problems of direct conversion receivers as DC offset, flicker noise, IQ mismatch, LO self mixing, and even order distortion. On the other hand, Direct conversion (Zero-IF) receivers [20, 21] do not require an Image Rejection Mixer (IRM) or a complex channel filter to reject the images created by the down-conversion technique. Also they don't need an external bulky SAW filter to reject out of band interferers. Same Local oscillator frequency can be used in transmit and receive states, and being able to implement coherent detection that gains 3dB more in sensitivity compared to LOW IF demodulators.

Direct Conversion receiver is used through out this design to detect I am Q data independently as QPSK receivers. The proposed architecture is shown in Figure 3.3.

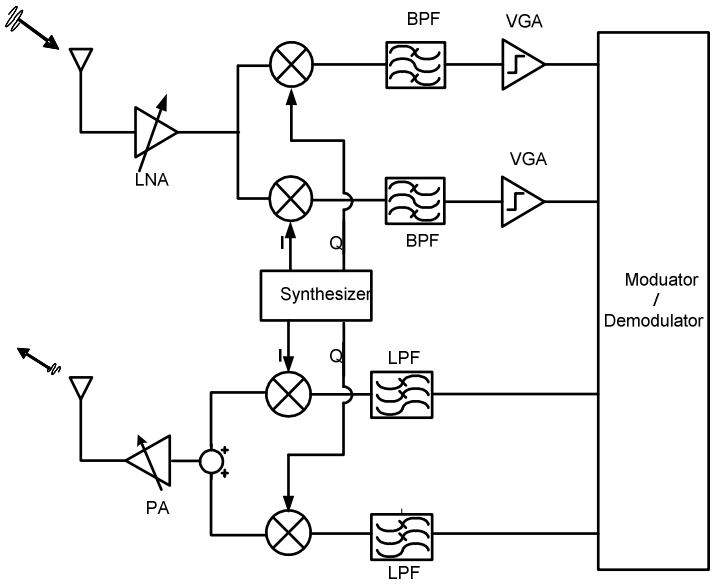


Figure 3.3 Transmitter/Receiver Direct Conversion Architecture

3.3 System Level Design and Block Specifications

3.3.1 Receiver System Design

Understanding the system and pinpointing the power saving features, is the key to design an optimum low power transceiver. A summary of the IEEE 802.15.4 target specifications is shown in Table 3.1. Targeted sensitivity is 3 dB lower than the required one, as a design margin. Also, targeted maximum receiver input is increased by 4 dB as a design safety. Thus the targeted Dynamic Range (DR) becomes 72 dB instead of the 65 dB stated by the standard.

Table 3.1 Summary of the Targeted IEEE802.15.4 Specifications

Name	Value	Name	Value
Frequency band (MHz)	2400-2483.5	Receiver Sensitivity	*-88 dBm*
# of Channels	16	Max. Receiver Input	*-18 dBm*
Channel Spacing (MHz)	5	Jamming Res. (adj. Ch.)	0 dB
Data Rate (Kbps)	250	Jamming Res. (alt. Ch.)	30 dB
Chip Rate (Kchips/s)	2000	Rx to Tx turnaroundtime	12 symbol periods
Modulation Scheme	O-QPSK	Preamble field for Synch.	32 binary zeros
Packet Error Rate	< 1%	Accuracy	± 40 ppm

A. Required Noise Figure (NF)

To get the required NF for the receive chain; the required Signal-to-Noise ratio (SNR) at the demodulator input to achieve the Packet Error Rate mentioned in Table 3.1 should be obtained.

$$
\begin{aligned}
&Noise\,Factor\,(F) \\
&\quad = \frac{SNR_i}{SNR_o} = \frac{S_i}{N_i}\frac{N_o}{S_o} = \frac{S_i}{kT_oBW}\cdot\frac{1}{SNR_o} \\
&Noise\,Figure\,(NF) \\
&\quad = 10\log_{10}(F) = S_i(dBm) + 174(dBm) - 10\log_{10} BW - SNR_0(dB) \\
&where\ N_i\big|_{dBm} = kT_oBW\big|_{dBm} = -174dBm + 10\log_{10} BW \\
&\quad k : Boltzmann's\,const. \qquad T_o : Room\ Temp.\ in\ \ Kelvin\,(300k)
\end{aligned}
\tag{3.1}
$$

N_i represents the noise input to the circuit from a 50Ohm antenna, under impedance matching conditions. This is so called *Noise floor*. Thus, for a specific receiver (specific NF), as the input signal power increases, the output SNR increases. Therefore, the worst case output SNR occurs at the minimum input signal power (receiver sensitivity), since the receiver NF is constant versus input power. Noise Figure should be calculated at this worst case scenario.

$$
SNR_0\big|_{\min} = \left.\frac{S_0}{N_o}\right|_{\min} = \frac{G_{Rx}\cdot S_i\big|_{\min}}{N_{generated} + G_{Rx}\cdot N_i} \tag{3.2}
$$

In order to obtain the required output SNR, analysis should be done from the Digital Signal Processing (DSP) section down to the RF section, as shown in Figure 3.4.

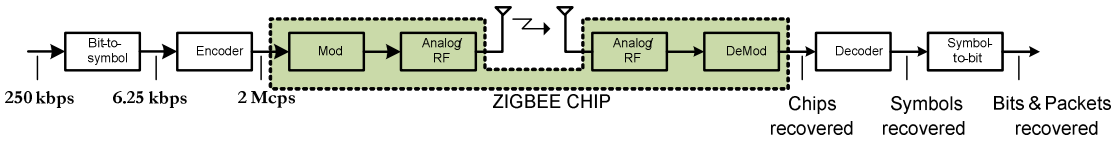


Figure 3.4 Transmitter/Receiver Main Building Blocks

The IEEE 802.15.4 uses a Direct Sequence Spread Spectrum (DSSS) encoding; after grouping the bits into symbols of 4-bits each, each symbol is mapped to one of pseudo-random words of 32-bits each, as shown in Table 2.2. By having a gain of 8, this redundancy increases the BW by the same ratio and improves the BER for the same SNR.

To obtain the gain in the BER, the effect of the coding technique should be studied. The pseudo random codes are chosen in a way to have a minimum distance of $d_{min}=12$ as shown in Table 3.2, where d_{min} of two codes is the summation of the different bits between the two codes. As this number increases the ability to detect and/or correct errors by the decoder will increase.

Table 3.2 Minimum Distances between IEEE802.15.4 Transmitted Codes

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	0	16	18	20	20	20	18	16	16	12	14	20	20	20	14	12
2	16	0	16	18	20	20	20	18	12	16	12	14	20	20	20	14
3	18	16	0	16	18	20	20	20	14	12	16	12	14	20	20	20
4	20	18	16	0	16	18	20	20	20	14	12	16	12	14	20	20
5	20	20	18	16	0	16	18	20	20	20	14	12	16	12	14	20
6	20	20	20	18	16	0	16	18	20	20	20	14	12	16	12	14
7	18	20	20	20	18	16	0	16	14	20	20	20	14	12	16	12
8	16	18	20	20	20	18	16	0	12	14	20	20	20	14	12	16
9	16	12	14	20	20	20	14	12	0	16	18	20	20	20	18	16
10	12	16	12	14	20	20	20	14	16	0	16	18	20	20	20	18
11	14	12	16	12	14	20	20	20	18	16	0	16	18	20	20	20
12	20	14	12	16	12	14	20	20	20	18	16	0	16	18	20	20
13	20	20	14	12	16	12	14	20	20	20	18	16	0	16	18	20
14	20	20	20	14	12	16	12	14	20	20	20	18	16	0	16	18
15	14	20	20	20	14	12	16	12	18	20	20	20	18	16	0	16
16	12	14	20	20	20	14	12	16	16	18	20	20	20	18	16	0

A decoder can be a soft decision or hard decision decoder. The hard decision decoder decides each bit separately, and then calculates the distance between the detected code and all the possible codes. It chooses the code with the minimum hamming distance [22] to be the estimated code. On the other hand, the soft decision decoder calculates the Euclidian distances before deciding clearly each bit. It can be performed in the analog domain, which makes it more complicated and power consuming compared to the simple digital hard decision decoders.

Assuming a hard decision decoding, and for each code word (32 chips), errors up to $t = \left\lfloor \frac{d_{\min}}{2} \right\rfloor = 6$ can be detected and corrected. Thus, a code word has an error if more than 6 errors occurred in this code word; consequently an error occurs in a packet if

at least one code word has an error within the packet. Each packet contains at most 127 code words in the PSDU field shown in Figure 2.10.

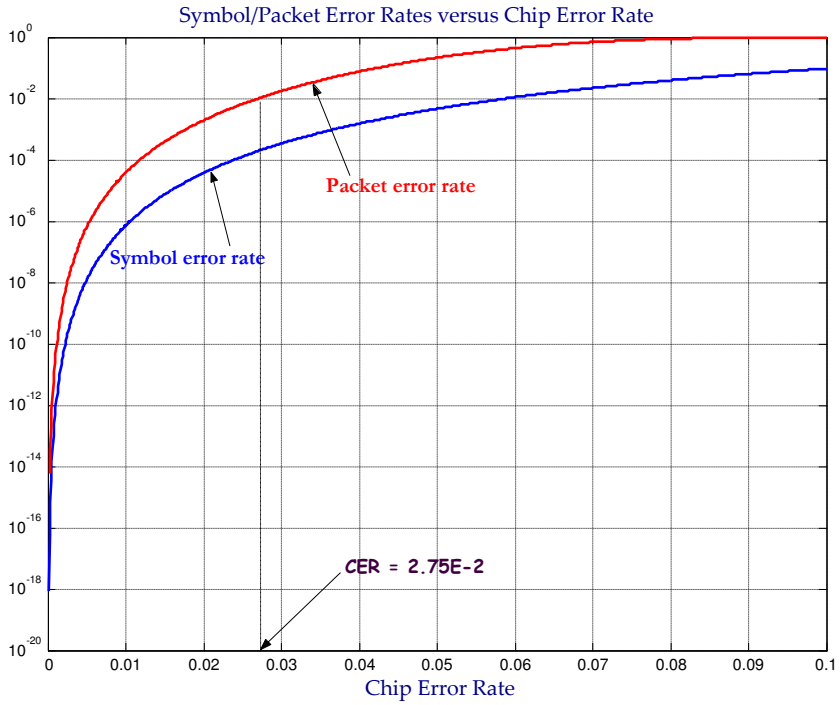


Figure 3.5 PER, SER, CER for IEEE 802.15.4

A *Matlab* script (Appendix A) has been written using these relations to indicate the Chip Error Rate (CER) causing the maximum Packet Error rate (PER) permitted by the standard of 1%. The relation between the Packet, Symbol, and Chip error rates are illustrated in Figure 3.5, using a **Hard Decision** Decoding Technique.

For a PER of 1%, the CER should not exceed 2.7% which is used in the derivations of the system specifications derivations.

For a direct conversion receiver, the BER curve versus the SNR, can be generated using *SystemView* [23]. Using an I and Q separate decision paths, Figure 3.6 shows the ideal BER curve without introducing any non-idealities such as: DC offset, I/Q mismatches, spurs, or Phase noise of the freq. synthesizer. As shown, the lower the SNR, the lower the ability of the demodulator to detect the transmitted bit, thus the more BER expected. The BER curve shape and roll off is determined by the modulation scheme as well as the demodulator implementation.

It is clear that a SNR of 4.5 dB is enough ideally to obtain the proper BER derived for the Hard Decision decoding and for this simple demodulator. To see the effect of each non-ideality and thus specify it down to the block level specifications through the SNR degradation, each non-ideality should be added at a time and the degradation in the SNR required for the same BER can be noted [24, 25]. Although, this method ignores the dependency between the non-idealities, as a first degree of approximation, it gives an insight of their tolerable optimistic levels.

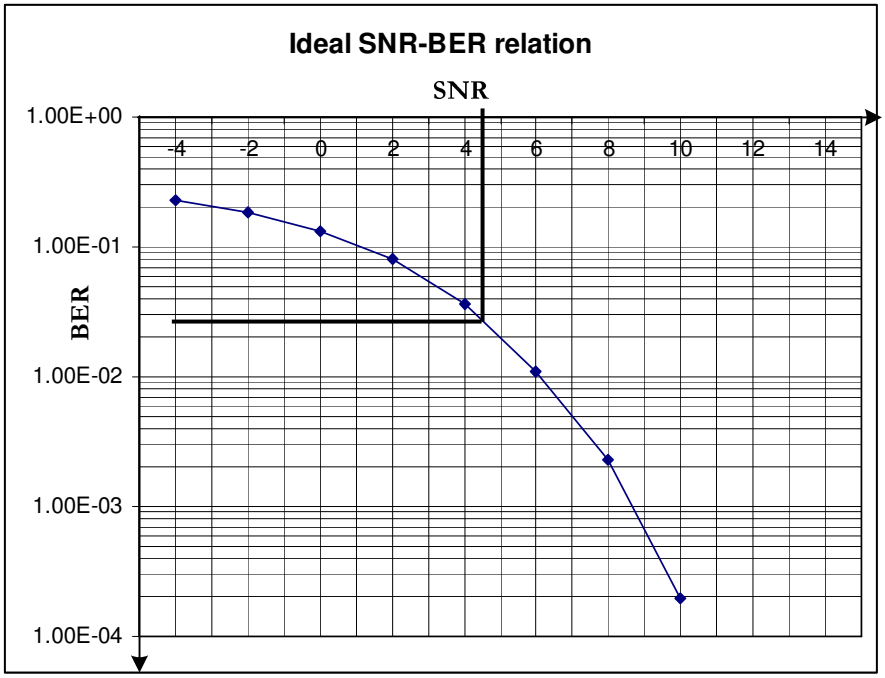


Figure 3.6 SNR-BER Relation for Ideal Performance

DC-Offset at the Demodulator Input

One of the main problems of direct conversion receivers is the DC offset generated by self-mixing, second order nonlinearity, systematic, and random process mismatches. Figure 3.7 shows possible sources of DC offset in direct conversion receivers. Although the proposed receiver will have a HPF to reject the DC offset after the Mixer, this will not be the case at the demodulator input. DC offset resulting from the LPF and the VGA will go directly to the demodulator. By introducing a DC offset to the signal at the input of the demodulator, the allowable percentage of DC offset can be detected.

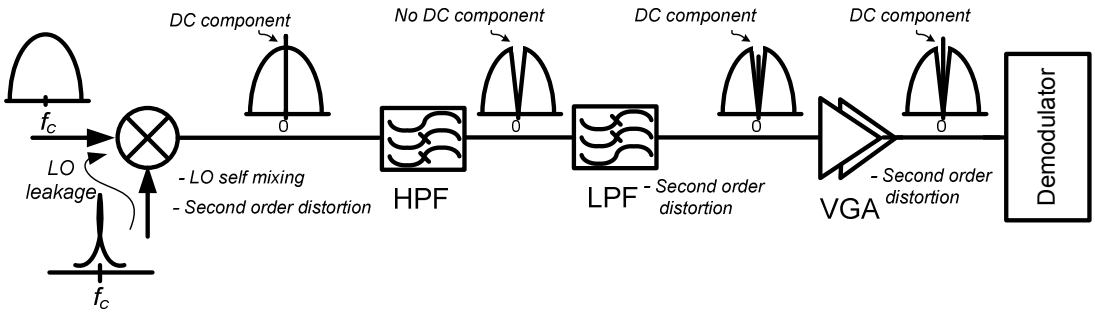


Figure 3.7 Sources of DC Offset in Direct Conversion Receiver

Figure 3.8 shows the simulation results for different DC offset ratios relative to the signal peak at the demodulator input. It is shown that a degradation of 0.25 dB in the SNR results from 5% offset while a degradation of 0.5 dB from 10 % offset, 1 dB from 15%, and 1.8 dB from 20% DC offset.

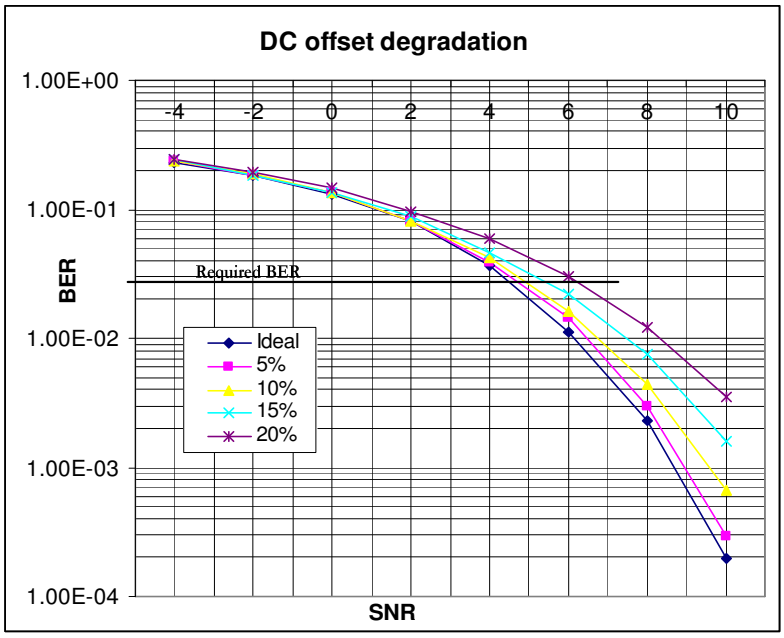


Figure 3.8 DC Offset Degradation for the SNR

By choosing the 10% DC offset degradation, means that an offset of 0.1 times the signal level is permitted to exist at the input of the demodulator, and this will result in 0.5 dB degradation in the SNR.

HPF Cut-Off Frequency

A HPF can be used to eliminate the DC offset at some intermediate nodes (e.g. Filter output) to meet the previous specification at the demodulator input. Moreover, it is a must in direct conversion receivers to remove flicker noise. But, there is a tradeoff between DC offset and flicker noise elimination on one side and between distorting the signal of interest on the other side. Preferably, the cut-off frequency (*fc*) should be close to zero, which is not feasible from the practical implementation perspective. As *fc* increases, signal degradation is expected, depending on the signal nature and its power spectral density. The maximum allowed *fc* can be derived by system simulations as follows.

By applying a first order RC HPF, with a variable cut-off frequency. When *fc* increases, SNR degradation increases as shown in Figure 3.9.

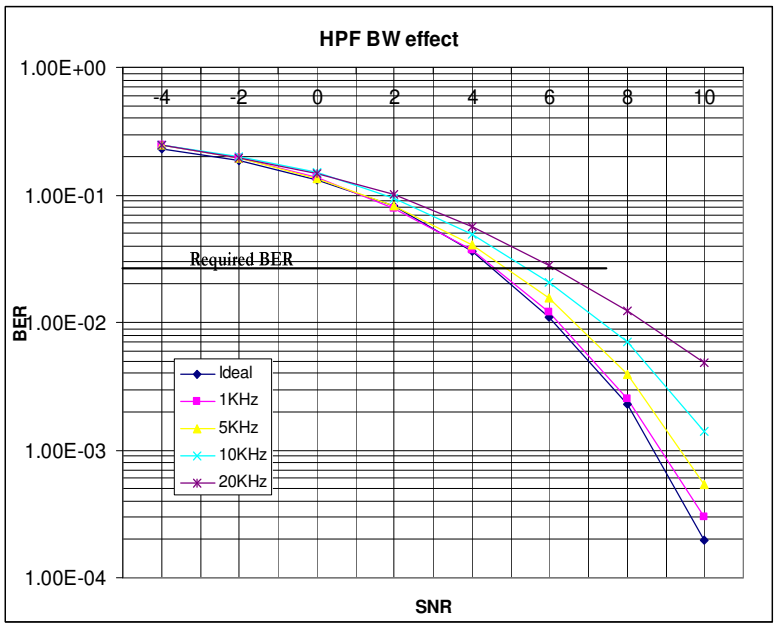


Figure 3.9 HPF Cut-off Frequency Effect on the BER

For *fc* of 1KHz, SNR degrades by 0.1 dB from the ideal values. The degradation continues till it reaches 1.8 dB for 20 KHz *fc*. By choosing *fc* to be 5 KHz, a SNR degradation of 0.5 dB should be considered.

Frequency Synthesizer Phase Noise and Spurs

For integer-N synthesizers, the reference frequency is equal to the frequency step (channel spacing). Thus, the reference spurs' frequency locations coincide with the adjacent and alternate interferers [26]. After being down-converted, interferes will fall in band with the signal as shown in Figure 3.10. Since at the spur location, the spur integrated power is much larger than the phase noise integrated power, therefore the phase noise can be neglected in this case.

First, a rough estimation for the spurs at 5 MHz and 10 MHz can be calculated to know their approximate required value.

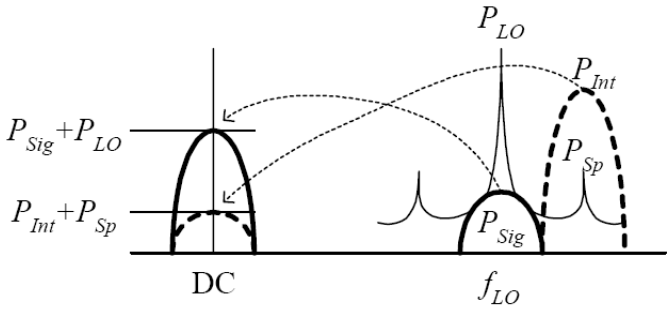


Figure 3.10 Spurs Effect on the SNR Degradation Analytically

For multiple interferers, equation (3.3) states the SNR_o at the output of the synthesizer as a result of these interferes only.

$$SNR_o = \left((P_{sig} + P_{LO}) - (P_{\text{int}1} + P_{sp1}) - (P_{\text{int}2} + P_{sp2}) - \ldots\right) > SNR_o\big|_{\min} \tag{3.3}$$

From IEEE 802.15.4 standard, There are only two possible interferes; 1) Adjacent Channel Interferer at 5MHz apart from the signal of interest with the same power level of the signal. 2) Alternate Channel Interferer at 10MHz apart from the signal of interest with 30 dB higher power than the desired signal power level. This means the first and second synthesizer spurs, from the receiver perspective. Since IEEE 802.15.4 standard states that only one interferer exists at a time, equations (3.4 – 3.5) states the required spur power that corresponds to the required contribution to the in-band noise:

$$Spurious\ \ power1\ in\ dBc = (P_{sp1} - P_{LO}) < P_{sig} - P_{\text{int}1} - SNR_{\min 1} \tag{3.4}$$

$$Spurious\ \ power2\ in\ dBc = (P_{sp2} - P_{LO}) < P_{sig} - P_{\text{int}2} - SNR_{\min 2} \tag{3.5}$$

Treating the down-converted in-band interferer as noise is an accepted approximation relying to the uncorrelated nature of the interferer with the signal of interested. Also, the fairly flat frequency spectrum of the MSK makes it almost uniformly distributed in the band of interest. Assuming the SNR to be 8 dB with some margin, and by taking into account that there are other multiple noise sources, therefore the spurious signal requirement at 5 MHz is -8 dB. While, the spurious signal requirement at 10 MHz is -38 dB.

For accurate results, Simulations are done using the two interferes multiplied by proper gains and injected in the same band of the signal. Figure 3.11 shows different values for the spurs power level with their corresponding SNR degradation.

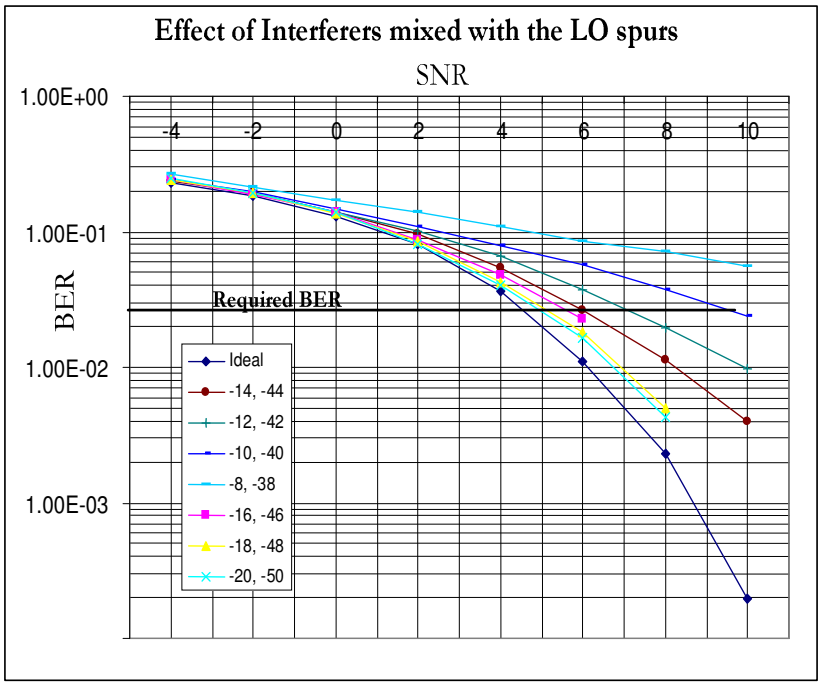


Figure 3.11 SNR Degradation for Interferers Combined with LO Spurs

For a -20, and -50 dBc, the degradation is 0.5 in the SNR, while for -18 dBc and -48 dBc, a 0.8 dBc degradation is obtained. Thus choosing -18 dBc and -48 dBc will be appropriate.

From simulations, it is clear that the above equation was a rough estimate for the spur requirement due to the assumptions used for this equation. Also, the simulations are done for both interferers together which is not the case stated by the standard, where only one interferer should be added separately.

Therefore, for better accuracy, another simulation was held with one interferer at a time, the results are shown in Figure 3.12.

From these results, one can choose the Spur requirement to be -16, and -46 for the 5MHz and the 10MHz interferers respectively, with only a degradation of 0.45 dB in each of them.

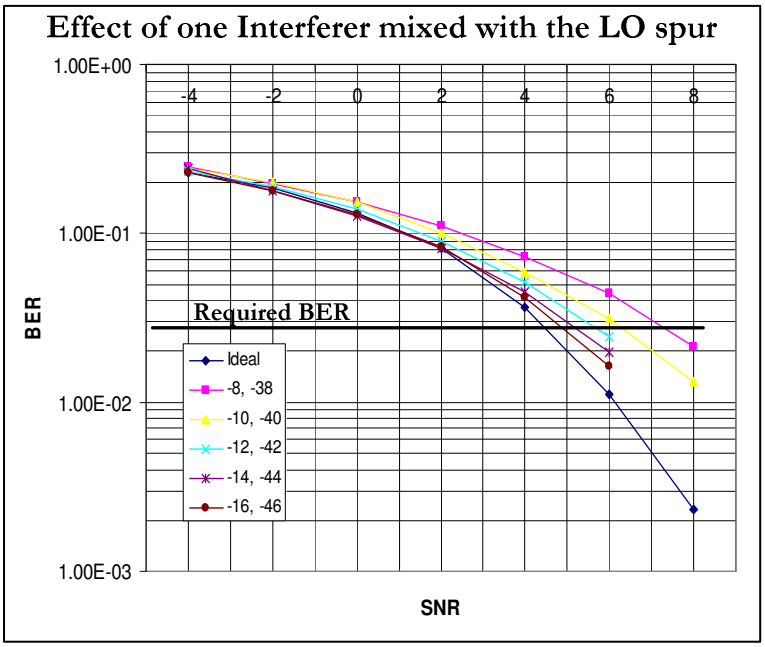


Figure 3.12 SNR Degradation of One Interferer at a Time

Receiver LPF Specifications

Now, the two interferers are introduced at 5MHz and 10 MHz away from the signal. Note that all simulations are done with a scale factor to lower frequencies to reduce the simulation time, while the relative effect remains the same. First, to identify the filter approximation, simulations are carried out between 3rd and 4th order Butterworth, versus 3rd and 4th order Chebychev. Figure 3.13 shows the results,

where the differences are very small between different approximations with different orders, thus choosing the simplest will reduce the power consumption without much degradation in the SNR. So, 3rd order Butterworth can be used.

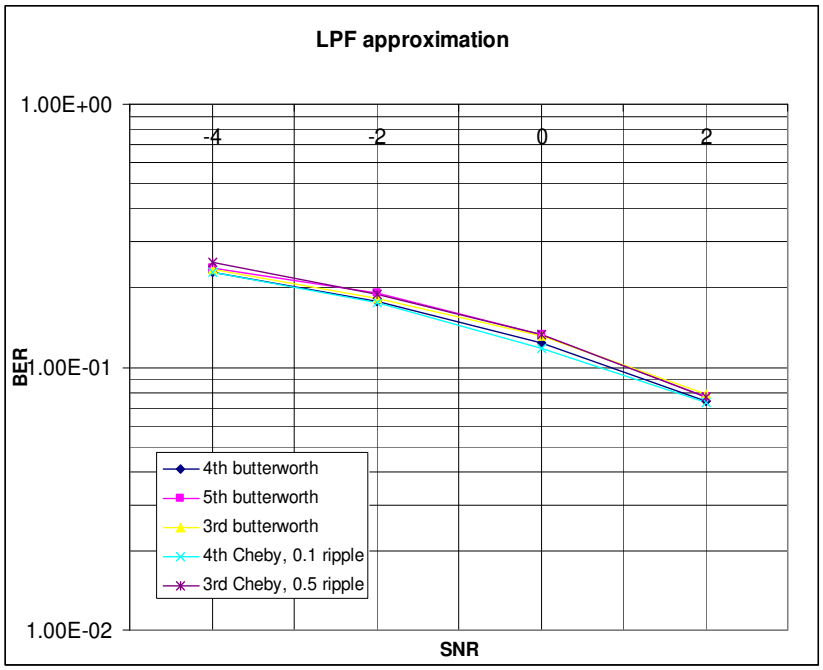


Figure 3.13 SNR versus BER for Different LPF Approximations

Then, for the BW of the filter, it should be varied to identify its ideal value. As the BW increases more noise is added just reducing the SNR value. On the other hand as filter BW reduces, more signal power will be filtered out and thus removing useful information and reducing the SNR as well. There is an optimum filter BW where the BER has its minimum. Since, the IEEE 802.15.4 Null to Null BW is 3 MHz, so sweeping the LPF BW around 1.5 MHz will give the optimum BW.

Figure 3.14 shows different performances for different BW in the presence of the interferer. It is concluded that 1MHz is the best cut-off frequency for the LPF. Degradation in SNR of at least ±0.5dB is expected for a variation of ±10% in the LPF bandwidth.

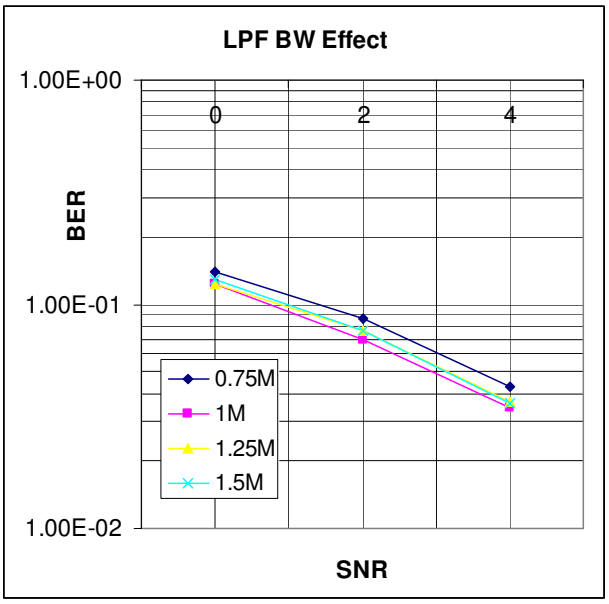


Figure 3.14 LPF Bandwidth Effect on BER

Required SNR

Assuming that the above non-idealities are independently generated and not affecting each others, a simple addition of the SNR degradation can be held. A summary for the previous decisions based on simulations is shown in Table 3.3.

Table 3.3 Summary for Non-idealities Used in BER Simulations

Non-ideality	**Value permitted**	**Degradation associated**
DC offset	10%	0.5 dB
HPF cut-off frequency	5 KHz	0.5 dB
Spur requirements	-16 dBc at 5 MHz	0.9 dB
	-46 dBc at 10 MHz	
LPF approximation, order	3rd order Butterworth	NA
LPF cut-off frequency	1 MHz	NA
IQ Gain Mismatch	11%	0.5 dB
Total degradation		**2.4 dB**

The required SNR with the above analysis becomes 6.9 dB instead of 4.5 dB. By using the NF equation (3.1), where BW is set to be 1MHz (filter bandwidth). Also, by adding another 3 dB of margin to account for the dependency between these non-idealities, equation (3.6) shows the overall receiver NF required.

$$\begin{aligned} NF &= S_i(dBm) + 174(dBm) - 10\log_{10} BW - SNR_0(dB) - Margin \\ &= -88 + 174 - 60 - 6.9 - 3 = 16.1dB \end{aligned} \tag{3.6}$$

B. Receiver Gain

Since the receiver dynamic range is 68dB, one receiver gain stage can not be used. This is the reason a VGA with multiple gains to relax the dynamic range required from the succeeding block (demodulator). An additional modification to relax the steps of the VGA is to switch off the LNA and replace it with an attenuator at higher input power levels. At such levels, the input SNR is very high reducing the importance of having an LNA or to reduce the overall receiver NF.

Assuming the demodulator input dynamic range ranges from -2dBm to 10dBm. This corresponds to 0.5vpp differential to 1vpp differential in a 50Ohm resistor. So the maximum gain and minimum gain can be calculated:

$$G_{\max} = min\ required\ output - max\ expected\ input = -2 - (-88) = 86dB$$
$$G_{\min} = max\ required\ output - min\ expected\ input = 10 - (-16) = 26dB \quad (3.7)$$

Splitting the dynamic range into two sections; Section1 has the LNA on where the power signal at the input ranges from -88dBm to -52dBm, while Section2 has the LNA off and the attenuator on where the signal power at the input ranges from -52dBm to -16dBm. In each section, the VGA gain will exercise all its steps as shown in 3.4.1.E.

C. Required IIP2

IIP2 is a very important requirement in a direct conversion receiver. Any interferer or even the signal of interest will cause a DC level because of the second order nonlinearity of the receiver. This DC shift can easily saturate the receiver stages leading to a BER close to 0.5. Although a fully differential receiver structure is used, but due to mismatchs, still a second order nonlinearity can be created.

In the proposed Receiver, there is a HPF at the filter input, the nonlinearity of the filter followed by the VGA can cause a DC offset at the demodulator input. As shown in section 3.4.1.A, a DC offset of 10% of the signal level can be tolerated.

Assuming a nonlinear system of $y = \alpha_1 x + \alpha_2 x^2 + \alpha_3 x^3$ and by having two tones at the input $A_1 \cos w_1 t + A_2 \cos w_2 t$, the output tones are shown in equation (3.8).

$$
\begin{aligned}
y = & \left(\frac{\alpha_2 A_1^{\,2}}{2} + \frac{\alpha_2 A_2^{\,2}}{2} \right) + \left(\alpha_1 A_1 + \frac{3\alpha_3 A_1^{\,3}}{4} + \frac{5\alpha_3 A_2^{\,2} A_1}{4} \right) \cos w_1 t \\
& + \left(\alpha_1 A_2 + \frac{5\alpha_3 A_1^{\,2} A_2}{4} + \frac{3\alpha_3 A_2^{\,3}}{4} \right) \cos w_2 t \\
& + \left(\frac{\alpha_2 A_1^{\,2}}{2} \right) \cos 2w_1 t + \left(\frac{\alpha_2 A_2^{\,2}}{2} \right) \cos 2w_2 t \\
& + \left(2\frac{\alpha_2 A_1 A_2}{2} \right) \cos(w_1 + w_2)t + \left(2\frac{\alpha_2 A_1 A_2}{2} \right) \cos(w_1 - w_2)t \\
& + \left(\frac{\alpha_3 A_1^{\,3}}{4} \right) \cos 3w_1 t + \left(\frac{\alpha_3 A_2^{\,3}}{4} \right) \cos 3w_2 t \\
& + \left(\frac{3\alpha_3 A_1^{\,2} A_2}{4} \right) \cos(2w_1 + w_2)t + \left(\frac{3\alpha_3 A_2^{\,2} A_1}{4} \right) \cos(2w_2 + w_1)t \\
& + \left(\frac{3\alpha_3 A_1^{\,2} A_2}{4} \right) \cos(2w_1 - w_2)t + \left(\frac{3\alpha_3 A_2^{\,2} A_1}{4} \right) \cos(2w_2 - w_1)t
\end{aligned}
\tag{3.8}
$$

As w_1 and w_2 are closer, their difference tone goes closer to DC. IEEE 802.15.4 has only one interferer at a time out of two possible interferers, this is equivalent to two tones in phase at the same frequency, and each has a 3dB less power than their total. Assuming the voltage peak of the input signal is (A_1), while the voltage peak of the single interferer is (A_2), then the voltage peak of each of these two assumed tones

is $(A_2/2)$. The total DC signal generated because of the filter and VGA nonlinearity is composed of three additive signals, as shown in Figure 3.15:

(a) DC offset due to the input signal $(\alpha_2 A_1^{\,2}/2)$

(b) DC offset due to each of the assumed tones $(\alpha_2 A_2^{\,2}/8)$

(c) Second order intermodulation (IM_2) of the two assumed tones $(\alpha_2 A_2^{\,2}/4)$

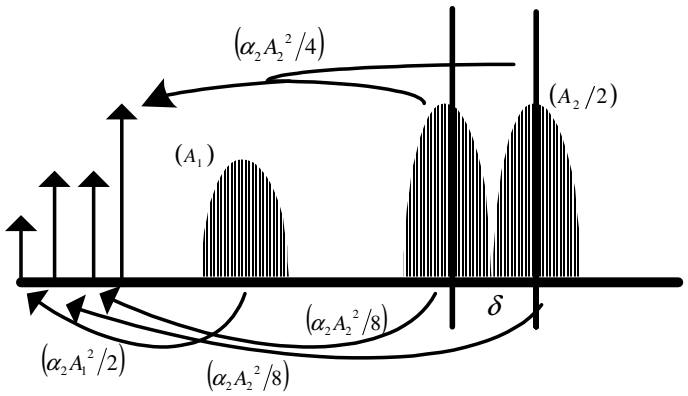


Figure 3.15 DC Components Generated from Signal and Interfere

These assumptions can be verified easily by assuming a single interferer tone with amplitude (A_2) and calculating the result DC offset at the receiver output using square law. To continue the derivation, the DC level tolerated at the demodulator input is recalled.

$$DC\ offset = \alpha_2\left(\frac{A_1^{\,2}}{2} + 2\cdot\frac{A_2^{\,2}}{8} + \frac{A_2^{\,2}}{4}\right) = \frac{\alpha_2 A_2^{\,2}}{4}\left(2 + \frac{2}{x^2}\right)$$

$$0.1(\alpha_1 A_1) = \frac{\alpha_2 A_2^{\,2}}{4}\left(2 + \frac{2}{x^2}\right)$$

$$Therefore,\ \underbrace{\frac{\alpha_2 A_2^{\,2}}{4}}_{IM2_o} = \frac{0.1x^2}{2+2x^2}\underbrace{(\alpha_1 A_1)}_{SiG_o}$$

$$Therefore,\ IM2_{in,Vpeak} = \frac{0.1x^2}{2+2x^2}\ S_{iin,Vpeak}$$

$$where,\ x = \frac{A_2}{A_1} = 1\ (adjacent\ channel) = 31.6\,(alternate\,channel) \tag{3.9}$$

Since the blocks of interest are the filter and the VGA, therefore the interferer power level in the IIP2 equation is its level at the filter input. Since there is one interferer at a time out of two interferers, there are two different IIP2 values, where the tighter will be the required specification.

$$
\begin{aligned}
IIP2 &= P_{in,I} + P_{in,I} - P_{in,IM2} \\
&= 2P_{in,I} - 20\log_{10}\left(\frac{0.1x^2}{2+2x^2}\right) - P_{in,S} \\
&= 2P_{in,I} - 20\log_{10}\left(\frac{0.1x^2}{2+2x^2}\right) - P_{in,S} + G_{LNA+Mixer} \\
IIP2_{adj} &= 2*(-85-3) - 20\log_{10}(0.025) + 85 + G_{LNA+Mixer} \\
&= (G_{LNA+Mixer} - 58.96)dBm \\
IIP2_{alt} &= 2*(-55-3) - 20\log_{10}(0.05) + 85 + G_{LNA+Mixer} \\
&= (G_{LNA+Mixer} - 4.97)dBm
\end{aligned}
\tag{3.10}
$$

By setting the gain of the LNA and Mixer, IIP2 can be calculated in both cases and the more tight number ($IIP2_{alt}$) is taken as the required specification. For example for a gain of 30dB for the LNA and Mixer combined, $IIP2_{alt}$=25dBm.

D. Required IIP3

There is no a two tone test in IEEE 802.15.4 standard to measure the IIP3. IEEE 802.15.4 identifies two different interferers, only one at a time. The first adjacent channel interferer; 5 MHz away from the signal and with the same power level of the signal, and the alternate channel interferer; 10 MHz away for the signal and at a power level 30dB higher than the signal power level. During this test, the signal of

interest power level is -85dBm (3 dB higher than the sensitivity level). Let's assume that the two interferers existed at the same time as a two tone test, resulting in an in-band IM3. Assume the input referred IM3 power is half the input referred noise of the receiver.

$$IIM3 = Sig - SNR_o - 3 = -85 - 9.9 - 3 = -97.9dBm \tag{3.11}$$

Since the two interferes are not of the same power level, simple IIP3 equation is not holding anymore. An alternative equation can be derived.

$$IIP3 = P_{in1} + \frac{P_{in2} - IM3_{in}}{2} = -85 + \frac{-55 + 97.9}{2} = -63.6dBm \tag{3.12}$$

Even with the two interferes; the required IIP3 is much relaxed. Another way to derive the IIP3 is to find the required 1dB compression point and roughly add 10dB to get the equivalent IIP3. As shown in 3.4.1.B, the maximum demodulator input will occur when the input signal power is -52dB, LNA is ON and VGA has maximum gain. The corresponding demodulator input level is 10dBm. At this signal level, the receiver should not exercise any compression to the signal. If a 0.1dB compression can be tolerated, and if the even order nonlinearity is ignored, it impacts the input referred 1dB compression point by 3 dB, as shown in equation (3.13).

$$For\ a\ system\ of\ \ y = \alpha_1 x + \alpha_3 x^3$$

$$A_{1dB} = \sqrt{0.145\frac{\alpha_1}{\alpha_3}}$$

$$A_{0.1dB} = \sqrt{0.075\frac{\alpha_1}{\alpha_3}} = \sqrt{\frac{0.145}{1.94}\frac{\alpha_1}{\alpha_3}} = 0.717A_{1dB} = A_{1dB} - 2.9dB \approx IIP3 - 13dB \tag{3.13}$$

$$IIP3 = A_{0.1dB} + 13dB = -52dBm + 13dB = -39dBm$$

This IIP3 is a tighter specification than the one before, and will be used as the receiver requirement. Thus by applying a two tone test and achieving this IIP3, the 1dB compression point is guaranteed.

E. Other Specifications

Other Specifications like synthesizer settling time, VGA Gain steps is derived next.

Frequency Synthesizer Settling Time

The settling time of the synthesizer is an indication of how fast the receiver/transmitter should be ready for channel frequency change either in the same session or for a new session. For the latter, this happen during establishing the connection and there is no time restrictions on that. The specification is generated in an existing session, where one of the terminals decides to change the channel of operation. Since the IEEE 802.15.4 works in a half duplex acknowledged system.

The terminal deciding the new channel sends a request to the other terminal on the current channel frequency, and waits for the acknowledgment. The second terminal sends the confirmation (if possible) on the current channel, and starts to shift its frequency to be able to receive the new data on the new channel frequency. This means the second terminal moves from “old-channel transmitter” state to “new-channel receiver” state. On the contrary, the first terminal receives the acknowledgment on the current channel frequency and starts shifting its frequency to be ready to send the new data on the new channel. This means the first terminal moves from “old-channel receiver” state to “new-channel transmitter” state. The standard clause that controls the turnaround time from the Rx mode to the Tx mode or vice versa. Figure 3.16 and Figure 3.17 show the channel change procedure for an existing session.

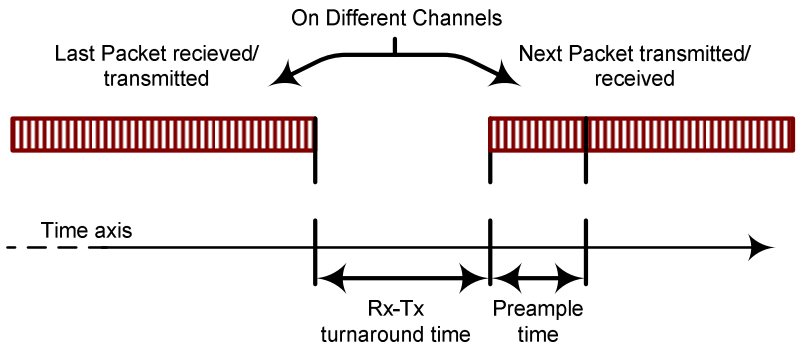


Figure 3.16 RX-TX and TX-RX Turn Around Time

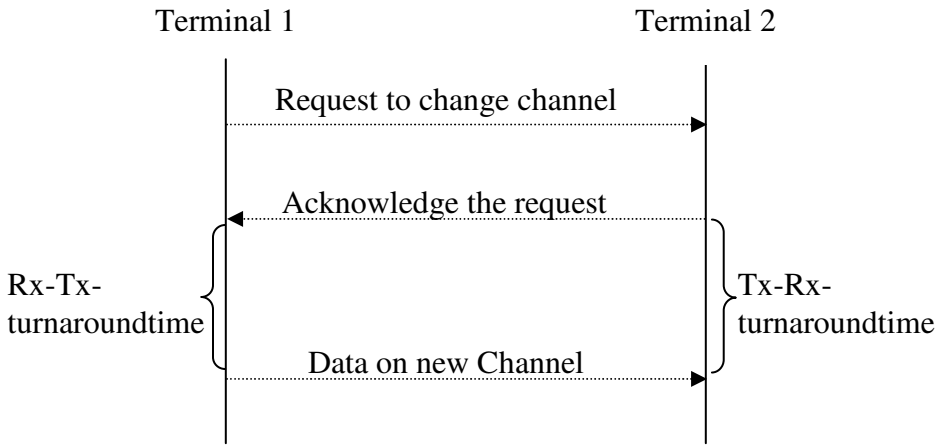


Figure 3.17. Procedure of Channel Change in an Exiting Session

The Rx/Tx turnaround time is 12 symbol periods, with a symbol rate of 62.5 Ksymbol/sec, so the synthesizer settling time is 192 μsec.

$$T_{settling} = T_{Rx-Tx\ turn-around-time} = 12\ symbols = \frac{12}{62.5 \cdot 1000} = 192\mu\text{sec} \qquad (3.14)$$

VGA Gain Steps

The VGA gain steps depend pretty much on the demodulator circuit. The gain steps are used to adjust the input of the demodulator to the optimum range for optimum detection. This can be estimated from the circuit level of the demodulator. On the other hand, choosing proper gain steps can add the ED function mentioned in section 2.2 without any extra cost. By defining the gain steps to be 12dB each and by having a peak detector followed by three comparators at the output of the VGA, The signal strength can be accurately measured within ±6dB of error as stated by the ED test.

Since for proper gain adjustment of the VGA two comparators are needed, therefore the ED implementation comes with a free cost, as shown in Figure 3.18.

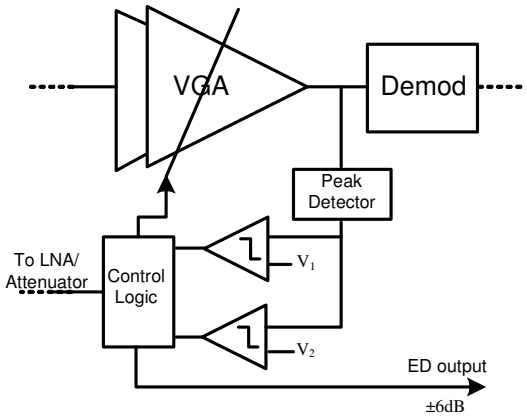


Figure 3.18 Signal Strength Detection (ED)

F. Receiver Budget Distribution and System Design Summary

After identifying the standard parameters, calculating NF, IIP2 and IIP3, $Gain_{max}$ and $Gain_{min}$ required by the receiver, the individual building blocks specifications can be calculated by applying the budget distribution equations. Figure 3.19 illustrates the receiver system design procedure, while Table 3.4 summarizes the overall specifications derived.

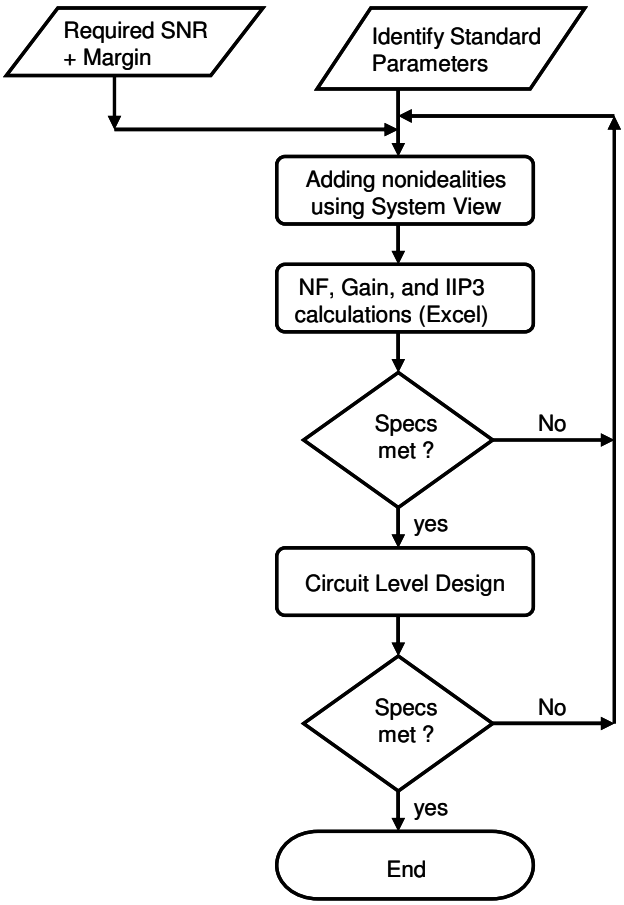


Figure 3.19 Receiver System Design Flowchart

Table 3.4 Derived Specifications

Metric		**Value**
NF		16.1dB
Maximum Gain		86dB
Minimum Gain		26dB
IIP2	Adjacent Channel	$(G_{LNA+MIXER}$-58.96)dBm
	Alternate Channel	$(G_{LNA+MIXER}$-4.97)dBm
IIP3		-39dBm

Gain equations: where G(dB)=10log(g)

$$g_{\max} = g_{LNA} * g_{Mixer} * g_{LPF} * g_{VGA,\max}$$

$$g_{\min} = l_{attenuator} * g_{Mixer} * g_{LPF} * g_{VGA,\min} \tag{3.15}$$

$$G(dB) = 10\log_{10}(g)$$

IIP2 equations are shown in equation (3.16), and assigning the LNA+Mixer to have a gain of 34dB. Also by having a 3rd order LPF with 1MHz cutoff frequency, its attenuation to the interferer at 5MHz is 42 dB, while it has 60dB attenuation to the interferer at 10MHz.

$$\sqrt{\frac{1}{iip2}} = \sqrt{\frac{1}{iip2_{LPF}}} + \sqrt{\frac{g}{iip2_{VGA} * \delta^2}}$$

$$\delta = LPF\ attenuation\ at\ Intereferer\ frequency$$
$$g = Inband\ \ filter\ \ gain \tag{3.16}$$

$$IIP2_{adj} = 10\log_{10} iip2_{adj} = -24.96dBm, \qquad \Delta_{adj} = 10\log_{10}\delta = -42dB$$

$$IIP2_{alt} = 10\log_{10} iip2_{alt} = 29.03dBm, \qquad \Delta_{alt} = 10\log_{10}\delta = -60dB$$

This requires a LPF IIP2 of 30dBm and a VGA IIP2 of -10dBm. Applying fully differential architectures should be able to achieve these IIP2 requirements.

IIP3 equations are shown in equations (3.17), where the attenuation of the interferers by the filter helped relaxing the VGA constraints.

$$\frac{1}{iip3} = \frac{1}{iip3_{LNA}} + \frac{g_{LNA}}{iip3_{Mixer}} + \frac{g_{LNA}g_{Mixer}}{iip3_{LPF}} + \frac{g_{LNA}g_{Mixer}g_{LPF}}{iip3_{VGA-Calculated}}$$

$$IIP3 = 10\log_{10} iip3, \quad G = 10\log_{10} g \tag{3.17}$$

$$IIP3_{VGA-Calculated} = IIP3_{VGA-designed} + \Delta_1 + \frac{\Delta_2}{2}$$

$$\Delta_1 = LPF\ attenuation\ at\ adjacent\ Interferer\,(5MHz) = 42dB,$$
$$\Delta_2 = LPF\ attenuation\ at\ alternate\ Interferer\,(10MHz) = 60dB$$

Finally, the NF can be calculated using the following formula:

$$F_T = F_{LNA} + \frac{F_{Mixer} - 1}{g_{LNA}} + \frac{F_{LNA} - 1}{g_{LNA}g_{Mixer}} + \frac{F_{VGA} - 1}{g_{LNA}g_{Mixer}g_{LPF}}$$

$$NF = 10\log_{10} F \tag{3.18}$$

Table 3.5 shows the receiver building blocks specifications followed by illustration plots for Gain distribution versus the input signal power level, Noise build up across the blocks versus signal build up.

Table 3.5 Specifications for Different Receiver Building Blocks

	LNA/Attenuator	Mixer	LPF	VGA	Total
Max. gain (dB)	14	18	0	54	86
Min. gain. (dB)	-22			42, 30	38,26
NF (dB)	3.5	23	40	20	12.2
IIP2 (dBm)	-	-	30	-10	29
IIP3 (dBm)	-15	-10	-5	-20	-37.1

Figure 3.20 shows the gain settings for different power input level. The LNA has a gain of 14dB up to input signal of -52dBm. Beyond this input level the LNA is turned off while an attenuator of -22dB replaces it. In each of these two sections the VGA is changing gain to keep the dynamic range of the signal at the demodulator input between -2dBm to 10dBm. Using these settings, the proper gain can be reached in only 3 steps. Also, through the setting, the signal level can be determined precisely within ±6dB of error as stated by the ED test of the IEEE 802.15.4.

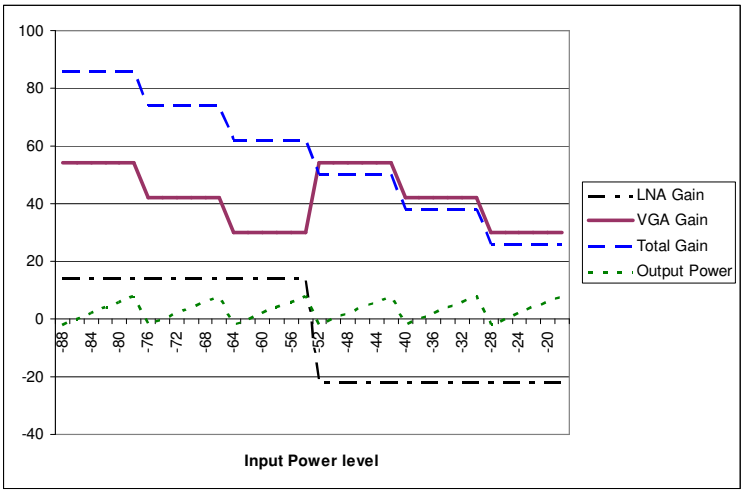


Figure 3.20 Gain Settings Versus Input Power Level

Figure 3.21 shows the NF and the SNR versus the input signal level, taking into account the gain changes. It is expected to have a jump in the NF when the attenuator is turned on, but the signal is high enough to keep the output SNR within the spec.

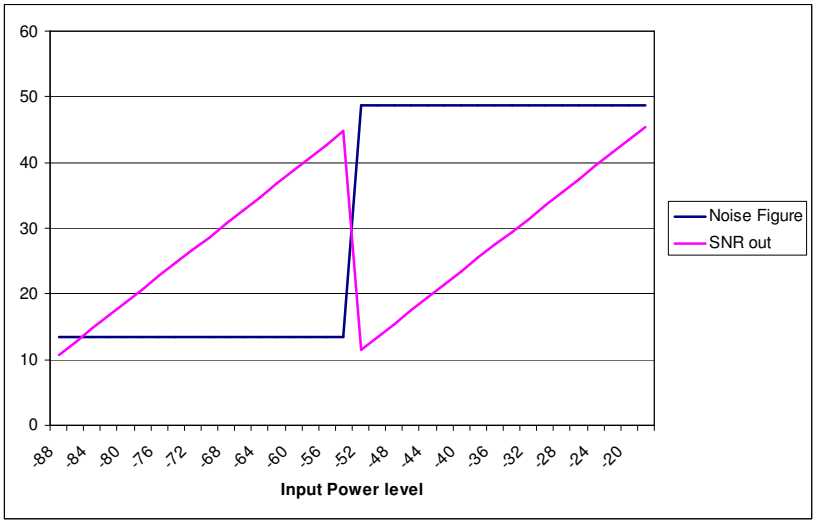


Figure 3.21 NF and SNRout

The overall IIP3 can be interpreted as a parallel combination of individual IIP3 contributions from different blocks as shown in equation (3.19). Figure 3.22 illustrates the IIP3 contributions of each block referred to the input of the LNA.

$$\frac{1}{iip3} = \frac{1}{iip3_{LNA}} + \frac{g_{LNA}}{iip3_{Mixer}} + \frac{g_{LNA}g_{Mixer}}{iip3_{LPF}} + \frac{g_{LNA}g_{Mixer}g_{LPF}}{iip3_{VGA-Calculated}}$$

$$\frac{1}{iip3} = \frac{1}{iip3_{LNA}} + \frac{1}{\frac{iip3_{Mixer}}{g_{LNA}}} + \frac{1}{\frac{iip3_{LPF}}{g_{LNA}g_{Mixer}}} + \frac{1}{\frac{iip3_{VGA-Calculated}}{g_{LNA}g_{Mixer}g_{LPF}}} \tag{3.19}$$

$$\frac{1}{iip3} = \frac{1}{iip3_{LNA-cont.}} + \frac{1}{iip3_{Mixer-cont.}} + \frac{1}{iip3_{LPF-cont.}} + \frac{1}{iip3_{VGA-Calculated-cont.}}$$

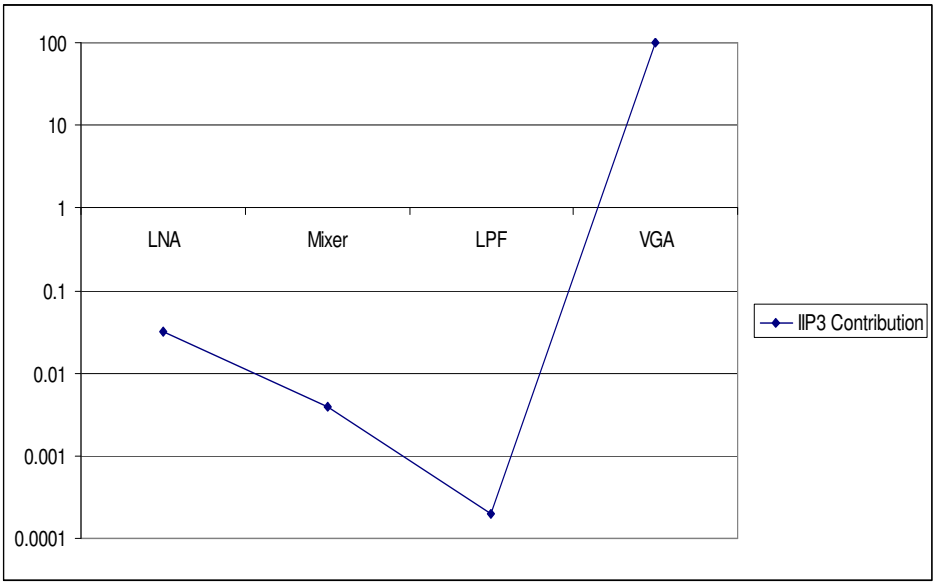


Figure 3.22 IIP3 Contributions

Figure 3.22 is very useful where it gives an insight where the linearity bottleneck occurs and where there is more design margin. It is shown clearly that the LPF represents the linearity bottle neck, such that any improvement will improve the overall system linearity. On the other hand, the VGA has a lot of linearity margin; it can degrade by 25dB without affecting the system linearity. The reason for this

comes from the fact that the LPF attenuates the adjacent and the alternate interferers drastically by 42dB and 60dB respectively.

The receiver system design concludes all the specifications of the building blocks including NF, Gain, IIp2 and IIP3. Following the transmitter system design where the transmitter chain specifications are determined with some synthesizer constraints.

3.3.2 Transmitter System Design

Direct conversion architecture is selected to implement the IEEE 802.15.4 transmitter to provide a low power solution. This relaxes the synthesizer complexity, as it is generating the same frequency carriers required by the corresponding receiver. Also, it decreases the number of the transmitter building blocks, thus reducing the spurious products resulting from the intermediate IF conversion. Super-heterodyne transmitters require off-chip passive components (IF filters) to suppress these spurious products, this comes on the expense of a one-chip solution and it increases the overall system cost [27-29]. Direct conversion transmitters may consume more power consumption, if the required gain is implemented in the RF section rather than the IF section in Super-heterodyne transmitters [26]. This can be compensated by having proper gain distribution between the Baseband section and RF section.

The selected architecture is shown in Figure 3.23, showing the modulator implementation as required by IEEE802.15.4 standard [3]. The bit stream after being mapped into chips as stated in Figure 3.4 using the DSSS mapping table shown in Table 2.2, the Chip rate becomes 2Mbps of chip duration (T_c). A splitter is used to create the I and Q data streams by taking the even chips to the I branch and the odd bits to the Q branch, creating two streams of 1Mbps each and with a chip duration ($2T_c$). Sine wave shaping is implemented on each channel before being up converted to the RF carrier using a fully differential fully balanced IQ up conversion Mixer. The inherent RF current addition in the Mixer makes the signal ready to be transmitted through the Power Amplifier (PA).

As mentioned in section 3.2, the IEEE 802.15.4 modulated signal is typically an MSK signal with constant amplitude and continuous phase. This relaxes the Power Amplifier linearity requirements, thus Class AB amplifier is used preceded by a preamplifier acts as a buffer between the up-conversion Mixer and the PA.

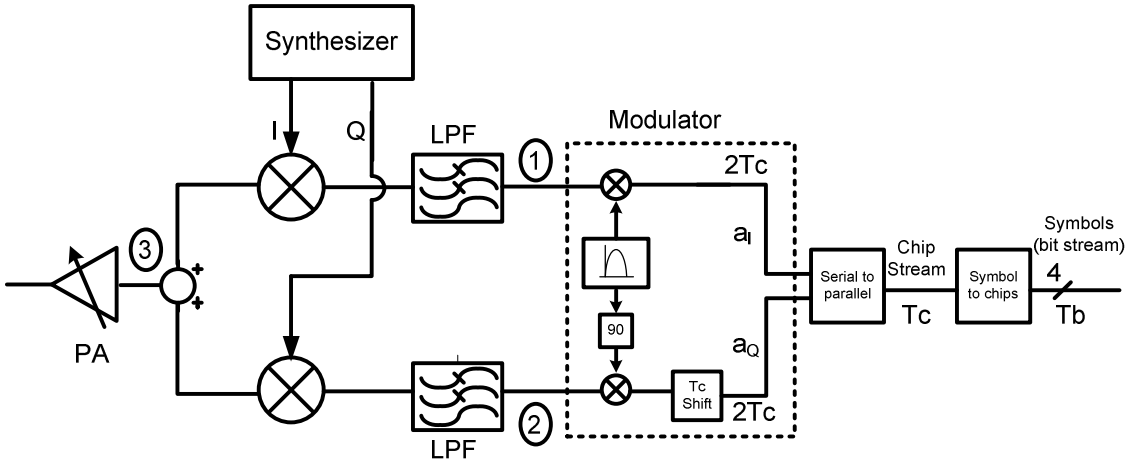


Figure 3.23 Transmitter Architecture

The signal at each point is shown in equation (3.20). For different TC durations the sine-wave shaping component can be positive or negative, and then it is multiplied by the chip equivalent resulting in a constant envelope signal with the data carried in its frequency component.

$$At1: \quad a_I \left| \sin\left(\frac{\pi t}{2T_c} \right) \right|$$

$$At2: \quad a_Q \left| \sin\left(\frac{\pi t}{2T_c} + \frac{\pi T_c}{2T_c} \right) \right| = a_Q \left| \cos\left(\frac{\pi t}{2T_c} \right) \right| \tag{3.20}$$

$$At3: \quad S = a_I \left| \sin\left(\frac{\pi t}{2T_c} \right) \right| \cos(w_c t) + a_Q \left| \cos\left(\frac{\pi t}{2T_c} \right) \right| \sin(w_c t) = \pm \sin\left(w_c t \pm \frac{\pi t}{2T_c} \right)$$

By implementing the modulator in SystemView and by using random data stream, Figure 3.24 shows the ideal Power Spectral Density (PSD) of the transmitted signal. The

Power Spectral Mask (PSM) required by IEEE802.15.4 standard [3] and mentioned in section 2.2.7 is shown on top of the PSD. The out of band signal power (3.5MHz away from the carrier) has to be -20dBc relative to the peak transmitted power. Also, it has an absolute limit in order not to exceed -30dBm.

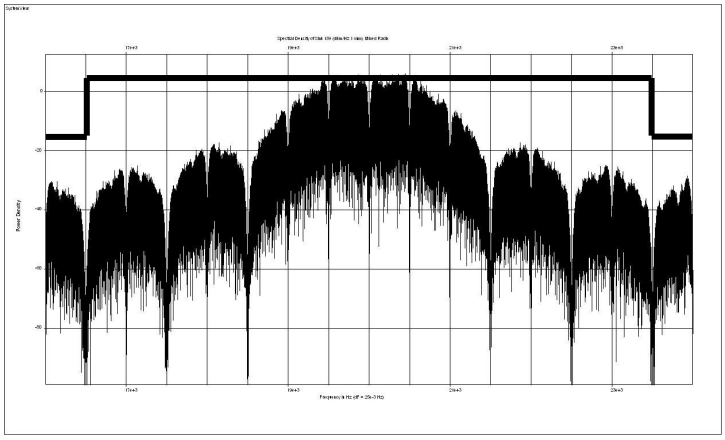


Figure 3.24 PSD/PSM of IEEE802.15.4

According to FCC regulations [3], the maximum transmitted power allowed in the 2.4GHz ISM band is 10dBm. For the ideal PSD shown in Figure 3.24, if the transmitted power increased to 10dBm, the signal side-lobes at 3.5MHz and beyond can easily reach -25dBm violating the absolute limit. Note that the relative limit will always hold in the ideal case. In order to achieve this maximum transmitted power, a LPF should be added at the modulator output to attenuate the side-lobes at 3.5MHz by at least 8dB (3dB of margin), taking into account the next stages nonlinearity. A pole for a first order LPF should be located at 1.4MHz, or a double pole for a second order LPF should be located at 2.2MHz to achieve the 8dB attenuation. As the pole frequency increases, distortion of the modulated signal decreases, improving the accuracy of the transmitted signal.

IEEE802.15.4 stated 0dBm as the nominal transmitted power; this relaxes the LPF BW to eliminate the higher order harmonics of the modulator only keeping the transmitted signal undistorted with a PSM margin of 5dB. This also saves area of LPF implementation since its cutoff frequency increased.

Other FCC regulations, interpreted by the IEEE802.15.4 standard [3], affects the frequency synthesizer phase noise, where the required phase noise at 3.5MHz is -92dBc and -102dBc for 0dBm and 10dBm transmitted power respectively. This is calculated based on the restricted band at 2483.5MHz to 2500MHz that does not allow any signal to be transmitted higher than -101.2dBm/Hz. The DSSS spreading gain of 9dB is used to relax the phase noise requirement.

A. Inband Modulation Accuracy

Transmitting an accurate signal is one of the most important features of a compliant transmitter. Standards specify the transmitted signal accuracy in terms of waveform quality factor (ρ); as a correlation between the actual and the ideal waveforms as in CDMA as stated in equation (3.21) [26, 30]. Z(t) is the actual waveform while R(t) is the ideal waveform.

$$\rho = \frac{\left|\sum_{k=1}^{M} R_k Z_k^*\right|^2}{\sum_{k=1}^{M}|R_k|^2 \sum_{k=1}^{M}|Z_k|^2} \tag{3.21}$$

Other standards specify the Error Vector Magnitude (EVM) as the accuracy measurement for the transmitted signal as IEEE802.15.4 [3]. EVM is the normalized mean square error between the transmitted and the actual signal as shown in equation (3.22). Where S is the magnitude of the ideal transmitted vector as shown in Figure 3.25.

$$EVM = \left[\frac{\frac{1}{N}\sum_{j=1}^{N}\left(\delta I_j^2 + \delta Q_j^2\right)}{S^2}\right]^{1/2} X100 \tag{3.22}$$

$$Where: \quad \left(\delta I_j, \delta Q_j\right) = \left(\tilde{I}_j, \tilde{Q}_j\right) - (I, Q)$$

$$and \quad S^2 = I^2 + Q^2 = ideal\ transmitted\ signal$$

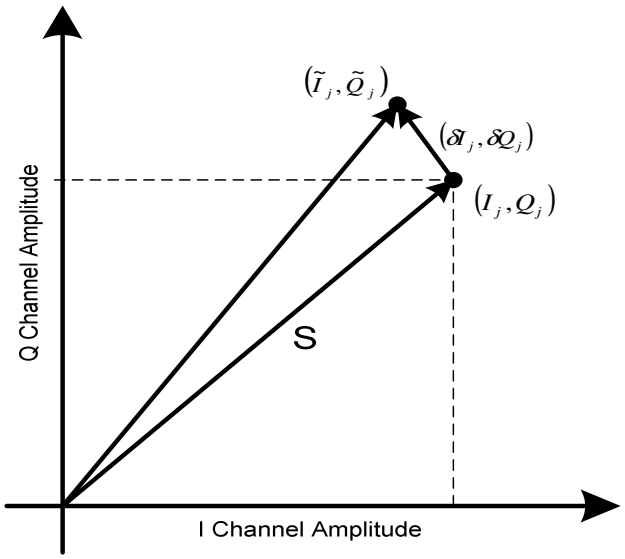


Figure 3.25 EVM Calculation of IEEE802.15.4

The relation between EVM and ρ is stated in equation (3.23) [31].

$$\rho \cong \frac{1}{1+EVM^2}, \; and \;\; EVM = \sqrt{\frac{1-\rho}{\rho}} \tag{3.23}$$

For IEEE802.15.4 compliant transmitter, EVM can be affected by Modulator accuracy, LPF transfer function, Upconversion Mixer IQ mismatch, LO phase noise, IQ channel mismatches, Carrier leakage, nonlinearity on the signal path, In-channel noise, and reverse modulation. Assuming all these random errors are uncorrelated, the resulted normalized mean square error is the summation of individual normalized mean square errors, giving the overall EVM shown in equation (3.24) [26]. All these non-idealities are explained next.

$$EVM_{\text{overall}} = \sqrt{\sum_i EVM_i^2} \tag{3.24}$$

IQ Signal Path Mismatches

Assuming one of the channels are the reference (e.g. I channel), thus mismatches between I signal path and Q signal path will be the deviation from this reference at the Q path.

Let α_1 be the gain error at the Q modulator, while θ_1 be the phase deviation from 90^o. Given that the LPF has a relatively high cut-off frequency, and by using layout techniques to achieve the proper matching between its passive components, the DC gain as well as the cut-off frequency can be assumed tracking with negligible error. Let's assume α_2 be the LO Q gain error with the up-conversion Mixer mismatch. While θ_2 be the IQ phase imbalance (deviation from 90^o). Equation (3.25) shows the RF signal to be transmitted including these errors, by removing the absolute values and include its sign in the a_I and a_q, and by ignoring the second order multiplication.

$$S = a_I \sin\left(\frac{\pi t}{2T_c}\right)\cos(w_c t) + (1+\alpha_1)(1+\alpha_2)a_Q \cos\left(\frac{\pi t}{2T_c} + \theta_1\right)\sin(w_c t + \theta_2)$$

$$= a_I \sin\left(\frac{\pi t}{2T_c}\right)\cos(w_c t) + (1+\alpha)a_Q \cos\left(\frac{\pi t}{2T_c} + \theta_1\right)\sin(w_c t + \theta_2) \quad (3.25)$$

where, $\alpha \cong \alpha_1 + \alpha_2$

Similarly, as derived in [26] for a regular OQPSK, the transmitted signal can be expressed in terms of an amplitude modulated desired signal, and another unwanted signal, as shown in equation (3.26). As a double check on the results, Ideally, $\theta_1 = \theta_2 = \alpha_1 = \alpha_2 = 0$, equation (3.27) shows the ideal transmitted signal based on I and Q components to cover the 4-point constellation.

$$S = \frac{A}{2}\sin\left(w_c t + \frac{\pi t}{2T_c} + \theta_3\right) - \frac{B}{2}\sin\left(w_c t - \frac{\pi t}{2T_c} - \theta_4\right)$$

$$\textit{Where},\ \theta_3 = \tan^{-1}\frac{a_Q(1+\alpha)\sin(\theta_1+\theta_2)}{a_I + a_Q(1+\alpha)\cos(\theta_1+\theta_2)}$$

$$\theta_4 = \tan^{-1}\frac{a_Q(1+\alpha)\sin(\theta_1-\theta_2)}{a_I - a_Q(1+\alpha)\cos(\theta_1-\theta_2)} \quad (3.26)$$

$$A = \sqrt{a_I^2 + 2a_I a_Q(1+\alpha)\cos(\theta_1+\theta_2) + a_Q^2(1+\alpha)^2}$$

$$B = \sqrt{a_I^2 - 2a_I a_Q(1+\alpha)\cos(\theta_1-\theta_2) + a_Q^2(1+\alpha)^2}$$

$$Ideally: \quad S = \frac{(a_I + a_Q)}{2}\sin\left(w_c t + \frac{\pi t}{2T_c}\right) - \frac{(a_I - a_Q)}{2}\sin\left(w_c t - \frac{\pi t}{2T_c}\right) \tag{3.27}$$

The EVM can be simplified as shown in equation (3.28), by ignoring θ_3 and θ_4, it matches the result reported in [26], and by assuming one of the existing data cases, where $a_I=a_Q=1$.

$$\begin{aligned} EVM_{mm} &= \sqrt{\frac{a_I^2 - 2a_I a_Q(1+\alpha)\cos(\theta_1 - \theta_2) + a_Q^2(1+\alpha)^2}{a_I^2 + 2a_I a_Q(1+\alpha)\cos(\theta_1 + \theta_2) + a_Q^2(1+\alpha)^2}} \\ &= \sqrt{\frac{1 - 2(1+\alpha)\cos(\theta_1 - \theta_2) + (1+\alpha)^2}{1 + 2(1+\alpha)\cos(\theta_1 + \theta_2) + (1+\alpha)^2}} \end{aligned} \tag{3.28}$$

For a modulator I and Q gain mismatch of 5% (α_1), modulator I and Q phase mismatch of 5^o (θ_1), LO I and Q gain mismatch of 11% (α_2), and LO I and Q phase mismatch of 10^o (θ_2), EVM_{mm} of 8.66% is obtained.

LO Phase Noise

Phase noise can be represented instantaneously by a phase shift (θ) in both I and Q LO signals preserving on their orthogonal relation. This will result in the same phase shift in the transmitted signal. The error vector is shown in equation (3.29) derived from Figure 3.26, by assuming $a_I=a_Q=1$.

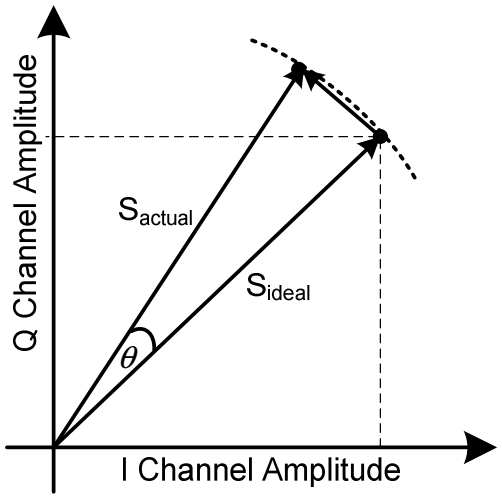


Figure 3.26 LO Phase Noise Effect on EVM

$$\left|error\right|^2 = \left|\sin\left(w_c t + \frac{\pi t}{2T_c} + \theta\right) - \sin\left(w_c t + \frac{\pi t}{2T_c}\right)\right|^2$$

$$= \left|\bar{S}_1 - \bar{S}_2\right|^2 = S^2 + S^2 - 2S^2\cos(\theta) \tag{3.29}$$

$$= 2 - 2\cos(\theta) = 4\left(\frac{1}{2} - \frac{1}{2}\cos\left(2\frac{\theta}{2}\right)\right) = 4\sin^2\left(\frac{\theta}{2}\right) \cong \theta^2$$

The expectation of θ^2 is the auto-correlation function of the synthesizer phase noise, which can be reduced to Power spectral density integration over the synthesizer loop bandwidth. The EVM results from the Synthesizer phase noise is shown in equation (3.30) [26].

$$EVM_{PN} = \sqrt{PN_{power}} \cong \sqrt{2 \cdot 10^{\frac{N_{phase}}{10}} BW}$$

$$Where: N_{phase} = average\ phase\ noise\ (dBc/Hz) \tag{3.30}$$

$$BW = Synthesizer\ loop\ BW\ \ (Hz)$$

For an average close-in phase noise of -70dBc/Hz, where the synthesizer loop BW is 30kHz, an EVM_{PN} of 7.75% is obtained.

LO Carrier Leakage

Any DC component leakage at the up-conversion Mixer input, will lead to a carrier transmission, as shown in Figure 3.27. This carrier leakage will deteriorate the signal accuracy by the ratio of its power to the ideal signal power.

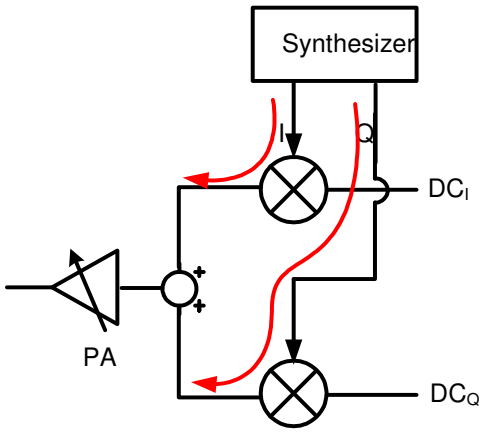


Figure 3.27 DC Leakage Causing Output Carrier Leakage

For DC_I and DC_Q leakage, the results transmitted signal is shown in equation (3.31), by taking the $a_I=a_Q=1$, and by analyzing the signal at the proper bit duration where both absolute values are positive quantities.

$$\begin{aligned} S &= \left(DC_I + \sin\left(\frac{\pi t}{2T_c} \right) \right) \cos(w_c t) + \left(DC_Q + \cos\left(\frac{\pi t}{2T_c} \right) \right) \sin(w_c t) \\ &\cong \overline{S}_{ideal} + DC\cos(w_c t + \theta) \end{aligned} \tag{3.31}$$

$$Where:\ S_{ideal}\ is\ the\ ideal\ transmitted\ signal\ vector$$

$$DC = \sqrt{DC_I{}^2 + DC_Q{}^2}, \qquad \theta = \tan^{-1}\frac{DC_Q}{DC_I}$$

Since DC_I and DC_Q are dc components, therefore θ is equal to zero. Thus the EVM_{DC} can be approximated as shown in equation (3.32). For a DC leakage on the modulator output for each branch (I and Q) of 5% of the signal of interest, an EVM_{DC} of 7.07 % can be estimated.

$$EVM_{DC} = \sqrt{\frac{carrier\ power}{signal\ power}} = \frac{DC}{V_{\max,\,ideal\ signal}} \tag{3.32}$$

PA Linearity

Mainly the 1dBc point is the main contributor to the modulated signal inaccuracy. As the transmitted signal is higher than the PA output 1dBc point, the signal bandwidth

can be divided into many sub-BW, each will experience different attenuation factors depending on its amplitude, thus distorting the modulation accuracy. This error can be easily ignored by having the PA output 1dBc point higher than 0dBm.

In-Band Noise

The in-band noise can affect the signal accuracy for low transmitted signal power only (-20dBm and below). This can be viewed as the same effect as the channel noise or the receiver noise, where it reduces the SNR thus degrading the BER at the receiver. For IEEE 802.15.4, the nominal transmitted power is 0dBm, while the minimum transmitted power is -3dBm. Thus the In-band noise effect on the transmission accuracy can be ignored.

Reverse Modulation

Coupling can occur between the transmitted signal and the LO signal at the up-conversion Mixer input, and defined as *Reverse Modulation* [26] as shown in Figure 3.28. This changes the ideality of the LO signal leading to equation (3.33), where α is the coupling coefficient. Thus the ratio of the error signal to the ideal signal (EVM) is the ratio of coupled power to the LO power at the up-conversion Mixer input, as shown in equation (3.34).

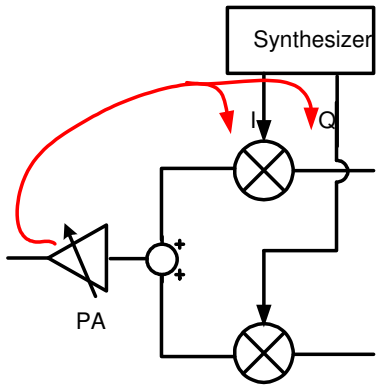


Figure 3.28 Reverse Modulation in a Direct Conversion Transmitter

$$LO_{mixer\_input} = LO_{ideal} + \alpha \cdot S_{transmitted} \tag{3.33}$$

$$EVM_{RM} = \sqrt{10^{\frac{\alpha_{dB} + S_{transmitted-dB} - LO_{ideal-dB}}{10}}} \tag{3.34}$$

In the proposed architecture, a preamplifier stage is introduced at the input of the PA to provide the necessary isolation. Meanwhile, careful layout is done to have as low coupling as possible through all parasitic elements. For IEEE802.15.4 the nominal transmitted power is 0 dBm, and by having a -12dBm LO power at each switch of the upconversion Mixer, the minimum allowed isolation can be set to 30dB to achieve and EVM_{RM} of 12.59 %.

Using the presented calculated EVM for each non-ideality, the overall expected EVM can be calculated as in equation (3.35) to be 18.5 %. This gives a 11.5 % as a design margin from the targeted EVM (30 %).

$$EVM_{RM} = \sqrt{EVM_{MM}{}^2 + EVM_{PN}{}^2 + EVM_{DC}{}^2 + EVM_{RM}{}^2}$$

$$= \sqrt{0.0866^2 + 0.0775^2 + 0.0707^2 + 0.01259^2} \quad (3.35)$$

$$= 18.5\%$$

B. Out of Band Emissions

The out of band emissions are controlled by the Power Spectral Mask (PSM), beside other restricted bands that may exist close to the IEEE 802.15.4 frequency band. Due to the nonlinearity of the transmitter, a phenomenon called *Spectral Regrowth* occurs, where the out of band side lobes' power increases violating the PSM requirement. The out of band emissions are dominated by the Spectral Regrowth. Figure 3.29 illustrates the spectral regrowth mechanism using a two tone approximation. One way to measure the spectral regrowth is to measure the adjacent channel power transmitted ratio to the actual channel power transmitted, defined as Adjacent Channel Power Ratio (*ACPR*).

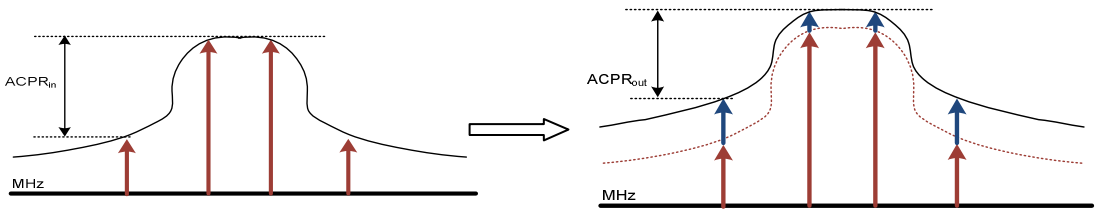


Figure 3.29 Spectral Regrowth Using a Two-tone Approximation

The $ACPR_i$ at the transmitter input (output of the modulator) is the ideal signal rejection of -35dB, as shown in Figure 3.19. For a 0dBm nominal transmitted power, the $ACPR_o$ required at the output of the transmitter is -30dBc, leaving only a margin of 5dB. Given these two values, the OIP_3 of the transmitter can be calculated from equation (3.36) [26] to be 11dBm.

$$OIP_3 = Tx + \frac{1}{2}\left(C - 10\log\left[10^{\frac{ACPR_o}{10}} - 10^{\frac{ACPR_i}{10}} \right] \right) \tag{3.36}$$

Given the required OIP3, the building blocks (up-conversion Mixer and PA) IIP3 can be calculated from individual gain values using equation (3.37).

$$OIP_3\big|_{dB} = -10\log\left(\frac{1}{P_{OIP-PA}} + \frac{1}{P_{OIP-mixer} G_{PA}} \right) \tag{3.37}$$

Out-of band noise emission can be calculated using the output noise power equation derived from the noise Figure calculations. For such a relaxed PSM of IEEE 802.15.4, the noise emissions can be ignored and dominated by the spectral regrowth.

Synthesizer Phase noise affects the out-of-band transmitted copies of the signal. IEEE 802.15.4 requires a transmitter synthesizer phase noise of -92dBm at 3.5MHz for a 0dBm transmitted power, taking into account restricted bands beyond 2.48GHz.

C. Gain Distribution

Gain budget distribution controls the out of band emissions. As the gain increase on RF stages, the overall linearity improves leading to lower spectral regrowth. While as the gain at Base-Band stages increases, the noise emission relative to the output power decreases. The overall gain required by the transmitter is simply the addition of individual gain stages.

D. Transmitter Overall Building Block Specifications

By following the transmitter design flowchart shown in Figure 3.30, as illustrated through out section 3.3.2, the overall building blocks specifications are shown in Table 3.6.

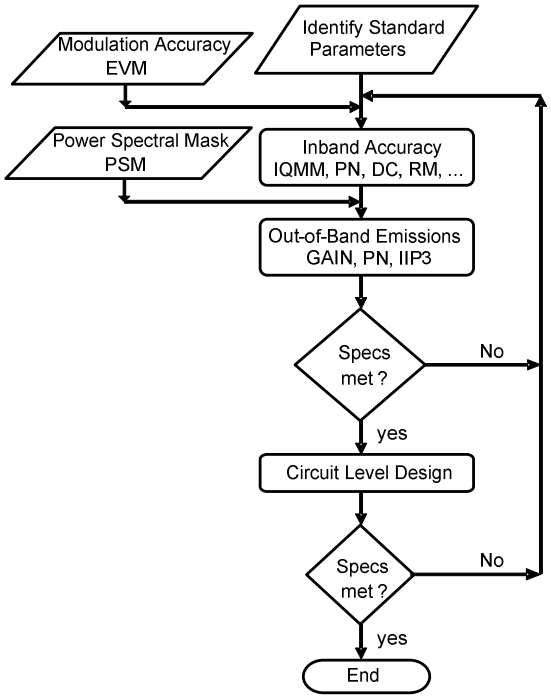


Figure 3.30 Transmitter System Design Flowchart

Table 3.6 Specifications for Different Transmitter Building Blocks

	Specifications	
Modulator	Gain Mismatch	5%
	Phase Mismatch	5^{o}
	Linearity (HD3)	-51dBc
Frequency Synthesizer	Phase Noise @ 3.5MHz	-92dBc/Hz
	Average close-in Phase Noise	-70dBc
	I-Q Phase MM	10^{o}
	I-Q Gain MM	11%
	Spur rejection @ 5MHz	-35dBc
Up-Conversion Mixer	Gain	-2dB
	IIP3	5dBm
Power Amplifier	Gain	12dB
	IIP3	-1dBm
Transmitted Signal isolation to LO output		30dB
DC leakage at modulator output		5%

3.4 Conclusions

A detailed system design procedure is introduced for an IEEE 802.15.4 standard compliant transceiver suitable for ZIGBEE applications. All building blocks' specs are derived using equations, Matlab codes, SystemView simulations, and Excel sheet relations. Frequency synthesizer building block is getting specifications from the receiver as well as the transmitter, where the tighter should apply

CHAPTER IV

IEEE 802.15.4/ZIGBEE: TRANCEIVER IMPLEMENTATION

4.1 Background and Motivation

IEEE 802.15.4/ZIGBEE standard is tailored for low power consumption, low cost applications. System level design is done taking these guidelines into accounts to have the architecture with the lowest possible power consumption and relaxed building blocks' specifications. Straight forward implementations of these building blocks are not required as they have high or moderate power consumptions. Low power implementations are the key issue in obtaining the low power solution aimed for.

4.2 Transceiver Building Blocks

A direct conversion receiver as shown in Figure 4.1, consists of an RF front end; LNA and down conversion Mixer, a BPF to remove the DC component of the signal as well as most of the flicker noise power generated by the Mixer. Also the BPF is used as a channel filter to limit the interferers' power and the out of band noise. An attenuator stage is added to bypass the LNA in case of large signal power, to avoid saturating the RF stages, otherwise highly linear circuits has to be implemented increasing the power consumption drastically. A Variable Gain Amplifier (VGA) with three gain stages is placed before the demodulator, to adjust the signal amplitude to fit in the demodulator

dynamic range for optimum data recovery. Also the gain steps are chosen in a way to inherently implement the ED function (RSSI) stated by IEEE 802.15.4 with a simple overhead comparator. Finally an optimum demodulator is implemented by matching the input data and comparing the output with a reference detecting the data transmitted.

On the other hand, the direct conversion transmitter shown in Figure 4.1, consists of the IQ modulators followed by LPF to remove its higher order harmonics. The Quadrature up-conversion Mixer has a differential-input, single-ended output to derive the preamplifier and thus the single-ended Power Amplifier.

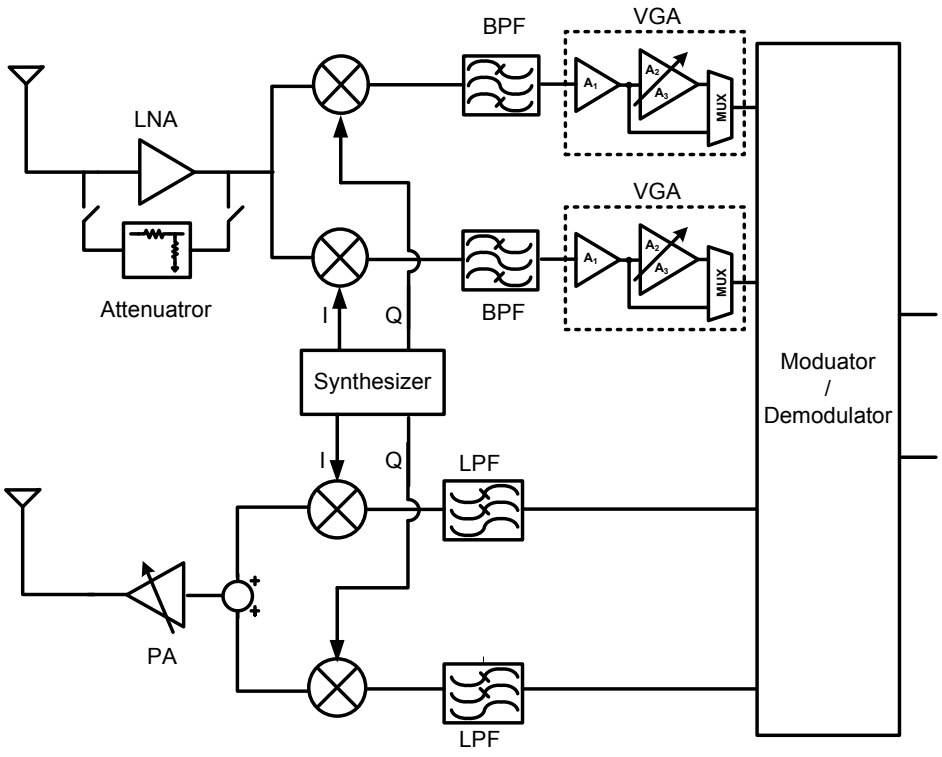


Figure 4.1 Transceiver Architecture

4.3 Receiver RF Front End

The RF front end design is the heart of the receiver; it controls its NF, performance and power consumption. A low noise low power front end leads to a low cost receiver. Many low power front end architectures are reported for various applications.

4.3.1 Proposed Implementation

The required specifications for the RF front end are shown in Table 4.1, where an overall gain of 32dB should be achieved, with a NF of 10dB and a linearity of -24.5dBm.

Table 4.1 Receiver RF Front End Specifications

	Gain	NF	IIP3
LNA	14dB	3.5dB	-15dBm
Mixer	18dB	23dB	-10dBm
Overall	32dB	10.06dB	-24.5dBm

A stacked LNA/Mixer implementation has been reported in [29] for a single ended common source LNA to reuse the DC current (I_{DC}) from a single supply terminal (VDD), reducing the overall power consumption. A similar architecture has been implemented for a fully differential CG LNA, with an attenuator bypass and a folded cascode Mixer output stage . The stacked block diagram is shown in Figure 4.2.

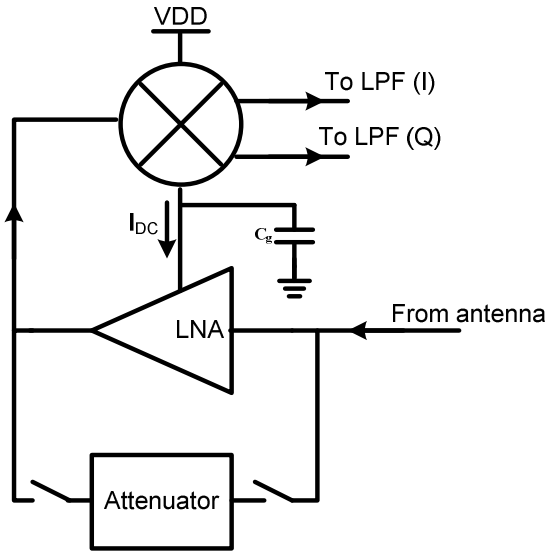


Figure 4.2 Stacked RF front end Block Diagram

A decoupling cap is connected at the intermediate point to keep it AC ground [29] at the frequency of operation. The Mixer input to its ground to the LNA output causes a closed loop that has the potential to oscillate. Careful choice of the intermediate capacitor shorts the loop to ground and thus no oscillations occur. Also, it may affect the Mixer gain as a source of degeneration.

All bias lines are connected to the pads through a small resistance, to avoid resonance at any terminal causing oscillations.

4.3.2 LNA Circuit Implementation

Common Gate (CG) architecture is chosen over common source architecture. Common Source (CS) can provide low noise performance with some noise cancellation techniques as in [32] or by using extra gate source capacitance as in [33, 34] to relax the inductor value, with effective Gm. On the other hand, its matching is more parasitic sensitive (process, voltage, and temperature variation dependent). Miller effect exists at its input stage, leading to cascode implementations to increase the reverse isolation, consuming more voltage headroom and more power. Also, CS requires extra source degenerated on-chip inductors (for 2.4GHz frequency range), demanding more are and thus extra chip cost.

For the relaxed NF required by the IEEE802.15.4, CG architectures become the best option for low power, low cost implementation. Figure 4.3 shows the CG-LNA implementation in standard 0.18um TSMC technology. A capacitor bank is used at the LNA output for Gain tuning to achieve a flat gain on the 2.4GHz IEEE 802.15.4, frequency band.

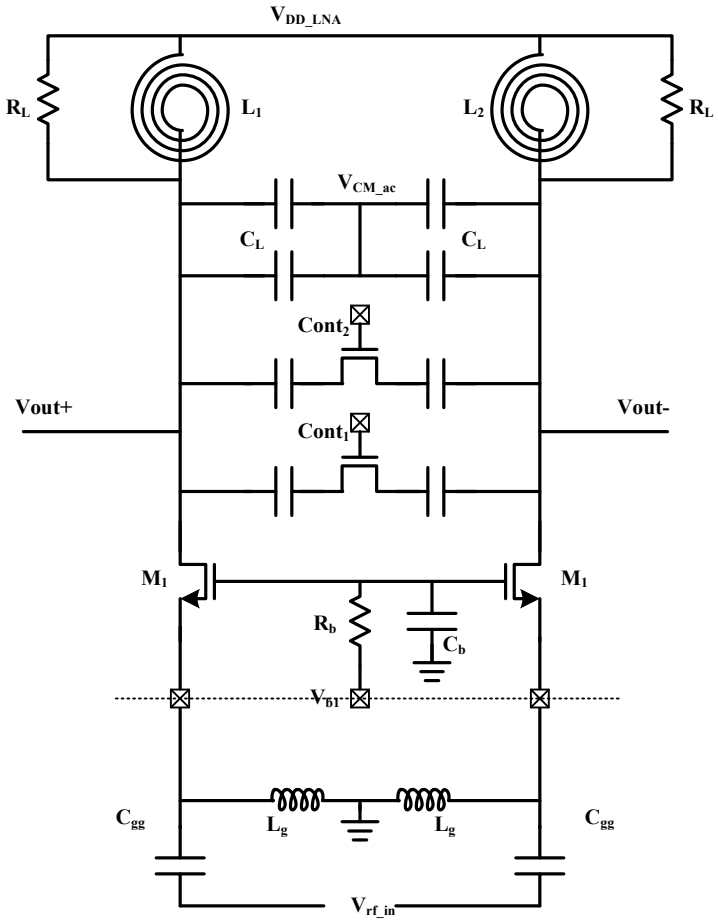


Figure 4.3 LNA Circuit Iimplementation

LNA gain is defined by equation (4.1), for proper matching g_m is designed to be 1/25mS. Noise factor for a single-ended CG LNA is defined by equation (4.2) [35].

$$G = g_m Z_L = \sqrt{2\mu_n C_{ox} \frac{w}{L} I_{DC}} \cdot \left(jwL // R_L // \frac{1}{jwC} \right) \tag{4.1}$$

$$F = 1 + \frac{\gamma}{\alpha}\frac{1}{g_m R_s} = 1 + \frac{\gamma}{\alpha}\frac{1}{R_s\sqrt{2\mu_n C_{ox}\frac{w}{L}I_{DC}}} \tag{4.2}$$

For the pseudo-differential architecture used, the noise generated is doubled while the matching is performed to (Rs/2) rather than Rs, leading to a g_mRs value of 2.

IIP3 is mainly dependent on (V_{GS}-V_t) as shown in equation (4.3) for a single MOS transistor.

$$iip3 = \left(\frac{4 \cdot \left(1 + \left(\theta + \frac{\mu_o}{V_{sat}L}\right)\left(V_{gs} - V_t\right)\right)^2 \cdot \left(2 + \left(\theta + \frac{\mu_o}{V_{sat}L}\right)\left(V_{gs} - V_t\right)\right) \cdot \left(V_{gs} - V_t\right)}{\left(\theta + \frac{\mu_o}{V_{sat}L}\right)} \right)^{1/2} \tag{4.3}$$

L_{min} is used to maximize the F_T improving the phase noise by minimizing the gate area and consequently C_{gs}. Moreover, L_{min} minimizes IDC required to achieve the gm of matching. A gm of 40mS is used to achieve the proper matching. W/L of the input pair is designed to be 625 with L=0.4um. For a load capacitance of 1pF, and inductor is chosen to be 4nH to maximize the gain in the band of interest. Beside the tuning capacitor bank, a physical resistor is added to flatten the gain and make it almost uniform in the ZIGBEE band.

Lg and Cgg are offchip passive components, which are used to cancel out the package parasitics and keep the input matching accurate.

4.3.3 Mixer Circuit Implementation

A fully differential fully balanced IQ quadrature Gilbert cell is used, with a folded cascode output stage to have a better linearity without increasing the required voltage headroom. Figure 4.4 shows the Mixer circuit implementation.

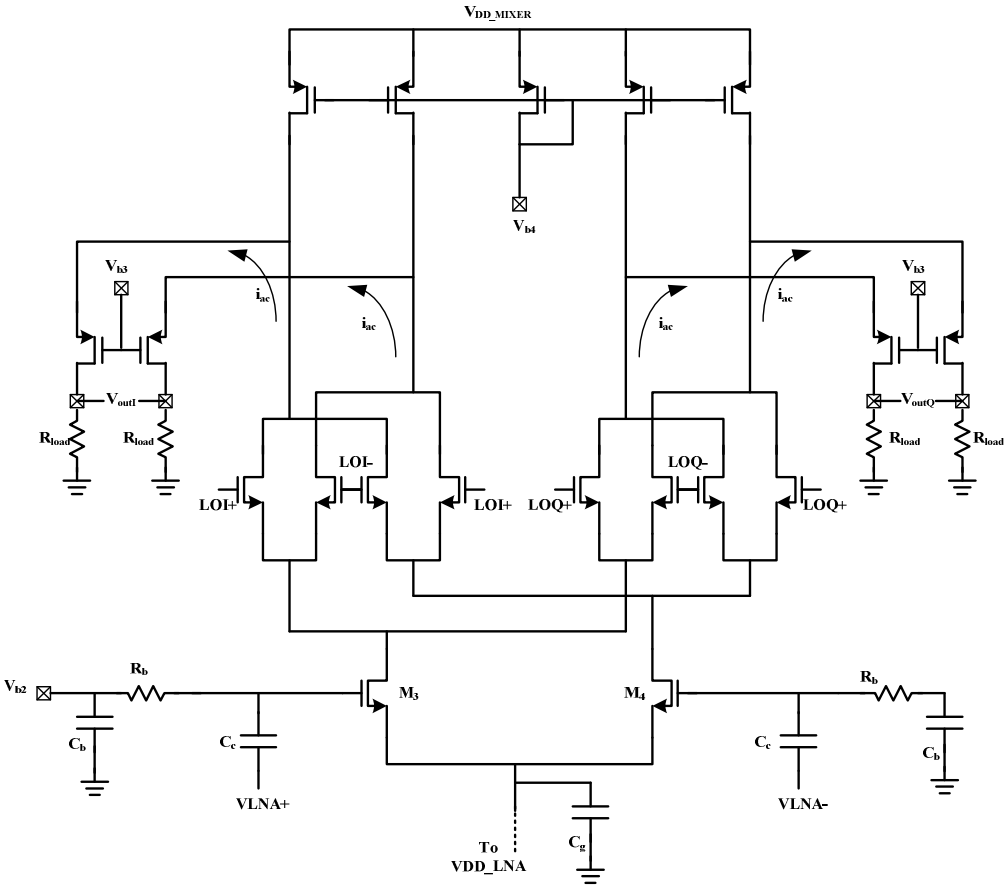


Figure 4.4 Mixer Circuit Iimplementation

The Mixer gain is mainly determined by its input stage gain, assuming proper LO swing capable of completely turning on and off the mixer switches. Mixer gain is given by equation (4.4). Since the RF Mixer current is split between the I and Q branches, the gm_{eff} is half the input stage gm. The input Gain stage has a maximum gain to reduce the switches contribution to the mixer noise.

$$Gain = \frac{4}{\pi} g_{m-eff} = \frac{2}{\pi} g_{m-rf} \tag{4.4}$$

As a first order approximation for the Mixer linearity, and assuming ideal switching, $(V_{GS}-V_t)$ of the input RF stage controls the IIP3 of the Mixer. Equation (4.5) shows the IIP3 of the fully-differential fully-balanced Mixer [36].

$$iip3 = \frac{4 \cdot \left[1 + \theta\left(V_{gs} - V_t\right)\right]^2 \cdot \left[2 + \theta\left(V_{gs} - V_t\right)\right] \cdot \left(V_{gs} - V_t\right)}{3\theta} \tag{4.5}$$

For a zero-IF receiver, down-conversion output noise is the sum of (1) mixer input stage thermal noise, (2) switches thermal noise, (3) resistive load thermal noise, and (4) switches flicker noise. The flicker noise is directly proportional to the DC current, thus reducing the DC current minimizes the flicker noise contribution. This is achieved by splitting the same mixer current onto the 8 switches of I and Q branches. Moreover, having a HPF at the output of the mixer eliminates most of the flicker noise preserving on the received signal integration.

The thermal noise contributions can be approximated as shown in equation (4.6) [37]. Where I is the DC current per LO switch, and A is the LO amplitude. By reducing the switches current and increasing the LO amplitude, the switch thermal noise becomes insignificant.

$$v_{on}^{\ 2} = \underbrace{8KTR_L}_{\text{Resistive load}} + \underbrace{16KTR_L^{\ 2}\gamma\frac{I}{\pi A}}_{\text{LO switch}} + \underbrace{8KT\gamma g_m R_L^{\ 2}}_{\text{Input stage}} \tag{4.6}$$

A high VDSAT of the input stage is chosen for higher linearity, and a large L for better matching. Large switches sizes are required to have lower VDSAT for the same current consumption. This makes the switches completely turned OFF and ON for the same LO amplitude. Thus it acts as a cascade device rather than a differential pair which reduces their noise contributions.

Layout matching techniques are used is minimize the IQ signal paths mismatch. The layout is an exact mirror around its vertical axis to have the entire parasitic routing identical as well as different signal coupling (if any). Large differential signals are routed closely to each others to reduce their coupling to other signals.

The feedback loop from the LNA output to the Mixer input to the Mixer virtual ground and back to the LNA output has to be open at all frequencies. The intermediate decoupling capacitor has very low impedance at the IEEE 802.15.4 frequency band, thus

shorting the loop to ground. On the other hand, the coupling capacitor value is optimized to keep the loop opened at lower frequencies without having much attenuation for the RF signal. Attenuation occurs due to the potential divider formed by the decoupling capacitor and the C_{gs} of the Mixer input stage.

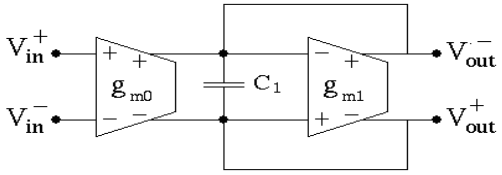
4.4 Third Order Butterworth Filter

As discussed in the Receiver system level design, a third-order butterworth LPF is required at the output of the Mixer after the passive single-pole HPF. Table 4.2 shows the required LPF specifications, as driven from the system design analysis.

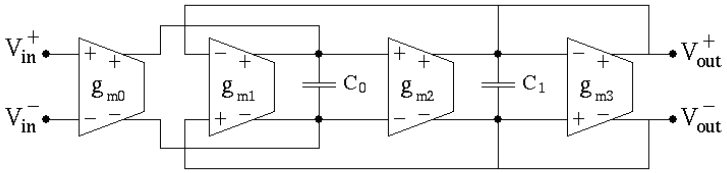
Table 4.2 LPF Specifications

	Gain	BW	NF	IIP2	IIP3
LPF	0dB	1MHz	40dB	30dBm	-5dBm

OTA-C type of filter is selected because it can achieve low power consumption and low distortion simultaneously. A fully differential structure is expected to reduce even order distortion. The architecture used is shown in Figure 4.5.



(a)



(b)

Figure 4.5 LPF Architecture (a)First Stage (b)Second Stage.

A PMOS differential pair is used, as shown in Figure 4.6, at each stage since it has lower flicker noise, larger slew rate for the same gm/c_L. On the other hand it has a lower non-dominant pole frequency, leading to a large excess phase. For Common mode feedback, a simple CMFB circuit is used to control Vcntrl. It uses the virtual ground point of the following stage input pair as the common mode detection point [38].

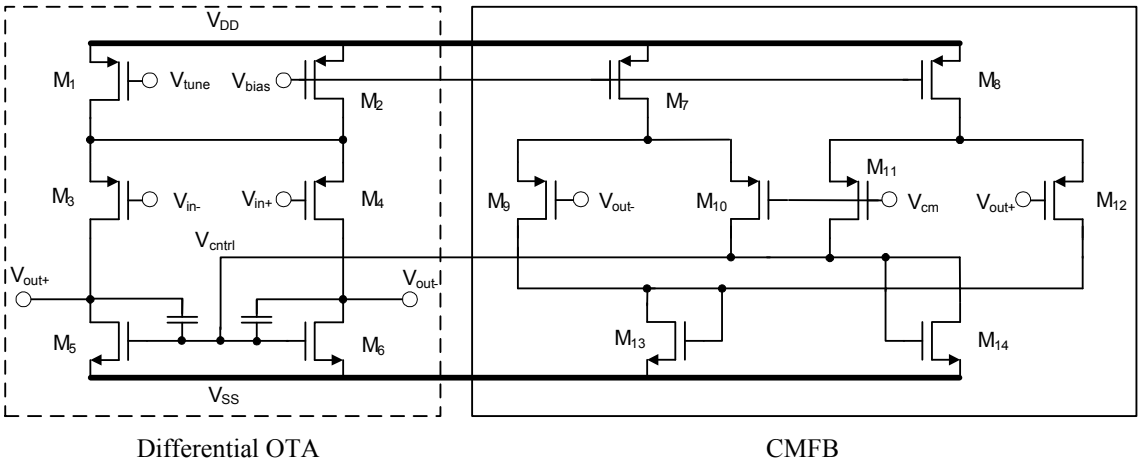


Figure 4.6 Differential OTA

Gm/C is designed to be 6.3 μS/pF. The noise contributors are thermal noise and flicker noise. Since the integrated thermal noise of the gm/C filter is proportional to kT/C, C value of 4pF is chosen to meet noise requirement, hence gm equals 25μS. Increasing C value helps reduce the thermal noise contribution, and the flicker noise can be reduced by increasing the device size. The BW is determined by gm/C, while the filter linearity is dependent on the gm cell (i.e. overdrive voltage and output voltage headroom).

4.5 Variable Gain Amplifier

IEEE 802.15.4 requires less number of steps for the VGA as derived in the Receiver system design. A VGA of three gain steps only is required. Table 4.3 shows the required VGA specifications.

Table 4.3 VGA Specifications

	Gain	NF	IIP2	IIP3
VGA	54, 42, and 30dB	20dB	-10dBm	-20dBm

The overall system is shown in Figure 4.7. The gain is split into two stages. The first stage has gain of 30dB and the second one has variable gain of 12dB or 24dB. This architecture reduces the sizes of the varying resistors, keeping the bandwidth variation to a minimum, and reducing the overall noise.

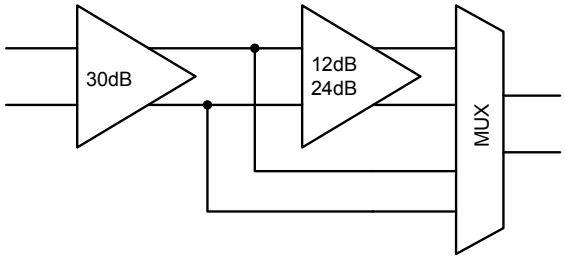


Figure 4.7 Proposed VGA Block Diagram

For each gain stage implementation, the proposed solution follows a similar approach as reported in [39] A transimpedance approach has also been reported in [40] and has proved very attractive for low voltage applications. In this work, a transconductance stage is embedded into a transimpedance stage to create a single stage VGA. The basic structure is shown in Figure 4.8. The transconductance stage is realized by a differential pair with source degeneration (M1, M2, and R_{SD}). This input stage has an effective transconductance based on the differential pair transconductance and the source degeneration resistance, along with a feedback loop, as shown in equation (4.7).

$$G_m = \frac{g_{m1}g_{m2}}{g_{o1} + g_{m1}g_{m2}R_{SD}} \approx \frac{1}{R_{SD}} \tag{4.7}$$

Using a transimpedance output stage guarantees a fixed bandwidth across the dynamic range. The transimpedance stage is realized by M1, M2, M3, and M4. Since M2 - M1 create a voltage buffer as in [41], any V_{in} variation generates a differential voltage across R_{SD}. This, in turn, will create a current flowing into the drain of M2. This can be analyzed as the input of the transimpedance amplifier.

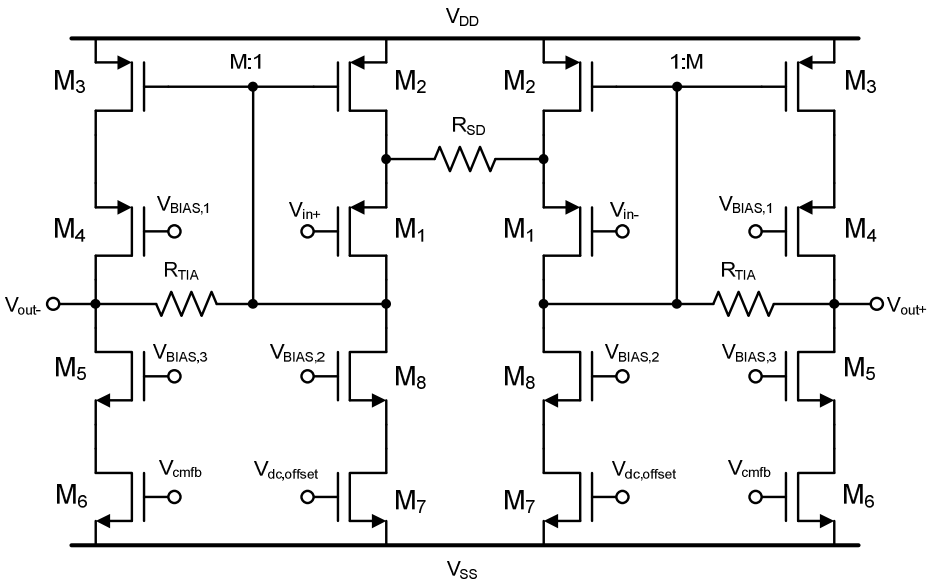


Figure 4.8 VGA Basic Stage Structure

The transimpedance gain is given by equation (4.8)

$$R_m = \frac{g_{TIA} - Mg_{m2}}{g_{TIA}g_{m2}(1+M)} \approx -\frac{1}{g_{TIA}}\bigg|_{as\ current\ gain\ increases} = -R_{TIA} \tag{4.8}$$

For the second stage, the two gain steps 12dB and 24dB can be achieved by several means; (1) Changing the effective transconductance by varying the values of R_{SD}, (2) Changing the amount of transimpedance current amplification M, (3) Changing the transimpedance gain R_{TIA}, or a combination of these. Each of these options has its own tradeoff. Any change in R_{SD} affects the system noise drastically, while M clearly impacts the system power consumption, and R_{TIA} controls not only the gain but also the system's effective badwidth. The final choice among these was the variation of the transimpedance, since the systems inherent bandwidth exceed the required 2MHz allowing for this tradeoff to be acceptable.

As in open loop system, especially high gain structures, any differential DC offset may saturate the VGA output. The proposed solution has a DC feedback loop to eliminate such offset. This loop inlcudes a passive RC low pass filter whose output is fed into a differential pair. The differential pair generates a voltage to eliminate the detected output offset by negating its effects at the transconductance stage. Since this approach will also eliminate part of the Zero-IF signal the pole of the feedback effect is limited to 5kHz which only degrades the BER by 0.5dB as shown in the system level design analysis. The implemented version is shown in Figure 4.9 where the large valued resistors are implemented by triode transistors.

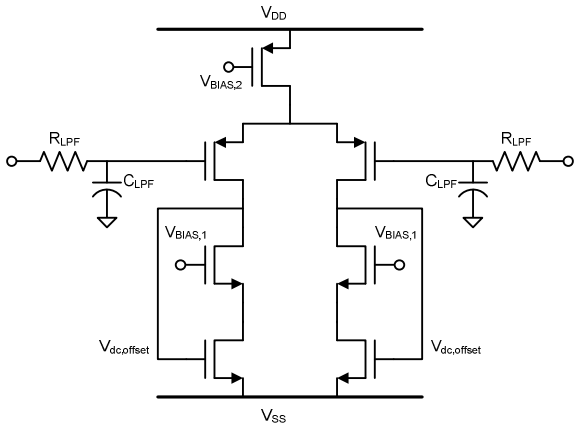


Figure 4.9 DC Offset Cancellation Schematic

4.6 Offset-QPSK Demodulator

Block and circuit diagrams of the optimum ZIGBEE demodulator [42] are shown in Figure 4.10. Where, the sine wave generator, multiplier and integrator can be combined into one circuit.

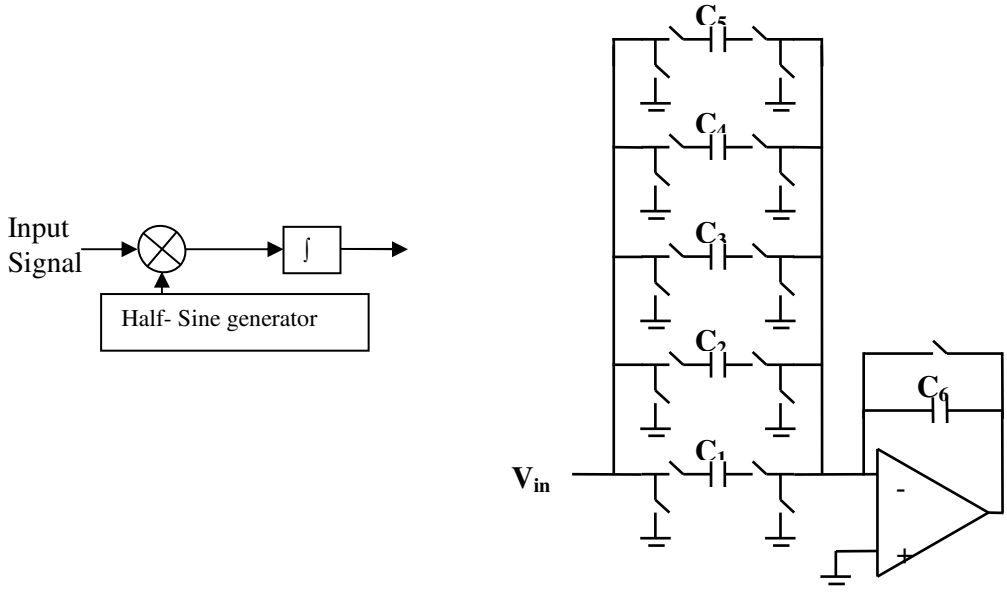


Figure 4.10 ZIGBEE Demodulator.

The weights of the multiplication are realized by the capacitor bank that have the values shown in equation (4.9).

$$\frac{C_5}{C_6}=\sin\left(\frac{\pi}{10}\right),\ \frac{C_4}{C_6}=\sin\left(\frac{2\pi}{10}\right),\ \frac{C_3}{C_6}=\sin\left(\frac{3\pi}{10}\right),\ \frac{C_2}{C_6}=\sin\left(\frac{4\pi}{10}\right),\ \frac{C_1}{C_6}=\sin\left(\frac{5\pi}{10}\right) \quad (4.9)$$

Thus, the circuit multiplies the received signal by different weights equivalent to the samples of sine wave, as the number of samples of this sine wave increases, the accuracy of the demodulator decreases but the total number of the capacitors used increases. The SNR of the demodulator improves as the number of samples increases; the SNR versus number of samples in each half cycle of sine wave is shown in Figure 4.11 using MATLAB simulation.

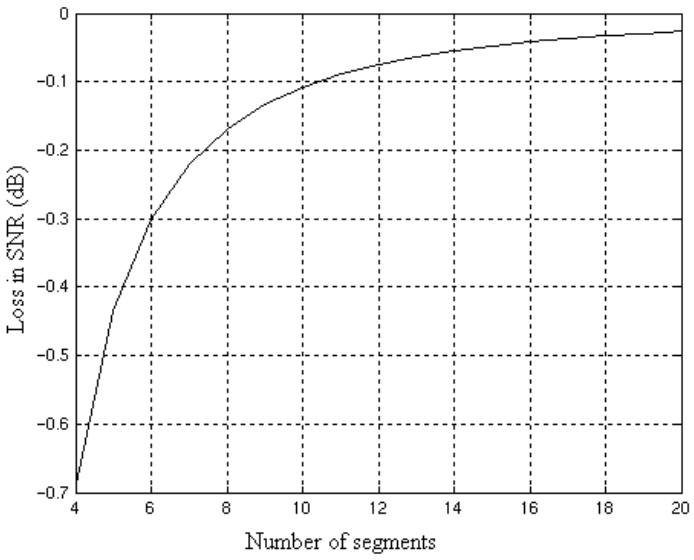


Figure 4.11 Loss in SNR Versus Number of Samples Used in Sine Wave Signal.

For number of segments = 10 the loss in SNR is only -0.1 dB. Using larger number of samples, the loss in SNR does not improve significantly. Hence, the number of samples in each half cycle of sine wave is chosen to be 10. The number of capacitors used is the number of sine wave samples in each quarter of the sine wave which is equivalent to 5 capacitors as shown in Figure 4.10.

Another alternative implementation, is to use just integrator which will result in SNR' given by equation (4.10). While the ideal demodulator circuit has SNR given by equation (4.11). Hence, the overall loss in SNR is given by equation (4.12). This is not a significant loss which makes the current circuit the easiest to implement.

$$SNR' = \frac{2}{N_0}\int_0^T A\sin\left(\frac{\pi t}{T}\right)\frac{1}{T}dt = A\frac{4\sqrt{T}}{\pi N_0} \tag{4.10}$$

$$SNR = \frac{2}{N_0}\int_0^T A\sin^2\left(\frac{\pi t}{T}\right)\sqrt{\frac{2}{T}}dt = A\frac{\sqrt{2T}}{N_0} \tag{4.11}$$

$$\frac{SNR'}{SNR} = 0.9 = -0.45\,dB \tag{4.12}$$

4.7 Offset-QPSK Modulator

The modulator circuit, shown in Figure 4.12, is used to generate the base-band sine wave shaped signal [43]. The modulator circuit is an integrator that has different weights C1/C6 to C5/C6 with switches that close sequentially to generate the first quarter of the

half-sine wave and then reverse direction to generate the other half of sine wave. To decrease the capacitor spread ratio another bank of capacitors (C1` to C5`) is added with negative the reference voltage at main capacitor bank. The switches of C1 first close to generate the first step of the output, then switches of C2 and C1` closes to generate the second step and so on.

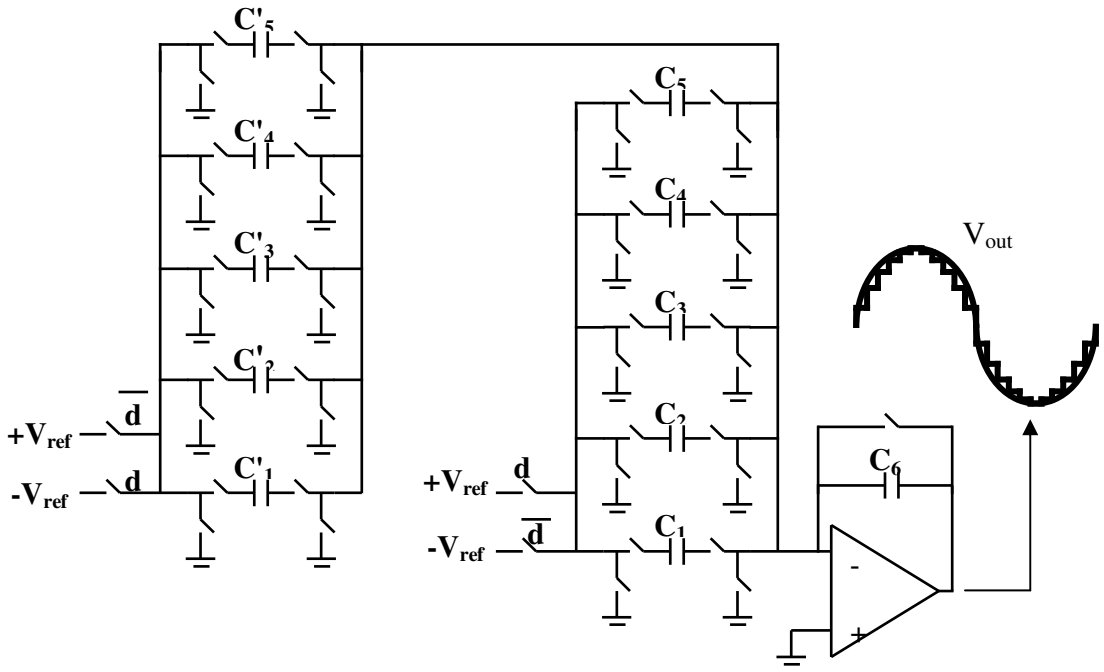


Figure 4.12 ZIGBEE Modulator Circuit

The frequency of switches is chosen to be 5 MHz which is the same as the reference frequency used in PLL of ZIGBEE transceiver. Since the frequency of the generated sine wave is 0.5 MHz, thus 10 samples for each half sine are chosen to make use of the available clock. The power consumption of the modulator circuit is 300 μW.

For the Op-amp circuit design: The GBW of the amplifier is chosen such that $aGBT > 5 \Rightarrow GB \approx 64MHz$, where a is the capacitor ratio between the sum of all feedback capacitors and the sum of all capacitor connected to the negative terminal of the op-amp.

4.8 Transmitter RF Front End

The transmitter front end consists of the up-conversion Mixer, Preamplifier and Power Amplifier stages. The front end building blocks are shown in Figure 4.13.

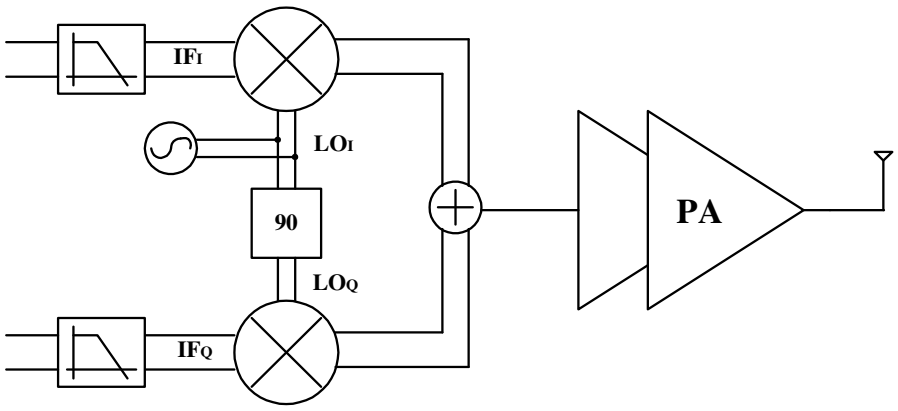


Figure 4.13 ZIGBEE Transmitter Front End Architecture

4.8.1 Up-conversion Mixer

In-phase (I) and quadrature (Q) baseband signals are up-converted to ISM band by two fully-differential fully-balanced quadrature up-converter mixers. Figure 4.14 shows the

schematic of the single sideband mixer. The mixer is preceded by a 2nd order passive low pass filter eliminates higher harmonics generated by a switch-cap sine wave generator and leakage from its clock. Two mixers' output currents are then added together at the tank to create single side-band mixing. This way, I and Q signals can be up-converted to the same band without cross-talking to each other. Thus, at the receiver side they can be down-converted and demodulated into two separate streams. Although rejection of cross-talk between I and Q lines is ideally high it is limited by the mixer's mismatch, deviation of the phase difference of LO quadrature signals from 90 degrees and their amplitude mismatch. This crosstalk rejection can be shown using the equation (4.13) [44].

$$rejection = \left(\frac{1 + (1+\varepsilon)\cos\theta}{1 - (1+\varepsilon)\cos\theta} \right)^2 \tag{4.13}$$

Where θ represents deviation of phase difference between LO quadrature signals from 90 degrees and ε is their amplitude mismatch.

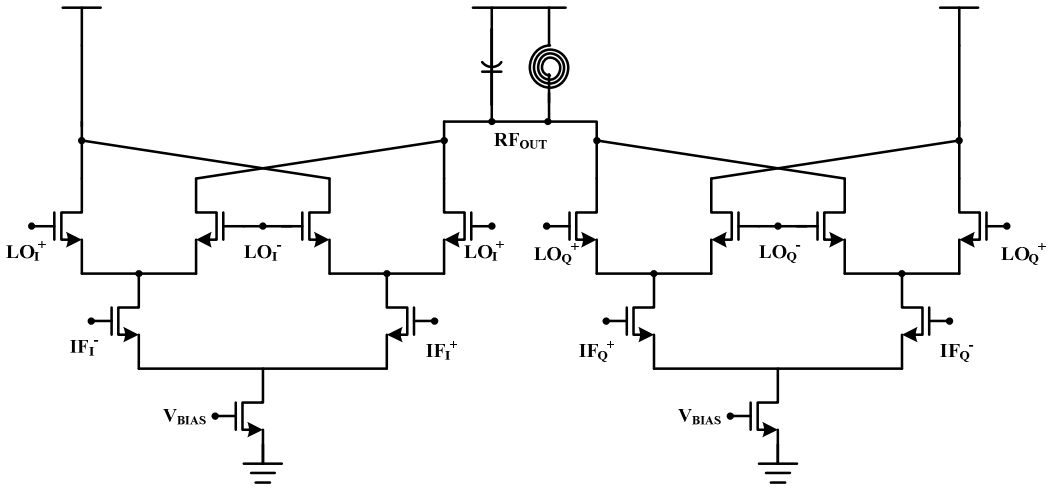


Figure 4.14 Differential Input Fully Balanced Single Ended SSB Mixer

4.8.2 Power Amplifier

Differential Mixer is followed by a single-input single-output power amplifier to deliver required 0 dBm nominal output power to the antenna. Only one of the outputs of the mixer is used for this purpose and use of on-chip active balun or off-chip passive balun is avoided to save power and increase system integration at the expense of half of the signal power. In order to make it a low power standard, IEEE 802.15.4 has relaxed linearity requirements of power amplifier and other building blocks of transmitter by loosening requirements for its output spectral power mask. Figure 4.15 compares spectral power masks of ZIGBEE and Bluetooth standards. This comparison shows that relaxed linearity requirements of the ZIGBEE standard can be exploited to minimize power consumption.

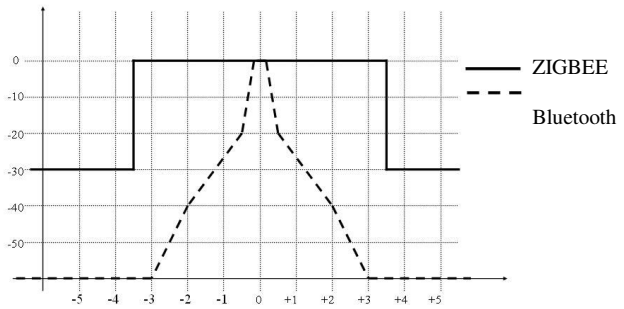


Figure 4.15 Comparison Between PSM of Bluetooth and ZIGBEE Standards

4.8.3 Design Considerations

Since this standard PA has a more relaxed linearity requirement, it can be exploited to lower power consumption. For this purpose switching type power amplifiers could be employed as well as linear type power amplifier with conduction angles less than 180° (class AB, B and C). Considering low output power required (around 0 dBm) and complexity of output network in switching type amplifiers, class AB amplifier was selected. Figure 4.16 shows the schematic of the pre-amplifier and power amplifier. Because mixer's conversion gain is about -2dB a pre-amplifier is needed to increase the swing at the output stage and hence improve its efficiency. Resistive network at the load of pre-amplifier could be used to vary its gain and hence PA's output power. Also pre-amplifier acts as isolation buffer between the output stage and mixer to increase its stability.

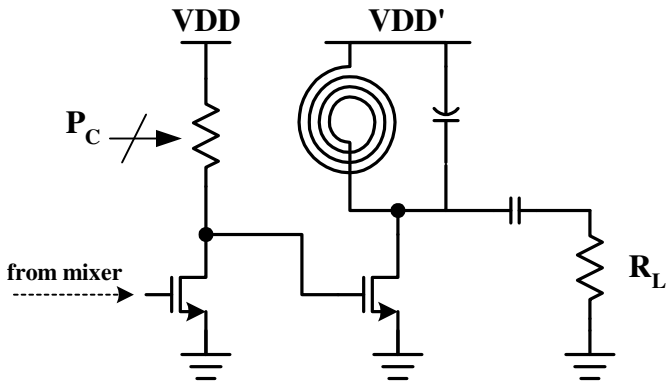


Figure 4.16 Schematic of Pre-amplifier and Output Stage

4.8.4 Stability Issues

Designing single-ended power amplifier simplifies the characterization by eliminating the need for a balun (on-chip or off-chip). However it comes with the price of second order harmonic, losing half the signal power and lacking a clean on-chip ground. As shown in Figure 4.17, virtual grounds created by using differential signals at power amplifier would diminish the effect of bond-wire inductance at the ground pin seen by preceding circuits. This minimizes the interference that bondwire inductance could have on a preceding resonance tank. Even so single-ended power amplifiers are desired when a compact and cost-effective transmitter design requires elimination of any on-chip or off-chip balun.

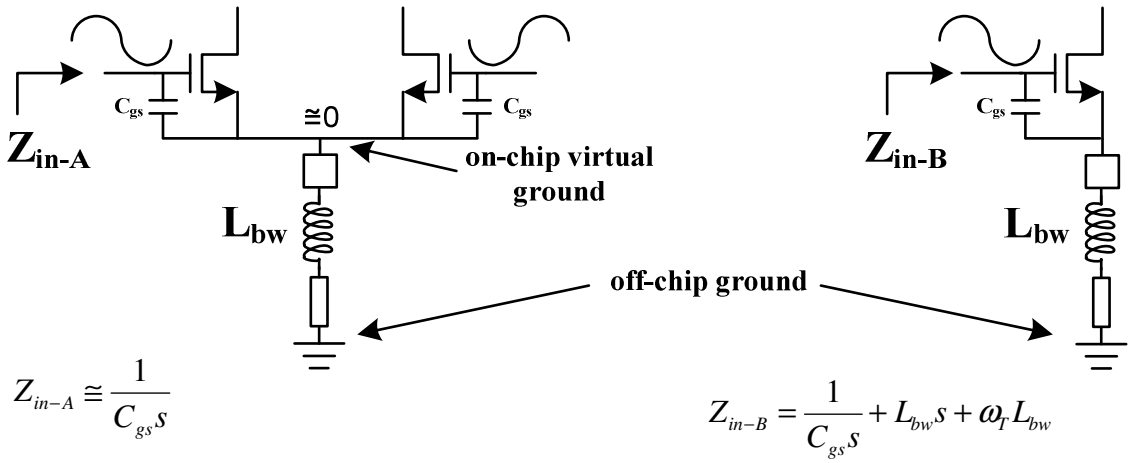


Figure 4.17 On-chip Virtual Ground Reduces the Effect of Bondwire Seen by Preceding Circuits

In this design a single-ended stage was selected in order to remove baluns and achieve a low-cost and more compact solution as is needed in ZIGBEE and wireless sensor network applications. However pre-amplifier's transistor and load sizes could be optimized to minimize the sensitivity of preceding resonance tank to changes in bondwire inductance. Also mixer's resonance tank should be "de-Q'ed" to reduce its sensitivity.

Other architectures use shunt peaking in order to increase the gain of pre-amplifier. A resonance tank at the drain of the pre-amplifier which creates high impedance around the frequency of operation gets reflected back at the impedance seen at the input of the pre-amplifier through transistor's gate-drain capacitance and interferes with mixer's tank. So

a resistive load was selected for the pre-amplifier to improve isolation between output stage and mixer's output and increase its stability.

4.9 Frequency Synthesizer

For a direct conversion transceiver, same carrier frequencies are used for both receiver and transmitter, reducing the Synthesizer complexity and area. The synthesizer specifications are shown in Table 4.4. The frequency synthesis is performed through the use of an integer N based PLL. A 3^{rd} order loop is designed and approximated as a critically damped, 2^{nd} order loop with a loop bandwidth of 30kHz. The reference frequency of the loop is 5MHz which is the spacing between the 16 channels of the 2.4GHz band of ZIGBEE.

The up-conversion and down-conversion mixers require the quadrature phases of the LO signal. VCO is operated at twice the channel frequency and a frequency divider is used following the VCO, to generate the quadrature LO signals. This technique is preferred over using passive RC networks due to its minimal phase and amplitude mismatch. Also, operating the VCO at a frequency other than the carrier eliminates injection pulling and PA load pulling issues that arise in a transceiver environment.

Table 4.4 FS Specifications

	Required Value
Frequency Range	2405-2480 MHz
Channel Spacing	5 MHz
Number of Channels	16 (11-26 of the PHY layer)
Settling Accuracy	± 40 ppm (96 KHz)
Lock time	< 192 µs
Phase Noise	< -112 dBc/Hz at 10 MHz offset < -92 dBc/Hz at 3.5MHz offset
Spur Suppression	< -35 dBc at 5MHz < - 46 dBc at 10MHz
Synthesizer Output (LO)	150-200 mVpp
I-Q Phase Mismatch	< 10 deg
I-Q Gain Mismatch	< 11%

A NAND based tri-state PFD is used for the phase frequency detection. A dead zone removal pulse of 2ns is used in this design which constitutes %1 of the total reference time. The reference frequency of 5MHz is generated on chip through the use of a divide-by-4 circuit as shown in the PLL block diagram of Figure 4.18. It is seen that the chip input reference is 20MHz and the divider generates the PLL reference of 5MHz to be fed into the PFD. This scheme is used to prevent the reference spurs due to the coupling of the input reference signal to the charge pump output through the testing board and the substrate. Note that, the ZIGBEE PLL spur rejection specifications are at the next channel (5MHz) and alternate channel frequencies (10MHz). Then, the coupling of the

20MHz input reference to the VCO control line will not constitute a significant concern for this design. Generating the PLL reference on chip by a divider also has the advantage of generating a synchronized clock since the gates in this divider are similar to the logic gates in the programmable divider.

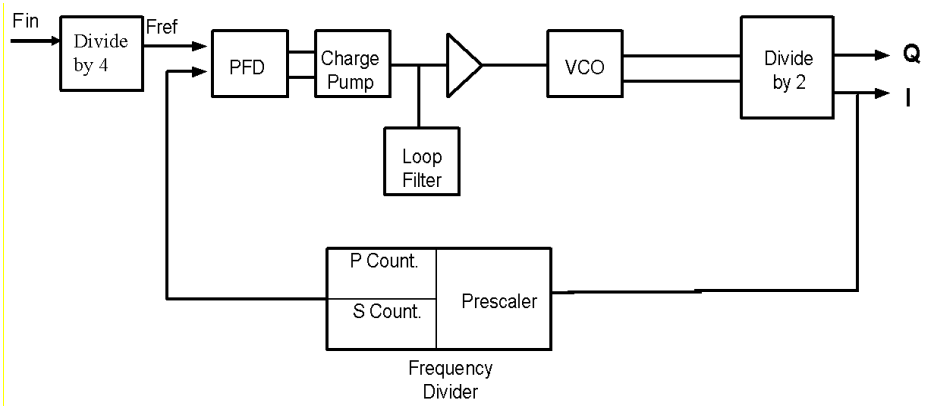


Figure 4.18 Block Diagram of the PLL

The charge pump schematic is shown in Figure 4.19. A low voltage cascode current mirror based topology is used to have accurate current matching [45]. This circuit also minimizes the sensitivity to the output node voltage variations and charge sharing issues. The current gain is 20 μA

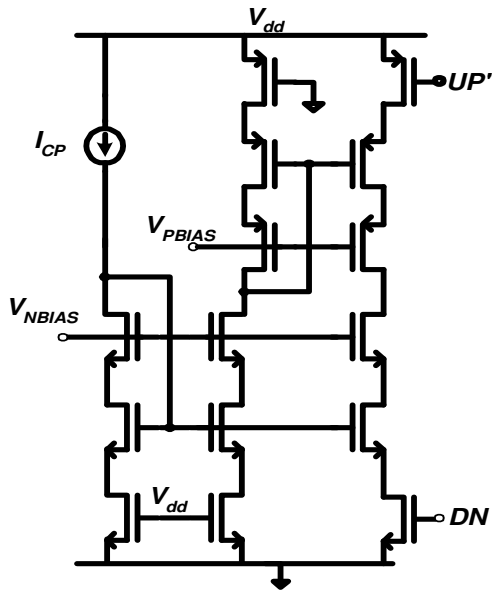


Figure 4.19 Charge Pump

The VCO is an LC tank based oscillator and its schematic is shown in Figure 4.20. The CMOS topology is preferred over the PMOS or NMOS VCO's due to its symmetry in rise and fall times which minimizes the coupling of the 1/f noise to the output [46]. This topology also allows the use of differential symmetric inductors which minimizes the inductor area requirement. A varactor bank is used to provide coarse tuning to the VCO to provide flexibility in the presence of process variations. The VCO consumes 4mW of power and has a sensitivity of 135 MHz/V.

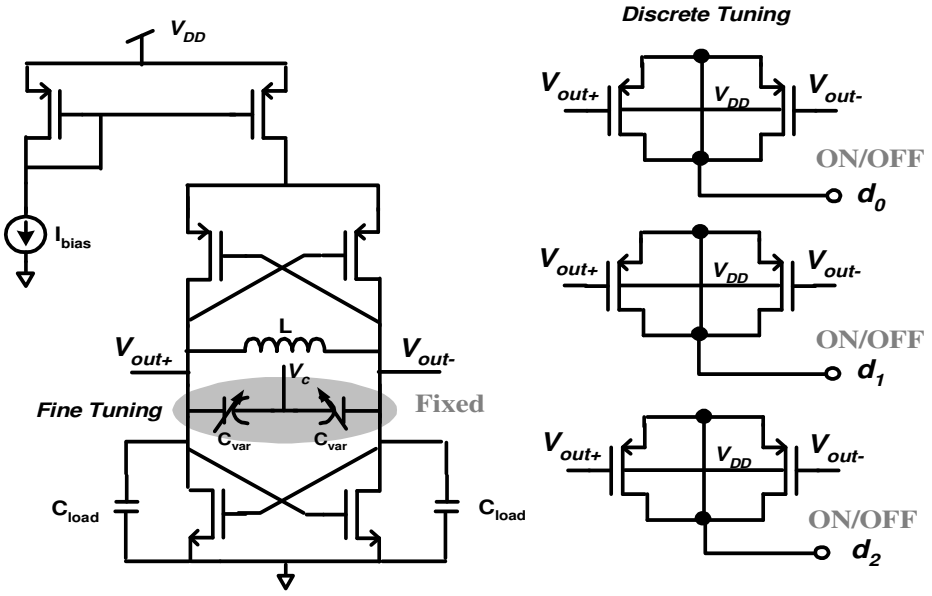


Figure 4.20 VCO Schematic

A divide by 2 circuit follows the VCO and generates the quadrature LO signals. A pulse-swallow programmable divider closes the feedback loop. Four channel selection bits program the loop to generate the 16 channels of the ZIGBEE band. The programmable divider consists of a dual modulus prescaler, program and swallow counters. The prescaler operates at 2.4GHz and its implementation is critical due to the high power consumption of these blocks in PLL's. The dual modulus prescaler is implemented using Differential Cascode Voltage Switch Logic circuits. To compensate for the slow rise time of these circuits, resistors are attached to the drains of the pmos pull-up latch transistors. This generates additional overdrive voltage to the pull-up latch, improving the rise time of the DCVSL circuit. The programmable divider circuit, and the buffer that drives it consume a total of 1.8mW of power.

An *LO Buffer* with inductive load is used between the PLL and the mixers to generate the required amplitude. The differential peak to peak amplitude generated for both the up-conversion and down-conversion mixers are 300 mV. The LO buffer constitutes of two differential inductors for two separate LC tanks for the two mixers. Each inductor is 4.2nH with an area of 400 µm by 400 µm including the inductor guard ring available in this technology. The LO buffer consumes 2.7mW of power.

4.10 Transceiver Experimental Results

The Transceiver architecture is implemented in standard TSMC CMOS 0.18µm technology and fabricated through TSMC. The chip microphotograph is shown in Figure 4.21. The total area of the transceiver is 12.5mm^2. The individual building blocks measurements are shown next.

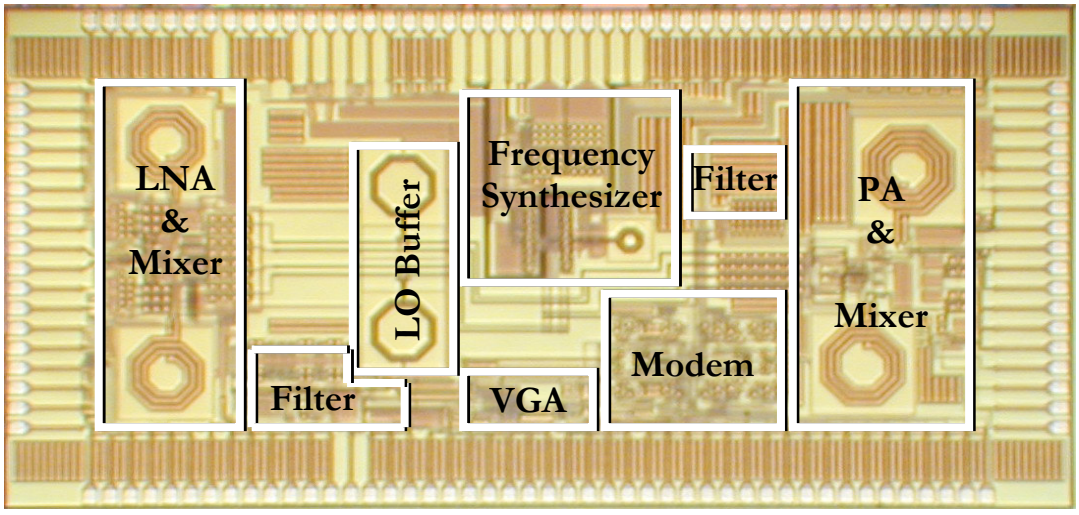


Figure 4.21 Chip Micrograph

4.10.1 Receiver Front End

As described in Section 4.3, a stacked architecture is used for the receiver front-end to reuse the DC current and thus saving power consumption. The Printed Circuit Board (PCB) used to characterize the LNA and Mixer is shown in Figure 4.22.

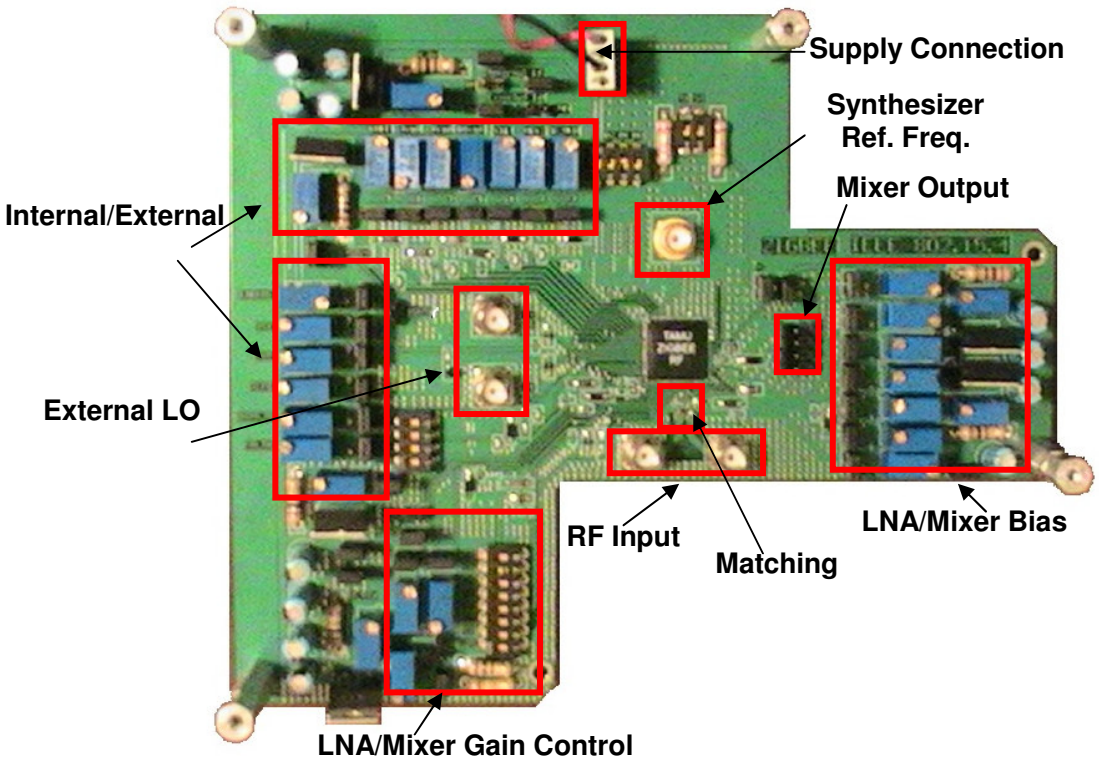


Figure 4.22 LNA and Mixer PCB

The PCB is designed to use either an external LO signal or an internal LO signal from the integrated Frequency Synthesizer. For the external LO option, a 4.8GHz differential signal is required to generate 2.4GHz I and Q signals internally using an integrated

divide-by-2 circuitry. Off-board BALUNS are used to generate the differential 2.4GHz input RF signal to the LNA and the differential 4.8GHz input RF signal to the Mixer switches. Each bias line on the PCB has a capacitor tank (47nF and 11pF) and a zener diode, to suppress any PCB noise and avoid its injection to the chip, as well as Electro Static Discharge (ESD) protection. Multiple Voltage regulators are used on board to provide the necessary bias to the chip. Switches controlling LNA gain peaking, LO channel selection, as well as VCO coarse tuning are included.

For input matching: Figure 4.23 shows the test setup for the Scattering parameter (S11) characterization. Each of the two differential inputs of the LNA is matched to 50ohm. Thus for an ideal 50:100 BALUN, the input impedance at the unbalanced input should match 50ohms. To avoid any erroneous measurement, Network analyzer calibration is done including the BALUN as well as the cables used for connection. Thus no de-embedding is required.

Figures 4.24 and 4.25 show the measured S11 for the IEEE802.15.4 band (2.4GHz to 2.48GHz). Across the band of interest, S11 is less than -14dB. This means that, -14dB of the incident signal to the LNA is reflected back due to mismatches. This corresponds to less than 4% of the incident signal.

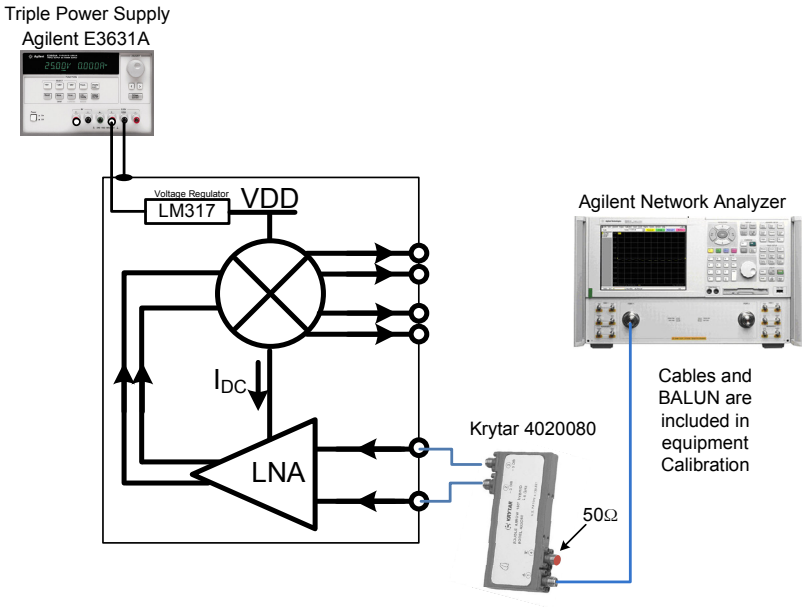


Figure 4.23 S11 Characterization TestSetup

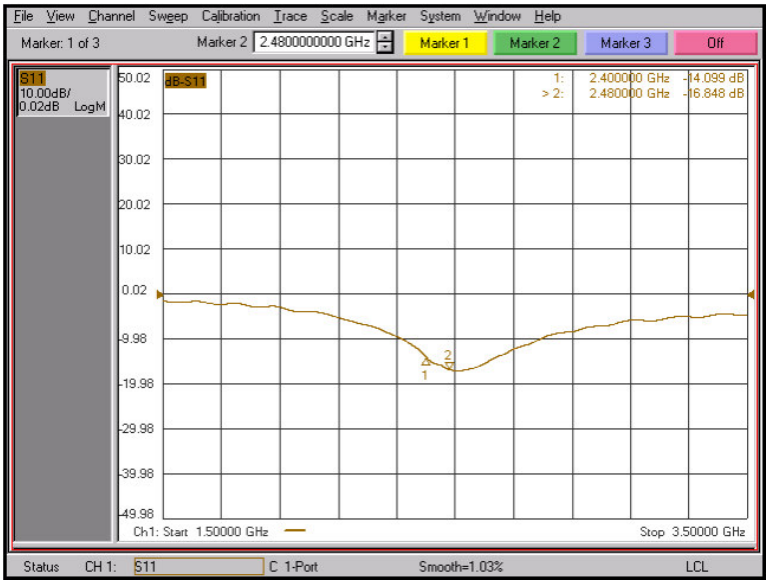


Figure 4.24 S11 in the High Gain Mode

Figure 4.25 S11 in the Low Gain Mode

For the front-end gain: Figure 4.26 shows the test-setup for gain measurements. An ideal BALUN has an attenuation of 3dB from the unbalanced input port (single ended side) to any of the balanced output ports (fully differential side). Any extra attenuation due to imperfect BALUN or due to cabling should be taken into account. The losses of the used 2.4GHz BALUN and cabling path is almost 6dBm. Thus extra 3dB attenuation is recorded.

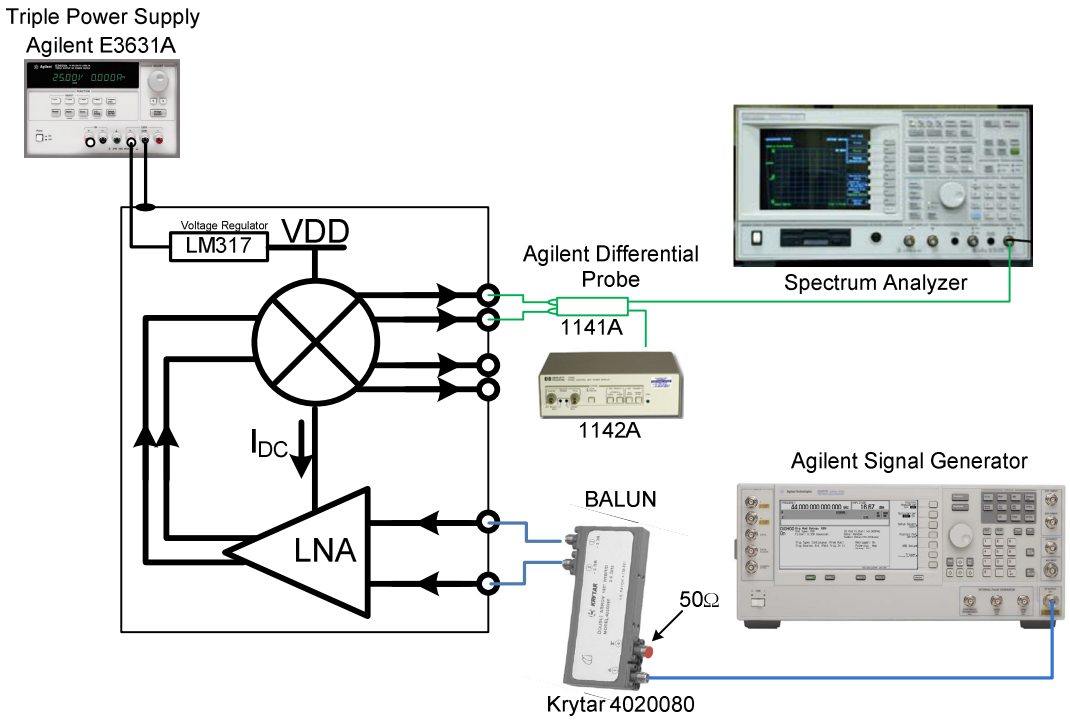


Figure 4.26 Gain Characterization TestSetup

To measure the gain, a -70dBm signal is applied from the signal generator, and the down-converted output is shown in Figures 4.27. By taking into account the extra 3dB attenuation, one can calculate a gain of 22dB in the high gain mode. This shows a degradation of 10dB from postlayout simulations. This can be due to process shift in either vt of MOS transistor or in inductor value to have a different gain peak frequency. More investigations and possible increase of power consumption is required to achieve the proper gain.

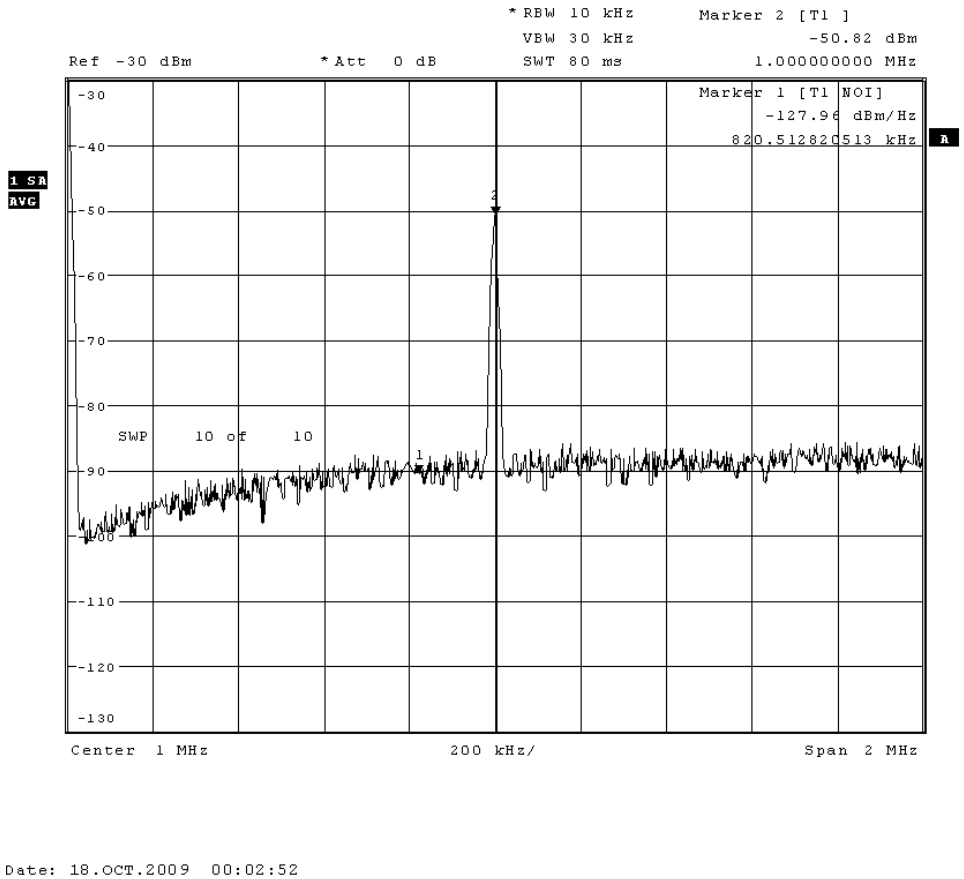


Figure 4.27 Mixer Output in High Gain Mode

For Noise Figure: Referring to Figure 4.27, Marker 1 shows the output noise density, where the spectrum analyzer is adjusted to measure the output noise density in dBm/Hz. NF can be calculated using equation (4.14) where the input path loss is taken into account in the gain term.

$$NF \approx N_{out}\big|_{dBm/Hz} - N_{50\Omega}\big|_{dBm/Hz} + G \tag{4.14}$$

Thus a NF of 24dB is achieved for the Receiver front-end. This is mainly degraded because of the 10dB gain drop. Taking into account the 6dB of margin in system design as well as the 4dB margin in blocks' specifications, a sensitivity of -81dBm is achieved rather than -85dBm required by ZIGBEE standard.

For IIP3: A two tone test is applied at the input with sweeping their input power simultaneously using the test setup shown in Figure 4.28. Figures 4.29, 4.30, and 4.31 show the down converted spectrum for multiple input levels (-25dBm, -20dBm, and -15dBm) with the resulted IM3 in each case. Figures 4.32 show the extrapolated curve indicating an IIP3 of -6dBm in the High gain mode. An extra path loss is added due to the power combiner and extra cabling. A total input path loss of 11dB is taken into account to specify the actual input power to the receiver.

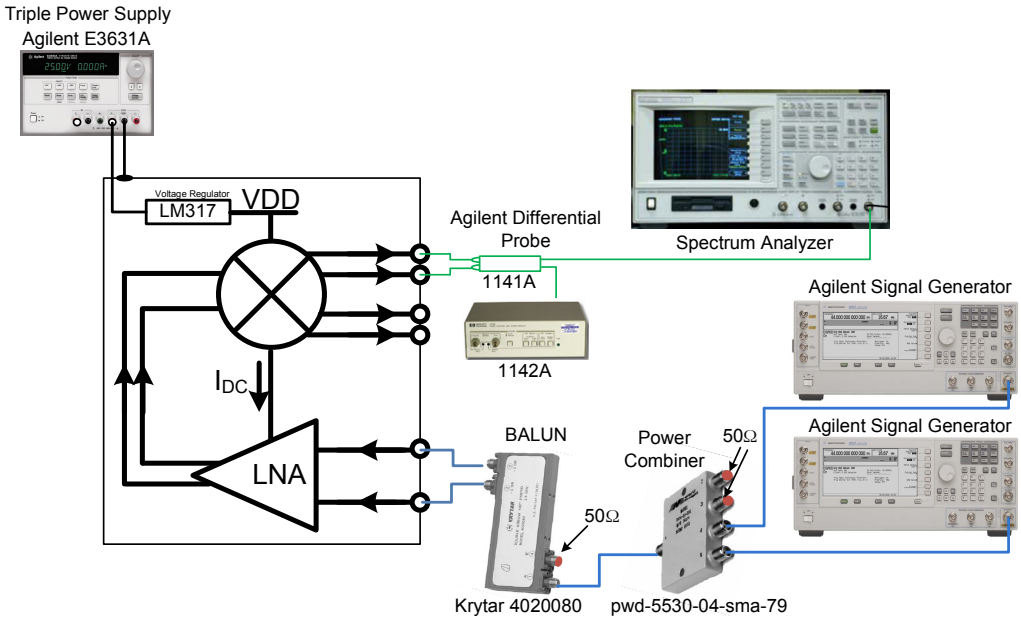


Figure 4.28 Two Tone Test Setup

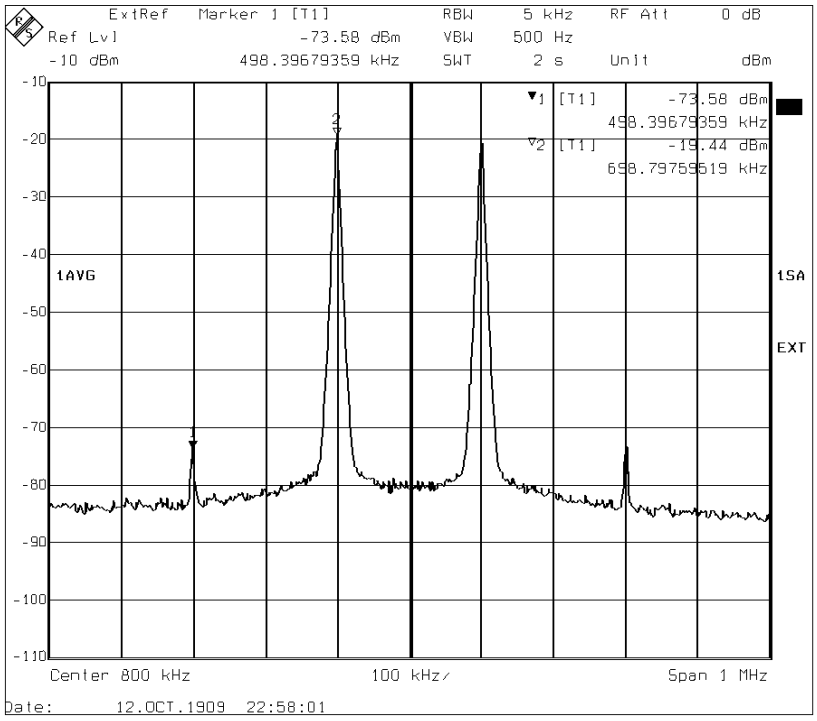


Figure 4.29 Two Tone Test Output for Pin of -25dBm

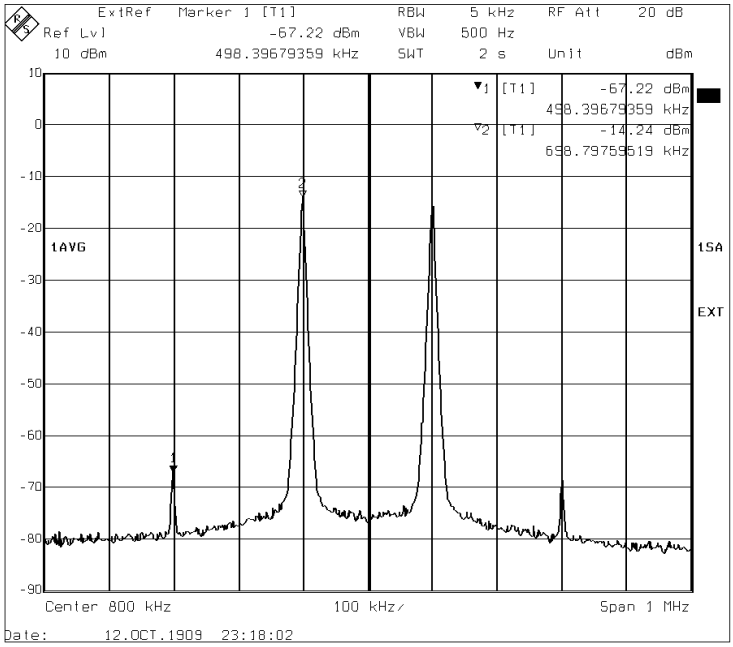


Figure 4.30 Two Tone Test Output for Pin of -20dBm

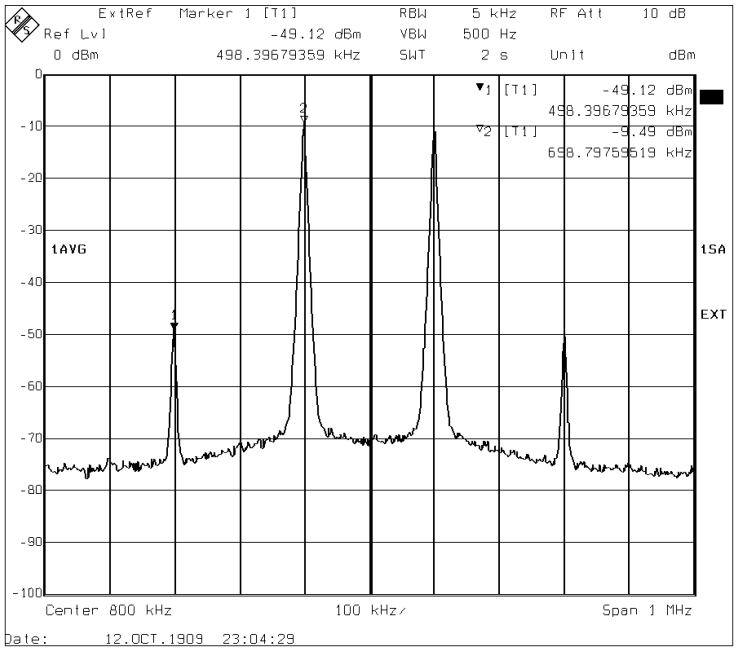


Figure 4.31 Two Tone Test Output for Pin of -15dBm

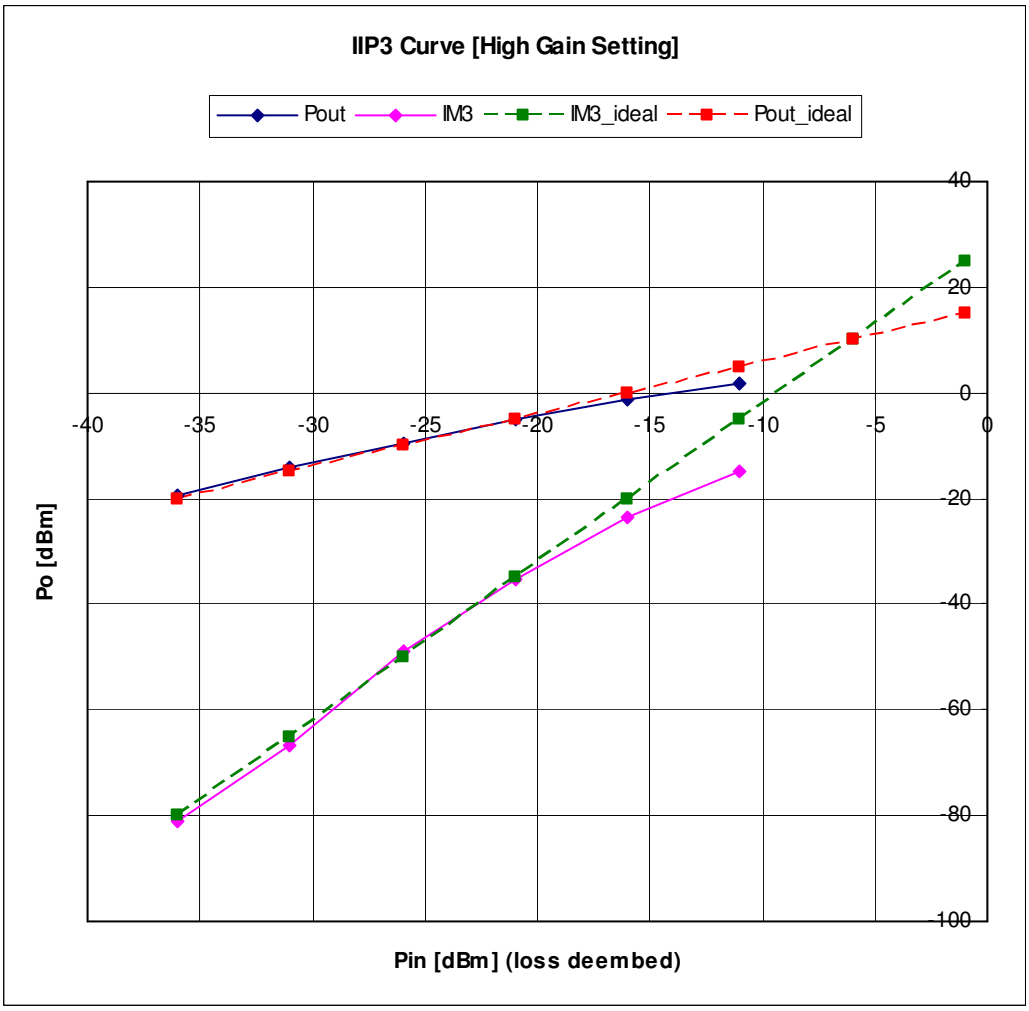


Figure 4.32 IIP3 curve in High Gain Mode

The improvement of the IIP3 from the post-layout simulations, results from the reduction of the gain. The RF front-end is consuming 3mA from 1.35v supply to have a total power consumption of 4.05mW. More test tweaking is required to achieve higher gain and thus lowering the overall NF to meet the required sensitivity.

4.10.2 Channel Filter

Figure 4.33 shows the frequency response of the 3rd order butterworth filter. Filter quality factor (Q) is determined by the capacitor and gm ratios. The C is affected by the pad capacitance as well as the external driver's input cap during the measurement, resulting in the enlarged Q value and degraded stop band attenuation. This degradation only happens for stand-alone solution, and is not a problem in integrated solution. Results are verified in simulations by adding 2~3pF loading, the same cut-off frequency peaking is observed.

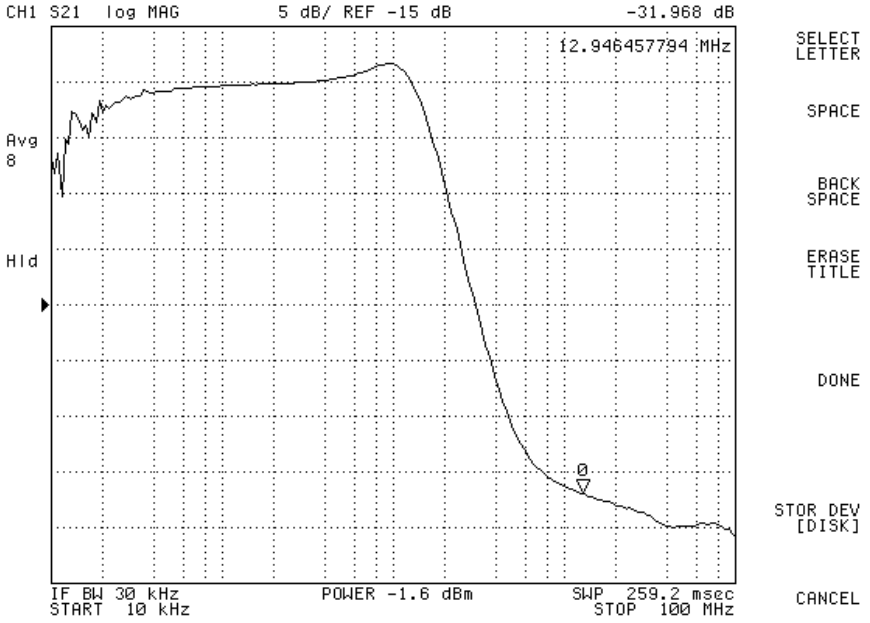


Figure 4.33 LPF Frequency Response

Figure 4.34 and 4.35 show the two tone test output for an input signal of -10dBm and the IIP3 curve indicating an IIP3 of 8dBm.

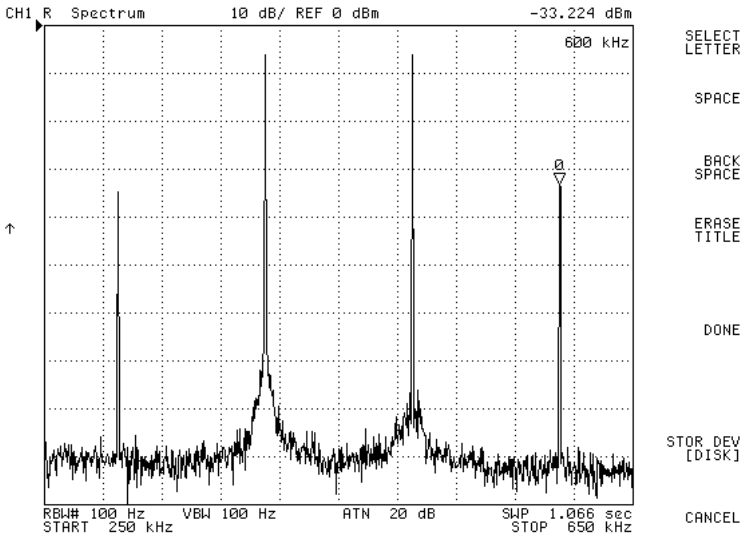


Figure 4.34 LPF two-tone test for -10dBm input signal

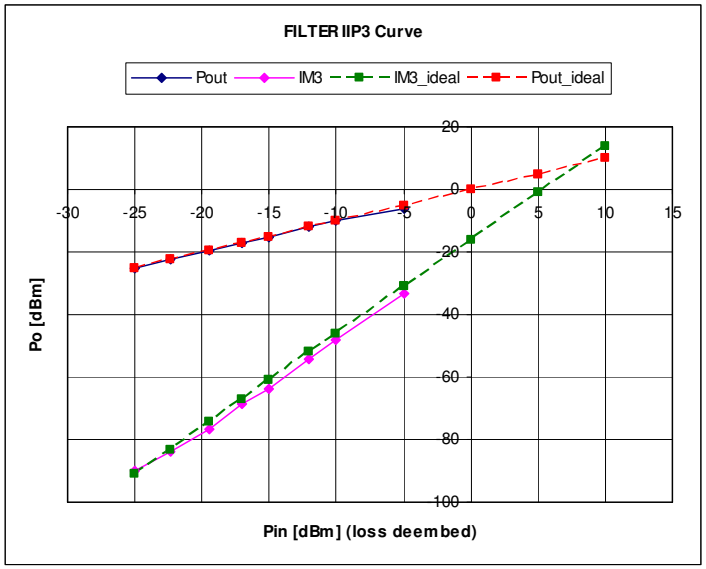


Figure 4.35 LPF IIP3

4.10.3 Transmitter Front End

Figure 4.36 shows the Transmitter front-end PCB, while Figure 4.37 shows the board connections. The PA output is terminated by 50 Ω to obtain a near-end matching. Given the spectrum analyzer has its own 50 Ω input impedance; the PA sees an overall of 25 Ω impedance. Thus only half the output current is measured by the spectrum analyzer. As a result 6dB should be added to the output measured power as a de-embedding factor for the 50 Ω termination on board. Another de-embedding factor due to the cable set attenuation is measured using S-parameter network analyzer to obtain S21 or S12. The cable attenuation is found to be 2dB in the band of interest. A de-embedded output power of -13dBm at 2.4GHz is achieved with a sideband rejection of -40dBc and LO leakage limited to -35dBc. The IEEE802.15.4 Power Spectral Mask (PSM) of -20dBc is measured. A maximum output power more than -10dBm (-17dBm before losses de-embed) occurs at 2.247GHz, rather than 2.4GHz due to process variations. PSM is characterized at the maximum output power where the worst case linearity exists. Figure 4.38 shows the PSM at 2.247GHz. The overall transmitter consumes 25mW.

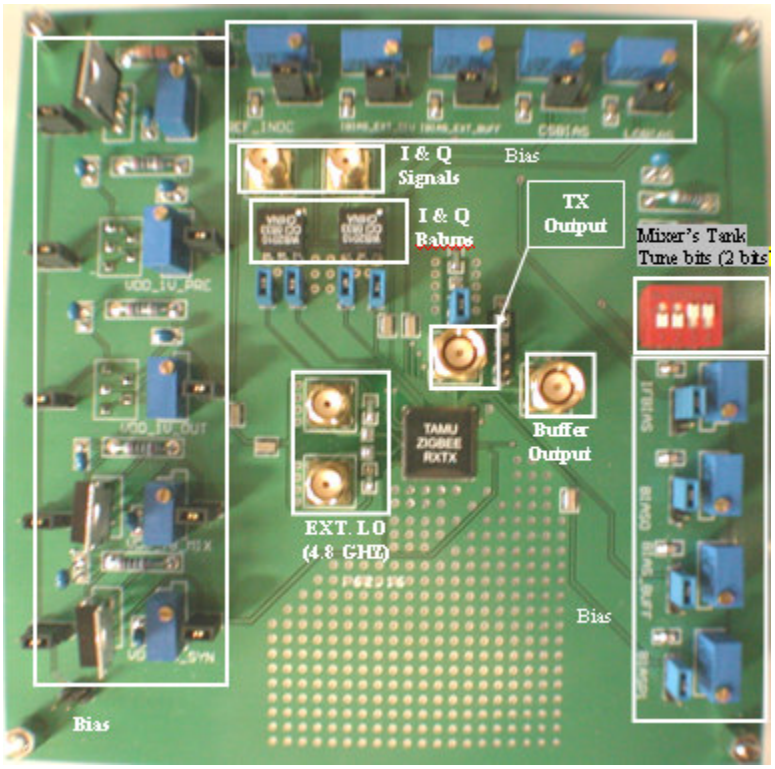


Figure 4.36 Transmitter Front End PCB

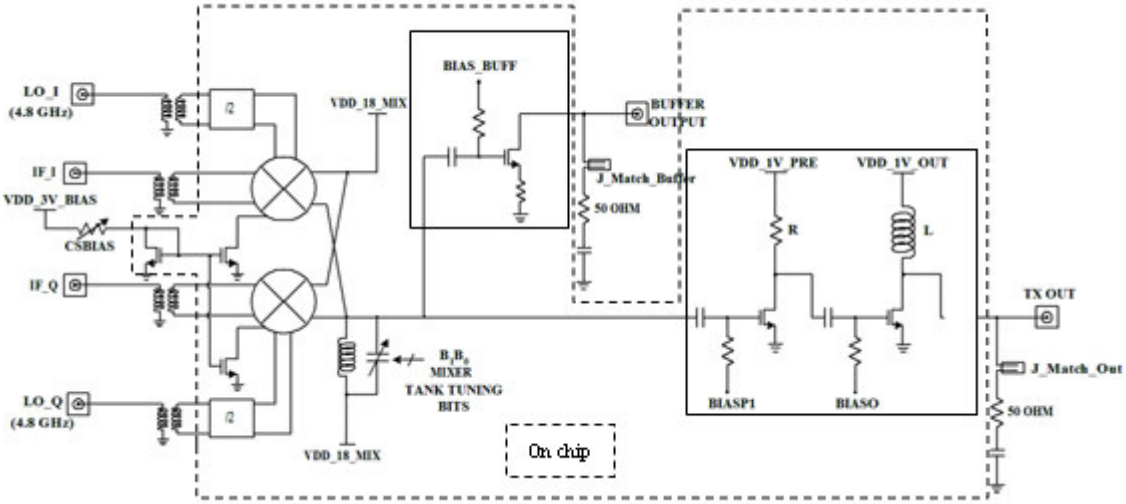


Figure 4.37 Transmitter Front End Board Connections

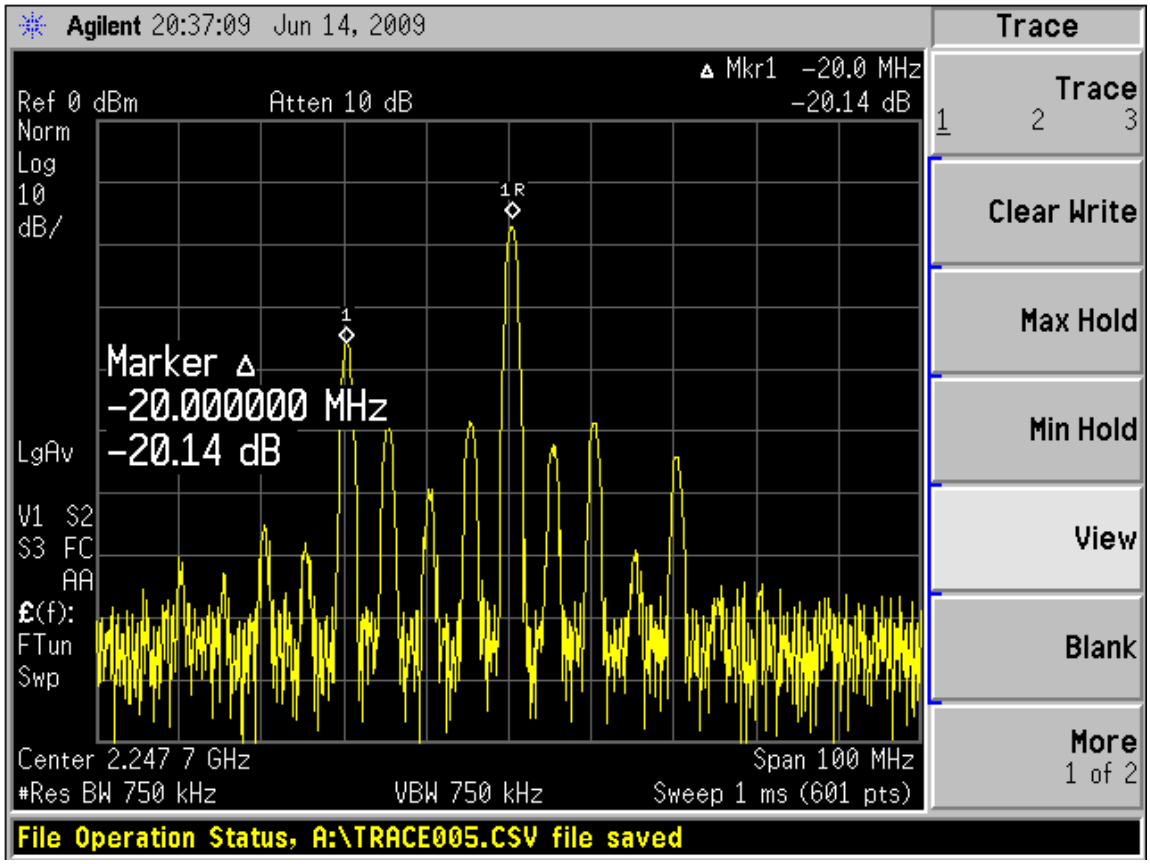


Figure 4.38 PSM at 2.247GHz Output Signal

4.10.4 Frequency Synthesizer

Figures 4.37 – 4.41 show the measurement results: VCO tuning curves, output spectrum channel 16, phase noise and settling time. Settling time measurement is performed while the channel selection is switched from first to last channel. The VCO control voltage is observed to determine the 1% settling time. The lock transient shows the critically damped behavior.

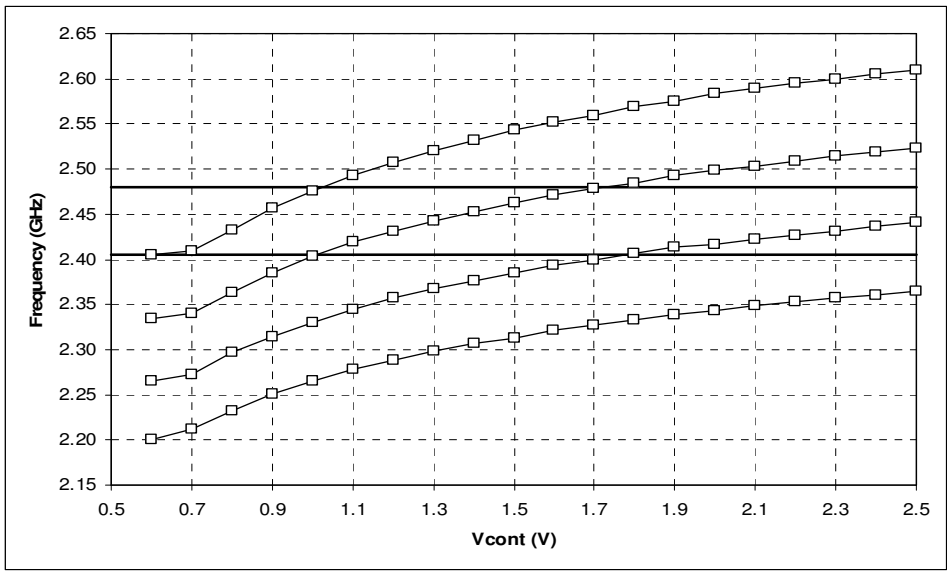


Figure 4.37 VCO Tuning Curves

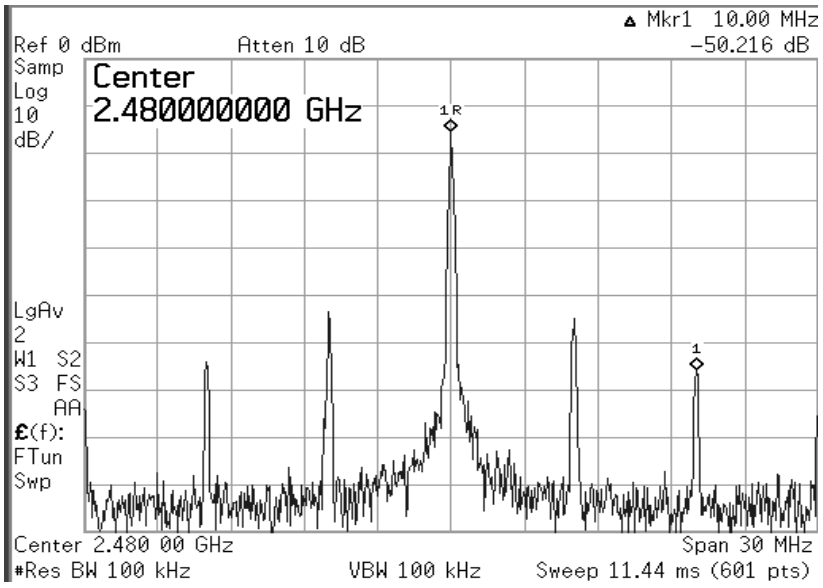


Figure 4.38 PLL Output Spectrum – Channel 16

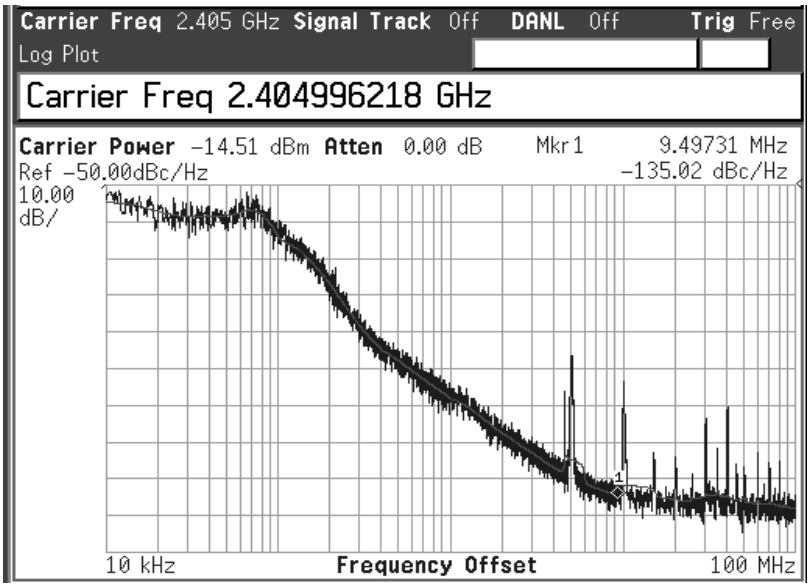


Figure 4.39 PLL Phase Noise at 10MHz Offset

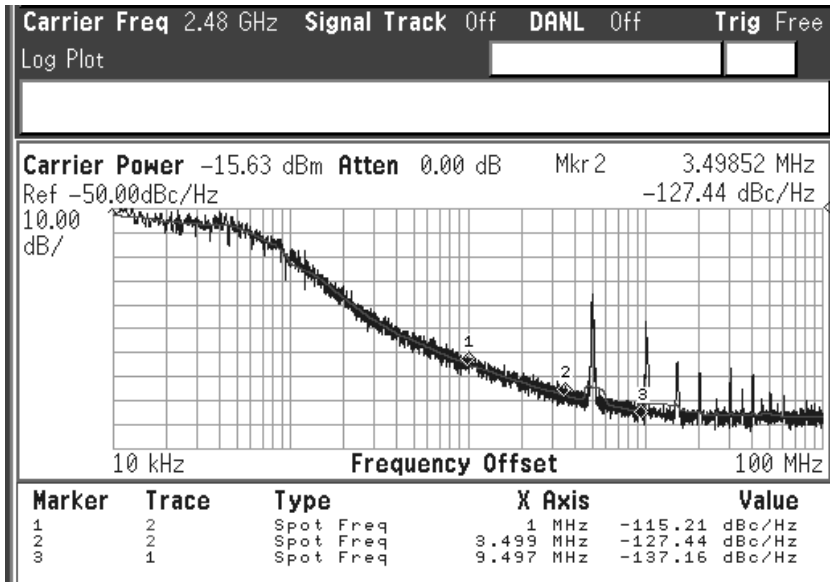


Figure 4.40 PLL Phase Noise at 3.5MHz Offset

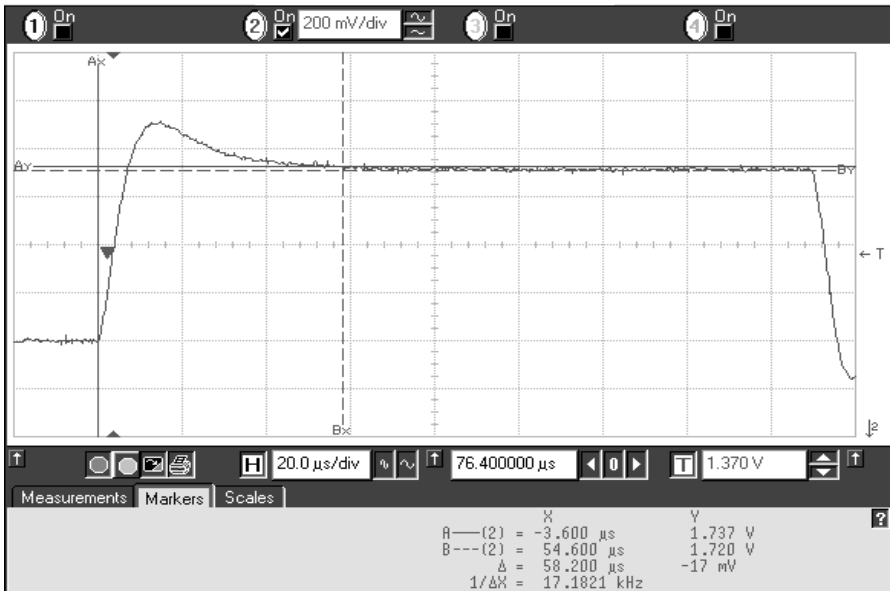


Figure 4.41 PLL 1% Settling Time

Table 4.5 shows the synthesizer required specifications and the measured results. The synthesizer meets the ZIGBEE specifications with 8.5mW total power.

Table 4.5 FS Specifications and Measurement Results

Metric	***Specification***	***Measurement***
Frequency Synthesis	2405-2480	2405-2480
Phase Noise	-112 dBc/Hz at 10MHz < -102 dBc/Hz at 3.5MHz	- 136 dBc/Hz at10 MHz -127 dBc/Hz at 3.5MHz offset
Spur Suppression	- 13 dBc at 5 MHz - 43 dBc at 10 MHz	- 48 dBc at 5 MHz - 55 dBc at 10 MHz
Settling Time	192 µs	58 µs
Power Consumption	Minimum	8.5 mW

4.11 Conclusions

A low power fully integrated IEEE 802.15.4/ZIGBEE compliant transceiver has been analyzed, designed, and implemented. Modulator to demodulator terminals have been discussed, passing through all the intermediate blocks. Selected key building blocks have been characterized and presented. As a low power solution, the designed transceiver is adequate for many home applications, sensor networks, and control systems.

CHAPTER V

PASSIVE AND ACTIVE RFID TAGS

5.1 Background and Motivation

Radio frequency identification (*RFID*) is one of the widely investigated hot topics of the communications area nowadays. Radio Frequency Identification systems are widely used in a variety of tracking, security and tagging applications. Their operation in non line–of-sight environments makes them superior over similar devices such as barcode and infrared tags. RFID systems span a wide range of applications: medical history storage, dental prosthesis tracking, oil drilling pipe and concrete stress monitoring, toll ways services, animal tracking applications, etc. RFID system consists of two main wireless components operating in a master-slave environment, as shown in Figure 5.1. The *interrogator* (reader) acts as the master; it controls the whole operation, starts the session, requests the information needed information, and ends the session. The Interrogator is stationary and mains powered. RFID *transponders* (tags) act as the slave; they are the mobile elements and can be passive or active or semi-passive (semi-active) based on their power generation scheme. Section 5.2 presents the RFID system and its idea of operation. Section 5.3 shows different tags' types and structures. Section 5.4 describes the reader structure and its main challenges with some of the literature solutions. Section 5.5 defines different frequency bands used for RFID technology associated with their standards. Different Applications are listed in Section 5.6 together

with system requirements for each application. A system design methodology is introduced including the main issues and tradeoffs between different design parameters in Section 5.7. Section 5.8 shows a design example of a 13.56 MHz RFID passive tag. The key building blocks such as the charge pump, voltage reference, and the regulator used to generate the DC supply voltage from the incoming RF signal are discussed along with their design tradeoffs for passive and semi-passive tags. The uplink modulation techniques used (ASK, PSK, FSK, and PWM) are illustrated showing how to choose the appropriate signaling scheme for a specific data rate, a certain distance of operation and a limited power consumption budget.

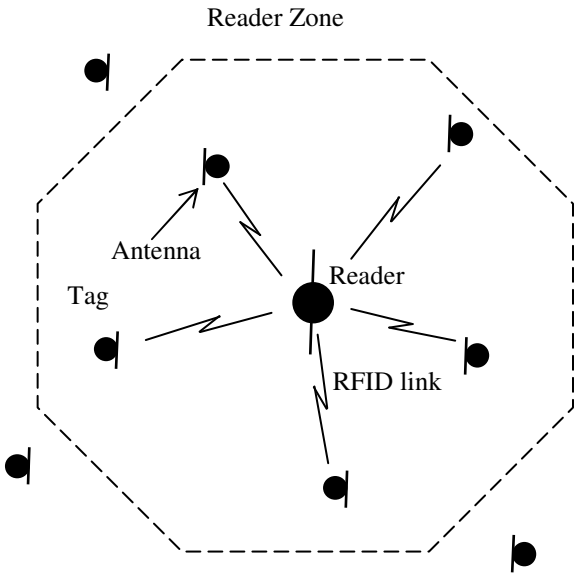


Figure 5.1 General RFID System Elements

Section 5.9 shows the backscatter modulation scheme used in the downlink. Different kinds: ASK-BM or PSK-BM and the differences between them are discussed. A

complete architecture for a passive RFID tag is provided with a complete set of postlayout simulations as an example to illustrate the proposed RFID tag design methodology.

5.2 RFID System

A basic RFID system operates in a Master-Slave operation [47]. It consists of two communicating devices, the reader (interrogator) and the tag (transponder). The interrogator is the stationary device that controls the overall operation; it has a continuous supply of power. While the transponder is the mobile part and it acts as a label or identification tag. The interrogator detects the presence of any transponder in its zone of operation. Then, it sends out the RF signal carrying commands to the transponder. Consequently, the transponder responds with its stored data at the same or at a different frequency to be authorized, detected, or counted as shown in Figure 5.2.

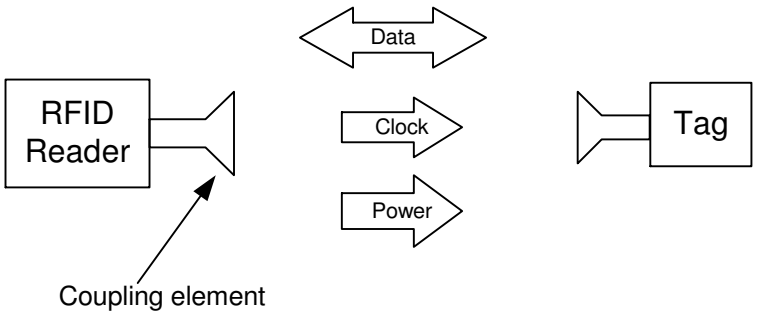


Figure 5.2 RFID Communication System

Some Interrogators are continuously sending RF signal till they detect the presence of a transponder, while some others send the signal every period of time and also some of them detect the transponders first by other means then send the signals.

The presence of many tags at the same time still can happen. The need of collision treatment algorithms is a must at some application. Anti-collision algorithms can be time, frequency or space multiplexing as shown in [48].

5.3 RFID Transponder (Tag)

The transponder is the mobile, low cost, low power consumption element in the RFID system. Transponders can be classified with respect to their power generation scheme, frequency of operation, or their read/write capability. Regarding the power generation scheme, there are three main types of RFID tags; active, passive, and semi-passive or (semi-active). Active tags are associated with batteries. This self-powered technique makes them able to detect low signals from the reader thus increasing their range of operation (achieving better sensitivity). Also, they are able to notify the Interrogator of their existence in the zone of operation, rather than waiting for the interrogator to detect their presence. This makes it suitable for many applications and saves the continuously transmitted power of the reader top detect tags.

Active transponders can edit their stored data and can save it because of the power availability. On top of that, they can transmit on a different frequency other than the interrogator transmitted frequency. This can solve the collision problem and relax the interrogator specifications and mainly the PA to LNA leakage problem as mentioned in Section 5.4.

The Active transponder structure is a typical low power transceiver structure with a simple processing unit and memory storage. The RF blocks, analog blocks, and Digital Signal Processing (DSP) blocks are all battery powered, independent on the interrogator transmitted power. Power saving techniques can be used as having an almost no-power sleeping mode and less than 0.1% transceiver duty cycle. This extends the battery life to be several years.

On the other hand, Passive transponders are much simpler and function limited. They are dependent on the interrogator transmitted power. They use the power of the received RF signal to generate their supply voltage to power up all their building blocks. Therefore, their power consumption should not go beyond micro-watts. This gives a permanent life to the tag but limits them to short-range. Their range of operation is the minimum but they are the cheapest and the most reliable tags. Interrogators dealing with passive transponders have more requirements of those dealing with active transponders. Passive transponders have the advantage of no-battery needed; they can be implanted once and never accessed again. This increases their span of applications to cover unreachable

places (inside concrete, or under ground) or human bodies (health applications). Besides having low power consumption for every building block in the passive transponder, an extra block is added which is the power generation block. This block is responsible of generating the DC supply signal for the whole transponder as it is shown Section 5.8. Table 5.1 summarizes the main comparison metrics between Active and Passive transponders [49] including the reader power, transponder power, if there is a power trade off between them or not , and a typical range of operation for each kind.

Semi-passive transponders (or semi-active) are half the way between Active and Passive transponders; also have a battery, but unlikely active tags, the battery is not used to communicate with the interrogator; it is used only for peripherals such as memory and LCD. Still RF and Analog blocks are powered using the received signal. This takes the advantage of much longer battery life and more processing capabilities to cover more applications. They also have an intermediate range of operation.

Table 5.1 Typical Power Levels and Ranges for Different RFID Transponder Kinds [49]

Tag kind	*Reader power*	*Transponder power*	*Power trade off*	*Range*
Passive	High > 1 W	null	no	< 1 m
Active	Medium < 10 mW	low < 100 μW	yes	< 10 m

Active and semi-passive tags are more costly than the passive tags and usually in many of the RFID applications the tag does not need to operate in very long read ranges

therefore passive tags are widely preferred in the industry for their low cost and good performance.

Also, the RFID transponders can be categorized to be either read-write (*R/W*) or ready only (*R/O*). The circuitry of the RFID tag should have a memory in order to store information. The tag can be read only, which will be cheaper, thus it is used in applications such as animal identification, access control and industrial automation, etc. where the data stored in the tag does not need to be updated after manufacturing and programming it. So the reader can just send an activation signal (a pure unmodulated carrier), then the tag will reply with its stored data. On the other hand, if the transponder has a non-volatile editable memory, it can be writable, so the reader acts as an interrogator in this case and can send different commands to the tag (read, write or delete), a modulated carrier is sent to the tag. In this case we need a demodulator at the tag side to interpret these commands and execute it.

Non-volatile memories such as Electrically Erasable Programmable Memory (EEPROM) or Ferro-electric Random Access Memory (FRAM) cells are used in R/W tags. Unlike EEPROM cells, the write operation a FRAM cell occurs at high speed, with typical write times in the region of 0.1μs (while 5-10 ms in EEPROM cells). Moreover, from the power consumption point of view, FRAMs offer a better performance when compared to the EEPROMs. However, EEPROMs are preferred due to the ease of integration between the CMOS processors and analog circuits in a single chip [48].

If a Passive transponder is used with a R/W operation, an additional high voltage charge pump circuitry that provides a higher power supply is required for the write operation in the memory cell. Also, the write ranges are usually smaller than the read ranges, since higher signal levels are required at the input of the tag during write operation [48]. Otherwise, an Active or semi-active transponders can be used.

Power generating circuits used in passive or semi-passive RFID tags are similar to RF power scavenging systems as illustrated in section 5.8.2.

5.4 RFID Interrogator (Reader)

RFID Interrogator is a typical short-range wireless transceiver. It acts as the master unit in an RFID system. It is a stationary device with a continuous supply of power. It is responsible of detecting tags, starting the communication session, reading their contents, and ending the session. Figure 5.3 shows the general block diagram of a typical RFID interrogator. Interacting with a passive or active tag will impact the design constraints and the interrogator specifications.

In a passive tag (or semi-passive) system: The interrogator has to detect the presence of the tag in its zone of operation. This can be done either by continuously sending a carrier in its surrounding space. Upon receiving this carrier, the transponder can generate its power signal and start sending a notification to the reader (by its id or information).

Some interrogators detect the presence of the tag first by other means (for example: infrared) and then send the needed power to save the amount of power needed for the whole communication session. After initiating the session, the interrogator is working in a full duplex mode. It has to send a continuous RF carrier to the tag to power it up and at the same time receiving the required information from the tag. The main challenges in such an interrogator are: PA to LNA carrier leakage, programmable transmitted power based on tag location, spurs rejection and Anti-collision algorithms.

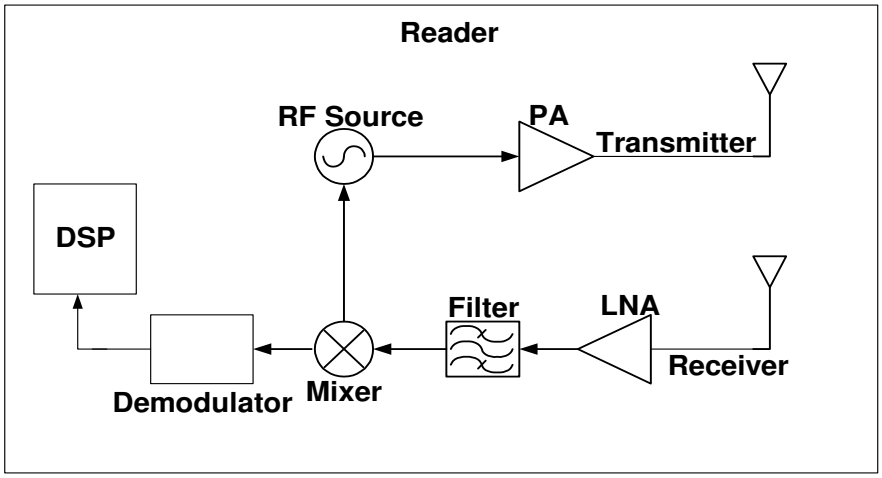


Figure 5.3 Typical RFID Interrogator Architecture

PA to LNA leakage: This happens in single antenna systems. Since the reader is sending the carrier to the tag and at the same time receiving the tag information at the same frequency. Any leakage from the output of the PA to the input of the LNA can saturate the receiver easily, as shown in Figure 5.4. A very high Q notch filter can be associated with the LNA to reject the carrier preserving on the received signal [50]. Another

solution of extracting the carrier and subtracting it leaving the received signal is also implemented [51].

Programmable transmitted power, based on tag location: The amount of power transmitted by the PA can be reduced if the tag is closer to the reader to reduce its power consumption. This can be detected by the amount of power received by the LNA terminal. *Spurs rejection*: For the full duplex operation, a stringent spurs rejection is required at the PLL output [52], spur reduction and attenuation techniques should be used.

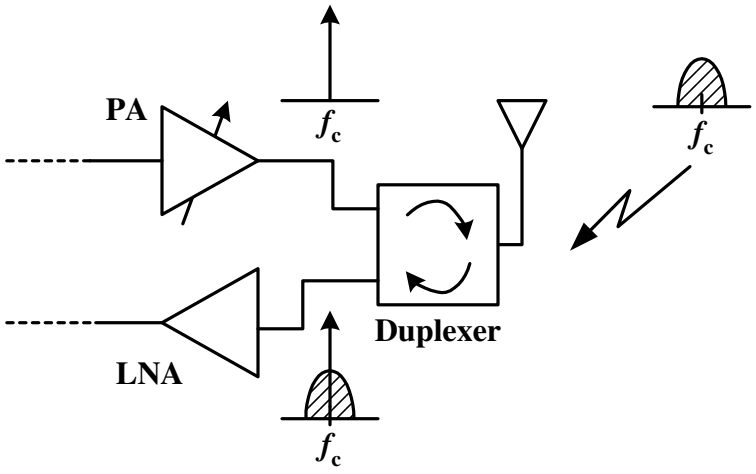


Figure 5.4 PA to LNA Leakage

Anti-collision Algorithms: In some applications, many tags can exist at the same time, if all of them start to talk to the reader, collision will occur. Time multiplexing can solve the problem to talk to only one tag at a time addressing it by its id with each command

send from the reader. Also, space multiplexing can be used, where the reader will have an antenna array with the proper phase shift between the array elements. By changing this phase shifts, the antenna beam can scan the space to work at one tag at a time as shown in Figure 5.5 [48].

In an active tag system: Either the interrogator or the transponder can start the communication session. Now, the interrogator can work in a half duplex operation and thus reducing the carrier leakage problem. For the Anti-collision algorithms and beside the time and space multiplexing, Frequency multiplexing can be used by having each tag working on a specific frequency band. This can be done in active tags, since they can generate their own separate carriers at any arbitrary frequency. There is a tradeoff between the reader power and the active tag power consumption as any two-point wireless communication.

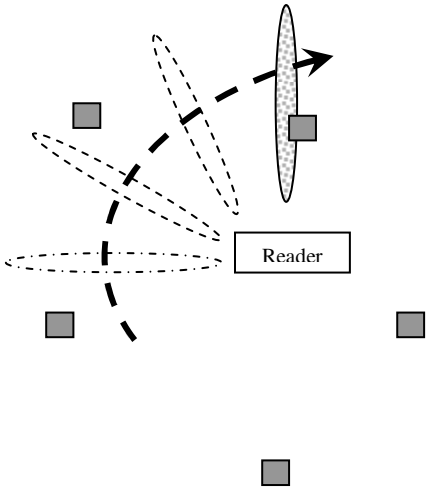


Figure 5.5 Space Multiplexing for RFID Systems [48]

Other general transceiver challenges are still applied to the reader, as phase noise and VCO pulling. The need for a global multi-standard reader is arising to be able to deal with multiple different tags in different applications.

Many RFID interrogators are presented in the literature as in [53-57] running in the 860-960MHz frequency ranges. A typical specifications for an RFID interrogator is shown in Table 5.2 [58]. For 13.56MHz, RFID interrogators are much simpler. It has a simple digitally driven antenna driver, and the demodulator is directly connected to the antenna. No frequency up-conversion or down-conversion is needed [59].

Table 5.2 A Typical RFID Interrogator's Specifications

Metric	*Value*	*Comments*
Power Consumption	540 mW	
Frequency of operation	860-960 MHz	
Transmitter output power	10 dBm	
LO Phase noise	-120 dBc/Hz	@ 1MHz
Output spurious emissions	< 50 dBc	
Receiver Sensitivity	-85 dBm	@ 40 kbps
Receiver IIP3	2dBm	

5.5 RFID Frequency Bands and Standards

Another important differentiating criterion for RFID systems is the operating frequency. There are four main frequency bands used for RFID systems. Low frequencies, at 125-134 KHz, have very small read range of operation (~10 cm), cheap tags, and high penetrating capability. High frequencies, at 13.56 MHz, have the same capabilities with higher range of operation (~1m). UHF at 900 MHz has the maximum range of operation (2-5 m) but with less penetrating capability and higher cost. Frequencies at 2.4 GHz have lower range of operation (1-2 m) and higher cost but can transmit high data rates [48, 60].

The frequencies of operation can be selected based on the application, the transmission medium, and the range of operation. High frequencies can work for higher ranges and need active tags.

Passive transponders can work at any frequency band, however the popular operating frequencies in the industry are 13.56MHz and 900MHz due to their lower cost and maximum range of operation respectively. As the frequency goes higher, active transponders is the optimum choice for acceptable range of operation.

Coupling between the antenna of the interrogator and that of the transponder is a very important issue and frequency dependent. It can be inductive coupling at low and

medium frequencies for passive tags, where the tag is operating in the near field of the interrogator antenna. In this case the antenna should be a coil with sufficient number of turns to collect enough energy for its operation. Also, propagation coupling is used at higher frequencies, where the tag operates in the far field of the interrogator antenna for passive, semi-passive, or active tags. In this case the antenna is an E-dipole with dimensions proportional to the wavelength of the operating frequency [61]. Table 5.3 shows different frequency bands and their performance metrics [62].

Table 5.3 Frequency Bands and Performance Requirements

Frequency Bands	*Antenna Components*	*Read Range*	*Orientation*	*Applications*
Low Frequency (LF) 125 KHz to 400 KHz	Coil (> 100 turns) and capacitor	Proximity (<0.5m)	Least	Proximity
Medium Frequency (HF) 4 MHz to 24 MHz	Coil (< 10 turns) and capacitor	Medium (<1m)	Not much	Low cost and High volume
High frequency (UHF) > 900 MHz	E-field dipole (a piece of conductor)	Long (<3m)	Very high	Line of Sight Long range

It is noticeable that using passive tags at 13.56 MHz with inductive coupling will not give more than 1 meter range of operation. So, how to increase this range? There are different methods to improve the range of operation; either to increase the power of the interrogator signal (where FSS regulations appear as a hard limit), or use a combination of highly directional antennas and multi-element array techniques. So there is a trade off

between power and area to increase the range of operation. Other trade-offs are shown in Section 5.7.

Several standards, tailored towards specific applications for passive RFID tags, have been developed. However, there is no unifying RFID standard. As a result, current RFID tags face potential compatibility problems with the existing systems. Several organizations are active in standardization of RFID technology. The main institutions include the International Organization of Standardization (ISO), EPCglobal, American National Standards Institute (ANSI), and the Automotive Industry Action Group (AIAG). Examples of some standards include the ISO 18000 series, ANSI INCITS 256, and AIAG B-11. Table 5.4 shows different Standards with their operating frequencies [63].

Table 5.4 RFID Standards Associated with Frequency Bands and Tag Type

	Passive	Semi-Passive	Active
125 KHz	ISO 11784/5, 14223, ISO 18000-2		
5-7 MHz	ISO 10536, iPico DF/iPX		
13.56 MHz	MIFARE (ISO 14443) Tag-IT (ISO15693) ISO 18000-3		
303/433 MHz			Savi (ANSI 371.2) ISO 18000-7, RFCode
860-960 MHz	ISO 18000-6, EPC class 0, EPC class 1, EPC GEN II, Intellitag tolls (Title 21), Rail (AAR S918)	Rail (AAR S918) Intelleflex	
2.45 MHz	ISO 18000-4, Intellitag, µ-chip	ISO 18000-4 Alien BAP	ISO 18000-4 WhereNet (ANSI 371.1)

5.6 RFID Applications

Radio frequency identification (RFID) is one of the widely investigated topics in wireless communications and is being used for a broad range of applications. The application requirements identify the RFID system specifications as shown in Figure 5.6 [48]. The expected range of operation and application medium specifies the operating frequency band. While the tag accessibility and the nature of its data specify the tag type and memory installed. Also, on the DSP and programming scale, some applications require anti-collision algorithms while others do not.

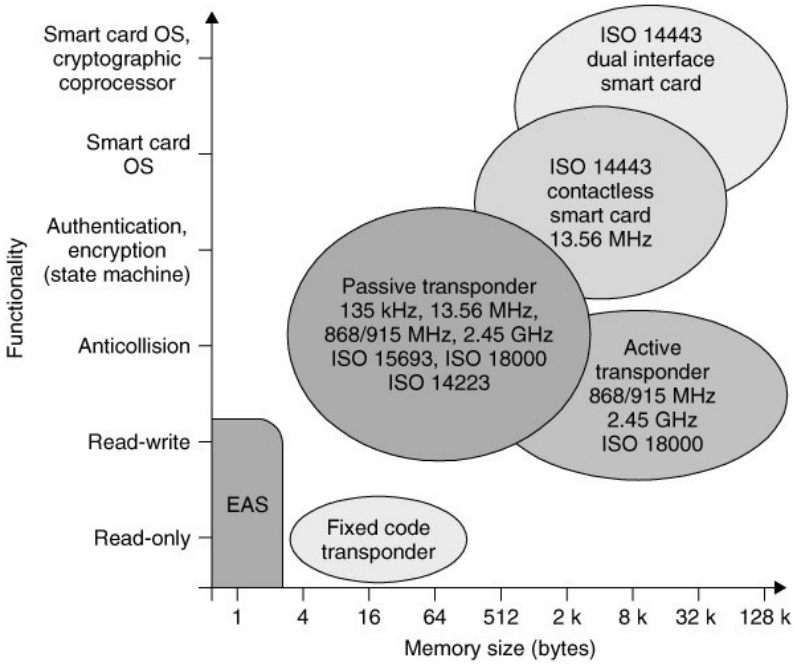


Figure 5.6 Application Specific RFID Parameters [48]

RFID can be used in *identification* as tagging of animal livestock [64], sea mammal identification [65], identification in automobile manufacturing [48], freight container identification [66], chip wafer manufacturing, weapons control, and prisoner identification. It can also be used in *tracking* as in animal vaccination history, supply chain management, supermarket's scanning [67], and airline bagging. *Security and access control* rely on RFID in many applications as employee entry ID badges, cars, secure doors, electronic shelf tags [68], and electronic article surveillance. *Sensors* can be incorporated with an RFID tag in some data acquisition systems as oil drilling pipe monitoring, temperature detection, and stress analysis for concrete units in civil engineering field. *Sports* also made use of the RFID technology by adding tags in race shoes to detect race winners, and to game tickets, and even to soccer balls to detect scoring goals and out-of-field unclear cases.

RFID technology can also be used in *medical applications*. Implantable tags are developed to be inserted in the patient's mouth, shoulder, or hand. These tags can store dental or medical records that may help in future emergency cases.

5.7 System Design Methodology

For Passive and Semi-Passive transponders, the incoming RF signal power is used to power up the Analog part. This limits other parameters from the system point of view as: transmission range of operation and data rate. A precise power budget distribution should be held to decrease the losses and improve the overall performance. On the other hand, for active tags, a system design procedure similar to that used for wireless communication standards can be incorporated. An example for such a procedure is shown in Chapter III.

A system design for an RFID communication system having a passive or semi-passive tag is presented in the following subsections. It relates the transmitted power suitable for a certain range of operation with the specific data rate, a certain modulation scheme and tag power consumption. For proper system design, one should follow the following steps.

Step 1: *Extraction of the design specifications for the target application such as:*

(a) The frequency of operation can be determined from the approximate desired range of operation, complexity involved and penetrating capability for a particular application.

(b) The antenna system should be designed efficiently, for this frequency of operation, to either be directive or isotropic, depending on the expected direction of the communication link.

(c) The data rate can be calculated from the amount of data exchanged and the required on-time of the tag.

Step 2: *Calculation of the power budget:*

The overall power incident at the input of the tag is given by equation (5.1).

$$\begin{aligned} P_{incident}\Big|_{dB} &= P_{transmitted} * (Propagation\ loss) * (Antenna\ gains) * (Multipath\ loss) \\ &= P_{dissipated\ in\ the\ antenna} + P_{absorbed\ by\ the\ tag} + P_{reflected} \end{aligned} \tag{5.1}$$

The power transmitted is the maximum power level allowed by country regulations for the specific frequency of operation. The antenna gain and loss are well defined for specific antenna dimensions. Thus, the power absorbed by the tag can be calculated for the given range of operation. The multi-path loss term is applicable only in the case of high frequency operation where long ranges can be achieved. The reflected power is dependent on the modulation index of the backscatter modulation technique, as it is discussed in Section 5.9. The lower the modulation index, the larger is the power absorbed by the tag and the higher is the range of operation achieved.

Step3: *Selection of the uplink modulation scheme (Reader to tag):*

The tag needs a minimum signal level at its antenna terminals to operate properly which determines the minimum SNR at the input of the demodulator given by equation (5.2) [44]. Since the demodulator is connected to the antenna terminals directly, the SNR level requirement determines the Bit Error Rate (BER) of the sent information.

$$SNR = Signal\ level\big|_{dB} - (noise\ floor + 10\log BW) \tag{5.2}$$

For noise floor at room temperature (-174 dBm), typical bandwidths (BW) in the range of tens to hundreds of KHz and signal levels of around 100 μW, the SNR is in the range of 100 dB. This achieves easily the BER specifications on the data demodulation requirements of the tag. Thus, the uplink modulation technique is chosen based on the tag complexity required, the tag power from step 2, and the data rate from step 1.

Step 4: *Decision on the downlink (tag to reader) modulation scheme*:

On the other side, the interrogator receives the backscattered wave from the tag with SNR given by equation (5.3):

$$SNR = P_{reflected} - propagation\ loss - (noise\ floor + 10\log BW) - NF\big|_{receiver} \tag{5.3}$$

The SNR calculated at the interrogator side is relatively small when compared to that of the tag. For a given data rate and range of operation, the SNR can be calculated. Then the backscatter modulation scheme can be chosen to achieve the required BER. Consequently, BER constraint identifies the maximum range of operation for a given data rate. If the BER doesn't meet the value stated by the application, the Noise Figure (NF) of the receiver should be reduced, demanding more power at the receiver end. Also, decreasing the NF helps to increase the B.W. by the same ratio for a given SNR. Hence, high data rates can be achieved. High data rates make the on-time of the tag shorter, decreasing the average power consumption of the system. Also, this decreases the probability of interference with other devices working at the same bandwidth of interest.

Step 5: *Decision on the implementation of the power generation circuit*:

All the previous parameters affect the power generation method as further discussed in Section 5.8.

These steps express the tradeoffs involved in the design. Several iterations can be done for an optimized solution. Following is the description of individual building blocks with the discussion of their tradeoffs and possible implementations.

5.8 13.56 MHz Passive RFID Tags

Passive RFID tags working at 13.56 MHz are the most widely spread tags in the industry. They are the simpler, the longer range of operation for the same power consumption. There are many standards dealing with such kind of tags as it is mentioned in Section 5.5. Since the tag is simple and doesn't have much processing capabilities, so it is just used in tagging and security applications. It has an ID or security code stored in it, and it releases it upon being interrogated by the proper reader.

Adding R/W capability will affect the range of operation or will require two different modes of operation; *read* phase, and *write* phase. In the read phase, the transmitted power of the reader can be low or the distance of operation can be high. On the other hand, the write phase should have more power transmitted from the reader or less range of operation.

A typical tag architecture is shown in Figure 5.7 [47]. Beside the antenna, the analog section has three main building blocks; power generator block, demodulator block, and modulator block.

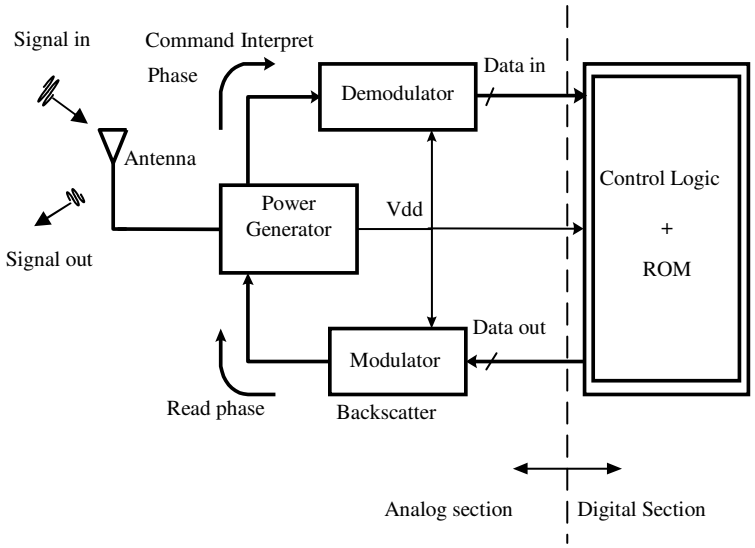


Figure 5.7 13.56 MHz Passive Tag Architecture [47]

Design trade-offs are shown in the following subsections for each building block, followed by post-layout simulations for the overall performance.

5.8.1 Antenna System

RFID antenna is one of the most critical components of the RFID system. Since the maximum power transmitted is controlled by government regulations, the antenna design determines the relation between the tag power received and the range of operation. The maximum allowed radiated electric field at 13.56 MHz is 15.848mv at a distance of 30m away from the transmitting antenna [69, 70].

At 13.56 MHz, inductive coupling is used because the estimated range of operation (1-1.5m) lies in the near field of the transmitting antenna. Loop antennas are used due to their realistic dimensions at low frequencies compared to dipole antennas.

On the transmitter (reader) side, the radiated magnetic field (*B*) at a distance (*r*) away from the center of the transmitting loop antenna is given by equation (5.4) [71]. Where *N* is the number of turns of the transmitting loop antenna, *a* is the radius of the loop, *I* is the current flowing into the loop, and μ_0 is the free space permittivity.

$$B = \frac{\mu_0 I N a^2}{2\left(a^2 + r^2\right)^{3/2}} = \frac{\mu_0 I N a^2}{2r^3} \qquad for\ r >> a \tag{5.4}$$

On the other hand, the induced voltage on the terminals of the receiving loop antenna placed at such a distance (*r*) is given by equation (5.5) [71]. Where *N* is the number of turns of the receiving loop antenna, S is the surface area, and B is the magnetic field incident on the antenna calculated from equation (5.4).

$$V = -N \int \frac{d\underline{B}}{dt} \bullet d\underline{S} \tag{5.5}$$

It is easily noticeable that increasing the number of turns could increase the power received, but on the contrary it increases the antenna losses as well. Also, increasing the antenna surface area will lead to an increase in the received power but it will increase the

area and thus the system cost. This trade-off can be optimized based on the application and the area available at the interrogator and the transponder sides.

Loop antennas are not isotropic antennas; they have maximum transmission/reception efficiency in one direction and have a zero power transfer in another direction. In some applications, where the tag orientation relative to the transmitting antenna is not guaranteed, multiple transmitting loop antennas can be used to form a 3D-antenna or an isotropic antenna system and thus covers any direction in the space [72]. Figure 5.8 shows different types of antennas that can be used in RFID systems [73, 74]. For MHZ range frequencies, loop antennas are dominating for their superior performance versus area and cost.

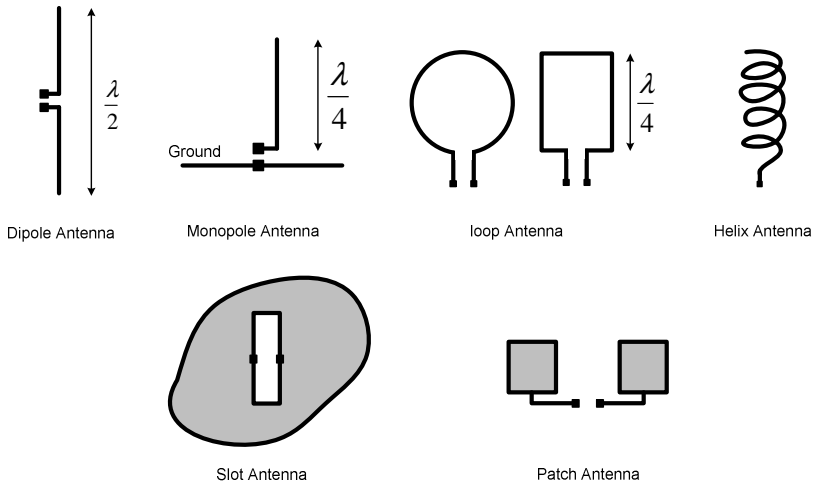


Figure 5.8 Types of Antenna

5.8.2 Power Generating Block

Power generating block is one of the most important blocks in a passive tag. It is directly connected to the antenna and it is responsible of converting the power incident on the antenna to a supply voltage, useful to operate the entire tag circuits.

The circuit losses should be as minimal as possible and the output supply should be ripple free to the limit of a proper operation for the successive blocks. Also, its output stage should be able to drive the rest of the tag without significant changes in the supply level. The entire block diagram is shown in Figure 5.9 [47]. For R/W tags, an additional high voltage generating circuit is used. It operates in the write mode only to provide the voltage necessary to edit the EEPROM memory module. This mode needs more power incident to the antenna, and this can be achieved whether by reducing the range of operation or by increasing the transmitted power as mentioned earlier. RF power scavenging systems use the same technique to generate the necessary DC power from the stray radio frequency energy [75, 76]. Whereas the RFID is using the interrogator transmitted signal to generate its DC supply, other RF scavenging systems are using stray radio frequency energy from different frequency bands. This requires complicated antenna arrays to cover more frequency bands, as shown in Figure 5.10. Such systems are designed for sensors, where an interrogator power may not exist all the time. Other energy harvesting techniques from other sources as solar, thermal and pressure are addressed in the literature [77-79].

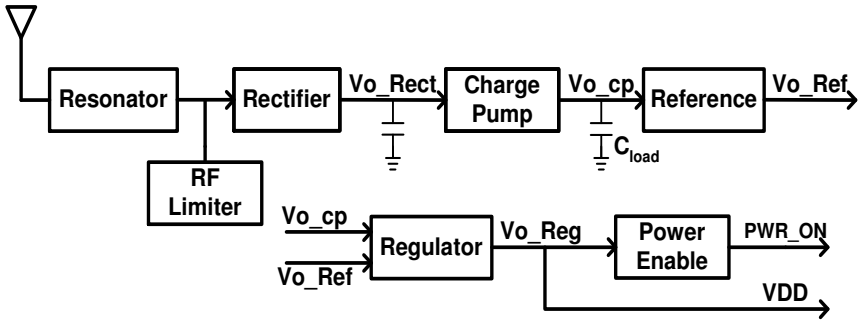


Figure 5.9 Block Level Diagram of the Power Generation Block [47]

Resonator block: It is a passive Band Pass Filter (BPF) composed of an inductor and a capacitor. It resonates at 13.56 MHz (frequency of incident carrier) to provide a significant voltage gain for the incoming signal. This signal conditioning stage is used to have a proper voltage swing at the rectifier input to be able to switch its diodes On and Off. The inductor of the resonator is the antenna inductance itself to save area and cost.

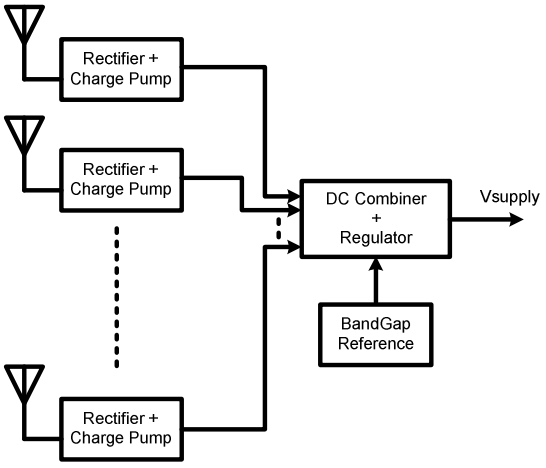


Figure 5.10 Typical RF Power Scavenging System with Antenna Array

Rectifier and Charge pump: They are used to generate the proper DC voltage to be used as a supply for the rest of the tag circuits. A full-wave rectifier converts the RF incident signal into a dc level at the input of the charge pump, which is considered a start voltage point for it. The charge pump has multiple cascaded stages. Each stage uses the RF signal as a clock and by switching it increments its input voltage level by (ΔV) and delivers it to its output. ΔV is dependent on the RF signal amplitude (received signal and resonator gain) and on process parameters (V_{th}). The number of the stages determines the voltage level at the output of the charge pump [80-82]. In some other passive tags, the charge pump can be replaced with another rectifier. This can build the required DC supply voltage but it can be more sensitive to load variations [83].

RF limiter: It is used to protect the circuit from being damaged due to any large increase in the received power level. This can happen if any high blocker is received within the antenna bandwidth or due to close communication with the reader.

The output of the charge pump has enough ripples making it unsuitable to drive the tag circuits. Voltage regulating techniques should be followed. This is one of the hot topics in RFID systems nowadays to have a highly efficient, ultra low power voltage regulation process. A *bandgap* reference is used to provide a clean voltage level to the *voltage regulator* to be able to regulate the charge pump output. Then the final output can be used as a supply voltage for other blocks.

Power enable block is used as a flag; it is activated upon reaching the required supply level. It sends a signal to indicate the power generation process is done and power supply is ready. This is a very important signal, before receiving this signal, all tag blocks are turned off, reducing the load of the regulator and thus the charge pump. This helps the power generating process to be faster and the whole reader-tag session to be shorter, thus saving power on the system level.

Also, this power on signal is used to send a signal to the reader to inform it of the tag existence and that it is ready to receive commands.

5.8.3 Demodulator Block

The demodulator circuit is also connected directly to the antenna terminals. After the power generation process occurs, the demodulator has the available power and is ready to receive the commands from the reader. It is responsible of interpreting the date sent by the tag and transfer it to the DSP unit in bits. In some passive tags, the demodulator is also responsible of generating the clock from the incoming signal and transfers it to the DSP.

The modulation technique used in the uplink communication (reader to tag) should be as simple as possible to reduce the burden on the tag demodulator.

Amplitude Shift Keying (*ASK*), Frequency Shift Keying (*FSK*), and Pulse Width Modulation (*PWM*) are the most popular schemes due to the simplicity of their demodulator circuits [80, 84-86]. On-Off Keying (OOK) can also be used which is an ASK with 100% modulation index.

Using ASK or FSK requires some sort of encoding (e.g. Manchester encoding) [48], to have an amplitude transition every bit or every clock cycle. This means the clock is embedded in the data and available for extraction at the tag side. PWM has a superior performance in this problem, since the clock is inherently available in the data stream as shown in Figure 5.11. There is a pulse every clock cycle with a deterministic rising edge at the beginning of each bit. Only the width of the pulse changes with the bit information. There is no need for encoding in this modulation scheme.

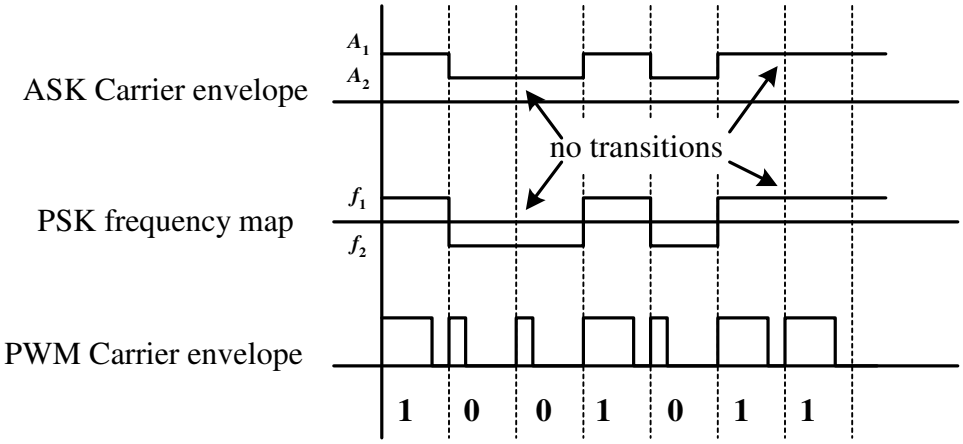


Figure 5.11 PWM has Inherent Clock Information

The PWM demodulator block diagram is shown in Figure 5.12 [47]. The envelope of the carrier is detected and the data itself is used as a positive edge clock for the rest of the DSP circuits. The unbalanced duty cycle of the clock should not affect the operation of any digital circuit as long as they are positive edge triggered and not level sensitive.

The choice of the modulation scheme is also affecting the power generation process. Since this process should continue till the end of the session, the modulated received signal should have enough power to keep it going. If an OOK is used and a pattern of successive logic '0' is received, the received power will go to zero for a significant time period. The charge pump should be robust enough to keep its output voltage level within the acceptable range. This limits the amount of successive bits carrying logic '0' to be sent to the tag. Even ASK (with modulation indexes less than 100%) will have the same problem but on a different scale.

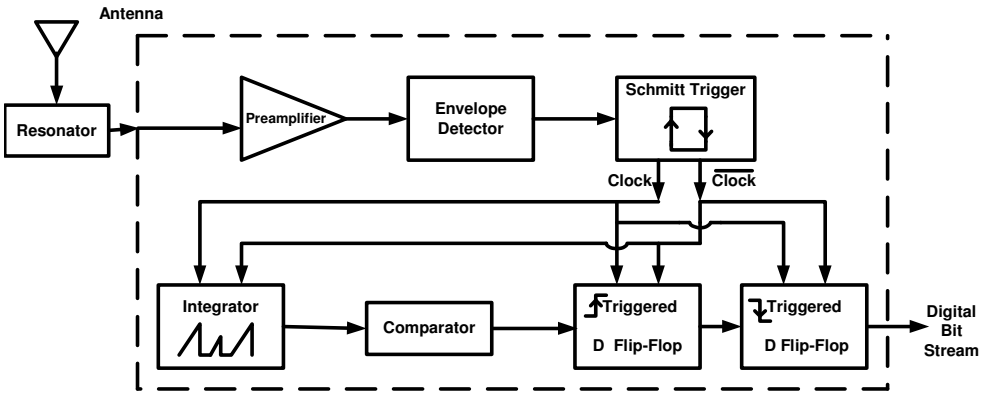


Figure 5.12 Block Level Diagram of the PWM Demodulator Block [47]

It is easily noticeable that FSK is the best choice to overcome this problem, where its envelope is always constant irrespective on the sent data. On the other hand its demodulator is more complicated. PWM comes as an intermediate solution to give no constraints on the transmitted bits with a simple demodulator circuit.

Increasing the pulse widths of logic '0' or logic '1' should solve this problem, as this reduces the time of zero power reception. On the other hand, if the two pulse widths are close to each others, this will increase the Bit Error Rate (BER). This trade-off can be resolved by testing the effect of different pulse widths on the charge pump and reach the optimum choice.

5.9 Backscatter Modulation Block

Passive tags do not have enough power to generate a carrier, modulate it, nor to have a full transmitter circuit. A modulation scheme providing an effective way of transmitting data with a simple implementation and negligible power consumption should be used in the downlink between the tag and the reader.

Backscatter Modulation (BM) is frequently used in microwave tagging or sensor systems for interrogating remote devices. A necessary background needed to understand and design the Backscatter modulator circuit in the RFID system is introduced. Previous work will be presented accompanied by its results. A simple circuit for BM will be

proposed. A brief comparison will be held at the end showing the advantages of our proposed circuit in this specific frequency range (13.56 MHz).

5.9.1 Basic Idea

In backscattered modulation technique (BM), the data stream from the DSP section after encoding is used to modulate the input impedance of the antenna. This impedance variation affects the matching property of the antenna circuit by introducing a mismatch factor proportional to the data level, '0' or '1'. Then, a portion of the incident wave will be reflected back to the receiver in the interrogator according to the mismatch factor introduced. The three different kinds of modulation schemes for backscattering are OOK, ASK with arbitrary modulation index (MI), and PSK. Figure 5.13 shows the block diagram of a backscatter implementation.

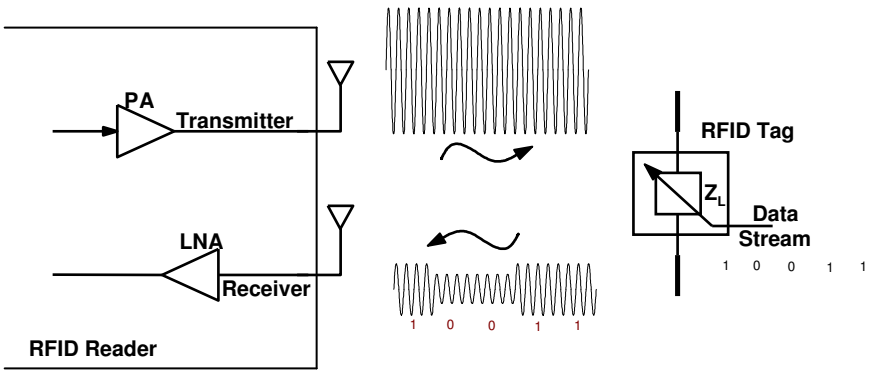


Figure 5.13 Backscatter Communications between a Passive Tag and a Reader

OOK-BM is achieved by switching the input impedance from the matched state to a complete mismatched state (open or short). Ideally, the reflected signal will be either 'no-signal' or the entire incident signal itself. But, due to the lossy nature of the antenna, the reflected signal will have certain attenuation. OOK has the disadvantage of zero power reception in case of mismatch which puts constraints on the transmission of data and necessitates a proper encoding scheme. By matching the imaginary part of the input impedance to the antenna impedance; and using the data stream to modulate the real part by the same percentage around the matching state, ASK-BM is obtained. The disadvantage of ASK-BM is the power loss in the real part of the impedance introduced by the antenna. PSK-BM is realized by alternating the imaginary part of the input impedance by controlling the phase of the reflected signal. In this case, there is no power loss during data transmission as opposed to ASK or OOK which makes PSK-BM the suitable scheme for the tag. However, the implementation of PSK-BM circuit is more complex than the other two schemes. Thus, there is a design tradeoff for the implementation of Backscatter Modulation between detection performance and complexity.

To compare between these three schemes, the equivalent circuit of the antenna in the receiving mode is analyzed and the average power reflected, the average power absorbed by the tag, and the average power dissipated in the antenna and the modulator circuits are calculated in each case. A detailed study is previously reported [80] and is

summarized in Table 5.5 where, m is the modulation index of the reflected wave, and P_{avail} is the power received by the tag in the matched condition.

Table 5.5 Comparison between Different Backscattered Modulation Techniques [80]

Modulation Technique	Power absorbed by the tag	Power back scattered to the interrogator	Power dissipated in the modulator circuit
ASK (On-Off Keying)	$\frac{P_{avail}}{2}$	$\frac{P_{avail}}{4}$	$\frac{P_{avail}}{4}$
PSK-BM ($\pm m$)	$(1-m^2)P_{avail}$	$m^2 P_{avail}$	0
ASK-BM ($\pm m$)	$\frac{1-m^4}{(1+m)^2} P_{avail}$	$m^2 P_{avail}$	$\frac{2m(1-m)}{(m+1)} P_{avail}$

It can be found from this comparison that the PSK is the most suitable backscattering scheme as it saves more power needed to energize the passive tag. The power dissipated in the antenna should be minimized to approach zero by proper design, the modulation index should be symmetric in sending logic '0' or logic '1' ($\pm m$). To choose the optimum modulation index (m), the minimum power needed by the charge pump to supply the DC for the tag during the data transfer from the tag to the reader should be taken into account.

5.9.2 Different Backscatter Modulator Circuits

The OOK circuit can be implemented by using a switch to connect or disconnect the tag to the antenna. The data stream to be sent to the reader controls this switch. ASK-BM uses a similar circuit but uses an additional resistor to introduce the mismatch factor. An illustrative diagram for the ASK is shown in Figure 5.14a [62].

ASK circuits are much simpler than PSK, but its inefficient power usage and low immunity to noise (where the information is added to the amplitude) makes PSK more preferable. The circuit implementation of the PSK is different, where variations are introduced in the capacitance instead of the resistance. This way a complex reflection coefficient is created that consequently changes the phase of the reflected signal according to the introduced variations [87].

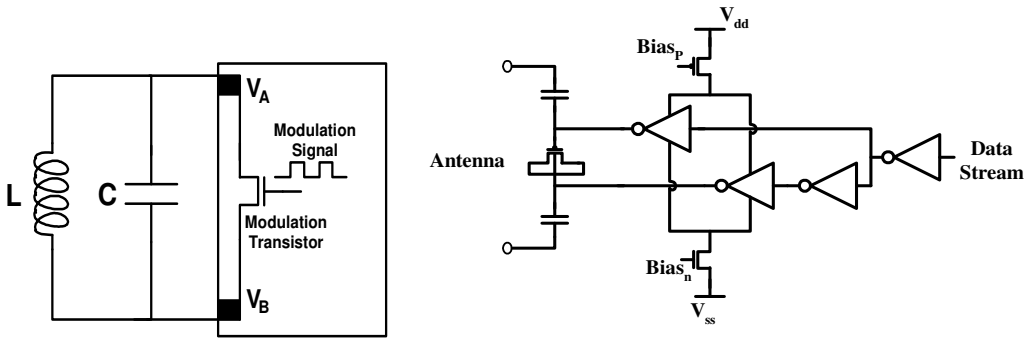


Figure 5.14 a) Modulation Signal and Modulated Signal [62], b) Block Diagram of the PSK-BM [80].

In Figure 5.14b [80], the input impedance is changed with the help of a varactor and two additional on-chip capacitors. For this circuit, the variations in the input capacitance are not very large (~ 500fF). These small variations are not significant at low frequencies (13.56 MHz, or 125 KHz). Therefore, very low modulation indexes will be achieved, which will be undetectable by the reader, as shown in Figure 5.15.

For very low frequencies (~ KHz), capacitor multiplier circuits can be used [88] at the cost of increasing the power consumption. This proves to be an optimal solution for ultra low-frequency active tags.

For 13.56 MHz, a capacitor array with switches can be used. This idea is very simple and it just adds an extra off-chip capacitor to the matching circuit. The circuit is shown in Figure 5.16. Now, the whole smith chart is available for placing the transmitted phases and there is more freedom in choosing the suitable modulation index.

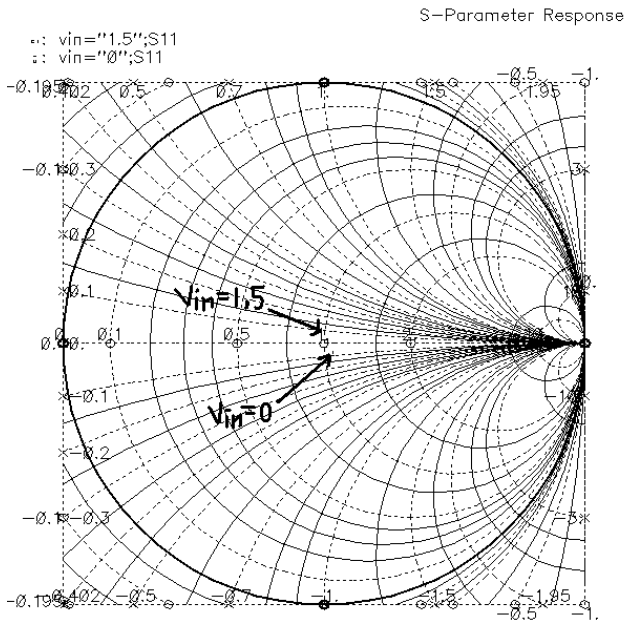


Figure 5.15 The two mismatch states on smith chart.

In this circuit, when the data stream supplies a '0', the extra branch is open circuit and the antenna can see L_1 and C_1 only (State 0). If the data stream is supplying a '1' the extra branch is now added and the antenna can see L_1 and (C_1 + C_2) (State 1). Table 5.6 compares the performance of different PSK-BM modulator circuit's implementations.

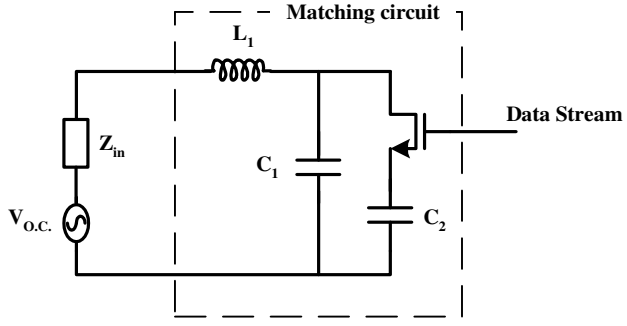


Figure 5.16 Backscatter Modulator Block.

Table 5.6 Comparison between Different Backscattered Modulator Implementations

Metrics	*[80]*	*Capacitor multiplier*	*Used circuit*
Power consumption	Low	High	minimum
Frequency range of operation	Above 900 MHz	Below 100KHz	Any frequency
ΔC variations	moderate	high	high
Area	minimum	small	Frequency dependent *
Dissipated power in antenna	small	small	small
Suitable application	High frequencies	Low frequency active tags	Moderate and low frequencies, passive tags

* Below 100 MHz we can use off-chip components while integrated components will be used in the range of GHz.

5.10 Design Example and Post-Layout Simulation Results

A design example of a 13.56 MHz Passive RFID tag, with 100 kbps data rate and a target operation range of 1m, is discussed in this section. The design methodology presented in Section 3 is followed, with some modifications to suit the low frequency used. For these frequency and range specifications, a rectangular antenna of dimensions 4 cm X 4 cm with 4 turns and a quality factor of 40 can be used at the tag side, while a circular antenna with 30 cm radius can be used at the reader side. An off-chip capacitor

should be added to realize the resonator along with the inherent inductance of the antenna coil, and to provide frequency selectivity at 13.56 MHz.

Unlike high frequency applications, the RFID tag operates in the near field of the reader antenna. The transmit antenna creates a magnetic field defined by its dimensions, number of Ampere-turns and permeability of the space of operation. The generated magnetic field strength at a distance r from the transmit antenna can be calculated as in equation (5.6). N is the number of turns, I is the current flowing in the antenna coil, a is the antenna loop radius, μ_o is the permeability of the application space, and r is the distance from the antenna loop center.

$$B = \frac{\mu_o \cdot I \cdot N \cdot a^2}{2 \cdot (a^2 + r^2)^{3/2} \cdot} \tag{5.6}$$

This magnetic field induces a voltage across the tag antenna defined by equation (5.7). N is the tag antenna number of turns, S is the antenna surface area, Q is the antenna quality factor, f is the frequency of operation, B is the magnetic field strength at the tag location, and α is the relative angle between the tag and reader antenna surfaces.

$$V = 2 \cdot \pi \cdot f \cdot N \cdot S \cdot Q \cdot B_o \cdot \cos\alpha \tag{5.7}$$

Using equations (5.6) and (5.7), for proper operation of the tag, a 2vpp is required at the antenna terminals; this requires a magnetic field of strength 0.09 μwb/m^2. For a 1m distance of operation, the reader antenna should have an Ampere turns value of 0.39. Thus the reader antenna can be one turn carrying 390mA or 2 turns carrying 195mA.

An off-chip cap is added to resonate with the antenna inductance, thus maximizing the voltage induced at the rectifier input. This voltage should exceed the rectifier dead zone for proper operation. Power loss due to substrate leakage is associated with the rectifier and defined by equation (5.8).

$$P_{loss} = \frac{1}{2} v^2 \frac{R_{sub}}{{R_{sub}}^2 + (\omega C_{sub})^{-2}} \tag{5.8}$$

Where v the device's peak RF voltage relative to the substrate

R_{sub} series resistance of Csub

C_{sub} capacitance to substrate

ω angular frequency of the RF signal

Figure 5.17 shows the rectifier used. The antenna induced voltage is used to trigger the two PMOS switches such that the common terminal is always at the higher of the two input differential voltages. The PMOS back-gate connection is connected to the output

common terminal to minimize the parasitic losses. Minimum switches' sizes are used (W/L=600n/400n), and a 10pF capacitor is used at the output of the rectifier.

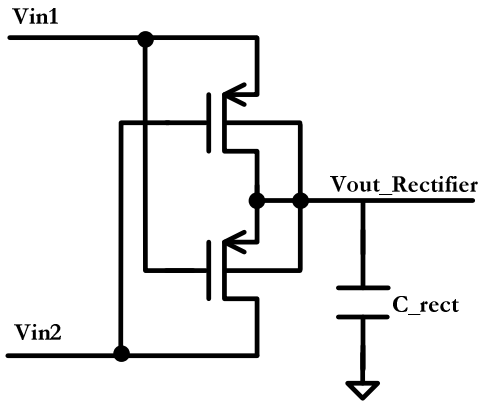


Figure 5.17 Full Wave Rectifier.

A charge pump is cascaded to boost the rectifier output to the desired supply. A generic Dickson charge pump is used [81], where the charges are pushed up in one direction using the antenna output as non-overlapping clocks. A 5-stage charge pump is used as shown in Figure 5.18 with minimum switches' sizes (600n/400n) and a capacitor value of 1pF for each stage. A ~100pF capacitor is added at the charge pump output to reduce the voltage ripples during normal operation.

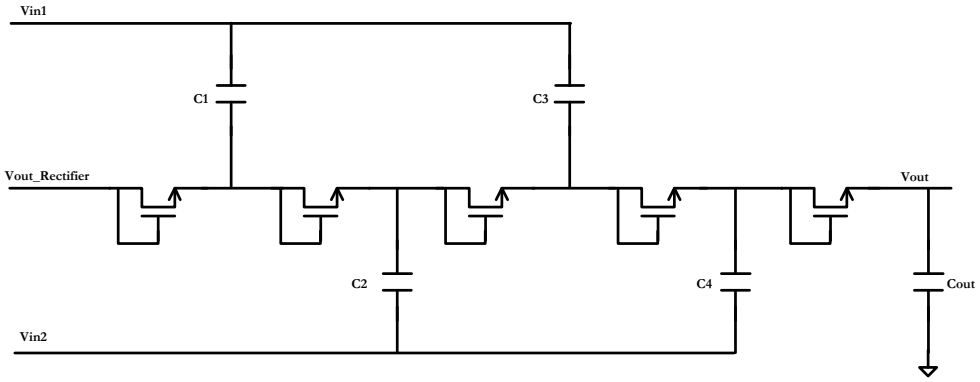


Figure 5.18 5-stage Dickson Charge Pump.

A binary PWM demodulation circuit is implemented as shown in Figure 5.19. The duty cycle of the PWM pulses are 0.8 and 0.6 to represent a '1' and a '0' respectively, for the required data rate. Due to the high input signal power level relative to the noise input, the BER performance is traded by choosing a small distance between the modulating signals to improve the performance of Power Generation circuitry.

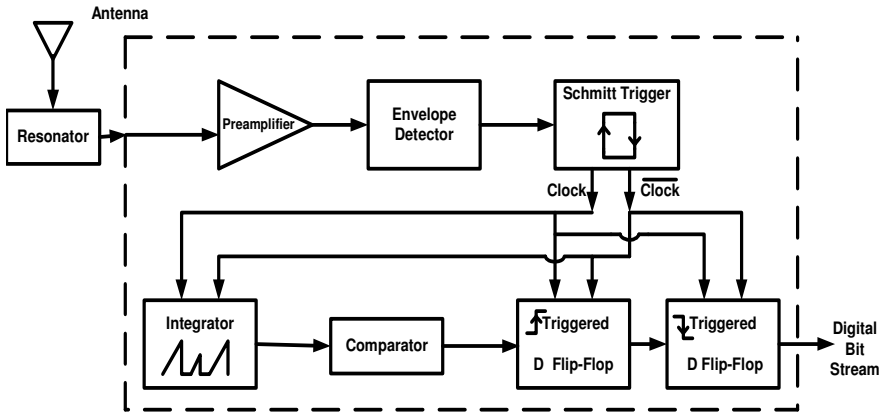


Figure 5.19 Block Level Diagram of the PWM Demodulator Block [47]

The preamplifier, envelope detector and Schmitt trigger circuits are used to recover the baseband PWM signal from the 13.56MHz carrier. Then the integrator converts the pulse width to a voltage level, thus converting time domain information to voltage domain. After being compared with a predefined voltage threshold, the comparator output gives the decided bit, either being “0” or “1”.

Figure 5.20 shows the preamplifier, envelope detector and Schmitt trigger circuits. The preamplifier is implemented using a NMOS input OTA that converts the fully differential input into a single ended output. The envelope detector is a simple diode connected MOS with an RC load to adjust charge and discharge time. Finally, the Schmitt trigger is a series of inverters to hard switch the slow signal coming from the envelope detector.

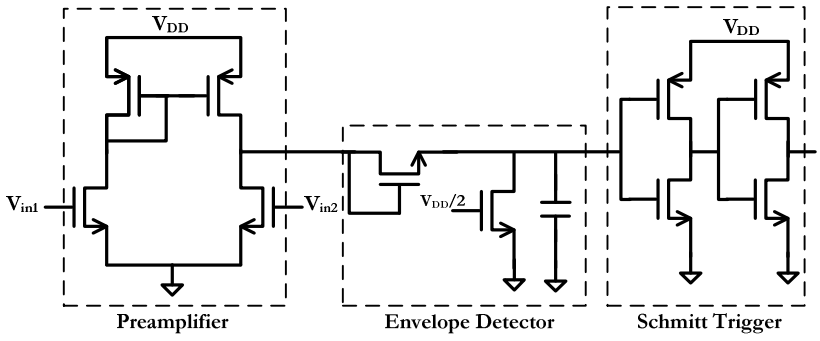


Figure 5.20 Preamplifier, Envelope Detector, and Schmitt Trigger Circuits

A simple integrate and dump circuitry is used as shown in Figure 5.21. The Schmitt trigger output is used as the clock input. Vout ramps up linearly when the clock signal is

enabled, while it goes to ground when the clock signal is disabled. During the charge time, if Vout exceeds the comparator threshold, the comparator output turns high indicating a logic "1" reception, other wise it remains zero for the current period, indicating a logic "0" reception. Figure 5.21 shows the comparator implementation.

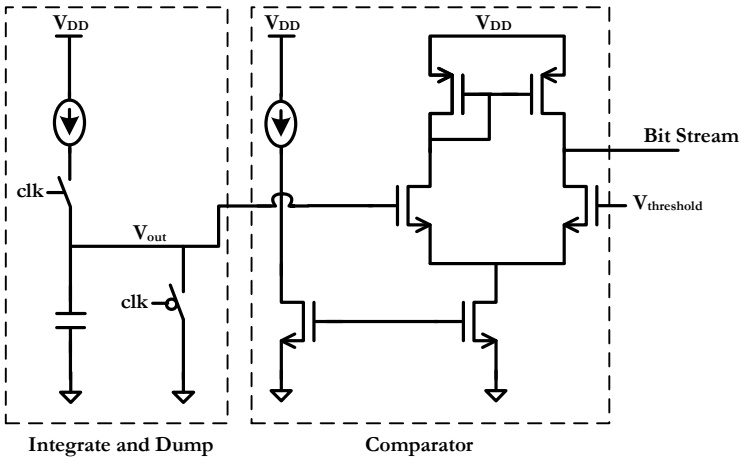


Figure 5.21 Integrate and Dump and Comparator Circuits.

For the backscatter operation, PSK-BM is preferred for its simple circuitry and power saving. The PSK-BM modulator circuit is implemented as shown in Figure 5.16. L_1 and C_1 are designed freely to identify mismatch factor for logic '0', while the value of C_2 determines the mismatch factor for logic '1'. By proper design to make both indices the same, L_1 = 1.1737 μH (off-chip), C_1 = 78.247 nF and C_2 = 156.493 nF. Using these values, the results in Figure 5.22 are obtained. The power generation circuitry is implemented as shown in Figure 5.9.

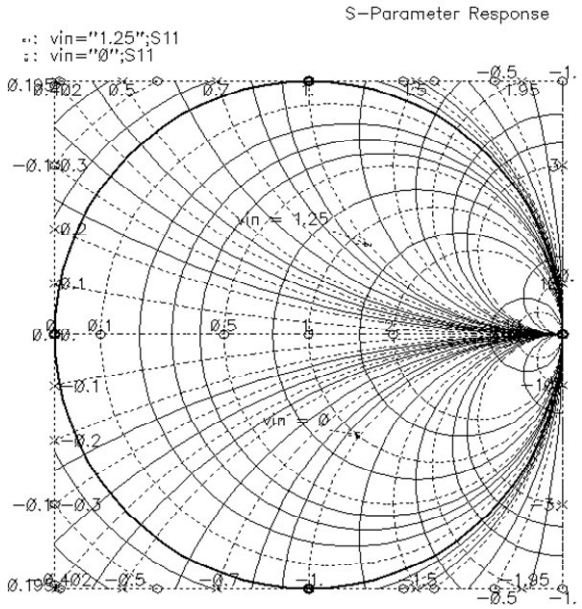


Figure 5.22 The Two Mismatch States on the Smith Chart.

Figure 5.23 [47] shows the Chip micrograph used. The tag consumes 0.64 mm^2 in CMOS TSMC 0.35 µm. The input RF power is 400 µwatt, and the generated power supply is 1.18 volt. Figures 5.24 [47] shows the postlayout simulation results of the *charge pump*, *regulator*, *bandgap reference generator.* While, Figure 5.25 [47] shows the PWM demodulator outputs for an input data stream of alternating '1's and '0's. It should be noted that the setup time of the charge pump circuit is around 150 µs. The ripples at the output of the charge pump circuit are significantly reduced at the regulator output. Successful data recovery is achieved at the output of the demodulator.

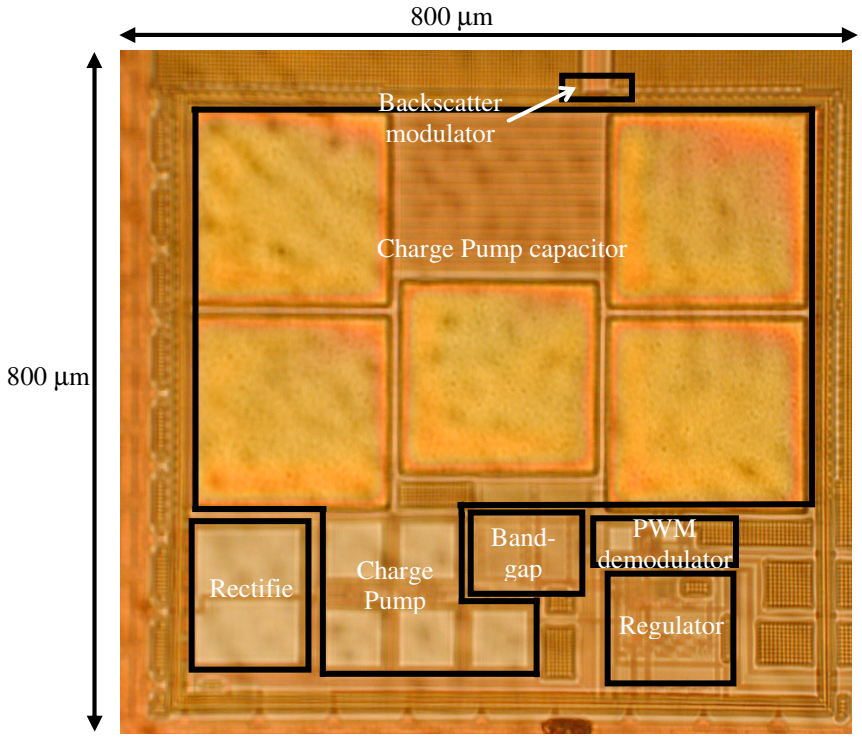


Figure 5.23 RFID Tag Chip Micrograph

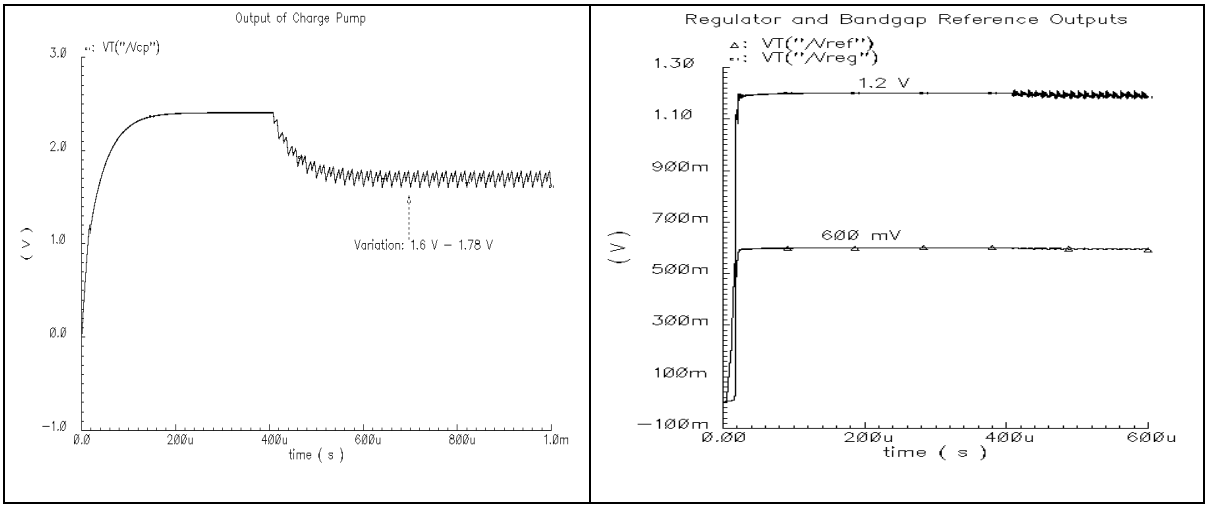


Figure 5.24 (a) Output of Charge Pump (b) Output of the Regulator and Internal Reference Generator.

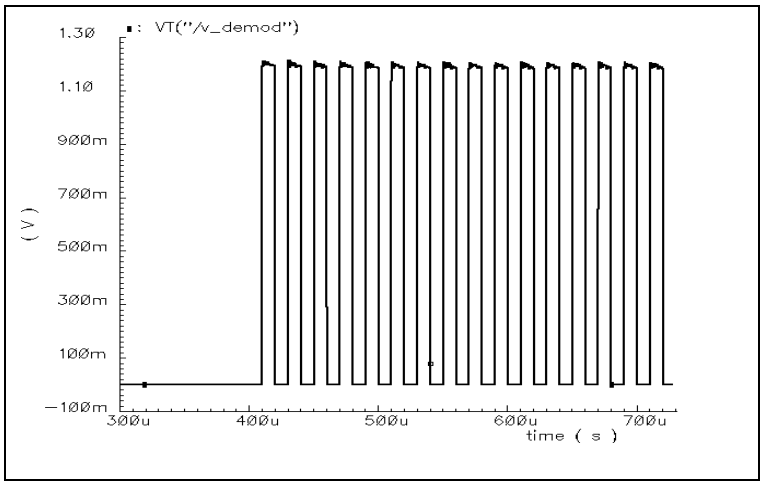


Figure 5.25 PWM Demodulator Output

5.11 Conclusions and Future Research

Passive RFID tags can work on different frequency bands, ranging from kHz to GHz. The choice of the frequency of operation affects the overall design of the tag, since it controls the complexity, the cost, and the range of operation. A complete analysis for Passive RFID tags has been introduced. Challenges and tradeoffs of each building block are analyzed. Implementation examples are provided for each block. A system design methodology is introduced where the main system equations are defined in terms of critical RFID parameters. Finally, a design example for a 13.56 MHz passive tag along with the main simulation results is provided.

RFID technology is getting involved in the industry more and more as it is clear in the widespread RFID applications. New applications appears recently as smart parking [89], capcitive pressure sensors with RFID tag for biomedical applications [90], and implantable biomedical applications [91]. However, many challenges are still in the research labs. The main challenge is to have a universal Reader [92] and a universal tag. EPCglobal is one of the organizations seeking the universal standard for RFID. Other circuit level research is still challenging, such as: highly linear reader front end, low spurs reader VCO, and ultra low power tag regulators.

CHAPTER VI

ULTRA LOW POWER 7-BIT ADC FOR BUILT-IN-TESTING APPLICATION

6.1 Background and Motivation

All currently developing circuits and research projects are targeting low cost, low power, and smaller size integrated solutions. The chip cost to the consumer includes the idea cost (patent if any), its design, technology, fabrication, packaging and testing. Thus the chip testing (either on-wafer or in-package) contributes to the whole chip cost. Reduced price testing techniques has been developed recently. But as the complexity of the system under test has grown, their testing at both, the product development and mass-production phases, has become increasingly challenging and one of the major portions of the overall cost. DSP units as memory cells and digital logic have a well developed automated tests. But still the challenges associated with the observability and test-cost of embedded analog/RF blocks remain an important bottleneck to guarantee the cost efficiency of contemporary and future integrated systems.

Conscious of these evolving challenges for the semiconductor industry, the most recent (2003) edition of the International Technology Roadmap for Semiconductors (ITRS) [93] calls for the development/improvement of solutions for different test issues. Some of the most important are: (1) Development of SoC test methodology, including test reusability and analog/digital built-in self-test (BIST). (2) Design-for-test (DfT) methods to localize failures and enable both development and production testing. (3) Wafer-level test and Known Good Die (KGD) test methodologies. (4) Analog DfT and BIST techniques that simplify test interface requirements and slow ever increasing instrument capability trends.

Several BIST and DFT techniques for analog circuits have been developed in recent years; [94-96] present a comprehensive summary of these efforts. The majority of these reported techniques have been discussed only through simulation or board-level results and important issues related to their integrated implementation have not been addressed. Few on-chip testing schemes have been demonstrated experimentally with integrated prototypes [97-100]. Some of the first devices for the test of RF circuits in the GHz range that have been evaluated with measurements employ bipolar transistors on a SiGe process [100]. Pure CMOS built-in test solutions with small area overhead, low off-chip data processing and high frequency of operation are required.

A robust technique for magnitude and phase response characterization based on an analog multiplier was introduced in [101]. Based on that approach, another system

presents a complete integrated frequency response characterization system (FRCS) is introduced in [102], where this work is part of. The goal of this system is to test the most important specifications of integrated analog circuits (gain and phase shift at different frequencies) by using very compact and simple test circuitry that communicates with automatic test equipment (ATE) through a low-speed digital interface. This work presents the Analog to Digital Converter (ADC) used in this interface. The overall application focus is on continuous time circuits operating in the range of tenths to hundreds of MHz which are the most common building blocks for baseband signal processing in SoCs. As the nature of any built-in testing, the used area should be negligible to the Circuit under Test (CuT).

Section 6.2 describes the architecture and operation of the proposed system. The design of the interface for this test architecture (algorithmic ADC) is discussed in Section 6.3. Section 6.4 presents the experimental results for the ADC as well as for the application of the entire system in the characterization of two 4^{th} order OTA-C filters. Finally, conclusions are drawn in Section 6.5.

6.2 Magnitude and Phase On-chip Characterization

Transfer function detection is the required and sufficient test for most analog systems. A general analog system, such as a line driver, equalizer or the baseband chain in a transceiver consists of a cascade of building blocks. At a given frequency ω_o each stage

is expected to show a gain or loss and a delay (phase shift) within certain specifications; these characteristics can be described by a transfer function $H(\omega_0)$. An effective way to detect and locate catastrophic and parametric faults in a given analog system is to test the magnitude and phase responses over frequency ($|H(\omega)|$, $\angle H(\omega)$) of each one of its building blocks. However, the observability of embedded analog blocks is very limited and the required equipment adds extra cost to the test process. It is desirable to add on-chip testing circuitry such that the entire SoC (both analog and digital sections) can be tested with a single digital ATE. Thus, a digital interface circuit is needed. The testing blocks should be controlled digitally, while the output data should be transferred in bits. The proposed system is meant to perform these functions as shown in Figure 6.1 [102]. The test architecture consists of a frequency synthesizer, an amplitude and phase detector (APD), a multiplexer that serves as an interface between the circuit under test (CUT) and the APD, and an ADC that digitizes the output of the APD which consists of DC voltages.

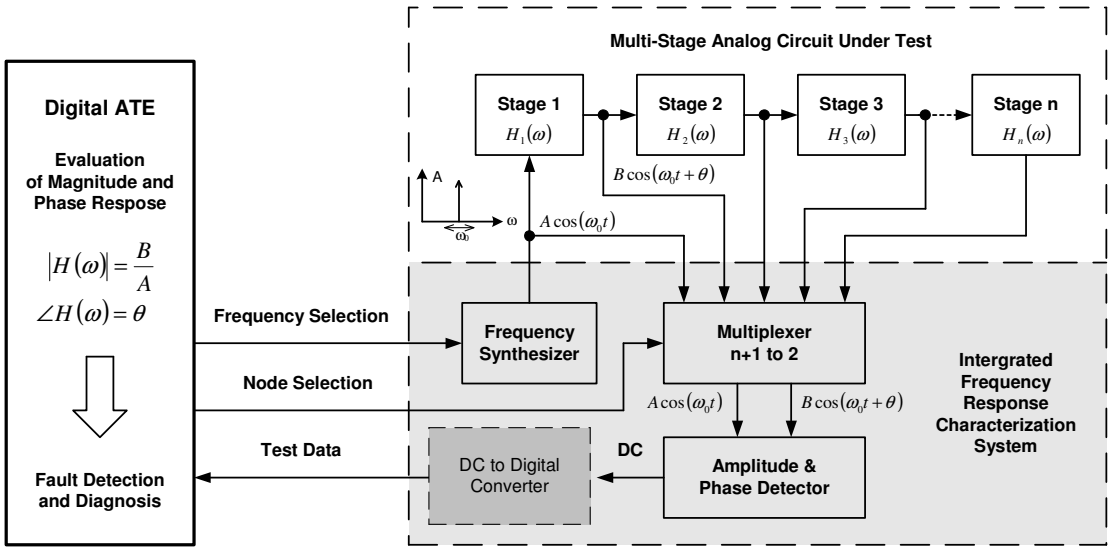


Figure 6.1 Architecture of the Proposed Frequency Response Characterization System

A block diagram of the proposed APD is depicted in Figure 6.2 [102]. The array of switches within the dashed-box is implemented in the multiplexer shown in Figure 6.1. An analog multiplier is employed to perform, in succession, three different multiplication operations between the input ($A\cos(\omega_0 t)$) and output ($B\cos(\omega_0 t+\theta)$) signals from the CUT.

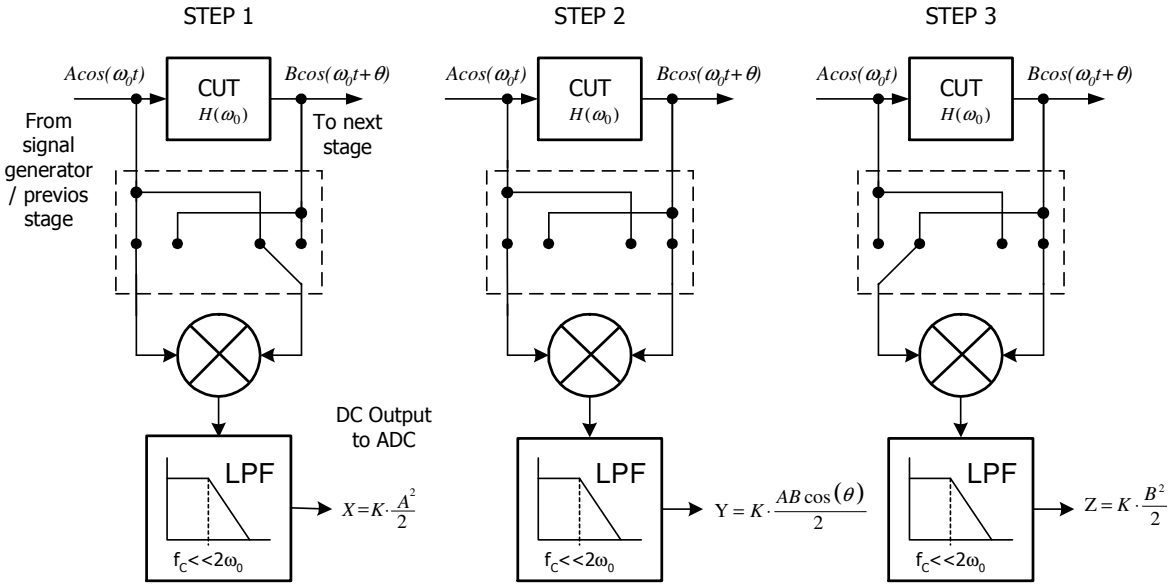


Figure 6.2 Operation of Phase and Amplitude Detector

For each operation, a DC voltage and a frequency component at $2\omega_0$ are generated; the latter is suppressed by a lowpass filter (LPF) at the output of the multiplier. The following three DC voltages are obtained sequentially:

$$X = LPF\left[k \cdot A\cos(w_o t) \cdot A\cos(w_o t)\right] = LPF\left[k\frac{A^2}{2}\left(1+\cos(2w_o t)\right)\right] = k\frac{A^2}{2} \tag{6.1}$$

$$X = LPF\left[k \cdot A\cos(w_o t) \cdot B\cos(w_o t+\theta)\right] = LPF\left[k\frac{AB}{2}\left(\cos(\theta)+\cos(2w_o t+\theta)\right)\right] = k\frac{AB\cos(\theta)}{2} \tag{6.2}$$

$$X = LPF\left[k \cdot B\cos(w_o t+\theta) \cdot B\cos(w_o t+\theta)\right] = LPF\left[k\frac{B^2}{2}\left(1+\cos(2w_o t+2\theta)\right)\right] = k\frac{B^2}{2} \tag{6.3}$$

Where K is the gain of the multiplier, A and B are the amplitude of the signals at the input and output of the CUT, respectively, and θ is the phase-shift introduced by the CUT at ω_0. From these DC outputs, the ATE can evaluate the phase and magnitude response of the CUT at ω_0 by performing the following simple operations:

$$|\theta| = \cos^{-1}\left(\frac{Y}{\sqrt{X \cdot Z}}\right) \tag{6.4}$$

$$\frac{B}{A} = \sqrt{\frac{Z}{X}} \tag{6.5}$$

Since Y is proportional to the cosine of the phase, it is the absolute value of the phase what is obtained. Notice that the parameters of interest (|θ| and B/A) are computed using only X, Y and Z. Neither the amplitude of the test signal (A) nor the multiplier's gain (K) play an important role in the computations and hence do not need an accurate control. Any static DC-offset that the multiplier may have can be measured when no signals are present and then cancelled before the computations. The cut-off frequency (ω_c) of the LPF should be only small enough to suppress the high frequency components generated at the output of the analog multiplier and does not require tuning. In this way, the proposed technique is inherently robust to the effect that process variations can have on the main performance characteristics of the building blocks of the APD.

A self-verification of the entire system can be performed by multiplying the output of the on-chip signal generator by itself and then reading the resultant digitized DC

voltage. This operation does not involve the CUT and can be performed at all of the frequencies of interest. Moreover, this procedure does not represent an overhead in terms of time since the resultant values are a vector for X, as described in equation 7.1.

The effect of the spectral content of the test signal is now analyzed. Let HD_i, be the relative amplitude of the i^{th} harmonic component (i = 2, 3, …n) with respect of the amplitude A of the fundamental tone. In the pessimistic assumption that the CUT does not introduce any attenuation or phase shift to neither of these frequency components, the DC error voltage (E) introduced by the harmonic distortion components to each of the voltages X, Y and Z is given by:

$$E = K \cdot \frac{A^2}{2} \cdot \sum_{i=2}^{n} \left(HD_i\right)^2 = K \cdot \frac{A^2}{2} \cdot \left(THD\right)^2 = X \cdot \left(THD\right)^2 \tag{6.6}$$

Where, THD is the total harmonic distortion of the signal generator. If THD is as high as 0.1 (10%), even in this pessimistic scenario the error voltage would be equivalent to only 0.01 (1%) of X. This tolerance to harmonic components is an important advantage since it eliminates the need for a high precision sinusoidal signal generator.

6.3 ADC Requirements

As discussed earlier, the output of the APD is a DC voltage hence, a low speed ADC can be used. A DC-ADC can be used for various on-chip testing and calibration purposes such as monitoring the DC operating points at different nodes of a SoC [103]. A sample and hold circuit is not needed for such a DC conversion circuit. Since the input will remain unchanged and constant for the conversion process. It will only change if the oscillator frequency changed and thus the multiplier output changes for a second point measurement.

The conversion rate is determined by the required time or the testing process, number of frequency points to be measured, as shown in equation (6.7):

$$Conversion\ \ Time = \frac{1}{Conversion\ \ Rate} = \frac{Test\ \ time * frequency\ \ step}{Test\ \ B.W.} \qquad (6.7)$$

As the conversion rate increases, the test time decreases and more tests can be achieved. This will be critical in mass production testing.

The ADC resolution is dependant on the dynamic range and accuracy needed. A variable or programmable number of bits are preferable to cover most applications.

6.4 ADC Architecture

Successive approximation (SA) ADC is the most appealing architecture for such an application, due to its small area, and low power consumption. On the other hand SA-ADC is only suitable for low frequency applications (MHz range). Figure 6.3 shows the basic structure of the SA-ADC. Sample and hold circuitry is used to fix the input signal during the conversion process. For DC input signals, the Sample and hold can be eliminated. For each analog input, the Successive Approximation Register (SAR) searches for the equivalent digital code using binary search algorithm, where it decide only one bit per step. Each step, the generated digital code is converted to analog using the DAC associated, compared to the analog input and the result help deciding the bit value. Upon finishing all the bit decisions, SAR sets an End of Conversion (EOC) signal. This generation, conversion, comparison, and decision is called *feedback subtraction* algorithm [104]. All these functions are explained in details next.

Equation (5.9) describes the basic operation per cycle of a successive approximation ADC. Where, V_{in} is the analog input, V_a is the analog equivalent for the estimated digital output, and <> denotes the comparison operation.

$$V_{in} - V_a <> 0 \tag{5.9}$$

The subtraction in Equation (5.9) is done through the two inputs of a comparator, which usually requires offset compensation techniques. In the ADC architecture introduced in [105], the subtraction is done inherently in a resistor ladder, thus the non-inverting input of the comparator has a constant voltage. This facilitates the offset cancellation of the comparator, by proper bias at its input. In that reported architecture, n comparators, n(n+3) resistors, and (n-1) output buffers are used to form the n-bit ADC.

Based on the described concept of inherent subtraction [105], a compact algorithmic architecture is proposed here; the number of components is reduced to decrease its power consumption and improve its robustness. In this architecture for an n-bit ADC, only one comparator, one resistor ladder with (2n+2) resistors, (2n-1) switches, and a simple digital controller are used. Figure 6.3 [102] shows the implemented 7-bit ADC. Two possible latch circuit designs are shown in Figure 6.4. The latch output should be either V_{ref} or Gnd, based on the input coming from the comparator. The circuit shown in Figure 6.4b is more compact and suitable for built-in-testing applications.

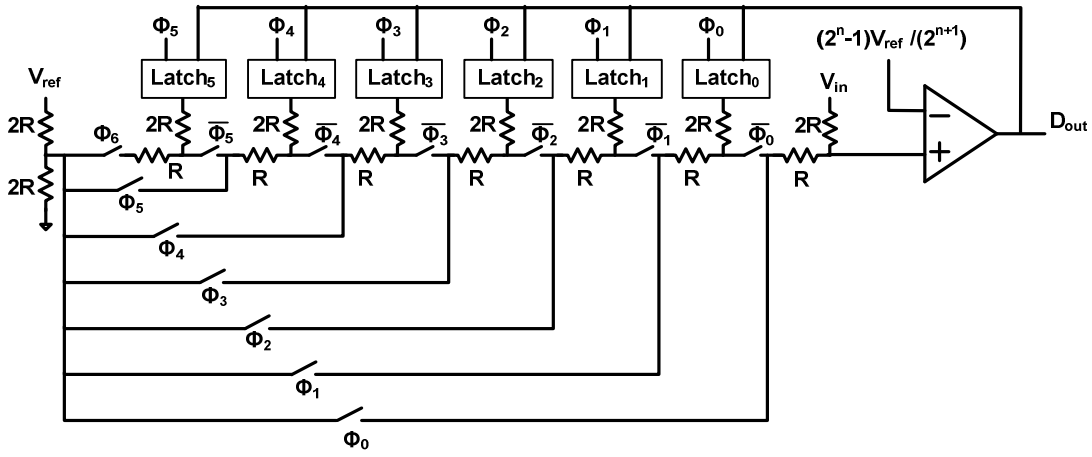


Figure 6.3 Proposed ADC Architecture

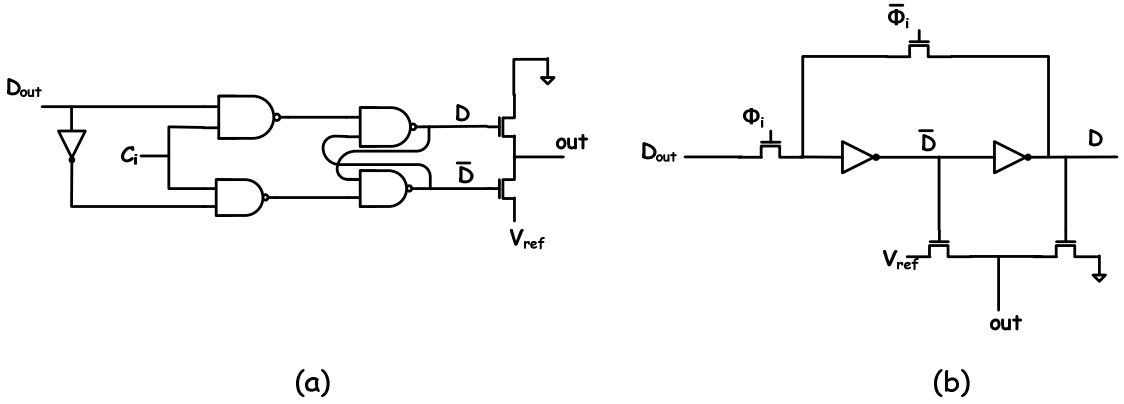


Figure 6.4 Two Possible Implementations for the Latch

The latch is used to fix the previously calculated bits to be used in the new bit decision. The control signals for the switches are shown in Figure 6.5 [102]. These time-shifted pulses and the end of conversion (EOC) signal are generated by a 3-bit binary counter with a 3-to-8 decoder.

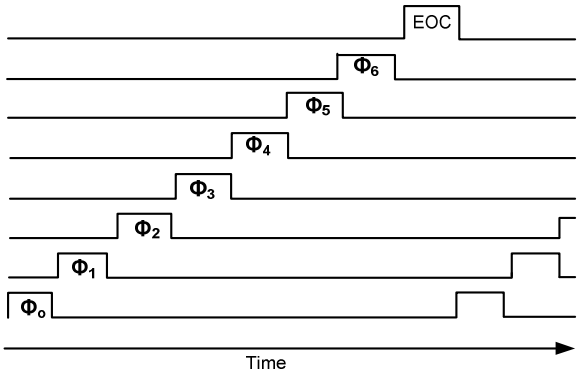


Figure 6.5 Control Signal

A simple 3-bit counter can be used followed by a 3X8 decoder. This architectures generates eight non-overlapping pulses with a duty cycle of 12.5% each driven by the input clock frequency. A set of inverters are used to provide the inverted signal needed in the circuit as well. The digital implementation of the control circuit is shown in Figure 6.6.

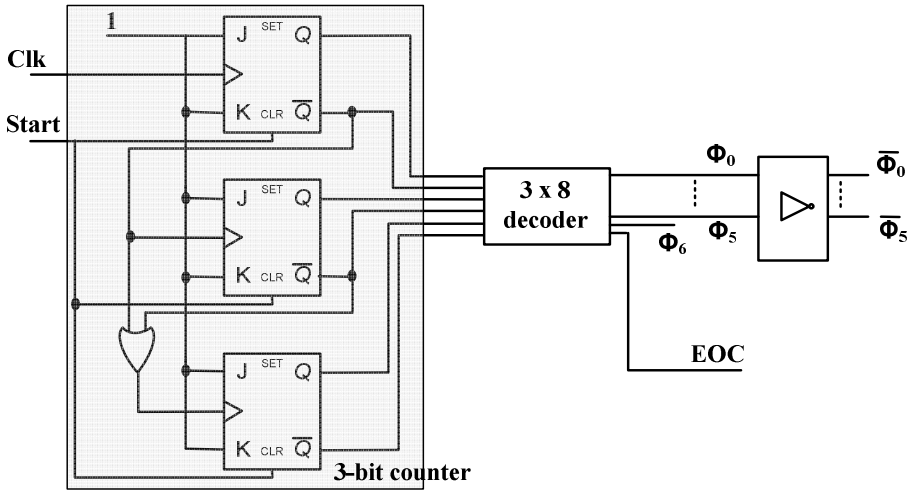


Figure 6.6 Control Circuit Implementation

Equation (6.8) represents the general operation of the proposed ADC using different control lines to generate the different bits in a recursive manner.

$$D_i = \begin{cases} 1 \; if \; \dfrac{v_{in}}{2} + \left[\dfrac{\overline{D}_7 V_{ref}}{4} + \dfrac{\overline{D}_6 V_{ref}}{8} + \; ... \; + \dfrac{\overline{D}_{i+1} V_{ref}}{2^{8-i}} \right] + \dfrac{V_{ref}}{2^{9-i}} > \left(\dfrac{2^n - 1}{2^{n+1}} \right) V_{ref} \\ 0 \;\; otherwise \end{cases} \quad (6.8)$$

$$where \; i = 7,6,...,1 \; and \; D_i = 1 \forall \, i > 7$$

The MSB (D_7) is generated first by comparing the input signal with half the input dynamic range. Then, the second bit (D_6) is resolved by using the information from D_7, and so on until the LSB is detected. By changing the status of the control signals, the resistor ladder is reshaped to calculate the corresponding bit. Figure 6.7 [102] and Figure 6.8 [102], show the first and the second time intervals to calculate D_7 and D_6 respectively.

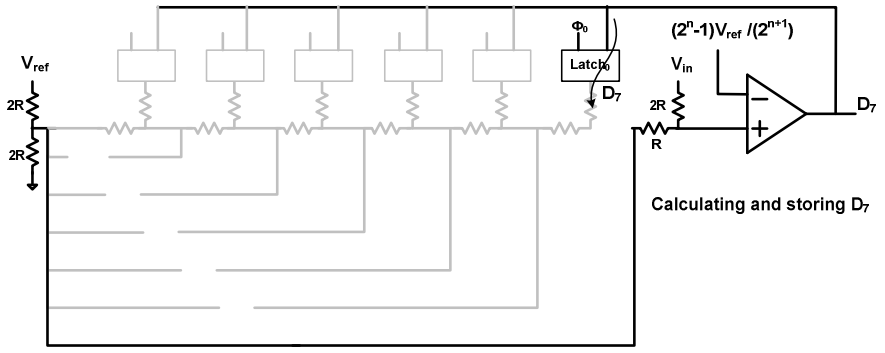


Figure 6.7 ADC Operation: MSB Detection

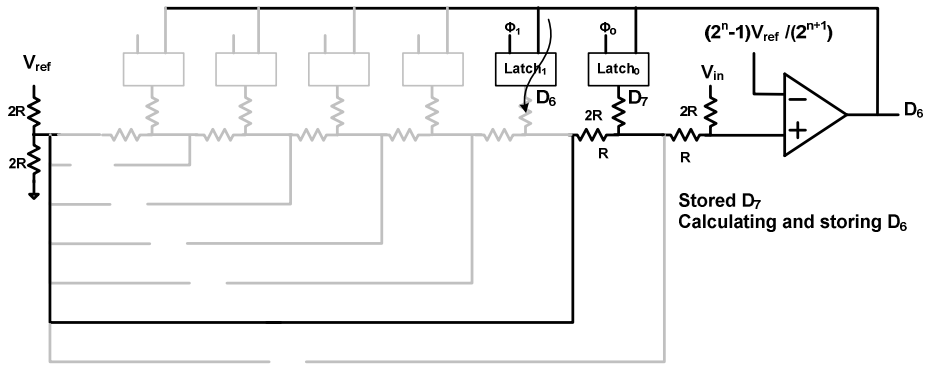


Figure 6.8 ADC Operation: 2nd Bit Detection

In this way, the digital output is taken serially and 7 clock periods are needed for a complete 7 bit conversion process. The proposed ADC operates up to 100 KHz clock frequency corresponding to 14 KHz conversion rate. The employed comparator uses an input stage, a regenerative comparator, and an SR latch in a similar way as the comparator proposed in [106]. Large resistor values are used in the resistor ladder (150KΩ) to make the effect of the switch on-resistance negligible, thus preserving accurate resistance ratios and better accuracy. By using the high resistivity n-well layer, these resistors can be implemented in an insignificant area.

As it is mentioned, the ADC is calculating the MSB first at a certain combination of the control lines. Following the second bit at a different combination and so on till it reaches the LSB and start over again for the following frequency sample. If only 3 bits are required, the ADC will calculate the first 3 bits, and then a start signal should be sent to

reset the counter and start the calculations again for the following frequency sample. This start signal is shown in Figure 6.6. Thus the number of bits can reduced to increase the conversion rate. If only 3 bits are needed, the conversion rate will increase by a factor of (7/3). This controlled programmability made this ADC capable of matching most test scenarios, by balancing the conversion rate with the dynamic range.

Due to its reduced number of components, this ADC architecture can make use of the existing circuitry in an IC compliant with the IEEE 1149.4 standard for a mixed-signal test bus [107]. In this standard, each test pin has an Analog Boundary Module (ABM) through which its DC voltage can be set, shorted to the supply, or compared with a threshold and latched as a logic value by the boundary scan test as shown in Figure 6.9 [107]. The ABM consists of a comparator, switches and a set of storage cells (Flip Flops). By incorporating simple programmability, these components can be used together with a resistor ladder to form this compact ADC for DC signals using only one ABM. This modification in the ABM leads to more accurate results in testing, where each voltage value is digitized (n-bit ADC) rather than compared with a single threshold (1-bit ADC).

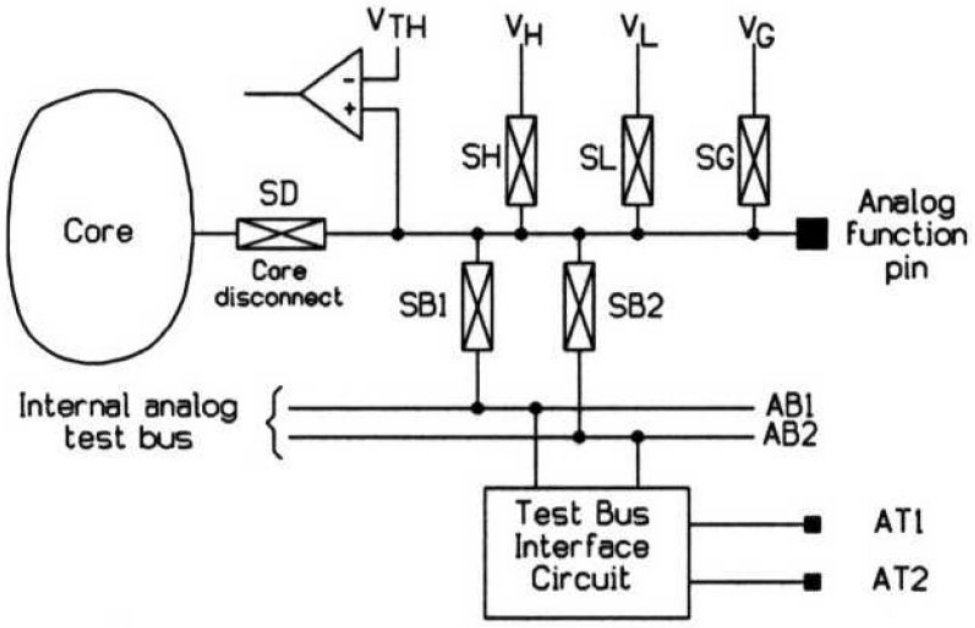


Figure 6.9 Basic ABM Structure

The presented ADC design is meant to show that the proposed system can have a complete implementation with fully digital interface in a compact area. Naturally, a more complex, high resolution ADC could be used instead if it is already available in the SoC or the ATE.

6.5 Experimental Results

The proposed system is implemented in standard TSMC CMOS 0.35µm technology and fabricated through the MOSIS service. Two different 4^{th} order OTA-C filters are

included as CUTs; a bandpass filter (BPF) with a center frequency of 11MHz and a low-pass filter (LPF) with a cutoff frequency of 20MHz. These filter's characteristics are common in the baseband section of communication systems. The chip microphotograph is shown in Figure 6.10 [102].

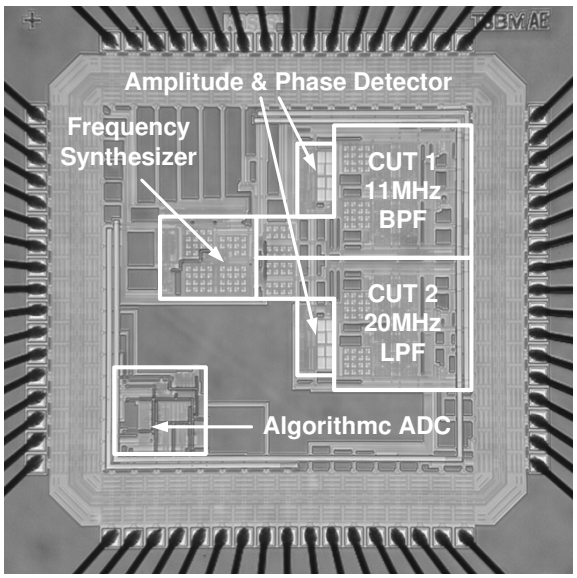


Figure 6.10 System Chip Microphotograph

The total area of the testing circuitry (frequency synthesizer, ADC and APD) is 0.3mm^2. Table 6.1 presents an area overhead analysis for the FRCS with respect to reported analog systems [108-110], which are suitable CUT candidates. Note that this area comparison is a pessimistic estimation since it is made with respect to circuits that are fabricated in technologies with smaller minimum feature sizes. The following subsections present the obtained experimental results.

Table 6.1 Area Overhead Analysis

Reference	System	Technology	Area	Overhead of FRCS
[108]	IF Baseband strip for GSM	0.25μm CMOS	1.9 mm^2	15.8%
[109]	2 MHz IQ receiver for Bluetooth	0.18μm CMOS	5.6mm^2	5.4%
[110]	Line driver for ADSL	0.25μm CMOS	5.3mm^2	5.7%

6.5.1 Algorithmic Analog-to-Digital Converter

For the test of the ADC with the full 7-bit detection, a 2 V input dynamic range is considered. Figure 6.11 shows the test setup with the equipments used. A triple power supply (Agilent 3631A) is used to provide the ADC supply as well as the analog DC input. On-board voltage regulators had to be designed and implemented on PCB using LM317 regulator, to obtain cleaner signals thus having better performance. Decoupling capacitors should be placed close to the chip for board noise rejection. Agilent 33220A is used to provide the clk input, while Agilent 5000 series oscilloscope is used to monitor the clk input, EOC signal, and serial data out. Figure 6.12 [102] shows the measured peak INL and DNL Vs. input clock frequency.

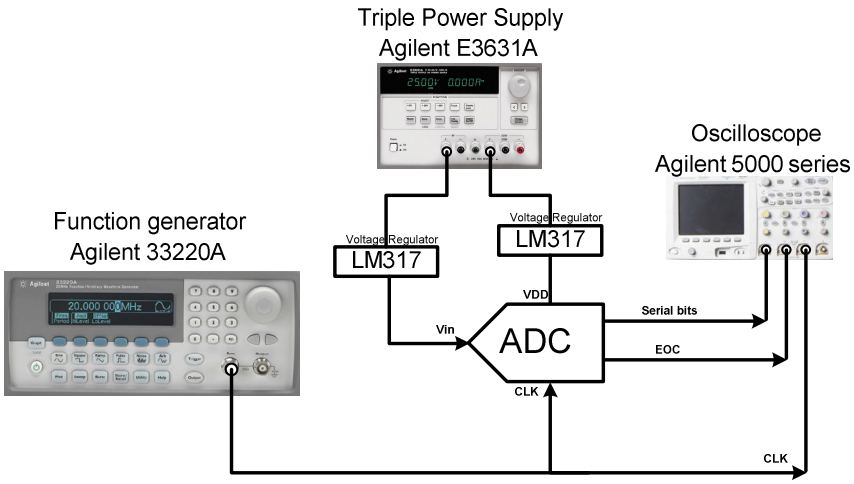


Figure 6.11 Test Setup for the ADC

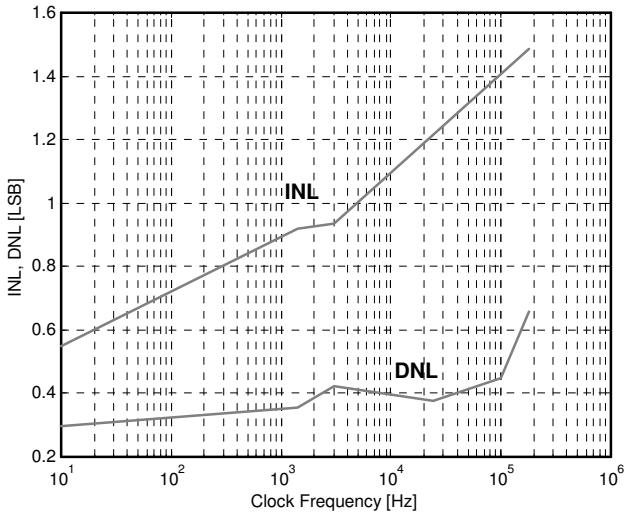


Figure 6.12 Measured Peak INL and DNL of the ADC Versus Clock Frequency

The ADC operates at a 100 KHz clock frequency (70µsec conversion time) with a peak INL of 1.4 LSB and a peak DNL of 0.45 LSB. Figure 6.13 [102] shows an oscilloscope screen capture showing the End of Conversion signal, the 10KHz clock signal and the

serial output data. An average power of 200 µW is consumed by the ADC and its area is 380µm×390µm.

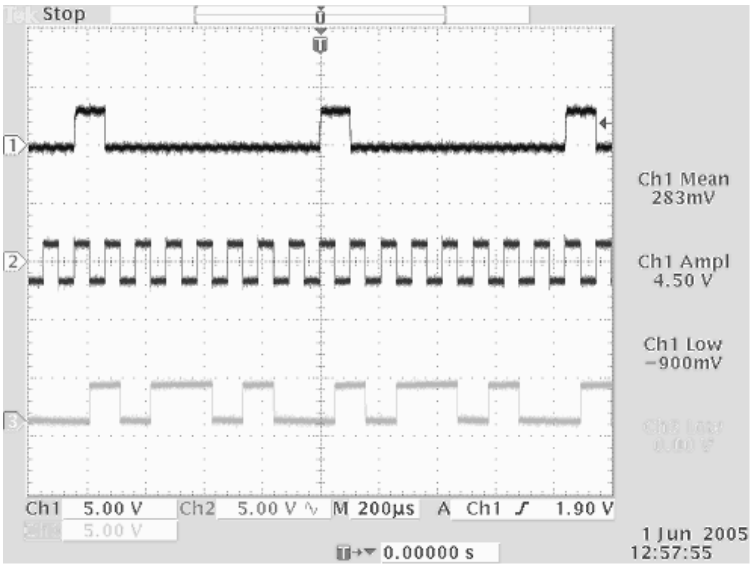


Figure 6.13 ADC Waveforms: EOC, CLK, and Serial Output Data

6.5.2 Frequency Response Characterization System

Figure 6.14 [102] describes the experimental setup for the evaluation of the entire system in the test of the integrated CUTs. Each 4^{th} order filter consists of two OTA-C biquads, and each biquad has two nodes of interest, namely bandpass (BP) node and lowpass (LP) node. In Figure 6.13, the filter configuration corresponds to the 11MHz BPF in which the output of each biquad is the BP node. For the 20MHz LPF the outputs are the LP nodes. A buffer is added at the output node of each biquad so that their frequency response can be evaluated with external equipment. The buffers are designed

to show a constant frequency response up to 200MHz while driving a 50Ω differential load through an off-chip balun.

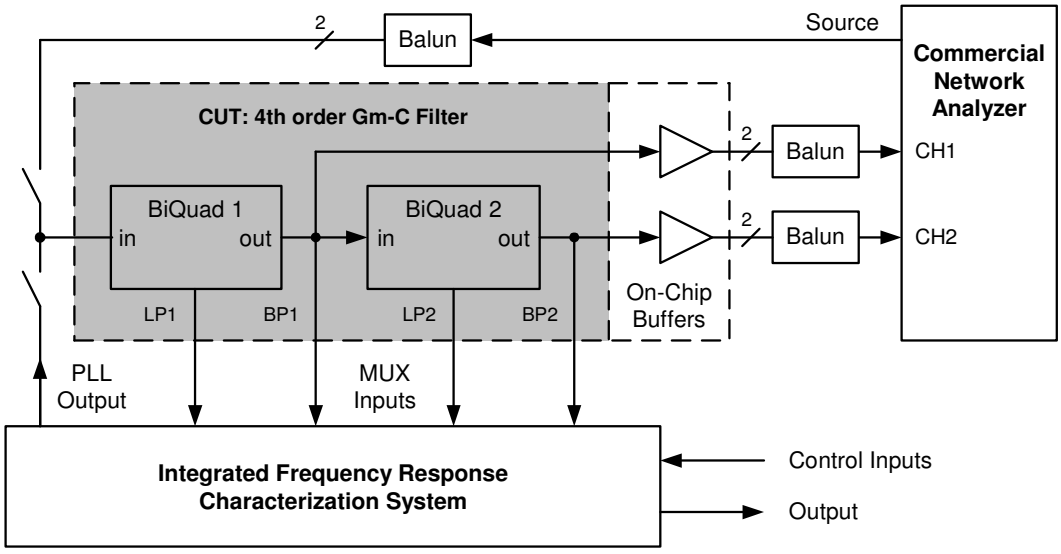
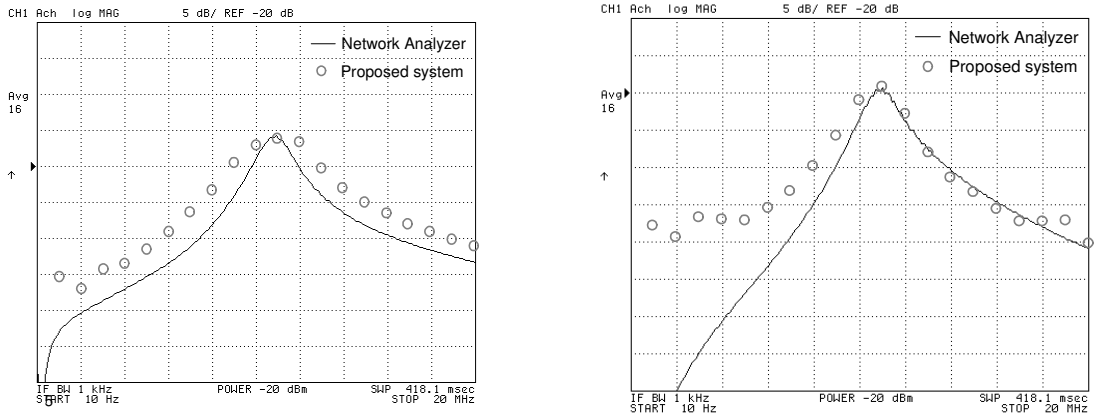


Figure 6.14 Experimental Setup for the Evaluation of the Proposed System

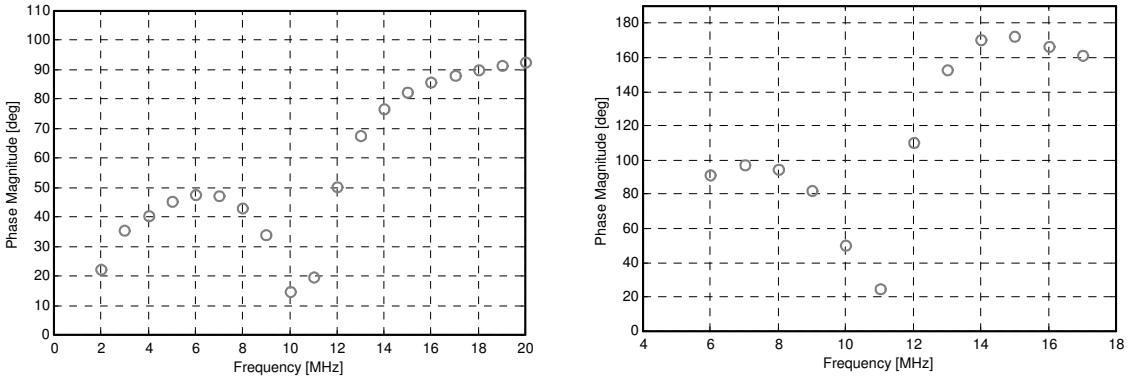
The results of the operation of the entire FRCS in the magnitude response characterization of the 11MHz BPF at its two BP outputs are shown in Figure 6.15 [102]. These results are compared against the voltage gain characterization performed with a commercial vector network analyzer. In this measurement, the dynamic range of the test system is limited by the resolution of the ADC. With 7 bits, the digitized DC voltages can take values of 1 to 128 and, as a result, the highest measurable CUT attenuation (B/A ratio as described by equation 5) is about -21dB. The phase response of the filter as measured by the FRCS is shown in Figure 6.16 [102].

The corresponding results for the characterization of the 20MHz LPF are presented in Figures 6.17 and 6.18 [102]. In this case, the DC output of the APD is measured through a data acquisition card with an accuracy of 10 bit. As it can be observed, the APD is able to track the frequency response of the filter and perform phase measurements in a dynamic range of 30dB up to 130MHz. On average, in the test of both CUTs, the magnitude response measured by the off-chip equipment is about 2dB below the estimation of the FRCS. This discrepancy is good agreement with the simulation results from the cascaded insertion loss of the output buffers and baluns. Table 6.2 presents the performance summary of the proposed test system.



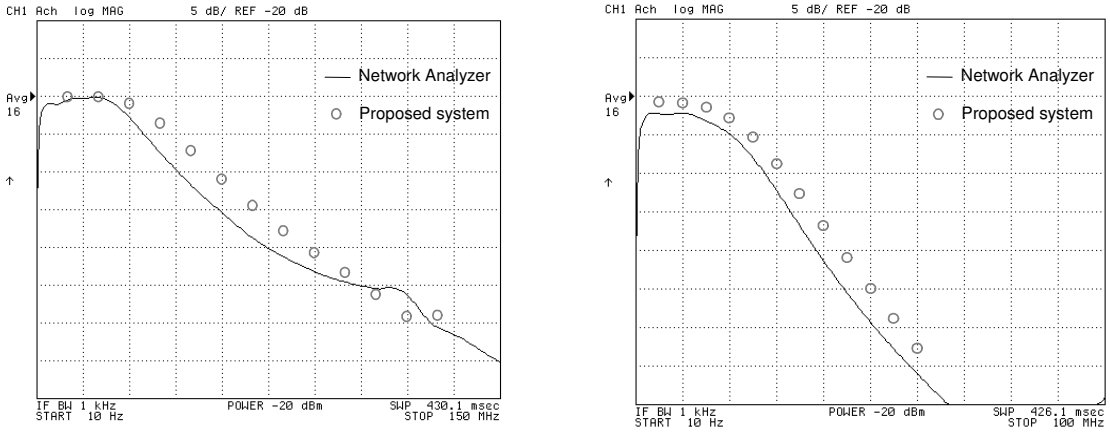
(a) (b)

Figure 6.15 Magnitude Response Test of the 11MHz BPF: (a) Results for the First Biquad (2^{nd} Order Filter), (b) Results for the 4^{th} Order Filter



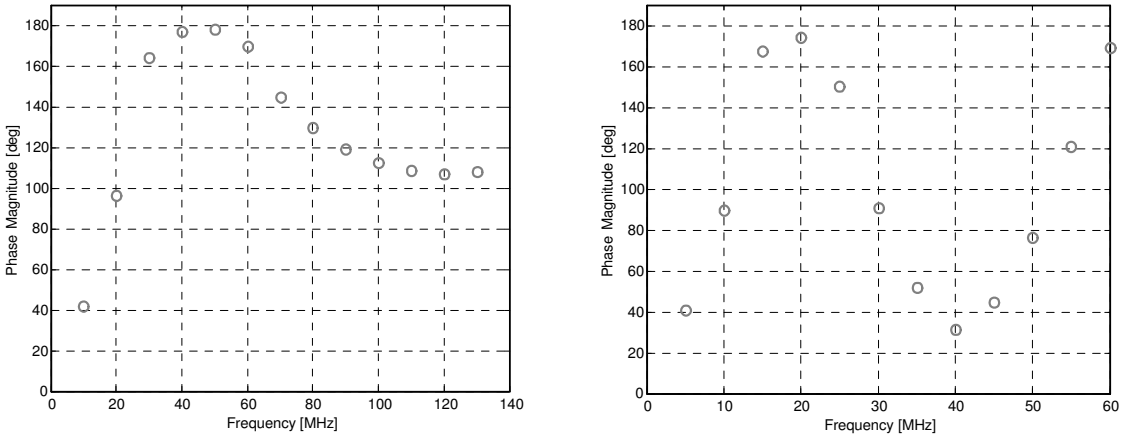
(a) (b)

Figure 6.16 Phase Response Test of the 11MHz BPF: (a) Results for the First Biquad (2^{nd} Order Filter), (b) Results for the 4^{th} Order Filter.



(a) (b)

Figure 6.17 Magnitude Response Test of the 20MHz LPF: (a) Results for the First Biquad (2^{nd} Order Filter), (b) Results for the 4^{th} Order Filter



(a) (b)

Figure 6.18 Phase Response Test of the 20 MHz LPF: (a) Results for the First Biquad (2^{nd} Order Filter), (b) Results for the 4^{th} Order Filter

Table 6.2 Performance Summary

Technology	TSMC 0.35µm CMOS
Dynamic range for measurement of magnitude response	30dB
Resolution for phase measurements	1 deg
Resolution for magnitude measurements	1dB
Frequency Range	1-130MHz
Digital Output Resolution	7 bits
Supply	3.3 V
Power Consumption (at 130MHz)	20mW
Area	0.3 mm^2

Its worth mentioning that even though some target CUT may have specifications in a dynamic range greater than 30dB, the significant amount of information provided by the

system (phase and magnitude responses at different nodes and frequencies) will suffice in most cases to establish correlations to faulty behavior and guarantee a high fault coverage through an appropriate test optimization methodology.

In order to place the achieved results into perspective, Table 6.3 presents a summary of the on-chip testing techniques that have been so far (up to the author's knowledge) demonstrated experimentally with CMOS integrated prototypes. It is important to emphasize that Table 6.3 is presented only with the purpose of providing an overview of the current state-of-the-art; the built-in test systems discussed have diverse characteristics and cannot be compared directly.

The mixed-signal test core presented in [97] is versatile, mostly digital and has the advantage of capturing signals in the GHz range through sub-sampling. Nevertheless, due to the use of oversampling techniques for its signal generator, frequency response measurements with this system are limited to only a fraction of the employed clock frequency (20MHz). It is worth mentioning that the required analog filter for the signal generator is not included in the reported area and that supplemental FFT processing is required to perform the frequency response characterization. Oscillation based test (OBT) is a well documented strategy in the literature [94]. The CUT is re-configured in an oscillation mode and its performance is estimated from the characteristics of the obtained signal; [98] presents a technique to evaluate the characteristics of the output waveform from the CUT on-chip. The on-chip spectrum analyzer presented in [99] has

the advantages of having a digital control and the capability of performing harmonic distortion measurements in addition to frequency response characterizations. The use of switched capacitor techniques improve the robustness of the system but limit its potential application to the range of few MHz. The main drawbacks of the proposed system as a test core are that it has an application space limited to continuous-time circuits, and a limited portability since some of the main analog building such as the multiplier and the VCO cannot be transferred directly from one technology to another.

Table 6.3 Current State-of-the-art in Integrated Solutions for Analog Test

Reference	System	Functions	Technology	Area
[97]	Integrated Mixed-Signal Test Core	Arbitrary waveform generation, frequency response, DC transfer characteristic and THD measurements at a clock speed of 20MHz. Capture of analog signals through sub-sampling at an effective sampling rate of 4GHz.	0.35µm CMOS	0.67 mm^2
[98]	On-Chip Evaluation of Oscillation-Based Test	Extraction of the amplitude, frequency and DC level from the output of a CUT in oscillation mode. Demonstrated on an integrated CUT for an oscillation frequency < 1KHz .	0.6µm CMOS	Not given
[99]	Switched Capacitor Spectrum Analyzer	Measurement of frequency response and harmonic distortion. Demonstrated up to 10KHz on an off-chip CUT.	0.5µm CMOS	0.5 mm^2
This Work	Frequency Response Characterization System	Measurement of magnitude and phase responses over frequency through a digital interface. Demonstrated up to 130MHz on integrated CUTs	0.35µm CMOS	0.3 mm^2

6.6 Conclusions

A compact integrated system for analog testing has been developed and evaluated experimentally. The magnitude and phase responses over frequency of an analog circuit or sub-system can be evaluated without the use of analog instrumentation. The simplicity and low-bandwidth of its digital interface make the proposed test core suitable for wafer-level test and compatible with the IEEE 1149.4 test standard. A very compact ADC has been proposed, it generates the digital equivalent of its DC input signal. The output is taken serially and the number of bits is programmable from 1-bit up to 7-bits depending on the dynamic range and the conversion rate required. The proposed system is an effective and area-efficient solution for low-cost testing of analog circuits. In order to further reduce the testing cost, higher speed ADC should be used. Moreover, higher resolution ADC is required to span high gain systems, where it needs to detect the relative difference between the small-amplitude signal input and the large-amplitude signal output.

CHAPTER VII

CONCLUSIONS

Low-power solutions have been examined throughout this dissertation. A system design procedure has been developed for IEEE 802.15.4/ZIGBEE standard as a LR-WPAN example for low power transceivers. The published standard is analyzed carefully to extract the main features tailored to relax the design of individual building blocks. System non-idealities have been addressed with robust system and circuit procedures to provide a reliable transceiver. New circuit techniques are shown for different building blocks in TSMC 0.18µm CMOS process. The proposed transceiver exhibits comparable or better performance with lower power consumption than commercial transceivers.

Another example of low power systems, RFID systems, has been introduced with complete analytical system design and circuit analysis. A 13.56MHz passive RFID tag is implemented in TSMC 0.35µm CMOS process as a design example. The tag can operate at 1m read range from the reader. It is capable of generating its power needs and recovering a PWM non-encoded signal sent by the reader.

An ultra low power 7-bit compact successive approximation ADC has been designed to be integrated in built-in testing architectures. The overall on-chip magnitude and phase characterization architecture is implemented and characterized in TSMC 0.35µm CMOS process with the proposed ADC. The ADC shows a competitive performance in terms of

power and area compared to similar ADCs reported in the literature. Moreover, it can be easily integrated with IEEE 1149.4 test standard without extra overhead circuitry, since its circuit components are already integrated in the ABM module of IEEE1149.4 standard.

In summary, the contribution highlights of this dissertation are:

- System design procedure for IEEE802.15.4/ZIGBEE compliant transceiver.
- Compact stacked receiver RF front end for the proposed transceiver.
- System design procedure and analysis of passive RFID system.
- Ultra low-power 7-bit compact successive approximation ADC for built-in testing applications

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APPENDIX A

MATLAB CODE TO CALCULATE CHIP ERROR RATE (CER) FROM PACKET ERROR RATE (PER)

```
function probcalc

% P1 (prob of error of a chip)
% P2 (prob of error of a symbol (symbol = 4 bit = 32 chip))
% P3 (prob of error of a packet (52 symbol = 26 octat = 208
bit))

for i=1:1:1001
   P2(i)=0;
   P3(i)=0;
end
z=0
for M=1:0.0001:1.1
    z=z+1
    P1=M-1;

    %P2(z)=0;
    %P3(z)=0;
    % Calculate the probability of error (P2)
    N=6;        % Number of error chips that can not be
recovered.
    L=32-N;
    for i=0:1:L
        k=32-i;
        P2(z)=P2(z)+nchoosek(32,k)*P1^k*(1-P1)^i;
    end

    % Calculate the probability of error (P3)
    N=52;        % Number of symbols in a packet.

    P3(z)=1-(1-P2(z))^N;
end

for i=1:1:1001
   P4(i)=0.1;
end

plot([0:0.0001:0.1],P2,'gd',[0:0.0001:0.1],P3,'r*',[0:0.0001:0.1
],P4,'y-')
  grid on
```

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