HIGH PERFORMANCE INTEGRATED CIRCUIT BLOCKS FOR HIGH-IF WIDEBAND RECEIVERS

A Thesis

by

JOSÉ FABIÁN SILVA RIVAS

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2009

Major Subject: Electrical Engineering

HIGH PERFORMANCE INTEGRATED CIRCUIT BLOCKS FOR HIGH-IF WIDEBAND RECEIVERS

A Thesis

by

JOSÉ FABIÁN SILVA RIVAS

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Approved by:

Co-Chairs of Committee:	Jose Silva-Martinez
	Aydin I. Karsilayan
Committee Members:	Deepa Kundur
	Charles S. Lessard
Head of Department,	Costas N. Georghiades

May 2009

Major Subject: Electrical Engineering

ABSTRACT

High Performance Integrated Circuit Blocks for High-IF Wideband Receivers.

May 2009

José Fabián Silva Rivas, B. S., Texas A&M University

Co-Chairs of Advisory Committee: Dr. Aydin Karsilayan
Dr. Jose Silva-Martinez

Due to the demand for high-performance radio frequency (RF) integrated circuit design in the past years, a system-on-chip (SoC) that enables integration of analog and digital parts on the same die has become the trend of the microelectronics industry. As a result, a major requirement of the next generation of wireless devices is to support multiple standards in the same chip-set. This would enable a single device to support multiple peripheral applications and services.

Based on the aforementioned, the traditional superheterodyne front-end architecture is not suitable for such applications as it would require a complete receiver for each standard to be supported. A more attractive alternative is the high-intermediate frequency (IF) radio architecture. In this case the signal is digitalized at an intermediate frequency such as 200MHz. As a consequence, the baseband operations, such as down-conversion and channel filtering, become more power and area efficient in the digital domain. Such architecture releases the specifications for most of the

front-end building blocks, but the linearity and dynamic range of the ADC become the bottlenecks in this system. The requirements of large bandwidth, high frequency and enough resolution make such ADC very difficult to realize. Many ADC architectures were analyzed and Continuous-Time Bandpass Sigma-Delta (CT-BP-ΣΔ) architecture was found to be the most suitable solution in the high-IF receiver architecture since they combine oversampling and noise shaping to get fairly high resolution in a limited bandwidth.

A major issue in continuous-time networks is the lack of accuracy due to power-voltage-temperature (PVT) tolerances that lead to over 20% pole variations compared to their discrete-time counterparts. An optimally tuned BP ΣΔ ADC requires correcting for center frequency deviations, excess loop delay, and DAC coefficients. Due to these undesirable effects, a calibration algorithm is necessary to compensate for these variations in order to achieve high SNR requirements as technology shrinks.

In this work, a novel linearization technique for a Wideband Low-Noise Amplifier (LNA) targeted for a frequency range of 3-7GHz is presented. Post-layout simulations show NF of 6.3dB, peak S21 of 6.1dB, and peak IIP3 of 21.3dBm, respectively. The power consumption of the LNA is 5.8mA from 2V.

Secondly, the design of a CMOS 6^{th} order CT BP-ΣΔ modulator running at 800 MHz for High-IF conversion of 10MHz bandwidth signals at 200 MHz is presented. A novel transconductance amplifier has been developed to achieve high linearity and high dynamic range at high frequencies. A 2-bit quantizer with offset cancellation is also

presented. The sixth-order modulator is implemented using 0.18 um TSMC standard analog CMOS technology. Post-layout simulations in cadence demonstrate that the modulator achieves a SNDR of 78 dB (~13 bit) performance over a 14MHz bandwidth. The modulator's static power consumption is 107mW from a supply power of ± 0.9V.

Finally, a calibration technique for the optimization of the Noise Transfer Function CT BP $\Sigma\Delta$ modulators is presented. The proposed technique employs two test tones applied at the input of the quantizer to evaluate the noise transfer function of the ADC, using the capabilities of the Digital Signal Processing (DSP) platform usually available in mixed-mode systems. Once the ADC output bit stream is captured, necessary information to generate the control signals to tune the ADC parameters for best Signal-to-Quantization Noise Ratio (SQNR) performance is extracted via Least-Mean Squared (LMS) software-based algorithm. Since the two tones are located outside the band of interest, the proposed global calibration approach can be used online with no significant effect on the in-band content.

To my Parents: Mayo and Jose

ACKNOWLEDGEMENTS

I would like to express my most sincere thanks to my advisors, Dr. Aydin Karsilayan and Dr. Jose Silva-Martinez, who have been an inspiration and support throughout my graduate studies. When I finished my B.S. I approached them to start my M.S. research. They accepted me as their student in spite of my limited knowledge in the field of analog and mixed signals. The endless doubts from my side never seemed to bother them and they patiently answered all my questions. The long discussions with them have helped me to understand different aspects of analog design and I am greatly indebted to them for their guidance during my graduate studies.

I would like to thank my committee members, Dr. Deepa Kundur, Dr. Peng Li, and Dr Charles Lessard, for agreeing to serve on my committee and reading my thesis. Dr. Kundur took me as her undergraduate research assistant to work on digital watermarking processes. Always with a smile, she explained various aspects of behavioral models in Matlab which helped me speed up my research. Dr. Peng Li was my professor in the digital VLSI field and a great source of knowledge and advice in digital design as well as other career choices. Finally, Dr. Lessard sponsored and coached my undergraduate final project in the development of a wireless ECG monitor for the heart. His numerous explanations and support were essential in the completion of the project. Our secretaries, Ella Gallagher, Tammy Carda, and Jeanie Marshall, have always been a tremendous help in all aspects of administrative issues.

I would like to thank my colleagues in the AMSC group for the great discussions and help throughout my stay. Special mention goes to Cho Yin Lu who helped with the design ADC project and to Younghoon Song who helped in the design and layout of the wideband LNA project.

I want to express my deep gratitude to my friends, officemates, and project partners, Venkat Gadde, Marvin Onabajo, John Mincey, Hyung-Joon Jeon, Alfredo Perez, Mohamed El-Nozahi, Manisha Gambir and Raghavendra Kulkarni. I will never forget their constant support, sincere friendship and company during the long hours of work at school.

Looking back in my career, I realize that I am deeply indebted to my teachers (from elementary school to graduate school) who have helped me grow in both technical and personal aspects.

I am always grateful for the love and support from my family. I would like to thank my parents and my brothers for their constant love, encouragement and their belief in me, which has been a great source of inspiration throughout my graduate studies. One person who has always been a constant support and made a great impact in my life is my mother - Mayo. I would like to thank my Kuina, who has been with me all these years with her unconditional love and a smiling face all the time. She is the shining light in my life and a great motivating factor for all my endeavors.

TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

Page

Page

LIST OF TABLES

Page

1. INTRODUCTION

1.1 Motivation

The wireless communication industry has experienced tremendous growth in the last decade throughout the world with an increasing demand due to the addition of new services which provide more functionality for the end users. One of the main reasons for this growth has been the major progress in the field of radio frequency (RF) integrated circuit design where the design trend is slowly advancing towards single chip solutions with very few external components. The major development in system-on-chip (SoC) solutions has led to integration of analog RF, analog baseband and digital signal processors on the same chip. This has resulted in sleek and low power handset devices with multi-purpose functionalities like internet access, video streaming, and global positioning systems (gps).

The number of wireless transmission standards has also increased along with the market growth, with each standard catering to specific market segments. The most common wireless communication applications along with some of their standards are shown in Fig. 1. The personal communication (cell phones) segment includes standards such as GSM (global system for mobile communications), GPRS (general packet radio service), EDGE (enhanced data rate for GSM evolution), CDMA (code division multiple

---

This thesis follows the style of *IEEE Transactions on Circuits and Systems*.

access), AMPS (advanced mobile phone systems), UMTS (universal mobile telecommunication system), PCS (personal communication service), TDMA (time division multiple access), DECT (digital European cordless telephone), IS-95 (digital version of AMPS) etc.

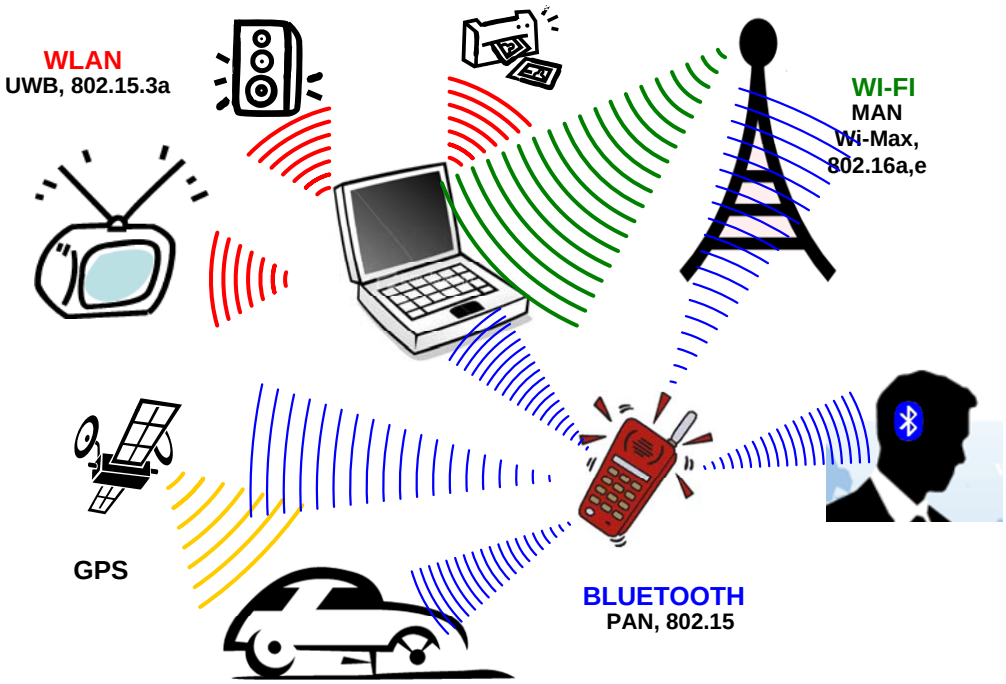


Figure 1 Wireless communication applications and standards

The wireless local area network (WLAN) for laptops, desktops and PDA's include standards like IEEE 802.15, also known as Bluetooth, for the personal area network (PAN); IEEE 802.11 a/b/g and Wi-Fi for wireless home area networking; IEEE 802.16 a/e and Wi-Max for wide-area high speed wireless zones and IEEE 802.20 for the wide area network (WAN). The satellite communication market segment comprising of navigation

systems for locating position of objects (such as commercial systems used in cars) use the GPS standard. Another wireless standard that is gaining popularity recently is IEEE 802.15.3a or UWB (Ultra wide band) for short range high data rate applications in the local area network segment. The number of wireless standards is increasing with committees being formed in all regions of the world to define these standards.

Wireless communication service providers all over the world invest a significant amount of infrastructure to support all these wireless standards in base stations for their respective coverage areas. The end user devices (cell phones, wireless network cards etc) cannot support transmission and reception of signals for only one standard anymore. A major requirement of the next generation of wireless devices and base stations is a single chip set with minimum external components that can support multiple standards. This would enable a single wireless device which makes use of functionality that is supported by multiple service providers. The support for multiple standards would increase the number of features supported by the mobile devices with a faster response time. There are many technical challenges, both at hardware and software level that needs to be overcome in order to realize such a chip set.

1.2 Receiver architectures

The main objective of a receiver for wireless communication applications is to recover the baseband signals that are modulated on a carrier wave at radio

frequencies. The up-converted baseband signals are transmitted over the air (channel) using power amplifiers and antennas, where the signal power at the transmitter output is very high, usually in the range of a few watts. The carrier signals are corrupted by noise and adjacent band interferers (that coexist in the electromagnetic spectrum) as they propagate through the channel so the signal power at the receiver input (after the antenna) is very low, usually in the nano-watt range. Two main considerations for signals as they pass through the receiver are noise and distortion. The lower bound of the signal is determined by the noise floor and the upper bound is dictated by the distortion components [1]. The lowest signal that can be detected at the input of the receiver is defined as the sensitivity of the receiver and is given by

$$\text{Sensitivity (dBm)} = -174 \text{ dBm/Hz} + \text{NF (dB)} + 10\log(\text{BW}) + \text{SNR}_{min}(\text{dB}) \quad (1.1)$$

where NF is the noise figure of the receiver, BW is the bandwidth of the signal and SNR_{min} is the minimum signal to noise ratio required at the output of the receiver for a given bit error rate (BER).

The nonlinear behavior of a receiver gives rise to distortion components and metrics such as IIP3 (third order input intercept point), IM3 (third order intermodulation distortion) and cross modulation, which are used to define the linearity properties of a receiver. Due to device and component nonlinearities, the signals from adjacent channel mix with the signal in the required bandwidth, which causes in-band distortion at the output. Wireless standards have blocking specifications

to determine how strong an adjacent band carrier can exist without corrupting the in-band signal. At the antenna, the power of the desired signal may be at the level of -112 dBm (0.56 μV_{rms} in a 50 Ω impedance) while the power of the interfering signals in adjacent bands may be 30-60 dB higher. Following the detection of signals at the antenna, the receiver must amplify the signals, suppress the interferers, translate the RF signals to baseband and extract the desired information.

Along with stringent specifications on noise and linearity, all portable wireless devices have an additional requirement of low power dissipation in order to increase the battery life, which adds extra complexity to the receiver. The design of a high performance, low power integrated RF receiver in mainstream silicon technologies (CMOS, BiCMOS) is a very challenging task involving numerous tradeoffs during the design process, especially between noise, linearity and power consumption. This section presents an overview of different types of receiver architectures that are suitable for integrated circuit implementation.

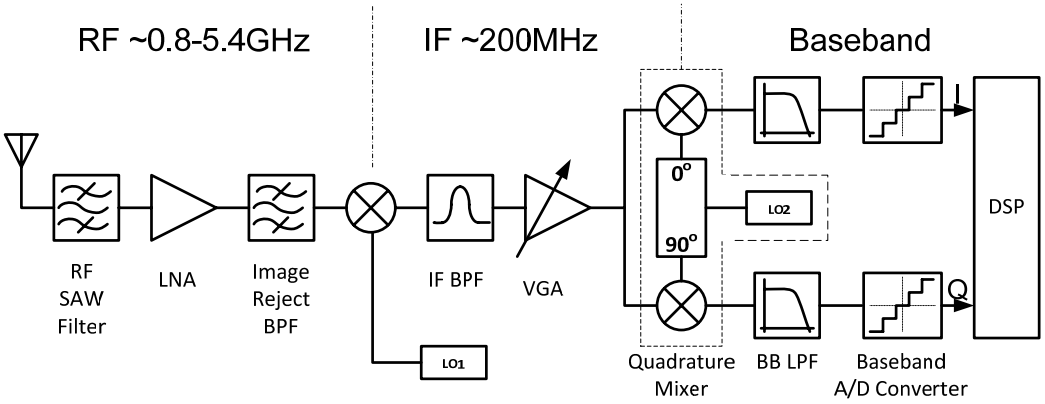


Figure 2 The superheterodyne receiver architecture

The superheterodyne receiver architecture, as shown in Fig. 2, operates as follows. First, the RF band signal is selected by a very sharp surface acoustic wave (SAW) filter and amplified by a very linear low noise amplifier (LNA). In the following stage, the signal goes through an image reject bandpass filter (BPF) before the down conversion to an intermediate frequency by the first local oscillator (LO1). The IF signal is further filtered by an intermediate frequency (IF) BPF and amplified by the variable gain amplifier (VGA) before being frequency translated to baseband into parallel in-phase (I) and quadrature (Q) signals by a quadrature mixer with the second local oscillator (LO2). This architecture reduces the design requirements of receiver implementation as amplification and filtering of signals is easier at low frequencies rather than at high frequencies. The typical approach for implementing a multi-standard receiver using superheterodyne architecture is to replicate paths for each standard and multiplex it in time using analog switches. The main problem is that most of the blocks are analog in nature and have to be redesigned for each standard and can not be reused. This approach becomes impractical as the requirement for number of standards increases.

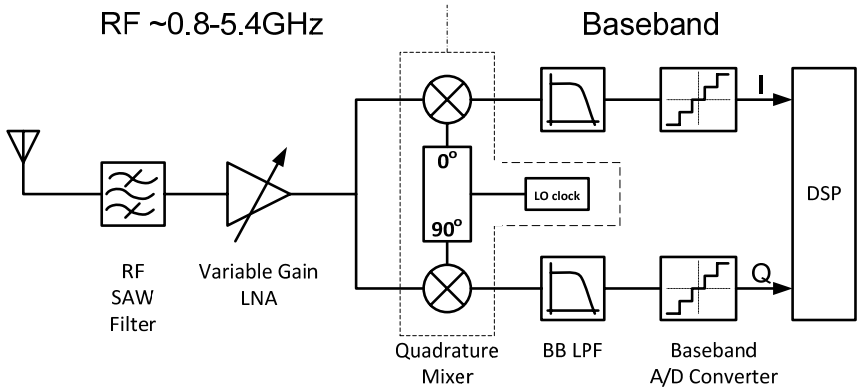


Figure 3 The direct conversion receiver architecture

Fig. 3 depicts the direct-conversion architecture. Similar to the previous topology, the RF signal is selected by a SAW filter and amplified by an LNA before being down converted directly to baseband as I and Q signals. The analog baseband filter performs the channel selection before Analog-to-Digital (A/D) conversion. This architecture eliminates all intermediate frequency components and their associated design challenges, especially the image reject problem.

Direct conversion architecture consumes less power than the superheterodyne receiver does since it eliminates the need for one mixer and one BPF. However, the direct conversion receiver architecture has several problems that affect the circuit performance such as DC offset, local oscillator leakage and excessive flicker noise. The power spectral density of the flicker noise of transistors is inversely proportional to frequency and it severely degrades the performance of baseband circuits. Direct conversion architectures are also not well suited for implementing multiple standards, as each block has to be replicated for every standard.

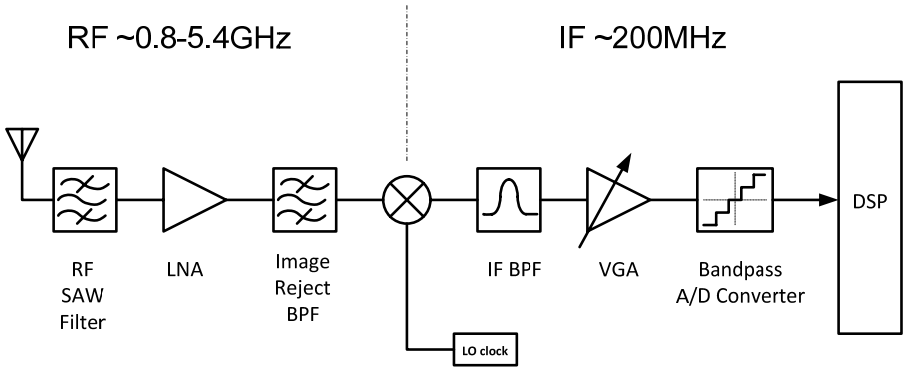


Figure 4 High-IF receiver architecture

The high-IF receiver architecture is the terminology used in literature to describe the idea of IF digitization. It is also sometimes referred to as a digital radio receiver. The block diagram of the high-IF receiver is shown in Fig. 4. The RF BPF selects the required channels from the signal appearing at the antenna. After amplification by the LNA, the signal is filtered by the image reject BPF to attenuate the components at image frequency. This operation is followed by down conversion to IF by the down conversion mixer. The IF BPF further filters the signals and the VGA adjusts the signal strength to be processed by an IF bandpass ADC, which directly gives the digital output to DSP. There is no particular standard for the location of IF signals and the choice of the intermediate frequency is based on the requirements of the IF circuits. The high-IF bandpass sampling overcomes flicker noise and DC offset problems which are usually present in baseband ADCs. Though IF digitization takes advantage of the capabilities of Digital Signal Processing (DSP) programs, it needs additional analog components with channel selection done by an analog filter [2].

1.3 Analog-to-digital converter architectures

Real world signals are inherently analog. However, digital signals can be processed in a more robust and cost-effective way. Therefore high performance data converters become critical with the extremely fast paced improvements of DSP.

Data converters have traditionally been related to high-resolution and low-frequency applications due to the constant use of the superheterodyne and the direct conversion architecture. It's always a tradeoff between speed and resolution. As Fig. 5 shows, flash Analog-to-Digital Converters (ADCs) are the fastest topology and suitable for low resolution applications. The folding, sub-ranging and pipeline ADC architectures are in the very high speed and medium to low resolution category, while the successive approximation and sigma-delta ADC architectures are in the high/medium speed with high resolution category. The incremental and integrating dual ramp ADC architectures fall in the slow speed and very high resolution category. [2]

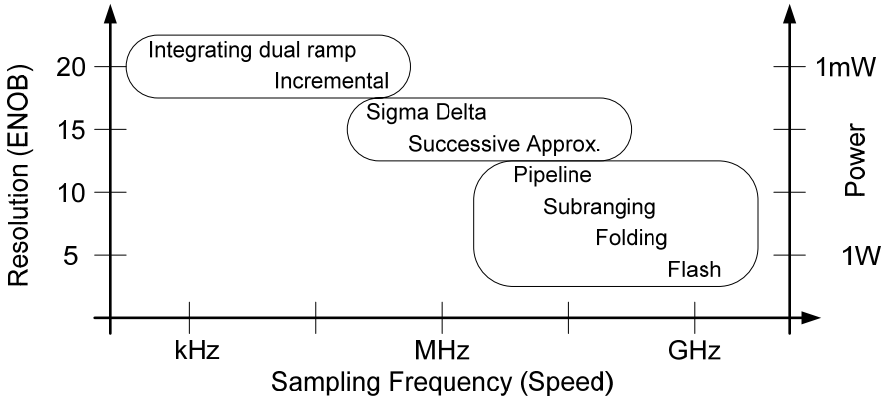


Figure 5 Classification of different ADC architectures as a function of resolution, speed and power

The power consumption for all ADCs increases at higher sampling frequencies, and is usually in the Watt range for GHz sampling frequencies. The ADC for the high-IF receiver application would require sampling frequency in the hundredths of MHz. There are two broad classifications of ADCs based on the relation of their sampling frequency to the bandwidth of the input analog signal, namely Nyquist rate and oversampled ADCs. The Sigma-Delta ($\Sigma\Delta$) ADC is the only architecture in the oversampled category, while all other architectures belong to the Nyquist rate category.

1.4 Overview of $\Sigma\Delta$ ADCs

There are two basic concepts involved in the operation of Sigma-delta ($\Sigma\Delta$) ADC: oversampling and noise shaping. Oversampling spreads the quantization noise over a frequency span larger than the signal bandwidth, therefore reduces the in-band quantization noise. In addition, the $\Sigma\Delta$ ADCs "shape" the quantization noise such that the in-band noise is decreased while the out-of-band noise is increased. The advantages of $\Sigma\Delta$ ADCs are outlined as follows. The cost of implementation is low since most circuits are digital, so integration with other circuitry becomes feasible. $\Sigma\Delta$ ADCs minimize the requirements for analog anti-aliasing filters due to the high oversampling ratio and inherited filtering. They achieve high resolution due to the noise shaping characteristics of the modulator noise transfer function. The quantization noise level is independent of the input analog signal level, thus shaping of the noise can be obtained

without affecting the Signal Transfer Function. The above advantages make ΣΔ ADCs very attractive for digital IF receivers or other wireless applications.

1.5 Research contributions and organization

The thesis is organized as follows: Section I is an introduction to the research, including a short summary of three receiver architectures and the most important advantages of ΣΔ modulators.

Section 2 focuses on the design of Common-Gate LNA for UWB applications. Such design focused on the description and development of a novel linearization technique that boost the linearity of the common-gate LNA by around 10dB by means of modulating the output conductance of the cascode transistor. Post-layout simulations will be presented.

Section 3 introduces the fundamental knowledge of the ΣΔ modulators. The fundamentals of the discrete-time lowpass ΣΔ modulator, discrete-time bandpass ΣΔ modulator and the continuous-time bandpass ΣΔ will be covered in the section. A method to transform transfer function of the loop filter in the discrete-time domain to one in the continuous-time domain will be described. Then some implementation considerations about bandpass ΣΔ modulators are listed. Furthermore, a proposed implementation for a 6^{th} order bandpass continuous-time ΣΔ modulator reaching 14MHz of bandwidth and 78dB of IM3 with signals at 200MHz is presented.

Section 4 focuses on the design of a linearized OTA that can achieve 82dB of IM3 at the cost of 45uW extra power consumption compared to its non-linearized counterpart. The impact of the non-linear output conductance of the OTA on the filter's linearity will be analyzed and conclusions will be drawn.

In Section 5, circuit level simulations and post-layout simulation results are presented for the design of a 2-bit quantizer for the CT BP$\Sigma\Delta$ ADC. The performance of the complete 6^{th} order CT BP$\Sigma\Delta$ modulator is summarized.

In Section 6, an online calibration technique for Noise Transfer Function (NTF) of Continuous-Time Bandpass Sigma-Delta (CT BP$\Sigma\Delta$) modulators is presented. The proposed technique employs two test tones applied at the input of the quantizer to evaluate the noise transfer function of the ADC using the capabilities of the Digital Signal Processing (DSP) platform usually available in mixed-mode systems.

Finally, in Section 7 conclusions of the research work are drawn.

2. WIDEBAND LOW-NOISE AMPLIFIER LINEARITY COMPENSATION TECHNIQUE

2.1 Introduction

A key component of any wireless receiver including the High-IF architecture is the Low-Noise Amplifier (LNA), which boosts the received signal from the antenna before it can be down-converted to intermediate frequencies.

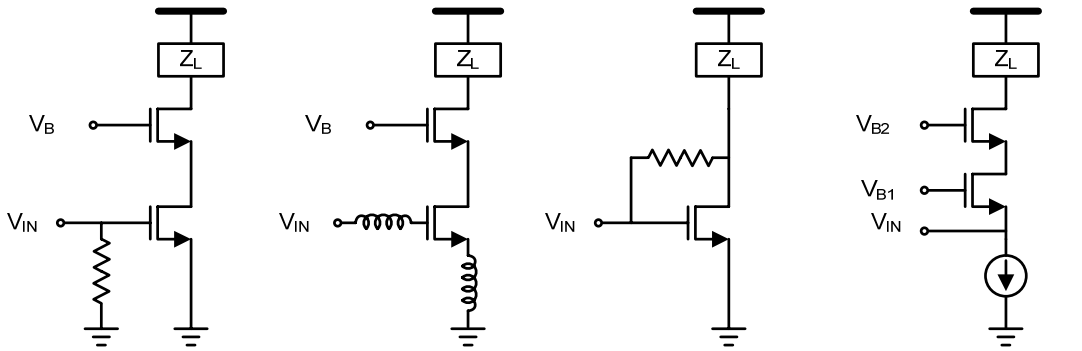
Since multiple standard receivers are targeted in this work, the amount of signal power present at the LNA's input is large compared with the case of single standard devices such as the regular cellular phone. The front-end's linearity must be more than 10 dB better than the one usually required by narrow-band devices. In the worst case, the signal of the service to be used could be very weak while the other channels could be very strong; a non-linear LNA generates intermodulation signals that could drastically corrupt the desired channel. Recently reported IIP3 numbers (-1 dBm in [3], ~4 dBm in [4] and -3.5 dBm in [5]) are certainly modest and due to the lack of linearization techniques for broadband amplifiers. Innovative linearization schemes are required for multi-standard systems. The design at the front-end LNA for multi-standard receivers presents several challenges which demand the development of circuit techniques different from the ones employed in conventional narrow-band receivers.

A wideband LNA must attain input impedance matching in a large band of operation (3 to 7 GHz). This specification is particularly difficult to meet if a commercial (relatively cheap) package is used for the IC because its parasitic effects become significant and may dominate the input impedance, especially at such high frequencies.

2.2 Conventional LNA structures

The broadband nature of the multi-standard transceiver limits the number of suitable front-end architectures. A first approach to the LNA design is a common-source input stage with input resistance as presented in Fig. 6a. This architecture is suitable for wideband applications since resistors are frequency insensitive, but they possess the worst noise performance. In addition, linearity is poor unless extra power is spent to introduce source degeneration. Fig. 6b shows the common-source configuration with inductive degeneration and complex LC impedance matching. This topology uses a number of inductors making the solution very expensive and input matching becomes difficult to control [6-9]. A different approach shown in Fig. 6c uses local resistive feedback and presents decent noise figure and voltage gain [10]. Even more, noise can be partially cancelled through an additional path [11] and can be made programmable [12]. Downsides of this architecture are its limited stability at very high frequencies due to the local feedback and excessive power consumption. A convenient architecture is based on a common-gate configuration [13]; a simplified schematic is depicted in Fig.

6d. Although competitive in most of the specifications, the IIP3 falls short of the over demanding linearity needed for broadband transceivers. Table 1 compares the performance of the four LNA topologies shown in Fig. 6.



(a) Common-Source with input resistor (b) C-S with inductive degeneration (c) C-S with resistive feedback (d) Common-Gate

Figure 6 Standard LNA topologies

Table 1 Summary of properties of standard LNA topologies

	Common-Source with input resistor	Common-Source with inductive degeneration	Common-Source with resistive feedback	Common-Gate
Linearity	Poor. Needs more power and source degeneration	Superior due to inductive degeneration	Improved linearity due to feedback.	Poor
Gain	Good	Very Good	Poor. High power required.	Good
Noise Figure	Worst	Very good	Moderate due to feedback	Moderate
Bandwidth	Very good	Narrow band applications only	Good	Good. Broadband input matching
Stability	Good	Good	Poor at high frequencies	Good
Area	Small	Very Large	Small	Small

2.3 The proposed linearization technique for wideband LNA

Nonlinear effects in RF circuits have been studied during the last decade, as linearity in the LNA is a performance bottleneck in broadband applications [3-4, 14]. The transistor is inherently non-linear, where the most relevant nonlinearity is the 3rd order component. The drain current of the CMOS transistor around the operation point Q (where $i_d=I_D$) can be expressed as a three dimensional Taylor series expansion [15] as described by

$$\begin{aligned} i_d &= I_D + c_{(1,0,0)}v_{gs} + c_{(2,0,0)}v_{gs}^{\ 2} + c_{(3,0,0)}v_{gs}^{\ 3} + c_{(0,1,0)}v_{ds} + c_{(0,2,0)}v_{ds}^{\ 2} \\ &+ c_{(0,3,0)}v_{ds}^{\ 3} + c_{(0,0,1)}v_{sb} + c_{(0,0,2)}v_{sb}^{\ 2} + c_{(0,0,3)}v_{sb}^{\ 3} + c_{(1,1,0)}v_{gs}v_{ds} \\ &+ c_{(1,0,1)}v_{gs}v_{sb} + c_{(0,1,1)}v_{ds}v_{sb} + c_{(2,1,0)}v_{gs}^{\ 2}v_{ds} + c_{(1,2,0)}v_{gs}v_{ds}^{\ 2} + c_{(2,0,1)}v_{gs}^{\ 2}v_{sb} \\ &+ c_{(1,0,2)}v_{gs}v_{sb}^{\ 2} + c_{(0,1,2)}v_{ds}^{\ 2}v_{sb} + c_{(0,2,1)}v_{ds}v_{sb}^{\ 2} + c_{(1,1,1)}v_{gs}v_{ds}v_{sb} \end{aligned} \tag{2.1}$$

where,

$$c(m,n,p) = \frac{1}{m!}\frac{1}{n!}\frac{1}{p!}\frac{\partial^{(m+n+p)}I_{ds}}{\partial^m V_{gs}\partial^n V_{ds}\partial^p V_{sb}}\bigg|_Q \tag{2.2}$$

are the non-linear coefficients, and c(1,0,0), c(0,1,0) and c(0,0,1) are the small signal parameters g_m, g_o and g_{mb}, respectively. Coefficients c(1,0,0), c(2,0,0) and c(3,0,0) describe the first, second and third order derivatives of i_d with respect to v_{gs}. c(0,2,0) and c(0,3,0) correspond to the derivatives of i_d with respect to v_{ds} and c(0,0,2) and

c(0,0,3) represent the derivatives of i_d with v_{sb}. The other non-linear terms are referred to as the cross-modulation terms.

Assuming bulk and source pins are connected together in the MOS device, the most relevant terms in the expansion are due to the non-linear relationship between i_d and v_{gs} and v_{ds}. Retaining the most relevant nonlinear coefficients, the output current becomes as follows.

$$i_d = I_D + c_{(1,0)}v_{gs} + c_{(2,0)}v_{gs}^{\ 2} + c_{(3,0)}v_{gs}^{\ 3} + c_{(0,1)}v_{ds} + c_{(0,2)}v_{ds}^{\ 2} + c_{(0,3)}v_{ds}^{\ 3} + c_{(1,1)}v_{gs}v_{ds} + c_{(2,1)}v_{gs}^{\ 2}v_{ds} + c_{(1,2)}v_{gs}v_{ds}^{\ 2} \tag{2.3}$$

Considering that the DC current I_D and all even order harmonic terms are negligible if a differential structure is utilized, the drain current i_d can be simplified and rewritten as

$$i_d = [g_m]v_{gs} + [g_0]v_{ds} + [coef_1]v_{gs}^{\ 2}v_{ds} + [coef_2]v_{gs}v_{ds}^{\ 2} \tag{2.4}$$

By combining (2.2) and (2.4) and rearranging the terms as functions of v_{gs} and v_{ds}, the expressions for the effective g_m, g_o, and the cross-modulation terms can be obtained around the fundamental frequency range as follows.

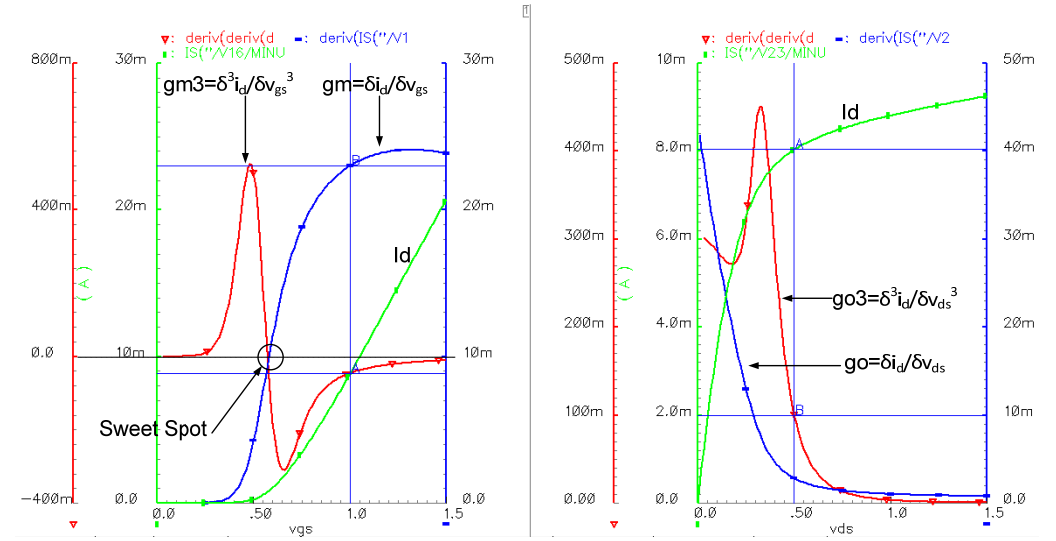
$$g_m = \left(\frac{\partial i_d}{\partial v_{gs}}\right)\Bigg|_Q + \frac{1}{6}\left(\frac{\partial^3 i_d}{\partial v_{gs}^{\ 3}}\right)\Bigg|_Q v_{gs}^{\ 2} \tag{2.5}$$

$$g_o = \left(\frac{\partial i_d}{\partial v_{ds}}\right)\Bigg|_Q + \frac{1}{6}\left(\frac{\partial^3 i_d}{\partial v_{ds}^{\ 3}}\right)\Bigg|_Q v_{ds}^{\ 2} \tag{2.6}$$

$$coef_1 = \frac{1}{2}\left(\frac{\partial^3 i_d}{\partial v_{gs}{}^2 \partial v_{ds}}\right)\Bigg|_Q \tag{2.7}$$

$$coef_2 = \frac{1}{2}\left(\frac{\partial^3 i_d}{\partial v_{gs} \partial v_{ds}{}^2}\right)\Bigg|_Q \tag{2.8}$$

According to (2.4) the third-order non-linearity is a function of both v_{gs} and v_{ds}. For a transistor operating in deep strong inversion, the non-linearity due to v_{gs} is dominant, but the nonlinear output resistance plays an important role when the DC value of V_{DS} is limited. Further characterization of the devices shows that $\partial^3 i_d/\partial v_{gs}{}^3$ is positive when the transistor operates in sub-threshold region and becomes negative mainly due to hot carrier effects when operated in strong inversion. Fig. 7a shows the behavior of the third-order non-linear terms for a transistor of 50um/0.18um implementing a small signal transconductance of 20mA/V.

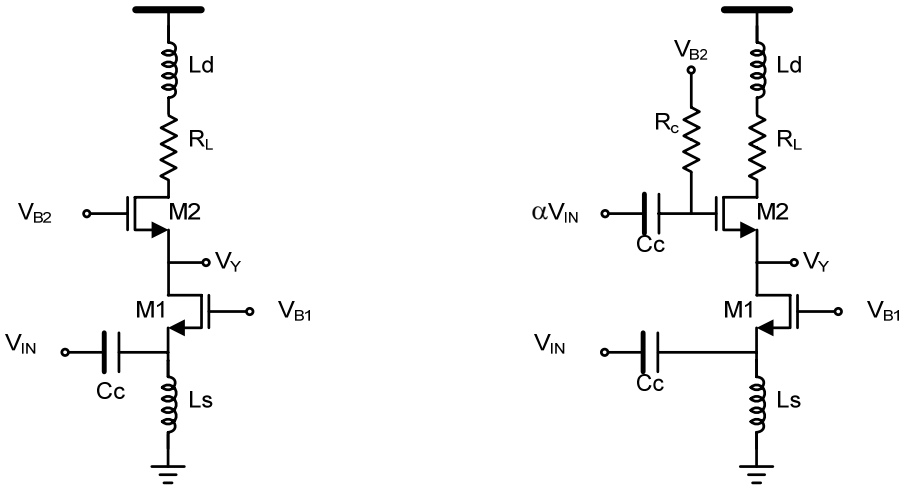


(a) id, gm and gm3 vs. Vgs Variations **(b) id, go and go3 vs. Vds variations**

Figure 7 1st and 3rd order behavior of i_d in NMOS device as a function of v_{gs} and v_{ds}

The $\partial^3 i_d/\partial v_{ds}^3$ curve shown in Fig. 7b follows a different trend when V_{ds} is varied; positive and large for transistors operating for small V_{ds} voltages and for large V_{ds} voltages, $\partial^3 i_d/\partial v_{ds}^3$ decreases due to large electric field. The terms $\partial^3 i_d/\partial v_{gs}^2 \partial v_{ds}$ and $\partial^3 i_d/\partial v_{gs} \partial v_{ds}^2$ have also significant effects when extremely demanding linearity figures are required.

Broadband LNAs previously reported did not emphasize linearity optimization, resulting in limited IIP3 figures because the effects of both v_{gs} and v_{ds} non-linearities usually combine such that the overall distortion increases. In the conventional common-gate LNA shown in Fig. 6d, the voltage gain measured at the output of M1 is 1 when the transconductance of M2 is equal to that of M1; hence v_{ds} variations in M1 are close to zero and g_m nonlinearity dominates. Notice that as pictured in Fig. 7a when V_{DS}< 0.6V, the transistor linearity degrades further and is dominated by $\partial^3 i_d/\partial v_{ds}^3$. Such effect is caused by the third order non-linearity of the output conductance of M1. As the technology trend keeps moving to smaller supply voltages, these effects will become more severe and will have to be taken into account.



(a) Traditional Common-Gate LNA **(b) Proposed Common-Gate with R_{o2} modulation**

Figure 8 Typical common-gate configuration LNA and proposed C-G LNA

Given that transistor M1 is the most critical component which defines input impedance and noise figure, it leaves no room for optimization; on the other hand, the proper selection of M2 parameters in the modified common-gate LNA can lead to huge linearity improvements without increasing power consumption.

Although formal Volterra series analysis is required for the analysis of LNA non-linearities across frequencies, simpler study of the topology shows that linearity optimization can be achieved if the novel topology shown in Fig. 8b is used where parameter $\alpha(\cong 1)$ indicates the level of signal injection at the gate of M2. In the schematic of Fig. 9, the small signal representation of the proposed linearized LNA is shown, where v_y is the voltage at the drain of transistor M1 and k stands for the third order non-linear coefficient of v_y. As stated before, it is assumed that the term $\partial^3 i_{d1}/\partial v_{ds}^3$ or g_{o13} is negligible since transistor M1 has a large v_{ds}. This is not the case for

transistor M2 where v_{ds} is set around 500mV and thus the non-linear term g_{o23} is included. The α factor is assumed to be equal to 1 for direct connection.

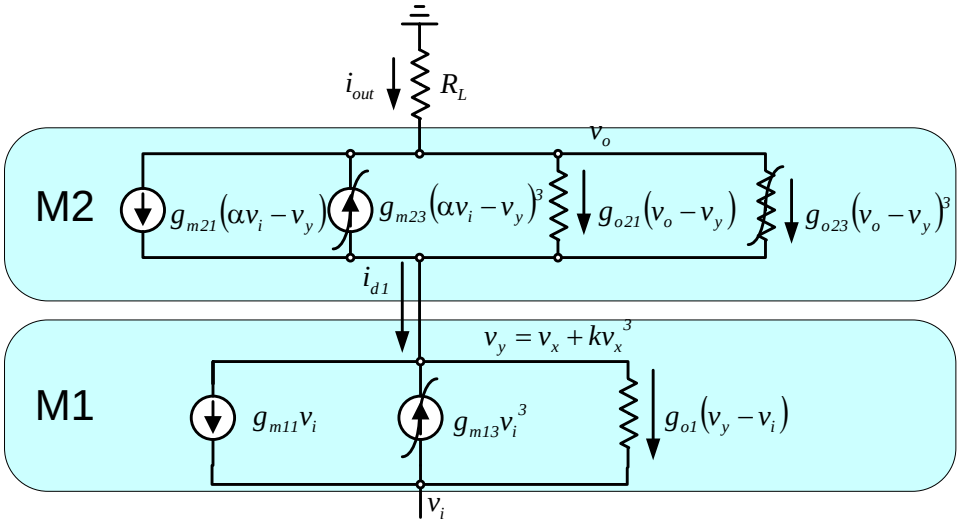


Figure 9 Small signal model of proposed C-G LNA

The linearization technique aims to achieve total cancellation of third order coefficients by creating a non-linear voltage at the drain of transistor M1 with some specific properties. The relationship between the desired non-linear voltage v_y at the drain of M1 and the desired linear current i_{d1} is given by

$$i_{d1} = g_{m11}v_i - g_{o1}(v_i - v_x) - g_{m13}v_i^3 + g_{o1}\left(kv_x^3\right) \tag{2.9}$$

The condition for third order distortion cancellation in M1 can be obtained by forcing the non-desired 3rd order terms equal to zero.

$$-g_{m13}v_i^3 + g_{o1}\left(kv_x^3\right) = 0 \tag{2.10}$$

Equation (2.11) shows the first condition for the linearization of transistor M1.

$$\left(\frac{v_x}{v_i}\right)^3 = \frac{g_{m13}}{g_{o1}k} \tag{2.11}$$

The second condition comes from the necessary bias conditions that transistor M2 must have in order to generate v_y. From Fig. 9, the expression for the output current ($i_{out}=i_{d1}$) as a function of M2 and M1 parameters is given by

$$\begin{aligned} i_{out} &= g_{m21}\left(\alpha v_i - v_x - k{v_x}^3\right) - g_{m23}\left(\alpha v_i - v_x - k{v_x}^3\right)^3 \\ &+ g_{o21}\left(v_o - v_x - k{v_x}^3\right) + g_{o23}\left(v_o - v_x - k{v_x}^3\right)^3 \end{aligned} \tag{2.12}$$

In the same fashion as before, the non-linear terms of the output current are set to zero as shown in (2.13) and the k term is found to be (2.14).

$$g_{m21}\left(k{v_x}^3\right) - g_{m23}\left(v_x\right)^3 + g_{o21}\left(k{v_x}^3\right) + g_{o23}\left(v_x\right)^3 = 0 \tag{2.13}$$

where,

$$k = \frac{g_{o23} - g_{m23}}{g_{m21} + g_{o21}} \tag{2.14}$$

Finally, combining equations (2.11) and (2.14), we can obtain the condition at which the output current i_{out} will be ideally linear as follows

$$\left(\frac{v_x}{v_i}\right)^3 = \left(\frac{g_{m13}}{g_{o1}}\right)\left(\frac{g_{m21}+g_{o21}}{g_{o23}-g_{m23}}\right) \tag{2.15}$$

From the configuration presented in Fig. 8b where the input is feedforwarded to the gate of M2, it can be seen that the gain v_x/v_i is around 2. The terms g_{o1} and g_{m13} are fixed since the transistor M1 operates in strong saturation region and its bias conditions are optimized for matching and noise purposes. From the previous assumptions and equation (2.15), the cancellation of non-linear effects is achieved if

$$8 \approx \left(\frac{g_{m13}}{g_{o1}}\right)\left(\frac{g_{m21}+g_{o21}}{g_{o23}-g_{m23}}\right) \tag{2.16}$$

The only optimization parameters are g_{m21}, g_{o21} and g_{o23}, which proves that adjusting the bias conditions for transistor M2 one could potentially linearize the common-gate LNA. Making $g_{o23} > g_{m23}$ we can potentially satisfy (2.16). In order to reach such state, it is required to reduce v_{ds2}. A graphical interpretation of the proposed linearization technique is depicted in Fig. 10 which shows the value of the IIP3 as the function of the DC voltage bias at the gate of the cascode transistor M2 in Fig. 8b.

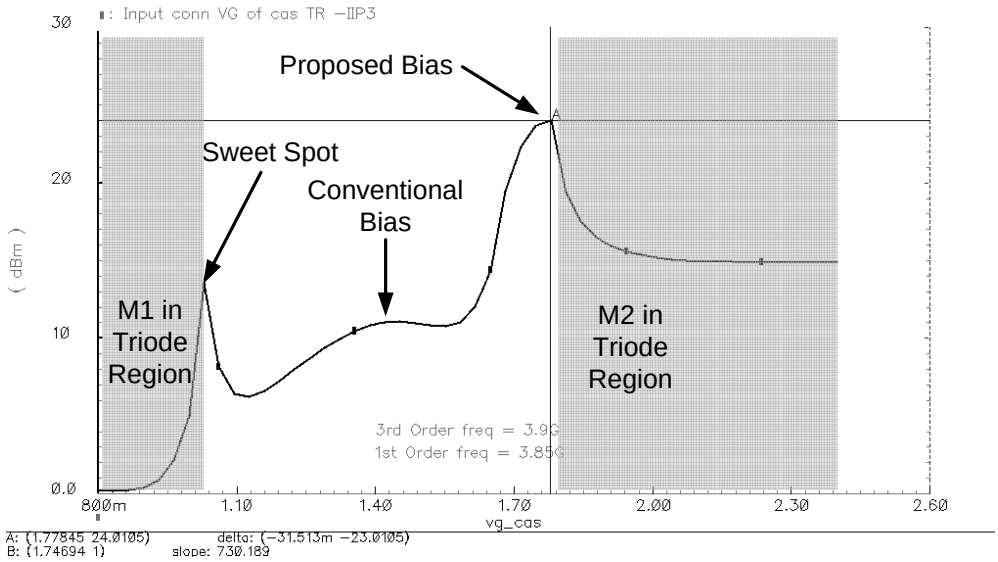


Figure 10 IIP3 of the proposed LNA as a function of the gate DC voltage in M2

As the voltage in the cascode device is swept from low to high, transistor M1 enters triode region while M2 is in saturation. At the transition between triode and saturation region for M1, the sweet spot is reached and a linearity spike occurs in a very narrow region and then it drops rapidly. As the voltage is further increased, transistor M1 enters deep saturation region and the linearity increases slowly. At the same time, transistor M2 starts to have a lower v_{ds} voltage since the voltage at the drain of M2 is fixed. According to Fig. 7a, such effect will increase the 3rd order non-linear behavior of g_{o2}. There is the condition at which equation (2.16) is satisfied and linearity cancellation occurs. In this case, at v_{ds2}=1.78V the linearity of the LNA can reach up to 24dBm.

2.4 LNA input matching and noise figure of proposed C-G LNA

The input impedance (z_{in}) of the Common-Gate architecture shown in Fig. 8b should ideally be defined as $1/g_{m1}$ for all frequencies. However, this is not the case since the gate of transistor M1 needs to be biased and thus inductor Ls is introduced creating a DC ground and an AC open at high frequencies. Now, z_{in} is defined in (2.17) as the parallel combination of the $1/g_{m1}$ with the active resonator created with the lossless inductor Ls and its series associated resistance R_{OL} and the parasitic capacitance C_{gs1}. The resonant frequency was set at 5GHz in order to have good S11 parameters in the 3-7GHz band.

$$Zin = \frac{1}{g_{m1}} \left\| \frac{sL_s + R_{oL}}{s^2 L_s C_{gs1} + sC_{gs1} R_{oL} + 1} \right. \tag{2.17}$$

The Noise Figure (NF) of the proposed architecture will increase compared to the standard common-gate structure due to the feed forward path from the input of the LNA and will now be given by

$$NF = 1 + \frac{\gamma}{\alpha}\left(1 + \frac{4g_{m1}}{g_{m2}}\right) \tag{2.18}$$

where, having R_s of 50 ohms and a g_{m2} of 15mA/V yield a minimum NF of 5.2dB assuming long-channel devices.

It can be shown that ignoring the effects of the parasitic capacitors, the voltage gain of the modified LNA becomes

$$\frac{v_0}{v_i} = \frac{R_L\left(g_{m1}R_{o1}g_{m2}R_{o2} + g_{m1}R_{o1} + g_{m2}R_{o2}(1-\alpha)+1\right)}{\left(g_{m2}R_{o2}R_{o1} + R_{o2} + R_{o1} + R_L\right)} \tag{2.19}$$

Parameters g_{mi} and g_{0i} are the nonlinear transconductance and conductance of Mi, respectively. By analyzing (2.19) it can be shown that the gain of the compensated LNA will not be degraded significantly by the feedforward path.

2.5 LNA post-layout simulation results

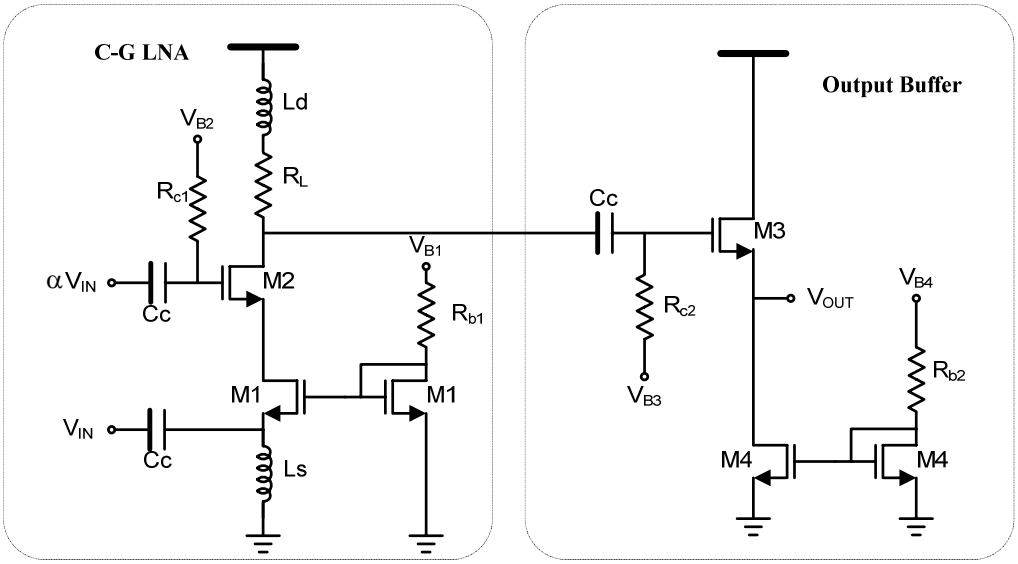


Figure 11 Complete schematic on proposed LNA

The complete architecture of the proposed LNA is shown in Fig. 11, where the devices sizes are shown in table 2. The proposed architecture utilizes an output buffer in order to measure the response of the LNA without corrupting the LNA's output node when probing the circuit. Linearity of the LNA is measured by characterizing $IIP3_{LNA+Buffer}$, $NF_{LNA+Buffer}$ and $S21_{LNA+Buffer}$ on the C-G LNA plus Buffer circuit. By creating a replica of the stand-alone buffer the values for $IIP3_{Buffer}$, NF_{Buffer} and $S21_{Buffer}$ are obtained and the performance measurements for the stand-alone LNA are obtained according to the following equations.

$$S21_{LNA} = \frac{S21_{LNA+buffer}}{S21_{buffer}} \tag{2.20}$$

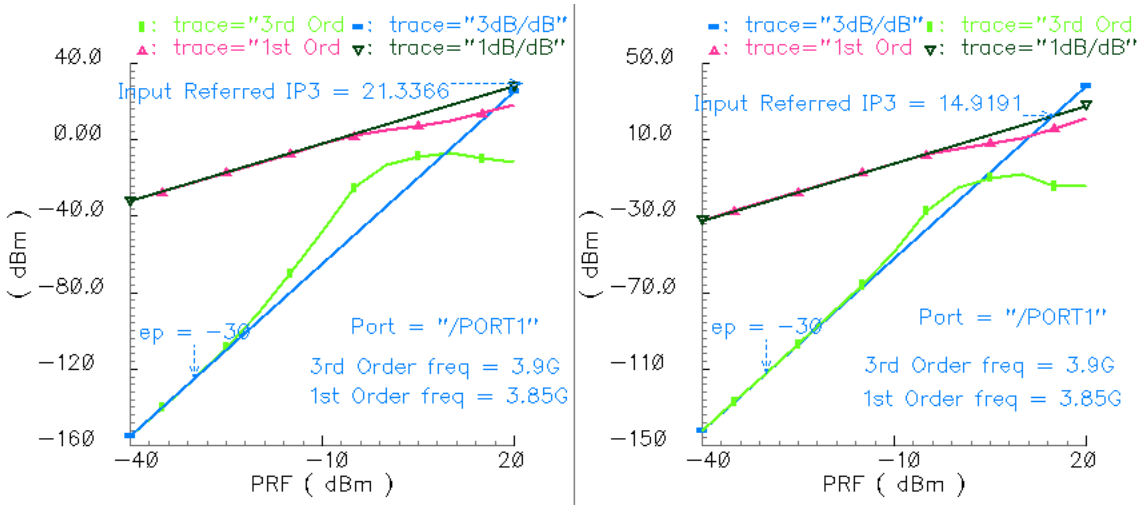
$$NF_{LNA}\big|_{dB} = 10\,log\left(NF_{LNA+Bufferl} - \frac{NF_{buffer} - 1}{S21_{LNA}} \right) \tag{2.21}$$

$$IIP3_{LNA}\big|_{dB} = -10\,log\left(\frac{1}{10^{IIP3_{LNA+Buffer}/10}} - \frac{1}{10^{\left(IIP3_{Buffer} - S21_{LNA}\right)/10}} \right) \tag{2.22}$$

The S11 achieved with this architectures is -10.4dB, with a NF = 7.3dB, S211 = 5.5 and an IIP3 of 18.3dBm across all frequencies. This topology guaranties approximately 6dB of improvement in the IIP3 compared to the standard LNA counterpart as shown in Fig. 12. This plot also shows similar linearity figures for both architectures for input power signals greater than -10dBm. For very large signals the LNAs enter into highly non-linear regimes, and cancellation becomes less efficient.

Table 2 Transistor and device sizes for the proposed LNA linearization

Device	Size	Device	Size
M1	(10) 5u/180n	**Rb1**	140 ohms
M2	(10) 5u/180n	**Rb2**	50 ohms
M3	(8) 5u/180n	**Rc1**	15k ohms
M4	(25) 5u/180n	**Rc2**	15k ohms
Ld	0.78nH	**Vb1**	1.85V
Ls	2.7nH	**Vb2**	1.95V
Cc	1.5pF	**Vb3**	1.35V
Vdd	2V	**Vb4**	2V
RL	150 Ohms		



(a) Linearized LNA **(b) Standard C-G LNA**

Figure 12 IIP3 comparison between proposed and standard LNA

The proposed topology has been extensively simulated for all technology corners; the IIP3 behavior for this LNA shows approximately 5dB degradation across process and temperature variations as illustrated in Fig. 13. This is due to the fixed voltage bias applied at the gate of transistor M2. If a temperature-tracking bias is used, linearity degradation due to temperature variations can be reduced.

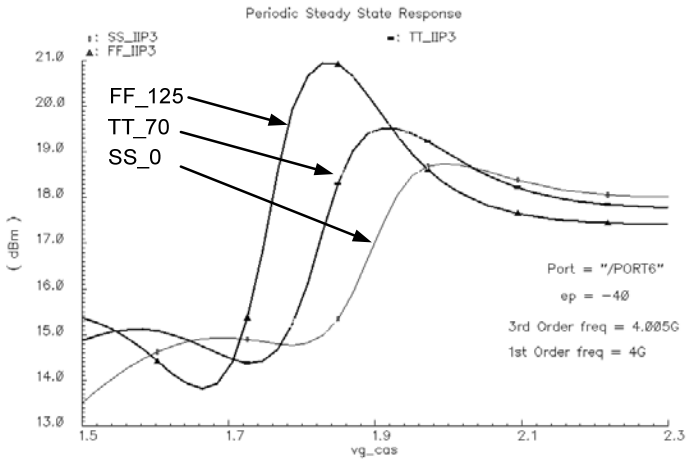
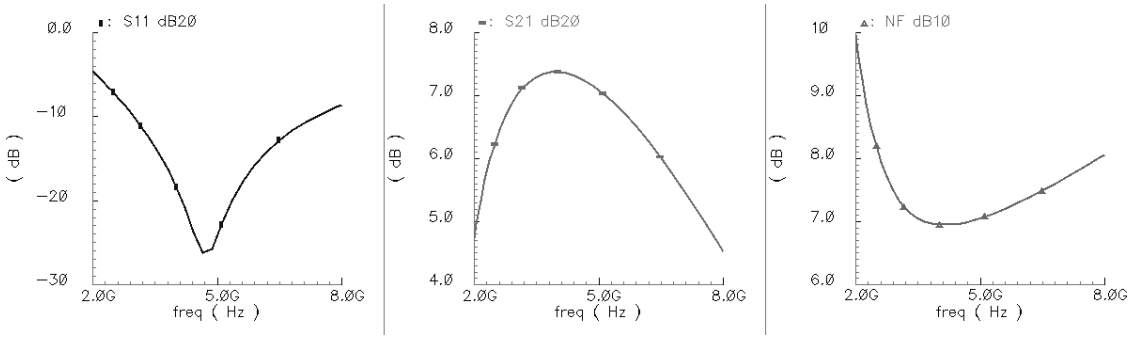


Figure 13 IIP3 behavior versus DC voltage for different corners



(a) S11 **(a) S21** **(a) NF**

Figure 14 S-parameters and noise figure of proposed linearized LNA

Tables 3 and 4 summarize the post layout simulations for the standard C-G LNA as well as the proposed linearized solution. The proposed linearization technique improves the IIP3 of the LNA at least by 6dB across all frequencies, while S11 and S21 parameters are similar to the standard C-G LNA. Noise figure in the proposed architecture is approximately 1dB higher due to the coupling of M2 directly to the input.

Table 3 De-embedded standard CG-LNA results

Frequency	IIP3 (dBm)	S11 (dB)	S21 (dB)	NF (dB)
3GHz	12.9	-10.2	6.1	4.6
4GHz	12.9	-20.4	6.3	4.3
5GHz	14.9	-35.6	6.4	4.5
6GHz	13.8	-19.5	6.0	4.2
7GHz	13.5	-14.0	5.9	4.6

Table 4 De-embedded linearized C-G LNA results

Frequency	IIP3 (dBm)	S11 (dB)	S21 (dB)	NF (dB)
3GHz	18.6	-10.4	6.1	6.3
4GHz	19.5	-18.4	6.6	6.5
5GHz	21.3	-33.6	6.5	6.3
6GHz	20.5	-19.7	6.1	6.4
7GHz	18.1	-14.9	5.5	6.3

The layout of the LNA shown in Fig. 15 is composed of the proposed LNA plus buffer solution, one standard LNA plus buffer, and one stand-alone buffer for de-embedding the performance of the amplifiers. The LNA design was fabricated in 0.18um CMOS technology thanks to TMSC sponsorship. The occupied area by the proposed LNA is 1umX0.6um and it consumes 5.8mA from a 2V power supply.

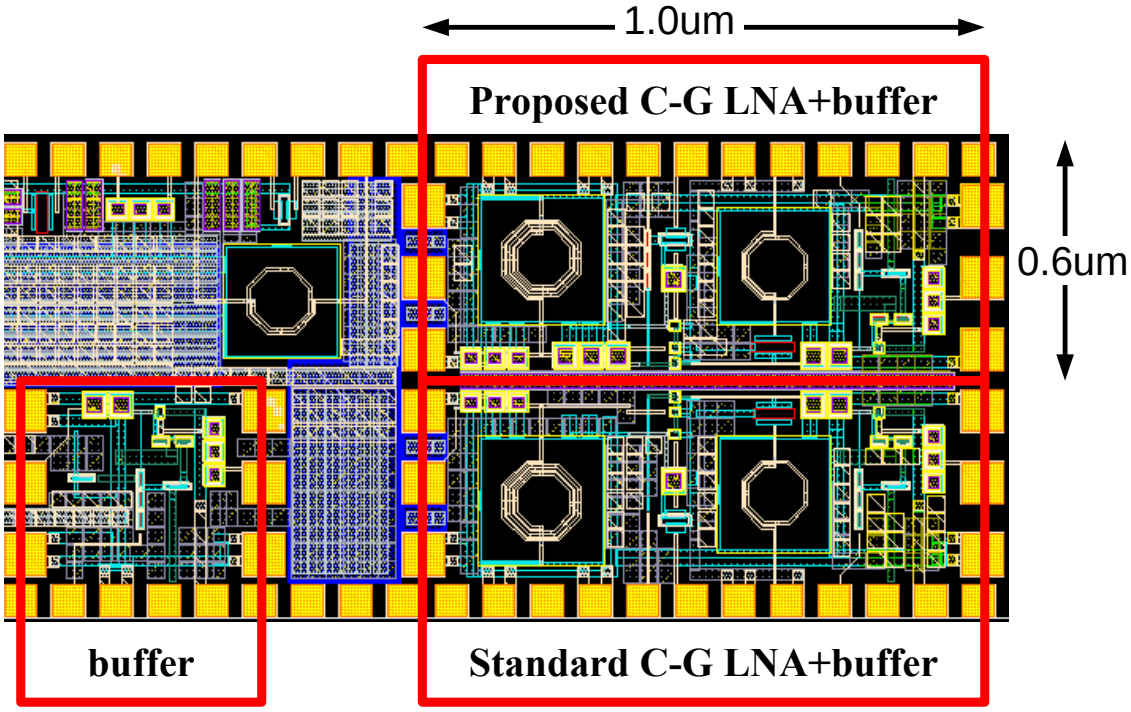


Figure 15 Layout of proposed LNA, standard LNA and stand alone buffer

3. THE CONTINUOUS-TIME ΣΔ MODULATOR

3.1 Introduction

Digital signal processing enables complex modulation and filtering of IF signal in digital domain. Appropriate A/D converters are required to digitize the input signals before processing. In recent years, some publications [16], [20]-[23] investigated the use of bandpass $\Sigma\Delta$ modulator for High-IF receivers. Most reported bandpass $\Sigma\Delta$ modulators were realized with discrete-time circuits such as switched capacitors [17]-[18] or switched-current circuits [19]. However, they have a rather low operating frequency. It's possible to replace discrete-time loop filter by continuous-time counterpart. This modified architecture is called the continuous-time modulator. It contains inherently anti-alias filtering and it is much faster because they relax the requirements of high speed Opamps and the settling time of the circuitry. An implementation of a continuous-time bandpass $\Sigma\Delta$ modulator with discrete components is relatively easy. However, it is always preferable to eliminate the discrete components and have an integrated on-chip system to reduce the size and cost.

In this section, the fundamentals of $\Sigma\Delta$ modulator are given to have a good understanding of its operation. Secondly, the proposed architecture of a 6^{th} order continuous-time bandpass $\Sigma\Delta$ modulator is depicted. Some practical design issues are explained and discussed.

3.2 Nyquist rate and oversampled ADCs

The process of sampling of a continuous time analog signal x(t) at a frequency F_s in an ADC is equivalent to multiplying the signal by an impulse train that repeat every T_s seconds as depicted below in Fig. 16.

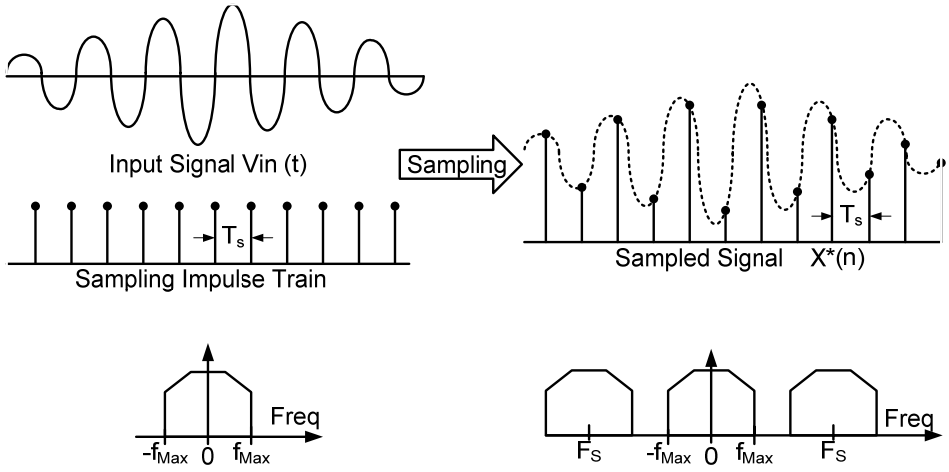


Figure 16 Sampling in time and frequency domain

Mathematically, the sampled discrete time signal is given in time domain by

$$x^*(t) = \sum_{n=-\infty}^{+\infty} x(t)\delta(t - nT_s) \tag{3.1}$$

where n is an integer and δ is the ideal impulse function. In frequency domain, the sampled discrete time signal is given by

$$X^*(f) = X(f) * \sum_{n=-\infty}^{+\infty} \frac{1}{T_s} \delta(f - n * F_s) \tag{3.2}$$

where X(f) is the Fourier transform of the signal x(t). The sampling function modulates x(t) by carrier signals having frequencies at F_s, $2F_s$, $3F_s$ ... etc and in frequency domain, this causes the spectrum of x(t) to be repeated at $n*F_s$ frequencies.

When the analog signal has a limited bandwidth (f_{Max}), then it must be sampled at a rate that is greater than $2*f_{Max}$ in order to avoid aliasing, where signal image components at higher frequencies fold back into the signal bandwidth. The Nyquist sampling theorem states that the sampling frequency should be at least $2*F_{in}$ in order to be able to recover the original signal perfectly from the sampled version. All Nyquist rate ADC architectures have sampling frequency of $2*F_{in}$.

The quantization noise power of Nyquist rate ADC's spreads in frequency from DC to $F_s/2$, as shown in Fig 17a. The signals at the input of bandpass ADCs are located around a center frequency and the bandwidth depends upon number of channels or standards that are required to be converted to digital output. This is especially inconvenient when a narrow-band signal is located at high frequencies with a bandwidth F_{Max} because a Nyquist rate ADC would have a sampling frequency of at least twice the maximum frequency of the signal in order to digitize the entire band from DC to F_{Max}. Since there is no inherent filtering in a Nyquist rate ADC, a lot of power is wasted while trying to reduce the quantization noise in the entire Nyquist bandwidth,

which contains frequency components outside the required signal bandwidth. This disadvantage makes Nyquist rate ADC unattractive for software radio applications.

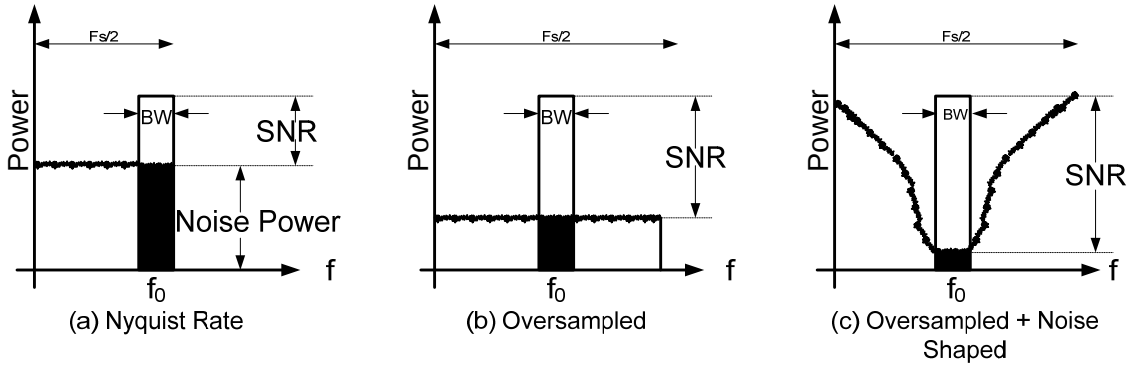


Figure 17 Different ADC architectures

The ADC architectures that have a sampling frequency much greater than the Nyquist sampling criterion belong to the category of oversampled ADC's ($F_s/2 >> f_{Max}$). The quantization noise power spreads in frequency from DC to $F_s/2$ and its root mean square value is the same as that of the Nyquist rate ADCs. The main difference is that the in-band quantization noise power is reduced as compared to Nyquist rate since the same power is spread over a much greater frequency range. The oversampling ratio (OSR) of the ADC is defined as $Fs/(2*F_{Max})$ and a 2x increase in sampling frequency results in 3 dB improvement of the ADC's SNR. An over sampled ADC frequency spectrum is shown in Fig. 17b.

A sigma-delta (ΣΔ) ADC combines oversampling with noise shaping (using negative feedback loop), which greatly reduces the in-band quantization noise power

and results in a high SNR within the signal bandwidth [23]. The negative feedback together with oversampling results in a SNR improvement of 9 dB (1.5 bits) for a 2x increase in the sampling frequency. The frequency spectrum of quantization noise in ΣΔ (oversampled) ADC is shown in Fig. 17c.

3.3 Sigma-delta modulator theory

The basic components of a ΣΔ ADC is shown in Fig. 18.

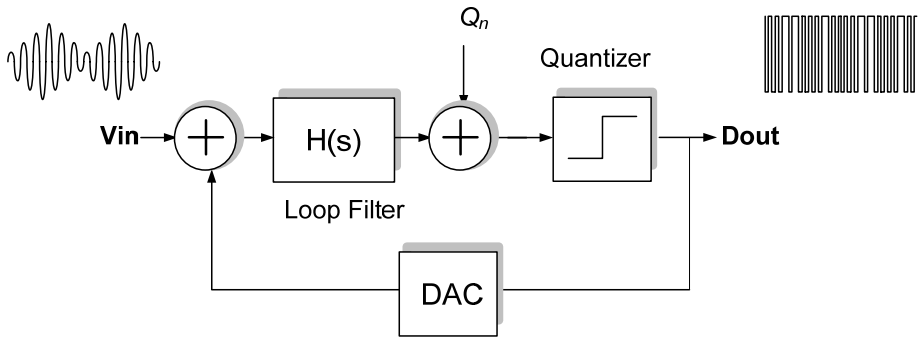


Figure 18 Block diagram of a sigma-delta ADC

It includes a loop filter followed by a comparator, with a feedback digital to analog converter (DAC) completing the negative-feedback loop. While considering a small signal model (a linearized model is used for the non-linear comparator block) and assuming a unity gain transfer function for the DAC and comparator, the output (D_{out}) is given by

$$D_{out} = STF * V_{in} + NTF * Q_n \tag{3.3}$$

where Q_n is quantization noise, STF and NTF are the signal and noise transfer functions. The STF and NTF of the ADC are given by

$$STF = \frac{D_{out}}{V_{in}} = \frac{H(z)}{1 + H(z)} \tag{3.4}$$

$$NTF = \frac{D_{out}}{Q_n} = \frac{1}{1 + H(z)} \tag{3.5}$$

The digital output (D_{out}) then passes through decimation and digital filter blocks, where down sampling is performed to get the final output. If bandpass architecture is utilized as a loop filter, the STF and NTF will take different shapes as shown in Fig. 19.

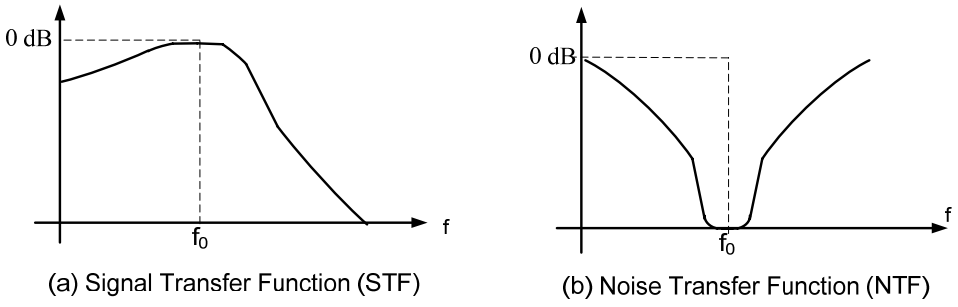


Figure 19 Typical STF and NTF for a bandpass ΣΔ Architecture

From (3.4) it is easy to see that the STF will get close to unity for a large H(z) value, which occurs at the resonant frequency f_0. On the other hand, (3.5) shows that the NTF will go to zero in the frequency of interest (f_o) and the quantization noise is notch-

filtered at the output, while the signal is delayed by one clock cycle at the output. The loop filter H(z) can be easily implemented as a discrete bandpass filter of the form

$$H_{BP}(z) = \frac{-z^{-2} + \alpha z^{-1}}{1 - 2\alpha z^{-1} + \beta z^{-2}} \tag{3.6}$$

where the filter is sampled at frequency F_s, α represents the location of the center frequency with respect to F_s, and β represents the Q-factor of the filter. When H(z) is a second order discrete time bandpass filter, STF and NTF is given by

$$NTF = \frac{1 - 2\alpha z^{-1} + \beta z^{-2}}{1 - \alpha z^{-1} + (\beta - 1) z^{-2}} \tag{3.7}$$

$$STF = \frac{\alpha z^{-1} - z^{-2}}{1 - \alpha z^{-1} + (\beta - 1) z^{-2}} \tag{3.8}$$

For a filter with infinite Q with α=0, the quantization noise is shaped by a notch transfer function around $\pm(F_s/4)$, while the input signals have a two-period time delay. This noise shaping results in a high SNR in the signal bandwidth around the center frequency of the bandpass filter [16]. The oversampling ratio (OSR) for a bandpass ADC is defined as $(F_s/(2*F_{in}))$, where F_{in} is the bandwidth of the signals around the center frequency.

3.4 The continuous-time sigma-delta modulator

The discrete-time bandpass ΣΔ modulator as shown in Fig. 20a enables the conversion of a bandpass signal with narrow band at high center frequency, and makes the circuit implementation easy. However, these modulators cannot operate at higher frequency because the maximum clock is limited by the Opamp bandwidth and the settling time of the circuitry. In this type of ΣΔ modulators, the analog input is converted to a digital signal by a sample-and-hold stage, which may limit the linearity and noise floor of the entire system.

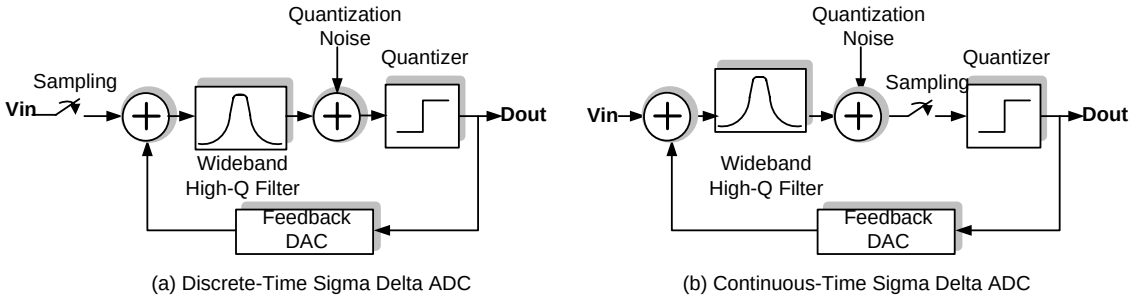
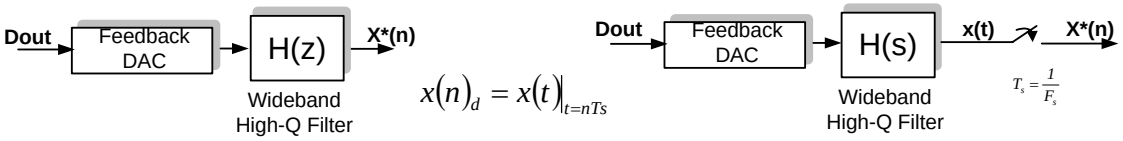


Figure 20 The discrete-time and continuous-time sigma-delta modulators

In contrast, a continuous-time ΣΔ modulator (fig. 20b) relaxes the requirements of high-speed Opamp because the signals vary continuously. The sampling occurs after the integrator rather than at the input of the ADC as in a discrete-time ADC; therefore the anti-alias filter may be eliminated. Also, a CT ΣΔ modulator has less power consumption than the discrete-time counterpart and thus it is suitable for high-speed and low-power applications.

It's intuitive that a continuous-time modulator can be obtained by replacing the discrete-time loop filter by continuous-time one. The question is how to choose the gain of loop filter. The key to designing a continuous-time filter is to make the two modulators behave exactly the same. If we apply the same input signal to the two modulators and simulate them in time domain, they will be equivalent when the same output bits are obtained at sampling time. It means that the input voltages of quantizer at sampling time are equal. This transformation between CT and DT domain is called impulse invariant transformation as they require the open loop impulse responses to be similar [24]. It maps the frequencies linearly from -π /(2*Ts*) to π /(2*Ts*) while other frequencies will be aliased to the transformed band.



(a) Discrete-Time Sigma Delta ADC (b) Continuous-Time Sigma Delta ADC

Figure 21 The impulse-invariant transformation

The open loop structure for both ADCs is obtained by breaking the feedback loop at the DAC inputs, as shown in Fig. 21. The value of $x(n)_c$ is obtained by sampling x(n), and condition for equivalence is given by

$$x(n)_d = x(t)|_{t=nT_s} \quad (3.9$$

This can be guaranteed if the impulse responses of both the open loop structures are the same at the sampling time instants. In frequency domain, the impulse-invariant transformation can be expressed as

$$Z^{-1}\left[H(z)\right] = L^{-1}\left[R_{dac}(s)H(s)\right]\Big|_{t=nT_s} \tag{3.10}$$

L^{-1} and Z^{-1} are the inverse Laplace and inverse Z transforms respectively. In time domain, the equivalence is given by

$$h(n) = \left[r_{dac}(t) * h(t)\right]\Big|_{t=nT_s} \tag{3.11}$$

where h(n), $r_{dac}(t)$ and h(t) are impulse responses of H(z), DAC and H(s), respectively. A continuous-time $\Sigma\Delta$ modulator can be designed by applying impulse invariant transformation [24]. If we have a discrete-time modulator with a loop filter *H*(*z*) that has a particular noise-shaping performance, we choose a DAC, and use (3.11) to find the transfer function of continuous-time loop filter. In this way, we can build a continuous-time modulator with the same behavior as the discrete-time modulator.

3.5 Non-linearities of ΣΔ modulators

The above theory describes the functionality of ideal $\Sigma\Delta$ modulator. There are certain considerations for the circuit realization regarding to the non-idealities. Here we will discuss some of them in continuous-time bandpass $\Sigma\Delta$ modulator [25].

Noise: In an ideal modulator, the quantization noise mainly determines the in-band noise floor of the modulator. However in practical circuit implementations, noise is also introduced by the active elements. As we know, noise due to the input, first integrator and first DAC are not shaped. These noise sources contribute to the noise levels of the modulator. The input OTA noise is inversely proportional to the transconductance Gm of the input differential pair. Increasing Gm will suppress the thermal noise, and the penalty is size or/and power consumption. Other noise may come from clock jitter and power supply noise. To achieve the best performance of modulator, it is common to make the contribution of circuit noise and distortion less than that of the quantization noise, which will preserve the performance of the modulator model.

Linearity: Transconductance nonlinearity introduces harmonic distortions, especially the third harmonic distortion. The harmonics will generate in-band noise and degenerate the SNDR. The major contribution of distortion comes from the non-linear behavior of transistors in the loop filter, thus transconductances used in such block need to be highly linear to achieve high SNDR performance. Source-degenerated differential pairs are mostly used in the transconductor's input to improve the integrator linearity. Increasing the saturation voltage of the input transistors reduces the distortion. However it will only help to some extent and is only valid for transistor in strong inversion. The suppression of distortion will inevitably come at the cost of power consumption.

Q-factor of the Loop Filter: The ideal loop filter in a $\Sigma\Delta$ modulator has an infinite Q-factor, which means that the gain and output impedance of transconductance amplifier are infinite too. However, it's not true. A finite Q-factor makes the noise transfer function flat in the center of signal band instead of sharp dip. For a modulator with high oversampling ratio (OSR), the effect is more obvious. There is always a minimum Q-factor to have a certain performance. The requirement of Q-factor is much relaxed as OSR is reduced. Also the Q-factor is related to the signal swing at the internal nodes of the system, which may cause saturation of transistors or instability.

Excess Loop Delay: In a continuous-time sigma-delta modulator, the output of quantizer drives feedback DACs and the output of DACs inject current or voltage back to the filter and close the loop. Ideally, the outputs of DACs respond immediately to the quantizer clock edge, however, transistor in DACs and comparator cannot switch instantaneously. The excess loop delay is caused by the fact that the time from the sampling clock edge until the output is fed back to the filter is not zero. With the excess loop delay, the discrete-time domain loop transfer function moves away from the desired loop transfer function because the modulator pulse response at the sampling instants is changed. It is imperative to consider the excess loop delay in design, especially for high-speed applications. The easy way to understand the effect of excess loop delay is to model it by a pole and look at the stability of the noise transfer function. With the pole existing and moving, the phase delay in loop may increase and

it implies worse modulator stability. Also the quantizer gain is not always a constant because it is input signal dependent, and the loop becomes unstable as the quantizer gain increases. Choosing a right DAC and tunable feedback coefficients can partially solve the problem and improve the performance of modulator. A multi-bit quantizer is somewhat helpful, but a feedback multi-bit DAC is required and a circuitry to reduce the DAC mismatch is not suitable for high-speed design.

Clock Jitter: The output of the feedback DAC is rectangular current or voltage pulses, and most of the charge transfer occurs at a constant value over a clock period. Therefore, clock jitter causes a random variation in the pulse widths of DAC and adds a random phase noise to the output bit stream because the feedback signal is added to the CT analog signal. Moreover, the timing uncertainty in the sampling clock causes an amplitude error in the continuous-time signal. Ideally, sampling of the sinusoidal signal occurs at a certain time ($t_{sampling}$); however, the time variation due to clock jitter makes the sampling occur at $t_{sampling}+t_{jitter}$, resulting in a magnitude error. Hence continuous-time $\Sigma\Delta$ modulators are sensitive to clock jitter. If a non-return to zero (NRZ) DAC is used, jitter only affects when the sign of output changes. However, in a return-to-zero (RZ) DAC, the pulse has both rising and falling edge during every clock cycle, so jitter problem worsens. NRZ feedback DACs are employed in the design instead of RZ to ease the impact of clock jitter.

3.6 Continuous-time bandpass ΣΔ modulator architecture

The choice of the ΣΔ ADC architecture depends on tradeoff between maximum signal to noise ratio (SNR) that can be obtained and the limited signal swing at all internal nodes (related to stability). The main architectural level choices for the ADC that affects its performance include the following: Order of the ADC (order of the loop filter), Single-loop or MASH (multi-stage noise shaping), Single-bit or multi-bit (number of comparator bits). A sixth order, single-loop and 2-bit quantizer architecture is chosen for the CT BP ΣΔ ADC implementation, which results in an optimum tradeoff between signal swing and SNR. A higher order loop filter increases the SNR, but it could suffer from potential stability problems as large signal swing may saturate the internal nodes. A single-loop is chosen over the multi-stage as the former leads to simpler implementation, thereby resulting in lower power consumption as compared to the latter choices.

The first step in the design is to identify the transfer function of a switched capacitor BP ΣΔ ADC which has the desirable loop transfer function with the required SNR and good stability performance. This is done by identifying the NTF of the ADC. In this case, it would be desired to have a notch transfer function around 200MHz with a 10MHz bandwidth. This could be achieved by forcing the NTF of the ADC equal to the inverse of a sixth order bandpass filter. The transfer function of the NTF is given as

$$NTF = \left(\frac{1}{H_{BP\_ideal}(z)} \right) \tag{3.12}$$

where the transfer function for a discrete bandpass filter is

$$H_{BP\_ideal}(z) = \frac{\left(\alpha_1 z^{-1} - z^{-2}\right)\left(\alpha_2 z^{-1} - z^{-2}\right)\left(\alpha_3 z^{-1} - z^{-2}\right)}{\left(1 - 2\alpha_1 z^{-1} + \beta z^{-2}\right)\left(1 - 2\alpha_2 z^{-1} + \beta z^{-2}\right)\left(1 - 2\alpha_3 z^{-1} + \beta z^{-2}\right)} \tag{3.13}$$

Such discrete-time transfer function implements a sixth order bandpass filter centered on 200MHz if a sampling frequency of 800MHz is used. The filter is realized by cascading three second order filters centered at 200MHz, 203MHz, and 197MHz thanks to coefficients α_1, α_2 and α_3. A Q-factor of 12 is used in all biquadratic sections in order to achieve a 10MHz bandwidth. A picture of the bandpass filter transfer function is shown below in Fig. 22.

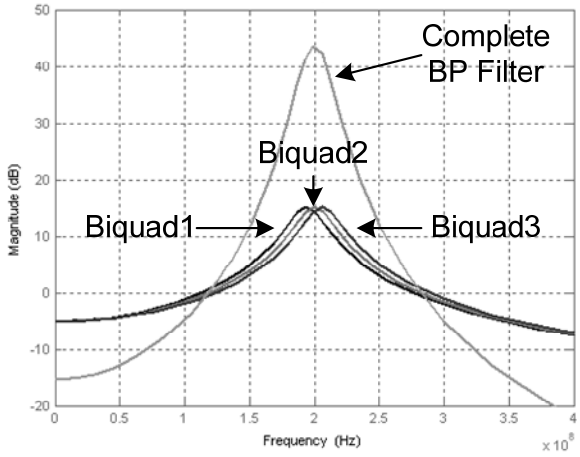


Figure 22 The transfer function of the sixth order bandpass filter

If equations 3.12 and 3.13 are plugged into 3.5, we can solve for the loop filter transfer function that yields the desired NTF as

$$H_{BP}(z)=\frac{\left(\alpha_1 z^{-1}-z^{-2}\right)\left(\alpha_2 z^{-1}-z^{-2}\right)\left(\alpha_3 z^{-1}-z^{-2}\right)}{\left(1-2\alpha_1 z^{-1}+\beta z^{-2}\right)\left(1-2\alpha_2 z^{-1}+\beta z^{-2}\right)\left(1-2\alpha_3 z^{-1}+\beta z^{-2}\right)}-1 \tag{3.14}$$

One important design consideration is the implementation of one clock period delay (z^{-1}) in digital domain from the quantizer and digital logic (this technique helps to reduce the metastability problem of the comparator, which is critical especially at high clock frequency). The z^{-1} delay can be accounted in the design procedure by factoring it out of (3.14). The modified H(z) that is used is given by

$$H_{BP\_mod}(z)=\left(\frac{\left(\alpha_1 z^{-1}-z^{-2}\right)\left(\alpha_2 z^{-1}-z^{-2}\right)\left(\alpha_3 z^{-1}-z^{-2}\right)}{\left(1-2\alpha_1 z^{-1}+\beta z^{-2}\right)\left(1-2\alpha_2 z^{-1}+\beta z^{-2}\right)\left(1-2\alpha_3 z^{-1}+\beta z^{-2}\right)}-1\right)\frac{1}{z^{-1}} \tag{3.15}$$

which together with the clock period delay from the quantizer and digital blocks results in the original loop filter transfer function.

The next step is to perform the impulse invariant transformation which transforms the z-domain (discrete-time) to s-domain (continuous time) transfer function, which is described in Section 3.3. The transformation ensures that the properties of both the structures are the same in terms of performance. A NRZ DAC is used for the IF ADC which reduces problems associated with clock jitter. The z-domain transfer function of loop filter transfer function given by (3.15) and the NRZ DAC transfer function is taken from [24]. Both are used in the transform to find the open

loop transfer function in CT domain. After the input invariant transformation is done as explained in [24], the open loop transfer function in the s-domain is given by

$$H_{BP}(s) = \frac{1.4e9s^5 + 2.5e18s^4 + 6e27s^3 + 6.7e36s^2 + 5.3e45s + 3.4e54}{s^6 + 1.9e8s^5 + 4.7e18s^4 + 6e26s^3 + 7.5e36s^2 + 4.7e44s + 3.9e54} \quad (3.16)$$

The block diagram of the CT BP ΣΔ ADC architecture for IF digitization is shown in Fig. 23. The loop filter in the forward path is a sixth order bandpass filter (cascade of three second order active-RC resonators). The output of the quantizer is a digitized version of the filter's output with an embedded half-period delay ($z^{-1/2}$). The digital bit stream D_{out} is in voltage mode and the delay control block provides another $z^{-1/2}$ delay to complete the full one period delay required in the loop. Then, D_{out} is converted into current by the six current DACs (b_1 to b_6) and injected back into the filter to close the negative feedback loop.

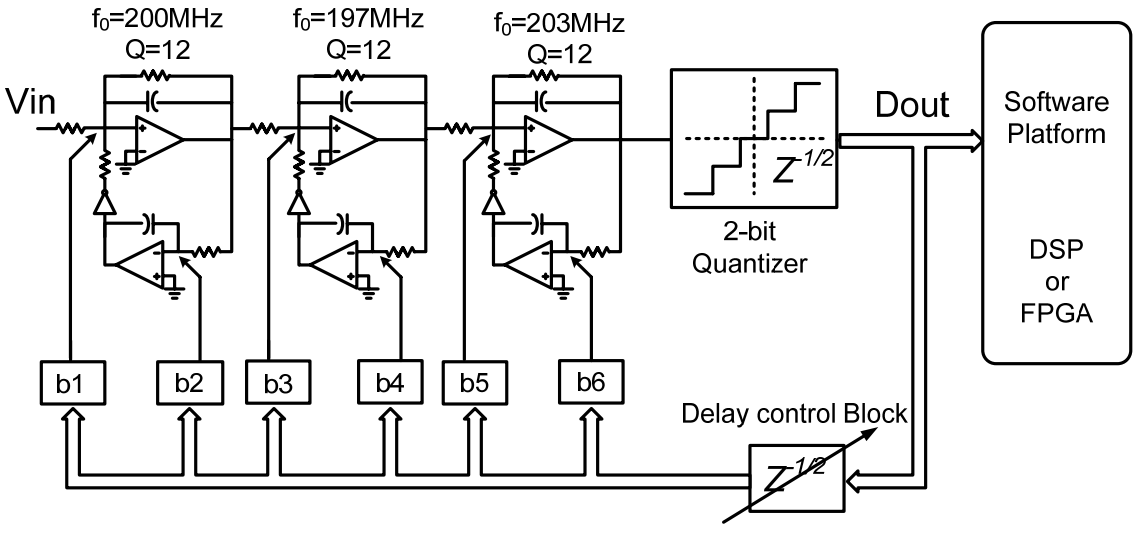


Figure 23 Block diagram of the IF ADC architecture

Assuming that the operational amplifiers are ideal, the open loop transfer function from the ADC output (V_{out}) to the comparator input (calculated by opening the loop) is given by

$$H(s)=\frac{A\left(k_5 s^5+k_4 s^4+k_3 s^3+k_2 s^2+k_1 s+k_0\right)}{\left(s^2+\frac{Q_1}{w_{o1}}+{w_{o1}}^2\right)\left(s^2+\frac{Q_2}{w_{o2}}+{w_{o2}}^2\right)\left(s^2+\frac{Q_3}{w_{o3}}+{w_{o3}}^2\right)} \tag{3.17}$$

where,

$$k5=b_6$$

$$k4=b_5+b_6\left(\frac{Q_1}{w_{o1}}+\frac{Q_2}{w_{o2}}\right)+Ab_4$$

$$k3=A^2b_2+Ab_3+Ab_4\frac{Q_1}{w_{o1}}+b_5\left(\frac{Q_2}{w_{o2}}+\frac{Q_1}{w_{o1}}\right)+b_6\left({w_{o2}}^2+\frac{Q_1Q_2}{w_{o1}w_{o2}}+{w_{o1}}^2\right)$$

$$k2=A^2b_1+Ab_3\frac{Q_1}{w_{o1}}+Ab_4{w_{o1}}^2+b_5\left({w_{o2}}^2+\frac{Q_1Q_2}{w_{o1}w_{o2}}+{w_{o1}}^2\right)+b_6\left(\frac{Q_1}{w_{o1}}{w_{o2}}^2+\frac{Q_2}{w_{o2}}{w_{o1}}^2\right)$$

$$k1=Ab_3{w_{o1}}^2+b_5\left(\frac{Q_1}{w_{o1}}{w_{o2}}^2+\frac{Q_2}{w_{o2}}{w_{o1}}^2\right)+b_6{w_{o1}}^2{w_{o2}}^2$$

$$k0=b_5{w_{o1}}^2{w_{o2}}^2$$

In the equations above, A stands for the DC gain of the biquadratic section. The terms w_{o1}, w_{o2}, and w_{o3} are the center frequencies of the three filters in units of radians per

second. Q_1, Q_2, and Q_3 are the Q-factors of the different sections. Finally, coefficients, b_1-b_6 are the feedback DAC coefficients introduced at different nodes of the filter.

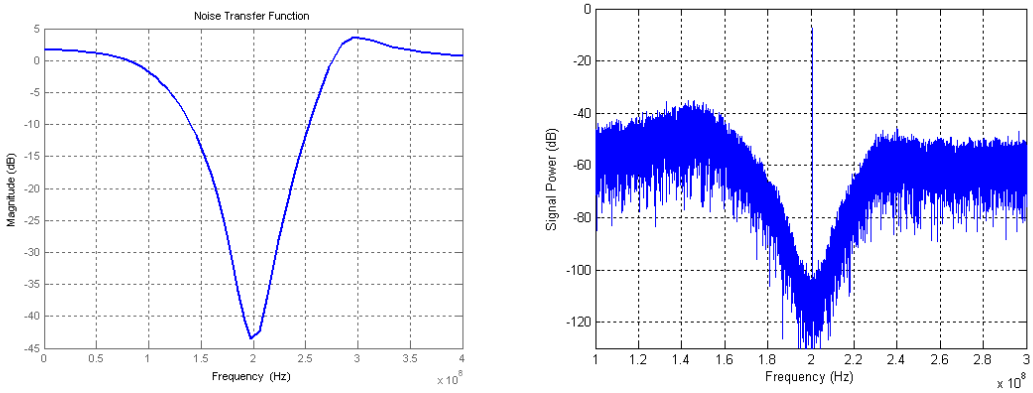
The shape of the NTF can be controlled precisely by tuning each of the numerator terms in the open loop transfer function, which results in the minimum possible integrated noise power over the entire bandwidth and SNR around 80dB. The loop coefficients b_1-b_6 can be calculated by equating each coefficients of the numerator in (3.16) and the (3.17). The final values of the optimized loop coefficients that are used in the IF ADC are shown in Table 5.

Table 5 6th order sigma-delta ADC transfer function parameters

Coefficient	Value	Coefficient	Value
A	2.5e11	**b_1**	2.1e-3
Q_1, Q_2, Q_3	12	**b_2**	1.80e6
w_{o1}	2π *200e6	**b_3**	2.2e-3
w_{o2}	2π *197e6	**b_4**	1.58e6
w_{o3}	2π*203e6	**b_5**	2.2e-3
z^{-1}	1.25e-9	**b_6**	1.75e6

The expected NTF of the ADC and the power spectrum of the 2-bit output of the IF ADC are shown in Fig. 24. The input signal is a sine wave at 200 MHz and the sampling clock frequency is 800 MHz. The measured SNR at the output of the ADC was 76 dB in a bandwidth of 14 MHz. The SNR was calculated for 65536 samples and the simulation used finite DC gain of 40 dB for each of the operational amplifier blocks in

Fig. 23. A step size of 0.05*Ts seconds (Ts is the time period of the clock) is used for the model, which ensures very good accuracy of the behavioral simulations.



(a) NTF of ADC **(b) Output Spectrum of ADC**

Figure 24 The NTF and the output power spectrum of the CT BP ΣΔ modulator

Two major challenges in the design of high performance CT BP ΣΔ ADCs are the analog filter and the 2-bit quantizer. In this case, demanding high-performance analog filters are needed to shape the in-band quantization noise and improve the Signal-to-Quantization Noise Ratio. (SQNR) The quantizer is another one of the most critical blocks for the high-speed operation. It requires a very low excess phase in order to ensure the stability of the system, and it requires very demanding offset immunity in order to avoid the degradation of the dynamic range in the system. In the following sections, the design of the 6^{th} order filter and the 2-bit quantizer will be described.

4. Gm-C FILTER CIRCUIT DESIGN

4.1 Introduction

A major challenge in the design of high performance CT BP ΣΔ ADCs is the design of the analog filter because large dynamic range is required due to the significant peak to average ratio of the resulting signals [26]. In this case, demanding high-performance analog filters are needed to shape the in-band quantization noise and improve the Signal-to-Quantization Noise Ratio. (SQNR)

Typical filter implementations are based on active elements such as active-*RC*, MOSFET-*C*, and Gm–C techniques [27]. Due to the need to handle speeds in the order of 200MHz and signal bandwidth up to 10 MHz, Gm–C solutions are generally preferred due to more efficient operation of wide-band operational transconductance amplifiers (OTAs) [28], [29]. However, the open-loop operated OTAs usually present limited linearity; therefore wide variety of alternative solutions were recently reported [28]–[36]. To optimize the performance of a Gm–C filter, it is desired to achieve a good balance between signal-to-noise ratio (SNR) and signal-to-distortion ratio (SDR). Therefore, the use of linearization schemes without sacrificing other important parameters such as noise level, power efficiency and frequency response is a must.

In [36], a novel linearization technique using a non-linear resistive degeneration scheme was presented. By creating a non-linear voltage at the source of a degenerated

transistor, total cancellation of 3rd order non-linearity is possible at the expense of a very small auxiliary differential pair. A linearity-tuning loop is also required since the cancellation scheme is based on the matching of N-type and P-type transistors which are more prone to PVT variations and mismatches. This section presents a modification to the linearization technique reported in [36] that removes the tuning loop by matching N-type transistors via AC coupling. The proposed OTA boosts the output current linearity of a typical source degenerated structure across temperature and PVT variations by more than 10 dB without the need of a calibration loop; the additional power needed by the auxiliary circuitry is less than 10% of the OTA's power, and the noise level increases by no more than 1 dB. The techniques are tested in the desired 6th order bandpass Gm-C filter consuming 113 mW and achieving a spurious-free dynamic range (SFDR) of 70dB with a 200mVp-p output swing.

4.2 Specifications of OTA

Since the desired filter is implemented using the Gm-C technique, the OTA is the core building block that determines the performance of the BP $\Sigma\Delta$ ADC. Linearity, noise and transconductance are critical specifications for the OTA to be used in the Gm-C bandpass filter.

High linearity and low noise are required in order to achieve the desired SNDR of the system. Since the desired in-band signal flows across the loop filter, having a very

linear filter is necessary. Any non-linearity in the filter would be reflected at the output of the ADC as spurs that would corrupt the desired signal. This is an independent effect from the noise shaping of the quantization noise, thus OTA non-linearities have to be lower than the predicted shaped in-band quantization noise.

As explained in section 3, noise injected by the loop filter degrades the performance of the ADC. Similar to the non-linear spurs of the loop filter, noise from the filter is not shaped by the loop. Instead, all in-band noise injected by the filter corrupts the desired signal content and is digitized by the quantizer degrading the effective SNR of the system. The noise introduced by the first stage for the loop filter is the most critical noise source in the filter since any noise from the following stages is attenuated by the gain of the previous stages when reflected to the input, and thus special attention must be paid to the first biquadratic section. Furthermore, if a high gain requirement is imposed on the filter in order to increase the noise shaping effect on the quantization noise; large output impedance for the OTA must be achieved. For a high DC-gain OTA with a demanding linearity specification at relatively high frequency, it is necessary to use large transistors, thus increasing the parasitic capacitance at the critical nodes. Since a differential structure is utilized, a common-mode feedback (CMFB) circuit is required at each output, which further increases the parasitics. As a result, the required effective transconductance $G_{m,eff}$ has to be increased since the center frequency of the resonator is determined by $G_{m,eff}/C$. After system simulations

on Matlab with macro-model representations of the OTA, the specifications of the OTA were obtained and listed in table 6.

Table 6 Loop filter OTA specifications

OTA Parameters	Values
DC-Gain	~40dB
Gm,eff	~3mA/V
Load Cap	2pF
Excess Phase @ 200MHz	< 2 degrees
IM3 @ 200MHz, 0.2 Vp-p Input	< 70dB
Integrated Noise (1MHz BW)	< 100uV
Power consumption	Minimized

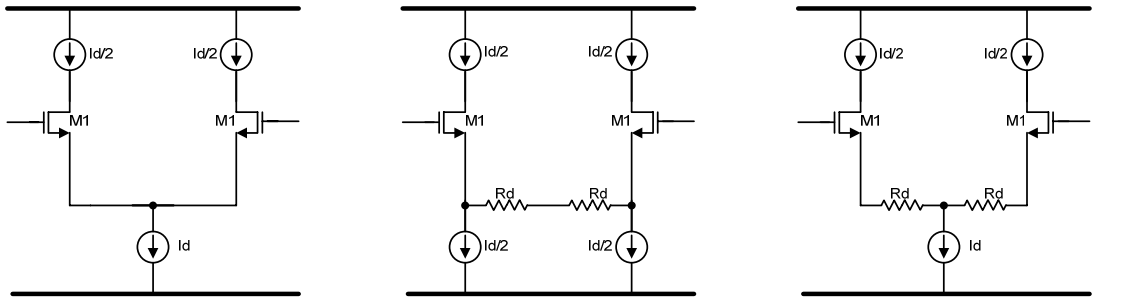
4.3 Typical OTA with source degeneration

The differential pair structure shown in Fig. 25 is a basic cell that offers good rejection to both common-mode input signals and power-supply noise. As long as all transistors operate in saturation region, the large-signal behavior of the single-ended output current can be described by a Taylor series expansion as follows:

$$i_d = I_D + g_{m1}v_{in} + g_{m3}v_{in}^{\ 3} + g_{m5}v_{in}^{\ 5} + \ldots \tag{4.1}$$

In this representation, it is assumed that the even-order harmonic distortions are not relevant due to the fully differential nature of the topology. For moderate signal swing, the first three terms are the most significant ones; I_D corresponds to the DC bias

current, g_{m1} is the linear transconductance term and g_{m3} is the undesired third-order nonlinear term.



(a) Conventional diff. pair **(b) Source degenerated diff. pair with lower voltage drop** **(c) Source degenerated diff. pair with improved noise**

Figure 25 Conventional structures for OTA with source degeneration techniques

A rough approximation for g_{m1} based on the saturation-square model for a MOS transistor and taking into account the mobility degradation effects as explained in [37]

$$g_{m1} = \frac{1}{2}\frac{\sqrt{\mu_n C_{ox}(W/L)I_T}}{1+\frac{2}{\varepsilon_{crit}}\sqrt{\frac{I_T}{WL\mu_n C_{ox}}}} \tag{4.2}$$

where μ_n and C_{ox} are a process parameters; W and L are the width and length of transistor, respectively. I_T is the tail current and ε_{crit} is the critical electric field. The coefficient of the third-order nonlinearity (g_{m3}) is obtained as

$$g_{m3} = -\frac{1}{16}\frac{\sqrt{\mu_n C_{ox}(W/L)I_T}}{\left(\frac{I_T L}{W\mu_n C_{ox}}\right)\left(1+\frac{2}{\varepsilon_{crit}}\sqrt{\frac{I_T}{WL\mu_n C_{ox}}}\right)^2} \tag{4.3}$$

If a source degeneration resistance R_d is added, as shown in Figs. 25b and 25c, the single-ended ac components of i_d approximately becomes

$$i_d = \frac{g_{m1}}{1 + g_{m1}R_d} v_{in} + \frac{g_{m3}}{\left(1 + g_{m1}R_d\right)^4} v_{in}^{\ 3} + \ldots \tag{4.4}$$

According to this expression, the third-order intermodulation distortion (IM3) is given by

$$IM3 = \frac{3}{4}\frac{G_{M3}}{G_{M1}} = \frac{3}{4}\frac{g_{m3}}{g_{m1}}\frac{1}{\left(1 + g_{m1}R_d\right)^3} v_{in}^{\ 2} \tag{4.5}$$

As shown in (4.5) the OTA's linearity can then be improved by increasing the product $g_{m1}R_d$. However, this approach decreases the overall transconductance which is given by $g_{m1}/(1+ g_{m1}*R_d)$ and usually results in higher noise levels, mainly due to the noise added by the DC current sources. The input referred thermal noise density for the differential pair of fig. 25b is easily derived and expressed as

$$\frac{\overline{v_{noise}^{\ 2}}}{\Delta f} = \frac{4kT}{g_{m1}}\left(\gamma + g_{m1}R_d + 2\gamma\left(g_{m1}R_d\right)^2 \frac{g_{mx}}{g_{m1}}\right) \tag{4.6}$$

where k is the Boltzmann constant, T the temperature in degrees Kelvin, γ is a fitting parameter, and g_{mx} is the small-signal transconductance of the transistor used as a DC current source.

Equation (4.6) shows that the input referred noise level will increase when the product $g_{m1}R_d$ is increased, especially due to the g_{mx} noise components. In fact, most of these noise components appear as differential noise at the OTA outputs if large source degenerated resistors are employed. In order to minimize this effect, the tail current transistor can be placed in the middle of the source degeneration resistor as shown in Fig. 25c. In this case the noise contribution of the tail current splits equally in both branches and appears as common-mode noise. The resistance and transistor mismatches present in the topology generate some differential output noise due to the tail current transistor, but noise increment is not significant even if those mismatches are unrealistically large as 10%. Another advantage of this topology is that the nonlinearities of the impedances lumped to the virtual ground node are not critical because it remains almost unaffected by the differential signal variations. The drawback of the circuit is the additional DC voltage drop across the resistors which reduce the headroom for the input signal. For 0.18um and smaller technologies headroom is limited and large v_{ds} voltages required in order to achieve fair IM3 performance are essential, thus architecture in Fig. 25b is a good candidate to achieve the desired performance.

4.4 Proposed OTA linearization technique

In the schematic depicted in Fig. 26a, the proposed linearized source degeneration OTA is shown. Its small signal representation is Fig. 26b, where v_x is the voltage at the source of transistor M1 and k in stands for the third order non-linear coefficient of v_x. It is assumed that the term $\partial^3 i_{d1}/\partial v_{ds1}^3$ is negligible since all transistors have large vds voltages so the non-linear behavior of the output impedance is minimized.

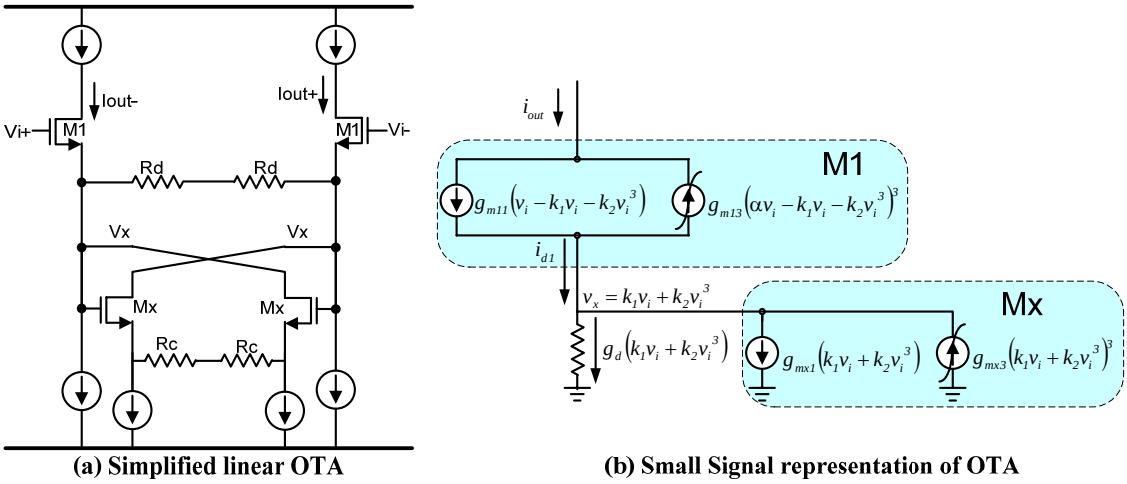


Figure 26 Small signal model of linearized source-degenerated OTA

The linearization technique aims to achieve total cancellation of third order coefficients by creating a non-linear voltage at the source of transistor M2 with some specific properties. Transistor Mx acts as a non-linear impedance that will modulate the v_{gs} voltage in M1 in order to achieve 3rd order non-linearity cancellation. Note that the

small signal voltage v_x in Fig. 26a can be considered as an odd signal function of v_{in} such as $K_1 v_{in+}K_2 v_{in}^3$ as shown in Fig. 26b.

The relationship between the output current I_{d1} and the input voltage v_i as a function of the desired non-linear voltage v_x at the drain of Mx is given by

$$i_{d1} = g_{mx1}(k_1 v_i + k_2 v_i^3) - g_{mx3}(k_1 v_i + k_2 v_i^3)^3 + g_d(k_1 v_i + k_2 v_i^3) \tag{4.7}$$

The expression for the output current I_{out} can also be obtained derived in the same fashion as shown below.

$$i_{out} = g_{m11}(v_i - k_1 v_i - k_2 v_i^3) - g_{m13}(k_1 v_i + k_2 v_i^3)^3 \tag{4.8}$$

By equating (4.7) and (4.8), manipulating both sides of the equation, and retaining the fundamental and the third order terms only, the equation below in obtained.

$$\begin{aligned} &v_i\left[g_{m11}(1-k_1) - g_{mx1}(k_1) - g_d(k_1)\right] + \\ &v_i^3\left[-g_{m11}(k_2) - g_{m13}(k_1)^3 - g_{mx1}(k_2) + g_{mx3}(k_1)^3 - g_d(k_2)\right] = 0 \end{aligned} \tag{4.9}$$

The expressions for k_1 and k_2 are extracted by equating the v_i and v_{i3} terms to zero which is the only valid solution for (4.9). After some algebraic manipulation and combining the result with $v_x = K_1 v_{in+}K_2 v_{in}^3$, the expression for the non-linear voltage v_x is derived as

$$v_x = \frac{g_{m11}}{g_{m11} + g_d + g_{mx1}} v_i + \frac{g_{m13}(g_d - g_{mx1})^3 + g_{mx3} g_{m11}^3}{(g_{m11} + g_d + g_{mx1})^4} v_i^3 \tag{4.10}$$

Finally, (4.8) and (4.10) are used to obtain the output current as a function of the input voltage, including the effects of the additional auxiliary circuitry.

$$i_{out} = \left(\frac{g_{m11}}{1 + \frac{R_d g_{m11}}{1 - R_d g_{mx1}}} \right) v_{in} + \left(\frac{g_{m13} - g_{mx3} \frac{(R_d g_{m11})^4}{(1 - R_d g_{mx1})^4}}{\left(1 + \frac{R_d g_{m11}}{1 - R_d g_{mx1}} \right)^4} \right) {v_{in}}^3 \tag{4.11}$$

From (4.11), the expression for the IM3 is obtained as (4.12) and simplified for the assumption of $R_d g_{mx1} << 1$, which in this case holds true.

$$IM3 = \frac{3}{4} \frac{g_{m13} - g_{mx3} (R_d g_{m11})^4}{g_{m11} (1 + R_d g_{m11})^3} {v_{in}}^2 \tag{4.12}$$

From (4.12) it is evident that making the numerator closer to zero yields an improvement in the linearity of the OTA by cancelling the third order non-linear coefficients of i_{out}.

In [36], a perfect non-linearity cancellation was very difficult to achieve due to the large fluctuations in process parameters tolerances and transistor mismatches. A linearity tuning scheme had to be introduced to alleviate such issue. While process tolerances and mismatches affect the proposed OTA as well, in this case the sensitivity to PVT variations is smaller since N-type auxiliary circuitry is utilized to be matched with the N-type main circuit. PVT variations will not be smaller, but they will affect both the main and the auxiliary parts in a more uniform fashion. Furthermore, (4.4) shows that

g_{m11} and g_{m13} come from source-degenerated transconductances; thus using a source-degenerated transconductance on the auxiliary circuitry will allow for a better matching of transconductances across process variations.

4.5 Simulation results for OTA

The complete input OTA is shown in Fig. 27. The OTA core consists of a degenerated differential pair with bias currents (MN1B) on the sides to avoid a voltage drop on Rd. The proposed N-type auxiliary circuit is connected to the gate of M1 via DC blocking capacitors. The degeneration factor ($g_{m11}R_d$) for the core circuit is about 3 since g_{m11} is 8.5mA/V and R_d is 350 Ohms with 1mA DC current flowing at each branch. The auxiliary differential pair is sized such that the bias current and the dimension of the devices are scaled with an 8 to 1 ratio resulting in a R_d*g_{mx} product of 0.2; thus holding true the condition $R_dg_{mx1} << 1$. Resistor R_b provides the necessary DC voltage to the drains of transistors M4.

In order to avoid large swing at the drain of transistor M1, C_x is used to provide an AC short to the source of M2 while Rx is used to provide the DC bias to the drain of M1. The voltage drop across R_x is 1.1V with 0.5mA DC current. Furthermore, Rx and C_x will introduce a zero pole pair that is located at low frequencies to avoid instability once the OTA is used in closed loop. The output stage of the OTA is introduced to take the current from the core stage and convert it into voltage due to the cascode

structure, which provides very high output impedance; therefore, large gain is achieved. The output cascode stage consumes 1mA of current per branch. The gates of transistors MN2B are connected to the common-mode feedback circuitry which will be discussed in section 4.5 as shown in Fig. 32 on page 68. Table 7 shows the transistor dimensions, resistor values and bias current of the proposed source degenerated OTA.

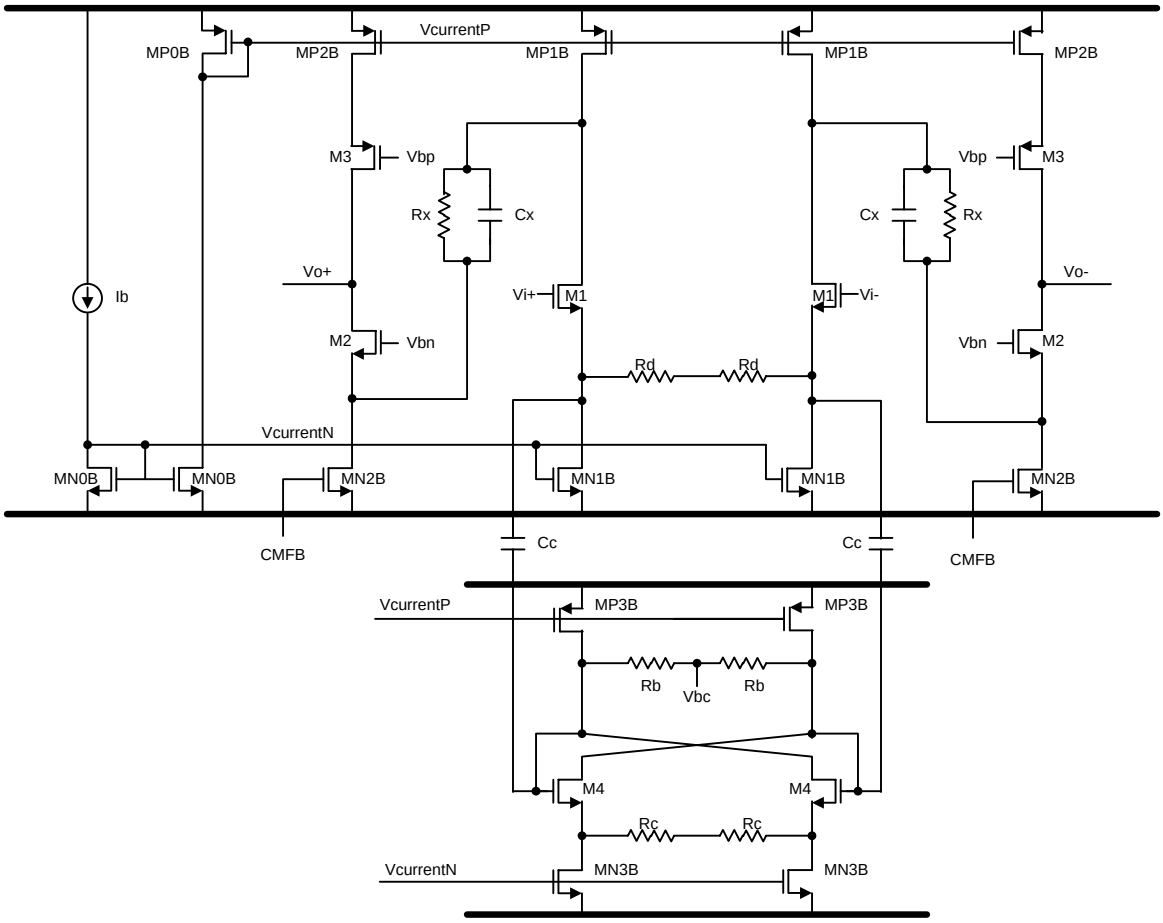
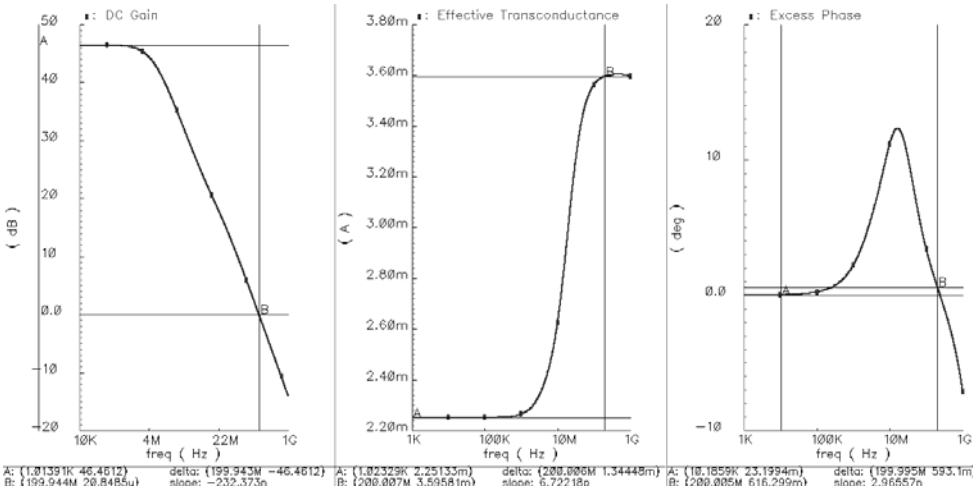


Figure 27 Complete circuit implementation of loop filter OTA

Table 7 Transistors dimensions, device values and bias conditions for loop filter OTA

Device	(m) width/length	Device	Size
M1	(32) 1.5um/300nm	Rd	350 ohms
M2	(48) 1.5um/300nm	Rc	360 ohms
M3	(60) 3.0um/300nm	Rb	1k ohms
M4	(4) 1.5um/300nm	Rx	2.25k ohms
MN0B	(48) 1.5um/600nm	Cx	5p F
MN1B	(48) 1.5um/600nm	Cc	10p F
MN2B	(72) 1.5um/600nm	Ib	1m A
MN3B	(6) 1.5um/600nm	Vin_dc	1.3 V
MP0B	(48) 3.0um/600nm	Vo_dc	1 V
MP1B	(72) 3.0um/600nm	Vbias	1.15 V
MP2B	(48) 3.0um/600nm	Vbias2	0.8 V
MP3B	(6) 3.0um/600nm	Vdd	1.8V

The simulation of effective transconductance and excess phase is performed by small signal AC analysis. A voltage source is connected at the output of OTA and the output current is measured. This setup eliminates the effect of the non-dominant pole. The DC gain of the OTA is 46dB. Fig. 28b shows that the effective transconductance of 3.5mA/V at 200 MHz. The excess phase is less than 0.6 ° at 200 MHz (Fig. 28c).



(a) DC gain and GBW **(b) Effective Transconductance** **(c) Excess Phase**

Figure 28 AC response of proposed OTA topology

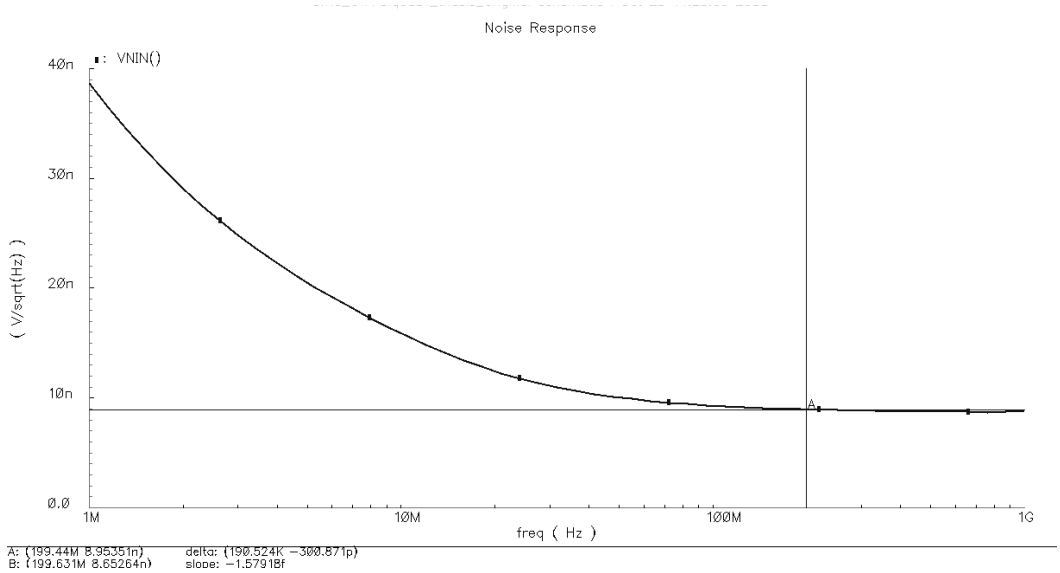
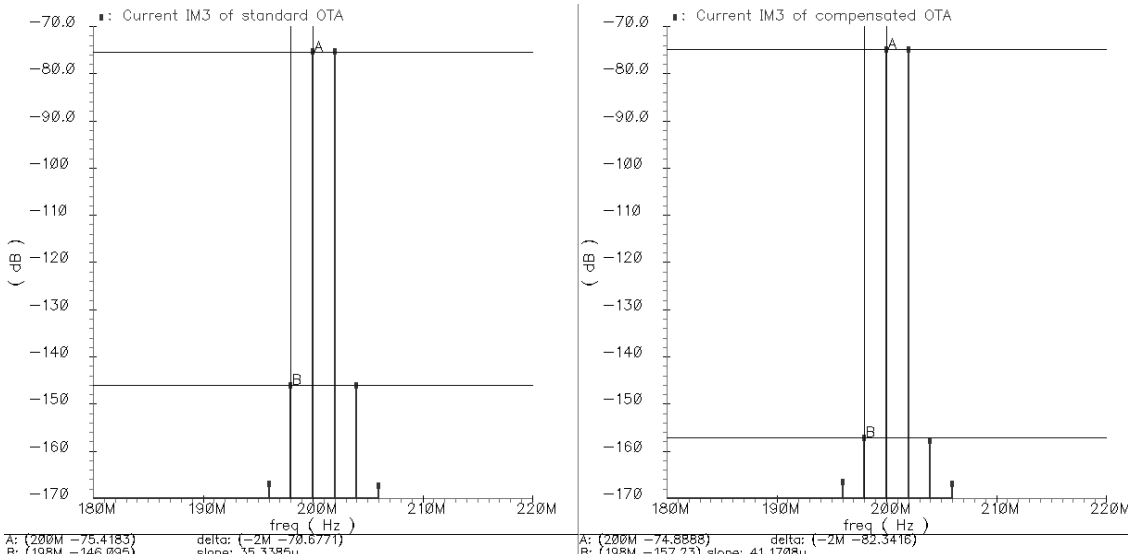


Figure 29 AC noise simulation of proposed source-degenerated OTA

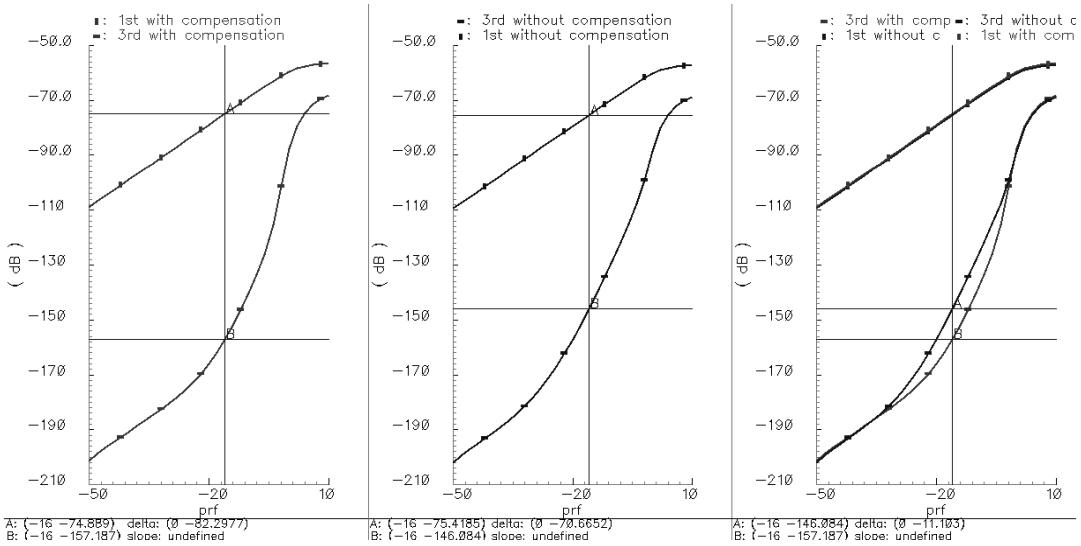
The linearity of the input OTA is characterized by IM3. The output is loaded with a capacitance of 2.5 pF to make the unity gain frequency 200 MHz. Two tones with 0.2V amplitude at 200MHz and 202MHz are applied to the input, and IM3 distortion is obtained by performing PSS analysis on Cadence and measuring the difference between one of the fundamentals and one of the intermodulation products at either 198MHz or 204MHz. Fig. 29 shows the AC noise results for the proposed OTA. Fig. 30 shows the IM3 of I_{out} for two different cases: a source degenerated OTA without auxiliary circuitry on Fig. 30a and the compensated OTA linearity on Fig. 30b. The image below shows a 12dB improvement in the linearity of i_{out} for the compensated OTA compared to the non-linearized one.



(a) Source degenerated OTA **(b) Source degenerated + linearity cacellation OTA**

Figure 30 IM3 comparison of standard OTA versus proposed scheme

Fig. 31 compares the behavior of the third order non-linearity as a function of the input signal swing. The behavior of the IM3 for the compensated OTA is shown in Fig. 31a. The uncompensated OTA is shown in 31b. A superposition of Fig. 31a and 31b is depicted in Fig. 31c. Note that for large input amplitudes, both 3rd order non-linearities follow the same trend. Such effect occurs because as the amplitude of the input signal is increased, the OTA starts to saturate which lead to signal clipping. At such condition non-linearity cancellation becomes impossible.



(a) Compensated OTA **(b) Standard OTA** **(c) Comparison**

Figure 31 1st and 3rd order terms of the output current for different OTAs

The simulation results for the proposed OTA are listed in the table 8 below. As shown below, the linearity of the output current exceeds by more than 12 dB the traditional source degenerated results at the cost of only 50uW increase in power consumption.

Table 8 Summary of OTA simulation results

OTA Parameters	Specifications	Traditional Source Degeneration	Proposed Linearization
DC-Gain	~40dB	48dB	46.6dB
Gm,eff	~3.5mA/V	3.6mA/V	3.58mA/V
GBW	200MHz	199.9MHz	199.9MHz
Load Cap	2.5pF	2.5pF	2.5pF
Excess Phase @ 200MHz	< 2 degrees	0.6^{o}	0.6^{o}
IM3 @ 200MHz 0.2 Vp-p Input	<70dB	70.6dB	82.3dB
Integrated Noise (1MHz BW)	< 10uV	8.6uV	8.9uV
Power consumption	Minimized	9.85mW	9.9mW

4.6 Structure of common-mode feedback for OTA

A Common-mode feedback (CMFB) circuit is necessary if the fully differential circuits are used. The common-mode signal of differential circuitry is sensed by a common-mode detector, and then compared to a reference voltage Vref. After the error is generated and amplified, a control signal forces the common-mode (CM) level of differential circuitry to a predetermined value. A CMFB circuit should meet several requirements. The DC gain of a CMFB loop should be large enough to force the CM signal to be very close to the reference voltage. A CMFB should only act on the CM signals and not affect the differential signals. Furthermore, a good phase margin is required in order to guarantee the stability in the loop. The CMFB circuit utilized in this work is depicted in Fig. 32.

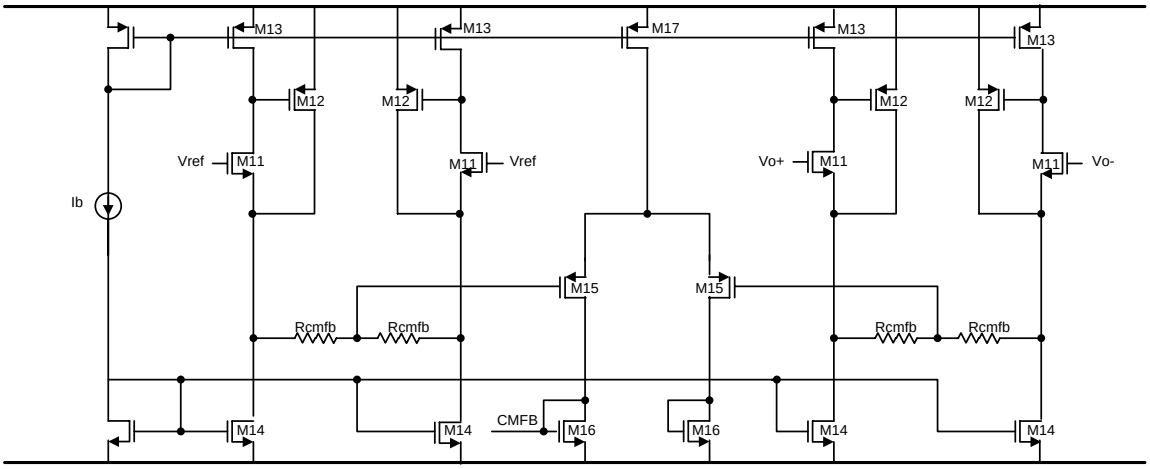


Figure 32 CMFB architecture

Note that the input of the CMFB circuit (on the right) comes from the output of the OTA and it is desired to have a DC bias of 1V. This is not convenient for a traditional differential pair (M11 for example) since the V_{gs} of the input transistor is around 0.7V leaving a very small room for the tail currents; this leads to a very non-linear circuit. In the proposed CMFB shown in Fig. 32, g_m of the input differential pair is increased not by increasing W/L of input transistors but by using a g_m boosting technique as explained in [37]. Such topology is realized by using M12 to increase the degeneration factor and to minimize g_m contribution for M1. In this way, the effective transconductance is dependent on the linear resistor R_{cmfb}, not on the non-linear M1 transistor.

A replica of the input differential pair is utilized to generate the proper bias voltage needed for the detection of common-mode errors. The output of the CMFB is the current of M16 that will be mirrored by transistors MN2B in the OTA. Table 9 shows the transistor dimensions, resistor values and bias current of the CMFB circuit.

Table 9 Transistors dimensions, device values and bias conditions for CMFB

Device	(m) width/length
M11	(48) 1.5um/300nm
M12	(22) 1.5um/300nm
M13	(2) 1.5um/300nm
M14	(12) 1.5um/600nm
M15	(30) 3.0um/300nm
M16	(24) 1.5um/600nm
Rcmfb	400 ohms
Ib	1.5mA

4.7 Simulation results for common-mode feedback for OTA

The phase margin and step-response of the common-mode loop are verified by AC and transient simulations. The frequency response is performed to a standalone OTA with a CMFB loop. Fig. 33 shows that the gain bandwidth product (GBW) of CMFB circuit is 195 MHz, and the phase margin is 55 °. The DC-gain of the CMFB loop is 55 dB. In order to test the step response of CMFB loop and to check the stability, a common-mode current pulse of 100 uA is injected to the loop and the input of OTA is measured. Fig. 33 shows that the 1% settling-time of the CMFB loop is around 5.5 ns. The common-mode current is 100uA, and a common-mode voltage around 26mV is generated.

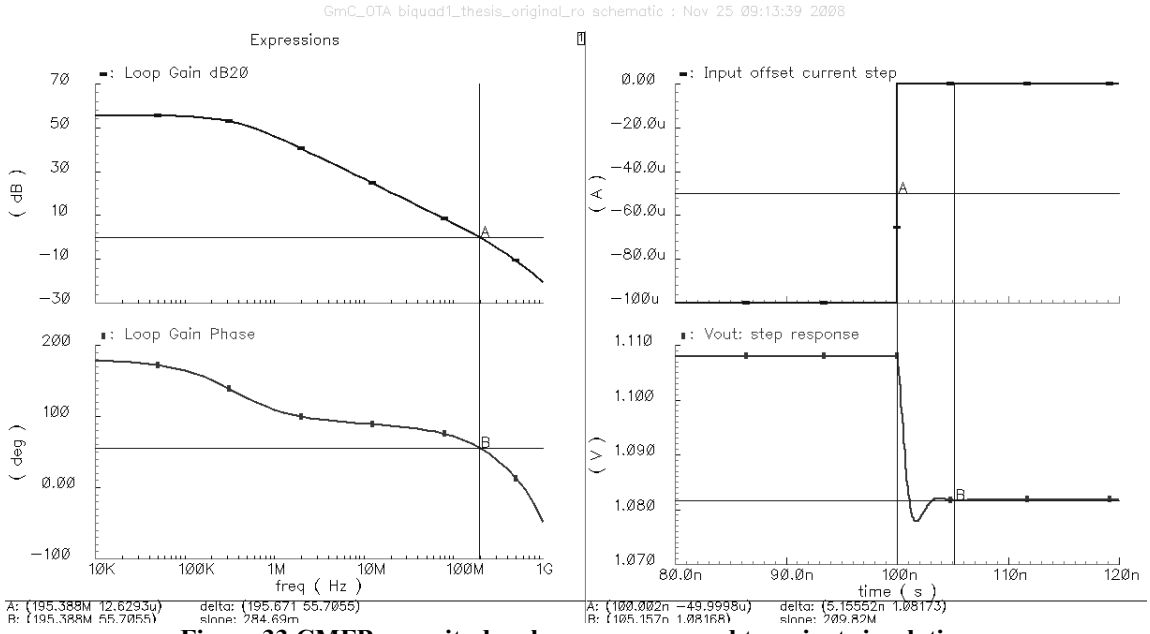


Figure 33 CMFB magnitude, phase response and transient simulation

Table 10 summarizes the performance of the CMFB circuit for the OTA.

Table 10 Summary of CMFB simulation results

CMFB Parameters	Values
DC-Gain	55dB
GBW	195MHz
Phase Margin	55^{o}
Power Consumption	5.4 mW
Settling Time (1%)	5.5ns

4.8 Gm-C filter structure

A Gm-C filter is designed using the aforementioned OTA cells. The CT CMOS OTA-C based high-order filter can be designed using either ladder structures or cascade of second order (biquadratic) sections. Ladder filters are superior to cascade structures in terms of insensitivity to parasitics and component variations. But, automatic tuning of ladders is in general more difficult, particularly with increasing filter order [28]. Cascading biquadratic sections allows almost independent control of resonant frequency, quality factors and peak gain of the filter. For bandpass applications, the dynamic range of both filters is similar. Higher programmability of the biquadratic sections makes it very attractive for tunable continuous-time bandpass filter applications [38]. Therefore, the sixth order continuous–time filter will be realized using cascade of three biquads with center frequencies at 197MHz, 200MHz and 203MHz in

order to achieve a 10MHz bandwidth. Furthermore, the impact of the non-linear output impedance of the OTA cells on the IM3 of the filter will be discussed.

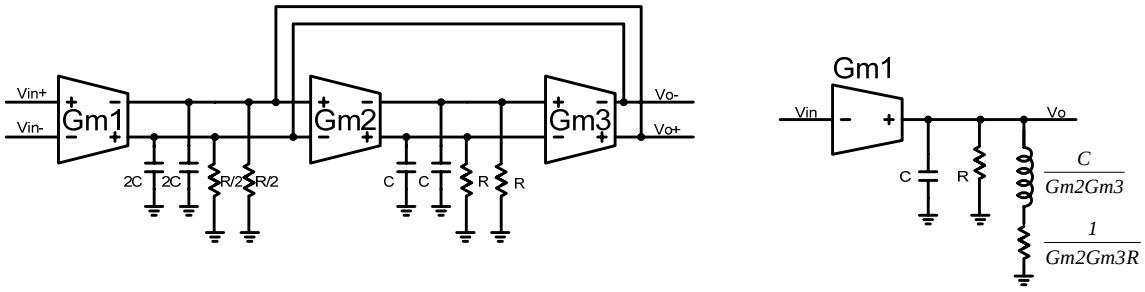


Figure 34 Lossy Gm-C filter

A lossy resonator, which is a second order bandpass filter, is depicted in Fig. 34. Gm1 converts the input voltage into current; Gm2 and Gm3 together with a capacitor C form a gyrator that emulates the effect of an inductor with ideal value of C/Gm2Gm3. If the output impedance R is included, the inductor the effective impedance becomes

$$Z_{eff} = \frac{1+sCR}{Gm2Gm3R} = s\frac{C}{Gm2Gm3} + \frac{1}{Gm2Gm3R} \tag{4.13}$$

which is nothing more than a lossy inductor. If no physical resistor R is placed, the quality factor Q of the inductor is limited by the output impedance of the OTA. From this result, the transfer function for the second order biquadratic cell is easily derived as (4.14) assuming that all three OTAs have the same output impedance.

$$V_{out} = \frac{\frac{Gm1(1+sCR)}{RC^2}}{s^2 + s\frac{2}{RC} + \frac{Gm2Gm3R^2+1}{R^2C^2}} \approx \frac{s\frac{Gm1}{C}}{s^2 + s\frac{2}{RC} + \frac{Gm2Gm3}{C^2}} \quad (4.14)$$

And the value for the center frequency ω_o and the Q-factor of the biquadratic sections are (4.15) and (4.16) respectively.

$$\omega_o \approx \sqrt{\frac{Gm2Gm3}{C^2}} \quad (4.15)$$

$$Q_{factor} \approx \frac{R\sqrt{Gm2Gm3}}{2} \quad (4.16)$$

The quality factor of the filter is given by the product Gm*R if Gm1=Gm2 =Gm3 is assumed; therefore, if a high Q filter is needed, it is a necessity to have large output impedance on the OTA. The complete implementation of one biquadratic cell is shown in Fig. 35. Note that capacitors Cc are used as AC couplers since the bias voltage at the input is set to 1.3V and the output of the OTA is around 1V. Resistors R_Q perform two functions: to provide the required DC bias at the input of the following OTA and it is used to tune the Q of the filter.

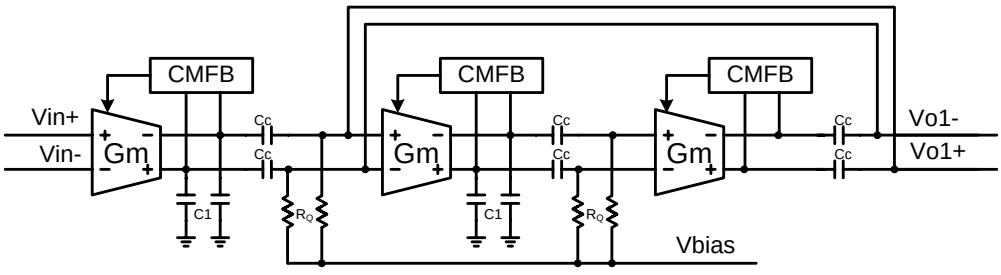


Figure 35 Complete biquadratic cell for CT bandpass filter

4.9 The linearity of the filter and the impact of the output impedance of the OTA

Due to the extremely high linearity specifications of the filter (>75dB) and the fact that smaller feature sizes come with a reduced voltage supply, many assumptions made on the design of the bandpass filter are no longer valid. In this case, the linearity of the filter is not only dependent on the output current but also on the linearity of the OTA output impedance. For the transfer function of a bandpass filter with signals operating only in the band of interest one can assume $\omega=\omega_o$, thus the transfer function of the filter in the band of interest is governed by $Gm1R_Q/2$ since the effect of the inductor is nullified by the feedback and grounded capacitor at the resonant frequency. From this result, it is normally assumed that Gm1 is the one responsible for the non-linearities of the filter while R_Q is linear; but a high-Q system is also limited by the output impedance of the OTA even if cascode output stages are used as depicted in Fig. 36.

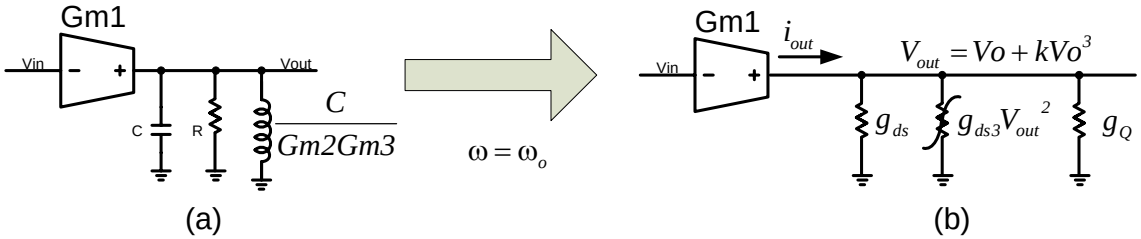


Figure 36 Small signal representation of the filter at resonant frequency

Let's consider the effect of the output impedance only. Assuming that the output voltage is of the form

$$V_{out} = V_o + kV_o^{\,3} \tag{4.17}$$

where, k is the third order coefficient of the output impedance of the OTA only. The value of k can be obtained if an ideal sinusoidal signal I_{out} is assumed and a non-linear V_{out} is obtained. From Fig. 36b, it is easy to derive the equation for the output current as a function of V_{out}.

$$i_{out} = \left(g_Q + g_{ds} + g_{ds3}V_{out}^{\,2}\right)V_{out} \tag{4.18}$$

where, g_Q is $1/R_Q$ or the physical conductance placed at the output of the filter for Q-tuning purposes, g_{ds} is the output conductance of the OTA, and g_{ds3} is the third order coefficient of the output conductance. Substituting of (4.17) in (4.18), we can obtain

$$i_{out} = \left(g_Q + g_{ds}\right)V_o + \left[k\left(g_Q + g_{ds}\right) + g_{ds3}\right]V_o^{\,3} + \ldots \tag{4.19}$$

which shows I_{out} as a function of k and Vo. If the assumption that an ideal sinusoid I_{out} was used, equation (4.19) will be valid only if the third order term is equal to zero. By doing this, the value for k is obtained in (4.20).

$$k = -\frac{g_{ds3}}{g_Q + g_{ds}} \tag{4.20}$$

From (4.16) and (4.20) the value for the IM3 of the output voltage as a function of the non-linear conductances in the OTA is derived.

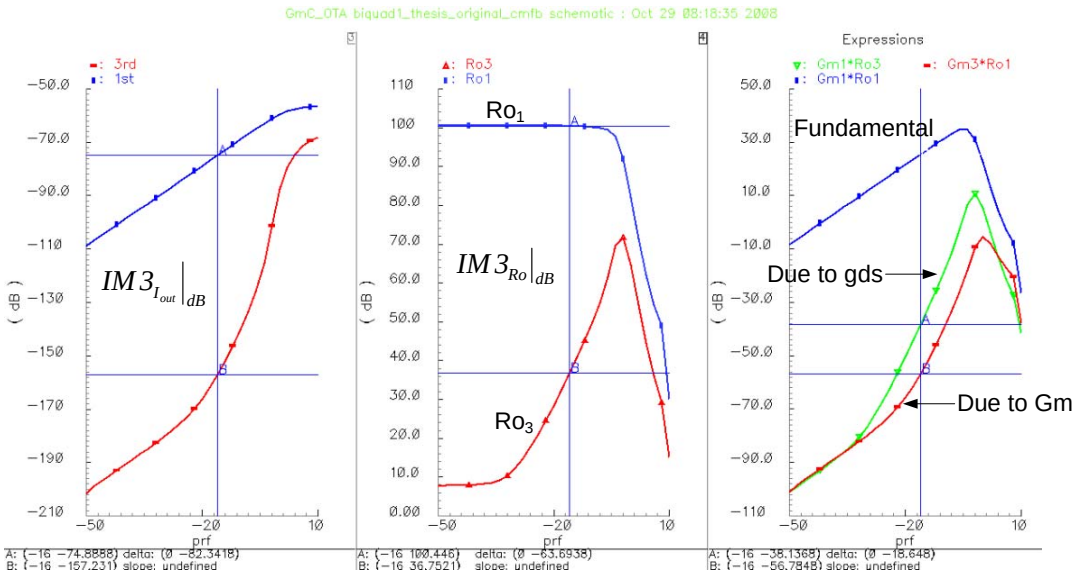
$$IM3_{Ro} = \frac{1}{24}\frac{g_{ds3}}{g_Q + g_{ds}} v_{in}^{\ 2} \tag{4.21}$$

From 4.21, it is clear that for better linearity performance lower g_{ds3} is required. This can be achieved by allowing larger Vds voltages for all transistors in the output stage of the filter. Sadly, this is not feasible since a limited power supply does not allow for such alternative.

It can be demonstrated that the total IM3 of the filter will be given by the combination of the non-linear voltage-to-current conversion performed by the Gm stage and the current-to-voltage conversion performed by the non-linear resistance as described by

$$IM3_{Filter} = IM3_{I_{out}}\Big|_{dB} + IM3_{Ro}\Big|_{dB} \tag{4.22}$$

The plot of the first and third order coefficients of the output current (g_{m1} and g_{m3}) as a function of the input voltage of the filter with Q=12 is shown below in Fig. 37a.

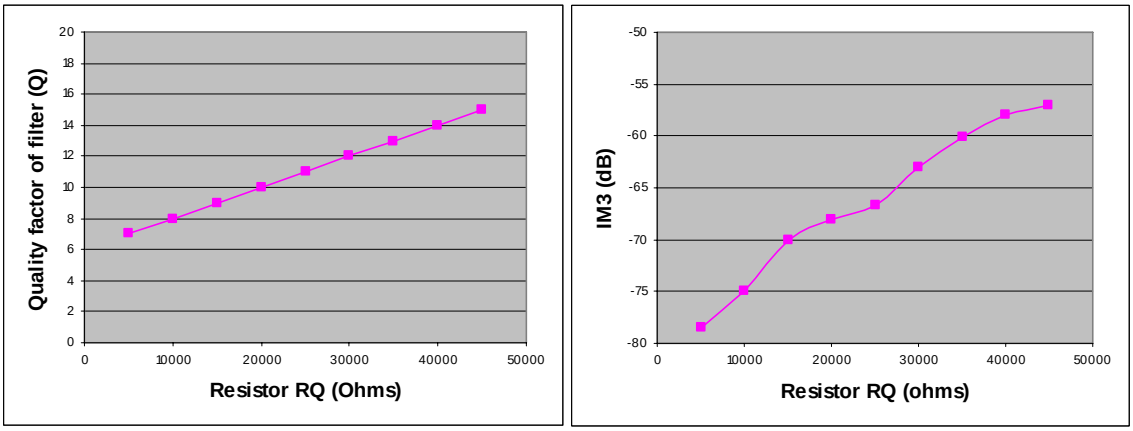


(a) gm1 and gm3 coefficients **(b) Ro1 and Ro3 coefficients** **(c) $IM3_{Iout}$ and $IM3_{Ro}$**

Figure 37 Output impedance and Gm linearity contributions

The markers are placed where the input voltage is 200mVp-p differential and the OTA is used at its maximum expected input power. At this condition the simulation plot yields an IM3 of -82.3dB for the linearity of the output current. While this result complies with the desired values, the coefficients for the output impedance of the OTA (g_{ds1} and g_{ds3}) shown in Fig. 37b yield an IM3 of only -63.7dB. By plotting the coefficients shown in (4.18) in Fig. 37c, it is clear that the limiting factor for the linearity of the filter is not the transconductor itself, but the output impedance. This effect introduces 18.6dB degradation on the linearity of the filter. Such effect, as stated before, applies to high Q systems, where g_{ds3} becomes dominant. For low Q systems, on the other hand, g_Q is large and the contribution of the non-linear behavior will be less

significant. For example, Fig. 38b shows the linearity of a biquadratic section as a function of the Q of the filter for a fixed output swing.



(a) Q-factor vs. RQ **(b) IM3 vs. RQ**

Figure 38 Q-factor and IM3 as a function of linear resistor R_Q

In this case, the resistor R_Q is varied and the input signal swing is adjusted to keep the output swing at 200mVp-p. On Fig. 38a, the quasi-linear relationship between the Q-factor of the filter and the resistor R_Q is shown. On the right side of Fig. 38b, it is clear that as the value for R_Q increases, the linearity of the system degrades considerably since the effect of the non-linear output impedance becomes more significant. For the same output swing but lower Q value, R_Q is small and the output resistance becomes more linear; therefore the IM3 increases.

4.10 Conclusions and final remarks

In this section, the design of a very linear OTA with more than 10dB improvement in the linearity of the output current at the cost of only 50uW power increase was presented. Even though such transconductor possesses more than 80dB IM3, the limiting factor for the implementation of a high-Q filter at 200MHz is the non-linear output impedance, which degrades filter performance by more than 12dB.

Larger headroom in the output stage and regulated cascode are some of the techniques that could be used to alleviate the output impedance issue. Such implementations require an increase in the power consumption of the OTA which may defeat the sole purpose of a Gm-C filter compared to an active-RC solution. As a consequence, the designed Gm-C architecture is not suitable for the implementation for the 6^{th} order filter in the CT-BP $\Sigma\Delta$ Modulator.

5. DESIGN OF A 2-BIT QUANTIZER WITH OFFSET CANCELLATION

5.1 Introduction

The two-bit non-return to zero (NRZ) quantizer samples the output of the sixth order filter and quantizes the sampled value to logic 1 or 0. The block diagram for the circuit implementation of the comparator is shown in Fig. 39. The summing amplifier is a gain stage and increases the signal swing in order to fully-load the quantizer. It is also the injection place of the two tones to be used in the digital calibration scheme to be discussed in section 6. The quantizer is composed of three switching comparators sampling the signal at 800MHz followed by current-steering latches and digital flip flops (DFFs) to complete the digitization of the signal. The switching action in the comparator causes the comparator output to couple back to the input (to the bandpass filter in this case), which may degrade the signal in the form of transient noise. This phenomenon is called kickback effect and it degrades the signal at the comparator input (thereby causing errors in the operation of the comparator) for high clock frequencies [39]. Preamplifier stages are used to isolate the analog from the digital blocks and to provide isolation and minimize the comparator kickback effect. The signal swing in the comparator should be within the power supply (± 0.90 V) and a DC level shifter is required before the gain stage in order to optimize the signal swing and to maintain all

transistors in proper operating region. The latch block samples the filter's output and also performs the quantization operation.

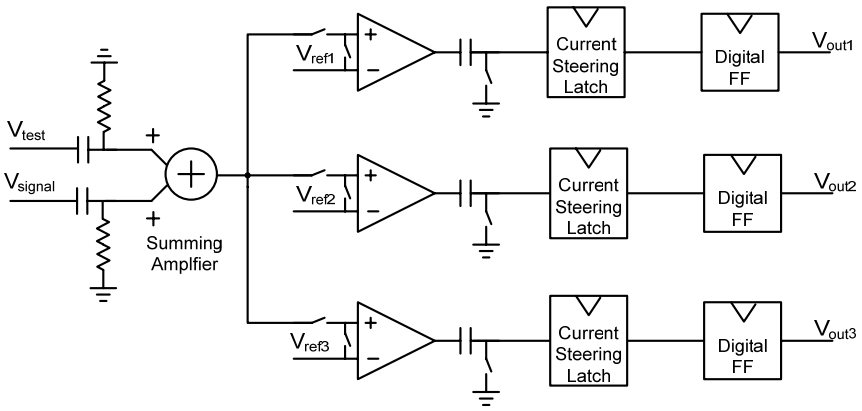


Figure 39 Simplified block diagram of the 2-bit quantizer

5.2 Circuit implementation of quantizer building blocks

The summing amplifier is depicted in Fig. 40. Its main purpose is the injection of two test tones at the input of the quantizer in order to perform digital background calibration for the ADC. The summing amplifier must also serve as a buffer between the quiet analog filter and the very noisy digital quantizer.

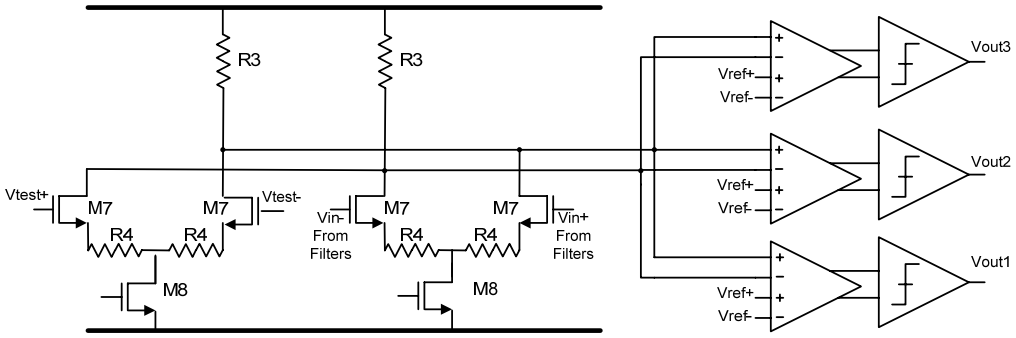


Figure 40 Schematic of the summing amplifier

The main concern in the design of the summing amplifier is large bandwidth. High speed is a necessity since excess loop delay must be minimized in order to guarantee stability in the system. Any extra delay needs to be taken into account when calibration of the loop delay is performed. The speed of the summing amplifier is determined by the RC product of the resistor R3 and the sum of the parasitic capacitance at the input of the three comparators. A gain of around 6dB in the summing amplifier is required in order to attenuate the digital glitches from the comparators that couple back to the filter. The gain of the summing amplifier is defined by the Gm*R3 product. Larger R3 yields larger gain, and larger swing, but it also leads to smaller bandwidth. The linearity requirement for the summing amplifier is not as stringent as that one of the filter, since the signal will be distorted by the comparators, but still an IM3 around -50dB is desirable. Resistor R4 introduces source degeneration in the design leading to a more linear circuit at the expense of lower Gm and lower gain. The final design of the summing amplifier yields a gain of 6dB, with 800MHz bandwidth and IM3 of -55dB. The component values and parameters for the summing amplifier are listed in table 11.

Table 11 Transistor sizes and bias conditions for the summing amplifier

Device	Size
M7	(20) 3.6u/360n
M8	(40) 3.6u/360n
R3	600 ohms
R4	325 ohms
Ibias	700uA
Vdd	1.8V

The schematic of the comparator is shown in Fig. 41. It takes the differential signal from the summing amplifier and compares it with the differential reference in order to obtain a single differential output. It performs offset cancellation of the differential amplifier and provides a DC level for the current steering latch to finally obtain a logic zero or one at the output of the comparator. The timing scheme for the sampling amplifier is shown in Fig. 42.

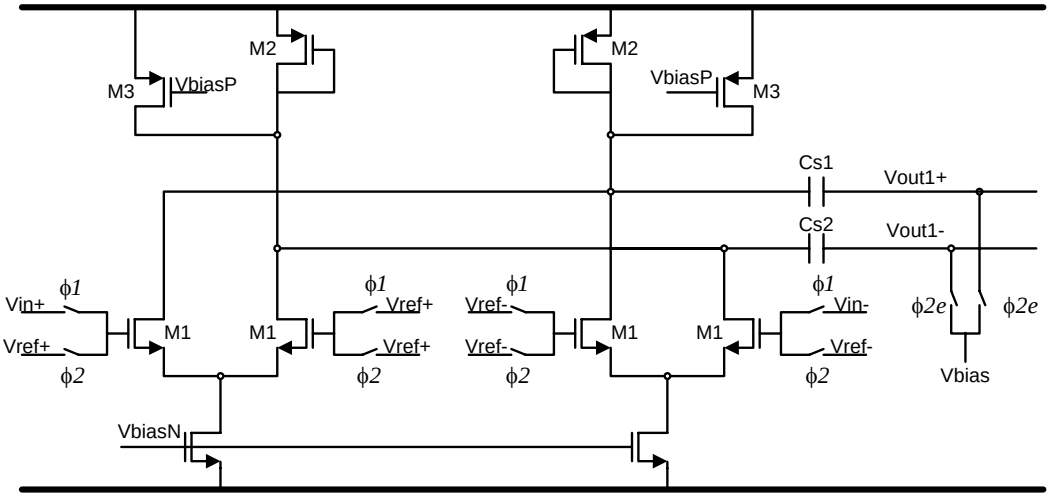


Figure 41 Schematic of the sampling amplifier

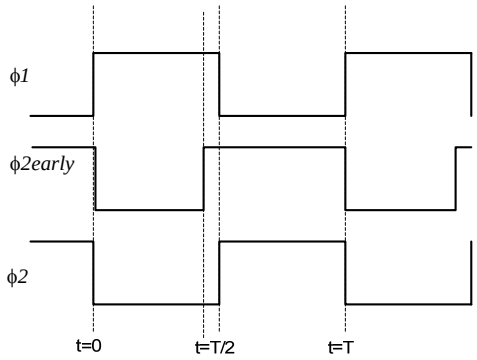


Figure 42 Timing scheme of the sampling amplifier and current-steering latch

The idea behind the offset cancellation scheme is to sample the offset of the differential amplifier during the decision stage of the latch and release it during the amplification stage in order to obtain an offset-free signal at the input of the decision latch. In order to fully understand the behavior of such circuit, a charge conservation analysis is required. By the charge conservation principle [40], it is known that the net amount of charge in a capacitive circuit will remain constant and is represented by the following equation:

$$\Delta Q_{phase1} + \Delta Q_{phase2} = 0 \tag{5.1}$$

Fig. 43 shows the behavior of the circuit comparator during phase two assuming both differential pairs have different static offsets such as V_{os1} and V_{os2}.

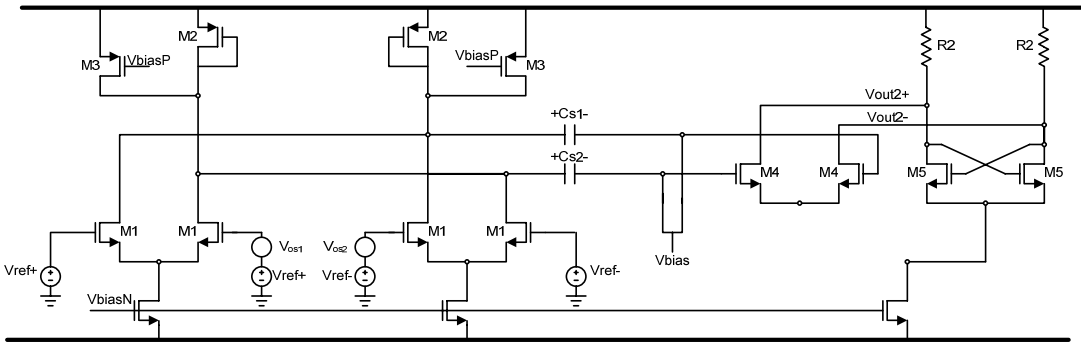


Figure 43 Sampling amplifier and latch during latching phase (ϕ2)

Note that during this phase, both inputs of every differential pair are tied either to V_{ref+} or V_{ref-} which are the reference voltages of the comparator in order to measure

and sample the offset introduced by the amplifiers. Starting from phase two, the charge stored in capacitors Cs1 and Cs2 are given by the product of the capacitance Cs times the voltage across Cs1 and Cs2, respectively. In this case, the charge stored in capacitors Cs1 and Cs2 is:

$$Q_1(t_o) = \frac{Cs}{2}\left[-\frac{g_{m1}}{g_{m2}}(V_{os1} - V_{os2}) - V_{bias}\right] @ \phi 2 \tag{5.2}$$

$$Q_2(t_o) = -Q_1(t_o) \ @ \ \phi 2 \tag{5.3}$$

where the gain of a single branch is given by the ratio of g_{m1}/g_{m2}. It is also important to remark that during $\phi 2$ the bottom plate of the capacitor is connected to V_{bias} in order to set the voltage bias for the input of the latch during the amplification.

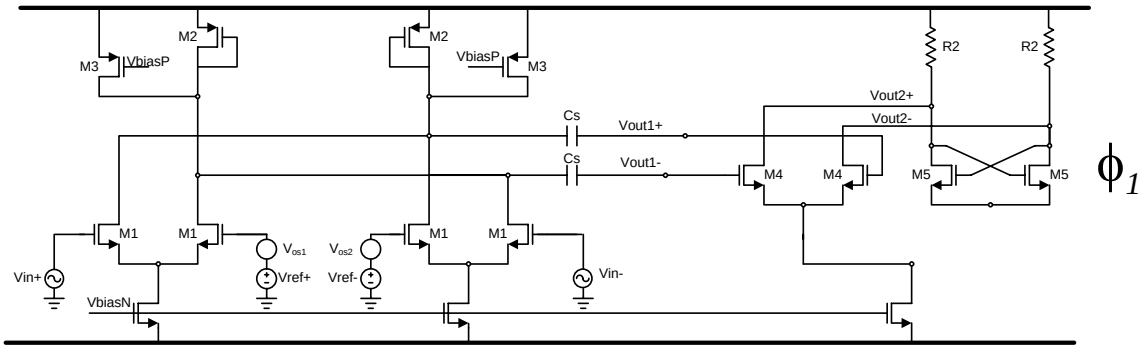


Figure 44 Sampling amplifier and latch during amplification phase (ϕ1)

Fig. 44 shows the behavior of the comparator during the amplification phase (ϕ1). In this case, two of the input terminals are switched from V_{ref+} and V_{ref-} to V_{in+} and V_{in-} in order to compare the signal from the filter with the reference voltages. The

bottom plates of capacitors Cs1 and Cs2 are disconnected from the bias voltage and are connected to the inputs of the current-steering latch (V_{out+} and V_{out-}) to perform amplification of the difference between V_{in} and V_{ref}. The charges stored in the capacitors are given by

$$Q_1(t) = \frac{Cs}{2}\left[\frac{g_{m1}}{g_{m2}} v_{in-}(t) + \frac{g_{m1}}{g_{m2}} V_{refp} - V_{os1}\right] + Q1(t_o) \text{ @ } \phi 1 \tag{5.4}$$

$$Q_2(t) = -Q_1(t) \text{ @ } \phi 1 \tag{5.5}$$

By plugging in equations (5.2) and (5.4) into (5.1), the value of V_{out+} can be derived as

$$V_{out+} = -\frac{g_{m1}}{g_{m2}} v_{in-}(t) + V_{bias} \tag{5.6}$$

$$V_{out-} = -V_{out+} \tag{5.7}$$

The effective voltage output sampled at the end of the amplification stage is given by the difference between V_{out+} and V_{out-} which is nothing more than the amplified version of the difference between the input signal and the reference voltage as given by

$$V_{out\_diff} = \frac{g_{m1}}{g_{m2}}\left(v_{in\_diff}(t) - V_{ref\_diff}\right) \tag{5.8}$$

Table 12 shows the components used for the implementation of the comparator's first stage.

Table 12 Transistor devices and bias conditions for the sampling amplifier

Device	Size
M1	(2) 7.2u/180n
M2	(2) 6.0u/180n
M3	(4) 7.2u/180n
MbiasN	(30) 7.2u/360n
SwitchN	(8) 4.5u/180n
Cs1	750fF
Cs2	750fF
IbasN	3mA
IbiasP	2mA
Vdd	1.8V

The schematic of the current-steering latch is shown in Fig. 45. When the clock is in the amplification phase (ϕ1), the differential pair formed by transistors M4 is active and it amplifies the input signal. At the falling clock edge, the signal is sampled and its value at that time instant becomes the initial condition for the next clock phase. When the clock reaches the latching phase (ϕ2), the positive feedback cross coupled differential pair formed by M5 is active and the output reaches either logic 0 or 1.

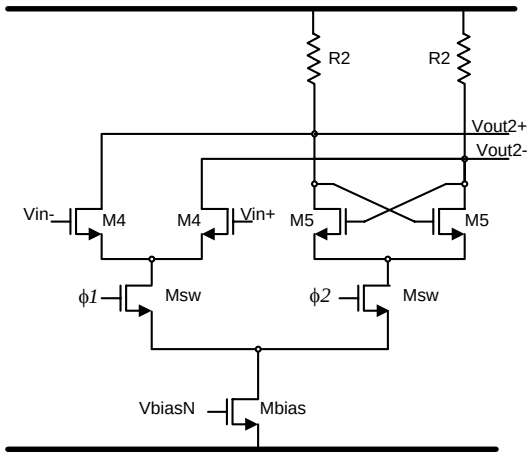


Figure 45 Schematic of the current-steering latch

The regeneration time of the latch, defined as the time taken for the output to reach a logic decision is given by equation (5.9) as explained in [39]:

$$T_{regeneration} = \frac{\tau_{latch}}{g_{m5}R_2 - 1} ln\left(\frac{V_{o,latch}}{V_{latch,t=0}}\right) \tag{5.9}$$

where τ_{latch} is the time constant of the latch (equal to the product of resistance and the total capacitance at the output node), $V_{o,latch}$ is the output voltage and $V_{latch,t=0}$ is the initial condition at the output. The regeneration time increases for very small value of inputs and it can be decreased by increasing g_{m5} (increase in the tail current), which results in higher power consumption. The value of the resistor R2 cannot be increased arbitrarily as it affects the output signal swing. The sizes and parameters of the current-steering latch are listed in table 13.

Table 13 Transistor sizes and bias conditions for the current steering latch

Device	Size
M5	(8) 1.8u/180n
M4	(2) 1.8u/180n
R2	500 ohms
Msw	(2) 1.8u/180n
Mbias	(30) 7.2u/360n
IbiasP	3mA
Vdd	1.8V

The DFFs in the signal path are implemented as shown in Fig. 46. Current Mode Logic is used in order to minimize propagation delay. The switching transistors, M1 and M2 are biased at the boundary of saturation region. The PMOS loading transistors M3,

M4, M5, and M6 operate in linear region, which lower the RC time constants associated with the output nodes of D flip–flop. The bias–dependent channel resistance of these load transistors also helps to increase the maximum speed at low power consumption. The output swing of D flip–flops is limited to 500mV. The reduction in voltage swing from input to output obviates the power–speed trade–off. The component values of the DFF are given in Table 14.

Table 14 Transistor sizes and bias conditions for D-flipflop

Device	Size
M8	(1) 2u/180n
M7	(2) 2u/180n
R6	(4) 5u/180n
Mbias	(4) 3.6u/180n
IbiasP	1m
Vdd	1.8V

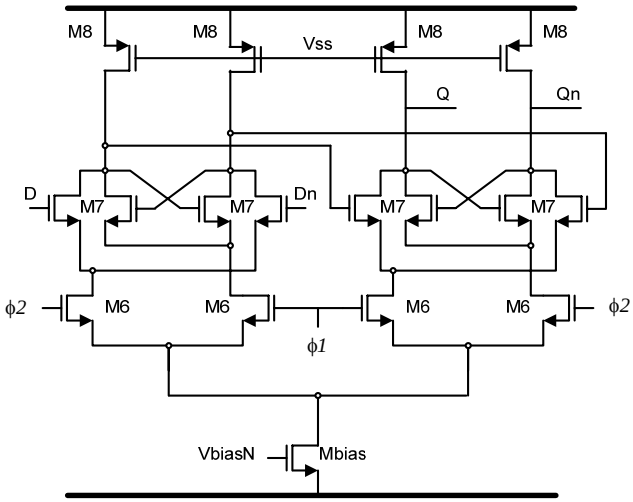


Figure 46 Schematic architecture for D-flipflop

5.3 Simulation results for 2-bit quantizer

The input and output waveforms of the comparator from post-layout simulations are shown in Fig. 47.

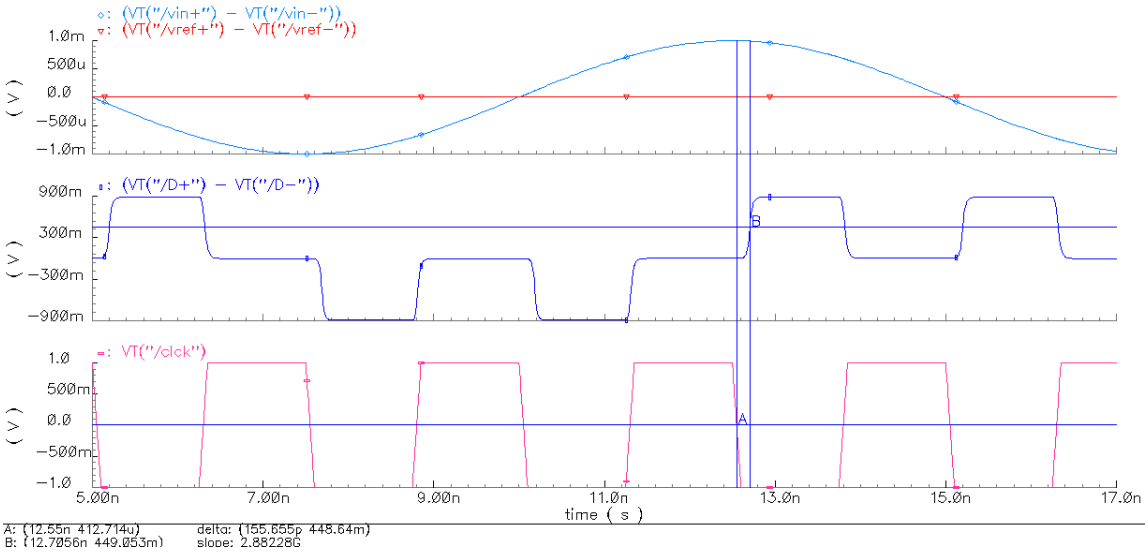


Figure 47 Simulation results of a single comparator (delay ~150ps)

As afore mentioned, the quantizer is a series of three latched-type comparators in parallel whose output drives a logic circuitry to adjust for the excess loop delay of the system. Ideally, the comparators should respond immediately to the quantizer clock edge; however, in practice the transistor cannot switch instantaneously. Fig. 47 shows that there is a delay (about 150ps) between the clocking instant and the transition at the output of the current steering latch. The excess delay is a contribution to the $z^{-1/2}$ delay required in the system. Since the latched-type comparator has a finite

regeneration gain, it means that the excess loop delay depends on the input signal and a small quantizer input leads to a longer delay. The comparator was further tested for offset immunity by injecting an static offset voltage at one of the four inputs of the sampling amplifier. Post-layout simulations showed immunity up to 10mV static offset voltages.

Shown in Fig. 48 is the output of the current steering latch for the first comparator running at 800MHz. In this block, the differential input signal (400mVp-p differential) is compared with the reference voltage (200mV). Fig. 49 shows the output for the second comparator where the input signal is compared with zero. In the same way, Fig. 50 depicts the output of the third comparator where the signal is measured against the negative reference voltage (-200mV).

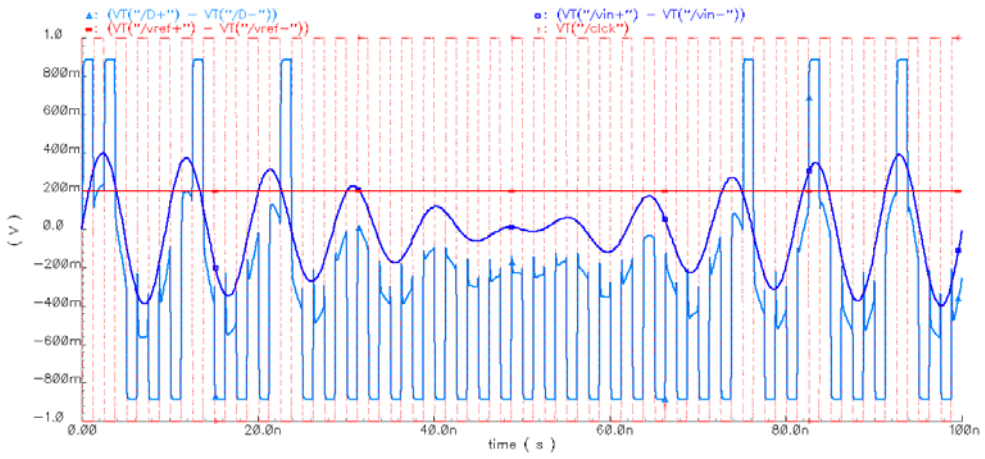


Figure 48 output of the first comparator (vref=200mV)

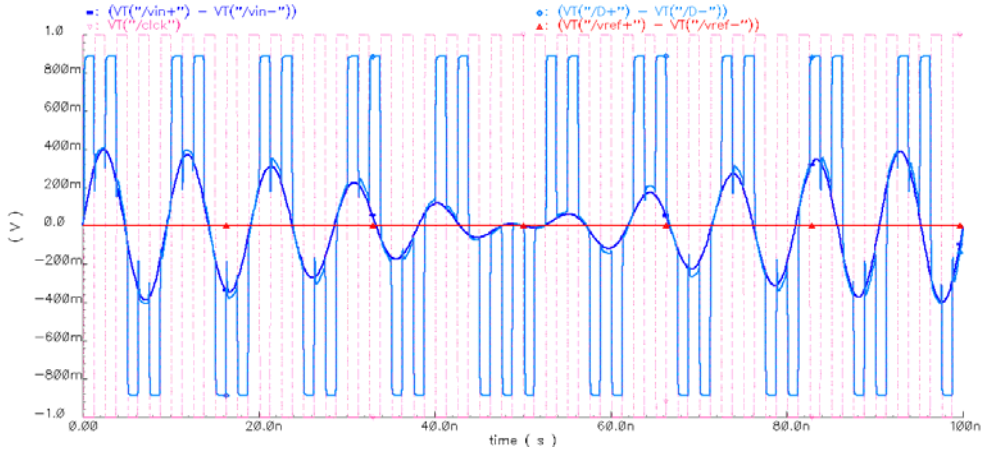


Figure 49 output of the second comparator (vref=0V)

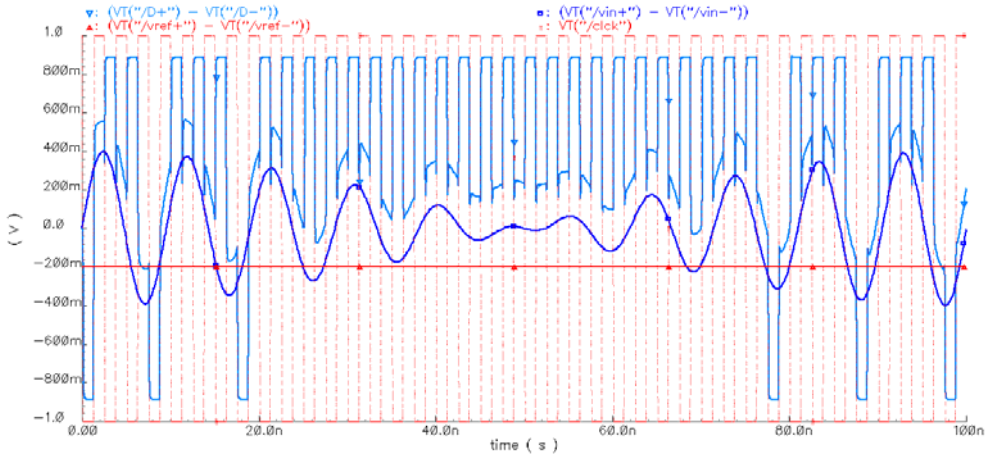


Figure 50 output of the third comparator (vref=-200mV)

The differential input swing can be as large as 200mVp-p and the output swing of the quantizer D-flip flop is around 0.8V as shown in Fig. 51, which is sufficient to drive the subsequent blocks. The output of the quantizer drive very low impedances since a series of D-flip flops are used to adjust the excess loop delay of the system. The image below shows the three differential signals coming out of the quantizer. The

signal at the bottom shows the summation of the three digital signals demonstrating the 4 output levels.

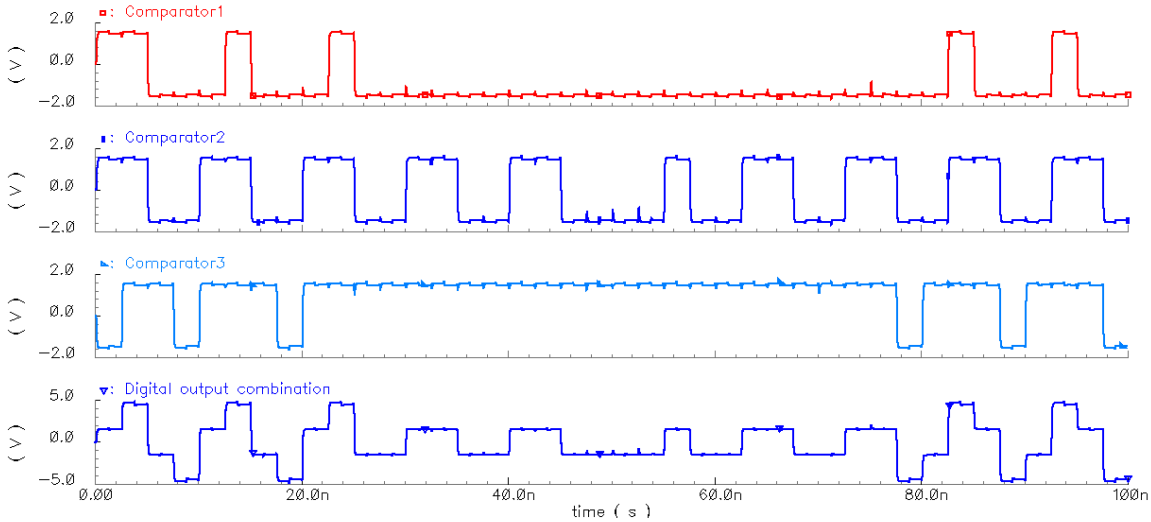


Figure 51 Digital Output of the D-flipflops

5.4 Post-layout simulations of the CT-BP ΣΔ ADC

The quantizer and all individual blocks described in section 3 were connected together according to the architecture in Fig. 23, in order to obtain the top level circuit implementation of the ADC. The transient simulation of the ADC is performed in Cadence by applying a test input signal at 200MHz. Impedance matching blocks are used both at the input and output to ensure proper coupling of all signals. The output bit stream is captured using the Analog artist calculator tool. The output bit stream file is processed in the calculator and the SNR of the ADC is calculated by using the FFT command. The power spectrum at the ADC output from post-layout simulations is

shown in Fig. 52. The number of samples used is 16384 and the output SNR was 72.2 dB in an 11 MHz bandwidth around 200 MHz. The number of samples is restricted by the limited computing resources, since a top level extracted simulation can take about 1 week to generate 16384 samples. A higher number of samples (65536 samples) are required to get an accurate estimate of signal and noise power values.

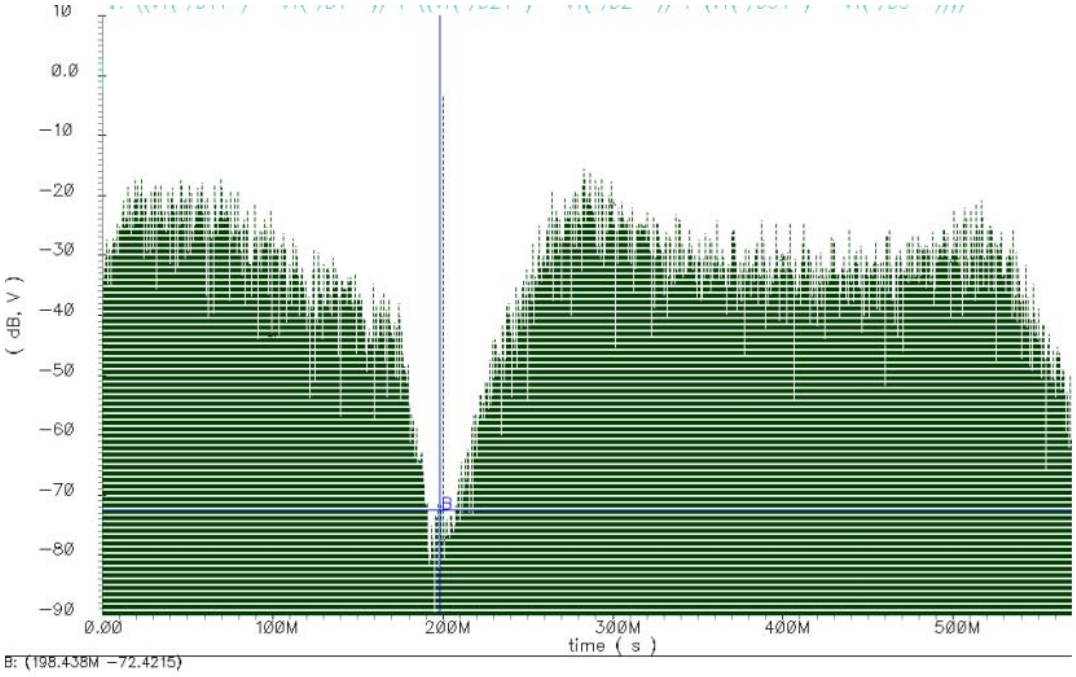


Figure 52 DFT of the digitized output signal using cadence calculator

Furthermore, if the data is exported to a digital platform such as Matlab, clearer results can be achieved as shown in Fig. 53. From the image below, we can see that the SNDR of the ADC is around 78dB when a two-tone test is performed.

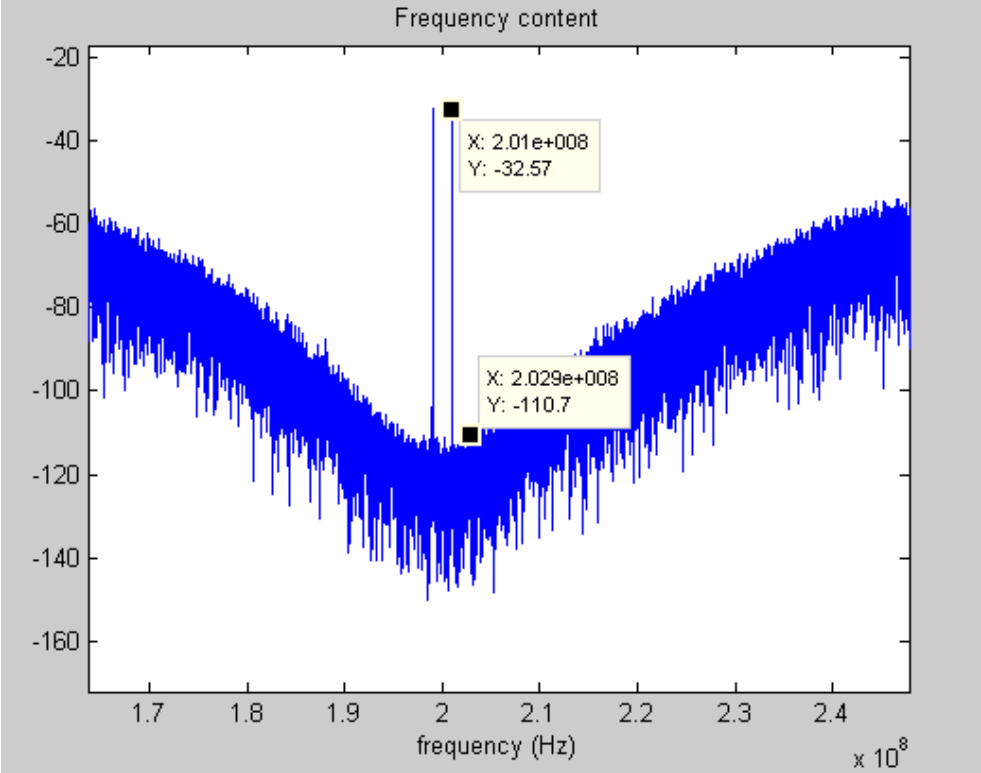


Figure 53 DFT of the output spectrum of the ADC after Matlab processing

The current consumption of the different ADC blocks is shown in Table 15. The largest share of power consumption is from the bandpass filter and is about 45%. The stringent linearity requirements increase the power consumption in both the bandpass filter and the integrator DACs. Power optimization is done at architecture and circuit level while maintaining the dynamic range and stability of the ADC.

Table 15 Current consumption distribution for the CT BP ΣΔ ADC

Block	Current consumption	Percentage of overall power
6^{th} order Bandpass filter	34.8 mA	45 %
Feedback DAC	8 mA	10 %
2-bit quantizer	21 mA	27 %
Digital delay	7.6mA	10%
DEM	6.4mA	8%
TOTAL	78 mA	100 %

The layout of the z^{-1} bandpass ΣΔ modulator is shown in Fig. 54, including analog and digital circuitry. The clock was placed at the middle of the chip in order to be able to evenly round the clock signal to all necessary components. Since the system contains digital circuits such as DAC, DFFs, clock and DEM, a guard ring around the filter and the analog side of the quantizer is used to isolate the analog circuit from digital part to reduce the noise.

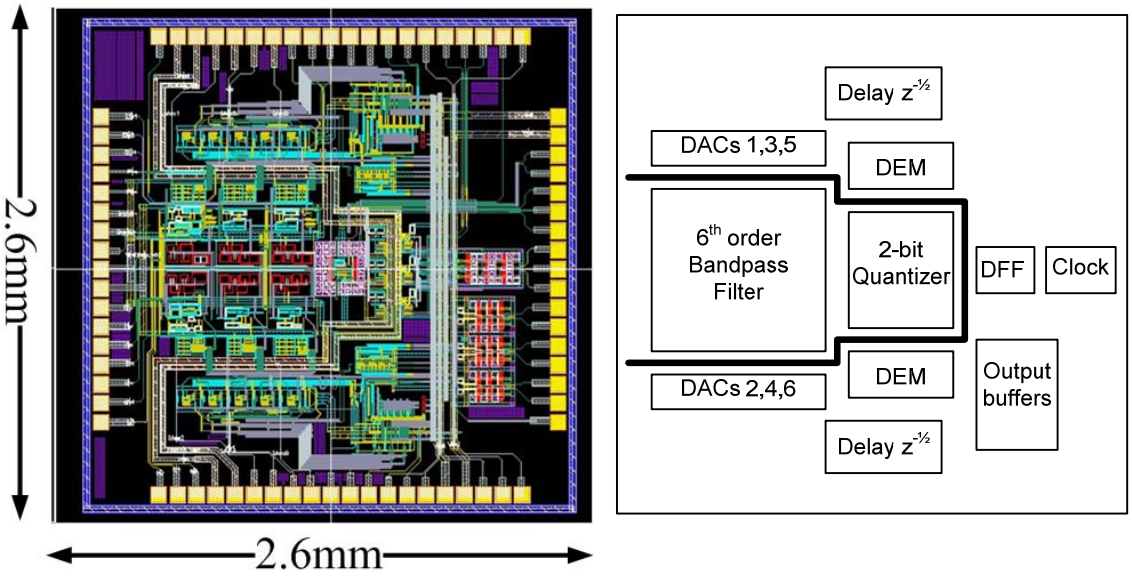


Figure 54 Layout of the 6th order CT-BP ΣΔ modulator

A summary of the performance of the ΣΔ Modulator is summarized in table 16. As shown in table 16 below, post-layout simulations demonstrate that the proposed architecture is expected to achieve more than 72.3dB of SNDR over a 14MHz bandwidth with moderate power consumption. The occupied area by the proposed ADC is 2.6mmX2.6um and it consumes 78mA from a 1.8V power supply. The ADC was fabricated in 0.18um CMOS technology thanks to TMSC sponsorship. The chip is back from fabrication currently under characterization.

Table 16 Summary of performance of ΣΔ modulator

Parameters	Post Layout results
Center Frequency	200Mz
Bandwidth	14MHz
Sampling Frequency	800MHz
SNDR (1MHz BW)	78.1dB
Power consumption	107mW
Supply voltage	1.8V
Technology	TSMC 0.18um CMOS
Active Area	6.7mm^2

Table 17 shows a performance comparison between different designs and this work. A direct comparison may be not accurate because there are no other works at this frequency. However, it still demonstrates superior performance of the work. This design operates at 1.8 V power supply with 107 mW power consumption. The power consumption of the work is very small compared to Raghavan's design that is fabricated

by advanced technology. Also we expect that the work can achieve more than 75 dB of SNDR, which is comparable to other continuous-time modulators at high frequency.

Table 17 Comparison of ADC performance

Ref	Type	Signal freq (MHz)	Clock Freq (MHz)	SNR (dB) @BW=1MHz	BW (MHz)	Power (mW)	Technology
This work	6^{th} CT BPΣΔ	200	800	78dB	14	107	0.18um CMOS
[22]	2nd CT BPΣΔ 4bit	2	48	64 dB	1	2.2	0.18um CMOS
[25]	4th CT BPΣΔ	125	400	64 dB	0.9	302	0.35um CMOS
[41]	4th CT BPΣΔ	950	3800	59 dB	1	75	0.25um BiCMOS
[42]	4th CT BPΣΔ + Mixer	100	80	42 dB (3.8M)	3.8	56	0.35um CMOS
[43]	8th CT BPΣΔ	44	264	77 dB	8.5	375	0.18um CMOS
[44]	4th CT BPΣΔ 4bit	75	480	65 dB	20	--	0.18um CMOS
[45]	4th DT BPΣΔ 4path	70	280	72 dB	4.4	480	0.35um CMOS
[46]	2nd CT BPΣΔ SAW	47.3	189.2	57 dB	0.2	30	0.35um CMOS

6. DIGITAL BASED CALIBRATION TECHNIQUE

6.1 Introduction

A major issue found in CTBP $\Sigma\Delta$ modulators is the lack of accuracy due to process, voltage and temperature (PVT) changes that may lead to over 25% variations on the time constants [24], [41], [46]-[49]. To alleviate this problem, the master-slave tuning techniques have been successfully used in continuous-time filters. This approach, however, has been accompanied by additional calibration schemes since tuning the loop filter is not enough to guarantee the best operation of the entire ADC loop [24], [42]-[43]. The optimally-tuned ADC requires corrections for the filter's center frequency deviations, excess loop delays and deviations in DAC coefficients. These issues are partially alleviated by optimizing the architecture using double delay resonators and feedforward techniques [49]. Another approach measures in the digital domain the notch-shaped noise coming out of the ADC [42]; this approach is however affected by the power of the incoming out-of band information in on-line calibration schemes but it is an interesting approach for off-line calibration. Optimization of individual building blocks and use of programmable delay lines for the optimization of the loop delay and reconfigurable filter-oscillator system for notch tuning were also reported in [43].

The online software-based loop calibration technique introduced in this work is intended for the optimization of the noise transfer function in CT BP ΣΔ modulators. The proposed approach measures the noise transfer function in digital domain using two auxiliary and non-critical test tones; based on the response of the loop to the strategically applied tones, the loop parameters are sequentially adjusted until the noise transfer function presents its best possible performance. The main concept introduced uses two out of band test tones suitable for online calibration.

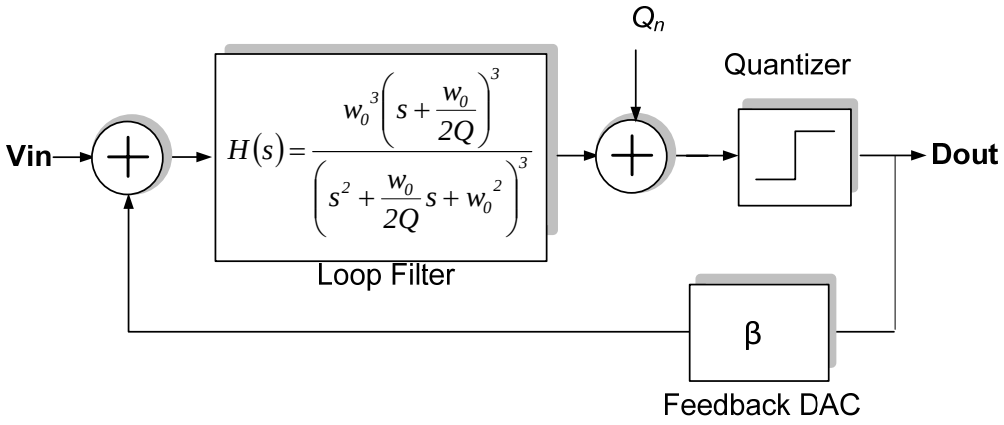


Figure 55 Simplified model for the 6th order CT BP ΣΔ modulator

Fig. 55 shows the simplified block diagram of a typical CT BP ΣΔ modulator, which provides a digital output D_{out} given by

$$D_{out} = STF * V_{in} + NTF * Q_n \tag{6.1}$$

where Vin is the analog input signal, Q_n is the quantization noise due to quantizer limited resolution, *STF* is the signal transfer unction and *NTF* is the noise transfer

function. As explained in [24], the *STF* and *NTF* can be obtained by looking at the linear transfer function from V_{in} to D_{out} and from Q_n to D_{out} respectively. Assuming 6th order modulator with a unity gain quantizer, it can be shown that the *STF* and the quantization *NTF* can be approximated as

$$STF(s) \approx \frac{\omega_o{}^3\left(s+\frac{\omega_o}{2Q}\right)^3}{\left(s^2+\frac{\omega_o}{Q}s+\omega_o{}^2\right)^3+\left(\omega_o{}^3\beta\right)\left(s+\frac{\omega_o}{2Q}\right)^3} \tag{6.2}$$

$$NTF(s) \approx \frac{\left(s^2+\frac{\omega_o}{Q}s+\omega_o{}^2\right)^3}{\left(s^2+\frac{\omega_o}{Q}s+\omega_o{}^2\right)^3+\left(\omega_o{}^3\beta\right)\left(s+\frac{\omega_o}{2Q}\right)^3} \tag{6.3}$$

where β is the gain of the feedback DAC; ω_0 and Q are filter's center frequency and finite quality factor, respectively. At the resonant frequency ($\omega=\omega_0$) and assuming high Q sections (Q>10 for example), these equations simplify to

$$STF(j\omega_o) = \frac{\left(j+\frac{1}{2Q}\right)^3}{-\left(\frac{1}{Q}\right)^3+(\beta)\left(j+\frac{1}{2Q}\right)^3} \cong \frac{1}{\beta} \tag{6.4}$$

$$NTF(j\omega_o) = \frac{-1}{-1+(\beta)\left(jQ+\frac{1}{2}\right)^3} \cong \frac{1}{\beta Q^3} \tag{6.5}$$

Assuming ideal components the Q factor can be made very large, and the magnitude of the NTF evaluated at the resonant frequency ($s=j\omega_0$) becomes very small, which leads to an excellent SQNR performance around the resonant frequency. However, ω_0 in continuous-time filters typically changes by ± 20% over PVT variations. Also, a finite gain of more than 30dB in single stage amplifiers and parasitic poles in high-gain amplifiers will limit the Q factor of high-frequency filters, which reduces the ADC's SQNR because resonant frequency the shape of the NTF given in (6.3) strongly depends on Q and the feedback DACs (β). In addition, the excess loop delay between the quantizer sampling time and the time when a change in the output bit is seen at the feedback point in the filter will cause SNR degradation and stability issues. Excess loop delay has to be limited to no more than 10% of the clock period in order not to degrade the SQNR [48]. Also, it has been reported in previous publications that 0.1 % and 0.4% RMS clock jitter reduces ADC's SQNR by over 1 dB and 10 dB, respectively. Fortunately, state of the art clock generators using on-chip PLLs can reduce the RMS clock jitter to the range of 1 ps, enabling the use of clocks in the range of 1 GHz.

The global calibration strategy described in the following section takes into account all PVT variations, DAC coefficient accuracy and excess loop delay to effectively optimize ADC's loop performance. The proposed strategy is not able to correct DAC non-linearities which may require the use of randomization techniques such as dynamic element matching [40].

6.2 Proposed calibration technique

The proposed loop calibration approach relies on a software-based platform instead of power hungry and inaccurate analog circuitry. The system level implementation of the proposed digital tuning scheme for the CT BP ΣΔ ADC is shown in Fig. 56. In addition to the in-band analog input signal, two out-of-band test tones equally spaced around the center frequency (f_0) are applied at the input of the quantizer to emulate a systematic and testable in-band quantization noise. Since the test tones are applied at the output of the loop, its noise is shaped by loop transfer function and the auxiliary circuitry has very little effect on the dynamics of the loop. The quantizer output digital bit stream is then processed by the digital signal processor (DSP), and the power of the test tone is then measured in the digital domain using the Fast Fourier transform (FFT). The estimated power of the test tone is used in an adaptive Least Mean Square (LMS) algorithm that controls several parameters with the aim of minimizing the power of the measured test tone and thus maximizing the rejection to quantization noise. The LMS algorithm generates the digital control signals to tune loop's notch frequency by controlling a bank of capacitors used for the realization of the bandpass filter. Once the notch frequency of the NTF is set at the desired frequency, the DAC coefficients and excess loop delay are then adjusted with the same aim: power minimization of the test tone to reach the best possible signal to quantization noise ratio.

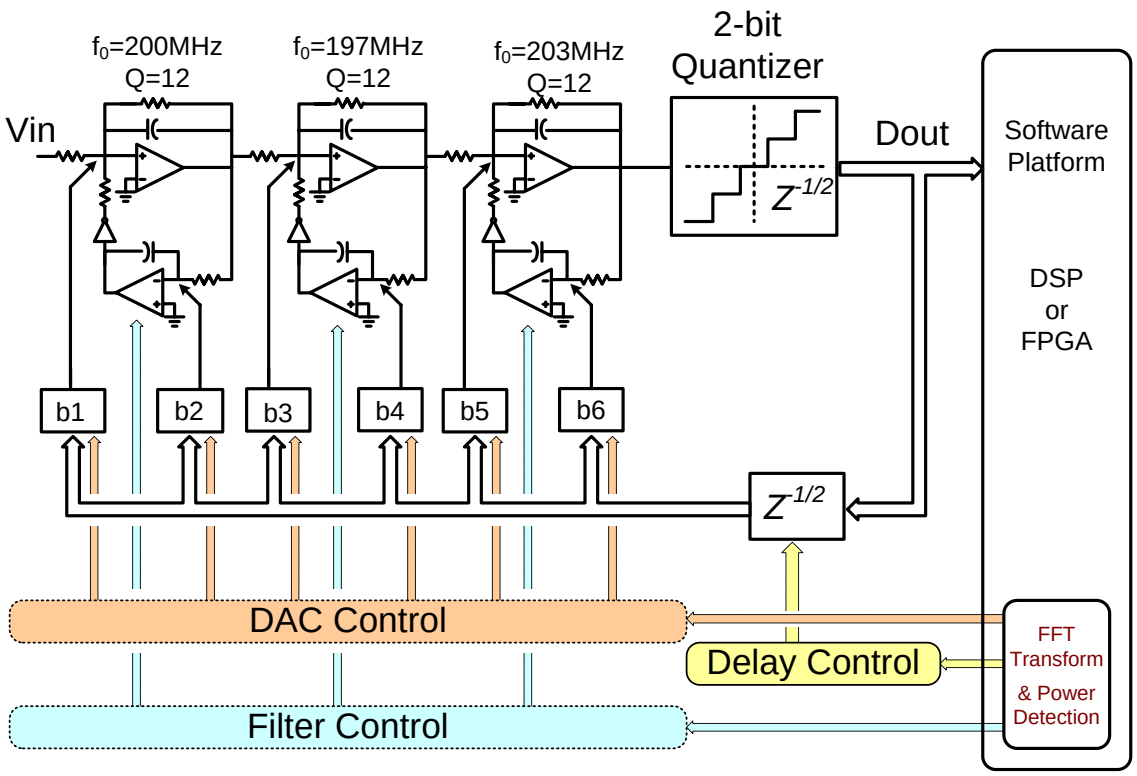


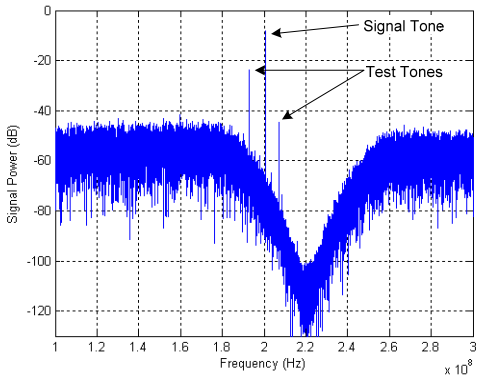
Figure 56System level implementation of the proposed digital calibration scheme

The algorithm for the digital tuning scheme is described by the following steps: i) Inject an input signal such that the loop operates properly; ii) Inject test tones signals around the desired frequency (f_0) at the quantizer input; iii) Find the frequency component of the test tone and store their value in digital format; iv) By means of an LMS algorithm a digital control tuning signal is computed based on the difference between the stored and the new estimated power value of the detected test tone; v) The parameters that control f_0 are tuned first; vi) Iterate between (iii) – (v) until the power of the measured test tone is minimized. Once the frequency of the NTF notch is tuned, the algorithm tunes the DAC coefficients and a programmable delay element, if

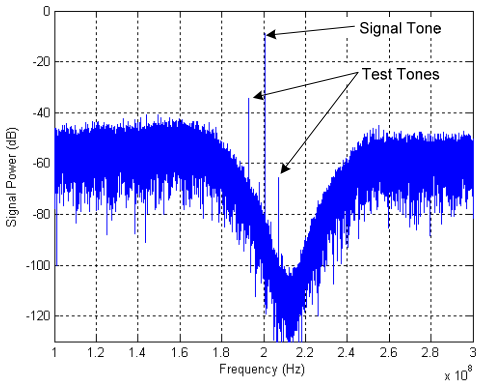
required, until the power of the detected test tone is minimized. The algorithm ensures that at the end of the process the critical loop parameters are tuned for the best SQNR.

6.3 Simulation results

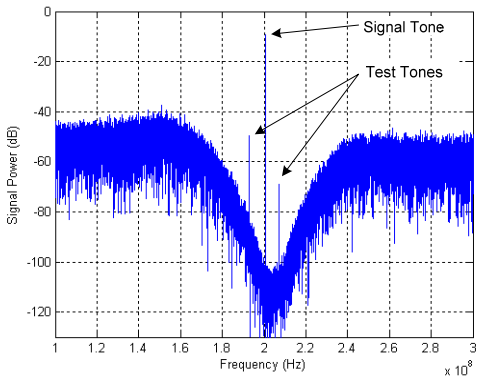
The magnitude of the test tones is not critical; it can be very small but it must be well above the noise floor to be easily detected. Fig. 57a shows the response of the un-calibrated $f_s/4$ 6^{th} order 200MHz ADC with the input signal and two test tones. The input signal is applied at the input of the ADC at 200MHz; the calibration tones are applied at the input of the quantizer at the out-of-band frequencies of 193MHz and 207MHz and used for the calibration of the NTF. Over 20% variations on the loop parameters were intentionally introduced; this results in a notch's frequency around 220 MHz instead of 200 MHz. After several iterations using the aforementioned algorithm, the notch frequency is tuned to the desired value by just monitoring the power of the test tone set at 200 MHz as shown in Fig. 57b-c and adjusting the bank of capacitors used in the loop filter for that purpose. Fig. 57d shows the ADC spectrum after calibration. The algorithm stops when the power of the tones at quantizer input are equal and are at its minimum value; e.g. -61 dB at the output while the power of the test tone applied to the quantizer input is -10 dB. Once the loop's notch frequency is tuned, there is room for additional (usually 3-9 dB) SQNR improvement by fine tuning DAC coefficients and excess loop delay.



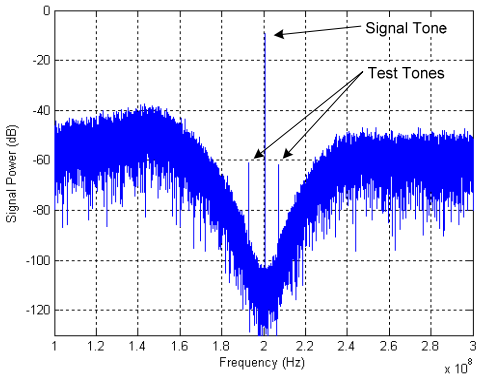
a) Uncalibrated ADC. SNR = 34dB



b) Calibration after 3 Iterations. SNR = 48dB



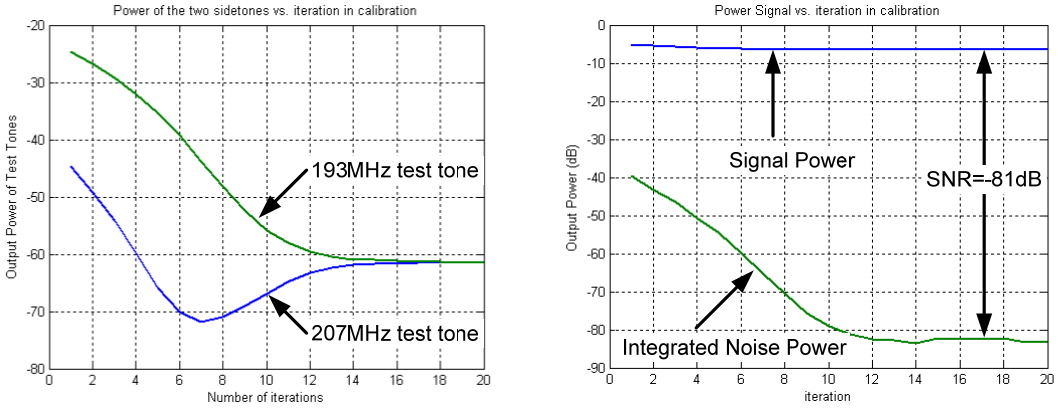
c) Calibration after 6 Iterations. SNR = 60dB



d) Calibration after 20 Iterations. SNR = 82dB

Figure 57Output spectrum of the 6th order ΣΔ modulator with digital calibration scheme

Since the loop tuning approach relies on power estimation in software and on the well controlled frequency of the test tone, the algorithm is quite robust and ensures the optimization of the most critical parameter in the bandpass ADCs: the noise transfer function. Fig. 58 on the left shows how the power of the two test tones changes equalizes as the calibration takes place. At the same time, the power of the in-band quantization noise is reduced while the signal power remains unchanged.



a) Power of test tones after calibration: -61dB **b) Power of in-band noise after calibration:-85dB**

Figure 58 Power of the test tones and SNR simulations vs. the number of iterations of the calibration scheme for 20% PVT variations on ADC

6.4 Digital calibration scheme conclusions

A software-based calibration scheme intended for continuous-time bandpass sigma-delta modulators has been proposed. The technique requires two test tones at around the desired center frequency; while tone's power is not critical, it is desirable to limit its power to 10 dB below the maximum input power tolerated by the ADC to ensure that the quantizer is not saturated. The proposed technique requires extensive digital computation since the power of the calibration tone must be extracted through FFT, but this is not a major drawback since digital processing is well suited for current and future deep-submicron technologies wherein digital circuitry is becoming faster and cheaper.

7. CONCLUSIONS AND FUTURE WORK

In this work, a novel linearization technique for a Low-Noise Amplifier (LNA) targeted for UWB applications was presented. Post-layout Simulations show NF of 6.3dB, peak S21 of 6.1dB, and peak IIP3 are 21.3dBm, respectively. The power consumption of the LNA is 5.8mA from 2V.

The design of a CMOS 6^{th} order CT-BP-ΣΔ modulator running at 800 MHz for High-IF conversion of 14MHz bandwidth signals at 200 MHz with 78dB of SNDR was presented. A novel transconductance amplifier has been developed to achieve high linearity and high dynamic range at high frequencies. The effects of the non-linearities of the output impedance were discussed and possible solutions were given.

A 2-bit Quantizer with offset cancellation is also presented. Post-layout simulations of the sixth-order modulator implemented using 0.18 um TSMC standard analog CMOS technology were presented demonstrating an SNDR of 78 dB (~13 bit) performance over a 10MHz bandwidth. The modulator's static power consumption is 107mW from supply power of ± 0.9V.

Finally, a calibration technique for Noise Transfer Function (NTF) optimization of the CT BP $\Sigma\Delta$ modulators was presented. The proposed technique employed a two test tones applied at the input of the quantizer to evaluate the noise transfer function of the Analog-to-Digital Converter using the capabilities of the Digital Signal Processing.

REFERENCES

[1] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, UK: Cambridge University Press, 1998.

[2] J. Mitola III and G. Q. Maguire, Jr., "Cognitive radio: Making software radios more personal," Royal Institute Of Technology, Stockholm, *IEEE Personal Communications*, Aug. 1999.

[3] H. Zhan, et.al., "Multi-band (1-6GHz), sampled, sliding-IF receiver with discrete-time filtering in 90nm digital CMOS process," *Proceedings of the VLSI Symposium conference*, Honolulu, HI, 15-17 June, 2006, pp. 230-231.

[4] N. Poobuapheun, C. Wei-Hung, Z. Boos and A.M. Niknejad, "A 1.5-V 0.7–2.5-GHz CMOS quadrature demodulator for multiband direct-conversion receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 1669-1677, Aug. 2007.

[5] R. Bagheri, A. Mirzaei, S. Chehrazi, M. E. Heidari, M. Lee, M. Mikhemar, W. Tang and A.Abidi, "An 800-MHz-6-MHz software-defined wireless receiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2860-2876, December 2006.

[6] C. Wei-Hung, L. Gang, Z. Boos and A.M. Niknejad, "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *Radio Frequency Integrated Circuits (RFIC) Symposium*, Honolulu, HI, 2007 IEEE, June 2007, pp. 61-64.

[7] A. Valdes-Garcia, C. Mishra, F. Bahmani, J. Silva-Martinez and E. Sánchez-Sinencio, "An 11-band 3.4 to 10.3 GHz MB-OFDM UWB receiver in 0.25um SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 935-948, April 2007.

[8] S. Chandrasekaran and W.C. Black Jr, "Sub-sampling sigma-delta modulator for baseband processing", *Proc. IEEE Custom Integrated Circuits Conf.*, Honolulu, HI, May 2002, pp.195-198.

[9] P.H. Gailus, W.J. Turney and F.R. Yester.Jr., "Method and arrangement for a sigma-delta converter for bandpass signals", U.S. Pat. 4857928, Aug. 15, 1989.

[10] J. Zhan, and S. Taylor, "A 5 GHz resistive-feedback CMOS LNA for low-cost multi-standard application", *IEEE International Solid State Circuit Conference (ISSCC)*, San Francisco, CA, 2006, p. 231-231.

[11] S. Ganesan, E. Sánchez-Sinencio and J. Silva-Martinez, "A Highly linear low loise amplifier," *IEEE Transactions on Microwave Theory and Techniques*. vol. 54, pp. 4079–4085, Dec. 2006.

[12] E. M. Cherry and D. E. Hooper, "The design of wide-band transistor feedback amplifiers," *Proceedings IEE*, vol. 110, pp. 375-389, February 1963.

[13] S. Chehrazi, A. Mirzalei, R. Bagheri and A. Abidi, "A 6.5 GHz wideband CMOS low noise amplifier for multi-band use", *Proc. IEEE Custom Integrated Circuits Conf.*, Boston, MA, Sep. 2005. pp. 801–804.

[14] P. H. Woerlee, M.J. Knitel, R. V. Langevelde, D. B. M. Klaasen, L. F. Tiemeijer, A. J. Scholten, and A. T. A. Z. Duijnhoven, "RF-CMOS performance trends," *IEEE Transactions on Electron Devices*, vol. 48, pp.1776-1782, August 2001.

[15] B. Toole, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs", *IEEE Transactions on Circuits and Systems*, vol. 51, pp. 319-328, February 2004.

[16] J. A. E. P van Engelen, R. J. van de Plassche, E. Stikvoort and A. G. Venes, "A sixth-order continuous-time bandpass sigma-delta modulator for digital radio IF", *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1573-1764, December 1999.

[17] C. I. Lao, H. L. Leong, K. F. Au, K. H. M and S. P. U, "A 10.7-MHz bandpass sigma-delta modulator using double-delay single-opamp SC resonator with doublesampling", *IEEE Circuit and System*, vol. 1, pp. 1061-1064, May 2003.

[18] V. Comino and A. C. Lu, " A bandpass sigma-delta modulator IC with digital branch-mismatch correction", *IEEE Proceeding on Custom Integrated Circuits*, pp. 129-132, May 1999.

[19] F. Henkel, U. Langmann, A. Hanke, S. Heinen and E. Wagner, " A 1-MHz-bandwidth second-order continuous-time quadrature bandpass sigma-delta modulator for low-IF radio receivers", *IEEE J. Solid-State Circuit*, vol. 37, no. 12, pp. 1628-1635, December 2002.

[20] R. Schreier and G. Temes, *Understanding Delta-Sigma Data Converters*, Hobken, NJ: Wiley-IEEE Press, 2005.

[21] P. Cusinato, D. Tonietto, F. Stefani and A. Baschirotto, "A 3.3-V CMOS 10.7MHz sixth order bandpass $\Sigma\Delta$ modulator with 74-dB dynamic range", *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 629-638, April 2001.

[22] P. C. Maulik, M. S. Chadha, W. L. Lee and P. J. Crawley, "A 16-bit 250-KHz delta-sigma modulator and decimation filter", *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp 458-467, April 2000.

[23] T. Georgantas, S. Bouras, Y. Panananos and D. Dervenis, "Switched-current sigma-delta modulator for baseband channel application", *IEEE International Symposium on Circuits and Systems*, Geneva, Vol. 4, May 2000, pp. 413-416.

[24] J. A. Cherry and W. M. Snelgrove, *Continuous–time delta–sigma modulators for high–speed A/D conversion: theory, practice and fundamental performance limits*. 1st Ed., Norwell, MA: Kluwer Academic Publishers, 2000.

[25] X. Liu, "Design of a 125MHz tunable continuous-time bandpass SD modulator for wireless IF applications," Ph.D. dissertation, EE Texas A&M University, College Station, Texas, September 2004.

[26] V. Tarokh and H. Jafarkhani, "On reducing the peak to average power ratio in multicarrier communications," *IEEE Trans. Commun.*, vol. 48, no. 1, pp. 37–44, Jan. 2000.

[27] Y. Tsividis, "Continuous-time filters in telecommunication chips," *IEEE Commun. Mag.*, vol. 163, pp. 132–137, 2001.

[28] J. Silva-Martínez, M. Steyaert, and W. Sansen, *High Performance CMOS Continuous-Time Filters*. Norwell, MA: Kluwer, 1993.

[29] R. Schaumann and V. Valkenburg, *Design of Analog Filters*. New York: Oxford, 2001.

[30] D. K. Shaeffer, A. R. Shahani, S. S. Mohan, H. Samavati, H. R. Rategh, M. del Mar Hershenson, X. Min, C. P. Yue, D. J. Eddleman, and T. H. Lee, "A 115-mW, 0.5-_m CMOS GPS receiver with wide dynamic range active filters," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2219–2231, Dec. 1998.

[31] G. Bollati, S. Marchese, M. Demicheli, and R. Castello, “An eighth-order CMOS low-pass filter with 30-120-MHz tuning range and programmable boost,” *IEEE J. Solid-State Circuits*, vol. 36, pp. 1056–1066, Jul. 2001.

[32] J. Silva-Martinez, J. Adut, J. Rocha-Perez, J. M. Robinson, and S. Rokhsaz, “A 60-mW 200-MHz continuous-time seventh-order linear phase filter with on-chip automatic tuning system,” *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 216–225, Feb. 2003.

[33] A. A. Emira and E. Sanchez-Sinencio, “A pseudo differential complex filter for Bluetooth with frequency tuning,” *IEEE Trans. Circuits and Syst. II*, vol. 50, pp. 742–754, Oct. 2003.

[34] Y. W. Choi and H. C. Luong, “A high-Q and wide-dynamic-range 70-MHz CMOS bandpass filter for wireless receivers,” *IEEE Trans. Circuits Syst. II*, Analog Digit. Signal Process., vol. 48, no. 5, pp. 433–440, May 2001.

[35] A. Lewinski and J. Silva-Martinez, “OTA linearity enhancement technique for high frequency applications with IM3 below -65 dB,” *IEEE Trans. Circuits Syst. II*, Exp. Briefs, vol. 51, no. 10, pp. 542–548, Oct. 2004.

[36] A. Lewinski and J. Silva-Martinez, “A 30-MHz fifth-order elliptic low-pass CMOS filter with 65-dB spurious-free dynamic range,” *IEEE Transactions on Circuits and Systems*, vol. 54, pp. 469-480, March 2007.

[37] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 2001.

[38] R. Schaumann, M. S. Ghausi, and K. R. Laker, *Design of analog filters*, New York, NY: Prentice Hall, 1990.

[39] B. Razavi, *Principles of Data Conversion System Design*, New York, NY: IEEE Press, 1995.

[40] B. K. Thandri, “Design of RF/IF analog to digital converters for software radio communication receivers,” Ph.D. dissertation, Texas A&M University, College Station, Texas, May 2006.

[41] B. K. Thandri and J. Silva-Martinez, “A 63 dB 75 mW bandpass ΣΔ RF ADC at 950 MHz using 3.8 GHz clock in 0.25 μm SiGe BiCMOS technology”, *IEEE Journal of Solid-State Circuits*, vol. 42, pp.269-279, Feb. 2007.

[42] H. Huang and E. F. K. Lee, “A 1.2V direct background digital tuned continuous-time bandpass sigma-delta modulator”, *Proc. of 27th European Solid-State Circuits Conference,(ESSCIRC 2001)*, Villach, Austria, pp. 526-529, Sep 2001.

[43] R. Schreier, A. Nazmy, H. Shibata, D. Paterson, S. Rose, I. Mehr, and Q. Lu, “A 375-mW quadrature bandpass ΣΔ ADC with 8.5-MHz BW and 90-dB DR at 44 MHz,” *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 2632-2640, Dec. 2006.

[44] R. Maurino and P. Mole, “A 200-MHz IF 11-bit fourth-order bandpass ΣΔ ADC in SiGe,” *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 959-2640, July 2000.

[45] G. Bernardinis, F. Borghetti, V. Ferragina, A. Fornasari, U. Gatti, P. Malcovati and F. Maloberti, “A wide-band 280-MHz four-path time-interleaved bandpass sigma-delta modulator,” *IEEE Trans. Circuits and Systems*, vol. 53, pp. 1423–1432, July 2006.

[46] R. Yu, P. Xu, “Bandpass sigma-delta modulator employing SAW resonator as loop filter,” *IEEE Trans. Circuits and Systems*, vol. 54, pp. 723–735, April 2007.

[47] T. Chavatzis, E. Gagnon, M. Repeta and S. P. Voinigescu, “A low noise 40 Gs/s continuous time bandpass ΣΔ ADC centered at 2 GHz for direct sampling receivers”, *IEEE Journal of Solid-State Circuits*, vol. 42, pp.1065-1075, May 2007.

[48] J. Silva-Martinez, M. Steyaert and W. Sansen, “A 10.7-MHz 68-dB SNR CMOS continuous-time filter with on-chip automatic tuning,” *IEEE Journal of Solid-State Circuits*, vol. 27, pp.1843-1853, Dec. 1992.

[49] A. Rosu, B. Dong and M. Ismail, “Putting the “flex” in flexible mobile wireless radios,” *IEEE Circuits and Devices Magazine*, pp. 24-30, Nov./Dec. 2006.

VITA

Jose Fabian Silva Rivas was born in Puebla, Mexico. He received his B.S. degree in electrical engineering from Texas A&M University in College Station, Texas, in 2005. From 2006 to the present, he has been a graduate student in the Department of Electrical Engineering, Analog and Mixed-Signal Center at Texas A&M University working towards his Master's degree. From March 2008 to September 2008, he was with Central Engineering group, Broadcom Co., Irvine, California, as an intern design engineer, working on 40nm front-end for next generation satellite receivers. His research interests are in analog circuit design, including high frequency filter and high speed wideband continuous-time sigma-delta ADCs. He can be reached through the Department of Electrical Engineering at Texas A&M University, College Station, Texas 77843-3128, USA. Email: fatosilva@gmail.com