EFFECTS OF LOW TEMPERATURE ANNEALING

ON

THE ADHESION OF ELECTROLESS PLATED COPPER THIN FILMS ON TiN DEPOSITED SILICON INTEGRATED CIRCUIT SUBSTRATES

by

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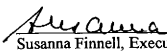

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ABSTRACT

The semiconductor manufacturing industry is increasingly using copper to design and fabricate faster and smaller integrated circuits. Despite copper's electrical advantages, few ways exist to deposit it uniformly into the steep vias and trenches present on modern IC substrates. Electroless deposition, which plates a seed layer of copper onto a substrate in a liquid bath without the use of a power source, is a reliable method of depositing copper. Effects of low temperature annealing on the adhesion of copper thin films deposited using electroless plating were investigated: electroless copper deposition was performed on silicon substrates onto which a thin barrier and adhesion layer of titanium nitride (TiN) had been previously deposited. The resulting samples were then annealed at a low temperature, and the adhesion of the copper film to the substrate was evaluated using a tape test. Results indicate that low temperature annealing improves the adhesion of the electroless plated copper thin film to the substrate. Since good adhesion is a fundamental requirement of an effective metallization method, this work paves the way for future integration of electroless copper deposition into modern semiconductor manufacturing facilities.

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I. INTRODUCTION

A. *Role of Interconnects in Determining Circuit Speed and Density*

In modern integrated circuits (ICs), patterned layers of conductive thin films are used to connect devices in the circuit and to connect the circuit to the outside world. Interconnects are the fine lines of a metal conductor which electrically connect individual devices.

Properties of interconnects govern the performance of modern integrated circuits. For all but the shortest interconnect lines, signal propagation delay in the interconnect lines is the governing factor in the operating speed of modern integrated circuits [1]. (Transistor switching speed also plays a part in circuit operating speed, but improvements in device technology have reduced transistor switching times far below that required for a signal to travel through even the shortest of interconnect lines.)

Signal propagation delay in an interconnect line is dictated by the *RC* time constant of the line, which governs how fast the line can be switched between binary logic levels. This *RC* time constant varies as $\frac{R_s^2 L^2}{d_{ox}}$, where R_s is the ohm-per-square (sheet) resistance of the interconnect material, L is the length of the line, and d_{ox} is the dielectric thickness separating adjacent lines [2].

Circuit designers have sought to reduce signal propagation delay in ICs while simultaneously to design as small of a circuit as possible. To minimize circuit size,

chip designers reduce both *L* and transistor sizes. A reduction in areas of transistor terminals necessitates corresponding reductions in the cross-sectional area of interconnect lines. Current density is the product of an electric current and the cross-sectional area of the line in which it travels: if the cross-sectional area of a line is scaled down at a rate greater than the rate at which the current in the line is reduced, the current density in the line increases.

B. Electromigration Issues

Electromigration is the mass transfer of metal atoms in an interconnect line due to stress conditions of high temperature and high current density. It is caused by the transfer of kinetic energy from electrons to metal atoms [1, 2]. The type of interconnect material used governs the maximum current density that a line can tolerate without experiencing electromigration. At a typical circuit operating temperature of 100°C, copper can tolerate a maximum current density several orders of magnitude greater than aluminum [1].

Reliability failures caused by electromigration-induced interconnect failures in aluminum-based ICs have motivated circuit manufacturers to choose copper over aluminum as an interconnect material. A bonus effect of the choice of copper over aluminum is copper's lower resistivity (for thin film Cu, $\rho \approx 2.0$ $\mu\Omega$-cm; for thin film Al, $\rho = 2.7\text{-}3.0$ $\mu\Omega$-cm [2, 3]). The change to copper allows manufacturers to take

advantage of copper's higher tolerance for electromigration as well as its lower resistivity, resulting in an even further decrease of the *RC* time constant [1].

C. Diffusion Barrier Materials

While copper's electrical properties are superior to those of aluminum, the use of copper introduces difficulties in the manufacturing process that have not been previously encountered with aluminum. One problem is copper's high diffusivity in silicon and silicon dioxide (SiO_2). Diffusion of copper into silicon is undesirable because the presence of copper atoms in silicon devices shortens the lifetime of carriers, which results in a greater leakage current and a lower device reliability in metal-oxide semiconductor (MOS) transistors [4]. The diffusion of copper atoms into SiO_2 causes increased *RC* delay due to an effective decrease in d_{ox}, the distance between lines. In extreme cases of diffusion, the diffused copper atoms form a unwanted short circuit between adjacent interconnects, which results in circuit failure.

The use of diffusion barrier materials in the copper deposition process eliminates the diffusion of copper into silicon and SiO_2. In the interconnect fabrication process, immediately after trenches and via openings are patterned in the dielectric layer, a thin layer of the diffusion barrier metal is deposited. The copper is then deposited and patterned, and another thin layer of the barrier metal is deposited, effectively encapsulating the copper inside the barrier metal, preventing the diffusion of copper atoms into the surrounding material [2].

In addition to preventing the diffusion of copper, the diffusion barrier layer promotes adhesion between copper and the surrounding dielectric material. The effects of various adhesion layer materials on the adhesion of copper are under much investigation. Adhesion is a fundamental requirement of an effective metallization scheme: metal must adhere to the silicon substrate and to the walls of the dielectric that defines the window through which the metal will make contact down to the substrate or to other interconnect lines [2].

Diffusion barrier metals currently used to contain copper and promote copper adhesion include titanium, titanium nitride, tantalum, tantalum nitride, silicon nitride, and silicon carbide. Titanium nitride (TiN) was chosen for this study because it has been shown to be an effective diffusion barrier material [1, 3, 5]. Its chief advantage as an adhesion layer is its ability to reduce SiO_2 to form interfacial bonds between TiN and SiO_2, which promote adhesion and stability [2].

D. Limitations of Existing Copper Deposition Methods

The principal disadvantage to replacing aluminum metallization methods with copper-based methods is the inadequacies of existing processes with which to process copper. Aluminum, because of its straightforward deposition process, has been used for decades to fabricate interconnects. Because copper's deposition processes are less developed, manufacturers have encountered difficulty in reliably depositing copper to create state-of-the-art interconnects.

To keep interconnect capacitance at a minimum, modern interconnect fabrication techniques deposit thick layers of dielectric between each successive horizontal layer of stacked copper interconnects. This thick dielectric must be selectively removed to create vias, or openings between adjacent metal layers into which additional metal will be deposited to make electrical connections between the layers. The aspect ratio of these vias – simply the ratio of the opening's height to its diameter – is large and increasing: current manufacturing processes require that void-free copper plugs be deposited into via openings with aspect ratios of greater than 4:1 [6].

When employed to deposit copper into such high-aspect ratio vias, conventional metallization methods perform poorly. Vacuum-based techniques, such as chemical vapor deposition (CVD) and physical vapor deposition (PVD), while able to deposit aluminum into vias of lower aspect ratios, are unable to deposit copper with satisfactory results. High-vacuum PVD sputtering methods provide nonuniform coverage of these vias. This is due to long mean free paths of the evaporant species, which result in low surface migration of the reactants [2], resulting in voids in the copper via plug. Previous research has found no reliable way to deposit a void-free copper plug into high-aspect ratio vias using conventional metallization methods [7].

Electroplating has been investigated as a technique to fill high-aspect ratio vias with copper. As employed in the semiconductor industry, electroplating consists of placing a wafer substrate into a liquid bath rich in ions of the metal to be deposited. A power source is connected to electrodes: one electrode is a ring clamped around

the wafer's edge; the other is fixed above the wafer in the bath. The resulting difference in voltage between the electrodes causes the metal ions to strike the wafer surface and lose their positive electric charge. As this process is continued, a uniform metal layer is deposited onto the wafer surface.

Electroplating requires the presence of a suitable conductive layer on the substrate surface for metal plating to begin. The diffusion barrier metal is thin and typically a poor conductor, resulting in a high resistance per unit length – and thus a large voltage drop from the electrode at the edge of the wafer to the wafer's center. Such a difference in voltage during electroplating causes the plating of a film with nonuniform thickness, which is undesirable. Instead, a thin seed layer, usually 10% or less of the total metal thickness desired in trenches and vias, is deposited onto the diffusion barrier metal prior to electroplating. Because of its higher conductivity, the seed layer causes uniform electroplated fill of vias and trenches.

The copper seed layer can be deposited using various methods. Despite their inability to reliably fill vias and trenches with copper, vacuum-based depositions do have limited usefulness in depositing thin copper seed layers. PVD and CVD processes for the deposition of copper seed layers have been developed, but they lack conformal coverage of the sides and bottoms of vias and trenches. These deposition methods are also slow and expensive.

E. Electroless copper deposition

Electroless copper deposition, also called "electroless plating", is an alternate method to deposit the copper seed layer needed for electroplating. Unlike electroplating, it requires no external voltage or current source (hence the term "electroless"); thus, it can be used to deposit a seed layer directly onto the diffusion barrier metal.

The electroless deposition process exhibits two advantages over using CVD or PVD to deposit a copper seed layer. First, because it is a liquid-based process, which features greater surface migration of reactants, the step coverage and uniformity of electroless plated seed films are superior to those deposited using vapor deposition techniques. Second, because it is performed at temperatures in the range of 30 to 60°C at atmospheric pressure, it is easier and cheaper to integrate into a manufacturing environment than high-temperature, high-vacuum systems.

II. ELECTROLESS COPPER DEPOSITION THEORY AND PROCESSES

A. Deposition Chemistry of Electroless Copper

The electroless deposition of copper atoms occurs when copper ions in aqueous solution are neutralized by electrons [6]. These electrons are supplied by a reduction reaction in the liquid phase:

$$HCOH + 2OH^- \rightarrow HCOO^- + \tfrac{1}{2}H_2 + H_2O + 2e^- \qquad (1)$$

The two electrons then neutralize one copper ion, resulting in its deposition:

$$Cu^{+2} + 2e^- \rightarrow Cu^0 \downarrow \qquad (2)$$

Thus the overall reaction, in which (1) and (2) occur simultaneously, is

$$4OH^- + 2H_2CO + Cu^{+2} \rightarrow Cu + 2H_2O + H_2 + 2HCOO^- \qquad (3)$$

This reaction is autocatalytic, that is, the presence of copper atoms on the substrate surface causes the plating of additional copper atoms to continue; however, if no copper or other catalyst is already present on the substrate surface, the reaction is difficult to initiate. (A TiN surface is conductive, but is not catalytic for electroless copper deposition [5].) To begin the deposition process, the surface is activated with palladium atoms prior to copper deposition. Palladium has been previously shown to initiate electroless deposition for many metals, including copper [3, 6, 8, 9].

B. Process Sequence To Deposit Electroless Copper

The electroless deposition of metals is a process employed in various industries for decades. In the electronics industry, its principal use has been to deposit nickel, gold, palladium, copper, or other metals onto fiberglass substrates to create electrical connections on printed wiring boards. Only during the last decade have researchers pursued the integration of electroless metal deposition into a VLSI or ULSI manufacturing process.

The following process is based on the M-Copper electroless plating process developed by MacDermid, Inc. MacDermid, a large supplier of industrial chemicals to manufacturers of printed wiring boards, provided the process and many of the chemicals used in this research.

1. Removal of surface oxide layer

TiN films oxidize to form a surface layer of TiO_2 when exposed to ambient air at room temperature. This TiO_2 layer must be removed in order to expose a pure TiN surface before further processing can be done [3]. Immersion in hydrofluoric acid (HF) solution can be used for this purpose, but since pure HF is a safety hazard and an extremely rapid etchant, a standard buffered oxide etch (BOE) solution is preferred. (A typical dilute BOE solution consists of 6.4% HF and 36.0% NH_4OH.)

2. Conditioning of surface

To promote the conformal coverage and adhesion of the electroless copper film, the substrate to be plated is then immersed in an aqueous solution of conditioner. The conditioner solution contains proprietary ingredients, typically surfactants, which help to control surface tension [5]. Other additives, including stabilizers and ductility promoters, may also be present in the conditioner solution.

3. Activation of surface

Deposition of electroless copper using wet activation is in wide use, with most research using the addition of $PdCl_2$ into the electroless plating solution [5, 8]. This results in nucleation of Pd atoms on the surface of the TiN layer, which continues only until the surface is covered with Pd atoms, since exposed areas of TiN are needed to continue the Pd nucleation. The electroless copper deposition process can then begin since the Pd atoms act as a catalyst to the copper deposition. Once the first layer of copper atoms covers the surface, the copper deposition process continues autocatalytically, as described above.

MacDermid's M-Copper electroless copper deposition process employs the use of a tin-palladium (SnPd) colloid to activate the surface on which deposition is desired. Activation occurs in two steps. First, the SnPd colloid nucleates on the TiN surface in an activator solution. Next, Sn atoms are stripped away from the Pd atoms in an accelerator solution, leaving exposed Pd atoms to act as an initial catalyst for electroless copper deposition.

4. Deposition of electroless copper

The last step in the deposition process deposits the actual copper atoms onto the activated substrate surface. Successful electroless copper deposition has been accomplished using both acid and alkaline copper deposition solutions; the copper deposition solution employed by MacDermid and in this research is alkaline.

III. ADHESION TESTS AND ANNEALING

A. *Qualitative Adhesion Tests*

While the electroless copper deposition process has been studied in depth for the past decade, few studies have been performed on the adhesion of electroless copper films to diffusion barrier materials such as TiN. This is somewhat puzzling, since copper in silicon ICs must be encapsulated in a diffusion barrier material. In addition, the fundamental requirement that a metallization film must adhere to the substrate motivates a study of the adhesion of electroless copper on diffusion barrier materials.

The simplest method of determining the adhesion of a thin film to a substrate is to apply a mechanical adhesion test. Such a test relates the adhesion of the film to the force applied or work done during the test [10]. Adhesion tests have been widely used to determine the adhesion strength of films, and several tests to determine the adhesion of a thin film to a substrate have been proposed. These include the peel test [11], pin-pull test, indentation test, scratch test, and others [12]. (These tests have been used to determine the adhesion of a variety of materials, not only thin films.) While many tests exist and have been employed to make qualitative comparisons of adhesion strengths, little quantitative data on thin film adhesion exists. The lack of quantifiable data on adhesion – and the lack of methods with which to determine it – is a problem that plagues the microelectronics industry. This is because most adhesion tests measure a combination of the stress required to delaminate a thin film

and the deformation stress that occurs following delamination [13], whereas the delamination stress alone is of primary interest.

In this research, the delamination stress of electroless plated copper films was qualitatively measured using the binary tape test, a type of peel test. (Use of the tape test to determine adhesion of a thin film to a substrate is common industry practice. This test was selected over other tests because of the lack of facilities to perform other tests in the Institute for Solid-State Electronics Laboratory at Texas A&M.) In the tape test, pressure-sensitive tape is applied to the surface of the film, then lifted away quickly. The presence of copper on the tape, or of any exposed area on the substrate, indicates poor adhesion of the film. This test is only a qualitative one, indicating only whether the film passes or fails, and provides no measure of the stress that causes the delamination.

B. Quantitative Adhesion Test

Researchers at Rice University and Texas Instruments have recently developed an electrostatic adhesion test, which allows the quantitative measurement of the delamination stress of thin films. This method uses electrostatic forces to generate high tensile stresses normal to the surface of the copper film, which allows a precise measurement of delamination stress of the film [10, 14].

As implemented by Rice and TI, the electrostatic adhesion test is accomplished using a structure similar to a parallel plate capacitor, with one plate being the thin film to be tested and the other mounted in a rigid ceramic probe

structure. To prevent arcing between the plates, this test is performed in a vacuum. As the voltage between the plates is increased, the thin film experiences an upward force due to electrostatic attraction to the probe. This force eventually becomes strong enough to delaminate the thin film from the substrate. When the film contacts the probe, a short circuit results between the probe and the substrate. The voltage at which this short circuit occurs is recorded, and the delamination stress can be determined from simple math [10, 13, 14]. This method allows allows for a wider measure of adhesion strength than other mechanical adhesion tests.

C. Use of Anneals to Improve Film Adhesion

It has been demonstrated that an anneal following metal deposition results in improved adhesion of the metal thin film to the substrate [2]. Both low temperature and high temperature anneals can be performed to improve the adhesion of a copper film to the underlying substrate: each employs a different mechanism to improve adhesion.

High temperature anneals are carried out at temperatures of several hundred degrees Celsius. The end result is that some copper atoms diffuse into – but not through – the diffusion barrier layer because of the high temperature. This promotes chemical bonding between the copper and barrier layers, resulting in improved adhesion between them.

High temperature anneals are advantageous because they form chemical bonds between films, but such anneals must be used judiciously. When silicon wafer

substrates are subjected to high-temperature conditions for any period of time, the properties of devices fabricated on the wafer during previous processing steps can be altered unfavorably and irreparably. Thus, lower-temperature anneals are used whenever possible.

Low temperature anneals do not result in chemical bonding between film and barrier layers, but do reduce the number of point defects and other irregularities in the deposited metal film. These defects are often responsible for poor adhesion of film to substrate [12]. It is also plausible that low temperature anneals purge the film of trapped gases evolved during the electroless copper deposition process.

IV. MOTIVATION AND PROBLEM STATEMENT

Copper metallization in integrated circuits has many advantages, but the implementation of processes to deposit copper has been difficult. Various copper deposition methods have been studied. The electroless deposition of copper seed layers followed by electroplated copper fill of vias and trenches is an especially attractive process because of its low cost, high reliability, and ease of integration into existing manufacturing flows.

Much research has been done on electroless metallization for multi-level interconnections on bare dielectrics [5, 6, 8], but little research has been performed specifically on the electroless deposition of copper onto barrier metals [3]. Because adhesion of a thin film to a substrate is the most important quality that a thin film should possess, it is important that the adhesion of electroless copper films to diffusion barrier materials be studied in more detail. Titanium nitride, one such barrier metal, has been extensively studied and is in widespread use in the manufacture of integrated circuits. However, a major obstacle to overcome in the use of electroless copper on TiN is the lack of adequate adhesion of copper to TiN. Extremely thin layers of copper have been shown to have adequate adhesion, but adhesion is weak for the thicknesses desired for seed layers (appoximately 300-600Å).

It has been found that electroless copper depositions exhibit high levels of compressive stress [15]. It is believed that a combination of high compressive stress and a non-chemical bond between the copper and TiN films causes a low

delamination stress of copper films above a certain thickness. It has been demonstrated that low temperature post-deposition annealing will significantly reduce the internal film stress of electroless copper deposited on silicon [15]. Based on this previous data, the hypothesis is that low-temperature annealing of electroless copper deposited on titanium nitride will also reduce the compressive stress and result in improved film adhesion.

The objective of this research is to investigate how the delamination stress of an electroless deposited copper thin film on a blanket TiN-deposited silicon substrate depends on the post-deposition annealing conditions applied to the substrate. Adhesion of the copper film to the substrate was characterized using the tape test, which gives a pass or fail result [11]. Factors affecting adhesion include the thickness of the deposited copper film, the annealing temperature, and the time of annealing.

V. EXPERIMENTAL PROCEDURE

A. Substrates and Supplies Used

The first step in this research was to develop an electroless copper deposition method suitable for semiconductor processing. The electroless copper deposition process in these experiments was adapted from MacDermid's M-Copper electroless copper deposition process for printed wiring boards. Chemicals used in this process contain proprietary additives which enhance the coverage, uniformity, and consistency of copper depositions.

Because the Institute for Solid-State Electronics Lab at Texas A&M lacked the capability to deposit uniform TiN films, 200mm-diameter silicon wafers were obtained from Advanced Micro Devices and Motorola and were used as the substrates in this experiment. The wafers were obtained with blanket TiN films already deposited. The thickness of the TiN film on both groups of wafers was 8kÅ.

Before experiments began, the electroless copper deposition process described below was performed on several substrates in order to fully understand the process sequence and much of the chemistry involved. After this initial learning stage, experiments were started.

B. Experiment Sequence

1. Preparation of solutions

The first step in plating an electroless copper film onto a substrate was to prepare the solutions required for plating. (Appendix A lists details of solution preparation.) The activator solution was disposed of and remixed once per three-month period; the copper plating solution was freshly mixed each day that plating was to be performed. All other solutions were disposed of and remixed approximately every two weeks.

Because it is necessary to perform predeposition steps at an elevated temperature, the beakers containing the BOE, conditioner, activator, and accelerator solutions were placed into a large pan filled with water. This arrangement was then placed on top of a hot plate. The water temperature was measured using a standard mercury thermometer, and was held at 46°C during processing. The predip and copper plating solutions were allowed to remain at room temperature, 26°C.

2. Preparation of sample for plating

A single 200mm wafer was removed from its box and was placed front-side-up on a lint-free disposable towel using plastic forceps. A diamond-tipped scribe was used to snap the wafer into 4 pieces of approximately equal shape and size. One such piece was picked up using plastic forceps, which would remain on the sample until the

conclusion of the plating process, and rinsed for 30 seconds under a steady stream of deionized (DI) water to remove particulates.

The sample was then immersed into the buffered oxide etch (BOE) solution and agitated for 60 seconds to remove any native TiO_2 growth. The sample was then removed from the solution and rinsed for 30 seconds under DI water.

3. Preparation of surface

The sample was then immersed into the conditioner solution and agitated for 5 minutes. The conditioner solution is a mildly alkaline solution designed to optimize copper film coverage and adhesion. The sample was then removed from the conditioner solution and rinsed for 30 seconds under DI water.

4. Activation of surface

The sample was then immersed into the predip solution and agitated for 60 seconds. The predip solution is mildly acidic and prepares the substrate surface for uniform adsorption of the activator. The sample was removed from the predip solution and was not rinsed.

The sample was then immersed into the activator solution and agitated for 5 minutes. The activator solution contained an SnPd colloid, which acted as a catalyst for the subsequent electroless copper deposition. The sample was then removed from the activator solution and rinsed for 30 seconds under DI water.

The sample was then immersed into the accelerator solution and agitated for 2 ½ minutes. The accelerator solution strips Sn atoms from the SnPd colloid, resulting in a high surface density of Pd atoms. The sample was then removed from the accelerate solution and rinsed for 30 seconds under DI water.

The sample was then immersed into the electroless copper plating solution and agitated for a variable length of time. In this research, deposition times ranged from 15 seconds to 5 minutes. The sample was then removed from the electroless plating solution and rinsed for 30 seconds under DI water.

The sample was then blown dry using compressed nitrogen gas. The plastic forceps were detached and the sample was placed inside a sealed Petri dish to prevent contamination or mechanical disturbances.

5. Measurement of film thickness

A square of approximately 20mm on a side was cut from the approximate center of each sample using a diamond-tipped scribe. Photolithography techniques were used to pattern and etch trenches through the plated copper film on this square sample. (Appendix B details photolithography and copper etch techniques used in this experiment.) A Sloan Dektak[3] diamond stylus profilometer was then used to measure the depth of the trench in the copper film. The depth of the trench indicates the approximate thickness of the copper film on the sample.

Copper film thicknesses ranged from 200Å to a nominal seed layer thickness of nearly 400Å. Further details can be found in Part VI.

6. Dicing of plated substrate sample into adhesion test samples

The remaining portion of each ¼-wafer sample was cut into rectangles of approximate dimensions 2cm × 1cm using a diamond-tipped scribe.

7. Pre-anneal tape test

To determine the adhesion of the copper film to the substrate prior to any anneal, a tape test was applied to each small adhesion test sample. Pre-anneal testing and post-anneal testing each used one-half of the available sample area. A 3-line × 3-line crosshatch pattern was scratched onto the surface using a diamond-tipped scribe in order to promote film delamination. A strip of 3M Scotch tape of length 2cm was peeled and cut from a roll of tape and placed on top of the sample to cover the scratched area. Air bubbles, if any, were smoothed out from under the tape. The tape was then pressed down onto the sample with the maximum possible hand pressure without cracking the sample. The edge of the tape overhanging the edge of the sample was then slowly peeled up until it was approximately perpendicular to the sample surface. The tape was then pulled away from the substrate as quickly as possible in an attempt to delaminate the copper film from the substrate.

The surfaces of the tape and of the sample were then investigated to determine if any copper had delaminated from the substrate and adhered to the tape. The presence of copper on the tape, or missing from the substrate, indicated a score of

"fail"on the pre-anneal tape test for that particular sample. The presence of copper that appeared to have delaminated from the lines in the scribed crosshatch pattern received a score of "marginal". A score of "pass" was recorded if no copper appeared on the tape.

The vast majority of samples exhibited failing scores for adhesion on the pre-anneal tape test. Complete results appear in Part VI.

8. Annealing of sample

Two annealing experiments were performed over the course of this investigation. At first, it was believed that varying the conditions of a rapid thermal anneal (RTA) in an annealing chamber would give a clear pass/fail signal in the post-anneal tape test as the anneal times and temperatures were varied. Preliminary RTA results were obtained on an AG Associates Heatpulse 210 in an ambient argon atmosphere using anneal times as low as 10 seconds, and at temperatures as low as 200°C. These data indicated that no pass/fail adhesion response could be found by lowering the temperature and time of the RTA, and thus this experiment was abandoned in favor of a technique that allowed a lower-temperature anneal.

To explore the effects of annealing at lower temperatures, a simple hot plate anneal was used. The apparatus for this second annealing experiment consisted of an electric hot plate, onto which was placed a solid copper disc of diameter 8cm and thickness 1cm to act as a heat source. A copper cylinder of diameter 3cm and height

5cm, into which a hole was drilled down the central axis, was placed atop the copper disc and secured using silver solder. A mercury thermometer capable of measuring temperatures up to 200°C was inserted into the hole and used to measure the annealing temperature. Because low temperature anneals do not result in reactions between the ambient atmosphere and the annealed film, these anneals were performed in ambient air.

Anneals were performed by first allowing the hot plate to stabilize at the desired temperature. A sample was placed face-down on the surface of the hot plate using tweezers and the start time and temperature of the anneal were logged. After the desired annealing time had elapsed, the sample was removed from the hot plate and allowed to cool face-up on a stainless steel tabletop.

Samples were subjected to low temperature (60-150°C) annealing for durations of 5 to 300 seconds. The low temperature annealing experiment was continued because critical pass/fail limits were found as annealing conditions were varied. Results appear in Part VI.

9. Post-anneal tape test of sample

A post-anneal tape test was then performed on each sample in the same manner as the pre-anneal tape test. Results indicated an improvement in film adhesion after anneal for specific combinations of annealing conditions and copper film thicknesses. Results appear in Part VI.

VI. RESULTS AND DISCUSSION

A. Results of Film Thickness Measurements

The electroless plating sequence described in Part V was performed on four substrate samples. Table I indicates a summary of plating time and film thickness measurement for each of the four samples.

TABLE I
COPPER PLATING TIME AND FILM THICKNESS
FOR FOUR SUBSTRATE SAMPLES

Sample	Time in Cu plating solution (s)	Cu film thickness (Å ± 25Å)
A	120	275
B	180	350
C	180	230
D	195	200

Two issues are of note here: First, the copper film thickness could not be measured very precisely because of the low resolution of the diamond stylus profilometer used to measure the height of the trenches in the etched copper film. Second, the plating time of a given sample does not always result in a thicker copper film. This may be due to the presence of organic contaminants on the substrate surface before plating is initiated. These contaminants may be present in the ambient air or in wafer storage containers [16]. Organic contaminants slow the electroless

film deposition because they prevent the BOE solution from adequately removing the native oxide layer [16] (in this case, TiO_2). It is believed that this results in inadequate nucleation of Pd atoms onto the surface during activation, thus resulting in reduced initial catalysis of the electroless copper deposition. It is believed that organic contamination did not have an effect on film adhesion.

B. Results of pre-anneal tape test, anneal, and post-anneal tape test

Following the measurement of film thickness on each of the samples, samples were diced into smaller portions, and a sequence of tape tests and anneals was performed as described in Part V. The result of each post-anneal tape test was given a score of "pass," "marginal," or "fail," as described in Part V, and was recorded. The following four scatterplots indicate results of the post-anneal tape test for samples from each of the four plated substrate samples.

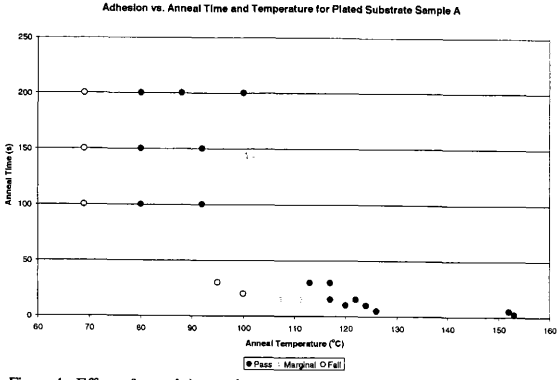

Figure 1. Effect of anneal time and temperature on adhesion for plated substrate sample A.

In Figure 1, note that anneals of length 15s first begin to pass the test near an annealing temperature of 110-115°C.

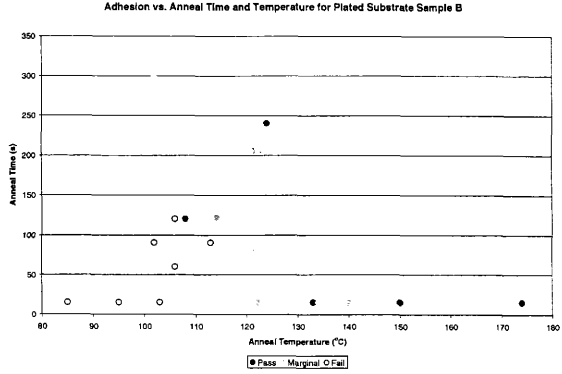

Figure 2. Effect of anneal time and temperature on adhesion for plated substrate sample B.

In Figure 2, note the presence of the apparent outlier with a passing score at 120s. This may be due to tape slippage due to sloppy tape handling during the post-anneal tape test for that particular sample. Note also the 15s anneal at 130-145°C range of marginal adhesion, with a passing score at 133°C.

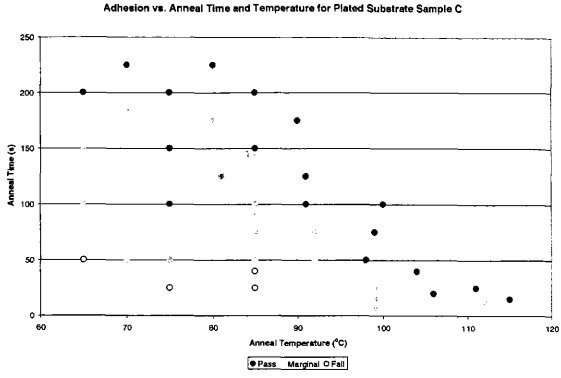

Figure 3. Effect of anneal time and temperature on adhesion for plated substrate sample C.

Figure 3 presents perhaps the clearest evidence for the effect of low temperature annealing on adhesion. Note the evidence of a linear relationship between annealing time, annealing temperature, and adhesion for this sample. Also note that a 15s anneal results in a passing score near 115°C.

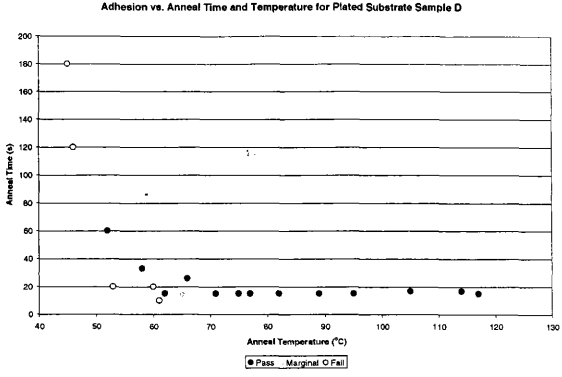

Figure 4. Effect of anneal time and temperature on adhesion for plated substrate sample D.

Here, note that even extremely low combinations of temperature and time resulted in passing scores on the post-anneal tape test. This may be due to the extreme thinness of the film.

Box plots of the post-anneal tape test results were also generated to determine the effect of annealing time and temperature on adhesion. See Figures 5 and 6.

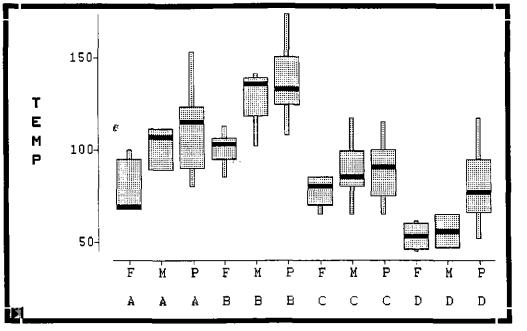

Figure 5. Distributions of passing, marginal, and failing results of the post-anneal tape test versus temperature for each of the 4 plated substrate samples.

Figure 5 indicates a general trend of samples failing, to marginally passing, to fully passing the post-anneal tape test with increased median anneal temperature. Thus, if anneal time remains constant, but anneal temperature is increased, it is expected that adhesion of the annealed copper film to the substrate would improve compared to its adhesion prior to annealing.

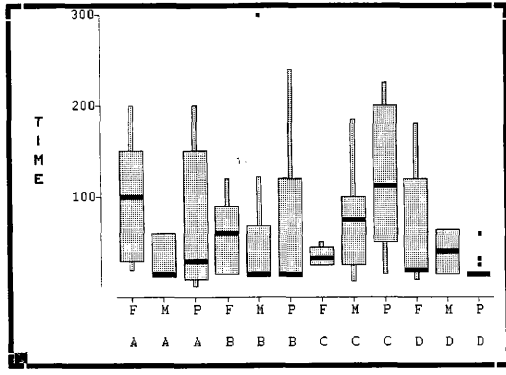

Figure 6. Distributions of passing, marginal, and failing results of the post-anneal tape test versus anneal time for each of the 4 plated substrate samples.

Figure 6 indicates a less clear relationship between post-anneal tape test results and median anneal time. This may be due to the treatment selection technique employed in this work: For each plated substrate sample, first a range of anneal temperatures was explored to find a critical region of temperature within which both passing and failing results for the post-anneal tape test could be found. After this range was found, the anneal time was varied for anneal temperatures within and below the critical range. A limited number of samples from each plated substrate sample could be cut: after these were used up, no further investigation of the effect of anneal time could be investigated. This resulted in a skewing of the adhesion vs.

time distribution, as seen in Figure 6, due to biased selections of anneal time. (The exception here is Plated Substrate Sample C, of which a sufficient number of samples could be cut so that a wider range of anneal time could be explored.)

The results displayed here indicate an improvement in the adhesion of electroless plated copper thin films on TiN deposited substrates after low temperature annealing. Anneal temperature is shown here to be the primary factor responsible for improved adhesion: both median temperature increase and individual temperature increases while holding anneal time constant result in improved adhesion.

Insufficient data exists to show that an increase in median anneal time results in a greater number of samples from a given plated substrate sample passing the post-anneal tape test. This is due to sampling over a biased range of anneal time; however, individual data, as seen in the scatterplots above, suggest that holding anneal temperature constant while increasing anneal time results in improved adhesion. Only the test data from plated substrate sample C suffer from less biased time sampling and thus indicate that an increase in median anneal time results in improved adhesion.

An examination of the lowest anneal temperatures at which each of the plated substrate samples pass a post-anneal tape test with an anneal time of 15s indicates a general trend of increased anneal temperature required for greater film thicknesses to pass the post-anneal tape test. Several explanations for this relationship may exist; however, based on previous work, it is thought that the thermal energy supplied by low temperature annealing allows atoms in the copper lattice to vibrate more freely, releasing hydrogen molecules trapped in the lattice during the electroless deposition

of copper [3]. Thicker films may require more thermal energy to allow all of the hydrogen to escape. Purging the hydrogen from the film with a low temperature anneal may decrease the compressive stress in the film, resulting in improved adhesion. Further work is needed to determine the amount of hydrogen purged from the film during low temperature annealing, as well as any decrease in compressive stress after such annealing.

VII. SUMMARY AND CONCLUSIONS

The superior electrical properties of copper have motivated a change from the use of aluminum to copper to fabricate interconnects on modern integrated circuits. This change has resulted in the building of faster, smaller, and more reliable circuits, but it has also required the development and implementation of new manufacturing processes to deposit copper reliably.

One such new process is the electroplating of copper onto thin copper seed layers. Seed layers can be deposited by a variety of methods, but a novel method is electroless copper plating, which results in extremely conformal coverage of copper into high-aspect ratio vias, featuring high reliability at a low cost.

Few studies of electroless copper deposition on diffusion barrier materials have been performed. Since the most important requirement of an effective metallization method is that the metal thin film must adhere to the substrate, this research investigated the adhesion of electroless plated copper thin films on titanium nitride, a barrier material in wide use for all types of copper deposition methods. The objective of the research is to characterize the effects of low temperature annealing on the adhesion of electroless copper films on TiN deposited substrates.

Results from this research indicate a trend of improved adhesion, as measured by the tape test, with increased time and temperature for a low temperature anneal of electroless plated copper films on TiN. Results also indicate that thicker films require

a combination of greater temperature and greater anneal time than do thinner films for an improvement in adhesion.

Further work is needed on two issues. First, a need exists to characterize the effects of low temperature annealing on the adhesion of electroless plated copper thin films on TiN beyond the limits of the tape test. A quantitative measurement of delamination stress is needed – indeed, the entire semiconductor fabrication industry suffers from the absence of a suitable measurement technique – but the electrostatic adhesion test is suggested to fill this need. Were this investigation performed using the electrostatic adhesion test instead of the tape test, this research would be a greater contribution to the field of semiconductor fabrication process development.

Second, a closer analysis of the effect of low temperature annealing on the hydrogen content of electroless plated copper films may well yield the answer as to why such simple annealing results in improved film adhesion. Additionally, a measurement of the compressive stress in annealed vs. unannealed electroless plated copper films, while not possible in this experiment, may give a more clear answer as to why low temperature annealing improves the adhesion of these films on TiN.

This investigation is another step in the development of electroless copper plating techniques to be employed in a modern semiconductor fabrication plant. These results pave the way for a greater understanding of reliable processes used to deposit copper and will eventually translate into the manufacture and availability of even smaller and faster integrated circuits utilizing copper metallization.

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APPENDIX A

PREPARATION OF SOLUTIONS FOR ELECTROLESS COPPER DEPOSITION

The following is adapted from the instructions for M-Copper Processing, MacDermid, Inc., 1997.

Conditioner

1. In a 1 L beaker, combine 825 mL DI water, 100 mL M-Condition A, 50 mL M-Condition B, and 25 mL M-Condition C.
2. Stir thoroughly using glass rod.

Predip

1. In a 1 L beaker, combine 250 mL DI water and 750 mL M-Predip L.
2. Stir thoroughly using glass rod.

Activator

1. In a 1 L beaker, combine 240 mL DI water, 750 mL M-Predip L, and 50 mL M-Activate.
2. Stir thoroughly using glass rod.

Accelerator

1. In a 1 L beaker, combine 990 mL DI water, 10 g M-Accelerate A powder. Stir thoroughly until M-Accelerate A powder is completely dissolved.
2. Add 10 mL M-Accelerate B.
3. Stir thoroughly using glass rod.

Copper

1. In a 1 L beaker, combine 823 mL DI water and 100 mL M-Copper 85B. Stir thoroughly.
2. Slowly add 40 mL M-Copper 85A.
3. Slowly add 30 mL M-Copper 85D.
4. Add 2 mL M-Copper 85G.
5. Stir thoroughly using glass rod.

APPENDIX B

PHOTOLITHOGRAPHY AND COPPER ETCH PROCEDURES

The following procedures are adapted from the *ELEN 472: Microelectronic Device Fabrication Laboratory Manual* by Dr. Mark H. Weichold, Texas A&M University, 1991.

APPENDIX B-1
PHOTORESIST APPLICATION AND PATTERNING

1. Immerse substrate in cold chloroethane and agitate for 3 minutes.
2. Remove and immerse in acetone and agitate for 3 minutes.
3. Remove and immerse in propanol and agitate for 3 minutes.
4. Remove and immerse in methanol and agitate for 3 minutes.
5. Blow substrate dry using N_2 gun.
6. Place substrate in dehydration oven for 5 minutes.
7. Place substrate on vacuum chuck in resist coater.
8. Place a small puddle (10 drops) of HMDS:PGMEA (1:1) on the center of the wafer and allow to spread.
9. Set the spinner controls to 12 seconds and 0 rpm. Turn on the spinner. Ramp the speed immediately up to 8000 rpm and then quickly back down to 4000 rpm. Spin at 4000 rpm for the remainder of the 12 seconds.
10. Coat the substrate with 15 to 20 drops of AZ5214 positive photoresist in the same fashion as step 8. Spin at 4000 rpm for 30 seconds.
11. Soft bake the substrate on a hot plate for 60 seconds at 80°C.
12. Place the substrate on the contact printer platform. Roughly align the mask above the substrate and turn the mask vacuum on. Expose for 6.5 seconds at 28.3 mW/cm^2.
13. Develop the substrate for 35 seconds in a 1:4 AZ400K:DI H_2O developer solution. Agitate while immersed.
14. Gently blow substrate dry using N_2 gun. Bake on hot plate at 135°C for 3 minutes.

APPENDIX B-2
COPPER ETCH AND PHOTORESIST REMOVAL

1. Immerse substrate in a dilute nitric acid solution (15% HNO_3) for 2 minutes or until no copper remains on the exposed surface.
2. Remove substrate from the acid and rinse for 1 minute under DI H_2O.
3. Immerse substrate in acetone and agitate for 5 minutes to remove photoresist.
4. Rinse substrate for 30 seconds under DI H_2O and blow dry with N_2 gun.

VITA

The author was born on October 21, 1977, in Baton Rouge, Louisiana. He is the son of Dr. and Mrs. Tim Tate also of Baton Rouge. After graduating from Catholic High School in Baton Rouge in 1995, he attended Texas A&M University with the support of a President's Endowed Scholarship in honor of Nami Uno Ando. After completing three co-op terms with Motorola, Inc. in Austin, Texas, he plans to graduate with a Bachelor of Science degree in Electrical Engineering in May, 1999. The author will be employed by Motorola in Austin in the Advanced Products Research and Development Laboratory beginning in June, 1999. He may be reached in care of Dr. Mark H. Weichold, Department of Electrical Engineering, Texas A&M University, College Station, Texas, 77843-3128. He is a member of the IEEE, Eta Kappa Nu, Tau Beta Pi, and Sigma Xi.