DESIGN OF CMOS INTEGRATED FREQUENCY SYNTHESIZERS FOR ULTRA-WIDEBAND WIRELESS COMMUNICATIONS SYSTEMS

A Dissertation

by

HAITAO TONG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2007

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Aydın İlker Karşılayan
Committee Members,	Jose Silva-Martinez
	Laszlo Kish
	Hans A. Schuessler
Head of Department,	Costas Georghiades

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ABSTRACT

Design of CMOS Integrated Frequency Synthesizers
for Ultra-wideband Wireless Communications Systems. (Auguest 2007)
Haitao Tong, B.S., Southeast University, China;
M.S., Southeast University, China
Chair of Advisory Committee: Dr. Aydın İlker Karşılayan

Ultra-wide band (UWB) system is a breakthrough in wireless communication, as it provides data rate one order higher than existing ones. This dissertation focuses on the design of CMOS integrated frequency synthesizer and its building blocks used in UWB system.

A mixer-based frequency synthesizer architecture is proposed to satisfy the agile frequency hopping requirement, which is no more than 9.5 ns, three orders faster than conventional phase-locked loop (PLL)-based synthesizers. Harmonic cancelation technique is extended and applied to suppress the undesired harmonic mixing components. Simulation shows that sidebands at 2.4 GHz and 5 GHz are below 36 dBc from carrier. The frequency synthesizer contains a novel quadrature VCO based on the capacitive source degeneration structure. The QVCO tackles the jeopardous ambiguity of the oscillation frequency in conventional QVCOs. Measurement shows that the 5-GHz CSD-QVCO in 0.18 μm CMOS technology draws 5.2 mA current from a 1.2 V power supply. Its phase noise is -120 dBc at 3 MHz offset. Compared with existing phase shift LC QVCOs, the proposed CSD-QVCO presents better phase noise and power efficiency.

Finally, a novel injection locking frequency divider (ILFD) is presented. Implemented with three stages in 0.18 μm CMOS technology, the ILFD draws 3-mA

current from a 1.8-V power supply. It achieves multiple large division ratios as 6, 12, and 18 with all locking ranges greater than 1.7 GHz and injection frequency up to 11 GHz. Compared with other published ILFDs, the proposed ILFD achieves the largest division ratio with satisfactory locking range.

To My parents

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CHAPTER I

INTRODUCTION

A. Motivation

The revolutionary ultra-wide band (UWB) technology brings several unprecedented challenges in the implementation of wireless communication systems. The frequency synthesizer design is one of such challenges, which resides in the requirement of extremely fast frequency hopping. The carrier frequency generated by the frequency synthesizer has to be changed from one to another within 9.5 nS, while conventional frequency synthesizer could only alter carrier frequency no faster than the order of microsecond. Novel architecture of frequency synthesizer is therefore indispensable.

The UWB systems can be realized with the zero-IF transceiver architecture, a promising low-cost and small-area solution for the integration of the whole system on one single chip. This zero-IF architecture demands the frequency synthesizer provide carrier frequency with quadrature phases. LC quadrature voltage-controlled oscillator (QVCO) is widely used in the generation of the quadrature carriers [1–4]. However, a recent publication [5] shows that conventional LC QVCO severely suffers from a certain unstable oscillation state, called bi-modal oscillation.

Frequency divider is another high-frequency component that draws research effort in this work. The disadvantages of low-speed high-power-consumption in conventional static frequency divider is increasingly problematic, as new wireless systems are often pushed to higher frequency and portable devices demand longer battery life.

This dissertation addresses the above challenges by presenting a mixer-based frequency synthesizer with agile frequency hopping, a harmonic-cancellation technique

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This dissertation follows the style of *IEEE Transactions on Automatic Control*.

to improve the signal spectrum purity at mixer output, a capacitive source degeneration QVCO (CSD-QVCO) to resolve the bi-modal oscillation, an injection frequency divider with highly nonlinear stages suitable to high-frequency and low-power applications.

B. Organization of the Dissertation

Chapter II presents a brief review of UWB technology and its impact on the design of frequency synthesizer.

Chapter III studies frequency synthesizer from a system point of view. It covers a summary of specifications with their effects on wireless systems, an introduction of phase-locked loop (PLL), and a comparison of existing frequency synthesizer approaches.

Starting from Chapter IV, design aspects of the frequency synthesizer for UWB are unfolded. Chapter IV presents the design of PLL in details.

Chapter V focuses on the design of harmonic-cancellation mixer, which helps to suppress undesired harmonic mixing components that are otherwise normally seen from conventional mixers.

Chapter VI presents frequency divider design in two parts. The first one is on the frequency divider implemented in the frequency synthesizer. The emphasis is put on the half-quadrature signal generation. The second one is on the design of an injection locking frequency divider. Its capability of high-frequency and low-power operation is discussed.

The CSD-QVCO is presented in Chapter VII. Detailed analysis reveals its ability to suppress bimodal oscillation. Also the start-up condition and phase error generation due to device mismatch are covered in this chapter.

Chapter VIII provides the experimental results of the prototype frequency synthesizer and some stand-alone building blocks, such as the CSD-VCO and the injection locking frequency divider.

Chapter IX draws conclusions of this dissertation.

CHAPTER II

RESEARCH BACKGROUND

A. Ultra-wide Band (UWB) Technology

The era of wireless communications started from Guglielmo Marconi's historical experiment in 1901 to sent radio signals across the Atlantic Ocean. While the various wireless systems and technology have been populated from then on, the development of wireless network has came into picture only in the very recent years, triggered by the vast usage of computers and the maturity of integrated circuits process and design technology. Wireless network utilizes radio waves, rather than cables, to keep computers connected. Therefore, wireless network offers the great advantage of mobility by eliminating messy cables. Nowadays wireless network are dominated by narrow band systems like Bluetooth, Zigbee and IEEE 802.1a/b/g. Their limited data rate, no more than 54Mb/s, is insufficient to fast transfer large files and high-quality videos. To address this speed limit issue, ultra-wideband (UWB) systems are proposed to increase the data rate to several hundreds of Mb/s. Table I compares key parameters of various wireless network technologies.

To achieve high data rate, UWB systems use a wide bandwidth rather than a large signal-to-noise ratio (SNR). This is understandable by referring to Shannon's theorem:

$$C = B \log_2(1 + SNR) \tag{2.1}$$

where C denotes the channel capacity in bits per second and B is the bandwidth of the channel in hertz. (2.1) shows that the channel capacity has a stronger dependence with bandwidth (linear relation) than the SNR (logarithmic relation). Therefore

Table I. Comparison of various wireless network systems

System	Data Rate (Mb/s)	Output Power (mW)	Range (meters)	Frequency Band
Bluetooth	1-2	100	100	2.4 GHz
Zigbee	0.02-0.25	1	75	0.868/0.915/2.4 GHz
IEEE 802.11a	54	40-800	20	5 GHz
IEEE 802.11b (Wi-Fi)	11	200	20	2.4 GHz
IEEE 802.11g	54	65	50	2.4 GHz
UWB	100-500	1	10	3.1-10.6 GHz

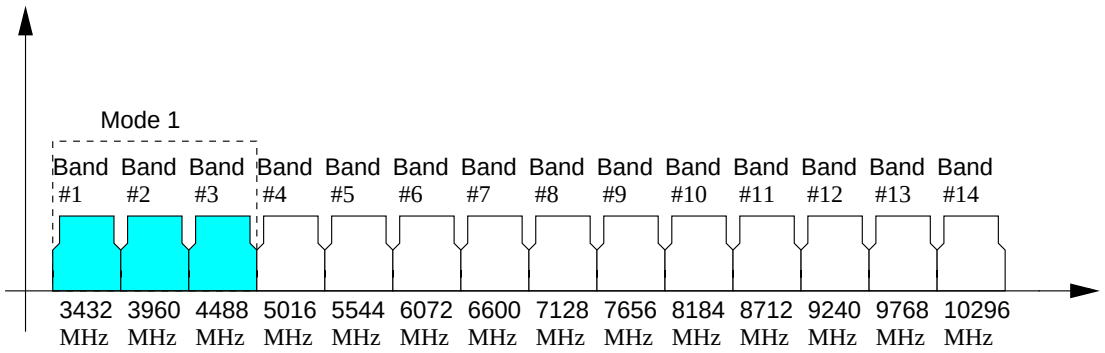


Fig. 1. UWB band chart

higher data rate is more efficiently realized by increasing the bandwidth. The spectrum released for UWB by the Federal Communications Commission (FCC) covers from 3.1 GHz to 10.6 GHz. While occupying such a wide bandwidth, the scarcity of spectrum requires the UWB systems co-exist with other wireless services. Therefore, a low transmit power level is required so that the UWB signals will not interfere signals from these services. In the mean time, UWB systems have to deal with relatively high interference levels due to these services. Particularly, the services at 2.4 GHz and 5 GHz ISM bands are harmful. This is because those bands are close the UWB band and can only be attenuated at a rather limited degree by the pre-select filter placed in the front of the UWB receiver.

The orthogonal frequency-division multiplexing (OFDM) based multiband standard was proposed on July 14, 2003 by Multiband OFDM Alliance (MBOA), including Intel, Texas Instruments and several other major companies. The MBOA divides the spectrum spanning from 3168 to 10560 MHz into 14 bands, each with a bandwidth of 528 MHz. The band chart is shown in Fig. 1. Bands 1-3 (mode-1) are mandatory, while the other bands are reserved for future use. The multiband approach requires the transmitted OFDM symbols being time-interleaved across the bands, as shown in Fig. 2. An advantage of this approach is that the robustness of the system with

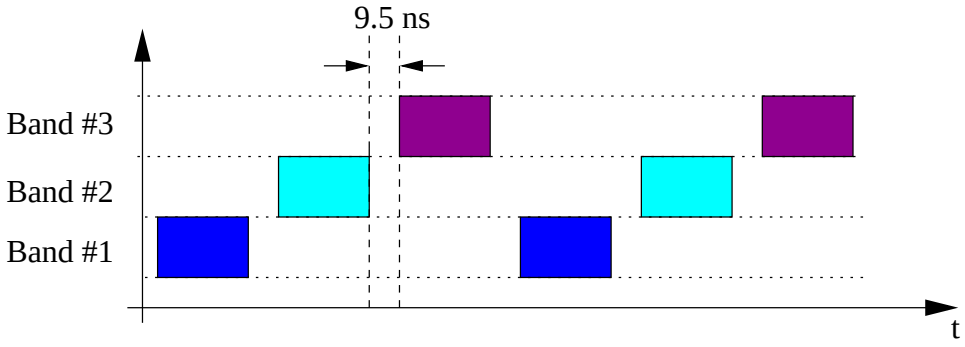


Fig. 2. UWB band hopping in mode-1

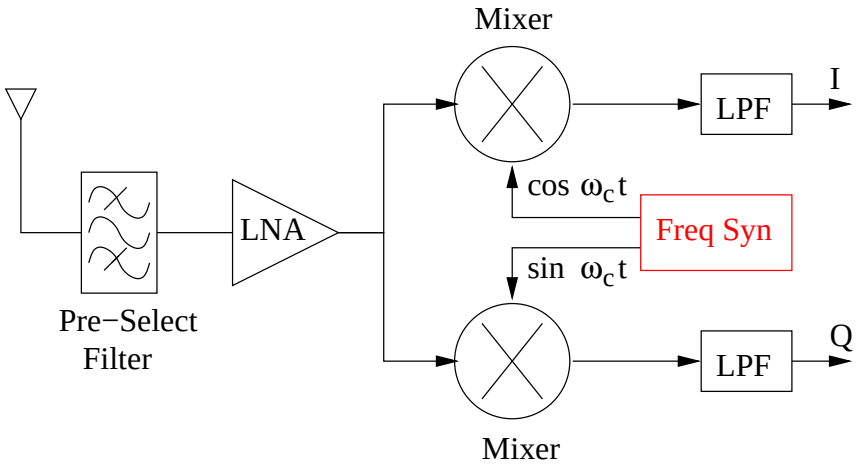


Fig. 3. Direct conversion receiver architecture

respect to interference is improved. This is because the average transmitted power is the same as a system designed to operate over the entire bandwidth. However, the hopping between the bands have to be below 9.5 ns, as suggested by MBOA.

Direct conversion, as shown in Fig. 3, is considered as the most promising receiver architecture for UWB [6–8]. In the direct conversion system, frequency synthesizer generates carrier frequency for mixers to down-convert received signal to baseband. Notice that quadrature output is demanded from the frequency synthesizer. This scheme needs the least number of components, leading itself to be a feasible solution to single-chip implementation. Its common issue of flicker noise at low frequencies

have a minor effect in this application, because MBOA UWB is intentionally devised to contain no signals at low frequencies.

CHAPTER III

FREQUENCY SYNTHESIZER: A SYSTEM REVIEW

A. Introduction

A frequency synthesizer is a system for generating any frequency of a certain range. Regarded as one of the most critical modules, frequency synthesizers are widely found in modern wireless communications systems. A simplified block diagram of a wireless system is shown in Fig. 4. On the transmitter side, frequency synthesizer provides carrier frequency for the up-convert mixer. This carrier frequency modulates the low frequency baseband signal coming to the up-convert mixer, which is then sent out by the power amplifier. On the receiver side, the low noise amplifier picks up the received signal and amplifies it to a certain level. The frequency synthesizer again provides the carrier frequency, but this time to demodulate the received signal to the baseband signal in the down-convert mixer.

1. Design Considerations

As a key block in wireless systems, frequency synthesizer demands quite a few of design considerations. One major concern is the functionality of frequency synthesizer, including frequency accuracy, frequency step and tuning range. Another concern is the quality of the carrier signal, including amplitude, phase noise and sideband. Also, attention has to be paid to general considerations of a circuit, such as power consumption and chip area. We discuss all those considerations as follows.

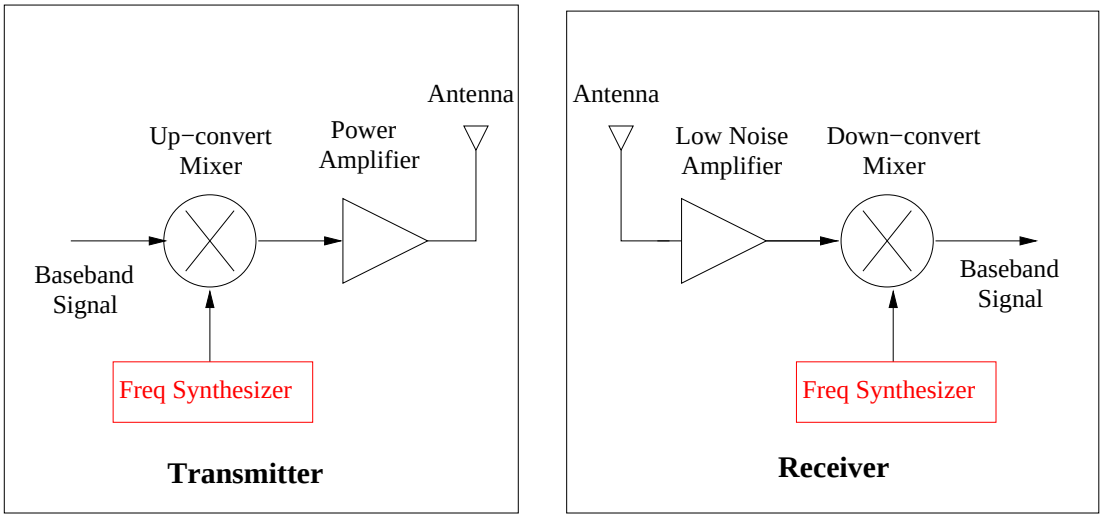


Fig. 4. A simplified wireless system block diagram

a. Frequency Accuracy

Frequency accuracy defines to which extent the synthesized frequency is close to the desired frequency. The frequency generated from frequency synthesizer has to be very accurate. Otherwise, on the transmitter side, the transmitted signal would move into adjacent channel, causing illegal interference; on the receiver side, the frequency information embedded in the received signal is corrupted. Indeed, in many wireless systems, the frequency accuracy has to maintain below a few parts per million (ppm). For example, the UWB system requires the frequency accuracy to be ± 20 ppm maximum. This means, for instance, the frequency error is only ± 84.5 KHz for a carrier frequency of 4224 MHz.

b. Frequency Step

Frequency step sets the finest frequency spacing between any two synthesized frequencies.The value of frequency step could vary a lot over different wireless communications systems. In North American Digital Cellular (NADC) system, frequency step is as small as 30 KHz. On the contrary, in UWB system, frequency step is as

large as 528 MHz.

c. Tuning Range

Tuning range is the output frequency range of a frequency synthesizer. Similar to frequency step, tuning range varies with wireless communications systems. While NADC system requires 25 MHz tuning range, UWB system demands the synthesizer covers 1584 MHz tuning range.

d. Lock Time

Lock time is a critical parameter that indicates how fast the frequency synthesizer output frequency is changed from one to another, upon receiving a command to change frequency. While typical RF systems require lock time to be from tens of milliseconds to tens of microseconds, UWB system needs much smaller lock time, which is no more than 9.5 nanosecond.

e. Amplitude

As frequency synthesizer is normally used to drive a mixer, the amplitude of the synthesized frequency is specified by the mixer requirement. Low amplitude leads to the reduction of the signal level at the mixer output. On the other hand, if the amplitude is too high, leakage problems occur. Fig. 5 shows possible leakage paths. First, it could be leaked to the inputs of the mixer, either in a direct way or through mixer to LNA and back to the mixer. The leakage signal is then mixed with synthesized signal and produces DC offset at the mixer output. This DC offset is one of the most critical problems in direct-conversion receivers. Also, the synthesized signal would be leaked to the antenna and radiated to air, which creates interference to other receivers using the same signal band.

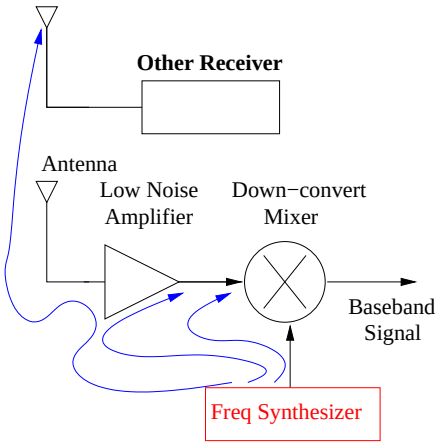


Fig. 5. LO leakage paths

f. Phase Noise

All real signals are accompanied with noise, so is the output of frequency synthesizer. More specifically, the noise presented at the frequency synthesizer output could be decomposed to amplitude modulation (AM) noise and phase modulation (PM) noise. For a nominally periodic sinusoidal signal $x(t)$, we can write,

$$x(t) = A[1 + \alpha_n(t)]\cos[\omega_c t + \phi_n(t)] \tag{3.1}$$

where $\alpha_n(t)$ is a small random excess amplitude representing AM noise and $\phi_n(t)$ is a small random excess phase presenting PM noise.

AM noise is normally not a critical design parameter. This is because mixer is insensitive to the amplitude of LO as long as it is higher than a certain level. On the contrary, PM noise, also called "phase noise", is the predominant noise form. To understand the importance of phase noise, let us first characterize it in spectrum. Note that by neglecting $\alpha_n(t)$ and assuming $\phi_n(t) \ll 1\ rad$, (3.1) could be simplified as,

$$x(t) \approx A\cos(\omega_c t) - A\phi_n(t)\sin(\omega_c t) \tag{3.2}$$

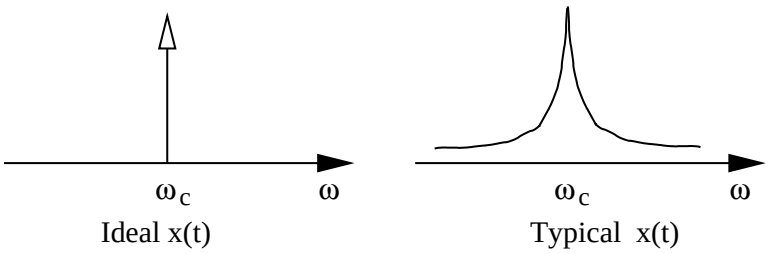


Fig. 6. LO phase noise

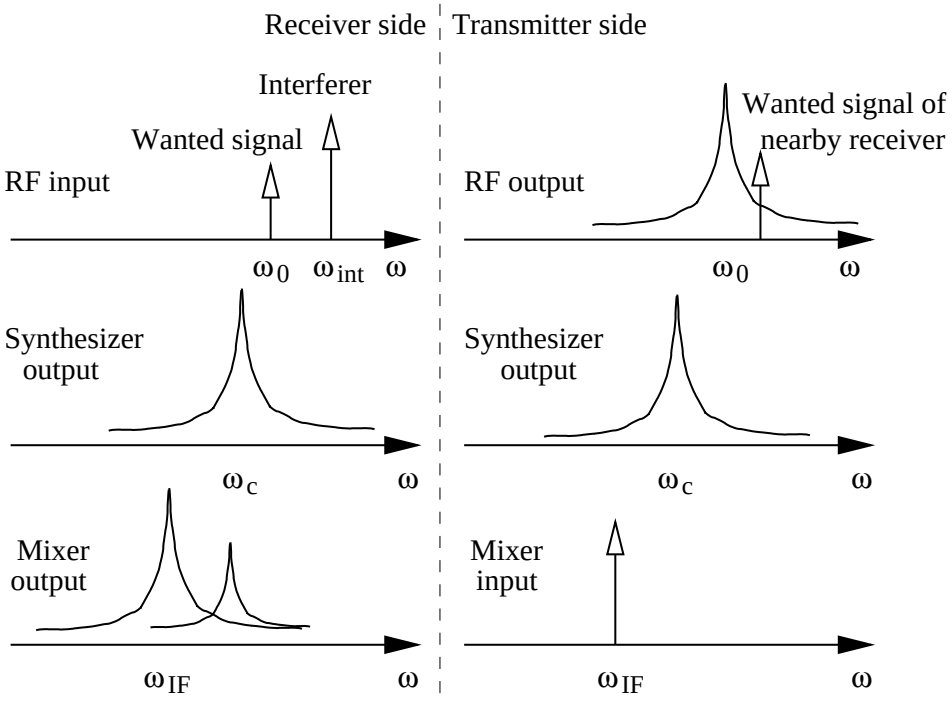


Fig. 7. Phase noise impact on transceiver

The second term in the right side of (3.2) shows that the spectrum of phase noise $\phi_n(t)$ is translated to $\pm\omega_c$. Fig. 6 shows the spectrum comparison of a typical $x(t)$ with an ideal $x(t)$ without noise. Unlike the impulse shape of an ideal $x(t)$ without noise, the spectrum of a typical $x(t)$ is spread over a large frequency range, with the trend of lower power level for frequency farther away from the carrier frequency. The quantization of phase noise is most commonly expressed in units of dBc/Hz at an offset from the carrier frequency. It could be measured or calculated by obtain the

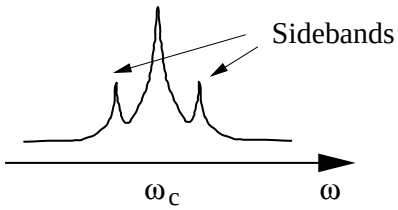


Fig. 8. LO sidebands

noise power over 1Hz bandwidth around that offset frequency, and divides the results by the carrier power.

The effect of phase noise in wireless transceivers is shown in Fig. 7. On the receiver side, as the desired signal may be accompanied by a large interference in nearby frequency band, both signals would be mixed with the frequency synthesizer output. Therefore, at the mixer output, the two spectra are overlapped at the desired band. This effect would increase the noise level and degrade the quality of the down-converted signal. In the extreme case, with a noisy frequency synthesizer and a strong interference, the interference spectra down-converted to the desired band is even higher than the desired spectra and eventually saturates following circuits. On the transmitter side, the noisy frequency synthesizer spreads signal to other band, which becomes interference to receivers nearby.

g. Sideband

Other than phase noise, as shown in Fig.8, the purity of frequency synthesizer output spectra is also degraded by sideband, also called "spur". There are several sources that could generate sideband. One is coupling signal from other circuits that either modulates or is directly coupled to the frequency synthesizer output. But more likely, sidebands are caused by non-idealities of frequency synthesizer, as will be studied in details in Chapter IV. Similar to phase noise, sideband is quantified in terms of the sideband amplitude relative to the carrier amplitude with the unit as dBc. Illustrated

in Fig. 9, depending on the desired signal bandwidth and the relative position of the sideband to the carrier in spectrum, receiver could be affected in two cases, as listed below,

1. If the sideband falls out of wanted signal band but close to a certain interference, the interference would be mixed with the sideband and translated to the desired mixer output band;

2. If the sideband falls into wanted signal band, the wanted signal would be down-converted to the desired mixer output band with a frequency offset equal to the one between the sideband and the carrier frequency.

On transmitter side, shown in Fig. 10, similar things happen. If sideband is far away from to the carrier, it can up-convert desired signal to other bands, affecting signal reception of receivers in those bands. If sideband is close to the carrier, it can contaminate its own transmitted band by up-converting desired signal to the band.

h. Area, Level of Integration and Power Consumption

Cost could be reduced by having less chip area while integrating more components. Less power consumption is also preferred, especially in wireless communications systems, of which in many applications circuit may be powered only by battery.

B. PLL Basics

Phase locked loop (PLL) is widely used in the design of frequency synthesizers. It is a key block in most frequency synthesizers. In many applications, the PLL itself serves as a frequency synthesizer.

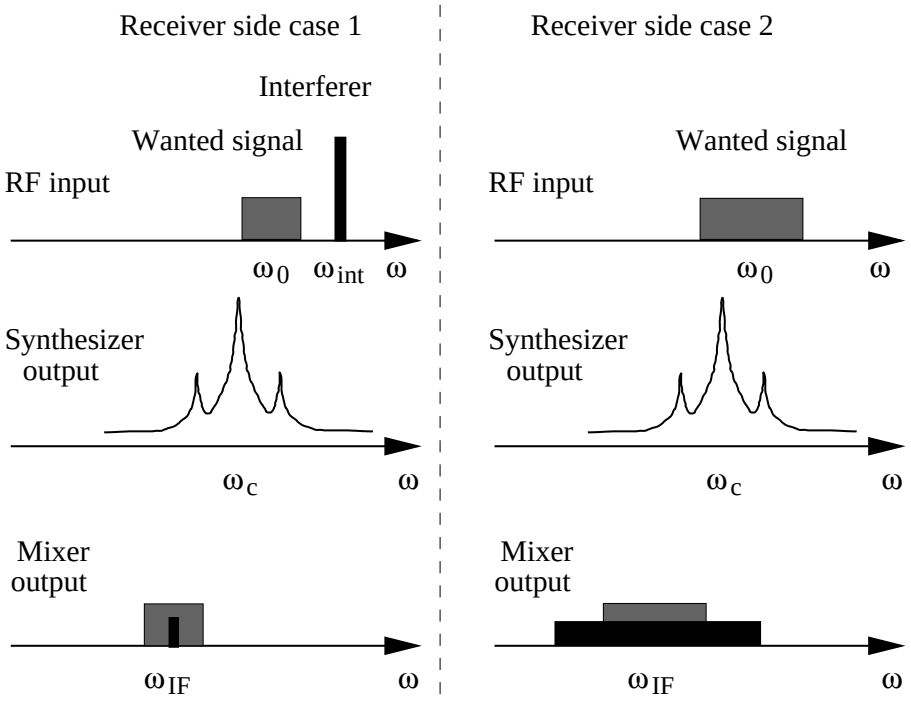


Fig. 9. Sideband impact on receiver

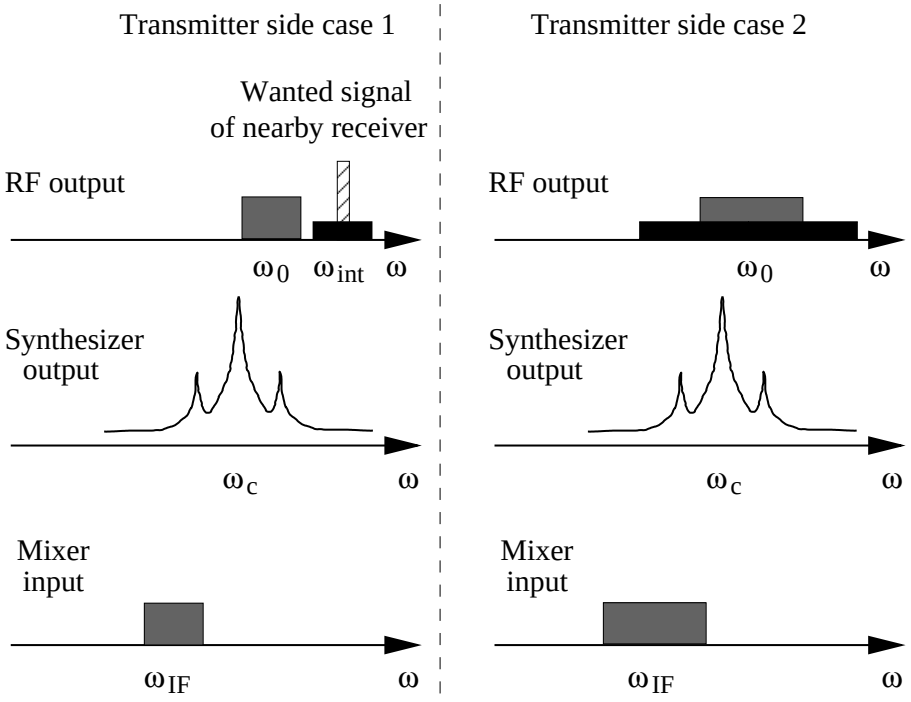


Fig. 10. Sideband impact on transmitter

1. Concept of Phase Locking

Considering two signals $x_1(t) = cos[\omega_1 t + \phi_1(t)]$ and $x_2(t) = cos[\omega_2 t + \phi_2(t)]$, the instant phases and frequencies of them would be

$$\Phi_1(t) = \omega_1 t + \phi_1(t) \tag{3.3}$$

$$\Phi_2(t) = \omega_2 t + \phi_2(t) \tag{3.4}$$

$$\Omega_1(t) = \delta[\Phi_1(t)]/\delta t = \omega_1 + \delta[\phi_1(t)]/\delta t \tag{3.5}$$

$$\Omega_2(t) = \delta[\Phi_1(t)]/\delta t = \omega_2 + \delta[\phi_2(t)]/\delta t \tag{3.6}$$

Phase locking means that the phase difference between those two signals is constant with time. Therefore,

$$\delta[\Phi_1(t) - \Phi_2(t)]/\delta t = \Omega_1(t) - \Omega_2(t) = 0 \tag{3.7}$$

This means that once phase locking is achieved, there is no frequency difference between those two signals.

The above conclusion is exploited in PLL. By using a feedback loop, a constant phase difference of two periodic signals is ensured when the loop reaches its steady state.

2. PLL Building Blocks

- **Phase detector (PD)** generates a signal with its DC component proportional to the phase difference between two periodic input signals,

$$\overline{v_{out}} = K_{PD}\Delta\phi \tag{3.8}$$

  where K_{PD} is the gain of the phase detector and $\Delta\phi$ is the input phase difference.

- **Low-pass filter (LPF)** takes in the output from PD and filters out its high-

frequency component. The mathematic characterization of LPF depends on its various implementations.

- **Voltage-control oscillator (VCO)** is a circuit that generates a periodic output with frequency that can be tuned over a certain range by applying a voltage to it. In PLL, the control voltage comes from LPF output.

$$\omega_{out} = \omega_{fr} + K_{VCO} V_{ctrl} \tag{3.9}$$

where ω_{fr} is the free running frequency of the VCO, K_{VCO} is the gain of the VCO and V_{ctrl} is the control voltage.

- **Frequency divider** divides input of high frequency to a lower value.

$$\omega_{out} = \omega_{in}/N \tag{3.10}$$

where N is the division ratio.

3. PLL Operation Basics

Fig. 11 presents a basic PLL structure. A PLL is a feedback system that minimizes the phase difference between reference input $x(t)$ and feedback signal $y(t)$. To do that, a PD generates an output whose DC value is proportional to the phase difference between $x(t)$ and $y(t)$. LPF extracts that DC value and applies it to frequency control terminal of VCO, which changes frequency of y(t), generated by VCO. In many applications, frequency of y(t) is much higher than frequency of x(t). Thus Frequency divider is employed to bring down frequency of y(t) to the one comparable to frequency of x(t). When the loop reaches its steady state, the phase difference between $x(t)$ and $y(t)$ is constant over time. Therefore, $f_{out} = N f_{ref}$, where N is the division ratio. It is deserved to point out here that by changing N, the VCO output

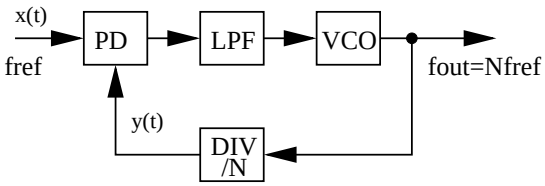


Fig. 11. A basic PLL

Table II. Transfer functions of PLL blocks

Block	Transfer Function
PD	K_{PD}
LPF	$L(s)$
VCO	$\frac{K_{VCO}}{s}$
Divider	$\frac{1}{N}$

frequency is changed accordingly, which is the output of the frequency synthesizer.

4. Types of PLL

a. Type I PLL

PLL could be analyzed using the transfer function of output phase versus input phase, i.e. $\phi_{out}(s)/\phi_{in}(s)$. Transfer function of each block inside PLL is listed in Table II.

A first-order low pass filter is a common implementation of $L(s)$. It is expressed as,

$$L(s) = \frac{1}{1 + s/\omega_p} \tag{3.11}$$

Fig. 12 shows the PLL linear model. The open loop transfer function $H_O(s)$

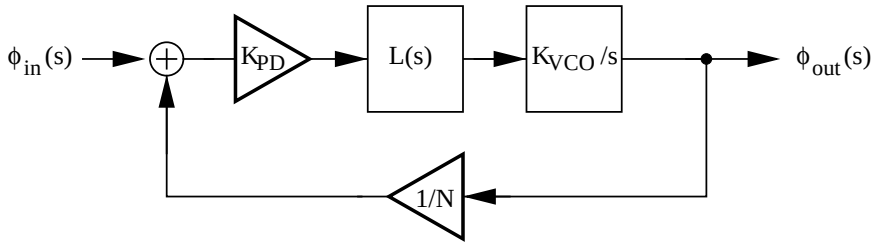


Fig. 12. Type I PLL linear model

could be obtained as,

$$H_O(s) = \frac{K_{PD}K_{VCO}}{N} \cdot \frac{1}{s(1 + s/\omega_p)} \tag{3.12}$$

$H_O(s)$ contains only one pole at zero. This is the reason why this type of PLL is called type I PLL. The unity-gain frequency ω_u is,

$$\omega_u = \frac{K_{PD}K_{VCO}}{N} \tag{3.13}$$

Therefore the phase margin PM is,

$$PM = 90^\circ - \arctan \frac{K_{PD}K_{VCO}}{N\omega_P} \tag{3.14}$$

(3.14) shows that small $K_{PD}K_{VCO}$ and large $N\omega_P$ are preferred for stability. The close loop transfer function $H_C(s)$ is derived as,

$$H_C(s) = \frac{K_{PD}K_{VCO}\omega_p}{s^2 + s\omega_p + K_{PD}K_{VCO}\omega_p/N} \tag{3.15}$$

The two poles of $H_C(s)$ are given by

$$s_{1,2} = \frac{1}{2}\left(-\omega_p \pm \sqrt{\omega_p^2 - \frac{4K_{PD}K_{VCO}}{N}}\right) \tag{3.16}$$

If $\omega_p^2 - 4K_{PD}K_{VCO}/N > 0$, the two poles are real and the transient step response is,

$$\begin{aligned}\omega_{out}(t) =& \frac{2K_{PD}K_{VCO}}{\sqrt{\omega_p^2 - \frac{4K_{PD}K_{VCO}}{N}}} \frac{1}{\omega_p - \sqrt{\omega_p^2 - \frac{4K_{PD}K_{VCO}}{N}}} \left[1 - e^{-\frac{1}{2}\left(\omega_p - \sqrt{\omega_p^2 - \frac{4K_{PD}K_{VCO}}{N}}\right)t}\right] \\ & - \frac{1}{\omega_p + \sqrt{\omega_p^2 - \frac{4K_{PD}K_{VCO}}{N}}} \left[1 - e^{-\frac{1}{2}\left(\omega_p + \sqrt{\omega_p^2 - \frac{4K_{PD}K_{VCO}}{N}}\right)t}\right] u(t)\Delta\omega \end{aligned} \quad (3.17)$$

(3.17) shows that the step response includes two exponential terms decaying with time constants c_1 and c_2 as,

$$\begin{aligned} c_1 &= \left[\frac{1}{2}\left(\omega_p - \sqrt{\omega_p^2 - \frac{4K_{PD}K_{VCO}}{N}}\right)\right]^{-1} \\ c_2 &= \left[\frac{1}{2}\left(\omega_p + \sqrt{\omega_p^2 - \frac{4K_{PD}K_{VCO}}{N}}\right)\right]^{-1} \end{aligned} \quad (3.18)$$

Since $c_1 > c_2$, the settling time is mainly determined by c_1, which decreases with the increase of $4K_{PD}K_{VCO}/N$. This observation implies a trade-off between the settling time and the stability. Larger $K_{PD}K_{VCO}/N$ is preferred for less settling time but it results in worse stability. When $\omega_p^2 < 4K_{PD}K_{VCO}/N$, both poles become complex and the transient step response is changed to,

$$\begin{aligned}\omega_{out}(t) =& 1 - e^{-\frac{1}{2}\omega_p t}\left[\cos\left(\sqrt{\frac{4K_{PD}K_{VCO}}{N} - \omega_p^2}\cdot t\right) + \right. \\ & \left. \frac{\omega_p}{\sqrt{\frac{4K_{PD}K_{VCO}}{N} - \omega_p^2}} \sin\left(\sqrt{\frac{4K_{PD}K_{VCO}}{N} - \omega_p^2}\cdot t\right)\right] N\Delta\omega u(t) \end{aligned} \quad (3.19)$$

Therefore, the step response now contains only one exponential term with the time constant of $2/\omega_p$, which is less than the time constant for real pole case. Further decrease of settling time requires increase of ω_p. However, as PD output signal normally contains high frequency components, the increase of ω_p results in less compression of those spurious components. This observation could be explained by showing the

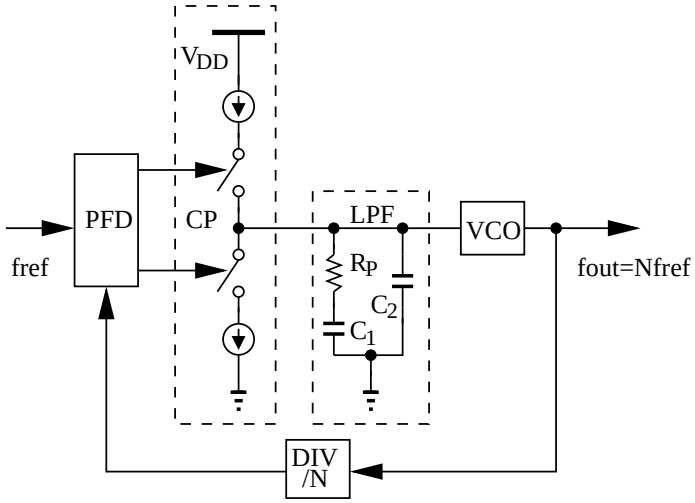


Fig. 13. Type II PLL

closed-loop transfer function from PD output to VCO output as,

$$H_{C-PD}(s) = \frac{K_{VCO}}{s^2/\omega_p + s + K_{PD}K_{VCO}/N} \tag{3.20}$$

The amplitude of $H_{C-PD}(s)$ at high frequency is decreased for the decrease of ω_p.

As a conclusion, type I PLL suffers from trade-offs between settling time, stability and high-frequency suppression at PD output. Those drawbacks drive people to seek alternative PLL solutions.

b. Type II PLL

A typical implementation of type II PLL is shown in Fig. 13. As the charge pump is controlled to either sink or source current in a digital fashion, the PLL becomes a discrete system, rather than a continuous one. Therefore, strictly speaking, this type of PLL can not be analyzed in s domain. A simplified Gardner limit [9] states that as long as the loop bandwidth is less than one-tenth the reference frequency, s domain analysis is still acceptable. Furthermore, PD is replaced by PFD (phase-frequency detector) to increase the locking range. The mechanism of PFD will be discussed in

Chapter IV, which will not prevent us from the analysis of the PLL in this chapter.

PFD together with CP could be modeled as $I_P/2\pi$, where I_P is the sink/source current in CP. The open loop transfer function is calculated as,

$$H_O(s) = \frac{I_P K_{VCO}}{2\pi N(C_1 + C_2)} \cdot \frac{1}{s^2} \cdot \frac{1 + sR_P C_1}{1 + sR_P \dfrac{C_1 C_2}{C_1 + C_2}} \tag{3.21}$$

(3.21) shows that $H_O(s)$ contains two poles at zero frequency, one from VCO and the other from CP together with LPF. Those two poles makes this type of PLL called type II PLL. The components inside LPF serve the following purposes,

- C_1: together with CP to generate one pole at zero frequency.
- R_P: together with C_1 to generate a zero at left half plane (LHP) to stabilize the system. To do that, this zero has to be less than unity-gain frequency
- C_2: together with R_P to generate a pole to suppress high frequency components at VCO control line. For stability, this pole has to be much larger than unity-gain frequency.

From (3.21), the phase margin PM is given by

$$PM = \arctan(\omega_u R_P C_1) - \arctan\left(\omega_u R_P \frac{C_1 C_2}{C_1 + C_2}\right) \tag{3.22}$$

where ω_u is the unity-gain frequency.

The inclusion of three poles and one zero in $H_O(s)$ makes the computation of ω_u rather complicated. But as the non-zero pole has to be far away from ω_u for stability, this pole could be ignored and $H_O(s)$ is simplified to

$$H_O(s) \approx \frac{I_P K_{VCO}}{2\pi N C_1} \cdot \frac{1}{s^2} \cdot (1 + sR_P C_1) \tag{3.23}$$

Therefore, ω_u is computed as,

$$\omega_u \approx \sqrt{\frac{I_P K_{VCO}}{2\pi N C_1}} \cdot \sqrt{\frac{\frac{I_P K_{VCO}}{2\pi N C_1}(R_P C_1)^2 + \sqrt{\left[\frac{I_P K_{VCO}}{2\pi N C_1}(R_P C_1)^2\right]^2 + 4}}{2}} \tag{3.24}$$

(3.24) shows that the increase of $I_P K_{VCO}$ results in the increase of ω_u, which leads to the increase of PM according to (3.22). This is contrary to the conclusion drawn for type I PLL, which states that the increase of $K_{PD}K_{VCO}$ jeopardizes stability by decreasing PM.

The closed loop transfer function $H_C(s)$ is shown as

$$H_C(s) = \frac{I_P K_{VCO}}{2\pi N(C_1 + C_2)} \cdot \frac{1 + sR_P C_1}{s^3 R_P \frac{C_1 C_2}{C_1 + C_2} + s^2 + s\frac{I_P K_{VCO} R_P}{2\pi N}\frac{C_1}{C_1 + C_2} + \frac{I_P K_{VCO}}{2\pi N(C_1 + C_2)}} \tag{3.25}$$

Again we ignore C_2 when we study the closed loop transient response. $H_C(s)$ is therefore approximated as,

$$H_C(s) \approx \frac{I_P K_{VCO}}{2\pi N C_1} \cdot \frac{1 + sR_P C_1}{s^2 + s\frac{I_P K_{VCO} R_P}{2\pi N} + \frac{I_P K_{VCO}}{2\pi N C_1}} \tag{3.26}$$

The two roots for he denominator of $H_C(s)$ is calculated as,

$$s_{1,2} = \frac{1}{2}\left(-\frac{I_P K_{VCO}}{2\pi N}R \pm \sqrt{\left(\frac{I_P K_{VCO}}{2\pi N}R\right)^2 - 4\frac{I_P K_{VCO}}{2\pi N C_1}}\right) \tag{3.27}$$

Similar to the case of type I PLL, the system will have higher settling speed when the two poles are complex, which means

$$\left(\frac{I_P K_{VCO}}{2\pi N}R\right)^2 - 4\frac{I_P K_{VCO}}{2\pi N C_1} < 0 \Rightarrow \frac{I_P K_{VCO}}{2\pi N} < \frac{1}{R^2 C} \tag{3.28}$$

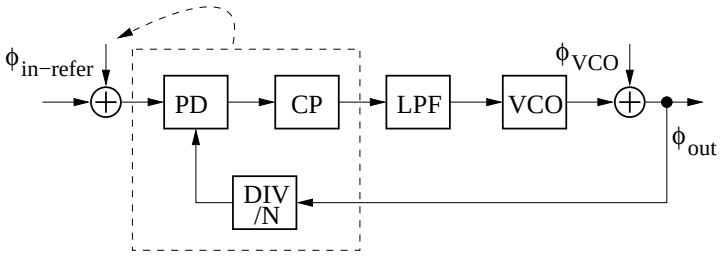


Fig. 14. PLL phase noise sources

Under this condition, the transient step response is given by

$$\omega_{out}(t) = 1 - e^{-\left(\frac{1}{2}\frac{I_P K_{VCO}}{2\pi N} R_P\right)t} \left[\cos\left(\sqrt{4\frac{I_P K_{VCO}}{2\pi N C_1} - \left(\frac{I_P K_{VCO}}{2\pi N} R\right)^2} \cdot t \right) + \frac{R_P C_1}{2\sqrt{4\frac{I_P K_{VCO}}{2\pi N C_1} - \left(\frac{I_P K_{VCO}}{2\pi N} R\right)^2}} \sin\left(\sqrt{4\frac{I_P K_{VCO}}{2\pi N C_1} - \left(\frac{I_P K_{VCO}}{2\pi N} R\right)^2} \cdot t \right) \right] N\Delta\omega u(t) \tag{3.29}$$

The step response contains only one exponential term with the time constant c expressed as

$$c = \left(\frac{1}{2}\frac{I_P K_{VCO}}{2\pi N} R_P\right)^{-1} \tag{3.30}$$

To minimize the settling time, $I_P K_{VCO}$ has to to maximized.

From the above study of stability and settling time, there is no tradeoff between those two critical specifications with regarding to choosing $I_P K_{VCO}$. However, the increase of $I_P K_{VCO}$ would be ultimately bounded by ω_u, which is limited by no more than one-tenth of the reference frequency.

5. PLL Phase Noise

An important advantage of using PLL for frequency generation is that when noisy oscillator output is forced to compare with a clean source, e.g. a crystal oscillator output, through the feedback loop, the phase noise at the oscillator output is much suppressed. We show this by deriving the following transfer function from VCO to PLL output,

$$H_{VCO}(s) = \frac{\phi_{out}}{\phi_{VCO}} \approx \frac{s^2}{s^2 + s\frac{I_P K_{VCO} R_P}{2\pi N} + \frac{I_P K_{VCO}}{2\pi N C_1}} \tag{3.31}$$

(3.31) shows that VCO phase noise is high-pass filtered by PLL. This is much expected, as when frequency goes higher and higher, the loop gain of PLL becomes so small that it can not correct the noise-induced phase deviations from VCO. On the other hand, noises from reference, PFD, charge pump and frequency divider are low-pass filtered at PLL output. To show this, we first refer all those mentioned noises to input as $\phi_{in-refer}$. The transfer function $H_{in-refer}(s)$ from $\phi_{in-refer}$ to ϕ_{out} is calculated as,

$$H_{in-refer}(s) \approx \frac{I_P K_{VCO}}{2\pi N C_1} \cdot \frac{1 + sR_P C_1}{s^2 + s\frac{I_P K_{VCO} R_P}{2\pi N} + \frac{I_P K_{VCO}}{2\pi N C_1}} \tag{3.32}$$

Thermal noise of resistor R_P is the only noise source inside LPF. Generally speaking, the thermal noise of a resistor R can be modeled by a series voltage source, with the one-sided spectral density given by

$$\overline{V_n^2}(f) = 4kTR \tag{3.33}$$

where k is the Boltzmann constant. Thus, ϕ_{out} due to R_P thermal noise is expressed

as,

$$\phi_{VCO} \approx \frac{\sqrt{4kTR_P}K_{VCO}s}{s^2 + s\frac{I_P K_{VCO} R_P}{2\pi N} + \frac{I_P K_{VCO}}{2\pi N C_1}} \tag{3.34}$$

(3.34) shows that the thermal noise of R_P is band-pass filtered at PLL output, which is proportional to the square root of R_P. The increase of R_P would degrade PLL output phase noise, but recall from (3.22) that for the same phase margin, the increase of R_P leads to the reduction of capacitors C_1 and C_2. This capacitor reduction is much favored as those two capacitors normally occupy significant chip area. Therefore, there is a tradeoff between phase noise and chip area in the selection of R_P. One practical criteria is that the phase noise from R_P should not be larger than the one from VCO when the noise frequency is out of loop bandwidth. For PLL, when the frequency component is out of loop bandwidth, approximately speaking, the feedback loop is not functioning. Therefore, when calculating the phase noise contribution from R_P, we can ignore the loop and concentrate on the LPF and VCO only. The thermal noise on the VCO control voltage is thus given by,

$$\sqrt{\overline{V_{n-ctrl}^2}} = \frac{C_1}{C_1 + C_2}\sqrt{\frac{1}{1 + \left(\omega R_P \frac{C_1 C_2}{C_1 + C_2}\right)^2}} \cdot \sqrt{\overline{V_{n-R_P}^2}} \tag{3.35}$$

The narrow-band frequency modulation theory [10] states that when a sinusoid signal with amplitude A_m and frequency ω_m modulates a VCO, the output sidebands fall at ω_m away from the carrier frequency. The amplitude of the sidebands, when referred to the amplitude of carrier, is expressed as $A_m K_{VCO}/(2\omega_m)$. Therefore, the

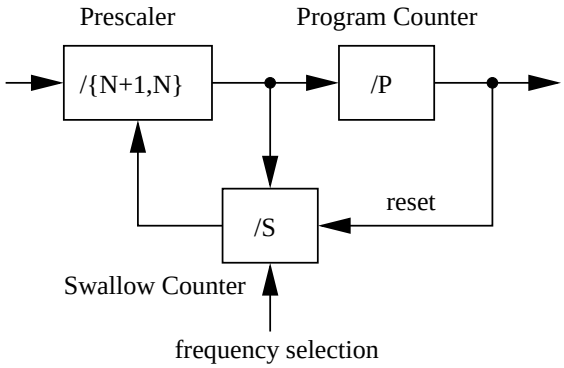


Fig. 15. Pulse swallow frequency divider

phase noise at VCO output due to R_P is given by,

$$PN_{R_P} = \left(\frac{C_1}{C_1 + C_2}\right)^2 \frac{1}{1 + \left(\omega R_P \frac{C_1 C_2}{C_1 + C_2}\right)^2} \cdot 2kTR_P \cdot \left(\frac{K_{VCO}}{2\omega}\right)^2 \tag{3.36}$$

C. Types of Frequency Synthesizer

1. PLL Based Frequency Synthesizer

It could be easily observed from the above study of PLL that PLL output frequency could be changed by setting frequency division ratio to different values. Therefore, PLL itself serve well as frequency synthesizer under some cases. Indeed, PLL based frequency synthesizer is the most widely used frequency synthesizer approach in modern wireless communications systems.

a. PLL Based Integer-N Frequency Synthesizer

PLL based integer-N frequency synthesizer consists of PLL with integer frequency division ratios. The advantages of this type of frequency synthesizer come from the simple yet robust implementation of integer frequency dividers.

Fig. 15 shows an example of integer frequency dividers, named as pulse swallow frequency divider. It consists of following blocks,

1. **Prescaler**: the prescaler divides its input either by $N + 1$ or N, which is controlled by the output from the swallow counter.

2. **Program counter**: the program counter takes the prescaler output and provides a fixed division ratio P.

3. **Swallow counter**: the swallow counter also takes the prescaler output but its division ratio S is variable, which is controlled by "Channel Selection" signal. Also the swallow counter would be reset by the output of the program counter.

Detailed analysis of the pulse swallow frequency divider [11] shows that the output is cycled for every $PN + S$ input cycles, resulting in the division ratio of $PN + S$.

The main drawback of the integer-N frequency synthesizer is its limited bandwidth, low settling speed and high close-in output phase noise. As the PLL output frequency is the integer multiples of the reference frequency, the finest PLL output frequency change equals to the reference frequency. Therefore, the required frequency spacing sets the upper-limit of the reference frequency. [9] mentions that stability concern demands the type II PLL loop bandwidth to be less than one tenth of the reference frequency. As a result, this rather limited loop bandwidth slows down the settling and allows more phase noise contribution from VCO.

b. PLL Based Fractional-N Frequency Synthesizer

The upper-limit of the reference frequency in integer-N frequency synthesizer is relaxed in fractional-N frequency synthesizer, as the smallest frequency step can be a fraction of the reference frequency for fractional-N frequency synthesizer.

A conceptual fractional divider is shown in Fig. 16. It consists of a $(N + 1)/N$ dual modulus divider and a modulus control unit. The modulus control unit sets the instantaneous division ratio to either N or $N + 1$ ratios so that the long term

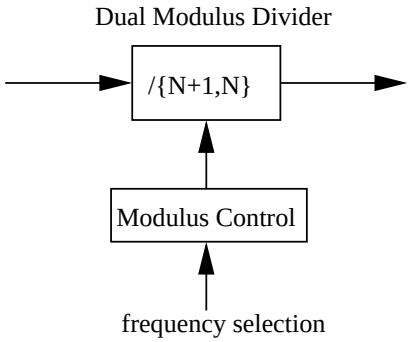


Fig. 16. Fractional frequency divider

equivalent division ratio is a fractional number between N and $N+1$. For example, if the division ratio is N for P cycles of output and $N+1$ for Q cycles of output, the number of cycles at input would be $PN+Q(N+1)$, and the equivalent division ratio is calculated as $[PN+Q(N+1)]/(P+Q) = N+Q/(P+Q)$.

Since the fractional division ratio is obtained not instantaneously but by averaging instant ratios over time, the spectrum of divider output is full of spurious tones, resulting in so called fractional spurs at PLL output. This problem is much severe when the modulus control unit provides a periodic control signal, or in other words, P and Q are constant over time. Under such case, sidebands only 20 to 30 dB below the carrier amplitude could be found at PLL output. To address this issue, a $\Sigma\Delta$ modulator has been used as the modulus control unit. By randomizing the control output, $\Sigma\Delta$ modulator helps to transform the fractional spurs to random noise. The drawbacks of this $\Sigma\Delta$ modulator approach are the increased complexity, die area and power consumption.

2. Direct Digital Synthesizer

While PLL based frequency synthesizer relies on low speed feedback loop to provide accurate carrier frequency, direct digital synthesizer (DDS) generates carrier frequency very fast by removing the feedback loop. Shown in Fig. 17, DDS gener-

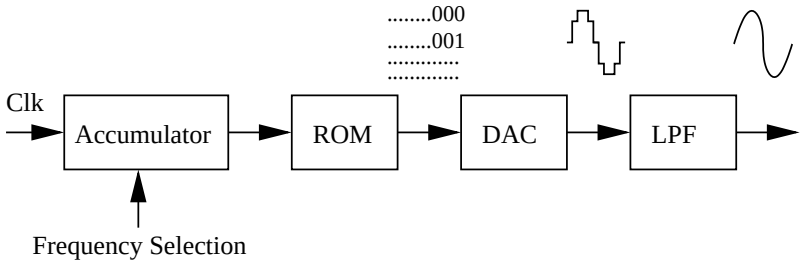


Fig. 17. Direct digital synthesizer

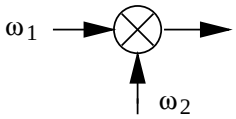


Fig. 18. Mixer based synthesizer

ates the signal in digital domain through an accumulator and a read-only memory (ROM), which is converted to analog waveform by digital-to-analog converter (DAC). Spurious harmonics at DAC outputs are filtered out by low pass filter (LPF). As no feedback is involved in synthesizing frequency, settling time is very fast. Indeed, it could be as fast as the order of gate delays. For example, DDS in [12] outputs frequency from DC to 75 MHz with settling time only 6.5 ns. Other merits include low phase noise, fine frequency steps and free of stability issue.

The most critical drawback of DDS is its low output frequency. To reconstruct the analog waveform correctly, according to Nyquist's sampling theorem, the clock frequency has to be no less than twice of the output frequency. In many RF applications, the carrier frequency has already reached the speed limit of the circuit, to have all the digital parts of DDS work at least twice the carrier frequency is challenging by any means. Furthermore, the non-idealities of DAC would degrade the output spectra purity.

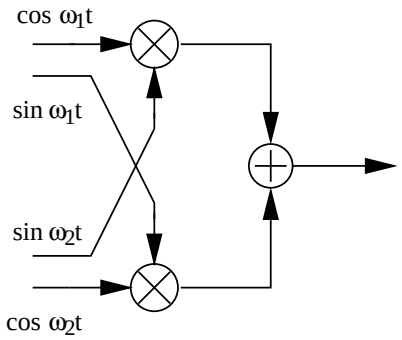


Fig. 19. SSB mixer

3. Mixer Based Synthesizer

A mixer is a device that could generate new frequencies by multiplying two input signals, as shown in Fig. 18. A simple mathematical representation of this operation is given by,

$$A_1 \cos\omega_1 t \times A_2 \cos\omega_2 t = \frac{A_1 A_2}{2}[\cos(\omega_1 - \omega_2)t - \cos(\omega_1 + \omega_2)t] \tag{3.37}$$

(3.37) shows that for two input frequencies, both their sum and difference frequencies appear at the output. This is not a desirable feature for synthesizer applications as carrier frequency has to be as pure as possible. Therefore, single-side band (SSB) mixer is adopted. Shown in Fig. 19, SSB mixer consists of two mixers and one adder. By mixing quadrature input signals and adding the two mixer outputs, only one frequency is left. This can be shown as,

$$A_1 \cos\omega_1 t \times A_2 \sin\omega_2 t + A_1 \sin\omega_1 t \times A_2 \cos\omega_2 t = A_1 A_2 \sin(\omega_1 + \omega_2)t \tag{3.38}$$

There are several advantages in using mixer to generate carrier frequency. First, as the carrier frequency is decomposed to two frequencies, each could be treated differently. Some tradeoffs mentioned in the previous synthesizer designs could be relaxed. For example, as shown in Fig.20, the overall frequency synthesizer is a

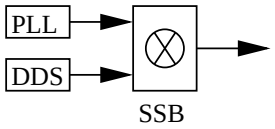


Fig. 20. A frequency synthesizer composed of DDS and mixer

hybrid of PLL, DDS and SSB mixer. The two inputs are generated by PLL and DDS each. PLL is used to output a fixed but high frequency signal, while DDS is used to output a variable but low frequency. In this way, for PLL, large loop bandwidth could be adopted to suppress the close-in VCO phase noise without the limit of the frequency spacing; for DDS, power consumption is dramatically reduced as the output frequency is much lowered. Another advantage is that the frequency generation could be fast. As there is no feedback loop involved in mixer, the output is settled just on the order of RC constant.

The primary issue of mixer based frequency synthesizers is the signal purity degradation at mixer output. This is mainly because of the nonlinear operation of mixer. In practice, not only the fundamental frequencies of the inputs signals, but also their DC and harmonic components would be possibly multiplied. Therefore, for input frequencies ω_1 and ω_2, output contains frequencies at $n\omega_1 \pm m\omega_2$, where n and m are integers. While a SSB mixer could ideally cancel out half of those sidebands, the remaining sidebands still exists. Also, the cancellation is indeed limited by the imbalance of phase and magnitude between quadrature signals and the mismatch between the two mixer cells.

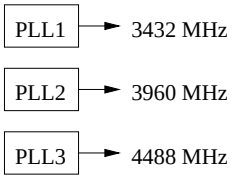


Fig. 21. Architecture of three-PLL approach for UWB frequency synthesizer

D. The Proposed Frequency Synthesizer Architecture

1. Existing Solutions

As stated in Section C of Chapter III, PLL alone could serve as a Frequency synthesizer, which is widely used in many applications. However, this approach faces the fundamental problem for UWB. The MBOA standard demands a frequency hopping time of only 9.5 ns. Typical PLLs take several hundred input cycles to settle. In order to settle the loop within 9.5 ns, the reference frequency must impractically be in the order of tens of GHz. Therefore, PLL alone can not be to used as frequency synthesizer in UWB applications. DDS approach is also not suitable as it can not handle the desired high frequency output.

Razavi et al proposed a three-PLL approach [6], as shown in Fig. 21. In this approach, each of the three independent PLLs is used to generate one of the three required center frequencies. Instead of changing the output frequencies of the PLLs, the hopping of those three frequencies are done by switches, which are incorporated in the mixers in the receiver signal path that are not shown here. As switches operate at very high speed, the 9.5 ns hopping time is easily met. Although straightforward, the drawbacks are also obvious. The silicon area are increased dramatically. What is more, the potential frequency pulling might drive the PLLs into malfunction.

TI proposed an approach as a combination of one PLL and several single side band (SSB) mixers [13]. Similar ideas are found in [7,8]. The diagram of this approach

is shown in Fig. 22. It exploits the fact that the new frequencies could be generated from two frequencies being mixed (multiplied) in mixer. The three center frequencies thus could be obtained by mixing the frequency from the PLL with the frequencies which is the difference frequencies from the PLL frequency to the center frequencies. The difference frequencies may be obtained from the PLL output frequency by using a combination of frequency dividers and SSB mixers. In TI's approach, the PLL outputs constant 4224 MHz frequency. Frequency synthesis is performed outside of the PLL. The band #1 center frequency 3432 MHz is generated by mixing 4224 MHz with 792 MHz. The 792 MHz frequency is generated by mixing 528 MHz and 264 MHz, which are obtained by using divider-by-8 and divider-by-16, respectively. The center frequencies for band #2 and #3 can be generated by mixing 4224 MHz with 264 MHz. As PLL only needs to settle down at start-up and produces a constant frequency, the unrealistic fast settling time requirement of PLL is eliminated. The problem of using SSB mixers to generate desired frequencies is related to the non-linearity operation in SSB mixers, which produces spurs as cross-products of the input harmonics. Since the image frequencies are canceled out at SSB mixer output in the first order, and the high order harmonics can be ignored as they normally have much less amplitudes than the fundamental one, there are several harmful cross-products in TI's architecture that needs special attention. One such harmful cross-product is $4224 - (528 + 5 * 264) = 2376\ MHz$. Others include $4224 - (-3 * 528 + 264) = 5544\ MHz$ and $4224 + 3 * 264 = 5016\ MHz$. Those spurs corrupt the received signal by transferring the high power signals in 2.4 GHz and 5 GHz ISM band to baseband. To solve the spur problem of SSB mixers, van de Beek et al [7] managed to reduce the number of SSB mixers by proposing a frequency synthesizer architecture, as shown in Fig. 23. As the three center frequencies are equally spaced, once the PLL generates band #2 center frequency 3960 MHz, the middle of the those three center frequencies,

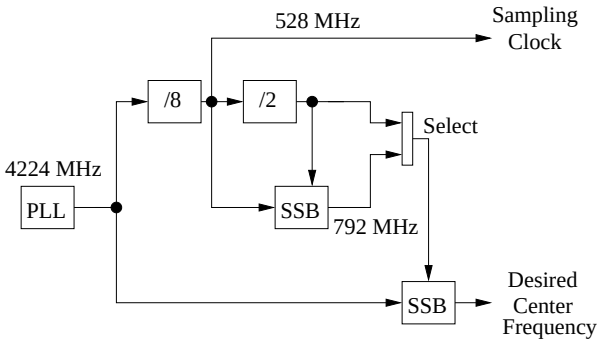


Fig. 22. Architecture of one-PLL approach for UWB frequency synthesizer in [13]

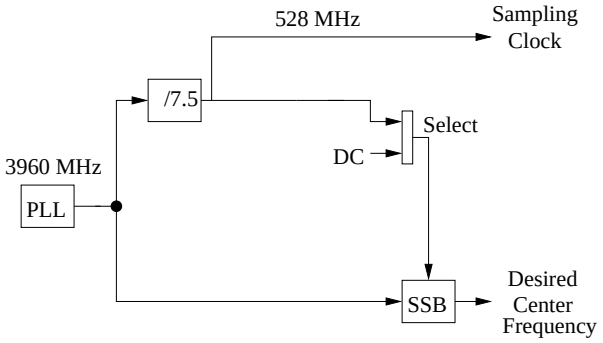


Fig. 23. Architecture of one-PLL approach for UWB frequency synthesizer in [7]

the other two center frequencies could be obtained by mixing the 3960 MHz frequency with 528 MHz frequency. Therefore, only one SSB mixer is needed. This approach, however, needs a fractional frequency divider with both inputs and outputs running at high frequencies. As to be explained in Chapter VI, it is very hard to design such frequency dividers in a robust and power-efficient way.

Roovers et al [8] presented another frequency synthesizer architecture, Fig. 24. Similar to [7], only one SSB mixer is used. But the problematic fractional divider is bypassed as the 528 MHz signal is generated by a second PLL. However, since the second PLL is totally independent to the first one, they do not share any block. The die area is almost doubled. Also, the additional power consumption is not negligible since this second PLL has to run at high frequency.

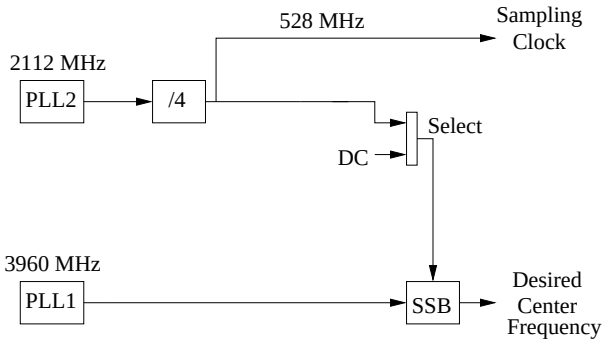


Fig. 24. Architecture of one-PLL approach for UWB frequency synthesizer in [8]

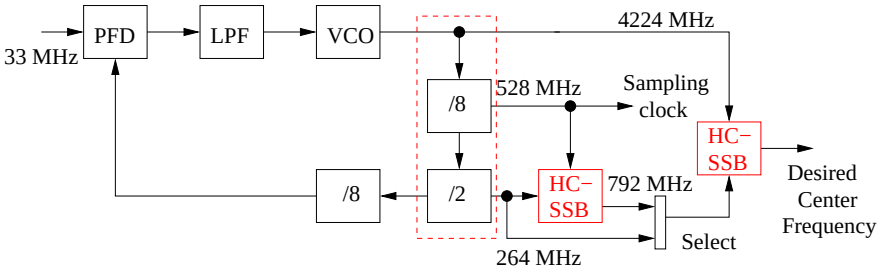


Fig. 25. Architecture of proposed UWB frequency synthesizer

2. Proposed Solution

To address the various issues associated with the existing approaches, a harmonic cancellation SSB mixer based frequency synthesizer is proposed for the UWB application. The system architecture of the proposed frequency synthesizer is shown in Fig. 25. It is similar to TI's approach, but there are two main differences. First, the frequency dividers generating 528 MHz and 264 MHz signals are shared between PLL and the frequency synthesis part. Therefore, the power consumption is reduced. Second, the conventional SSB mixers are replaced with the harmonic cancellation mixers. The harmonic cancellation SSB mixers cancel the cross-products of the third and fifth harmonics, which are the sources for the harmful spurs mentioned above.

The advantages of the proposed architecture is listed below,

1. The silicon area are saved by using only one PLL and sharing divide-by-8 and

divide-by-2 circuits.

2. The PLL only needs to output a constant frequency, eliminating the unrealistic fast settling requirement.

3. The frequency switching time could be very fast as it is only limited by the settling of parasitic capacitances at the switch outputs.

4. The harmful spurs from SSB mixer non-linearity are canceled out by using harmonic cancellation SSB mixers.

CHAPTER IV

PLL DESIGN

A. System Design

The relaxation of settling time requirement virtually allows us to choose any reference available. But the goal of full chip integration still demands fast reference if possible. This is because reference frequency is inversely proportional to loop filter time constant. Thus, 33 MHz is chosen as the reference frequency, leading to the division ratio of 128. For the same reason, the resistor R_P in the loop filter needs to be as large as possible, since the area of resistor is normally much smaller than that of capacitor. But the upper limit of resistor value is set by its phase noise contribution, which should not be larger than that of VCO.

The design of the PLL system starts from the given parameters shown in Table III, and the design procedure is given as follows.

1. **Calculation of** R_PC_P: derived from (3.22), R_PC_P is given by,

$$R_PC_P = \frac{\sqrt{m/\tan PM - (m/\tan PM)^2 - 4(m+1)}}{4\pi f_u} \tag{4.1}$$

   Using the numbers from Table III, $R_PC_P = 0.73 \cdot 10^{-6}$.

2. **Calculation of** R_P: We specify the phase noise due to R_P as -114 dBc at 1

Table III. Given parameters to initialize PLL system design

f_{ref}	N	f_u	PM	$m = C_P/C_2$
33 MHz	128	550 KHz	60°	16

MHz offset. According to (3.36), R_P is given by,

$$R_P = 10^{-PN/10}\left[1+\left(\frac{R_P C_1 2\pi f_n}{1+m}\right)^2\right]\cdot\left(\frac{m+1}{m}\right)^2\cdot\left(\frac{4\pi f_n}{K_{VCO}}\right)^2\cdot\frac{1}{2kT} \quad (4.2)$$

where PN is phase noise in dBc. Therefore, $R_P = 4.4\Omega$.

3. **Calculation of** C_P: with $R_P C_P$ and R_P known, C_P equals to 165 pF.

4. **Calculation of** C_2: $C_2 = C_P/m = 10.4\ pF$.

5. **Calculation of** I_{CP}: with all other parameters are set before this step, I_{CP} has to meet the following equation,

$$|H_C(s)|_{s=j2\pi f_u} = 1 \quad (4.3)$$

The calculation of I_{CP} from (4.3) entails the aid of numeric solution, which results in $I_P = 137\ \mu A$.

To verify the PLL stability, R_P, C_P, C_2, I_{CP}, N and K_{VCO} are input to a PLL behavioral model in Cadence Spectre. Fig. 26 shows the frequency response of the PLL in open loop, which confirms f_u and PM to be desired values. The transient step response of the PLL in closed loop is shown in Fig. 27.

B. PFD and CP Design

1. PFD Design

a. XOR Based PD

Logic gate XOR could be used as a phase detector, as shown in Fig. 28. The output of XOR is complementary, i.e. from "-1" to "+1". The transfer function of XOR PD could be graphically shown in Fig. 29.

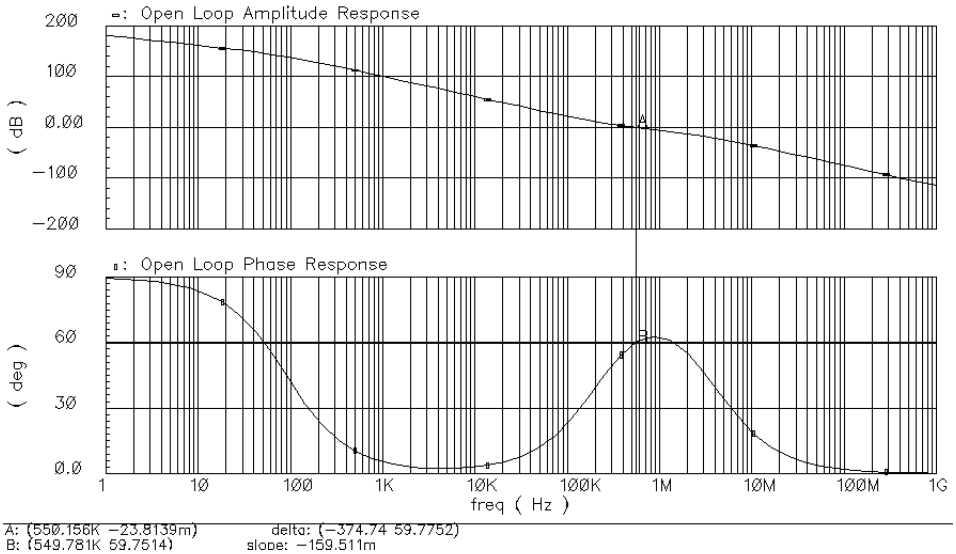


Fig. 26. Frequency response of the open-loop PLL

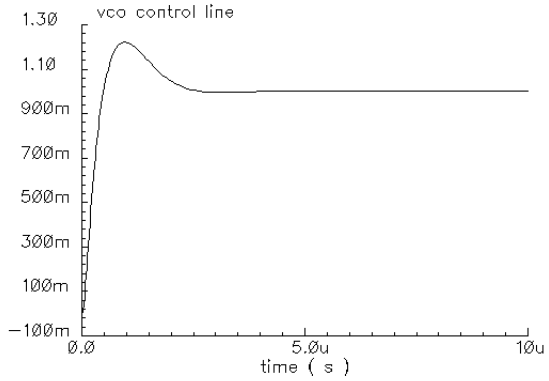


Fig. 27. Step response of the closed-loop PLL

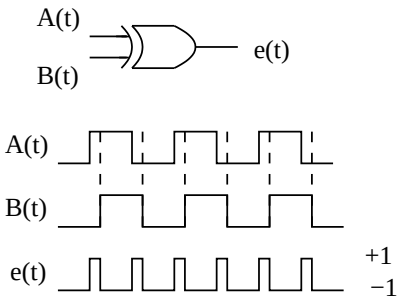


Fig. 28. XOR based PD

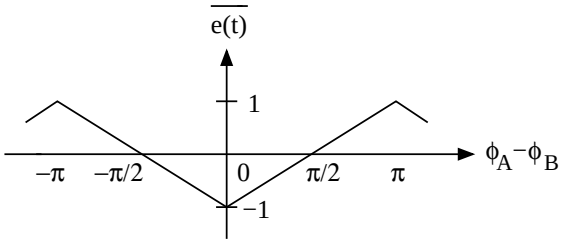


Fig. 29. Transfer function of the XOR based PD

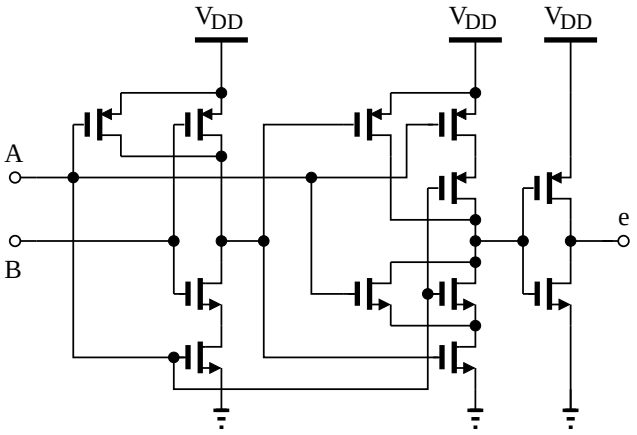


Fig. 30. An XOR based PD implementation

An example of XOR PD implementation is shown in Fig. 30. The simplicity of XOR PD ensures that its operation speed could be fast, making itself suitable for high speed applications.

The primary drawback of XOR PD is its inability to detect frequency difference. This is explained by revisiting the transfer function curve in Fig. 31. As any frequency difference exists, the phase difference would be accumulated either in a positive direction (for reference frequency slower than divided frequency) or in a negative direction (for reference frequency faster than divided frequency). But Fig. 31 shows that as the transfer function is symmetrical over y-axis, it fails to differentiate the polarity of phase difference, and thus the frequency difference. Another issue is that the inherent reference spur appears at XOR PD output. When PLL is locked, the

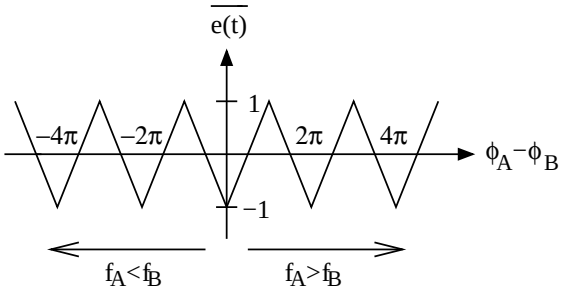


Fig. 31. A revisit of the XOR based PD transfer function

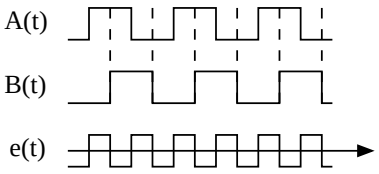


Fig. 32. XOR input/output waveforms when PLL is locked

average of XOR PD output is zero. However, as shown in Fig. 32, this zero voltage is averaged from a square wave with twice the reference frequency. Therefore, the pole of LPF has to be low enough to attenuate this reference spur, which slows down the settling speed and jeopardizes the loop stability. The third issue is that the XOR PD transfer function is sensitive to duty cycle distortion (DCD) of input signals. An example of such DCD effect is shown in Fig. 33. As could be seen, the linear region is shrunk and the phase of zero voltage output is deviated from $\pi/2$.

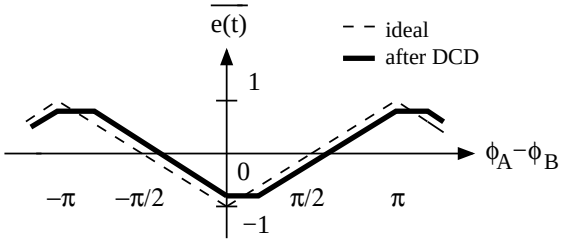


Fig. 33. DCD impact on the XOR based PD transfer funciton

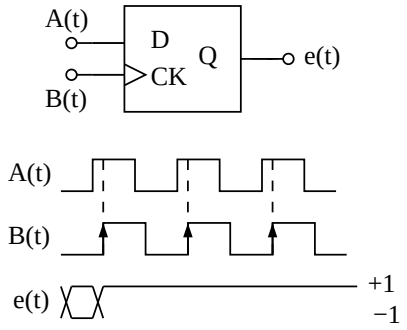


Fig. 34. DFF based PD

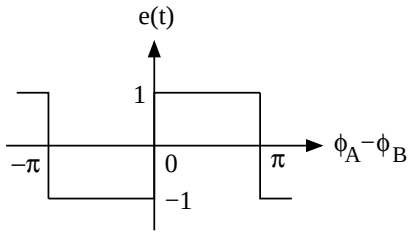


Fig. 35. Transfer function of the DFF based PD

b. DFF Based PD

A single D flip-flop (DFF) could also be used as a phase detector. Shown in Fig. 34, reference serves as a clock to sample divided clock. As long as reference leads divided clock, the output would be logic ONE. On the contrary, if reference lags divided clock, the output would be logic ZERO. Therefore, DFF PD operation is highly nonlinear, leading to the stability issue and uncertainty of phase error when PLL is settled down. The transfer function curve is shown in Fig. 35. Since when the phase difference goes to either positive direction or negative direction the average values are all zero, DFF PD also fails to detect frequency difference.

c. Tristate PFD

The frequency detection incompetence of XOR PD and DFF PD prevents themselves from many PLL applications, where initial VCO oscillation frequencies are far away

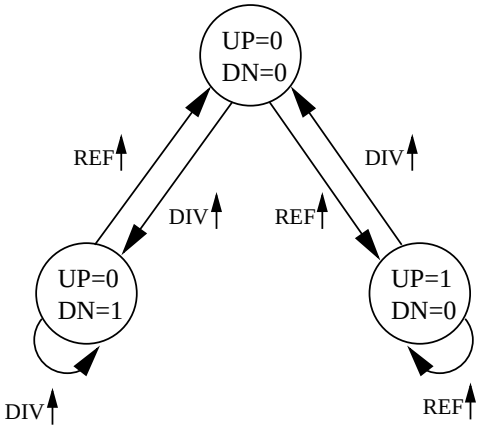


Fig. 36. State diagram of tristate PFD

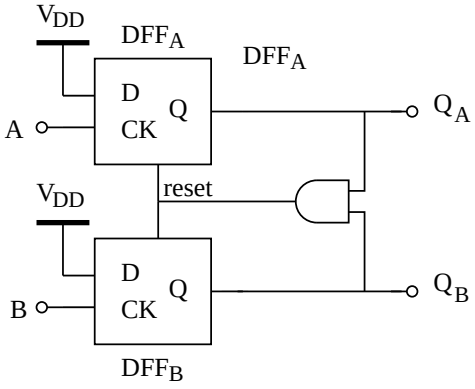


Fig. 37. A PFD implementation

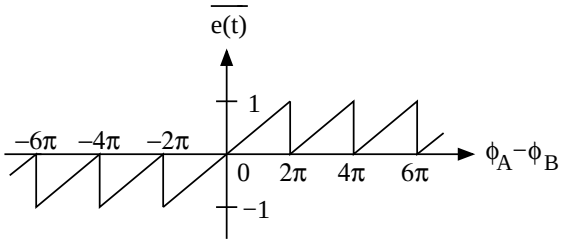


Fig. 38. Transfer function of the PFD

from references or PLL is expected to output large frequency range. On the contrary, tristate PFD is able to not only detect phase difference but also frequency difference. Fig. 36 shows the state diagram of the tristate PDF, whose operation is explained as follows. Assuming REF leads DIV, the rising edge of REF triggers DFF_A, resulting to UP is switched from 0 to 1 and DN remains 0. After that, UP will stay in 1 until the rising edge of DIV triggers DFF_A and UP is reset to 0 by the AND gate. Similar behavior happens when DIV leads REF. Therefore, the phase difference between REF and DIV is indicated by $UP - DN$. A circuit implementation of the PFD is shown in Fig. 37.

The transfer function curve is shown in Fig. 38, which explains the frequency detection of tristate PFD. The curve is unsymmetrical over y-axis and the output has the same sign as the phase difference. Therefore, the output would be in opposite polarities between positive and negative frequency difference. An alternative way to understand the frequency detection is to assume $f_{REF} > f_{DIV}$, then REF always leads DIV, resulting positive pulses appearing at UP while DN stays at 0. When $f_{REF} < f_{DIV}$, REF always lags DIV, resulting positive pulses appearing at DN while UP stays at 0. Thus, the average of $UP - DN$ suggests the frequency difference.

In practice, tristate PFD suffers from two issues. The first one is so called "dead zone". When REF and DIV phase difference is close to zero, the width of the output pulses would approach to minimal, which is set by the feedback delay from AND gate

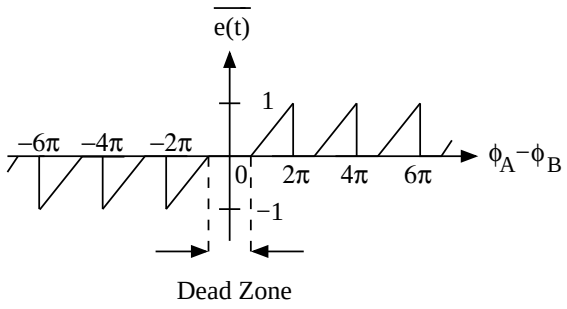


Fig. 39. Dead zone in the PFD

input to output. However, the charge pump may not be able to detect such narrow pulses, resulting to no current injecting to LPF, a scenario the same as when phase difference is zero. The transfer function curve under dead zone effect is shown in Fig. 39. As the PFD gain is down to zero in dead zone, the PLL loop would not be functional and there would be unpredictable phase error between the two inputs . One straightforward solution is to add more delays in the feedback path to increase the propagation of reset, as shown in Fig. 40. The side effect of this approach is the increased CP-mismatch-current induced reference spur. Another problem with PFD is the skew between two output signals arriving at CP input. CP commonly needs the polarity of output UP to be inverted while output DN polarity remains the same, meaning the two paths from tristate outputs to CP inputs are different. As the phase is compared every cycle of reference, the fluctuation due to the skew would also appear at VCO control line in the period the same as reference, producing reference spurs. One way to decrease this skew is to add a complementary pass gate in the path without inverter, as shown in Fig. 40. But the skew can not be diminished even in the first order, as the paths are still different. Another way to suppress the effect of skew is to design a PLL with small loop bandwidth, which is limited by the requirement of settling time.

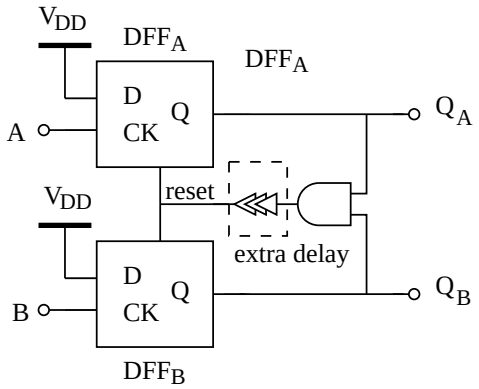


Fig. 40. Extra delay cells to remove dead zone

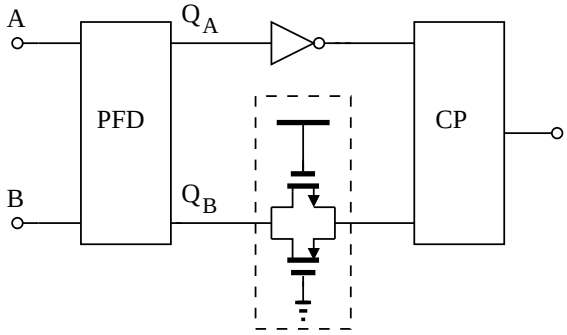


Fig. 41. Suppression of PFD skew

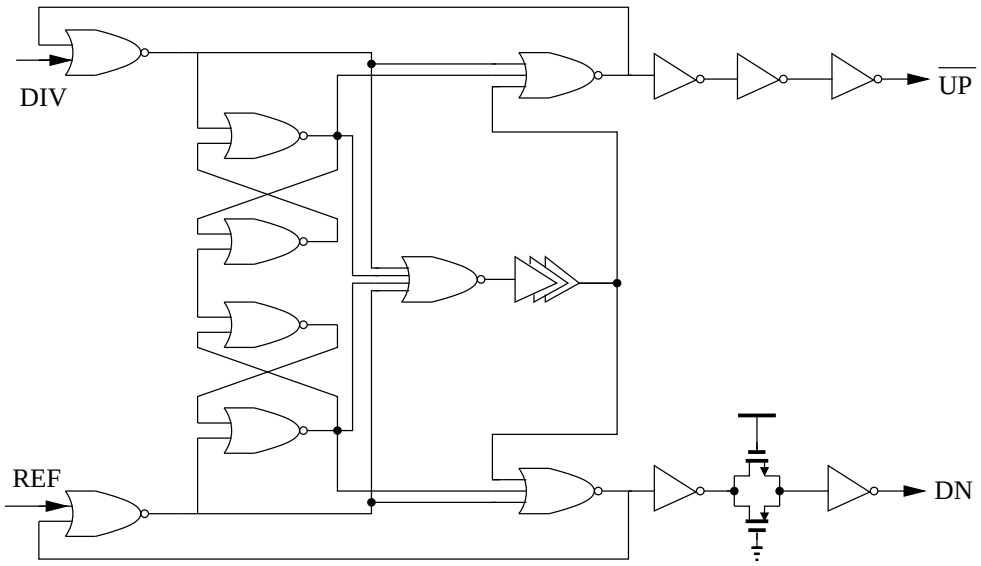


Fig. 42. PFD schematic

d. PFD Schematic

Fig. 42 shows the block level schematic of PFD. All the blocks use standard CMOS logic circuits.

2. CP Design

a. CP Non-idealities

Current leakage exists when both UP and DN currents are expected to be off. The presence of the current leakage causes the VCO control voltage off from its desired value. A certain amount of phase error has to be presented to compensate the control line offset, as shown in Fig. 43. The immediate consequence is the generation of reference spurs, the value of which is calculated as follows. Ignoring reset time, the waveform of CP output current is shown in Fig. 44. When PLL is locked, the averaged current of one period should be zero. Therefore, the time length t_{CP} for charge pump current I_{CP} has to meet the following condition,

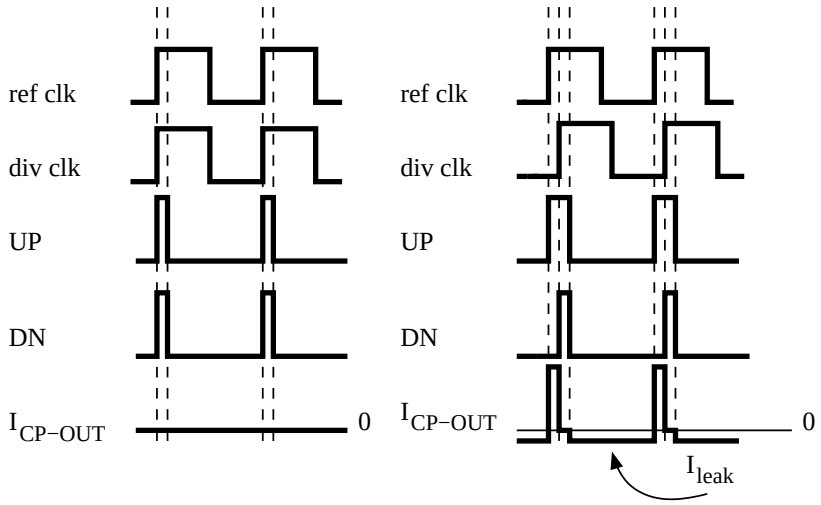


Fig. 43. Current leakage of CP

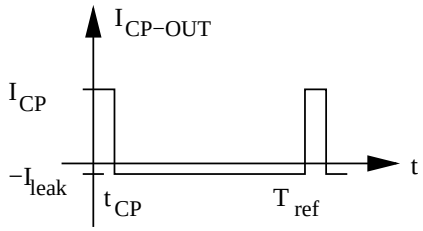


Fig. 44. Simplified CP output waveform under current leakage

$$I_{CP} \cdot t_{CP} - I_{leak} \cdot (T_{ref} - t_{CP}) = 0 \tag{4.4}$$

which results in $t_{CP} = T_{ref} \cdot I_{leak}/(I_{CP} + I_{leak})$. Thus CP output current $I(t)$ over one reference period could be expressed as,

$$I(t) = \begin{cases} I_{CP} & \text{if } 0 \leq t < t_{CP} \\ I_{leak} & \text{if } t_{CP} \leq t < T_{ref} \end{cases} \tag{4.5}$$

where T_{ref} is the reference period. Using Fourier transform, $I(t)$ could be treated as a sum of harmonics of reference. The coefficient C_N for N_{th} harmonic is calculated as,

$$C_N = -\frac{I_{CP} + I_{leak}}{2\pi N} \left[\sin 2\pi N \frac{I_{leak}}{I_{CP} + I_{leak}} + 2\sin^2 \left(\pi N \frac{I_{leak}}{I_{CP} + I_{leak}} \right) \right] \tag{4.6}$$

Assuming $I_{leak} \ll I_{CP}$, C_N could be approximated as,

$$C_N \approx -\frac{I_{leak}}{N} \tag{4.7}$$

As the loop bandwidth could only be one-tenth of the reference frequency, those harmonics contained in $I(t)$ are far out of loop bandwidth, which would only be attenuated by LPF. Thus, assuming LPF is second order, the amplitude of N_{th} harmonic appearing at VCO control line is expressed as,

$$A_N \approx -\frac{I_{leak}}{N^2} \frac{R}{f_{ref}/f_p} \tag{4.8}$$

where f_p is the pole of the LPF. Among all the harmonics, we are interested in the first order one, as it has the largest amplitude. Using narrow-band FM theory, the

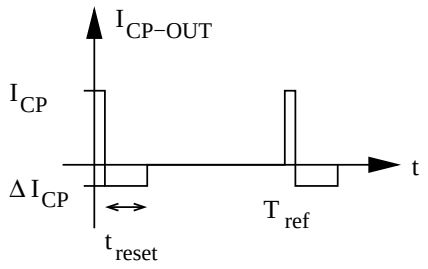


Fig. 45. Current mismatch of CP

amount of the reference spur is given by,

$$A_{leak-spur} = \frac{I_{leak} R K_{VCO}}{2 f_{ref} \cdot f_{ref}/f_p} \tag{4.9}$$

(4.9) shows that for a given ratio of f_{ref}/f_p and I_{leak}, the increase of f_{ref} helps to reduce this reference spur.

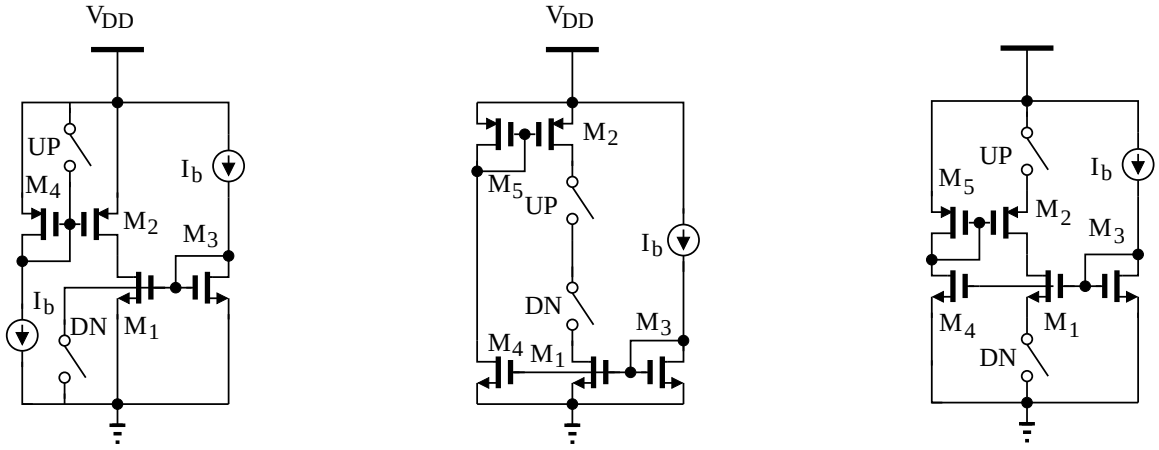
Current mismatch happens as UP and DN currents are not usually matched, which is due to the fact that the UP and DN currents are usually generated by PMOS and NMOS, respectively. Under this situation, the waveform of CP output current in steady state is shown in Fig. 45. Following the similar procedure as the leakage current case, the amount of the reference spur is determined by

$$A_{mis-spur} = \frac{\Delta I_{CP} R K_{VCO}}{2 f_{ref} \cdot f_{ref}/f_p} \cdot \frac{t_{reset}}{T_{ref}} \tag{4.10}$$

where ΔI_{CP} is the current difference between UP and DN current, t_{reset} is the reset time. (4.10) shows that for a given ΔI_{CP} and reference frequency, to minimize $A_{mis-spur}$, reset time has to be minimized.

b. CP Architectures

Single ended CPs are widely used as they do not need an additional loop filter, which normally demands much chip area. The three typical topologies are shown in Fig. 46. Those CPs are different in the various positions where switches are placed .



(a) G-SCP (b) D-SCP (c) S-SCP

Fig. 46. Three types of single-ended CP

G-SCP in Fig. 46(a) has switches placed at the gate of the current mirror transistors M_1 and M_2. One of the main drawbacks of G-SCP is leakage current. When DN switch is switched to ON state to turn off M_1, the gate voltage of M_1 is not virtually ground as the bias current has to flow through the ON resistance of DN switch. Therefore, to minimize the leakage current, the bias current should be minimized. However, when the bias current is decreased, the switching time is enlarged as the $g_{m3,4}$ of the bias transistors M_3 and M_4 are decreased. Another issue is the charge sharing between drain capacitances of M_1 and M_2, and the loop filter capacitors. This is originated from the fact that the V_{GS} of both M_1 and M_2 are changed between ON and OFF states. Fig. 46(b) shows D-SCP, where switches are placed at the drain of the current mirror transistors. Similar as G-SCP, D-SCP suffers from charge sharing problem. Also the switching of D-SCP is not fast since the switches are directly connect to the loop filter capacitors. Another problem of D-SCP is the existence of large current spike. After DN switch is turned on, M_1 is initially in triode region, leading to a low impedance path between the output and ground, which draws large

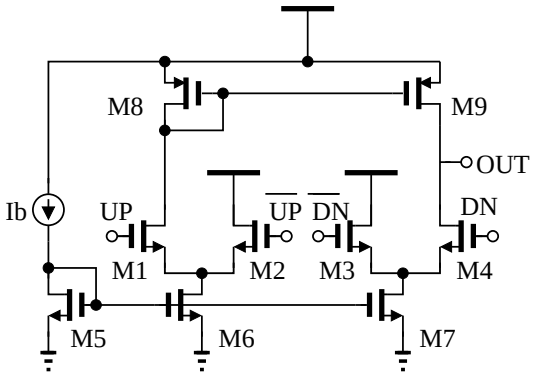


Fig. 47. A differential-ended CP

amount of current. S-SCP in Fig. 46(c) has several advantages over the other two. First, there is no compromise in choosing bias current between leakage and switching time as in G-SCP. Bias current could be low since bias transistors are not connected to switches and thus do not affect switching time. In the mean time, S-SCP shows the smallest leakage current. Since the gate of DN switch could be virtually ground at OFF state, the leakage current is smaller than G-SCP. Also in OFF state, the output impedance of S-SCP could be higher than D-SCP, as it comes from a series connection of two OFF transistors instead of one in D-SCP. Furthermore, large spike current does not exist in S-SCP, since M_1 and M_2 stay in saturation. The common issue of the three architectures discussed above is that the UP and DN switches are of different types, i.e. PMOS and NMOS for UP and DN, respectively, leading to the timing skew. Such skew could be eliminated by using NMOS switch only, as shown in Fig. 47. This architecture can be regarded as an extension of G-SCP in the sense that switches $M_1 - M_4$ are placed at the drains of current mirror transistors. However, the switching speed is improved because of the utilization of current switching. The main drawback is the increased power consumption as current is always on.

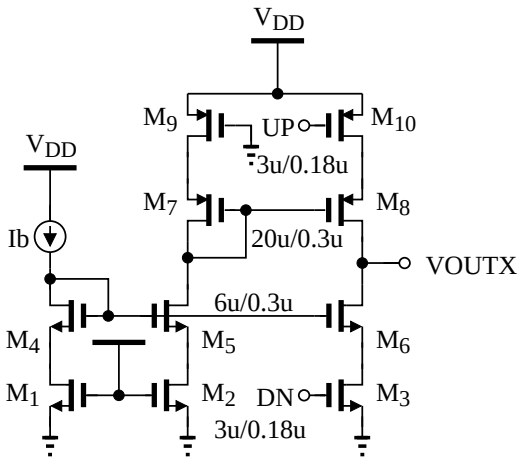


Fig. 48. Implemented CP

c. CP Implementation

Several considerations directed us to implement CP in S-SCP configuration. First, the CP needs to be single-ended to save chip area by using only one loop filter. Second, the CP has to operate in a relatively high speed with small power consumption.

The schematic of the implemented CP is shown in Fig. 48. M_3 and M_{10} are DN and UP switches, respectively. $M_4 - M_8$ serve as current mirror. M_1, M_2 and M_9 are used to improve current matching. UP and DN currents are set to be $137\mu A$ nominal. But as Fig. 49 shows, both currents are varied with output voltage V_{CPOUT}. When V_{CPOUT} is between 0.6 V and 1.2 V, current mismatch is within $\pm 5\%$ of the nominal value. In this region, the current mismatch induced reference spur is calculated as -45 dBc according to (4.10). The leakage current is 5 nA, which introduces -76 dBc reference spur according to (4.9).

C. PLL Implementation and Simulation

The whole PLL is integrated in one chip. Post-layout simulations were performed with results shown in Fig. 50. The step response matches well with the behavior

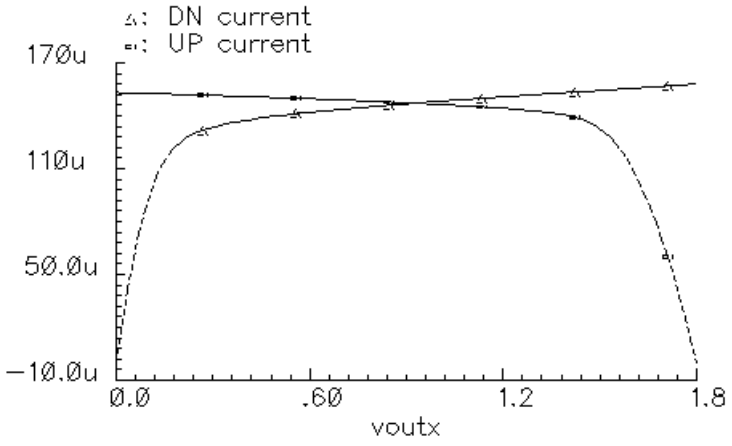


Fig. 49. Simulated UP/DW current over output voltage

simulation one in Fig. 27. The reference spur is -56 dBc below the carrier.

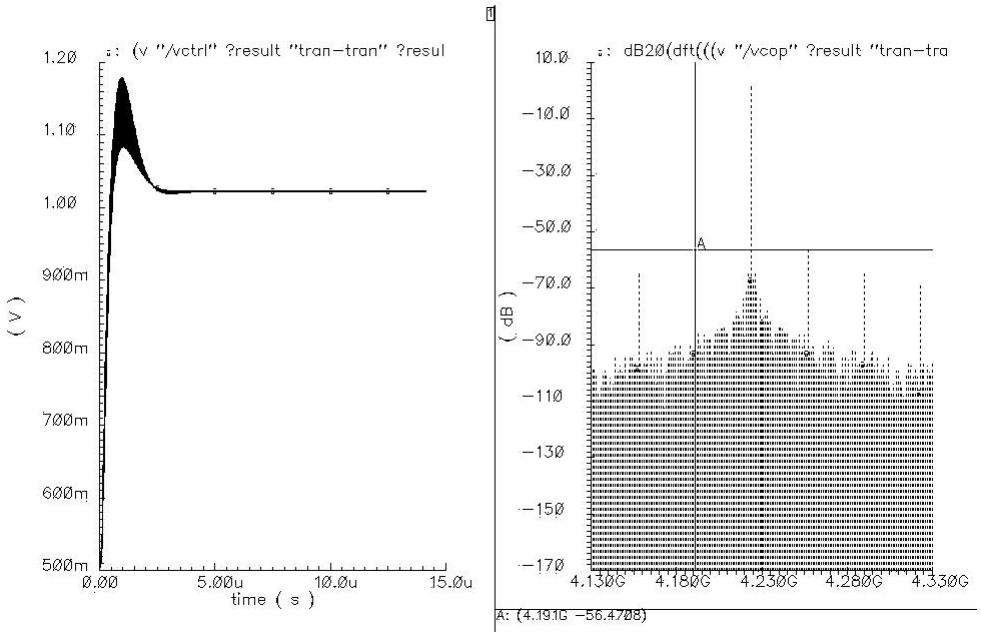


Fig. 50. PLL simulation results

CHAPTER V

HARMONIC CANCELLATION MIXER

A. Introduction

1. Mixer Basics

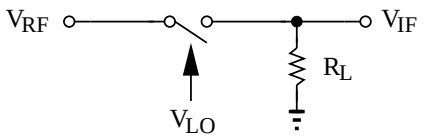


Fig. 51. A conceptual mixer diagram

Mixer achieves frequency conversion by multiplying its two input signals. The operation of mixer could be explained in a conceptual diagram shown in Fig. 51[1]. Here switch SW serves as a simple mixer, which is controlled by V_{LO}. While SW is ON, the other input signal V_{RF} passes to the output as at the port; while SW is OFF, the output is zero. Assuming V_{RF} is a sinusoid signal as $A\sin(2\pi f_{RF}t)$, the mathematical representation of $V_{IF}(t)$ is expressed as,

$$V_{IF}(t) = \begin{cases} A\sin(2\pi f_{RF}t), & \text{if } (k-1)\dfrac{1}{f_{LO}} \le t < (k-1)\dfrac{1}{f_{LO}} + \dfrac{1}{2f_{LO}} \\ 0, & \text{if } (k-1)\dfrac{1}{f_{LO}} + \dfrac{1}{2f_{LO}} \le t < k\dfrac{1}{f_{LO}} \end{cases} \tag{5.1}$$

where k is positive integer.

[1]To be consistent with other publications [11], the switch control port is called LO port, whose input is called RF port and its output is called IF port

Using Fourier series, $V_{IF}(t)$ could also be expressed as,

$$V_{IF}(t) = A\sin(2\pi f_{RF}t)\left\{\frac{1}{2} + \sum_{k=1}^{\infty}\frac{1}{(2k-1)\pi}\cdot\cos[2\pi(2k-1)f_{LO}t]\right\} \tag{5.2}$$

$$= \frac{A}{2}\sin(2\pi f_{RF}t) + \frac{A}{2}\sum_{k=1}^{\infty}\frac{1}{(2k-1)\pi}\cdot\cos\{2\pi[f_2 \pm (2k-1)f_{LO}]t\} \tag{5.3}$$

(5.3) shows that this conceptual mixer output contains frequency components as f_{RF} and $|f_{RF} \pm (2k-1)f_{LO}|$. In reality, $V_{f_{LO}}$ contains f_{LO} and its harmonics mf_{LO}; $V_{f_{RF}}$ is not exactly 50% duty cycle, meaning it contains not only odd harmonics but also even ones. Therefore, the practical mixer generates various cross products of its two input signals and their harmonics, expressed as $|mf_{LO} \pm nf_{RF}|$. On the other hand, since mixer serves to generate desired carrier frequencies in this design, spurious frequency components at mixer should be minimized.

2. Mixer Architectures

a. Passive Mixer and Active Mixer

Passive mixer replaces SW in Fig. 51 with a MOS transistor. The main drawback is the voltage loss from RF port to IF port. Even ignoring the on-resistance of the MOS switch, as (5.3) shows, the amplitude of $f_{LO} \pm f_{RF}$ at IF port is $1/2\pi$ smaller than that of f_{RF} at RF port. While this voltage loss may not be an issue if the desired output frequency is low, since loss is easily compensated by subsequent circuits; it is a critical drawback when desired output is at high frequency, where boosting signal levels demands considerable power consumption. Active mixer includes gain-stage to boost the output signal level. An example of active mixer is shown in Fig. 52. In this mixer, SW is implemented by two current switch M_1 and M_2, which controls current flowing either from R_1 or R_2. $V_{f_{RF}}(t)$ is converted to current through g_m stage M_3, then the current would be transformed to voltage at the output through R_1 or R_2.

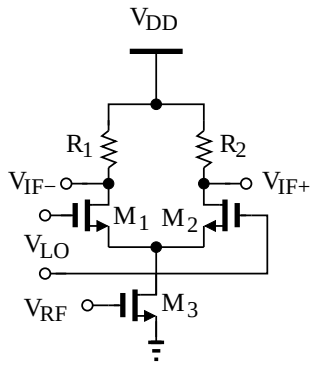


Fig. 52. Single balanced mixer

By using Fourier series, assuming $R_1 = R_2 = R_L$, $V_{IF+}(t)$ and $V_{IF-}(t)$ are calculated as,

$$V_{IF+}(t) = [I_{DC} + V_{f_{RF}}(t) g_m R_L] \left\{ \frac{1}{2} + \sum_{k=1}^{\infty} \frac{1}{(2k-1)\pi} \cdot \cos[2\pi(2k-1) f_{LO} t] \right\} \quad (5.4)$$

$$V_{IF-}(t) = [I_{DC} + V_{f_{RF}}(t) g_m R_L] \left\{ \frac{1}{2} - \sum_{k=1}^{\infty} \frac{1}{(2k-1)\pi} \cdot \cos[2\pi(2k-1) f_{LO} t] \right\} \quad (5.5)$$

Therefore, the voltage conversion gain at each output side is $g_m R_L / 2\pi$. Immediately, a gain increase by twice is available by taking the difference of the two outputs. The main disadvantage of active mixer is its poor linearity. There are several approaches to improve the linearity. The first one is using source degeneration resistor, which comes with the decrease of conversion gain. Another approach is to increase over drive voltage of M_3, which results in the increase of current for the same W/L of M_3.

b. Single-Balanced Mixer and Double Balanced Mixer

The active mixer shown in Fig. 52 could also be categorized as single-balanced mixer because one of its input is differential and the other is single-ended. The major benefit of single-balanced mixer is the immunity of RF-IF feed-through, which is

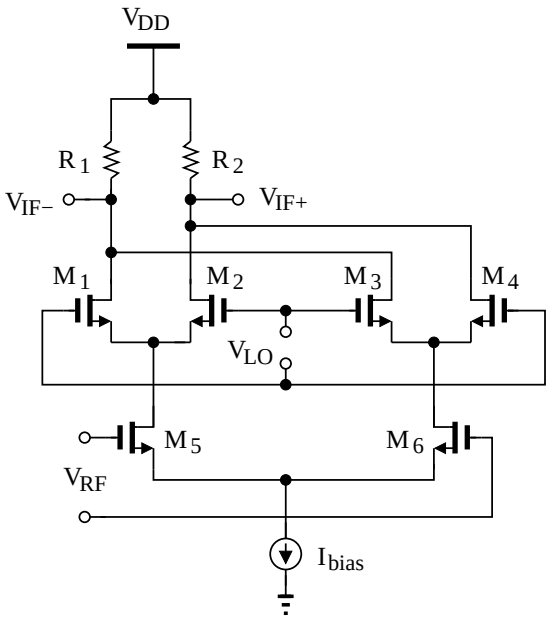


Fig. 53. Double-balanced mixer

made obvious by taking the difference of $V_{IF+}(t)$ and $V_{IF-}(t)$ as,

$$\begin{aligned} V_{IF}(t) &= V_{IF+}(t) - V_{IF-}(t) \\ &= 2[I_{DC} + V_{f_{RF}}(t) g_m R_L] \left\{ \sum_{k=1}^{\infty} \frac{1}{(2k-1)\pi} \cdot \cos[2\pi(2k-1) f_{LO} t] \right\} \end{aligned} \tag{5.6}$$

The LO-RF feed-through could be canceled in the first order by using double balanced mixer, as shown in Fig 53. In double balanced mixer, both LO and RF signals are differential. The differential output is expressed as,

$$V_{IF}(t) = V_{IF+}(t) - V_{IF-}(t) = 2V_{f_{RF}}(t) g_m R_L \left\{ \sum_{k=1}^{\infty} \frac{1}{(2k-1)\pi} \cdot \cos[2\pi(2k-1) f_{LO} t] \right\} \tag{5.7}$$

(5.7) shows that the differential output does not contain direct feed-through part from RF port, only the cross products of RF and LO fundamental frequency and even order harmonics are presented.

3. Harmonic Cancellation Concept and Considerations

a. Harmonic Cancellation Concept

Harmonic cancellation concept was first presented by [14], which focused only on canceling harmonic components from square wave. Here we extend it to arbitrary periodic wave. For a given periodic signal $f(t)$, it could always be expressed as a sum of fundamental frequency and its harmonics by using Fourier series. If the signal is differential with period T, it contains harmonics only in odd-orders as shown below,

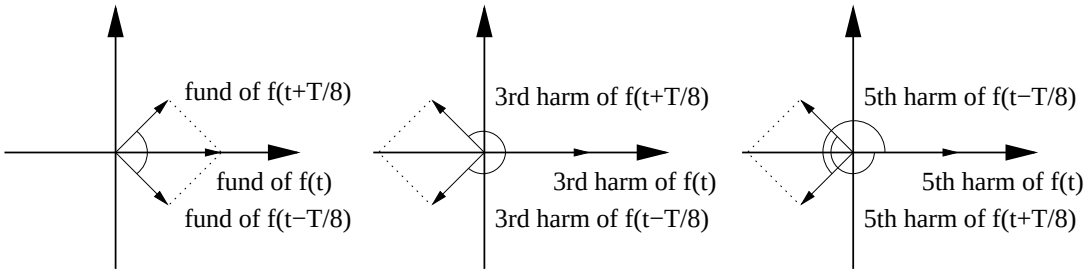
$$f(t) = A_1 \sin(\omega_n t + \phi_1) + A_3 \sin(3\omega_n t + \phi_3) + ...A_{2k-1} \sin[(2k-1)\omega_n t + \phi_{2k-1}] + ... \tag{5.8}$$

where $\omega_n = 2\pi/T$. Therefore, $f(t - \Delta t)$ is expressed as,

$$\begin{aligned} f(t - \Delta t) =& A_1 \sin(\omega_n t + \phi_1 - \omega_n \Delta t) + A_3 \sin(3\omega_n t + \phi_3 - 3\omega_n \Delta t) + ... \\ &+ A_{2k-1} \sin[(2k-1)\omega_n t + \phi_{2k-1} - (2k-1)\omega_n \Delta t] + ... \end{aligned} \tag{5.9}$$

(5.9) shows that for a certain time delay Δt, different harmonics see different phase shifts, as $(2k-1)_{th}$ harmonic sees phase shift of $(2k-1)\omega_n \Delta t$. Thus we postulate that when taking a sum of different time delayed versions of $f(t)$, some harmonics are canceled because they are added out-of-phase. Such a possible combination is shown below,

$$g(t) = \sqrt{2} f(t) + f\left(t - \frac{T}{8}\right) + f\left(t + \frac{T}{8}\right) \tag{5.10}$$



(a) Fundamental (b) $3rd$ order (c) $5th$ order

Fig. 54. Phasor diagram of harmonic cancellation

The $(2k-1)_{th}$ harmonic of $g(t)$ is calculated as,

$$
\begin{aligned}
& 2\sqrt{2}A_{2k-1}\left\{\frac{1}{2}+\frac{\sqrt{2}}{2}\cos\left[(2k-1)\frac{\pi}{4}\right]\right\}\sin[(2k-1)\omega_n t+\phi_{2k-1}] \\
&= \begin{cases} 2\sqrt{2}A_{2k-1}\sin[(2k-1)\omega_n t+\phi_{2k-1}] & \text{if } k=4m-3,4m \\ 0 & \text{if } k=4m-2,4m-1 \end{cases}
\end{aligned} \tag{5.11}
$$

where m is a positive integer. Therefore, $g(t)$ preserves $(8m-7)_{th}$ and $(8m-1)_{th}$ harmonics, while $(8m-5)_{th}$ and $(8m-3)_{th}$ harmonics are eliminated. In particular, the fundamental frequency is kept and the $3rd$ and $5th$ order harmonics are canceled. To understand this $3rd$ and $5th$ order harmonic cancellation in a more intuitive way, we use the phasor diagram shown in Fig. 54. A $T/8$ delay of $f(t)$ equals to a 45° phase shift of fundamental. The sum of $f(t-T/8)$ and $f(t+T/8)$ leads to an in-phase of fundamental referred to $f(t)$. On the contrary, as the sum of either the $3rd$ or the $5th$ order harmonics of $f(t-T/8)$ and $f(t+T/8)$ results 180° phase shift to $f(t)$'s with amplitude $\sqrt{2}$ larger. Therefore, when $\sqrt{2}f(t)$ are added with $f(t-T/8)$ and $f(t+T/8)$, the $3rd$ and $5th$ order harmonics are canceled.

This harmonic cancellation is very helpful to increase the linearity of $f(t)$ and we give reason as follows. The $3rd$ and $5th$ order harmonics are the most dominant

harmonics other than the fundamental one. This is because not only those two harmonics are the closest to the fundamental but also in general they present the largest amplitudes than others. Indeed, the $3rd$ harmonic alone is commonly used to characterize the linearity of various circuits by means of $HD3$.

b. Impact of Amplitude and Delay Mismatch

(5.11) shows that ideally the $3rd$ and $5th$ order harmonics are completely canceled. In practice, there are residues of those two harmonics due to mismatches of amplitude and delay between $f(t)$, $f(t-T/8)$ and $f(t+T/8)$. Particularly, we assume that the mismatches are mainly between $f(t)$ and $f(t \pm T/8)$, while we ignore the mismatches between $f(t-T/8)$ and $f(t+T/8)$. This is because $f(t)$ has to pass different gain stage than $f(t-T/8)$ and $f(t+T/8)$, and the nature of irrational number as $\sqrt{2}$ makes it impossible to implement this gain stage by a combination of identical stages as the ones for $f(t-T/8)$ and $f(t+T/8)$. To incorporate such mismatches, we express $\sqrt{2}f(t)$ as $\sqrt{2}(1+\alpha)f(t+\theta/\omega_n)$. The amplitudes of the fundamental, $3rd$ and $5th$ order harmonics appearing at $g(t)$ are calculated as,

$$\begin{aligned} A_{1-g} &= \sqrt{2}A_1\sqrt{(2+\alpha)^2 - 4(1+\alpha)\sin^2\theta} \\ &\approx 2\sqrt{2}A_1 \qquad \text{if } \alpha \ll 1 \text{ and } \theta \ll 1 \end{aligned} \tag{5.12}$$

$$A_{3-g} = \sqrt{2}A_3\sqrt{\alpha^2 + 4\sin^2\left(\frac{3}{2}\theta\right)} \tag{5.13}$$

$$A_{5-g} = \sqrt{2}A_5\sqrt{\alpha^2 + 4\sin^2\left(\frac{5}{2}\theta\right)} \tag{5.14}$$

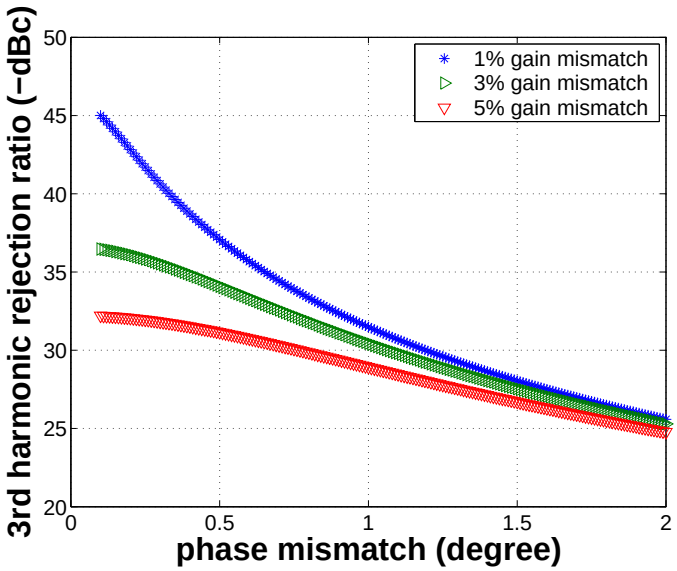


Fig. 55. Suppression of $3rd$ order harmonic with mismatch

Therefore, the suppression of the $3rd$ and $5th$ order harmonics referred to fundamental are expressed as,

$$Supp_{3rd} = \frac{1}{2}\sqrt{\alpha^2 + 4\sin^2\left(\frac{3}{2}\theta\right)} \tag{5.15}$$

$$Supp_{5th} = \frac{1}{2}\sqrt{\alpha^2 + 4\sin^2\left(\frac{5}{2}\theta\right)} \tag{5.16}$$

Figs. 55 and 56 shows the calculated $3rd$ and $5th$ harmonic suppression ratio over phase and amplitude mismatch.

B. Harmonic Cancellation Mixer Design

1. Harmonic Cancellation in Mixer

The harmonic cancellation idea could be applied to mixer. As mixer has two inputs, $V_{LO}(t)$ and $V_{IF}(t)$, harmonic cancellation could be performed on either of them. For

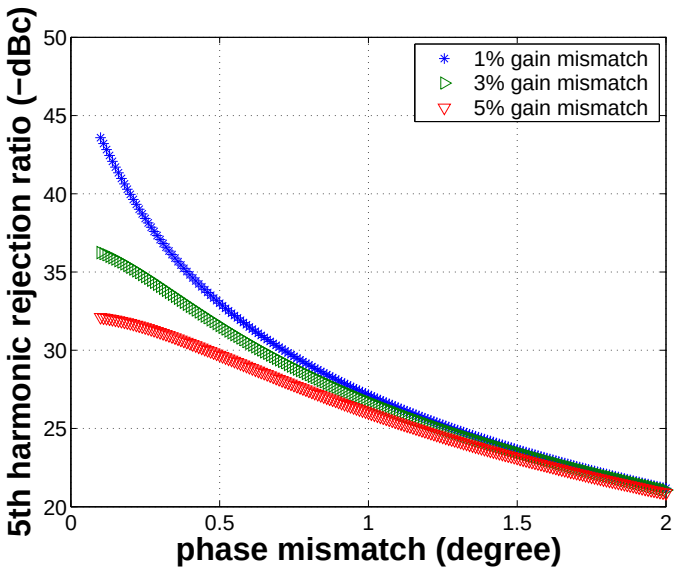


Fig. 56. Suppression of $5th$ order harmonic with mismatch

example, if harmonic cancellation can be performed on $V_{LO}(t)$, as shown below,

$$\begin{aligned} V_{IF}(t) &= V_{IF1}(t) + V_{IF2}(t) + V_{IF3}(t) \\ &= V_{LO}(t)\sqrt{2}V_{RF}(t) + V_{LO}(t)V_{RF}(t - T_{RF}/8) + V_{LO}(t)V_{RF}(t + T_{RF}/8) \\ &= V_{LO}(t)[\sqrt{2}V_{RF}(t) + V_{RF}(t - T_{RF}/8) + V_{RF}(t + T_{RF}/8)] \end{aligned} \tag{5.17}$$

(5.17) shows that a harmonic cancellation mixer (HCM) could be realized by a set of three sub-mixers, as presented in Fig. 57.

2. Harmonic Cancellation Mixer in the Frequency Synthesizer

a. Harmonic Cancellation Plan

Fig. 25 shows that there are two places of the frequency synthesizer where mixers are used. The first one is to generate 792 MHz signal from mixing 528 MHz and 264 MHz signals coming from frequency dividers of the 4224 MHz PLL. As the frequency dividers operate in digital fashion, both 528 MHz and 264 MHz signals contain no-

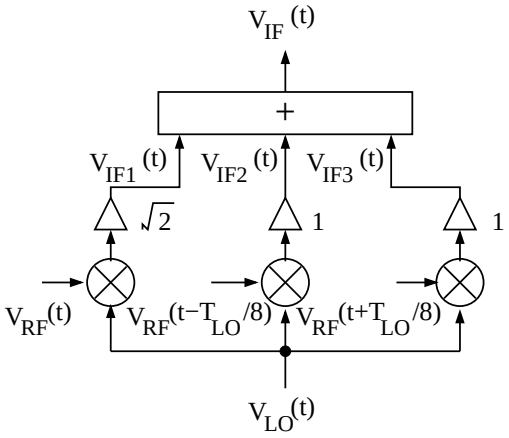


Fig. 57. A block diagram of a mixer with harmonic cancellation

ticeable harmonics and thus demand harmonic cancellation. But we do not plan to perform harmonic cancellation on both signals at this stage. The frequency synthesizer architecture shows that the 792 MHz mixer output would be directed to the 4224 MHz mixer, which, as explained later, also needs harmonic cancellation anyway. Therefore, we only need one signal undergo harmonic cancellation at the 792 MHz mixer and leave the other to be done at the 4224 MHz mixer. While some low pass filtering technique could be utilized to reduce the harmonics before signals reach mixer inputs, the harmonic reduction effect is not remarkable as every one pole only causes 20dB/Dec amplitude drop at most. Another reason that low pass filtering is not sufficient is that input signal levels have to be high enough to ensure large output amplitude, meaning the nonlinearity of mixer is not ignorable and external low pass filtering is not helpful to reduce harmonics generated inside the mixer.

As for 4224 MHz mixer, 4224 MHz signal does not need harmonic cancellation since the harmonics of 4224 MHz are far away from the desired output frequencies. On the contrary, the harmonics of 264/792 MHz signals, when mixed with 4224 MHz one, is close to the desired output frequencies. Therefore, 4224 MHz signal is processed without harmonic cancellation and applied to LO port, where large harmonics are

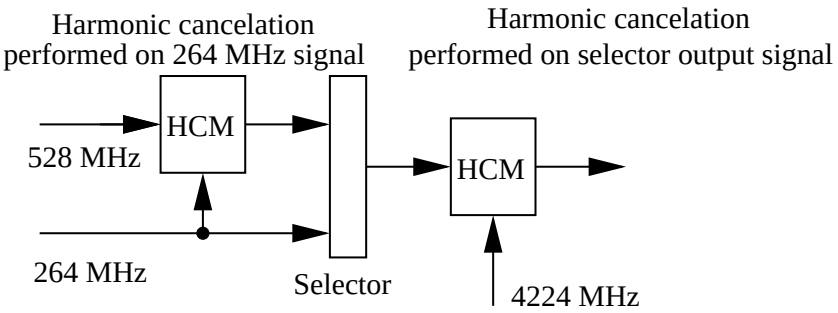


Fig. 58. Harmonic cancellation plan

generated due to hard switching. 264/792 MHz signals are processed with harmonic cancellation and applied to RF port, where less harmonics are generated.

Fig. 58 presents the harmonic cancellation plan for the two mixers.

b. Mixer Topology

Double balanced active mixer topology is adopted to realize the mixer cells of HCM. First, double balanced mixer generates least unwanted harmonic mixing terms. Even-order harmonic mixing terms between both input signals are canceled at first order. Second, active mixer output signal is not attenuated, which helps to reach required signal level for subsequent circuits without the usage of buffers demanding additional power.

3. Implementation

Fig. 59 shows the schematic of the implemented HCM. Compared with Fig. 57, the adder stage is realized by sharing the load among the three mixer cells; the gain stages are merged in the IF ports of mixer cells. Therefore, the mixer cell that takes in $V_{IF}(t)$ has IF gain $\sqrt{2}$ larger than others. This is achieved by having both the DC current and W/L ratio in that IF port $\sqrt{2}$ larger than others. In addition, the transistors in LO port are also increased by $\sqrt{2}$. This scaling approach helps all mixer

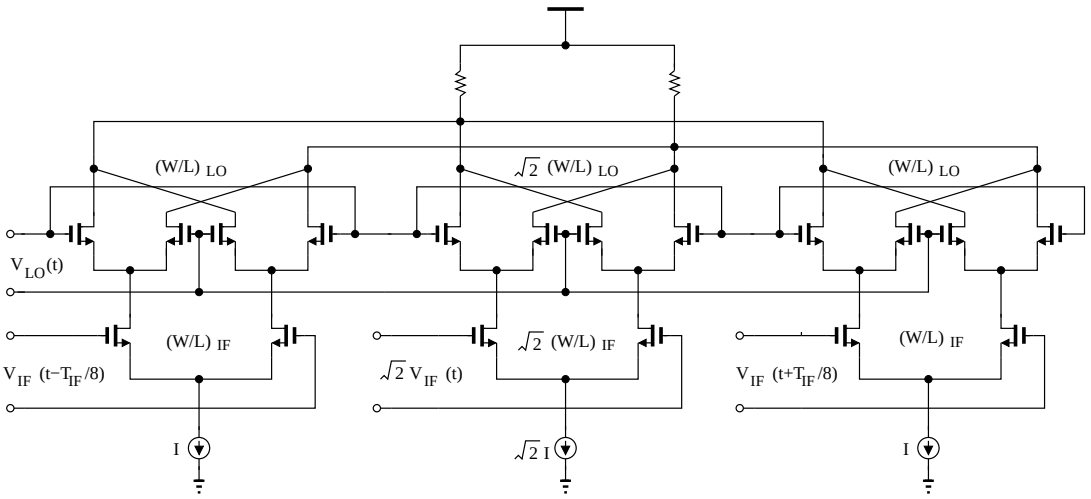


Fig. 59. HCM schematic

cells keep the same linearity characteristic by biasing all the transistors with the same voltages. In reality, however, the exact $\sqrt{2}$ times of W/L ratio is not possible. This is because the geometry precision of transistor is limited by minimum lithograph step. In our implementation, $\sqrt{2}$ is best approximated as 1.414, which corresponds to 0.2% of systematic amplitude mismatch.

C. Selector Design

Selector is inserted between the two harmonic mixers to pick one signal from 762 MHz, 264 MHz and -264 MHz. Similar to the mixers, linearity of this selector is the main concern. Therefore, we implement the selector as shown in Fig. 60. $M_1 - M_6$ are used as switches. Their W/L ratio is chosen such that the ON resistance is comparable with the transconductance of the differential pairs. In this way, the output is linearized by the switches as source degeneration resistors. The W/L ratio of the differential pairs are chosen to be small for two reasons: the linearity is improved as for the same current, the over drive voltage V_{DSAT} is increased; the coupling from the differential pair inputs to outputs is reduced because of less parasitic capacitance. To reduce the

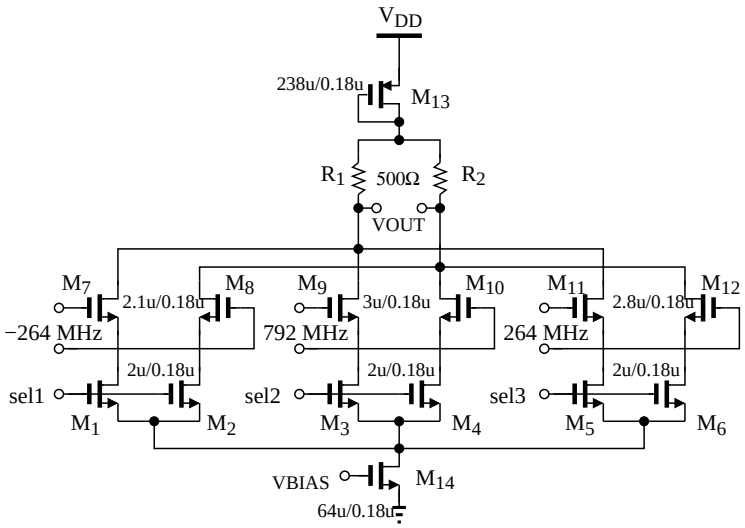


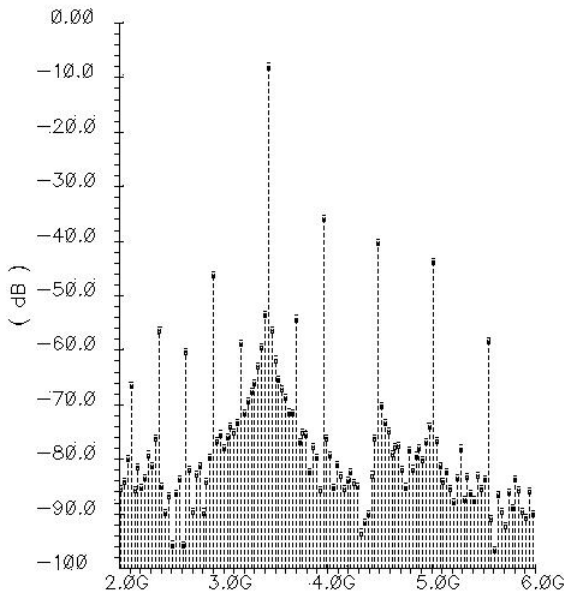
Fig. 60. Selector schematic

power consumption and avoid harmonic generation, the output of selector is directly connected to the IF portion of the 4224 MHz mixer without buffers. Thus to have the output DC voltage compliant with the 4224 MHz mixer IF inputs, which is at the lower end of the mixer. A PMOS in diode connection placed from V_DD to load is used to lower the output DC voltage.

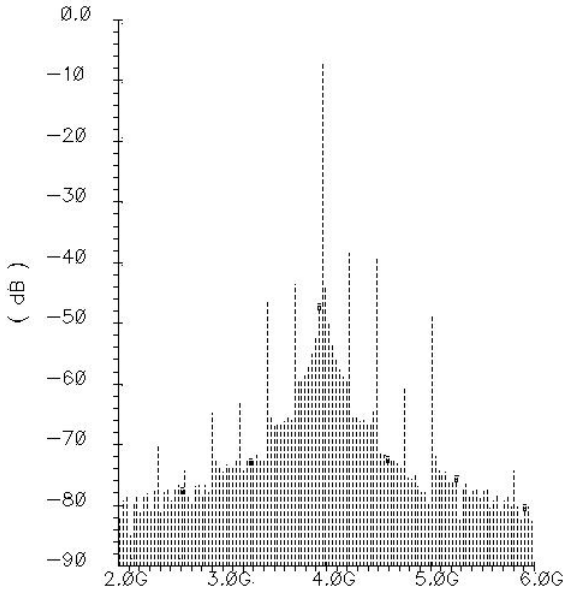
D. Simulation

Post-layout simulation was performed on the whole set of mixer and frequency divider part in the UWB frequency synthesizer. Fig. 61 shows the spectrum at mixer output when generating three carrier frequencies. The sidebands around 2.4 GHz and 5 GHz are suppressed to be below the carrier frequencies by more than 41 dBc and 36 dBc, respectively. Those simulated rejection ratios are 6 dB more than the requirement.

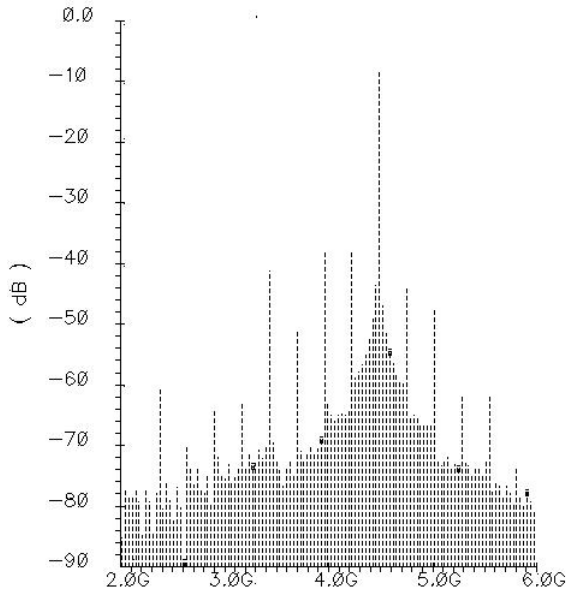
Figs. 62, 63 and 64 show the simulated $3rd$ and $5th$ harmonic rejection ratio under various kinds of mismatch, including input amplitude and phase mismatch, RF port transistor size mismatch. To have the degradation of rejection ratio less than 6dB, it requires less than 2% amplitude mismatch, 1° phase mismatch and 3%



(a) 3432 MHz Output

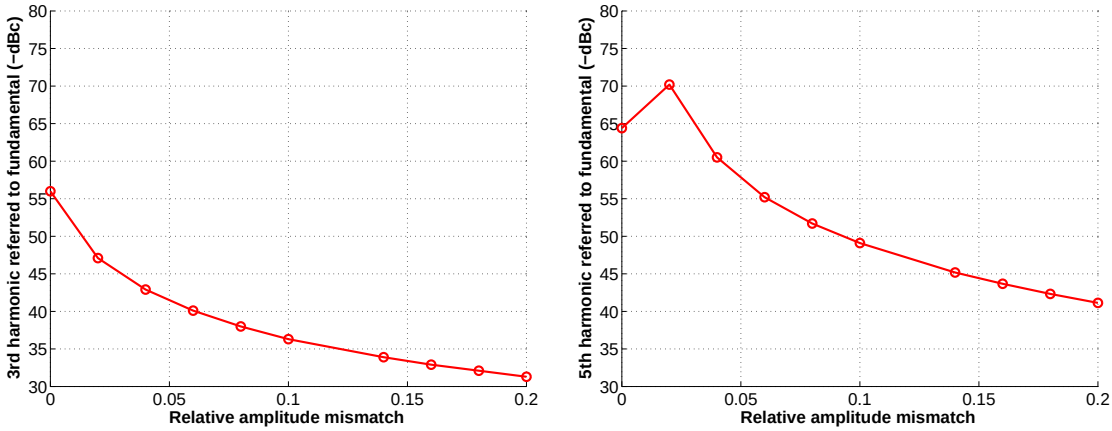


(b) 3960 MHz Output



(c) 4488 MHz Output

Fig. 61. Spectrum of mixer output for the three carrier frequencies



(a) $3rd$ harmonic rejection ratio (b) $5th$ harmonic rejection ratio

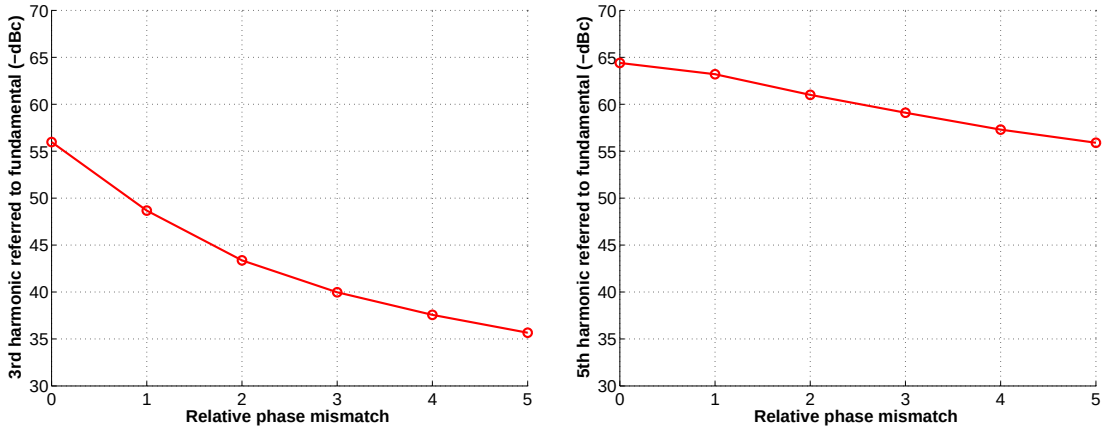
Fig. 62. Simulated harmonic rejection ratios under input amplitude mismatch

RF port transistor mismatch, which of course draw careful design consideration but are feasible in practice.

Frequency hopping simulation result is shown in Fig. 65. The frequency hopping time can be seen to be well below 9.5 nS, which is true for all the cases.

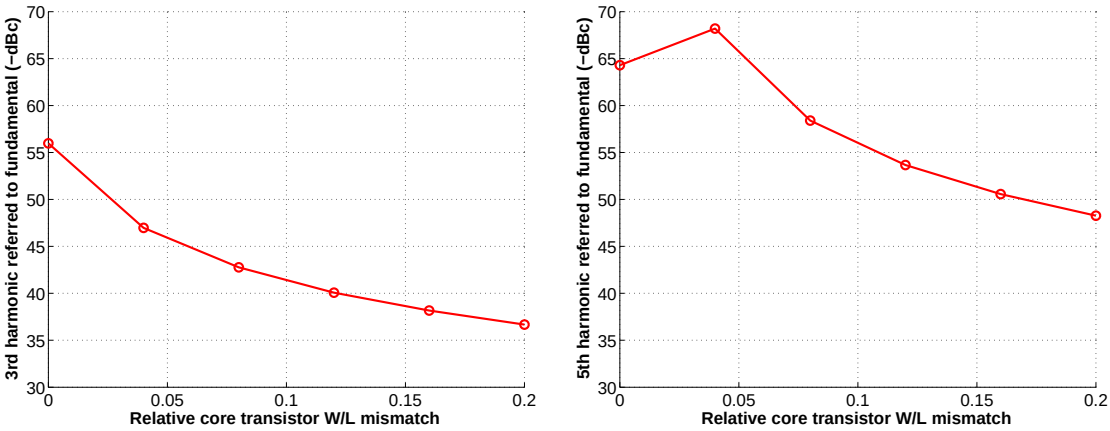
E. Frequency Synthesizer Layout

The layout of the whole frequency synthesizer is shown in Fig. 66. It occupies an area of $1380 \times 1200 \mu m^2$. One main area is occupied by the capacitors of loop filter, which is implemented by MIM capacitors with top metal layer. The MIM capacitor provides capacitance density of 1.1 $fF \mu m^2$, which translates to chip area of $600 \times 380 \mu m^2$ for C_1 and C_2. Another part is for the frequency divider and mixer, which has an area of $700 \times 500 \mu m^2$. The VCO takes the largest area as $1150 \times 540 \mu m^2$, which is due to the two inductors being used.



(a) $3rd$ harmonic rejection ratio (b) $5th$ harmonic rejection ratio

Fig. 63. Simulated harmonic rejection ratios under input phase mismatch



(a) $3rd$ harmonic rejection ratio (b) $5th$ harmonic rejection ratio

Fig. 64. Simulated harmonic rejection ratios under input phase mismatch

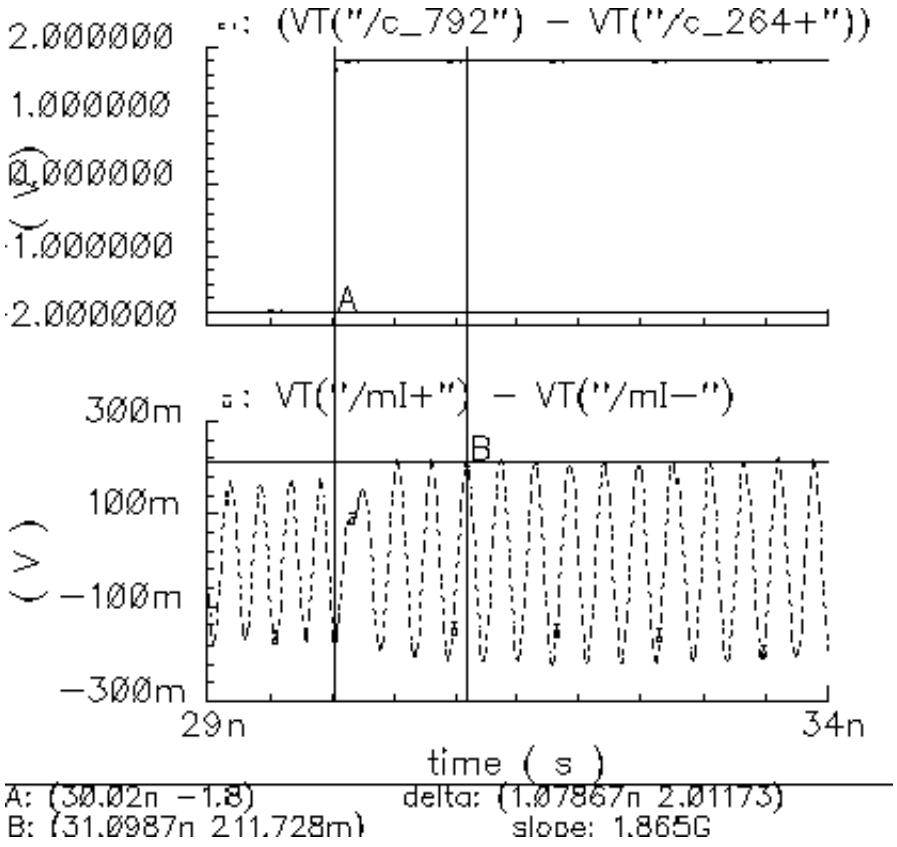


Fig. 65. Carrier frequency hopping time

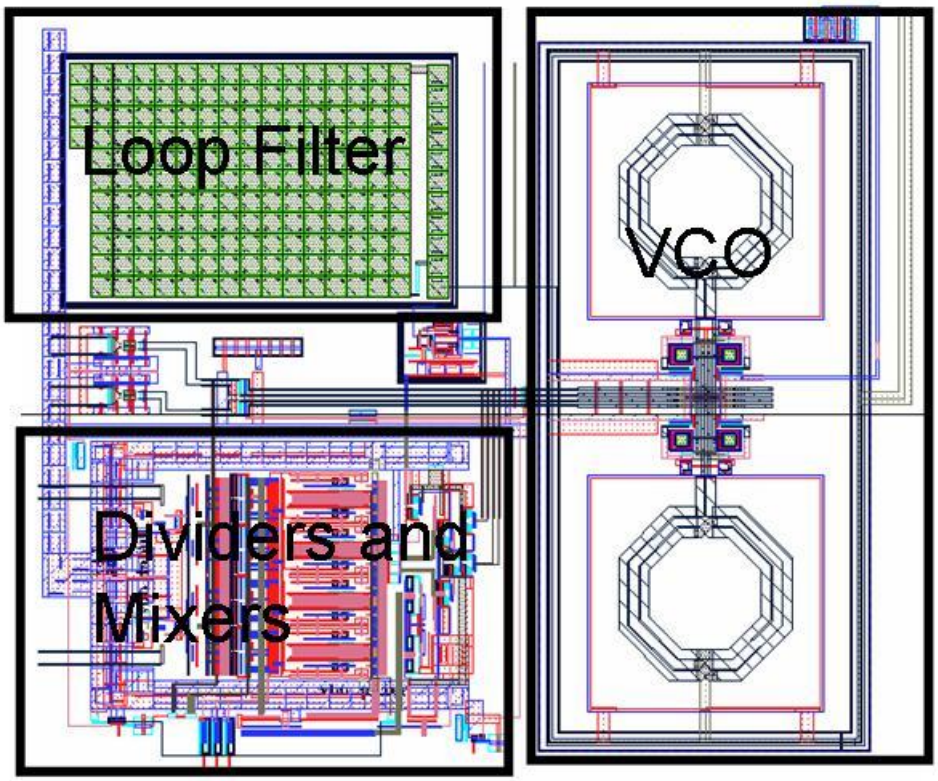


Fig. 66. Frequency synthesizer layout

CHAPTER VI

FREQUENCY DIVIDER

A. Introduction

Frequency dividers are widely used in frequency synthesizers to divide down high-frequency clocks. In this research, frequency dividers serve three purposes as follows.

1. To generate a low frequency for the comparison with the reference frequency in the PLL.

2. To provide a clock frequency for the ADC.

3. To output necessary low frequencies, which are then mixed with the PLL output frequency to synthesize required center frequencies.

While the required center frequencies and the ADC clock frequency are set by the system specification, the reference frequency and the PLL output frequency are varied, depending on the achievable frequency division ratios. In most cases, the integer division ratios are easier to be implemented than fractional one.

1. Integer Frequency Divider

Integer frequency divider is most widely implemented by using digital counter, as shown in Fig. 67. The input frequency serves as the clock signal of the N-counter. The N-counter outputs the same value for every N clock cycles. Therefore, the function of divide-by-N is implemented. A simple example is shown in Fig. 68. A 2-counter is realized by applying the D flip-flop complementary output back to its input. For every rising edge of the clock, the output will be changed from "0" to "1" or vice versa. A division ratio of two is then realized. The division ratios of

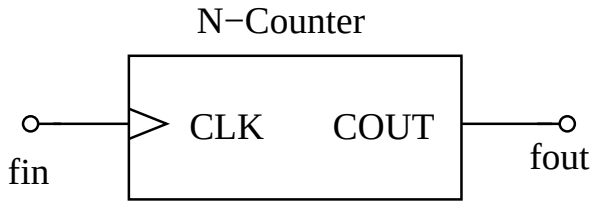


Fig. 67. Counter based integer frequency divider circuit

integer frequency dividers could be varied. Those frequency dividers might be rather complicated, depending on the range of the division ratios [11].

2. Fractional Frequency Divider

Similar to integer frequency divider, fractional frequency divider is commonly implemented in a digital fashion, due to the robustness nature of digital circuit. The structures of those digital fractional frequency divider are inherently more complicated than those of integer ones. Fig. 69 shows a typical fractional frequency divider structure. It consists of a $\Sigma\Delta$ modulator and a dual-modulus integer frequency divider. The instantaneous division ratio could be either N or $N+1$, controlled by the modulator. Therefore, an average division ratio $N+\alpha$ $(0<\alpha<1)$ is implemented. $\Sigma\Delta$ modulator helps converting the systematic fractional sidebands to random noise and shaping the resulting noise spectrum such that most of its energy appears at large offset frequencies [11] . The achievable speed of this divider, however, is limited by the $\Sigma\Delta$ modulator.

3. Comparison of Integer Frequency Divider and Fractional Frequency Divider

The above discussion leads to the following Table IV, which compares integer frequency divider and fractional frequency divider. The choice for those two frequency dividers is a compromise among division ratio, complexity and speed.

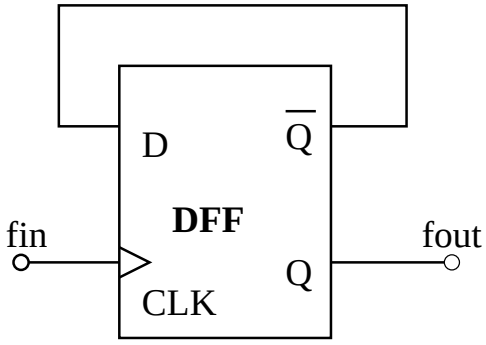


Fig. 68. Divide-by-two circuit

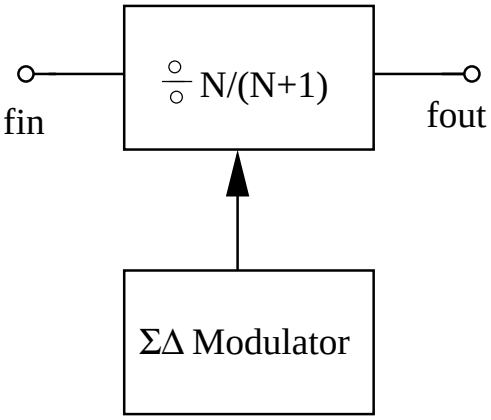


Fig. 69. ΣΔ modulated fractional frequency divider diagram

Table IV. Comparison of integer frequency divider and fractional frequency divider

	Integer Frequency Divider	Fractional Frequency Divider
Division Ratio	Integer	Fractional
Complexity	simple	complicated
Speed	Fast	Low

B. Frequency Dividers in the UWB frequency synthesizer

1. Design Consideration

a. Programmability

The fast settling requirement of the UWB frequency synthesizer actually relaxes the requirement of the PLL, as it only needs to output one fixed high-frequency clock. The frequency division ratios of the dividers in the PLL, therefore, are also fixed. No programmability is needed for those dividers.

b. Division Ratio

As shown in Chapter III, there are two possible frequency synthesizer architectures, depending on the types of the frequency dividers. The fractional frequency divider based architecture requires the divider output frequency as high as 528 MHz. $\Sigma\Delta$ modulator in conventional fractional frequency divider, however, normally operates below tens of MHz, which makes those fractional frequency dividers not suitable for this application. Some recent papers [7, 15] propose to use several specific techniques to achieve the division ratio 7.5.

Fig. 70 shows the divide-by-7.5 circuit proposed in [15]. The trigger polarity of the first DFF is changeable and controlled by the last DFF. The feedback signal toggles every eight triggering events for the first DFF, including only one trigger polarity change, which effectively 'eats' half cycle of the input period. Therefore, the feedback frequency is one fifteenth of the input frequency. Since the output frequency is double of the feedback frequency, the output frequency would be the input frequency divided by 7.5. The input frequency of this approach, however, is rather limited. The critical timing, shown in Fig. 71 happens when the trigger polarity

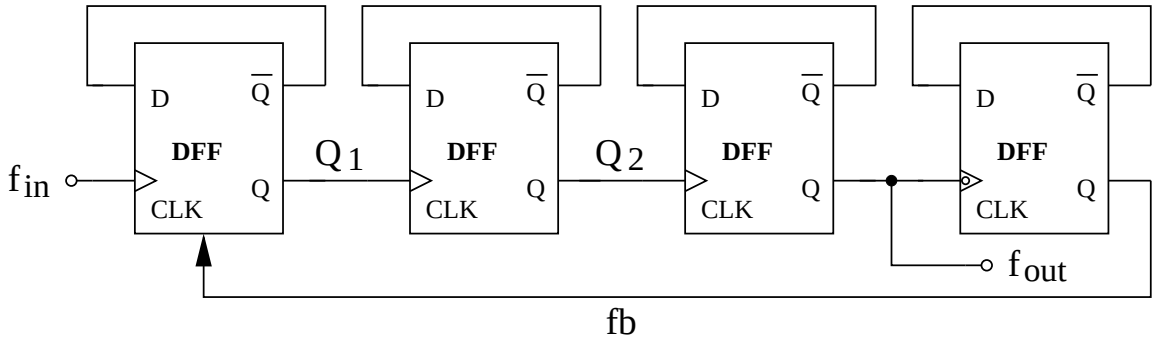


Fig. 70. Divide-by-7.5 circuit in [15]

is changed. Indeed, the change of the trigger polarity has to be finished within half cycle of the input signal, which includes four clk-to-Q delays. Compared to a normal divide-by-2 circuit, which only needs a clk-to-Q delay over a whole cycle of input frequency, the operation speed of this divide-by-7.5 is much lower.

Fig. 72 shows the divide-by-1.5 circuit proposed in [7], which would be followed by a divide-by-5 circuit for the overall 1/7.5. The phase rotating technique is used there to achieve the fractional division. The structure consists of a MUX tree and two cascading divide-by-2 circuits for generation of rotating control signals. While the output of the first divide-by-2 circuit is the 1/1.5 frequency, this means that the frequency of the MUX tree output and also the input clock of this divide-by-2 is 2/1.5 of the PLL output frequency, even higher than the PLL output frequency. Therefore, both the MUX tree and the first divide-by-2 mandate high power consumption. Furthermore, any phase error between the quadrature inputs and mismatch between the MUX cells would be translated to the output frequency variation. As could be seen, the existing fractional divider solutions are either questionable in robustness or not power efficient. The integer frequency divider based architecture, on the contrary, only needs a chain of simple divide-by-2 circuits.

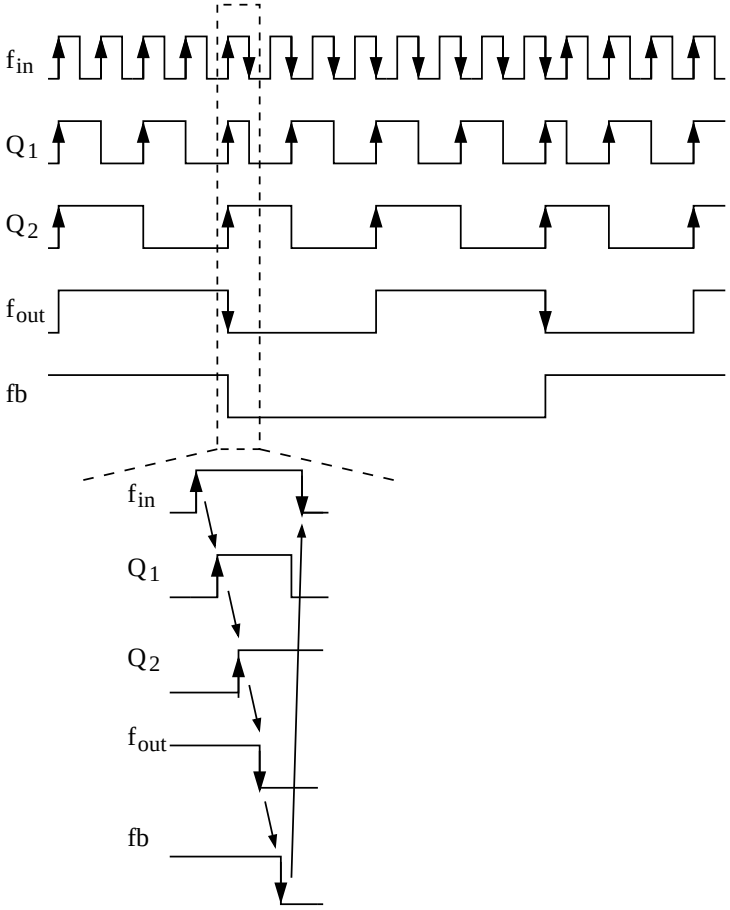


Fig. 71. Timing diagram of the divide-by-7.5 circuit in in [15]

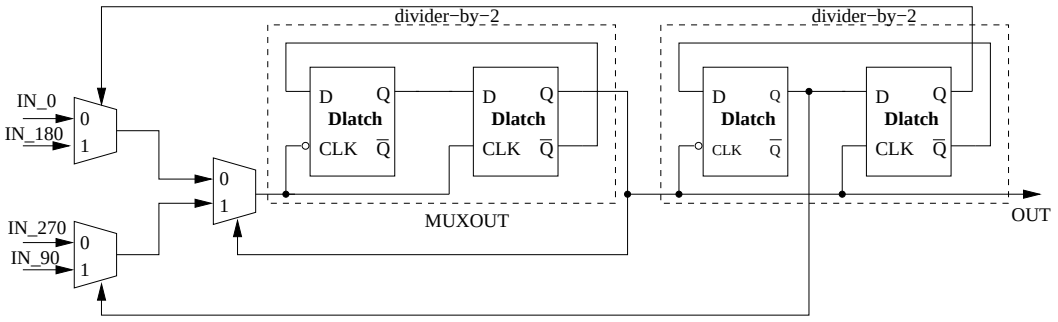


Fig. 72. Divide-by-1.5 circuit in [7]

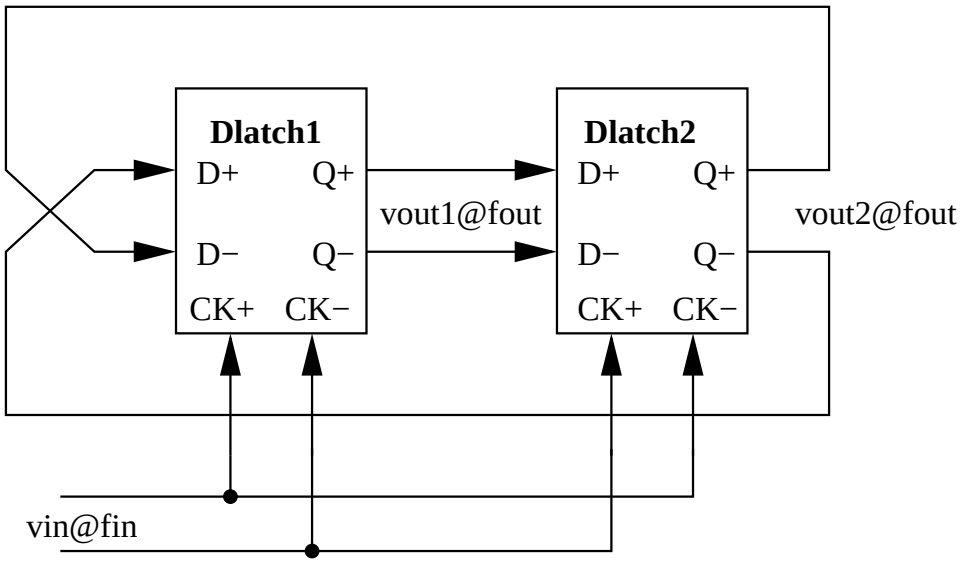


Fig. 73. Differential divide-by-two circuit

c. 45° Phase Generation

The usage of harmonic cancelation SSB mixer necessitates the frequency dividers output eight 45° spaced clocks both at 528 MHz and 264 MHz. The phase relation between those eight clocks has to be known, i.e. for any two of those clocks, the phase difference between them should be well defined.

It is well-known that a differential divide-by-2 circuit is able to generate 90° spaced clocks by using two identical D-latch cells, as shown in Fig. 73. This is because the two latches are triggered by oppositive input clock levels. Assume that the input clock is 50% duty cycle, the two outputs would be spaced by half of input clock period, which is the quarter period of the output clock. Furthermore, Fig. 74 shows that as the second latch output follows the first one, the timing relation between the two outputs are fixed, i.e. the second latch output is always $T_{out}/4$ (90°) delayed compared to the first one. This phase relationship is independent of initial states of the two latches.

The 90° phase generation approach described above could be extended to produce

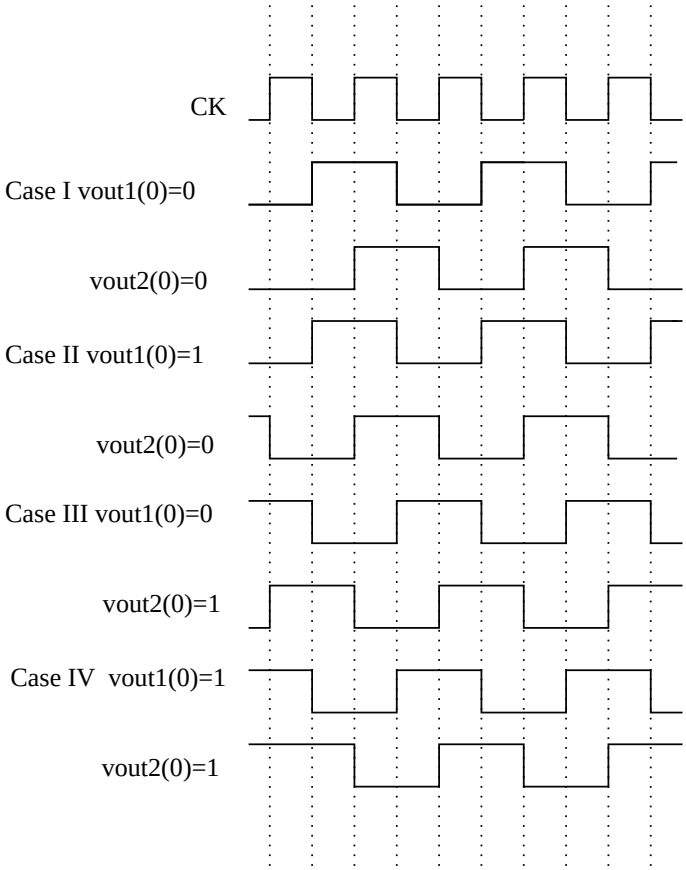


Fig. 74. Conventional divide-by-2 circuit timing

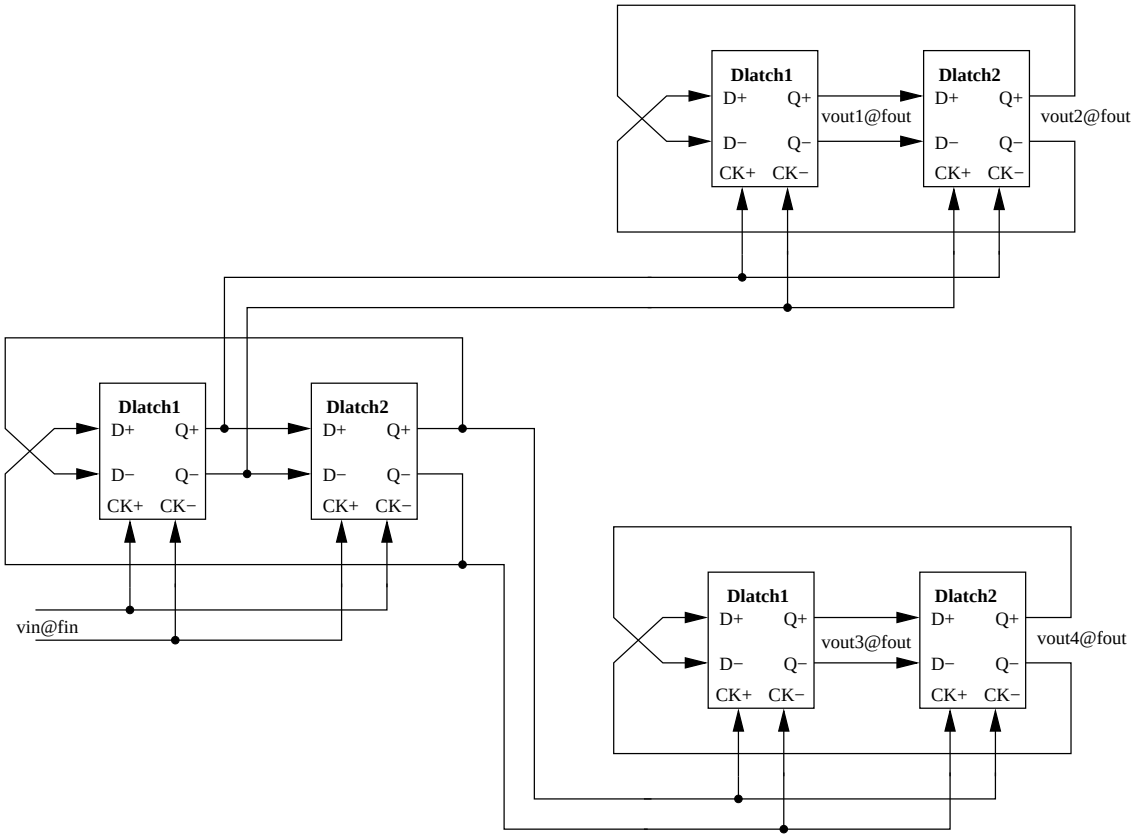


Fig. 75. Diagram of 45° generation circuit using divide-by-two circuits

45° spaced clocks. As shown in Fig. 75, it is done by having each of two quadrature clocks driving a differential divide-by-two circuit. The quadrature clocks are obtained by using another differential divide-by-two circuit. However, unlike the 90° generation approach, this approach along does not guarantee that the phase relation between those eight output clocks is in order. Fig. 76 shows that different initial states of the two differential divide-by-two circuits in the second stage lead to different phase relations between the eight output clocks. Also, Fig. 77 shows that the phase relation is dependant on the initial states of the input clocks, which comes from the divide-by-two at the first stage. Therefore, all those three differential divide-by-two circuits have to be resettable. In this way, the initial states are well defined, so is the phase relation between the output clocks.

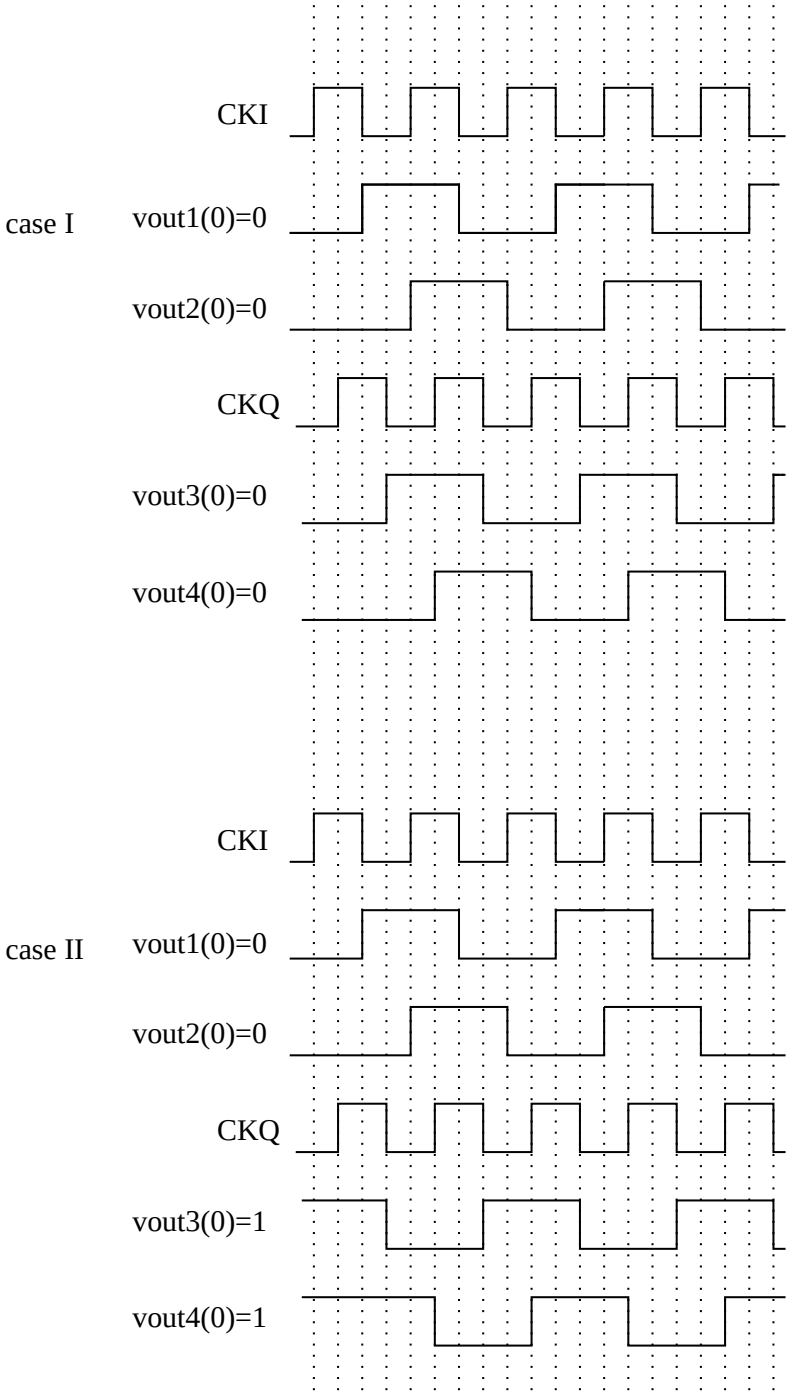


Fig. 76. An example of 45° phase relationship depending on initial state of the second stage

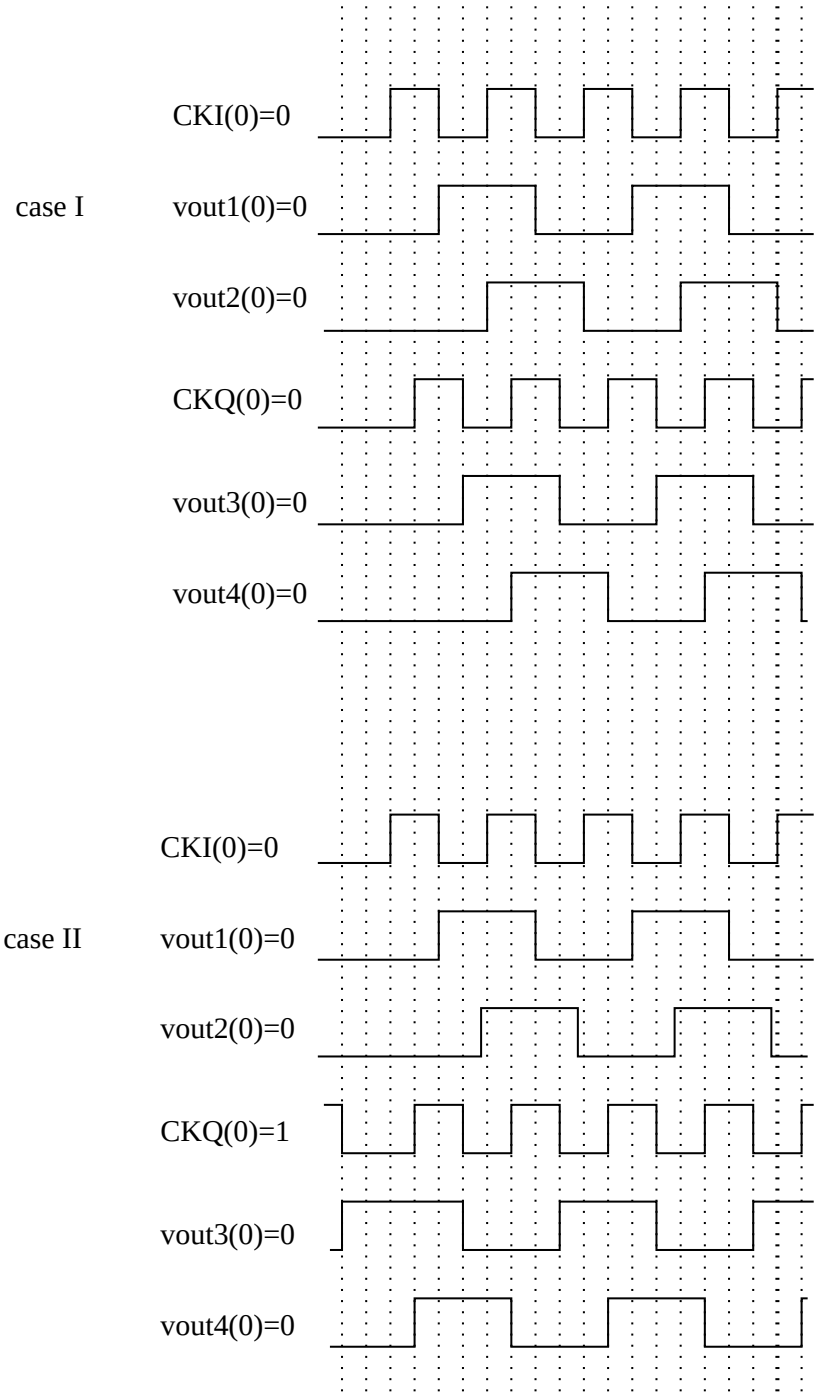


Fig. 77. An example of 45° phase relationship depending on initial state of the first stage

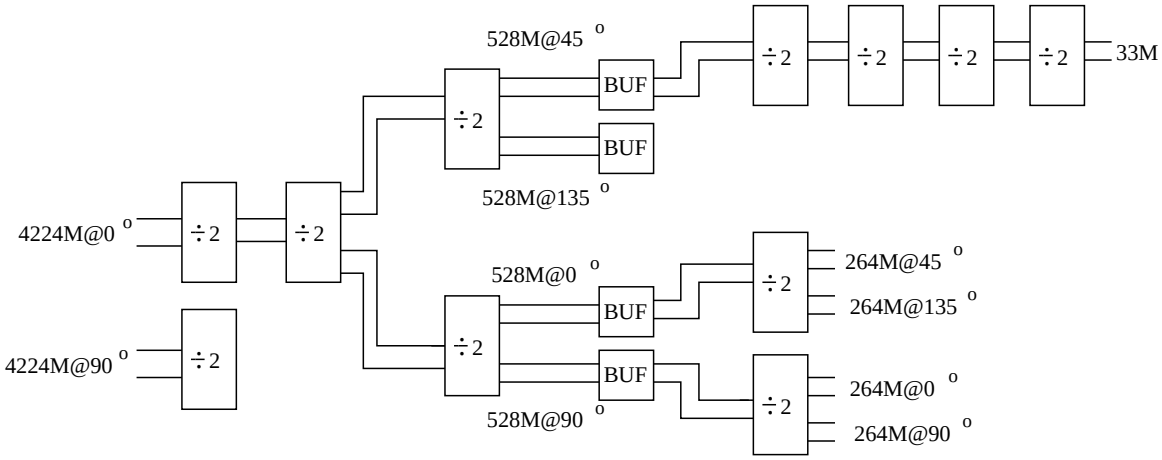


Fig. 78. Frequency divider circuit for the UWB receiver

2. Structure of Frequency Dividers in the UWB Receiver

Fig. 78 shows the overall frequency divider circuit. It consists of divide-by-two circuits. In between 528 MHz and 264 MHz clock, buffers are inserted. A dummy divide-by-two circuit and a dummy buffer are used to provide balanced load for 4224 MHz and 525 MHz clock, respectively. There are three types of divide-by-two circuits used in this circuit, which will be described in detail as follows.

3. Design of Divide-by-two Circuit

a. CML Differential Divide-by-two Circuit with Reset

The generation of 45° phase spaced clocks at both 528 MHz and 264 MHz requires the usage of current-mode-logic (CML) differential divide-by-two circuits with reset. The high speed property of CML ensures the robust operation of those divide-by-two circuits at such frequencies. The differential structure leads to the symmetrical outputs to reduce phase error. Fig. 79 shows the circuit implementation for a latch used in such divide-by-two circuits. When CK is high, the output Q tracks the input D through the differential pair M_2s. When CK is low, the output Q holds its current

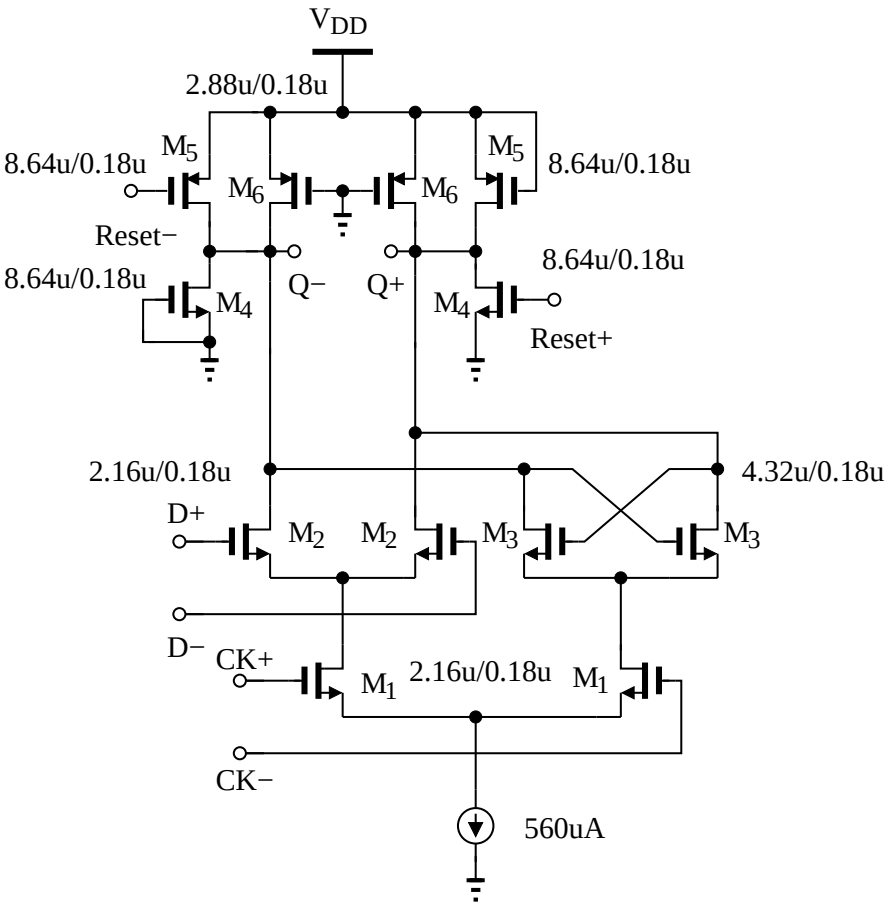


Fig. 79. CML implementation of the latch cell for the divide-by-two circuit with reset

value through the differential pair M_3s in a positive feedback configuration. M_{8-9} are operated in triode region as passive loadings. $M_{(4-7)}$ form the reset network. When *Reset* is high, M_6 pull down the $Q+$ to ground while M_5 pull up the $Q-$ to VDD. When *Reset* is low, M_4 and M_7 serve as dummy transistors to provide equal capacitance from the reset network to the outputs. When *Reset* is high, M_4 and M_7 set the output to ZERO state.

b. CML Differential Divide-by-two Circuit without Reset

For the divide-by-two in the first stage, as it is not involved in the 45° phase generation, it does not need the reset function, as shown in 80. While the circuit becomes

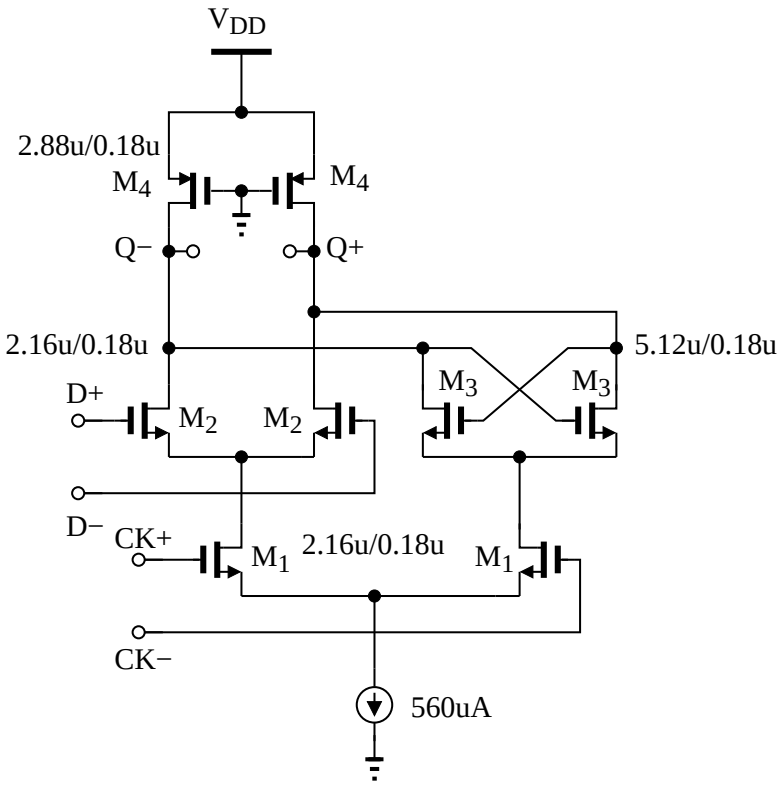


Fig. 80. CML implementation of the latch cell for the divide-by-two circuit without reset

less complicated, the additional benefit of removing the reset function is the increase of the operation speed, which is critical for the robust operation of this divide-by-two, as it has to work at the highest speed among all dividers. The speed improvement is because the reset transistors are removed and so are their parasitic capacitances.

c. CMOS Logic Divide-by-two Circuit without Reset

The divide-by-two circuits after the generation of the 45° spaced 264 MHz clock does not need the reset function, as their only purpose is to further divide down the 264 MHz clock to a frequency comparable with the reference clock. Also, as the operation frequency for those divide-by-two circuits are low enough, CMOS logic divide-by-two is used to save power. Fig. 81 shows the schematic for a CMOS logic latch. When

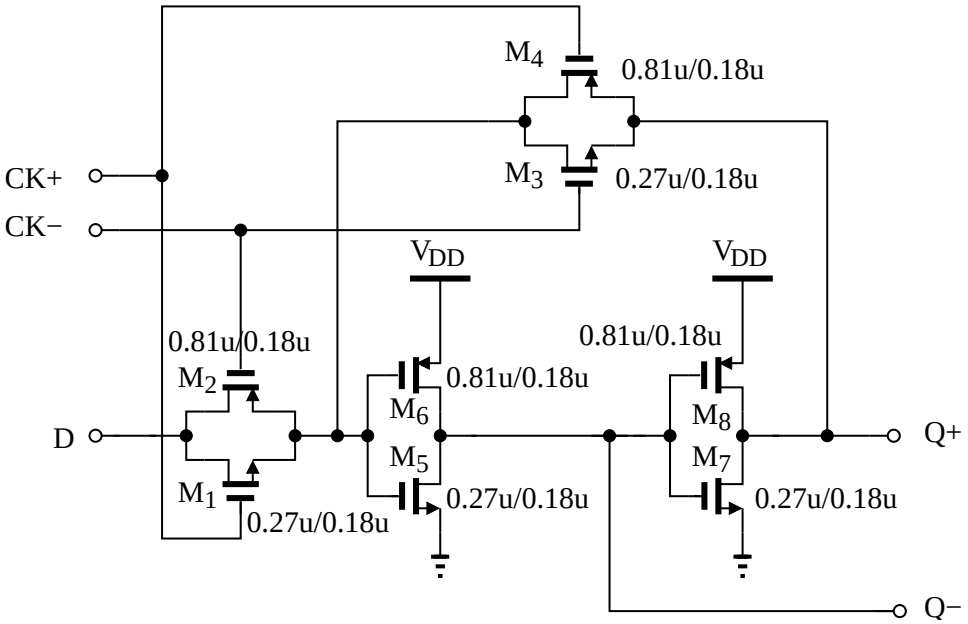


Fig. 81. CMOS implementation of the latch cell for the divide-by-two circuit without reset

CK is high, the output $Q+$ and $Q-$ track the input. When CK is low, the two inverters are configured as a positive feedback to hold the value of the output.

C. Injection Locked Frequency Dividers

1. Introduction

All the types of frequency dividers used in the UWB frequency synthesizer fall into the category of digital static frequency dividers. This is because those frequency dividers are essentially digital counters and all have positive feedbacks to hold the output values when necessary. Indeed, digital static frequency dividers are usually employed in many applications. However, their limitation on power consumption and maximum operating frequency drives IC designers to seek alternative solutions. One such candidate is injection-locked frequency divider (ILFD).

ILFDs consist of free running oscillators synchronized to injected signals. While

digital static frequency dividers could work from their maximum operation frequency down virtually to DC, ILFDs have both higher end and lower end operating frequency limits. Therefore, one of the primary design efforts for ILFDs is to increase its working range (so called locking range).

Depending on types of oscillators incorporated in ILFDs, they can be classified as LC oscillator based ILFDs (LC-ILFDs) and ring oscillator based ILFDs (ring-ILFDs). Fig. 82 shows an example of LC-ILFDs presented in [16]. The inductor L and the capacitor C compose an LC resonance network. The incident signal is injected trough the gate of M_3 to the common source node of M_1 and M_2. M_1 and M_2 deliver output signal to the LC tank. The LC tank helps to filter out unwanted frequency components and feeds back output signal to the gates of M_1 and M_2. This LC-ILFD is good for divide-by-2 operation, which is understandable as the common source node sees the doubled frequency of the output signal, which is the fundamental frequency of the incident signal.

The high quality factor Q and narrow band nature of LC oscillators limit the locking range of an LC-ILFD. Its locking range would likely fail to cover the desired operating range in the presence of process parameter variations. To maximize the locking range, the Q of the LC tank have to be lowered at the cost of either large die area [16] or high power consumption [17]. Although varactors can be used to increase the locking range [17], simultaneous tuning of the divider and the VCO in PLL is still a challenging problem. On one hand, the tuning of the divider needs to know the VCO output frequency after the VCO is tuned to the desired one. On the other hand, the tuning of the VCO needs the divider works properly, which could only happen after the divider is tuned. This dilemma hinders the usage of the varactor tuning in practice. Another issue associated with LC-ILFD is that the output amplitude changes a lot along the locking range because the tank impedance drops rapidly

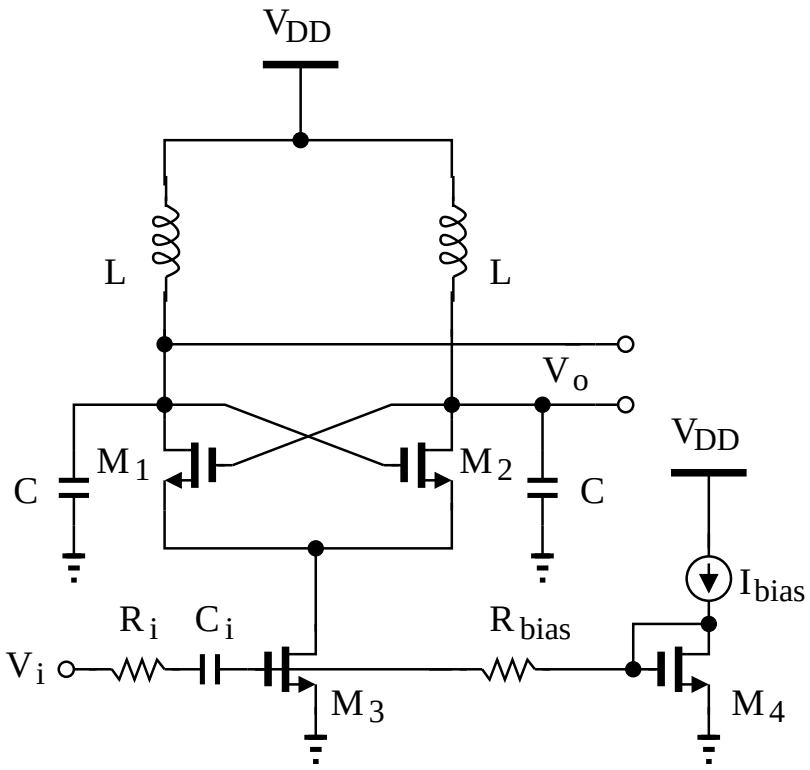


Fig. 82. An LC-ILFD in [16]

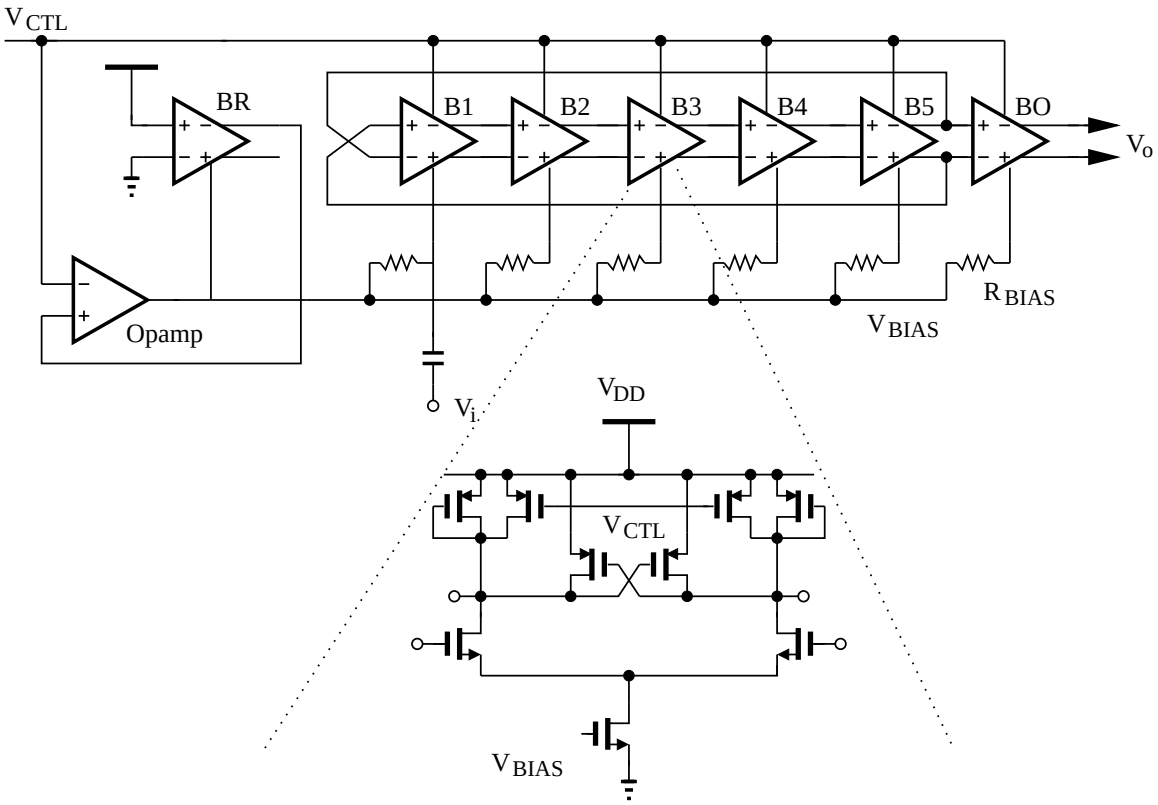


Fig. 83. A ring ILFD in [24]

when the output frequency is shifted from the resonance frequency. Power-hungry buffers have to be used to provide enough voltage swing for the robust operation of the circuitries following the ILFDs.

With their low Q by nature, ring-ILFDs recently draw much research effort. They have been shown to have a larger locking ranges and less amplitude fluctuations [18–23].

Fig. 83 shows a ring-ILFD example [24]. The $B_1 - B_5$ stages compose a five-stage ring oscillator. BO is the output buffer. BR and $Opamp$ together provide the voltage bias for the gate of the tail transistor in each differential pairs. The incident signal is injected to the gate of the tail transistor in the first stage B_1. The output signal of B_1 goes through the following four stages and is fed back to its differential inputs. Both

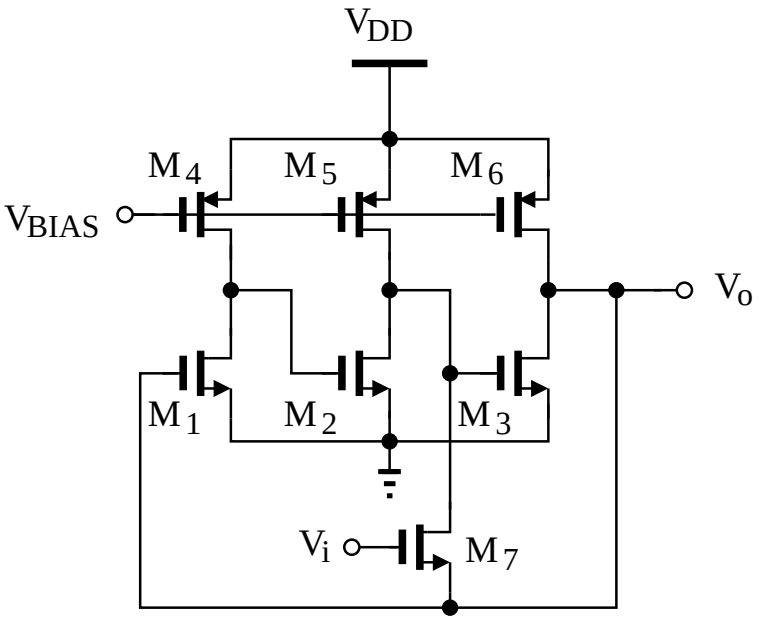


Fig. 84. A ring ILFD in [23]

the output signal and the incident signal would be presented at the common source node. [24] shows that such a ring-ILFD achieves multi-division ratios as 2,4,6,8, the locking range, however, is only 32 MHz at most.

Fig. 84 shows another ring-ILFD example [23]. Unlike the above two ILFDs, the incident signal is not injected through the tail transistor. Instead, the incident signal is injected to M_7, which connects the outputs of the last two stages. M_7 functions as a switch, modulated by the incident signal. When M_7 is ON, the two outputs are forced to be the same. When M_7 is OFF, the two outputs have the phase difference set only by the ILFD, not the incident signal. Yamamoto el al [23] manipulated the sizes of $M_1 - M_7$ in such a way that that phase difference is 180 degrees when M_7 is OFF. It is shown by doing this way that a divide-by-2 operation is realized.

Both LC-ILFDs and ring-ILFDs have so far shown to be able to work at very high frequencies, however, none of the existing solutions could provide large division ratios with acceptable locking ranges. Large division ratio is necessary to reduce the

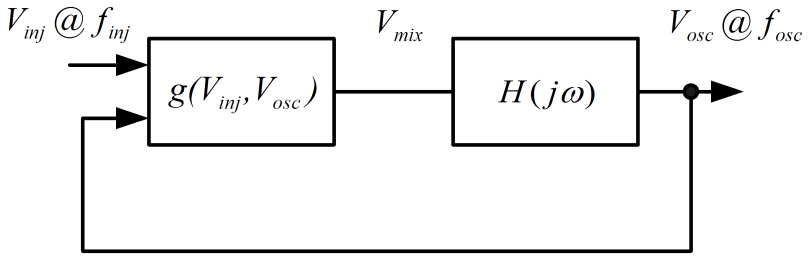


Fig. 85. A conventional model for ILFD [25]

output frequencies of the ILFDs, which relaxes the requirements on speed and power for the following circuitries.

In this section, a new architecture of ring-ILFD is presented. Although only 3 stages are used for the implementation in a standard 0.18 μm CMOS technology, the measurement shows that the division ratio can be as high as 6, 12, and 18 depending on the injection frequency. The corresponding locking ranges are 2.1 GHz, 1.9 GHz, and 1.7 GHz, respectively. The locking ranges are relatively large due to the multiple injection stages and highly nonlinear operation of the topology. The injection frequency could be up to 11 GHz while the power consumption is 7.2 mW.

2. Circuit Architecture

a. Study of Conventional ILFD Model

Verma et al [25] introduced a general model for the ILFD as shown in Fig. 85. It consists of a nonlinear gain block g and a linear filter $H(j\omega)$. The nonlinear block mixes the injection signal V_{inj} with the oscillator input signal V_{osc}, which is the feedback from the output of the linear filter. The linear filter $H(j\omega)$ rejects frequency components far from f_{osc} and provides necessary phase shift to sustain the oscillation.

The frequency components at the output of the block g could be expressed as $|mf_{osc} \pm nf_{inj}|$, where f_{inj} is the fundamental frequency of V_{inj}, m and n are integers.

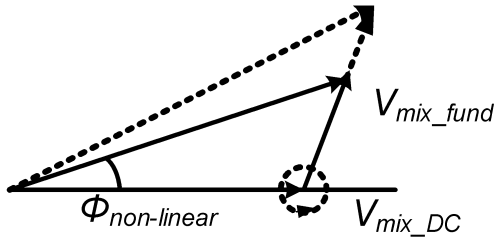


Fig. 86. Generation of $\phi_{non-linear}$ from V_{mix_dc} and V_{mix_fund}

Assuming weak injection [25], n could be 0 and 1 since the harmonics of injection frequency are ignored. When $n = 0$, the DC component of V_{inj} is multiplied by the fundamental component f_{osc} of V_{osc}. The resulting product is denoted as V_{mix_DC}. If the nonlinear function of g is assumed to be memoryless [25], there is no phase shift from f_{osc} of V_{osc} to V_{mix_DC}. When $n = 1$, the fundamental component f_{inj} of V_{inj} is mixed with the harmonics of f_{osc} to generate a component at f_{osc}. The resulting product is denoted as V_{mix_fund}. For instance, for the division ratio of k between f_{inj} and f_{osc},

$$f_{osc} = \frac{f_{inj}}{k} \Longrightarrow f_{inj} - (k-1)f_{osc} = f_{osc} \tag{6.1}$$

As the phase of f_{inj} relative to f_{osc} of V_{osc} is arbitrary, the phase of V_{mix_fund} relative to V_{mix_DC} is also arbitrary. Because the frequency component at f_{osc} in V_{mix} is the sum of V_{mix_dc} and V_{mix_fund}, as shown in Fig. 86, the overall phase shift $\phi_{non-linear}$ depends on the relative amplitude and phase difference of these two components.

As suggested in [25], if the loop has sufficient gain so that the Barkhausen criterion of magnitude is satisfied, the locking range is determined by the phase criterion given by

$$\phi_{linear} + \phi_{non-linear} = 2i\pi \tag{6.2}$$

where ϕ_{linear} is the phase shift due to $H(j\omega)$ and i is an integer. Since the value of

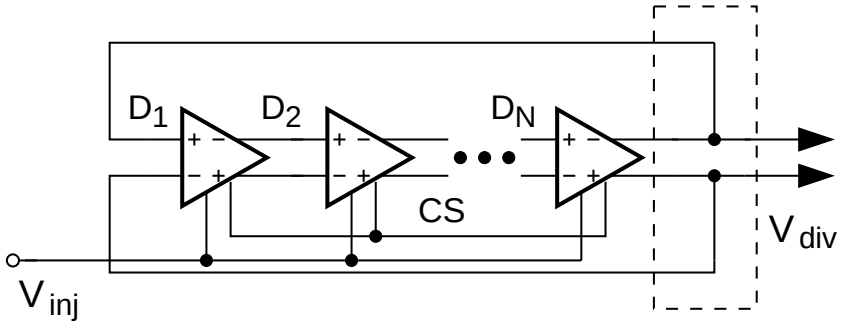


Fig. 87. Architecture of the proposed multiple highly nonlinear injection stage ring-ILFD

ϕ_{linear} across frequencies is fixed for a certain ILFD, the ILFD fails to lock when the nonlinear block could not provide the required phase shift $\phi_{non-linear}$ to meet (6.2). The larger the range of $\phi_{non-linear}$, the larger the locking range is.

High nonlinearity increases the amplitude of V_{mix_fund} so that it becomes more comparable to V_{mix_DC}. Therefore, more phase shift could be generated. As a result, not only the locking range for the small division ratio is extended, but the implementation of large division ratios is also made possible.

The range of $\phi_{non-linear}$ could also be enlarged by cascading multiple nonlinear stages in the circuit, under which case, the overall $\phi_{non-linear}$ will be the multiplication of $\phi_{non-linear}$ from a single stage. While it is difficult to have multiple injection stages in LC-ILFD, which normally consists of one-stage LC oscillator, ring-ILFD could provide multiple injection stages, which is usually realized with several identical stages in the loop.

b. Ring-ILFD with Multiple Highly-Nonlinear Injection Stages

The above study of the general model of ILFDs shows that a large locking range could be achieved by implementing ring-ILFD with multiple highly nonlinear stages. The seeming disadvantage of using ring-ILFD is its poor internal phase noise. However,

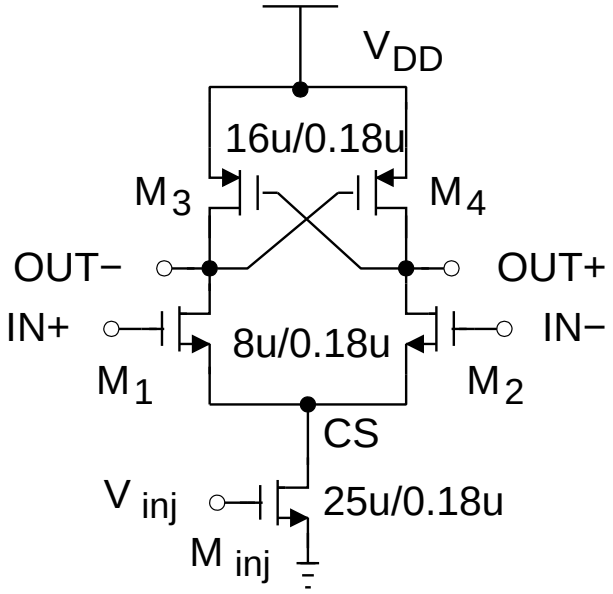


Fig. 88. Schematic of one stage of the proposed multiple highly nonlinear injection stage ring-ILFD

[25] shows that the internal phase noise is high-pass filtered at the output, which becomes negligible compared with the phase noise from the injection signal that is low-pass filtered. What is more, it is also shown that the pole frequency of the high-pass transfer function increases with the increase of the locking range. Therefore one benefit of large locking range is that the contribution of internal phase noise to the output is much suppressed with a large frequency range.

The architecture of the proposed multiple highly-nonlinear injection stage ring-ILFD is shown in Fig. 87. It consists of N stages of differential pair ($M_{1\text{-}2}$) with PMOS transistors ($M_{3\text{-}4}$) in positive feedback configuration as load, as shown in Fig. 88. If N is an even number, the outputs of the last stage need to be cross-coupled to the inputs of the first stage. The injection points are the gates of the current bias transistor M_{inj} in all stages. This architecture shares the common source nodes of all the stages. The advantage of this approach is that the operating frequency of the ILFD is increased, which will be explained in the next section.

The high nonlinearity operation is achieved by using the positive feedback load. Similar technique was used in a saturated ring oscillator design [26]. By doing so, outputs with sharp transition and large amplitude are generated, both of which facilitate the nonlinearity. However, the strong nonlinear operation of the load transistors makes the conventional ILFD model not suitable for the analysis of the proposed ILFD. In the conventional model, the load is modeled as a linear block, which is not the case for the proposed ILFD. Without such linear blocks, the frequency domain analysis is not correct. Instead, large signal transient analysis has to be utilized. Similar method was introduced recently in [27], in which Gangasani et al also show the necessity of time domain analysis.

3. Locking Range of the ILFD

a. Operation of the Free Running ILFD

Let us consider how one stage of the free running ILFD (Fig. 88) responds to a low-to-high transition at the input $IN+$ and a high-to-low transition at $IN-$. Before the transition, as both V_{in+} and V_{out+} are low, M_1 is OFF and M_3 is in the triode region. Meanwhile, M_2 is ON and M_4 is in the cut-off region as V_{in-} and V_{out-} are high. Right after this transition, M_1 turns to the saturation region and provides a path for the current of M_{inj} to discharge the loading capacitance at V_{out-}. As M_3 is still in the triode region, the loading capacitance at $OUT-$ is only partially discharged by M_1 with the rest bypassed by the low impedance of M_3. Thus, the V_{out-} transition from high-to-low is slow at the beginning. In the meantime, as both M_2 and M_4 are in the cut-off region, V_{out+} does not change. This state continues until V_{out-} is below $V_{DD} - |V_{TP}|$ so that M_4 enters the saturation region. Then M_4 provides current to charge the parasitic capacitance at $OUT+$. When V_{out+} increases,

it in turn speeds up the discharging at $OUT-$ by increasing the output resistance of M_3. A positive feedback is set up and the transitions at both outputs are very fast. Therefore the time delay from the input transition to the output transition is mainly taken to change the output from V_{DD} to $(V_{DD} - |V_{TP}|)$, which is modeled as the current from M_{inj} discharges the RC parallel network, formed by the loading capacitance and the low output resistance of the load transistor. This current from M_{inj} varies during the process of discharging in the architecture without the common source node sharing. This is due to the fact that before the input transition, M_{inj} is pushed into the triode region as M_4 is in the cutoff region and M_2 is ON. Therefore, after the input transition, M_{inj} has to take time to change from the triode region to the saturation region, which effectively reduces the average discharging current. As a result, the output frequency decreases. For the common source node sharing, after the output transition at one stage, its following stage undergoes transition, and sources the discharging current from M_{inj}. Therefore, M_{inj} stays in the saturation region, providing the constant current.

From the above discussion, the response of $V_{out\_fr}(t)$ from V_{DD} to $V_{DD} - |V_{TP}|$ could be modeled as a constant current I_B discharging a RC parallel network. Hence $V_{out\_fr}(t)$ can be approximated as,

$$V_{out\_fr}(t) \approx V_{DD} - (1 - e^{-t/R_{out}C_{out}})I_B R_{out} U(t) \tag{6.3}$$

where $U(t)$ is the step function. The time delay, t_d, defined as the time that it takes for the output to be changed from V_{DD} to $V_{DD} - |V_{TP}|$, is computed as,

$$t_{d\_fr} \approx R_{out}C_{out} \ln \frac{1}{1 - |V_{TP}|/(I_B R_{out})} \tag{6.4}$$

where R_{out} is the output resistance of M_3 in triode region, C_{out} is the loading capacitance at $OUT-$, including the parasitic capacitance and the input capacitance of

next stage. Thus the free running oscillation frequency is approximately given by the following expression,

$$f_{osc\_fr} \approx \frac{1}{2Nt_{d\_fr}} \tag{6.5}$$

where N is the number of stages in the ILFD.

b. Locking Range of the ILFD

We will first show that in the locked state, i.e. $f_{osc} = f_{inj}/2kN$, each stage sees the same time delay of its input signal and the injection signal. This conclusion provides the basis for us to predict the locking condition by analyzing the operation of a single stage.

Let us consider two stages, stage J and $(J+P)$. Assume that the input of stage J is expressed as $V_{in,J}(t)$. Under the locked state, if t_{d_inj} is the delay of one stage, the input of stage $(J+P)$ is delayed from $V_{in,J}(t)$ by $P \cdot t_{d\_osc}$, where $t_{d\_osc} = 1/(2Nf_{osc}) = k/f_{inj}$. Therefore $V_{in,P}(t)$ could be expressed as $V_{in,J}(t - Pk/f_{inj})$. Meanwhile, for the injection signal $V_{inj}(t)$, due to its periodic nature, $V_{inj}(t - Pk/f_{inj}) = V_{inj}(t)$. Since for the stage $(J + P)$, both its input and the injection signal could be regarded as being time delayed by Pk/f_{inj} from stage J, the response at stage $(J+P)$ is expected to be the same as stage J, only being time delayed by Pk/f_{inj}.

Assuming that the injection signal amplitude is small compared to V_{GS}, the bias current $I_b(t)$ is expressed as,

$$I_b(t) = I_B + g_{m_{inj}} V_{INJ} \sin(\omega_{inj} t + \phi) \tag{6.6}$$

where V_{INJ} is the amplitude of the injection signal.

Similar to the above discussion for the free running ILFD, we study the output response to $I_b(t)U(t)$ whose initial voltage level is V_{DD}. Again, we model this response

as a current source discharging C_{out} in parallel with R_{out}. The laplace transform of $I_b(t)$ in (6.6) is given by

$$I_b(s) = I_B\frac{1}{s} + g_{m_{inj}}V_{INJ}\frac{\omega_{inj}\cos\phi + s\sin\phi}{s^2+\omega_{inj}^2} \tag{6.7}$$

The transfer function $T(s)$ for a current discharging a RC parallel network is,

$$T(s) = -\frac{R_{out}}{1+sR_{out}C_{out}} \tag{6.8}$$

Therefore, the output voltage laplace transform is,

$$\begin{aligned}
V_{out}(s) =& I_b(s)\cdot T(s) \\
=& -I_B\frac{1}{s}\frac{R_{out}}{1+sR_{out}C_{out}} - g_{m_{inj}}V_{INJ}\frac{\omega_{inj}\cos\phi + s\sin\phi}{s^2+\omega_{inj}^2}\frac{R_{out}}{1+sR_{out}C_{out}} \\
=& -I_BR_{out}\frac{1}{s}\frac{1}{1+sR_{out}C_{out}} - g_{m_{inj}}V_{INJ}R_{out}\frac{1}{1+(R_{out}C_{out}\omega_{inj})^2} \\
& \Bigg[((R_{out}C_{out})^2\omega_{inj}\cos\phi - R_{out}C_{out}\sin\phi)\frac{1}{1+sR_{out}C_{out}} \\
& ((-R_{out}C_{out}\omega_{inj}\cos\phi + \sin\phi)s + (\omega_{inj}\cos\phi + R_{out}C_{out}\omega_{inj}^2\sin\phi))\frac{1}{s^2+\omega_{inj}^2}\Bigg]
\end{aligned} \tag{6.9}$$

The $V_{out}(s)$ in (6.9) is referred to V_{DD}. Using the inverse laplace transform, and

referring the V_{out} to ground, we have

$$\begin{aligned}
V_{out}(t) =& V_{DD} - I_B R_{out}(1 - e^{-t/R_{out}C_{out}}) - g_{m_{inj}} V_{INJ} R_{out} \frac{1}{1 + (R_{out}C_{out}\omega_{inj})^2} \\
& \big[(R_{out}C_{out}\omega_{inj} \cos\phi - \sin\phi)e^{-t/R_{out}C_{out}} + \\
& \cos\omega_{inj}t(-R_{out}C_{out}\omega_{inj}\cos\phi + \sin\phi) + \sin\omega_{inj}t(\cos\phi + R_{out}C_{out}\omega_{inj}\sin\phi)\big] \\
=& V_{DD} - I_B R_{out}(1 - e^{-t/R_{out}C_{out}}) \\
& - g_{m_{inj}} V_{INJ} R_{out} \frac{1}{1 + (R_{out}C_{out}\omega_{inj})^2} \cos\phi \\
& \big(\sin\omega_{inj}t - R_{out}C_{out}\omega_{inj}\cos\omega_{inj}t + R_{out}C_{out}\omega_{inj}e^{-t/R_{out}C_{out}}\big) \\
& - g_{m_{inj}} V_{INJ} R_{out} \frac{1}{1 + (R_{out}C_{out}\omega_{inj})^2} \sin\phi \\
& \big(\cos\omega_{inj}t + R_{out}C_{out}\omega_{inj}\sin\omega_{inj}t - e^{-t/R_{out}C_{out}}\big)
\end{aligned} \tag{6.10}$$

At $t = k/f_{inj} = 2\pi k/\omega_{inj}$,

$$\begin{aligned}
V_{out}(k/f_{inj}) =& V_{DD} - I_B R_{out}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \\
& + g_{m_{inj}} V_{INJ} R_{out} \frac{1}{1 + (R_{out}C_{out}\omega_{inj})^2} \\
& \cos\phi R_{out}C_{out}\omega_{inj}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \\
& - g_{m_{inj}} V_{INJ} R_{out} 1 + (R_{out}C_{out}\omega_{inj})^2 \\
& \sin\phi(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \\
=& V_{DD} - I_B R_{out}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \\
& \left[1 + \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{1 + (R_{out}C_{out}\omega_{inj})^2}(-R_{out}C_{out}\omega_{inj}\cos\phi + \sin\phi)\right]
\end{aligned} \tag{6.11}$$

The last term is limited by ϕ, as

$$|-R_{out}C_{out}\omega_{inj}\cos\phi + \sin\phi| \leq \sqrt{1 + (R_{out}C_{out}\omega_{inj})^2} \tag{6.12}$$

Therefore, $V_{out}(k/f_{inj})$ is bounded as,

$$V_{DD} - I_B R_{out}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \left(1 + \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + (R_{out}C_{out}\omega_{inj})^2}}\right) \leq V_{out}(k/f_{inj}) \leq V_{DD} - I_B R_{out}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \left(1 - \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + (R_{out}C_{out}\omega_{inj})^2}}\right) \quad (6.13)$$

The definition of t_{d_osc} requires $V_{out}(k/f_{inj})$ equal to $V_{DD} - |V_{TP}|$. We thus have

$$\begin{aligned} V_{DD} - I_B R_{out}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \left(1 + \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + (R_{out}C_{out}\omega_{inj})^2}}\right) &\leq V_{DD} - V_{TP} \leq \\ V_{DD} - I_B R_{out}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \left(1 - \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + (R_{out}C_{out}\omega_{inj})^2}}\right) & \\ \Rightarrow I_B R_{out}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \left(1 - \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + (R_{out}C_{out}\omega_{inj})^2}}\right) \leq V_{TP} \leq & \\ I_B R_{out}(1 - e^{-2k\pi/R_{out}C_{out}\omega_{inj}}) \left(1 + \frac{g_{m_{inj}} V_{INJ}}{I_B} \frac{1}{\sqrt{1 + (R_{out}C_{out}\omega_{inj})^2}}\right) & \end{aligned} \quad (6.14)$$

Since $\omega_{osc} = \omega_{inj}/2kN$,

$$R_{out}C_{out} = \frac{\pi}{N} \frac{1}{\omega_{osc\_fr} \ln \frac{1}{1 - |V_{TP}|/(I_B R_{out})}} \quad (6.15)$$

$$\omega_{osc} = 2\pi f_{osc} \quad (6.16)$$

$$\omega_{osc\_fr} = 2\pi f_{osc\_fr} \quad (6.17)$$

The ratio of f_{osc_inj}/f_{osc_fr} is limited by the following inequalities,

$$\left|1 - \frac{|V_{TP}|}{(1 - (1 - |V_{TP}|/(I_B R_{out}))^{f_{osc\_fr}/f_{osc\_inj}})}\right| \leq \frac{g_{m_{inj}} V_{INJ}}{I_B} \quad (6.18)$$

It is difficult to get an analytical solution for f_{osc} from (6.18). However, some insights

could still be derived. If $V_{INJ} = 0$, i.e., there is no signal injected, as expected, (6.18) has only one solution, which is $f_{osc} = f_{osc\_fr}$. In other words, this indicates that the free running oscillation frequency f_{osc_fr} falls into the locking range. With the increase of V_{INJ}, the range of f_{osc} that meets (6.18) is extended. (6.18) also predicts the existence of multiple division ratios, shown as $2kN$, as k appears in (6.18). However, with larger k, the conditions for f_{osc} to meet the inequality become tight, leading to the decrease of the locking range.

CHAPTER VII

VCO

A. Oscillation Start-up Condition

VCO generates periodic signals without an external source. The oscillation mechanism of VCO could be generally explained by feedback theory. Consider a linear feedback system shown in Fig. 89. Its transfer function is given by

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)} \tag{7.1}$$

Oscillation happens if a stable periodic signal is produced, which means, according to (7.1), at a certain frequency ω_o, $H(j\omega_o) = 1$. This observation leads to the so-called Barkhausen's criteria, which is more often described as the simultaneous satisfaction of the following two conditions at ω_o,

1. The loop gain, $|H(j\omega_o)|$ must be unity.

2. The phase shift, $\angle H(j\omega_o)$ must be integer times of 360°

While Barkhausen's criteria explains the steady state of VCO, it does not give hints on how VCO transfers its own noise into periodic signal with certain amplitude. Actually, during oscillation start-up, the loop gain $|H(j\omega_o)|$ must be larger than unity to amplify noise at ω_o. The nonlinearity of VCO would eventually limit the amplitude

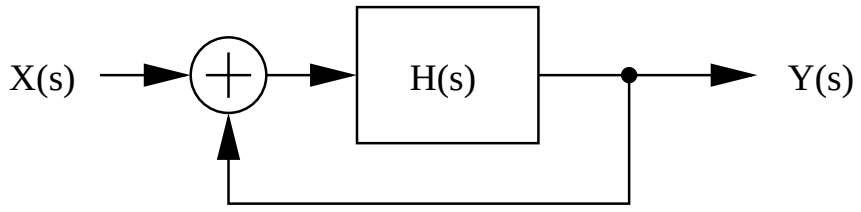


Fig. 89. Feedback oscillatory system

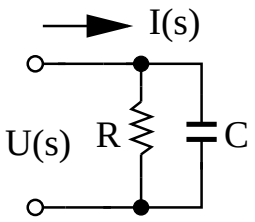


Fig. 90. A typical RC network used in VCO

of the signal to a certain level, arriving at the steady state when the average loop gain is unity.

B. VCO Architecture

1. RC-VCO and LC-VCO

The oscillation mechanism explained in the previous section suggests two necessary components for VCO. Active devices provide amplification of the signal and therefore ensure loop gain larger than unity. Phase shift networks, normally consist of passive components, ensure $\angle H(j\omega_o)$ to be integer times of 360°. While active devices themselves could amplify signals across large frequency range, phase shift networks only provide needed phase shift at certain frequencies. Therefore, the oscillation frequency is normally set by the phase shift networks. Depending on the types of the components that make up the phase shift networks, VCOs can be categorized as RC VCOs and LC VCOs. A typical RC network is shown in Fig. 90. The parallel connection of R and C forms a one-pole low-pass filter, with the impedance given as,

$$Z(s) = \frac{U(s)}{I(s)} = \frac{R}{1 + sRC} \tag{7.2}$$

(7.2) unveils several important properties of RC VCOs. First, phase shift of one RC network reaches its maximum value as 90° when frequency goes to infinity. Since at infinity frequency the loop gain could not be larger than unity as $Z(s)$ approaching

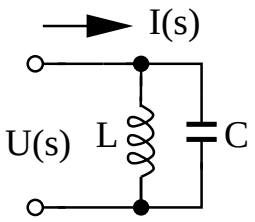


Fig. 91. A typical LC network in VCO

zero, to meet Barkhausen's criteria, RC VCO needs at least cascading three RC networks to provide minimum oscillation phase shift as 180°, assuming DC feedback is negative. Second, the phase noise performance is generally poor, as R is noisy and sets the time constant RC that determines the oscillation frequency. Navid et al [28] show the following equation for the minimum achievable phase noise of RC VCO,

$$PN_{min}(\Delta f) \approx \frac{7.33kT}{P_{min}} \left(\frac{f_o}{\Delta f}\right)^2 \tag{7.3}$$

where PN_{min} is minimum phase noise for a given power, Δf is offset frequency, f_o is oscillation frequency, k is Boltzmann constant and P_{min} is minimum power dissipation. (7.3) shows that PN_{min} is inferior to that of LC VCO, which will be presented later.

One advantage of RC VCO is that the die area of RC VCO is normally compact as both R and C occupy relatively small area. Indeed, many RC VCOs just use the loading capacitance from active devices as C, further shrinking the die area. Moreover, the tuning range of RC VCO is wide especially when R is implemented by transistor, which could be tuned from linear region to cutoff region.

Fig. 91 shows a typical LC network, with the impedance given as,

$$Z(s) = \frac{U(s)}{I(s)} = \frac{sL}{1 + s^2LC} \tag{7.4}$$

(7.4) shows that the phase shift is 180° when frequency is across the resonance frequency $f_o = 1/2\pi\sqrt{LC}$. Therefore, only one LC network is needed to meet

Barkhausen's criteria. Also, as f_o is only dependent on noiseless components L and C, the LC VCO phase noise performance is generally good. Herzel et al [29] show the phase noise of a single stage differential LC VCO is given by,

$$PN_{min}(\Delta f) \approx \frac{1.67kT}{Q^2 P_{min}} \left(\frac{f_o}{\Delta f}\right)^2 \tag{7.5}$$

where Q is the quality factor of inductor normally larger than unity and expressed as $\omega L/R_s$; R_s is the resistor in series with L, which represents the loss of the inductor. Compared with (7.2), for a given power dissipation and oscillation frequency, the LC VCO achieves phase noise roughly $4Q^2$ less than the RC VCO. The disadvantages of LC VCO include large die area (due to inductors) and small tuning range.

2. Single-stage VCO and Multi-stage VCO

Single stage VCO gains its popularity due to its compact size and good phase noise. However, this type of VCO fails to provide multi-phase outputs that are essential to some applications such as direct conversion wireless systems and half-rate clock and data recovery systems. On the contrary, as multi-stage VCO consists of several identical stages, it is able to generate multi-phase outputs. The penalties include increased power dissipation, worse phase noise and larger die area.

C. Quadrature Signal Generation

The generation of quadrature signal is essential toward implementation of several widely used communications systems. Quadrature signal, for example, is required for modulation/demodulation in direct conversion architecture, which is the most promising solution for full integration of wireless transceiver on a single chip. Another example could be found in half-rate clock and data recovery (CDR) system [30], where

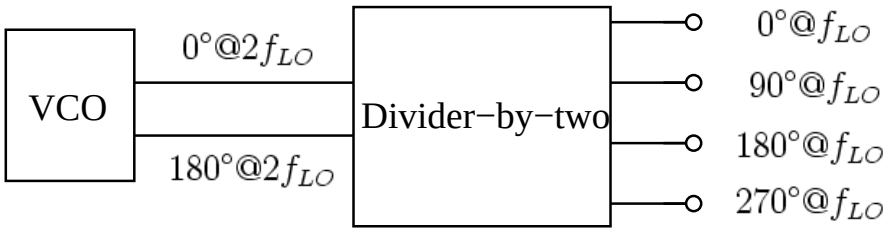


Fig. 92. Quadrature signal generation by divider-by-two

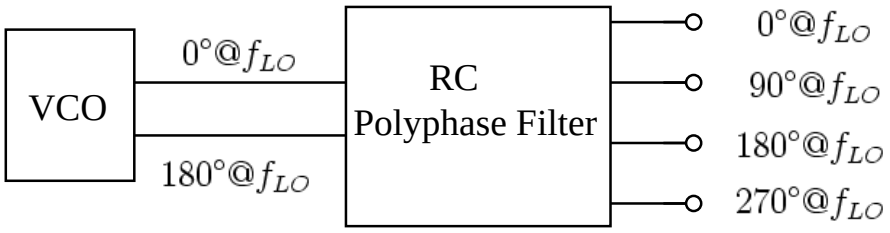


Fig. 93. Quadrature signal generation by RC polyphase filter

quadrature signal helps to slow down the operation speed of the most critical sampling block. One kind of quadrature signal generation circuits consist of a VCO and a divider-by-two [31]. Shown in Fig. 92, the differential VCO output signal is sent to the divider-by-two, where the frequency is lowered by half and quadrature signal is produced. The main drawback comes from the fact that the VCO oscillation frequency is doubled, resulting in the increased power consumption. Also the phase accuracy is heavily dependent on the duty cycle of the VCO output. A VCO followed by a passive RC polyphase filter is another approach to generate quadrature signal [32], as shown in Fig. 93. While transforming the differential VCO output to quadrature signals, the passive RC polyphase filter, however, attenuates the signal. To resume the required signal level for driving subsequent circuits, power-hungry buffers have to be added. Another issue is the phase accuracy. Especially at high frequency, while RC constant has to be lowered accordingly, the parasitic capacitance adds uncertainty in determination of output phases. A third approach of quadrature signal

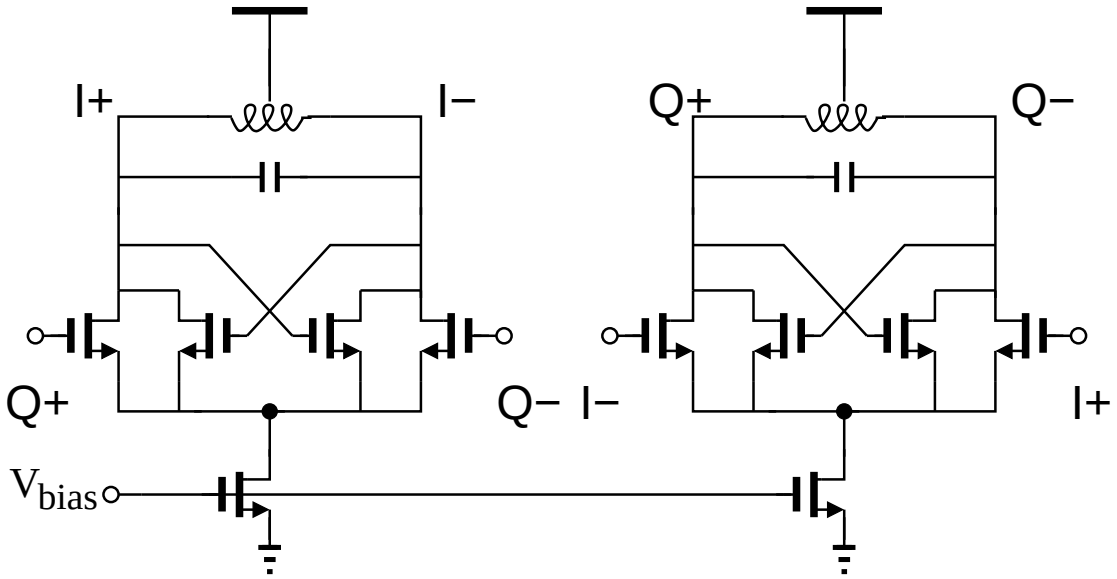


Fig. 94. A conventional QVCO

generation is to utilize the multi-stage VCO [33]. This approach minimizes the number of components and thus demands the least power consumption.

D. Quadrature VCO Design

1. Introduction

A conventional LC-QVCO is shown in Fig. 94. It consists of two identical LC-VCO stages coupled to each other. A problem of the conventional LC-QVCO is bi-modal oscillation, meaning the oscillator can have two stable oscillation frequency for the same control condition. [2, 3, 33] rely on the asymmetrical frequency response of resonator to obtain a unique oscillation frequency. However, recently Li et al [5] did observe the bi-modal oscillation during measurements. [5] continued to propose to add some phase shift in the coupling pairs to solve the oscillation ambiguity. Other phase shift LC-QVCO strictures have been reported in existing literatures [3, 4]. However, those existing solutions suffer from various problems, such as poor phase noise, limited

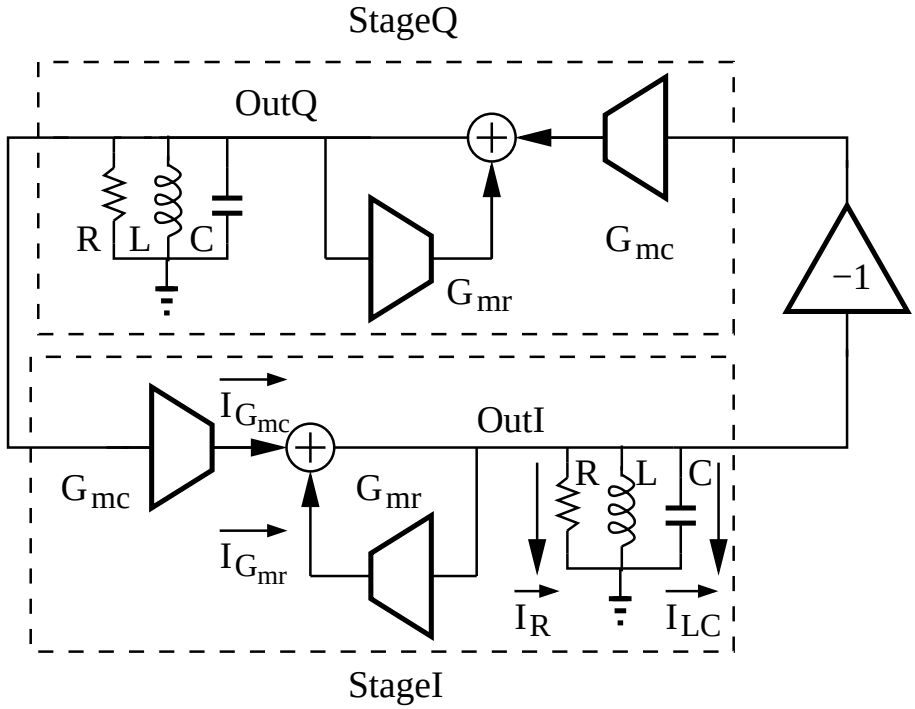


Fig. 95. Small signal model of QVCO

voltage headroom.

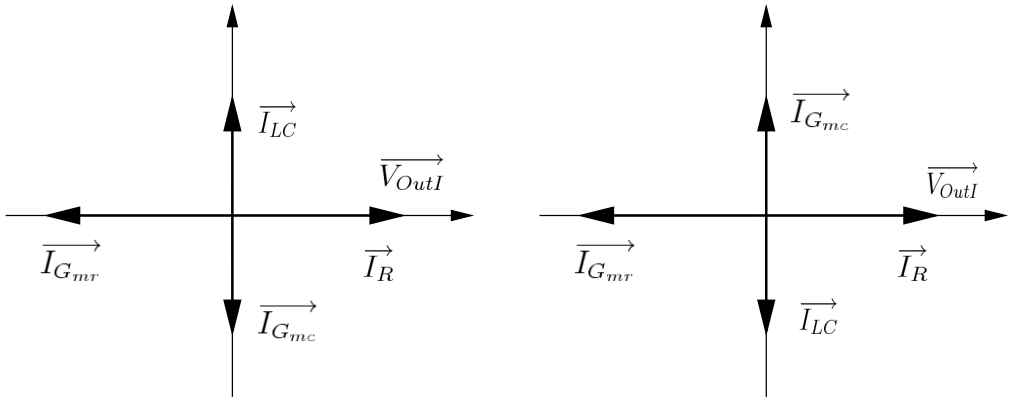
2. Bi-modal Oscillation

Fig. 95 shows a linear model for a general QVCO. $G_{mc}(s)$ represents the coupling part, $G_{mr}(s)$ represents the local feedback part and the RLC parallel network is the equivalent circuit for the LC resonator. The transfer function of each of the QVCO stages is expressed as,

$$H|_{I,Q}(s) = \frac{G_{mc}(s)sL}{s^2LC - \left(G_{mr}(s) - \frac{1}{R_p}\right)sL + 1} \tag{7.6}$$

The loop transfer function $H(s)$ is given by,

$$H(s) = -H_I(s)H_Q(s) \tag{7.7}$$



(a) *StageI* leads *StageQ* by 90° (b) *StageI* lags *StageQ* by 90°

Fig. 96. Phasor diagram of conventional QVCO

As $H_I(s)$ and $H_Q(s)$ are identical, (7.7) shows when the oscillation is stable, $H|_{I,Q}(j\omega_o) = \pm j$, confirming that quadrature signals are generated. In the conventional QVCO case, both $G_{mc}(s)$ and $G_{mr}(s)$ are real positive numbers. The conventional QVCO loop transfer function could therefore be given as,

$$H(s)|_{conv} = -\left(\frac{G_{mc}sL}{s^2LC - \left(G_{mr} - \frac{1}{R_p}\right)sL + 1}\right)^2 \tag{7.8}$$

While the phase requirement of Barkausen's criteria demands $G_{mr} = \frac{1}{R_p}$, there are two possible oscillation frequencies that can meet the magnitude requirement [2], and they are given as follows,

$$\omega_{1,2} = \frac{1}{\sqrt{LC}}\sqrt{1 + \frac{1}{4}\frac{G_{mc}^2 L}{C}} \pm \frac{G_{mc}}{2C} \tag{7.9}$$

Assuming $G_{mc} \leq G_{mr}$, since $G_{mr}L = 1/\omega_o Q$, ω_1 and ω_2 are approximated as,

$$\omega_{1,2} \approx \omega_o \pm \frac{G_{mc}}{2C} \tag{7.10}$$

The co-existence of the two possible oscillation frequencies (called bimodal oscillation in [5]) could also be explained through phasor diagrams as shown in Fig. 96. The current flowing out of node $OutI$ in Fig.95 could be decomposed into four parts, as $\overrightarrow{I_{G_{mr}}}$, $\overrightarrow{I_{G_{mc}}}$, $\overrightarrow{I_R}$ and $\overrightarrow{I_{LC}}$. While $\overrightarrow{I_R}$ is always in phase with $\overrightarrow{V_{OutI}}$, $\overrightarrow{I_{G_{mr}}}$ is always out of phase. Both $\overrightarrow{I_{G_{mc}}}$ and $\overrightarrow{I_{LC}}$ can only be either $-90°$ or $+90°$ phase shift from $\overrightarrow{V_{OutI}}$. Since the sum of those four currents has to be zero, $|\overrightarrow{I_R}|$ has to be equal to $|\overrightarrow{I_{G_{mr}}}|$, leading to $G_{mr} = 1/R$. Fig. 96(a) shows that when $StageI$ leads $StageQ$ by $90°$, $\angle\overrightarrow{I_{G_{mc}}}$ is $-90°$. As a result, $\angle\overrightarrow{I_{LC}}$ has to be $+90°$, indicating the oscillation frequency is higher than the LC resonance frequency. Fig.96(b) shows when $StageI$ lags $StageQ$ by $90°$, $\angle\overrightarrow{I_{G_{mc}}}$ is $+90°$ and $\angle\overrightarrow{I_{LC}}$ is $-90°$, indicating the oscillation frequency is lower than the LC resonance frequency.

Bimodal oscillation is jeopardous for a VCO, because even for a fixed control voltage, the oscillation frequency is out of control. [33] argues that in practice, a unique oscillation frequency is assured as the practical resonator shows asymmetric phase and magnitude responses across its resonance frequency. Fig. 97 are the example plots shown in [33]. The QVCO [33] has $G_{mr} = G_{mc}$, leading to the phase as $\pm 45°$ from the resonator, which appear at three frequencies, f_1, f_2 and f_3. But since at f_3, the magnitude and thus the loop gain are the distinctively largest, this frequency becomes the only solution that is stable. While the above argument has been deemed as true in several publications such as [3] and [2], Li et al. demonstrated in a recent paper [5] that bi-modal oscillation did happen in a QVCO measurement. Li et al. continued to argue that as the frequency characteristics of the resonator is determined by many parameters/components, there is no guarantee that a resonator will always have the same asymmetrical characteristics to favor one over the other. To investigate the frequency characteristics of the resonator used in our implementation, we follow [33]'s approach by searching which mode has larger magnitude in how much amount along

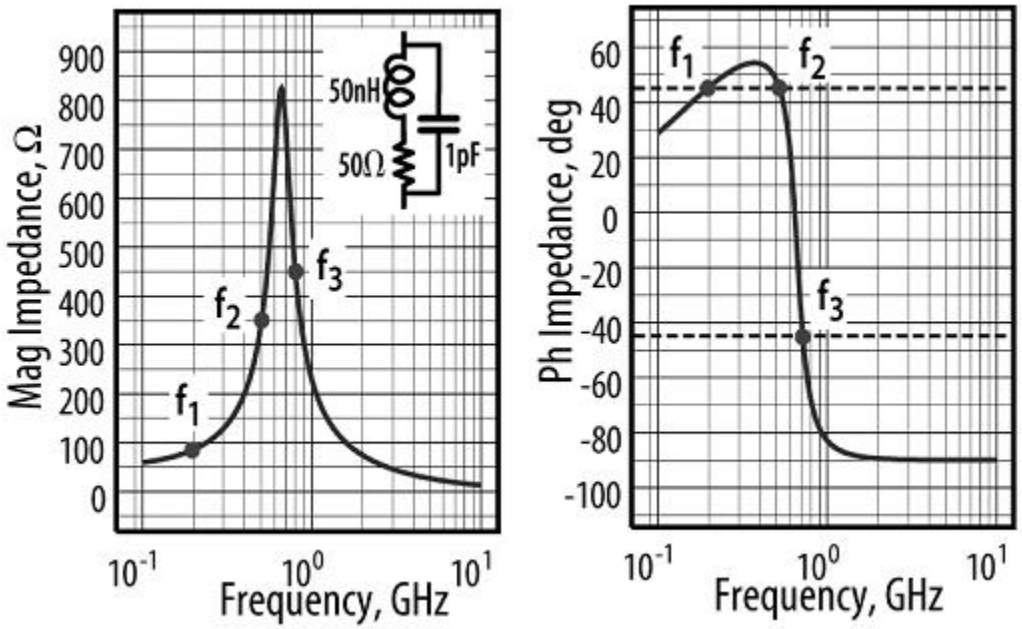
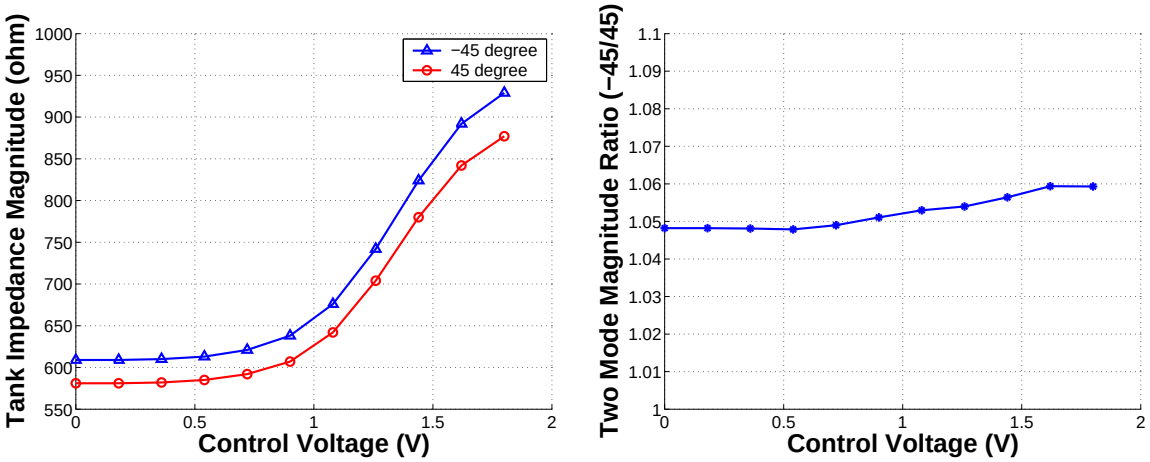
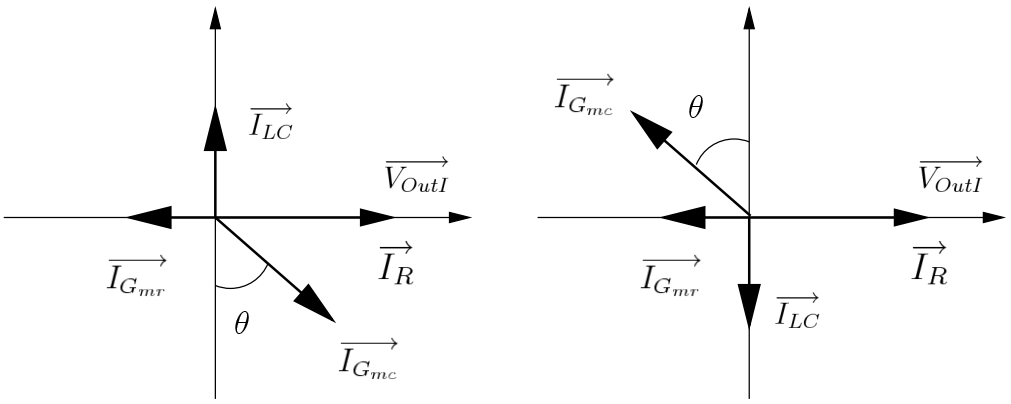


Fig. 97. LC resonator frequency response in [33]



(a) (b)

Fig. 98. Frequency response of the implemented LC resonator across the whole tuning range



(a) *StageI* leads *StageQ* by 90° (b) *StageI* lags *StageQ* by 90°

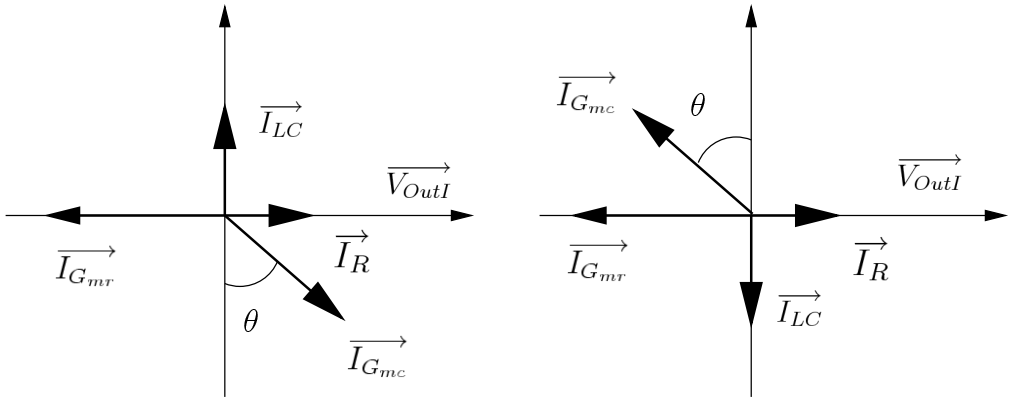
Fig. 99. Phasor diagram of QVCO with phase shift when $G_{mr} < \frac{1}{R}$

the whole tuning range. Fig. 98 shows the simulation results. As can be seen, along the whole control voltage range, the tank impedance magnitude at the frequency with $-45°$ is always larger than the 45° one. However, the magnitude difference is very marginal, and therefore, easily subject to the problem of bi-modal oscillation.

3. Bi-Modal Suppression and Oscillation Frequency

a. Bi-Modal Suppression Theory

[5] proposed to add some phase shift at G_{mc} stage so that the QVCO will favor only one mode. We prove this approach by using the phasor diagram shown in Figs. 99 and 100. Assuming a positive phase shift θ within the range $0 < \theta < 90°$, Fig. 99 shows that if $G_{mr} < 1/R$, the only chance for the sum of the currents to be zero is *StageI* lags *StageQ* by 90°, while the oscillation frequency is lower than the LC resonance frequency. Fig. 100 shows that if $G_{mr} > 1/R$, the only chance for the sum of the currents to be zero is *StageI* leads *StageQ* by 90° while the oscillation frequency is higher than the LC resonance frequency.



(a) *StageI* leads *StageQ* by 90° (b) *StageI* lags *StageQ* by 90°

Fig. 100. Phasor diagram of QVCO with phase shift when $G_{mr} > \frac{1}{R}$

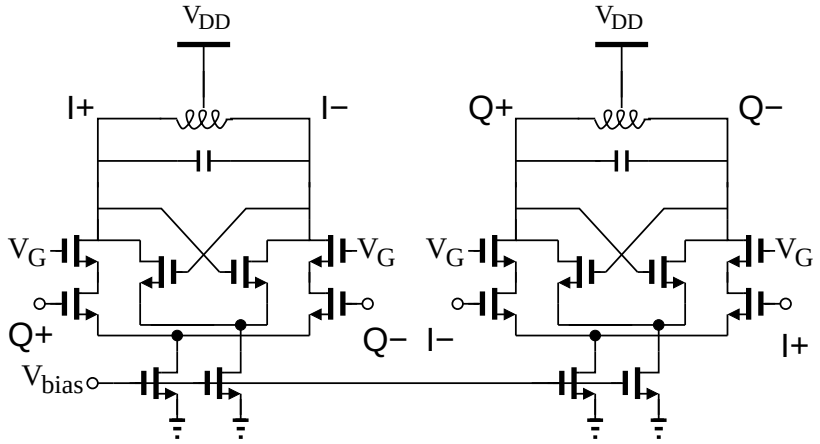


Fig. 101. Bi-modal suppression QVCO in [5]

The additional benefit of the phase shift approach is that the phase noise of the QVCO is reduced. This is so because the introduction of the phase shift in the G_{mc} cell reduces the required phase from the resonator to meet Barkausen's phase criteria. Therefore, the oscillation frequency is made closer to the resonance frequency, where Q reaches its peak value to filter noise to the most extent.

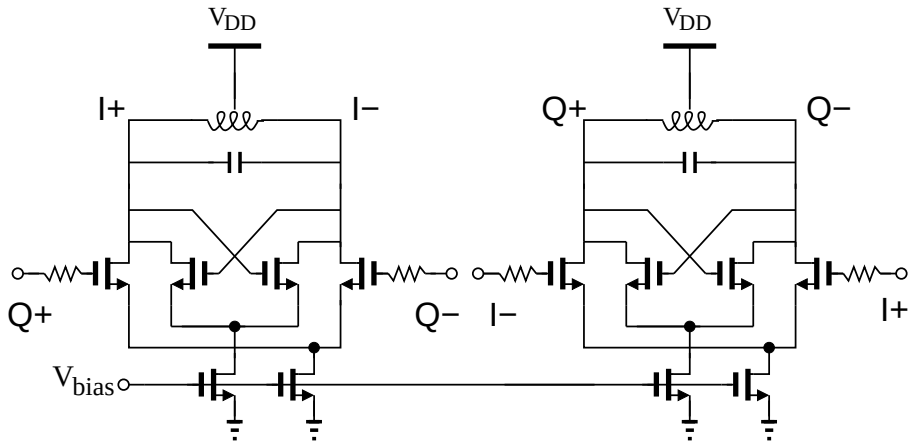


Fig. 102. Phase-shift QVCO in [4]

b. Existing Bi-modal Suppression Solutions

[5] suggests to replace the normal differential common source coupling stage with a differential cascode (common-source and common-gate) configuration, shown in Fig 101. In this way, an additional phase shift is generated at the source node of the common-gate transistor. However, the phase shift is normally limited and may not be sufficient to suppress the bi-modal oscillation, because this source node only provides a pole at very high frequency. Also the usage of cascode configuration decreases the voltage headroom, unsuitable for low-voltage operation. There are some publications discussing other phase shift techniques. Although their main target is to improve the phase noise performance, they help to suppress the bi-modal oscillation as Figs. 99 and 100 show. Valla et al. [4] adds a resistor at the gate of the each coupling transistor to build a RC low-pass network with the gate capacitance, as shown in Fig. 102. However, the phase noise performance would be degraded because of the following two reasons. First, the resonator Q is reduced as the RC network is in parallel with the resonator. Second, the resistor itself is an extra noise source. Tang et al. [3] inserts phase-shifters in between the oscillator stages, as shown in Fig. 103. However, similar to [4]'s approach, the limited g_m of the transistor inside the phase-shifter not

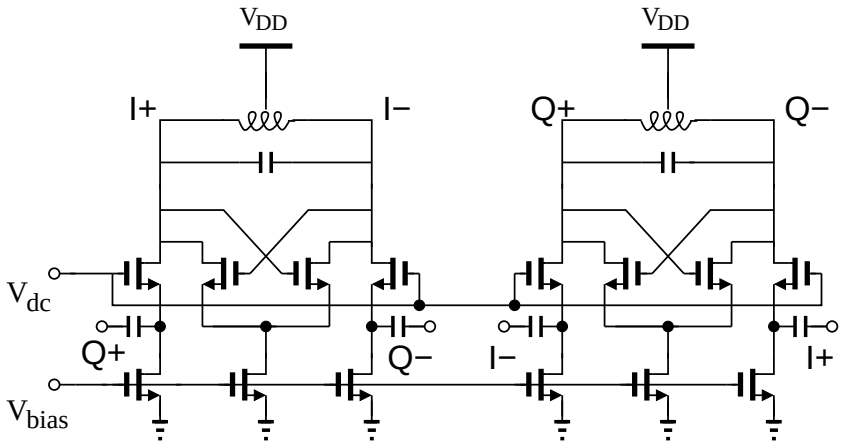


Fig. 103. Phase-shift QVCO in [3]

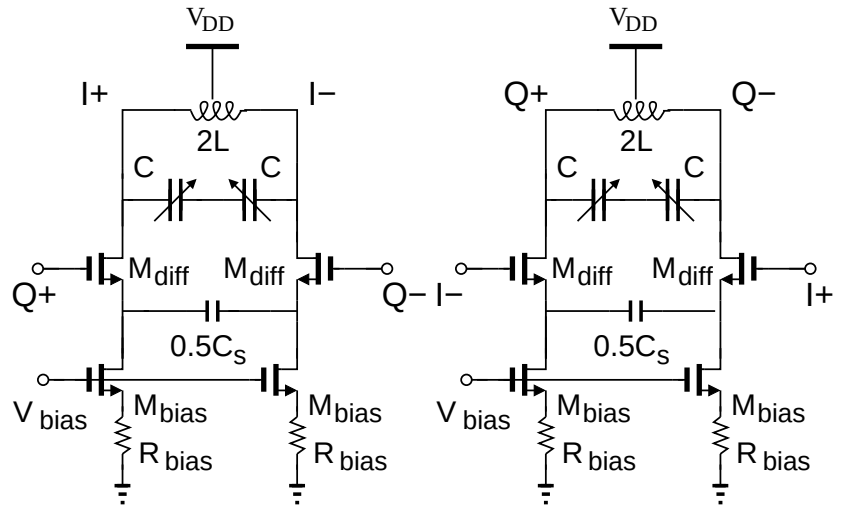


Fig. 104. Proposed capacitive source degeneration QVCO

only degrades the resonator Q but also brings extra noise.

4. The Proposed Bi-modal Suppression QVCO

a. Structure of the Proposed QVCO

A capacitive source degeneration QVCO (CSD-QVCO) is proposed to suppress bi-modal oscillation, as shown in Fig. 104. The capacitive source degeneration provides

a certain amount of phase shift from its input to output so that only one oscillation is favored. The placement of the Cs in between the two source nodes instead of from each source node to ground is for two reasons: in the latter case, first each capacitance has to be doubled with area penalty; secondly, the oscillator is subject to common-mode oscillation [34]. The phase noise performance is superior as the capacitors Cs are noiseless and do not contribute any phase noise. The commonly used positive feedback differential pairs are removed as the the capacitive source degeneration differential pairs can provide necessary negative resistive input loads for the oscillation startup.

b. Coupling Stage Phase Shift

The coupling transconductance G_{Mc} is expressed as,

$$G_{Mc} = \frac{sC_s}{1 + s(C_s + C_{gs})/g_m} \tag{7.11}$$

Therefore, the phase shift β in the coupling stage is calculated as,

$$\beta = 90^\circ - \arctan(\omega(C_s + C_{gs})/g_m) \tag{7.12}$$

c. Oscillation Frequency and Resonator Phase Shift

The CSD-QVCO loop transfer function is given by,

$$G(s) = -G_{Mc}^2 \left(\frac{sL}{1 + sL(\frac{1}{R_P} - G_{Mr}) + s^2LC} \right)^2 \tag{7.13}$$

$$= - \left(\frac{s^2}{1 + s(C_s + C_{gs})/g_m} \cdot \frac{LC_s}{1 + sL(\frac{1}{R_P} - G_{Mr}) + s^2LC} \right)^2 \tag{7.14}$$

where G_{Mr} is the negative conductance at the input of the capacitive source degeneration differential pair, which is expressed as,

$$G_{Mr} = g_m \cdot \frac{\omega^2 C_s C_{gs}}{g_m^2 + \omega^2 (C_s + C_{gs})^2} \tag{7.15}$$

According to Barkausen's phase criteria, the circuit oscillates when the phase of $G(j\omega)$ is 0°. To satisfy this condition, $(1 + sC_L/g_m) \cdot (1 + sL(1/R_P - G_M) + s^2 LC)|_{s=j\omega}$has to be a pure imaginary number, which leads to

$$\begin{aligned} &\omega^2 \left(LC + LC_L/g_m \left(1/R_P - G_m\right)\right) = 1 \\ \Rightarrow &\omega_{osc} = \sqrt{\frac{1}{LC\left(1 + \frac{C_L}{g_m R_p C}\left(1 - G_M R_P\right)\right)}} \\ \Rightarrow &\omega_{osc} \approx \omega_0 \left(1 - \frac{1}{2}\frac{1}{AQ}\left(1 - G_M R_P\right)\right) \end{aligned} \tag{7.16}$$

where $Q = \omega_o/CR_p$ is the quality factor of the tank, $A = g_m/\omega_o C_L$. Notice here only one solution is obtained, which theoretically validates the complete suppression of bimodal oscillations. Also (7.16) agrees well with the phasor diagrams in Figs. 99 and 100 in showing the oscillation frequency dependence on the polarity of $G_{mr} - 1/R$.

Calculating the resonator phase shift $\Delta\phi$ from the definition $Q = (\omega_0/2)(\Delta\phi/\Delta\omega)$, where $\Delta\omega = \omega_{osc} - \omega_0$, we get

$$\Delta\phi = -\frac{(C_s + C_{gs})\omega_0}{g_m}\left(1 - G_{mr}R\right) \tag{7.17}$$

According to (7.14) and (7.16), $G(j\omega_{osc})$ is expressed as,

$$G(j\omega_{osc}) = \left[\frac{\omega_{osc} C_s}{\left(\left(\frac{\omega_{osc}(C_s + C_{gs})}{g_m}\right)^2 + 1\right)\left(1 - G_{mr}R\right)}\right]^2 \tag{7.18}$$

As at oscillator steady state $G(j\omega_{osc}) = 1$, (7.18) leads to

$$|1 - G_{mr}R| = \frac{\omega_{osc}C_s}{\left(\frac{\omega_{osc}(C_s + C_{gs})}{g_m}\right)^2 + 1} \tag{7.19}$$

Using (7.16), (7.18) can be rewritten as

$$\begin{aligned} |1 - G_{mr}R| =& R|G_{mc}|\cos\beta\frac{g_m}{\omega_{osc}(C_s + C_{gs})} \\ \approx& R|G_{mc}|\cos\beta\frac{g_m}{\omega_0(C_s + C_{gs})} \end{aligned} \tag{7.20}$$

Therefor, (7.17) can be rewritten as

$$\Delta\phi = \pm R|G_{mc}|\cos\beta \tag{7.21}$$

where the polarity of $\Delta\phi$ depends on that of $G_{mr} - 1/R$.

As a comparison, we calculate the resonator phase shift for a conventional QVCO without phase shift in coupling pair. According to (7.10),

$$\Delta\omega = \pm\frac{1}{2}\frac{G_{mc}}{C} \tag{7.22}$$

Therefore, $\Delta\phi$ is derived as

$$\begin{aligned} \Delta\phi =& \pm\frac{Q}{\omega_0}\frac{G_{mc}}{C} \\ =& \pm RG_{mc} \end{aligned} \tag{7.23}$$

(7.21) and (7.23) verify that the introduction of phase shift β in coupling pair reduces the resonator phase shift and make the oscillation frequency closer to the resonance frequency.

d. Start-up Conditions

The CSD-QVCO The CSD-QVCO start-up condition is expressed as

$$\left| G_{mc}^2 \left(\frac{sL}{1 + sL(\frac{1}{R} - G_{mr}) + s^2 LC} \right)^2 \right|_{s=j\omega_{osc}} > \alpha_{min} \tag{7.24}$$

where α_{min} is the minimum loop gain for the startup condition. Normally α_{min} is selected as 3 [35] to ensure worst case startup and overcome process variations. Substituting (7.16) into (7.24) results in a rather complicated inequality. But since in the CSD-QVCO, the oscillation frequency ω_{osc} is approximately equal to tank resonance frequency ω_o. We have

$$|G_{mc}| > \sqrt{\alpha_{min}} \left| \frac{1}{R} - G_{mr} \right| \tag{7.25}$$

(7.25) can be decomposed into two cases. Decompose (7.25) into

$$\begin{cases} \dfrac{|G_{mc}|}{\sqrt{\alpha_{min}}} + G_{mr} > \dfrac{1}{R} & \text{(7.26a)} \\ \dfrac{|G_{mc}|}{\sqrt{\alpha_{min}}} + \dfrac{1}{R} > G_{mr} & \text{(7.26b)} \end{cases}$$

According to (7.11) and (7.15), G_{mr} is related to G_{mc} as,

$$G_{mr} = |G_{mc}| \frac{1}{\sqrt{\left(\dfrac{\omega_T}{\omega}\right)^2 + \left(\dfrac{C_s + C_{gs}}{C_{gs}}\right)^2}} \tag{7.27}$$

where ω_T is transistor unity gain frequency and is expressed as $\omega_T = g_m / C_{gs}$.

Substituting (7.27) into (7.26a) results in (7.29a). For (7.26b), it is transformed to (7.28a) and (7.28b).

$$\begin{cases} \dfrac{1}{R}\dfrac{\sqrt{\alpha_{min}}\sqrt{\left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2}}{\sqrt{\alpha_{min}}-\sqrt{\left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2}} \\ > |G_{mc}| > \dfrac{1}{R}\sqrt{\left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2} & \text{if } \alpha_{min} > \left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2 \end{cases} \tag{7.28a}$$

$$\begin{cases} |G_{mc}| > \dfrac{1}{R}\sqrt{\left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2} & \text{if } \alpha_{min} < \left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2 \end{cases} \tag{7.28b}$$

$$\begin{cases} \dfrac{1}{R}\sqrt{\left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2} \\ > |G_{mc}| > \dfrac{1}{R}\dfrac{\sqrt{\alpha_{min}}\sqrt{\left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2}}{\sqrt{\alpha_{min}}+\sqrt{\left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2}} & \text{if } G_{mr} < 1/R \quad (7.29a) \\ |G_{mc}| > \dfrac{1}{R}\sqrt{\left(\frac{\omega_T}{\omega}\right)^2+\left(\frac{C_s+C_{gs}}{C_{gs}}\right)^2} & \text{if } G_{mr} > 1/R \quad (7.29b) \end{cases}$$

In practice, as the operating frequency ω is much less than ω_T and $\alpha_{min} = 3$ is enough to ensure oscillation, i.e. condition of (7.28b) is always satisfied, (7.28a) and (7.28b) are reduced to (7.29b).

For G_{mr} less than $1/R$ case, the value of $|G_{mc}|$ has to be chosen within a small range, which is problematic for practical concerns. Indeed, $|G_{mc}|$ is determined by many factors, such as transistor size, bias current, source degeneration and parasitic capacitors, oscillation frequency, etc. There is no guarantee that the oscillator always stays in this case under process, voltage supply and temperature variations. On the other hand, for G_{mr} larger than $1/R$ case, as long as $|G_{mc}|$ is large enough, the

oscillator is ensure to operate.

e. Phase Error By Coupling Mismatch

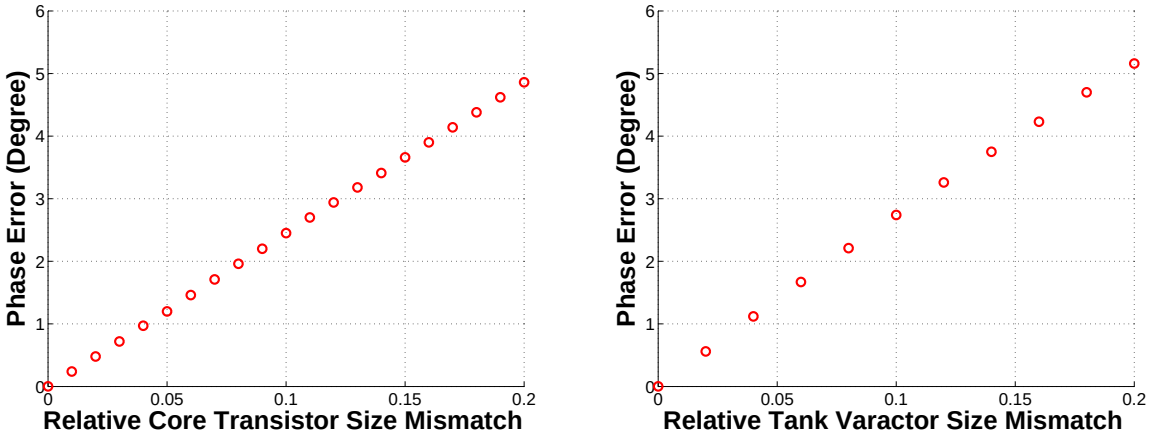
Because of mismatches between two stages, phase error exists in QVCO. We categorize the sources of mismatches into two kinds, LC tank mismatch and transistor mismatch. [4] shows that the phase error induced by mismatches between the two LC tanks is given by,

$$\phi_{err} \approx \frac{Q^2 \Delta\omega^2}{\omega_o^2} \left(\frac{G_{mr}}{G_{mc}} \right) \frac{360^\circ}{2\pi} \tag{7.30}$$

where $\Delta\omega$ is the frequency difference between the oscillation frequency and the resonance frequency. (7.30) shows that the phase error could be reduced by pushing the oscillation frequency close to the resonance frequency. On the other hand, the transistor mismatch is more serious, not only because the physical size of transistors is smaller than the physical size of inductors and varactors, but because other sources contribute to mismatches, such as doping levels in channels and gates [9]. For a conventional QVCO, [36] presents that the phase error induced by the feedback differential pair mismatch is expressed as,

$$\phi_{err} \approx \arcsin(\Delta G_{mr}/2G_{mc}) \tag{7.31}$$

The phase errors caused by tank and transistor mismatch in the proposed CSD-QVCO are at similar levels, as illustrated in Fig. 105. If the phase error, for example, is required to be below 1°, the mismatch of the tank and transistor cannot surpass 5%, which are quite feasible in this technology.



(a) Phase error versus core transistor W/L mismatch

(b) Phase error versus tank capacitance

Fig. 105. Phase error in CSD-QVCO

f. Phase Noise

A general LC-QVCO phase noise expression [3] can be given as,

$$\mathcal{L}(\Delta f) = 10\log\left(\frac{1}{16}\cdot\frac{1}{(Q\cos\phi)^2}\cdot\left(\frac{f_{osc}}{\Delta f}\right)^2\cdot\frac{\overline{i_n^2}}{i_{carrier}^2}\right) \tag{7.32}$$

where Q is the quality factor of the LC resonator, $\overline{i_n^2}$ is the total current noise and $i_{carrier}^2$ is the squared rms carrier current. (7.32) shows the less the phase shift from the resonator, the less the phase noise is produced. In the proposed CSD-QVCO, $|\phi|$ is reduced from the conventional approach and thus helps to reduce the phase noise.

Low-frequency bias noise degrades phase noise not only through varactor AM-PM conversion and differential pair nonlinearity, but also through direct ways of changing coupling between the two stages. First, we consider the low-frequency noise appearing at the node G where the gates of bias transistors are connected together. From (**??**), it is obvious that the oscillation frequency ω_{osc} is a function of degeneration factor A, which depends on the current provided by bias. Any voltage fluctuation on node G

thus leads to the change of the oscillation frequency and generates phase noise, which can be expressed as

$$\begin{aligned}\frac{\mathrm{dBc}}{Hz}(\Delta\omega) &= \frac{1}{2(\Delta\omega)^2}\left|\frac{\partial\omega_{osc}}{\partial V_G}\right|\overline{v_g^2}(\Delta\omega) \\ &= \frac{1}{64(\Delta\omega)^2}\cdot\frac{\omega_{osc}^4 C_L^2}{I_B^3 Q^2 \mu_n C_{ox}(W/L)_D}\cdot g_{mB}^2\overline{v_g^2}(\Delta\omega) \end{aligned} \tag{7.33}$$

To minimize this type of phase noise, a low pass filter is preferred between the node G and the noisy voltage source. Also the decrease of effective g_{mB} of the bias transistors helps transfer less noise current to the oscillator. A source degeneration technique is utilized in this design to suppress the noise by a factor of $1 + g_{mB}R_{sB}$.

5. Circuit Implementation

Two CSD-QVCOs are implemented at different frequencies, i.e. 5 GHz and 4.2 GHz. The former is to push the frequency to higher limit and achieve best phase noise performance while the latter is tailored to the UWB application.

a. Inductor

The proposed CSD-QVCO use differential inductor due to its higher quality factor and smaller silicon area [37]. Fig. 106 shows the layout of the differential inductor. Top metal layer is used for the inductor wire because of the two reasons. Firstly, top metal layer is far away from the substrate, reducing the coupling capacitance to the ground and loss from the substrate. Secondly, top metal layer itself is made of thick metal so that the series resistance is minimized for the benefit of quality factor. Fig.107 presents simulated inductance and quality factor across the frequency range of interest in the two cases. The parallel conductances are roughly 1.4 mS for the 5-GHz CSD-QVCO and 0.9 mS for the 4.2-GHz CSD-QVCO.

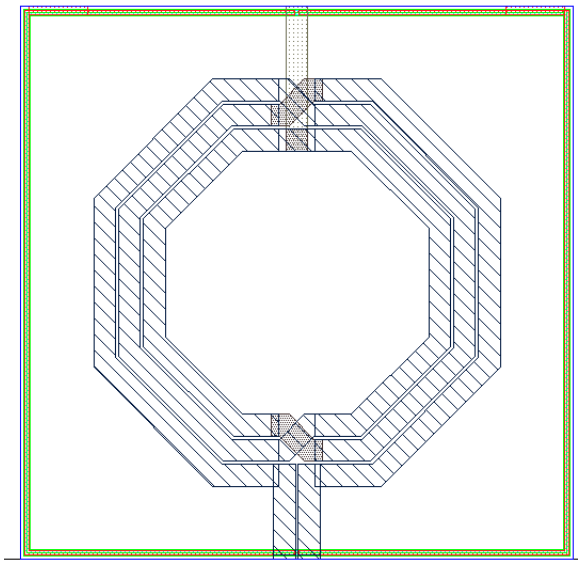


Fig. 106. Layout of inductor in CSD-QVCO

b. Varactor

Accumulation-mode MOS is used as varactor due to its superior quality factor, wide tuning range, and monotonic dependence on control voltage [38]. Shown in Fig. 108, this non-standard MOS is realized in the n-well, source and drain are n+ instead of p+. When used as varactor, the source, drain and bulk are connected as one terminal while the gate is another one. Fig. 109 presents simulated results for the capacitance and quality factor as a function of V_{GS}. C_{max}/C_{min} is 2.7 in two oscillators and the worst case quality factors are 55 and 38 for the 5-GHz CSD-QVCO and the 4.2-GHz CSD-QVCO, respectively, both much larger than the inductors. The worst case parallel conductances in two cases are 0.085 mS and 0.4 mS, respectively.

c. Oscillator

The two CSD-QVCOs are both implemented in the TSMC 0.18 μm CMOS technology. The 5-GHz CSD-QVCO is a stand-alone circuit while the 4.2-GHz CSD-QVCO

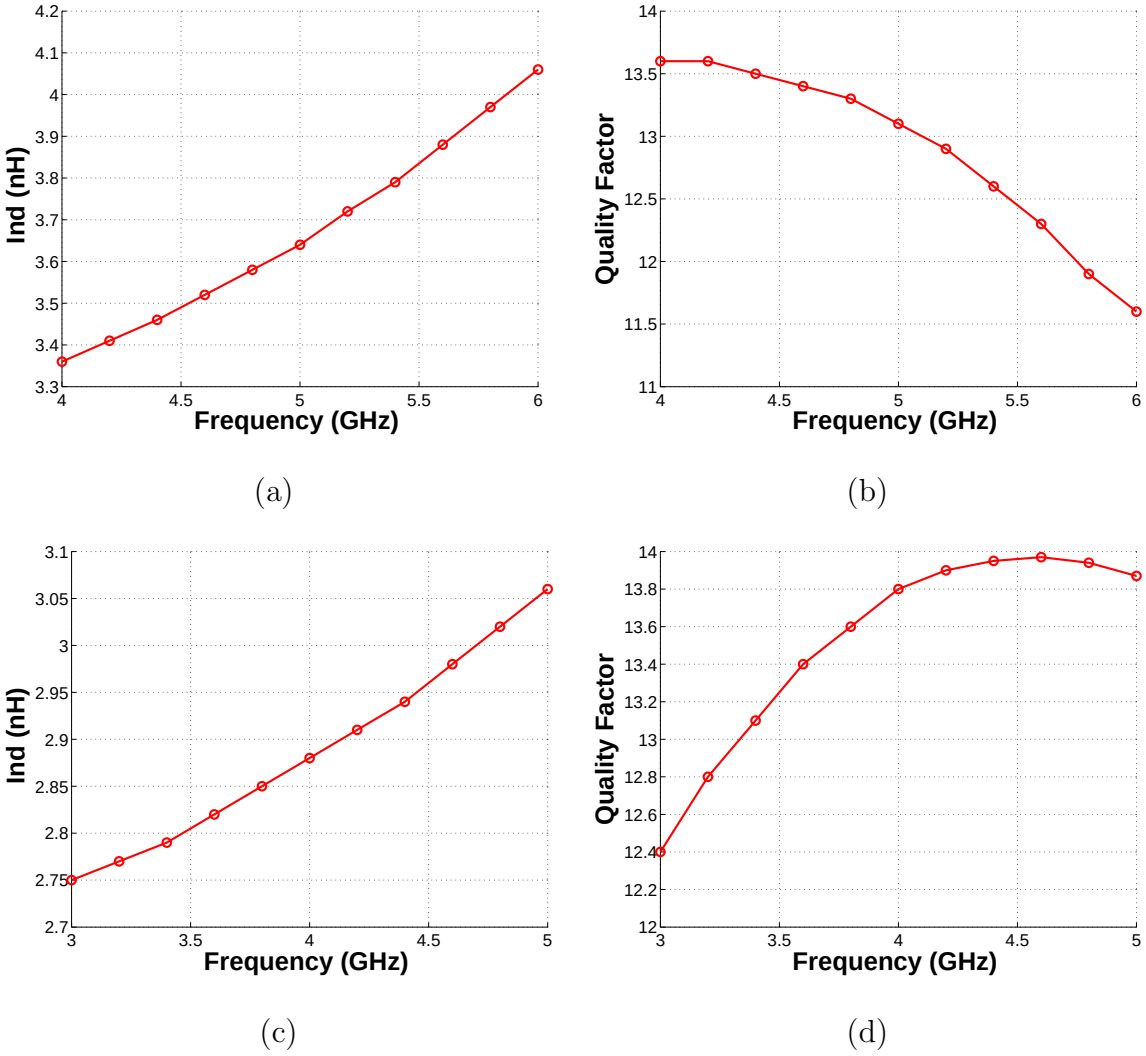
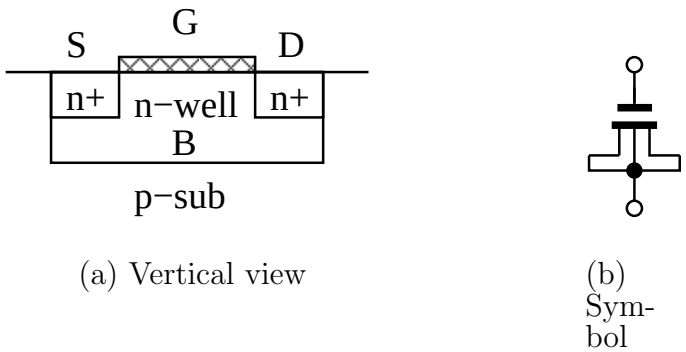


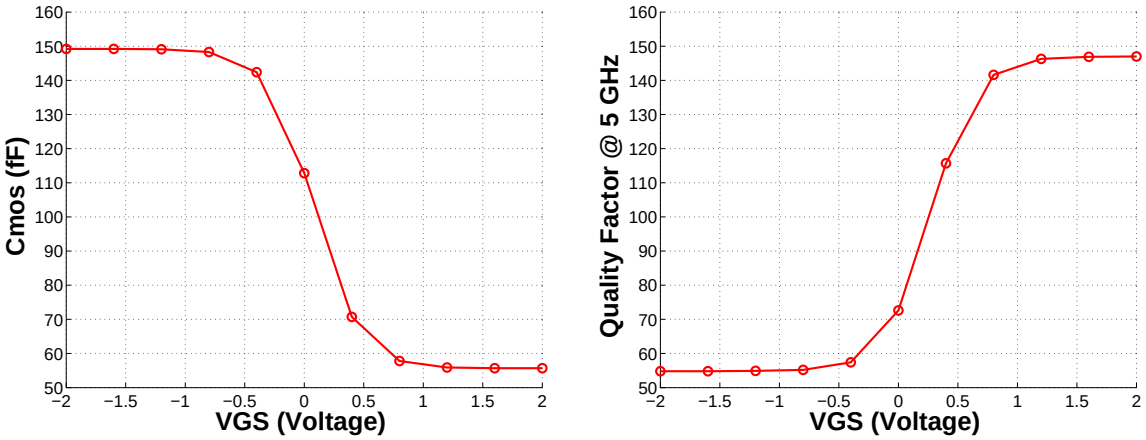
Fig. 107. Simulation results of implemented inductors



(a) Vertical view

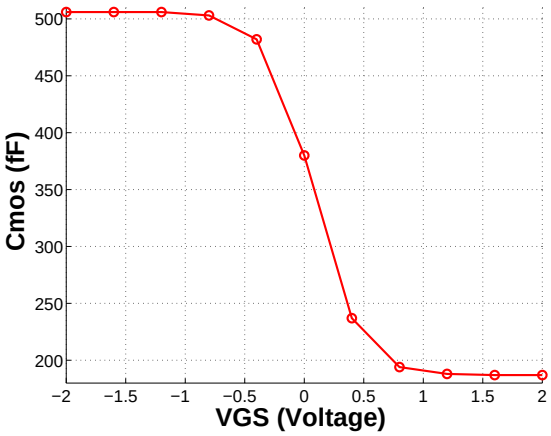
(b) Symbol

Fig. 108. Accumulation-mode MOS as varactor

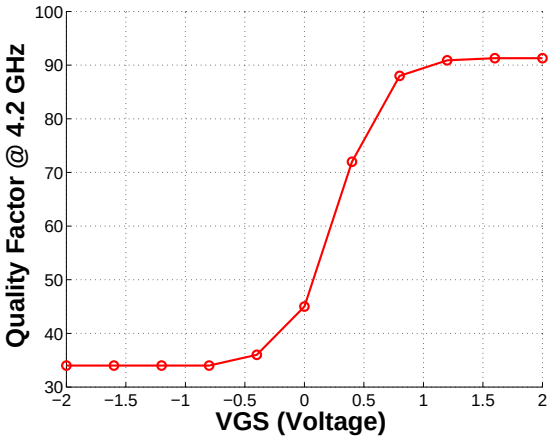


(a)

(b)



(c)



(d)

Fig. 109. Simulation results of implemented varactors

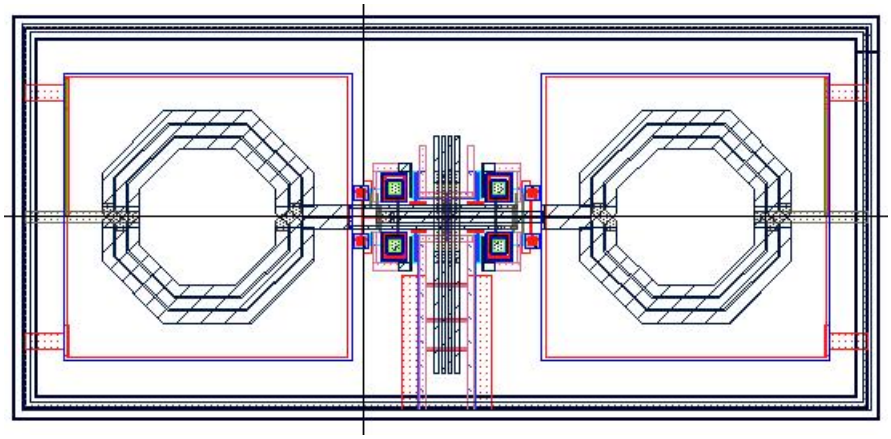


Fig. 110. CSD-QVCO layout

is integrated in the UWB frequency synthesizer. With the purpose of pushing the oscillation frequency to the higher limit and achieving best phase noise performance, the 5-GHz CSD-QVCO uses smaller varactor and larger inductor. Small varactor helps to increase the oscillation frequency. Large inductor increases signal amplitude to obtain smaller phase noise. The consequence of this approach is the decrease of the tuning range, which can be compensated by using capacitor bank with the disadvantage of complicated tuning algorithm [39]. To guarantee the desired oscillation frequency of 4224 MHz fall into the tuning range of the 4.2-GHz CSD-QVCO, the inductance is lowered while the varactor is increased by four times. In both CSD-QVCOs, the transistor gate length for the differential pairs is not minimal, which helps to decrease the phase error due to mismatch. Same layout floor plan is adopted in each CSD-QVCO, as shown in Fig.110. Symmetry is kept both vertically and horizontally for the matching purpose. The two inductors are intentionally located far away from each other to reduce the phase error due to their mutual inductance [40]. The interconnections between the oscillator core and the inductors use the top thick metal layer to minimize the adverse effect on the tank quality factor. Fig. 111 presents the simulated 5-GHz CSD-QVCO startup. The tuning curves of the two oscillators are

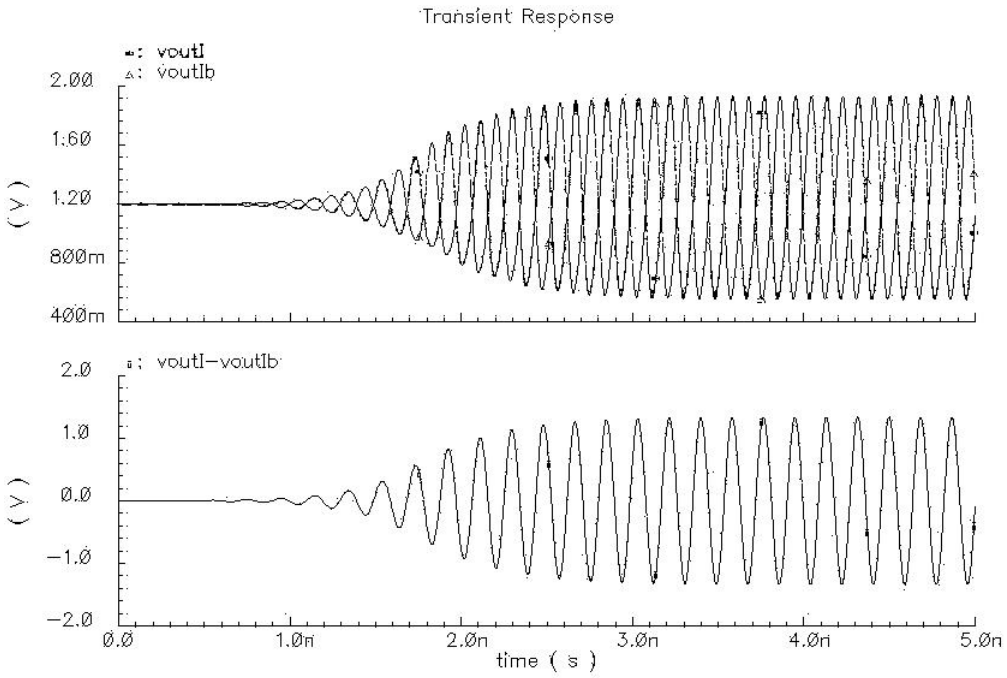


Fig. 111. QVCO startup simulation results

shown in Fig. 112.

Table V summarizes the sizes and values for the various components used in the two CSD-QVCOs.

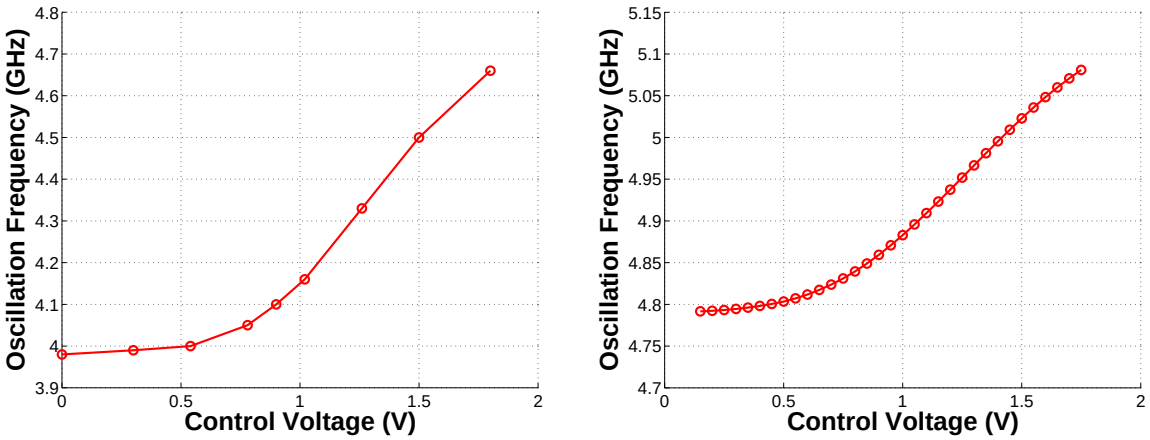
Table VI summarizes the simulation results of the two CSD-QVCOs.

Table V. Sizes and values of the components in the two CSD-QVCOs, as shown in Fig. 104

	5-GHz CSD-QVCO	4.2-GHz CSD-QVCO
M_{diff}	100 μm/0.24 μm	100 μm/0.24 μm
M_{bias}	100 μm/1.2 μm	100 μm/1.2 μm
M_{var}	30 μm/0.5 μm	100 μm/0.5 μm
R_{bias}	85 Ω	85 Ω
C_s	110 fF	110 fF
Inductor	2.9 nH	2.5 nH

Table VI. Simulation results of the two CSD-QVCOs

	5-GHz CSD-QVCO	4.2-GHz CSD-QVCO
Center Frequency (GHz)	4.3 GHz	4.9 GHz
Tuning Range (GHz)	690 MHz	290 MHz
Power Supply (V)	1.2 V	1.2 V
Current Consumption (mA)	4.7 mA	5.3 mA
Phase Noise (dBc)	-123	-128



(a) 4 GHz CSD-QVCO (b) 5 GHz CSD-QVCO

Fig. 112. Simulated tuning curve of the two CSD-QVCOs

CHAPTER VIII

EXPERIMENTAL RESULTS

A. Experiment Results of Frequency Synthesizer

The frequency synthesizer was integrated in a UWB receiver chip and fabricated in a TSMC 0.18 μm CMOS technology with top thick metal layer. Due to the limitation of available pins, only mixer outputs, the oscillator control lines and power lines are connected to the external pins.

The chip was mounted on a standard FR4 PC board. The measurement was performed by powering up the circuit and measuring the mixer outputs. The signal we found the mixer output are off from what we expected. Further investigation leaded us to conclude that the root cause is the ESD damage on the gate oxide of differential pairs inside the CSD-QVCO. There are several evidence support our conclusion.

- There is no ESD protection circuit at the pad connected to the power supply of the CSD-QVCO.
- The power supply of the CSD-QVCO is connected to gates of differential pairs through inductors, which can be regarded as DC short.
- The measured resistance between the power supply pad to ground is only 2k Ohm, several orders less than simulated results. This measurement was performed when the whole chip was completely off, excluding the possibilities of turning on any active devices in the chip. Careful examination of the layout and schematic does not reveal any such low impedance path.
- [41] shows that a signature of oxide breakdown due to ESD is the existence of

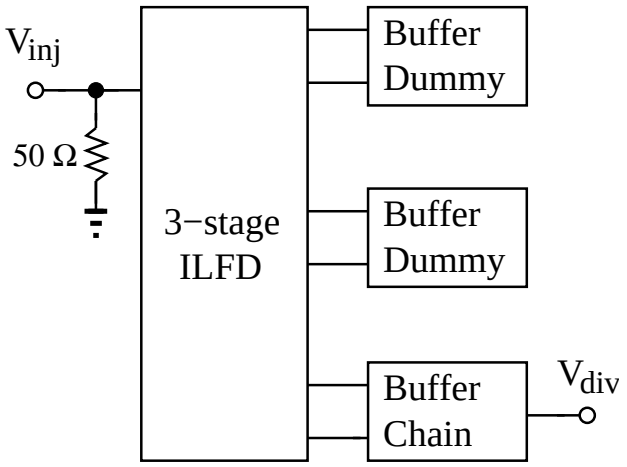


Fig. 113. Block diagram of the implemented ILFD

large leakage current from gate to substrate. This explains why the above low impedance is measured.

As a result of this ESD damage, the mixer would not be fed with expected signals from the CSD-QVCO. On the other hand, as will be shown later, the experiment results of the stand-alone CSD-QVCO with ESD protection closely match the simulation results.

B. Experiment Results of Injection-locking Frequency Divider

To verify circuit performance, a three-stage injection-locked frequency divider was implemented in a standard $0.18\mu m$ CMOS technology. Fig. 113 shows the block diagram of the implemented ILFD with buffers. A 50 Ω resistor is put at the input to terminate the source impedance. A differential three-stage buffer chain is connected from one of the three stages to contact pads for testing purpose. In the last stage of the buffer chain, two 50 Ω resistors are used to load each branch of the differential pair. As our test equipment only has single-ended input, one output of the last buffer stage is connected to the contact pad, while the other one is left unconnected. To

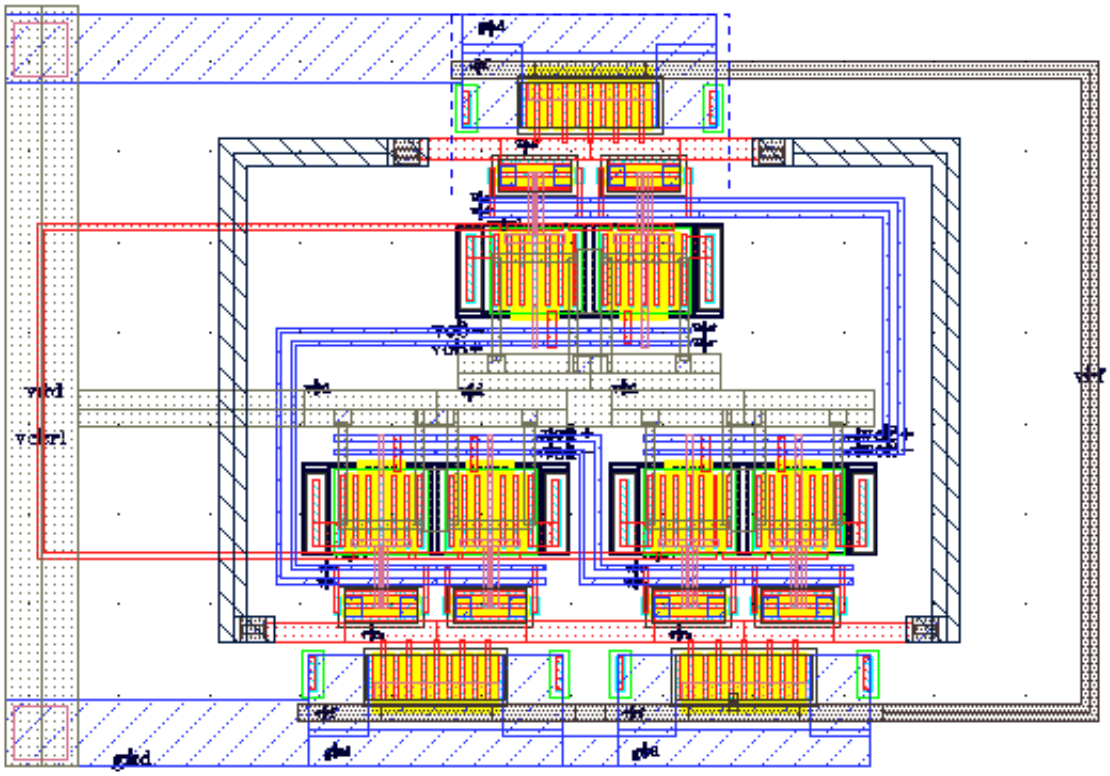


Fig. 114. Layout of the three-stage ILFD

balance the load for all the stages, dummy buffers identical to the first buffer in the buffer chain are also connected to the other two stages. The layout of the three stage ILFD is shown in Fig. 114.

Fig. 115 shows the micro photograph of the frequency divider with output buffers. The total chip area is 940×470 μm^2 including the contact pads. The core of the frequency divider and the buffer chain occupy 77×66 μm^2 and 88×71 μm^2.

The measurement was performed on a standard FR4 PC board. Fig. 116 shows the photograph of the board. Two SMA connectors were mounted for input and output signals respectively. A voltage regulator was used to provide clean supply voltage.

Fig.116 shows the test bench. The injection signal is generated from a HP 8673C

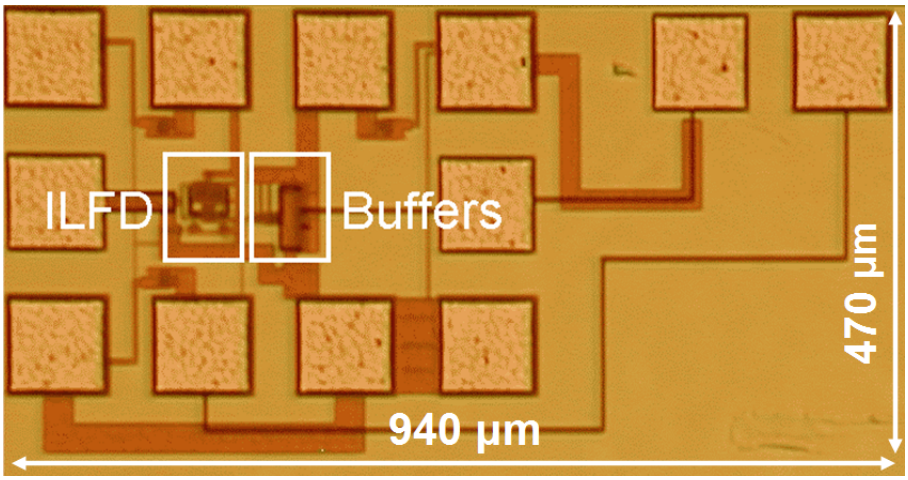


Fig. 115. ILFD chip micro photograph

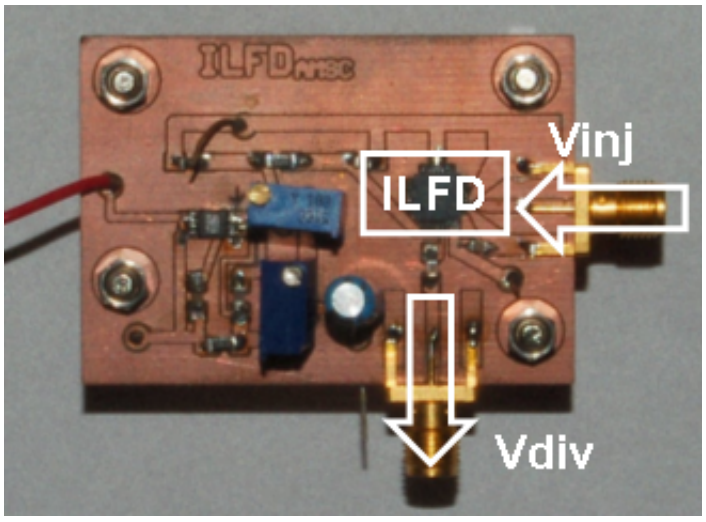


Fig. 116. ILFD test board

synthesized signal generator. The output signal is measured through a R&S FSEB 30 spectrum analyzer. Both the injection signal and the DC bias voltage are applied to the gate of the tail current source transistor through a bias tee. Another bias tee is inserted between the output and the spectrum analyzer to block the DC component of the output from going to the spectrum analyzer. Because of the limited bandwidth of the bias tee (4.2 GHz), the injection signal is attenuated to some extent when its frequency is above the bias tee bandwidth. For instance, the measured attenuation at 6 GHz is 2.2 dB. The attenuation measurement, however, are limited by the upper range of our spectrum analyzer (7 GHz). Fig. 117 shows the phase noise of the locked output signal with the division ratio of 12 when the injection frequency is 7.2 GHz. As a reference, the phase noises of the signal generator at 7 GHz (the highest frequency that could be measured by the spectrum analyzer) are -95 dBc/Hz and -120 dBc/Hz, at 10 kHz and 500 kHz offset respectively. We could not obtain the phase noise plot for the free running ILFD, because without the input signal, the center frequency is not stable. Any voltage variation present at the bias input changes the bias current. As indicated in (6.4) and (6.5), the free running oscillation frequency is fluctuated accordingly. It is, however, another way to show that the ILFD was locked to the external signal.

The measured average free running oscillation frequency is 562 MHz, which is 20% below the simulated value. This result shows that the parasitic capacitance was under-estimated. The measured input sensitivity of the ILFD is shown in Fig. 118. It shows that higher input power is needed for higher division ratio. There are two reasons. Firstly, the frequency dependent attenuation of the bias tee is not accounted for. Secondly, the parasitic capacitance at the common source node further attenuates the injection signal, especially at high frequencies. The highest division ratio is able to reach 24. But the unaccounted bias tee loss prevents us from collecting realistic

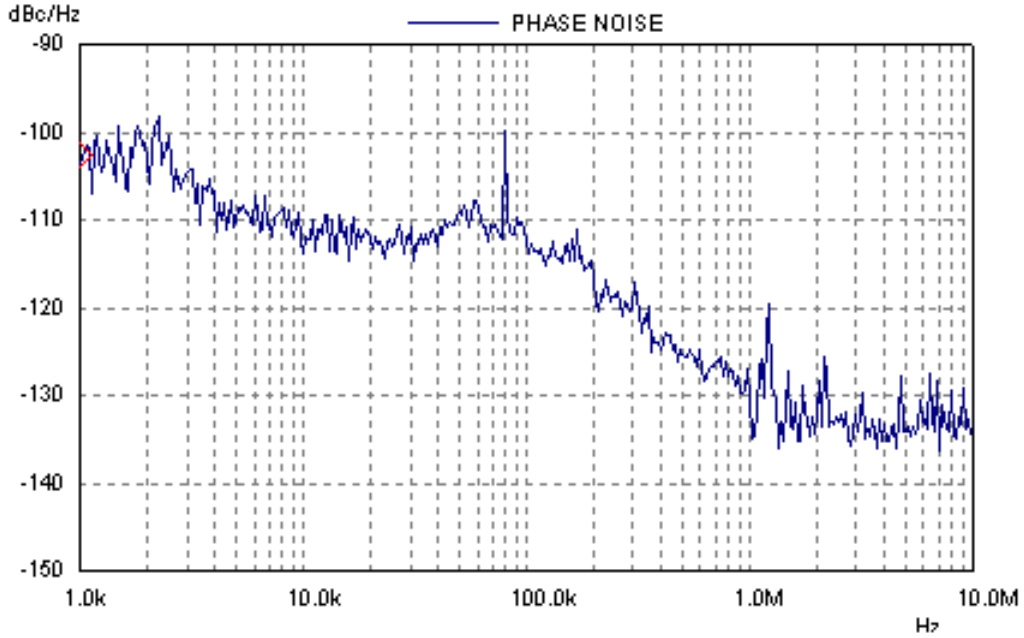


Fig. 117. Measured output phase noise of the ILFD for the division ratio of 12 with injection frequency of 7.2 GHz

input power data. Other than this, the maximum injection frequency is 11.2 GHz with the division ratio of 18. As the measured power consumption is 7.2 mW, using definition of the figure of merit (FoM) from [23], which is the maximum injection frequency per unit power consumption, the FoM of this ILFD is 1.5 GHz/mW. This figure is not rated excellent among the ones from the frequency dividers listed in [23]. However, the larger division ratio achieved in this ILFD helps to reduce considerable power consumed by its following circuits that could operate at lower speed.

Fig. 118 shows that for the division ratios of 6, 12, and 18, the locking ranges are 2.1 GHz, 1.9 GHz, and 1.7 GHz, respectively. To compare the measured locking range results with the numeric calculation results and the published ones, we normalized all locking range data to their center frequencies. Fig. 119 shows the normalized locking range of this work and other published data against division ratio [18–23]. The proposed architecture achieves the best normalized locking range so far. Of all

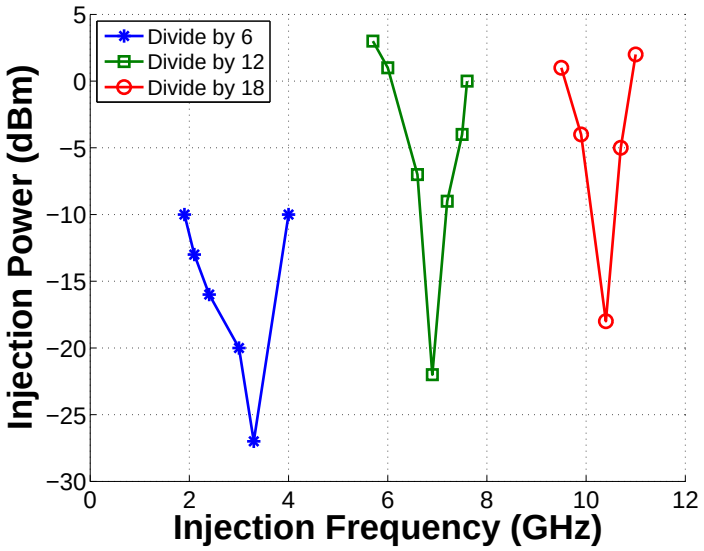


Fig. 118. Measured input sensitivity

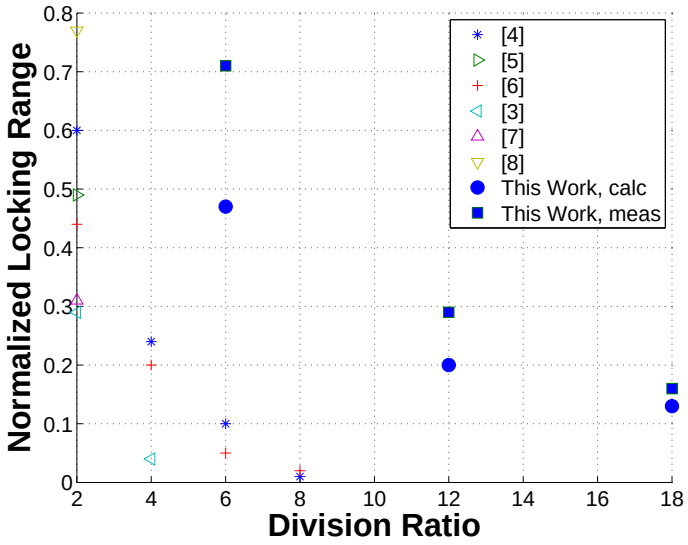


Fig. 119. Comparison of normalized locking range versus division ratio

Table VII. Performance summary of the measured injection-locked frequency divider

Technology	0.18 μm CMOS
Supply Voltage	1.8 V
Power Dissipation	7.2 mW
Active Area	0.17×0.14 mm^2
Divide-by-6 Locking Range	$1.9 - 4.0$ GHz
Divide-by-12 Locking Range	$5.7 - 7.6$ GHz
Divide-by-18 Locking Range	$9.5 - 11.2$ GHz

the previously published results, only one with division ratio of 2 [23] has larger normalized locking range than the proposed topology with division ratio of 6. However, that solution only outputs pseudo differential signals. Division ratios larger than 8 with acceptable locking ranges are not reported in any of the previous publications. The graph shows a general downward trend, with the normalized locking range decreasing as the division ratio increases. Compared with the measurement results, the theoretical results show large discrepancies at the lowest division ratio. This is because we assume weak injection in our model, while in the measurement we applied relatively large injection signal power. The discrepancy becomes less as the division ratio goes higher. Again, this is because the attenuation of the bias tee and the underestimated parasitic capacitance reduce the measured locking range. The performance of the measured injection-locked frequency divider is summarized in Table VII.

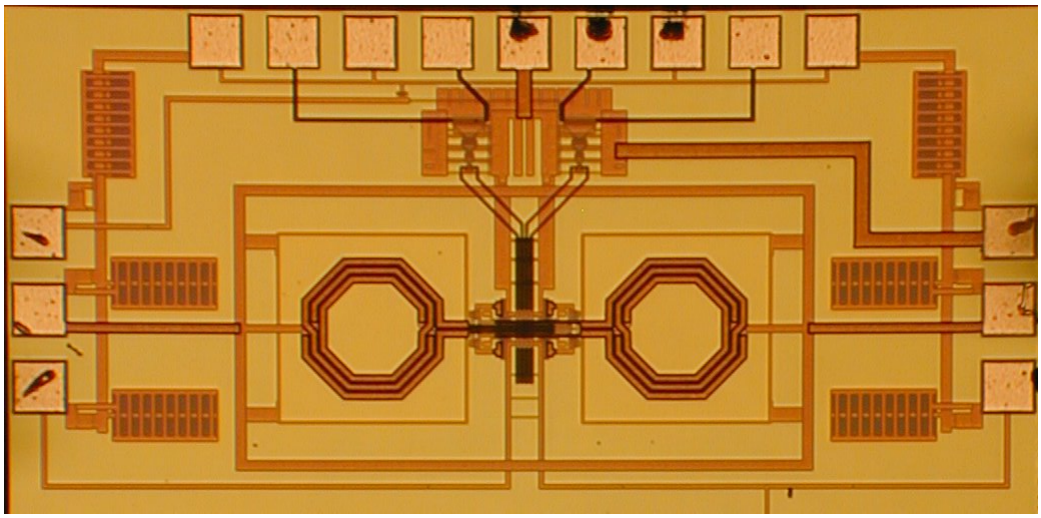


Fig. 120. 5-GHz CSD-QVCO chip microphoto

C. Experiment Results of CSD-QVCO

The two CSD-QVCOs have been separately fabricated in a TSMC 0.18 μm CMOS process with top thick metal layer. The 4.2-GHz CSD-QVCO are ESD (Electro Static Discharge) damaged.

Fig. 120 shows the micro photograph of the 5-GHz CSD-QVCO with buffers. The total chip area is 930×2000 μm^2 including the contact pads. The oscillator occupies 550×1100 μm^2. The measurement was performed on a standard FR4 PC board. Fig. 121 shows the photograph of the board. One of the four CSD-QVCO outputs is picked up by a SMA connector, with other outputs each terminated with a 50 Ω resistor. A voltage regulator was mounted to provide clean supply voltage.

The output signal was measured through a R&S FSEB 30 spectrum analyzer. Fig. 122 shows the plots of the oscillation frequency versus varactor control voltage from both measurement and simulation results. For a certain control voltage, measured oscillation frequency is a little less than the simulated one, suggesting under-estimation of parasitic capacitance. A plot of the phase noise at a oscilla-

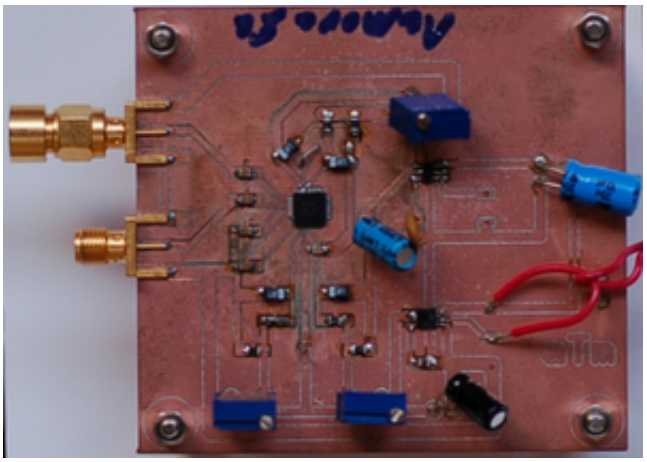


Fig. 121. 5-GHz CSD-QVCO test board

Table VIII. CSD-QVCO performance comparison with prior works

	Technology [μm]	Frequency [GHz]	Power [mW]	Phase Noise [dBc/Hz]	FoM [dBc]
[**5**]	CMOS 0.13	10	14.4	-95@1 MHz	163
[**3**]	BiCMOS $f_T = 30$ GHz	4.9	21.2	-113@2 MHz	168
[**4**]	CMOS 0.13	5.5	14.4	-112@1 MHz	175
This Work	CMOS 0.18	5	6.4	-120@3 MHz	176

tion frequency of 5 GHz is shown in Fig. 123. The CSD-QVCO is powered by a 1.2 V supply and consumes 5.2 mA current. To compare the CSD-QVCO performance with other publication results, a generally used FoM expression is used

$$\text{FoM} = 20\log(f_{osc}/\Delta f) - 10\log(\pounds(\Delta f)) - 10\log(P\ mW) \tag{8.1}$$

Table VIII compares the CSD-QVCO performance with prior works using various phase shifting techniques. The CSD-QVCO achieves the best FoM with the least power consumption.

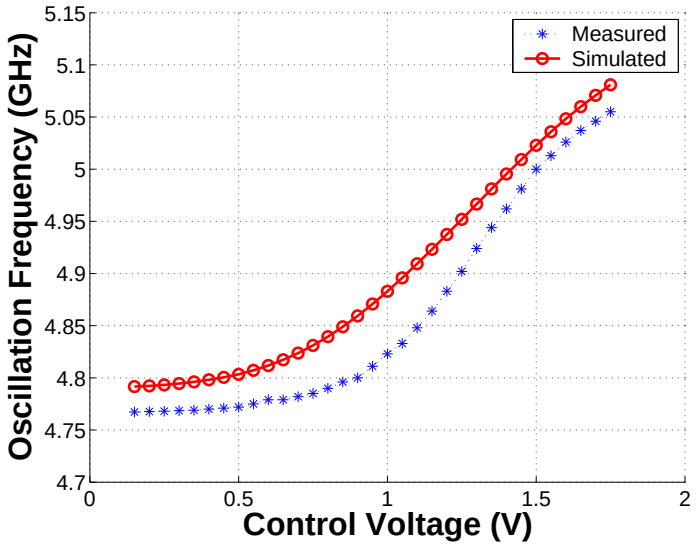


Fig. 122. Comparison of measured tuning curve with simulated one

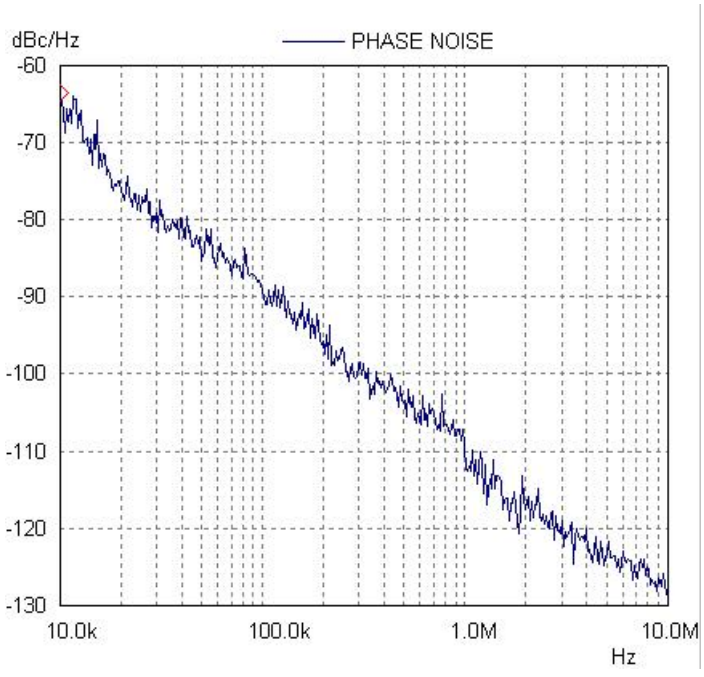


Fig. 123. Measured 5-GHz CSD-QVCO phase noise at 5 GHz

CHAPTER IX

CONCLUSIONS

In this dissertation, the design challenges of a frequency synthesizer for UWB systems are examined. The existing design approaches are reviewed and their weaknesses are identified. A harmonic-cancelation-mixer based frequency synthesizer architecture is proposed to achieve agile frequency hopping and minimize undesired sidebands.

The harmonic-cancelation mixer demands half-quadrature signals from frequency dividers. A robust half-quadrature signal generation scheme is introduced. Also, as frequency divider is the speed bottleneck of a frequency synthesizer, a power-efficient high-frequency ILFD architecture is proposed. By utilizing multi-stage with highly nonlinear operation, the divider provides multi division ratios and large locking ranges.

A novel CSD-QVCO is presented to overcome the problem of bi-modal oscillation existed in conventional QVCOs. The operation of CSD-QVCO is analyzed in details.

All the circuits have been verified by simulations to achieve satisfactory performance. The tests of the ILFD and CSD-QVCO show consistent results as simulation ones. The ILFD is implemented with three stages. It achieves multiple large division ratios as 6, 12, and 18 with locking range greater than 1.7 GHz, for a power consumption of 7.2 mW from a 1.8 V power supply. Compared with other published ILFDs, it achieves the largest division ratio with satisfactory locking range. The 5-GHz CSD-QVCO draws 5.2 mA current from a 1.2 V power supply. Its phase noise is -120 dBc at 3 MHz offset. Compared with existing phase shift LC QVCOs, the proposed CSD-QVCO presents better phase noise and power efficiency.

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VITA

Haitao Tong was born in Nanjing, People's Republic of China in 1976. He received his Bachelor and Master degrees in electrical engineering from Southeast University, China, in 1998 and 2001, respectively. In 2001, he joined the Analog & Mixed-signal Center, Department of Electrical Engineering, Texas A&M University to pursue his Ph.D. degree. From January 2006 to November 2006, he was an Engineering Intern with Broadcom Corporation, CA, where he worked on high-speed serial data link transceivers. He can be reached through the Department of Electrical and Computer Engineering, Texas A&M University, College Station, Texas 77843-3128.