ANALOG INTEGRATED CIRCUIT DESIGN TECHNIQUES FOR HIGH-SPEED SIGNAL PROCESSING IN COMMUNICATIONS SYSTEMS

A Dissertation

by

DAVID HERNANDEZ GARDUNO

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2006

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Edgar Sanchez-Sinencio
	Kai Chang
	Alexander Parlos
Head of Department,	Costas Georghiades

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ABSTRACT

Analog Integrated Circuit Design Techniques for
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David Hernandez Garduno, B.S., Universidad Iberoamericana
Chair of Advisory Committee: Dr. Jose Silva-Martinez

This work presents design techniques for the implementation of high-speed analog integrated circuits for wireless and wireline communications systems.

Limitations commonly found in high-speed switched-capacitor (SC) circuits used for intermediate frequency (IF) filters in wireless receivers are explored. A model to analyze the aliasing effects due to periodical non-uniform individual sampling, a technique used in high-Q high-speed SC filters, is presented along with practical expressions that estimate the power of the generated alias components. The results are verified through circuit simulation of a 10.7MHz bandpass SC filter in TSMC 0.35μm CMOS technology. Implications on the use of this technique on the design of IF filters are discussed.

To improve the speed at which SC networks can operate, a continuous-time common-mode feedback (CMFB) with reduced loading capacitance is proposed. This increases the achievable gain-bandwidth product (GBW) of fully-differential amplifiers. The performance of the CMFB is demonstrated in the implementation of a second-order 10.7MHz bandpass SC filter and compared with that of an identical filter using the conventional switched-capacitor CMFB (SC-CMFB). The filter using the continuous-time CMFB reduces the error due to finite GBW and slew rate to less than 1% for clock frequencies up to 72MHz while providing a dynamic range of 59dB and a PSRR$^-$ $>$ 22dB.

The design of high-speed transversal equalizers for wireline transceivers requires

the implementation of broadband delay lines. A delay line based on a third-order linear-phase filter is presented for the implementation of a fractionally-spaced 1Gb/s transversal equalizer. Two topologies for a broadband summing node which enable the placement of the parasitic poles at the output of the transversal equalizer beyond 650MHz are presented. Using these cells, a 5-tap 1Gb/s equalizer was implemented in TSMC 0.35μm CMOS technology. The results show a programmable frequency response able to compensate up to 25dB loss at 500MHz. The eye-pattern diagrams at 1Gb/s demonstrate the equalization of 15 meters and 23 meters of CAT5e twisted-pair cable, with a vertical eye-opening improvement from 0% (before the equalizer) to 58% (after the equalizer) in the second case. The equalizer consumes 96mW and an area of 630μm $\times$ 490μm.

To my sister, Leticia, my brother, Antonio, and my dear parents.

ACKNOWLEDGMENTS

Thanks to the National Council of Science and Technology of Mexico (CONACYT) for their financial support of my graduate studies.

Thanks to Texas Instruments, Xilinx and VLSIP for their support during the testing and packaging phases of the equalizer.

Thanks to my committee members. I would like to specially thank my advisor, Dr. Silva-Martinez, for his academic guidance during the course of my program, and for providing the required technical insight in my research. Also, I want to thank Dr. Sanchez-Sinencio for his advice, not only in the technical aspect, but also in life as a whole. Your comments always gave me a different perspective.

I want to express my gratitude to my friends and colleagues at the Analog and Mixed Signal Center. In particular, thanks to Alberto, Artur, Chinmaya, Adriana and Antonio, who were always there, encouraging me in the good and the bad times. Antonio, I will always be in debt to you, since you made my dream of pursuing a Ph.D. possible. Thanks also to Veronica, for her wise words of support when it most mattered. Couldn't have done it without you. Thank you Susana, for always believing in me.

Finally, thanks to my brother, Antonio, my sister, Leticia, and my parents, for their love and guidance. You have always been my inspiration in all my endeavors. I dedicate this work to you.

TABLE OF CONTENTS

CHAPTER Page

Page

LIST OF TABLES

LIST OF FIGURES

FIGURE Page

FIGURE Page

FIGURE Page

FIGURE Page

CHAPTER I

INTRODUCTION

Signal processing is at the core of communications systems. Radio-frequency (RF) front-ends for wireless receivers provide gain and filtering through the use of analog circuits [1, 2, 3, 4]. These operations must provide enough selectivity, low-noise and distortion for proper operation of the receiver while using low-power consumption. After an Analog-to-Digital Converter (ADC), further signal processing is done in the digital domain. For the case of wireline receivers, analog front-ends also provide gain and filtering [5, 6, 7], the latter being an equalizer, to properly detect the transmitted symbols even in the presence of noise and inter-symbol interference (ISI). For this signal processing, modern communications systems are increasingly using discrete-time systems.

Discrete-time systems, also referred to as sampled-data systems, sample continuous-time signals at a determined sampling rate, denoted by $f_s = 1/T_s$, where T_s is the sampling period. Given a continuous-time signal $x(t)$, the discretized or sampled signal, denoted as $x(n)$, is given by

$$x(n) = x(t)\Big|_{t=nT_s} \tag{1.1}$$

where n is an integer.

The advantages of discrete-time systems over their continuous-time counterpart depend on whether the implementation is (1) digital: generally using a digital signal processor (DSP) or a field-programmable gate array (FPGA), or (2) analog: traditionally using switched-capacitor or switched-current circuits. In general, discrete-

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time systems are less sensitive to noise, and more robust against supply and process variations than continuous-time systems. DSPs and FPGAs offer a high-degree of versatility and programmability, although their accuracy is usually limited by the quantization error due to the analog-to-digital converter (ADC) [8]. On the other hand, analog implementations can also be programmable, and do not suffer from quantization error, but suffer from the so-called kT/C noise [9, 10]. Nevertheless, for a number of applications they can provide a better trade-off between accuracy, power consumption and silicon area when compared to digital implementations.

There are two general types of discrete-time filters: Finite Impulse Response (FIR) and Infinite Impulse Response (IIR).

An FIR filter is described by the following difference equation [11]:

$$y(n) = \sum_{k=0}^{N-1} c_k x(n-k) \tag{1.2}$$

where c_k are the filter coefficients that determine the frequency response and $N-1$ is the order of the filter. Notice that in order to compute the current sample at the output, $y(n)$, we do not require the previous outputs $y(n-k)$. In other words, these are non-recursive filters.

By taking the Z-transform, we can obtain the filter's transfer function:

$$H(z) = \frac{Y(z)}{X(z)} = \sum_{k=0}^{N-1} c_k z^{-k} \tag{1.3}$$

Furthermore, the unit impulse response $h(n)$, which is the inverse Z-transform of $H(z)$, is given by

$$h(n) = \begin{cases} c_n, & 0 \leq n \leq N-1 \\ 0, & \text{otherwise} \end{cases} \tag{1.4}$$

FIR filters receive their name from the fact that their impulse response has a finite length, in this case equal to N.

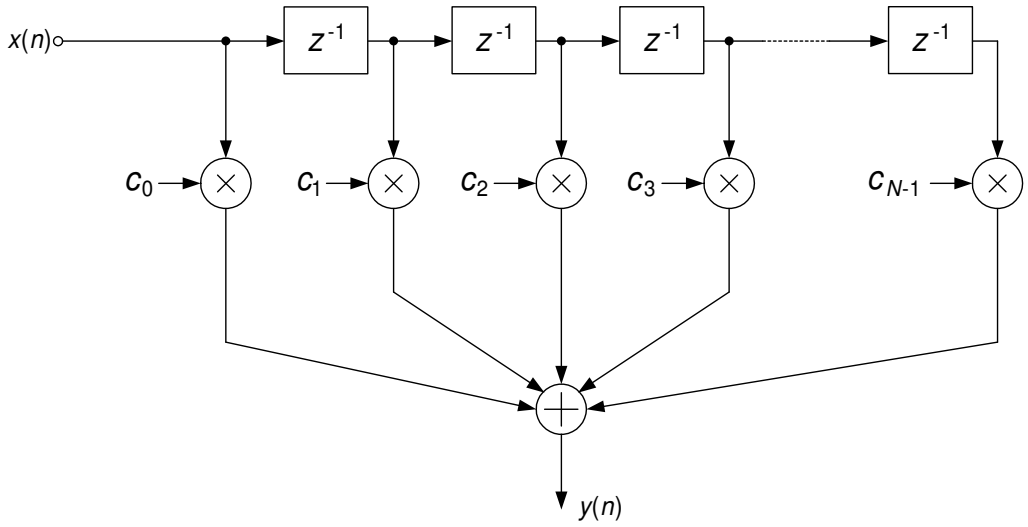


Fig. 1. Direct-form realization of an FIR filter.

The block diagram of a direct-form realization of an FIR filter is shown in figure 1[1].

An IIR filter on the other hand is described by the recursive difference equation

$$y(n) = \sum_{k=0}^{N-1} a_k y(n-k) + \sum_{k=0}^{M-1} b_k x(n-k), \tag{1.5}$$

with the filter's transfer function given by the ratio of two polynomials as follows:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{\sum_{k=0}^{M-1} b_k z^{-k}}{\sum_{k=0}^{N-1} a_k z^{-k}} \tag{1.6}$$

Coefficients a_k and b_k determine the location of the poles and zeros respectively.

One of the main advantages of IIR filters is that for the same frequency response specifications, they often require less number of coefficients than FIR filters.

[1]The reader is referred to [11] for other forms of realizations.

Nevertheless, because of the use of feedback, they are susceptible to stability issues. Furthermore, if linear phase is required across all frequencies, FIR filters will offer a better solution.

The first part of this work, namely chapters II-IV, studies the implementation of discrete-time systems using switched-capacitor (SC) circuits and their limitations at high-speed operation. Chapter II presents the foundations of switched-capacitor circuits and their fundamental limitations for high-speed operation. Chapter III deals with the effect of periodical non-uniform individual sampling used in high-speed, high quality-factor SC filters. Chapter IV proposes a new common-mode feedback circuit for high-speed SC filters, and its performance is demonstrated in the implementation of a 10.7MHz bandpass filter (typically used as intermediate-frequency filters in FM receivers).

As the required speed of operation increases beyond a few hundred MHz, SC circuit techniques can not be used due to their limited settling time characteristics. Nevertheless, high-speed wireline communications systems for data-rates of 1Gbps (1 giga-bit per second) and above require the use of equalizers to reduce the ISI. The second part of this work, namely chapters V-VII present analog circuit techniques to implement high-speed FIR filters. An introduction to equalizers is given in chapter V, while an overview of current high-speed implementations is provided in chapter VI. Chapter VII presents the design of a 1Gbps transversal equalizer using proposed continuous-time artificial delay lines.

Final conclusions and remarks are given in the last chapter.

CHAPTER II

SWITCHED-CAPACITOR CIRCUITS AND PRACTICAL LIMITATIONS IN HIGH-SPEED APPLICATIONS

This chapter provides a short introduction to the fundamentals of switched-capacitor circuits. Practical limitations such as speed and common-mode feedback design are discussed, since these set the foundation for the material presented in chapters III and IV. For other topics such as noise and offset compensation techniques, the reader is referred to [12, 13, 14].

A. Switched-Capacitor Filters: Basic Building Blocks

Discrete-time systems can be implemented using switched-capacitor (SC) circuits. A basic unity-gain sample-and-hold is shown in figure 2 [13], where two complementary clock phases ϕ_1 and ϕ_2 are used. During phase ϕ_1 (i.e. when switches controlled by ϕ_1 are closed), capacitor C_H is charged to $V_H = V_{in} - V_{off}$, where V_{off} is the input offset of the amplifier. During this phase, the output of the sample and hold is V_{off}. On phase ϕ_2, the capacitor is connected to the output, and the output voltage is given by $V_{out} = V_H + V_{off} = V_{in}$, transferring the sampled input with a delay of half a period. Therefore, $V_{out}(z) = z^{-1/2}V_{in}(z)$, or equivalently the transfer function is $H(z) = V_{out}(z)/V_{in}(z) = z^{-1/2}$.

For filter design, the basic first-order building blocks are the inverting and non-inverting lossless integrators shown in figure 3, and the lossy integrators shown in figure 4.

Assuming that the output is sampled on phase ϕ_1, and using charge re-distribution techniques [13], we can determine that the transfer functions of these first-order blocks are:

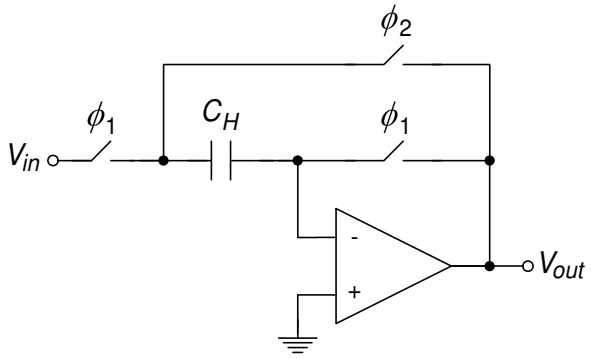


Fig. 2. Unity-gain sample-and-hold.

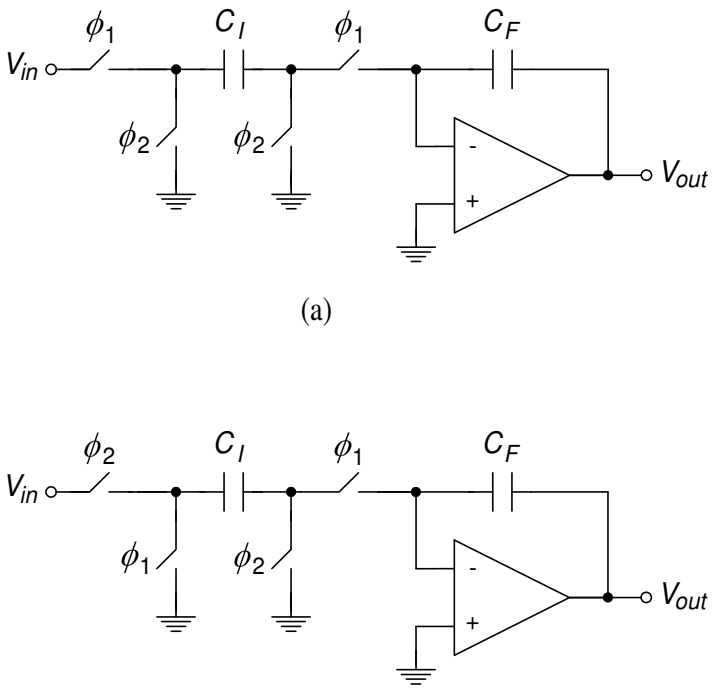
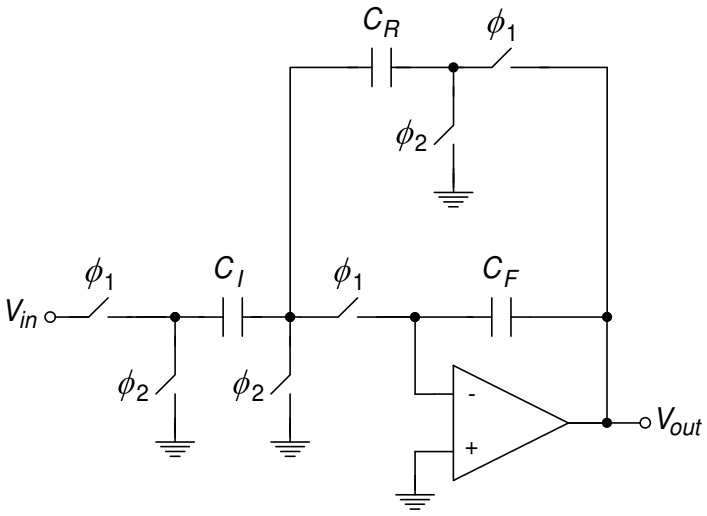
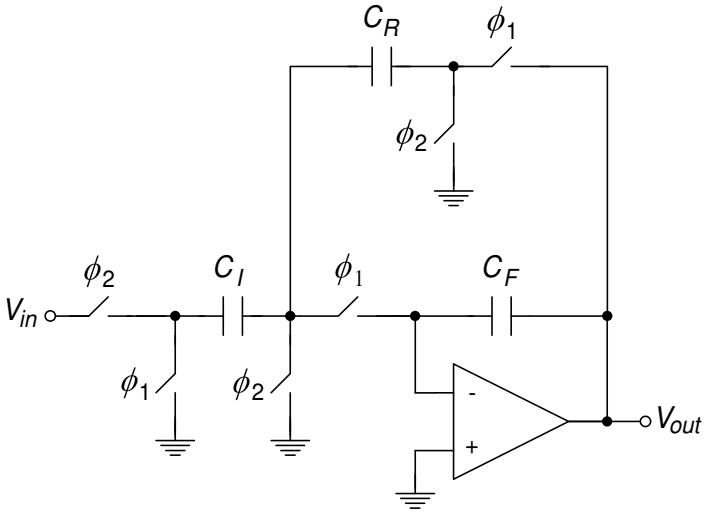


Fig. 3. Lossless integrators. (a) Inverting and (b) non-inverting.



(a)



(b)

Fig. 4. Lossy integrators. (a) Inverting and (b) non-inverting.

Lossless Inverting Integrator (output sampled at ϕ_1):

$$H(z) = -\left(\frac{C_I}{C_F}\right)\frac{1}{1-z^{-1}} \tag{2.1}$$

Lossless Non-Inverting Integrator (output sampled at ϕ_1):

$$H(z) = \left(\frac{C_I}{C_F}\right)\frac{z^{-1/2}}{1-z^{-1}} \tag{2.2}$$

Lossy Inverting Integrator (output sampled at ϕ_1):

$$H(z) = -\left(\frac{C_I}{C_F}\right)\frac{1}{\left(1+\frac{C_R}{C_F}\right)-z^{-1}} \tag{2.3}$$

Lossy Non-Inverting Integrator (output sampled at ϕ_1):

$$H(z) = \left(\frac{C_I}{C_F}\right)\frac{z^{-1/2}}{\left(1+\frac{C_R}{C_F}\right)-z^{-1}} \tag{2.4}$$

By using these basic building blocks, more complex filter structures can be designed, such as the biquadratic (second-order) filter shown in figure 5 [15]. Again, using charge re-distribution techniques, or by solving its equivalent block diagram shown in figure 6, it can be found that the transfer function is given by

$$H(z) = -\frac{(C_5+C_6)z^2 + (C_1C_2 - C_5 - 2C_6)z + C_6}{z^2 + (C_2C_3 + C_2C_4 - 2)z + (1 - C_2C_4)} \tag{2.5}$$

where $C_A = C_B = 1$ has been assumed.

B. Practical Limitations in High-Speed Switched-Capacitor Filters

1. Switches, Amplifier's Non-idealities, Capacitance Spread

As the frequency range and clock speed at which the switched-capacitor filter needs to operate increases, non-idealities such as the switch resistance, amplifier's finite gain-

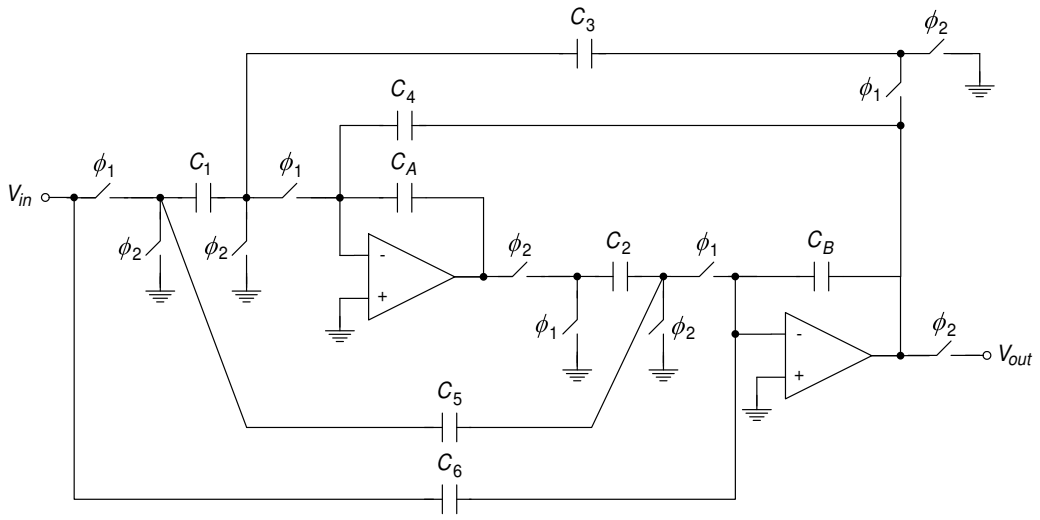


Fig. 5. Switched-capacitor biquadratic filter proposed by Martin.

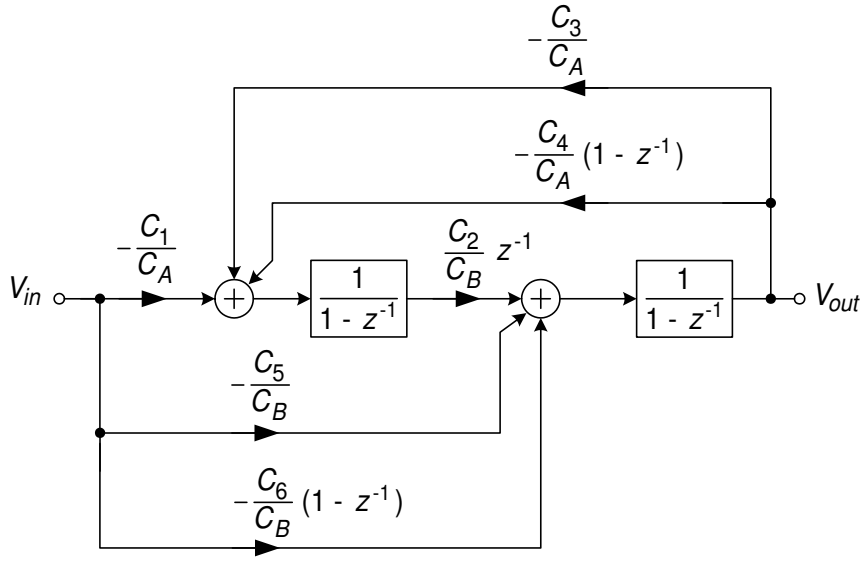


Fig. 6. Block diagram of the SC biquadratic filter proposed by Martin.

bandwidth product, slew rate, and load capacitance need to be further considered.

The non-zero resistance associated with MOS switches limits the speed at which capacitors can be charged and discharged. The charging/discharging time associated to this resistance is approximately

$$t_{sw} \approx 5R_{on}C \tag{2.6}$$

where C is the value of the capacitor being charged/discharged and R_{on} is the on-resistance of the switch. For example, for an MOS switch, R_{on} is given by

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)} \tag{2.7}$$

In this expression, μ_n and C_{ox} are process parameters which the designer generally can not accurately control, W and L are the transistor dimensions, and $V_{GS}-V_T$ is the overdrive voltage. Notice that increasing W/L improves the speed only to a certain point, after which the parasitic capacitance of the switch itself starts to increase t_{sw}. Also the designer can increase the overdrive voltage, but only up to a maximum V_{GS} specified by the technology. Therefore, the best alternative for high-speed switched-capacitor filters is to use minimum L and keep the values of all switching capacitors small.

The amplifier's gain-bandwidth product (GBW) also imposes a limitation on the speed at which SC circuits can operate. If the amplifier, which for SC applications is implemented as an output transconductance amplifier (OTA), is modeled as an integrator (i.e. has infinite DC gain and its dominant pole is at 0Hz), it can be demonstrated [16] that the amplifier's linear settling time is given by

$$t_{GBW} = \frac{5}{2\pi \cdot \beta \cdot GBW} \tag{2.8}$$

where GBW is the gain-bandwidth product in Hertz and β is the feedback factor, which is the attenuation from the output to the inverting terminal of the amplifier. In SC circuits, this can be expressed as

$$\beta = \frac{\sum C_f}{\sum_i C_i} \tag{2.9}$$

with $\sum C_f$ being the sum of all the feedback capacitors (connecting the output of the amplifier to its inverting terminal) and $\sum_i C_i$ being the sum of all capacitors connected to the inverting terminal (including those in the feedback).

Additional settling time is also required due to finite slew rate, which is the ability of the amplifier to source/sink current to/from the load capacitance during the amplifier's non-linear operation. For instance, in a single-stage OTA, the slew rate is given by $SR = dV/dt = I_{out,max}/C_L$, where $I_{out,max}$ is the maximum output current and C_L is the load capacitance at the output of the amplifier. Again, the settling time t_{SR} associated with the finite slew rate is limited by the load capacitance and the amplifier's current consumption.

For low-power, high-speed SC filters, it is necessary to design for a large slew rate and GBW without spending too much power. Given that $SR = I_{out,max}/C_L$ and $GBW = G_m/C_L$, where G_m is the effective transconductance of the OTA, we can improve both by increasing the power consumption or by keeping the load capacitance at a minimum. Increasing the power consumption is generally not desirable. Also, large bias currents might decrease significantly the OTA's DC gain, which degrades the accuracy of the filter. For example, it can be proved [16] that for the biquadratic filter in figure 5 operating as a bandpass filter, the actual center frequency f_c and

quality factor Q are given by

$$f_{c,\,actual} = \frac{A_0}{1+A_0} f_{c,\,ideal} \tag{2.10}$$

$$Q_{actual} \approx \left(1 - \frac{2Q_{ideal}}{A_0}\right) Q_{ideal} \tag{2.11}$$

where A_0 is the OTA's DC gain, and the quality factor is defined as the ratio between the center frequency and the filter's bandwidth (i.e. $Q = f_c/BW$).

For high-speed SC applications, such as Intermediate Frequency (IF) filters, the biquadratic bandpass filter shown in figure 7 can be used [17, 18, 19]. The sampling frequency f_s and the capacitor ratios C_4/C_2, C_4/C_3 and C_1/C_3 determine the filter's center frequency, quality factor, and peak gain, respectively. Notice that this topology has a reduced number of capacitors with respect to the biquad previously shown in figure 5, and thus larger slew rate and GBW for each amplifier can be obtained without increasing the power consumption. Still, for high Q filters, the ratio $C_4/C_3 \approx Q$ can result in a large capacitance spread [18], which is the ratio between the largest and smallest capacitors. Since the minimum value for C_3 is determined by kT/C noise [9, 10] and matching considerations, this results in impractical large values of C_4 in terms of silicon area and load capacitance to the amplifiers. As an example, the 6^{th} order bandpass filter reported in [18] (center frequency=10.7MHz, bandwidth=400kHz, ripple=1dB, clock frequency=62.5MHz) requires a maximum capacitance spread of $C_4/C_3 = 32$, leading to a total capacitance of $782C_u$, where C_u is the unit capacitance (typically 200fF in CMOS 0.35μm technologies). To overcome this limitation, T-networks [20], charge recombination techniques [21] and periodical non-uniform individual sampling [22] have been used. While the first approach [20] increases the input referred noise and sensitivity to process variations and parasitic capacitors, the technique proposed in [21] uses the amplifiers operating during both

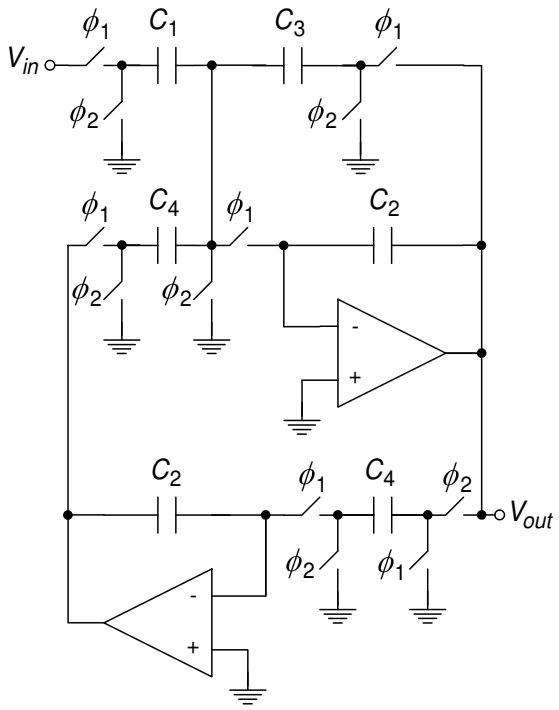


Fig. 7. Biquadratic section with reduced number of capacitors.

phases, requiring faster amplifiers and reducing the filter's flexibility. In chapter III, periodical non-uniform individual sampling is explained, and an analysis of its aliasing effects is presented.

2. Common-Mode Feedback and Its Loading Effects

Fully-differential (FD) amplifiers are widely used in switched-capacitor filters. They provide twice the signal swing when compared to single-ended implementations. Furthermore, they are less sensitive to common-mode signals such as substrate noise, and significantly reduce the effect of clock-feedthrough [13]. Nevertheless, FD amplifiers require a common-mode feedback circuit (CMFB) to stabilize their DC operating point and at the same time, provide rejection to common-mode signals.

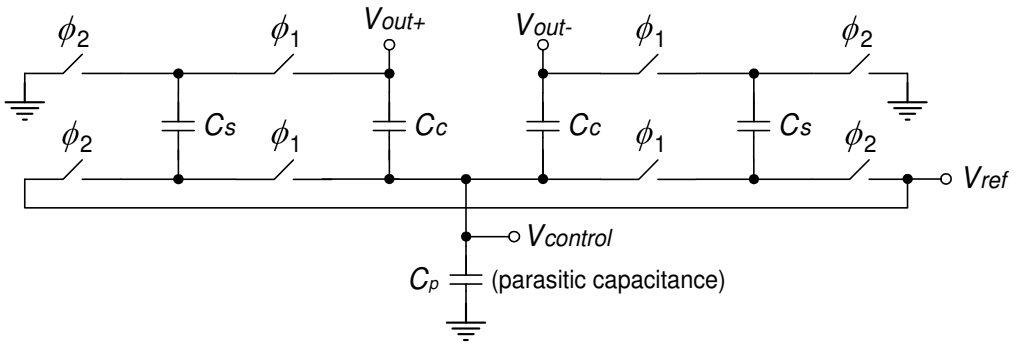
Several CMFB circuits have been proposed in the past [23, 24, 25, 26, 27, 28, 29, 30]. Typically continuous-time active implementations [25, 26, 27] are required for continuous-time applications, while for switched-capacitor applications, it has been preferred to use switched-capacitor-based CMFB circuits (SC-CMFB) [23, 24, 28, 29, 30] since they do not consume significant power and have better linearity when compared to their continuous-time counterparts.

A typical SC-CMFB circuit is shown in figure 8 [28, 29] along with a fully-differential folded-cascode amplifier. Capacitors C_c detect the common-mode output of the amplifier, which is then used to create the control voltage $V_{control}$ connected to transistors M_5, whose parasitic capacitance is denoted by C_p. V_{ref} is the reference common-mode voltage used by the CMFB.

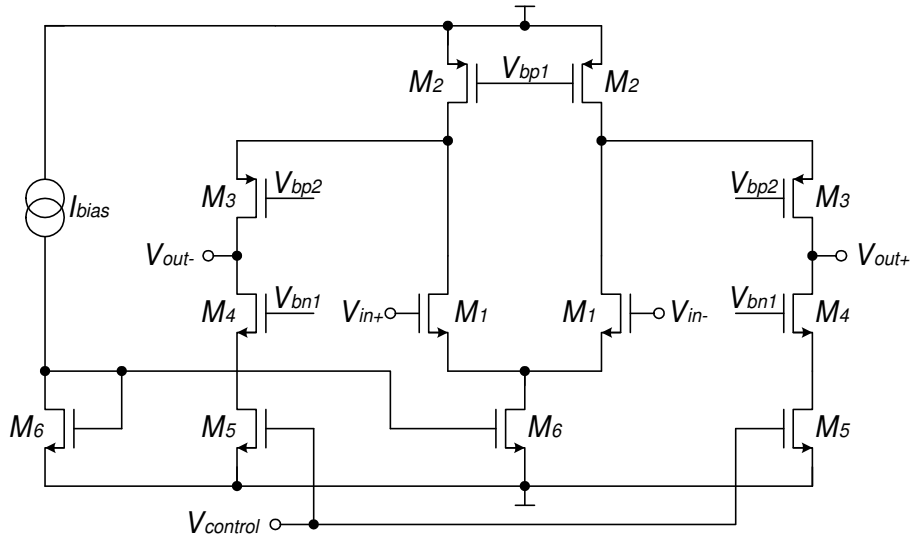
A continuous-time equivalent model of the SC-CMFB is shown in figure 9, where $R_s \approx 1/(f_{clock}C_s)$ and f_{clock} is the clock frequency. The control voltage $v_{control}$ (small-signal) is given by

$$v_{control} = \frac{v_{out+} + v_{out-}}{2} \frac{1/R_s + sC_c}{1/R_s + s(C_c + C_p/2)} \tag{2.12}$$

Observe that there is a pole at $\omega_p = 1/\left[R_s(C_c + C_p/2)\right]$ and a zero at $\omega_z = 1/\left[R_s C_c\right]$. The pole-zero mismatch leads to significant slow settling components if C_c is not at least 2 to 3 times larger than the parasitic capacitance C_p. Amplifiers for SC applications in CMOS 0.35μm can typically lead to parasitic capacitances due to M_5 of $\sim$ 400fF, resulting in $C_c \approx$ 1pF. C_s can be fixed to the minimum allowed by the technology. Therefore, the capacitive loading on the amplifier's output terminals due to the SC-CMFB can be over 1pF in these designs, drastically reducing its GBW and slew rate. To overcome this limitation, a continuous-time CMFB circuit for high-speed switched-capacitor networks is proposed in chapter IV.



(a)



(b)

Fig. 8. Switched-capacitor based common-mode feedback. (a) SC-CFMB (b) folded–cascode amplifier.

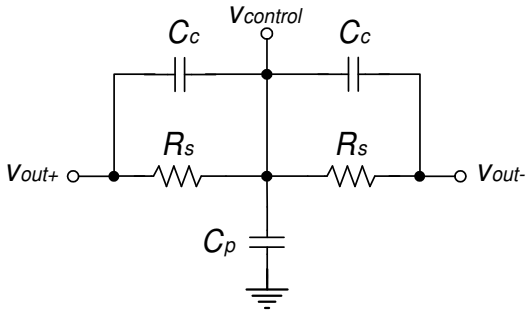


Fig. 9. Continuous-time equivalent circuit model for the SC-CFMB.

3. Common-Mode Rejection Ratio and Power Supply Rejection Ratio

The common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR) parameters are defined as

$$\text{CMRR} = \frac{v_{out,\,dm}/v_{in,\,dm}}{v_{out,\,cm}/v_{in,\,cm}} \tag{2.13}$$

$$\text{PSRR} = \frac{v_{out,\,dm}/v_{in,\,dm}}{v_{out,\,cm}/v_{supply}} \tag{2.14}$$

where dm and cm denote differential and common mode respectively, and v_{supply} is the small-signal present at the supply rail (supply noise). These two parameters are particularly important in switched-capacitor applications, since a significant amount of "switching" noise will be present in the substrate and in the power supply rails. It is therefore highly desired to have CMFB circuits with large CMRR and PSRR.

Let's analyze the PSRR^- of the SC-CMFB in figure 8. Since we are interested in the common-mode output, it is sufficient to analyze the half-circuit representation of the SC-CMFB shown in figure 10, which has been further simplified in figure 11 with its continuous-time equivalent circuit. Z_L is the load impedance, composed by the output resistance of the amplifier R_L in parallel with the load capacitance C_L due to

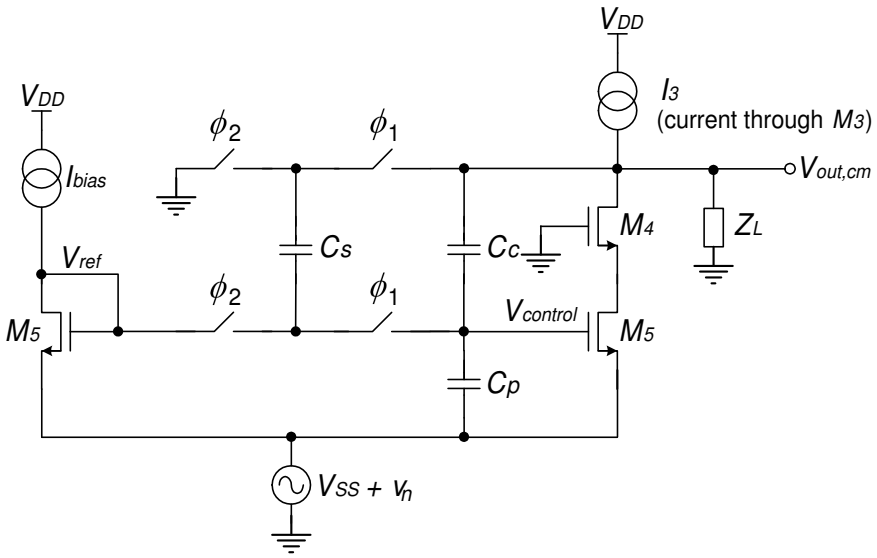


Fig. 10. Half-circuit for the PSRR$^-$ analysis of the SC-CFMB.

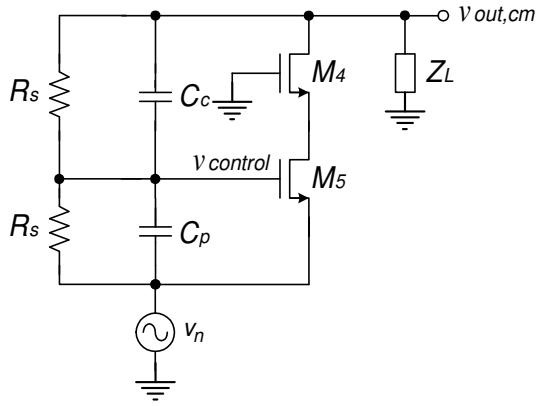


Fig. 11. Simplified continuous-time equivalent circuit of the SC-CMFB for PSRR$^-$ analysis.

the switching-capacitors comprising the filter's network; v_n denotes the noise voltage present in the negative power supply. By using circuit analysis, it can be found that

$$\frac{v_{out,\,cm}}{v_n} = \frac{g_{m,5}C_c s + g_{m,5}/R_s}{\left(C_p C_c + (C_p + C_c)C_L\right) s^2 + g_{m,5}C_c s + \left(g_{m,5} + 2/R_L\right)/R_s} \tag{2.15}$$

with the zero and poles located at:

$$\omega_z = \frac{1}{R_s C_c} \tag{2.16}$$

$$\omega_{p1} = \omega_z \left(1 + \frac{2}{g_{m,5}R_L}\right) \tag{2.17}$$

$$\omega_{p2} = \frac{g_{m,5}}{C_p + C_L + \dfrac{C_p\,C_L}{C_c}} \tag{2.18}$$

Since $g_{m,5}R_L \gg 2$, we have that $\omega_{p1} \approx \omega_z$, creating a medium-frequency pole-zero pair that has no significant impact on the frequency response of the PSRR$^-$. Meanwhile, ω_{p2} is a high-frequency pole (>100MHz). As a result, the PSRR$^-$ is approximately constant and close to 0dB typically up to $f_{clock}/2$. Verification of these results through circuit simulation is presented in chapter IV, where a comparison between the PSRR$^-$ of a switched-capacitor filter using the proposed CMFB and the PSRR$^-$ of the same filter using the SC-CMFB is shown. The proposed CMFB circuit significantly improves this parameter.

CHAPTER III

PERIODICAL NON-UNIFORM INDIVIDUAL SAMPLING: ALIASING EFFECTS

In chapter II, we mentioned the importance of reducing the capacitance spread in switched-capacitor filters to reduce the load capacitance driven by the amplifiers, and therefore obtain a faster settling-time with reduced power consumption. The Periodical Non-uniform Individual Sampling (PNIS) technique has been shown suitable for capacitance spread and total capacitor-area reduction in high Q filters. However, the use of periodical non-uniform clock signals results in additional alias components in the output spectrum. This chapter presents a model to analyze the generation of such alias components and gives expressions to estimate their power. The results are verified through circuit simulation of a 10.7MHz second-order SC bandpass filter in CMOS 0.35μm technology. Implications of the use of this technique in the design of Intermediate Frequency (IF) filters are then discussed.

A. Description of Periodical Non-Uniform Individual Sampling

Consider the biquadratic bandpass filter using PNIS shown in figure 12. According to this technique, any individual SC structure is active during m clock periods over a given number of N cycles ($1 \leq m \leq N$) of the master clock ϕ. Thus, the equivalent resistance of each SC branch in a circuit is individually controlled by programming the number of clock pulses m. For illustration, let us now consider that the operating clock phases of the switched-capacitor C_3 in figure 12 are generated from a periodical non-uniform clock signal θ (i.e. θ_1 and θ_2, $m = 1$ and $N = 2$ in figure 12). With such

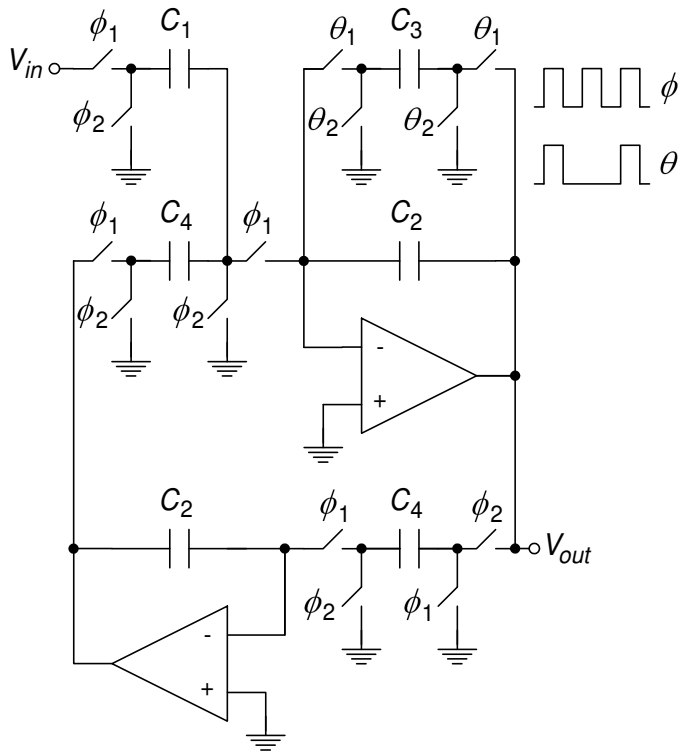


Fig. 12. Switched-capacitor biquadratic bandpass filter using PNIS.

a clock scheme, the equivalent filter's Q-factor is given by

$$Q \approx \frac{NC_4}{mC_3} \tag{3.1}$$

Therefore, for the implementation of a given Q-factor value, the required capacitance spread C_4/C_3 is now reduced to $(N/m)Q$. For high Q-factors, $m = 1$ and $N > 1$ is chosen to obtain the maximum Q with the smallest capacitance spread. By using PNIS with $m = 1$ and $N = 4$, the total capacitance in [18] was reduced from $782C_u$ down to $219C_u$.

Unfortunately, as a consequence of the larger repetition period of the slower clock signal θ, additional alias components appear at integer multiples of f_s/N that may limit the filter's performance. This issue is similar to the case of N-path narrow-band filters where the effective speed of the clock is reduced by $1/N$ [3, 31]. Section B in this chapter analyzes the generation of such alias components and derives expressions to estimate their power; a simple and intuitive alias model that can be used for more complex structures is presented.

B. Analysis and Estimation of Aliasing Effects

An equivalent representation of the lossy SC integrator section operating with PNIS is illustrated in figure 13. The master clock ϕ is used to generate the non-overlapping clock phases ϕ_1 and ϕ_2, whereas the operating clock phases of the switched-capacitor C_3 used in figure 13, θ_1 and θ_2 are modeled by means of an ideal multiplier and a square wave $P(t)$. Notice that the branch C_3 is now operating at the sampling frequency f_s, and the multiplier modulates the integrator's output with the signal $P(t)$, whose effective sampling frequency is equal to $f_s' = f_s/N$; for $m = 1$, f_s' has a duty cycle of $(100/N)\%$. This model is derived from the fact that the clock signal θ

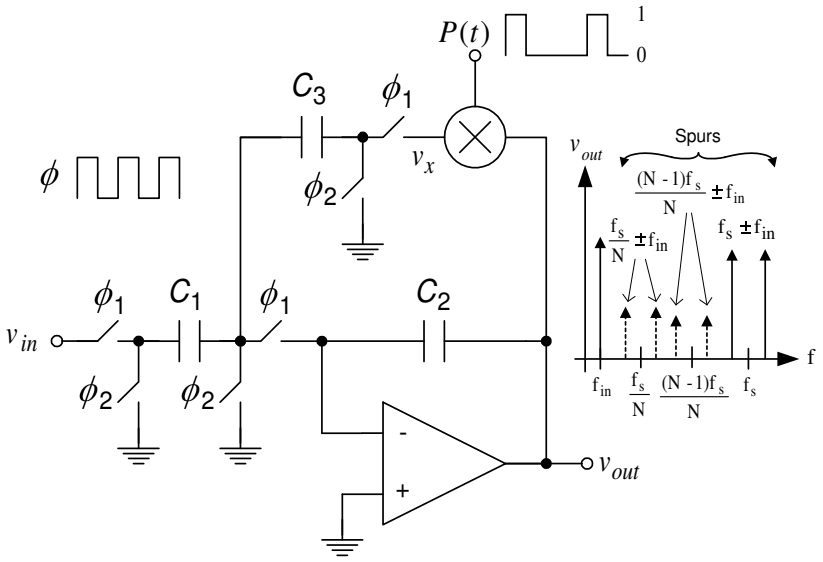


Fig. 13. Equivalent representation of a SC lossy-integrator operating with PNIS.

can be obtained by masking the master clock signal ϕ with the train of unity pulses $P(t)$.

Expressing the signal $P(t)$ in its Fourier series expansion we have[1]

$$P(t) = \frac{1}{N} + \frac{2}{\pi}\sin\left(\frac{\pi}{N}\right)\cos\left(2\pi\frac{f_s}{N}\,t\right) + \ldots \tag{3.2}$$

In eq. (3.2), the term $1/N$ represents a constant that leads to an attenuation of the integrator's output at node v_x, which is the desirable effect of the PNIS scheme to reduce the capacitance spread. The second term, a tone at the frequency of the slower clock running at f_s/N, is responsible for the generation of the most relevant spurious tones (i.e. alias components) in the lossy integrator. In this analysis, the

[1]The results can be generalized to the case where $m \neq 1$, and the secondary clock θ is active during m consecutive clock periods of the master clock ϕ and inactive during the remaining $N - m$ periods. In this case, the following Fourier series expansion should be considered $P(t) = \dfrac{m}{N} + \dfrac{2\sin(m\pi/N)}{\pi}\cos\left(\dfrac{2\pi f_s t}{N}\right) + \ldots$

effect of higher frequency terms is ignored, but it is evident that they will generate alias components as well.

Considering the first two terms in eq. (3.2), and assuming a continuous-time sinusoidal waveform $v_{in}(t) = Ae^{\pm j2\pi f_{in}t}$ at the input terminal of the SC integrator, it is expected that the integrator's output will have several tones generated by the sampling of the signal (considered ideal in this analysis) and the use of the slower clocks. In a first approximation, the output signal can be expressed as

$$\begin{aligned} v_{out} \cong\ & H_1 Ae^{\pm j2\pi f_{in}t} + H_1 kAe^{\pm j2\pi(f_s \pm f_{in})t} + \\ & + H_2 Ae^{\pm j2\pi(f_s/N \pm f_{in})t} + H_3 Ake^{\pm j2\pi(f_s(N-1)/N \pm f_{in})t} \end{aligned} \tag{3.3}$$

The first term in eq. (3.3) represents the output component at the original input frequency that leads to the ideal integrator's transfer function. Due to the sampled nature of SC circuits, alias components appear at the output at $f = f_s \pm f_{in}$, as depicted in figure 13 and represented by the second term in eq. (3.3). Although ideal sampling of a continuous-time signal would result in a spectrum with replicas at integer multiples of f_s with the same magnitude, in practice the sample-and-hold operation embedded in SC circuits, the finite conductance of the switches, and the speed of the amplifiers partially reduce the amplitude of these replicas. Therefore k is introduced in equation (3.3) and its value is always smaller than one. Assuming that $k = 1$ leads to an upper bound in the alias estimation. The third and fourth terms in (3.3) represent the alias components or spurious tones due to PNIS (dashed lines in the frequency spectrum shown in figure 13).

Analysis of the lossy SC integrator using charge re-distribution techniques leads to the following expressions for the integrator's transfer function (ratio of the funda-

mental tone at the output and the input tone), which corresponds to H_1 in (3.3)

$$H_1 = H(f) = \left[-\frac{C_1}{C_2 + \frac{C_3}{N}}\right] \cdot \left[\frac{1}{1 - \frac{C_2}{C_2 + C_3/N}\, e^{-j\left(\frac{2\pi f}{f_s}\right)}}\right] \tag{3.4}$$

To obtain the magnitude of the alias due to PNIS, notice that the transfer function from a signal applied at node v_x to v_{out} is an integrator given by

$$G(f) = v_{out}(f)/v_x(f) = (C_3/C_1)\, H(f) \tag{3.5}$$

On the other hand, the mixing of the second term of $P(t)$ in equation (3.2), $\frac{2}{\pi}\sin\left(\frac{\pi}{N}\right)\cos\left(2\pi\frac{f_s}{N}\,t\right)$, with the integrator's output (taking into account the fundamental tone at f_{in} and the alias at $f_s \pm f_{in}$ due to the master clock) leads to the spurious tones at v_x generated by PNIS that can be expressed as

$$v_x = \frac{b}{2} H(f_{in}) \left[A e^{\pm j2\pi\left(\frac{f_s}{N} \pm f_{in}\right)t} + A e^{\pm j2\pi\left(\frac{(N-1)f_s}{N} \pm f_{in}\right)t}\right] \tag{3.6}$$

where $b = \frac{2}{\pi}\sin\left(\frac{\pi}{N}\right)$. In this expression, it has been assumed that $k = 1$, leading to an upper bound in the alias estimation. From eqs. (3.3)-(3.6), it can be obtained that

$$H_2 = \frac{b}{2}\frac{C_3}{C_1} H(f_{in}) H\left(\frac{f_s}{N} \pm f_{in}\right) \tag{3.7}$$

$$H_3 = \frac{b}{2}\frac{C_3}{C_1} H(f_{in}) H\left(\frac{(N-1)f_s}{N} \pm f_{in}\right) \tag{3.8}$$

For $N \geq 3$, the ratio between the magnitude of the alias components due to PNIS and the fundamental tone at the output of the integrator is then given by

$$\left|\frac{v_{out}\left(\frac{f_s}{N} \pm f_{in}\right)}{v_{out}(f_{in})}\right| = \frac{b}{2}\frac{C_3}{C_1}\left|H\left(\frac{f_s}{N} \pm f_{in}\right)\right| \tag{3.9}$$

$$\left|\frac{v_{out}\left(\frac{(N-1)f_s}{N}\pm f_{in}\right)}{v_{out}(f_{in})}\right| = \frac{b}{2}\frac{C_3}{C_1}\left|H\left(\frac{(N-1)f_s}{N}\pm f_{in}\right)\right| \tag{3.10}$$

For $N = 2$, the ratio of the alias to the fundamental component is computed as

$$\left|\frac{v_{out}\left(\frac{f_s}{N}\pm f_{in}\right)}{v_{out}(f_{in})}\right| = b\frac{C_3}{C_1}\left|H\left(\frac{f_s}{N}\pm f_{in}\right)\right| \tag{3.11}$$

Repeating the analysis for the biquadratic filter of figure 12, it can be found that expressions (3.3) and (3.5)-(3.11) are still valid if $H(f)$ is replaced by the proper filter's transfer function. This case is considered in the following section.

C. Simulation Results

For the verification of the analytical results, a 10.7MHz second-order SC bandpass filter using PNIS (figure 12) with unity peak gain, $Q = 10$, $f_s = 65$MHz, $m = 1$, and $N = 2$ was designed and simulated in TSMC 0.35μm CMOS technology; the technology files were provided by MOSIS through its MEP Educational Program. The capacitor ratios were $C_4/C_2 = 1$, $C_4/C_3 = 5$, and $C_3/C_1 = 2$; the actual Q is determined by NC_4/C_3 (10 in this case). The magnitude of the frequency response $|H(f)| = v_{out}(f)/v_{in}(f)$ is shown in the top trace of figure 14. In the bottom trace, the output spectrum due to a 10.7MHz sinusoidal input signal, normalized to the magnitude of the input signal, is also shown. The ratio between the power of the alias tone at $f_{spur} = f_s/2 - f_{in} = (65/2)\text{MHz} - 10.7\text{MHz} = 21.8\text{MHz}$ generated at the output of the filter and the power of the input tone, obtained through circuit simulations, is -21.7dB. For $N = 2$, $C_3/C_1 = 2$ and magnitude response at f_{spur} of -22dB (see figure 14), equation (3.11) predicts a ratio of the tones of -20dB, which is relatively close to the simulated value.

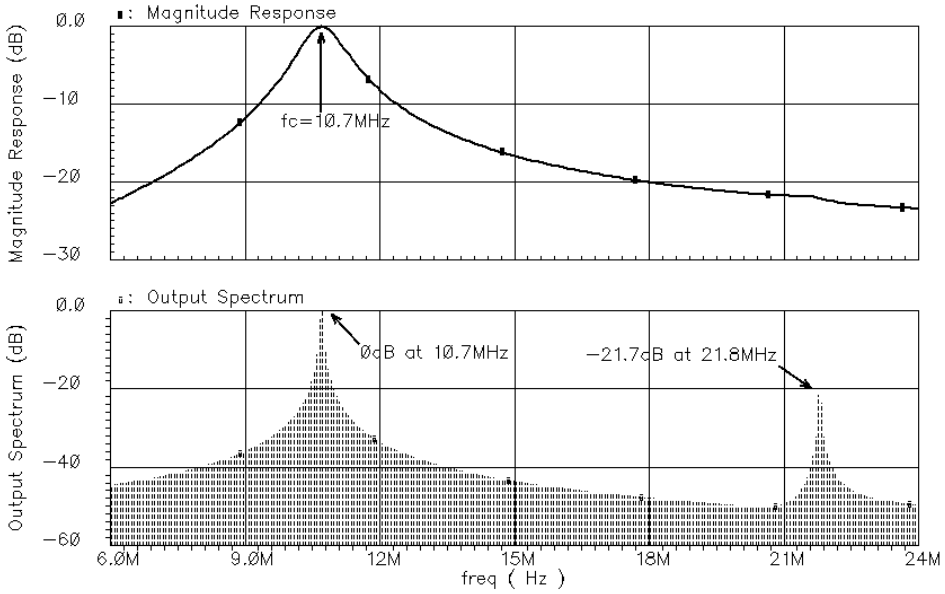


Fig. 14. Simulated frequency response and output spectrum of the bandpass filter using PNIS. Simulated frequency response (top) and output spectrum (bottom). Input tone at the filter's center frequency.

Extensive simulations have been carried out for different frequencies; the results are presented in figure 15. Figure 15(a) shows the ratio of the alias tone at $f_s/2 - f_{in}$ and the amplitude of the input tone, and compares it with the results predicted by equation (3.3), (3.7) and (3.8). The two peaks in this plot are the result of the multiplication of the transfer functions, one of them shifted by (f_s/N) Hz. The ratios between such alias tones and the fundamental tone at the output of the filter predicted by eq. (3.11), and those obtained through circuit simulations are shown in figure 15(b). Notice that these latter plots are a scaled version of the filter's frequency response (shown in figure 14) but mirrored and shifted by (f_s/N) Hz at the x-axis, as expected from eq. (3.11). The error in the estimation of such powers is less than 2.5dB for all frequencies, and as aforementioned this is an upper bound error in the estimation of the alias components.

D. Implications of PNIS in the Design of IF Filters

The use of periodical non-uniform individual sampling for the design of intermediate-frequency (IF) filters results in additional image sidebands; the most important ones located at $f_{sb} = \frac{f_s}{N} \pm f_c$ and $f_{sb} = \frac{(N-1)f_s}{N} \pm f_c$, where f_c is the filter's center frequency. From equations (3.9)-(3.11), for the same input power level of the signal at the filter's center frequency and the interferer at f_{sb}, the ratio between the magnitude of the in-band alias component and that of the desired signal at f_c, at the output of the filter, is given by

$$\frac{in\text{-}band\ alias}{desired} = b\frac{C_3}{C_1}\Big|H(f_{sb})\Big| \quad \text{when} \quad N = 2 \tag{3.12}$$

$$\frac{in\text{-}band\ alias}{desired} = \frac{b}{2}\frac{C_3}{C_1}\Big|H(f_{sb})\Big| \quad \text{when} \quad N \geq 3 \tag{3.13}$$

For the case of the design example discussed in section C (with $N = 2$), according

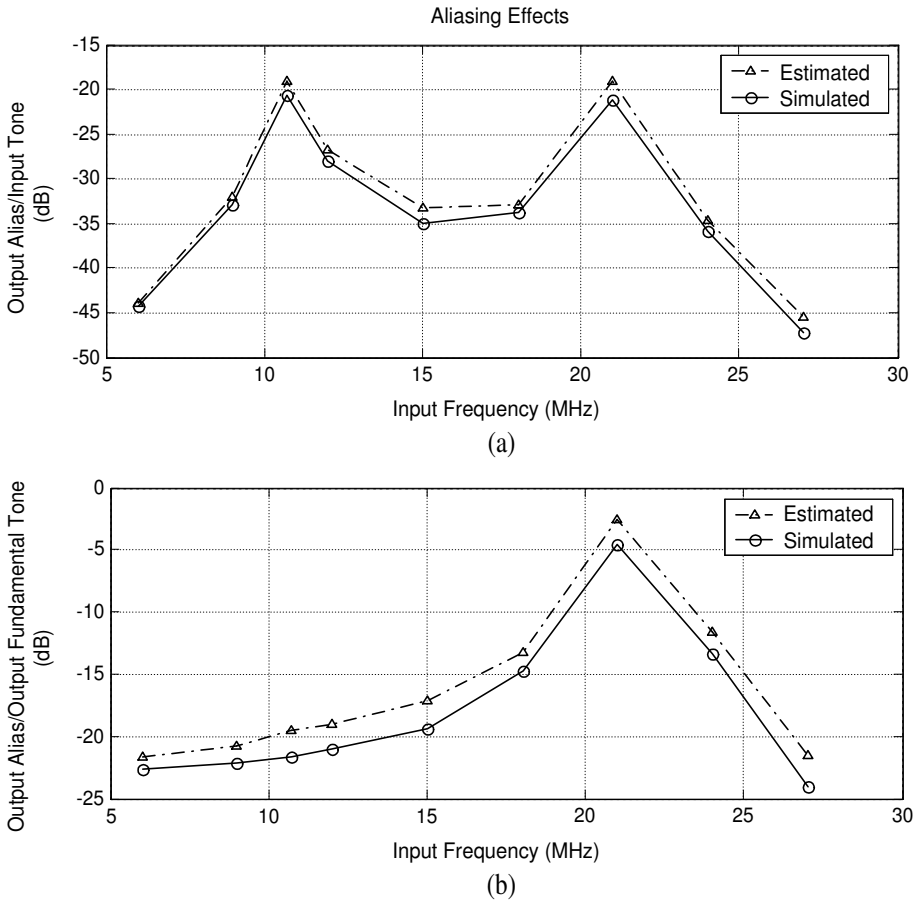


Fig. 15. Simulated vs. predicted aliasing effects at the output of the filter. (a) Power of the alias component at the output of the filter relative to the input tone power, and (b) power of the alias component at the output of the filter relative to the power of the fundamental tone at the output.

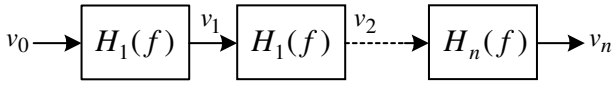


Fig. 16. Higher-order cascaded filter.

to eq. (3.12) an interferer at $f_{sb} = 21.8$MHz generates an in-band alias component at $f_c = 10.7$MHz whose magnitude is -20dBc. Obviously, it is desirable to suppress as much as possible the out-of-band interferers before the filter section that uses slower clocks.

Now, let's extend the analysis to higher-order filters by cascading second-order sections such as the one shown in figure 12, and possibly a first-order section such as figure 13 for the case of odd-order filters. The general case is shown in figure 16. The output power of a tone in the stop-band of the filter at f_{sb} is attenuated by the overall filter's transfer function

$$H_{overall}(f_{sb}) = H_1(f_{sb}) \cdot H_2(f_{sb}) \cdots H_n(f_{sb}) \tag{3.14}$$

which will typically offer high rejection as the number of stages increases. Nevertheless, it is the first stage that uses PNIS the one that determines the rejection to these sidebands. This stage will generate in-band alias signals that will not be filtered by subsequent stages. Therefore, in the design of IF filters using PNIS, the next guidelines should be followed:

1. Place the low-Q resonators as the first stages of the design, and do not use slower clocks on these stages. Usually, low-Q sections do not demand high-capacitor ratios. The first filter stages will attenuate the power of the signals at the critical frequencies without generating in-band spurs.

2. If using PNIS for the first stage, it must provide the required attenuation at f_{sb} as given by equations (3.12) or (3.13). Be sure that the signal to alias interferer ratio is good enough for the application.

3. Choose f_s and N such that possible interferers do not fall at or close to the critical frequencies around f_{sb}.

4. If additional rejection is required, precede the SC IF filter using PNIS with a continuous-time filter (or a SC filter not using PNIS) that provides additional attenuation at f_{sb}.

CHAPTER IV

A 10.7MHz SWITCHED-CAPACITOR FILTER IN CMOS 0.35μm WITH A LOW-INPUT CAPACITANCE/HIGH PSRR COMMON-MODE FEEDBACK

In this chapter, the design of a continuous-time common-mode feedback (CMFB) for switched-capacitor networks is presented. Its reduced input capacitance decreases the capacitive load at the output of the fully-differential amplifier, improving its achievable gain-bandwidth (GBW) product and slew-rate. This topology is more suitable for high-speed switched-capacitor applications when compared to a conventional switched-capacitor CMFB, enabling operation at higher clock frequencies. Additionally, it provides a superior rejection to the negative power supply noise (PSRR$^-$). The performance of the CMFB is demonstrated in the implementation of a second-order 10.7MHz bandpass switched-capacitor filter and compared with that of an identical filter using the conventional switched-capacitor CMFB (SC-CMFB). The filter using the continuous-time CMFB reduces the error due to finite GBW and slew rate to less than 1% for clock frequencies up to 72MHz while providing a dynamic range of 59dB and a PSRR$^-$ > 22dB. Both circuits were fabricated in TSMC 0.35μm CMOS technology.

A. Proposed Common-Mode Feedback Circuit

A fully-differential folded-cascode amplifier with the proposed CMFB is shown in figure 17. Transistors M_{7a}–M_{7d} (all of which are equally sized) sense the output voltages of the amplifier $V_{out+} = V_{out,\,cm} + V_{out,\,dm}/2$ and $V_{out-} = V_{out,\,cm} - V_{out,\,dm}/2$. A DC bias generator such as the one shown in figure 17(c) places a DC voltage between the two resistors R equal to $V_{DC} = V_{ref} - V_{GS,7}$, where V_{ref} is the desired common-mode voltage. Only one DC bias generator is needed for all FD amplifiers

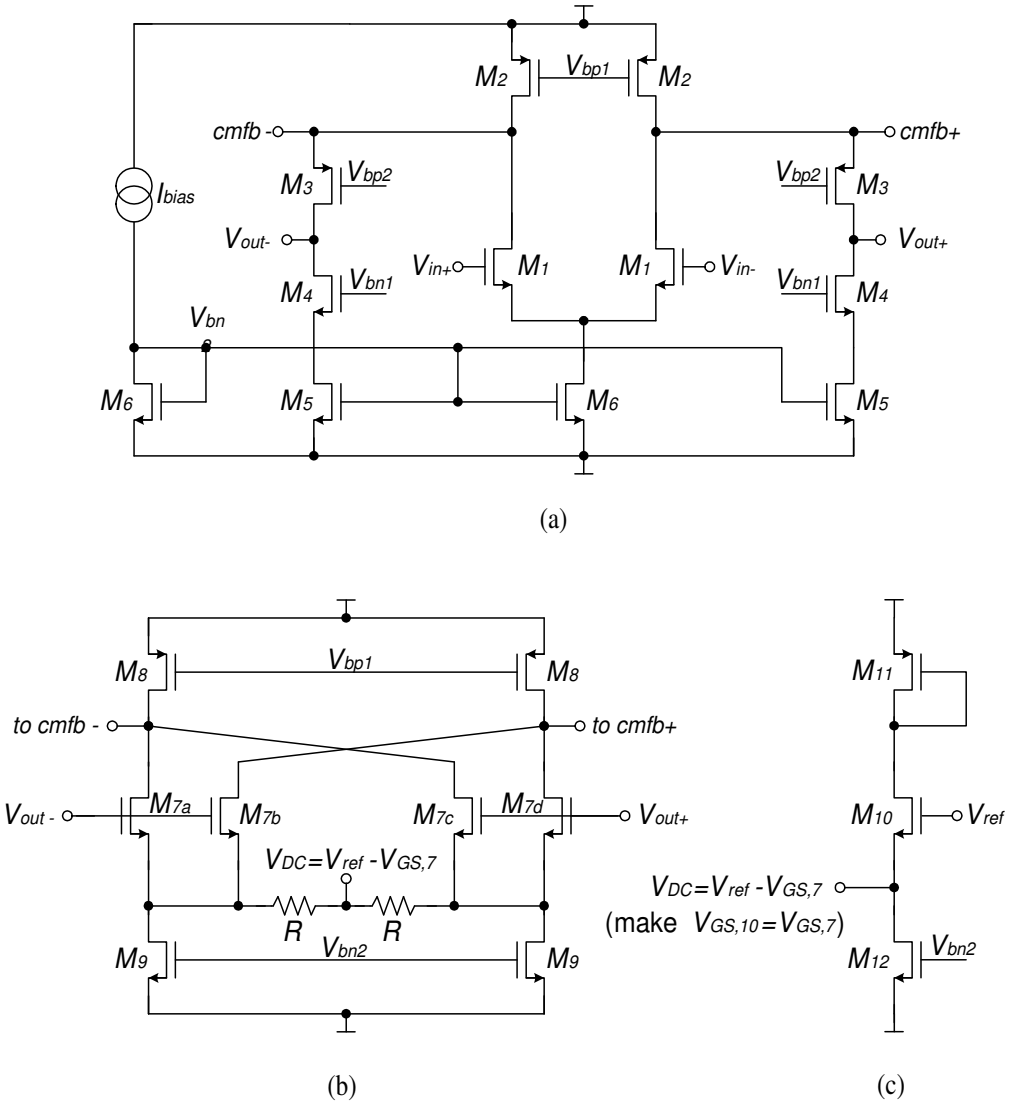


Fig. 17. Proposed continuous-time common-mode feedback. (a) Folded-cascode amplifier, (b) proposed continuous-time CMFB, and (c) DC bias generator.

in the filter. If the circuit operates in its linear range, the voltage drop across R generates the following currents through transistors $M_{7a}..M_{7d}$:

$$\Delta I_{7a} = \Delta I_{7b} = \frac{g_{m,7}}{1 + 2g_{m,7}R}\left(V_{out,\,cm} - \frac{V_{out,\,dm}}{2} - V_{ref}\right) \tag{4.1}$$

$$\Delta I_{7c} = \Delta I_{7d} = \frac{g_{m,7}}{1 + 2g_{m,7}R}\left(V_{out,\,cm} + \frac{V_{out,\,dm}}{2} - V_{ref}\right) \tag{4.2}$$

where $\Delta I_{7i} = I_{7i} - I_9/2$ for $i = \{a, b, c, d\}$ and I_9 is the current through M_9. The resistors R extend the common-mode detector's linear range delimited by $\pm V_{DSAT7}(1 + 2g_{m,7}R)$, making it better suited for switched-capacitor applications when compared to other non-resistive based active common-mode detectors [25]. The cross-coupled connections between the drains of transistors M_{7a},M_{7c} and M_{7b},M_{7d} remove the differential component obtaining the common-mode correction currents as follows:

$$\Delta I_{cmfb+} = \Delta I_{cmfb-} = \frac{2g_{m,7}}{1 + 2g_{m,7}R}\left(V_{out,\,cm} - V_{ref}\right) \tag{4.3}$$

These currents are injected at the source of transistors M_3, therefore compensating for any mismatch between I_3 and I_5, which are the currents through M_3 and M_5 respectively. The output common-mode voltage converges to a final value of $V_{out,cm} \approx V_{ref}$ with a DC error inversely proportional to the loop gain of the common-mode feedback.

The input capacitance of the CMFB circuit, which is the capacitive load added to each output node of the amplifier by the CMFB is given by:

$$C_{in} \approx \frac{2C_{gs,7}}{1 + 2g_{m,7}R} \tag{4.4}$$

which in a typical design in 0.35μm CMOS technologies is around 100–150fF. This value is an order of magnitude smaller when compared to the load capacitance due to the SC-CMFB of figure 8.

1. Loop Gain, Frequency Response and Stability

Using typical circuit analysis techniques, it can be found that the open-loop gain of the proposed CMFB shown in figure 17 is given by

$$H_{CMFB}(s) = A_{CMFB}\left(\frac{p_1}{s+p_1}\right)\left(\frac{p_2}{s+p_2}\right)\left(\frac{p_3}{s+p_3}\right)\left(\frac{s+z_1}{z_1}\right) \tag{4.5}$$

$$\begin{aligned} A_{CMFB} &= \frac{2g_{m,7}R_L}{1+2g_{m,7}R} \\ p_1 &= \frac{1}{R_L C_L} \\ p_2 &= \frac{g_{m,3}}{C_{pp}} \\ p_3 &= \frac{1+2g_{m,7}R}{R\left(2C_{sb,7}+2C_{gs,7}+C_{db,9}\right)} \\ z_1 &= \frac{1}{R\left(2C_{sb,7}+2C_{gs,7}+C_{db,9}\right)} \end{aligned}$$

where R_L and C_L are the output resistance of the amplifier and load capacitance respectively, and C_{pp} is the sum of the parasitic capacitances to ground at the source of M_3. A_{CMFB} is the DC gain of the CMFB loop. The dominant pole p_1 is located at the output node. The non-dominant pole p_2 is located at the source of M_3. The other non-dominant pole p_3 is located at the source of transistors $M_{7a}..M_{7d}$. The only zero z_1 is located also at the source of transistors $M_{7a}..M_{7d}$. Notice from eq. (4.5) and figure 17 that poles p_1 and p_2 are common to both the CMFB and the differential path of the amplifier itself. On the other hand, z_1 is a left half-plane zero and always of lower frequency than p_3, forming a pole-zero pair that will add positive phase margin to the

frequency response of the CMFB. Therefore, designing the amplifier to be stable for unity gain in differential mode and making $2g_{m,7} \leq g_{m,1}$ will guarantee the stability of the CMFB, making it simple to design. This in contrast to other continuous-time implementations such as opamp based approaches [13, 25] which add additional poles that degrade the CMFB loop bandwidth and phase margin.

2. Non-linear and Mismatch Effects

Taking into account the square-law behavior of the MOS transistor working in the saturation region, the AC currents flowing through transistors $M_{7a}..M_{7d}$ of the pseudo-differential CMFB can be expressed as

$$i_{7a} = i_{7b} = a\left(v_{out,\,cm} - \frac{v_{out,\,dm}}{2}\right) + b\left(v_{out,\,cm} - \frac{v_{out,\,dm}}{2}\right)^2 \tag{4.6}$$

$$i_{7c} = i_{7d} = a\left(v_{out,\,cm} + \frac{v_{out,\,dm}}{2}\right) + b\left(v_{out,\,cm} + \frac{v_{out,\,dm}}{2}\right)^2 \tag{4.7}$$

where $a = \dfrac{g_{m,7}}{1 + 2g_{m,7}R}$ and $b = \dfrac{g_{m,7}}{(V_{GS,7} - V_T)\,(1 + 2g_{m,7}R)^3}$.

The feedback currents $i_{cmfb-} = i_{7a} + i_{7c}$ and $i_{cmfb+} = i_{7b} + i_{7d}$ are given by

$$i_{cmfb+} = i_{cmfb-} = 2a \cdot v_{out,\,cm} + 2b \cdot v_{out,\,cm}^2 + 2b\left(\frac{v_{out,\,dm}}{2}\right)^2 \tag{4.8}$$

The third term of equation (4.8) shows a differential-mode to common-mode conversion mechanism due to the non-linearity of the CMFB. The common-mode voltage generated by the differential signal at the output of the amplifier due to the non-linearity of the CMFB is given by

$$v'_{out,\,cm} = \frac{2b\,Z_L}{1 + A_{CMFB}}\left(\frac{v_{out,\,dm}}{2}\right)^2 \tag{4.9}$$

where $Z_L = \dfrac{1}{sC_L} \parallel R_L$ and A_{CMFB} was defined in eq. (4.5). The second-order

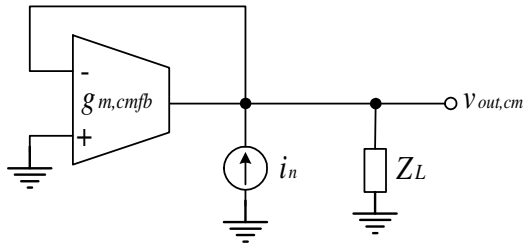


Fig. 18. Equivalent circuit for PSRR$^-$ analysis of the proposed CMFB.

common-mode component as defined in equation (4.9) provides a figure of merit to measure the linearity of the CMFB.

A mismatch between i_{cmfb+} and i_{cmfb-} will also cause a common-mode to differential-mode conversion given by $v'_{out,\,dm} = \Delta i_{cmfb} Z_L$, where $\Delta i_{cmfb} = i_{cmfb+} - i_{cmfb-}$. On the other hand, transistor mismatches in the main amplifier will cause a differential-mode to common-mode conversion [32]. The common-mode output will be attenuated by the CMFB yielding $v'_{out,\,cm} \approx \dfrac{\Delta g_{md}}{g_{m,\,cmfb}}$, where Δg_{md} represents the mismatch of the transconductance in the amplifier's differential pair, and $g_{m,\,cmfb} = \dfrac{2g_{m,7}}{1 + 2g_{m,7}R}$ is the small-signal CMFB's loop transconductance.

3. PSRR of the Proposed Common-Mode Feedback

In this section, the rejection of the noise coming from the negative power supply will be considered. In chapter II, section B.3, after analyzing the PSRR$^-$ of the SC-CMFB, it was concluded that it offers 0dB of rejection in all the frequency range $0 < f < f_{clock}/2$. On the other hand, the PSRR$^-$ of the amplifier with the proposed CMFB shown in figure 17 is dominated by the parasitic drain-substrate capacitances of transistors M_5, M_6 and M_9, the source-substrate capacitances of transistors M_1 and M_4, and the finite output of resistances of transistors M_5, M_6 and M_9. An

equivalent circuit is shown in figure 18, where $g_{m,\,cmfb} = \dfrac{2g_{m,7}}{1+2g_{m,7}R}$ stands for the transconductance of the CMFB as previously defined. The current i_n injected by the noise voltage coming from the negative power supply v_n is given by

$$i_n = v_n \left[g_{o,5} + \frac{g_{o,6}}{2} + g_{o,9} + s\left(C_{db,5} + \frac{C_{db,6}}{2} + C_{db,9} + C_{sb,1} + C_{sb,4} + 2C_{sb,7} \right) \right] \tag{4.10}$$

The voltage gain from the negative power supply noise to the common-mode output of the amplifier is then determined by

$$\frac{v_{out,\,cm}}{v_n} = \frac{g_{o,5} + \dfrac{g_{o,6}}{2} + g_{o,9} + s\left(C_{db,5} + \dfrac{C_{db,6}}{2} + C_{db,9} + C_{sb,1} + C_{sb,4} + 2C_{sb,7} \right)}{g_{m,\,cmfb} + \dfrac{1}{R_L} + sC_L} \tag{4.11}$$

which is well below 0dB for $\omega \leq \dfrac{g_{o,5} + 0.5g_{o,6} + g_{o,9}}{C_{db,5} + 0.5C_{db,6} + C_{db,9} + C_{sb,1} + C_{sb,4} + 2C_{sb,7}}$.

The PSRR$^-$ is inversely proportional to $g_{m,\,cmfb}$, and for fixed dimensions of transistors $M_{7a}..M_{7d}$, it is inversely proportional to the square-root of the power dissipated by the CMFB.

B. Simulation Results

To compare the CMFB schemes, a second-order bandpass switched-capacitor filter was designed with a center frequency $f_c = 10.7$MHz, quality factor $Q = 10$, and a master clock frequency of $f_s = 65$MHz. The filter's schematic is shown in figure 19. Non-uniform individual sampling was used to reduce the capacitance spread. The main clock running at $f_s = 65$MHz is denoted by ϕ. The secondary clock running at $f_s/2 = 32.5$MHz is denoted by θ. Early phases, denoted by $\phi_{i,e}$ and $\theta_{i,e}$, have been used to reduce the effects of charge injection [13]. The capacitor values are included

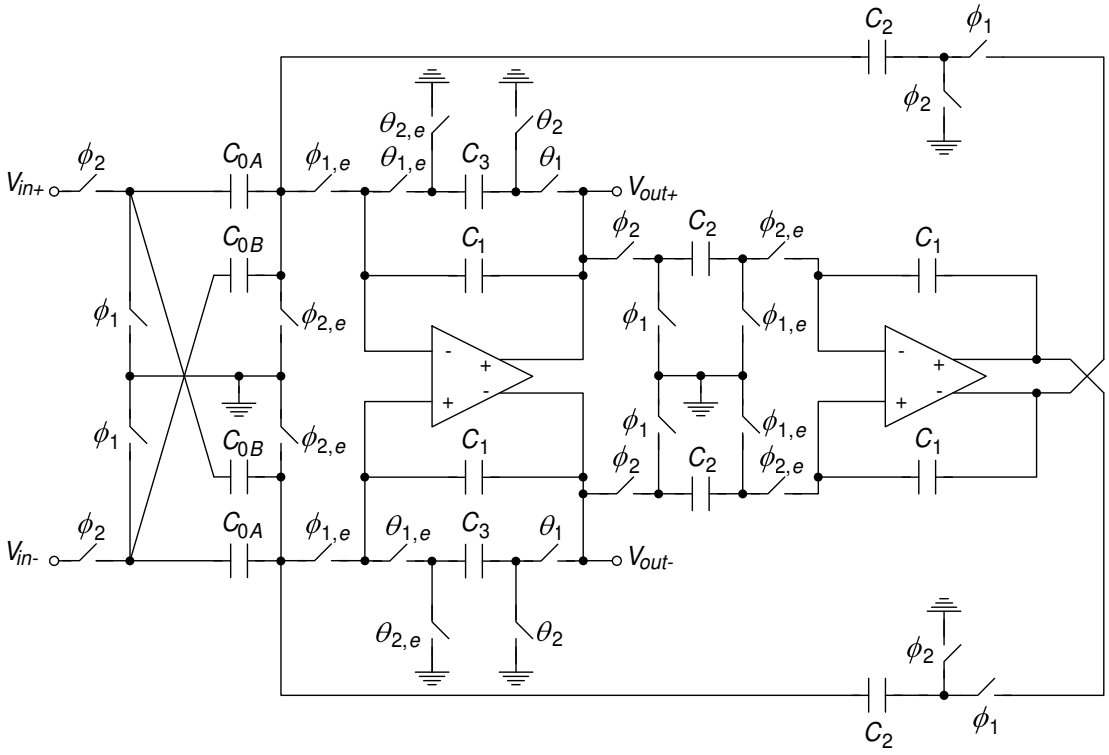


Fig. 19. A fully-differential 10.7MHz second-order bandpass filter.

in table I.

Table I. Capacitor values for the 10.7MHz bandpass filter.

Capacitor	**Value**
C_{0A}	300fF
C_{0B}	200fF
C_1	978fF
C_2	996fF
C_3	200fF

The same filter was implemented using the SC-CMFB (fig. 8) and the proposed CMFB (fig. 17) to compare their performance, keeping the rest of the circuit the same. The transistor dimensions and bias conditions of the folded-cascode amplifier with the proposed CMFB are shown in table II. The capacitors used for the SC-CMFB are shown in table III (the same folded-cascode amplifier was used in both cases).

The differential open-loop gain and common-mode feedback open-loop gain of the folded-cascode amplifier and proposed CMFB are shown in figures 20 and 21 respectively, along with their corresponding phase responses. A load capacitance of $C_L = 660$fF and a feedback factor of $\beta = 0.28$ have been used (these are values required for one of the integrators in the filter). A phase margin of 63° in the differential loop gain and 82° in the CMFB loop gain show that proper stability conditions are satisfied in both modes of operation. Since the CMFB loop gain has its non-dominant poles at higher frequencies than its gain-bandwidth product GBW_{CMFB}, its closed-loop 1% settling time is approximately given by $t_s \approx 5/GBW_{CMFB}$, with the units of

Table II. Component values and currents for the FD amplifier and CMFB.

Component Name	**Value**	$\boldsymbol{I_D}$
M_1, M_{10}	168μm/0.6μm	512μA
M_2	88μm/1.2μm	1.024mA
M_3	80μm/0.4μm	512μA
M_4, M_5, M_9, M_{12}	54.4μm/0.9μm	512μA
M_6	108.8μm/0.9μm	1.024mA
M_{7a}, M_{7b}, M_{7c}, M_{7d}	84μm/0.6μm	256μA
M_8, M_{11}	44μm/1.2μm	512μA
R	330Ω	–

Table III. Capacitor values for the SC-CMFB.

Capacitor	**Value**
C_c	1pF
C_s	200fF

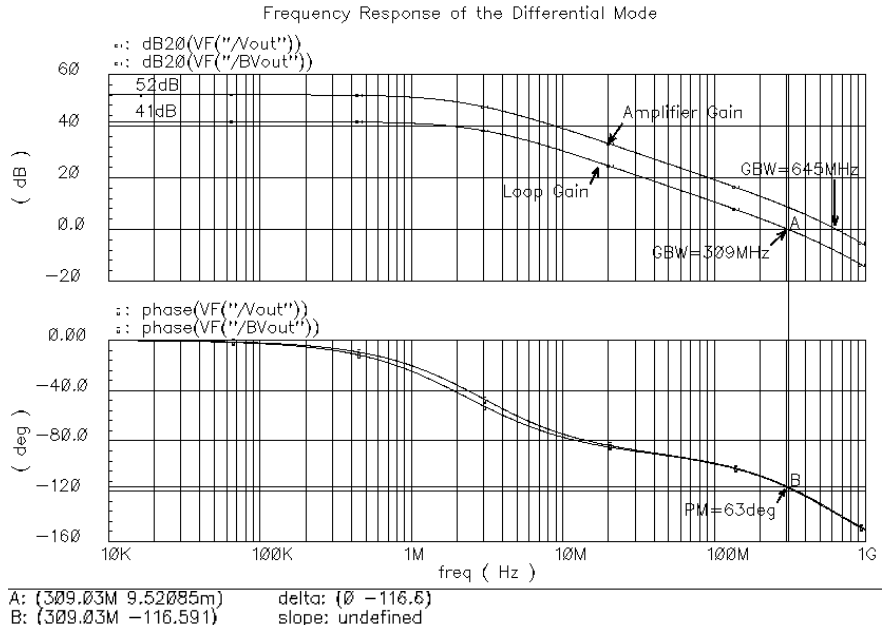


Fig. 20. Differential-mode open loop frequency response.

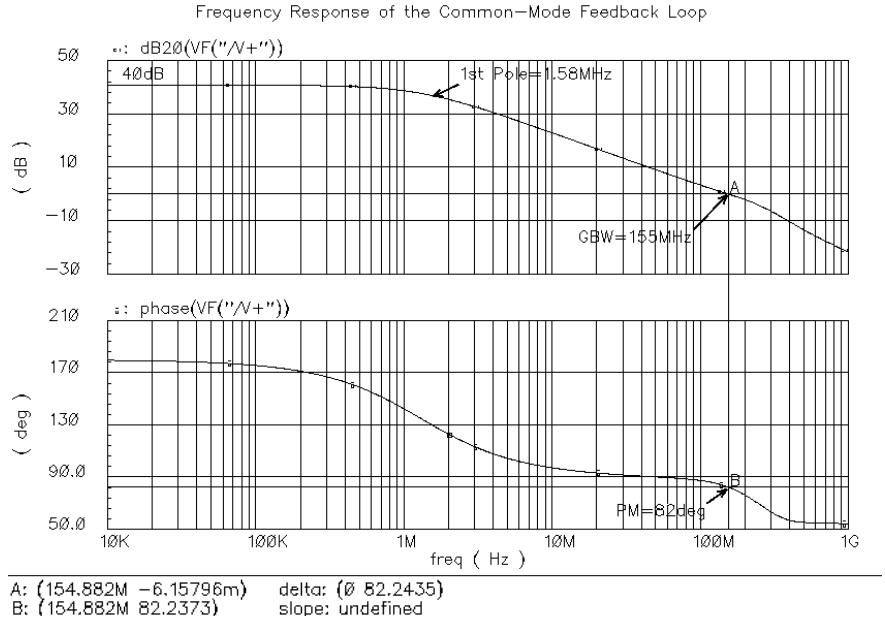


Fig. 21. CMFB open loop frequency response.

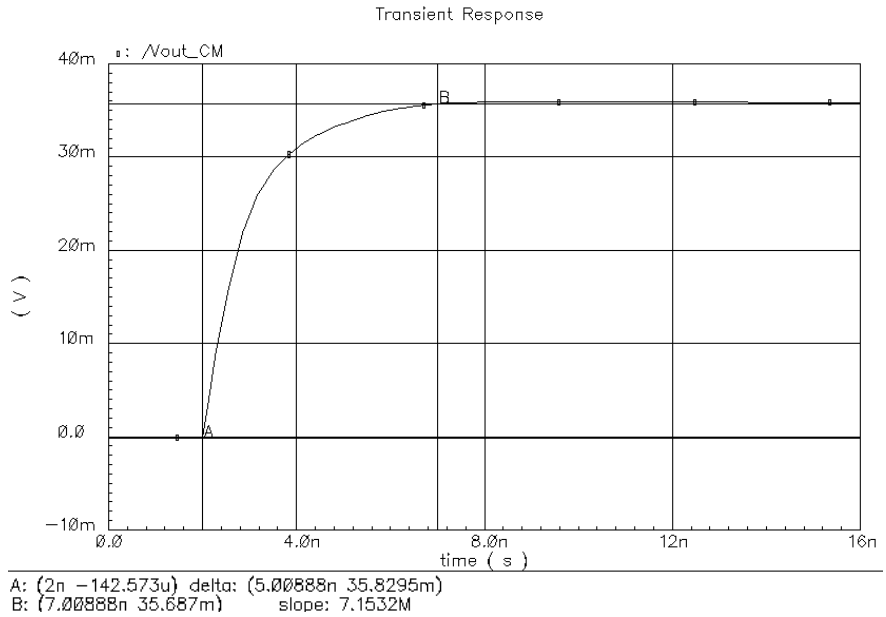


Fig. 22. Time response of the common-mode output.

GBW_{CMFB} being in rad/s. This is shown in figure 22, where a 40μA common-mode current pulse has been injected at each output of the amplifier, and the settling of its output common-mode voltage is verified to be $t_s \approx 5/(2\pi \cdot 155\text{MHz}) = 5\text{ns}$. Therefore, the CMFB can handle clock frequencies up to 100MHz (clock periods of 10ns).

The magnitude of the second-order common-mode component generated by the proposed CMFB (defined in section A.2) versus the magnitude of the differential output, obtained through circuit simulations, is shown in figure 23 using different values of R, and compared with the theoretical results predicted by eq. 4.9. The minimum value of R can then be determined from the maximum common-mode distortion and DC offset that can be tolerated. A value of $R = 330\Omega$ (or $V_{DSAT7}(1 + 2g_{m,7}R) = 500\text{mV}$) was chosen to achieve a second-order common-mode harmonic of $v'_{out,\,cm} = 10\text{mV}_{\text{pp}}$ for a differential output of 600mV_{pp}.

The simulated negative power supply rejection of the FD amplifier with the pro-

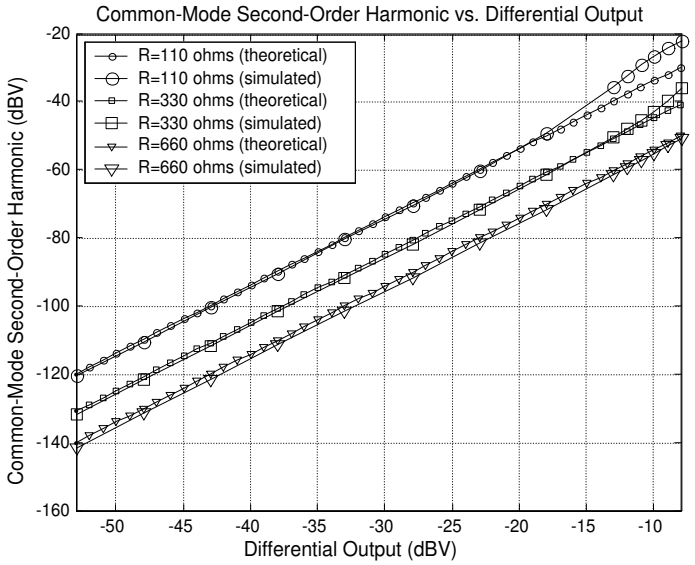


Fig. 23. Common-mode second-order harmonic vs. differential output.

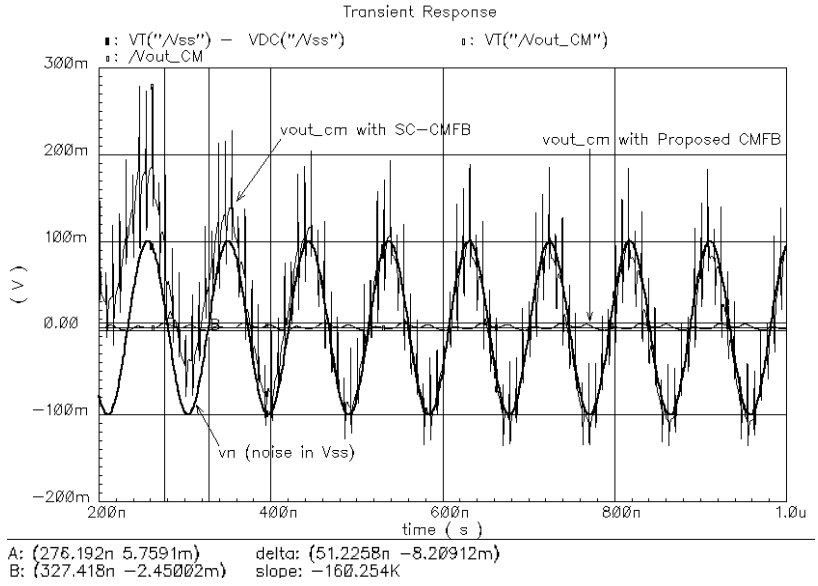


Fig. 24. PSRR$^-$ of the SC-CMFB and proposed CMFB. Comparison between the common-mode output due to noise on V_{SS} when the SC-CMFB and proposed CMFB are used ($f_{signal} = 10.7MHz$).

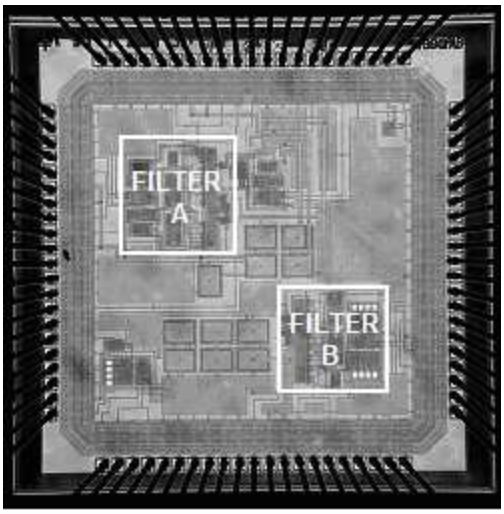


Fig. 25. Chip micrograph of the CMFB circuits. (a) filter A uses SC-CMFB, (b) filter B uses proposed CMFB.

posed CMFB is shown in figure 24. A 100mV_{pp} signal at 10MHz was applied on V_{SS}. A 26dB rejection was achieved at the output, along with the second-order common-mode harmonic as previously discussed in section A.2. This result is compared with the rejection of 0dB obtained using the SC-CMFB (also shown in figure 24), which results in a common-mode output of $V_{out,\,cm} = 100\text{mV}_{\text{pp}}$.

C. Experimental Results

The two filters with the different CMFB circuits were fabricated in TSMC 0.35μm CMOS technology through the MOSIS Educational Program. The chip micrograph is shown in figure 25. The die size is 2.5mm $\times$ 2.5mm.

The measured frequency response of the bandpass filter designed with the proposed CMFB is shown in figure 26. This was obtained using the test setup depicted in figure 27. The relative error in the center frequency due to finite GBW and slew rate

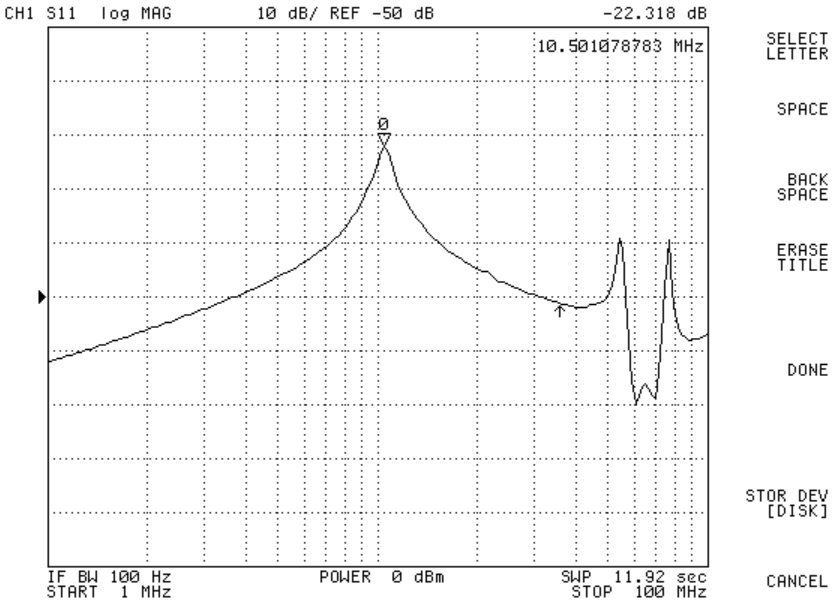


Fig. 26. Frequency response of bandpass filter with the proposed CMFB.

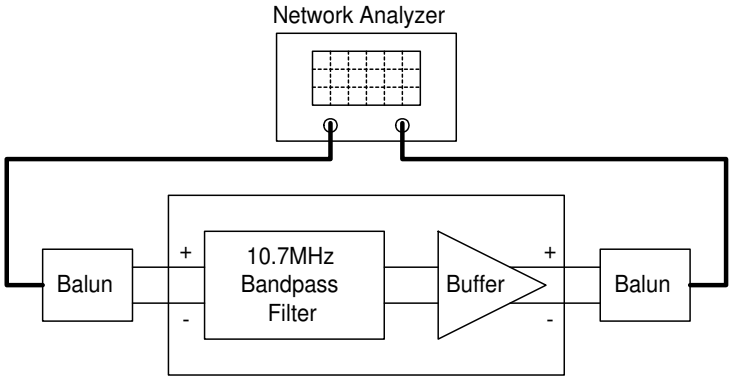


Fig. 27. Test setup for the frequency response characterization of the 10.7MHz bandpass filters.

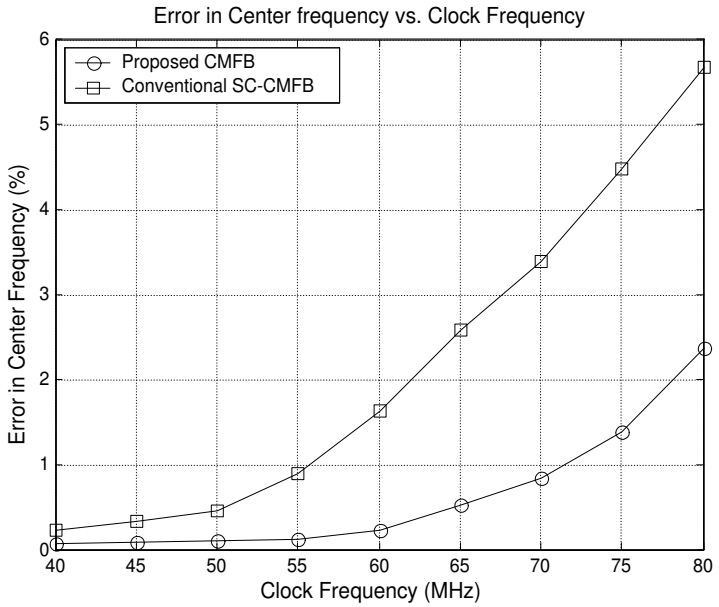


Fig. 28. Measured errors in center frequency vs. clock frequency.

(i.e. dynamic error) versus different clock frequencies ranging from 40MHz to 80MHz is shown in figure 28. For this test, the static errors (f_c/f_s and Q) due to fringe capacitances and capacitor mismatches were removed by measuring the error when the filter operates at low clock frequencies. The same tests were performed for the bandpass filter using the conventional SC-CMFB. The error starts to increase drastically when using the SC-CMFB, while kept relatively small (below 1%) for faster clock frequencies (up to 72MHz) when using the proposed CMFB, proving to be more suitable for high-speed applications.

The IM3 (with two input tones of -3dBm each) versus different clock frequencies was measured for both filters, and the results are shown in figure 29. The test setup used for this characterization is shown in figure 30 (the IM3 of the buffer was designed to be >16dB better than the filters' to not affect the linearity measurements).

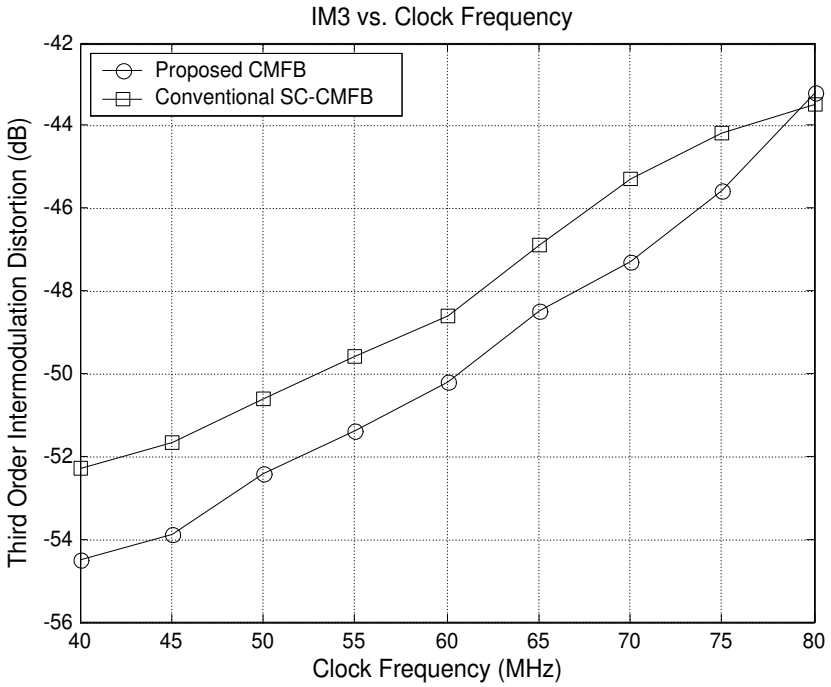


Fig. 29. Measured IM3 vs. clock frequency.

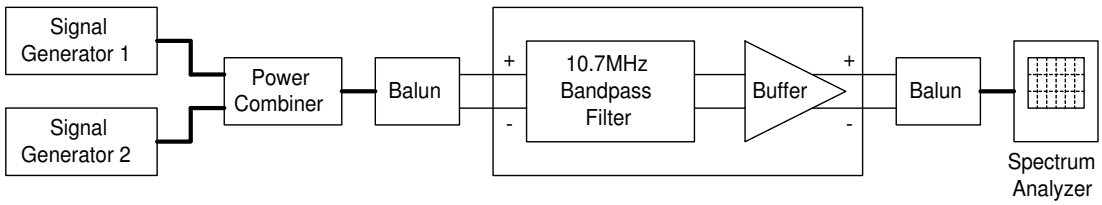


Fig. 30. Test setup for the intermodulation distortion characterization of the 10.7MHz bandpass filters.

The filter with the continuous-time CMFB shows a slightly superior performance by approximately 1.5dB at the nominal clock frequency of 65MHz. As the clock frequency goes beyond 80MHz, both filters exhibit similar IM3 performance because the distortion is dominated by the on-resistance of the switches rather than by the amplifier or the CMFB.

The PSRR^- of the filter with the SC-CMFB is 1.5dB, while that with the proposed CMFB is 22dB, which is a significant improvement. The filter with the continuous-time CMFB showed a worse CMRR by 5.5dB than that with the SC-CMFB, but its CMRR and PSRR can be further improved by increasing $g_{m,\,cmfb}$.

A comparison of the experimental results of the two filters is summarized in table IV. It is worth to mention that while the proposed CMFB increases the power consumption (it uses about 1/3 of the total bias current consumed by the amplifier), the same performance can not be achieved if this additional power is used in the amplifier while keeping the SC-CMFB. Besides having a poor PSRR^-, increasing the bias current on the amplifier reduces its DC gain (increasing errors in f_c/f_s and Q), and the larger output devices needed to keep the output swing reduce the frequency of the non-dominant poles, degrading the differential-mode GBW and phase margin.

Table IV. Comparison of the filter performance for the two CMFB circuits.

	Proposed CMFB	**Conventional SC-CMFB**
Clock Frequency	65MHz	65MHz
Center Frequency	10.50MHz	10.28MHz
Quality Factor	9.78	9.72
Passband Gain	−1.28dB	−1.28dB
IM3 with $P_{in} = 0$dBm	−48.3dB	−47.4dB
SNR (IM3 = −48dB, BW = 1MHz, including buffer)	59dB	58dB
CMRR (at $f_c = 10.7$MHz)	41dB	46.5dB
PSRR$^+$ (at $f_c = 10.7$MHz)	32.5dB	41dB
PSRR$^-$ (at $f_c = 10.7$MHz)	22dB	1.5dB
I_{DC} @ Analog Supply	9.76mA	6.72mA
Analog Supply	±1.5V	±1.5V

CHAPTER V

EQUALIZERS AND THEIR APPLICATION IN WIRELINE TRANSCEIVERS

The ever increasing speed at which data needs to be transmitted through telecommunication networks demands newer technologies and state of the art solutions to bottlenecks that limit the performance of current systems. As a result, the research in the design of integrated circuits for broadband communications systems has become increasingly important. This chapter provides an overview on the fundamentals of Fast Wireline Data Transmission: Transceiver Architecture, Channel Distortion, Inter-symbol Interference and Channel Equalization. Then the discussion focuses on the implementation of different types of equalizers and their limitations, as this will provide the basis for the material to be covered in the following chapters.

A. Architecture of Wireline Transceivers

A generic architecture of a wireline transceiver for serial communications is shown in figure 31 [7, 33].

The input data to be transmitted coming from N different digital channels is serialized and synchronized with a Multiplexer (Mux) and a Retimer [34]. The resulting signal has a higher baud rate (symbol rate) than each of the N input channels. This serialized data is then coupled into the channel through a Line Driver [35], which must provide the required transmission power and the adequate output impedance that matches the characteristic impedance of the transmission line [36]. For some applications, pre-emphasis is added into the frequency response of the line driver [37], as will be discussed in this chapter, subsection B.3.

Due to the finite bandwidth of the channel, the high frequency content of the signal is attenuated, causing Inter-symbol Interference (ISI). To compensate for this

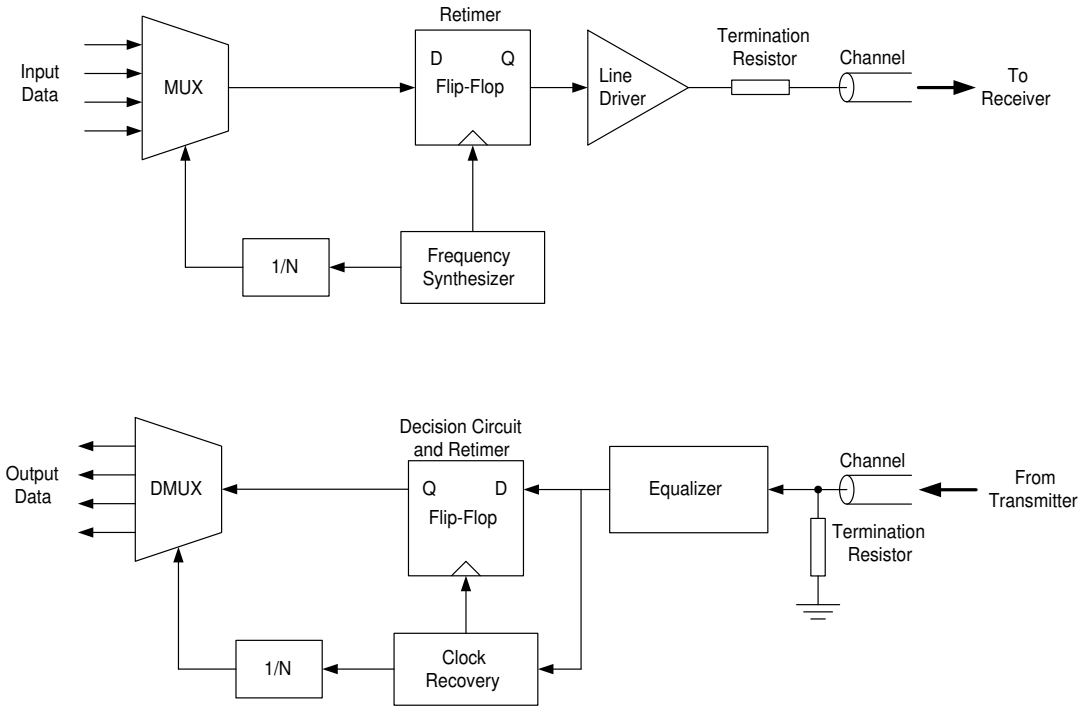


Fig. 31. Transceiver architecture.

distortion, the input on the receiver goes through an Equalizer [38]. The data is then recovered and retimed using a Clock and Data Recovery (CDR) circuit [39]. The decision circuit used in the data recovery is sometimes referred to as "slicer". Finally, the data is deserialized through a demultiplexer (DMUX) [40] to recover the original N transmitted channels.

B. Channel Distortion, Inter-symbol Interference and Equalization

1. Channel Distortion

The voltage of a signal propagating along a transmission line at a particular location z can be expressed as [41]

$$V(z) = V_o^+ e^{-\gamma z} + V_o^- e^{\gamma z} \tag{5.1}$$

where V_o^+ denotes the signal propagating in the $+z$ direction (transmitted wave) and V_o^- denotes the signal propagating in the $-z$ direction (reflected wave). γ is called the propagation constant and can be defined in terms of an attenuation constant α and a phase constant β as

$$\gamma = \alpha + j\beta \tag{5.2}$$

The attenuation and phase constants are given by

$$\alpha(\omega) = \frac{k_R}{2}\sqrt{\frac{\omega C}{L}} \tag{5.3}$$

$$\beta(\omega) = \omega\sqrt{LC} + \frac{k_R}{2}\sqrt{\frac{\omega C}{L}} \tag{5.4}$$

where ω is the angular frequency in rad/sec of the propagating signal, and L (inductance per unit length), C (capacitance per unit length) and k_R are determined by the physical dimensions of the transmission line [42].

As equations 5.1 and 5.3 show, the attenuation increases as the frequency and the length of the transmission line increase. A typical attenuation profile of an unshielded twisted-pair (UTP) CAT5e cable used for Ethernet applications is shown in table V [43]. The magnitude and phase responses of a 15 meters cable are shown in figures 32 and 33, respectively. Notice that the phase is approximately linear resulting in a constant group delay. Therefore, the phase response has a negligible effect on the

Table V. Typical attenuation vs. frequency profile in CAT5e cable.

Frequency (MHz)	**Attenuation (dB/m)**
31.25	0.11
62.5	0.15
100	0.20
155	0.25
200	0.29
250	0.33
300	0.37
350	0.40
400	0.43
450	0.46
500	0.49
550	0.52

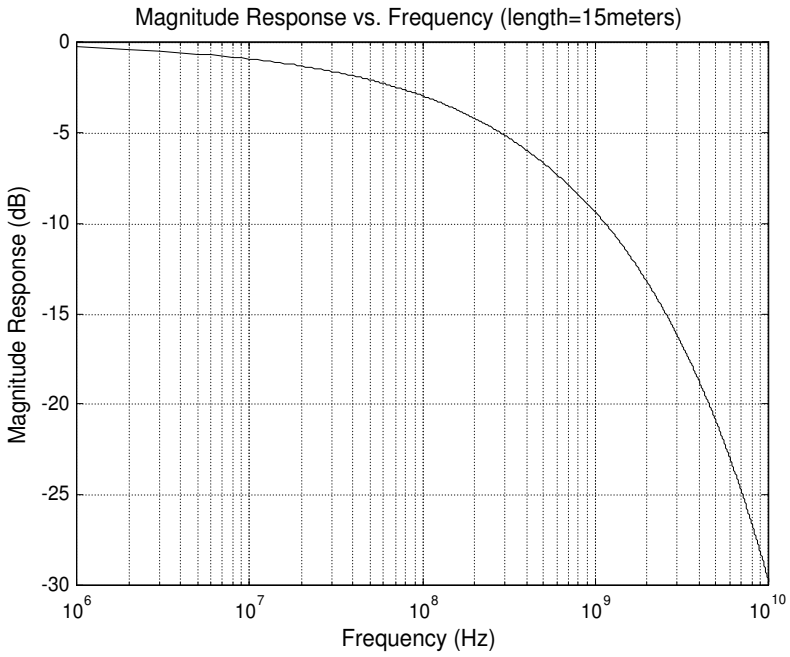


Fig. 32. Magnitude response of a 15 meter UTP CAT5e cable.

propagating signal, and the distortion is dominated by the magnitude response. This is in contrast to fiber optic systems, where the main cause of distortion is the pulse spreading due to the phase response of the fiber (also called fiber dispersion) [44].

2. Inter-symbol Interference

Inter-symbol interference (ISI) is the term to denote that a received symbol depends on the symbols that were sent before (precursor ISI) and after (postcursor ISI). In other words, if the received signal $y(t)$ is sampled every T seconds, it can be expressed as [5]

$$y(kT) = \sum_{n=0}^{\infty} I_n h(kT - nT) \tag{5.5}$$

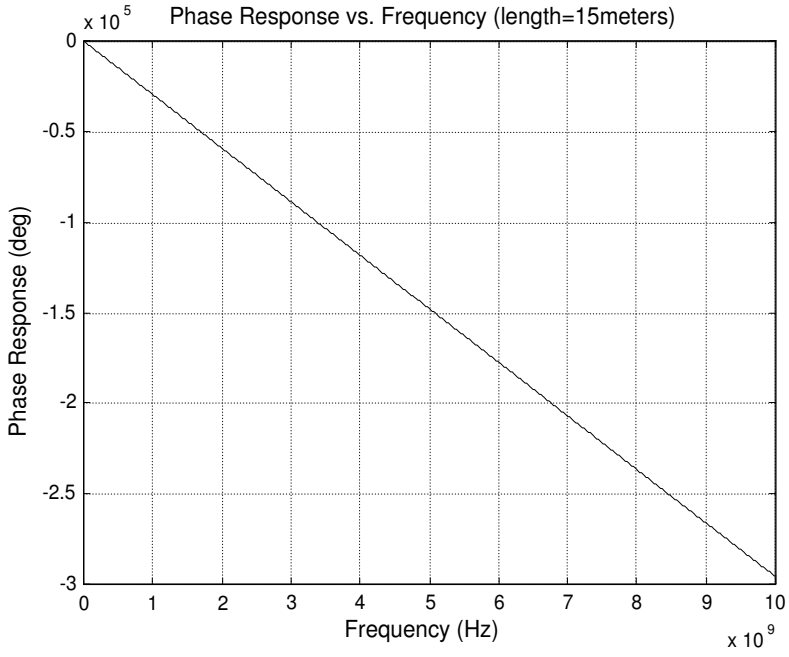


Fig. 33. Phase response of a 15 meter UTP CAT5e cable.

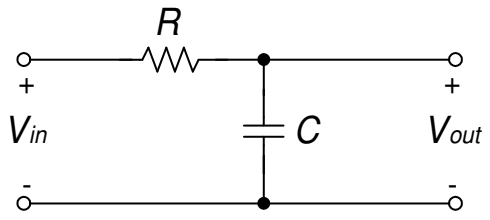


Fig. 34. First-order channel model.

or equivalently

$$y_k = \sum_{n=0}^{\infty} I_n h_{k-n} = \underbrace{h_0 I_k}_{desired} + \underbrace{\sum_{n=0}^{n<k} I_n h_{k-n}}_{precursor ISI} + \underbrace{\sum_{n>k}^{\infty} I_n h_{k-n}}_{postcursor ISI} \tag{5.6}$$

where k is a positive integer, I_n are the original transmitted symbols, and $h(t)$ is the overall impulse response of the system, including the transmitter filter, channel response and receiver filter.

Bandlimited channels generate ISI. Consider a first order channel model as shown in figure 34. If a random bit sequence at a certain data rate containing frequency components beyond the 3dB frequency is passed through the channel, the filtered output will have significant ISI as shown in figure 35. It can be observed that if a $+1$ bit is preceded and followed by long sequences of -1, it will have a smaller amplitude compared to the case in which it is preceded and followed by long sequences of $+1$. Therefore, the received symbols depend on the previous a following data, making it difficult for the decision circuit in the receiver to recover the original information.

When testing a wireline communication system, the output of the channel is typically monitored using an oscilloscope. If the oscilloscope is synchronized using the system's clock, and the traces of the signal are allowed to overlay continuously on the scope, an "Eye-Pattern Diagram" is generated, as shown in figure 36.

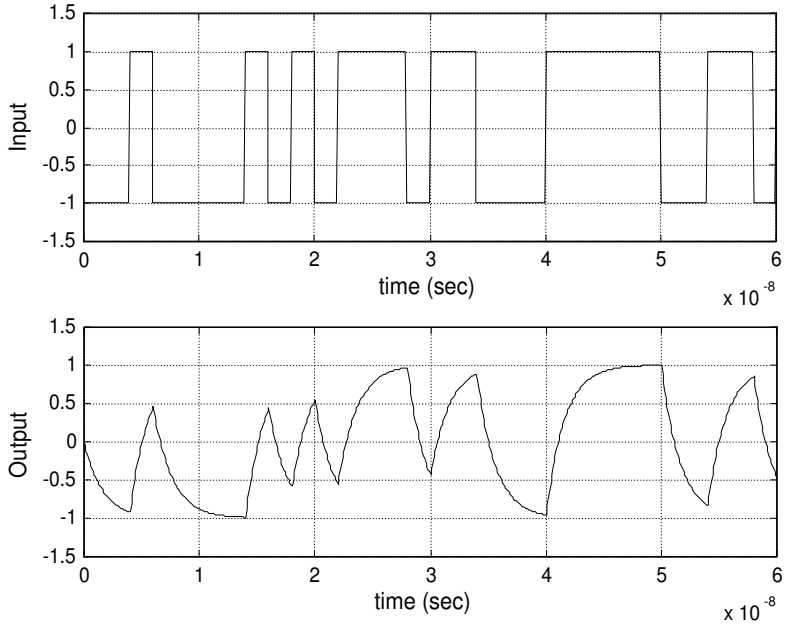


Fig. 35. Input (upper) and output (lower) from a first-order channel.

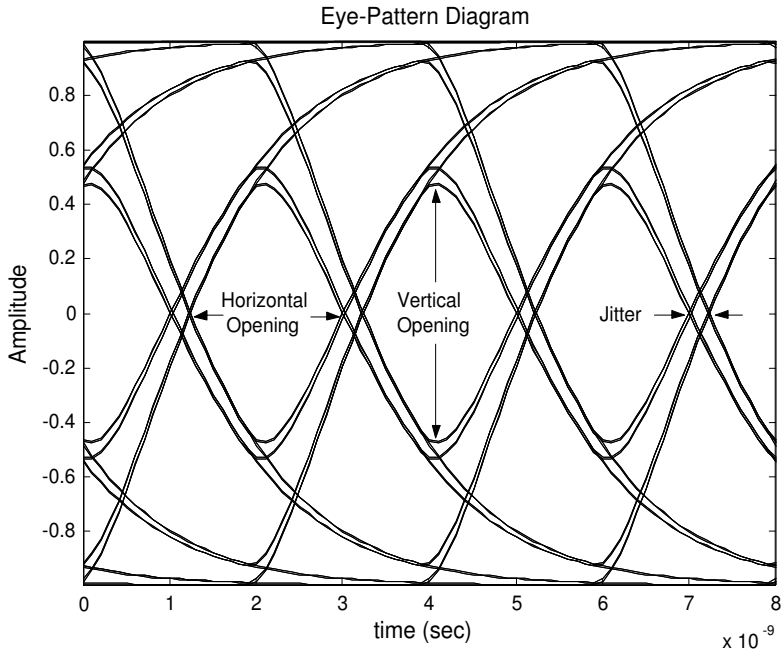


Fig. 36. Eye-pattern diagram.

The definitions of vertical and horizontal openings are self-explanatory from figure 36. Jitter is the time variation of the zero-crossing points. The are two kinds of jitter: (a) deterministic jitter, which is the result of bandlimited channels and (b) random jitter, which results from finite signal-to-noise ratio in the system.

3. Equalization

To overcome the limitations imposed by the finite frequency response of the channel and the resulting ISI, equalization is used in the receiver as shown in figure 37.

To compensate for the channel's distortion, the equalizer must theoretically have a transfer function given by

$$E(z) = \frac{1}{C(z)} \tag{5.7}$$

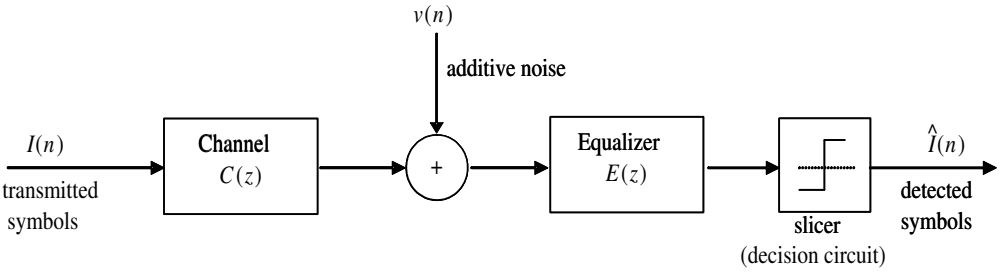


Fig. 37. Equalization applied on the receiver.

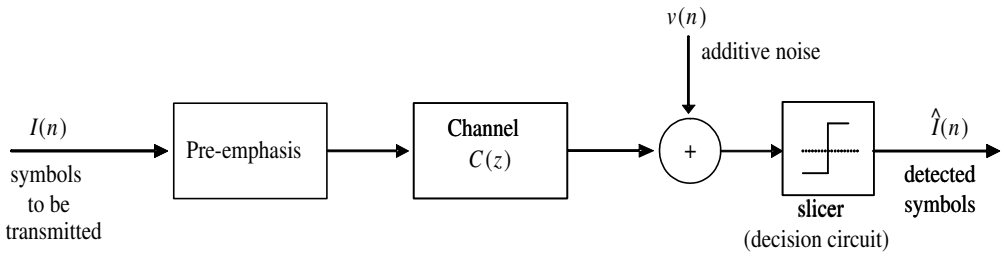


Fig. 38. Pre-emphasis applied on the transmitter.

where $C(z)$ is the frequency response of the discretized channel. The different types of equalizers and their limitations are discussed in section C of this chapter.

Alternatively, as shown in figure 38, pre-emphasis can be applied in the transmitter to boost the high-frequencies that will be attenuated by the channel [37]. The drawbacks of this technique are: (a) increased transmitted power, (b) additional dynamic range required depending on the amount of peaking in the transmitter, and (c) increased electromagnetic interference.

C. Types of Equalizers

A classification of the different types of receiver equalizers is shown in figure 39.

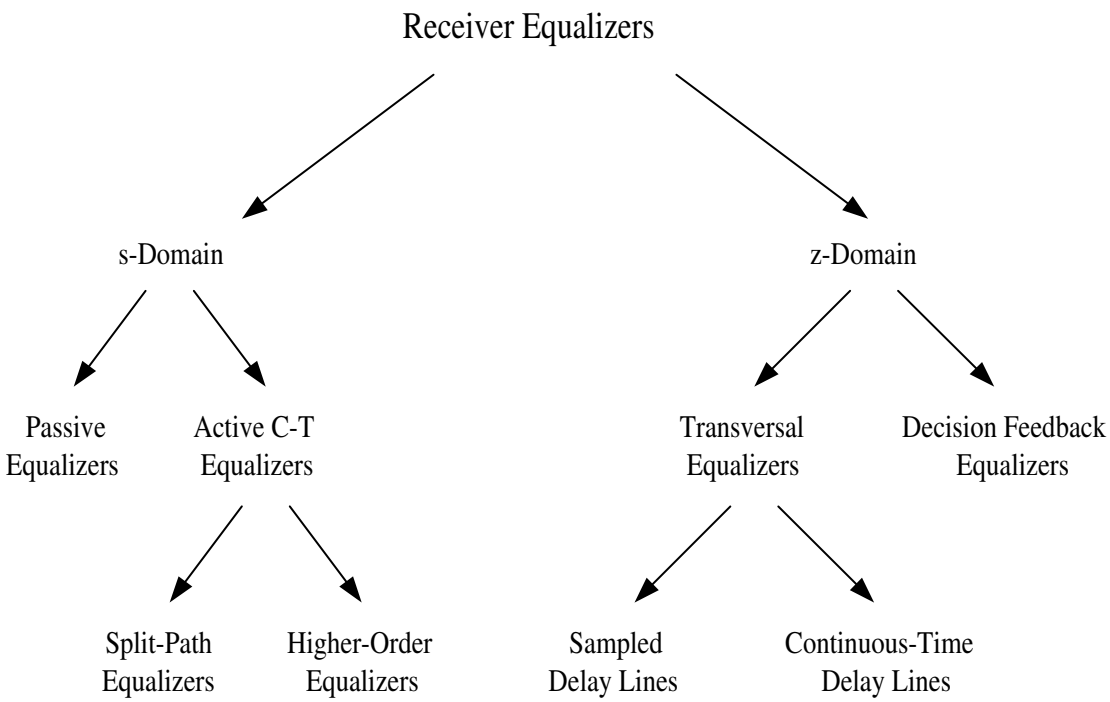


Fig. 39. Classification of receiver equalizers.

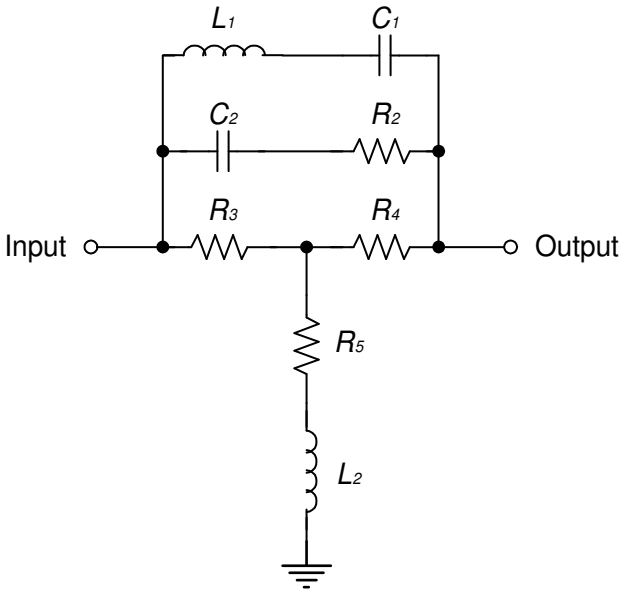


Fig. 40. Passive T-bridge equalizer.

1. Passive Equalizers

Figure 40 shows a passive equalizer using a bridged-T network reported in [45]. R_3, R_4, R_5 and L_2 set the characteristic impedance; C_2 and R_2 set the low frequency compensation; L_2 sets the mid-band frequency compensation; L_1 and C_1 define the high frequency compensation. The advantages of using a passive equalizer are low power consumption and ease of implementation. The main disadvantages include low signal-to-noise level, and narrow compensation range.

2. Active Continuous-Time Equalizers

An active continuous-time equalizer proposed in [6] is shown in figure 41. This feedforward equalizer provides two different paths for the signal. The main path is comprised of a flat response amplifier. The additional feedforward path provides the necessary

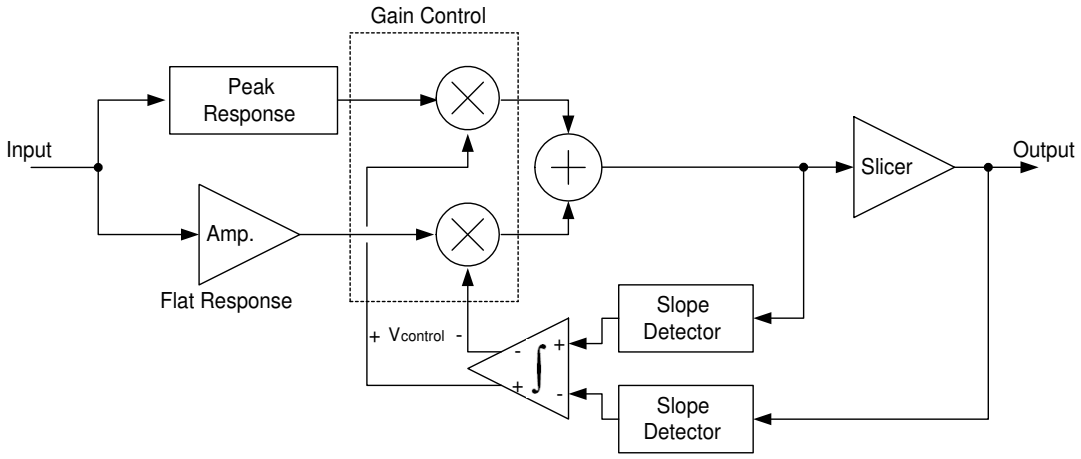


Fig. 41. Active continuous-time feedforward equalizer.

high-frequency emphasis or peak response. The gain of each path is controlled by a feedback loop which monitors the slopes of the transitions before and after the slicer. The gain of each path converges when the error between these slopes is minimized. Higher-order active continuous-time equalizers have also been proposed [46, 47].

3. Transversal Equalizers

Transversal equalizers are FIR filters with adjustable coefficients (also referred to as taps). There are two kinds of transversal equalizers: (1) symbol-rate equalizers and (2) fractionally-spaced equalizers [48].

Symbol-rate equalizers have their sampling period T_s equal to the symbol or baud rate T_b. Although these equalizers work at the Nyquist Rate, aliasing is observed in the sampled spectrum due to residual frequency components beyond $f_s/2 = 1/(2T_s)$.

To overcome the above limitation, fractionally-spaced equalizers (FSE) are used. The sampling period $T_s < T_b$ is chosen such that aliasing and consequently interference between adjacent spectra is avoided. A sampling frequency of $T_s = T_b/2$ is

typically used [48].

With the advent of digital signal processing, z-domain equalizers have become very popular. Depending on the number of coefficients, they can provide more degrees of freedom than s-domain equalizers, an compensate for a wider range of channel responses. Furthermore, they can incorporate adaptive techniques such as the Least-Mean-Square (LMS), Recursive-Least-Squares (RLS), and Zero-Forcing algorithms to find the optimal coefficients for minimum ISI [38, 49]. Other techniques to find the coefficients include: (1) sgn-sgn LMS [50], and (2) eye-opening monitor [51].

Unfortunately, the speed at which data communications systems need to operate has increased faster than the speed at which a digital signal processor (DSP) can work. Furthermore, the design of high-speed ADCs required to convert the received analog signal into digital bits at Gb/s rates is still a challenge in current CMOS technologies [5] and require high power consumption. As a result, analog and mixed-signal implementations of transversal equalizers have been proposed. In such architectures, the unit delay cells z^{-1}, multipliers and summing node are implemented with dedicated analog or mixed-signal circuits. Different topologies and their limitations will be the topic of chapters VI and VII.

4. Decision Feedback Equalizers

The block diagram of a Decision Feedback Equalizer (DFE) is shown in figure 42. The DFE uses the previous outputs of the slicer to cancel the ISI of previous symbols onto the current symbol. The output is given by

$$y(n) = x(n) - \sum_{k=1}^{N} c_k \tilde{y}(n-k) \tag{5.8}$$

Suppose that a channel has an impulse response that if sampled at the symbol rate $T_s = T_b$, results in a unilateral sequence (i.e. consists of only postcursor

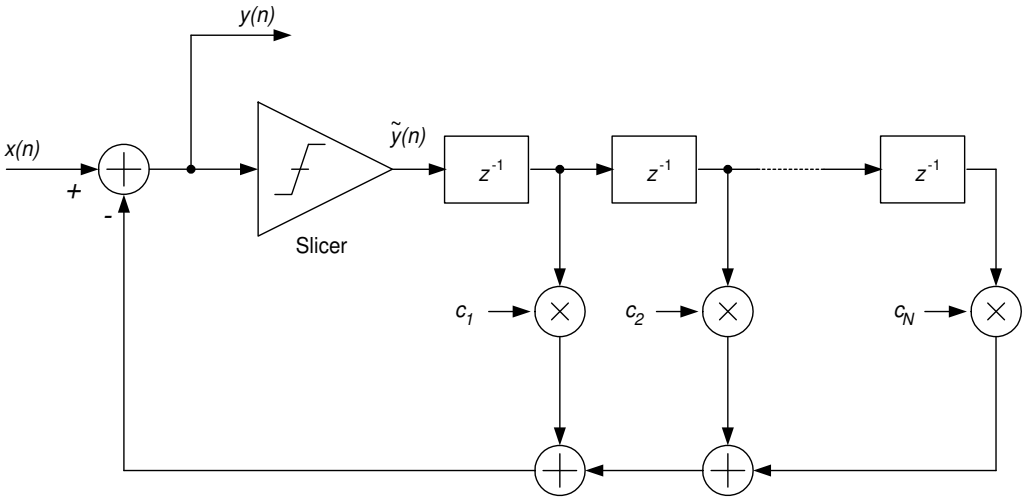


Fig. 42. Decision feedback equalizer.

components). For example:

$$H = [h_0, h_1, h_2] = [1, 0.25, -0.15]$$

The output of the slicer is used to reproduce this impulse response and cancel it at its input for the next decision. Therefore, if the coefficients of the DFE $[c_1, c_2] = [0.25, -0.15]$, the ISI will be removed. One advantage over transversal equalizers is that, since DFEs operate with the data after the slicer (i.e. does not operate with the noisy data prior to the slicer), the noise is not amplified by the DFE. The two main disadvantages are: (1) the propagation of error if an incorrect decision is taken by the slicer [48], and (2) the DFE only removes postcursor ISI. To remove precursor ISI, a transversal of feed-forward equalizer typically precedes a DFE [40].

In high-speed decision feedback equalizers, the delay cells are implemented using current mode logic (CML) flip-flops, since the delay cells need only to operate on digital values coming from the slicer [40, 52, 53]. This simplification offers a signifi-

cant advantage over transversal equalizers, which need to operate with analog valued signals.

Because of the significant delay introduced by the slicer, it might be difficult to obtain a delay of T_b for the first delay cell. Therefore, the symbol at the output of the first delay cell, i.e. $\tilde{y}(n-1)$, might not be available when computing the current output $y(n)$. To overcome this limitation, look-ahead techniques have been proposed [52, 54, 55]. In such techniques, two parallel paths calculate the output of the slicer in the presence of both $\tilde{y}(n-1) = +1$ and $\tilde{y}(n-1) = -1$. The selection between this two tentative decisions is made once the previous data are known.

To find the optimum coefficients, the same algorithms of transversal equalizers described in subsection C.3 can be used.

A general description of the different types of equalizers has been presented. The following chapter discusses the details in the implementation of transversal equalizers.

CHAPTER VI

HIGH-SPEED CIRCUIT IMPLEMENTATIONS OF TRANSVERSAL EQUALIZERS AND PRACTICAL LIMITATIONS

The implementation of high-speed transversal equalizers requires dedicated analog or mixed-signal circuits for the unit delay cells, multipliers and summing node (recall the FIR structure shown in figure 1). In this chapter, different proposed topologies and their limitations will be explored. Also, the impact of noise on the bit error rate will be examined to determine the necessary signal-to-noise ratio in transversal equalizers.

A. Delay Lines: Implementations and Practical Limitations

The different implementations of delay cells, also called delay lines, can be classified into two categories: (1) sampled delay lines, and (2) continuous-time delay lines.

1. Sampled Delay Lines

Sampled delay lines can be implemented using unity-gain sample-and-hold (S&H) cells (see section A in chapter II). The disadvantage is that each S&H will introduce distortion and attenuation due to nonlinearity and clock feedthrough of the switches, and these will accumulate along the signal path. Furthermore, requirements on the gain-bandwidth product and slew rate of the amplifier, as well as switch resistance, limit the speed of operation to a few hundred MHz [56].

To avoid using a line of S&H cells in series, and the error accumulation associated with this technique, parallel samplers can be connected directly to the input (as shown in figure 43) sampling at a frequency of f_{clk}/N, where f_{clk} is the main clock frequency and N is the number of samplers in parallel and equal to the number of taps. The clock

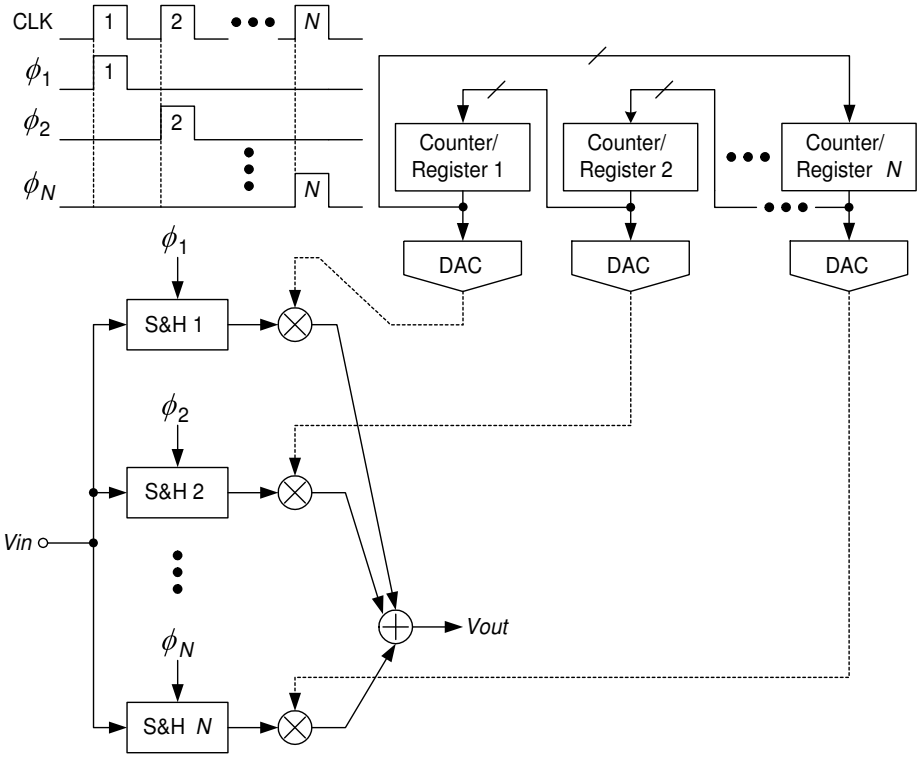


Fig. 43. Equalizer based on sampled delay lines and coefficient rotation.

of each sampler is delayed by $1/f_{clk}$. The effective sampling frequency of the array is f_{clk}. To implement the FIR's difference equation (see equation 1.2), it is necessary to rotate either the coefficients or the samples. In [57] and [58], the coefficients, stored in the digital domain, are rotated through parallel registers, and then converted to the analog domain with high-speed digital-to-analog converters (DAC), as shown in figure 43. Since the transfer of the coefficients, the digital-to-analog (D/A) conversion, and the multiplication with the corresponding sample $x(n-k)$ has to occur within less than one clock cycle $1/f_{clk}$, high power consumption is spent in the high-speed DACs. An alternative architecture uses a rotating switch matrix [56, 59]. The switch matrix connects the coefficients c_k to their corresponding sample $x(n-k)$. Because the number of switches in the matrix increases proportional to N^2 (N being the number of taps), this solution rapidly increases in complexity, layout area and crosstalk.

To alleviate the settling time requirements on the equalizer, time-interleaved FIR filters working at a slower sampling rate can also be used. In [60], 8 time-interleaved FIR filters working at $f_{clk}/8$ were implemented at the expense of increasing the layout area by a factor of 8.

2. Continuous-Time Delay Lines

For the implementation of high-speed equalizers (with speeds > 1Gbps), continuous-time delay lines have been recently proposed [33, 61, 62, 63]. Ideally, the delay line must have a transfer function such that

$$H(\omega) = A(\omega)e^{j\phi(\omega)} = e^{-j\omega T} \tag{6.1}$$

where $A(\omega)$ and $\phi(\omega)$ are the magnitude and phase response respectively of the delay line and T is the equivalent sampling period of the equalizer. Thus, the main challenges in the design of continuous-time delay lines are to have a constant group delay

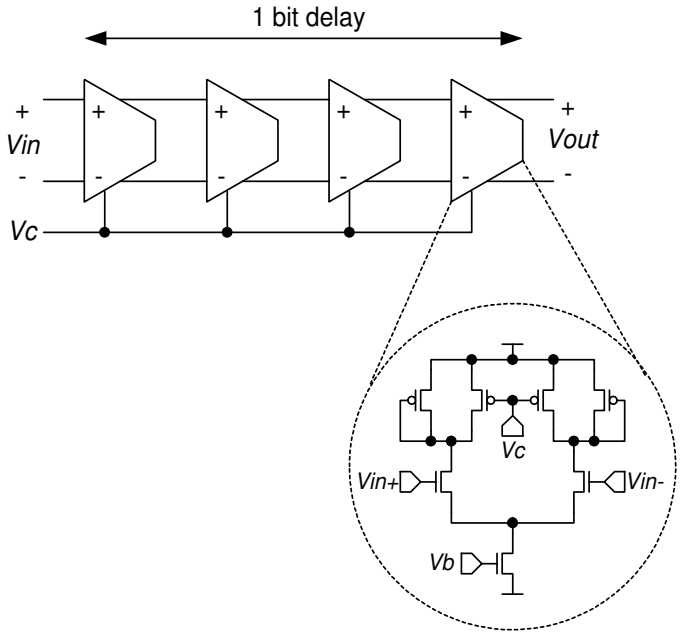


Fig. 44. Delay line implementation using four cascaded 1^{st} order sections.

(i.e. a linear phase given by $\phi(\omega) = -\omega T$) and a constant magnitude response $A(\omega)$ over a bandwidth of at least half of the symbol rate $f_b = 1/T_b$ (most of the frequency content of the data is confined to $f < f_b/2$), while keeping a low complexity in the implementation.

The delay lines proposed in [33] consist of four cascaded 1^{st} order sections, as shown in figure 44. The delay is controlled through V_c. The phase response of each 1^{st} order section is given by

$$\theta_1(\omega) = -\arctan\frac{\omega}{\omega_1} \tag{6.2}$$

where ω_1 is the location of the pole of each section determined by its output resistance

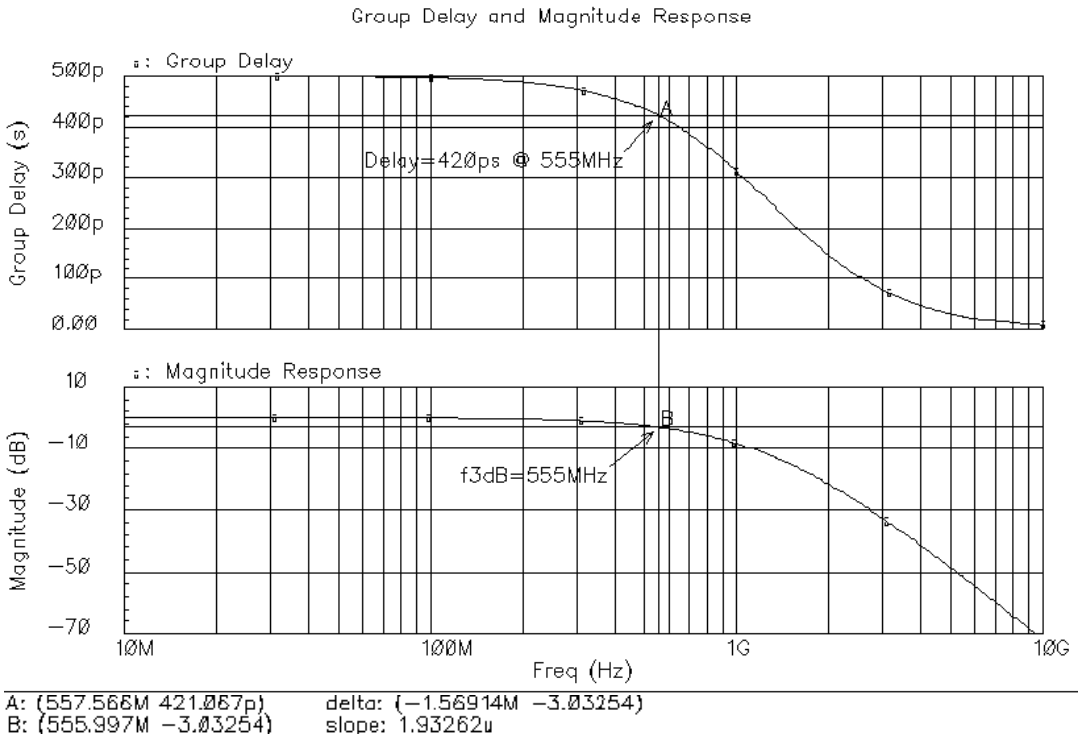


Fig. 45. Group delay and magnitude response of four cascaded 1^{st} order sections.

and load capacitance. The group delay is

$$\tau_1(\omega) = -\frac{\partial\theta}{\partial\omega} = \frac{1}{\omega_1}\,\frac{1}{1+(\omega/\omega_1)^2} \tag{6.3}$$

For the four cascaded stages, the total group delay is given by

$$\tau(\omega) = \frac{4}{\omega_1}\,\frac{1}{1+(\omega/\omega_1)^2} \tag{6.4}$$

Therefore, the group delay at low frequencies is approximately $4/\omega_1$. Notice that tuning the delay line to increase the group delay (smaller ω_1) decreases the 3dB bandwidth. This is a design challenge in the implementation of transversal equalizers for broadband systems, where both a large delay and a wide bandwidth are required.

The group delay and magnitude response for this delay line were simulated in

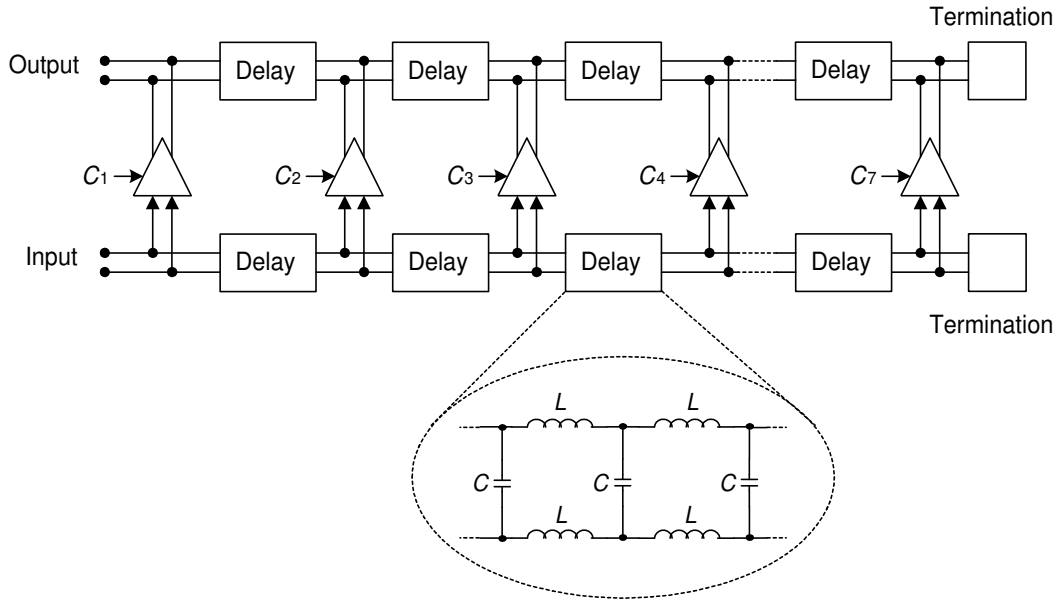


Fig. 46. Delay lines using artificially emulated transmission lines.

Cadence; the results are shown in figure 45 for a nominal delay of 500ps. The group delay has a variation of 16% within the 3dB bandwidth of 555MHz.

In [61], the delay lines were implemented by artificially emulating transmission lines with cascaded LC sections using passive on-chip inductors, as shown in figure 46. Recall from eq. (5.4) in chapter V, section B, that the phase in an ideal transmission line is quasi-linear and therefore the group delay is practically constant for all frequencies. Because of the large group delay required in transversal equalizer working at 10Gbps or below, physical transmission lines would result in impractical lengths for on-chip implementation. Transmission line (T.L.) emulation using lumped elements offer a practical alternative. Notice that for this emulation, the inductors and capacitors are chosen such that $Z_o = \sqrt{L/C}$, where Z_o is the termination impedance.

The group delay and magnitude response of these delay lines simulated in Cadence are shown in figure 47 ($L = 1.9$nH, $C = 340$fF and $Z_o = 75\Omega$). The delay was

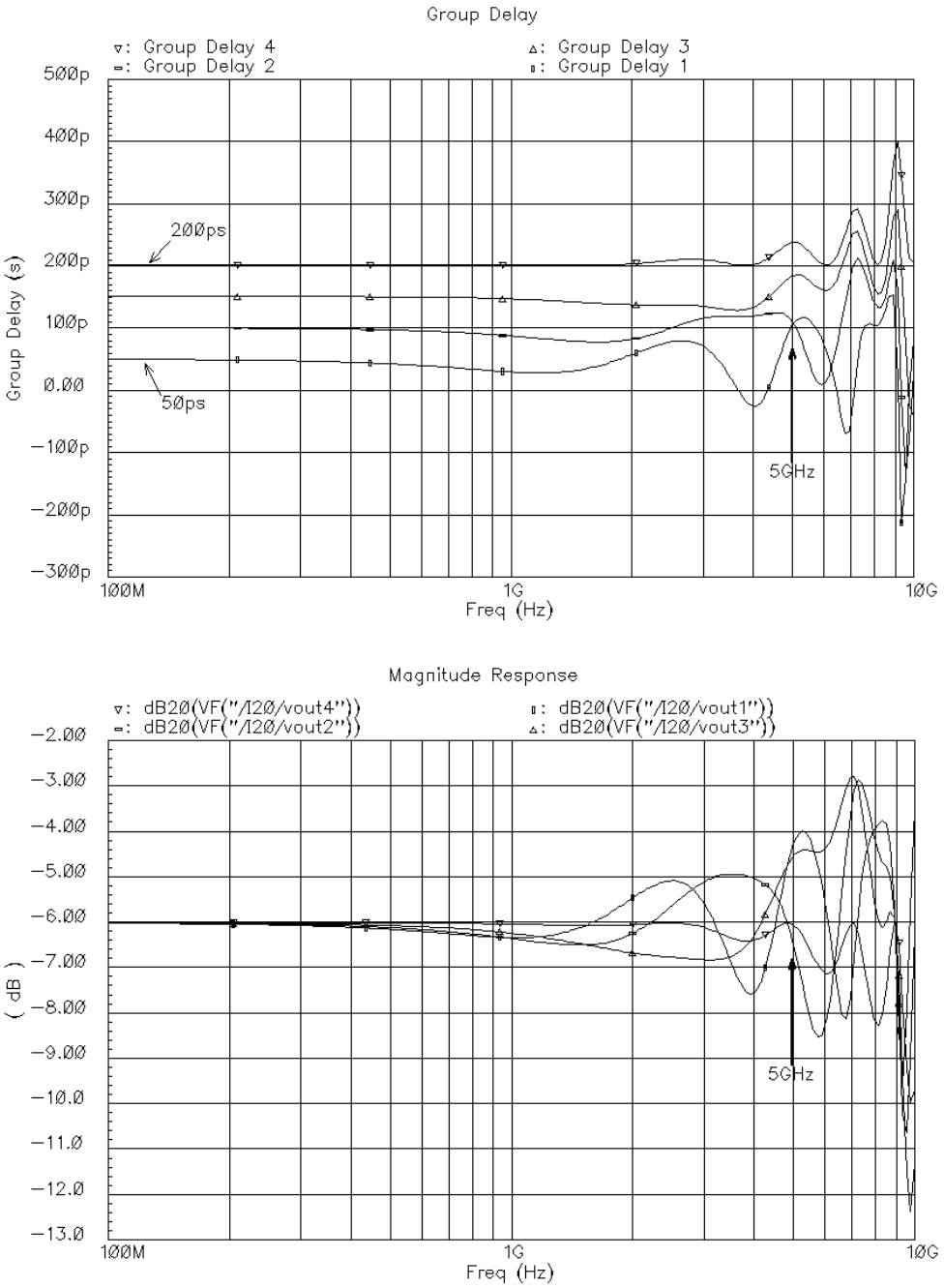


Fig. 47. Group delay and magnitude response of artificially emulated T.L.

tuned to 50ps in [61] for a FSE for 10Gbps optical communications. Therefore, most of the frequency content is within a bandwidth of 5GHz. The plots show the response for each of the first 4 delay cells along the emulated transmission line in figure 46. In other words, the plots show delays of 50, 100, 150 and 200ps. It can be observed that the group delay has large variations within 5GHz, and so does the magnitude response. The first delay cells are the ones that show more ripple (in both group delay and magnitude). This is due to the fact that a more constant group delay and magnitude response is achieved when the number of LC sections emulating the T.L. increases (i.e. tends to infinity). On the other hand, if a linear phase filter is desired with a finite number of inductors and capacitors, the optimum design does not yield all the capacitors and inductors to be of the same value [64]. This will be further addressed in chapter VII.

Because of the large size and number of on-chip inductors, this technique is not area efficient for equalizers working at speeds <10Gbps. In [62], a delay line based on a first-order approximation of e^{-sT} was presented. The transfer function implementing a constant group delay of T seconds was approximated as:

$$H(s) = e^{sT} \approx \frac{1 - sT/2}{1 + sT/2} \tag{6.5}$$

The circuit implementation is shown in figure 48. If the circuit is designed to have a unity DC gain, then

$$\frac{g_m R_c}{1 + g_m R_e} = 1 \tag{6.6}$$

and

$$H(s) = \frac{1 - sC_t R_c}{1 + sC_t R_c} \tag{6.7}$$

The simulated group delay is shown in figure 49. The circuit was tuned for a group delay of 400ps. The delay line has a group delay variation of more than

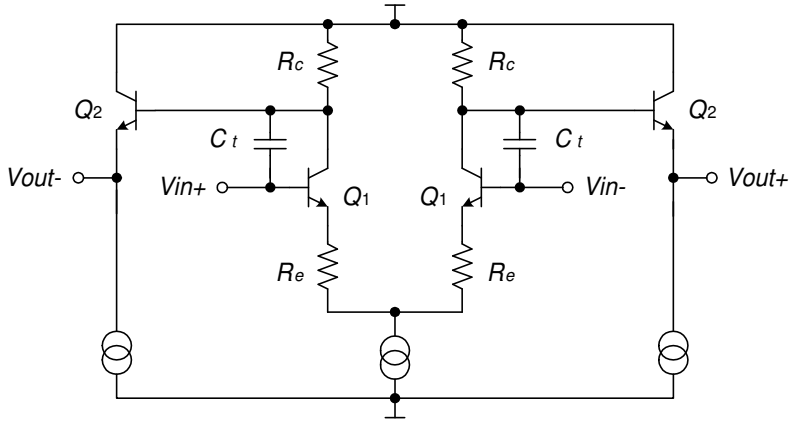


Fig. 48. First-order approximation of e^{-sT}.

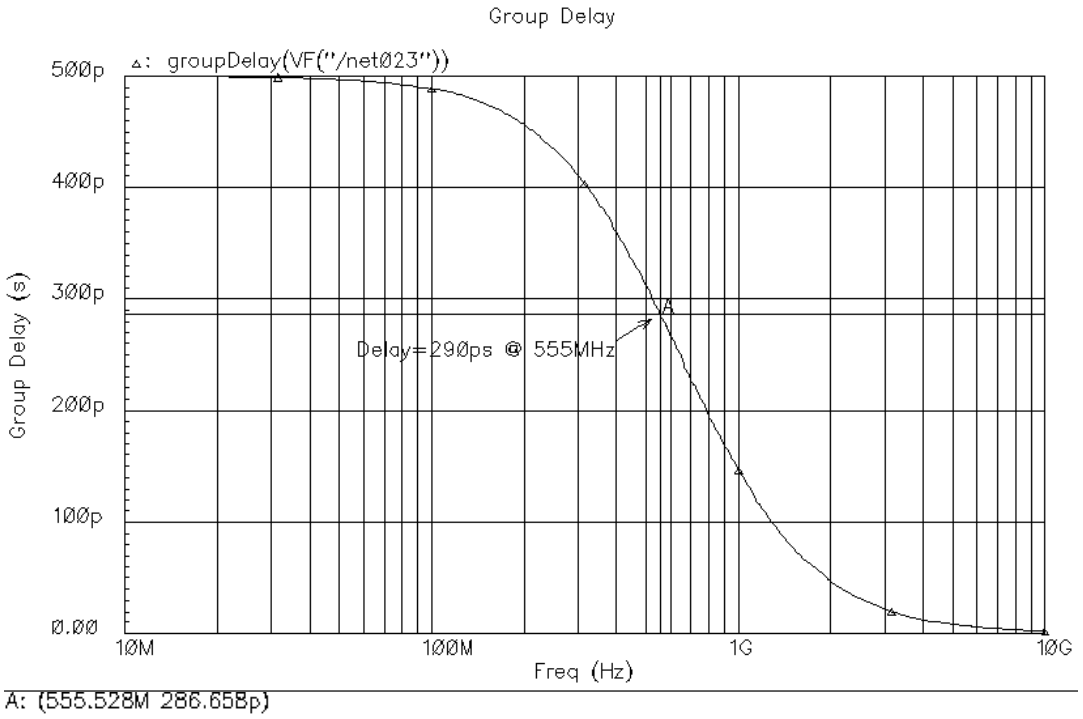


Fig. 49. Group delay of a first-order approximation of e^{-sT}.

42% within 555MHz, which is a worse performance than the one in [33] previously discussed.

A second-order delay line was proposed in [63] using a current-mode biquad. The transfer function given by

$$H(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{6.8}$$

where Q is the quality factor and ω_0 is the poles' frequency, has a phase response of

$$\theta(\omega) = -\arctan\left(\frac{\frac{\omega}{\omega_0}\frac{1}{Q}}{1-\left(\frac{\omega}{\omega_0}\right)^2}\right) \tag{6.9}$$

and a group delay given by

$$\tau(\omega) = \frac{1}{\omega_0}\eta \tag{6.10}$$

where $\eta = (\partial/\partial x)\left(\arctan\left((x/Q)/(1-x^2)\right)\right)$ and $x = \omega/\omega_0$. To have a flat group delay Q must have a value between 0.5 to 0.8 [63]. Second-order delay lines will be further discussed in chapter VII.

B. Multiplication and Addition in the Analog Domain: Practical Limitations

In transversal equalizers, the delayed signals are multiplied by the filter coefficients c_i and then added, as shown in figure 50(a). The multiplication by the coefficients in high-speed transversal equalizers is typically carried out using variable gain amplifiers [33], MDACs (multiplying digital-to-analog converters) [63], or four-quadrant analog multipliers (Gilbert cells) [61]. A typical CMOS Gilbert cell is shown in figure 50(b).

To realize the addition operation, the outputs of the multipliers are connected together to a summing node, since the Gilbert cell's output is a current. The output currents of each multiplier add together and the result is translated into a voltage

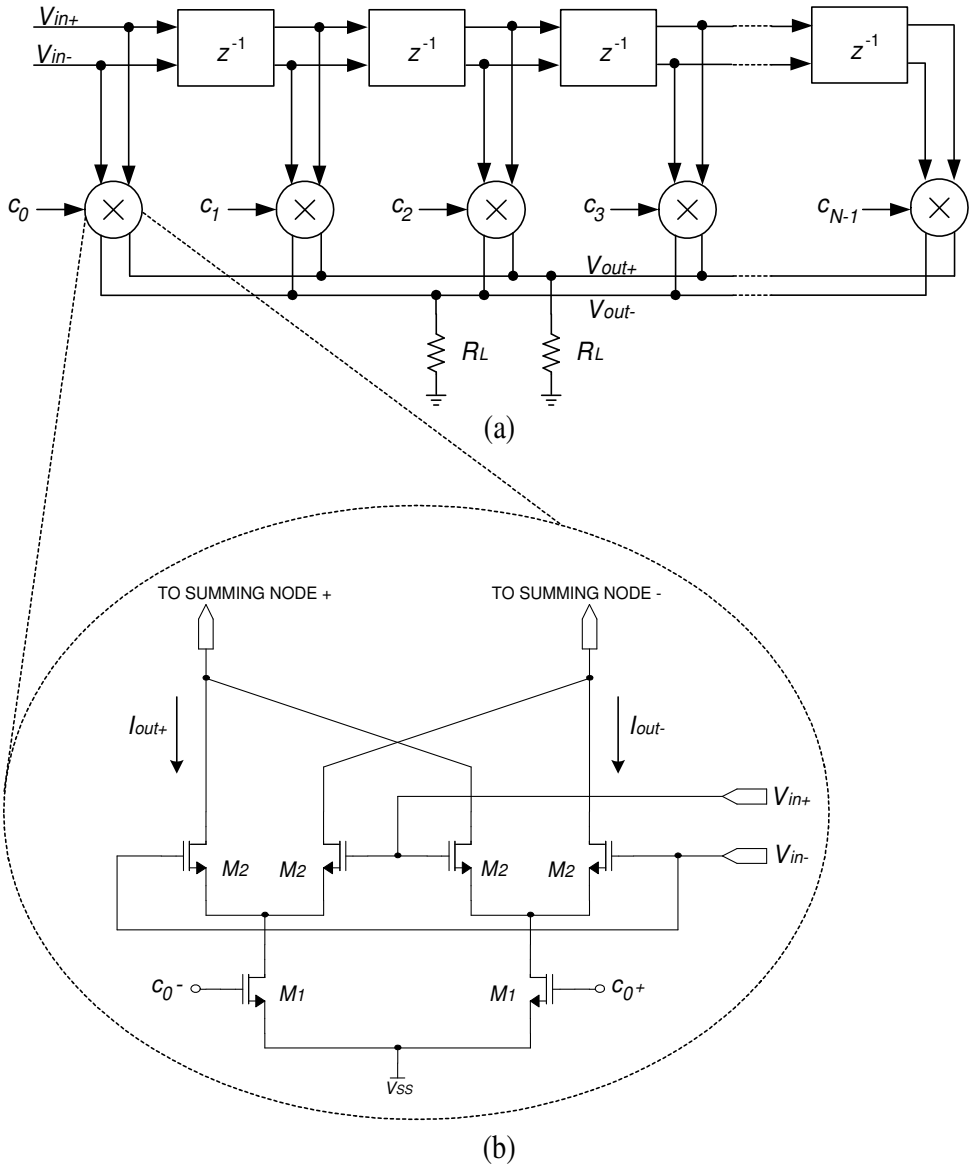


Fig. 50. (a) Transversal equalizer with resistive load and (b) a four-quadrant analog multiplier.

through a load resistor (R_L) as shown in figure 50(a).

In practice, the parasitic capacitance in the summing node limits the bandwidth and therefore the speed of operation of the equalizer. For the CMOS equalizer shown in figure 50, the pole's location at the summing node is given by

$$\omega_L = \frac{1}{R_L \cdot \sum C_p} \tag{6.11}$$

where $\sum C_p$ is the sum of all the parasitic capacitances lumped to the summing node. Since the parasitic capacitance increases with the number of multipliers used, the required bandwidth imposes a limitation in the number of taps for the equalizer.

The gain of the equalizer without boosting, obtained as the ratio between the output and the input when the coefficients are

$$\mathbf{C} = \begin{bmatrix} c_0 \neq 0 \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix}$$

in other words, when all of the coefficients are 0 except for c_0, the equalizer's gain is given by

$$\frac{V_{out}}{V_{in}} = g_{mc}\, R_L \tag{6.12}$$

where g_{mc} is the transconductance of the multiplier driven by the coefficient c_0. Thus, the choice of R_L results in a trade-off between gain and bandwidth. As an example, in CMOS 0.35μm technology, the 3dB bandwidth of a 5-tap CMOS equalizer, driving a parasitic capacitance of 580fF, is only 275MHz if a gain of 0dB is desired with g_{mc} = 1mA and R_L = 1kΩ. The bandwidth can be extended to 550MHz if the value of R_L is decreased to 500Ω, but results in a gain drop of 6dB. To improve the

bandwidth without further degrading the gain, two high-speed summing nodes will be presented in chapter VII.

C. Signal-to-Noise Ratio Considerations

While increasing the vertical eye opening and reducing the jitter, equalizers must also provide adequate signal-to-noise ratio to achieve a given bit error rate (BER). The noise introduced by the equalizer might degrade the eye opening thus increasing the BER. To this end, we need to analyze the effect of noise $n(t)$ on random binary data.

Assuming additive white gaussian noise with zero mean, and that "1"s correspond to $+V_o$ and "0"s correspond to $-V_o$, the probability of error or bit error rate is given by [7]

$$\begin{aligned} \text{BER} = P_{total} &= P(1|0) + P(0|1) \\ &= \frac{1}{2}\int_0^\infty \frac{1}{\sigma_n\sqrt{2\pi}} \exp\frac{-(x+V_o)^2}{2\sigma_n^2}\,dx \\ &\quad + \frac{1}{2}\int_{-\infty}^0 \frac{1}{\sigma_n\sqrt{2\pi}} \exp\frac{-(x-V_o)^2}{2\sigma_n^2}\,dx \\ &= Q\left(\frac{V_o}{\sigma_n}\right) \end{aligned} \tag{6.13}$$

where $P(1|0)$ and $P(0|1)$ are the probabilities of the slicer deciding that a "1" was received when actually a "0" was transmitted and vice-versa. $Q(x)$ is the so-called Q-function defined as

$$Q(x) = \int_x^\infty \frac{1}{\sqrt{2\pi}} \exp\frac{-v^2}{2}\,dv \tag{6.14}$$

The standard deviation σ_n is the rms value of the noise.

For a vertical eye opening (in Volts) at the equalizer's output of $V_m = 2V_o$, the bit error rate is given by

$$\text{BER} = Q\left(\frac{V_m}{2\sigma_n}\right) \tag{6.15}$$

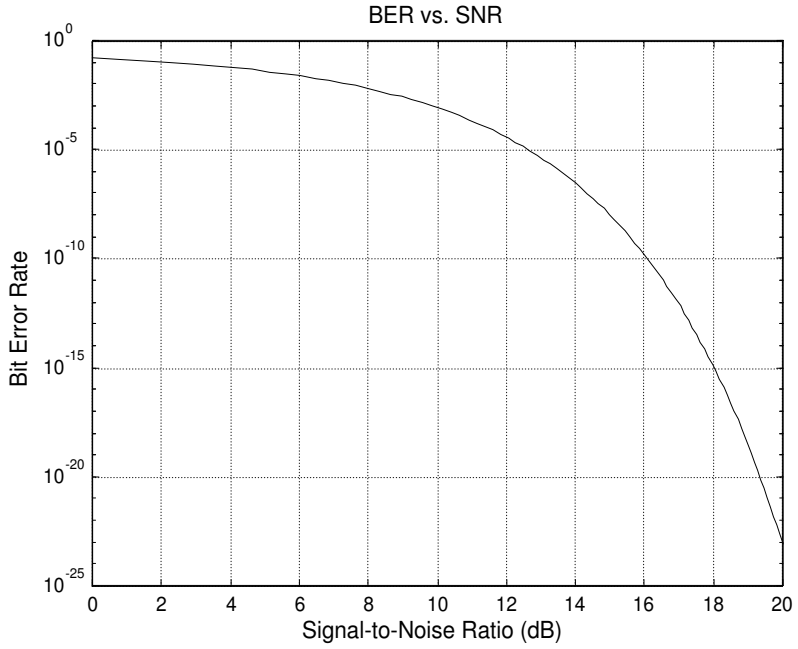


Fig. 51. Bit error rate vs. signal to noise ratio.

Defining the output signal-to-noise ratio as $\text{SNR}_{out} = \dfrac{V_m}{2\sigma_n}$, figure 51 shows the BER vs. SNR_{out}. This plot will be used in chapter VII to estimate the BER from eye-pattern diagrams obtained through simulations.

CHAPTER VII

A 1 GB/S 5-TAP TRANSVERSAL EQUALIZER IN CMOS 0.35μm

As discussed in the previous chapter, the design of high-speed transversal equalizers requires the implementation of broadband delay lines. In this chapter, a delay line based on a third-order linear-phase filter is presented for the implementation of a fractionally-spaced 1Gb/s transversal equalizer. The delay lines are tuned for a group delay of 500ps, offering an approximately constant group delay over a 3dB bandwidth greater than 600MHz. Furthermore, two different topologies for a broadband summing node which enable the placement of the parasitic poles at the output of the transversal equalizer beyond 650MHz are presented. Using these cells, a 5-tap 1Gb/s equalizer was implemented in TSMC 0.35μm CMOS technology. The results show a programmable frequency response able to compensate up to 25dB loss at 500MHz for a 1Gb/s binary data stream. The eye-pattern diagrams at 1Gb/s demonstrate the equalization of 15 meters and 23 meters of CAT5e twisted-pair cable. The equalizer consumes 96mW and an area of 630μm $\times$ 490μm.

A. Proposed Active Delay Lines

For the implementation of a T/2 fractionally-spaced equalizer at 1Gb/s, the delay lines must have a group delay of 500ps $= 1/(2 \cdot 1\text{GHz})$. In other words, the equalizer works at an equivalent sampling rate of 2 GHz. Since most of the spectrum of the bit stream is contained within 0-500MHz, the 3dB bandwidth of the delay lines must be higher than 500MHz. To obtain a flat group delay in the passband, the design of the delay lines can be approached as a linear-phase filter.

1. Third-Order Linear-Phase Low-Pass Filter: Current-to-Voltage

The group delay characteristics for linear-phase filters with equiripple error of 0.05° are shown in figure 52. The magnitude response is shown in figure 53. Both are plotted versus a normalized frequency of 1 rad/sec and for various filter orders n [64]. Linear-phase filters with equiripple error of 0.05° are chosen since they provide a more linear phase and therefore a flatter group delay over a wider bandwidth when compared to other filter approximations such as Butterworth, nonlinear-phase Chebyshev, and Elliptic[1]. From figure 52, it can be observed that in order to have a flat group delay in the passband (normalized to 1 rad/sec), at least a third-order filter ($n = 3$) is required. Furthermore, increasing the order of the filter allows for a larger delay while keeping the same 3dB bandwidth. Nevertheless, the complexity has to be kept to a minimum to allow a feasible implementation. From figure 52, it can also be determined that for a third-order linear-phase filter implementing a delay line of 500ps, the resulting 3dB bandwidth is

$$\omega_{3dB} = \frac{1.8\text{s}}{500\text{ps}} \times 1\text{rad/s} = 3.6\text{Grad/s}$$

or equivalently $f_{3dB} = 573$MHz. As a comparison, a second-order delay line with the same delay would have a bandwidth of $f_{3dB} = 440$MHz, while a first-order delay line would result in $f_{3dB} = 318$MHz. On the other hand, a higher-order delay line allows for a wider bandwidth for a given group delay requirement, but the complexity increases.

The normalized pole locations are: $s_{1,2} = 0.8541 \pm j1.0725, s_3 = 1.0459$. The complex poles have a Q of 0.8. Two LC ladder prototype filters are shown in figures 54 and 55 [64]. The first one has a voltage as the input, and requires two floating

[1] A Bessel maximally flat delay approximation gives similar results to the linear-phase filter with equiripple error of 0.05° for a third-order filter [64].

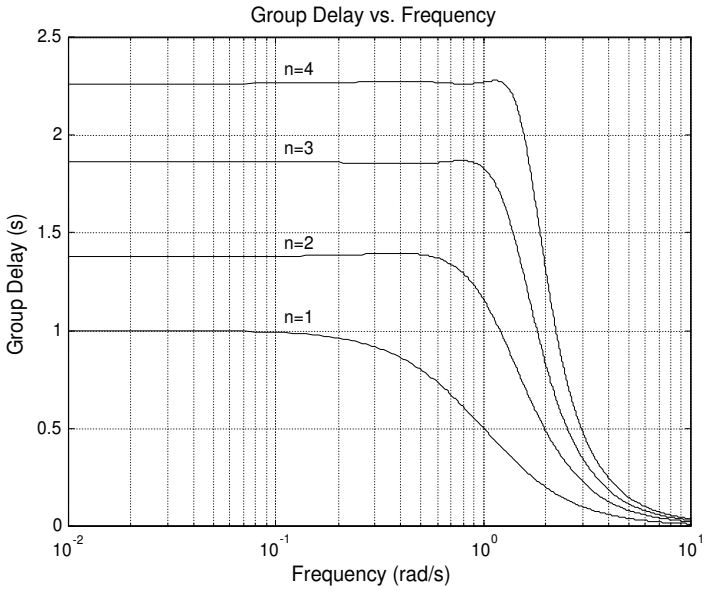


Fig. 52. Normalized group delay characteristics for linear-phase filters with equiripple error of 0.05°.

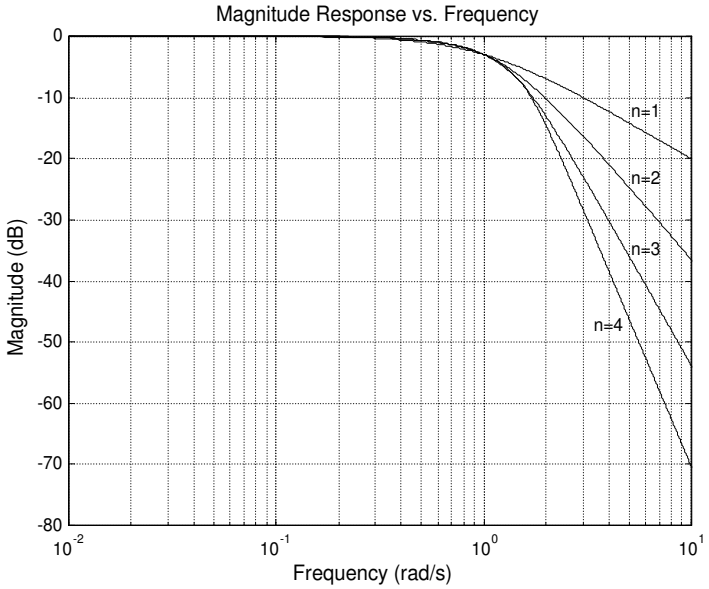


Fig. 53. Normalized magnitude response for linear-phase filters with equiripple error of 0.05°.

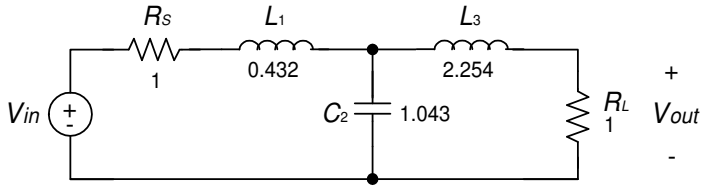


Fig. 54. Voltage-driven LC ladder prototype.

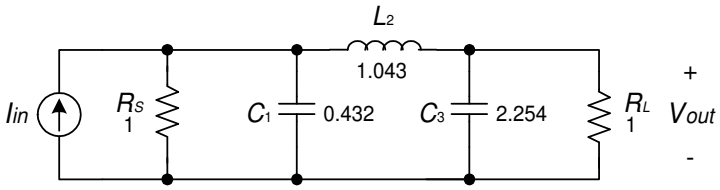


Fig. 55. Current-driven LC ladder prototype.

inductors. The second one is a current-driven topology, and requires only one floating inductor. It is important to reduce the number of inductors, either if implemented by on-chip inductors which occupy large silicon area, or if emulated using active circuitry which requires additional power consumption. Therefore, the current-driven prototype is better suited for on-chip realizations.

The component values for a delay line of 500ps are shown in table VI.

2. OTA-C Filter Implementation with Inductive Emulation

The proposed OTA-C implementation of the third-order delay line is shown in figure 56. The component values (transconductances and capacitors) are shown in table VII.

The input is fed directly to an OTA (denoted by g_{m0}) to generate the input current, as required in fig. 55. The transistor level schematic for this OTA is shown

Table VI. Component values for a delay line of 500ps.

Component Name	**Value**
R_S	500Ω
C_1	240fF
L_2	145nH
C_3	1.25pF
R_L	500Ω

in figure 57. The transistors' sizes were optimized for a low input capacitance of the delay line ($<$ 200fF).

Because of the large area that the 146nH floating inductors would occupy, inductive emulation with an active impedance inverter is used, as shown in fig. 56. The equivalent inductance is given by

$$L_2 = \frac{C_2}{g_{m1}g_{m2}} \tag{7.1}$$

The transistor level schematics of the amplifiers used in the emulation of the inductors are shown in figure 58. Notice that one of the amplifiers (fig. 58(b)) also implements the active loads $R_S = R_L = 1/g_{m3}$ by re-using the current of g_{m2}, therefore saving on power consumption while providing tunability on the values of R_S and R_L. Additionally, these low impedance nodes do not require a common-mode feedback circuit. Only one CMFB circuit is needed for the complete delay line.

The gain is adjusted by I_{bias1}, while the group delay is controlled by I_{bias2}. Since the transconductance is proportional to the square root of the bias current, increasing

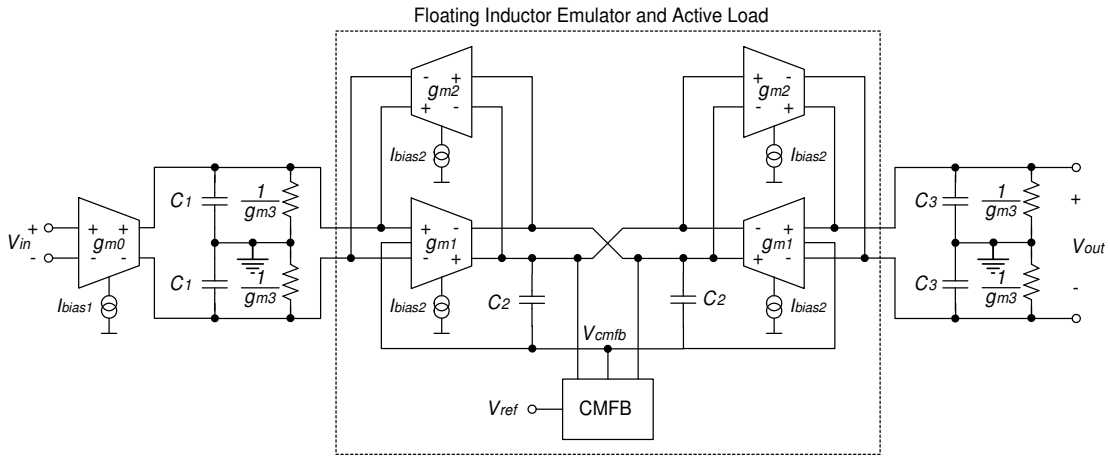


Fig. 56. Proposed OTA-C implementation of a third-order delay line.

Table VII. Component values for the OTA-C delay line.

Component Name	**Value**
g_{m0}	4mA/V
g_{m1}, g_{m2}	1.5mA/V
g_{m3}	2mA/V
C_1	240fF
C_2	330fF
C_3	1.25pF

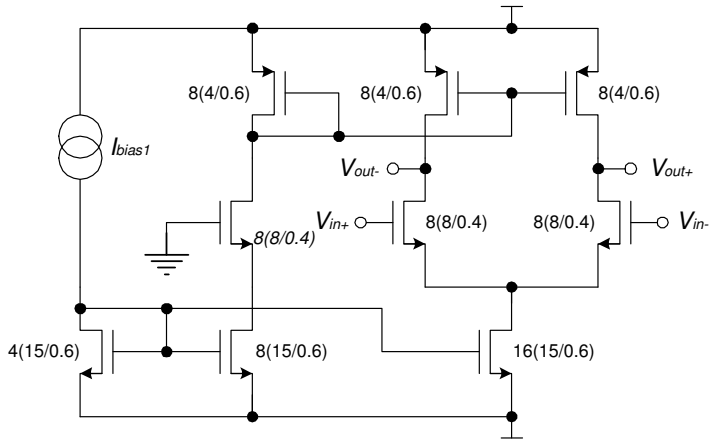


Fig. 57. Transistor level schematic of the input OTA: g_{m0}.

I_{bias2} by a factor k corresponds to a frequency scaling of $k_F = \sqrt{k}$ and an impedance scaling of $k_I = 1/\sqrt{k}$. Thus, the flatness of the group delay in the passband is, in a first-order approximation, not modified when the delay line is tuned by changing the bias currents.

The layout of the proposed delay line implemented in CMOS 0.35μm technology is shown in figure 59. It occupies an area of 165μm$\times$225μm. The simulation results are presented in the next section.

3. Simulation Results

A comparison between the group delay of a third-order linear-phase delay line versus previously proposed delay lines (4 cascaded 1^{st} order sections [33], Emulated T. L. [61], 1^{st} order all-pass approximation [62], and 2^{nd} order low-pass [63]) is shown in figure 60. All delay lines have been tuned for a group delay of 500ps, needed for a 1Gb/s T/2 fractionally-spaced equalizer. In this plot, ideal components have been used in all cases. The third-order linear-phase topology outperforms the rest, keeping

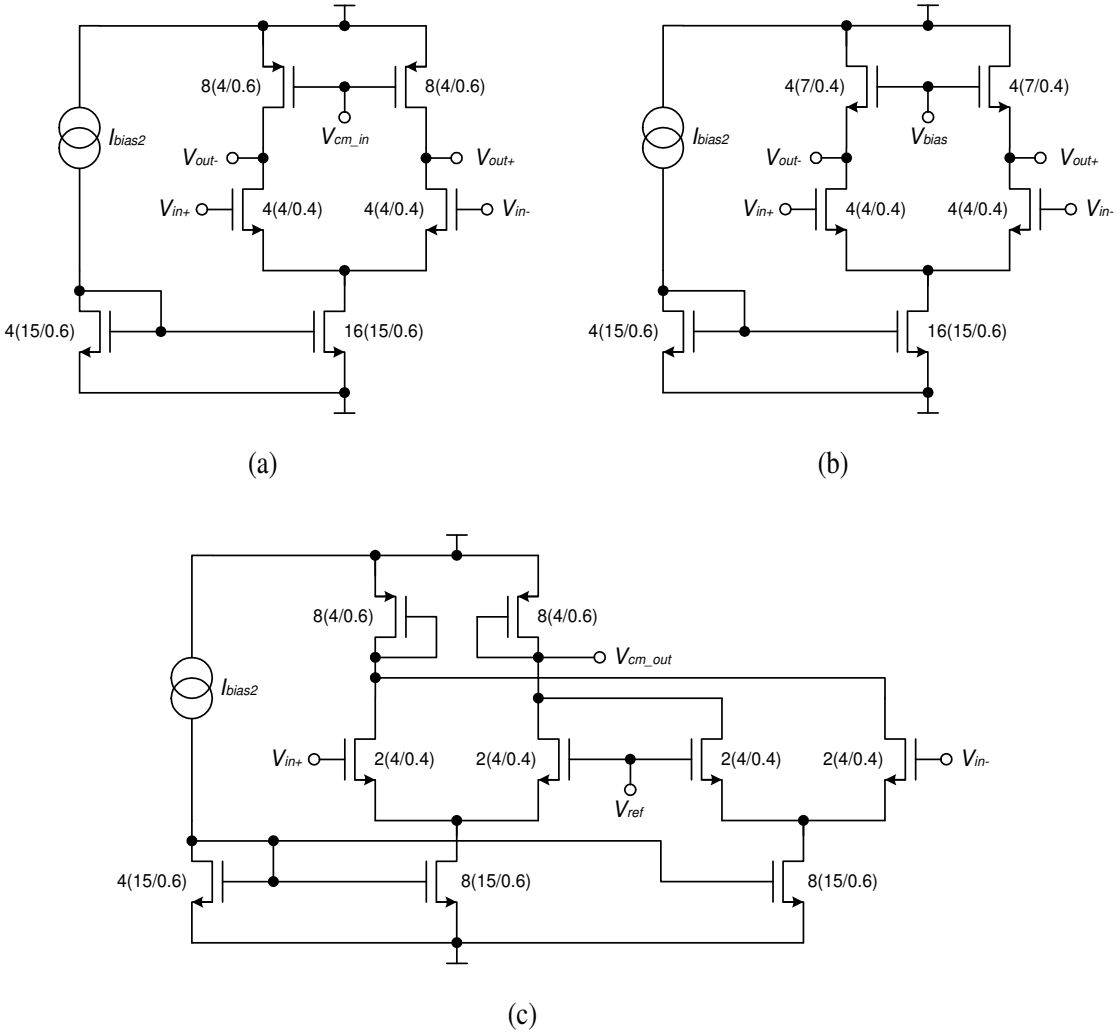


Fig. 58. Transistor level schematics of the amplifiers in the inductor emulator. (a) g_{m1}, (b) g_{m2} with an active load of $1/g_{m3}$, and (c) CMFB.

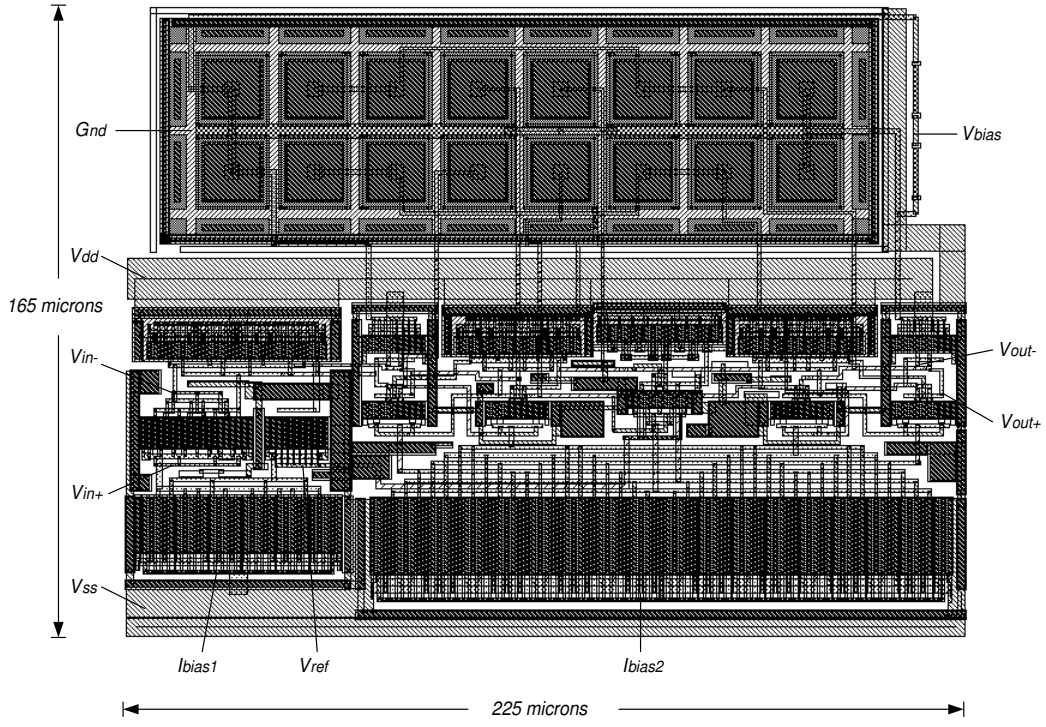


Fig. 59. Layout of the proposed delay line.

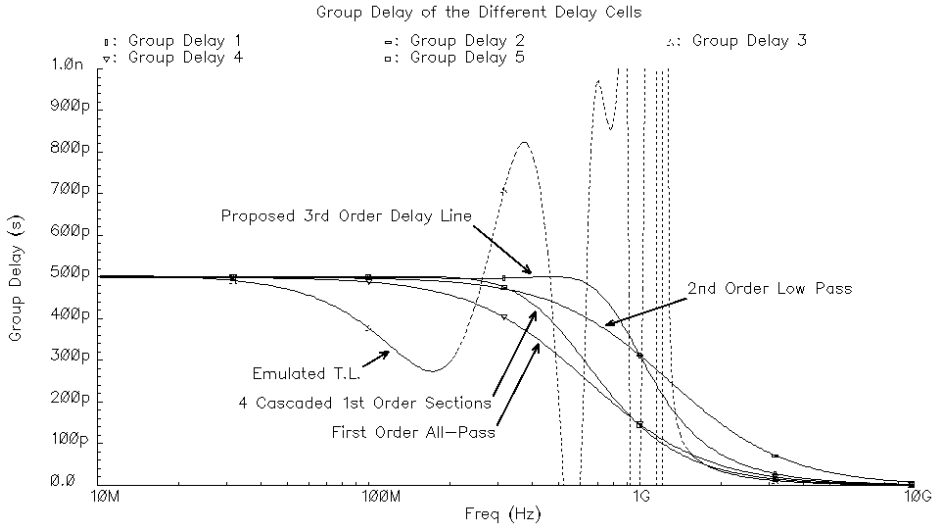


Fig. 60. Comparison between the group delay of different delay cells.

a flat group delay up to 600MHz. Recall that most of the frequency content is within 0-500MHz, and the previously proposed delay lines do not keep a constant group delay in all this bandwidth.

The magnitude response and group delay of the transistor level implementation of the proposed OTA-C delay line in CMOS 0.35μm technology is shown in figure 61. Even with the additional parasitic capacitances of the active devices and layout interconnects, the group delay varies less than 8% from 0 to 610MHz, which is the simulated 3dB bandwidth.

By varying I_{bias2} from 390μA to 140μA, the group delay can be tuned from 420ps to 580ps as shown in figure 62, and can be used to compensate for process variations. As mentioned before, the flatness of the group delay versus frequency is kept approximately the same regardless of I_{bias1} and I_{bias2}. The low frequency group delay versus I_{bias2} is shown in figure 63.

The step response is shown in figure 64. The linear phase of the delay line results

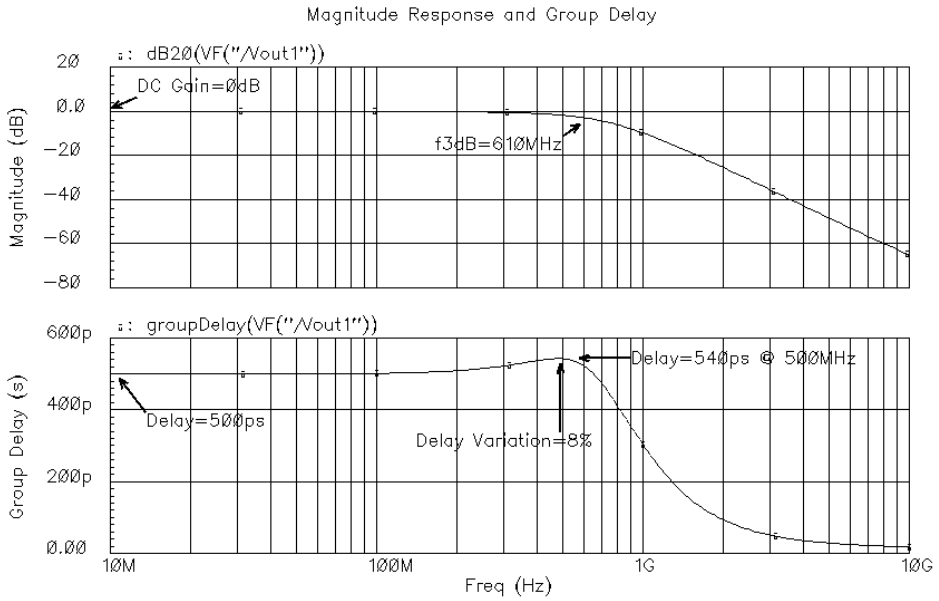


Fig. 61. Simulated magnitude and group delay of the designed OTA-C delay line.

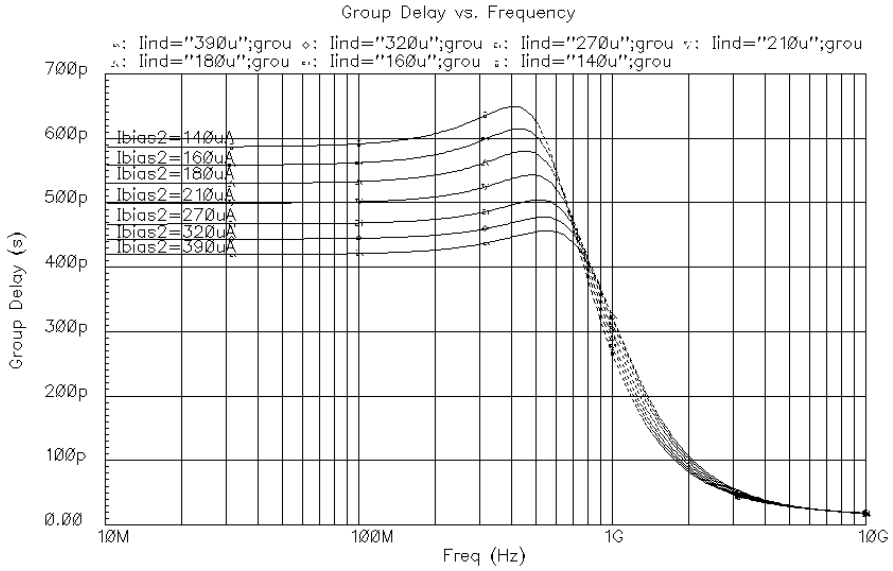


Fig. 62. Simulated group delay vs. frequency for various values of I_{bias2}.

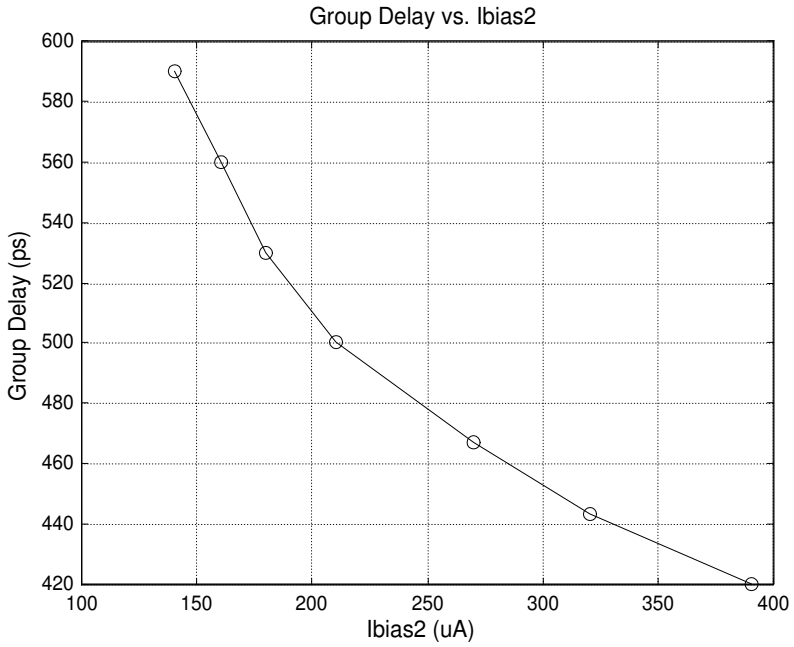


Fig. 63. Low frequency group delay vs. I_{bias2}.

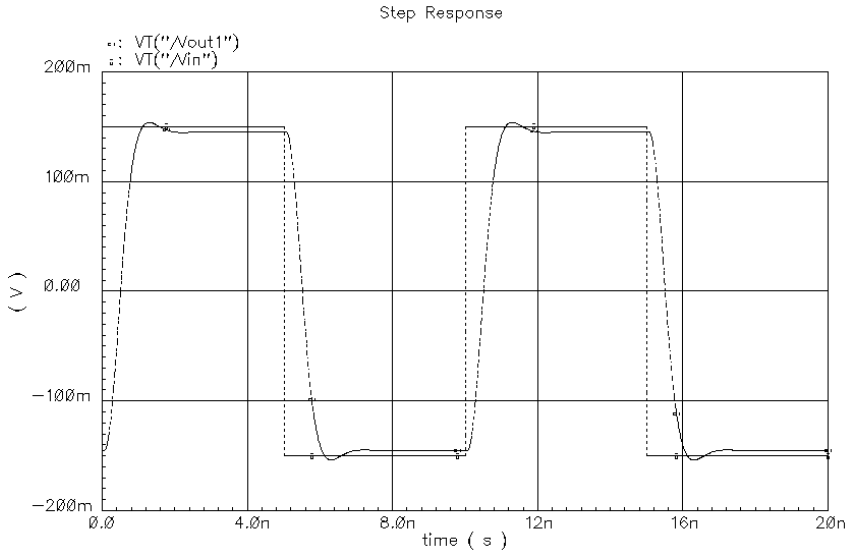


Fig. 64. Step response of the designed OTA-C delay line ($I_{bias2} = 210\mu$A).

in an undistorted pulse, which shows fall and rise times of less than 1ns.

The delay line was optimized for an ECL compatible voltage input swing of 300mV_{pp}. The simulated third-order harmonic distortion for such input amplitude is -36dB, which was found to be sufficiently small not to impact the eye opening when used in the complete equalizer. The simulated input referred noise is $136\mu\text{V}_{\text{rms}}$. For a 300mV_{pp} input signal, this corresponds to a signal-to-noise ratio of 61dB. (recall definition in chapter VI section C).

The proposed delay line consumes a power of 16.8mW (Supply = $\pm$1.5V) when tuned for a group delay of 500ps.

B. Proposed High-Speed Summing Nodes

In the implementation of high-speed equalizers, equations 6.11 and 6.12 showed that there is a trade-off between bandwidth and gain. In the following subsections, two high-speed summing nodes will be presented. Both are based on increasing the frequency of the pole present in the summing node, thus improving the bandwidth, while avoiding a degradation in the gain.

1. Cascode Summing Node

Consider the 5-tap structure depicted in figure 65. Instead of transforming the output current into a voltage using a resistor as discussed in chapter VI, the speed of the summing node can be improved by simply using a cascode configuration [57, 60]. The proposed summing node is depicted in figure 66. The output of the five multipliers is connected to the source of the cascode transistors M_3, which provides an equivalent input resistance of

$$R_{in} = \frac{R_L}{(g_{m3} + g_{mb3})\, r_{ds3}} + \frac{1}{g_{m3} + g_{mb3}} \approx \frac{1}{g_{m3} + g_{mb3}} \tag{7.2}$$

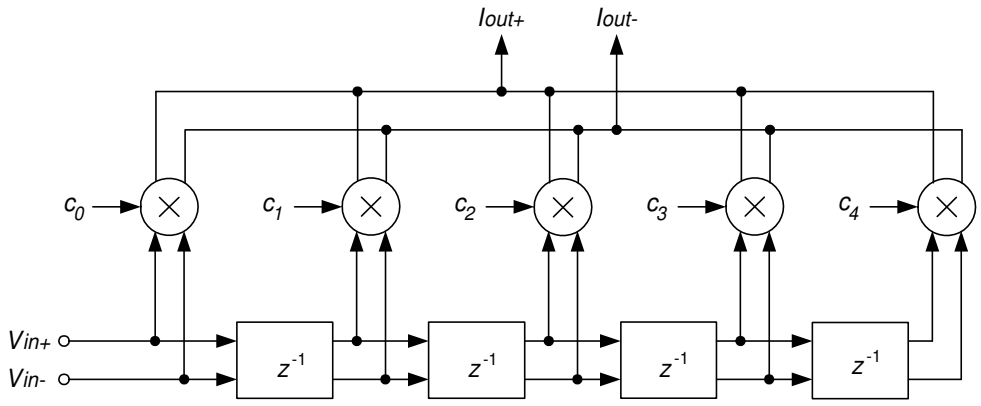


Fig. 65. 5-tap equalizer structure.

where g_{mb3} is the additional transconductance due to the body effect, and r_{ds3} is the output resistance of M_3 due to channel-length modulation. Because of the low equivalent resistance, the pole can be placed at high frequencies as long as the additional gate-source capacitance of transistors M_3 and drain capacitance of transistors M_5 are kept reasonably smaller compared to the other parasitic capacitances in this node.

The current injected into the source of M_3 is converted to the output voltage by R_L at the drain of M_3 and M_4, where the parasitic capacitance, $C_{p,out} = C_{db3} + C_{gd3} + C_{db4} + C_{gd4}$, is smaller than the parasitic capacitance due to the 5 multipliers, thus obtaining a wider bandwidth for the same gain, which is again given by equation 6.12. The two poles of the cascode summing node are approximately given by $\omega_1 \approx g_{m3}/(C_{p,mult} + C_{gs3})$ and $\omega_2 \approx 1/\left(R_L\left(C_{p,out} + C_L\right)\right)$, where $C_{p,mult}$ is the parasitic capacitance due to the multipliers and C_L is the load capacitance of next stage.

In terms of DC bias, let's now consider the multipliers as previously shown in figure 50. Notice that the bias current of the five multipliers must go through the summing node of figure 66. Thus, one of the advantages of the cascode summing node is that it does not require additional current other than the one already used

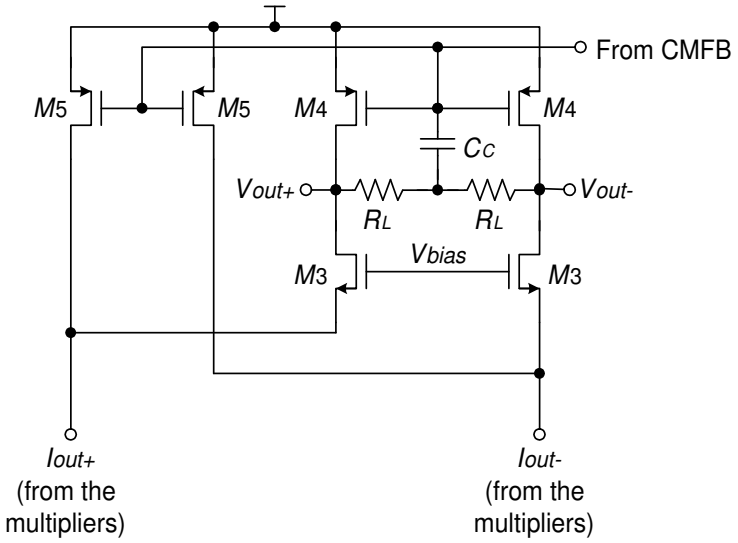


Fig. 66. Proposed cascode summing node.

by the multipliers. Transistors M_5 provide an alternate path to avoid large currents through M_3 and M_4, which would result in headroom problems due to large values of V_{GS3} and V_{DSAT4}. The ratio between M_5 and M_4 determines how much current is deviated to this alternate path. Finally, capacitor C_C is optional and can be placed for compensation of the common-mode feedback circuit if required.

The component values of the proposed cascode summing node implemented in CMOS 0.35μm technology are shown in table VIII. The simulation results are presented in section B.3.

2. Transimpedance Summing Node

A high-speed summing node can also be designed using the principle behind the Cherry-Hooper amplifier, commonly used in high-speed limiting amplifiers [7]. To achieve a wide bandwidth, the Cherry-Hooper amplifiers uses a transconductance stage followed by a transimpedance amplifier [65].

Table VIII. Component values for the cascode summing node.

Component Name	**Value**
R_L	1kΩ
M_3	6 (8μm/0.4μm)
M_4	16 (4μm/0.4μm)
M_5	38 (4μm/0.4μm)

The proposed transimpedance summing node is shown in figure 67. Resistors R_1 provide a feedback path for transistors M_3 to implement a transimpedance amplifier. Resistors R_2 bias the gate of transistors M_4 and M_5 without requiring an additional common-mode feedback circuit, thus saving power consumption. The transconductors are provided by the four-quadrant multipliers in the equalizer; their output current being injected as depicted in figure 67.

For AC analysis, we can draw the small-signal equivalent circuit of the transimpedance summing node as shown in figure 68.

The equivalent input resistance is given by

$$R_{in} = \frac{R_1 + R_Y}{1 + g_{m3} R_Y} \parallel R_X \tag{7.3}$$

where $R_X = R_2 \parallel r_{ds5}$ and $R_Y = R_2 \parallel r_{ds3} \parallel r_{ds4}$. The transimpedance gain of the summing node, i.e. the ratio between the output voltage V_{out} and the output current

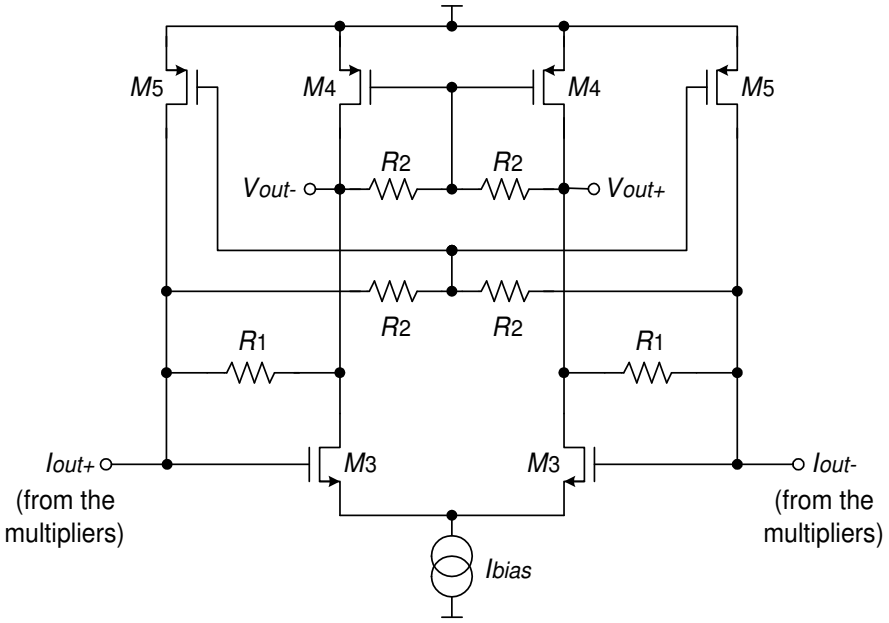


Fig. 67. Proposed transimpedance summing node.

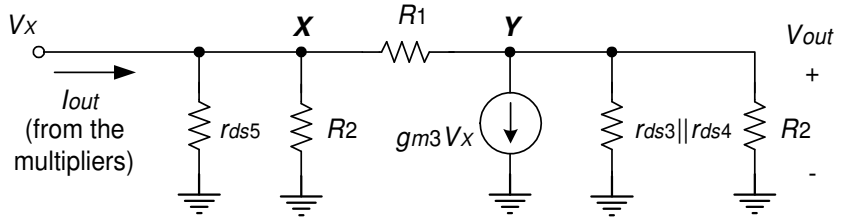


Fig. 68. Small-signal equivalent circuit of the transimpedance summing node.

of the multipliers I_{out} can be expressed as

$$\text{Transimpedance Gain} = \frac{1 - g_{m3}R_1}{g_{m3} + \dfrac{1}{R_Y}} \left(\frac{R_X}{R_X + \dfrac{R_1 + R_Y}{1 + g_{m3}R_Y}} \right) \tag{7.4}$$

The output resistances of transistors $M_3 - M_5$ are typically much larger than R_1, R_2 and $1/g_{m3}$. Furthermore, if we design the circuit such that $R_2 \gg R_1$ and $R_1 \gg 1/g_{m3}$, then

$$R_{in} \approx \frac{1}{g_{m3}} \tag{7.5}$$

$$\text{Transimpedance Gain} \approx -R_1 \tag{7.6}$$

The pole at the input of the summing node can been place at high frequencies due to the small equivalent resistance $1/g_{m3}$, as long as the additional gate-source capacitance of transistors M_3 and drain capacitance of transistors M_5 do not significantly increase the parasitic capacitance at this node.

On the other hand, under the same assumptions above, the equivalent resistance at the output of the summing node can be found to be

$$R_{out} \approx \frac{1}{g_{m3}} \tag{7.7}$$

Observe that this equivalent low resistance also permits the output pole to be placed at high frequencies. This is an advantage over the cascode summing node, where the output pole depends on the value of R_L, and therefore limits the gain.

Using equation 7.6, the gain of the equalizer without boosting is approximately given by (refer to its definition in page 77)

$$\left| \frac{V_{out}}{V_{in}} \right| \approx g_{mc}\ R_1 \tag{7.8}$$

Thus, the gain can be controlled independently from the bandwidth as long as $R_1 >$

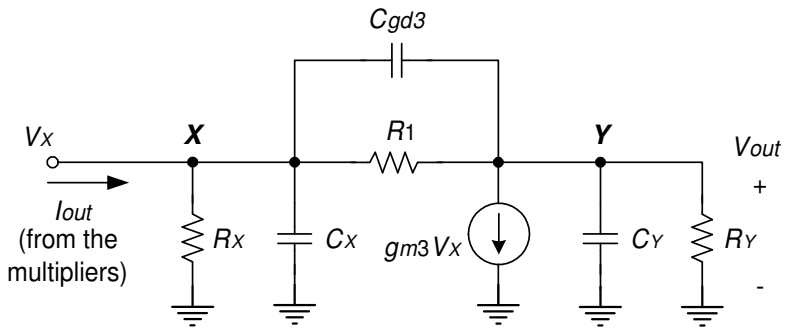


Fig. 69. Small-signal equivalent circuit of the transimpedance summing node including parasitic capacitances.

$1/g_{m3}$.

In practice, the parasitic capacitances decrease the transimpedance gain of the summing node at high-frequencies. Repeating the analysis using now the equivalent circuit depicted in figure 69, where C_X and C_Y denote the total shunt capacitance to ground at nodes X and Y respectively, the transimpedance gain can be expressed as

$$\text{Transimpedance Gain} = -\frac{b_1 s + b_0}{a_2 s^2 + a_1 s + a_0} \tag{7.9}$$

where

$$b_1 = -C_{gd3} \tag{7.10}$$

$$b_0 = g_{m3} - G_1 \tag{7.11}$$

$$a_2 = C_X C_Y + C_{gd3} C_X + C_{gd3} C_Y \tag{7.12}$$

$$a_1 = G_Y C_X + G_1 C_X + G_X C_Y + G_X C_{gd3} + G_Y C_{gd3} + G_1 C_Y + g_{m3} C_{gd3} \tag{7.13}$$

$$a_0 = G_X G_Y + G_X G_1 + G_Y G_1 + g_{m3} G_1 \tag{7.14}$$

and $G_1 = 1/R_1$, $G_X = 1/R_X$, $G_Y = 1/R_Y$.

To have unity gain with a transconductance from the multipliers of $g_{mc} =$

Table IX. Component values for the transimpedance summing node.

Component Name	**Value**
R_1	1kΩ
R_2	5kΩ
M_3 ($g_{m3} = 7$mA/V)	16 (6.8μm/0.4μm)
M_4	4 (10μm/0.4μm)
M_5	10 (10μm/0.4μm)
I_{bias}	2mA

1mA/V, a value of $R_1 = 1$kΩ has been selected. Furthermore, for a 3dB bandwidth of $\sim$ 1GHz, transistor M_3 has been sized to obtain $g_{m3} = 7$mA. Table IX presents the final resistor and transistor values, along with the bias current I_{bias}. Notice that R_1 and R_2 are much greater than $1/g_{m3}$ as has been suggested for high-speed performance, while $R_2 = 5R_1$. The reason for not increasing R_2 further is to keep the parasitic capacitances due to the layout of the resistors small. Poly2 has been used, since it has a larger sheet resistance and less capacitance to substrate than poly1. The layout is shown in figure 70. The location of the serpentine resistors in the upper portion has been chosen to match the rest of the equalizer's layout.

3. Simulation Results

Three FIR structures, one using a conventional load resistor as the summing node, and two using the proposed summing nodes have been simulated. The multiplier cell

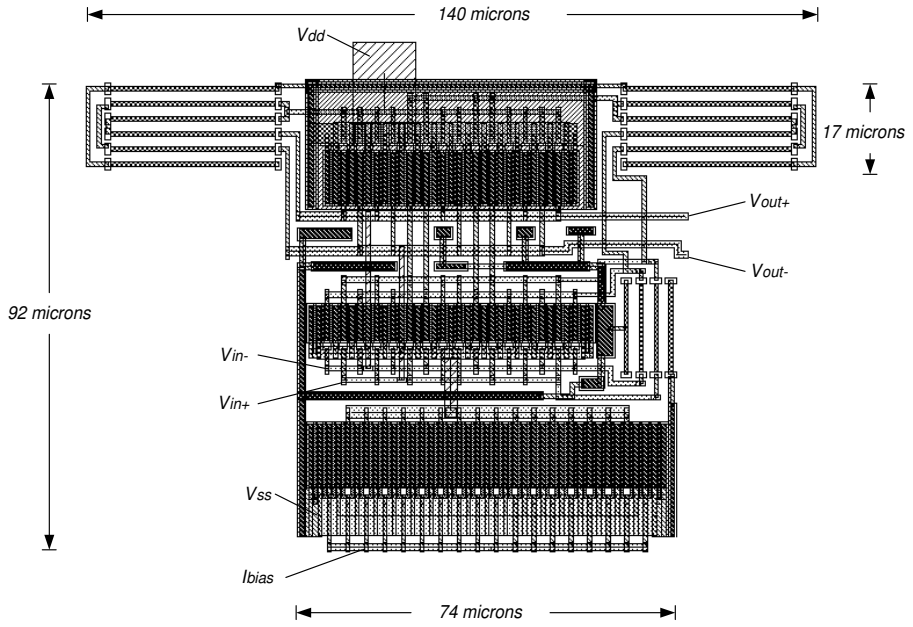


Fig. 70. Layout of the proposed transimpedance summing node.

used in the design is shown in figure 71. Notice that a PMOS driver and two current mirrors are used to control the coefficients applied to the Gilbert Cell. This improves the PSRR$^-$ compared to the case where the coefficients are directly applied to the gate of transistors M_1. Each multiplier consumes 1.5mA of current.

The magnitude response of the two proposed summing nodes is shown in figure 72, and compared against the response obtained with a conventional resistive load with a value of $R_L = 1k\Omega$. All three circuits use the same current for the multipliers. The transimpedance summing node uses an additional current of 2mA to bias transistors M_3.

The proposed cascode summing node improves the 3dB bandwidth by a factor of 1.9 with respect to the conventional resistive load, resulting in a 3dB bandwidth of 520MHz. The improvement comes at no expense of additional power consumption.

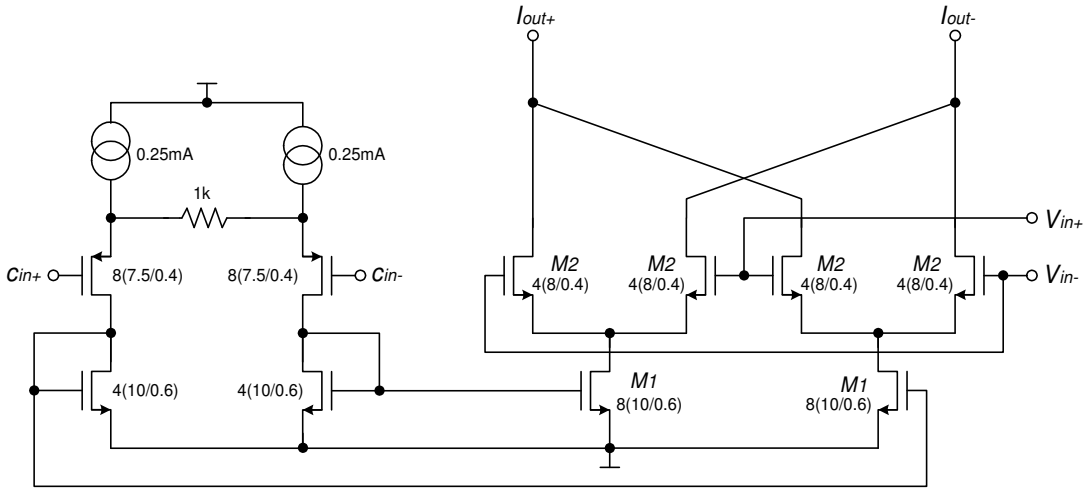


Fig. 71. Transistor level schematic of the multiplier.

Without this technique, the equalizer gain would need to be decreased $20\log(1.9) = 5.6$dB to achieve the same bandwidth with the same power consumption. The total power consumption of the 5 multipliers and the summing node is 22.5mW (Supply = $\pm$1.5V).

The proposed transimpedance summing node improves the bandwidth by a factor of 3.8 with respect to the conventional resistive load. Its wider bandwidth compared to the cascode topology leads to less deterministic jitter at the output of the equalizer. Because of its superior performance, the transimpedance summing node has been selected for inclusion in the high-speed 5-tap equalizer architecture. The total power consumption of the 5 multipliers and the summing node is 28.5mW (Supply = $\pm$1.5V).

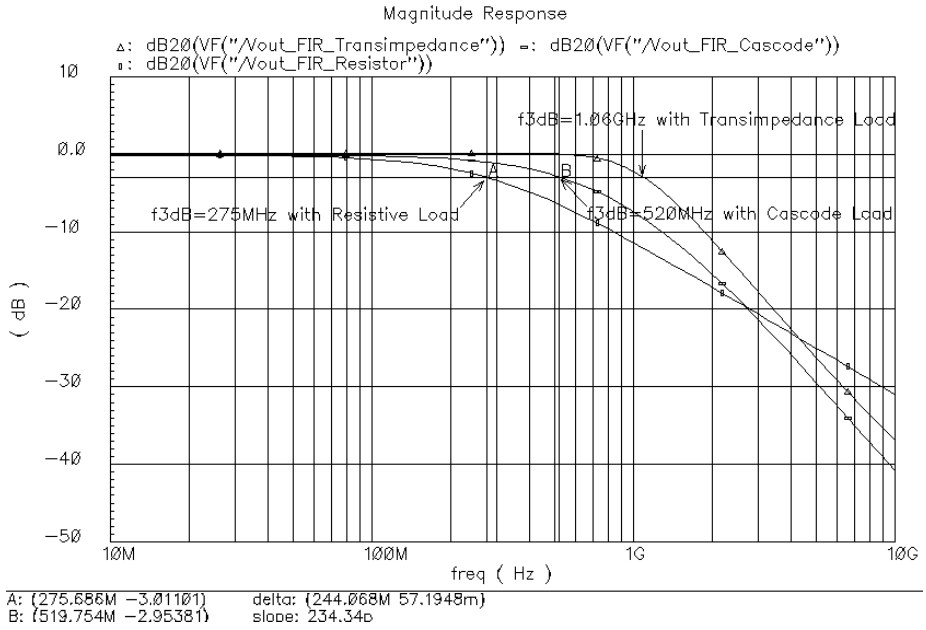


Fig. 72. Comparison between the proposed summing nodes and the conventional resistive load.

C. 1 Gb/s 5-Tap Transversal Equalizer

The complete design of the 1Gb/s 5-tap equalizer includes: 4 third-order linear-phase delay lines, 5 multipliers, 1 transimpedance summing node, 1 pre-amplifier, and 1 output buffer to drive the 50Ω load of the test equipment as well as its capacitance and that of the pads and PCB traces. The layout is shown in figure 73. Coefficients $[C_0 \ldots C_4]$, connected to the 5 multipliers, control the frequency response of the equalizer. Independent supply connections (V_{dd} and V_{ss}) are provided for the delay lines, multipliers/summing node, and output buffer.

1. Simulation Results

The simulated frequency response of the complete equalizer is shown in figure 74 for different set of coefficients with increasing high-frequency boosting. The results show

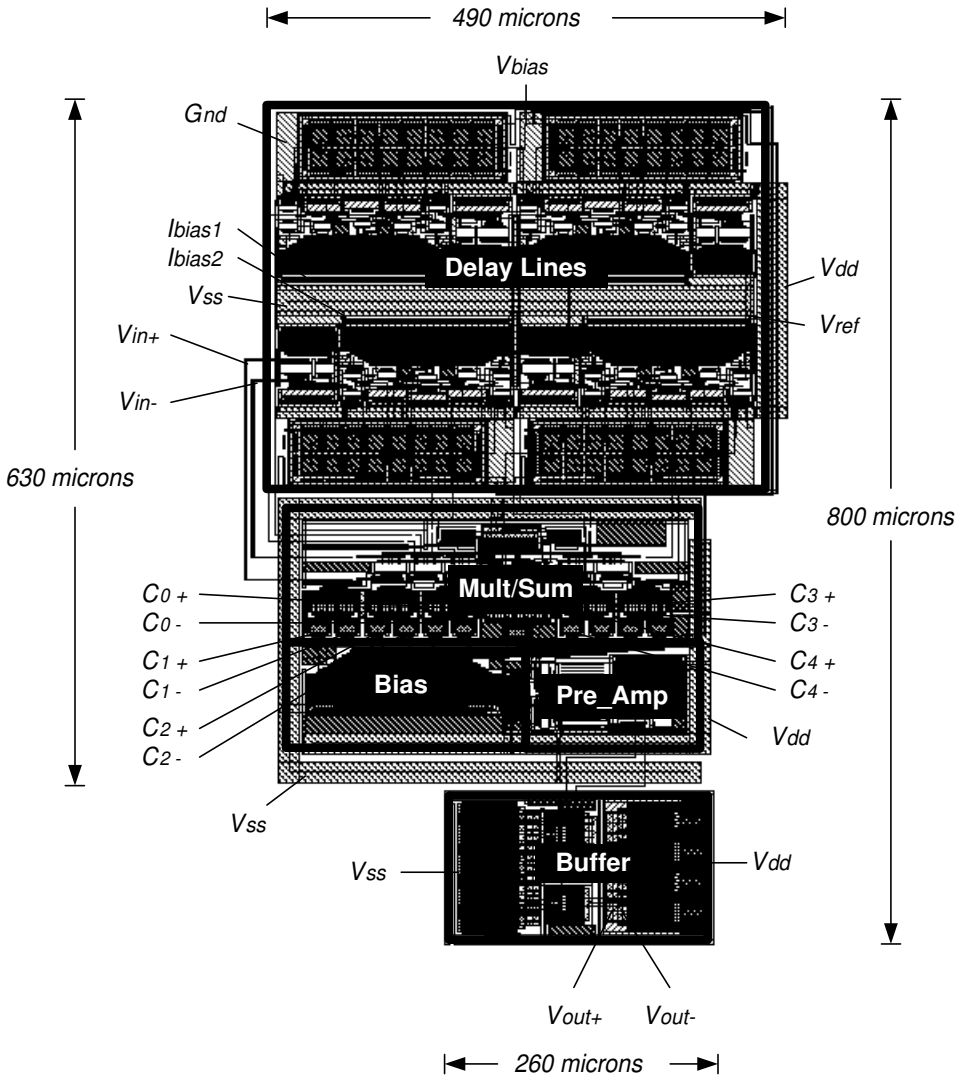


Fig. 73. Layout of the complete 1Gb/s 5-tap equalizer.

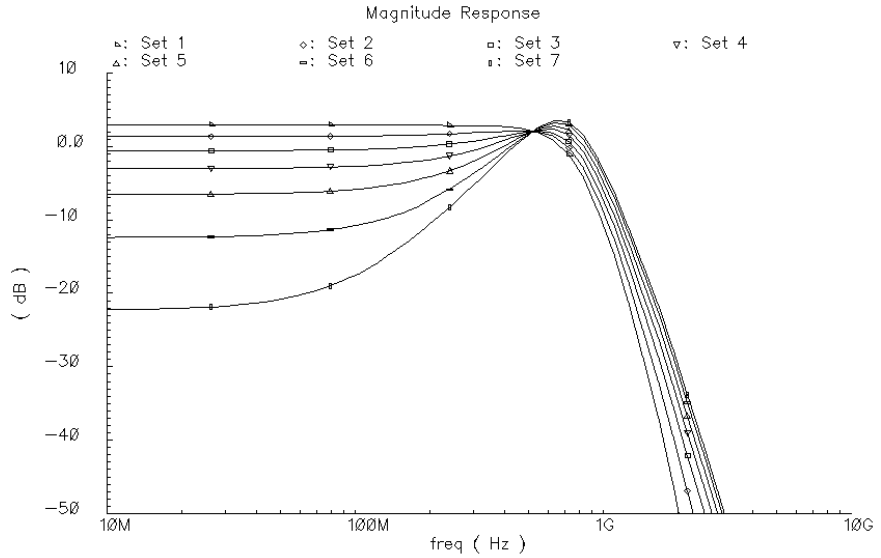


Fig. 74. Simulated magnitude response for different set of coefficients.

that the equalizer can compensate for more than 25dB of attenuation at 500MHz.

The equalization of 15 meters of CAT5e cable is demonstrated in figure 75. The eye-pattern diagram before equalization (left plot) shows a vertical eye opening of 10mV, which corresponds to 10mV/140mV = 7.1% of the peak amplitude. After the equalizer (right plot), the vertical eye opening has been increased to 210mV, which corresponds to 210mV/300mV = 70% of the peak amplitude. The simulated output noise due to the equalizer+preamp+buffer is $2.4\text{mV}_{\text{rms}}$. Ignoring other sources of noise in a wireline transceiver, this results in an output signal-to-noise ratio of $\text{SNR}_{out} = 20\log(210/4.8) = 32.8\text{dB}$, enough to provide theoretically a BER $< 1 \times 10^{-25}$ (see chapter VI, section C).

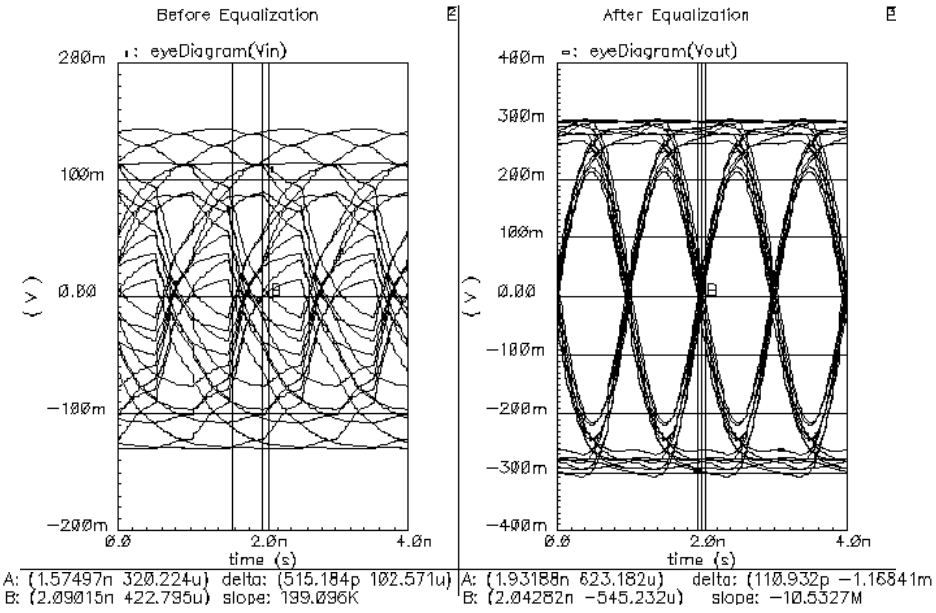


Fig. 75. Simulated eye-pattern diagrams before and after equalization of 15 meters of CAT5e cable.

D. Experimental Results

The design was fabricated using the TSMC 0.35μm technology through the MOSIS Educational Program. The chip micrograph is shown in figure 76. The die size is 1.8mm $\times$ 1.8mm.

To characterize the frequency response of the delay line, the test setup shown in figure 77 was used. Since the delay line had an output buffer to drive the 50Ω impedance of the network analyzer, the frequency response of the buffer itself had to be obtained to de-embed it from the delay line measurements. By including a stand-alone buffer replica on-chip, this de-embedding was possible. The measured group delay and magnitude response of the delay line itself are shown in figures 78 and 79 respectively. The additional parasitic capacitances in practice increased the group delay variations on the passband to 92ps (at 710MHz), but are only 40ps within a

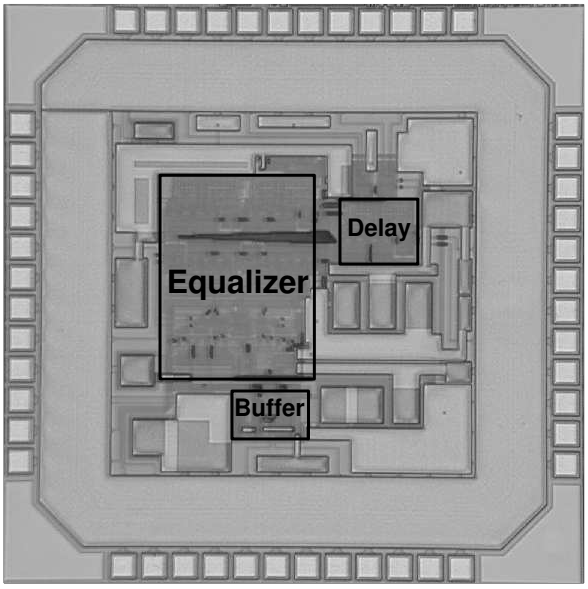


Fig. 76. Chip micrograph of the equalizer.

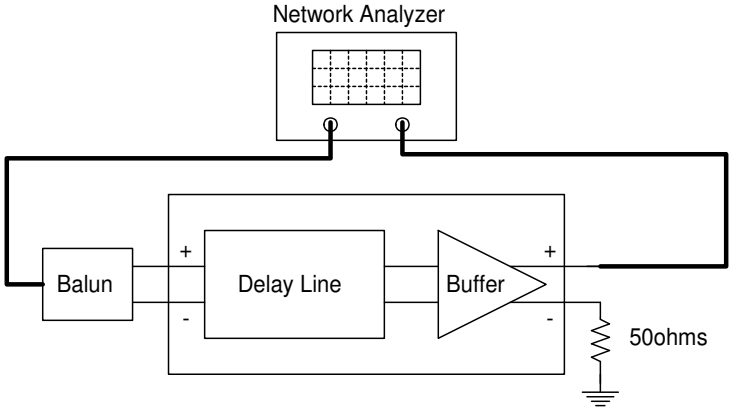


Fig. 77. Test setup for the frequency response characterization of the delay line.

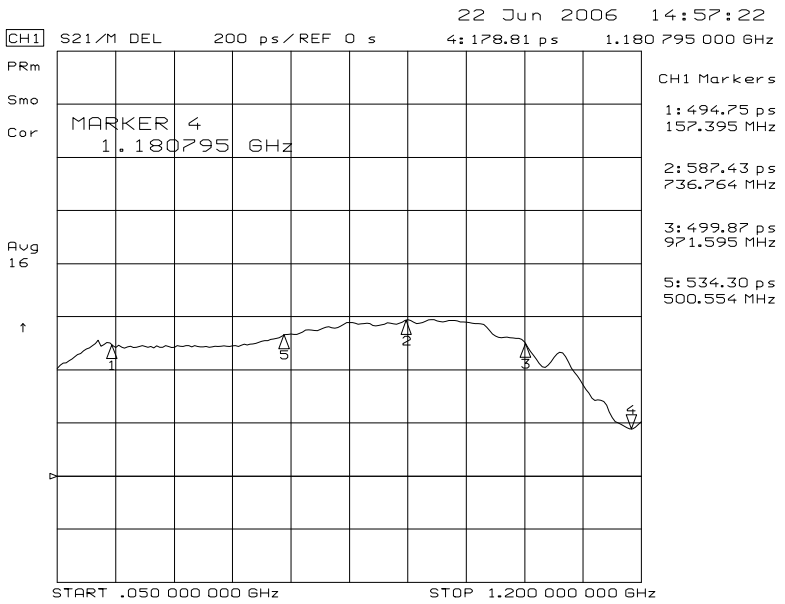


Fig. 78. Measured group delay of the delay line.

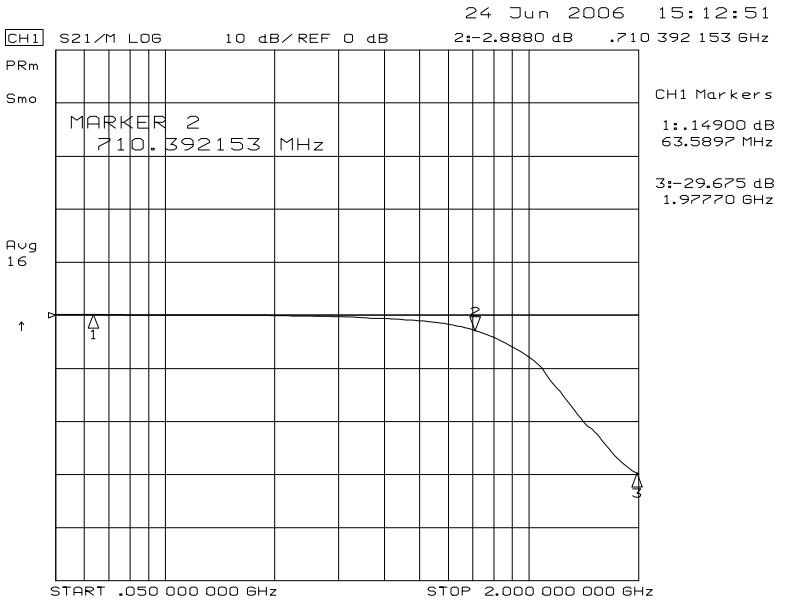


Fig. 79. Measured magnitude response of the delay line.

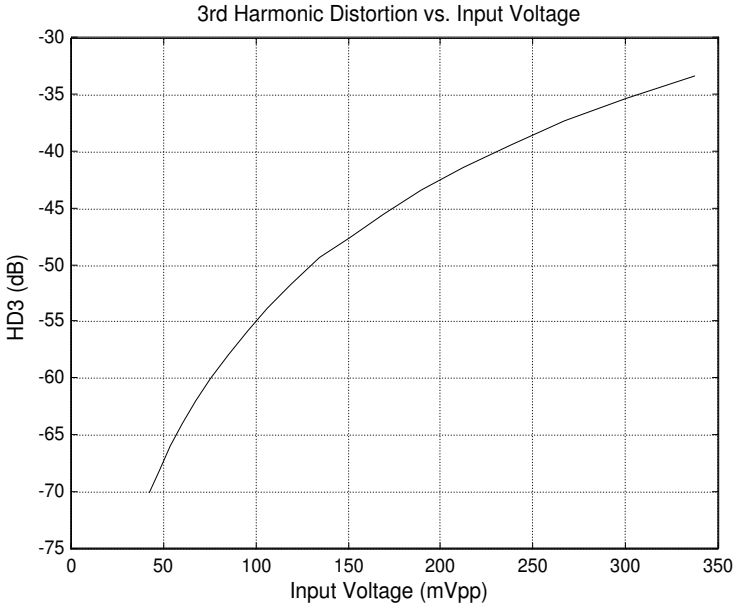


Fig. 80. Measured third-harmonic distortion of the delay line vs. input voltage.

500MHz bandwidth. It is worth mentioning that the group delay below 150MHz can not be accurately measured, since it is very close to the lower cut-off frequency of the Agilent 8719ES Network Analyzer used for the characterization.

To test the linearity of the delay lines, a third-order intermodulation (IM3) test was carried out with two input tones at 499MHz and 501MHz. From the measured IM3, the third-order harmonic distortion given by HD3 = IM3$-20\log(3)$ was obtained and plotted as a function of the input amplitude in figure 80.

To characterize the frequency response of the equalizer, as well as of the summing node alone, the test setup shown in figure 81 was used. To measure the bandwidth of the summing node, the magnitude response of the equalizer without boosting (i.e. only the first coefficient, C_0, is different from 0) was tested. The result is shown in figure 82. The measured 3dB bandwidth is 938MHz, which is sufficient for a

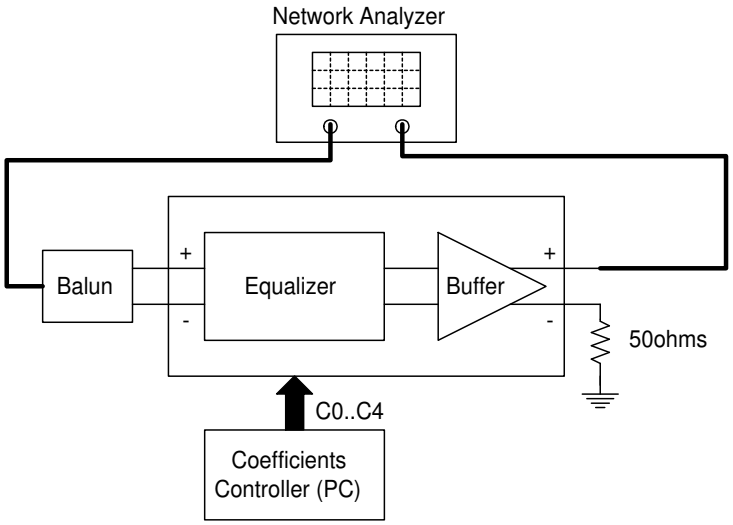


Fig. 81. Test setup for the frequency response characterization of the equalizer.

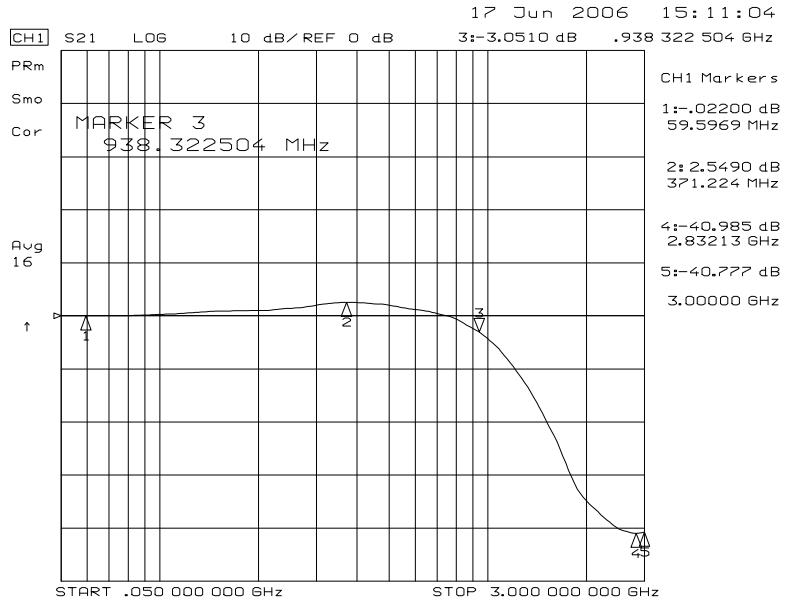


Fig. 82. Measured magnitude response of equalizer without boosting.

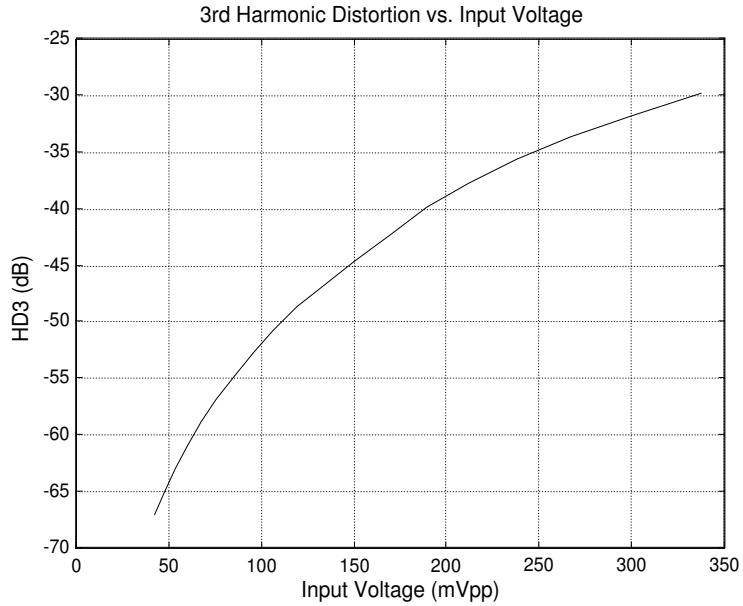


Fig. 83. Measured third-harmonic distortion of the equalizer vs. input voltage.

1Gb/s bit stream. A variation of 2.5dB in the passband gain is present due to the inductance of the bonding wires in the IC package and the PCB trace. (To reduce this undesired ripple, the 50Ω termination resistor of the output buffer should have been placed on-chip, along with a proper broadband impedance matching network that required better prior knowledge of the bondwire parasitics.) The third-order harmonic distortion under these conditions is shown in figure 83 as a function of the input amplitude. Again, the HD3 has been obtained from IM3 tests with input tones at 499MHz and 501MHz. For an ECL compatible input swing of 300mV_{pp}, an HD3 = −32dB was obtained.

The measured frequency response of the equalizer is shown in figure 84 for different set of coefficients with increasing high-frequency boosting. Similar to the simulation results, this plot shows that the equalizer can compensate for a loss of more

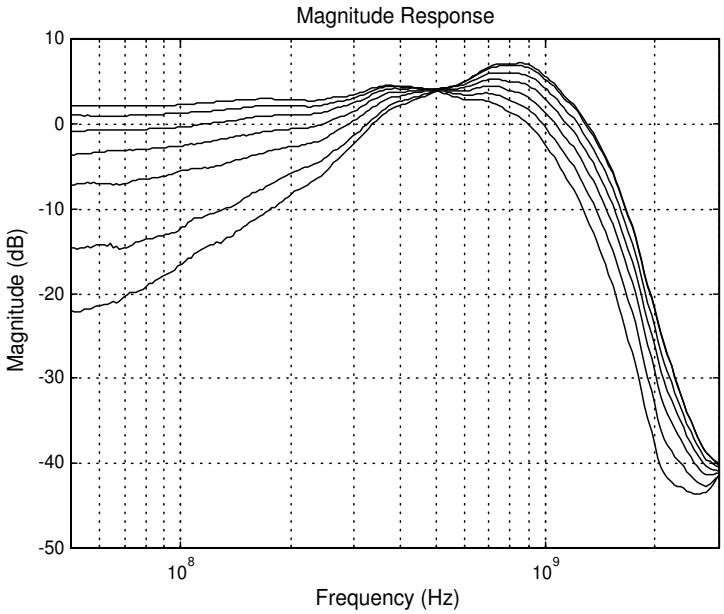


Fig. 84. Measured magnitude response of the equalizer with boosting.

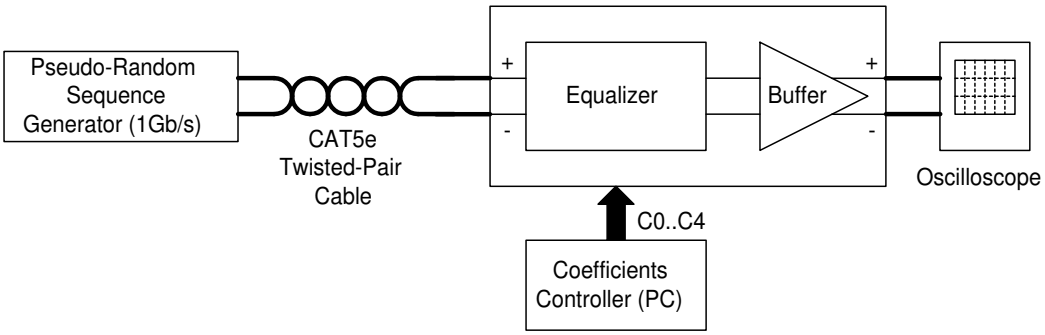
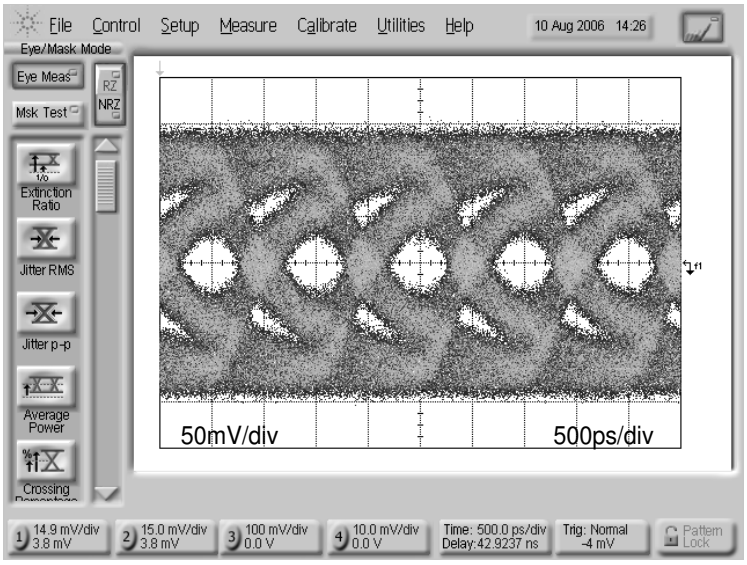


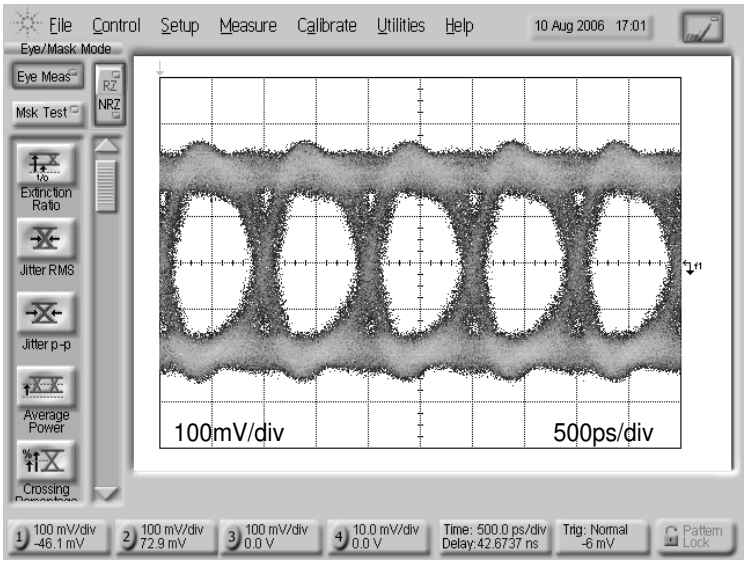
Fig. 85. Test setup for the equalization of 1Gb/s binary data using CAT5e twisted-pair cable.

than 25dB at 500MHz.

The equalization of 15 meters and 23 meters of CAT5e twisted-pair cable was demonstrated using the setup shown in figure 85. The measured eye-pattern diagrams of a 1Gb/s pseudo-random binary sequence ($2^{23} - 1$ bits long) before and after the equalizer are shown in figures 86 and 87. For 15 meters, the vertical eye opening before and after equalization are 15% and 59% respectively. For 23 meters, the vertical eye opening before and after equalization are 0% and 58% respectively.

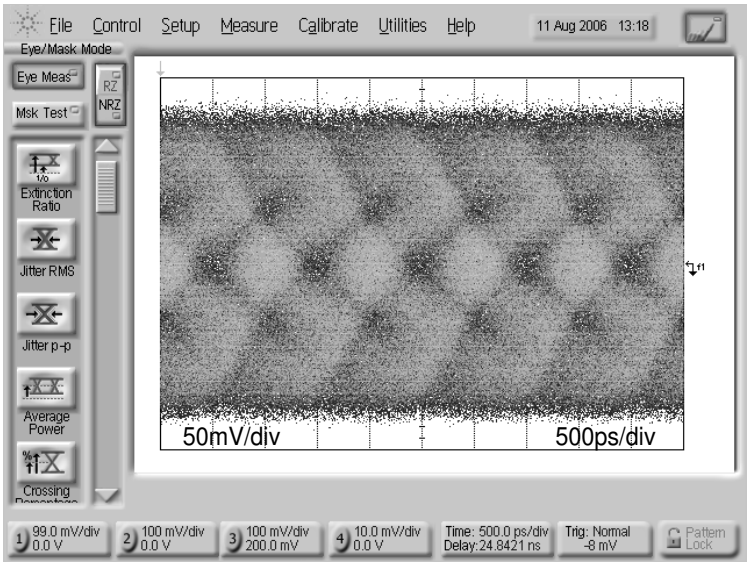


(a)

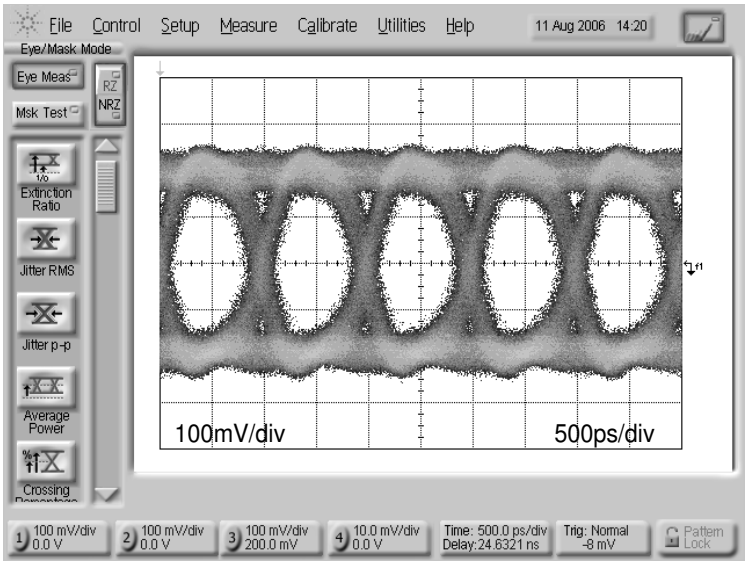


(b)

Fig. 86. Measured eye pattern diagrams for 15 meters of CAT5e cable. (a) Before equalizer and (b) after equalizer.



(a)



(b)

Fig. 87. Measured eye pattern diagrams for 23 meters of CAT5e cable. (a) Before equalizer and (b) after equalizer.

Table X. Comparison of the proposed delay line with previous work normalized to 500ps.

Delay Line Technique	**3dB Bandwidth f_{3dB}**	**Group Delay Ripple within 500MHz**	**Group Delay Ripple within f_{3dB}**
[33]	436MHz	84ps	124ps
[61]	909MHz	320ps	320ps
[62]	NA	188ps	NA
[63]	440MHz	68ps	80ps
This Work	710MHz	40ps	92ps

A comparison between the performance of the proposed delay line and that of previously published techniques when normalized to 500ps is presented in table X. This work significantly outperforms the group delay flatness of all the cited references. Although the measured group delay variation within the 3dB bandwidth is larger than in [63], this is because the proposed delay line offers a significantly wider bandwidth of operation (by a factor of 1.3), which in turn leads to a better vertical eye opening and reduced jitter [7].

A comparison between the performance of the proposed 1Gb/s transversal equalizer with previously proposed works is shown in table XI, where the figure of merit to compare the achieved speed given the bandwidth limitation imposed by the technology has been defined as

$$FOM = \frac{\text{Data Rate (Mb/s)}}{\text{Transit Frequency} f_t \text{(GHz)}} \tag{7.15}$$

Table XI. Comparison of the proposed equalizer with previous work.

Reference	**Technology**	**Transit Frequency f_t (GHz)**	**Data Rate (Gb/s)**	**FOM Data Rate/f_t (Mbps/GHz)**
[33]	0.18μm CMOS	60	3.125	52
[61]	0.18μm SiGe BiCMOS	120	10	83
[63]	0.25μm CMOS	30	1	33
This Work	0.35μm CMOS	15	1	67

where the transit frequency is the unity current gain frequency of a single transistor in a given technology.

It is clear from table XI that the proposed equalizer is competitive in rate/bandwidth efficiency given the technology limitations.

A complete summary of the results is shown in table XII.

Table XII. Performance summary of the 1Gb/s equalizer.

Parameter	**Value**
Number of Taps	5
Equivalent Sampling Rate of Equalizer	1/500ps = 2GHz
Input Voltage Range (ECL Compatible)	300mVpp
3dB Bandwidth of Delay Lines	710MHz
Group Delay Variation of Delay Lines within 500MHz	40ps
Signal-to-Noise Ratio of Delay Lines with V_{in} = 300mVpp	61dB
3dB Bandwidth of Summing Node	938MHz
Signal-to-Noise Ratio of Equalizer with Flat Unity Gain (no boosting) and V_{in} = 300mVpp	36dB
Maximum Boosting at 500MHz	> 25dB
Supply Voltage	±1.5V
Total Power Consumption	96mW
Silicon Area	630μm × 490μm
Technology	TSMC 0.35μm

CHAPTER VIII

CONCLUSIONS

To increase the speed at which switched-capacitor (SC) networks can implement signal processing blocks in communications systems, a continuous-time common-mode feedback (CMFB) circuit has been presented. Its reduced input capacitance loading the output of the amplifier improves the achievable gain-bandwidth product. Furthermore, it provides a better rejection to noise coming from the negative power supply. A second-order 10.7MHz bandpass filter was designed to compare the performance of the proposed CMFB with a conventional switched-capacitor based CMFB. Experimental results demonstrate that the settling-time error introduced by the finite gain-bandwidth product of the amplifiers is significantly reduced when using the proposed CMFB. The third-order intermodulation distortion of the proposed architecture is comparable with conventional solutions, showing that the linearity of the proposed continuous-time CMFB is sufficient for typical switched-capacitor applications. A major advantage of this approach is that it improves the PSRR^- by > 20dB over that of a conventional SC-CMFB scheme.

While periodical non-uniform individual sampling (PNIS) reduces the capacitive spread in high-Q SC filters, it introduces additional alias components due to the use of slower clocks. An equivalent model for the analysis of such alias components has been presented. Practical expressions that estimate their power at the output of the filter within 2.5dB of error have been obtained in the context of first-order and second-order sections. The theoretical results were then extended to cascaded higher-order filters, and design guidelines for the implementation of intermediate frequency filters have been provided.

The design of a 1Gb/s 5-tap transversal equalizer for wireline transceivers has

also been presented. The implementation is based on proposed third-order linear-phase delay lines using Gm-C emulated inductors. Experimental results show group delay variations of 40ps within 500MHz, and 92ps within the 3dB bandwidth of the delay line, which was measured to be 710MHz. Also, a high-speed transimpedance summing-node has been proposed with a measured 3dB bandwidth of 938MHz. Experimental results of the equalizer's frequency response show that it can compensate for $>$ 25dB of cable attenuation at 500MHz. The eye-pattern diagrams at 1Gb/s demonstrate the equalization of 15 meters and 23 meters of CAT5e twisted-pair cable, with a vertical eye-opening improvement from 0% (before the equalizer) to 58% (after the equalizer) in the second case.

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