

CMOS RF FRONT-END DESIGN
FOR TERRESTRIAL AND MOBILE DIGITAL TELEVISION SYSTEMS

A Dissertation

by

JIANHONG XIAO

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2007

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee, Jose Silva-Martinez
Committee Members, Edgar Sanchez-Sinencio
Peng Li
Cesar O. Malave
Head of Department, Costas Georgiades

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ABSTRACT

CMOS RF Front-End Design

for Terrestrial and Mobile Digital Television Systems (May 2007)

Jianhong Xiao, B.S., Peking University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

With the increasing demand for high quality TV service, digital television (DTV) is replacing the conventional analog television. DTV tuner is one of the most critical blocks of the DTV receiver system; it down-converts the desired DTV RF channel to baseband or a low intermediate frequency with enough quality. This research is mainly focused on the analysis and realization of low-cost low-power front-ends for ATSC terrestrial DTV and DVB-H mobile DTV tuner systems.

For the design of the ATSC terrestrial tuner, a novel double quadrature tuner architecture, which can not only minimize the tuner power consumption but also achieve the fully integration, has been proposed. A double quadrature down-converter has been designed and fabricated with TSMC 0.35 μ m CMOS technology; the measurement results verified the proposed concepts.

For the mobile DTV tuner, a zero-IF architecture is used and it can achieve the DVB-H specifications with less than 200mW power consumption. In the implementation of the mobile DVB-H tuner, a novel RF variable gain amplifier (RFVGA) and a low flicker noise

current-mode passive mixer have been proposed. The proposed RFVGA achieves high dynamic range and robust input impedance matching performance, which is the main design challenge for the traditional implementations. The current-mode passive mixer achieves high-gain, low noise (especially low flicker noise) and high-linearity (over 10dBm IIP3) with low power supplies; it is believed that this is a promising topology for low voltage high dynamic range mixer applications. The RFVGA has been fabricated in TSMC 0.18 μ m CMOS technology and the measurement results agree well with the theoretical ones.

DEDICATION

To my parents, my dearest wife Mingya Xu

For all their love and unconditional support

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I would like to express my sincere appreciation to my advisor, Dr. Jose Silva-Martinez, for his guidance, support and encouragement during my study at Texas A&M University. He showed me the art of analog integrated circuit design through his in-depth knowledge and pioneering expertise. His great personality made my research experience more joyful and encouraging. His guidance during the development of my research has been invaluable. I feel very grateful for his supervision both on the technical and the personal levels during my stay in College Station.

I would like to thank and acknowledge Dr. Edgar Sanchez-Sinencio, the director of the Analog and Mixed-signal center. It was he who gave me the admission into this group. His analog courses have educated me a lot not only in the detailed techniques but also in the spirit of analog design. His kind help, support and encouragement made my study fruitful.

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Most of my research time was spent on the two research projects, the designs of terrestrial DTV tuner and mobile DTV tuner. The contributions and cooperation of the team members made the learning and research study a great experience of life. Here I would like to thank all of my team members, including Tianwei Li, Guang Zhang, Raghavendra Kulkarni and Dr. Yong Moon.

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CHAPTER I

INTRODUCTION

1.1. Digital Television Systems

Television is a very cost-effective system which informs, educates, and entertains all societies around the world. The television system can be simply described by Fig. 1.1. In the transmission side, the TV data including video and audio information is firstly modulated using an efficient modulation scheme and then transmitted. Usually the modulated baseband TV data is up-converted to a predefined radio frequency (RF) band before the transmission. The RF TV signal will be transmitted out from the TV tower station and received by TV receivers. For the broadcasting TV, the transmission channel is air. In the receiver side, the RF TV signal is captured and down-converted to baseband (or low intermediate frequency) by the TV tuner. The demodulator, after the DTV tuner, will complete the data demodulation and feed the signal into the signal processing block (usually digital decoder). Finally, the TV signal will be displayed in the monitor.

In the conventional TV system, the TV data is modulated employing an analog modulation scheme; hence the TV system is called analog television. Analog television broadcasting systems based on NTSC, PAL or SECAM standards have been successfully established in many countries since the middle of the last century. In recent years, due to the development

of the data compression techniques (like MPEG compression) and digital communication, the digital television system is emerging and will replace analog television system eventually.

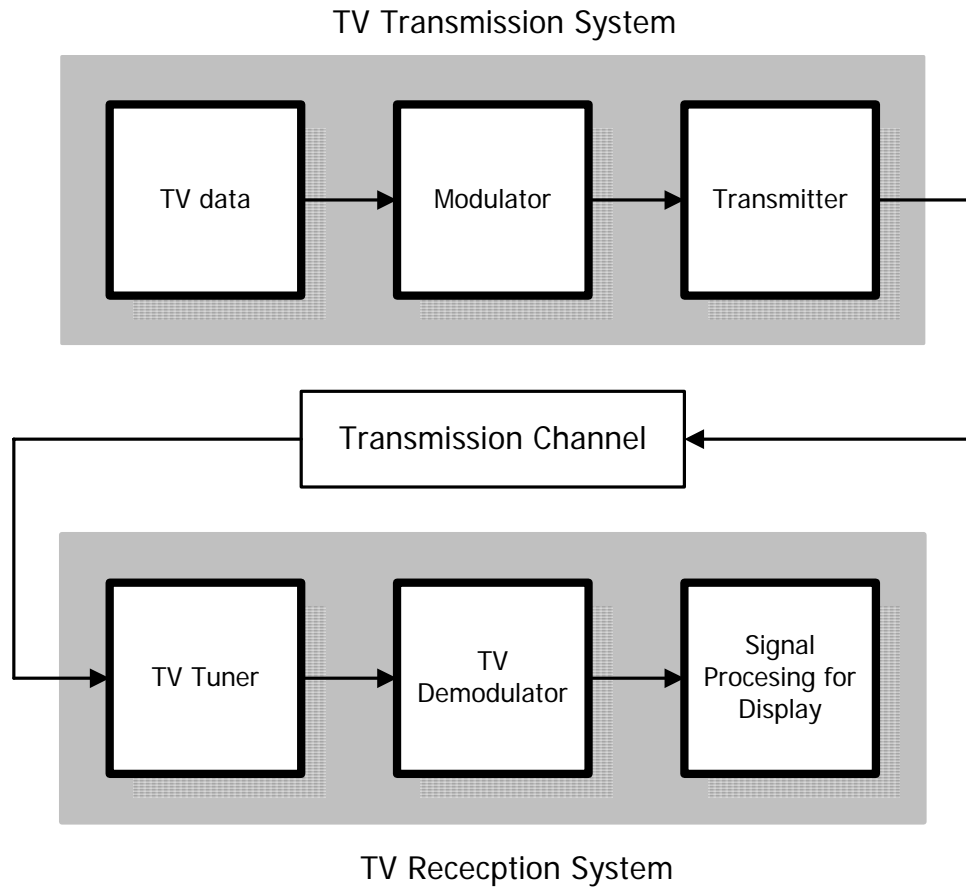


Fig. 1.1. Block diagram of the television system

There are multiple advantages for the DTV compared with analog television. DTV not only delivers interference and distortion-free video and audio signals; more importantly it can do so while achieving much higher spectrum efficiency than analog television. DTV can also seamlessly interface with other communication systems, computer networks, digital media,

enabling datacasting and multimedia interactive services; it is a key element of the ongoing digital revolution leading toward the information society [1].

Table 1.1. Summary of terrestrial and mobile DTV standards

	ATSC	DVB-T	ISDB-T	DVB-H	ISDB-T (Mobile)
Frequency Range (MHz)	54-806	47-854	470-770	470-862	470-770
Channel Bandwidth (MHz)	6	8	6	6/7/8	0.43
Modulation Scheme	8-VSB	COFDM	OFDM	COFDM	OFDM
Threshold CNR (dB)	15	18.7	25	24.8	25
Sensitivity (dBm)	-83	-80	-75	-75	-86

Currently multiple DTV standards are used worldwide. In USA, the Advanced Systems Committee (ATSC) developed the 8-VSB standard for the terrestrial DTV [2]; in Europe, the Digital TV Project has finalized the series of DTV standards named as DVB [3]; the ISDB standards were developed by Japan [4]. In addition, China is developing another terrestrial DTV standard, which is expected to be finalized soon [1]. For each series of standards, based on the transmission method, they are classified as terrestrial DTV, cable DTV and satellite DTV. Remarkably, the mobile DTV standards, like DVB-H [5], which is the modified version of the original terrestrial DVB-T standard, have been proposed for the

emerging mobile handset reception and can reduce the average power consumption of the mobile DTV receiver by 90%.

In Table 1.1, the critical transmission parameters of multiple terrestrial and mobile DTV standards are listed. For the DVB-T standard, the threshold carrier to noise ratio (CNR) and sensitivity are defined for 64QAM modulation and $2/3$ code rate case. For the ISDB-T standard, the threshold CNR and sensitivity are defined for 64QAM and $7/8$ code rate. For the DVB-H mobile standard, the frequency range listed here is only for Europe and the sensitivity is calculated based on 8MHz channel and 64QAM modulation ($3/4$ code rate). For the ISDB-T mobile standard, only one segment of the 6MHz (totally 13 segments) is used for mobile DTV transmission and the sensitivity is referred to segment power instead of 6MHz channel power.

1.2. Digital Television Tuner

Television tuner is the first block of the television receiver, as shown in Fig. 1.1. The functionality of the tuner is to select and down-convert the desired TV channel from RF frequency to DC or a predefined intermediate frequency. Because there are multiple TV transmission methods like terrestrial, cable and satellite, different tuners are required such as terrestrial TV tuner, cable TV tuner and satellite TV tuner. For each kind of tuner, since there are different standards in different regions, it is common to have a tuner specially designed for each region. And since the analog TV will be replaced by digital TV soon, commercially available devices are all DTV tuners. It is important to notice that during the

transition time from analog TV to digital TV, it is mandatory that the tuner has to handle not only digital TV but also analog TV. For example, the market available terrestrial TV tuner for USA has to handle not only ATSC digital TV (ATSC) but also NTSC analog TV.

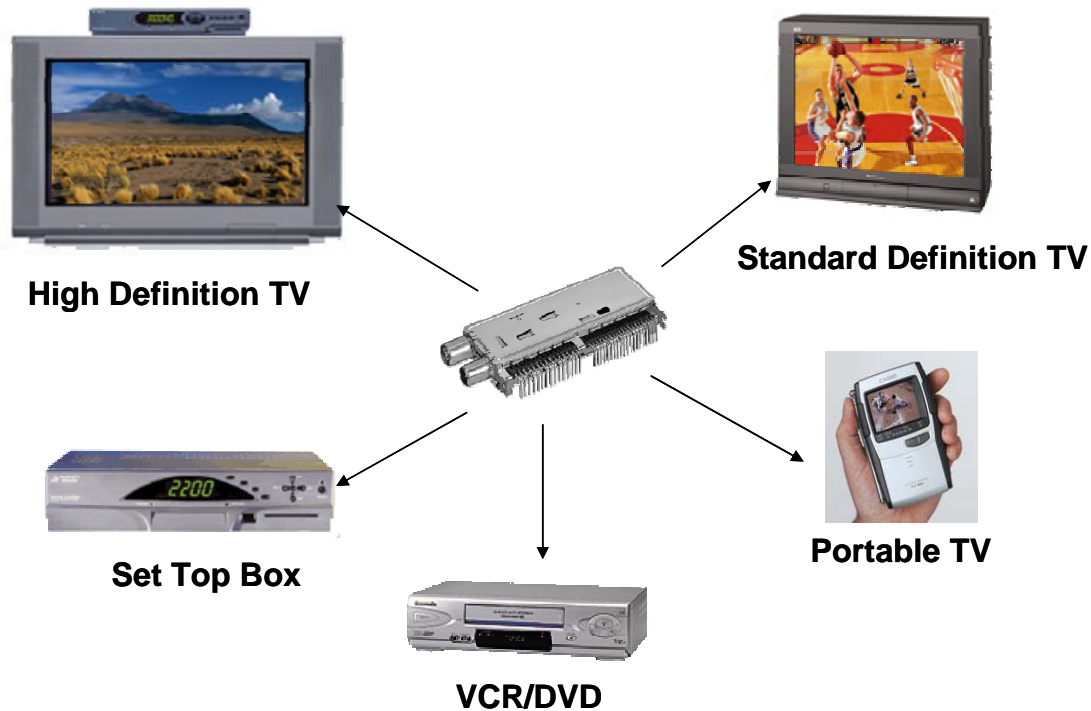


Fig. 1.2. DTV tuner applications

As discussed before, the tuner is the necessary block for the DTV receiver. More specifically, the tuner can be used in high definition TV (HDTV), standard definition TV (SDTV), set top box (STB), VCR/DVD and even portable TV like PDA or cellphone. These applications are also described in Fig. 1.2. For all of these applications, they have similar design targets, which are low-power and low-cost.

Low-power design can help to reduce the overall power consumption of the DTV receiver. More important, low-power is mandatory for the emerging portable and mobile DTV applications. For example, over 1w power consumption might be acceptable in HDTV or STB but cannot be tolerated in a handset device. Typically, the handset device requires the average power consumption less than 100mW due to limited battery life time, which becomes a design challenge for the tuner industry.

Low-cost means to reduce the bill of material (BOM). It can increase the product profit margin, or alternatively allow more price reduction to strength the market competition. The most efficient way to reduce the cost is to increase the integration level. In the history, bulky can tuners have been used since the invention of the TV. A lot of discrete components including tunable or fixed coils have to be used in the tuner design. Those components usually vary a lot with process and temperature variations, which requires extra labor to tune the parameters. In addition, the bulky area limited its usage in many applications especially the emerging mobile market. On the contrast, the manufactures of highly integrated silicon tuners are much easier and they require much less extra labor, which reduces the overall cost dramatically. In addition, a tiny integrated chip reduces the area a lot compared with the can tuner. Therefore, with the development of silicon technology, there is no doubt that the fully integrated tuner will replace the can tuner eventually just as the transistors replaced the vacuum tube.

For the available integrated DTV tuners, there are still a lot of remaining challenges to achieve low-power low-cost design. For example, most of commercial integrated tuners are

implemented with expensive technologies like SiGe BiCMOS technology instead of standard massive volume CMOS technology. By using CMOS technology, we can reduce the fabrication cost, especially when considering the future receiver system integrated on chip (SOC). Therefore, CMOS DTV tuner design is the main research target for this dissertation, including system level architecture modifications and block level novel circuit implementations to reduce the power consumption and achieve fully integration.

1.3. Research Focus and Dissertation Overview

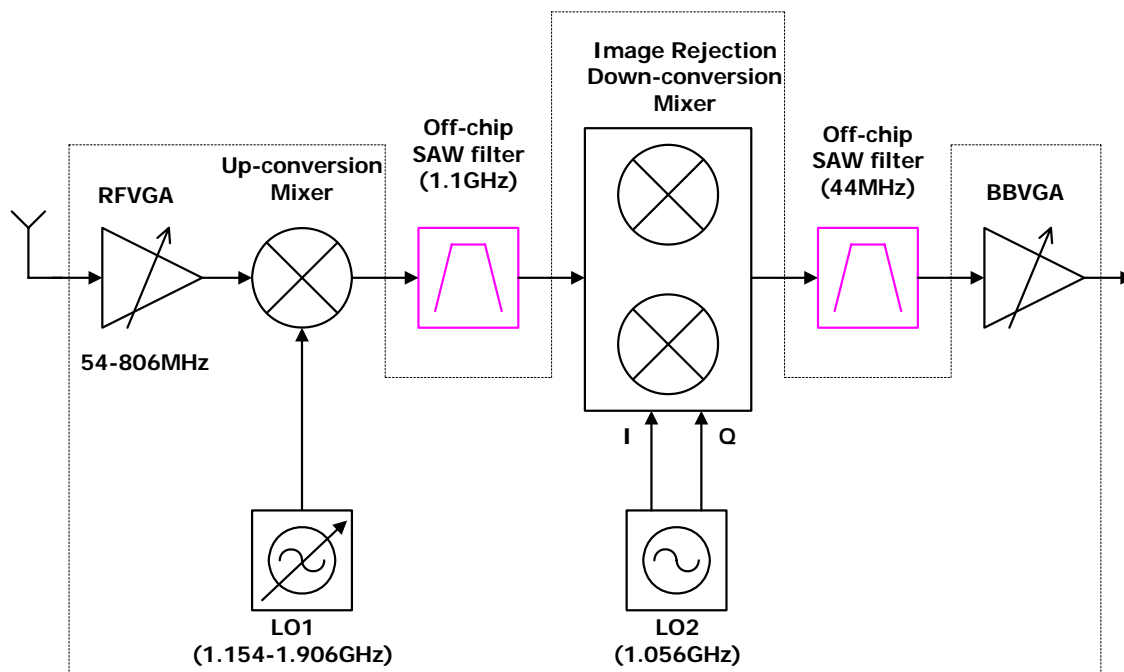


Fig. 1.3. Dual-conversion tuner architecture for ATSC terrestrial tuner

Current commercially available DTV tuners are usually implemented using dual-conversion architecture, as shown in Fig. 1.3. In this configuration, the incoming RF signal

is first up-converted to a RF frequency (usually more than 1 GHz) and then down-converted to the intermediate frequency (like 44MHz). This approach has multiple drawbacks. First of all, usually two off-chip SAW filters are required in the implementation. This limits the integration level and adds extra cost. Second, due to the up-and-down conversions, it consumes over 1w power consumption and cannot be used for low-power architectures.

In order to achieve the fully integration and low power, a novel tuner architecture has been employed, which will be addressed in the second chapter. Based on that architecture, the main system and block specifications are derived for the ATSC application. The critical RF front-end blocks are implemented in main stream CMOS technologies. Proper circuit configurations and design trade-offs are discussed and the experimental results are given at the end of the second chapter. With this novel implementation, the SAW filter is avoided and fully integration can be achieved. In addition, the power consumption can be reduced dramatically from over 1 watt to less than 0.5 watt.

Recently, the DTV tuner for mobile application is strongly demanded by the wireless market. Compared with the terrestrial TV tuner, the power consumption and area are more critical due to the feature of handset devices. A direct conversion (zero IF) tuner architecture has been proposed and will be presented in the chapter III. System and block specifications will be derived based on the DVB-H application. In addition, the system level design issues like DC offset, I/Q mismatch, even-order distortion and flicker noise are addressed.

RF variable gain amplifier (RFVGA) is one of the most critical blocks for the tuner application, which adjusts the amplifier gain to achieve maximum system dynamic range. In general, this block requires extremely high dynamic range because this is the first block for the tuner system. To achieve high dynamic range, low noise high linearity and wide gain range are required. In addition, as the RF input block, it requires good input impedance matching, which usually adds extra design constraints and degrades its dynamic range. In order to overcome these issues, a novel RFVGA architecture has been proposed. In the fourth chapter, the RFVGA design including architecture design, block implementation, experimental results are completely presented. The RFVGA is implemented in CMOS technology and suitable for mobile DTV applications.

For the tuner application, high dynamic range mixer is another critical RF block. It requires extremely high linearity, high gain and moderate noise figure, which is difficult to achieve for low voltage CMOS implementations. In chapter V, a novel current-mode passive mixer design will be presented. It can achieve the high dynamic range specifications and contribute very small amount of flicker noise. More importantly, the proposed topology can work properly in low power supply, which is believed to be a promising candidate for the future scaled-down technologies.

In chapter VI, the dissertation is summarized and the main conclusions are given.

CHAPTER II

LOW POWER FULLY INTEGRATED CMOS DTV TUNER FRONT-END

FOR ATSC TERRESTRIAL BROADCASTING

2.1. ATSC Terrestrial DTV Tuner System

8-VSB is the modulation scheme for USA digital television broadcasting. According to ATSC digital television standard [2], digital television information including video data and audio data are compressed into MPEG-2 format; the digital data is modulated with 8-VSB and up-converted to the desired RF channel for the transmission. Digital television uses the same frequency plan as conventional analog TV broadcasting, which is from 54MHz to 806MHz. For the receiver design, the major difference between analog TV and digital TV is the threshold SNR requirement for the demodulator. Due to noise-like flat spectrum (digital television) instead of discrete carriers (analog television); the SNR for DTV only needs 15dB, which will potentially make it suitable for wide coverage broadcasting.

Fig. 2.1 shows the input spectrum for the ATSC DTV tuner. During the transition time from analog TV to DTV, both analog TV channel and digital TV channel must be received by the tuner. After the DTV fully replaces analog TV, only DTV channels will be observed at the tuner input. For the desired DTV channel, the signal power (average power) can vary from -81dBm to -20dBm. In the worst case, the maximum power can be much higher than -20dBm. However, for a practical purpose, -20dBm is considered for the design. If the tuner

average output power level is set as 0dBm, the tuner needs provide the power gain from 81dB to 20dB.

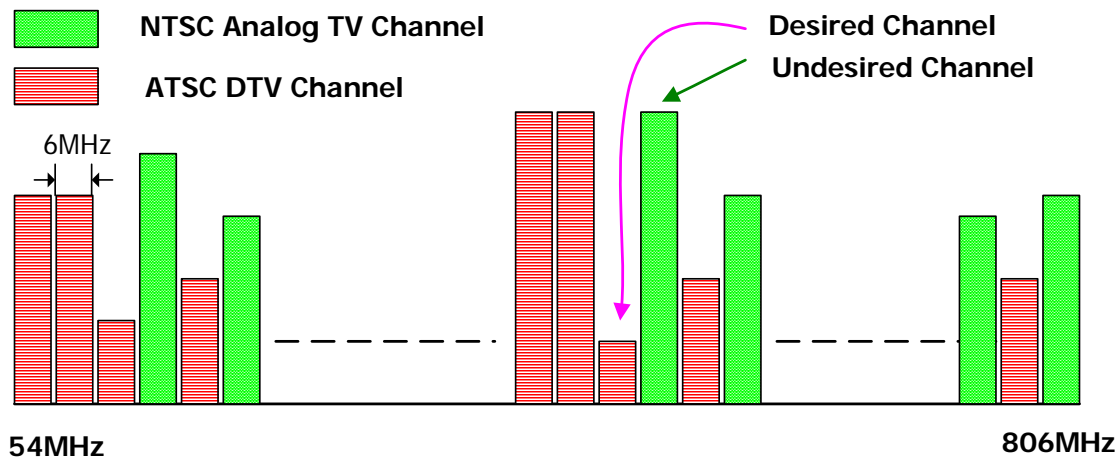


Fig. 2.1. ATSC DTV tuner input spectrum

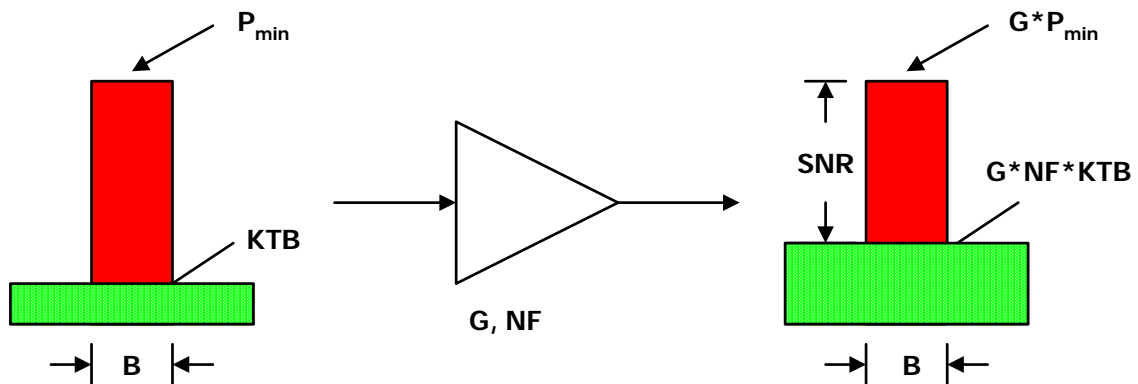


Fig. 2.2. Noise figure calculation plot

One of the critical parameters for the tuner system is noise figure, as shown in Fig. 2.2. P_{min} is the minimum input power level (also called sensitivity). kT is the product of Boltzmann

constant and absolute temperature, which is -173.8dBm/Hz in the normal room temperature (300K). B is the channel bandwidth, which is 6MHz for ATSC standard. G and NF are the gain and noise figure of the tuner, respectively. The noise figure is calculated so that the minimum output signal to noise ratio above the threshold (15dB here). Therefore, noise figure can be calculated as below

$$NF(\text{dB}) = P_{\min}(\text{dBm}) + 173.8(\text{dBm}) - 10\log(B) - SNR \quad (1)$$

The calculated noise figure will be around 10dB.

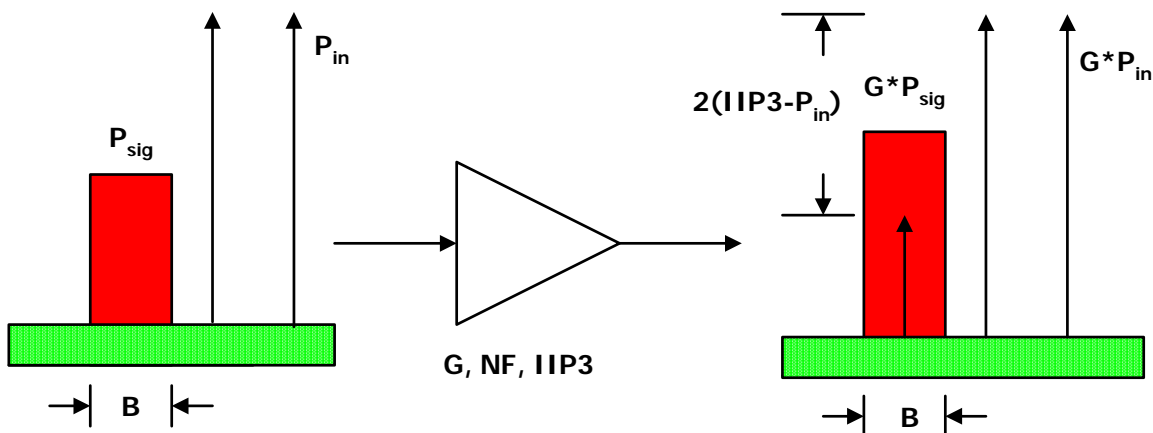


Fig. 2.3. IIP3 calculation plot

Another critical issue for the tuner design is linearity. There are many parameters required to characterize the non-linearity performance. The typical parameters are weak non-linearity specification $IIP3$ (input referred third order intermodulation intercept point) and strong non-linearity specification P_{1dB} (input referred 1dB compression point). In addition,

there are other specifications required such as CSO (composite second order distortion) and CTB (composite triple beat distortion) required in practical applications like cable TV. However, there are direct relationships between these specifications and the normal distortion specifications [6]. Therefore, those specifications are neglected for the design point of view. In addition, there is also a relationship between IIP3 and P_{1dB} [7]. Therefore, only IIP3 specification is required to fully characterize the system non-linearity performances.

Fig. 2.3 shows the IIP3 calculation plot, where the power level of the (N+1) and (N+2) adjacent channels is P_{in} and the power level of the desired channel is P_{sig} . The protection ratio is defined as P_{in} / P_{sig} . The adjacent interference channels will create third order intermodulation product due to the tuner non-linearity and the product falls within the desired channel. To ensure that the output SNR is above the threshold when considering the inter-modulation product, the IIP3 must satisfy the following equation

$$IP3 = \frac{2P_{in} + PR + SNR + 3}{2} \quad (2)$$

where 3 is the 3dB margin used in the derivation. For ATSC application, in the worst case, the protection ratio can be more than 40dB [2]. If considering the maximum interference power level is -20dBm, it results in IIP3=9dBm. Under this condition, the desired signal power level is around -60dBm.

In addition to those gain, noise and linearity specifications, the selectivity is also important. The tuner needs to attenuate the interference channels enough at the output so that the analog to digital converter in the demodulator is not saturated. In the worst case, the tuner needs to provide over 50dB attenuation for the adjacent channel, which defines the baseband filter requirement.

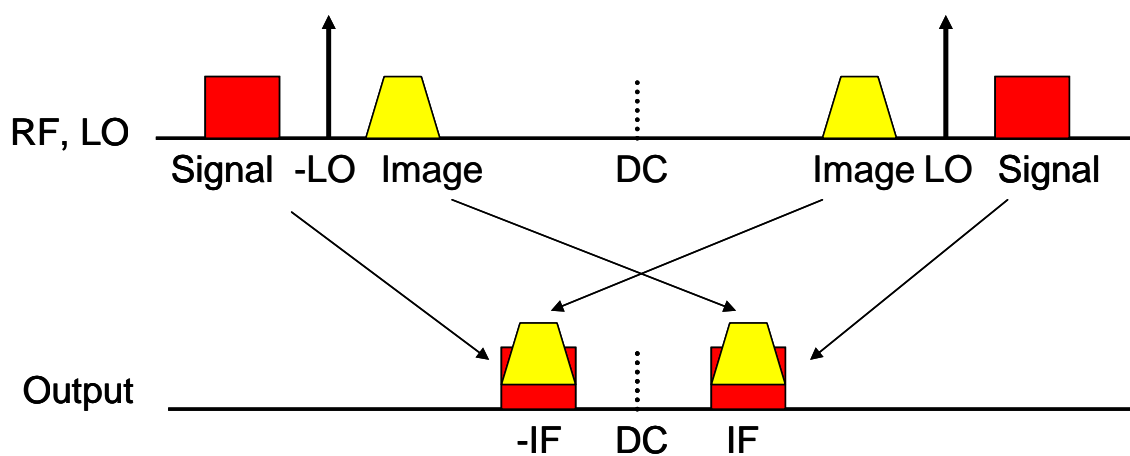


Fig. 2.4. Illustration of image problem during down-conversion in low-IF tuner

Currently, the commercial ATSC tuner needs to provide a 44MHz output, which ensures the tuner compatible with conventional demodulator baseband chip. Although this requirement can be changed in future generations, 44MHz IF is still used for this research. Therefore, there will be image issues to be solved, as shown in Fig. 2.4. For typical low-IF receiver, after the down-conversion, the image channel will be down-converted to the same frequency as signal frequency and degrades the output signal quality. In this specific application, because the final intermediate frequency is 44MHz, the image channel is 88MHz away from the desired channel; the required image rejection ratio is usually over

60dB. This image rejection requirement is the critical factor for the tuner architecture design [8], which will be discussed in the next section.

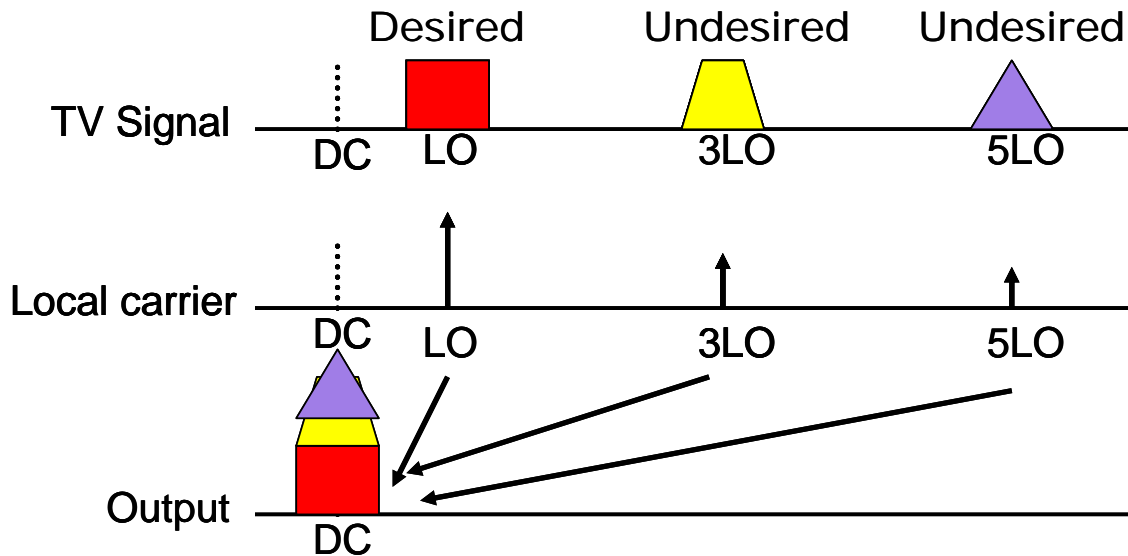


Fig. 2.5. Illustration of harmonic mixing in zero-IF tuners

In addition to image rejection issue, the tuner also has harmonic mixing issue, as illustrated in Fig. 2.5. For the zero-IF tuner, if the LO signal has some harmonic components, those harmonics will mix with the in-band interference channels and generate the undesired product in the baseband, which is called harmonic mixing issue. It is interesting to note that it also matters for low-IF architecture due to the broadband nature of the TV signal. For ATSC application, over 60dB harmonic suppression ratio is required.

From the above discussions, the overall tuner specifications are summarized and listed in Table 2.1.

Table 2.1. System specifications for ATSC tuner

Parameters	Value
Channel bandwidth	6MHz
DTV frequency range	54MHz to 806MHz
Input power	-81 dBm to -20 dBm
Output range	1 V _p @ 500Ω = 0 dBm
Intermediate Frequency	44 MHz
System gain range	81 dB to 20 dB
NF	10 dB
IIP3	9 dBm
Minimum SNR	15 dB
Channel selection ratio	50 dB
Image rejection Ratio	60 dB

2.2. Double Quadrature Down-conversion Architecture

Nowadays the most popular tuner architectures employ either the single-conversion (with bulky off-chip tracking filter) or the dual-conversion; both tuner architectures are shown in Fig. 2.6. As shown in Fig. 2.6 (a), the center frequency of the tracking filter is set according to the desired channel frequency and the desired channel is pre-selected. After this tracking filter, the image channel is attenuated and single down-conversion architecture can be used without huge image rejection ratio requirement. After the down-conversion, an off-chip SAW filter is used to achieve the desired selectivity. Because of the tracking filter, the tuner architecture is simplified. However, the tracking filter has to be programmable from

50MHz to 800MHz and it is not practical to implement it on-chip; therefore, this architecture is not suitable for integrated tuner solution.

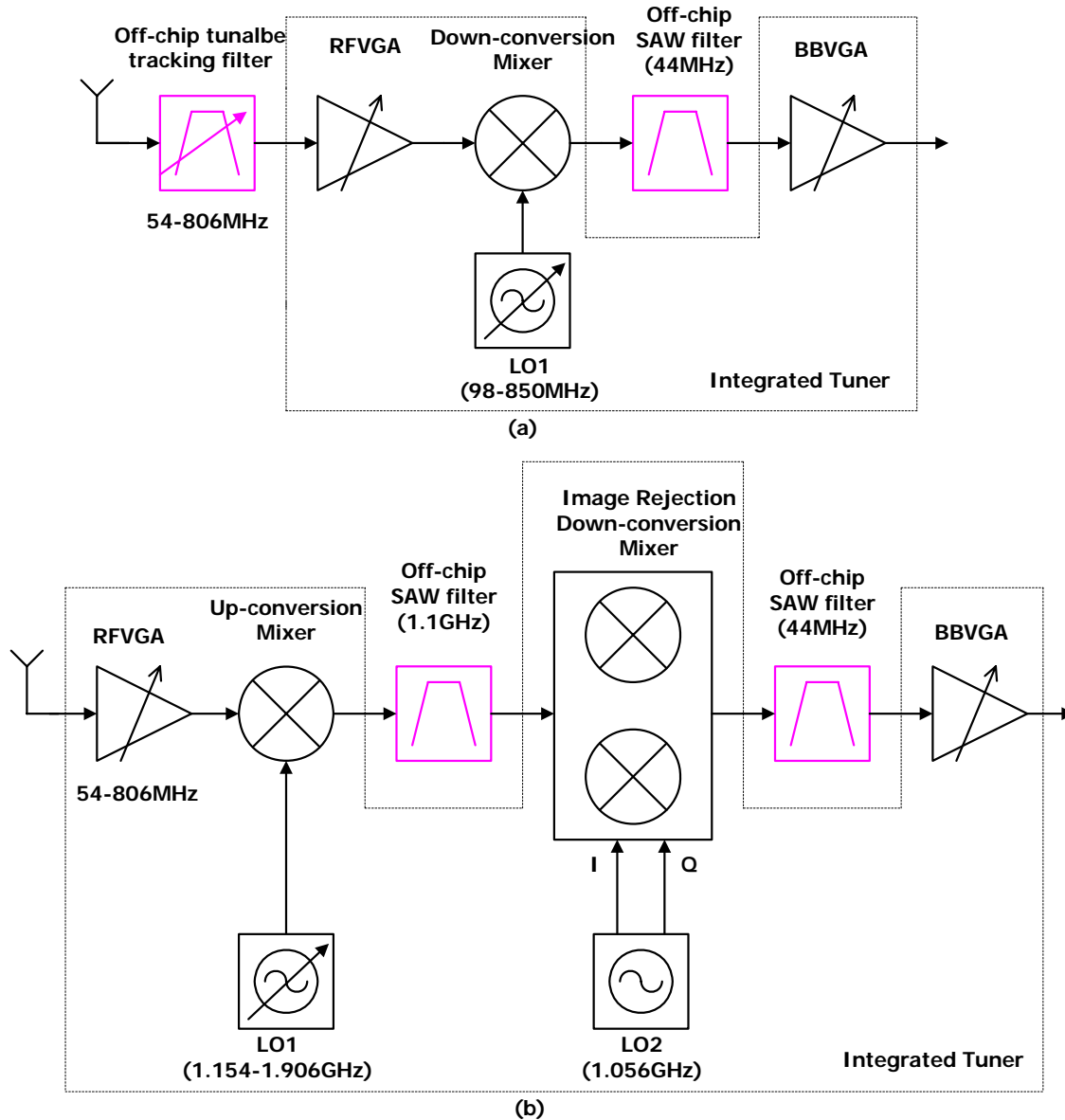


Fig. 2.6. Typical TV-Tuner architectures (a) single-conversion; (b) dual-conversion

In the dual-conversion architecture, as depicted in Fig. 2.6 (b), the desired channel is first up-converted to a high inter-mediate frequency like 1.1GHz, pre-selected by an off-chip high-Q bandpass SAW filter and then down-converted to the standard 44MHz frequency. In the first up-conversion, the frequency of the image channel is out of band and not relevant. In the second down-conversion, the image channel is fixed and 88MHz away from the desired channel. The high-Q off-chip SAW filter can attenuate this image channel by more than 30dB; the second image rejection quadrature mixer also provides more than 30dB image rejection. Therefore, over 60dB image rejection ratio can be achieved without major challenges. Without the need of bulky tracking filter, the tuner has more compact size compared with Fig. 2.6 (a). The dual-conversion architecture is the most popular solution for market available integrated DTV tuners [8]-[10]. The main drawbacks for this architecture are power consumption and requirement of off-chip SAW filter. Due to the high frequency up-conversion, the circuits work at higher frequencies (over 1GHz) and the overall tuner power consumption is usually over 1W. Unfortunately, it is hard to design an on-chip filter to replace the SAW filter and the tuner cannot be fully integrated. These two drawbacks limit this architecture's usage for future low power low cost tuner design.

In both architectures shown in Fig. 2.6, the image rejection is the key consideration. The high image rejection specification is achieved by the filtering, either variable frequency tracking filter or fixed frequency SAW filter. In principle, the image can also be rejected if image cancellation architectures like Hartley and Weaver architectures are used [11].

However, those architectures suffer from I/Q mismatch and it is not possible to achieve 60dB image rejection ratio without the use of sophisticated calibration schemes [12]. The main principle and limitation for the conventional image cancellation architecture are discussed below.

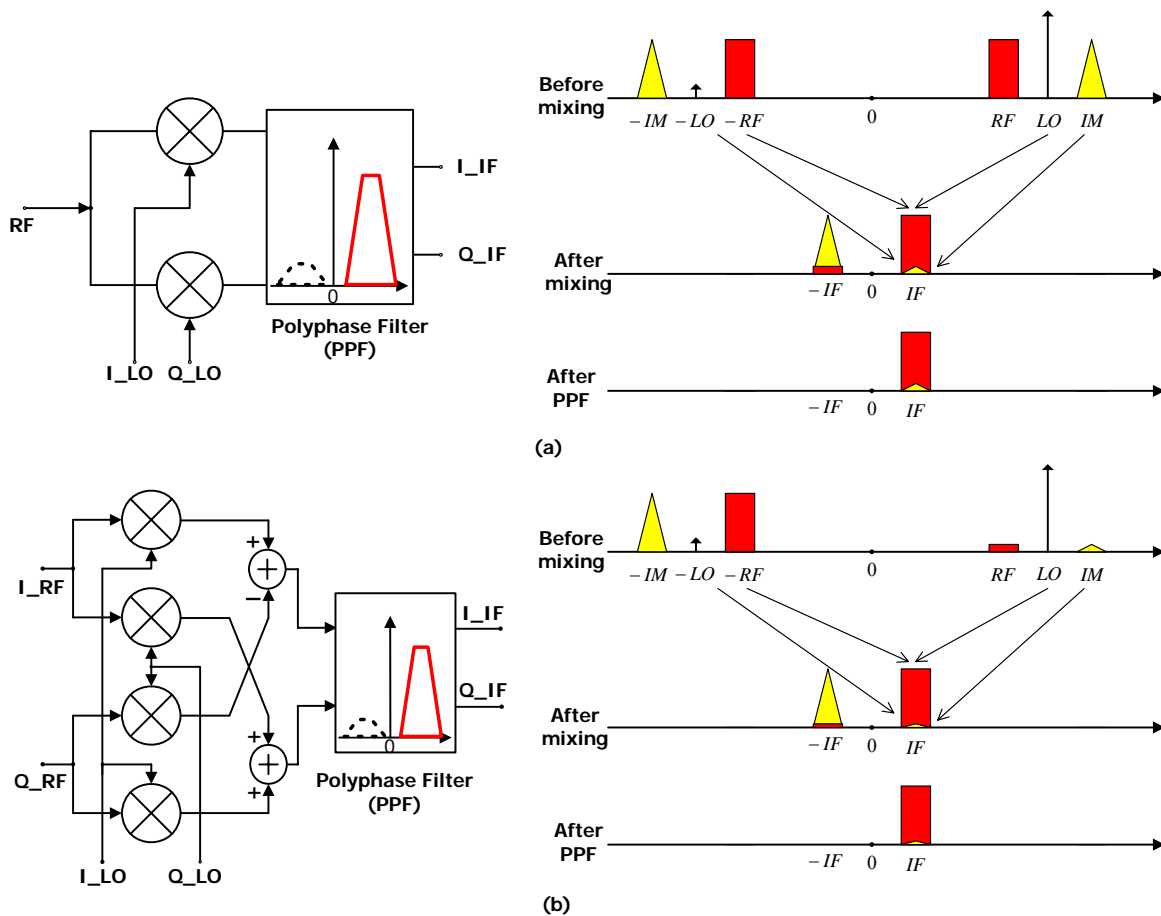


Fig. 2.7. (a) Single quadrature down-converter; (b) Double quadrature down-converter

The typical quadrature down-converter is shown in Fig. 2.7 (a), where the RF input is mixed with two quadrature mixers and the quadrature outputs of the mixer are processed by

the image rejection polyphase filter. For the analysis, the RF input can be expressed as $A_{RF} \cos(\omega_{RF}t) + A_{IM} \cos(\omega_{IM}t)$; the ideal quadrature LO signals can be described as $A_{LO} \cos(\omega_{LO}t)$ and $A_{LO} \sin(\omega_{LO}t)$. A_{RF} , A_{IM} and A_{LO} are the amplitudes of desired RF signal, image signal and LO signal, respectively. For the simplicity, the quadrature LOs can be combined and viewed as a complex LO signal $A_{LO}e^{j\omega_{LO}t}$. Thus the quadrature output of the mixer can also be expressed as $[A_{RF} \cos(\omega_{RF}t) + A_{IM} \cos(\omega_{IM}t)]A_{LO}e^{j\omega_{LO}t}$.

If $\omega_{IF} = \omega_{LO} - \omega_{RF}$, and ignoring the high frequency components ($\omega_{RF} + \omega_{LO}$ and $\omega_{IM} + \omega_{LO}$),

the output can be further simplified as $\frac{1}{2}A_{RF}A_{LO}e^{j\omega_{IF}t} + \frac{1}{2}A_{IM}A_{LO}e^{-j\omega_{IF}t}$. Therefore, after the

down-conversion the desired RF signal and undesired image signal are separated as positive IF and negative IF. The polyphase filter after the mixer can eliminate the negative frequency components and keep the positive frequency ones only. Usually image rejection

ratio is defined as $\frac{P_{image}}{P_{signal}}$, where P_{image} is the image signal power at the final output and

P_{signal} is the desired signal power at the output. Therefore, the overall image rejection ratio only depends on the attenuation ratio provided by the polyphase filter.

However, practical devices mismatches and process parameter tolerances limit drastically its performance. Fig. 2.7 (a) graphically shows the effect of the LO quadrature mismatch. In the ideal case, the spectrum of the complex LO will be only one tone (positive LO); the mismatch of the LOs generate an undesired negative LO component. This undesired

negative LO mixes with undesired positive image signal and the product falls in desired positive IF frequency, which cannot be filtered away by the polyphase filter. Even if the polyphase filter has infinite attenuation, the achievable image rejection ratio is still limited as

$$IRR \approx \frac{1}{4} \left[\left(\frac{\Delta A}{A} \right)^2 + (\tan(\Delta\Phi))^2 \right] \quad (3)$$

where ΔA is the overall gain mismatch between the I/Q paths and A is the nominal gain, $\Delta\Phi$ is the overall phase imbalance in radians. Both ΔA and $\Delta\Phi$ are determined by the LO and mixer's mismatches as shown below

$$\begin{aligned} \frac{\Delta A}{A} &\approx \frac{\Delta A_{LO}}{A_{LO}} + \frac{\Delta G_{mixer}}{G_{mixer}} \\ \tan(\Delta\Phi) &\approx \tan(\Delta\Phi_{LO}) + \tan(\Delta\Phi_{mixer}) \end{aligned} \quad (4)$$

where the LO signals are modeled as $A_{LO} \cos(\omega_{LO}t)$ and $(A_{LO} + \Delta A_{LO}) \cos(\omega_{LO}t + \Delta\Phi_{LO})$, and the mixer gains are modeled with $G_{mixer} e^{j\Phi_{mixer}}$ and $(G_{mixer} + \Delta G_{mixer}) e^{j(\Phi_{mixer} + \Delta\Phi_{mixer})}$. Usually the LO amplitude mismatch is small compared with mixer gain mismatch, also the mixer's phase imbalance is negligible compared with LO's phase imbalance. To achieve 60dB image rejection ratio, both LO phase mismatch and mixer gain mismatch should be less than 0.1 degree and 0.1%, respectively. The mixer's gain mismatch can be minimized by using a proper architecture like passive mixer and good layout techniques, but the LO phase imbalance is usually over 1 degree, which implies no more than 40dB image

rejection. Therefore, to achieve over 60dB image rejection ratio, double quadrature architecture, which can relax the matching requirement of the LO, is preferred [13]-[14].

As shown in Fig. 2.7 (b), the double quadrature architecture handles the down-conversion with complex LO and complex RF. Four mixers instead of two mixers are needed to achieve complex mixing as shown in the equation below

$$I_{IF} + jQ_{IF} = (I_{RF}I_{LO} - Q_{RF}Q_{LO}) + j(I_{LO}Q_{RF} + Q_{LO}I_{RF}) \quad (5)$$

Because the RF input is complex, only the negative frequency components (desired RF and undesired image signals) are present at the input of the mixer. Considering the mismatch between quadrature RF signals, part of the positive frequency components will be pre-filtered before the mixing. Therefore, the undesired product due to negative LO and positive image, which cannot be filtered away by the complex filter as pointed earlier, will be much smaller than the counterpart in the conventional single quadrature architecture shown in Fig.2(a). The overall gain mismatch and phase imbalance for double quadrature architecture can be obtained below

$$\frac{\Delta A}{A} = \frac{\Delta A_{RF}}{A_{RF}} \frac{\Delta A_{LO}}{A_{LO}} + \frac{\Delta G_{mixer}}{G_{mixer}} \quad (6)$$

$$\tan(\Delta\Phi) = \tan(\Delta\Phi_{RF}) * \tan(\Delta\Phi_{LO}) + \tan(\Delta\Phi_{mixer})$$

Therefore, to achieve 60dB image rejection ratio, assuming 0.1% mixer gain mismatch, only 2.4 degree phase imbalance and 3% gain mismatch are required for the quadrature RF and LO, which can be easily achieved.

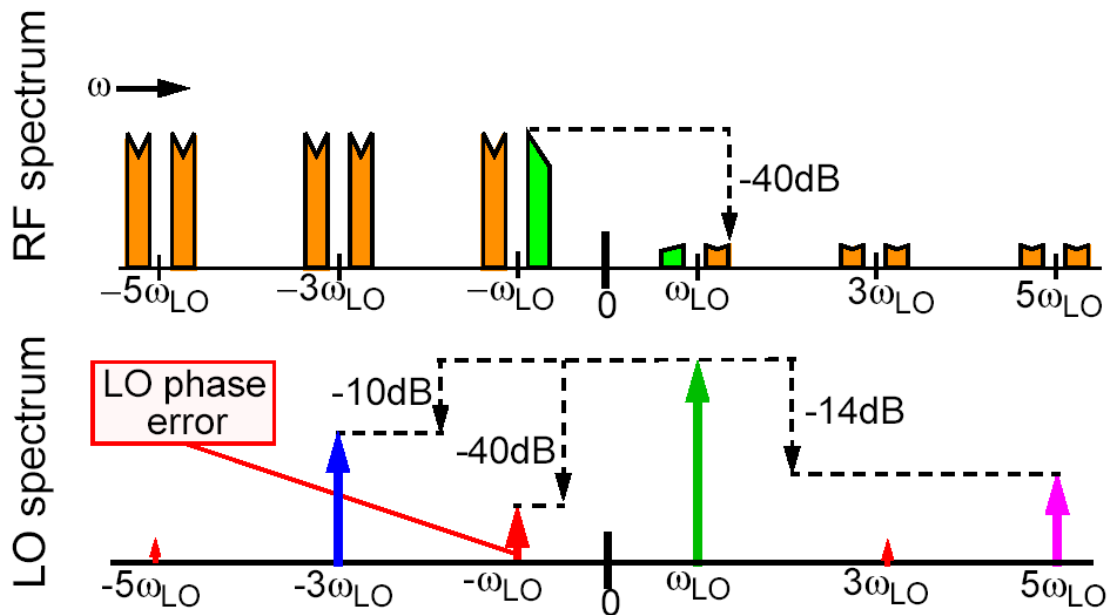


Fig. 2.8. Harmonic suppression of double quadrature down-converter

In addition to the high image rejection ratio, the double quadrature down-converter provides inherent third order harmonic suppression, which is illustrated in Fig. 2.8. For the ideal quadrature LO (square wave), only $(4n-3)\omega_{LO}$ appear in the positive frequency side and $-(4n-1)\omega_{LO}$ appear in the negative frequency side, where n is the integer (≥ 1). Therefore, $3\omega_{LO}$ is missing in the spectrum and the third order harmonic mixing can be avoided in ideal case. However, the $5\omega_{LO}$ component appears with only -14dB attenuation. Hence, fifth order harmonic mixing issue needs to be considered in the system design.

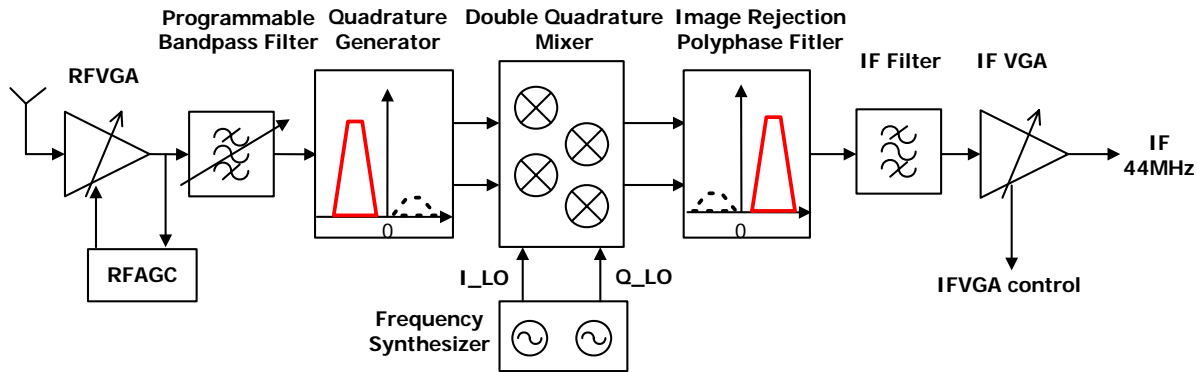


Fig. 2.9. Double quadrature DTV tuner architecture

Based on the double quadrature architecture, single-conversion DTV tuner architecture can be built; the block diagram is shown on Fig. 2.9. Off-air DTV signal is firstly received by the antenna and pre-filtered by an external filter (not shown in the figure), which removes the out-of-the DTV band interferences. A wideband on-chip low noise variable gain amplifier is used as a front-end and it must provide two functions. First, the gain of the LNA should be adjusted to ensure that the following stages will not be saturated by the output signal of the LNA; for that purpose the LNA operates as a variable gain amplifier. Second, this amplifier needs to convert the single-ended input signal into differential signal with good differential matching properties. Differential signals are required not only because of better common mode rejection but also the requirement of the quadrature generation. In this implementation, the quadrature generator is designed with passive polyphase filter [15], which requires differential inputs to generator quadrature output. The quality of the differential signal affects the matching performance of the quadrature output and eventually degrades the overall image rejection ratio.

The programmable bandpass filter serves to suppress the harmonic components. In this broadband system, the harmonics of the LO ($n \times LO$) will mix with in-band interference channels ($n \times LO + IF$) and generate additional undesired images, which cannot be filtered by the baseband filter and degrades the output quality. The double quadrature down-converter provides inherited 3rd harmonic suppression as described above, and the programmable bandpass filter removes those $5LO + IF$ interferences and achieves 5th harmonic suppression. In addition, the programmable filter can also serve as rough band selection and relax the following stages linearity challenges.

After image rejection due to IF complex filter, some baseband blocks including the baseband filter and a low-frequency variable gain amplifier are used to further reject the out of band signals and amplify the desired signal before the conversion of the selected channel to digital format. With double quadrature down-conversion architecture, 60dB image rejection ratio is achievable without requiring any bulky tracking filters or high frequency off-chip SAW filter. This will greatly reduce manufacture cost and power consumption.

2.3. Double Quadrature Down-converter Design

Currently, most of the integrated terrestrial and cable DTV tuners are built employing bipolar or BiCMOS technologies [8], [10] and [16], which are more expensive than mainstream CMOS technologies. Furthermore, with the increasing demand for system integration (tuner, ADC and decoder), CMOS implementation will greatly reduce the overall silicon area, power consumption and cost. Therefore, 0.35 μ m CMOS technology is

chosen for the design of this prototype. In this chip, the main goal is to verify the image rejection concept and only the most critical blocks are designed. These blocks include a wideband (fixed gain in this prototype) LNA, double quadrature down-converter and frequency synthesizer. In this dissertation, only the double quadrature down-converter design will be covered.

2.3.1. Broadband quadrature generator

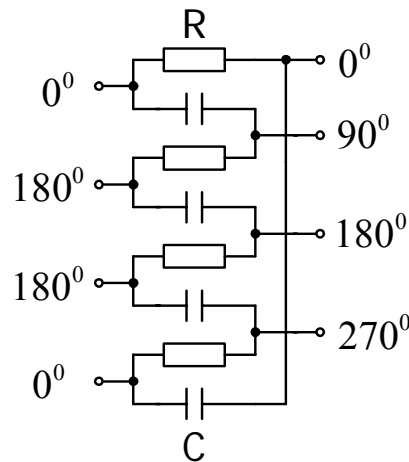


Fig. 2.10. Single stage passive polyphase filter

The broadband quadrature signal generator is the critical block of the double quadrature down-converter. In order to generate such broad band quadrature signal with less than 3% I/Q mismatch, we need a filter's attenuation of at least 40dB for the entire image frequency band from positive 50MHz up to 806MHz; these specifications can be achieved if a multi-stage passive polyphase filter is used [13]-[15]. The single stage polyphase filter is shown

in Fig. 2.10. If the differential inputs (at $\omega_0 = \frac{1}{2\pi RC}$) are applied at the input, quadrature

outputs can be generated. However, the quadrature relationship is only valid at the specific frequency ω_0 . In order to achieve the broadband quadrature generation, multiple stages are required.

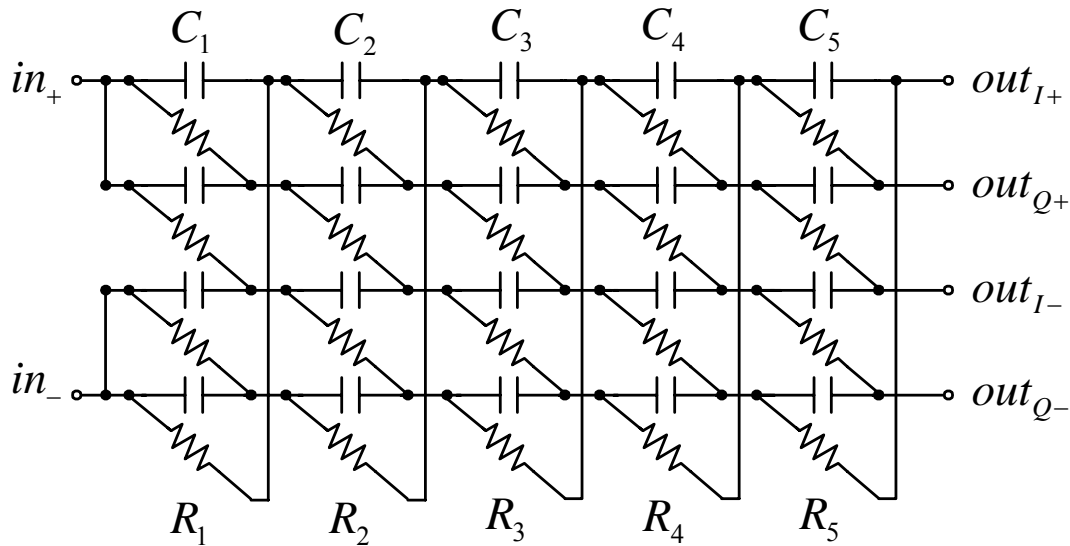


Fig. 2.11. Schematic of broadband quadrature generator

Due to the presence of the unavoidable process and temperature variations, on-chip resistors and capacitors can deviate from the nominal value and the filter must be over-designed to cover the typical 30% RC variations. Therefore five stages are required to provide multiple poles evenly distributed in log scale from 40MHz up to 1.1GHz. The complete schematic is shown in Fig. 2.11.

The design challenge of this circuit comes from the gain and noise figure requirements. This circuit is passive and does not have gain and the losses have to be minimized not to degrade the down-converter overall noise figure, which implies that the impedance for each

stage has to be tapped up from the first stage to final stage. Also due to the lossy property of this circuit, the final stage is the dominant noise source of this filter; hence small resistor value at the final stage is preferred to minimize the noise. But this constraint adds a design challenge because the previous stage of this quadrature generator needs to drive low input impedance up to 1GHz. A proper design strategy to deal with the trade-off between noise and gain is used; the components values are set as listed in Table 2.2. Notice that high frequency poles are distributed at the earlier stages to allocate smaller resistor for similar capacitance.

Table 2.2. Component values of quadrature generator

R1	C1	R2	C2	R3	C3	R4	C4	R5	C5
125 Ω	1.29pF	250 Ω	1.25pF	500 Ω	1.52pF	1000 Ω	1.85pF	2000 Ω	1.79pF

Based on this design, the frequency response for the quadrature generator is simulated and the results are shown in Fig. 2.12 (a). The positive frequency attenuation is over 40dB from 40MHz to 1.1GHz and less than -4dB attenuation is observed for the negative frequency input (desired). Here positive frequency means the phases of the inputs are counterclockwise and negative frequency means the phases of the inputs are clockwise. Alternatively, the output I/Q mismatch is less than 1% in the desired frequency range.

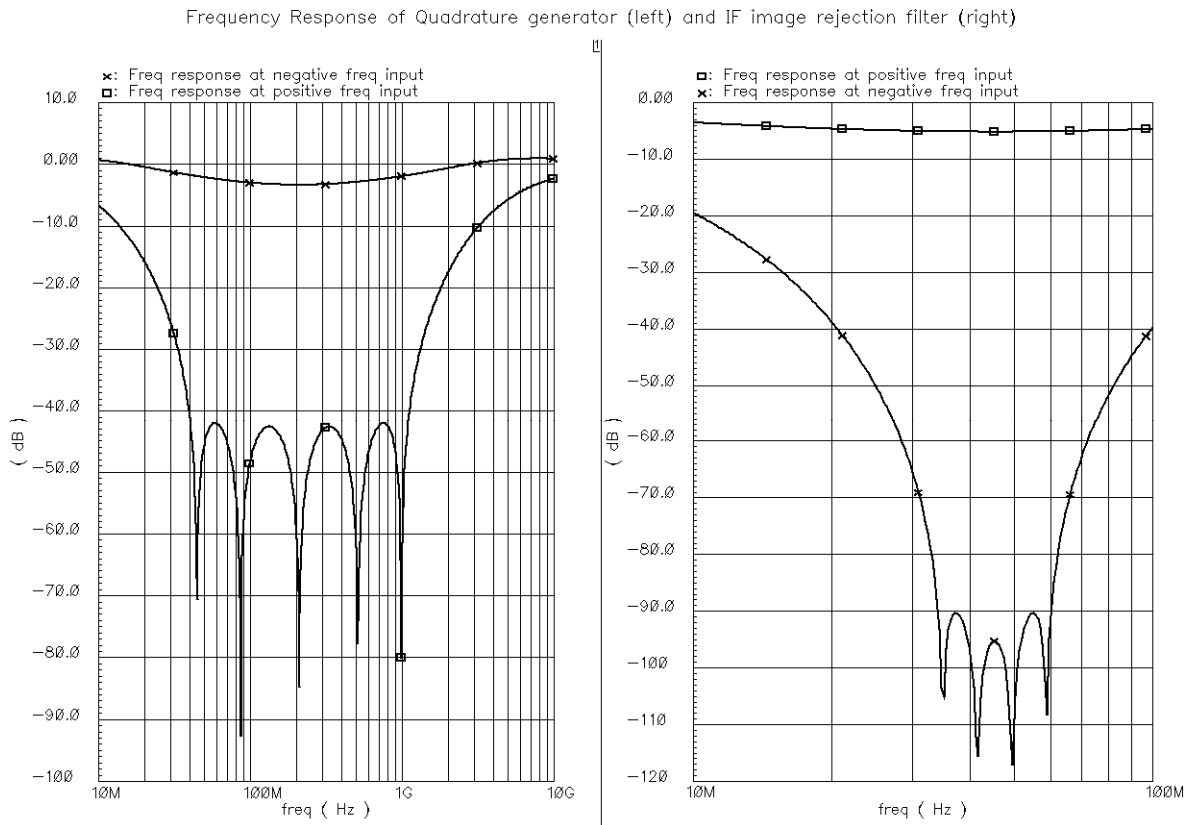


Fig. 2.12. Frequency response plot of: (a) quadrature generator; (b) image rejection filter

In addition to those variations, the mismatch between the RC components also introduces additional I/Q mismatch and eventually degrades the image rejection performance [17]. Monte Carlo simulations can verify the sensitivity between I/Q mismatch and component mismatch. 200 samples has been used and the component mismatch mean is 1% (3σ is 3%). The simulated phase error (in degree) and gain error (in dB) are provided in Fig. 2.13. The maximum phase error and gain error are 2 degree and 0.025 dB, respectively; the mean phase error and gain error are 1.47 degree and 0.009 dB, respectively. Based on these simulation results, less than 3% I/Q mismatch can be relatively easy to achieve with 1% component mismatch.

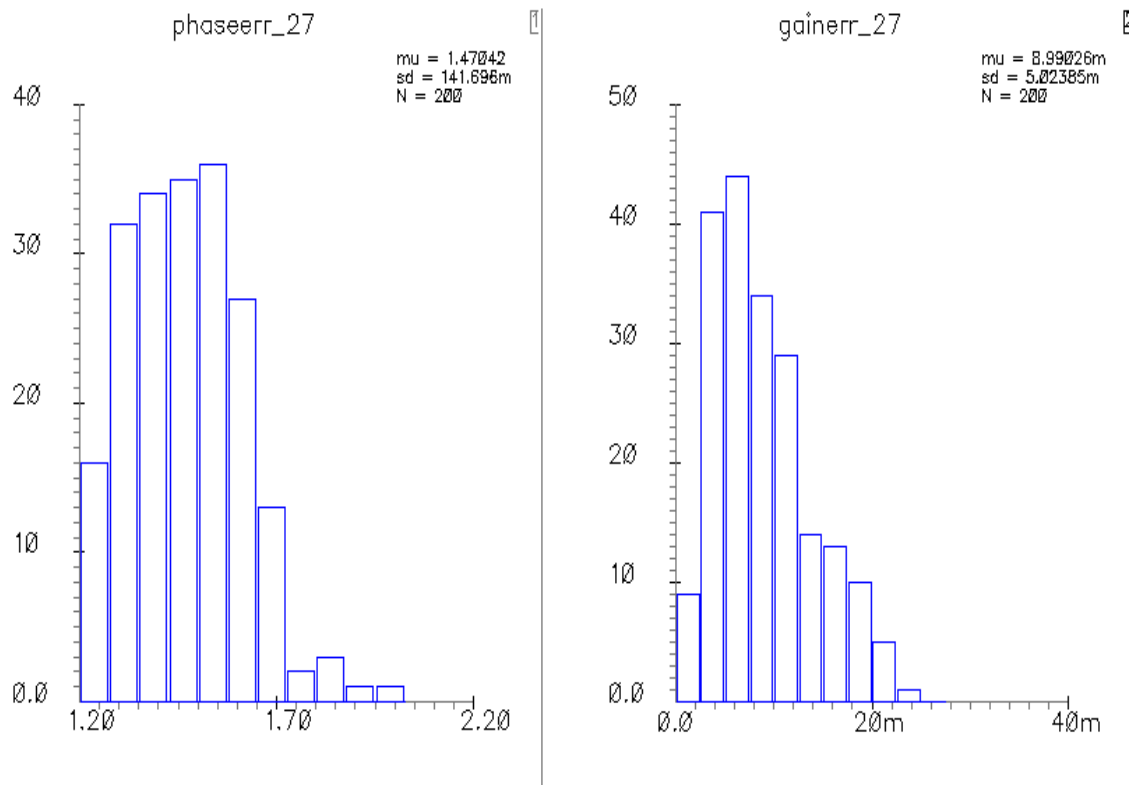


Fig. 2.13. Quadrature generator Monte Carlo simulation results

2.3.2. Image rejection polyphase filter

Similar to the quadrature signal generator, the IF image rejection filter also uses the passive polyphase filter structure. Fig. 2.14 shows the image rejection functionality with one stage polyphase filter. When the counterclockwise quadrature signals (negative frequency) are applied with, the inputs will be bypassed. When the clockwise quadrature signals (positive frequency) are applied, the signals will be suppressed. Notice that the image signal and desired signal are separated in the positive and negative frequency spectrum after the complex mixing operation. Therefore, if the RC product is chosen at the intermediate frequency (like 44MHz), image rejection at 44MHz can be achieved. For this image

rejection filter, more than 60dB attenuation over the image band (negative 41MHz to 47MHz) is required. In fact, the designed frequency band needs to be from 32MHz to 63MHz so that it can cover the desired 41MHz-47MHz band even with 30% process variations. Based on the simulation, four stages are required and the complete schematic is shown in Fig. 2.15. For the operation of the image rejection filter, the quadrature outputs of the mixer are directly connected to the four inputs of the filter (counterclockwise phase). The component values are designed following the similar design strategy used for quadrature generator and they are given in Table 2.3. The simulated frequency response is given in Fig. 2.12 (b). More than 60dB attenuation is observed from 30MHz to 70MHz for the typical process corner.

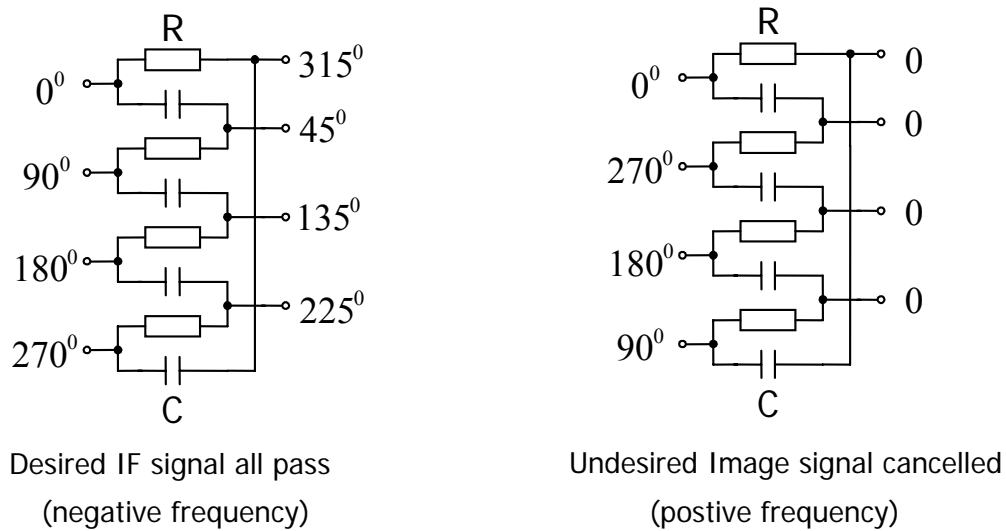


Fig. 2.14. Image rejection demonstration of single stage passive polyphase filter

The major concern of this filter is the high components' matching requirement. In the case of components mismatch, undesired image signal will be coupled to desired signal band,

which degrades the image rejection ratio; in order to ensure less than -60dBc coupling (or more than 60dB image rejection ratio), less than 0.1% component mismatch is required. The values of resistors and capacitors have been properly selected to achieve the matching requirement. Also, careful layout techniques such as common centroid, placement of dummy elements and minimization of parasitic capacitances have been used to improve the matching of components.

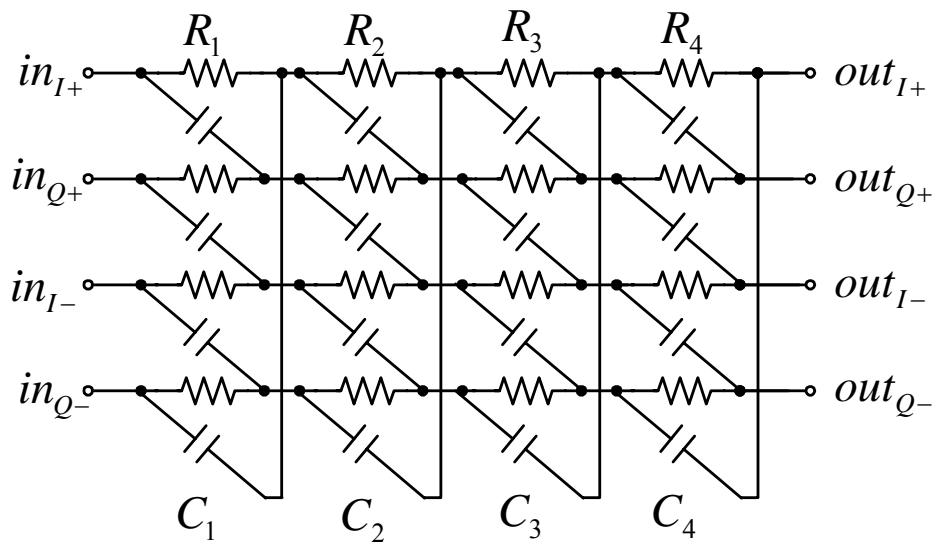


Fig. 2.15. Image rejection polyphase filter

Table 2.3. Component values of image rejection polyphase filter

R1	C1	R2	C2	R3	C3	R4	C4
250Ω	10.85pF	375Ω	8.6pF	560Ω	6.85pF	845Ω	5.4pF

2.3.3. Double quadrature mixer

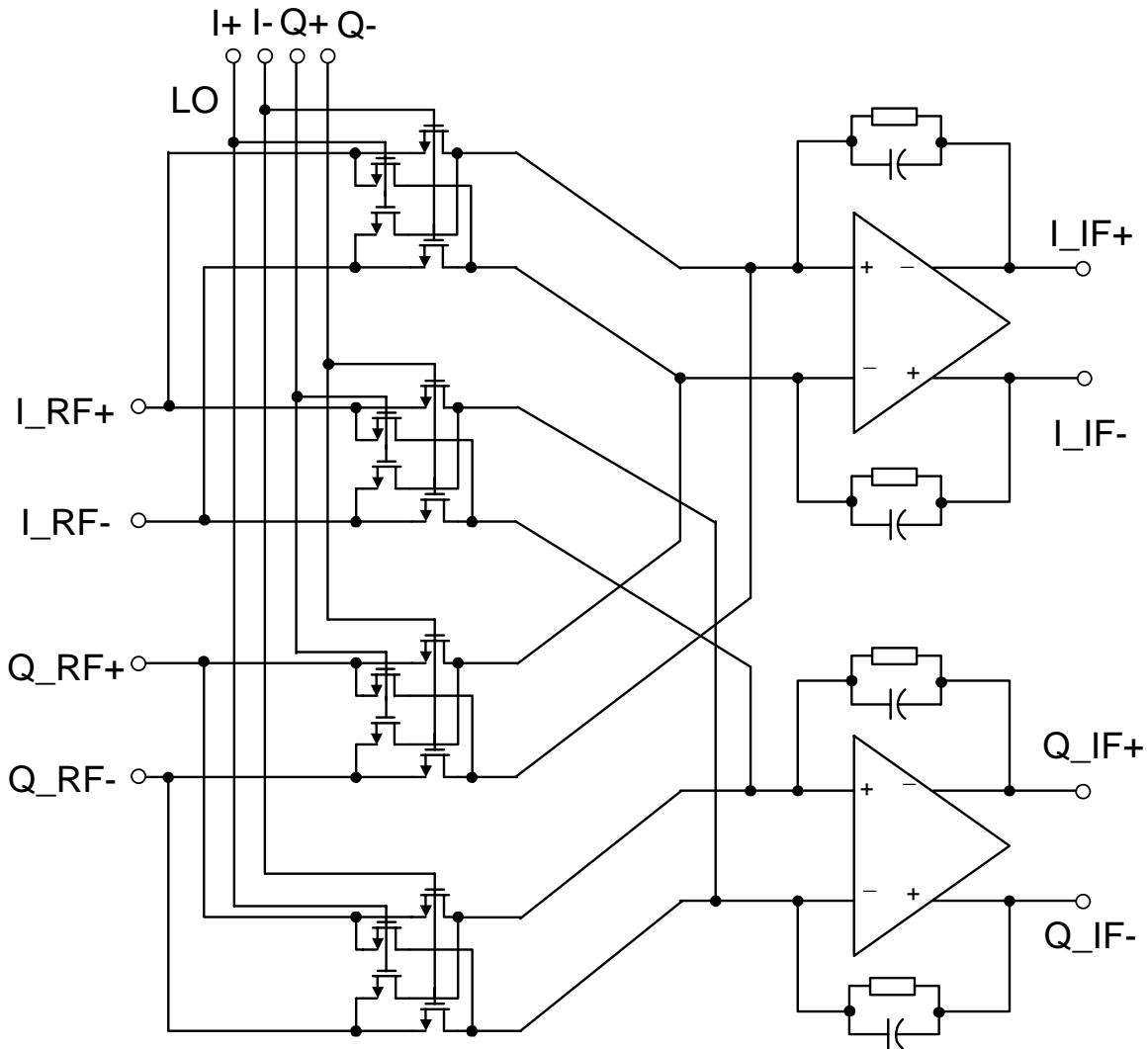


Fig. 2.16. Double quadrature passive mixer schematic

As mentioned in the previous section, the double quadrature architecture relaxes the matching requirement for the RF and LO inputs, however the matching requirement for the mixer remains as 0.1%, which is still quite challenging. The designed mixer schematic is shown in Fig. 2.16. Passive CMOS switching mixer is chosen because it has better trade-off between matching and power-consumption [13], [15]; large size transistors are used to

improve the matching of the mixer section while power consumption is not affected. In addition, resistors can be added in series with the switch (degenerated switch) to improve the matching performance of the switch.

In this double balanced switching mixer, all transistors operate as switches. When the switch is on, the on-resistance will be modulated by the LO. When the switch is off, the off-resistance will be very large and there is no signal flow. The input and LO modulated currents are combined in the OPAMP input node and converted to voltage by the negative feedback resistors. The feedback capacitors were added to provide first order filtering. If ideal LO and amplifier are assumed, the mixer's gain can be obtained as

$$G = \frac{2}{\pi} \left(\mu_n C_{ox} \frac{W}{L} \right) \left(\frac{R}{1 + sRC} \right) V_{LO} \quad (7)$$

where μ_n is the channel mobility factor and C_{ox} is the gate oxide capacitance; W/L is the aspect ratio of the switch transistor; R and C are the feedback resistor and capacitor; V_{LO} is the amplitude of the LO signal. It is apparent from (7) that the mixer conversion gain is proportional to the LO swing and feedback resistor. If properly designed, the gain of the mixer can be around 8dB. It is beneficial because it minimizes the noise contribution from the IF stages.

In the derivation above, an ideal amplifier is assumed and the conversion gain is not function of amplifier gain. If the amplifier is not ideal, the conversion gain will be affected

the amplifier gain, which has two effects. First, the matching of the double quadrature mixer will be affected. In ideal case, the matching of the mixer will be mainly defined by the matching of passive mixer and feedback passive components, which can be optimized if properly designed. However, it is difficult to design the active amplifier with enough matching performance. As a conclusion, the matching performance can be degraded by the finite gain amplifier. Second, the non-linearity of the amplifier will degrade the mixer's overall linearity performance.

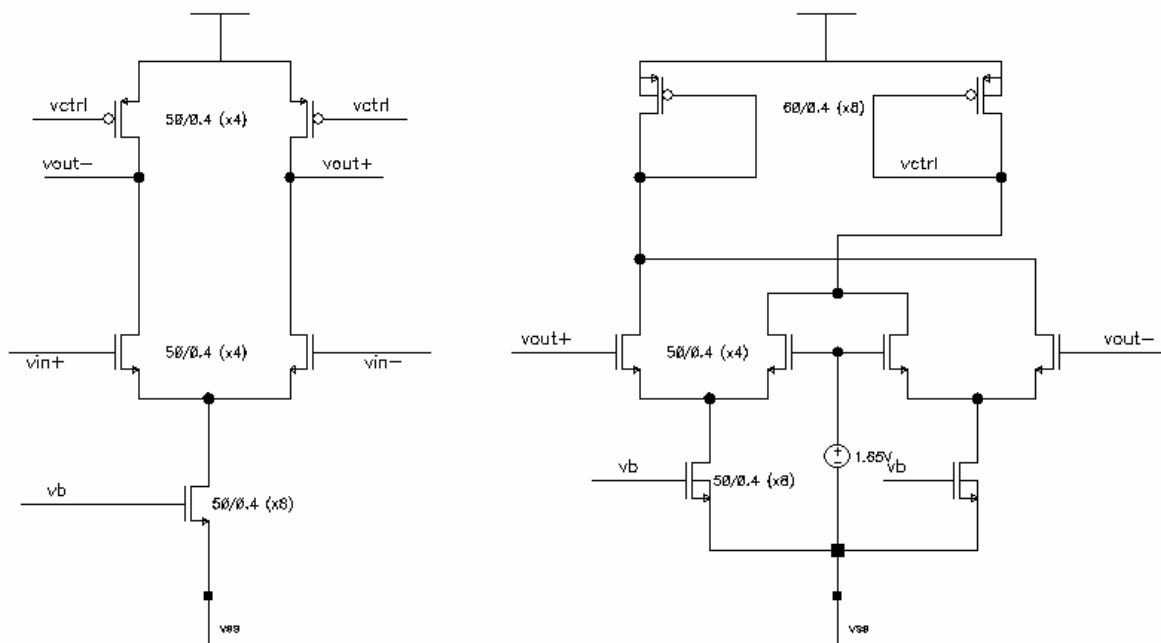


Fig. 2.17. OTA schematic

Although the high gain amplifier is desired, it is difficult to have over 40dB gain at 44MHz in $0.35\mu\text{m}$ CMOS technology. In this prototype, the amplifier is implemented with a single stage operational transconductance amplifier (OTA). The schematic of the amplifier

including the common mode feedback circuitry is shown in Fig. 2.17. The simulated OTA frequency response is given in Fig. 2.18. The OTA has over 800MHz unity gain frequency and the gain at 50MHz is around 24dB. With more advanced technologies such as $0.18\mu\text{m}$ CMOS, it is expected to achieve better amplifier performance.

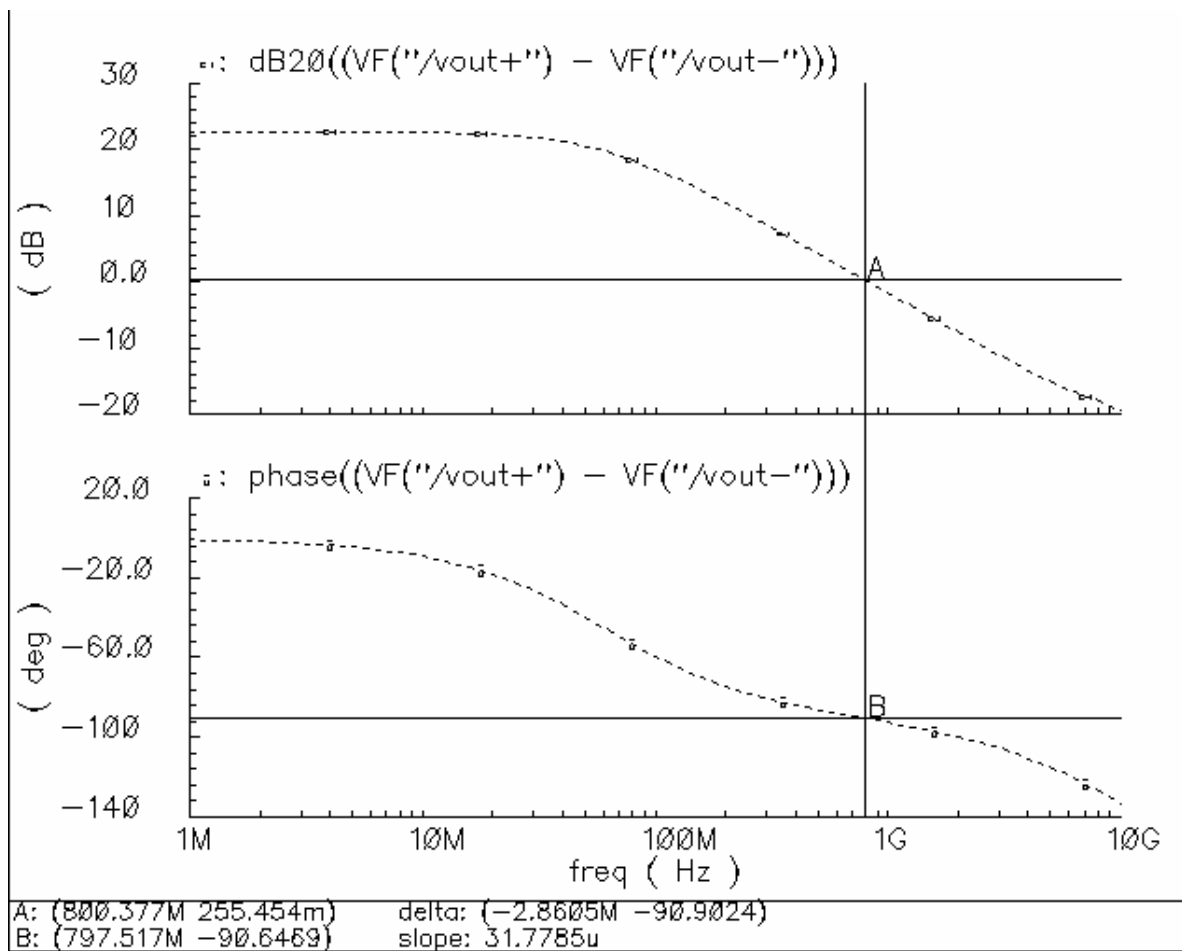


Fig. 2.18. Frequency response of the OTA

Using basic noise analysis techniques, the mixer's overall input referred noise power spectral density (including the OTA) can be obtained as

$$v_{n_in}^2 = 4KT \frac{1}{g_0} + KT \frac{\pi^2 (1+sRC)^2}{g_0^2 R} + \frac{\pi^2 v_{n_OTAin}^2 G_{mOTA}^2}{4g_0^2} \quad (8)$$

where $g_0 = \mu_n C_{ox} \frac{W}{L} V_{LO}$; K is the Boltzmann constant and T is the absolute temperature;

the OTA input referred noise voltage spectral density and overall transconductance are denoted as v_{n_OTAin} and G_{mOTA} , respectively. The dominant noise sources of this mixer are the switches and OTA, which can be minimized by reducing both switch on-resistance and input referred noise of the OTA.

As described in equations (7) and (8), high swing LO can help to increase the mixer gain and reduce the noise figure. In this design, the LO signal can be provided by the on-chip frequency synthesizer or externally. In both cases, $2f_{LO}$ signal is first divided by two to generate quadrature LO signal and multiple stages inverter are used to drive the LO signal for mixer.

2.3.4. Inter-stage buffer design and overall down-converter

Due to small input impedance of polyphase filter and mixer, inter-stage buffer is required to drive the circuitry without significant gain degradation. The buffer needs to be low noise and high linearity. The high linearity is extremely critical because the down-converter requires high linearity. Therefore, the buffer is implemented with a source degenerated differential pair, which is shown in Fig. 2.19. The load resistor is 160Ω and degeneration

resistor is 40Ω . The differential pair transistor size is $360\mu\text{m}/0.6\mu\text{m}$ and the tail current is 3.8mA .

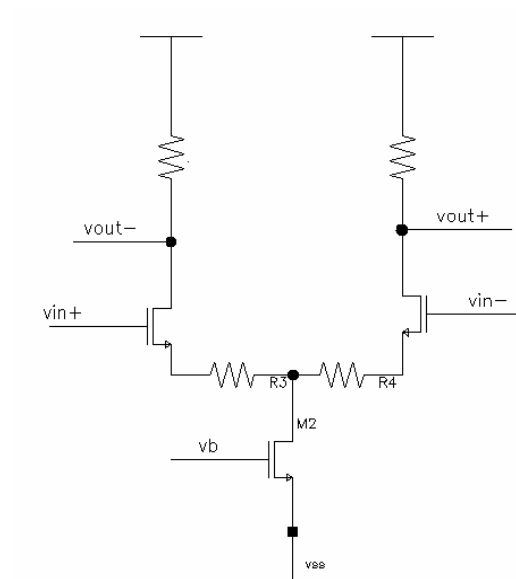


Fig. 2.19. Inter-stage buffer schematic

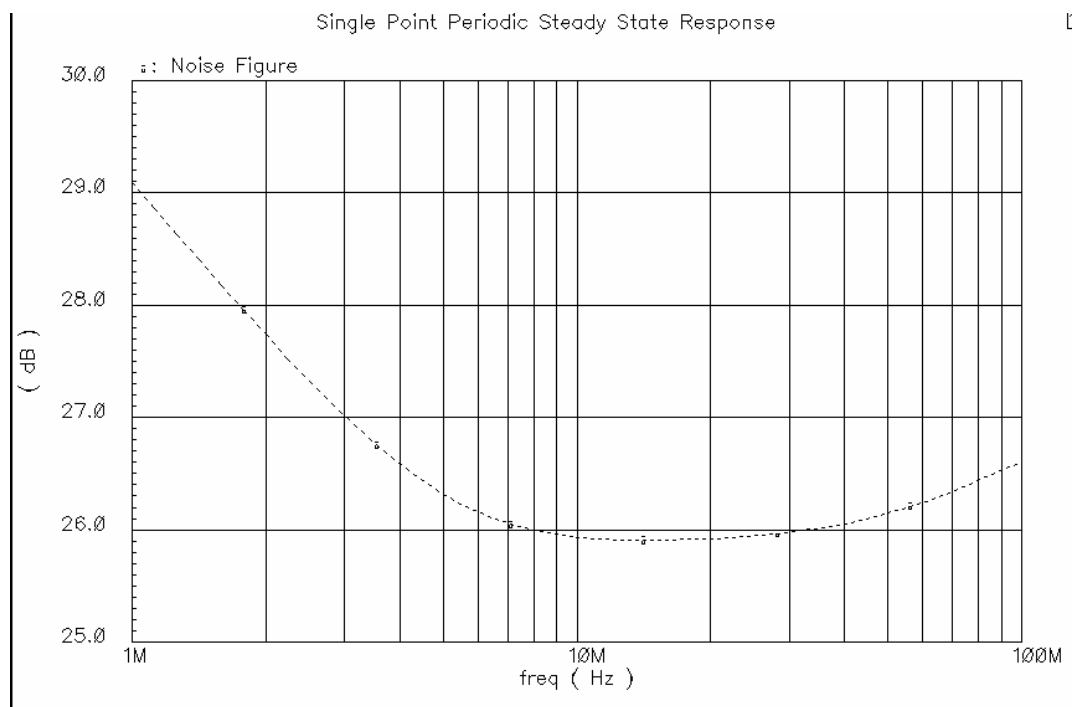


Fig. 2.20. Overall down-converter noise figure plot

The overall down-converter including quadrature generator, double quadrature mixer and image rejection polyphase filter was simulated. The gain, noise figure and IIP3 are -4dB, 20dB and 10dBm, respectively, which are also shown in Fig. 2.20 and Fig. 2.21.

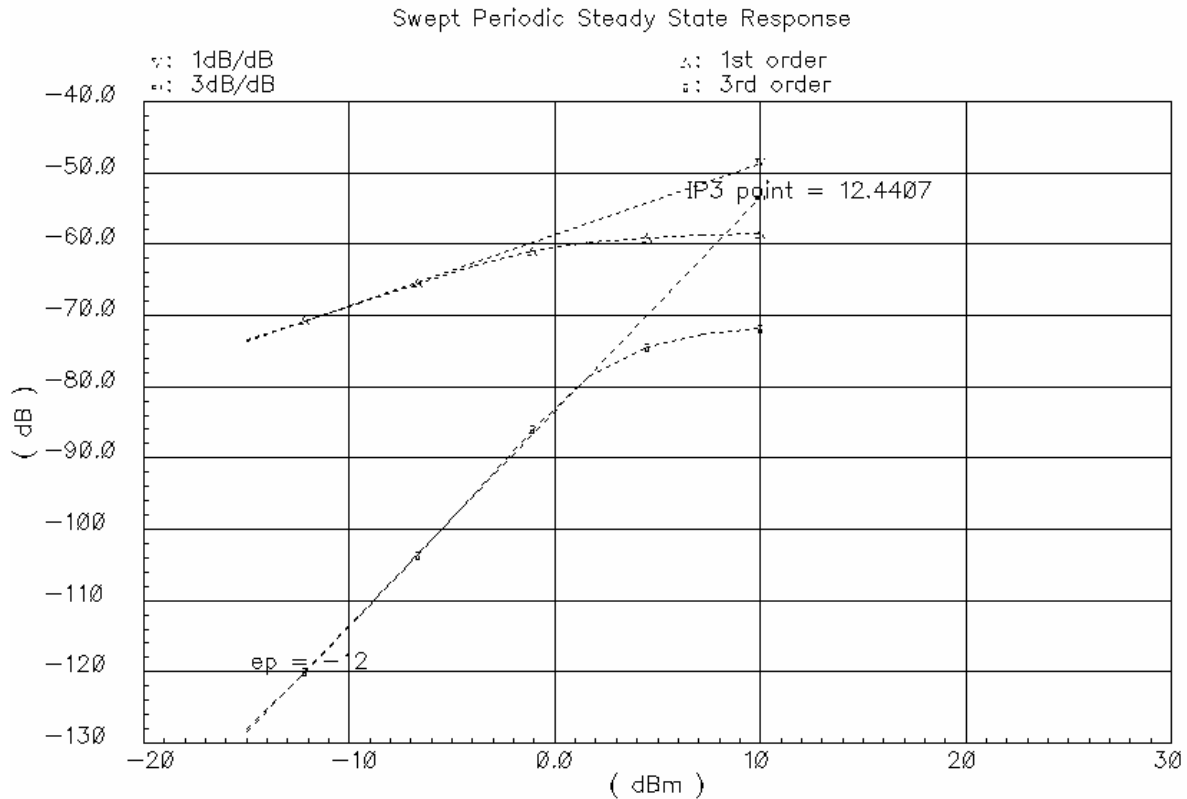


Fig. 2.21. Overall down-converter IIP3 plot

2.4. Experimental Results

In order to validate the design aforementioned, a test chip has been fabricated in the TSMC 0.35 μ m technology through the MOSIS educational program. The chip photograph is shown in Fig. 2.22. The frequency synthesizer including four on-chip inductors are on the top side of the die and the low noise amplifier is on the left bottom side; the down-

converter is implemented on the middle and right bottom. The total active area for this die is roughly $3.5\text{mm}\times 3.5\text{mm}$ and packaged with TQFP100A. To test the chip, careful PCB design has been made, especially for high frequency paths such as the RF inputs and external LO input.

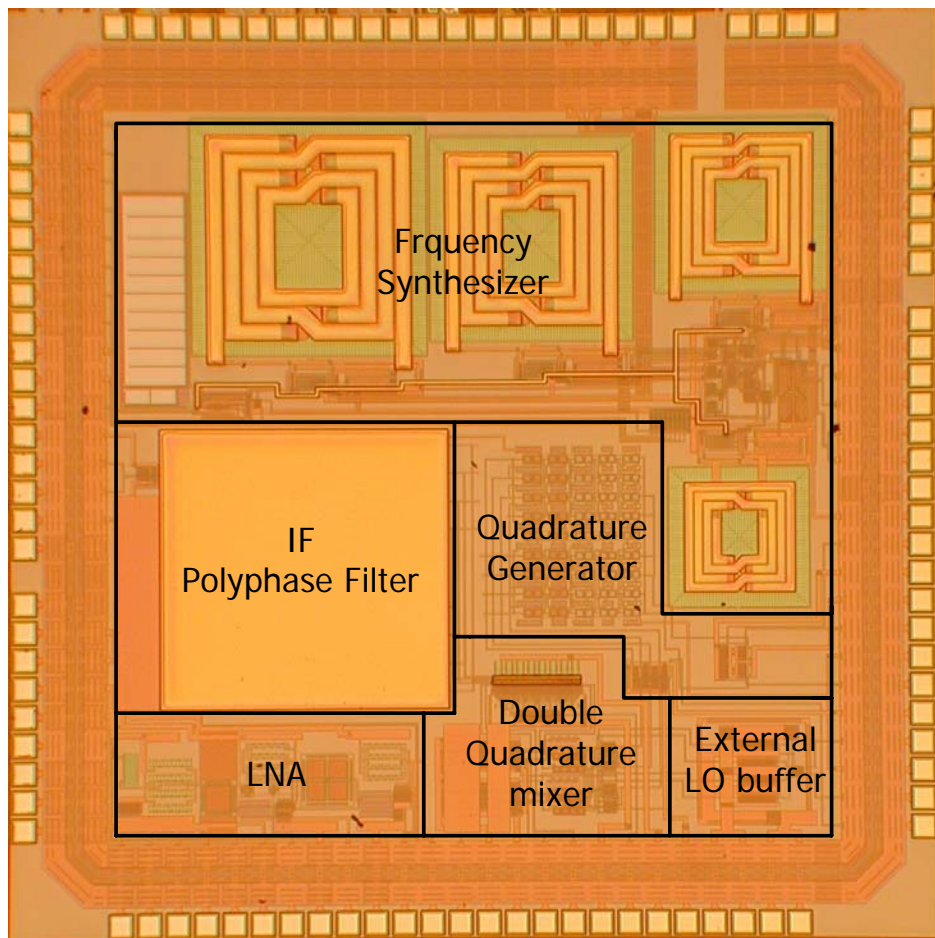


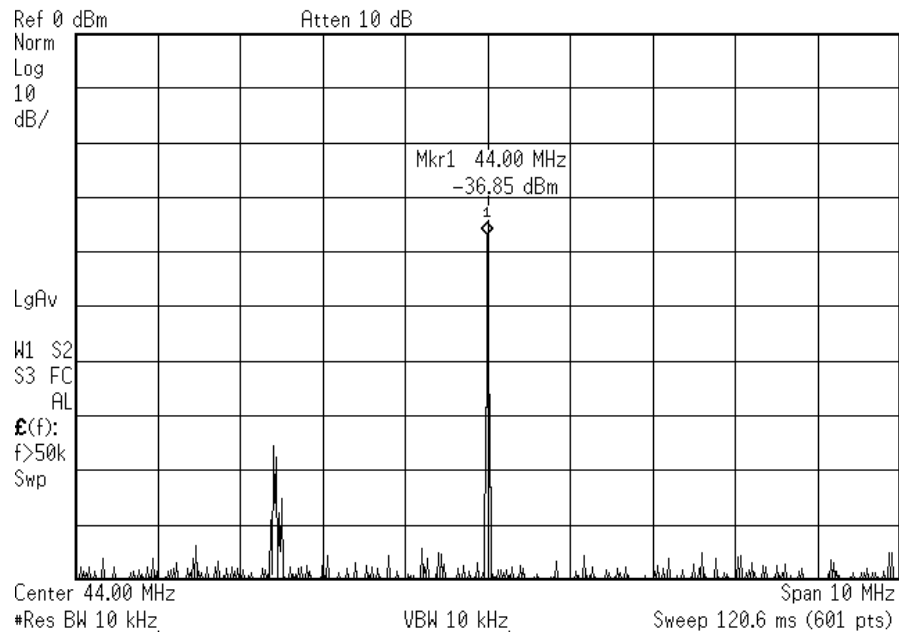
Fig. 2.22. Photograph of the terrestrial tuner test chip

The most important parameter for the down-converter is the image rejection ratio. In order to measure the image rejection ratio, same power level desired RF input and undesired image signal need to be applied in the down-converter RF input separately. The external

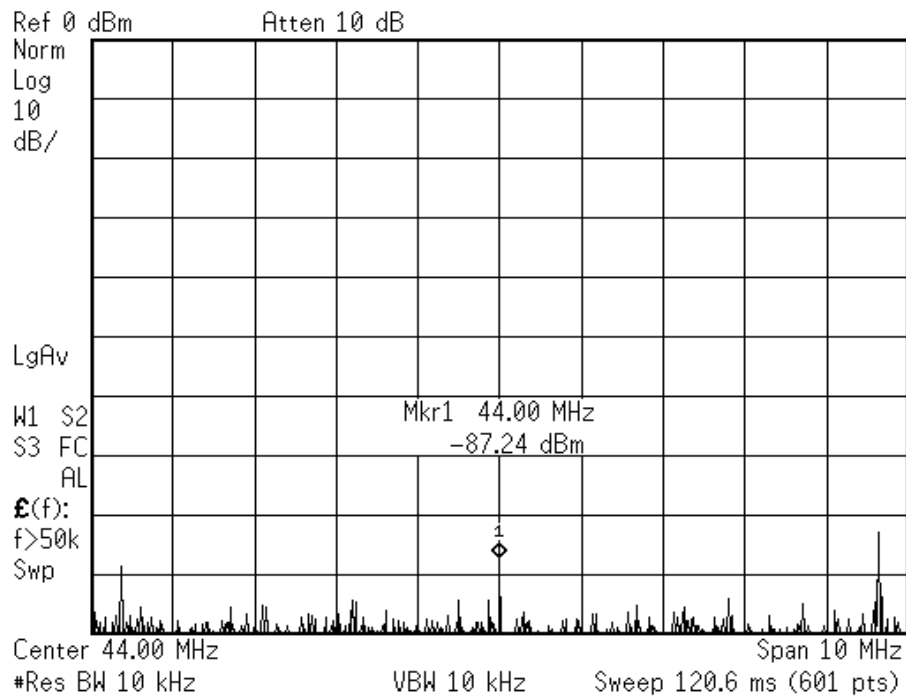
LO input is provided so that the output frequency will be 44MHz. For example, the image rejection ratio at 200MHz is measured as follows. First, a 200MHz signal with -20dBm power level is applied to the RF input and the LO is set as 244MHz. The output spectrum is shown in Fig. 2.23 (a) and the power of output signal (44MHz) is -36.85dBm. Second, the image signal (288MHz) is applied with same input power level and the LO is still set as 244MHz. The output power spectrum is shown in Fig. 2.23 (b) and the output power at 44MHz is -87.24dBm. The output power difference is the measured image rejection ratio, which is 50dB in this case.

Similar procedure has been carried out for the entire DTV band and the broadband image rejection ratio is given in Fig. 2.24. For most of the frequencies, the image rejection ratio is over 40dB. Although it is still less than our expected rejection requirement, this prototype is better than conventional single quadrature down-converter which usually cannot achieve more than 40dB image rejection ratio.

The remaining parameters for the down-converter including gain, NF and IIP3, in addition to the front-end LNA measured parameters are given in Table 2.4. Those measured values agree with the simulations and they are suitable for the terrestrial tuner applications. This prototype failed to get measurement result for the frequency synthesizer because the output buffer did not operate properly. Excluding the frequency synthesizer, the LNA and down-converter consume around 300mW power consumption with a 3.3v power supply.



(a)



(b)

Fig. 2.23. Output spectral plots @ LO 244MHz: (a) -20dBm RF input @ 200MHz; (b) -20dBm RF input @ 288MHz



Fig. 2.24. Measured image rejection ratio vs. frequency

Table 2.4. Prototype measurement summary

Parameter	Value
S11	-7dB
LNA Gain	22dB
LNA NF	4.5dB
LNA differential phase error	$\pm 1.5^\circ$
LNA differential magnitude error	± 0.65 dB
Down-converter gain	-6dB
Down-converter NF	20dB
Down-converter IIP3	7dBm
Image rejection ratio	45dB
Total power consumption	300mW

2.5. Conclusion

In this chapter, the ATSC terrestrial DTV tuner system has been introduced briefly and system level specifications were obtained. A low power low cost architecture has been adopted based on the double quadrature down-converter. The circuit design trade-off for the critical blocks has been discussed and the prototype chip was fabricated with low cost TSMC 0.35um CMOS technology. Measurement results of the blocks mostly validate our design. This prototype demonstrates that, by using the double quadrature architecture, fully integrated terrestrial DTV tuner can be designed with less power consumption and lower manufacturing cost.

CHAPTER III

MOBILE DTV (DVB-H) TUNER SYSTEM DESIGN

3.1. Introduction

With the ever-increasing demands for personal multimedia services, the mobile Digital TV (DTV) became very popular recently. TV is the biggest media and the last one missing from mobile phones. This emerging mobile DTV service allows the real time digital television program to be watched in the handset devices, “all on the go”, as shown in Fig. 3.1. For example, for the business users and travelers, it can delivery real time stock charts, weather forecast, news, etc., which is quite attractive.



Fig. 3.1. Mobile DTV applications

Currently there are multiple DTV standards suitable for the worldwide mobile application. DVB-H standard is the most popular one used in Europe and USA. ISDB-T and DMB are

mainly used in Japan and Korea. One of the critical parts for the DTV reception is the high performance DTV tuner. It receives broadband mobile DTV channels and converts the desired TV channel to baseband with enough quality for future signal processing (demodulation and decoding) and display the image on the LCD panel. Certainly the tuner suitable for multi-stand is the ultimate goal, but during the initial phase of this application, the tuner is mainly designed for a single standard and this research targets for the DVB-H standard. But without any doubt, this design methodology can be applied to other standards.

In the second section of this chapter, the DVB-H system is described and the main specifications for tuner are discussed. In the third section, the direct conversion architecture is introduced after the comparison of several architectures. In the fourth section, the main design specifications for the each building block are given.

3.2. DVB-H System and Mobile DTV Tuner

3.2.1. DVB-H and DVB-T system

In 1997, the DVB-T (Digital video broadcasting-Terrestrial) is published from the DVB Project (an industry-led consortium) for off-air digital television broadcasting. Recently, due to increasing demand for personnel multimedia services, combing the most two successful consumer electronic products (cell phone and TV) becomes attractive. One way is to carry DTV data in the mobile data from base station and it does not require any extra network. However, that will require extra bandwidth and have several potential limits.

Therefore, a terrestrial broadcasting network is preferred, as shown in Fig. 3.2. However, the original DVB-T standard is not suitable for the emerging market because of huge power consumption and the hostile reception environment (Doppler Effect). Therefore, based on original DVB-T standard, the DVB-H (Digital Video Broadcasting–Handheld) has been proposed [5].

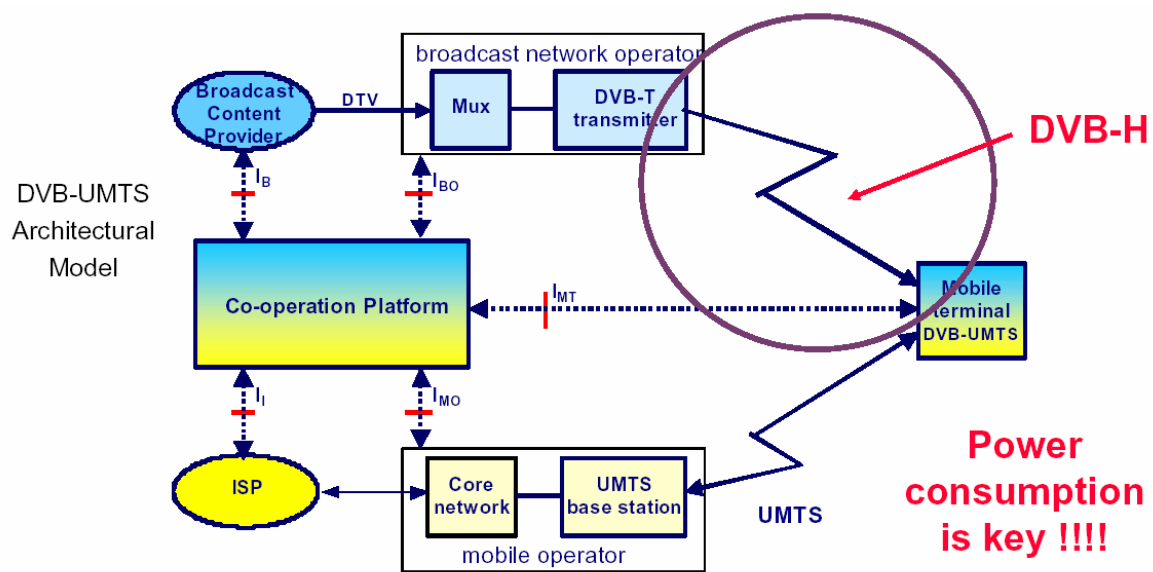


Fig. 3.2. DTV for mobile terminal

The DVB-H system is fully compatible with DVB-T network and system to make use of the existing facilities. A block diagram of using a DVB-H system is given in Fig. 3.3 [5]. The DVB-H data is sharing the MUX with MPEG2 TV service and transmitted with OFDM modulation scheme. Inside of the OFDM modulator, in addition to original 2k and 8k OFDM carrier numbers, a 4k option is added. For each carrier, the constellation scheme can be QPSK, 16QAM or 64QAM, depending on the service requirement. The transmitted channel bandwidth is programmable from 6MHz to 8MHz. The most important feature is

the power saving provided by time-slicing technique, which means the data is transmitted in burst mode and the receiver only needs to be turned on during the burst reception time to save up to 90% power consumption. In addition, the added forward error correction functionality (MPE-FEC) provides more robustness against the hostile mobile reception environment.

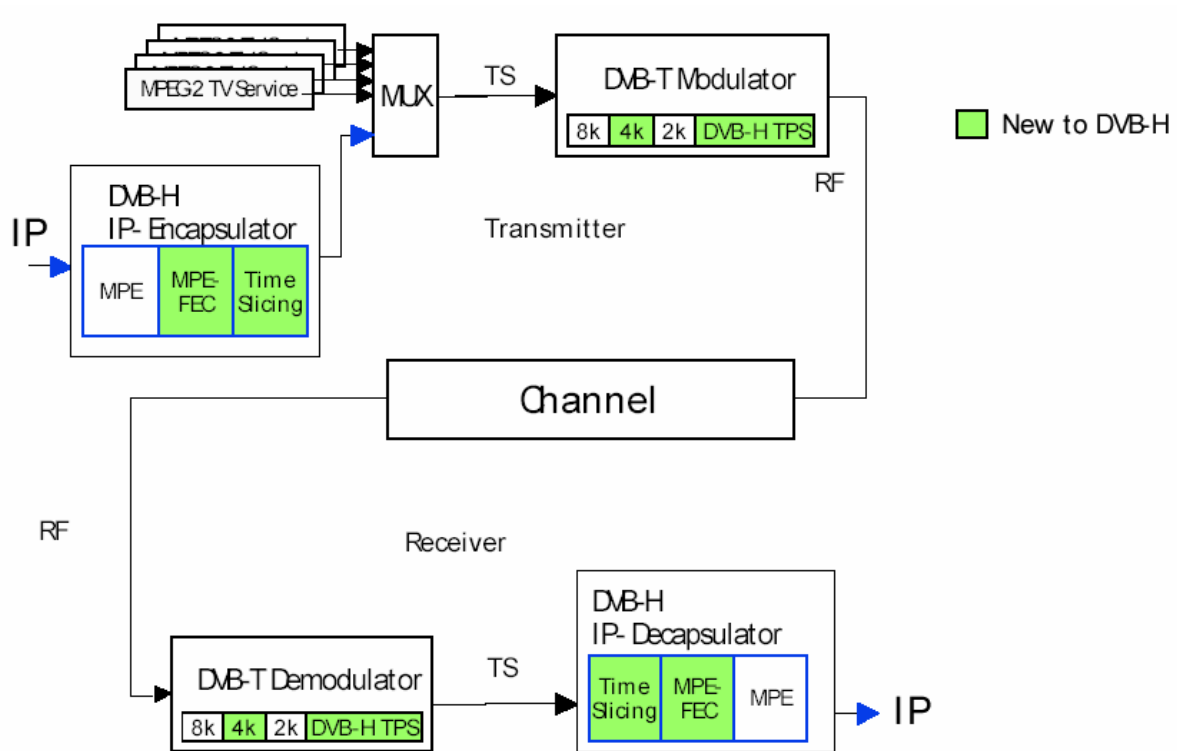


Fig. 3.3. DVB-H system block diagram

3.2.2. Frequency plan

The DVB-H system utilizes part of the frequency range used for DVB-T and the channel bandwidth can be 6MHz, 7MHz and 8MHz, depending on the region. Specifically, for the 8MHz channel bandwidth case, the channel center frequency can be expressed as

$$f_c = 474\text{MHz} + (N - 21) \times 8\text{MHz} + f_{\text{offset}} \quad (9)$$

where $N = \{21, \dots, 69\}$.

For the 6MHz channel bandwidth case, the channel center frequency can be expressed as

$$f_c = 473\text{MHz} + (N - 14) \times 6\text{MHz} + f_{\text{offset}} \quad (10)$$

where $N = \{14, \dots, 83\}$.

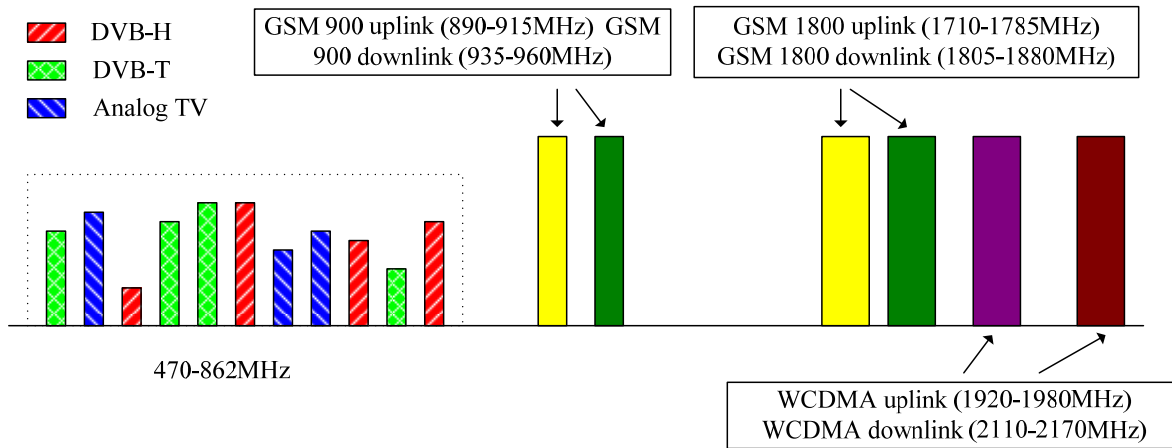


Fig. 3.4. Spectrum of the DVB-H receiver input

In both equations, the offset frequency will be $\pm n \times \frac{1}{6} \text{MHz}$ and $n = \{1, 2, \dots\}$. Therefore, the

DVB-H can use the frequency range from 470 to 862MHz. The DVB-H receiver input spectrum can be found in Fig. 3.4. Notice in the DVB-H frequency band, not only desired DVB-H channel is present but also undesired DVB-T channel and analog TV channel co-

exist, which has to be considered during the receiver design. In addition to these in-band interferences, due to the mobile service used in the same terminal, the uplink and downlink signal in the GSM or WCDMA will become strong out-band interferences.

3.2.3. Desired signal power range and tuner noise figure

In Fig. 3.3, the receiver is modeled as a demodulator. In fact, there should be a RF receiver before the demodulator, which is the DTV tuner. Regardless the implementation of the tuner, it always can be modeled as the simple block diagram shown in Fig. 3.5. The incoming data is amplified (or attenuated) by the RF variable gain amplifier first and then down-converted to baseband. The baseband variable gain amplifier adjusts the gain based on the input power level so that the power at the demodulator input is constant. The noise contributed from the tuner can be modeled as the noise factor F and the noise contribution after the ideal AGC (including phase noise and quantization noise) can be equivalently modeled as the excess backstop noise P_x . Based on the demodulator's output performance such as bit error rate (2×10^{-4} here), the threshold signal to noise ratio (also called C/N ratio) for the demodulator input can be derived for the specific constellation scheme. For example, the C/N ratios for Gaussian channel for different modulation scheme are listed in Table 3.1 [18].

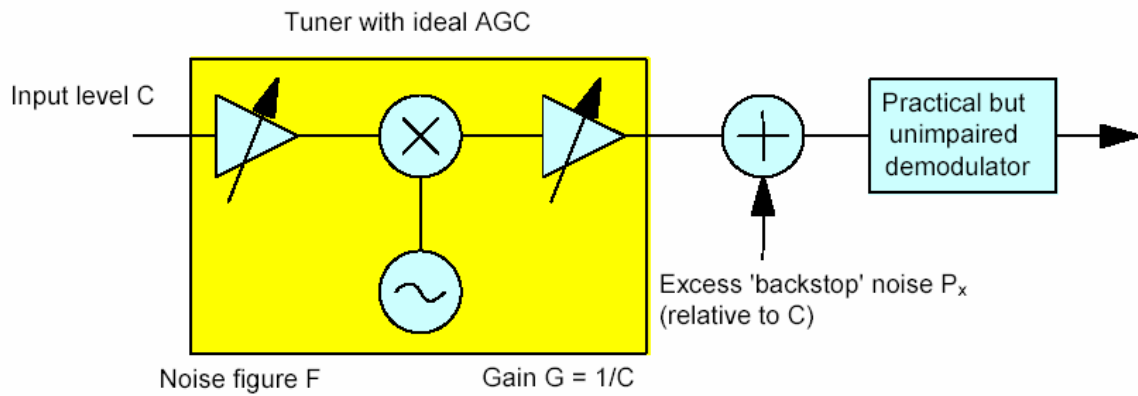


Fig. 3.5. Simplified model of DTV receiver

Table 3.1. Threshold C/N performance

Modulation	Gaussian Channel C/N (dB)	Portable Channel C/N (dB)
QPSK (1/2 code rate)	5.6	5.6
16QAM (3/4 code rate)	15.1	19.4
64QAM (3/4 code rate)	20.8	24.8

According to [18], the DVB-H tuner sensitivity for 8MHz channel is expressed below

$$P_{\min} = -100.2 + C / N \quad (11)$$

Therefore, the sensitivity for QPSK scheme is approximately -95dBm while for 64QAM is around -75dBm.

Based on the sensitivity and threshold C/N ratio, the tuner noise figure (NF) can be derived

$$NF = P_{\min} + 174 - 10 \log BW - C/N \quad (12)$$

which is 5dB for 8MHz bandwidth.

In the absence of any interference, the maximum wanted DVB-H signal for the tuner input is -28dBm. Therefore, the tuner has to provide at least 67dB gain range if considering -95dBm sensitivity for QPSK constellation. The absolute gain of the tuner depends on the output power level of tuner, which is -8dBm in this design. Thus, the maximum gain of the tuner will be around 87dB.

3.2.4. Tuner nonlinearity requirement

Like any electronic system, the nonlinear performance of the tuner will degrade the output signal quality in addition to the added noise. For the tuner, the desired signal band is from 470-862MHz and the transmitted and received cellular signals (GSM and WCDMA) act as out of band interferences. Those out of band interferences can be suppressed by the off-chip bandpass filter and then they can be neglected. However, those unwanted analog or digital TV channels from 470-862MHz are difficult to be pre-filtered. In the worst case, the interference channels can be very close to the desired channel with over 45dB higher power level than the desired channel. The tuner system has to be linear enough to receive the small signal in the presence of large interferences.

In order to calculate the tuner linearity requirement, it is necessary to know the linearity pattern first, which is provided in Table 3.2. The linearity pattern indicates that the tuner

has to process the desired channel (N) with the undesired adjacent channels (N+2 and N+4). And in the worst case, the undesired adjacent channel power can be 45dBc higher than desired signal. Notice the maximum interference channel power is -35dBm according to [18].

Table 3.2. Linearity pattern

Linearity Pattern	N+2	N+4
L1	Digital Channel (40dB)	Analog Channel (45dB)
L2	Analog Channel (45dB)	Digital Channel (45dB)
L3	Digital Channel (40dB)	Digital Channel (40dB)

Due to the third order non-linearity of the system, the undesired adjacent channels generate distortion components, which may fall within the desired channel, as shown in Fig. 3.6. If the undesired interference channel input power is P_u in dBm and desired channel input power is P_s in dBm, the desired channel output power is $G + P_s$ and the undesired interference power in the desired channel is $G + P_u - 2(IIP3 - P_u)$, where G is the power gain of the tuner. The system IIP3 needs to be large enough so that output can achieve enough SNR. Therefore the minimum IIP3 can be derived as below

$$IIP3 = P_u + \frac{P_u - P_s + SNR + 3}{2} \quad (13)$$

Notice that in the expression 3dB is added to provide a safety design margin.

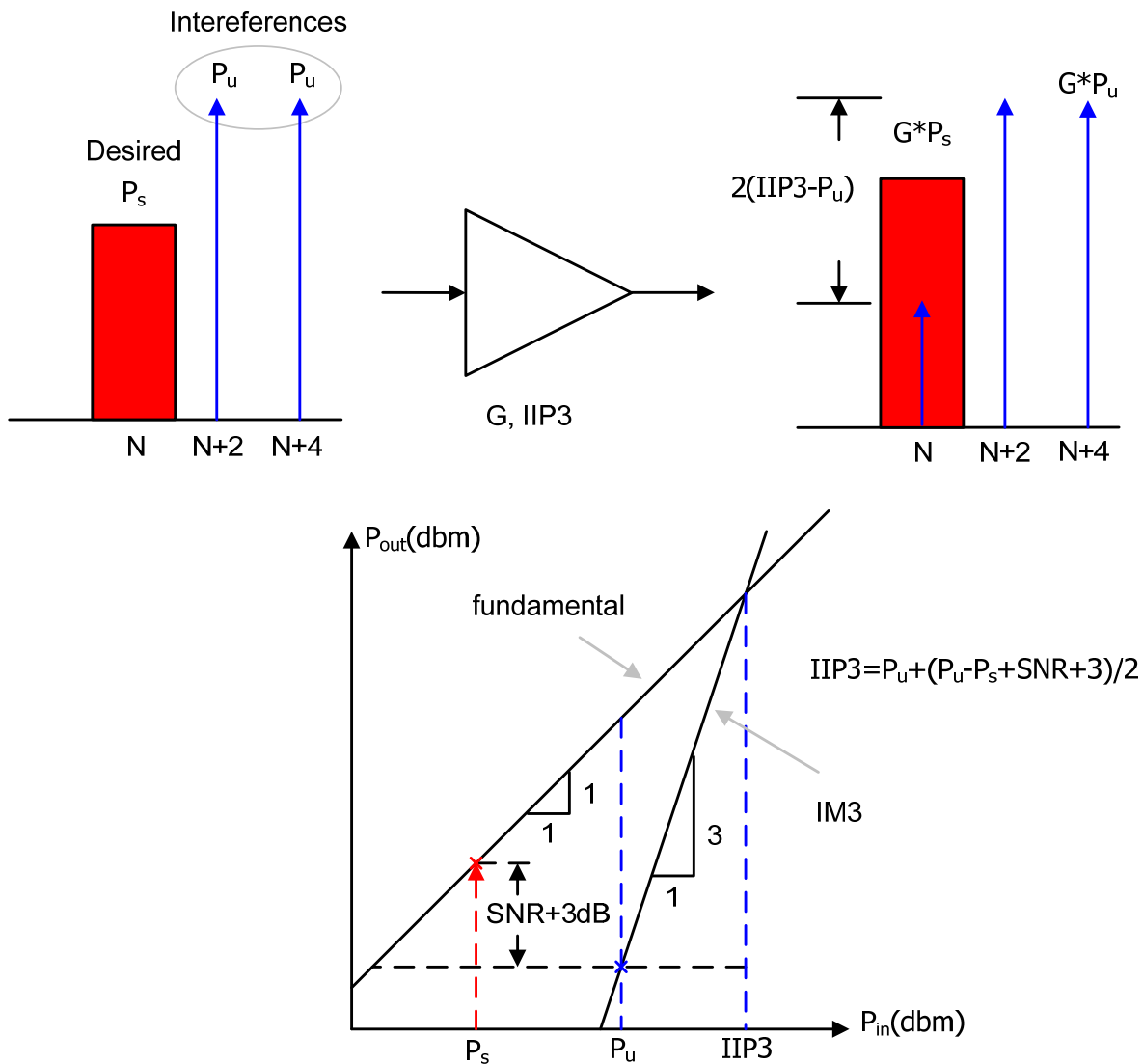


Fig. 3.6. IIP3 calculation illustration

Based on the linearity pattern, the worst scenario is happened when the desired signal power is minimum (-75dBm for 64QAM case) and undesired interference power is maximum (-35dBm). It can be calculated that the IIP3 is -1dBm.

3.2.5. Tuner selectivity requirement

Another important specification for the tuner is the channel selectivity requirement. As listed in Table 3.3, the unwanted adjacent analog channel can be 38dBc higher than the desired DVB-H channel. In order not to saturate the analog to digital converter in the demodulator block (not included in the tuner), the tuner has to provide enough attenuation for those adjacent channels. Based on the selectivity pattern, the filter requirements can be derived. To minimize the passband ripple and also maximize the stopband attenuation, the filter is better synthesized with inverse-chebyshev approximation. The magnitude response of the required 8th order filter is shown in Fig. 3.7, where the channel bandwidth is 4MHz. The filter provides 30dB attenuation at 5.25MHz offset, 50dB attenuation at 5.75MHz offset; over 50dB attenuation is achieved for the higher frequencies.

Table 3.3. Selectivity patterns

Selectivity pattern	Undesired/desired
S1 (analog adjacent channel)	38dBc
S2 (digital adjacent channel)	29dBc

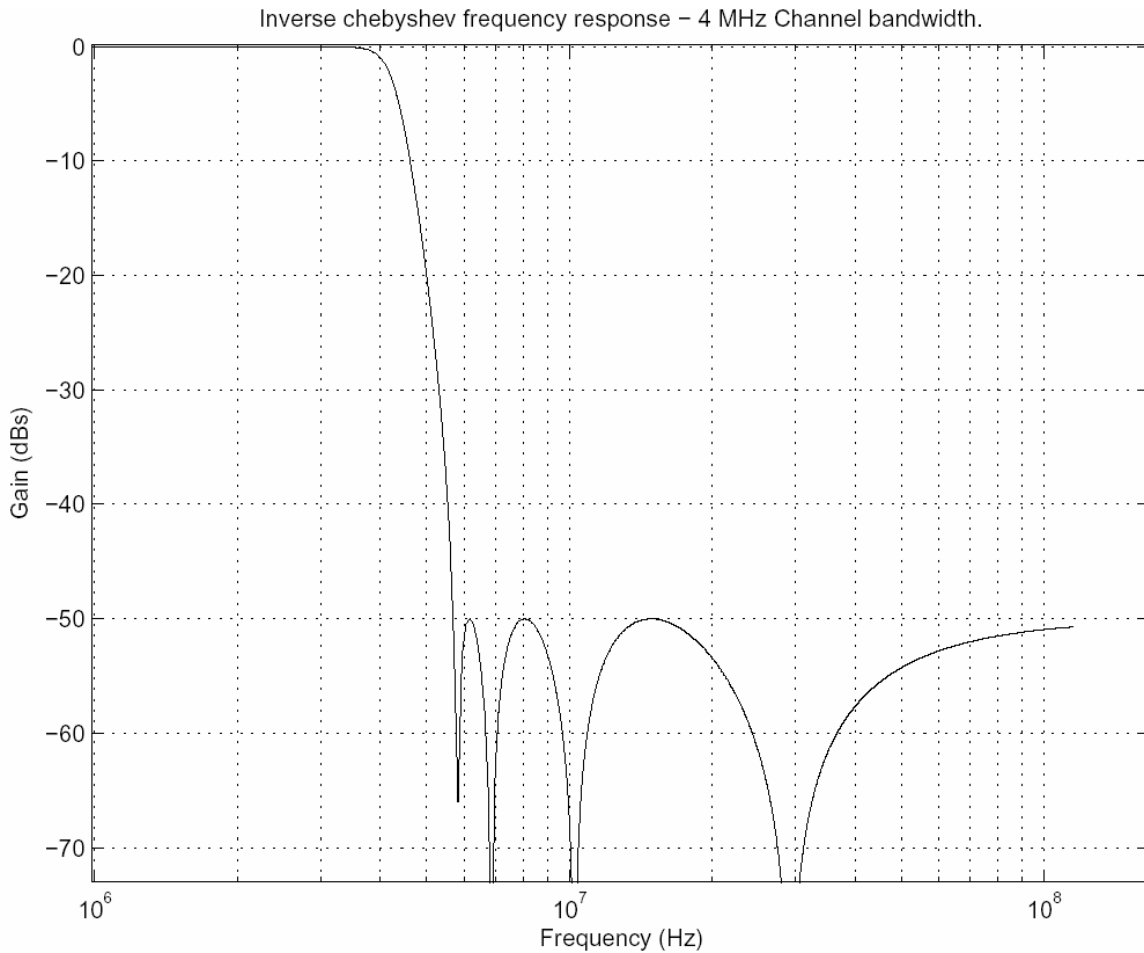


Fig. 3.7. Magnitude response plot of the baseband filter

3.2.6. Tuner phase noise requirement

Regardless of the tuner architecture, there is a local oscillator (LO) for the mixer to implement the down-conversion. The non-ideality of the LO is usually specified with phase noise [19], which is a critical parameter for the system design. The spectral noise sidebands usually appear at both sides of the carrier (desired LO) and it is typically specified with the term dBc/Hz (power reference to 1Hz bandwidth relative to the carrier). At different offset

frequency, the phase noise requirement can be different. The derivation of the phase noise requirement is discussed below.

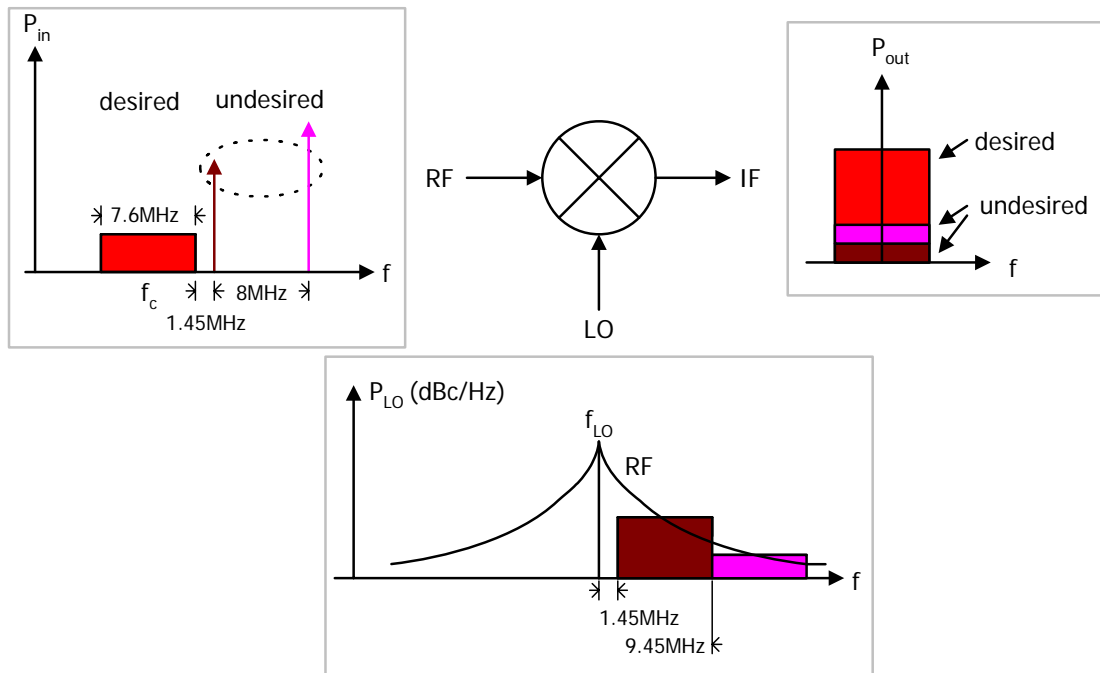


Fig. 3.8. Phase noise calculation illustration

When the input RF signal (including desired channel and undesired interferences) is mixed with the LO signal, the desired RF channel will be translated to baseband (or intermediate frequency), as shown in Fig. 3.8. In reality, due to the phase noise, the undesired signal will also be down-converted to baseband, which is called “reciprocal mixing”. The degradation due to reciprocal mixing depends on the phase noise and interference power level. In DVB-H system, the worst case happens when the interference channel is analog TV channel, which is 1.45MHz away from the desired DVB-H channel edge. Notice that the desired DVB-H channel bandwidth (effective bandwidth) is 7.61MHz. Therefore, the phase noise at 1.45MHz offset can be calculated according to equation below

$$PN(dBc) = -(P_u - P_s + SNR + 10 \log(BW) + 3) \quad (14)$$

where P_u is the power of undesired interference channel and P_s is the power of desired signal [19]. In this system, the N+1 analog channel can be 38dBc higher than desired DVB-H channel; the SNR is around 25dB for 64QAM; bandwidth is 7.6MHz. Therefore, the phase noise at 1.45MHz offset is around -133dBc/Hz.

Similarly, considering the N+2 analog interference channel, the phase noise at 9.45MHz offset is around -142dBc/Hz because $P_u - P_s = 48dBc$.

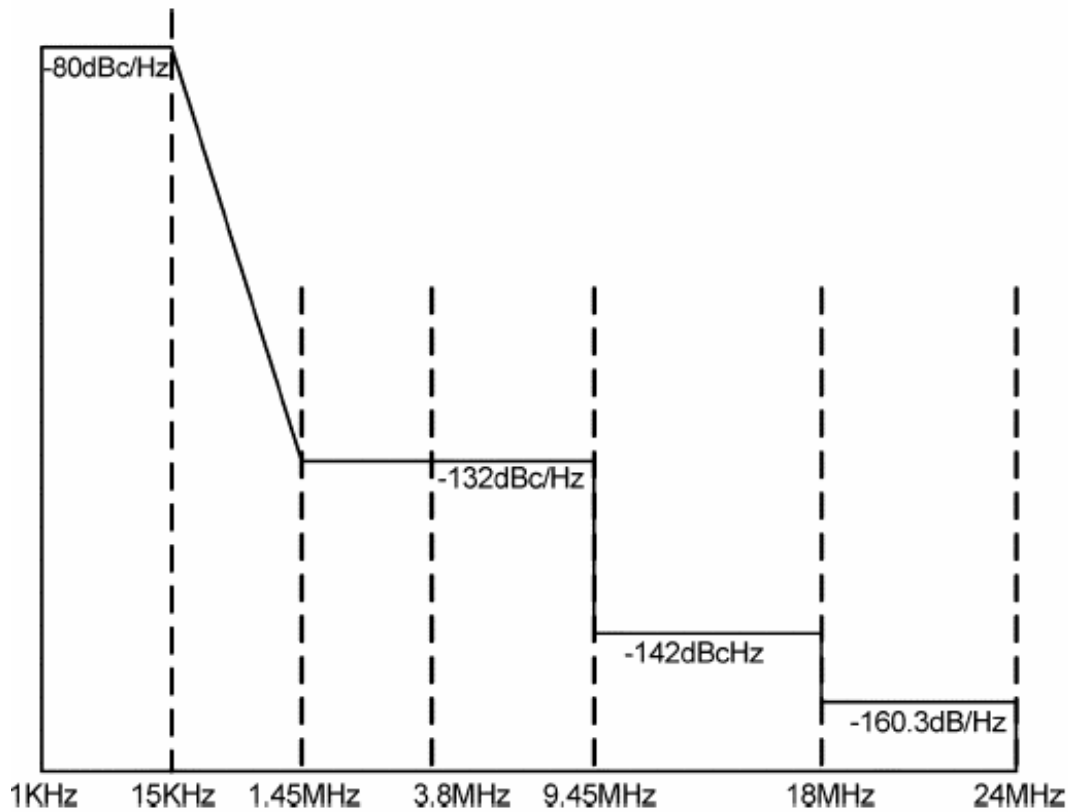


Fig. 3.9. PLL phase noise mask

Except for the reciprocal mixing introduced by the interference channel, the phase noise will degrade the output quality even without any interference channel. This is because for quadrature modulation scheme, the signal phase conveys information and it can be distorted by the LO phase noise. According to MBRAI specification, the integrated phase noise from 1k Hz up to 3.8M Hz needs to be less than -33dBc.

Based on these calculations, the phase noise mask can be plotted, as shown in Fig. 3.9.

3.3. Tuner Architecture

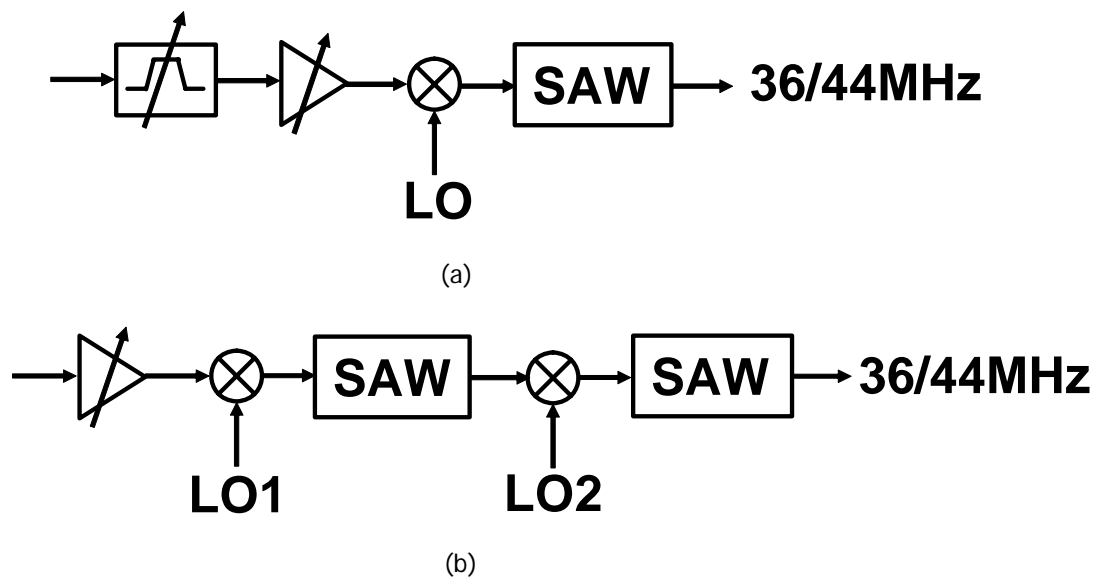


Fig. 3.10. Conventional TV tuner architectures: (a) single-conversion with RF tracking filter; (b) dual-conversion

There are several possible architectures available for the tuner design. The most conventional architecture is the single step low-IF architecture with tracking filter, as

shown in Fig. 3.10 (a). The incoming channel is pre-selected by the RF filter, which is usually implemented off-chip. The image channel and most of interference channels can be rejected by this filter and the input for the following stages become narrowband, and a simple low-IF architecture is suitable. After the down-conversion, due to high selectivity requirement in the 36/44 MHz, an off-chip SAW filter is required to attenuate the undesired adjacent channels.

This architecture proved to be successful in the past because the board level design was more convenient than chip design. However, with the increasing demand of fully integration to reduce the cost, this approach is not suitable any more because it is very difficult to design the on chip RF programmable tracking filter.

The dual-conversion architecture is widely used for integrated tuner, as shown in Fig. 3.10 (b). The incoming TV signal is first up-converted to very high intermediate frequencies such as 1.1GHz, and then the desired channel is roughly selected by the fixed frequency SAW filter. With the second down-conversion, the desired channel is down-converted to 36/44MHz while the undesired adjacent channels are filtered by the second SAW filter. In the first up-conversion, because of high intermediate frequency (over 1GHz), the image channel and harmonic channels are set out of band automatically, which further relax the image rejection and harmonic suppression problems. Also, the first SAW filter rejects most of the image and harmonic channels for the second down-conversion. Apparently, this architecture minimizes the off-chip components to two SAW filters and greatly improves

the integration level. Currently, this architecture is popular in both cable and terrestrial TV tuner industries.

Because of the dual-conversion, the power consumption of the tuner is usually over 1w, which makes itself not suitable for the mobile devices. Also, in order to fit in the tiny mobile device, it is critical to remove the bulky SAW filters. Therefore, the zero-IF architecture is believed to be the best solution and it is adopted in this design. The simplified system block-diagram is shown in Fig. 3.11.

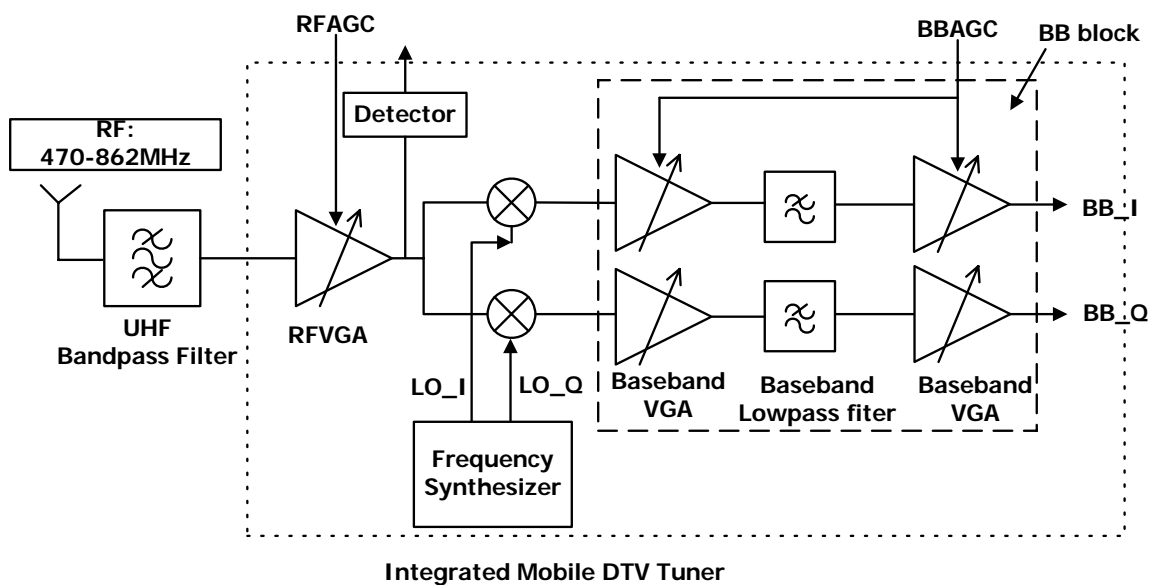


Fig. 3.11. Block diagram of direct conversion (zero-IF) DVB-H tuner

As shown in Fig. 3.11, an external UHF bandpass filter eliminates the out of band interferences. Depending on the location of out-of band interferences, that filter requirement can be slightly different. For the CDMA or WCDMA transmitted signal, the attenuation requirement of the filter can be relaxed compared to the GSM case. In the

extreme case like GSM, because it is difficult to reject the GSM signals due to small frequency offset, the channels above 700MHz will not be used [18]. In summary, with selection of the proper filter, the out of band interferences are attenuated enough and only the TV channels are considered in the tuner input.

The main difference between this architecture and those conventional ones is the final down-converted frequency. Here the center frequency of the desired channel is DC after the down-conversion while the others are 36/44MHz. Therefore, there is no need for the image rejection. Also, because the frequency band is from 470MHz to 890MHz instead of 50MHz to 890MHz (terrestrial and cable TV), the harmonic frequencies of the LO are out of band. Furthermore, the channel selection filter can be designed on-chip because it will be a low pass filter instead of the band pass filter required in conventional architectures.

The main design challenge for this mobile tuner is the low power consumption. However, the required high dynamic range in this system requires huge power consumption. To alleviate this tradeoff the system uses multiple AGC loops. The gain of the RFVGA is adjusted based on the broadband power at the mixer input; this ensures that the mixer and the baseband stages are not saturated by potential large input signals. Also this RFVGA gain can be adjusted based on the final baseband output to maximize the output SNR. For the baseband VGAs, they mainly serve for two purposes. One is adjusting the signal level for the filter to relax the filter design challenge. The other is amplifying the signal to provide constant signal level for the next stage such as ADC.

The other design challenges for this tuner are DC offset, even-order distortion, IQ mismatch, and flicker noise (if CMOS implementation), which are discussed in the following sections.

3.3.1. DC offset

In the RF front-end (RFVGA and mixer), because the zero frequency (DC) is part of the down-converted channel, offset voltages corrupt the signal. More importantly, the baseband VGA and filter section may be saturated. In general, there are two sources for the DC offset generation. The first one is due to the limited isolation between mixer's LO and RF port. LO signal from PLL can leak to RFVGA input or the mixer input and then mix with LO signal to create the DC offset, which is called "self-mixing"; this effect is shown in Fig. 3.12. In addition, the strong interference signal from the input may also leak to the LO port. The DC offset introduced by self-mixing strongly depends on the isolation performance. For example, the coupling from LO port to RFVGA input (usually bondwire coupling or substrate coupling) is around -40dBc. If the LO power is 0dBm, a -40dBm LO signal will leak to the RF input. If the gain from RF to baseband is 87dB (the maximum value), the output DC offset could be as large as 47dBm, which means that the baseband circuitry will be saturated and will not function properly. In order to minimize the self-mixing issue, we have to improve the port isolation and minimize the undesired coupling. For example, multiple guard rings can be used to isolate the PLL circuitry from other RF blocks.

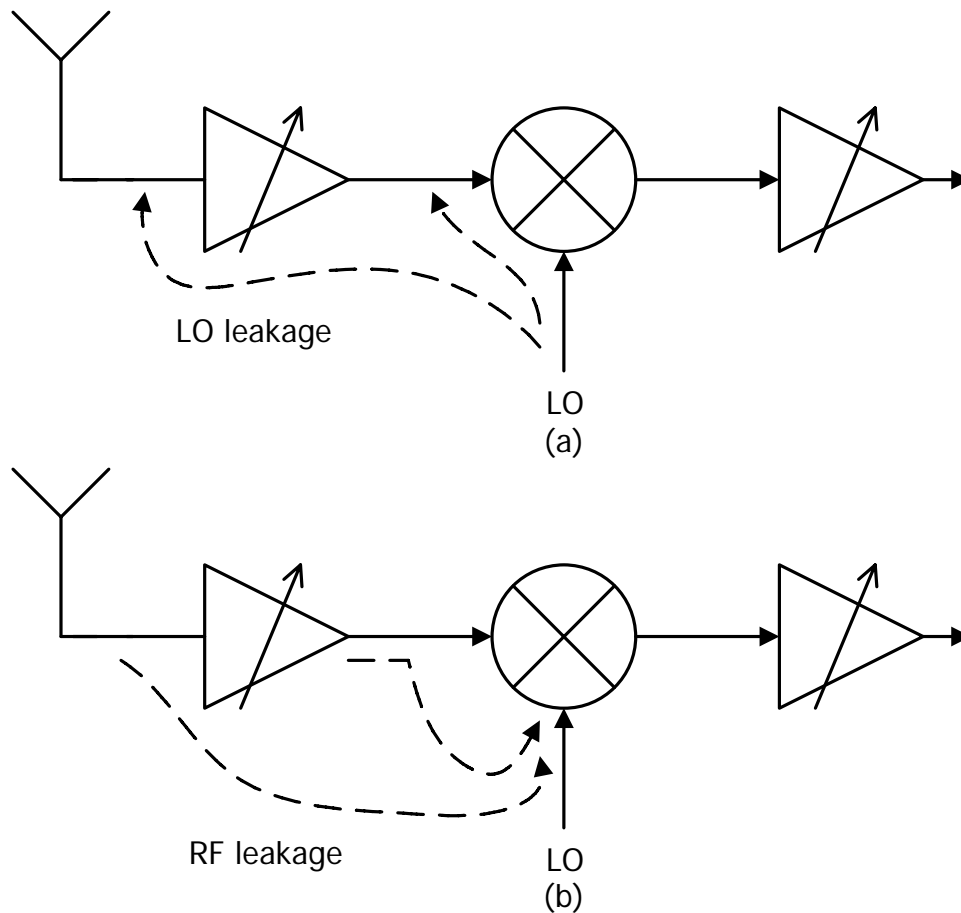


Fig. 3.12. DC offset introduced due to self mixing

The second DC offset source is the finite on-chip matching performance. The mismatch of transistors or passive components will generate DC offset. This DC offset becomes troublesome especially for the building block after the mixer. Due to the large gain in the baseband, the DC offset in the baseband amplifier will saturate the receiver. Increasing the matching performance can help to minimize the DC offset.

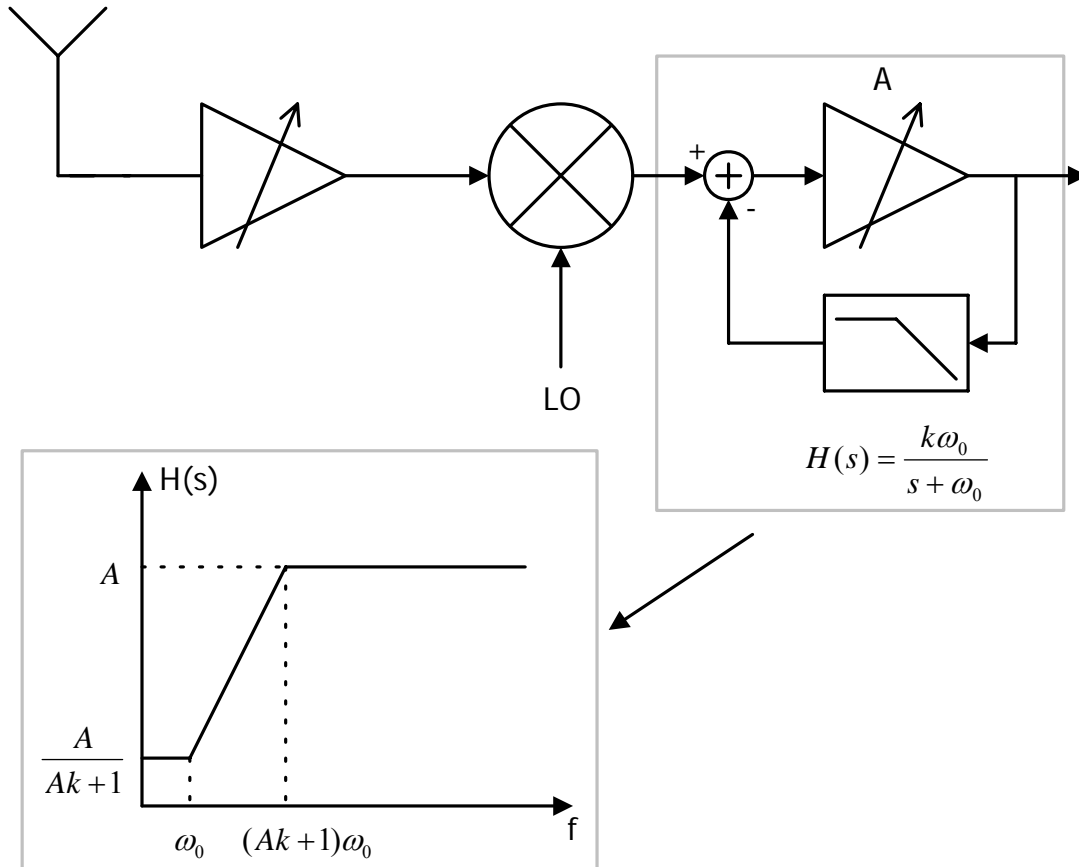


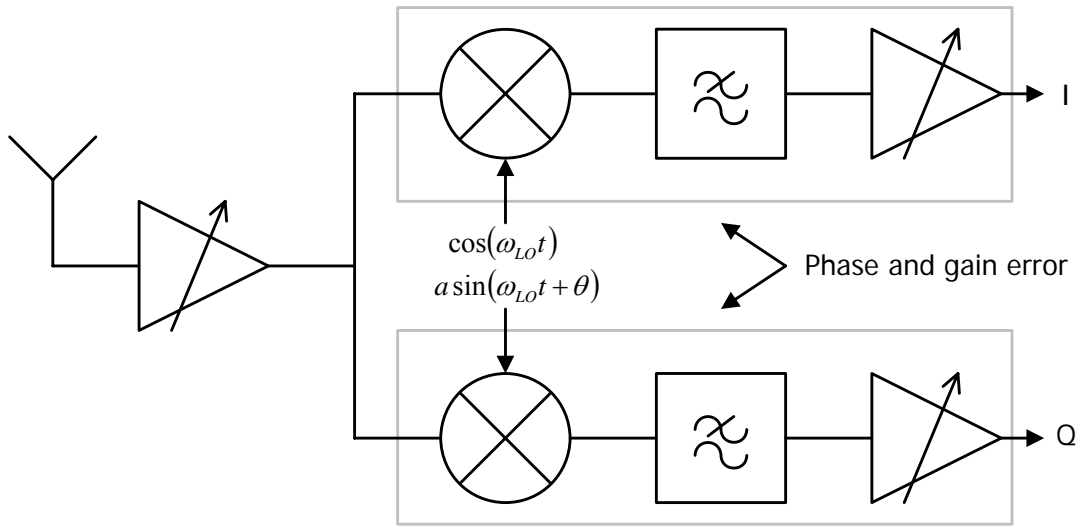
Fig. 3.13. DC offset suppression loop

Considering the DC offsets discussed above, an offset-cancellation technique is required for the tuner to deal with this issue. Due to the lackness of large on-chip blocking capacitor, one basic approach, which implements a high pass transfer function for the desired signal, is shown in Fig. 3.13. The output information of the baseband variable gain amplifier is feedback with a lowpass filter and the DC information is grabbed after the filter. Then the baseband input DC information is subtracted, which is equivalent as a high pass filtering for the baseband input. For the system like DVB-H, desired signal bandwidth is from DC to 3.8MHz. Therefore, it is necessary to minimize the high pass corner frequency. However, in order to minimize the corner frequency, large capacitor has to be used, which means a lot

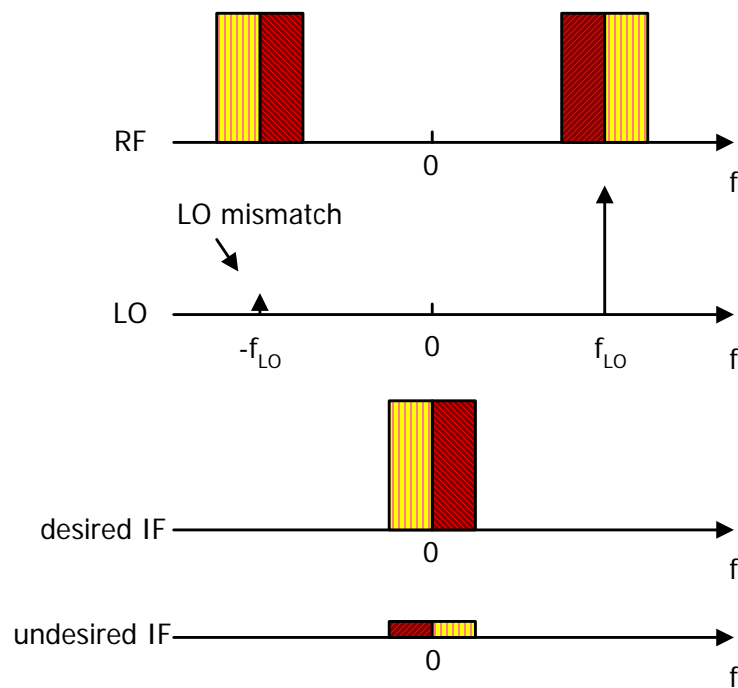
of area or extra external component. In this design, 1 kHz corner frequency is selected, which impacts only couple of carriers with negligible degradation and allows practical on-chip implementation.

3.3.2. I/Q mismatch

Because the data constellation of the DVB-H system is either QPSK or QAM and the spectrum is not symmetrical, the quadrature down-conversion is utilized to avoid loss of information. In the practical implementation, the phase difference of the quadrature LO is not exactly 90 degree (phase imbalance) and the gains of the two quadrature path (from mixer input to baseband out) might be different (gain mismatch), as depicted in Fig. 3.14 (a). As a result, the signal constellation is corrupted and the bit error rate increases. A simple view of the degradation is given in Fig. 3.14 (b). The overall I/Q mismatch at the output can be modeled as the LO I/Q mismatch and this causes a leakage component in the negative LO frequency. This undesired $-f_{LO}$ mixes with the positive RF input and generates undesired baseband component. This is similar as the image rejection issue for the low-IF architecture but the image channel is the desired channel itself in this case. The I/Q mismatch requirement depends on the specific data constellation scheme. Based on system simulations, it can be found that the most stringent I/Q matching requirement is -35dB, which is for 64QAM constellation scheme.



(a)



(b)

Fig. 3.14. I/Q mismatch illustration

The most critical blocks for the I/Q matching performance are the mixer and frequency synthesizer because the baseband operating frequency is less than 5MHz and large area can

be used to improve the baseband matching. Therefore, when designing the mixer and PLL, special attention about I/Q mismatch is required.

3.3.3. Even-order distortion and flicker noise

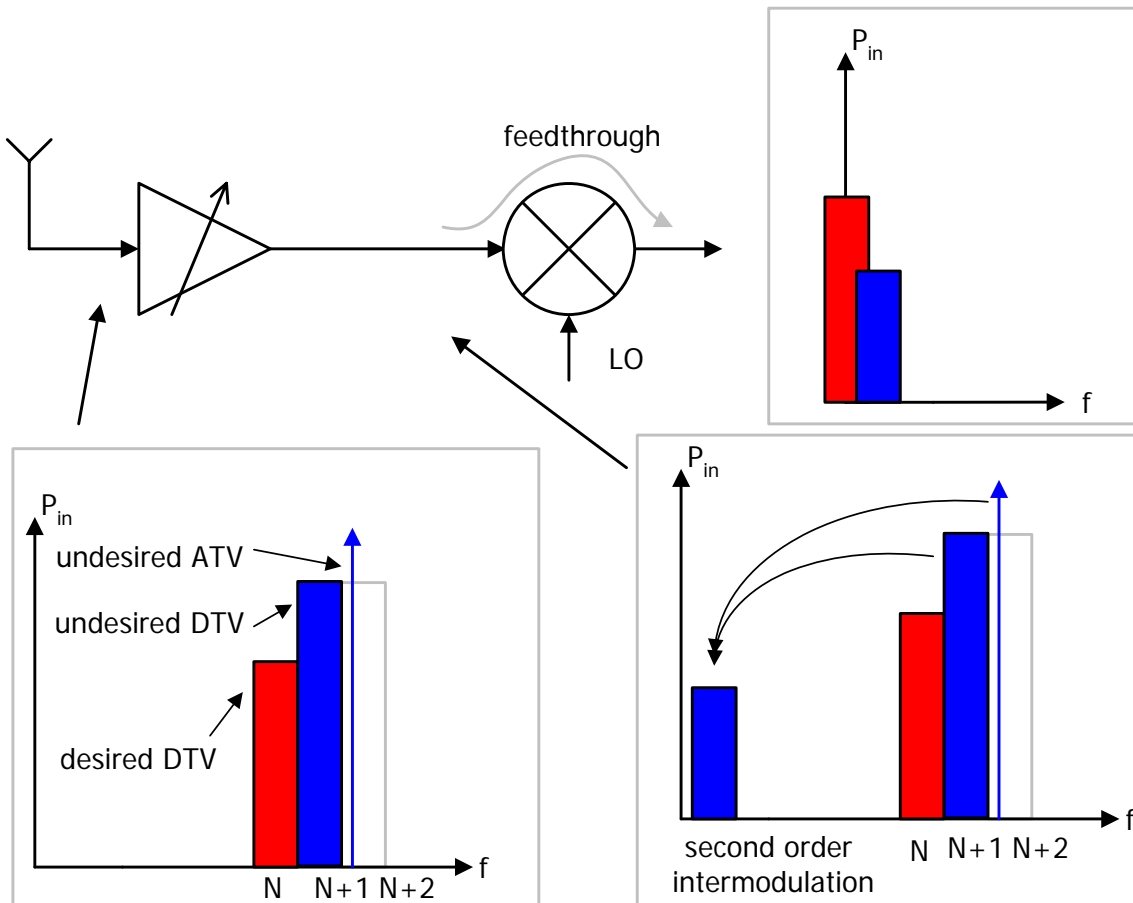


Fig. 3.15. Even order distortion due to feedthrough

In the aforementioned non-linearity issue, only third order distortion was considered. However, in the direct conversion receiver, the second order distortion is also an important issue, especially second order intermodulation distortion.

The first kind of even order distortion is related to the non-linearity of the RFVGA and the feedthrough, as shown in Fig. 3.15. In this system, the RFVGA is implemented with single-ended configuration to save power and prevent the usage of broadband off-chip single-differential balun. Unfortunately this RFVGA has second order distortions. Assuming that two very close interferences (N+1 DTV channel and N+2 analog channel) and desired weak signal (N DTV channel) are received at the tuner input in the same time; because the analog TV video carrier is very close to the edge of the N+1 DTV channel (1.25MHz), the undesired low frequency band generated after the RFVGA will be from 1.25MHz to 9.25MHz. In real implementation of the mixer, there is always a finite feedthrough from RF input to baseband output. Therefore, this low frequency interference band will corrupt the desired baseband (DC to 4MHz) and this degradation cannot be suppressed with the baseband filtering.

In order to overcome this kind of even order distortion, we may use differential RFVGA or suppress the feedthrough of the mixer. However, implementing a fully differential RFVGA does not only add extra power and noise, but also require expensive off-chip balun, which are not acceptable for the low cost target. Therefore, suppressing the RF to baseband feedthrough is preferred. In a practical implementation, we can use double balanced mixer configuration and utilize capacitive coupling between RFVGA and mixer for better even order distortion performance.

The second kind of even order distortion is mainly associated with the “self-mixing” issue, as depicted in Fig. 3.16. There is always the leakage between tuner RF input (or mixer

input) and the LO port, which can be due to substrate coupling, bondwire coupling and circuit parasitic coupling. If two undesired strong interferences ($N+1$ DTV and $N+2$ analog TV) are coupled to the mixer LO port, they will mix with themselves. The desired down-converted baseband will be distorted by the spurs generated due to self-mixing. It is important to notice, this sort of even-order distortion cannot be suppressed even if a fully differential implementation; the only effective solution is to suppress the leakage as much as possible. In order to do that, proper isolation between LO and the RF part is necessary.

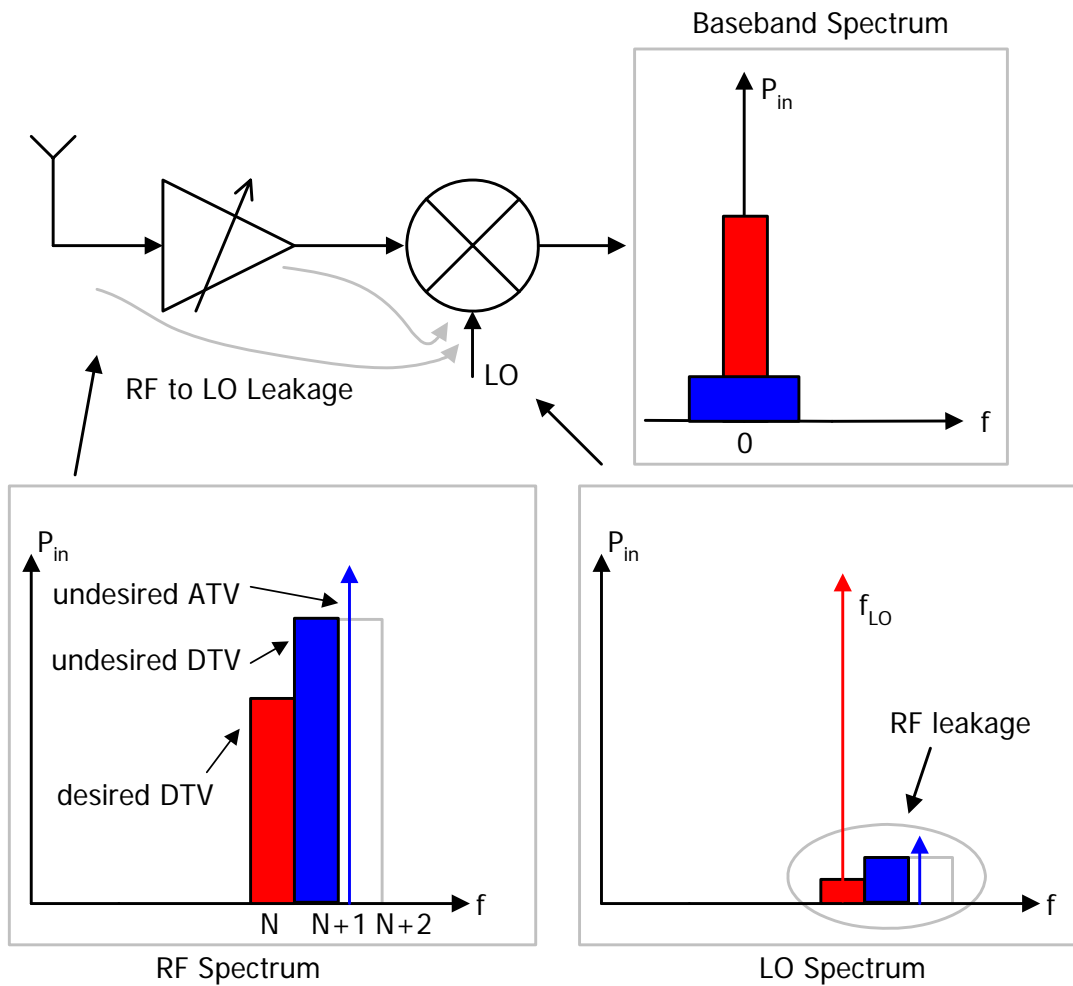


Fig. 3.16. Even-order distortion due to RF leakage

Regardless of the origin of the even-order distortion, it can always be characterized with the specification IIP2, which is the input referred extrapolation point for second order inter-modulation distortion figure. Following similar approach as the derivation of IIP3, the overall IIP2 can be derived as shown in Fig. 3.17. Any undesired interference P_u generates an output inter-modulation product IP2. The desired signal P_s generates the desired output signal and this signal must be large enough to ensure sufficient output signal to noise ratio.

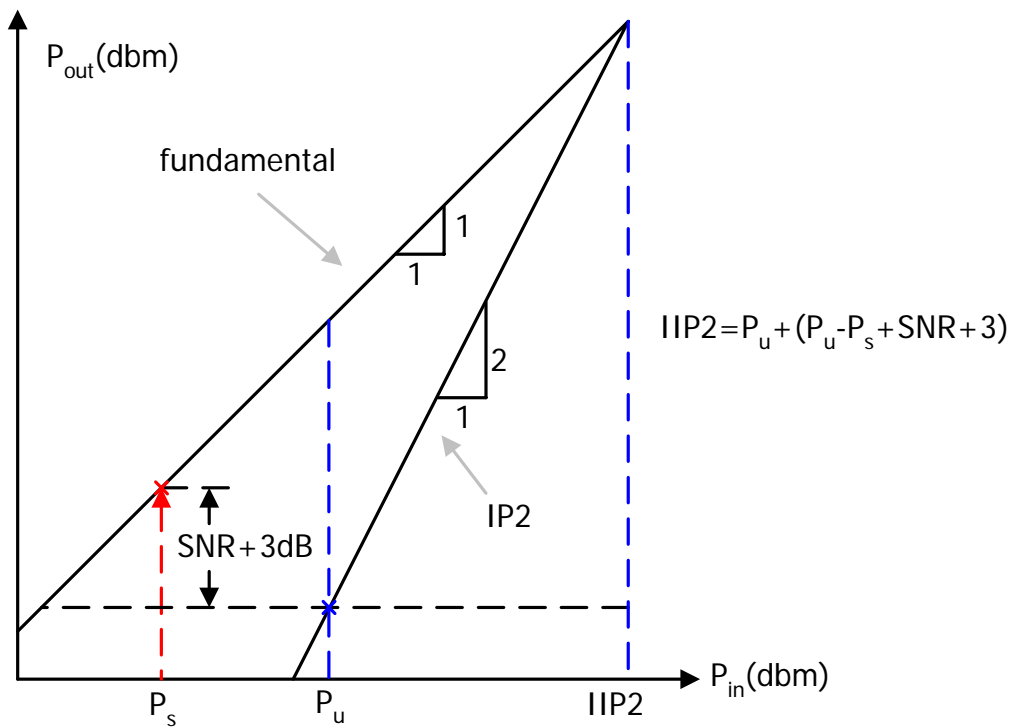


Fig. 3.17. IIP2 derivation plot

Therefore the IIP2 can be expressed as

$$IIP2 = P_u + (P_u - P_s + SNR + 3) \quad (15)$$

When the desired signal power is -75dBm and undesired interference power is -35dBm, the overall system IIP2 specification is 33dBm.

The flicker noise needs to be specially considered for CMOS implementations. When the tuner is designed in CMOS technology, the flicker noise of the CMOS transistors will degrade the output SNR. In this tuner system, the most critical block for the flicker noise is the mixer. The flicker noise of the baseband circuits can be minimized with large transistor area and high front end gain. Proper mixer topology like passive mixer will help to reduce the flicker noise. In addition, the DC offset cancellation loop helps to remove the flicker noise below 1 kHz.

3.4. Block Level Specifications

In order to achieve the overall dynamic range specifications, the gain/noise/linearity specifications for the main building blocks are carefully derived and listed in Table 3.4.

Table 3.4. Block design specifications

Parameter	RFVGA	MIXER	BASEBAND (VGA and filter)
Gain	From 16dB to -14dB	12dB	From 59dB to 22dB
Noise Figure	3dB @16dB gain 30dB @-14dB gain	12dB	25dB @ 59dBgain
IIP3	0dBm @16dB gain 20dBm @ -14dB gain	15dBm	30dBm @ 59dBgain

For the RFVGA, 30dB gain range is required to ensure the mixer and baseband stages are not saturated. In this design, the takeover point for the RFVGA is set as -20dBm, which means that the RFVGA's gain starts to decrease when the input power of mixer exceeds -20dBm. Higher noise figure for low gain settings can be tolerated because the input signal power is larger. At the same time, the better linearity is expected. For the baseband part, over 27dB variable gain range has to be distributed properly between baseband VGA and filter to ensure enough output SNR. For both RFVGA and BBVGA, it is better to adjust the gain smoothly and finely because the DVB-H application is sensitive to abrupt signal variation. Therefore, it is advisable to have gain step smaller than 1dB and analog smooth gain control.

3.5. Conclusion

In this chapter, a mobile DTV tuner system is discussed to target for DVB-H standard. To implement a low cost low power mobile DTV tuner, the direct conversion architecture was proposed, which increases the integration level and reduces the power consumption compared with the conventional cable or terrestrial tuner. The specifications for the system and building block have been derived. In addition, the main design challenges like DC offset, even-order distortion, I/Q mismatch and flicker noise have been addressed.

CHAPTER IV

DESIGN OF RF VARIABLE GAIN AMPLIFIER (RFVGA)

4.1. Introduction

With the increasing demand for personal multimedia services, mobile DTV is becoming a popular application. As discussed in previous chapter, there are several standards available worldwide for this application including DVB-H and ISDB-T one segment reception. Different frequency plans are utilized for these standards like the UHF band IV-V (470MHz-890MHz) with variable channel bandwidth 5MHz-8MHz for DVB-H, and the UHF band (470MHz-770MHz) with 6MHz channel bandwidth and 430kHz per segment for ISDB-T one segment reception.

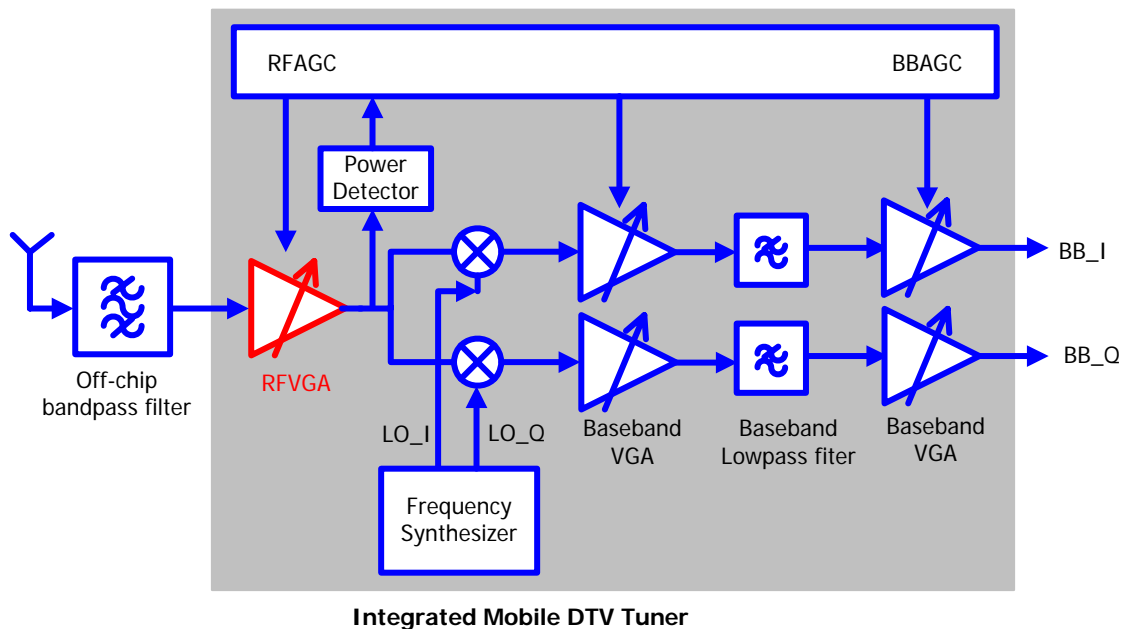


Fig. 4.1. Mobile DTV tuner architecture

During the reception, the desired channel is usually presented with multiple in-band interferers (like analog TV and DTV terrestrial channels), while the power of these interferers could be 40dBc higher. One solution is to filter these interferers before being received by the front-end of the tuner. However, this proves to be difficult without using tracking filters. Another option is to employ an RFVGA with high dynamic range as the first stage of the tuner [9], [16], [20]-[24]. For example, in our DVB-H mobile tuner design, the RFVGA is used for the first stage of the integrated tuner, as shown in Fig. 4.1.

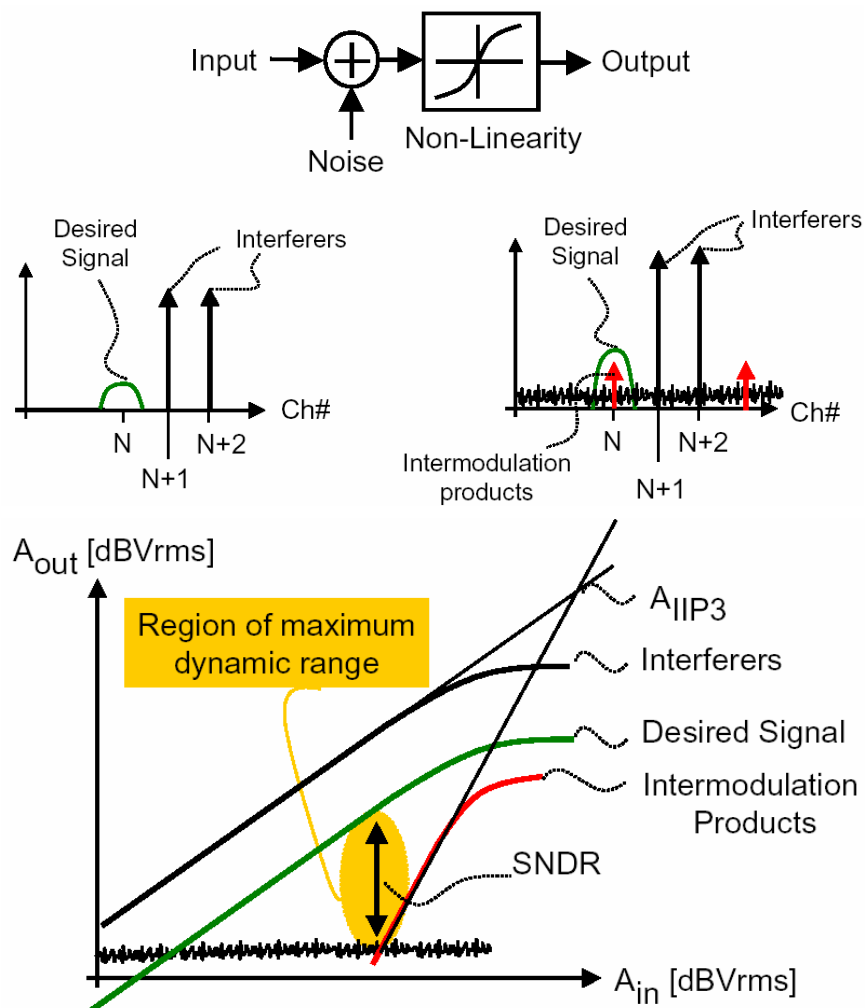


Fig. 4.2. Why the RFVGA is needed

The fundamental role of the RFVGA is to maximize the overall system dynamic range and also prevent the overloading of the following stages in the signal-chain, which is illustrated in Fig. 4.2. For a practical system, the quality of the output signal will be usually degraded by the added noise and distortion (especially due to third order intermodulation). The added noise is usually fixed and independent of the incoming signal and interference power level. However, the added distortion increases with the interference power level. For a given interference to signal ratio, there will be always an input power level which provides the maximum output signal to noise plus distortion ratio (SNDR). If the incoming signal and interference power are larger, the output SNDR will be limited by the non-linearity issue. In another way, the output SNDR will be limited by the noise. Therefore, adjusting the input level in that region will be helpful. The RF variable gain amplifier is the best candidate to achieve this target. Usually, a local RF automatic gain control loop (RFAGC) is required to set the RFVGA gain properly according to RFVGA output power level. It ensures the output power under the control and the following stages not being saturated.

In general, a low noise figure, high linearity, and sufficient gain range with fine gain steps are required for this RFVGA. As the front-end of the tuner, the RFVGA must also provide resistive input impedance match (75Ω) to ensure proper operation of an off-chip RF filter (like GSM rejection filter in [21]) and to reduce the power reflected to the antenna. In addition, the power consumption of the RFVGA has to be maintained small to enhance the mobile device battery life. All the above considerations need to be weighed against the overall tuner noise figure and linearity.

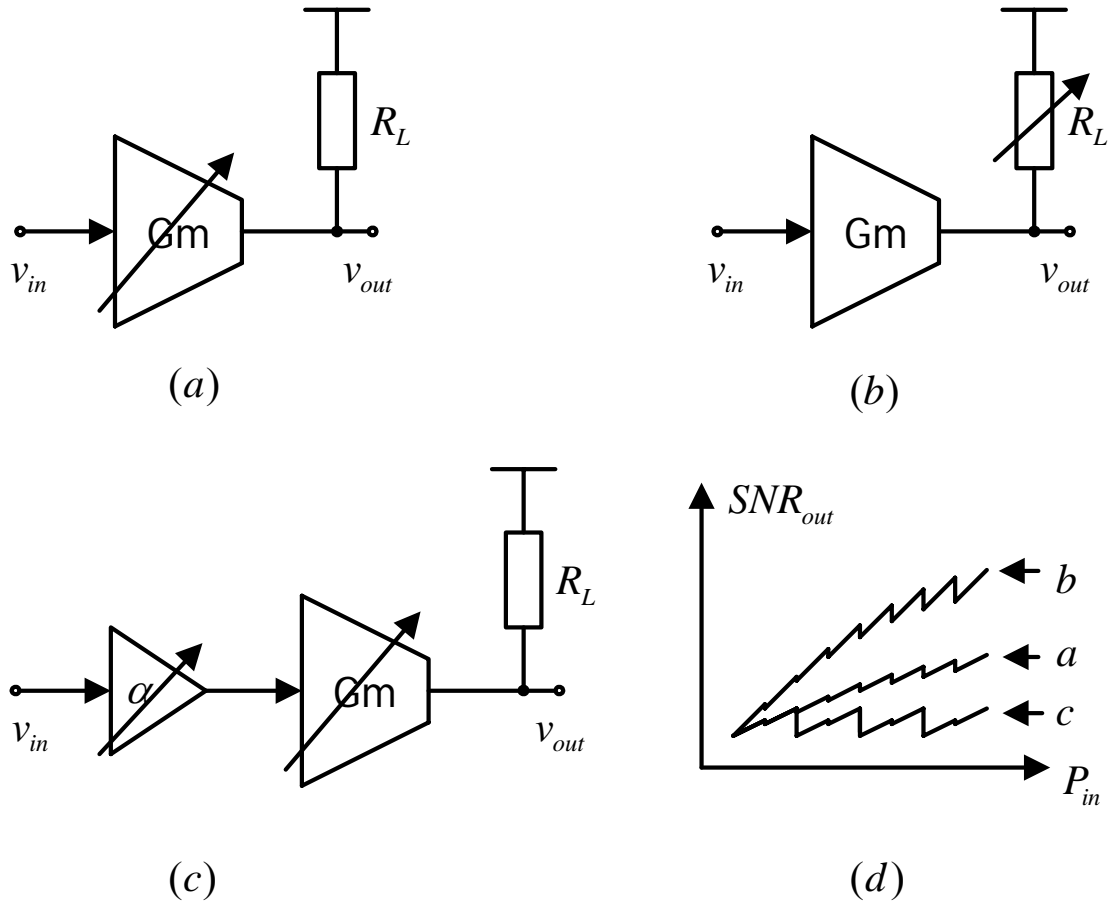


Fig. 4.3. (a) Variable G_m VGA; (b) Variable load VGA; (c) Pre-attenuation plus variable G_m VGA; (d) Different VGAs' output SNR plots

4.2. RFVGA Architecture Design

A variable gain amplifier can be designed by varying either the transconductance (G_m) or the load, as shown in Fig. 4.3 (a) and (b), respectively. For these configurations, to ensure constant peak output signal, G_m or R_L has to be reduced when input level increases. The signal to noise ratio for the CMOS implementations of (a) and (b) can be computed as

$$SNR = \frac{V_{in,RMS}^2 G_m}{4kT \left(\gamma + \frac{1}{G_m R_L} \right) f_{BW}} \quad (16)$$

where the Gm stage's output noise current spectral density is modeled as $4\gamma KTG_m$, γ is a noise fitting parameter; f_{BW} is the noise bandwidth and $V_{in,RMS}$ is the root-mean-square of the input voltage. According to equation (16), the SNR for both configurations increase with the input power, as shown in Fig. 4.3 (d); due to the finite resolution of the VGA in practical implementations, the SNR plots may not increase continuously. Usually active devices are used to implement the Gm stage; these topologies are non-linear and degrade the quality of the output signal. For high input levels, the VGA's output is limited by distortion instead of noise; attenuation at the output does not help in improving VGA's linearity. Thus it is beneficial to provide a variable pre-attenuation (α) prior to the active variable Gm stage as shown in Fig. 4.3 (c). When the input increases, α is correspondingly reduced to ensure that the input of the Gm stage is within its linear range; Gm is also adjusted to achieve constant output. In this case, the SNR becomes

$$SNR = \frac{(\alpha V_{in,RMS})^2 G_m}{4kT \left(\gamma + \frac{1}{G_m R_L} \right) f_{BW}} \quad (17)$$

Thus, for $\alpha = 1$ the output SNR will be same as the SNR of variable-Gm configuration and remains around the same value for smaller α (larger input signals), as shown in Fig. 4.3 (d).

Although the SNR does not keep increasing with input power, it is enough if its minimum meets the specifications.

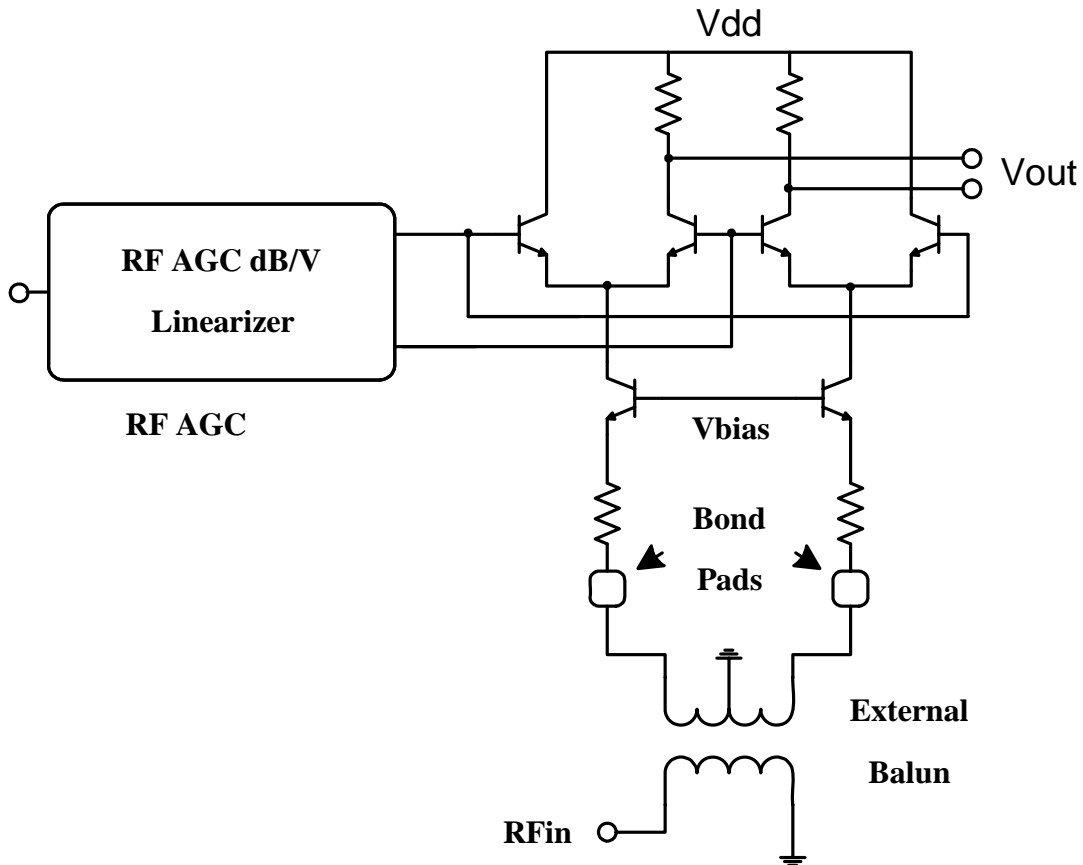


Fig. 4.4. Schematic of variable-Gm based RFVGA

RFVGAs based on the variable-Gm configuration have been reported in [9], [16] and [21]. A typical implementation is shown in Fig. 4.4, where the emitter-degenerated common-base stage provides broadband input impedance matching [21]. To achieve the high linearity required at low gain settings, a large degeneration factor has to be used, which results in huge power consumption and high noise figure. Thus, usually an external LNA is required to reduce system noise figure.

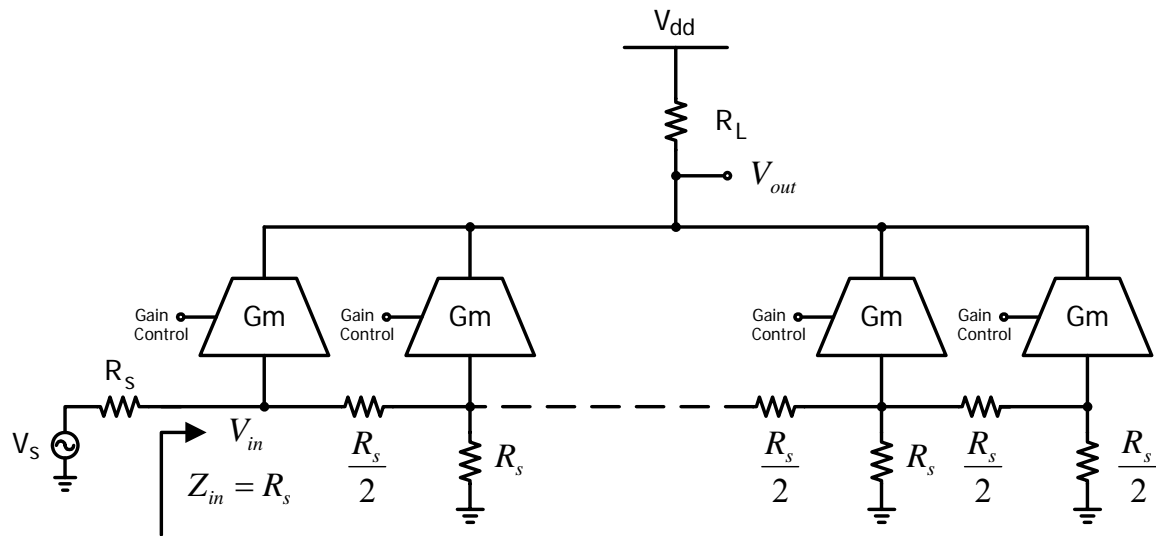


Fig. 4.5. Block diagram of pre-attenuation type RFVGA (single-ended)

The pre-attenuation based RFVGAs have also been implemented in [8], [20] and [22]. A typical implementation is shown in Fig. 4.5, where an R-2R based attenuator provides 6dB attenuation per stage along with good input impedance matching [8]. The main drawback of this architecture is the additional noise due the resistive attenuator that results in noise figures greater than 3dB. In [22], a capacitive attenuator and conventional shunt-feedback input matching are used to achieve low noise figure. In that topology, however, the input impedance strongly depends on the RFVGA gain; hence it is difficult to maintain the input matching performance during the gain adjustment. As a result, low noise figures can be achieved at the expense of poor input matching.

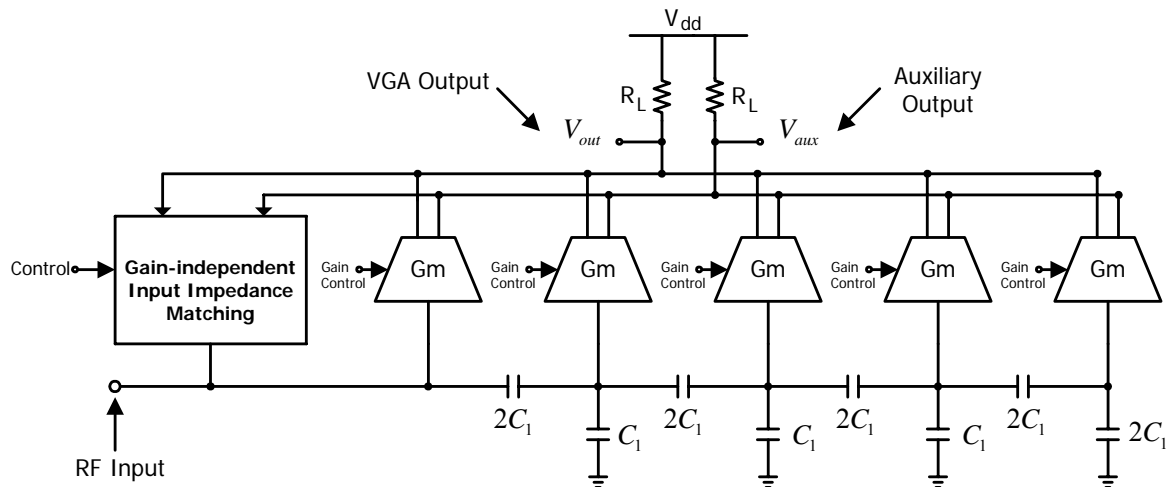


Fig. 4.6. Block diagram of the proposed RFVGA architecture

In this design, the pre-attenuation type RFVGA is modified to ensure both low noise and robust input matching performance; the block diagram of the proposed topology is shown in Fig. 4.6. A capacitive attenuator provides 6dB attenuation per stage; the total 30dB gain range is achieved with five identical G_m stages. Only one G_m stage is enabled at a time; however the small signal transconductance is adjusted to cover 6dB gain programmability range with 1dB resolution. Resistive loads R_L are used to provide flat frequency response from 470MHz to 890MHz (UHF band for mobile DTV standards). The RFVGA output (V_{out}) and the in-phase auxiliary output (V_{aux}) are fed back to the gain-independent input impedance matching block to generate the desired input impedance.

To reduce the power consumption and eliminate the need for the external single-ended to differential balun, the circuit is implemented in a single-ended configuration. Usually, single-ended circuits suffer from limited CMRR and PSRR and even-order distortions. Because of limited CMRR and PSRR, noise and interference from digital circuits and other

RF blocks can be coupled to the RFVGA and degrade tuner performance; using large on-chip decoupling capacitors and isolating the RFVGA from other critical blocks alleviate this issue. The even-order distortions will not be critical because the distortion tone will be out of band.

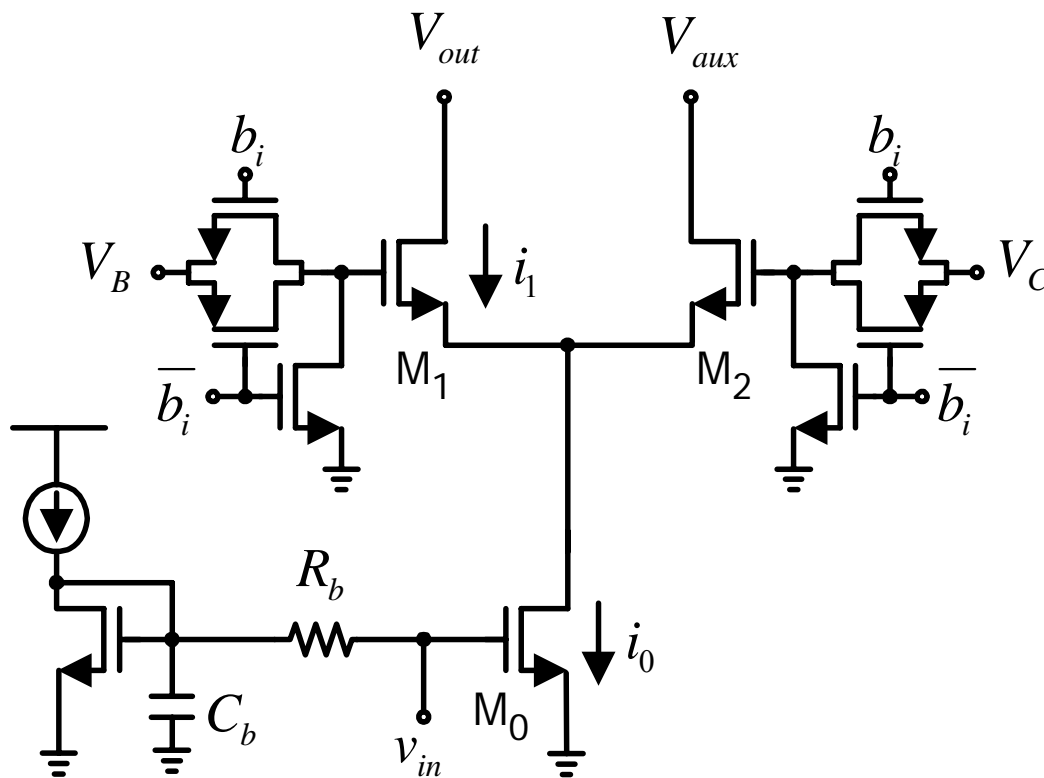


Fig. 4.7. Simplified schematic of the current-steering Gm stage

4.3. Design of Current-steering Transconductance (Gm) Stage

Because DTV reception is sensitive to abrupt or sudden gain changes, fine gain steps with smooth gain adjustment is required. To satisfy this requirement, the variable Gm stage is implemented based on the current-steering configuration shown in Fig. 4.7. Transistor M0

converts the input voltage into a current, which is steered between transistors M1 and M2 (identical dimensions) according to V_B and V_C . V_B is a fixed DC voltage while V_C is the DC control voltage generated by the gain control block. Digital controls b_i and $\overline{b_i}$ enable (disable) the Gm stage. The bias circuitry for M0 is also shown in Fig. 4.7; large values for C_b (4pF) and R_b (20k) ensure negligible noise contribution from the bias circuitry.

When the Gm stage is enabled (b_i is high) the small signal current (i_1) flowing through transistor M1 can be expressed as

$$i_1 \approx \left(\frac{1}{2} + \frac{\sqrt{\beta_1} V_D}{4 \sqrt{I_0 - \frac{1}{4} \beta_1 V_D^2}} \right) i_0 \quad (18)$$

where $V_D = V_B - V_C$; I_0 and i_0 are the DC and AC current components of M0 and $\beta_1 = \mu_n C_{ox} \left(\frac{W}{L} \right)_1$. For the maximum gain, V_C is set sufficiently low to fully turn off transistor M2, and the entire current of M0 flows through M1. If V_D is reduced, by increasing V_C , the current flowing through M1 reduces accordingly. Considering the pre-attenuation provided by the capacitive attenuator, the overall VGA's transconductance (Gm) can be computed as

$$G_m \approx \frac{1}{2^{i-1}} \left(\frac{1}{2} + \frac{\sqrt{\beta_1} V_D}{4 \sqrt{I_0 - \frac{1}{4} \beta_1 V_D^2}} \right) g_{m,0} \quad (19)$$

where i represents the index of the enabled Gm stage and $g_{m,0}$ is the small signal transconductance of M0.

4.4. Design of Gain-independent Impedance Matching Block

4.4.1. Broadband impedance matching configurations

Since the tuner input frequency range is between 400MHz and 900MHz, the input impedance matching needs to be broadband. Therefore, the typical low noise inductive degeneration configuration cannot be used. In principle, there are three ways to achieve the broadband input impedance matching, as shown in Fig. 4.8.

In Fig. 4.8 (a), the input impedance is provided by the simple resistive termination. The impedance matching is robust but the noise figure is large (over 3dB without considering the active circuit noise). Hence this topology is not suitable for low noise purpose.

In Fig. 4.8 (b), the input impedance matching is achieved using a common-gate configuration. Neglecting the parasitic capacitances and finite impedance of the current source, the input impedance will be decided by the transconductance of the common-gate transistor. This configuration provides less noise compared with the simple resistive

termination, but there are two drawbacks. First of all, the transconductance (g_m) of the input transistor is fixed due to matching requirement, and the noise performance of the circuit is fixed. Alternatively, this configuration cannot adjust the input transistor g_m for lower noise figure. Second of all, it is difficult to add the attenuator before this common-gate stage without affecting the input impedance. Common source and common gate cross-coupled configuration can help to reduce the noise figure [9], however, it cannot allow the attenuator to be added either. Therefore, this approach cannot be used for this design.

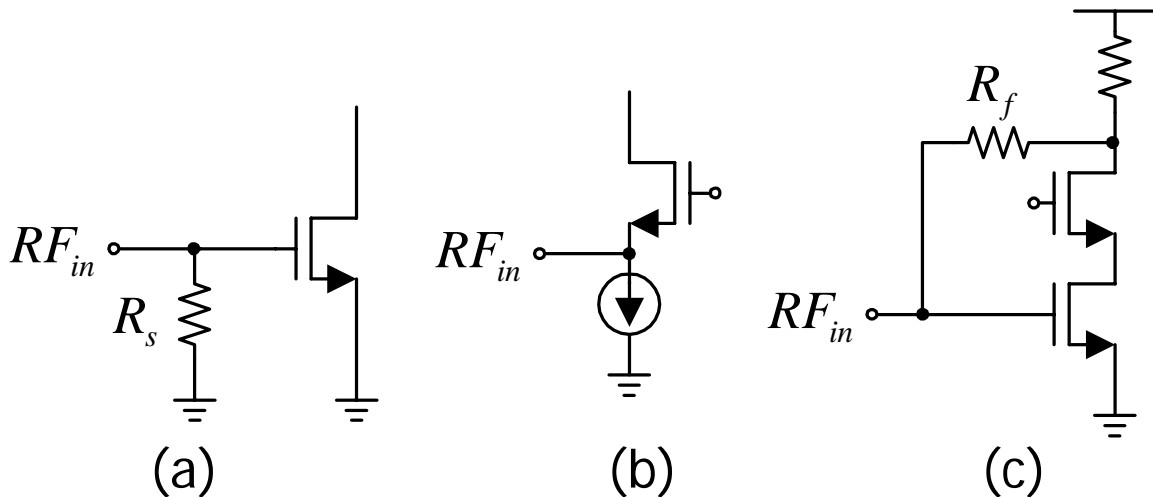


Fig. 4.8. Broadband impedance matching configurations

In Fig. 4.8 (c), the shunt-feedback input impedance matching configuration is shown. The input impedance is mainly determined as $\frac{R_f}{1+A}$, where A is the amplifier gain and R_f is the feedback resistor. In general, the larger the feedback resistor and the smaller the resistor noise contribution. Thus, the noise contribution from that resistor can be neglected assuming large amplifier gain. In addition, the feedback can practically cancel the bottom

transistor's input referred noise. Therefore, this configuration is widely used for low noise broadband impedance matching as demonstrated in [25]-[26].

However, notice that the input impedance for this configuration strongly depends on the amplifier's gain. In our case, the gain change of the RFVGA will change the input impedance and affect the input impedance matching performance, which is not acceptable. To overcome this issue, two approaches can be adopted: 1) adjusting the feedback resistor (R_f) simultaneously with the change of VGA gain such that the input impedance remains constant; or 2) modifying the amplifier to have constant open loop gain. If using the first approach, the value of the feedback resistor has to be adjusted with fine resolution, when the gain is varied by controlling V_c of the current-steering Gm stage, which increases the design complexity. Thus the second approach is used.

4.4.2. Modified shunt-feedback input impedance matching

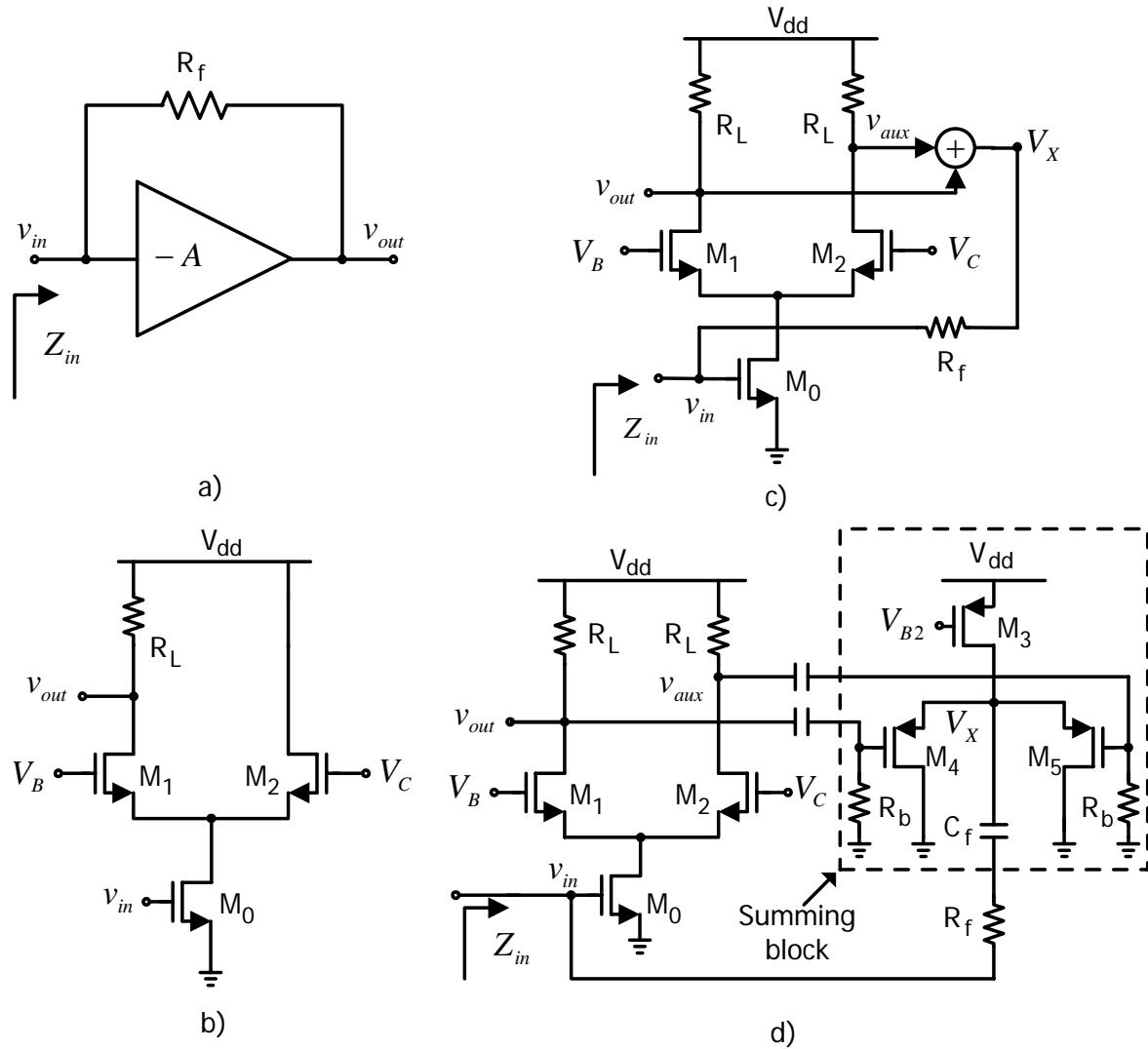


Fig. 4.9. (a) Block diagram of resistive shunt-feedback input impedance matching; (b) Simplified current-steering VGA schematic; (c) Simplified schematic of the proposed configuration; (d) Circuit implementation of the proposed shunt-feedback input impedance matching configuration

Fig. 4.8 (a) shows the conceptual block diagram of the shunt-feedback matching and a conventional current-steering VGA is shown in Fig. 4.9 (b); the voltage gain is controlled by V_C . Fig. 4.9 (c) shows a balanced topology by adding a resistor load at the drain of M2. The additional resistor allows the current of M2 to be used for input impedance matching. Notice that the sum of the in-phase signals v_{out} and v_{aux} equals $g_{m,0}R_L v_{in}$, which is independent of the gain control V_C . Therefore, $v_{out} + v_{aux}$ can be used to implement VGA's gain-independent shunt-feedback input impedance matching. Fig. 4.9 (d) shows the conceptual circuit implementation, where the summing block is implemented at the common-source node of an AC coupled PMOS differential pair. Defining the transconductance of identical devices M4 and M5 as $g_{m,4}$ and ignoring the parasitic capacitors, the input impedance Z_{in} without any pre-attenuation can be expressed as

$$Z_{in} = \frac{R_f + \frac{1}{2g_{m,4}}}{1 + \frac{1}{2}g_{m,0}R_L} \quad (20)$$

Since the capacitive pre-attenuation factor affects the overall loop gain; the shunt-feedback resistor has to be adjusted to provide constant input impedance when the pre-attenuation factor changes. When the i^{th} Gm stage enabled, the value of the feedback resistor must be adjusted according to the following relationship

$$R_f(i) = \left(1 + \frac{1}{2^i} g_{m,0} R_L\right) R_s - \frac{1}{2g_{m,4}} \quad (21)$$

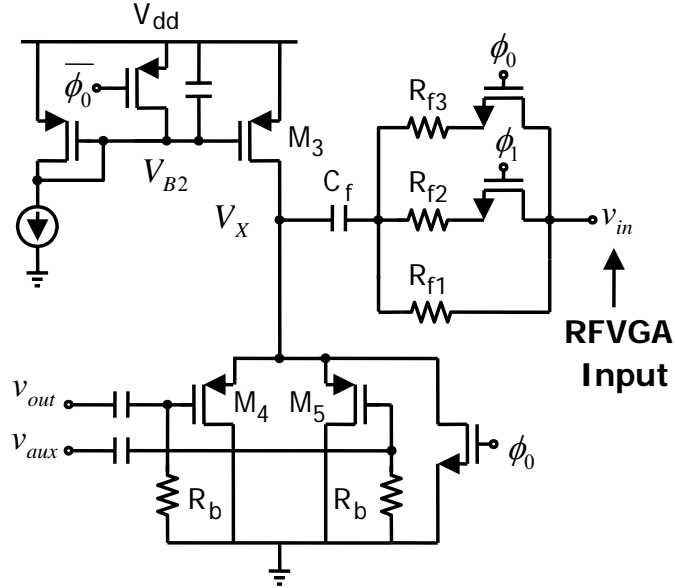


Fig. 4.10. Schematic of gain-independent input impedance matching block

When the pre-attenuation is large ($i \geq 3$), R_f value is close to R_s and there is no noise benefit to implement the feedback matching. To save power, for $i \geq 3$ the shunt-feedback network is disabled and simple resistive matching is used. The adaptive input impedance matching is digitally controlled by ϕ_0 and ϕ_1 as shown in Fig. 4.10. If ϕ_0 is set high to pull node V_X down and to disable the P-type current source; the simple resistor matching through $R_{f1} // R_{f3}$ ($=75\Omega$) is enabled. If ϕ_0 is set low, the shunt-feedback matching is enabled and ϕ_1 is used to adjust the feedback resistor when needed. The resistors are properly designed to ensure 75Ω input impedance for all gain settings.

4.4.3. Input impedance frequency response

In the previous analysis, the capacitors were ignored for simplicity, but all of them affect the frequency response of the input impedance. The AC coupling capacitor C_f (35pF) used in the input impedance matching block (Fig. 4.10) degrades the low frequency response of the impedance matching loop. The capacitive attenuator (Fig. 4.6) produces $2C_1$ capacitance from the RF input node to ground and degrades the high frequency impedance matching; C_1 (~ 0.3 pF) is mainly implemented by the M0 gate capacitance. The gate-drain capacitance is also accounted when equivalent capacitors were dimensioned; notice that miller effect in this case is not a major issue since the drain of M0 is connected to a low-impedance node due to the effect of M1 and M2, see Fig. 4.9 (d).

Another parasitic capacitor present at VGA output is denoted as C_L , not shown in Fig. 4.9 (d); this capacitor and R_L are responsible for VGA's dominant pole and affect the input impedance for the shunt-feedback configuration.

The input admittance for the simple resistive termination consisting of R_s ($R_f = R_s$) in series with C_f and the grounded capacitor $2C_1$ can be expressed as

$$G_{in} = \frac{s}{s + \frac{1}{R_s C_f}} \frac{1}{R_s} + 2sC_1 \approx \frac{1}{R_s} + 2sC_1 \quad (22)$$

In the second approximation, the term $\frac{1}{R_s C_f}$ is ignored for the frequency above 100MHz

because the pole frequency $\frac{1}{2\pi R_s C_f}$ is around 60MHz.

For the proposed shunt-feedback matching configuration, when the i^{th} G_m stage is active and equation (21) is valid, the input admittance can be approximated as

$$G_{in} = \frac{s}{s + \frac{1}{A_L} \frac{1}{R_s C_f}} \frac{s + A_L \omega_L}{s + \omega_L} \frac{1}{A_L R_s} + 2sC_1 \quad (23)$$

$$\approx \frac{1}{A_L R_s} \frac{\omega^2 + A_L \omega_L^2}{\omega^2 + \omega_L^2} + 2sC_1 \left[1 - \frac{1}{2R_s C_1} \frac{A_L - 1}{A_L} \frac{\omega_L}{\omega^2 + \omega_L^2} \right]$$

where $A_L = 1 + \frac{1}{2^i} g_{m,0} R_L$ and $\omega_L = \frac{1}{R_L C_L}$. The second expression (ignoring C_f) is a reasonable approximation for frequencies above 100MHz.

For both input matching configurations, $S_{11} = 20 \log \left| \frac{1 - G_{in} R_s}{1 + G_{in} R_s} \right|$ is further affected by C_f at

low frequencies and improves until the frequencies where the effects of $2C_1$ are relevant, as shown in Fig. 4.11 and Fig. 4.12. Comparing equation (22) and equation (23), smaller S_{11} for feedback matching configuration is obtained at medium frequencies because the imaginary part in equation (23) is partially cancelled by the feedback loop. At high frequencies, however, the real part in equation (23) reduces, which worsens S_{11} . In this

design, $C_f = 35\text{pF}$ and $C_1 = 0.3\text{pF}$ were chosen to ensure S_{11} less than -10dB from 100MHz to 900MHz , as shown in both Fig. 4.11 and Fig. 4.12.

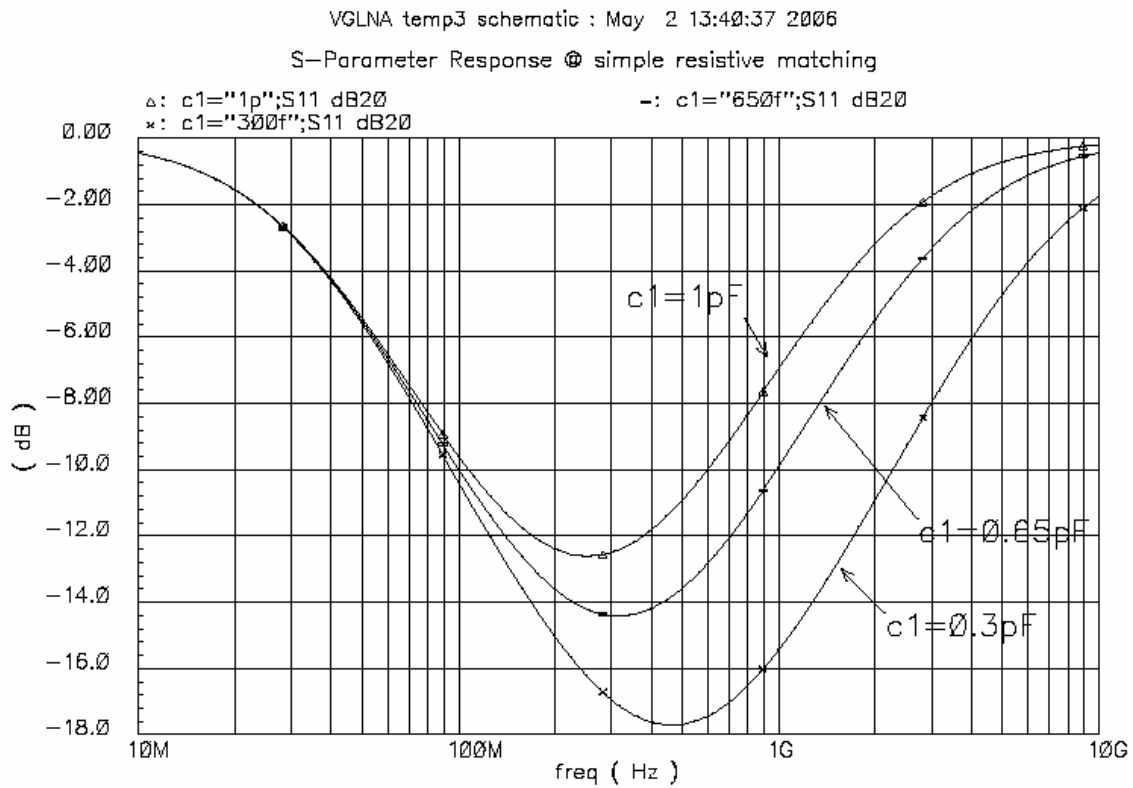


Fig. 4.11. Simulated S_{11} plots for different C_1 values @ simple resistive matching

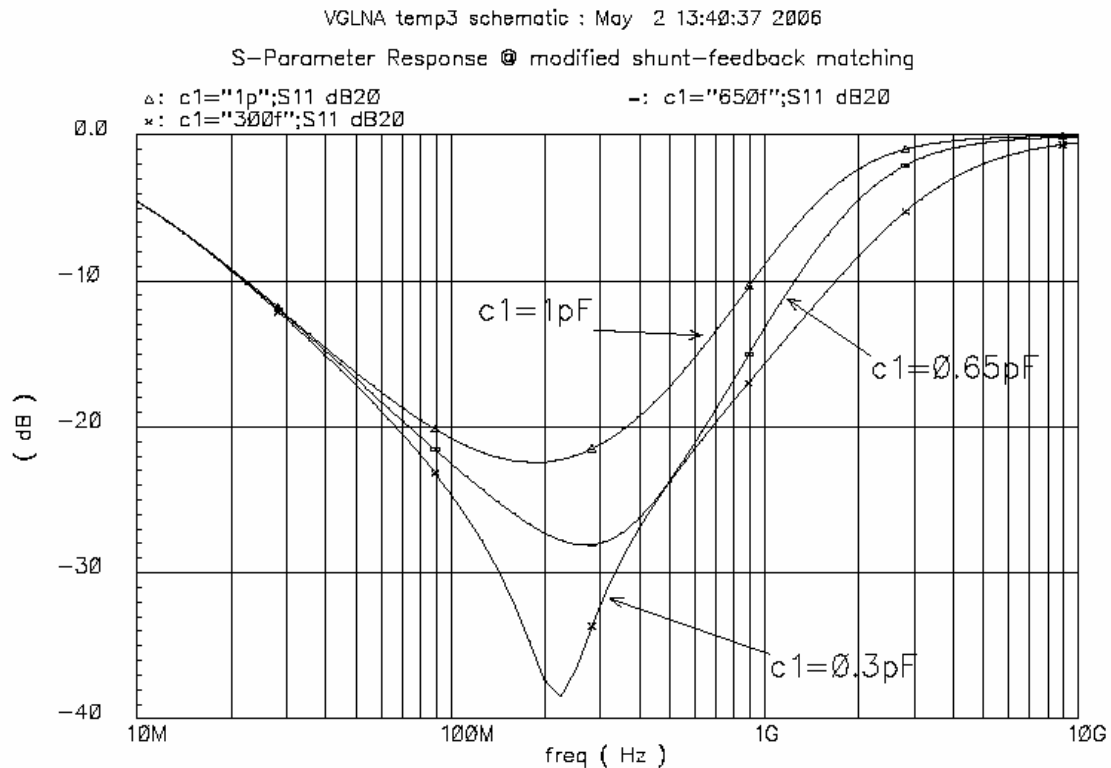


Fig. 4.12. Simulated S11 plots for different C1 values @ shunt-feedback matching

4.5. Design of Gain Control Block

In order to smoothly adjust the VGA's gain with 1dB resolution, a gain control block based on a master-slave technique is implemented to generate V_C . There are multiple advantages with that implementation. First, the gain control block can generate analog control voltage based on digital control input, which can introduce negligible glitches during the gain adjustment. Second, the accuracy of the gain control is independent of process and temperature variations and only limited by the on-chip matching performance of the components.

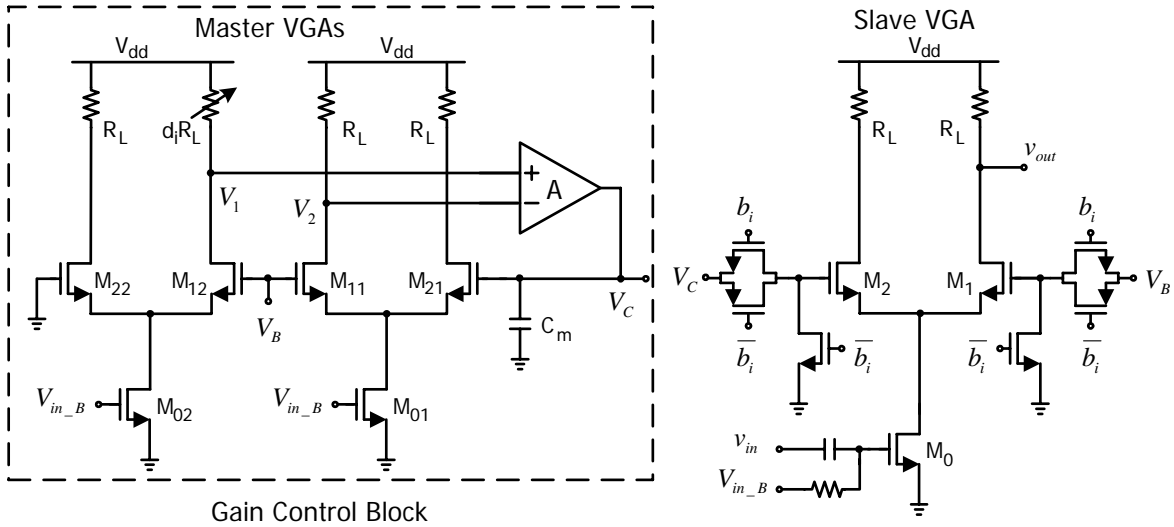


Fig. 4.13. Schematic of the gain control concept circuit

The conceptual circuit of the gain control block is shown in Fig. 4.13; two replicas of the main VGA are used. The DC bias voltage V_{in_B} is applied to the gate of M_{01} , M_{02} , and M_0 to ensure equal bias currents. M_{22} is permanently off, therefore the current from transistor M_{02} flows through M_{12} . M_{12} is loaded by a digitally controlled resistive bank $d_i * R_L$. The high DC gain amplifier (A) forces $V_1 = V_2$ and the capacitor C_M is designed large enough to stabilize the control loop and also minimize the loop noise. V_C is

generated automatically to adjust the DC current of M_{11} to satisfy the condition $\frac{I_{11}}{I_{01}} = d_i$

since $I_{01} = I_{02}$. The control voltage V_C is also applied to the main VGA, leading to $\frac{I_1}{I_0} = d_i$.

Ignoring the channel length modulation effects, the small signal transconductance of the

main VGA can then be approximated as $\frac{\sqrt{d_i}}{\sqrt{d_i} + \sqrt{1-d_i}} g_{m,0}$, where $g_{m,0}$ is transistor M_0 's

transconductance. To have 1dB gain step, a look-up table for d_i is generated as $[1, 0.97, 0.92, 0.83, 0.69, 0.51]$. The resistive array $d_i * R_L$ is implemented as shown in Fig. 4.14. Because the gain is only controlled by d_i (ratio of resistors), process parameter tolerances and temperature variations have negligible effects on the gain control accuracy.

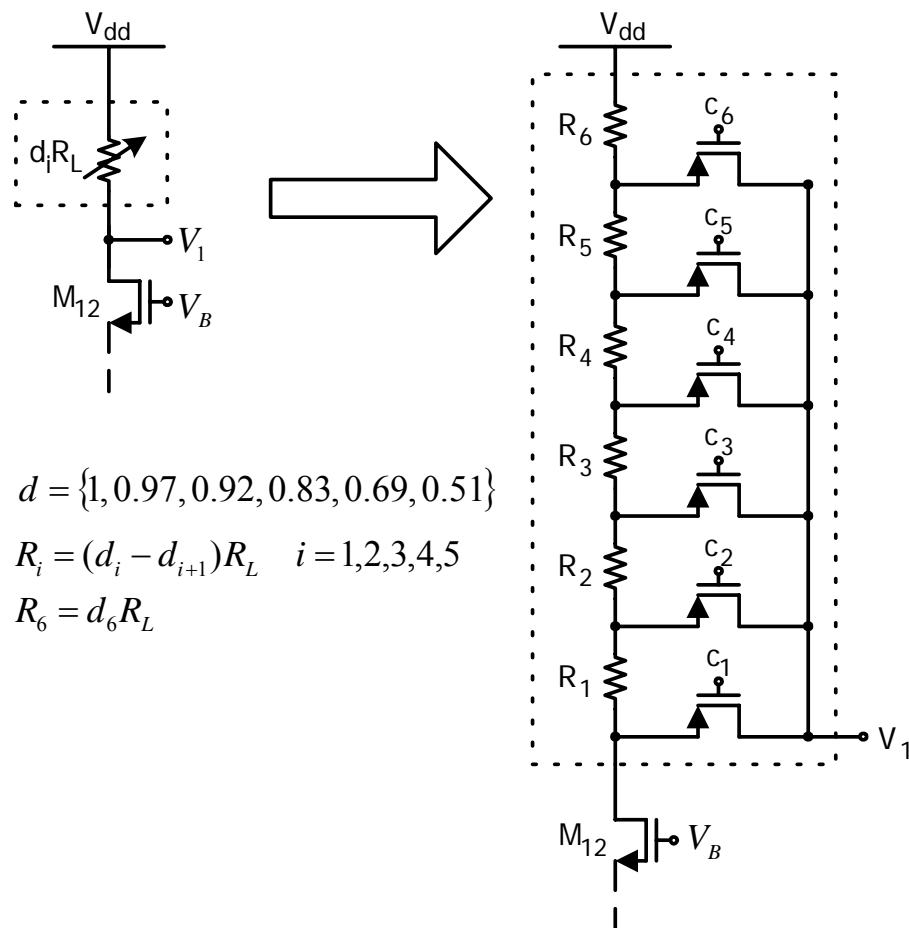


Fig. 4.14. Schematic of digital control variable resistor implementation

The accuracy of the gain control is mainly affected by the unavoidable transistor non-idealities and mismatches. If the gain and input offset of the amplifier shown in Fig. 4.13

are defined as A and V_{os} , respectively, and if the composite mismatch between the master VGAs is assumed to be δ_1 and the mismatch between the master VGA and slave VGAs is denoted by δ_2 , then using conventional circuit analysis techniques, the following relationships can be derived

$$\frac{I_1}{I_0} = (1 + \delta_2) \left[(1 + \delta_1) d_i + \frac{1}{AI_{01}R_L} (V_C - V_{C_ini}) + \frac{V_{os}}{I_{01}R_L} \right] \quad (24)$$

$$G_m = \frac{\sqrt{\frac{I_1}{I_0}}}{\sqrt{\frac{I_1}{I_0} + \sqrt{1 - \frac{I_1}{I_0}}}} g_{m,0} \quad (25)$$

where V_{C_ini} is the value of V_C when $d_i = 1$. According to equation (24), the non-idealities have different effects for different gain settings (d_i). The worst case occurs when the d_i is in the range of 1 and 0.97 (large gain settings); due to the finite value of A and the presence of V_{os} more than one gain control setting can force $\frac{I_1}{I_0} = 1$ (or 0.97), which results in non-monotonic gain adjustment that should be avoided. To minimize these errors, the amplifier's gain A is required to be over 40dB; $I_{01}R_L$ is in the range of 700mV. The loop DC offset V_{os} should be maintained below 10mV. Meanwhile, $\delta_1 + \delta_2$ has to be kept less than 3% to ensure VGA's gain monotonicity. Large transistor areas and proper layout techniques must be used to achieve the aforementioned level of accuracy.

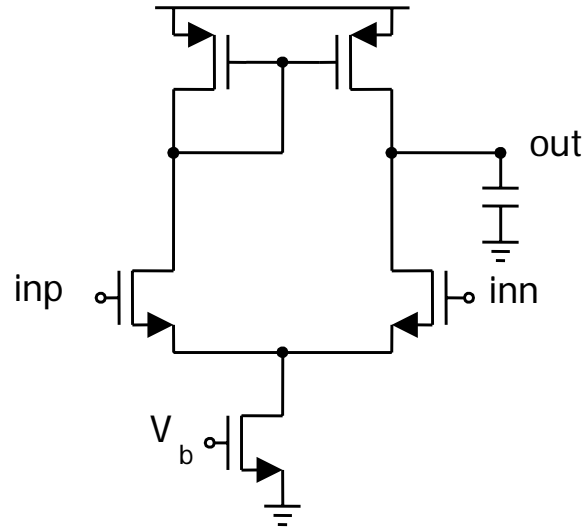


Fig. 4.15. Schematic of the amplifier used in gain control block

In order to achieve the gain control accuracy, the amplifier is designed using a differential pair and current mirror load, as depicted in Fig. 4.15. Long channel devices ($L=1\mu\text{m}$) are used for this amplifier to improve the matching and minimize the offset voltage. A large NMOS capacitor is used at the output node, to stabilize the control loop. The simulated gain of the amplifier is over 40dB for all of the corners and the phase margin is well guaranteed above 60 degree.

4.6. Noise and Linearity Analysis

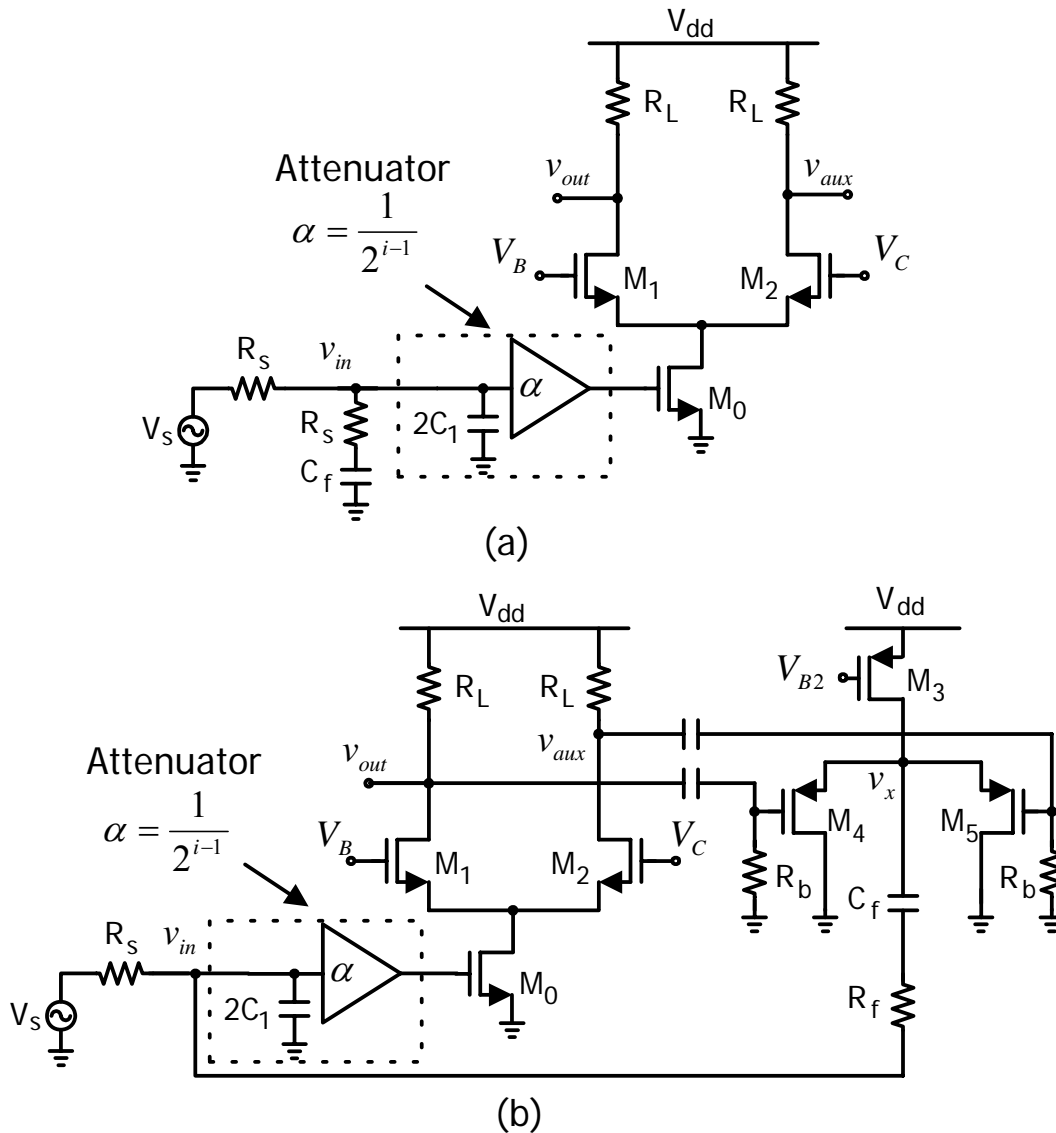


Fig. 4.16. Simplified schematic of the RFVGA: (a) with simple resistive termination input impedance matching (b) with proposed shunt-feedback input impedance matching

Since noise and linearity performances are affected by the input matching, the analysis is carried for both configurations (resistive termination and shunt-feedback). The simplified

configurations of the proposed RFVGA are shown in Fig. 4.16. The gain control block is ignored in the analysis because it only provides DC bias and has negligible effect to the main VGA's noise and linearity performance.

4.6.1. Noise analysis

To simplify the noise analysis, the channel current noise is considered the dominant transistor noise contribution and its current spectral noise density is modeled as $4kT\gamma g_m$, where γ is a fitting parameter. If ideal input impedance matching is assumed, the noise factor of Fig. 4.16 (a) can be approximated as

$$F_a \approx 2 + \frac{1}{\alpha^2} \frac{4\gamma}{g_{m,0} R_s} + \frac{1}{\alpha^2} \left(\frac{g_{m2}}{g_{m,0}} \right)^2 \left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}} \right) \frac{4\gamma}{R_s} + \frac{1}{\alpha^2} \left(\frac{g_{m1} + g_{m2}}{g_{m,0} g_{m,1}} \right)^2 \frac{4}{R_L R_s} \quad (26)$$

The noise contribution due to source and input resistors is represented by the first term, which makes the noise figure over 3dB for all gain settings. The remaining terms represent the noise contributions due to M0, M1 and M2 and the load resistor R_L , respectively.

Similarly, the noise factor of Fig. 4.16 (b) can be approximated as

$$\begin{aligned}
F_a \approx F_b \approx & 1 + \frac{1}{\alpha^2} \left(\frac{2 + \frac{1}{2} \alpha g_{m,0} R_L}{2 + \alpha g_{m,0} R_L} \right)^2 \frac{4\gamma}{g_{m,0} R_s} + \frac{1}{\alpha^2} \left(\frac{g_{m,2}}{g_{m,0}} \right)^2 \left(\frac{1}{g_{m,1}} + \frac{1}{g_{m,2}} \right) \frac{4\gamma}{R_s} \\
& + \frac{1}{\alpha^2} \left(\frac{2 + \frac{g_{m,1} + 2g_{m,2}}{2g_{m,1} + 2g_{m,2}} \alpha g_{m,0} R_L}{2 + \alpha g_{m,0} R_L} \right)^2 \left(\frac{g_{m,1} + g_{m,2}}{g_{m,0} g_{m,1}} \right)^2 \frac{4}{R_L R_s} \\
& + \left(\frac{1}{2 + \alpha g_{m,0} R_L} \right)^2 \left(\frac{R_L}{R_s} + \frac{\left(2 + \frac{g_{m,3}}{g_{m,4}} \right) \gamma}{g_{m,4} R_s} + \frac{4R_f}{R_s} \right)
\end{aligned} \tag{27}$$

The second term represents the noise contribution of M0, which is slightly smaller than its counterpart in equation (26) for the same α . The noise reduction is attributed to the noise canceling of the feedback configuration [26]; the larger the feedback factor $\alpha g_{m,0} R_L$ the more noise from M0 can be cancelled. The third and fourth terms represent the noise contributions due to M1, M2 and R_L . The noise contributions from the additional impedance matching block, including R_L in the v_{aux} branch, the summing block and the feedback resistor, are shown in the final term. Notice that the last term is less than 1 for the high gain settings because of very small coefficient $\frac{1}{(2 + \alpha g_{m,0} R_L)^2}$. In general, due to partially canceling the noise of M0 and lower noise contribution from the input matching block, lower noise factors can be achieved in equation (27) than in equation (26) for the same VGA gain settings. Also, when α decreases (small gain settings), the noise figure

difference between equation (26) and equation (27) reduces and the improvement due to proposed shunt-feedback matching becomes negligible. The main reasons are: 1) input referred noise due to the active G_m stage becomes more dominant due to the increased attenuation factor; 2) less input referred noise from M0 is cancelled since the control loop gain decreases; 3) the noise contribution due to R_f increases since its value must be lowered to maintain the impedance matching. Therefore, when $\alpha \leq \frac{1}{4}$, the shunt-feedback is disabled and impedance matching is achieved using the simple resistive termination.

4.6.2. Linearity analysis

The weak non-linearity performance (like IIP3) of the RFVGA in Fig. 4.16 (a) is mainly defined by the nonlinear behavior of transistor M0. In addition, the RFVGA linearity improves with large attenuation factors, provided that the attenuator itself is not a limiting factor.

In principle, for the same gain setting, the linearity of the configuration in Fig. 4.16 (b) is lower than the configuration Fig. 4.16 (a) due to the additional nonlinearities of the summing block and feedback network. However, the summing block exhibits good linearity and the linearity difference between these two configurations is usually negligible.

Ignoring the parasitic capacitors and assuming that transistor's current follows the conventional square law, the voltage at node V_x (Fig. 4.16 (b)) can be approximated as

$$v_X \approx a_1 v_T + a_2 v_T^2 + a_3 v_T^3 + \dots \quad (28)$$

where $v_T = v_{out} + v_{aux}$ and the coefficients a_i are given as follows:

$$\begin{aligned} a_1 &= \frac{g_{m,4} R_0}{2g_{m,4} R_0 + 1} \\ a_2 &= \frac{g_{m,4} R_0 \left((2k-1)^2 (2g_{m,4} R_0 + 1)^2 + 1 \right)}{4V_{dsat,4} (2g_{m,4} R_0 + 1)^3} \\ a_3 &= -\frac{(g_{m,4} R_0)^2 \left((2k-1)^2 (2g_{m,4} R_0 + 1)^2 + 1 \right)}{4V_{dsat,4}^2 (2g_{m,4} R_0 + 1)^5} \end{aligned} \quad (29)$$

In these expressions $k = \frac{v_{out}}{v_T}$; $R_0 = R_s + R_f$ is the overall load resistor at the summing

block and $V_{dsat,4} = V_{GS,4} - V_{TH}$.

In equation (28), a_1 leads to the fundamental component $0.5v_T$, while a_2 and a_3 represent the second and third-order distortion coefficients, respectively. Two desired properties of the summing block are observed in equation (29): 1) Due to the inherent source degeneration by R_0 , the linearity of this block is superior to that of a single transistor; the term $2g_{m,4} R_0 + 1$ in the denominator shows this effect; 2) Although not evident in equation (29), another relevant advantage of the summer block is that its linearity improves for small gain settings (large input signals); in this case v_{out} and v_{aux} have similar signal swing ($k \approx 0.5$) and the coefficients a_2 and a_3 decrease. In fact, when $k = 0.5$, the summing

block operates as a source follower with a source degeneration factor given by $2g_{m,4}R_0$ and preserves the linearity of the RFVGA.

4.7. Experimental Results

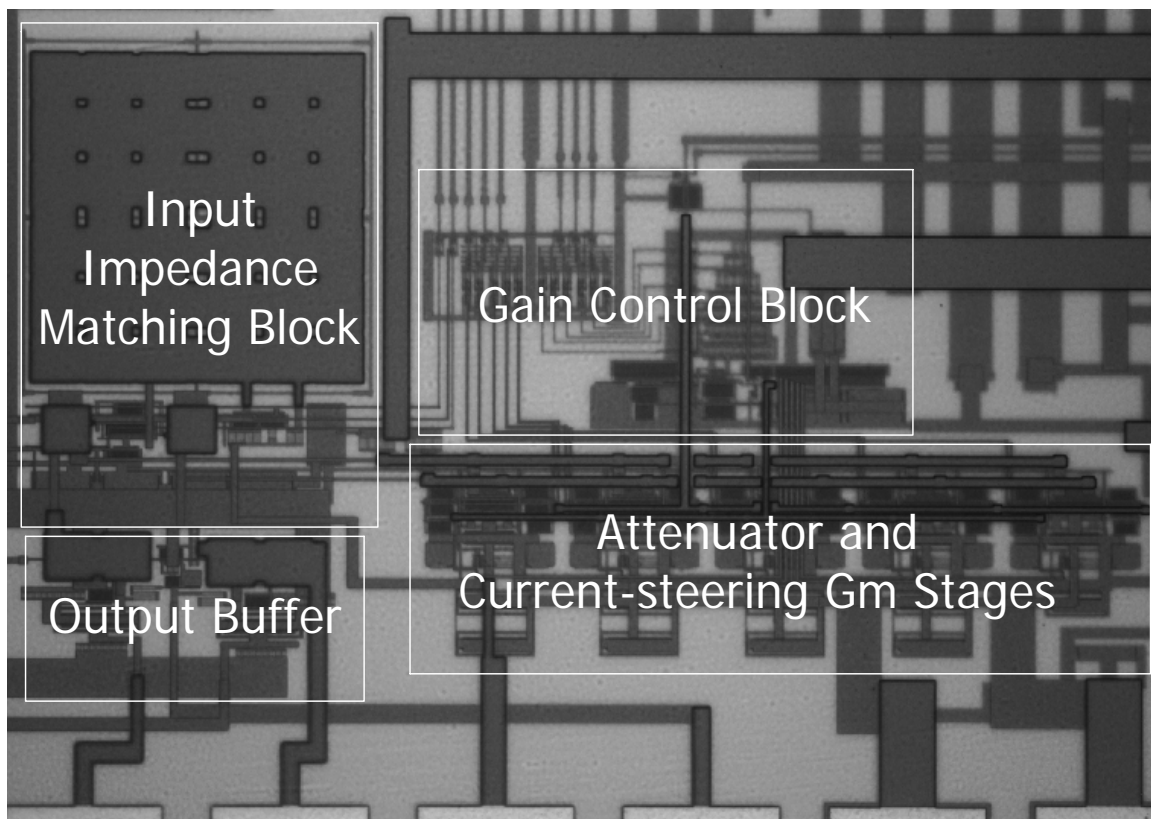


Fig. 4.17. Photograph of the RFVGA test chip

The RFVGA was fabricated in $0.18\mu\text{m}$ CMOS one poly six-metal technology through the MOSIS educational service; the chip microphotograph is shown in Fig. 4.17. There are two identical buffers included in the chip used to achieve output impedance matching and

characterize the buffer performance, respectively. The overall active area is around $0.74\text{mm}\times 0.43\text{mm}$.

4.7.1. Gain measurement

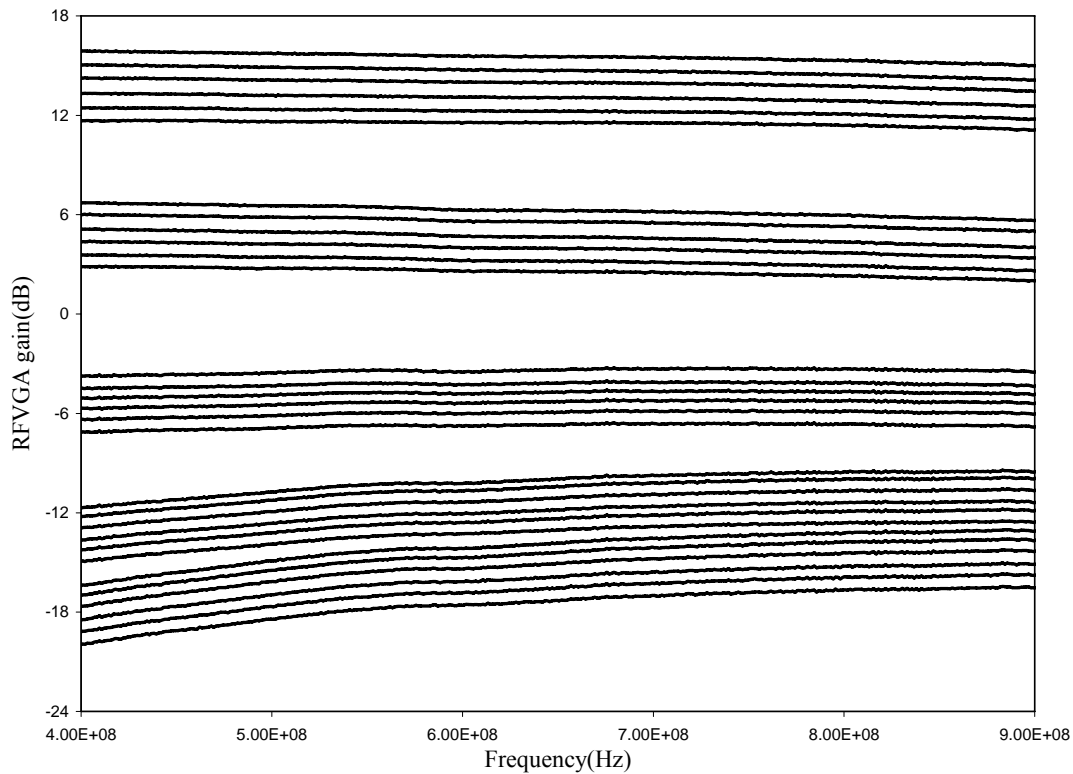


Fig. 4.18. Measured RFVGA gain vs. frequency

Fig. 4.18 shows the measured RFVGA power gain (S21). Within each Gm stage, the measured gain step is around 0.8dB, which proves that the proposed gain control scheme works properly. For each gain setting, the magnitude gain variation from 400MHz to 900MHz is less than 2dB.

Unexpected large gain steps occur when switching between G_m stages. These effects are due to the lack of accuracy in the capacitive attenuator. The capacitive attenuator of Fig. 4.6 was implemented using deep N-well MOS transistors as shown in Fig. 4.19, where C_1 is implemented by the input transistor of the G_m stage (M_0) and $2C_1$ is implemented by the auxiliary transistors $MC1$ and $MC2$ (gate-channel capacitance). There is a reverse-biased parasitic diode from the bulk to the deep N-well; its cathode terminal is connected to a clean V_{dd} . Unfortunately, diodes' parasitic capacitors were not accurately predicted from the simulations, which results in higher attenuation than expected when switching from one G_m stage to another one. These effects have been verified in Cadence simulations with a more accurate modeling of deep N-well transistors. To avoid this issue, $MC1$ and $MC2$ should be replaced by MIM capacitors [22].

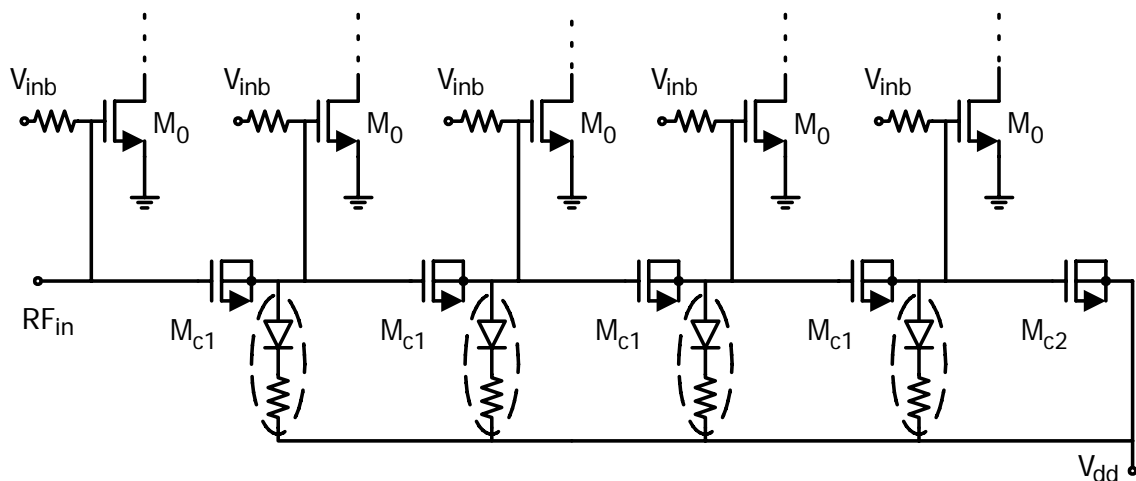


Fig. 4.19. Schematic of the capacitive attenuator with parasitic diodes and resistors

4.7.2. Input impedance matching performance measurement

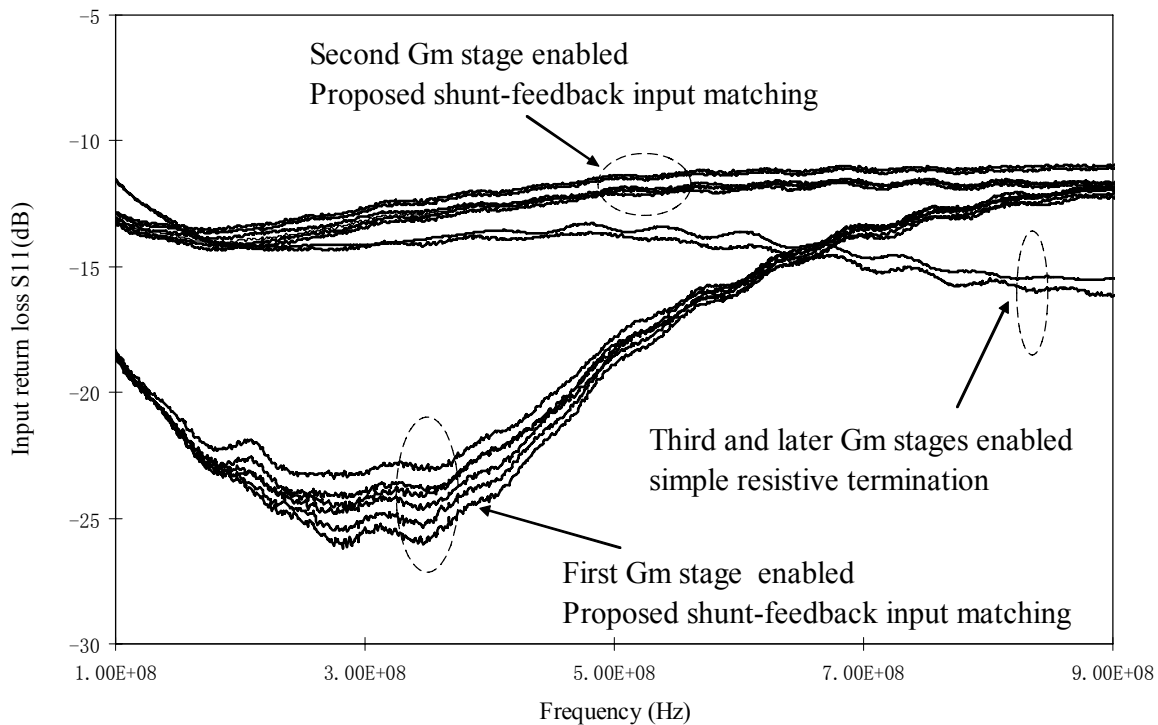


Fig. 4.20. Measured input return loss (S11) vs. frequency

The measured input return loss (S11) is shown in Fig. 4.20. When the first G_m stage is enabled, S11 curves agree well with the expected behavior; input matching is affected at low frequency by the blocking capacitor C_f , while at very high frequencies S11 is limited by the capacitors C_L and C_1 . When the second G_m stage is enabled, S11 is higher than expected. As aforementioned, the higher capacitive attenuation factor reduces the loop gain, leading to larger input impedance and degrading the input matching performance. For the third-fifth G_m stages, the simple resistive matching configuration is enabled; in this last case, the S11 improves at high frequencies because the resistor is slightly larger than the

ideal 75Ω and bond wire inductance combined with parasitic capacitors of the package improve the high frequency impedance matching.

4.7.3. Noise figure measurement

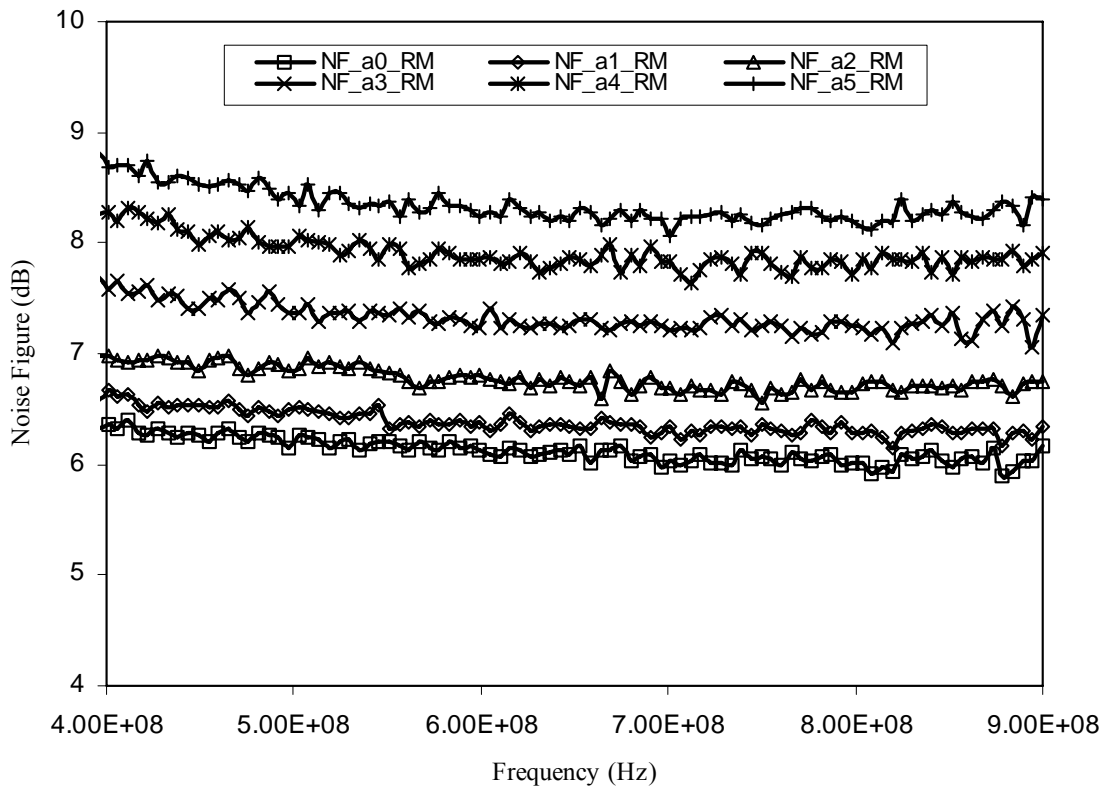


Fig. 4.21. Measured RFVGA noise figure with simple resistive matching (first six high gain settings)

To compare the noise performance of the proposed shunt-feedback configuration with conventional resistive termination, noise figures at the six highest gain settings for both input impedance matching configurations have been measured; the results are shown in Fig.

4.21 and Fig. 4.22. According to these results, the proposed shunt-feedback matching shows lower noise figure by roughly 1.7dB.

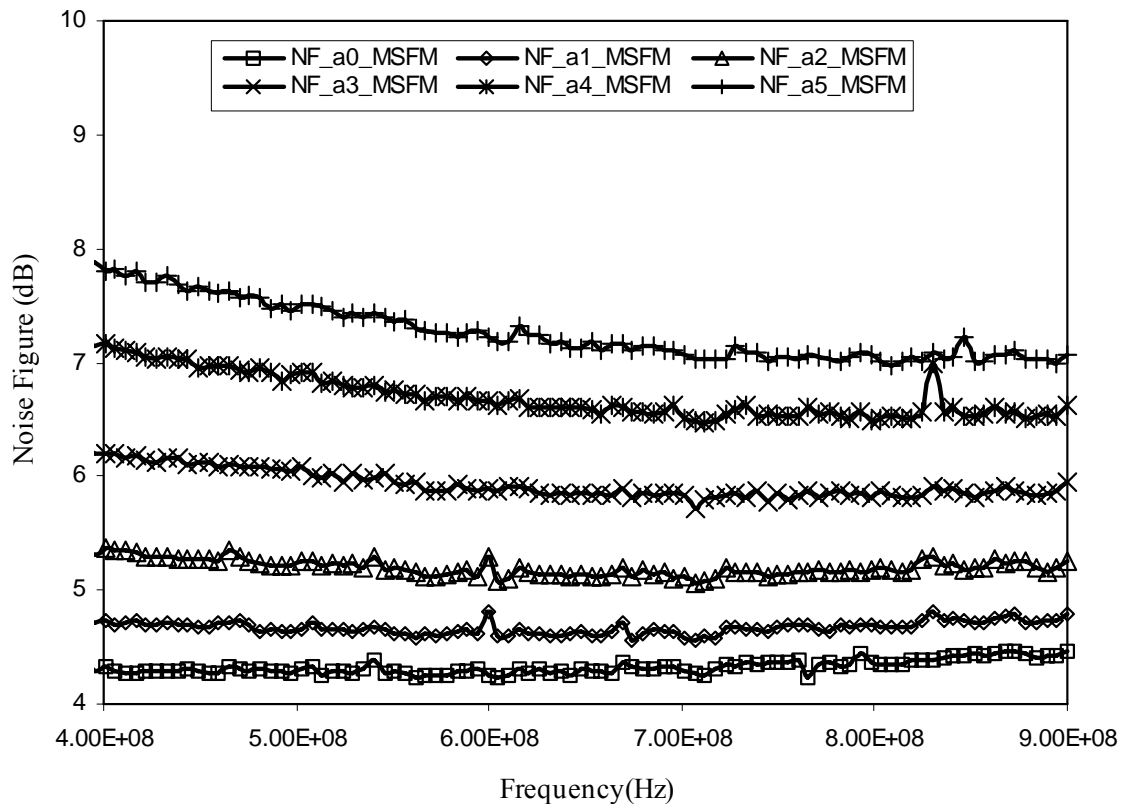


Fig. 4.22. Measured RFVGA noise figure with modified shunt-feedback matching (first six high gain settings)

The noise figure of the RFVGA for all of the gain settings have been measured and will be provided late. Notice for the first 12 highest gain settings, the input impedance is matched with modified shunt-feedback and other gain settings disables the feedback loop to use simple resistive matching.

4.7.4. Two tone test

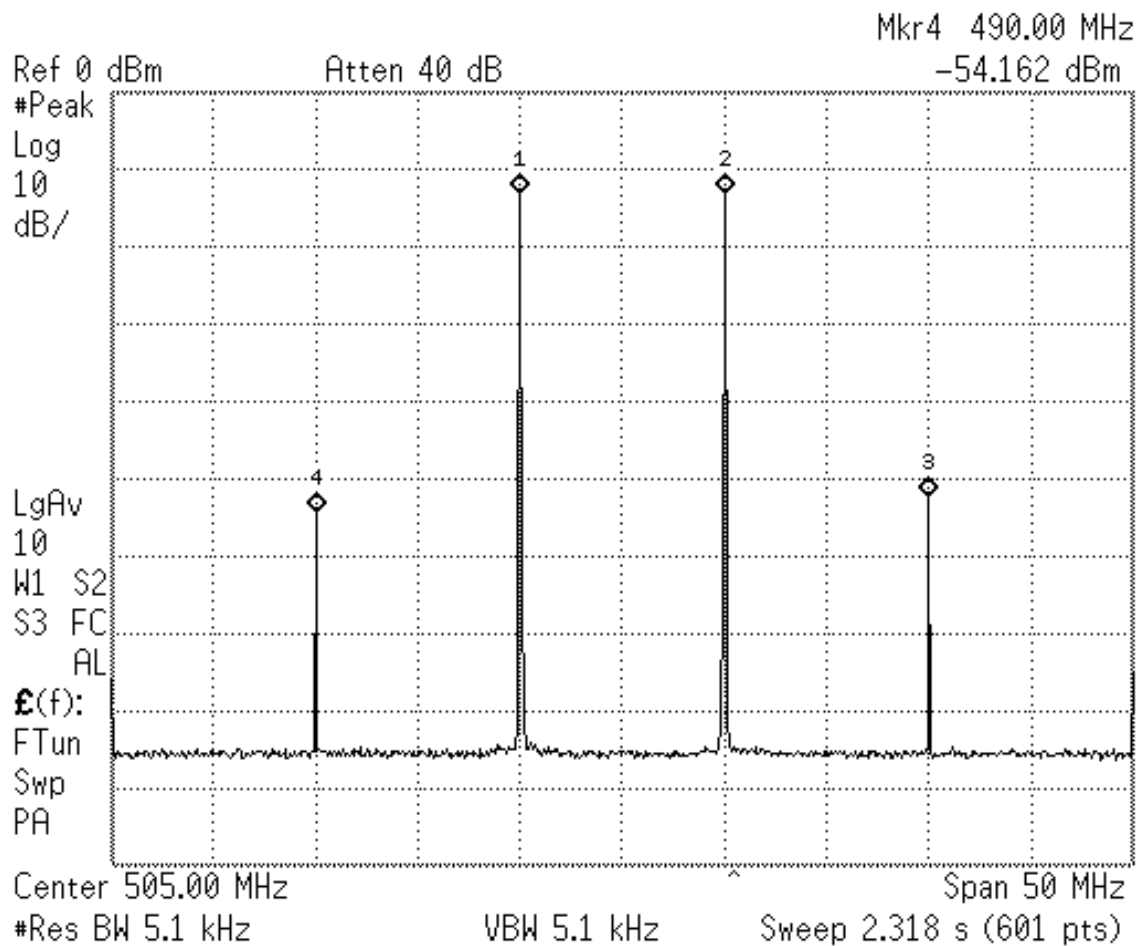


Fig. 4.23. Output spectral plot for the two tone test @ 500MHz & 510MHz inputs (-20dBm)

and the maximum gain setting

Two-tone test is a typical method to measure the RF non-linearity performance. In the test, two fundamental tones with same power and small frequency distance need to be applied in the system input. And the output power of fundamental tones and third order inter-modulation tones can be measured. The input power is swept and the IIP3 was extrapolated from the plot.

Fig. 4.23 shows the spectrum of the output when 500MHz and 510MHz tones (-20dBm each) were applied, while the RFVGA gain was set as the maximum. The output power of the fundamental signal is -13dBm and the power of IM3 tone (490MHz and 520MHz) is around -54dbm. Fig. 4.24 presents the IIP3 plot when the input power is swept from -34dBm to -14dBm; the extrapolated IIP3 at 500MHz for the maximum gain setting is 1dBm.

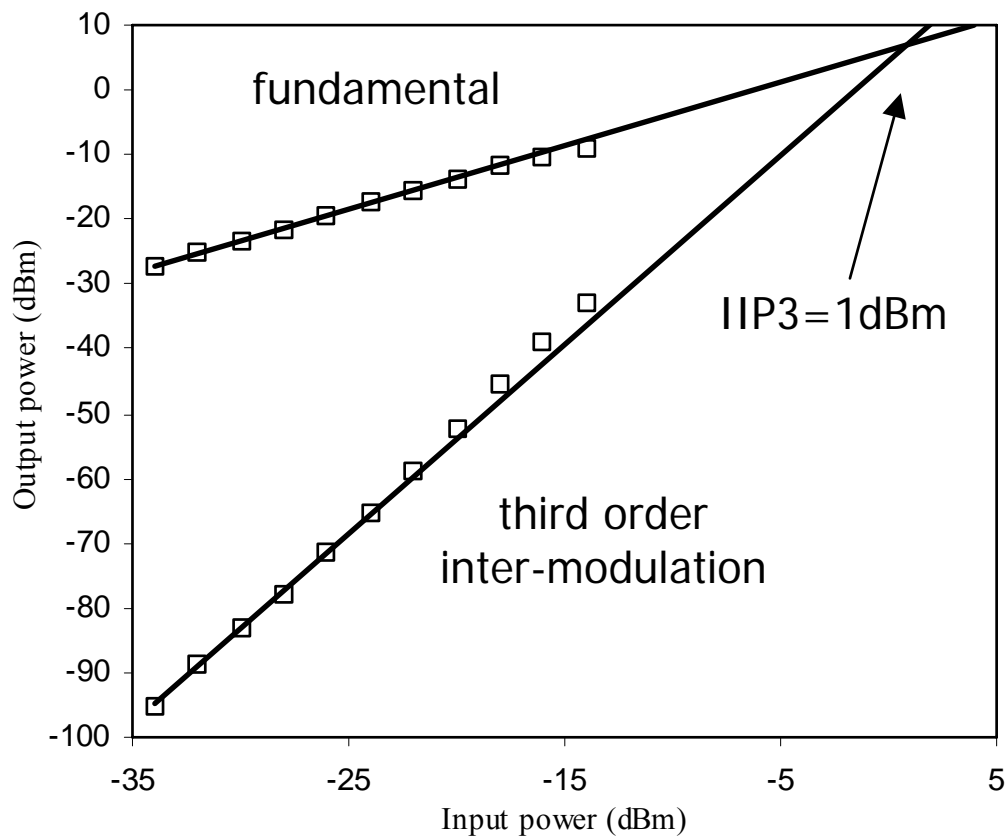


Fig. 4.24. IIP3 plot for the two tone test @ 500MHz & 510MHz inputs (-20dBm) and the maximum gain setting

The IIP3 performance for different gain settings and different frequencies has been measured and will be discussed below.

4.7.5. Overall dynamic range measurement

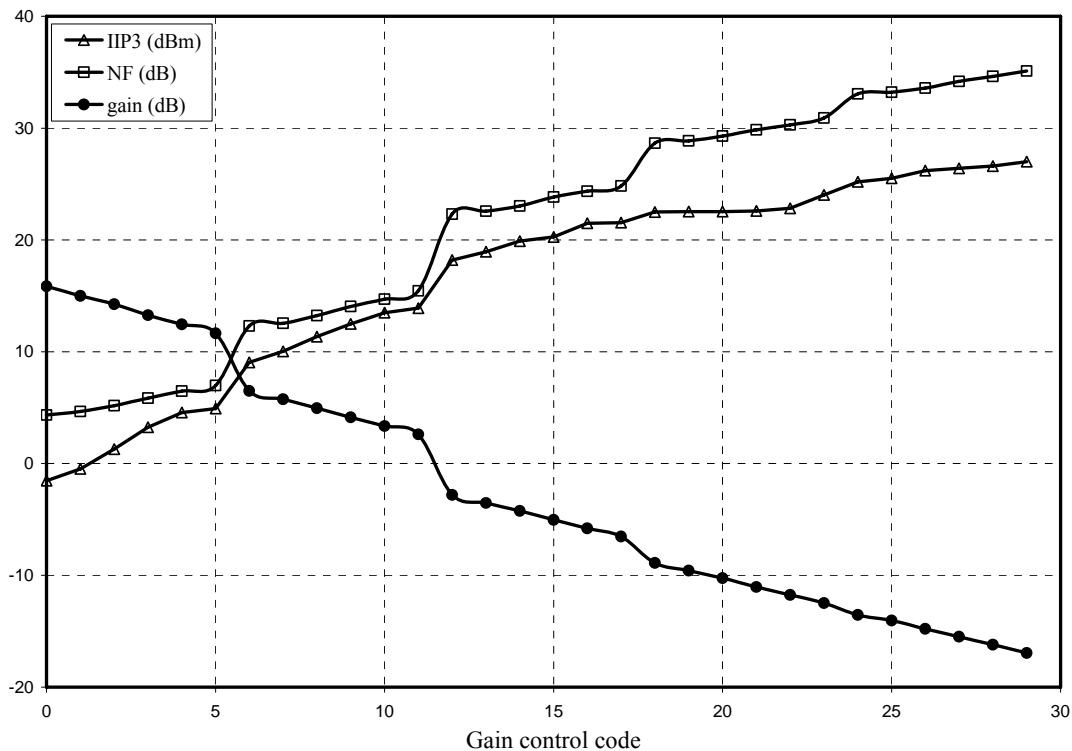


Fig. 4.25. Measured RFVGA gain, NF and IIP3 vs. gain control setting @ 800MHz

The overall performance of the RFVGA, including gain NF and IIP3, as function of gain control settings have been measured across different frequencies. As we expected, these parameters does not show dramatic variation with the frequency. Therefore, only the performance at 800MHz is given in Fig. 4.25 for the overall performance demonstration. The measured gain can be adjusted from 16dB down to -17dB. Correspondingly, the noise figure increases from 4.3dB to 35dB and IIP3 increases from -1.5dBm up to 27dBm.

The entire RFVGA consumes 12.3mA static current with 1.8v single power supply when the shunt-feedback is enabled; 6mA is used by the G_m stage and 2mA is consumed by the input impedance matching block, while the rest is for the gain control block and bias. A summary of measured results are given in Table 4.1.

Table 4.1. Summary of the RFVGA experimental results

Parameter	MEASURED VALUE
Frequency Range	470MHz to 870Mhz
Gain	16dB to -17dB
Noise Figure	4.3dB @ 16dB gain 15dB @ 3dB gain -35dB @ -17dB gain
IIP3	-1.5dBm @ 16dB gain 14dBm @ 3dB gain 27dBm @ -17dB gain
Input return loss	< -11dB
Power Consumption	22 mW ($V_{dd}=1.8V$)
Area	0.32mm ²

4.8. Conclusion

A high dynamic range CMOS RFVGA suitable for mobile DTV tuner applications has been presented. To provide low noise input impedance matching for the RFVGA, a shunt-feedback input matching scheme has been proposed. Also, a gain control block is implemented to achieve accurate gain control for the current-steering VGA. The experimental results of the prototype validate the proposed techniques. This work meets the requirements for the mobile DTV (UHF band) application and there is no need for an external or internal fixed gain LNA, while input matching is maintained under -11dB.

CHAPTER V

HIGH DYNAMIC RANGE DOWN-CONVERSION MIXER DESIGN

5.1. Introduction

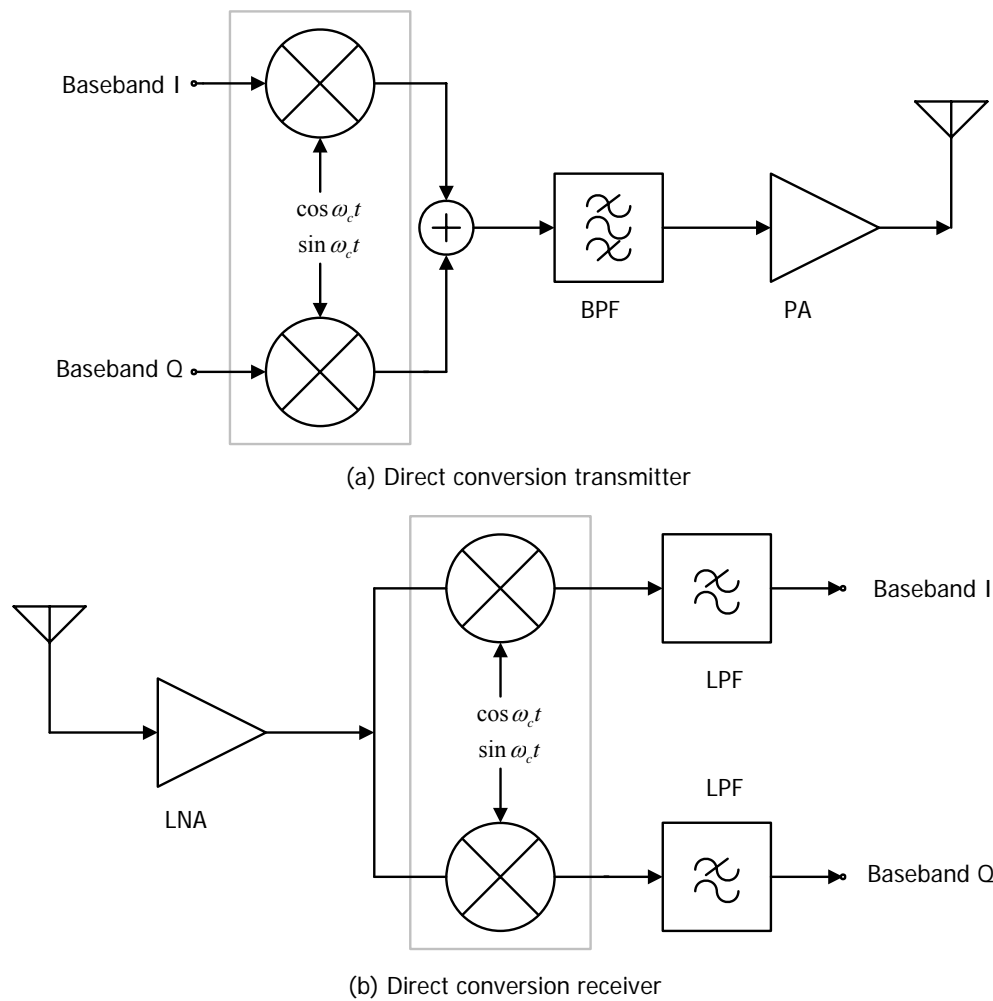


Fig. 5.1. Block diagram of direct conversion transmitter and receiver

Mixer is the block that performs frequency translation by multiplying two signals. It has two inputs (RF and LO) and the output is usually the product of these two inputs. For

example, as shown in Fig. 5.1 (a), mixers are used in the direct conversion transmitter to up-converted the desired baseband data to specific RF frequency; in Fig. 5.1 (b), they are used in the direct conversion receiver to down-converted the desired channel from RF frequency to baseband.

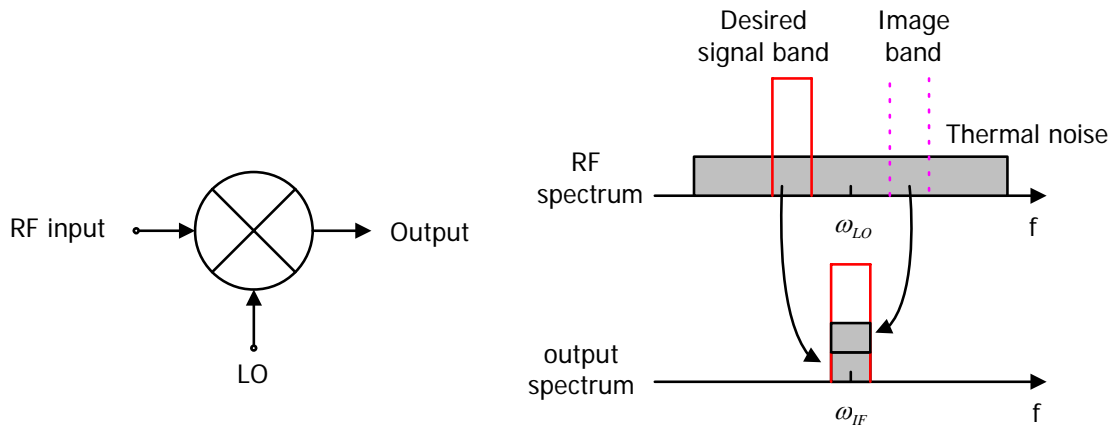
5.1.1. Key specifications for the mixer

5.1.1.1. Conversion gain

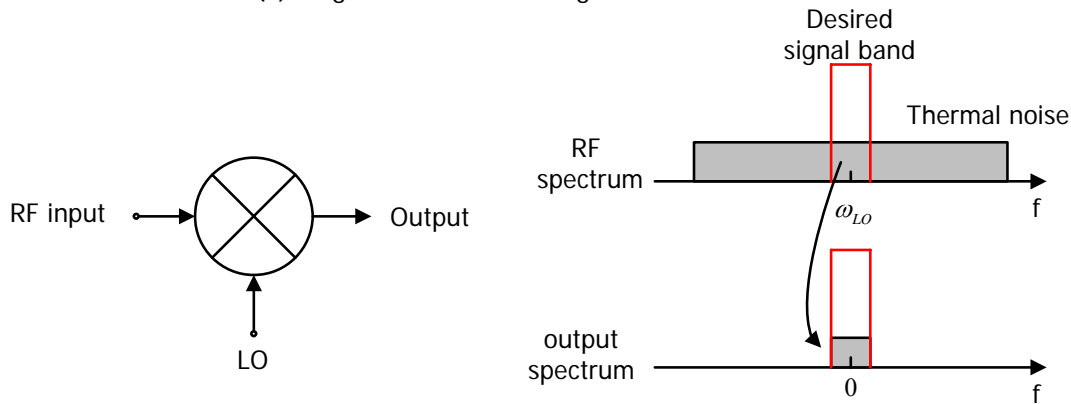
The conversion gain of the mixer is defined as the ratio of the output signal level and input signal level. Notice that the output signal and input signal locate at different frequencies. The signal level can be specified as voltage level or power level. Correspondingly, the conversion gain will be voltage conversion gain or power conversion gain. For the discrete mixer, the input and output impedance matching are usually required and it is convenient to use the power conversion gain for the characterization. For the fully integrated system, there is no power matching requirement between mixer and other blocks and voltage conversion gain is preferred. Nevertheless, if the matched input impedance and output impedance are same, the power conversion gain will be equal as voltage conversion gain.

5.1.1.2. Noise figure

The noise figure of the mixer can be defined as the ratio of input SNR and output SNR. In general, there are two types of noise figures such as double sideband (DSB) noise figure and single sideband (SSB) noise figure, as addressed in Fig. 5.2.



(a) Single side band noise figure



(a) Double side band noise figure

Fig. 5.2. Double side band noise figure and single side band noise figure

For a low-IF receiver, the incoming RF signal will be down-converted to an intermediate frequency, as shown in Fig. 5.2 (a). Without considering the noise added due to the mixer implementation, the incoming thermal noise in the RF frequency band will be down-converted to intermediate frequency. At the same time, the thermal noise in the image band ($2\omega_{IF}$ away from the signal band) will also be down-converted to intermediate frequency, which is similar as the image issue. Therefore, even if the mixer is noiseless; the noise figure of the mixer will be 3dB. In principle, this is because the desired signal band locates

only one side of the LO frequency. Therefore this type of noise figure is called as single-sideband noise figure.

If it is the direct conversion receiver, the incoming RF signal will be down-converted to baseband, as shown in Fig. 5.2 (b). In the same time, the thermal noise in the RF signal band will be down-converted to baseband also. Because the desired signal band locates on both side of the LO frequency, if the mixer is noiseless, the noise figure will be 0dB. Therefore, the noise figure in this case is called double-sideband noise figure. Usually single sideband noise figure will be 3dB higher than double sideband noise figure.

5.1.1.3. Non-linearity

There are two types of non-linearity that affects the receiver performance drastically. The first one is due to the active circuit's odd-order non-linearity (mainly third-order distortion) and it is characterized with input referred third order intercept point (IIP3). As shown in Fig. 5.3 (a), assuming two undesired interferences (f_1 and f_2) present at the mixer input, a distortion tone will be generated in $2f_2 - f_1 - f_{LO}$. If f_1 and f_2 are close to the desired signal, it can be proved that the generated distortion tone will be in the desired baseband. This happens not only for the direct conversion receivers but also in low-IF receivers.

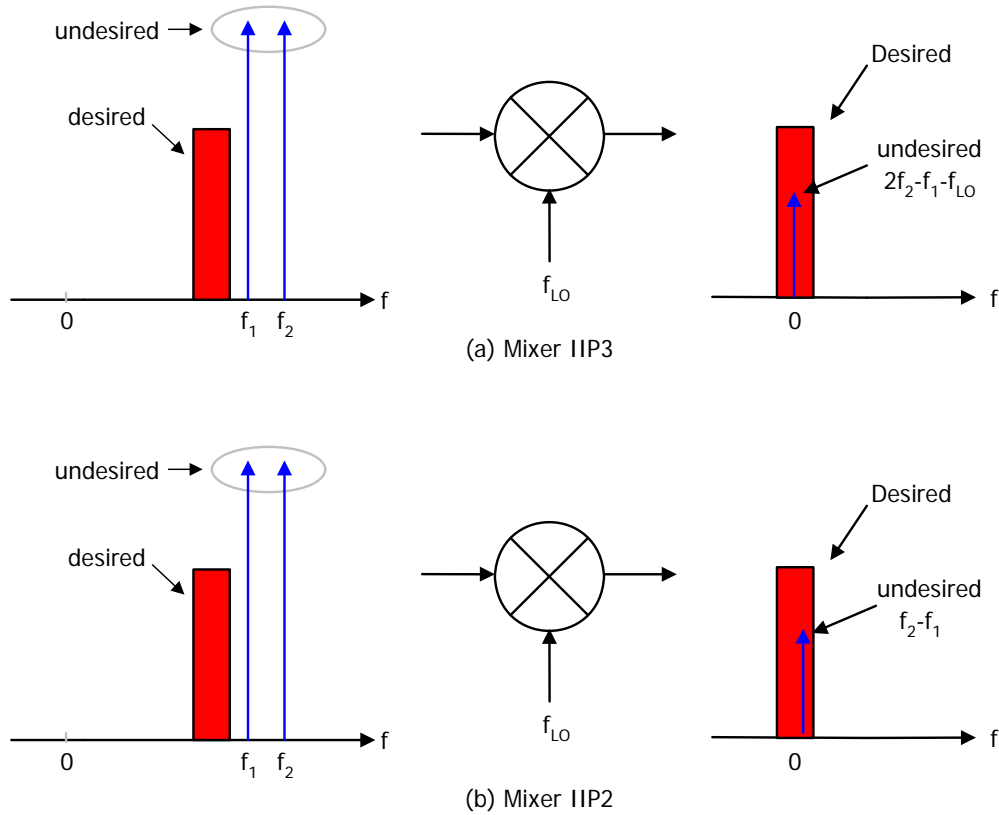


Fig. 5.3. Illustration of mixer IIP3 and IIP2

The second type of non-linearity is due to even-order distortion especially second-order, which is characterized as input referred second order inter-modulation (IIP2). As shown in Fig. 5.3 (b), two interferences (f_1 and f_2) in the mixer input may generate undesired distortion tone $f_2 - f_1$. And this distortion tone will be in the desired baseband if two input interferences are close to each other.

5.1.1.4. Dynamic range

Dynamic range is usually defined as the ratio of the maximum input level and minimum input level. For the RF receiver, the maximum input level is defined when the inter-

modulation tone is below output noise floor and the minimum input level is defined as the sensitivity level, as shown in Fig. 5.4. P_{\min} is the minimum input power level to ensure the output SNR above SNR_{\min} and P_{\max} is the maximum input power level which ensures output IP3 same as output noise floor. Clearly SFDR can be expressed as

$$SFDR = \frac{2}{3}(IIP3 - F) - SNR_{\min} \quad (30)$$

where $F = -174dBm + NF + 10\log B$ is the input referred noise floor; B is the signal bandwidth.

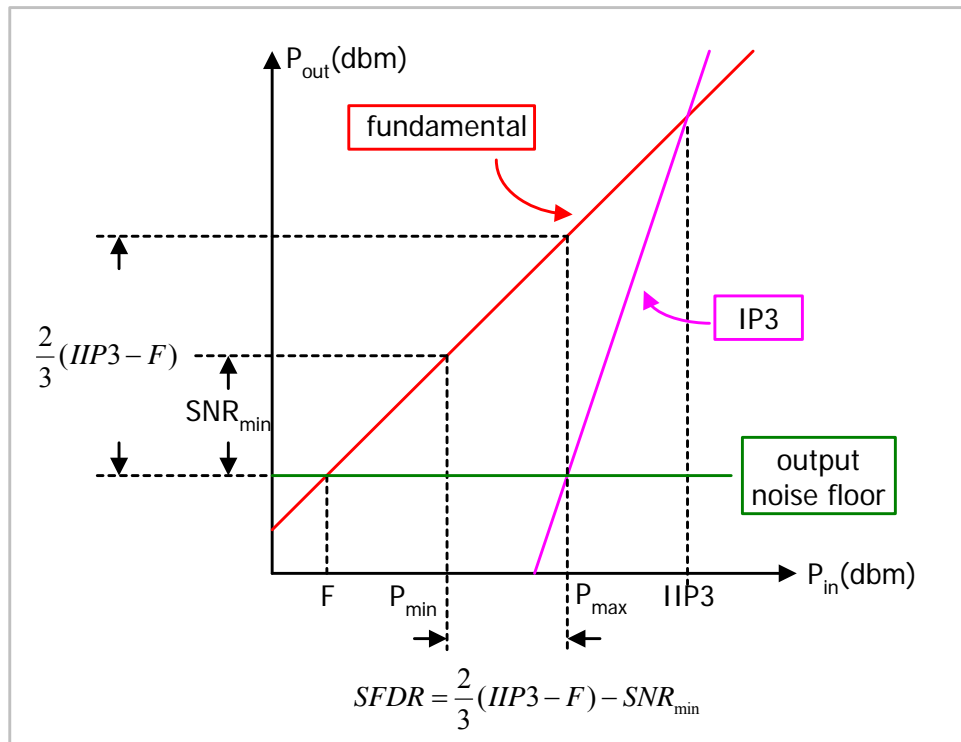


Fig. 5.4. Spurious-free dynamic range (SFDR) illustration

5.1.2. Mixer design specifications for DVB-H tuner

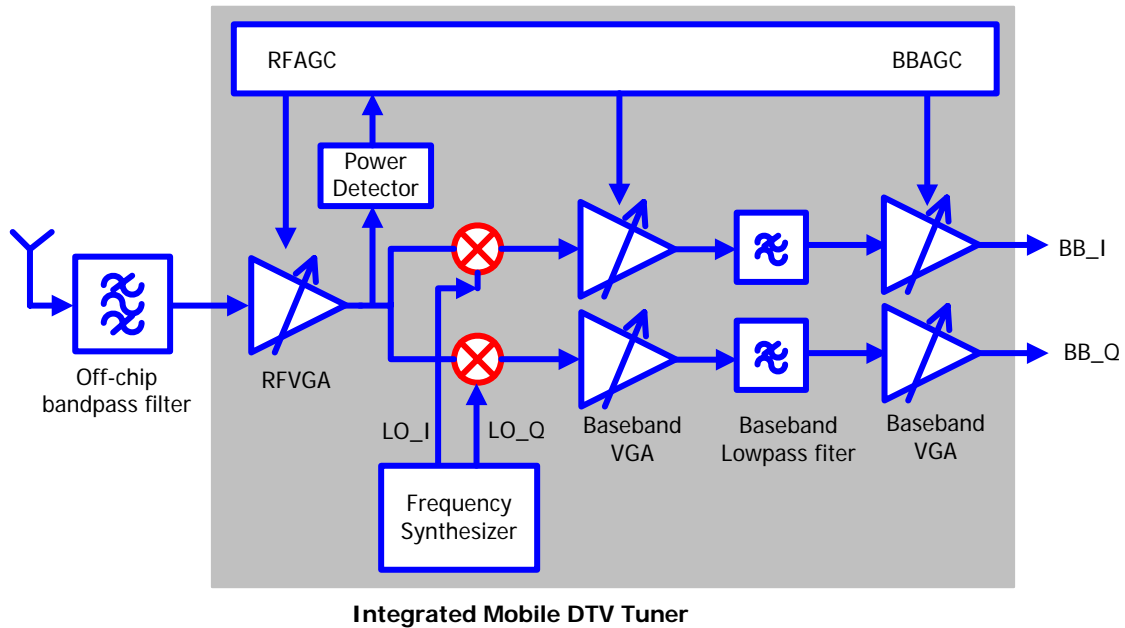


Fig. 5.5. DVB-H mobile tuner architecture

Table 5.1. Mixer design specifications

Conversion gain	12dB
NF	12dB
IIP3	15dBm
Flicker noise	minimum
I/Q mismatch	-35dBc
Single-differential conversion	Yes
IIP2	40dBm
Technology	CMOS 0.18 μ m
Power supply	1.8V

In this work, the mixer is designed for the integrated DVB-H tuner; the tuner architecture is shown in Fig. 5.5. The quadrature mixer needs to down-convert the RF channel between 470MHz and 870MHz baseband. The design specifications of the mixer are listed in Table 5.1. The conversion gain, noise figure and IIP3 have been derived in chapter III according to system excel budget link calculation. Other specifications will be derived below.

5.1.2.1. Flicker noise

The noise figure for the mixer we have derived is referred to thermal noise. Due to the random trapping of the charge at the oxide-silicon interface of MOSFETS, flicker noise becomes troublesome when CMOS design is utilized. In this design, the mixer's flicker noise must be smaller enough so that the majority of the noise is due to thermal noise. Alternatively, we need ensure flicker noise corner frequency is as low as possible.

5.1.2.2. I/Q mismatch

As discussed in chapter III, I/Q mismatch will degrades the output quality and it is necessary to ensure that the overall I/Q mismatch is always below -35dBc. Therefore, the mixer I/Q mismatch needs to be less 1.78%.

5.1.2.3. Single-differential conversion

The RFVGA is a single-ended configuration to save power consumption and remove off-chip balun. However, single-ended to differential conversion is required in the mixer stage

so that all the common mode noise due to substrate or power supply is suppressed. This conversion needs to be done as early as possible in the signal chain.

5.1.2.4. IIP2

The derivation of IIP2 for the system has been discussed in chapter III. It has been mentioned that there are two types of IIP2 generation. The first type is due to the RFVGA non-linearity and the leakage from RF to baseband. With fully balanced mixer design, the RF to baseband leakage can be further suppressed. More importantly, the even-order inter-modulation tone generated by the RFVGA is low frequency, which will be suppressed by the capacitive coupling between RFVGA and mixer. Therefore, this type of IIP2 can be ignored.

The second type of IIP2 is due to self-mixing and the mixer's own IIP2 performance. The self-mixing is mainly due to the coupling between RF and LO port, which can be suppressed with good layout technique such as guard rings or deep Nwell. For the mixer itself, the mismatch may cause IIP2. Anyway, the mixer's IIP2 can be derived based on equation below

$$IIP2 = P_u + (P_u - P_s + SNR_{\min} + 3) \quad (31)$$

where P_u is the power of the undesired interference and P_s is the power of the desired signal. The RFVGA is used before the mixer to control the maximum input power for the mixer to be less than -20dBm. Therefore P_u can be roughly assumed as -23dBm and the

desired signal power will be 40dBc lower. Considering the minimum SNR required is 25dB, the IIP2 can be calculated as 45dBm.

5.1.2.5. Power supply and technology

With even-reduced transistor minimum length, the power supply of the circuit is scaled down at the same time. For example, in the terrestrial tuner design, a 0.35 μ m CMOS technology is used and the power supply is 3.3V. While in this design, we use 0.18 μ m CMOS technology and the power supply is 1.8V. The reduction of the power supply will limit the maximum signal swing and overall gain. Therefore it is difficult to design high gain and high dynamic range circuits with low voltage supply. In this section, a circuit topology, suitable for low voltage operation, is proposed.

5.2. Current Mode Passive Mixer Topology

Various CMOS mixers used in wireless receivers have been reported in the literature, [27]-[41]. Most of those mixers belong to either active Gilbert mixer or voltage mode passive mixer. In this section, these two kinds of mixers are analyzed and compared with a proposed current mode passive mixer topology.

5.2.1. Active Gilbert mixer

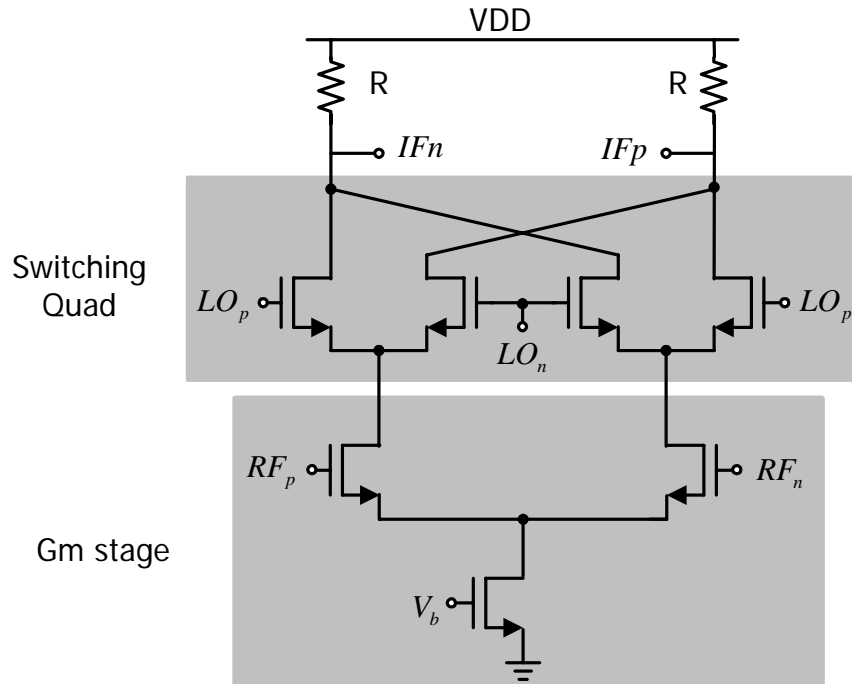


Fig. 5.6. Gilbert mixer schematic

The typical double balanced Gilbert mixer is shown in Fig. 5.6. On the bottom, usually a fully differential Gm stage is used to convert input RF voltage to current. The generated AC current is modulated by the switching quad, which is controlled by the LO signal. The resistor loads at the top convert the modulated current into voltage. When the switch is turned on, the switch serves as current switch, which means the transistor works in saturation region and operates as a cascode device. If ideal switching is assumed, the conversion gain of the mixer can be easily obtained as

$$G = \frac{2}{\pi} G_m R \quad (32)$$

where G_m is the overall transconductance of the bottom differential pair.

The mixer's noise and linearity performance have been further studied in [28]-[32]. In general, if square wave LO is assumed, the dominant thermal noise comes from the Gm stage and load resistors; the switching transistors are the main flicker noise contributor. The third order intermodulation (like IIP3) is mainly defined by the linearity performance of the Gm stage and the even-order distortion are mainly due to transistor mismatch and limited isolation between RF and LO port.

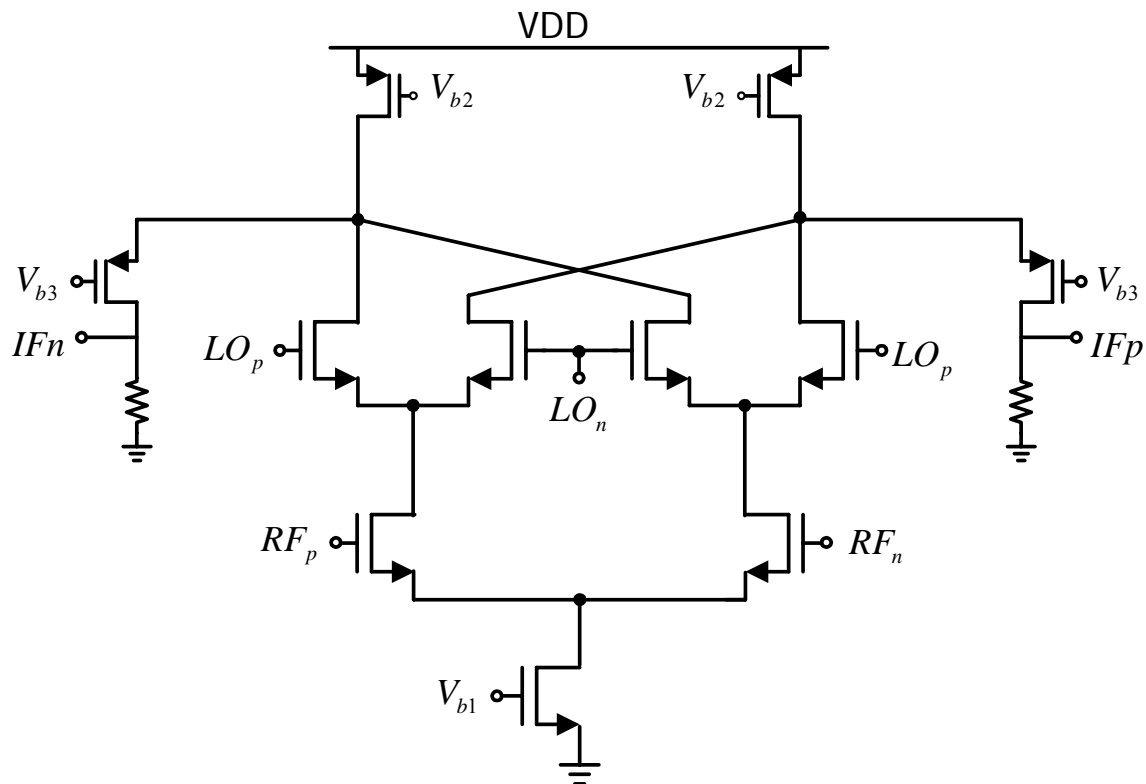


Fig. 5.7. Schematic of folded-cascode active load Gilbert mixer

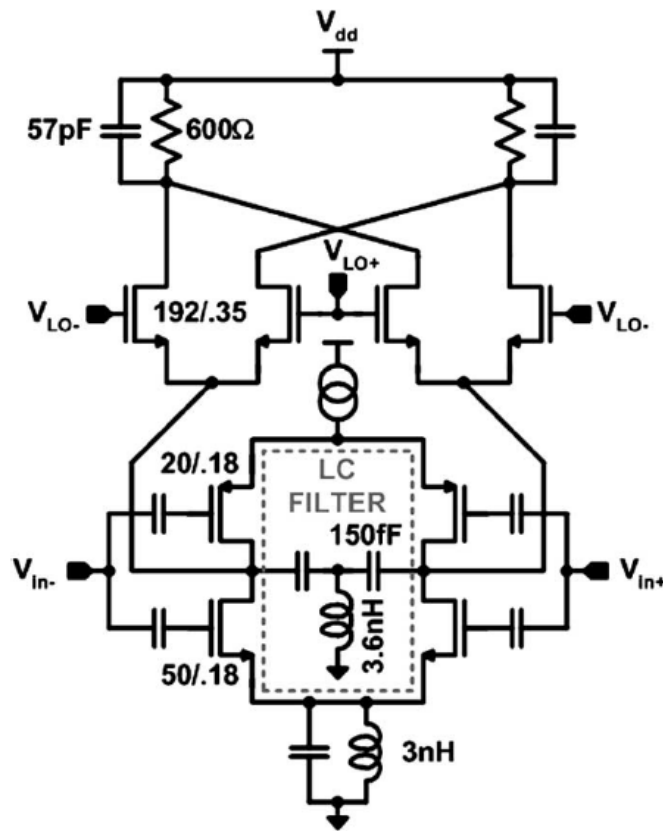


Fig. 5.8. Schematic of folded-switching mixer

In order to utilize this topology for direct conversion receiver, the main challenges will be high gain, high dynamic range, low flicker noise and low voltage operation. In order to achieve high linearity and low noise figure, huge DC current is required for the G_m stage. This DC current will not allow large resistor to be used as the load due to limited headroom. The large gain cannot be achieved with high dynamic range at the same time, especially with low voltage power supply. In order to prevent this constraint, folded-cascode active loads instead of resistor loads can be used, as shown in Fig. 5.7 [27]. This topology can achieve higher gain with huge DC currents but the extra current sources contribute more noise. Another topology called “folded switching” mixer was reported in [33]-[35]; the

schematic is shown in Fig. 5.8. In this topology extra PMOS Gm stage is added to subtract part of the DC current so that large resistor can be tolerated in the design for large gain. In addition, the current-reuse Gm stage effectively increases the overall Gm and reduces the input referred noise. However, due to reduced DC current in the switching pair, the impedance at the common source node becomes larger so that the overall noise and linearity may get worse, as reported in [29], [30] and [32].

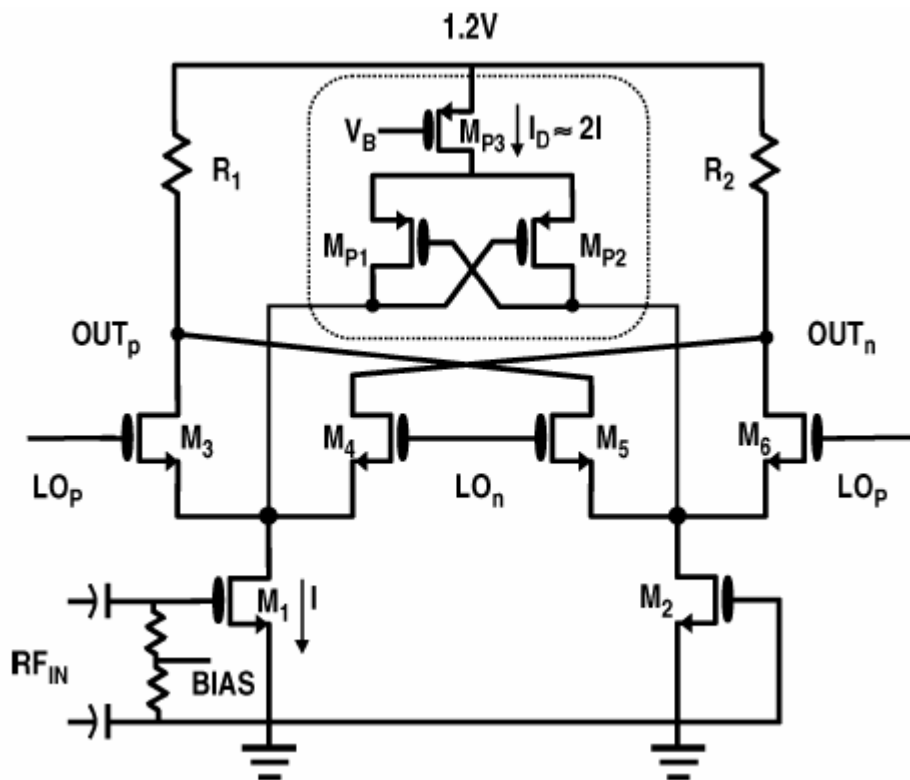


Fig. 5.9. Dynamic current injection Gilbert mixer

In the Gilbert mixer flicker noise is mainly generated by the switching transistor. According to [28], the practical way to reduce the flicker noise can be either reducing the switch transistor's gate referred flicker voltage noise or lowering the DC current flowing through

the switches. The first method implies large transistor size. However, the parasitic capacitor increases and the noise and linearity will be further affected by the internal pole [29]-[30]. Therefore there is limited room to increase the transistor size and the approach of reducing the DC current is preferred. For example, a folded switching mixer topology has been used in [35]. Since the DC current flows into the switching pair is reduced due to the subtraction of extra differential pair, the flicker noise will be reduced. However, the AC impedance at the common source node increases due to the reduced DC current, which increases the noise and distortion [29]-[30]. An interesting implementation was reported in [37], as shown in Fig. 5.9. With dynamic current injection, the DC current flowing through the switch pair will be subtracted only during the switching time. When the switch is fully turned on, the current injection is disabled and the impedance of the common source node remains same. Other approach, which explores to upconvert the flicker noise to higher frequencies, has been reported in [38]. Unfortunately that approach requires extra cascaded device and it is not suitable for low voltage operation

As a conclusion, although several techniques have been tried to increase the gain for low voltage operation and reduce the flicker noise, none of them meet the DVB-H design specifications at the same time. This is mainly because high dynamic range (15dBm IIP3 and 12dB NF) requires huge DC current, which limit the voltage gain even with the low voltage gain enhancement techniques. In addition, it is difficult to modify the flicker noise reduction topology to achieve such high dynamic range and gain.

5.2.2. Passive mixer

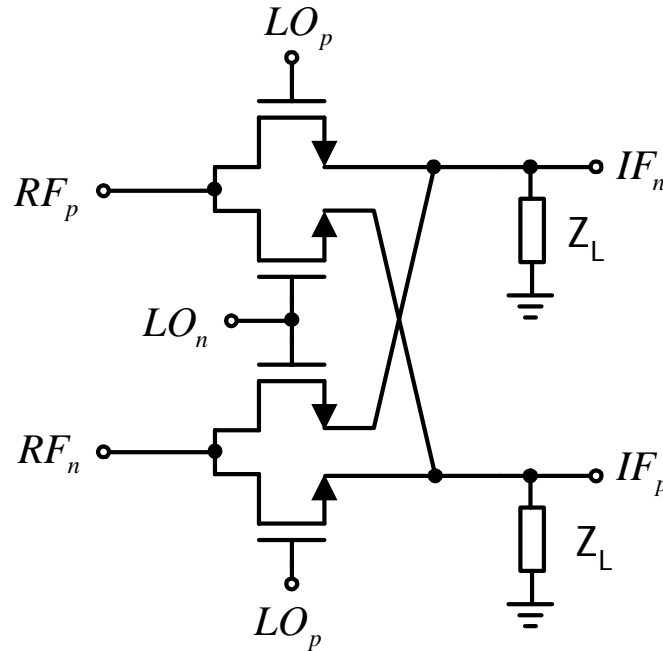


Fig. 5.10. Double balanced fully differential passive mixer

Fig. 5.10 shows the schematic of the double balanced fully differential passive mixer. The NMOS transistors work as a voltage switch and the load Z_L can be implemented as either resistor or capacitor. When the LO is high, the switch is turned on (working in the triode region) and the RF voltage input is sensed by the output; when the LO is low, the switch is turned off. If square wave LO is assumed, the conversion gain of the mixer can be obtained as

$$G = \frac{2}{\pi} \frac{Z_L}{R_{on} + Z_L} \quad (33)$$

where R_{on} is the switch on-resistance and Z_L is the load impedance. Usually R_{on} is relatively small compared with the load impedance, therefore the gain is around $-4\text{dB} \left(\frac{2}{\pi}\right)$ and that is the reason for being called passive mixer.

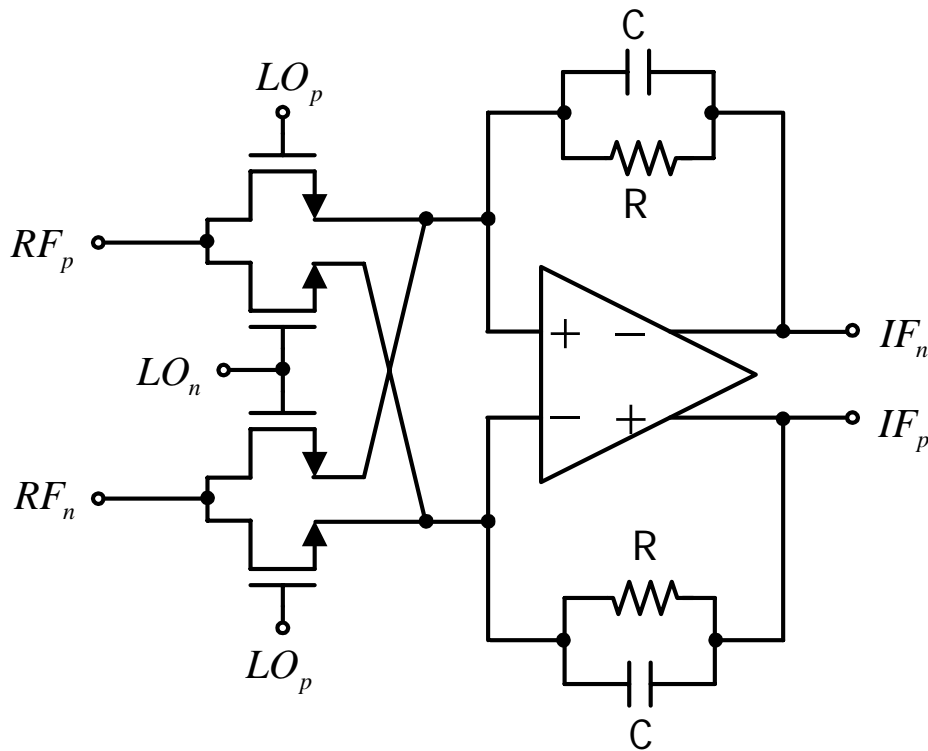


Fig. 5.11. Double balanced passive mixer with TIA load

Although the gain is less than 0dB, the passive mixer has multiple advantages. First of all, because no DC current flows through this switch transistor during the operation, in principle the mixer is free of flicker noise [39]-[40]. Another advantage is the inherent high linearity. Because when the switch is turned on, it works in the triode region, which is much more linear than the saturation region transistor.

In order to boost the gain of the passive mixer, several approaches have been reported. For example, single balanced instead of double balanced passive mixer is designed to boost the voltage conversion gain above 0dB, as reported in [40]. Notice that the gain is voltage gain not power gain, which doesnot violate the power conversion rule [40]. However, the gain is only 3dB, which is still not sufficient for most of the applications. Another popular way is to load the passive resistor with a trans-impedance amplifier (TIA), as shown in Fig. 5.11. In this topology, when the switch is on, the current flowing through the switch is absorbed by the feedback components and converted to voltage. Equivalently, when the switch is on, this circuit can be viewed as a first order active RC filter and the gain is defined by the ratio of feedback resistor and switch resistance. If ideal square wave LO is assumed, the conversion gain of the mixer can be obtained

$$G = \frac{2}{\pi} \frac{R}{R_{on}} \quad (34)$$

Comparing this configuration with the passive load, it can achieve higher conversion gain and other specifications such as noise and linearity will not be affected too much if proper design techniques are used. As a conclusion, it is a promising topology for typical direct conversion mixer design.

5.2.3. Current mode passive mixer

Although the TIA loaded passive mixer shown in Fig. 5.11 can achieve high gain, high dynamic range and low flicker noise, a major modification is still required when

considering the interface between RFVGA and mixer. The input impedance of the TIA loaded mixer is almost the switch resistance R_{on} ; and it is usually small (less than 100Ω) to minimize the switch thermal noise. Therefore, the gain of the RFVGA will be degraded. In addition, this mixer cannot take a single-ended input. As a conclusion, an extra buffer stage is required to drive the mixer and also provide the single-ended to differential conversion. Since the input impedance of this mixer is low, it is natural to drive it using current mode techniques. Instead of designing a voltage buffer, a transconductor is designed to achieve single-differential conversion and also drive the mixer. The schematic of the new mixer is shown in Fig. 5.12.

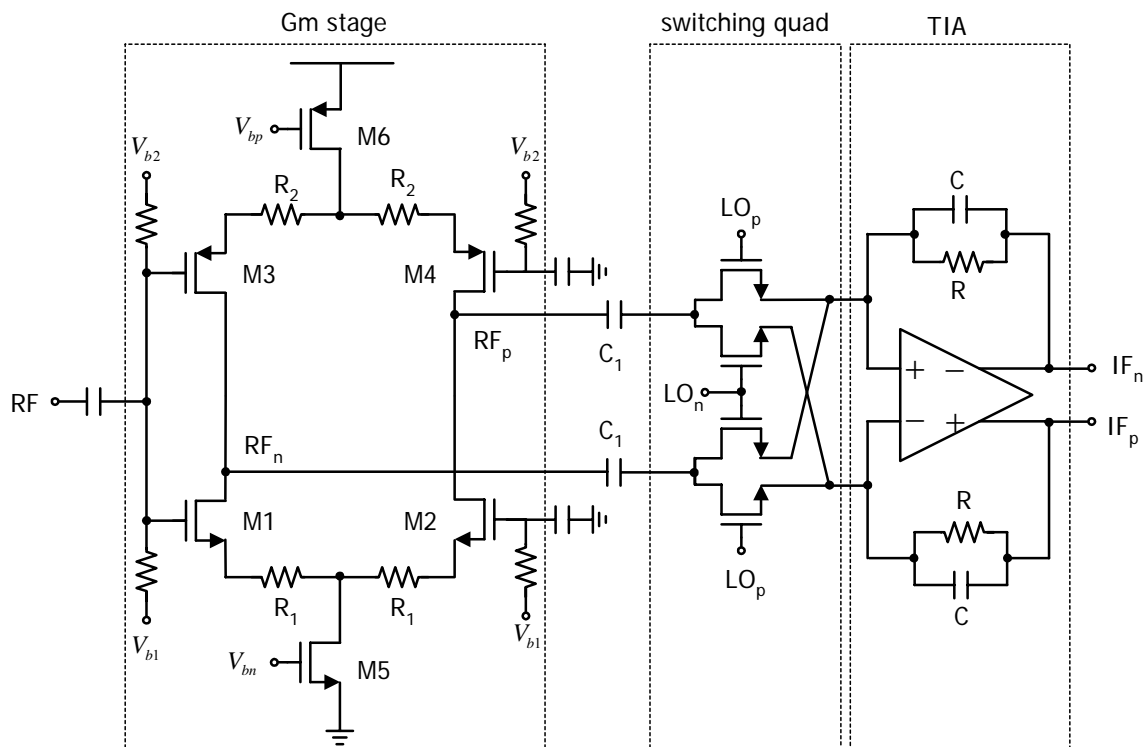


Fig. 5.12. Current mode passive mixer

The first stage of the mixer is a transconductor stage, which has several properties: i) the complementary NMOS and PMOS differential pairs increase the overall Gm for a fixed DC current and reduce the input referred noise voltage. Notice that DC bias voltages of the NMOS and PMOS differential pairs are different. In fact, to ensure the operation, V_{b1} is generated by a basic bias circuitry and V_{b2} is generated by a common mode feedback block (not shown in Fig. 5.12); ii) one of the inputs is connected to AC ground, which generates the differential output currents with a single-ended input voltage; iii) source degeneration is used to achieve highly linear voltage to current conversion.

The overall Gm can be obtained as

$$G_m = \frac{g_{m,N}}{1 + g_{m,N}R_1} + \frac{g_{m,P}}{1 + g_{m,P}R_2} \quad (35)$$

where $g_{m,N}$ and $g_{m,P}$ are the transconductance of the NMOS and PMOS differential pair transistors, respectively.

The second stage of the mixer is the switching quad and the operation is similar as that of the traditional passive mixer. The only difference is that the mixer input is AC current instead of voltage. The AC current from the Gm stage is capacitive coupled to switching quad, which helps to minimize the flicker noise and also reduce the even-order distortions generated from RFVGA and Gm stage.

The final stage of the mixer is the trans-impedance amplifier (TIA), which converts the current into voltage. The capacitive feedback provides first-order filtering. Proper resistor and capacitor values are chosen to achieve enough gain and also low input impedance. Due to the lackness of the filtering before this mixer, the in-band interference (in the frequency range of 470-890MHz) is down-converted to baseband (from DC to 420MHz) without any attenuation. It is necessary to keep the TIA input impedance low at least up to 420MHz. Otherwise huge voltage swing may be observed at the TIA inputs and degrade the non-linearity performance.

If square wave LO is assumed, the conversion gain of this mixer can be obtained as

$$G = \frac{2}{\pi} G_m R \quad (36)$$

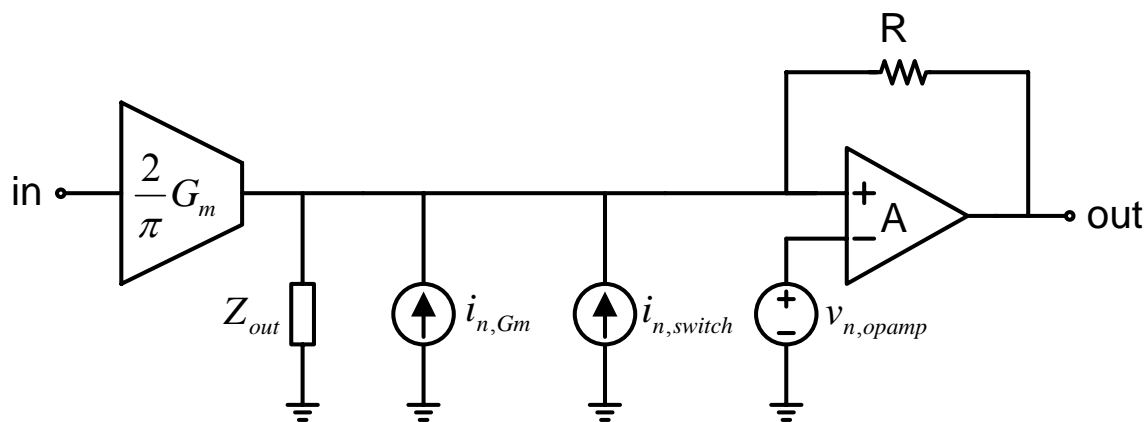


Fig. 5.13. Simplified mixer noise model

In order to analyze the noise performance, the mixer can be approximately modeled as shown in Fig. 5.13. The G_m and switch quad are modeled as a block, which has the output

impedance Z_{out} and overall transconductance $\frac{2}{\pi}G_m$. In ideal case, Z_{out} is very large.

However, when considering the parasitic ground capacitance from the output of the Gm stage to ground, a switch capacitor resistor will be observed due to the switch operation and the extra resistance may further degrade the output impedance Z_{out} , as reported in [40].

Nevertheless, for the desired frequency range (below 1GHz), it may not be critical and that effect is ignored. The noise contribution from Gm stage and switch can be modeled as current noise $i_{n,Gm}$ and $i_{n,switch}$ which were injected to the TIA input node. The OPAMP input referred noise voltage is modeled as $v_{n,opamp}$. Therefore the output noise can be obtained as

$$i_{n,out}^2 \approx (i_{n,Gm}^2 + i_{n,switch}^2)R^2 + \left(1 + \frac{R}{Z_{out}}\right)^2 v_{n,opamp}^2 \quad (37)$$

And the input referred noise can be obtained as

$$v_{n,in}^2 \approx \left(\frac{\pi}{2G_m}\right)^2 \left(i_{n,Gm}^2 + i_{n,switch}^2 + \left(\frac{1}{R} + \frac{1}{Z_{out}}\right)^2 v_{n,opamp}^2 \right) \quad (38)$$

Therefore, in order to minimize the overall noise, large overall Gm and large feedback resistor is preferred. Usually the OPAMP noise is not significant due to the feedback. Regarding the switch, it is better to maximize the switch-on resistance to minimize the current noise, which is different from the traditional voltage driven passive mixer.

In the analysis above, only the thermal noise is considered. For the flicker noise, due to the capacitive coupling between Gm stage and mixer, there is no DC current flowing through the switching quad and the flicker noise due to the switches is negligible. Therefore most of the flicker noise is generated by the OPAMP, which can be minimized with gate large area and proper circuit design.

The linearity of the mixer is determined by the nonlinearity of the Gm stage, the switching quad and the baseband TIA. The switching quad can be highly linear with large LO swing and the linearity of the TIA is superior due to the local feedback. In general, the nonlinearity will be mainly defined by the linear performance of the Gm stage.

From the discussions above, the advantages of the proposed mixer can be concluded as below:

- (1) High gain can be achieved even for low voltage power supplies. The gain of the mixer depends on the Gm and feedback resistor, which belong to separate stages and can be optimized for large gain even with 1V power supply.
- (2) High linearity and low noise figure can be achieved at the expense of the high power consumption. Unlike the Gilbert mixer, the huge DC current used in the input stage to increase the dynamic range will not limit the mixer gain.
- (3) The flicker noise is mainly determined by the OPAMP, which can be reduced because it operates at baseband.

5.3. Circuit Implementation and Simulation Results

5.3.1. Gm stage and switching quad

For the Gm stage design, large source degeneration factor is required to achieve over 15dBm IIP3 linearity. Also the overall Gm is designed to ensure small noise figure to meet the noise specification. The best way to achieve high linearity and low noise is to use large DC current. After several design iterations, the final design of the Gm stage is listed in Table 5.2. A simple common mode feedback for this Gm stage is used to control the PMOS tail current source. Otherwise, the Gm stage may not work properly.

Table 5.2. Gm stage design parameters

M1, M2	W=60 μ m, L=0.18 μ m
M3, M4	W=120 μ m, L=0.18 μ m
R1	100 Ω
R2	100 Ω
Tail current	3mA
Overall Gm	10mA/V
IIP3	15dBm

The switch is implemented using NMOS transistor (bulk connected to ground); the width of the transistor is 60 μ m. The switch uses minimum length 0.18 μ m to relax the design of LO driver. To achieve enough linearity the square wave LO is preferred and the LO swing is 0.8V peak-to-peak. The square wave LO is applied to the switch gate by using capacitive

coupling. In order to ensure the switch has identical turn on and turn off time, the gate DC voltage of the switches are properly biased, which is higher than the source DC voltage by V_T . The DC voltage of the source node is fixed by the common mode feedback of the OPAMP and it is around 0.8V. Hence, the gate DC bias voltage is 1.5V when considering $V_{th} = 0.7V$.

5.3.2. Trans-impedance amplifier

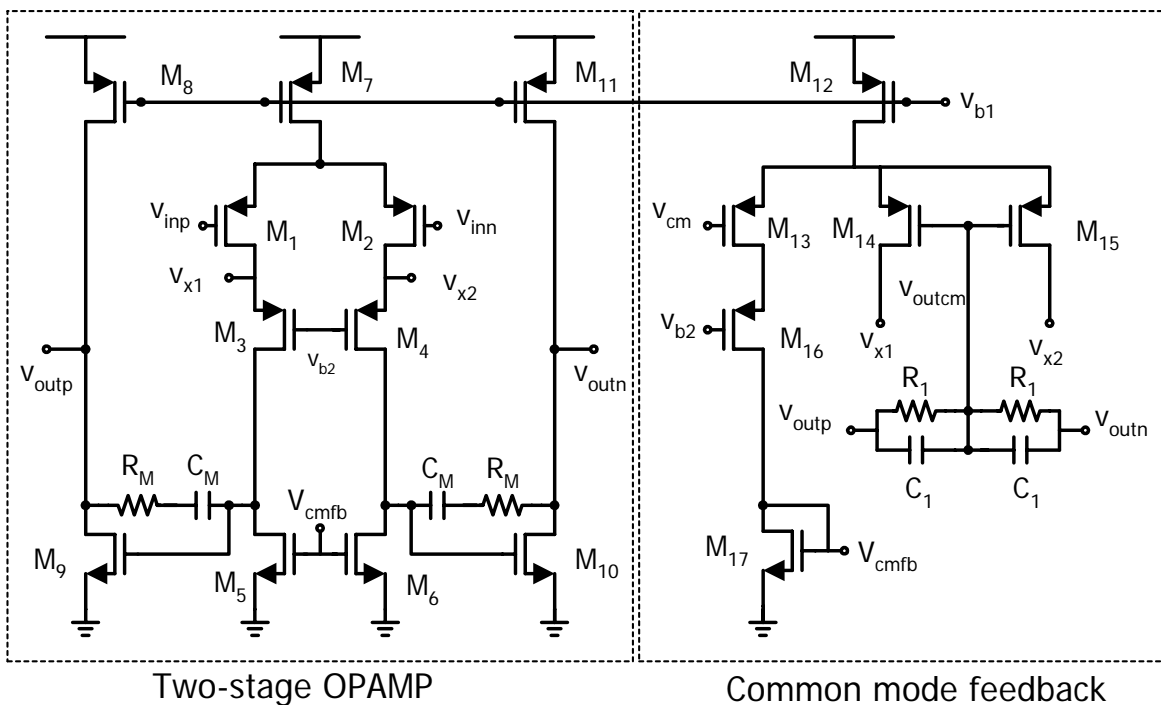


Fig. 5.14. Two-stage amplifier schematic

Regarding the OPAMP design, the main target is to provide more than 40dB gain at the edge of the channel (5MHz in the worst case). In addition, the thermal noise and flicker

noise must be minimized. The schematic of the two-stage amplifier with common mode feedback is shown in Fig. 5.14.

The first stage of the amplifier is designed with a PMOS type differential pair and NMOS type current source load. PMOS input stage is chosen because it gives better flicker noise performance. Cascode stage (M3 and M4) increase the first stage gain. The second stage of the OPAMP is a common source amplifier. Miller compensation is employed to ensure close-loop stability. The design procedure of this OPAMP can be found in [42].

The common mode feedback circuitry is required for this fully differential two-stage OPAMP mainly for two reasons. First, the output nodes of these two stages are high impedance nodes, the DC current mismatch between top and bottom (for example, M7 and M6) may affect the operation of the circuitry. Second, all of the common mode noise and interferences from previous stage or power supply can be suppressed.

For the implementation, the common mode output signal V_{outcm} is detected with a passive RC network. V_{outcm} is compared with a fixed voltage V_{cm} using differential pairs (M13, M14 and M15) and the common mode feedback control signal V_{cmfb} is generated to bias M5 and M6. In addition, V_{x1} and V_{x2} are connected to the sources of the M3 and M4. These extra connections ensure the common mode feedback loop to work even at start up [43]. In the extreme case, when V_{cmfb} is too small and transistor M17 is not operating, M5 (M6) does not work and the loop is broken. Since the DC current of M12 flows into M14

and M15 (eventually M5 and M6 due to the extra connections), M5 and M6 are turned on and the loop can be eventually activated.

Table 5.3. OPAMP design parameters

M1, M2	W=540 μ m, L=0.54 μ m
M3, M4	W=210 μ m, L=0.18 μ m
M5, M6	W=84 μ m, L=0.9 μ m
M7	W=1080 μ m, L=0.54 μ m
M8, M11	W=120 μ m, L=0.18 μ m
M9, M10	W=30 μ m, L=0.18 μ m
M12	W=360 μ m, L=0.54 μ m
M13	W=60 μ m, L=0.18 μ m
M14, M15	W=30 μ m, L=0.18 μ m
M16	W=60 μ m, L=0.18 μ m
M17	W=24 μ m, L=0.9 μ m
R_M	400 Ω
C_M	3pF
R1	20k Ω
C1	0.5pF
First stage DC current	2.25mA
Second stage DC current	1.8mA
CMFB DC current	0.75mA

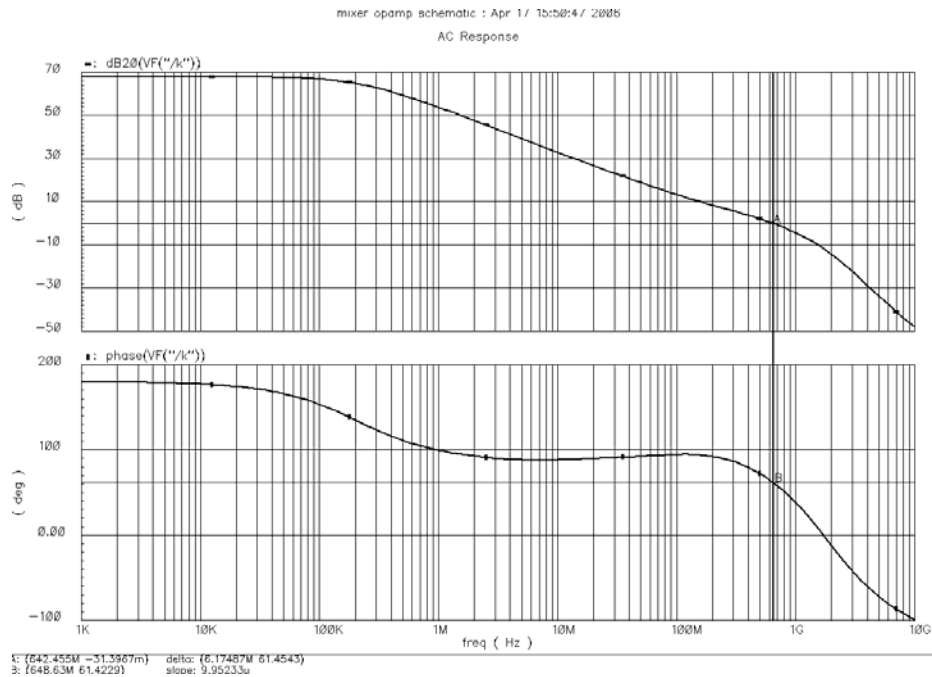


Fig. 5.15. OPAMP differential-mode open loop frequency response

The amplifier design parameters including transistor dimensions, DC current and passive component values are given in Table 5.3. The feedback resistor and capacitor are 2k and 15pF, respectively. The differential-mode open loop frequency response of the OPAMP has been simulated when it is loaded with the 2k resistor and 15pF capacitor, as shown in Fig. 5.15. The OPAMP has a GBW of 648MHz and the phase margin is 61 degree; the gain at 5MHz is around 42dB, which is enough for our application. In order to ensure the common-mode stability, the common mode feedback loop is broken at the V_{outcm} node and the open loop frequency response is simulated and given in Fig. 5.16. The open loop unity gain frequency is around 350MHz and the phase margin is around 40 degree. The OPAMP input referred noise has also been simulated and depicted in Fig. 5.17; the input referred thermal noise voltage spectral density is $21.9\text{nV}/\sqrt{\text{Hz}}$ and the flicker noise corner frequency is

around 533 kHz. For the complete TIA, the input impedance is always less than 40Ω from DC up to 1GHz and less than 10Ω from DC up to 10MHz.

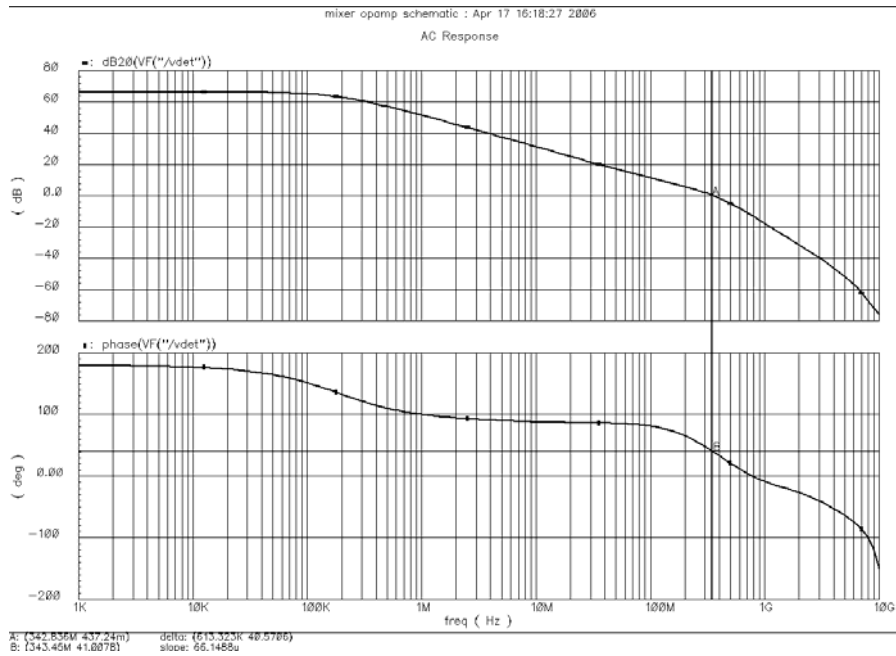


Fig. 5.16. OPAMP common mode feedback open loop frequency response

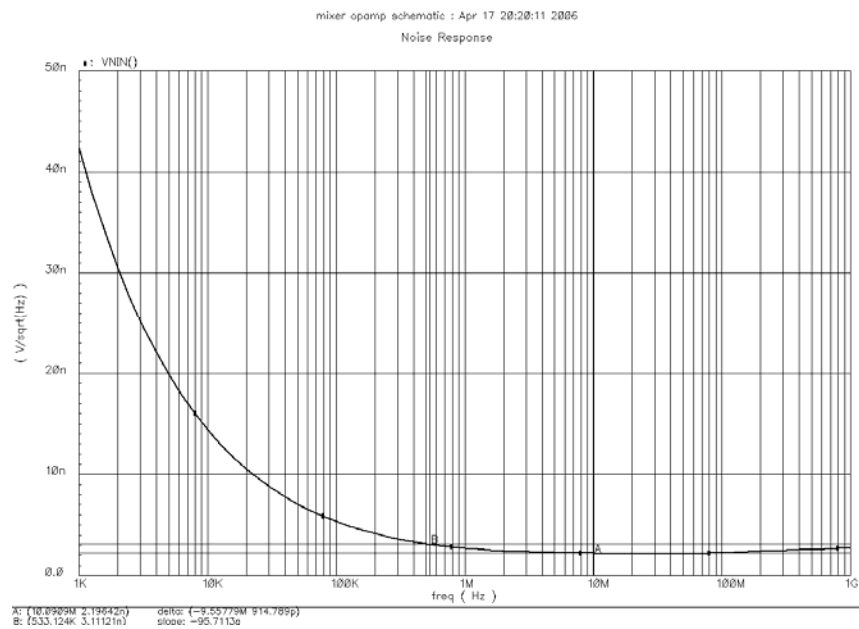


Fig. 5.17. OPAMP input referred noise voltage spectral density plot

5.3.3. Mixer simulation results

The complete mixer specifications have been simulated and the main results are listed in Table 5.4. Those simulation results meet the design specifications except the linearity. IIP3 is slightly less than the desired 15dBm mainly because the 800mV peak-peak LO limits the switch linearity. It is difficult to increase the LO swing because it consumes much more power consumption for the LO driver. In addition, the overall tuner IIP3 only degrades by 1dB, which is tolerable for the system. The mixer power consumption is 15mW and for the entire quadrature mixer it will be 30mW.

Table 5.4. Mixer simulation results

Conversion gain	18dB
NF	11.6dB
IIP3	12dBm
Flicker noise corner frequency	62kHz
Power consumption	15mW
Technology	CMOS 0.18 μ m
Power supply	1.8V

5.4. Conclusions

In direct conversion DVB-H tuner system, the high gain, low noise figure, low flicker noise and high linearity CMOS mixer is required, which is challenging when the technology is scaled down and low voltage power supplies are used. After the review of available down-conversion CMOS mixer topologies, it was concluded that none of them can achieve all

specifications at the same time, especially when the power supply is only 1.8V. Therefore, a novel current mode passive mixer topology is proposed. It allows the high gain high dynamic range specifications to be achieved with low power supply (1.8V and even below). In addition, because the switching core is free of DC current, the mixer can achieve low flicker noise. To demonstrate the concept, the mixer has been designed with TSMC 0.18 μ m CMOS technology and it meets the DVB-H tuner specifications.

CHAPTER VI

CONCLUSIONS

DTV tuner is one of the most critical blocks of the DTV receiver system and the main design target is low-power and low-cost. The fully integration with mainstream CMOS technology is preferred. In this dissertation, the design efforts have been focused on the tuner system level and novel RF front-end block level implementations. Two different tuner architectures and RF front-ends have been designed for the ATSC terrestrial DTV and DVB-H mobile DTV systems.

In the terrestrial DTV tuner design, a novel double quadrature low-IF tuner architecture is proposed. The main advantage of the proposed architecture is to get rid of the bulky and expensive off-chip SAW filter and to provide a fully integrated solution, which cannot be achieved with the conventional approaches. In addition, this architecture allows the tuner to get similar specifications with less power consumption. A double quadrature down-converter, which is the most critical RF front-end block for the proposed tuner architecture, has been designed with TSMC 0.35 μ m CMOS technology. Achieving more than 40dB image rejection ratio with less than 200mW, the test chip fully demonstrated the proposed concepts.

For the mobile DTV tuner, the most challenging specification is low power consumption because of the limited handset battery life. A zero-IF tuner architecture was employed and the complete system and block specifications were derived. The RF front-end, including the

RFVGA and down-conversion mixer, has been designed with TSMC 0.18 μm CMOS technology. A novel RFVGA architecture has been proposed to achieve high dynamic range and robust input impedance matching for the entire DTV band. By doing so, this RFVGA prevents the usage of additional fixed gain low noise amplifier or off-chip low noise amplifier. Comparing with the conventional implementations, this implementation reduces the noise figure by more than 1.5dB. The design challenge for the down-conversion mixer is the high gain, high dynamic range specifications with only 1.8V power supply. Implementing the mixer through three stages (transconductor, passive switching quad, and trans-impedance amplifier), the proposed current-mode passive mixer can achieve over 12dB gain, less than 12dB noise figure, 12dBm IIP3 with 15mW power consumption. In addition, this down-conversion mixer demonstrated superior flicker noise performance (less than 100 kHz corner frequency).

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VITA

Jianhong Xiao was born in Taixing Country, Jiangsu Province, P. R. China in 1979. He received his B.Sc. degree from Department of Computer Science and Technology, Peking University, Beijing, China in July 2001. In September 2001, he joined Analog and Mixed-signal Center, Department of Electrical and Computer Engineering, Texas A&M University, College Station, Texas to pursue his Ph.D. degree. He worked at Analog Devices as design engineer intern for the low-power low-cost DTV tuner design in 2004 summer and fall and 2005 summer. His main research interests cover system design and RF front-end circuit design for broadband communication systems. He can be reached through the Department of Electrical and Computer Engineering, Texas A&M University, College Station, Texas 77843.